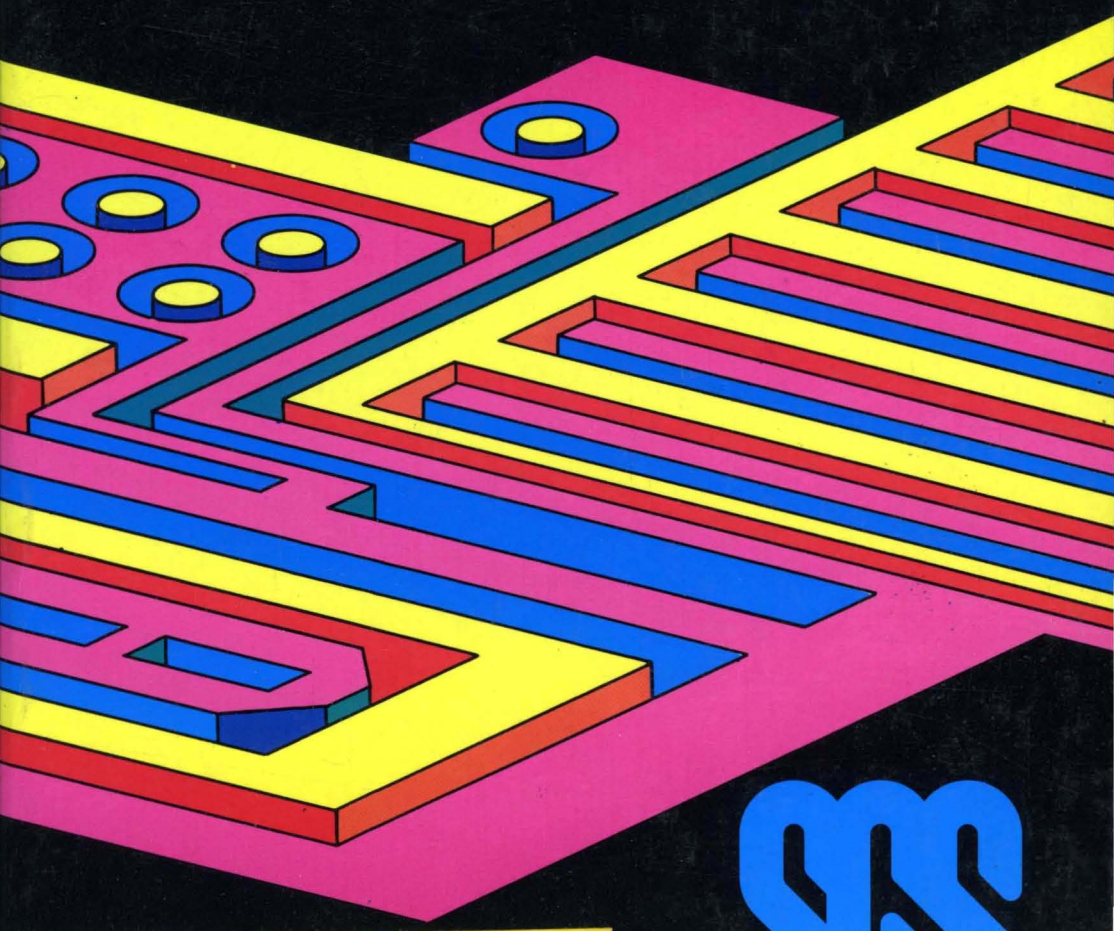
DATABOOK

LINEAR INTEGRATED CIRCUITS

3rd EDITION



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LINEAR INTEGRATED CIRCUITS

3rd EDITION

ISSUED JUNE 1982

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of linear integrated circuits for professional, industrial and consumer applications.
Selection guides are provided in the following pages to facilitate rapid identification of the most suitable device for the intended use.
The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.

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APPLICATION GUIDE: CONSUMER CIRCUITS

TV

FUNCTION		DEVICE
Complete sound channel		TDA1190Z TDA2190 TDA3190
Deflection	Horizontal	TDA1180P
Deflection	Vertical	TDA1170 TDA1170D TDA1170N TDA1170S TDA1470 TDA1670 TDA1770 TDA2170
Video IF system		TDA440S TDA4420
Chroma	Oscillator	TDA2140
Chroma	Lumin. & Chromin.	TDA2151
Chroma	Demodulator	TDA2161
TV signal identification		TDA4431 TDA4433
Varicap supply		TAA550A TAA550B TAA550C
TV channels display driver		TDA4092

Preamplifiers

FUNCTION	DEVICE
General purpose	TBA231A
Tape	TDA1054M TDA2054M TDA3410 TDA3420
Hi-Fi	TDA2310
Infrared receiver	TDA2320
Stereo preamplifier	TDA2320A

Tape Recorders

FUNCTION	DEVICE
DC Motor Regulators	TCA900 TCA910 TDA1151
Multifunction	TDA7270S

Audio Power Amplifiers

APPLICATION	DEVICE
Car radio	TBA810P TBA810S TBA810CB TDA2002 TDA2003 TDA2004 TDA2005
Portable radio	TAA611A TAA611B TAA611C TBA820 TBA820M TDA1904 TDA1905
TV receiver	TBA800 TCA940N TDA1904 TDA1905 TDA1908 TDA2006 TDA2008 TDA2009
Hi-Fi and Hi-Fi TV	TDA1910 TDA2009 TDA2010 TDA2020 TDA2030 TDA2030A TDA2040
Driver	TDA2020D TDA2030A

Radio

FUNCTION	DEVICE
IF/FM radio system	TCA3089 TCA3189 TDA1200
AM/FM radio	TDA1220A TDA1220B TDA1220L

Transistor Array

FUNCTION	DEVICE
NPN array	LS159 TBA331

APPLICATION GUIDE: PROFESSIONAL CIRCUITS

Operational Amplifiers

FUNCTION	DEVICE
Single general purpose	LS107/207/307 LS141/A/C LS148/A/C LS709/A/C
Single high performance	LS101/201/301
Programmable	LS776/C
Dual general purpose	MC1458/C
Dual high performance	LS204/A/C LS4558N
Quad general purpose	LM324/A LM2902
Quad high performance	LS404/C

Telecommunications Circuits

FUNCTION	DEVICE
Balanced modulator	LS025
Channel amplifier	LS045
Compandor	LS150
Telephone speech circuit	LS156 LS285/A LS288 LS356 LS656
Multifrequency interface	LS342
Op-amps for active filter	LS204 LS404

Positive Voltage Regulators

FUNCTION	DEVICE
Positive fixed	L7800 series L78M00 series L78S00 series
Negative fixed	L7900 series
With integrated bridge	L194 series
Adjustable	L123 L146 L200 LM117/217/317
Automotive	L2600 series
Very low drop	L487

Industrial Circuits

FUNCTION	DEVICE
Power operational amplifier	L165
DC motor positioning system	L290 L291 L292
DC and stepping motor driver	L293 L293E
Switch-mode solenoid driver	L294
Printer solenoid driver	L3654
Quad comparator	LM339
Darlington array	L201/2/3/4 L601/2/3/4 L702
Current boosters	L149 TDA1410A TDA1420A TDA1420L
Triac/SCR control	L120A L121A

AUDIO POWER AMPLIFIERS

Selection table (test conditions; d = 10%, f = 1 kHz)

Supply (V)	Device	Output Power (W)			
		$R_L = 2\Omega$	$R_L = 4\Omega$	$R_L = 8\Omega$	R_L = ...
4	TBA820M		0.35		
6	TAA611A		0.5	0.35	
	TBA810S		1		
	TBA820M		0.75	0.45	
	TDA1904		0.8		
9	TAA611A		1.8	1.15	
	TAA611B		1.8	1.15	
	TBA810P	3.4	2.5		
	TBA820		1.6	1.2	
	TBA820M		1.6	1.2	
	TDA1904		2.2		
	TDA1905		2.5	1.3	
12	TAA611B			2.1	
	TAA611C		3	2.1	
	TBA820			2	
14.4	TBA810CB	7	6		
	TBA810P	7	6		
	TDA1904		4.5		
	TDA1905		5.4	3	
	TDA1908		5.8	3	
	TDA2002	8	5.2		
	TDA2003	10	6		12 } R_L=1.6Ω
	TDA2004	2x10	2x6.5		2x11 } R_L=1.6Ω
	TDA2005	2x10	2x6.5 (°)		2x11 } R_L=1.6Ω
18	TBA800			4.5	
	TCA940N		9	5	
	TDA1905			5.5	
	TDA1908		9	5	
22	TDA2008		12	8	
23	TDA2009		2x10	(°)	
24	TBA800				5 } R_L=16Ω
	TDA1905				5.3 } R_L=16Ω
	TDA1908				5 } R_L=16Ω
	TDA2006		12	8	
28	TDA2010*		12	9	
	TDA2030*		14	9	
32	TDA2030A*		18	12	
	TDA2040*		22	12	
36	TDA2020*		20	–	

(°) 20W in Bridge

(*) d = 0,5%, f = 1 KHz.

OPERATIONAL AMPLIFIERS

Device	Temperature Range (°C)	Frequency compensat.	CMRR (dB)	Input Bias Curr. (nA)	Slew Rate (V/μs)	Max supply Voltage (V)	Package
LS101T	-55 to 125		90	120	10	± 22	TO-99
LS101AT	-55 to 125		96	30	10	± 22	
LS107T	-55 to 125	●	96	30	0.7	± 22	
LS141T	-55 to 125	●	90	80	0.5	± 22	
LS141AT	-55 to 125	●	95	30	0.7	± 22	
LS141CT	0 to 70	●	90	80	0.5	± 18	
LS148T	-55 to 125		90	80	5.5	± 22	
LS148AT	-55 to 125		95	20	5.5	± 22	
LS148CT	0 to 70		90	80	5.5	± 22	
LS201T	0 to 70		90	250	10	± 22	
LS201AT	-25 to 85		96	30	10	± 22	
LS207T	-25 to 85	●	96	30	0.7	± 22	
LS301AT	0 to 70		90	70	10	± 18	
LS307T	0 to 70	●	90	70	0.5	± 18	
LS709T	-55 to 125		90	200	0.25	± 18	
LS709AT	-55 to 125		110	100	0.25	± 18	
LS709CT	0 to 70		90	300	0.25	± 18	
LS776T	-55 to 125	●	90	15	0.35	± 18	
LS776CT	0 to 70	●	90	15	0.8	± 18	
LS204T*	-25 to 85	●	100	50	1.5	± 18	
LS204AT*	-55 to 125	●	100	50	1.5	± 18	
LS204CT*	0 to 70	●	95	80	1	± 18	
LS141CM.	0 to 70	●	90	80	0.5	± 18	Minidip
LS148CB	0 to 70		90	80	5.5	± 22	
LS201B	0 to 70		90	250	10	± 22	
LS301AB	0 to 70		90	70	10	± 18	
LS307B	0 to 70	●	90	70	0.5	± 18	
LS776CB	0 to 70	●	90	15	0.8	± 18	
LS204CB*	0 to 70	●	95	80	1	± 18	
LS4558NB*	0 to 70	●	90	50	1.5	± 18	
MC1458P1*	0 to 70	●	90	80	0.5	± 18	
MC1458CP1*	0 to 70	●	90	80	0.5	± 18	
LS141CM	0 to 70	●	90	80	0.5	± 18	SO-8
LS148CM	0 to 70		90	80	5.5	± 22	
LS201M	0 to 70		90	250	10	± 22	
LS301AM	0 to 70		90	70	10	± 18	
LS307M	0 to 70	●	90	70	0.5	± 18	
LS776CM	0 to 70	●	90	15	0.8	± 18	
LS204M*	-25 to 85	●	100	50	1.5	± 18	
LS204CM*	0 to 70	●	95	80	1	± 18	
LS4558NM*	0 to 70	●	90	50	1.5	± 18	
MC1458M*	0 to 70	●	90	80	0.5	± 18	
MC1458CM*	0 to 70	●	90	80	0.5	± 18	
LM324N**	-25 to 85	●	70	45		32	DIP
LM324AN**	-55 to 125	●	85	45		32	
LM2902N**	0 to 70	●	70	45		32	
LS709CB	0 to 70		90	300	0.25	± 18	
LS404CB**	0 to 70	●	90	100	1	± 18	
LM324CM**	-25 to 85	●	70	45		32	SO-14
LM2902CM**	0 to 70	●	70	45		32	
LS404M**	-25 to 85	●	94	50	1	± 18	
LS404CM**	0 to 70	●	90	100	1	± 18	

* Dual ** Quad.

POSITIVE VOLTAGE REGULATORS

I_O max (A)	Device	Regulated output voltage (V)												Package
		5	6	7.5	8	8.5	9	10	12	15	18	20	24	
2	L200CH/CV	2.9 ← ADJUSTABLE → 36												Pentawatt®
	L200CT/T	2.9 ← ADJUSTABLE → 36												TO-3 (4-lead)
	L78S00CV	●		●			●	●	●	●	●		●	Versawatt
	L78S00CT/T	●		●			●	●	●	●	●		●	TO-3
1.5	LM117K	1.2 ← ADJUSTABLE → 37												TO-3
	LM217K	1.2 ← ADJUSTABLE → 37												TO-3
	LM317K	1.2 ← ADJUSTABLE → 37												TO-3
	LM317T	1.2 ← ADJUSTABLE → 37												Versawatt
1	L7800CV	●	●		●				●	●	●	●	●	Versawatt
	L7800CT/T	●	●		●				●	●	●	●	●	TO-3
0.5	L2600V	●				●		●						Versawatt
	L78M00CV	●	●		●				●	●	●	●	●	Versawatt
	L194-5V*	●												Pentawatt®
	L194-12V*								●					Pentawatt®
	L194-15V*									●				Pentawatt®
	L487	●												Pentawatt®
0.15	L123CB	2 ← ADJUSTABLE → 36												P001-A
	L123CT/T	2 ← ADJUSTABLE → 36												TO-100
	L146CB	2 ← ADJUSTABLE → 77												P001-L
	L146CT/T	2 ← ADJUSTABLE → 77												TO-100

* With integrated rectifying bridge.

NEGATIVE VOLTAGE REGULATORS

I_O max (A)	Device	Regulated output voltage (V)								Package
		-5	-5.2	-8	-12	-15	-18	-20	-24	
1	L7900CV	●	●	●	●	●	●	●	●	Versawatt
	L7900CT/T	●	●	●	●	●	●	●	●	TO-3

Device	Function	Package	$V_{S\ MAX}$ (V)	NOTES
TAA 550	TV VOLTAGE STABILIZER	TO-18	–	V_Z = 30V to 36V, $I_{Z\ (max)}$ = 20 mA
TAA 611A	1.8W AUDIO AMPLIFIER	14-DIP/TO-100	12	P_O = 1.8W (9V - 4Ω), P_O = 1.15W (9V - 8Ω)
TAA 611B	2.1W AUDIO AMPLIFIER	14-DIP	15	P_O = 2.1W (12V - 8Ω), P_O = 1.15W (9V - 8Ω)
TAA 611C	3.3W AUDIO AMPLIFIER	14-DIP	22	P_O = 3.3W (15V - 8Ω), P_O = 1.7W (12V - 8Ω)
TBA 820	2W AUDIO AMPLIFIER	14-DIP	16	P_O = 2W (12V - 8Ω), P_O = 1.2W (9V - 8Ω)
TCA 830S	3,4W AUDIO AMPLIFIER	FIN-DIP	20	P_O = 3.4W (12V - 4Ω), P_O = 2.3W (12V - 8Ω)
TDA 1200	FM-IF RADIO SYSTEM	16-DIP	16	See TCA 3089
TDA 1410A	QUASI COMPLEMENTARY DUAL DARLINGTON	PENTAWATT®	36	$h_{FE} > 800$ @ 2A
TDA 1420A		PENTAWATT®	44	$h_{FE} > 500$ @ 3A
TDA 1420L		PENTAWATT®	40	$h_{FE} > 800$ @ 2A
TDA 2140	KIT CHROMA	16-DIP	15	
TDA 2151		16-DIP	15	
TDA 2161		16-DIP	15	
TDA 3310	LOW-NOISE NPN TRANSISTORS ARRAY	14-DIP	20	$h_{FE} > 300$ @ 100 μA, NF = 0.5 dB
TDA 7770	MULTIFUNCTION SYSTEM FOR TAPE RECORDERS	FIN-DIP	20	Motor speed regulator, Bias Oscillator, DC record-play switching, Automatic stop.

PRECAUTIONS FOR PHYSICAL HANDLING OF POWER LINEAR ICs

When mounting power ICs certain precautions must be taken in operations such as bending of leads, mounting of heatsink, soldering and removal of flux residue. If these operations are not carried out correctly, the device can be damaged or reliability compromised.

1. **Bending and cutting leads**
   The bending or cutting of the leads requires the following precautions:

1.1 When bending the leads they must be clamped tightly between the package and the bending point to avoid strain on the package (in particular in the area where the leads enter the resin) (fig. 1). This also applies to cutting the leads (fig. 2).

1.2. The leads must be bent at a minimum distance of 3 mm from the package (fig. 3a).

1.3. The leads should not be bent at an angle of more than 90° and they must be bent only once (fig. 3b).

1.4. The leads must never be bent laterally (fig. 3c).

1.5. Check that the tool used to cut or form the leads does not damage them or ruin their surface.

Fig. 1 - Bending the leads

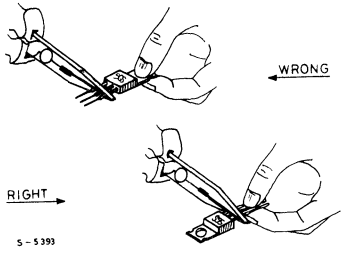


Fig. 2 - Lead forming or cutting mechanism

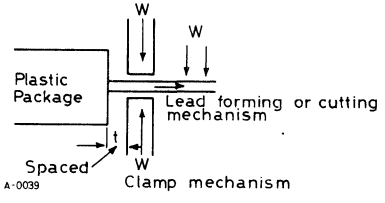
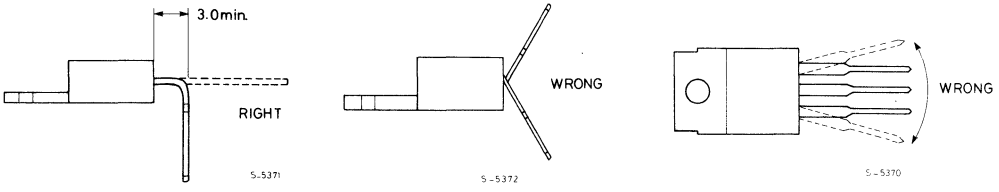


Fig. 3 - Angles for lead wire bending



2. Mounting on printed circuit

During mounting operations be careful not to apply stress to the integrated circuit.

2.1. Adhere strictly to the pin spacing of the IC to avoid forcing the leads.

2.2. Leave a suitable space between printed circuit and integrated circuit, if necessary use a spacer.

2.3. When fixing the device to the printed circuit do not put mechanical stress on the IC. For this purpose the device should be soldered to the printed circuit board after the IC has been fixed to the heatsink and the heatsink to the printed circuit board.

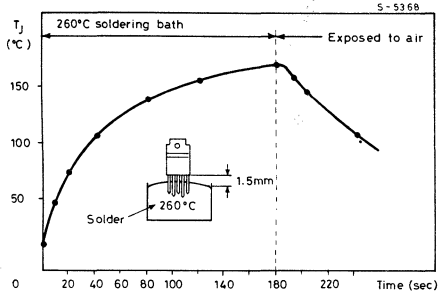
3. Soldering

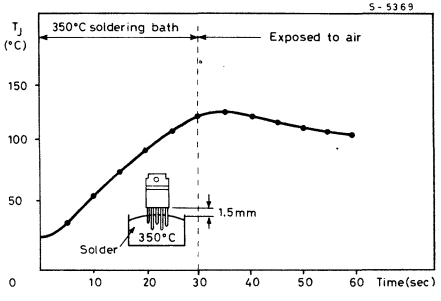
In general an IC should never be exposed to high temperatures for any length of time. It is therefore preferable to use soldering methods where the IC is exposed to the lowest possible temperatures for a short time.

3.1. Tolerable conditions are 260°C for 10 sec or 350°C for 3 sec. The graphs in fig. 4 give an idea of the excess junction temperature during the soldering process for a TO-220 (Versawatt). It is also important to use suitable fluxes for the tin baths to avoid deterioration of the leads or of the package resin.

3.2. An excess of residual flux between the pins of the integrated circuit or in contact with the resin can reduce the long-term reliability of the device. The solvent for removing excess flux must be chosen with care.
The use of solvents derived from trichloroethylene is not recommended on plastic packages because the residue can cause corrosion.

Fig. 4 - Junction temperatures during soldering



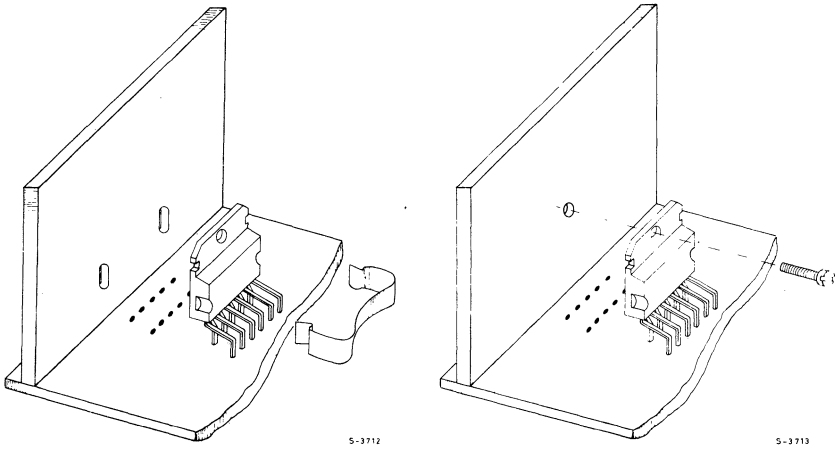


4. Mounting of heatsink

To exploit best the performance of power ICs a heatsink with R_{th} suitable for the power that the IC will dissipate must be used.

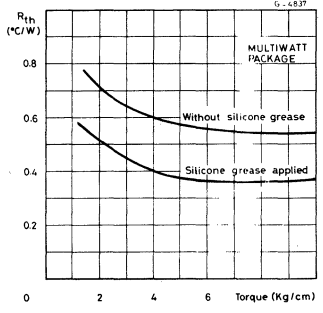
4.1. The plastic packages used by SGS for its linear ICs (Pentawatt, Multiwatt, Versawatt) provide for the use of a single screw to fix the package to the heatsink. A compression spring (clip) can be sufficient as an alternative (fig. 5).

Fig. 5 - MULTIWATT® mounting examples



The screw should be properly tightered to ensure good contact between the back of the package and the heatsink but should not be too tight to avoid deformation of the copper part (tab) of the package causing breaking of the die or separation of the resin from the tab (fig. 6).

Fig. 6 - Contact thermal resistance vs. tightening torque



4.2. The suggested tightening torques with a 3 MA screw are:

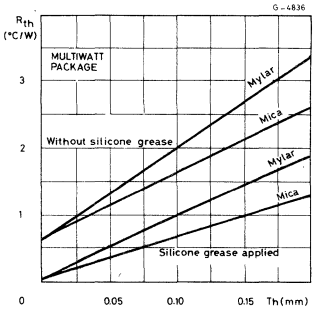
Versawatt 6 Kg/cm
Pentawatt 6 Kg/cm
Multiwatt 8 Kg/cm

If different screws are used the force transmitted to the tab must not exceed that encountered in the above conditions.

When fixing the device avoid bumping or stressing the resin and pins with the tools used for this operation (pneumatic screw drivers, tweezers etc.).

4.3. The contact R_{th} between device and heatsink can be improved by inserting a thin layer of silicone grease with fluidity sufficient to guarantee perfectly uniform distribution on the surface of the tab. The thermal resistance with and without silicone grease is given in fig. 7. An excessively thick layer or an excessive viscosity of the silicone grease can be damaging for the R_{th} and for any tab deformations.

Fig. 7 - Contact thermal resistance vs. insulator thickness



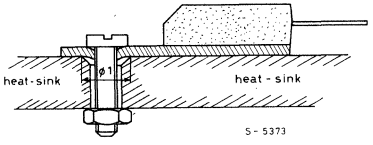
5. Heatsink problems

The most important aspect from the point of view of reliability of a power IC is that the heatsink should be dimensioned to keep the T_j of the device as low as possible. From the mechanical point of view, however, the heatsink must be realized so that it does not damage the integrated circuit.

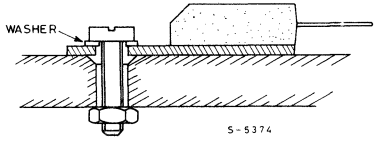
5.1. The planarity of the contact surface between device and heatsink must be $< 10\ \mu m$ for Pentawatt and Versawatt and $< 20\ \mu m$ for Multiwatt.

5.2. If self threading screws are used there must be an outlet for the material that is deformed during formation of the thread. The diameter ϕ 1 (fig. 8) must be large enough to avoid distortion of the

Fig. 8 - Device mounting



WRONG



RIGHT

tab during tightening. For this purpose it may be useful to insert a washer or use screws of the type shown in fig. 9 where the pressure on the tab is distributed on a much larger surface. Sometimes when the hole in the heatsink is formed with a punch, around the hole or hollow there may be a ring which is lower than the heatsink surface. This is dangerous because it may lead to distortion of the tab as mentioned before.

Fig. 9 - Suggested screw

5.3. A very serious problem is that of the rigidity between heatsink, device and printed circuit board. When mounting the heatsink, device (which may be fixed to frame of apparatus) and printed circuit board are bound together by the leads of the device. A solution of this type is extremely dangerous, especially if the equipment is subjected to vibrations.

SEMICONDUCTOR USERS RELIABILITY EVALUATION

SGS SURE III programme is an important improvement of SURE II programme obtained with tightened quality levels. Moreover there are many level's options to satisfy various customer's requests.

SGS SURE III programme aims to inform customers of basic production operations and internal quality and reliability assurance procedures, paying particular attention to the tests and guarantees on the finished product.
This programme covers the set of 100% operations, controls and testing operations undergone by the devices produced to standard specification, i.e. without any special customer requirements.
In other words, unless special co-produced specifications are used, the majority of SGS customers in the professional, consumer and industrial markets buy products tested according to the **SURE III programme.**
The programme thus fully meets the requirements of almost all applications.
Moreover, since the programme offers more options, the customer can request the product with certain supplementary screenings, while the entire production process, apart from the optional operations indicated in the programme, remains identical to that of the standard product.

General Information

This information is valid for all products ordered from SGS or which are ordered to one of the SURE Programme options.

Marking

Each device will be marked in a contrasting ink with the following standard information (if sufficient space is available);
1 – SGS logo
2 – Device type as shown in the detail specification
3 – Manufacturing plant number
4 – Lot code (Production lot)

Packing

Device will be packed in the SGS standard package.
The following information will be marked on the primary package.
1 – SGS logo
2 – Device type as shown on the order confirmation
3 – Quantity in the package
4 – SGS order confirmation
5 – Warning label on Mos products

Testing and finishing

1 – Screenings according to MIL or CECC or however to this programme
2 – 100% electrical testing according to SGS data sheet
3 – Temperature acceptance

When an extended temperature range is guaranteed SGS Outgoing QC may carry out the test at temperatures other than those shown on the data sheet on the basis of temperature correlation of the parameters.
SGS, guarantees the applicability of the AQL levels at the temperature limits and will accepts any lot rejected as a consequence.

External visual and Mechanical Inspection Criteria (group A Acceptance)

- Inoperative mechanical defects (critical):
  e.g. wrong pin indication, wrong marking or splitting, broken or weakened leads, short circuits between leads, missing or partially detached cap, mixed package, cap and frame not aligned at the same side, catastrophic bent leads.
- Major defects (significant mechanical defects, but not functional defects):
  e.g. open packages, deformed leads, unmarked packages or with illegible marking, deep cracks on packages, incomplete tinning or with bubbles – roughness – blackenings, lead straightness and position not in accordance with relevant drawing.
- Minor defects:

Reference specification

a) Basic Sampling Procedures and tables for inspection by attributes: MIL-STD-105D, IEC 410.
   In general the single sampling plan will be used but it is acceptable for the customer to use double or multiple sampling (with, naturally, the same AQLs and inspection levels).
   Similarly Q.C. managers can also use double or multiple sampling.

b) The Sure III Programme has been prepared considering the following specs: IEC 68-2, MIL-STD-883B, CECC 50000, MIL-STD-38510 D and IEC 147-5.
   It should be noted that conformance with these specs should be assumed only where specifically stated in this programme.

Precedence of documents

For the purpose of contractual interpretation in case of conflict, documents shall take the following order of precedence:

1 – Purchase order or contract. The text of the order or contract prevails over any other specification.

2 – Detail specification. The detail specification agreed between customer and vendor prevails over this present specification and any other reference specification.

3 – Generic specification. The generic specification (including this programme) prevails over all reference specifications.

4 – Relevant specification. All reference documents apply only to the extent defined here in.

Essential terms and definitions

For the purpose of interpretation of this general specification the following terms and definitions are applied:

Detail/relevant/blank specification

A specification which covers a particular component or range of components, and which describes that component including rated and/or limiting values and characteristics. The detail specification will also give the inspection requirements or appropriate reference to this general specification.

Inspection lot

A quantity of components presented together for inspection from which a sample is to be drawn and inspected to determine conformance with the acceptance criteria of the specification.

Production lot

Consists of one lot of devices sealed within a period not exceeding six weeks.

Delivery lot

A quantity of components delivered to an order at one time. One delivery lot may consist of one or more inspection lots or parts thereof.

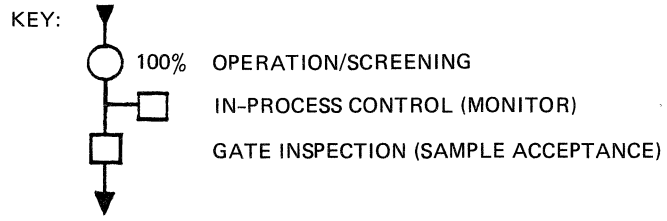
Structurally similar devices

Structurally similar devices are those devices produced concurrently through final seal by the same fabrication techniques, using the same type of machines and apparatus and having the same basic design rules and the same packaging.
Details of structural similarity for various components will be defined, when required, by the SGS Quality Assurance Mgr(s).

Certificate of Conformance

A document issued with a delivery lot stating that the components have been taken from one or more inspection lots accepted under the requirements of the particular specification.

Standard production process flow chart



HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

1 MATERIAL INSPECTION
Starting materials are inspected following written specification and records are maintained for traceability.

2 WAFER FABRICATION
Masking, etching, diffusion and metallization processes produce finished dice in wafer form.

3 IN-PROCESS CONTROL
Wafers and process environment are inspected at main process steps.

4 ELECTRICAL WAFER SORT
Each die is electrically tested and identified when doesn't meet electrical requirements.

5 FINISHED WAFER INSPECTION
Active surface and back finish are inspected on each diffusion lot before release for die fab and assembly.

6 DIE-FABRICATION
Wafers are separated into individual dice and electrical rejects are removed.

7 VISUAL SCREENING
Dice are inspected and selected at high magnification.

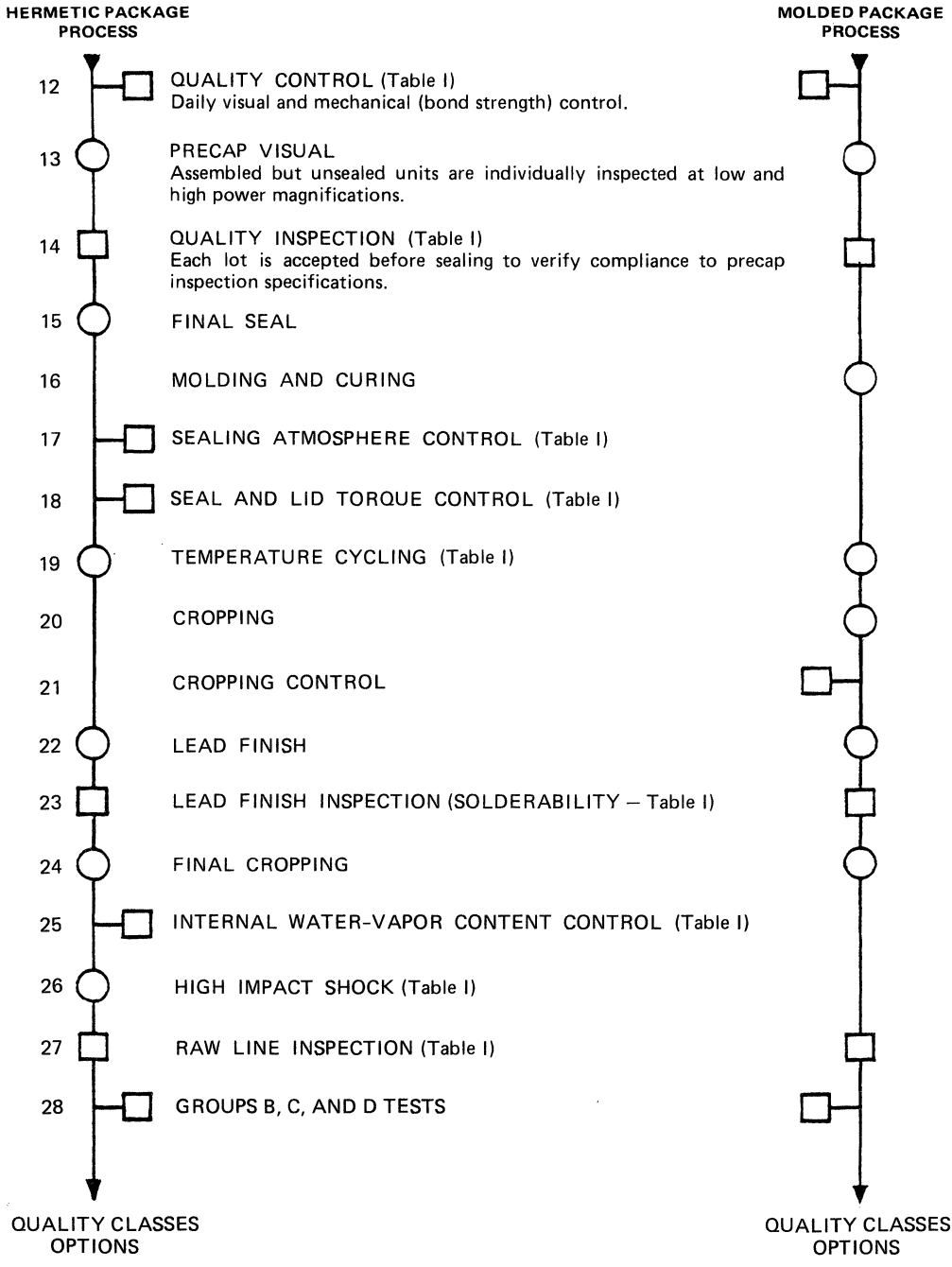
8 QUALITY INSPECTION
Each dice lot is accepted before assembly (visual inspection of active surface)

9 DIE ATTACH

10 QUALITY CONTROL (Table I)
Daily visual and mechanical (die shear strangth) control.

11 WIRE BOND

Standard production process flow chart (continued)

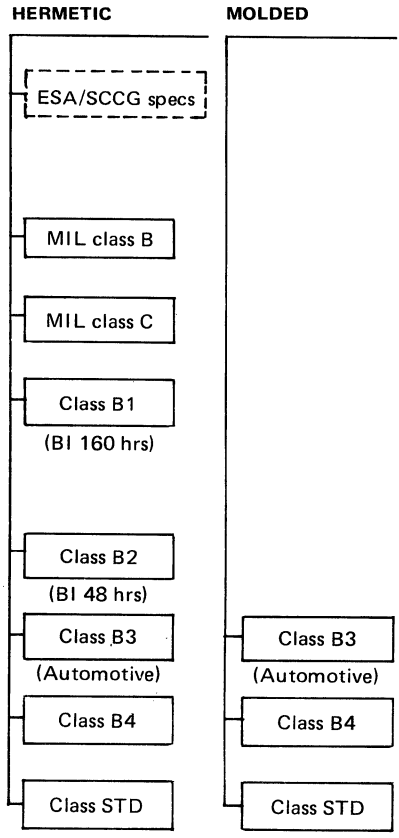


Production quality tests description and screenings

TABLE I

Process steps	Tests	Description
10	DIE-ATTACH CONTROL	MIL STD 883B Mth 2010 cond. B (internal visual) and Mth 2019 (die shear strength).
12	BONDING CONTROL	MIL STD 883B Mth 2010 cond. B (internal visual) and Mth 2011 cond. C (bond strength).
14	PRECAP INSPECTION	MIL STD 883B Mth 2010 cond. B (internal visual)
17	SEALING ATMOSPHERE CONTROL	Moisture content: < 50 ppm for Ceramic packages < 120 ppm for Metal Can packages
18	SEAL CONTROL	– Fine Leak: – Metal can packages IEC 68-2-17 test QK (CECC 50000 para 4.4.10) Helium leak detector after pressurization in He for 16 hrs at 5 atm. Limiti $5 \cdot 10^{-7}$ cc/s – Ceramic packages MIL STD 883B Mth 1014 cond. A1 Helium leak detector after pressurization in He for 2 hrs at 4 atm. Limit: $5 \cdot 10^{-8}$ cc/s for I.C.V. * < 0.4 cc $5 \cdot 10^{-7}$ cc/s for I.C.V. ⩾ 0.4 cc * (I.C.V. = internal cavity volume). – Gross Leak: – Metal Can packages IEC 68-2-17 test Qc Mth 2 (CECC 50000 para 4.4.10). Bubble test in mineral oil at T_{amb}= 125°C after pressurization in He for 16 hrs at 5 atm. – Ceramic packages MIL STD 883B Mth 1014 cond. C.
	LID TORQUE TEST (CONTROL)	– Ceramic Packages only – MIL STD 883B Mth 2024.
19	TEMPERATURE CYCLING	– From -25°C to +150°C; 30 min at extreme temperatures; 5 minutes transfer time; n° 5 cycles
20-21-24	CROPPING	Not for Metal Can packages.
23	SOLDERABILITY INSPECTION	– IEC 68-2-20 Test TA (bath method) – CECC 50000 para 4.4.7 - 230 ± 5°C with preconditioning for 16 hrs at 155°C.
25	INTERNAL WATER VAPOR CONTENT CONTROL	Dew Point method MIL STD 883B Mth 1018 procedure 3 - 5000 ppm max. (dew point temperature less than -15°C).
26	HIGH IMPACT SHOCK	Metal Can packages only except TO-3 and TO-66. 20000 G min.; T = 25 μsec min; Y1 axis only.
27	RAW LINE INSPECTION	– External Visual – MIL STD 883B Mth 2009. – Lid torque test: as per step 18. – Centrifuge (ceramic packages only) MIL STD 883B Mth 2001 – High Impact Shock: as per step 26 – Seal control: as per step 18

Available class options (*)



(*) *SGS-ATES will also supply devices to CECC specifications when these are issued.*

Quality & reliability tests

GROUPS	MIL classes	STD and Others
A	Each lot	Each lot
B	Each lot	See group C
C	3 months	3 months
D	6 months	6 months

Quality class options

B1	B2	B3, B4, STD
(Hermetic packages only)	(Hermetic packages only)	(Hermetic and molded packages)
100% electrical test	Reduced electrical test	100% electrical test
Group A acceptance (STD)		
Marking	Marking	Marking
Burn-in 160 H	Burn-in 48 H	
100% electrical test	100% electrical test	
Group A acceptance (B1)	Group A acceptance (B2)	Group A acceptance (B3 or B4 or STD)
Pack	Pack	Pack
Pack and documentation acc.	Pack and documentation acc.	Pack and documentation acc.
Ship	Ship	Ship

Group A acceptance (♦)

Sub-group	Parameters	Temp. °C	Insp. level	Acceptable quality level (AQL)							
				Molded packages			Hermetic packages				
				B3*	B4	STD°	B1	B2	B3*	B4	STD°
A1	Visual and mechanical insp. Major Minor		I	0.25 1	0.25 1	0.25 1	0.25 1	0.25 1	0.25 1	0.25 1	0.25 1
A2	Inoperative failure (electrical and mechanical) over guaranteed temperature range	T_{max} 25°C T_{min}	II	0.15	0.15 —	— 0.15 —	0.065	0.1	0.1	0.1 —	— 0.1 —
A3	DC parameters and main AC parameters over guaranteed temperature range	T_{max} 25°C T_{min}	II	0.65	0.65 —	— 0.65 —	0.25	0.25	0.4	0.4 —	— 0.4 —
A4	Other AC parameters	25°C	S4	1	1	1	0.65	0.65	0.65	0.65	0.65

° Parameters are guaranteed within the temperature range by 25°C correlation measurements.

* Automotive devices only.

(♦) For MIL class B/C and ESA/SCCG products see relevant SGS-ATES documents.

TABLE III – Group C tests - every 3 months on raw line material (♦)

Tests	MIL-STD-883B		LTPD	Max. Acc. N°
	Method	Condition		
Subgroup 1 Physical dimensions	2016		2 devices (no failure)	
Subgroup 2 (1) Resistance to solvent	2015	– Ceramic packages – Molded packages: solvent solution 2.1A only – Metal can packages	4 devices (no failure)	
Subgroup 3 (1) Solderability (2)	2003	– Soldering temperature of 260 + 10°C or IEC method 68-2-20 test T_A (230 ± 5°C)	15	2
Subgroup 4 Steady state and operating life test or Intermittent life test End-point electrical parameters	1005	– 1000 hrs; according to device spec. type – 5000 cycles Key parameters (Table V); measurements at 0, 168, 500 and 1000 hrs.	5	2
Subgroup 5 (Hermetic packages only) Temperature cycling Constant acceleration Seal (4) a) fine b) gross End-point electrical paramet.	1010 2001 1014	– Test condition C (10 cycles -65°C to +150°C) – Test condition E (30000 G) Y1 orientation only(3) – Test condition A1 or IEC 68-2-17 method, test Q_K – Test condition C or IEC 68-2-17 method, test Q_c (Mth 2 - mineral oil at T = 125°C) Key parameters (Table V)	15	2
Subgroup 6 (1) (Moldel packages only) Pressure pot End-point electrical		121°C, 2 atm, for 48 to 96 hrs, according to package type Key parameters (Table V)	15	2

(1) Performed weekly on finished products.
(2) According to IEC Mth 68-2-20 test T_A.
(3) 20000 G for packages with cavity perimeter of 2 inches or more and/or with a mass of 5 grams or more.
(4) Metal can packages: according to IEC 68-2-17 tests Q_K and Q_c
Ceramic packages : according to MIL-STD-883B Mth 1014.
(♦) For MIL class B/C and ESA/SCCG products see relevant SGS-ATES documents.

TABLE IV – Group D tests - every 6 months on raw line material (♦)

Tests	MIL STD 883B		LTPD	Max. Acc. N°
	Method	Condition		
Subgroup 1 Design and temperature electrical characteristics		This subgroup comprises those parameters complementary to group A parameters. As alternative to LTPD sampling plan. X-R charts may be used to keep the process under control.	30	2
Subgroup 2 Lead integrity	2004	Test condition B2 (lead fatigue)	15	2
Seal (hermetic packages only) (1) a) fine b) gross	1014	Test condition A1 or IEC 68-2-17 method, test Q_K Test condition C or IEC 68-2-17 method, test Q_C (method 2, mineral oil at T = 125°C)		
Lid torque (2) (hermetic packages only)	2024			
Subgroup 3 Thermal shock Temperature cycling Moisture resistance	1011 1010 1004	Test condition B, 15 cycles (-55°C to +125°C Test condition C, 100 cycles (-65°C to +150°C) 10 cycles of 24h; T = 25°C to 65°C, RH= 90% five 3h cycles at -10°C	15	2
Seal (hermetic packages only) (1) a) fine b) gross	1014	Test condition A1 or IEC 68-2-17 method, test Q_K Test condition C or IEC 68-2-17 method, test Q_C (Method 2, mineral oil at T = 125°C)		
Visual examination End-point electrical paramet.		Per visual criteria of method 1004 and 1010. Key parameters (Table V)		
Subgroup 4 (hermetic packages only) Mechanical shock	2002	Test condition B; 1500 G - 0.5 ms - 5 blows in each of the 6 orientations - non operating.	15	2
Vibration, variable frequency	2007	Test condition A; 20 G - 3 orientations - F = 20 to 2000 cps; four 4 minutes cycles, 48 minutes total - non operating.		
Constant acceleration (3)	2001	Test condition E (30000 G), Y1 orientation only.		
Seal (1) a) fine b) gross	1014	Test condition A1 or IEC 68-2-17 method, test Q_K Test condition C or IEC 68-2-17 method, test Q_C (Method 2; mineral oil at T = 125°C)		
Visual examination End-point electrical paramet.		Per visual criteria of method 1010 or 1010. Key parameters (Table V)		
Subgroup 5 Salt atmosphere	1009	Test condition A; 10 to 50 gr of NaCl per square meter per day for 23 hrs at T_A= 35°C.	15	2
Seal (hermetic packages only) (1) a) fine b) gross	1014	Test condition A1 or IEC 68-2-17 method, test Q_K Test condition C or IEC 68-2-17 method, test Q_C (Method 2; mineral oil at T = 125°C)		
Visual examination		Per visual criteria of method 1009.		
Subgroup 6 (molded packages only) Humidity test		85°C/85% RH with bias, t = 1000 hrs. For linear ICs with or without bias according to device specification.	15	2
End-point electrical parameters		Key parameters (Table V); measurements at 0, 198, 500 and 1000 hrs.		

TABLE IV (continued)

Tests	MIL STD 883B		LTPD	Max. Acc. N°
	Method	Conditions		
Subgroup 7 (hermetic packages only) Internal water-vapor content	1018	Dew point method-procedure 3 (5000 ppm max)	3 devices 0 failure or 5 devices 1 failure (4)	
Subgroup 8 Adhesion of lead finish	2025		15	2

(1) Metal can packages: according to IEC 68-2-17 tests Q_k and Q_c.
Ceramic packages : according to MIL-STD-883B method 1014.

(2) Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (I.E. wherever frit seal establishes hermeticity or package integrity).

(3) 20000 G for packages with cavity perimeter of 2 inches or more and/or with a mass of 5 grams or more.

(4) Test three devices; if one fails, test two additional devices with no failure. At the manufacturer's option, if the initial test sample (I.E. 3 or 5 devices) fails a second complete sample may be tested at an alternative laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

(♦) For MIL class B/C and ESA/SCCG products see relevant SGS-ATES documents.

Post test end point

When conducting reliability tests, the definition of the failure, i.e. the determination whether a semiconductor device is good or bad by means of a precisely established failure criteria is required.
Thus care must be taken establishing failure criteria items, since results of failure assessment will depend on such criteria.
During the internal qualification phase, at the various steps of each life and environmental tests, an electrical characterization with electrical parameters recording and Δ calculation on all the samples involved is performed.
On the other hand, on the running products the electrical measurements at the end of the reliability tests are performed according to the data sheets and parameters recording on all failed devices is required.
Table V gives a list of basic failure criteria

TABLE V

Parameters at $T_{amb} = 25°C$		Post test end points
Tests	Symbol	
Voltage Regulator		
Reference voltage	V_{ref}	± 10% spec. limit
Quiescent current drain	I_d	± 20% spec. limit
Load regulation	ΔV_o	± 20% spec. limit
Operational Amplifier		
Input offset voltage	$\|VI\|$	+ 20% spec. limit
Voltage gain (closed loop)	G_v	± 20% spec. limit
Audio Amplifier		
Quiescent output voltage	V_o	± 10% spec. limit
Output power (d = 10%)	P_o	- 10% spec. limit
Input resistance	R_i	- 20% spec. limit
Quiescent current drain	I_d	+ 25% spec. limit or + 100% initial value whichever is greater
Other Linear I.C.		All other end points parameters shall be referred to our internal programs.

Sample size code letters (group A tests)

Lot or batch size			Special inspection levels				General inspection levels		
			S-1	S-2	S-3	S-4	I	II	III
2	to	8	A	A	A	A	A	A	B
9	to	15	A	A	A	A	A	B	C
16	to	25	A	A	B	B	B	C	D
26	to	50	A	B	B	C	C	D	E
51	to	90	B	B	C	C	C	E	F
91	to	150	B	B	C	D	D	F	G
151	to	280	B	C	D	E	E	G	H
281	to	500	B	C	D	E	F	H	J
501	to	1200	C	C	E	F	G	J	K
1201	to	3200	C	D	E	G	H	K	L
3201	to	10000	C	D	F	G	J	L	M
10001	to	35000	C	D	F	H	K	M	N
35001	to	150000	D	E	G	J	L	N	P
150001	to	500000	D	E	G	J	M	P	Q
500001	and	over	D	E	H	K	N	Q	R

Single sampling plans for normal inspection (group A tests)

Sample size code letter	Sample size	Acceptable Quality Levels (normal inspection)																									
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc	Ac Rc
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑	↑
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑
G	32	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑
H	50	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑
J	80	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	125	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	200	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	315	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	500	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	800	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	1250	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	2000	↑	↑	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑

Double and multiple sampling plan inspection may be used.

↓ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection.

↑ = Use first sampling plan above arrow.

Ac = Acceptance number.

Rc = Rejection number.

Sampling plan for "LTPD" Method (group B and C tests)

(as presented in MIL-S-19500E. MIL-STD-883, NEPR 61, and similar specifications).

Poisson sampling plans for lot sizes greater than 200.

Minimum size of sample to be tested to assure, with 90 percent confidence, a lot tolerance percent defective or λ no greater than the LTPD specified.

Max. Percent Defective (LTPD) or λ	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance Number (a) (r = a + 1)	Minimum Sample Sizes																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
5	19 (13.8)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	8904 (0.086)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.334)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

Notes:
The life test failure rate lambda λ shall be defined as the LTPD per 1000 hours.
The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

Conversion between LTPD and AOL Systems

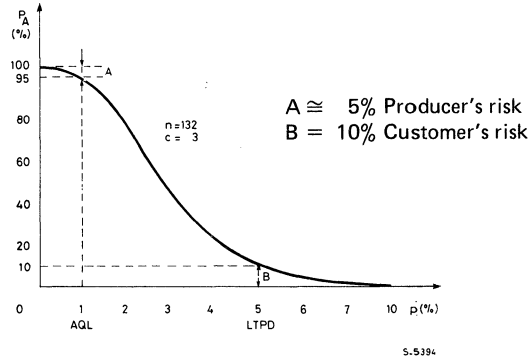
The following table gives a practical method for conversion between the two systems. This conversion is applicable for lot sizes used in practice.
The table has been recommended by the IEC.

AQL	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5
LTPD	0.7	1.0	2.0	3	5	7	10	20	30	50

AQL and LTPD definitions

The availability of suitable sampling plan in various military specifications has led to a general use of AQL and LTPD plans.
The assumptions of a certain sample size (n) and of an acceptance number (c) together with the use of typical distributions (Binomial and Poisson) generate an Operating Characteristic Curve (OC) as shown in fig. 10.

Fig. 10 - Probability of lot acceptance vs. percent defective



The AQL (Acceptable Quality level) is the percentage of defects defined at about 95% probability of lot acceptance, while the LTPD (Lot tolerance percent defective) is the percentage of defects defined at the 10% probability of acceptance.
In other words a sampling plan with 1% AQL passes (accepts) lots will 1% defective about 95% of the time and when a sampling plan with 5% LTPD is used a lot which is trully 5% defective is rejected 90% of the time.
The AQL points defines the Producer's Risk of rejecting a good lot (~ 5%) while the LTPD point defines the Consumer's Risk of accepting a bad lot (10%).

DATA SHEETS

L120A

LINEAR INTEGRATED CIRCUIT

TRIAC/SCR PHASE CONTROL

The L 120A is a monolithic integrated circuit in 16-lead dual in-line plastic package. It incorporates the following functions:

- AC supply 50/60 Hz
- Zero-voltage and zero-current detector
- Ramp generator
- Inhibition of casual firing pulses
- Stabilization of the internal positive DC supply
- High gain operational amplifier
- Output short-circuit protection

The L 120A is intended for use as a phase controller in industrial and consumer applications.

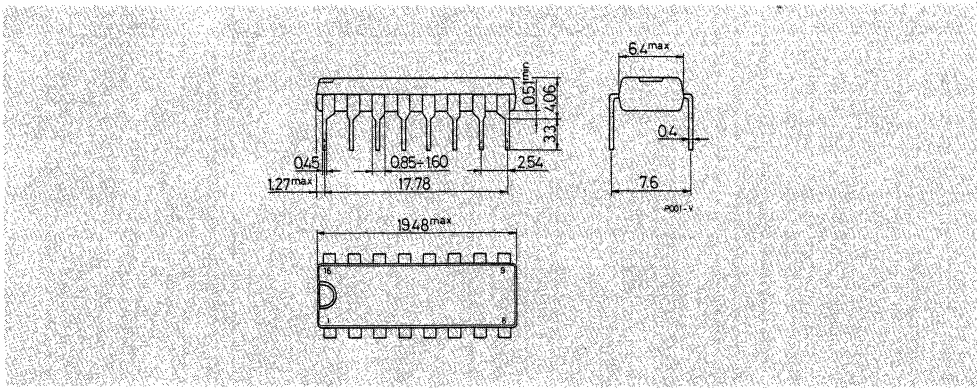
ABSOLUTE MAXIMUM RATINGS

I_9	AC peak supply current	60	mA
I_{14}	Max input current (pin 14)	20	mA
I_{D1}, I_{D2}	Input diodes peak current	1	A
V_{8-12}	Positive clamp voltage	15	V
V_{10-12}	Negative clamp voltage	15	V
V_{1-2}	Differential input voltage	± 7	V
V_{3-5}	Differential input voltage	± 8	V
P_{tot}	Total power dissipation at T_{amb}= 85°C	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature	-25 to 150	°C

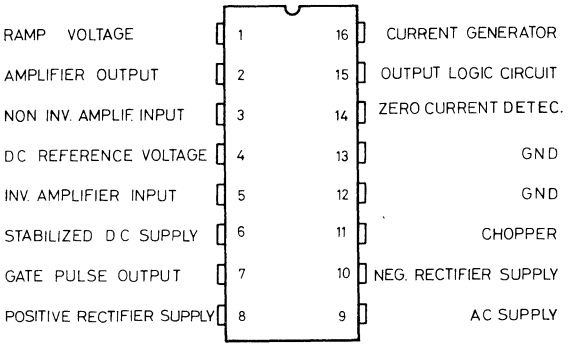
ORDERING NUMBER: L 120AB

MECHANICAL DATA

Dimensions in mm



CONNECTION DIAGRAM (top view)



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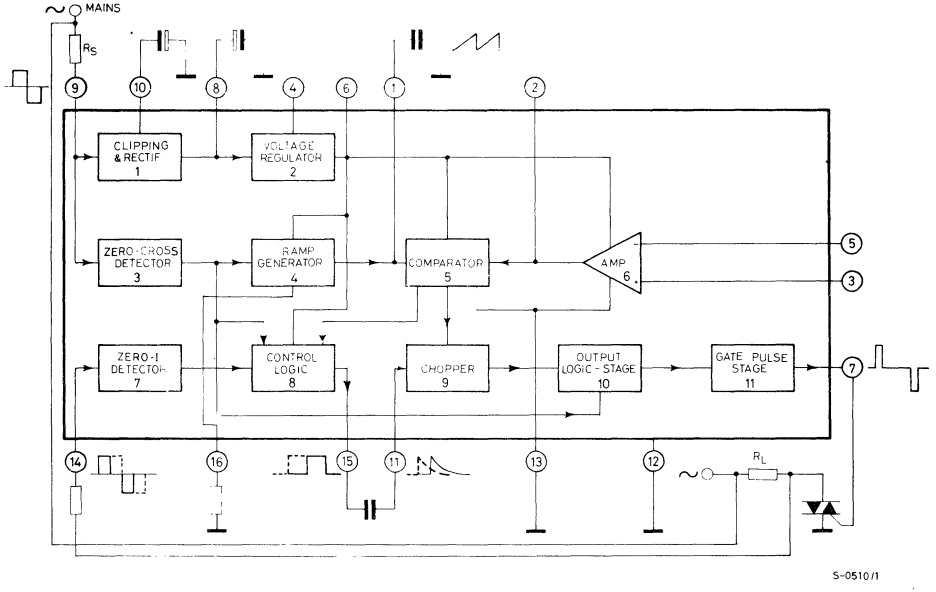
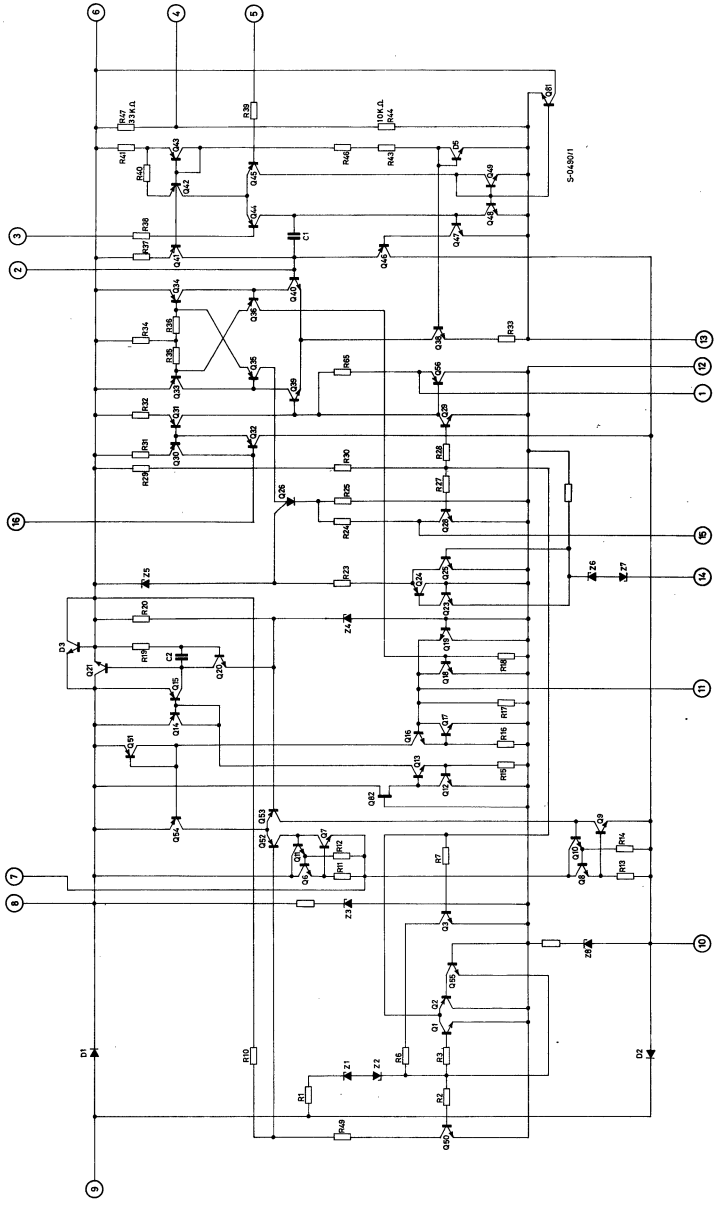
BLOCK DIAGRAM

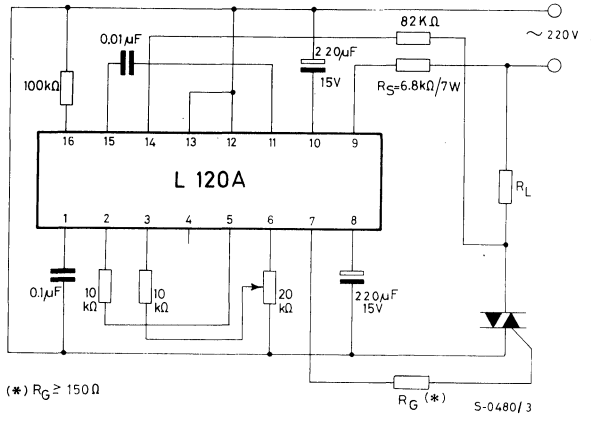


S-0510/1

SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, refer to the test circuit unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{8-12}	Positive clamp voltage		10	11.5	13	V
V_{10-12}	Negative clamp voltage		10	11.5	13	V
V_{8-12}	External DC supply voltage		10.5			V
V_{10-12}	External DC supply voltage		-10.5			V
V_{9-12}	Sync input threshold			± 12.5		V
V_{14-12}	Zero current threshold		± 8.8	± 10	± 11.2	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{10-14} V_{8-14}	Zero current threshold			1.2			V
I_{14}	Operative input current to avoid inibition (pin 14)			0.4			mA
V_{1-12}	Ramp discharge level					1.1	V
V_{1-12}	Maximum ramp level			7.2			V
V_{1-2}	Comparat. differential trigger level				70	100	mV
G_v	Amplifier voltage gain (open loop)	V_2 (peak to peak) = 6V		60	70		dB
V_{2-13}	Max output voltage			7			V
V_{2-13}	Min output voltage					0.9	V
V_{3-13}, V_{5-13}	Input offset voltage	$R_{3-13} = R_{5-13} = 50\Omega$			3	6	mV
I_b	Input bias current (pin 3, 5)				0.1	1	μA
V_{3-5}	Differential input voltage					$\pm$ 7	V
V_{3-13}, V_{5-13}	Input voltage range			0.5		7.5	V
CMR	Common mode rejection	$R_{3-13} = R_{5-13} \leq 1k\Omega$			60		dB
V_{6-13}	Regulator output voltage			8.3		9.5	V
I_6	Max regulator output current			3			mA
$\frac{\Delta V_6}{V_6}$	Load regulation	$I_6 = 0$ to 3 mA			0.5	2	%
$\frac{\Delta V_6}{\Delta V_8}$	Line regulation	V_8 = 12 to 14V $I_6 = 0$			46		dB
SVR	Supply voltage rejection	V_8 = 12V f_{ripple} = 50 Hz V_{ripple} (peak to peak) = 4V			46		dB
V_4	Reference voltage	$I_4 = 10\ \mu A$			1.5		V
V_{7-12}	Firing pulse amplitude	$R_{7-12} = 1\ k\Omega$	positive	4.5	5.5		V
			negative	8	9.5		V
I_7	Maximum output current	$R_{7-12} = 10\Omega$		80			mA
t_{pw}	Output pulse width	$R_{7-12} = 50\Omega$			200		μs
t_r	Output pulse rise time				200		ns

Fig. 1 - Peak supply current vs. dropping resistor R_S

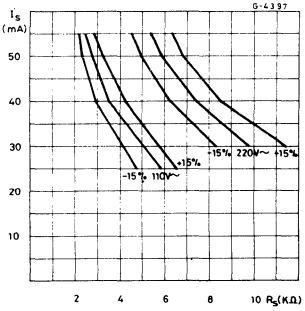


Fig. 2 - Maximum allowable average supply current vs. ambient temperature

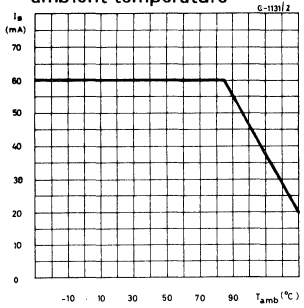


Fig. 3 - Gate pulse amplitude vs. gate resistance

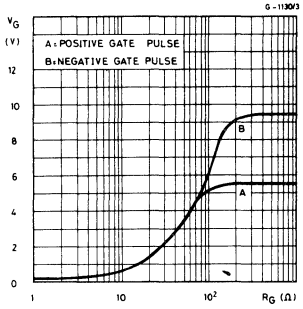


Fig. 4 - Gate current variation vs. ambient temperature

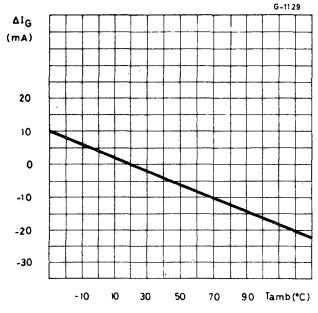


Fig. 5 - Gate pulse width vs. C_{11-15}

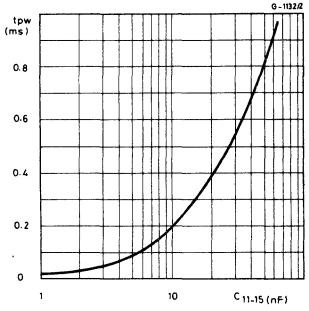
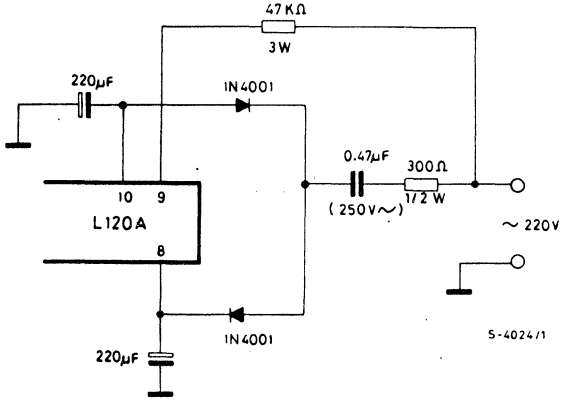


Fig. 6 - Alternative system for reduction of power dissipation



APPLICATION INFORMATION

Fig. 7 - Application circuit for AC motor speed regulators

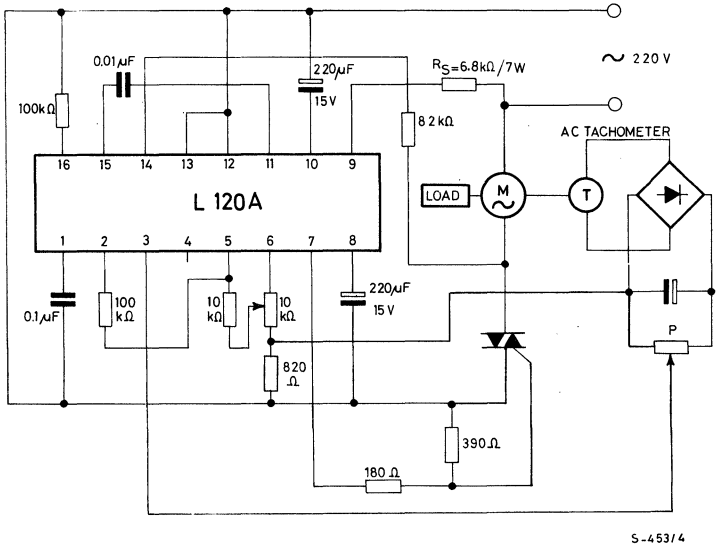
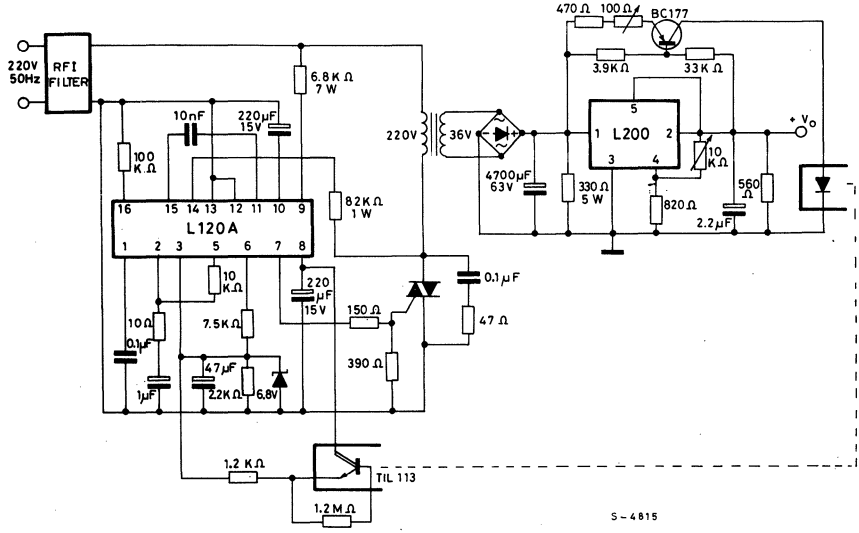


Fig. 8 - 3 to 30V adjustable power supply with preregulation



NOTE - For a more detailed description of the L120A and its applications refer to SGS-DESIGN NOTE - DN 382.

LINEAR INTEGRATED CIRCUIT

L121A

TRIAC/SCR BURST CONTROL

The L 121A is a monolithic integrated circuit in 16-lead dual in-line plastic package. It incorporates the following functions:

- AC supply 50/60 Hz
- Zero-voltage detector
- Ramp generator
- Inhibition of casual firing pulses
- Stabilization of the internal positive DC supply
- High gain operational amplifier
- Output short-circuit protection

The L 121A is intended for use as a burst controller in industrial and consumer applications.

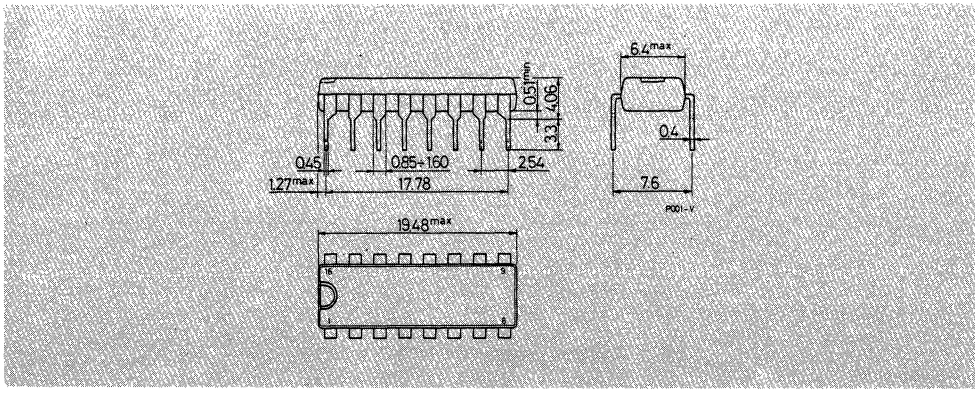
ABSOLUTE MAXIMUM RATINGS

I_9	AC Peak supply current	60	mA
I_{D1}, I_{D2}	Input diodes peak current	1	A
V_{14}	Maximum voltage (pin 14)	20	V
V_{8-12}	Positive clamp voltage	15	V
V_{10-12}	Negative clamp voltage	15	V
V_{1-2}	Differential input voltage	± 7	V
V_{3-5}	Differential input voltage	± 8	V
P_{tot}	Total power dissipation at T_{amb} = 85°C	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating junction temperature	-25 to 150	°C

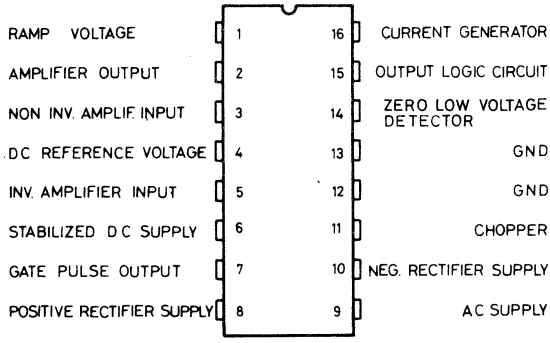
ORDERING NUMBER: L 121AB

MECHANICAL DATA

Dimensions in mm

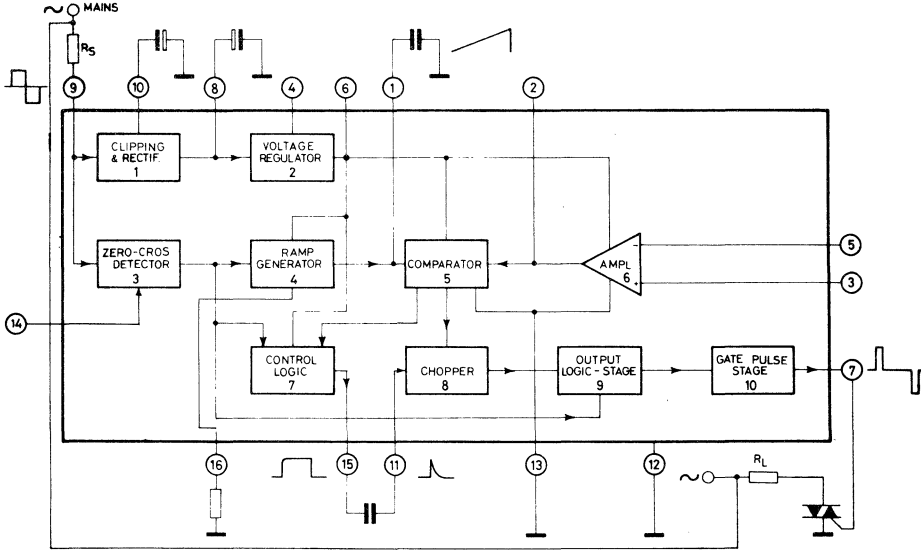


CONNECTION DIAGRAM (top view)



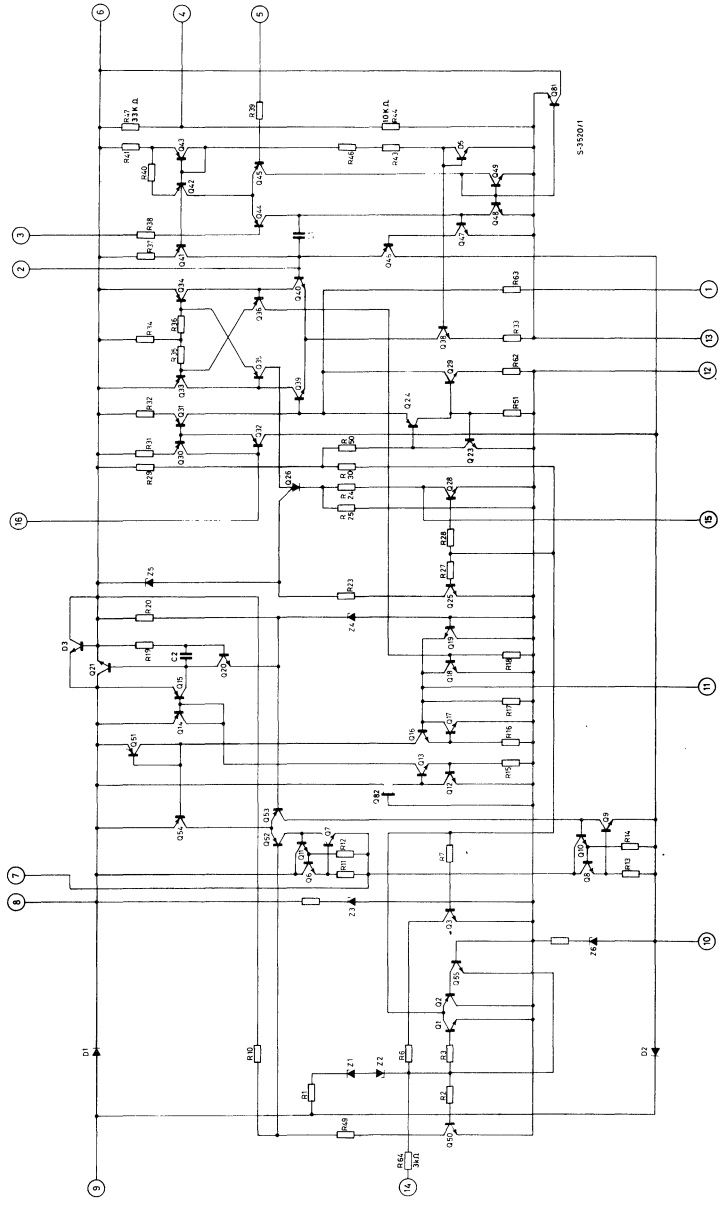
S-3517/1

BLOCK DIAGRAM

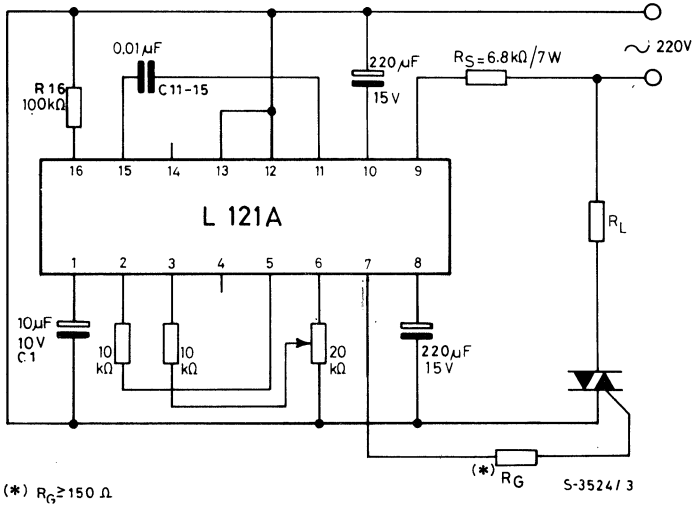


S-3518

SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, refer to the test circuit unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{8-12}	Positive clamp voltage		10	11.5	13	V
V_{10-12}	Negative clamp voltage		10	11.5	13	V
V_{8-12}	External DC supply voltage		10.5			V
V_{10-12}	External DC supply voltage		-10.5			V
V_{9-12}	Sync input threshold			± 12.5		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{14-12}	Minimum input voltage	(pin 9 open)		±2.5			V
V_{1-12}	Ramp discharge level					1.2	V
V_{1-12}	Maximum ramp level			5.2			V
V_{1-2}	Comparator differential trigger level				70	100	mV
G_v	Amplifier voltage gain (open loop)	V_2 (peak to peak) = 6V		60	70		dB
V_{2-13}	Max output voltage			7			V
V_{2-13}	Min output voltage					0.9	V
V_{3-13}, V_{5-13}	Input offset voltage	$R_{3-13} = R_{5-13} = 50\Omega$			3	6	mV
I_b	Input bias current				0.1	1	μA
V_{3-5}	Differential input voltage					± 7	V
V_{3-13}, V_{5-13}	Input voltage range			0.5		7.5	V
CMR	Common mode rejection	$R_{3-13} = R_{5-13} \leq 1k\Omega$			60		dB
V_{6-13}	Regulator output voltage			8.3		9.5	V
I_6	Max regulator output current			3			mA
$\frac{\Delta V_6}{V_6}$	Load regulation	I_6 = 0 to 3 mA			0.5	2	%
$\frac{\Delta V_6}{\Delta V_8}$	Line regulation	V_8 = 12 to 14V I_6 = 0			46		dB
SVR	Supply voltage rejection	V_8 = 12V f_{ripple} = 50 Hz V_{ripple} (peak to peak) = 4V			46		dB
V_4	Reference voltage	$I_4 = 10 \cdot \mu A$			1.5		V
V_{7-12}	Firing pulse amplitude	R_{7-12} = 1 kΩ	positive	4.5	5.5		V
			negative	8	9.5		V
I_7	Maximum output current	$R_{7-12} = 10\Omega$		80			mA
ɔw	Output pulse width	$R_{7-12} = 50\Omega$			200		μs
	Output pulse rise time				200		ns

Fig. 1 - Peak supply current vs. dropping resistor R_S

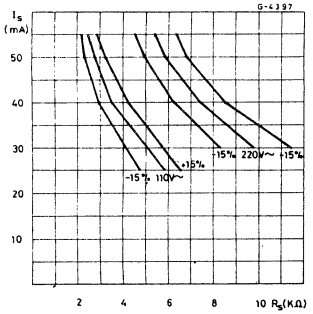


Fig. 2 - Maximum allowable average supply current vs. ambient temperature

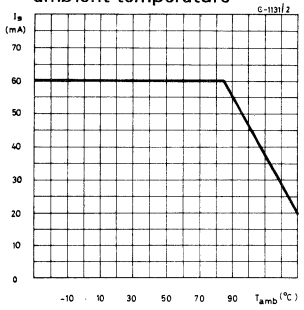


Fig. 3 - Gate pulse amplitude vs. gate resistance

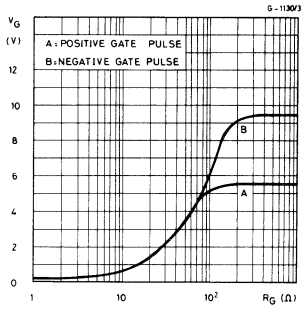


Fig. 4 - Gate current variation vs. ambient temperature

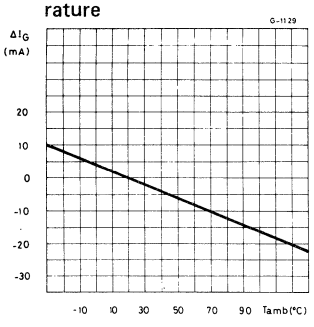


Fig. 5 - Gate pulse width vs. C_{11-15}

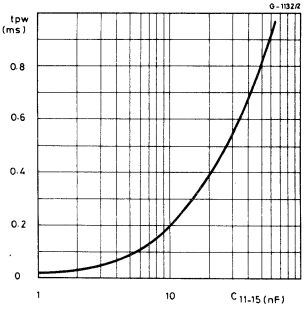


Fig. 6 - Ramp width vs. external time constant $R_{16} \cdot C_1$

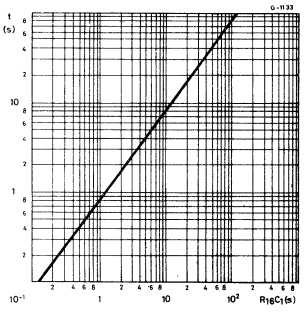
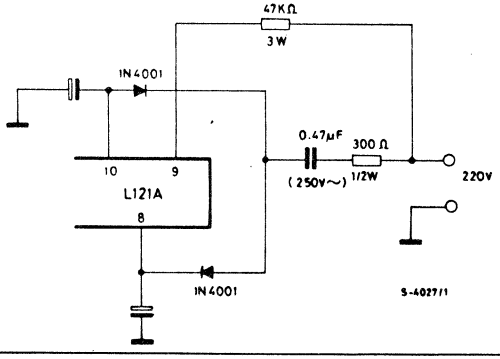


Fig. 7 - Alternative system for reduction of power dissipation



APPLICATION INFORMATION

Fig. 8 - Application circuit for temperature control (proportional type)

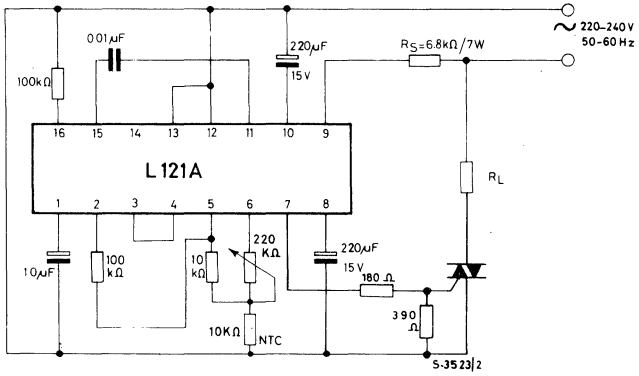


Fig. 9 - Application circuit for temperature control (ON-OFF type)

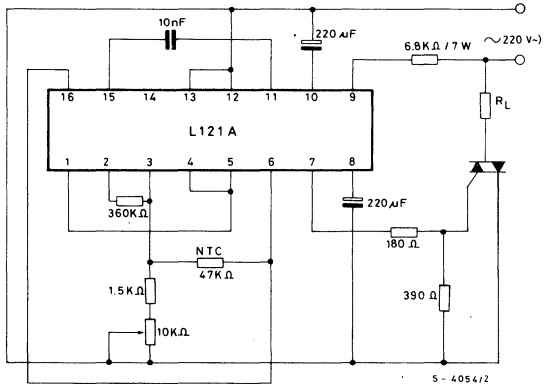


Fig. 10 - Application circuit for **low AC supply voltage** (by using pin 14)

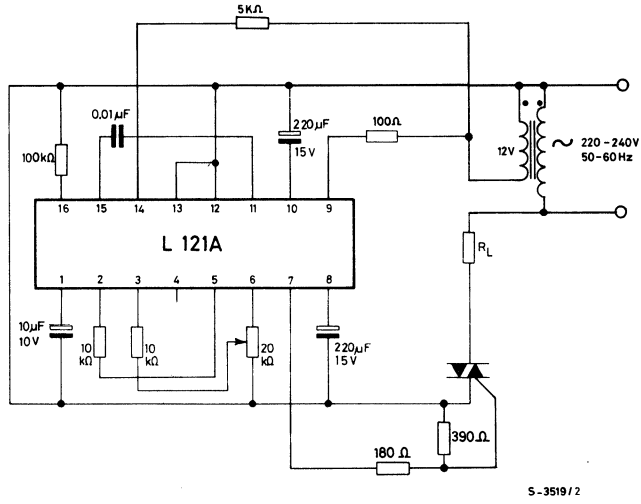
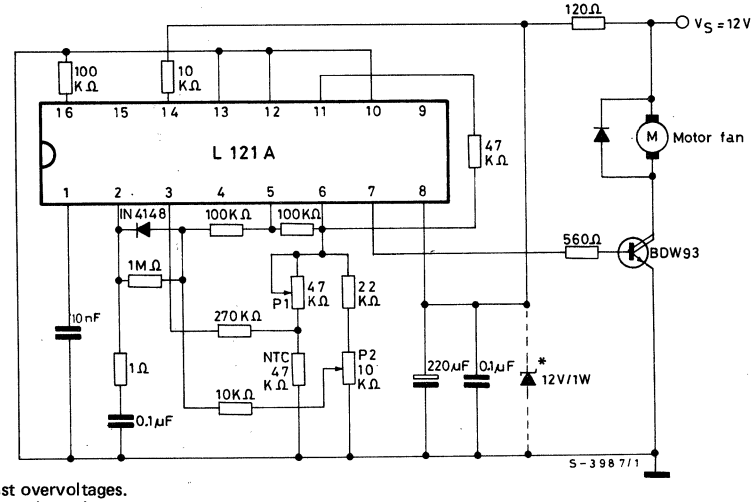


Fig. 11 - Cimate control for car.



* Protection against overvoltages.
P_1 : system hysteresis setting
P_2 : temperature setting

NOTE - For a more detailed description of the L120A and its applications refer to SGS-DESIGN NOTE - DN 382.

LINEAR INTEGRATED CIRCUIT

L123

HIGH PRECISION VOLTAGE REGULATOR

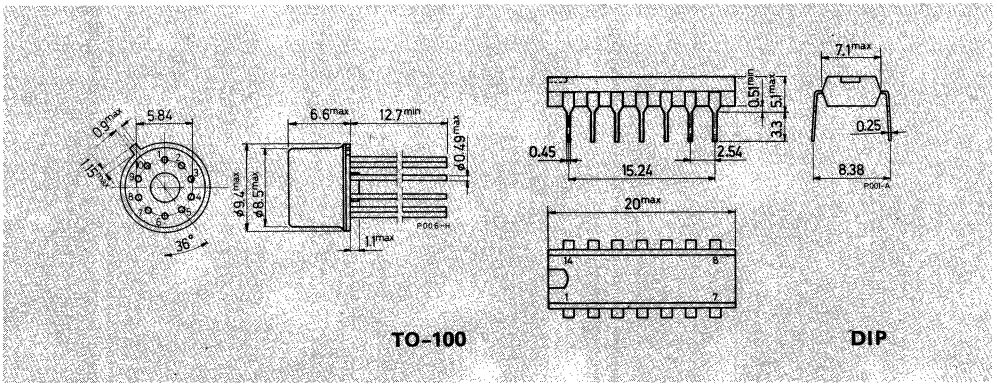
- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING

The L123 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic package and 10-lead Metal Can (TO-100 type). The circuit provides internal current limiting. When the output current excedes 150 mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

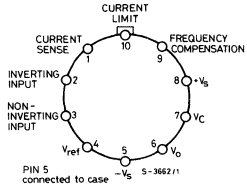
ABSOLUTE MAXIMUM RATINGS		L123	L123 C
V_i	Input voltage	40 V	40 V
ΔV_{i-o}	Dropout voltage	40 V	40 V
I_o	Output current	150 mA	150 mA
I_{ref}	Current from V_{ref}	15 mA	25 mA
P_{tot}	Power dissipation (at T_{amb} = 70°C) Plastic DIP	–	1 W
	TO-100	520 mW	520 mW
T_{op}	Operating junction temperature	-25 to 150 °C	0 to 70 °C
T_{stg}	Storage temperature	-65 to 150 °C	-65 to 150 °C

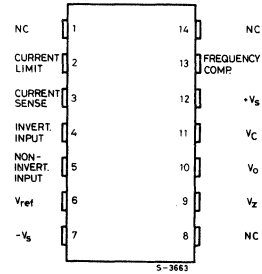
MECHANICAL DATA

Dimensions in mm



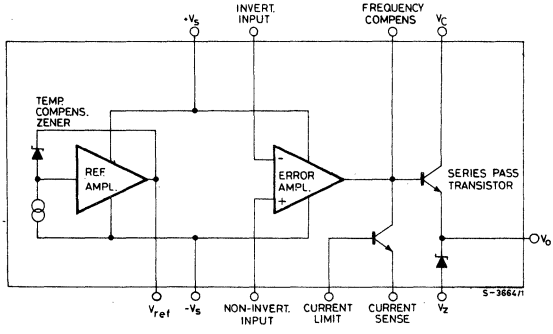
CONNECTION DIAGRAM AND ORDERING NUMBERS
(top views)



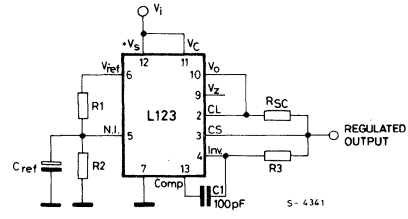


Type	TO-100	Plastic DIP
L123	L123T	—
L123C	L123CT	L123CB

BLOCK DIAGRAM



TEST CIRCUIT
(Pin configuration relative to the Plastic package)



$V_i = 12V$
$V_o = 5V$
$I_o = 1\ mA$
$R_1 // R_2 \leq 10\ K\Omega$

THERMAL DATA			TO-100	Plastic DIP
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	80 °C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	L123C			L123			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\frac{\Delta V_o}{\Delta V_i}$	Line regulation	V_i = 12 to 15V		0.01	0.1		0.01	0.1	%
		V_i = 12 to 40V		0.1	0.5		0.02	0.2	%
		V_i = 12 to 15V; $T_{min} \leqslant T_{amb} \leqslant T_{max}$			0.3			0.3	%
$\frac{\Delta V_o}{V_o}$	Load regulation	I_o = 1 to 50 mA		0.03	0.2		0.03	0.15	%
		$T_{min} \leqslant T_{amb} \leqslant T_{max}$ I_o = 1 to 10 mA			0.6			0.6	%
V_{ref}	Reference voltage	I_{ref}= 160 μA	6.8	7.15	7.5	6.95	7.15	7.35	V
SVR	Ripple rejection	f = 100 Hz to 10 KHz C_{ref}= 0		74			74		dB
		C_{ref}= 5 μF		86			86		dB
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				150			150	$\frac{ppm}{°C}$
I_{sc}	Short circuit current limiting	R_{sc}= 10Ω V_o= 0		65			65		mA
V_i	Input voltage range		9.5		40	9.5		40	V
V_o	Output voltage range		2		37	2		37	V
V_i-V_o			3		38	3		38	V
I_d	Quiescent drain current	I_o = 0 V_i = 30V		2.3	4		2.3	5	mA
	Long term stability			0.1			0.1		$\frac{\%}{1000\ hrs}$
e_N	Output noise voltage	BW= 100 Hz to 10 KHz C_{ref}= 0		20			20		μV
		C_{ref}= 5 μF		2.5			2.5		μV
V_z	Output zener voltage (for plastic package only)	I_z = 1 mA	6.9		7.7				V

Note: T_{min} = 0°C (L123C); -25°C (L123).
T_{max} = 70°C (L123C); 150°C (L123).

Fig. 1 - Maximum output current vs. voltage drop

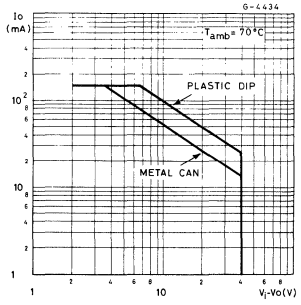


Fig. 2 - Current limiting characteristics

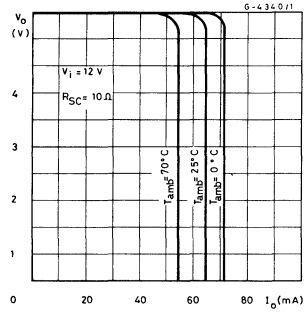


Fig. 3 - Current limiting characteristics vs. junction temperature

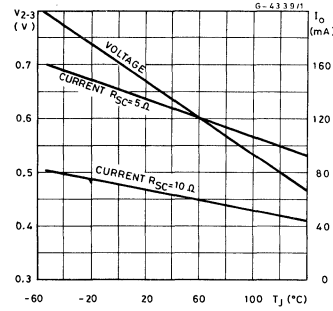


Fig. 4 - Load regulation characteristics without current limiting

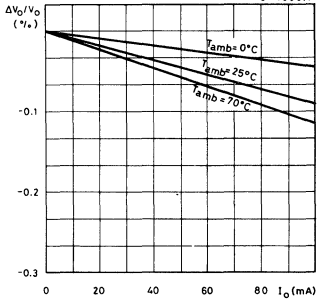


Fig. 5 - Load regulation characteristics with current limiting

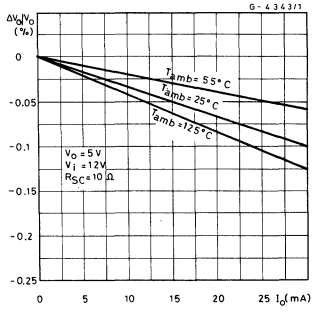


Fig. 6 - Load regulation characteristics with current limiting

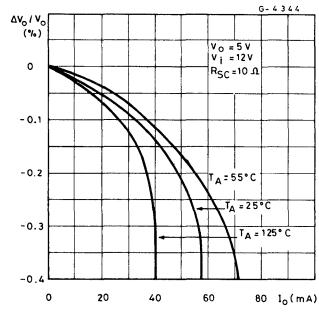


Fig. 7 - Line regulation vs. voltage drop

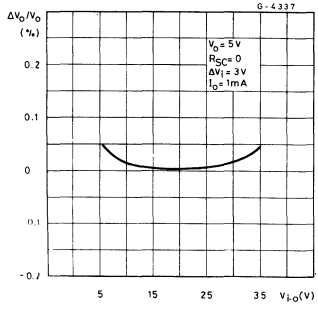


Fig. 8 - Load regulation vs. voltage drop

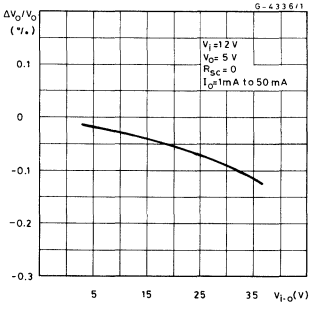


Fig. 9 - Quiescent drain current vs. input voltage

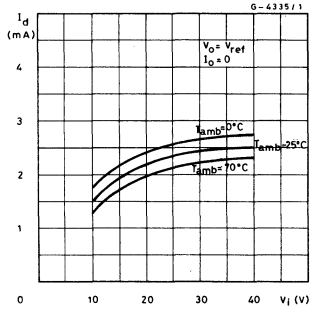


Fig. 10 - Line transient response

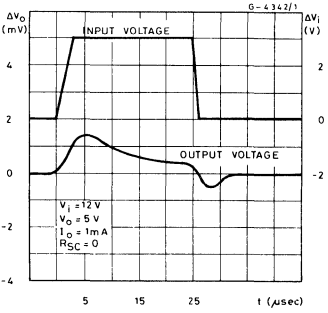


Fig. 11 - Load transient response

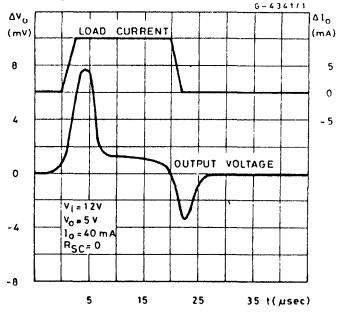


Fig. 12 - Output impedance vs. frequency

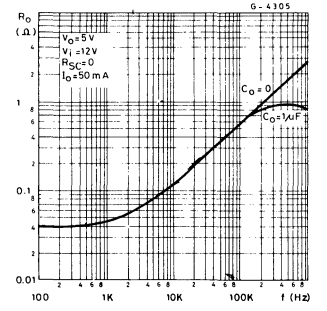


Table I — Resistor values (KΩ) for standard output voltages

Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)			Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% (°)		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	13, 16, 17 18, 21, 23	4.12	3.01	1.8	0.5	1.2	+100	19	3.57	102	2.2	10	91
+ 5	13, 16, 17 18, 21, 23	2.15	4.99	0.75	0.5	2.2	+250	19	3.57	255	2.2	10	240
+ 6	13, 16, 17 18, 21, 23	1.15	6.04	0.5	0.5	2.7	- 6(°°)	15	3.57	2.43	1.2	0.5	0.75
+ 9	14, 16, 17 18, 21, 23	1.87	7.15	0.75	1	2.7	- 9	15	3.48	5.36	1.2	0.5	2
+12	14, 16, 17 18, 21, 23	4.87	7.15	2	1	3	- 12	15	3.57	8.45	1.2	0.5	3.3
+15	14, 16, 17 18, 21, 23	7.87	7.15	3.3	1	3	- 15	15	3.65	11.5	1.2	0.5	4.3
+28	14, 16, 17 18, 21, 23	21	7.15	5.6	1	2	- 28	15	3.57	24.3	1.2	0.5	10
+45	19	3.57	48.7	2.2	10	39	- 45	20	3.57	41.2	2.2	10	33
+75	19	3.57	78.7	2.2	10	68	-100	20	3.57	97.6	2.2	10	91
							-250	20	3.57	249	2.2	10	240

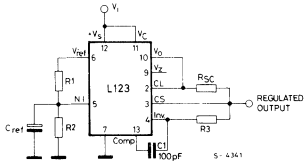
Note: (°) Replace R_1/R_2 divider with the circuit of fig. 24.
(°°) V^+ must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 13, 17, 18, 21, 23, 16 $V_O = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts Fig. 19 $V_O = [\frac{V_{ref}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 14, 16, 17, 18, 21, 23 $V_O = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from -6 to -250 volts Fig. 15, 20 $V_O = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_O}{R_{sc}} \frac{R_3}{R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

APPLICATION INFORMATION (Pin numbers relative to the plastic package)

Fig. 13 - Basic low voltage regulator
(V_o = 2 to 7V)

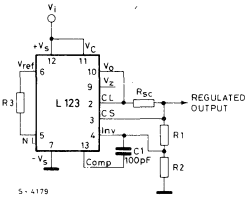


NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance
Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) . . . . . .0.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .1.5 mV

Fig. 14 - Basic high voltage regulator
(V_o = 7 to 37V)

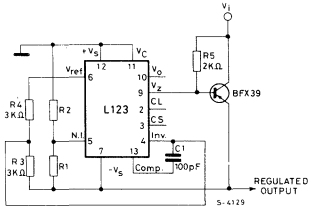


NOTE: $\frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

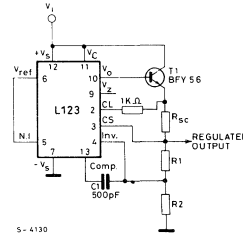
Typical performance
Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . .1.5 mV
Load Regulation (ΔI_O = 50 mA) . . . .4.5 mV

Fig. 15 - Negative voltage regulator



Typical performance
Regulated Output Voltage . . . . . .-15V
Line Regulation (ΔV_i = 3V) . . . . . .1 mV
Load Regulation (ΔI_O = 100 mA) . . . .2 mV

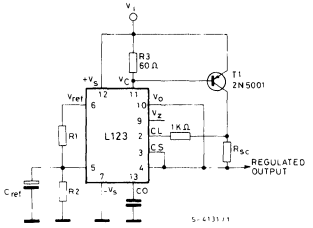
Fig. 16 - Positive voltage regulator (External NPN Pass Transistor)



Typical performance
Regulated Output Voltage . . . . . .+15V
Line Regulation (ΔV_i = 3V) . . . . . .1.5 mV
Load Regulation (ΔI_O = 1A) . . . . . 15 mV

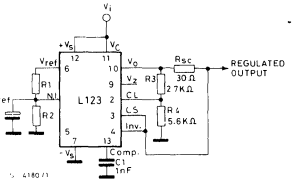
APPLICATION INFORMATION (continued)

Fig. 17 - Positive voltage regulator (External PNP Pass Transistor)



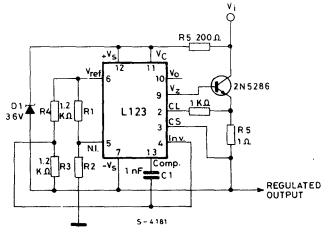
Typical performance
Regulated Output Voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 3V$) . . . . . .0.5 mV
Load Regulation ($\Delta I_O = 1A$) . . . . . .5 mV

Fig. 18 - Foldback current limiting



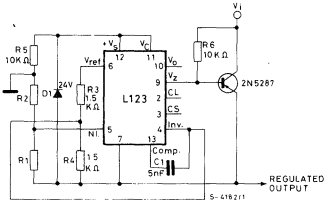
Typical performance
Regulated Output Voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 3V$) . . . . . .0.5 mV
Load Regulation ($\Delta I_O = 10$ mA) . . . . .1 mV
Current Limit Knee . . . . . .20 mA

Fig. 19 - Positive floating regulator



Typical performance
Regulated Output Voltage . . . . . .+100V
Line Regulation ($\Delta V_i = 20V$) . . . . . .15 mV
Load Regulation ($\Delta I_O = 50$ mA) . . . .20 mV

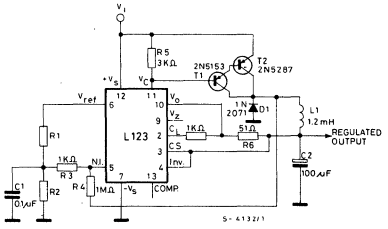
Fig. 20 - Negative floating regulator



Typical performance
Regulated Output Voltage . . . . . .-100V
Line Regulation ($\Delta V_i = 20V$) . . . . . .30 mV
Load Regulation ($\Delta I_O = 100$ mA) . . .20 mV

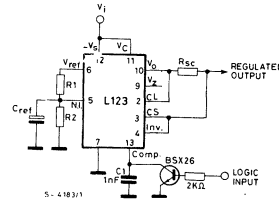
APPLICATION INFORMATION (continued)

Fig. 21 - Positive switching regulator



Typical performance
Regulated Output voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 30V$) . . . . . 10 mV
Load Regulation ($\Delta I_O = 2A$) . . . . . 80 mV

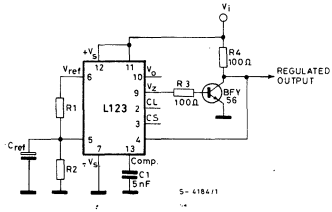
Fig. 22 - Remote shutdown regulator with current limiting



Typical performance
Regulated Output Voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 3V$) . . . . . .0.5 mV
Load Regulation ($\Delta I_O = 50$ mA) . . . .1.5 mV

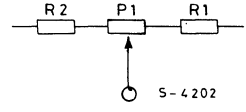
NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

Fig. 23 - Shunt regulator



Typical performance
Regulated Output Voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 10V$) . . . . . .2 mV
Load Regulation ($\Delta I_O = 100$ mA) . . . .5 mV

Fig. 24 - Output voltage adjust



LINEAR INTEGRATED CIRCUIT

L146

HIGH PRECISION HIGH VOLTAGE REGULATOR

- INPUT VOLTAGE UP TO 80V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 77V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT UP TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING
- THERMAL PROTECTION

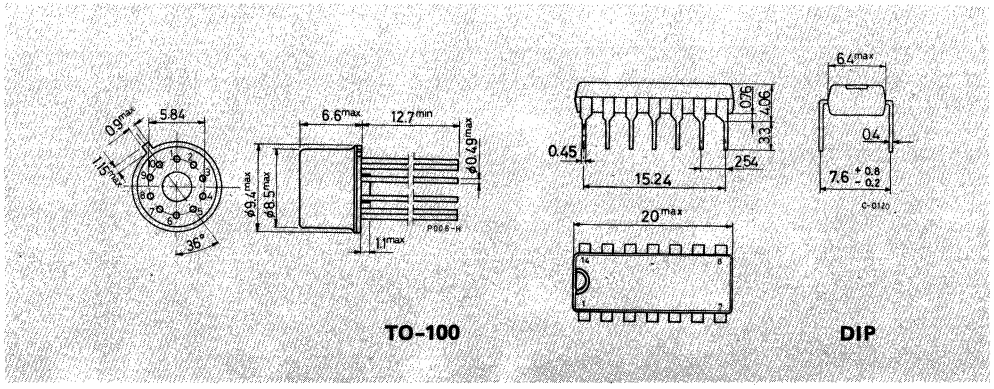
The L146 is a monolithic integrated programmable voltage regulator in 14-lead dual in-line plastic package and 10-lead Metal Can (TO-100 type). It is made with high voltage technology and provides internal current limiting and thermal shut down protection; when current exceeds 150 mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut down. **The L146 is intended to widen the application range of L123 up to 80V.**

ABSOLUTE MAXIMUM RATINGS

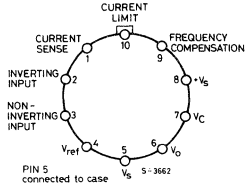
V_i	Input voltage	80	V
V_i-V_o	Voltage drop	78	V
I_o	Output current	150	mA
I_{ref}	Current from V_{ref}	8	mA
P_{tot}	Power dissipation (at T_{amb}= 70°C) Plastic DIP	1	W
	TO-100	520	mW
T_{op}	Operating junction temperature L146	-25 to + 85	°C
	L146C	0 to +70	°C
T_{stg}	Storage temperature	-65 to +150	°C

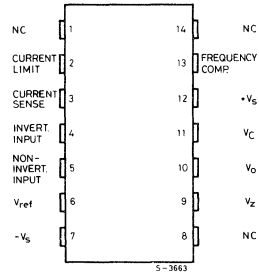
MECHANICAL DATA

Dimensions in mm



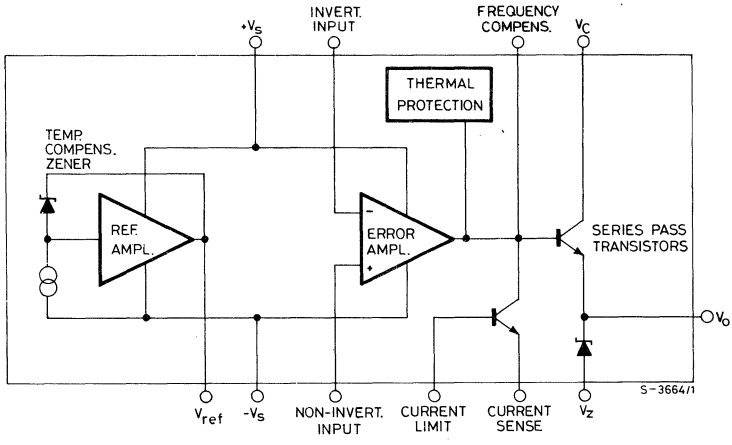
CONNECTION DIAGRAMS
(top view)





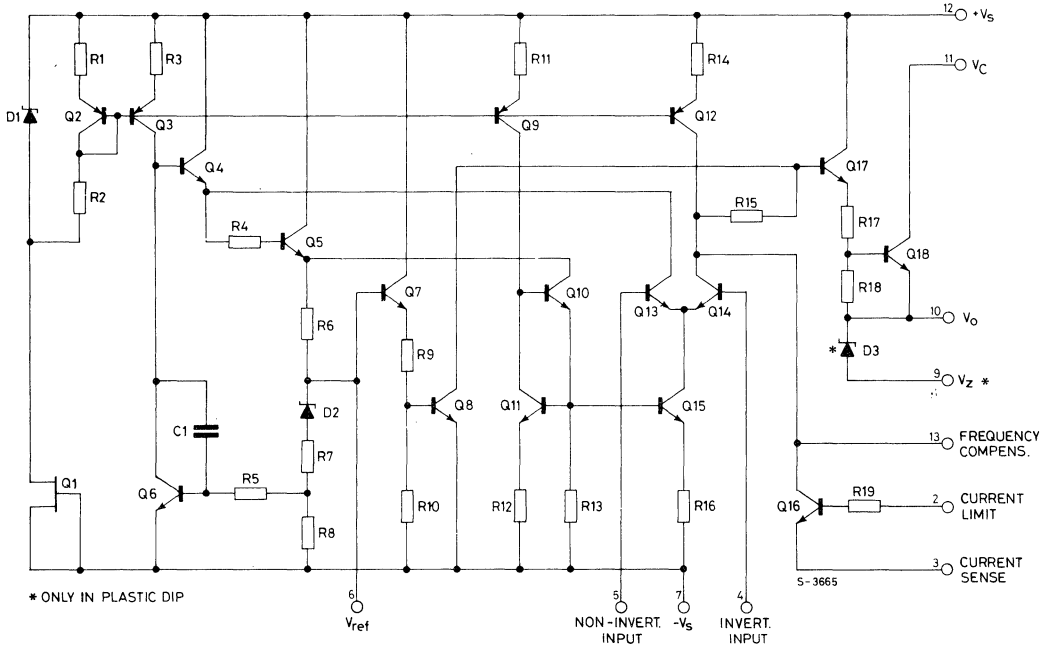
Type	TO-100	Plastic DIP
L146	L146 T	
L146 C	L146 CT	L146 CB

BLOCK DIAGRAM

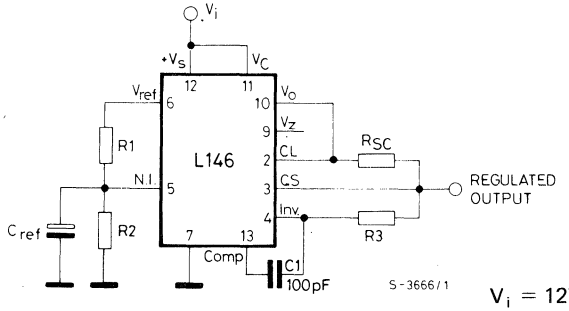


THERMAL DATA			TO-100	Plastic DIP
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155°C/W	80°C/W

SCHEMATIC DIAGRAM (pin number relative to the plastic package)



TEST CIRCUIT



$V_i = 12V$
$V_o = 5V \quad I_o = 1\ mA$
$R_1 // R_2 \leqslant 10\ K\Omega$

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	L146 C			L146			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$\frac{\Delta V_o}{V_o}$	Line regulation	V_i = 12 to 15V V_i = 12 to 40V V_i = 40 to 80V		0.05 0.1 0.1	0.15 0.5 0.5		0.05 0.1 0.1	0.15 0.2 0.2	%
$\frac{\Delta V_o}{V_o}$	Load regulation	V_i = 12V V_o = 5V I_o = 1 to 50 mA		0.03	0.2		0.03	0.15	%
		V_i = 40V V_o = 37V I_o = 1 to 10 mA		0.1	0.5		0.1	0.3	%
		V_i = 80V V_o = 77V I_o = 1 to 10 mA		0.12	0.8		0.12	0.5	%
V_{ref}	Reference voltage	I_{ref}= 160 μA	7.75	8.15	8.55	7.9	8.15	8.4	V
ΔV_{ref}		I_{ref}= 160 μA to 5 mA		4	14		4	14	mV
SVR	Ripple rejection	f = 100 Hz to 10 KHz C_{ref}= 0 C_{ref}= 5 μF		60 88			60 88		dB
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				150			150	$\frac{ppM}{°C}$
I_{sc}	Short circuit current limiting	R_{sc}= 10Ω V_o = 0	50	60	70	50	60	70	mA
V_i	Input voltage range		10		80	10		80	V
V_o	Output voltage range		2		77	2		77	V
$V_i - V_O$	Voltage drop		3		78	3		78	V
I_d	Quiescent drain current	I_o = 0 V_o = 5V (including I_{ref}= 160 μA) V_i = 12V V_i = 40V V_i = 80V		 4 5.6 6	 5.5 7 7.5		 4 5.6 6	 5.5 7 7.5	mA
ΔI_d	Quiescent drain current change	I_o= 1 mA V_o= 5V; V_i = 12 to 40V			2.2			1.6	mA
		I_o= 1 mA V_o= 5V; V_i = 12 to 80V			2.6			2	mA
	Long term stability			0.1			0.1		$\frac{\%}{1000\ hrs}$
e_N	Output noise voltage	BW = 100 Hz to 10 KHz C_{ref}= 0 C_{ref}= 5 μF		300 30			300 30		μV
V_z	Output zener voltage (for plastic package only)	I_z= 1 mA	6.9		7.7				V

Fig. 1 - Maximum output current vs. voltage drop

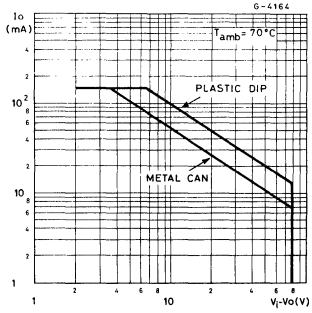


Fig. 2 - Load regulation vs. output current (with current limiting)

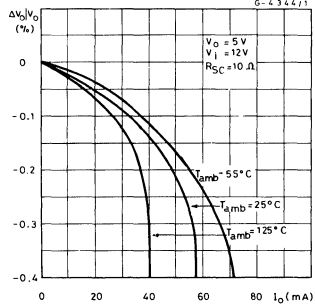


Fig. 3 - Load regulation vs. output current (with current limiting)

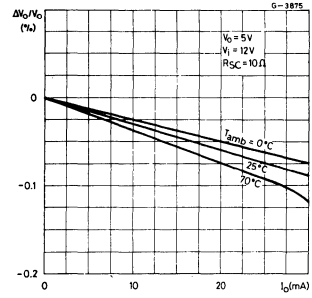


Fig. 4 - Load regulation vs. output current (without current limiting)

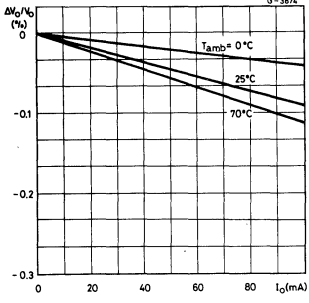


Fig. 5 - Current limiting characteristics

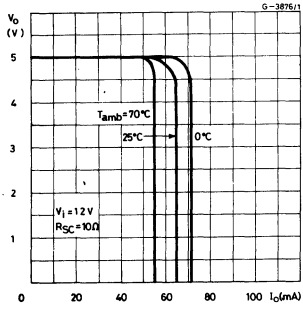


Fig. 6 - Current limiting characteristics vs. junction temperature

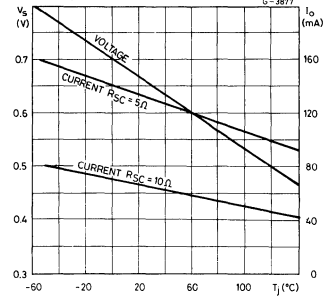


Fig. 7 - Line transient response

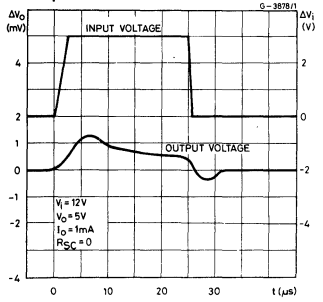


Fig. 8 - Load transient response

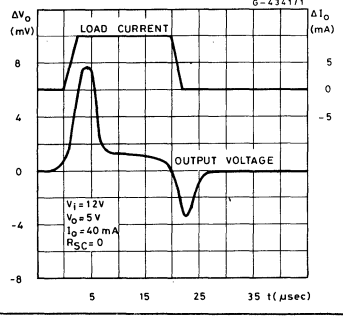


Fig. 9 - Output impedance vs. frequency

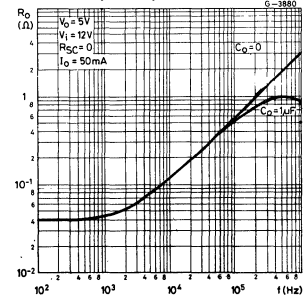


Table I -- Resistor values (KΩ) for standard output voltage

Positive output voltage	Applicable figures	Fixed output ± 5%	
		R_1	R_2
+6	10, 13, 14 18, 20	2.4	6.8
+12	11, 13, 14, 15, 18, 20	3.2	6.8
+30		15	5.6
+50		24	47
+70		30	39
+100	16	2.7	68
+250		4.7	120

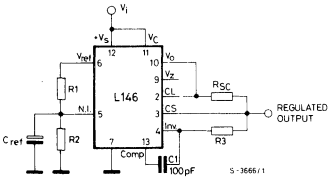
Negative output voltage	Applicable figures	Fixed output ± 5%	
		R_1	R_2
-9	12	2.2	2.7
-12		1.5	3
-30		4.7	30
-50		2.7	30
-100	17	2	47
-250		2	120

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 10, 13, 14, 15, 18, 20 $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts Fig. 16 $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +77 volts Fig. 11, 13, 14, 15, 18, 20 $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Output from -6 to -250 volts Fig. 12, 17 $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT}}{R_{sc}} \frac{R_3}{R_4} + \frac{V_{SENSE}}{R_{sc}} \frac{(R_3 + R_4)}{R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

APPLICATION CIRCUITS (continued)

Fig. 10 - Basic low voltage regulator (V_{OUT} = 2 to 7V)



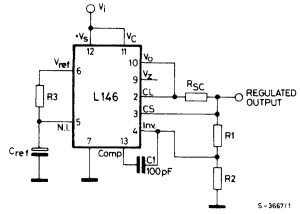
NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) . . . . . .0.5 mV
Load Regulation (ΔI_o = 50 mA) . . . .1.5 mV

Fig. 11 - Basic high voltage regulator (V_{OUT} = 7 to 77V)



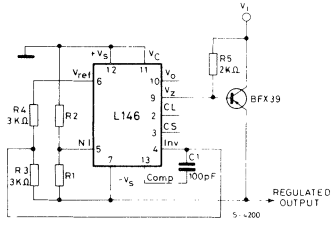
NOTE: $R3 = \frac{R1 \cdot R2}{R1 + R2}$ for minimum temperature drift.

R3 may be eliminated for minimum component count.

Typical performance

Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . .1.5 mV
Load Regulation (ΔI_o = 50 mA) . . . .4.5 mV

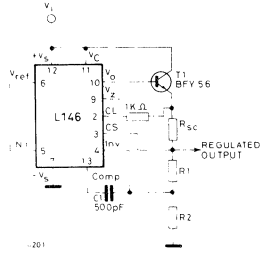
Fig. 12 - Negative voltage regulator



Typical performance

Regulated Output Voltage . . . . . .+15V
Line Regulation (ΔV_i = 3V) . . . . . .1.5 mV
Load Regulation (ΔI_o = 1 A) . . . . . 15 mV

Fig. 13 - Positive voltage regulator (External NPN Pass Transistor)

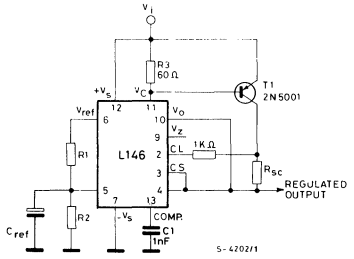


Typical performance

Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) . . . . . .1 mV
Load Regulation (ΔI_o = 100 mA) . . . .2 mV

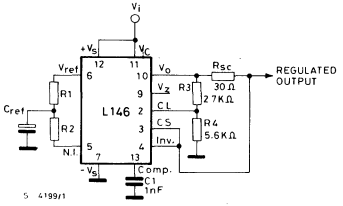
APPLICATION CIRCUITS (continued)

Fig. 14 - Positive voltage regulator (External PNP Pass Transistor)



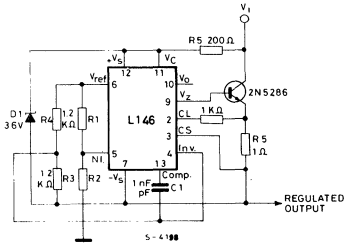
Typical performance
Regulated Output Voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 3V$) . . . . . .0.5 mV
Load Regulation ($\Delta I_o = 1A$) . . . . . .5 mV

Fig. 15 - Foldback current limiting



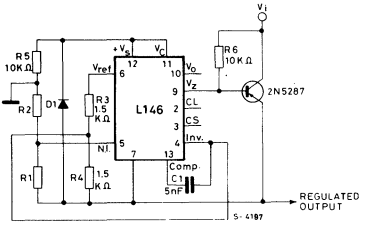
Typical performance
Regulated Output Voltage . . . . . .+5V
Line Regulation ($\Delta V_i = 3V$) . . . . . .0.5 mV
Load Regulation ($\Delta I_o = 10$ mA) . . . . .1 mV
Current Limit Knee . . . . . .20 mA

Fig. 16 - Positive floating regulator



Typical performance
Regulated Output Voltage . . . . . .+100V
Line Regulation ($\Delta V_i = 20V$) . . . . . .15 mV
Load Regulation ($\Delta I_o = 50$ mA) . . . .20 mV

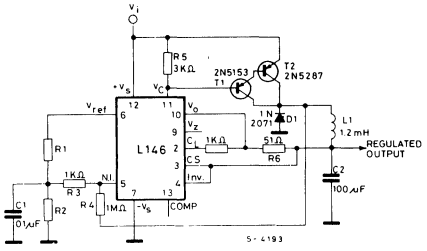
Fig. 17 - Negative floating regulator



Typical performance
Regulated Output Voltage . . . . . .-100V
Line Regulation ($\Delta V_i = 20V$) . . . . . .30 mV
Load Regulation ($\Delta I_o = 100$ mA) . . .20 mV

APPLICATION CIRCUITS (continued)

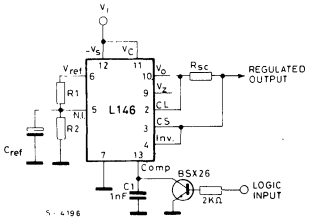
Fig. 18 - Positive switching regulator



Typical performance

Regulated Output Voltage . . . . . +5V
Line Regulation ($\Delta V_i = 30V$) . . . . . 10 mV
Load Regulation ($\Delta I_o = 2A$) . . . . . 80 mA

Fig. 19 - Remote shutdown regulator with current limiting

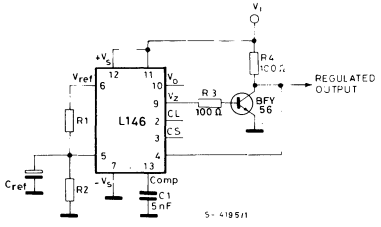


Typical performance

Regulated Output Voltage 5V
Line Regulation ($\Delta V_i = 3V$) 0.5V
Load Regulation ($\Delta I_o = 50$ mA) . . . .1.5 mV

NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

Fig. 20 - Shunt regulator



Typical performance

Regulated Output Voltage . . . . . +5V
Line Regulation ($\Delta V_i = 10V$) . . . . . 2 mV
Load Regulation ($\Delta I_o = 100$ mA) 5mV

APPLICATION CIRCUITS (continued)

Fig. 21 - 60V voltage regulator with foldback characteristic

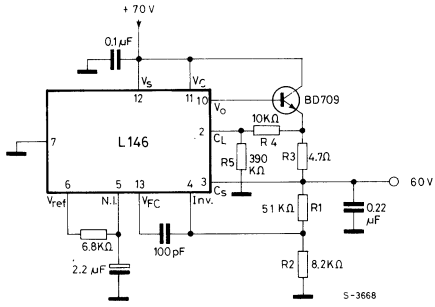
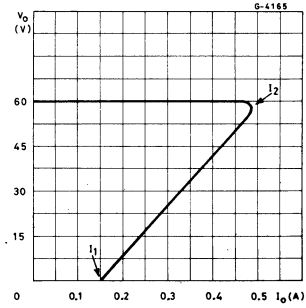
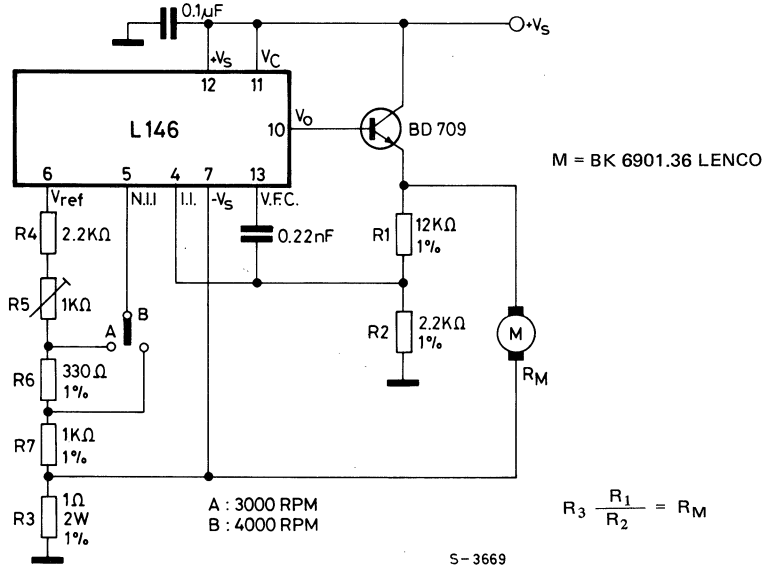


Fig. 22



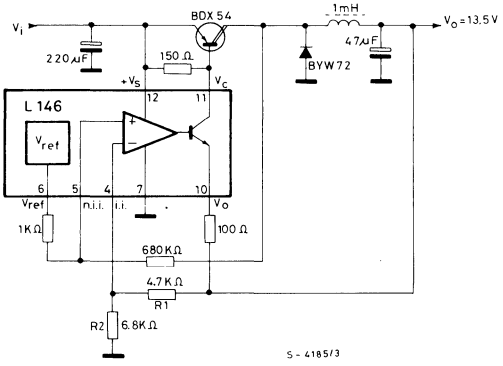
$$I_2 = \frac{V_o \frac{R_4}{R_5} + V_{2-3}}{R_{SC}} \; ; \qquad I_1 = \frac{V_{2-3}}{R_{SC}} \left(1 + \frac{R_4}{R_5}\right); \qquad V_{2-3} \cong 0.7V$$

Fig. 23 - Motor speed control



APPLICATION CIRCUITS (continued)

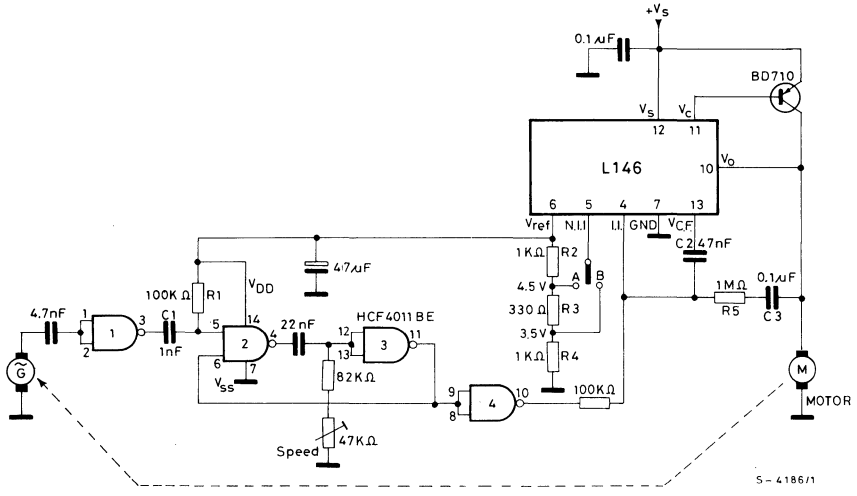
Fig. 24 - Step-down switching regulator for 12V car radio



Performance:

Output voltage	13.5V
Max output current	3A
Input voltage range	20 to 30V
Line regulation	50 dB (I_o= 2A) ΔV_i= 10V
Load regulation	0.1% (ΔI_o= 3A)
Ripple	100 mVpp
Efficiency	75% (I_o= 3A)
Switching frequency	25 KHz

Fig. 25 - 30W motor speed regulator with tacho adjustment and speed change-over switch



NOTE - For a more detailed description of the L146 and its applications, refer to SGS-TECHNICAL NOTE TN.150.

L149

LINEAR INTEGRATED CIRCUIT

MONOLITHIC HIGH GAIN POWER OUTPUT STAGE

The L149 is a general purpose power booster in Pentawatt® package consisting of a quasi-complementary darlingtons output stage with the associated biasing system and inhibit facility.
The circuit features are:

- High output current (4A peak)
- High current gain (10 000 typ.)
- Operation up to ± 20V
- Thermal protection
- Short circuit protection
- Operation within SOA
- High slew-rate

The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current (P_o= 20W, d = 0.5%, R_L= 4Ω, V_s= ± 16V).

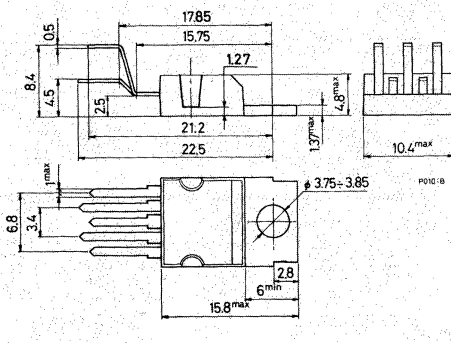
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	±20	V
V_i	Input voltage	V_s	
I_o	DC output current	3	A
I_o	Peak output current (internally limited)	4	A
V_{INH}	Input inhibit voltage	$-V_s$ +5	V
		$-V_s$ - 1.5	V
P_{tot}	Power dissipation at T_{case}= 75°C	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

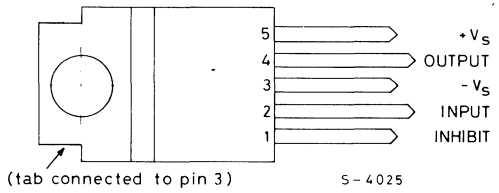
ORDERING NUMBER: L149V

MECHANICAL DATA

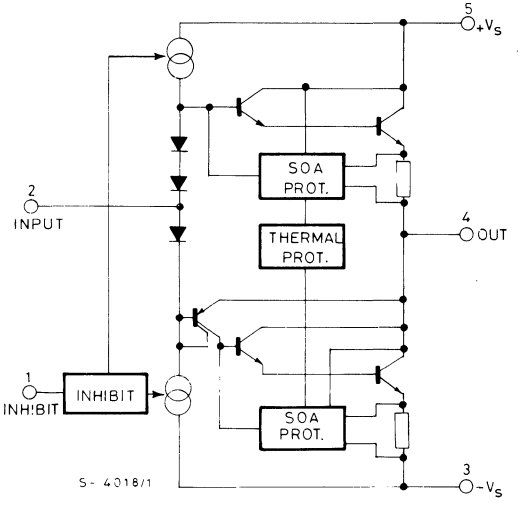
Dimensions in mm



CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage				± 20	V
I_d	Quiescent drain current	V_s = ± 16V		30		mA
I_{in}	Input current	V_s = ± 16V V_i = 0V		200	400	μA
h_{FE}	DC current gain	V_s = ± 16V I_o = 3A	6000	10000		–
G_v	Voltage gain	V_s = ± 16V I_o = 1.5A		1		–
V_{CEsat}	Saturation voltage (for each transistor)	I_o = 3A			3.5	V
V_{os}	Input offset voltage	V_s = ± 16V			0.3	V
V_{INH}	Inhibit input voltage (pins 1–3)	ON condition			± 0.3	V
		OFF condition	± 1.2			
R_{INH}	Inhibit input resistance	f = 1 KHz		2.0		KΩ
SR	Slew rate			30		V/μs
B	Power bandwidth	V_s= ±18V, d = 1%, R_L= 8Ω		200		KHz

TEST CIRCUIT

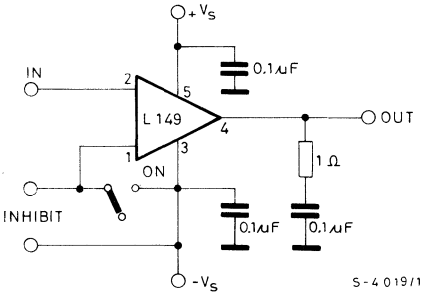


Fig. 1 - Maximum saturation voltage vs. output current

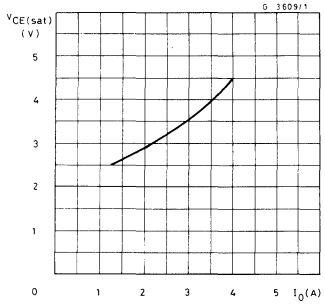


Fig. 2 - Current limiting characteristics

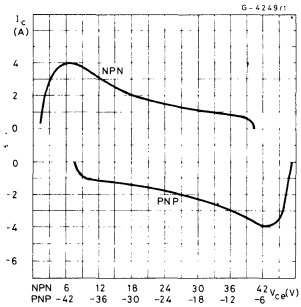
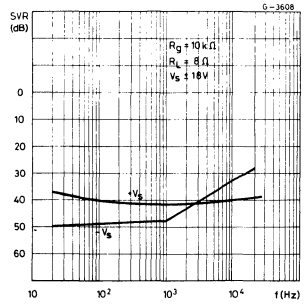


Fig. 3 - Supply voltage rejection vs. frequency



APPLICATION INFORMATION

Fig. 4 - High power amplifier with single power supply (G_v= 30 dB)

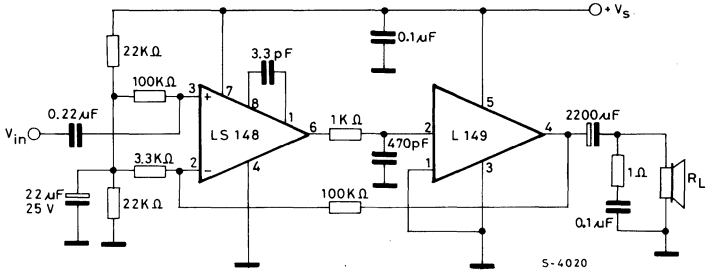


Fig. 5 - Distortion vs. output power (f = 1 KHz)

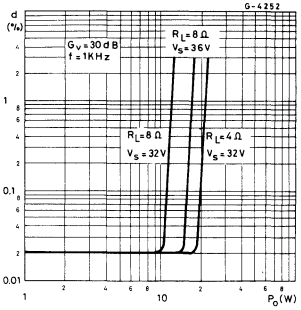


Fig. 6 - Distortion vs. output power (f= 10 KHz)

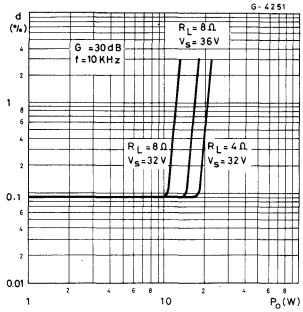
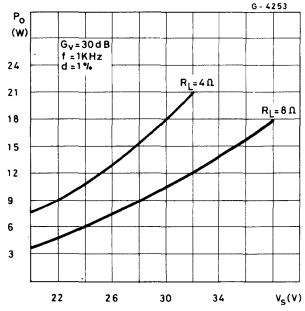


Fig. 7 - Output power vs. supply voltage



APPLICATION INFORMATION (continued)

Fig. 8 - High slew-rate power operational amplifier

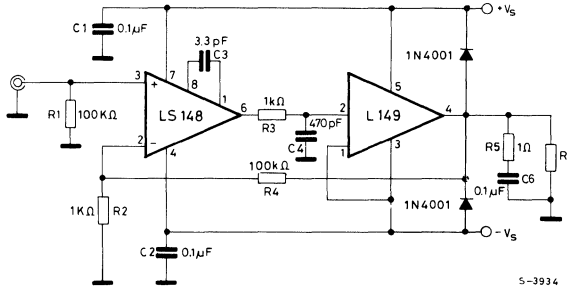


Fig. 9 - Electronic potentiometer (short-circuit protected)

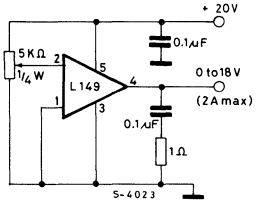
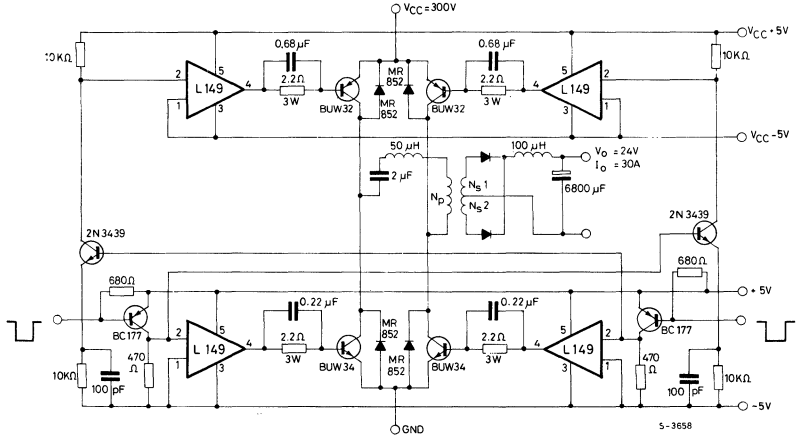


Fig. 10 - 720W Switch-Mode Power Supply using the L149 as driver stage for the power transistors



NOTE - For a more detailed description of the L149 and its applications, refer to SGS-TECHNICAL NOTE TN.150.

LINEAR INTEGRATED CIRCUIT

L165

3A POWER OPERATIONAL AMPLIFIER

The L165 is a monolithic integrated circuit in Pentawatt® package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required,

- Output current up to 3A.
- Large common-mode and differential mode ranges.
- SOA protection.
- Thermal protection.

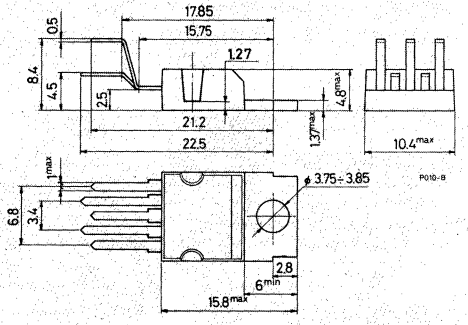
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

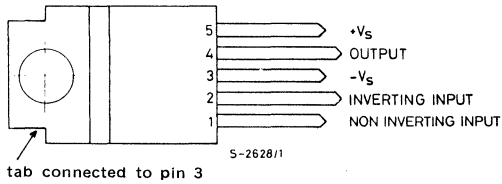
ORDERING NUMBER: L165V

MECHANICAL DATA

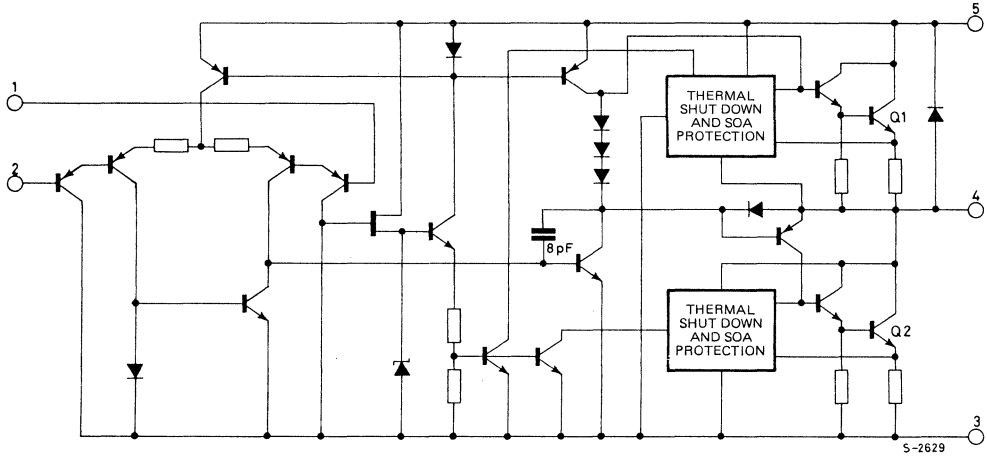
Dimensions in mm



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_s = ± 15V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 6		±18	V
I_d	Quiescent drain current	V_s = ± 18V			40	60	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage				± 2	±10	mV
I_{os}	Input offset current				±20	±200	nA
SR	Slew-Rate	G_V= 10			8		V/μs
		G_V= 1 (°)			6		
V_o	Output voltage swing	f = 1 kHz	I_p = 0.3A I_p = 3A		27 24		V_{pp}
		f = 10 kHz	I_p = 0.3A I_p = 3A		27 23		V_{pp}
R_i	Input resistance (pin 1)	f = 1 KHz		100	500		KΩ
G_v	Voltage gain (open loop)				80		dB
e_N	Input noise voltage	B = 10 to 10 000 Hz			2		μV
i_N	Input noise current				100		pA
CMR	Common mode rejection	$R_g \leqslant$ 10 KΩ G_V= 30 dB			70		dB
SVR	Supply voltage rejection	R_g= 22 kΩ V_{ripple}= 0.5 V_{rms} f_{ripple}= 100 Hz	G_v = 10		60		dB
			G_v = 100		40		dB
η	Efficiency	f = 1 kHz R_L= 4Ω	I_p = 1.6A; P_o = 5W		70		%
			I_p = 3A; P_o = 18W		60		%
T_{sd}	Thermal shut-down case temperature	P_{tot}= 12W			110		°C
		P_{tot}= 6W			130		

(°) Circuit of fig. 8.

Fig. 1 - Open loop frequency response

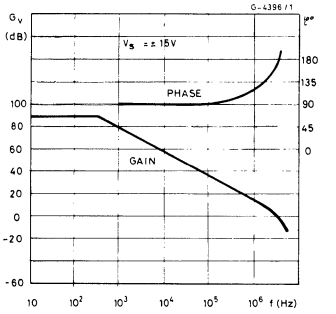


Fig. 2 - Closed-loop frequency response (circuit of fig. 8)

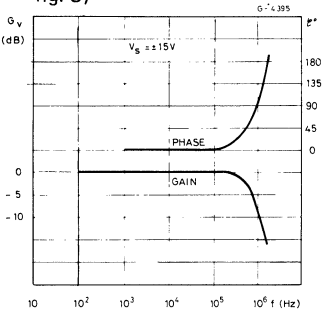


Fig. 3 - Large signal frequency response

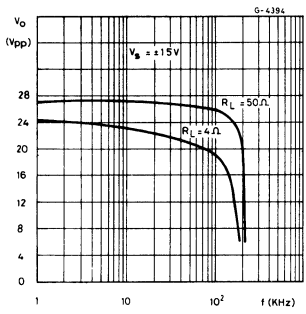


Fig. 4 - Maximum output current vs. voltage [V_{CE}] across each output transistor

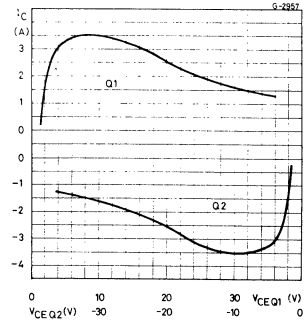


Fig. 5 - Safe operating area and collector characteristics of the protected power transistor

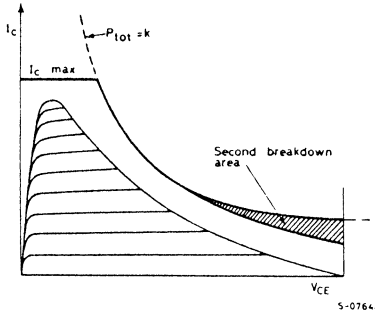


Fig. 6 - Maximum allowable power dissipation vs. ambient temperature

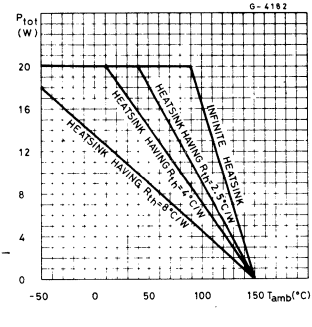


Fig. 7 - Application circuit ($G_V > 10$)

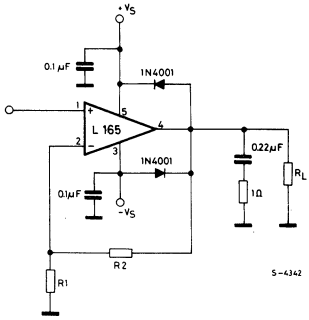


Fig. 8 - Unity gain configuration

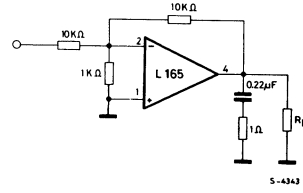
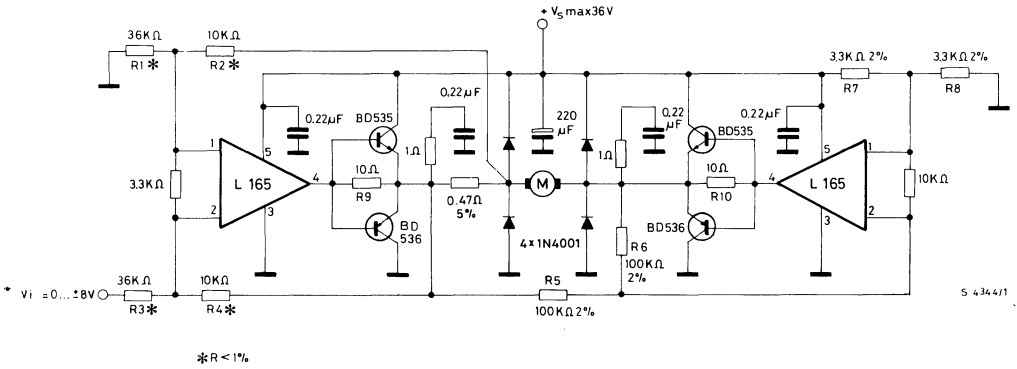
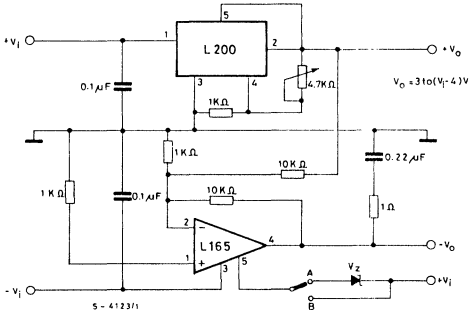


Fig. 9 - Motor current control circuit with external power transistors ($I_{motor} > 3.5A$)



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 10 - High current tracking regulator



A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – V_z must be chosen in order to verify
$2\,V_i - V_z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

Fig. 11 - Bidirectional speed control of DC motor

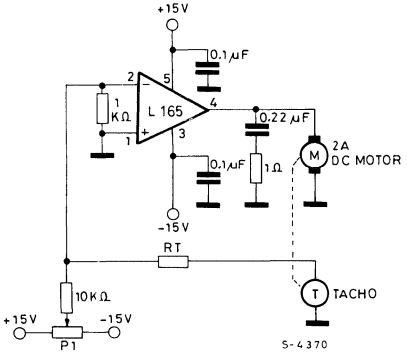


Fig. 12 - Split power supply

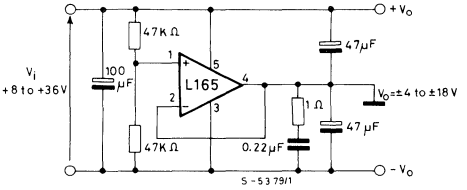
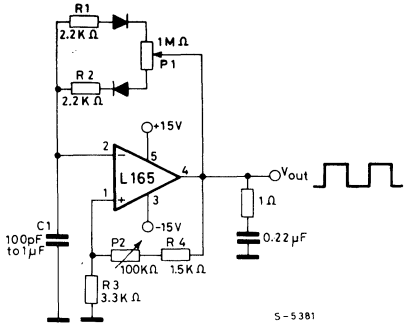
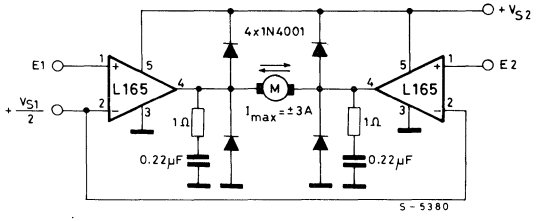


Fig. 13 - Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



P1 : duty-cycle adjust
P2 : frequency adjust (f = 700 Hz with C1= 10 nF, P2= 100 KΩ, f=25 Hz with C1= 10 nF, P2= 0)

Fig. 14 - Bidirectional DC motor control with TTL/C-MOS/μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} \geqslant V_{S1}$

E1, E2 = logic inputs

NOTE - For a more detailed description of the L165 and its applications, refer to SGS-TECHNICAL NOTE TN.150.

L194-5
L194-12
L194-15

POSITIVE VOLTAGE REGULATORS WITH RECTIFYING BRIDGE

- OUTPUT VOLTAGE: 5V, 12V AND 15V
- OUTPUT CURRENT UP TO 500 mA
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION
- OVERVOLTAGE PROTECTION (60V - 10 ms)

The L194-5, L194-12 and L194-15 are fixed voltage regulators assembled in Pentawatt® package. They incorporate a rectifying diode bridge with 7A surge current capability.

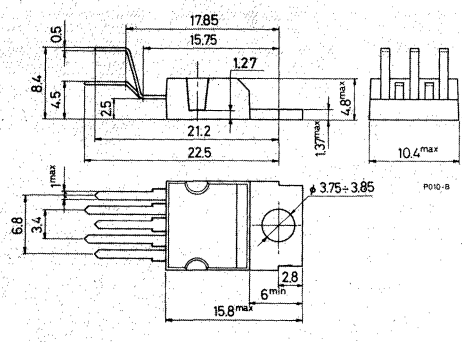
ABSOLUTE MAXIMUM RATINGS

V_i	Peak input voltage (10ms)	60	V
V_i	DC input voltage (at pin 2)	40	V
V_i	AC input voltage (rms)	28	V
V_R	Peak reverse voltage across each diode	80	V
I_D	Input diode repetitive current	2	A
I_{DS}	Input diode surge current (10 ms)	7	A
I_o	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to + 150	°C
T_j	Operating junction temperature	-25 to + 150	°C

ORDERING NUMBERS: L194-5V (V_o= 5V)
L194-12V (V_o= 12V)
L194-15V (V_o= 15V)

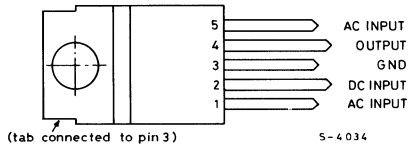
MECHANICAL DATA

Dimensions in mm

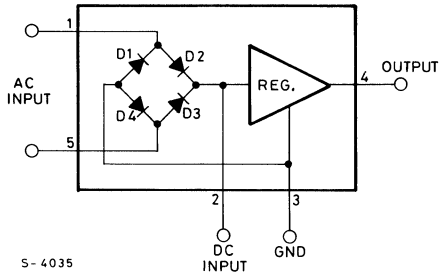


L194-5
L194-12
L194-15

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_d	Quiescent drain current	$I_o = 0$	V_i (pin 2) = 28V		5	14	mA
V_o	Output voltage	I_o = 100 mA	V_i = 15V (L194-5) V_i = 22V (L194-12) V_i = 25V (L194-15)	4.75 11.4 14.25	5 12 15	5.25 12.6 15.75	V
ΔV_o	Line Regulation	I_o = 100 mA	V_i = 8 to 18V (L194-5) V_i = 15 to 25V (L194-12) V_i = 18 to 28V (L194-15)		5 10 15		mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
$\frac{\Delta V_o}{V_o}$	Load Regulation	I_o = 10 to 250 mA	V_i = 15V (L194-5) V_i = 22V (L194-12) V_i = 25V (L194-15)		1 1 1		%
V_{i-o}	Dropout voltage (pin 2-4)	I_o = 300 mA			2	3	V
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 100 mA	V_i = 15V (L194-5) V_i = 22V (L194-12) V_i = 25V (L194-15)		0.3 0.6 0.8		mV/°C
I_o	Output current	$\frac{\Delta V_o}{V_o} \leq 1\%$	L194-5/12 L194-15 (*)	500 300			mA
I_{sc}	Short-circuit current		V_i = 15V (L194-5) V_i = 22V (L194-12) V_i = 25V (L194-15)		700 500 400		mA
I_p	Peak output current			0.7		1.4	A
SVR	Supply voltage Rejection	f = 100 Hz I_o = 200 mA ΔV_i = 10V	L194-5/12 L194-15		46 40		dB
R_o	Output Resistance	f = 1 kHz	I_o = 100 mA		80		mΩ
V_d	Diode Forward Voltage	I_f = 1A I_f = 5A			1.6 4.5		V

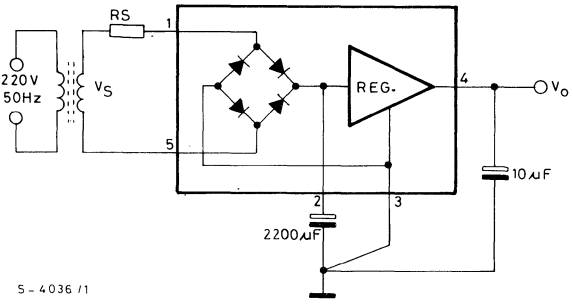
(*) See diagram of fig. 1.

APPLICATION CIRCUIT

In the design of power supplies using the L194, it must be always verified that:

$$I_{peak} = \frac{\sqrt{2}\, V_s}{R_s} < 7A$$

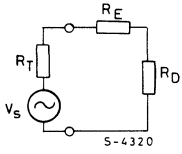
where R_s is the sum of the transformer resistance, the equivalent diode resistance and external resistors.



S-4036/1

APPLICATION INFORMATION

The Absolute Maximum Ratings guarantee a max of 40V at pin 2 with max peak current of 7A in the rectifying diodes.
To avoid to damage the device, a suitable transformer secondary must be used so that even when there are network variations the limits set are always respected during operation.
For example, with a nominal voltage of 24 V_{rms} the maximum variations due to the transformer tolerance are ± 20%.
In order to limit (to the maximum value allowed) the current peak, which occurs in diodes during switch-on, an external resistance R_E, in series with the secondary of the transformer, must be introduced.
Supposing that the capacitor of the filter is discharged at switch-on, the following equivalent circuit can be drawn:



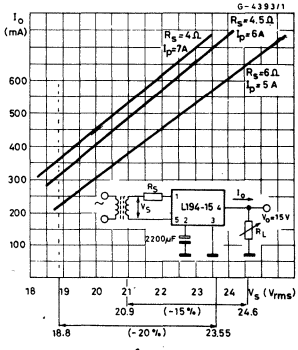
V_S = Secondary voltage.
R_T = Secondary resistances of transformer.
R_D = Resistance produced by the diode pair involved in conduction.

If values R_T and R_D are known R_E is calculated in such a way that the peak current at switch-on does not exceed 7A.

$$R_E \geqslant \frac{V_{S\ peak} - 7\ (R_T + R_D)}{7}$$

For the 5V, with the nominal voltage of the 10VA transformer at 12V and with a total voltage variation of ±15%, the transformer secondary is connected directly to pins 1 and 5.
For correct use of the device at 15V the graph in fig. 1 gives the max output current.

Fig. 1 - Guaranteed output current vs. secondary voltage



Note:
V_S nom = 24.6 V_{rms} for 220V ± 15%.
V_S nom = 23.55 V_{rms} for 220V ± 20%.

LINEAR INTEGRATED CIRCUIT

L200

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

- ADJUSTABLE OUTPUT CURRENT UP TO 2A (GUARANTEED UP TO T_j= 150°C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

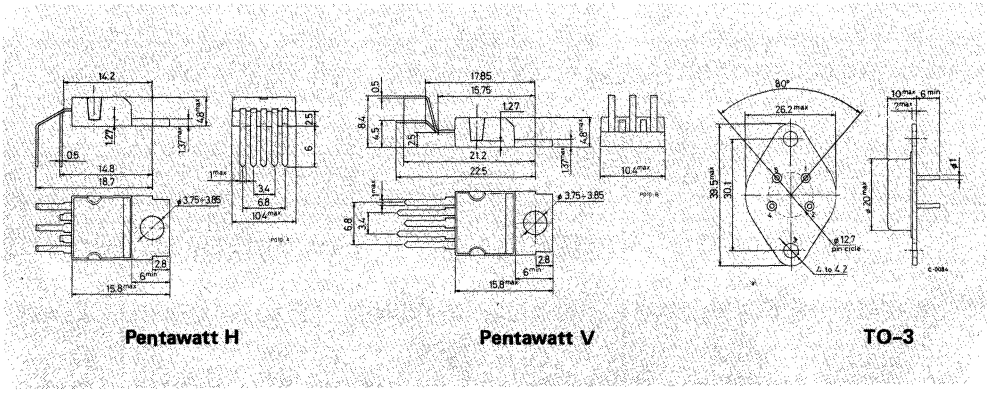
The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60V) make the L200 virtually blowout proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.

ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	40 V
V_i	Peak input voltage (10 ms)	60 V
ΔV_{i-o}	Dropout voltage	32 V
I_o	Output current	internally limited
P_{tot}	Power dissipation	internally limited
T_{stg}	Storage temperature	-55 to 150 °C
T_{op}	Operating junction temperature for L200C	-25 to 150 °C
	for L200	-55 to 150 °C

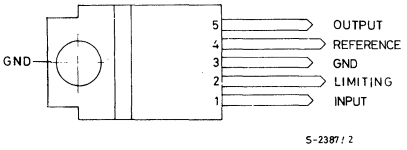
MECHANICAL DATA

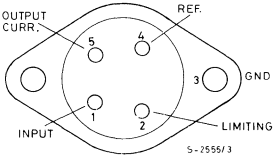
Dimensions in mm



Pentawatt H Pentawatt V TO-3

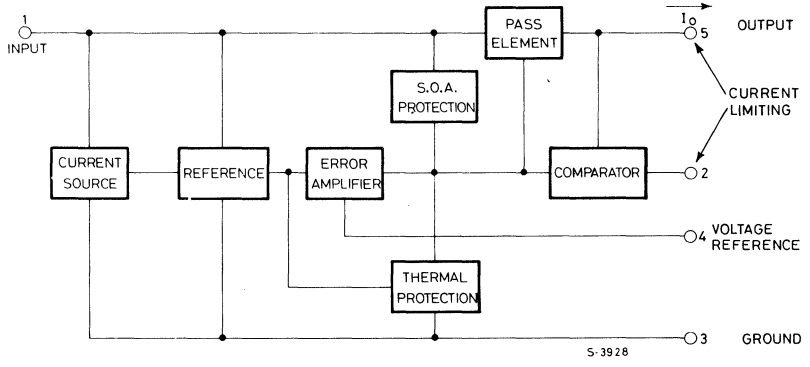
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



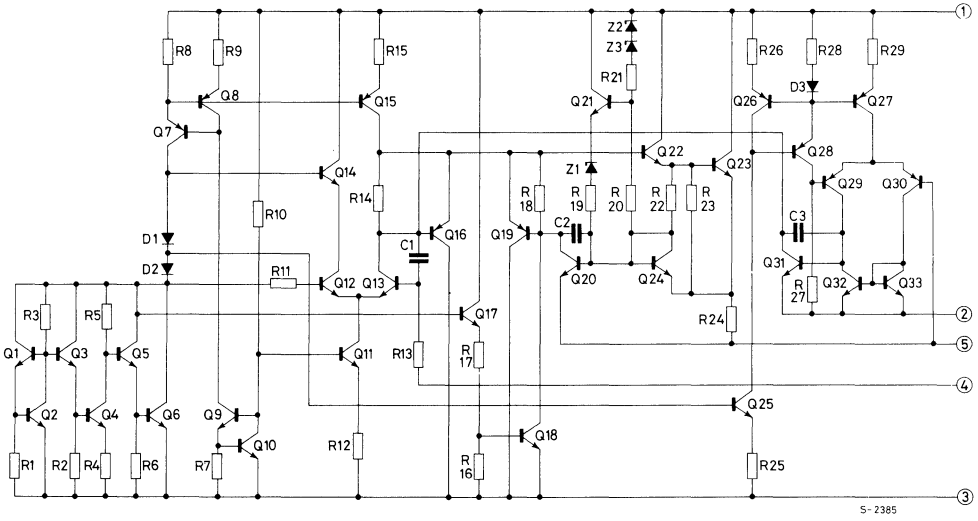


Type	Pentawatt®	TO-3
L 200		L 200 T
L 200 C	L 200 CH L 200 CV	L 200 CT

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	Pentawatt®
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent drain current (pin 3)	V_i = 20V		4.2	9.2	mA
e_N	Output noise voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		μV
V_o	Output voltage range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage load regulation (note 1)	ΔI_o = 2A ΔI_o = 1.5A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line regulation	V_o = 5V V_i = 8 to 18V	48	60		dB
SVR	Supply voltage rejection	V_o = 5V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
ΔV_{i-o}	Droupout voltage between pins 1 and 5	I_o = 1.5A $\Delta V_o \leqslant 2\%$		2	2.5	V
V_{ref}	Reference voltage (pin 4)	V_i = 20V I_o = 10 mA	2.64	2.77	2.86	V
ΔV_{ref}	Average temperature coefficient of reference voltage	V_i = 20V I_o = 10 mA for T_j = -25 to 125°C for T_j = 125 to 150°C		-0.25 -1.5		mV/°C mV/°C
I_4	Bias current at pin 4			3	10	μA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average temperature coefficient (pin 4)			-0.5		%/°C
Z_o	Output impedance	V_i = 10V $V_o = V_{ref}$ I_o = 0.5A f = 100 Hz		1.5		mΩ

CURRENT REGULATION LOOP

V_{SC}	Current limit sense voltage between pins 5 and 2	V_i = 10V $V_o = V_{ref}$ I_5 = 100 mA	0.38	0.45	0.52	V
$\frac{\Delta V_{sc}}{\Delta T \cdot V_{sc}}$	Average temperature coefficient of V_{SC}			0.03		%/°C
$\frac{\Delta I_o}{I_o}$	Current load regulation	V_i = 10V ΔV_o = 3V I_o = 0.5A I_o = 1A I_o = 1.5A		 1.4 1 0.9		 % % %
I_{sc}	Peak short circuit current	$V_i - V_o$ = 14V (pins 2 and 5 short circuited)			3.6	A

Note 1): A load step of 2A can be applied provided that input-output differential voltage is lower than 20V (see fig. 1).

Note 2): The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Fig. 1 - Typical safe operating area protection

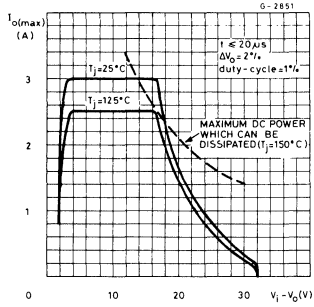


Fig. 2 - Quiescent current vs. supply voltage

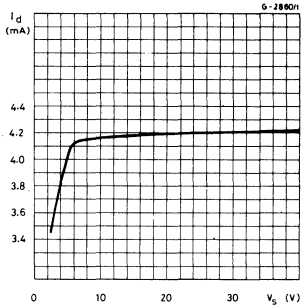


Fig. 3 - Quiescent current vs. junction temperature

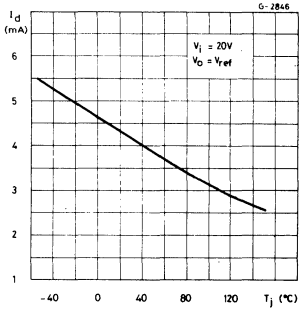


Fig. 4 - Quiescent current vs. output current

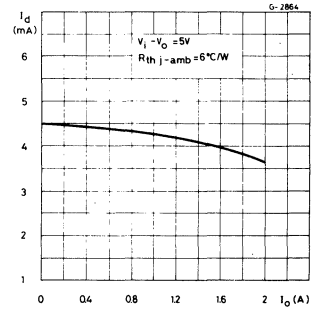


Fig. 5 - Output noise voltage vs. output voltage

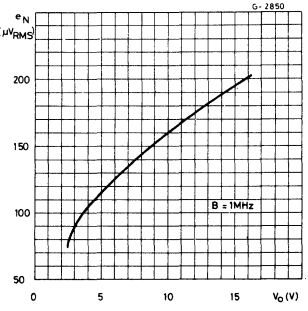


Fig. 6 - Output noise voltage vs. frequency

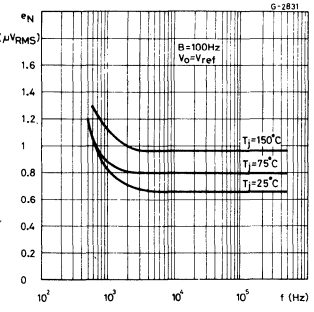


Fig. 7 - Reference voltage vs. junction temperature

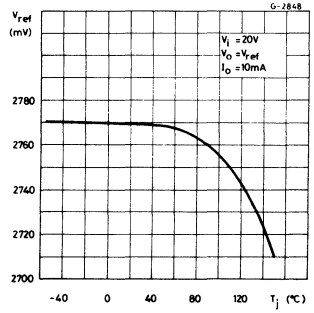


Fig. 8 - Voltage load regulation vs. junction temperature

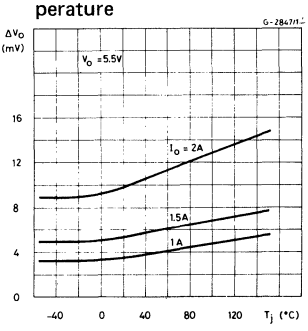


Fig. 9 - Supply voltage rejection vs. frequency

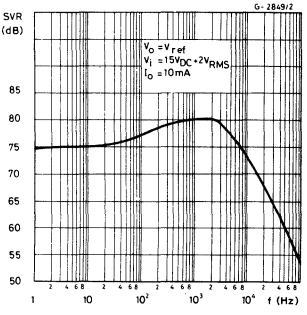


Fig. 10 - Dropout voltage vs. junction temperature

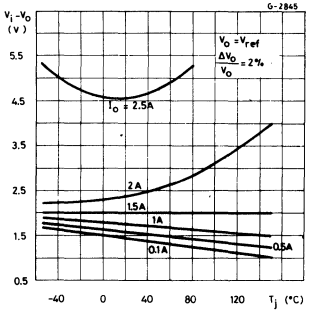


Fig. 11 - Output impedance vs. frequency

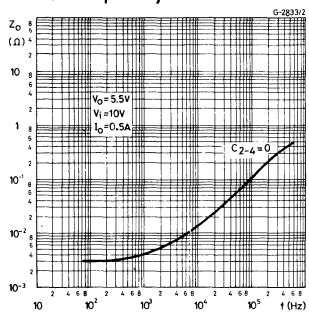


Fig. 12 - Output impedance vs. output current

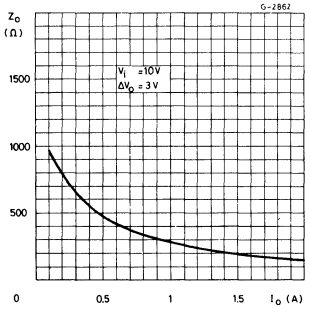


Fig. 13 - Voltage transient response

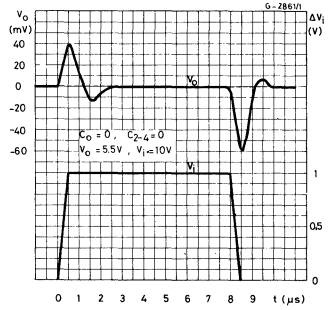


Fig. 14 - Load transient response

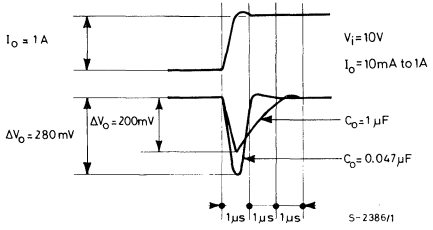


Fig. 15 - Load transient response

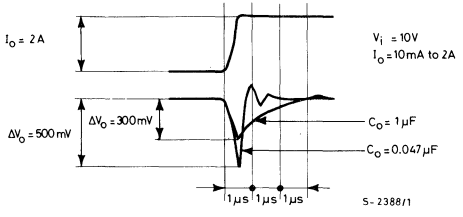
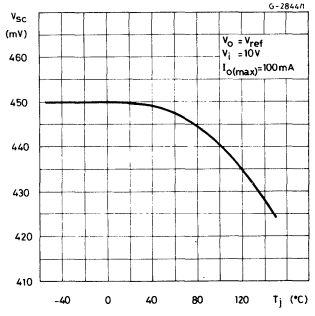


Fig. 16 - Current limit sense voltage vs. junction temperature



APPLICATION CIRCUITS

Fig. 17 - Programmable voltage regulator

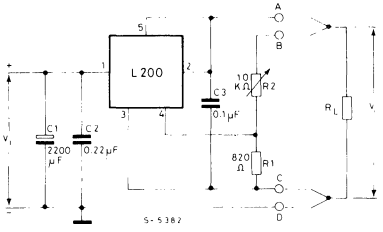


Fig. 18 - P.C. board and components layout of fig. 17 (1 : 1 scale)

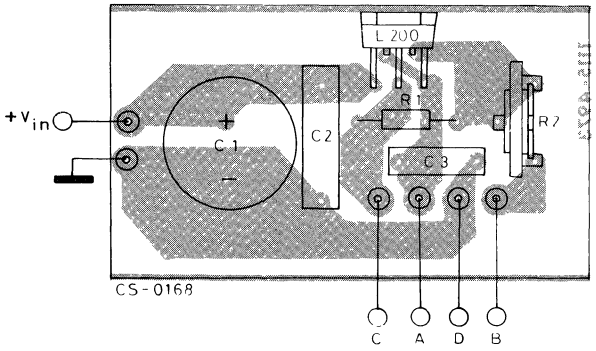


Fig. 19 - Programmable voltage regulator with current limiting

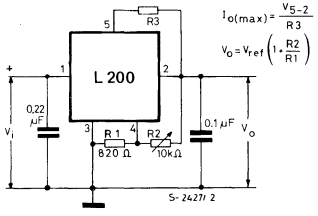


Fig. 20 - Programmable current regulator

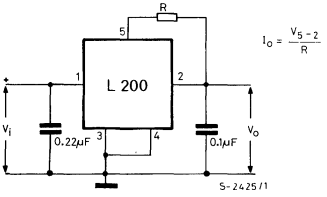


Fig. 21 - High current voltage regulator with short circuit protection

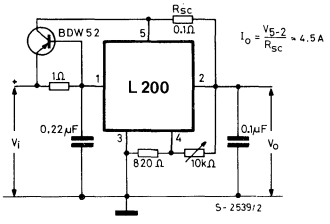
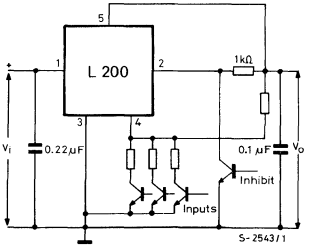
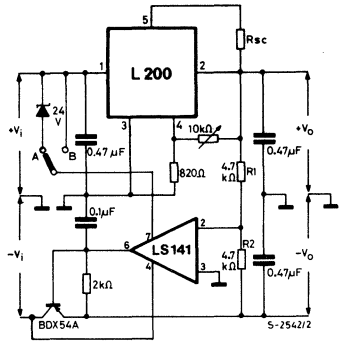


Fig. 22 - Digitally selected regulator with inhibit



APPLICATION CIRCUITS

Fig. 23 - Tracking voltage regulator



A : $V_{i(max)} \leqslant \pm 34V$; $3 < V_o < 30$.
B : $V_{i(max)} \leqslant \pm 22V$; $3 < V_o < 18$.

Fig. 24 - High current regulator with NPN pass transistor

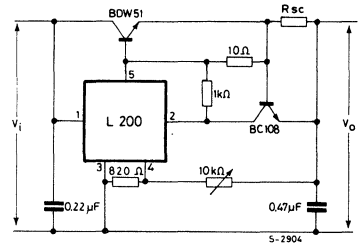
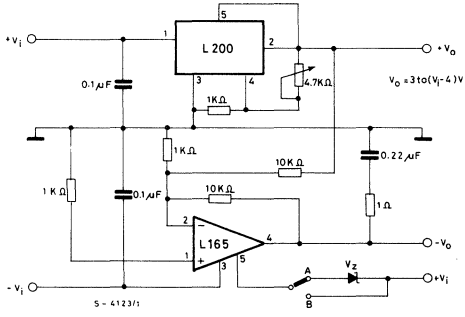


Fig. 25 - High current tracking regulator

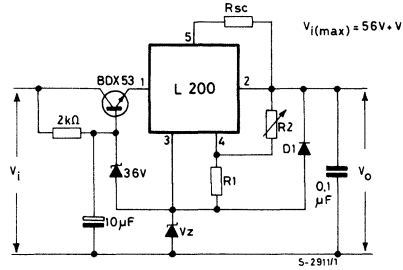


A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – V_z must be chosen in order to verify $2\,V_i - V_z \leqslant 36V$

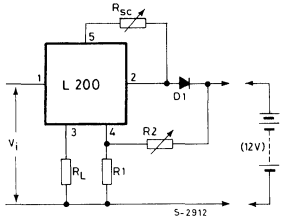
B: for $V_i \leqslant \pm 18V$

Fig. 26 - High input and output voltage



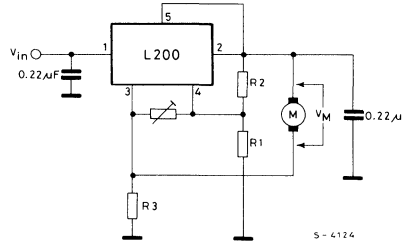
APPLICATION CIRCUITS (continued)

Fig. 27 - Constant current battery charger



The resistors R_1 and R_2 determine the final charging voltage and R_{sc} the initial charging current. D_1 prevents discharge of the battery throught the regulator.
The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12V/50 mA rating this will indicate incorrect connection.

Fig. 28 - 30W Motor speed control



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Fig. 29 - Low turn on

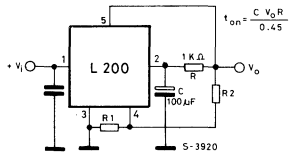
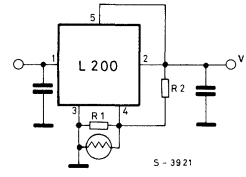
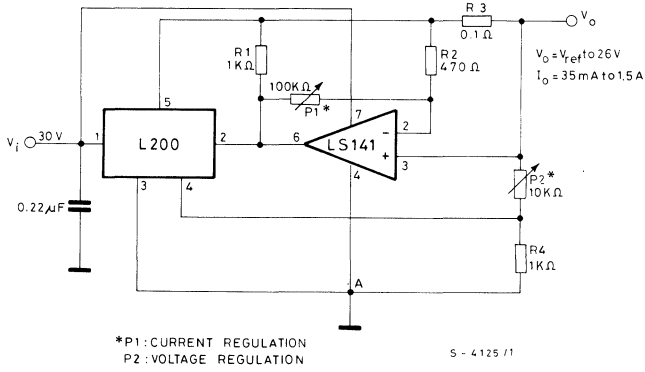


Fig. 30 - Light controller



APPLICATION CIRCUITS (continued)

Fig. 31 - Programmable voltage and current regulator



Note: Connecting point A to a negative voltage (for example-3V/10 mA) it is possible to extend the output voltage range down to 0V and to obtain the current limiting down to this level (output short-circuit condition).

NOTE - For a more detailed description of the L200 and its applications refer to SGS-TECHNICAL NOTES TN146 and TN150.

LINEAR INTEGRATED CIRCUITS

L201 L202
L203 L204

HIGH-VOLTAGE, HIGH-CURRENT 7 DARLINGTON ARRAYS

These high-voltage, high-current Darlington transistor arrays comprise seven NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak currents of 600 mA can be withstood, making them ideal for driving tungsten filament lamps.
The L 201 is a general-purpose array wich may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate circuit board layout and is priced to compete directly with discrete transistor alternatives.
The L 202 was specifically designed for use with 14 to 25V PMOS devices.
Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.
The L203 has a series base resistor to each Darlington pair allowing operation directly with TTL or CMOS operating at a supply voltage of 5V.
The L204 has a series base resistor to each Darlington pair, allowing operation directly with PMOS or CMOS utilizing supply voltage of 6 to 15V.
In all cases, the individual Darlington pair collector current rating is 500 mA. However, outputs may be paralleled for higher load current capability. The devices are supplied in a 16-lead dual in-line plastic package with copper frame.

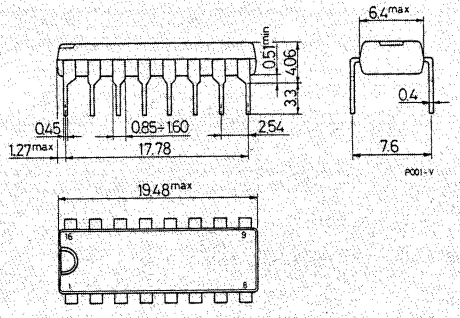
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (for **L 202, L 203** and **L 204**)	30	V
V_o	Output voltage (collector-emitter)	50	V
$V_{CEO(sus)}$	Collector-emitter sustaining voltage	36	V
I_C	Collector current	500	mA
I_B	Base current (for **L 201** only)	25	mA
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

ORDERING NUMBERS: L201B, L203B
L202B, L204B

MECHANICAL DATA

Dimensions in mm



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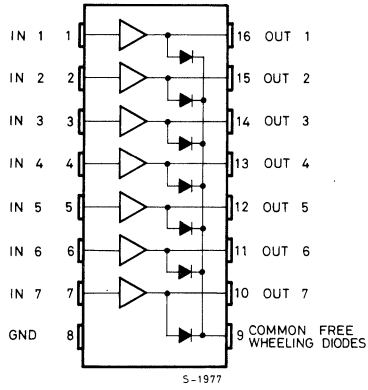
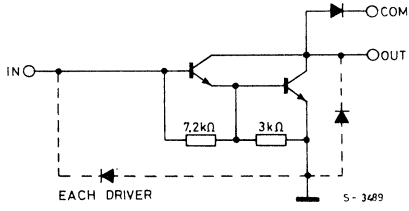
L201 L202 L203 L204

CONNECTION DIAGRAM (top view)

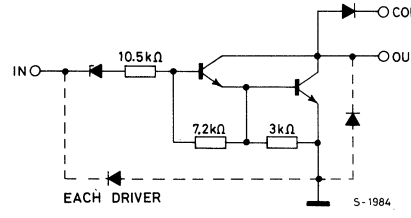


SCHEMATIC DIAGRAM

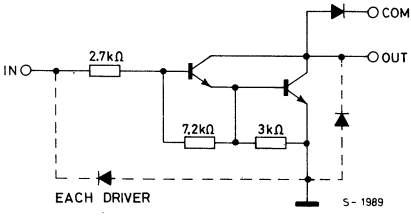
For L 201



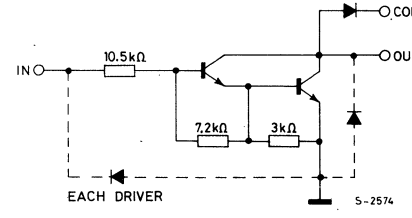
For L 202



For L 203



For L 204



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig. No.
I_{CEX}	Collector cutoff current	for **L 201** V_{CE} = 50V		0.2	3	μA	1
		for **L 202** V_{CE} = 50V V_i = 7V		0.2	3	μA	2
		for **L 203, L 204** V_{CE} = 50V I_i = 0		0.2	3	μA	1
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 350 mA I_B = 500 μA I_C = 200 mA I_B = 350 μA I_C = 100 mA I_B = 250 μA		1.25 1 0.85	1.6 1.3 1.1	V V V	3
I_i	Input current	for **L 202** V_i = 17V		0.75	1.3	mA	
		for **L 203** V_i = 3.85V		0.9	1.35	mA	5
		for **L 204** V_i = 5V V_i = 12V		0.35 1.1	0.5 1.45	mA mA	
$I_{C(off)}$		V_{CE} = 50V I_i = 25 μA			25	μA	4
V_i	Input voltage	for **L 202** I_C = 300 mA V_{CE} = 2V		10.5	13	V	
		for **L 203** I_C = 300 mA V_{CE} = 2V I_C = 250 mA V_{CE} = 2V		1.8 1.7	3 2.4	V V	7
		for **L 204** V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 350 mA		4.5 5	6 8	V V	
h_{FE}	DC current gain (for **L 201** only)	I_C = 350 mA V_{CE} = 2V	1000	3000		–	3
I_R	Parallel diode reverse current	V_R = 50V		0.5	50	μA	6
V_F	Parallel diode forward voltage	I_F = 350 mA		1.4	2	V	8
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o			5	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o			5	μs	–

TEST CIRCUITS

Fig 1 - For L 201, L 203 and L 204

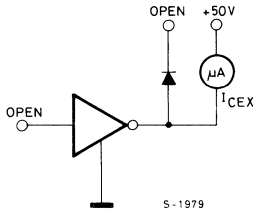


Fig. 2 - For L 202

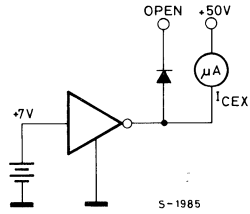


Fig. 3 - For L 201, L 202, L 203 and L 204

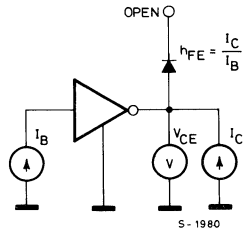


Fig. 4 - For L 201, L 202, L 203 and L 204

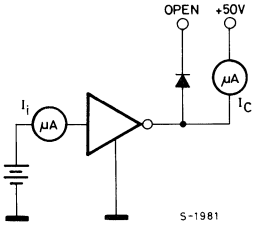


Fig. 5 - For L 202, L 203, and L 204

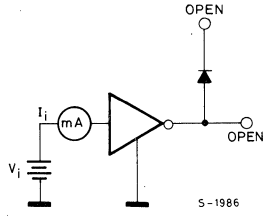


Fig. 6 - For L 201, L 202, L 203 and L 204

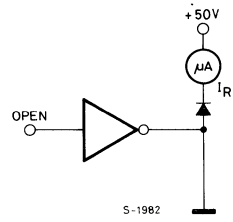


Fig. 7 - For L 202, L 203, and L 204

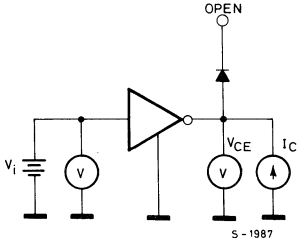
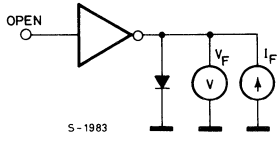
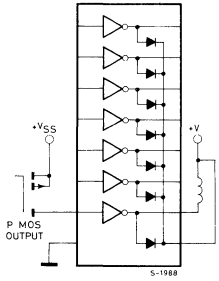


Fig. 8 - For L 201, L 202, L 203 and L 204

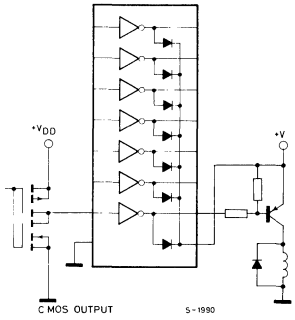


APPLICATION CIRCUITS

PMOS to load
(L 202 and L 204)



Buffer for high current load
(L 203 and L 204)



TTL to load (L 203)

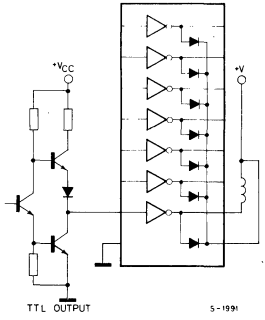


Fig. 9 - DC current gain. vs. collector current (for L 201)

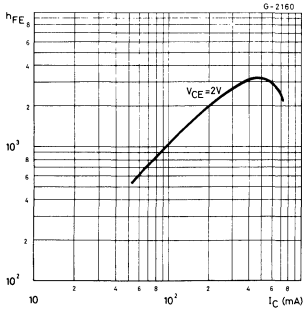


Fig. 10 - Collector current vs. collector emitter saturation voltage

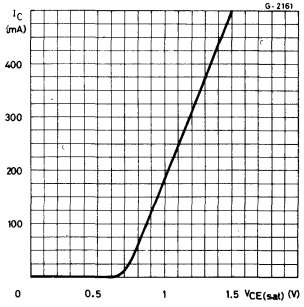


Fig. 11 - Peak collector current as a function fo duty cycle and number of outputs

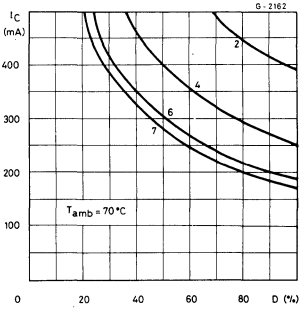


Fig. 12 - Input current vs. input voltage (for L 202 and L 204)

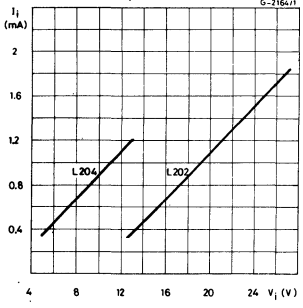


Fig. 13 - Input current vs. input voltage (L 203)

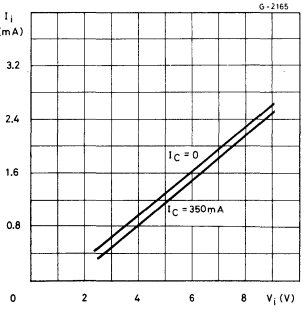
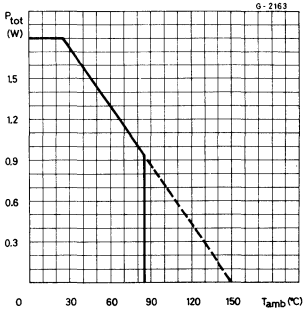


Fig. 14 - Power rating chart



SGS L290

LINEAR INTEGRATED CIRCUIT

TACHOMETER CONVERTER

The L290, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L291 and L292 which together form a complete 3-chip DC motor positioning system for applications such as carriage/daisy-wheel position control in typewriters.
The L290/1/2 system can be directly controlled by a microprocessor. The L290 integrates the following functions:

- tacho voltage generator (F/V converter)
- reference voltage generator
- position pulse generator.

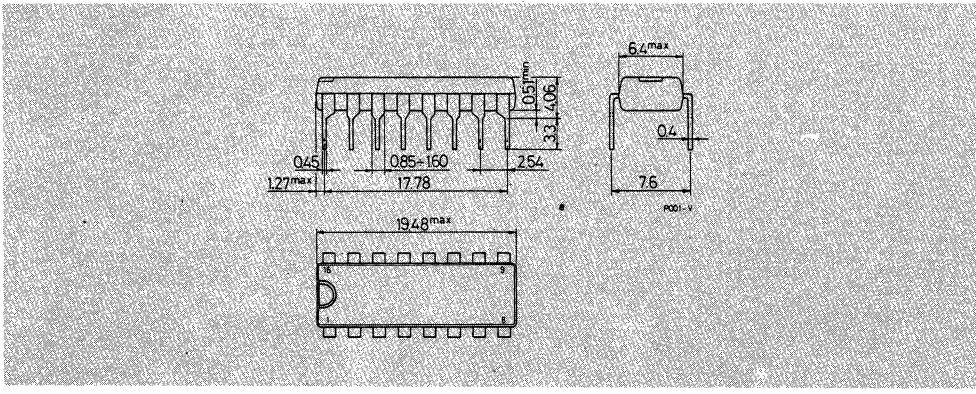
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i (FTA, FTB, FTF)	Input signals	± 7	V
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to +150	°C

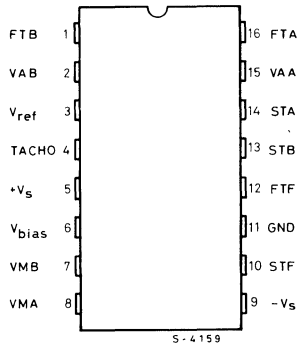
ORDERING NUMBER: L290 B

MECHANICAL DATA

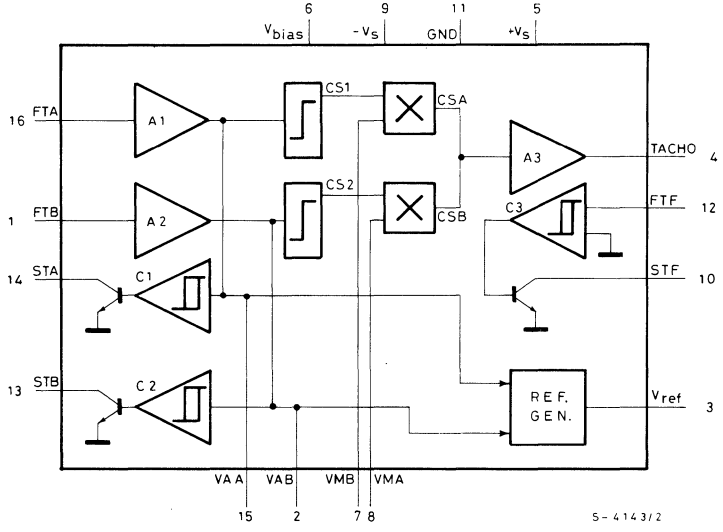
Dimensions in mm



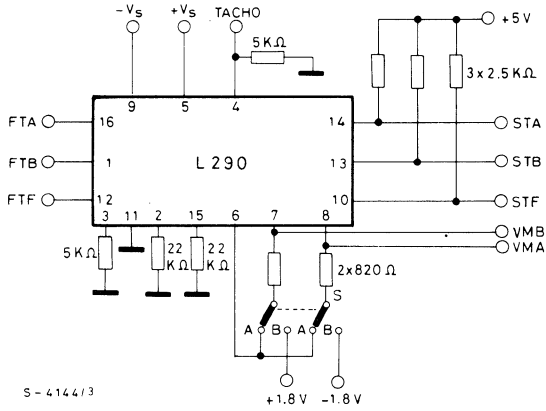
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, S in (A), $V_s = \pm 12V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		±10		±15	V
I_d	Quiescent drain current	$V_s = \pm 15V$		13	20	mA

INPUT AMPLIFIERS (A_1 and A_2)

FTA, FTB	Input signal from encoder (pin 1, 16)	$f_{max} = 20$ KHz	±0.4		±0.6	V_p
V_{os}	Output offset voltage (pin 2, 15)	FTA = FTB = 0V			± 55	mV
I_b	Input bias current (pin 1, 16)			0.15		μA
G_v	Voltage gain	f = 10 KHz FTA=FTB=±0.6V_p	22	23	24	dB
V_o	Output voltage swing (pin 2, 15)	FTA= FTB= ± 1 V_p	±9.5			V

ELECTRICAL CHARACTERISTICS (continued)

Parameters	Test conditions	Min.	Typ.	Max.	Unit
COMPARATORS WITH HYSTERESIS (C_1, C_2 and C_3)					
V_{THP}(°) Positive Threshold voltage (pin 2, 12, 15)	C_1 and C_2	550		850	mV
	C_3	700		900	mV
V_{THN}(°°) Negative Threshold voltage (pin 2, 12, 15)	C_1 and C_2	55		175	mV
	C_3	570		830	mV
V_L Output voltage (low level) (pin 10, 13, 14)	I_o = 2 mA FTA= FTB= FTF= 0V		0.2	0.4	V
I_{leak} (pins 10, 13, 14)	FTA= FTB= 0.5V V_{CE}= 5V FTF= 1V			1	μA
REFERENCE GENERATOR					
V_{ref} DC reference voltage (pin 3)	FTA= FTB= ± 0.5V_p(*) I_{ref}= 1 mA	4.5	5	5.5	V
I_{ref} Output current (pin 3)				1.4	mA
"TACHO" AMPLIFIER (A_3)					
V_{os} Output offset voltage (pin 4)	FTA= ± 15 mV FTB= 0.5V			± 80	mV
V_o DC output voltage (pin 4)	FTA= FTB= ±0.5Vp (**) V_{o1}	5.4	6	6.6	V
	V_{MA}= V_{MB}= ±1.25V_p (***) V_{o2}	-5.4	-6	-6.6	
ΔV_o	V_{o1} + V_{o2}	-150		+150	mV
V_o Output voltage swing (pin 4)	S in (B) FTA= FTB= 0.5V	9			V
	S in (B) FTA= FTB= -0.5V	-9			
V_{MA} V_{MB} Multiplier input voltage (pin 7, 8)			± 1.25	± 1.7	Vp
V_{bias} Bias voltage (pin 6)	FTA and FTB floating	-6.5		-8	V

(°) : FTA = FTB = FTF = 0 / 1V

(°°) : FTA = FTB = FTF = 1V / 0

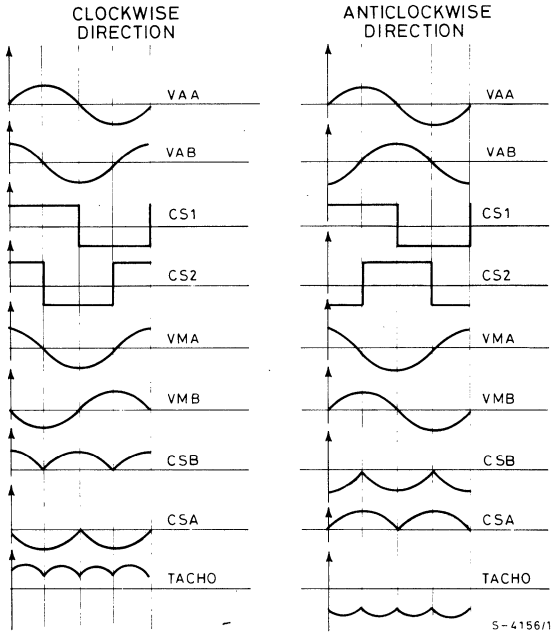
Note : Phase relationship between the signals:

* FTA : 0° FTB : 90°

** FTA : 0° FTB : -90° V_{MA}= 90° V_{MB}= 0°

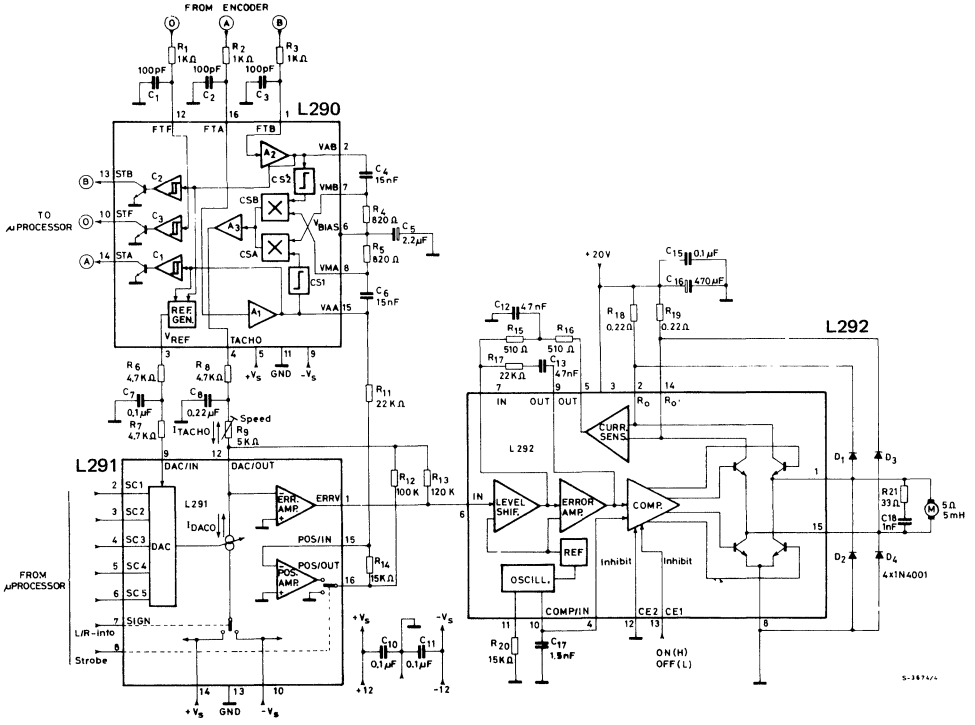
*** FTA : 0° FTB : 90° V_{MA}= 90° V_{MB}= 180°

WAVEFORMS (Neglecting threshold voltage level of the comparators)



SYSTEM DESCRIPTION : refer to the L292 data sheet

Fig. 1 - Complete application circuit



L291

LINEAR INTEGRATED CIRCUIT

5 BIT - D/A CONVERTER AND POSITION AMPLIFIER

The L291, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L290 and L292 to form a complete 3 chip DC motor positioning system for applications such as carriage/daisy-wheel position control in typewriters.
The L290/1/2 system can be directly controlled by a microprocessor.
The L291 integrates the following functions:

- 5 bit D/A converter ($\frac{1}{2}$ LSB max linearity error)
- error amplifier
- position amplifier

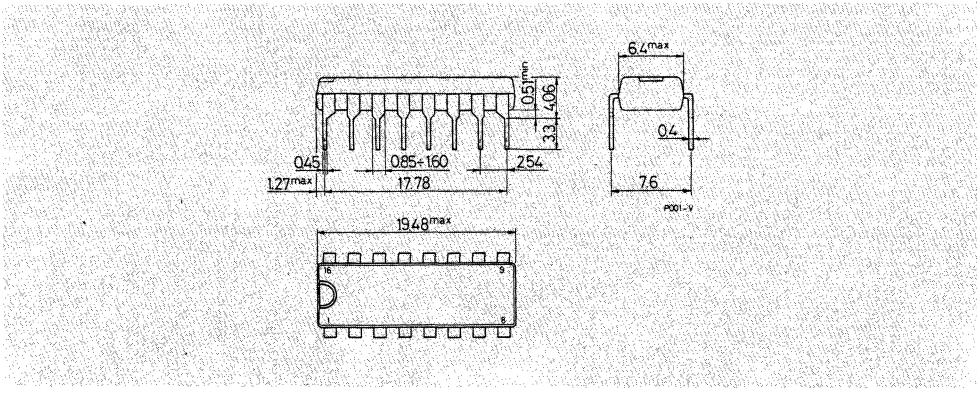
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
P_{tot}	Total power dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

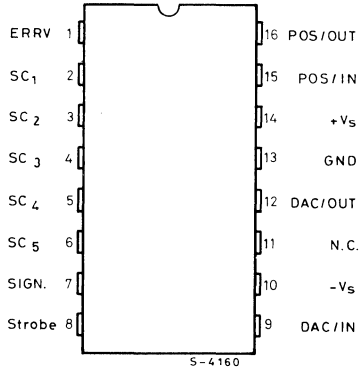
ORDERING NUMBER: L291 B

MECHANICAL DATA

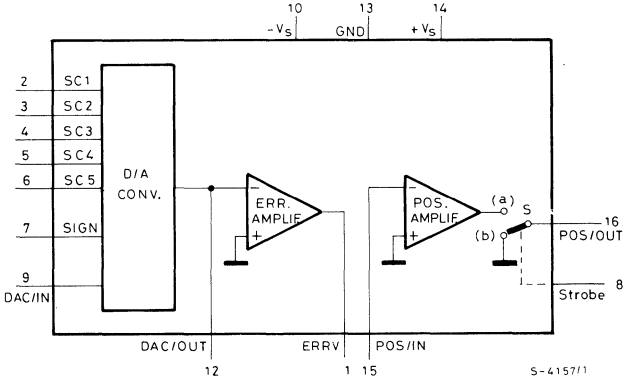
Dimensions in mm



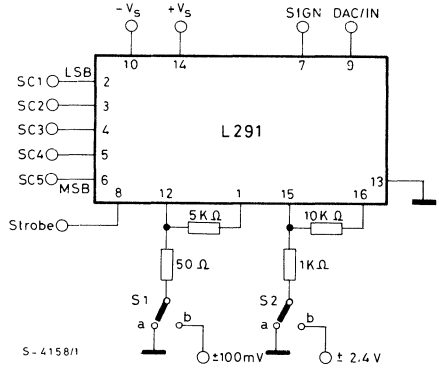
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the circuit, S1 and S2 in (a), V_s = ± 12V, T_{amb} = 25°C, unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 10		± 15	V
I_d	Quiescent drain current	V_s = ± 15V		6.5	10	mA

POSITION AMPLIFIER

V_{strobe}	Enable voltage level	V_L (S in (a)) *	0		0.8	V
		V_H (S in (b)) *	2.4		$+V_s$	V
V_{os}	Output offset voltage (pin 16)	V_{strobe}= V_L; G_v= 20 dB			± 50	mV
I_b	Input bias current (pin 15)	V_{strobe}= V_L			0.3	μA
V_o	Output voltage swing (pin 16)	V_{strobe}=V_L; S2 in(b); V_s=±10.8V	± 9			V
V_R	Residual output voltage (pin 16)	V_{strobe}= V_H			± 20	mV

* See block diagram and the note for Position Amplifier.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
D/A CONVERTER						
I_{ref}	Current reference input range (pin 9)		0.3		1.2	mA
V_{os}	Current reference offset voltage (pin 9)	I_{ref}= 0.3 to 1.2 mA All inputs high			± 20	mV
I_o	Output current range (pin 12)				1.4	mA
I_o	Output current (pin 12)	I_{ref}= 0.722 mA SIGN = L (I_{o1}) SC1 to SC5 = L	-1.358	-1.4	-1.442	mA
		SIGN = H (I_{o2})	+1.358	+1.4	+1.442	
ΔI_o		$I_{o1} + I_{o2}$	-21		+21	μA
	Linearity error	I_{ref}= 0.722 mA			1.61	%FS
I_{os}	Pin 12 output offset current (including Error Amplifier bias current)	All inputs high			± 0.4	μA
V_L	Low voltage level (digital inputs)	SC1 = LSB SC5 = MSB	0		0.8	V
V_H	High voltage level (digital inputs)		2.4		+V_S.	V
I_L	Digital inputs current (low state)	V_L= 0.4V			-50	μA
I_H	Digital inputs current (high state)	V_H= +V_s			1	μA
ERROR AMPLIFIER						
V_{os}	Output offset voltage (pin 1)	I_{ref}= 0.5 mA; All inputs high G_V= 40 dB			± 200	mV
I_o	Output current (pin 1)				± 5	mA
V_o	Output voltage swing (pin 1)	All inputs high S1 in (b); R_L= 10 KΩ	± 7.4		± 8.4	Vp

D/A Converter

The L291 contains a 5-bit D/A converter accepting a binary code and generating a bipolar output current, the polarity of which depends on the SIGN input. The amplitude of the output current is a multiple of a reference current I_{ref}.
The maximum output current is

$$I_{FS} = \pm \frac{31}{16} I_{ref}$$

The following table shows the value of I_o for different input codes. Note that the input bits are active low.

DIGITAL INPUT WORD						Output Current I_o
SIGN	SC5	SC4	SC3	SC2	SC1	
L	L	L	L	L	L	$-\frac{31}{16} I_{ref}$
L	H	H	H	H	L	$-\frac{1}{16} I_{ref}$
X	H	H	H	H	H	0
H	H	H	H	H	L	$+\frac{1}{16} I_{ref}$
H	L	L	L	L	L	$+\frac{31}{16} I_{ref}$

X = indifferent
L = low
H = high

This D/A converter has a maximum linearity error equal to ± 1/2 LSB (or ± 1.61% Full Scale); that guarantees its monotonicity.

Error Amplifier

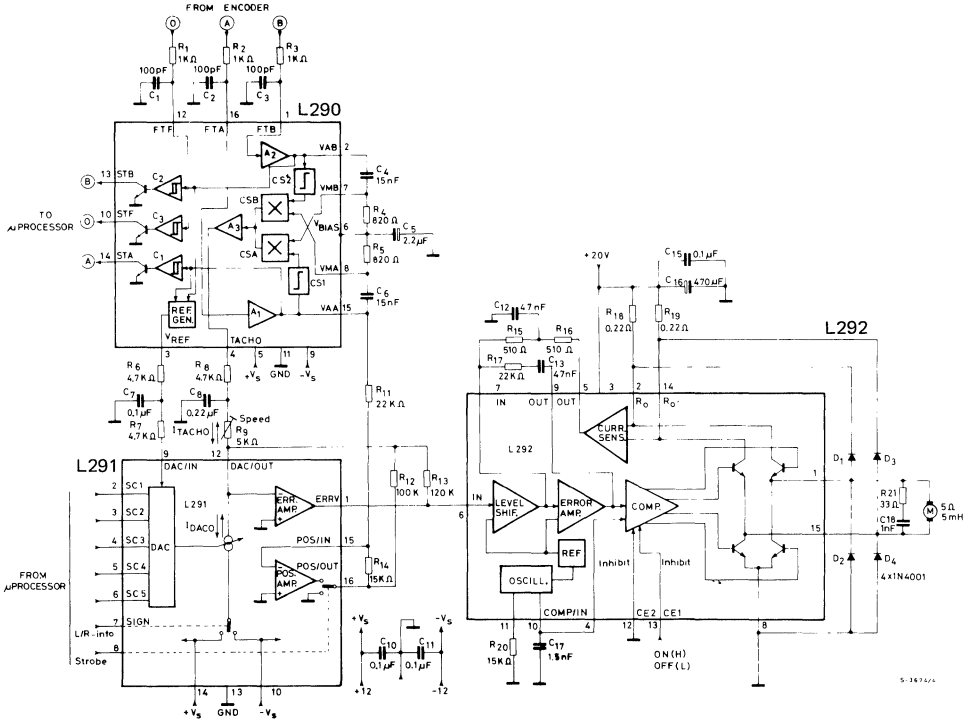
In order to have a good stability, the Error Amplifier must work with a closed loop gain greater or equal than 20 dB.

Position Amplifier

It is inserted by means of the strobe signal, TTL and microprocessor compatible. Its output is connected to pin 16 when V_{strobe}= Low; pin 16 is grounded for V_{strobe}= High.

SYSTEM DESCRIPTION: refer to the L292 data sheet.

Fig. 1 - Complete application circuit



L292

LINEAR INTEGRATED CIRCUIT

SWITCH-MODE DRIVER FOR DC MOTORS

The L292 is a monolithic LSI circuit in 15-lead MULTIWATT® package. It is intended for use, together with L290 and L291, as a complete 3-chip DC motor positioning system for applications such as carriage/daisy-wheel position control in typewriters.
The L290/1/2 system can be directly controlled by a microprocessor. The outstanding characteristics of the L292 are:

- Driving capability: 2A, 36V, 30 KHz.
- 2 Logic chip enable.
- External loop gain adjustment.
- Single power supply (18 to 36V).
- Input signal symmetric to ground.
- Thermal protection.

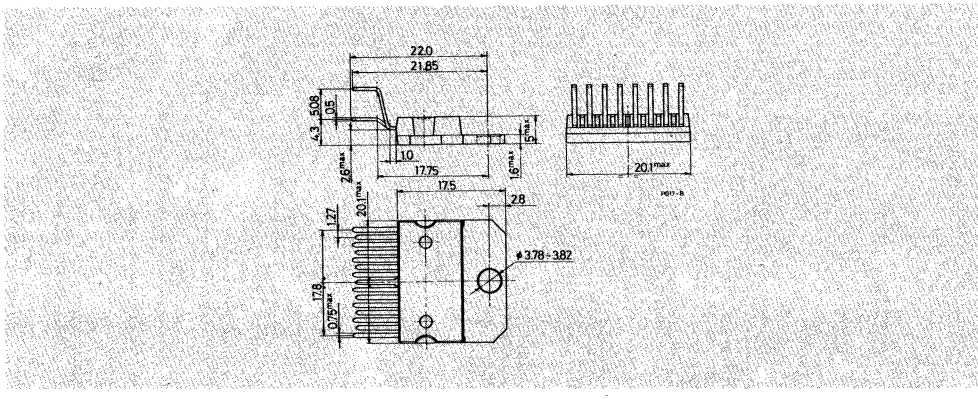
ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	36	V
V_i	Input voltage	-15 to $+V_s$	V
$V_{inhibit}$	Inhibit voltage	0 to V_s	V
P_{tot}	Total power dissipation (T_{case} = 75°C)	25	W
T_{stg}	Storage and junction temperature	-40 to +150	°C

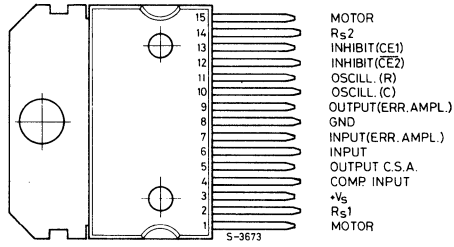
ORDERING NUMBER: L292

MECHANICAL DATA

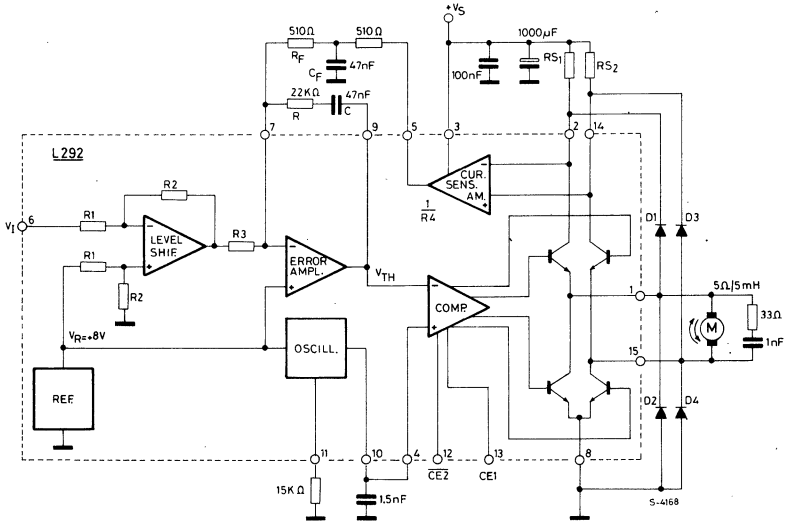
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



$D_1 \cdot D_2 \cdot D_3 \cdot D_4$ = High speed diodes (BYW 72 or equivalent)

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, f_{osc}= 20 KHz unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			18		36	V
I_d	Quiescent drain current	V_s = 20V (offset null)			30	50	mA
V_{os}	Input offset voltage (pin 6)	V_s = 36V I_o = 0				±350	mV
$V_{inh.}$	Inhibit low level (pin 12, 13)					2	V
	Inhibit high level (pin 12, 13)			3.2			V
$I_{inh.}$	Low voltage condition	$V_{inh.}$ (L)= 0.4V				-100	μA
	High voltage conditions	$V_{inh.}$ (H)= 3.2V				10	μA
I_i	Input current (pin (6)	V_I = -8.8V V_I = +8.8V				-1.8 0.5	mA mA
V_i	Input voltage (pin 6)	R_{s1}= R_{s2}=0.2Ω	I_o= 2A		9.1		V
			I_o= -2A		-9.1		V
I_o	Output current	V_I = ± 9.8V R_{s1}= R_{s2}= 0.2Ω		± 2			A
V_D.	Total drop out voltage	(inluding sensing resistors)	I_o= 2A			5	V
			I_o= 1A			3,5	V
V_{RS}	Sensing resistor voltage drop	T_j = 150°C I_o= 2A				0.44	V
$\frac{I_o}{V_i}$	Transconductance	R_{s1}= R_{s2}= 0.2Ω		205	220	235	mA/V
		R_{s1}= R_{s2}= 0.4Ω			120		mA/V
f_{osc}	Frequency range (pin 10)			1		30	KHz

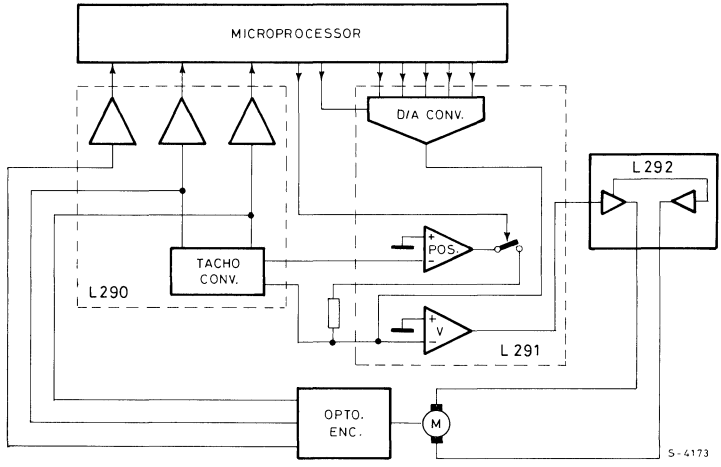
TRUTH TABLE

$V_{inhibit}$		Output stage condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal operation
H	L	Disabled
H	H	Disabled

SYSTEM DESCRIPTION

The L290, L291 and L292 are intended to be used as a 3-chip microprocessor controlled positioning system. These devices may be used separately - particularly the L292 motor driver - but since they will usually be used together, a description of a typical L290/1/2 system follows.

Fig. 1 - System block diagram



The system operates in two modes to achieve high-speed, high-accuracy positioning.
Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes a 5-bit control word that sets the system speed dependent on the distance to travel.
When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open-loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processor signal thus reducing accelerating torque.
The motor continues to run at top speed but under closed-loop control.
As the target position is approached, the microprocessor lowers the value of the speed-demand word; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed.
At that time, the microprocessor orders a switch to the position mode, (strobe signal at pin 8 of L291) and within 3 to 4 ms the L292 drives the motor to a null position, where it is held by electronic "detenting".

SYSTEM DESCRIPTION (continued)

The mechanical/electrical interface consists of an optical encoder which generates two sinusoidal signals 90° out of phase (leading or lagging according to the motor direction) and proportional in frequency to the speed of rotation. The optical encoder also provides an output at one position on the disk which is used to set the initial position.
The opto encoder signals, FTA and FTB are filtered by the networks R_2 C_2 and R_3 C_3 (referring to Fig. 4) and are supplied to the FTA/FTB inputs on the L290.
The main function of the L290 is to implement the following expression:

$$\text{Output signal (TACHO)} = \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|} - \frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|}$$

Thus the mean value of TACHO is proportional to the rotation speed and its polarity indicates the direction of rotation.
The above function is performed by amplifying the input signals in A_1 and A_2 to obtain V_{AA} and V_{AB} (typ. 7 V_p). From V_{AA} and V_{AB} the external differentiator RC networks R_5 C_6 and R_4C_4 give the signals V_{MA} and V_{MB} which are fed to the multipliers.
The second input to each multiplier consists of the sign of the first input of the other multiplier before differentiation, these are obtained using the comparators C_{S1} and C_{S2}. The multiplier outputs, C_{SA} and C_{SB}, are summed by A_3 to give the final output signal TACHO. The peak-to-peak ripple signal of the TACHO can be found from the following expression:

$$V_{ripple\ p-p} = \frac{\pi}{4}(\sqrt{2} - 1) \cdot V_{thaco\ DC}$$

The max value of TACHO is:

$$V_{tacho\ max} = \frac{\pi}{4}\sqrt{2} \cdot V_{thaco\ DC}$$

Using the comparators C_1 and C_2 another two signals from V_{AA} and V_{AB} are derived - the logic signals STA and STB.
These signals are used by the microprocessor to determine the position by counting the pulses.
The L290 internal reference voltage is also derived from V_{AA} and V_{AB}:

$$V_{ref} \equiv |V_{AA}| + |V_{AB}|$$

This reference is used by the D/A converter in the L291 to compensate for variations in input levels, temperature changes and ageing.
The "one pulse per rotation" opto encoder output is connected to pin 12 of the L290 (FTF) where it is squared to give the STF logic output for the microprocessor.
The TACHO signal and V_{ref} are sent to the L291 via filter networks R_8 C_8 R_9 and R_6 C_7 R_7 respectively. Pin 12 of this chip is the main summing point of the system where TACHO and the D/A converter output are compared.
The input to the D/A converter consists of 5 bit word plus a sign bit supplied by the microprocessor. The sign bit represents the direction of motor rotation. The (analogue) output of the D/A converter - DAC/OUT - is compared with the TACHO signal and the resulting error signal is amplified by the error amplifier, and subsequently appears on pin 1.

SYSTEM DESCRIPTION (continued)

The ERRV signal (from pin 1, L291) is fed to pin 6 of the final chip, the L292 H-bridge motor-driver. This input signal is bidirectional so it must be converted to a positive signal because the L292 uses a single supply voltage. This is accomplished by the first stage - the level shifter, which uses an internally generated 8V reference.

This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_{20}, C_{17} - pins 11 and 10) where:

$$f_{osc} = \frac{1}{2RC} \qquad \text{(with } R \geqslant 8.2\ K\Omega\text{)}$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30 KHz.

Motor current is regulated by an internal loop in the L292 which is performed by the resistors R_{18}, R_{19} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.

The choice of the external components in these RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements. The values shown in the diagram are for a 5Ω, 5 mH motor. (See L292 Transfer Function Calculation in Application Information).

The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.

The interval between one side of the bridge switching off and the other switching on, τ, is programmed by C_{17} in conjunction with an internal resistor R_τ.

This can be found from:

$$\tau = R_\tau \cdot C_{pin\ 10}. \quad (C_{17} \text{ in the diagram})$$

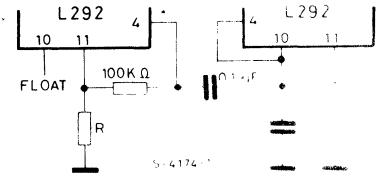
Since R_τ is approximately 1.5 KΩ and the recommended τ to avoid simultaneous conduction is 2.5 μs $C_{pin\ 10}$ should be around 1.5 nF.

The current sense resistors R_{18} and R_{19} should be high precision types (maximum tolerance ± 2%) and the recommended value is given by:

$$R_{max} \cdot I_{o\ max} \leqslant 0.44V$$

It is possible to synchronize two L292's, if desired, using the network shown in fig. 2.

Fig. 2



Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively).

SYSTEM DESCRIPTION (continued)

Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18V.
The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generates spikes as high as 1.5V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see fig. 3).

Fig. 3

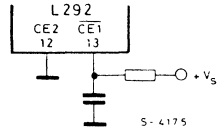
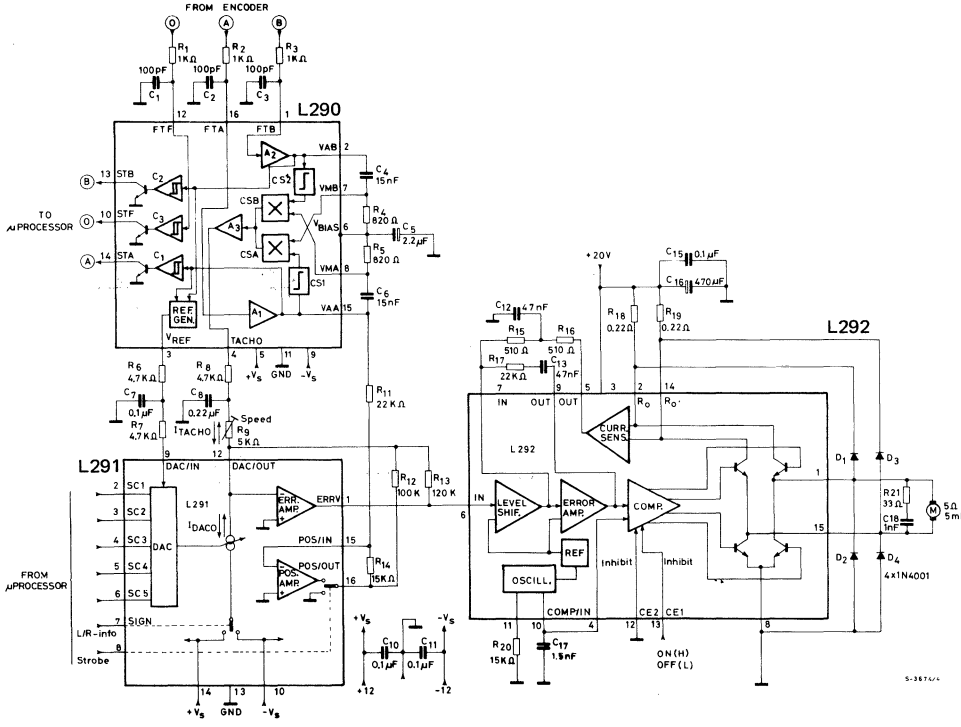


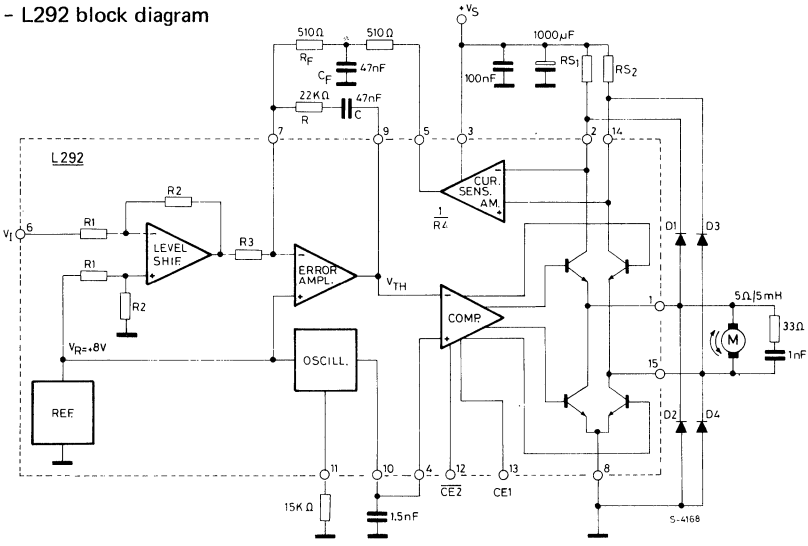
Fig. 4 - Application circuit



APPLICATION INFORMATION

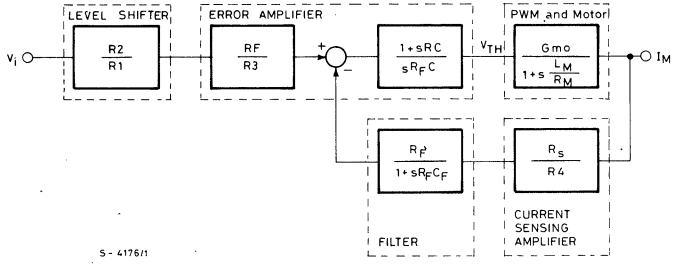
This section has been added in order to help the designer for the best choise of the values of external components.

Fig. 5 - L292 block diagram



The schematic diagram used for the Laplace analysis of the system is shown in fig. 6.

Fig. 6



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 0.005\ \Omega^{-1}$ (current sensing amplifier transconductance)

L_M = Motor inductance

R_M = Motor resistance

I_M = Motor current

$G_{mo} = \frac{I_M}{V_{TH}}\Big|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current (I_M)).

APPLICATION INFORMATION (continued)

Neglecting the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes:

$$G_{mo} = \frac{1}{R_M} \frac{2\,V_s}{V_R} \qquad \text{where: } V_s = \text{supply voltage},\ V_R = 8V \text{ (reference voltage)} \tag{1}$$

DC transfer function

In order to be sure that the current loop is stable the following condition is imposed:

$$1 + sRC = 1 + s\,\frac{L_M}{R_M} \qquad \text{(pole cancellation)} \tag{2}$$

$$\text{from which } RC = \frac{L_M}{R_M} \qquad \text{(Note that in practice R must be greater than 5.6 K}\Omega\text{)}$$

The transfer function is then,

$$\frac{I_M}{V_I}(s) = \frac{R_2\,R_4}{R_1\,R_3} G_{mo}\,\frac{1 + sR_FC_F}{G_{mo}\,R_s + s\,R_4C + s^2\,R_FC_FR_4C} \tag{3}$$

In DC condition, this is reduced to

$$\frac{I_M}{V_I}(o) = \frac{R_2\,R_4}{R_1\,R_3} \cdot \frac{1}{R_s} = \frac{0.044}{R_s}\ \left[\frac{A}{V}\right] \tag{4}$$

Open-loop gain and stability criterion

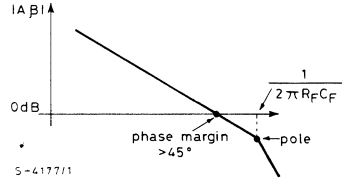
For $RC = L_M/R_M$, the open loop gain is:

$$A\beta = \frac{1}{sR_FC} \cdot G_{mo}\,\frac{R_s}{R_4}\,\frac{R_F}{1 + sR_FC_F} = \frac{G_{mo}\,R_s}{R_4C}\,\frac{1}{s\,(1 + sR_FC_F)} \tag{5}$$

In order to achieve good stability, the phase margin must be greater than 45° when $|A\beta| = 1$.
That means that, at $f_F = \frac{1}{2\pi R_FC_F}$, must be $|A\beta| < 1$ (see fig. 7), that is

$$|A\beta|_{f = \frac{1}{2\pi R_FC_F}} = \frac{G_{mo}\,R_s}{R_4C}\,\frac{R_FC_F}{\sqrt{2}} < 1 \tag{6}$$

Fig. 7 - Open-loop frequency response



APPLICATION INFORMATION (continued)

Closed-loop system step response

a) **Small-signals analysis.**

The transfer function (3) can be written as follows:

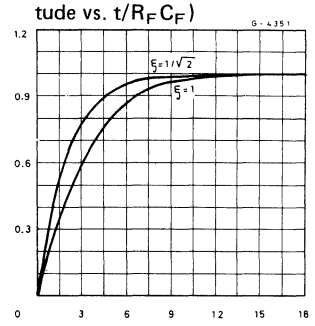
$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_s} \cdot \frac{1 + \frac{s}{2\xi\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \qquad (7)$$

where: $\omega_o = \sqrt{\frac{G_{mo} R_s}{R_4 C R_F C_F}}$ is the cutoff frequency

$\xi = \sqrt{\frac{R_4 C}{4 R_F C_F G_{mo} R_s}}$ is the dumping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal. Examples:

Fig. 8 - Small signal step response (normalized amplitude vs. $t/R_F C_F$)

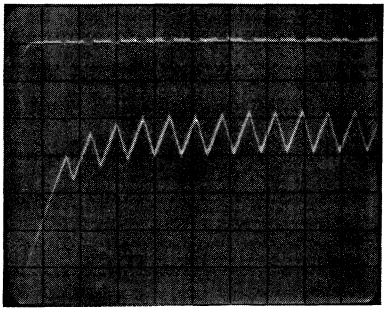


1) $\xi = 1$ from which

$$I_M(t) = \frac{0.044}{R_s}\left[1 - e^{-\frac{t}{2R_F C_F}}\left(1 + \frac{t}{4 R_F C_F}\right)\right] \cdot V_i$$

(where V_i is the amplitude of the input step).

Fig. 9 - Motor current and pin 7 voltage waveforms (application of fig. 5). Small signal response



V_7 = 200mV/div.
I_M = 100mA/div.
t = 100μs/div.
with V_I = 1.5 Vp.

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.044}{R_s}\left(1 - \cos\frac{t}{2R_F C_F} e^{-\frac{t}{2R_F C_F}}\right) V_i$$

From fig. 9, it is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time: the voltage at pin 7 (inverting input of the error amplifier) is locked to the reference voltage V_R, present at the non-inverting input of the same amplifier.
The previous linear analysis is correct for this example.
Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is:

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \qquad \text{(phase margin} = 45°\text{)}$$

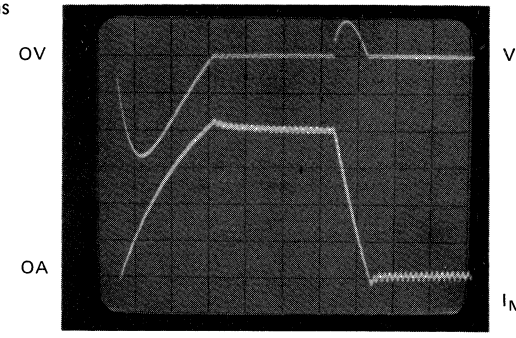
APPLICATION INFORMATION (continued)

b) **Large signal response**

The large step signal response is limited by slew-rate and inductive load.
In this case, during the rise-time of the motor current, the L292 works in open-loop condition, as can be seen from the photograph of fig. 10.

Fig. 10 - Motor current and pin 7 voltage waveforms (application of fig. 5) Large signal response.

V_7 = 1V/div.
I_M = 0.5A/div.
t = 500μs/div.



The voltage at pin 7 (inverting input of the error amplifier) departs from the reference voltage V_R present at the non-inverting input and the feedback loop is open.
The fedback loop is on when the motor current reaches its steady-state value (2A).

Closed loop system bandwidth

A good choice for ξ is the value $1/\sqrt{2}$. In this case:

$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_s} \frac{1 + s R_F C_F}{1 + 2s R_F C_F + 2s^2 R_F^2 C_F^2} \quad (8)$$

The module of the transfer function is:

$$\left|\frac{I_M}{V_I}\right| = \frac{0.044}{R_s} \frac{2\sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2\omega R_F C_F)^2 + 1] \cdot [(1 - 2\omega R_F C_F)^2 + 1]}} \quad (9)$$

The cutoff frequency is derived by the expression (9) by putting $\left|\frac{I_M}{V_I}\right| = 0.707$ (-3 dB), from which:

$$\omega_T = \frac{0.9}{R_F C_F} \qquad f_T = \frac{0.9}{2\pi R_F C_F}$$

APPLICATION INFORMATION (continued)

Example:

a) Data

- Motor characteristics : $L_M = 5$ mH, $R_M = 5\Omega$, $L_M/R_M = 1$ msec
- Voltage and current characteristics: $V_s = 20V$ $I_M = 2A$ $V_I = 9.1V$
- Closed loop bandwidth: 6 KHz.

b) Calculation

- From relationship (4):

$$R_s = \frac{0.044}{I_M} \quad V_I = 0.2\Omega$$

and from (1):

$$G_{mo} = \frac{2\,V_s}{R_M\,V_R} = 1\ \Omega^{-1}$$

- $RC = 1$ msec [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows:

$$\xi^2 = \frac{1}{2} = \frac{200\,C}{4\,R_F C_F \cdot 0.2}$$

- The cutoff frequency is:

$$f_T = \frac{143 \cdot 10^{-3}}{R_F C_F} = 6\ \text{KHz}$$

c) Summarising

- $RC = 1 \cdot 10^{-3}$ sec
- $\frac{500\,C}{R_F C_F} = 1$
- $R_F C_F \cong 24\ \mu$sec

} $C = 47$ nF, $R = 22$ KΩ

For $R_F = 510\ \Omega \rightarrow C_F = 47$ nF.

NOTE - For a more detailed description of the L290-L291-L292 and its applications refer to SGS - TECHNICAL NOTES TN149 and TN150.

PRELIMINARY DATA

PUSH-PULL FOUR CHANNEL DRIVERS

The L293 and the L293E are monolithic integrated high voltage, high current four channel drivers in dual in-line plastic package with 16 leads and 20 leads respectively. They are designed to accept standard DTL or TTL input logic levels and drive inductive loads (such as relays, solenoids, DC and stepping motors) and switching power transistors.
Both are provided of complementary push-pull output stage, two inhibit inputs (which disable two channels each), and an additional supply inputs so that the logic circuitry may run at a lower voltage to reduce power dissipation.
In the L293E the emitters of the lower transistors of each push-pull stage are not internally grounded and the corresponding pins can be used for the connection of an external sensing resistor, making very easy switch-mode current control.
The main features of the L293 and of the L293E are:
- 1A output current capability per channel
- 2A peak output current (non-repetitive) per channel
- Inhibit facility
- Overtemperature protection
- Logical "0" input voltage up to 1.5V (high noise immunity).

The devices are assembled in new packages which have the four central pins connected together and used for heatsinking and grounding.

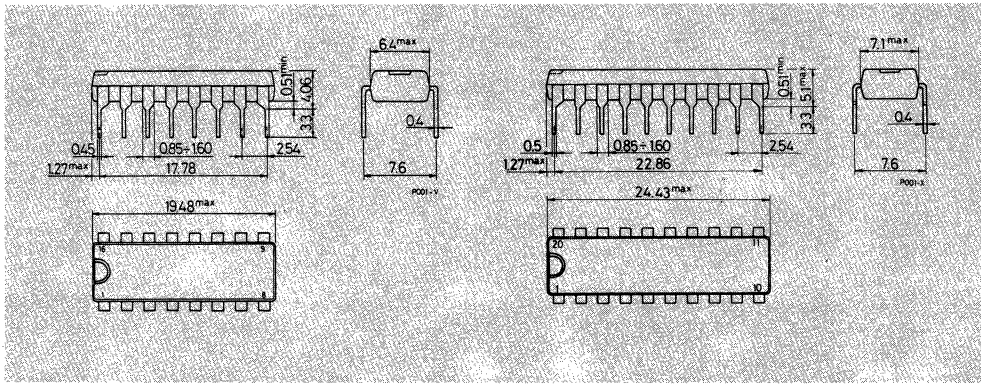
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
V_{ss}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{inh}	Inhibit voltage	7	V
I_{out}	Peak output current (non-repetitive)	2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

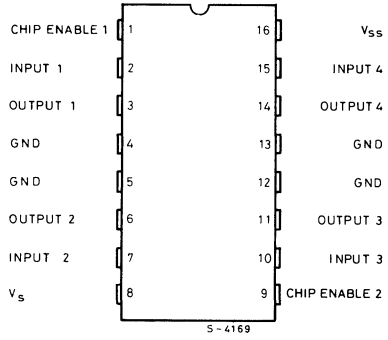
ORDERING NUMBERS: L293B (16 leads)
L293E (20 leads)

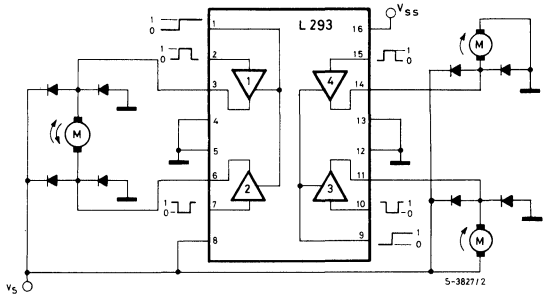
MECHANICAL DATA

Dimensions in mm

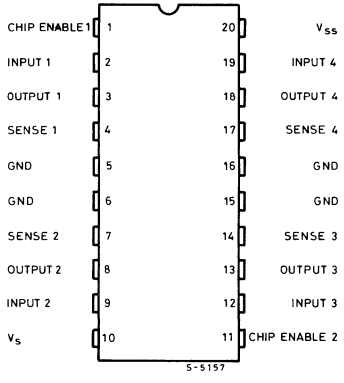


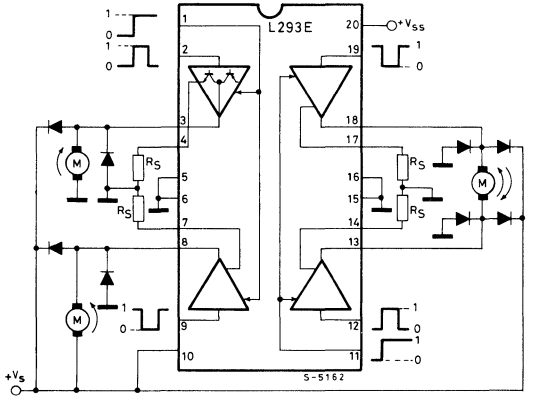
CONNECTION AND BLOCK DIAGRAM (L293)
(top view)



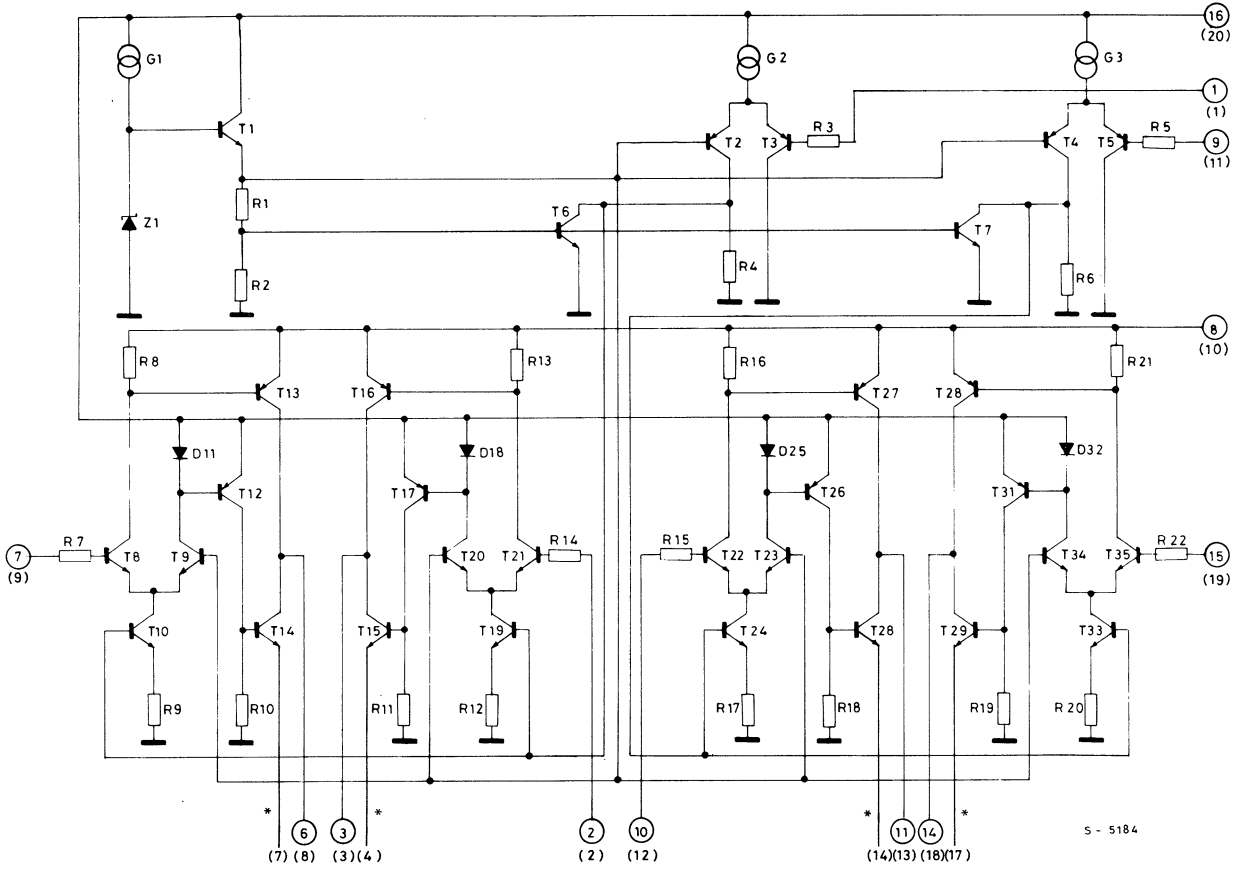


CONNECTION AND BLOCK DIAGRAM (L293E)
(top view)





SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).

○ Pins of L293 ( ) Pins of L293E

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_S= 24V, V_{SS}= 5V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions			Min.	Typ.	Max.	Unit
V_s	Supply voltage						36	V
V_{ss}	Logic supply voltage				4.5		36	V
I_s	Total quiescent supply current	V_i = L	I_o = 0	V_{inh}= H		2	6	mA
		V_i = H	I_o = 0	V_{inh}= H		16	24	
				V_{inh}= L			4	
I_{ss}	Total quiescent logic supply current	V_i = L	I_o = 0	V_{inh}= H		44	60	mA
		V_i = H	I_o = 0	V_{inh}= H		16	22	
				V_{inh}= L		16	24	
V_{iL}	Input low voltage				-0.3		1.5	V
V_{iH}	Input high voltage	$V_{ss} \leqslant 7V$			2.3		V_{ss}	V
		$V_{ss} > 7V$			2.3		7	
I_{iL}	Low voltage input current	V_i = L					-10	μA
I_{iH}	High voltage input current	V_i = H				30	100	μA
V_{inhL}	Inhibit low voltage				-0.3		1.5	V
V_{inhH}	Inhibit high voltage	$V_{ss} \leqslant 7V$			2.3		V_{ss}	V
		$V_{ss} > 7V$			2.3		7	
I_{inhL}	Low voltage inhibit current					-30	-100	μA
I_{inhH}	High voltage inhibit current						± 10	μA
V_{CEsatH}	Source output saturation voltage	I_o = 1A				1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage	I_o = -1A				1.2	1.8	V
V_{SENS}	Sensing Voltage (pins 4, 7, 14, 17) (**)						2	V
t_r	Rise time	0.1 to 0.9 V_o (*)				250		ns
t_f	Fall time	0.9 to 0.1 V_o (*)				250		ns
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o (*)				450		ns
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o (*)				200		ns

(*) See fig. 1.

(**) Referred to L293E.

TRUTH TABLE

V_i (each channel)	V_o	$V_{inh.}$ (°°)
H	H	H
L	L	H
H	X (°)	L
L	X (°)	L

(°) High output impedance.
(°°) Relative to the considerate channel.

Fig. 1 - Switching times

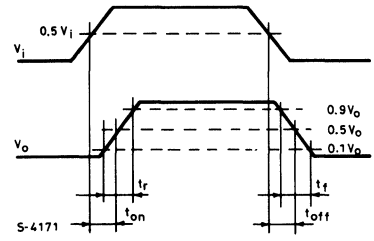


Fig. 2 - Saturation voltage vs. output current

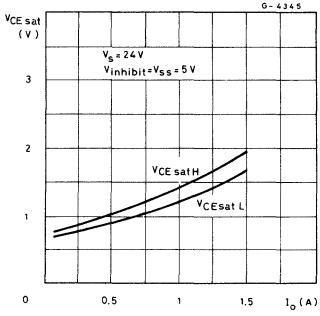


Fig. 3 - Source saturation voltage vs. ambient temperature

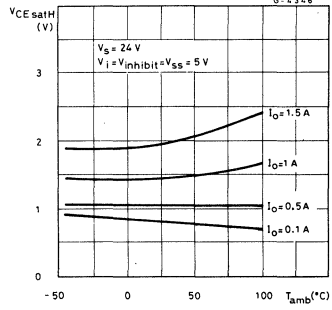


Fig. 4 - Sink saturation voltage vs. ambient temperature

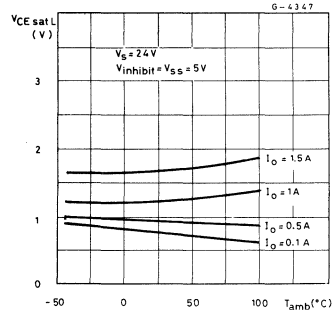


Fig. 5 - Quiescent logic supply current vs. logic supply voltage

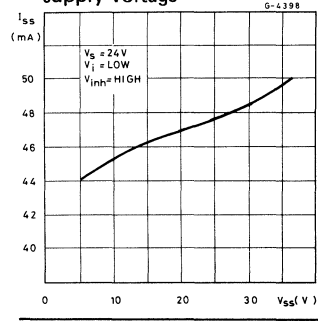


Fig. 6 - Output voltage vs. input voltage

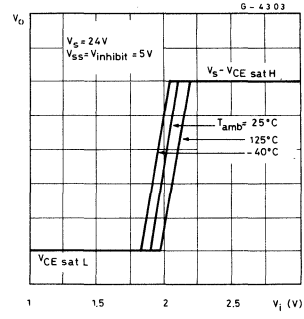
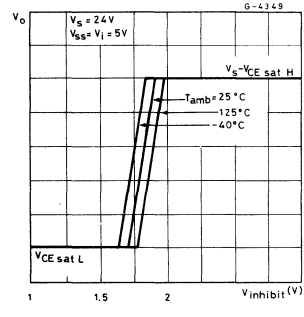
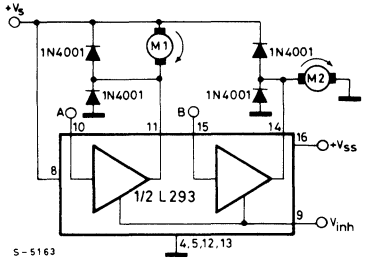


Fig. 7 - Output voltage vs. inhibit voltage



APPLICATION INFORMATION

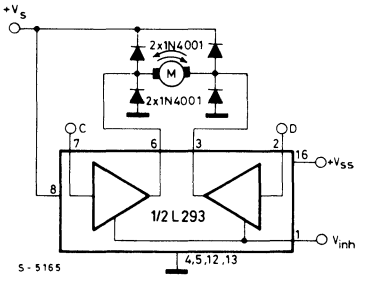
Fig. 8 - DC motor controls (with connection to ground and to the supply voltage)



V_{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

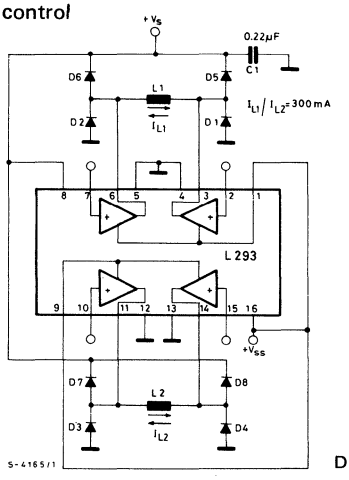
Fig. 9 - Bidirectional DC motor control



INPUTS		FUNCTION
V_{inh}= H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{inh}= L	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

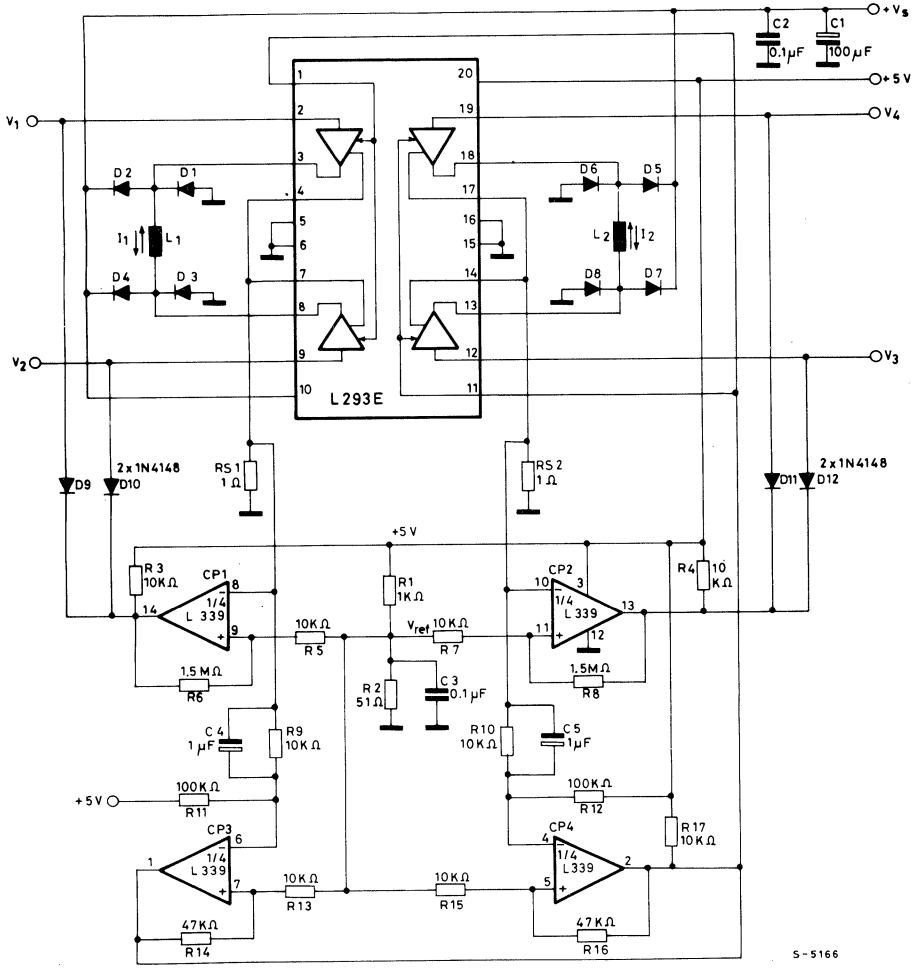
Fig. 10 - Bipolar stepping motor control



D1 - D8 = 1N4001

APPLICATION INFORMATION (continued)

Fig. 11 - Stepping motor driver with phase current control and short circuit protection



D1 ÷ D8 : 0.5A fast diodes (1N4001 or equivalent).

NOTE - For a more detailed description of the L293/L293E and its applications, refer to SGS-TECHNICAL NOTE TN.150.

MOUNTING INSTRUCTIONS

The $R_{thj-amb}$ of the L293 and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.
The diagram of fig. 13 shows the maximum dissipable power P_{tot} and the $R_{thj-amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 μ (see fig. 12). In addition, it is possible to use an external heatsink (see fig. 14).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area which is used as heatsink

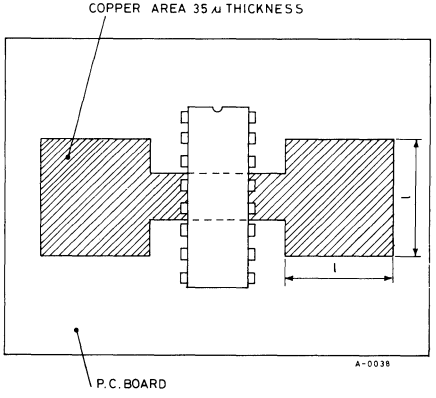


Fig. 13 - Max. dissipable power and junction to ambient thermal resistance vs. size "ℓ"

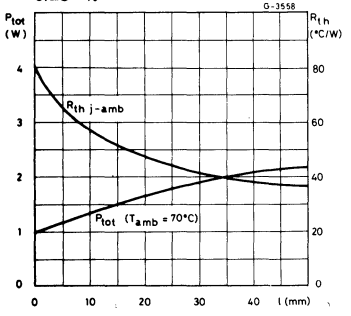


Fig. 14 - External heatsink mounting example (R_{th} = 30 °C/W)

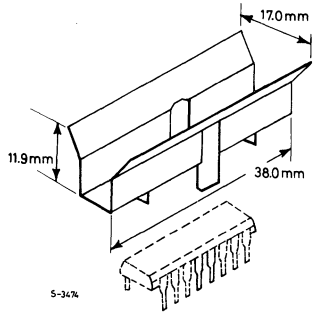
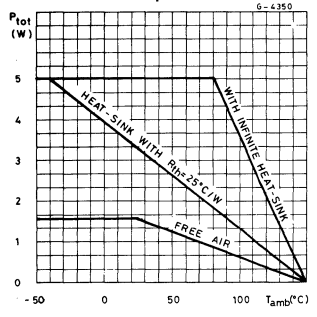


Fig. 15 - Maximum allowable power dissipation vs. ambient temperature



L294

LINEAR INTEGRATED CIRCUIT

SWITCH MODE SOLENOID DRIVER

The L294 is a monolithic integrated circuit in an 11-lead MULTIWATT® package. It is particularly suited for solenoid driving, such as hammers and needles in printers and computer hard-copy peripherals. The switch-mode control of the output current allows electromechanical actuators with high working speed to be driven (switch ON/switch OFF time is very short) and to reduce the power dissipation compared to standard solutions.

Furthermore, the L294 incorporates a diagnostic circuit with latched output which points out any malfunction (for instance electromagnet coil in short circuit).

The L294 main features are:

- high voltage operation (up to 50V)
- high output current capability (up to 4A)
- low saturation voltage
- μP compatible input

It also includes the following protections:

- output short circuit to ground, to supply voltage and across the load
- thermal shut down
- load overdriving protection

ADVANCE DATA

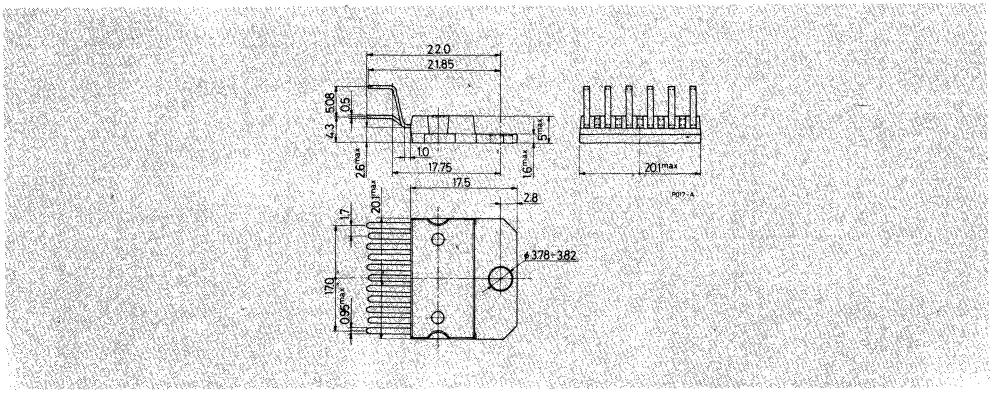
ABSOLUTE MAXIMUM RATING

V_s	Power supply voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_{EN}	Enable voltage	7	V
V_i	Input voltage	7	V
I_p	Peak output current (repetitive)	4.5	A
P_{tot}	Total power dissipation (at T_{case}= 75°C)	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

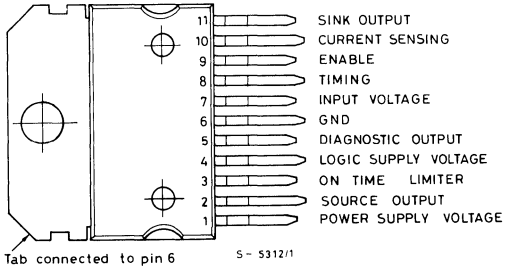
ORDERING NUMBER: L294

MECHANICAL DATA

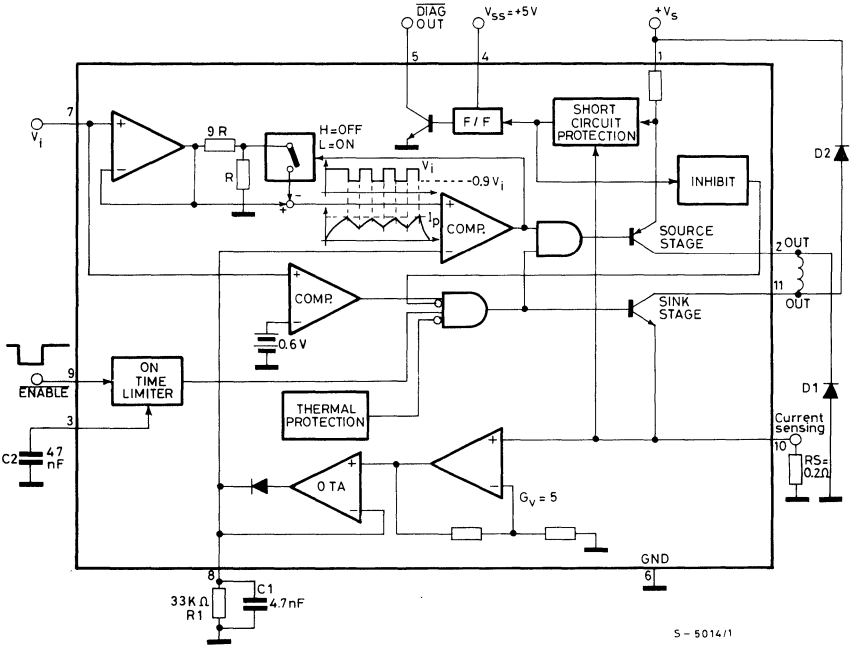
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 40V$, $V_{ss} = 5V$, $T_{amb} = 25°C$, unless otherwise specified).

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Power supply voltage (pin 1)	Operative condition	12		46	V
I_d	Quiescent drain current (pin 1)	$V_{ENABLE} = H$		20	30	mA
		$V_i \geq 0.6V$; $V_{ENABLE} = L$		70		
V_{ss}	Logic supply voltage (pin 4)		4.5		7	V
I_{ss}	Quiescent logic supply current	$V_{DIAG} = L$		5	8	mA
		DIAG output at high impedance		10	100	μA
V_i	Input voltage (pin 7)	Operating output	0.6			V
		Non-operative output			0.45	
I_i	Input current (pin 7)	$V_i \geq 0.6V$		-1		μA
		$V_i \leq 0.45V$		-3		
V_{ENABLE}	Enable input voltage (pin 9)	Low level	-0.3		0.8	V
		High level	2.4			
I_{ENABLE}	Enable input current (pin 9)	$V_{ENABLE} = L$			-100	μA
		$V_{ENABLE} = H$			100	
I_{load}/V_i	Transconductance	$R_s = 0.2\ \Omega$ $V_i = 1V$	0.95	1	1.05	A/V
		$V_i = 4V$	0.97	1	1.03	
$V_{sat\ H}$	Source output saturation voltage	$I_p = 4A$		1.7		V
$V_{sat\ L}$	Sink output saturation voltage	$I_p = 4A$		2		V
$V_{sat\ H} + V_{sat\ L}$	Total saturation voltage	$I_p = 4A$			4.5	V
$I_{leakage}$	Output leakage current	$R_s = 0.2\Omega$; $V_i \leq 0.45V$		1		mA
K	On time limiter constant (°)	$V_{ENABLE} = L$		120		KΩ
V_{DIAG}	Diagnostic output voltage (pin 5)	$I_{DIAG} = 10$ mA			0.4	V
I_{DIAG}	Diagnostic leakage current (pin 5)	$V_{DIAG} = 40V$			10	μA
$\frac{V_{pin\ 8}}{V_{pin\ 10}}$	OP AMP and OTA DC voltage gain (°°)	$V_{pin\ 10} = 100$ to 800 mV		5		
V_{SENS}	Sensing voltage (pin 10) (°°°)				0.9	V

(°) After a time interval $t_{max} = KC_2$, the output stages are disabled.
(°°) See the block diagram.
(°°°) Allowed range of V_{SENS} without the intervention of the short circuit protection.

CIRCUIT OPERATION

The L294 works as a transconductance amplifier: it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see fig. 1).
The following explanation refers to the Block Diagram, to fig. 1 and to the typical application circuit of fig. 3.
The t_{on} time is fixed by the width of the Enable input signal (TTL compatible): it is active low and enables the output stages "source" and "sink". At the end of t_{on}, the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.
The rise time t_r depends on the load characteristics, on V_i and on the supply voltage value (V_s, pin 1). During the t_{on} time, I_{load} is converter into a voltage signal by means of the external sensing resistance R_s connected to pin 10. This signal, amplified by the op amp and converted by the transconductance amplifier OTA, charges the external RC network at pin 8 (R1, C1). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 7).
After t_r, the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i (1/10), allowing hysteresis operation. The current in the load now flows through D1.
Two cases are possible: the time constant of the recirculation phase is higher than R1. C1; the time constant is lower than R1.C1. In the first case, the voltage sensed on the non-inverting input of the comparator is just the value proportional to I_{load}. In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the R1 C1 network.
In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of R1.C1.
In other words, R1.C1 fixes the minimum value of t_1 ($t_1 \geqslant 1/10$ R1.C1. Note that C1 should be chosen in the range 2.7 to 10 nF for stability reasons of the OTA).
After t_1, the comparator switches again: the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).
Now the cycle starts again: t_2, t_4 and t_6 have the same characteristics as t_r, while t_3 and t_5 are similar to t_1. The peak current I_p depends on V_i as shown in the typical transfer function of fig. 2.
It can be seen that for V_i lower than 450 mV the device is not operating.
For V_i greater than 600 mV, the L294 has a transconductance of 1A/V with $R_s = 0.2\Omega$. For V_i included between 450 and 600 mV, the operation is not guaranteed.
The other parts of the device have protection and diagnostic functions. At pin 3 is connected an external capacitor C2, charged at constant current when the Enable is low.
After a time interval equal to K · C2 (K is defined in the table of Electrical Characteristics and has the dimensions of ohms) the output stages are switched off independently by the Input signal.
This avoids the load being driven in conduction for an excessive period of time (overdriving protection). The action of this protection is shown in fig. 1b. Note that the voltage ramp at pin 3 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 3 and to restore the normal conditions, pin 9 must return high.
This protection can be disabled by grounding pin 3.
The thermal protection included in the L294 has a hysteresis.
It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.
Finally, the device is protected against any type of short circuit at the outputs: to ground, to supply and across the load.
When the source stage current is higher than 5A and/or when the pin 10 voltage is higher then 1V (i.e. for a sink current greater than $1V/R_s$) the output stages are switched off and the device is inhibited.
This condition is indicated at the open-collector output DIAG (pin 5); the internal flip-flop F/F changes and forces the output transistor into saturation. The F/F must be supplied independently through V_{ss} (pin 4). The DIAG signal is reset and the output stages are still operative by switching off the supply

CIRCUIT OPERATION (continued)

voltage at pin 1 and then by switching the device on again. After that, two cases are possible: the reason for the "bad operation" is still present and the protection acts again; the reason has been removed and the device starts to work properly.

Fig. 1 - Output current waveforms

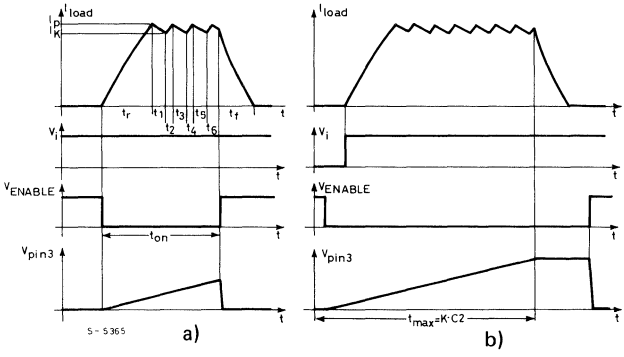


Fig. 2 - Peak output current vs. input voltage

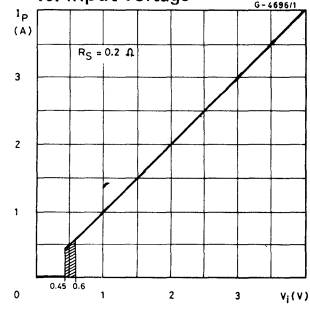


Fig. 3 - Test and typical application circuit

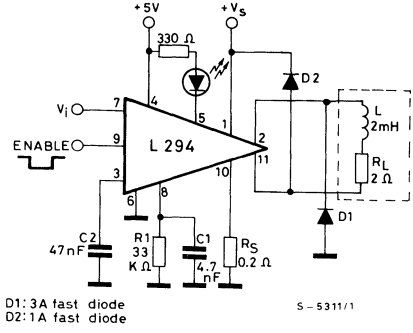


Fig. 4 - Output saturation voltages vs. peak output current

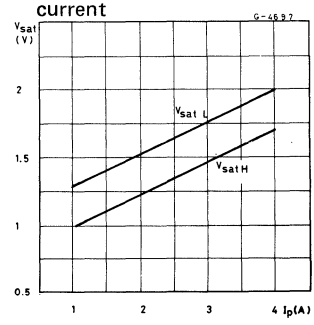


Fig. 5 - Safe operating areas

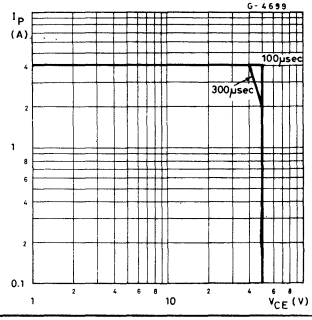
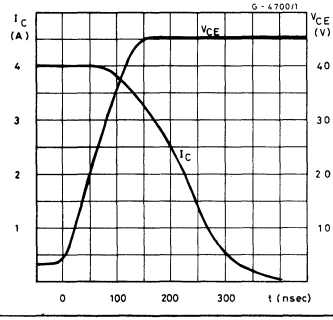


Fig. 6 - Turn-off phase



CALCULATION OF THE SWITCHING TIMES

Referring to the block diagram and to the waveforms of fig. 1, it is possible to calculate the switching times by means of the following relationships.

$$t_r = -\frac{L}{R_L} \ln\left(1 - \frac{R_L}{V1} \cdot I_p\right)$$

where: $V1 = V_s - V_{satL} - V_{satH} - V_{R\ sens}$

$$t_f = -\frac{L}{R_L} \ln \frac{V2}{V2 + R_L \cdot I_o}$$

where: $V2 = V_s + V_{D1} + V_{D2}$

$I_K \leqslant I_o \leqslant I_p$

I_o is the value of the load current at the end of t_{on}.

$$t_1 = t_3 = t_5 = \ldots = \begin{cases} \text{a)} -\dfrac{L}{R_L} \ln \dfrac{0.9\ I_p \cdot R_L + V3}{I_p\ R_L + V3} \\ \text{b)} -R1\ C1 \ln 0.9 \cong \dfrac{1}{10} R1\ C1 \end{cases}$$

where $V3 = V_{satL} + V_{R\,sens} + V_{D1}$

$$t_2 = t_4 = t_6 = \ldots = -\frac{L}{R_L} \ln \left(\frac{V1 - I_p\ R_L}{V1 - I_K\ R_L}\right)$$

Note that the time interval $t_1 = t_3 = t_5 = \ldots$. takes the longer value between case a) and case b). The switching frequency is always:

$$f_{switching} = \frac{1}{t_1 + t_2}$$

In the case a) the main regulation loop is always closed and it forces:

$$I_K = (0.9 \pm S)\ I_p$$

where: $S = 3\%$ @ $V_i = 1V$
$S = 1.5\%$ @ $V_i = 4V$

In the case b), the same loop is open in the recirculation phase and I_K, which is always lower than $0.9\ I_p$, is obtained by means of the following relationship.

$$I_K = I_p\ e^{-\frac{t_1\ R_L}{L}} - \frac{V3}{R_L}\left(1 - e^{-\frac{t_1\ R_L}{L}}\right)$$

With the typical application circuit, in the conditions $V_s = 40V$, $I_p = 4A$, the following switching times result:

$t_r = 255\ \mu s$ $\quad$ $t_f = 174\ \mu s$ @ $I_o = I_p$

$t_1 =$ a) $70\ \mu s$
b) $16\ \mu s$ $\quad$ $t_2 = 29\ \mu s$ $\quad$ $f = 10.2$ KHz

L487

LINEAR INTEGRATED CIRCUIT

VERY LOW DROP 5V VOLTAGE REGULATOR

- PRECISE OUTPUT VOLTAGE (5V ± 2.5%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500 mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- +100/-100V LOAD DUMP PROTECTION
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTIONS
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN

The L487 is a monolithic integrated circuit in Pentawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L487 can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems: a pulse is available (after an externally programmable delay) to reset the microprocessor at power-on phase; at power-off, this pulse becomes low inhibiting the microprocessor.

ADVANCE DATA

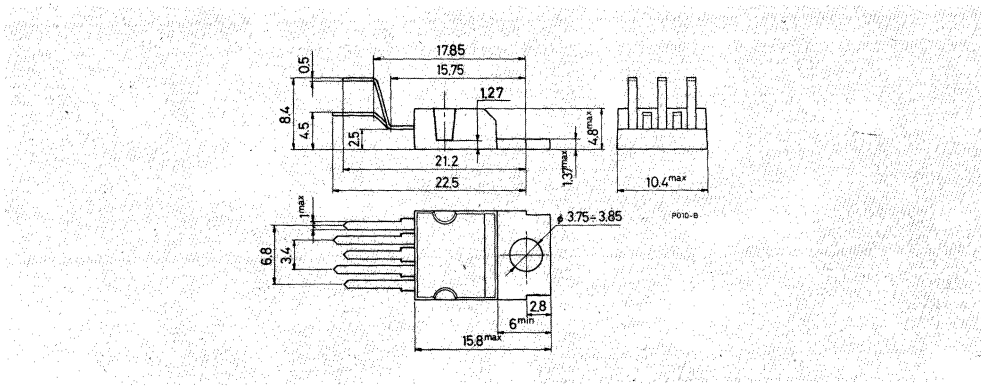
ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	30	V
V_i	Reverse input voltage	-18	V
	Positive transient peak voltage (t = 300 ms)	100	V
	Negative transient peak voltage (t = 100 ms)	-100	V
T_{op}	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

ORDERING NUMBER: L487B

MECHANICAL DATA

Dimensions in mm



LINEAR INTEGRATED CIRCUIT

L296

ADVANCE DATA

HIGH CURRENT SWITCHING REGULATOR

- 5.1V TO 40V OUTPUT
- 4A OUTPUT CURRENT
- UP TO 160W OUTPUT POWER
- PROGRAMMABLE CURRENT LIMITER
- SOFT START
- RESET OUTPUT
- PRECISE (± 2%) ON-CHIP REFERENCE
- VERY FEW COMPONENTS
- SWITCHING FREQUENCY TO 200 kHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- THERMAL SHUTDOWN
- REMOTE INHIBIT AND SYNC INPUT
- CONTROL CIRCUIT FOR CROWBAR SCR

The L296 is a monolithic power switching regulator delivering 4A at a voltage variable from 5.1V to 40V in step down configurations. Features of the device include programmable current limiting, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a synchronisation input for multichip configurations. The L296 is mounted in a 15-lead MULTIWATT plastic power package and requires very few external components. Efficient operation at switching frequencies up to 200 kHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

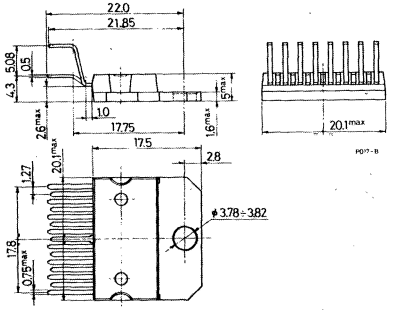
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage	50	V
I_o	Output current	internally limited	
I_R	Reset output current	50	mA
V_R	Reset output voltage	50	V
V_{inh}	Inhibit voltage	15	V
P_d	Power dissipation at $T_{case} < 90°C$	20	W
T_j	Junction temperature range	-25 to +150	°C
T_{stg}	Storage temperature range	-65 to +150	°C

ORDERING NUMBER: L296

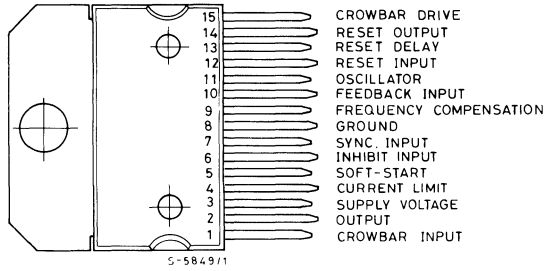
MECHANICAL DATA

Dimensions in mm

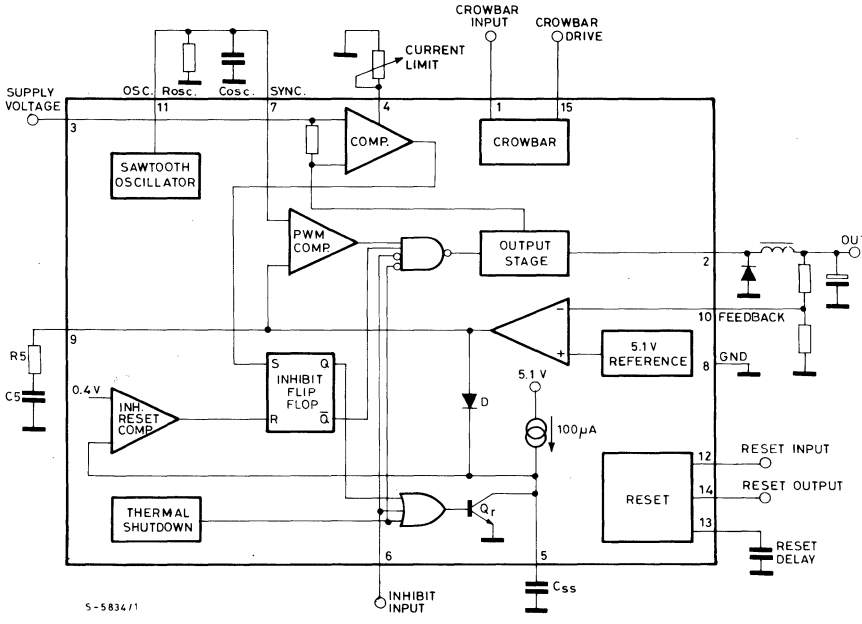


L296

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	CROWBAR INPUT	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator output.
3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	CURRENT LIMITER	A resistor connected between this terminal and ground sets the current limiter threshold (1.5 to 5A). If this terminal is left unconnected the threshold will be 5A.
5	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – level remote inhibit. A logic high level on this input disables the L296.
7	SYNC INPUT	Multiple L296s are synchronised by connecting the sync inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common ground terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to the sync input when the internal oscillator is used.

PIN FUNCTIONS (continued)

N°	NAME	FUNCTION
12	RESET INPUT	This input fixes the threshold of the reset signal generator. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is ON when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION

The L296 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.
The precision and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_s and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

CIRCUIT OPERATION (continued)

A TTL – level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches 150°C and has a hysteresis of 20°C.

Fig. 1 - Reset output waveforms

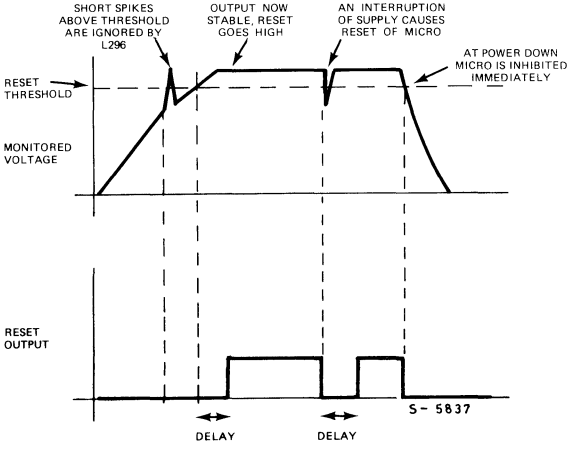


Fig. 2 - Soft start waveforms

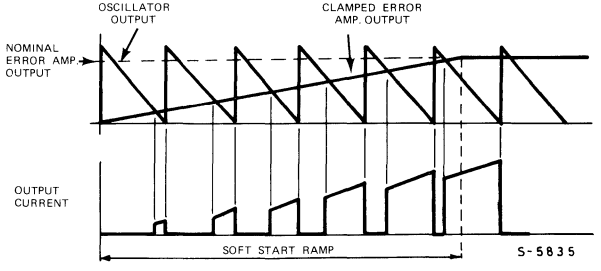
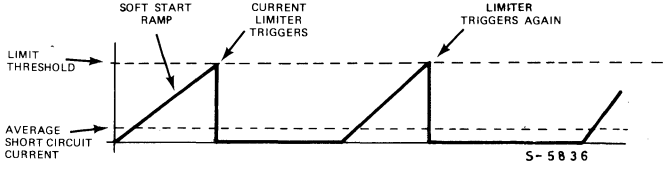


Fig. 3 - Current limiter waveforms



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage range		5.1		40	V
V_i	Supply voltage range		8		50	V
$I_{o\ max}$	Output current		4			A
I_{OL}	Current limit	Pin 4 open		5		A
		R_{lim}= 33 KΩ		2.5		A
V_{sat}	Output transistor saturation voltage	I_o = 4A I_o = 2A		2 1.3		V V
f_s	Switching frequency	R_{osc}= 4.7 KΩ C_{osc}= 2.2 nF		100		kHz
	Efficiency	f = 100 KHz V_i = 35V V_o = 5.1V I_o = 3A V_o = 12V		 75 85		 % %
V_o	Line regulation	V_i = 10 to 40V V_o = 5.1V I_o = 2A		 20		 mV
V_o	Load regulation	V_i = 15V V_o = 5.1V I_o = 2A to 4A I_o = 0.5A to 4A		 10 15		 mV mV
SVR	Supply voltage rejection	f = 100 Hz		60		dB
V_{REF}	Internally reference voltage	V_i = 8 to 50V	5	5.1	5.2	V
V_{REF}	Average temperature coeff. of reference voltage			0.2		mV/°C
t_{ss}	Stoft start time	C_s = 2.2 μF		20		ms
I_{SH}	Output average current with short circuit output			0.5		A
RESET SECTION						
V_{RTi}	Reset threshold voltage (pin 12)	V_i = 8 to 50V	-10%	V_{ref} -100mV	+10%	V
V_{RTo}	Reset out low voltage (pin 14)	I_L = 16 mA			0.2	V
	Delay time (pin 13)	C_{reset} = 2.2 μF		100		ms
CROWBAR SECTION						
	Threshold voltage (pin 12)		+12%	V_{ref} +20%	+23%	
	I source (Pin 15)			100		mA
	I sink (Pin 15)			5		mA
	Delay time			10		μs

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INHIBIT SECTION						
V_{INHL}	Low input voltage				1.2	V
V_{INHH}	High input voltage		2.2			V
I_{INHL}	Input current with low input voltage				100	μA
I_{INHH}	Input current with high input voltage				10	μA
ERROR AMPLIFIER SECTION						
V_{os}	Input offset voltage			2		mV
I_{os}	Input offset current			25		nA
I_b	Input bias current			0.2		μA
G_v	Large signal open loop gain		60			dB
I_{OE}	Out sink current			200		μA
	Out source current			200		μA

Fig. 4 - Test circuit

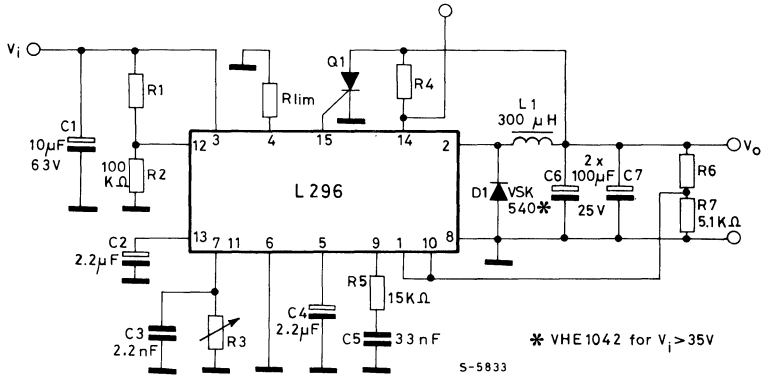
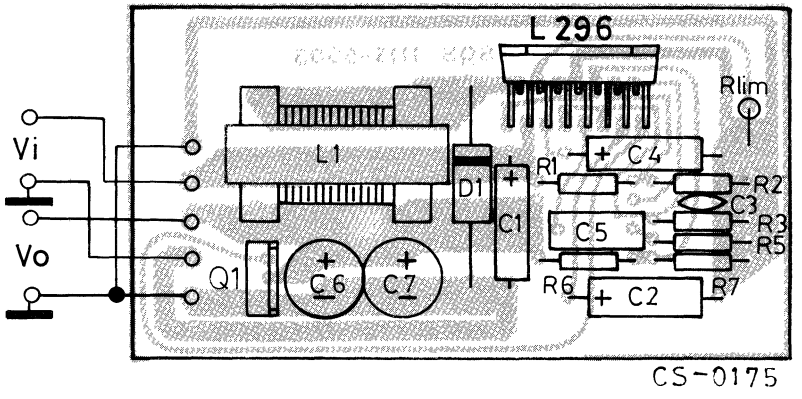


Fig. 5 - P.C. board and component layout of the circuit of fig. 4 (1:1 scale)



SELECTION OF COMPONENT VALUES

Component	Recommended Value	Purpose	Allowed Range Min.	Allowed Range Max.	NOTE
R1 R2	– 100 kΩ	Reset sensing threshold	–	220 kΩ	$R1/R2 = \frac{V_{i\ min.}}{V_T\ (pin\ 12)}$
R3	4.7 kΩ	f_o setting	1 kΩ	100 kΩ	
R4	1 kΩ				$R4_{min} = \frac{V_o}{50\ mA}$
R5	15 kΩ	Frequency compensation	10 kΩ		See application note "Designing with the L296 Power Switching Regulator".
R6 R7	– 51 kΩ	Voltage divider	– –	– 51 kΩ .	$R6/R7 = \frac{V_o - V_{ref}}{V_{ref}}$
C1	10 μF	Stability	1 μF		
C2	2.2 μF	Reset delay	1 μF	4.7 μF	
C3	2.2 nF	f_o setting	1 nF	3.3 nF	
C4	2.2 μF	Soft start	1 μF	4.7 μF	
C5	33 nF	Frequency compensation			See application note "Designing with the L296 Power Switching Regulator".
C6	100 μF	Output filter			
C7	100 μF				
L1	300 μH				

Fig. 6 - Efficiency vs. output current

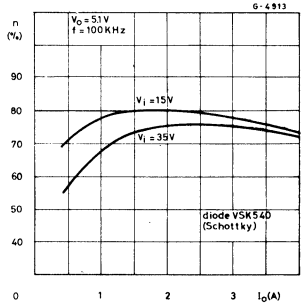


Fig. 7 - Dissipated Power vs. output current (L296 only)

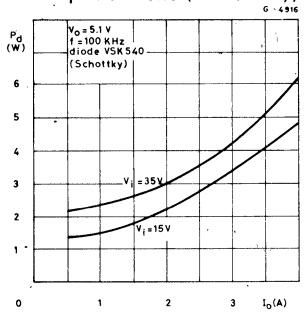


Fig. 8 - Efficiency vs. output current

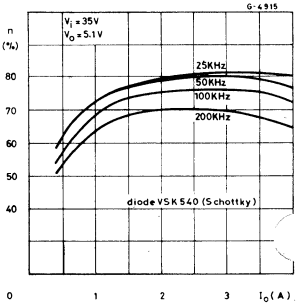


Fig. 9 - Efficiency vs. output voltage

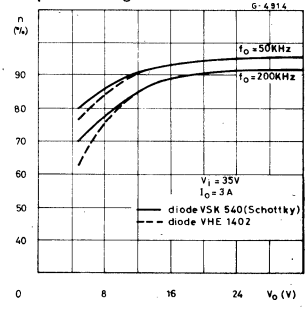


Fig. 10 - Operating frequency vs. R3 and C3

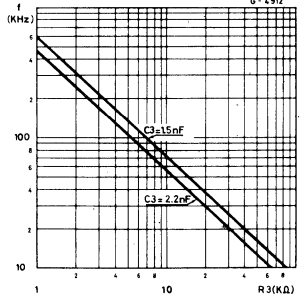


Fig. 11 - Power dissipation derating curve

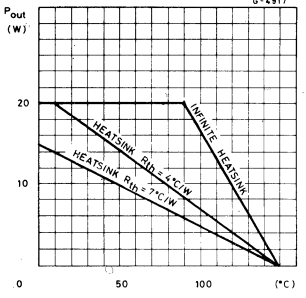


Fig. 12 - Voltage sensing for remote load

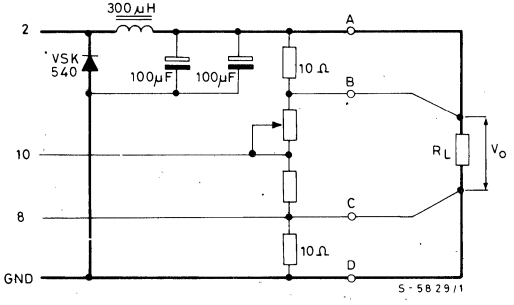
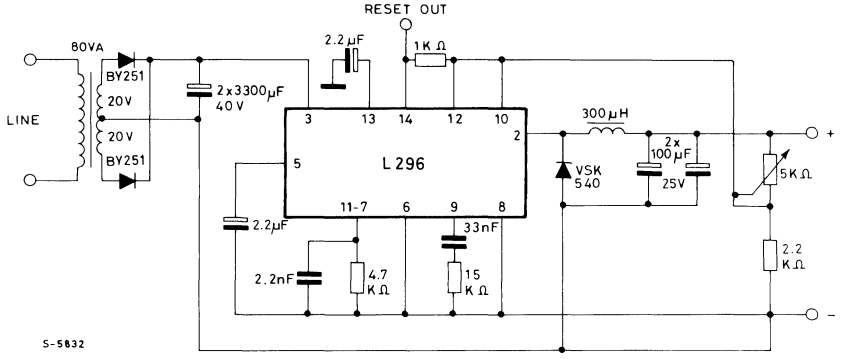


Fig. 13 - Typical application



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100 mA)
ripple $\leqslant$ 20 mV
load regulation (1A to 4A) = 10 mV (V_o = 5.1V)
line regulation (220V ± 15% and to I_o = 3A) = 15 mV (V_o = 5.1V)

Fig. 14 - Preregulator for distributed supplies

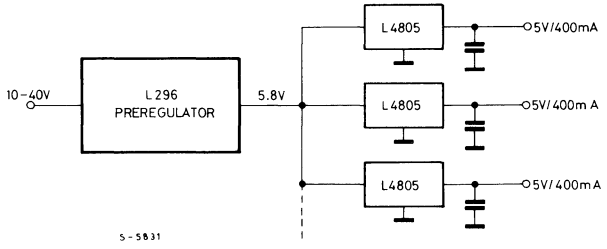
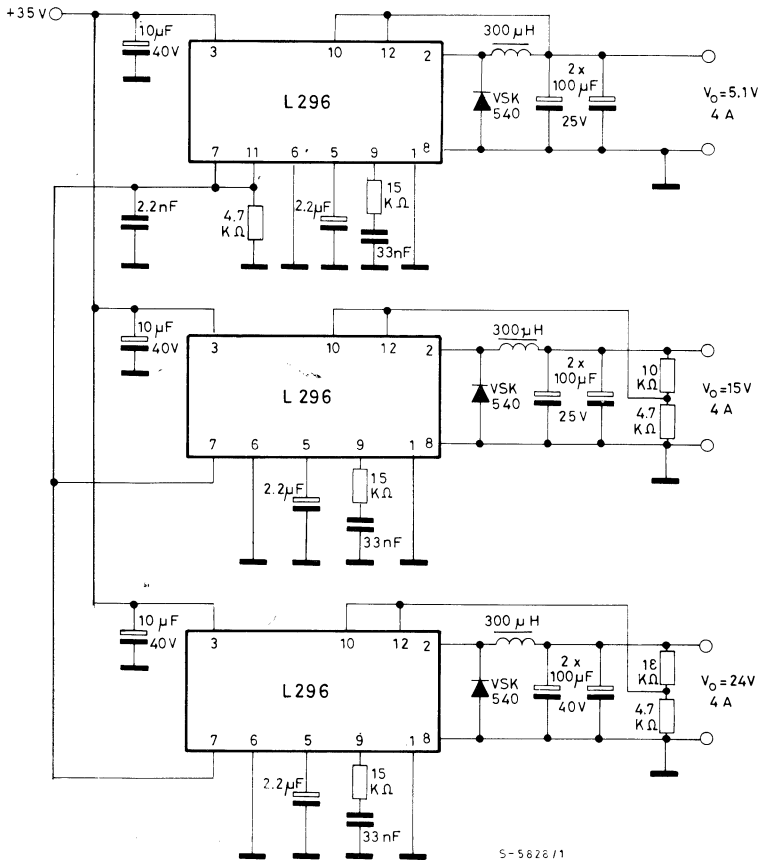


Fig. 15 - Multiple supply



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DESIGNING WITH THE L296 POWER SWITCHING REGULATOR

The L296 Power Switching Regulator is a cost-effective replacement for hybrid switching regulators and can also be used in place of conventional series regulators to improve efficiency. This design guide presents application circuits for the L296 and useful design rules for the choice of support components.

The L296 is a monolithic power switching regulator designed for use in stepdown configurations. It supplies an output current up to 4A and an output voltage variable from 5.1V to 40V. In a single plastic-packaged chip it includes all the regulator control circuitry, a power stage handling 160W and many special features that reduce the cost of external components. These features include soft start, programmable current limiting, remote inhibit, a reset output for microprocessors and an overvoltage protection circuit for use with an external SCR. The device operates efficiently at frequencies to 200 kHz, reducing the size of the output filter components, and a zener-zap trimmed precise reference avoids the need for trimmers in most applications. The L296 is packaged in a 15-lead Multiwatt plastic power package.

Reducing the cost of switchmode supplies, the L296 can replace linear regulators in many applications where switching techniques have been excluded in the past for reasons of cost. It also offers an alternative to more expensive hybrid switching regulators without sacrificing performance.

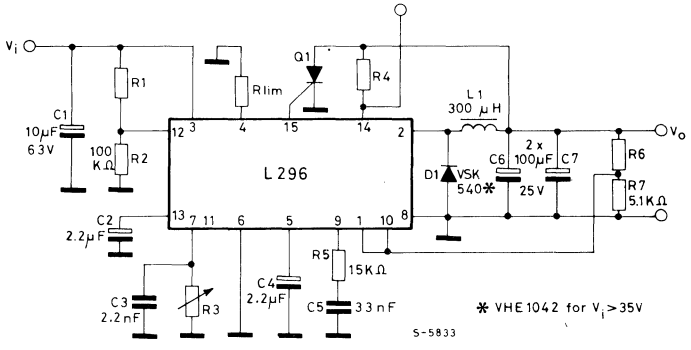
OUTPUT VOLTAGE PROGRAMMING

The output voltage can be varied from 5.1V to 40V and is set by the divider connected between the output and the feedback input (R6 and R7 in figure 1). The divider ratio is given by:

$$\frac{R6}{R7} = \frac{V_o - V_{ref}}{V_{ref}}$$

(V_{ref} is the reference voltage, nominally 5.1V). R7 should not be greater than 51 kΩ or the feedback input leakage current will load the divider. For an output voltage of 5.1V the divider is omitted.

Fig. 1 - Test and evaluation circuit of the L296. All the features are used in this circuit; components can be omitted in many applications.



CURRENT LIMIT SETTING

A resistor connected to pin 4 sets the current limit threshold. If this resistor is omitted, and pin 4 left open circuit, the limit threshold is 5A. The threshold can be varied from 0.5 to 4A. For a threshold of 2.5A the resistor is about 33 kΩ.

THE LC FILTER

The LC filter converts the pulse output of the L296's power stage into a continuous output voltage with a superimposed ripple, ΔV. The inductor determines the voltage ripple on the capacitor.

The ripple ΔI_L is generally chosen to be twice the minimum load current to avoid periods when the transistor and diode are both non-conducting.

The formulae used to calculate LC as a function of ΔI_L and ΔV are:

$$L = \frac{V_o (V_i - V_o)}{V_i \, f \, \Delta I_L}$$

$$C = \frac{V_o \, (V_i - V_o)}{8Lf^2 \, \Delta V}$$

For example, for the test circuit (figure 5) the LC filter was calculated from the following data:

$V_i = 35V$ $\quad V_o = 5V$

$\Delta I_L = 150$ mA $\quad f = 100$ kHz

$\Delta V = 3$ mV

Therefore $L = \frac{5\,(35-5)}{35 \times 100000 \times 150 \times 10^{-3}} \cong 300\ \mu H$

and

$$C = \frac{5\,(35-5)}{8 \times 300 \times 10^{-6} \times (100 \times 10^3)^2 \times 30 \times 10^{-3}} \cong 220\ \mu F$$

In practice the ripple depends on the quality of the filter capacitor. With standard components the ripple will be roughly twice the value implied by this calculation. In this example the actual ripple is about 5 mV.

A multiple capacitor — two or more connected in parallel with a total capacity of C — is recommended. Smaller electrolytics have a lower inductance — important at high frequencies — and handle higher peak currents.

COMPENSATION AND STABILITY

The system is non linear because the output stage operates in switchmode. However, in certain conditions the system can be represented as linear blocks. Delays are introduced by the output stage which can contribute to instability of the system.

When the switching frequency is at least ten times greater than the frequency at which the open loop gain is unity, the system can be approximated to a linear system. The PWM block can then be characterised as a linear block with gain independent of frequency.

Compensating the system with a series RC network on the output of the error amplifier (pin 9), we obtain:

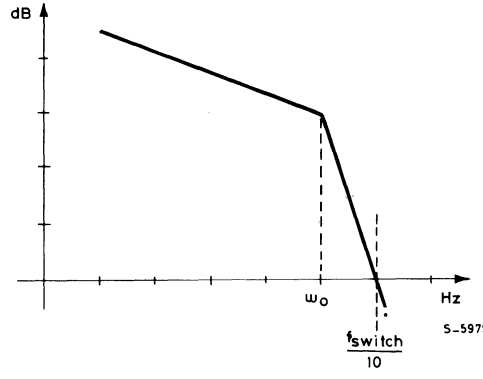
$$Z = \frac{1 + sRC}{sC}$$

Placing the zero introduced by the error amplifier at the resonance frequency of the LC output filter ($\omega_o = 1/\sqrt{LC}$) we obtain the Bode plot shown in figure 2.

The slope when it crosses the frequency axis at 0 dB is roughly 40 dB/decade. In practice the LC filter contains parasitic elements which give a lower slope.

The series resistance of the capacitor (ESR) introduces a zero at high frequencies, guaranteeing stability of the system.

Fig. 2 – Bode plot of regulation loop.



DIODE

The diode should be a fast type to avoid high current peaks in the output transistor. The choice is therefore between Schottky diodes and fast diodes with a Trr of less than 35 ns.

These diodes cost roughly the same. The only significant difference is the lower forward voltage of Schottky diodes. At low output voltages — around 5V — a Schottky diode therefore improves the efficiency of the system.

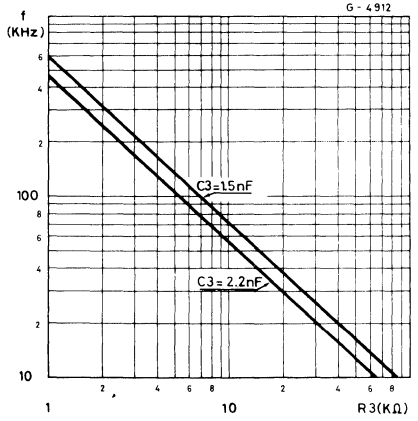
SWITCHING FREQUENCY

The choice of switching frequency depends on the inductor chosen (a smaller inductor can be used at higher frequencies), the power dissipation and desired efficiency. It should not exceed 200 kHz or efficiency will be reduced; the lower limit is set

only by the maximum acceptable dimensions of the output filter.

The chosen frequency is set by the RC network connected to pins 7 and 11 (OSC and SYNC). Suitable values can be found from the nomogram, figure 3. The capacitor must be in the range 1 nF – 3.3 nF and the resistor in the range 1 kΩ to 100 kΩ.

Fig. 3 - Nomogram to find the values of the oscillator components.

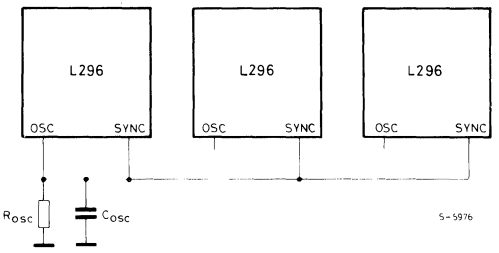


SYNCHRONISATION

When several L296s are used in a multiple supply the switching frequencies should be synchronised to avoid interference propagated on the ground plane.

This is done by connecting the SYNC pins together and omitting the oscillator components on all but the first device. The OSC pins of the subsequent devices are left open, as shown in figure 4.

Fig. 4 - In multiple supplies several L296s can be synchronised as shown here to reduce interference on the ground plane.



LAYOUT

In view of the high currents (5A peak) and fast risetimes involved, care is necessary in the printed circuit layout to avoid problems. In particular, the tracks connecting the L296 output, recirculation diode and LC filter must be short to reduce voltage drop and avoid stray coupling.

It is also important to connect the input filter capacitor, the recirculation diode and output capacitor to the same ground point. A separate ground should be used for the signal processing circuit grounds, connected to the power ground at the negative output terminal.

Figure 5 shows a suitable layout for the test and evaluation circuit of figure 1.

To guarantee good load regulation the two sensing terminals, pin 8 and 10, should be connected directly to the load as shown in figure 6. The two ten ohm resistors shown in this circuit are necessary to ensure that feedback will still be supplied to the L296 even when the sensing wires are disconnected.

Fig. 5 - PC board layout for the test and evaluation circuit of figure 1.

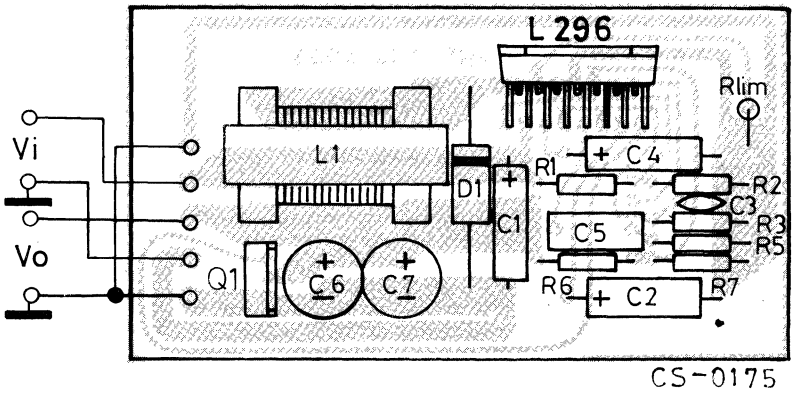
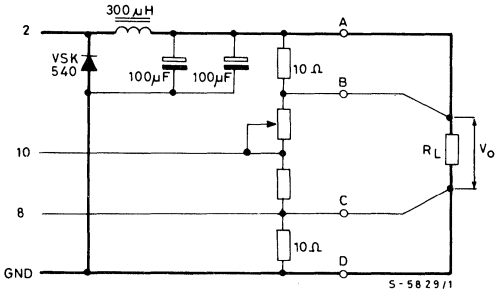


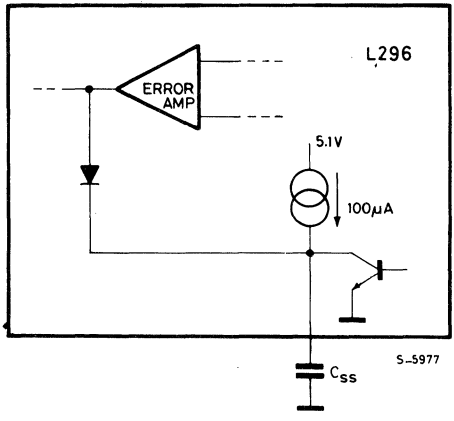
Fig. 6 - When the load is some distance away this four wire connection should be used to ensure good regulation.



SOFT START

The soft start risetime is set by the capacitor on pin 5. This capacitor must be in the range 1 μF to 4.7 μF; The suggested value, 2.2 μF, gives a rise-time of 100 ms; the time for other values is easily calculated bearing in mind that the capacitor is charged by a 100 μA constant current source (figure 7). Note that this capacitor also affects the average current in short circuit conditions.

Fig. 7 - The soft start capacitor clamps the output of the L296's error amplifier and is charged by a 100 μA current source.



RESET CIRCUIT

The reset circuit has three connections: the reset signal output, the sense input and a connection for the capacitor that sets the delay.

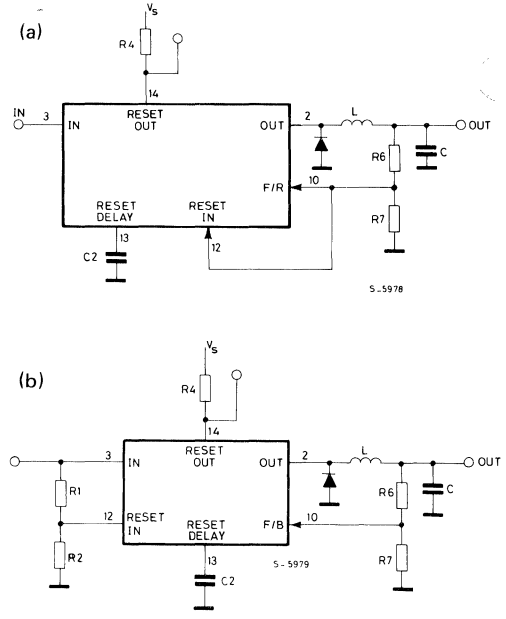
The reset delay capacitor must be in the range 1 μF to 4.7 μF. A delay of about 100 ns given by the recommended value of 2.2 μF.

The sense input, pin 14, may be connected directly to the feedback point (pin 10) or, with a suitable divider, to the unregulated input (figure 8).
The internal threshold of the reset circuit is V_{ref} - - 100 mV (roughly 5V). Therefore the divider for the second case is found from:

$$\frac{R1}{R2} = \frac{V_{i\,min}}{V_{ref} - 100\ mV}$$

R2 should not exceed 200 kΩ.
The reset output is open collector and the maximum allowed collector current is 50 mA.

Fig. 8 - The reset circuit's sense input can be connected to the feedback point (a) or to the input via a divider (b).



INHIBIT INPUT

The inhibit input, pin 6, is TTL, NMOS and CMOS-compatible. It disables the L296 when high and must be connected to ground if not used. When the inhibit signal goes from high to low the circuit restarts softly.

CROWBAR PROTECTION

The crowbar overvoltage protection block has tw connections: a voltage sense input and an SCR gate drive output. The SCR is triggered when the voltage on the sense input exceeds the voltage reference by about 20%, i.e. the voltage sense input has a threshold of about 6V.

Normally the sense input is connected directly to the feedback point, pin 10. It can, however, be

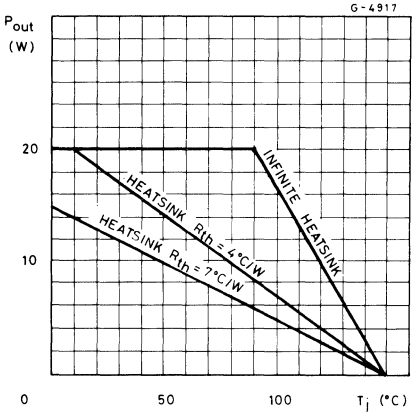
used to monitor the input voltage, adding a suitable voltage divider to set the threshold.

The gate drive output supplies up to 100 mA and connects directly to the gate of the SCR. The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.

HEATSINK

The choice of heatsink depends on the power dissipated in the device and the desired operating junction temperature. Figure 9 shows the power dissipation derating curves for typical heatsinks.

Fig. 9 - Derating curve for package power dissipation.



Silicone grease is often used to improve the contact thermal resistance. The grease should not be too thick or viscous – the thermal resistance may be worsened or the tab deformed.

Care should also be taken when mounting the device on the heatsink. To avoid deforming the tab, which can affect reliability, the mounting screw should be tightened to roughly 8 kg/cm and the heatsink surface should have a planarity no worse than 20 μm. A washer on the screw helps spread the load on the tab and minimize distortion.

RFI/EMI SUPPRESSION

Electromagnetic interference generated by a high current switching regulator can affect sensitive circuitry. Metal shielding of the regulator is the simple solution. Since the L296 circuit is very compact the board can be housed in the L296's heatsink.

EFFICIENCY

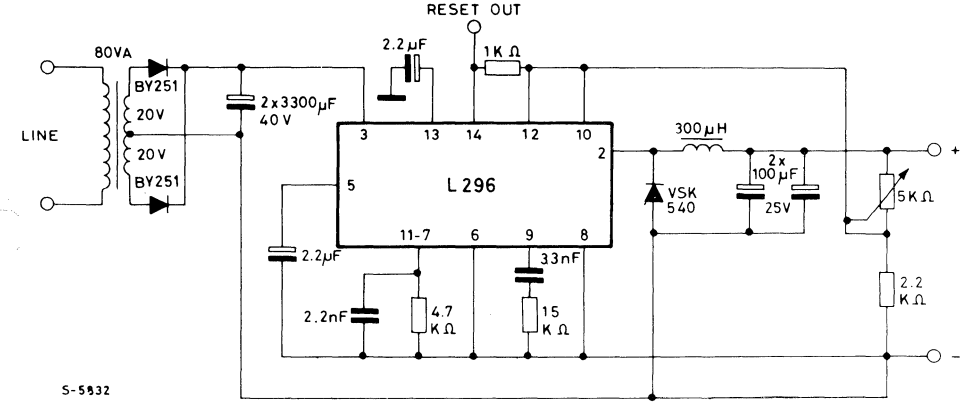
The efficiency of a complete regulator depends on many factors including the switching frequency, the recirculation diode, the input/output differential, and the output current.

In applications where very high efficiency is required, a lower switching frequency must be chosen. Efficiency is also improved by choosing an input voltage not too high.

APPLICATION CIRCUITS

Figure 10 shows a complete 5.1V - 15V/4A regulator. This circuit gives a ripple lower than 20 mV, load regulation (about 3A) of 10 mV and line regulation of 15 mV (at 220V ± 15% in; 3A out). The crowbar protection is not used in this circuit. Note in particular the ground connections.

Fig. 10 - A complete 5.1-15V/4A supply.



A multiple supply, 5.1V/15V/24V, is shown in figure 11. This example shows how several L296s can be synchronised and indicates suitable values for the voltage programming divider.

Figure 12 shows a minimal 5.1V fixed regulator circuit. Using the 5A current limit default and omitting the crowbar gives an extremely low component count. Soft start still operates and the reset circuit can be used if a suitable collector load is connected to the reset output.

The L296 is also useful as a preregulator in distributed supply systems (figure 13). With very low drop linear regulators on each card the overall efficiency of sych a system is very high. Recommended types are the L4800 series very low drop regulators or L7800 series standard regulators.

Fig. 11 - A 5.1V/15V/24V multiple supply. Note the synchonisation of the three L296s.

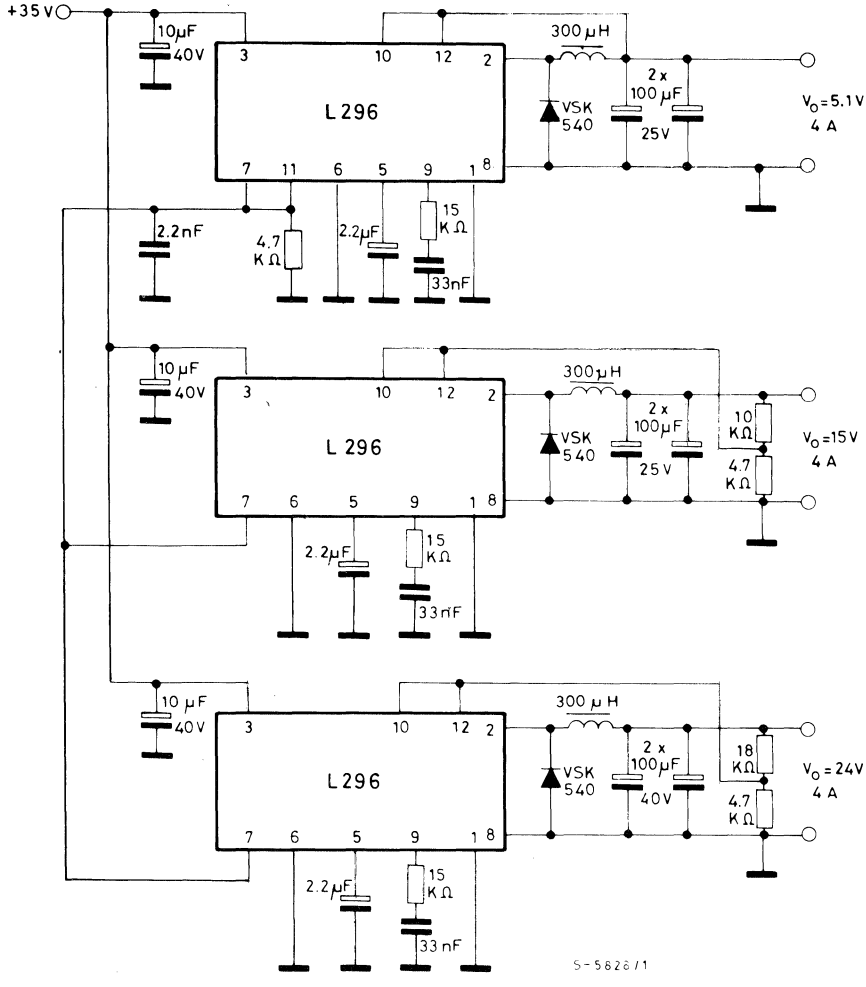


Fig. 12 - A minimal 5.1V fixed regulator. Very few components are required.

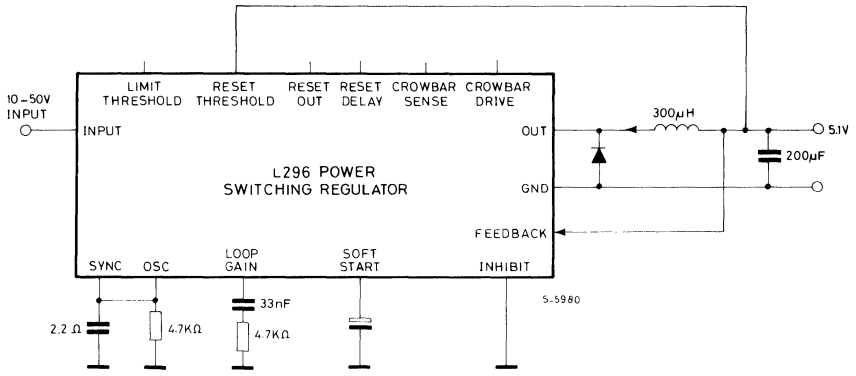
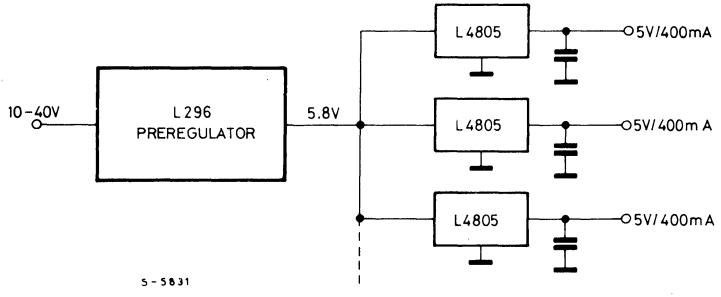


Fig. 13 - The L296 is also useful as a preregulator in distributed supply systems. Using low drop series regulators as shown in here, the overall efficiency is very high.



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INTRODUCING THE L296: THE WORLD'S FIRST MONOLITHIC POWER SWITCHING REGULATOR

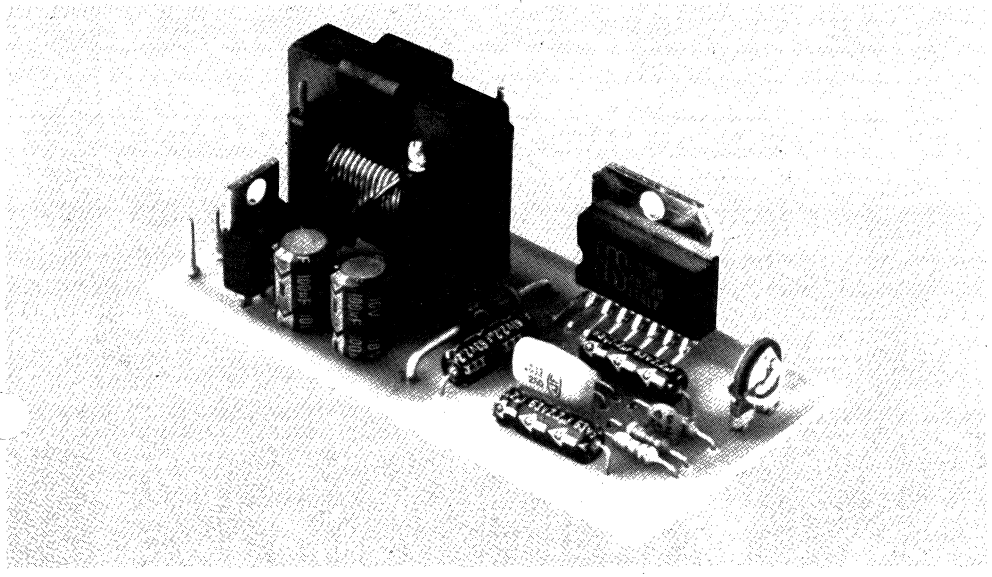
Supplying 4A at 5.1V to 40V, the L296 power switching regulator challenges both costly hybrid switching regulators and the much less efficient high current linear regulators. This article explains how the device operates and highlights its advantages.

The key advantage of a switchmode regulator is high efficiency. In practical terms this means that very little power is dissipated in the supply so less power is consumed, a smaller transformer can be used, the supply is more compact and there is less heat to be dissipated. With all these benefits it's not surprising that more and more designers are turning to switchmode supplies – even for applications traditionally the realm of linear regulators.

But up to now high current switching regulators have always been realized with discrete components, an IC controller with external power transistors or hybrids – all of which are expensive solutions.

The L296 offers a new alternative: a high power **monolithic** switching regulator. Combining a new ion-implanted bipolar process with power package know-how, SGS has packed a full-feature 4A/

Fig. 1 – With a few external components the L296 forms a very compact 4A/5.1–40V switching regulator. Many of the components shown here may be omitted.



5.1-40V switching regulator onto a single chip. Further, since this chip is mounted in a Multiwatt® plastic package the cost-per watt is very low.

Complementing the low cost of the device, the L296 is designed to minimize the cost of external component support. This has been achieved in a number of ways. Firstly, the device is capable of operating at switching frequencies up to 200 kHz without sacrificing efficiency. Consequently, the output filter components — an inductor and a capacitor — can be very small and relatively expensive. Second, as much as possible has been integrated — all the standard power supply features are included on the chip and it even incorporates the load current sense resistor. Third, a high precision zener-zap trimmed voltage reference eliminates the need for a trimmer in most applications. Finally, all the extra features are designed so that components can be omitted if the feature is not required.

These features include soft start, programmable current limiting, thermal shutdown, remote inhibit, a reset output for microprocessors and a voltage sense/SCR driver circuit for crowbar overvoltage protection with an external SCR.

The soft start circuit slows down the risetime of the output voltage when power is applied. It thus eliminates power-on transients which can damage sensitive components. An external capacitor sets the risetime so that it can be tailored to suit specific requirements.

Output current limiting protects the device from short circuits of the load and, since the limit threshold is adjustable, can be used to protect the load itself. The limit threshold can be varied from 0.5A to 5A with an external resistor. If this resistor is omitted the L296 assumes a limit of 5A, thus protecting itself.

Intended for microprocessor systems, the reset circuit provides a logic signal when the output voltage is above a preset threshold. The threshold can be adjusted externally and the reset signal is delayed to prevent false starts. Coupled to the reset input of a micro, the signal inhibits operation whenever the supply is unsafe.

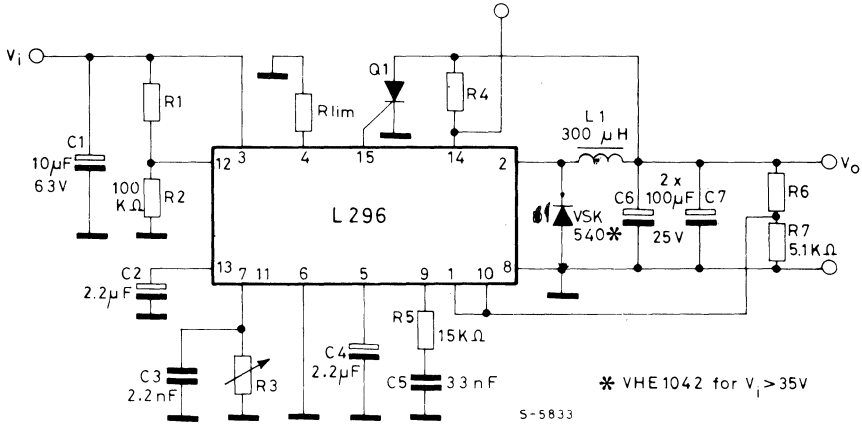
The overvoltage protection circuit is of the crowbar type and operates with an external SCR connected across the output. It provides direct gate drive for the SCR and has an external voltage sense input so that either the input voltage or output voltage can be monitored.

The L296 is also protected by a thermal shutdown circuit which disables the output stage when the junction temperature exceeds 150°C. Normal operation is restored when the temperature falls below 130°C.

TYPICAL CIRCUITS

Figure 2 shows a regulator that uses all the features of the L296. Even in this example few external components are needed. This circuit delivers up to 4A at a voltage set by the divider in the feedback loop. The current limit is adjusted by a resistor and the reset delay is set by a capacitor. Additionally, the reset threshold can be adjusted. The small size of this regulator can be judged from the photograph, figure 1.

Fig. 2 - This application circuit uses all the features of the L296.



Taking away all the optional components gives the even simpler configuration of figure 3. This circuit provides 4A at 5.1V, soft start, thermal shutdown and current limiting with the default 5A threshold.

The L296 is also ideal for use as a preregulator in distributed supply systems. Combined with low drop series regulators such as the L4800 series, an L296 gives extremely high efficiency plus very good regulation (figure 4).

Fig. 3 - Many components can be omitted as shown here. This is a 4A/5.1V supply.

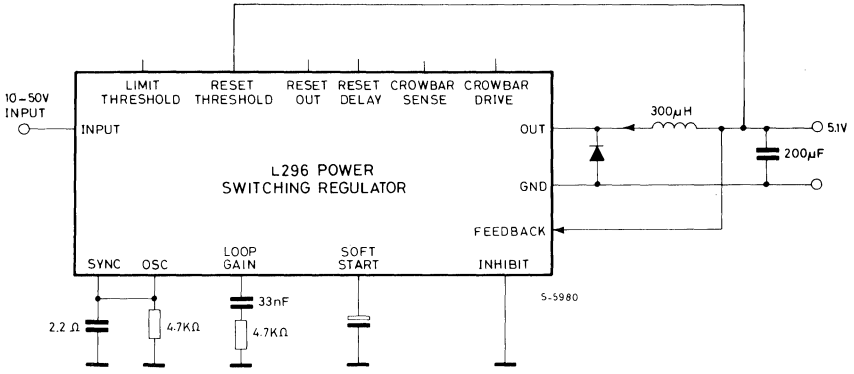
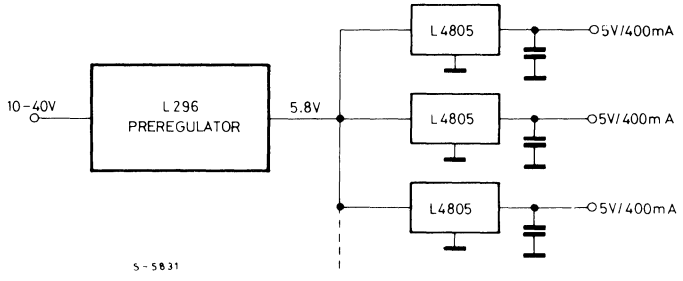


Fig. 4 - The L296 is ideal for use as a preregulator in distributed supply systems. Efficiency is very high and regulation is excellent.



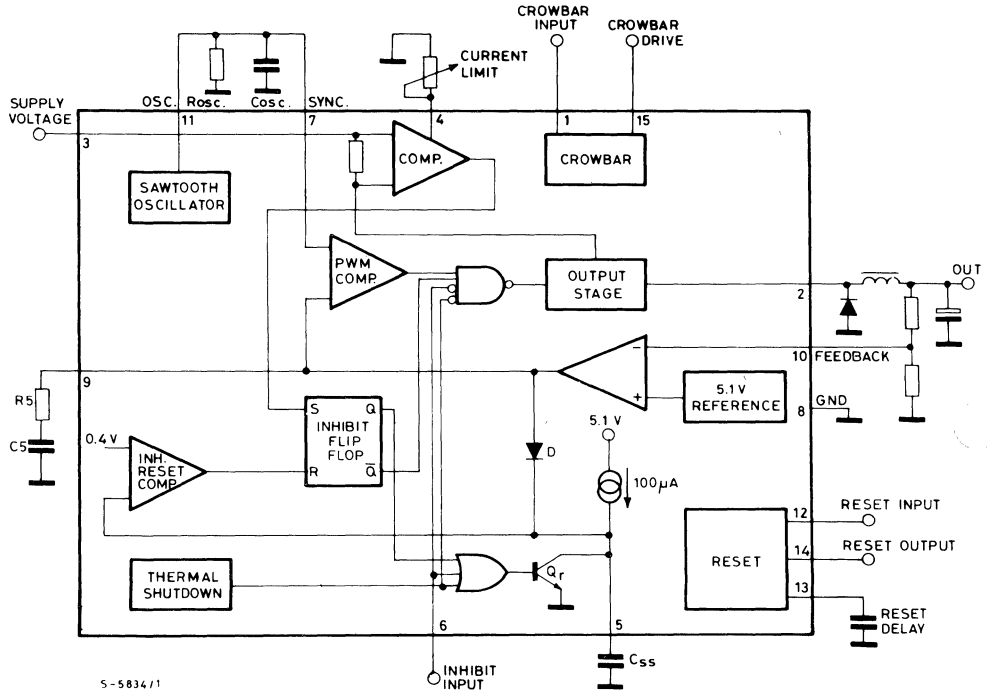
LOOKING INSIDE

Looking at the simplified block diagram, figure 5, the main regulation loop can be identified quite easily; it consists of a 5.1V reference, loop error amplifier, PWM modulator (sawtooth oscillator ...s comparator), power stage and an external LC ...er.

Voltage feedback from the output is compared with the 5.1V reference in the error amplifier. The output of this amplifier sets the threshold of the PWM comparator and thus controls the duty cycle of the switching pulses. These pulses drive the output stage, producing the desired output voltage with the help of the LC filter. If the output is connected to the feedback point directly the regulated output voltage is 5.1V; a divider is added to the feedback loop to produce higher voltages. The loop gain characteristics can be adjusted by the external RC network, RgCg, to give the required stability, ripple rejection at twice the mains frequency and immunity against supply and load variations.

The output of the oscillator is not connected internally to the PWM comparator. This is done deliberately so that several L296s can be synchronised, avoiding interference and switching noise on the ground plane in multiple supplies. The SYNC pins of all the devices to be synchronised are connected together and only one is equipped with the oscillator components, as shown in figure 6.

Fig. 5 - Simplified block diagram of the L296.



SWITCHING vs LINEAR

How much do you gain?

It's a well known fact that switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain? We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4A/5V supply.

Linear

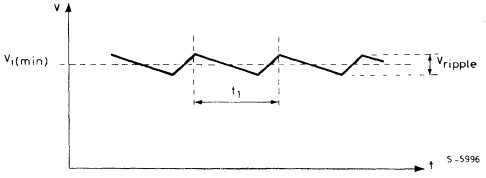
For a good linear regulator the minimum dropout will be at least 4V at 4A. The minimum input voltage is given by:

$$V_{i\,min} = V_O + V_{DROP} + \tfrac{1}{2} V_{ripple}$$

where $V_{ripple} \cong \dfrac{I_O\, T1}{C} = \dfrac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2V$

(a good approximation is 8 ms for t_i (at mains frequency of 50 Hz) and 1000 µF for C, the filter capacitor after the bridge).

Therefore $V_{i\,min} \cong 10.6V$



Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be:

$$V_{nom} = \frac{V_{i\,min}}{0.8} = \frac{10.6}{0.8} = 13.25V$$

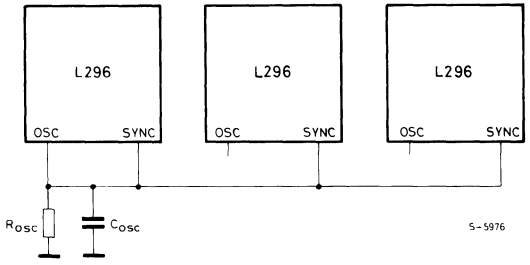
To allow even a small margin we have to choose:

$$V_{nom} = 14V$$

The power that the series element must dissipate is therefore:

$$P_d = (V_{nom} - V_O)\, I_O = 36W$$

Fig. 6 – Several L296s can be synchronised easily to avoid switching noise and save components.

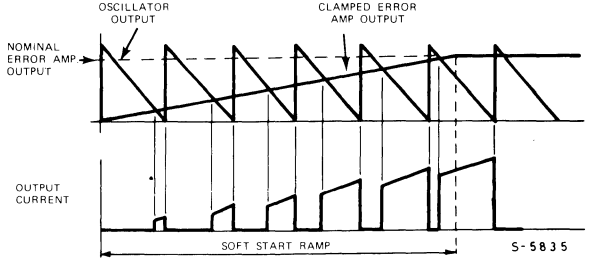


SOFT START AND CURRENT LIMITING

The soft start is produced by the diode, D, an external capacitor, C_{SS}, and a constant current source.

When power is applied, after an inhibit, or after a current limit, the voltage across C_{SS} is zero, clamping the error amplifier output to zero via the diode D. The capacitor is charged by the constant current generator, thereby allowing the error amplifier output – and hence the output voltage – to rise (figure 7).

Fig. 7 – Waveforms showing the soft start.



and the transformer must supply a power of:

$$P_{diss} = 14x4 = 56W$$

It must therefore be dimensioned for:

$$P_D = \frac{56}{0.9} = 62\ VA$$

and a heatsink will be necessary with a thermal resistance of:

$$R_{th\ heats.} = 0.8°\ C/W$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30 VA and the heatsink thermal resistance about 11° C/W.

	Linear	Switching
Transformer	*62 VA*	*30 VA*
Heatsink	*0.8° C/W*	*11° C/W*

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active & passive components is roughly the same for both types.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

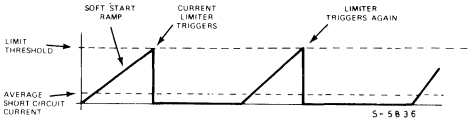
Current limiting is more complex and involves two comparators, a flip flop, an AND gate, an OR gate and the transistor Q_r. A comparator compares the output current, sensed by an on-chip metal resistor, with the limit threshold preset by an external resistor.

As soon as the current tops the threshold, this comparator switches, setting the flip flop which disables the output stage and shorts the soft start capacitor via Q_r.

A second comparator resets the flip flop when the voltage across C_{SS} has fallen below 0.4V, re-enabling the output stage. With the usual slow ramp, the output current rises again and if the cause of the excess current is still present the whole process is repeated.

This cycle continues until the fault condition is removed (figure 8). Thanks to the dead time and the soft start ramp the average current in this condition is not high enough to damage the device.

Fig. 8 - Waveforms illustrating the action of the current limiter.



ION-IMPLANTED ISOLATION

The L296 is one of the first products to exploit an advanced bipolar process which allows the combination of fast-switching high power devices and dense control circuitry on the same chip. One of the key features of this process is the use of a two-step ion-implantation technique to form the isolation wells.

Normally this isolation is created by diffusing p-type impurities from above. The result is a bowl-like cross section which wastes silicon area (figure 9). Moreover, since prolonged high temperature processing is needed to perform this diffusion, the n+ buried layer spreads, reducing the breakdown voltage.

In the new process a heavy p+ implant is made before the n- epitaxial collector growth, followed by a further implant from above. When the wafer is heated both implants diffuse, joining in the middle to create a narrow but deep isolation well (figure 10). Since high temperature processing is much reduced the n+ buried layer spreads very little and the resulting NPN transistor has a breakdown voltage in excess of 50V.
The narrower isolation results in an increased density, with minimal geometry transistors reduced to a compact 18 mil^2. Speed is correspondingly increased.

Teamed with the Multiwatt plastic package, this process allows the integration of complex devices handling in excess of 200W. Other devices already introduced include the L295 dual solenoid driver (220W), the L294 switchmode driver (180 W) and the L298 dual bridge driver (200 W).

Fig. 9 - Diffusing the isolation from above gives the familiar bowl-shaped cross section which wastes spaces.

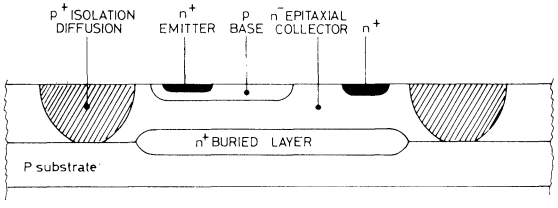
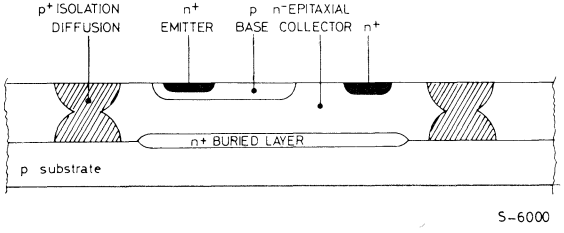


Fig. 10 - The above/below two-step implanted isolation is more compact and results in an increased n- thickness between base and buried layer. raising the breakdown voltage.



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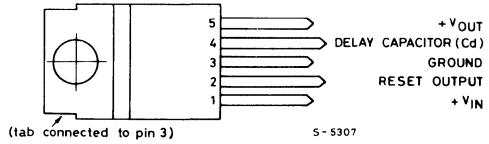
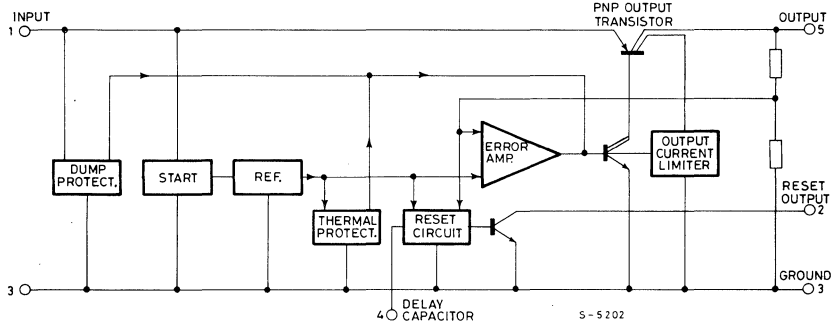
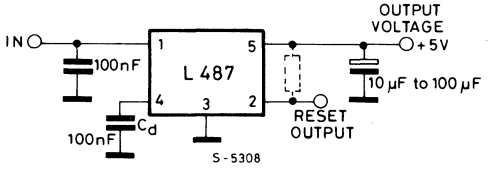
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST CIRCUIT



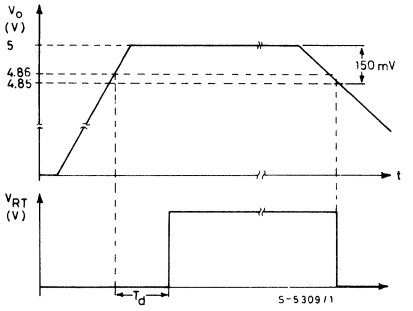
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max 3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_i = 14.4V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 5 mA to 500 mA	4.80	5	5.20	V
V_i	Operating input voltage				28	V
ΔV_o	Line regulation	V_i = 6 to 26V I_o = 5 mA		5		mV
ΔV_o	Load regulation	I_o = 5 to 500 mA		15		mV
V_i-V_o	Dropout voltage	I_o = 500 mA		0.6		V
I_d	Quiescent current	I_o = 0 mA I_o = 150 mA I_o = 500 mA		5 20 100		mA
$\frac{\Delta V_o}{\Delta T}$	Temperature output voltage drift			0.5		mV/°C
SVR	Supply voltage rejection	I_o = 350 mA f = 120 Hz C_o = 10 μF V_i = 12V ± 5 Vpp		60		dB
I_{sc}	Output short circuit current			0.8		A
V_R	Reset output voltage	I_R= 16 mA $V_o \leqslant$ 4.75V			0.8	V
I_R	Reset output leakage current	V_o in regulation			50	μA
t_d	Delay time for reset output	Cd = 100 nF		30		ms
V_{RT}	Reset threshold		4.75	V_o-0.15		V
V_{RTH}	Threshold hysteresis			10		mV

Fig. 1 - Timing diagram for reset function



L601 L602 L603 L604

HIGH-VOLTAGE, HIGH-CURRENT 8 DARLINGTON ARRAYS

These high-voltage, high-current Darlington transistor arrays comprise eight NPN Darlington on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak currents of 500 mA can be withstood. They are pinned with inputs opposite outputs to facilitate circuit board layout.

- The L601 is a general-purpose array wich may be used with DTL, TTL, PMOS, CMOS, etc.
- The L602 is specifically designed for use with 14 to 25V PMOS devices. Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.
- The L603 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.
- The L604 has a series base resistor to each Darlington pair, and thus allows operation directly with PMOS or CMOS utilizing supply voltage of 6 to 15V.

In all cases, the individual Darlington collector current rating is 400 mA. However, outputs may be paralleled for higher load current capability. The devices are supplied in a 18-lead dual in-line plastic package with copper frame.

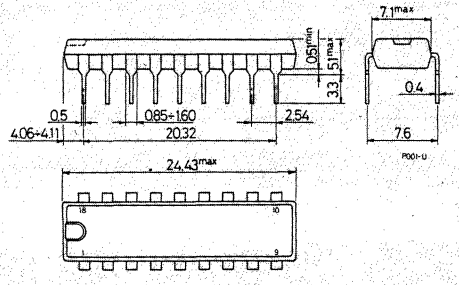
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector emitter voltage (input open)	90	V
I_C	Collector current	0.4	A
I_C	Collector peak current	0.5	A
V_i	Input voltage (for L602, L603 and L604)	30	V
I_i	Input current (for L601 only)	25	mA
P_{tot}	Total power dissipation a $T_{amb} = 25°C$	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

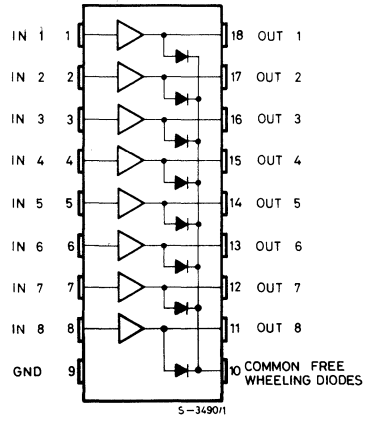
ORDERING NUMBERS: L601B, L602B, L603B, L604B

MECHANICAL DATA

Dimensions in mm

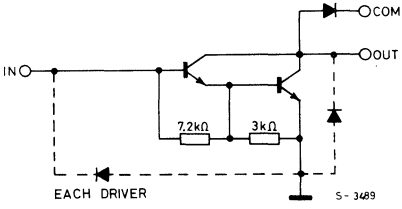


CONNECTION DIAGRAM
(top view)

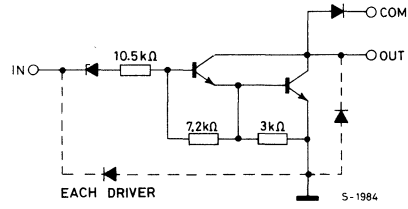


SCHEMATIC DIAGRAMS

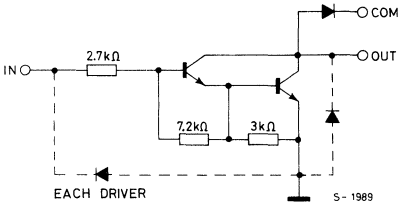
L601



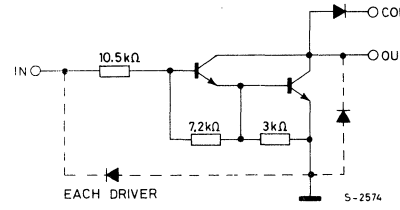
L602



L603



L604



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE}= 90V			10	μA
$V_{CE(sat)}$	Collector emitter saturation voltage	I_C= 300 mA I_B= 500 μA I_C= 200 mA I_B= 350 μA I_C= 100 mA I_B= 250 μA			2 1.7 1.2	V V V
h_{FE}	DC forward current gain (L601 only)	V_{CE}= 3V I_C= 300 mA	1000			—
V_i	Minimum input voltage (ON condition)	V_{CE}= 3V I_C= 300 mA for L602 for L603 for L604			 11.5 2.5 2.5	 V V V
V_i	Maximum input voltage (OFF condition)	V_{CE}= 90V I_C= 25 μA for L601 for L602 for L603 for L604	 0.55 7 0.75 1			 V V V V
I_R	Clamp diode reverse current	V_R= 90V			50	μA
V_F	Clamp diode forward voltage	I_F= 300 mA		2	2.4	V
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o		0.4		μs
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o		0.4		μs

L702

LINEAR INTEGRATED CIRCUIT

QUAD DARLINGTON SWITCH

- SUSTAINING VOLTAGE: MIN. 70V
- 2A OUTPUT
- HIGH CURRENT GAIN

The L 702 is a monolithic integrated circuit for high current and high voltage switching applications. It comprises four darlington transistors with common emitter and open collector, suitable for current sinking applications, mounted on the new **Powerdip** and **Multiwatt** packages.
This circuit reduces components, sizes and costs; it can provide direct interface between low level logic and a variety of high current applications.

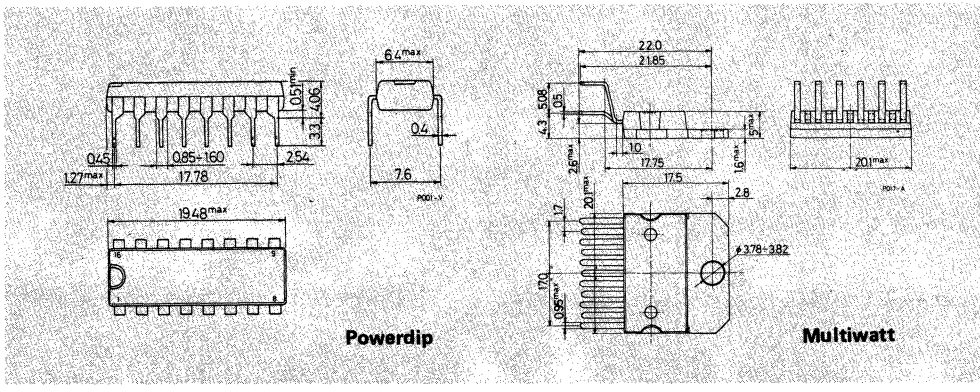
ABSOLUTE MAXIMUM RATINGS

V_{CEX}	Collector-emitter voltage (input open)		90	V
V_i	Input voltage		30	V
I_C	Collector current		2	A
I_C	Collector peak current (repetitive)		3	A
P_{tot}	Total power dissipation at $T_{pin\ 9\ to\ 16} \leqslant 90°C$	Powerdip	4	W
	Total power dissipation at $T_{amb} \leqslant 70°C$	Powerdip	1.1	W
	Total power dissipation at $T_{case} \leqslant 90°C$	Multiwatt	20	W
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Operating junction temperature		-25 to 150	°C

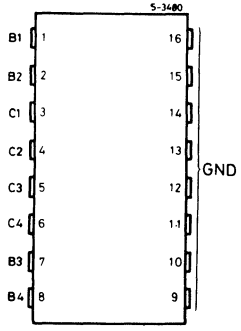
ORDERING NUMBER: L 702B - Powerdip
L 702N - Multiwatt

MECHANICAL DATA

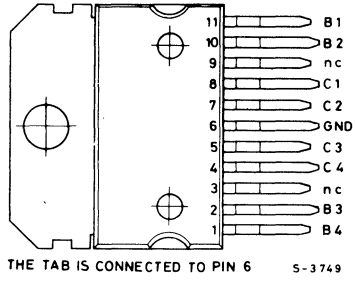
Dimensions in mm



CONNECTION DIAGRAMS (top view)

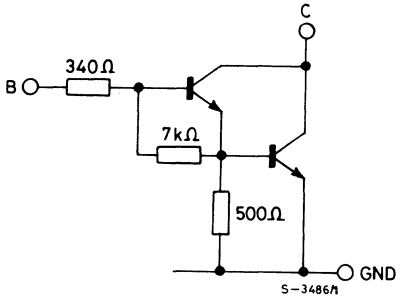


Powerdip



Multiwatt

SCHEMATIC DIAGRAM (each Darlington)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	Powerdip	max	70	°C/W
$R_{th\ j\text{-}pins\ 9/16}$	Thermal resistance junction pins 9 to 16	Powerdip	max	14	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	Multiwatt	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE} = 90V		10	50	μA
$V_{CE\ (sust)}$	Collector emitter (°) sustaining voltage	I_C = 100 mA	70			V
$V_{CE\ (sat)}$	Collector emitter saturation voltage	I_C = 1.25A I_i = 2 mA		1.3	1.9	V
h_{FE}	DC forward current gain	I_C = 1A V_{CE} = 3V	1000	4000		
I_i	Input current	V_i = 3.75V V_i = 2.4V open collector		7 3	11 6	mA mA
V_i	Input voltage off condition	V_{CE} = 70V $I_C \leq$ 0.1 mA			0.4	V
	on condition	V_{CE} = 3V $I_C \geq$ 1A	2.4			V
t_{on}	Turn on time	V_s = 12V		0.3		μs
t_{off}	Turn off time	R_L = 10 Ω		1		μs

(°) Pulsed: pulse duration = 300 μs, duty cycle = 1.5%.

Fig. 1 - Switching time

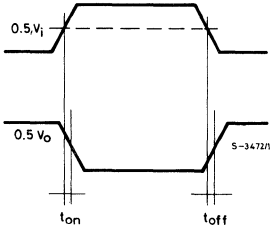


Fig. 2 - t_{on} and t_{off} test circuit

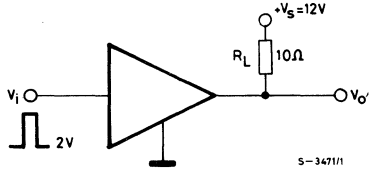


Fig. 3 - Peak collector current vs. duty cycle and number of outputs(L702B only)

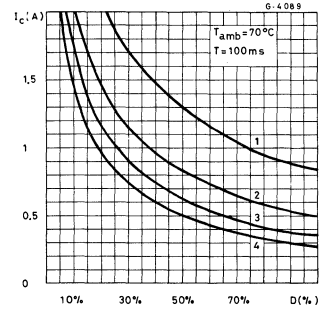


Fig. 4 - Collector emitter saturation voltage vs. collector current

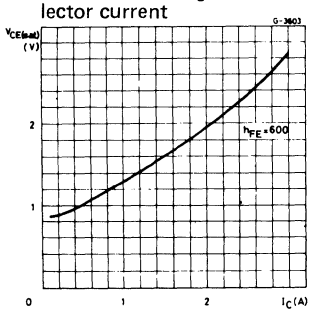


Fig. 5 - Collector current vs. input voltage

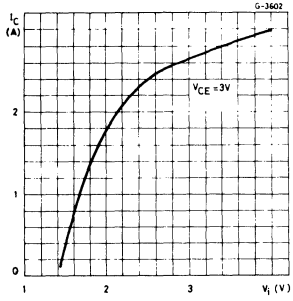


Fig. 6 - Input current vs. input voltage

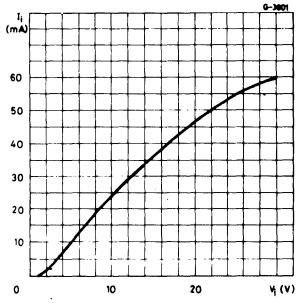


Fig. 7 - Safe operating areas (L702B)

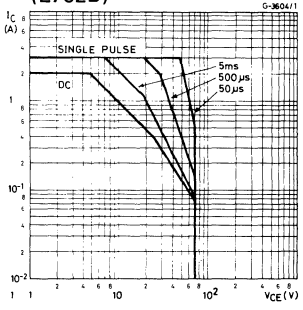


Fig. 8 - Safe operating areas (L702N)

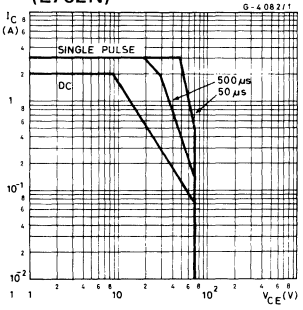
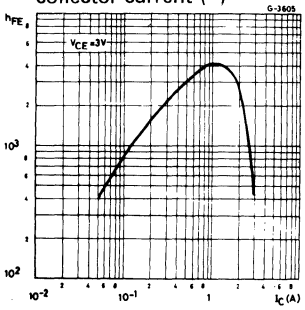
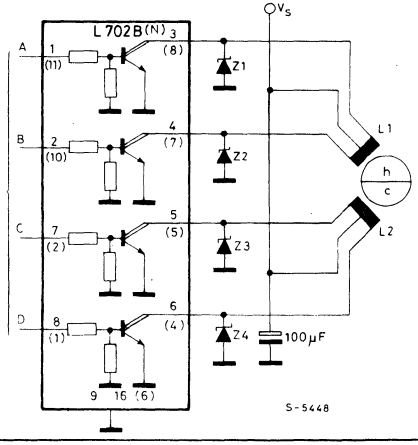


Fig. 9 - DC current gain vs. collector current (*)



(*) Pulse width = 300 μs, duty cycle 1.5%.

Fig. 10 - Stepping motor buffer



L2605
L2685
L2610

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

POSITIVE VOLTAGE REGULATORS FOR AUTOMOTIVE

- OUTPUT VOLTAGE OF 5, 8.5 AND 10V
- OUTPUT CURRENT UP TO 500 mA
- NO EXTERNAL COMPONENTS
- LOW DROP-OUT VOLTAGE
- LOAD DUMP VOLTAGE SURGE PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION
- CURRENT LIMITING
- THERMAL SHUTDOWN

The L2600 series of three therminal positive regulators is specially designed to stabilize power supplies for car instrumentation in vehicles with 12V battery. They can supply an output current up to 500 mA.

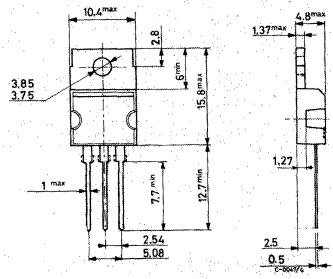
ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	35	V
V_i	DC input reverse voltage	-28	V
V_d	Positive transient peak voltage (t = 40 ms, duty cycle = 1%)	120	V
V_d	Negative transient peak voltage (t = 30 ms, duty cycle = 1%)	-90	V
T_{op}	Operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-65 to 150	°C
P_{tot}	Power dissipation	Internally limited	

ORDERING NUMBERS: L2605V (V_o= 5V)
L2685V (V_o= 8.5V)
L2610V (V_o= 10V)

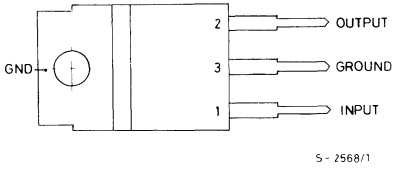
MECHANICAL DATA

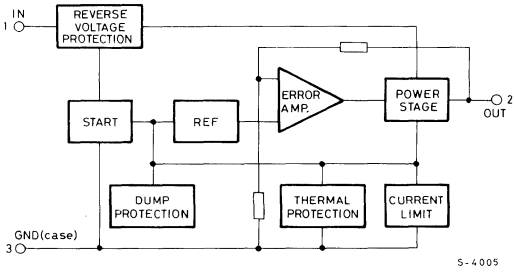
Dimensions in mm



CONNECTION AND BLOCK DIAGRAMS

(top view)





THERMAL DATA

$R_{th\,j\text{-}case}$	Thermal resistance junction-case	max.	4 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_o	Output voltage	I_o = 500 mA	V_i = 12 to 16V (L2605) V_i = 12 to 16V (L2685) V_i = 12 to 16V (L2610)	4.8 8.15 9.55	5 8.5 10	5.2 8.85 10.45	V
V_i	Operating input voltage	see note (°)				28	V
ΔV_o	Line regulation	I_o = 50 mA	V_i = 12 to 16V		2		mV
$\frac{\Delta V_o}{V_o}$	Load regulation	V_i = 14V	I_o = 50 to 500 mA		0.3		%
$\Delta V_{i\text{-}o}$	Dropout voltage	I_o = 500 mA				1.8	V
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o = 50mA T_{amb} = -12 to 80°C	V_i = 14V		-1		mV/°C
I_{sc}	Output short circuit current	V_i = 14V			900		mA
SVR	Supply voltage rejection	V_i = 16V f = 100Hz	ΔV_i = 2V I_o = 500mA		60		dB
R_o	Output resistance	I_o = 500mA			0.05		Ω
e_N	Output noise voltage	BW = 100Hz to 10KHz			20		μV

(°) Note: For a DC input voltage 28V < V_i < 35V the device is not operating

L3654

LINEAR INTEGRATED CIRCUIT

PRELIMINARY DATA

PRINTER SOLENOID DRIVER

The L3654 is a printer solenoid driver containing ten open-collector driver outputs and a ten-bit serial-in, parallel-out shift register.
Data is clocked into the shift register serially and transferred to the open-collector outputs by an enable input. Serial input data is loaded by the rising edge of the clock. A serial output from the tenth bit is provided which changes at the falling edge of the clock. This output is not controlled by the enable input and remains active at all time.
Output stages are inhibited when the logic supply voltage falls below 6V.
Each output is rated at 250 mA (sink) and is clamped to ground internally at 50V to dissipate stored energy in inductive loads.
The L3654 is supplied in a 16 lead dual in-line plastic package, and its main fields of application comprise thermal printers, cash registers and printing pocket calculators.

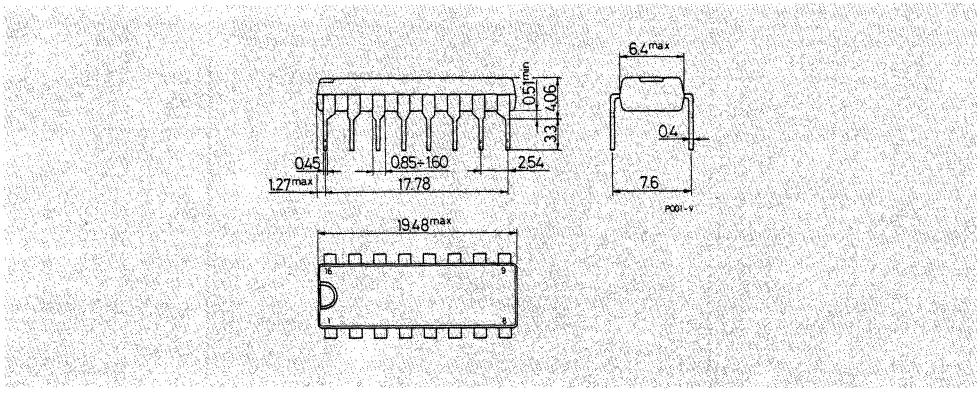
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9.5	V
V_i	Input voltage	9.5	V
V_E	External supply voltage	45	V
I_o	Output current (single output)	0.4	A
I_g	Ground current	4.0	A
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

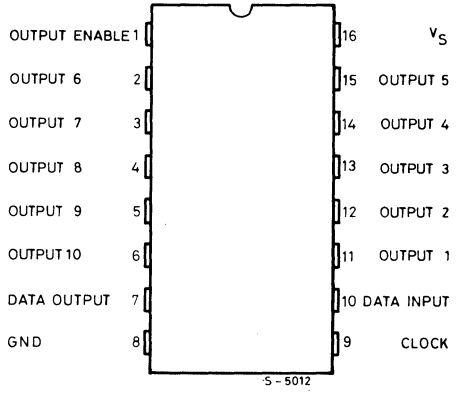
ORDERING NUMBER: L3654 B

MECHANICAL DATA

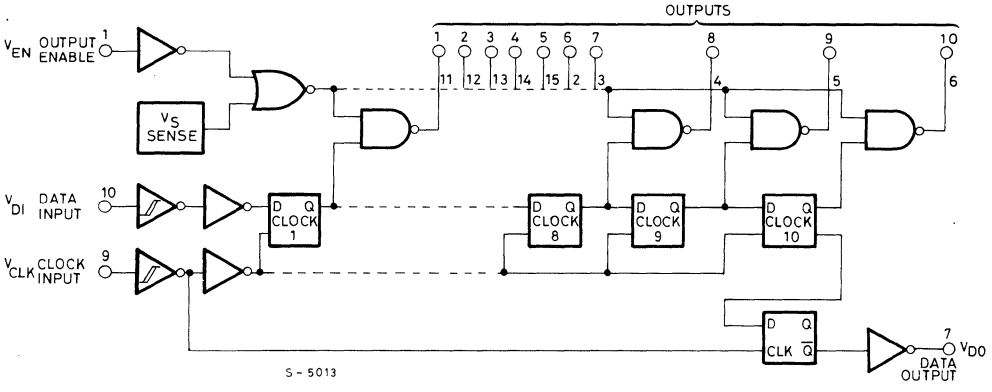
Dimensions in mm



CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



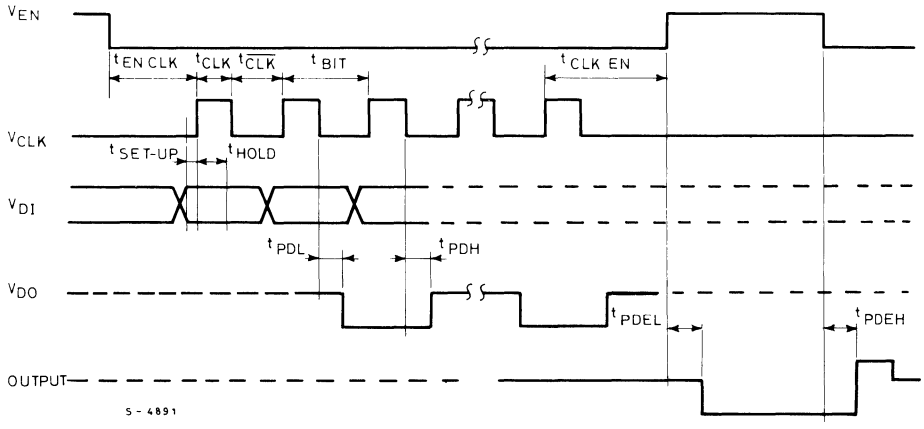
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 8.5V, V_{ss}= 30V, T_{amb}= 0° to 70°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			7.5		9.5	V
I_S	Supply current	T_{amb}= 25°C V_s = 9.5V	V_{EN}= 0V; V_{DO}= 0V		27	40	mA
			V_{EN}= 2.6V I_o = 250 mA (each bit)		55	70	mA
V_E	External operating supply voltage					40	V
I_{leak}	Output leakage current (each output)	V_{ss}= 40V	V_{EN}= 0V			1	mA
V_Z	Internal clamp voltage	I_Z = 0.3A	V_{EN}= 0V	45	50	65	V
$V_{CE\ sat}$	Output saturation voltage	I_o = 250 mA	V_{EN}= 2.6V			1.6	V
V_{DI} V_{CLK} V_{EN}	Input logic levels (pins 1, 9, 10)	Low State (L)				0.8	V
		High state (H)		2.6			
I_{DI}	Data input current	V_{DI}= 2.6V	T_{amb}= 70°C	0.3	0.57		mA
			T_{amb}= 0°C		0.57	0.75	
		V_{DI}= 1V	T_{amb}= 70°C		220		μA
I_{CLK}	Clock input current	V_{CLK}= 2.6V	T_{amb}= 70°C	0.2	0.33		mA
			T_{amb}= 0°C		0.33	0.5	
		V_{CLK}= 1V	T_{amb}= 70°C		125		μA
I_{EN}	Enable input current	V_{EN}= 2.6V	T_{amb}= 70°C	0.2	0.33		mA
			T_{amb}= 0°C		0.33	0.5	
		V_{EN}= 1V	T_{amb}= 70°C		125		μA
R_{IN}	Input pull-down resistance Clock input	T_{amb}= 25°C	$V_{CLK} < V_s$		8		KΩ
	Enable input	T_{amb}= 25°C	$V_{EN} < V_s$		8		
	Data input	T_{amb}= 25°C	$V_{DI} < V_s$		4.5		
V_{DO}	Output logic levels (pin 7)	Low state (L) V_{DI}= 0V	I_{DO}(pin 7)= 0		0.01	0.5	V
		High state (H) V_{DI}= 2.6V I_{DO} (pin 7) = -0.75 mA		2.6	3.4		V
R_{DO}	Output pull-down resistance (pin 7)	V_{DI}= 0V	V_{DO}= 1V		14		KΩ

Fig. 1 - Timing diagram



ELECTRICAL CHARACTERISTICS (see fig. 1 and the section "definition of terms")

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Clock, data and enable input	t_{CLK}		4			µs
	$\overline{t_{CLK}}$		5.5			
	t_{SET-UP}		1			
	t_{HOLD}		3			
Clock to enable delay	$t_{CLK\ EN}$		2 t_{BIT}			
Enable to clock delay	$t_{EN\ CLK}$		t_{BIT}			
Data output delay	t_{PDH}, t_{PDL}	R_L= 5KΩ, $C_L \leqslant$ 10 pF		0.8	2.5	µs
Output delay	t_{PDEL}			3		µs
	t_{PDEH}			3.5		
Output rise time		R_L= 100 Ω, $C_L <$ 100 pF		1.2		µs
Output fall time		R_L= 100 Ω, $C_L <$ 100 pF		1.2		µs
V_{DO} rise time				0.4		µs
V_{DO} fall time				0.4		µs

DEFINITION OF TERMS

V_{ss} : External power supply voltage. The return for open-collector relay driver outputs.

V_{DI}, V_{CLK}, V_{EN} : The voltages at the data, clock and enable inputs respectively.

V_{DO} : The voltage at data output.

t_{BIT} : Period of the incoming clock.

t_{CLK} : The portion of t_{BIT} when $V_{CLK} \geqslant 2.6V$.

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leqslant 0.8V$.

t_{HOLD} : The time following the start of t_{CLK} required to transfer data within the shift register.

$t_{SET\text{-}UP}$: The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

LINEAR INTEGRATED CIRCUITS

L7800 Series

3-TERMINAL POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

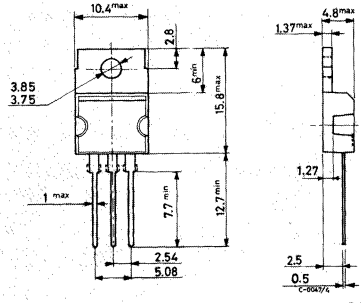
The L7800 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

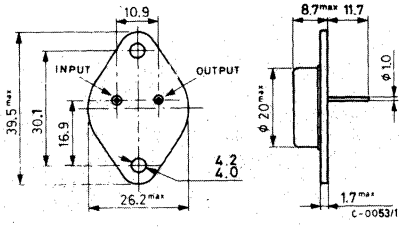
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	internally limited	
T_{op}	Operating junction temperature (for **L7800**)	-55 to +150	°C
	(for **L7800C**)	0 to +150	°C
T_{stg}	Storage temperature	-65 to +150	°C

MECHANICAL DATA

Dimensions in mm



TO-220

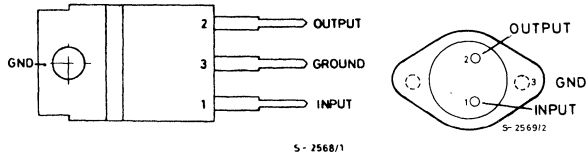


TO-3

L7800 Series

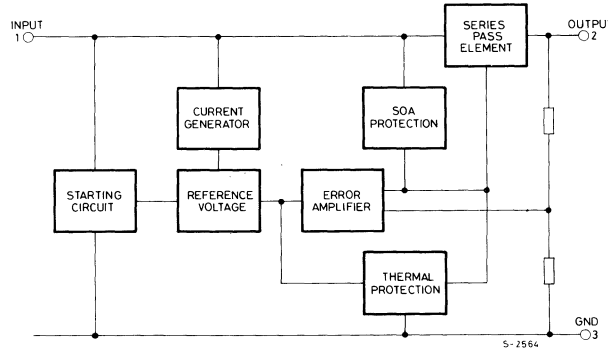
CONNECTION DIAGRAMS AND ORDERING NUMBERS

(top views)

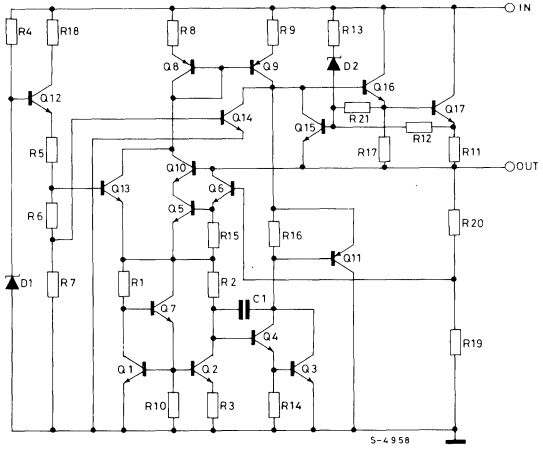


Type	TO-220	TO-3	Output voltage
L 7805	–	L 7805T	5V
L 7805C	L 7805CV	L 7805 CT	5V
L 7806	–	L 7806T	6V
L 7806C	L 7806 CV	L 7806CT	6V
L 7808	–	L 7808T	8V
L 7808C	L 7808 CV	L 7808CT	8V
L 7812	–	L 7812T	12V
L 7812C	L 7812CV	L 7812CT	12V
L 7815	–	L 7815T	15V
L 7815C	L 7815CV	L 7815CT	15V
L 7818	–	L 7818T	18V
L 7818C	L 7818CV	L 7818CT	18V
L 7820	–	L 7820T	20V
L 7820C	L 7820CV	L 7820CT	20V
L 7824	–	L 7824T	24V
L 7824C	L 7824CV	L 7824CT	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

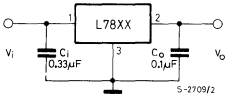


Fig. 2 - Load regulation

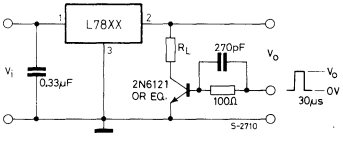
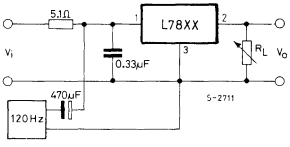


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L 7800 (Refer to the test circuits, T_j= -55 to 150°C, I_o = 500 mA, C_i = 0.33 µF, C_o= 0.1 µF unless otherwise specified)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o= 5 mA to 1A, $P_o \leq$ 15W	4.65	5	5.15 (V_i= 8 to 20V)	5.65	6	6.35 (V_i= 9 to 21V)	7.6	8	8.4 (V_i= 11.5 to 23V)	11.4	12	12.6 (V_i= 15.5 to 27V)	
ΔV_o	Line regulation	T_j= 25°C			50 (V_i= 7 to 25V)			60 (V_i= 8 to 25V)			80 (V_i= 10.5 to 25V)			120 (V_i= 14.5 to 30V)	mV
					25 (V_i= 8 to 12V)			30 (V_i= 9 to 13V)			40 (V_i= 11 to 17V)			60 (V_i= 16 to 22V)	
ΔV_o	Load regulation	T_j= 25°C, I_o= 5 mA to 1.5A			100			100			100			120	mV
		T_j= 25°C, I_o= 250 to 750 mA			25			30			40			60	
I_d	Quiescent current	T_j= 25°C			6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					0.8 (V_i= 8 to 25V)			0.8 (V_i= 9 to 25V)			0.8 (V_i= 11.5 to 25V)			0.8 (V_i= 15 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		0.6			0.7			1			1.5		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz, T_j= 25°C			40			40			40			40	$\frac{\mu V}{V_o}$
SVR	Supply voltage rejection	f = 120 Hz	68 (V_i= 8 to 18V)			65 (V_i= 9 to 19V)			62 (V_i= 11.5 to 21.5V)			61 (V_i= 15 to 25V)			dB
V_d	Dropout voltage	I_o= 1A, T_j= 25°C		2	2.5		2	2.5		2	2.5		2	2.5	V
R_o	Output resistance	f = 1 KHz		17			19			16			18		mΩ
I_{sc}	Short circuit current	V_i= 35V, T_j= 25°C		0.75	1.2		0.75	1.2		0.75	1.2		0.75	1.2	A
I_{scp}	Short circ. peak current	T_j= 25°C	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS L 7800 (continued)

OUTPUT VOLTAGE			15			18			20			24			
INPUT VOLTAGE (Unless otherwise specified)			23			26			28			33			Unit
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_o= 5 mA to 1A, $P_o \leq$ 15W	14.25	15	15.75 (V_i= 18.5 to 30V)	17.1	18	18.9 (V_i= 22 to 33V)	19	20	21 (V_i= 24 to 35V)	22.8	24	25.2 (V_i= 28 to 38V)	
ΔV_o	Line regulation	T_j = 25°C			150 (V_i= 17.5 to 30V)			180 (V_i= 21 to 33V)			200 (V_i= 22.5 to 35V)			240 (V_i= 27 to 38V)	mV
					75 (V_j= 20 to 26V)			90 (V_i= 24 to 30V)			100 (V_i= 26 to 32V)			120 (V_i= 30 to 36V)	
ΔV_o	Load regulation	T_j= 25°C, I_o= 5 mA to 1.5A			150			180			200			240	mV
		T_j= 25°C, I_o= 250 to 750 mA			75			90			100			120	
I_d	Quiescent current	T_j= 25°C			6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					0.8 (V_i= 18.5 to 30V)			0.8 (V_i= 22 to 33V)			0.8 (V_i= 24 to 35V)			0.8 (V_i= 28 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		1.8			2.3			2.5			3		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz, T_j= 25°C		40			40			40			40		$\frac{\mu V}{V_o}$
SVR	Supply voltage rejection	f = 120 Hz	60 (V_i=18.5 to 28.5V)			59 (V_i= 22 to 32V)			58 (V_i= 24 to 35V)			56 (V_i= 28 to 38V)			dB
V_d	Dropout voltage	I_o= 1A, T_j= 25°C		2	2.5		2	2.5		2	2.5		2	2.5	V
R_o	Output resistance	f = 1 KHz		19			22			24			28		mΩ
I_{sc}	Short circuit current	V_i= 35V, T_j= 25°C		0.75	1.2		0.75	1.2		0.75	1.2		0.75	1.2	A
I_{scp}	Short circ. peak current	T_j= 25°C	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS L 7800C (Refer to the test circuits, T_j = 0 to 125°C, I_o = 500 mA, C_i = 0.33 μF, C_o = 0.1 μF unless otherwise specified)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			Unit
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o= 5 mA to 1A $P_o \leq$ 15W	4.75	5	5.25 (V_i= 7 to 20V)	5.7	6	6.3 (V_i= 8 to 21V)	7.6	8	8.4 (V_i= 10.5 to 25V)	11.4	12	12.6 (V_i= 14.5 to 27V)	
ΔV_o	Line regulation	T_j= 25°C		3	100 (V_i= 7 to 25V)			120 (V_i= 8 to 25V)			160 (V_i= 10.5 to 25V)			240 (V_i= 14.5 to 30V)	mV
				1	50 (V_i= 8 to 12V)			60 (V_i= 9 to 13V)			80 (V_i= 11 to 17V)			120 (V_i= 16 to 22V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			100			120			160			240	mV
		T_j= 25°C I_o= 250 to 750 mA			50			60			80			120	
I_d	Quiescent current	T_j= 25°C			8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3 (V_i= 7 to 25V)			1.3 (V_i= 8 to 25V)			1 (V_i= 10.5 to 25V)			1 (V_i= 14.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-1.1			-0.8			-0.8			-1		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz T_j= 25°C		40			45			52			75		μV
SVR	Supply voltage rejection	f = 120 Hz	62 (V_i= 8 to 18V)			59 (V_i= 9 to 19V)			56 (V_i= 11.5 to 21.5V)			55 (V_i= 15 to 25V)			dB
V_d	Dropout voltage	I_o= 1A		2			2			2			2		V
R_o	Output resistance	f = 1 KHz		17			19			16			18		mΩ
I_{sc}	Short circuit current	V_i= 35V T_j= 25°C		750			550			450			350		mA
I_{scp}	Short circ. peak current	T_j = 25°C		2.2			2.2			2.2			2.2		A

ELECTRICAL CHARACTERISTICS L 7800C (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			28			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_o= 5 mA to 1A $P_o \leqslant$ 15W	14.25	15	15.75 (V_i= 17.5 to 30V)	17.1	18	18.9 (V_i= 21 to 33V)	19	20	21 (V_i= 23 to 35V)	22.8	24	25.2 (V_i= 27 to 38V)	
ΔV_o	Line regulation	T_j= 25°C			300 (V_i= 17.5 to 30V)			360 (V_i= 21 to 33V)			400 (V_i= 22.5 to 35V)			480 (V_i= 27 to 38V)	mV
					150 (V_i= 20 to 26V)			180 (V_i= 24 to 30V)			200 (V_i= 26 to 32V)			240 (V_i= 30 to 36V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			300			360			400			480	mV
		T_j= 25°C I_o= 250 to 750 mA			150			180			200			240	
I_d	Quiescent current	T_j= 25°C			8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1 (V_i= 17.5 to 30V)			1 (V_i= 21 to 33V)			1 (V_i= 23 to 35V)			1 (V_i= 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-1			-1			-1			-1.5		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz T_j= 25°C		90			110			150			170		μV
SVR	Supply voltage rejection	f = 120 Hz	54			53			52			50			dB
V_d	Dropout voltage	I_o= 1A		2			2			2			2		V
R_o	Output resistance	f = 1 KHz		19			22			24			28		mΩ
I_{sc}	Short circuit current	V_i= 35V T_j = 25°C		230			200			180			150		mA
I_{scp}	Short circ. peak current	T_j = 25°C		2.1			2.1			2.1			2.1		A

Fig. 4 - Dropout voltage vs. junction temperature

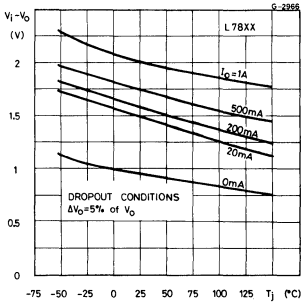


Fig. 5 - Peak output current vs. input/output differential voltage

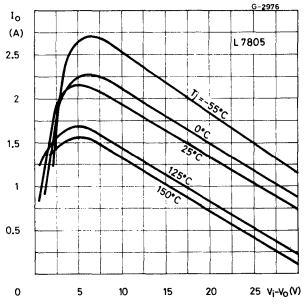


Fig. 6 - Supply voltage rejection vs. frequency

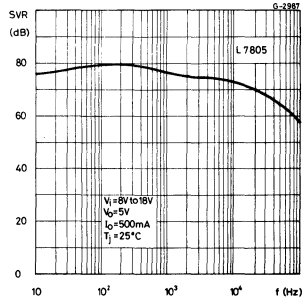


Fig. 7 - Output voltage vs. junction temperature

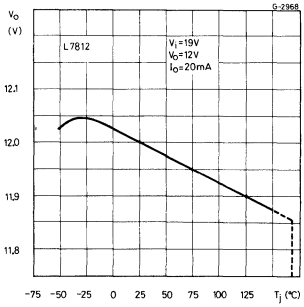


Fig. 8 - Output impedance vs. frequency

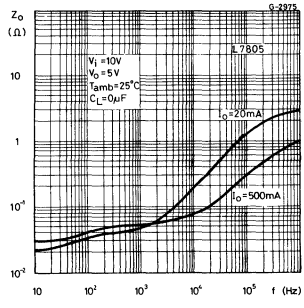


Fig. 9 - Quiescent current vs. junction temperature

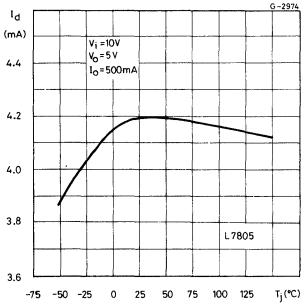


Fig. 10 - Load transient response

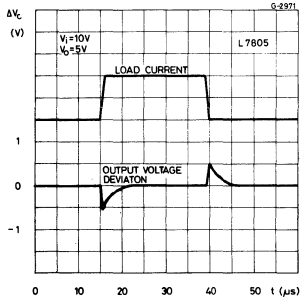


Fig. 11 - Line transient response

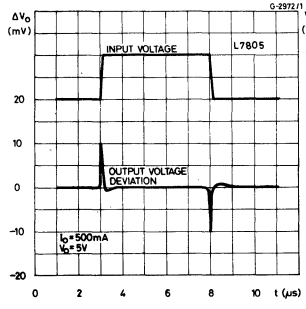
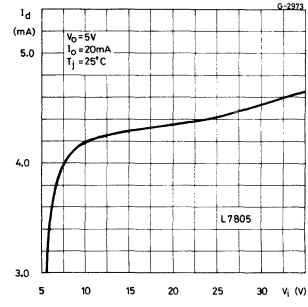
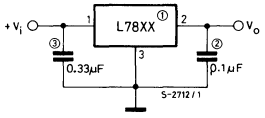


Fig. 12 - Quiescent current vs. input voltage



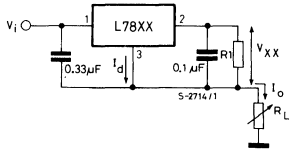
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



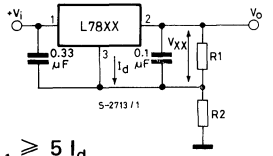
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\ (1 + \frac{R_2}{R_1}) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

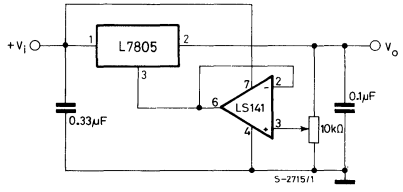
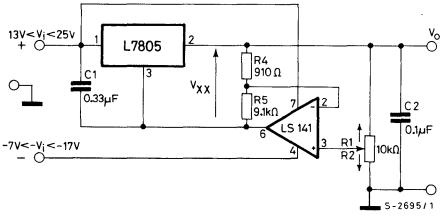
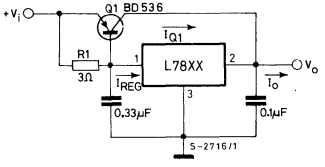


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\ \frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

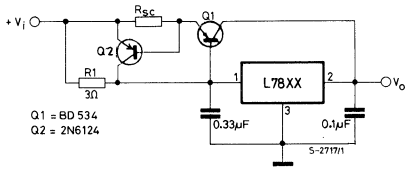


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\ [I_{REG} - \frac{V_{BEQ_1}}{R_1}]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

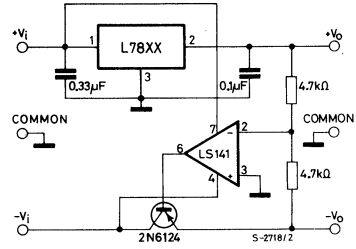
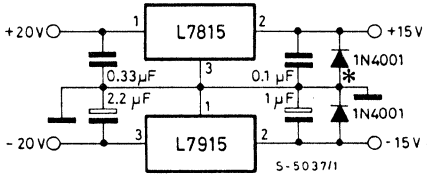


Fig. 21 - Split power supply (±15V - 1A)



* Against potential latch-up problems

Fig. 22 - Negative output voltage circuit

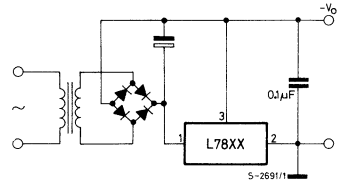


Fig. 23 - Switching regulator

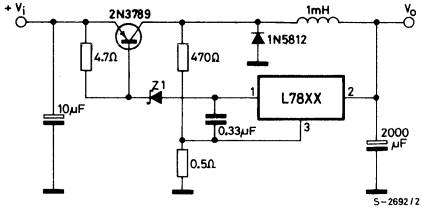
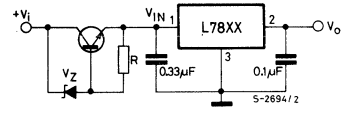


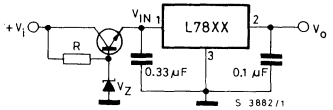
Fig. 24 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

APPLICATION INFORMATION (continued)

Fig. 25 - High input voltage circuit



$$V_{IN} = V_Z - V_{BE}$$

Fig. 26 - High output voltage regulator

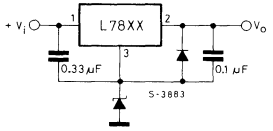
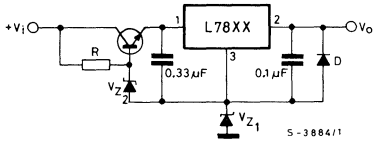
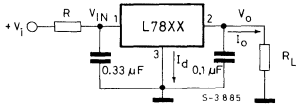


Fig. 27 - High input and output voltage



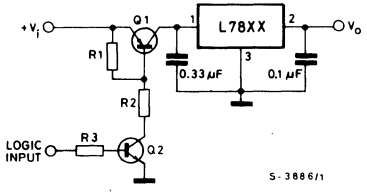
$$V_O = V_{XX} + V_{Z1}$$

Fig. 28 - Reducing power dissipation with dropping resistor



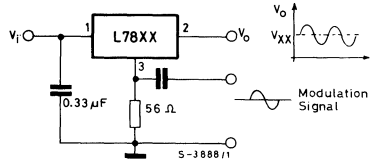
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 29 - Remote shuntdown



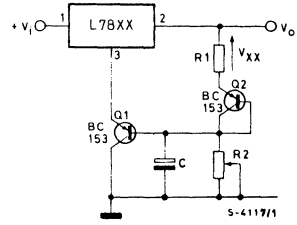
APPLICATION INFORMATION (continued)

Fig. 30 - Power AM modulator (unity voltage gain, $I_o \leq 1A$)



Note: The circuit performs well up to 100 KHz.

Fig. 31 - Adjustable output voltage with temperature compensation

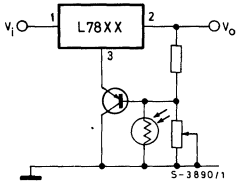


Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

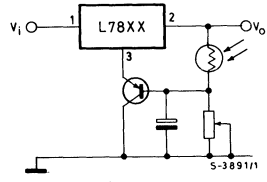
Fig. 32 - Light controllers ($V_{o\ min} = V_{XX} + V_{BE}$)

(a)



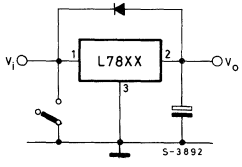
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 33 - Protection against input short-circuit with high capacitance loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

LINEAR INTEGRATED CIRCUITS

L78M00 Series

PRELIMINARY DATA

3-TERMINAL POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 0.5A
- OUTPUT VOLTAGES OF 5; 6; 8; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

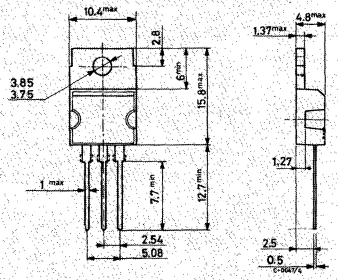
The L78M00 series of three-terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

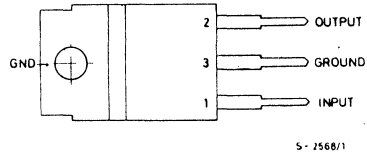
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 20, 24V)	40	V
I_o	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_{op}	Operating junction temperature	0 to +150	°C

MECHANICAL DATA

Dimensions in mm

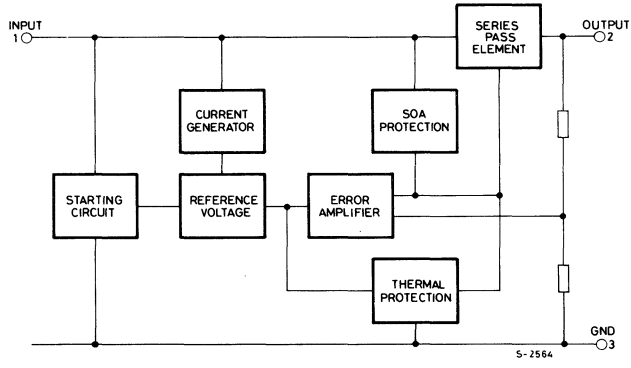


CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)

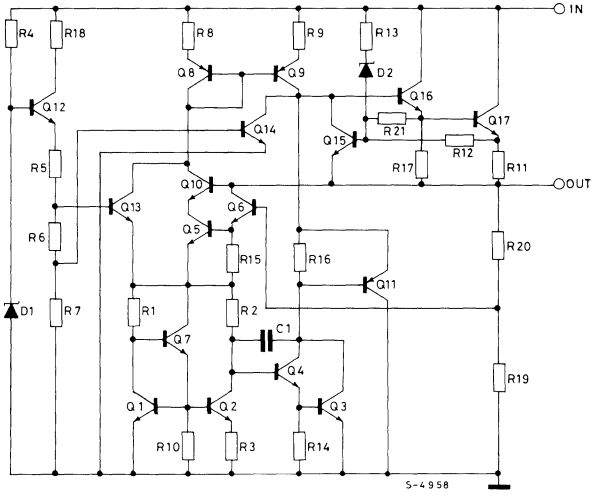


Ordering Numbers	Output Voltage
L78M05CV	5V
L78M06CV	6V
L78M08CV	8V
L78M12CV	12V
L78M15CV	15V
L78M18CV	18V
L78M20CV	20V
L78M24CV	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

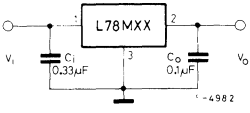


Fig. 2 - Load regulation

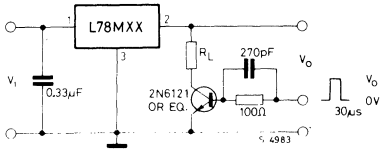
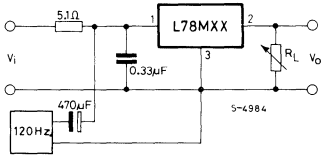


Fig. 3 - Ripple rejection



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

ELECTRICAL CHARACTERISTICS L78M00C (Refer to the test circuits, T_j= 25°C, I_o= 350 mA unless otherwise specified, C_i = 0.33 μF, C_o = 0.1 μF)

OUTPUT VOLTAGE			5			6			8			12			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			11			14			19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	11.5	12	12.5	V
		I_o= 5 to 350 mA	4.75	5	5.25 (V_i= 7 to 20V)	5.7	6	6.3 (V_i= 8 to 21V)	7.6	8	8.4 (V_i= 10.5 to 23V)	11.4	12	12.6 (V_i= 14.5 to 27V)	
ΔV_o	Line regulation	I_o= 200 mA			100 (V_i= 7 to 25V)			100 (V_i= 8 to 25V)			100 (V_i= 10.5 to 25V)			100 (V_i= 14.5 to 30V)	mV
					50 (V_i= 8 to 25V)			50 (V_i= 9 to 25V)			50 (V_i= 11 to 25V)			50 (V_i= 16 to 30V)	
ΔV_o	Load regulation	I_o= 5 mA to 0.5A			100			120			160			240	mV
		I_o= 5 mA to 200 mA			50			60			80			120	
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_o= 200 mA			0.8 (V_i= 8 to 25V)			0.8 (V_i= 9 to 25V)			0.8 (V_i= 10.5 to 25)			0.8 (V_i= 14.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output Voltage drift	I_o= 5 mA T_j= 0 to 125°C		-0.5			-0.5			-0.5			-1.0		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		40			45			52			75		μV
SVR	Supply voltage rejection	f = 120 Hz I_o= 300 mA	62 (V_i= 8 to 18V)			59 (V_i= 9 to 19V)			56 (V_i=11.5 to 21.5V)			55 (V_i= 15 to 25V)			dB
V_d	Dropout voltage			2			2			2			2		V
I_{sc}	Short circuit current	V_i= 35V		300			270			250			240		mA
I_{scp}	Short circ. peak current			700			700			700			700		mA

ELECTRICAL CHARACTERISTICS L78M00C (continued)

OUTPUT VOLTAGE			15			18			20			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			23			26			29			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage		14.4	15	15.6	17.3	18	18.7	19.2	20	20.8	23	24	25	V
		I_o= 5 to 350 mA	14.25 (V_i= 17.5 to 30V)	15	15.75	17.1 (V_i= 20.5 to 33V)	18	18.9	19 (V_i= 23 to 35V)	20	21	22.8 (V_i= 27 to 38V)	24	25.2	
ΔV_o	Line regulation	I_o= 200 mA			100 (V_i= 17.5 to 30V)			100 (V_i= 21 to 33V)			100 (V_i= 23 to 35V)			100 (V_i= 27 to 38V)	mV
					50 (V_i= 20 to 30V)			50 (V_i= 24 to 33V)			50 (V_i= 24 to 35V)			50 (V_i= 28 to 38V)	
ΔV_o	Load regulation	I_o= 5 mA to 0.5A			300			360			400			480	mV
		I_o= 5 mA to 200 mA			150			180			200			240	
I_d	Quiescent current				6			6			6			6	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 350 mA			0.5			0.5			0.5			0.5	mA
		I_o= 200 mA			0.8 (V_i= 17.5 to 30V)			0.8 (V_i= 21 to 33V)			0.8 (V_i= 23 to 35V)			0.8 (V_i= 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA T_{amb}= 0 to 125°C		-1			-1.1			-1.1			-1.2		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		90			100			110			170		μV
SVR	Supply voltage rejection	f = 120 Hz I_o= 300 mA	54 (V_i=18.5 to 28.5V)			53 (V_i= 22 to 32V)			53 (V_i= 24 to 34V)			50 (V_i= 28 to 38V)			dB
V_d	Dropout Voltage			2			2			2			2		V
I_{sc}	Short circuit current	V_i= 35V		240			240			240			240		mA
I_{scp}	Short circ. peak current			700			700			700			700		mA

Fig. 4 - Dropout voltage vs. junction temperature

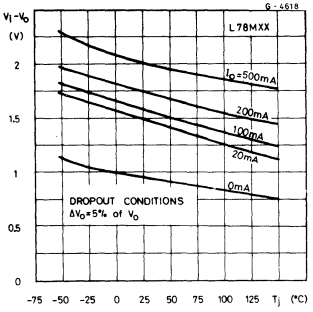


Fig. 5 - Dropout characteristics

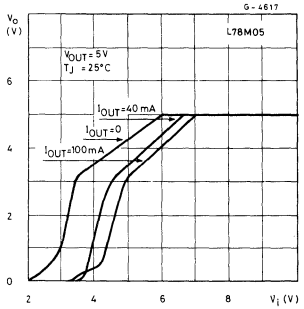


Fig. 6 - Peak output current vs. input-output differential voltage

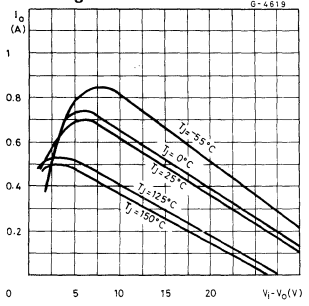


Fig. 7 - Output voltage vs. junction temperature

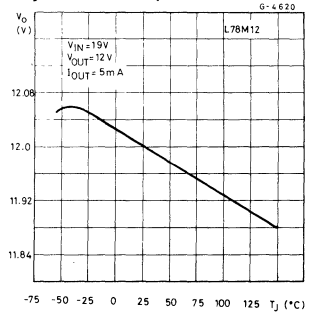


Fig. 8 - Supply voltage rejection vs. frequency

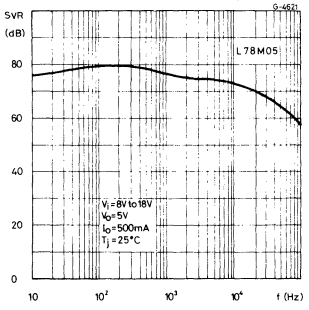


Fig. 9 - Quiescent current vs. junction temperature

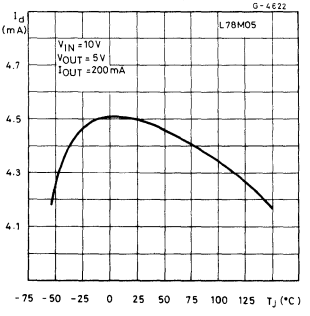


Fig. 10 - Load transient response

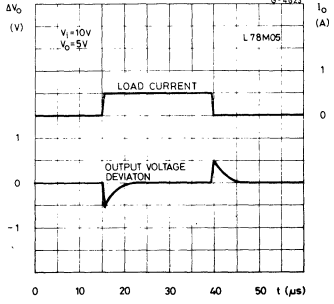


Fig. 11 - Line transient response

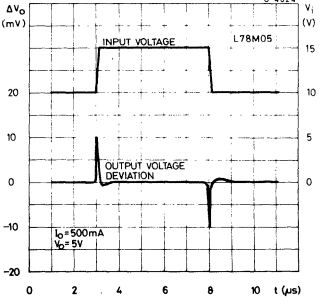
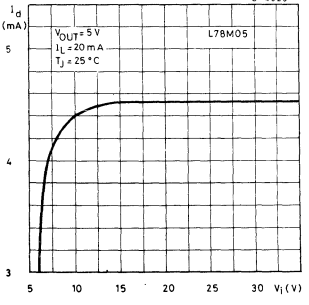
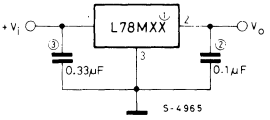


Fig. 12 - Quiescent current vs. input voltage



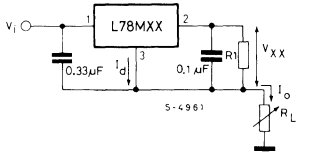
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



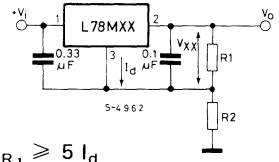
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\ (1 + \frac{R_2}{R_1}) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

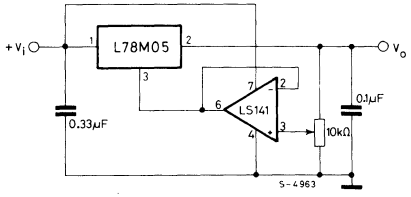
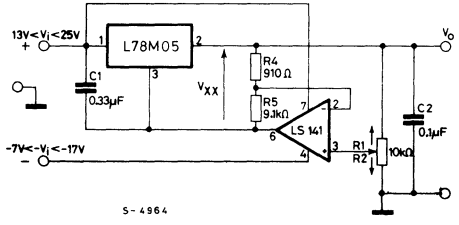
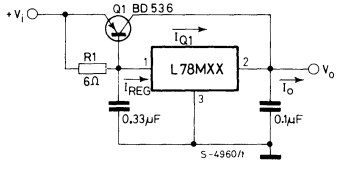


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\ \frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

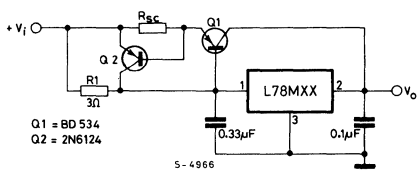


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\ [I_{REG} - \frac{V_{BEQ_1}}{R_1}]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

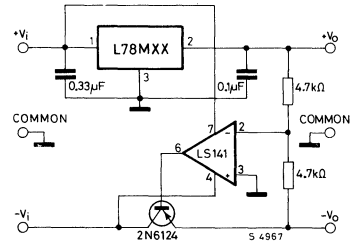
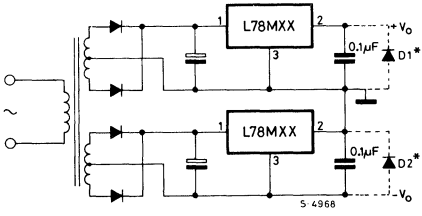


Fig. 21 - Positive and negative regulator



(*) D_1 and D_2 are necessary if the load is connected between $+V_o$ and $-V_o$

Fig. 22 - Negative output voltage circuit

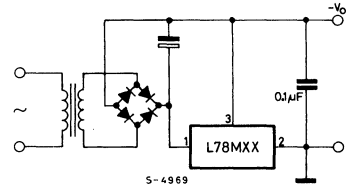
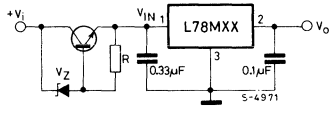
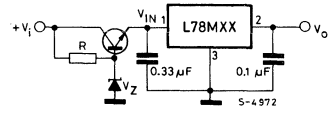


Fig. 23 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

Fig. 24 - High input voltage circuit



$$V_{IN} = V_Z - V_{BE}$$

APPLICATION INFORMATION (continued)

Fig. 25 - High output voltage regulator

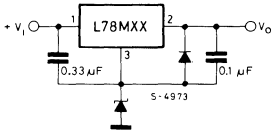
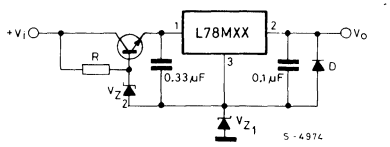
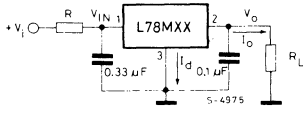


Fig. 26 - High input and output voltage



$$V_O = V_{XX} + V_{Z1}$$

Fig. 27 - Reducing power dissipation with dropping resistor



$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 28 - Remote shuntdown

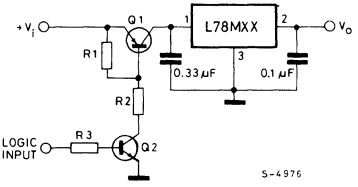
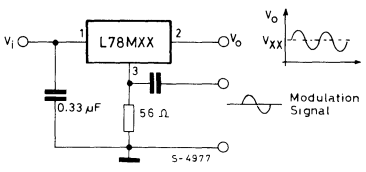
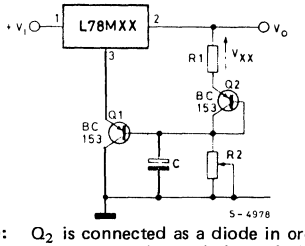


Fig. 29 - Power AM modulator (unity voltage gain, $I_o \leqslant 0.5$)



Note: The circuit performs well up to 100 KHz.

Fig. 30 - Adjustable output voltage with temperature compensation



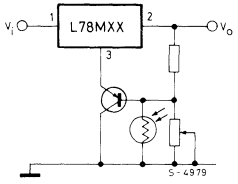
Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

APPLICATION INFORMATION (continued)

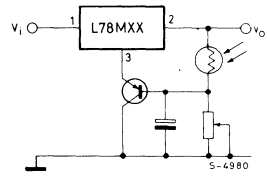
Fig. 31 - Light controllers ($V_{o\ min} = V_{XX} + V_{BE}$)

(a)



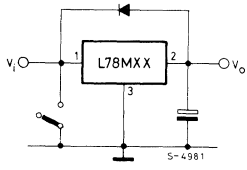
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 32 - Protection against input short-circuit with high capacitance loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 32) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

3-TERMINAL POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 2A
- OUTPUT VOLTAGES OF 5; 7.5; 9; 10; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

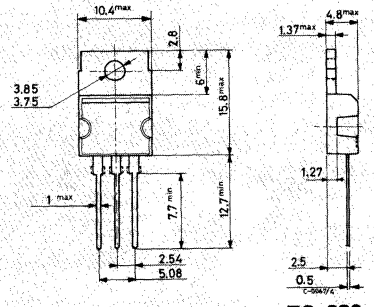
The L78S00 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 2A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

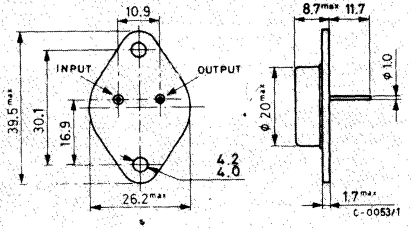
V_i	DC input voltage (for V_o = 5 to 18V)	35	V
	(for V_o = 24V)	40	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation	Internally limited	
T_{stg}	Storage temperature	-65 to +150	°C
T_{op}	Operating junction temperature (for **L78S00**)	-55 to +150	°C
	(for **L78S00C**)	0 to +150	°C

MECHANICAL DATA

Dimensions in mm



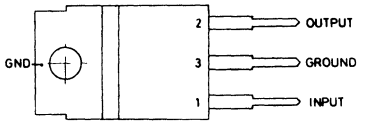
TO-220

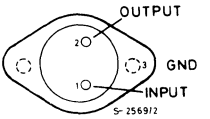


TO-3

L78S00 Series

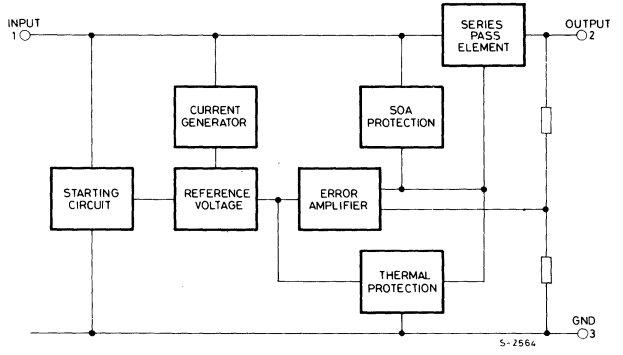
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



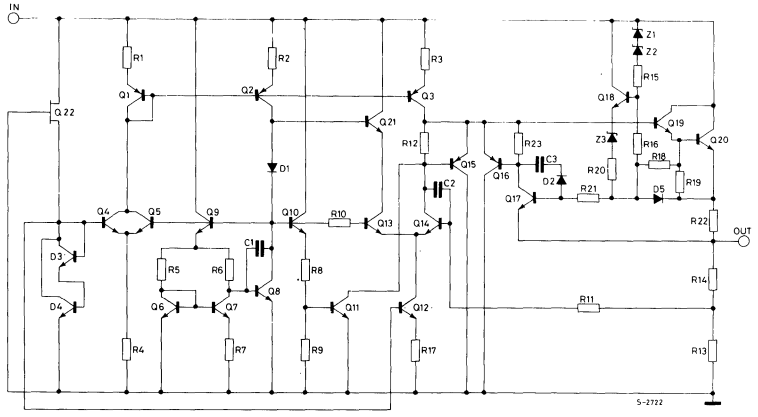


Type	TO-220	TO-3	Output voltage
L 78S05	–	L 78S05T	5V
L 78S05C	L 78S05CV	L 78S05CT	5V
L 78S75	–	L 78S75T	7.5V
L 78S75C	L 78S75CV	L 78S75CT	7.5V
L 78S09	–	L 78S09T	9V
L 78S09C	L 78S09CV	L 78S09CT	9V
L 78S10	–	L 78S10T	10V
L 78S10C	L 78S10CT	L 78S10CT	10V
L 78S12	–	L 78S12T	12V
L 78S12C	L 78S12CV	L 78S12CT	12V
L 78S15	–	L 78S15T	15V
L 78S15C	L 78S15CV	L 78S15CT	15V
L 78S18	–	L 78S18T	18V
L 78S18C	L 78S18CV	L 78S18CT	18V
L 78S24	–	L 78S24T	24V
L 78S24C	L 78S24CV	L 78S24CT	24V

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUITS

Fig. 1 - DC parameters

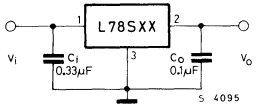


Fig. 2 - Load regulation

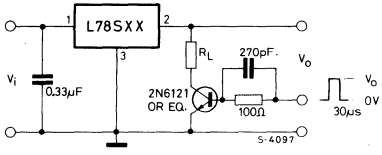
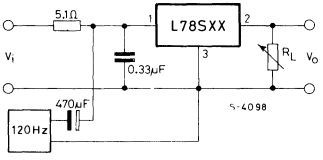


Fig. 3 - Ripple rejection



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L78S00 (Refer to the test circuits, T_j= 25°C, I_o= 500 mA unless otherwise specified)

OUTPUT VOLTAGE			5			7.5			9			10			Unit
INPUT VOLTAGE (Unless otherwise specified)			10			12.5			14			15			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		4.8	5	5.2	7.15	7.5	7.9	8.65	9	9.35	9.5	10	10.5	V
		I_o= 1A	4.75	5	5.25 (V_i= 7V)	7.1	7.5	7.95 (V_i= 9.5V)	8.6	9	9.4 (V_i= 11V)	9.4	10	10.6 (V_i= 12.5V)	
ΔV_o	Line regulation				100 (V_i= 7 to 25V)			120 (V_i= 9.5 to 25V)			130 (V_i= 11 to 25V)			200 (V_i= 12.5 to 30V)	mV
					50 (V_i= 8 to 12V)			60 (V_i= 10.5 to 20V)			65 (V_i= 11 to 20V)			100 (V_i= 14 to 22V)	
ΔV_o	Load regulation	I_o= 20 mA to 2A			100			120			130			150	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1.3 (V_i= 7 to 25V)			1.3 (V_i= 9.5 to 25V)			1.3 (V_i= 11 to 25V)			1 (V_i= 12.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA T_j= -55 to 150°C			-1.1			-0.8			-1			-1	mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz			40			52			60			65	μV
SVR	Supply voltage rejection	f = 120 Hz	60			54			53			53			dB
V_i	Operating input voltage	$I_o \leqslant$ 1.5A	8			10.5			12			13			V
R_o	Output resistance	f = 1 KHz		17			16			17			17		mΩ
I_{sc}	Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short circ. peak current				3.5			3.5			3.5			3.5	A

ELECTRICAL CHARACTERISTICS L78S00 (continued)

OUTPUT VOLTAGE			12			15			18			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			19			23			26			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
		I_o= 1A	11.4 (V_i= 14.5V)	12	12.6	14.25 (V_i= 17.5V)	15	15.75	17 (V_i= 20.5V)	18	19	22.8 (V_i= 27V)	24	25.2	
ΔV_o	Line regulation				240 (V_i= 14.5 to 30V)			300 (V_i= 17.5 to 30V)			360 (V_i= 20.5 to 30V)			480 (V_i= 27 to 38V)	mV
					120 (V_i= 16 to 22V)			150 (V_i= 20 to 26V)			180 (V_i= 22 to 28V)			240 (V_i= 30 to 36V)	
ΔV_o	Load regulation	I_o= 20 mA to 2A			160			180			200			250	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1 (V_i= 14.5 to 30V)			1 (V_i= 17.5 to 30V)			1 (V_i= 22 to 33V)			1 (V_i= 28 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5mA T_{amb}= 0 to 70°C		-1			-1			-1			-1.5		mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz		75			90			110			170		μV
SVR	Supply voltage rejection	f = 120 Hz	53			52			49			48			dB
V_i	Operating input voltage	$I_o \leq$ 1.5A	15			18			21			27			V
R_o	Output resistance	f = 1 KHz		18			19			22			28		mΩ
I_{sc}	Short circuit current	V_i = 27V	500			500			500			500			mA
I_{scp}	Short circ. peak current				3.5			3.5			3.5			3.5	A

ELECTRICAL CHARACTERISTICS L78S00C (Refer to the test circuits, T_j= 25°C, I_o= 500mA unless otherwise specified)

OUTPUT VOLTAGE			5	7.5	9	10	Unit
INPUT VOLTAGE (Unless otherwise specified)			10	12.5	14	15	
Parameter		Test conditions	Min. Typ. Max.	Min. Typ. Max.	Min. Typ. Max.	Min. Typ. Max.	
V_o	Output voltage		4.8 5 5.2	7.15 7.5 7.9	8.65 9 9.35	9.5 10 10.5	V
		I_o= 1A	4.75 5 5.25 (V_i= 7V)	7.1 7.5 7.95 (V_i= 9.5V)	8.6 9 9.4 (V_i= 11V)	9.4 10 10.6 (V_i= 12.5V)	
ΔV_o	Line regulation		100 (V_i= 7 to 25V)	120 (V_i= 9.5 to 25V)	130 (V_i= 11 to 25V)	200 (V_i= 12.5 to 30V)	mV
			50 (V_i= 8 to 12V)	60 (V_i= 10.5 to 20V)	65 (V_i= 11 to 20V)	100 (V_i= 14 to 22V)	
ΔV_o	Load regulation	I_o= 20 mA to 2A	100	140	170	240	mV
I_d	Quiescent current		8	8	8	8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A	0.5	0.5	0.5	0.5	mA
		I_o= 20 mA	1.3 (V_i= 7 to 25V)	1.3 (V_i = 9.5 to 25V)	1.3 (V_i = 11 to 25V)	1.0 (V_i= 12.5 to 30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA T_{amb}= 0 to 70°C	-1.1	-0.8	-1	-1	mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz	40	52	60	65	μV
SVR	Supply voltage rejection	f = 120 Hz	54	48	47	47	dB
V_i	Operating input voltage	$I_o \leqslant$ 1.5A	8	10.5	12	13	V
R_o	Output resistance	f = 1 KHz	17	16	17	17	mΩ
I_{sc}	Short circuit current	V_i = 27V	500	500	500	500	mA
I_{scp}	Short circ. peak current		3.5	3.5	3.5	3.5	A

ELECTRICAL CHARACTERISTICS L78S00C (continued)

OUTPUT VOLTAGE			12			15			18			24			Unit
INPUT VOLTAGE (Unless otherwise specified)			19			23			26			33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage		11.5	12	12.5	14.4	15	15.6	17.1	18	18.9	23	24	25	V
		I_o= 1A	11.4 (V_i= 14.5V)	12	12.6	14.25 (V_i= 17.5V)	15	15.75	17 (V_i= 20.5V)	18	19	22.8 (V_i= 27V)	24	25.2	
ΔV_o	Line regulation				240 (V_i= 14.5 to 30V)			300 (V_i= 17.5 to 30V)			360 (V_i= 20.5 to 30V)			480 (V_i= 27 to 38V)	mV
					120 (V_i= 16 to 22V)			150 (V_i= 20 to 26V)			180 (V_i= 22 to 28V)			240 (V_i= 30 to 36V)	
ΔV_o	Load regulation	I_o= 20 mA to 2A			240			300			360			480	mV
I_d	Quiescent current				8			8			8			8	mA
ΔI_d	Quiescent current change	I_o= 20 mA to 1A			0.5			0.5			0.5			0.5	mA
		I_o= 20 mA			1.0 (V_i = 14.5 to 30V)			1.0 (V_i = 17.5 to 30V			1.0 (V_i = 20.5 to 30V)			1.0 (V_i = 27 to 38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5mA T_{amb}= 0 to 70°C			-1			-1			-1			-1.5	mV/°C
e_N	Output noise voltage	B= 10Hz to 100KHz			75			90			110			170	μV
SVR	Supply voltage rejection	f = 120 Hz	47			46			43			42			dB
V_i	Operating input voltage	$I_o \leqslant$ 1.5A	15			18			21			27			V
R_o	Output resistance	f = 1 KHz		18			19			22			28		mΩ
I_{sc}	Short circuit current	V_i = 27V		500			500			500			500		mA
I_{scp}	Short circ. peak current				3.5			3.5			3.5			3.5	A

Fig. 4 - Dropout voltage vs. junction temperature

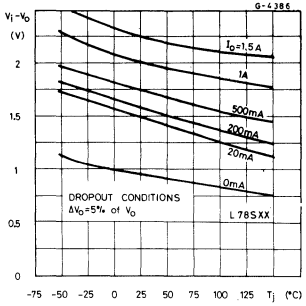


Fig. 5 - Peak output current vs. input/output differential voltage

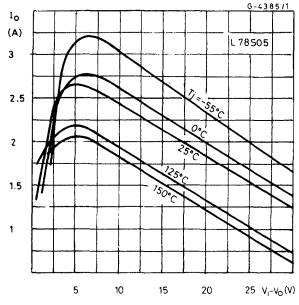


Fig. 6 - Supply voltage rejection vs. frequency

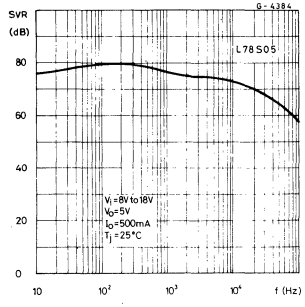


Fig. 7 - Output voltage vs. junction temperature

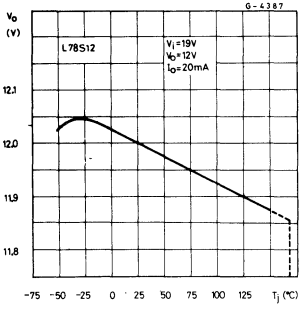


Fig. 8 - Output impedance vs. frequency

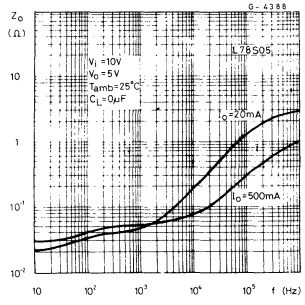


Fig. 9 - Quiescent current vs. junction temperature

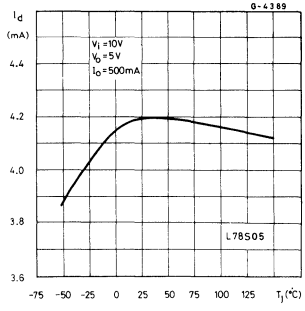


Fig. 10 - Load transient response

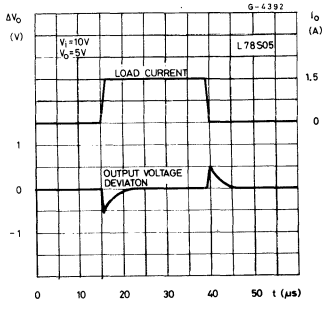


Fig. 11 - Line transient response

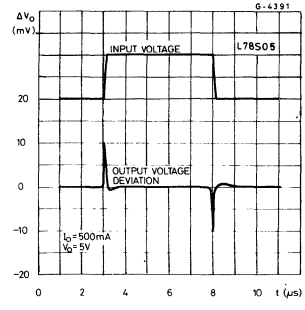
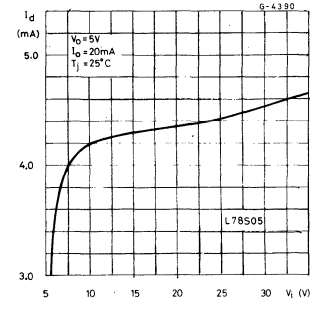
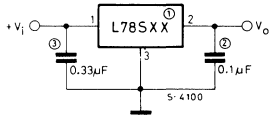


Fig. 12 - Quiescent current vs. input voltage



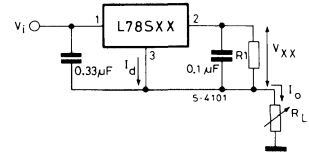
APPLICATION INFORMATION (continued)

Fig. 13 - Fixed output regulator



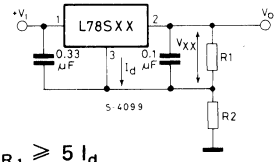
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Fig. 14 - Costant current regulator



$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Fig. 15 - Circuit for increasing output voltage



$$I_{R_1} \geqslant 5\, I_d$$

$$V_o = V_{XX}\ (1 + \frac{R_2}{R_1}) + I_d\, R_2$$

Fig. 16 - Adjustable output regulator (7 to 30V)

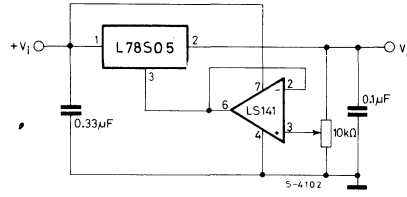
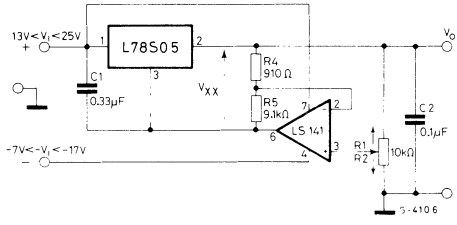
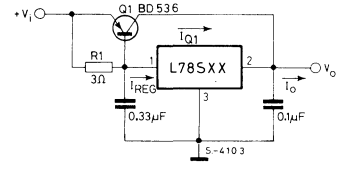


Fig. 17 - 0.5 to 10V regulator



$$V_o = V_{XX}\ \frac{R_4}{R_1}$$

Fig. 18 - High current voltage regulator

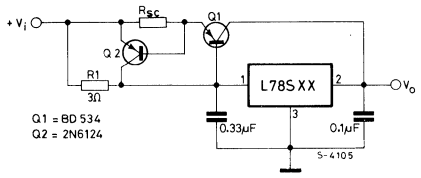


$$R_1 = \frac{V_{BEQ_1}}{I_{REG} - \frac{I_{Q_1}}{\beta_{Q_1}}}$$

$$I_o = I_{REG} + \beta_{Q_1}\ [I_{REG} - \frac{V_{BEQ_1}}{R_1}]$$

APPLICATION INFORMATION (continued)

Fig. 19 - High output current with short circuit protection



$$R_{SC} = \frac{V_{BEQ_2}}{I_{SC}}$$

Fig. 20 - Tracking voltage regulator

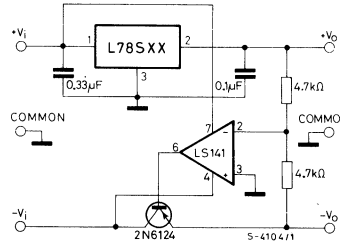
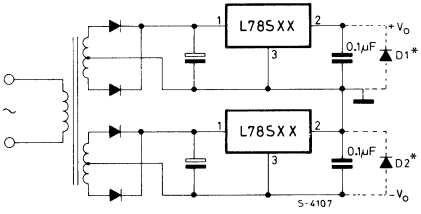


Fig. 21 - Positive and negative regulator



(*) D_1 and D_2 are necessary if the load is connected between $+V_o$ and $-V_o$

Fig. 22 - Negative output voltage circuit

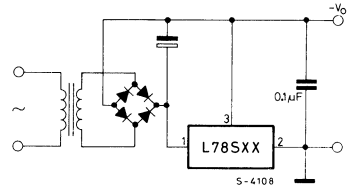


Fig. 23 - Switching regulator

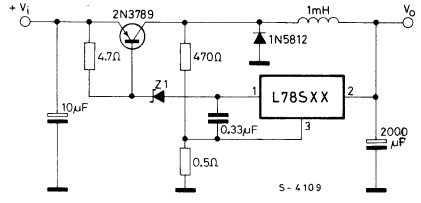
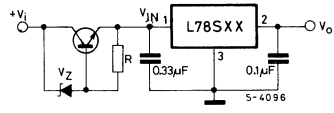


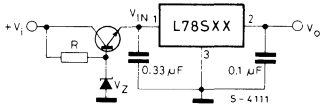
Fig. 24 - High input voltage circuit



$$V_{IN} = V_i - (V_Z + V_{BE})$$

APPLICATION INFORMATION (continued)

Fig. 25 - High input voltage circuit



$$V_{IN} = V_Z - V_{BE}$$

Fig. 26 - High output voltage regulator

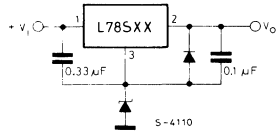
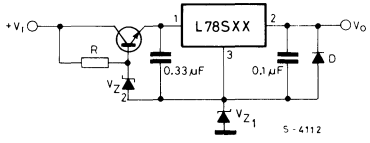
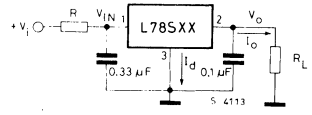


Fig. 27 - High input and output voltage



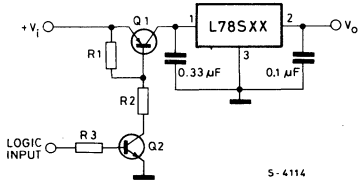
$$V_O = V_{XX} + V_{Z1}$$

Fig. 28 - Reducing power dissipation with dropping resistor



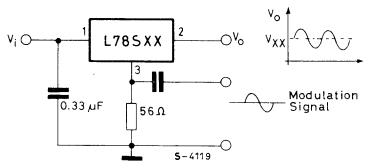
$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{o(max)} + I_{d(max)}}$$

Fig. 29 - Remote shuntdown



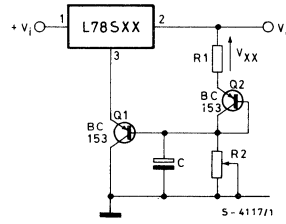
APPLICATION INFORMATION (continued)

Fig. 30 - Power AM modulator oscillator (unity voltage gain, $I_o \leq 1.5A$)



Note: The circuit performs well up to 100 KHz.

Fig. 31 - Adjustable output voltage with temperature compensation

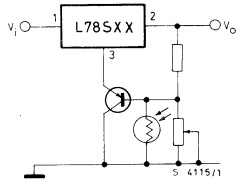


Note: Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_o

$$V_o = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

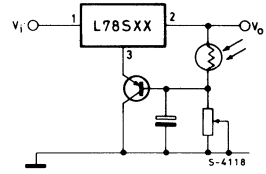
Fig. 32 - Light controllers ($V_{o\ min} = V_{XX} + V_{BE}$)

(a)



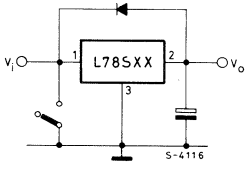
V_o falls when the light goes up

(b)



V_o rises when the light goes up

Fig. 33 - Protection against input short-circuit with high capacitance loads



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

LINEAR INTEGRATED CIRCUITS

L7900 Series

PRELIMINARY DATA

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5A
- OUTPUT VOLTAGES OF -5; -5.2; -8; -12; -15; -18; -20; -24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION

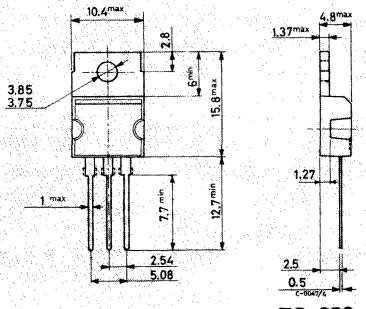
The L7900 series of three-terminal negative regulators is available in TO-220 and TO-3 packages and with several output voltages. They can provide local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the L7800 positive standard series, they are particularly suited for split power supplies. In addition, the -5.2V is also available for ECL system.
If adeguate heatsinking is provided, the L7900 series can deliver an output current in excess of 1.5A. Although designed primarly as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

ABSOLUTE MAXIMUM RATINGS

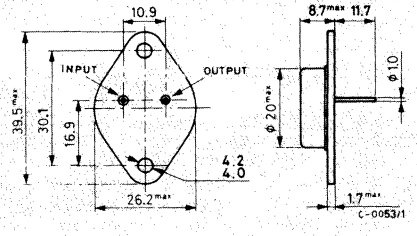
V_i	DC input voltage (for V_o = -5 to -18V)	-35 V
	(for V_o = -20, -24V)	-40 V
I_o	Output current	Internally limited
P_{tot}	Total power dissipation	Internally limited
T_{op}	Operating junction temperature	0 to +150 °C
T_{stg}	Storage temperature	-65 to +150 °C

MECHANICAL DATA

Dimensions in mm



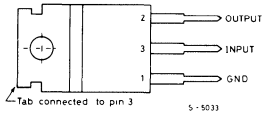
TO-220

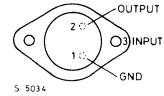


TO-3

L7900 Series

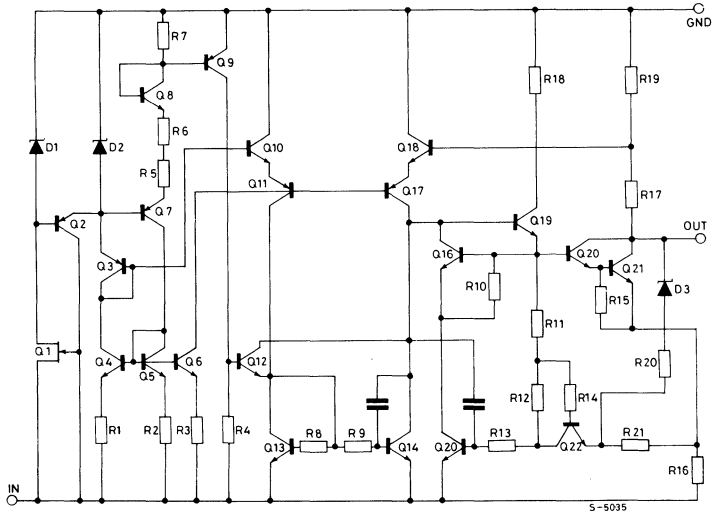
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-220	TO-3	Output Voltage
L7905C	L7905CV	L7905CT	-5V
L7952C	L7952CV	L7952CT	-5.2V
L7908C	L7908CV	L7908CT	-8V
L7912C	L7912CV	L7912CT	-12V
L7915C	L7915CV	L7915CT	-15V
L7918C	L7918CV	L7918CT	-18V
L7920C	L7920CV	L7920CT	-20V
L7924C	L7924CV	L7924CT	-24V

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3 °C/W	4 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS L7900C (C_i = 2.2 μF, C_o = 1 μF, T_j = 0 to 125°C, I_o = 500 mA unless otherwise specified)

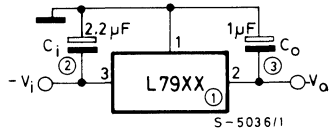
OUTPUT VOLTAGE			-5			-5.2			-8			-12			Unit
INPUT VOLTAGE (Unless otherwise specified)			-10			-10			-14			-19			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j= 25°C	-4.8	-5	-5.2	-5	-5.2	-5.4	-7.7	-8	-8.3	-11.5	-12	-12.5	V
		I_o= 5 mA to 1A P_o < 15W	-4.75	-5	-5.25 (V_i= -8 to -20V)	-4.95	-5.2	-5.45 (V_i= -9 to -21V)	-7.6	-8	-8.4 (V_i= -11.5 to -23V)	-11.4	-12	-12.6 (V_i= -15.5 to -27V)	
ΔV_o	Line regulation	T_j = 25°C			100 (V_i= -7 to -25V)			105 (V_i= -8 to -25V)			160 (V_i= -10.5 to -25V)			240 (V_i= -14.5 to -30V)	mV
					50 (V_i= -8 to -12V)			52 (V_i= -9 to -13V)			80 (V_i= -11 to -17V)			120 (V_i= -16 to -22V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			100			105			160			240	mV
		T_j= 25°C I_o= 250 to 750 mA			50			52			80			120	
I_d	Quiescent current	T_j= 25°C			2			2			2			3	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1.3 (V_i= -8 to -25V)			1.3 (V_i= -9 to -25V)			1 (V_i=-11.5 to -25V)			1 (V_i= -15 to -30V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-0.4			-0.5			-0.6			-0.8		mV/°C
e_N	Output noise voltage	B = 10Hz to 100KHz T_j= 25°C		100			125			175			200		μV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j= 25°C I_o= 1A ΔV_o= 100 mV		2			1.8			1.1			1.1		V
I_{sc}	Short circuit current			2.1			2			1.5			1.5		A
I_{scp}	Short circ. peak current	T_j= 25°C		2.5			2.5			2.5			2.5		A

ELECTRICAL CHARACTERISTICS L7900 (continued)

OUTPUT VOLTAGE			-15			-18			-20			-24			Unit
INPUT VOLTAGE (Unless otherwise specified)			-23			-27			-29			-33			
Parameter		Test conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output voltage	T_j = 25°C	-14.4	-15	-15.6	-17.3	-18	-18.7	-19.2	-20	-20.8	-23	-24	-25	V
		I_o= 5 mA to 1A P_o < 15W	-14.3	-15	-15.7 (V_i=-18.5 to -30V)	-17.1	-18	-18.9 (V_i= -22 to -33V)	-19	-20	-21 (V_i= -24 to -35V)	-22.8	-24	-25.2 (V_i= -27 to -38V)	
ΔV_o	Line regulation	T_j = 25°C			300 (V_i=-17.5 to -30V)			360 (V_i= -21 to -33V)			400 (V_i= -23 to -35V)			480 (V_i= -27 to -38V)	mV
					150 (V_i= -20 to -26V)			180 (V_i= -24 to -30V)			200 (V_i= -26 to -32V)			240 (V_i= -30 to -36V)	
ΔV_o	Load regulation	T_j= 25°C I_o= 5 mA to 1.5A			300			360			400			480	mV
		T_j= 25°C I_o= 250 to 750 mA			150			180			200			240	
I_d	Quiescent current	T_j= 25°C			3			3			3			3	mA
ΔI_d	Quiescent current change	I_o= 5 mA to 1A			0.5			0.5			0.5			0.5	mA
					1 (V_i=-18.5 to -30V)			1 (V_i= -22 to -33V)			1 (V_i= -24 to -35V)			1 (V_i= -27 to -38V)	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift	I_o= 5 mA		-0.9			-1			-1.1			-1		mV/°C
e_N	output noise voltage	B= 10Hz to 100KHz T_j= 25°C		250			300			350			400		μV
SVR	Supply voltage rejection	f = 120 Hz ΔV_i= 10V	54	60		54	60		54	60		54	60		dB
V_{i-o}	Dropout voltage	T_j= 25°C I_o= 1A ΔV_o= 100 mV		1.1			1.1			1.1			1.1		V
I_{sc}	Short circuit current			1.3			1.1			0.9			1.1		A
I_{scp}	Short circ. peak current	T_j= 25°C		2.2			2.2			2.2			2.2		A

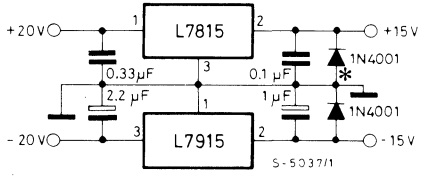
APPLICATION INFORMATION

Fig. 1 - Fixed output regulator



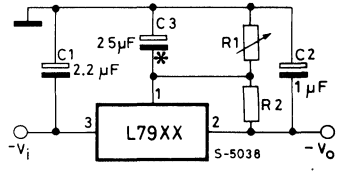
Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. C_i is required if regulator is located an appreciable distance from power supply filter.
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 - Split power supply (± 15V/1A)



* Against potential latch-up problems.

Fig. 3 - Circuit for increasing output voltage



$$V_o \cong V_{xx} \cdot \frac{R1 + R2}{R2} \qquad \frac{V_{xx}}{R2} > 3\,I_d$$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 - High current negative regulator (-5V/4A with 5A current limiting)

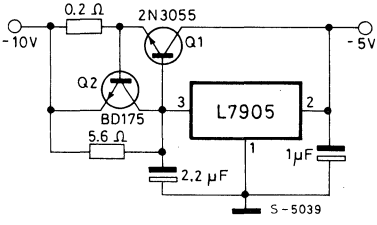
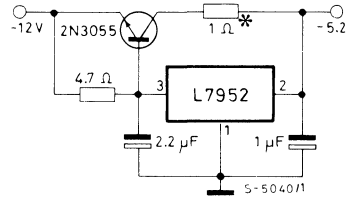


Fig. 5 - Typical ECL system power supply (-5.2V/ 4A)



* Optional dropping resistor to reduce the power dissipated in the boost transistor.

LM117
LM217
LM317

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

1.2V to 37V ADJUSTABLE VOLTAGE REGULATOR

The LM 117/LM 217/LM 317 are monolithic integrated circuits in TO-220 and TO-3 packages intended for use as positive adjustable voltage regulator.
They are designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V range.
The nominal output voltage is selected by means of only a resistive divider, making the device exceptionally easy to use and eliminating the stocking of many fixed voltage regulators.
Their main features are:

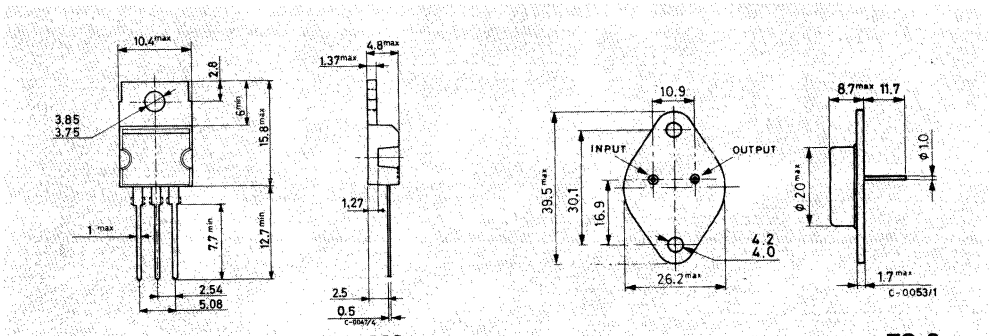
- Output voltage range: 1.2 to 37V
- Output current in excess of 1.5A
- 0.1% line and load regulation
- Floating operation for high voltages
- Complete series of protections: current limiting, thermal shut-down and SOA control.

ABSOLUTE MAXIMUM RATINGS

V_{i-o}	Input-output differential voltage		40 V
I_o	Output current		Internally limited
T_{op}	Operating junction temperature for:	LM 117	-55 to 150 °C
		LM 217	-25 to 150 °C
		LM 317	0 to 125 °C
P_{tot}	Power dissipation		Internally limited
T_{stg}	Storage temperature		-65 to 150 °C

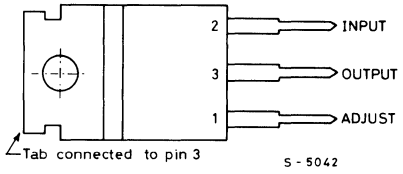
MECHANICAL DATA

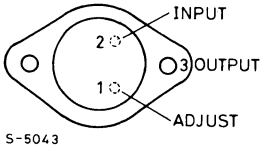
Dimensions in mm



CONNECTION DIAGRAMS AND ORDERING NUMBERS

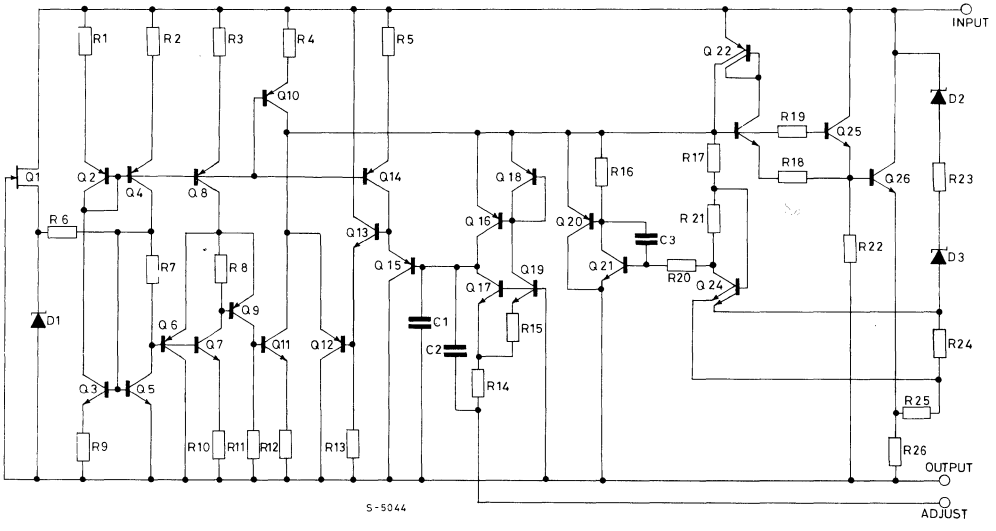
(top views)





Type	TO-220	TO-3
LM 117	—	LM 117K
LM 217	—	LM 217K
LM 317	LM 317T	LM 317K

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-3	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35 °C/W	50 °C/W

ELECTRICAL CHARACTERISTICS (V_i-V_o = 5V, I_o = 500 mA, unless otherwise specified)

Parameter		Test conditions		LM 117/LM 217			LM 317			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
ΔV_o	Line regulation	V_i-V_o= 3 to 40V	T_j= 25°C		0.01	0.02		0.01	0.04	%/V
					0.02	0.05		0.02	0.07	
ΔV_o	Load regulation	$V_o \leqslant$ 5V, I_o= 10mA to 1.5A	T_j= 25°C		5	15		5	25	mV
					20	50		20	70	
		$V_o \geqslant$ 5V, I_o= 10 mA to 1.5A	T_j= 25°C		0.1	0.3		0.1	0.5	%
					0.3	1		0.3	1.5	
I_{ADJ}	Adjustment pin current				50	100		50	100	μA
ΔI_{ADJ}	Adjustment pin current	V_i-V_o= 2.5 to 40V, I_o= 10 mA to 1.5A			0.2	5		0.2	5	μA
V_{REF}	Reference voltage (between pin 3 and pin 1)	V_i-V_o= 3 to 40V, I_o= 10 mA to 1.5A		1.2	1.25	1.3	1.2	1.25	1.3	V
$\frac{\Delta V_o}{V_o}$	Output voltage temperature stability				1			1		%
$I_{o\,min}$	Minimum load current				3.5	5		3.5	10	mA
$I_{o\,max}$	Maximum load current	V_i-$V_o \leqslant$ 15V		1.5	2.2		1.5	2.2		A
		V_i-V_o= 40V			0.4			0.4		
e_N	Output noise (percentage of V_o)	T_i= 25°C, 10Hz to 10KHz			0.003			0.003		%
SVR	Supply voltage rejection (*)	T_j= 25°C, f = 120 Hz	C_{ADJ}= 0		65			65		dB
			C_{ADJ}= 10 μF	66	80		66	80		

(*) C_{ADJ} is connected between pin 1 and ground.

Note — Unless otherwise specified the above specs, apply over the following conditions: LM 117 T_j= -55 to 150°C; LM 217 T_j = -25 to 150°C; LM 317 T_j = 0 to 125°C.

Fig. 1 - Output current vs. input-output differential voltage

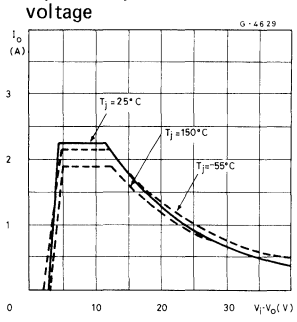


Fig. 2 - Dropout voltage vs. junction temperature

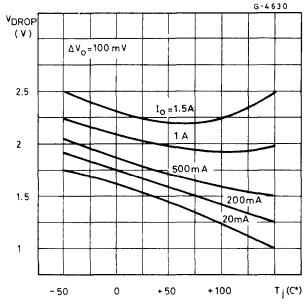
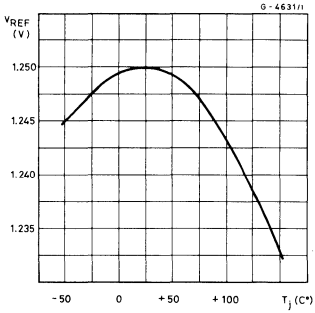


Fig. 3 - Reference voltage vs. junction temperature

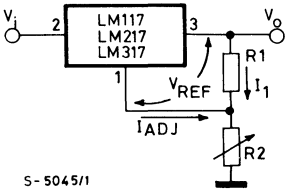


APPLICATION INFORMATION

The LM 117/LM 217/LM 317 provides an internal reference voltage of 1.25V between the output and adjustment terminals. This is used to set a constant current flow across an external resistor divider (see fig. 4), giving an output voltage V_o of:

$$V_o = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\ R2$$

Fig. 4 - Basic adjustable regulator



The device was designed to minimize the term I_{ADJ} (100 μA max) and to maintain it very constant with line and load changes. Usually, the error term I_{ADJ} · R2 can be neglected. To obtain the previous requirement, all the regulator quiescent current is returned to the output terminal, imposing a minimum load current condition. If the load is insufficient, the output voltage will rise.

Since the LM 117/LM 217/LM 317 is a floating regulator and "sees" only the input-to-output differential voltage, supplies of very high voltage with respect to ground can be regulated as long as the maximum input-to-output differential is not exceeded. Furthermore, programmable regulator are easily obtainable and, by connecting a fixed resistor between the adjustment and output, the device can be used as a precision current regulator.

In order to optimise the load regulation, the current set resistor R1 (see fig. 4) should be tied as close as possible to the regulator, while the ground terminal of R2 should be near the ground of the load to provide remote ground sensing.

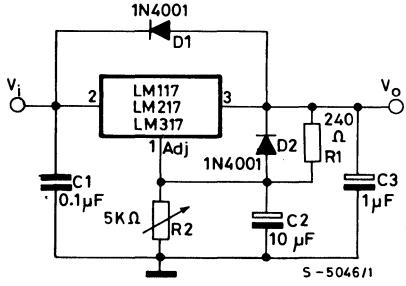
No external capacitors are required, but performance may be improved with added capacitance as follows:

- An input bypass capacitor of 0.1 μF.
- An adjustment terminal to ground 10 μF capacitor to improve the ripple rejection of about 15 dB (C_{ADJ}).
- An 1 μF tantalum capacitor on the output to improve transient response.

APPLICATION INFORMATION (continued)

In additional to external capacitors, it is good practice to add protection diodes, as shown in fig. 5.

Fig. 5 - Voltage regulator with protection diodes.



D1 protects the device against input short circuit, while D2 protects against output short circuit for capacitors discharging.

Fig. 6 - Slow turn-on 15V regulator

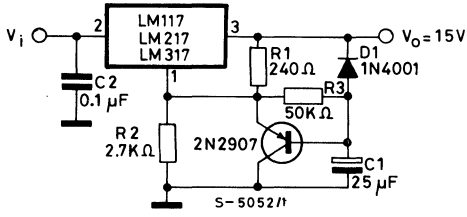
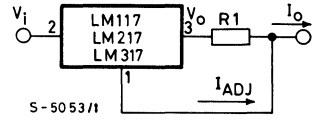


Fig. 7 - Current regulator



$$I_o = \frac{V_{ref}}{R1} + I_{ADJ} \cong \frac{1.25V}{R1}$$

(I_o = 10 mA to 1.5A)

Fig. 8 - 5V electronic shut-down regulator

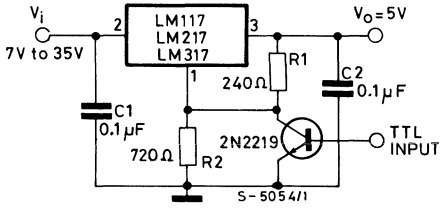
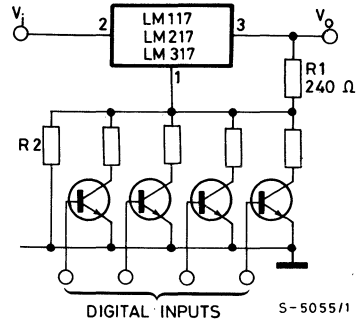


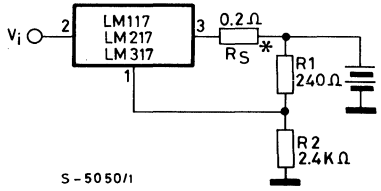
Fig. 9 - Digitally selected outputs



(R2 sets maximum V_o)

APPLICATION INFORMATION (continued)

Fig. 10 - Battery charger (12V).

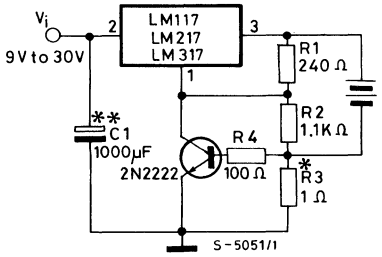


* R_S sets output impedance of charger

$$Z_o = R_s\,(1 + \frac{R2}{R1})$$

Use of R_S allows low charging rates with fully charged battery.

Fig. 11 - Current limited 6V charger.



* R3 sets peak current (0.6A for 1Ω).
** C1 recommended to filter out input transients.

LM324
LM324A
LM2902

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

LOW POWER QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT POWER SUPPLY
- VERY LOW POWER CONSUMPTION
- INPUT COMMON-MODE RANGE INCLUDING GROUND
- LARGE DC VOLTAGE GAIN (100 dB)

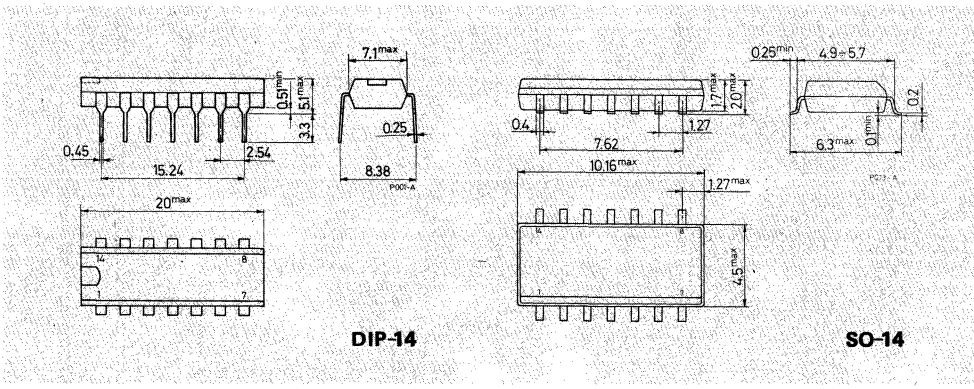
The LM 324 consists of four indipendent, high gain, internally frequency compensated opamps specifically designed to operate from a single power supply over a wide range of voltages. Both in split and in single supply the current drain is independent of the magnitude of the power supply voltage.
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operating from only a single power supply voltage.
The LM 324 is available in a standard 14-lead dual in-line plastic package and in a 14-lead micropackage version for thick or thin film hybrid circuits.

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		32	V
V_i	Input voltage (single supply)		-0.3 to 26	V
V_i	Differential input voltage		32	V
P_{tot}	Total power dissipation		400	mW
T_{op}	Operating temperature for :	**LM 2902**	0 to 70	°C
		LM 324	-25 to 85	°C
		LM 324A	-55 to 125	°C
T_{stg}	Storage temperature		-65 to 150	°C

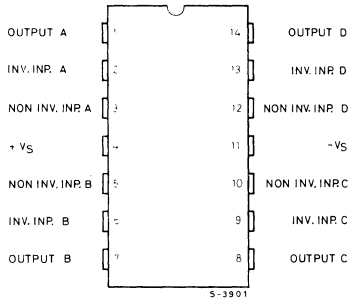
MECHANICAL DATA

Dimensions in mm



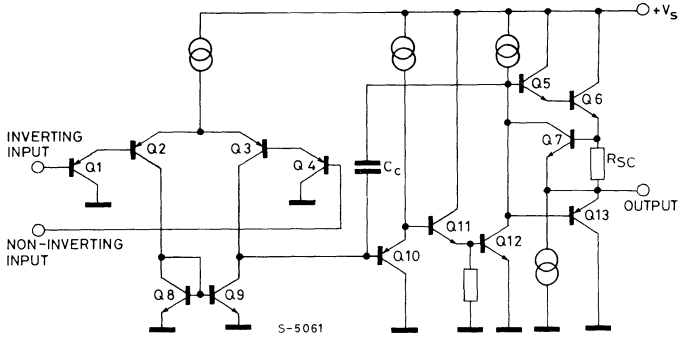
DIP-14 **SO-14**

CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	DIP-14	SO-14
LM 324	LM 324N	LM 324CM
LM 324A	LM 324AN	–
LM 2902	LM 2902N	LM 2902CM

SCHEMATIC DIAGRAM
(one section)



THERMAL DATA

			DIP 14	SO 14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200 °C/W	200 °C/W*

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

LM324
LM324A
LM2902

ELECTRICAL CHARACTERISTICS (V_s = +5V, T_{amb} = -55 to 125°C for the LM 324A, T_{amb} = -25 to 85°C for the LM 324 and T_{amb} = 0 to 70°C for the LM 2902, unless otherwise specified)

Parameter		Test conditions		LM 324			LM 324A			LM 2902			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_S	Supply current	$R_L = \infty$	V_s = 30V		1.5	3		1.5	3		1.5	3	mA
					0.7	1.2		0.7	1.2		0.7	1.2	
I_b	Input bias current	T_{amb} = 25°C			45	250		45	100		45	250	nA
						500			200			500	
V_{os}	Input offset voltage	R_g = 0 V_s = 5V to 30V	T_{amb} = 25°C		± 2	± 7		± 2	± 3		± 2	± 7	mV
						± 9			± 5			± 10	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 0			7			7	30		7		µV/°C
I_{os}	Input offset current	T_{amb} = 25°C			± 5	± 50		± 5	±30		± 5	± 50	nA
						±150			±75			±200	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift				10			10	300		10		pA/°C
I_{sc}	Output short circuit to ground current	T_{amb} = 25°C (*)			40	60		40	60		40	60	mA
G_v	Large signal open loop voltage gain	V_s = 15V $R_L \geqslant$ 2 KΩ	T_{amb} = 25°C	88	100		88	100			100		dB
				83			83			83			
	Input common-mode voltage range	V_s = 30V	T_{amb} = 25°C	0		V_s-1.5	0		V_s-1.5	0		V_s-1.5	V
				0		V_s-2	0		V_s-2	0		V_s-2	
V_o	Output voltage swing	T_{amb} = 25°C	R_L = 2 KΩ			V_s-1.5			V_s-1.5				V
			$R_L \geqslant$ 10 KΩ									V_s-1.5	
		V_s = 30V	R_L = 2 KΩ	26			26			22			V
			$R_L \geqslant$ 10 KΩ	27	28		27	28		23	24		
$V_{o\ sat}$	Output saturation voltage to ground	$R_L \leqslant$ 10 KΩ			5	20		5	20		5	100	mV
CMR	Common mode rejection	T_{amb} = 25°C		65	70		65	85		50	70		dB
SVR	Supply voltage rejection	T_{amb} = 25°C		65	70		65	100		50	70		dB
CS	Channel separation	f = 1 KHz to 20 KHz T_{amb} = 25°C (Input referred)			120			120			120		dB
I_o^+	Output source current	V_s = 15V V_i^+ = 1V V_i^- = 0V	T_{amb} = 25°C	20	40		20	40		20	40		mA
				10	20		10	20		10	20		
I_o^-	Output sink current	V_i^+ = 0V V_i^- = 1V V_o = 200 mV	T_{amb} = 25°C	12	50		12	50					µA
		V_i^- = 1V V_i^+ = 0V V_s = 15V	T_{amb} = 25°C	10	20		10	20		10	20		mA
				5	8		5	8		5	8		

(*) Short circuits from the output to positive supply voltage can cause excessive heating and eventual destruction. The maximum output current is 40 mA typ. independent of the magnitude of V_s. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Fig. 1 - Supply current vs. supply voltage

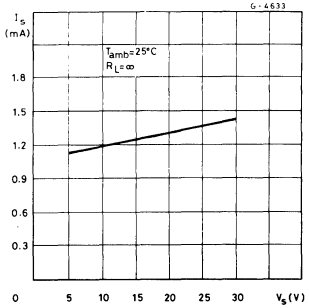


Fig. 2 - Input voltage range vs. supply voltage

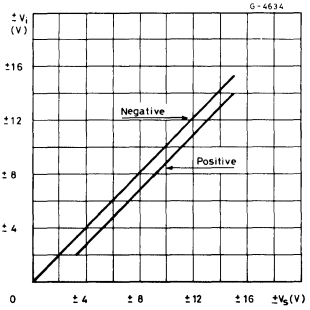


Fig. 3 - Output short circuit current vs. ambient temperature

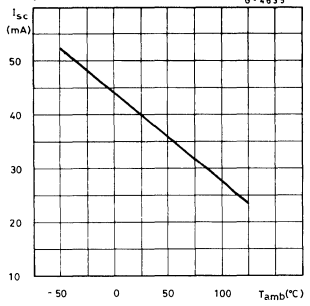


Fig. 4 - Open loop frequency response

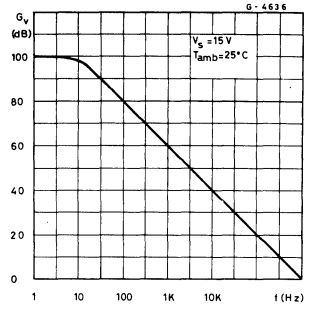


Fig. 5 - Large signal frequency response

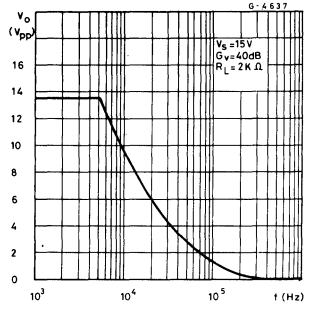
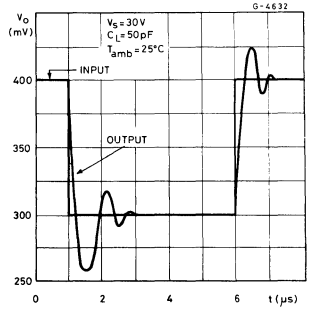


Fig. 6 - Voltage follower pulse response (small signal)



APPLICATION INFORMATION

The LM 324 can operate with a single power supply voltage, has true-differential inputs and remains in the linear mode with an input common-mode voltage of 0V. The four included op amps work over a wide range of power supply voltage with little change in performance characteristics. At 25°C operation is possible down to a minimum supply voltage of 2.3V.

The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_s-1.5V, but either or both inputs can go to +32V without damage.

If the voltage at any of the input leads is driven negative ($V_{in} < -0.3V$), the collector-base junction of the input PNP transitor becomes forward biased and thereby acts as an input diode clamps (max current: 50 mA). In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This can cause the output voltage to go to the positive supply voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns positive ($V_{in} > -0.3V$).

The output stage design allows the amplifiers to both source and sink large output currents.

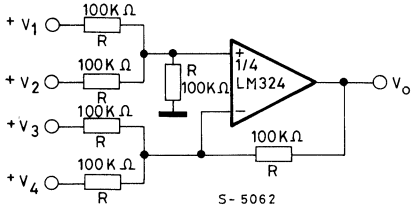
Therefore both NPN and PNP external current boost transistors can be used to extend the power capa-

APPLICATION INFORMATION (continued)

bility of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperature. **Putting direct short-circuits on more than one amplifier at a time, the total IC power dissipation will increase to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers.** The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.
The circuits presented in the following section emphasize operation on a single power supply voltage. If split supplies are used, all the standard op amps configuration can be realised.

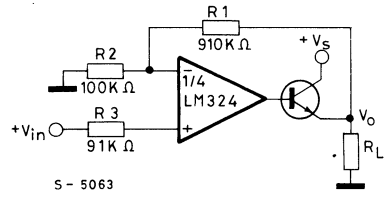
TYPICAL SINGLE SUPPLY APPLICATION CIRCUITS (V_s = 5V)

Fig. 7 - DC summing amplifier



where: $V_o = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2)' \geq (V_3 + V_4)$ to keep $V_o > 0V$

Fig. 8 - Power amplifier



V_o= 0V for V_{IN}= 0V
G_V= 20 dB

Fig. 9 - LED driver

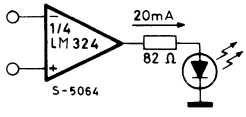


Fig. 10 - Lamp driver

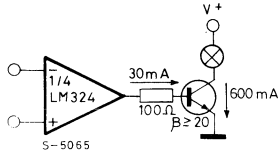
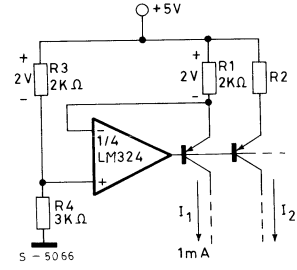


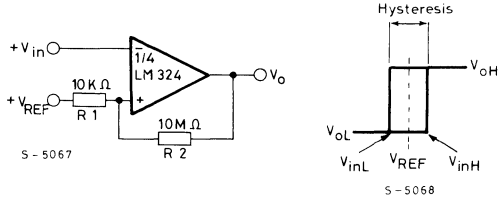
Fig. 11 - Fixed current sources



$I_2 = \left(\frac{R1}{R2}\right) I_1$

TYPICAL SINGLE SUPPLY APPLICATION CIRCUITS (continued)

Fig. 12 - Comparator with Hysteresis

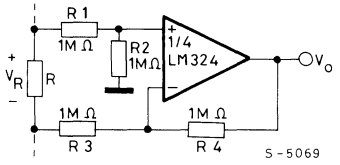


$$V_{in\,L} = \frac{R1}{R1+R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{in\,H} = \frac{R1}{R1+R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$\text{Hysteresis} = \frac{R1}{R1+R2}(V_{OH} - V_{OL})$$

Fig. 13 - Ground referencing a differential input signal



$$V_O = V_R$$

Fig. 14 - Driving TTL

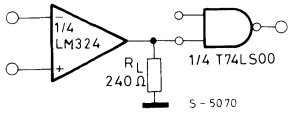


Fig. 15 - Squarewave oscillator

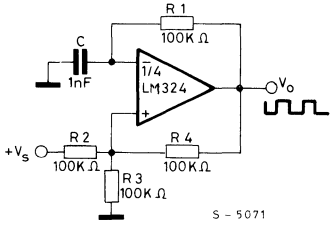
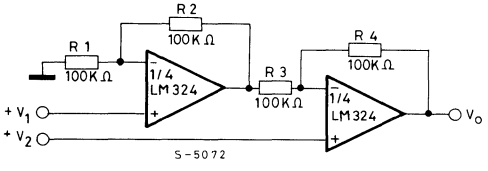


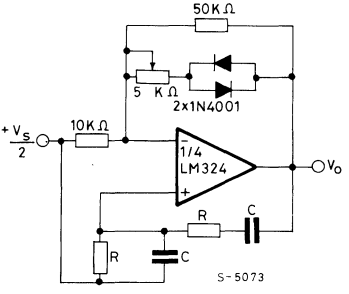
Fig. 16 - High input Z, DC differential amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V2 - V1)$$

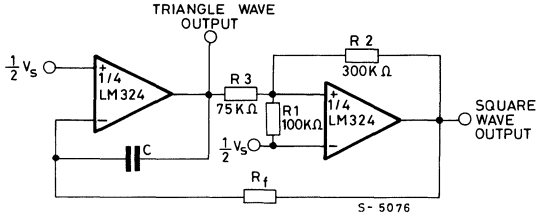
Fig. 17 - Wien bridge oscillator



$$f_o = \frac{1}{2\pi RC}$$

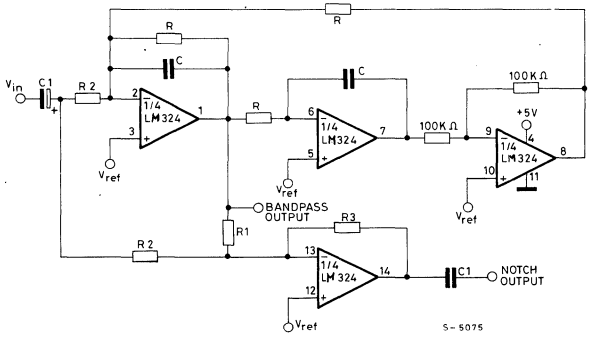
TYPICAL SINGLE SUPPLY APPLICATION CIRCUITS (continued)

Fig. 18 - Function generator



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \therefore \quad R3 = \frac{R2\ R1}{R2 + R1}$$

Fig. 19 - Bi-Quad filter



$f_o = \frac{1}{2\pi\ RC}$; R1= QR; R2= $\frac{R1}{G_{BP}}$;

$V_{ref} = \frac{1}{2}\ V_s$; R3= G_N R2; C1= 10C

Example:

f_o = 1 KHz	R = 160 KΩ
Q = 10	C = 1 nF
G_{BP}= 1	R1= 1.6 MΩ
G_N= 1	R2= 1.6 MΩ
	R3= 1.6 MΩ

Where: G_{BP}= Center Frequency Gain
G_N = Passband Notch Gain

LINEAR INTEGRATED CIRCUITS

LM 339
LM 339A

PRELIMINARY DATA

QUAD VOLTAGE COMPARATOR

The LM 339 and the LM 339A are monolithic integrated circuits in a 14-lead dual in-line plastic package and in a 14-lead micropackage. They consists of four independent precision voltage comparators and are specially designed to offer a versatility as high as possible; application areas include limit comparators, A/D converters, waveforms generators, high voltage logic gates and so on. Furthermore, the open collector output stage provides easy interfacing with all types of logic circuitry.
The LM 339/LM 339A main features are:

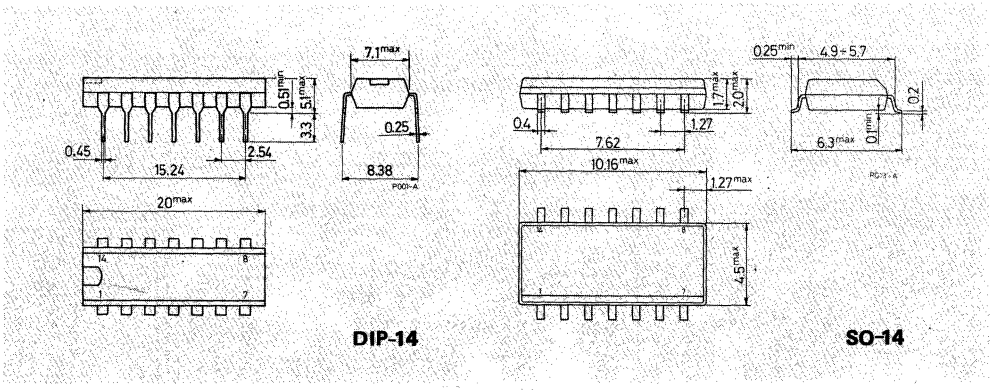
- Wide supply range (2 to 36V)
- **Single or split supply operation**
- Very low current consumption (0.8 mA, regardless of supply voltage)
- Ground input compatibility
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Output short circuit to ground continuous

ABSOLUTE MAXIMUM RATINGS

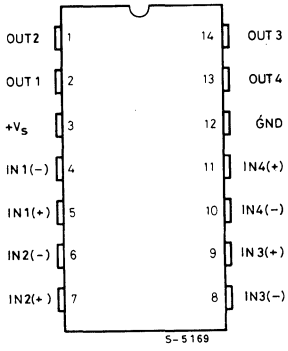
V_s	Supply voltage	± 18 or +36	V
V_l	Input voltage range	-0.3 to 36	V
V_i	Differential input voltage	36	V
I_i	Input current ($V_{in} < -0.3\ V_{dc}$)	50	mA
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	600	mW
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage and junction temperature	-65 to 150	°C

MECHANICAL DATA

Dimensions in mm

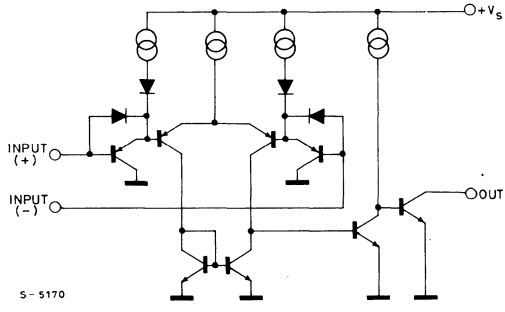


CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	DIP14	SO-14
LM 339	LM 339N	LM 339CM
LM 339A	LM 339AN	–

SCHEMATIC DIAGRAM
(each section)



THERMAL DATA

			DIP-14	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200 °C/W	200 °C/W*

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s = +5V for the LM 339; V_s = +15V for the LM 339A; T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions		LM 339A			L339			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	At out.switch point; $V_o \cong 1.4V$; $R_g = 0$ $V_{REF} = 1.4\ V_{dc}$			± 1	± 2		± 2	± 5	mV
			T_{amb}= 0 to 70°C			± 4			± 9	
I_b	Input bias current (1)	Output in linear range			25	250		25	250	nA
			T_{amb}= 0 to 70°C			400			400	
I_{os}	Input offset current				± 5	±50		± 5	±50	nA
			T_{amb}= 0 to 70°C			±150			±150	
	Input Common-Mode voltage range (2)			0		V_s-1.5	0		V_s-1.5	V
			T_{amb}= 0 to 70°C	0		V_s-2	0		V_s-2	
I_s	Supply current	$R_L = \infty$			0.8	2		0,8	2	mA
G_v	Voltage gain	$R_L \geq 15\ K\Omega$		94	106			106		dB
	Large signal response time	V_{IN}= TTL logic swing; V_{REF}= +1.4V; R_L= 5.1 KΩ V_{RL}= 5V			300			300		nsec
	Response time (3)	V_{RL}= 5V; R_L= 5.1 KΩ			1.3			1.3		µsec
I_o	Output sink current	$V_{IN(-)} \geq 1V$; $V_{IN(+)}$= 0V; $V_o \leq 1.5V$		6	16		6	16		mA
V_{sat}	Output saturation voltage	$V_{IN(-)} \geq 1V$ $V_{IN(+)}$= 0V $I_{sink} \leq 4$ mA			250	500		250	500	mV
			T_{amb}= 0 to 70°C			700			700	
$I_{o\ leak}$	Output leakage current	$V_{IN(+)} \geq 1V$ $V_{IN(-)}$ = 0V	V_o = 5V		0.1			0.1		nA
			T_{amb}= 0 to 70°C V_o= 30V			1			1	µA
	Differential input voltage	All $V_{IN} \geq 0V$ (or $-V_s$ if split supply is used); T_{amb}= 0 to 70°C				36			36	V

Notes: (1) The direction of the current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(2) If either input of any comparators goes more negative than 0.3V below ground, a parasitic transistor turns on causing high input current and possible faulty outputs. This condition is not destructive providing the input current is limited to less than 50 mA.

(3) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 nsec can be obtained.

APPLICATION INFORMATION

The LM 339 includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.
To minimize this problem, PC board layout should be designed to reduce stray input-output coupling; reducing the input resistors to less than 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.
It is good design practice to ground all unused pins.
The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than -0.3V should not be used: an input clamping diode can be used as protection.

The output of the LM 339 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.
The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

Fig. 1 - Basic comparator

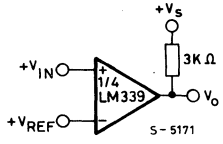


Fig. 2 - Non-inverting comparator with Hysteresis

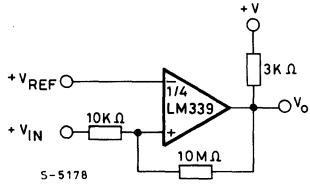


Fig. 3 - Inverting comparator with Hysteresis

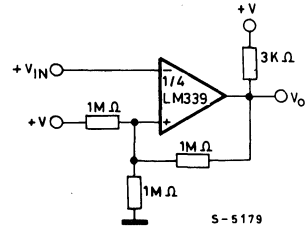


Fig. 4 - Driving C/MOS

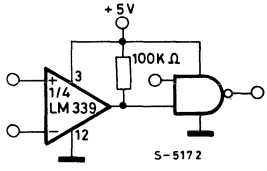
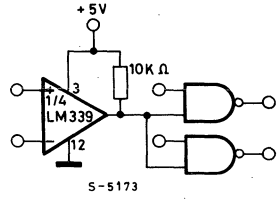


Fig. 5 - Driving TTL



APPLICATION INFORMATION (continued)

Fig. 6 - AND gate

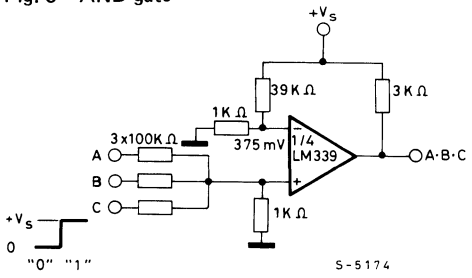


Fig. 7 - OR gate

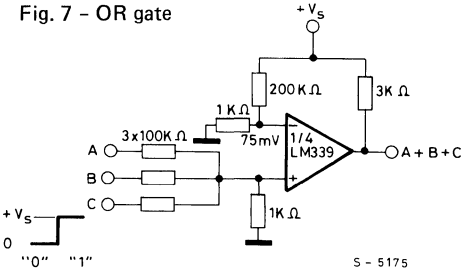


Fig. 8 - Large fan-in AND gate

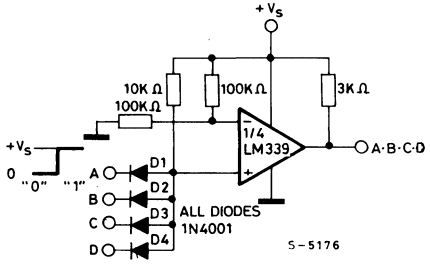


Fig. 9 - Squarewave oscillator

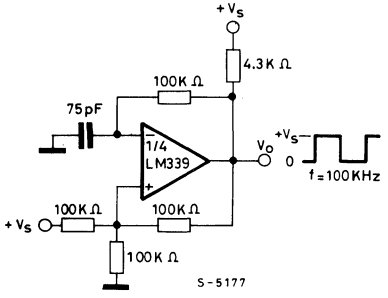


Fig. 10 - Time delay generator

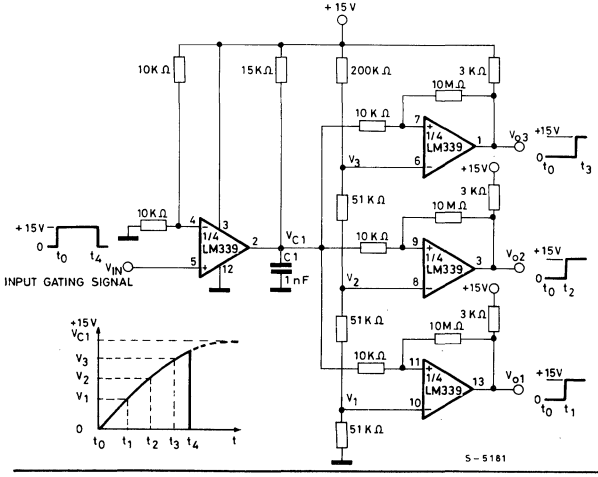
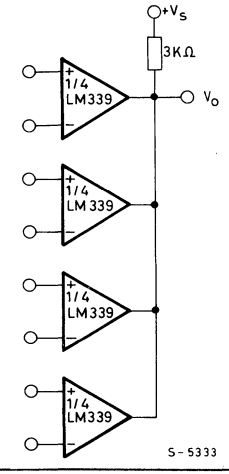


Fig. 11 - ORing the outputs



APPLICATION INFORMATION (continued)

Fig. 12 - Peak audio level display

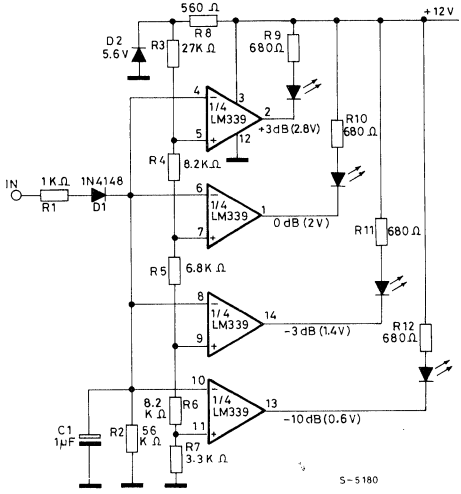


Fig. 13 - PC Board and component layout of the circuit of fig. 12

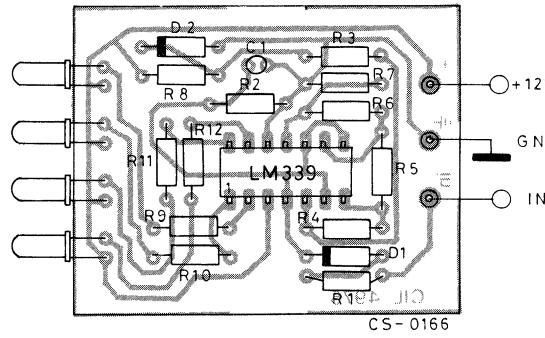
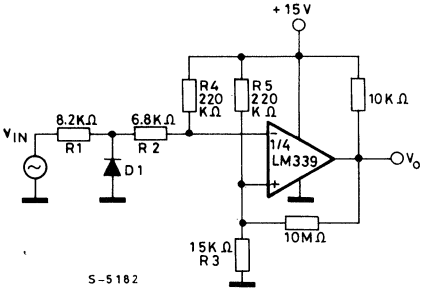


Fig. 14 - Zero crossing detector (single supply)



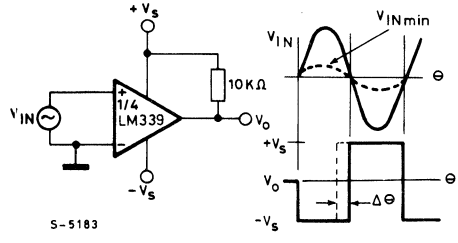
D1 prevents input from going negative by more than 0.6V:

$$R1 + R2 = R3$$

$$R3 \leqslant \frac{R5}{10}$$ for smaller error in zero crossing

Fig. 15 - Zero crossing detector (split supplies)

$V_{INmin} \approx 0.4V$ peak for 1% phase distortion ($\Delta\ \theta$)



LINEAR INTEGRATED CIRCUIT

LS025

BALANCED MODULATOR

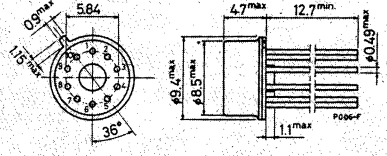
- SINGLE OR DUAL SUPPLY OPERATION
- LOW POWER CONSUMPTION
- LOW CARRIER LEAKAGE
- LOW DISTORTION
- LOW NOISE

The LS025 is a low noise linear integrated circuit, intended for use as a channel modulator and demodulator in FDM telephone equipments and as analogue AC and DC multiplier in industrial and professional applications. It features low quiescent power consumption, low distortion and intermodulation. It shows a typical carrier leakage better than 85 dB throughtout the audio bandwidth. The LS025 is available in TO-100 metal case, while the hermetic gold chip (8000 series) is available in SO-14 (14-lead plastic micropackage). This last version is particularly suitable for professional and telecom applications wherever very high MTBF are required.

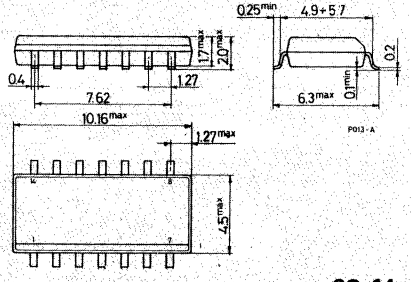
ABSOLUTE MAXIMUM RATINGS		TO-100	μpackage
V_s	Supply voltage	30 V	
ΔV_i	Differential input voltage	± 5 V	
T_{op}	Operating temperature	-25 to 85 °C	
P_{tot}	Power dissipation at T_{amb} = 70 °C	520 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C

MECHANICAL DATA

Dimensions in mm

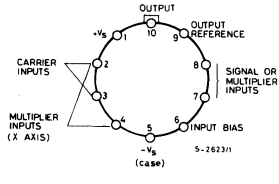


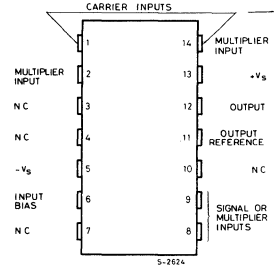
TO-100



SO-14

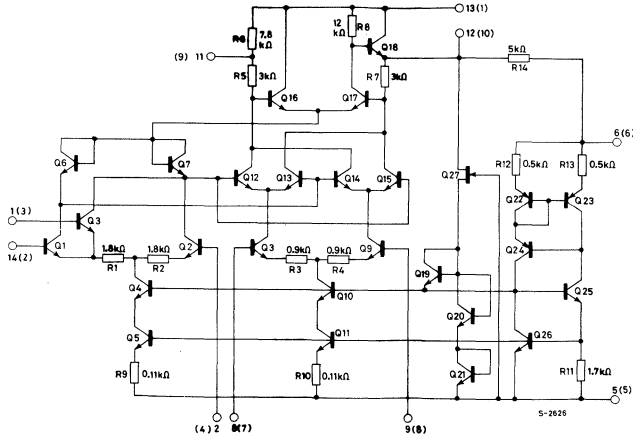
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-100	SO-14
LS 025	LS 025T	LS025M
LS 8025		LS 8025M

SCHEMATIC DIAGRAM
(The pin numbers refer to the μ package version, while the numbers in brackets refer to the TO-100 version)



THERMAL DATA

			TO-100	SO-14
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	155 °C/W	200* °C/W

* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

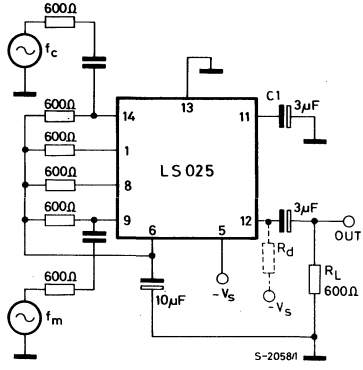
ELECTRICAL CHARACTERISTICS (Referred to the circuit of fig. 1; T_{amb}= 25°C unless otherwise specified. The pins correspond to the μpackage version)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range		-12		-30	V
I_s	Supply current			2	2.5	mA
I_b	Input bias current	Pins 14-1 Pins 14-2 Pins 8-9		0.7 0.7 1.4	2 2 4	μA μA μA
ΔI	Input offset current	Pins 14-1 Pins 14-2 Pins 8-9		50 70 100		nA nA nA
	Positive input common mode voltage			4.5		V
	Negative input common mode voltage			-8		V
V_o	DC output voltage (pin 12)		-3.2	-3.8	-4.6	V
ΔV_o	Differential output voltage (pins 11-12)			25	100	mV
V_{ref}	Input biasing reference voltage (pin 6)			-7.5		V
R_i	Input resistance	Pins 14-1 Pins 14-2 Pins 8-9		30 300 150		kΩ kΩ kΩ
R_o	Output resistance	f = 1 kHz		3	10	Ω
V_o	Output voltage swing		1	1.3		Vpp
CMR	Common mode rejection	CM signal (pins 14-1) V = 700 mVrms f_1= 10 kHz Diff. signal (pins 8-9) V = 350 mVrms f_2= 40 kHz		98		dB
		CM signal (pins 14-2) V = 700 mVrms f_1= 10 kHz Diff. signal (pins 8-9) V = 350 mVrms f_2= 40 kHz		86		dB
		CM signal (pins 8-9) V = 350 mVrms f_1= 10 kHz Diff. signal (pins 14-1) V = 175 mVrms f_2= 40 kHz		80		dB
SVR	Positive supply voltage rejection	f = 1 kHz		33		dB
SVR	Negative supply voltage rejection			80		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
K	Scale factor			3.2		V^{-1}
G_c	Conversion gain		4.5	5	5.5	dB
ΔG_c	Conversion gain change	T_{amb}= 10 to 50°C		± 0.1		dB
	Carrier leakage	V_m= 0	-35	-50		dBv
$\frac{V_{fm}}{V_{(f_c \pm f_m)}}$	Modulating signal leakage		-35	-50		dBmo
$\frac{V_{(2f_m)}}{V_{(f_c \pm f_m)}}$	2nd harmonic modulating signal leakage			-75		dBmo
$\frac{V_{(f_c \pm 2f_m)}}{V_{(f_c \pm f_m)}}$	2nd harmonic distortion		-60	-75		dBmo
$\frac{V_{2(f_c \pm f_m)}}{V_{(f_c \pm f_m)}}$	2nd harmonic distortion		-55	-80		dBmo
$\frac{V_{(f_c \pm 3f_m)}}{V_{(f_c \pm f_m)}}$	3rd harmonic distortion		-60	-79		dBmo
	Low frequency thermal noise	V_m= 0 f = 1 kHz B = 100 Hz	-115	-125		dBv
	High frequency thermal noise	V_m= 0 f = 30 kHz B = 100 Hz		-127		dBv

Fig. 1 - Test and application circuit of modulator with single supply voltage



Working conditions

V_s = -20V
f_c = 130 kHz
f_m = 25 kHz
V_o = -15 dBv ($f_c \pm f_m$)
V_c = -13 dBv
$R_L \equiv$ 600 Ω

Fig. 2 - Carrier leakage vs. modulation signal input offset

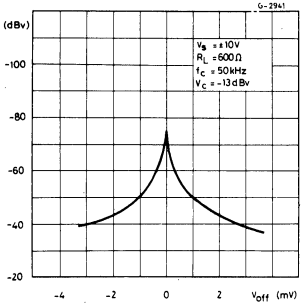


Fig. 3 - Conversion gain vs. frequency

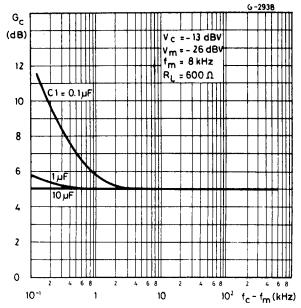


Fig. 4 - Distortion vs. output level

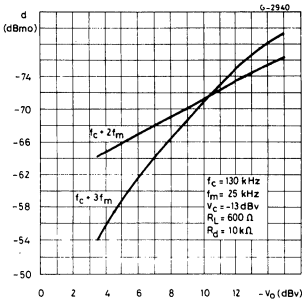


Fig. 5 - Carrier leakage adjustment circuit for system with two supply voltages

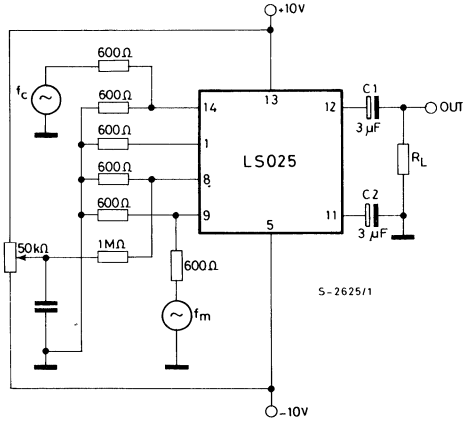
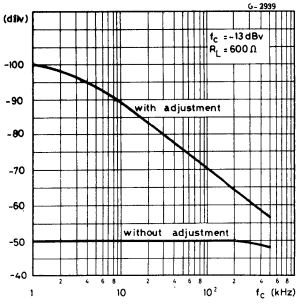
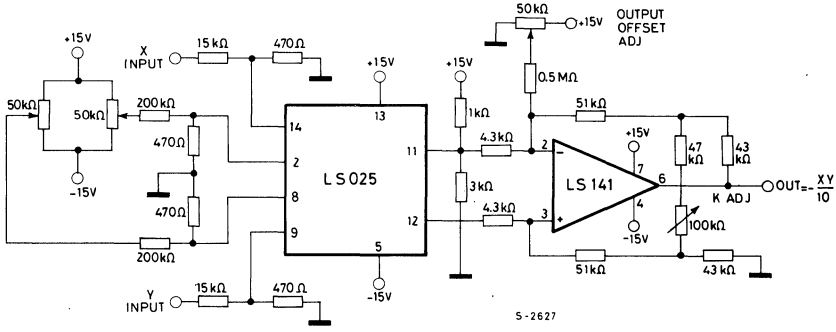


Fig. 6 - Carrier leakage vs. frequency



APPLICATION INFORMATION

Fig. 7 - DC multiplier



Application diagram of DC multiplier, have a scale factor K = 0.1. Typical linearity and leakage errors are less than 1%.
The input voltage range is ± 10V.

Definition of units

dBm : power level ($10 \lg \frac{P_2}{P_1}$) is expressed in dBm when P_1 is 1 mW, therefore 0 dBm= 1 mW.

dBmo : the power is expressed in dBmo when referred to an established power level in the circuit, generally the output signal level.
e.g.: if the output level is -15 dBm and this level is chosen as reference, then 0 dBmo = -15 dBm; if another signal, i.e. the distortion measured at the same point of the circuit, is -90 dBm, then the distortion is -75 dBmo.

dBv : $20 \lg \frac{V_2}{V_1}$ when V_1= 775 mVrms.

Definition of terms

Common mode rejection ratio : $CMR = 20 \lg \frac{V_{CM}\, G}{V_o}$

with G = Conversion gain with specified circuit conditions
V_{CM} = Common mode signal level
V_o = Output signal level at frequency = $f_2 \pm f_1$

Scale factor : $K = \frac{V_o}{V_x \cdot V_y}$

with V_x = voltage input (pins 14 - 2)
V_y = voltage input (pins 8 - 9)

APPLICATION INFORMATION (continued)

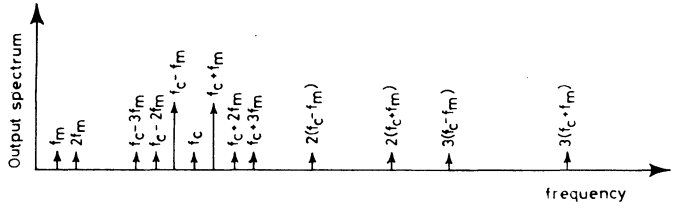
Conversion gain : $G_c = 20 \lg \frac{V_o (f_c \pm f_m)}{V_i (f_m)}$

Carrier leakage : is defined as the output voltage at carrier frequency with only the carrier applied to the input (modulating voltage = 0)

Modulating signal leakage : is defined as the output voltage, at modulating frequency, referred to fundamental carrier sidebands

$$M.S.L. = 20 \lg \frac{V_o (f_m)}{V_o (f_c \pm f_m)}$$

Output spectrum vs. frequency



f_c = carrier fundamental (leakage)
f_m = mod. sig. (leakage)
nf_m = harmonic modulating signal (leakage)
$f_c \pm f_m$ = fundamental carrier sidebands
$f_c \pm nf_m$ = fundamental carrier sideband harmonics
$n (f_c \pm f_m)$ = carrier harmonic sidebands

LS045

LINEAR INTEGRATED CIRCUIT

CHANNEL AMPLIFIER

The LS 045 is a monolithic integrated circuit intended for use as channel amplifier in FDM and PCM telephone equipment. It features low quiescent power consumption, low distortion, high gain. The LS 045 is available in TO-99 metal case, while the hermetic gold chip (8000 series) is available in SO-8 (8-lead plastic micropackage). This last version is particularly suitable for professional and telecom applications wherever very high MTTF are required.

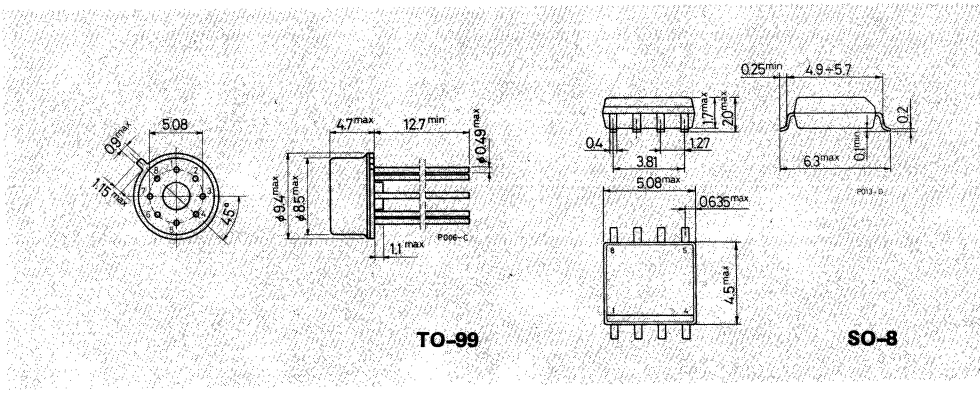
ABSOLUTE MAXIMUM RATINGS

		TO-99	μpackage
V_s	Supply voltage	± 18 V	
$V_{i(1)}$	Input voltage	± 12 V	
ΔV_i	Differential input voltage	± 30 V	
T_{op}	Operating temperature	-25 to 85 °C	
	Output short circuit duration (2)	indefinite	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C

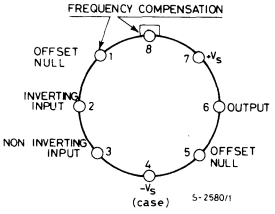
(1) For supply voltages less than ± 12V, input voltage is equal to supply voltage.
(2) The short circuit duration is limited by thermal dissipation.

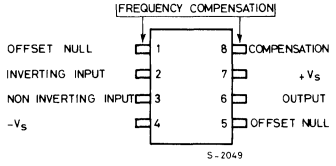
MECHANICAL DATA

Dimensions in mm



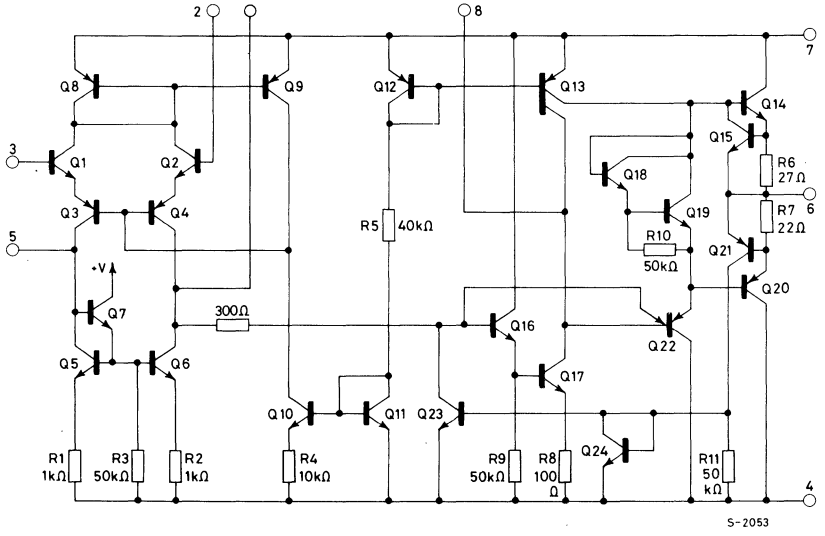
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-99	SO-8
LS 045	LS 045T	LS045M
LS 8045		LS 8045M

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	200* °C/W

* The thermal resistance is measured with the device mounted on a ceramic substrate (25x16x0.6 mm).

ELECTRICAL CHARACTERISTICS (V_s= -20V, V_{bal}= -10V, T_{amb}= 25°C unless otherwise specified. For V_{bal} see fig. 7)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{os}	Input offset voltage	R_g= 10 kΩ			± 1.5	± 10	mV
I_b	Input bias current				100	750	nA
R_i	Input resistance	Open loop			2		MΩ
R_o	Output resistance				75		Ω
G_V	Open loop voltage gain	R_L= 2 kΩ	f = 10 Hz	83	105		dB
d	Distortion	f = 1 kHz $Z_{L\,eq}$= 470Ω	G_V= 40 dB P_o= -5 dBm P_o= 8 dBm		 0.15 0.15	 0.3 0.3	 % %
P_{tot}	Quiescent power dissipation	P_o= 0			20	30	mW
P_o	Maximum output power	d = 1% G_V= 40 dB	Z_{Leq}= 470Ω	14	16		dBm
P_n	Noise power referred to input	$R_g \leqslant$ 1.5 kΩ G_V= 40 dB	f = 1 kHz B = 100 Hz			-120.5	dBm
SVR	Supply voltage rejection referred to output	f = 1 kHz	G_V= 40 dB	30	36		dB

THE FOLLOWING SPECIFICATION APPLY FOR T_{amb} = -25 to 85°C

V_{os}	Input offset voltage	R_g= 10 kΩ			± 15	mV
I_b	Input bias current				1.5	μA
G_V	Open loop voltage gain	R_L= 2 kΩ	78			dB

Fig. 1 - Quiescent power dissipation vs. ambient temperature

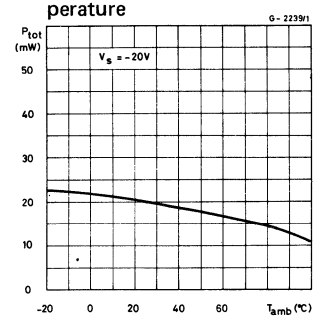


Fig. 2 - Quiescent power dissipation vs. supply voltage

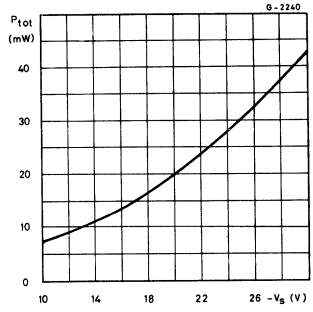


Fig. 3 - Voltage gain (open loop) vs. frequency

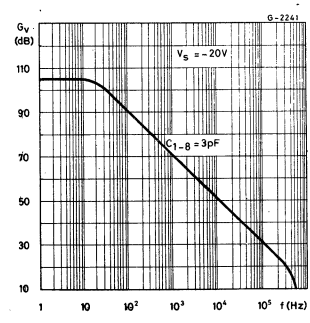


Fig. 4 - Maximum output power vs. load resistance

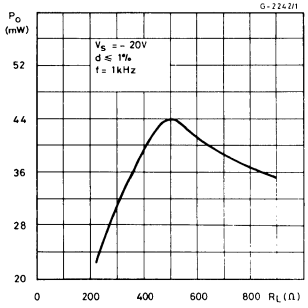


Fig. 5 - Distortion vs. output power

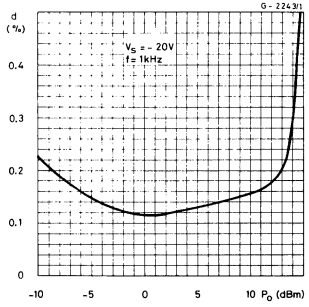
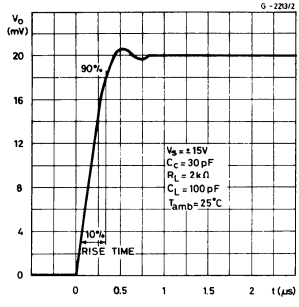


Fig. 6 - Transient response (unity gain)



APPLICATION INFORMATION

Fig. 7 - Channel amplifier circuit

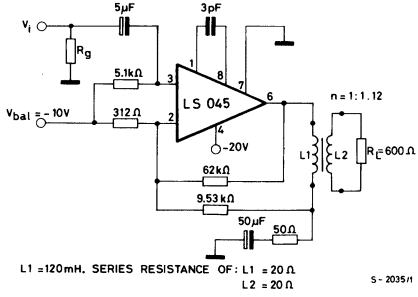


Fig. 8 - Return loss vs. frequency

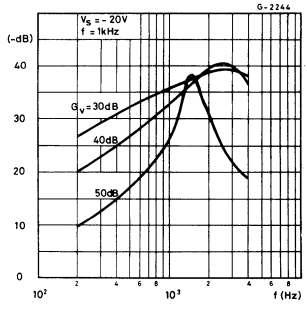
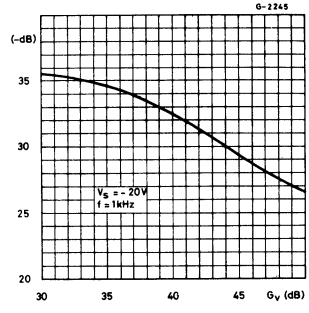


Fig. 9 - Return loss vs. voltage gain



LS101
LS201
LS301

LINEAR INTEGRATED CIRCUITS

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

- GUARANTED DRIFT CHARACTERISTICS
- SLEW RATE OF 10V/μs AS A SUMMING AMPLIFIER
- UNITY GAIN PHASE COMPENSATION WITH A SINGLE 30 pF CAPACITOR
- 3 mV MAX OFFSET VOLTAGE OVER TEMPERATURE RANGE
- 100 nA MAX INPUT BIAS CURRENT OVER TEMPERATURE RANGE

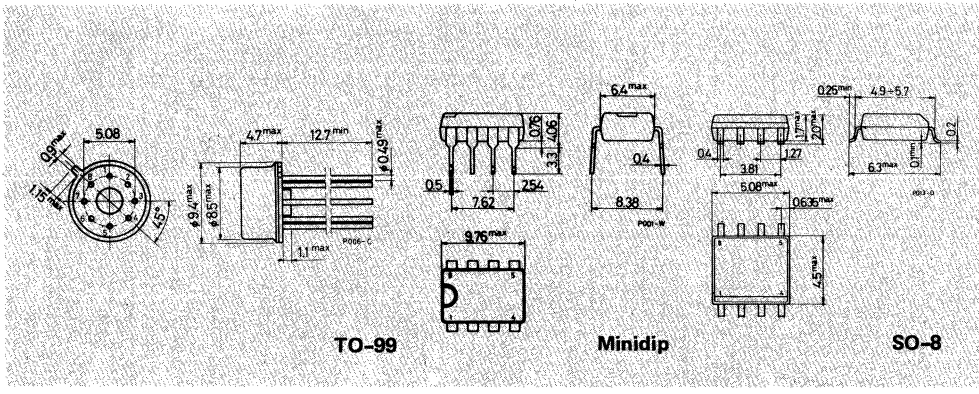
The LS 101 series consists of high performance operational amplifiers, intended for a wide range of analog applications, where tailoring of frequency characteristics is desirable. The LS 101 series is short circuit protected and has the same pin configuration as the LS 141 and LS 148. Absence of latch-up and high common mode voltage range make the LS 101 series ideal for use as voltage followers. In addition, the LS 101 series provides better accuracy and lower noise in high impedance circuitry: the low input current also makes it particularly well suited for long interval integrators, timers, sample and hold circuits and low frequency generators. The LS 101 series is also available with hermetic gold chip (8000 series), particularly suitable for professional and telecom applications, wherever very high MTBF are required.

ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	μpackage
V_s	Supply voltage for **LS 101/101A/201/201A**		± 22 V	
	for **LS 301A**		± 18 V	
V_i (1)	Input voltage		± 15 V	
ΔV_i	Differential input voltage		± 30 V	
T_{op}	Operating temperature for **LS 101/LS 101A**		-55 to 125 °C	
	for **LS 201A**		-25 to 85 °C	
	for **LS 201/LS 301A**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70 °C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C

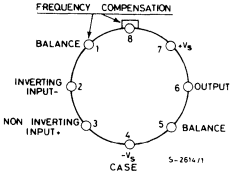
(1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage.
(2) The short circuit duration is limited by thermal dissipation.

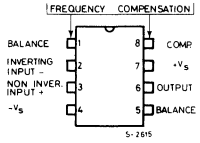
MECHANICAL DATA

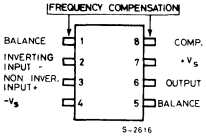
Dimensions in mm



CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

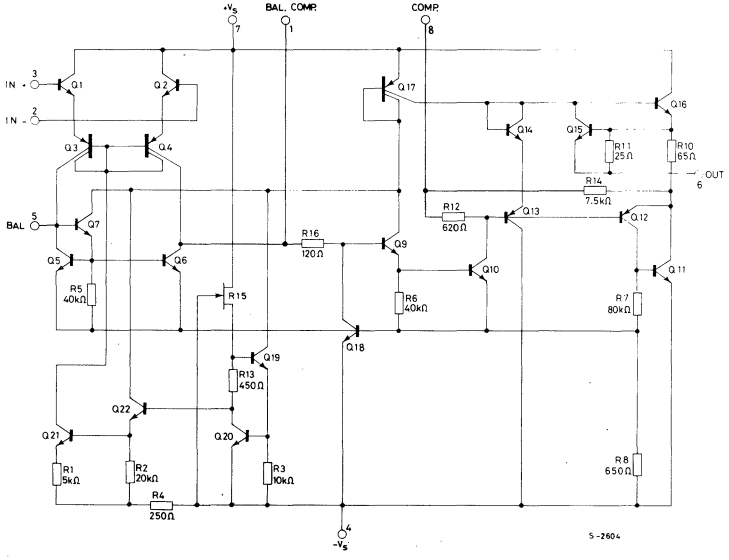






Type	TO-99	Minidip	SO-8
LS 101	LS 101T	—	—
LS 101A	LS 101AT	—	—
LS 201	LS 201T	LS 201B	LS 201M
LS 201A	LS 201AT	—	—
LS 301A	LS 301AT	LS 301AB	LS 301AM
LS 8101	—	—	LS 8101M
LS 8101A	—	—	LS 8101AM
LS 8201	—	—	LS 8201M
LS 8201A	—	—	LS 8201AM
LS 8301A	—	—	LS 8301AM

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25x16x0.6 mm)

ELECTRICAL CHARACTERISTICS* for LS 101 and LS 201

Parameter		Test conditions	LS 101			LS 201			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 10\ k\Omega$ $T_{amb}= 25°C$		 1	6 5		 2	10 7.5	mV mV
$\frac{\Delta V_{os}}{\Delta T}$	Average temperat. coefficient of input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$		6 3			10 6		µV/°C µV/°C
I_{os}	Input offset current	$T_{amb}= 25°C$ $T_{amb}= T_{max}$ $T_{amb}= T_{min}$		40 10 100	200 200 500		100 50 150	500 400 750	nA nA nA
I_b	Input bias current	 $T_{amb}= 25°C$		 0.12	1.5 0.5		 0.25	2 1.5	µA µA
R_i	Input resistance	$T_{amb}= 25°C$	0.3	0.8		0.1	0.4		MΩ
V_i	Input voltage range	$V_s = \pm 15V$	± 12			± 12			V
G_v	Large signal voltage gain	$V_s = \pm 15V$ $V_o= \pm 10V$ $R_L \geq 2\ k\Omega$	88			83			dB
		$V_s = \pm 15V$ $V_o= \pm 10V$ $R_L \geq 2\ k\Omega$ $T_{amb}= 25°C$	94	104		86	103		dB
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	90		65	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	70	90		70	90		dB
V_o	Output voltage swing	$V_s = \pm 15V$ $R_L= 10\ k\Omega$ $R_L= 2\ k\Omega$	 ± 12 ± 10	 ± 14 ± 13		 ± 12 ± 10	 ± 14 ± 13		 V V
I_s	Supply current	$V_s \pm 20V$		1.8	3		1.8	3	mA

* These specifications, unless otherwise specified, apply for $C_1= 30$ pF, $V_s= \pm 5$ to $\pm 20V$ and $T_{amb}= -55$ to 125 °C (LS 101/LS 101A), $T_{amb}= -25$ to 85 °C (LS 201A) and $T_{amb}= 0$ to 70 °C (LS 201); $V_s= \pm 5$ to $\pm 15V$ and $T_{amb}= 0$ to 70 °C (LS 301A).

ELECTRICAL CHARACTERISTICS* for LS 101A, LS 201A and LS 301A

Parameter		Test conditions	LS 101A/LS 201A			LS 301A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 10\ k\Omega$ $T_{amb}= 25°C$		 0.7	3 2		 2	10 7.5	mV mV
$\frac{\Delta V_{os}}{\Delta T}$	Average temperat. coefficient of input offset voltage	$R_g \leq 10\ k\Omega$		3	15		6	30	μV/°C
I_{os}	Input offset current	$T_{amb}= 25°C$		 1.5	20 10		 3	70 50	nA nA
$\frac{\Delta I_{os}}{\Delta T}$	Average temperat. coefficient of input offset current	$T_{amb}= 25°C$ to T_{max} $T_{amb}= T_{min}$ to 25°C		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
I_b	Input bias current	 $T_{amb}= 25°C$		 30	0.1 75		 70	0.3 250	μA nA
R_i	Input resistance	$T_{amb}= 25°C$	1.5	4		0.5	2		MΩ
V_i	Input voltage range	$V_s = \pm 20V$ $V_s = \pm 15V$	± 15			 ±12			V V
G_v	Large signal voltage gain	$V_s= \pm 15V$ $V_o= \pm 10V$ $R_L \geq 2\ k\Omega$	 88			 83			dB
		$V_s = \pm 15V$ $V_o= \pm 10V$ $R_L \geq 2\ k\Omega$ $T_{amb}= 25°C$	94	104		86	104		dB
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	80	96		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	80	96		70	96		dB
V_o	Output voltage swing	$V_s = \pm 15V$ $R_L= 10\ k\Omega$ $R_L= 2\ k\Omega$	 ± 12 ± 10	 ± 14 ± 13		 ± 12 ± 10	 ± 14 ± 13		 V V
I_s	Supply current	$V_s= \pm 20V$ $T_{amb}= T_{max}$		1.2	2.5				mA
		$T_{amb}= 25°C$ $V_s = \pm 20V$ $V_s = \pm 15V$		 1.8	 3		 1.8	 3	 mA mA

* These specifications, unless otherwise specified, apply for $C_1= 30$ pF, $V_s= \pm 5$ to $\pm 20V$ and $T_{amb}= -55$ to 125 °C (LS 101/LS 101A), $T_{amb}= -25$ to 85 °C (LS 201A) and $T_{amb}= 0$ to 70 °C (LS 201); $V_s= \pm 5$ to $\pm 15V$ and $T_{amb}= 0$ to 70 °C (LS 301A).

Guaranteed characteristics (LS 101/LS 201)

Fig. 1 - Input voltage range vs. supply voltage

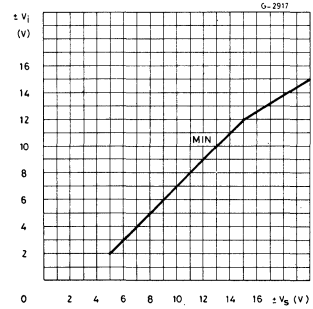


Fig. 2 - Output voltage swing vs. supply voltage

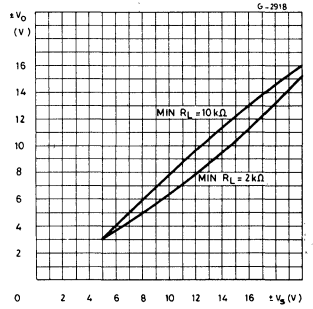
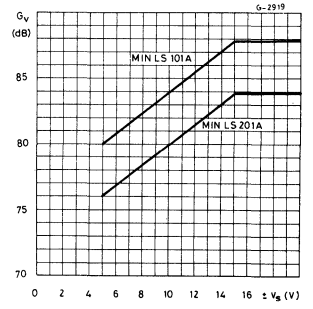


Fig. 3 -- Voltage gain vs. supply voltage



Guaranteed characteristics (LS 101A/LS 201A)

Fig. 4 - Input voltage range vs. supply voltage

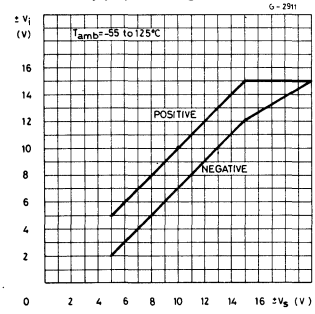


Fig. 5 - Output voltage swing vs. supply voltage

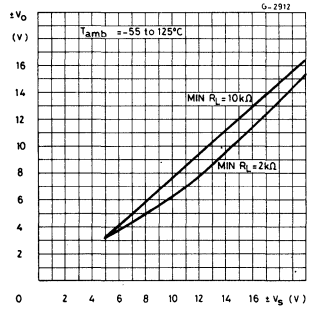
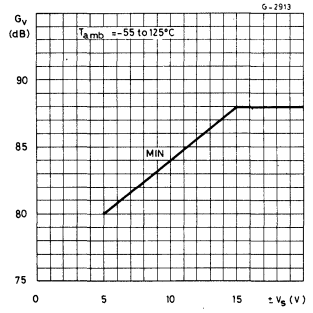


Fig. 6 - Voltage gain vs. supply voltage



Guaranteed characteristics (LS 301A)

Fig. 7 - Input voltage range vs. supply voltage

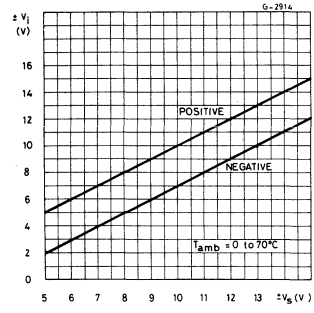


Fig. 8 - Output voltage swing vs. supply voltage

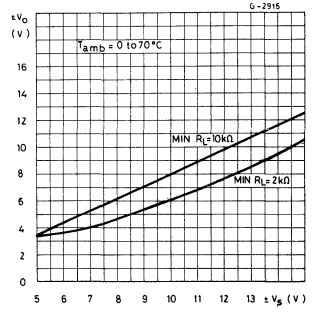


Fig. 9 - Voltage gain vs. supply voltage

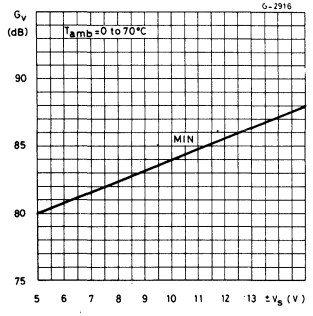


Fig. 10 - Input bias current vs. ambient temperature (for LS 101A/201A/301A)

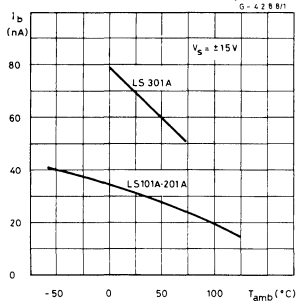


Fig. 11 - Input offset current vs. ambient temperature (for LS 101A/201A/301A)

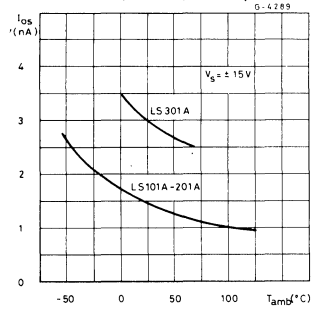


Fig. 12 - Input bias current vs. ambient temperature (for LS 101/201)

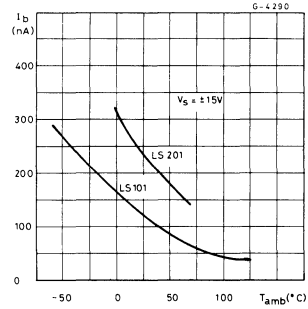


Fig. 13 - Input offset current vs. ambient temperature (for LS 101/201)

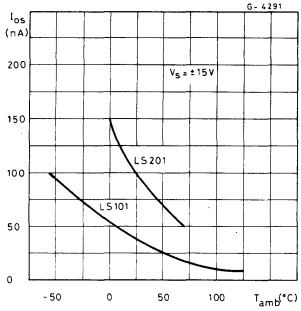


Fig. 14 - Supply current vs. supply voltage

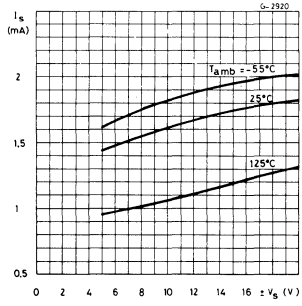


Fig. 15 - Voltage gain vs. supply voltage

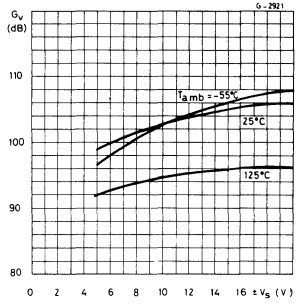


Fig. 16 - Output voltage swing vs. output current

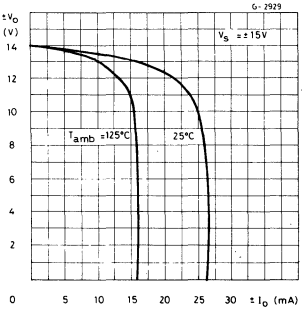


Fig. 17 - Input noise voltage vs. frequency

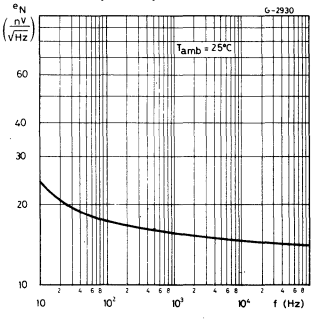
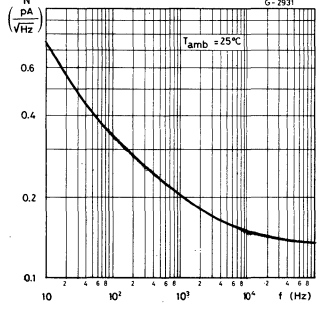


Fig. 18 - Input noise current vs. frequency



OPERATIONAL AMPLIFIER COMPENSATION

SINGLE POLE

Fig. 19

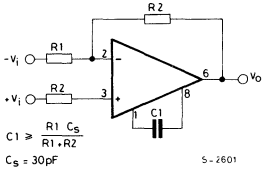


Fig. 20 - Open loop frequency response

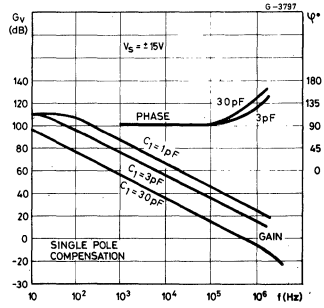
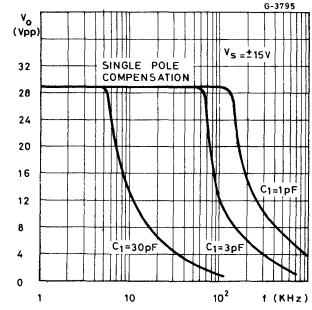


Fig. 21 - Large signal frequency response



TWO POLE

Fig. 22

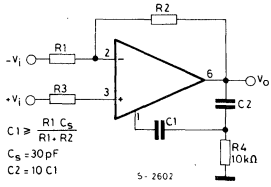


Fig. 23 - Open loop frequency response

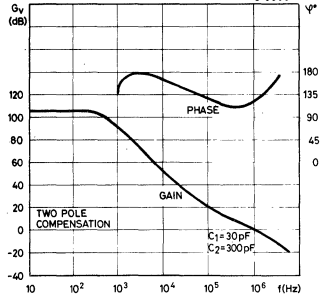
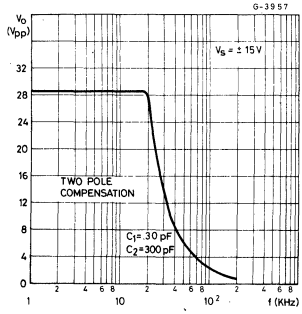


Fig. 24 - Large signal frequency response



FEED FORWARD

Fig. 25

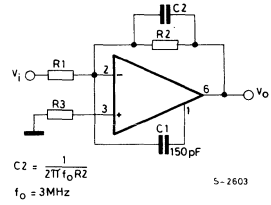


Fig. 26 - Open loop frequency response

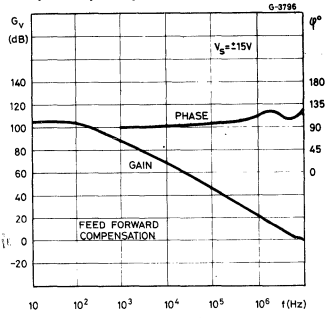


Fig. 27 - Large signal frequency response

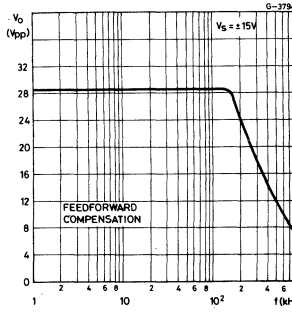


Fig. 28 - Single pole compensation pulse response

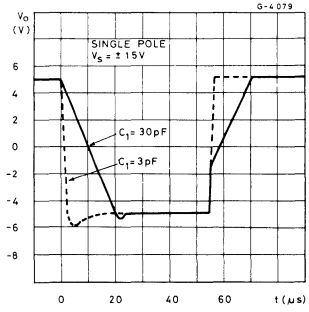


Fig. 29 - Two pole compensation pulse response

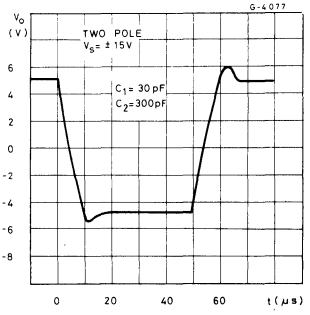
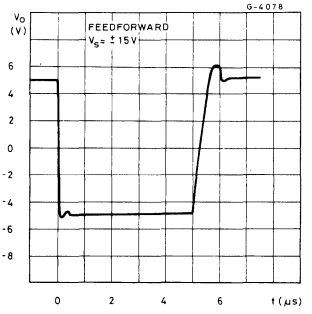


Fig. 30 - Feed forward pulse response



TYPICAL APPLICATIONS

Fig. 31 - Inverting amplifier with balancing circuit

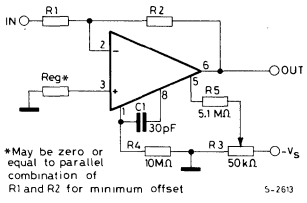


Fig. 32 - Integrator with bias current compensation

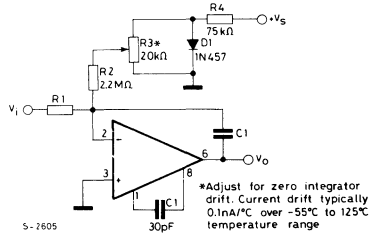


Fig. 33 - Standard compensation and offset balancing circuit

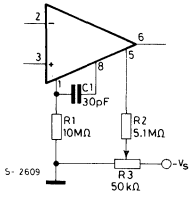
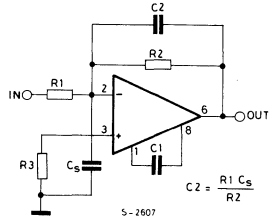


Fig. 34 - Compensation for stray input capacitances or large feedback resistor



TYPICAL APPLICATIONS (continued)

Fig. 35 - Protecting against gross fault conditions

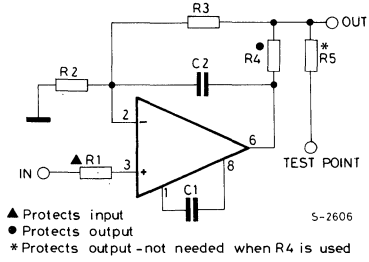


Fig. 36 - Bilateral current source

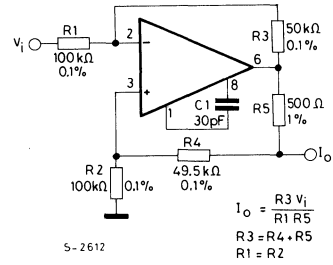
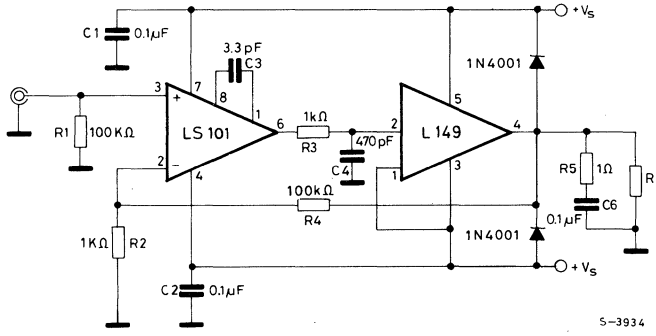


Fig. 37 - Power operational amplifier (G_v = 40 dB)



LINEAR INTEGRATED CIRCUITS

LS107
LS207
LS307

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIERS

- LOW OFFSET CURRENT AND VOLTAGE
- LOW INPUT CURRENT
- GUARANTEED DRIFT CHARACTERISTICS

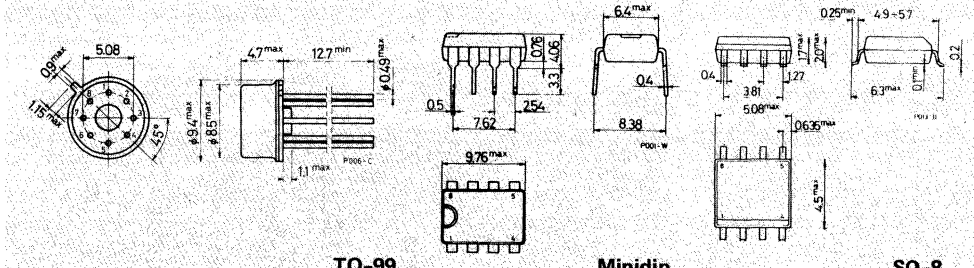
The LS 107 series consists of general purpose operational amplifiers, with the frequency compensation built into the chip. They replace pin-to-pin the LS 709, LS 101, LS 141 and LS 148.
The LS 107 series offers features similar to the LS 101A, providing better accuracy and lower noise in high impedance circuits. The low input currents allow the device to be used in slow charge applications, such as long interval integrators, slow ramps, sample and hold circuits.
The LS 107 series is available with hermetic gold chip (8000 series), particularly suitable for professional and telecom applications, wherever very high MTBF are required.

ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	μpackage
V_s	Supply voltage for **LS 107** and **LS 207**		± 22V	
	for **LS 307**		± 18V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
T_{op}	Operating temperature for **LS 107**		-55 to 125 °C	
	for **LS 207**		-25 to 85 °C	
	for **LS 307**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C
	Lead soldering temperature	300 °C (10s)	260 °C (12s)	260 °C (5s) 235 °C (11s)

1) For supply voltages less than ±15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

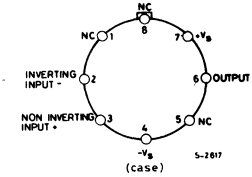
MECHANICAL DATA

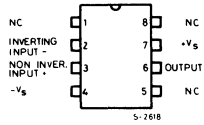
Dimensions in mm

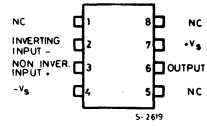


LS107
LS207
LS307

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

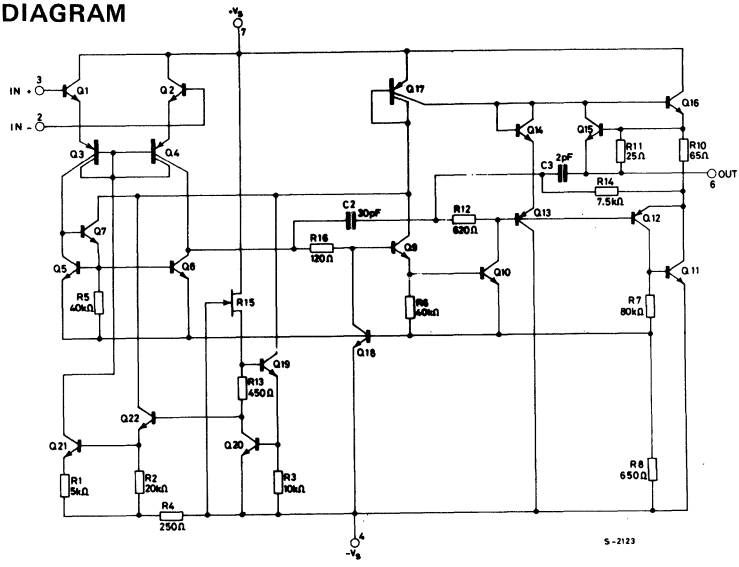






Type	TO-99	Minidip	SO-8
LS 107	LS 107T	–	–
LS 207	LS 207T	–	–
LS 307	LS 307T	LS 307B	LS 307M
LS 8107	–	–	LS 8107M
LS 8207	–	–	LS 8207M
LS 8307	–	–	LS 8307M

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25x16x0.6 mm)

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 107/LS 207			LS 307			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leqslant 10\ k\Omega$			3			10	mV
		$R_g \leqslant 10\ k\Omega$ $T_{amb}= 25°C$		0.7	2		2	7.5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Average temperature coefficient of input offset voltage			3	15		6	30	$\mu V/°C$
I_{os}	Input offset current				20			70	nA
		$T_{amb}= 25°C$		1.5	10		3	50	nA
$\frac{\Delta I_{os}}{\Delta T}$	Average temperature coefficient of input offset current	$T_{amb}= 25°C$ to T_{max}		0.01	0.1		0.01	0.3	nA/°C
		$T_{amb}= T_{min}$ to 25°C		0.02	0.2		0.02	0.6	nA/°C
I_b	Input bias current				100			300	nA
		$T_{amb}= 25°C$		30	75		70	250	nA
R_i	Input resistance	$T_{amb}= 25°C$	1.5	4		0.5	2		MΩ
G_v	Large signal voltage gain	$V_s= \pm 15V$ $V_o= \pm 10V$ $R_L \geqslant 2\ k\Omega$	88			84			dB
		$V_s= \pm 15V$ $V_o= \pm 10V$ $R_L \geqslant 2\ k\Omega$ $T_{amb}= 25°C$	94	104		88	104		dB
V_i	Input voltage range	$V_s= \pm 20V$	±15						V
		$V_s= \pm 15V$				±12			V
V_o	Output voltage swing	$V_s= \pm 15V$ $R_L= 10\ k\Omega$	±12	±14		±12	±14		V
		$V_s= \pm 15V$ $R_L= 2\ k\Omega$	±10	±13		±10	±13		V
CMR	Common mode rejection	$R_g \leqslant 10\ k\Omega$	80	96		70	90		dB
SVR	Supply voltage rejection	$R_g \leqslant 10\ k\Omega$	80	96		70	96		dB
I_s	Supply current	$V_s= \pm 20V$							
		$T_{amb}= 25°C$		1.8	3				mA
		$T_{amb}= 125°C$		1.2	2.5				mA
		$V_s= \pm 15V$ $T_{amb}= 25°C$					1.8	3	mA

Note: These specifications, unless otherwise specified, apply for $V_s= \pm 5V$ to $\pm 20V$ and $T_{amb}= -55$ to 125°C for LS 107; $V_s= \pm 5V$ to $\pm 20V$ and $T_{amb}= -25$ to 85°C for LS 207; $V_s= \pm 5V$ to $\pm 15V$ and $T_{amb}= 0$ to 70°C for LS 307.

LS107 LS207 LS307

Fig. 1 - Supply current vs. supply voltage

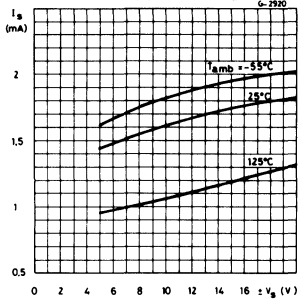


Fig. 2 - Voltage gain vs. supply voltage

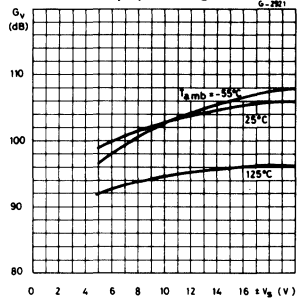


Fig. 3 - Input current vs. ambient temp.

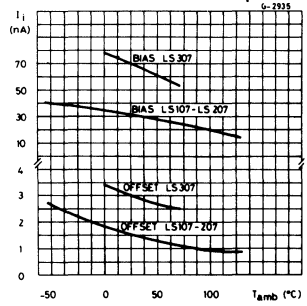


Fig. 4 - Current limiting vs. output current

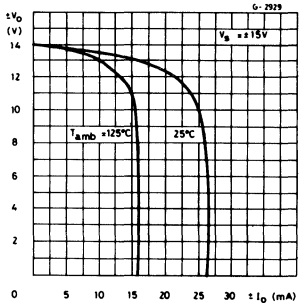


Fig. 5 - Input noise voltage vs. frequency

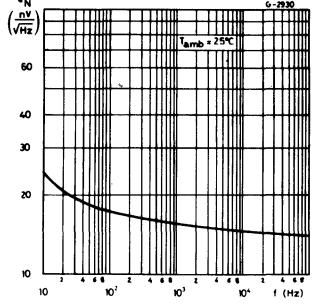


Fig. 6 - Input noise current vs. frequency

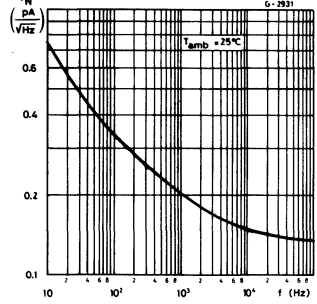


Fig. 7 - Open loop frequency response

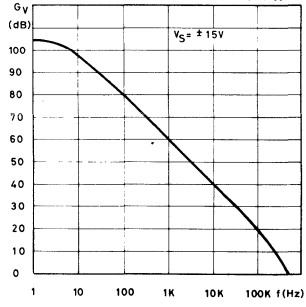


Fig. 8 - Large signal frequency response

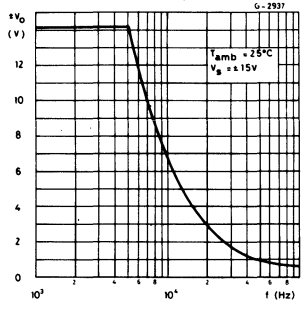
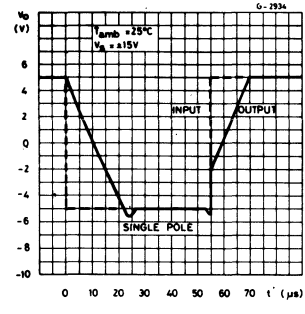


Fig. 9 - Voltage follower pulse response



Guaranteed performance characteristics (LS 107/LS 207)

Fig. 10 - Input voltage range vs. supply voltage

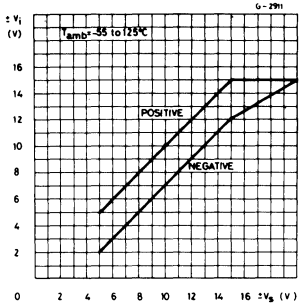


Fig. 11 - Output voltage swing vs. supply voltage

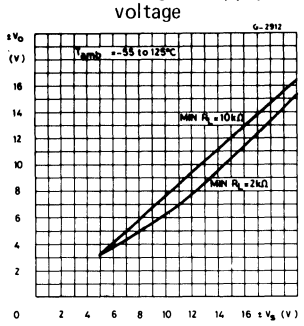
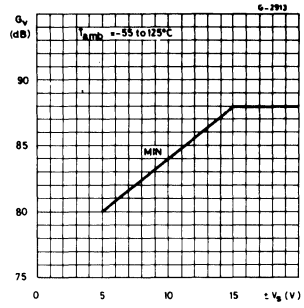


Fig. 12 - Voltage gain vs. supply voltage



Guaranteed performance characteristics (LS 307)

Fig. 13 - Input voltage range vs. supply voltage

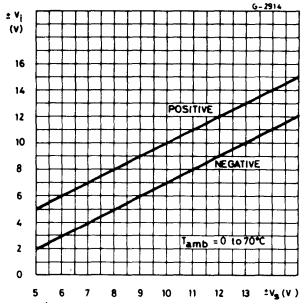


Fig. 14 - Output voltage swing vs. supply voltage

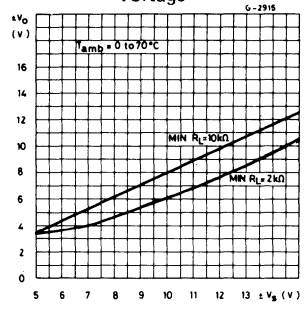
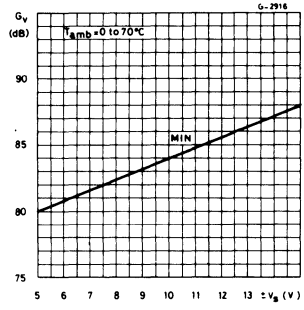


Fig. 15 - Voltage gain vs. supply voltage



TYPICAL APPLICATIONS

Fig. 16 - Inverting amplifier

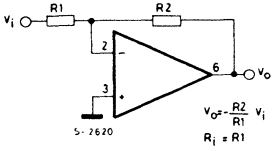


Fig. 17 - Non-inverting AC amplifier

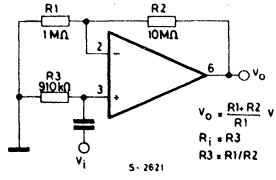
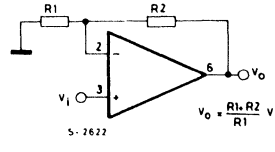


Fig. 18 - Non-inverting amplifier



LS141
LS141A
LS141C

LINEAR INTEGRATED CIRCUITS

FREQUENCY COMPENSATED OPERATIONAL AMPLIFIERS

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP

The LS 141 series consists of general purpose operational amplifiers, intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the LS 141 series ideal for use as a voltage follower.The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers, and general feedback applications. The LS 141 series is available with hermetic gold chip (8000 series). This is particularly suitable for professional and telecom applications, wherever very high MTBF are required.

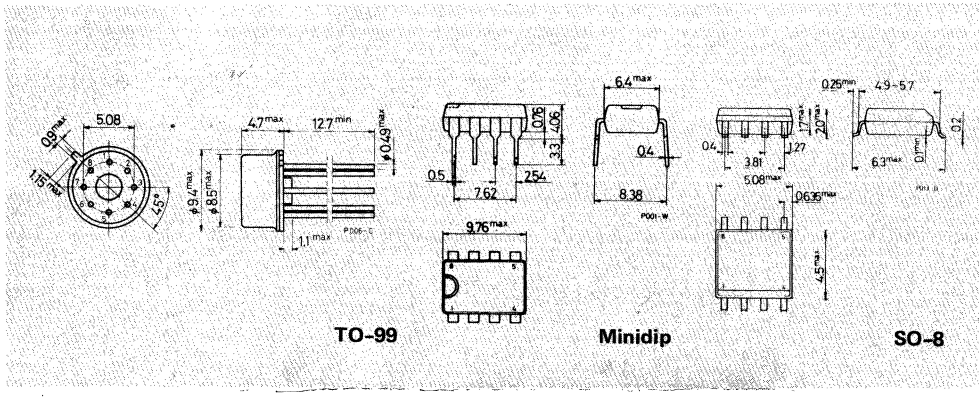
ABSOLUTE MAXIMUM RATINGS

		TO-99	Minidip	µpackage
V_s	Supply voltage for **LS 141/LS 141A**		± 22V	
	for **LS 141C**		± 18V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
T_{op}	Operating temperature for **LS 141/LS 141A**		-55 to 125°C	
	for **LS 141C**		0 to 70°C	
	Output short circuit duration(2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70°C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150°C	-55 to 150°C	-55 to 150°C
	Lead soldering temperature	300°C (10s)	260°C (12s)	260°C (5s) 235°C (11s)

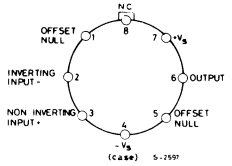
1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

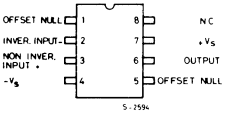
MECHANICAL DATA

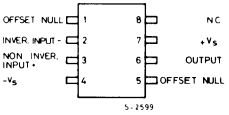
Dimensions in mm



CONNECTION DIAGRAMS AND ORDERING NUMBERS

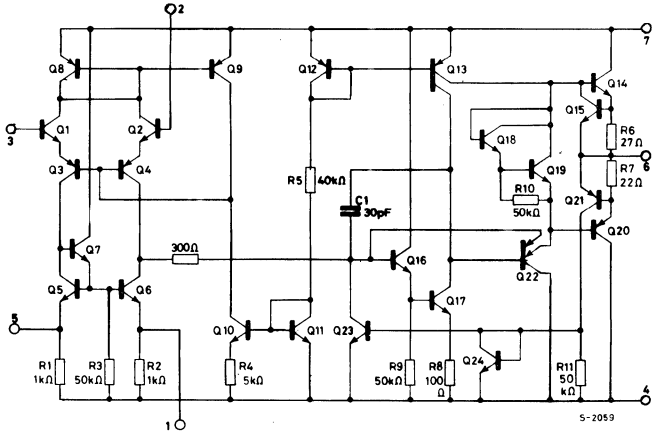






Type	TO-99	Minidip	SO-8
LS 141	LS 141T	—	—
LS 141A	LS 141 AT	—	—
LS 141C	LS 141 CT	LS 141 CB	LS 141 CM
LS 8141	—	—	LS 8141M
LS 8141A	—	—	LS 8141 AM
LS 8141C	—	—	LS 8141 CM

SCHEMATIC DIAGRAM



THERMAL DATA

			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm)

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 141			LS 141A			LS 141C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C $R_g \leq 10\ k\Omega$ $R_g \leq 50\ \Omega$		1	5		0.8	3		2	6	mV mV
		T_{amb}= T_{min} to T_{max} $R_g \leq 10\ k\Omega$ $R_g \leq 50\ \Omega$			6			4			7.5	mV mV
ΔV_{os}	Input offset voltage adjust. range	V_s= ± 20V V_s= ± 15V T_{amb}= 25°C		±15		±10				±15		mV mV
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift							15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		20 85	200 500		3	30 70		20	200 300	nA nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.5				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		80	500 1.5		30	80 0.21		80	500 0.8	nA μA
R_i	Input resistance	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}	0.3	2		1 0.5	6		0.3	2		MΩ MΩ
V_i	Input voltage range	T_{amb}= T_{min} to T_{max}	±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V	94	106		94			86	106		dB
		T_{amb}= T_{min} to T_{max} $R_L \geq 2\ k\Omega$ V_s= ±15V V_o= ±10V V_s= ±5V V_o= ±2V	88			90 80			84			dB
V_o	Output voltage swing	V_s= ±15V $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
I_{sc}	Output short circuit current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		25		10 10	25	35 40		25		mA mA
CMR	Common mode rejection	V_s = ±20V $R_g \leq 10\ k\Omega$ V_{CM}=±12V	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 50\Omega$ V_s=±5to±20V $R_g \leq 10k\Omega$ V_s=±5to±15V	77	96		86	96		77	96		dB dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LS 141			LS 141A			LS 141C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain) Rise time Overshoot	T_{amb}= 25°C		 0.3 5			 0.25 6	 0.8 20		 0.3 5		 µs %
B	Bandwidth	T_{amb}= 25°C				0.437	1.5					MHz
SR	Slew rate	T_{amb}= 25°C		0.5		0.3	0.7			0.5		V/µs
I_S	Supply current	T_{amb}= 25°C		1.7	2.8					1.7	2.8	mA
P_{tot}	Power consumption	T_{amb}= 25°C V_S= ±20V V_S= ±15V		 50	 85		 80	 150		 50	 85	 mW mW
		V_S= ±20V T_{amb}= T_{min} T_{amb}= T_{max}						 165 135				 mW mW
		V_S= ±15V T_{amb}= T_{min} T_{amb}= T_{max}		 60 45	 100 75							 mW mW

Note: These specifications, unless otherwise specified, apply for V_S= ±15V and T_{amb}= -55 to 125°C for LS 141 and LS 141A. For the LS 141C these specifications apply for T_{amb}= 0 to 70°C

Fig. 1 - Open loop voltage gain vs. supply voltage

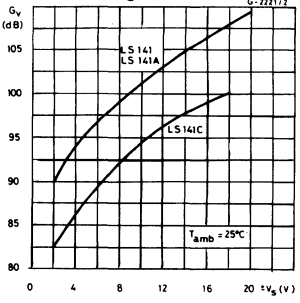


Fig. 2 - Output voltage swing vs. supply voltage

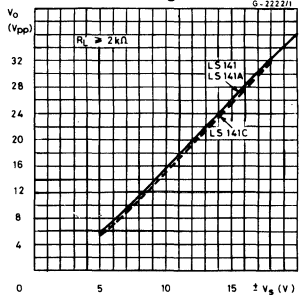


Fig. 3 - Power consumption vs. supply voltage

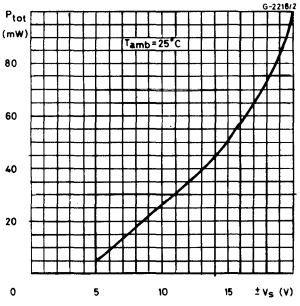


Fig. 4 - Open loop voltage gain vs. frequency

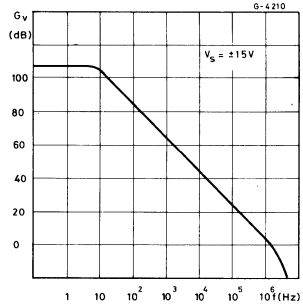


Fig. 5 - Open loop phase response vs. frequency

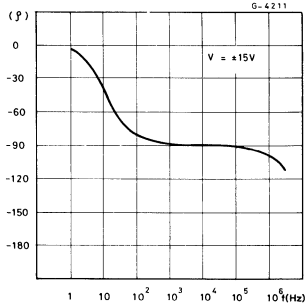


Fig. 6 - Input offset current vs. supply voltage (for LS 141 and LS 141C)

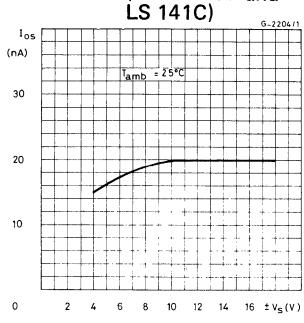


Fig. 7 - Input resistance and capacitance vs. frequency (for LS 141 and LS 141C)

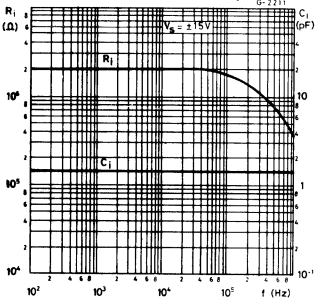


Fig. 8 - Output resistance vs. frequency.

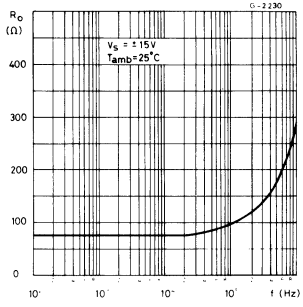


Fig. 9 - Output voltage swing vs. load resistance

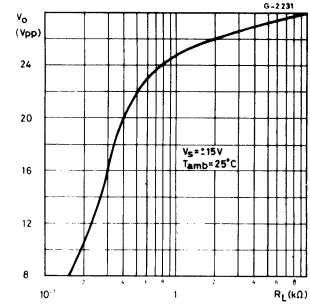


Fig. 10 - Output voltage swing vs. frequency

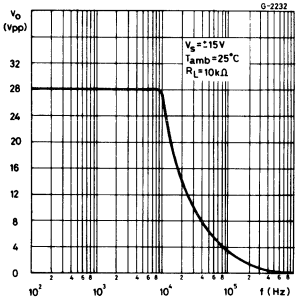


Fig. 11 - Input noise voltage vs. frequency

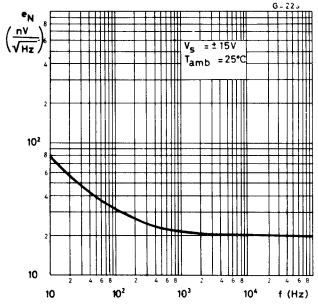


Fig. 12 - Input noise current vs. frequency

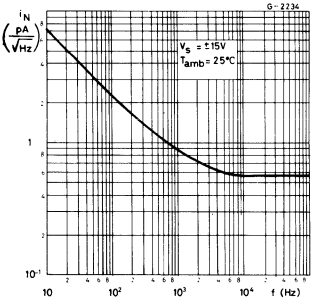


Fig. 13 - Transient response

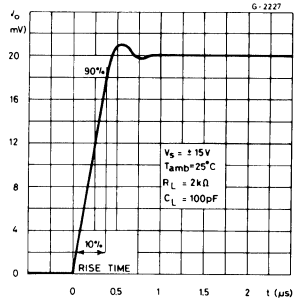


Fig. 14 - Common mode rejection ratio vs. frequency

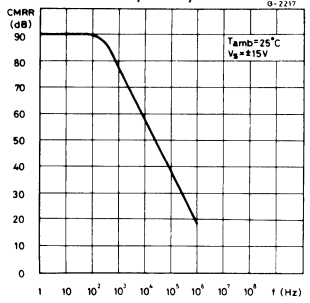
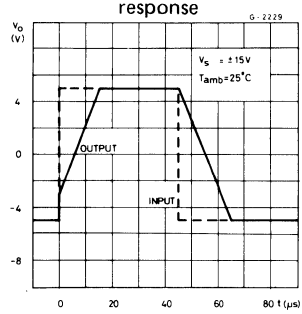


Fig. 15 - Voltage follower large signal pulse response



Typical performance curves for LS 141 and LS 141A

Fig. 16 - Input bias current vs. ambient temperature

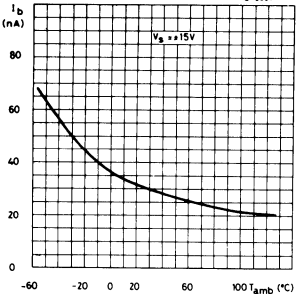


Fig. 17 - Input resistance vs. ambient temperature

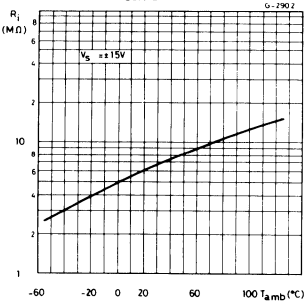


Fig. 18 - Input offset current vs. ambient temperature

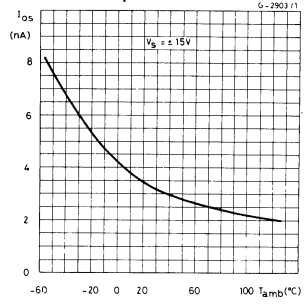


Fig. 19 - Output short-circuit current vs. ambient temperature

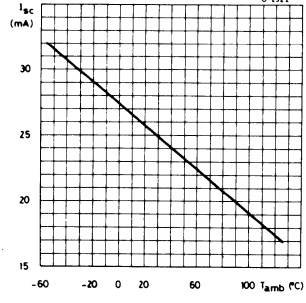


Fig. 20 - Power consumption vs. ambient temperature

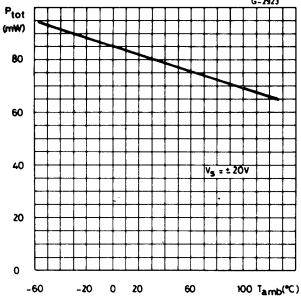
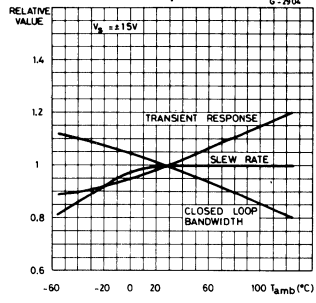


Fig. 21 - Frequency characteristics vs. ambient temperature



Typical performance curves for LS 141C

Fig. 22 - Input bias current vs. ambient temperature

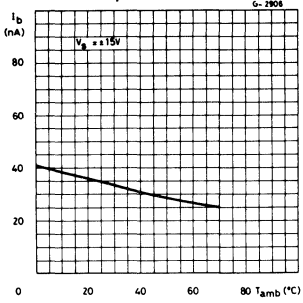


Fig. 23 - Input resistance vs. ambient temperature

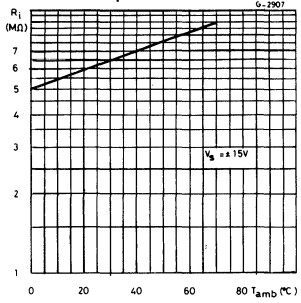


Fig. 24 - Input offset current vs. ambient temperature

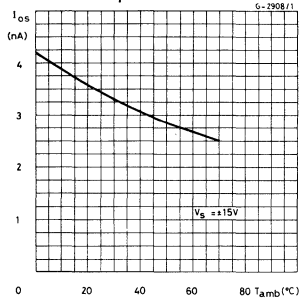


Fig. 25 - Output short circuit current vs. ambient temperature

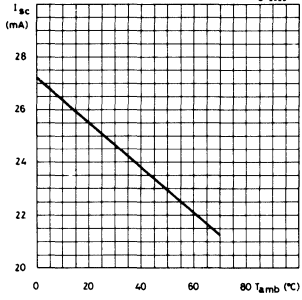


Fig. 26 - Power consumption vs. ambient temperature

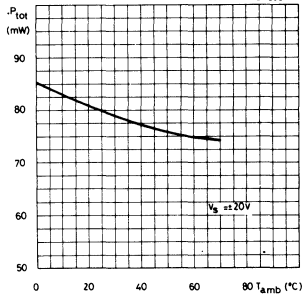
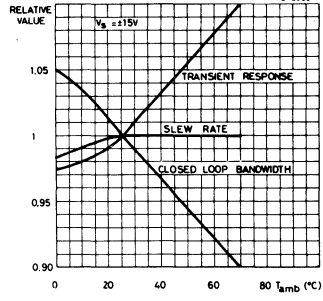


Fig. 27 - Frequency characteristics vs. ambient temperature



TYPICAL APPLICATIONS

Fig. 28 - Clipping amplifier

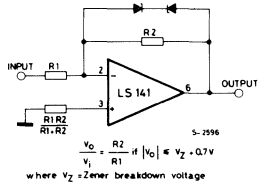


Fig. 29 - Simple integrator

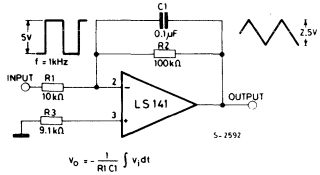
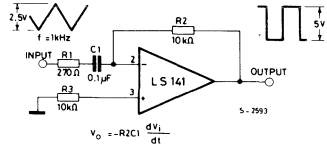


Fig. 30 - Simple differentiator



LINEAR INTEGRATED CIRCUITS

LS148
LS148A
LS148C

OPERATIONAL AMPLIFIERS

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE
- NO LATCH-UP
- SLEW-RATE = 5.5V/μs (G_v = 10, C_C = 3.5 pF)

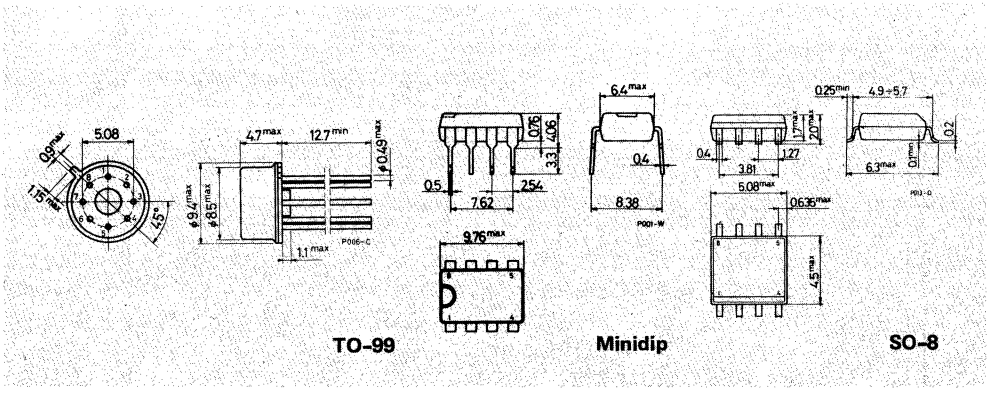
The LS 148 series consists of general purpose operational amplifiers, intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "Latch-up" tendencies make the LS 148 series ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrators, summing amplifiers and general feedback applications. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. The LS 148 series is available with hermetic gold chip (8000 series). This is particularly suitable for professional and telecom applications, wherever very high MTBF are required.

ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	μpackage
V_s	Supply voltage		± 22V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
T_{op}	Operating temperature for **LS 148/LS 148A**		-55 to 125 °C	
	for **LS 148C**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70°C	520 mW	665 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C

1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation.

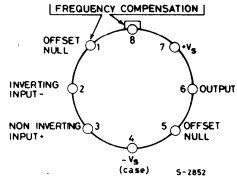
MECHANICAL DATA

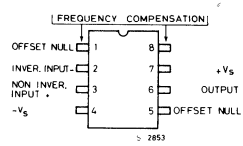
Dimensions in mm

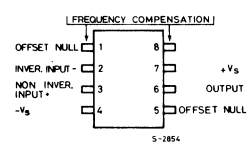


LS148
LS148A
LS148C

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

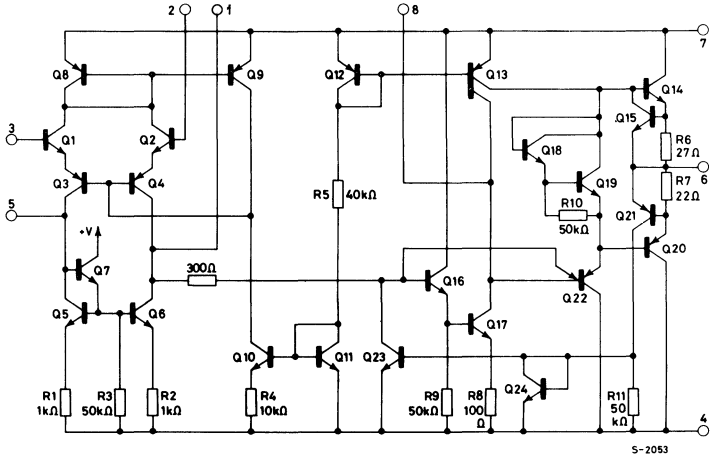






Type	TO-99	Minidip	SO-8
LS 148	LS 148T	–	–
LS 148A	LS 148 AT	–	–
LS 148C	LS 148 CT	LS 148 CB	LS 148 CM
LS 8148	–	–	LS 8148M
LS 8148A	–	–	LS 8148 AM
LS 8148C	–	–	LS 8148 CM

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm)

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 148			LS 148A			LS 148C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	T_{amb}= 25°C $R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$		1	5		 0.5	 2		2	6	mV mV
		T_{amb}= T_{min} to T_{max} $R_g \leq 10\ k\Omega$ $R_g \leq 50\Omega$		1	6		 0.5	 3			7.5	mV mV
ΔV_{os}	Input offset voltage adjust. range	T_{amb}= 25°C		±15			±25			±15		mV
$\frac{\Delta V_{os}}{\Delta T}$	Average input offset voltage drift	$R_g \leq 50\Omega$					2.5	15				$\frac{\mu V}{°C}$
I_{os}	Input offset current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		20 50	200 500		2	10 25		20	200 300	nA nA
$\frac{\Delta I_{os}}{\Delta T}$	Average input offset current drift							0.15				$\frac{nA}{°C}$
I_b	Input bias current	T_{amb}= 25°C T_{amb}= T_{min} to T_{max}		80	500 1.5		20	75 0.1		80	500 0.8	nA μA
R_i	Input resistance	T_{amb}= 25°C	0.3	2		2	10		0.3	2		MΩ
V_i	Input voltage range		±12	±13		±12	±13		±12	±13		V
G_v	Large signal voltage gain	T_{amb}= 25°C $R_L \geqslant 2\ k\Omega$ V_s= ±15V V_o= ±10V T_{amb}= T_{min} to T_{max} $R_L \geqslant 2\ k\Omega$ V_s= ±15V V_o= ±10V	 94 88	 104		 94 88	 108		 86 84	 104		 dB dB
V_o	Output voltage swing	V_s= ±15V $R_L \geqslant 10\ k\Omega$ $R_L \geqslant 2\ k\Omega$	 ±12 ±10	 ±14 ±13		 ±12 ±10	 ±14 ±13		 ±12 ±10	 ±14 ±13		 V V
I_{sc}	Output short circuit current			25			25			25		mA
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$ V_{CM}= ±12V	70	90		80	95		70	90		dB
SVR	Supply voltage rejection	V_s= ±5 to ± 20V $R_g \leq 10\ k\Omega$	 76	 90		 80	 97		 76	 90		 dB
SR	Slew rate	T_{amb}= 25°C G_v= 1 $R_L \geqslant 2\ k\Omega$ G_v= 10*	 	0.5 5.5		 	0.5 5.5		 	0.5 5.5		V/μs V/μs

* C_C = 3.5 pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	LS 148			LS 148A			LS 148C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Transient respon. (unity gain)	T_{amb}= 25°C V_i= 20 mV C_c= 30 pF R_L= 2 kΩ $C_L \leqslant$ 100 pF										
	Rise time			0.2			0.2			0.2		µs
	Overshoot			5			5			5		%
I_s	Supply current	T_{amb}= 25°C		1.9	2.8		1.9	2.8		1.9	2.8	mA
P_S	Power consumption	T_{amb}= 25°C V_s= ±20V					60	85				mW
		V_s= ±15V		60	85					60	85	mW
		V_s= ±15V T_{amb}= T_{min}		60	100		60	100		60	100	mW
		T_{amb}= T_{max}		45	75		40	75				mW

Note: These specifications, unless otherwise specified, apply for V_s= ±15V and T_{amb}= -55 to 125°C for LS 148 and LS 148A. For LS 148C these specifications apply for T_{amb}= 0 to 70°C (C_c= 30 pF).

Fig. 1 - Voltage offset null circuit

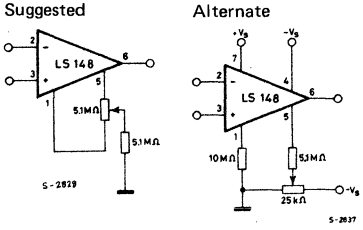
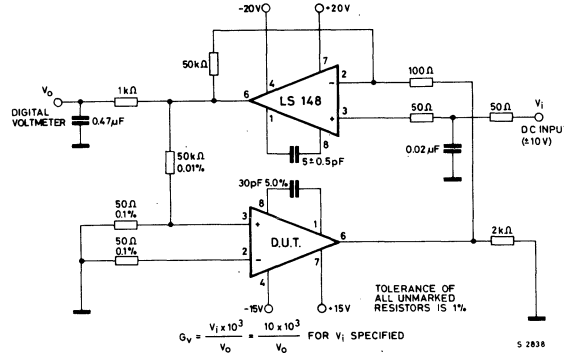


Fig. 2 - Gain test circuit



Typical performance curves for LS 148

Fig. 3 - Input bias current vs. ambient temperature

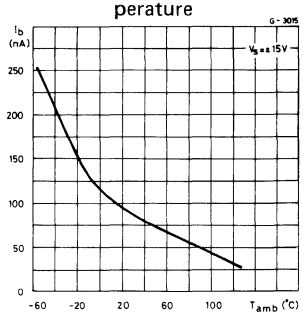


Fig. 4 - Input resistance vs. ambient temperature

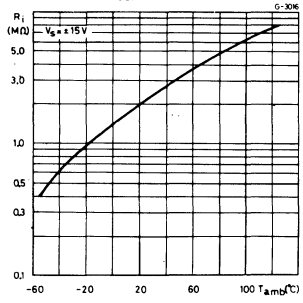


Fig. 5 - Output short-circuit current vs. ambient temperature

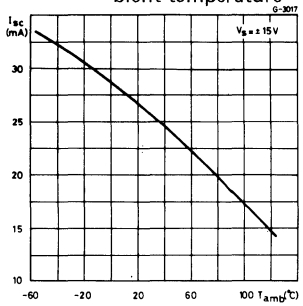


Fig. 6 - Input offset current vs. ambient temperature

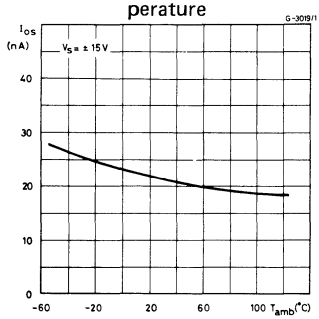


Fig. 7 - Power consumption vs. ambient temperature

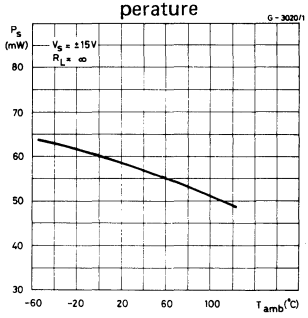
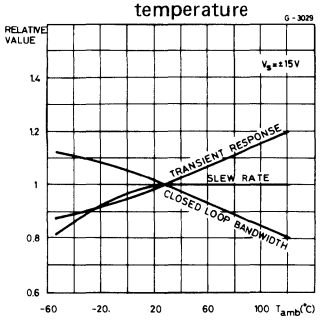


Fig. 8 - Frequency characteristics vs. ambient temperature



Typical performance curves for LS 148C

Fig. 9 - Input bias current vs. ambient temperature

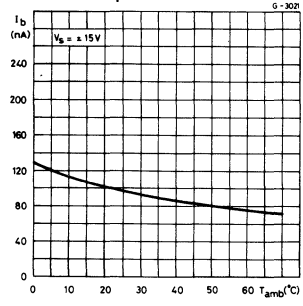


Fig. 10 - Input resistance vs. ambient temperature

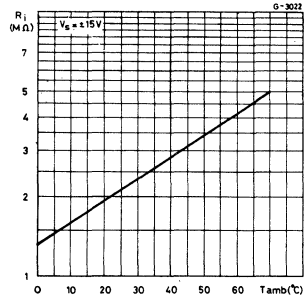


Fig. 11 - Output short-circuit current vs. ambient temperature

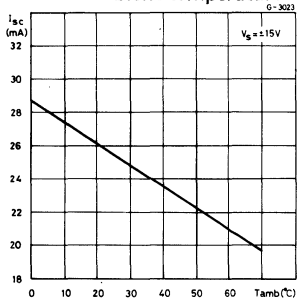


Fig. 12 - Input offset current vs. ambient temperature

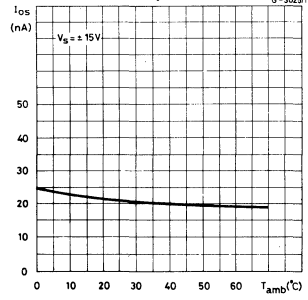


Fig. 13 - Power consumption vs. ambient temperature

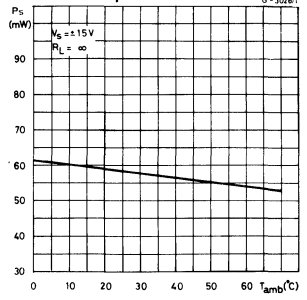
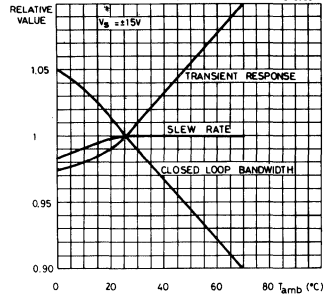


Fig. 14 - Frequency characteristics vs. ambient temperature



Typical performance curves for LS 148 and LS 148C

Fig. 15 - Open loop voltage gain vs. supply voltage

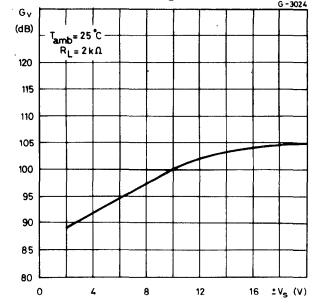


Fig. 16 - Output voltage swing vs. supply voltage

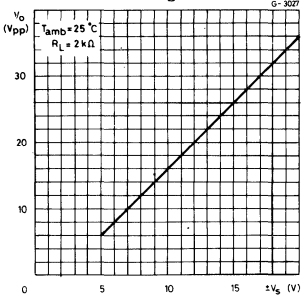


Fig. 17 - Power consumption vs. supply voltage

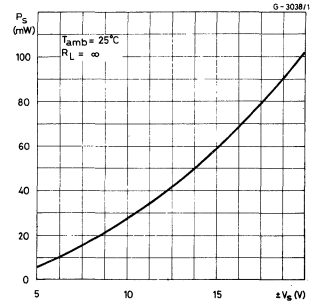


Fig. 18 - Output voltage swing vs. load resistance

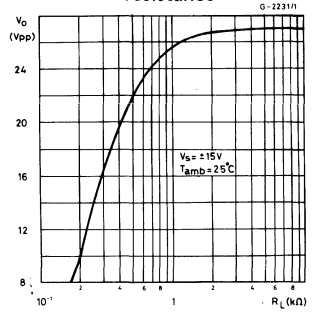


Fig. 19 - Input offset current vs. supply voltage

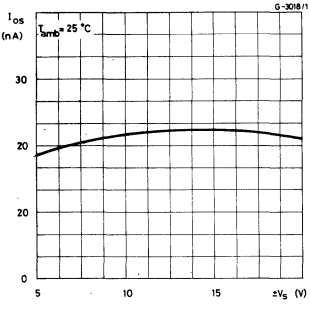


Fig. 20 - Input common mode voltage range vs. supply voltage

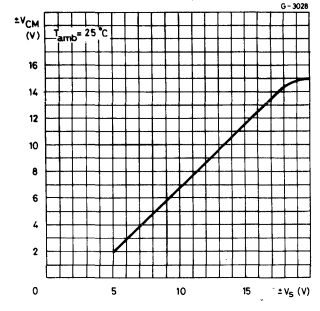


Fig. 21 - Input noise voltage vs. frequency

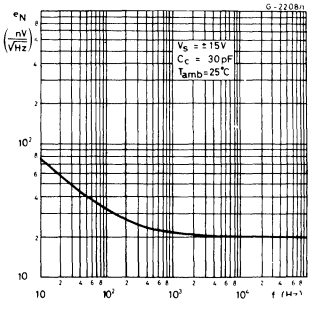


Fig. 22 - Input noise current vs. frequency

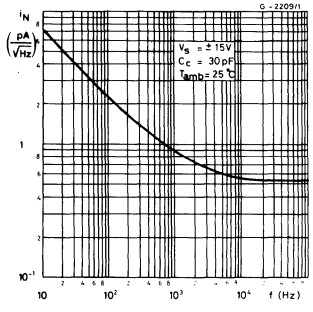


Fig. 23 - Broadband noise for various bandwidths

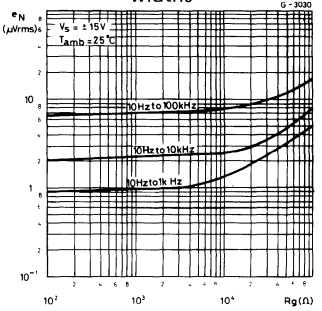


Fig. 24 - Open loop frequency and phase response vs. frequency

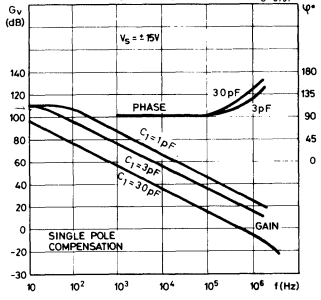


Fig. 25 - Output voltage swing vs. frequency

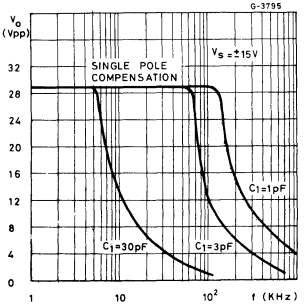


Fig. 26 - Slew-rate

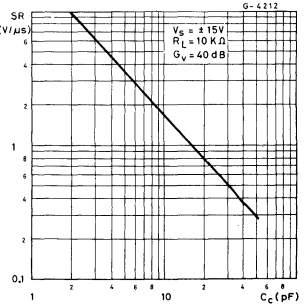


Fig. 27 - Compensation capacitance vs. closed loop voltage gain

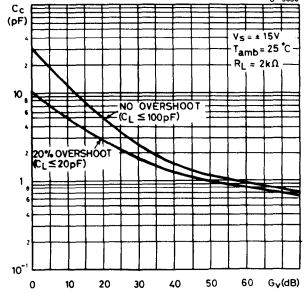


Fig. 28 - Input resistance and input capacitance vs. frequency

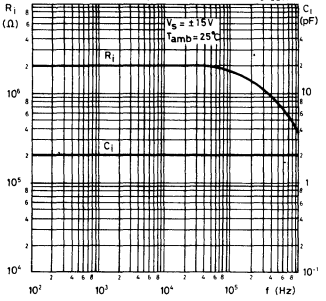


Fig. 29 - Output resistance vs. frequency

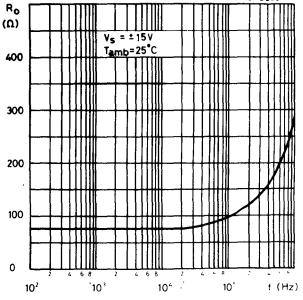


Fig. 30 - Frequency characteristics vs. supply voltage

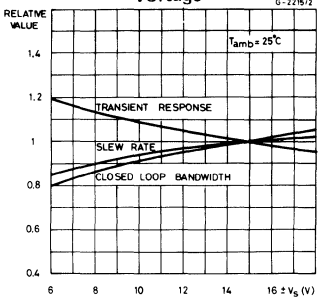


Fig. 31 - Voltage follower transient response (unity gain)

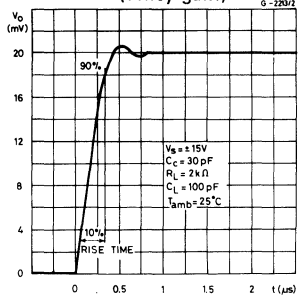


Fig. 32 - Transient response test circuit

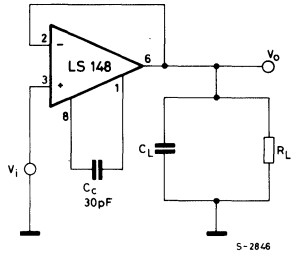


Fig. 33 - Voltage follower large-signal pulse response

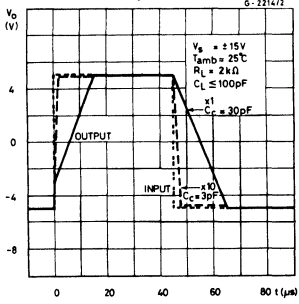


Fig. 34 - Feed forward compensation

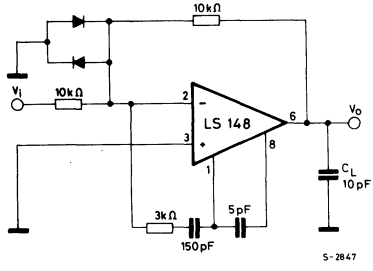
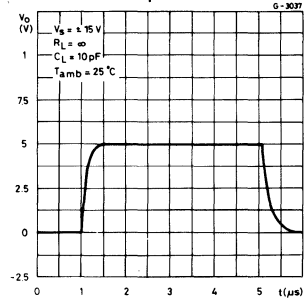
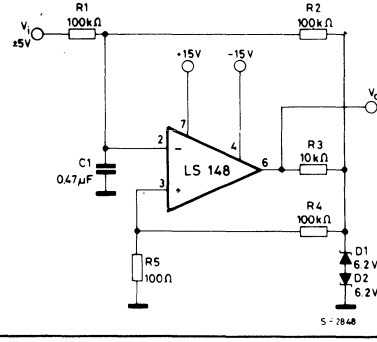


Fig. 35 - Large signal feed forward transient response



TYPICAL APPLICATIONS

Fig. 36 - Pulse width modulator



$$f_c = \frac{1}{2\pi R2\,C1}$$

$$f_n = \frac{1}{2\pi R1\,C1} = \frac{1}{2\pi R2\,C2}$$

$f_c < f_n < f_{unity\ gain}$

LINEAR INTEGRATED CIRCUIT

LS150

HIGH PERFORMANCE 80 dB COMPANDOR

The LS150 is a monolithic integrated circuit in 14-lead dual in-line ceramic and plastic packages; it performs signal level expansion in an 80-dB range [with an overall accuracy of ± 0.2 dB in a 60 dB range] and, when used in the feedback path of an operational amplifier, it performs complementary signal compression. The LS150 has been designed to improve audio channel signal-to-noise ratio according to CCITT recommendations which require an unaffected reference level of-14 dBm across 600Ω. The device can also be used to reduce crosstalk and may be converted into a unity gain amplifier for data transmission links by means of a simple switch without affecting output and input impedance levels. Another possible application is as a **noise reducer and dynamic range expandor** in cassette tape recorders and intercoms.

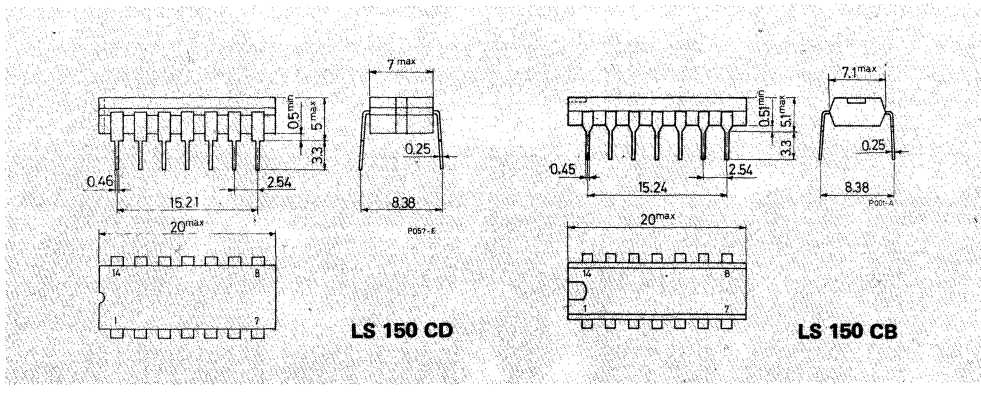
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	24	V
I_{5-6}	Differential current between pins 5 and 6	20	mA
V_i	Common mode input voltage	V_s	
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C
T_{op}	Operating temperature	-20 to 85	°C

ORDERING NUMBERS: LS150 CD (Ceramic package)
LS150 CB (Plastic package)

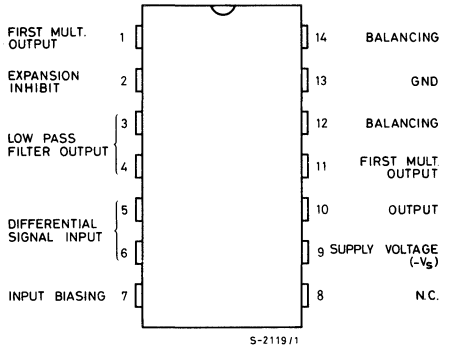
MECHANICAL DATA

Dimensions in mm

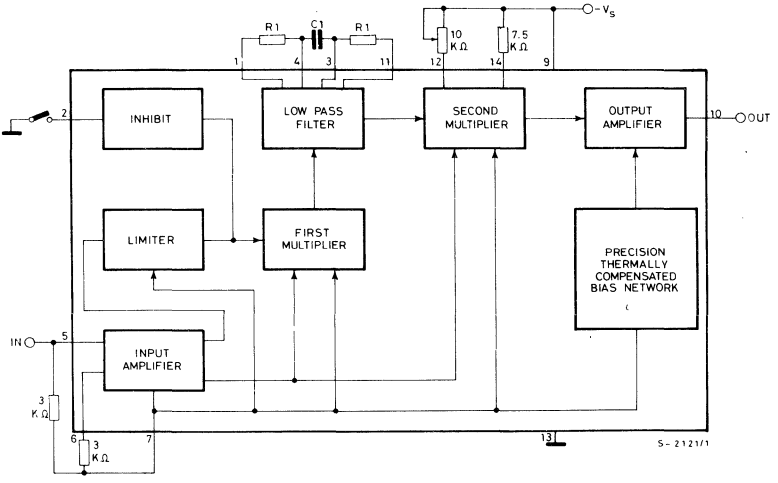


LS150

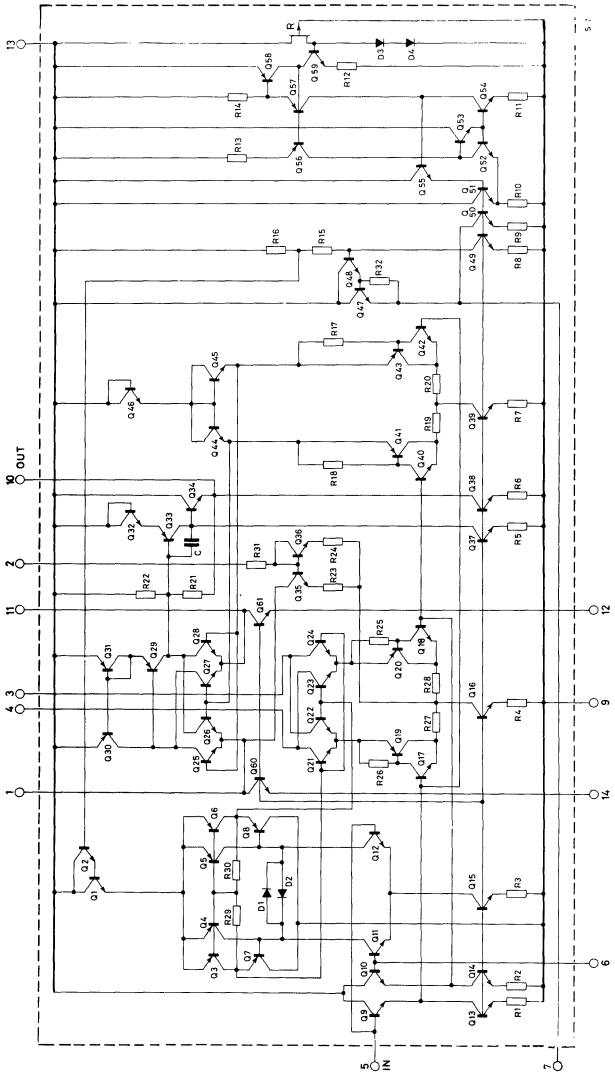
CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

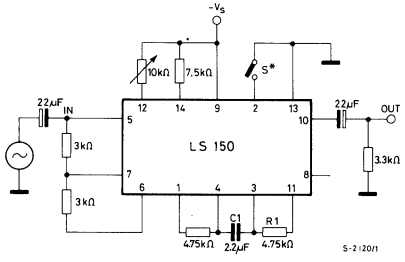
			Plastic	Ceramic
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W	120 °C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit of fig. 1, $-V_s = -12V$; $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current			5	8	mA
R_7	Input dynamic biasing resistance (pin 7)	$L_i = -14$ dBv f = 800 Hz External time constant 2 R1 • C1 = 20 ms		60	90	Ω
G_v	Gain		-1	0	+1	dB
ΔG_v	Gain variation	T_{amb}= 5 to 55°C $\Delta V_s = \pm 2\%$		±0.2 ±0.03		dB dB
B	Bandwith (-3 dB)			500		KHz
R_o	Output resistance	$L_i = -14$ dBv f = 800 Hz		25	60	Ω
R_i	Input resistance (pin 5)			100		KΩ
d	Distortion			0.7		%
d_3	Two-tone third order intermodulation	f_1 = 900 Hz f_2 = 1020 Hz $V_1 = V_2 = 88$ mV		0.5		%
e_N	Output noise in psophometric band			-100		dBm
$\Delta \lvert G \rvert$	Expansion accuracy after balancing	L_i = -40 to -10 dBv, f = 800 Hz T_{amb}= 5 to 55°C , f = 800 Hz		0.1 0.2	0.2 0.3	dB dB
I_{off}	Inhibit current consumption (pin 2)			0.3	1	mA
G	Amplifier gain	Inhibit ON (pin 2 grounded) f = 800 Hz	-1.5	0	+1.5	dB

TEST AND APPLICATION CIRCUITS

Fig. 1 - Expandor circuit



(*) S closed : unity gain amplifier.
S open : expandor.

Fig. 2 - Compressor circuit

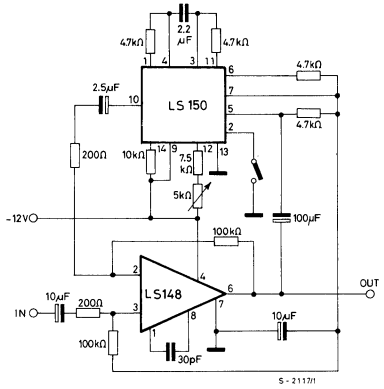


Fig. 3 - Compandor Characteristics

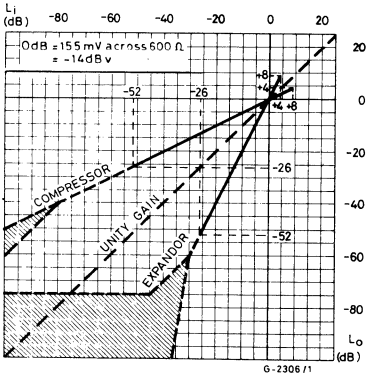


Fig. 4 - Comparison between LS150 performance (curve A) and limits from CCITT recommendation (curve B) - Green Book - Geneva 1972 - G162.

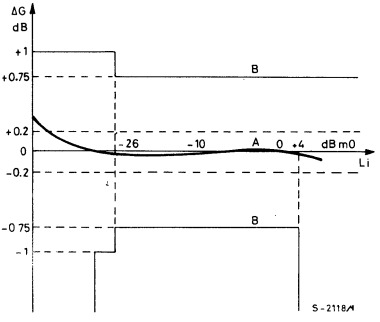


Fig. 5 - Expandor gain vs. temperature

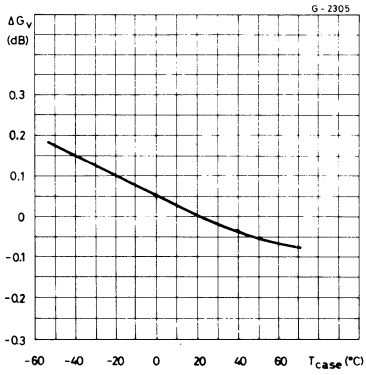
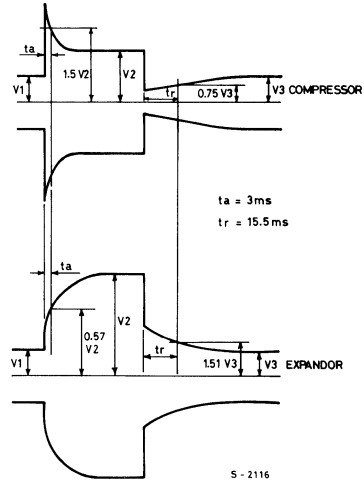


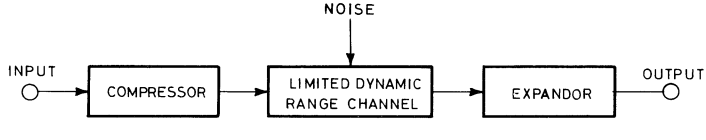
Fig. 6 - Transient response

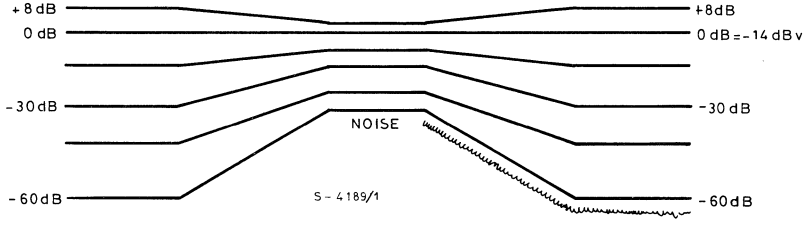


APPLICATION INFORMATION

The fig. 7 shows the basic configuration (with relative signal levels) of a compandorized system.
It is clear the action against the line noise: the system using a compressor in sending and an expandor in receiving can improve very much the signal-to-noise ratio, especially with very high noise lines.
By using the LS150 it is possible to built both the compressor and the expandor blocks.

Fig. 7 - Compandorized system.

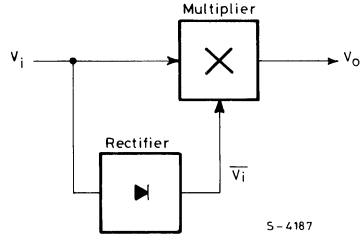




APPLICATION INFORMATION (continued)

The basic block diagram of an expandor is shown in fig. 8. The product of the input voltage V_i and its mean value $\overline{V_i}$ (obtained from the rectifier with time constant τ) is supplied at the output of an "ideal" multiplier.

Fig. 8 - Basic expandor circuit.



The output voltage V_o is proportional to the product of V_i and $\overline{V_i}$:

$$V_o = KV_i \times \overline{V_i}$$

where K is a factor that defines a level for unity gain.
For a constant input level,

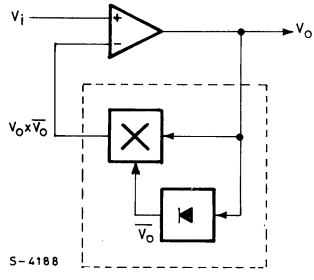
$$\overline{V_o} = K\overline{V_i} \times \overline{V_i} = K\overline{V_i}^2$$

Expressing all levels in decibels relative to a reference level:

$$\overline{V_o}\ (\text{dB}) = 20 \log_{10} \overline{V_i}^2 = 2\,\overline{V_i}\ (\text{dB}).$$

Signals with an input level equal to the reference level are unaffected by the expandor while higher levels are raised and lower levels attenuated. It is recommended by CCITT, and practically advantageous, that the unaffected level be - 14 dBv, a voltage corresponding to -14 dBm across 600Ω. A time constant for the average rectifier of 20 ms is also recommended, giving "syllabic" operation of the compandor.

Fig. 9 - Basic compressor circuit.



A compressor can easily be implemented with an expandor in the feedback path of an operational amplifier (Fig. 9). Assuming infinite gain for the amplifier:

$$V_i = KV_o \times \overline{V_o}$$

and for a constant input level

$$\overline{V_o} = \sqrt{\frac{\overline{V_i}}{K}}$$

In decibels, with respect to the unaffected level,

$$\overline{V_o}\ (\text{dB}) = 20 \log_{10} (\overline{V_i})^{\frac{1}{2}} = \tfrac{1}{2}\,\overline{V_i}\ (\text{dB}).$$

APPLICATION INFORMATION (continued)

Design Constraints

There are several constraints on the design of a compandor to be used in telecommunication equipment.

Level: The reference (or unity gain) level is -14 dBv, i.e. 155 mV rms. For application in high-quality multiplexer transmission systems between exchanges, and expansion accuracy better than 0.2 dB in the same range (+40 to -25 dBmo) considered by CCITT for all operating conditions is required. These parameters had to be compatible with mass production manufacturing techniques. Particularly when taking into account the low signal levels, this requirement is very demanding. It was the main target in designing the device and had a strong influence on the fabrication process, circuit configurations, and layout.

Power Supply: The circuit has to operate with a single 12V negative supply, unregulated, and with relatively high noise.

Input Impedance: This has to be precisely defined by an external resistor, which is the passive termination of an LC filter before the expandor. Thus the input impedance of the IC must be very high. A differential input stage is preferable to reduce ground loop noise.

Gain: The expandor (or compressor) shall not modify the level diagram of existing channel modems, already optimized for crosstalk and noise. This means that the gain at the unaffected level shall be 0 dB, with small spread.

Inhibition: It must be possible to inhibit the operation of the compandor for testing and maintenance purpose, and to allow the transmission of telegraph channels.

Definition of units

dBmo : power level ($10 \log \frac{P_2}{P_1}$) is expressed in dBm when P_1 is 1 mW, therefore 0 dBm = 1 mW.

dBm : the power is expressed in dBmo when referred to an established power level in the circuit, generally the output signal level.

e.g.: if the output level is -15 dBm and this level is chosen as reference, then 0 dBmo = -15 dBm; if another signal, i.e. the distortion measured at the same point of the circuit, is -90 dBm, then the distortion is -75 dBmo.

dBv : $20 \log \frac{V_2}{V_1}$ when $V_1 = 775$ mVrms.

LINEAR INTEGRATED CIRCUIT

LS156

PRELIMINARY DATA

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

The LS156 is a monolithic integrated circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically piezoceramic capsules, but the device can work also with dynamic ones). Many of its electrical characteristics can be controlled by means of external components to meet different specifications. In addition to the speech operation, the LS156 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).
The LS156 basic functions are the following:

- It presents the proper DC path for the line current.
- It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing the line length through the line current.
- It acts as linear interface for MF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated by the M761.

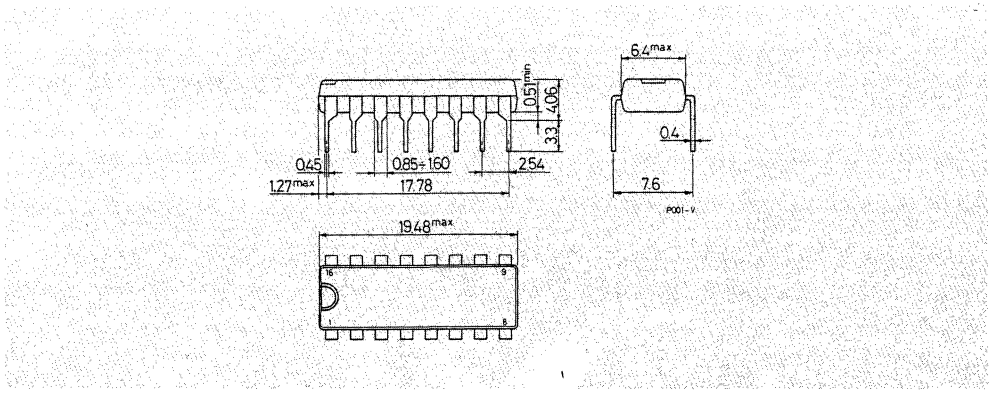
ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb}= 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

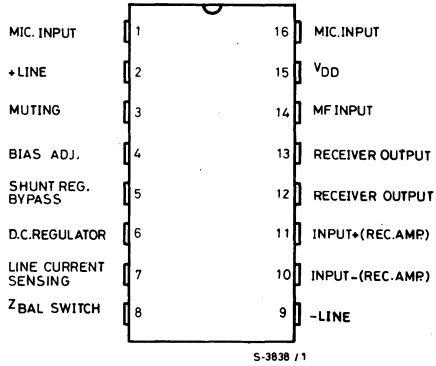
ORDERING NUMBER: LS 156B

MECHANICAL DATA

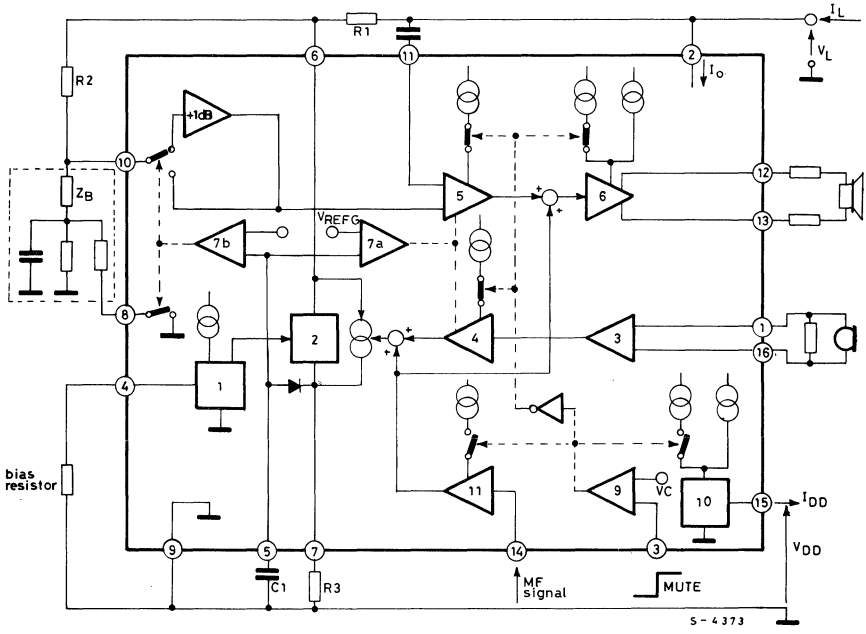
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST CIRCUITS

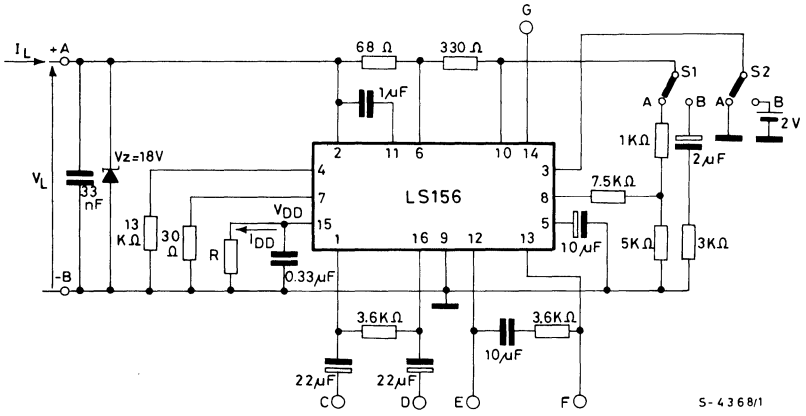
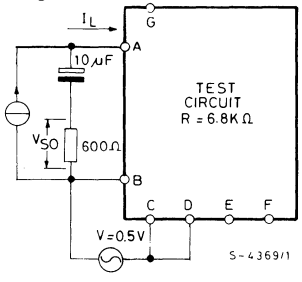
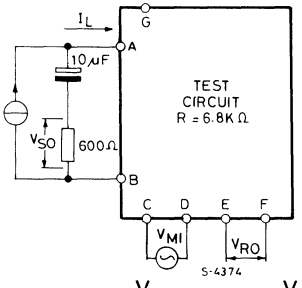


Fig. 1



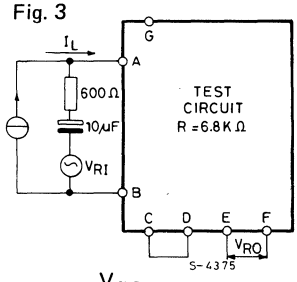
V = 0,5V; CMRR

Fig. 2



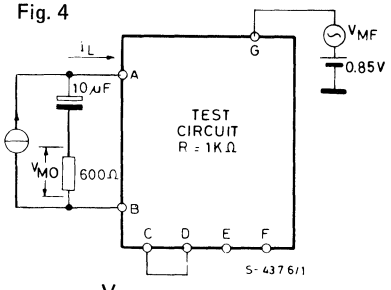
Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_s = \frac{V_{SO}}{V_{MI}}$

Fig. 3



$G_R = \frac{V_{RO}}{V_{RI}}$

Fig. 4



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, S1 and S2 in (a), T_{amb} = -25 to +50°C, f = 200 to 3400 Hz, unless otherwise specified)

Parameter		Test condition		Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION								
V_L	Line voltage	T_{amb}= 25°C	I_L= 12 mA I_L= 20 mA I_L= 80 mA	3.9		4.7 5.5 12.2	V	–
CMRR	Common mode rejection	f = 1 KHz	I_L= 12 to 80 mA	50			dB	1
G_s	Sending gain	T_{amb}= 25°C f = 1 KHz V_{MI}= 2 mV	I_L= 52 mA I_L= 25 mA	44 48	45 49	46 50	dB	2
	Sending gain flatness	V_{MI}= 2 mV	f_{ref}= 1 KHz I_L= 12 to 80 mA			± 1	dB	2
	Sending distortion	f = 1 KHz I_L= 12 to 80 mA	V_{so}= 1V V_{so}= 1.3V			2 10	%	2
	Sending noise	V_{MI}= 0V	I_L= 40 mA		-70		dBmp	2
	Microphone input impedance pin 1-16	V_{MI}= 2 mV	I_L= 12 to 80 mA	40			KΩ	
	Sending loss in MF operation	V_{MI}= 2 mV S_2 in (b)	I_L= 52 mA I_L= 25 mA	-30 -30			dB	2
G_R	Receiving gain	V_{RI}= 0.3V f = 1 KHz T_{amb}= 25°C	I_L= 52 mA I_L= 25 mA	3 7	4 8	5 9	dB	3
	Receiving gain flatness	V_{RI}= 0.3V	f_{ref}= 1 KHz I_L= 12 to 80 mA			± 1	dB	3
	Receiving distortion	f = 1 KHz	I_L= 12 mA V_{RO}= 1.6V I_L= 12 mA V_{RO}= 1.9V I_L= 50 mA V_{RO}= 1.8V I_L= 50 mA V_{RO}= 2.1V			2 10 2 10	%	3
	Receiving noise	V_{RI}= 0V	I_L= 12 to 80 mA		150		μV	3
	Receiver output impedance pin 12-13	V_{RO}= 50 mV	I_L= 40 mA			100	Ω	
	Sidetone	f = 1 KHz T_{amb}= 25°C S_1 in (b)	I_L= 52 mA I_L= 25 mA			36 36	dB	2
Z_{ML}	Line matching impedance	V_{RI}= 0.3V	f = 1 KHz I_L= 12 to 80 mA	500	600	700	Ω	3

ELECTRICAL CHARACTERISTICS (continued)

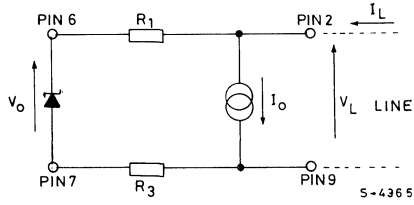
Parameter		Test condition	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF supply voltage Stand by	I_L= 12 to 80 mA	2.4	2.5		V	–
I_{DD}	MF supply current Stand by Operation	I_L= 12 to 80 mA I_L= 12 to 80 mA; S_2 in (b)	0.5 2			mA	–
	MF amplifier gain	I_L= 12 to 80 mA $f_{MF\ in}$= 1 KHz $V_{MF\ in}$= 80 mV	15		17	dB	4
V_i	DC input voltage level (pin 14)	$V_{M\ Fin}$= 80 mV		.3V_{DD}		V	–
R_i	Input impedance (pin 14)	$V_{M\ Fin}$= 80 mV	60			KΩ	–
d	Distortion	$V_{M\ Fin}$= 110 mV I_L= 12 to 80 mA			2	%	4
	Starting delay time	I_L= 12 to 80 mA			5	ms	–
	Muting threshold voltage (pin 3)	Speech operation			1	V	–
		MF Operation	1.6			V	–
	Muting stand by current (pin 3)	I_L= 12 to 80 mA			-10	μA	–
	Muting operating current (pin 3)	I_L= 12 to 80 mA S_2 in (b)			+10	μA	–

CIRCUIT DESCRIPTION

1. DC characteristic

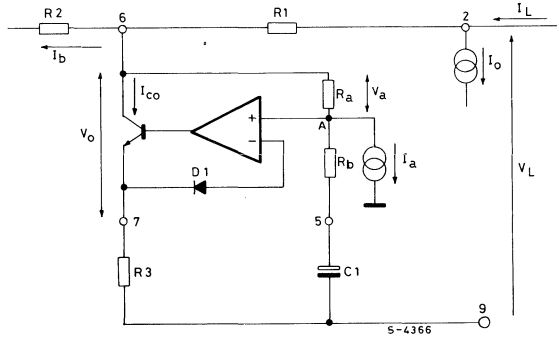
In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristics V_L, I_L.
The DC characteristic of the LS 156 it is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3. The equivalent circuit of the total system is shown in fig. 5.

Fig. 5 - Equivalent DC load to the line



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit.
The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).
The recommended minimum of I_o is 7.5 mA.
The voltage $V_o \cong 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Fig. 6 - Circuit configuration of the shunt regulator



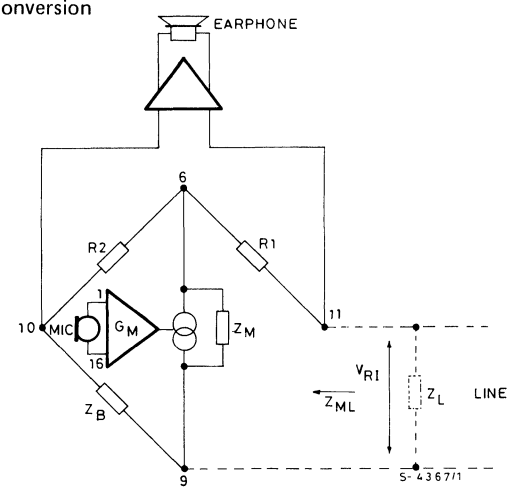
CIRCUIT DESCRIPTION (continued)

The difference $I_L - I_o$ flows through the shunt regulator being I_b negligible.
I_a is an internal constant current generator; hence $V_o = V_{BED1} + I_a \cdot R_a \cong 3.8V$. The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.
It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_{BED1} \cong (I_L - I_o)\, R_3 + V_{BED1}$).

2. 2/4 wires conversion

The LS156 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 7).

Fig. 7 - Two to four wires conversion



For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B \gg Z_L$); the main part is sent to the line via R_1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6\text{-}9}}{\Delta I_{6\text{-}9}}$.

From fig. 6, considering C_1 as a short circuit for AC signal, any variation ΔV_6 generates a variation.

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

CIRCUIT DESCRIPTION (continued)

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R_3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R_1 + Z_M \,//\, (R_2 + Z_B)$$

By choosing $Z_M \gg R_1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R_1 (of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must be always valid).

The received signal is related to R_1 value according to the approximated relationship

$$V_R = 2 \cdot V_{RI} \frac{R_1}{R_1 + Z_M}$$

Note that by changing the value of R_1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. Automatic gain control

The LS156 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation by sensing the line length through the line current.
The line current is sensed across R_3 (see fig. 6) and transferred to pin 5 by the regulator.

$$V_5 = V_{BED1} + V_7 \cong V_{BED1} + (I_L - I_o) \cdot R_3.$$

The pin 5 V_5 voltage, after a comparison with an internal reference V_{REFG} (see the block diagram) is used to modify the gain of the amplifiers (4) and (5) on both the sending and receiving path.
The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.
Minimum gain is reached for a line current of about 52 mA for the same drain current $I_o = 7.5$ mA.
When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.
Automatic switching of the balance network Z_B for a better sidetone is performed by the LS156 through V_5 information. This information, proportional to the line length, drives the comparator (7b) (see the block diagram).
For long lines, the impedance level of Z_B is high (pin 8 open) and the additional +1 dB gain is added to the receiving amplifier chain.

CIRCUIT DESCRIPTION (continued)

For short lines, the impedance level of Z_B is automatically switched to a lower value (pin 8 shorted to ground) and the additional +1 dB block is bypassed by the received signal.
A built in hysteresis circuit avoids uncertain operation of the comparator.

4. Transducers interfacing

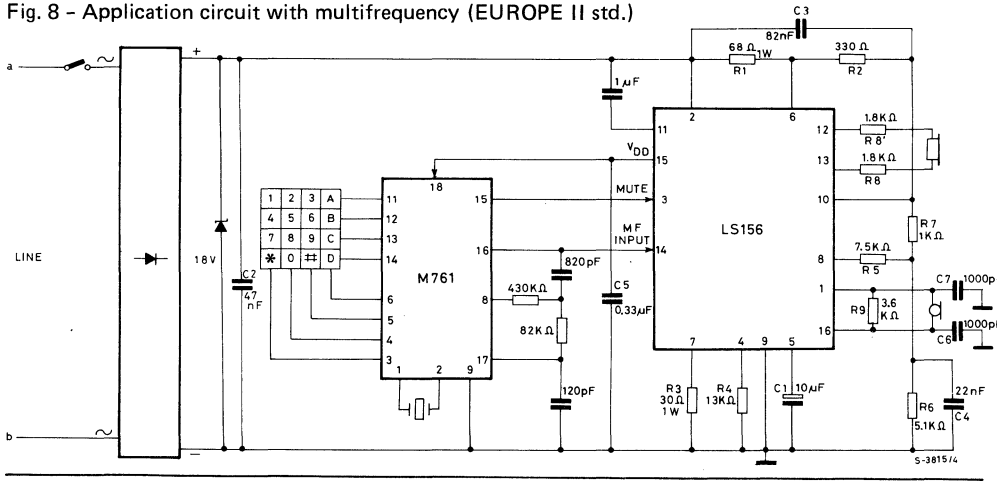
The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistors without affecting the sending gain.
The receiving output stage (6) is particularly intended to drive piezoceramic capsules. [Low output impedance (100Ω max); high voltage swing (close to V_L); current capability of 1.8 mAp].
When a dynamic capsule is used, it is useful to decrease the receiving gain by decreasing R_1 value (see the relationship for V_R).
With very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency interfacing

The LS156 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.
When no key of the keyboard is pressed the mute state is low and the LS156 feeds the M761 through pin 15 with low current (standby operation of the M761). The oscillator of the M761 is not operating.
When one key is pressed, the M761 sends a "high state" mute condition to the LS156. A voltage comparator (9) of LS156 drives internal electronic switches: the current delivered by the voltage supply (10) is increased to allow the operation of the oscillator. This extra current is diverted by the receiving and sending section of the LS156 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.
A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber; the MF amplifier (11) delivers the dial tones to the sending paths.
The application circuit shown in fig. 9 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm), an external divider must be used (fig. 11).
The mute function can be used also when a temporary inhibition of the output signal is requested.

APPLICATION INFORMATION

Fig. 8 - Application circuit with multifrequency (EUROPE II std.)



APPLICATION INFORMATION (continued)

Fig. 9 - Application circuit with multifrequency (EUROPE I std.)

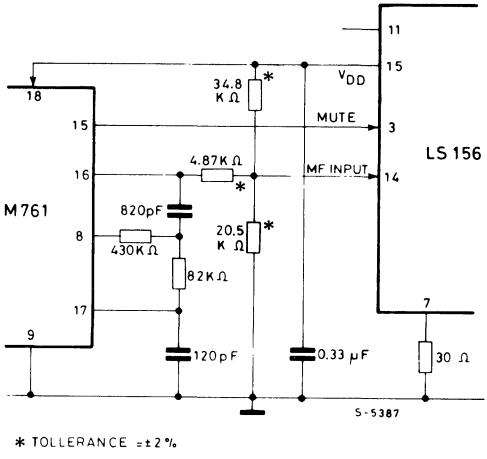


Fig. 10 - External mute function

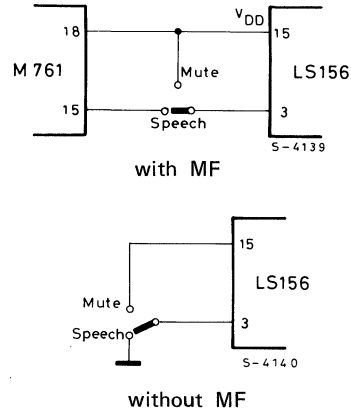
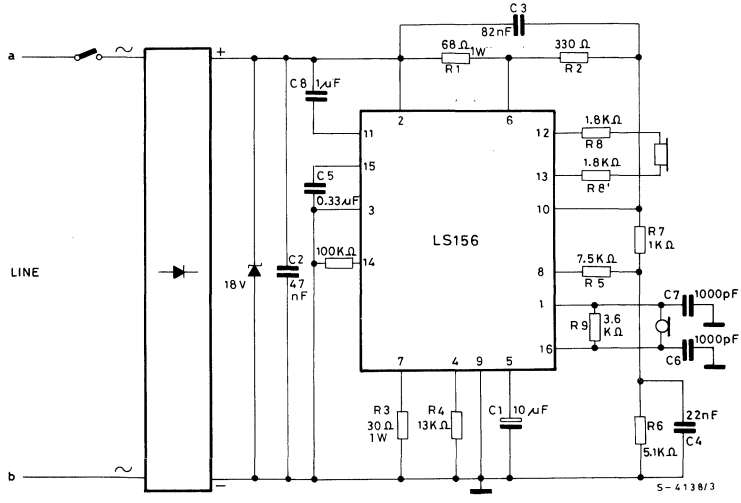


Fig. 11 - Application circuit without multifrequency.



The circuits shown in fig. 8 and fig. 11 are referred to the Italian standard. The fig. 10 shows the connection for mute function (inhibition of the output stage when it is requested) by using an external switch at pin 3.
Different values for the external components can be used in order to satisfy different requirements. The following table can help the designer.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
R_1	68 Ω	Bridge Resistors	R_1 controls the receiving gain. The ratio R_2/R_1 fixes the amount of signal delivered to the line. R_1 helps in fixing the DC characteristic (see R_3 note).
R_2	330 Ω		
R_3	30 Ω	Line current sensing. Fixing DC characteristic.	The relationships involving R_3 are: • $Z_{ML} = (20\ R_3\ //\ Z_B) + R_1$ • $G_s = K \cdot \frac{Z_L\ //\ Z_{ML}}{R_3}$ • $V_L = (I_L - I_o)\ (R_3 + R_1) + V_o$; V_o= 3.8V. Without any problem it is possible to have a Z_{ML} ranging from 500 up to 900 Ω.
R_4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R_4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (See fig. 12).
R_5	7.5 KΩ	Balance Network	The balance network has two possible impedance levels, selected by the circuit referring to the line current (i.e. to the line length) in order to optimize the sidetone. It's possible to change R_5, R_6, R_7 values in order to improve the matching to different lines; in any case: $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ with the two possible values for Z_B: $Z_{B(1)} = R_7 + R_6\ //\ C_4$ (long lines) $Z_{B(2)} = R_7 + (R_6\ //\ R_5)\ //\ C_4$ (short lines) (see fig. 13).
R_6	5.1 KΩ		
R_7	1 KΩ		
$R_8 - R_8'$	1.8 KΩ	Receiver impedance matching	R_8 and R_8' must be equal; the suggested value is good for matching to piezoceramic capsule; there is no problem in increasing and decreasing (down to 0 Ω) this value, but when low resistance levels are used a DC decoupling must be inserted to stop the current due to the receiver output offset voltage (max 400 mV).
R_9	3.6 KΩ	Microphone impedance matching	The suggested value is typical for a piezoceramic microphone, but it is possible to choose R_9 in a wide range.
C_1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency.
C_2	47 nF	Matching to a capacitive line	C_2 changes with the characteristics of the transmission line.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
C_3	82 nF	Receiving gain flatness.	C_3 depends on balancing and line impedance versus frequency.
C_4	22 nF	Balance network.	See note for R_7, R_6, R_5.
C_5	0.33 μF	DC filtering	The C_5 range is from 0.1 μF to 0.47 μF. The lowest value is ripple limited, the higher value is starting up time limited.
C_6 - C_7	1000 pF	RF bypass.	
C_8	1 μF	DC decoupling for receiving input.	

Fig. 12 - Sending and receiving gain vs. line current

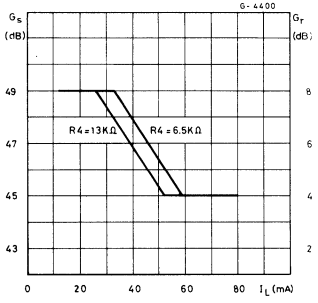
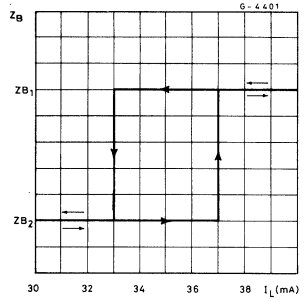


Fig. 13 - Balance network impedance vs. line current



LINEAR INTEGRATED CIRCUIT

LS159

HIGH RELIABILITY TRANSISTOR ARRAY

The LS159 is an array of 5 NPN transistors on a common monolithic substrate in an SO-14 (14-lead plastic micropackage). This package is easily mounted on thick and thin film hybrid circuits. Two transistors are internally connected to form a differential amplifier. The transistors of the LS159 are well suited to low noise general purposes and to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete components in conventional circuits; in addition they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The device is also available with a ermetic goldchip (LS8159M) that is particularly suitable for professional and telecom applications, wherever very high MTBF are required. This performance is guaranteed by silicon nitride sealing of chip surface and Ti-Pt-Au metallization, protected with a double passivated layer, providing resistance against contamination, electrolytic corrosion and electromigration.

ABSOLUTE MAXIMUM RATINGS

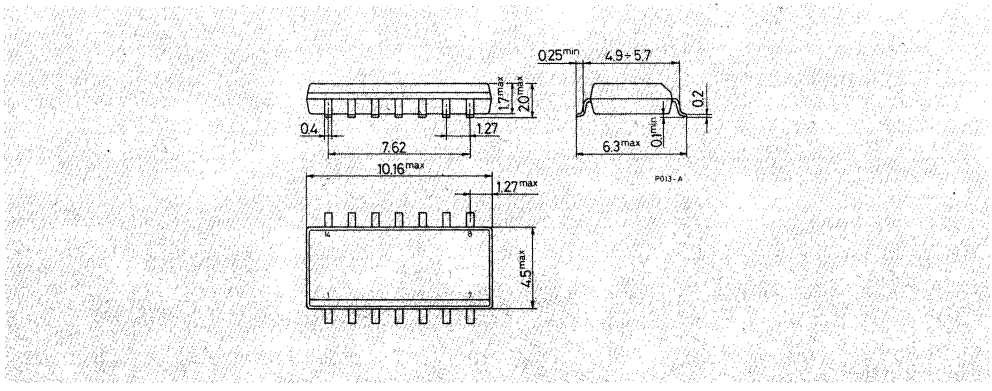
		Each transistor	Total package
V_{CBO}	Collector-base voltage ($I_E = 0$)	20 V	–
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	15 V	–
V_{CSS}*	Collector--substrate voltage	20 V	–
V_{EBO}	Emitter-base voltage ($I_C = 0$)	5 V	–
I_C	Collector current	50 mA	–
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	250 mW	500 mW
T_{stg}, T_j	Storage, and junction temperature	-55 to 150 °C	
	Soldering dip or wave at 5 s	260 °C	
	11 s	235 °C	

*) The collector of each transistor of the LS159 is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ORDERING NUMBERS: LS 159M – LS 8159M

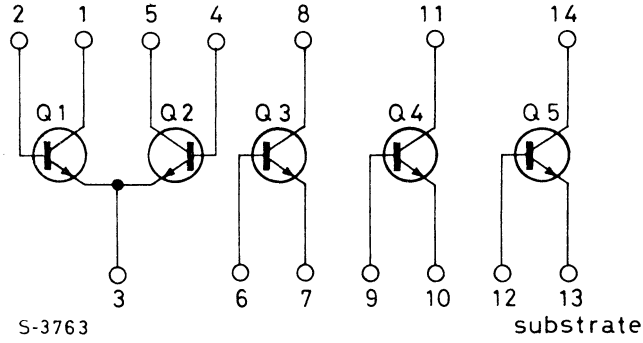
MECHANICAL DATA

Dimensions in mm



LS159

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	250	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB}= 10V		0.002	40	nA	1
I_{CEO}	Collector cutoff current (I_B = 0)	V_{CE}= 10V		see curve	0.5	μA	2
$\lvert I_{B1}-I_{B2}\rvert$	Input offset current	I_C = 1 mA V_{CE}= 3V		0.3	2	μA	7
V_{CBO}	Collector-base voltage (I_E = 0)	I_C = 10 μA	20	60		V	—
V_{CEO}	Collector-emitter voltage (I_B = 0)	I_C = 1 mA	15	24		V	—
V_{CSS}	Collector-substrate voltage (I_{CSS}= 0)	I_C = 10 μA	20	60		V	—
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 10 mA I_B = 1 mA		0.23		V	—

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
V_{EBO}	Emitter-base voltage ($I_C = 0$)	$I_E = 10\ \mu A$	5	7		V	–
V_{BE}	Base-emitter voltage	$I_E = 1$ mA $V_{CE} = 3V$ $I_E = 10$ mA $V_{CE} = 3V$		0.71 0.8		V V	4
$\lvert V_{BE1}-V_{BE2}\rvert$	Input offset voltage	$I_C = 1$ mA $V_{CE} = 3V$		0.45	5	mV	4-6
$\lvert V_{BE3}-V_{BE4}\rvert$	Input offset voltage						
$\lvert V_{BE4}-V_{BE5}\rvert$	Input offset voltage						
$\lvert V_{BE5}-V_{BE4}\rvert$	Input offset voltage						
$\frac{\Delta V_{BE}}{\Delta T}$	Base-emitter voltage temperature coefficient	$I_C = 1$ mA $V_{CE} = 3V$		-1.9		mV/°C	5
$\frac{\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T}$	Input offset voltage temperature coefficient	$I_C = 1$ mA $V_{CE} = 3V$		1.1		µV/°C	6
h_{FE}	DC current gain	$I_C = 10$ mA $V_{CE} = 3V$ $I_C = 1$ mA $V_{CE} = 3V$ $I_C = 10\ \mu A$ $V_{CE} = 3V$	40	100 100 54		– – –	3
f_T	Transition frequency	$I_C = 3$ mA $V_{CE} = 3V$	300	550		MHz	14
NF	Noise figure	$I_C = 100\ \mu A$ $V_{CE} = 3V$ $R_g = 1\ k\Omega$ $f = 1$ kHz		3.25		dB	8
h_{ie}	Input impedance	$I_C = 1$ mA $V_{CE} = 3V$ f = 1 KHz		3.5		kΩ	9
h_{fe}	Forward current transfer ratio			110		–	
h_{re}	Reverse voltage transfer ratio			1.8×10^{-4}		–	
h_{oe}	Output admittance			15.6		µS	
y_{ie}	Input admittance	$I_C = 1$ mA $V_{CE} = 3V$ f = 1 MHz		0.3+j0.04		mS	11
y_{fe}	Forward transadmittance			31-j1.5		mS	10
y_{re}	Reverse transadmittance			see curve		mS	13
y_{oe}	Output admittance			0.001+j0.03		mS	12
C_{EBO}	Emitter-base capacitance	$I_C = 0$ $V_{EB} = 3V$		0.6		pF	–
C_{CBO}	Collector-base capacitance	$I_E = 0$ $V_{CB} = 3V$		0.58		pF	–
C_{CSS}	Collector-substrate capacitance	$I_C = 0$ $V_{CSS} = 3V$		2.8		pF	–

Fig. 1 - Collector cutoff current vs. ambient temperature

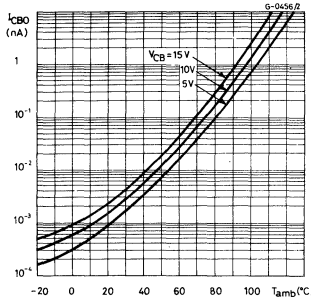


Fig. 2 - Collector cutoff current vs. ambient temperature

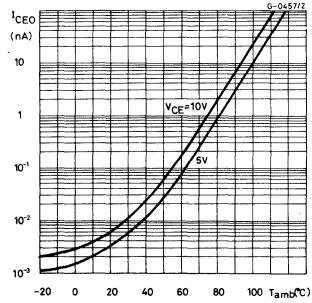


Fig. 3 - DC current gain

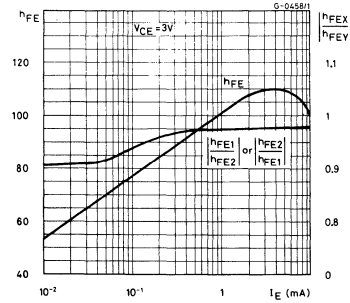


Fig. 4 - Input voltage and input offset voltage vs. emitter current

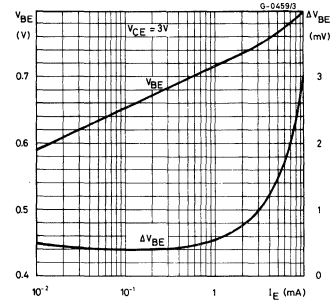


Fig. 5 - Input characteristics for each transistor

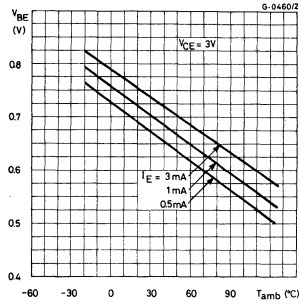


Fig. 6 - Input offset voltage vs. ambient temperature

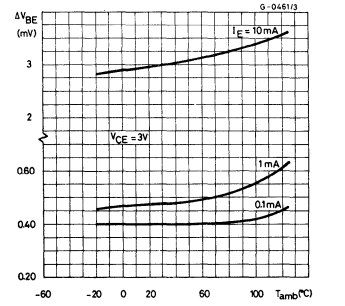


Fig. 7 - Input offset current for matched transistor pair

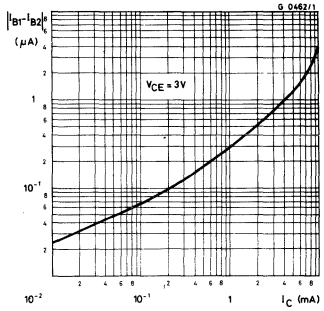


Fig. 8 - Noise figure vs. collector current

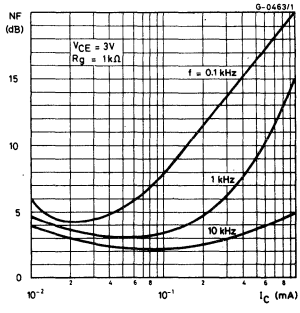


Fig. 9 - Normalized h parameters vs. collector current

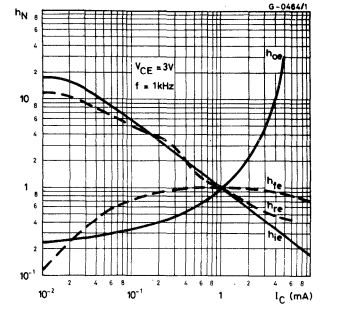


Fig. 10 - Forward admittance vs. frequency

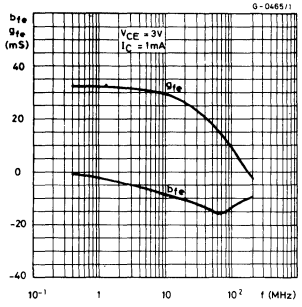


Fig. 11 - Input admittance vs. frequency

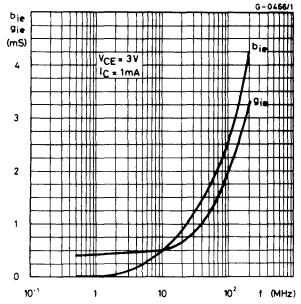


Fig. 12 - Output admittance vs. frequency

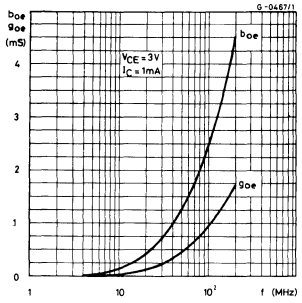


Fig. 13 - Reverse admittance vs. frequency

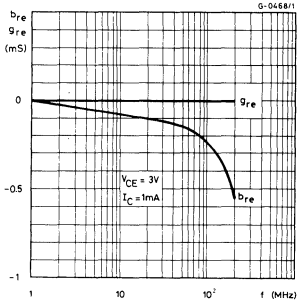
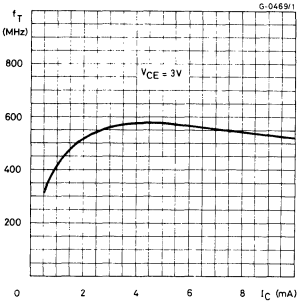


Fig. 14 - Transition frequency vs. collector current



LS204
LS204A
LS204C

LINEAR INTEGRATED CIRCUITS

HIGH PERFORMANCE DUAL OPERATIONAL AMPLIFIER

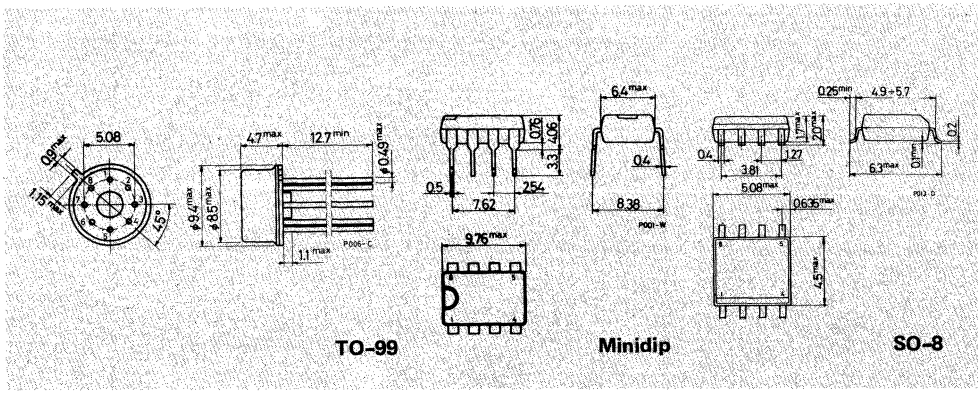
- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

The LS 204 is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.). The LS 204 series is available with hermetic gold chip (8000 series).

ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	μpackage
V_s	Supply voltage		± 18V	
V_i	Input voltage		$\pm V_s$	
V_i	Differential input voltage		$\pm (V_s - 1)$	
T_{op}	Operating temperature for **LS 204**		-25 to 85°C	
	LS 204A		-55 to 125°C	
	LS 204C		0 to 70 °C	
P_{tot}	Power dissipation at T_{amb} = 70°C	520 mW	665 mW	400 mW
T_j	Junction temperature	150°C	150°C	150°C
T_{stg}	Storage temperature	-65 to 150°C	-55 to 150°C	-55 to 150°C

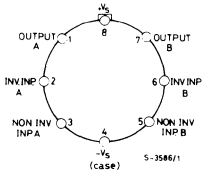
MECHANICAL DATA

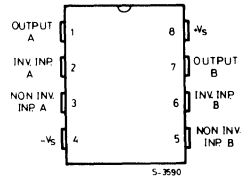
Dimensions in mm

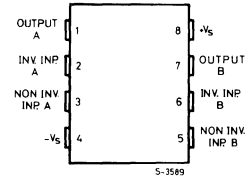


LS 204
LS 204A
LS 204C

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

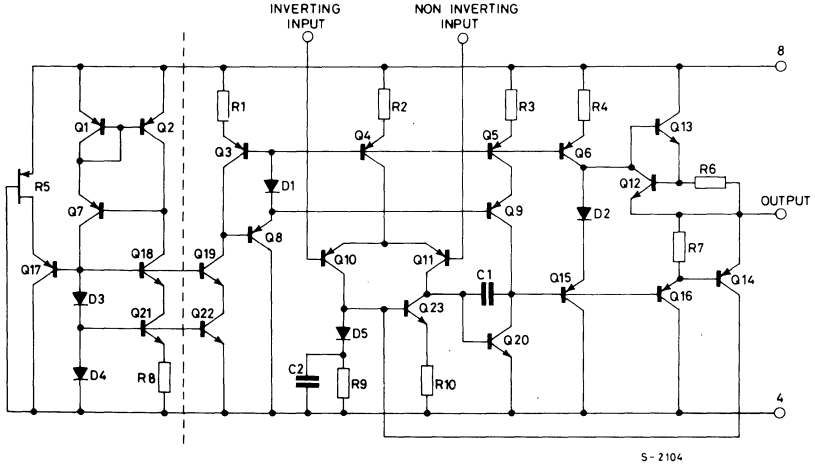






Type	TO-99	Minidip	SO-8
LS 204	LS 204 T	—	LS 204 M
LS 204 A	LS 204 AT	—	—
LS 204 C	LS 204 CT	LS 204 CB	LS 204 CM
LS 8204	—	—	LS 8204 M
LS 8204 A	—	—	LS 8204 AM
LS 8204 C	—	—	LS 8204 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25x16x96 mm)

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	LS 204/LS204A			LS 204C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			0.7	1		0.8	1.5	mA
I_b	Input bias current			50	150		100	300	nA
		$T_{min} < T_{op} < T_{max}$			300			700	nA
R_i	Input resistance	f = 1 KHz		1			0.5		MΩ
V_{os}	Input offset voltage	$R_g \leq 10$ KΩ		0.5	2.5		0.5	3.5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			3.5			5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10 KΩ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input offset current			5	20		12	50	nA
		$T_{min} < T_{op} < T_{max}$			40			100	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	$T_{min} < T_{op} < T_{max}$ R_L= 2KΩ V_s= ±15V V_s= ± 4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20 KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1 KHz R_g = 50Ω R_g = 1 KΩ R_g = 10 KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	G_v= 20 dB R_L= 2KΩ V_o= 2 Vpp f = 1 KHz		0.03	0.1		0.03	0.1	%
V_o	DC output voltage swing	R_L= 2KΩ V_s= ±15V V_s= ± 4V	±13	±3		±13	±3		V
V_o	Large signal voltage swing	R_L= 10 KΩ f = 10 KHz		28			28		Vpp
SR	Slew rate	unity gain R_L= 2KΩ	0.8	1.5			1		V/μs
CMR	Common mode rejection	V_i= 10V $T_{min} < T_{op} < T_{max}$	90			86			dB
SVR	Supply voltage rejection	V_i= 1V f = 100 Hz $T_{min} < T_{op} < T_{max}$	90			86			dB
CS	Channel separation	f = 1 KHz	100	120			120		dB

Note:

	LS 204	LS 204A	LS 204C
$T_{min.}$	-25°C	-55°C	0°C
$T_{max.}$	+85°C	+125°C	+70°C

Fig. 1 - Supply current vs. supply voltage

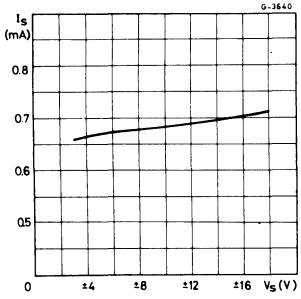


Fig. 2 - Supply current vs. ambient temperature

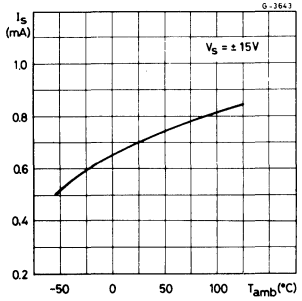


Fig. 3 - Output short circuit current vs. ambient temperature

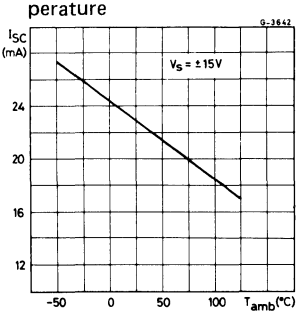


Fig. 4 - Open loop frequency and phase response

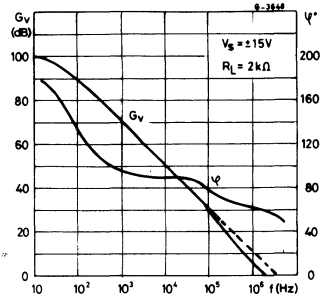


Fig. 5 - Open loop gain vs. ambient temperature

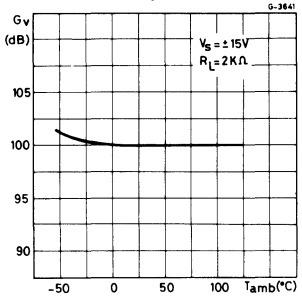


Fig. 6 - Supply voltage rejection vs. frequency

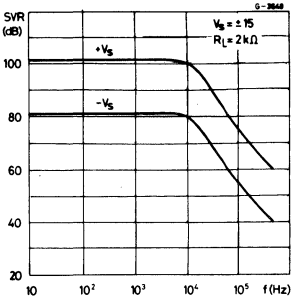


Fig. 7 - Large signal frequency response

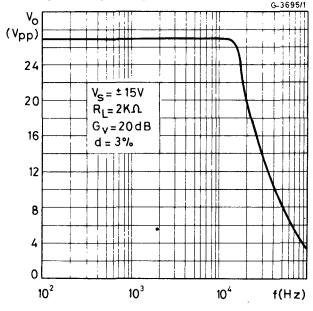


Fig. 8 - Output voltage swing vs. load resistance

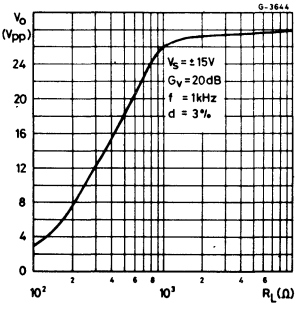
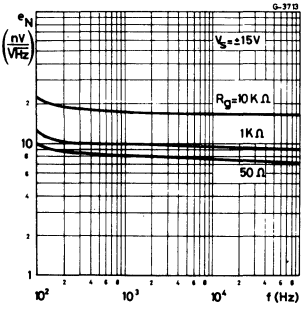


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

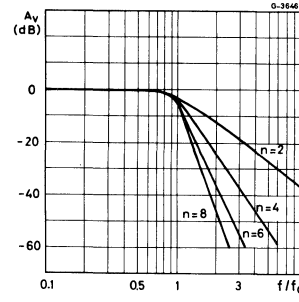
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband

Fig. 10 - Amplitude response



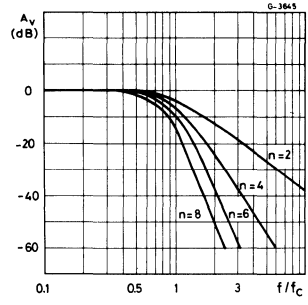
BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Fig. 11 - Amplitude response



Other characteristics:

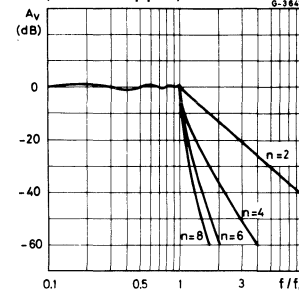
- Selectivity not as great as Chebyschev or Butterworth.
- Very little overshoot response to step inputs
- Fast rise time.

CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from ± 0.2 dB to ± 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

Fig. 12 - Amplitude response (± 1 dB ripple)



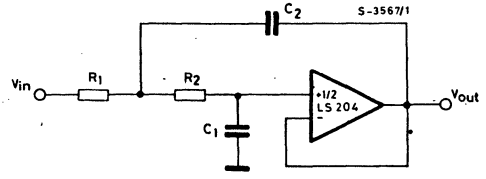
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1\ f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	-
	4	18	$3.0/f_c$	$5.4/f_c$	-
	6	21	$5.9/f_c$	$10.4/f_c$	-
	8	23	$8.4/f_c$	$16.4/f_c$	-
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	-
	4	28	$4.8/f_c$	$8.4/f_c$	-
	6	32	$8.2/f_c$	$16.3/f_c$	-
	8	34	$11.6/f_c$	$24.8/f_c$	-

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\,\xi\,\frac{S}{\omega_c} + \frac{S^2}{\omega_c{}^2}}$$

where:

$\omega_c = 2\pi\ f_c$ with f_c = cutoff frequency

ξ = damping factor.

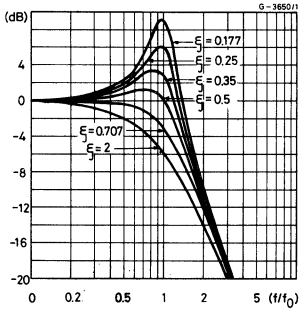
APPLICATION INFORMATION (continued)

Three parameters are needed to characterise the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).
The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required.
The choice of 'ξ' (or Q-factor) determines the filter response (see table).

Tab. I

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v= -3 dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

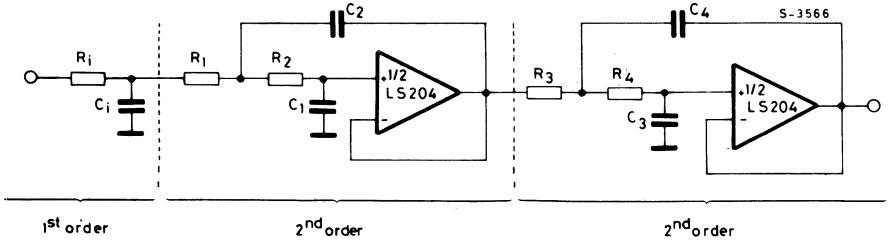
$$C_1 = \frac{1}{R}\,\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\,\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4$ = 10 KΩ, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33 \text{ nF}$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97 \text{ nF}$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20 \text{ nF}$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45 \text{ nF}$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14 \text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4$ = 1 nF we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5 \text{ KΩ}$$

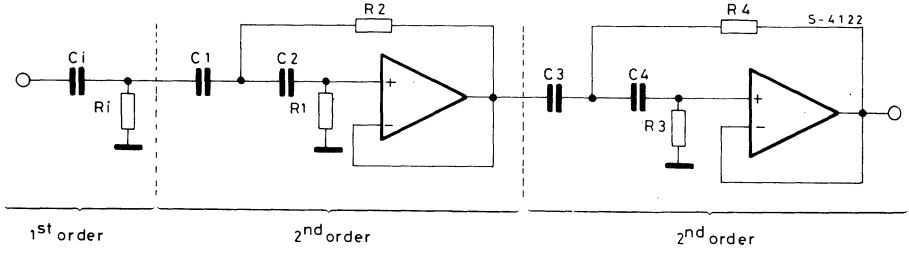
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6 \text{ KΩ}$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2 \text{ KΩ}$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103 \text{ KΩ}$$

$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6 \text{ KΩ}$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.



LINEAR INTEGRATED CIRCUITS

TELEPHONE SPEECH CIRCUITS

The LS285 and LS285A are monolithic integrated circuits for replacement of the hybrid circuit (2-4 wire interface) in conventional telephones interfacing the two transducers to the line and providing a controlled amount of sidetone.
The same type of transducer can be used for both transmitter and receiver, usually a 350Ω dynamic type.
By sensing the line current, LS285 and LS285A adjust the gain in both directions to compensate for line attenuation.
Output impedance can be matched to the line, independent of transducer impedance.
The LS285 and LS285A are packaged in a 14 lead dual in-line plastic package.

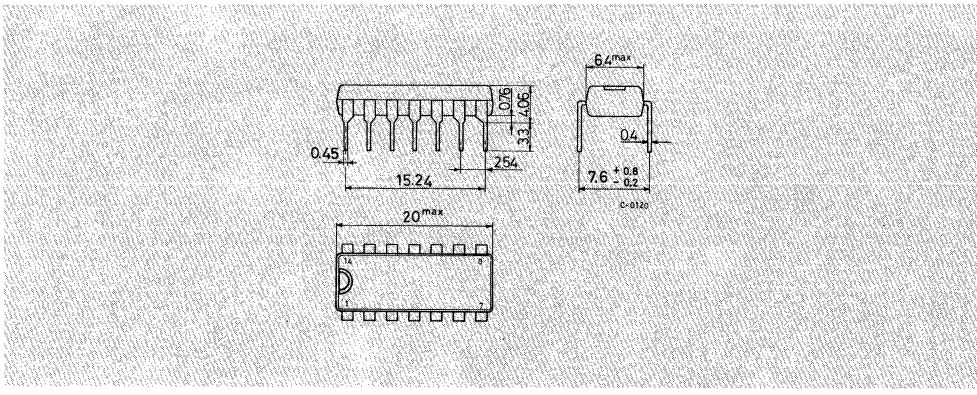
ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward current	120	mA
I_L	Reverse current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{stg}	Storage and junction temperature	-55 to 150	°C
T_{op}	Operating temperature	-40 to 70	°C

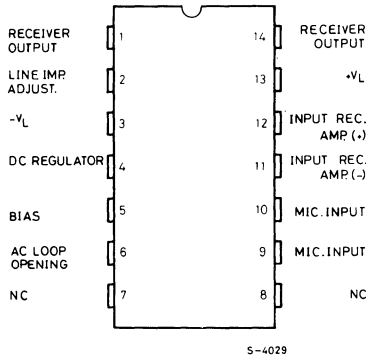
ORDERING NUMBERS: LS285 B
LS285 AB

MECHANICAL DATA

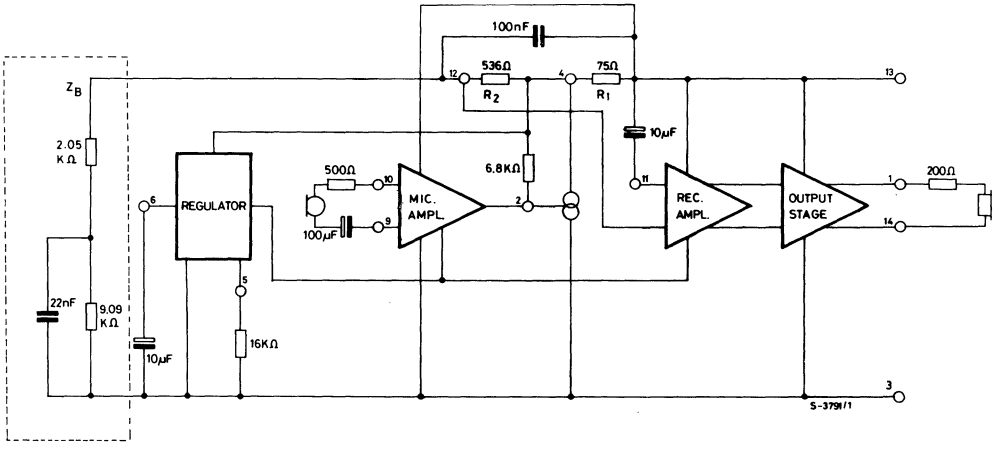
Dimensions in mm



CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



LS285
LS285A

DESCRIPTION

The LS285 and the LS285A are based on a bridge configuration. They contain a regulator block, a sending amplifier and a receiver amplifier.
The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length. It provides DC characteristics in line with CEPT standards.
The transmit/receiver amplifiers are connected to the line via an external bridge to provide sidetone attenuation.
The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line lenght. When he is hearing, the signal level on the receiver capsule is constant.
The amplifiers can also be matched to different transducers simply by varying external components. Gain variation over the operating temperature range is less than ± 1 dB.
The impedance to the line can be adjusted; without any change in circuit parameters; by changing an external resistor (6.8 KΩ at pin 2).

Basic circuit configuration

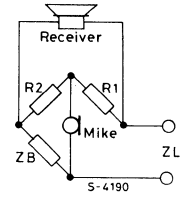


Fig. 1 - Test circuit

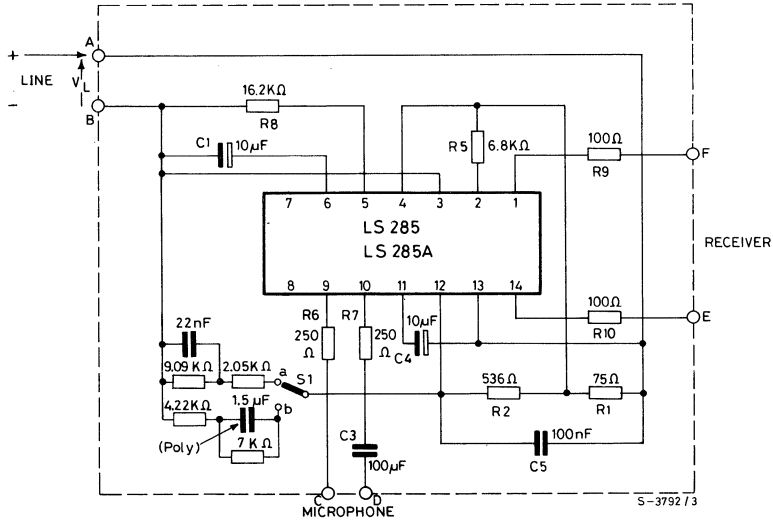
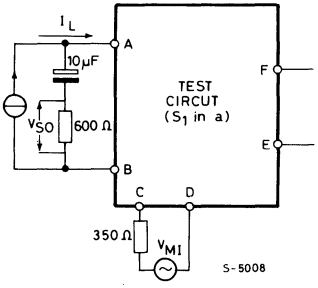
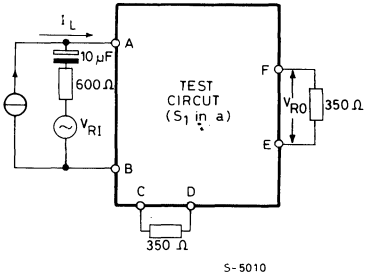


Fig. 2 - Sending gain



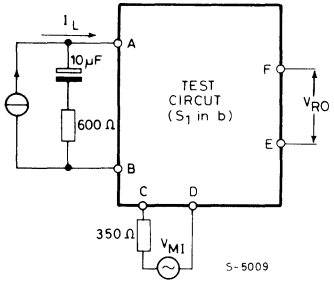
$$G_S = \frac{V_{SO}}{V_{MI}}$$

Fig. 3 - Receiving gain



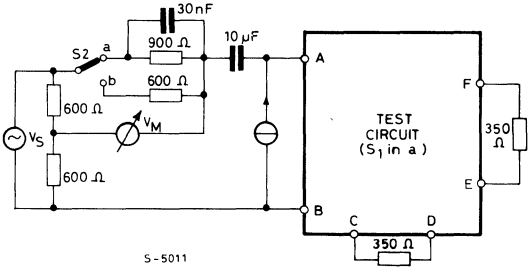
$$G_R = \frac{V_{RO}}{V_{RI}}$$

Fig. 4 - Sidetone



$$\text{Sidetone} = \frac{V_{RO}}{V_{MI}}$$

Fig. 5 - Return loss



$$R_L = \frac{V_s}{2\,V_M}$$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS(Refer to the test circuits, T_{amb}= -15 to +45°C, f = 300 Hz to 3400 Hz; unless otherwise specified)

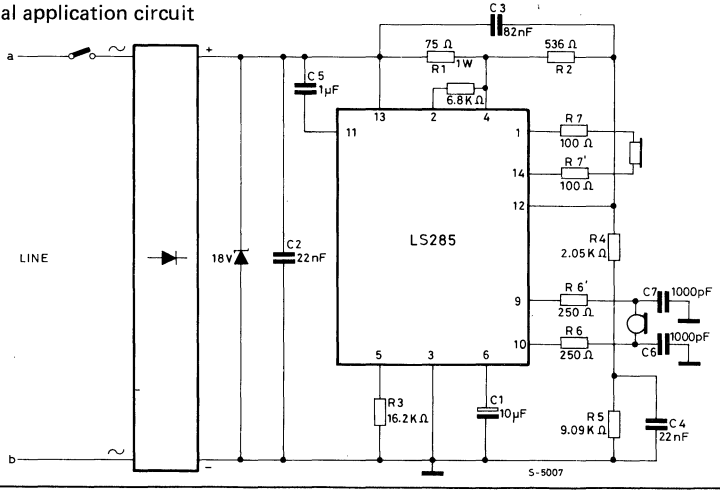
Parameter		Test conditions		Min.	Typ.	Max.	Unit	Fig.
V_L	Line voltage		I_L= 80 mA I_L= 20 mA I_L= 10 mA	10 5 3.8		11.5 5.8 4.6	V	1
G_S	Sending gain	f = 1 KHz T_{amb}=25°C (LS 285)	I_L= 10 mA I_L= 20 mA I_L= 40 mA I_L= 60 mA I_L= 80 mA	46.5 46.5 43.5 41 40		49.5 48.5 45.5 43 43	dB	2
		f = 1 KHz T_{amb}=25°C (LS 285A)	I_L= 10 mA I_L= 20 mA I_L= 60 mA I_L= 80 mA	46.5 40.7 40		50.5 49.5 44 44	dB	2
ΔG_S	Sending gain variation	Refer to the value at T_{amb}=25°C				± 1	dB	2
	Sending gain flatness	f_{ref}= 1 KHz	I_L= 10 to 80 mA			± 0.5	dB	2
	Sending distortion	I_L= 10 to 15 mA; V_{so}= 0.7 Vp				2	%	2
		I_L= 15 to 80 mA; V_{so}= 1 Vp				2	%	
	Sending noise	V_{MI}= 0V	I_L= 60 mA			-73	dBmp	2
	Microphone amplifier impedance (pin 9-10)			45		85	Ω	1
	Max sending output (°)	I_L= 10 to 80 mA V_{MI}= 1V				3	Vp	2
G_R	Receiving gain	f = 1 KHz T_{amb}=25°C (LS 285)	I_L= 10 mA I_L= 20 mA I_L= 40 mA I_L= 60 mA I_L= 80 mA	-13 -13 -16 -18 -19		-10 -11 -14 -16 -16	dB	3
		f = 1 KHz T_{amb}=25°C (LS 285A)	I_L= 10 mA I_L= 20 mA I_L= 60 mA I_L= 80 mA	-13.6 -13.6 -18 -19		-10 -10.6 -15 -16	dB	3
ΔG_R	Receiving gain variation	Refer to the value at T_{amb}= 25°C				± 1	dB	3
	Receiving gain flatness	f_{ref}= 1 KHz	I_L=10 to 80 mA			± 0.5	dB	3

(°) This output is limited to allow for input overvoltages.

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions		Min.	Typ.	Max.	Unit	Fig.
Receiving distortion	LS 285	I_L= 10 to 15 mA V_{RO}= 350 mVp			2	%	3
		I_L= 15 to 80 mA V_{RO}= 600 mVp			2		
	LS 285A	I_L= 15 to 80 mA V_{RO}= 500 mVp			2	%	3
Receiving noise	V_{RI}= 0V psophometric	I_L= 60 mA			100	µV	3
Receiving amplifier output impedance (pin 1-14)			60		100	Ω	1
Max receiving output current	I_L= 10 to 80 mA V_{RI}= 10V				2	mA	3
Sidetone	f = 1 KHz	I_L= 20 mA		7		dB	4
	T_{amb}= 25°C	I_L= 60 mA		0		dB	
Return loss	S_2 in a		12			dB	5
	S_2 in b		12			dB	

Fig. 6 - Typical application circuit



APPLICATION INFORMATION

The following table shows the recommended values for the typical application circuit of fig. 6. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R1	75 Ω	Bridge resistors	The ratio R2/R1 fixes the amount of the signal delivered to the line. (see fig. 7)
R2	536 Ω		
R3	16.2 KΩ	Bias resistor	Changing R3 value it is possible to shift the gain characteristics. The value can be chosen from 15 KΩ to 20 KΩ. The recommended value assures the maximum swing (see fig. 9).
R4	2.05 KΩ	Balance network	In order to optimize the sidetone it is possible to change R4 and R5 values. In any case: $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ where Z_B= R4 + R5//C4.
R5	9.09 KΩ		
R6 and R6'	250 Ω	Microphone impedance matching	R6 and R6' must be equal; 250Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to: $\Delta G_s = 20 \log \frac{Rx}{850\Omega}$ where Rx = R6 + R6' + R_{mike}. The trend of ΔG_s as a function of Rx value is shown in fig.8.
R7 and R7'	100 Ω	Receiver impedance matching	R7 and R7' must be equal; 100Ω is a typical value for dynamic capsules
C1	10 μF	AC loop opening	Ensures a high regulator impedance for AC signals (≅ 20 KΩ). This capacitor should not be higher than 10 μF in order to have a short response time of the system.
C2	22 nF	Matching to a capacitive line	C2 changes with the characteristics of the transmission line.
C3	82 nF	High frequency roll-off	C3 determines the high frequency response of the circuit. It also acts as RF bypass.
C4	22 nF	Balance network	See note for R4 and R5.
C5	1 μF	DC decoupling for receiving input	
C6 and C7	1000 pF	RF bypass	

APPLICATION INFORMATION (continued)

Fig. 7 - Receiving gain variation vs. R1 value (with fixed R1/R2 ratio)

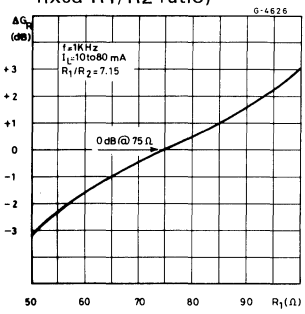


Fig. 8 - Sending gain variation vs. Rx value (see note for R6 and R6')

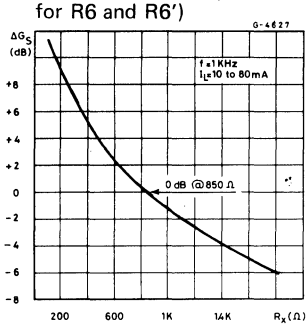
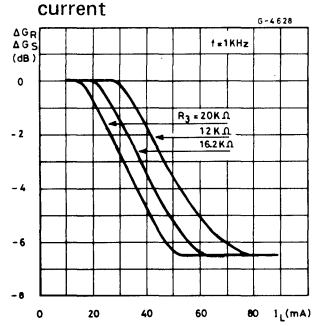


Fig. 9 - Sending and receiving gain variation vs. line current



LS288

LINEAR INTEGRATED CIRCUIT

PROGRAMMABLE TELEPHONE SPEECH CIRCUIT

The LS288 is a monolithic integrated circuit in 16 lead dual in-line plastic package. Designed as a replacement for the hybrid circuit in telephone sets it performs all the functions previously carried out by this circuit.
With the LS288 it is possible to select the operating mode (fixed or variable gain). The device works with both piezoceramic and dynamic transducers and therefore its gain, both in sending and receiving paths, can be preset by means of two external resistors. This feature can also be obtained in AGC operating mode, when the device automatically adjusts the Rx/Tx gains to compensate for the line attenuation by sensing the line current.
The LS288 can supply the decoupling FET when working with an electret microphone. Output impedance can be matched to the line independently of transducer impedance.

ADVANCE DATA

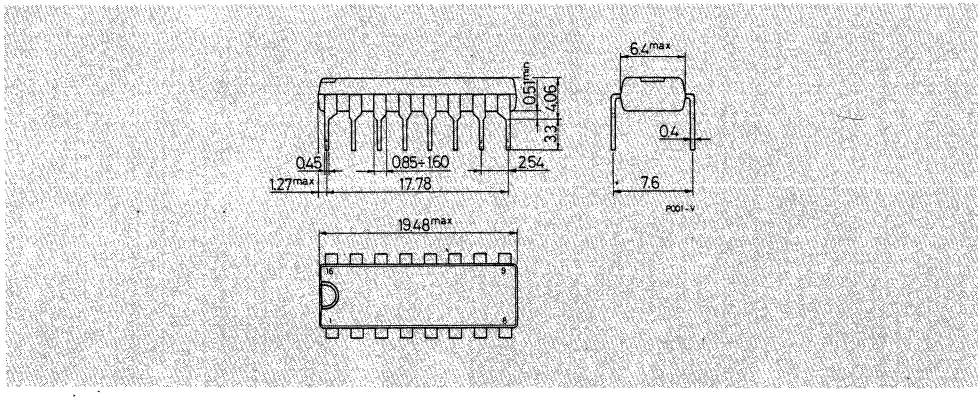
ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

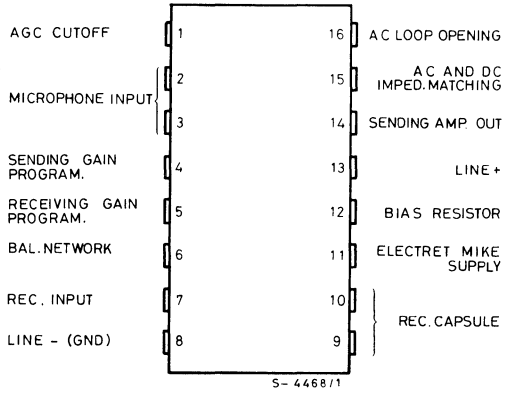
ORDERING NUMBER : LS288 B

MECHANICAL DATA

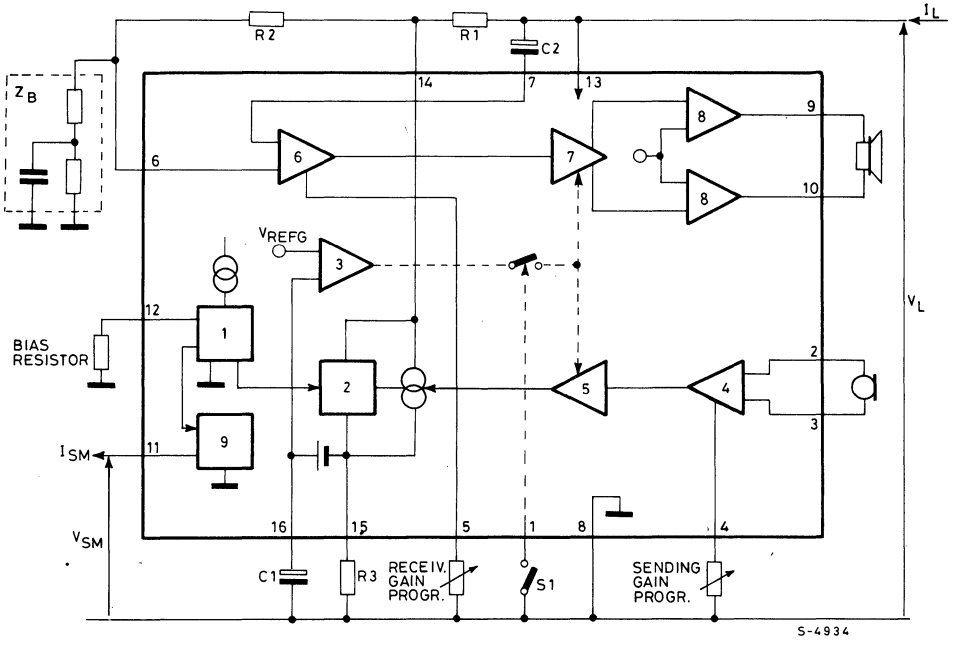
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST CIRCUITS

Fig. 1 - Test Circuit

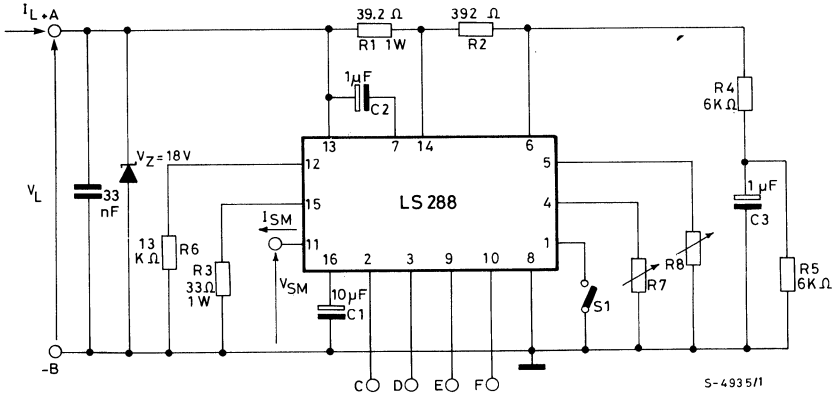
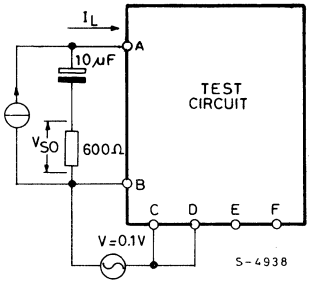
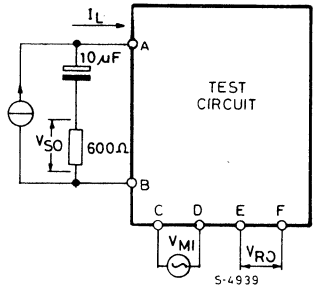


Fig. 2



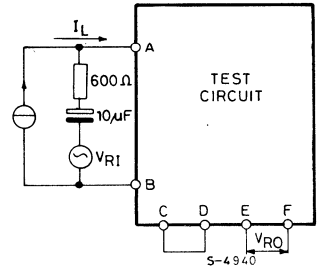
CMRR

Fig. 3



Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_s = \frac{V_{SO}}{V_{MI}}$

Fig. 4



$G_R = \frac{V_{RO}}{V_{RI}}$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max 80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, T_{amb}= -25 to +50°C, f = 200 to 3400 Hz, I_L = 12 to 120 mA, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit	Fig.
AGC off (pin 1 floating)								
V_L	Line voltage	T_{amb}= 25°C	I_L= 15 mA I_L= 22 mA I_L= 60 mA I_L= 120 mA	4.1	4.5	4.9 5.4 10 14	V	1
CMRR	Common mode rejection	f = 1 KHz			50		dB	2
G_S	Sending gain (*)	I_L= 15 mA T_{amb}= 25°C f = 1 KHz R_8 = 17 KΩ V_{MI}= 3 mV	R_7 = 8 KΩ R_7 = 29 KΩ R_7 = 47 KΩ	40	26 41 51	42	dB	3
ΔG_S	Sending gain flatness (vs. freq.)	V_{MI}= 3 mV f_{ref}= 1 KHz	I_{Lref}= 60 mA			± 0.5	dB	3
ΔG_S	Sending gain flatness (vs. current)					± 0.5	dB	
d_S	Sending distortion	f = 1 KHz G_S= 42 dB	V_{SO}= 450 mV V_{SO}= 775 mV			2 5	%	3
	Sending noise	G_S= 42 dB	V_{MI}= 0			-72	dBmp	3
R_{2-3}	Microphone input impedance pin 2-3	V_{MI}= 3 mV		11	15		KΩ	3
G_R	Receiving gain (*)	I_L= 15 mA T_{amb}= 25°C f = 1 KHz R_7 = 29 KΩ V_{RI}= 0.3V	R_8 = 8 KΩ R_8 = 17 KΩ R_8 = 23 KΩ	4	-6 5 14	6	dB	4
ΔG_R	Receiving gain flatness (vs. freq.)	V_{RI}= 0.3V f_{ref}= 1 KHz	I_{Lref}= 60 mA			± 0.5	dB	4
ΔG_R	Receiving gain flatness (vs. current)					± 0.5	dB	
d_R	Receiving distortion	f = 1 KHz G_R= -3 dB	V_{RI}= 570 mV V_{RI}= 1.2V			2 5	%	4
	Receiving noise	G_R= 0 dB V_{RI}= 0			250		μV	4
R_{9-10}	Receiver output impedance (pin 9 and 10)	V_{RO}= 50 mV			20		Ω	4
	Sidetone	f = 1 KHz G_S= 42 dB G_R= -3 dB			15		dB	3
Z_{ML}	Line matching impedance	V_{RI}= 0.3V	f = 1 KHz	650	750	850	Ω	4
	Max receiving output (click suppressor)	V_{RI}= 2V G_R = 0 dB			2.3		Vp	4
V_{SM}	Microphone supply voltage (pin 11)	I_{SM}= 0.8 mA		1.9		2.1	V	1

(*) The sending and receiving gains are not completely independent but the variation in sending gain over the whole range of receiving gain (and vice-versa) is less than 0.5 dB.

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test condition		Min.	Typ.	Max.	Unit	Fig.
AGC on (pin 1 grounded)							
ΔG_S and ΔG_R Sending and receiving gain variation (**)	T_{amb}= 25°C	I_L = 25 mA	-1		+1	dB	3-4
		I_L = 50 mA	-6		-4		
	f = 1 KHz	I_L = 110 mA	-7		-5		

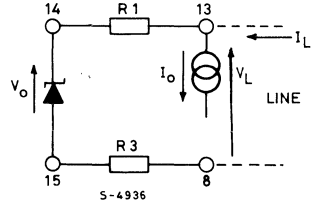
(**) Referred to any value fixed by means of R_7 and R_8.

CIRCUIT DESCRIPTION

1. DC Characteristic

In accordance with CCITT recommendations, any device connected to a telephone line must exhibit a proper DC characteristic V_L, I_L.
The DC characteristics of the LS288 is determined by the shunt regulator (block 2) together with two series resistors R_1 and R_3 (see the block diagram). The equivalent circuit is shown in fig. 5.

Fig. 5 - Equivalent DC load to the line

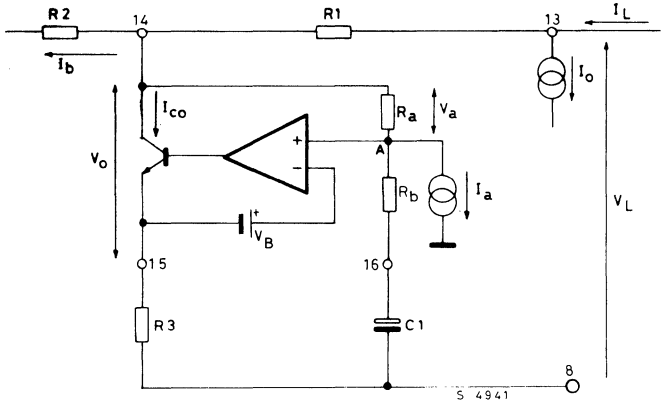


A fixed amount, I_o, of the total available current, I_L, is drained to allow the circuit to operate correctly. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 12.

CIRCUIT DESCRIPTION (continued)

The recommended minimum value of I_o is 7.5 mA with R pin 12 = 13 KΩ.
The voltage $V_o \cong 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (block 2) is controlled by a temperature compensated voltage reference (block 1).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Fig. 6 - Circuit configuration of the shunt regulator



The difference $I_L - I_o$ flows through the shunt regulator since I_b is negligible.
I_a is an internal constant current generator; hence $V_o = V_B + I_a \cdot R_a = 3.8V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series with a battery.
It is important to note that the DC voltage at pin 16 is proportional to the line current $V_{16} = V_{15} + V_B = (I_L - I_o)\, R_3 + V_B$.

2. Two to four wires conversion

The LS288 performs the two wire (line) to four wire (microphone, earphone) conversion by means of a Wheatstone bridge configuration thus obtaining the proper decoupling between sending and receiving signals (see fig. 7).

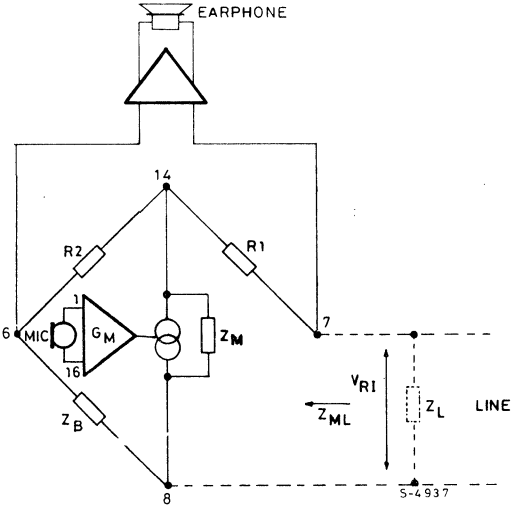
For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$

The AC signal from the microphone is sent to one diagonal of the bridge (pin 8 and 14). A small percentage of the signal power is lost on Z_B (since $Z_B \gg Z_L$); the main part is sent to the line via R_1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 6 and 7). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator which also acts as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{(14-8)}}{\Delta I_{(14-8)}}$.

CIRCUIT DESCRIPTION (continued)

Fig. 7 - Two to four wires conversion



From fig. 6, considering C_1 as a short circuit to the AC signal, any variation in ΔV_{14} generates a variation as follows:

$$\Delta V_{15} = \Delta V_A = \Delta V_{14} \frac{R_b}{R_a + R_b}$$

The corresponding current change is:

$$\Delta I = \frac{\Delta V_{15}}{R_3}$$

therefore

$$Z_M = \frac{\Delta V_{14}}{\Delta I} = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The total impedance across the line connections (pin 13 and 8) is given by

$$Z_{ML} = R_1 + Z_M // (R_2 + Z_B)$$

By choosing $Z_M \gg R_1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R_3 \left(1 + \frac{R_a}{R_b}\right)$$

The amplitude of the signal received across pins 6 and 7 can be changed using different values of R_1. (Of course the relationship $\frac{Z_L}{Z_B} = \frac{R_1}{R_2}$ must always be valid).

The received signal is related to the value of R_1 according to the approximated relationship:

$$V_R = V_{RI}\ 2\ \frac{R_1}{R_1 + Z_M}$$

Note that if the value of R_1 is changed the transmission signal current is not changed, since the microphone amplifier is a transconductance amplifier.

3. Input and output amplifiers

The microphone amplifier (4) has a differential input stage with high impedance (min 11 KΩ) so allowing a good matching to the microphone by means of an external resistor without affecting the sending gain.
The receiving output stage (8) is intended to drive both piezoceramic and dynamic capsules. It has low output impedance, a maximum voltage swing greater than 2 V_p and a peak current of 2 mA.
With very low impedance transducers, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

4. Gain Control

It is possible to set the LS288 gain characteristics by means of one pin (pin 1).
When the pin 1 is floating, the gains of the sending and receiving amplifiers do not depend on the line current (AGC off). When the pin 1 is grounded the LS288 automatically changes the gain to compensate for line attenuation (AGC on).

4.1. AGC OFF

In this conditions, as already mentioned, both the sending and the receiving gain are fixed. Their values are determined, independently for the two paths, by the two external resistors R_7 (for T_x, between pin 4 and ground) and R_8 (for R_x, between pin 5 and ground). R_7 values ranging from 8 KΩ up to 50 KΩ giving sending gains from 26 dB to 51 dB. R_8 values range from 8 KΩ to 23 KΩ giving receiving gains from -6 dB to +14 dB (see fig. 9 and 10).
This allows the LS288 to be used with a variety of different transducers.

Fig. 9 - Sending gain vs. R_7 value (AGC off)

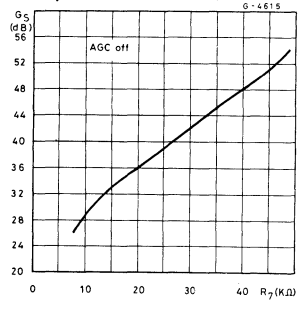
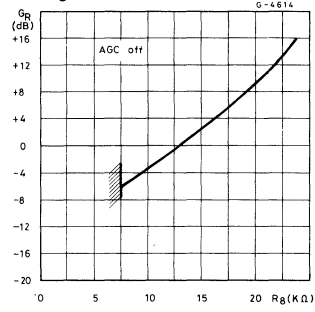


Fig. 10 - Receiving gain vs. R_8 value (AGC off)



DESCRIPTION CIRCUIT (continued)

4.2. AGC ON

Starting from any couple of gain values, fixed by the appropriate values of R_7 and R_8, the LS288 can automatically change the sending and receiving gains depending on the line current.
The line current is sensed across R_3 (see fig. 7) and transferred to pin 16 by the regulator.

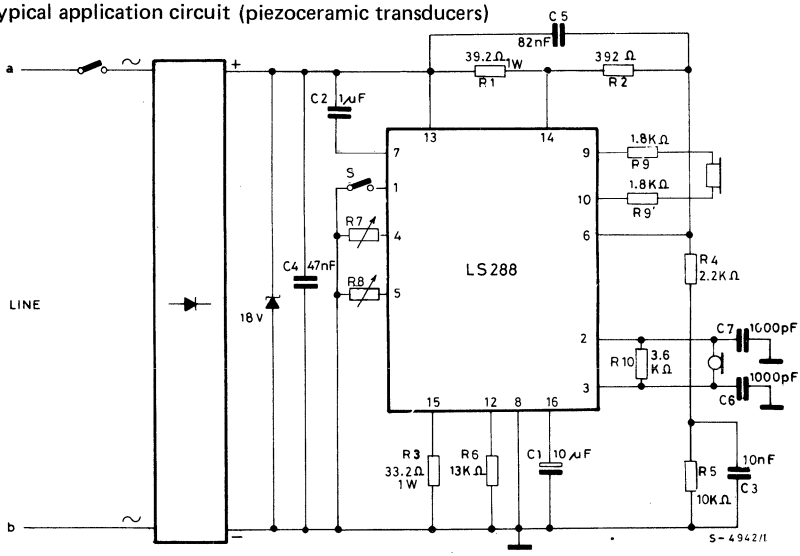
$$V_{16} = V_B + V_{15} = V_B + (I_L - I_o) \cdot R_3$$

Following comparison with an internal reference V_{REFG} (see the block diagram) the voltage at pin 16 is used to modify the gain of the amplifiers (5) and (7) on both the sending and receiving paths.
The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.
The external resistors R_7 and R_8 fix the maximum value for the gains.
Minimum gain is reached for a line current of about 110 mA when the same drain current I_o of 7.5 mA is used.
When I_o is increased by means of the external resistor connected to pin 12 the two above mentioned line current values for the starting point and for the minimum gain increase accordingly.

5. DC Shunt Regulator

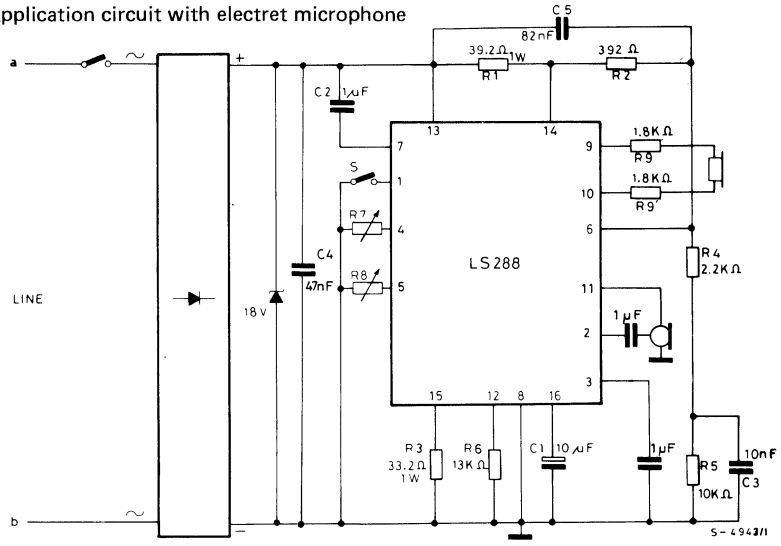
The LS288 has built into the chip a DC shunt regulator intended to supply the coupling FET when an electret microphone is used. It delivers 1 mAp current with a voltage of 2 Volts (typ) regardless of the line current.

Fig. 11 - Typical application circuit (piezoceramic transducers)



CIRCUIT DESCRIPTION (continued)

Fig. 12 - Application circuit with electret microphone



The following table can be helpful to the designer when choosing different values for the external components; it refers to the typical application circuit of fig. 11.

Component	Value	Function	Note
R_1	39.2 Ω	Bridge	R_1 controls the receiving gain. The ratio R_2/R_1 fixes the amount of signal delivered to the line. R_1 helps in fixing the DC characteristic (see R_3 note)
R_2	392 Ω	Resistors	
R_3	33.2 Ω	Line current sensing Fixing DC characteristic	The relationships involving R_3 are: $-Z_{ML} = (25\,R_3 // Z_B) + R_1$ $-G_s = K \cdot \frac{Z_L // Z_{ML}}{R_3}$ $-V_L = (I_L - I_o)(R_3 + R_1) + V_o$ [$V_o = 3.8V$] Values of Z_{ML} ranging from 650 up to 850Ω are easily obtainable.
R_4	2.2 KΩ	Balance Network	In order to optimize the sidetone it is possible to change R_4 and R_5 values; in any case the following relationship applies: $\frac{Z_B}{Z_L} = \frac{R_2}{R_1}$ where $Z_B = R_4 + R_5 // X_{C3}$
R_5	10 KΩ		

APPLICATION INFORMATION (continued)

Component	Value	Function	Note
R_6	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R_6 (they are inversely proportional), in order to achieve the shifting of the AGC starting point
R_7	8 to 50 KΩ	Sending gain programming Resistor	
R_8	8 to 23 KΩ	Receiving gain programming Resistor	
R_9, R_9'	1.8 KΩ	Receiver impedance matching	R_9 and R_9' must be equal; the suggested value is good for matching to piezoceramic capsule; there is no problem in increasing and decreasing (down to 0Ω) this value, but when low resistance levels are used DC decoupling must be inserted to stop the current due to the receiver output offset voltage (max 400 mV).
R_{10}	4 KΩ	Microphone impedance matching	The suggested value is typical for a piezoceramic microphone, but it is possible to choose R_{10} from a wide range of values: $R_{Mike} = R_{10} // R_{pin\ 2-3}$.
C_1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low line current. A lower value gives an alteration of the AC line impedance at low frequency.
C_2	1 μF	DC decoupling for receiving input	
C_3	10 nF	Balance network	See note for R_4 and R_5.
C_4	47 nF	Matching to a capacitive line	C_4 must be chosen according to the characteristics of the transmission line.
C_5	82 nF	Receiving gain flattness	C_5 depends on balancing and line impedance versus frequency.
C_6, C_7	1000 pF	RF bypass	

LINEAR INTEGRATED CIRCUIT

LS342

MULTIFREQUENCY TO TELEPHONE LINE INTERFACE CIRCUIT

The LS342 is a monolithic integrated circuit in dual in-line minidip plastic package. It interfaces the multifrequency tone diallers M751 and M761/761A to the line in telephone sets, performing the following functions:

- Adjustment of the DC current/voltage characteristic and AC input line impedance by means of an external resistor (R_E).
- Sending to the line of the multifrequency signal.
- Adjustment of the signal level by means of an external resistor (R_T).
- Stabilized supply voltage to the tone dialler.

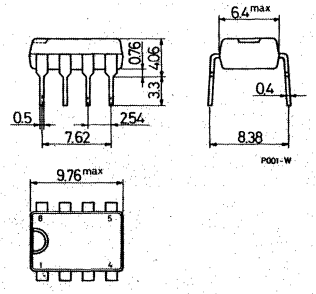
ABSOLUTE MAXIMUM RATINGS

V_L	Maximum line voltage (pulse duration $\leqslant$ 10 ms)	22	V
I_L	Maximum forward current	155	mA
I_L	Maximum reverse current	-150	mA
P_{tot}	Total power dissipation at T_{amb} = 70°C	800	mW
T_{op}	Operating temperature	-40 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

ORDERING NUMBER: LS342D

MECHANICAL DATA

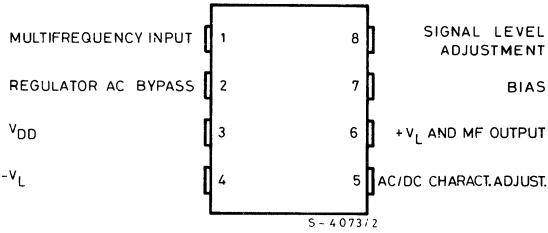
Dimensions in mm



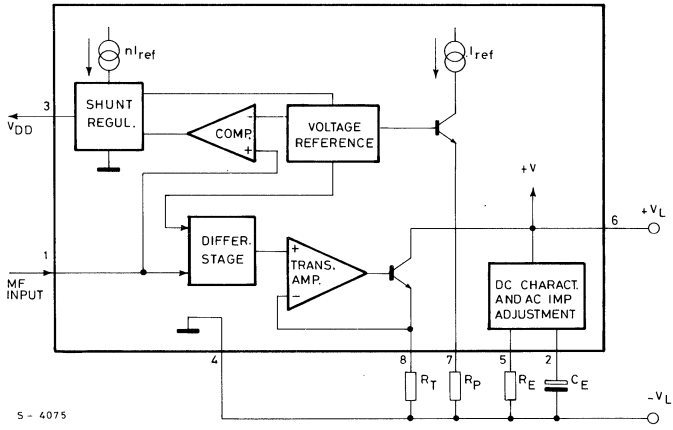
LS342

CONNECTION DIAGRAM

(top view)



BLOCK DIAGRAM



DESCRIPTION

The LS342 interface the M751 and M761/761A tone diallers with the telephone line. Power is only applied to the system when the handset is lifted and a key pressed. At this time S1 is also switched (see fig. 2) disconnecting the speech circuit from the line and connecting the dialling circuit.
In the dialling condition the LS342 performs 3 functions:

1) D.C. and A.C. line termination
2) Tone dialler power supply
3) Amplification and transmission of tone pairs.

In the initial stage of switch-on the supply voltage V_{DD} is regulated at $\cong$ 4 volt. This overdrives the M751/761/761A internal oscillator causing a rapid start-up and therefore rapid generation of output tones.
When the system reaches its normal operating point the supply voltage V_{DD} is stabilized at 2.5V $\pm$ 4%.

THERMAL DATA

$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS (I_L = 10 to 100 mA; T_{amb} = -25 to +60°C; f = 1 KHz; S in (b), unless otherwise specified).

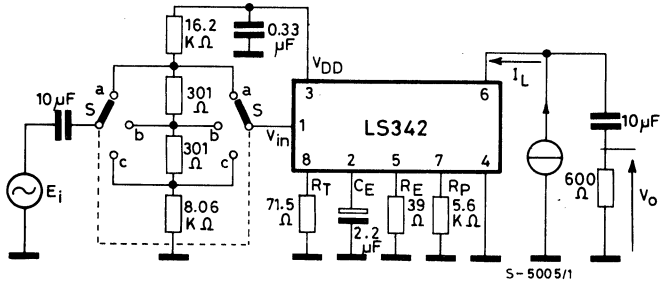
Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_L	Line voltage	E_i = 0	I_L = 10 mA I_L = 17 mA I_L = 60 mA I_L = 150 mA		4.2 4.6 6.3 9.8	4.5 5 6.8 11.5	V
G_s	Sending gain	T_{amb} = 25°C E_i = 50 mV f = 500 Hz to 2 KHz		12.4		14	dB
ΔG_s	Sending gain spread over temperature					± 0.2	dB
THD*	Distortion	S in (a) E_i = 120 mV **				2	%
		S in (c) E_i = 95 mV **				2	
A_R	Return loss	Z_{REF} = 600Ω f = 300 Hz to 3.4 KHz		14			dB
Z_{OUT}	Output impedance (pins 6, 4)	C_E = 2.2 μF R_E = 39Ω			750		Ω
V_{DD}	Supply voltage for digital device	T_{amb} = 25°C		2.4	2.5	2.6	V
I_{DD}	Supply current for digital device	V_{DD} = 2.4V		1.8			mA
t_s***	Start-up time					5	msec
Z_{IN}	Input impedance (pin 1)			4			MΩ

* The distortion of the device is not affected by a signal coming from the line with the following levels: -13 dBm if I_L = 10 mA, -8 dBm if I_L = 20 mA.

** The different AC and DC levels are intended to simulate the limit working operation of the digital devices M751, M761, M761A.

*** The time necessary because the AC signal is varying within ± 1 dB of its steady-state value.

Fig. 1 - Test circuit

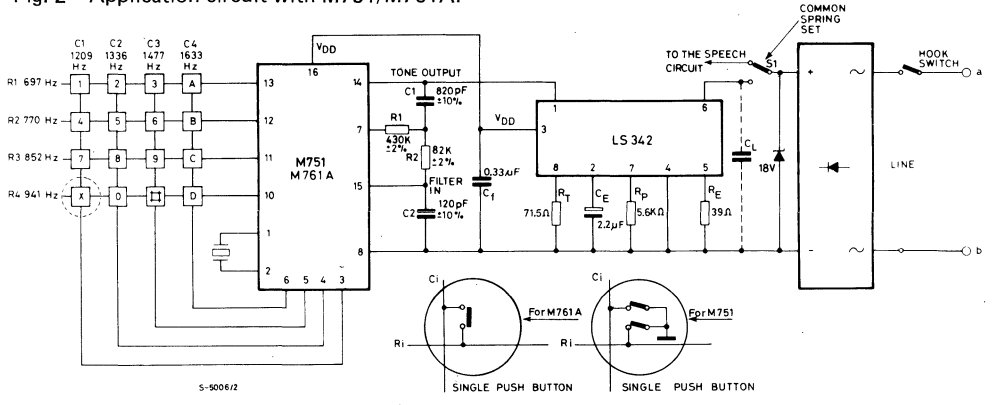


APPLICATION INFORMATION

The table shows the recommended values for the circuit of fig. 2.

Component	Recomm. value	Purpose	Note
R_E	39 Ω	DC characteristic AC impedance adjustment	The relationships involving R_E are: • $V_L = (I_L - I_o) R_E + V_o$ where $I_o \cong 6$ mA and $V_o \cong 4V$ • $Z_o = 22 R_E$ (f = 1 KHz) The following relationship must be always verified $R_E \geqslant \frac{Vp \cdot Z_L}{(I_L - I_o) Z_L - 22 Vp}$ where Vp is the maximum peak value of the MF signal in the line and Z_L is the line impedance.
R_p	5.6 KΩ	Bias resistor	R_p can be reduced in order to increase the output current from pin 3 (V_{DD}). In this case, the total current consumption is increased.
R_T	71.5Ω	Signal level adjustment	The MF gain is: $G_{MF} = 0.97 \frac{Z_L // Z_o}{R_T}$ The recommended value for R_T is good to set the Europe I standard (-9 dBm, -11 dBm). If the Europe II or the American Standard is required, R_T must be decreased. In the mean time, the minimum operation current will increase because the pin 8 voltage is fixed by an internal reference (190 mV typ.).
C_E	2.2 μF	Regulator AC bypass	A value greater than 2.2 μF gives a system start time too high when line current is between 10 mA and 17 mA. A value less than 2.2 μF gives an alteration of the AC line impedance because its reactance is not negligible at low frequencies.
C_f	0.33 μF	DC filtering	The C_f range is from 0.33 μF to 0.47 μF. The lowest values is ripple limited, the higher values is starting up time limited.
C_L	30 nF	Matching to a capacitive line	This is needed with a capacitive line because the output impedance of the LS342 is essentially resistive. The range of C_L is between 30 and 60nF.

Fig. 2 - Application circuit with M751/M761A.



LINEAR INTEGRATED CIRCUIT

LS356

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

The LS356 is a monolithic integrated circuit in 16-lead dual in-line plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically dynamic capsules, but the device can also work with **piezoceramic ones**). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS356 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).
The LS356 basic functions are the following:

- It presents the proper DC path for the line current.
- It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing either the line current or the line voltage. **In addition, the LS356 can also work in fixed gain mode.**
- It acts as linear interface for MF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated by the M761.

PRELIMINARY DATA

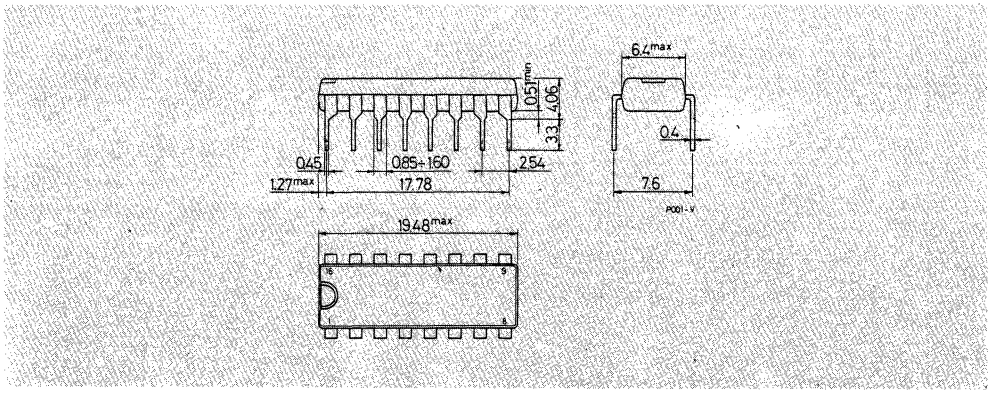
ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

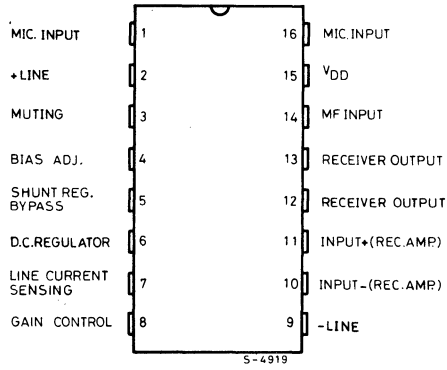
ORDERING NUMBER: LS356B

MECHANICAL DATA

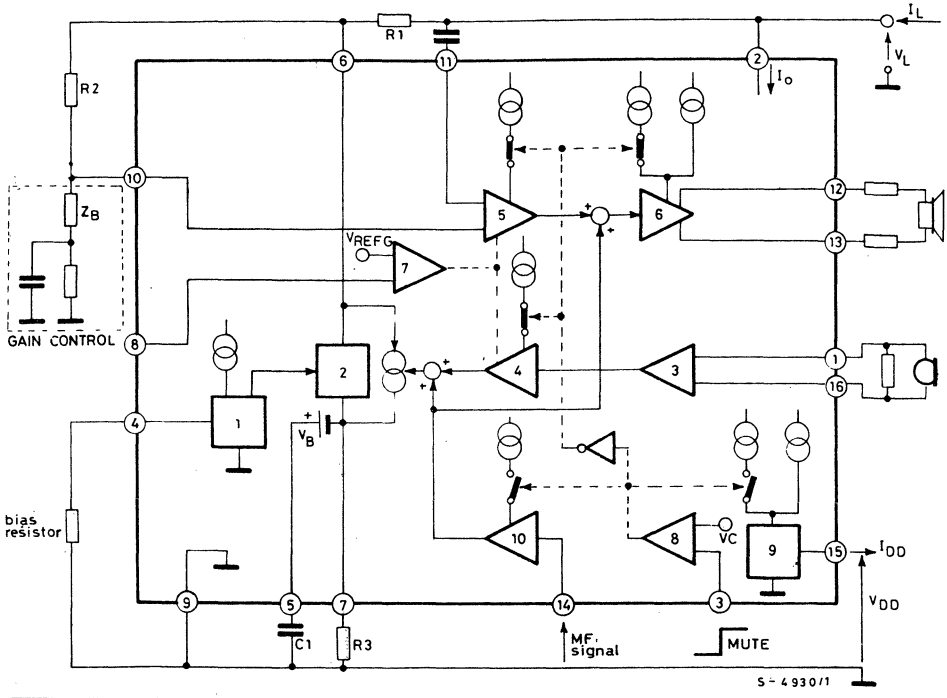
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST CIRCUITS

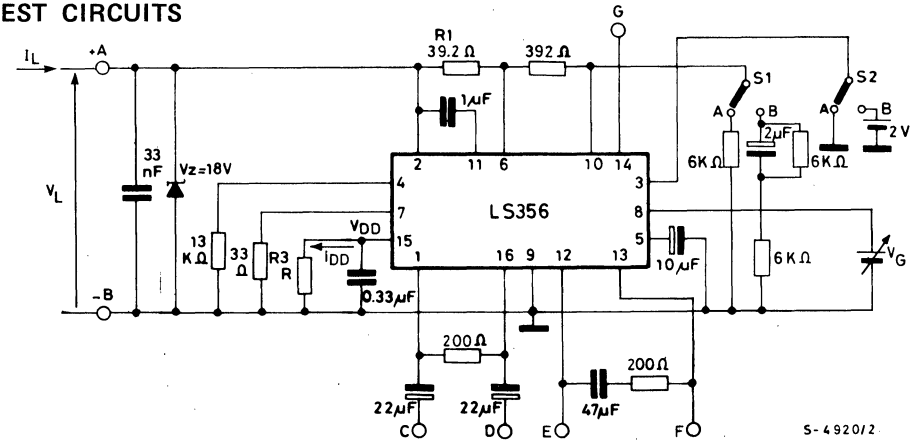
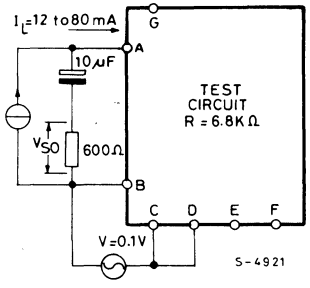
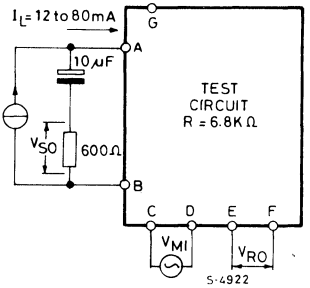


Fig. 1



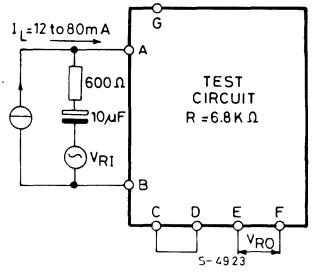
CMRR

Fig. 2



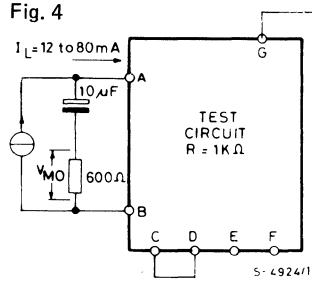
Side tone = $\frac{V_{RO}}{V_{MI}}$; $G_s = \frac{V_{SO}}{V_{MI}}$

Fig. 3



$G_R = \frac{V_{RO}}{V_{RI}}$

Fig. 4



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_G = 1 to 2V, I_L = 12 to 80 mA, S1 and S2 in (a), T_{amb} = -25 to +50°C, f = 200 to 3400 Hz, unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line voltage	T_{amb}= 25°C I_L= 12 mA I_L= 20 mA I_L= 80 mA	3.9		4.7 5.5 12.2	V	–
CMRR	Common mode rejection	f = 1 KHz	50			dB	1
G_S	Sending gain	T_{amb}= 25°C f= 1KHz V_G= 2V V_{MI}= 3 mV V_G= 1V	44 48		46 50	dB	2
	Sending gain flatness (vs. frequency)	V_{MI}= 3 mV f_{ref}= 1 KHz			± 1	dB	2
*	Sending gain flatness (vs. current)				± 0.5	dB	2
	Sending distortion	f = 1 KHz V_{so}= 1V V_{so}= 1.3V			2 10	%	2
	Sending noise	V_{MI}= 0V V_G= 1V		-70		dBmp	2
	Microphone input impedance (pin 1-16)	V_{MI}= 3 mV	40			KΩ	–
	Sending gain in MF operation	V_{MI}= 3 mV S2 in (b)	-30			dB	2
G_R	Receiving gain	V_{RI}= 0.3V V_G= 2V f = 1 KHz V_G= 1V T_{amb}= 25°C	-3 -1	-4 0	-5 1	dB	3
	Receiving gain flatness (vs. frequency)	V_{RI}= 0.3V f_{ref}= 1 KHz			± 1	dB	3
*	Receiving gain flatness (vs. current)				± 0.5	dB	3
	Receiving distortion	f = 1 KHz V_{RO}= 400 mV V_{RO}= 480 mV		10	2	%	3
	Receiving noise	V_{RI}= 0V		100		μV	3
	Receiver output impedance (pin 12-13)	V_{RO}= 50 mV			100	Ω	–
	Sidetone	f = 1 KHz T_{amb}= 25°C S1 in (b)			36	dB	2
Z_{ML}	Line matching impedance	V_{RI}= 0.3V f = 1 KHz	500	600	700	Ω	3
I_8	Input current for gain control (pin 8)				-10	μA	–

* Fixed gain mode.

ELECTRICAL CHARACTERISTICS (continued)

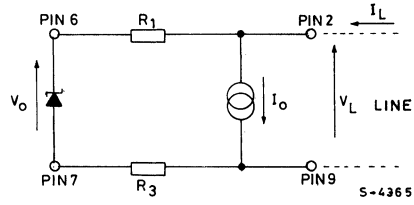
Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF supply voltage (Standby and operation)	S2 in (b)	2.4	2.5		V	–
I_{DD}	MF supply current Standby Operation	S2 in (b)	0.5 2			mA	–
	MF amplifier gain	$f_{MF\ in}$= 1 KHz $V_{MF\ in}$= 80 mV	15		17	dB	4
V_I	DC input voltage level (pin 14)	$V_{MF\ in}$= 80 mV		0.3 V_{DD}		V	–
R_I	Input impedance (pin 14)	$V_{MF\ in}$= 80 mV	60			KΩ	–
d	Distortion	$V_{MF\ in}$= 110 mV			2	%	4
	Starting delay time				5	ms	–
	Muting threshold voltage (pin 3)	Speech operation			1	V	–
		MF operation	1.6			V	–
	Muting standby current (pin 3)				-10	μA	–
	Muting operating current (pin 3)	S2 in (b)			+10	μA	–

CIRCUIT DESCRIPTION

1. DC characteristic

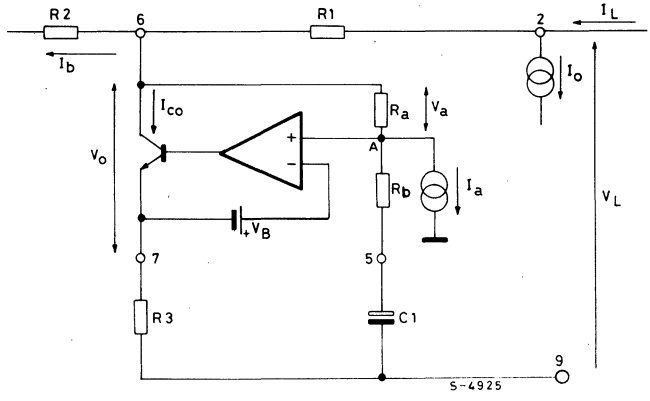
The fig. 5 shows the DC equivalent circuit of the LS356.

Fig. 5 - Equivalent DC load to the line



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).
The minimum value of I_o is 7.5 mA.
The voltage $V_o = 3.8V$ of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

Fig. 6 - Circuit configuration of the shunt regulator



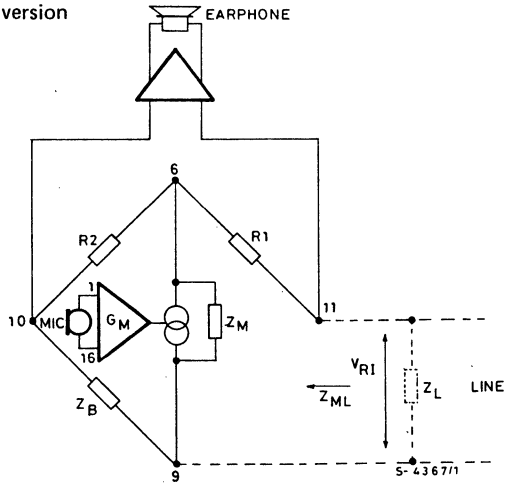
The difference $I_L - I_o$ flows through the shunt regulator being I_b negligible.
I_a is an internal constant current generator; hence $V_o = V_B + I_a \cdot R_a = 3.8V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery. It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).

CIRCUIT DESCRIPTION (continued)

2. Two to four wires conversion

The LS356 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 7).

Fig. 7 - Two to four wires conversion



For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R1}{R2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B \gg Z_L$); the main part is sent to the line via R1.
In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$.

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation:

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3 \left(1 + \frac{R_a}{R_b}\right)$$

CIRCUIT DESCRIPTION (continued)

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R1 + Z_M \,//\, (R2 + Z_B)$$

By choosing $Z_M \gg R1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R3\,(1 + \frac{R_a}{R_b})$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).
The received signal is related to R1 value according to the approximated relationship:

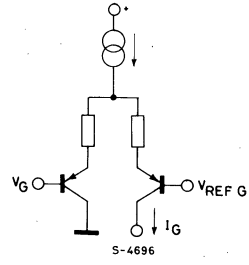
$$V_R = 2\,V_{RI}\,\frac{R1}{R1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3.Automatic gain control

The LS356 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.
This function is performed by the circuit of fig. 8.

Fig. 8



The differential stage is progressively unbalanced by changing V_G in the range 1 to 2V (V_{REFG} is an internal reference voltage, temperature compensated).
It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken:

a) from the LS356 itself (both in variable and in fixed mode) and

b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain characteristic depending on the current.
In fact (see fig. 6):

$$V_5 = V_B + V_7 \cong V_B + (I_L - I_o)\,R3$$

The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.

CIRCUIT DESCRIPTION (continued)

Minimum gain is reached for a line current of about 52 mA for the same drain current $I_o = 7.5$ mA. When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.
It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too; for example using a division 1:1 (50K/50K) the AGC starting point shifts to about $I_L = 40$ mA, and the minimum gain is obtained at $I_L = 95$ mA.
In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain values (Rx, Tx) independently of the line conditions.
For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.
This type of operation meets for istance the requirements of the French standard. (See the application circuit of fig. 12).

4. Transducers interfacing

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain.
The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance, 100 Ω max; high current capability, 3 mAp).
When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).
With very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency interfacing

The LS356 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.
When no key of the keyboard is pressed the mute state is low and the LS356 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.
When one key is pressed, the M761 sends a "high state" mute condition to the LS 356. A voltage comparator (8) of LS356 drives internal electronic switches: the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.
This extra current is diverted by the receiving and sending section of the LS356 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.
A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber; the MF amplifier (10) delivers the dial tones to the sending paths.
The application circuit shown in fig. 9 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm) an external divider must be used (fig. 10).
The mute function can be used also when a temporary inhibition of the output signal is requested.

APPLICATION INFORMATION

Fig. 9 - Application circuit with multifrequency (EUROPE II STD)

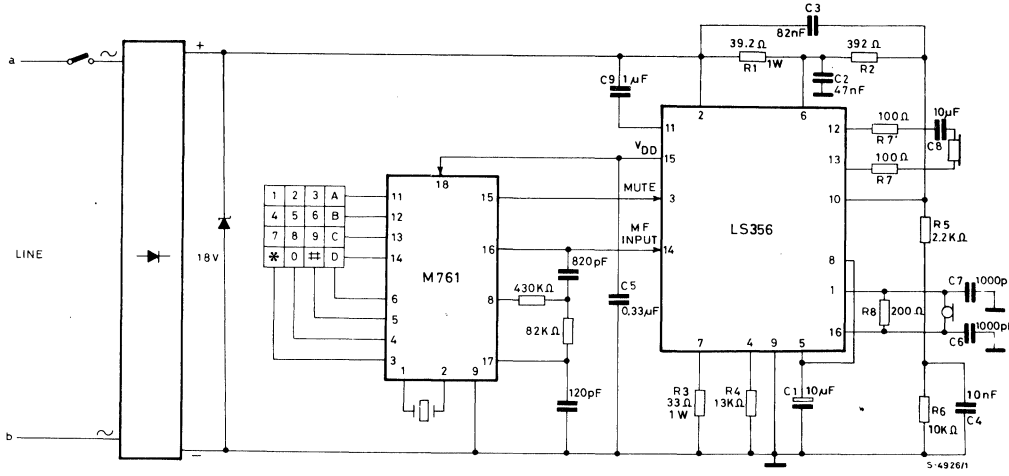
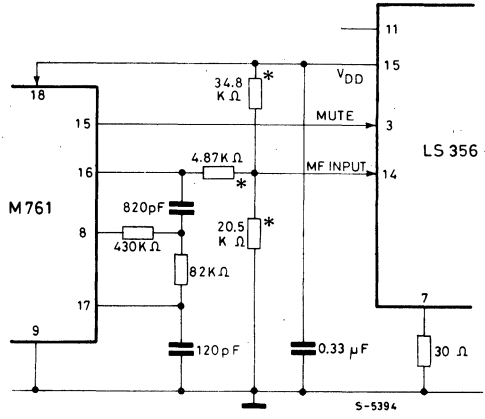


Fig. 10 - Application circuit with multifrequency (EUROPE I)



* TOLLERANCE =±2%

APPLICATION INFORMATION (continued)

Fig. 11 - Sending and receiving gain vs. line current (application circuit of fig. 13)

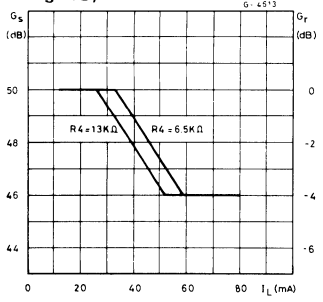


Fig. 12 - Application circuit without multifrequency

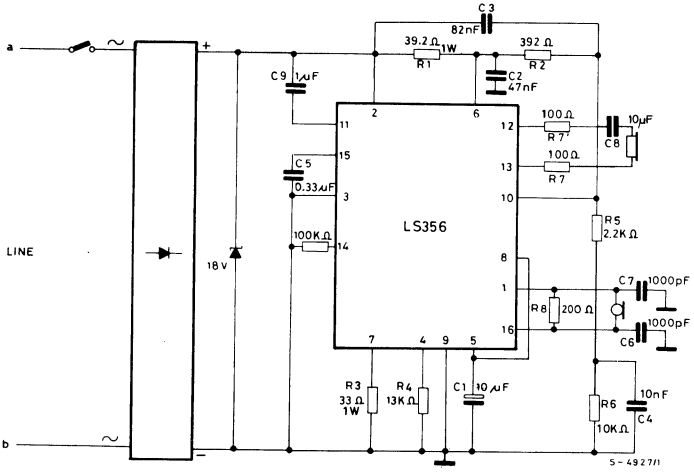
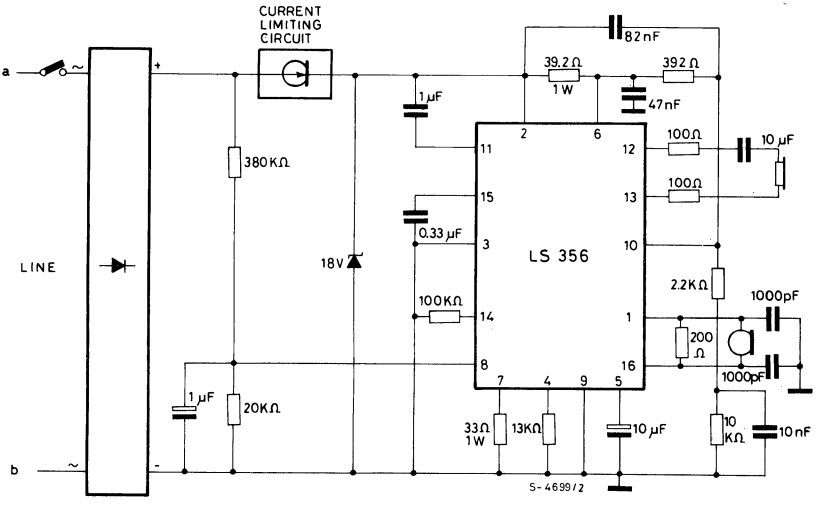
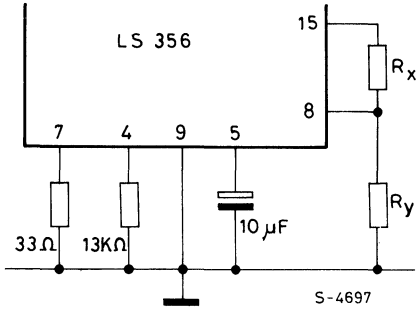


Fig. 13 - Application circuit with gain controlled by line voltage (French standard)



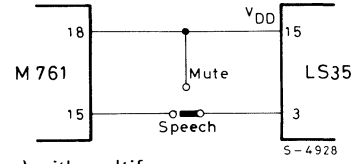
APPLICATION INFORMATION (continued)

Fig. 14 - Application circuit with fixed gain operation

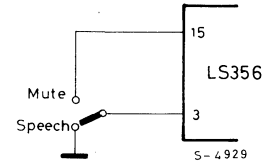


$R_y = 0$ Max gain condition
$R_x = 0$ Min gain condition

Fig. 15 - External mute function



a) with multifrequency



b) without multifrequency

In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.
The following table (refer to the application circuit of fig. 9) can help the designers.

Component	Value	Purpose	Note
R1	39.2 Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1W. The ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristic (see R3 note).
R2	392 Ω		
R3	33 Ω	Line current sensing. Fixing DC characteristic	The relationships involving R3 are: – $Z_{ML} = (20\ R3//Z_B) + R1$ – $G_s = K \cdot \frac{Z_L//Z_{ML}}{R3}$ – $V_L = (I_L - I_o)(R3 + R1) + V_o$; $V_o = 3.8V$. Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900 Ω. As far as the power dissipation is concerned, see R1 note.

APPLICATION INFORMATION (continued)

Component	Value	Purpose	Note
R4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point.
R5	2.2 KΩ	Balance Network	It is possible to change R5 and R6 values in order to improve the matching to different lines; in any case:
R6	10 KΩ		$\frac{Z_B}{Z_L} = \frac{R2}{R1}$ $Z_B = R5 + R6//X_{C4}$
R7-R7'	100 Ω	Receiver impedance matching	R7 and R7' must be equal; the suggested value is good for matching to dynamic capsule; there is no problem in increasing and decreasing (down to 0 Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop the current due to the receiver output offset voltage (max 200 mV).
R8	200 Ω	Microphone impedance matching	The suggested value is typical for a dynamic microphone, but it is possible to choose R8 in a wide range.
C1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47 nF	Matching to a capacitive line	C2 changes with the characteristics of the transmission line.
C3	82 nF	Receiving gain flatness	C3 depends on balancing and line impedance versus frequency
C4	10 nF	Balance, network	See note for R5, R6
C5	0.33 μF	DC filtering	The C5 range is from 0.1 μF to 0.47 μF. The lowest value is ripple limited, the higher value is starting up time limited.
C6-C7	1000 pF	RF bypass	
C8	10 μF	Receiving output DC decoupling	See note for R7, R7'.
C9	1 μF	Receiving input DC decoupling	

LS 404
LS 404C

LINEAR INTEGRATED CIRCUITS

HIGH PERFORMANCE QUAD OPERATIONAL AMPLIFIERS

- SINGLE OR SPLIT SUPPLY OPERATION
- VERY LOW POWER CONSUMPTION
- SHORT CIRCUIT PROTECTION
- LOW DISTORTION, LOW NOISE
- HIGH GAIN-BANDWIDTH PRODUCT
- HIGH CHANNEL SEPARATION

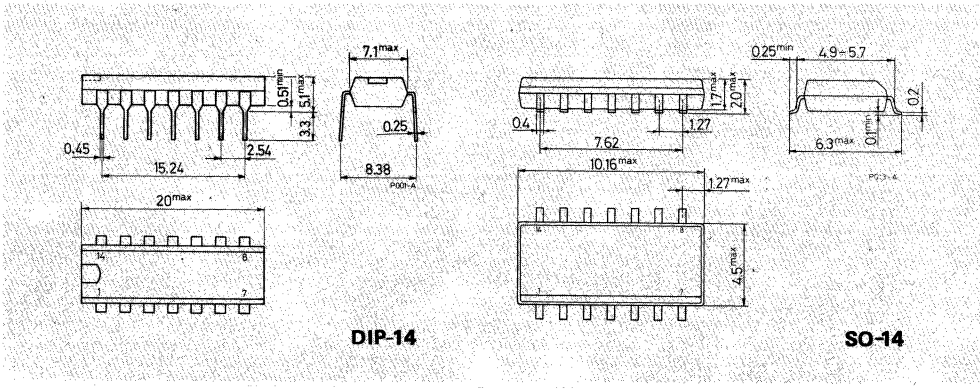
The LS 404 is a high performance quad operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth product. The circuit presents very stable electrical characteristics over the entire supply voltage range, and it is particularly intended for professional and telecom applications (active filters, etc.).
The patented input stage circuit allows small input signal swings below the negative supply voltage and prevents phase inversion when the input is over driven.
The LS 404 is available with hermetic gold chip (8000 series).

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_i	Input voltage	(positive)	$+ V_s$	
		(negative)	$-V_s - 0.5$	V
V_i	Differential input voltage		± (V_s - 1)	
T_{op}	Operating temperature	**LS 404**	-25 to + 85	°C
		LS 404C	0 to + 70	°C
P_{tot}	Power dissipation	(T_{amb} = 70°C)	400	mW
T_{stg}	Storage temperature		-55 to + 150	°C

MECHANICAL DATA

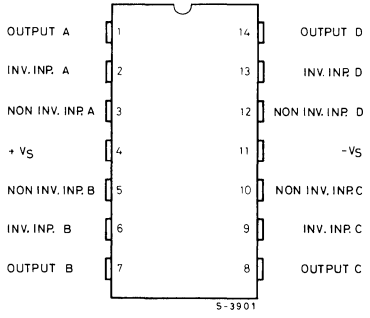
Dimensions in mm



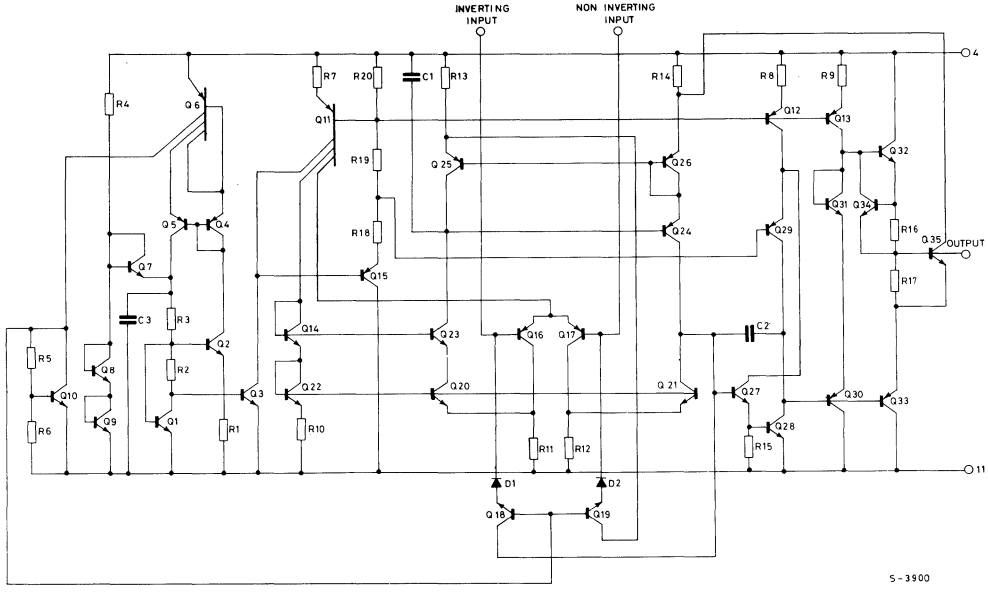
CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)

Type	DIP 14	SO-14
LS 404 LS 404C	— LS 404CB	LS 404M LS 404CM
LS 8404 LS 8404C	— —	LS 8404M LS 8404CM



SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			DIP 14	SO-14
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	200°C/W	200°C/W*

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm.)

ELECTRICAL CHARACTERISTICS ($V_s = \pm 12V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	LS 404			LS 404C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current			1.3	2		1.5	3	mA
I_b	Input bias current			50	200		100	300	nA
R_i	Input resistance	f = 1KHz		0.7			0.5		MΩ
V_{os}	Input offset voltage	R_g = 10KΩ		1	2.5		1	5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	R_g = 10KΩ $T_{min} < T_{op} < T_{max}$		5			5		μV/°C
I_{os}	Input offset current			10	40		20	80	nA
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$T_{min} < T_{op} < T_{max}$		0.08			0.1		$\frac{nA}{°C}$
I_{sc}	Output short circuit current			23			23		mA
G_v	Large signal open loop voltage gain	R_L = 2KΩ V_s = ±12V V_s = ±4V	90	100 95		86	100 95		dB
B	Gain-bandwidth product	f = 20KHz	1.8	3		1.5	2.5		MHz
e_N	Total input noise voltage	f = 1KHz R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		8 10 18	15		10 12 20		$\frac{nV}{\sqrt{Hz}}$
d	Distortion	unity gain R_L = 2KΩ f = 1 KHz V_o = 2Vpp f = 20 KHz		0.01 0.03	0.04		0.01 0.03		%
V_o	DC output voltage swing	R_L = 2KΩ V_s = ± 12V V_s = ± 4V	± 10	 ± 3		± 10	 ± 3		V
V_o	Large signal voltage swing	f = 10KHz R_L = 10 KΩ R_L = 1 KΩ		22 20			22 20		Vpp
SR	Slew rate	unity gain R_L = 2KΩ	0.8	1.5			1		V/μs
CMR	Comm. mode rejection	V_i = 10V	90	94		80	90		dB
SVR	Supply voltage rejection	V_i = 1V f = 100Hz	90	94		86	90		dB
CS	Channel separation	f = 1KHz	100	120			120		dB

Fig. 1 - Supply current vs. supply voltage

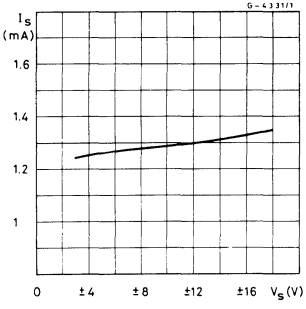


Fig. 2 - Supply current vs. ambient temperature

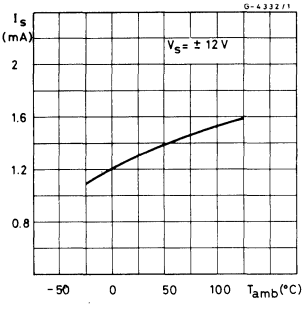


Fig. 3 - Output short circuit current vs. ambient temperature

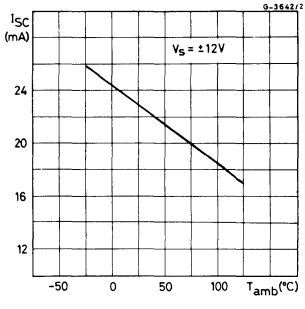


Fig. 4 - Open loop frequency and phase response

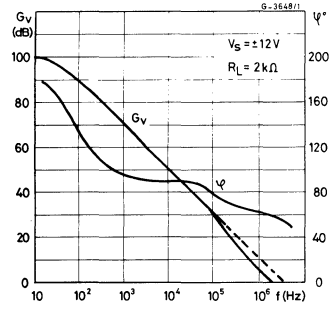


Fig. 5 - Open loop gain vs. ambient temperature

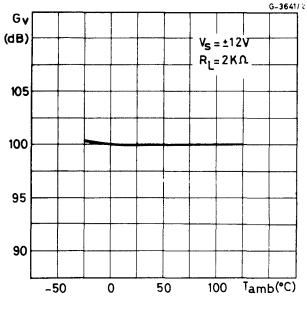


Fig. 6 - Supply voltage rejection vs. frequency

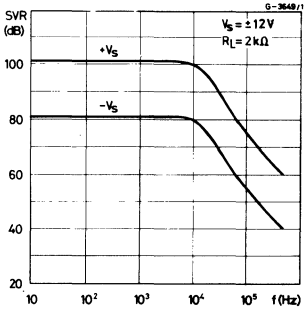


Fig. 7 - Large signal frequency response

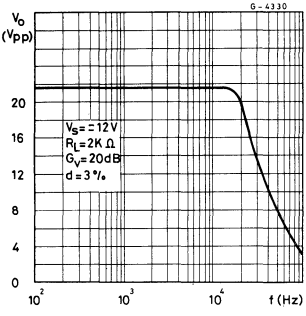


Fig. 8 - Output voltage swing vs. load resistance

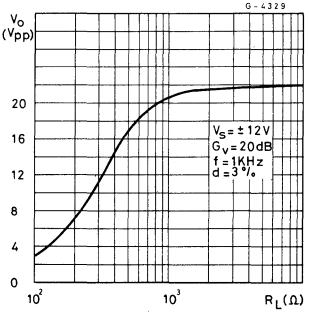
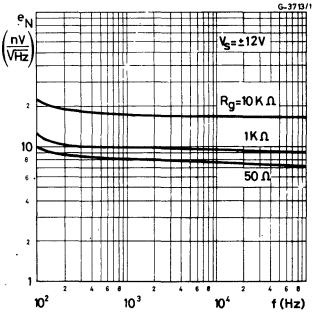


Fig. 9 - Total input noise vs. frequency



APPLICATION INFORMATION

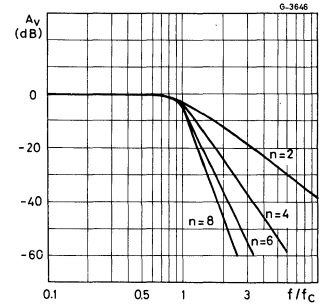
Active low-pass filter:

BUTTERWORTH

The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.
The cutoff frequency, f_c, is the frequency at which the amplitude response in down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.
Other characteristics:

- Flattest possible amplitude response.
- Excellent gain accuracy at low frequency end of passband.

Fig. 10 - Amplitude response



BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

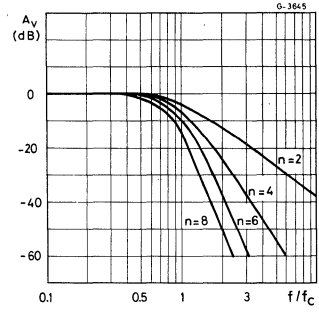
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half to this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
-3 dB frequency	0.77 f_c	0.67 f_c	0.57 f_c	0.50 f_c

Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth.
- Very small overshoot response to step inputs
- Fast rise time.

Fig. 11 - Amplitude response

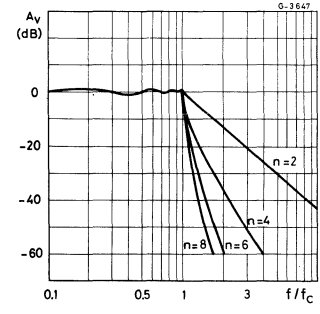


CHEBYSCHEV

Chebyschev filters have greater selectivity than either Bessel or Butterworth at the expense of ripple in the passband.
Chebyschev filters are normally designed with peak-to-peak ripple values from 0.2 dB to 2 dB.
Increased ripple in the passband allows increased attenuation above the cutoff frequency.
The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.
Other characteristics:

- Greater selectivity
- Very nonlinear phase response
- High overshoot response to step inputs.

Fig. 12 - Amplitude response (± 1 dB ripple)



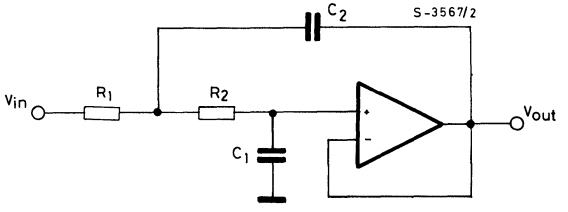
APPLICATION INFORMATION (continued)

The table below shows the typical overshoot and settling time response of the low pass filter to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	± 1%	± 0.1%	± 0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (RIPPLE ± 0.25 dB)	2	11	$1.1/f_c$	$1.6/f_c$	–
	4	18	$3.0/f_c$	$5.4/f_c$	–
	6	21	$5.9/f_c$	$10.4/f_c$	–
	8	23	$8.4/f_c$	$16.4/f_c$	–
CHEBYSCHEV (RIPPLE ± 1 dB)	2	21	$1.6/f_c$	$2.7/f_c$	–
	4	28	$4.8/f_c$	$8.4/f_c$	–
	6	32	$8.2/f_c$	$16.3/f_c$	–
	8	34	$11.6/f_c$	$24.8/f_c$	–

Design of 2nd order active low pass filter
(Sallen and Key configuration unity gain op-amp)

Fig. 13 - Filter configuration



$$\frac{V_o}{V_i} = \frac{1}{1 + 2\xi\frac{S}{\omega_c} + \frac{S^2}{\omega_c^2}}$$

where:

$\omega_c = 2\pi f_c$ with f_c = cutoff frequency

ξ = damping factor.

APPLICATION INFORMATION (continued)

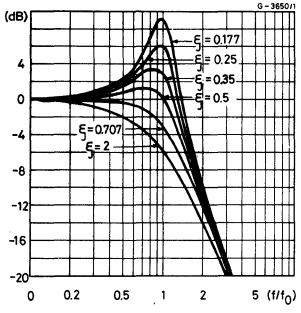
Three parameters are needed to characterize the frequency and phase response of a 2nd order active filter: the gain (G_v), the damping factor (ξ) or the Q-factor ($Q = (2\xi)^{-1}$), and the cutoff frequency (f_c).

The higher order responses are obtained with a series of 2nd order sections. A simple RC section is introduced when an odd filter is required. The choice of 'ξ' (or Q-factor) determines the filter response (see table).

TAB. 1

Filter response	ξ	Q	Cutoff frequency f_c
Bessel	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$	Frequency at which phase shift is -90°
Butterworth	$\frac{\sqrt{2}}{2}$	$\frac{1}{\sqrt{2}}$	Frequency at which G_v = -3 dB
Chebyschev	$< \frac{\sqrt{2}}{2}$	$> \frac{1}{\sqrt{2}}$	Frequency at which the amplitude response passes through specified max. ripple band and enters the stop band

Fig. 14 - Filter response vs. damping factor



Fixed $R = R_1 = R_2$, we have (see fig. 13)

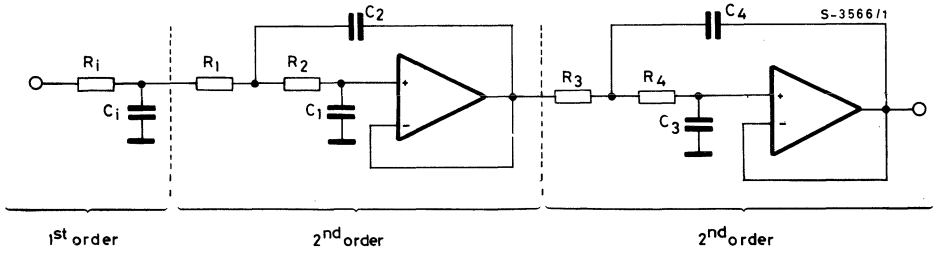
$$C_1 = \frac{1}{R}\frac{\xi}{\omega_c}$$

$$C_2 = \frac{1}{R}\frac{1}{\xi\,\omega_c}$$

The diagram of fig. 14 shows the amplitude response for different values of damping factor ξ in 2nd order filters.

EXAMPLE:

Fig. 15 - 5th order low pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

In the circuit of fig. 15, for f_c = 3.4 KHz and $R_i = R_1 = R_2 = R_3 = R_4 = 10\ K\Omega$, we obtain:

$$C_i = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33\ nF$$

$$C_1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97\ nF$$

$$C_2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20\ nF$$

$$C_3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45\ nF$$

$$C_4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 15.14\ nF$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Tab. II
Damping factor for low-pass Butterworth filters

Order	C_i	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
2		0.707	1.41						
3	1.392	0.202	3.54						
4		0.92	1.08	0.38	2.61				
5	1.354	0.421	1.75	0.309	3.235				
6		0.966	1.035	0.707	1.414	0.259	3.86		
7	1.336	0.488	1.53	0.623	1.604	0.222	4.49		
8		0.98	1.02	0.83	1.20	0.556	1.80	0.195	5.125

The same method, referring to Tab. II and fig. 16, is used to design high-pass filter. In this case the damping factor is found by taking the reciprocal of the numbers in Tab. II. For f_c = 5KHz and $C_i = C_1 = C_2 = C_3 = C_4 = 1$ nF we obtain:

$$R_i = \frac{1}{1.354} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 23.5\ K\Omega$$

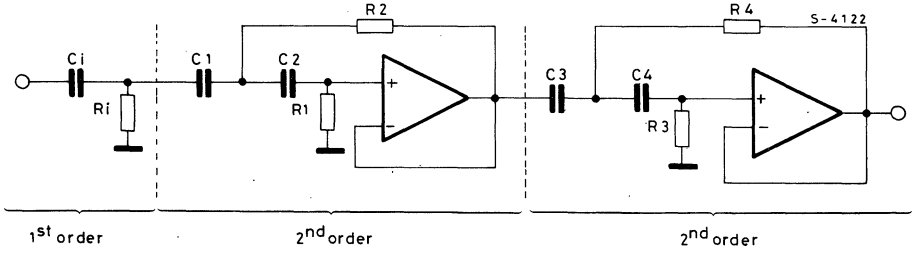
$$R_1 = \frac{1}{0.421} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 75.6\ K\Omega$$

$$R_2 = \frac{1}{1.753} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 18.2\ K\Omega$$

$$R_3 = \frac{1}{0.309} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 103\ K\Omega$$

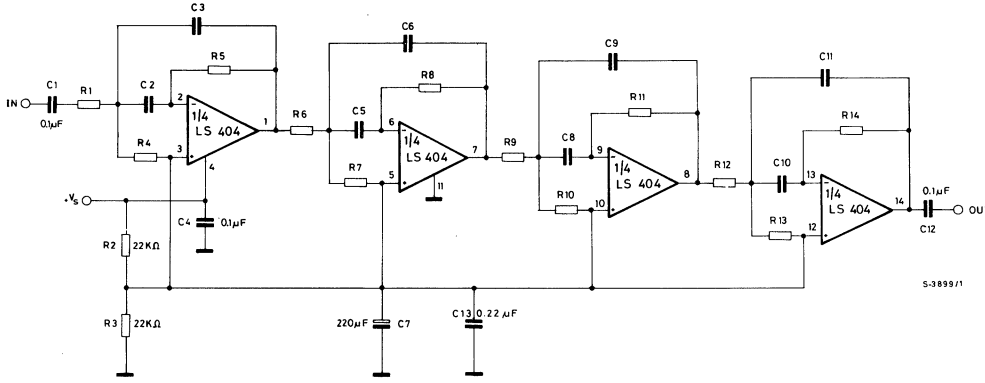
$$R_4 = \frac{1}{3.325} \cdot \frac{1}{C} \cdot \frac{1}{2\pi f_c} = 9.6\ K\Omega$$

Fig. 16 - 5th order high-pass filter (Butterworth) with unity gain configuration.



APPLICATION INFORMATION (continued)

Fig. 17 - Multiple feedback 8-pole bandpass filter.



f_c = 1.180Hz; A = 1; $C_2 = C_3 = C_5 = C_6 = C_8 = C_9 = C_{10} = C_{11}$ = 3.300 pF;
$R_1 = R_6 = R_9 = R_{12}$ = 160 KΩ; $R_5 = R_8 = R_{11} = R_{14}$ = 330KΩ; $R_4 = R_7 = R_{10} = R_{13}$ = 5.3KΩ

Fig. 18 - Frequency response of band-pass filter

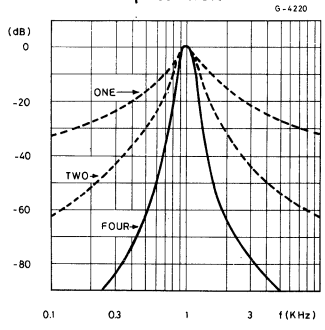
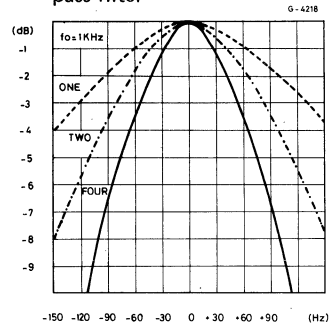


Fig. 19 - Bandwidth of band-pass filter



LINEAR INTEGRATED CIRCUIT

LS656

TELEPHONE SPEECH CIRCUIT WITH MULTIFREQUENCY TONE GENERATOR INTERFACE

The LS656 is a monolithic integrated circuit in 16-lead plastic package to replace the hybrid circuit in telephone set. It works with the same type of transducers for both transmitter and receiver (typically dynamic capsules). Many of its electrical characteristics can be controlled by means of external components to meet different specifications.
In addition to the speech operation, the LS656 acts as an interface for the MF tone signal (particularly for M761 C/MOS frequency synthesizer).
The LS656 basic functions are the following:

- It presents the proper DC path for the line current, **particular care being paid to have low voltage drop.**
- It handles the voice signal, performing the 2/4 wires interface and changing the gain on both sending and receiving amplifiers to compensate for line attenuation by sensing either the line current or the line voltage. **In addition, the LS656 can also work in fixed gain mode.**
- It acts as linear interface for MF, supplying a stabilized voltage to the digital chip and delivering to the line the MF tones generated by the M761.

DEVICE DATA

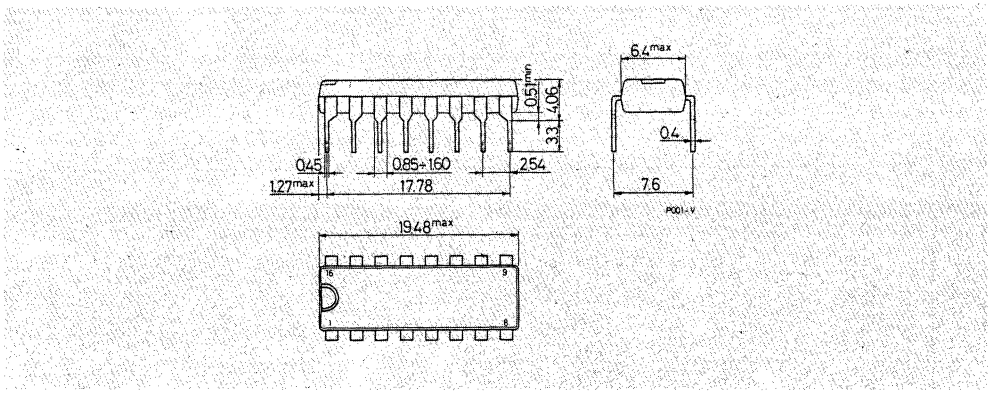
ABSOLUTE MAXIMUM RATINGS

V_L	Line voltage (3 ms pulse duration)	22	V
I_L	Forward line current	150	mA
I_L	Reverse line current	-150	mA
P_{tot}	Total power dissipation at T_{amb}= 70°C	1	W
T_{op}	Operating temperature	-45 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

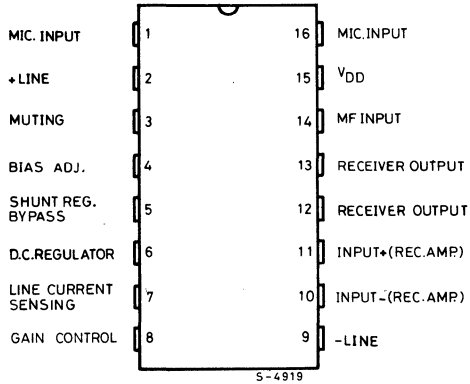
ORDERING NUMBER: LS656B

MECHANICAL DATA

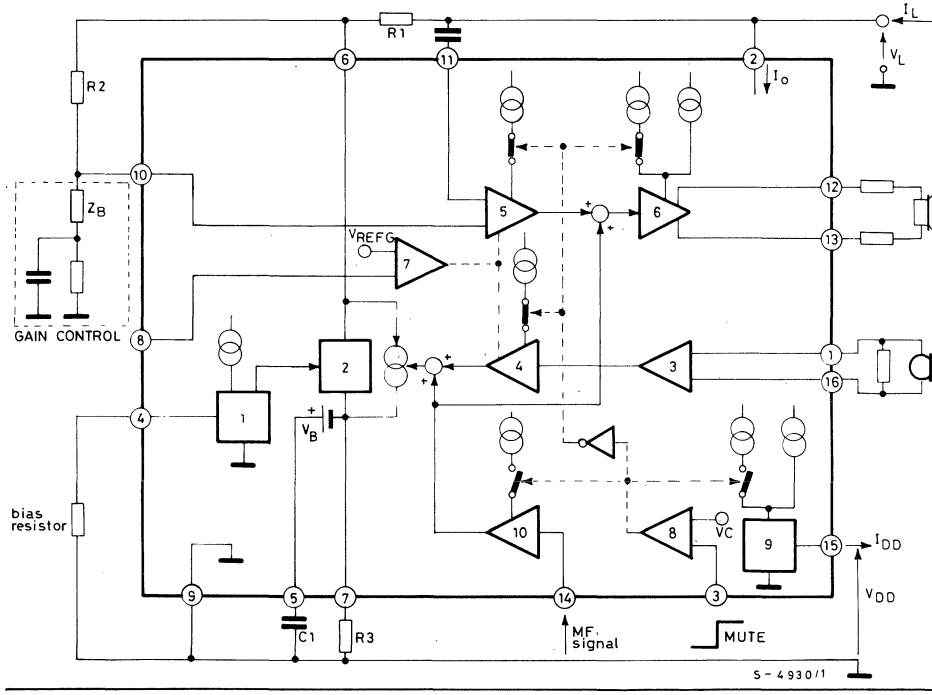
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



TEST CIRCUITS

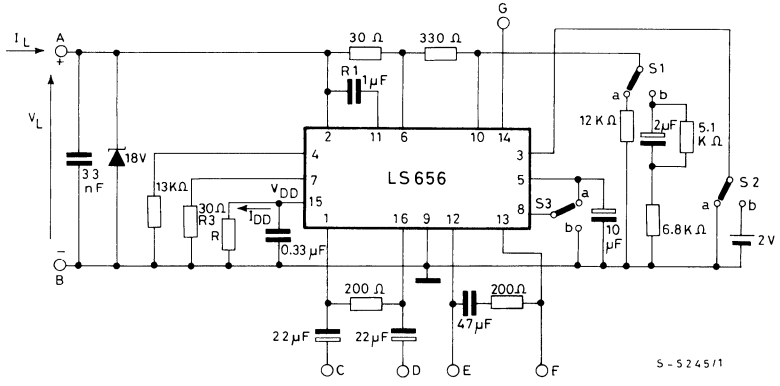
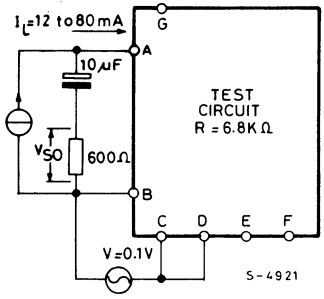
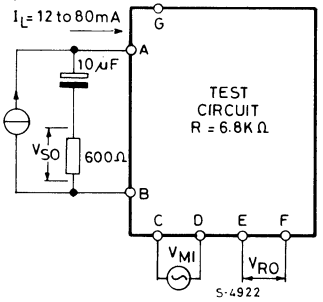


Fig. 1



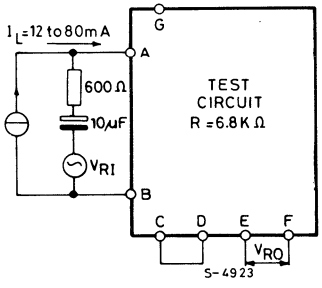
V = 0.1V CMRR

Fig. 2



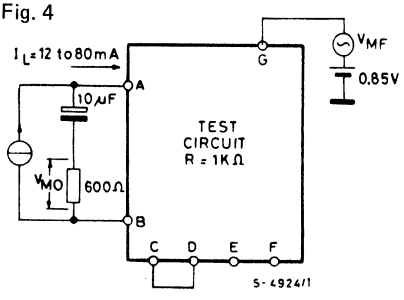
Side tone = $\frac{V_{RO}}{V_{MI}}$ Gs = $\frac{V_{SO}}{V_{MI}}$

Fig. 3



$G_R = \frac{V_{RO}}{V_{RI}}$

Fig. 4



$G_{MF} = \frac{V_{MO}}{V_{MF}}$

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_G = 1 to 2V, I_L = 12 to 80 mA, S1, S2 and S3 in (a), T_{amb} = 25 to +50°C, f = 200 to 3400 Hz, unless otherwise specified).

	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
SPEECH OPERATION							
V_L	Line voltage	T_{amb}= 25°C I_L= 12 mA I_L= 30 mA I_L= 60 mA			4 5 6.9	V	–
CMRR	Common mode rejection	f = 1 KHz	50			dB	1
G_s	Sending gain	T_{amb}= 25°C f= 1KHz I_L 25 mA V_{MI}= 3 mV I_L= 50 mA	48 44		50 46	dB	2
	Sending gain flatness (vs. freq.)	V_{MI}= 3 mV f_{ref}= 1 KHz			± 1	dB	2
	Sending gain flatness* (vs. current)	V_{MI}= 3 mV S3 in (b)			± 0.5	dB	2
	Sending distortion	f = 1 KHz V_{so}= 700 mV I_L= 15 mA V_{so}= 800 mV			2 10	% %	2
	Sending noise	V_{MI}= 0V; V_G= 1V		-70		dBmp	2
	Microphone input impedance (pin-16)	V_{MI}= 3 mV	40			KΩ	–
	Sending gain in MF operation	V_{MI}= 3 mV S2 in (b)	-30			dB	2
G_R	Receiving gain	V_{RI}= 0.3V I_L= 25 mA f = 1 KHz I_L= 50 mA T_{amb}= 25°C	-4 -8		-2 -6	dB	3
	Receiving gain flatness (vs. freq.)	V_{RI}= 0.3V f_{ref}= 1 KHz			± 1	dB	3
	Receiving gain flatness* (vs. current)				±0.5	dB	3
	Receiving distortion	f = 1 KHz V_{RO}= 440 mV I_L= 15 mA V_{RO}= 480 mV			2 10	% %	3
	Receiving noise	V_{RI}= 0V; V_G= 1V		150		μV	3
	Receiver output impedance (pin 12-13)	V_{RO}= 50 mV		30		Ω	–
	Sidetone	f = 1 KHz T_{amb}= 25°C S1 in (b)			36	dB	2
Z_{ML}	Line matching impedance	V_{RI}= 0.3V f = 1 KHz	500	600	700	Ω	3
I_8	Input current for gain control (pin 8)				-10	μA	–

* Fixed gain mode.

ELECTRICAL CHARACTERISTICS (continued)

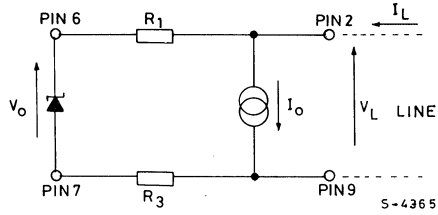
Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
MULTIFREQUENCY SYNTHESIZER INTERFACE							
V_{DD}	MF supply voltage Stand by and Operation	S2 in (b)	2.4	2.5		V	–
I_{DD}	MF supply current Stand by Operation	S2 in (b)	0.5 2			mA mA	– –
	MF amplifier gain	$f_{MF\ in}$= 1 KHz $V_{MF\ in}$= 80 mV	15		17	dB	4
V_I	DC input voltage level (pin 14)	$V_{MF\ in}$= 80 mV		0.3 V_{DD}		V	–
R_I	Input impedance (pin 14)	$V_{MF\ in}$= 80 mV	60			KΩ	–
d	Distortion	$V_{MF\ in}$= 150 mVp I_L > 15 mA			2	%	4
	Starting delay time				5	ms	–
	Muting threshold voltage (pin 3)	Speech operation			1	V	–
		MF operation	1.6			V	–
	Muting stand by current (pin 3)				-10	μA	–
	Muting operating current (pin 3)	S2 in (b)			+10	μA	–

CIRCUIT DESCRIPTION

1. DC characteristic

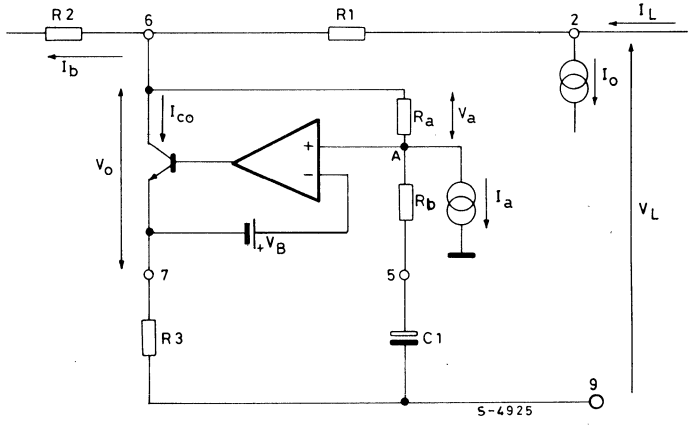
The fig. 5 shows the DC equivalent circuit of the LS656.

Fig. 5 - Equivalent DC load to the line



A fixed amount I_o of the total available current I_L is drained for the proper operation of the circuit. The value of I_o can be programmed externally by changing the value of the bias resistor connected to pin 4 (see block diagram).
The minimum value of I_o is 7.5 mA.
The voltage V_o= 37V of the shunt regulator is independent of the line current.
The shunt regulator (2) is controlled by a temperature compensated voltage reference (1) (see the block diagram).
Fig. 6 shows a more detailed circuit configuration of the shunt regulator.

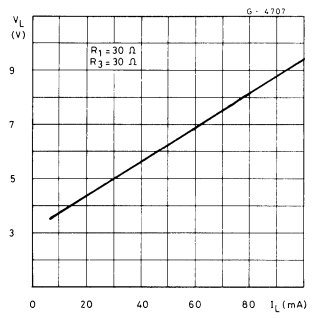
Fig. 6 - Circuit configuration of the shunt regulator



The difference I_L-I_o flows through the shunt regulator being I_b negligible. I_a is an internal constant current generator; hence $V_o = V_B + I_a \cdot R_a = 3.7V$.
The V_L, I_L characteristic of the device is therefore similar to a pure resistance in series to a battery.

It is important to note that the DC voltage at pin 5 is proportional to the line current ($V_5 = V_7 + V_B = (I_L - I_o)\ R3 + V_B$).
The DC characteristic of the LS656 is shown in fig. 7.

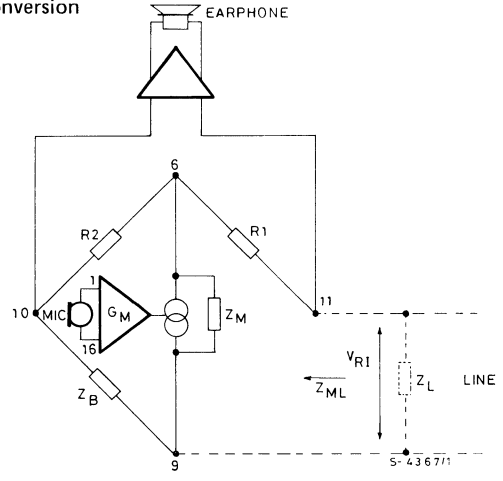
Fig. 7 - DC characteristic



2. Two to four wires conversion

The LS656 performs the two wires (line) to four wires (microphone, earphone) conversion by means of a Wheatstone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see fig. 8).

Fig. 8 - Two to four wires conversion



For a perfect balancing of the bridge $\frac{Z_L}{Z_B} = \frac{R1}{R2}$.

The AC signal from the microphone is sent to one diagonal of the bridge (pin 6 and 9). A small percentage of the signal power is lost on Z_B (being $Z_B \gg Z_L$); the main part is sent to the line via R1. In receiving mode, the AC signal coming from the line is sensed across the second diagonal of the bridge (pin 11 and 10). After amplification it is applied to the receiving capsule.
The impedance Z_M is simulated by the shunt regulator that is also intended to work as a transconductance amplifier for the transmission signal.

APPLICATION INFORMATION (continued)

The impedance Z_M is defined as $\frac{\Delta V_{6-9}}{\Delta I_{6-9}}$.

From fig. 6 considering C1 as a short circuit for AC signal, any variation ΔV_6 generates a variation:

$$\Delta V_7 = \Delta V_A = \Delta V_6 \cdot \frac{R_b}{R_a + R_b}$$

The corresponding current change is

$$\Delta I = \frac{\Delta V_7}{R3}$$

Therefore

$$Z_M = \frac{\Delta V_6}{\Delta I} = R3\,(1 + \frac{R_a}{R_b})$$

The total impedance across the line connections (pin 11 and 9) is given by

$$Z_{ML} = R1 + Z_M // (R2 + Z_B)$$

By choosing $Z_M \gg R1$ and $Z_B \gg Z_M$

$$Z_{ML} \cong Z_M = R3\,(1 + \frac{R_a}{R_b})$$

The received signal amplitude across pin 11 and 10 can be changed using different values of R1 (of course the relationship $Z_L/Z_B = R1/R2$ must be always valid).
The received signal is related to R1 value according to the approximated relationship:

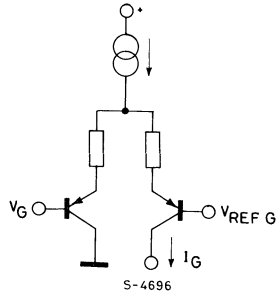
$$V_R = 2\,V_{RI}\,\frac{R1}{R1 + Z_M}$$

Note that by changing the value of R1, the transmission signal current is not changed, being the microphone amplifier a transconductance amplifier.

3. Automatic gain control

The LS656 automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation.
This function is performed by the circuit of fig. 9.

Fig. 9



The differential stage is progressively unbalanced by changing V_G in the range 1 to 2V (V_{REFG} is an internal reference voltage, temperature compensated).
It changes the current I_G, and this current is used as a control quantity for the variable gain stages (amplifier (4) and (5) in the block diagram). The voltage V_G can be taken:

a) from the LS656 itself (both in variable and in fixed mode) and.

b) from a resistive divider, directly at the end of the line.

a) In the first case, connecting V_G (pin 8) to the regulator bypass (pin 5) it is possible to obtain a gain characteristic depending on the current.
In fact (see fig. 6)

$$V_5 = V_B + V_7 \cong V_B + (I_L - I_o)\, R3$$

The starting point of the automatic level control is obtained at $I_L = 25$ mA when the drain current $I_o = 7.5$ mA.
Minimum gain is reached for a line current of about 50 mA for the same drain current $I_o = 7.5$ mA.
When I_o is increased by means of the external resistor connected to pin 4, the two above mentioned values of the line current for the starting point and for the minimum gain increase accordingly.
It is also possible to change the starting point without changing I_o by connecting pin 8 to the centre of a resistive divider placed between pin 5 and ground (the total resistance seen by pin 5 must be at least 100 KΩ). In this case, the AGC range increases too; for example using a division 1:1 (50K/50K) the AGC starting point shifts to about $I_L = 40$ mA, and the minimum gain is obtained at $I_L = 95$ mA.
In addition to this operation mode, the V_G voltage can be maintained constant thus fixing the gain values (Rx, Tx) independently of the line conditions.
For this purpose the V_{DD} voltage, available for supplying the MF generator, can be used.

b) When gains have to be related to the voltage at the line terminals of the telephone set, it is necessary to obtain V_G from a resistive divider directly connected to the end of the line.
This type of operation meets the requirements of the French standard. (See the application circuit of fig. 13).

4. Transducer interfacing

The microphone amplifier (3) has a differential input stage with high impedance (≅ 40 KΩ) so allowing a good matching to the microphone by means of external resistor without affecting the sending gain.
The receiving output stage (6) is particularly intended to drive dynamic capsules. (Low output impedance (100Ω max); high current capability 3 mAp).
When a piezoceramic capsule is used, it is useful to increase the receiving gain by increasing R1 value (see the relationship for V_R).
Whit very low impedance transducer, DC decoupling by an external capacitor must be provided to prevent a large DC current flow across the transducer itself due to the receiving output stage offset.

5. Multifrequency interfacing

The LS656 acts as a linear interface for the Multifrequency synthesizer M761 according to a logical signal (mute function) present on pin 3.
When no key of the keyboard is pressed the mute state is low and the LS656 feeds the M761 through pin 15 with low voltage and low current (standby operation of the M761). The oscillator of the M761 is not operating.

When one key is pressed, the M761 sends a "high state" mute condition to the LS656. A voltage comparator (8) of LS656 drives internal electronic switches; the voltage and the current delivered by the voltage supply (9) are increased to allow the operation of the oscillator.
This extra current is diverted by the receiving and sending section of the LS656 and during this operation the receiving output stage is partially inhibited and the input stages of sending and receiving amplifiers are switched OFF.
A controlled amount of the signalling is allowed to reach the earphone to give a feedback to the subscriber; the MF amplifier (10) delivers the dial tones to the sending paths.
The mute function can be used also when a temporary inhibition of the output signal is requested.
The application circuit shown in fig. 10 fulfils the EUROPE II standard (-6, -8 dBm). If the EUROPE I levels are required (-9, -11 dBm) an external divider must be used (see fig. 11).

APPLICATION INFORMATION

Fig. 10 - Application circuit with multifrequency (EUROPE II STD)

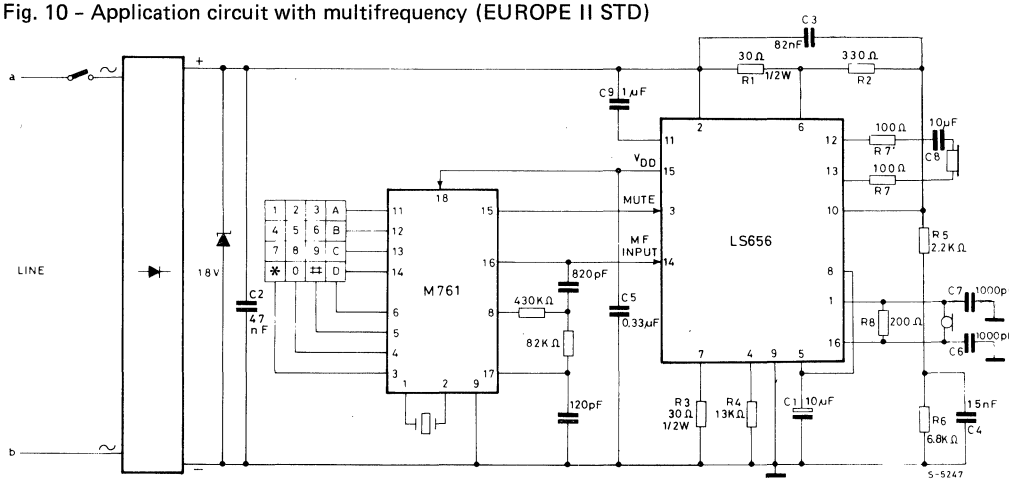
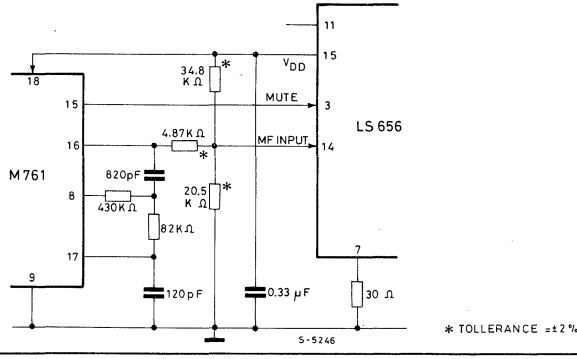


Fig. 11 - Application circuit with multifrequency (EUROPE I STD)



APPLICATION INFORMATION (continued)

Fig. 12 - Sending and receiving gain vs. line current (application circuit of fig.10)

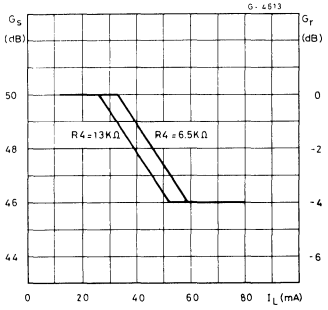


Fig. 13 - Application circuit without multifrequency

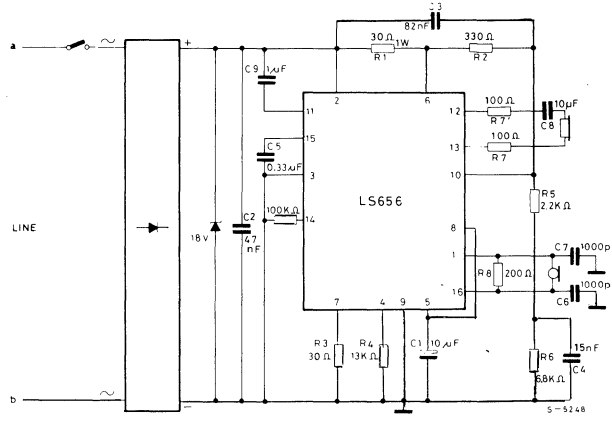
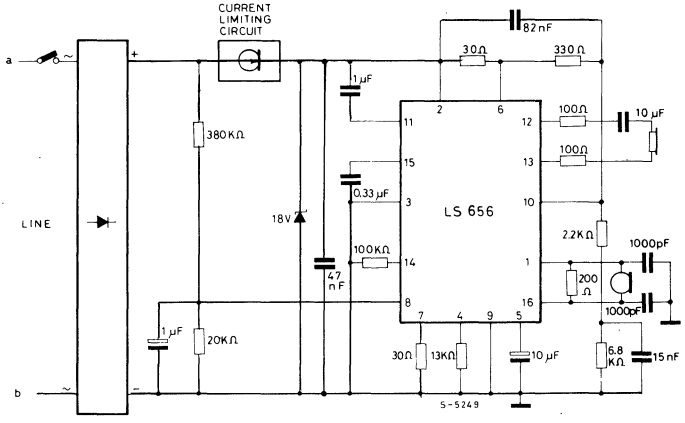
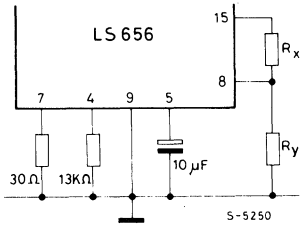


Fig. 14 - Application circuit with gain controlled by line voltage (French standard)



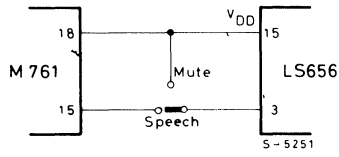
APPLICATION INFORMATION (continued)

Fig. 15 - Application circuit with fixed gain operation

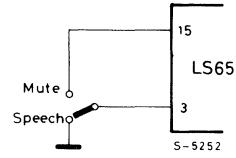


R_y= 0 Main gain condition
R_x= 0 Main gain condition

Fig. 16 - External mute function



a) with multifrequency



b) without multifrequency

In addition to the above mentioned applications, different values for the external components can be used in order to satisfy different requirements.
The following table (refer to the application circuit of fig. 10) can help the designers.

Component	Value	Purpose	Note
R1	30 Ω	Bridge Resistors	R1 controls the receiving gain. When high current values are allowed, R1 must be able to dissipate up to 1W. The ratio R2/R1 fixes the amount of signal delivered to the line. R1 helps in fixing the DC characteristics (see R3 note).
R2	330 Ω		
R3	30 Ω	Line current sensing. Fixing DC characteristic.	The relationships involving R3 are: – Z_{ML}= (20 R3//Z_B) + R1 – $G_s = K \cdot \frac{Z_L//Z_{ML}}{R3}$ – $V_L = (I_L - I_o)$ (R3 + R1) + V_o; V_o= 3.7V. Without any problem it is possible to have a Z_{ML} ranging from 600 up to 900Ω. As far as the power dissipation is concerned, see R1 note.
R4	13 KΩ	Bias Resistor	The suggested value assures the minimum operating current. It is possible to increase the supply current by decreasing R4 (they are inversely proportional), in order to achieve the shifting of the AGC starting point. (See fig. 16). After R4 changement, some variations could be found also in other parameters, i.e. line voltage.

Component	Value	Purpose	Note
R5	2.2 KΩ	Balance Network	It's possible to change R5 and R6 values in order to improve the matching to different lines; in any case: $\frac{Z_B}{Z_L} = \frac{R2}{R1}$ $Z_B = R5 + R6//X_{C4}$
R6	6.8 KΩ		
R7–R7'	100 Ω	Receiver impedance matching	R7 and R7' must be equal; the suggested value is good for matching to dynamic capsule; there is no problem in increasing and decreasing (down to 0Ω) this value. A DC decoupling must be inserted when low resistance levels are used to stop the current due to the receiver output offset voltage (max 200 mV).
R8	200 Ω	Microphone impedance matching	The suggested value is typical for a dynamic microphone, but it is possible to choose R8 in a wide range.
C1	10 μF	Regulator AC bypass	A value greater than 10 μF gives a system start time too high for low current line during MF operation; a lower value gives an alteration of the AC line impedance at low frequency.
C2	47 nF	Matching to a capacitive line	C2 changes with the characteristics of the transmission line.
C3	82 nF	Receiving gain flatness	C3 depends on balancing and line impedance versus frequency.
C4	15 nF	Balance network	See note for R5, R6.
C5	0.33 μF	DC filtering	The C5 range is from 0.1 μF to 0.47 μF. The lowest value is ripple limited, the higher value is starting up time limited.
C6–C7	1000 pF	RF bypass	
C8	100 μF	Receiving output DC decoupling	See note for R7, R7.
C9	1 μF	Receiving input DC decoupling	

LS709
LS709A
LS709C

LINEAR INTEGRATED CIRCUITS

OPERATIONAL AMPLIFIERS

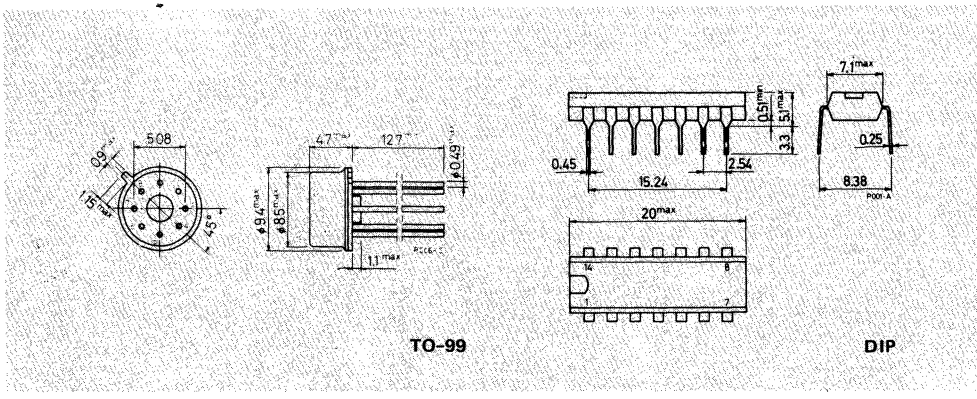
The LS 709 series features low offset, high input impedance, large input common mode range, high output voltage swing. The amplifier is intended for use in D.C. servosystems, high impedance analog computer, low level instrumentation applications, and for the generation of special linear and non linear transfer functions.

ABSOLUTE MAXIMUM RATINGS		TO-99	DIP
V_s	Supply voltage	± 18 V	
V_i (1)	Input voltage	± 10 V	
ΔV_i	Differential input voltage	± 5 V	
T_{op}	Operating temperature for **LS 709/LS 709A**	-55 to 125 °C	
	for **LS 709C**	0 to 70 °C	
P_{tot}	Power dissipation at T_{amb} = 70 °C	520 mW	400 mW
T_{stg}	Storage temperature	-65 to 150 °C	-55 to 150 °C

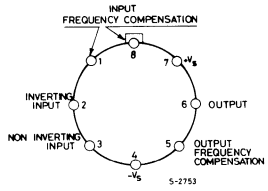
1) For supply voltages less than ± 10V maximum input voltage is equal to the supply voltage.

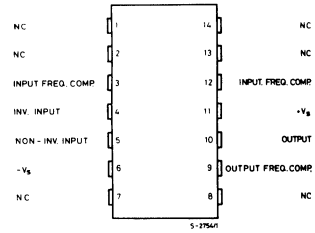
MECHANICAL DATA

Dimensions in mm



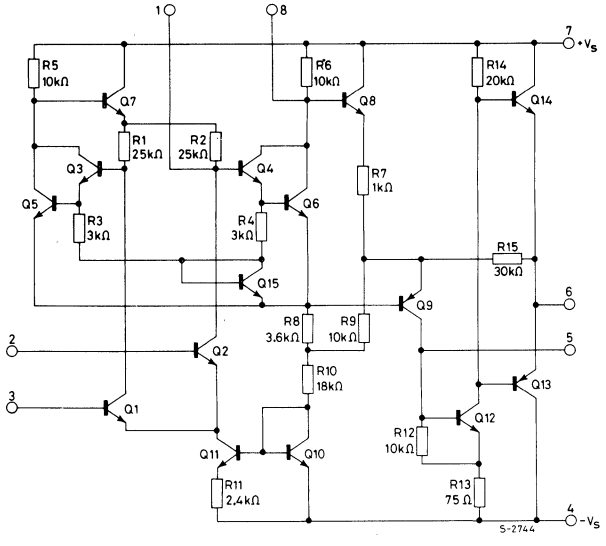
CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)





Type	TO-99	DIP
LS 709	LS 709T	—
LS 709A	LS 709 AT	—
LS 709C	LS 709 CT	LS 709 CB

SCHEMATIC DIAGRAM (pin numbers are referred to the TO-99 version)



THERMAL DATA

			TO-99	DIP
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	155 °C/W	200 °C/W

ELECTRICAL CHARACTERISTICS (see note)

Parameter		Test conditions	LS 709A			LS 709			LS 709C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{os}	Input offset voltage	$R_g \leq 10\ k\Omega$ $R_g \leq 10\ k\Omega$ $T_{amb}=25°C$		 0.6	3 2		 1	6 5		 2	10 7.5	mV mV
I_b	Input bias current	$T_{amb}=T_{min}$ $T_{amb}=25°C$		0.3 100	0.6 200		0.5 200	1.5 500		0.36 300	2 1500	μA nA
I_{os}	Input offset current	$T_{amb}=T_{max}$ $T_{amb}=T_{min}$ $T_{amb}=25°C$		3.5 40 10	50 250 50		20 100 50	200 500 200		75 125 100	400 750 500	nA nA nA
R_i	Input resistance	$T_{amb}=T_{min}$ $T_{amb}=25°C$	85 350	170 700		40 150	100 400		50 50	250 250		kΩ kΩ
R_o	Output resistance	$T_{amb}=25°C$		150			150			150		Ω
I_s	Supply current	$V_s=\pm15V$ $T_{amb}=25°C$		2.5	3.6		2.6	5.5		2.6	6.6	mA
	Transient response Risetime Overshoot	$V_i=20$ mV $C_L \leq 100$ pF $T_{amb}=25°C$			1.5 30		0.3 10	1 30		0.3 10	1 30	μs %
SR	Slew rate	$T_{amb}=25°C$		0.25			0.25			0.25		V/μs
$\frac{\Delta V_{os}}{\Delta T}$	Average temperature coefficient of input offset voltage	$R_g=50\Omega$ $T_{amb}=25°C$ to T_{max} $T_{amb}=25°C$ to T_{min} $R_g=10\ k\Omega$ $T_{amb}=25°C$ to T_{max} $T_{amb}=25°C$ to T_{min}		 1.8 1.8 2 4.8	 10 10 15 25		 3 6 			 6 12 		 μV/°C μV/°C μV/°C μV/°C
G_v	Large signal voltage gain	$V_s=\pm15V$ $R_L \geq 2\ k\Omega$ $V_o=\pm10V$	88	93	97	88	93	97	83	93		dB
V_o	Output voltage swing	$V_s=\pm15V$ $R_L=10\ k\Omega$ $V_s=\pm15V$ $R_L=2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
V_i	Input voltage range	$V_s=\pm15V$	±8			±8	±10		±8	±10		V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	80	110		70	90		65	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	80	88		76	92		74	92		dB

Note: These specifications, unless otherwise specified, apply for $T_{amb}=-55$ to 125°C for LS 709/LS 709A and $T_{amb}=0$ to 70°C for LS 709C with the following conditions: $V_s=\pm 9V$ to $\pm 15V$, C1= 5000 pF, R1= 1.5 kΩ, C2= 200 pF and R2= 51Ω. (See fig. 8 and fig. 17).

Fig. 1 - Voltage gain vs. supply voltage (for 709A)

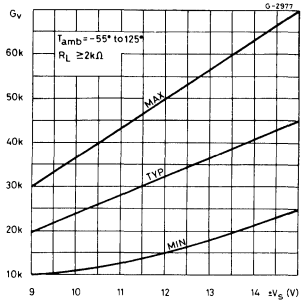


Fig. 2 - Output voltage swing vs. supply voltage (for 709A)

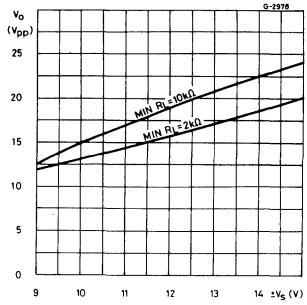


Fig. 3 - Input common mode voltage range vs. supply voltage (for 709A)

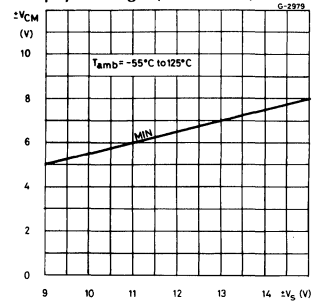


Fig. 4 - Power consumption vs. supply voltage (for 709A)

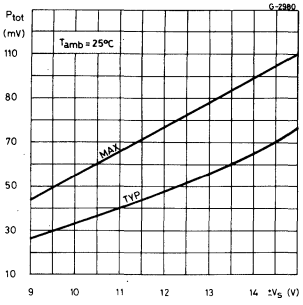


Fig. 5 - Output voltage swing vs. load resistance (for 709A)

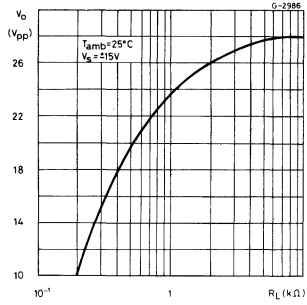


Fig. 6 - Input bias current vs. ambient temperature (for 709A)

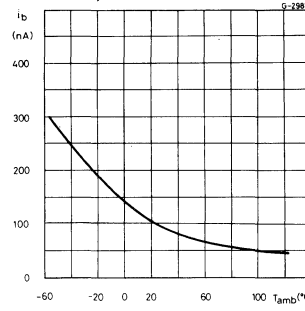


Fig. 7 - Input offset current vs. ambient temperature (for 709A)

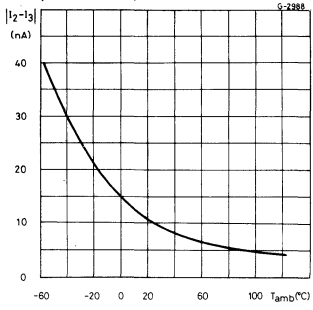


Fig. 8 - Transient response test circuit

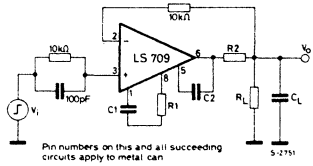
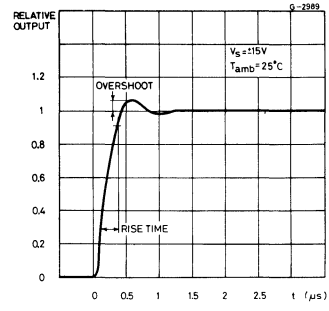


Fig. 9 - Transient response (for 709A)



LS709
LS709A
LS709C

Fig. 10 - Slew rate vs. closed loop gain using recommended compensation networks (for 709A)

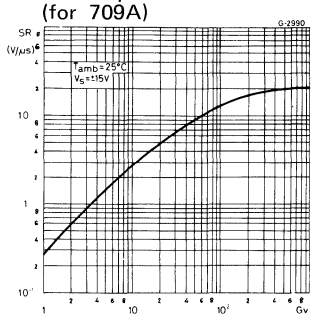


Fig. 11 - Voltage gain vs. supply voltage (for 709)

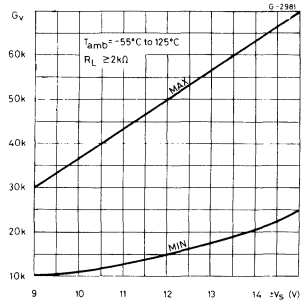


Fig. 12 - Output voltage swing vs. supply voltage (for 709 and 709C)

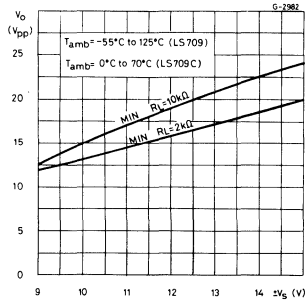


Fig. 13 - Voltage gain vs. supply voltage (for 709C)

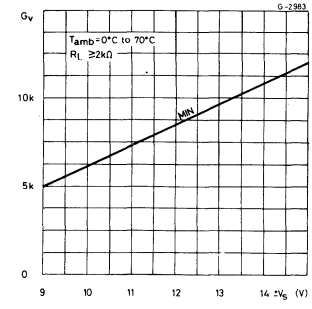


Fig. 14 - Input bias current vs. ambient temperature (for 709C)

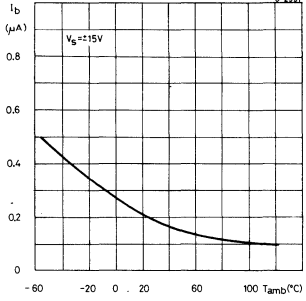
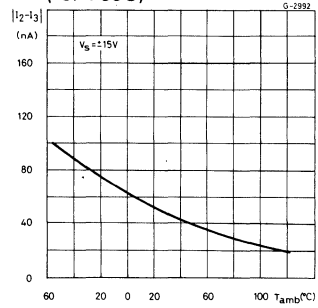


Fig. 15 - Input offset current vs. ambient temperature (for 709C)



Frequency compensation for all types

Fig. 16 - Open loop frequency response for various values of compensation

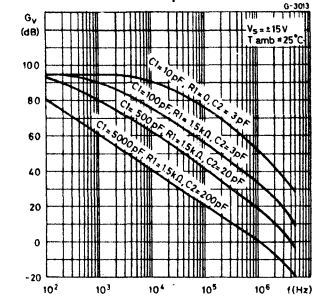


Fig. 17 - Frequency compensation circuit

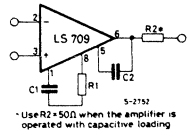
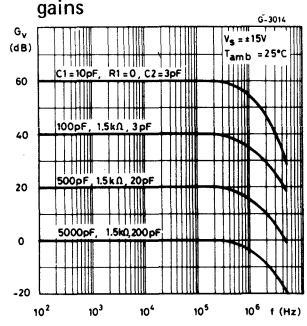


Fig. 18 - Frequency response for various closed loop gains



LINEAR INTEGRATED CIRCUITS

LS776
LS776C

PROGRAMMABLE OPERATIONAL AMPLIFIER

- MICROPOWER CONSUMPTION
- INTERNALLY FREQUENCY COMPENSATION
- OFFSET NULL CAPABILITY
- SHORT CIRCUIT PROTECTION
- LOW INPUT BIAS CURRENTS
- LOW NOISE

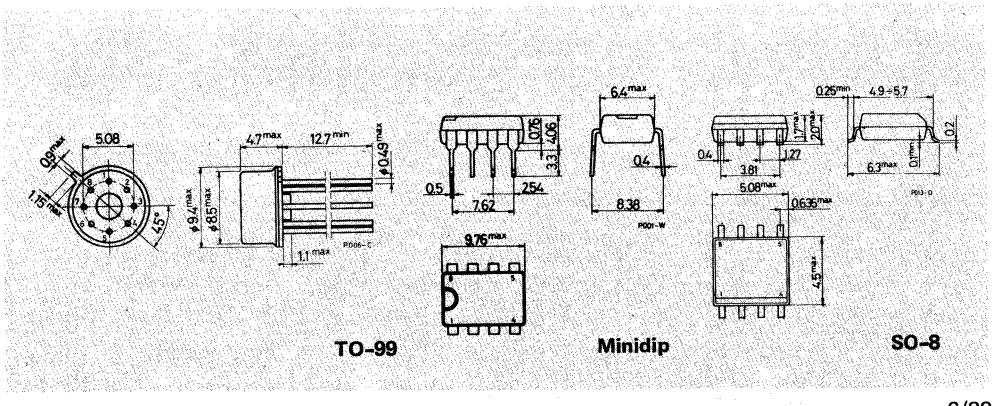
The LS 776 is a programmable operational amplifier available in three different packages (TO-99, Minidip and SO-8 micropackage). High input impedance, low supply currents and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics, make it an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption and input current can be optimized by a single resistor of current source that sets the quiescent current for nanowatt power consumption or for characteristics similar to the LS 141. Internal frequency compensation, absence of "latch-up", high slew rate and short circuit current protection assure ease of use in long interval integrators, active filters and sample and hold circuits. The LS 776 is available with hermetic gold chip (8000 Series).

ABSOLUTE MAXIMUM RATINGS		TO-99	Minidip	μpackage
V_s	Supply voltage		± 18V	
V_i (1)	Input voltage		± 15V	
ΔV_i	Differential input voltage		± 30V	
V_{SET}	Maximum voltage to ground at I_{SET}		V_s -2V to V_s	
I_{SET}	Maximum current at I_{SET}		500 μA	
T_{op}	Operating temperature for **LS 776**		-55 to 125 °C	
	for **LS 776 C**		0 to 70 °C	
	Output short circuit duration (2)		indefinite	
P_{tot}	Power dissipation at T_{amb}= 70 °C	520 mW	665 mW	400 mW
T_{sta}, T_j	Storage and junction temperature	-65 to 150 °C	-55 to 150 °C	-55 to 150 °C

1) For supply voltage less than ± 15V, input voltage is equal to the supply voltage
2) The short circuit duration is limited by thermal dissipation

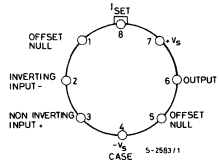
MECHANICAL DATA

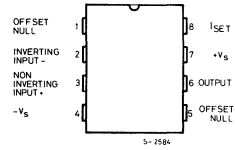
Dimensions in mm

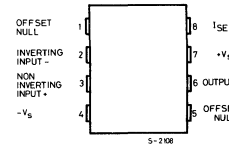


LS776
LS776C

CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)

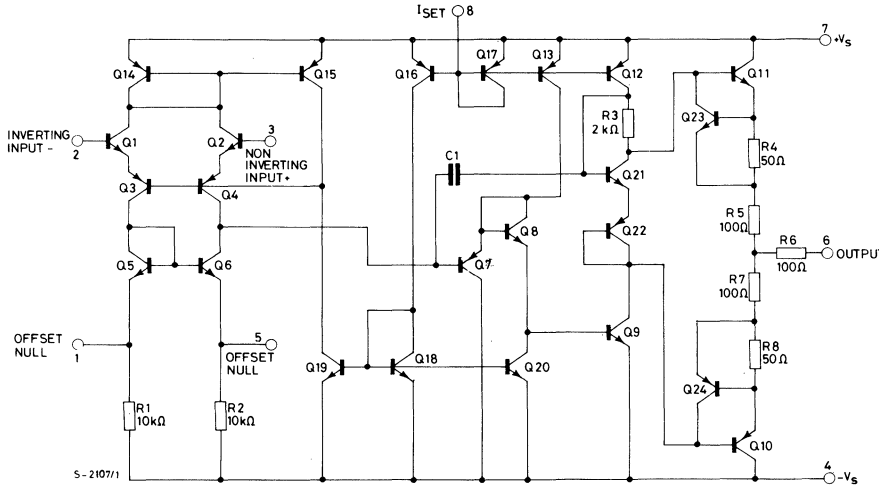






Type	TO-99	Minidip	SO-8
LS 776	LS 776T	—	—
LS 776C	LS 776CT	LS 776 CB	LS 776CM
LS 8776	—	—	LS 8776M
LS 8776C	—	—	LS 8776CM

SCHEMATIC DIAGRAM



THERMAL DATA			TO-99	Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	155 °C/W	120 °C/W	200* °C/W

* The thermal resistance is measured with device mounted on a ceramic substrate (25 x 16 x 0.6 mm)

ELECTRICAL CHARACTERISTICS for LS 776

(V_s= ± 15V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$		2	5		2	5	mV
I_{OS}	Input offset current	$R_g \leq 10\ k\Omega$		0.7	3		2	15	nA
I_b	Input bias current			2	7.5		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ V_o= ± 10 V	106	112					dB
		$R_L \geq 5\ k\Omega$ V_o= ± 10 V				100	112		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			12		mA
I_s	Supply current			20	25		160	180	μA
P_S	Power consumption				0.75			5.4	mW
	Transient response (unity gain)	V_i = 20 m V $R_L \geq 5\ k\Omega$ C_L= 100 pF							
	Rise time t_r			1.6			0.35		μs.
	Overshoot Δ V_o			0			10		%
SR	Slew rate	$R_L \geq 5\ k\Omega$		0.1			0.8		V/μs
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 12	± 14					V
		$R_L \geq 5\ k\Omega$				± 10	± 13		V
The following specifications apply for T_{amb}= -55 to 125 °C									
V_{OS}	Input offset voltage	$R_g \leq 10\ k\Omega$			6			6	mV
I_{OS}	Input offset current	T_{amb}= 125°C			5			15	nA
		T_{amb}= -55°C			10			40	nA
I_b	Input bias current	T_{amb}= 125°C			7.5			50	nA
		T_{amb}= -55°C			20			120	nA
V_i	Input voltage range		± 10			± 10			V
CMR	Common mode rejection	$R_g \leq 10\ k\Omega$	70	90		70	90		dB
SVR	Supply voltage rejection	$R_g \leq 10\ k\Omega$	76	92		76	92		dB
G_v	Large signal voltage gain	$R_L \geq 75\ k\Omega$ V_o= ± 10V	100			98			dB
V_o	Output voltage swing	$R_L \geq 75\ k\Omega$	± 10			± 10			V
I_s	Supply current				30			200	μA
P_S	Power consumption				0.9			6	mW

ELECTRICAL CHARACTERISTICS for LS 776

(V_s= ± 3V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ		2	5		2	5	mV
I_{OS}	Input offset current			0.7	3		2	15	nA
I_b	Input bias current			2	7.5		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	94	106					dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				94	106		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			5		mA
I_s	Supply current			13	20		130	160	μA
P_S	Power consumption			78	120		780	960	μW
	Transient response (unity gain)	V_i = 20 m V $R_L \geq$ 5 kΩ $C_L \leq$ 100 pF							
	Rise time t_r			3			0.6		μs
	Overshoot ΔV_o			0			5		%
SR	Slew rate	$R_L \geq$ 5 kΩ		0.03			0.35		V/μs
The following specifications apply for T_{amb}= -55 to 125°C									
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ			6			6	mV
I_{OS}	Input offset current	T_{amb}= 125°C			5			15	nA
		T_{amb}= -55°C			10			40	nA
I_b	Input bias current	T_{amb}= 125°C			7.5			50	nA
		T_{amb}= -55°C			20			120	nA
V_i	Input voltage range		± 1			± 1			V
CMR	Common mode rejection	$R_g \leq$ 10 kΩ	70	86		70	86		dB
SVR	Supply voltage rejection	$R_g \leq$ 10 kΩ	76	92		76	92		dB
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	88						dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				88			dB
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 2	± 2.4					V
		$R_L \geq$ 5 kΩ				± 1.9	± 2.1		V
I_s	Supply current				25			180	μA
P_S	Power consumption				150			1080	μW

ELECTRICAL CHARACTERISTICS for LS 776C

(V_s= ± 15V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ		2	6		2	6	mV
I_{OS}	Input offset current			0.7	6		2	25	nA
I_b	Input bias current			2	10		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 10V	94	112					dB
		$R_L \geq$ 5 kΩ V_o= ± 10V				94	112		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			12		mA
I_s	Supply current			20	30		160	190	μA
P_S	Power consumption				0.9			5.7	mW
	Transient response (unity gain)	V_i = 20 mV $R_L \geq$ 5 kΩ $C_L \leq$ 100 pF							
	Rise time t_r			1.6			0.35		μs
	Overshoot ΔV_o			0			10		%
SR	Slew rate	$R_L \geq$ 5 kΩ		0.1			0.8		V/μs
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 12	± 14					V
		$R_L \geq$ 5 kΩ				± 10	± 13		V
The following specifications apply for T_{amb}= 0 to 70°C									
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ			7.5			7.5	mV
I_{OS}	Input offset current	T_{amb}= 70°C			6			25	nA
		T_{amb}= 0°C			10			40	nA
I_b	Input bias current	T_{amb}= 70°C			10			50	nA
		T_{amb}= 0°C			20			100	nA
V_i	Input voltage range		± 10			± 10			V
CMR	Common mode rejection	$R_g \leq$ 10 kΩ	70	90		70	90		dB
SVR	Supply voltage rejection	$R_g \leq$ 10 kΩ	74	92		74	92		dB
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 10V	94			94			dB
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 10			± 10			V
I_s	Supply current				35			200	μA
P_S	Power consumption				1.05			6	mW

ELECTRICAL CHARACTERISTICS for LS 776C

(V_s= ± 3V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	I_{SET}= 1.5 μA			I_{SET}= 15 μA			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ		2	6		2	6	mV
I_{OS}	Input offset current			0.7	6		2	25	nA
I_b	Input bias current			2	10		15	50	nA
R_i	Input resistance			50			5		MΩ
C_i	Input capacitance			2			2		pF
ΔV_{OS}	Input offset voltage adjustment range			9			18		mV
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	88	106					dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				88	106		dB
R_o	Output resistance			5			1		kΩ
I_{sc}	Output short-circuit current			3			5		mA
I_s	Supply current			13	20		130	170	μA
P_S	Power consumption			78	120		780	1020	μW
	Transient response (unity gain)	V_i = 20 m V $R_L \geq$ 5 kΩ $C_L \leq$ 100 pF							
	Rise time t_r			3			0.6		μs
	Overshoot ΔV_o			0			5		%
SR	Slew rate	$R_L \geq$ 5 kΩ		0.03			0.35		V/μs
The following specifications apply for T_{amb}= 0 to 70°C									
V_{OS}	Input offset voltage	$R_g \leq$ 10 kΩ			7.5			7.5	mV
I_{OS}	Input offset current	T_{amb}= 70°C			6			25	nA
		T_{amb}= 0°C			10			40	nA
I_b	Input bias current	T_{amb}= 70°C			10			50	nA
		T_{amb}= 0°C			20			100	nA
V_i	Input voltage range		± 1			± 1			V
CMR	Common mode rejection	$R_g \leq$ 10 kΩ	70	86		70	86		dB
SVR	Supply voltage rejection	$R_g \leq$ 10 kΩ	74	92		74	92		dB
G_v	Large signal voltage gain	$R_L \geq$ 75 kΩ V_o= ± 1V	88						dB
		$R_L \geq$ 5 kΩ V_o= ± 1V				88			dB
V_o	Output voltage swing	$R_L \geq$ 75 kΩ	± 2	± 2.4					V
		$R_L \geq$ 5 kΩ				± 2	± 2.1		V
I_s	Supply current				25			180	μA
P_S	Power consumption				150			1080	μW

Fig. 1 - Input bias current vs. set current

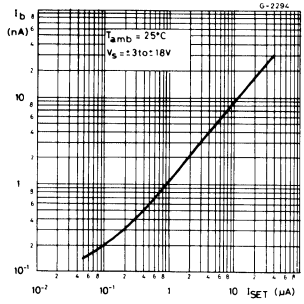


Fig. 2 - Input bias current vs. ambient temperature

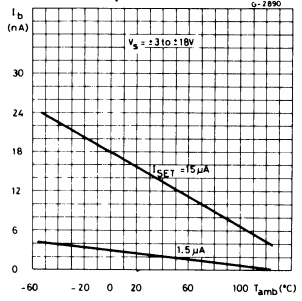


Fig. 3 - Input offset current vs. ambient temperature

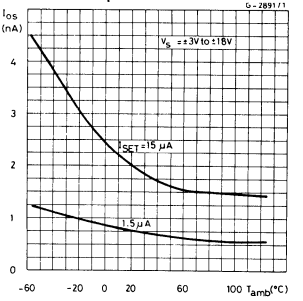


Fig. 4 - Change in input offset voltage vs. set current

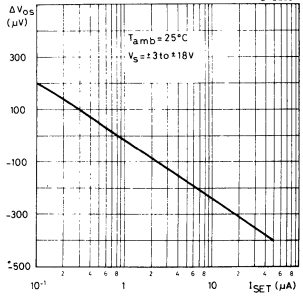


Fig. 5 - Change in input offset voltage vs. ambient temperature (unnulled)

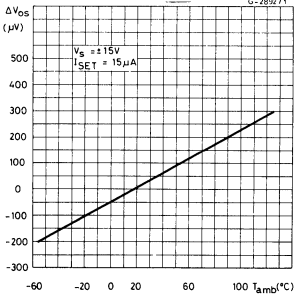


Fig. 6 - Input noise voltage vs. set current

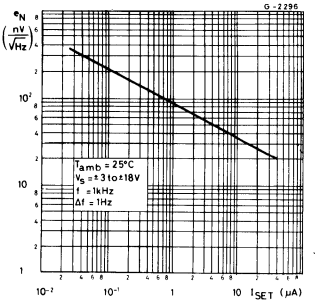


Fig. 7 - Input noise voltage and current vs. frequency

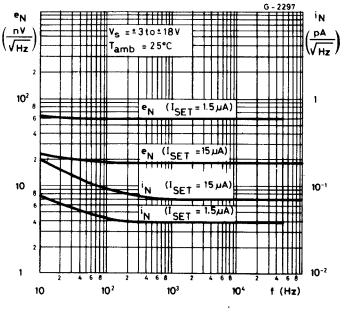


Fig. 8 - Input noise current vs. set current

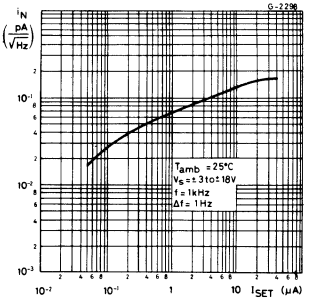


Fig. 9 - Optimum source resistance for minimum noise vs. set current.

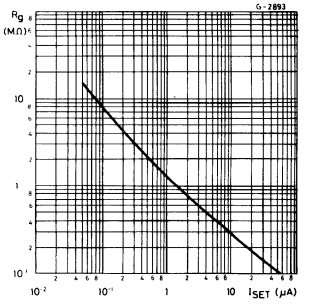


Fig. 10 - Output voltage swing vs. load resistance

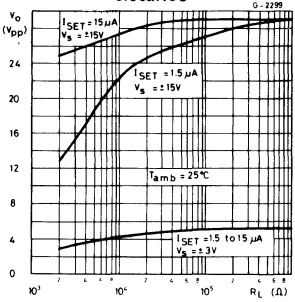


Fig. 11 - Output voltage swing vs. supply voltage

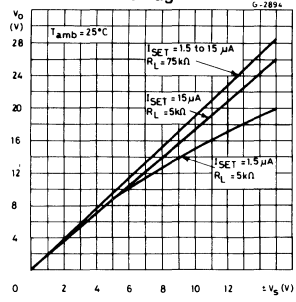


Fig. 12 - Gain bandwidth product vs. set current

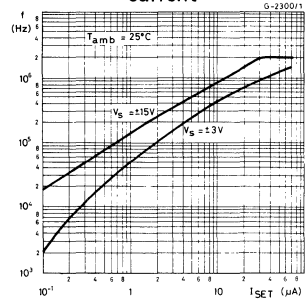


Fig. 13 - Open loop voltage gain vs. ambient temperature

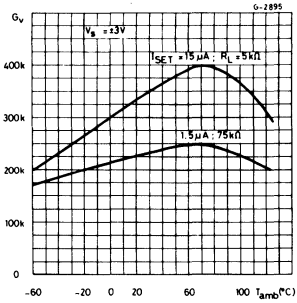


Fig. 14 - Open loop voltage gain vs. ambient temperature

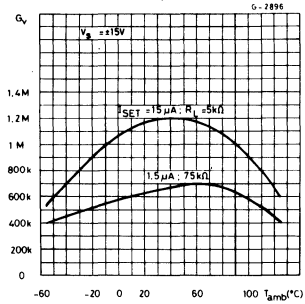


Fig. 15 - Open loop voltage gain vs. set current

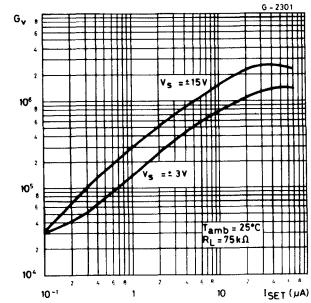


Fig. 16 - Common mode rejection vs. set current

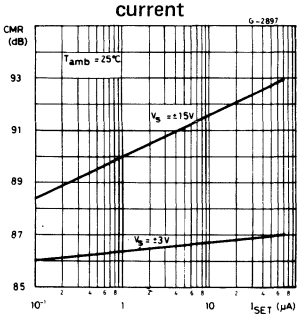


Fig. 17 - Supply voltage rejection vs. set current

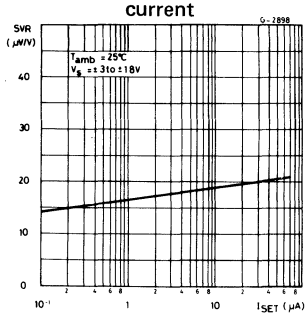


Fig. 18 - Supply current vs. ambient temperature

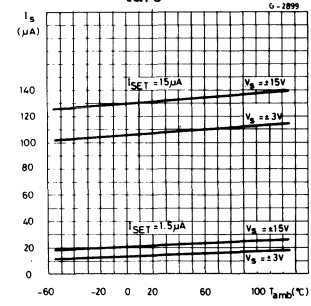


Fig. 19 - Standby supply current vs. set current

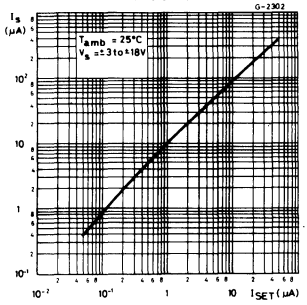


Fig. 20 - Slew rate vs. set current

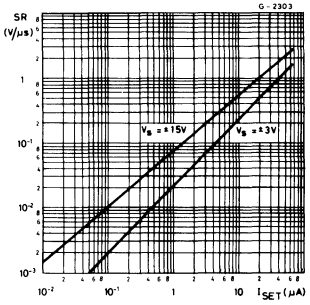
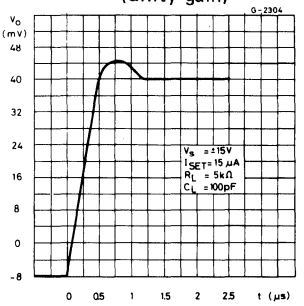


Fig. 21 - Voltage follower transient response (unity gain)



TYPICAL APPLICATIONS

Fig. 22 - High accuracy sample and hold

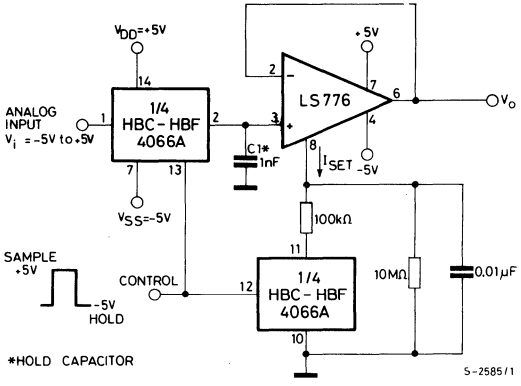


Fig. 23 - Nanowatt amplifier

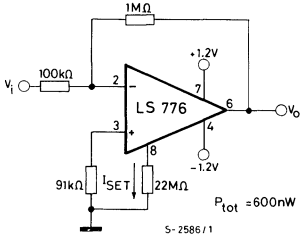
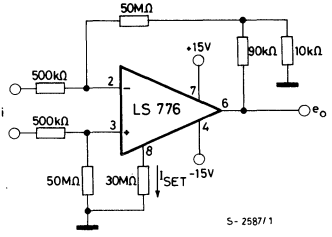


Fig. 24 - High input impedance amplifier



TYPICAL APPLICATIONS (continued)

Fig. 25 - Multiplexing and signal conditioning

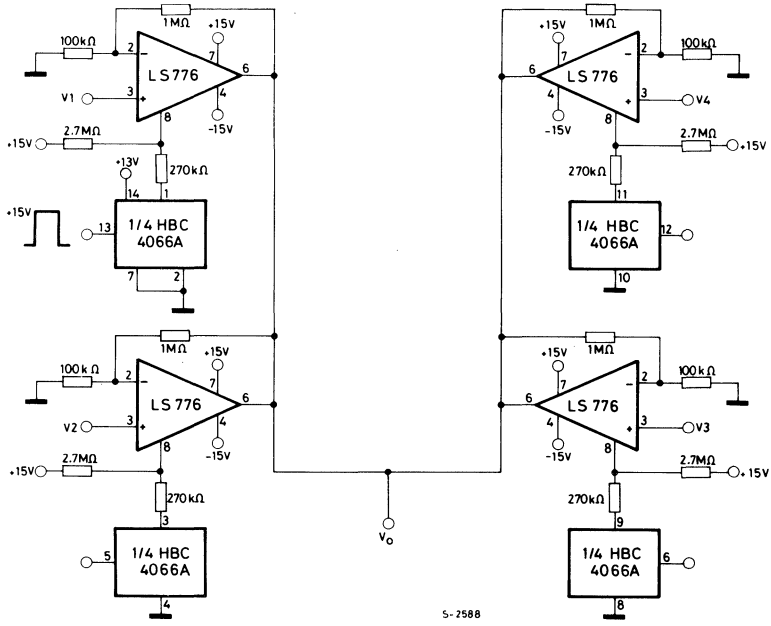


Fig. 26 - Multiple feedback bandpass filter

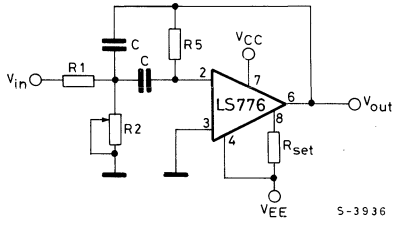
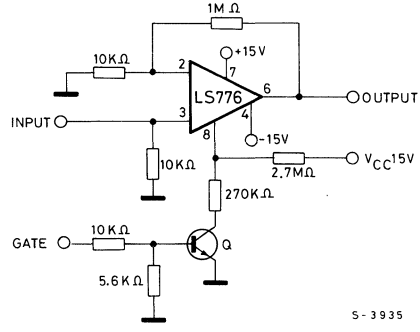


Fig. 27 - Gated amplifier



LINEAR INTEGRATED CIRCUIT

LS 4558N

PRELIMINARY DATA

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- LOW POWER CONSUMPTION
- HIGH UNITY GAIN BANDWIDTH
- NO CROSSOVER DISTORTION
- NO POP NOISE
- SHORT CIRCUIT PROTECTION
- HIGH CHANNEL SEPARATION

The LS 4558N is a high performance dual operational amplifier with frequency and phase compensation built into the chip. The internal phase compensation allows stable operation as voltage follower in spite of its high gain-bandwidth products. The circuit presents very stable electrical characteristics over the entire supply voltage range and the specially designed input stage allow the LS 4558N to be used in **low noise audio signal processing application.** The optimized class AB output stage completely eliminates crossover distortion, under any load conditions, has large source and sink capacity and is short circuit protected.

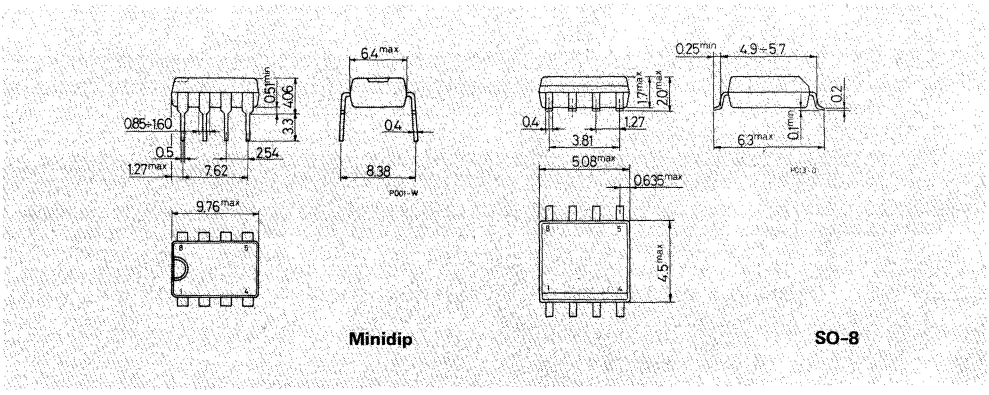
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_I	Input voltage		± V_s	
V_i	Differential input voltage		± (V_s - 1)	V
P_{tot}	Power dissipation at T_{amb} = 70°C	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_j	Junction temperature		150	°C
T_{stg}	Storage temperature		-55 to 150	°C

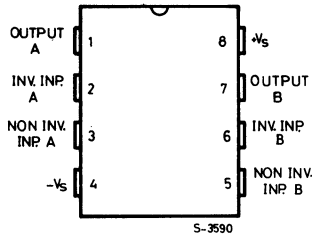
ORDERING NUMBER: LS 4558 NB (Minidip)
LS 4558 NM (Micropackage)

MECHANICAL DATA

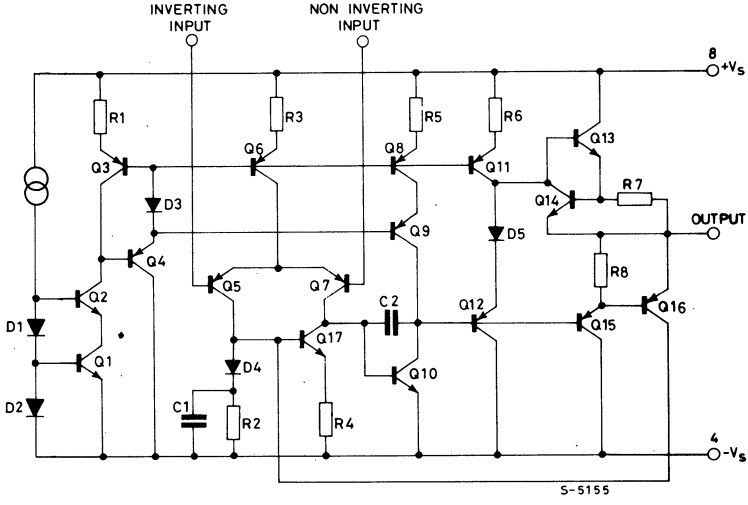
Dimensions in mm



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one section)



THERMAL DATA

		Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	120 °C/W	200* °C/W

(*) Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current (*)			1	2	mA
I_b	Input bias current			50	500	nA
		$T_{min} < T_{op} < T_{max}$			800	nA
R_i	Input resistance	f = 1 KHz	0.3	1		MΩ
V_{os}	Input offset voltage	$R_g \leq 10$ KΩ		0.5	5	mV
		$R_g \leq 10$ KΩ $T_{min} < T_{op} < T_{max}$			7.5	mV
I_{os}	Input offset current			20	200	nA
		$T_{min} < T_{op} < T_{max}$			500	nA
I_{sc}	Output short circuit current			23		mA
G_v	Large signal open loop voltage gain	$R_L = 2$ KΩ	86	100		dB
B	Gain-bandwidth product	f = 20 KHz	2	3		MHz
e_N	Total input noise voltage	f = 1 KHz $R_g = 50\Omega$ $R_g = 1$ KΩ $R_g = 10$ KΩ		8 10 18	15	$\frac{nV}{\sqrt{Hz}}$
e_N	Popcorn noise	B = 1 Hz to 1 KHz $R_g = 10$ KΩ t = 10 sec			10	μV peak
d	Distortion	$G_v = 20$ dB $R_L = 2$ KΩ $V_o = 2$ Vpp f = 1 KHz		0.03		%
V_o	Output voltage swing	$R_L = 2$ KΩ		± 13		V
V_o	Large signal voltage swing	$R_L = 10$ KΩ f = 10 KHz		28		Vpp
Transient response	Rise time	$V_i = 20$ mV $R_L = 2$ KΩ $C_L = 100$ pF		0.13		μS
	Overshoot			5		%
SR	Slew rate	unity gain $R_L = 2$ KΩ	0.8	1.5		V/μs
CMR	Common mode rejection	$V_i = 10V$ $T_{min} < T_{op} < T_{max}$	70	90		dB
SVR	Supply voltage rejection	$V_i = 1V$ f = 100 Hz $T_{min} < T_{op} < T_{max}$	80	100		dB
CS	Channel separation	f = 10 KHz $R_g = 1$ KΩ		105		dB

(*) Both amplifiers.

Fig. 1 - Open loop frequency and phase response

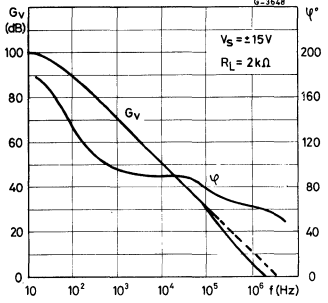


Fig. 2 - Open loop gain vs. ambient temperature

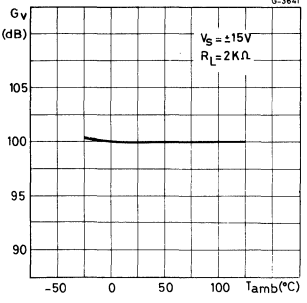


Fig. 3 - Supply voltage rejection vs. frequency

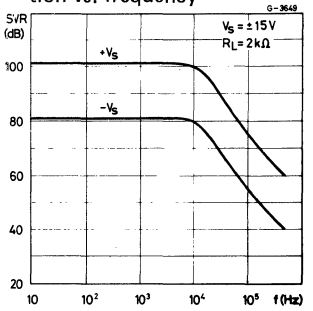


Fig. 4 - Large signal frequency response

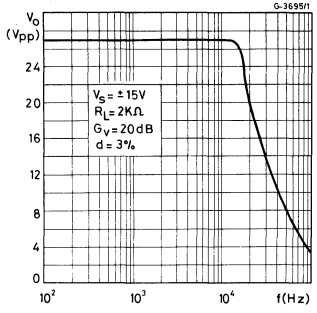


Fig. 5 - Output voltage swing vs. load resistance

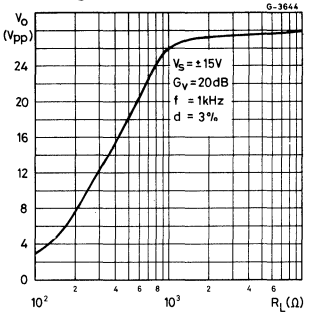


Fig. 6 - Total input noise vs. frequency

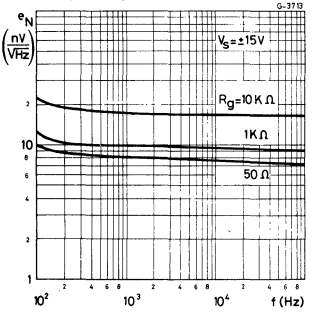


Fig. 7 - Channel separation

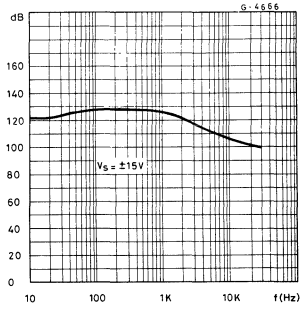


Fig. 8 - Transient response

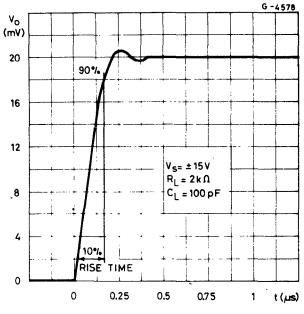
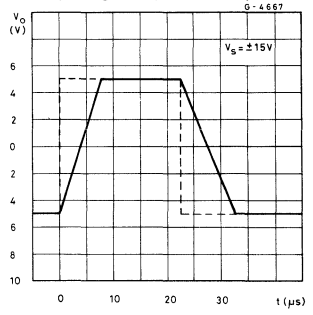
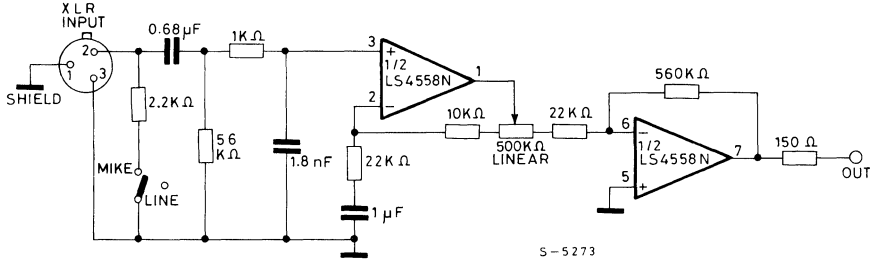


Fig. 9 - Voltage follower large-signal pulse response



APPLICATION INFORMATION

Fig. 10 - Mike/Line preamplifier for audio mixers (0 dB to 60 dB continuously variable gain)



Note — The particular characteristics of the circuit of fig. 10 is that using a linear potentiometer, the gain is continuously variable in a logarithmic mode from 0 dB to 60 dB in the audio band.

Fig. 11 - Microphones nomograph

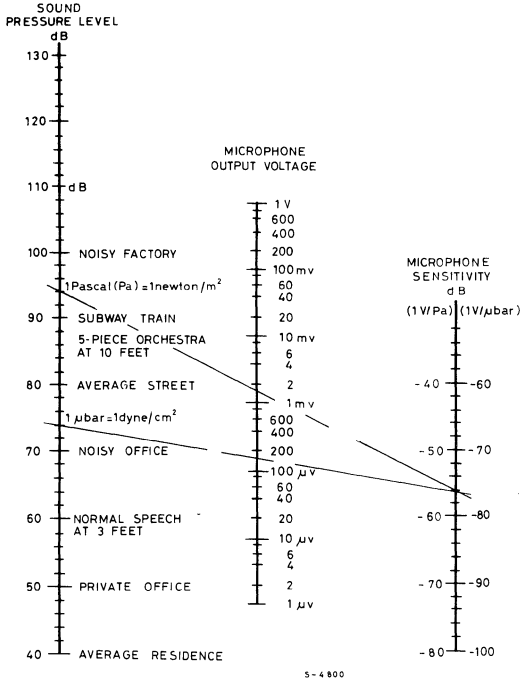


Fig. 12 - Very Low-Noise mike preamplifier (G_v= 40 dB)

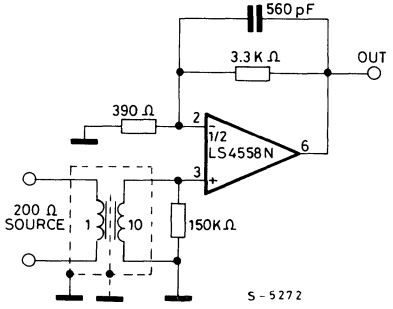
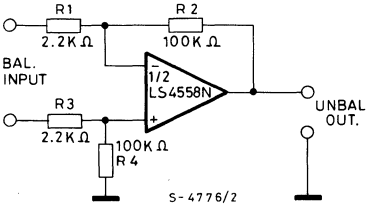


Fig. 13 - Balanced input audio preamplifier



APPLICATION INFORMATION (continued)

Fig. 14 - 20 Hz to 200 Hz variable High-pass filter (G_v = 3 dB)

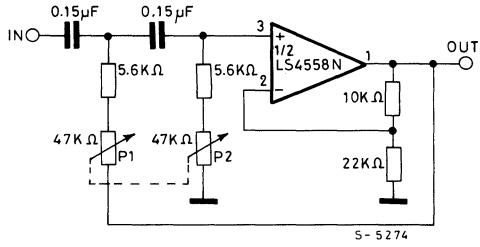


Fig. 15 - Frequency response of the High-pass filter of fig. 14

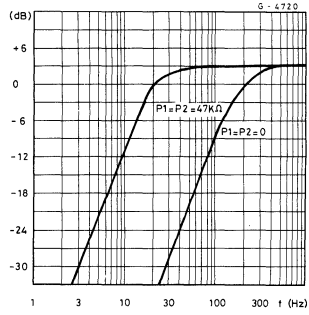


Fig. 16 - DC coupled low-pass active filter (f = 1KHz, G_v= 6 dB)

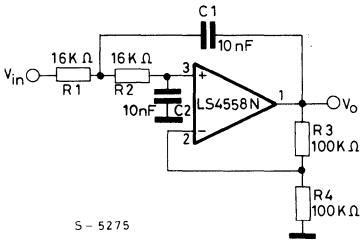


Fig. 17 - Switchable HP-LP audio filter

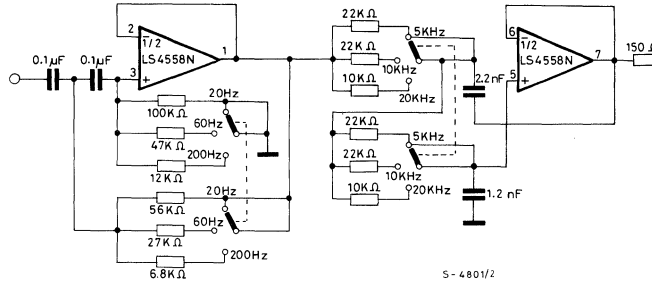
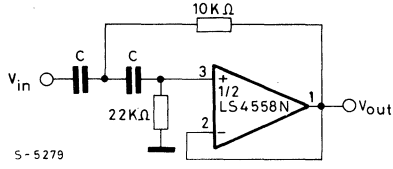
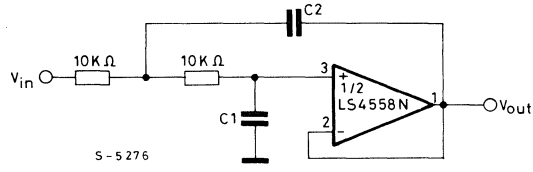


Fig. 18 - Subsonic or rumble filter (G_v= 0 dB)



f_c (Hz)	C (µF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

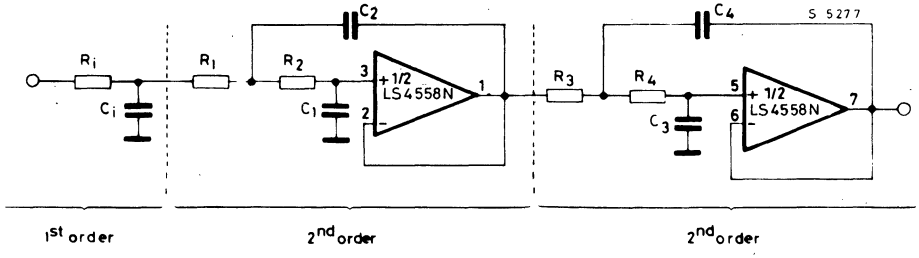
Fig. 19 - High-cut filter (G_v= 0 dB)



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 20 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33$ nF

$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97$ nF

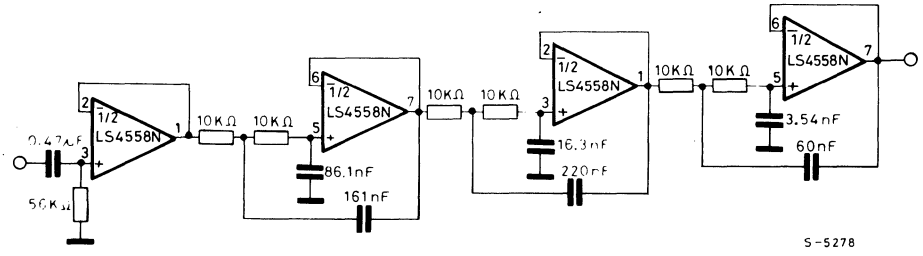
$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20$ nF

$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45$ nF

$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14$ nF

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 21 - Six-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80 dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 0.5 dB at 0.9 fc.

MC1458
MC1458C

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY COMPENSATED
- SHORT-CIRCUIT PROTECTED
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

The MC 1458 is a dual operational amplifier with frequency and phase compensation built into the chip, available in 8-lead minidip package and in 8-lead micropackage. It is intended for a wide range of applications where space and cost saving are the main goals. In spite of that, the MC 1458 offers good performance and absence of latch-up makes the device ideal for use as voltage follower, integrator, summing amplifier and general feedback applications.

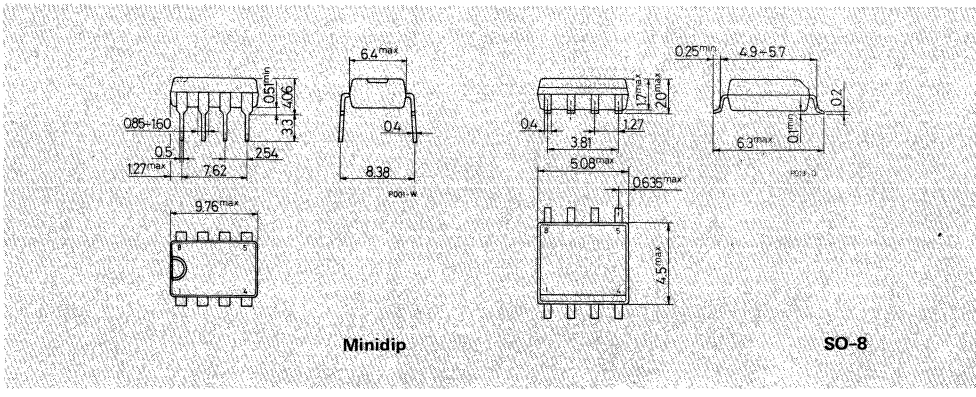
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage		± 18	V
V_i	Input voltage (*)		± 15	V
V_i	Differential input voltage		± 30	V
P_{tot}	Power dissipation at T_{amb}= 70°C	Minidip	665	mW
		Micropackage	400	mW
T_{op}	Operating temperature		0 to 70	°C
T_{stg}	Storage temperature		-55 to 150	°C

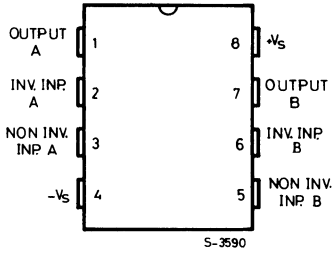
(*) For V_s lower than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

MECHANICAL DATA

Dimensions in mm

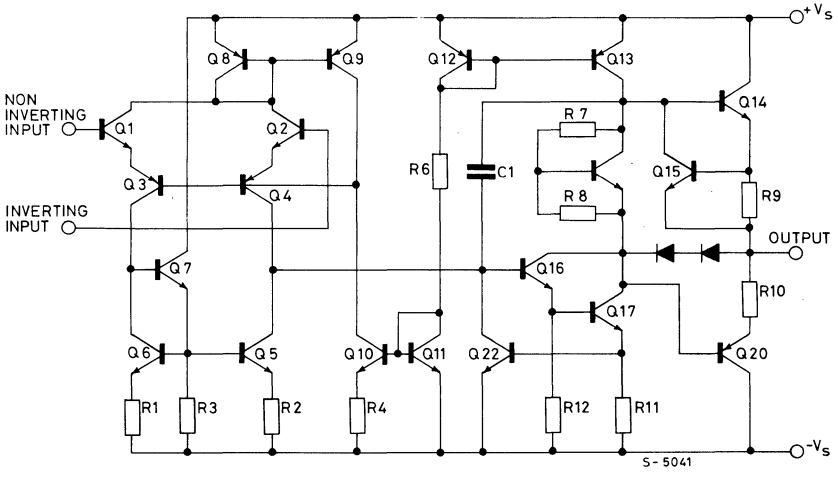


CONNECTION DIAGRAM AND ORDERING NUMBERS
(top view)



Type	Minidip	SO-8
MC 1458	MC 1458 P1	MC 1458 M
MC 1458C	MC 1458 CP1	MC 1458 CM

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			Minidip	SO-8
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120 °C/W	200* °C/W

* Measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm.).

ELECTRICAL CHARACTERISTICS (V_s= ± 15V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions		MC 1458			MC 1458C			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
I_s	Supply current (both amplifiers)					5.6			8	mA
I_b	Input bias current					0.5			0.7	µA
		$0°C < T_{op} < 70°C$				0.8			1	
V_{os}	Input offset voltage	$R_g \leq 10\ K\Omega$			2	6		2	10	mV
		$R_g \leq 10\ K\Omega$ $0°C < T_{op} < 70°C$				7.5			12	
$\frac{\Delta V_{os}}{\Delta T}$	Input offset voltage drift	$R_g = 10\ K\Omega$ $0°C < T_{op} < 70°C$			6			6		µV/°C
I_{os}	Input offset current				20	200		20	300	nA
		$0°C < T_{op} < 70°C$				300			400	
$\frac{\Delta I_{os}}{\Delta T}$	Input offset current drift	$0°C < T_{op} < 70°C$			0.5			0.5		nA/°C
I_{sc}	Output short circuit current				20			20		mA
G_v	Large signal open loop voltage gain	R_L= 2KΩ	T_{amb}= 0 to 70°C	83						dB
				86	106					
		R_L= 10KΩ	T_{amb}= 0 to 70°C				83			dB
							86	106		
B	Unity gain bandwidth				0.8			0.8		MHz
e_N	Input noise voltage	B= 10Hz to 10 KHz	R_g= 1 KΩ		3			3		µV
			R_g= 500 KΩ		25			25		
V_o	Output voltage swing	R_L= 2 KΩ		± 10	± 13		± 9	± 13		V
		R_L= 10 KΩ		± 12	± 14		± 11	± 14		
SR	Slew Rate			0.3			0.3			V/µs
CMR	Common mode rejection			70	90		60	90		dB
SVR	Supply voltage rejection			76	90			90		dB
	Common mode input voltage range			± 12	± 13		± 11	± 13		V

LINEAR INTEGRATED CIRCUIT

TBA231A

DUAL AUDIO PREAMPLIFIER

- SINGLE OR DUAL SUPPLY OPERATION
- LOW NOISE FIGURE
- HIGH GAIN
- LARGE INPUT VOLTAGE RANGE
- EXCELLENT GAIN STABILITY VERSUS SUPPLY VOLTAGE
- NO LATCH UP
- OUTPUT SHORT CIRCUIT PROTECTED

The TBA 231A is a monolithic integrated dual operational amplifier in a 14-lead dual in-line plastic package.
These low-noise, high-gain amplifiers show extremely stable operating characteristics over a wide range of supply voltage and temperatures.
The device is intended for a variety of applications requiring two high performance operational amplifiers, such as phono and tape stereo preamplifier, TV remote control receiver, etc.

ABSOLUTE MAXIMUM RATINGS

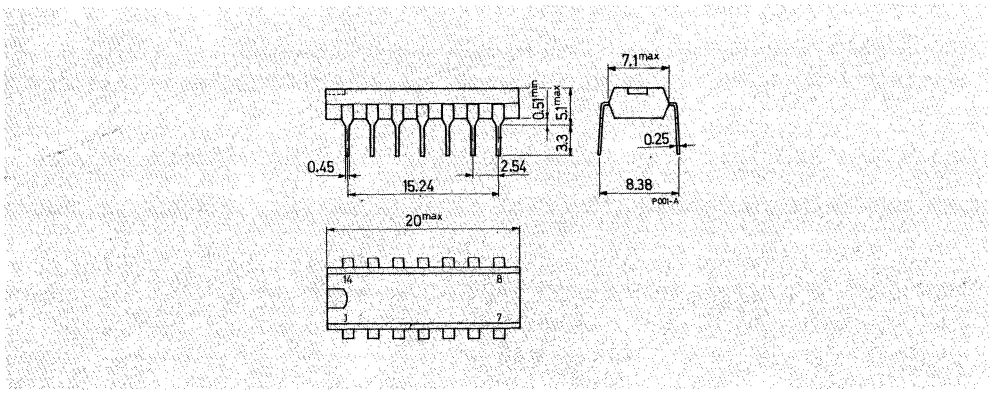
V_s	Supply voltage	± 18	V
V_i	Differential input voltage	± 5	V
V_{CM}	* Common mode input voltage	± 15	V
P_{tot}	Power dissipation at $T_{amb} \leqslant 60$ °C	500	mW
T_{stg}	Storage temperature	-40 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* For $V_s \leqslant \pm 15V$, $V_{CM\ max} = V_s$.

ORDERING NUMBER: TBA 231A

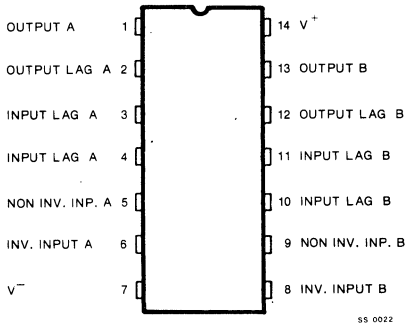
MECHANICAL DATA

Dimensions in mm

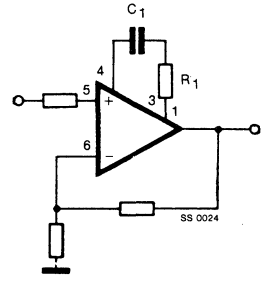


TBA231A

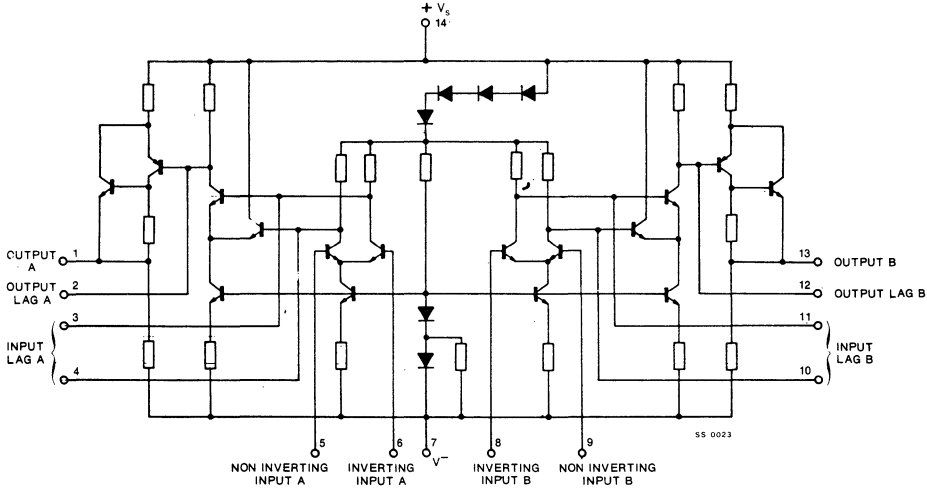
CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	180	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, R_L = 50 kΩ to pin 7, unless otherwise specified, V_s = ± 15V)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_d	Quiescent drain current	V_o = 0		9	14	mA
V_{os}	Input offset voltage	R_g = 200Ω		1	6	mV
I_{os}	Input offset current			50	1000	nA
I_b	Input bias current			250	2000	nA
V_{CM}	Common mode input voltage range		± 10	± 11		V
R_i	Input resistance	f = 1 kHz	37	150		kΩ
G_v	Voltage gain	V_o = ± 5V	6500	20 000		—
V_o	Positive output voltage swing		+12	+13		V
V_o	Negative output voltage swing		-14	-15		V
R_o	Output resistance	f = 1 kHz		5		kΩ
CMR	Common mode rejection	R_g = 200Ω	70	90		dB
SVR	Supply voltage rejection	R_g = 200Ω		50		μV/V
SR	Slew rate	Unity gain C_1 = 0.1 μF R_1 = 4.7Ω		1		V/μs
CS	Channel separation	R_g = 10 kΩ f = 10 kHz		140		dB
NF	Noise figure	R_g = 10 kΩ B = 10 Hz to 10 kHz		1.5		dB

Fig. 1 - Output voltage swing vs. supply voltage

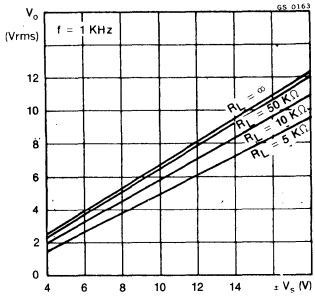


Fig. 2 - Quiescent drain current vs. supply voltage

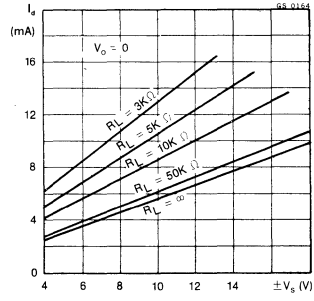


Fig. 3 - Open loop voltage gain vs. supply voltage

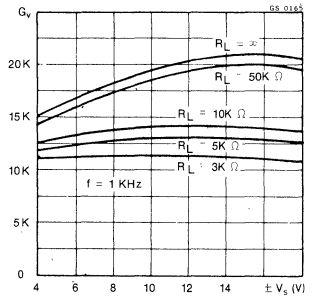


Fig. 4 - Open loop frequency response using recommeded compensation networks

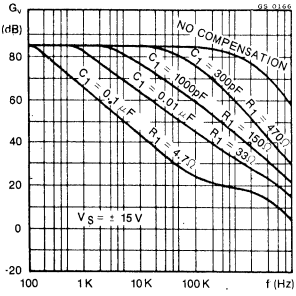


Fig. 5 - Output voltage swing vs. frequency for various compensation networks

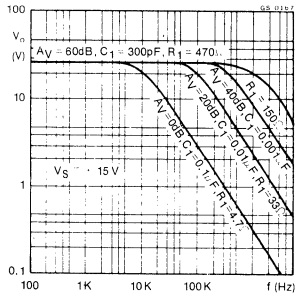


Fig. 6 - Input noise voltage vs. frequency

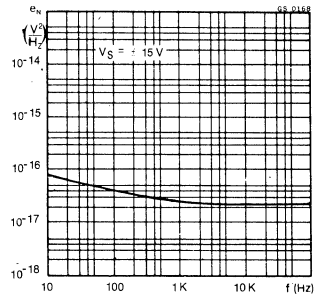


Fig. 7 - Input noise current vs. frequency

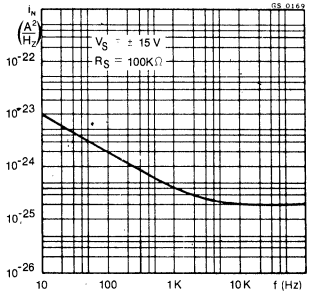


Fig. 8 - Closed loop gain vs. frequency

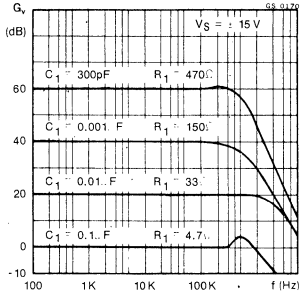
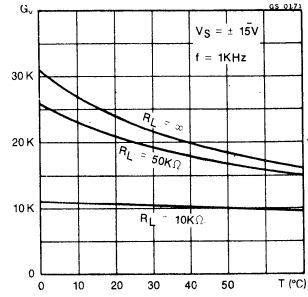
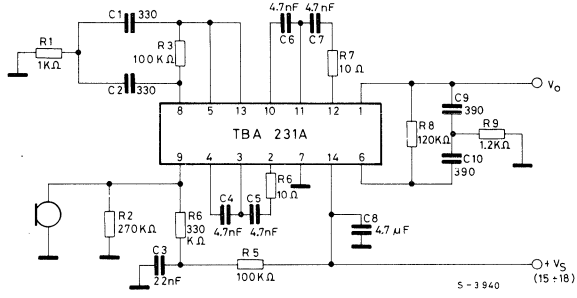


Fig. 9 - Open loop voltage gain vs. temperature



APPLICATION INFORMATION

Fig. 10 - TV remote control receiver



LINEAR INTEGRATED CIRCUIT

TBA 331

GENERAL PURPOSE TRANSISTOR ARRAY

The TBA 331 is an array of 5 monolithic NPN transistors in a 14-lead dual in-line plastic package. Two transistors are internally connected to form a differential amplifier.
The transistors of the TBA 331 are well suited to low noise general purpose and to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete components in conventional circuits; in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

ABSOLUTE MAXIMUM RATINGS

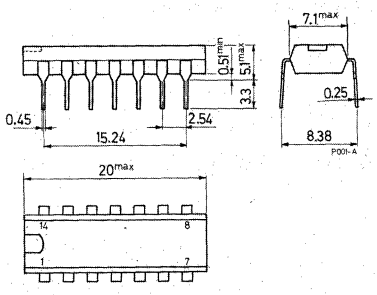
		Each transistor	Total package	
V_{CBO}	Collector-base voltage ($I_E = 0$)	20	–	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	15	–	V
V_{CSS} *	Collector-substrate voltage	20	–	V
V_{EBO}	Emitter-base voltage ($I_C = 0$)	5	–	V
I_C	Collector current	50	–	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 55°C$	300	750	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150		°C
T_{op}	Operating temperature	0 to 85		°C

* The collector of each transistor of the TBA 331 is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

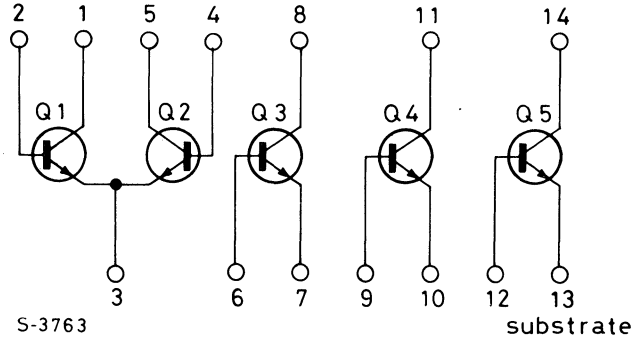
ORDERING NUMBER: TBA 331

MECHANICAL DATA

Dimensions in mm



SCHEMATIC DIAGRAM



THERMAL DATA

			each	Total
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	315° C/W	126° C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB} = 10 V		0.002	40	nA	1
I_{CEO}	Collector cutoff current (I_B = 0)	V_{CE} = 10 V		see curve	0.5	μA	2
$\lvert I_{B1}-I_{B2}\rvert$	Input offset current	I_C = 1 mA V_{CE} = 3 V		0.3	2	μA	7

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
V_{CBO}	Collector-base voltage (I_E = 0)	I_C = 10 μA	20	60		V	–
V_{CEO}	Collector-emitter voltage (I_B = 0)	I_C = 1 mA	15	24		V	–
V_{CSS}	collector-substrate voltage (I_{CSS} = 0)	I_C = 10 μA	20	60		V	–
$V_{CE\ (sat)}$	Collector-emitter saturation voltage	I_B = 1 mA I_C = 10 mA		0.23		V	–
V_{EBO}	Emitter-base voltage (I_C = 0)	I_E = 10 μA	5	7		V	–
V_{BE}	Base-emitter voltage	I_E = 1 mA V_{CE} = 3 V I_E = 10 mA V_{CE} = 3 V		0.715 0.8		V V	4 4
$\lvert V_{BE1}-V_{BE2}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV	4-6
$\lvert V_{BE3}-V_{BE4}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV	4-6
$\lvert V_{BE4}-V_{BE5}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV	4-6
$\lvert V_{BE5}-V_{BE4}\rvert$	Input offset voltage	I_C = 1 mA V_{CE} = 3 V		0.45	5	mV	4-6
$\frac{\Delta V_{BE}}{\Delta T}$	Base-emitter voltage temperature coefficient	I_C = 1 mA V_{CE} = 3 V		-1.9		mV/°C	5
$\frac{\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T}$	Input offset voltage temperature coefficient	I_C = 1 mA V_{CE} = 3 V		1.1		μV/°C	6

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.	Fig.
h_{FE}	DC current gain	I_C = 10 mA V_{CE} = 3 V		100		–	3
		I_C = 1 mA V_{CE} = 3 V	40	100		–	3
		I_C = 10 μA V_{CE} = 3 V		54		–	3
f_T	Transition frequency	I_C = 3 mA V_{CE} = 3 V	300	550		MHz	14
NF	Noise figure	I_C = 100 μA V_{CE} = 3 V f = 1 KHz R_g = 1 kΩ		3.25		dB	8
H_{ie}	Input impedance	I_C = 1 mA V_{CE} = 3 V f = 1 kHz		3.5		kΩ	9
h_{fe}	Forward current transfer ratio	I_C = 1 mA V_{CE} = 3 V f = 1 kHz		110		–	9
h_{re}	Reverse voltage transfer ratio	I_C = 1 mA V_{CE} = 3 V f = 1 kHz		1.8×10^{-4}		–	9
h_{oe}	Output admittance	I_C = 1 mA V_{CE} = 3V f = 1 kHz		15.6		μS	9
y_{ie}	Input admittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		0.3+j0.04		mS	11
y_{fe}	Forward transadmittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		31-j1.5		mS	10
y_{re}	Reverse transadmittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		see curve		mS	13

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit.	Fig.
Y_{ce}	Output admittance	I_C = 1 mA V_{CE} = 3 V f = 1 MHz		0.001+j0.03		mS	12
C_{EBO}	Emitter-base capacitance	I_C = 0 V_{EB} = 3 V		0.6		pF	—
C_{CBo}	Collector-base capacitance	I_E = 0 V_{CB} = 3 V		0.58		pF	—
C_{CSS}	Collector-sustrate capacitance	I_C = 0 V_{CSS} = 3 V		2.8		pF	—

Fig. 1 - Collector cutoff current vs ambient temperature

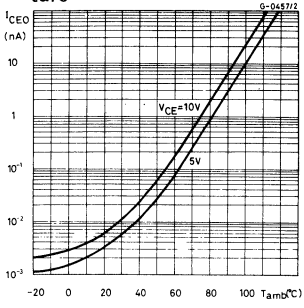


Fig. 2 - DC current gain vs. emitter current.

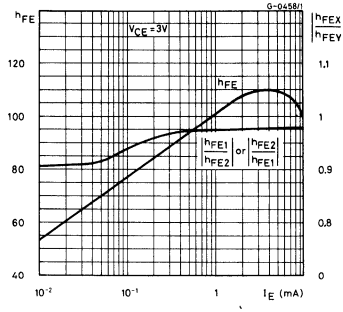


Fig. 3 - Input voltage and input offset voltage vs. emitter current

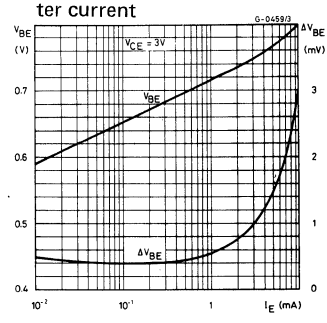


Fig. 4 - Input characteristic for each transistor

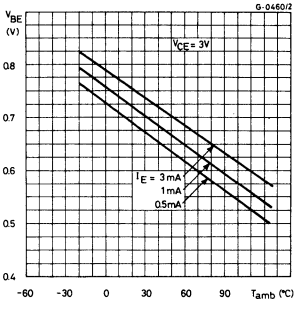


Fig. 5 - Input offset voltage vs. ambient temperature

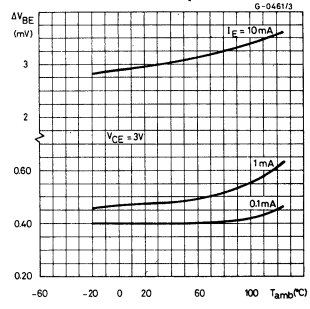


Fig. 6 - Input offset current for matched transistor pair

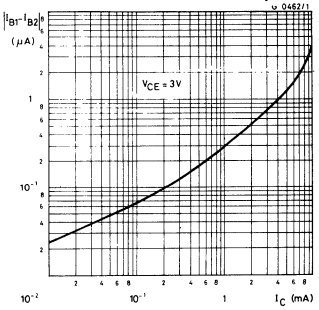


Fig. 7 - Noise figure vs collector current

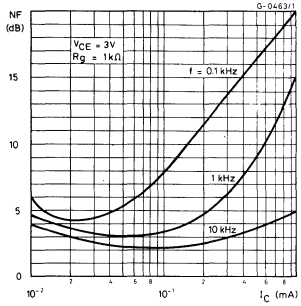


Fig. 8 - Forward admittance

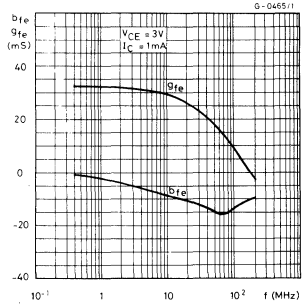


Fig. 9 - Input admittance

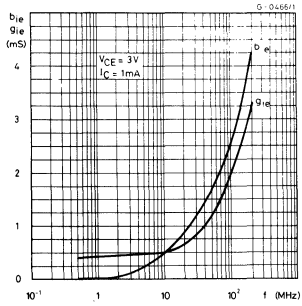


Fig. 10 - Output admittance

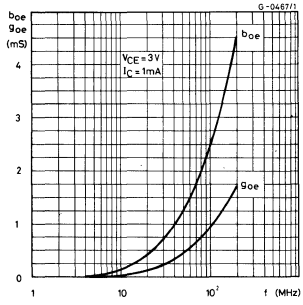


Fig. 11 - Reverse admittance

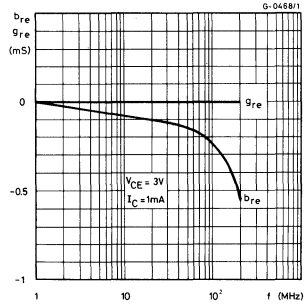
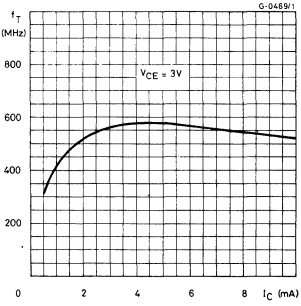


Fig. 12 - Transition frequency



LINEAR INTEGRATED CIRCUIT

TBA800

5W AUDIO AMPLIFIER

The TBA 800 is a monolithic integrated power amplifier in a 12-lead quad in-line plastic package. The external cooling tabs enable 2.5W output power to be achieved without external heatsink and 5W output power using a small area of the P.C. board copper as a heatsink.
It is intended for use as a low frequency Class B amplifier.

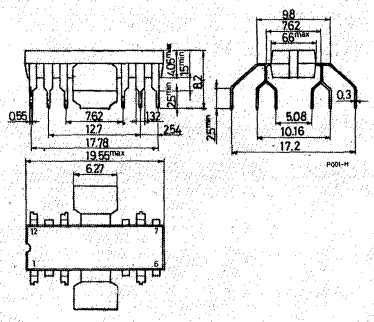
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Peak output current (non repetitive)	2	A
I_o	Peak output current (repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb}= 80°C	1	W
	at T_{tab} = 90°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

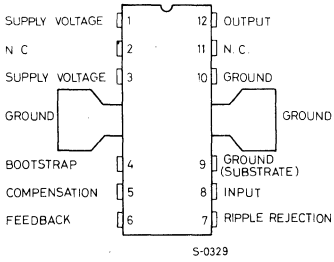
ORDERING NUMBER: TBA 800

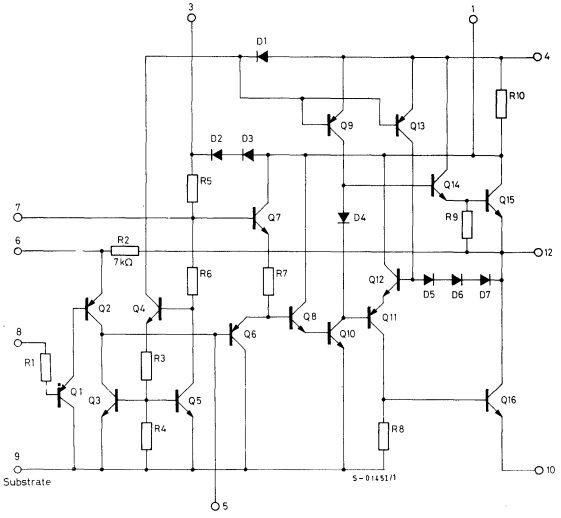
MECHANICAL DATA

Dimensions in mm

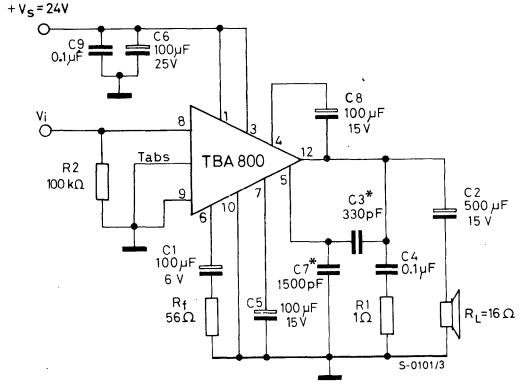


CONNECTION AND SCHEMATIC DIAGRAMS
(top view)





TEST CIRCUIT



* C3, C7 see fig. 5.

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}=25°C$, $V_s=24V$, $R_L=16\Omega$, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Quiescent output voltage (pin 12)		11	12	13	V
I_d	Quiescent drain current			9	20	mA
I_b	Input bias current (pin 8)			1	5	μA
P_o	Output power	d = 10% f = 1 kHz	4.4	5		W
$V_{i(rms)}$	Input saturation voltage		220			mV
V_i*	Input sensitivity	P_o = 5W f = 1 kHz		80		mV
R_i	Input resistance (pin 8)	f = 1 KHz		5		MΩ
B	Frequency response (-3 dB)	C3 = 330 pF	40 to 20,000			Hz
d	Distortion	P_o = 50 mW to 2.5W f = 1 kHz		0.5		%
G_v	Voltage gain (open loop)	f = 1 kHz		80		dB
G_v	Voltage gain (closed loop)	f = 1 kHz	39	42	45	dB
e_N	Input noise voltage	B = 22 Hz to 22 KHz		5		μV
i_N	Input noise current			0.2		nA
η	Efficiency	P_o = 5W f = 1 kHz		75		%
SVR	Supply voltage rejection	f_{ripple} = 100 Hz C5 = 25 μF C5 = 100 μF		35 38		dB dB
I_d	Drain current	P_o = 5W		280		mA

* See fig. 6.

Fig. 1 - Output power vs. supply voltage

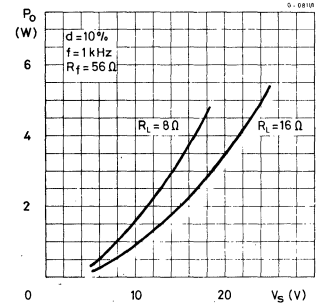


Fig. 2 - Maximum power dissipation vs. supply voltage

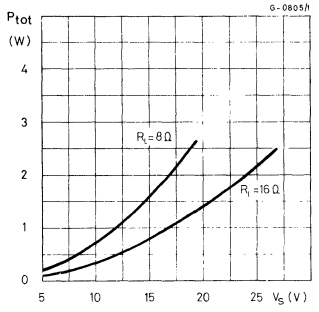


Fig. 3 - Distortion vs. output power

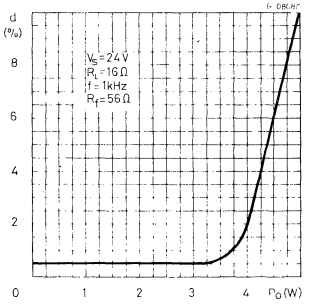


Fig. 4 - Distortion vs. frequency

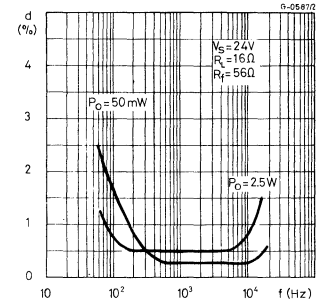


Fig. 5 - Value of C3 vs. R_f for various values of B

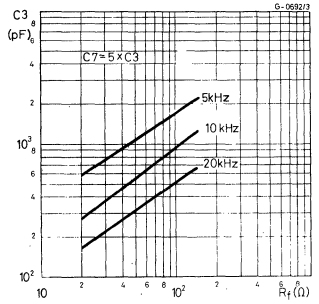


Fig. 6 - Voltage gain (closed loop) and input voltage vs. R_f

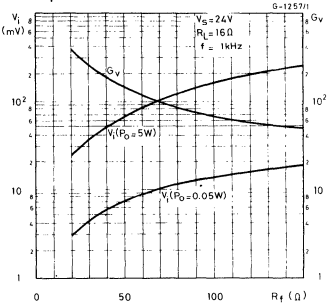


Fig. 7 - Power dissipation and efficiency vs. output power

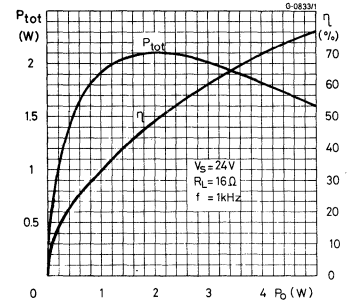


Fig. 8 - Quiescent output voltage (pin 12) vs. supply voltage

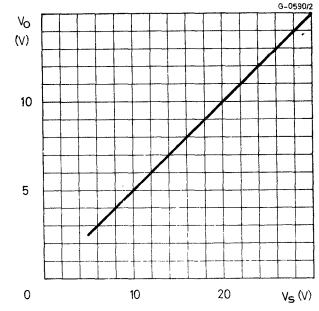
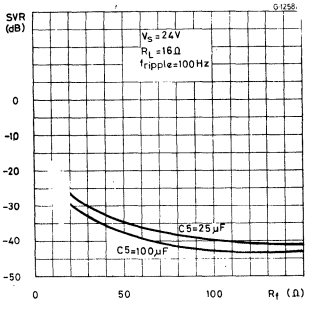
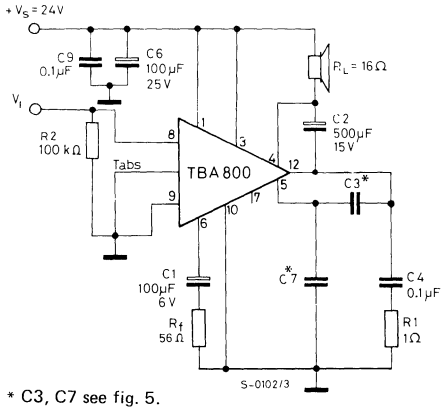


Fig. 9 - Supply voltage rejection vs. R_f.



APPLICATION INFORMATION

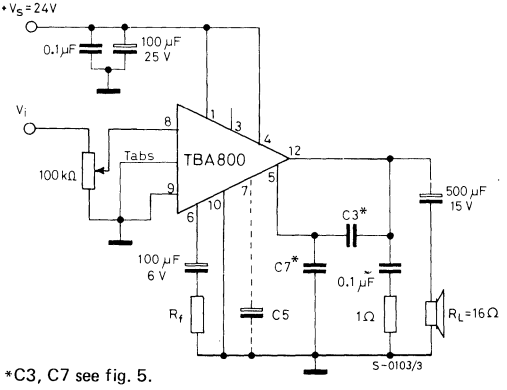
Fig. 10 - Circuit with the load connected to the supply voltage



* C3, C7 see fig. 5.

Compared with the other circuits, this configuration entails a lower number of external components and can be used at low supply voltages.

Fig. 11 - Circuit with load connected to ground without bootstrap.



*C3, C7 see fig. 5.

This circuit is only for use at high voltages. The pin 3 is left open circuit, this automatically inserts diodes D2-D3 (see schematic diagram) and this enables a symmetrical wave to be obtained at the output.

TBA810CB

LINEAR INTEGRATED CIRCUIT

FULLY-PROTECTED 7W AUDIO AMPLIFIER FOR CB RADIO

- HIGH OUTPUT POWER (7W AT 16V/4Ω ; 14.4V/2Ω)
- HIGH OUTPUT CURRENT (3A REPETITIVE)
- LOAD DUMP PROTECTION UP TO 40V
- LOAD SHORT CIRCUIT PROTECTION UP TO V_s = 15V
- POLARITY INVERSION PROTECTION
- THERMAL PROTECTION

The TBA 810CB is a monolithic integrated circuit in a 12-lead quad in-line plastic package, expressly designed for use as a power audio amplifier in CB radios.
The TBA 810 ACB has the same electrical characteristics as the TBA 810CB but its cooling tabs are flat and pierced so that an external heatsink can be easily attached.

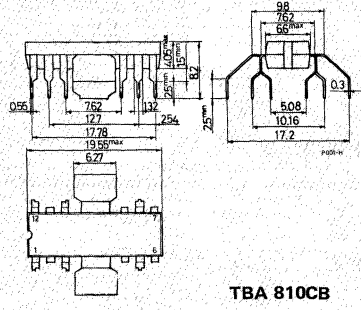
ABSOLUTE MAXIMUM RATINGS

$V_{s(peak)}$	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	20	V
I_o	Output peak current (non repetitive)	4	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation at $T_{amb} \leqslant$ 80°C (for **TBA 810CB**)	1	W
	$T_{tab} \leqslant$ 100°C (for **TBA 810ACB**)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

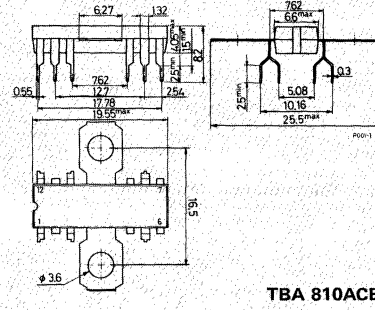
ORDERING NUMBER: TBA 810CB
TBA 810ACB

MECHANICAL DATA

Dimensions in mm



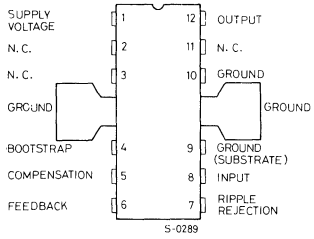
TBA 810CB

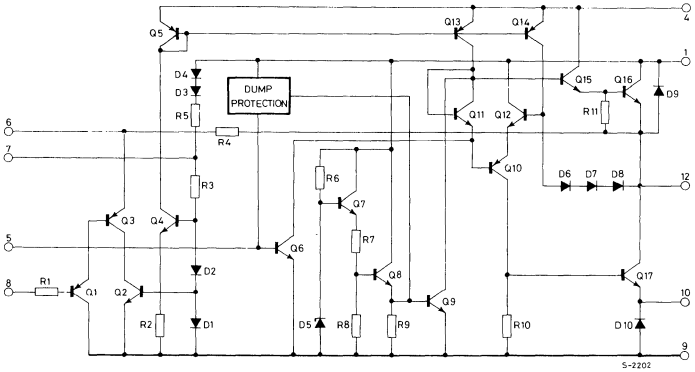


TBA 810ACB

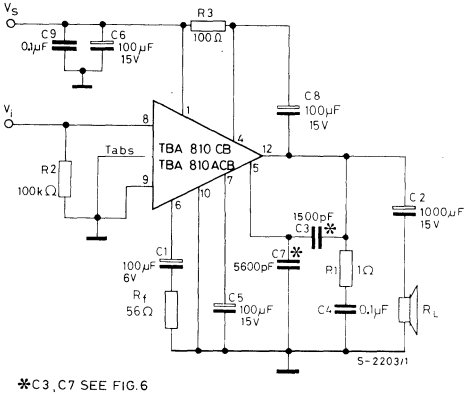
CONNECTION AND SCHEMATIC DIAGRAMS

(top view)





TEST AND APPLICATION CIRCUIT



*C3, C7 SEE FIG.6

THERMAL DATA

			TBA 810CB	TBA 810ACB
$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12 °C/W	10 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70* °C/W	80 °C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)		6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Input bias current (pin 8)			0.4		μA
P_o	Output power	d = 10% f = 1 kHz R_L = 4Ω R_L = 2Ω	 5.5 5.5	 6 7		 W W
$V_{i(rms)}$	Input saturation voltage		220			mV
V_i	Input sensitivity	f = 1 kHz P_o = 6W R_L = 4Ω R_f = 56Ω R_f = 22Ω P_o = 7W R_L = 2Ω R_f = 56Ω R_f = 22Ω		 75 30 55 20		 mV mV mV mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3 dB)	R_L = 4Ω/2Ω C_3 = 820 pF C_3 = 1500 pF		40 to 20 000 40 to 10 000		Hz Hz
d	Distortion	P_o = 50 mW to 2.5W R_L = 4Ω/2Ω f = 1 kHz		 0.3		 %
G_v	Voltage gain (open loop)	R_L = 4Ω f = 1 kHz		80		dB
G_v	Voltage gain (closed loop)	R_L = 4Ω/2Ω f = 1 kHz	34	37	40	dB
e_N	Input noise voltage	V_s = 16V B (-3 dB) = 40 to 15 000 Hz		2		μV
i_N	Input noise current			80		pA
η	Efficiency	P_o = 6W R_L = 4Ω f = 1 kHz		 75		 %
SVR	Supply voltage rejection	R_L = 4Ω V_{ripple} = 1 V_{rms} f_{ripple} = 100 Hz	40	48		dB

Fig. 1 - Output power vs. supply voltage

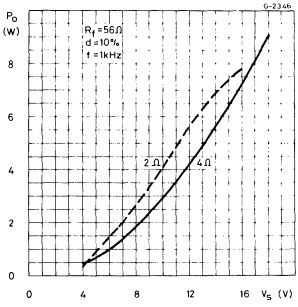


Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

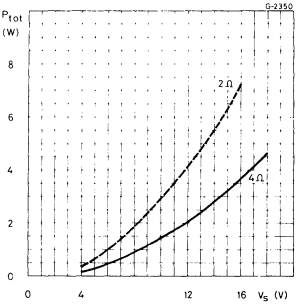


Fig. 3 - Distortion vs. frequency ($R_L = 4\Omega$)

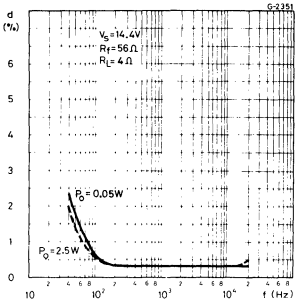


Fig. 4 - Distortion vs. frequency ($R_L = 2\Omega$)

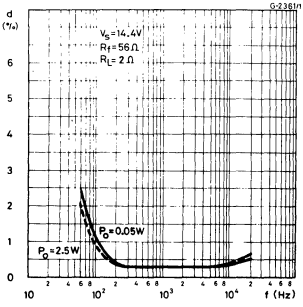


Fig. 5 - Distortion vs. output power

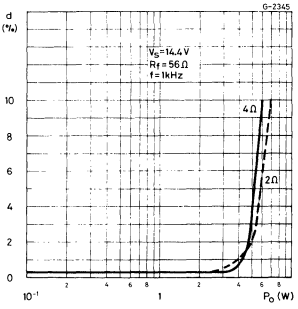


Fig. 6 - Value of C3 vs. feedback resistance for various values of B

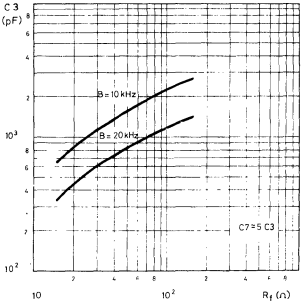


Fig. 7 - Relative voltage gain (closed loop) and input voltage vs. feedback resistance

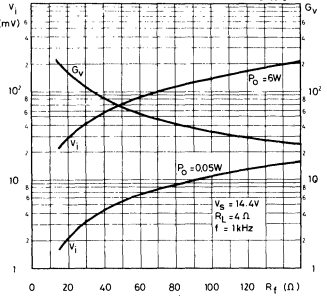


Fig. 8 - Relative voltage gain (closed loop) and input voltage vs. feedback resistance

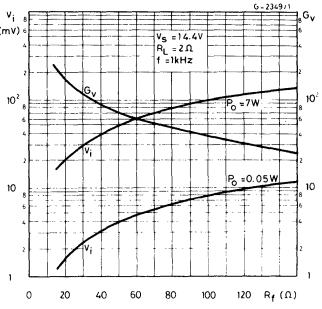


Fig. 9 - Power dissipation and efficiency vs. output power

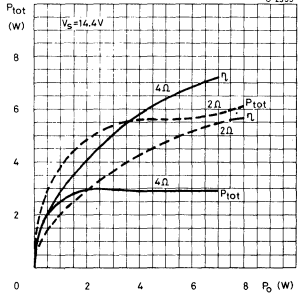


Fig. 10 - Quiescent output voltage (pin 12) vs. supply voltage

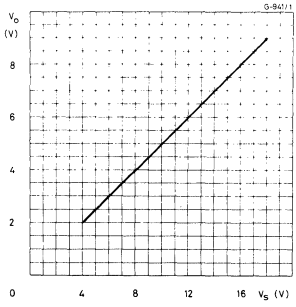


Fig. 11 - Quiescent drain current vs. supply voltage

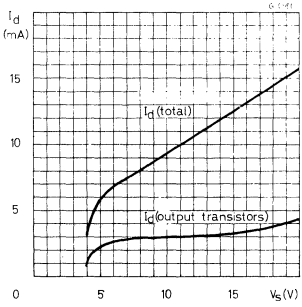
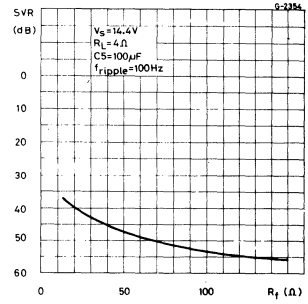


Fig. 12 - Supply voltage rejection vs. feedback resistance



BUILT-IN PROTECTION SYSTEMS

Load dump protection

The load dump case occurs in a car when the engine is running and the battery is disconnected: voltage spikes on the power line are supplied by the alternator since there is no clamping effect due to battery capacitance.

The TBA 810CB was designed to withstand a pulse train on pin 1, of the type shown in Fig. 13. Providing an LC filter is included, as shown in Fig. 14, a much higher pulse train amplitude (up to 100 V_{peak}) is allowed on the supply line with no damage to the device.

Fig. 13

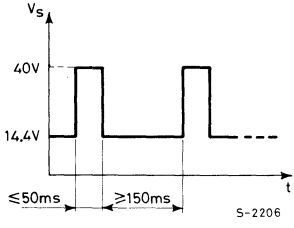
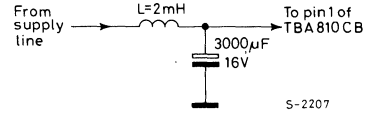


Fig. 14



Short-circuit protection

The TBA 810CB can withstand a permanent short circuit across the load for a supply voltage up to 15V.

Polarity inversion protection

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1A fuse (normally connected in series with the supply).

This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

BUILT-IN PROTECTION SYSTEMS (continued)

Open ground protection

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TBA 810CB, protection diodes are included to avoid any damage.

Inductive load protection

A protection diode is provided between pin 12 and pin 1 (see the internal schematic diagram) to allow use of the TBA 810CB with inductive loads.
In particular, the TBA 810CB can drive the coupling transformer for audio modulation in CB transmitters.

DC voltage protection

The maximum operating DC voltage on the TBA 810CB is 20V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

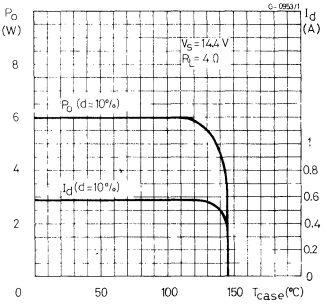
Thermal protection

A thermal limiting circuit is internally provided on TBA 810CB to prevent chip temperature exceeding 150°C. This protection offers the following advantages:

1. An overload on the output (even if permanent), or an above-limit ambient temperature can be withstood.
2. The heatsink can be designed with smaller safety margins compared with that of a conventional power audio amplifier.

The TBA 810CB will remain undamaged in the event of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) are reduced (Fig. 15).

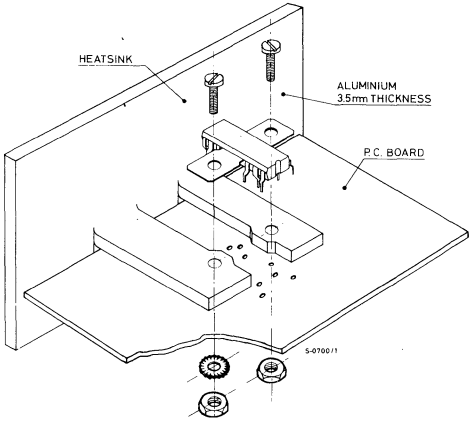
Fig. 15 - Output power and drain current vs. package temperature

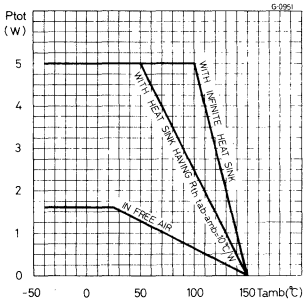


MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heatsink (Fig. 16) or by soldering them to an area of copper on the printed circuit board (Fig. 17). During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

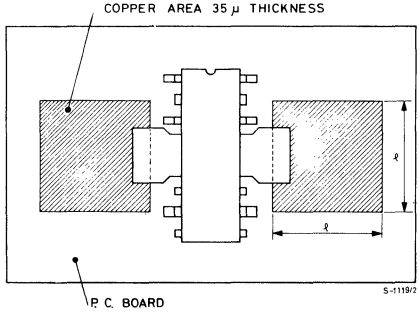
Fig. 16 - TBA 810 ACB mounting example

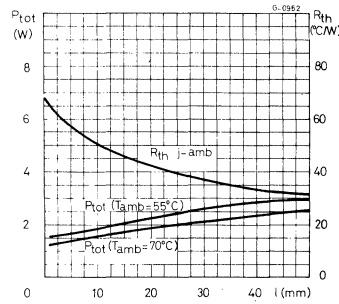




MOUNTING INSTRUCTIONS (continued)

Fig. 17 - TBA 810CB mounting example



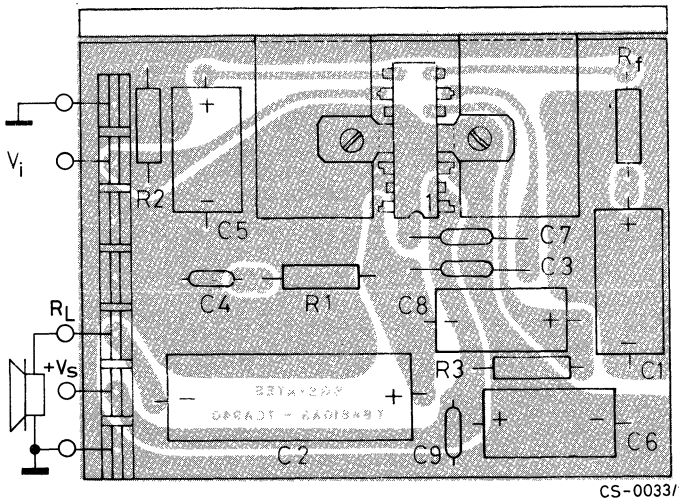


RELIABILITY

The reliability of the TBA 810CB is very high thanks to the Fin-Dip package and assembly process. A CB radio is switched ON and OFF many thousands of times during the lifetime of the car. This causes thermal fatigue of the device and if suitable package and assembly processes were not used, failure of the die or wire bonding would be probable. Thanks to the particular process adopted for the TBA 810CB, the device can easily withstand the following stresses:

- thermal fatigue: more than 10^4 cycles with $\Delta T_{case} = 100°C$
- thermal cycling: more than 10^3 cycles between -55°C and +125°C
- thermal shocks: more than 10^3 cycles between -55°C and +125°C
- relative humidity of 85% at 85°C is resisted for more than 10^3 hours.

Fig. 18 - P.C. board and component layout for the test and application circuit (1:1 scale)



LINEAR INTEGRATED CIRCUIT

TBA810P

7W AUDIO AMPLIFIER

The TBA 810P is an improvement of TBA 810S.

It offers:
- Higher output-power ($R_L = 4\Omega$ and 2Ω)
- Lower noise
- Polarity inversion protection
- Fortuitous open ground protection
- Higher supply voltage rejection (40 dB min.)

The TBA 810P is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.
The TBA 810 P provides 7-W output power at 16V/4Ω; 7-W at 14.4V/2Ω.
It gives high output current (up to 3A), high efficiency (75% at 6W output), very low harmonic and crossover distortion. The circuit is provided with a thermal limiting circuit and can withstand a short-circuit on the load for supply voltages up to 15V.
The TBA 810AP has the same electrical characteristics as the TBA 810P, but its cooling tabs are flat and pierced so that an external heatsink can easily be attached.

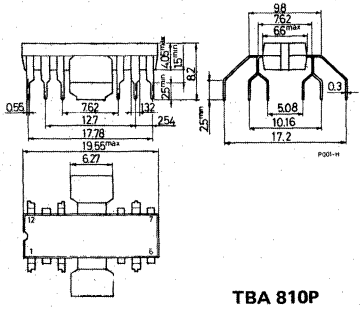
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Output peak current (non repetitive)	4	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation at $T_{amb} \leqslant$ 80°C (for **TBA 810P**)	1	W
	$T_{tab} \leqslant$ 100°C (for **TBA 810AP**)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

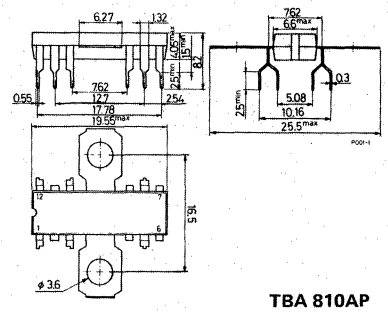
ORDERING NUMBERS: TBA 810P
TBA 810AP

MECHANICAL DATA

Dimensions in mm



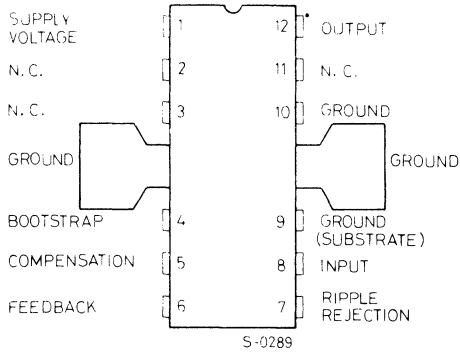
TBA 810P



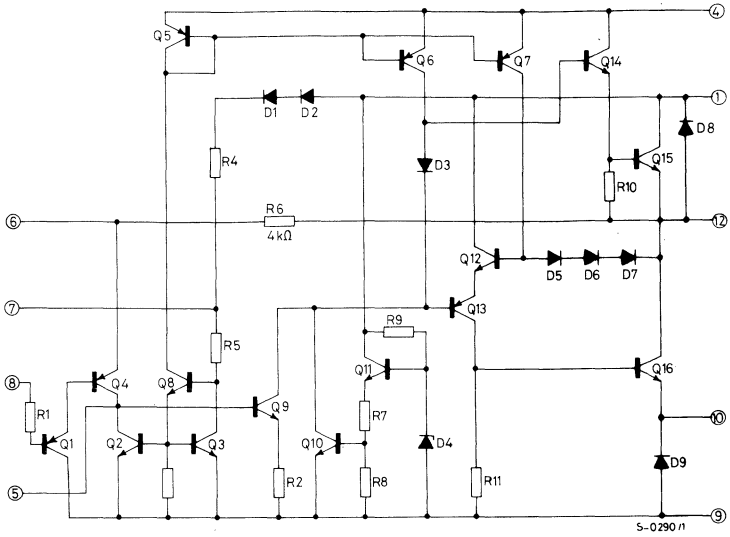
TBA 810AP

TBA810P

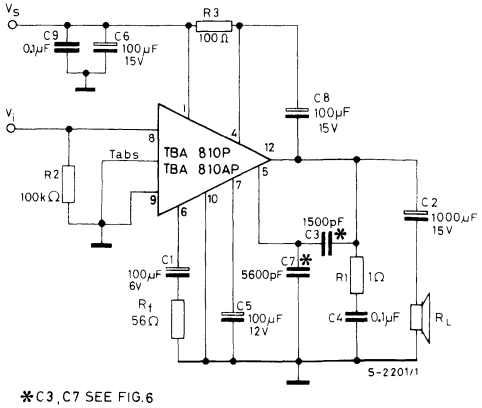
CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



TEST AND APPLICATION CIRCUIT



*C3, C7 SEE FIG.6

THERMAL DATA

			TBA 810P	TBA 810AP
$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12°C/W	10°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70**°C/W	80°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit; V_s = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)		6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Input bias current			0.4		μA
P_o	Output power	d = 10% f = 1 kHz R_L = 4Ω R_L = 2Ω	 5.5 5.5	 6 7		 W W
$V_{i(rms)}$	Input saturation voltage		220			mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_i	Input sensitivity	f = 1 kHz P_o = 6W R_L = 4Ω R_f = 56Ω R_f = 22Ω P_o = 7W R_L = 2Ω R_f = 56Ω R_f = 22Ω		 75 30 55 20		 mV mV mV mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (- 3 dB)	R_L = 4Ω/2Ω C_3 = 820 pF C_3 = 1500 pF		40 to 20 000 40 to 10 000		Hz Hz
d	Distortion	P_o = 50 mW to 2.5W R_L = 4Ω/2Ω f = 1 kHz		0.3		%
G_v	Voltage gain (open loop)	R_L = 4Ω f = 1 kHz		80		dB
G_v	Voltage gain (closed loop)	R_L = 4Ω/2Ω f = 1 kHz	34	37	40	dB
e_N	Input noise voltage	V_s = 16V B (-3 dB) = 40 to 15 000 Hz		2		μV
i_N	Input noise current			80		pA
η	Efficiency	P_o = 6W R_L = 4Ω f = 1 kHz		75		%
SVR	Supply voltage rejection	R_L = 4Ω V_{ripple} = 1V_{rms} f_{ripple} = 100 Hz	40	48		dB
I_d	Drain current	P_o = 6W R_L = 4Ω		600		mA

Fig. 1 - Output power vs. supply voltage

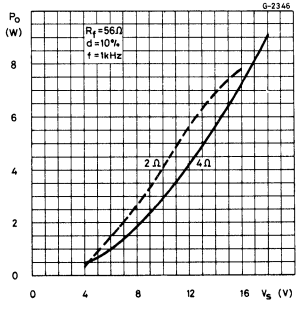


Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

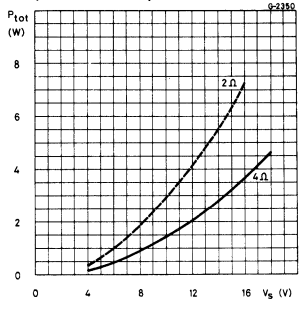


Fig. 3 - Distortion vs. frequency (R_L = 4Ω)

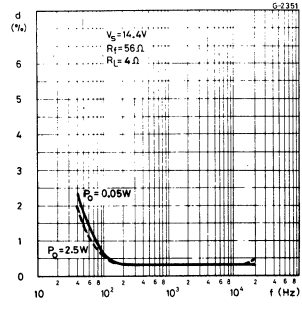


Fig. 4 - Distortion vs. frequency ($R_L = 2\Omega$)

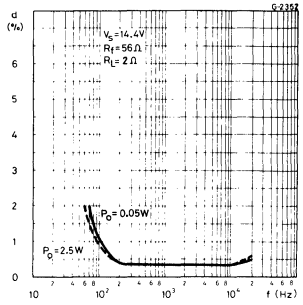


Fig. 5 - Distortion vs. output power

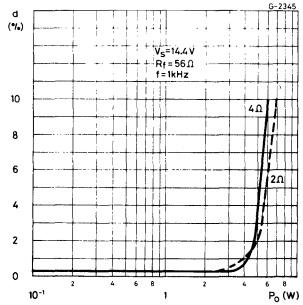


Fig. 6 - Value of C3 vs. feedback resistance for various values of B

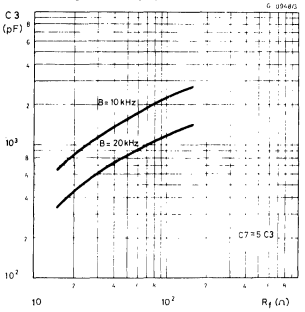


Fig. 7 - Relative voltage gain (closed loop) and input voltage vs. feedback resistance

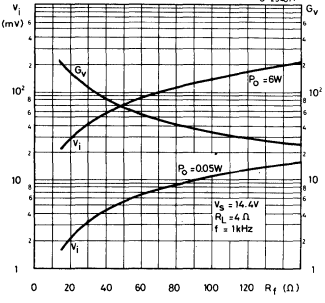


Fig. 8 - Relative voltage gain (closed loop) and input voltage vs. feedback resistance

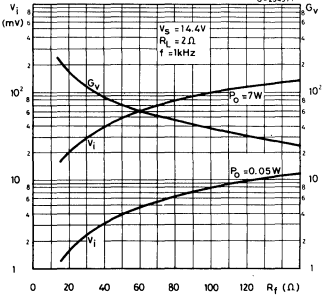


Fig. 9 - Total power dissipation and efficiency vs. output power

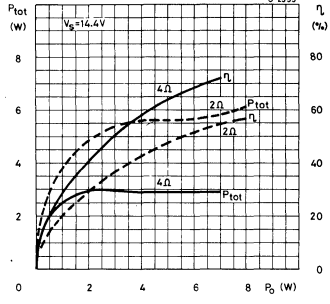


Fig. 10 - Quiescent output voltage (pin 12) vs. supply voltage

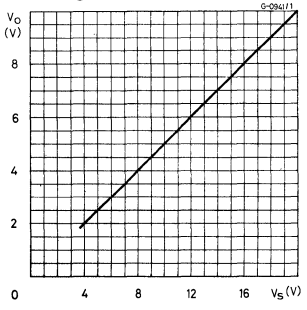


Fig. 11 - Quiescent drain current vs. supply voltage

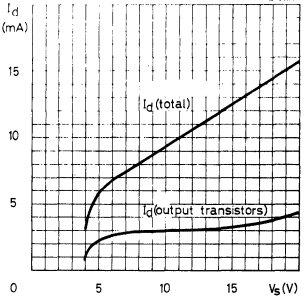
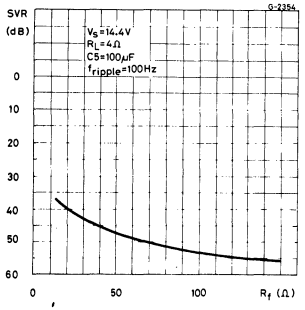


Fig. 12 - Supply voltage rejection vs. feedback resitance



MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heatsink (TBA 810 AP see figs. 13 and 14), or by soldering them to an area of copper on the printed circuit board (TBA 810P see fig. 15). During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 13 - Maximum power dissipation vs. ambient temperature (TBA810AP only)

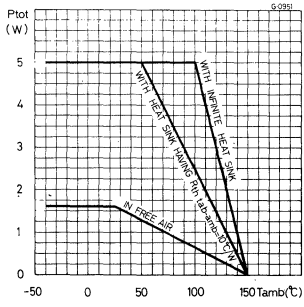


Fig. 14 - Mounting example of the TBA 810 AP

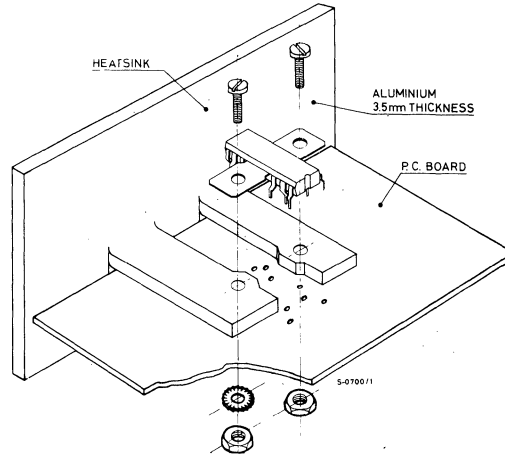
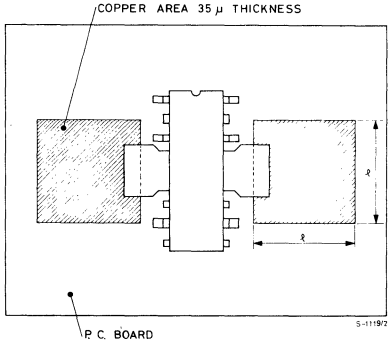
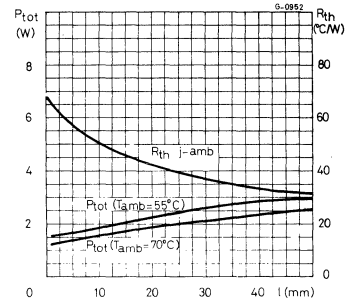


Fig. 15 - Maximum power dissipation vs. cooper area of the P.C. board (TBA 810P only)





THERMAL SHUTDOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily withstood.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the event of excessive junction temperature: all that happens is that P_o, (and therefore P_{tot}) are reduced.

Fig. 16 - Output power and drain current vs. package temperature

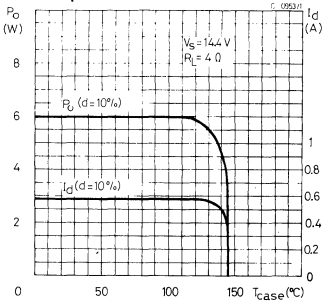
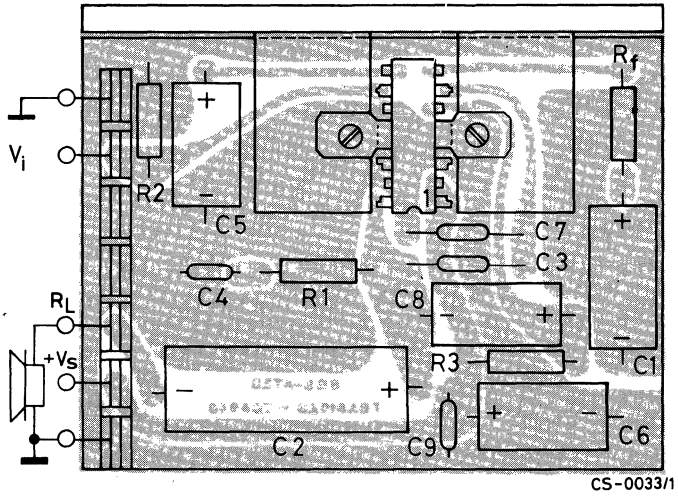


Fig. 17 - P.C. board and component layout for the test and application circuit (1:1 scale)



TBA810S

LINEAR INTEGRATED CIRCUIT

7 W AUDIO AMPLIFIER

The TBA 810 S is a monolithic integrated circuit in a 12 lead quad in-line plastic package, intended for use as a low frequency class B amplifier.
The TBA 810 S provides 7 W power output at 16 V/4 Ω, 6 W at 14.4 V/4 Ω, 2.5 W at 9 V/4 Ω, 1 W at 6 V/4 Ω and works with a wide range of supply voltages (4 to 20 V); it gives high output current (up to 2.5 A), high efficiency (75% at 6 W output), very low harmonic and cross-over distortion. In addition, the circuit is provided with a thermal protection circuit.
The TBA 810 AS has the same electrical characteristics as the TBA 810S, but its cooling tabs are flat and pierced so that an external heatsink can easily be attached.

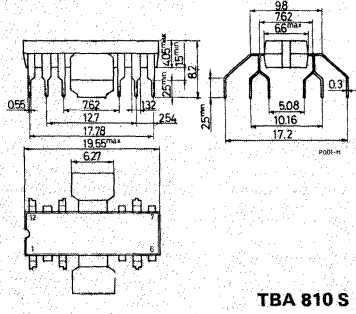
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Output peak current (non-repetitive)	3.5	A
I_o	Output current (repetitive)	2.5	A
P_{tot}	Power dissipation: at T_{amb} = 70°C	1	W
	at T_{tab} = 100°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

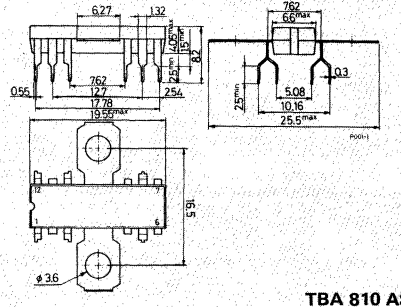
ORDERING NUMBERS: TBA 810 S
TBA 810 AS

MECHANICAL DATA

Dimensions in mm



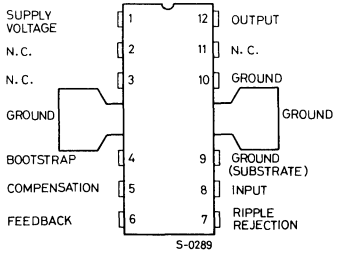
TBA 810 S

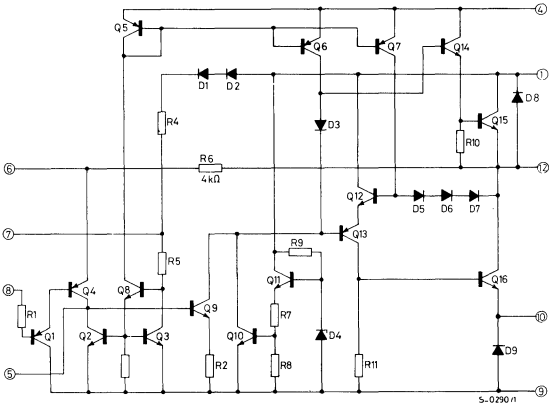


TBA 810 AS

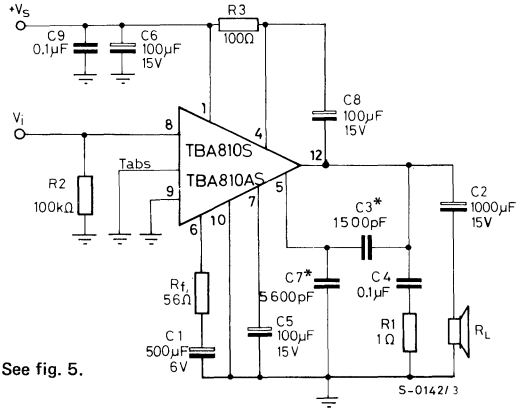
CONNECTION AND SCHEMATIC DIAGRAM

(top view)





TEST AND APPLICATION CIRCUIT



* See fig. 5.

THERMAL DATA

			TBA810S	TBA810AS
$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12 °C/W	10 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70** °C/W	80 ° C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; T_{amb} = 25 °C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		4		20	V
V_o	Quiescent output voltage (pin 12)	V_s = 14.4V	6.4	7.2	8	V
I_d	Quiescent drain current			12	20	mA
I_b	Bias current (pin 8)			0.4		μA
P_o	Power output	d = 10% R_L = 4Ω f = 1 kHz V_s = 16V V_s = 14.4V V_s = 9V V_s = 6V	 5.5	 7 6 2.5 1	 	 W W W W
$V_{i(rms)}$	Input voltage				220	mV
V_i	Input sensitivity	P_o = 6W V_s = 14.4V R_L = 4Ω f = 1kHz R_f = 56Ω R_f = 22Ω		 80 35		 mV mV
R_i	Input resistance (pin 8)			5		MΩ
B	Frequency response (-3 dB)	V_s = 14.4V R_L = 4Ω C3 = 820 pF C3 = 1500 pF		 40 to 20,000 40 to 10,000		 Hz Hz
d	Distorsion	P_o = 50mW to 3W V_s = 14.4V R_L = 4Ω f = 1kHz		 0.3		 %
G_v	Voltage gain (open loop)	V_s = 14.4V R_L = 4Ω f = 1kHz		 80		 dB
G_v	Voltage gain (closed loop)	V_s = 14.4V R_L = 4Ω f = 1kHz	 34	 37	 40	 dB
e_N	Input noise voltage	V_s = 14.4V R_g = 0 B (-3 dB) = 20Hz to 20,000 Hz		 2		 μV
i_N	Input noise current	V_s = 14.4V B (-3 dB) = 20 Hz to 20,000 Hz		 0.1		 nA
η	Efficiency	P_o = 5W V_s = 14.4V R_L = 4Ω f = 1kHz		 70		 %
SVR	Supply voltage rejection	V_s = 14.4V R_L = 4Ω f_{ripple} = 100 Hz		 38		 dB

Fig. 1 - Power output versus supply voltage

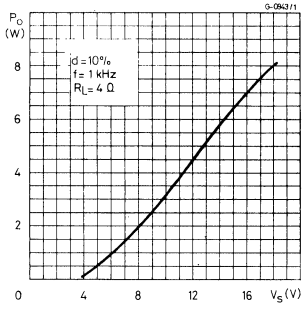


Fig. 2 - Maximum power dissipation versus supply voltage (sine wave operation)

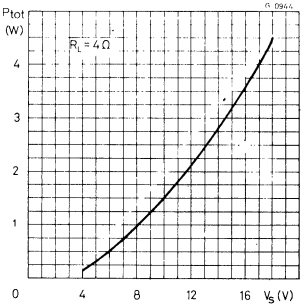


Fig. 3 - Distorsion versus output power

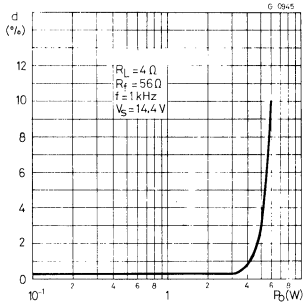


Fig. 4 - Distorsion versus frequency

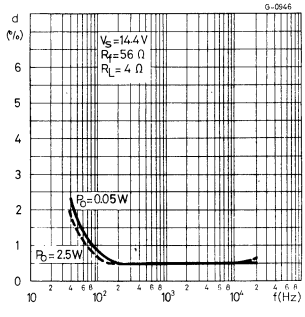


Fig. 5 - Value of C3 versus R_f for various values of B

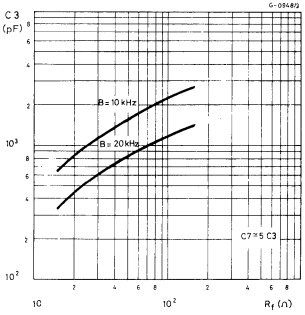


Fig. 6 - Power dissipation and efficiency versus output power

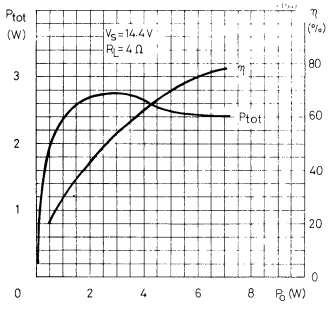


Fig. 7 - Quiescent output voltage (pin 12) versus supply voltage

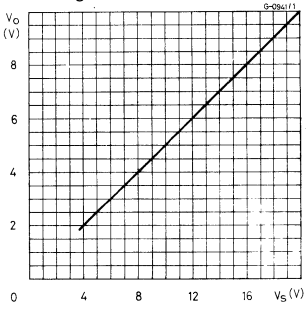


Fig. 8 - Quiescent current versus supply voltage

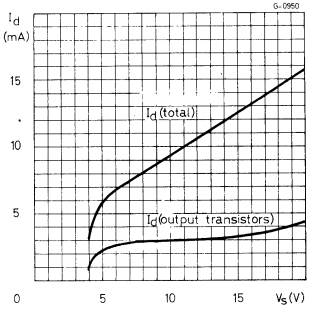
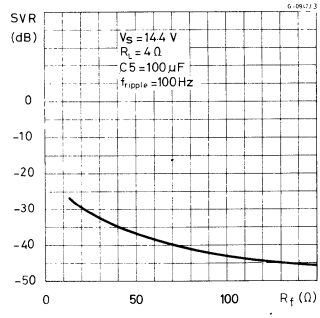
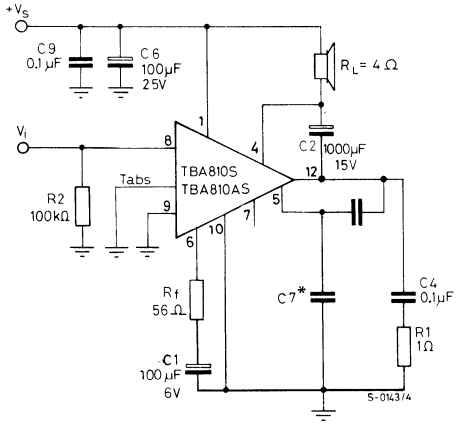


Fig. 9 - Supply voltage rejection



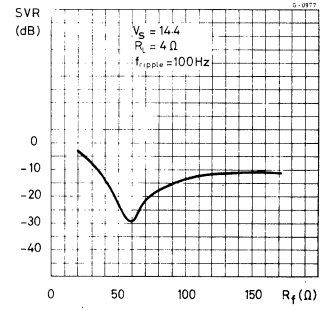
For portable equipment the circuit in Fig. 10 has the advantages of fewer external components and a better behaviour at low supply voltages (down to 4 V).

Fig. 10 - Application circuit with load connected to the supply voltage



* C3, C7 see fig. 5

Fig. 11 - Supply voltage rejection versus R_f (circuit of fig. 10)



MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heat sink (TBA 810 AS - fig. 12) or by soldering them to an area of copper on the printed circuit board (TBA 810 S - fig. 13).

Fig. 12 - Maximum power dissipation versus ambient temperature (for TBA 810 AS only)

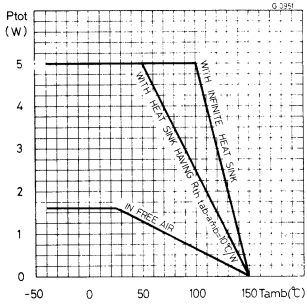
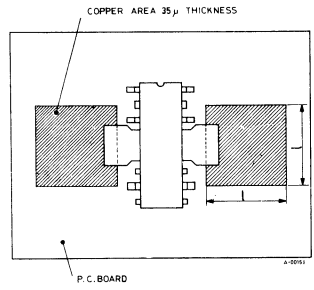
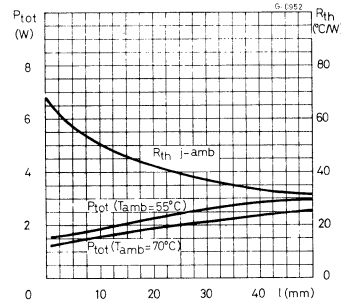


Fig. 13 - Maximum power dissipation versus copper area of the P.C. board (for TBA 810 S only)





During soldering the tabs temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.
Fig. 14a and 14b show two ways that can be used for mounting the device.

Fig. 14a shows a method of mounting the TBA 810 S, that is satisfactory both from the point of view of heat dissipation and from mechanical considerations. For TBA 810 AS the desired thermal resistance is obtained by fixing the elements shown in fig. 14b, to a suitably dimensioned plate. This plate can also act as a support for the whole printed circuit board; the mechanical stresses do not damage the integrated circuit. This is firmly fixed to the element, in fig. 14b.

Fig. 14a

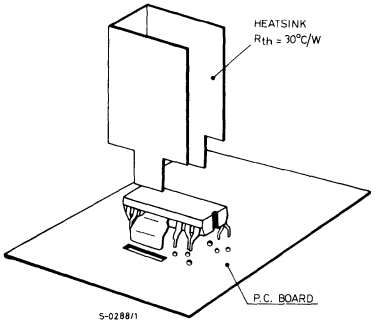
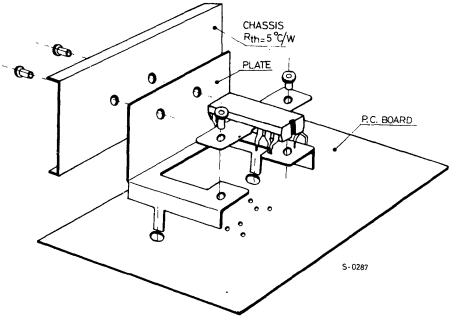


Fig. 14b

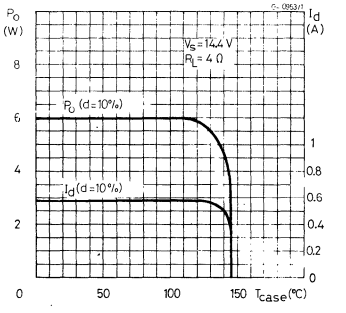


THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported.
2) The heat sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of too high a junction temperature: all that happens is that P_o (and therefor P_{tot}) and I_d are reduced (fig. 15).

Fig. 15 - Output power and drain current versus package temperature



TBA820M

LINEAR INTEGRATED CIRCUIT

MINIDIP 1.2W AUDIO AMPLIFIER

The TBA 820M is a monolithic integrated audio amplifier in a 8 lead dual in-line plastic package. It is intended for use as low frequency class B power amplifier with wide range of supply voltage: 3 to 16V, in portable radios, cassette recorders and players etc. Main features are: minimum working supply voltage of 3V, low quiescent current, low number of external components, good ripple rejection, no crossover distortion, low power dissipation.
Output power: P_o= 2W at 12V/8Ω, 1.6W at 9V/4Ω and 1.2W at 9V/8Ω.

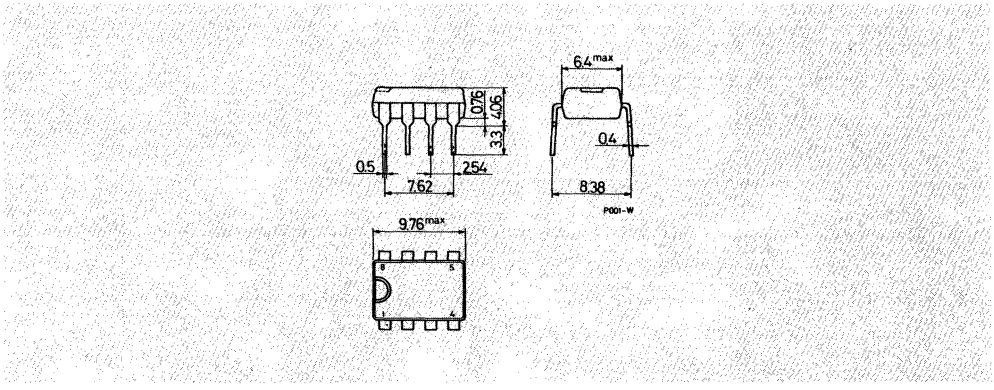
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output peak current	1.5	A
P_{tot}	Power dissipation at T_{amb}= 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TBA 820M

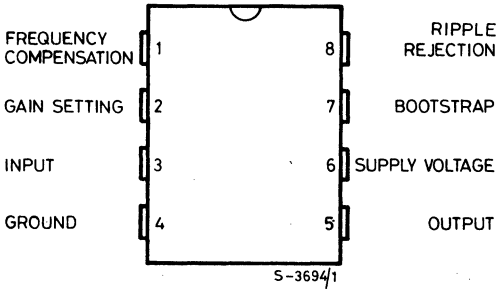
MECHANICAL DATA

Dimensions in mm

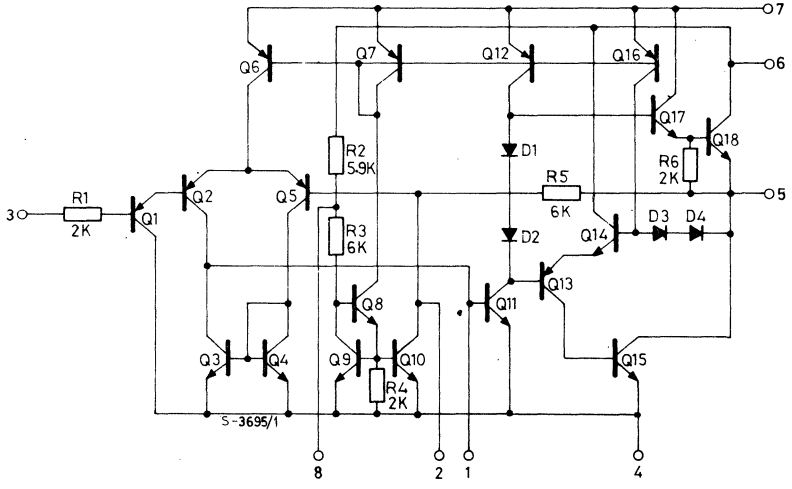


CONNECTION DIAGRAM

(top view)



SCHEMATIC DIAGRAM



TEST AND APPLICATION CIRCUITS

Fig. 1 - Circuit diagram with load connected to the supply voltage.

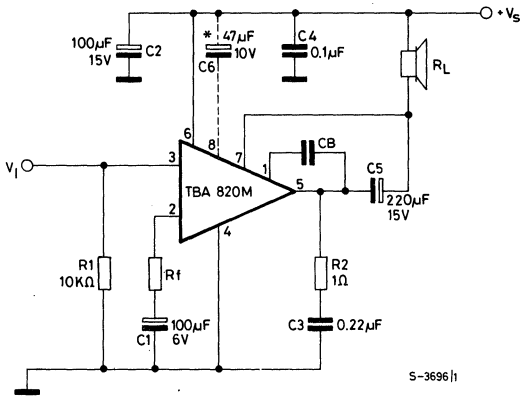
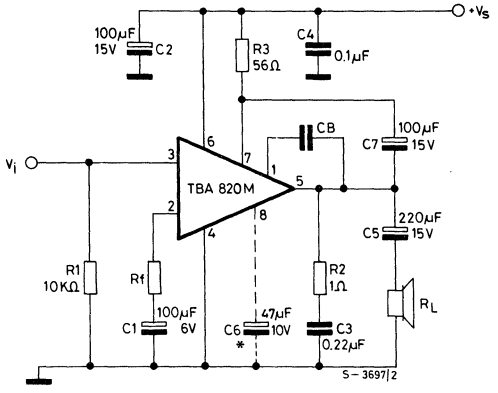


Fig. 2 - Circuit diagram with load connected to ground.



* Capacitor C6 must be used when high ripple rejection is requested.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits V_s= 9V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			3		16	V
V_o	Quiescent output voltage (pin 5)			4	4.5	5	V
I_d	Quiescent drain current				4	12	mA
I_b	Bias current (pin 3)				0.1		μA
P_o	Output power	d = 10% R_f= 120Ω V_s= 12V V_s= 9V V_s= 9V V_s= 6V V_s= 3.5V V_s= 3V	f = 1 kHz R_L= 8Ω R_L= 4Ω R_L= 8Ω R_L= 4Ω R_L= 4Ω R_L= 4Ω	 0.9 	 2 1.6 1.2 0.75 0.25 0.20	 	 W W W W W W
$V_{i\ (rms)}$	Input sensitivity	P_o= 1.2W R_L= 8Ω f = 1 kHz	R_f= 33Ω		16		mV
			R_f= 120Ω		60		
		P_o= 50 mW R_L= 8Ω f = 1 kHz	R_f= 33Ω		3.5		mV
			R_f= 120Ω		12		
R_i	Input resistance (pin 3)	f = 1 kHz			5		MΩ
B	Frequency response (-3 dB)	R_L= 8Ω C_5 = 1000 μF R_f= 120Ω	C_B= 680 pF	25 to 7,000			Hz
			C_B= 220 pF	25 to 20,000			
d	Distortion	P_o= 500 mW R_L= 8Ω f = 1 kHz	R_f= 33Ω		0.8		%
			R_f= 120Ω		0.4		
G_v	Voltage gain (open loop)	f = 1 kHz	R_L= 8Ω		75		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
G_v	Voltage gain (closed loop)	R_L= 8Ω	R_f= 33Ω		45		dB
		f = 1 kHz	R_f= 120Ω		34		
e_N	Input noise voltage (*)				3		μV
i_N	Input noise current (*)				0.4		nA
$\frac{S+N}{N}$	Signal to noise ratio (*)	P_o= 1.2W R_L= 8Ω G_v= 34 dB	R1= 10KΩ		80		dB
			R1= 50 kΩ		70		
SVR	Supply voltage rejection (test circuit of fig. 2)	R_L= 8Ω $f_{(ripple)}$ = 100 Hz C6= 47 μF R_f= 120Ω			42		dB

(*) B = 22 Hz to 22 KHz

Fig. 3 - Output power vs. supply voltage

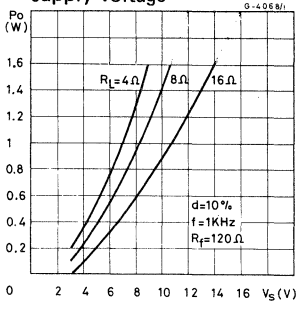


Fig. 4 - Harmonic distortion vs. output power

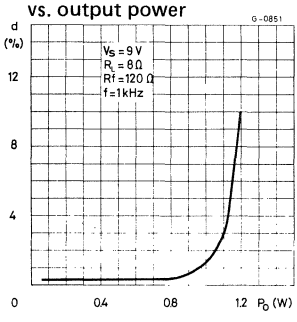


Fig.5 - Power dissipation and efficiency vs. output power

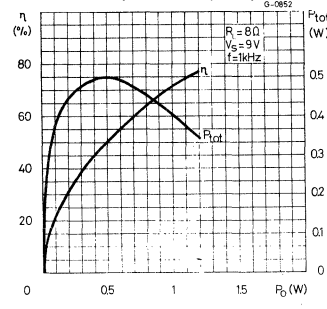


Fig. 6 - Maximum power dissipation (sine wave operation)

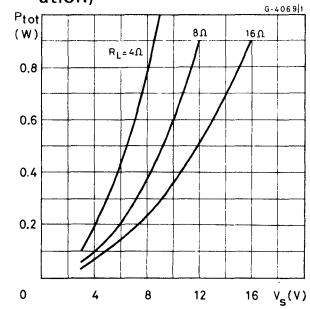


Fig. 7 - Suggested value of C_B vs. R_f

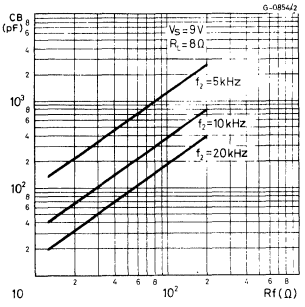


Fig. 8 - Frequency response

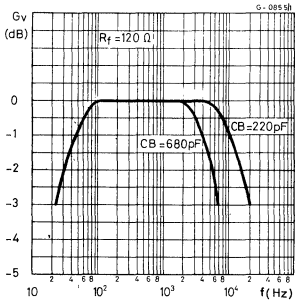


Fig. 9 - Input sensitivity vs. R_f

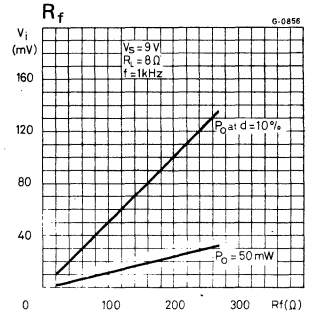


Fig. 10 - Voltage gain (closed loop) vs. R_f

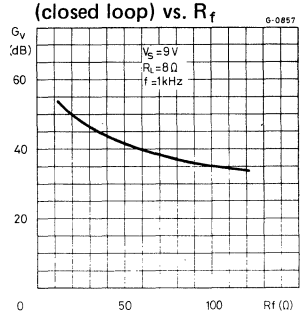


Fig. 11 - Harmonic distortion vs. frequency

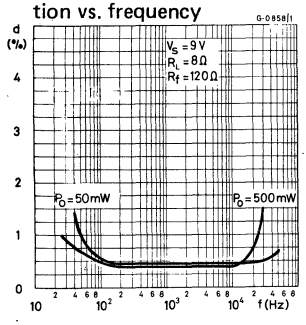


Fig. 12 - Supply voltage rejection (fig. 2 circuit)

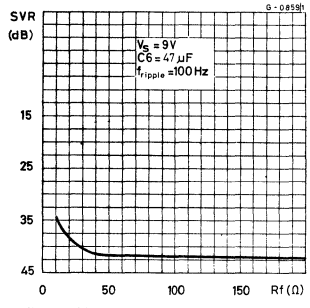


Fig. 13 - Quiescent output voltage at pin 5 vs. supply voltage

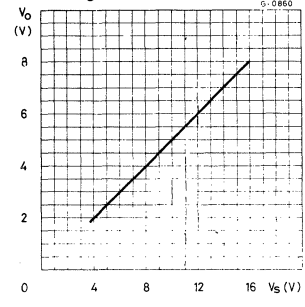
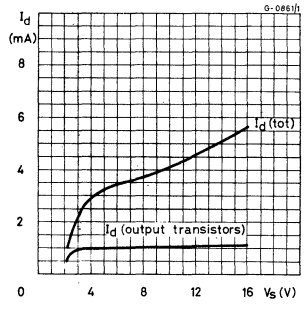


Fig. 14 - Quiescent current vs. supply voltage



APPLICATION INFORMATION

Fig. 15 - Low cost toy AM radio (0,5 to 1,5 MHz)

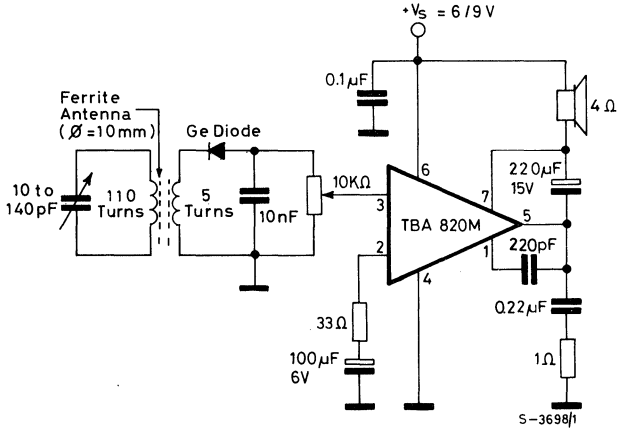
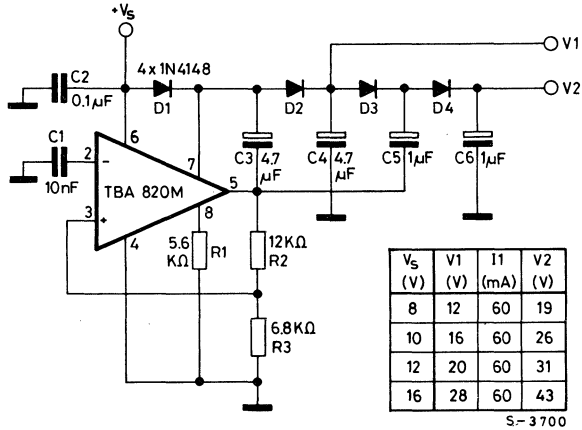


Fig. 16 - 1.5W DC/DC converter (f = 40 KHz)



V_S (V)	V1 (V)	I1 (mA)	V2 (V)
8	12	60	19
10	16	60	26
12	20	60	31
16	28	60	43

TCA 900
TCA 910

MOTOR SPEED REGULATORS

The TCA 900 and TCA 910 are monolithic integrated circuits in Jedec TO-126 plastic package. They are designed for use as speed regulators for DC motors of record players, cassette recorders and players. The TCA 900 is particularly suitable for battery operated portable equipments, and the TCA 910 for car-battery and mains operations.

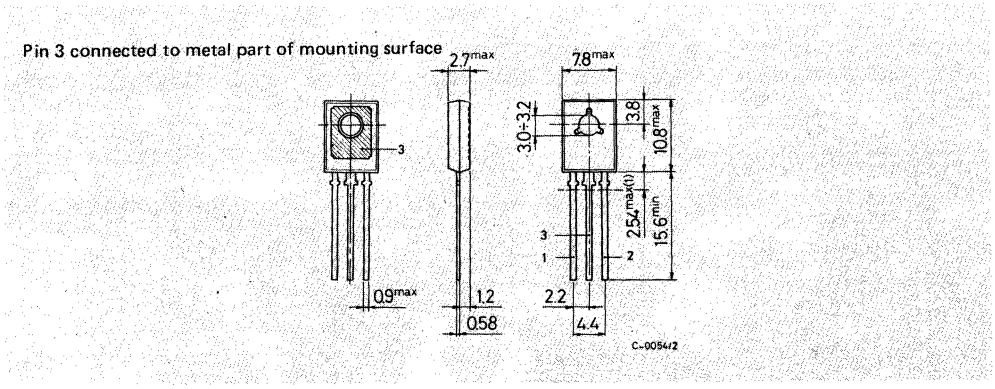
ABSOLUTE MAXIMUM RATINGS

		TCA 900	TCA 910
V_s	Supply voltage	14V	20V
P_{tot}	Total power dissipation at T_{amb} = 70°C	0.8 W	
	at T_{case} = 100°C	5 W	
T_{stg}	Storage temperature	-55 to 150 °C	
T_j	Junction temperature	150 °C	

ORDERING NUMBERS: TCA 900
TCA 910

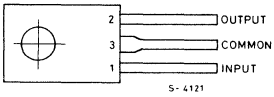
MECHANICAL DATA

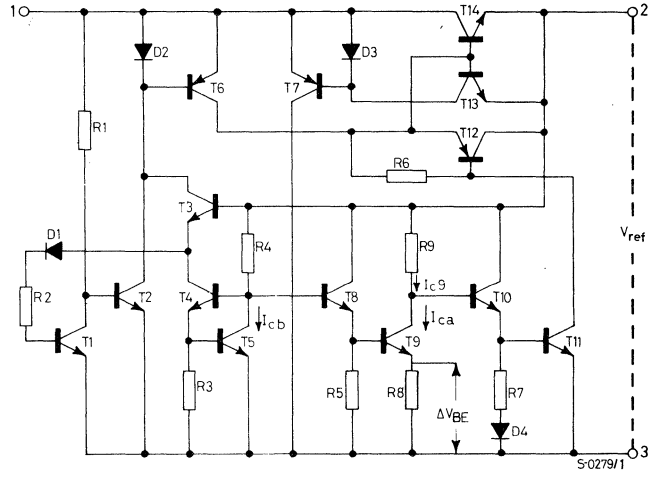
Dimensions in mm



TCA900
TCA910

CONNECTION AND SCHEMATIC DIAGRAMS





THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	Typ.	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	Typ.	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage (between pins 2 and 3)	V_s = 5.5V I_m = 70 mA R_T = 0		2.6		V
I_{d3}	Quiescent current (at pin 3)	V_s = 5.5V I_m= 0 R_T = 0		2.6		mA
V_m	Output voltage (for **TCA 900** only)	V_s = 5.5V I_m = 70 mA R_T = 91Ω		3.6	3.9	V
V_m	Output voltage (for **TCA 910** only)	V_s = 9V I_m = 70 mA R_T = 270Ω		5.6	6.3	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{1-2}	Dropout voltage	$\Delta V_m/V_m$= -1% I_m = 70 mA R_T = 91Ω		1.2		V
I_2	Limiting output current (at pin 2)	V_s = 5.5V V_{2-3}= 0		400		mA
$k = \Delta I_2/\Delta I_3$		V_s = 5.5V I_2 = 70 mA ΔI_2 = ± 10 mA R_T = 0		8.5		–
$\frac{\Delta V_m}{V_m}/\Delta V_s$	Line regulation (for **TCA 900** only)	V_s = 5.5V to 12V I_m = 70 mA R_T = 91Ω		0.1		%/V
$\frac{\Delta V_m}{V_m}/\Delta V_s$	Line regulation (for **TCA 910** only)	V_s = 10V to 16V I_m = 70 mA R_T = 270Ω		0.1		%/V
$\frac{\Delta V_m}{V_m}/\Delta I_m$	Load regulation	V_s = 5.5V I_m = 40 to 100 mA R_T = 0		0.005		%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T_{amb}$	Temperature coefficient	V_{1-3}= 5.5V I_2 = 70 mA T_{amb}= -20 to 70°C		0.01		%/°C

Fig. 1 - Test circuit.

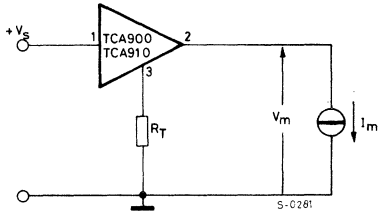


Fig. 2 - Typical application circuit.

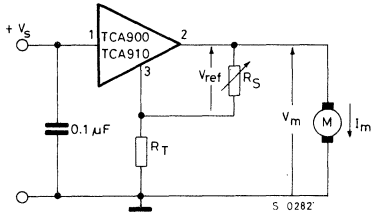


Fig. 3 - Normalized k vs. I_2.

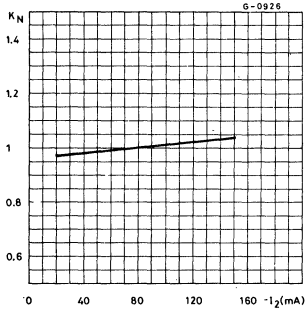


Fig. 4 - Dropout voltage vs. output current

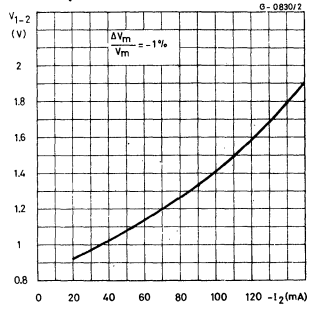
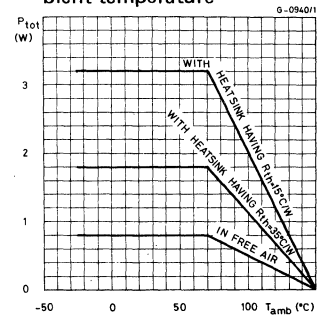


Fig. 5 - Maximum allowable power dissipation vs. ambient temperature



APPLICATION INFORMATION

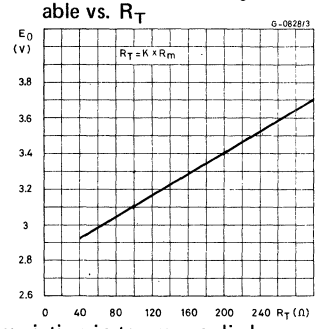
The regulator supplies the motor in such a way as to keep its speed constant, independent of supply voltage, applied torque and ambient temperature variations.
The basic equation for the motor is:

$$V_m = E_0 + R_m I_m = a_1 n + a_2 c$$

Where: V_m = supply voltage applied to the motor
E_0 = back electromotive force
n = motor speed (r.p.m.)
R_m = internal resistance (of the motor)
I_m = current absorbed (by the motor)
a_1 and a_2 = constants
c = drive torque

A voltage supply with the following characteristics
$E = E_0$ E = electromotice force
$R_o = -R_m$ R_o = output resistance
gives performance required.

Fig. 6 - Minimum E_0 allowable vs. R_T



This means that a variation in current absorbed by the motor, due to a variation in torque applied, causes a proportional variation in regulator output voltage. In fig. 6 is shown the minimum allowable E_0 vs. R_T.
The TCA 900 and TCA 910 give a reference constant voltage V_{ref} (between pins 2 and 3) independent of variations of V_s, I_2 and ambient temperature.
They also give: $I_3 = I_{d3} + I_2/k$

Where: I_3 = total current at pin 3
I_{d3} = quiescent current at pin 3 ($I_2 = 0$)
I_2 = current at pin 2
k = constant

The output voltage V_m, applied to the motor has the following value:

$$V_m = \underbrace{V_{ref} + R_T \left[\frac{V_{ref}}{R_s} \left(1 + \frac{1}{k}\right) + I_{d3} \right]}_{\text{Term 1}} + \underbrace{\frac{I_m}{k} R_T}_{\text{Term 2}}$$

Term 1 equals E_0 and fixes the motor speed by means of the variable resistor R_s;

Term 2 $\frac{I_m}{k} \cdot R_T$ equals the term $R_m \cdot I_m$ and, therefore, compensates variations of torque applied.
Complete compensation is achieved when:

$$R_T = k\ R_m$$

If $R_{T\ max} > k\ R_{m\ min}$ instability may occur.

LINEAR INTEGRATED CIRCUIT

TCA940N

10W AUDIO POWER AMPLIFIER

The TCA 940N is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier. The TCA 940N provides 10W output power @ 20V/4Ω, 7W @ 16V/4Ω and 6.5W @ 20V/8Ω. It gives high output current (up to 3A), very low harmonic and cross-over distortion. Besides the thermal shut-down, the device contains a current limiting circuit which restricts the operation within the safe operating area of the power transistors. The TCA 940N is pin to pin equivalent to the TBA 810 AS.

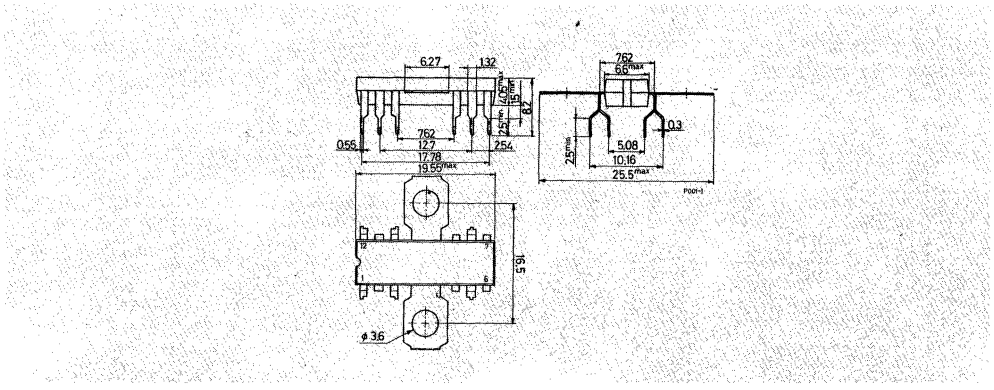
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (non-repetitive)	3.5	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation: at T_{amb} = 50°C	1.25	W
	at T_{tab} = 70°C	8	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TCA 940N

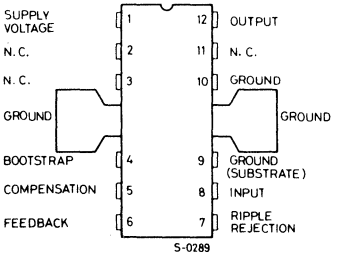
MECHANICAL DATA

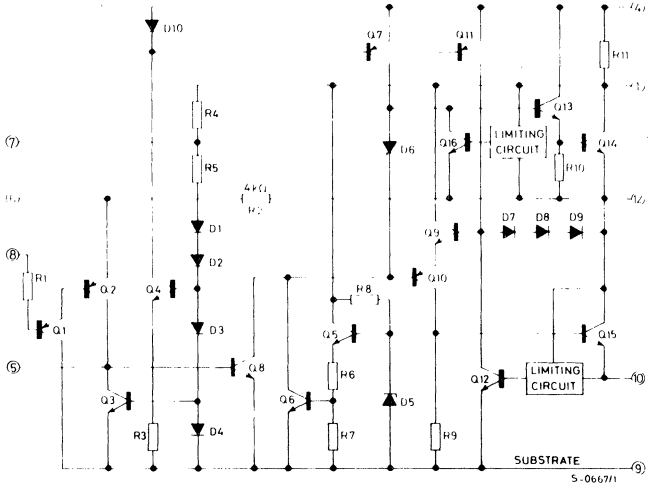
Dimensions in mm



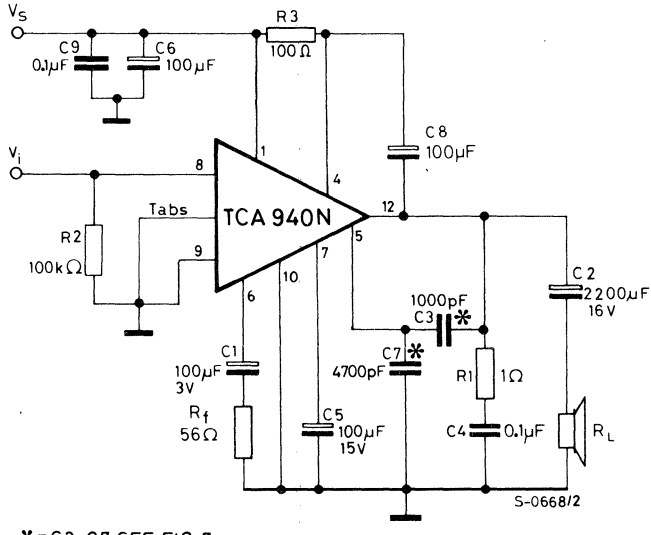
CONNECTION AND SCHEMATIC DIAGRAMS

(top view)





TEST AND APPLICATION CIRCUIT



*=C3, C7 SEE FIG. 7

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 1)		6		28	V
V_o	Quiescent output voltage (pin 12)	V_s = 18V	8.2	9	9.8	V
I_d	Quiescent drain current	V_s = 12V V_s = 24V		13 20		mA mA
I_b	Input bias current (pin 8)	V_s = 18V		0.5		μA
P_o	Output power	d = 10% f = 1 kHz V_s = 20V R_L = 4Ω V_s = 18V R_L = 4Ω V_s = 16V R_L = 4Ω V_s = 20V R_L = 8Ω V_s = 18V R_L = 8Ω	 7	 10 9 7 6.5 5		 W W W W W
$V_{i(rms)}$	Voltage for input saturation		250			mV
V_i	Input sensitivity	P_o = 9W V_s = 18V R_L = 4Ω f = 1 kHz		 90		 mV
B	Frequency response (-3 dB)	V_s = 18V R_L = 4Ω C_3 = 1000 pF	40 Hz to 20 KHz			
d	Distortion	P_o = 50 mW to 5W V_s = 18V R_L = 4Ω f = 1 kHz		 0.3		 %
R_i	Input resistance (pin 8)			5		MΩ
G_v	Voltage gain (open loop)	V_s = 18V R_L = 4Ω f = 1 kHz		 75		 dB
G_v	Voltage gain (closed loop)	V_s = 18V R_L = 4Ω f = 1 kHz	 34	 37	 40	 dB
e_N	Input noise voltage	V_s = 18V R_g = 0		3		μV
i_N	Input noise current	V_s = 18V		0.15		nA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
η	Efficiency	P_o = 9W V_s = 18V R_L = 4Ω f = 1 kHz		65		%
SVR	Supply voltage rejection	V_s = 24V R_L = 4Ω f_{ripple} = 100 Hz		45		dB
I_d	Drain current	P_o = 9W V_s = 18V R_L = 4Ω		770		mA
T_{sd}	Thermal shut-down (*) Case temperature	P_{tot} = 4.8W		110		°C

(*) See fig. 15.

Fig. 1 - Output power vs. supply voltage.

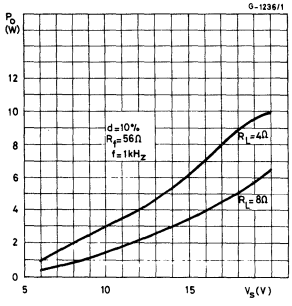


Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

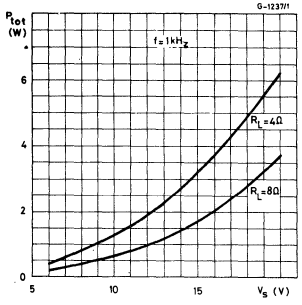


Fig. 3 - Distortion vs. output power.

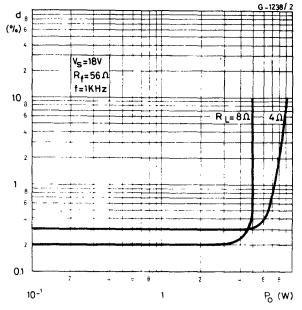


Fig. 4 - Voltage gain and input sensitivity vs. feedback resistance (R_f)

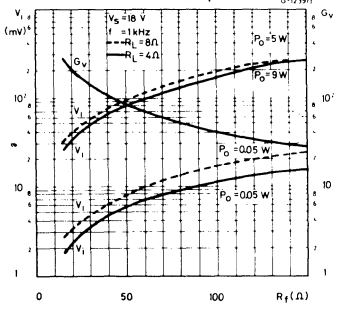


Fig. 5 - Distortion vs. frequency (R_L= 4Ω)

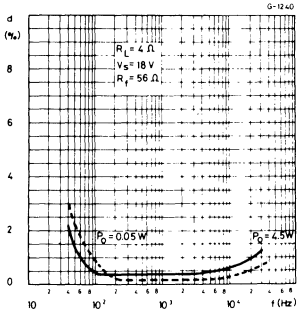


Fig. 6 - Distortion vs. frequency (R_L= 8Ω)

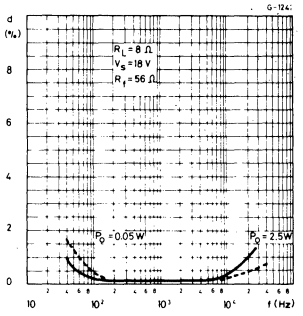


Fig. 7 - Value of C3 vs. R_f for different bandwidths

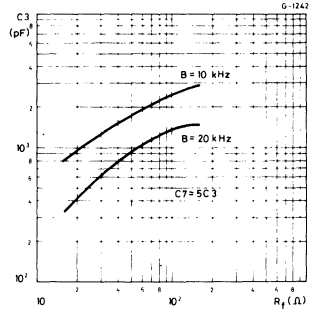


Fig. 8 - Supply voltage rejection vs. feedback resistance (R_f)

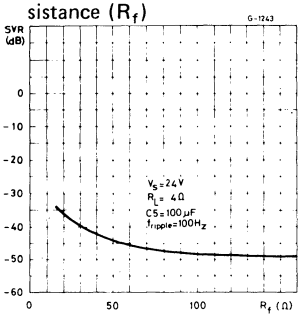


Fig. 9 - Power dissipation and efficiency vs. output power (R_L= 4Ω)

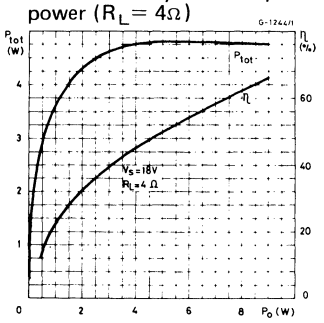


Fig. 10 - Power dissipation and efficiency vs. output power (R_L= 8Ω)

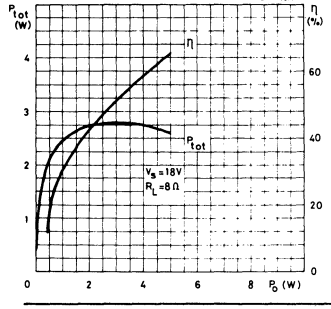


Fig. 11 - Quiescent output voltage (pin 12) vs. supply voltage

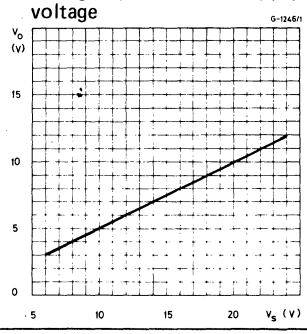
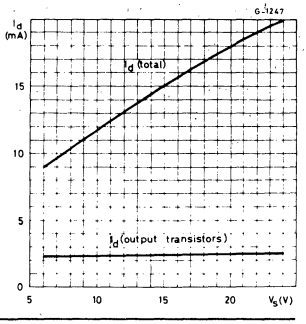


Fig. 12 - Quiescent current vs. supply voltage



SHORT CIRCUIT PROTECTION

The most important innovation in the TCA 940N is an original circuit which limits the current of the output transistors. Fig. 13 shows that the maximum output current is a function of the collector-emitter voltage; hence the circuit works within the safe operating area of the output power transistors. This can therefore be considered as being power limiting rather than simple current limiting. The TCA 940N is thus protected against temporary overloads or short circuit by the above circuit. Should the short circuit exists for a longer time, the thermal shut-down comes into action and keeps the junction temperature within safe limits.

Fig. 13 - Maximum output current vs. voltage (V_{CE}) across each output transistor

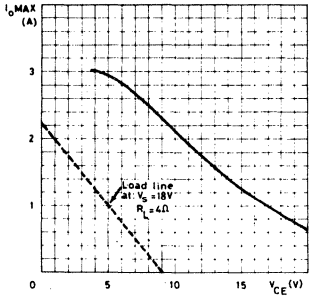
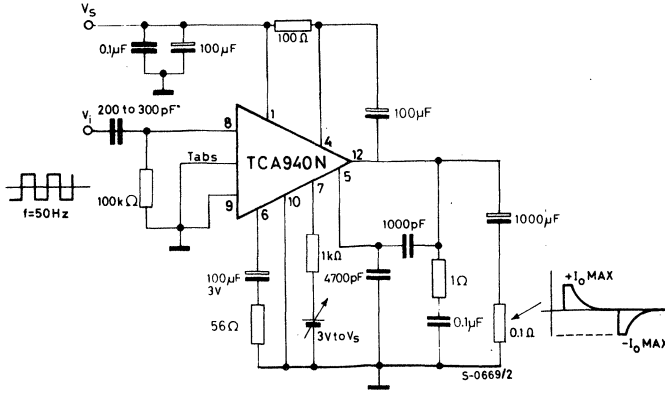


Fig. 14 - Test circuit for the limiting characteristics

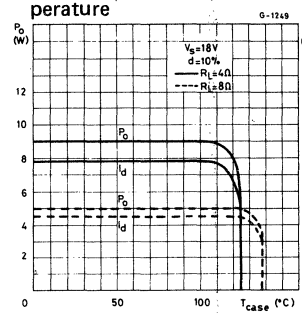


THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of too high a junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced (fig. 15).

Fig. 15 - Output power and drain current vs. case temperature



MOUNTING INSTRUCTION

The power dissipated in the circuit may be removed by connecting the tabs to an external heatsink according to fig. 16. The desired thermal resistance may be obtained by fixing the TCA 940N to a suitably dimensioned plate as shown in fig. 17. This plate can also act as a support for the whole printed circuit board; the mechanical stresses do not damage the integrated circuit. During soldering the tabs temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 16 - Maximum allowable power dissipation vs. ambient temperature

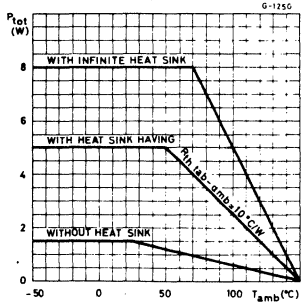


Fig. 17 - Mounting example

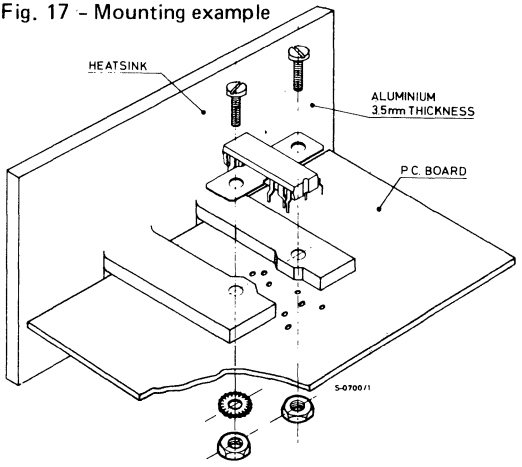
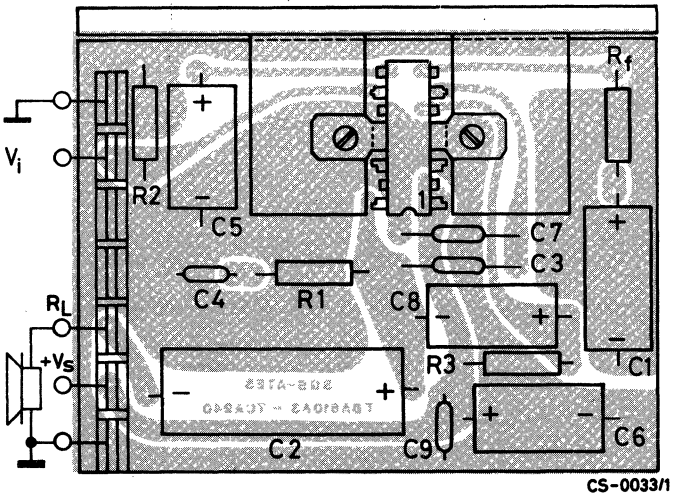


Fig. 18 - P.C. board and components layout of the test and application circuit (1:1 Scale).



TCA3089

LINEAR INTEGRATED CIRCUIT

FM-IF RADIO SYSTEM

- HIGH LIMITING SENSITIVITY
- HIGH AMR
- HIGH RECOVERED AUDIO
- GOOD CAPTURE RATIO
- LOW DISTORTION
- MUTING CAPABILITY

The TCA 3089 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It provides a complete subsystem for amplification of FM signals.
The functions incorporated are:
– FM amplification and detection
– Interchannel controlled muting
– AFC and delayed AGC for FM tuner
– Switching of stereo decoder
– Driver of a field strength meter
The TCA 3089 can be used for FM-IF amplifier application in Hi-Fi, car-radios and communication receivers.

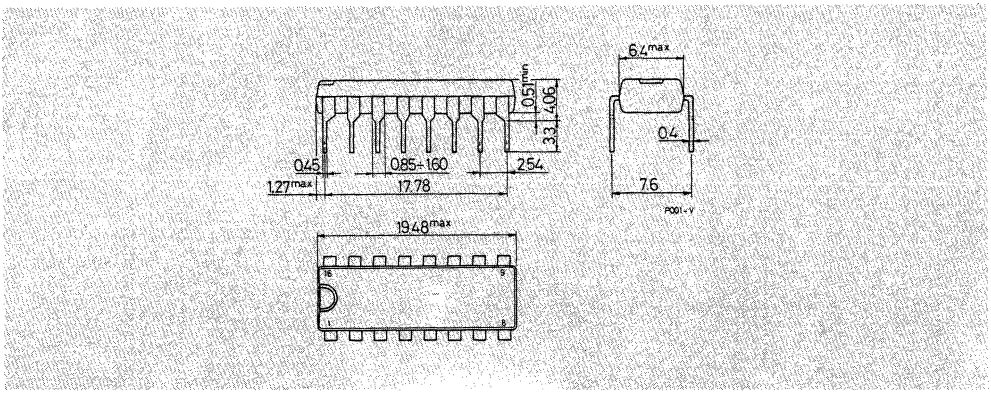
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output current (from pin 15)	2	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	-25 to 70	°C

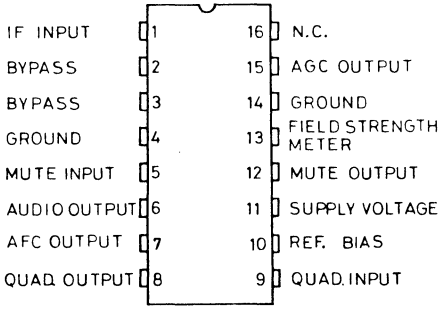
ORDERING NUMBER: TCA 3089

MECHANICAL DATA

Dimensions in mm



CONNECTION DIAGRAM
(top view)



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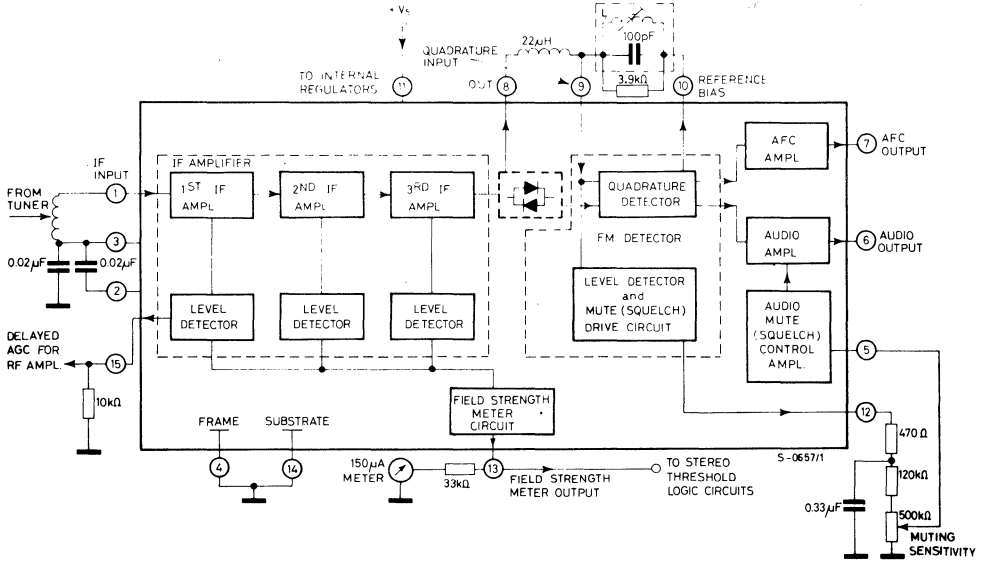
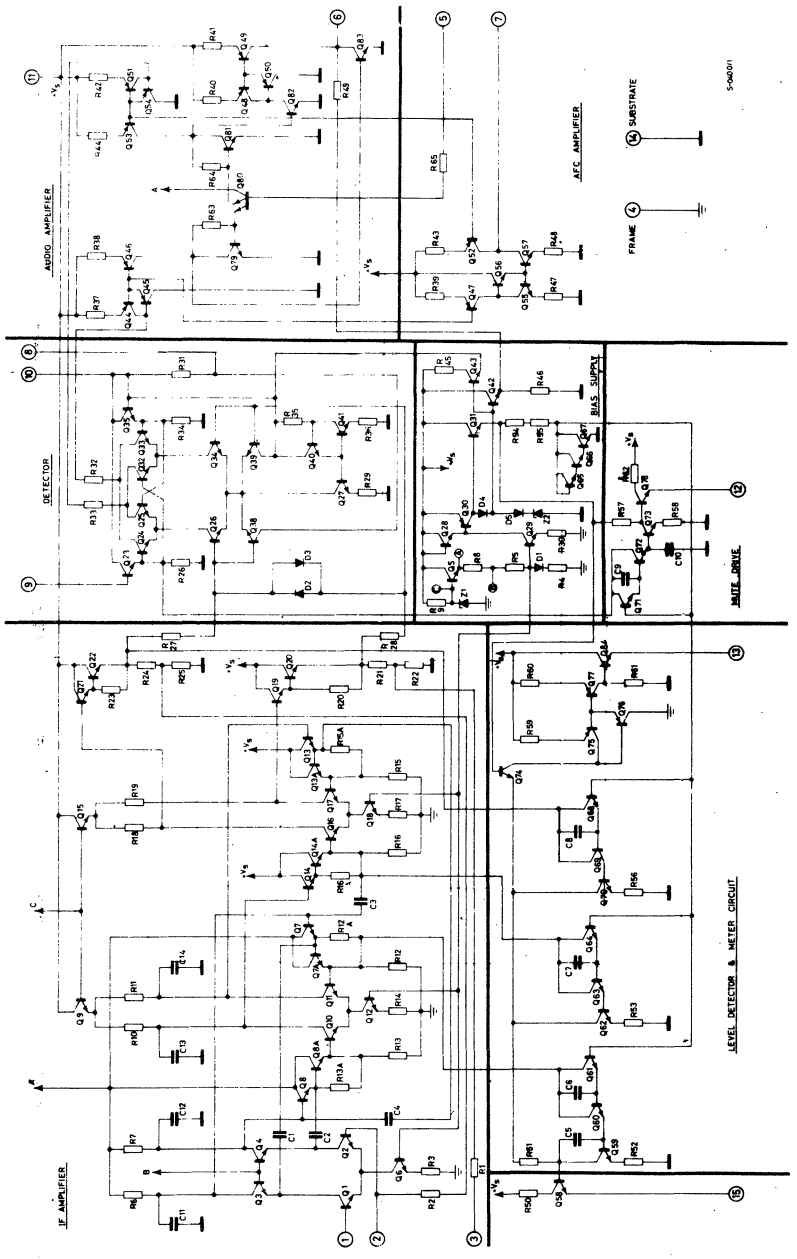
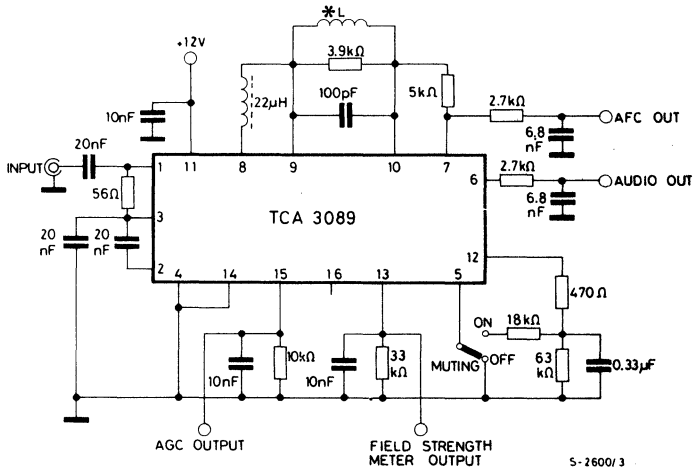
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUIT



*L tunes with 100pF at 10.7 MHz (Q_O=75)

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit; V_s= 12V, f_o = 10.7 MHz, V_5= 0V, T_{amb}= 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
I_s	Supply current		16	23	30	mA
V_i	Voltage at the IF amplifier input		1.2	1.9	2.4	V
V_2, V_3	Voltage at the input bypassing		1.2	1.9	2.4	V
V_6	Voltage at the audio output		5	5.6	6	V
V_{10}	Reference bias voltage		5	5.6	6	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
$V_{i(threshold)}$	Input limiting voltage (-3 dB) at pin 1	f_m= 1 kHz Δf= ± 75 kHz		12	25	μV
V_o	Recovered audio voltage (pin 6)	$V_i \geqslant 100\ \mu V$ f_m= 1 kHz Δf= ± 75 kHz	300	400	500	mV
V_7	Recovered audio voltage (pin 7)		200	350	500	mV
d	Distortion	$V_i \geqslant 1$ mV f_m= 1 kHz Δf= ± 75 kHz		0.5	1	%
$\frac{S+N}{N}$	Signal to noise ratio		60	67		dB
AMR	Amplitude modulation rejection	V_i = 100 mV f_m= 1 kHz Δf = ± 75 kHz m = 0.3	45	55		dB
V_i	Input voltage for delayed AGC action (pin 1)			10		mV
V_{15}	AGC output	V_i = 100 mV			0.5	V
$\frac{\Delta I_7}{\delta f}$	AFC control slope (note 1)	V_i = 10 mV		1.2		$\frac{\mu A}{kHz}$
V_{13}	Field strength meter output sensitivity	V_i = 0.5 mV		1.5		V
	No signal mute (note 2)	muting: ON	55			dB

Note: 1) $\Delta I_7 = \frac{\Delta V_{7,10}}{R_{7,10}}$

2) No signal mute = $20 \log \frac{V_o @ V_i \geqslant 100\ \mu V}{V_o @ V_i = 0}$

Fig. 1 - Relative recovered audio and noise output vs. input voltage

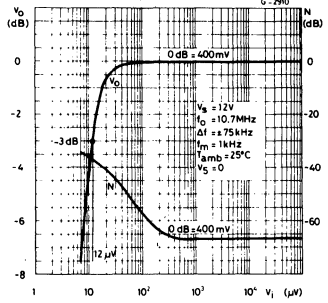


Fig. 2 - Capture ratio vs. input voltage

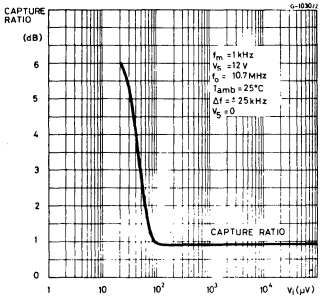


Fig. 3 - AGC (V_{15}) and field strength meter output (V_{13}) vs. input voltage

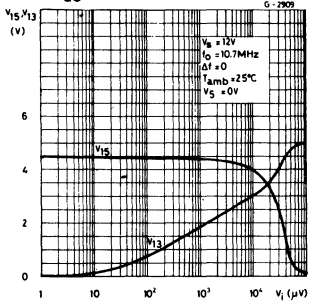


Fig. 4 - AFC output current vs. change in tuning frequency

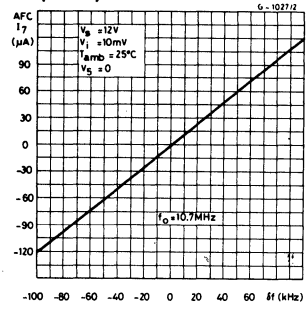


Fig. 5 - Amplitude modulation rejection vs. input voltage

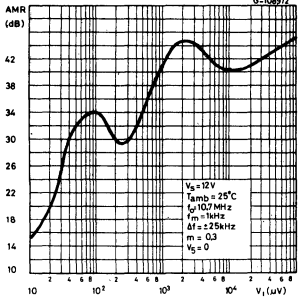
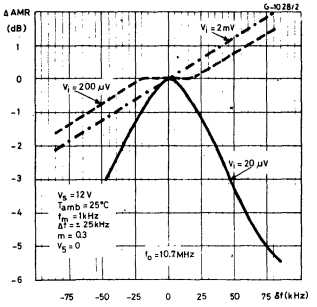


Fig. 6 - AMR vs. change in tuning frequency



APPLICATION INFORMATION

Fig. 7 - P.C. board and component layout of the circuit of fig. 8 (1:1 scale)

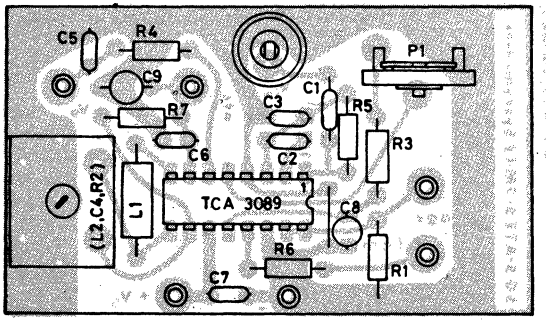


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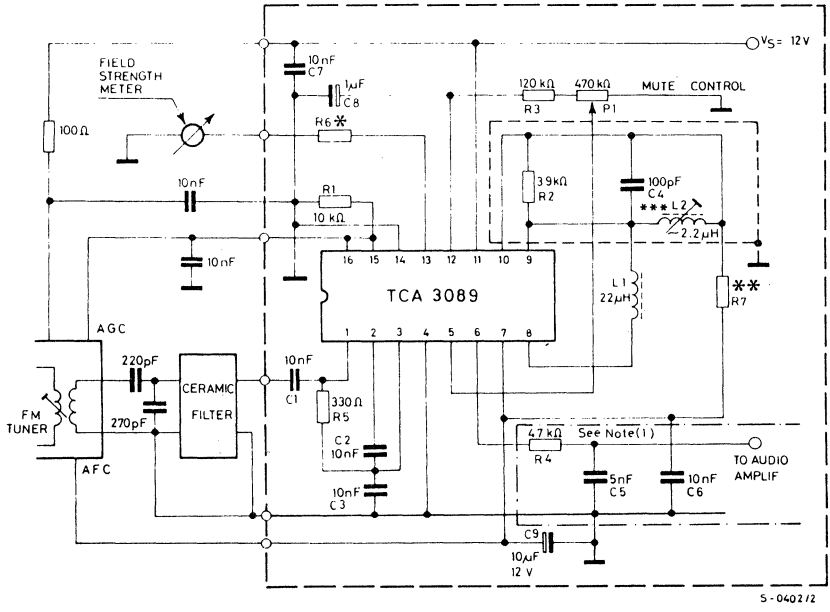
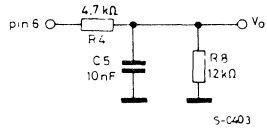
Fig. 8 - Typical application circuit



Notes (1): When V_S is less than 12V, a resistor R8= 12 kΩ must be connected between audio output and ground, and the integrator capacitor C5 must be changed to 10 nF, as follows:



* Dependent on field strength meter sensitivity.
** Dependent on the tuner's AFC circuit.
*** L2 tunes with 100 pF at 10.7 MHz (Q_o = 75)

LINEAR INTEGRATED CIRCUIT

TCA3189

FM-IF HIGH QUALITY RADIO SYSTEM

- EXCEPTIONAL LIMITING SENSITIVITY
- VERY LOW DISTORTION (0.1% - DOUBLE TUNED DETECTOR COIL)
- IMPROVED S/N RATIO
- EXTERNALLY PROGRAMMABLE AUDIO LEVEL
- ON CHANNEL STEP FOR SEARCH CONTROL
- PROGRAMMABLE AGC VOLTAGE AND AFC FOR TUNER
- INTERCHANNEL MUTING (SQUELCH)
- DEVIATION MUTING
- DIRECT DRIVE OF TUNING METER
- DIRECT DRIVE OF FIELD STRENGTH METER

The TCA 3189 is a monolithic integrated circuit in a 16-lead dual in-line plastic package, which provides a **complete subsystem** for amplification of 10.7 MHz FM signal in Hi-Fi, car-radios and communications receivers.

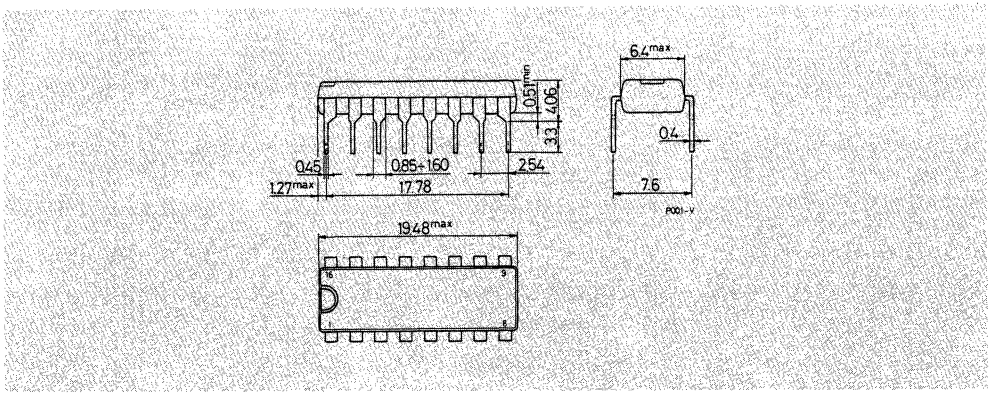
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
I_o	Output current (from pin 15)	2	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	-25 to 85	°C

ORDERING NUMBER: TCA 3189

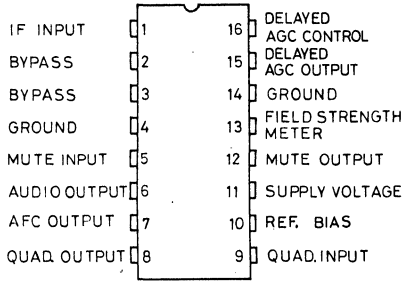
MECHANICAL DATA

Dimensions in mm



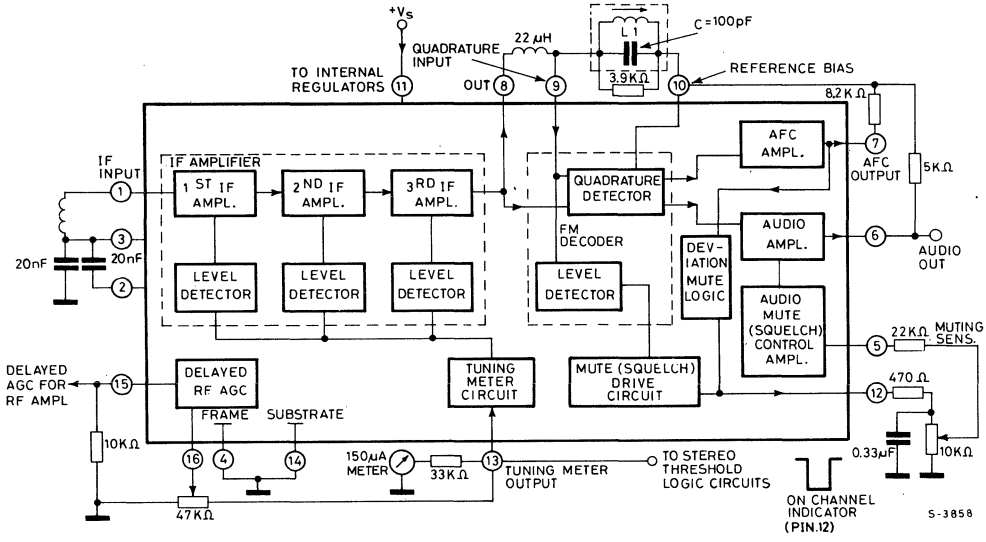
TCA3189

CONNECTION DIAGRAM
(top view)

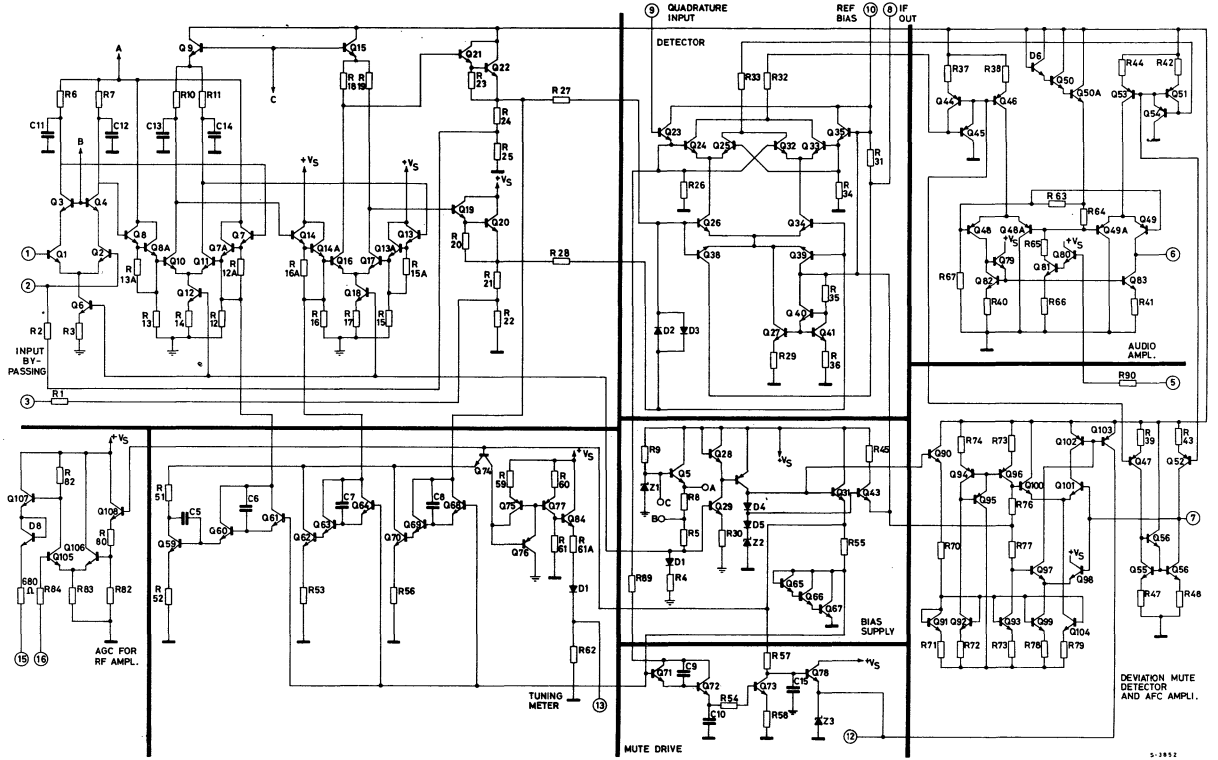


S-3286

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

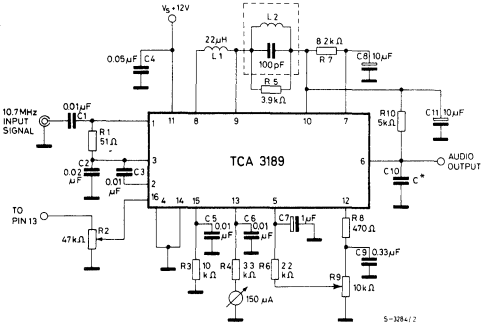
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 12V$, $T_{amb} = 25°C$)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage range	No signal input, non muted		9		16	V
I_s	Supply current			20	31	44	mA
V_1	Voltage at the IF amplifier input			1.2	1.9	2.4	V
V_2, V_3	Voltage at the input bypass			1.2.	1.9	2.4	V
V_{15}	Voltage at the pin 15 (RF AGC)			7.5	9.5	11	V
V_{10}	Reference bias voltage			5	5.6	6	V
V_i	Input limiting voltage (-3 dB) at pin 1	f_o = 10.7 MHz f_m= 1 KHz Δf= ± 75 KHz			12	25	μV
V_o	Recovered audio voltage (pin 6)	$V_i \geqslant 50\ \mu V$ f_o = 10.7 MHz f_m= 1 KHz Δf= ± 75 KHz		325	500	650	mV
d	Distortion (single tuned)	$V_i \geqslant 1$ mV f_o = 10.7 MHz f_m= 1 KHz Δf = ± 75 KHz			0.5	1	%
d	Distortion (double tuned)				0.1		%
$\frac{S+N}{N}$	Signal to noise ratio			65	72		dB
AMR	Amplitude modulation rejection	V_i = 100 mV f_o = 10.7 MHz f_m = 1 KHz Δf = ± 75 KHz AM mod. 30%		45	55		dB
V_{16}	RF AGC threshold				1.25		V
$\frac{\Delta I_7}{\Delta f}$	AFC control slope				1.9		$\frac{\mu A}{KHz}$
V_{12}	On channel step (deviation mute)	V_i = 100 mV	$f_{DEV.} <$ ± 40 KHz		0		V
		f_o = 10.7 MHz	$f_{DEV.} >$ ± 40 KHz		5.6		V

TEST CIRCUITS

Single tuned detector coil



Double tuned detector coil

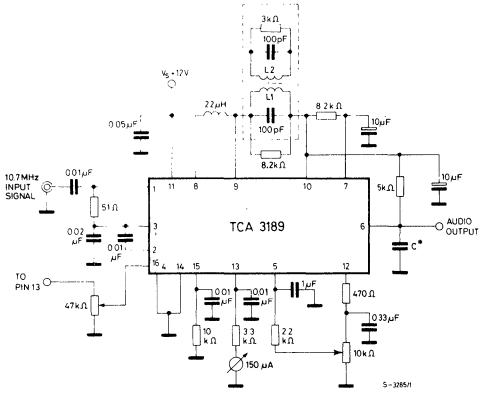


Fig. 1 - P.C. board and component layout of the single tuned circuit (1:1 scale)

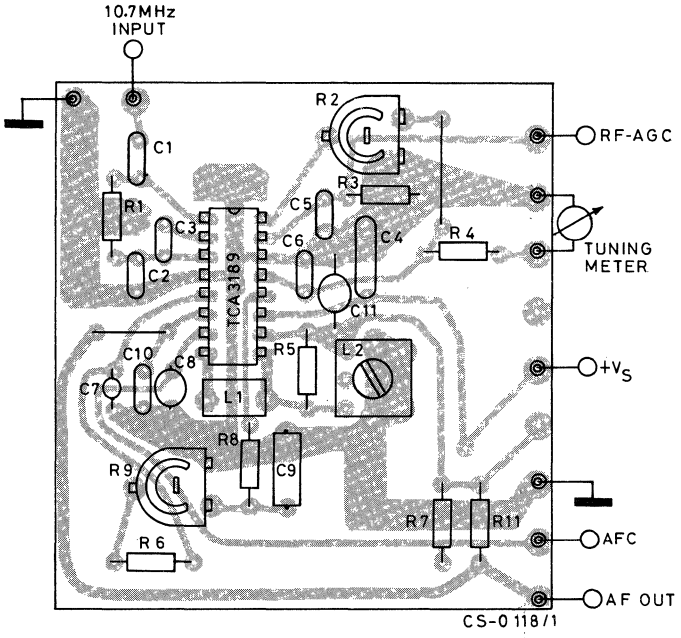


Fig. 2 - Limiting and noise characteristics

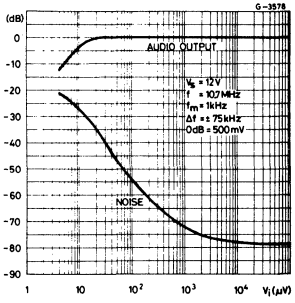


Fig. 3 - Deviation mute threshold vs. R_{7-10}

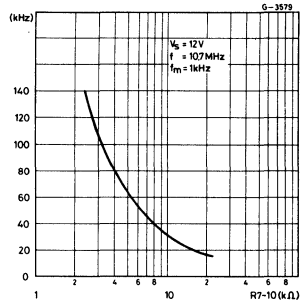


Fig. 4 - Recovered audio and muting action vs. input level

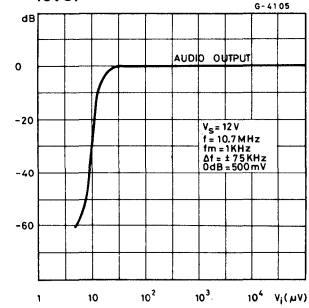


Fig. 5 - AFC characteristics

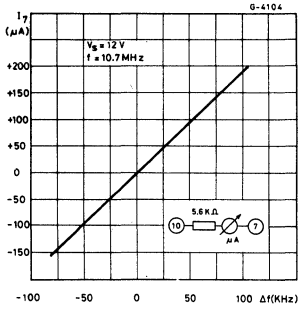


Fig. 6 - AGC voltage for FM tuner vs. input level

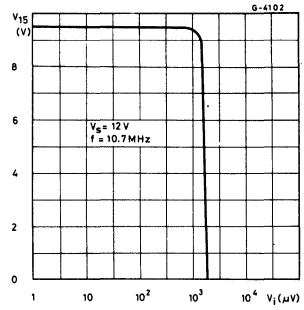
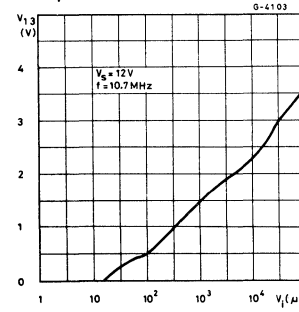


Fig. 7 - Field strength and tuning meter output vs. input level



FEATURES	TCA 3189	TCA 3089
Low Limiting Sensitivity (25 μV max.)	Yes	Yes
Low Distortion (< 1%)	Yes	Yes
Single-coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No
AFC and delayed AGC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Typical S + N/N > 60 dB	Yes	Yes
Meter Drive Voltage Depressed at Very-Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No

LINEAR INTEGRATED CIRCUIT

TDA440S

TV VISION IF SYSTEM

The TDA 440S is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:

- Gain controlled vision IF amplifier
- Synchronous detector
- AGC detector with gating facility
- AGC amplifier for PNP tuner drive with variable delay
- Video preamplifier with positive and negative outputs.

It is intended for use in black and white and colour TV receivers.

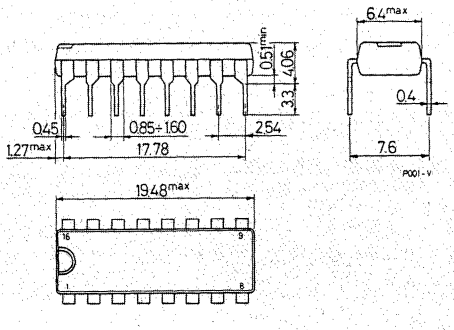
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 13)	15	V
V_5	Voltage at pin 5	15	V
V_{10}	Voltage at pin 10	-1 to 3	V
V_{11}	Voltage at pin 11 (with load connected to V_s)	8	V
I_{11}, I_{12}	Output current	5	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}	Storage temperature	-55 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBER: TDA 440S

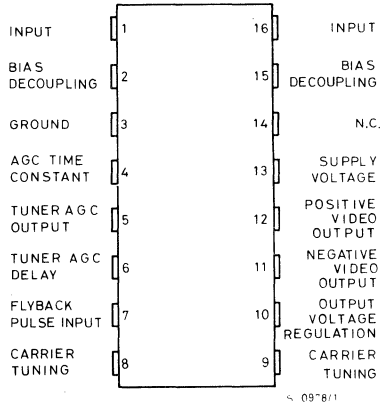
MECHANICAL DATA

Dimensions in mm

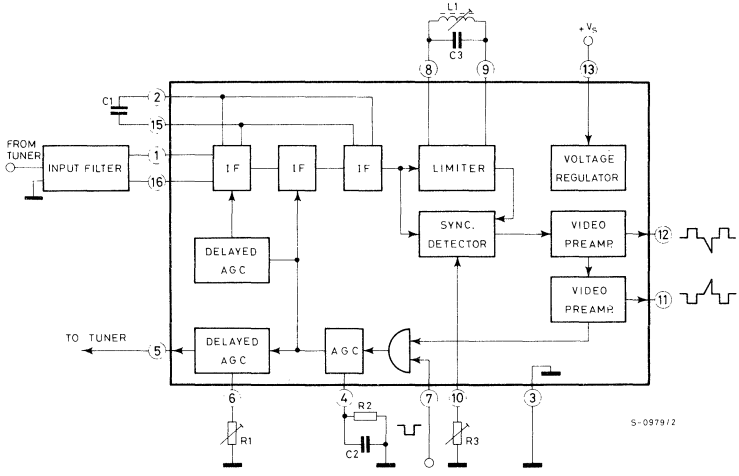


TDA440S

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to fig. 1 test circuit, T_{amb}= 25°C)

Parameter		Test conditions		Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS								
V_s	Supply voltage range (pin 13)			10	12	15	V	
I_s	Supply current (pin 13)	V_s = 12V			50		mA	1a
$-I_{11}$ (1)	Output current	V_s = 15V	V_{11}= 8V		1.6		mA	1b
V_{11} (2)	Output voltage	V_s = 12V	$R_5 = \infty$			4.5	V	
			R_5 = 0	7				1a
V_{12} (2)	Output voltage	V_s = 12V	V_{11} = 5.5V		5.6		V	1a
$\frac{\Delta V_{11}}{\Delta V_s}$	Output voltage drift	V_s = 11 to 14V			3.5		%	1b
AC CHARACTERISTICS (Refer to fig. 2 test circuit, V_s = 12V, T_{amb}= 25°C)								
I_5 (3)	Tuner AGC current	V_7 = 0 f_0 = 38.9 MHz	R_4 = 2.5 KΩ	6	9.5		mA	3c
V_7	AGC gating pulse input peak voltage	f = 15.6 kHz		-1.5		-5	V	—
V_i (4)	Input sensitivity	V_7 = 0 V_{11} = 3.3V peak to peak	f_0 = 38.9 MHz	100	150	220	μV	3c
ΔV_i	AGC range	V_7 = 0 f_0 = 38.9 MHz V_{11} = 3.3V peak to peak	ΔV_o = 1 dB	50	60		dB	
V_o	Peak to peak output voltage at pin 11	V_7 = 0 f_0 = 38.9 MHz V_i = see note (5)	V_{11} = 5.5V	3.3	3.5	3.7	V	

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
ΔV_o	Video output variation over the AGC range (0 to 5.5 MHz)	V_7 = 0 ΔV_i = 50 dB V_{11} = 3.3V peak to peak f_0 = 38.9 MHz f_m = 0 to 5.5 MHz		1	2	dB	3b
V_{11}, V_{12}	Sound IF at video outputs (5.5 MHz)	V_7 = 0 V_i = see note (5) f_0 (vision) = 38.9 MHz f_0 (sound) = 33.4 MHz	30			mV	3d
	Differential error of the output voltage (B & W)	V_7 = 0 f_0 = 38.9 MHz V_{11} = 3.3V peak to peak			15	%	—
V_{11}, V_{12}	Video carrier and video carrier 2nd harmonic leakage at video outputs	V_7 = 0 V_i = see note (5) f_0 = 38.9 MHz		15		mV	3c
V_{11}, V_{12}	Video carrier leakage at video outputs			5		mV	
B	Frequency response (-3 dB)		8	10		MHz	3d
d_{im}	Intermodulation products at video outputs	V_7 = 0 V_i = see note (5) f_0 (vision) = 38.9 MHz f_0 (sound) = 33.4 MHz f_0 (chroma) = 34.5 MHz		-50	-40	dB	3a
R_i	Input resistance (between pins 1 and 16)	V_7 = 0 V_i = see note (5) f_0 = 38.9 MHz		1.4		kΩ	—
C_i	Input capacitance (between pins 1 and 16)			2		pF	—

NOTES:
(1) Current flowing out from pin 11 with the load connected to V = 8V.
(2) V_{11} and V_{12} are adjustable simultaneously by means of the resistance, or by a variable voltage $\leqslant$ 0.6V, connected between pin 10 and ground.
(3) Measured with an input voltage 10 dB higher than the V_i at which the tuner AGC current starts.
(4) RMS values of the unmodulated video carrier (modulation down).
(5) The input voltage V_i can have any value within the AGC range.

Fig. 1a – Test circuit for measurement of I_S, V_{11}, V_{12}

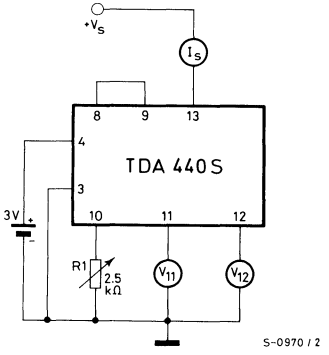


Fig. 1b – Test circuit for measurement of $-I_{11}$ and $\Delta V_{11}/\Delta V_s$

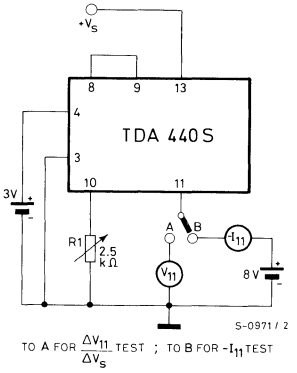
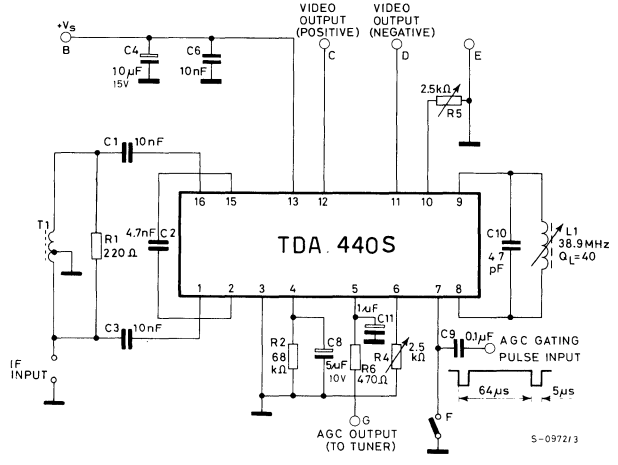


Fig. 2 – AC test circuit



Note: T_1 = 50/200Ω Balun transformer.
V_i = Input voltage between pins 1 and 16.

Fig. 3a - Set-up for measurement of d_{im}

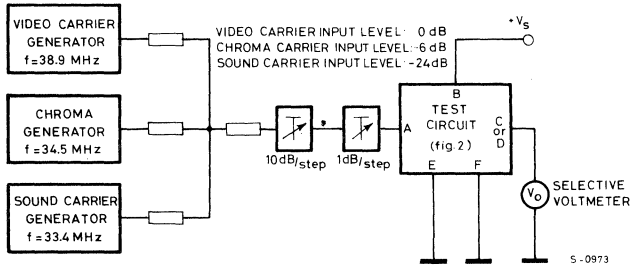


Fig. 3b - Set-up for measurement of ΔV_o

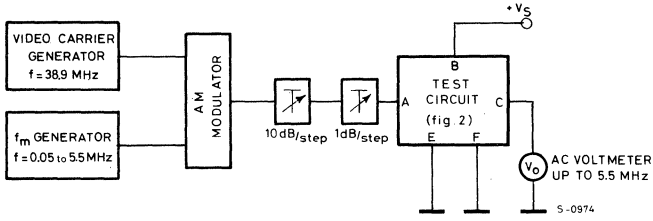


Fig. 3c - Set-up for measurement of I_5, V_i, ΔV_i, V_o, V_{11} and V_{12}

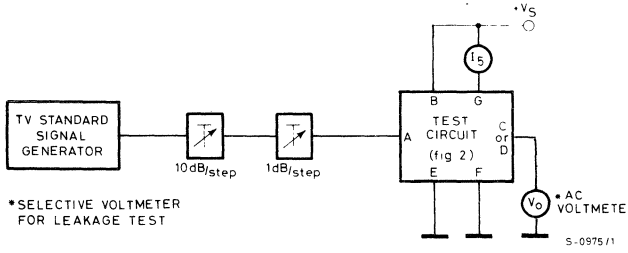


Fig. 3d - Set-up for measurement of B, V_{11} and V_{12}

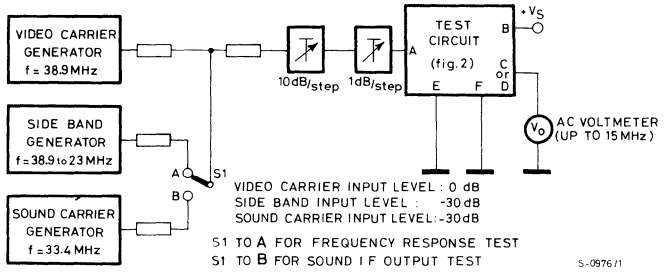


Fig. 4 - AGC voltage vs. input voltage variation

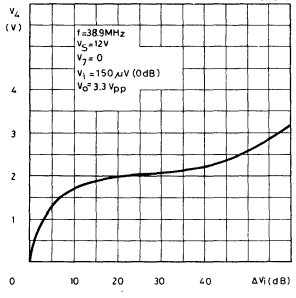


Fig. 5 - Tuner AGC output current vs. IF gain variation

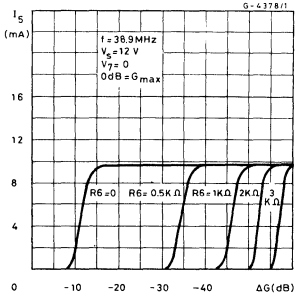
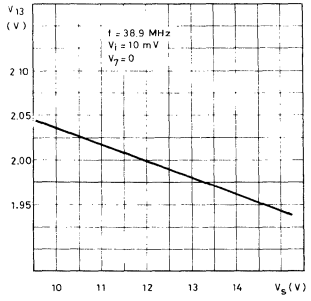


Fig. 6 - Output black level vs. supply voltage



APPLICATION INFORMATION

The TDA 440S enables very compact IF amplifiers to be designed and provides the performance demanded by high quality receivers.

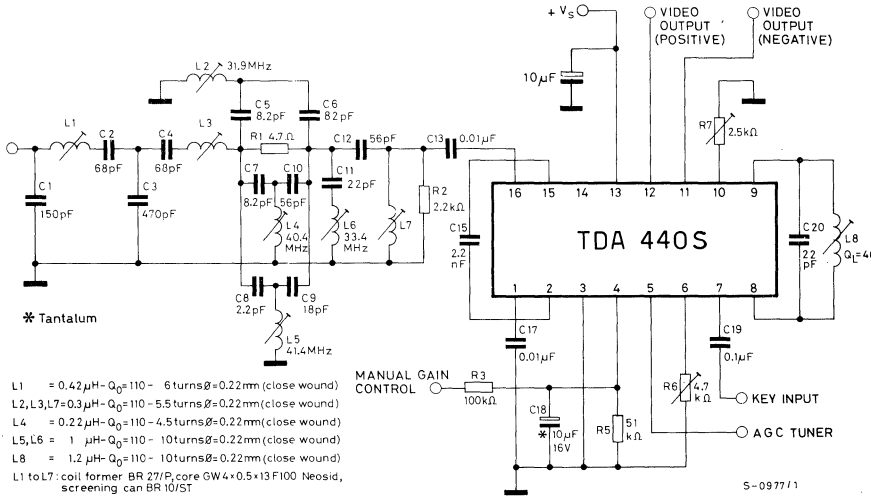
The input tuning-trapping circuitry and the detector network can be aligned independently with respect to each other.

The value of Q for the parallel tuned circuit between pin 8 and 9 is not critical, although the higher it is, the better is the chroma-sound beat rejection, but the tuning is more critical. Values of Q from 30 to 50 give good rejection with non-critical tuning.

The LC circuit between pins 8 and 9 is tuned to the vision carrier thus appreciably attenuating the sidebands. Hence a small amount of signal can be removed whose amplitude is almost constant over the whole working range of the AGC and it can be used to drive an AFC circuit.

The black level at the output is very stable against variations of V_s and of temperature: this enables the contrast control to be kept simple. The AGC is of the gated type and can take the top of the synchronism or the black level (back porch) as its reference: when the latter is used, the output black level is particularly stable.

Fig. 8 - Typical application circuit.



Typical performance of the Fig. 8 circuit

Frequency response (f_0 vision = 38.9 MHz, f_0 sound = 33.4 MHz) standard CCIR		
Sound carrier attenuation	28	dB
31.9 MHz trap attenuation	⩾ 60	dB
40.4 MHz trap attenuation	⩾ 56	dB
41.4 MHz trap attenuation	⩾ 44	dB
AGC range	55	dB
Overall gain including IF filter and trap circuits (note 1)	86	dB
Intermodulation products over the whole AGC range (note 2)	- 55	dB

NOTES: (1) The gain is measured at video output 3.3V peak to peak and is defined as peak to peak output voltage to RMS input voltage (modulation down).

(2) Measured at 1.07 MHz, vision carrier level = 0 dB, chroma carrier level = -6 dB, sound carrier level = -6 dB.

Fig. 9 - Overall frequency response of the fig. 8 circuit

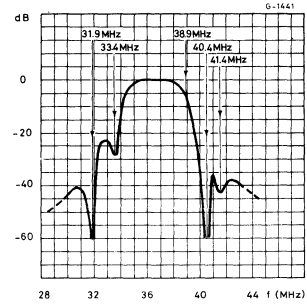
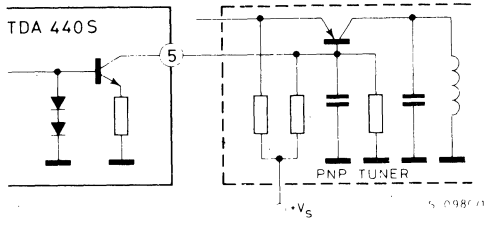
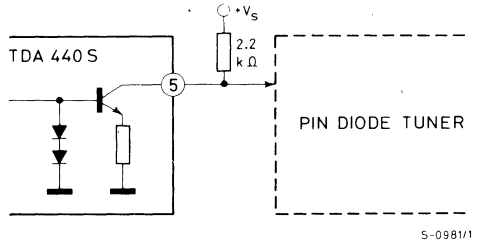
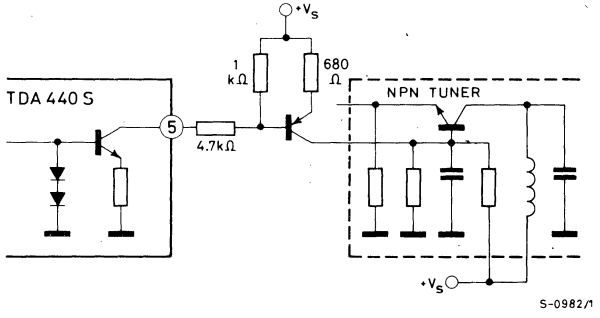


Fig. 10 – Circuit options for tuner AGC driving







TDA1054M

LINEAR INTEGRATED CIRCUIT

PREAMPLIFIER WITH ALC FOR CASSETTE RECORDERS

- EXCELLENT VERSATILITY in USE (V_s from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- GOOD SUPPLY RIPPLE REJECTION
- STEREO MATCHING BETTER THAN 3 dB

The TDA 1054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:
- Low noise preamplifier
- Automatic level control system (ALC)
- High gain equalization amplifier
- Supply voltage rejection facility (SVRF).

It is intended as preamplifier in cassette tape recorders and players, dictaphones, compressor and expander in industrial equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

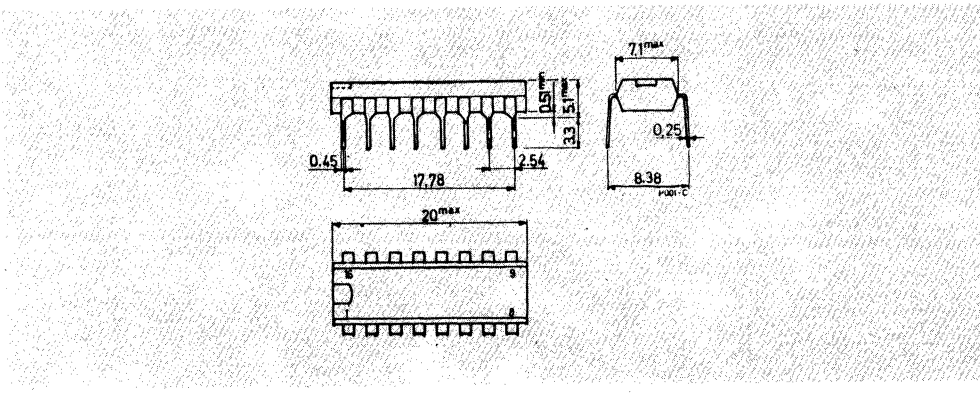
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 50°C$	500	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

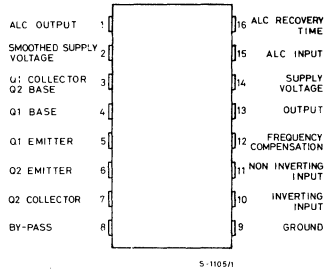
ORDERING NUMBERS: TDA 1054M mono applications
2 TDA 1054M stereo applications

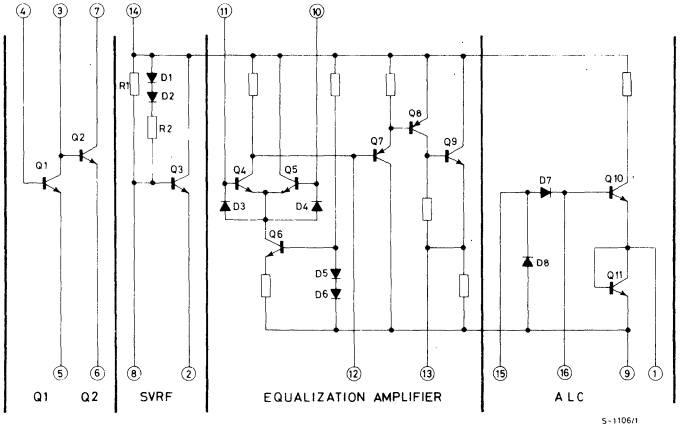
MECHANICAL DATA

Dimensions in mm

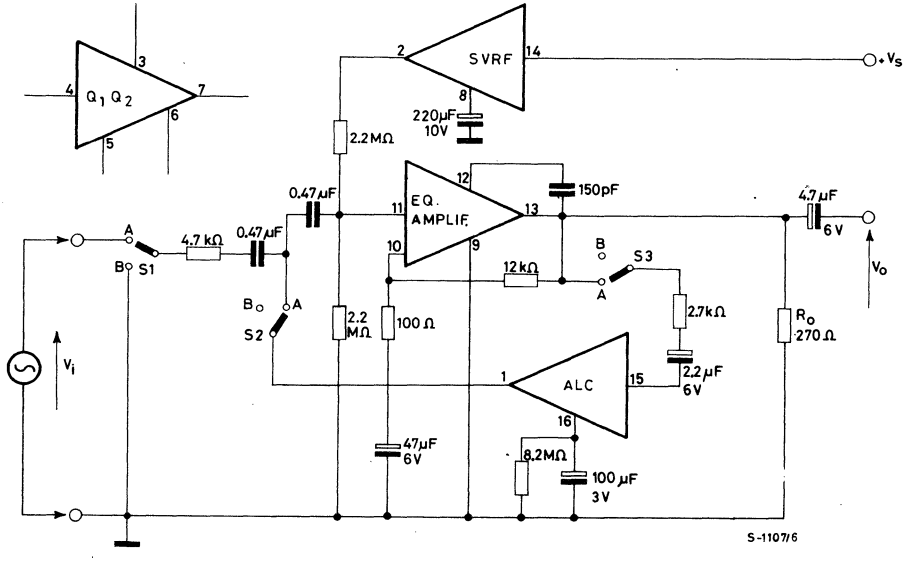


CONNECTION AND SCHEMATIC DIAGRAMS
(top view)





TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $T_{amb} = 25°C$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_d	Quiescent drain current	$V_s = 9V$ $R_L = \infty$ S1 = S2 = S3 = B		6		mA
h_{FE}	DC current gain	$I_C = 0.1$ mA $V_{CE} = 5V$	300	500		–
e_N	Input noise voltage (Q1)	$I_C = 0.1$ mA $V_{CE} = 5V$ f = 1 kHz		2		$\frac{nV}{\sqrt{Hz}}$
i_N	Input noise current (Q1)			0.5		$\frac{pA}{\sqrt{Hz}}$
NF	Noise figure (Q1)	$I_C = 0.1$ mA $V_{CE} = 5$ V $R_g = 4.7$ kΩ B (-3 dB) = 20 to 10,000 Hz		0.5	4	dB
G_V	Open loop voltage gain (for equalization amplifier)	$V_s = 9V$ f = 1 kHz		60		dB
V_o	Output voltage with A.L.C.	$V_s = 9V$ $V_i = 100$mV f = 1 kHz S1 = S2 = S3 = A		1.1		V
R1	(for SVRF system)	see schematic diagram		7.5		kΩ
R2	(for SVRF system)			120		Ω
e_N	Input noise voltage (for equalization amplifier pin 11)	$V_s = 9V$ $R_g = 4.7$ kΩ $G_V = 40$ dB S1 = B B (-3 dB)= 22 Hz to 22 KHz		1.3		μV
V_{DR}	Drop-out (between pins 14 and 2)	$V_s = 9V$ $I_d = 6$ mA		0.8		V

Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (input transistor Q_1)

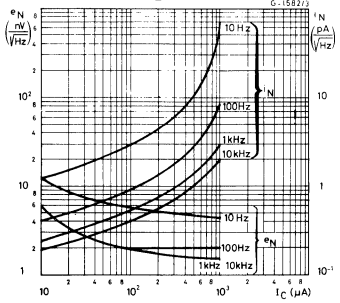


Fig. 2 - Equivalent input noise current vs. frequency (input transistor Q_1)

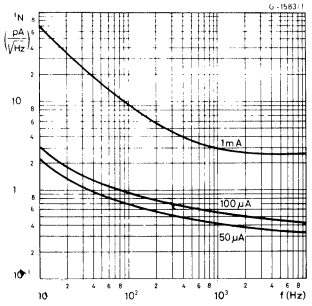


Fig. 3 - Equivalent input noise voltage vs. frequency (input transistor Q_1)

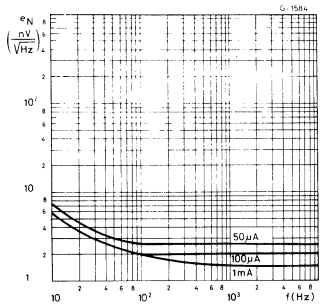


Fig. 4 - Noise figure vs. bias current (input transistor Q_1)

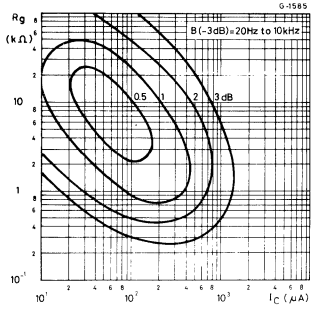


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (input transistor Q_1)

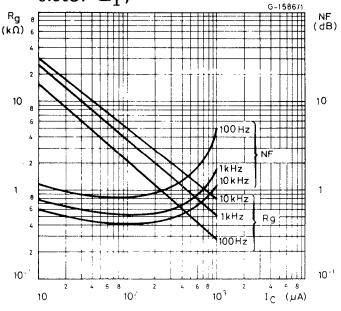


Fig. 6 - Current gain vs. collector current (input transistor Q_1)

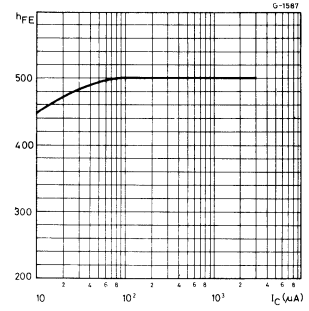


Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

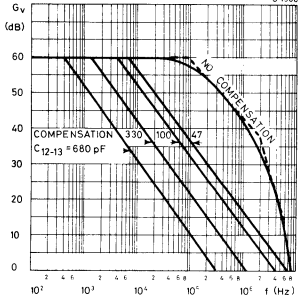
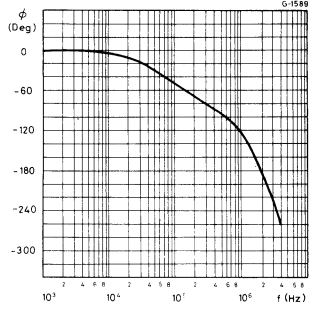


Fig. 8 - Open loop phase response vs. frequency (equalization amplifier)



APPLICATION INFORMATION

Fig. 9 - Application circuit for battery/mains cassette player and recorder

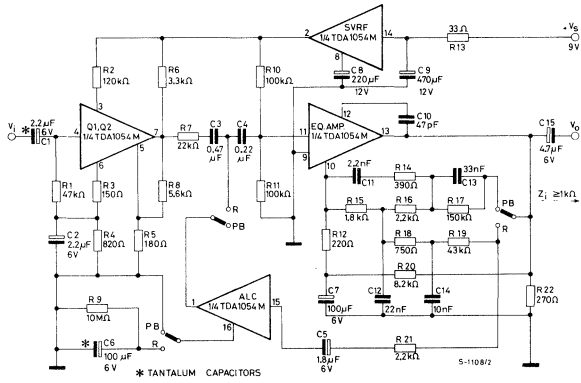
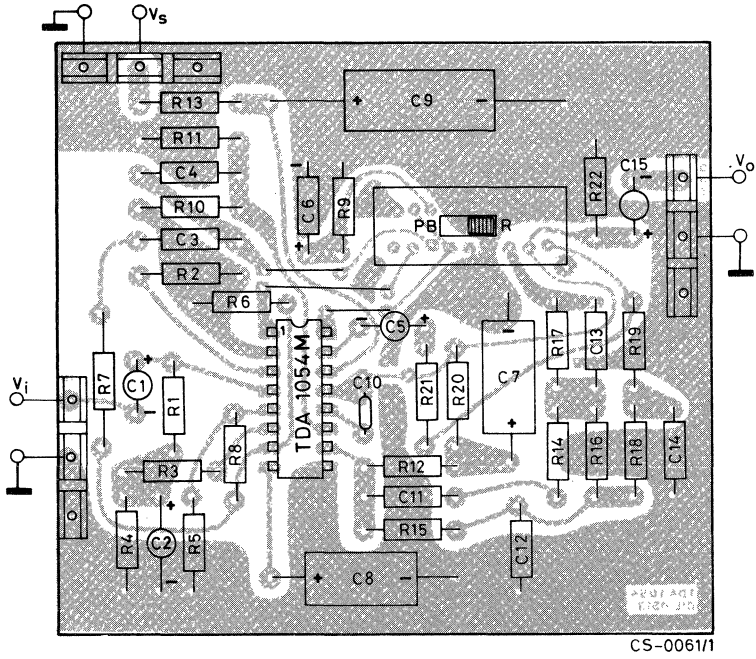


Fig. 10 - P.C. board and component layout for the circuit fig. 9 (1:1 scale)



Typical performance of circuit in fig. 9

(T_{amb} = 25°C, V_s = 9V)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK						
G_v	Voltage gain (open loop)	f = 20 to 20,000 Hz		110		dB
G_v	Voltage gain (closed loop)	f = 1 kHz		57		dB
$\|Z_i\|$	Input impedance	f = 100 Hz f = 1 kHz f = 10 kHz		10 41 43		kΩ kΩ kΩ
$\|Z_o\|$	Output impedance	f = 1 kHz		12	35	Ω
B	Frequency response			see fig. 12		
d	Distortion	V_o = 1V f = 1 kHz		0.1		%
	Output background noise	Z_g = 300 Ω + 120 mH (DIN 45405)		1.3		mV
***	Output weighted background noise			1.3		mV
$\frac{S+N}{N}$	Signal to noise ratio	V_o = 1.3V Z_g = 300 Ω + 120 mH		60		dB
SVR	Supply voltage ripple rejection at the output	f_{ripple} = 100 Hz		30		dB
t_{on}**	Switch-on time	V_o = 1V		500		ms
RECORDING						
G_v	Voltage gain (open loop)	f = 20 to 20,000 Hz		110		dB
G_v	Voltage gain (closed loop)	f = 1 kHz		70		dB
B	Frequency response			see fig. 14		
d*	Distortion without ALC	V_o = 1.1V f = 1 kHz		0.3		%
d	Distortion with ALC	V_o = 1.1V f = 10 kHz		0.4		%
ALC	Automatic level control range (for 3 dB of output voltage variation)	$V_i \leqslant$ 40 mV f = 10 kHz		54		dB
V_o	Output voltage before clipping without ALC	f = 1 kHz		2.3		V
V_o	Output voltage with ALC	V_i = 30 mV f = 10 kHz		1.1		V

Typical performance of circuit in fig. 9 (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_l **	Limiting time (see fig. 11)	ΔV_i = +40 dB f = 1 kHz		75		ms
t_{set} **	Level setting time (see fig. 11)			300		ms
t_{rec} **	Recovery time (see fig. 11)	ΔV_i = -40 dB f = 1 kHz		150		s
t_{on} **	Switch-on time	V_o = 1.1V		500		ms
$\frac{S+N}{N}$ ****	Signal to noise ratio with ALC	V_o = 1.1V R_g = 470 Ω		64		dB

* Measured with selective voltmeter
** This value depends on external network
*** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 10 kHz can be avoided – so halving the output noise
**** Weighted noise measurement (DIN 45405)

Fig. 11 - Limiting, level setting, recovery time

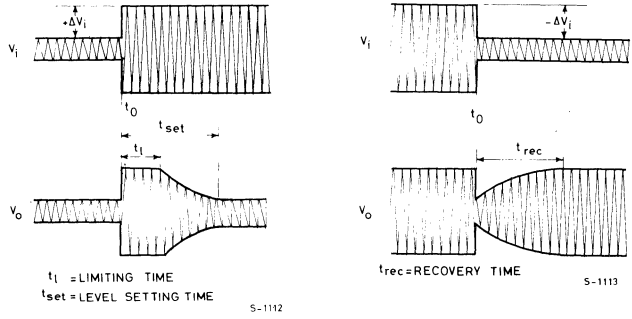


Fig. 12 - Relative frequency response for the circuit in fig. 9 (playback)

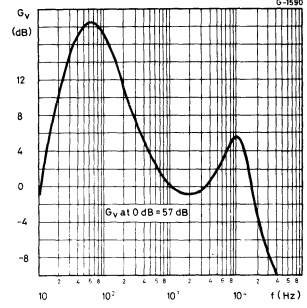


Fig. 13 - Distortion vs. frequency for the circuit in fig. 9 (playback)

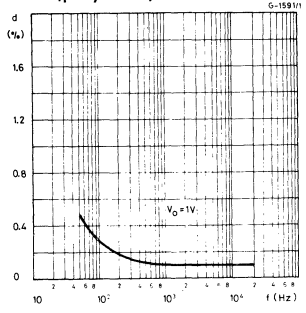


Fig. 14 - Relative frequency response for the circuit in fig. 9 (recording)

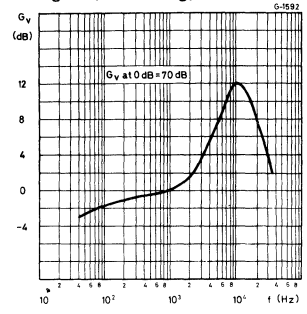


Fig. 15 - Output voltage variation and distortion with ALC vs. input voltage for the circuit in fig. 9 (recording)

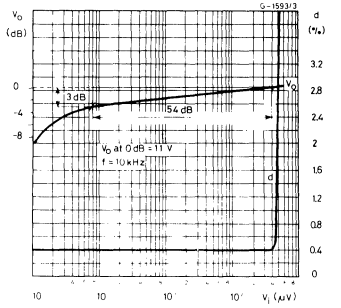


Fig. 16 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

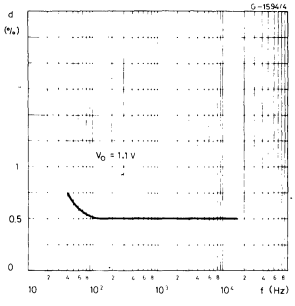


Fig. 17 - Limiting and level setting time vs. input signal variation

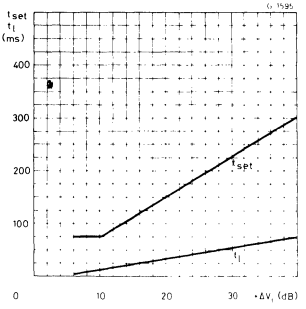


Fig. 18 - Low cost application circuit

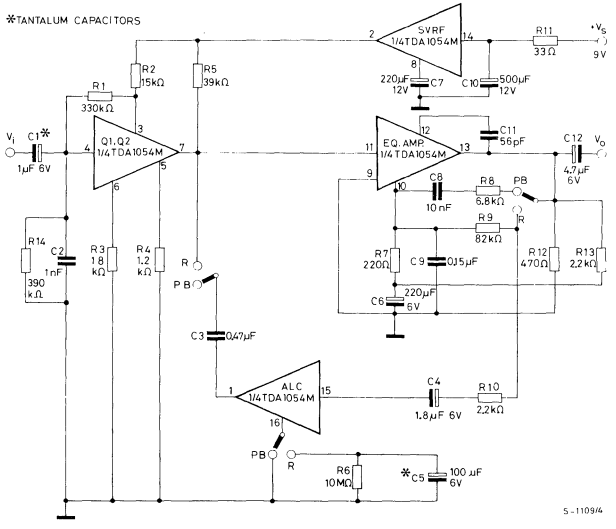
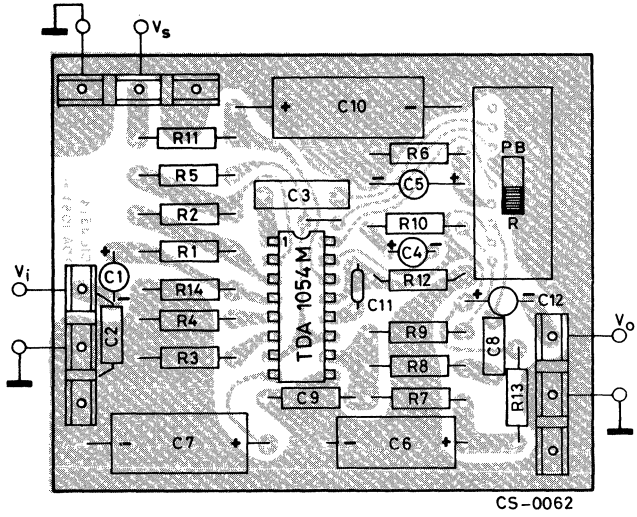


Fig. 19 - P.C. board and component layout for the circuit in fig. 18 (1:1 scale)



Typical performance of circuit in fig. 18

(T_{amb} = 25°C, V_s = 9V)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK						
V_s	Supply voltage		5		12	V
I_d	Quiescent drain current			18		mA
G_v	Voltage gain (closed loop)	f = 1 kHz		54		dB
B	Frequency response	f = 100 Hz f = 1 kHz f = 6 kHz f = 10 kHz f = 60 kHz		12 0 5 11 10		dB dB dB dB dB
d	Distortion	V_o = 1V f = 1 kHz		0.6		%
e_N	Output weighted background noise	Z_g = 300 Ω + 120 mH (DIN 45405)		1.3		mV

Typical performance of circuit in fig. 18 (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
RECORDING						
G_v	Voltage gain (closed loop)	f = 1 kHz		70		dB
B	Frequency response	f = 140 Hz f = 1 kHz f = 10 kHz		-3 0 4		dB dB dB
d	Distortion	V_o = 1.1V f = 10 kHz		0.7		%
ALC	Range for 3 dB of output voltage variation	$V_i \leq$ 40 mV f = 10 kHz		54		dB

Fig. 20 - Typical stereo application circuit for battery/mains cassette player and recorder

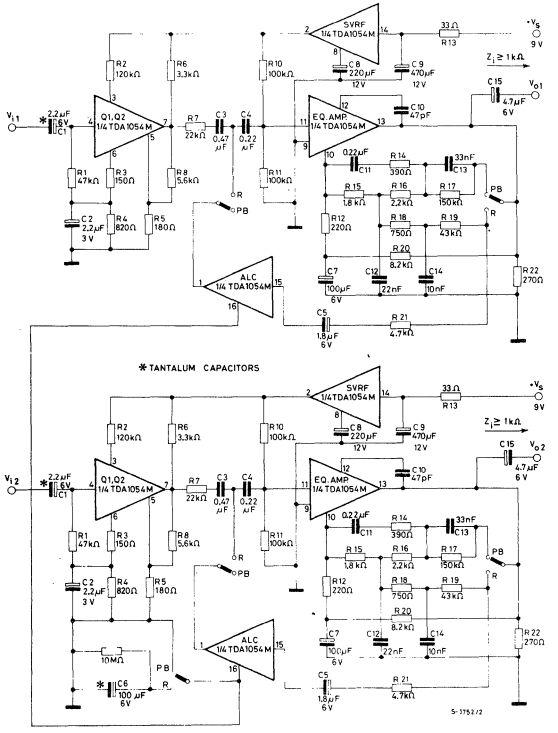


Fig. 21 - Complete cassette player and recorder

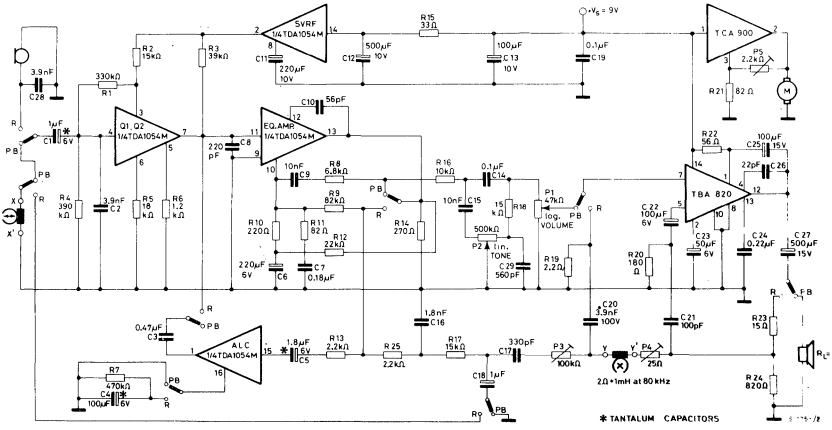
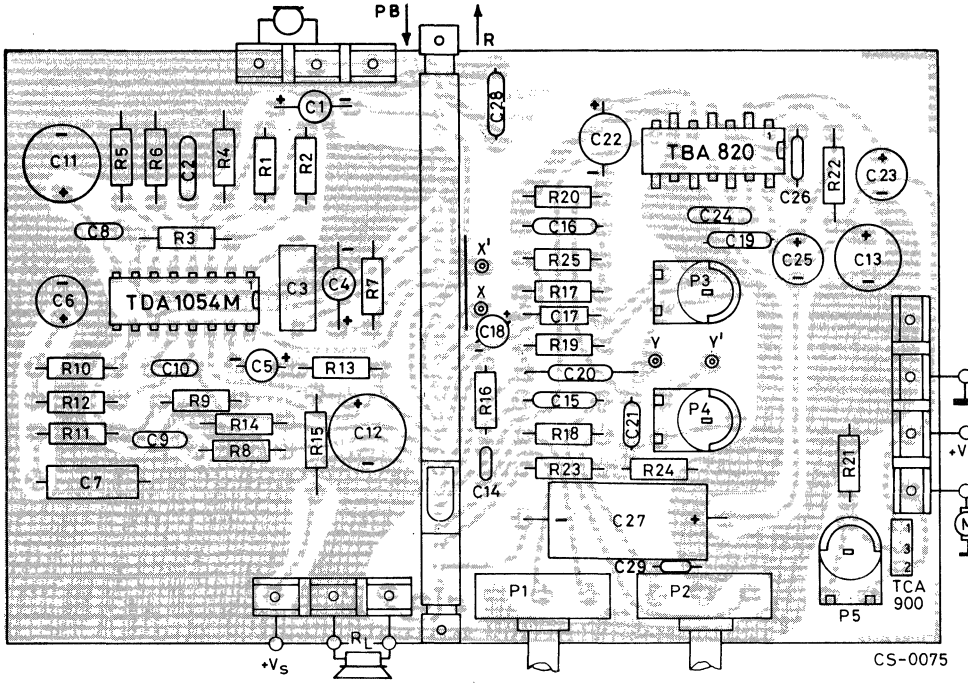


Fig. 22 - P.C. board and component layout for the circuit in fig. 21 (1:1 scale)



LINEAR INTEGRATED CIRCUIT

TDA1151

MOTOR SPEED REGULATOR

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (UP TO 800 mA)
- LOW QUIESCENT CURRENT (1.7 mA)
- LOW REFERENCE VOLTAGE (1.2V)
- EXCELLENT PARAMETERS STABILITY VERSUS TEMPERATURE

The TDA 1151 is a monolithic integrated circuit in Jedec TO-126 plastic package. It is intended for use as speed regulator for DC morors of record players, tape and cassette recorders, movie cameras, toys etc.

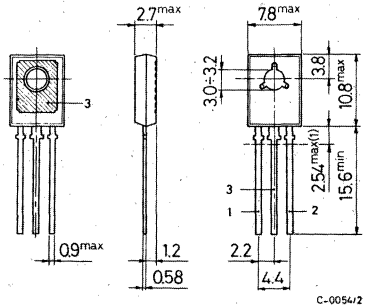
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 70°C	0.8	W
	at T_{case} = 100°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1151

MECHANICAL DATA

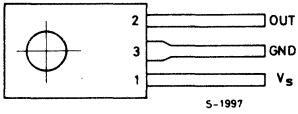
Dimensions in mm

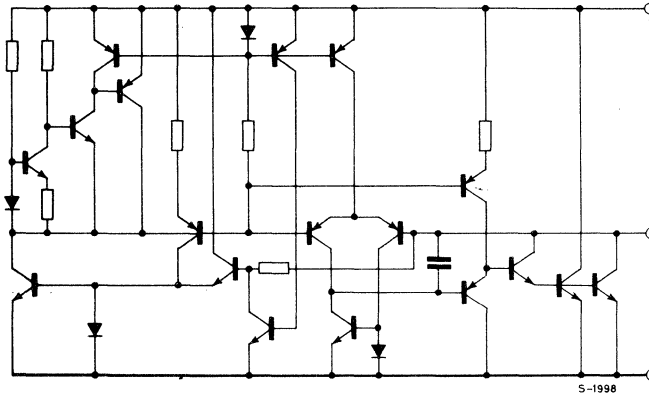


(1) Within this region the cross-section of the leads is uncontrolled

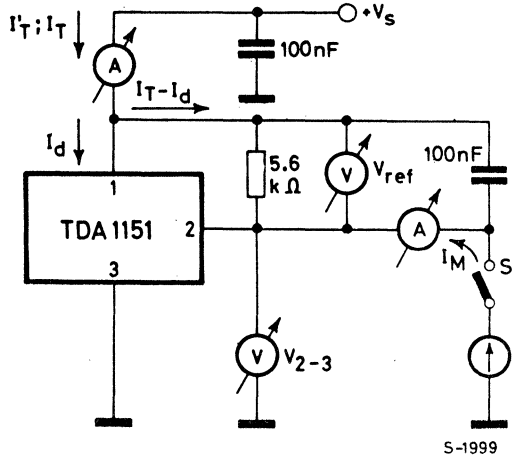
TO-126 (SOT 32)

CONNECTION AND SCHEMATIC DIAGRAMS





TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ref}	Reference voltage (between pins 1 and 2)	V_s = 6V I_M= 0.1A	1.1	1.2	1.3	V
I_d	Quiescent drain current	V_s = 6V I_M= 100 μA		1.7		mA
I_{MS}	Starting current	V_s = 5V $\Delta V_{ref}/V_{ref}$= -50%	0.8			A
V_{1-3}	Minimum supply voltage	I_M= 0.1A $\Delta V_{ref}/V_{ref}$= -5%			2.5	V
$K=I_M/I'_T$	Reflection coefficient	V_s = 6V I_M= 0.1A	18	20	22	—
$\frac{\Delta K}{K}/\Delta V_s$		V_s = 6V to 18V I_M= 0.1A		0.45		%/V
$\frac{\Delta K}{K}/\Delta I_M$		V_s = 6V I_M= 25 to 400 mA		0.005		%/mA
$\frac{\Delta K}{K}/\Delta T$		V_s = 6V I_M= 0.1A T_{amb}= -20 to 70°C		0.02		%/°C
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$	Line regulation	V_s = 6V to 18V I_M= 0.1A		0.02		%/V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$	Load regulation	V_s = 6V I_M= 25 to 400 mA		0.009		%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$	Temperature coefficient	V_s = 6V I_M= 0.1A T_{amb}= -20 to 70°C		0.02		%/°C

Fig. 1 - Quiescent drain current vs. power supply

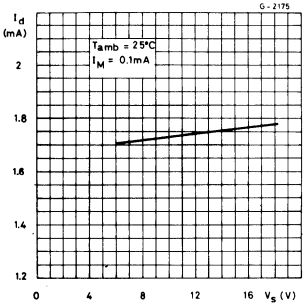


Fig. 2 - Quiescent drain current vs. ambient temperature

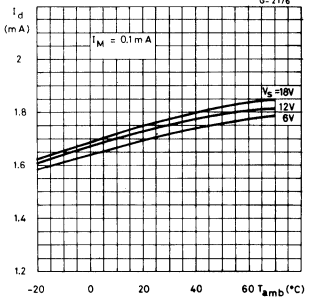


Fig. 3 - Reference voltage vs. supply voltage

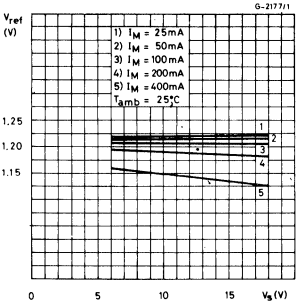


Fig. 4 - Reference voltage vs. motor current

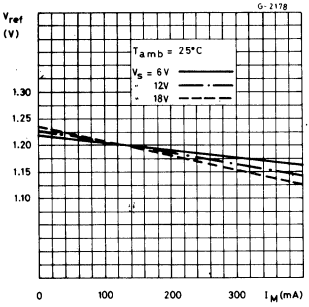


Fig. 5 - Reference voltage vs. ambient temperature

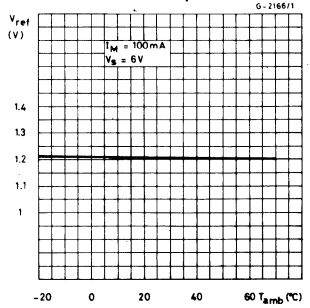


Fig. 6 - Reflection coefficient vs. supply voltage

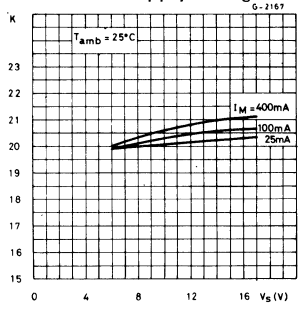


Fig. 7 - Reflection coefficient vs. motor current

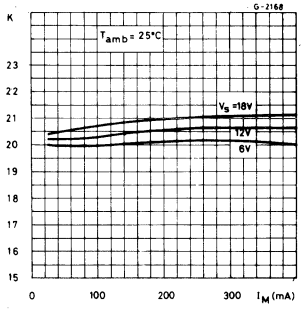


Fig. 8 - Reflection coefficient vs. ambient temperature

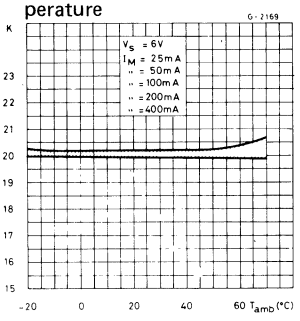
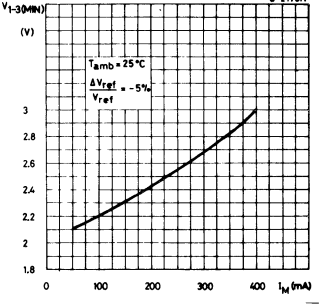
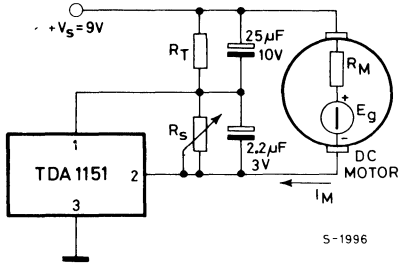


Fig. 9 - Typical minimum supply voltage vs. motor current



APPLICATION INFORMATION

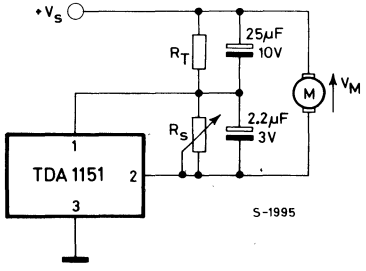


I_M = Motor current at rated speed
R_M = Motor resistance
E_g = Back electromotive force

$$R_{S\ min} = \frac{V_{ref} \cdot R_T}{E_g - (V_{ref} - I_d \cdot R_T)}$$

$R_T = K \cdot R_M$
$R_T = K_{typ} \cdot R_{M\ typ}$
If $R_{T\ max} > KR_{M\ min}$ instability may occur

Application circuit



V_s = +9V
R_M = 14.2Ω
R_T = 280Ω
R_S = 1 kΩ
E_g = 2.9V
I_M = 150 mA
$V_M = R_M \cdot I_M + E_g = 5.03V$

Note: A ceramic capacitor of 10 nF between pins, 1 and 2 improves stability in some applications.

Fig. 10 - Speed variation vs. supply voltage

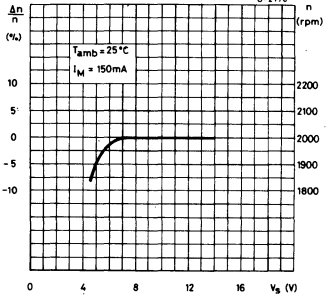


Fig. 11 - Speed variation vs. motor current

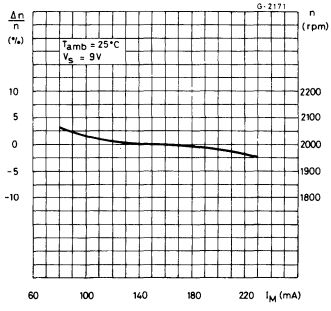
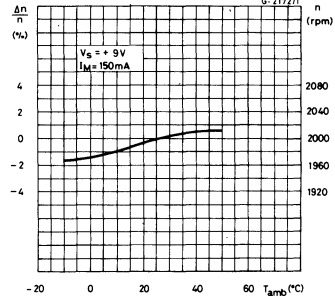
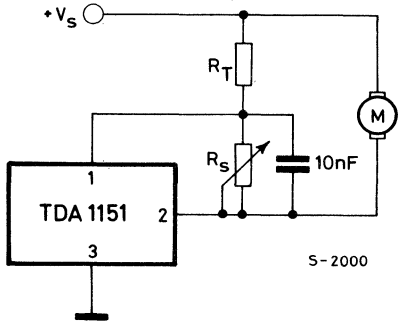


Fig. 12 - Speed variation vs. ambient temperature



APPLICATION INFORMATION (continued)

Low cost application circuit



V_S = +12V
R_M = 14.7Ω
R_T = 290Ω
R_S = 1 kΩ
E_g = 2.65V
I_M = 110 mA

Fig. 13 - Speed variation vs. supply voltage

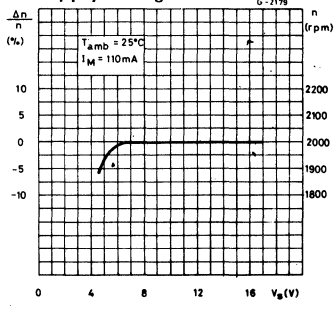


Fig. 14 - Speed variation vs. motor current

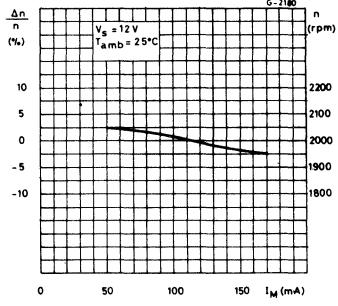
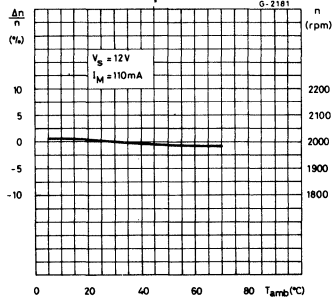


Fig. 15 - Speed variation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA1170

TV VERTICAL DEFLECTION SYSTEM

The TDA 1170 is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is designed mainly for use in large and small screen black and white TV receivers.
The functions incorporated are:

- oscillator
- voltage ramp generator
- high power gain amplifier
- flyback generator

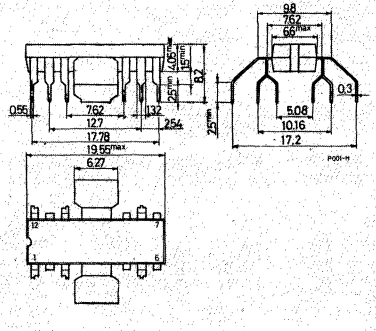
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 2)	27	V
V_4-V_5	Flyback peak voltage	58	V
V_8	Sync. input voltage	± 12	V
V_{10}	Power amplifier input voltage	10	V
		-0.5	V
I_o	Output peak current (non-repetitive) @ t = 2 ms	2	A
I_o	Output peak current @ f = 50 Hz, t ⩽ 10 μs	2.5	A
	@ f = 50 Hz, t > 10 μs	1.5	A
P_{tot}	Power dissipation: at T_{tab} = 90°C	5	W
	at T_{amb} = 80°C (free air)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1170

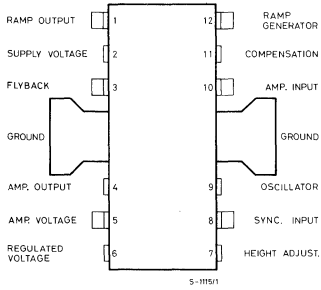
MECHANICAL DATA

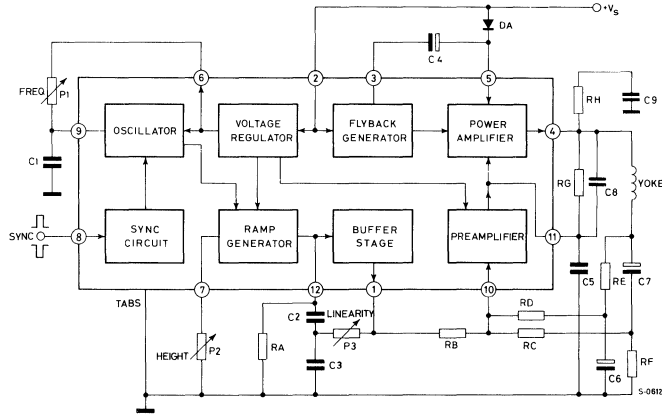
Dimensions in mm



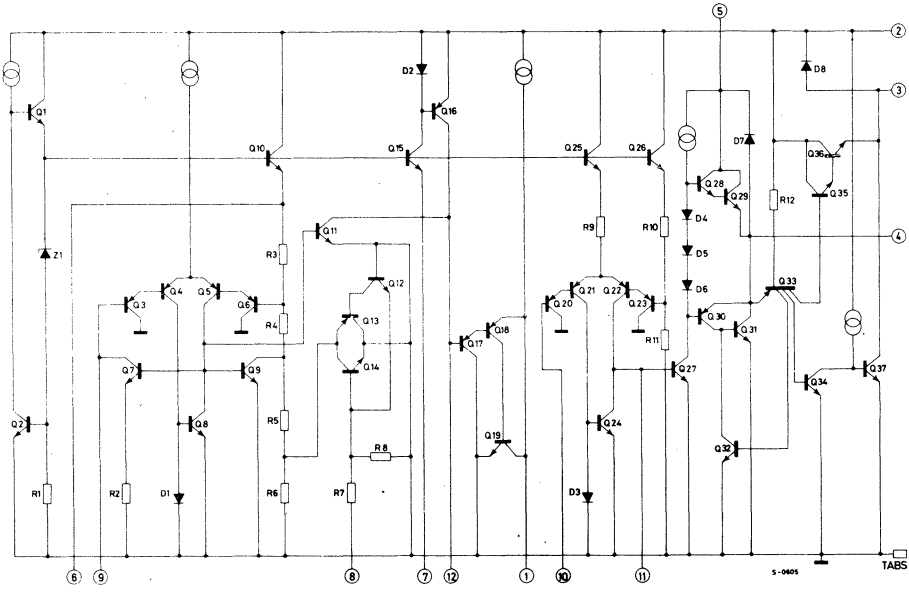
TDA1170

CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 25V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
$-I_9$	Oscillator bias current	V_9 = 1V		0.2	1	μA	1a
$-I_{10}$	Amplifier input bias current	V_{10}= 1V		0.15	1	μA	1b
$-I_{12}$	Ramp generator bias current			0.05	0.5	μA	1a
V_s	Supply voltage		10			V	–
V_4	Quiescent output voltage	R2 = 10 kΩ V_s = 25V R1 = 30 kΩ V_s = 10V R1 = 10 kΩ	 8 4	 8.8 4.4	 9.6 4.8	 V V	1a
V_6, V_7	Regulated voltage		6	6.5	7	V	1b
$\frac{\Delta V_6}{\Delta V_s}$ $\frac{\Delta V_7}{\Delta V_s}$	Line regulation	V_s = 10 to 27V		1.5		mV/V	
AC CHARACTERISTICS (f = 50 Hz)							
I_s	Supply current	I_Y = 1A		140		mA	2
I_Y	Peak to peak yoke current (pin 4)				1.6	A	
V_4	Flyback voltage	I_Y = 1A		51		V	
V_8	Peak sync. input voltage (positive or negative)		1			V	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
V_9	Peak to peak oscillator sawtooth voltage			2.4		V	2
R_8	Sync. input resistance	V_8 = 1V		3.5		kΩ	
t_{fly}	Flyback time	I_Y = 1A		0.6	0.8	ms	
δf	Pull-in range (below 50 Hz)			7		Hz	
$\frac{\delta f}{\Delta V_s}$	Oscillator frequency drift with supply voltage	V_s = 10 to 27V		0.01		$\frac{Hz}{V}$	
$\frac{\delta f}{\Delta T_{tab}}$	Oscillator frequency drift with tab temperature	T_{tab}= 40 to 120 °C		0.015		$\frac{Hz}{°C}$	

Fig. 1a - DC test circuit for measurement of $-I_9$, $-I_{12}$ and V_4

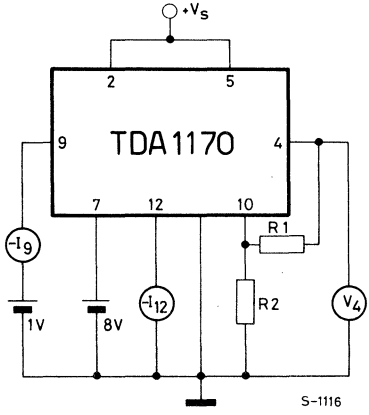


Fig. 1b - DC test circuit for measurement of $-I_{10}$, V_6, V_7, $\Delta V_6/\Delta V_s$ and $\Delta V_7/\Delta V_s$

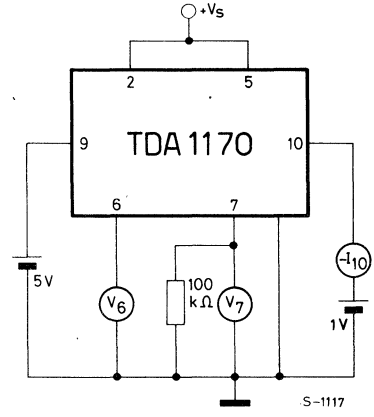


Fig. 2 - AC test circuit

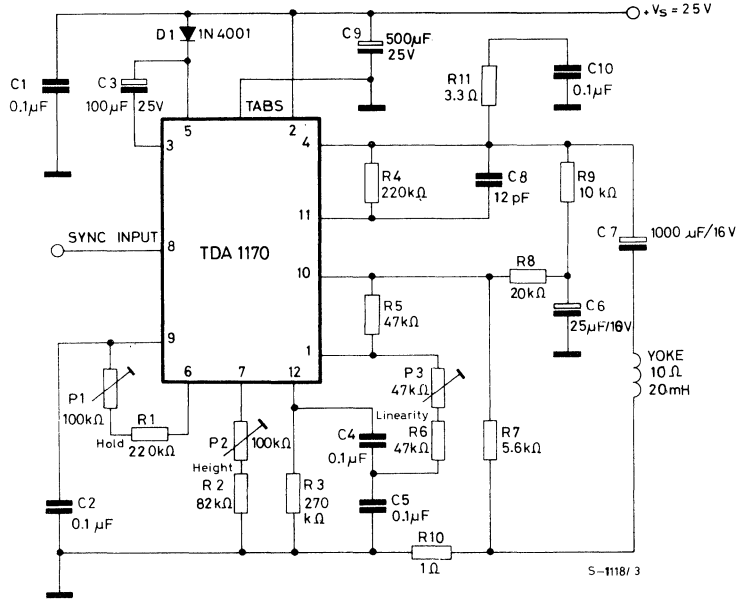


Fig. 3 - Relative quiescent voltage variation vs. supply voltage

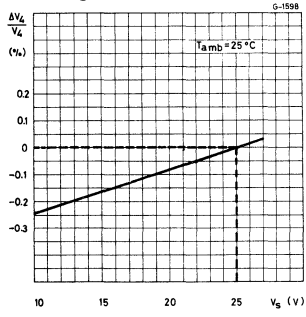


Fig. 4 - Relative quiescent voltage variation vs. tab temperature

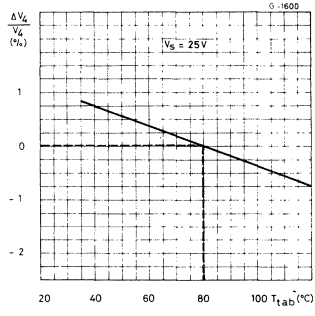


Fig. 5 - Regulated voltage vs. supply voltage

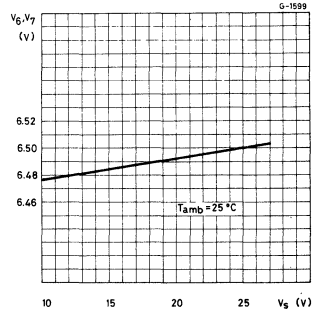


Fig. 6 - Regulated voltage vs. tab temperature

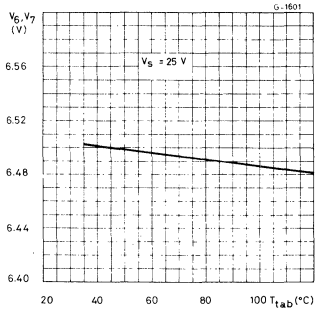


Fig. 7 - Frequency variation of unsynchronized oscillator vs. supply voltage

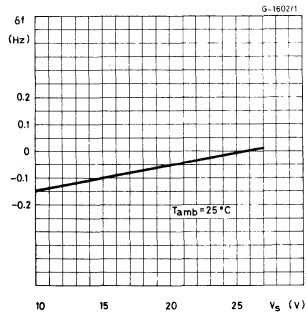
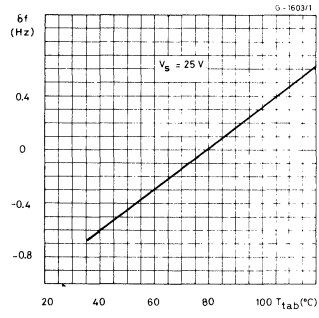


Fig. 8 - Frequency variation of unsynchronized oscillator vs. tab temperature



APPLICATION INFORMATION

The thermistor in series to the yoke is not required because the current feedback enables the yoke current to be independent of yoke resistance variations due to thermal effects. The oscillator is directly synchonized by the sync. pulses (positive or negative), therefore its free frequency must be lower than the sync. frequency. The flyback generator applies a voltage, about twice the supply voltage, to the yoke. This produces short flyback time together with a high useful power to dissipated power ratio.

The flyback time is:

$$t_{fly} \cong \frac{2}{3} \frac{L_Y I_Y}{V_s}$$

where: L_Y = Yoke inductance
V_s = Supply voltage
I_Y = Peak to peak yoke current

The supply current is:

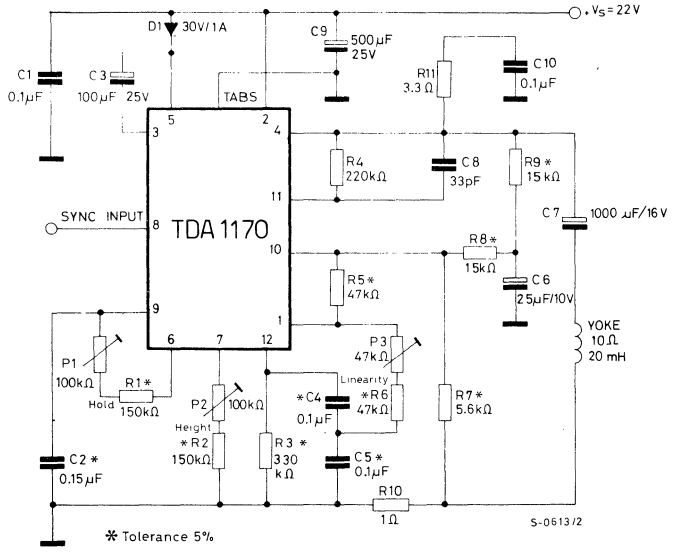
$$I_s \cong \frac{I_Y}{8} + 0.02 \text{ (A)}$$

It does not depend on the value of V_s but only on yoke characteristics. The minimum value of V_s necessary for the required output current permits the maximum efficiency.
The quiescent output voltage (pin 4) is fixed by the voltage feedback network R7, R8 and R9 (refer to fig. 2) according to:

$$V_4 = V_{10} \frac{R7 + R8 + R9}{R7}$$

Pin 10 is the inverting input of the amplifier and its voltage is $V_{10} \cong 2V$.

Fig. 9 - Typical application circuit for B & W 24" 110° TV sets

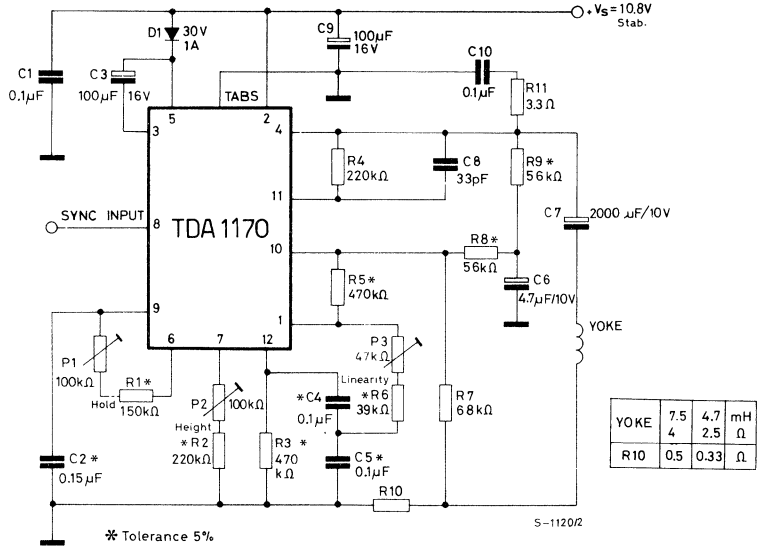


Typical performance (V_s = 22V; I_Y = 1A; R_Y = 10Ω; L_Y = 20 mH)

I_s	Supply current	140	mA
t_{fly}	Flyback time	0.75	ms
I_Y.	Maximum scanning current (peak to peak)	1.2	A
V_s	Operating supply voltage	20 to 24	V
P_{tot}	TDA 1170 power dissipation	2.2	W

For safe working up to T_{amb} = 50°C a heatsink of R_{th} = 40 °C/W is required and each tab of TDA 1170 must be soldered to 1 cm² copper area of the printed circuit board.

Fig. 10 - Typical application circuit for B & W small screen TV sets

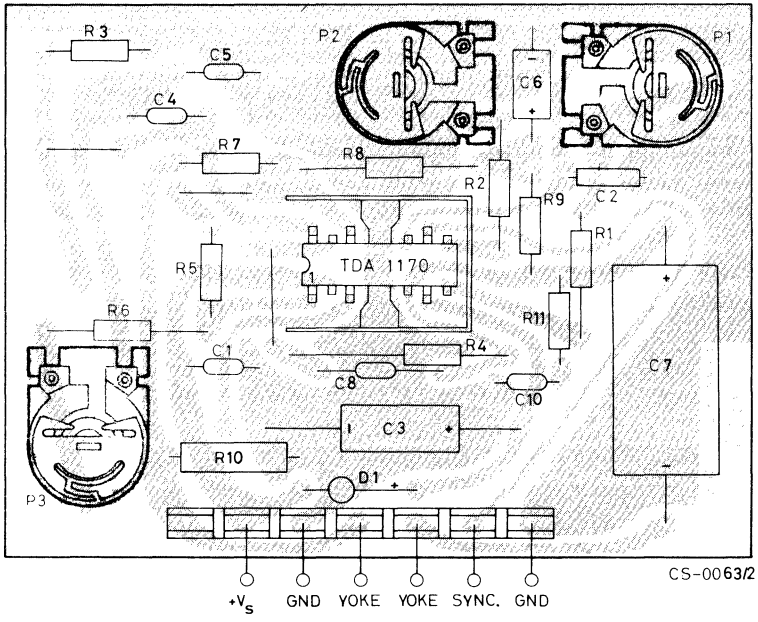


Typical performance (V_s = 10.8V; I_Y = 1A; R_Y = 4Ω; L_Y = 7.5 mH)

I_s	Supply current	150	mA
t_{fly}	Flyback time	0.7	ms
I_Y	Maximum scanning current (peak to peak)	1.15	A
V_s	Operating supply voltage	10.8	V
P_{tot}	TDA 1170 power dissipation	1.3	W

For safe working up to T_{amb} = 50°C a heatsink of R_{th} = 30 °C/W is required and each tab of the TDA 1170 must be soldereb to 1 cm² copper area of the printed circuit board.

Fig. 11 - P.C. board and component layout for the circuit of fig. 9 and fig. 10 (1:1 scale)



C9 is not mounted on the P.C. board.

MOUNTING INSTRUCTIONS

The junction to ambient thermal resistance of the TDA 1170 can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 12) or to an external heatsink (fig. 13).
The diagram of fig. 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "s" of two equal square copper areas having a thickness of 35 μ (1.4 mil).
During soldering the tab temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area used as heatsink

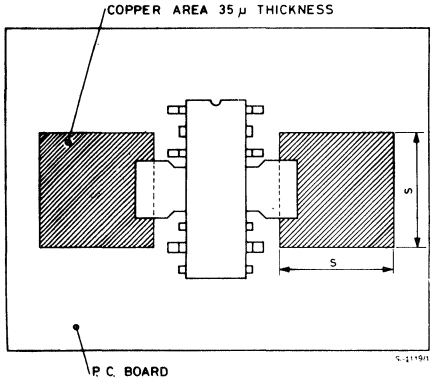


Fig. 13 - Example of TDA 1170 with external heatsink

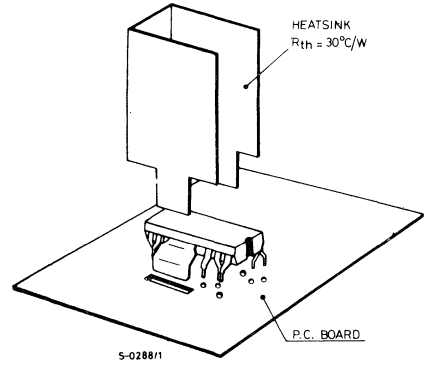


Fig. 14 - Maximum power dissipation and junction-ambient thermal resistance vs. "s"

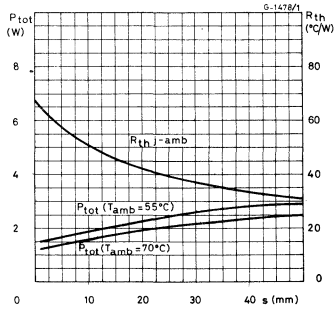
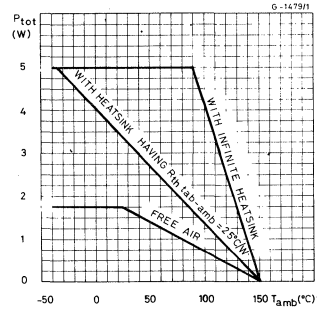


Fig. 15 - Maximum allowable power dissipation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA1170D

LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

The TDA 1170D is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise meakes this device particularly suitable for use in monitors.** The functions incorporated are:

- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- flyback generator
- voltage regulator

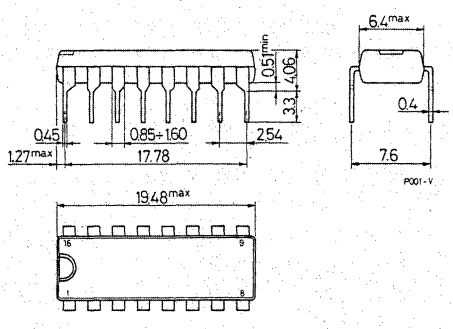
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage at pin 2	35	V
V6, V7	Flyback peak voltage	60	V
V14	Power amplifier input voltage	+ 10	V
		- 0.5	V
I_o	Output peak current (non repetitive) at t = 2 msec	2	A
I_o	Output peak current at f = 50 Hz t $\leqslant$ 10 μsec	2.5	A
I_o	Output prak current at f = 50 Hz t $>$ 10 μsec	1.5	A
I_3	Pin 3 DC current at V6 $<$ V2	100	mA
I_3	Pin 3 peak to peak flyback current for f = 50 Hz, $t_{fly} \leqslant$ 1.5 msec	1.8	A
I_{10}	Pin 10 current	± 20	mA
P_{tot}	Power dissipation: at T_{tab} = 90°C	4.3	W
	at T_{amb} = 70°C (free air)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1170D

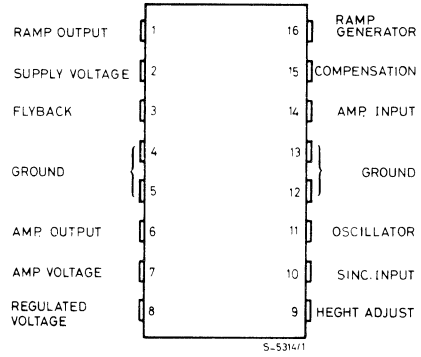
MECHANICAL DATA

. Dimensions in mm

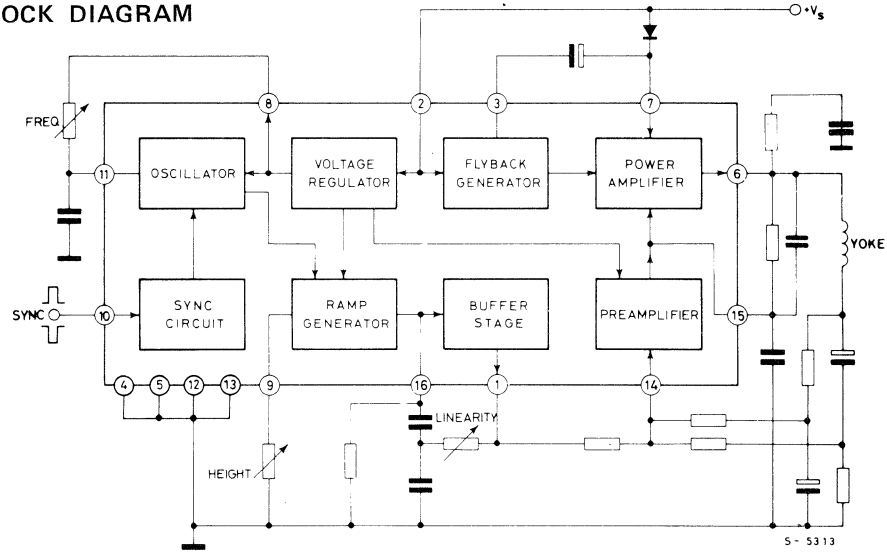


TDA1170D

CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-pins	max	14 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80 °C/W (◦)

(◦) Obtained with pins 4, 5, 12, 13 soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 35V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
I_2	Pin 2 quiescent current	I_3 = 0		7	14	mA	1b
I_7	Pin 7 quiescent current	I_4 = 0		8	15	mA	1b
$-I_{11}$	Oscillator bias current	V11= 1V		0.1	1	μA	1a
$-I_{12}$	Amplifier input bias current	V12= 1V		1	7	μA	1b
$-I_{16}$	Ramp generator bias current	V16= 0		0.02	0.3	μA	1a
$-I_{16}$	Ramp generator current	I_7 = 20 μA V16= 0	19	20	24	μA	1b
$\frac{\Delta I_{16}}{I_{16}}$	Ramp generator non-linearity	ΔV16= 0 to 12V I_9 = 20 μA		0.2	1	%	1b
V_s	Supply voltage range		10		35	V	–
V1	Pin 1 saturation voltage to ground	I_1 = 1 mA		1	1.4	V	–
V3	Pin 3 saturation voltage to ground	I_3 = 10 mA		1.7	2.6	V	1a
V6	Quiescent output voltage	V_s= 10V R1= 10 KΩ R2 = 10 KΩ	4.17	4.4	4.63	V	1a
		V_s= 35V R1= 30 KΩ R2 = 10 KΩ	8.35	8.8	9.25	V	1a
V6L	Output saturation voltage to ground	$-I_6$= 0.1A		0.9	1.2	V	1c
		$-I_6$= 0.8A		1.9	2.3	V	1c
V6H	Output saturation voltage to supply	I_6= 0.1A		1.4	2.1	V	1d
		I_6= 0.8A		2.8	3.2	V	1d
V8	Regulated voltage at pin 6		6.1	6.5	6.9	V	1b
V9	Regulated voltage at pin 7	I_9= 20 μA	6.2	6.6	7	V	1b
$\frac{\Delta V8}{\Delta V_s}$; $\frac{\Delta V9}{\Delta V_s}$	Regulated voltage drift with supply voltage	ΔV_s= 10 to 35V		1		mV/V	1b
V14	Amplifier input reference voltage		2.07	2 2	2.3	V	--
R10	Pin 10 input resistance	V10 ⩽ 0.4V	1			MΩ	1a

Fig. 1 - DC test circuit

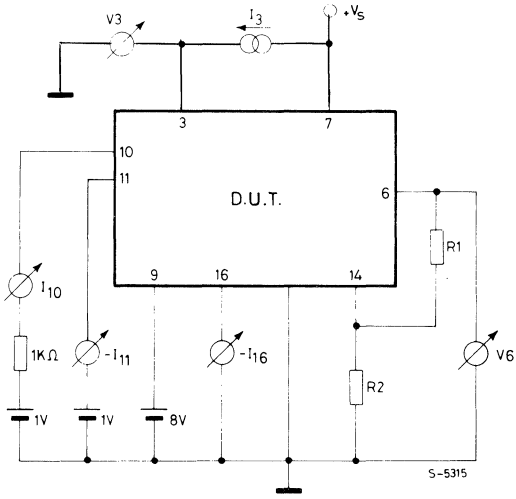


Fig. 1a

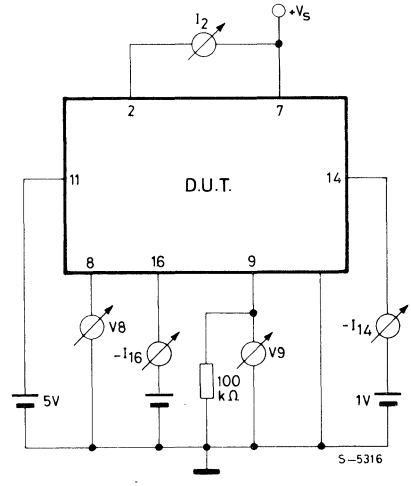


Fig. 1b

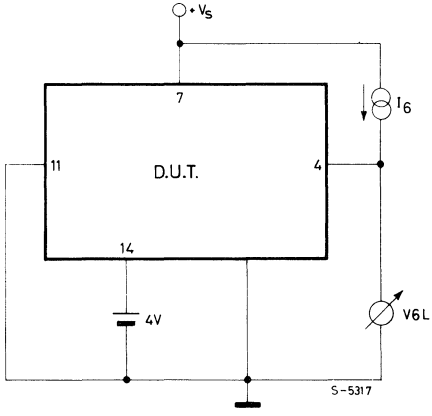


Fig. 1c

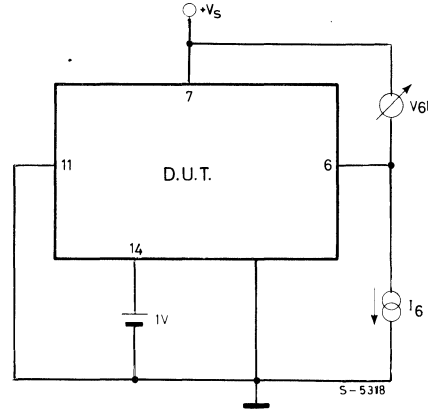


Fig. 1d

ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit, V_s = 25V; f = 50 Hz; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
I_s	Supply current	I_y = 1 App		140		mA
I_{10}	Sync. input current (positive or negative)		500			μA
V6	Flyback voltage	I_y = 1 App		51		V
t_{fly}	Flyback time	I_y = 1 App		0.7		ms
V_{ON}	Peak to peak output noise	Bw= 20 ÷ 20.000 Hz			50	mV
f_o	Free running frequency	(P1 + R1) = 260 KΩ C2 = 0.1 μF		52.4		Hz
		(P1 + R1) = 300 KΩ C2 = 100 nF		43.7		Hz
Δf	Synchronization range	I_8 = 0.5 mA	14			Hz
$\frac{\Delta f}{\Delta V_s}$	Frequency drift with supply voltage	V_s = 10 to 35V		0.005		Hz/V
$\frac{\Delta f}{\Delta T_{pins}}$	Frequency drift vs. pins 4, 5, 12 and 13 temp.	T_{tab}= 40 to 120°C		0.01		Hz/°C

Fig. 2 - AC test circuit

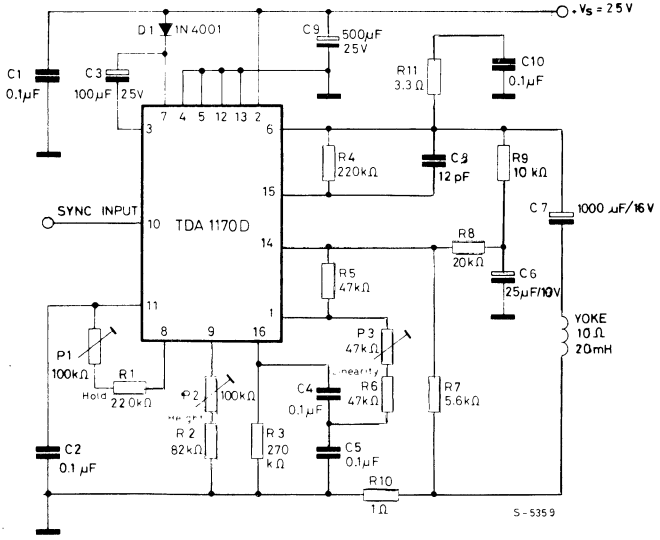
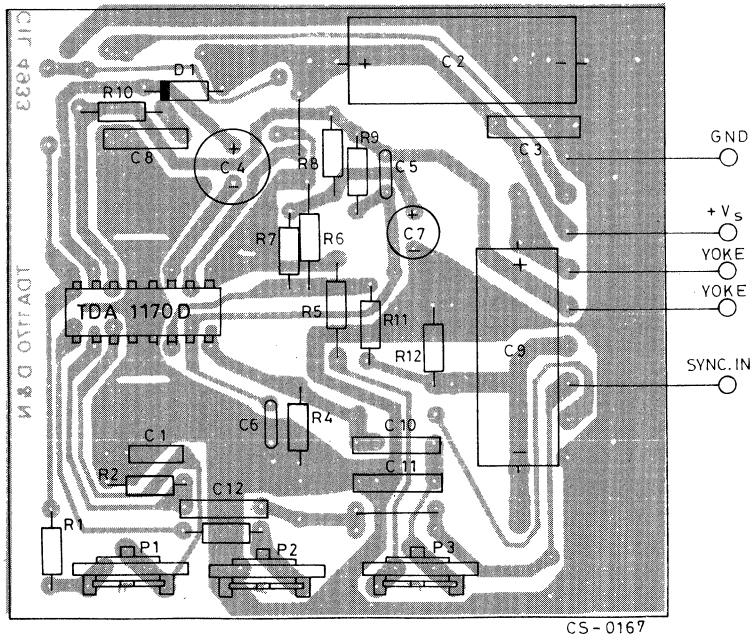


Fig. 3 - P.C. board and components layout of the AC test circuit.



LINEAR INTEGRATED CIRCUIT

TDA1170N

LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

The TDA 1170N is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise meakes this device particularly suitable for use in monitors.** The functions incorporated are:

- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- flyback generator
- voltage regulator

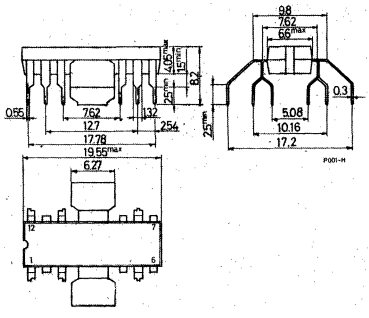
PRELIMINARY DATA

ABSOLUTE MAXIMUM RATINGS

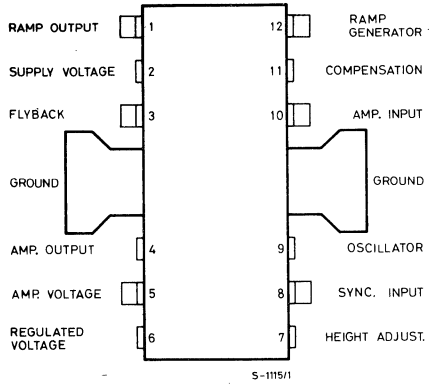
V_s	Supply voltage at pin 2	35	V
V4, V5	Flyback peak voltage	60	V
V10	Power amplifier input voltage	+ 10	V
		- 0.5	V
I_o	Output peak current (non repetitive) at t = 2 msec	2	A
I_o	Output peak current at f = 50 Hz t ⩽ 10 μsec	2.5	A
I_o	Output peak current at f = 50 Hz t > 10 μsec	1.5	A
I_3	Pin 3 DC current at V4 < V2	100	mA
I_3	Pin 3 peak to peak flyback current for f = 50 Hz, t_{fly} ⩽ 1.5 msec	1.8	A
I_8	Pin 8 current	± 20	mA
P_{tot}	Power dissipation: at T_{tab} = 90°C	5	W
	at T_{amb} = 80°C (free air)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

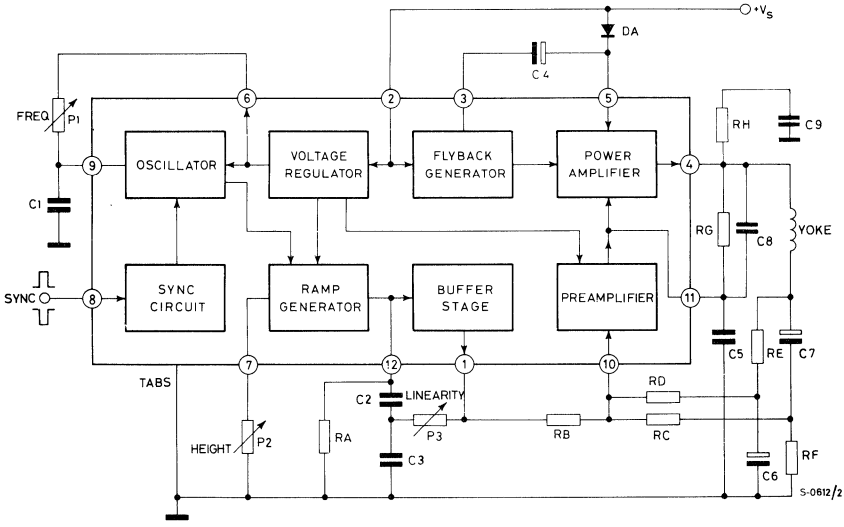
MECHANICAL DATA

Dimensions in mm



CONNECTION AND BLOCK DIAGRAMS





THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W(°)

(°) Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 35V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
I_2	Pin 2 quiescent current	I_3 = 0		7	14	mA	1b
I_5	Pin 5 quiescent current	I_4 = 0		8	15	mA	1b
$-I_9$	Oscillator bias current	V9 = 1V		0.1	1	μA	1a
$-I_{10}$	Amplifier input bias current	V10= 1V		1	7	μA	1b
$-I_{12}$	Ramp generator bias current	V12= 0		0.02	0.3	μA	1a
$-I_{12}$	Ramp generator current	I_7 = 20 μA V12= 0	19	20	24	μA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp generator non-linearity	ΔV12= 0 to 12V I_7 = 20 μA		0.2	1	%	1b
V_s	Supply voltage range		10		35	V	–
V1	Pin 1 saturation voltage to ground	I_1 = 1 mA		1	1.4	V	–
V3	Pin 3 saturation voltage to ground	I_3 = 10 mA		1.7	2.6	V	1a
V4	Quiescent output voltage	V_s= 10V R1= 10 KΩ R2 = 10 KΩ	4.17	4.4	4.63	V	1a
		V_s= 35V R1= 30 KΩ R2 = 10 KΩ	8.35	8.8	9.25	V	1a
V4L	Output saturation voltage to ground	$-I_4$= 0.1A		0.9	1.2	V	1c
		$-I_4$= 0.8A		1.9	2.3	V	1c
V4H	Output saturation voltage to supply	I_4 = 0.1A		1.4	2.1	V	1d
		I_4 = 0.8A		2.8	3.2	V	1d
V6	Regulated voltage at pin 6		6.1	6.5	6.9	V	1b
V7	Regulated voltage at pin 7	I_7 = 20 μA	6.2	6.6	7	V	1b
$\frac{\Delta V6}{\Delta V_s}$; $\frac{\Delta V7}{\Delta V_s}$	Regulated voltage drift with supply voltage	ΔV_s= 10 to 35V		1		mV/V	1b
V10	Amplifier input reference voltage		2.07	2.2	2.3	V	–
R8	Pin 8 input resistance	V8 ⩽ 0.4V	1			MΩ	1a

Fig. 1 - DC test circuits

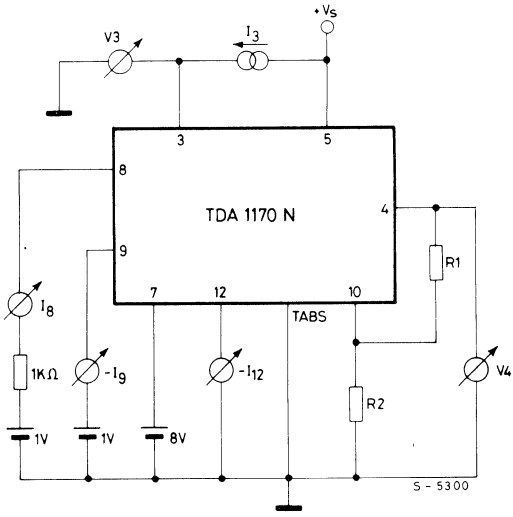


Fig. 1a

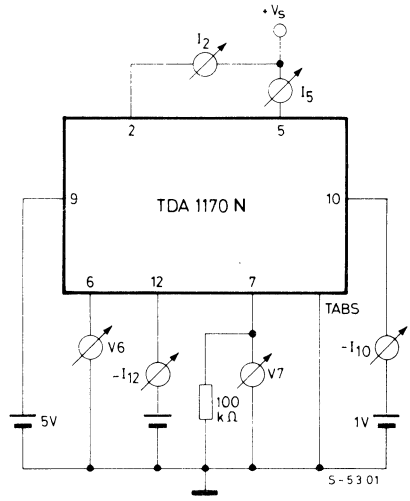


Fig. 1b

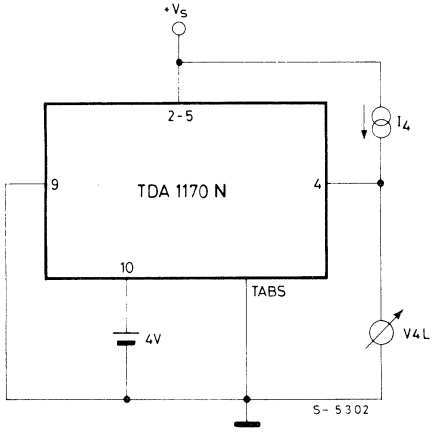


Fig. 1c

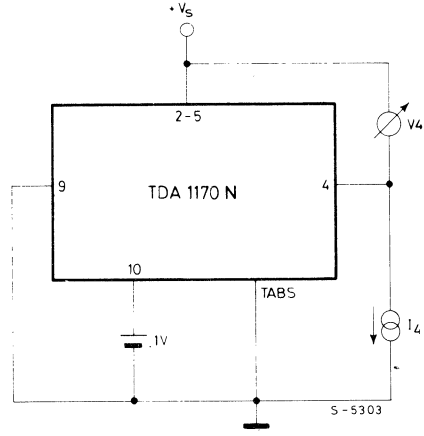


Fig. 1d

ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit, V_S = 25V; f = 50 Hz; T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
I_s	Supply current	I_y = 1 App		140		mA
I_8	Sync. input current (positive or negative)		500			μA
V4	Flyback voltage	I_y = 1 App		51		V
t_{fly}	Flyback time	I_y = 1 App		0.7		ms
V_{oN}	Peak to peak output noise	Bw = 20 ÷ 20.000 Hz			50	mV
f_o	Free running frequency	(P1 + R1) = 300 KΩ C2 = 0.1 μF		52.4		Hz
		(P1 + R1) = 360 KΩ C2 = 100 nF		43.7		Hz
Δf	Synchronization range	I_8 = 0.5 mA	14			Hz
$\frac{\Delta f}{\Delta V_s}$	Frequency drift with supply voltage	V_s = 10 to 35V		0.005		Hz/V
$\left\lvert\frac{\Delta f}{\Delta T_{tab}}\right\rvert$	Frequency drift with tab temperature	T_{tab} = 40 to 120°C		0.01		Hz/°C

Fig. 2 - AC test circuit

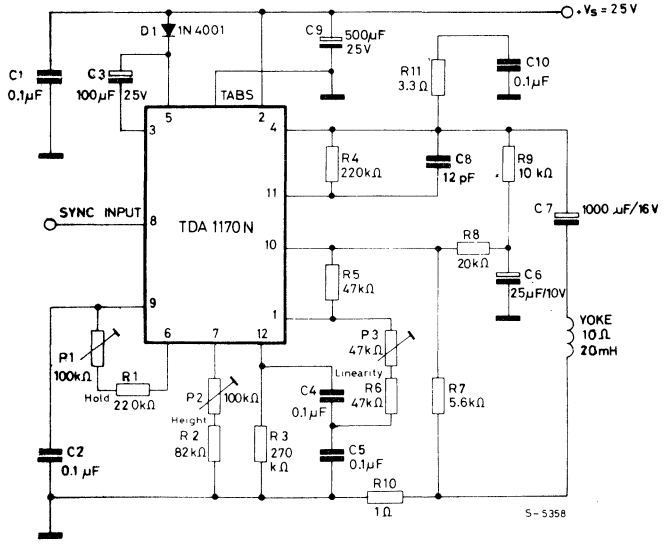
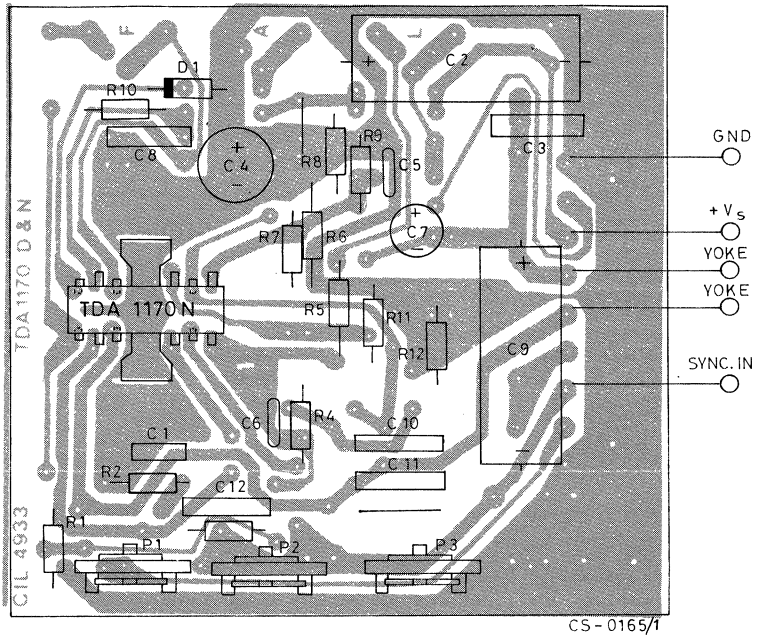


Fig. 3 - PC board and component layout of the AC test circuit (1:1 scale)



LINEAR INTEGRATED CIRCUIT

TDA1170S

TV VERTICAL DEFLECTION SYSTEM

The TDA 1170S is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers.
The functions incorporated are:

- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- flyback generator
- voltage regulator

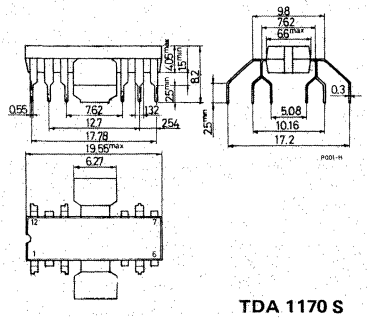
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage at pin 2	35	V
V_4, V_5	Flyback peak voltage	60	V
V_{10}	Power amplifier input voltage	+ 10	V
		- 0.5	V
I_o	Output peak current (non repetitive) at t = 2 msec	2	A
I_o	Output peak current at f = 50 Hz $t \leqslant 10\ \mu$sec	2.5	A
I_o	Output peak current at f = 50 Hz $t > 10\ \mu$sec	1.5	A
I_3	Pin 3 DC current at $V_4 < V_2$	100	mA
I_3	Pin 3 peak to peak flyback current for f = 50 Hz, $t_{fly} \leqslant 1.5$ msec	1.8	A
I_8	Pin 8 current	± 20	mA
P_{tot}	Power dissipation: at T_{tab} = 90°C, at T_{amb} = 80°C — TDA1170S	5	W
		1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

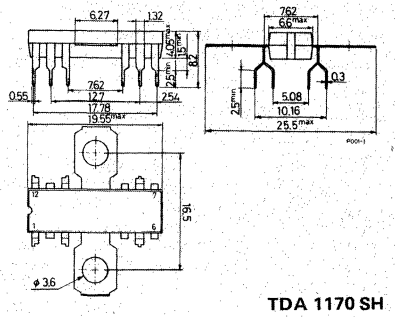
ORDERING NUMBERS: TDA 1170 S
TDA 1170 SH

MECHANICAL DATA

Dimensions in mm



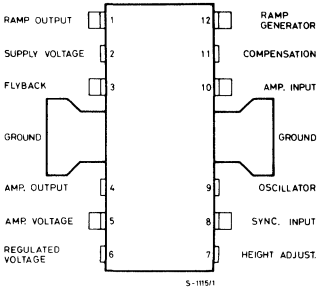
TDA 1170 S

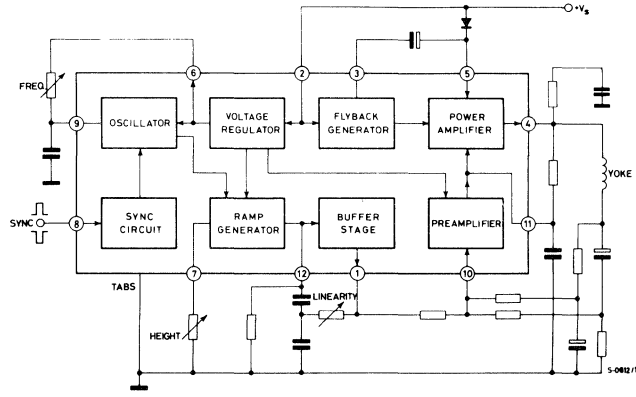


TDA 1170 SH

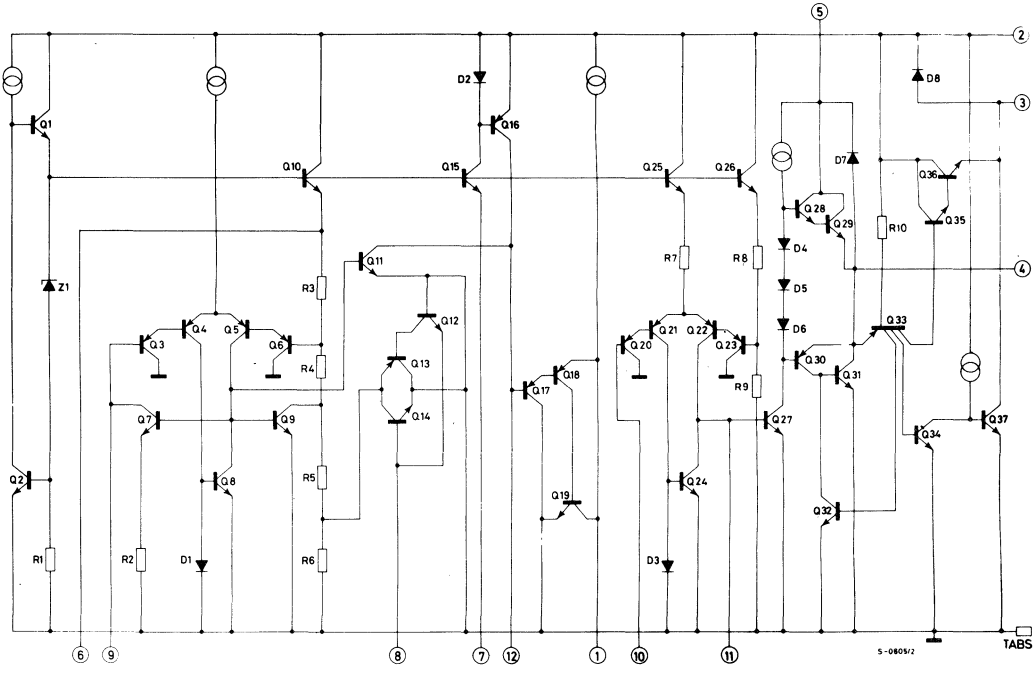
TDA1170S

CONNECTION AND BLOCK DIAGRAMS





SCHEMATIC DIAGRAM



THERMAL DATA

		TDA 1170S	TDA 1170SH
$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max 12°C/W	max 10°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max 70°C/W(°)	max 80°C/W

(°) Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s= 35V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
I_2	Pin 2 quiescent current	I_3 = 0		7	14	mA	1b
I_5	Pin 5 quiescent current	I_4 = 0		8	15	mA	1b
$-I_9$	Oscillator bias current	V_9 = 1V		0.1	1	μA	1a
$-I_{10}$	Amplifier input bias current	V_{10}= 1V		0.1	1	μA	1b
$-I_{12}$	Ramp generator bias current	V_{12}= 0		0.02	0.3	μA	1a
$-I_{12}$	Ramp generator current	I_7 = 20 μA V_{12}= 0	19	20	24	μA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp generator non-linearity	ΔV_{12}= 0 to 12V I_7 = 20 μA		0.2	1	%	1b
V_s	Supply voltage range		10		36	V	–
V_1	Pin 1 saturation voltage to ground	I_1 = 1 mA		1	1.4	V	–
V_3	Pin 3 saturation voltage to ground	I_3 = 10 mA		1.7	2.6	V	1a
V_4	Quiescent output voltage	V_s= 10V R_1=10 KΩ R_2=10 KΩ	4.17	4.4	4.63	V	1a
		V_s= 35V R_1=30 KΩ R_2= 10 KΩ	8.35	8.8	9.25	V	1a
V_{4L}	Output saturation voltage to ground	$-I_4$ = 0.1A		0.9	1.2	V	1c
		$-I_4$ = 0.8A		1.9	2.3	V	1c
V_{4H}	Output saturation voltage to supply	I_4 = 0.1A		1.4	2.1	V	1d
		I_4 = 0.8A		2.8	3.2	V	1d
V_6	Regulated voltage at pin 6		6.1	6.5	6.9	V	1b
V_7	Regulated voltage at pin 7	I_7 = 20 μA	6.2	6.6	7	V	1b
$\frac{\Delta V_6}{\Delta V_s} \cdot \frac{\Delta V_7}{\Delta V_s}$	Regulated voltage drift with supply voltage	ΔV_s= 10 to 35V		1		mV/V	1b
V_{10}	Amplifier input reference voltage		2.07	2.2	2.3	V	–
R_8	Pin 8 input resistance	$V_8 \leq 0.4V$	1			MΩ	1a

Fig. 1 - DC test circuits

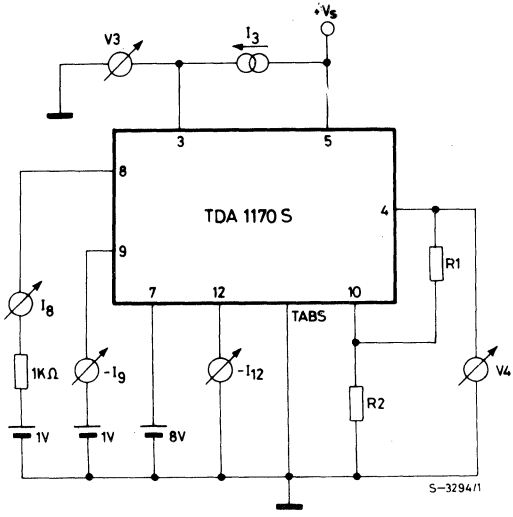


Fig. 1a

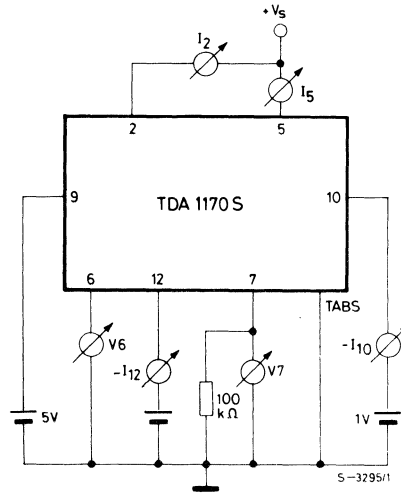


Fig. 1b

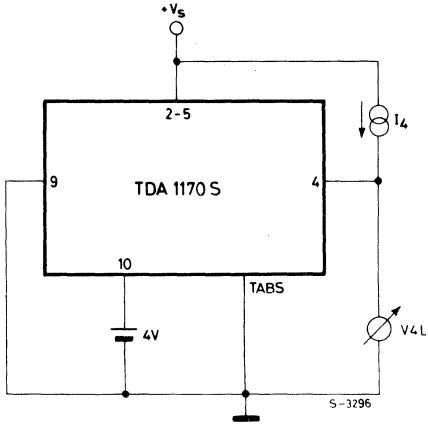


Fig. 1c

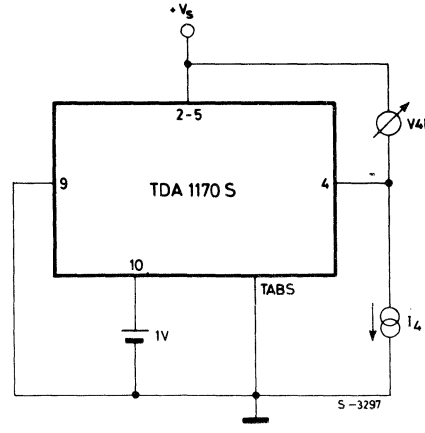


Fig. 1d

AC CHARACTERISTICS (Refer to the test circuit, V_S= 25V; f = 50 Hz; T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_s	Supply current	I_y = 1 App		140		mA	2
I_8	Sync. input current (positive or negative)		500			μA	2
V_4	Flyback voltage	I_y = 1 App		51		V	2
V_9	Peak to peak oscillator sawtooth voltage			2.4		V	2
t_{fly}	Flyback time	I_y = 1 App		0.7		ms	2
f_o	Free running frequency	$(P_1 + R_1)$ = 300 KΩ C_2 = 100 nF		44		Hz	2
		$(P_1 + R_1)$ = 260 KΩ C_2 = 100 nF		52		Hz	2
Δf	Synchronization range	I_8 = 0.5 mA	14			Hz	2
$\frac{\Delta f}{\Delta V_s}$	Frequency drift with supply voltage	V_s = 10 to 35V		0.005		Hz/V	2
$\left\|\frac{\Delta f}{\Delta T_{tab}}\right\|$	Frequency drift with tab temperature	T_{tab}= 40 to 120°C		0.01		Hz/°C	2

Fig. 2 - AC test circuit

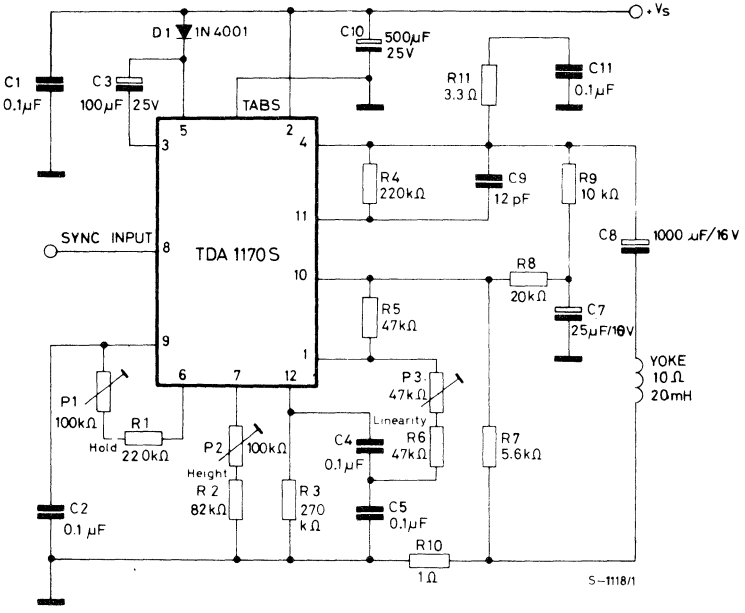
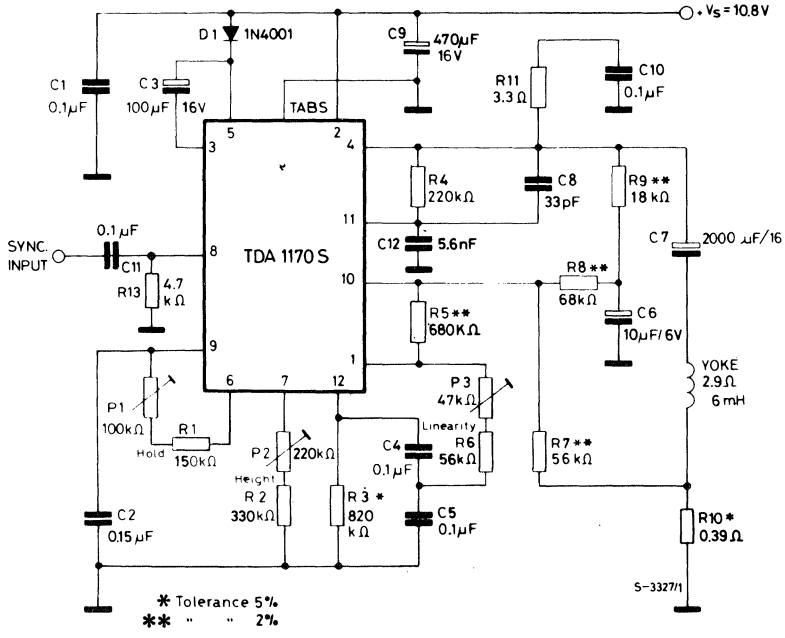


Fig. 3 - Typical application circuit for small screen B/W TV set (R_y = 2.9Ω, L_y= 6 mH; I_y= 1.1 App)

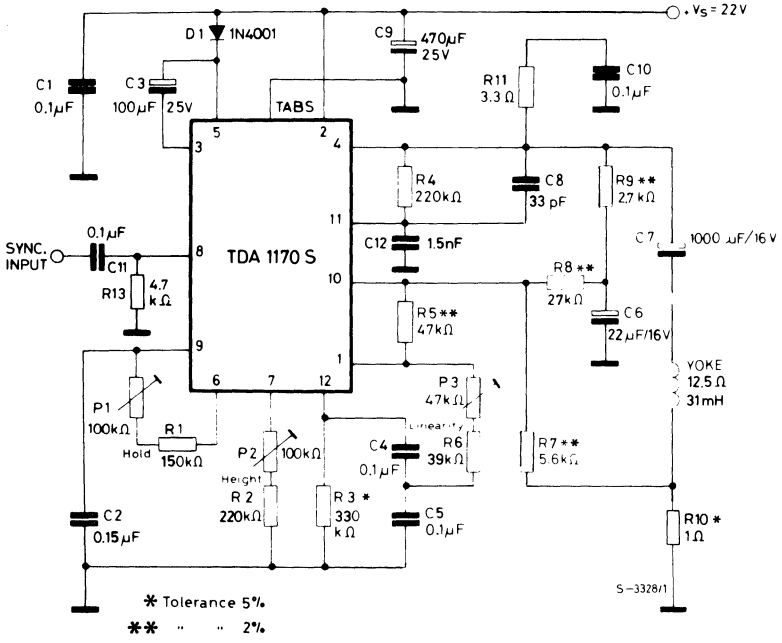


Typical performance

V_s	Operating supply voltage	10.8	V
I_s	Supply current	155	mA
t_{fly}	Flyback time	0.5	ms
P_{tot}	TDA 1170S power dissipation	1.35	W
I_y	Maximum scanning current (peak to peak)	1.30	A

For safe working up to T_{amb}= 60°C a heatsink of R_{th}= 30°C/W is required.

Fig. 4 - Typical application circuit for small screen 90° PIL TVC set (R_y= 12.5Ω ; L_y= 31 mH; I_y= 0.8 App)

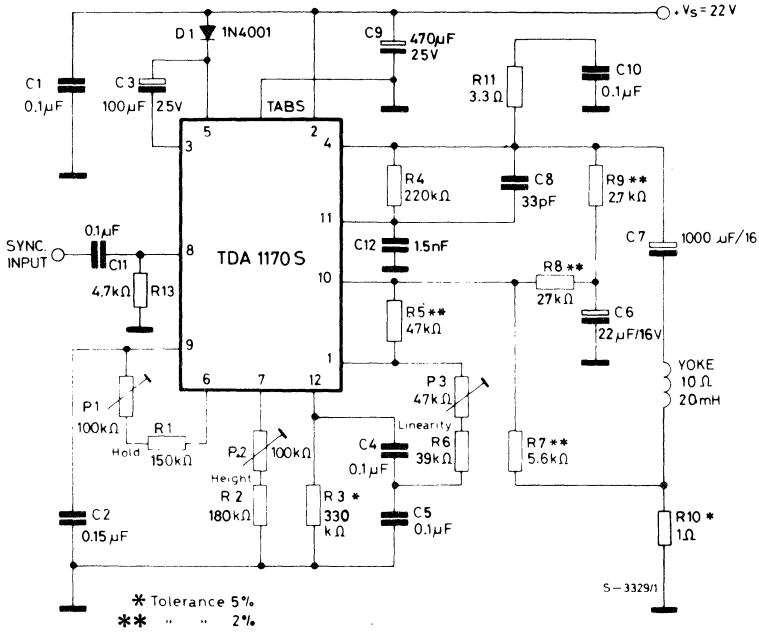


Typical performance

V_s	Operating supply voltage	22	V
I_s	Supply current	120	mA
t_{fly}	Flyback time	0.8	ms
P_{tot}	TDA 1170S power dissipation	1.95	W
I_y	Maximum scanning current (peak to peak)	1.0	A

For safe working up to T_{amb}= 60°C a heatsink of R_{th}= 18°C/W is required.

Fig. 5 - Typical application circuit for large screen B/W TV set (R_y= 10Ω; L_y= 20 mH; I_y= 1 App)

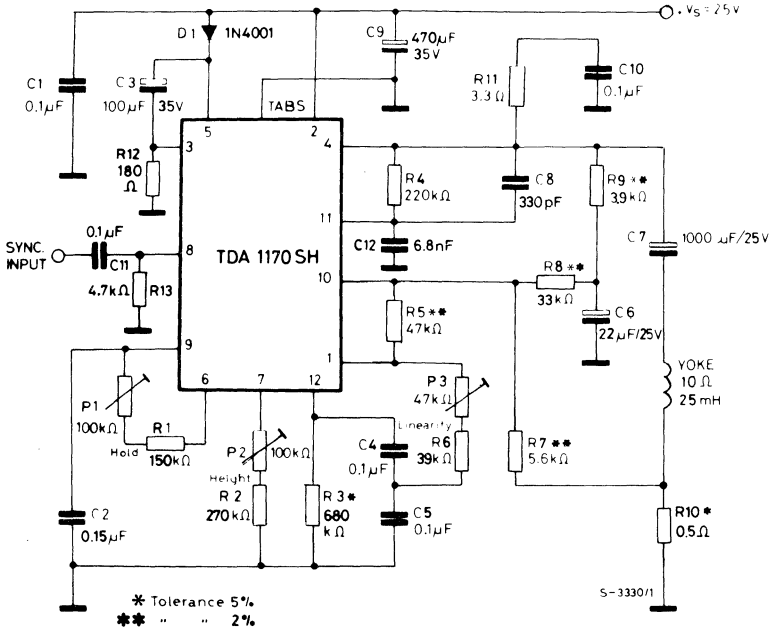


Typical performance

V_s	Operating supply voltage	22	V
I_s	Supply current	145	mA
t_{fly}	Flyback time	0.7	ms
P_{tot}	TDA 1170S power dissipation	2.3	W
I_y	Maximum scanning current (peak to peak)	1.2	A

For safe working up to T_{amb}= 60°C a heatsink of R_{th}= 14°C/W is required.

Fig. 6 - Typical application circuit for large screen 110° PIL TVC set (R_y= 10Ω ; L_y= 25 mH; I_y= 1.25 App)

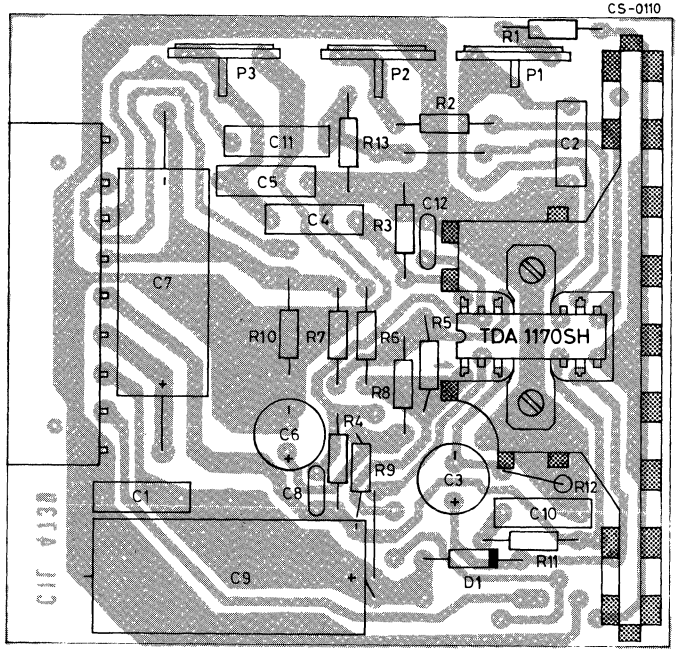


Typical performance

V_s	Operating supply voltage	25	V
I_s	Supply current	175	mA
t_{fly}	Flyback time	1	ms
P_{tot}	TDA 1170SH power dissipation	3.25	W
I_y	Maximum scanning current (peak to peak)	1.4	A

For safe working up to T_{amb}= 60°C a heatsink of R_{th}= 8.5°C/W is required.

Fig. 7 - P.C. board and component layout of the circuit of fig. 6 (1 : 1 scale)



Note: For the heatsink (1170 S and 1170 SH) see mounting instructions

MOUNTING INSTRUCTIONS

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

TDA 1170S

The junction to ambient thermal resistance of the TDA 1170S can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 8) or to an external heatsink (fig. 9).
The diagram of fig. 10 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "s" of two equal square copper areas having a thickness of 35 μ (1.4 mil).

MOUNTING INSTRUCTIONS (continued)

Fig. 8 - Example of P.C. board copper area used as heatsink.

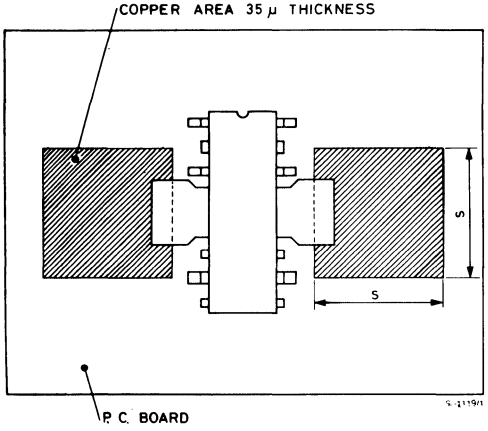


Fig. 9 - Example of TDA 1170 S with external heatsink.

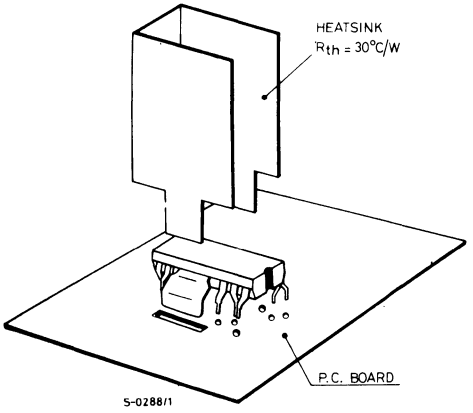


Fig. 10 - Maximum Power dissipation and junctional-ambient thermal resistance vs. "S"

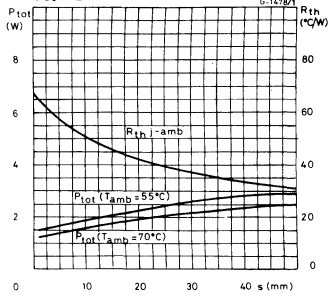


Fig. 11 - Maxim. allowable power dissipation vs. ambient temp. (TDA1170S)

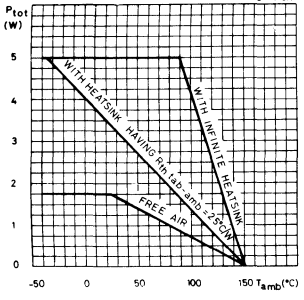
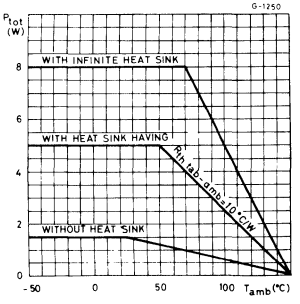


Fig. 12 - Maxim. allowable power dissipation vs. ambient temp. (TDA1170SH)

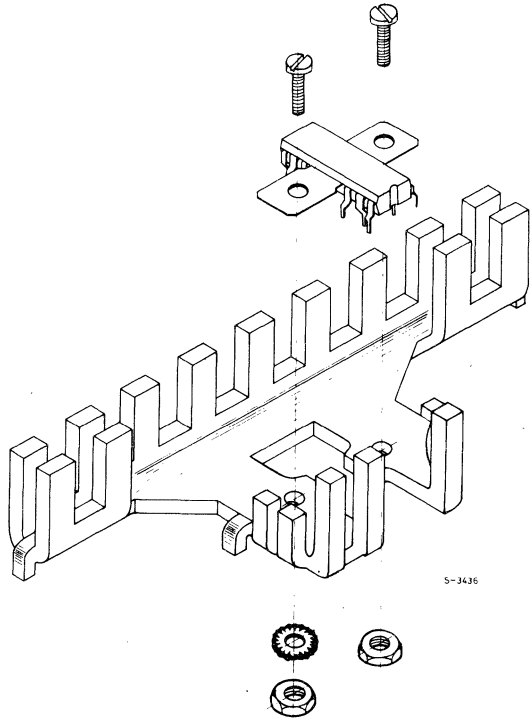


TDA 1170SH

The power dissipated in the circuit may be removed by connecting the tabs to an external heatsink according to fig. 12. The desired thermal resistance may be obtained by fixing the TDA1170SH to a suitable dimensioned plate as shown in fig. 13.

MOUNTING INSTRUCTIONS (continued)

Fig. 13 - Mounting example.



LINEAR INTEGRATED CIRCUIT

TDA1180P

TV HORIZONTAL PROCESSOR

The TDA 1180P is a horizontal processor circuit for b.w. and colour television receiver. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package. The TDA 1180P combines the following functions:

- Noise gated horizontal sync separator.
- Noise gated vertical sync separator.
- Horizontal oscillator with frequency range limiter.
- Phase comparator between sync pulses and oscillator pulses (PLL).
- Phase comparator between flyback pulses and oscillator pulses (PLL).
- Loop gain and time constant switching (VCR).
- Composite blanking and key pulse generator.
- Protection circuits.
- Output stages with high current capability.

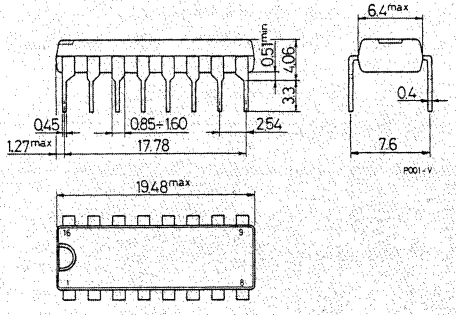
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 1)	15	V
V_2	Voltage at pin 2	18	V
V_4	Voltage at pin 4	V_s	
V_8	Voltage at pin 8	$\begin{cases} V_s \\ -6 \end{cases}$	V
V_9	Voltage at pin 9	$\begin{cases} +6 \\ -6 \end{cases}$	V
V_{11}	Voltage at pin 11	V_s	
I_2	Pin 2 peak current	1	A
I_3	Pin 3 peak current	0.5	A
I_6	Pin 6 current	30	mA
I_7	Pin 7 current	20	mA
I_{10}	Pin 10 current	30	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1180P

MECHANICAL DATA

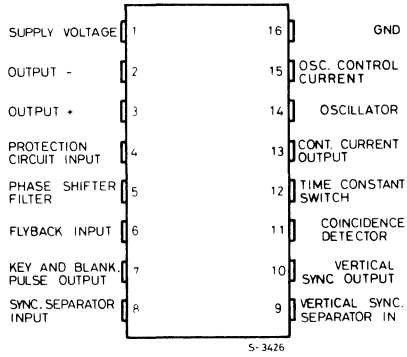
Dimensions in mm



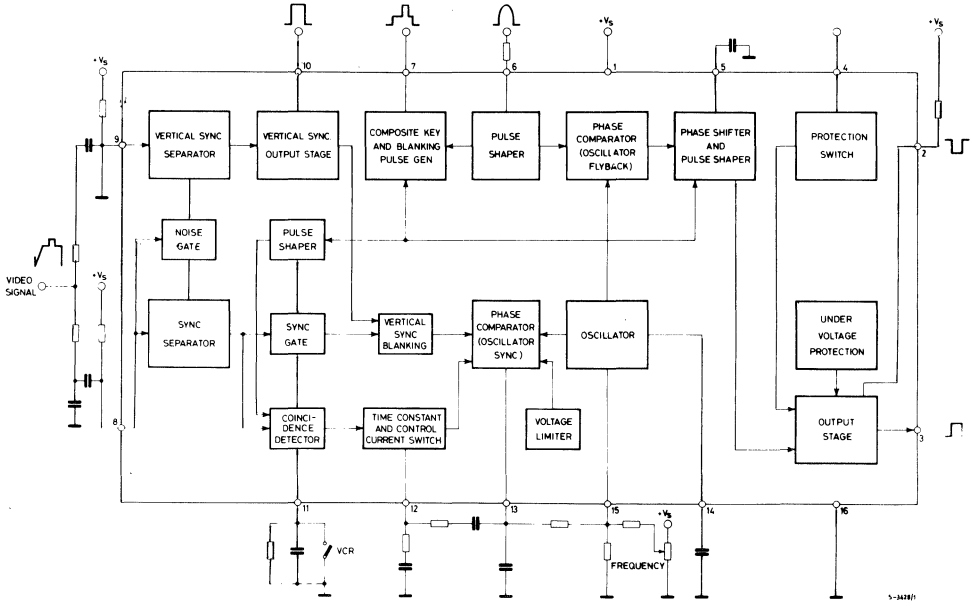
TDA1180P

CONNECTION DIAGRAM

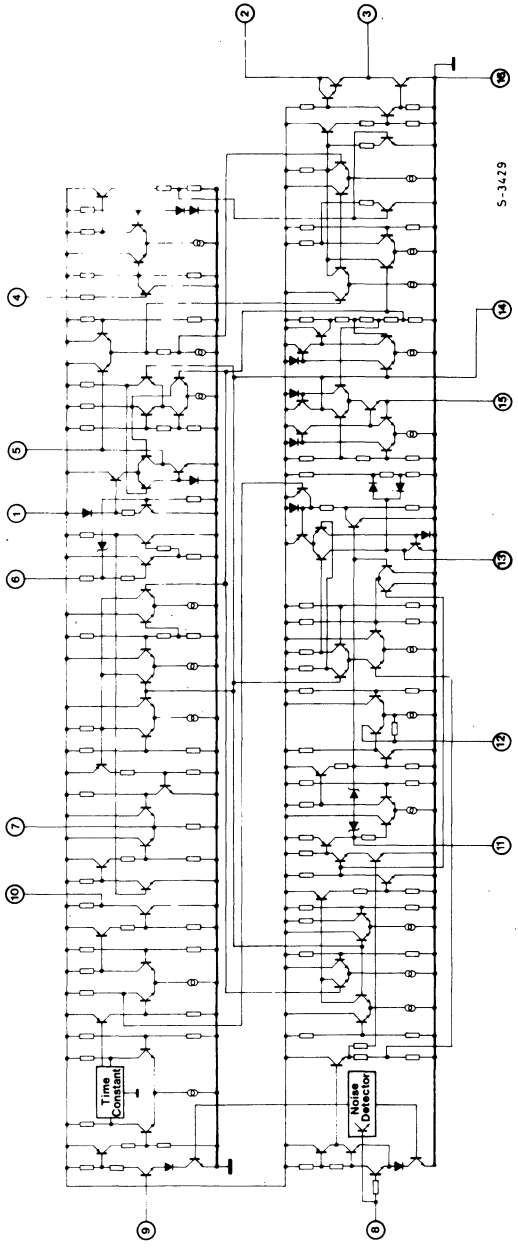
(top view)



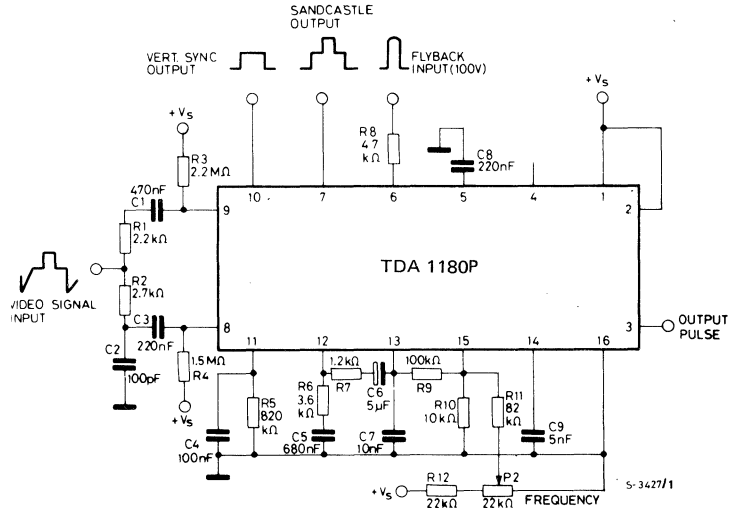
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= 12V, T_{amb}= 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		10	12	13.2	V
I_s	Supply current	I_3= 0		40	52	mA
V_s	Supply voltage at which the output pulses (at pin 2 and 3) are switched off				4	V

HORIZONTAL SYNC. SEPARATOR AND NOISE GATE

V_i	Peak to peak input signal		1	3	6	V
V_8	Input switching voltage	I_8 = 80 µA		1.5		V
I_8	Input switching current	V_8 = 1.4V		10		µA
I_8	Input blocking current for noise suppression			0.9		mA
V_8	Input switching voltage for noise suppression			2.1		V
I_8	Leakage current	V_8 = -5V			1	µA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
VERTICAL SYNC. SEPARATOR						
V_I	Peak to peak input signal		1	3	6	V
V_9	Input switching voltage	$I_9 = 80\ \mu A$		1.5		V
I_9	Input switching current	$V_9 = 1.4V$		5		μA
I_9	Leakage current	$V_9 = -5V$			1	μA
V_{10}	Vertical sync. pulse output voltage	No load at pin 10	11			V
R_{10}	Output resistance			10		$K\Omega$
t_{LV}	Delay between leading edge of input and output signals			17		μs
t_{TV}	Delay between trailing edge of input and output signals			50		μs
t_V	Vertical sync pulse duration			190		μs
PROTECTION CIRCUIT						
V_4	Input voltage for switching off the output pulses	Output pulses OFF			0.5	V
		Output pulses ON	1			
R_4	Input resistance			200		$K\Omega$
I_4	Input current		5			μA
FLYBACK PULSE						
V_6	Input threshold voltage of blanking generator			1.5		V
V_6	Input threshold voltage of phase comparator			7.6		V
I_6	Input switching current	$V_6 \geqslant 1.7V$		0.23		mA
OUTPUT PULSE						
V_3	Peak to peak output voltage	$I_3 = 150$ mApp		10		V
I_3	Output current	$V_3 = 5V$		500		mA
R_3	Output resistance	at leading edge of output pulse		3		Ω
		at trailing edge of output pulse		20		
t_p	Output pulse duration		20	22	26	μs
COMPOSITE BLANKING AND KEY PULSE						
V_{7K}	Key pulse output peak voltage		9	11		V
V_{7B}	Blanking pulse output voltage		4.2	4.5	4.8	V
R_7	Output resistance			100		Ω
t_{SK}	Phase relation between trailing edge of key pulse and middle of sync input pulse			2.7		μs
t_K	Key pulse duration		3.5	3.8		μs
t_{fb}	Delay between flyback pulse and blanking pulse	$V_6 = 1.7$ V			0.2	μs

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
INTERNAL GATING PULSE						
t_g	Gating pulse duration			7.5		μs
t	Phase relation between middle of sync pulse and trailing and leading edge of gating pulse			3.75		μs
COINCIDENCE DETECTOR						
V_{11}	Output voltage	with coincidence		6.8		V
		without coincidence			4	
I_{11}	Peak output current			0.5		mA
VCR SWITCH						
V_{11}	Input voltage		0 to 4 or 8.5 to 12			V
$-I_{11}$	Output current		35			μA
I_{11}	Output current		0.4			mA
TIME CONSTANT SWITCH						
V_{12}	Output voltage			3		V
R_{12}	Output resistance	$4.5V < V_{11} < 8V$		100		Ω
		$V_{11} > 8.5V$ or $V_{11} < 4V$		40		KΩ
OSCILLATOR						
V_{14}	Low level threshold voltage			5.4		V
V_{14}	High level threshold voltage			8.2		V
I_{14}	Charge current			0.6		mA
I_{14}	Discharge current			0.3		mA
V_{15}	Current source supply voltage			3		V
I_{15}	Current source supply current			0.3		mA
f_o	Free running frequency			15625		Hz
$\frac{\Delta f_o}{f_o}$	Adjustment range			± 10		%
$\frac{\Delta f_o}{\Delta I_{15}}$	Frequency control sensitivity			52		$\frac{Hz}{\mu A}$
Δf_o	Frequency change when V_s drops to 4V				± 10	%

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OSCILLATOR-FLYBACK PULSE PHASE COMPARATOR						
V_5	Control voltage range			9.4 to 8.2		V
I_5	Peak control current				± 0.5	mA
I_5	Input current (blocked phase detector)				5	μA
t_d	Permissible delay between output pulse leading edge and flyback pulse leading edge			$t_p - t_f$		μs
$\frac{\Delta t}{\Delta t_d}$	Static control error				0.2	%
SYNC PULSE-OSCILLATOR PHASE COMPARATOR						
V_{13}	Control voltage range			4.6 to 1.4		V
I_{13}	Control peak current			±2		mA
$\frac{\Delta f}{\Delta t}$	Phase lock loop gain			2		$\frac{KHz}{\mu s}$
f	Catching and holding range			± 700		Hz
OVERALL PHASE RELATIONSHIP						
t_o	Phase relation between middle of flyback pulse and middle of sync pulse			2.6		μs
$\frac{\Delta V_5}{\Delta t_o}$	Adjustment sensitivity			65		$\frac{mV}{\mu s}$
$\frac{\Delta I_5}{\Delta t_o}$	Adjustment sensitivity			10		$\frac{\mu A}{\mu s}$

Fig. 1 - Vertical sync. output pulse

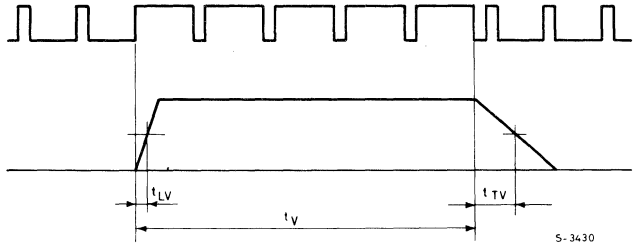


Fig. 2 - Relationship of main waveform phases

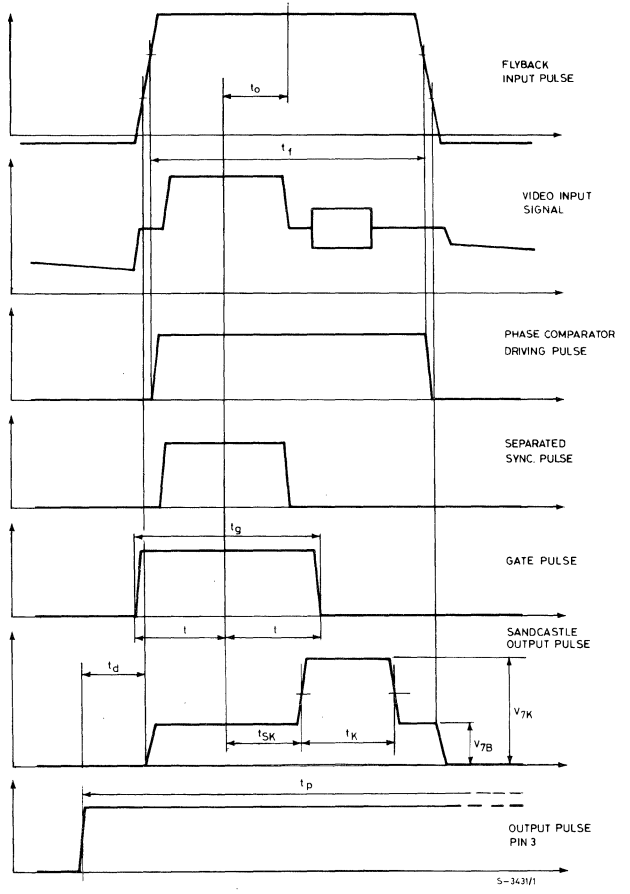


Fig. 3 - Free running frequency vs. supply voltage

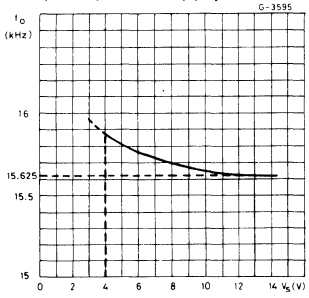


Fig. 4 - Overall phase relation vs. supply voltage

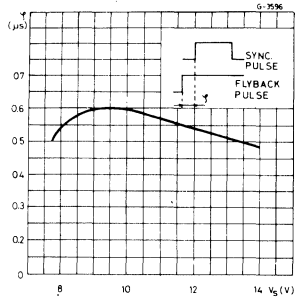
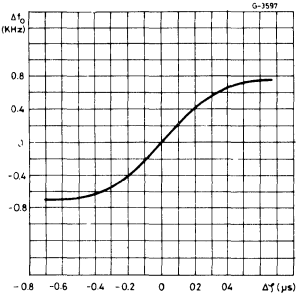


Fig. 5 - Loop gain



APPLICATION INFORMATION

Pin 1 – Positive supply

The operating supply voltage of the device ranges from 10V to 13.2V.

Pin 2 and 3 – Output

The outputs of TDA 1180P are suitable for driving transistor output stages, they deliver positive pulse at pin 3 and negative pulse at pin 2.
The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required.
The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.
Furthermore the output stages are internally protected against short circuit.

Pin 4 – Protection circuit input

By connecting pin 4 of the IC to earth the output pulses at pin 2 and 3 are shut off; this function has been introduced to protect the final stages from overloads.
The same pulses are also shut off when the supply voltage falls below 4V.

Pin 5 – Phase shifter filter

To compensate for the delay introduced by the line final stages, the flyback pulses to pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator.
The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.
The maximum phase shift allowed is:

$$t_d = t_p - t_f$$

where t_f is the flyback pulse duration.
Pin 5 has high input and output resistance (current generator).

APPLICATION INFORMATION (continued)

Pin 6 – Flyback input

The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.
The flyback input pulses are processed by a double threshold circuit; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

Pin 7 – Key and blanking pulse output

The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.
The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at pin 6.
The sum of the two signals (sandcastle pulse) is available on low impedance at output pin 7.

Pin 8 and 9 – Sync separators inputs

The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.
The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing.
An amplitude detector also connected to pin 8, blocks operation of the sync separators when interference or noise peaks exceed a certain preset value.

Pin 10 – Vertical sync output

The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin.
The output impedance is typically 10KΩ and the lowest amplitude without load is 11V.

Pin 11 – Coincidence detector

From the oscillator waveform a gate pulse 7 μs wide is taken whose phase position is centered on the horizontal syncronism.
The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.
This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync.
When the two signals are not accurately aligned in time it means that the oscillator is not synchronized.
In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on pin 12 (small time constant of low-pass filter).
This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.
In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.

APPLICATION INFORMATION (continued)

Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on pin 12 and reduces the sensitivity of the phase comparator.
In these conditions the phase lock has high noise immunity (narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.
To optimize the behaviour of the IC if a video recorder is used, the state of the detector can be forced by connecting pin 11 to earth or to $+V_s$. The characteristics of the phase lock thus correspond to the lack of synchronization.

Pin 12 – Time constant switch, (see pin 11)

Pin 13 – Control current output

The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current I_{13} (proportional to the phase difference between the two signals) to pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.
The time constant of the filter can be switched between two values according to the impedance presented by pin 12.
The voltage limiter at the output of the phase comparator limits the voltage excursion on pin 13 and therefore the frequency range in which the oscillator remains held-in.
The output resistance of pin 13 is :

low when $V_{13} > 4.3V$ or $V_{13} < 1.6V$
high when $1.6V < V_{13} < 4.3V$

To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync, a signal which inhibits the phase detector during the vertical interval is taken from the vertical output stage; inhibition remains even if the video signal is not present.
The free running frequency of the oscillator is determined by the values of the capacitor and of the resistor connected to pins 14 and 15 respectively.
To generate the line frequency output pulses, two thresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

Pin 14 – Oscillator (see pin 13)

Pin 15 – Oscillator control current input (see pin 13)

Pin 16 – Ground

Fig. 6 - Application circuit for large screen b.w. and colour TV

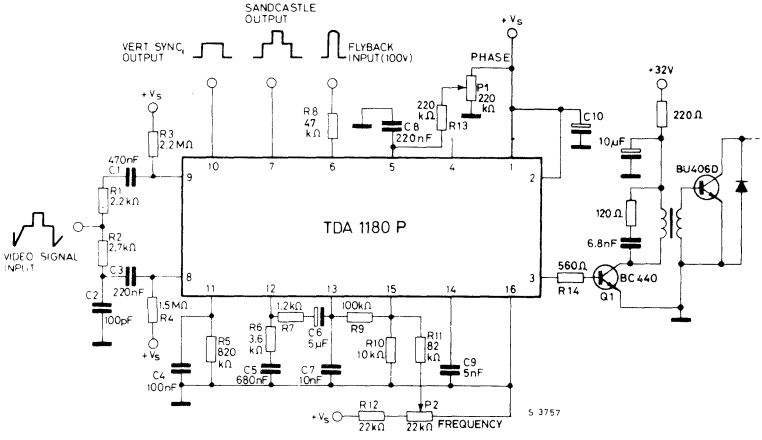


Fig. 7 - P.C. board and component layout for the circuit in fig. 6 (1:1 scale)

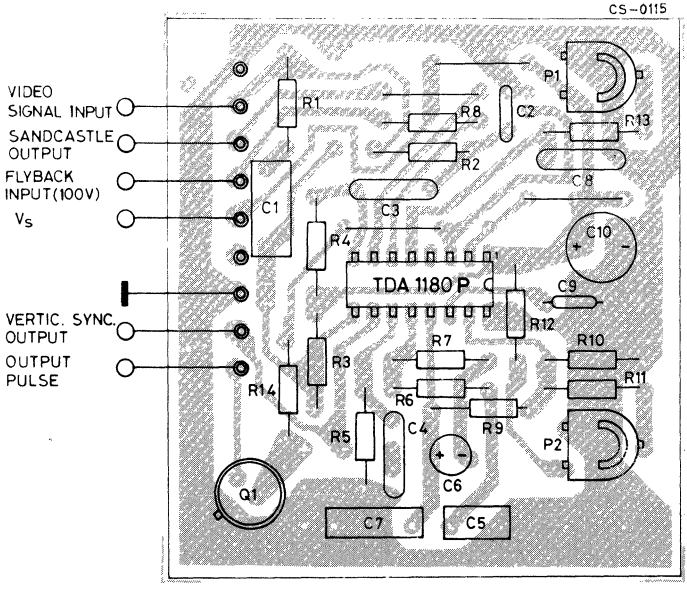


Fig. 8 - Application circuit for small screen b.w. TV.

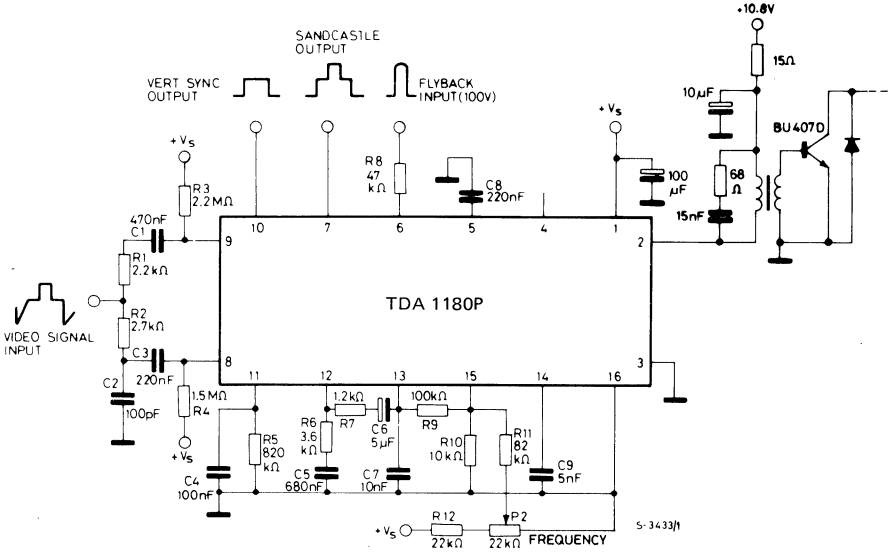
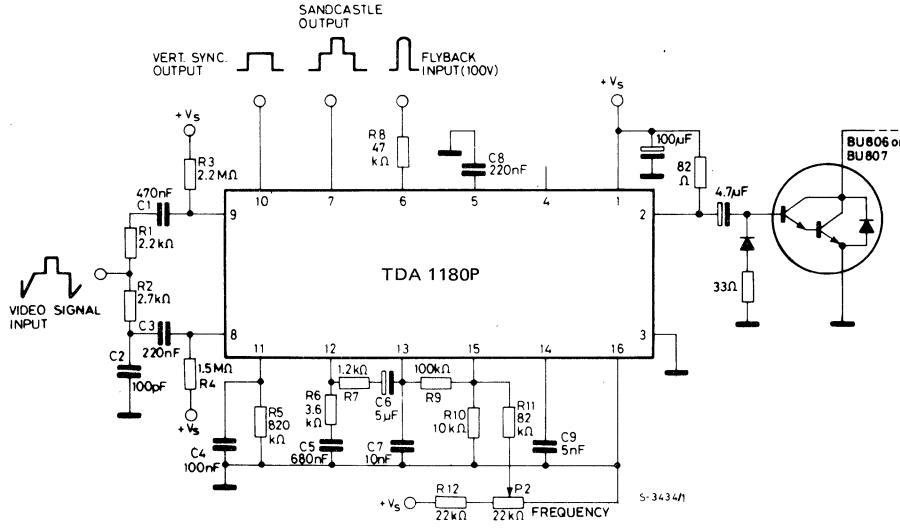


Fig. 9 - Application circuit for Darlington output stage



TDA1190Z

LINEAR INTEGRATED CIRCUIT

COMPLETE TV SOUND CHANNEL

The TDA 1190Z is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It performs all the functions needed for the TV sound channel:

- IF limiter-amplifier
- Active low-pass filter
- FM detector
- DC volume control
- AF preamplifier
- AF output stage

The TDA 1190Z can give an output power of 4.2W (d = 10%) into a 16Ω load at V_s = 24V, or 1.5W (d = 10%) into an 8Ω load at V_s = 12V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.

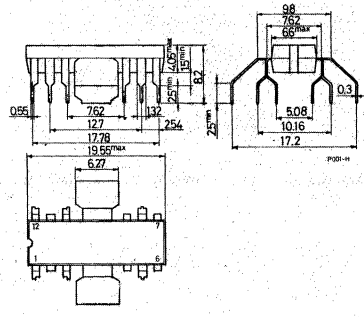
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 10)	28	V
V_i	Input signal voltage (pin 1)	1	V
I_o	Output peak current (non-repetitive)	2	A
I_o	Output peak current (repetitive)	1.5	A
P_{tot}	Power dissipation: at T_{tab} = 90°C	5	W
	at T_{amb} = 80° (free air)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

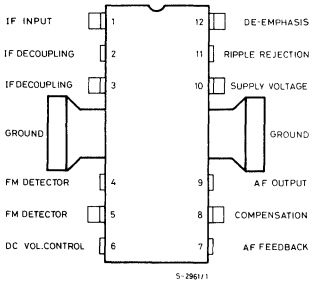
ORDERING NUMBER: TDA 1190Z

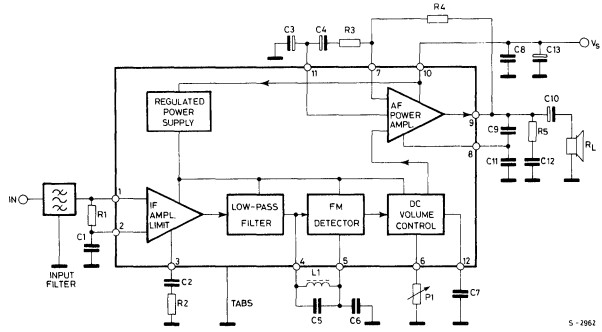
MECHANICAL DATA

Dimensions in mm

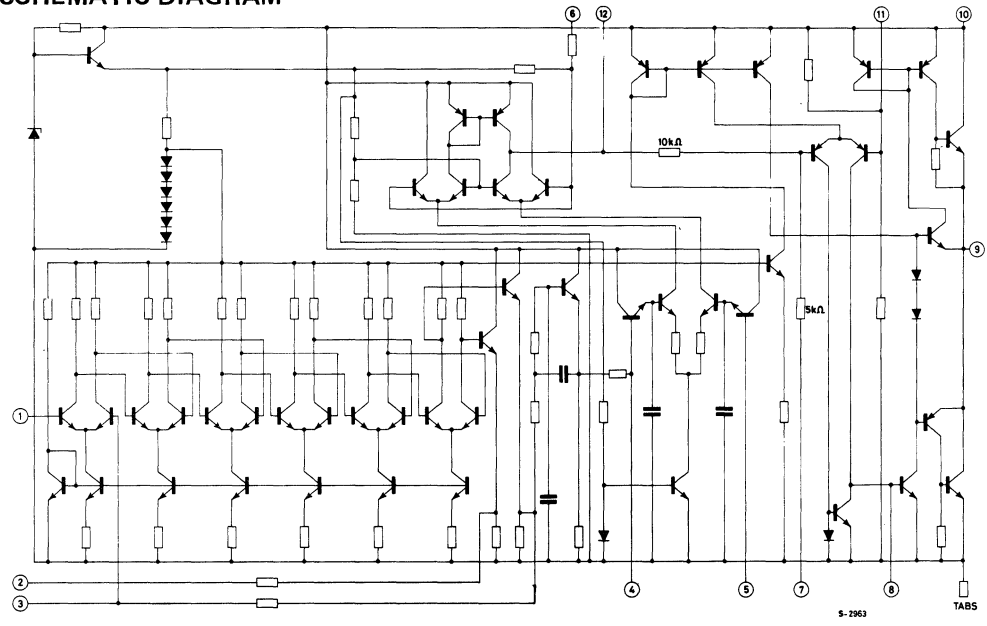


CONNECTION AND BLOCK DIAGRAM
(top view)



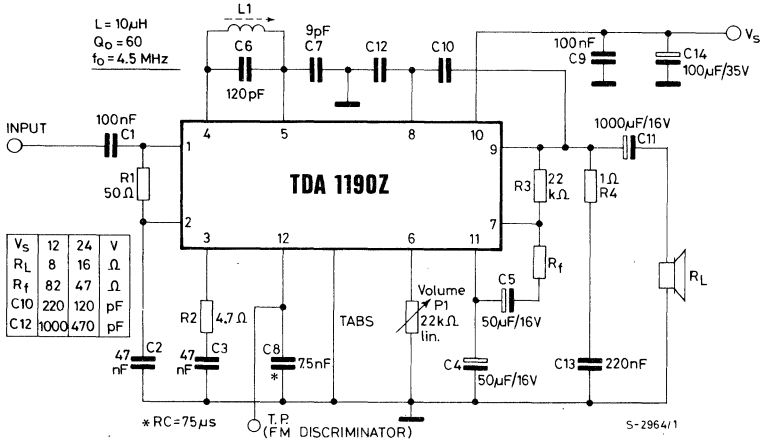


SCHEMATIC DIAGRAM



TDA1190Z

TEST CIRCUIT



V_s	12	24	V
R_L	8	16	Ω
R_f	82	47	Ω
C10	220	120	pF
C12	1000	470	pF

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max.	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 10)		9		28	V
V_o	Quiescent output voltage (pin 9)	V_s = 24V V_s = 12V	11 5.1	12 6	13 6.9	V V
I_d	Quiescent drain current	P_1 = 22 KΩ V_s = 24V V_s = 12V	11	22 19	45 40	mA mA
P_o	Output power	d = 10% f_m = 400 Hz f_o = 4.5 MHz Δf = ±25 kHz V_s = 24V R_L = 16Ω V_s = 12V R_L = 8Ω		4.2 1.5		W W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
P_o	Output power	d = 2% f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 kHz V_s = 24V R_L = 16Ω V_s = 12V R_L = 8Ω		3.5 1.4		W W
V_i	Input limiting voltage (-3 dB) at pin 1	f_o = 4.5 MHz Δf = ± 7.5 kHz f_m = 400 Hz P_1 = 0		40	100	μV
d	Distortion	P_o = 50 mW f_m = 400 Hz f_o = 4.5 MHz Δf = ± 7.5 kHz V_s = 24V R_L = 16Ω V_s = 12V R_L = 8Ω		0.75 1		% %
B	Frequency response of audio amplifier (-3 dB)	R_L = 16Ω C_{10} = 120 pF C_{12} = 470 pF P_1 = 22 kΩ R_f = 82Ω R_f = 47Ω		70 to 12 000 70 to 7 000		Hz Hz
V_o	Recovered audio voltage (PIN. 12)	$V_i \geqslant$ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δf = ± 7.5 kHz P_1 = 0		120		mV
AMR	Amplitude modulation rejection	$V_i \geqslant$ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δf = ± 25 kHz m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to noise ratio	$V_i \geqslant$ 1 mV V_o = 4 V f_o = 4.5 MHz f_m = 400 Hz Δf = ± 25 kHz	50	65		dB
R_f	External feedback resistance (between pins 7 and 9)				25	kΩ
R_i	Input resistance (pin 1)	V_i = 1 mV f_o = 4.5 MHz		30		kΩ
C_i	Input capacitance (pin 1)			5		pF
SVR	Supply voltage rejection	R_L = 16Ω f_{ripple} = 120 Hz P_1 = 22 kΩ		46		dB
A	DC volume control attenuation	P_1 = 12 kΩ		90		dB

Fig. 1 - Relative audio output voltage and output noise vs. input signal

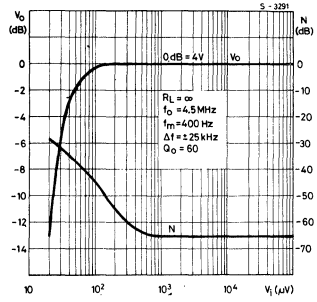


Fig. 2 - Output voltage attenuation vs. DC volume control resistance

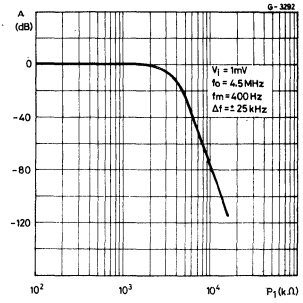


Fig. 3 - Amplitude modulation rejection vs. input signal

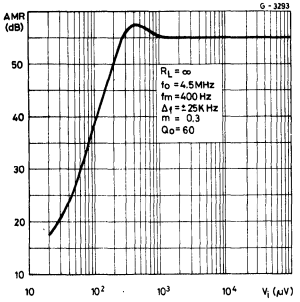


Fig. 4 - ΔAMR vs. tuning frequency change

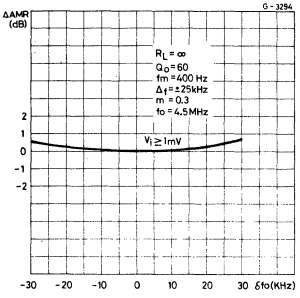


Fig. 5 - Recovered audio voltage vs. unloaded Q factor of the detector coil

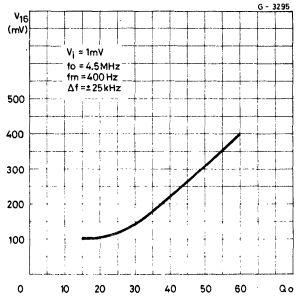


Fig. 6 - Distortion vs. output power

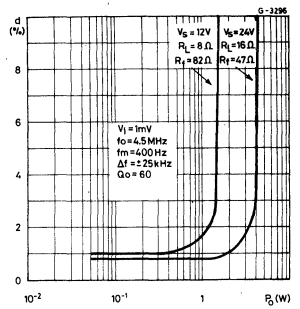


Fig. 7 - Distortion vs. frequency deviation

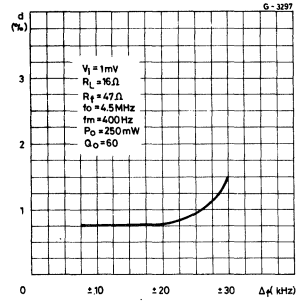


Fig. 8 - Distortion vs. tuning frequency change

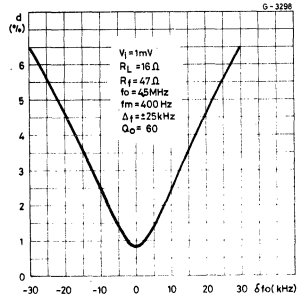


Fig. 9 - Audio amplifier frequency response

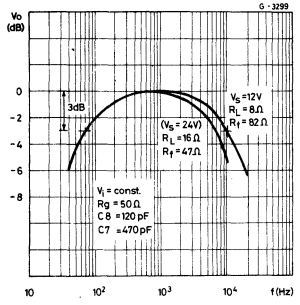


Fig. 10 - Supply voltage ripple rejection vs. ripple frequency

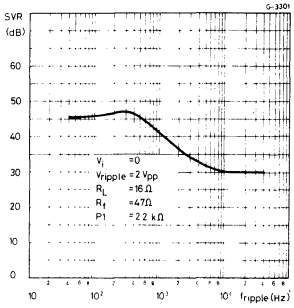


Fig. 11 - Supply voltage ripple rejection vs. volume control attenuation

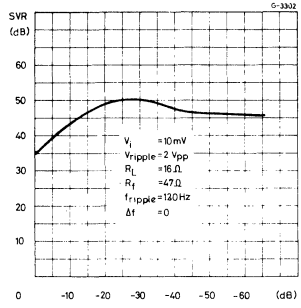


Fig. 12 - Output power vs. supply voltage

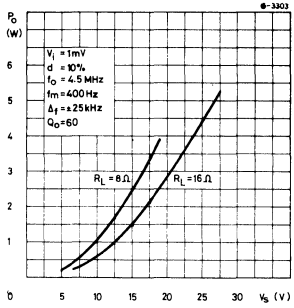


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

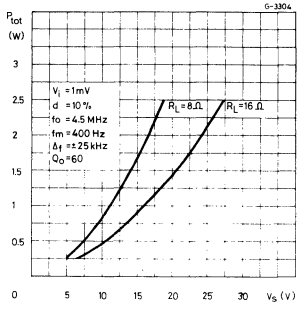


Fig. 14 - Power dissipation and efficiency vs. output power

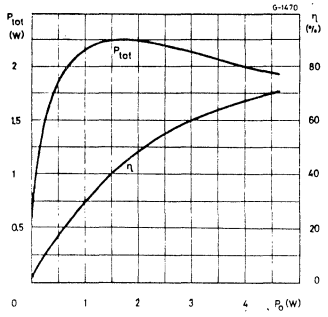
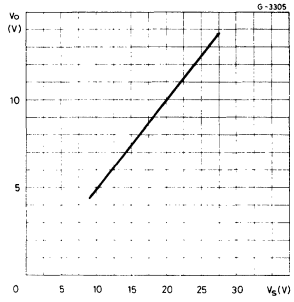


Fig. 15 - Quiescent output voltage (pin 9) vs. supply voltage



APPLICATION INFORMATION

The electrical characteristics of the TDA 1190Z remain almost constant over the frequency range of 4.5 to 6 MHz, therefore it can be used in all television standard (FM mod.). The TDA 1190Z has a high input impedance, so it can function with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 7, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier must enter into clipping.

The capacitor connected between pins 9 and 8 determines the upper cut-off frequency of the audio band. If larger bandwidth is required C_{10}, C_{12} must be reduced keeping C_{12}/C_{10} as in Fig. 16.

The capacitor connected between pin 12 and ground, toghether with the internal resistor of 10 KΩ, forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by inductive load and the wires connecting the loudspeaker.

APPLICATION INFORMATION (continued)

Fig. 16 - Typical application circuit

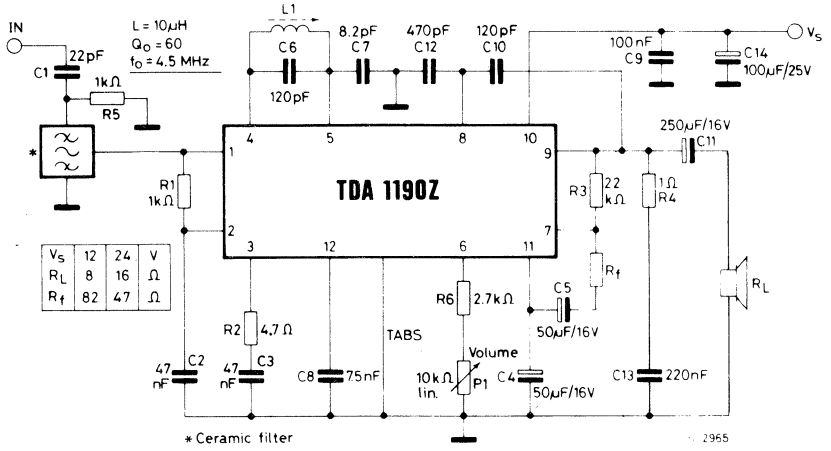
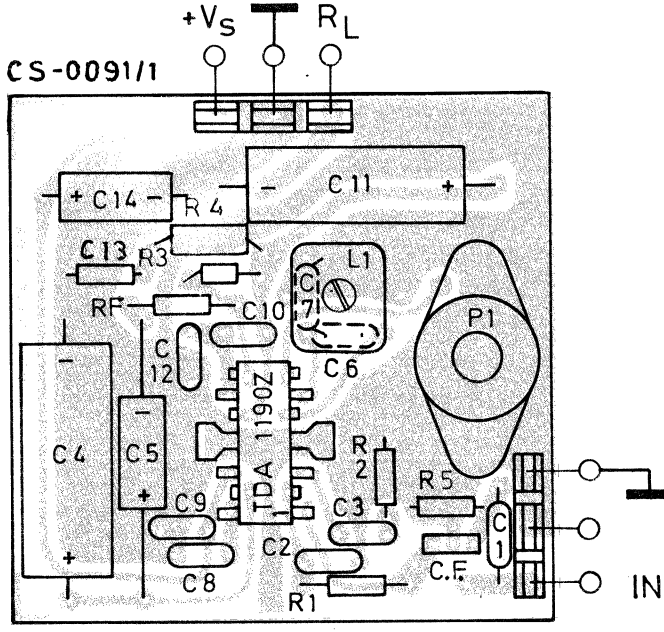


Fig. 17 - P.C. board and component layout of the circuit shown in Fig. 16



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA 1190Z can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (Fig. 18) or to an external heatsink (Fig. 19).
The diagram of figure 20 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 18 - Example of P.C. board copper area which is used as heatinsk

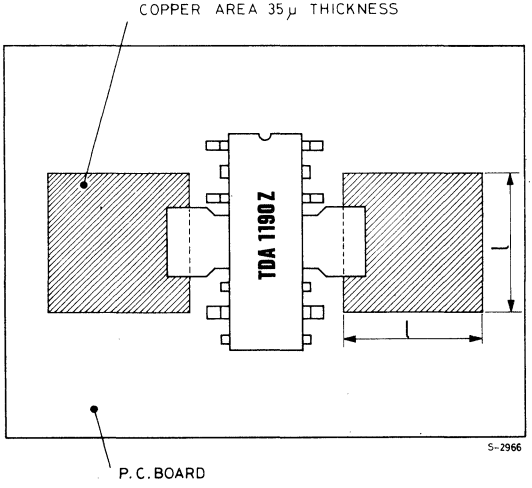


Fig. 19 - External heatsink mounting example

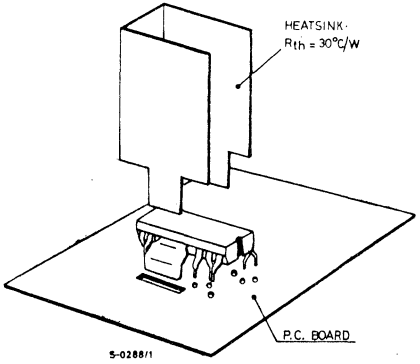


Fig. 20 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

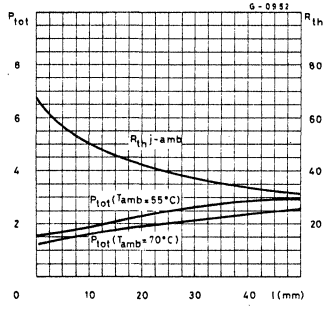
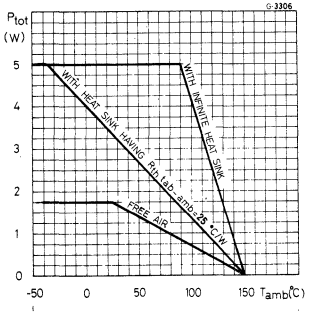


Fig. 21 - Maximum allowable power dissipation vs. ambient temperature



TDA1220A

LINEAR INTEGRATED CIRCUIT

AM-FM RADIO

The TDA 1220A is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in portable and home AM-FM radio sets as well as in industrial communication systems.
The functions incorporated are:

AM SECTION
- Preamplifier and double balanced mixer
- Local oscillator
- IF amplifier with internal AGC
- Balanced detector
- AF preamplifier

FM SECTION
- IF amplifier
- Quadrature detector
- AF preamplifier

The TDA 1220A is suitable for all AM and FM broadcasting bands and it features:

- Very low noise
- High sensitivity
- Wide supply voltage range (2.8 ÷ 16V)
- Low quiescent current (9 mA)
- Very simple DC switching of AM-FM sections
- Minimized number of external components
- Local oscillator up to 30 MHz

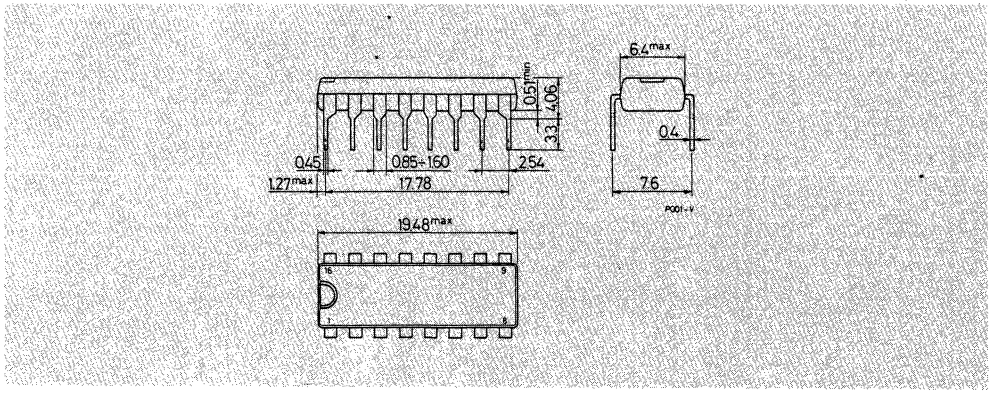
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} \leqslant 110\,°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

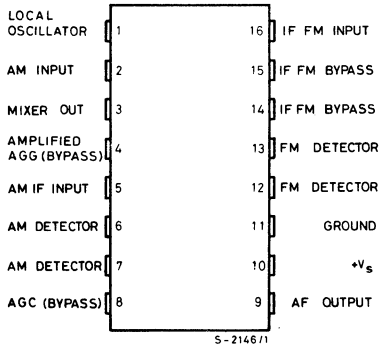
ORDERING NUMBER: TDA 1220A

MECHANICAL DATA

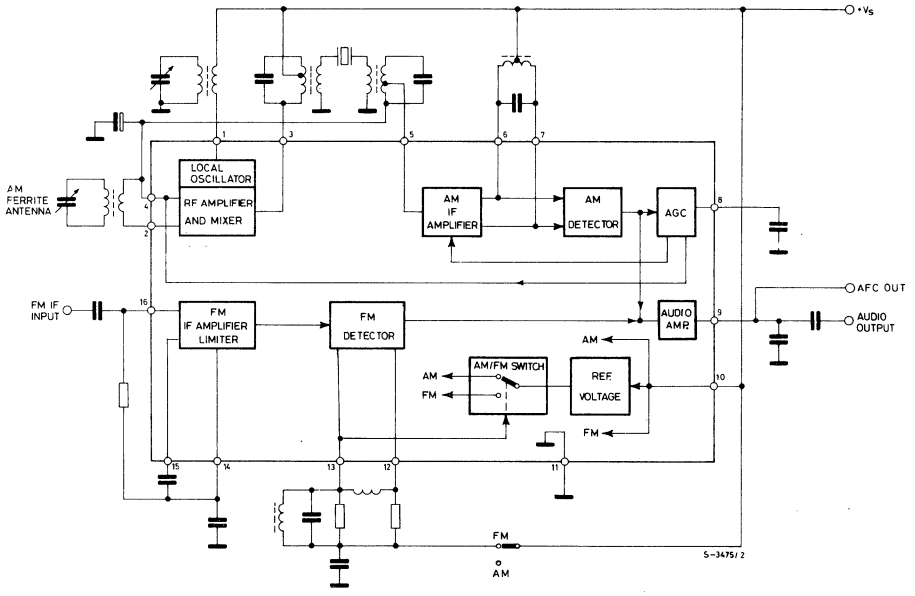
Dimensions in mm



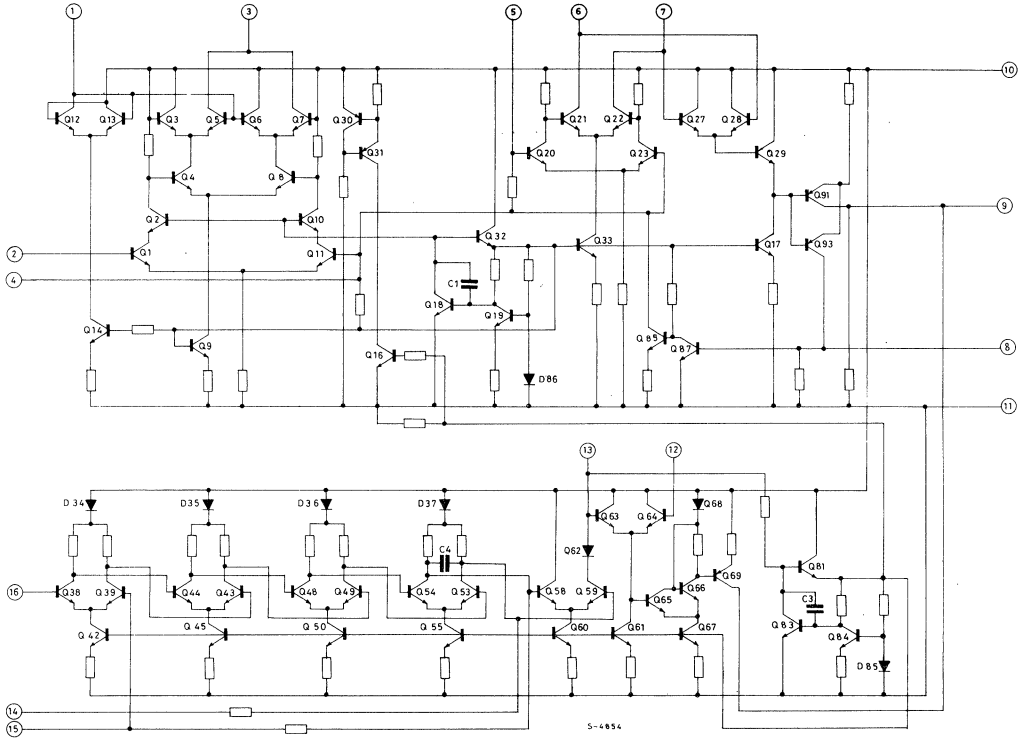
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s = 9V unless otherwise specified, refer to test circuit)

Parameter		Test condition	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_s	Supply Voltage		2.8		16	V
I_d	Drain current	AM section		9	15	mA
		FM section		9	15	
AC CHARACTERISTICS						
AM SECTION (f_o = 1 MHz; f_m = 1 KHz)						
V_i	Input sensitivity	S/N = 26 dB m = 0.3		12	25	μV
S/N	Ultimate quieting	V_i = 10 mV m = 0.3	50	60		dB
ΔV_i	AGC range	ΔV_{out}= 10 dB m = 0.3	80			dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV m = 0.3	40	80	160	mV
d	Distortion	V_i = 1 mV m = 0.8		1	3	%
d	Distortion	V_i = 1 mV m = 0.3		0.4	1	%
V_H	Max input signal handling capability	m = 0.8 d = 10%		80		mV
R_i	Input resistance between pins 2 and 4	m = 0		7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0		18		pF
R_o	Output resistance (pin 9)			7		KΩ
FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)						
V_i	Input limiting voltage	-3 dB limiting point			36	μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	35	48		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz V_i = 1 mV	55	70		dB
d	Distortion (single tuned)	Δf = ± 75 KHz V_i = 1 mV		0.7	3	%
d	Distortion (double tuned)	Δf = ± 22.5 KHz V_i = 1 mV		0.2		
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz V_i = 1 mV	40	80	160	mV
R_i	Input resistance between pin 16 and ground	Δf = 0		6.5		KΩ
C_i	Input capacitance between pin 16 and ground	Δf = 0		14		pF
R_o	Output resistance (pin 9)			7		KΩ

TEST CIRCUIT

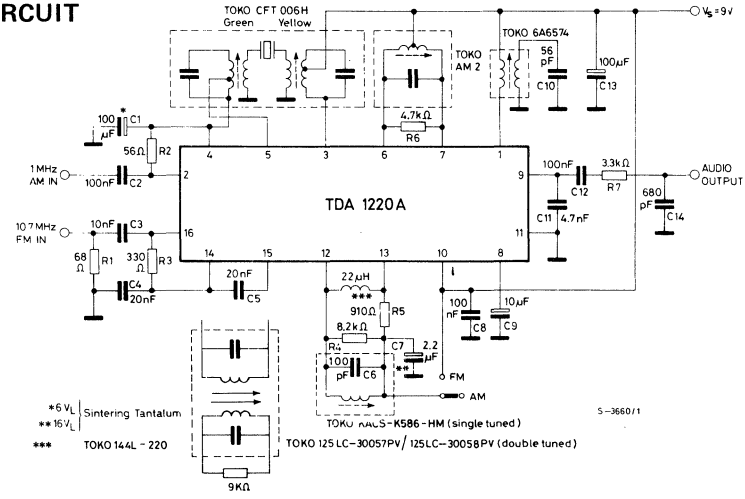


Fig. 1 - PC board and component layout (1 : 1 scale) of the test circuit

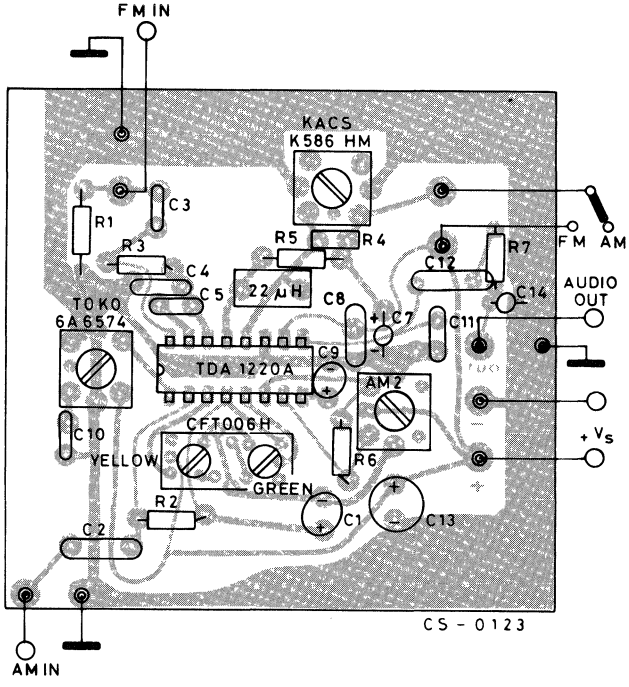


Fig. 2 - Drain current vs. supply voltage.

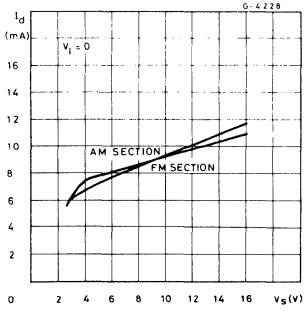


Fig. 3 - Audio output and signal to noise ratio vs. input signal (AM section)

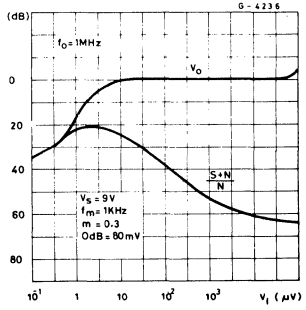


Fig. 4 - Audio output and signal to noise ratio vs. input signal (AM section)

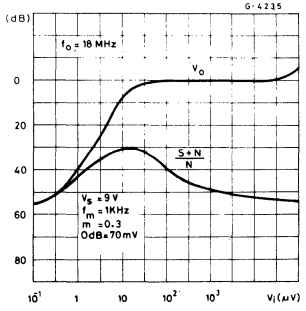


Fig. 5 - Distorsion vs. input signal (AM section)

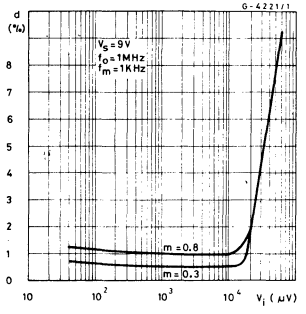


Fig. 6 - Distortion vs. modulation index (AM section)

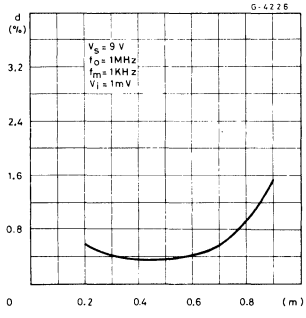


Fig. 7 - Amplified AGC voltage (pin 4) vs. input signal (AM section)

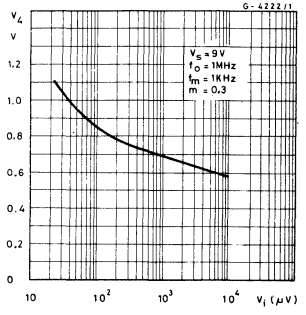


Fig. 8 - Audio output vs. supply voltage with DC level shift resistor (AM section)

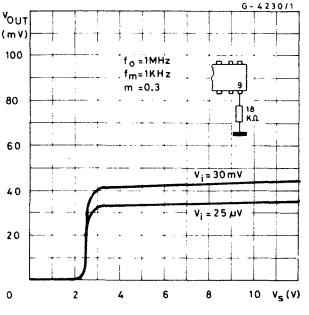


Fig. 9 - Audio output vs. supply voltage (AM section)

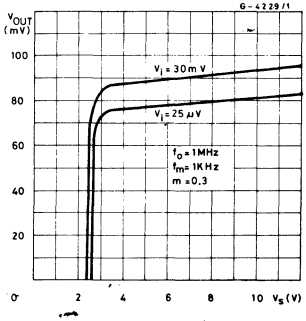


Fig. 10 - Δ DC voltage (pin 9) vs. ambient temperature (FM section)

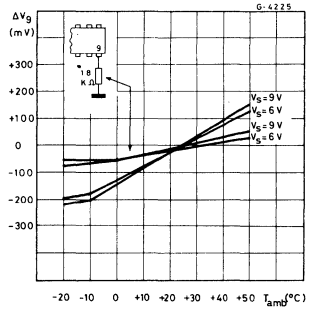


Fig. 11 - Audio output and signal to noise ratio vs. input signal (FM section)

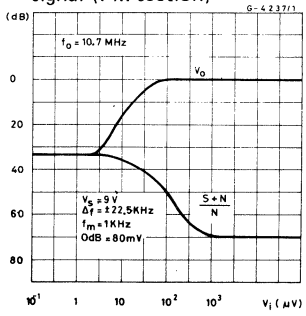


Fig. 12 - Distorsion vs. frequency deviation (FM section)

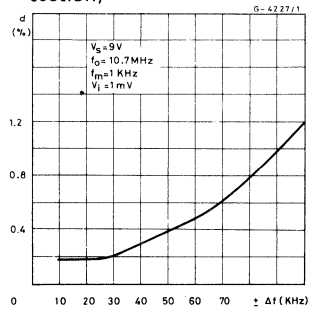


Fig. 13 - Distortion vs. input signal (FM section)

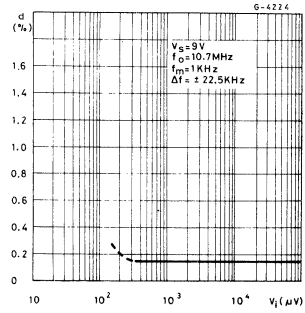


Fig. 14 - Amplitude modulation rejection vs. input signal (FM section)

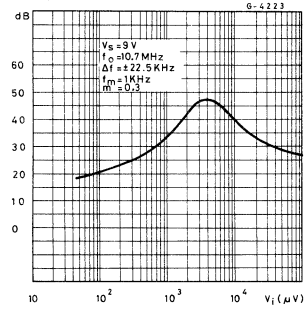


Fig. 15 - Audio output vs. supply voltage (FM section)

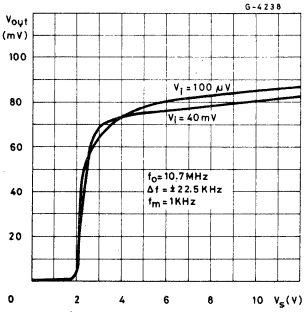


Fig. 16 - Audio output vs. supply voltage with DC level shift resistor (FM section)

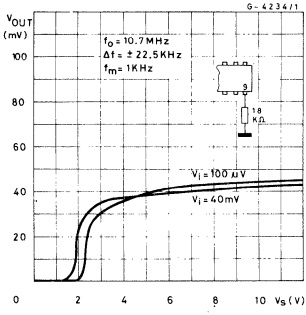


Fig. 17 - ΔDC output voltage (pin 9) vs. frequency shift (FM section)

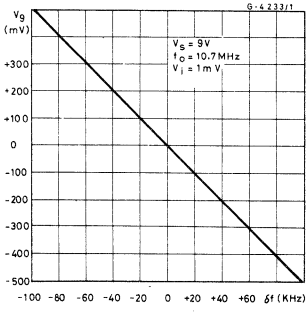


Fig. 18 -- DC output voltage (pin 9) vs. supply voltage (FM section)

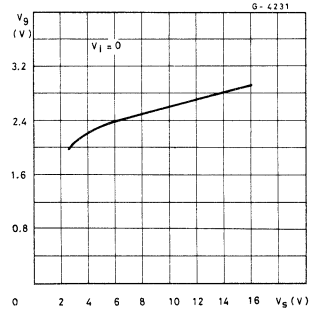
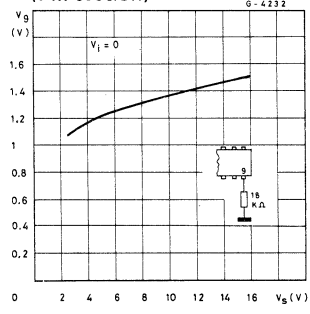


Fig. 19 - DC output voltage (pin 9) with DC level shift resistor vs. supply voltage (FM section)



APPLICATION INFORMATION

FM Section

IF Amplifier and limiter

The 10.7 MHz IF signal from the ceramic filter is amplified and limited by a chain of four differential stages.
Pin 16 is the amplifier input and has a typical input impedance of 6.5 KΩ in parallel with 14 pF at 10.7 MHz.
Bias for the first stage is available at pin 14 and provides 100% DC feedback for stable operating conditions. Pin 15 is the second input to the amplifier and is decoupled to pin 14, which is grounded by a 20 nF capacitor.
An RLC network is connected to the amplifier output and gives a 90° phase shift (at the IF centre frequency) between pins 13 and 12. The signal level at pin 13 is about 150 mV rms.

FM Detector

The circuit uses a quadrature detector and the choise of component values is determined by the acceptable level of distortion at a given recovered audio level.
With a double tuned network the linearity improves (distortion is reduced) and the phase shift can be optimized; however this leads to a reduction in the level of the recovered audio. A satisfactory compromise for most FM receiver applications is shown in the test circuit.

Care should be taken with the physical layout.
The main recommandations are:

- Locate the phase shift coil as near as possible to pin 13.
- Shunt pins 14 and 16 with a low value resistor (between 56Ω and 330Ω).
- Ground the decoupling capacitor of pin 14 and the 10.7 MHz input filter at the same point.

If the supply voltage goes under 6V add a DC level shift resistor of 18 KΩ from pin 9 to ground and change C11 to 8 nF.

AM-FM Switching

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

Typical DC Voltages (refer to the test circuit)

Pins	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Unit
AM	9	1.3	9	1.3	1.3	9	9	0.7	2	9	0	0	0	8.4	8.4	8.4	V
FM	9	0.4	9	0.4	0	9	9	0	2.6	9	0	9	9	8.1	8.1	8.1	V

APPLICATION INFORMATION (continued)

AM Section

RF Amplifier and mixer stages

The RF amplifier stage (pin 2) is connected directly to the secondary winding of the ferrite rod antenna or input tuned circuit. Bias is provided at pin 4 which must be adequately decoupled. The RF amplifier provides stable performance extending beyond 30 MHz.
The Mixer employed is a double - balanced multiplier and the IF output at pin 3 is connected directly to the IF filter coil.

Local oscillator

The local oscillator is a cross coupled differential stage which oscillates as the frequency determined by the load on pin 1.
The oscillator resonant circuit is transformer coupled to pin 1 to improve the Q factor and frequency stability.
The oscillator level at pin 1 is about 100 mV rms and the performance extends beyond 30 MHz, however to enhance the stability and reduce to a minimum pulling effects of the AGC operation or supply voltage variations, a high C/L ratio should be used above 10 MHz.
An external oscillator can be injected at pin 1. The level should be 50 mV rms and pin 1 should be connected to the supply via a 100Ω resistor.

IF Amplifier Detector

The IF amplifier is a wide band amplifier with a tuned output stage.
The outputs are at pins 6 and 7 which drive the balanced load and the differential positive peak AM detector, which is biased to reduce distortion at high modulation levels. At the output of balanced detectors of this type there is a low level signal at double the IF frequency (about 920 KHz). To avoid feedback of this signal by radiation from the detector coil, the shield around this coil must be grounded and the ferrite antenna placed in a suitable position.
The Audio output is at pin 9 (for either AM or FM); the IF frequency is filtered by an external capacitor which is also used as the FM mono de-enphasis network. The audio output impedance is about 7 KΩ and a high impedance load (~ 50 KΩ) must be used.

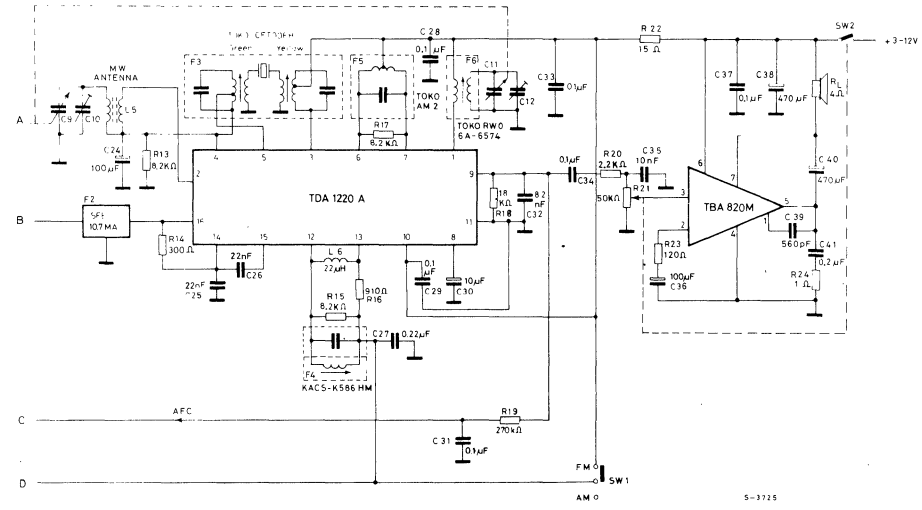
AGC

Both the RF and the first IF amplifiers have the same differential amplifier circuit configuration. The AGC action is obtained by control of the collector current of these stages.
At pin 8 there is a carrier envelope signal which is filtered by an external capacitor to remove the Audio and RF content and obtain a mean DC signal to drive the AGC circuit.

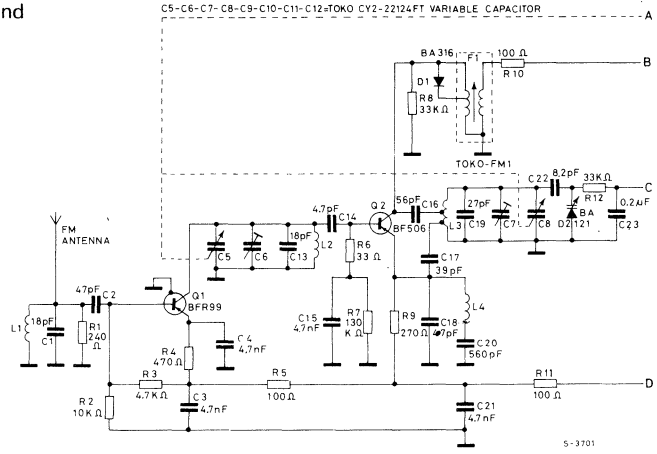
APPLICATION INFORMATION (continued)

Fig. 20 - Low cost AM-FM radio

(a)



(b) FM front end



COILS

L1 FM Antenna coil - 6 Turns copper wire 0.9 mm diameter. Inner diameter 4 mm. Winding pitch 1 mm.
L2 FM Tuning coil - 5 Turns copper wire 0.9 mm diameter. Inner diameter 4 mm Winding pitch 0.5 mm.
L4 - 18 Turns copper wire 0.6 mm diameter. Inner diameter 2.5 mm. Closely wound.
L5 MW Antenna coil - Televox.
L3 FM osc. coil - 4 Turns copper wire 0.9 mm diameter. Inner diameter 4 mm. Winding pitch 2 mm.

APPLICATION INFORMATION (continued)

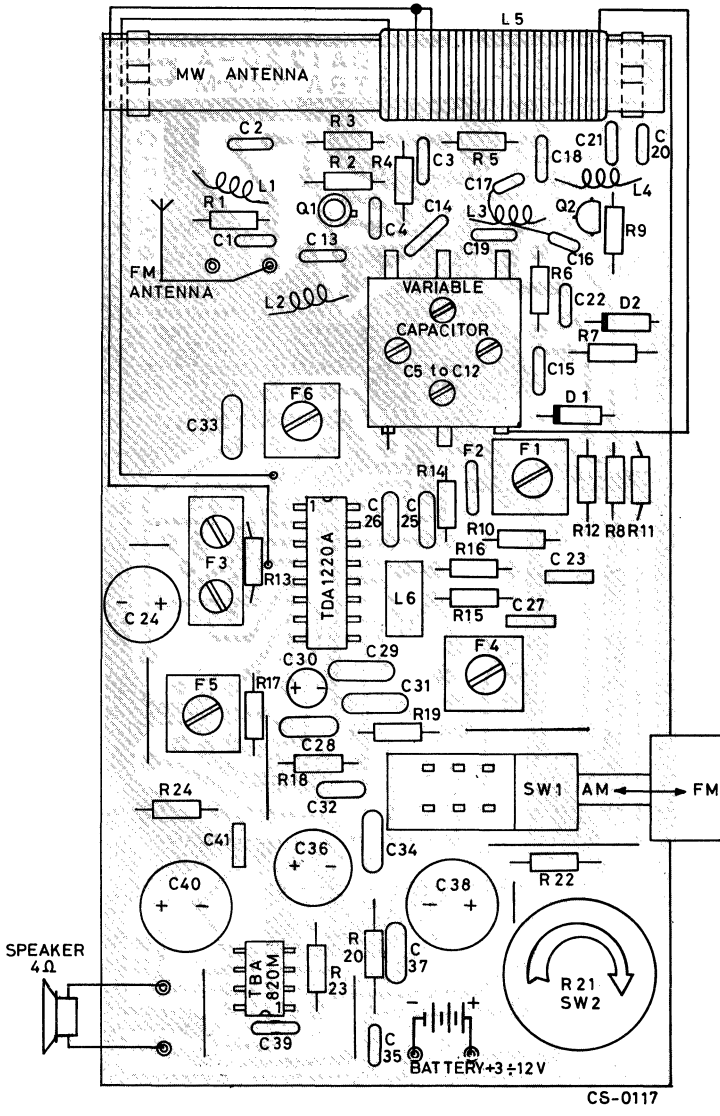


Fig. 21 - PC board and component layout (1:1 scale) of the low cost AM-FM radio in fig. 20.

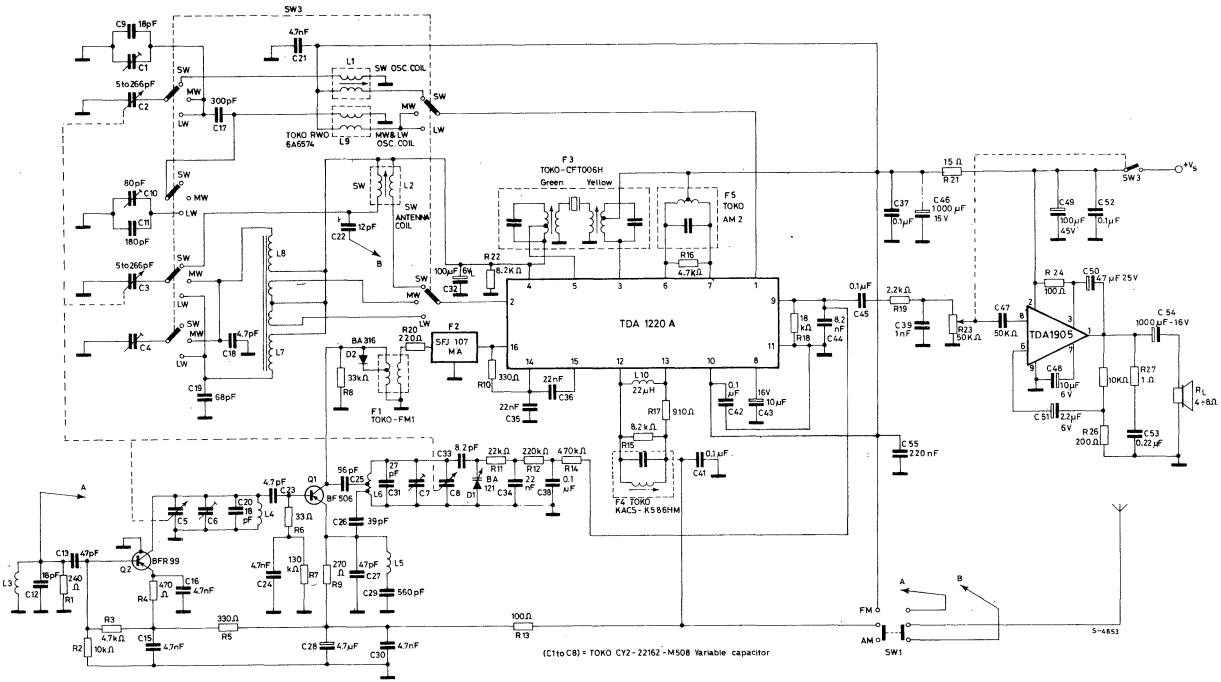
APPLICATION INFORMATION (continued)

Low cost receiver performance (V_s = 9V)

Parameter	Test conditions	Value
Wavebands	FM	87.5 ÷ 108 MHz
	AM	510 ÷ 1620 KHz
Sensitivity	FM : 75Ω (S + N/N) = 26 dB Δf = 22.5 KHz	⩽ 2 μV
	AM (S + N/N) = 6 dB m = 0.3	1 μV
	AM (S + N/N) = 26 dB m = 0.3	10 μV
Distortion f_m = 1 KHz	FM V_i = 100 μV Δf = 22.5 KHz P = 0.5W	⩽ 0.25 %
	FM V_i = 100 μV Δf = 75 KHz P = 0.5W	⩽ 1 %
	AM V_i = 100 μV m = 0.3 P = 0.5W	⩽ 0.6 %
	AM V_i = 100 μV m = 0.8 P = 0.5W	⩽ 1 %
$\frac{S+N}{N}$ f_m = 1 KHz	FM V_i = 100 μV Δf = 22.5 KHz P = 0.5W	⩾ 70 dB
	AM V_i = 1000 μV m = 0.3 P = 0.5W	⩾ 55 dB
Input limiting voltage	FM -3 dB point	⩽ 1.5 μV
A M R	FM V_i = 100 μV Δf = 22.5 KHz m = 0.3	⩾ 45 dB
I F	FM	10.7 MHz
	AM	460 KHz
Quiescent current	FM	23 mA
	AM	15 mA
Supply voltage range	FM	3 ÷ 12 V
	AM	3 ÷ 12 V

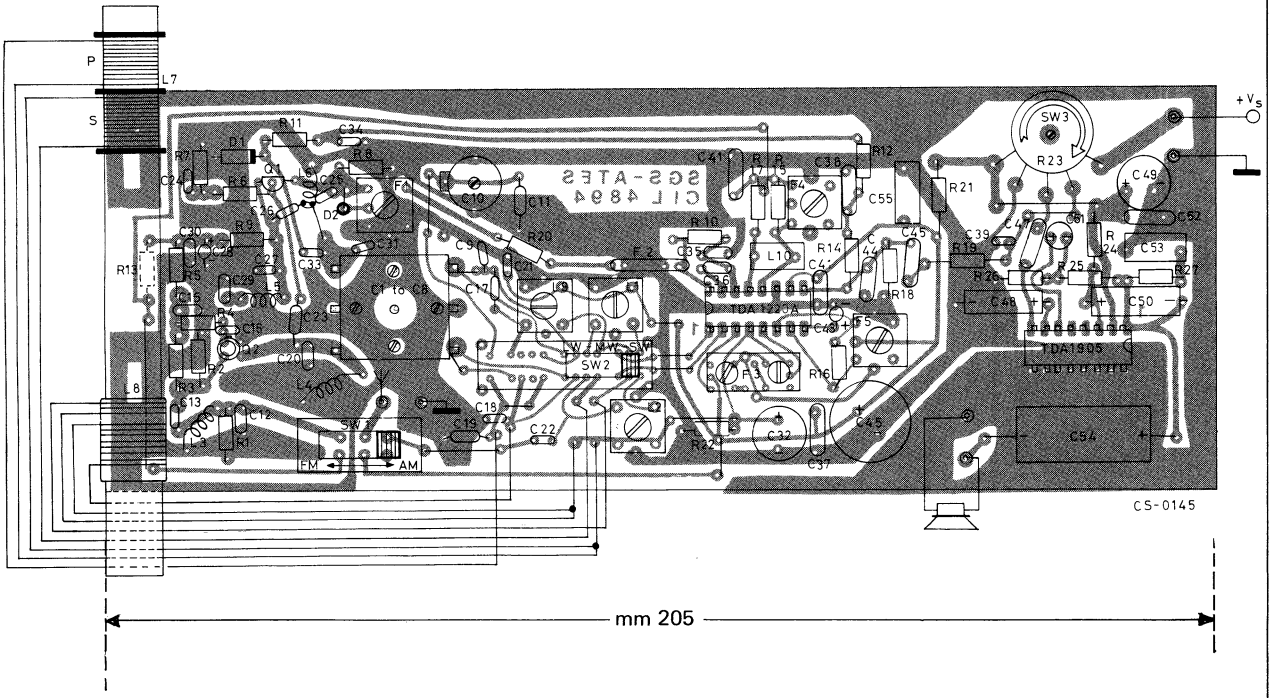
APPLICATION INFORMATION (continued)

Fig. 22 - LW - MW - SW - FM - radio



APPLICATION INFORMATION (continued)

Fig. 23 - PC board and component layout of the four band radio (fig. 22)

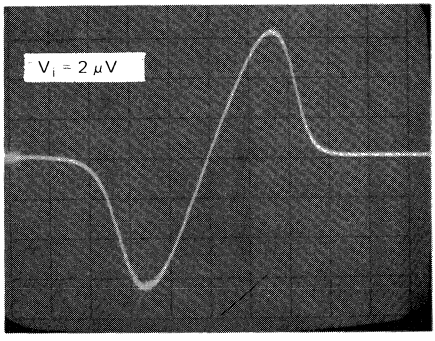


APPLICATION INFORMATION (continued)

FOUR BAND RADIO PERFORMANCE

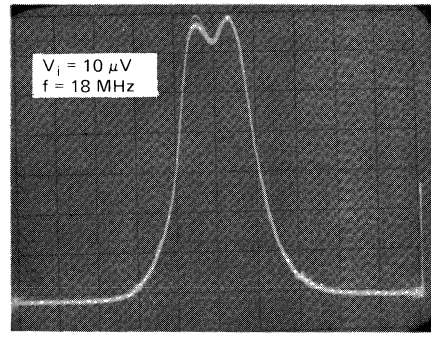
Parameter	Test conditions	Values
AM SECTION (*)		
$\left\lvert\frac{S+N}{N}\right\rvert$	V_i = 10 μV m = 0.3	26 dB
	V_i = 1 mV m = 0.3	55 dB
BW	-3 dB	10 KHz
Distortion	V_i = 20 μV m = 0.3	0.5 %
	V_i = 100 μV m = 0.3	0.5 %
	V_i = 1 mV m = 0.3	0.5 %
	V_i = 20 μV m = 0.8	0.9 %
	V_i = 1 mV m = 0.8	1 %
FM SECTION		
AMR	V_i = 30 μV Δf = 22.5 KHz m = 0.3 f_m = 1 KHz	45 dB
	V_i = 100 μV Δf = 22.5 KHz m = 0.3 f_m = 1 KHz	47 dB
Distortion	V_i = 10 μV Δf = 22.5 KHz	0.3 %
	V_i = 100 μV Δf = 22.5 KHz	0.2 %
	V_i = 1 mV Δf = 22.5 KHz	0.2 %
	V_i = 10 μV Δf = 75 KHz	1 %
	V_i = 100 μV Δf = 75 KHz	1 %
$\left\lvert\frac{S+N}{N}\right\rvert$	V_i = 10 μV Δf = 22.5 KHz	60 dB
	V_i = 100 μV Δf = 22.5 KHz	70 dB
	V_i = 1 mV Δf = 22.5 KHz	70 dB
Input limiting voltage	-3 dB	1 μV

(*) The performance remains substantially the same over LW, MW and SW bands.



100 KHz/div.

Fig. 24 - FM-SECTION
S curve response

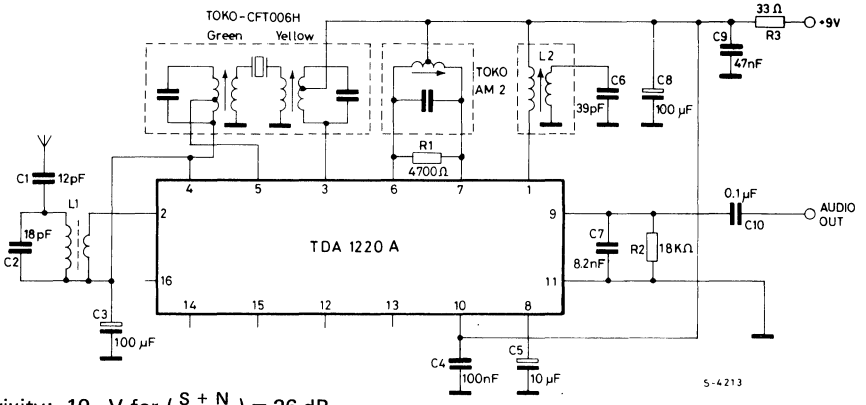


5 KHz/div.

Fig. 25 - AM-SECTION
Band pass IF filter response at AGC starting point.

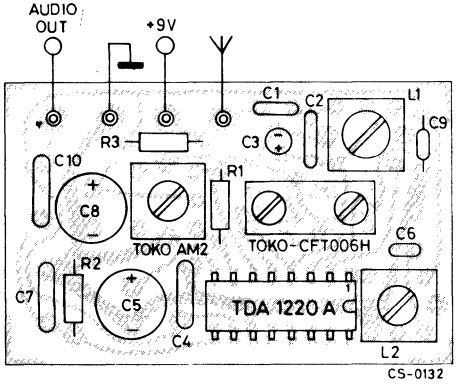
APPLICATION INFORMATION (continued)

Fig. 26 - Low cost 27 MHz receiver



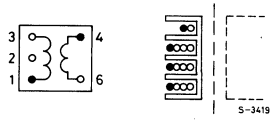
Sensitivity: 10 μV for $(\frac{S+N}{N}) = 26$ dB

Fig. 27 - PC board and component layout of the low cost 27 MHz receiver (1:1 scale)



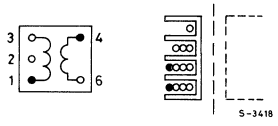
NOTE - For a more detailed description of the TDA 1220A and its applications refer to SGS-TECHNICAL NOTE TN.148.

Fig. 28 - L2 Oscillator Coil



Coil support: Toko 10K.
Primary winding: 10 Turns of enamelled copper wire 0.16 mm diameter (pins 3-1).
Secondary winding: 4 Turns copper wire 0.16 mm diameter (pins 6-4).

Fig. 29 - L1 Antenna Coil



Coil support: Toko 10K.
Primary winding: as L2 (pins 3-1)
Secondary winding: 2 Turns copper wire 0.16 mm diameter (pins 6-4).

TDA1220B

LINEAR INTEGRATED CIRCUIT

AM-FM QUALITY RADIO

The TDA 1220B is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed as an improved version of the TDA 1220A.
It is intended for quality receivers produced in large quantities.
The functions incorporated are:

AM SECTION
- Preamplifier and double balanced mixer (1)
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

FM SECTION
- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA 1220B is suitable up to 30 MHz (*) AM and for FM bands (including 450 KHz narrow band) and features:

- Very constant characteristics (3V to 16V)
- High sensitivity and low noise
- Very low tweet
- Very high signal handling (1V)
- Sensitivity regulation facility (**)
- High recovered audio signal (100 mV) suited for stereo decoders and radio recorders
- Very simple DC switching of AM-FM
- Low current drain

(1) Patent pending.
* Up to 50 MHz with external cristal oscillator.
** Maximum AM sensitivity can be reduced by mean of a resistor (5 to 12 KΩ) between pin 4 and ground.

ADVANCE DATA

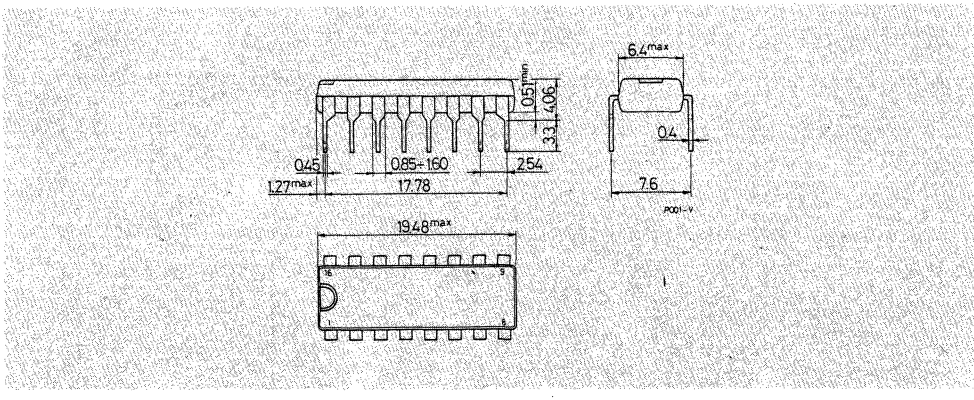
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	16	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$	400	mW
T_{op}	Operating temperature	-30 to 85	°C
T_{stg}, T_j.	Storage and junction temperature	-55 to 150	°C

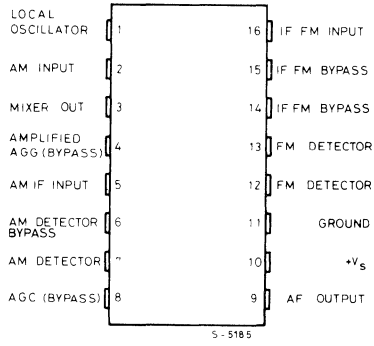
ORDERING NUMBER: TDA 1220B

MECHANICAL DATA

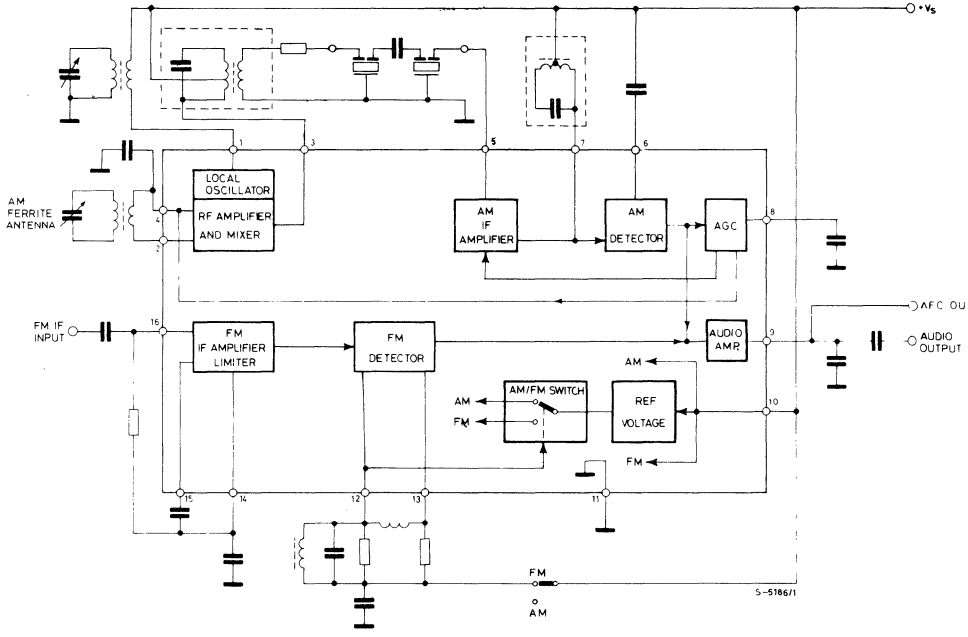
Dimensions in mm



CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s= 9V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			3		16	V
I_d	Drain current				10		mA
AM SECTION(f_o = 1 MHz; f_m= 1 KHz)							
V_i	Input sensitivity	S/N = 26 dB	m = 0.3		12	25	μV
S/N		V_i = 10 mV	m = 0.3		52		dB
V_i	AGC eange	ΔV_{out}= 10 dB	m = 0.8		100		dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3	65	120		mV
d	Distortion				0.4		%
V_H	Max input signal handling capability	m = 0.8	d < 10%		1		V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)				7		KΩ
	Tweet 2 IF	m = 0.3	V_i = 1 mV		38		dB
	Tweet 3 IF				55		dB
FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)							
V_i	Input limiting voltage	-3 dB limiting point			22		μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3		52		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz	V_j = 1 mV		64		dB
d	Distortion	Δf = ± 75 KHz	V_i = 1 mV		0.7		%
d	Distortion	Δf = ± 22.5	V_i = 1 mV		0.25		%
d	Distortion (double tuned)				0.1		%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV	65	100		mV
R_i	Input resistance between pin 16 and ground	Δf = 0			6.5		KΩ
C_i	Input capacitance between pin 16 and ground	Δf = 0			14		pF
R_o	Output resistance (pin 9)				7		KΩ

Fig. 1 - Test circuit

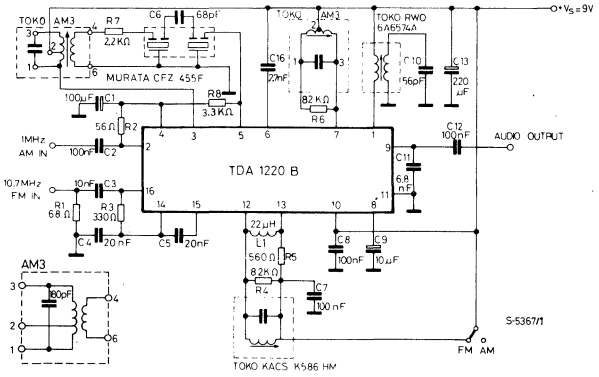


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.

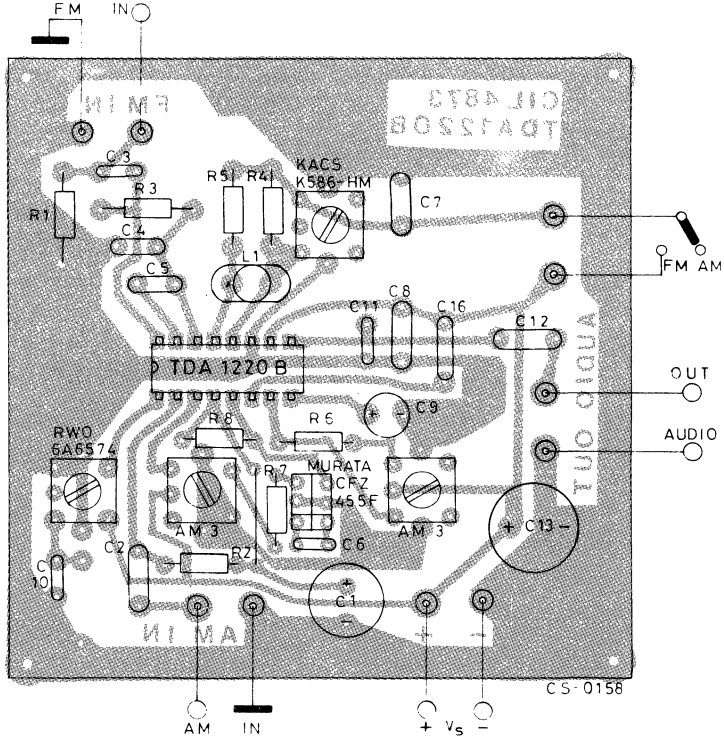


Fig. 3 - Suggestion for 7 x 7 mm "LC" conventional filter use.

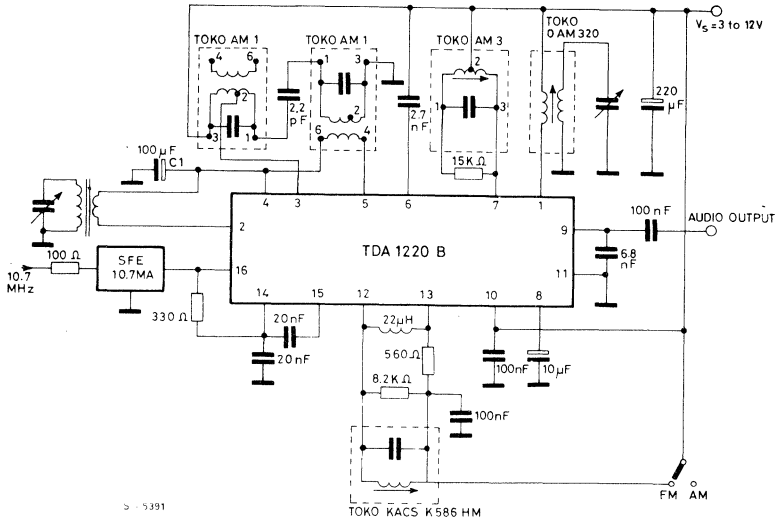
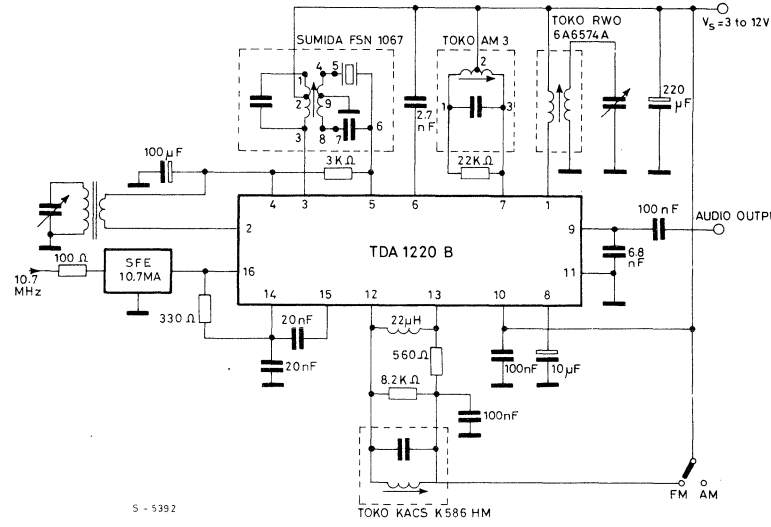


Fig. 4 - Suggestion for "coil block" use.



LINEAR INTEGRATED CIRCUIT

TDA1220L

LOW VOLTAGE AM-FM RADIO

The TDA 1220L is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in 3V-4.5V-6V portable AM-FM radio receivers.
The functions incorporated are:

AM SECTION

- Preamplifier and double balanced mixer*
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

FM SECTION

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA 1220L is suitable up to 30 MHz AM and for FM bands and features:

- High sensitivity and low noise
- Very low **tweet**
- High signal handling (1V)
- Low battery drain
- AM sensitivity regulation facility
- High stability of electrical characteristics from 2V to 9V
- Very simple DC switching of AM-FM

* Patent pending.

ADVANCE DATA

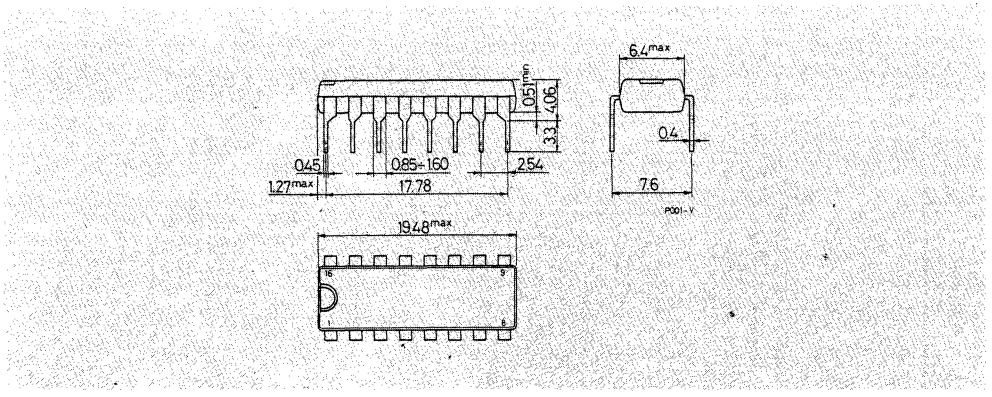
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	12	V
P_{tot}	Total power dissipation at $T_{amb} < 110°C$	400	mW
T_{op}	Operating temperature	-20 to 85	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C

ORDERING NUMBER: TDA 1220L

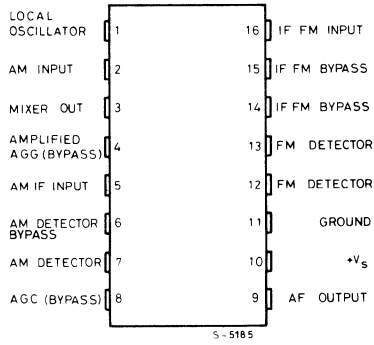
MECHANICAL DATA

Dimensions in mm

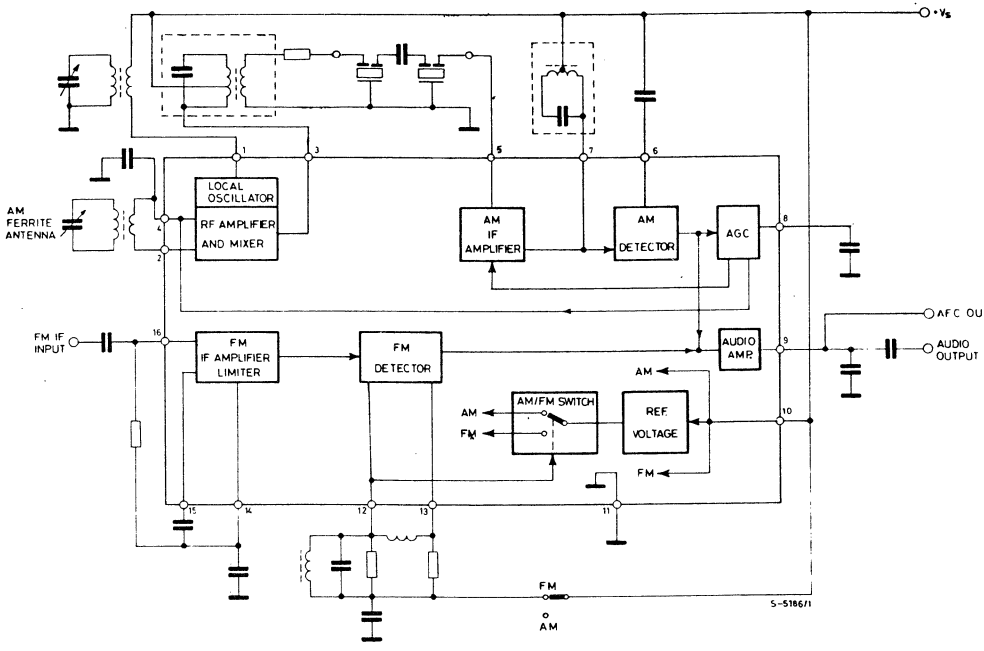


TDA1220L

CONNECTION DIAGRAM



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_s = 4.5V unless otherwise specified, refer to test circuit)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Operating supply voltage			2		9	V
I_d	Drain current				10		mA

AM SECTION (f_o = 1 MHz; f_m = 1 KHz)

V_i	Input sensitivity	S/N = 26 dB	m = 0.3		15		μV
S/N		V_i = 10 mV	m = 0.3		52		dB
V_i	AGC range	ΔV_{out} = 10 dB	m = 0.8		100		dB
V_o	Recovered audio signal (pin 9)	V_i = 1 mV	m = 0.3		80		mV
d	Distortion				0.4		%
V_H	Max input signal handling capability	m = 0.8	d < 10%		1		V
R_i	Input resistance between pins 2 and 4	m = 0			7.5		KΩ
C_i	Input capacitance between pins 2 and 4	m = 0			18		pF
R_o	Output resistance (pin 9)				5		KΩ
	Tweet 2 IF	m = 0,3	V_i = 1 mV		40		dB
	Tweet 3 IF				55		dB

FM SECTION (f_o = 10.7 MHz; f_m = 1 KHz)

V_i	Input limiting voltage	-3 dB limiting point			20		μV
AMR	Amplitude modulation rejection	Δf = ± 22.5 KHz V_i = 3 mV	m = 0.3		50		dB
S/N	Ultimate quieting	Δf = ± 22.5 KHz	V_i = 1 mV		70		dB
d	Distortion	Δf = ± 22.5 KHz	V_i = 1 mV		0.3		%
V_o	Recovered audio signal (pin 9)	Δf = ± 22.5 KHz	V_i = 1 mV		80		mV
R_i	Input resistance between pin 16 and ground	Δf = 0			6.5		KΩ
C_i	Input capacitance between pin 16 and ground	Δf = 0			14		pF
R_o	Output resistance (pin 9)				5		KΩ

Fig. 1 - Test circuit

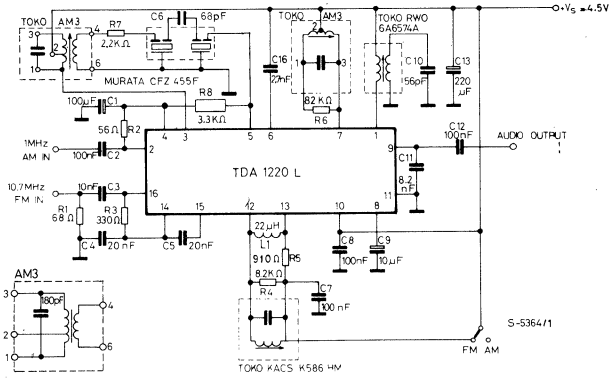


Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.

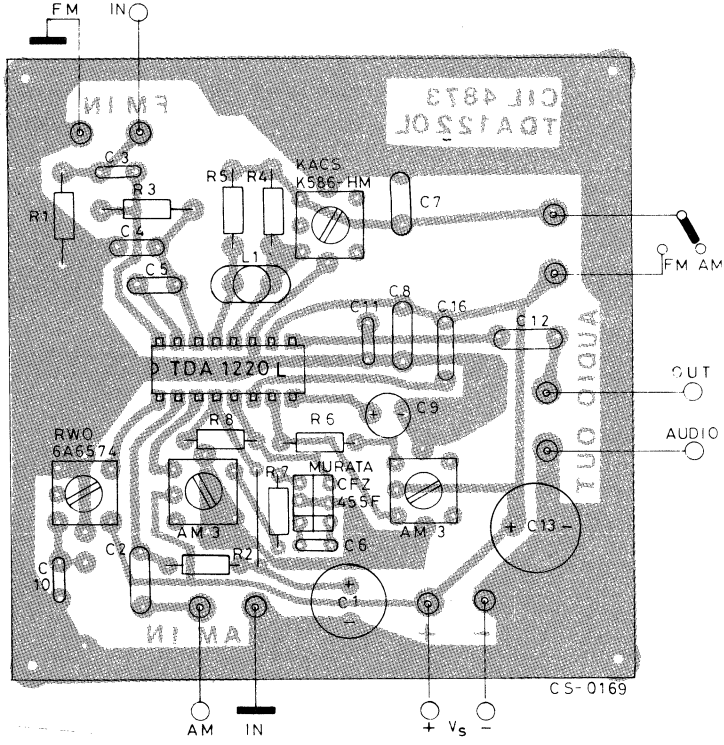


Fig. 3 - Suggestion for varicap tuned receiver.

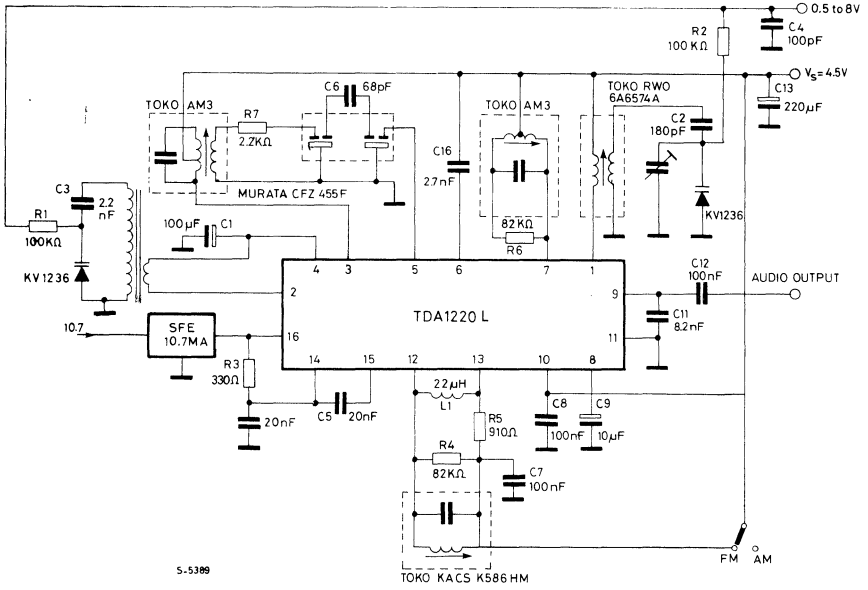
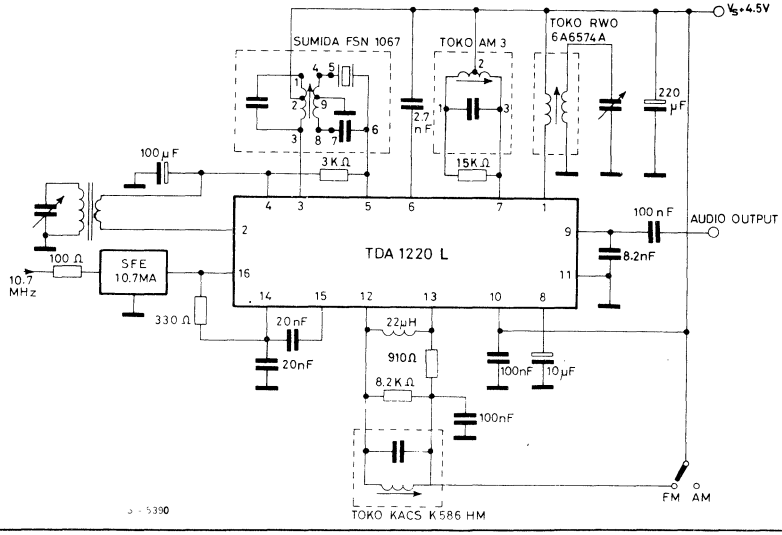


Fig. 4 - Suggestion for "coil block" use



TDA1470

LINEAR INTEGRATED CIRCUIT

TV VERTICAL DEFLECTION SYSTEM

The TDA 1470 is a monolitic integrated circuit in a 16-lead dual in-line plastic package with or without external bar. It is intended for direct driving of colour TV yokes, but it offers a wide application range also in BW TVs, monitors and displays.
The functions incorporated are:

- Synchronization circuit
- Oscillator and ramp generator
- Power amplifier with high current capability
- Flyback generator
- Voltage regulator

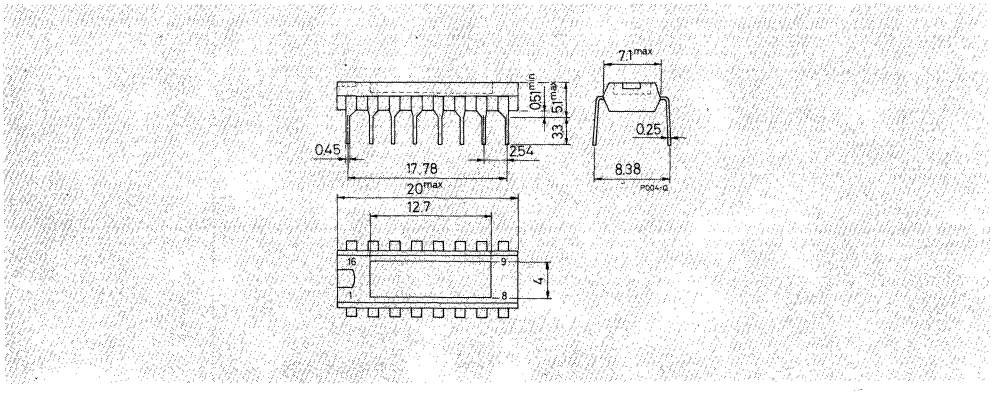
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage at pin 3	35	V
V_{14}, V_{16}	Flyback peak voltage	60	V
V_7, V_8	Power amplifier input voltage	+10	V
		-0.5	V
I_o	Output peak current (non repetitive) at t = 2 ms	3	A
I_o	Output peak current at f = 50 Hz, $t \leqslant 10\,\mu s$	3.5	A
I_o	Output peak current at f = 50 Hz, $t > 10\,\mu s$	2	A
I_2	Pin 2 D.C. current at $V_{16} < V_3$	100	mA
I_2	Pin 2 peak to peak flyback current for f = 50 Hz, $t_{fly} \leqslant 1.5$ ms	3	A
I_{11}	Pin 11 current	20	mA
P_{tot}	Maximum power dissipation at $T_{case} \leqslant 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

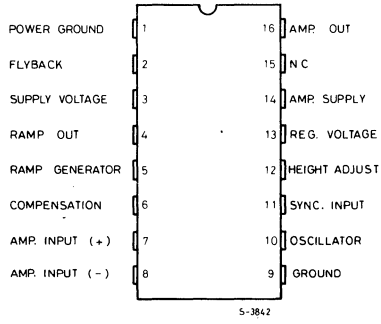
ORDERING NUMBER: TDA 1470

MECHANICAL DATA

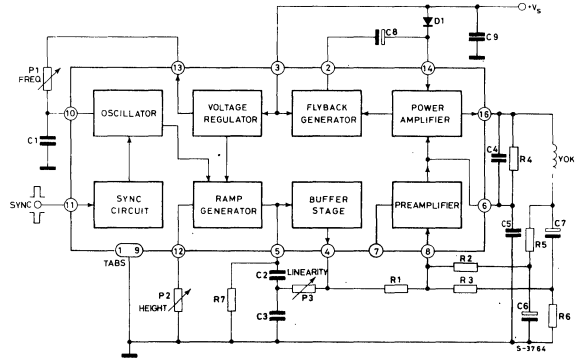
Dimensions in mm



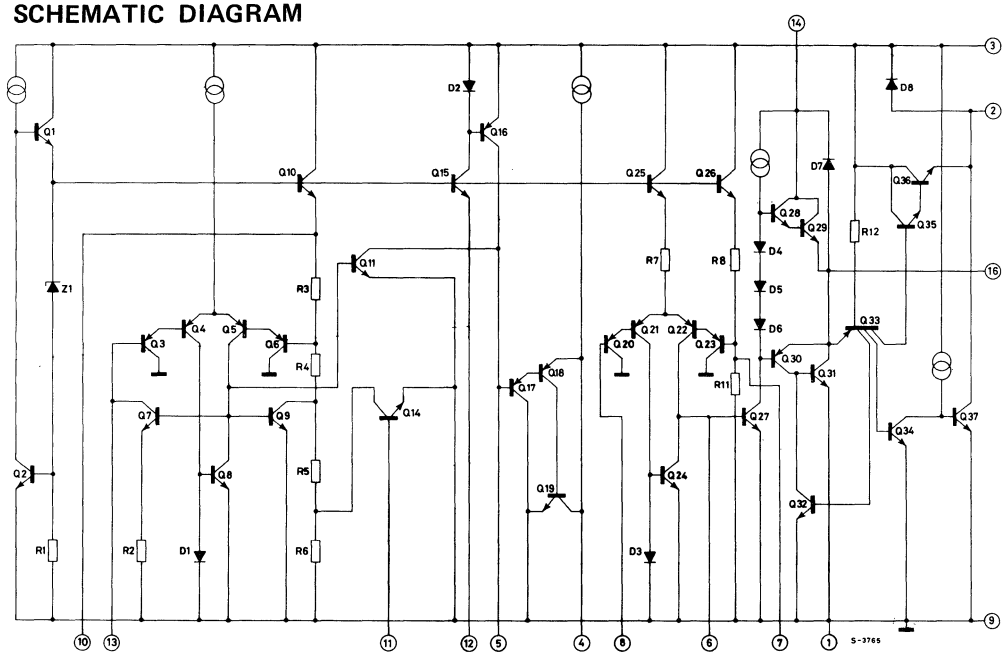
CONNECTION AND BLOCK DIAGRAMS
(top view)



The copper slug is electrically connected to pin 9 (substrate)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

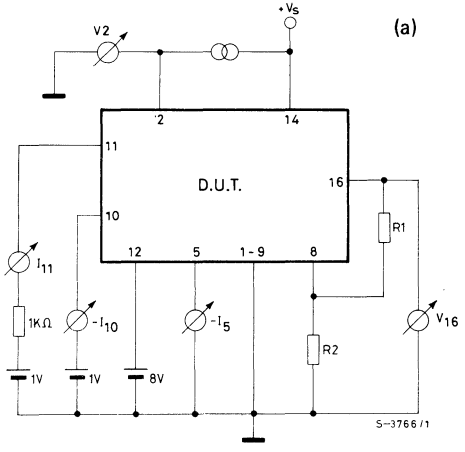
DC ELECTRICAL CHARACTERISTICS (Refer to the DC test circuits, $V_s = 35V$, $T_{amb} = 25°C$, unless otherwise specified)

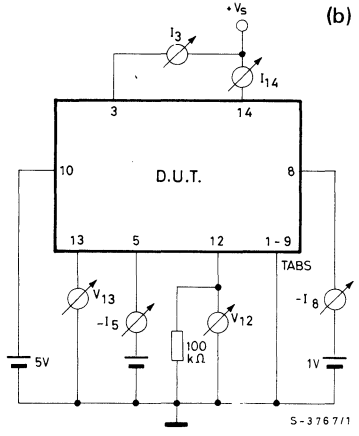
Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_3	Pin 3 quiescent current	$I_2 = 0$		7		mA	1b
I_{14}	Pin 14 quiescent current	$I_{16} = 0$		10		mA	1b
$-I_{10}$	Oscillator bias current	$V_{10} = 1V$		0.1		μA	1a
$-I_8$	Amplifier input bias current	$V_8 = 1V$		1		μA	1b
$-I_5$	Ramp generator bias current	$V_5 = 0V$		0.02		μA	1a
$-I_5$	Ramp generator current	$V_5 = 0V$ $I_{12} = 20\ \mu A$		20		μA	1b
$\frac{\Delta I_5}{I_5}$	Ramp generator linearity	$\Delta V_5 = 0$ to 12V $I_{12} = 20\ \mu A$		0.2	1	%	1b
V_s	Supply voltage range(pin3)		10		35	V	–
V_4	Pin 4 saturation voltage to ground	$I_4 = 1$ mA		1	1.4	V	–
V_2	Pin 2 saturation voltage to ground	$I_2 = 10$ mA		0.5		V	1a
V_{16}	Quiescent output voltage	$V_s = 10V$ $R_1 = 10K\Omega$ $R_2 = 10\ K\Omega$	4.15	4.45	4.73	V	1a
		$V_s = 35V$ $R_1 = 30\ K\Omega$ $R_2 = 10\ K\Omega$	8.3	8.9	9.45	V	1a
V_{16L}	Output saturation voltage to ground	$-I_{16} = 0.8A$		1.3		V	1c
		$-I_{16} = 1.5A$		1.7		V	1c

D.C. ELECTRICAL CHARACTERISTICS (continued)

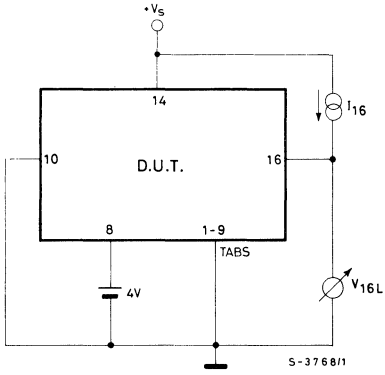
Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
V_{16H}	Output saturation voltage to supply	I_{16}= 0.8A		1.9		V	1d
		I_{16}= 1.5A		2.3		V	1d
V_{13}	Regulated voltage at pin 13		6.1	6.5	6.9	V	1b
V_{12}	Regulated voltage at pin 12	I_{12}= 20 μA	6.2	6.5	7	V	1b
$\frac{\Delta V_{13}}{\Delta V_s}$; $\frac{\Delta V_{12}}{\Delta V_s}$	Regulated voltages drift	ΔV_s= 10 to 35V		1		mV/V	1b
V_7	Amplifier input reference voltage		2.07	2.2	2.3	V	

Fig. 1 - DC test circuits

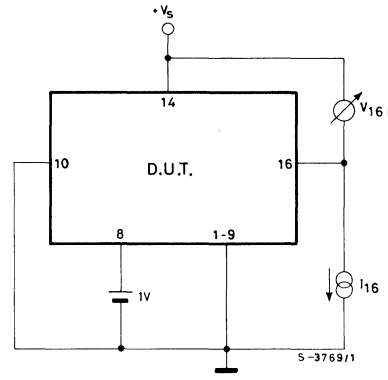




(c)



(d)



AC ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit f = 50 Hz, V_s = 24V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Operating supply voltage	$I_{y\ max}$= 2.2 App		24		V
I_s	Supply current	I_y = 2 App		270		mA
I_{11}	Sync. input current		500			μA
V_{16}	Flyback voltage	I_y = 2 App		49		V
V_{10}	Peak to peak oscillator sawtooth voltage			2.4		V
t_{fly}	Flyback time	I_y = 2 App		0.6		ms
f_o	Free running frequency	R_1+P_1 = 300 KΩ C_2 = 100 nF		44		Hz
		R_1+P_1 = 260 KΩ C_2 = 100 nF		52		Hz
Δf	Synchronization range	I_{11}= 500 μA	14			Hz
$\frac{\Delta f}{\Delta V_s}$	Frequency drift vs. supply voltage	V_s= 10 to 35V		0.005		Hz/V
$\frac{\Delta f}{\Delta T_{tab}}$	Frequency drift vs. tab temperature	T_{amb}= 40 to 120 °C		0.01		Hz/°C

Fig. 2 - AC Test circuit

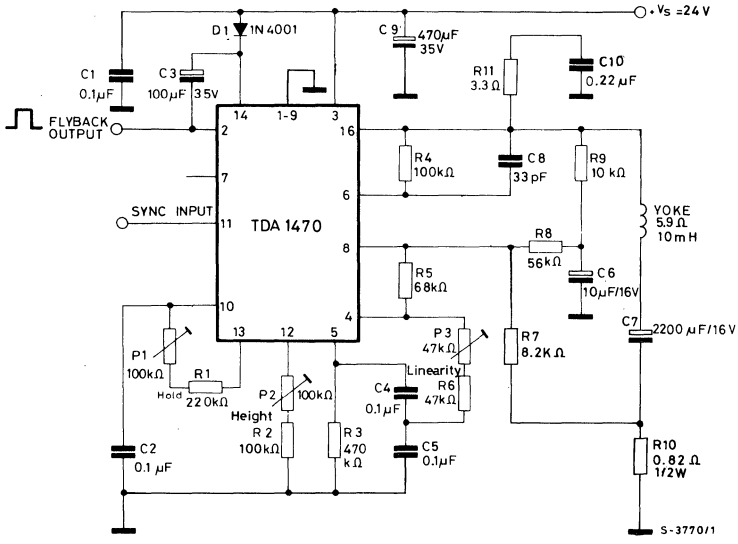


Fig. 3 - Relative output voltage drift vs. supply voltage

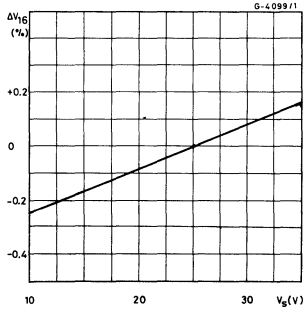


Fig. 4 - Relative output voltage drift vs. case temperature

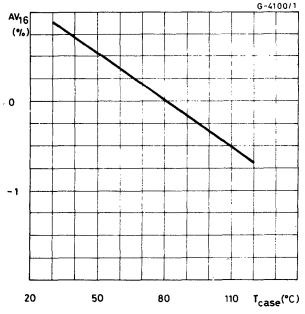


Fig. 5 - Output saturation voltage vs. output current

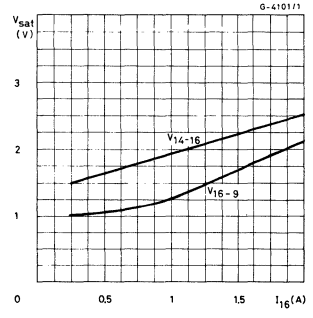
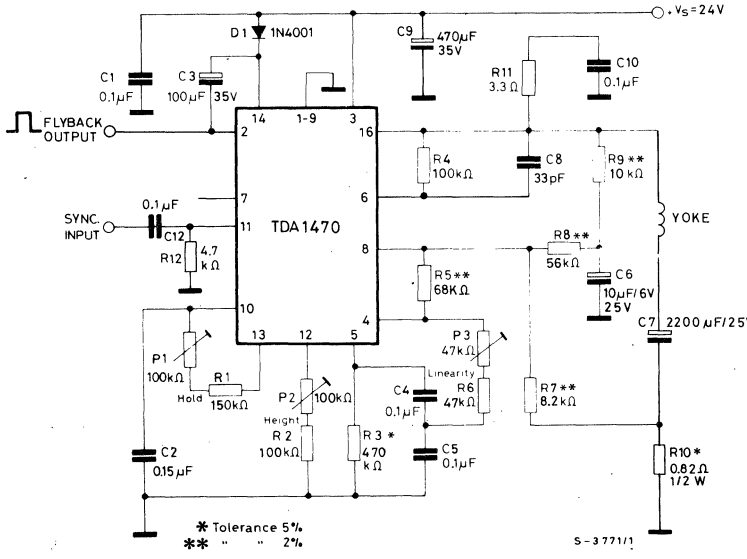


Fig. 6 - Application circuit for large screen 110° TVC set (R_y= 5.9Ω; L_y= 10 mH; I_y= 1.95 App)

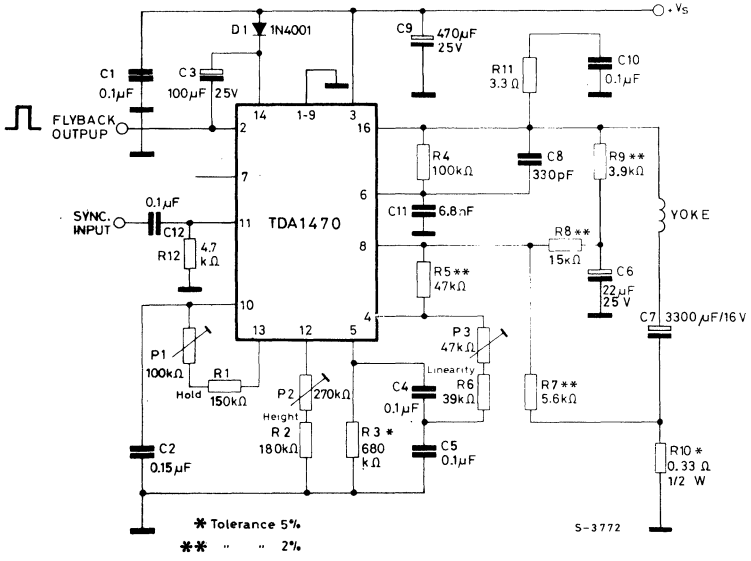


Typical performance

V_s	Operating supply voltage	24	V
I_s	Supply current	300	mA
t_{fly}	Flyback time	0.7	ms
P_d	TDA 1470 power dissipation	4	W
I_y	Maximum scanning current	2.3	App

For safe operation up to T_{amb}= 60°C a heatsink of R_{th}= 7°C/W is required.

Fig. 7 - Application circuit for PIL 26" -110° parallel connected ($R_y = 2.5\Omega$; $L_y = 6.6$ mH; $I_y = 2.36$ App)

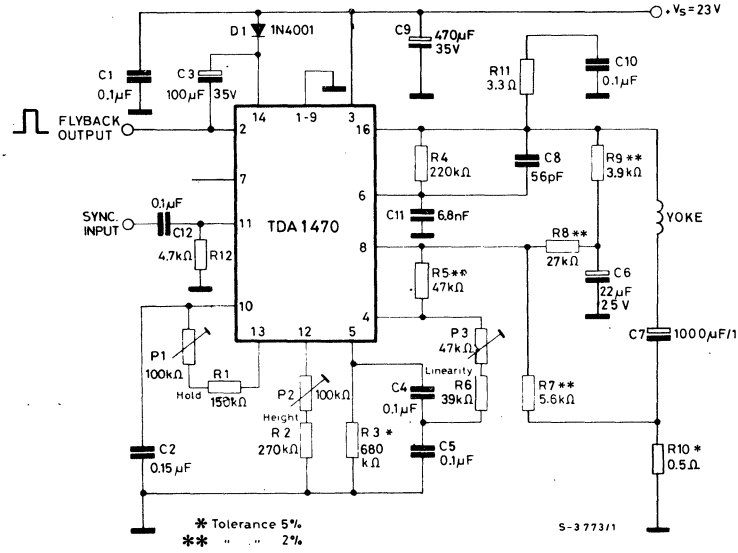


Typical performance

V_s	Operating supply voltage	16	V
I_s	Supply current	345	mA
t_{fly}	Flyback time	0.85	ms
P_d	TDA 1470 power dissipation	3.5	W
I_y	Maximum scanning current	2.5	App

For safe operation up to $T_{amb} = 60°C$ a heatsink of $R_{th} = 8$ °C/W is required.

Fig. 8 - Application circuit for PIL 26" -110° series connected (R_y=9.7Ω; L_y=26.4 mH; I_y=1.18 App)

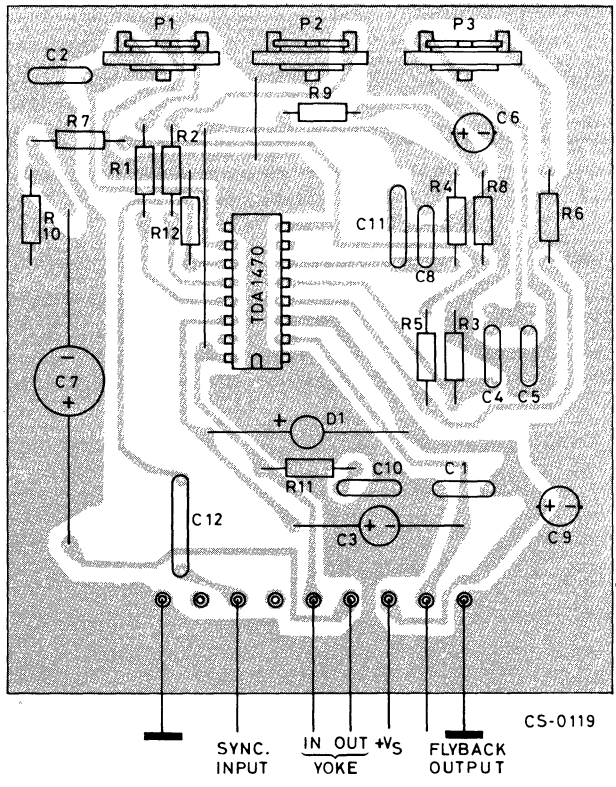


Typical performance

V_s	Operating supply voltage	23	V
I_s	Supply current	185	mA
t_{fly}	Flyback time	1	ms
P_d	TDA 1470 power dissipation	2.8	W
I_y	Maximum scanning current	1.4	App

For safe operation up to T_{amb}= 60°C a heatsink of R_{th}= 10 °C/W is required.

Fig. 9 - P.C. board and component layout (Application circuits of fig. 6, 7 and 8)

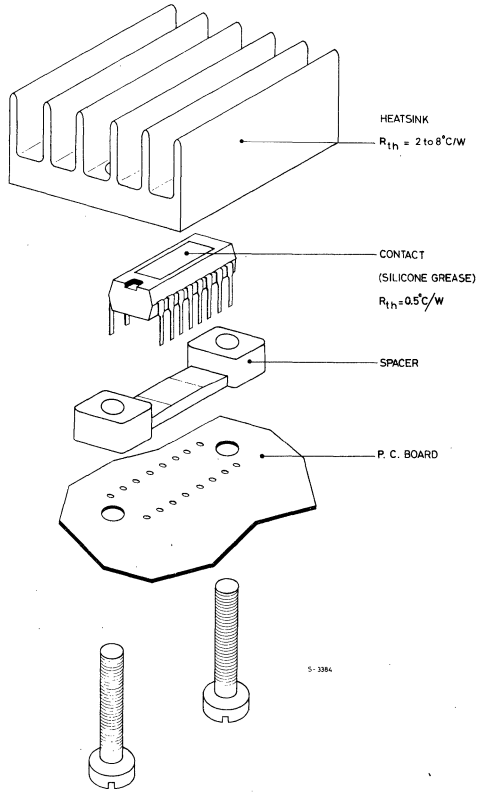


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink as shown in fig. 10. The system for attaching the heatsink is very simple; it uses a plastic spacer which is supplied with the device on request (TDA 1470 F2).
Thermal contact between the copper slug (of the package) and the heatsink is guaranteed by the pressure which the screws exert via the printed circuit board; this is due to the particular shape of the spacer.

Note: The most negative supply voltage is connected to the copper slug, hence to the heatsink (because it is in contact with the slug).

Fig. 10 - Mounting system example (TDA 1470)



LINEAR INTEGRATED CIRCUIT

TDA1670

PRELIMINARY DATA

VERTICAL DEFLECTION CIRCUIT

The TDA 1670 is a monolithic integrated circuit in 15-lead Multiwatt® package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, BW TVs, monitors and displays. The functions incorporated are.

- Synchronization circuit
- Precision oscillator and ramp generator
- Power output amplifier with high current capability
- Flyback generator
- Voltage regulator
- Precision blanking pulse generator
- Thermal shut down protection
- CRT screen protection circuit which blanks the beam current in the event of loss of vertical deflection current.

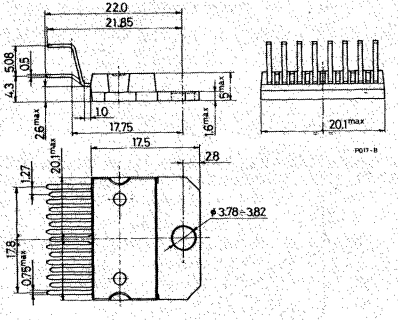
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage at pin 14	35	V
V_1, V_2	Flyback peak voltage	60	V
V_5	Sync. input voltage	20	V
V_{11},V_{12}	Power amplifier input voltage	$\begin{cases} V_s \\ -10 \end{cases}$	V
V_{13}	Voltage at pin 13	V_s	
I_o	Output current (non repetitive) at t = 2 msec	3	A
I_o	Output peak current at f = 50 Hz t > 10 μsec	2	A
I_o	Output peak current at f = 50 Hz t ⩽ 10 μsec	3.5	A
I_{15}	Pin 15 peak to peak flyback current at f = 50 Hz, t_{fly} ⩽ 1.5 msec	3	A
I_{15}	Pin 15 DC current at $V_1 < V_{14}$	100	mA
P_{tot}	Maximum power dissipation at T_{case} ⩽ 60°C	30	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1670

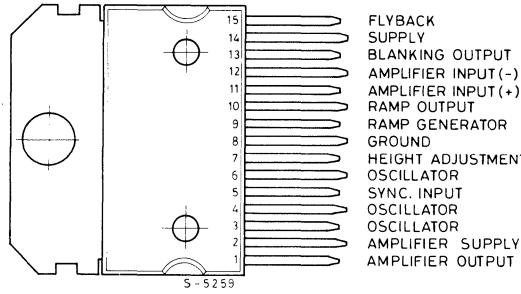
MECHANICAL DATA

Dimensions in mm

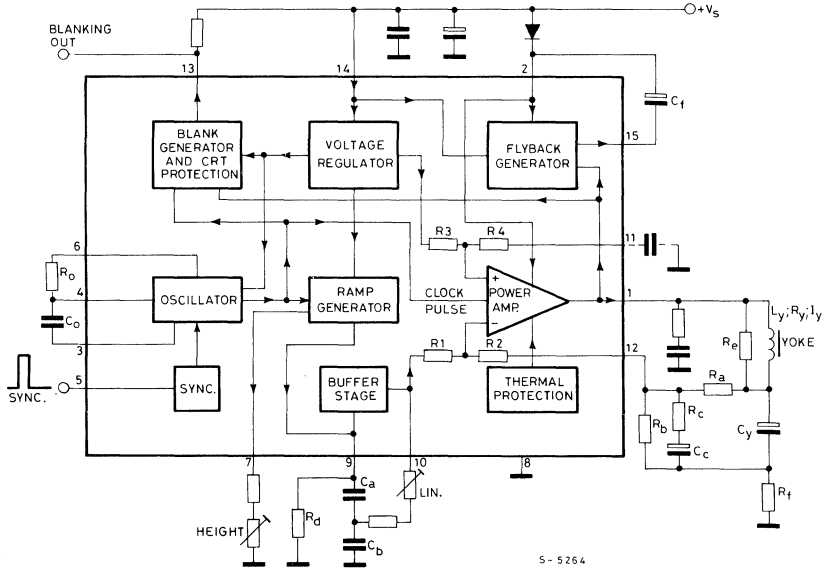


TDA1670

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	40	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 35V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
I_2	Pin 2 quiescent current	I_1= 0		18	30	mA	1b
$-I_9$	Ramp generator bias current	V_9= 0		0.02	1	μA	1b
$-I_9$	Ramp generator current	V_9= 0; $-I_7$= 20 μA	18.5	20	21.5	μA	1b
$\lvert\frac{\Delta I_9}{I_9}\rvert$	Ramp generator non linearity	ΔV_9= 0 to 15V $-I_7$= 20 μA		0.2	1	%	1b
I_{14}	Pin 14 quiescent current			25	50	mA	1b
V_1	Quiescent output voltage	V_s= 35V; R_a= 2.2 KΩ R_b= 1 KΩ	16.8	17.8	18.6	V	1a
		V_s= 15V; R_a= 390Ω R_b= 1 KΩ	7	7.5	8	V	
V_{1L}	Output saturation voltage to ground	I_1= 1.2A		1	1.4	V	1c
V_{1H}	Output saturation voltage to supply	$-I_1$= 1.2A		1.6	2.2	V	1d
V_4	Oscillator virtual ground			0.45		V	1b
V_7	Regulated voltage at pin 7	$-I_7$= 20 μA	6.3	6.6	7.1	V	1b
$\frac{\Delta V_7}{\Delta V_s}$	Regulated voltage drift with supply voltage	ΔV_s= 15 to 35V		1		$\frac{mV}{V}$	1b
V_{11}	Amplifier input (+) reference voltage		4.2	4.4	4.6	V	1b
V_{13}	Blanking output saturation voltage	I_{13}= 10 mA		0.35		V	1a
V_{15}	Pin 15 saturation voltage to ground	I_{15}= 20 mA		1	1.3	V	1a

Fig. 1 - DC test circuit

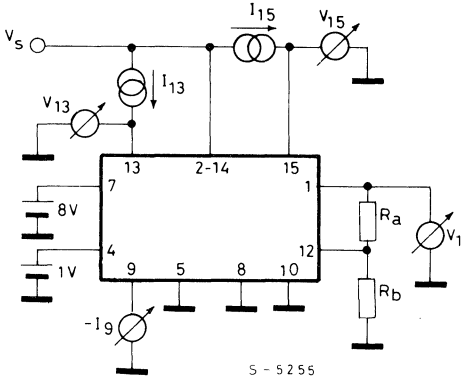


Fig. 1a

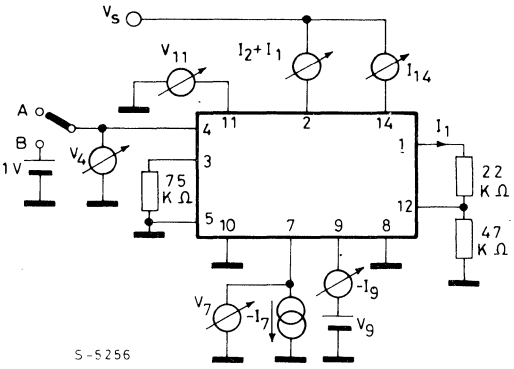


Fig. 1b

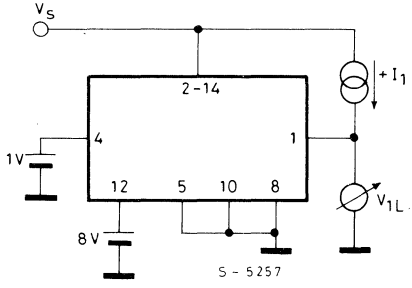


Fig. 1c

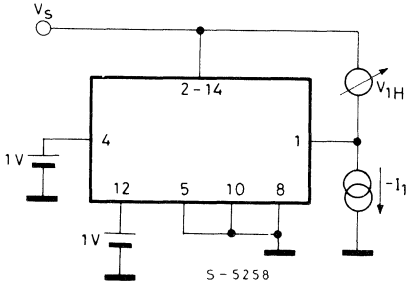


Fig. 1d

ELECTRICAL CHARACTERISTICS (Refer to the A.C. test circuit of fig. 2, T_{amb} = 25°C, V_s = 24V, f = 50 Hz, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
AC CHARACTERISTICS							
I_s	Supply current	I_y = 2 App			295		mA
I_5	Sync input current required to sync.			100			μA
v_1	Flyback voltage	I_y = 2 App			50		V
v_3	Peak to peak oscillator sawtooth voltage	I_5 = 0			3.6		V
		I_5 = 100 μA			3.4		V
V_{10thL}	Start scan level of the input ramp				1.85		V
t_{fly}	Flyback time	I_y = 2 App			0.6		ms
t_{blank}	Blanking pulse duration	f_o = 50 Hz	T_j = 75°C		1.4		ms
		f_o = 60 Hz	T_j = 75°C		1.17		ms
f_o	Free running frequency	R_o = 7.5 KΩ C_o = 330 nF	T_j = 75°C		43.5		Hz
		R_o = 6.2 KΩ C_o = 330 nF	T_j = 75°C		52.5		Hz
Δf	Synchronization range	I_5 = 100 μA	T_j = 75°C		16		Hz
T_j	Junction temperature for thermal shut-down				145		°C

Fig. 2 - AC test circuit

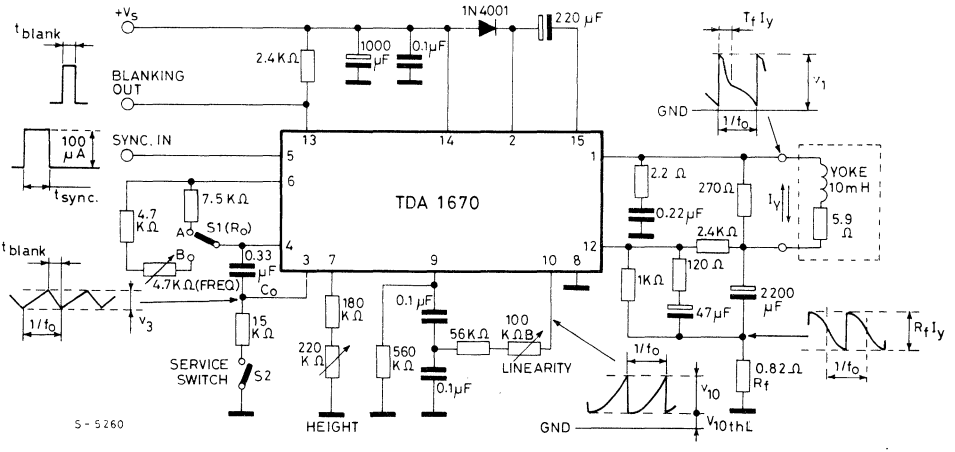
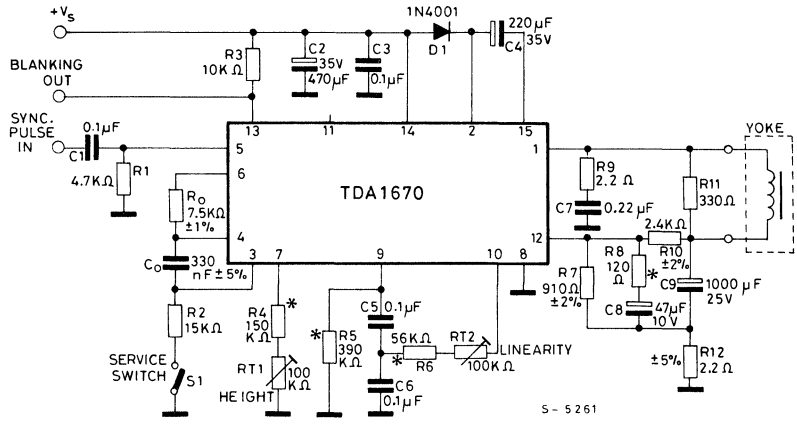


Fig. 3 - Application circuit for small screen 90° TVC set (Ry= 15Ω ; Ly= 30 mH, Iy= 0.82 App)

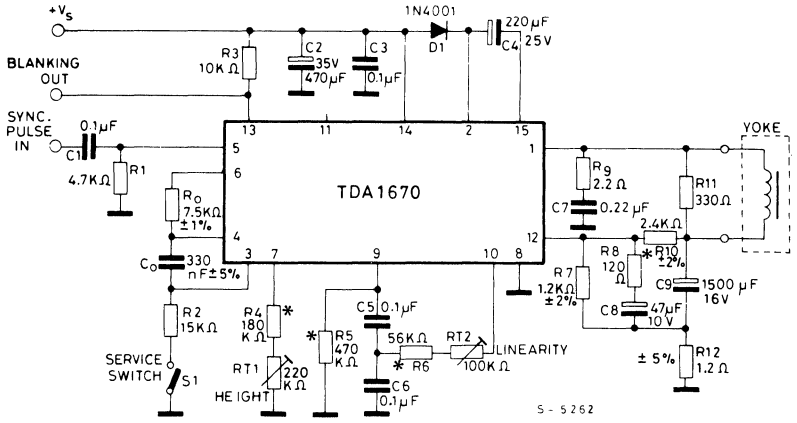


* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	25	V
I_s	Supply current	140	mA
t_{fly}	Flyback time	0.7	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	2.4	W
$R_{th\ heatsink}$	Thermal resistance of the heatsink		
	for T_{amb}= 60°C and $T_{j\ max}$= 110°C	13	°C/W
	for T_{amb}= 60°C and $T_{j\ max}$= 120°C	16	°C/W

Fig. 4 - Application circuit for 110° TVC set (Ry= 9.6Ω ; Ly= 27 mH; Iy= 1.17 App)

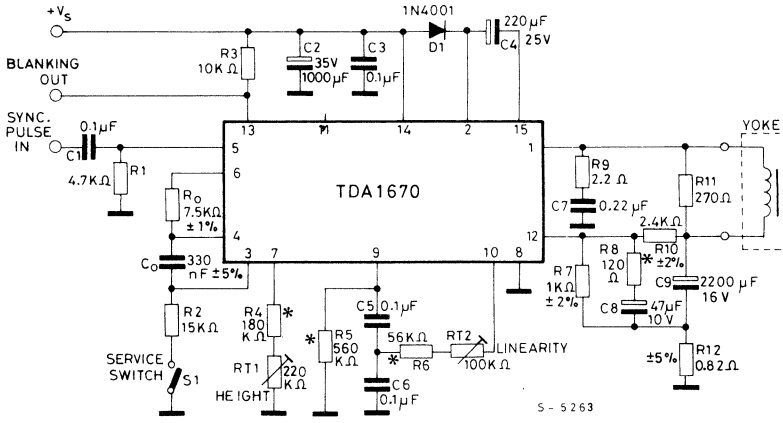


* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	22.5	V
I_s	Supply current	185	mA
t_{fly}	Flyback time	1	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	2.7	W
$R_{th\ heatsink}$	Thermal resistance for the heatsink		
	for T_{amb}= 60°C and $T_{j\ max}$= 110°C	11.5	°C/W
	for T_{amb}= 60°C and $T_{j\ max}$= 120°C	14.5	°C/W

Fig. 5 - Application circuit for 110° TVC set (Ry= 5.9Ω; Ly= 10 mH; Iy= 1.95 App)

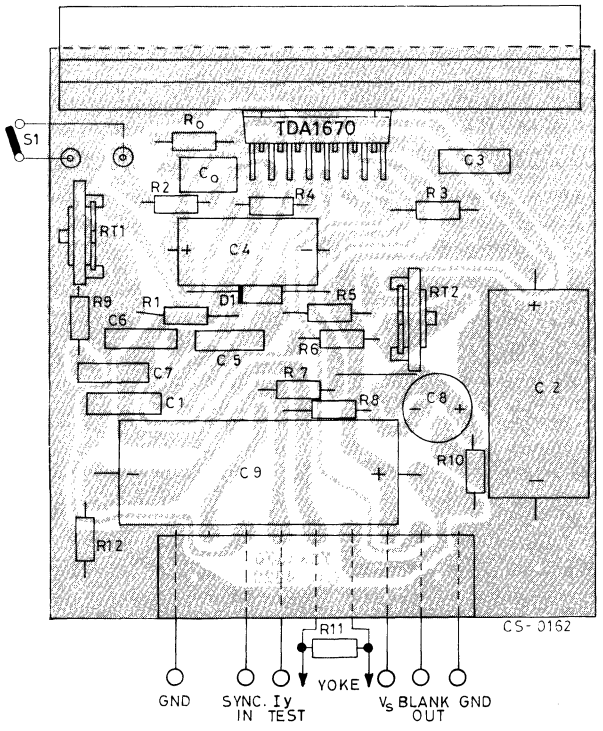


* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	24	V
I_s	Supply current	285	mA
t_{fly}	Flyback time	0.6	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	4.3	W
$R_{th\ heatink}$	Thermal resistance of the heatsink		
	for T_{amb}= 60°C and $T_{j\ max}$= 110°C	6.5	°C/W
	for T_{amb}= 60°C and $T_{j\ max}$= 120°C	8.5	°C/W

Fig. 6 - PC board and components layout for the application circuits of fig. 3, 4 and 5 (1 : 1 scale)



APPLICATION INFORMATION (Refer to the block diagram)

Oscillator and Sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches R_o high or low so allowing the charge or the discharge of C_o under constant current conditions.
The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 4 is the inverting input of the amplifier used as integrator.
Pin 6 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.
Pin 3 is the output of the amplifier.
Pin 5 is the input for sync pulses (positive)

Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.
The internal clock pulse stops the ramp increasing by a very fast discharge of the capacitor; a new voltage ramp is immediately allowed.
The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

Pin 7 The resistance between pin 7 and ground defines the current mirror current and than the height of the scanning.

Pin 9 is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.

Pin 10 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.
The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.
The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 12 is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 12 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

Pin 11 is the non-inverting input and it is not used. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.
This pin is only used on a quasi-bridge configuration.

Pin 1 is the output of the power amplifier and it drives the yoke by a negative slope current ramply. Re and the Boucherot cell are used to stabilize the power amplifier.

Pin 2 The supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_s by a diode, while during the retrace time this pin is supplied from the flyback generator.

Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).
The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 14, the flyback pulse front end drives the flyback

generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.
An integrated diode stops the rising of this output increase and the voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 2).
When the current across the yoke changes its direction, the output of the flyback generator falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.
Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 1) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 15 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 2 (see pin 2).

Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 13 is an open collector output where the blanking pulse is available.

Voltage regulator

The main supply voltage V_s is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 14 is the main supply voltage input V_s (positive).
Pin 8 is the GND pin or the negative input of V_s.

Fig. 7 - Output saturation voltage to ground vs. peak output current

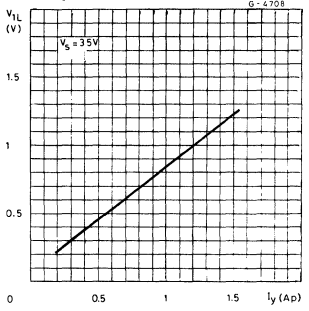


Fig. 8 - Output saturation voltage to supply vs. output peak current

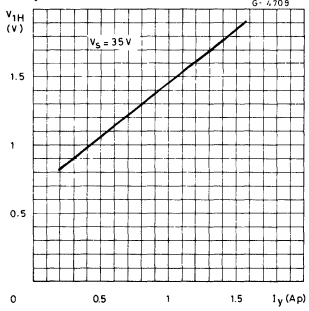
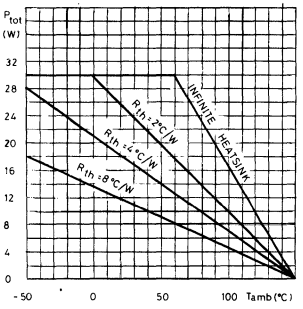


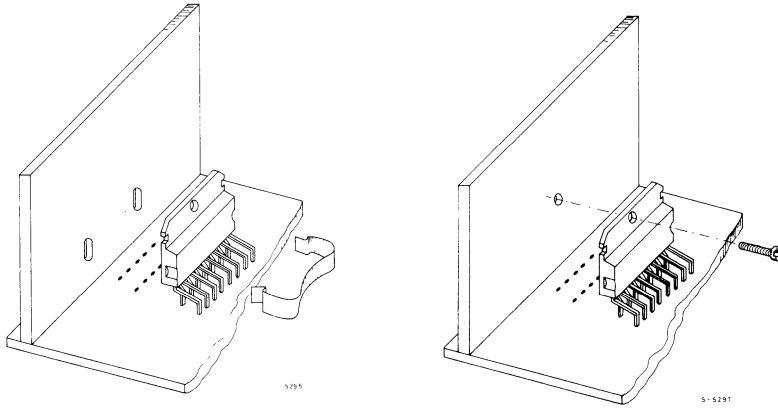
Fig. 9 - Maximum allowable power dissipation vs. ambient temperature



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 10 - Mounting example



LINEAR INTEGRATED CIRCUIT

TDA1770

PRELIMINARY DATA

VERTICAL DEFLECTION CIRCUIT

The TDA 1770 is a monolithic integrated circuit in 20-lead plastic package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke.
It offers a wide range of applications in portable CTVs, BW TVs, monitors and displays. The functions incorporated are:

- synchronization circuit.
- precision oscillator and ramp generator
- power output amplifier
- flyback generator
- voltage regulator
- precision blanking pulse generator
- thermal shut down protection
- CRT screen protection circuit which blanks the beam current in the event of loss of vertical deflection current.

The TDA 1770 is assembled in a new 20-lead plastic package which has 4 centre pins connected together and used for heatsinking.

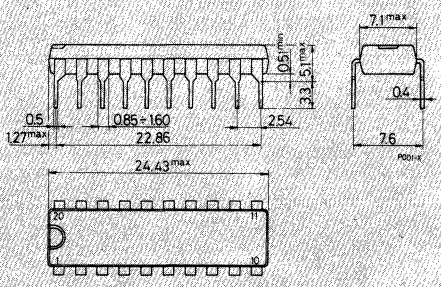
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage at pin 2	35	V
V_7, V_8	Flyback peak voltage	60	V
V_{11}	Sync. input voltage	20	V
V_{19}, V_{20}	Power amplifier input voltage	V_s / -10	V
V_1	Voltage at pin 1	V_s	
I_o	Output current (non repetitive) at t = 2 msec	2	A
I_o	Output peak current at f = 50 Hz t > 10 μsec	1.2	A
I_o	Output peak current at f = 50 Hz t ⩽ 10 μsec	2.2	A
I_3	Pin 3 peak to peak flyback current at f = 50 Hz, t_{fly} ⩽ 1.5 msec	2	A
I_3	Pin 3 DC current at $V_7 < V_2$	50	mA
P_{tot}	Maximum power dissipation: at T_{pins} ⩽ 90°C	4.3	W
	at T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1770

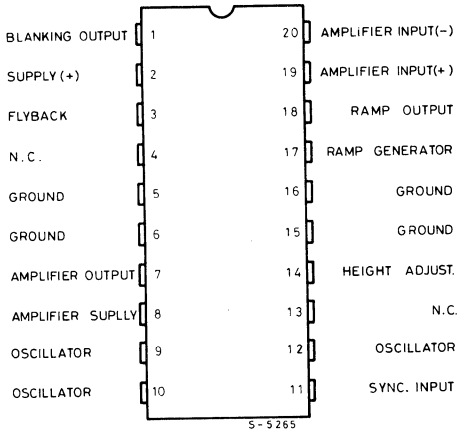
MECHANICAL DATA

Dimensions in mm

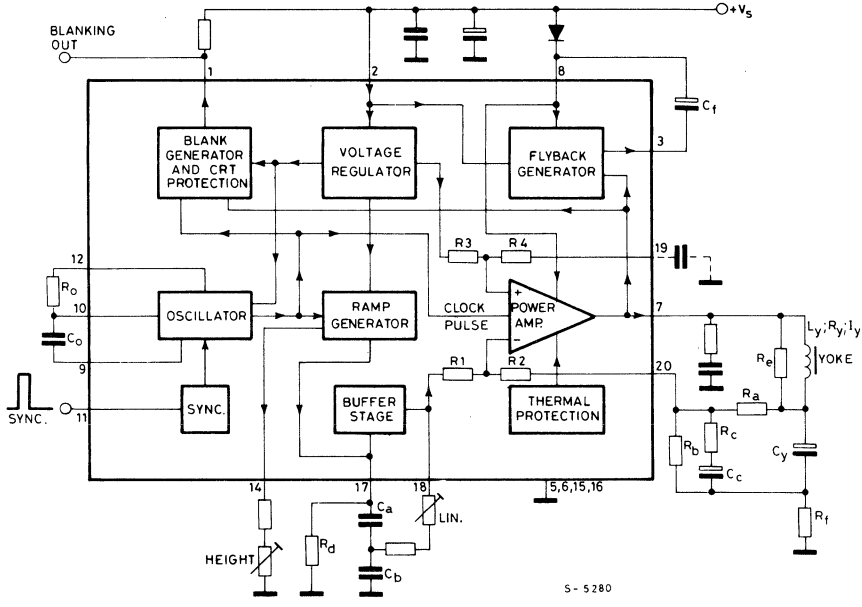


TDA1770

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 35V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
I_2	Pin 2 quiescent current			30	50	mA	1b
I_8	Pin 8 quiescent current	I_7= 0		18	30	mA	1b
$-I_{17}$	Ramp generator bias current	V_{17}= 0		0.02	1	μA	1a
$-I_{17}$	Ramp generator current	V_{17}= 0; $-I_{14}$= 20 μA	18.5	20	21.5	μA	1b
$\left\lvert\frac{\Delta I_{17}}{I_{17}}\right\rvert$	Ramp generator non linearity	ΔV_{17}= 0 to 15V $-I_{14}$= 20 μA		0.2	1	%	1b
V_1	Blanking output saturation voltage	I_1= 10 mA		0.35		V	1b
V_3	Pin 3 saturation voltage to ground	I_3= 20 mA		1	1.3	V	1a
V_7	Quiescent output voltage	V_s= 35V; R_a= 2.2 KΩ R_b= 1 KΩ	16.8	17.8	18.6	V	1a
		V_s= 15V; R_a= 390Ω R_b= 1 KΩ	7.1	7.5	8	V	
V_{7L}	Output saturation voltage to ground	I_7= 0.7A		0.7	1	V	1c
V_{7H}	Output saturation voltage to supply	$-I_7$= 0.7A		1.3	1.8	V	1d
V_{10}	Oscillator virtual ground			0.45		V	1a
V_{14}	Regulated voltage at pin 14	$-I_{14}$= 20 μA	6.3	6.6	7.1	V	1b
$\frac{\Delta V_{14}}{\Delta V_s}$	Regulated voltage drift with supply voltage	ΔV_s= 15 to 35V		1		$\frac{mV}{V}$	1b
V_{19}	Amplifier input (+) reference voltage		4.2	4.4	4.6	V	1b

Fig. 1 - DC test circuit

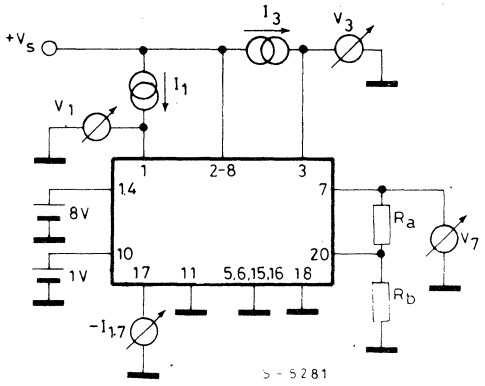


Fig. 1a

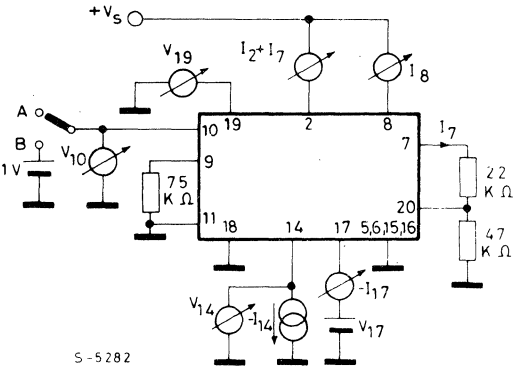


Fig. 1b

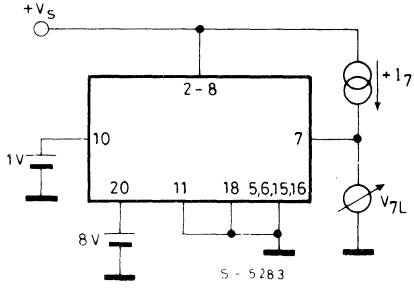


Fig. 1c

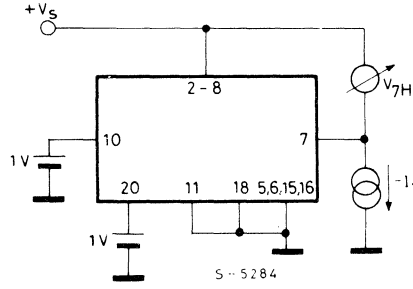


Fig. 1d

ELECTRICAL CHARACTERISTICS (Refer to the A.C. test circuit of fig. 2, V_s= 20V, f= 50 Hz, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
I_s	Supply current	I_y= 1 App		160		mA
I_{11}	Sync. input current		100			μA
V_7	Flyback voltage	I_y= 1 App		42		V
V_9	Peak to peak oscillator sawtooth voltage	I_{11}= 0		3.6		V
		I_{11}= 100 μA		3.4		V
V_{18thL}	Start scan level of the input ramp			1.85		V
t_{fly}	Flyback time	I_y= 1 App		0.75		msec
t_{blank}	Blanking pulse duration	f_o= 50 Hz		1.4		ms
		f_o= 60 Hz		1.17		ms
f_o	Free running frequency	R_o= 7.5 KΩ C_o= 330 nF		43.5		Hz
		R_o= 6.2 KΩ C_o= 330 nF		52.5		Hz
Δf	Synchronization range	I_{11}= 100 μA		16		Hz
T_j	Junction temperature for thermal shut-down			145		°C

Fig. 2 - AC test circuit

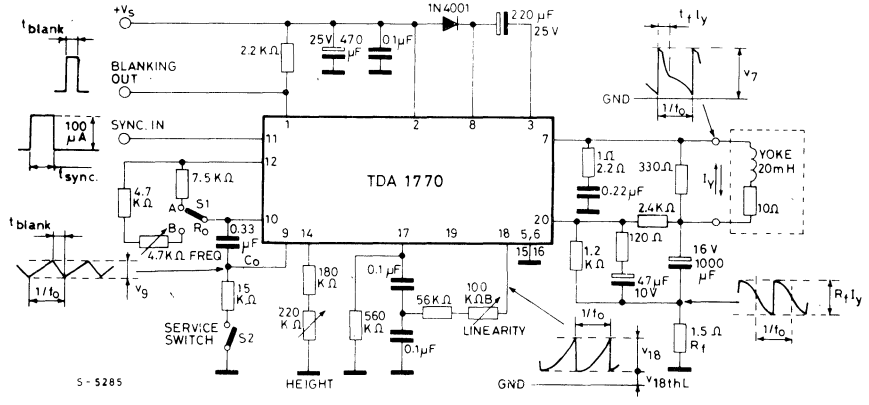
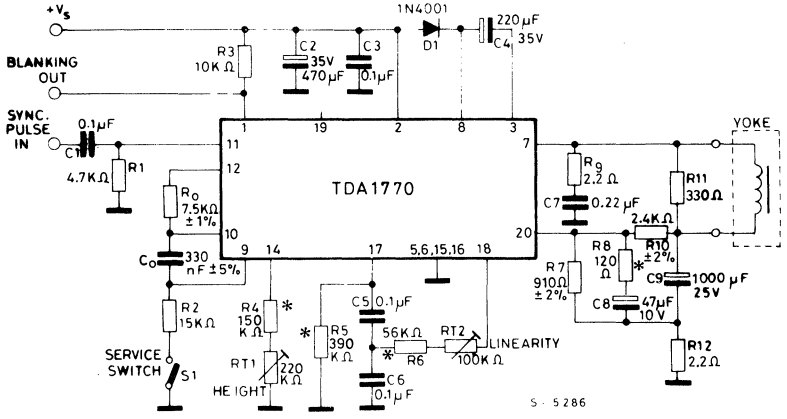


Fig. 3 - Typical application circuit for small screen 90° TVC set (Ry= 15Ω; Ly= 30 mH; Iy= 0.82 App)



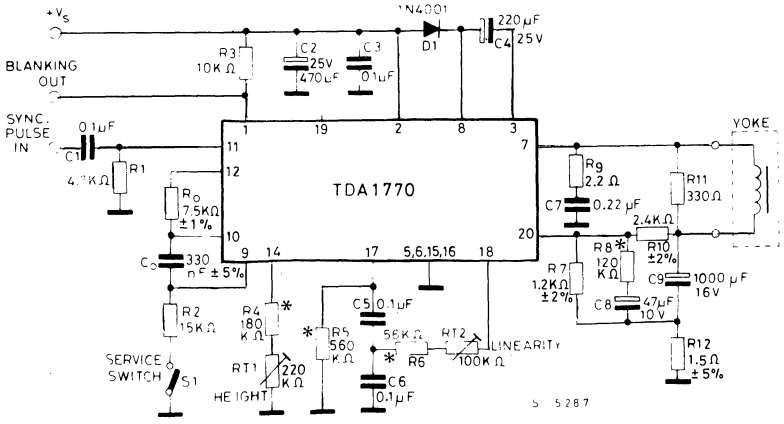
* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	25	V
I_s	Supply current	140	mA
t_{fly}	Flyback time	0.7	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Total dissipation	2.4	W
$R_{th\ heatsink}$ **	Thermal resistance of the heatsink for T_{amb}= 60°C and $T_{j\ max}$= 130°C	8	°C/W

** See "Thermal considerations".

Fig. 4 - Typical application circuit for B/W TV set (Ry= 10Ω; Ly= 20 mH; Iy= 1 App)



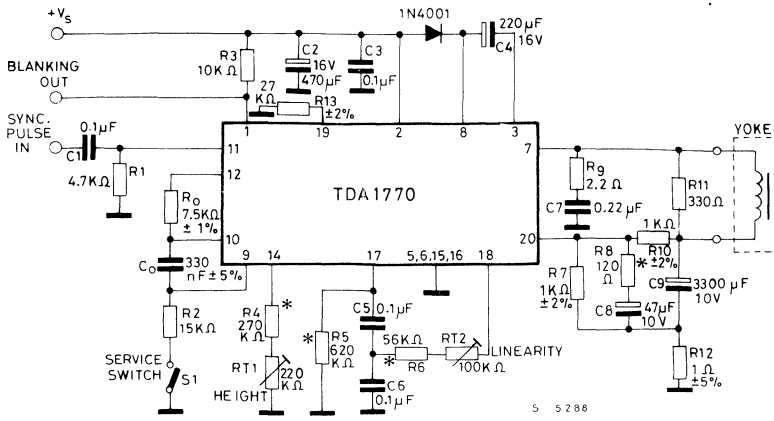
* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	20	V
I_s	Supply current	160	mA
t_{fly}	Flyback time	0.75	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	2.1	W
$R_{th\ heatsink}$ **	Thermal resistance of the heatsink for T_{amb}= 60°C and $T_{j\ max}$= 130°C	11	°C/W

** See "Thermal considerations".

Fig. 5 - Typical application circuit for small screen (Ry= 2.9Ω ; Ly= 6 mH; Iy= 1.1 App)



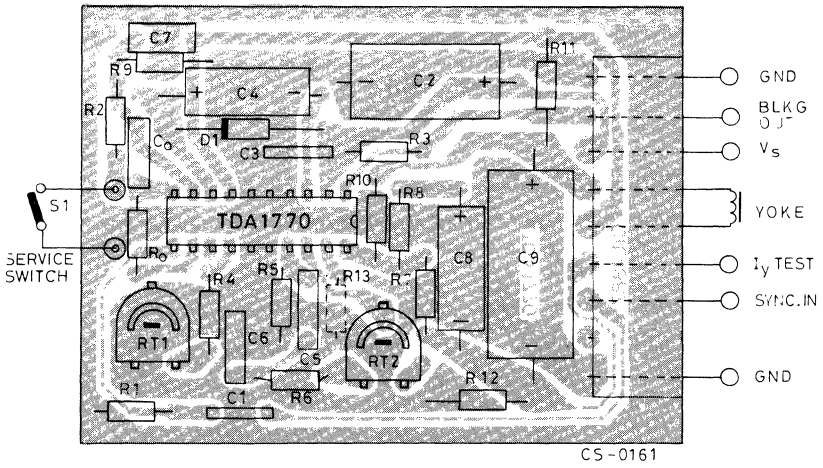
* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	10.5	V
I_s	Supply current	170	mA
t_{fly}	Flyback time	0.45	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	1.25	W
$R_{th\ heatsink}$ **	Thermal resistance of the heatsink for T_{amb}= 60°C and $T_{j\ max}$= 130°C	28	°C/W

** See "Thermal considerations".

Fig. 6 - PC board and components layout for the application circuits of fig. 3, 4 and 5 (1:1 scale)



APPLICATION INFORMATION (Refer to the block diagram)

Oscillator and Sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches Ro high or low so allowing the charge or the discharge of Co under constant current conditions.
The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 10 is the inverting input of the amplifier used as integrator.
Pin 12 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.
Pin 9 is the output of the amplifier.
Pin 11 is the input for sync pulses (positive).

Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.
The internal clock pulse stops the ramp increasing by a very fast discharge of the capacitor; a new voltage ramp is immediately allowed.
The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

Pin 14 The resistance between pin 7 and ground defines the current mirror current and than the height of the scanning.
Pin 17 is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.
Pin 18 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

APPLICATION INFORMATION (continued)

Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.
The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.
The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 20 is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 20 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

Pin 19 is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.
This pin is used on a quasi-bridge configuration or on portable TVS.

Pin 7 is the output of the power amplifier and it drives the yoke by a negative slope current ramp Iy. Re and the Boucherot cell are used to stabilize the power amplifier.

Pin 8 the supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_s by a diode, while during the retrace time this pin is supplied from the flyback generator.

Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).
The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 2, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.
An integrated diode stops the rising of this output increase and voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 8).
When the current across the yoke changes its direction, the output of the flyback generation falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.
Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 7) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 3 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 8 (see pin 8).

Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection.

APPLICATION INFORMATION (continued)

The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 1 is an open collector output where the blanking pulse is available.

Voltage regulator

The main supply voltage V_s is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 2 is the main supply voltage input V_s (positive).
Pin 5, 6, 15, 16 are the GND pins or the negative input of V_s.

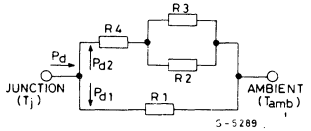
THERMAL CONSIDERATIONS (a note referred to Fig. 3, 4 and 5)

The shown value of case to ambient thermal resistance is the equivalent to three thermal resistances that are:

R1 – Thermal resistance junction to ambient of the device.
R2 – Thermal resistance of the p.c. copper side.
R3 – Thermal resistance of the auxiliary heatsink.

The circuit that contains these thermal resistances is shown on fig. 7 where R3 is the thermal resistance junction to pins of the device and Pd is the maximum dissipated power.

Fig. 7 - Semiconductor heatsink thermal circuit.



Since the thermal resistance R3 of the heatsink is defined from its physical and mechanical characteristics, it is necessary to define the required copper side on the p.c. board for the necessary R2 value. For instance, let's consider the application for the 90° yoke.
It is known:

$T_{j\ max}$= 130°C; $T_{amb\ max}$= 60°C; $R_{th\ c\text{-}amb}$= 8°C/W; $R_{th\ j\text{-}pins}$ (or R4)= 14°C/W; $R_{th\ j\text{-}amb}$= 80°C/W.

It can be calculated:

$$P_d = \frac{T_{j\ max} - T_{amb\ max}}{R_{th\ c\text{-}amb} + R_{th\ j\text{-}pins}} = \frac{130 - 60}{8 + 14} = 3.18W$$

Using an auxiliary heatsink of a thermal resistance R3= 20°C/W (including some losses), it can be easily calculated (see fig. 7): R2 = 94°C/W.
From fig. 9, it can be found: $\ell \geqslant 21$ mm.

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the TDA 1770 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 8) or to an external heatsink.
The diagram of figure 9 shows the R_{th} as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 8 - Example of P.C. board copper area which is used as heatsink.

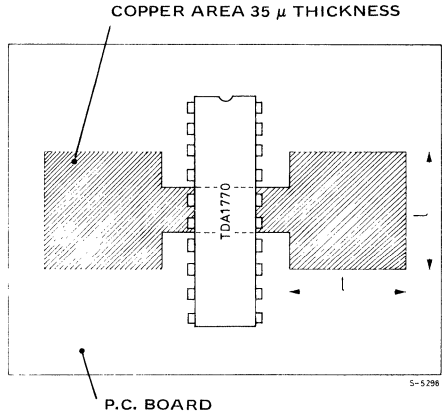


Fig. 9 - Thermal resistance of the P.C. copper side vs. side "ℓ"

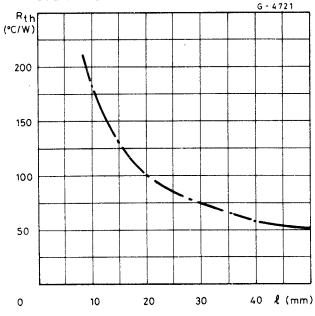
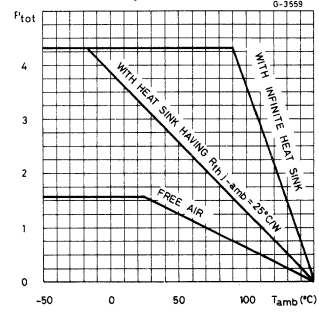


Fig. 10 - Maximum allowable power dissipation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA1904

4W AUDIO AMPLIFIER

The TDA 1904 is a monolithic integrated circuit in POWERDIP package intended for use as low-frequency power amplifier in a wide range of applications in portable radio and TV sets.
Its main features are:

- High output current capability (up to 2A)
- Protection against chip overtemperature
- Low noise
- High supply voltage rejection
- Supply voltage range: 4V to 20V

ADVANCE DATA

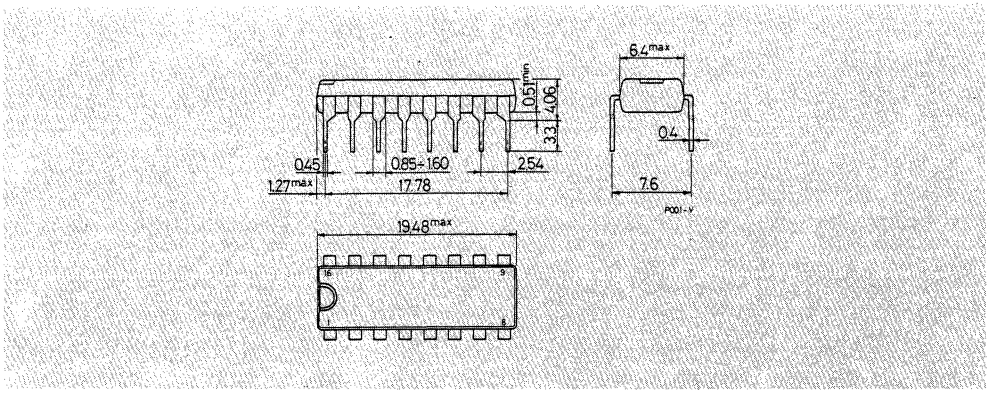
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_o	Peak output current (non repetitive)	2.5	A
I_o	Peak output current (repetitive)	2	A
P_{tot}	Total power dissipation at $T_{amb} = 80°C$	1	W
	$T_{case} = 60°C$	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

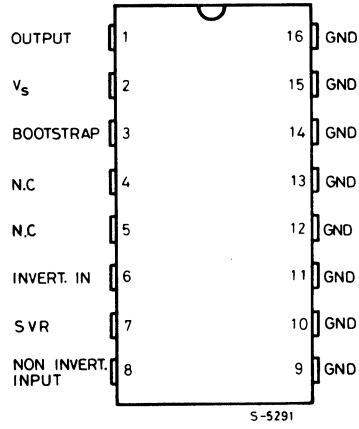
ORDERING NUMBER: TDA 1904

MECHANICAL DATA

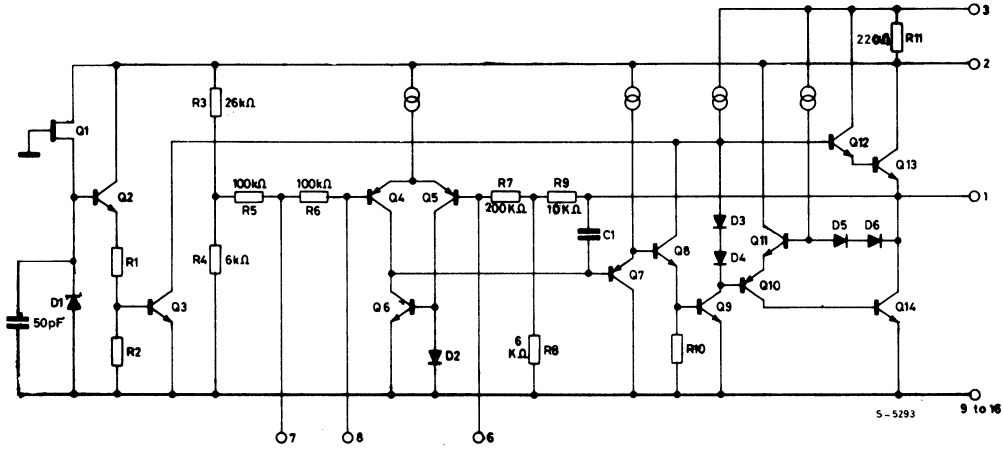
Dimensions in mm



CONNECTION DIAGRAM
(top view)



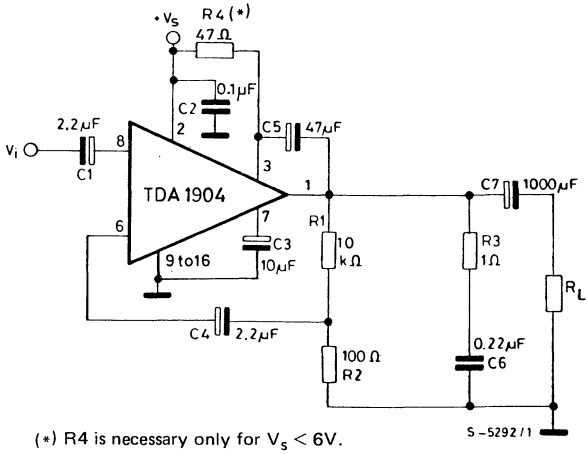
SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W

TEST CIRCUIT



(*) R4 is necessary only for $V_s < 6V$.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, $G_v = 40$ dB, $R_L = 4\Omega$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_d	Quiescent drain current	V_s= 9V V_s= 14V		16 19		mA mA
P_o	Output power	d = 10% f = 1 KHz V_s= 9V V_s= 12V V_s= 6V		 2 3.5 0.8		 W W W
d	Distortion	V_s= 9V f = 1 KHz P_o= 50 mW to 1.2W V_s= 14V P_o= 50 mW to 2W		 0.1 0.1		 % %
R_i	Input resistance (pin 8)			150		KΩ
B	Frequency response			40 to 40 000		Hz
G_v	Voltage gain (open loop)			80		dB
G_v	Voltage gain (closed loop)			40		dB
e_N	Total input noise voltage	R_g= 10 KΩ; B= 22Hz to 22KHz		3		μV
		R_g= 10 KΩ; B = curve A		2	4	
η	Efficiency	V_s= 9V P_o= 2W V_s= 12V P_o= 3.5W		70 65		%
SVR	Supply voltage rejection	V_s= 12V R_g= 10 KΩ f_{ripple}= 100 Hz		50		dB

Fig. 1 - Application circuit

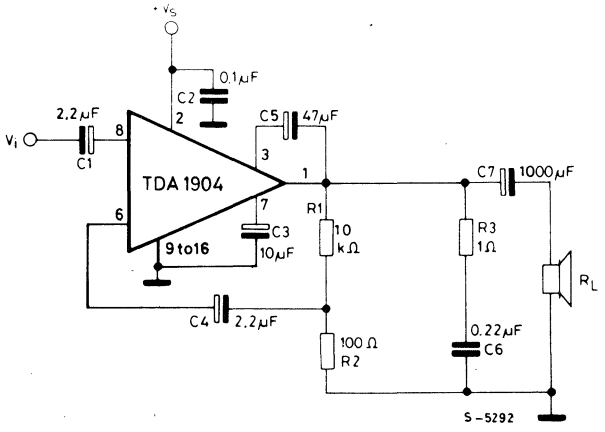
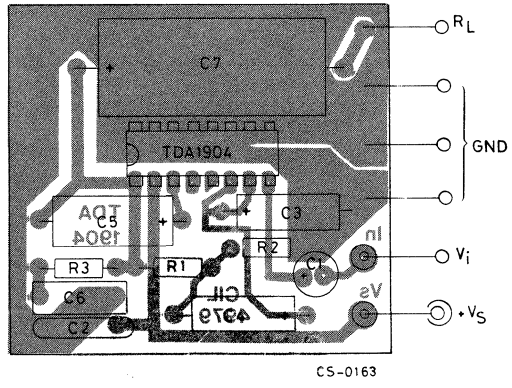


Fig. 2 - P.C. board and components layout of fig. 1 (1:1 scale)



LINEAR INTEGRATED CIRCUIT

TDA1905

5W AUDIO AMPLIFIER WITH MUTING

The TDA 1905 is a monolithic integrated circuit in POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets.
Its main features are:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise
- voltage range 4V to 30V

The TDA 1905 is assembled in a new plastic package, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6W and a thermal resistance of 15°C/W (junction to pins).

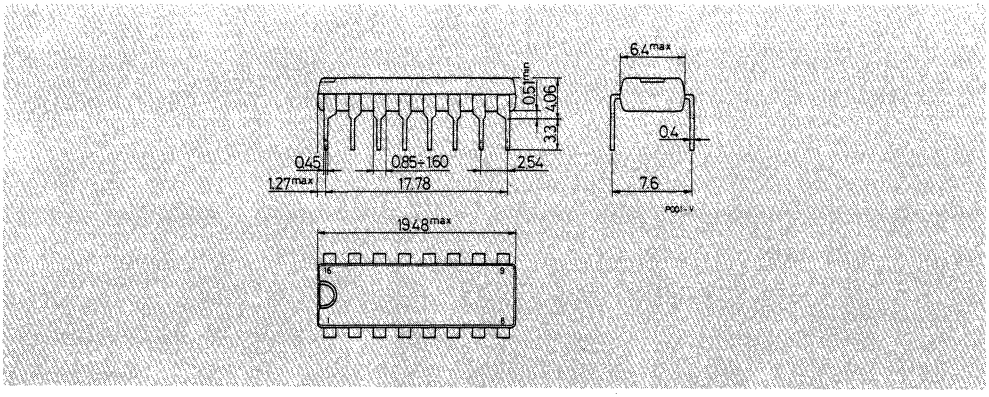
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3	A
I_o	Output peak current (repetitive)	2.5	A
V_i	Input voltage	0 to + V_s	V
V_i	Differential input voltage	± 7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at T_{amb} = 80°C	1	W
	T_{case} = 60°C	6	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1905

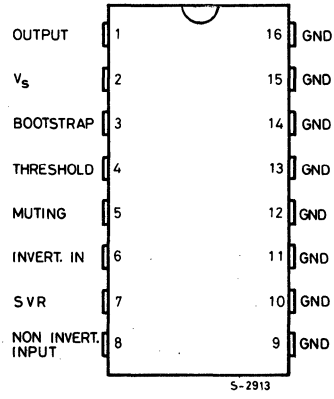
MECHANICAL DATA

Dimensions in mm

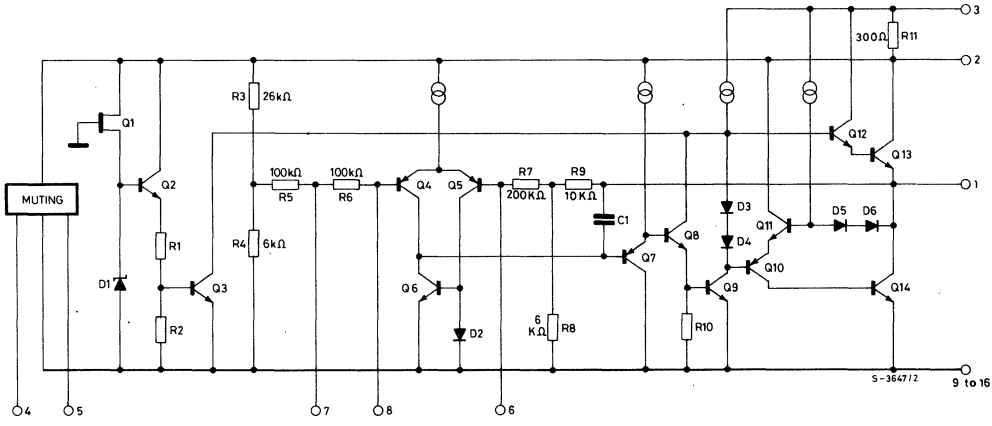


CONNECTION DIAGRAM

(Top view)



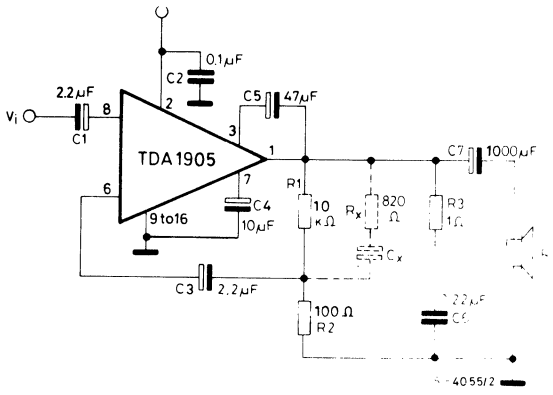
SCHEMATIC DIAGRAM



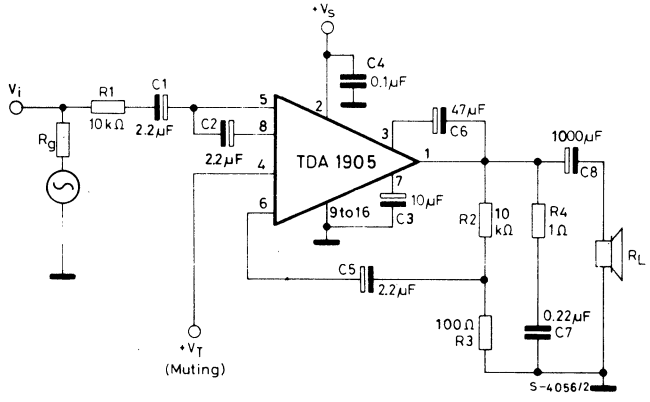
THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	max	70	°C/W

TEST CIRCUIT



MUTING CIRCUIT



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb} = 25°C, R_{th} (heatsink) = 20°C/W, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		30	V
V_o	Quiescent output voltage	V_s = 4V V_s = 14V V_s = 30V	1.6 6.7 14.4	2.1 7.2 15.5	2.5 7.8 16.8	V
I_d	Quiescent drain current	V_s = 4V V_s = 14V V_s = 30V		15 17 21	 35	mA
$V_{CE\ sat}$	Output stage saturation voltage	I_C = 1A I_C = 2A		0.5 1		V
P_o	Output power	d = 10% f = 1KHz V_s = 9V R_L = 4Ω (*) V_s = 14V R_L = 4Ω V_s = 18V R_L = 8Ω V_s = 24V R_L = 16Ω	 2.2 5 5 4.5	 2.5 5.5 5.5 5.3		W
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 14V R_L = 4Ω P_o = 50 mW to 3W V_s = 18V R_L = 8Ω P_o = 50 mW to 3W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		 0.1 0.1 0.1 0.1		%
V_i	Input sensitivity	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 37 49 73 100		mV
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4			V
R_i	Input resistance (pin 8)	f = 1KHz	60	100		KΩ
I_d	Drain current	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 380 550 410 295		mA
η	Efficiency	f = 1KHz V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 8Ω P_o = 5.5W V_s = 24V R_L = 16Ω P_o = 5.3W		 73 71 74 75		%

(*) With an external resistor of 100Ω between pin 3 and $+V_s$.

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
BW	Small signal bandwidth (-3dB)	V_s = 14V R_L = 4Ω P_o = 1W	40 to 40,000			Hz
G_v	Voltage gain (open loop)	V_s = 14V f = 1KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 14V R_L = 4Ω f = 1KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	R_g = 50Ω (°)		1.2		μV
		R_g = 1KΩ (°)		1.3		μV
		R_g = 10KΩ (°)		1.5	4.0	μV
		R_g = 50Ω (°°)		2.0		μV
		R_g = 1KΩ (°°)		2.0		μV
		R_g = 10KΩ (°°)		2.2	6.0	μV
S/N	Signal to noise ratio	V_s = 14V P_o = 5.5W R_L = 4Ω R_g = 10KΩ R_g = 0 (°)		90		dB
		R_g = 10KΩ R_g = 0 (°)		92		dB
		R_g = 10KΩ R_g = 0 (°°)		87		dB
		R_g = 10KΩ R_g = 0 (°°)		87		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 8Ω f_{ripple} = 100 Hz R_g = 10KΩ V_{ripple} = 0.5Vrms	40	50		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot} = 2.5W		115		°C

MUTING FUNCTION (Refer to Muting circuit)

$V_{T_{OFF}}$	Muting-off threshold voltage (pin 4)		1.9		4.7	V
$V_{T_{ON}}$	Muting-on threshold voltage (pin 4)		0		1.3	V
			6.2		V_s	V
R_5	Input resistance (pin 5)	Muting off	80	200		KΩ
		Muting on		10	30	Ω
R_4	Input resistance (pin 4)		150			KΩ
A_T	Muting attenuation	$R_g + R_1$ = 10KΩ	50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 30 and fig. 31

Fig. 1 - Quiescent output voltage vs. supply voltage

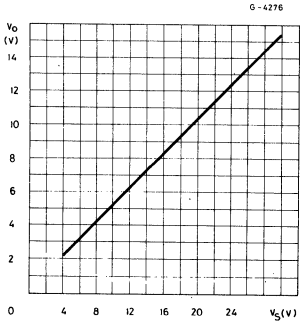


Fig. 2 - Quiescent drain current vs. supply voltage

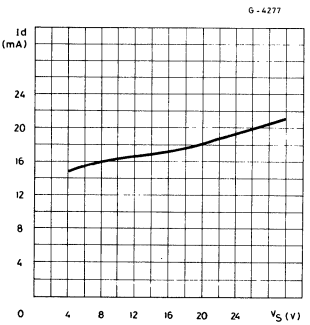


Fig. 3 - Output power vs. supply voltage

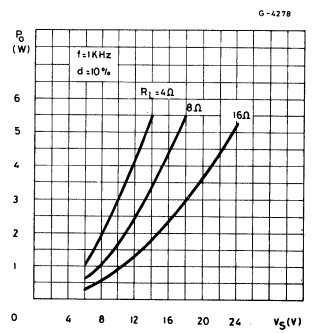


Fig. 4 - Distortion vs. output power ($R_L = 16\Omega$)

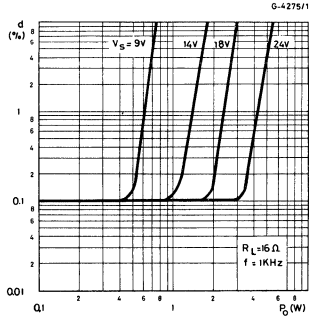


Fig. 5 - Distortion vs. output power ($R_L = 8\Omega$)

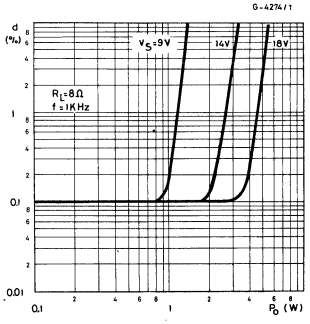


Fig. 6 - Distortion vs. output power ($R_L = 4\Omega$)

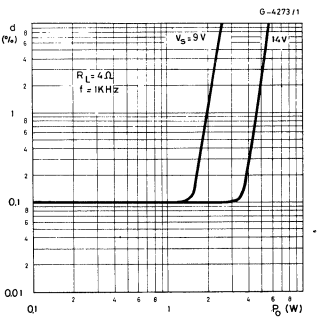


Fig. 7 - Distortion vs. frequency ($R_L = 16\Omega$)

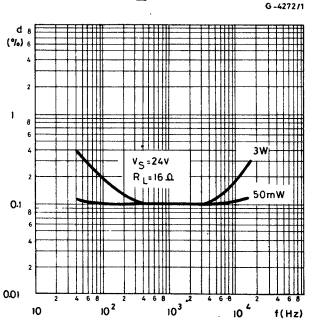


Fig. 8 - Distortion vs. frequency ($R_L = 8\Omega$)

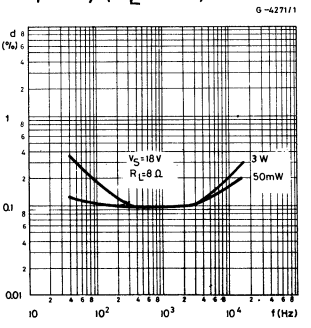


Fig. 9 - Distortion vs. frequency ($R_L = 4\Omega$)

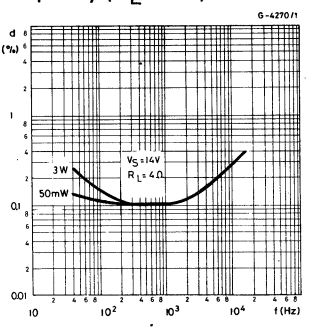


Fig. 10 - Open loop frequency response

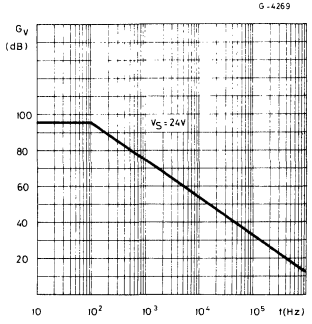


Fig. 11 - Output power vs. input voltage

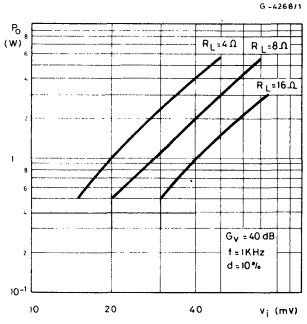


Fig. 12 - Value of capacitor Cx vs. bandwidth (BW) and gain (Gv)

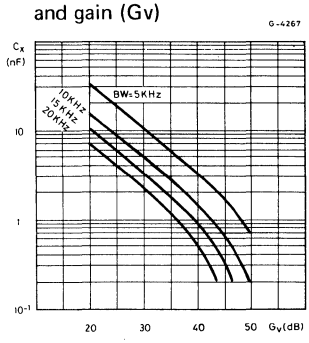


Fig. 13 - Supply voltage rejection vs. voltage gain (ref. to the Muting circuit)

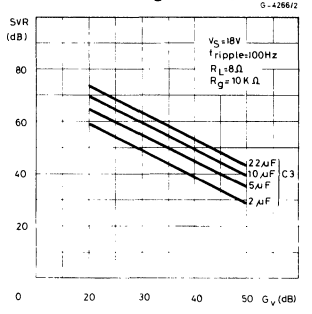


Fig. 14 - Supply voltage rejection vs. source resistance

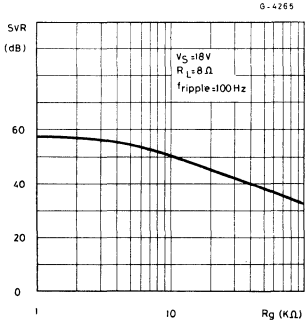


Fig. 15 - Max power dissipation vs. supply voltage (sine wave operation)

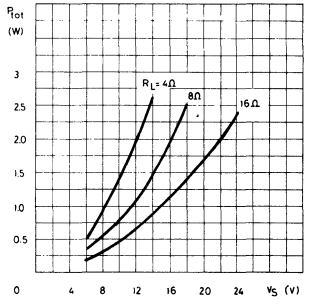


Fig. 16 - Power dissipation and efficiency vs. output power

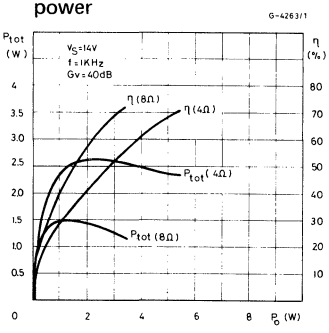


Fig. 17 - Power dissipation and efficiency vs. output power

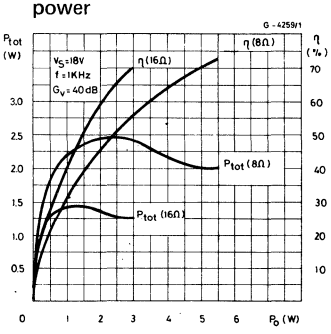
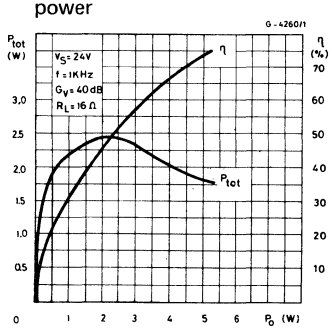
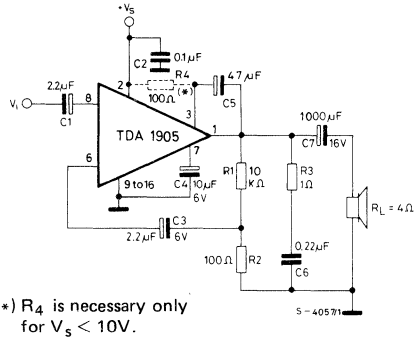


Fig. 18 - Power dissipation and efficiency vs. output power



APPLICATION INFORMATION

Fig. 19 - Application circuit without muting



(*) R_4 is necessary only for $V_s < 10V$.

$P_o = 5.5W$ (d = 10%)
$V_s = 14V$
$I_d = 0.55A$
$G_v = 40$ dB

Fig. 20 - PC board and components lay-out of the circuit of fig. 19 (1:1 scale)

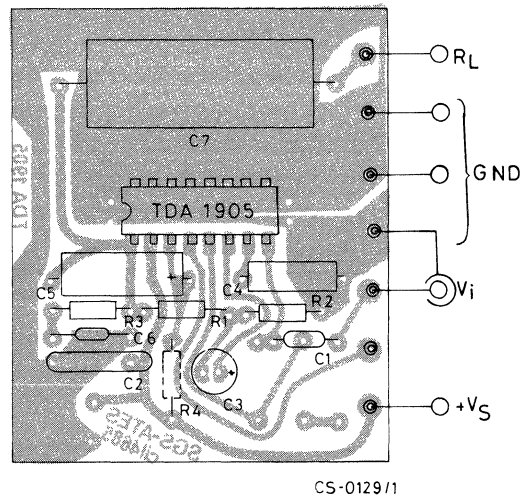


Fig. 21 - Application circuit with muting

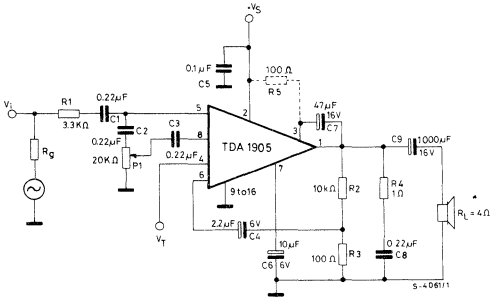
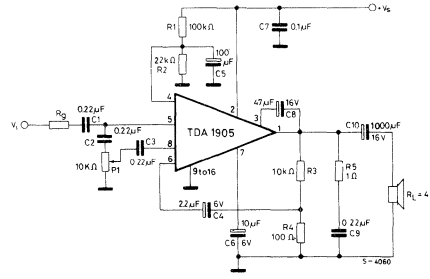


Fig. 22 - Delayed muting circuit



APPLICATION INFORMATION (continued)

Fig. 23 - Low-cost application circuit without bootstrap.

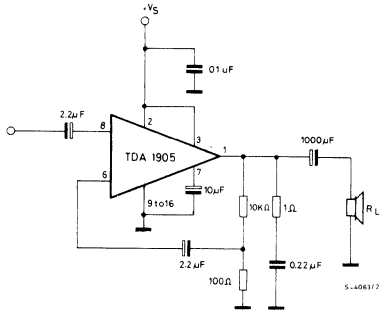


Fig. 24 - Output power vs. supply voltage (circuit of fig. 23)

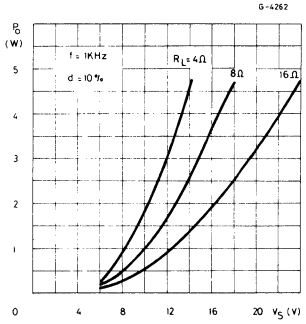


Fig. 25 - Two position DC tone control using change of pin 5 resistance (muting function)

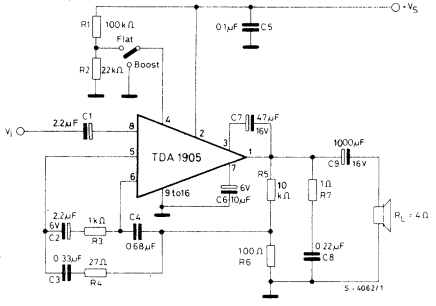


Fig. 26 - Frequency response of the circuit of fig. 25

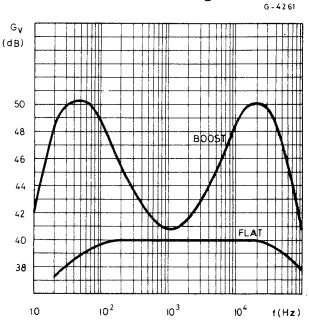


Fig. 27 - Bass Bomb tone control using change of pin 5 resistance (muting function)

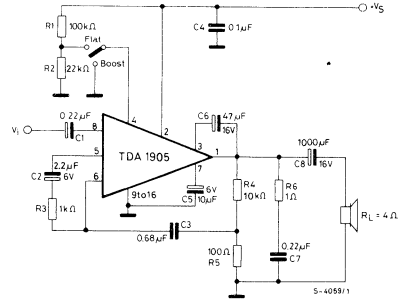
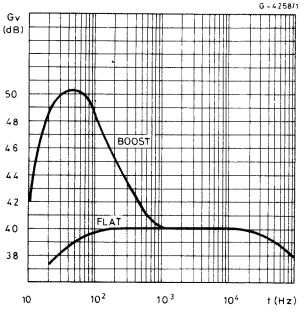


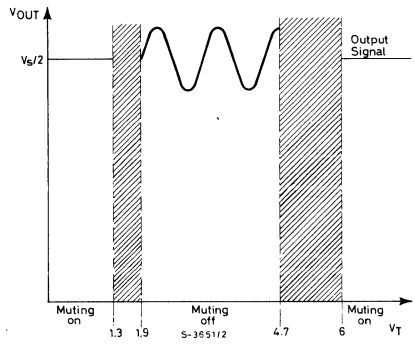
Fig. 28 - Frequency response of the circuit of fig. 27



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 4, as shown in fig. 29

Fig. 29

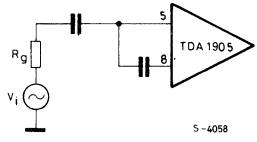


The input resistance at pin 5 depends on the threshold voltage V_T at pin 4 and is typically:

$R_5 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_5 = 10\Omega$ @ $0V \leqslant V_T \leqslant 1.3V$ $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression:



$$A_T = \frac{V_i}{V_8} = \frac{R_g + \left(\frac{R_8 \cdot R_5}{R_8 + 5}\right)}{\left(\frac{R_8 \cdot R_5}{R_8 + R_5}\right)}$$

where $R_8 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, tipically 1.2 dB.
A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 4 is greater than 150 KΩ. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 22)
- during switching at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 5 can be useful in many application and two examples are shown in fig. 25 and 27, where it has been used to change the feedback network, obtaining 2 different frequency response.

APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 21. When the supply voltage V_s is less than 10V, a 100Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Component	Raccom. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range Min.	Max.
$R_g + R_1$	10KΩ	Input signal imped. for muting operation	Increase of the attenuation in muting-on condition. Decrease of the input sensitivity.	Decrease of the attenuation in muting on condition.		
R_2	10KΩ	Feedback resistors	Increase of gain.	Decrease of gain. Increase quiescent current.	$9\,R_3$	
R_3	100Ω		Decrease of gain.	Increase of gain.		1KΩ
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R_5	100Ω	Increase of the output swing with low supply voltage.			47	330
P_1	20KΩ	Volume potentiometer	Increase of the switch-on noise.	Decrease of the input impedance and of the input level.	10KΩ	100KΩ
C_1 C_2 C_3	0.22 μF	Input DC decoupling.	Higher cost lower noise.	Higher low frequency cutoff. Higher noise		
C_4	2.2μF	Inverting input DC decoupling.	Increase of the switch-on noise.	Higher low frequency cutoff.	0.1μF	
C_5	0.1μF	Supply voltage bypass.		Danger of oscillations.		
C_6	10 μF	Ripple rejection	Increase of SVR increase of the switch-on time	Degradation of SVR	2.2 μF	100 μF
C_7	47μF	Bootstrap.		Increase of the distortion at low frequency.	10μF	100μF
C_8	0.22μF	Frequency stability.		Danger of oscillation.		
C_9	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 32 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 30 - Output power and drain current vs. case temperature.

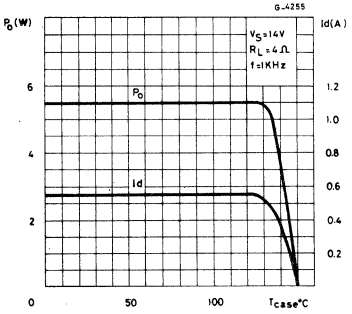


Fig. 31 - Output power and drain current vs. case temperature

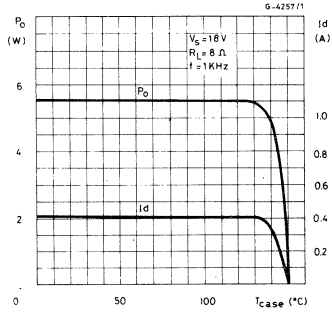
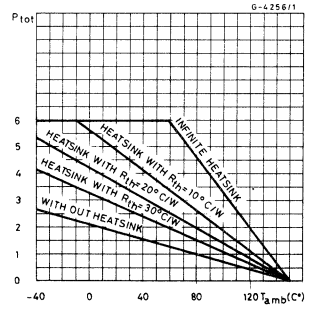


Fig. 32 - Maximum allowable power dissipation vs. ambient temperature.



MOUNTING INSTRUCTION

The TDA 1905 is assembled in a new plastic package, the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat produced by the chip.

Figure 33 and 34 show two ways of heatsinking. In the first case, a PC board copper area is used as a heatsink l = 65 mm. while in the second case, the device is soldered to an external heatsink.
In both examples, the thermal resistance junction-ambient is 35°C/W.

Fig. 33 - Example of heatsink using PC board copper (l = 65 mm)

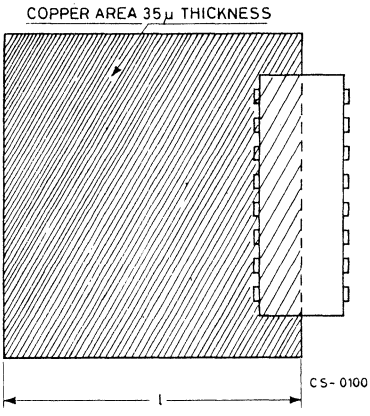
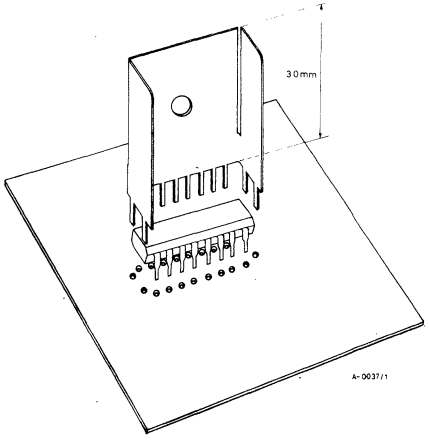


Fig. 34 - Example of an external heatsink



TDA1908

LINEAR INTEGRATED CIRCUIT

8W AUDIO AMPLIFIER

The TDA 1908 is a monolithic integrated circuit in 12 lead quad in-line plastic package intended for low frequency power applications. The mounting is compatible with SGS TBA 800, TBA 810S, TCA 830S and TCA940N. Its main features are:

- flexibility in use with a max output current of 3A and an operating supply voltage range of 4V to 30V
- protection against chip overtemperature
- soft limiting in saturation conditions
- low "switch-on" noise
- low number of external components
- high supply voltage rejection
- very low noise

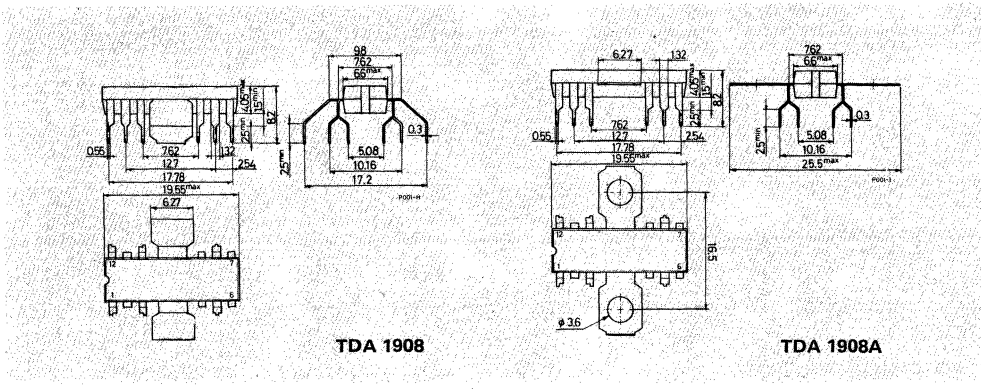
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3.5	A
I_o	Output peak current (repetitive)	3	A
P_{tot}	Power dissipation: at T_{amb} = 80°C (TDA 1908)	1	W
	at T_{tab} = 100°C (TDA 1908A)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

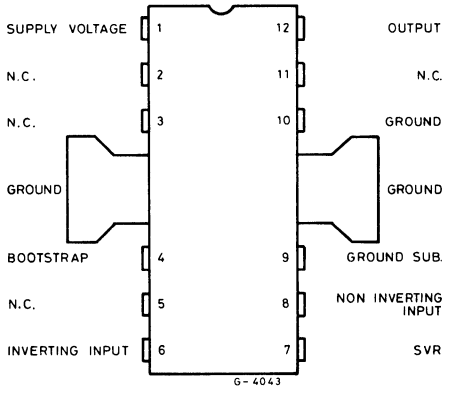
ORDERING NUMBERS: TDA 1908, TDA 1908A

MECHANICAL DATA

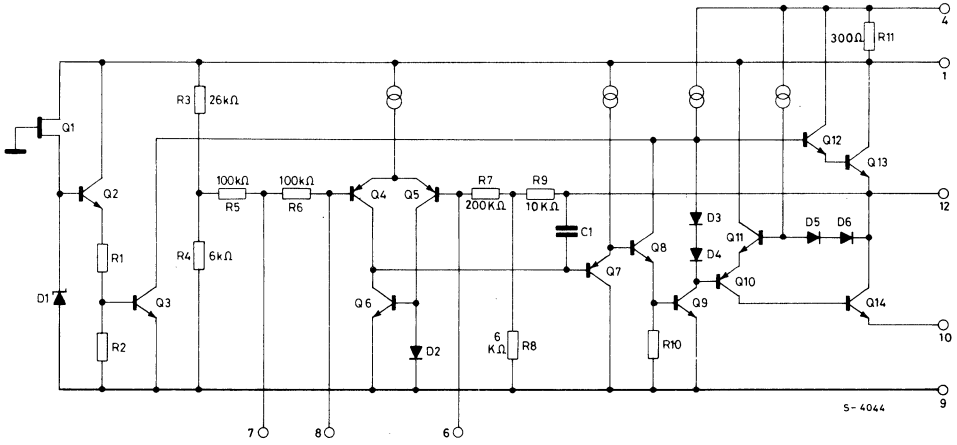
Dimensions in mm



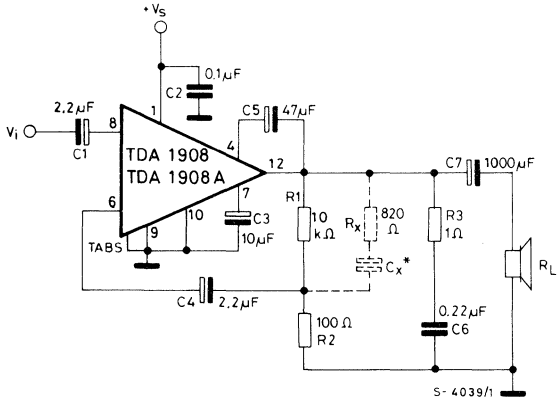
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



TEST CIRCUIT



* See fig. 12.

THERMAL DATA

			TDA 1908	TDA 1980A
$R_{th\ j\text{-}tab}$	Thermal resistance junction-tab	max	12 °C/W	10 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-amb	max	(°) 70 °C/W	80 °C/W

(°) Obtained with tabs soldered to printed circuit board with min copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, R_{th} (heatsink)= 8 °C/W, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		30	V
V_o	Quiescent output voltage	V_s = 4V V_s = 18V V_s = 30V	1.6 8.2 14.4	2.1 9.2 15.5	2.5 10.2 16.8	V
I_d	Quiescent drain current	V_s = 4V V_s = 18V V_s = 30V		15 17.5 21	 35	mA
V_{CEsat}	Output stage saturation voltage (each output transistor)	I_C= 1A I_C= 2.5A		0.5 1.3		V
P_o	Output power	d = 10% f = 1 KHz V_s = 9V R_L= 4Ω V_s = 14V R_L= 4Ω V_s = 18V R_L= 4Ω V_s = 22V R_L= 8Ω V_s = 24V R_L= 16Ω	 7 6.5 4.5	 2.5 5.5 9 8 5.3		W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test condition	Min.	Typ.	Max	Unit
d	Harmonic distortion	f = 1KHz V_s = 9V R_L = 4Ω P_o = 50 mW to 1.5W V_s = 18V R_L = 4Ω P_o = 50 mW to 4W V_s = 24V R_L = 16Ω P_o = 50 mW to 3W		 0.1 0.1 0.1		%
V_i	Input sensitivity	V_s = 9V R_L = 4Ω P_o = 2.5W V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 4Ω P_o = 9W V_s = 22V R_L = 8Ω P_o = 8W V_s = 24V R_L = 16Ω P_o = 5.3W		37 52 64 90 110		mV
V_i	Input saturation voltage (rms)	V_s = 9V V_s = 14V V_s = 18V V_s = 24V	0.8 1.3 1.8 2.4			V
R_i	Input resistance (pin 8)	f = 1 KHz	60	100		KΩ
I_s	Drain current	f = 1 KHz V_s = 14V R_L = 4Ω P_o = 5.5W V_s = 18V R_L = 4Ω P_o = 9W V_s = 22V R_L = 8Ω P_o = 8W V_s = 24V R_L = 16Ω P_o = 5.3W		 570 730 500 310		mA
η	Efficiency	V_s = 18V f = 1 KHz R_L = 4Ω P_o = 9W		 72		%
BW	Small signal bandwidth (-3 dB)	V_s = 18V R_L = 4Ω P_o = 1W	40 to 40 000			Hz
G_v	Voltage gain (open loop)	f = 1 KHz		75		dB
G_v	Voltage gain (closed loop)	V_s = 18V R_L = 4Ω f = 1 KHz P_o = 1W	39.5	40	40.5	dB
e_N	Total input noise	(°) R_g = 50Ω R_g = 1KΩ R_g = 10 KΩ		1.2 1.3 1.5	 4.0	μV
		(°°) R_g = 50Ω R_g = 1KΩ R_g = 10KΩ		2.0 2.0 2.2	 6.0	μV
S/N	Signal to noise ratio	V_s = 18V, P_o = 9W, R_L = 4Ω: R_g = 10KΩ, R_g = 0 (°)		92 94		dB
		V_s = 18V, P_o = 9W, R_L = 4Ω: R_g = 10KΩ, R_g = 0 (°°)		88 90		dB
SVR	Supply voltage rejection	V_s = 18V R_L = 4Ω f_{ripple} = 100 Hz R_g = 10KΩ	40	50		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot} = 4W		110		°C

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 24 and fig. 25.

Fig. 1 - Quiescent output voltage vs. supply voltage

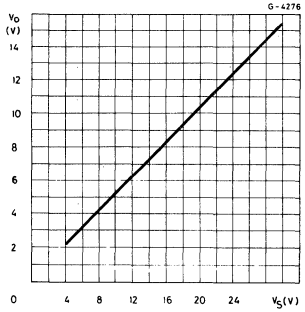


Fig. 2 - Quiescent drain current vs. supply voltage

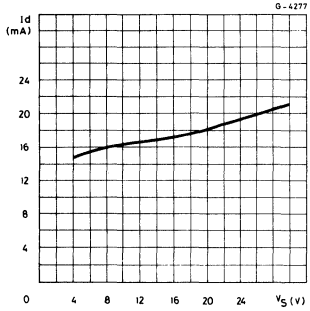


Fig. 3 - Output power vs. supply voltage

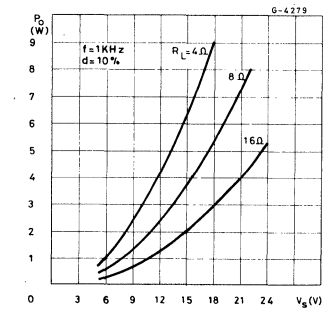


Fig. 4 - Distortion vs. output power (R_L= 16Ω)

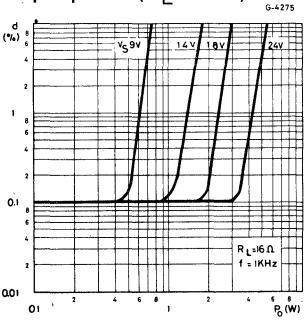


Fig. 5 - Distortion vs. output power (R_L= 8Ω)

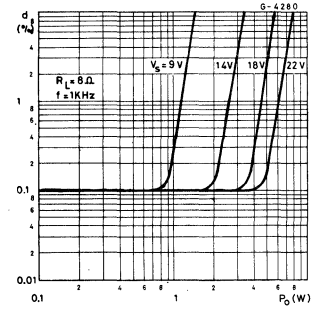


Fig. 6 - Distortion vs. output power (R_L= 4Ω)

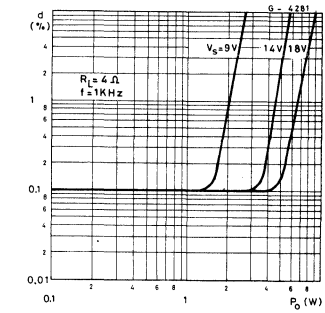


Fig. 7 - Distortion vs. frequency (R_L= 16Ω)

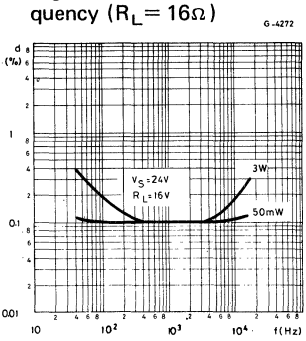


Fig. 8 - Distortion vs. frequency (R_L= 8Ω)

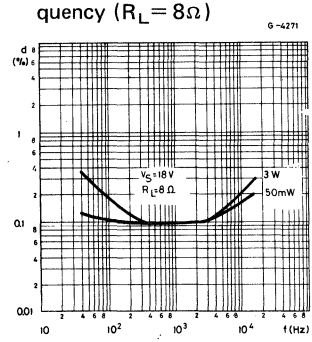


Fig. 9 - Distortion vs. frequency (R_L= 4Ω)

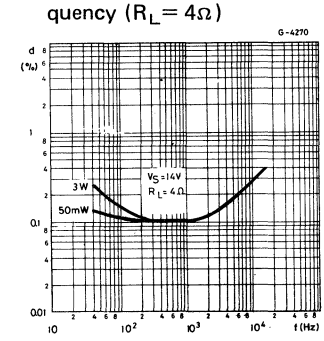


Fig. 10 - Open loop frequency response

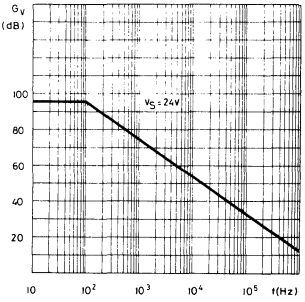


Fig. 11 - Output power vs. input voltage

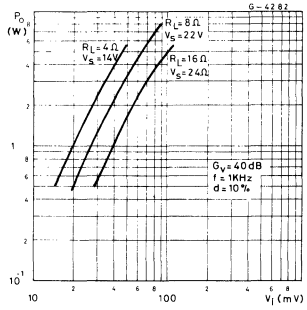


Fig. 12 - Values of capacitor C_X versus gain and B_W

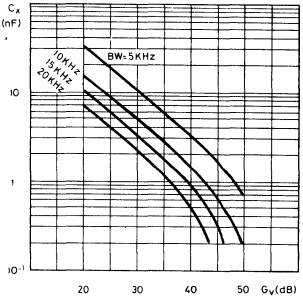


Fig. 13 - Supply voltage rejection vs. voltage gain

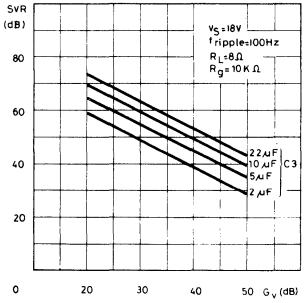


Fig. 14 - Supply voltage rejection vs. source resistance

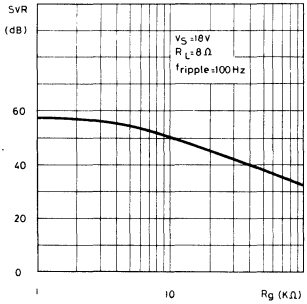


Fig. 15 - Max power dissipation vs. supply voltage

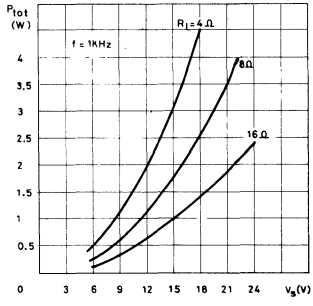


Fig. 16 - Power dissipation and efficiency vs. output power (V_S= 14V)

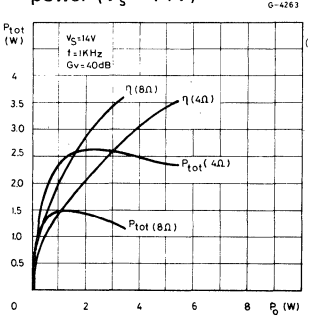


Fig. 17 - Power dissipation and efficiency vs. output power (V_S= 18V)

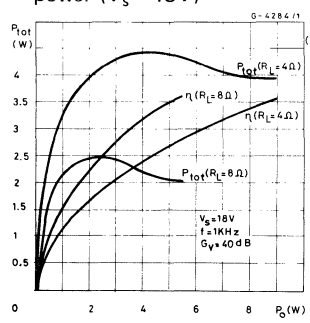
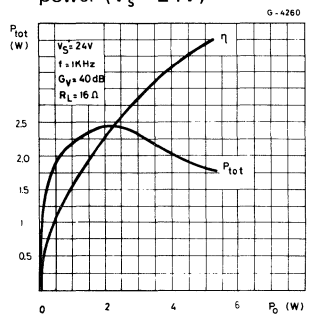
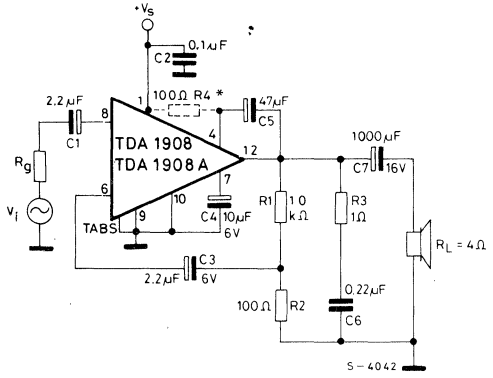


Fig. 18 - Power dissipation and efficiency vs. output power (V_S= 24V)



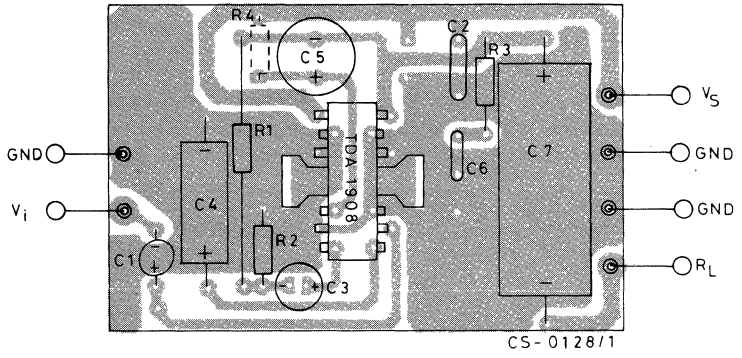
APPLICATION INFORMATION

Fig. 19 - Application circuit with bootstrap



* R4 is necessary when V_s is less than 10V.

Fig. 20 - P.C. board and component lay-out of the circuit of fig. 19 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 21 - Application circuit without bootstrap

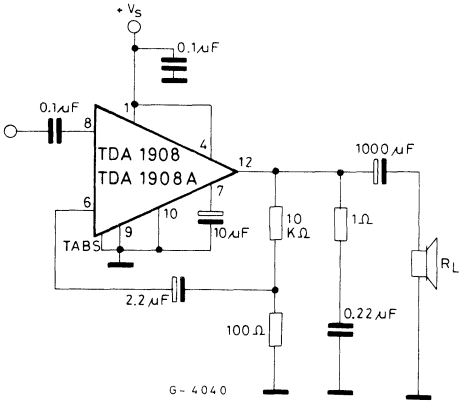


Fig. 22 - Output power vs. supply voltage (circuit of fig. 21)

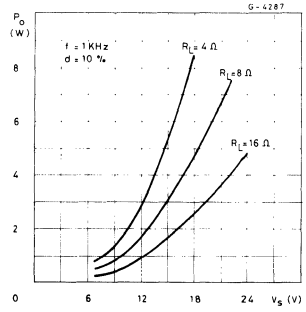
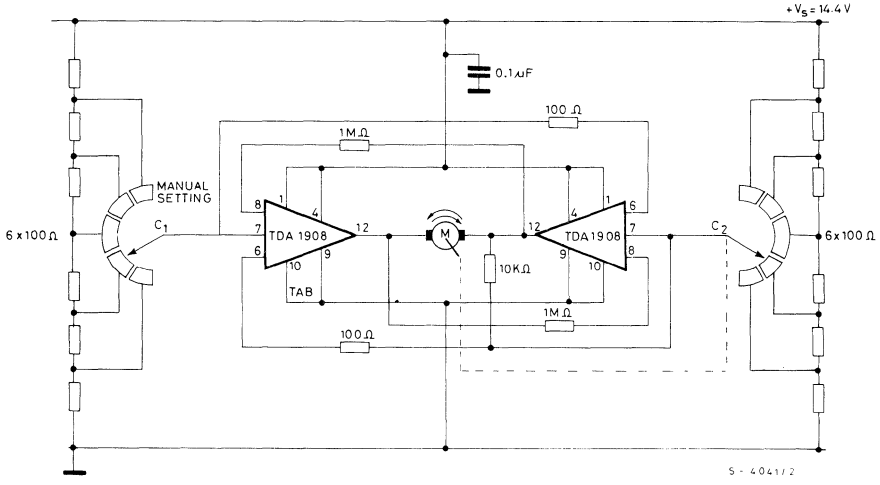


Fig. 23 - Position control for car headlights



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 19.
When the supply voltage V_s is less than 10V, a 100Ω resistor must be connected between pin 1 and pin 4 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

Component	Raccom. value	Purpose	Larger than raccomanded value	Smaller than raccomanded value	Allowed range	
					Min.	Max.
R_1	10 KΩ	Close loop gain setting.	Increase of gain.	Decrease of gain. Increase quiescent current.	9 R_2	
R_2	100 Ω	Close loop gain setting.	Decrease of gain.	Increase of gain.		$R_1/9$
R_3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
R_4	100 Ω	Increasing of output swing with low V_s.			47Ω	330Ω
C_1	2.2 μF	Input DC decoupling.	Lower noise	Higher low frequency cutoff. Higher noise.	0.1 μF	
C_2	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C_3	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise	Higher low frequency cutoff.	0.1 μF	
C_4	10 μF	Ripple Rejection.	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.	2.2 μF	100 μF
C_5	47 μF	Bootstrap		Increase of the distortion at low frequency	10 μF	100 μF
C_6	0.22 μF	Frequency stability.		Danger of oscillation.		
C_7	1000 μF	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If, for any reason,, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 26 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 24 - Output power and drain current vs. case temperature

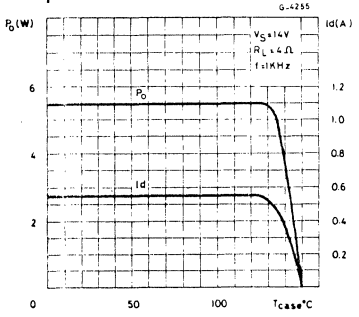


Fig. 25 - Output power and drain current vs. case temperature

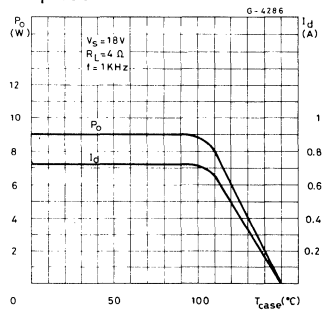
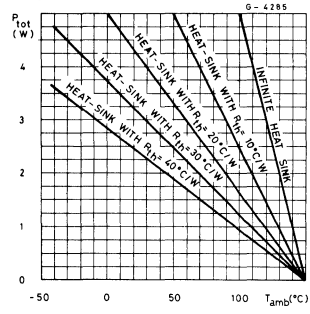


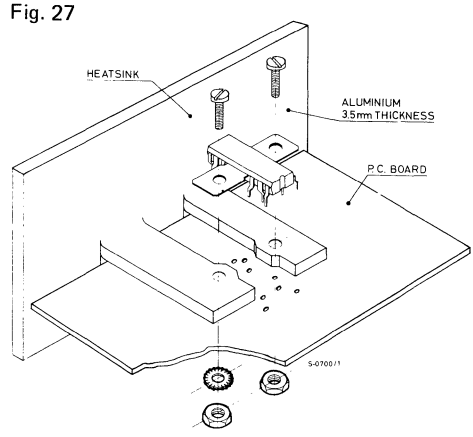
Fig. 26 - Maximum power dissipation vs. ambient temperature



MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heatsink (TDA 1908A see fig. 27), or by soldering them to a copper area on the PC board (TDA 1908 see fig. 28). During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 27



MOUNTING INSTRUCTIONS (continued)

Fig. 28 - Mounting example (TDA 1908)

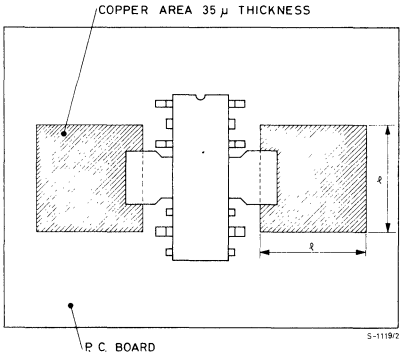
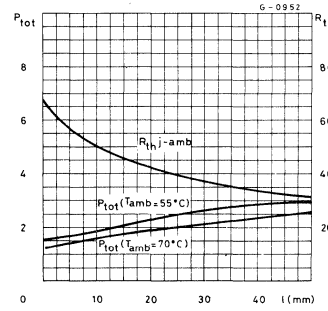


Fig. 29 - Maximum power dissipation and thermal resistance vs. side "ℓ" (TDA 1908)



LINEAR INTEGRATED CIRCUIT

TDA1910

10W AUDIO AMPLIFIER WITH MUTING

The TDA 1910 is a monolithic integrated circuit in MULTIWATT ® package, intended for use in Hi-Fi audio power applications, **as high quality TV sets.**
The TDA 1910 meets the DIN 45500 (d = 0.5%) guaranteed output power of 10W when used at 24V/4Ω. At 24V/8Ω the output power is 7W min. Features:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise.

The TDA 1910 is assembled in MULTIWATT ® package that offers:

- easy assembly
- simple heatsink
- space and cost saving
- high reliability.

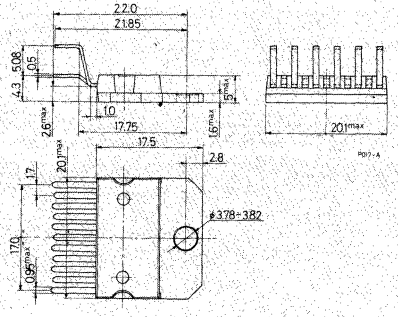
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	30	V
I_o	Output peak current (non repetitive)	3.5	A
I_o	Output peak current (repetitive)	3.0	A
V_i	Input voltage	0 to + V_s	V
V_i	Differential input voltage	± 7	V
V_{11}	Muting thresold voltage	V_s	V
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1910

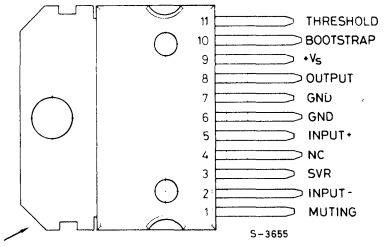
MECHANICAL DATA

Dimensions in mm



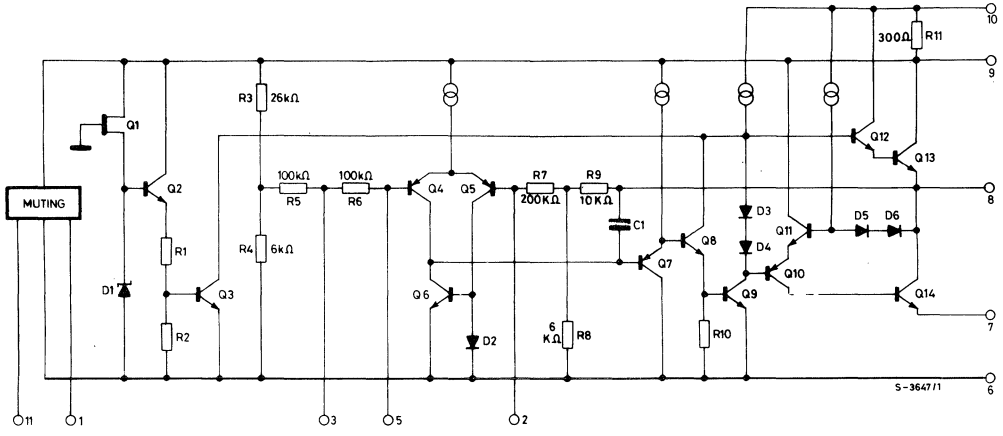
TDA1910

CONNECTION DIAGRAM (Top view)

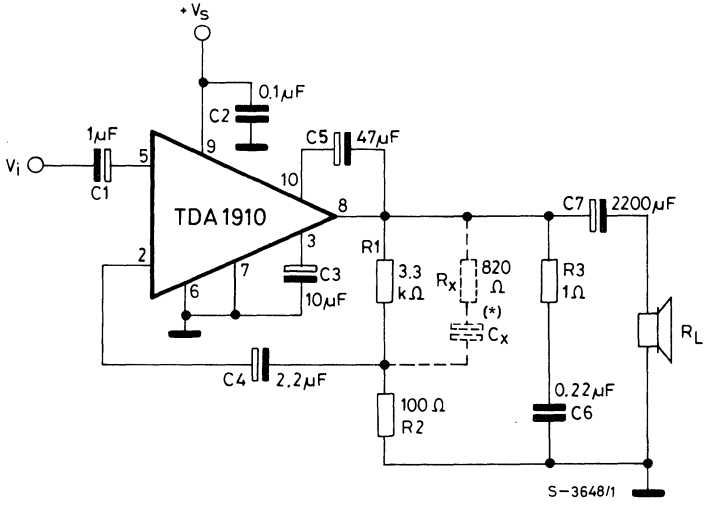


tab connected to pin 6

SCHEMATIC DIAGRAM

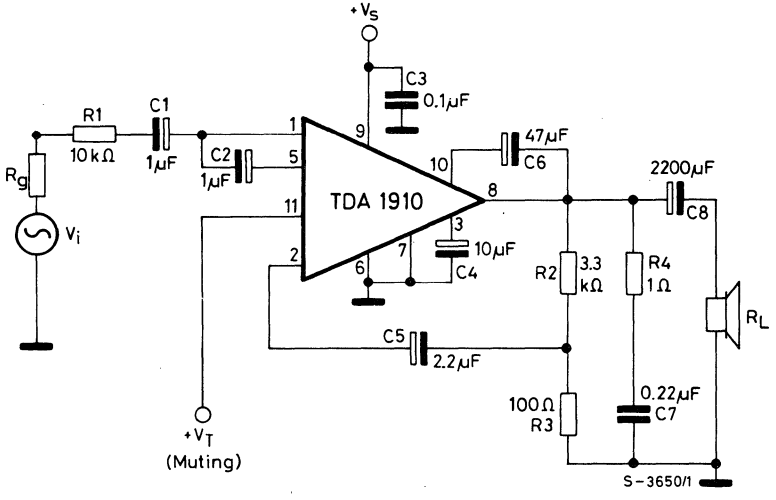


TEST CIRCUIT



(*) See fig. 13.

MUTING CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, R_{th} (heatsink) = 4°C/W, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		30	V
V_o	Quiescent output voltage	V_s = 18V V_s = 24V	8.3 11.5	9.2 12.4	10 13.4	V
I_d	Quiescent drain current	V_s = 18V V_s = 24V		19 21	32 35	mA
$V_{CE\ sat}$	Output stage saturation voltage	I_C= 2A		1		V
		I_C= 3A		1.6		
P_o	Output power	d = 0.5% f = 40 to 15,000Hz V_s = 18V R_L= 4Ω V_s = 24V R_L= 4Ω V_s = 24V R_L= 8Ω	 6.5 10 7	 7 12 7.5		W
		d = 10% f = 1 KHz V_s = 18V R_L= 4Ω V_s = 24V R_L= 4Ω V_s = 24V R_L= 8Ω	 8.5 15 9	 9.5 17 10		W
d	Harmonic distortion	f = 40 to 15,000 Hz V_s = 18V R_L= 4Ω P_o= 50 mW to 6.5W V_s= 24V R_L= 4Ω P_o= 50 mW to 10W V_s = 24V R_L= 8Ω P_o= 50 mW to 7W		 0.2 0.2 0.2	 0.5 0.5 0.5	%
d	Intermodulation distortion	V_s = 24V R_L= 4Ω P_o= 10W f_1= 250 Hz f_2= 8 KHz (DIN 45500)		0.2		%
V_i	Input sensitivity	f = 1 KHz V_s = 18V R_L= 4Ω P_o= 7W V_s = 24V R_L= 4Ω P_o= 12W V_s = 24V R_L= 8Ω P_o= 7.5W		 170 220 245		mV
V_i	Input saturation voltage (rms)	V_s = 18V V_s = 24V	1.8 2.4			V
R_i	Input resistance (pin 5)	f = 1 KHz	60	100		KΩ
I_d	Drain current	V_s = 24V f = 1 KHz R_L= 4Ω P_o= 12W R_L= 8Ω P_o= 7.5W		 820 475		mA

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test condition		Min.	Typ.	Max.	Unit
η	Efficiency	V_s = 24V f = 1 KHz R_L= 4Ω P_o= 12W R_L= 8Ω P_o= 7.5W			62 65		%
BW	Small signal bandwidth	V_s = 24V R_L= 4Ω P_o= 1W		10 to 120,000			Hz
BW	Power bandwidth	V_s = 24V R_L= 4Ω P_o = 12W d ⩽ 0.5%		40 to 15,000			Hz
G_v	Voltage gain (open loop)	f = 1 KHz			75		dB
G_v	Voltage gain (closed loop)	V_s = 24V R_L= 4Ω f = 1 KHz P_o = 1W		29.5	30	30.5	dB
e_N	Total input noise		R_g = 50Ω R_g = 1KΩ (°) R_g = 10KΩ		1.2 1.3 1.5	3.0 3.2 4.0	μV
			R_g = 50Ω R_g = 1KΩ (°°) R_g = 10KΩ		2.0 2.0 2.2	5.0 5.2 6.0	μV
S/N	Signal to noise ratio	V_s = 24V P_o = 12W R_L= 4Ω	R_g = 10KΩ (°) R_g = 0	97	103 105		dB
			R_g = 10KΩ (°°) R_g = 0	93	100 100		dB
SVR	Supply voltage rejection	V_s = 24V R_L= 4Ω f_{ripple}= 100 Hz R_g= 10 KΩ		50	60		dB
T_{sd}	Thermal shut-down case temperature (*)	P_{tot}= 8W		110	125		°C
MUTING FUNCTION (Refer to Muting circuit)							
V_T	Muting-off threshold voltage (pin 11)			1.9		4.7	V
V_T	Muting-on threshold voltage (pin 11)			0		1.3	V
				6		V_s	
R_1	Input resistance (pin 1)	Muting off		80	200		KΩ
		Muting on			10	30	Ω
R_{11}	Input resistance (pin 11)			150			KΩ
A_T	Muting attenuation	$R_g + R_1$= 10 KΩ		50	60		dB

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 29 and fig. 30.

Fig. 1 - Quiescent output voltage vs. supply voltage

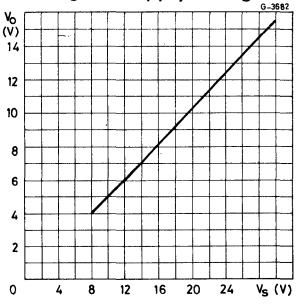


Fig. 2 - Quiescent drain current vs. supply voltage

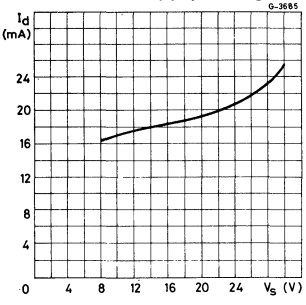


Fig. 3 - Open loop frequency response

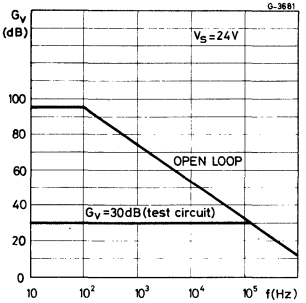


Fig. 4 - Output power vs. supply voltage

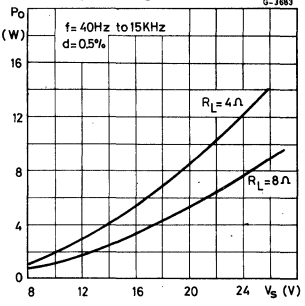


Fig. 5 - Output power vs. supply voltage

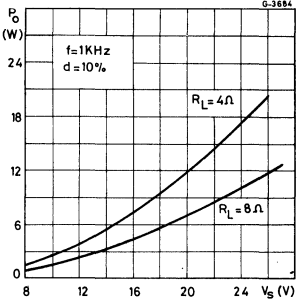


Fig. 6 - Distortion vs. output power

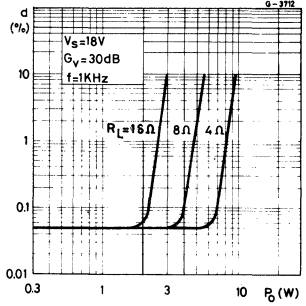


Fig. 7 - Distortion vs. output power

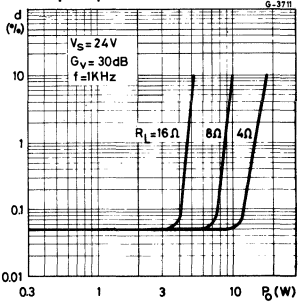


Fig. 8 - Output power vs. frequency

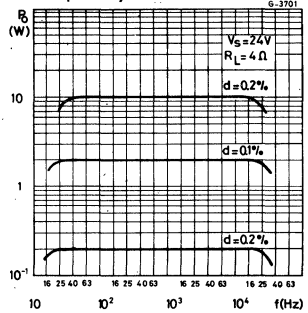


Fig. 9 - Output power vs. frequency

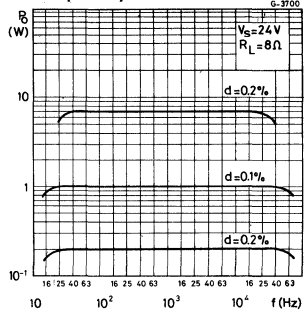


Fig. 10 - Output power vs. input voltage

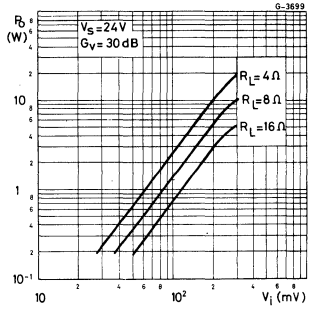


Fig. 11 - Output power vs. input voltage

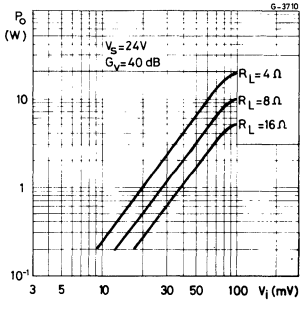


Fig. 12 - Total input noise vs. source resistance

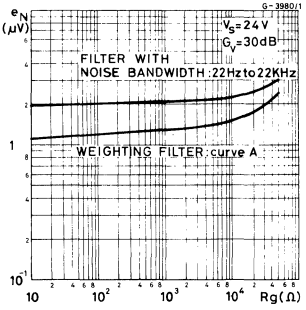


Fig. 13 - Values of capacitor C_X vs. bandwidth (BW) and gain (G_V)

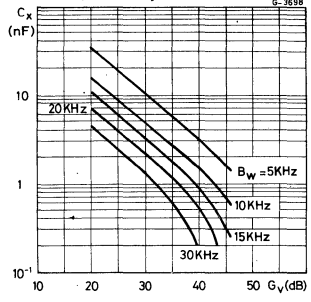


Fig. 14 - Supply voltage rejection vs. voltage gain

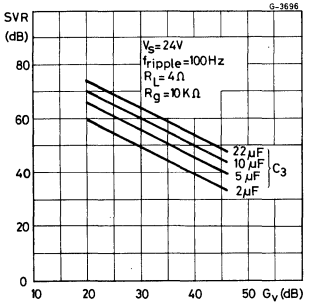


Fig. 15 - Supply voltage rejection vs. source resitance

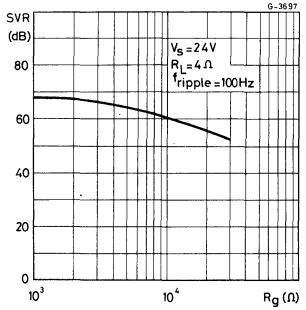


Fig. 16 - Power dissipation and efficiency vs. output power

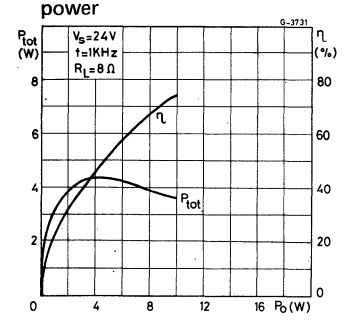


Fig. 17 - Power dissipation and efficiency vs. output power

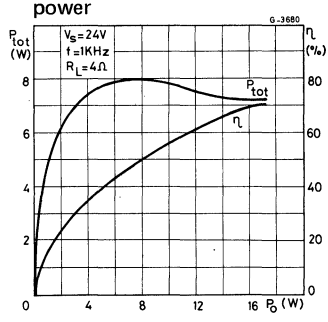
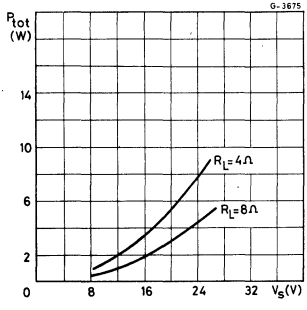


Fig. 18 - Max power dissipation vs. supply voltage



APPLICATION INFORMATION

Fig. 19 - Application circuit without muting

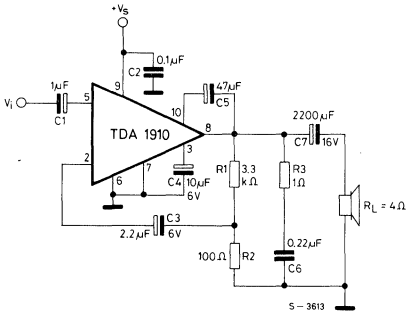


Fig. 20 - PC board and component lay-out of the circuit of fig. 19 (1:1 scale)

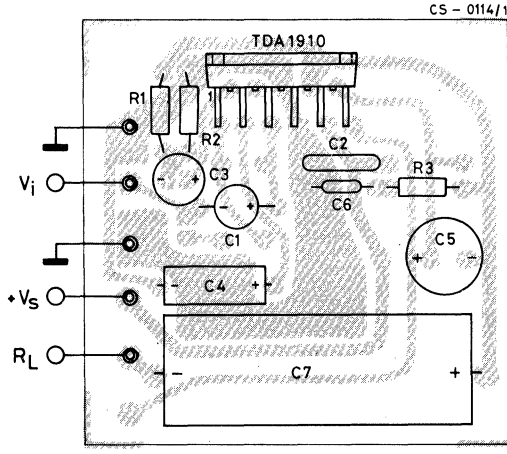
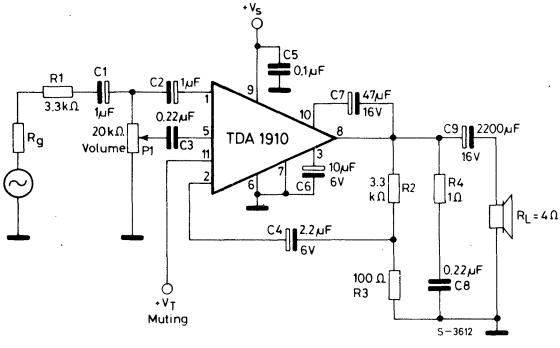


Fig. 21 - Application circuit with muting



Performance (circuits of fig. 19 and 21)

P_o = 12W (40 to 15000 Hz, d ⩽0.5%)
V_s = 24V
I_d = 0.82A
G_v = 30 dB

APPLICATION INFORMATION (continued)

Fig. 22 - Two position DC tone control (10 dB boost 50 Hz and 20 KHz) using change of pin 1 resistance (muting function)

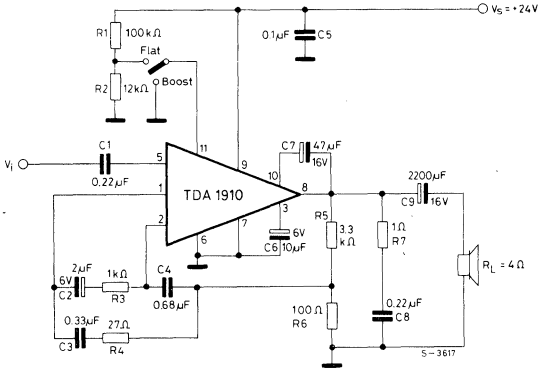


Fig. 23 - Frequency response of the circuit of fig. 22

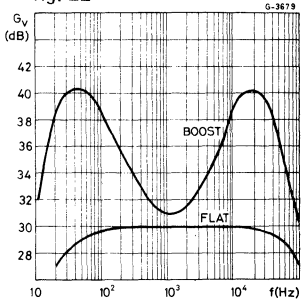


Fig. 24 - 10 dB 50 Hz boost tone control using change of pin 1 resistance (muting function)

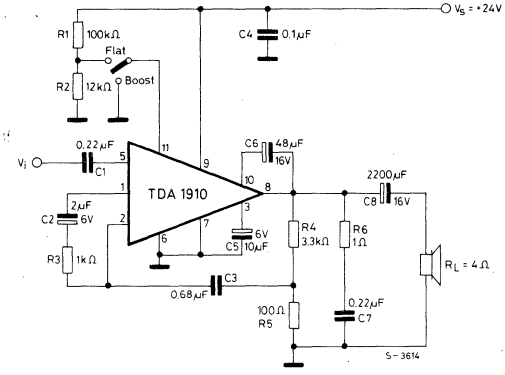


Fig. 25 - Frequency response of the circuit of fig. 24

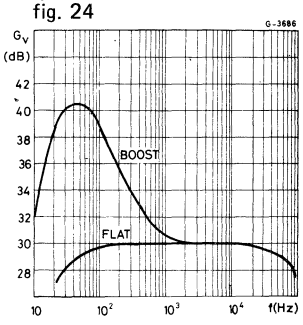


Fig. 26 - Squelch function in TV applications

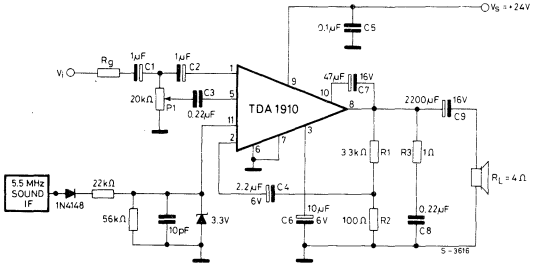
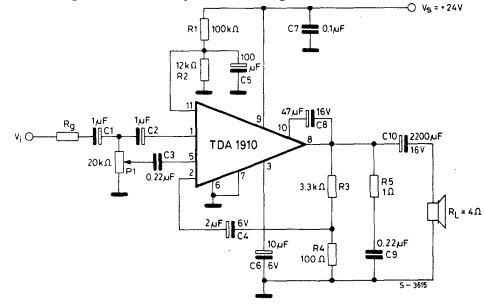


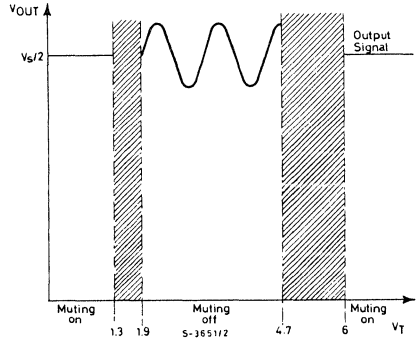
Fig. 27 - Delayed muting circuit



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 11, as shown in fig. 28

Fig. 28

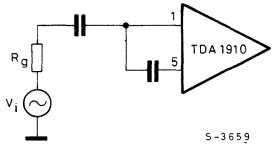


The input resistance at pin 1 depends on the threshold voltage V_T at pin 11 and is typically.

$R_1 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_1 = 10\ \Omega$ @ $0V \leqslant V_T \leqslant 1.3V$ $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression.



$$A_T = \frac{V_i}{V_5} = \frac{R_g + R_5//R_1}{R_5//R_1}$$

where $R_5 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, typically 1.2 dB.
A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 11 is greater than 150 KΩ. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 27)
- during commutations at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 1 can be useful in many applications and we have shown 2 examples in fig. 22 and 24, where it has been used to change the feedback network, obtaining 2 different frequency responses.

APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 21. Different values can be used.
The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range	
					Min.	Max.
$R_g + R_1$	10KΩ	Input signal imped. for muting operation	Increase of the attenuation in muting-on condition.Decrease of the input sensitivity.	Decrease of the attenuation in muting on condition.		
R_2	3.3KΩ	Close loop gain setting.	Increase of gain.	Decrease of gain. Increase quiescent current.	$9\,R_3$	
R_3	100Ω	Close loop gain setting.	Decrease of gain.	Increase of gain.		$R_2/9$
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads.			
P_1	20KΩ	Volume potentiometer.	Increase of the switch-on noise.	Decrease of the input impedance and the input level.	10KΩ	100KΩ
C_1 C_2 C_3	1 μF 1 μF 0.22 μF	Input DC decoupling.		Higher low frequency cutoff.		
C_4	2.2 μF	Inverting input DC decoupling.	Increase of the switch-on noise.	Higher low frequency cutoff.	0.1 μF	
C_5	0.1 μF	Supply voltage bypass.		Danger of oscillations.		
C_6	10 μF	Ripple Rejection.	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.	2.2 μF	100 μF
C_7	47 μF	Bootstrap.		Increase of the distortion at low frequency.	10 μF	100 μF
C_8	0.22 μF	Frequency stability.		Danger of oscillation.		
C_9	2200 μF (R_L = 4Ω) 1000 μF (R_L = 8Ω)	Output DC decoupling.		Higher low frequency cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 31 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 29 - Output power and drain current vs. case temperature

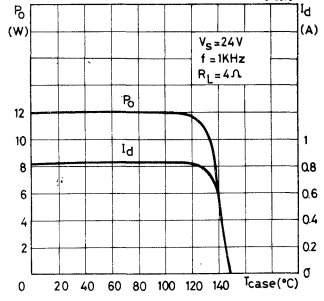


Fig. 30 - Output power and drain current vs. case temperature

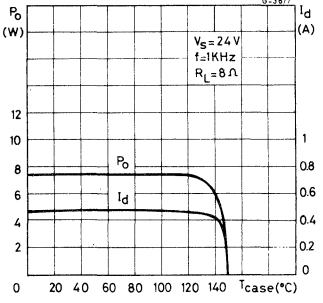
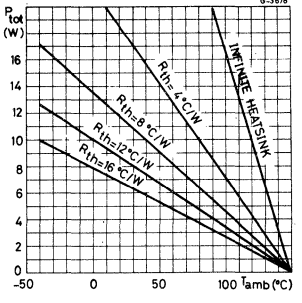


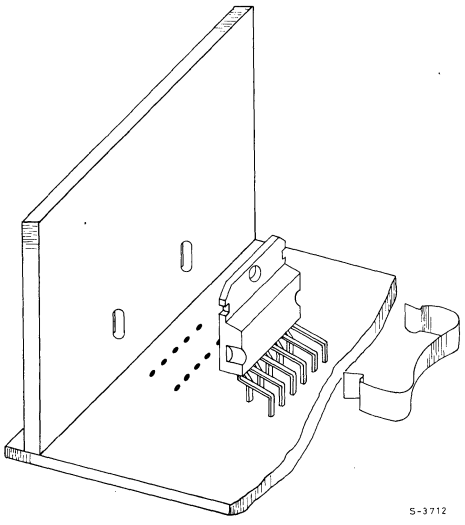
Fig. 31 - Maximum allowable power dissipation vs. ambient temperature

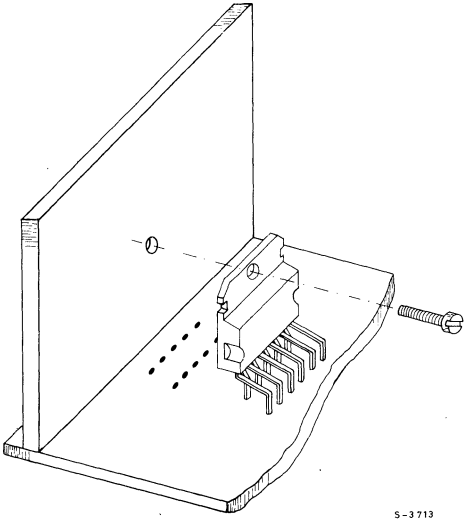


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 34 - Mounting examples





TDA2002

LINEAR INTEGRATED CIRCUIT

8W CAR RADIO AUDIO AMPLIFIER

The TDA 2002 is a class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 1.6Ω). The device provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion. In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use
- complete safety during operation due to protection against:
  a) short circuit; b) thermal over range; c) fortuitous open ground; d) polarity inversion (V_s max= 12V); e) load dump voltage surge.

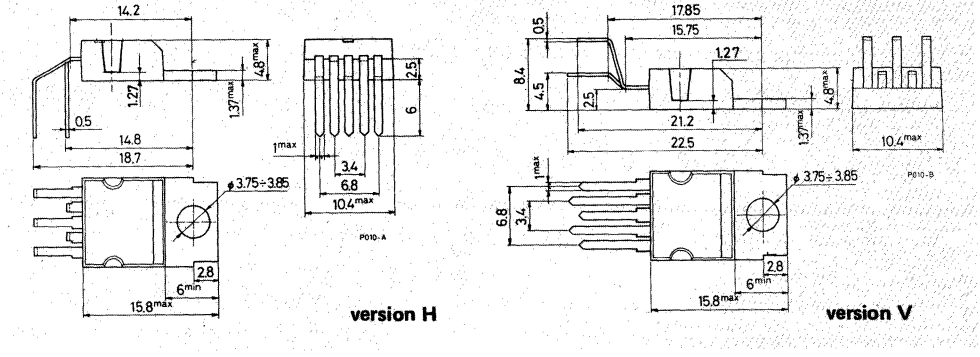
ABSOLUTE MAXIMUM RATINGS

V_s	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	18	V
I_o	Output peak current (repetitive)	3.5	A
I_o	Output peak current (non repetitive)	4.5	A
P_{tot}	Power dissipation at T_{case}= 90°C	15	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

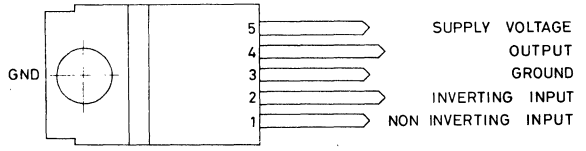
ORDERING NUMBERS: TDA 2002 H
TDA 2002 V

MECHANICAL DATA

Dimensions in mm

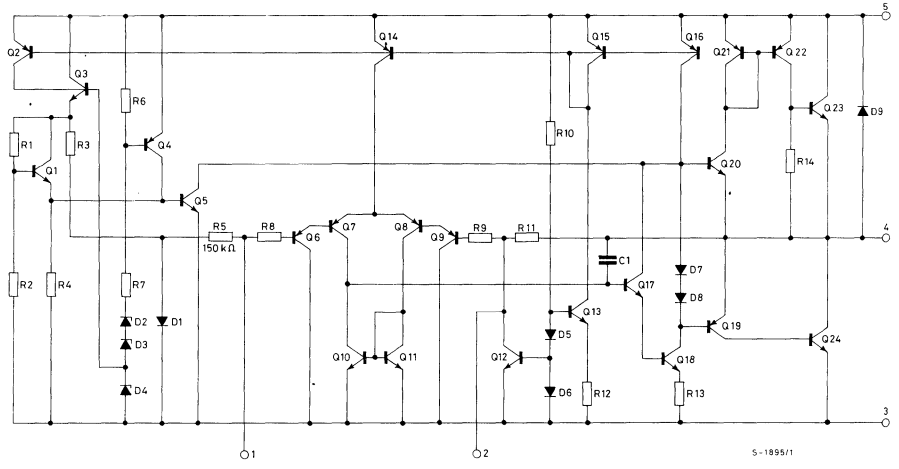


CONNECTION DIAGRAM
(top view)

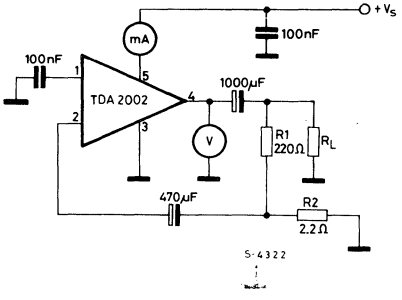


S-1894/1

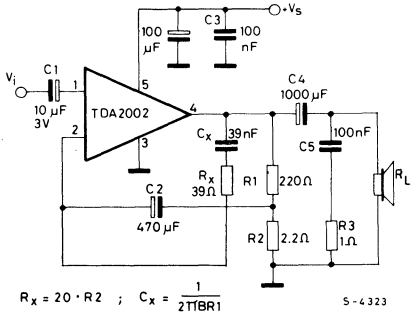
SCHEMATIC DIAGRAM



DC TEST CIRCUIT



AC TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 14.4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS (Refer to DC test circuit)						
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage (pin 4)		6.4	7.2	8	V
I_d	Quiescent drain current (pin 5)			45	80	mA
AC CHARACTERISTICS (Refer to AC test circuit, G_v= 40 dB)						
P_o	Output power	d = 10% f = 1 kHz R_L= 4Ω R_L= 2Ω V_s = 16V R_L= 4Ω R_L= 2Ω	4.8 7	5.2 8 6.5 10		W W W W
$V_{i\,(rms)}$	Input saturation voltage		600			mV
V_i	Input sensitivity	f = 1 kHz P_o = 0.5W R_L= 4Ω P_o = 0.5W R_L= 2Ω P_o = 5.2W R_L= 4Ω P_o= 8W R_L= 2Ω		15 11 55 50		mV mV mV mV
B	Frequency response (-3 dB)	R_L= 4Ω P_o= 1W	40 to 15 000			Hz
d	Distortion	f = 1 kHz P_o = 0.05 to 3.5W R_L= 4Ω P_o = 0.05 to 5W R_L= 2Ω		0.2 0.2		% %
R_i	Input resistance (pin 1)	f = 1 kHz	70	150		kΩ
G_V	Voltage gain (open loop)	R_L= 4Ω f = 1 kHz		80		dB
G_V	Voltage gain (closed loop)	R_L= 4Ω f = 1 kHz	39.5	40	40.5	dB
e_N	Input noise voltage (*)			4		μV
i_N	Input noise current (*)			60		pA
η	Efficiency	f = 1 kHz P_o = 5.2W R_L= 4Ω P_o = 8W R_L= 2Ω		68 58		% %
SVR	Supply voltage rejection	R_L= 4Ω R_g= 10 kΩ f_{ripple}= 100 Hz	30	35		dB

(*) Filter with noise bandwidth: 22 Hz to 22 KHz.

Fig. 1 - Quiescent output voltage vs. supply voltage

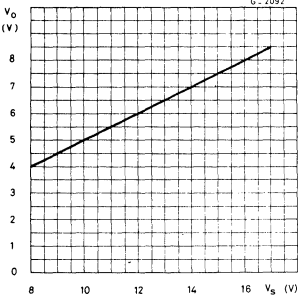


Fig. 2 - Quiescent drain current vs. supply voltage

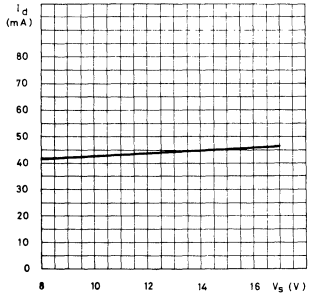


Fig. 3 - Output power vs. supply voltage

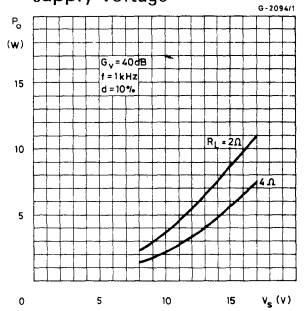


Fig. 4 - Output power vs. load resistance R_L

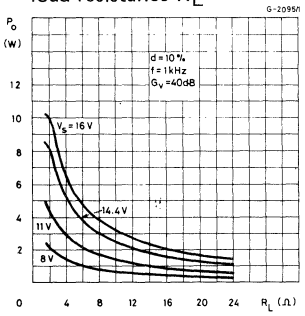


Fig. 5 - Input voltage vs. voltage gain ($R_L = 4\Omega$)

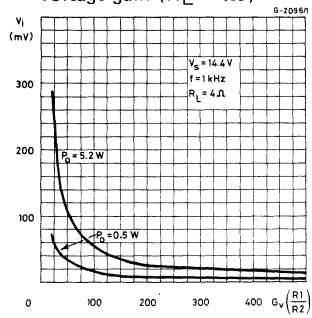


Fig. 6 - Input voltage vs. voltage gain ($R_L = 2\Omega$)

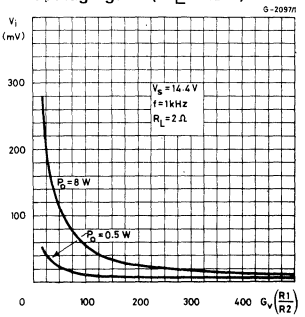


Fig. 7 - Distortion vs. output power

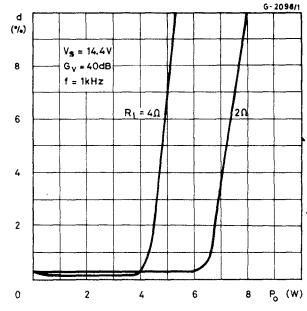


Fig. 8 - Distortion vs. frequency

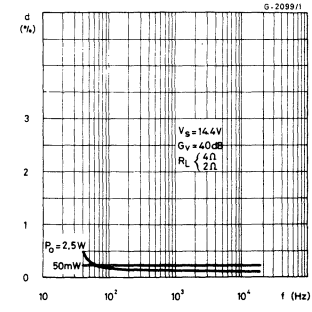


Fig. 9 - Supply voltage rejection vs. voltage gain

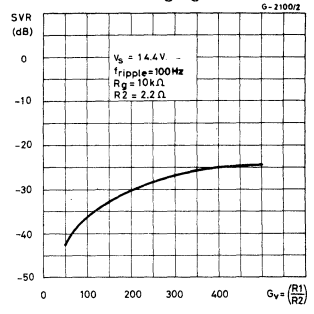


Fig. 10 - Supply voltage rejection vs. frequency

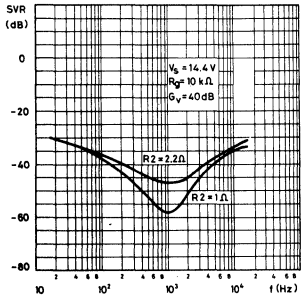


Fig. 11 - Power dissipation and efficiency vs. output power ($R_L = 4\Omega$)

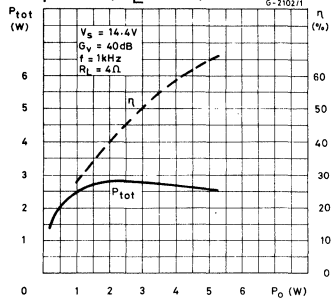


Fig. 12 - Power dissipation and efficiency vs. output power ($R_L = 2\Omega$)

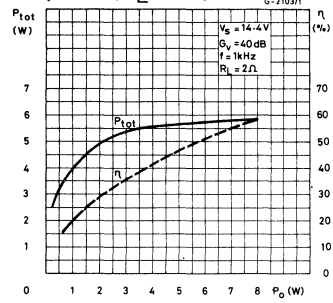


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

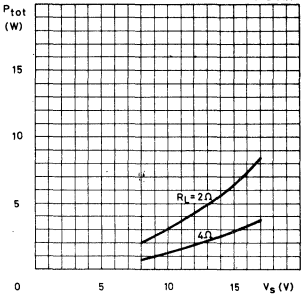


Fig. 14 - Maximim allowable power dissipation vs. ambient temperature

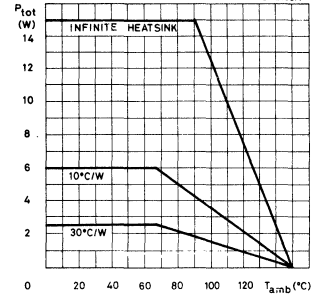
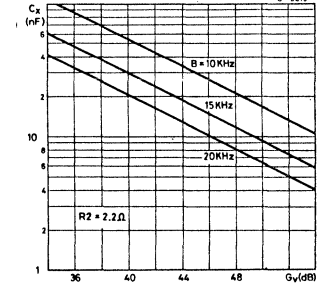


Fig. 15 - Values of capacitor (C_X) for different values of frequency response (B)



APPLICATION INFORMATION

Fig. 16 - Application circuit

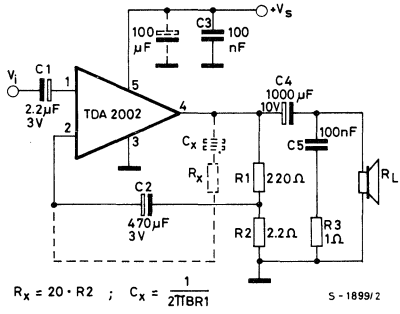
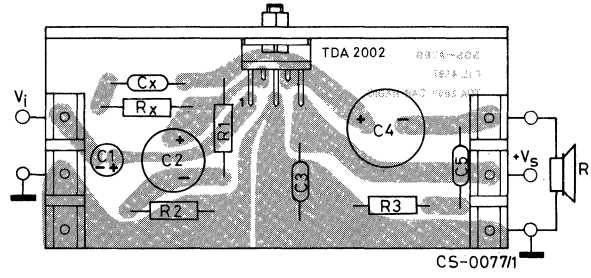


Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)



LOAD DUMP VOLTAGE SURGE PROTECTION

The TDA 2002 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 18. If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig.18.
A suggested LC network is shown in fig. 19. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

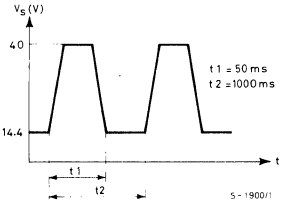
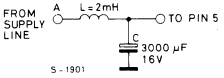


Fig. 19



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:
1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood
2) the heat-sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced (figs. 20 and 21)

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

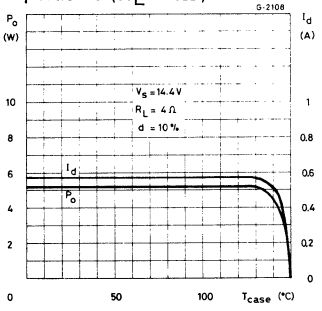
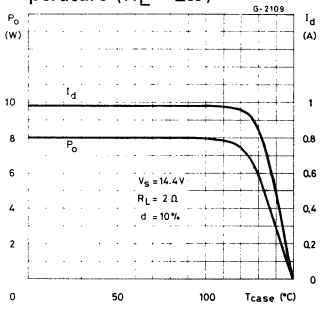


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 2\Omega$)



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion

No electrical insulation is needed between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions

The recommended component values are those shown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_X	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(G_V-1) \cdot R2$	Setting of gain		Increase of drain current
R2	2.2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_X	≅ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

LINEAR INTEGRATED CIRCUIT

TDA2003

10W CAR RADIO AUDIO AMPLIFIER

The TDA 2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002, very low number of external components, ease of assembly, space and cost saving, are maintained.
The device provides a high output current capability (up to 3.5A) very low harmonic and cross-over distortion.
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range, load dump voltage surge up to 40V, polarity inversion and fortuitous open ground.

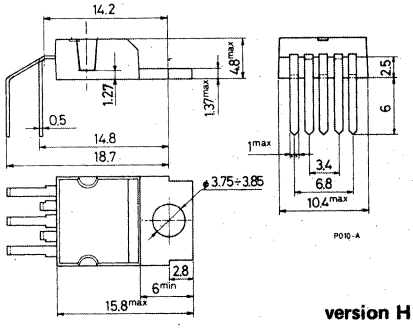
ABSOLUTE MAXIMUM RATINGS

V_s	Peak supply voltage (50 ms)	40	V
V_s	DC supply voltage	28	V
V_s	Operating supply voltage	18	V
I_o	Output peak current (repetitive)	3.5	A
I_o	Output peak current (non repetitive)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

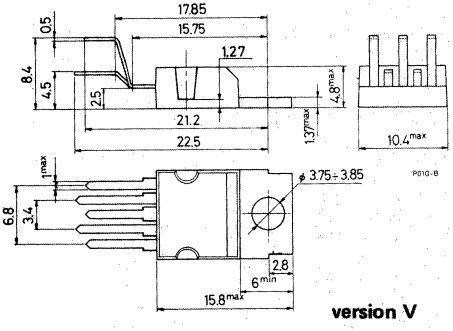
ORDERING NUMBERS: TDA 2003H
TDA 2003V

MECHANICAL DATA

Dimensions in mm

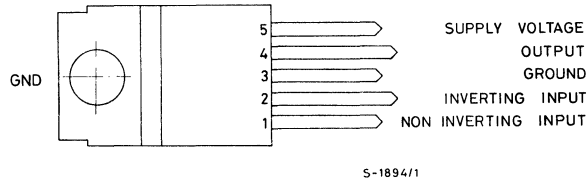


version H

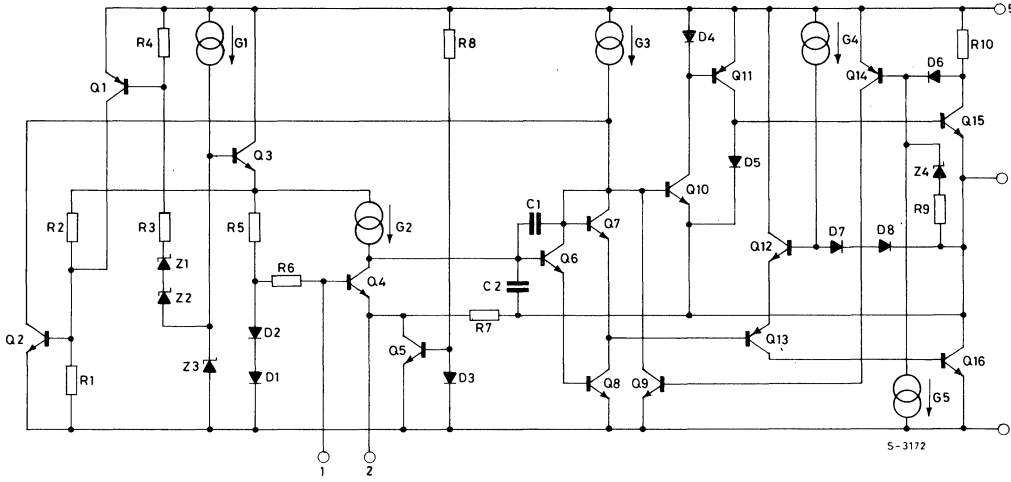


version V

CONNECTION DIAGRAM
(top view)



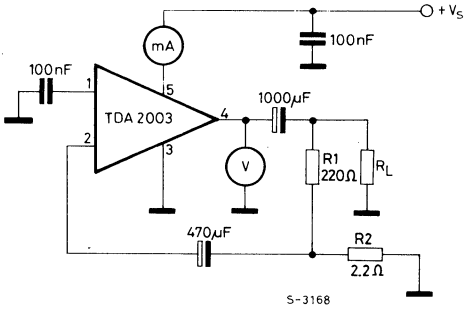
SCHEMATIC DIAGRAM



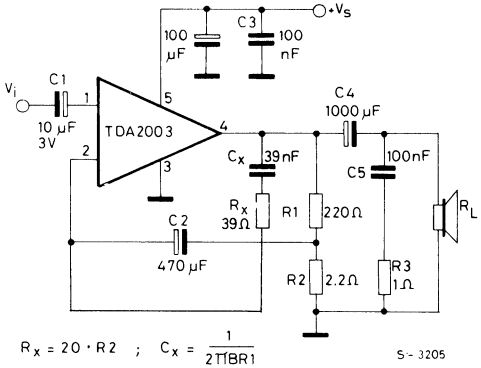
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

DC TEST CIRCUIT



AC TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_s= 14.4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS (Refer to DC test circuit)							
V_s	Supply voltage			8		18	V
V_o	Quiescent output voltage (pin 4)			6.1	6.9	7.7	V
I_d	Quiescent drain current (pin 5)				44	50	mA
AC CHARACTERISTICS (Refer to AC test circuit, G_v= 40 dB)							
P_o	Output power	d = 10% f = 1 kHz	R_L= 4Ω R_L= 2Ω R_L= 3.2Ω R_L= 1.6Ω	5.5 9	6 10 7.5 12		W W W W
$V_{i(rms)}$	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 kHz P_o = 0.5W P_o = 6W P_o = 0.5W P_o = 10W	 R_L= 4Ω R_L= 4Ω R_L= 2Ω R_L= 2Ω		 14 55 10 50		 mV mV mV mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
B	Frequency response (–3 dB)	P_o = 1W R_L = 4Ω		40 to 15,000		Hz
d	Distortion	f = 1 kHz P_o = 0.05 to 4.5W R_L = 4Ω P_o = 0.05 to 7.5W R_L = 2Ω		0.15 0.15		% %
R_i	Input resistance (pin 1)	f = 1 kHz	70	150		kΩ
G_v	Voltage gain (open loop)	f = 1 kHz f = 10 kHz		80 60		dB dB
G_v	Voltage gain (closed loop)	f = 1 kHz R_L = 4Ω	39.5	40	40.5	dB
e_N	Input noise voltage (0)			1	5	μV
i_N	Input noise current (0)			60	200	pA
η	Efficiency	f = 1 kHz P_o = 6W R_L = 4Ω P_o = 10W R_L = 2Ω		69 65		% %
SVR	Supply voltage rejection	f = 100 Hz V_{ripple} = 0.5V R_g = 10 kΩ R_L = 4Ω	30	36		dB

(0) Filter with noise bandwidth: 22 Hz to 22 kHz

Fig. 1 - Quiescent output voltage vs. supply voltage

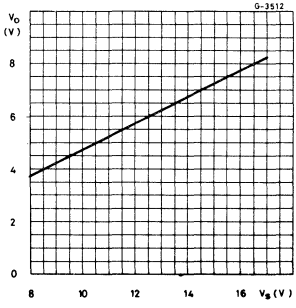


Fig. 2 - Quiescent drain current vs. supply voltage

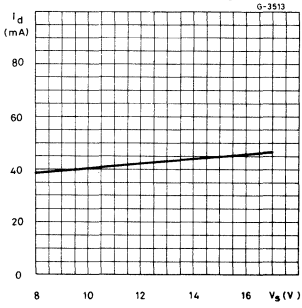


Fig. 3 - Output power vs. supply voltage

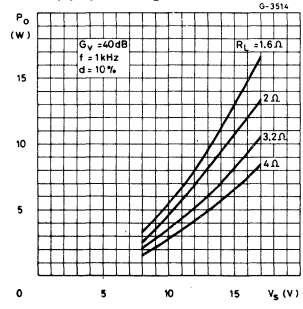


Fig. 4 - Output power vs. load resistance R_L

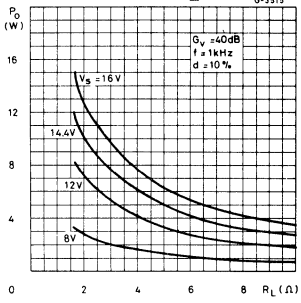


Fig. 5 - Gain vs. input sensitivity

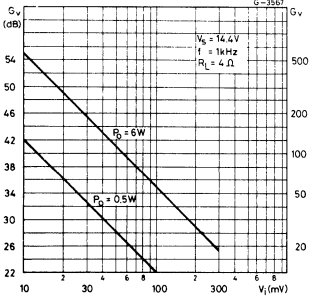


Fig. 6 - Gain vs. input sensitivity

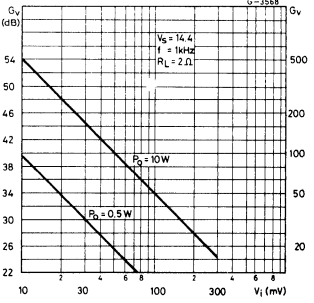


Fig. 7 - Distortion vs. output power

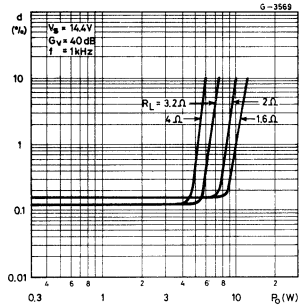


Fig. 8 - Distortion vs. frequency

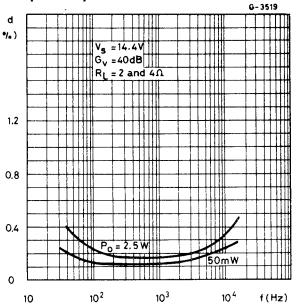


Fig. 9 - Supply voltage rejection vs. voltage gain

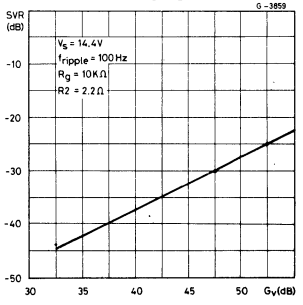


Fig. 10 - Supply voltage rejection vs. frequency

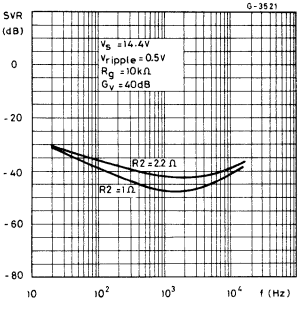


Fig. 11 - Power dissipation and efficiency vs. output power (R_L = 4Ω)

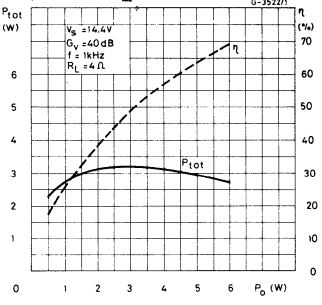


Fig. 12 - Power dissipation and efficiency vs. output power (R_L = 2Ω)

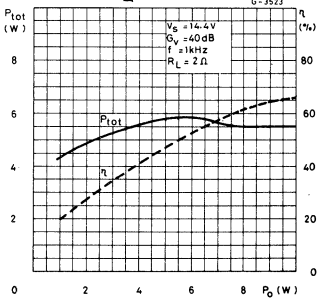


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

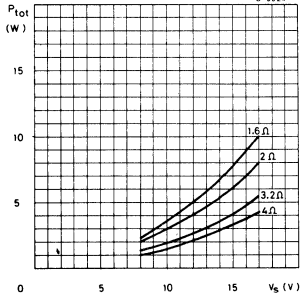


Fig. 14 - Maximum allowable power dissipation vs. ambient temperature

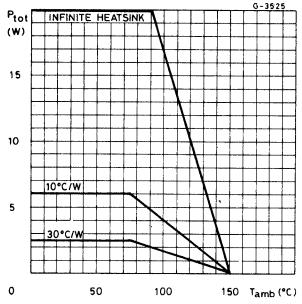
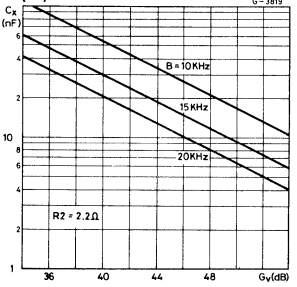


Fig. 15 - Typical values of capacitor (C_X) for different values of frequency response (B)



APPLICATION INFORMATION

Fig. 16 - Typical application circuit

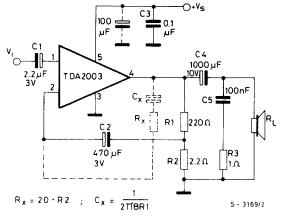


Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)

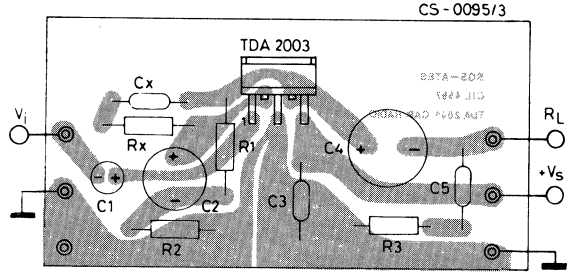
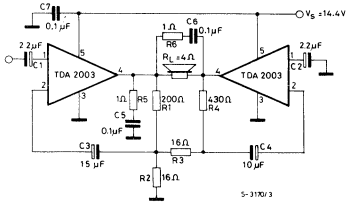
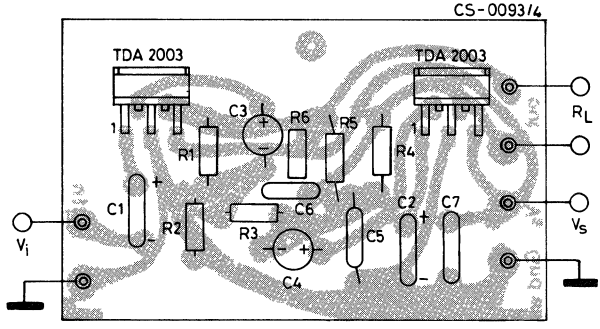


Fig. 18 - 20W bridge configuration application circuit (*)



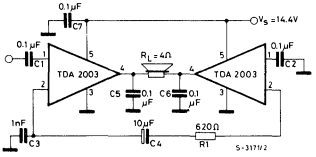
(*) The values of the capacitors C3 and C4 are different to optimize the SVR (Typ.= 40 dB)

Fig. 19 - P.C. board and component layout for the circuit of fig. 18 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 20 - Low cost bridge configuration application circuit (*) (P_o= 18W)



(*) In this application the device can support a short circuit between every side of the loudspeaker and ground.

Fig. 21 - P.C. board and component layout for the circuit of fig. 20 (1:1 scale)

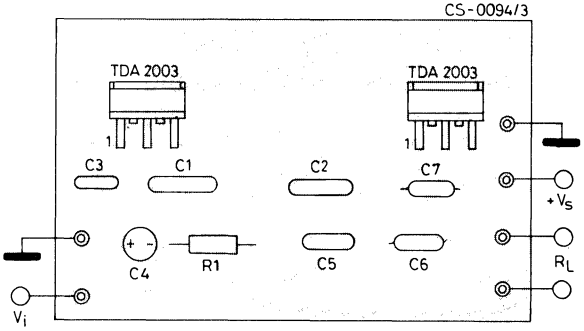
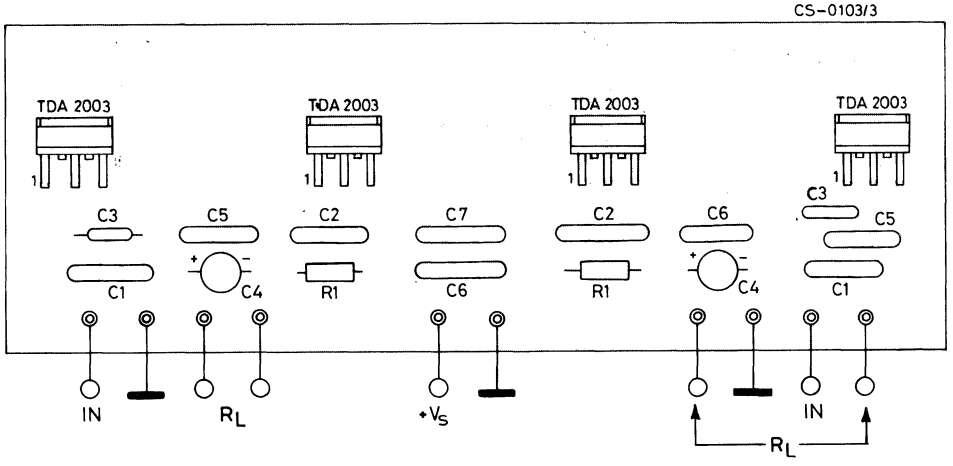


Fig. 22 - P.C. board and component layout for the low-cost bridge amplifier of fig. 20, in stereo version (1:1 scale)



BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA 2003 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 23.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 23. A suggested LC network is shown in fig. 24. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 23

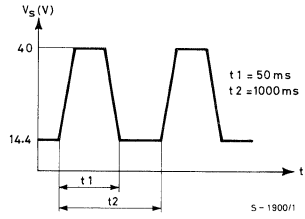
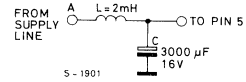


Fig. 24



Short-circuit (AC and DC conditions)

The TDA 2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1A fuse (normally connected in series with the supply).
This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2003 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA 2003 with inductive loads.
In particular, the TDA 2003 can drive a coupling transformer for audio modulation.

DC voltage

The maximum operating DC voltage on the TDA 2003 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:
1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heat-sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced (figs. 25 and 26).

Fig. 25 - Output power and drain current vs. case temperature (R_L = 4 Ω)

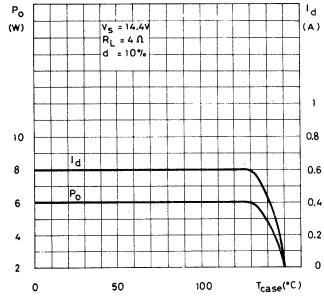
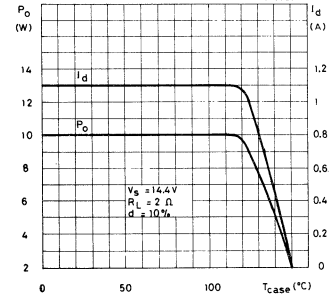


Fig. 26 - Output power and drain current vs. case temperature (R_L = 2Ω)



PRATICAL CONSIDERATIONS

Printed circuit board
The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

Assembly suggestion
No electrical insulation is required between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

Application suggestions
The recommended component values are those shown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	2.2 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of SVR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
C_X	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(G_V-1) \cdot R2$	Setting of gain		Increase of drain current
R2	2.2 Ω	Setting of gain and SVR	Degradation of SVR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_X	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

TDA2004

LINEAR INTEGRATED CIRCUIT

10 + 10W STEREO AMPLIFIER FOR CAR RADIO

The TDA 2004 is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio applications: stereo amplifiers are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6Ω).
Its main features are:

Low distortion.
Low noise.
High reliability of the chip and of the package with additional complete safety during operation thanks to protections against:
- output AC short circuit to ground
- very inductive loads
- overrating chip temperature
- load dump voltage surge
- fortuitous open ground
- polarity inversion

Space and cost saving: very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).

ABSOLUTE MAXIMUM RATINGS

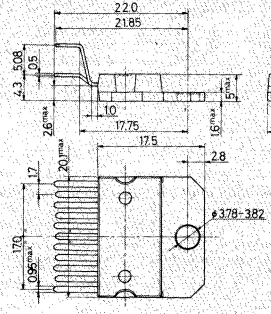
V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50 ms)	40	V
I_o (*)	Output peak current (non repetitive t = 0.1 ms)	4.5	A
I_o (*)	Output peak current (repetitive f ⩾ 10 Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 60 °C	30	W
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

(*) The max. output current is internally limited.

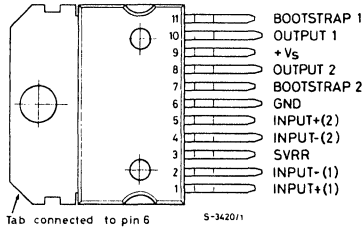
ORDERING NUMBER: TDA 2004

MECHANICAL DATA

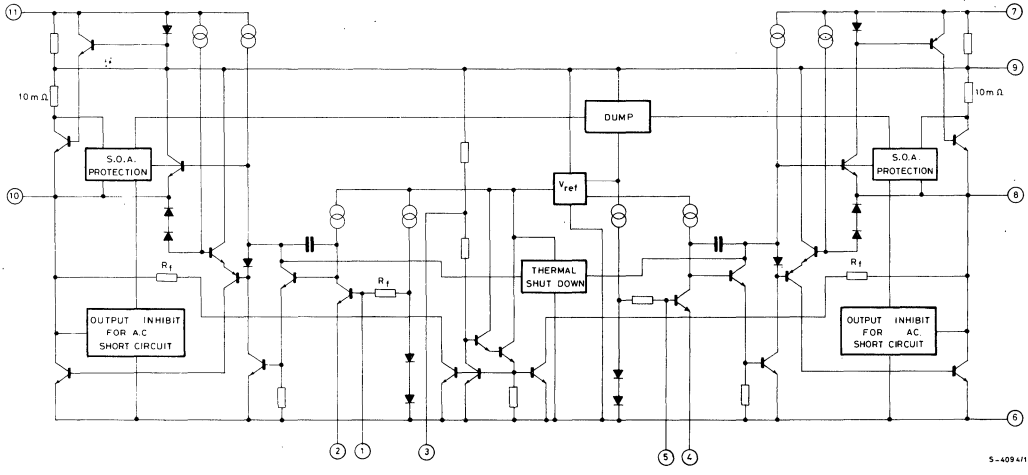
Dimensions in mm



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

Fig. 1 - Test and application circuit

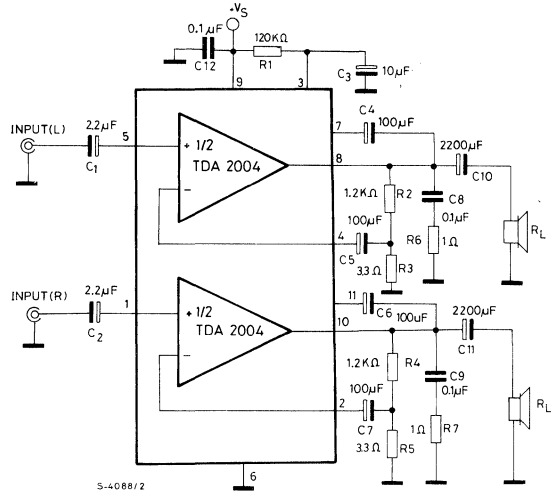
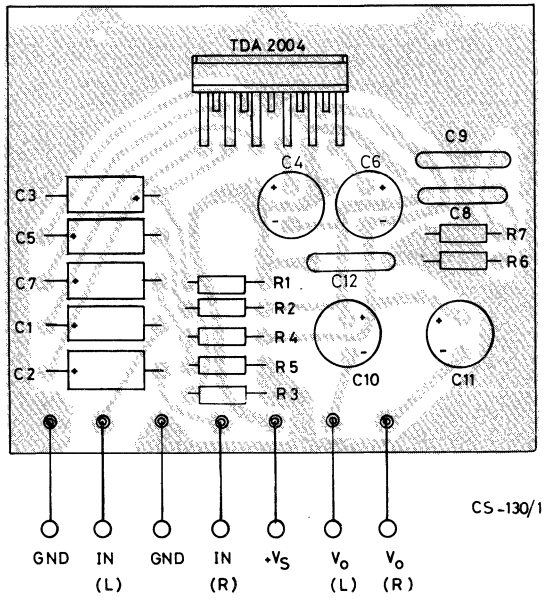


Fig. 2 - PC board and components layout (scale 1:1)



ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_o	Quiescent output voltage	V_s = 14.4V V_s = 13.2V	6.6 5.0	7.2 6.6	7.8 7.2	V V
I_d	Total quiescent drain current	V_s = 14.4V V_s = 13.2V		65 62	120 120	mA mA
I_{SB}	Stand-by current	Pin 3 grounded		5		mA
P_o	Output power (each channel)	f = 1 KHz d = 10% V_s = 14.4V R_L= 4Ω R_L= 3.2Ω R_L= 2Ω R_L= 1.6Ω V_s = 13.2V R_L= 3.2Ω R_L= 1.6Ω V_s = 16V R_L= 2 Ω	 6 7 9 10 6 9 	 6.5 8 10(*) 11 6.5 10 12	 	 W W W W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o= 50 mW to 4W V_s = 14.4V R_L= 2Ω P_o= 50 mW to 6W V_s = 13.2V R_L= 3.2Ω P_o= 50 mW to 3W V_s = 13.2V R_L= 1.6Ω P_o= 50 mW to 6W		0.2 0.3 0.2 0.3	1 1 1 1	% % % %
CT	Cross talk	V_s = 14.4V V_o= 4 V_{rms} R_L= 4Ω f = 1 KHz f = 10 KHz	 50 40	 60 45	 	 dB dB
V_i	Input sensitivity	f = 1 KHz P_o = 1W R_L= 4Ω R_L= 3.2Ω		 6 5.5	 	 mV mV
V_i	Input saturation voltage		300			mV
R_i	Input resistance (non inverting input)	f = 1 KHz	70	200		KΩ
R_i	Input resistance (inverting input)	f = 1 KHz		10		KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 4Ω R_L= 2Ω R_L= 3.2Ω R_L= 1.6Ω			35 50 40 55	Hz Hz Hz Hz
f_H	High frequency roll off (-3 dB)	R_L= 4Ω R_L= 2Ω R_L= 3.2Ω R_L= 1.6Ω	15 15 15 15			KHz KHz KHz KHz

ELECTRICAL CHARACTERISTICS (continued)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
G_v	Voltage gain (open loop)	f = 1 KHz		90		dB
G_v	Voltage gain (closed loop)	f = 1 KHz	48	50	51	dB
	Closed loop gain matching			0.5		dB
e_N	Total input noise voltage	R_g= 10 KΩ(°)		1.5	5	μV
SVR	Supply voltage rejection	f_{ripple}= 100 Hz R_g= 10 KΩ C_3= 10 μF V_{ripple}=0.5V_{rms}	35	45		dB
η	Efficiency	V_s = 14.4V f = 1 KHz R_L= 4Ω P_o= 6.5W R_L= 2Ω P_o= 10W V_s= 13.2V f = 1 KHz R_L= 3.2Ω P_o= 6.5W R_L= 1.6Ω P_o= 10W		70 60 70 60		% % % %
T_{sd}	Thermal shut down case temperature	V_s = 14.4V R_L= 4Ω f = 1 KHz P_{tot}= 5.5W	125	135		°C

(*) 9.3W without bootstrap.
(°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Quiescent output voltage vs. supply voltage

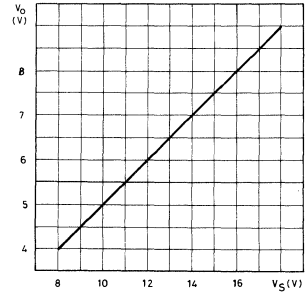


Fig. 4 - Quiescent drain current vs. supply voltage

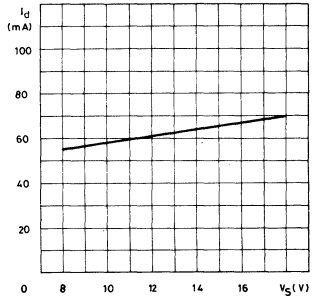


Fig. 5 - Distortion vs. output power

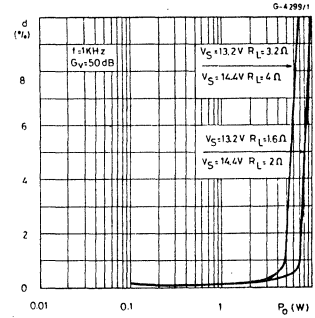


Fig. 6 - Output power vs. supply voltage

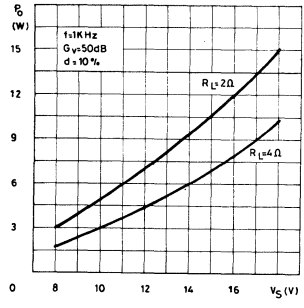


Fig. 7 - Output power vs. supply voltage

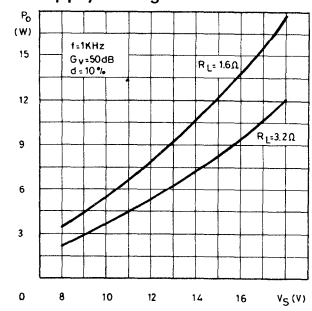


Fig. 8 - Distortion vs. frequency

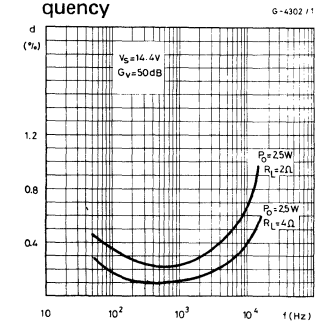


Fig. 9 - Distortion vs. frequency

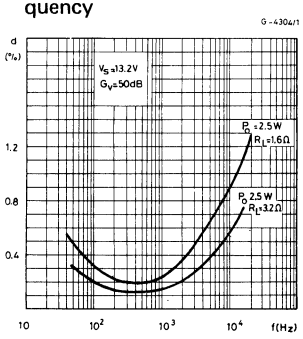


Fig. 10 - Supply voltage rejection vs. C_3

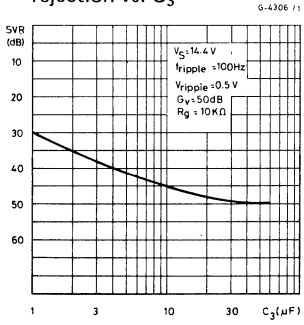


Fig. 11 - Supply voltage rejection vs. frequency

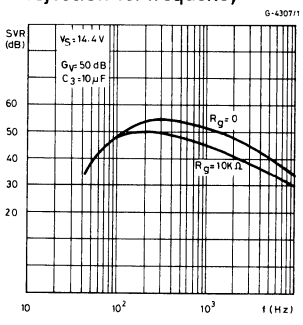


Fig. 12 - Supply voltage rejection vs. values of capacitors C_2 and C_3

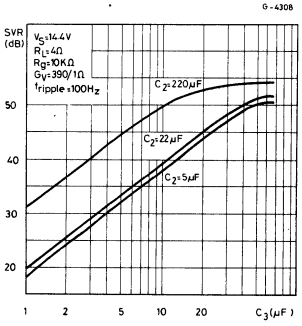


Fig. 13 - Supply voltage rejection vs. values of capacitors C_2 and C_3

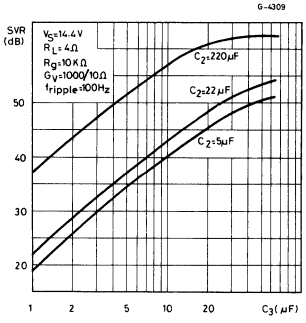


Fig. 14 - Gain vs. input sensitivity

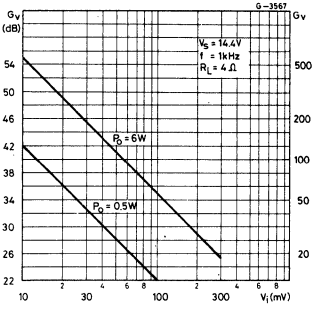


Fig. 15 - Gain vs. input sensitivity

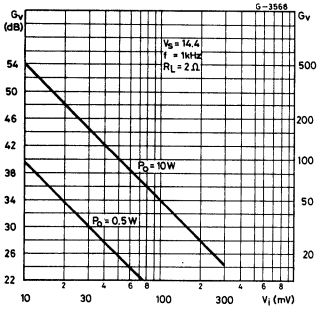


Fig. 16 - Total power dissipation and efficiency vs. output power

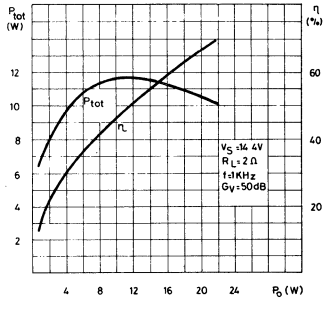
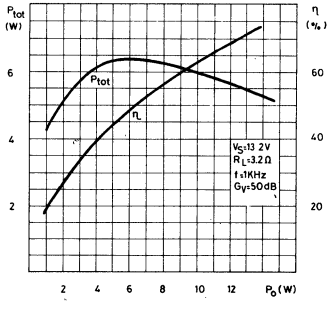


Fig. 17 - Total power dissipation and efficiency vs. output power



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

Component	Recomm. value	Purpose	Larger than	Smaller than
R_1	120 KΩ	Optimisation of the output signal simmetry	Smaller $P_{o\ max}$	Smaller $P_{o\ max}$
R_2 and R_4	1 KΩ	Close loop gain setting	Increase of gain	Decrease of gain
R_3 and R_5	3.3 Ω		Decrease of gain	Increase of gain
R_6 and R_7	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C_1 and C_2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise.
C_3	10 μF	Ripple rejection	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.
C_4 and C_6	100 μF	Bootstrapping		Increase of distortion at low frequency.
C_5 and C_7	100 μF	Feedback Input DC decoupling.		
C_8 and C_9	0.1 μF	Frequency stability.		Danger of oscillation.
C_{10} and C_{11}	1000 μF to 2200 μF	Output DC decoupling.		Higher low-frequency cut-off.

BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA 2004 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in fig. 19.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.
A suggested LC network is shown in fig. 18. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied to point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

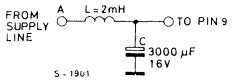
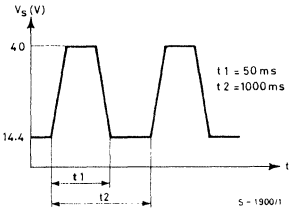


Fig. 19



Short circuit (AC conditions)

The TDA 2004 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2004 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided to allow use of the TDA 2004 with inductive loads.

DC voltage

The maximum operating DC voltage on the TDA 2004 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

BUILD-IN PROTECTION SYSTEMS (continued)

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 20 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 20 - Maximum allowable power dissipation vs. ambient temperature

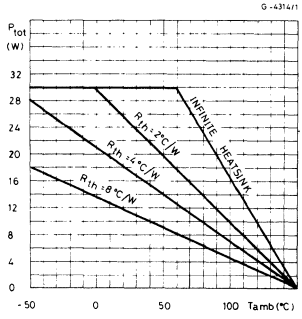


Fig. 21 - Output power and drain current vs. case temperature

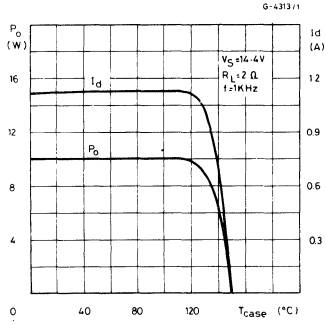
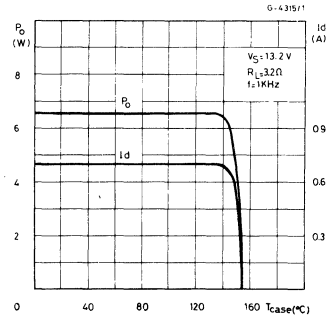


Fig. 22 - Output power and drain current vs. case temperature

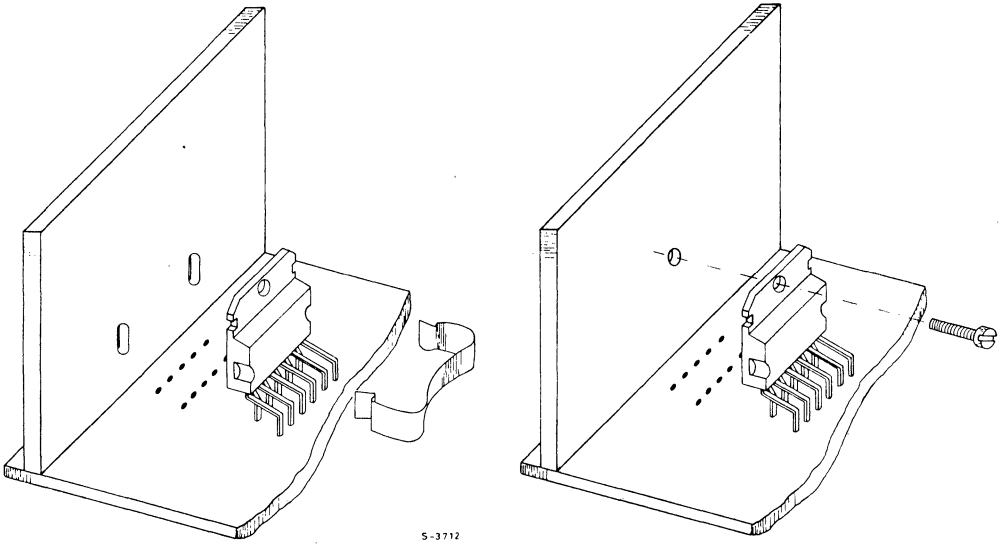


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

MOUNTING INSTRUCTIONS (continued)

Fig. 23 - Mounting examples



TDA2005

LINEAR INTEGRATED CIRCUIT

20 W BRIDGE AMPLIFIER FOR CAR RADIO

The TDA 2005 is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio application: **power booster amplifiers** are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6 Ω in stereo applications) obtaining an output power of more than 20W (bridge configuration).

High output power: $P_o = 10 + 10W$ @ $R_L = 2\Omega$, d = 10% ; $P_o = 20W$ @ $R_L = 4\Omega$, d = 10%

High reliability of the chip and package with additional complete safety during operation thanks to protection against:

- output DC and AC short circuit to ground.
- overrating chip temperature (150°C)
- load dump voltage surge.
- fortuitous open ground.
- polarity inversion.
- very inductive loads.

Flexibility in use: bridge or stereo booster amplifiers with or without bootstrap and with programmable gain and bandwidth.

Space and cost saving: very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).
In addition, the circuit offers **loudspeaker protection** during short circuit for one wire to ground.

ABSOLUTE MAXIMUM RATINGS

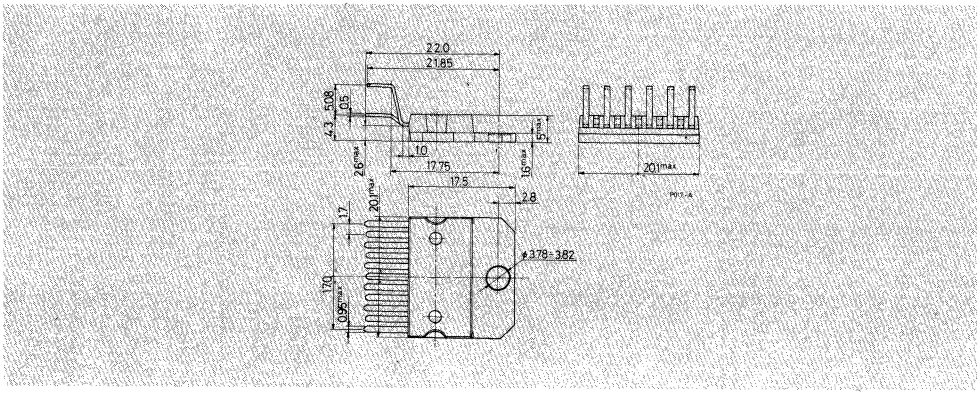
V_s	Operating supply voltage	18	V
V_s	DC supply voltage	28	V
V_s	Peak supply voltage (for 50 ms)	40	V
I_o (*)	Output peak current (non repetitive t = 0.1 ms)	4.5	A
I_o (*)	Output peak current (repetitive f ⩾ 10Hz)	3.5	A
P_{tot}	Power dissipation at T_{case} = 60°C	30	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150°	C

(*) The max. output current is internally limited

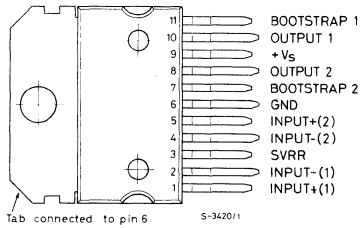
ORDERING NUMBERS: TDA 2005 M - Bridge application
TDA 2005 S - Stereo application

MECHANICAL DATA

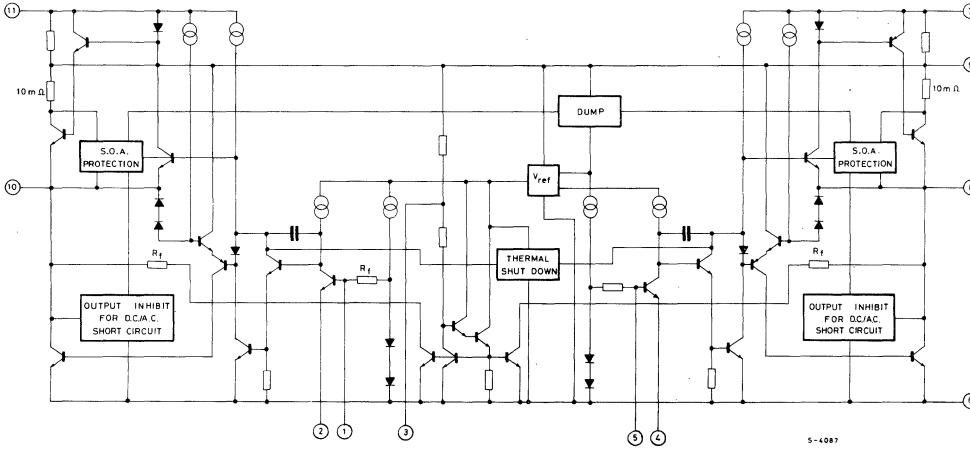
Dimensions in mm



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

BRIDGE AMPLIFIER APPLICATION (TDA 2005M)

Fig. 1 - Test and application circuit (Bridge amplifier)

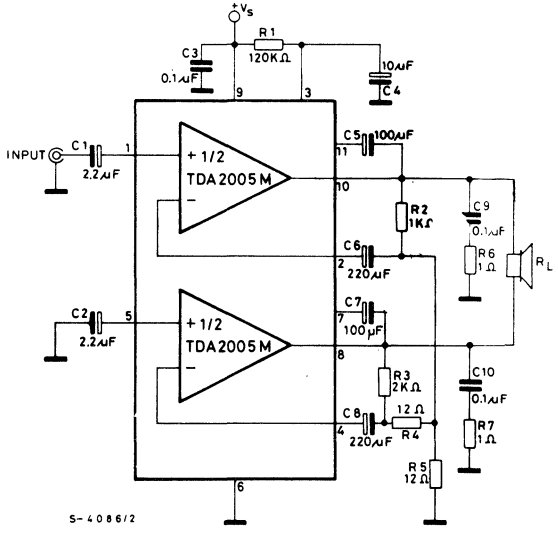
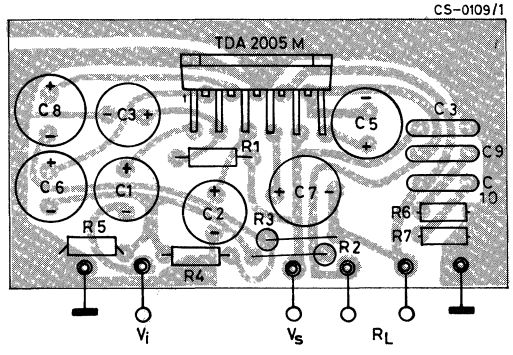


Fig. 2 - P.C. board and component layout (scale 1:1)



ELECTRICAL CHARACTERISTICS (Refer to the **bridge** application circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$= 4°C/W, unless otherwise specified).

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		18	V
V_{os}	Output offset voltage(°) (between pin 8 and 10)	V_s = 14.4V V_s = 13.2V			150 150	mV mV
I_d	Total quiescent drain current	V_s = 14.4V R_L= 4Ω		75	150	mA
		V_s = 13.2V R_L= 3.2 Ω		70	160	mA
P_o	Output power	d = 10% f = 1 KHz				
		V_s = 14.4V R_L= 4Ω	18	20		W
		R_L= 3.2Ω	20	22		W
		V_s = 13.2V R_L= 3.2Ω	17	19		W
d	Distortion	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o = 50 mW to 15W			1	%
		V_s = 13.2V R_L= 3.2Ω P_o = 50 mW to 13W			1	%
V_i	Input sensitivity	f = 1 KHz P_o = 2W R_L= 4Ω		9		mV
		P_o = 2W R_L= 3.2Ω		8		mV
R_i	Input resistance	f = 1 KHz	70			KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 3.2 Ω			40	Hz
f_H	High frequency roll off (-3 dB)	R_L= 3.2 Ω	20			KHz
G_v	Closed loop voltage gain	f = 1 KHz		50		dB
e_N	Total input noise voltage	R_g= 10 KΩ(°°)		3	10	μV
SVR	Supply voltage rejection	R_g= 10 KΩ C_4= 10 μF f_{ripple}= 100 Hz V_{ripple}= 0.5 V	45	55		dB
η	Efficiency	V_s = 14.4V f = 1 KHz P_o = 20W R_L= 4Ω		60		%
		P_o = 22W R_L= 3.2Ω		60		%
		V_s = 13.2V f = 1 KHz P_o = 19W R_L= 3.2Ω		58		%
T_{sd}	Thermal shut-down case temperature	V_s = 14.4V R_L= 4Ω f = 1 KHz P_{tot}= 13W	100	110		°C
V_{OSH}	Output voltage with one side of the speaker shorted to ground	V_s = 14.4V R_L= 4Ω V_s= 13.2V R_L= 3.2Ω			2	V

(°) For TDA 2005M only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Output offset voltage vs. supply voltage

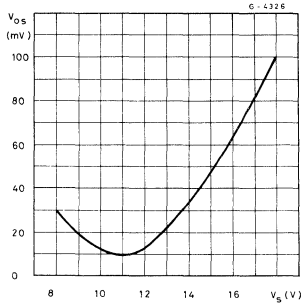


Fig. 4 - Distortion vs. output power (Bridge amplifier)

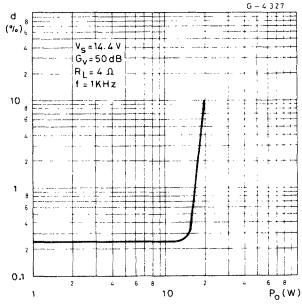
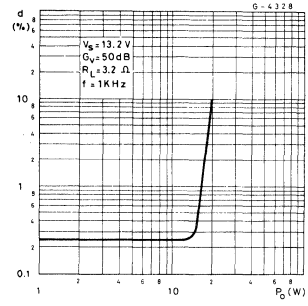


Fig. 5 - Distorsion vs. output power (Bridge amplifier)



BRIDGE AMPLIFIER DESIGN

The following considerations can be useful when designing a bridge amplifier.

Parameter		Single ended	Bridge
$V_{o\ max}$	Peak output voltage (before clipping)	$\frac{1}{2}(V_s - 2\,V_{CE\ sat})$	$V_s - 2\,V_{CE\ sat}$
$I_{o\ max}$	Peak output current (before clipping)	$\frac{1}{2}\frac{(V_s - 2\,V_{CE\ sat})}{R_L}$	$\frac{V_s - 2\,V_{CE\ sat}}{R_L}$
$P_{o\ max}$	rms output power (before clipping)	$\frac{1}{4}\frac{(V_s - 2\,V_{CE\ sat})^2}{2\,R_L}$	$\frac{(V_s - 2\,V_{CE\ sat})^2}{2\,R_L}$

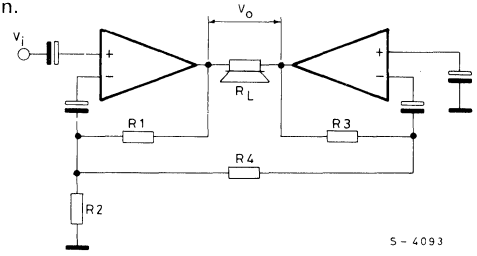
where: $V_{CE\ sat}$ = output transistors saturation voltage
V_S = allowable supply voltage
R_L = load impedance.

Voltage and current swings are twice for a bridge amplifier in comparison with single ended amplifier. In other words, with the same R_L the bridge configuration can deliver an output power that is four times the output power of a single ended amplifier, while, with the same max output current the bridge configuration can deliver an output power that is twice the output power of a single ended amplifier. Care must be taken when selecting V_s and R_L in order to avoid an output peak current above the absolute maximum rating.
From the expression for $I_{o\ max}$, assuming V_s = 14.4V and V_{CEsat}= 2V, the minimum load that can be driven by TDA 2005 in bridge configuration is:

$$R_{Lmin} = \frac{V_s - 2\,V_{CEsat}}{I_{o\ max}} = \frac{14.4 - 4}{3.5} = 2.97\ \Omega$$

BRIDGE AMPLIFIER DESIGN (continued)

Fig. 6 - Bridge configuration.



The voltage gain of the bridge configuration is given by (see fig. 6):

$$G_v = \frac{V_o}{V_i} = 1 + \frac{R_1}{\left(\frac{R_2 \cdot R_4}{R_2 + R_4}\right)} + \frac{R_3}{R_4}$$

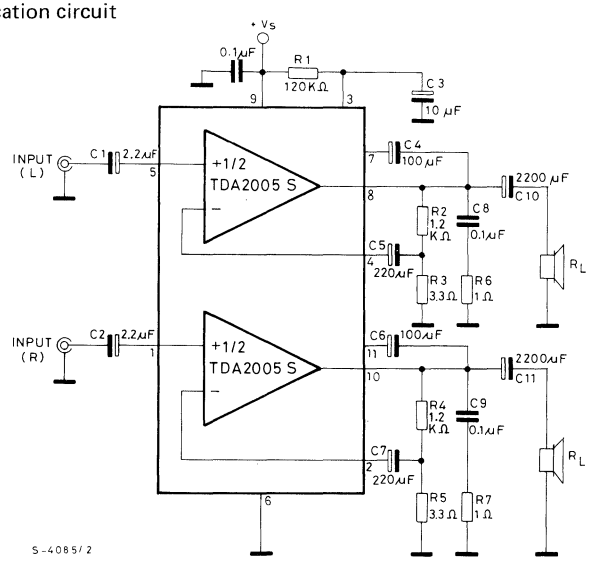
For sufficiently high gains (40 ÷ 50 dB) it is possible to put $R_2 = R_4$ and $R_3 = 2\,R_1$, simplifing the formula in:

$$G_v = 4\,\frac{R_1}{R_2}$$

G_v (dB)	R_1 (Ω)	$R_2 = R_4$ (Ω)	R_3 (Ω)
40	1000	39	2000
50	1000	12	2000

STEREO AMPLIFIER APPLICATION (TDA 2005S)

Fig. 7 - Typical application circuit



ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb}= 25°C, G_v= 50 dB, $R_{th\ (heatsink)}$= 4°C/W, unless otherwise specified).

Parameters		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			8		18	V
V_o	Quiescent output voltage	V_s = 14.4V V_s = 13.2V		6.6 6	7.2 6.6	7.8 7.2	V V
I_d	Total quiescent drain current	V_s = 14.4V V_s = 13.2V			65 62	120 120	mA mA
P_o	Output power (each channel)	f = 1 KHz V_s = 14.4V V_s = 13.2V V_s = 16V	d = 10% R_L= 4Ω R_L= 3.2Ω R_L= 2Ω R_L= 1.6Ω R_L= 3.2Ω R_L= 1.6Ω R_L= 2Ω	 6 7 9 10 6 9	 6.5 8 10 11 6.5 10 12		 W W W W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 14.4V R_L= 4Ω P_o = 50 mW to 4W V_s = 14.4V R_L= 2Ω P_o = 50 mW to 6W V_s = 13.2V R_L= 3.2Ω P_o= 50 mW to 3W V_s = 13.2V R_L= 1.6Ω P_o = 40 mW to 6W			 0.2 0.3 0.2 0.3	 1 1 1 1	 % % % %
CT	Cross talk (°)	V_s= 14.4V R_L= 4Ω	f = 1 KHz		60		dB
		V_o = $4V_{rms}$ R_g= 10 KΩ	f = 10 KHz		45		dB
V_i	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 KHz	P_o = 1W R_L= 4Ω R_L= 3.2Ω		6 5.5		mV
R_i	Input resistance	f = 1 KHz	non inverting input	70	200		KΩ
			inverting input		10		KΩ
f_L	Low frequency roll off (-3 dB)	R_L= 2Ω				50	Hz
f_H	High frequency roll off (-3 dB)	R_L= 2Ω		15			KHz
G_v	Voltage gain (open loop)	f = 1 KHz			90		dB
G_v	Voltage gain (closed loop)	f = 1 KHz		48	50	51	dB
ΔG_v	Closed loop gain matching				0.5		dB
e_N	Total input noise voltage	R_g= 10 KΩ (°°)			1.5	5	μV

(°) For TDA 2005S only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

ELECTRICAL CHARACTERISTICS (continued)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	R_g= 10 KΩ f_{ripple}= 100 Hz C_3= 10 μF V_{ripple}= 0.5V	35	45		dB
η	Efficiency	V_s = 14.4V f = 1 KHz R_L= 4Ω P_o= 6.5W R_L= 2Ω P_o= 10W V_s = 13.2V f = 1 KHz R_L= 3.2Ω P_o= 6.5W R_L= 1.6Ω P_o= 10W		 70 60 70 60		 % % % %
T_{sd}	Thermal shut-down case temperature	V_s = 14.4V R_L= 2Ω P_{tot}= 6.6W	120	130		°C

Fig. 8 - Quiescent output voltage vs. supply voltage

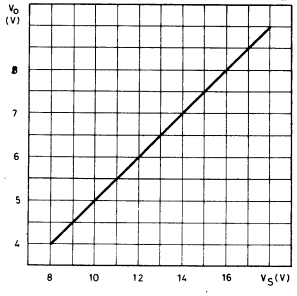


Fig. 9 - Quiescent drain current vs. supply voltage

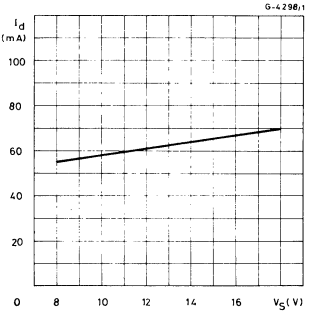


Fig. 10 - Distortion vs. output power

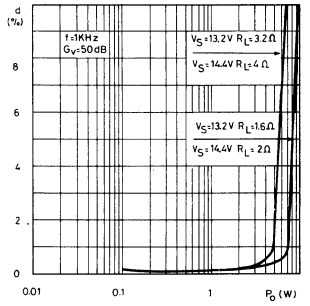


Fig. 11 - Output power vs. supply voltage

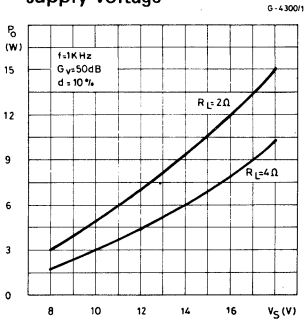


Fig. 12 - Output power vs. supply voltage

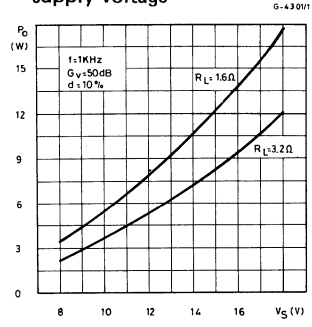


Fig. 13 - Distortion vs. frequency

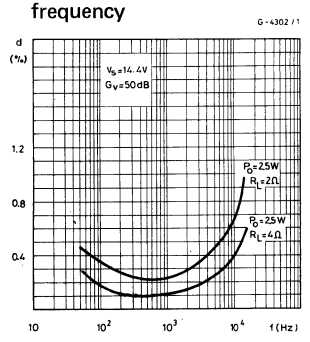


Fig. 14 - Distorsion vs. frequency

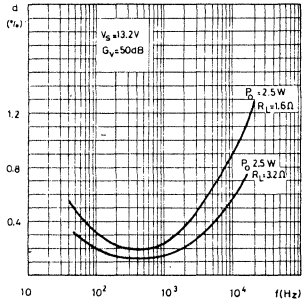


Fig. 15 - Supply voltage rejection vs. C_3

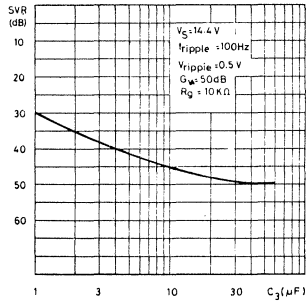


Fig. 16 - Supply voltage rejection vs. frequency

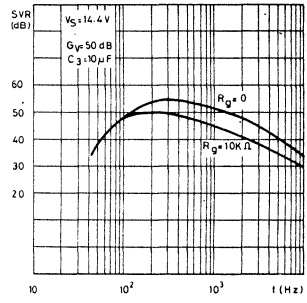


Fig. 17 - Supply voltage rejection vs. values of capacitors C_2 and C_3

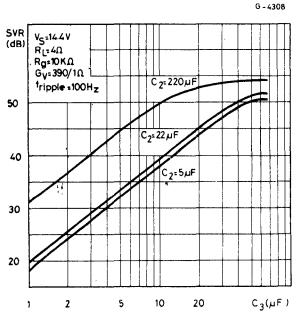


Fig. 18 - Supply voltage rejection vs. values of capacitors C_2 and C_3

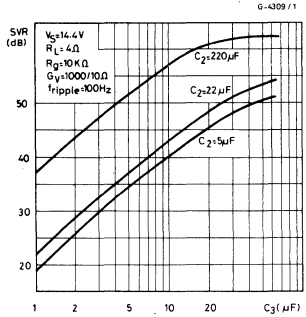


Fig. 19 - Gain vs. input sensitivity

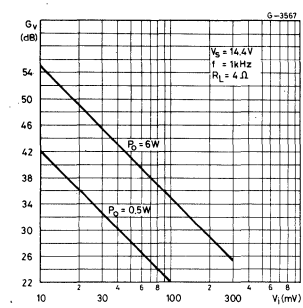


Fig. 20 - Gain vs. input sensitivity

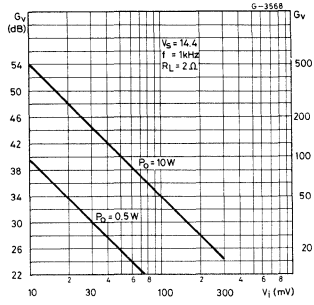


Fig. 21 - Total power dissipation and efficiency vs. output power (bridge)

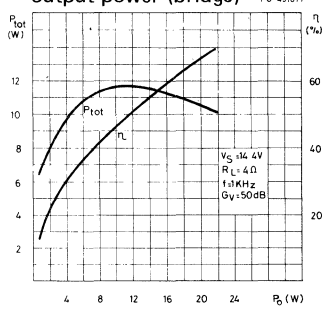
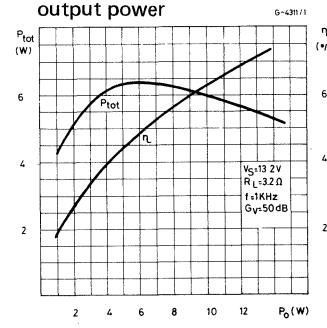


Fig. 22 - Total power dissipation and efficiency vs. output power



APPLICATION INFORMATION

Fig. 23 - 10 + 10W stereo amplifier with tone balance and loudness control

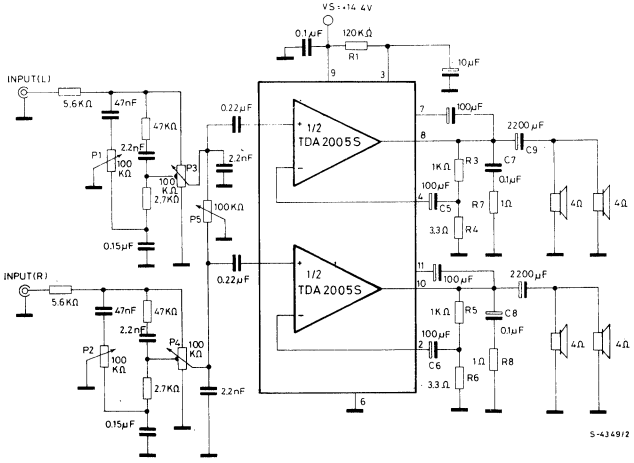


Fig. 24 - Tone control response (circuit of fig. 23)

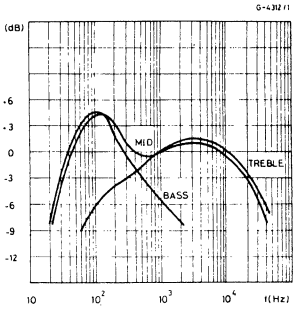


Fig. 25 - 20W Bus amplifier

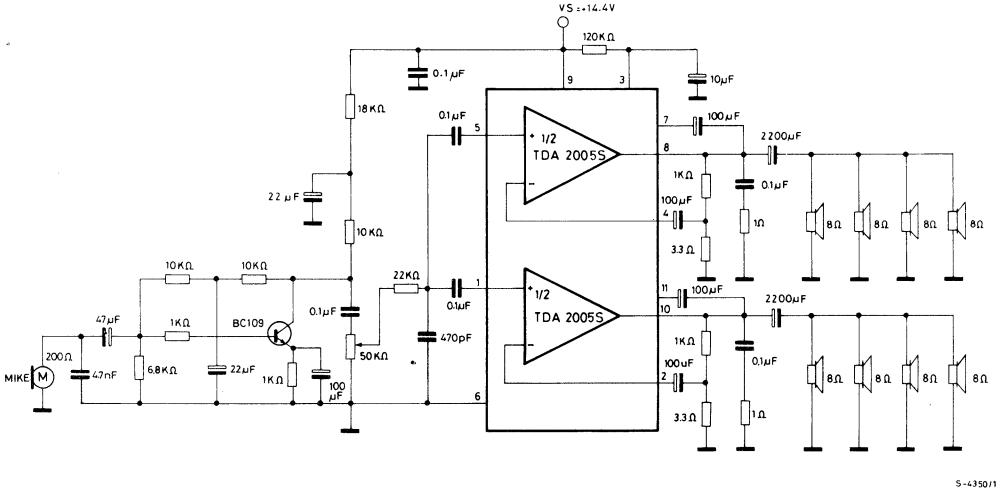


Fig. 26 - Simple 20W two way amplifier (f_c = 2 KHz)

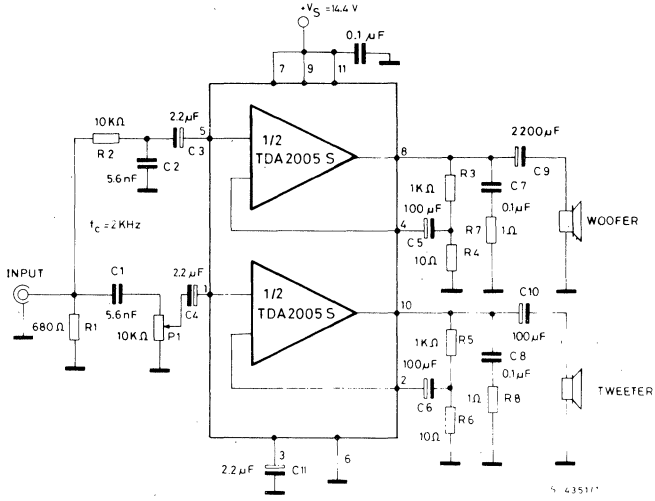
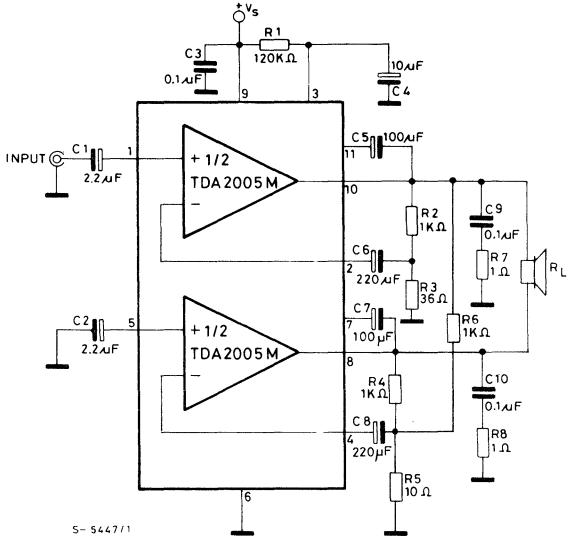


Fig. 27 - Bridge amplifier circuit suited for low-gain applications (G_v = 34 dB)



APPLICATION SUGGESTION

The recommended values of the components are those shown on Bridge application circuit of fig. 1. Different values can be used, the following table can help the designer.

Component	Recommended Value	Purpose	Larger than	Smaller than
R_1	120 KΩ	Optimization of the output symmetry	Smaller P_o max	Smaller P_o max
R_2	1 KΩ	Closed loop gain setting (see BRIDGE AMPLIFIER DESIGN)		
R_3	2 KΩ			
R_4 and R_5	12 Ω			
R_6 and R_7	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive loads	
C_1	2.2 μF	Input DC decoupling	High turn on delay	Higher turn on pop. Higher low frequency cutoff. Increase of noise.
C_2	2.2 μF	Optimization of turn on pop and turn on delay.		
C_3	0.1 μF	Supply by pass		Danger of oscillation.
C_4	10 μF	Ripple Rejection	Increase of SVR. Increase of the switch-on time.	Degradation of SVR.
C_5 and C_7	100 μF	Bootstrapping		Increase of distortion at low frequency.
C_6 and C_8	220 μF	Feedback input DC decoupling, low frequency cutoff.		Higher low frequency cutoff.
C_9 and C_{10}	0.1 μF	Frequency stability.		Danger of oscillation.

BUILT-IN PROTECTION SYSTEMS

Load dump voltage surge

The TDA 2005 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in fig. 29.

If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.

A suggested LC network is shown in fig. 28. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 28

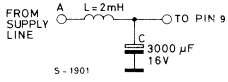
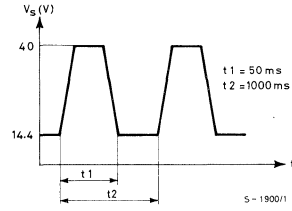


Fig. 29



Short circuit (AC and DC conditions)

The TDA 2005 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2005 protection diodes are included to avoid any damage.

Inductive load

A protection diode is provided to allow use of the TDA 2005 with inductive loads.

DC voltage

The maximum operating DC voltage for the TDA 2005 is 18V.

However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 30 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 30 - Maximum allowable power dissipation vs. ambient temperature

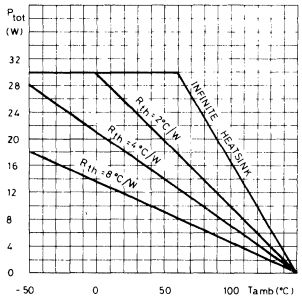


Fig. 31 - Output power and drain current vs. case temperature

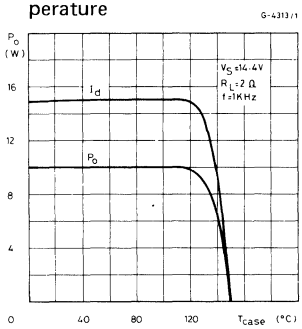
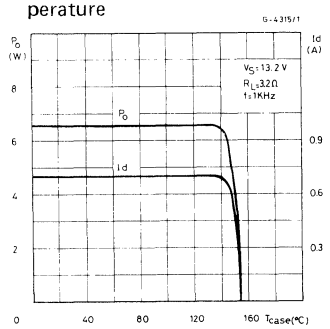


Fig. 32 - Output power and drain current vs. case temperature



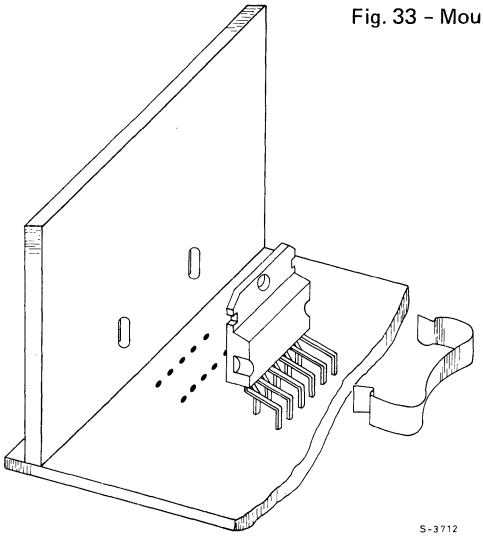
Loudspeaker protection

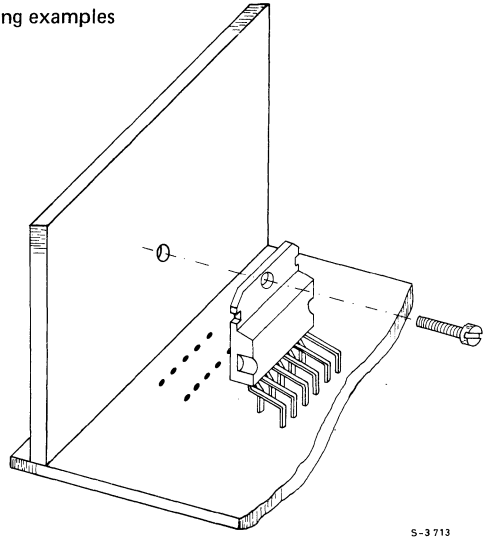
The circuit offers loudspeaker protection during short circuit for one wire to ground.

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 33 - Mounting examples





TDA2006

LINEAR INTEGRATED CIRCUIT

10W AUDIO AMPLIFIER

The TDA 2006 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class "AB" amplifier. At ± 12V, d = 10% typically it provides 12W output power on a 4Ω load and 8W on a 8Ω. The TDA 2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA 2006 is pin to pin equivalent to the TDA 2030.

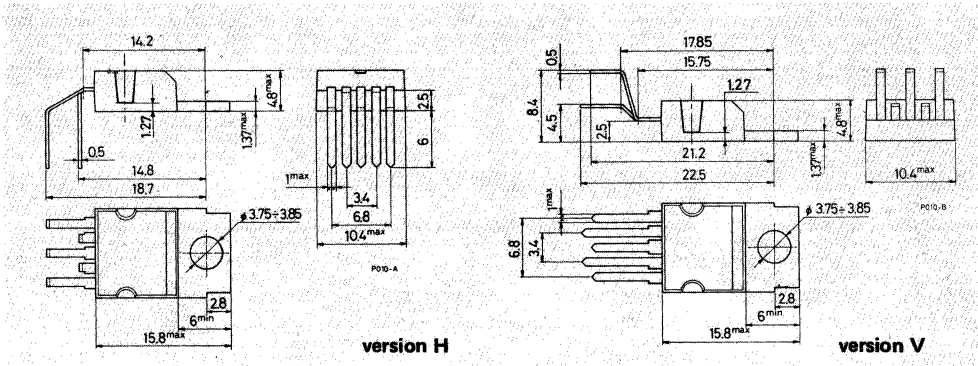
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 15	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 12	V
I_o	Output peak current (internally limited)	3	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

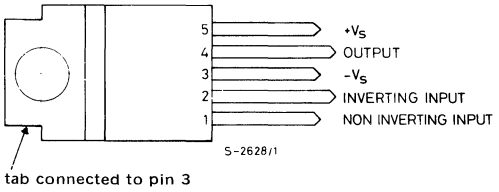
ORDERING NUMBERS: TDA 2006H; TDA 2006V

MECHANICAL DATA

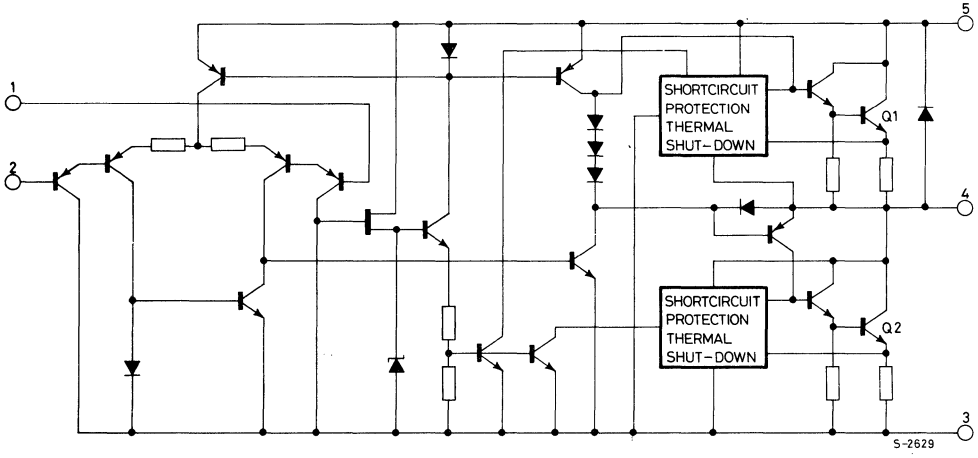
Dimensions in mm



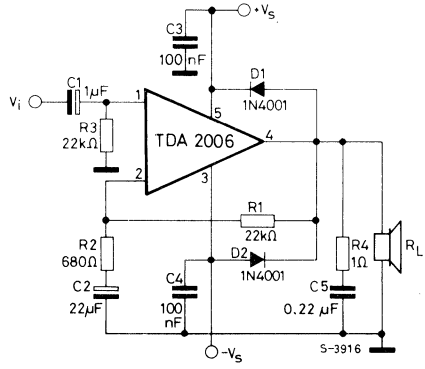
CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



TEST AND APPLICATION CIRCUIT



THERMAL DATA

$R_{th\text{-}j\ case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s= ±12V, T_{amb}= 25°C unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 15	V
I_d	Quiescent drain current	V_s = ± 15V		40	80	mA
I_b	Input bias current			0.2	3	μA
V_{OS}	Input offset voltage			± 8		mV
I_{OS}	Input offset current			± 80		nA
V_{OS}	Output offset voltage			± 10	± 100	mV
P_o	Output power	d = 10% f = 1 KHz R_L= 4Ω R_L= 8Ω	 6	 12 8		 W W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Units
d	Distortion	P_o= 0.1 to 8W R_L= 4Ω f = 1 KHz		0.2		%
		P_o= 0.1 to 4W R_L= 8Ω f = 1 KHz		0.1	1	%
V_i	Input sensitivity	f = 1 KHz P_o= 10W R_L= 4Ω P_o= 6W R_L= 8Ω		200 220		mV mV
B	Frequency response (-3 dB)	P_o= 8W R_L= 4Ω	10 to 140,000			Hz
R_i	Input resistance (pin 1)	f = 1 KHz	0.5	5		MΩ
G_v	Voltage gain (open loop)			75		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB
e_N	Input noise voltage	B (-3 dB) = 22Hz to 22kHz R_L= 4Ω		3	10	μV
i_N	Input noise current			80	200	pA
SVR	Supply voltage rejection	R_L= 4Ω R_g= 22 KΩ f_{ripple}= 100 Hz (*)	40	50		dB
I_d	Drain current	P_o= 12W R_L= 4Ω P_o= 8W R_L= 8Ω		850 500		mA mA
T_j	Thermal shut down junction temperature			145		°C

(*) Referring to fig. 15, single supply.

Fig. 1 - Output power vs. supply voltage

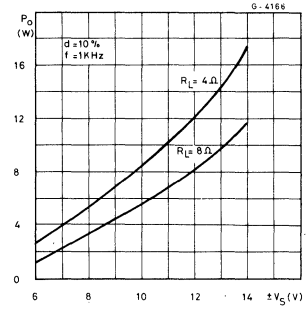


Fig. 2 - Distortion vs. output power

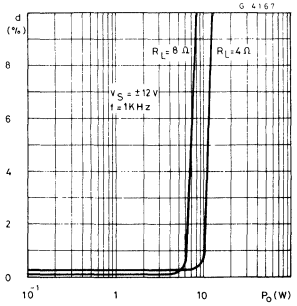


Fig. 3 - Distortion vs. frequency

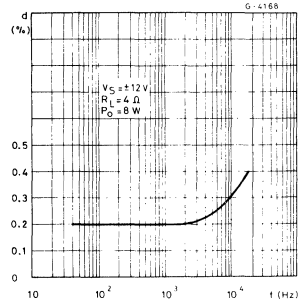


Fig. 4 - Distortion vs. frequency

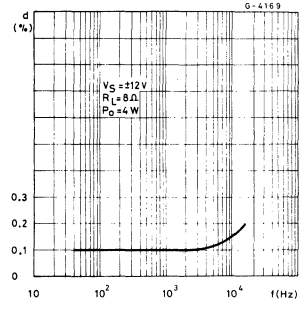


Fig. 5 - Sensitivity vs. output power

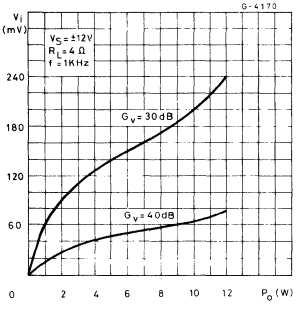


Fig. 6 - Sensitivity vs. output power

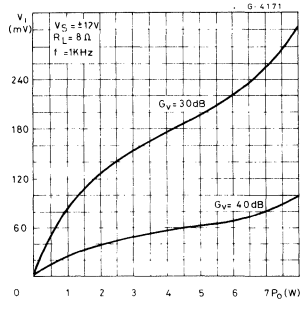


Fig. 7 - Frequency response with different values of the rolloff capacitor C_8 (see fig. 13)

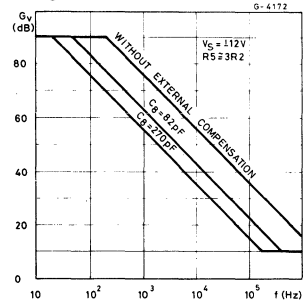


Fig. 8 - Value of C_8 vs. voltage gain for different bandwidths (see fig. 13)

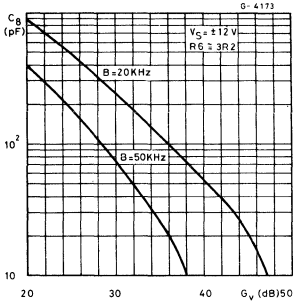


Fig. 9 - Quiescent current vs. supply voltage

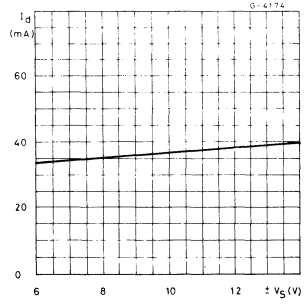


Fig. 10 - Supply voltage rejection vs. voltage gain

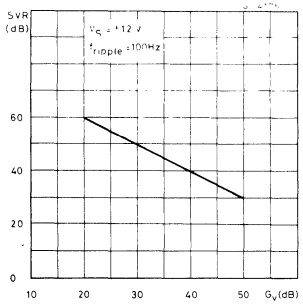


Fig. 11 - Power dissipation and efficiency vs. output power

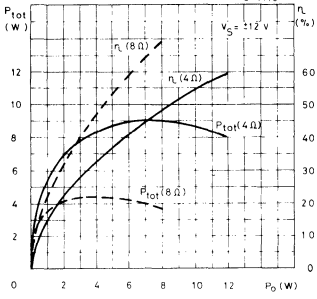


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)

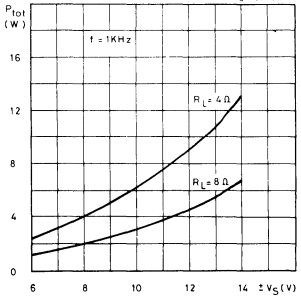


Fig. 13 - Application circuit with split power supply

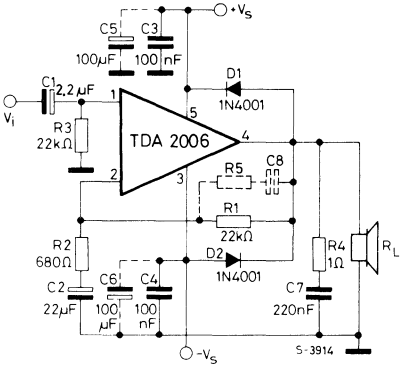


Fig. 14 - P.C. board and component layout for the circuit of fig. 13

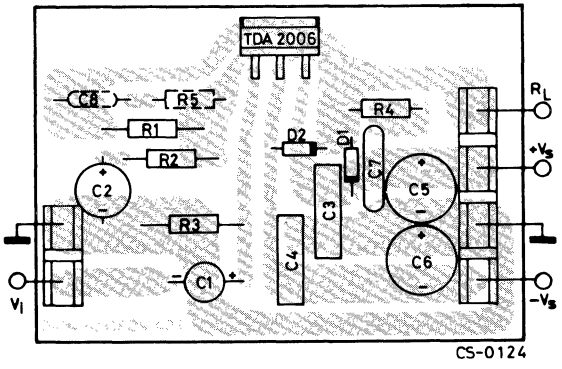


Fig. 15 - Application circuit with single power supply

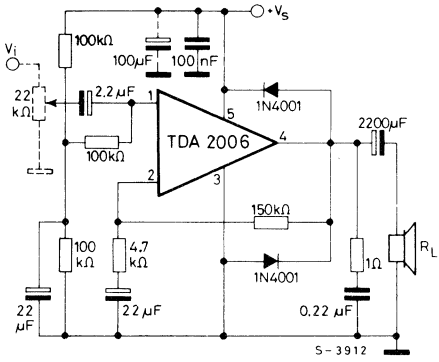


Fig. 16 - P.C. board and component layout for the circuit of fig. 15

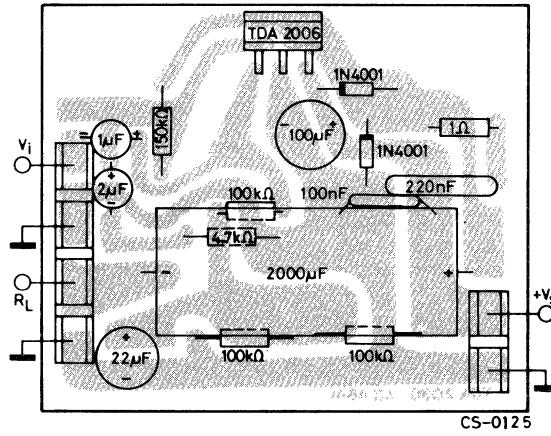
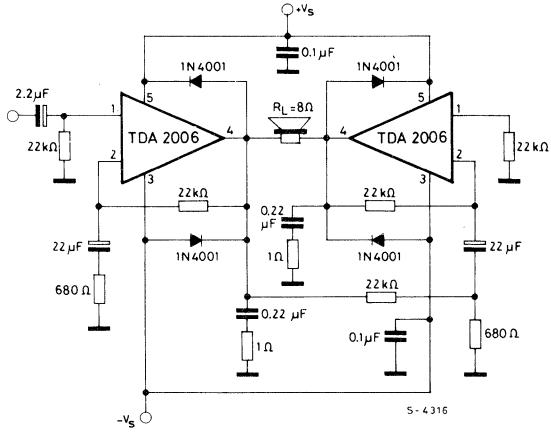


Fig. 17 - Bridge amplifier configuration with split power supply (Po = 24W, $V_s = \pm 12V$)



PRACTICAL CONSIDERATION

Printed circuit board

The layout shown in fig. 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

Application suggestion

The recommended values of the components are the ones shown on application circuits of fig. 13. Different values can be used. The following table can help the designers.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R_1	22 KΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R_2	680Ω	Closed loop gain setting	Decrease of gain	Increase pf gain
R_3	22 KΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R_4	1Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_5	$3\,R_2$	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C_1	2.2 μF	Input DC decoupling		Increase of low freqencies cut off
C_2	22 μF	Inverting input DC decoupling		Increase of low frequencies cutoff
C_3C_4	0.1 μF	Supply voltage by pass		Danger of oscillation
C_5C_6	100 μF	Supply voltage by pass		Danger of oscillation
C_7	0.22 μF	Frequency stability		Danger of oscillation
C_8	$\frac{1}{2\pi BR_1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
D_1D_2	1N4001	To protect the device against output voltage spikes.		

SHORT CIRCUIT PROTECTION

The TDA 2006 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (fig. 19).
This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2006 is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shutdown protection keeps the junction temperature within safe limits.

Fig. 18 - Maximum output current vs. voltage $V_{Ce(sat)}$ across each output transistor

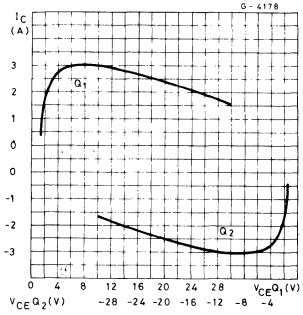
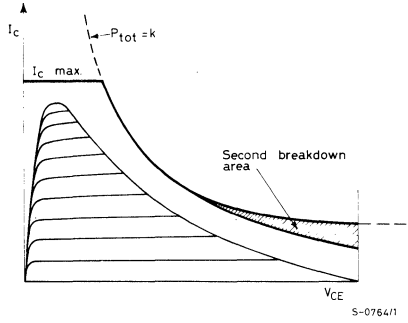


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

   If for any reason, the junction temperature increases up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

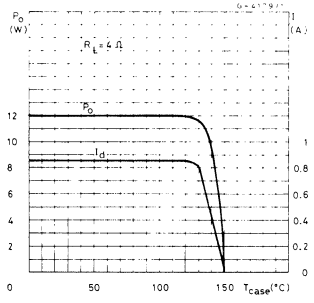
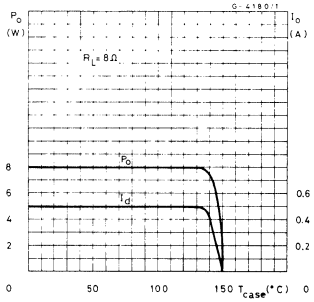


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistances.

Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

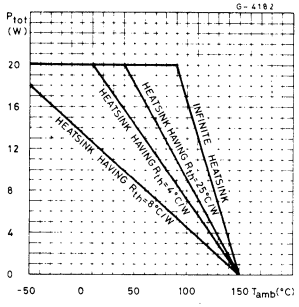
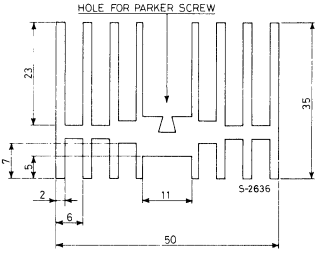


Fig. 23 - Example of heatsink



Dimension suggestion

The following table shows the lenght of the heatsink in fig. 23 for several values of P_{tot} and R_{th}.

P_{tot} (W)	12	8	6
Lenght of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

TDA2008

LINEAR INTEGRATED CIRCUIT

12W AUDIO AMPLIFIER (V_s = 22V, R_L = 4Ω)

The TDA 2008 is a monolithic class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 3.2Ω). The device provides a high output current capability (up to 3A), very low harmonic and crossover distortion.
In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use
- thermal protection

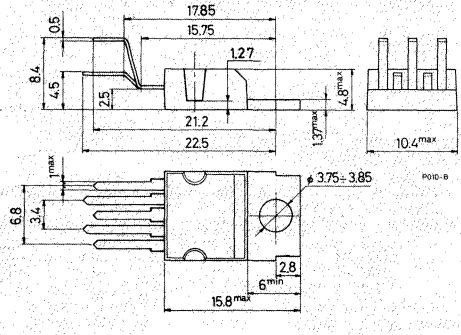
ABSOLUTE MAXIMUM RATINGS

V_s	DC supply voltage	28	V
I_o	Output peak current (repetitive)	3	A
I_o	Output peak current (non repetitive)	4	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

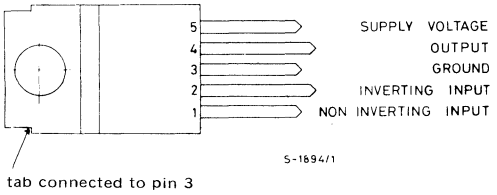
ORDERING NUMBERS: TDA 2008V

MECHANICAL DATA

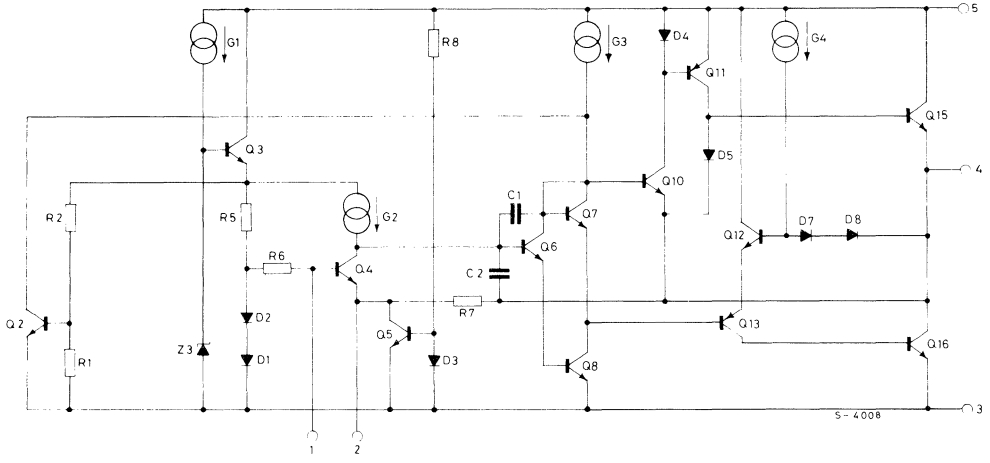
Dimensions in mm



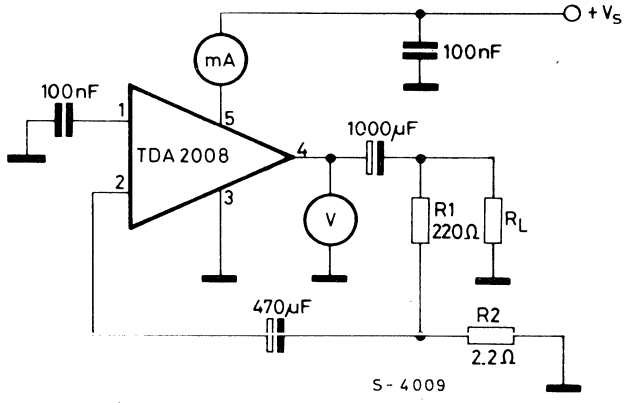
CONNECTION DIAGRAM (top view)



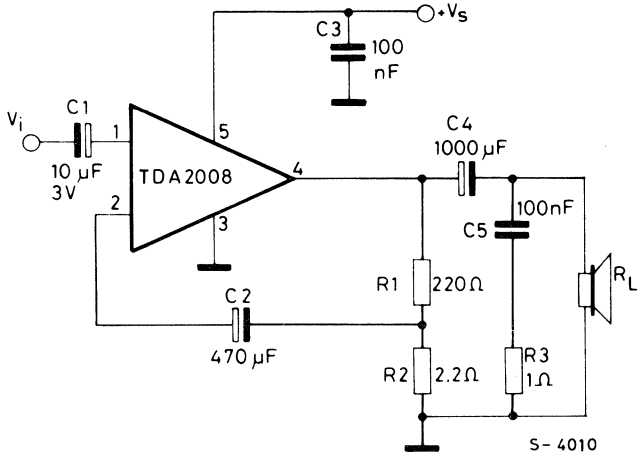
SCHEMATIC DIAGRAM



DC TEST CIRCUIT



AC TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 22V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			10		28	V
V_o	Quiescent output voltage (pin 4)				10.5		V
I_d	Quiescent drain current (pin 5)				65	115	mA
P_o	Output power	d = 10%	R_L = 8Ω		8		W
		f = 1 KHz	R_L = 4Ω	10	12		W
V_i (RMS)	Input saturation voltage			300			mV
V_i	Input sensitivity	f = 1 KHz P_o = 0.5W P_o = 8W P_o = 0.5W P_o = 12W	 R_L = 8Ω R_L = 8Ω R_L = 4Ω R_L = 4Ω		 20 80 14 70		 mV mV mV mV
B	Frequency response (-3 dB)	P_o = 1W R_L = 4Ω		40 to 15 000			Hz
d	Distortion	f = 1 KHz P_o = 0.05 to 4W P_o = 0.05 to 6W	 R_L = 8Ω R_L = 4Ω		 0.15 0.15		 % %
R_i	Input resistance (pin 1)	f = 1 KHz		70	150		KΩ
G_v	Voltage gain (open loop)	f = 1 KHz	R_L = 8Ω		80		dB
G_v	Voltage gain (closed loop)			39.5	40	40.5	dB
e_N	Input noise voltage	BW= 22Hz to 22 KHz			1	5	μV
i_N	Input noise current				60	200	pA
SVR	Supply voltage rejection	V_{ripple} = 0.5V R_g = 10KΩ R_L = 4Ω	f = 100 Hz	30	36		dB
			f = 15 KHz		36		dB

APPLICATION INFORMATION

Fig. 1 - Typical application circuit

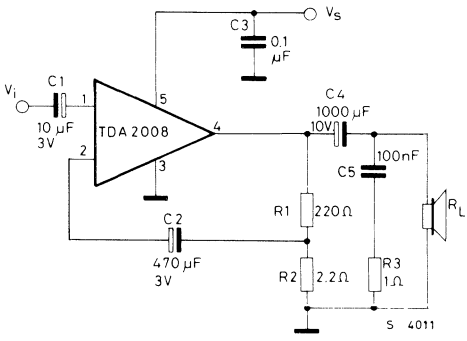


Fig. 2 - P.C. board and component layout for the circuit of fig. 1 (1:1 scale)

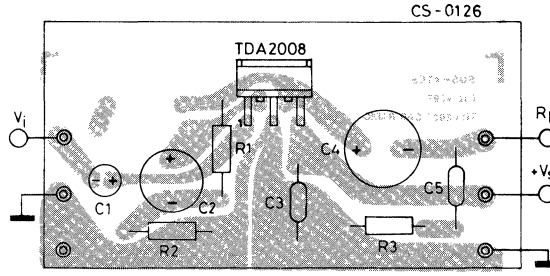


Fig. 3 - 25W bridge configuration application circuit (°)

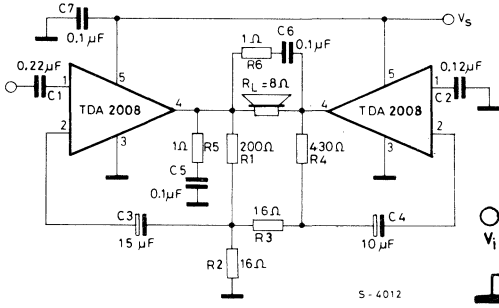
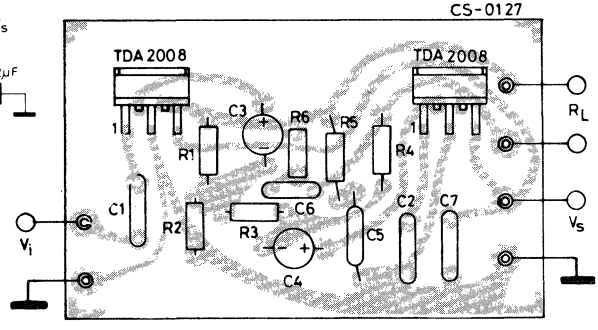
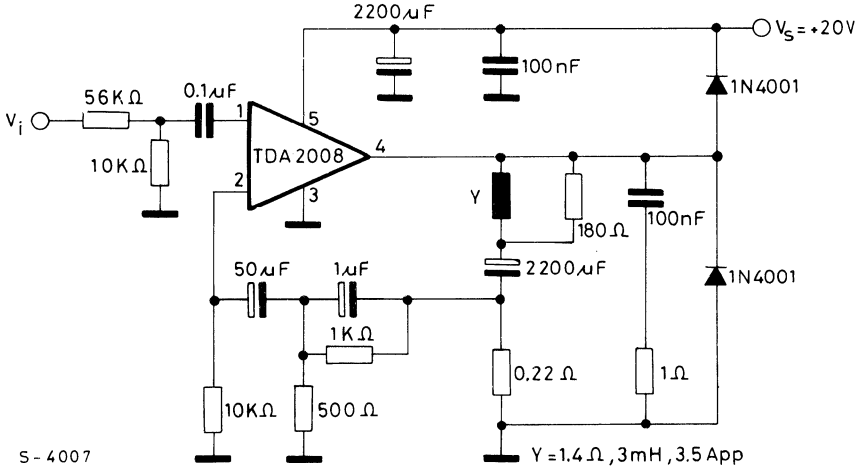


Fig. 4 - P.C. board and component layout for the circuit of fig. 3 (1:1 scale)



(°) The value of the capacitors C3 and C4 are different to optimize the SVR (Typ. = 40 dB)

Fig. 5 - Vertical deflection for count-down circuits



TDA2009

LINEAR INTEGRATED CIRCUIT

10 + 10W HIGH QUALITY STEREO AMPLIFIER

The TDA 2009 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo applications as Hi-Fi TV and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 0.5%)
- High current capability (up to 3.5A)
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.

ADVANCE DATA

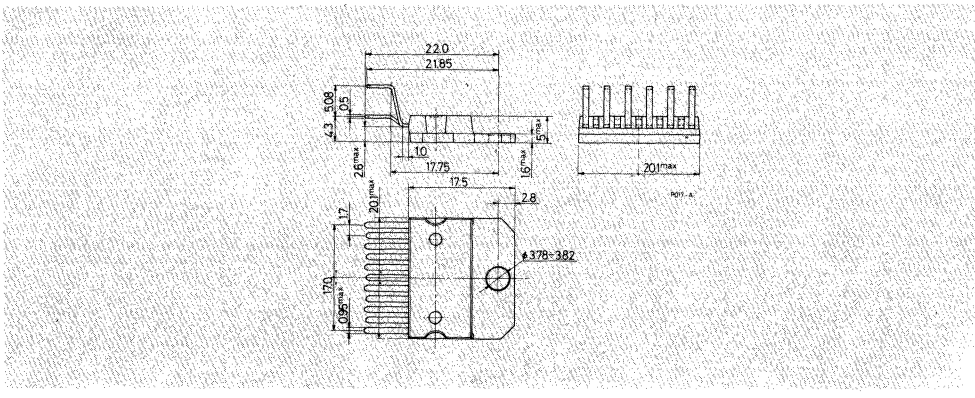
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
I_o	Output peak current (repetitive f ⩾ 20 Hz)	3.5	A
I_o	Output peak current (non repetitive, t = 100 μs)	4.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

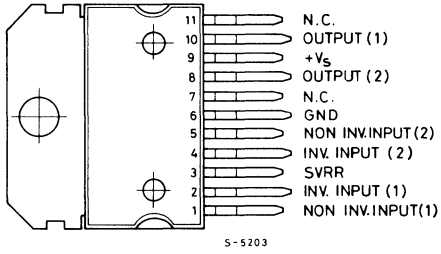
ORDERING NUMBER: TDA 2009

MECHANICAL DATA

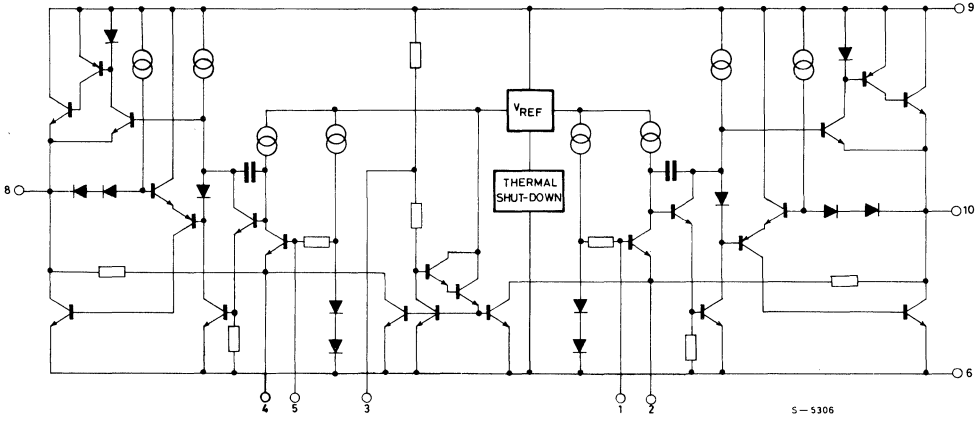
Dimensions in mm



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

Fig. 1 - Test circuit (G_v = 36 dB)

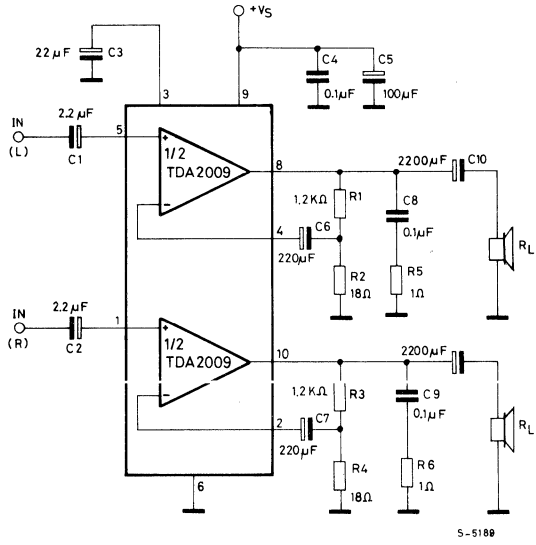
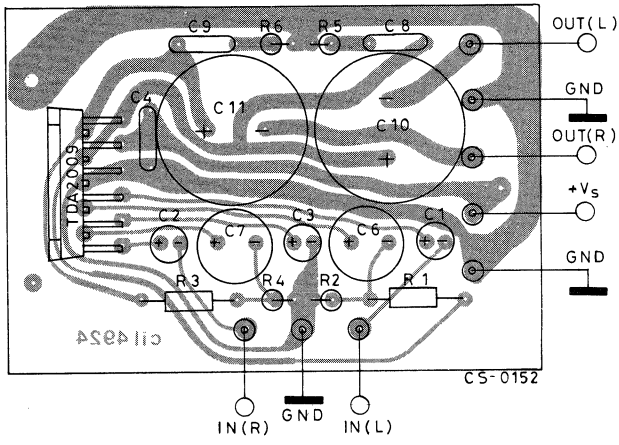


Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (Refer to the **stereo** application circuit, T_{amb}= 25°C, G_v = 36 dB, unless otherwise specified)

Parameters		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		8		28	V
V_o	Quiescent output voltage	V_s = 23V		11		V
I_d	Total quiescent drain current	V_s = 23V		80	120	mA
P_o	Output power (each channel)	f = 40 Hz to 16 KHz d = 0.5% V_s = 23V R_L= 4 Ω R_L= 8 Ω V_s = 18V R_L= 4 Ω R_L= 8 Ω	 10 5.5	 12 7 7 4		 W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 23V R_L= 4 Ω P_o= 100 mW to 8W V_s = 23V R_L= 8 Ω P_o= 100 mW to 3W		 0.1 0.05		 %
CT	Cross talk (°°°)	R_L = ∞ f = 1 KHz		60		dB
		R_g = 10 KΩ f = 10 KHz		50		dB
V_i	Input saturation voltage (rms)		300			mV
R_i	Input resistance	f = 1 KHz non inverting input	70	200		KΩ
		inverting input		10		KΩ
f_L	Low frequency roll off (-3 dB)	R_L = 4Ω		15		Hz
f_H	High frequency roll off (-3 dB)			80		KHz
G_v	Voltage gain (open loop)	f = 1 KHz		85		dB
G_v	Voltage gain (closed loop)	f = 1 KHz	35.5	36	36.5	dB
ΔG_v	Closed loop gain matching			0.5		dB
e_N	Total input noise voltage	R_g = 10 KΩ (°)		1.5		μV
		R_g = 10 KΩ (°°)		2		μV
SVR	Supply voltage rejection (each channel)	R_g = 10 KΩ f_{ripple}= 100 Hz V_{ripple}= 0.5V		55		dB
T_J	Thermal shut-down junction temperature			145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Fig. 3 - Output power vs. supply voltage

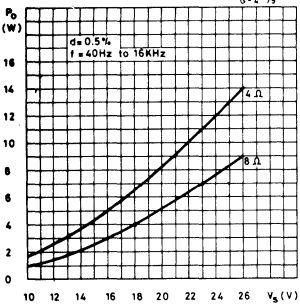


Fig. 4 - Output power vs. supply voltage

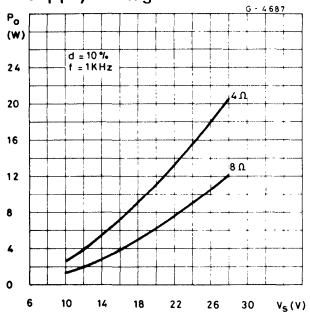


Fig. 5 - Distortion vs. output power

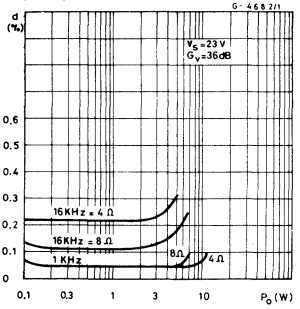


Fig. 6 - Distortion vs. frequency

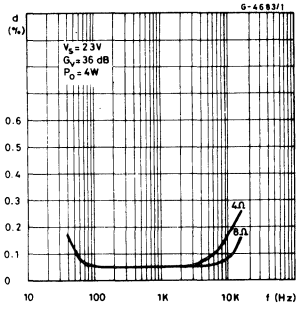


Fig. 7 - Quiescent current vs. supply voltage

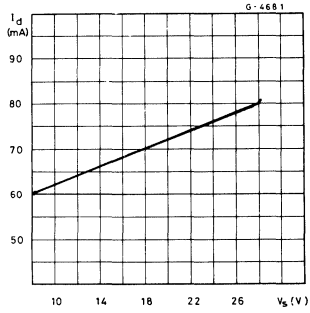


Fig. 8 Supply voltage rejection vs. value of capacitor C3

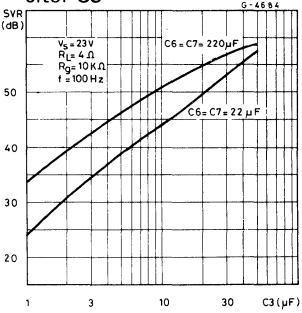


Fig. 9 - Supply voltage rejection vs. frequency

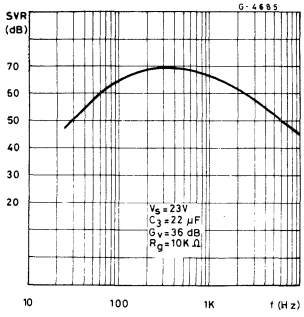


Fig. 10 - Total power dissipation an efficiency vs. output power

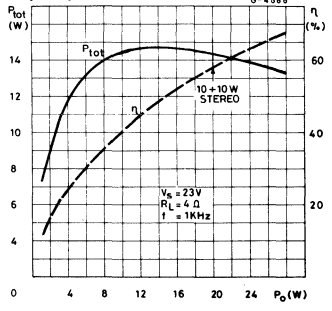
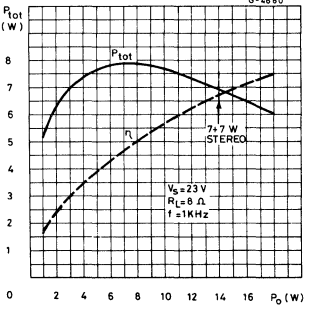


Fig. 11 - Total power dissipation and efficiency vs. output power



APPLICATION INFORMATION

Fig. 12 - Typical application circuit

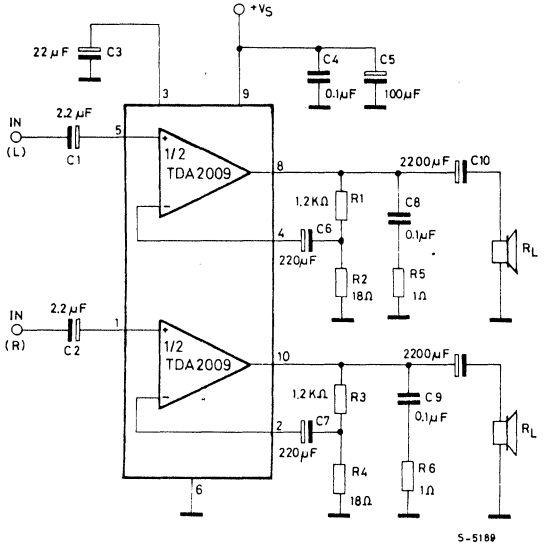


Fig. 13 - 10 + 10W stereo amplifier with tone balance and loudness control

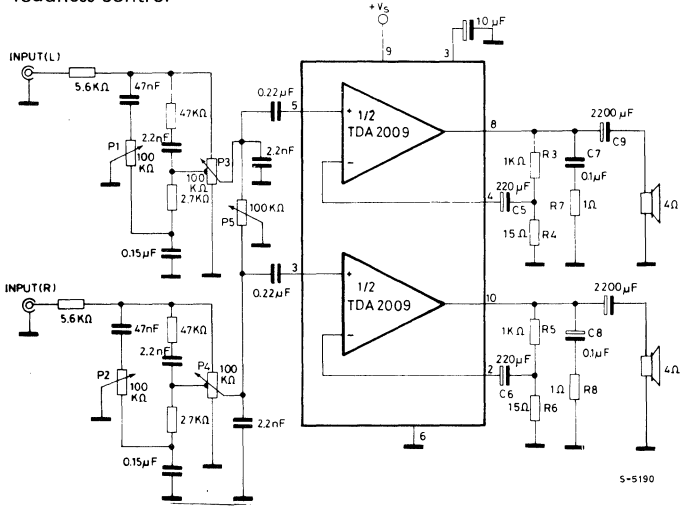
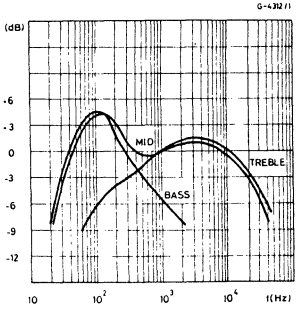


Fig. 14 - Tone control response (circuit of fig. 13)



APPLICATION INFORMATION (continued)

Fig. 15 - 10 + 10W high quality cassette player

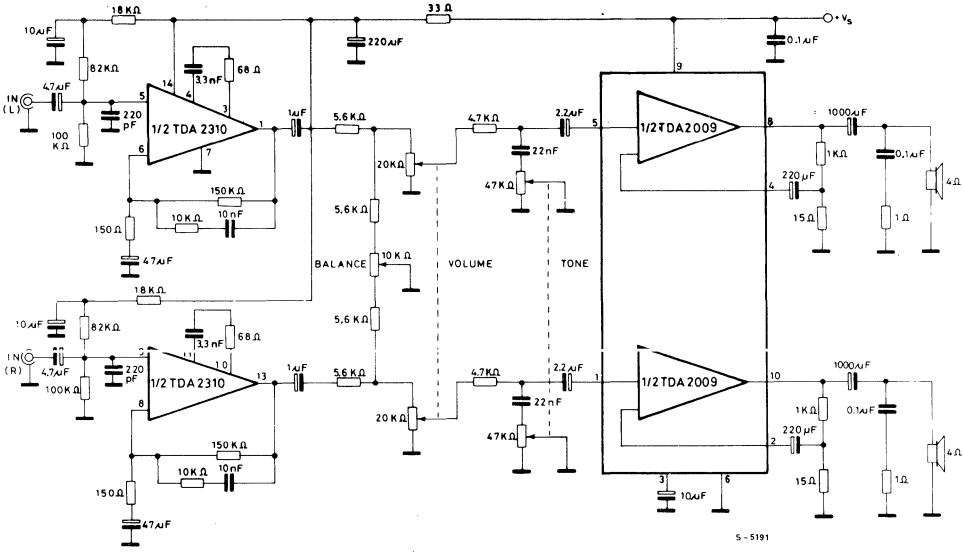
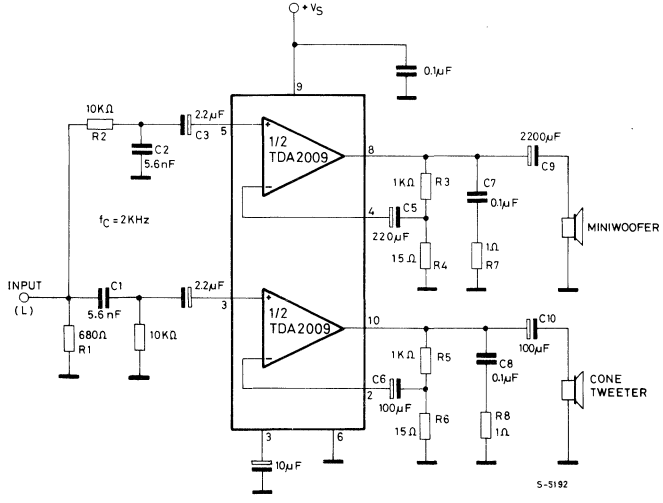
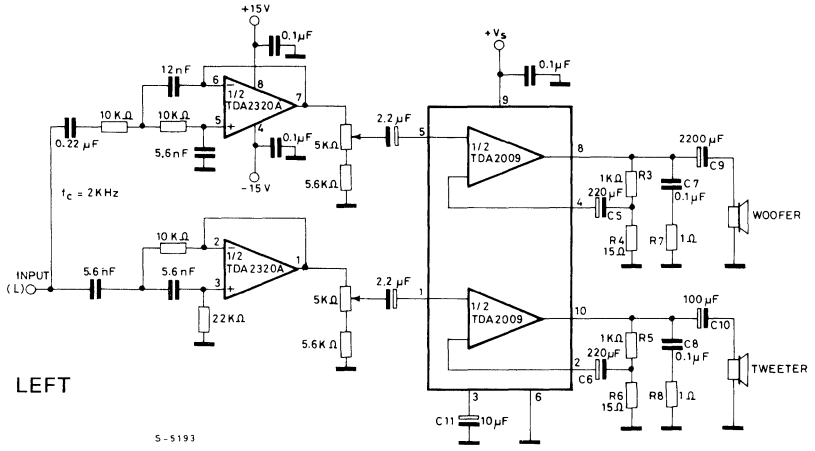


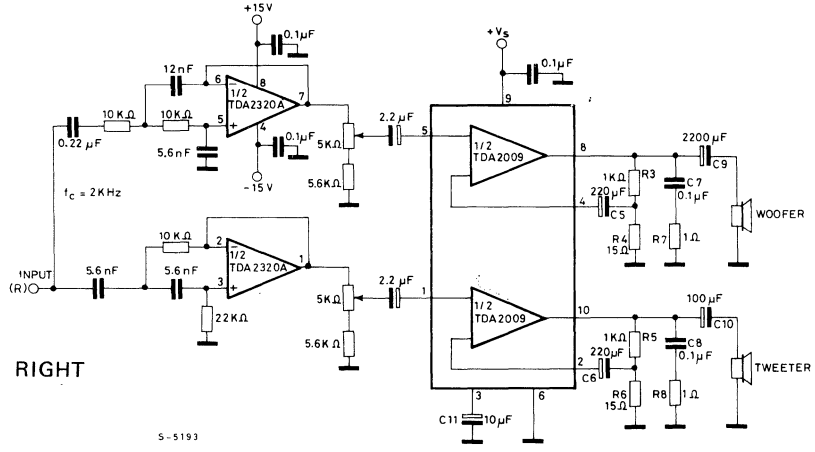
Fig. 16 - 20W Hi-Fi TV two way amplifier (f_c = 2 KHz)



APPLICATION INFORMATION (continued)

Fig. 17 - High quality 20 + 20W two way amplifier for stereo music center





APPLICATION INFORMATION (continued)

Fig. 18 - 18W bridge amplifier (d = 0.5%, G_v = 42 dB)

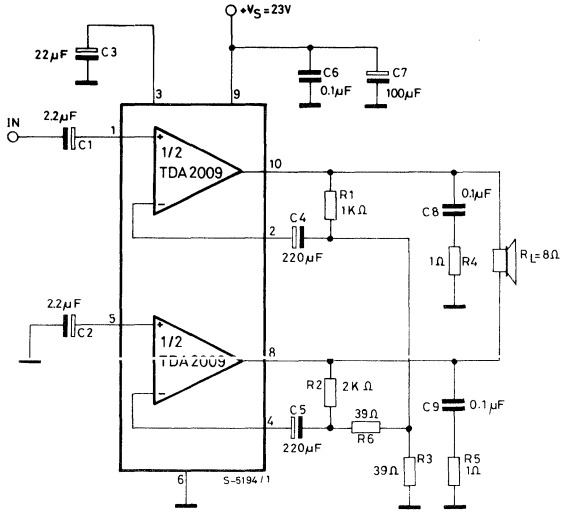
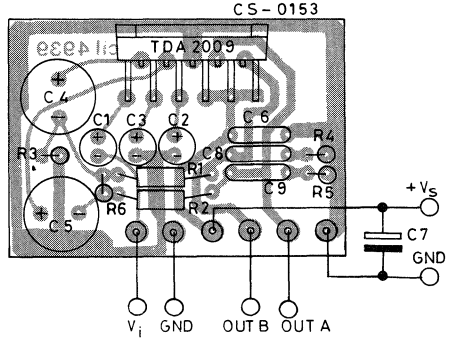


Fig. 19 - P.C. board and components layout of the circuit of fig. 18 (1 : 1 scale)



APPLICATION SUGGESTION

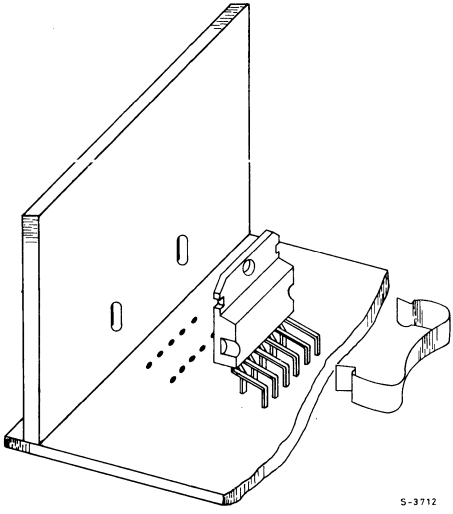
The recommended values of the components are those shown on application circuit of fig. 12. Different values can be used; the following table can help the designer.

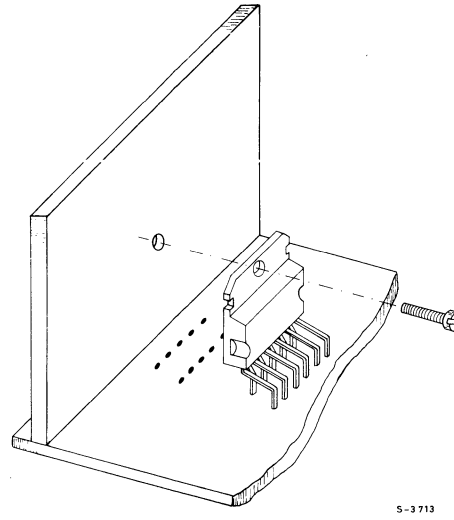
Component	Recomm. value	Purpose	Larger than	Smaller than
R1 and R3	1.2 KΩ	Close loop gain setting	Increase of gain	Decrease of gain
R2 and R4	18 Ω		Decrease of gain	Increase of gain
R5 and R6	1 Ω	Frequency stability	Danger of oscillation at high frequency with inductive load	
C1 and C2	2.2 μF	Input DC decoupling	High turn-on delay	High turn-on pop Higher low frequency cutoff. Increase of noise
C3	22 μF	Ripple rejection	Better SVR. Increase of the switch-on time	Degradation of SVR.
C6 and C7	220 μF	Feedback Input DC decoupling.		
C8 and C9	0.1 μF	Frequency stability.		Danger of oscillation.
C10 and C11	1000 μF to 2200 μF	Output DC decoupling.		Higher low-frequency cut-off.

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 20 - Mounting examples





LINEAR INTEGRATED CIRCUIT

TDA2010

12W Hi-Fi AUDIO AMPLIFIER

The TDA 2010 is a monolithic integrated operational amplifier in a 14-lead quad in-line plastic package, inteded for use as a low frequency class B power amplifier. Typically it provides 12W output power (d = 1%) at ± 14V/4Ω; at V_s = ± 14V the guaranteed output power is 10W on a 4Ω load and 8W on a 8Ω load (DIN norm 45500). The TDA 2010 provides high output current (up to 3.5 A) and has very low harmonic and cross-over distortion. Further, the device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep to working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included. The TDA 2010 is pin to pin equivalent to TDA 2020.

ABSOLUTE MAXIMUM RATINGS

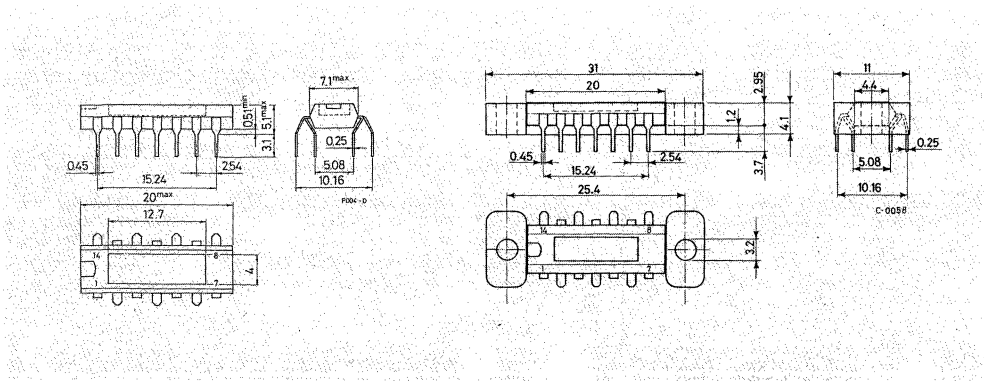
V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at $T_{case} \leqslant 95°C$	18	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMERS:

TDA 2010 B82	dual in-line plastic package
TDA 2010 B92	quad in-line plastic package
TDA 2010 BC2	dual in-line plastic package with spacer
TDA 2010 BD2	quad in-line plastic package with spacer

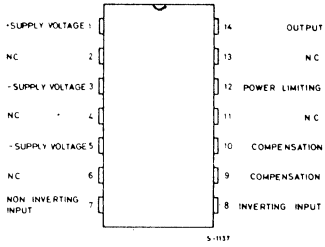
MECHANICAL DATA

Dimensions in mm

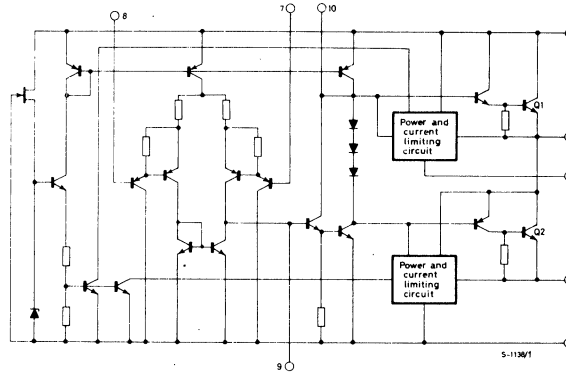


CONNECTION AND SCHEMATIC DIAGRAMS

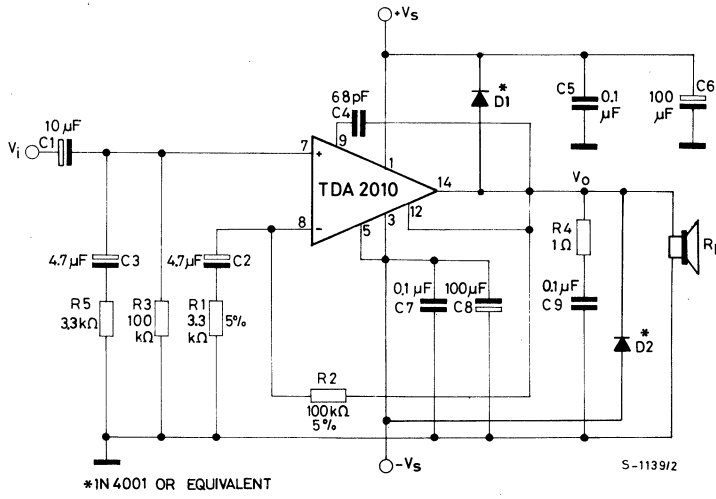
(top view)



The copper slug is electrically connected to pin 5 (substrate)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 5		± 18	V
I_d	Quiescent drain current	$V_s = \pm 18V$		45		mA
I_b	Input bias current	$V_s = \pm 17V$		0.15		μA
V_{os}	Input offset voltage			5		mV
I_{os}	Input offset current			0.05		μA
V_{os}	Output offset voltage			10	100	mV
P_o	Output power	d = 1% $T_{case} \leq 70°C$ f = 40 to 15 000 Hz $R_L = 4\ \Omega$ $R_L = 8\ \Omega$	10 8	12 9		W W
		d = 10% $T_{case} \leq 70°C$ f = 1 kHz $R_L = 4\ \Omega$ $R_L = 8\ \Omega$		15 12		W W
V_i	Input sensitivity	f = 1 kHz $P_o = 10$ W $R_L = 4\ \Omega$ $P_o = 8$ W $R_L = 8\ \Omega$		220 250		mV mV
B	Frequency response (-3dB)	$R_L = 4\ \Omega$ C4 = 68 pF	10 to 160 000			Hz
d	Distortion	P_o = 100 mW to 10 W $R_L = 4\ \Omega$ $T_{case} \leq 70°C$ f = 1 kHz f = 40 to 15 000 Hz		0.1 0.3	 1	 %
		P_o = 100 mW to 8 W $R_L = 8\ \Omega$ $T_{case} \leq 70°C$ f = 1 kHz f = 40 to 15 000 Hz		0.1 0.2	 1	 %
R_i	Input resistance (pin 7)			5		MΩ
G_v	Voltage gain (open loop)	$R_L = 4\ \Omega$ f = 1 kHz		100		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB
e_N	Input noise voltage	$R_L = 4\ \Omega$		4		μV
i_N	Input noise current	B (-3 dB) = 22 Hz to 22 KHz		0.1		nA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	R_L = 4 Ω f_{ripple} = 100 Hz		50		dB
I_d	Drain current	P_o = 12 W R_L = 4 Ω P_o = 9 W R_L = 8 Ω		0.8 0.5		A A
T_{sd}	Thermal shut-down junction temperature			145		°C
T_{sd}	(*) Thermal shut-down case temperature	P_{tot} = 10.5 W		120		°C

(*) See fig. 14.

Fig. 1 - Output power vs. supply voltage

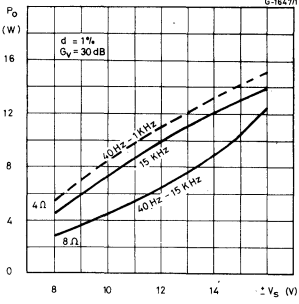


Fig. 2 - Output power vs. supply voltage

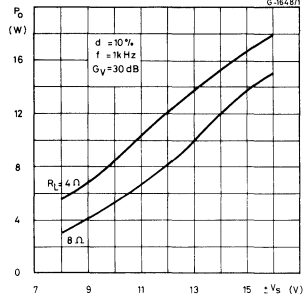


Fig. 3 - Distortion vs. output power

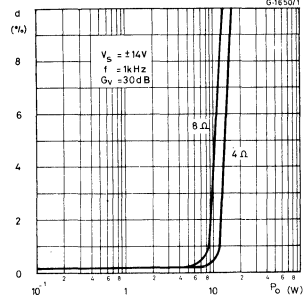


Fig. 4 - Distortion vs. output power (R_L = 4 Ω)

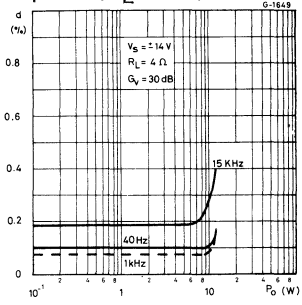


Fig. 5 - Distortion vs. output power (R_L = 8 Ω)

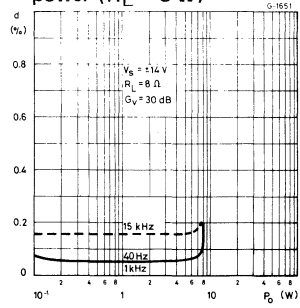


Fig. 6 - Distortion vs. frequency

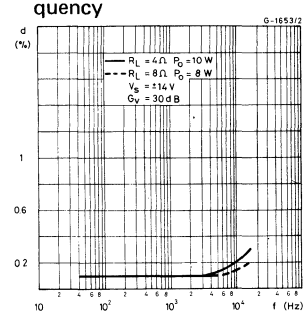


Fig. 7 - Output power vs. frequency

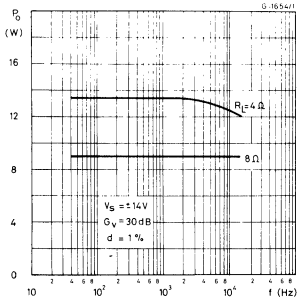


Fig. 8 - Sensitivity vs. output power (R_L = 4 Ω)

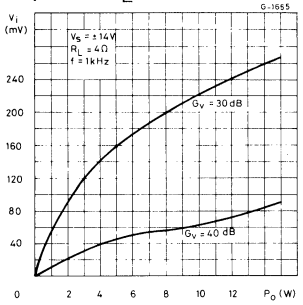


Fig. 9 - Sensitivity vs. output power (R_L = 8 Ω)

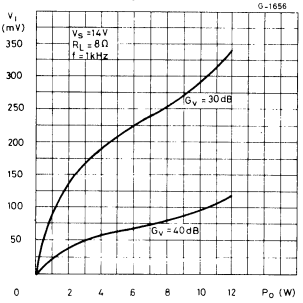


Fig. 10 - Open loop frequency response with different values of the rolloff capacitor C4

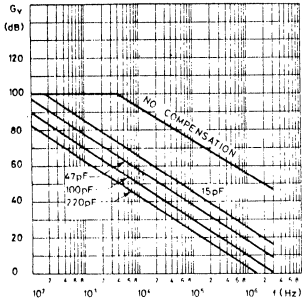


Fig. 11 - Value of C4 vs. voltage gain for different bandwidths

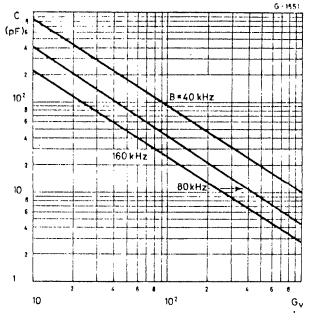


Fig. 12 - Quiescent current vs. supply voltage

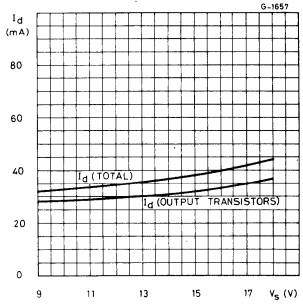


Fig. 13 - Supply voltage rejection vs. voltage gain

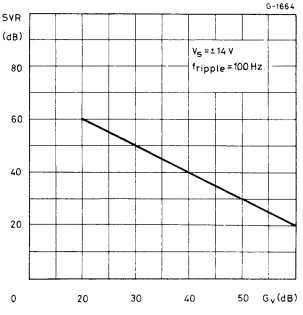


Fig. 14 - Power dissipation and efficiency vs. output power

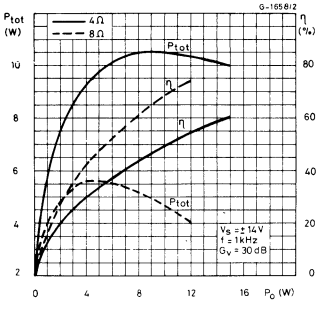
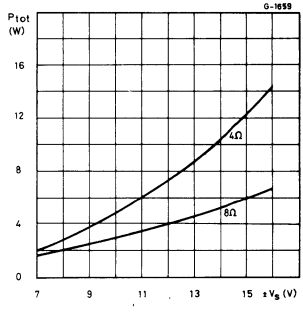


Fig. 15 - Maximum power dissipation vs. supply voltage (sine wave operation)



APPLICATION INFORMATION

Fig. 16 - Application circuit with split power supply

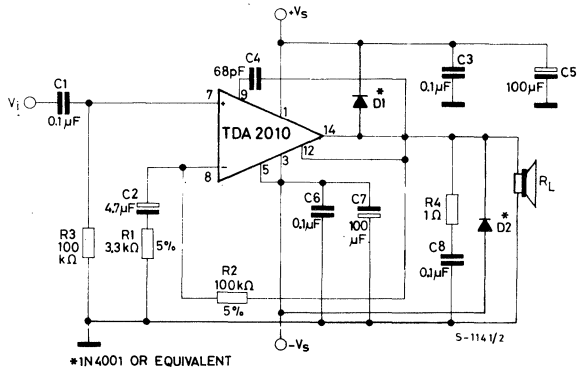
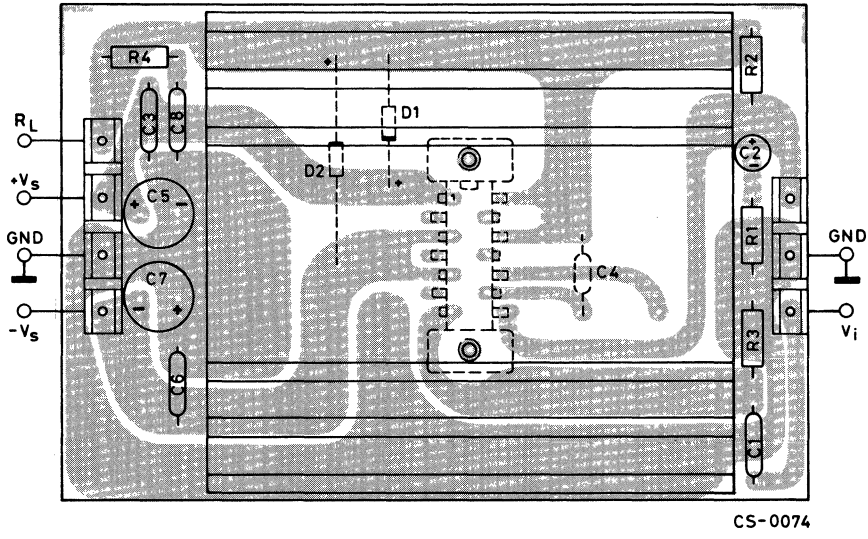


Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)



SHORT CIRCUIT PROTECTION

The most important innovation in the TDA 2010 is an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector-emitter voltage; hence the output transistors work within their safe operating area (fig. 19). This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2010 is thus protected against temporary overloads or short circuit. Should the short circuit exists for a longer time, the thermal shut-down comes into action and keeps the junction temperature within safe limits.

Fig. 18 - Maximum output current vs. voltave (V_{CE}) across each output transistor

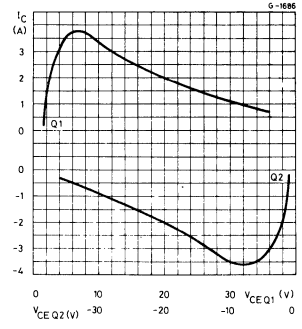
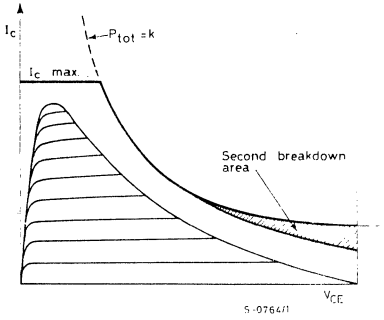


Fig. 19 - Safe operating area and collector characteristics of the protected power transistor.



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If, for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 8\ \Omega$)

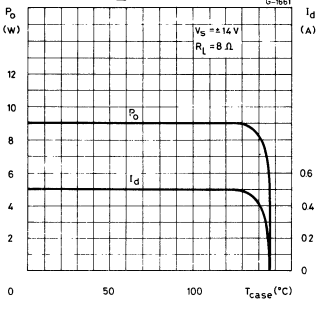
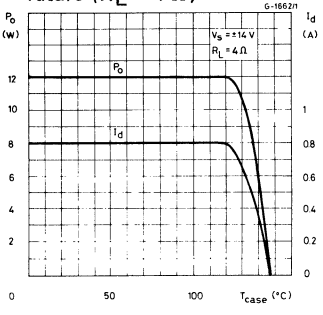


Fig. 21 - Output power and drain current vs. case temperature ($R_L = 4\ \Omega$)



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink as shown in figs. 22 and 23.
The system for attaching the heatsink is very simple: it uses a plastic spacer which is supplied with the device.
Thermal contact between the copper slug (of the package) and the heatsink is guaranteed by the pressure which the screws exert via the spacer and the printed circuit board; this is due to the particular shape of the spacer.

Note: The most negative supply voltage is connected to the copper slug, hence to the heatsink (because it is in contact with the slug).

Fig. 22 - Mounting system of TDA 2010

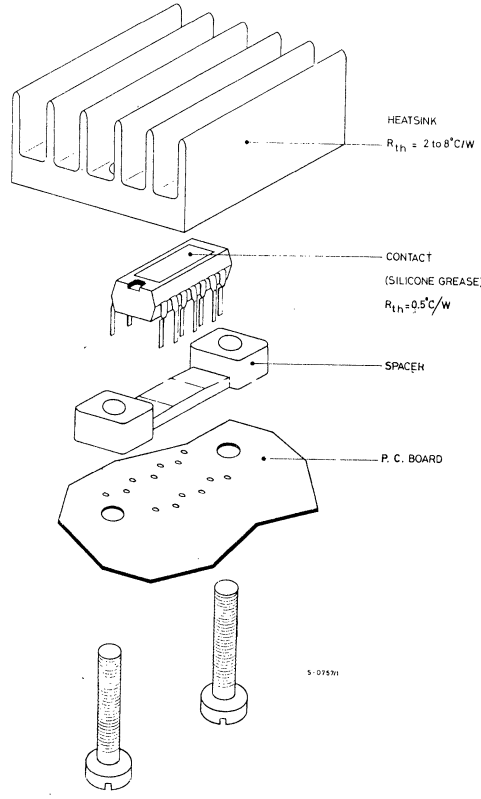
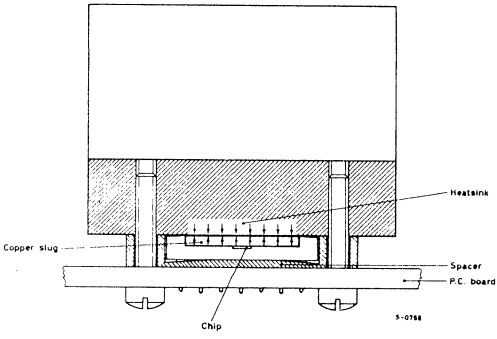
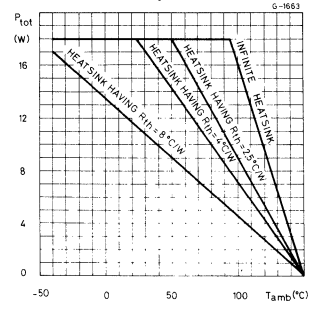


Fig. 23 - Cross-section of mounting system



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 24 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 24 - Maximum allowable power dissipation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA2020

20W Hi-Fi AUDIO AMPLIFIER

The TDA 2020 is a monolithic integrated **operational amplifier** in a 14-lead quad in-line plastic package, intended for use as a low frequency class B power amplifier. Typically it provides 20W output power (d = 1%) at ± 18V/4Ω; the guaranteed output power at ± 17V/4Ω is 15W (DIN norm 45500). The TDA 2020 provides high output current (up to 3.5 A) and has very low harmonic and cross-over distortion. Further, the device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep to working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.

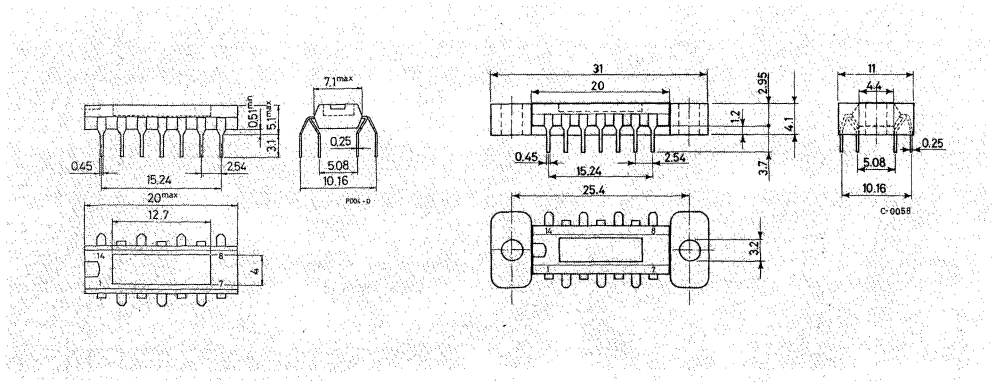
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 22	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at $T_{case} \leqslant 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

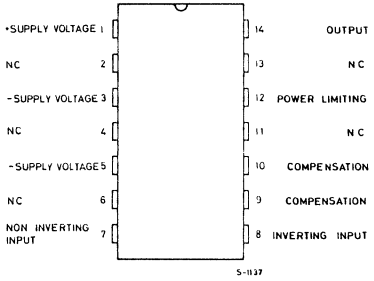
ORDERING NUMBERS: TDA 2020 A82 dual in-line plastic package
TDA 2020 A92 quad in-line plastic package
TDA 2020 AC2 dual in-line plastic package with spacer
TDA 2020 AD2 quad in-line plastic package with spacer

MECHANICAL DATA

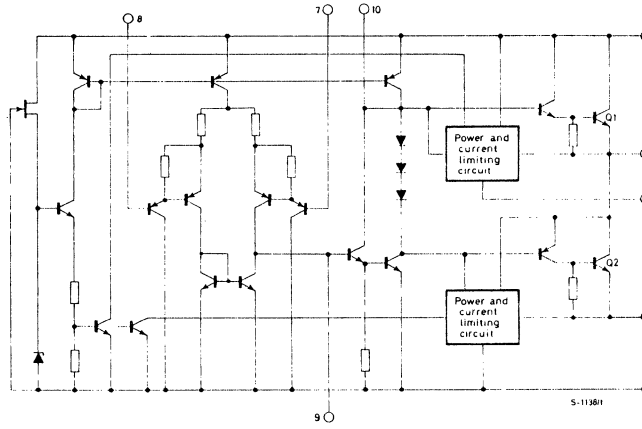
Dimensions in mm



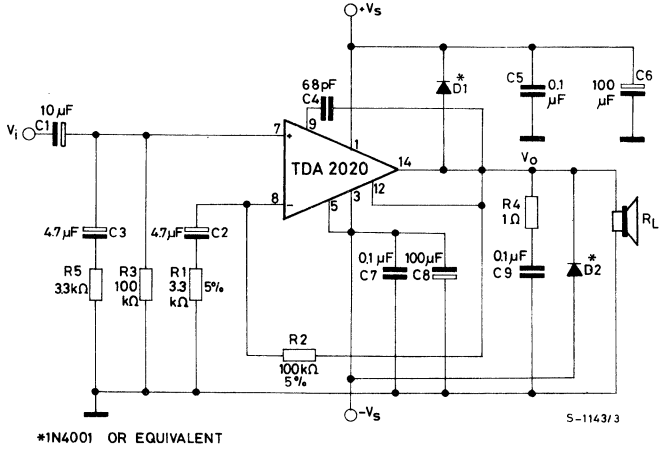
CONNECTION AND SCHEMATIC DIAGRAMS
(top view)



The copper slug is electrically connected to pin 5 (substrate)



TEST CIRCUIT



*1N4001 OR EQUIVALENT

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $V_s = \pm 17V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 5		± 22	V
I_d	Quiescent drain current	V_s = ± 22 V		60		mA
I_b	Input bias current			0.15		μA
V_{os}	Input offset voltage			5		mV
I_{os}	Input offset current			0.05		μA
V_{os}	Output offset voltage			10	100	mV
P_o	Output power	d = 1% G_v = 30 dB $T_{case} \leq 70°C$ f = 40 to 15 000 Hz				
		V_s = ± 17V R_L = 4 Ω V_s = ± 18V R_L = 4 Ω V_s = ± 18V R_L = 8 Ω	15	18.5 20 16.5		W W W
		d = 10% G_v = 30 dB $T_{case} \leq 70°C$ f = 1 kHz				
		V_s = ± 17V R_L = 4 Ω V_s = ± 18V R_L = 8 Ω		24 20		W W
V_i	Input sensitivity	G_v = 30 dB f = 1 kHz P_o = 15 W				
		V_s = ± 17V R_L = 4 Ω V_s = ± 18V R_L = 8 Ω		260 380		mV mV
B	Frequency response (-3 dB)	R_L = 4 Ω C4 = 68 pF		10 to 160 000		Hz
d	Distortion	P_o = 150 mW to 15W R_L = 4 Ω G_v = 30 dB $T_{case} \leq 70°C$				
		f = 1 kHz f = 40 to 15 000 Hz		0.2 0.3	 1	% %
		P_o = 150 mW to 15W V_s = ± 18V R_L = 8 Ω G_v = 30 dB $T_{case} \leq 70°C$				
		f = 1 kHz f = 40 to 15 000 Hz		0.1 0.25		% %
R_i	Input resistance (pin 7)			5		MΩ
G_v	Voltage gain (open loop)	R_L = 4 Ω f = 1 kHz		100		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
e_N	Input noise voltage	R_L = 4 Ω		4		μV
i_N	Input noise current	B(-3 dB) = 10 to 20,000 Hz		0.1		nA
SVR	Supply voltage rejection	R_L = 4 Ω G_v = 30 dB f_{ripple} = 100 Hz		50		dB
I_d	Drain current	P_o = 18.5W R_L = 4 Ω		1		A
		P_o = 16.5W V_s = ± 18V R_L = 8 Ω		0.7		A
T_{sd}	Thermal shut-down junction temperature			140		°C
T_{sd}	Thermal shut-down case temperature	P_{tot} = 15.5W		105		°C

Fig. 1 - Output power vs. supply voltage

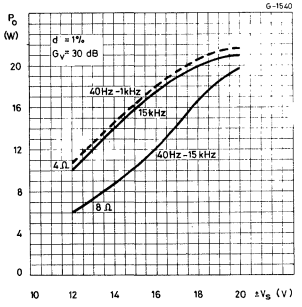


Fig. 2 - Output power vs. supply voltage

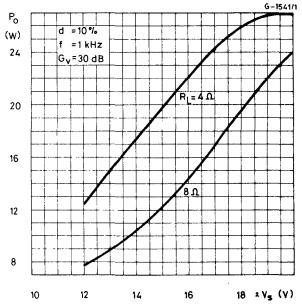


Fig. 3 - Distortion vs. output power

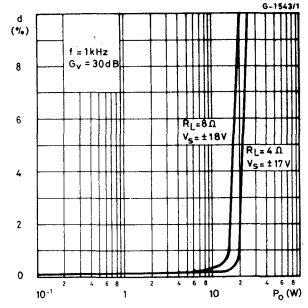


Fig. 4 - Distortion vs. output power ($R_L = 4\ \Omega$)

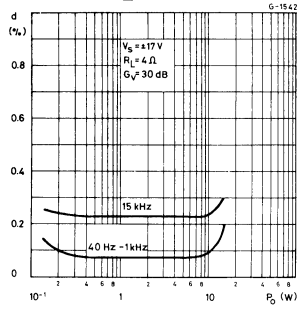


Fig. 5 - Distortion vs. output power ($R_L = 8\ \Omega$)

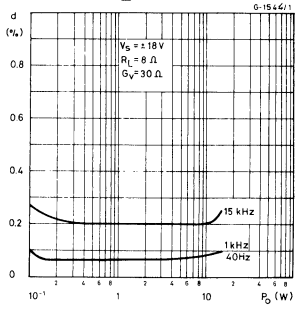


Fig. 6 - Distortion vs. frequency

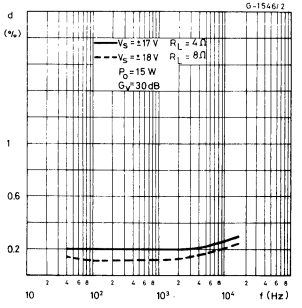


Fig. 7 - Output power vs. frequency

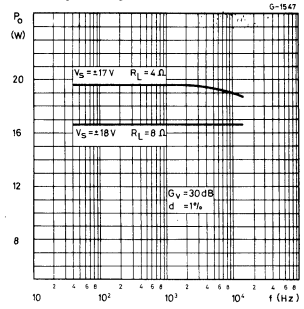


Fig. 8 - Sensitivity vs. output power ($R_L = 4\ \Omega$)

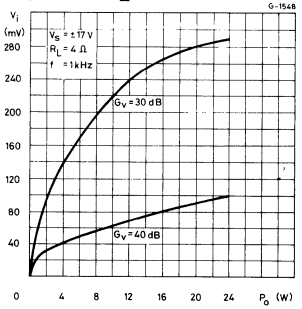


Fig. 9 - Sensitivity vs. output power ($R_L = 8\ \Omega$)

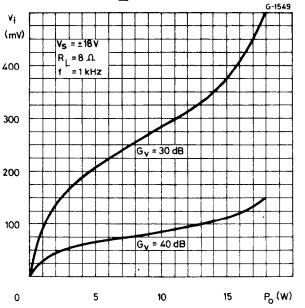


Fig. 10 - Open loop frequency response with different values of the rolloff capacitor C4

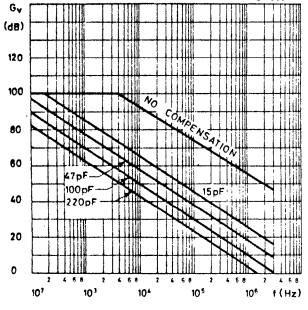


Fig. 11 - Value of C4 vs. voltage gain for different bandwidths

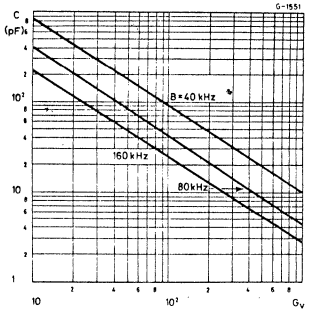


Fig. 12 - Quiescent current vs. supply voltage

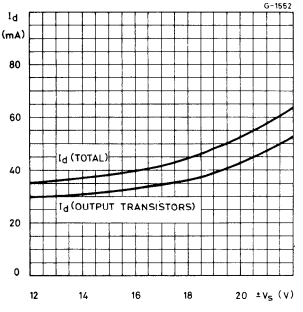


Fig. 13 - Supply voltage rejection vs. voltage gain

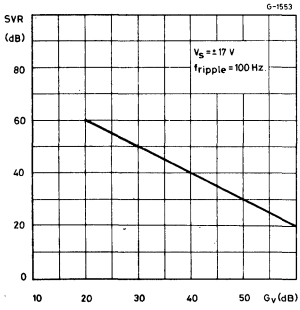


Fig. 14 - Power dissipation and efficiency vs. output power

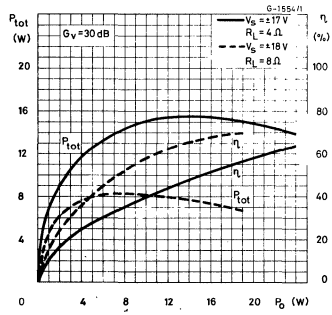
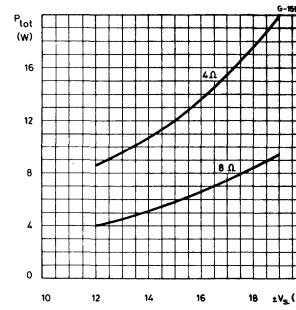


Fig. 15 - Maximum power dissipation vs. supply voltage (sine wave operation)



APPLICATION INFORMATION

Fig. 16 - Application circuit with split power supply

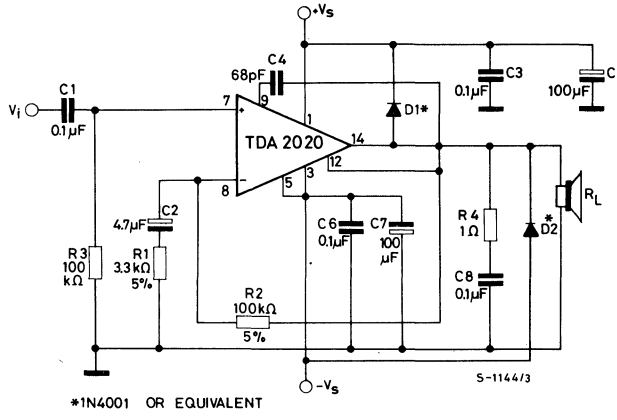


Fig. 17 - P.C. Board and component layout for the circuit of fig. 16 (1:1 scale)

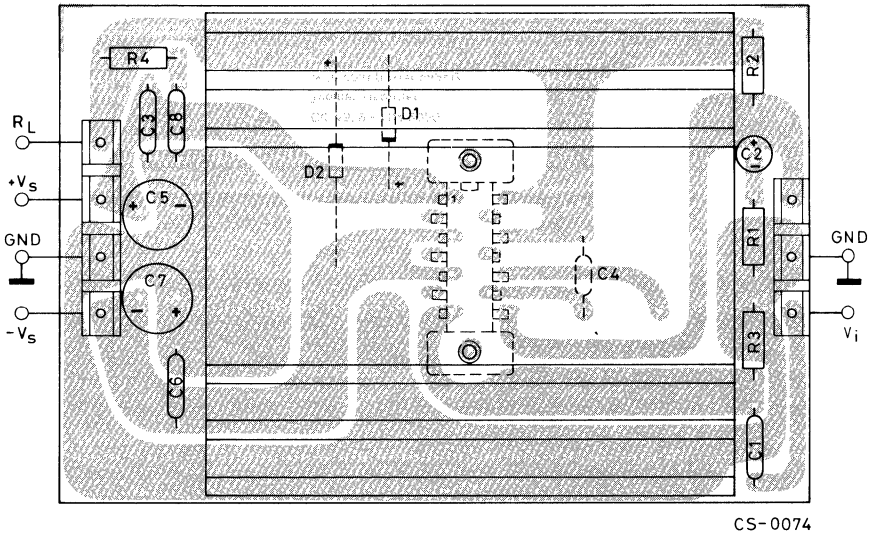
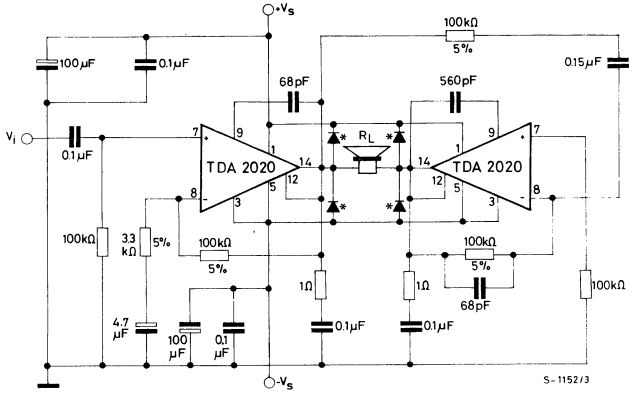


Fig. 18 - 30W bridge amplifier configuration with split power supply ($R_L = 8\ \Omega$ d $\leqslant 1\%$; $V_s = \pm 17V$)



SHORT CIRCUIT PROTECTION

The most important innovation in the TDA 2020 is an original circuit which limits the current of the output transistors. Fig. 19 shows that the maximum output current is a function of the collector-emitter voltage; hence the output transistors work within their safe operating area (fig. 20). This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2020 is thus protected against temporary overloads or short circuit. Should the short circuit exists for a longer time, the thermal shut-down comes into action and keeps the junction temperature within safe limits.

Fig. 19 - Maximum output current vs. voltage (V_{CE}) across each output transistor

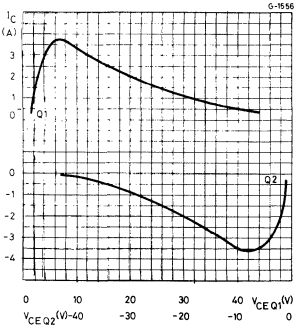
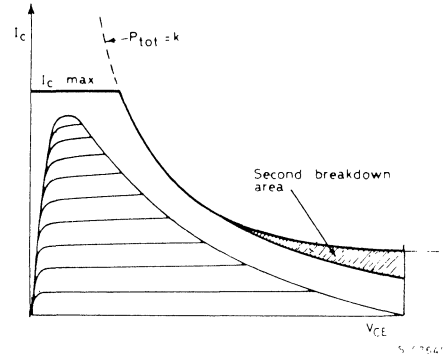


Fig. 20 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an above-limit ambient temperature can be easily supported since the T_j cannot be higher than 150° C
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If, for any reason, the junction temperature increases up to 150° C, the thermal shut-down simply reduces the power dissipation and the current consumption.

Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\ \Omega$)

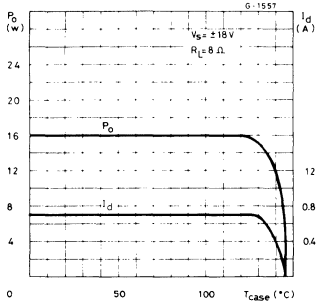


Fig. 22 - Output power and drain current vs. case temperature ($R_L = 4\ \Omega$)

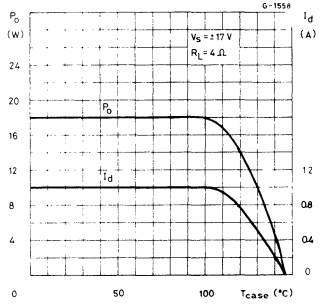
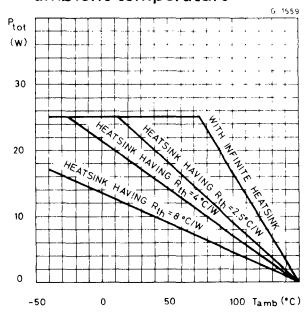


Fig. 23 - Maximum allowable power dissipation vs. ambient temperature



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink as shown in figs. 24 and 25.
The system for attaching the heatsink is very simple: it uses a plastic spacer which is supplied with the device.
Thermal contact between the copper slug (of the package) and the heatsink is guaranteed by the pressure which the screws exert via the spacer and the printed circuit board; this is due to the particular shape of the spacer.
Note: the most negative supply voltage is connected to the copper slug, hence to the heatsink (because it is in contact with the slug).

Fig. 24 - Mounting system of TDA 2020

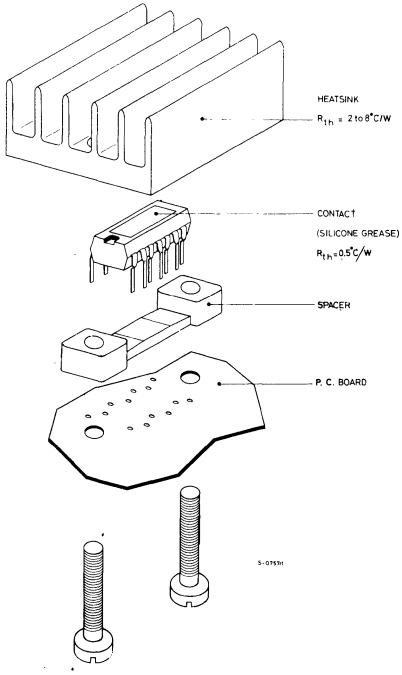
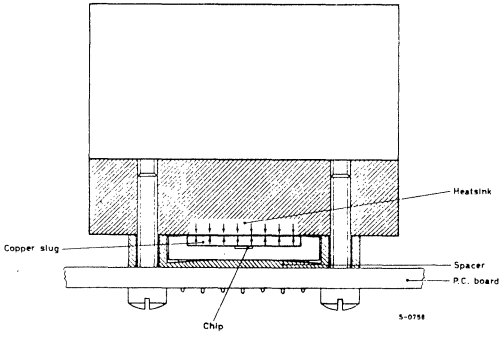


Fig. 25 - Cross-section of mounting system



TDA2020D

LINEAR INTEGRATED CIRCUIT

40W AUDIO DRIVER

- HIGH SUPPLY VOLTAGE: ± 25V
- HIGH SUPPLY REJECTION: 80 dB
- PROGRAMMABLE SOA PROTECTION
- LOW DISTORTION (0.05% TYP.)
- LOW INPUT NOISE VOLTAGE (4 μV TYP.)

The TDA 2020D is a monolithic integrated **operational amplifier** in a 14 lead quad in-line plastic-package, intended for driving external power transistors in Hi-Fi amplifier (30 to 100W). This device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the external transistors within their safe operating area. A thermal shut-down system is also included. This thermal shut-down can also protect the external power transistors.

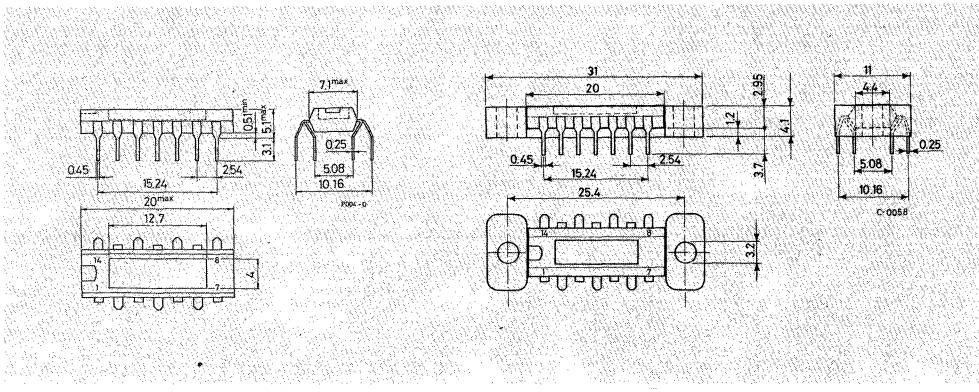
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 25	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current	1	A
P_{tot}	Power dissipation at $T_{case} \leqslant 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

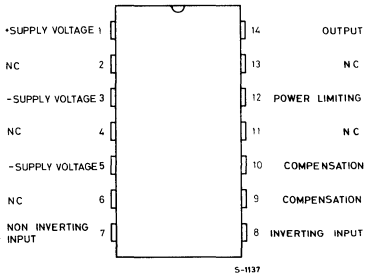
ORDERING NUMBERS: TDA 2020D A82 dual in-line plastic package
TDA 2020D A92 quad in-line plastic package
TDA 2020D AC2 dual in-line plastic package with spacer
TDA 2020D AD2 quad in-line plastic package with spacer

MECHANICAL DATA

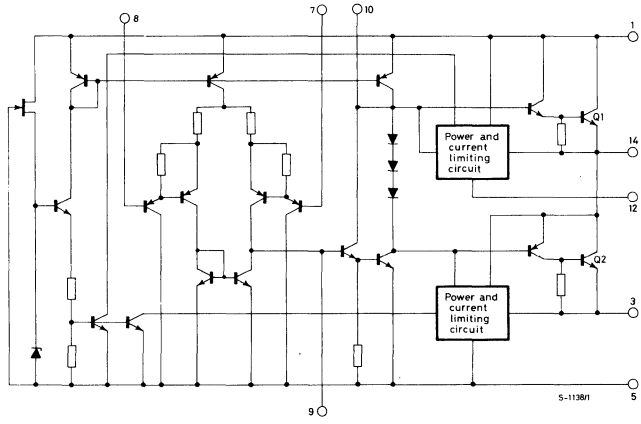
Dimensions in mm



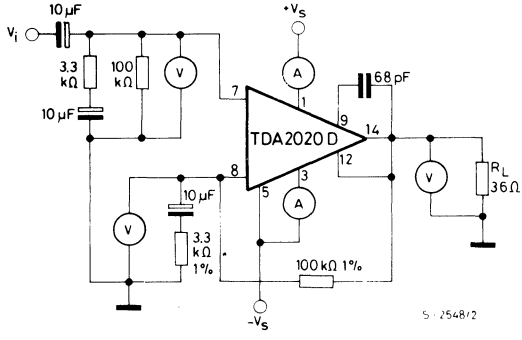
CONNECTION AND SCHEMATIC DIAGRAMS
(top view)



The copper slug is electrically connected to pin 5 (substrate)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= ±20V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 5		± 25	V
I_d	Quiescent drain current	V_s = ±25V		40	80	mA
I_b	Input bias current			0.15		μA
V_{os}	Input offset voltage			5		mV
I_{os}	Input offset current			0.05		μA
V_{os}	Output offset voltage			10	100	mV
$V_{CE(sat)}$	Output saturation voltage	I_o = 0.5A		± 1.7	± 2	V
B	Frequency response (-3 dB)	I_o = 0.5A		10 to 160 000		Hz
d	Distortion	G_v= 30 dB I_o = 0.5A f = 1 kHz f = 40 to 15 000 Hz		 0.05 0.2	 0.3	 % %
	Intermodulation	DIN 45500		0.2		%
R_i	Input resistance (pin 7)			5		MΩ
G_v	Voltage gain (open loop)	f = 1 kHz		100		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB
e_N	Input noise voltage	B (-3 dB) = 10 to 20 000 Hz		4		μV
i_N	Input noise current			0.1		nA
SVR	Supply voltage rejection	f_{ripple}= 100 Hz G_v= 30 dB	35	50		dB
I_d	Drain current	P_o = 4.5W R_L= 36Ω P_o = 2W R_L= 36Ω		160 100		mA mA
T_{sd}	Thermal shut-down junction temperature			145		°C
T_{sd}	Thermal shut-down case temperature	P_{tot}= 5W		135		°C

Fig. 1 - Quiescent current vs. supply voltage

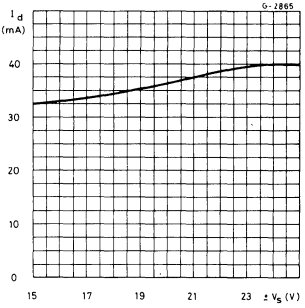


Fig. 2 - Output current vs. $V_{CE(sat)}$

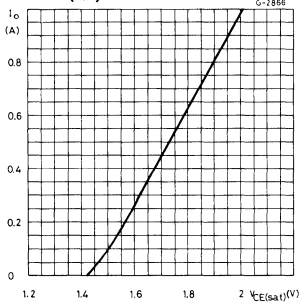


Fig. 3 - Power dissipation vs. supply voltage

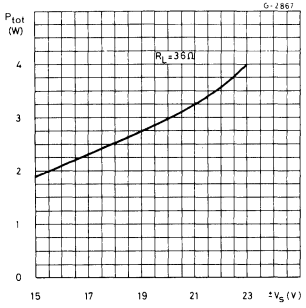


Fig. 4 - Open loop frequency response with different values of the rolloff capacitor

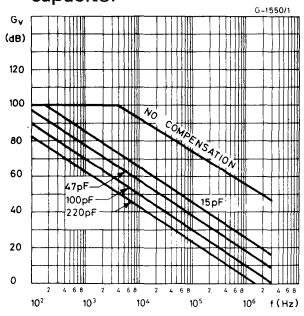


Fig. 5 - Value of rolloff capacitor vs. voltage gain for different bandwidths

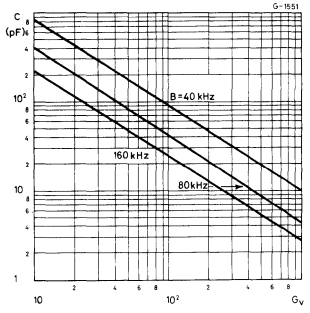


Fig. 6 - Supply voltage rejection vs. voltage gain

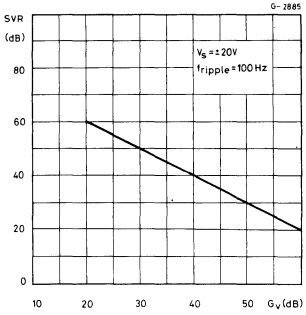


Fig. 7 - Transient response

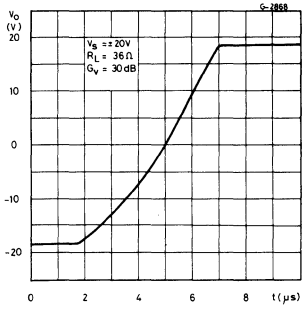
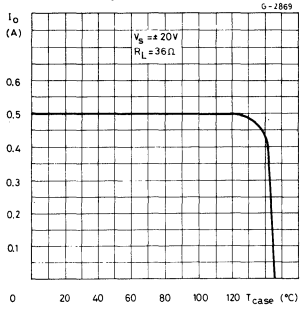
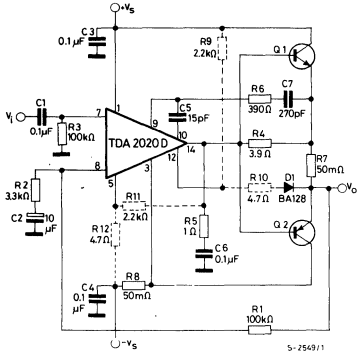


Fig. 8 - Output current vs. case temperature



APPLICATION INFORMATION

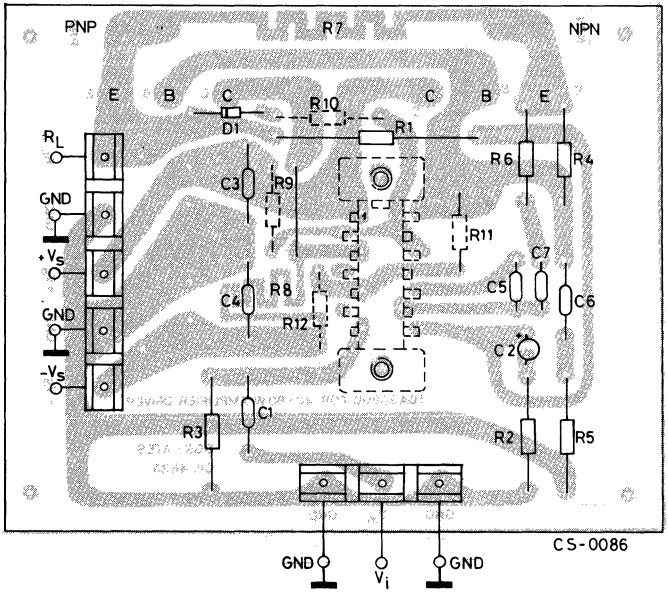
Fig. 9 - Application circuit for P_o= 30 to 50W



Note:
Resistors R9, R10, R11 and R12 are optional. Their purpose is to change the allowable operating area of the output transistors (see fig. 23).
The designer can choose different values according to working conditions (V_s, R_L) and to the SOA of the external transistors. When these resistors are not used the application circuit is modified as follows:

a) R7, R8 are changed to 25 mΩ.
b) R10, R12 are substituted by a short circuit.

Fig. 10 - P.C. board and component layout for the circuit of fig. 9 (1:1 scale)



P_o R_L= 4Ω	30W	40W
± V_s	18V	20V
R9/R11	–	2.2 kΩ
R10/R12	4.7Ω	4.7Ω
Q1	BD707 or BDW21A	BD907 or BDW21A
Q2	BD708 or BDW22A	BD908 or BDW22A

Note:
If resistors R9, R10, R11 and R12 are not used, R7 and R8 must be 25 mΩ. The following table shows what length of wire (copper and constantan) is required to obtain a resistor of 25 mΩ for different values of φ

φ (mm)	1	0.8	0.7	0.5	0.4	0.3
l (mm) copper	–	–	570	290	180	100
l (mm) constantan	40	25	20	10	6.5	–

Application suggestions

The recommended values of the components are those shown in application circuit of fig. 9, although different values can be used. The following table may help the amplifier designers.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
C1	0.1 μF	Elimination of DC current on volume control	Reduced lower cutoff frequency	Increased lower cutoff frequency
C2	10 μF	To obtain DC gain equal to 1	Reduced lower cutoff frequency	Increased lower cutoff frequency
C3 and C4	0.1 μF	Frequency stabilization		Danger of oscillations
C5	15 pF	Upper frequency cutoff	Reduced upper cutoff frequency	Increased upper cutoff frequency
C6	0.1 μF	Frequency stabilization		Danger of oscillation
C7	270 pF	Compensation		Danger of oscillations
R1	100 kΩ	Closed loop gain determination	Larger closed loop gain	Smaller closed loop gain
R2	3.3 kΩ	Closed loop gain determination	Smaller closed loop gain	Larger closed loop gain
R3	R1	Input bias	Output DC offset variation	Output DC offset variation
R4	3.9 Ω	External power transistor driving	Danger of distortion	Increased load for the driver
R5	1 Ω	Frequency stabilization	Danger of oscillations	Danger of oscillations
R6	390 Ω	Compensation		
R7 and R8	50 mΩ	Current protection sensing	Reduced maximum output current value	Increased maximum output current value
R9, R10, R11, R12	see Fig. 23			
Q1 - Q2	BD 707 – BD 708 or BD 907 – BD 908 or BDW 21A – BDW 22A			
D1	BA 128	Short circuit prot.		

Fig. 11 - Output power vs. supply voltage

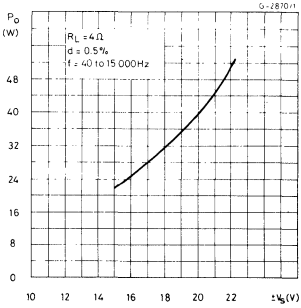


Fig. 12 - Output power vs. supply voltage

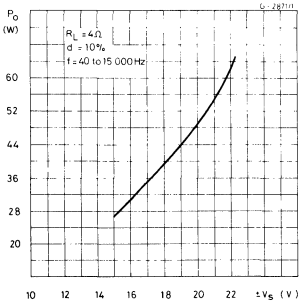


Fig. 13 - Distortion vs. output power

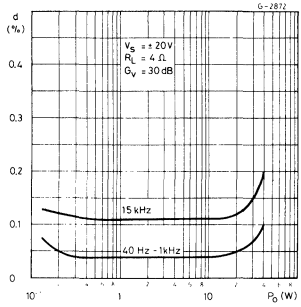


Fig. 14 - Distortion vs. output power

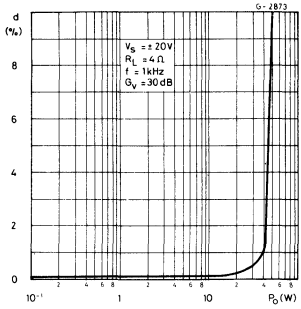


Fig. 15 - Distortion vs. frequency

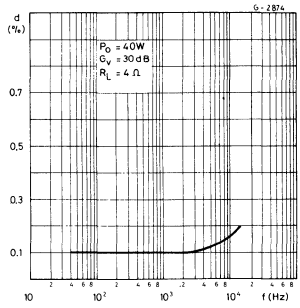


Fig. 16 - Input sensitivity vs. output power

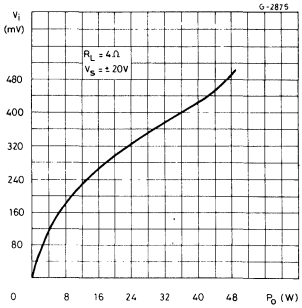


Fig. 17 - Maximum power dissipation vs. supply voltage (sine wave operation)

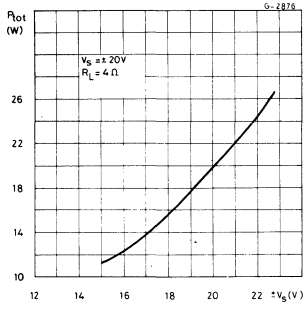


Fig. 18 - Power dissipation and efficiency vs. output power

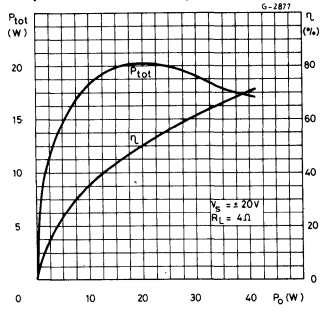
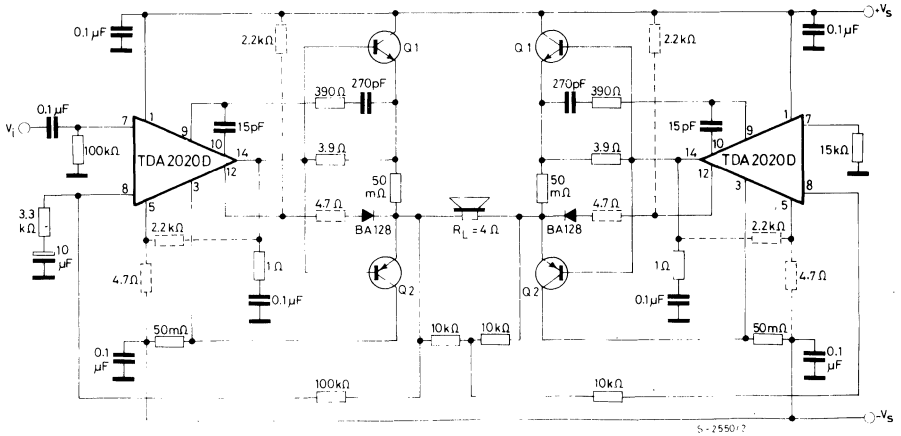


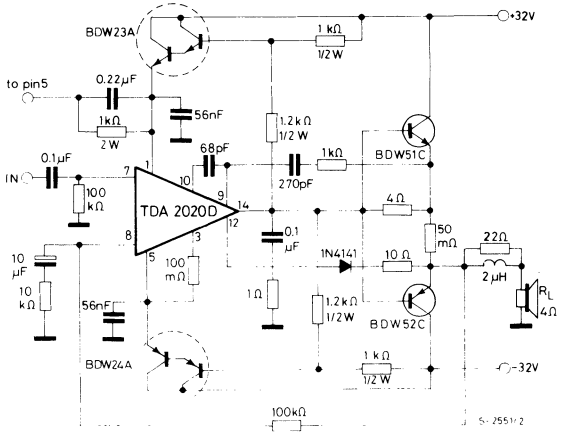
Fig. 19 - 60W to 100W bridge configuration application circuit



Note: With a bridge configuration the output power is increased while the other performances are the same as that of the application in fig. 9. The table shows the output power that can be obtained using different power transistor pairs.

A { Q1 = BDW21A; Q2 = BDW22A; V_s = ±15V; R_L = 4Ω • 60W
B { Q1 = BD707; Q2 = BD708; V_s = ±20V; R_L = 8Ω • 80W
C { Q1 = BDW51A; Q2 = BDW52A; V_s = ±18V; R_L = 4Ω • 100W

Fig. 20 - 80W Hi-Fi amplifier



For this application the maximum value of V_s in no-load condition is ± 45V.

Application suggestions for circuit in fig. 20

Using the two circuits shown in fig. 21 and fig. 22 it is possible to use a transformer with a large spread of output voltage between load and no-load condition.
The voltage on pins 1 and 5 follows V_o according to the equations:

$$V_1 = V_o + (V_s - V_o) \cdot \frac{R2}{R1 + R2} - 2\,V_{BE}$$

$$V_5 = V_o - (V_s + V_o) \cdot \frac{R2}{R1 + R2} + 2\,V_{BE}$$

while the voltage between pins 1 and 5 is a constant. In fact:

$$V_{1\text{-}5} = V_1 - V_5 = V_s \cdot \frac{2\,R2}{R1 + R2} - 4\,V_{BE}$$

$V_{1\text{-}5}$ must not exceed 50V and then the maximum value of V_s in no-load condition will be:

$$V_{s\,max} = (50 + 4\,V_{BE}) \cdot \frac{R1 + R2}{2\,R2}$$

The minimum value of V_s depends on the output power requested and will be:

$$V_{s(min)} = V_L + V_{CE\,(sat)} \text{ with } V_L = \sqrt{2\,P_o\,R_L}$$

Resistance R2 must be greater than R1 to guarantee a positive voltage on pin 1 and a negative voltage on pin 5 for correct working of TDA 2020D.

Note 1 – Between pins 1 and 5 a ceramic capacitor must be inserted to guarantee good stability.

Note 2 – It is possible to insert an electrolytic capacitor (10 μF) between pin 1 and GND and between pin 5 and GND, but in this case the maximum output voltage must be $V_{peak} = 23V$.

With the circuit in fig. 22 the voltage at pins 1 and 5 is kept constant by two zener diodes. In load conditions a current equal to $I_o = I/\beta$ flows in R; the value of R is then given by $R = \frac{(V_{CE} - V_{BE})}{I}\beta$. In no-load condition, if ΔV is the increase in the supply voltage, the zener diodes dissipate a power depending on ΔV and β according to the equation:

$$P_z = V_z \cdot I_z = V_z \cdot \frac{\Delta V}{R} = V_z \cdot \frac{\Delta V \cdot I}{\beta\,(V_{CE} - V_{BE})}$$

Fig. 21

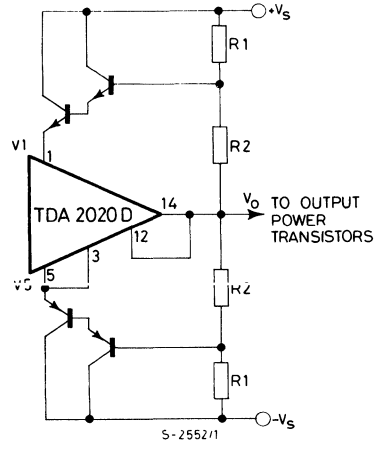
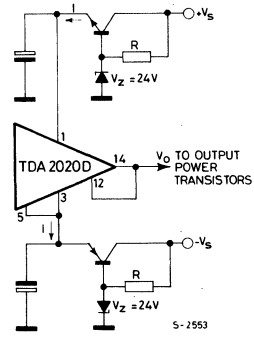


Fig. 22



SHORT CIRCUIT PROTECTION

The most important innovation in the TDA 2020D is an original circuit which limits the current of the output transistors. Fig. 23 shows that the maximum output current is a function of the collector-emitter voltage; hence the output transistors work within their safe operating area (fig. 24). This function can therefore be considered as being peak power limiting rather than simple current limiting.
By choosing the appropriate values for R9, R10, R11, R12, (fig. 9) the maximum output current can be established as a function of the SOA of the output parameters being used.

Fig. 23 - Maximum output current vs. voltage [$V_{Ce(sat)}$] across one output transistor, for different values of R10 (typical application circuit)

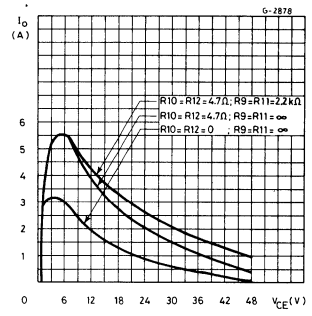
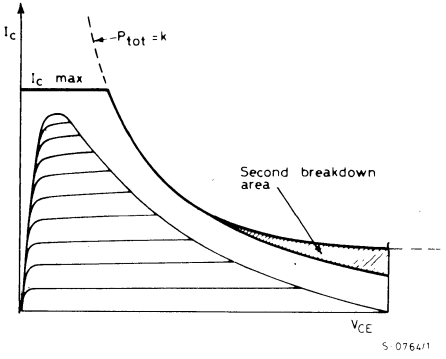


Fig. 24 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent) or an above-limit ambient temperature can be easily withstood since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller safety factor than a conventional circuit. There is no possibility of device damage due to high junction temperature.

If, for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.
The thermal protection unit of the TDA 2020D will also provide thermal protection of the output transistors if they are mounted on the same heatsink as the I.C.

MOUNTING INSTRUCTIONS

Fig. 25 - Mounting system of TDA 2020D

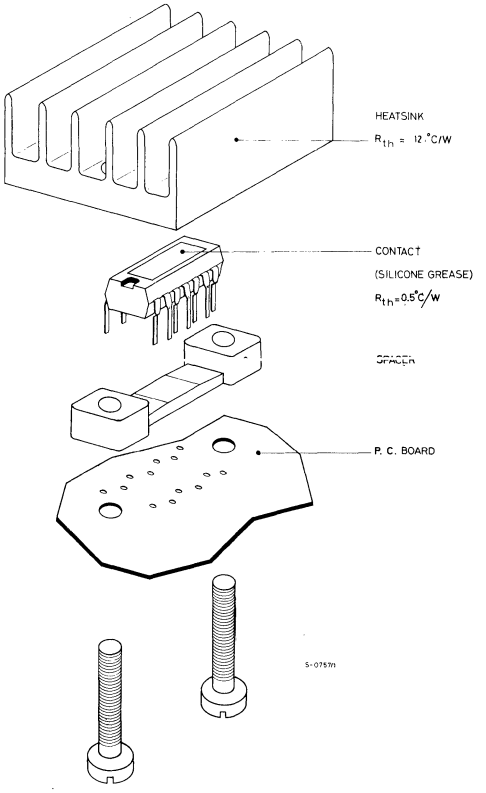
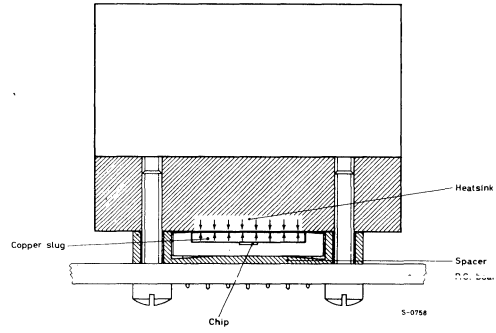


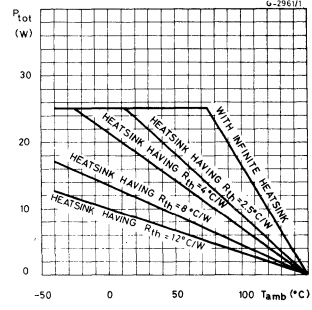
Fig. 26 - Cross-section of mounting system



The power dissipated in the circuit must be removed by adding an external heatsink as shown in figs. 25 and 26.
The system for attaching the heatsink is very simple: it uses a plastic spacer which is supplied with the device.
Thermal contact between the copper slug (of the package) and the heatsink is guaranteed by the pressure which the screws exert via the spacer and the printed circuit board; this is due to the special shape of the spacer.

Note: The most negative supply voltage is connected to the copper slug, hence to the heatsink (because it is in contact with the slug).

Fig. 27 - Maximum allowable power dissipation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA2030

14W Hi-Fi AUDIO AMPLIFIER

The TDA 2030 is a monolithic integrated circuit in Pentawatt® package. intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at ± 14V/4Ω; at ± 14V the guaranteed output power is 12W on a 4Ω load and 8W on a 8Ω (DIN 45500). The TDA 2030 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system si also included.

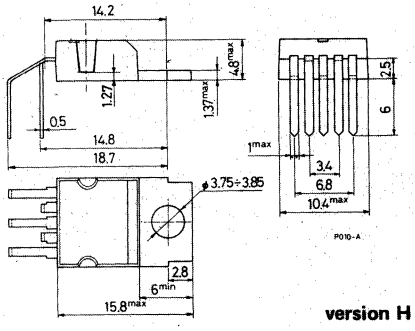
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

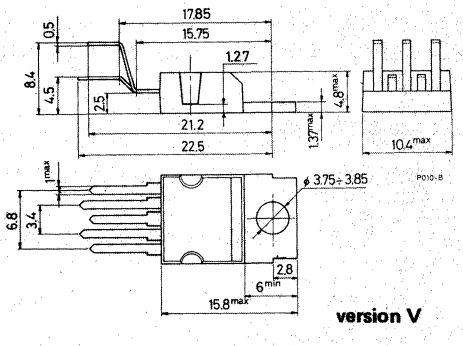
ORDERING NUMBERS: TDA 2030 H; TDA 2030 V

MECHANICAL DATA

Dimensions in mm

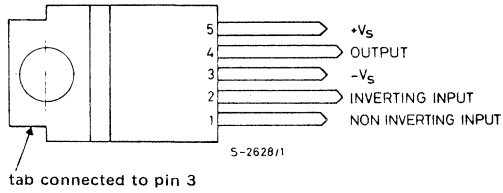


version H

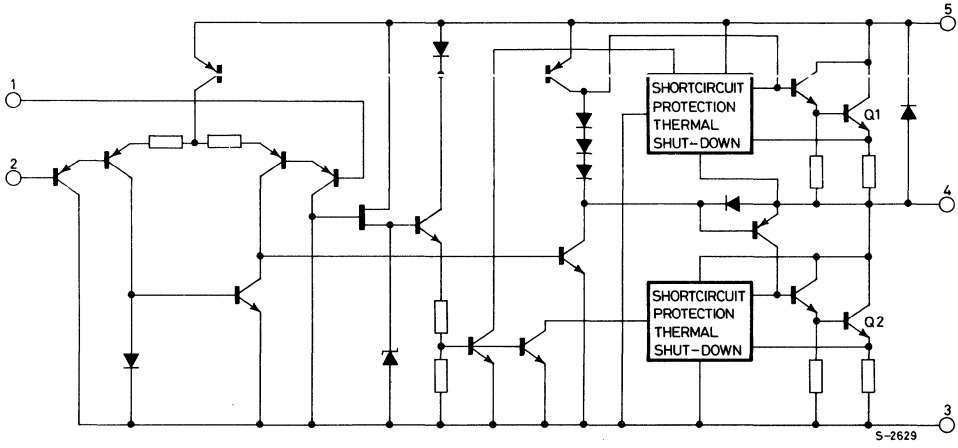


version V

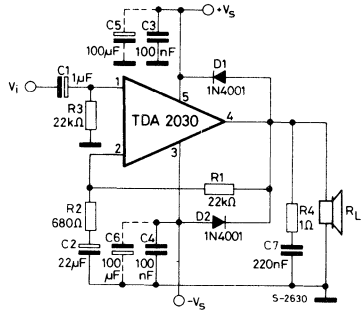
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 6		± 18	V
I_d	Quiescent drain current	$V_s = \pm 18V$		40	60	mA
I_b	Input bias current			0.2	2	μA
V_{os}	Input offset voltage			± 2	± 20	mV
I_{os}	Input offset current			± 20	± 200	nA
P_o	Output power	d = 0.5% G_v = 30 dB f = 40 to 15 000 Hz R_L = 4Ω R_L = 8Ω	 12 8	 14 9		 W W
		d = 10% G_v = 30 dB f = 1 kHz R_L = 4Ω R_L = 8Ω		 18 11		 W W
d	Distortion	P_o = 0.1 to 12W R_L = 4Ω G_v = 30 dB f = 40 to 15 000 Hz		0.2	0.5	%
		P_o = 0.1 to 8W R_L = 8Ω G_v = 30 dB f = 40 to 15 000 Hz		0.1	0.5	%
B	Power Bandwidth (-3 dB)	G_v = 30 dB P_o = 12W R_L = 4Ω	10 to 140 000			Hz
R_i	Input resistance (pin 1)		0.5	5		MΩ
G_v	Voltage gain (open loop)			90		dB
G_v	Voltage gain (closed loop)	f = 1 kHz	29.5	30	30.5	dB
e_N	Input noise voltage	B = 22 Hz to 22 KHz		3	10	μV
i_N	Input noise current	R_L = 4Ω		80	200	pA
SVR	Supply voltage rejection	R_L = 4Ω G_v = 30 dB R_g = 22 kΩ V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz	40	50		dB
I_d	Drain current	P_o = 14W R_L = 4Ω P_o = 9W R_L = 8Ω		900 500		mA mA
T_j	Thermal shut-down junction temperature			145		°C

Fig. 1 - Output power vs. supply voltage

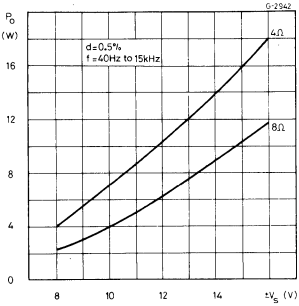


Fig. 2 - Output power vs. supply voltage

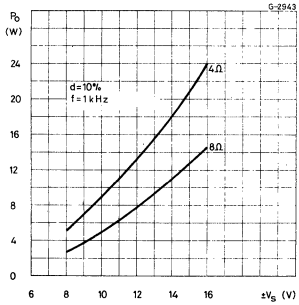


Fig. 3 - Distortion vs. output power

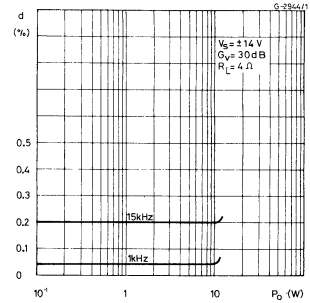


Fig. 4 - Distortion vs. output power

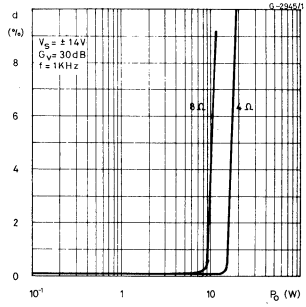


Fig. 5 - Distortion vs. output power

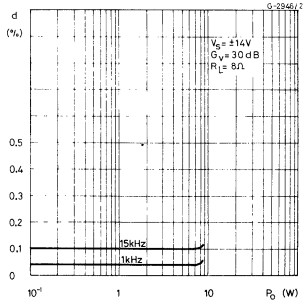


Fig. 6 - Distortion vs. frequency

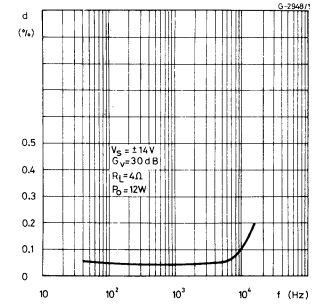


Fig. 7 - Distortion vs. frequency

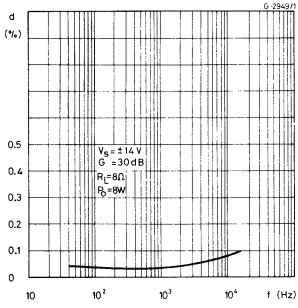


Fig. 8 - Frequency response with different values of the rolloff capacitor C8 (see fig. 13)

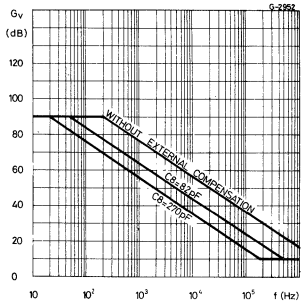


Fig. 9 - Quiescent current vs. supply voltage

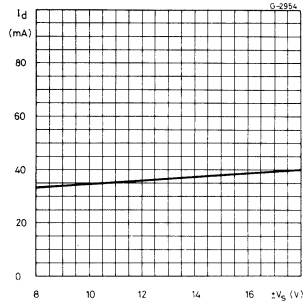


Fig. 10 - Supply voltage rejection vs. voltage gain

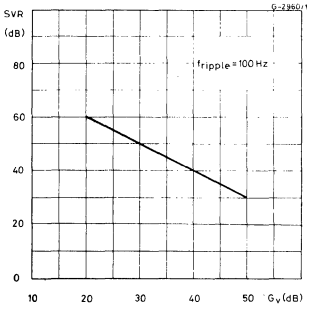


Fig. 11 - Power dissipation and efficiency vs. output power

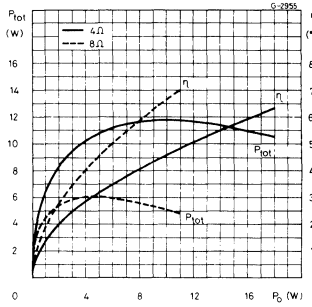
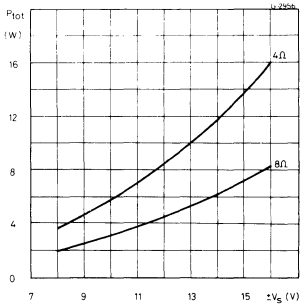


Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)



APPLICATION INFORMATION

Fig. 13 - Typical amplifier with split power supply

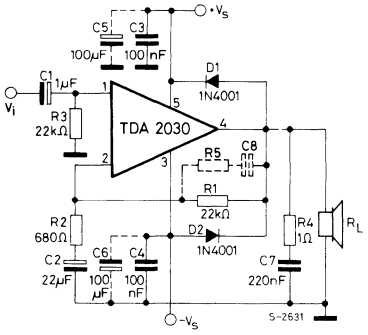
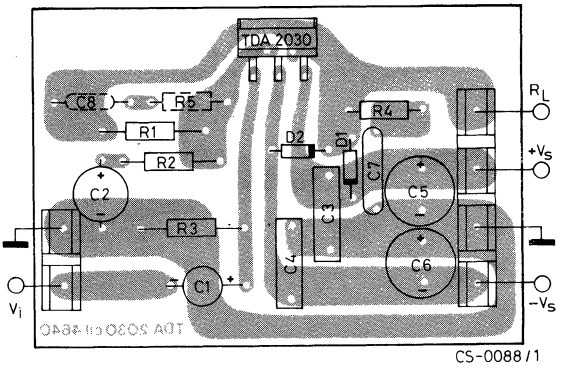


Fig. 14 - P.C. board and component layout for the circuit of fig. 13 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 15 - Typical amplifier with single power supply

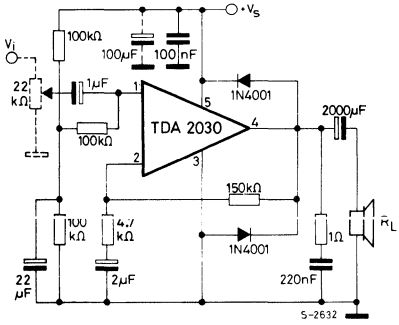


Fig. 16 - P.C. board and component layout for the circuit of fig. 15 (1:1 scale)

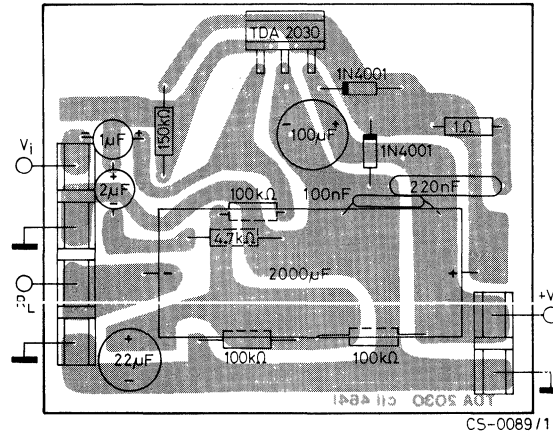
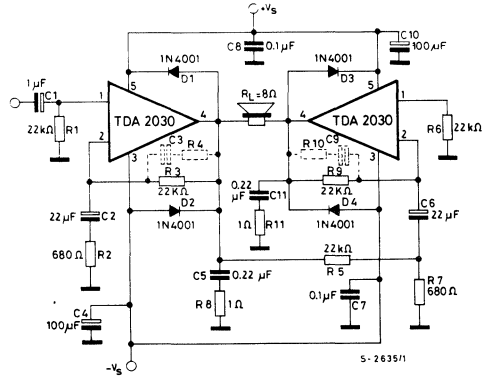


Fig. 17 - Bridge amplifier configuration with split power supply (P_o = 28W, V_s = ±14V)



APPLICATION INFORMATION (continued)

Fig. 18 - P.C. board and component layout for the circuit in fig. 17 (1 : 1 scale)

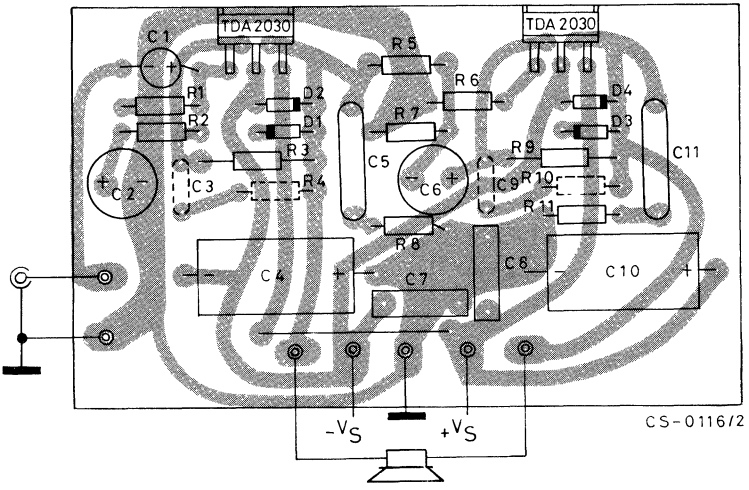
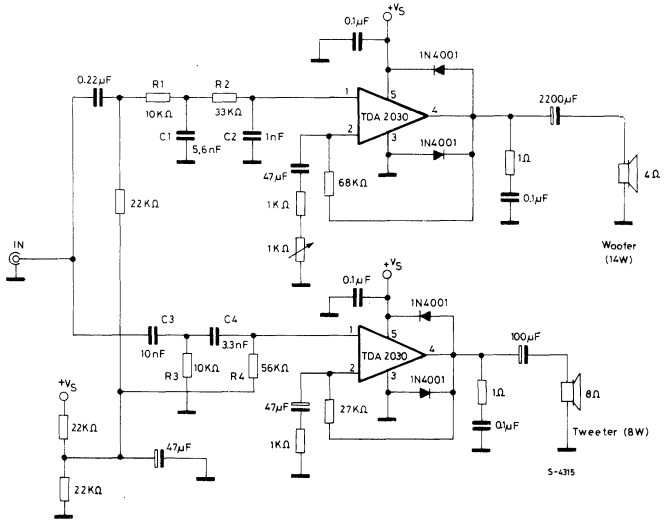


Fig. 19 - Two-way 22W Hi-Fi active-box



PRACTICAL CONSIDERATIONS

Printed circuit board

The layout shown in fig. 16 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

Application suggestions

The recommended values of the components are those shown on application circuit of fig. 13. Different values can be used. The following table can help the designer.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
R1	22 kΩ	Closed loop gain setting	Increase of gain	Decrease of gain
R2	680 Ω	Closed loop gain setting	Decrease of gain	Increase of gain
R3	22 kΩ	Non inverting input biasing	Increase of input impedance	Decrease of input impedance
R4	1 Ω	Frequency stability	Danger of oscillat. at high frequencies with induct. loads	
R5	$\cong$ 3 R2	Upper frequency cutoff	Poor high frequencies attenuation	Danger of oscillation
C1	1 μF	Input DC decoupling		Increase of low frequencies cutoff
C2	22 μ F	Inverting DC decoupling		Increase of low frequencies cutoff
C3,C4	0.1 μF	Supply voltage bypass		Danger of oscillation
C5,C6	100 μF	Supply voltage bypass		Danger of oscillation
C7	0.22 μF	Frequency stability		Danger of oscillat.
C8	$\cong \frac{1}{2\pi B R1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D1,D2	1N4001	To protect the device against output voltage spikes		

SHORT CIRCUIT PROTECTION

The TDA 2030 has an original circuit which limits the current of the output transistors.Fig. 20 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (fig. 21). This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2030 is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

Fig. 20 - Maximum output current vs. voltage [V_{CEsat}] across each output transitor

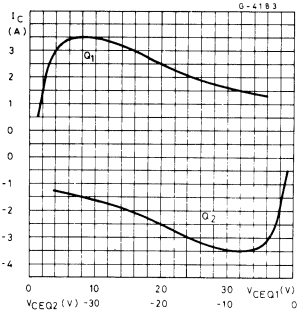
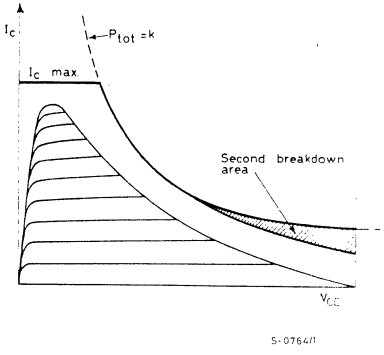


Fig. 21 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 24 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 22 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

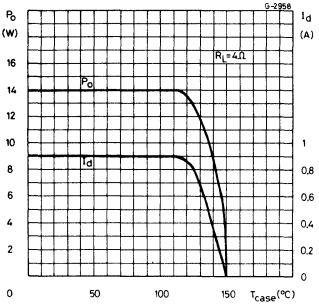


Fig. 23 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)

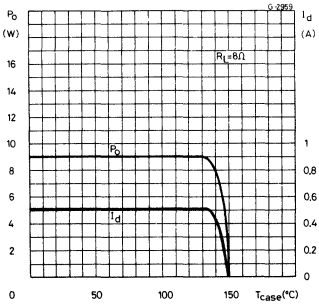


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature

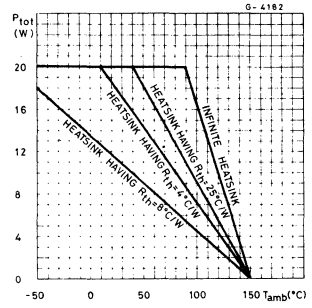
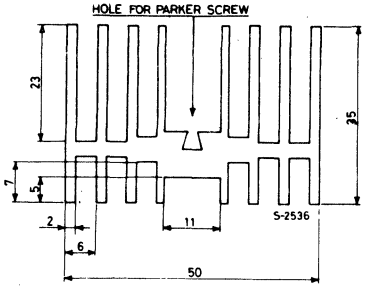


Fig. 25 - Example of heat-sink



Dimension : suggestion.

The following table shows the length that the heatsink in fig. 25 must have for several values of P_{tot} and R_{th}.

P_{tot}(W)	12	8	6
Length of heatsink (mm)	60	40	30
R_{th} of heatsink (°C/W)	4.2	6.2	8.3

LINEAR INTEGRATED CIRCUIT

TDA2030A

PRELIMINARY DATA

18W Hi-Fi AMPLIFIER AND 30W DRIVER

The TDA 2030A is a monolithic IC in Pentawatt® package intended for use as low frequency class AB amplifier.
With $V_{s\ max}$= 44V it is particularly suited for more reliable applications without regulated supply and for 30W driver circuits using low-cost complementary pairs.
The TDA 2030A provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.

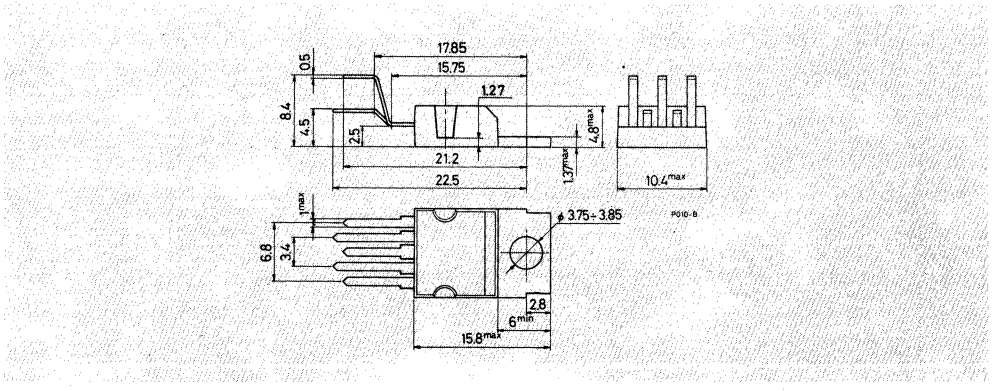
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 22	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current	3.5	A
P_{tot}	Total power dissipation at T_{case}= 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

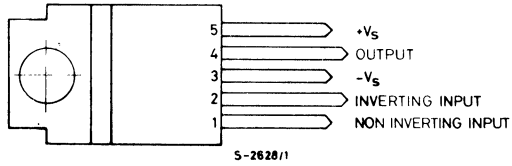
ORDERING NUMBER: TDA 2030AV

MECHANICAL DATA

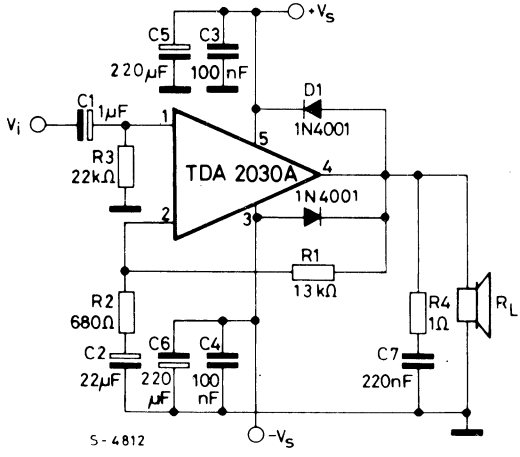
Dimensions in mm



CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= ±16V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			± 6		± 22	V
I_d	Quiescent drain current				50	80	mA
I_b	Input bias current	V_s = ± 22V			0.2	2	μA
V_{os}	Input offset voltage				± 2	± 20	mV
I_{os}	Input offset current				± 20	± 200	nA
P_o	Output power	d = 0.5% f = 40 to 15000 Hz	G_v = 26 dB R_L= 4 Ω R_L= 8 Ω	 15 10	 18 12		W
		V_s = ± 19V	R_L= 8Ω	13	16		
BW	Power bandwidth	P_o= 15W	R_L= 4 Ω		100		KHz
SR	Slew Rate				8		V/μsec
G_v	Open loop voltage gain	f = 1 KHz			80		dB
G_v	Closed loop voltage gain			25.5	26	26.5	dB
d	Total harmonic distortion	P_o= 0.1 to 14W f = 40 to 15000 Hz	R_L= 4 Ω f = 1 KHz		 0.08 0.03		%
		P_o = 0.1 to 9W f = 40 to 15000 Hz	R_L= 8 Ω		0.05		%
d_2	Second order CCIF intermodulation distortion	P_o= 4W R_L= 4Ω	f_2-f_1 = 1 KHz		0.03		%
d_3	Third order CCIF intermodulation distortion	f_1= 14 KHz f_2= 15 KHz	2 f_1-f_2= 13KHz		0.08		%
e_N	Input noise voltage	B = curve A			2		μV
		B = 22 Hz to 22 KHz			3	10	
i_N	Input noise current	B = curve A			50		pA
		B = 22 Hz to 22 KHz			80	200	
S/N	Signal to noise ratio	R_L= 4Ω R_g= 10 KΩ B = curve A	P_o = 15W		106		dB
			P_o = 1W		94		

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
R_i	Input resistance (pin 1)	(open loop)	f = 1 KHz	0.5	5		MΩ
SVR	Supply voltage rejection	R_L= 4 Ω R_g= 22 KΩ	G_v= 26 dB f = 100 Hz		54		dB
T_j	Thermal shut-down junction temperature				145		°C

Fig. 1 - Single supply amplifier

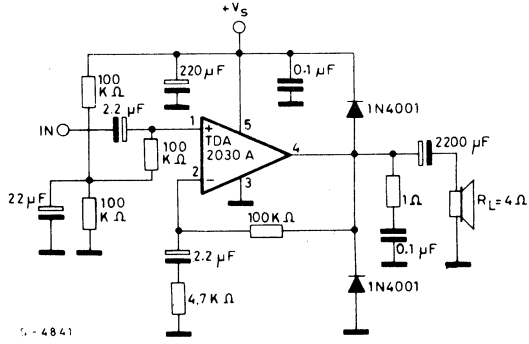


Fig. 2 - Open loop-frequency response

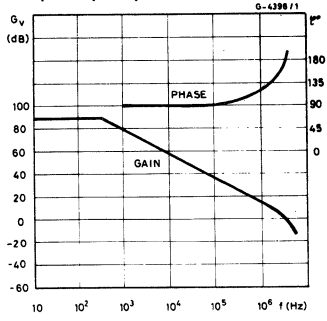


Fig. 3 - Output power vs. supply voltage

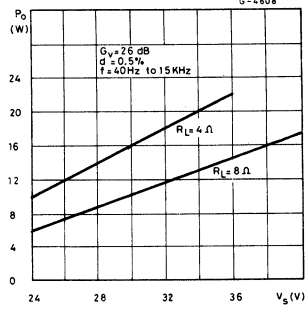
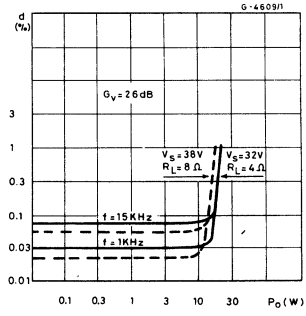


Fig. 4 - Total harmonic distortion vs. output power(*)



*) Test using noise filters.

Fig. 5 - Two tone CCIF intermodulation distortion

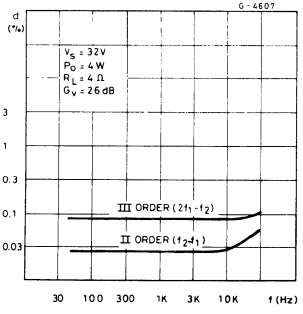


Fig. 6 - Large signal frequency response

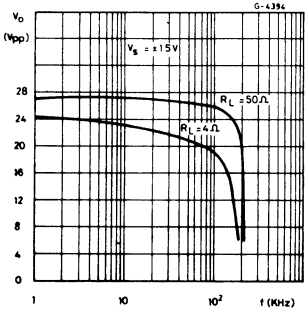


Fig. 7 - Maximum allowable power dissipation vs. ambient temperature

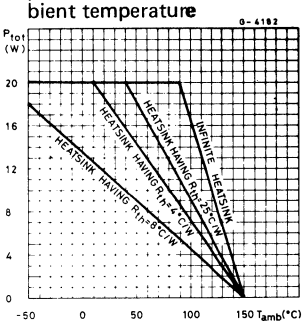


Fig. 8 - Split-supply high power amplifier (TDA 2030A + BD907/BD908)

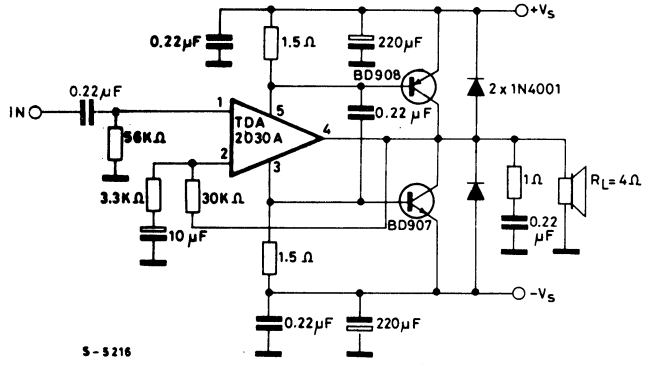


Fig. 9 - Single supply high power amplifier (TDA 2030A + BD907/BD908)

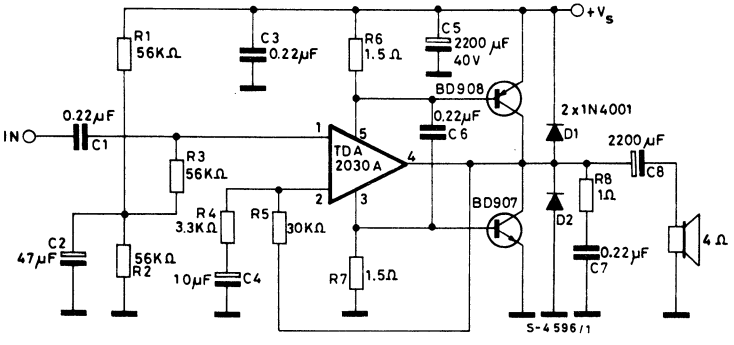
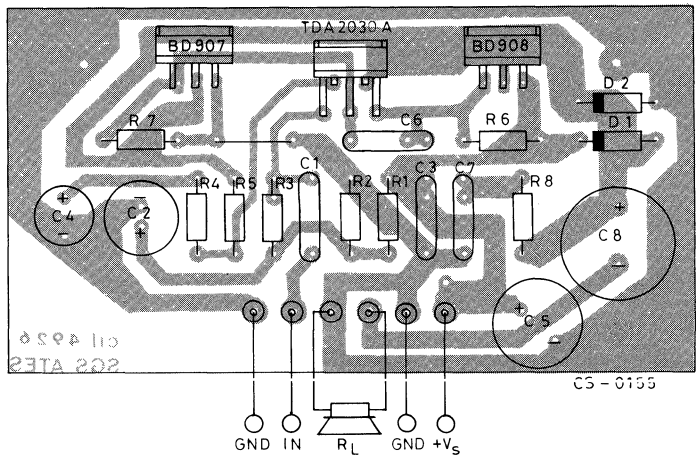


Fig. 10 - P.C. board and component layout for the circuit of fig. 9 (1:1 scale)



Typical performance of the circuit of fig. 9

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage				36	44	V
I_d	Quiescent drain current	V_s = 36V			50		mA
P_o	Output power	d = 0.5% R_L= 4Ω f = 40Hz to 15KHz	V_s= 39V		35		W
			V_s= 36V		28		
		d = 10%; f = 1KHz	V_s= 39V		44		W
		R_L= 4Ω	V_s= 36V		35		
G_v	Voltage gain	f = 1 KHz		19.5	20	20.5	dB
SR	Slew Rate				8		V/μsec
d	Total harmonic distortion	P_o= 20W	f = 1KHz		0.02		%
			f = 40 Hz to 15 KHz		0.05		
V_i	Input sensitivity	G_v= 20 dB P_o= 20W	f = 1 KHz R_L= 4Ω		890		mV
S/N	Signal to noise ratio	R_L= 4Ω R_g= 10 KΩ B = curve A	P_o= 25W		108		dB
			P_o= 4W		100		

Fig. 11 - Output power vs. supply voltage

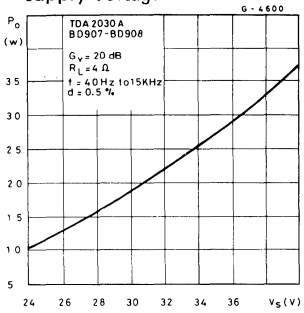


Fig. 12 - Total harmonic distortion vs. output power

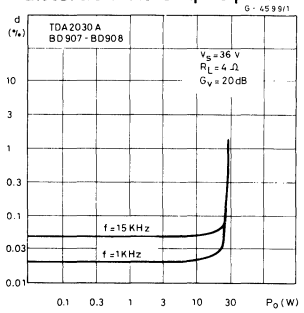


Fig. 13 - Output power vs. input level

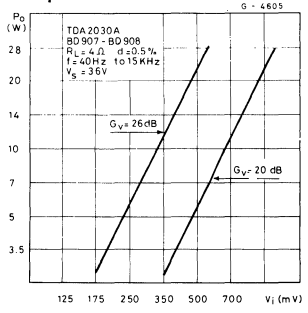


Fig. 14 - Power dissipation vs. output power

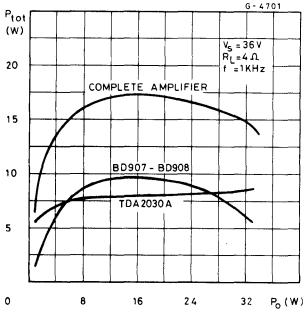


Fig. 15 - Typical amplifier whit split power supply

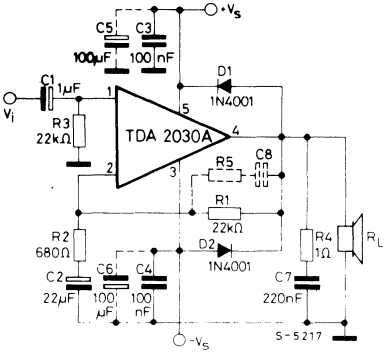


Fig. 16 - P.C. board and component layout for the circuit of fig. 15 (1 : 1 scale)

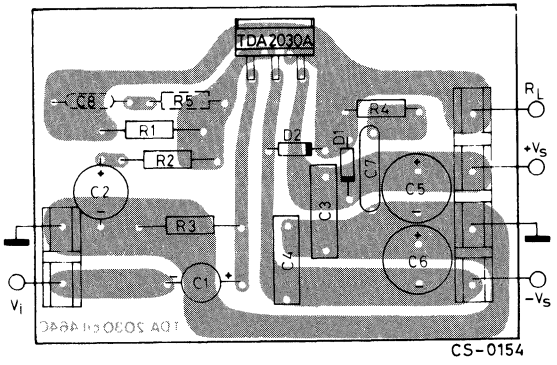


Fig. 17 - Bridge amplifier whit split power supply (P_o= 34W, V_s= ±16V)

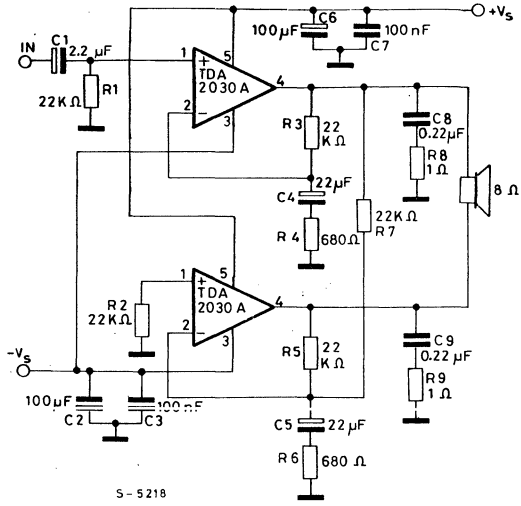
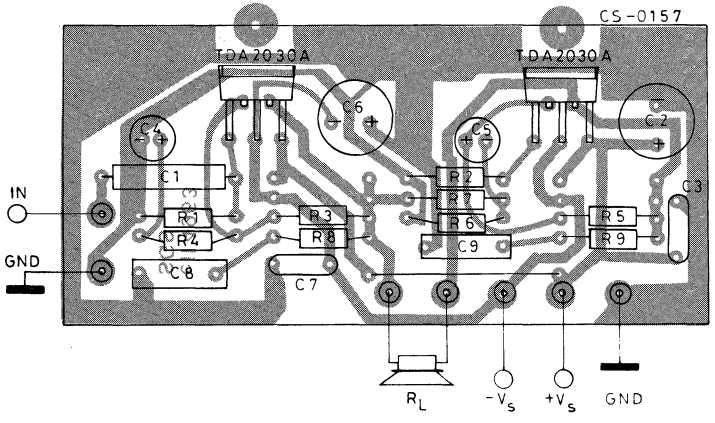


Fig. 18 - P.C. board and component layout for the circuit in fig. 17 (1:1 scale)



Multiway speaker systems and active boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two or three bands.
To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see fig. 19). As an example, a 100W three-way system with crossover frequencies of 400 Hz and 3 KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.
Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance.

Fig. 19 - Power distribution vs. frequency

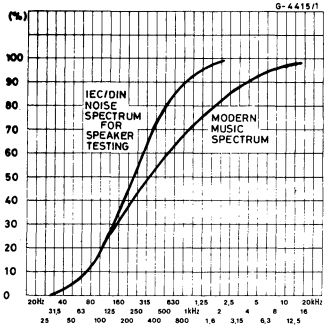
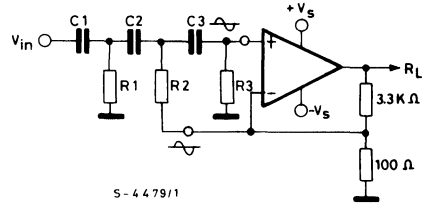


Fig. 20 - Active power filter



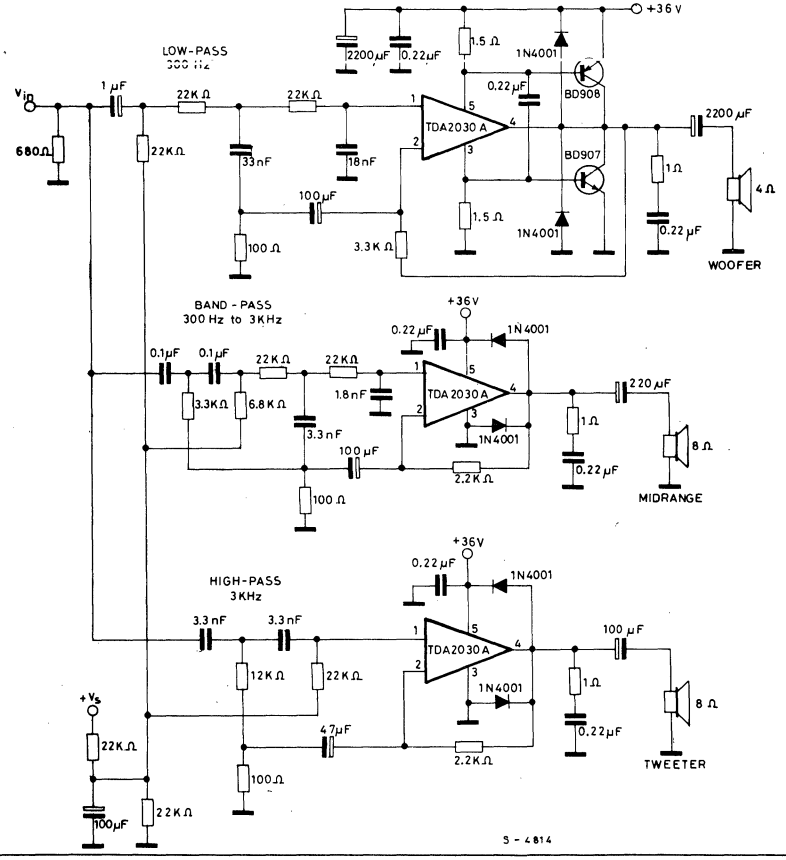
Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit.
This makes it particularly interesting and economically sound to use monolithic power amplifiers.
In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6 dB/octave) can be recommended.
The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.
The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.
A more effective solution, named "Active Power Filter" by SGS is shown in fig. 20.
The proposed circuit can realize combined power amplifiers and 12 dB/octave or 18 dB/octave high-pass or low-pass filters.
In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (–) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for f_c = 900 Hz using a Bessel 3rd order Sallen and Key structure are:

$C_1 = C_2 = C_3$	R_1	R_2	R_3
22 nF	8.2 KΩ	5.6 KΩ	33 KΩ

Using this type of crossover filter, a complete 3-way 60W active loudspeaker system is shown in fig. 21.
It employs 2nd order Buttherworth filters with the crossover frequencies equal to 300 Hz and 3 KHz.
The midrange section consists of two filters, a high pass circuit followed by a low pass network.
With V_s = 36V the output power delivered to the woofer is 25W at d = 0.06% (30W at d = 0.5%).
The power delivered to the midrange and the tweeter can be optimized in the design phase taking in account the louspeaker efficiency and impedance (R_L = 4Ω or 8Ω).
It is quite common that midrange and tweeter speakers have an efficiency 3 dB higher than woofers.

Fig. 21 - 3 way 60W active loudspeaker system (V_s = 36V)



Musical instruments amplifiers

Another important field of application for active systems is music.
In this area the use of several medium power amplifiers is more convenient than a single high power amplifier, and it is also more reliable.
A typical example (see fig. 22) consist of four amplifiers each driving a low-cost, 4Ω, 12 inch loudspeaker. This application can supply 80 to 160W rms.
Similar output power can be obtained by a single amplifier using the "superbridge" circuit of fig.24.As shown in the diagram of fig. 16 this circuit can supply output power of 120W and more.

Fig. 22 - High power active box for musical instrument

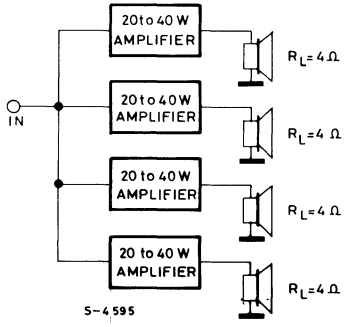


Fig. 23 - Output power vs. supply voltage (application circuit of fig. 24)

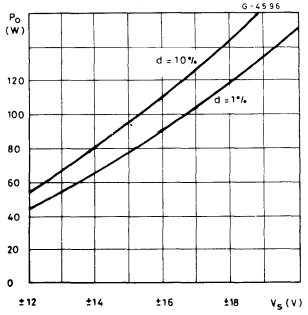
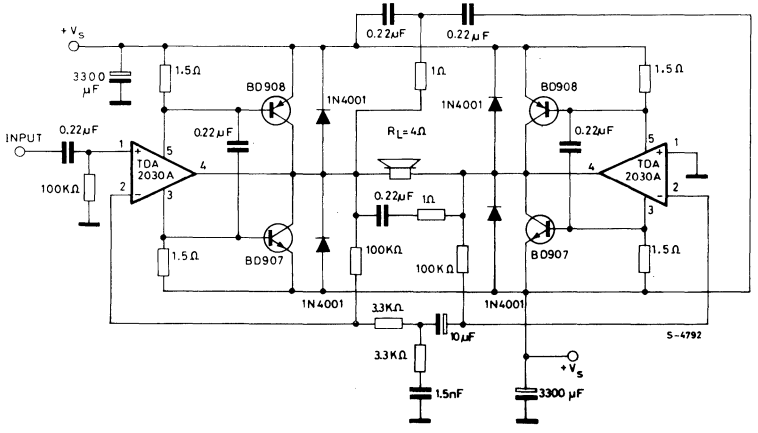


Fig. 24 - 120W "superbridge" power amplifier



Transient intermodulation distortion (TIM)

Transient intermodulation distortion is an unfortunate phenomen associated with negative-feedback amplifiers. When a feedback amplifier receives an input signal which rises very steeply, i.e. it contains high-frequency components, the feedback can arrive too late so that the amplifiers overloads and a burst of intermodulation distortion will be produced as in fig. 25. Since transients occur frequently in music this is obviously a problem for the designer of audio amplifiers. Unfortunately, heavy negative feedback is frequently used to reduce the total harmonic distortion of an amplifier, which tends to aggravate the transient intermodulation (TIM) situation. The best known method for the measurement of TIM consists of feeding sine waves superimposed onto square waves, into the amplifier under test. The output spectrum is then examined using a spectrum analyser and compared to the input. This method suffers from serious disadvantages: the accuracy is limited, the measurement is a rather delicate operation and an expensive spectrum analyser is essential. A new approach (see Technical Note 143) applied by SGS to monolithic amplifiers measurement is fast cheap-it requires nothing more sophisticated than an oscilloscope – and sensitive – and it can be used down to the values as low as 0.002% in high power amplifiers. The "inverting-sawtooth" method of measurement is based on the response of an amplifier to a 20 KHz sawtooth waveform. The amplifier has no difficulty following the slow ramp but it cannot follow the fast edge. The output will follow the upper line in fig. 26 cutting of the shaded area and thus increasing the mean level. If this output signal is filtered to remove the sawtooth, a direct voltage remains which indicates the amount of TIM distortion, although it is difficult to measure because it is indistinguishable from the d.c. offset of the amplifier. This problem is neatly avoided in the IS-TIM method by periodically inverting the sawtooth waveform at a low audio frequency as shown in fig. 27. In the case of the sawtooth in fig. 26 the mean level was increased by the TIM distortion, for a sawtooth in the other direction the opposite is true.

Fig. 25 - Overshoot phenomenon in feedback amplifiers

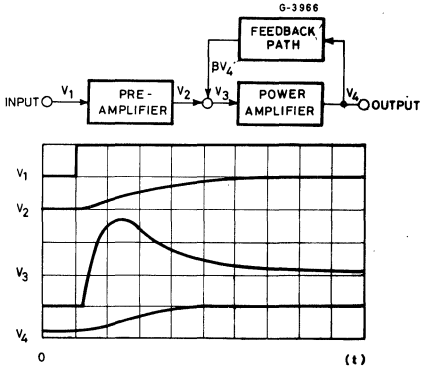


Fig. 26 - 20 KHz sawtooth waveform

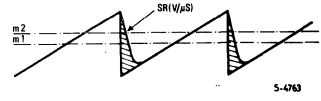
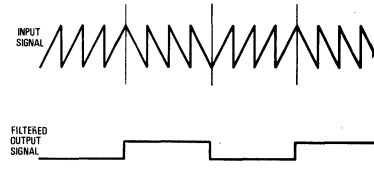


Fig. 27 - Inverting sawtooth waveform



The result is an a.c. signal at the output whose peak-to-peak value is the TIM voltage, which can be measured easily with an oscilloscope.
If the peak-to-peak value of the signal and the peak-to-peak of the inverting sawtooth are measured, the TIM can be found very simply from:

$$TIM = \frac{V_{out}}{V_{sawtooth}} \cdot 100$$

In fig. 28 the experimental results are shown for the 30W amplifier using the TDA2030A as a driver and a low-cost complementary pair.
The measured performances are perfectly suitable for Hi-Fi systems.
A simple RC filter on the input of the amplifier to limit the maximum signal slope (SS) is an effective way to reduce TIM.
The diagram of fig. 29 originated by SGS can be used to find the Slew-Rate (SR) required for a given output power or voltage and a TIM design target.
For example if an anti-TIM filter with a cutoff at 30 KHz is used and the max. peak-to-peak output voltage is 20V then, referring to the diagram, a Slew-Rate of 6V/μS is necessary for 0,1% TIM.
As shown Slew-Rates of above 10V/μS do not contribute to a further reduction in TIM.
Slew-Rates of 100V/μS are not only useless but also a disadvantage in Hi-Fi audio amplifiers because they tend to turn the amplifier into a radio receiver.

Fig. 28 - TIM distortion vs. output power

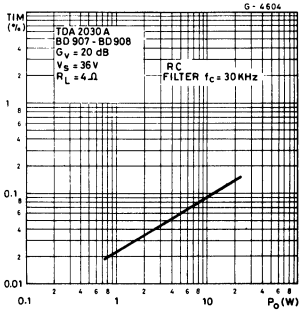
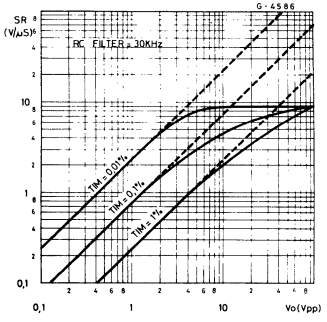


Fig. 29 - TIM design diagram (f_C = 30 KHz)

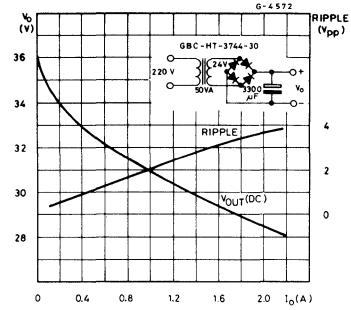


Power supply

Using monolithic audio amplifier with non-regulated supply voltage it is important to design the power supply correctly. In any working case it must provide a supply voltage less than the maximum value fixed by the IC breakdown voltage.
It is essential to take into account all the working conditions, in particular mains fluctuations and supply voltage variations with and without load.
The TDA 2030A ($V_{s\ max}$ = 44V) is particularly suitable for substitution of the standard IC power amplifiers (with $V_{s\ max}$ = 36V) for more reliable applications.
An example, using a simple full-wave rectifier followed by a capacitor filter, is shown in the table and in the diagram of fig. 30.
A regulated supply is not usually used for the power output stages because of its dimensioning must be done taking into account the power to supply in the signal peaks. They are only a small percentage of the total music signal, with consequently large overdimensioning of the circuit.
Even if with a regulated supply higher output power can be obtained (V_s is constant in all working conditions), the additional cost and power dissipation do not usually justify its use. Using non-regulated supplies, there are fewer design restriction. In fact, when signal peaks are present, the capacitor filter acts as a flywheel supplying the required energy.
In average conditions, the continuous power supplied is lower. The music power/continuous power ratio is greater in this case than for the case of regulated supplied, with space saving and cost reduction.

Mains (220V)	Secondary voltage	DC output voltage (V_O)		
		I_O= 0	I_O= 0.1A	I_O= 1A
+20%	28.8V	43.2V	42V	37.5V
+15%	27.6V	41.4V	40.3V	35.8V
+10%	26.4V	39.6V	38.5V	34.2V
—	24V	36.2V	35V	31V
-10%	21.6V	32.4V	31.5V	27.8V
-15%	20.4V	30.6V	29.8V	26V
-20%	19.2V	28.8V	28V	24.3V

Fig. 30 - DC characteristics of 50W non-regulated supply



SHORT CIRCUIT PROTECTION

The TDA 2030A has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. The TDA 2030A is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

LINEAR INTEGRATED CIRCUIT

TDA2040

22W Hi-Fi AUDIO POWER AMPLIFIER

The TDA 2040 is a monolithic integrated circuit in Pentawatt® package, intended for use as an audio class AB amplifier. Typically it provides 22W output power (d = 0.5%) at V_s = 32V/4Ω. The TDA 2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.

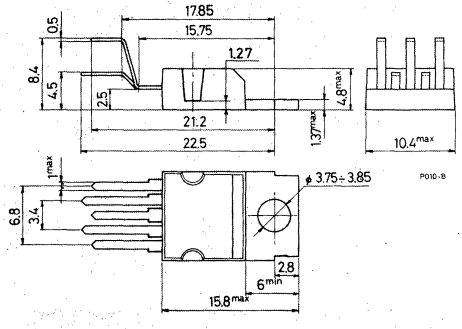
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 20	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o.	Output peak current (internally limited)	4	A
P_{tot}	Power dissipation at T_{case} = 75°C	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

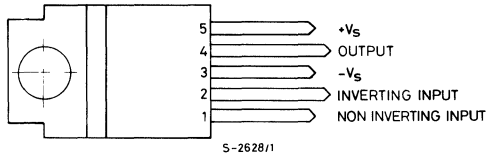
ORDERING NUMBER: TDA 2040V

MECHANICAL DATA

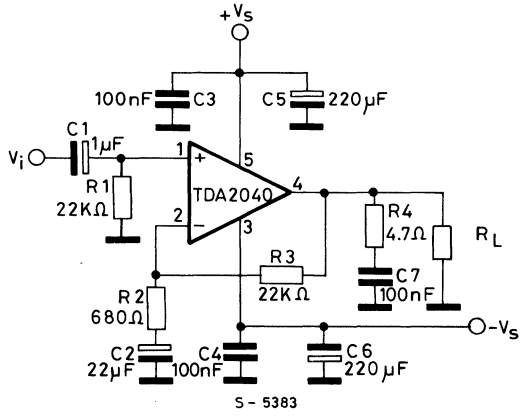
Dimensions in mm



CONNECTION DIAGRAM
(top view)



TEST CIRCUIT



THERMAL DATA

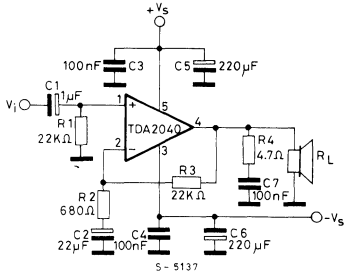
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 16V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 2.5			V
I_d	Quiescent drain current	$V_s = \pm 4.5V$			30	mA
				45	100	mA
I_b	Input bias current			0.3	1	μA
V_{os}	Input offset voltage			± 2	± 20	mV
I_{os}	Input offset current				±200	nA
P_o	Output power	d = 0.5% $T_{case} = 60°C$ f = 1 KHz $R_L = 4\Omega$ $R_L = 8\Omega$	20	22 12		W
		f = 15 KHz $R_L = 4\Omega$	15	18		W
BW	Power bandwidth	$P_o = 1W$ $R_L = 4\Omega$		100		KHz
G_v	Open loop voltage gain	f = 1 KHz		80		dB
G_v	Closed loop voltage gain		29.5	30	30.5	dB
d	Total harmonic distortion	$P_o = 0.1$ to 10W $R_L = 4\Omega$ f = 40 to 15000Hz f = 1 KHz		0.08 0.03		%
e_N	Input noise voltage	B = curve A		2		μV
		B = 22 Hz to 22 KHz		3		
i_N	Input noise current	B = curve A		50		pA
		B = 22 Hz to 22 KHz		80		
R_i	Input resistance (pin 1)		0.5	5		MΩ
SVR	Supply voltage rejection	$R_L = 4\Omega$ $G_v = 30$ dB $R_g = 22$ KΩ f = 100 Hz $V_{ripple} = 0.5\ V_{rms}$	40	48		dB
η	Efficiency	f = 1 KHz $P_o = 12W$ $R_L = 8\Omega$ $P_o = 22W$ $R_L = 4\Omega$		66 63		%
T_j	Thermal shut-down junction temperature			145		°C

APPLICATION INFORMATION

Fig. 1 - Amplifier with split power supply (*)



$V_s = \pm 16V$
$R_L = 4\Omega$
$P_o \geqslant 15W$ (d = 0.5%)

Fig. 2 - P.C. board and components layout of the circuit of fig. 1.

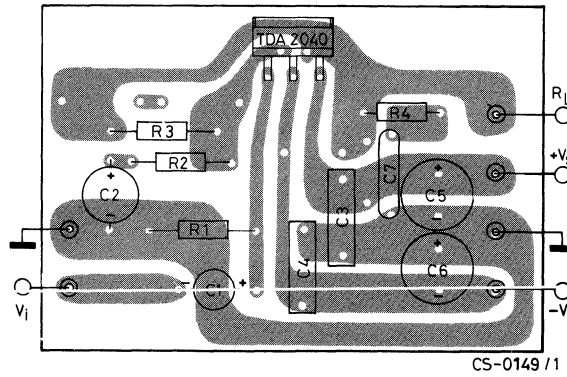
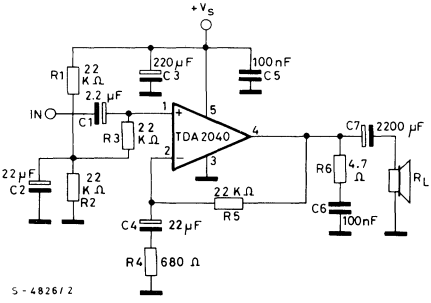
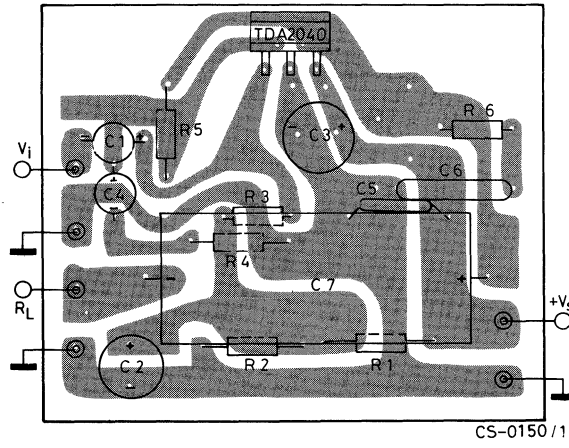


Fig. 3 - Amplifier with single supply (*)



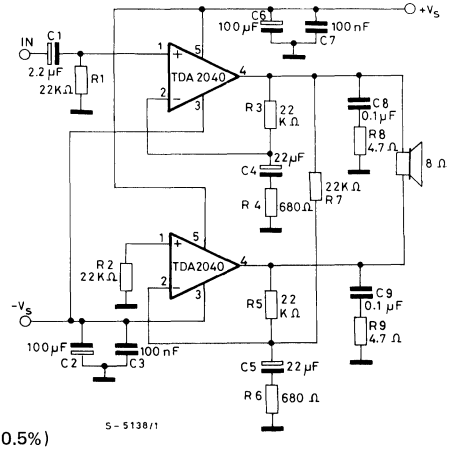
* In the case of highly inductive loads protection diodes may be necessary.

Fig. 4 - P.C. board and components layout of the circuit of fig. 3.



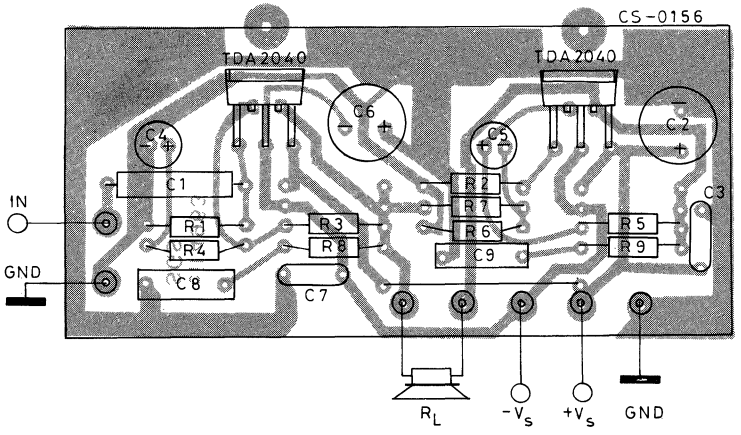
APPLICATION INFORMATION (continued)

Fig. 5 - 30W Bridge amplifier with split power supply



$V_s = \pm 16V$
$R_L = 8\Omega$
$P_o \geqslant 30W$ (d = 0.5%)

Fig. 6 - P.C. board and components layout for the circuit of fig. 5.



APPLICATION INFORMATION (continued)

Multiway speaker systems and active boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each lodspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two, three or four bands.
To maintain a flat frequency response over the HiFi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see fig. 7). As an example, a 100 W three-way system with crossover frequencies of 400 Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.
Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:
- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance

Fig. 7 - Power distribution vs. frequency

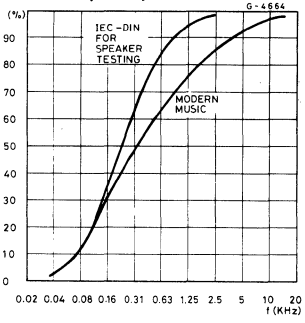
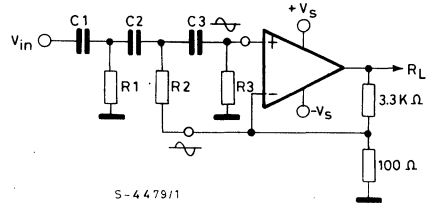


Fig. 8 - Active power filter



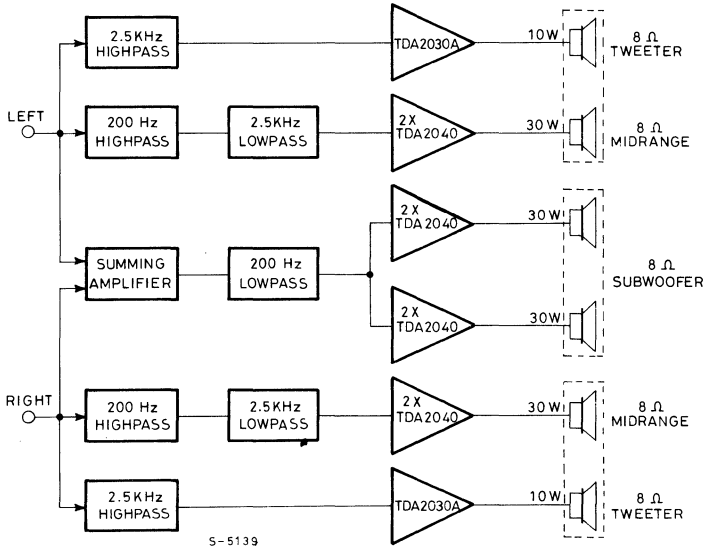
Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit.
This makes it particularly interesting and economically sound to use monolithic power amplifiers.
In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6 dB/octave) can be recommended.
The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.
The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.
A more effective solution, named "Active Power Filter" by SGS is shown in fig. 8.
The proposed circuit can realize combined power amplifiers and 12 dB/octave or 18 dB/octave high-pass or low-pass filters.
In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (—) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for f_c = 900 Hz using a Bessel 3rd order Sallen and Key structure are:

C1 = C2 = C3	R1	R2	R3
22 nF	8.2 KΩ	5.6 KΩ	33 KΩ

In the block diagram of fig. 9 is represented an active loudspeaker system completely realized using power integrated circuits, rather than the traditional discrete transistors or hybrids, very high quality is obtained by driving the audio spectrum into three bands using active crossovers (TDA 2320A) and a separate amplifier and loudspeaker for each band.
A modern subwoofer/midrange/tweeter solution is used.

Fig. 9 - High power active loudspeaker system using TDA 2030A and TDA 2040



TDA2054M

LINEAR INTEGRATED CIRCUIT

PREAMPLIFIER WITH ALC FOR C_rO_2 CASSETTE RECORDERS

- EXCELLENT VERSATILITY IN USE (V_S from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- STEREO MATCHING BETTER THAN 3 dB (matched pair)

The TDA 2054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package.
The functions incorporated are:

– low noise preamplifier
– automatic level control system (ALC)
– high gain equalization amplifier

It is intended as preamplifier in tape and cassette recorders and players (C_rO_2), dictaphones, compressor and expander in telephonic equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

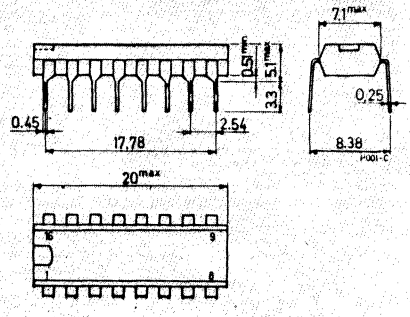
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 50°C	500	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

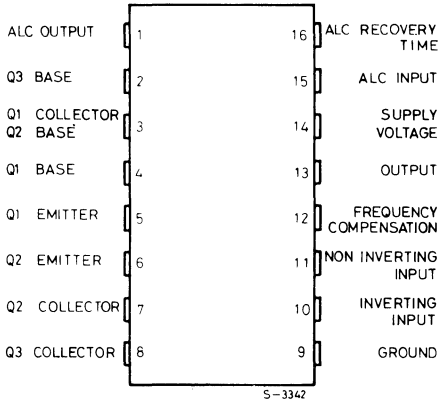
ORDERING NUMBERS: TDA 2054M mono applications
2 TDA 2054M stereo applications

MECHANICAL DATA

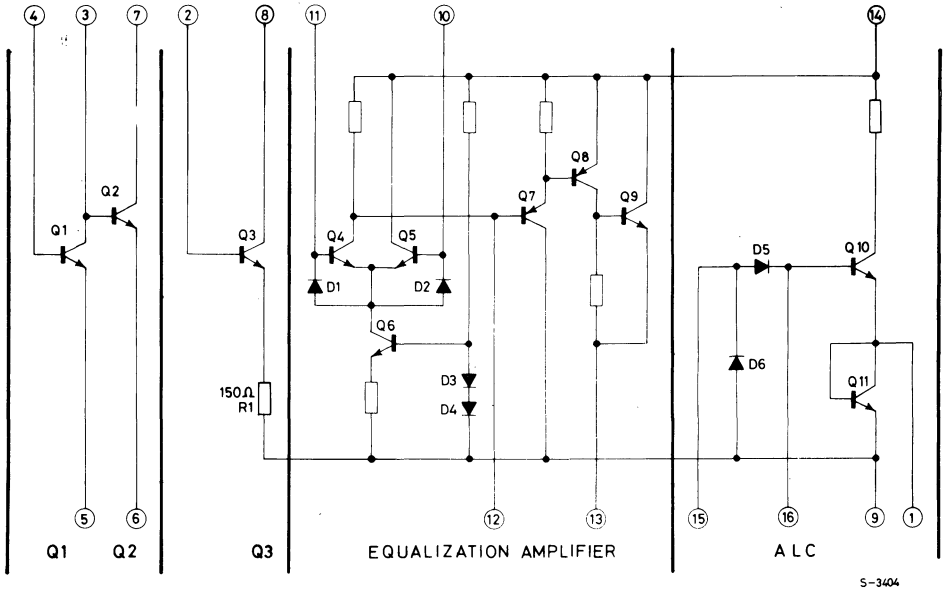
Dimensions in mm



CONNECTION DIAGRAM

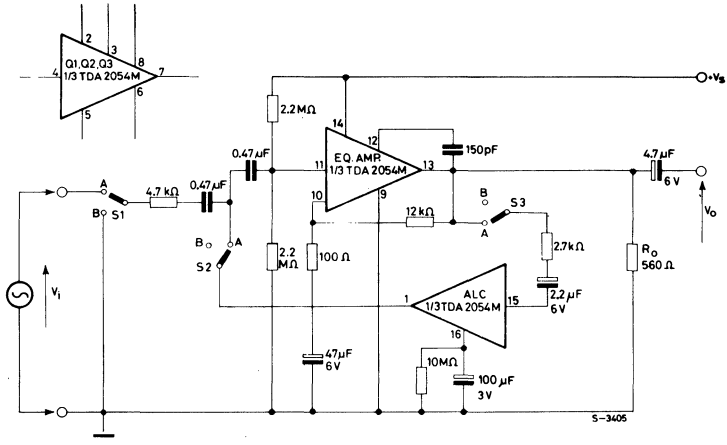


SCHEMATIC DIAGRAM



TDA2054M

TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, T_{amb}= 25°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_d	Quiescent drain current	V_s = 9V S1 = S2 = S3 = at B		10		mA
h_{FE}	DC current gain (Q1, Q2, Q3)	I_c = 0.1 mA V_{CE}= 5V	300	500		—
e_N	Input noise voltage (Q1, Q2, Q3)	I_c = 0.1 mA V_{CE}= 5V f = 1 KHz		2		$\frac{nV}{\sqrt{Hz}}$
i_N	Input noise current (Q1, Q2, Q3)			0.5		$\frac{pA}{\sqrt{Hz}}$
NF	Noise figure (Q1, Q2, Q3)	I_c = 0.1 mA V_{CE}= 5V R_g = 4.7 KΩ B (-3 dB)= 20 to 10000 Hz		0.5	4	dB
G_v	Open loop voltage gain(for equalization amplifier)	V_s = 9V f = 1 KHz		60		dB
V_o	Output voltage with A.L.C.	V_s = 9V V_i = 100 mV f = 1 KHz S1= S2= S3 at A		0.6		V
e_N	Equivalent input noise voltage (for equalization amplifier pin 11)	V_s = 9V G_v = 40 dB S1 at B B (-3 dB)= 20 to 20000 Hz		1.3		μV
R_1	Q3 emitter resistance		105	150	195	Ω

Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (transistors Q1, Q2, Q3)

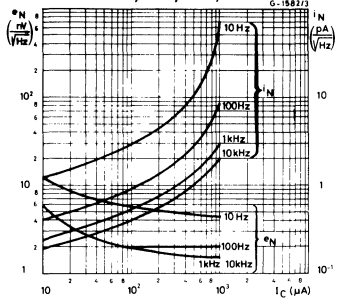


Fig. 2 - Equivalent input noise current vs. frequency (transistors Q1, Q2, Q3)

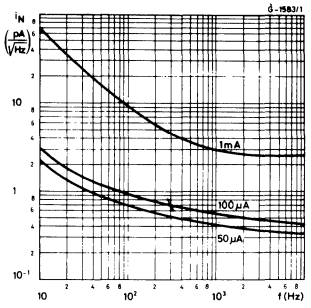


Fig. 3 - Equivalent input noise voltage vs. frequency (transistors Q1, Q2, Q3)

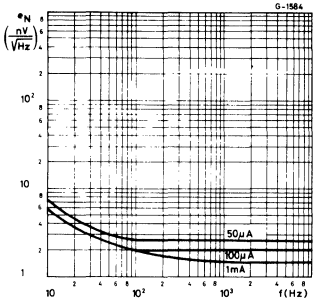


Fig. 4 - Noise figure vs. bias current (transistors Q1, Q2, Q3)

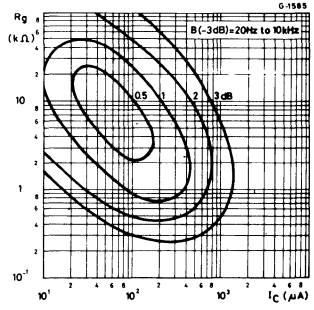


Fig. 5 - Optimum source resistance and minimum NF vs. bias current (transistors Q1, Q2, Q3)

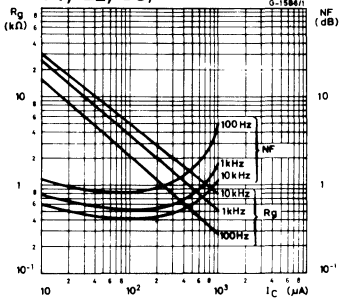


Fig. 6 - Current gain vs. collector current (transistors Q1, Q2, Q3)

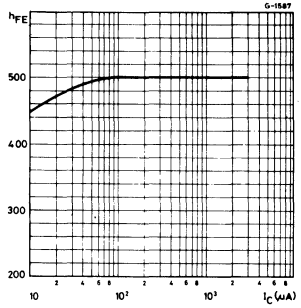


Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

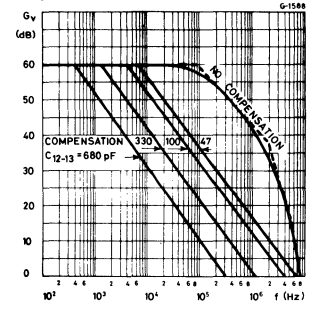


Fig. 8 - Open loop phase response vs. frequency(equalization amplifier)

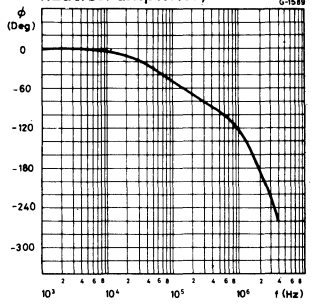
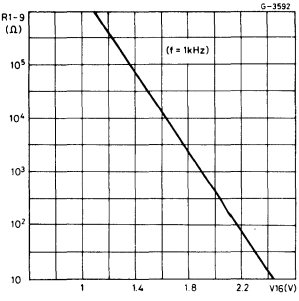


Fig. 9 - Dinamic resistance R_{1-9} vs. ALC voltage V_{16}



APPLICATION INFORMATION

Fig. 9 - Application circuit for C_rO_2 cassette player and recorder

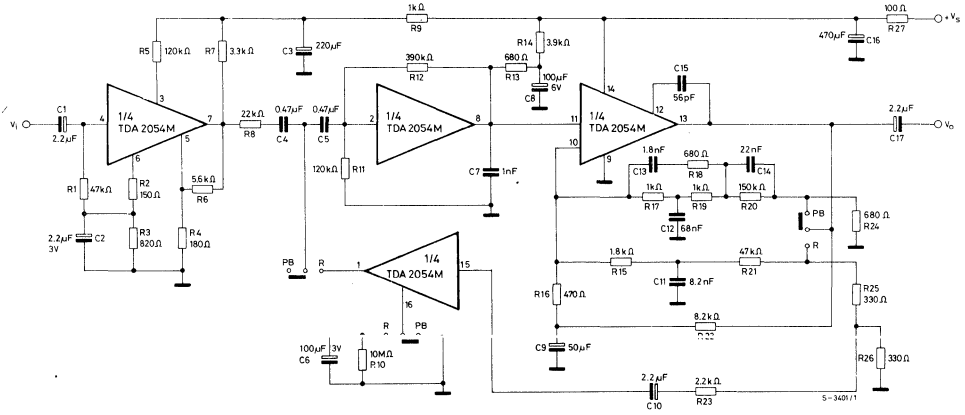
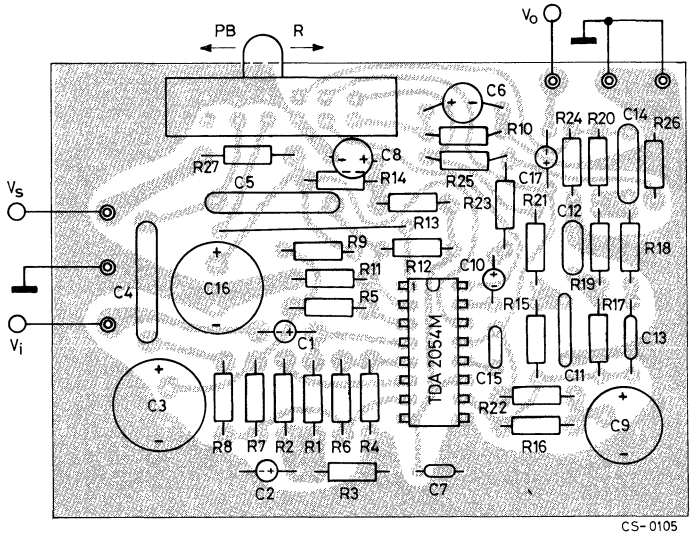


Fig. 10 - P.C. board and component layout for the circuit of Fig. 9 (1:1 scale)



TYPICAL PERFORMANCE OF CIRCUIT IN FIG. 9 (T_{amb} = 25°C, V_s = 9V)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
PLAYBACK						
G_v	Voltage gain (open loop)	f = 20 to 20000 Hz		134		dB
G_v	Voltage gain (closed loop)	f = 1 KHz		60		dB
Z_i	Input impedance	f = 100 Hz f = 1 KHz f = 10 KHz		10 41 43		KΩ KΩ KΩ
Z_o	Output impedance	f = 1 KHz		12	35	Ω
B	Frequency response			see fig. 11		
d	Distortion	V_o = 1V f = 1 KHz		0.2		%
	Output background noise	Z_g = 300Ω + 120 mH (DIN 45405)		1.5		mV
***	Output weighted background noise			1		mV
$\frac{S+N}{N}$	Signal to noise ratio	V_o = 1.5V Z_g = 300Ω + 120 mH		60		dB
t_{on}*	Switch-on time	V_o = 1V		500		ms
RECORDING						
G_v	Voltage gain (open loop)	f = 20 to 20000 Hz		134		dB
G_v	Voltage gain (closed loop)	f = 1 KHz		72		dB
B	Frequency response			see fig. 13		
d	Distortion with ALC	V_o = 1V f = 10 KHz		0.5		%
ALC	Automatic level control range(for 3 dB of output voltage variation)	$V_i \leqslant$ 40 mV f = 10 KHz		54		dB
V_o	Output voltage before clipping without ALC	f = 1 KHz		3		V
V_o	Output voltage with ALC	V_i = 30 mV f = 1 KHz		1.1		V
t_l*	Limiting time (see fig. 17)	ΔV_i = +40 dB f = 1 KHz		75		ms
t_{set}*	Level setting time (see fig. 17)			300		ms
t_{rec}*	Recovery time (see fig. 17)	ΔV_i = -40 dB f = 1 KHz		150		sec.
t_{on}*	Switch-on-time	V_o = 1V		500		ms
$\frac{S+N}{N}$***	Signal to noise ratio with ALC	V_o = 1V R_g = 470Ω		64		dB

* This value depends on external network.

** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 15 KHz can be avoided - so halving the output noise.

*** Weighted noise measurement (DIN 45405).

Fig. 11 - Frequency response for the circuit in fig. 9 (playback)

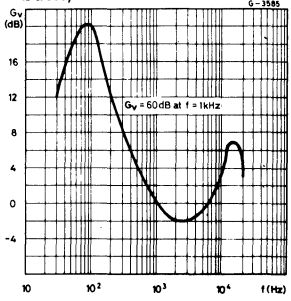


Fig. 12 - Distortion vs. frequency for the circuit in fig. 9 (playback)

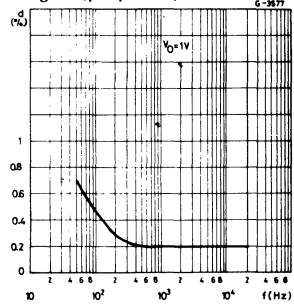


Fig. 13 - Frequency response for the circuit in fig. 9 (recording)

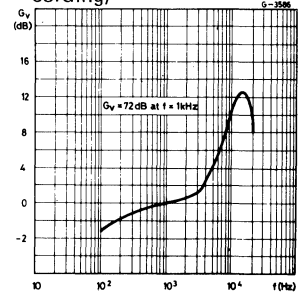


Fig. 14 - Output voltage variation and distortion with ALC vs. input voltage for the circuit in fig. 9 (recording)

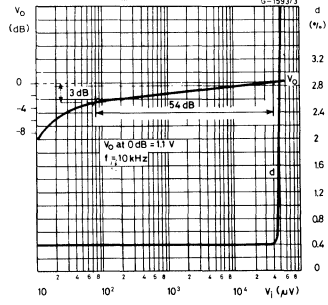


Fig. 15 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

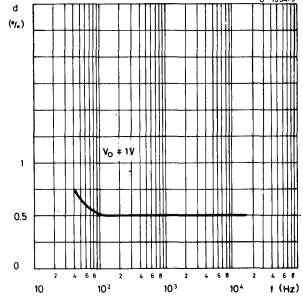


Fig. 16 - Limiting and level setting time vs. input signal variation

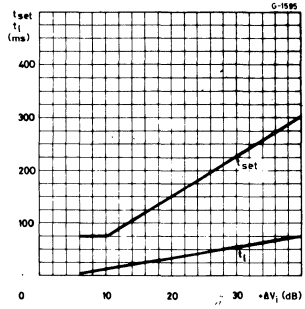
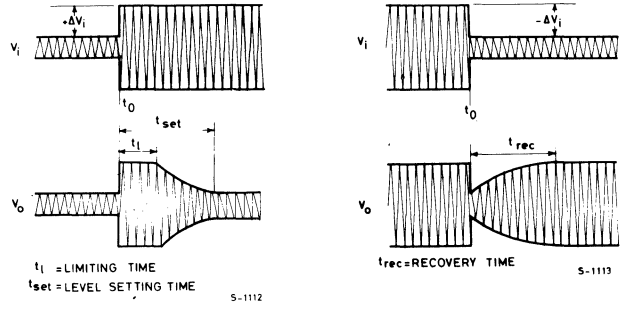


Fig. 17 - Limiting, level setting, recovery time



LINEAR INTEGRATED CIRCUIT

TDA2170

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

The TDA 2170 is a monolithic integrated circuit in 11-lead Multiwatt® package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Colour and B & W television receivers as well as in monitors and displays. The functions incorporated are:

- power amplifier
- flyback generator
- reference voltage
- thermal protection

PRELIMINARY DATA

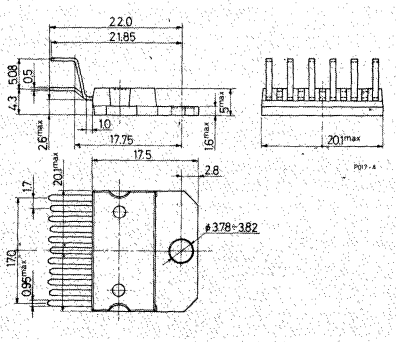
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 4)	35	V
V_7, V_8	Flyback peak voltage	60	V
V_5	Voltage at pin 5	$+ V_s$	
V_2, V_3	Amplifier input voltage	$+ V_s$	
I_o	Output peak current (non repetitive, t = 2 msec)	-0.5 2.5	V A
I_o	Output peak current at f = 50 or 60 Hz, $t \leq 10$ μsec	3	A
I_o	Output peak current at f = 50 or 60 Hz, $t > 10$ μsec	2	A
I_5	Pin 5 DC current at $V_7 < V_4$	100	mA
I_5	Pin 5 peak to peak flyback current at f = 50 or 60 Hz, $t_{fly} \leq 1.5$ msec	3	A
P_{tot}	Total power dissipation at $T_{case} = 60°C$	30	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

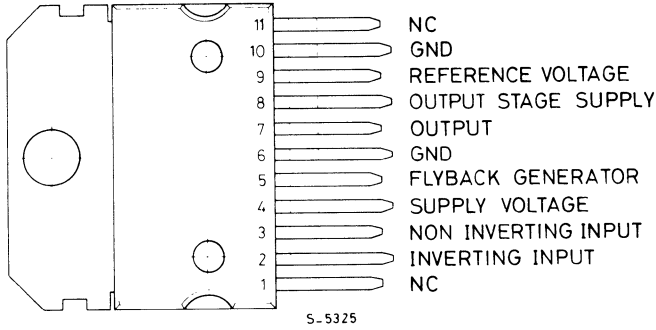
ORDERING NUMBER: TDA 2170

MECHANICAL DATA

Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM

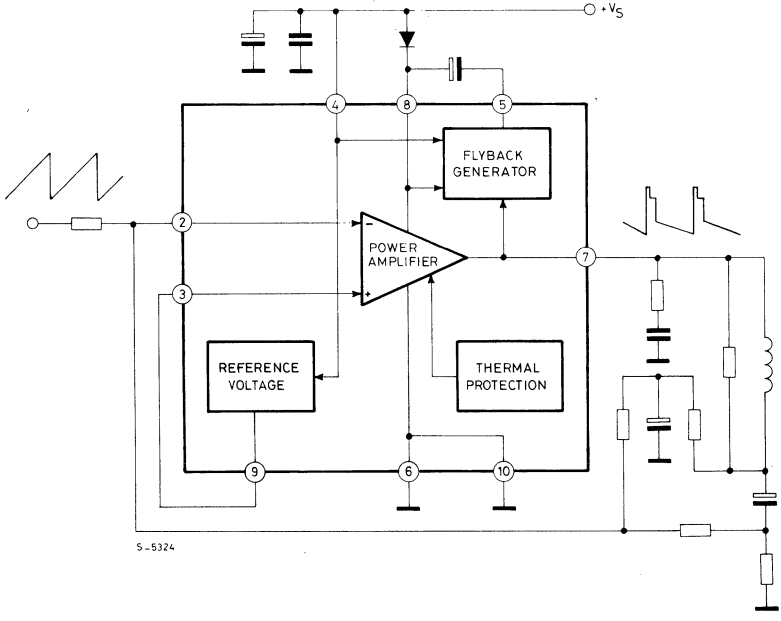


Fig. 1 - DC test circuits

Fig. 1a - Measurement of I_2; I_3; I_4; I_8; V_9; $\Delta V_9/\Delta V_s$; R9

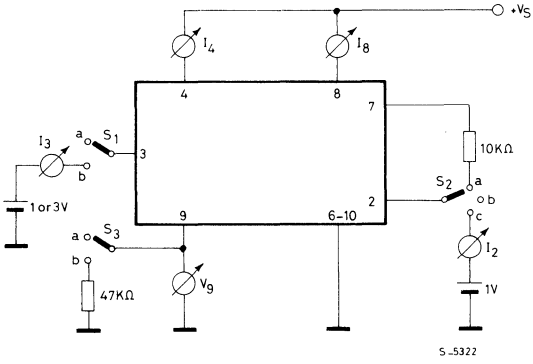
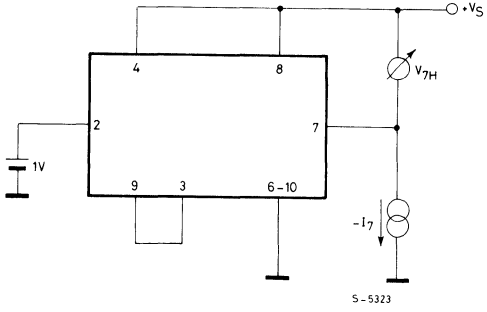


Fig. 1b - Measurement of $V7_H$



S_1 : (a) I_2; (b) I_3, I_4 and I_8.
S_2 : (a) I_4 and I_8; (b) I_3; (c) I_2.
S_3 : (a) I_2, I_3, I_4, I_8, I_9 and V_9; (b) R9.

Fig. 1c - Measurement of V_{5L}; V_{7L}

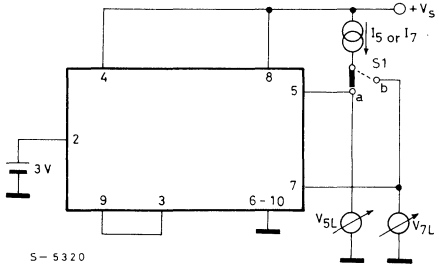
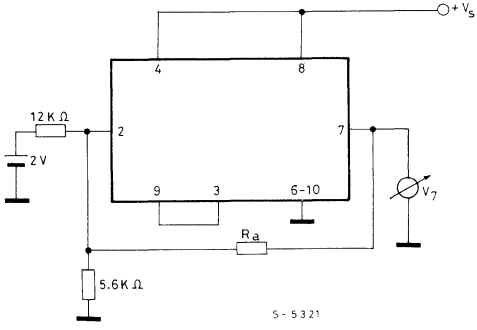


Fig. 1d - Measurement of V_7



S1 : (a) V_{5L}; (b) V_{7L}.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	40	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 35V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_4	Pin 4 quiescent current	$I_5 = 0$; $I_7 = 0$; $V_3 = 3V$		8		mA	1a
I_8	Pin 8 quiescent current	$I_5 = 0$; $I_7 = 0$; $V_3 = 3V$		18		mA	1a
I_3	Amplifier input bias current	$V_3 = 1V$		-0.1	-1	μA	1a
I_2	Amplifier input bias current	$V_2 = 1V$		-0.1	-1	μA	1a
V_9	Reference voltage	$I_9 = 0$		2.2		V	1a
$\frac{\Delta V_9}{\Delta V_s}$	Reference voltage drift vs. supply voltage	V_s = 15 to 30V		0.5		mV/V	1a
V_{5L}	Pin 5 saturation voltage to GND	I_5 = 20 mA		0.5		V	1c
V_7	Quiescent output voltage	V_s = 35V; R_a = 39 KΩ		18		V	1d
		V_s = 15V; R_a = 13 KΩ		7.5		V	1d
V_{7L}	Output saturation voltage to GND	I_7 = 1.2A		1		V	1c
		I_7 = 0.7A		0.6		V	1c
V_{7H}	Output saturation voltage to supply	$-I_7$ = 1.2A		1.6		V	1b
		$-I_7$ = 0.7A		1.2		V	1b
R9	Reference voltage output resistance			2.1		KΩ	
T_j	Junction temperature for thermal shut down			140		°C	

Fig. 2 - AC test circuit

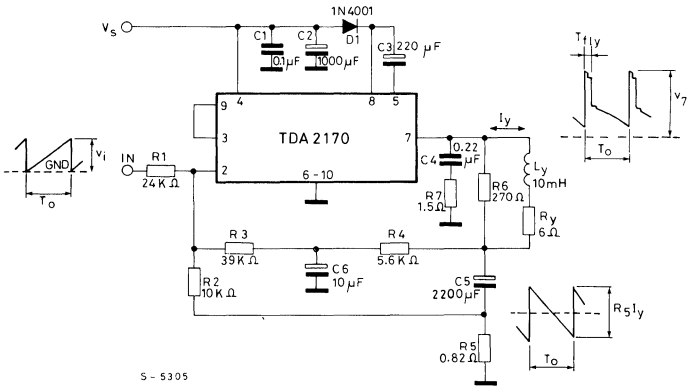
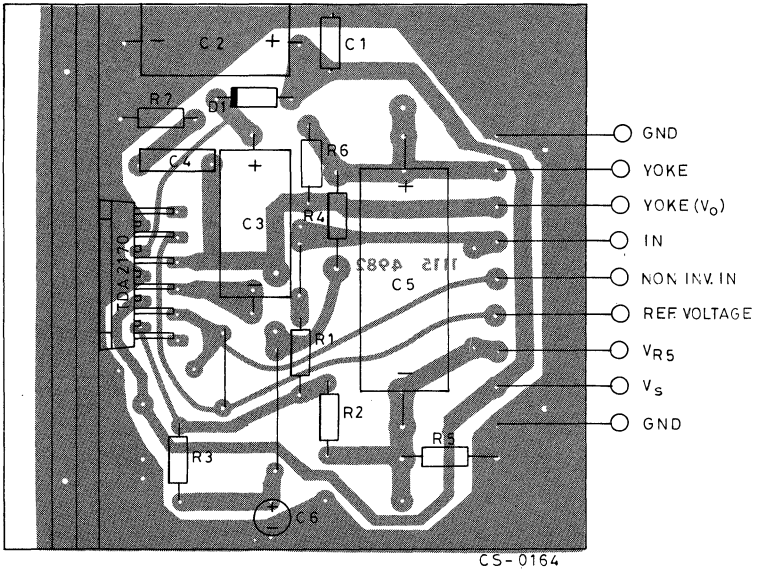


Fig. 3 - PC board and component layout (1:1 scale)



Components list for typical applications

Component	110° TVC 5.9Ω/10 mH 1.95 App	110° TVC 9.6Ω/27 mH 1.17 App	90° TVC 15Ω/30 mH 0.82 App	Unit
R1	24	18	12	KΩ
R2	10	6.8	5.6	KΩ
R3	39	22	22	KΩ
R4	5.6	5.6	5.6	KΩ
R5	0.82	1.2	2.2	Ω
R6	270	330	330	Ω
R7	1.5	1.5	1.5	Ω
D1	1N 4001	1N 4001	1N 4001	–
C1	0.1	0.1	0.1	μF
C2 el.	1000/25V	470/25V	470/25V	μF
C3 el.	220/25V	220/25V	220/25V	μF
C4	0.22	0.22	0.22	μF
C5 el.	2200/25V	1500/25V	1000/16V	μF
C6 el.	10/16V	10/16V	10/16V	μF

Typical performances

Parameter	110° TVC 5.9Ω/10 mH	110° TVC 9.6Ω/27 mH	90° TVC 15Ω/30 mH	Unit
V_s – Supply voltage	24	22.5	25	V
I_s – Current	280	175	125	mA
t_{fly} – Flyback time	0.6	1	0.7	ms
P_{tot} – Power dissip.	4.2	2.5	2.05	W
$R_{th\ c-a}$ – Heatsink	7	13	16	°C/W
T_{amb}	60	60	60	°C
$T_{j\ max.}$	110	110	110	°C
T_o	20	20	20	ms
v_i	4	4	4	Vpp
v_7	50	47	52	Vp

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 4 – Mounting examples

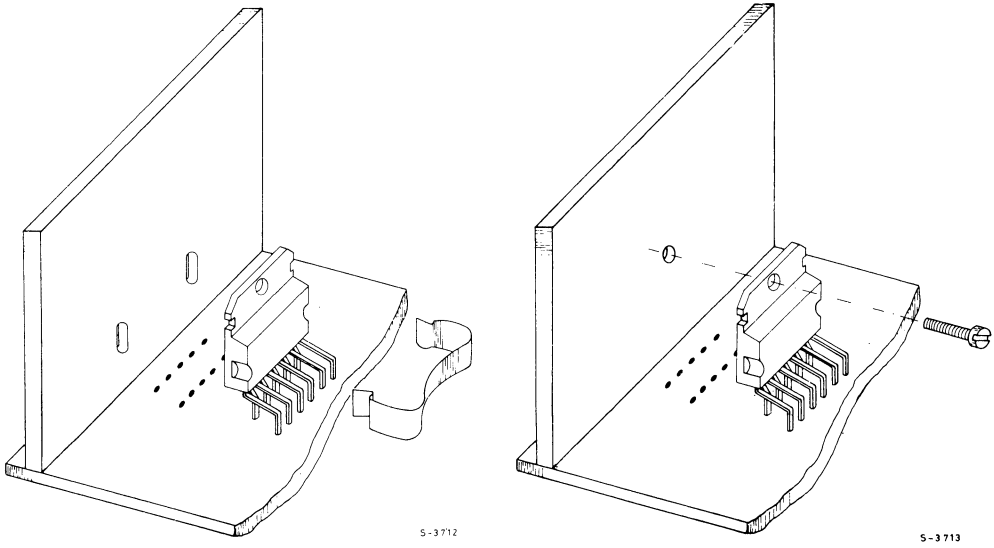
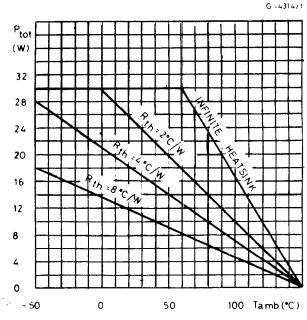


Fig. 5 – Maximum allowable power dissipation vs. ambient temperature



TDA2190

LINEAR INTEGRATED CIRCUIT

COMPLETE TV SOUND CHANNEL WITH V.C.R. AND C.C.C.

The TDA 2190 is a monolithic integrated circuit in 16-lead dual in-line power dip. It performs the following functions:

- IF limiter-amplifier and low-pass filter.
- FM detector.
- DC volume control.
- AF preamplifier and AF power amplifier with thermal shut-down protection and choice of class B or C.C.C. operation mode
- VCR facility with common pin for input and output (playback and recording).
- VCR input and FM Detector DC switching for recording and playback.

The main features of TDA 2190 are:

- Suitable for all TV standards with FM modulation.
- Class B or constant current consumption (C.C.C.) operation mode.
- Video cassette recorder (VCR) facility according to DIN norms.
- DC or AC volume control.
- Physiological volume and tone controls (AC volume control mode).
- LC or ceramic filters can be used for input and detector networks.
- High output power (10W) easily achieved by very simple external stage.

Performance

- Very low spread of DC volume control.
- DC volume control thermally compensated.
- Very low current ripple in C.C.C. operation mode.
- 4W output power.
- No radiation problem

Safety

- Thermal protection of AF output stage.
- Short-circuit protection of VCR input-output pin.

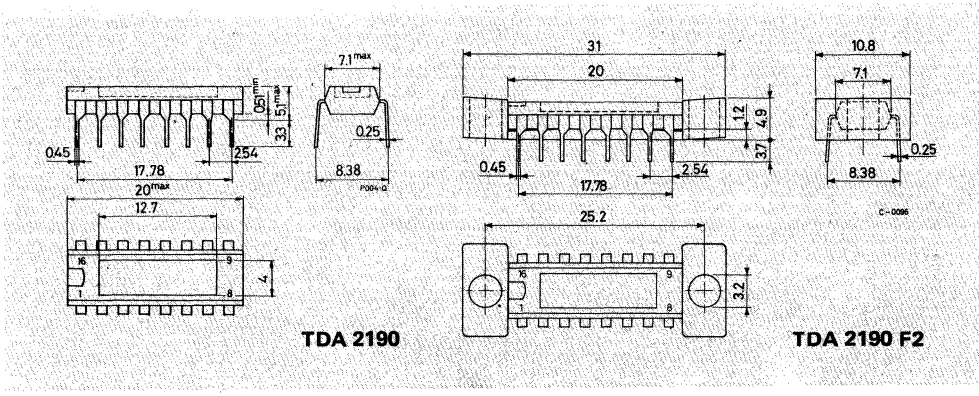
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pins 14 and 15)	28	V
V_i	Input peak voltage (pin 10)	1	V
V_3	Voltage at pin 3	V_S	V
I_o	Output peak current (non repetitive)	2	A
I_o	Output peak current (repetitive)	1.5	A
P_{tot}	Power dissipation at T_{case}= 75°C	15	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

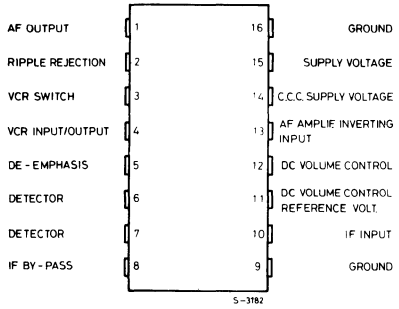
ORDERING NUMBERS: TDA 2190
TDA 2190 F2

MECHANICAL DATA

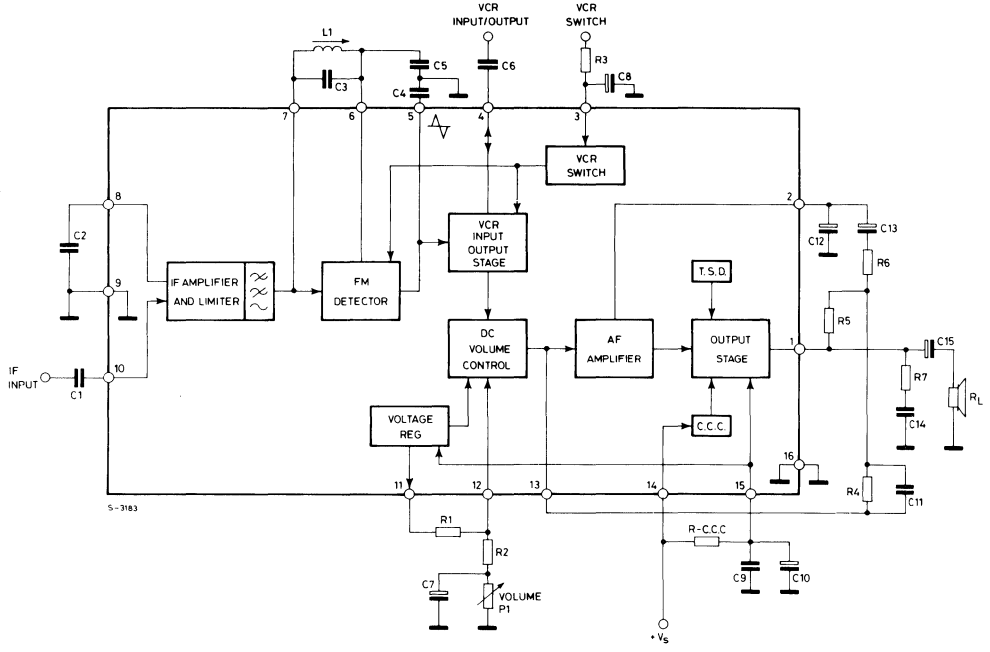
Dimensions in mm



CONNECTION DIAGRAM



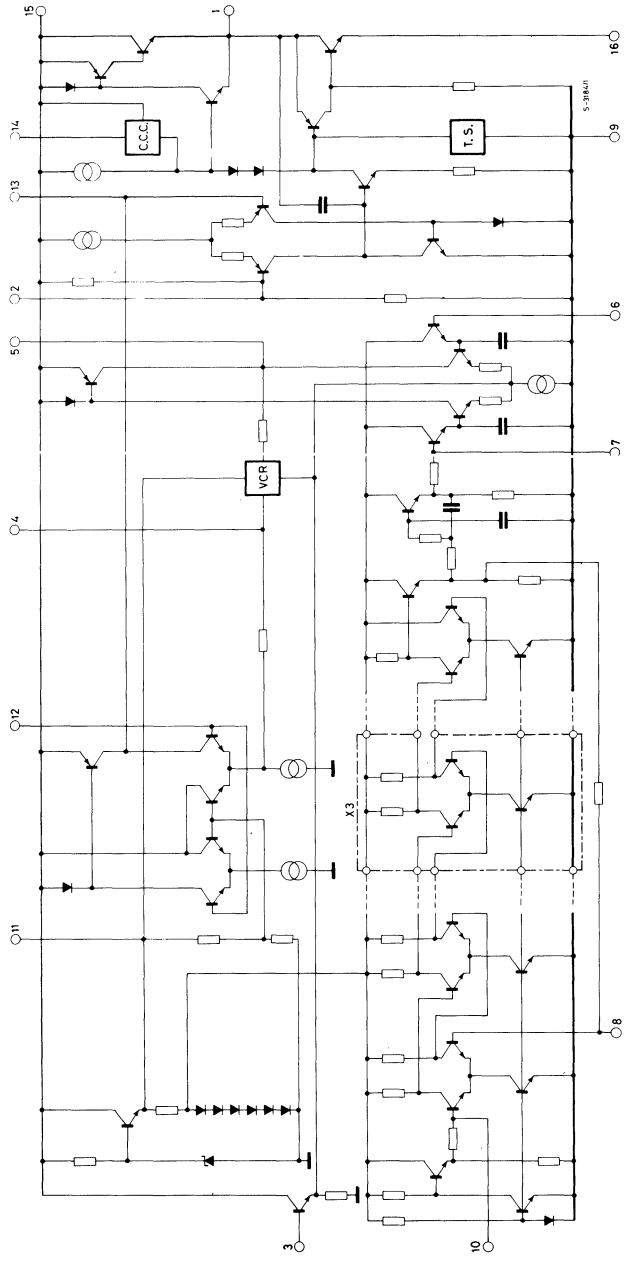
BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	5	°C/W

SCHEMATIC DIAGRAM



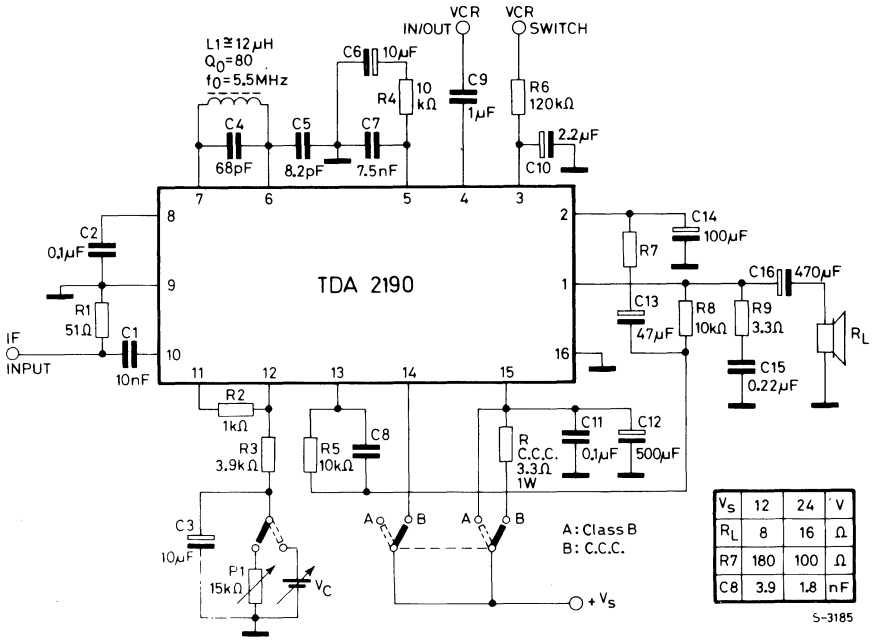
ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = 24V$, $f_o = 5.5MHz$, $f_m = 1KHz$, class B, $T_{amb} = 25°C$, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
V_s	Supply voltage (pins 14 and 15)			11		28	V
V_o	Quiescent output voltage (pin 1)	$V_s = 24V$	$P_1 = 0$	11	12	13	V
		$V_s = 12V$	$P_1 = 0$	5.1	6	6.9	
V_4	Pin 4 DC voltage	Playback and recording		5	6	7	V
V_{11}	DC volume control reference voltage	$P_1 = 0$ to 5 KΩ		4	4.7	5.5	V
V_{14-15}	C.C.C. reference voltage (between pins 14 and 15)			0.9	1.1	1.3	V
I_d	Quiescent drain current	$V_s = 24V$	$P_1 = 0$	25	45	65	mA
		$V_s = 12V$	$P_1 = 0$	20	35	50	
IF AMPLIFIER AND DETECTOR							
$V_{i\ (threshold)}$	Input limiting voltage at pin 10	$P_1 = 0$	$\Delta f = \pm 25$ KHz		40	100	μV
V_5	Recovered audio voltage	$V_i \geq 1$ mV, $P_1 = 0$	$\Delta f = \pm 25$ KHz	240	400	480	mV
AMR	Amplitude modulation rejection	$V_i = 1$ mV, $m = 0.3$	$\Delta f = \pm 50$ KHz		62		dB
R_i	Input resistance (pin 10)	$V_i = 1$ mV			10		KΩ
C_i	Input capacitance (pin 10)	$V_i = 1$ mV			5		pF
DC VOLUME CONTROL							
A	Volume attenuation (resistance control)	$P_1 = 0\Omega$		80	90		dB
		$P_1 = 2.3$ KΩ		22	30	38	dB
		$P_1 = 5$ KΩ			0	3	dB
V_C	Control voltage	A = 90 dB			0		V
		A = 30 dB			1.5		V
		A = 0 dB			3		V
$\frac{\Delta A}{\Delta T_{tab}}$	Volume attenuation thermal drift (resistance control)	$T_{tab} = 25$ to 85°C, $P_1 = 2.3$ KΩ			-0.05		$\frac{dB}{°C}$
AUDIO FREQUENCY AMPLIFIER							
P_o	Output power in class B mode	d = 10%					
		$V_s = 24V$	$R_L = 16\Omega$		4.1		W
		$V_s = 12V$	$R_L = 8\Omega$		1.5		W
		d = 2%					
		$V_s = 24V$	$R_L = 16\Omega$		3		W
		$V_s = 12V$	$R_L = 8\Omega$		1.2		W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AUDIO FREQUENCY AMPLIFIER (continued)						
P_o	Output power in C.C.C. mode	d = 10% V_s = 24V R_L = 16Ω V_s = 12V R_L = 8Ω		3.5 1.2		W W
B	Frequency response of audio amplifier (-3 dB)	P_o = 1W R_L = 16Ω		50 ÷ 10000		Hz
SVR	Supply voltage rejection ratio	P_1 = 0 V_i = 1 mV Δf = 0 R_L = 16Ω f_{ripple} = 100 Hz		50		dB
V.C.R.						
V_3	Input switching voltage for recording				2	V
V_3	Input switching voltage for playback		8.5			V
R_3	Input resistance	V_3 = 1 to 10V	50	100		KΩ
V_{4i}	Input voltage (playback)	$V_3 \geq$ 8.5V P_{out} = 1W P_1 = 5 KΩ	45	90	180	mV
V_{4out}	Output voltage (recording)	$V_3 \leq$ 2V V_i = 1 mV P_1 = 0 Δf = ± 25 KHz	240	400	480	mV
R_{4i}	Input resistance (playback)	$V_3 \geq$ 8.5V	10	13		KΩ
R_{4out}	Output resistance (recording)	$V_3 \leq$ 2V		140		Ω
d	Total harmonic distortion of pin 4 output signal	P_1 = 0 V_i = 1 mV Δf = ± 25 KHz $V_3 \leq$ 2V		0.5		%
SVR	Supply voltage rejection at output pin 4	P_1 = 0 $V_3 \leq$ 2V $V_i \geq$ 1 mV Δf = 0 f_{ripple} = 100 Hz		50		dB
$\frac{S+N}{N}$	Signal and noise to noise ratio (pin 4)	$V_3 \leq$ 2V $V_i \geq$ 1 mV Δf = ± 50 KHz	50	67		dB
OVERALL CIRCUIT						
$\frac{S+N}{N}$	Signal and noise to noise ratio	$V_i \geq$ 1 mV V_o = 4V Δf = ± 50 KHz	50	67		dB
d	Distortion	P_o = 50 mW Δf = ± 25 KHz V_s = 24V R_L = 16Ω V_s = 12V R_L = 8Ω		 0.5 0.5		 % %

TEST CIRCUIT



V_S	12	24	V
R_L	8	16	Ω
R7	180	100	Ω
C8	3.9	1.8	nF

Fig. 1 - Relative audio output and signal to noise ratio vs. input signal

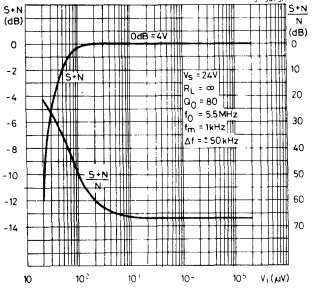


Fig. 2 - AM rejection vs. input signal

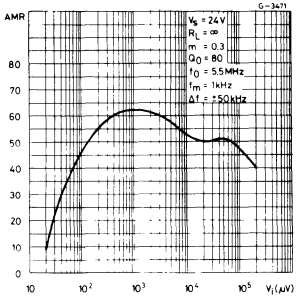


Fig. 3 - ΔAM rejection vs. tuning frequency change

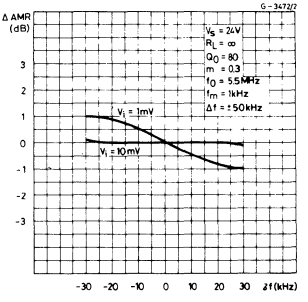


Fig. 4 - Detected audio voltage (pin 5) vs. unloaded Q-factor of the detector coil

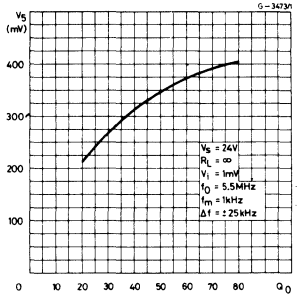


Fig. 5 - Distortion of the detected signal (pin 5) vs. unloaded Q-factor of the detector coil

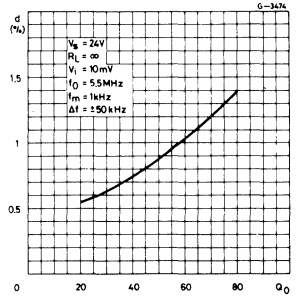


Fig. 6 - Output voltage attenuation vs. DC volume control resistance (P1) and vs. DC volume control voltage (V_C)

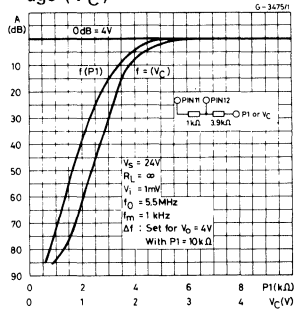


Fig. 7 - Distortion vs. frequency deviation

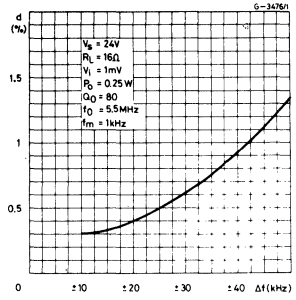


Fig. 8 - Distortion vs. tuning frequency change

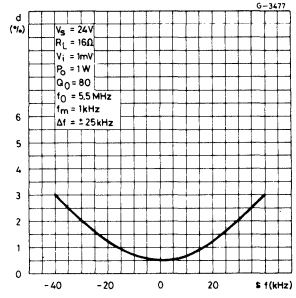


Fig. 9 - Switch-off attenuation of the VCR at pin 4 vs. switch-off voltage at pin 3

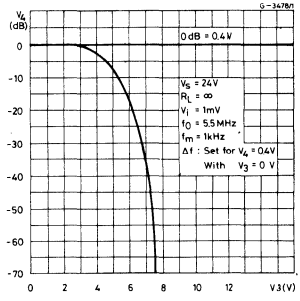


Fig. 10 - Overall frequency response

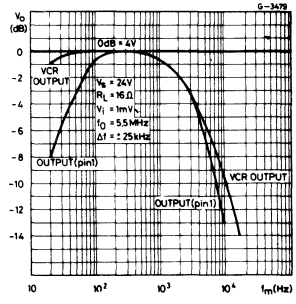


Fig. 11 - Audio amplifier frequency response

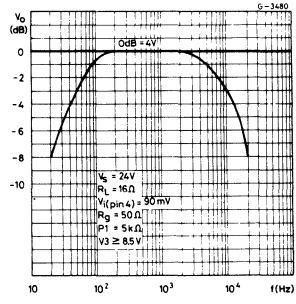


Fig. 12 - Distortion vs. output power (V_s= 24V and R_L= 16Ω)

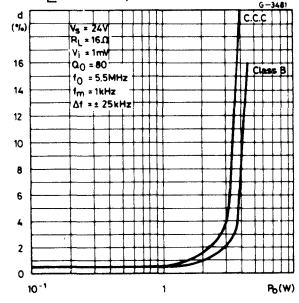


Fig. 13 - Distortion vs. output power (V_s= 12V and R_L= 8Ω)

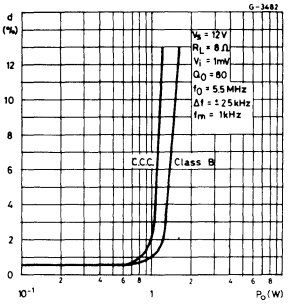


Fig. 14 - Output power vs. supply voltage (class B mode)

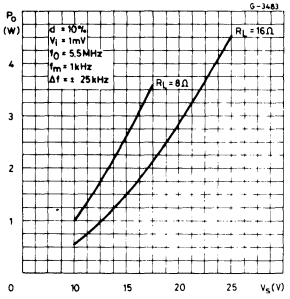


Fig. 15 - Maximum power dissipation vs. supply voltage (sine wave operation; class B mode)

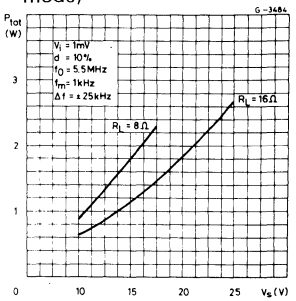


Fig. 16 - Power dissipation and efficiency vs. output power (class B mode)

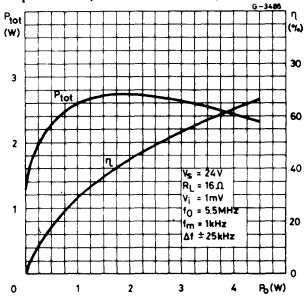


Fig. 17 - Output power vs. supply voltage (C.C.C. mode)

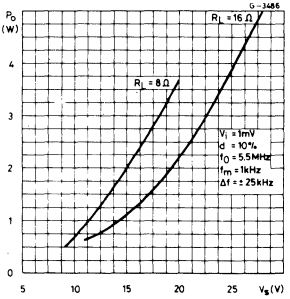


Fig. 18 - Power dissipation and efficiency vs. output power (C.C.C. mode)

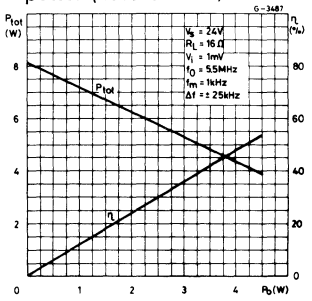


Fig. 19 - Current ripple vs. R-CCC value (C.C.C. mode only)

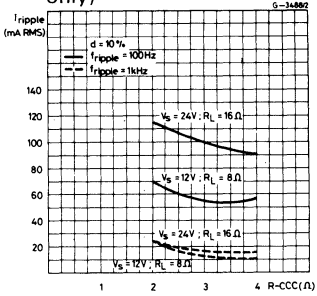


Fig. 20 - Current ripple vs. signal frequency (C.C.C. mode only)

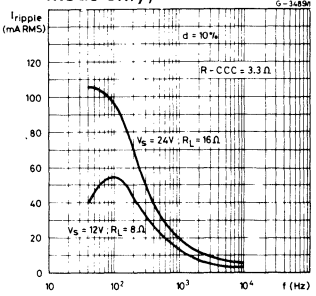


Fig. 21 - Quiescent drain current vs. supply voltage (C.C.C. mode only).

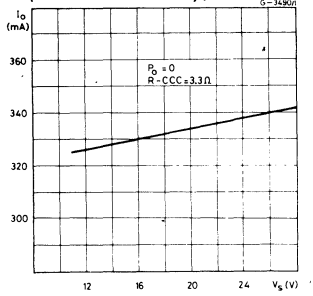


Fig. 22 - Quiescent output voltage (pin 1) vs. supply voltage

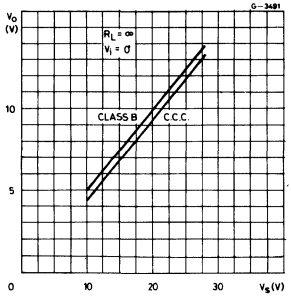


Fig. 23 - Supply voltage ripple rejection vs. volume control attenuation

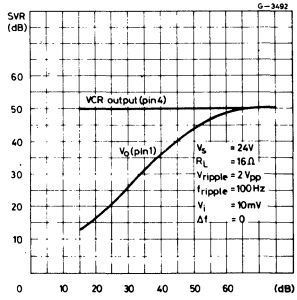
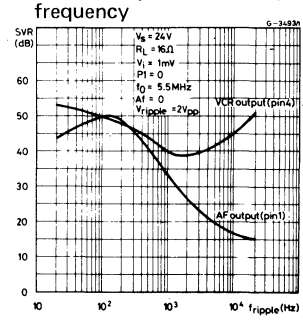


Fig. 24 - Supply voltage ripple rejection at the AF and VCR outputs vs. ripple frequency



APPLICATION INFORMATION (Refer to the block diagram)

IF amplifier and limiter

The IF sound signal is amplified and limited by a chain of 6 differential stages. To avoid the possibility of radiation problems an active low pass filter has been integrated to eliminate the high frequency harmonics from the signal sent to the detector.

Pin 10 is the non inverting input of the amplifier-limiter and it is used as input of the IF sound signal coming from the input network which can employ either LC or ceramic filters.
The typical input impedance of pin 10 is 10 KΩ, 5 pF at f_o = 5.5 MHz.

Pin 8 is the inverting input, of the amplifier-limiter. The DC negative feedback of the amplifier is applied internally to this pin which must therefore be decoupled by means of a by pass capacitor toward ground.

FM detector

Signal detection is obtained by means of a peak differential detector which enables radiation problems to be minimized.

Pin 7 is the first input of the peak differential detector and it is the output of the low pass filter. The typical output impedance is 2.7 KΩ.

Pin 6 is the second input of the peak differential detector. This pin must be supplied with the same DC voltage as the other input (pin 7) and this is done by coil L1.
External components L1 C3 and C5 transform the frequency variations into amplitude variations useful to drive the detector. Network L1 C3 C5 has two resonance frequencies:

$$f_1 \text{ series resonance for } X_{C5} = \frac{X_{L1} \cdot X_{C3}}{X_{C3} + X_{L1}}$$

$$f_2 \text{ parallel resonance for } X_{L1} = X_{C3}$$

APPLICATION INFORMATION (continued)

Coil L1 must be tuned at frequency f_o = IF sound, equidistant from frequencies f_1 and f_2 to which the peaks of the "S" response of the detector correspond. The separation between the peaks is defined by the ratio $\frac{f_2^2}{f_1^2} = 1 + \frac{C5}{C3}$.

Network L1 C3 C5 can obviously be substituted by a ceramic filter.

Pin 5 is the output of the FM detector. Its output impedance of 20 KΩ, in combination with capacitor C4 connected between pin 5 and ground, defines the time constant of the deemphasis. The detector "S" curve is visible at pin 5. Improved AMR performance can be obtained by connecting a 10 KΩ 10 μF RC series network between pin 5 and ground.

VCR

This function, required by receivers capable of recording complete TV signals, is made in accordance with DIN Norms. A single pin (pin 4) acts both as output of the signal to be recorded and as input of the signal to be played back. The function of this pin is changed by means of a control, applied to pin 3, consisting of two different levels of DC voltage. The operating conditions of pins 3 and 4 are:

Mode	VCR Switch pin 3	Function of pin 4	Impedance of pin 4	Signal at pin 4
Recording	$V_3 \leqslant 2V$	Output	R4 = 140Ω	V_4 = 400 mV
Playback	$V_3 \geqslant 8.5V$	Input	R4 = 13 KΩ	V_4 = 90 mV

In the recording state the output signal at pin 4 is independent of the volume control, while during playback the signal applied at pin 4 is regulated by the volume control before being sent to the audio amplifier.

Pin 3, input of the VCR switch, has an impedance greater than 50KΩ for any value of input voltage. Control pulses at pin 3 with very sharp edges cause temporary unbalancing of the circuit and produce audible signals. This effect is eliminated by means of R3 C8 which slows down the control edges. In the playback state the IF sound signal coming from the detector is automatically blocked by the VCR switch.

Pin 4, input-output of the audio signal, has a DC typical voltage of 6V. C6 must therefore be used to decouple it from the VCR.
The output signal of pin 4 can be used to perform the AC volume control (fig. 31). The potentiometer must be connected between pin 4 and ground and the slider must be connected to pin 13 after DC decoupling.

DC volume control

The audio signal coming from the FM detector or from the VCR is adjusted in amplitude by means of a DC controlled active attenuator. The attenuation can be changed either by means of a potentiometer or by means of a DC voltage.

Pin 11 supplies the reference voltage for the volume control.
This voltage is between 4V and 5.5V and has a thermal coeff. of +0.25%/°C. The maximum current which can be supplied by pin 11 is 10 mA.

APPLICATION INFORMATION (continued)

Pin 12 is the input of the DC volume control. To minimize the attenuation spreads, the volume control network R1, R2, P1 is supplied by the reference voltage of pin 11. The attenuation of the signal is inversely proportional to the voltage applied at pin 12; therefore maximum attenuation is for $V_{12} = 0$ or for P1 = 0 . Capacitor C7, connected in parallel to the volume potentiometer, eliminates any signals or spikes picked up by the connection wires of the potentiometer. The volume control characteristic depends on the configuration and on the values of the components of the network connected to pins 11 and 12. The suggested values are: R1= 1 KΩ R2= 3.9 KΩ and P1= 5 KΩ with linear variation; with this network a linear variation of the output power is obtained. Different slopes of the volume control and relative networks are shown in figs. 25 and 26.

Fig. 25

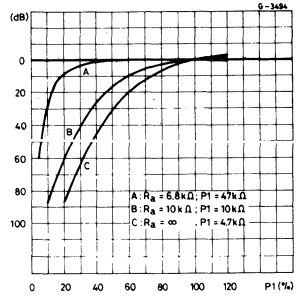
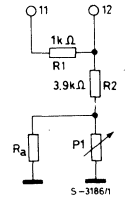


Fig. 26



The volume can also be controlled by means of a DC voltage applied between resistor R2 and ground instead of potentiometer P1. Using this configuration, volume variation can be obtained by means of remote control as shown in fig. 36.

AF amplifier

The AF amplifier consists of an operational amplifier with thermally protected (thermal shut down) output stage. By using a simple external variant the power stage can be made to operate in class B or in costant current consumption.

Pin 1 is the output of the power amplifier. The network which defines the gain and the band of the audio amplifier is connected between pins 1, 2 and 13.
The input voltage of the amplifier is $I \cdot R4$, where I is the signal output current of the DC volume control block. The closed loop gain of the amplifier is given by $G_v = R5/R6$;
Therefore the output voltage is given by

$$V_o = I \cdot R4 \cdot \frac{R5}{R6}$$

Changing the values of these resistors, different output voltage (i.e. different closed loop gain) can be obtained.
When impedances, rather than pure resistors, are used, the closed loop gain is changed with frequency. In particular at high frequencies the gain is reduced by capacitor C11 and at low frequencies it is reduced by capacitor C13.
The Boucherot cell R7 C14 guarantees the stability of the circuit in all the operating conditions.

Pin 2, the non inverting input of the audio amplifier, is connected to an integrated voltage divider which fixes its DC voltage at $V_s/2$.

APPLICATION INFORMATION (continued)

Since the voltage of pin 2 is the reference of the input differential stage of the audio amplifier, both the voltage of pin 13 and the voltage of pin 1 are equal to $V_s/2$. Capacitor C12, connected between pin 2 and ground, has the dual function of eliminating the audio signals from pin 2 and providing the supply voltage ripple rejection.

Pin 13 is the inverting input of the audio preamplifier; the outoput of the DC volume control is also connected to this pin.

Supply

The device can operate either in class B or in C.C.C. mode. In class B the supply current is highly variable and depends on the power supplied to the load. The supply must therefore be well filtered to prevent modulation effects on the supply itself which may influence other circuits in the TV. In C.C.C. mode supply current is constant and the supply system can therefore be simplified; for example the sound channel can be supplied directly by the line transformer without problems of modulation of the picture size.

Pin 15 is the main supply of the device; when it is connected directly to the power supply and pin 14 is left open, the circuit operates in class B.

Pin 14 is the supply point for C.C.C. The reference system, connected between pin 14 and pin 15, determines a constant voltage of 1.1V between the two pins. To make the device operate in C.C.C. mode, pin 14 must be connected to the supply and a resistor R-CCC must be connected between pin 14 and pin 15; the value of this resistor defines the quiescent current $I_{CCC} = 1.1V/R\text{-}CCC$.

Pin 9 is the main ground of the circuit.

Pin 16 is the ground of the power output stage only.

APPLICATION INFORMATION (continued)

Fig. 27 - Typical application circuit (class B mode)

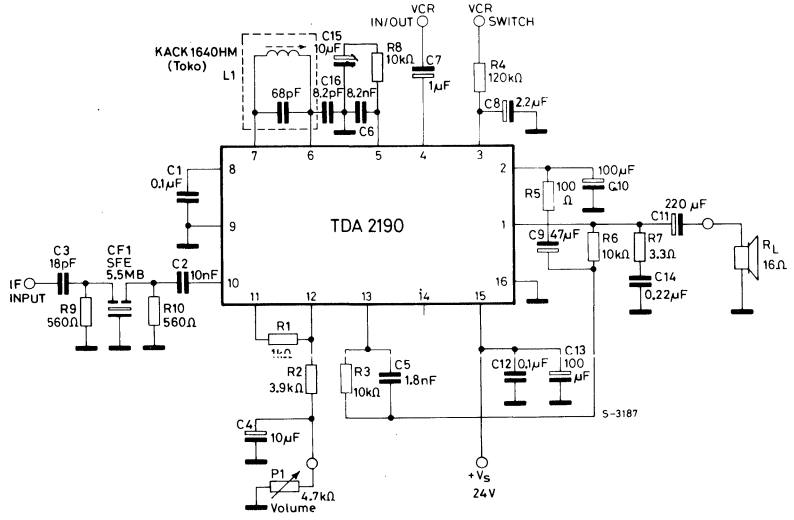
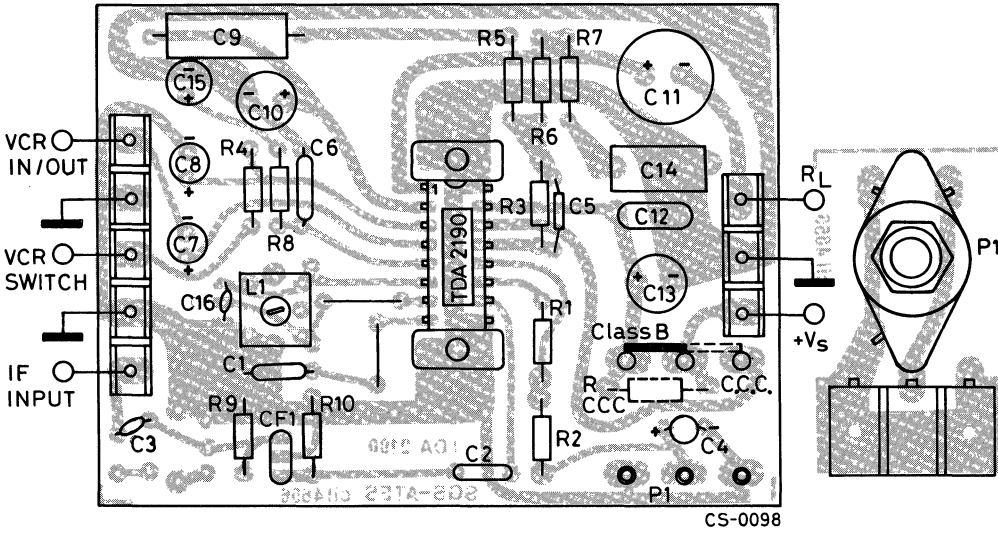


Fig. 28 - P.C. board and component layout of the circuit shown in fig. 27 (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 29 - Application using a ceramic discriminator and an LC network at the IF input (C.C.C. mode)

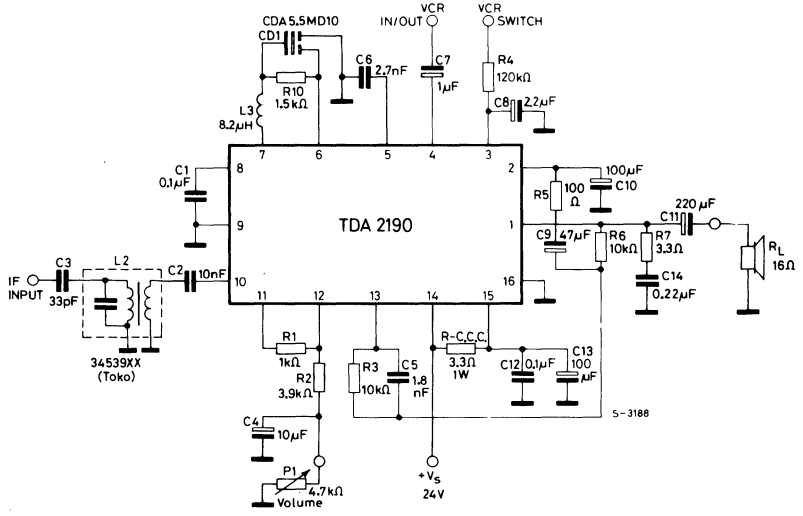
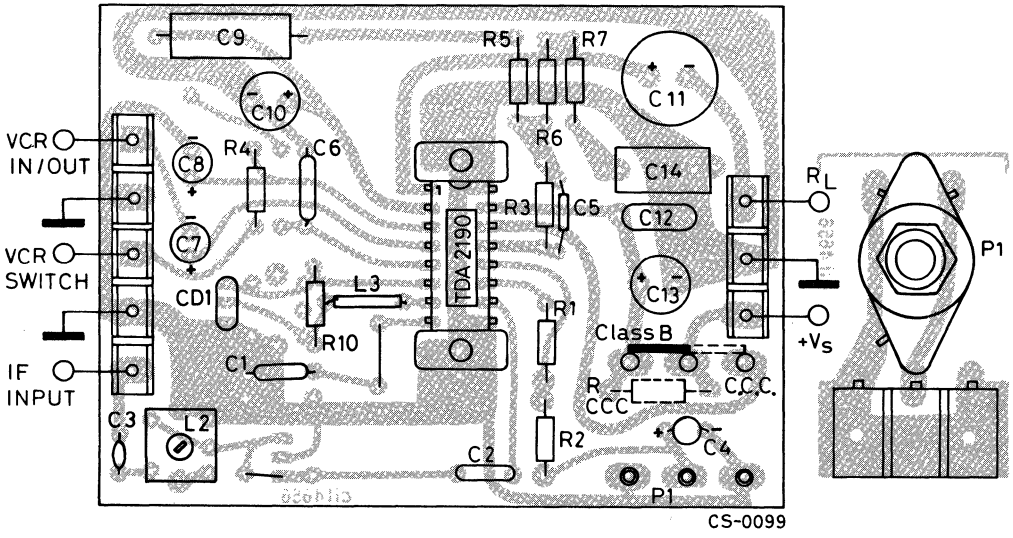


Fig. 30 - P.C. board and component layout of the circuit shown in fig. 29. (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 31 - Application circuit with AC volume control

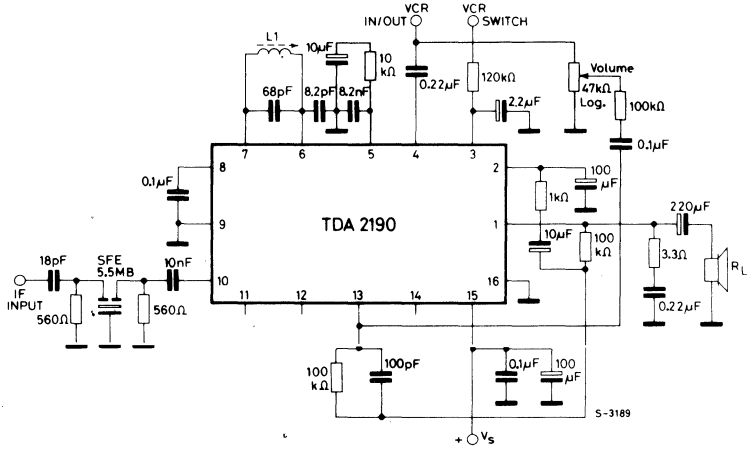
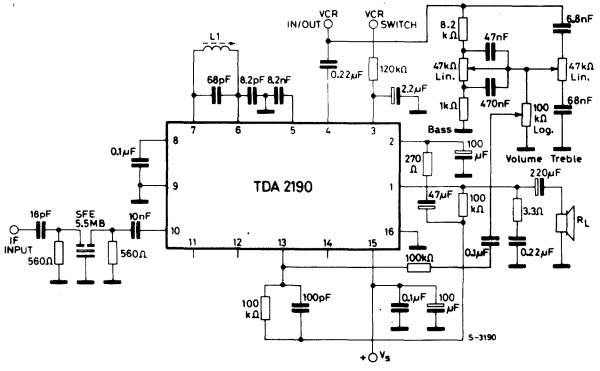
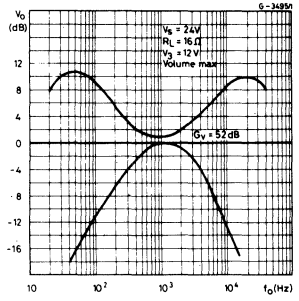


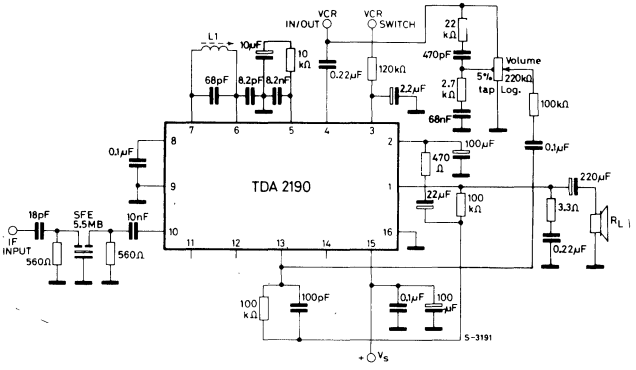
Fig. 32 - Application circuit with tone controls





APPLICATION INFORMATION (continued)

Fig. 33 - Application circuit with physiological volume control



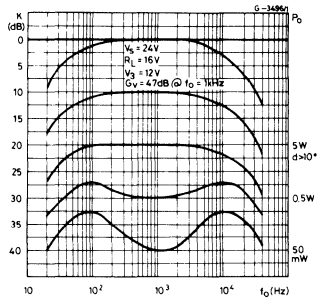
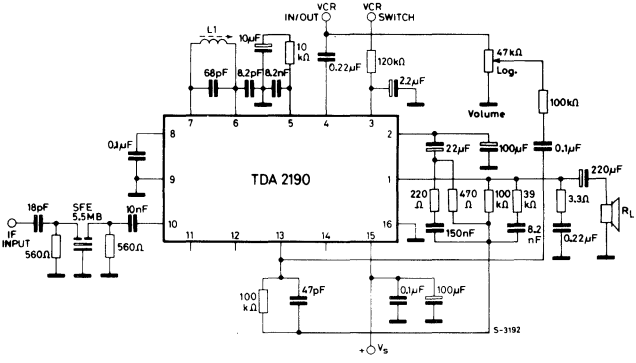
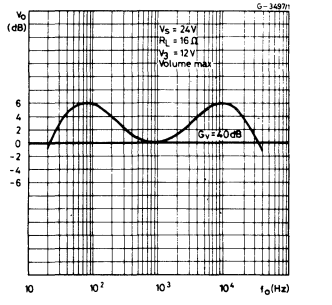


Fig. 34 - Application circuit with fixed bass and treble boost





APPLICATION INFORMATION (continued)

Fig. 35 - Application circuit for 10W of output power when V_s= 22V and R_L= 4Ω

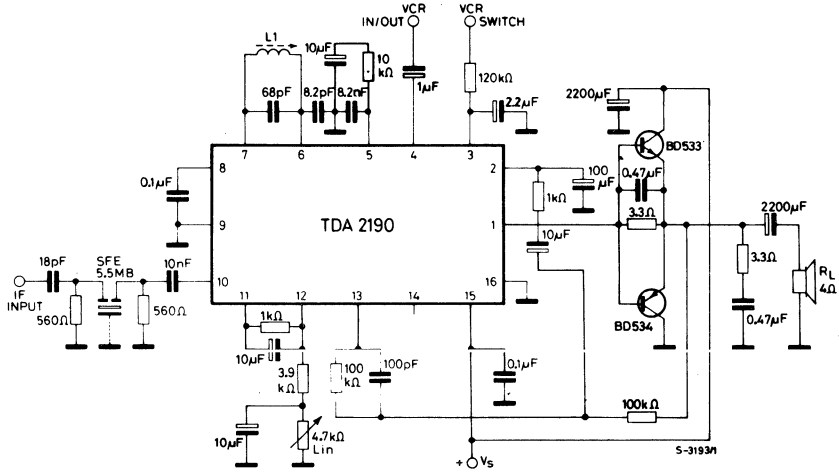
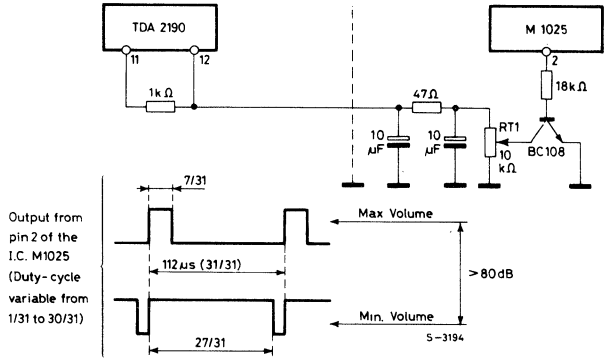


Fig. 36 - Remote volume control. The output of the sound channel increases when the duty-cycle at pin 2 of the I.C. M1025 decreases



NOTE:
RT1 must be set for the normalization of the output power (P_o= 100 mW).
Procedure:
– IF input at pin 10 of the TDA 2190
V_s= 24V; R_L= 16Ω; V_i= 1 mV; f_o= 5.5 MHz; Δf = ± 25 KHz; f_m = 1 KHz.

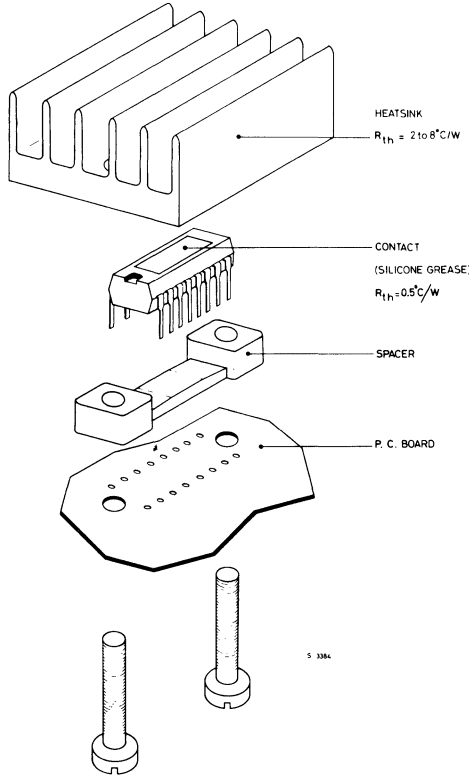
Whith the normalizated output of the I.C. M1025 (duty cycle of 10/31), set RT1 for 1.26 V_{RMS} across the load R_L = 16Ω.

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink as shown in figs. 37 and 38.
The system for attaching the heatsink is very simple: it uses a plastic spacer which is supplied with the device on request (TDA 2190 F2).
Thermal contact between the copper slug (of the package) and the heatsink is guaranteed by the pressure which the screws exert via the spacer and the printed circuit board; this is due to the particular shape of the spacer.

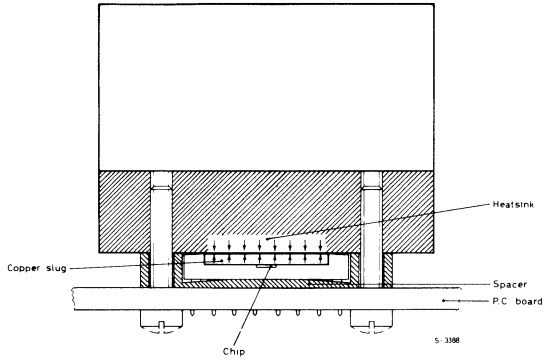
Note : The most negative supply voltage is connected to the copper slug, hence to the heatsink (because it is in contact with the slug).

Fig. 37 - Mounting system



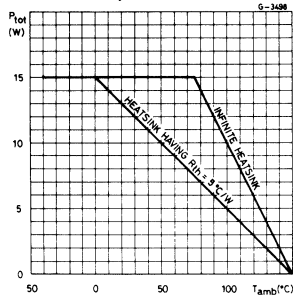
MOUNTING INSTRUCTIONS (continued)

Fig. 38 - Cross-section of mounting system



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance): fig. 39 shows this dissipable power as a function of ambient temperature for an heatsink having 5°C/W.

Fig. 39 - Maximum allowable power dissipation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA2310

Hi-Fi DUAL PREAMPLIFIER

The TDA2310 is a dual high quality **class A** preamplifier intended for extremely low distortion application in Hi-Fi systems.
The TDA2310 is a monolithic integrated circuit in a 14-lead dual-in-line plastic package and its main features are:

- Very high dynamic range
- Very low distortion
- High open loop bandwidth
- Very low noise
- No pop-noise
- High slew-rate: 14V/μs (G_v= 30 dB) - 50V/μs (G_v= 50 dB)
- Large output voltage swing
- Single or split supply operation
- Output short circuit protection

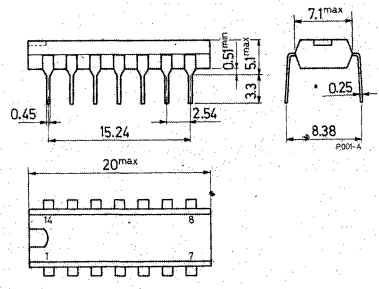
ABSOLUTE MAXIMUM RATINGS

V_s	DC supply voltage	± 22	V
V_s	Operating supply voltage	± 20	V
V_{cm}	Common mode input voltage	± 15	V
V_i	Differential input voltage	± 5	V
P_{tot}	Total power dissipation at $T_{amb} \leq 60°C$	500	mW
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

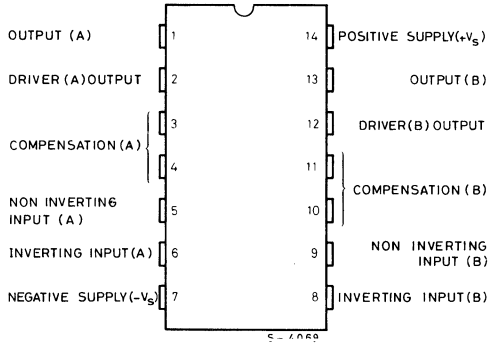
ORDERING NUMBER: TDA2310

MECHANICAL DATA

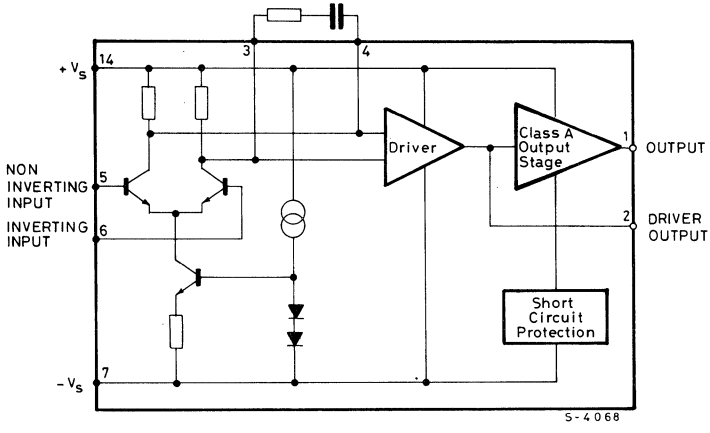
Dimensions in mm



CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM
(one section)



THERMAL DATA

$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max.	180	°C/W

Fig. 1 - Gain and distortion test

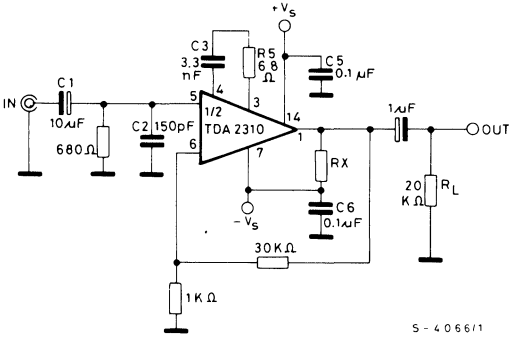
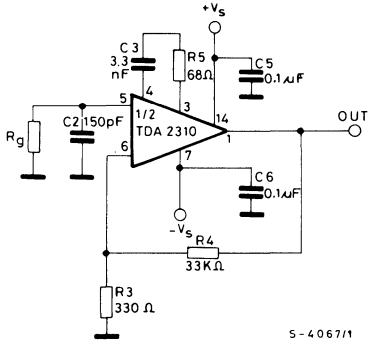


Fig. 2 - Noise test



ELECTRICAL CHARACTERISTICS (Refer to the Test circuit of fig. 1, $T_{amb} = 25°C$, $V_s = \pm 15V$, $G_v = 30dB$, $R_L = 20K\Omega$ unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 5		± 20	V
I_s	Supply current			10	15	mA
I_b	Input bias current			0.2	1	μA
I_{os}	Input offset current			50	300	nA
V_{os}	Input offset voltage			1	3	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
G_v	Voltage gain (open loop)	f = 1KHz	No compensation		85		dB
		f = 20KHz			85		dB
ΔG_v	Voltage gain spread (closed loop)	f = 1KHz			±0.2		dB
		f = 100KHz			±0.5		dB
R_i	Input resistance	f = 1KHz			5		MΩ
R_o	Output resistance				10		Ω
V_{pp}	Output voltage swing (peak to peak)	d = 1%	f = 1KHz		24		V
			f = 100KHz		22		V
V_o	Output voltage (rms)	R_x = 8.2KΩ	f = 1KHz	6	8		V
			f = 20KHz	6	8		V
BW	Power bandwidth	V_o = 20 V_{pp}, R_x = 8.2 KΩ			100		KHz
SR	Slew rate	G_v = 30dB			14		V/μs
		G_v = 50dB (C_3 = 330pF, R_5 = 470Ω)			50		V/μs
d	Total harmonic distortion	V_o = 3V	f = 1KHz		0.035		%
			f = 20 KHz		0.035		%
d_2	Second order CCIF intermodulation distortion	V_{o1} = 1V, V_{o2} = 1V	f2 - f1 = 1 KHz		0.01	0.1	%
d_3	Third order CCIF intermodulation distortion	f1 = 14KHz, f2 = 15KHz	$2f_1 - f_2$ = 13 KHz		0.03	0.1	%
e_N	* Total input noise	R_g = 600Ω R_g = 3.3KΩ (°)			0.6 1.0	0.8	μV
		R_g = 600Ω R_g = 3.3KΩ (°°)			0.75 1.2		μV
S/N	* Signal to noise ratio	V_o = 500mV	R_g = 3.3K R_g = 600 (°) R_g = 0		74 78 80		dB
			R_g = 3.3K R_g = 600 (°°) R_g = 0		72 76 78		dB
C_s	Channel separation	f = 20KHz R_g = 600Ω			100		dB
CMR	Common mode rejection	R_g = 600Ω			95		dB
SVR	Supply voltage rejection	R_g = 600Ω			85		dB
I_{sh}	Output short circuit current				15		mA

(*) Test circuit of fig. 2 (G_v = 40 dB)
(°) BW = curve A (°°) BW = 22Hz to 22KHz

Fig. 3 - Harmonic distortion vs. output level.

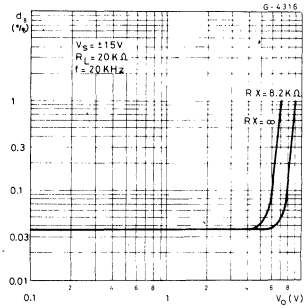


Fig. 4 - Harmonic distortion vs. frequency.

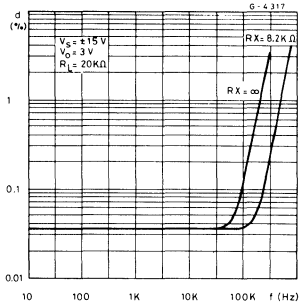


Fig. 5 - Output voltage swing vs. frequency.

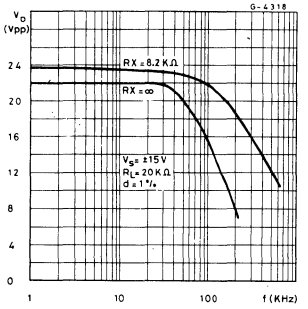


Fig. 6 - Output voltage swing vs. load resistance.

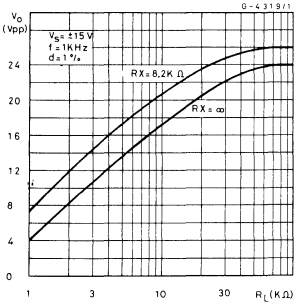


Fig. 7 - Total input noise vs. source resistance.

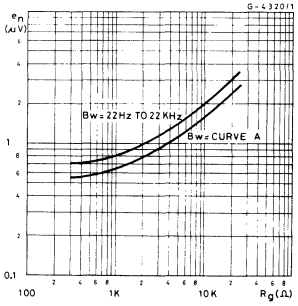


Fig. 8 - Noise density vs. frequency.

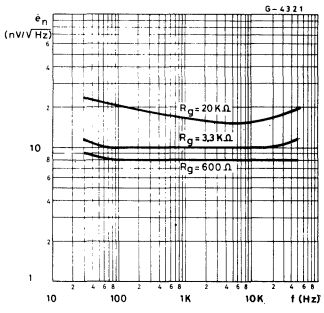


Fig. 9 - Open loop frequency response.

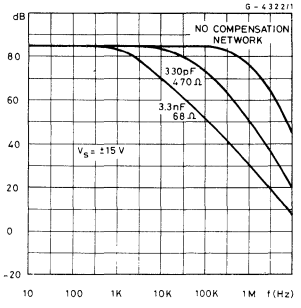


Fig. 10 - Closed loop gain vs. frequency.

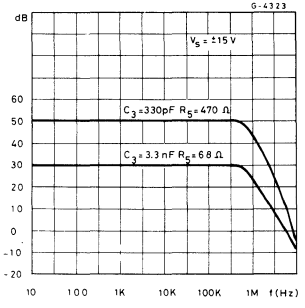
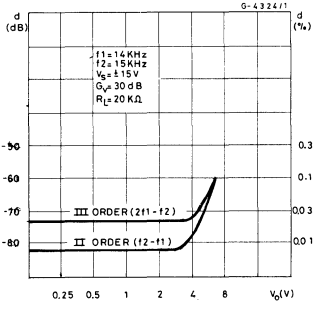


Fig. 11 - Two tone CCIF intermod. distortion.



APPLICATION INFORMATION

Fig. 12 - Very low dynamic distortion stereo RIAA preamplifier.
$V_s = \pm 15V$
RIAA frequency response (20Hz to 20KHz) = ± 0.5 dB
Harmonic distortion = 0.02% (f = 20KHz)

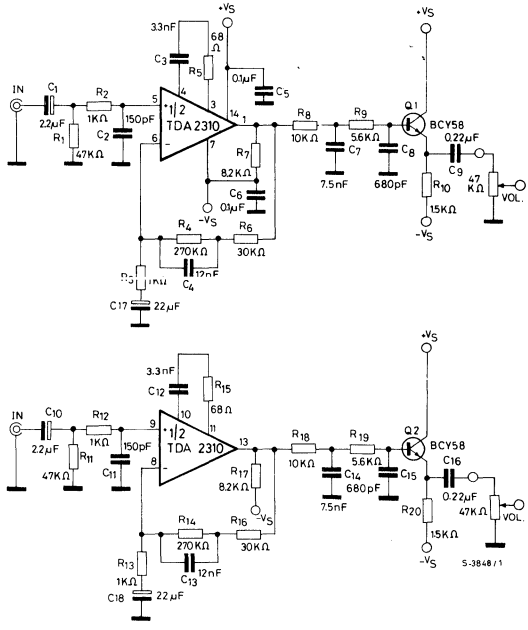


Fig. 13 - RIAA preamplifier response.

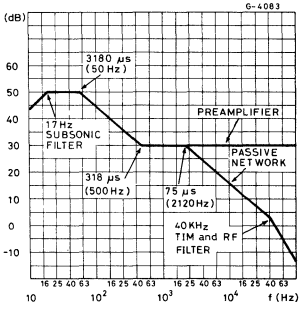


Fig. 14 - Two tone intermodulation distortion vs. input level.

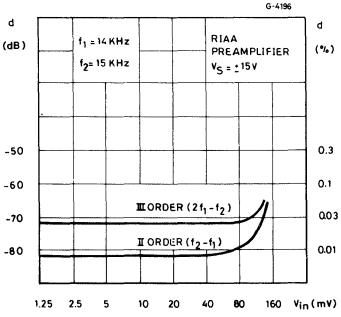
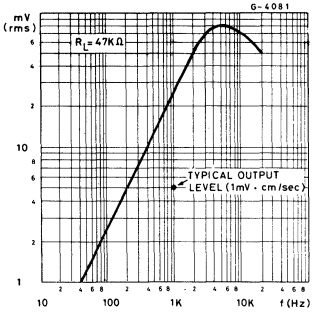
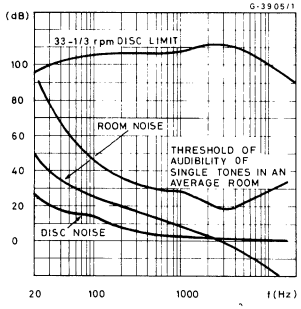


Fig. 15 - Maximum output level of high quality magnetic cartridge vs. frequency.



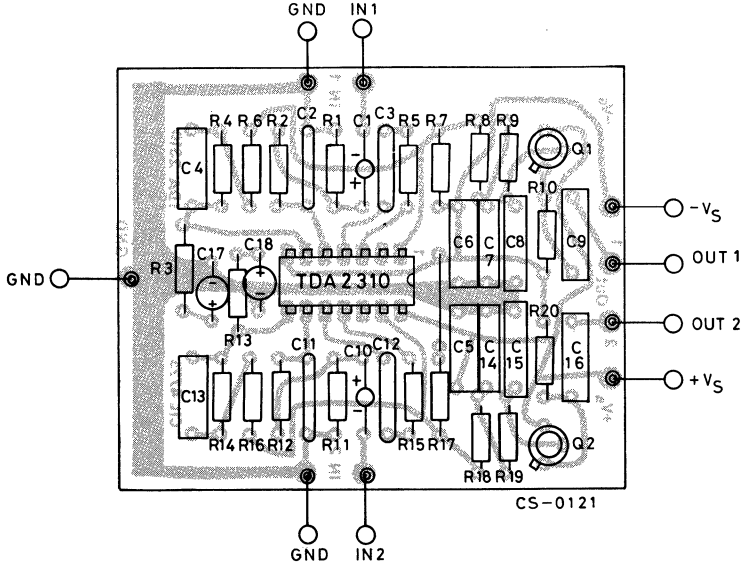
APPLICATION INFORMATION (continued)

Fig. 16 - Dynamic range of disc music.



As shown in fig. 15 the maximum expected output level of an high quality magnetic cartridge playing modern discs is lower than 80mV rms.
The dynamic range needed is about 70dB (fig. 16).
The TDA2310 is perfectly suited to RIAA preamplifier applications due to the ~100 dB dynamic range (150mV input 0.1% distortion to 1 μV noise).

Fig. 17 - PC board and components layout of RIAA preamplifier (1:1 scale)



APPLICATION INFORMATION (continued)

Fig. 18 - Hi-Fi tape preamplifier (EQ. = 70μs).

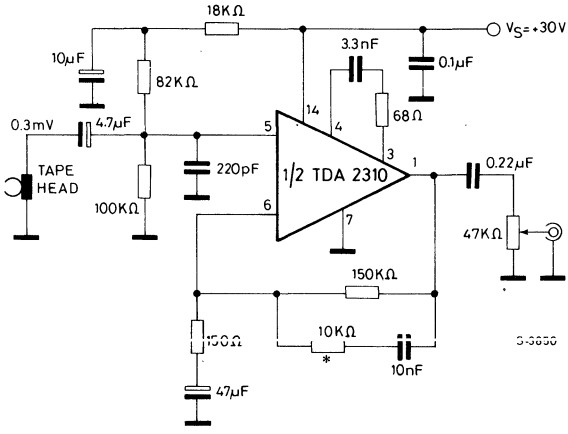
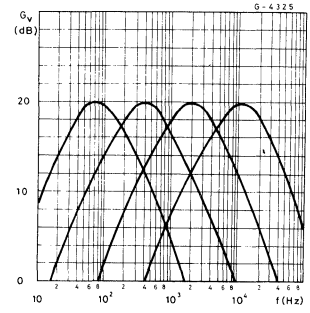
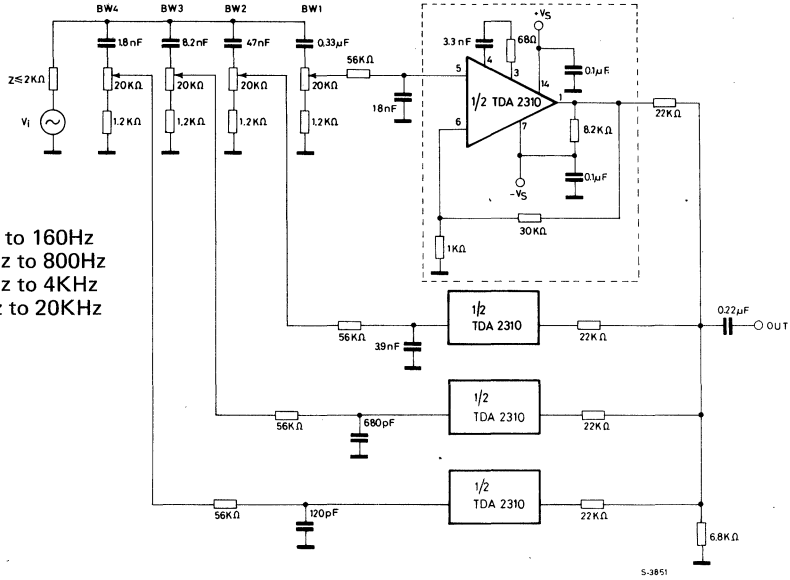


Fig. 19 - Frequency response of graphic equalizer of fig. 20



* 18KΩ for EQ = 120μs.

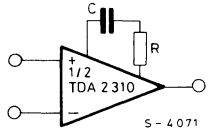
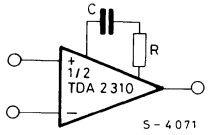
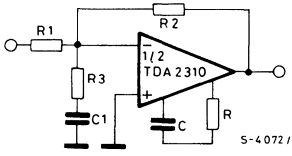
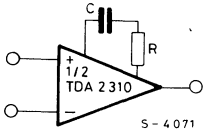
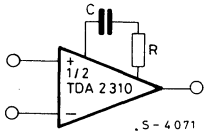
Fig. 20 - Four band graphic equalizer



BW1 = 30Hz to 160Hz
BW2 = 160Hz to 800Hz
BW3 = 800Hz to 4KHz
BW4 = 4KHz to 20KHz

APPLICATION INFORMATION (continued)

The table shows the suggested compensation networks depending on the slew-rate and gain required in the application.

Slew-Rate (V/μs)	G_v min. (dB)	Compensation Network		Note
50	50		R = 470Ω C = 330pF	High gain Applications
14	30		R = 68Ω C = 3.3nF	RIAA Preamplifier
14	10		R_1 = 56KΩ R_2 = 180KΩ R_3 = 680Ω C_1 = 10nF	Inverting Configuration
	0	R = 68Ω C = 3.3nF	R_1=R_2=56KΩ R_3 = 680Ω C_1 = 10nF	
5	20		R = 33 Ω C = 10nF	Low Slew-Rate Applications
2	6		R = 10 Ω C = 47 nF	

TDA2320

LINEAR INTEGRATED CIRCUIT

PRELIMINARY DATA

PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

The TDA 2320 is a monolithic integrated circuit in Minidip package specially designed to amplify the IR signal in remote controlled TV or radio sets. It directly interfaces with the digital control circuitry.
The TDA 2320 incorporates a two stages amplifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and "with" or "without" carrier transmission modes as provided for example by the M709/M710 C/MOS transmitter.
The TDA 2320 is particularly intended to be used in conjunction with the M103, M104 and M206 + M3870 remote control receivers.

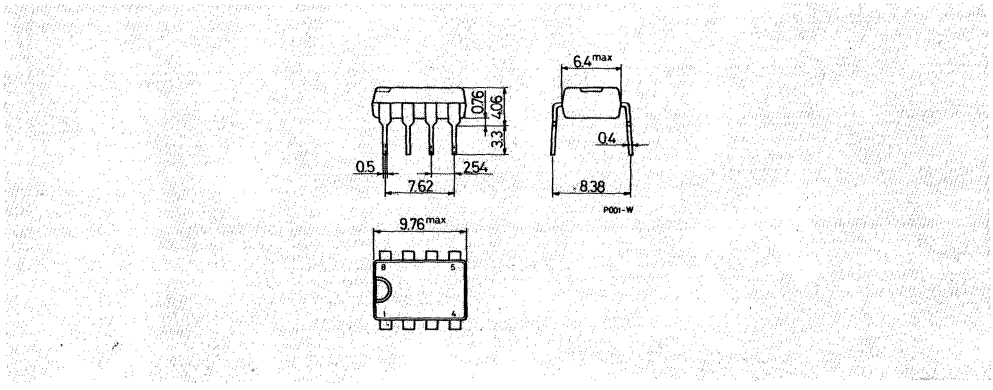
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
$T_{stg,\ j}$	Storage and Junction temperature	-40 to 150	°C
P_{tot}	Total power dissipation at T_{amb} = 70°C	400	mW

ORDERING NUMBER: TDA 2320

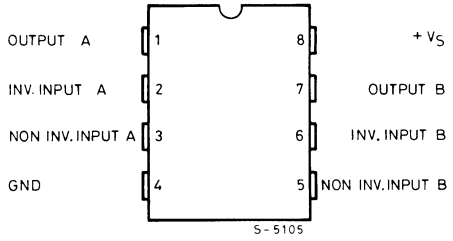
MECHANICAL DATA

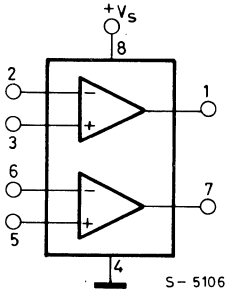
Dimensions in mm



CONNECTION AND BLOCK DIAGRAM

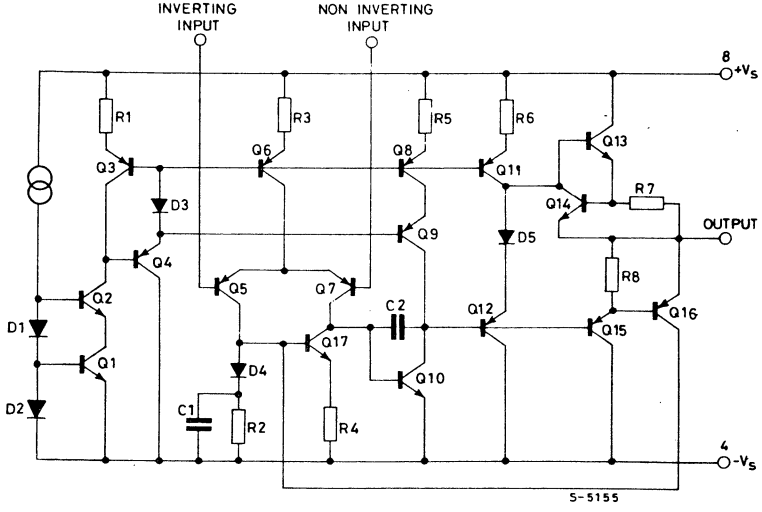
(top view)





SCHEMATIC DIAGRAM

(one section)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 5V, T_{amb}= 25°C, single amplifier, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		20	V
I_s	Total supply current	V_s = 20V		0.8	2	mA
I_b	Input bias current			100	500	nA
V_{os}	Input offset voltage	R_g < 10 KΩ		0.5		mV
I_{os}	Input offset current			15		nA
G_v	Open loop voltage gain	f = 1 KHz	64	70		dB
		f = 100 KHz		30		dB
B	Gain bandwidth product	f = 40 KHz	1.5	3		MHz
SR	Slew rate	R_L= 2 KΩ		1.5		V/μs
e_N	Total input noise voltage	f = 40 KHz Rg= 10KΩ		20		$nV/\sqrt{Hz}$
V_o.	DC output voltage swing			2.5		Vpp
SVR	Supply voltage rejection (*)	f = 100 Hz		80		dB

(*) Circuit of fig. 1.

APPLICATION INFORMATION

Fig. 1 - Application circuit with carrier

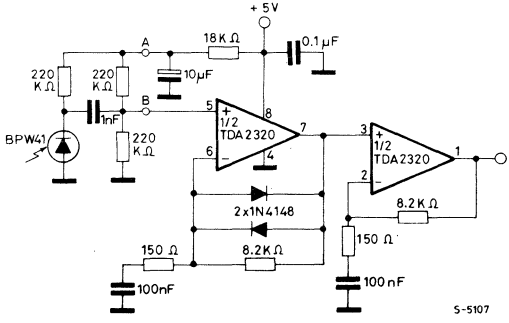
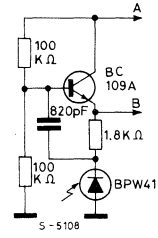


Fig. 2 - Alternative input stage



APPLICATION INFORMATION (continued)

The preamplifier shown in fig. 1 must be used with carrier mode transmission. It is particularly suitable for use with microprocessor decoding system (for instance with the M206 + M3870 or M3872 TV PLL frequency synthesizer).
The "with carrier" signal is sent as a burst (f_{carr} = 38 KHz) to reduce power consumption at the transmitter (duty cycle = 1%) and to allow the receiver to have some bandwidth limiting in the preamplifier to improve noise immunity (50/100 Hz pulses from incandescent lighting).
The fig. 2 shows an alternative configuration for the input stage: this new circuit allows the correct operation of the preamplifier even when an incandescent lamp is very close to the IR diode.
Using this configuration, the circuit has only a slight degradation in the useful range.

Fig. 3 - Tuned amplifier application (with carrier)

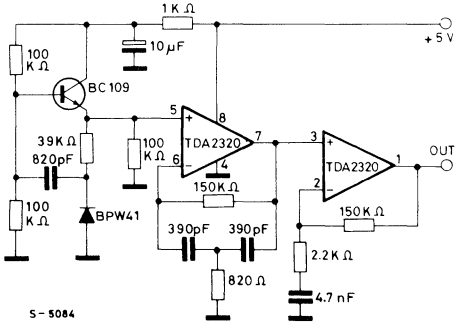
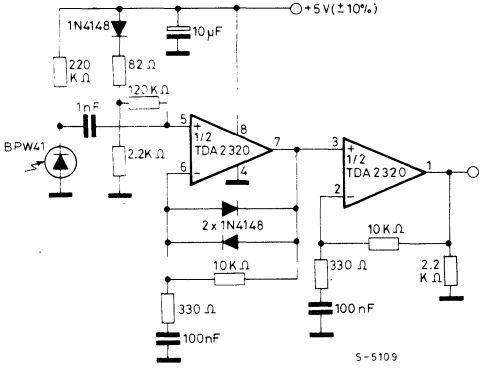


Fig. 4 - Application circuit without carrier



APPLICATION INFORMATION (continued)

The circuit shown in fig. 4 works in transmission mode without carrier. The transmitted signal is sent as a series of single pulses (rather than bursts, as with the carrier solution).
The DC bias network formed by the 82/2.2 KΩ divider and 1N4148 diode fixes the DC output voltage near the supply voltage (just under the saturation level). In this way it is possible to optimize the noise immunity of the receiver. The 2.2 KΩ output resistance avoids turn-off problems in the final stage.

Performance

Supply voltage	4.5V min; 5.5V max
Quiescent drain current	6 mA
Supply voltage rejection (f = 100 Hz)	greater than 50 dB
Useful range (using the transmitter of fig. 7)	14 mt

With a incandescent light (75W) as a noise source located at 1 mt from the receiver the useful range decreases to 10 mt.

Fig. 5 - Optimized preamplifier ("no carrier" mode)

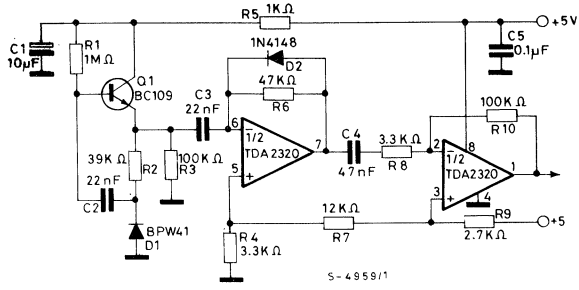
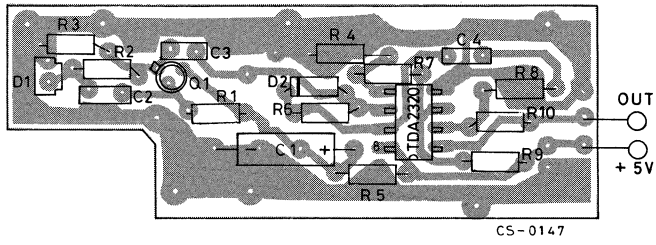


Fig. 6 - P.C. and components layout of the circuit of fig. 5 (1 : 1 scale)



APPLICATION INFORMATION (continued)

Fig. 7 - IR transmitter using M709 or M710

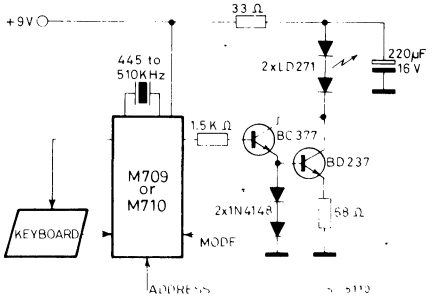


Fig. 8 - MMC II - PLL TV Frequency synthesizer

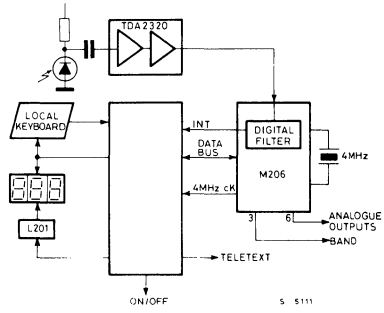
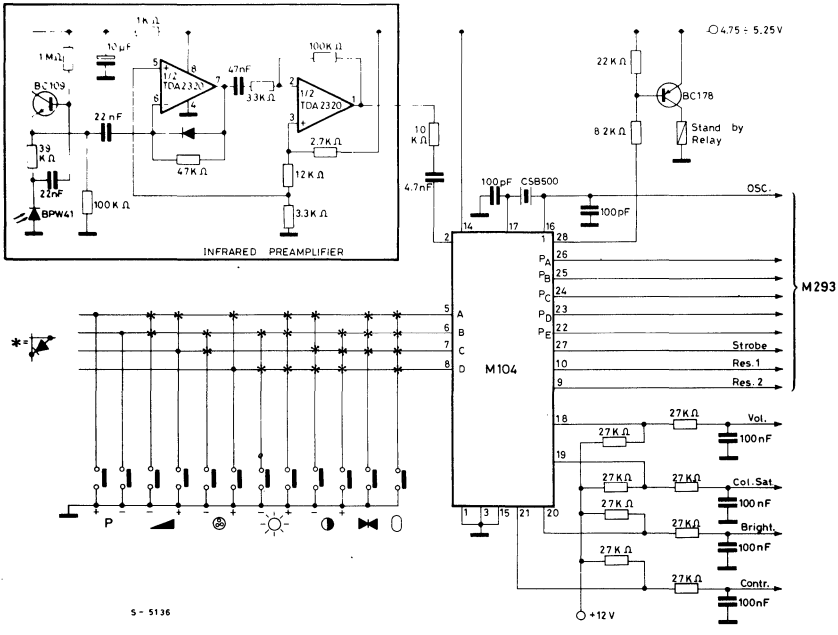


Fig. 9 - IR Preamplifier and Remote Control receiver for 32 channels voltage synthesizer (EPM - M293)



TDA2320A

LINEAR INTEGRATED CIRCUIT

PRELIMINARY DATA

MINIDIP STEREO PREAMPLIFIER

The TDA 2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.
The TDA 2320A is a monolithic integrated circuit in a 8 lead minidip which features:

- Wide supply voltage range (3 to 36V)
- Single or split supply operation
- Very low current consumption (0.8 mA)
- Very low distortion
- No pop-noise
- Short circuit protection

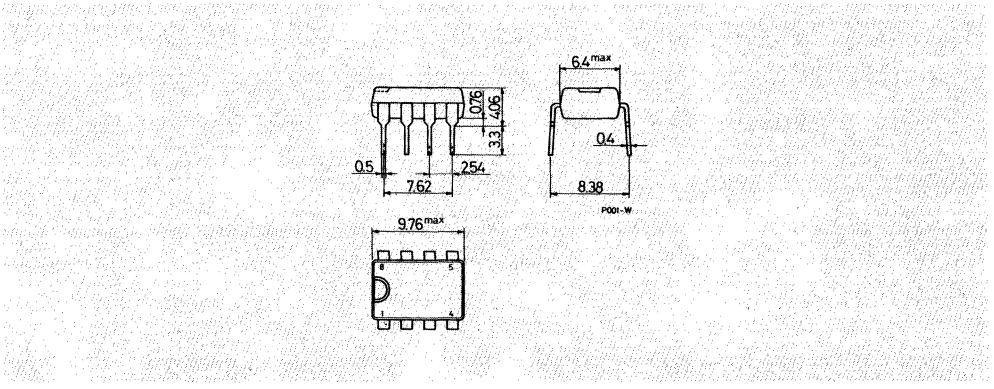
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
P_{tot}	Total power dissipation at $T_{amb} = 70°C$	400	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

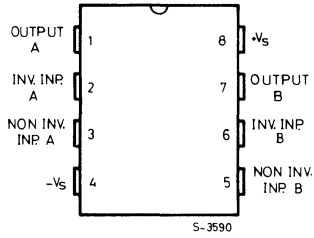
ORDERING NUMBER: TDA 2320A

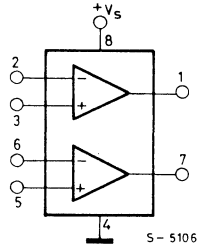
MECHANICAL DATA

Dimensions in mm

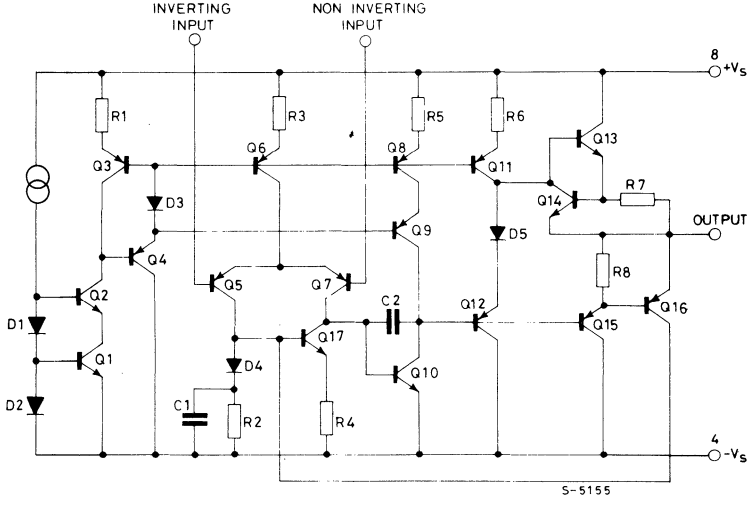


CONNECTION AND BLOCK DIAGRAM
(top view)





SCHEMATIC DIAGRAM
(one section)



TEST CIRCUITS

Fig. 1

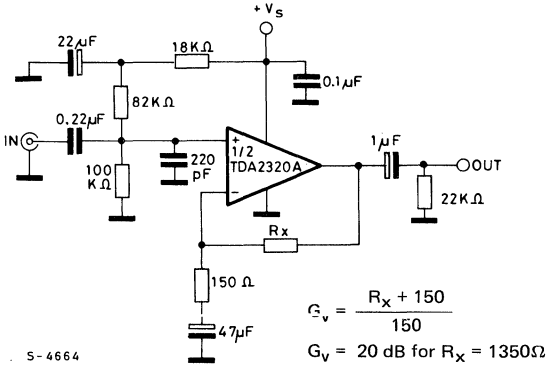
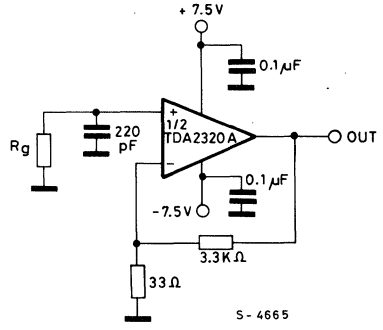


Fig. 2



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	200	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_s = 15V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage (*)			3		36	V
I_s	Supply current (*)				0.8	2	mA
I_b	Input bias current				150	500	nA
V_{os}	Input offset voltage	$R_g < 10\ K\Omega$			0.5	5	mV
I_{os}	Input offset current				10	50	nA
G_v	Open loop voltage gain	V_s = 15V	f = 333 Hz		80		dB
			f = 1 KHz		70		
			f = 10 KHz		50		
		V_s = 4.5V	f = 1 KHz		70		
V_o	Output voltage swing (*)	f = 1 KHz	V_s= 15V		13		Vpp
		R_L= 600Ω	V_s= 4.5V		2.5		
B	Gain-bandwidth product	f = 20 KHz		1.5	2.5		MHz
BW	Power bandwidth (*)	V_o= 5 Vpp d = 1%		40	70		KHz
SR	Slew rate (*)			1	1.6		V/μS
d	Distortion (*)	V_o= 2V	f = 1 KHz		0.03		%
		G_v= 20 dB	f = 10 KHz		0.08		
e_N	Total input noise voltage (**)	Curve A	R_g= 50Ω		1		μV
			R_g= 600Ω		1.1	1.4	
			R_g= 5 KΩ		1.5		
		B = 22 Hz to 22 KHz	R_g= 50Ω		1.3		μV
			R_g= 600Ω		1.5		
			R_g= 5 KΩ		2		
		f = 1 KHz	R_g= 600Ω		9		$nV/\sqrt{Hz}$
Cs	Channel separation (**)		f = 1 KHz		100		dB
SVR	Supply voltage (**) rejection		f = 100 Hz		80		dB

(*) Test circuit of fig. 1.
(**) Test circuit of fig. 2.

Fig. 3 - Supply current vs. supply voltage

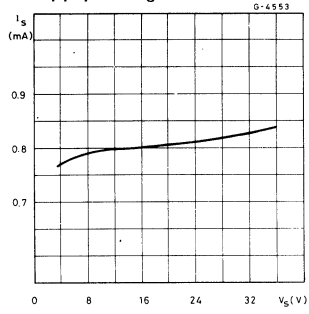


Fig. 4 - Supply current vs. ambient temperature

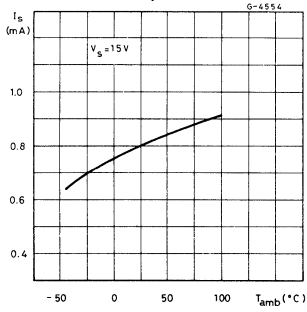


Fig. 5 - Output voltage swing vs. load resistance

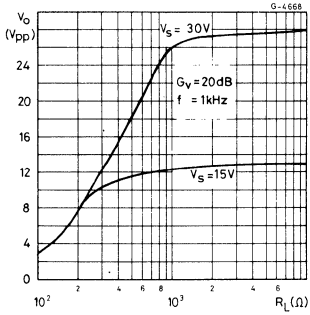


Fig. 6 - Power bandwidth

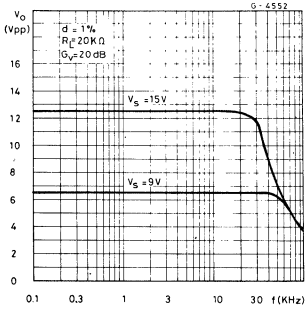


Fig. 7 - Total harmonic distortion vs. output voltage

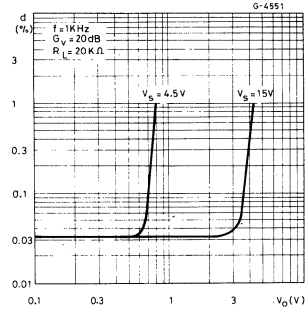


Fig. 8 - Total input noise vs. source resistance

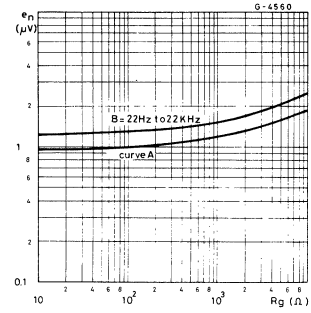


Fig. 9 - Noise density vs. frequency

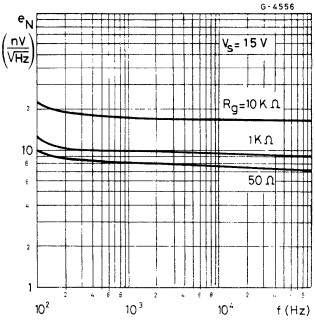


Fig. 10 - RIAA preamplifier response (circuit of fig. 12)

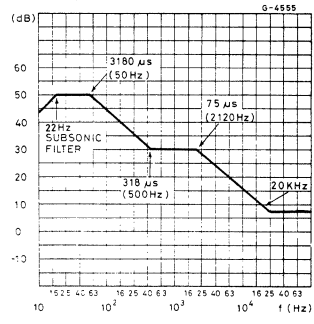
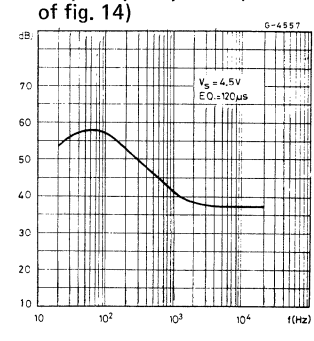


Fig. 11 - Tape preamplifier frequency response (circuit of fig. 14)



APPLICATION INFORMATION

Fig. 12 - Stereo RIAA preamplifier

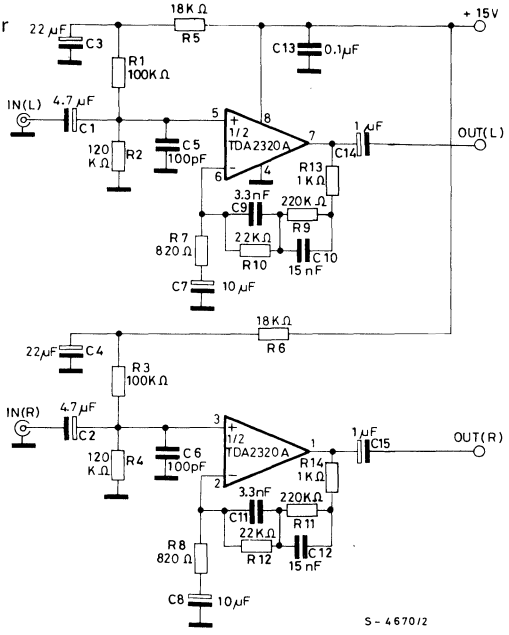
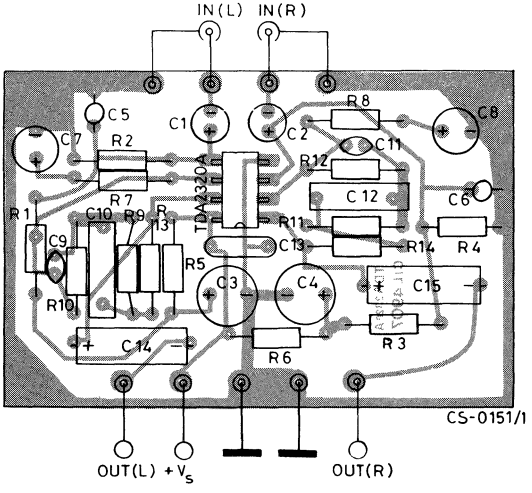


Fig. 13 - P.C. board and components layout of the circuit of fig. 12



APPLICATION INFORMATION (continued)

Fig. 14 - Stereo preamplifier for Walkman cassette players

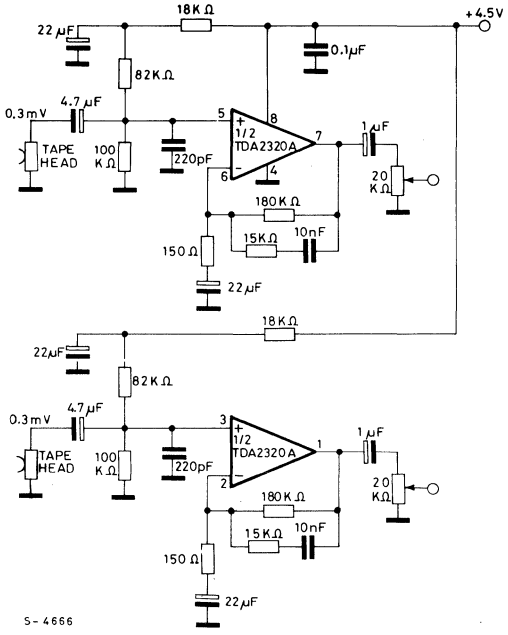


Fig. 15 - Second order 2 KHz Butterworth crossover filter for Hi-Fi active boxes

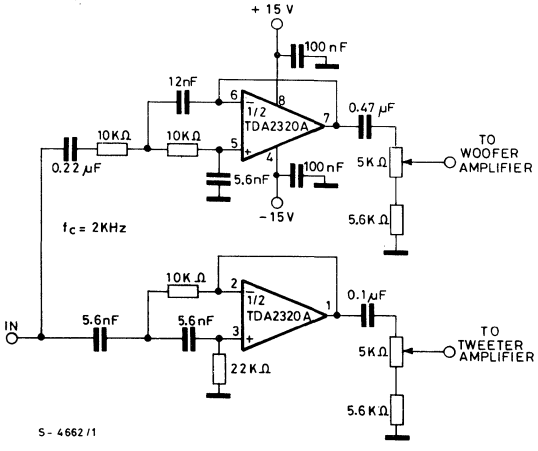
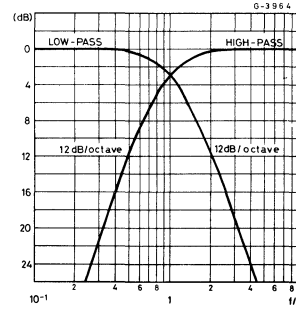


Fig. 16 - Frequency response (circuit of fig. 15)



APPLICATION INFORMATION (continued)

Fig. 17 - Third order 2.8 KHz Bessel crossover filter for Hi-Fi active boxes

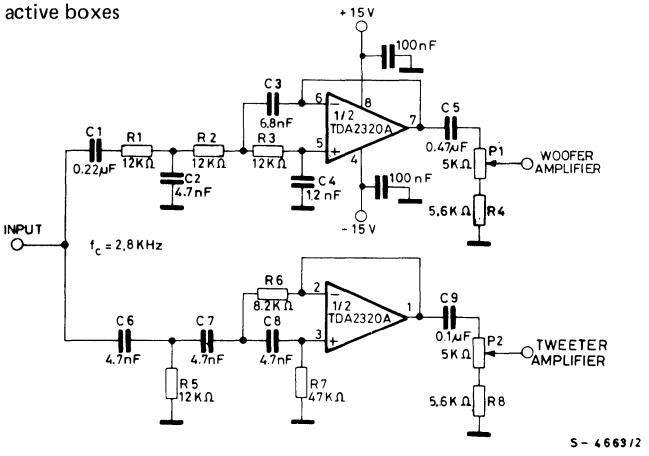


Fig. 18 - Frequency response (circuit of fig. 17)

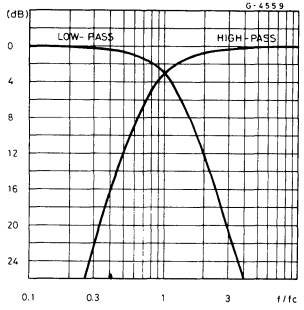


Fig. 19 - 200 Hz to 2 KHz Active Bandpass Filter for midrange speakers

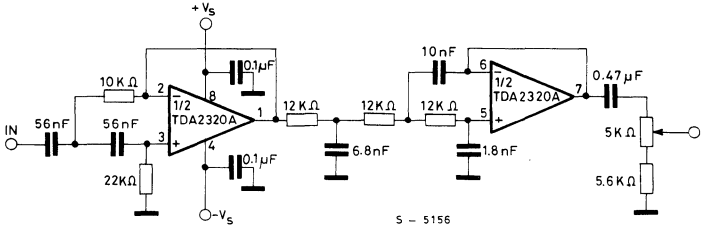
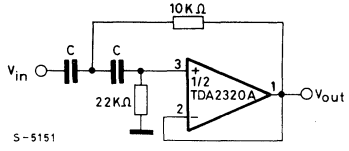
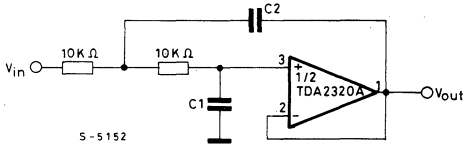


Fig. 20 - Subsonic or rumble filter



f_c (Hz)	C (μF)
15	0.68
22	0.47
30	0.33
55	0.22
100	0.1

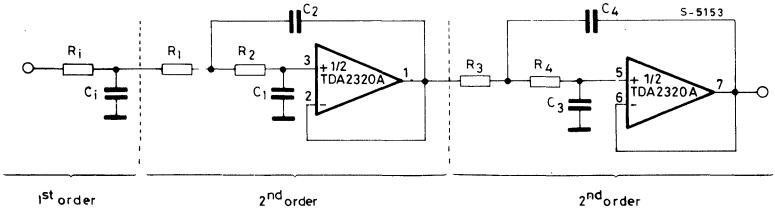
Fig. 21 - High-cut filter



f_c (KHz)	C1 (nF)	C2 (nF)
3	3.9	6.8
5	2.2	4.7
10	1.2	2.2
15	0.68	1.5

APPLICATION INFORMATION (continued)

Fig. 22 - Fifth order 3.4 KHz low-pass Butterworth filter



For f_c = 3.4 KHz and R_i = R1 = R2 = R3 = R4 = 10 KΩ, we obtain:

$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33$ nF

$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97$ nF

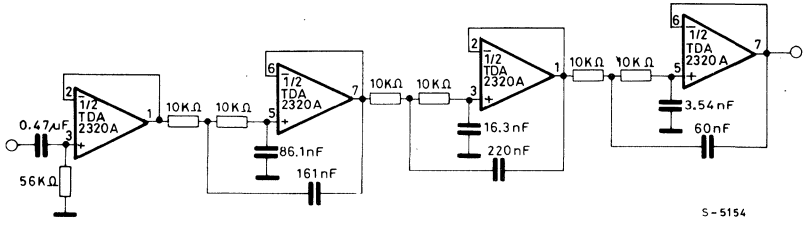
$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20$ nF

$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45$ nF

$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14$ nF

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 23 - Sixth-pole 355 Hz low-pass filter (Chebychev type)



This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

APPLICATION INFORMATION (continued)

Fig. 24 - Three band tone control

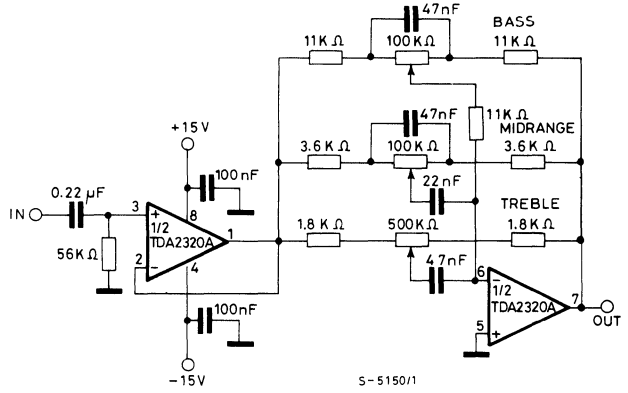
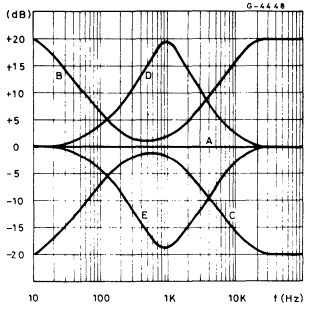


Fig. 25 - Frequency response of the circuit of fig. 24.

A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat



TDA3190

LINEAR INTEGRATED CIRCUIT

COMPLETE TV SOUND CHANNEL

The TDA3190 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It performs all the functions needed for the TV sound channel:

- IF limiter--amplifier
- Active low-pass filter
- FM detector
- DC volume control
- AF preamplifier
- AF output stage

The TDA 3190 can give an output power of 4.2W (d = 10%) into a 16Ω load at V_s= 24V, or 1.5W (d = 10%) into an 8Ω load at V_s= 12V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.
The TDA 3190 is a pin to pin replacement of TDA 1190Z.

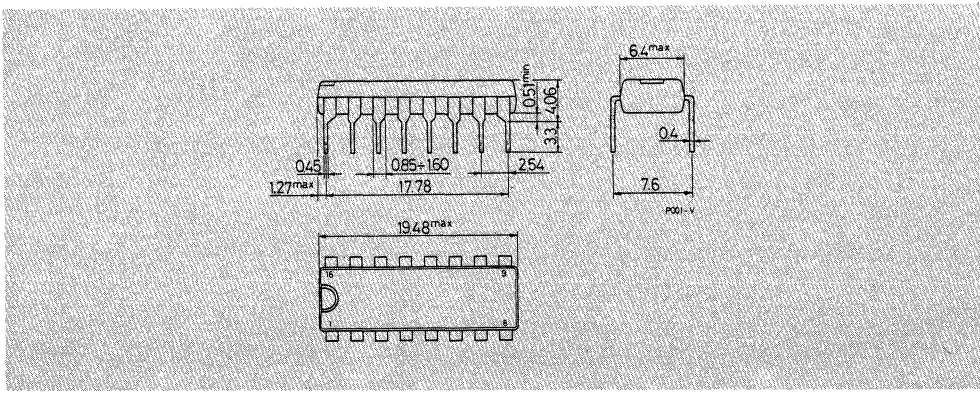
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 10)	28	V
V_i	Input signal voltage (pin 1)	1	V
I_o	Output peak current (non-repetitive)	2	A
I_o	Output peak current (repetitive)	1.5	A
P_{tot}	Power dissipation: at T_{pins} = 90°C	4.3	W
	at T_{amb} = 70°C (free air)	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

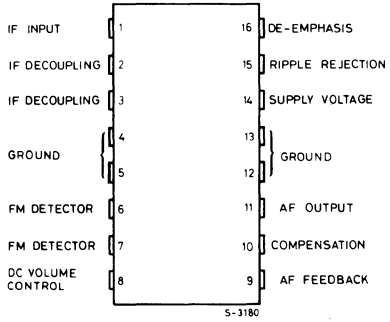
ORDERING NUMBERS: TDA 3190

MECHANICAL DATA

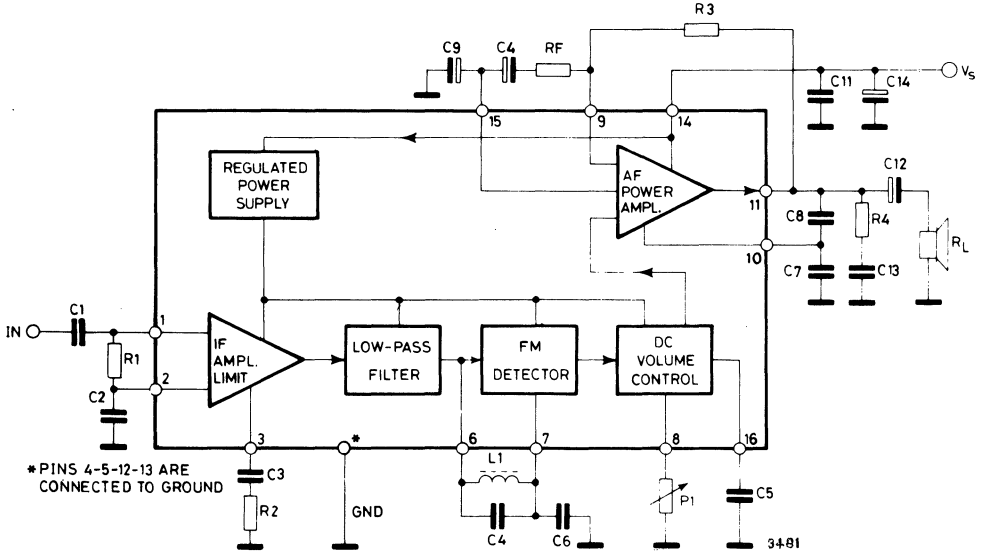
Dimensions in mm



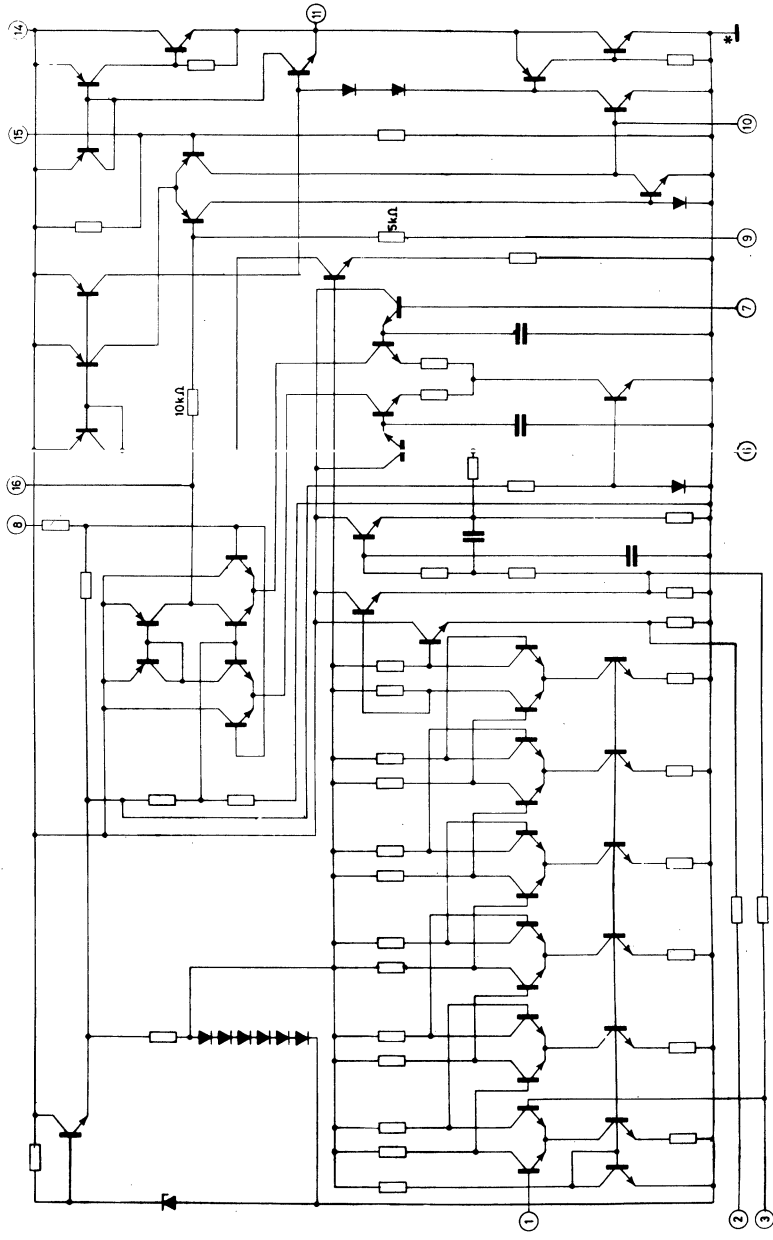
CONNECTION DIAGRAM



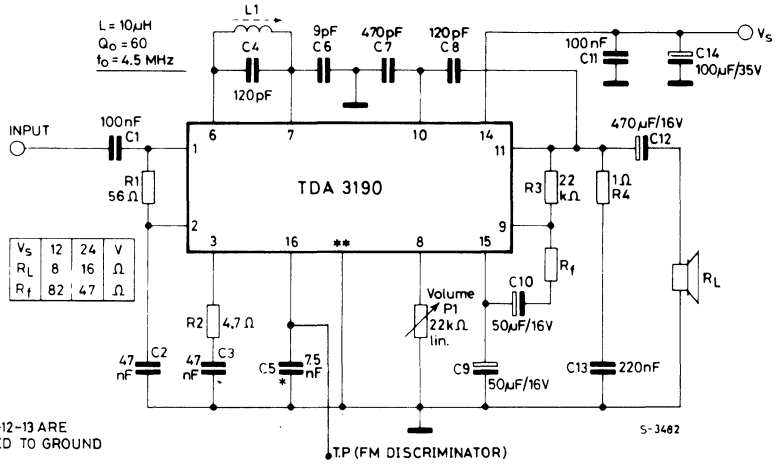
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80*	°C/W

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= 24V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 14)		9		28	V
V_o	Quiescent output voltage (pin 11)	V_s= 24V V_s= 12V	11 5.1	12 6	13 6.9	V V
I_d	Quiescent drain current	P_1 = 22KΩ V_s = 24V V_s = 12V	11	22 19	45 40	mA mA
P_o	Output power	d = 10% f_m= 400 Hz f_o= 4.5 MHz Δf = ± 25 KHz V_s = 24V R_L= 16Ω V_s = 12V R_L= 8Ω		 4.2 1.5		 W W
		d = 2% f_m= 400 Hz f_o = 4.5 MHz Δf= ± 25 KHz V_s = 24V R_L= 16Ω V_s = 12V R_L= 8Ω		 3.5 1.4		 W W

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_i	Input limiting voltage (-3 dB) at pin 1	f_o = 4.5 MHz Δf = ± 7.5 KHz f_m= 400 Hz P_1 = 0		40	100	μV
d	Distortion	P_o = 50 mW f_m= 400 Hz f_o = 4.5 MHz Δf = ± 7.5 KHz V_s = 24V R_L= 16Ω V_s = 12V R_L= 8Ω		0.75 1		% %
B	Frequency response of audio amplifier (-3 dB)	R_L = 16Ω C_8= 120 pF C_7= 470 pF P_1= 22 KΩ R_f = 82Ω R_f = 47Ω		70 to 12000 70 to 7000		Hz Hz
V_o	Recovered audio voltage (pin 16)	V_i ⩾ 1 mV f_o = 4.5 MHz f_m= 400 Hz Δf = ± 7.5 KHz P_1 = 0		120		mV
AMR	Ampliture modulation rejection	V_i ⩾ 1 mV f_o = 4.5 MHz f_m= 400 Hz Δf = ± 25 KHz m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to noise ratio	V_i ⩾ 1 mV V_o = 4V f_o = 4.5 MHz f_m= 400 Hz Δf = ± 25 KHz	50	65		dB
R_3	External feedback resistance (between pins 9 and 11)				25	KΩ
R_i	Input resistance (pin 1)	V_i = 1 mV f_o = 4.5 MHz		30		KΩ
C_i	Input capacitance (pin 1)			5		pF
SVR	Supply voltage rejection	R_L = 16Ω f_{ripple}= 120 Hz P_1 = 22 KΩ		46		dB
A_V	DC volume control attenuation	P_1 = 12 KΩ		90		dB

Fig. 1 - Relative audio output voltage and output noise vs. input signal.

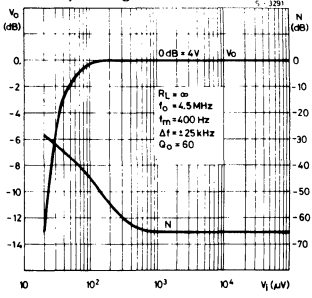


Fig. 2 - Output voltage attenuation vs. DC volume control resistance.

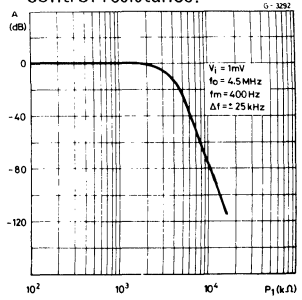


Fig. 3 - Amplitude modulation rejection vs. input signal

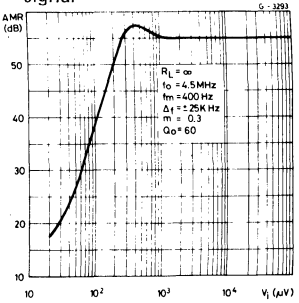


Fig. 4 - ΔAMR vs. tuning frequency change.

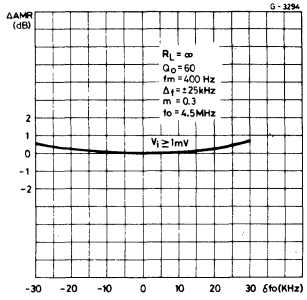


Fig. 5 - Recovered audio voltage vs. unloaded Q factor of the detector coil

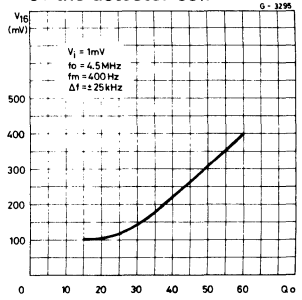


Fig. 6 - Distortion vs. output power

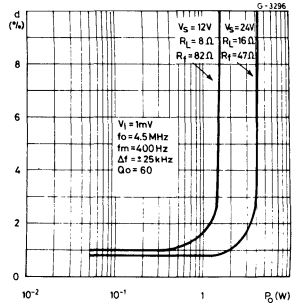


Fig. 7 - Distortion vs. frequency deviation

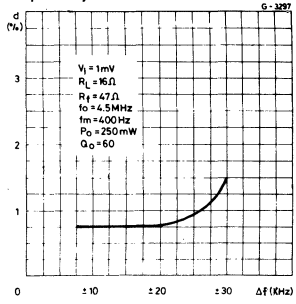


Fig. 8 - Distortion vs. tuning frequency change

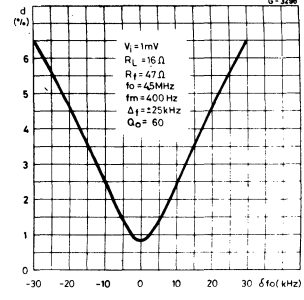


Fig. 9 - Audio amplifier frequency response

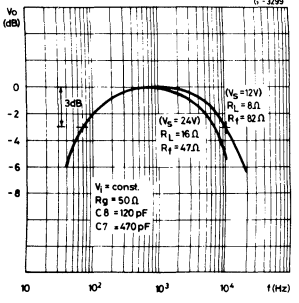


Fig. 10 - Supply voltage ripple rejection vs. ripple frequency

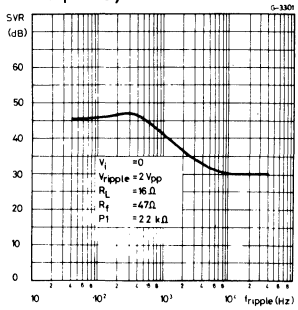


Fig. 11 - Supply voltage ripple rejection vs. volume control attenuation

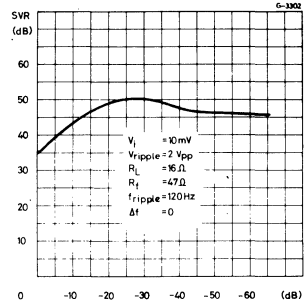


Fig. 12 - Output power vs. supply voltage

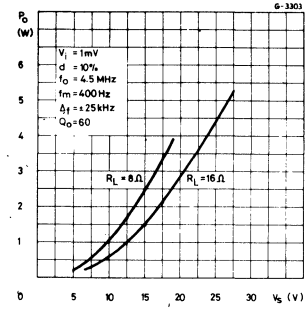


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

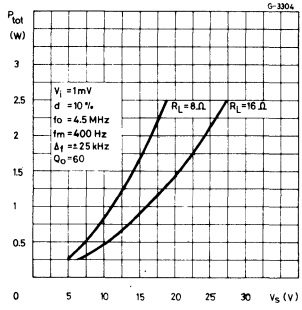


Fig. 14 - Power dissipation and efficiency vs. output power

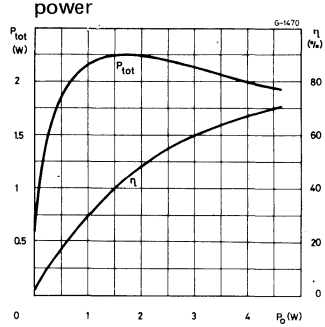
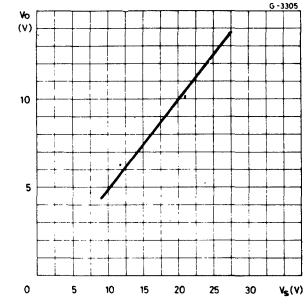


Fig. 15 - Quiescent output voltage (pin 11) vs. supply voltage



APPLICATION INFORMATION

The electrical characteristics of the TDA 3190 remain almost constant over the frequency range 4.5 to 6 MHz, therefore it can be used in all television standards (FM mod.). The TDA 3190 has a high input impedance, so it can function with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 9, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier, must enter into clipping.

Capacitor C8, connected between pins 10 and 11, determines the upper cutoff frequency of the audio bandwidth. To increase the bandwidth the values of C8 and C7 must be reduced, keeping the ratio C7/C8 as shown in the table of fig. 16.

The capacitor connected between pin 16 and ground, together with the internal resistor of 10 KΩ forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by the inductive load and the wires connecting the loudspeaker.

APPLICATION INFORMATION (continued)

Fig. 16 - Typical application circuit

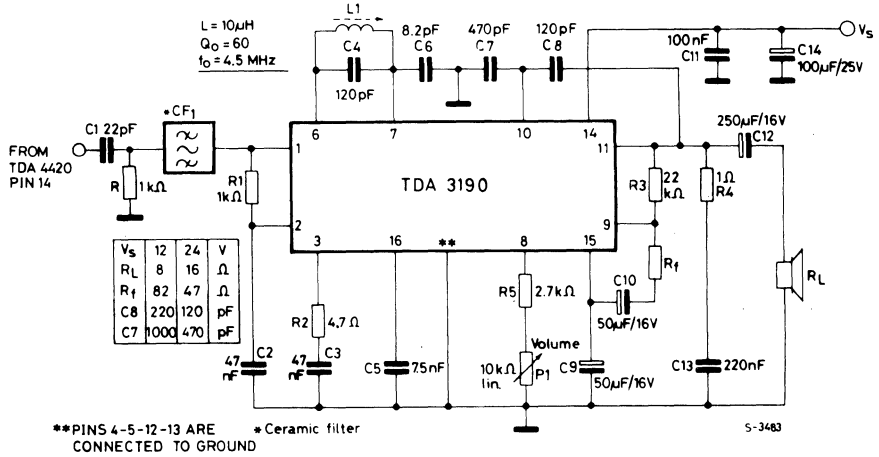
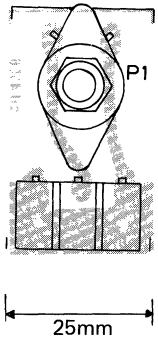
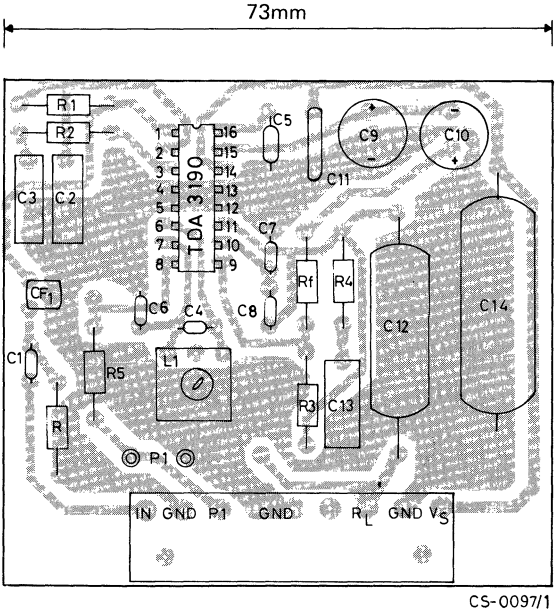


Fig. 17 - P.C. board and component layout of the circuit shown in Fig. 16 (1:1 scale)





CS-0097/1

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the TDA 3190 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 18) or to an external heatsink (Fig. 19).
The diagram of figure 20 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 18 - Example of P.C.board copper area which is used as heatsink.

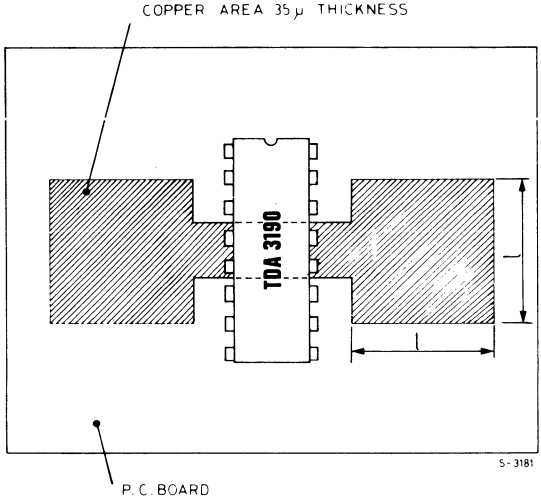


Fig. 19 - External heatsink mounting example

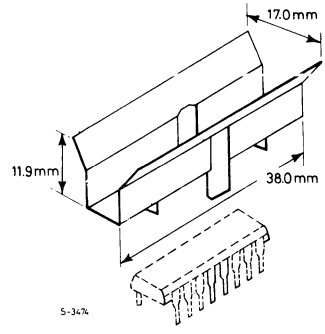


Fig. 20 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

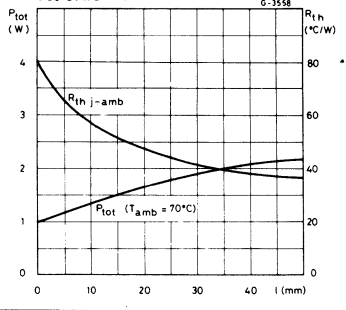
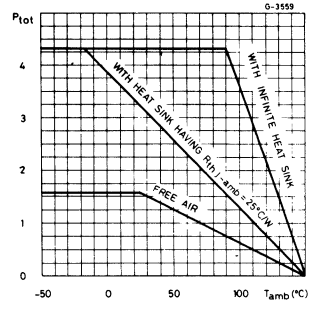


Fig. 21 - Maximum allowable power dissipation vs. ambient temperature



LINEAR INTEGRATED CIRCUIT

TDA3410

DUAL LOW NOISE TAPE PREAMPLIFIER WITH AUTOREVERSE

The TDA 3410 is a dual preamplifier with tape autoreverse facility for the amplification of low level signals in applications requiring very low noise performance, as stereo cassette players. Each channel consists of two independent amplifiers. The first has a fixed gain of 30 dB while the second one is an operational amplifier optimized for high quality audio application.
The TDA 3410 is a monolithic integrated circuit in a 16-lead dual in-line plastic package and its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Wide supply range
- SVR = 120 dB
- Large output voltage swing
- Tape autoreverse facility
- Short circuit protection

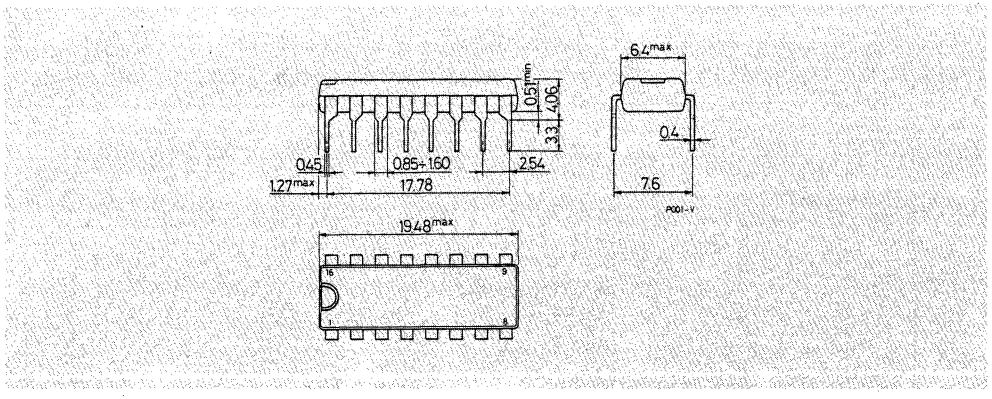
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
P_{tot}	Total power dissipation at T_{amb} = 60°C	600	mW
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

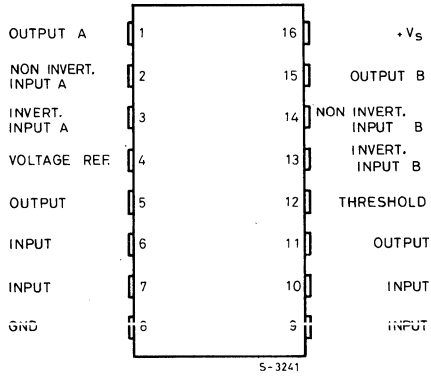
ORDERING NUMBER: TDA 3410

MECHANICAL DATA

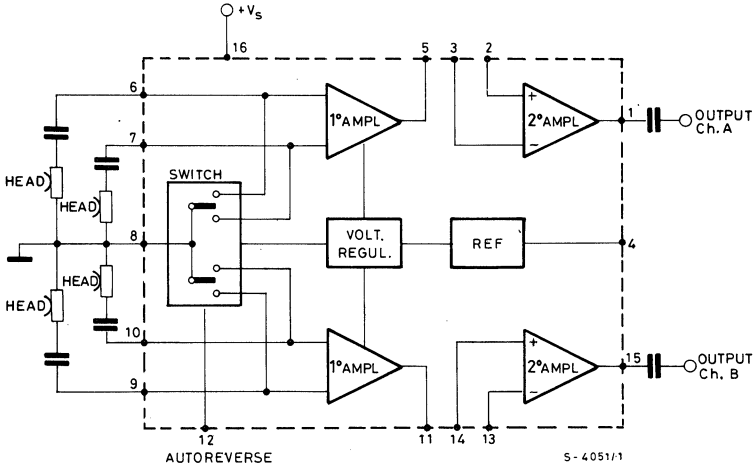
Dimensions in mm



CONNECTION DIAGRAM (top view)



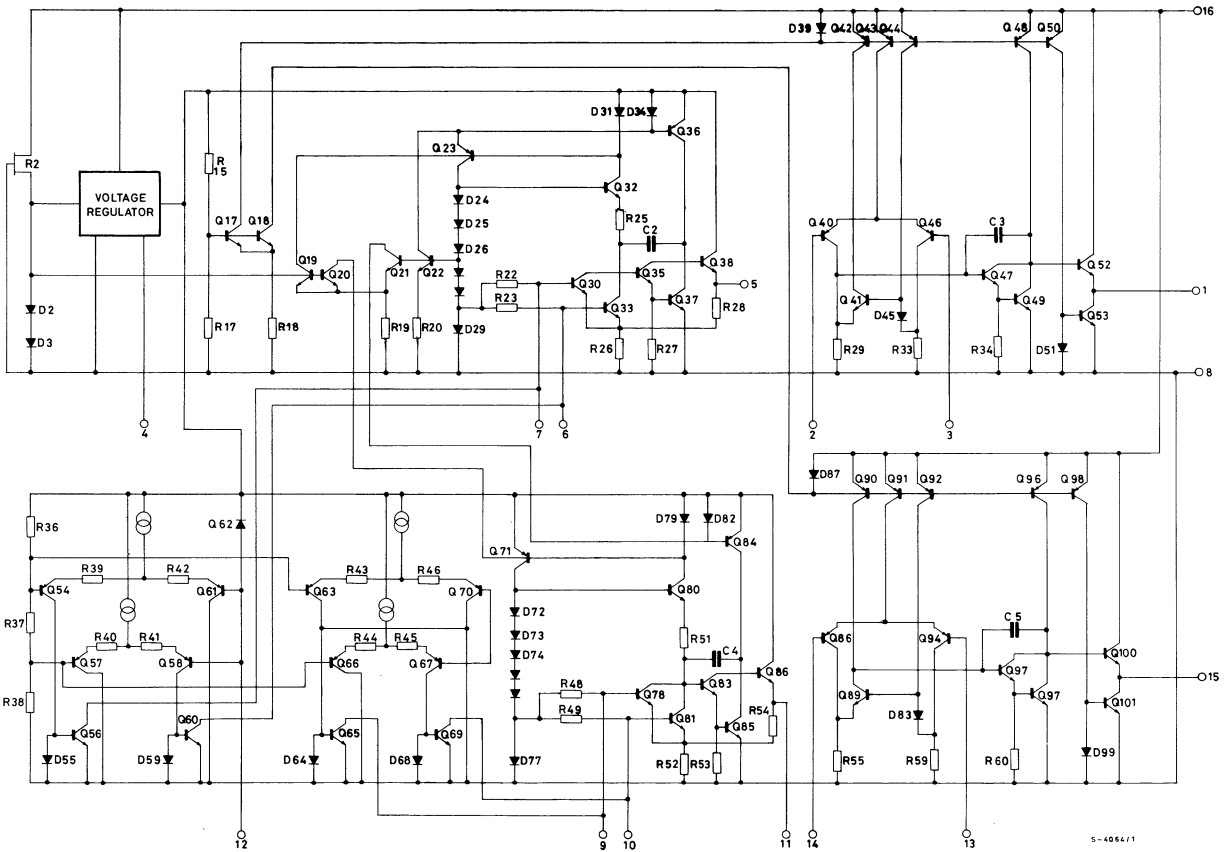
BLOCK DIAGRAM



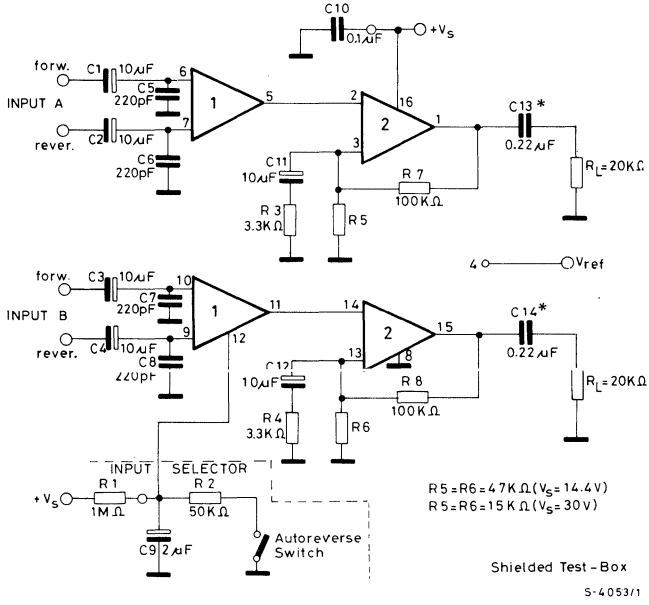
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150	°C/W

SCHEMATIC DIAGRAM



TEST CIRCUIT (Flat Gain - G_v= 60 dB)



* Mylar or polycarbonate capacitors.

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s= 14.4V, G_v= 60 dB, refer to the test circuit, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_s	Supply current	V_s= 8V to 30V		10		mA
I_o	Output current (pins 1-15)	Source V_s= 8V to 30V		10		mA
		Sink		1		mA
G_v	Closed loop gain	f = 20 Hz to 20 KHz		60		dB
R_i	Input resistance	f = 1 KHz	50	80		KΩ
R_o	Output resistance (pins 1-15)	f = 1 KHz		50		Ω
THD	Total harmonic distortion	V_o= 300 mV f = 1 KHz		0.05		%
		f = 10 KHz		0.05		%

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage swing (pins 1-15)	Peak to Peak V_s= 14.4V V_s= 30V		12 28		.V V
V_o	Output voltage (pins 1-15)	d = 0.5% V_s= 14.4V f = 1 KHz V_s= 30V		4 8		V_{rms} V_{rms}
e_n	Total input noise (°)	R_g= 50Ω R_g= 600Ω R_g= 5KΩ		0.25 0.4 1.3	0.6	μV μV μV
S/N	Signal to noise ratio (°)	V_{in}= 0.3 mV R_g= 600Ω V_{in}= 1 mV R_g= 0		57 73		dB dB
CS	Channel separation	f = 1 KHz		60		dB
CT(°°°)	Cross-talk (differential input)	f = 1 KHz		80		dB
SVR	Supply voltage rejection (°°)	f = 1 KHz R_g= 600Ω		120		dB
SVR (°°)	Of reference voltage (Pin 4)	f = 1 KHz R_g= 600Ω		100		dB
V_{ref}	Reference voltage (pin 4)			55		mV
R_{ref}	Ref. voltage output resistance (pin 4)			100		Ω
$\frac{\Delta V_{ref}}{\Delta T}$	Voltage temperature coefficient			10		μV/°C

(°) The weighting filter used for the noise measurement has a curve A frequency response.
(°°) Referred to the input.
(°°°) Between a disabled input and an input ON.

ELECTRICAL CHARACTERISTICS (Refer test circuit, V_s= 30V)

AMPLIFIER N° 1

Parameter		Test conditions	Min.	Typ.	Max.	Unit
G_v	Gain (pins 6 to 5)		29	30	30.5	dB
d	Distortion	V_o= 300 mV f = 1 KHz f = 10 KHz		0.05 0.05		%
e_n	Total input noise (°)	R_g= 600Ω		0.4		μV
Z_o	Output impedance (pin 5)	f = 1 KHz		100		Ω
I_o	Output current (pin 5)			1		mA
V_5	DC output voltage (pin 5)	V_s = 10V	1.3	2	2.7	V

AMPLIFIER N° 2

G_v	Open loop voltage gain (pins 2 to 1)			100		dB
I_B	Input bias current			0.2		μA
V_{os}	Input offset voltage			2		mV
I_{os}	Input offset current			0.05		μA
BW	Small signal bandwidth	G_v= 30 dB		150		KHz
e_n	Total input noise (°)	R_g= 600Ω		2		μV
R_i	Input impedance	f = 1 KHz (open loop)	150	500		KΩ

AUTOREVERSE

P_{in}	$V_{12} < 2V$	$V_{12} > 4.5V$
6 – 10	OFF	ON
7 – 9	ON	OFF

(°) The weighting filter used for the noise measurement has a curve A frequency response.

Fig. 1 - Total input noise vs. source resistance (curve A)

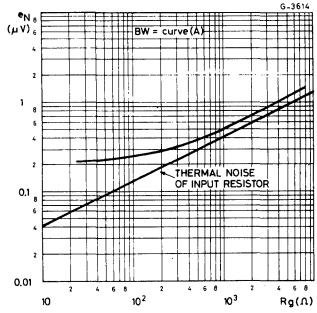


Fig. 2 - Total input noise vs. source resistance (BW= 22 Hz to 22 KHz)

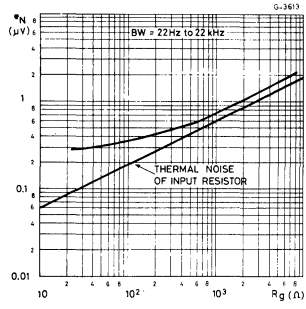


Fig. 3 - Total harmonic distortion vs. output voltage

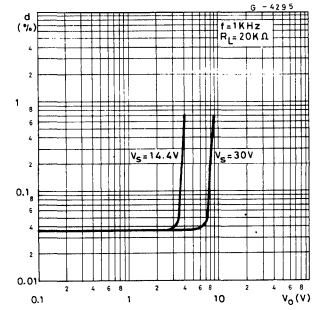


Fig. 6 - Very low noise stereo preamplifier for car cassette players (with Gap Loss Correction and autoreverse function)

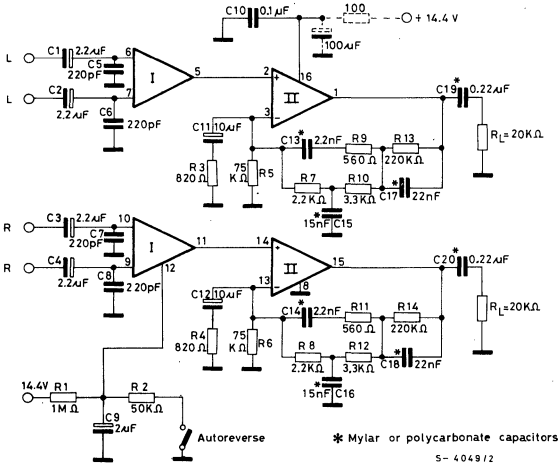


Fig. 5 - Frequency response

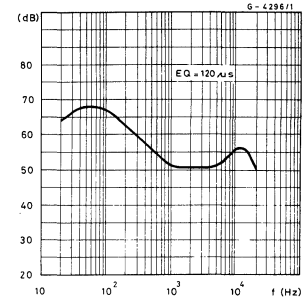


Fig. 6 - P.C. board and component lay-out (1:1 scale) for the circuit of fig. 4

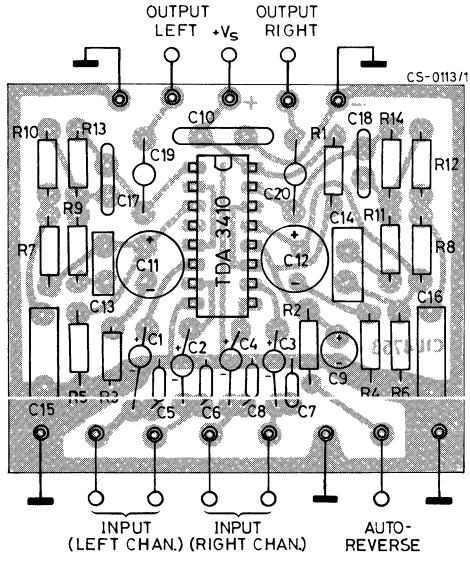


Fig. 7 - Stereo preamplifier for car cassette players, with low value capacitors (Autoreverse function)

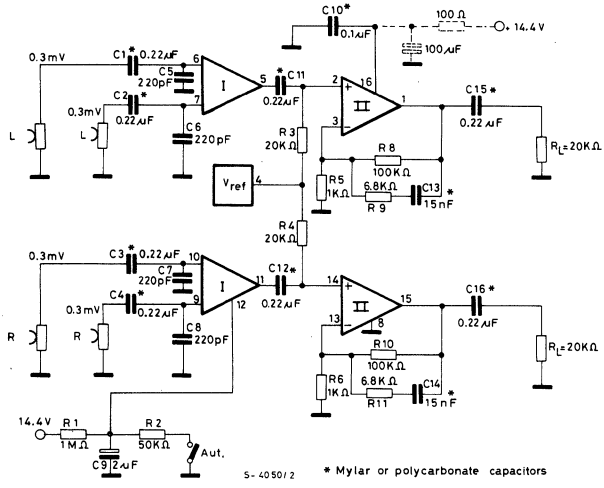
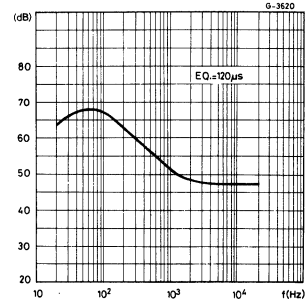


Fig. 8 - Frequency response



LINEAR INTEGRATED CIRCUIT

TDA3420

PRELIMINARY DATA

DUAL VERY LOW NOISE PREAMPLIFIER

The TDA 3420 is a dual preamplifier for applications requiring very low noise performance, **as stereo cassette players** and quality audio systems. Each channel consists of two independent amplifiers.
The first one has a fixed gain while the second one is an operational amplifier for audio application.
The TDA 3420 is available in two packages: 16-lead daul in-line plastic and 16 lead micropackage.
Its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Large output voltage swing
- Short circuit protection

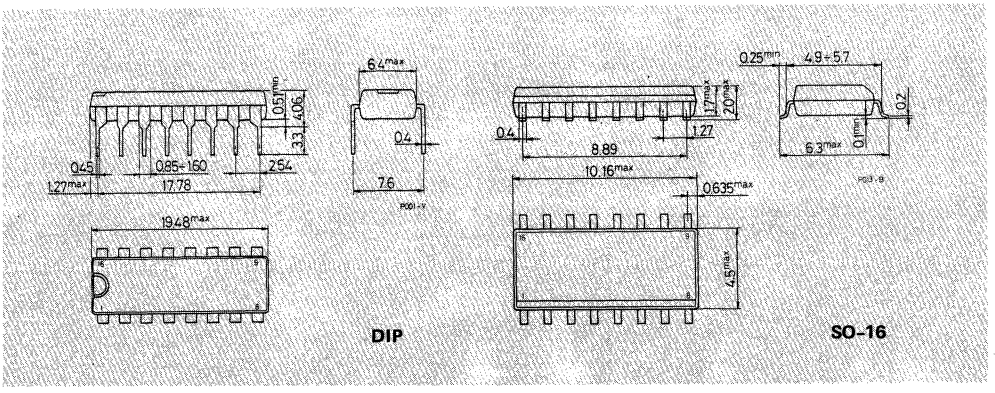
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
P_{tot}	Total power dissipation at T_{amb} = 70°C Dip	530	mW
	SO-16	400	mW
T_j, T_{stg}.	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBERS: TDA 3420 (DIP)
L 343M (SO-16)

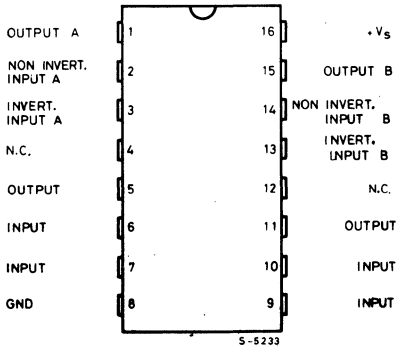
MECHANICAL DATA

Dimensions in mm

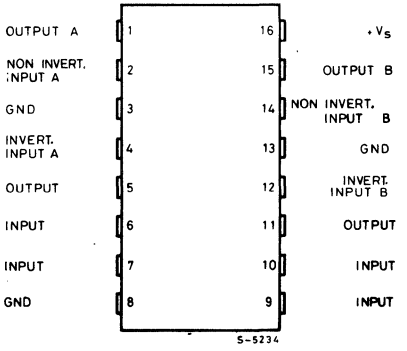


TDA3420

CONNECTION DIAGRAMS

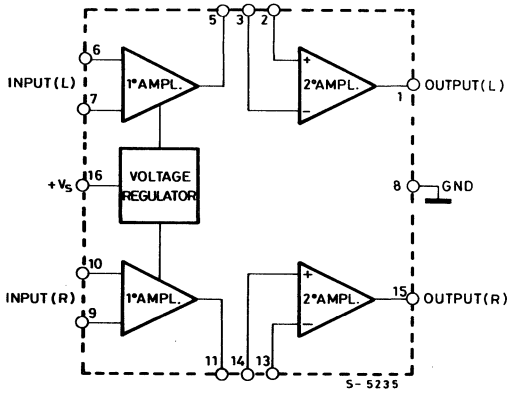


DIP



SO-16

BLOCK DIAGRAM (Pin numbers refer to the DIP)

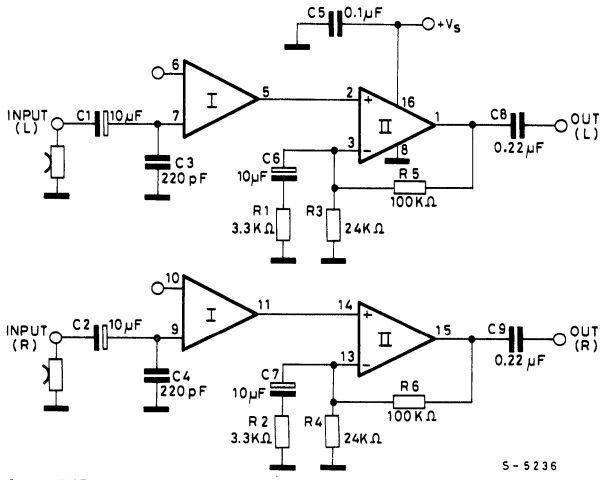


THERMAL DATA

			DIP	SO-16
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	150 °C/W	200°C/W *

* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

Fig. 1 - Test circuit



Note: Pin numbers refer to DIP.

Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1:1 scale)

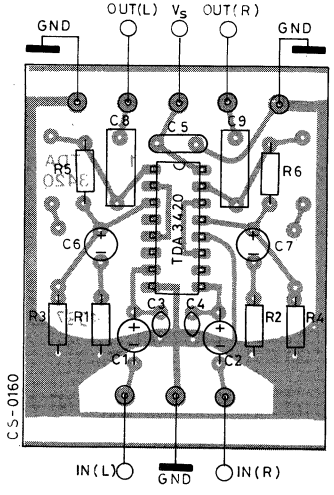
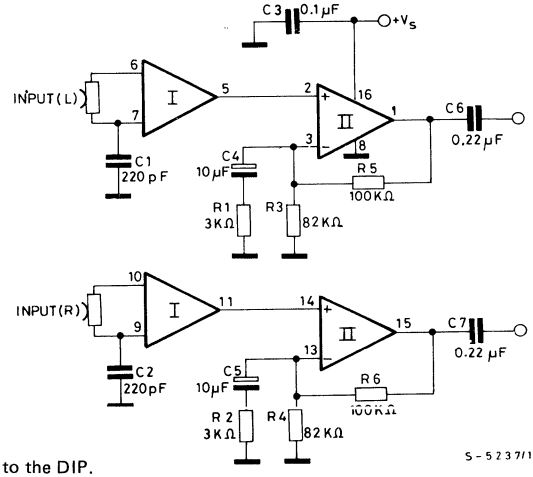


Fig. 3 - Test circuit without input capacitors



Note: Pin numbers refer to the DIP.

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, V_s= 14.4V, G_v= 60 dB refer to the test circuit of fig. 1, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_s	Supply current	V_s= 8V to 20V			8		mA
I_o	Output current	Source	V_s= 8V to 20V		10		mA
		Sink			1		mA
G_v	Gain	f = 1 KHz			60		dB
R_i	Input resistance			50	100		KΩ
R_o	Output resistance				50		Ω
THD	Total harmonic distortion without noise	V_o= 300 mV	f = 1 KHz		0.05		%
			f = 10 KHz		0.05		%

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Peak to peak output voltage	f = 40 Hz to 15 KHz		12		V
e_n	Total input noise (°)	R_s= 50 Ω R_s= 600 Ω R_s= 5 KΩ		0.25 0.4 1.3	0.7	μV μV μV
S/N	Signal to noise ratio (°)	V_{in}= 0.3 mV R_s= 600 Ω V_{in}= 1 mV R_s= 0		57 73		dB
	(°°)	V_{in}= 0.3 mV R_s= 600 Ω V_{in}= 1 mV R_s= 0		55 71		dB
CS	Channel separation	f = 1 KHz		60		dB
SVR	Supply voltage rejection (°°°)	f = 1 KHz R_s= 600 Ω		110		dB

(°) Weighting filter : curve A.
(°°) Weighting filter : Dolby CCIR/ARM.
(°°°) Referred to the input.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit of fig. 1, V_s= 14.4V)

AMPLIFIER N° 1

Parameter		Test conditions	Min.	Typ.	Max.	Unit
G_v	Gain (pin 6 to pin 5)		27.5	28.5	29	dB
d	Distortion	V_o= 300 mV f = 1 KHz f = 10 KHz		0.05 0.05		%
e_n	Total input noise (°)	R_s= 600Ω		0.4		μV
Z_o	Output impedance (pin 5)	f = 1 KHz		100		Ω
I_o	Output current (pin 5)			1		mA
V5	DC output voltage (pin 5)	Test circuit fig. 3		2.8		V
		Test circuit fig. 1	1.0	1.5		

(°) Weighting filter: curve A.

ELECTRICAL CHARACTERISTICS (continued)

AMPLIFIER N° 2

Parameter		Test conditions	Min.	Typ.	Max.	Unit
G_v	Open loop voltage gain			100		dB
I_B	Input bias current			0.2		μA
V_{os}	Input offset voltage			2		mV
I_{os}	Input offset current			50		nA
e_n	Total input noise (°)	R_s= 600Ω		2		μV
R_i	Input impedance	f = 1 KHz (open loop)	150	500		KΩ

(°) Weighting filter: curve A.

Fig. 4 - Total input noise vs. source resistance (curve A)

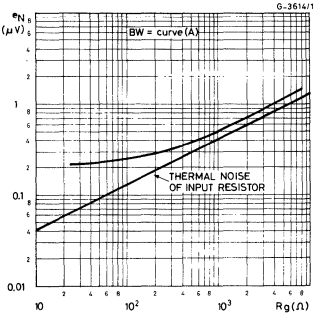


Fig. 5 - Total input noise vs. source resistance(BW=22Hz to 22 KHz)

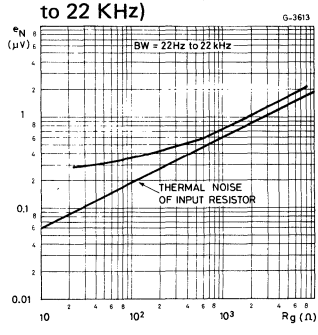


Fig. 6 - Total harmonic distortion vs. output voltage

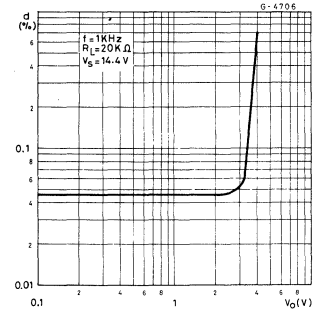


Fig. 7 - Output voltage vs. frequency

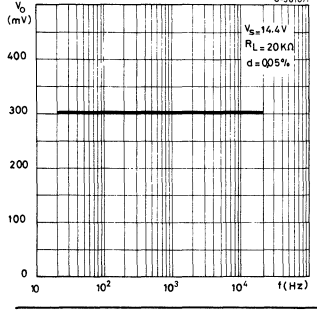


Fig. 8 - Distortion vs. input level (test circuit of fig. 1)

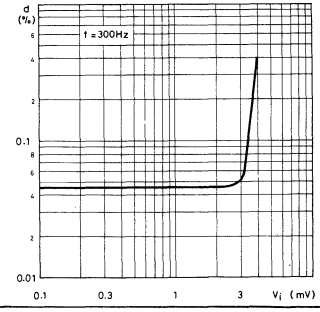


Fig. 9 - Frequency response of the circuit of fig. 10

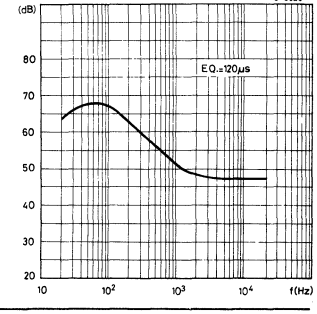


Fig. 10 - Very low noise stereo preamplifier for cassette players

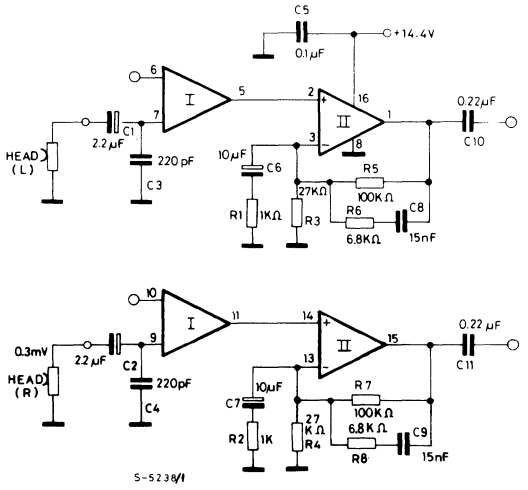
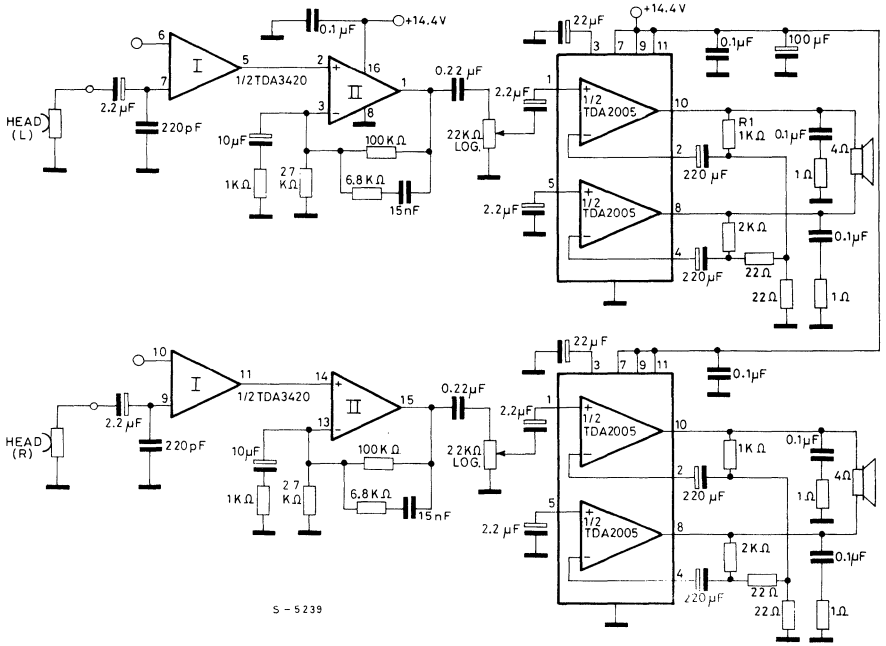


Fig. 11 - Complete 20 + 20W stereo tape playback system



TDA4092

LINEAR INTEGRATED CIRCUIT

PRELIMINARY DATA

5 BIT BINARY TO 7-SEGMENT DECODER DRIVER

- ROM MASK OPTION
- STANDARD CONFIGURATION FOR 2 DIGIT 7-SEGMENT LED TO PRESENT THE NUMBERS 1 TO 32
- CONSTANT CURRENT OUTPUT STAGES FOR DIRECT DRIVING OF COMMON ANODE LEDs
- OUTPUT PROVIDED TO DISPLAY THE STAND-BY MODE
- $\overline{AV}$ OUTPUT ACTIVATED WHENEVER PROGRAM 32 IS SELECTED
- TTL COMPATIBLE INPUTS
- 5V SUPPLY VOLTAGE

The TDA 4092 is a monolithic integrated circuit designed to display the program number (1 to 32) in TV or Radio sets in conjunction with voltage or frequency synthesizers. The inputs accept a 5 bit binary code with TTL levels and have internal pull-up.

The outputs can directly drive LED display elements with common anode.

One of these outputs is intended to display the stand-by mode of the set.

No external resistors are required if the LEDs are supplied at 5V.

The LEDs can also be supplied with higher voltage (up to 18V) but in this case a single resistor in series with the LED elements must be used in order to limit the power dissipation of the IC; moreover, a suitable R_{ext} must be chosen.

The circuit is produced in I^2L technology and is available in a 24 pin dual in-line plastic package.

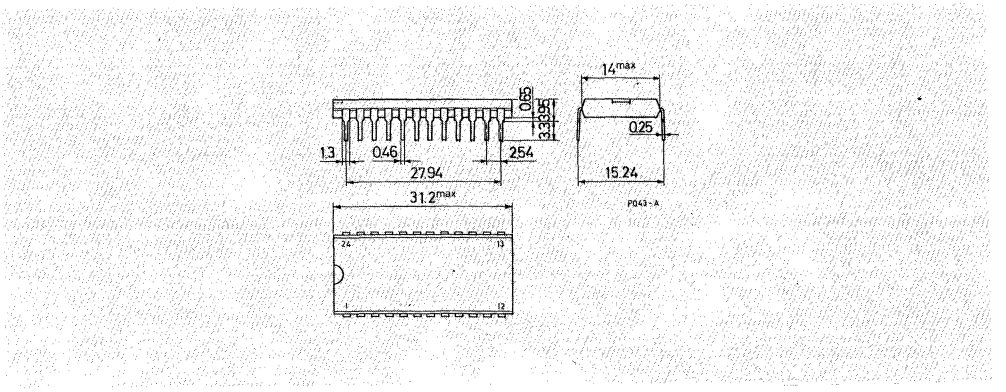
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	10	V
V_I	Input voltage	10	V
$V_{O\,(off)}$	Off state output voltage	20	V
I_{OL}	Output current	22	mA
P_{tot}	Total power dissipation at $T_{amb} = 55°C$	0.8	W
T_{stg}, T_j	Storage and junction temperature	-25 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

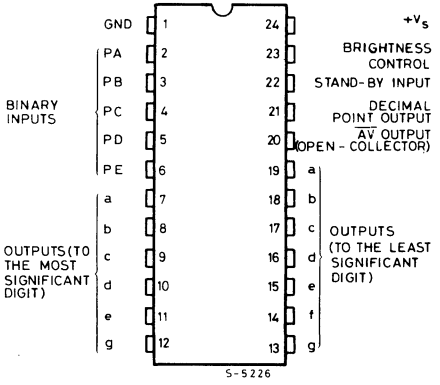
ORDERING NUMBER: TDA 4092

MECHANICAL DATA

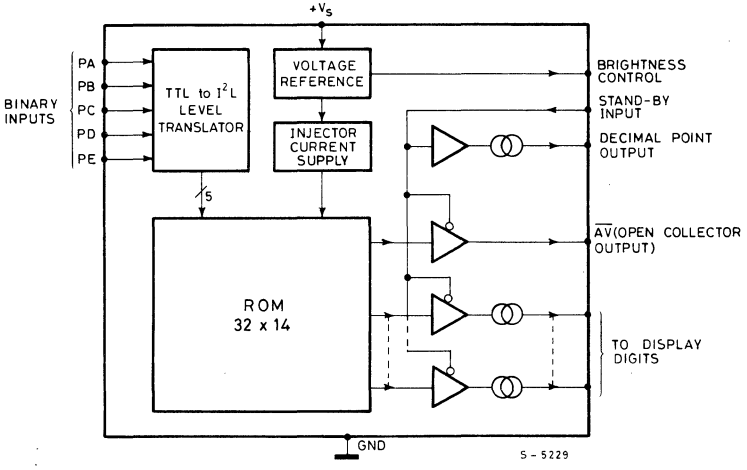
Dimensions in mm



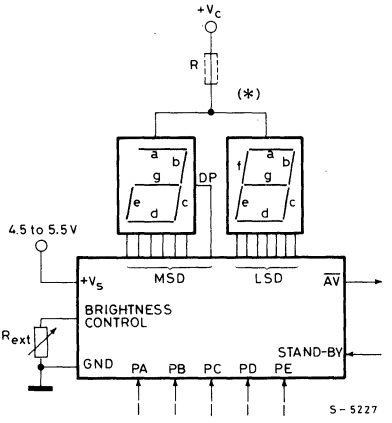
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



APPLICATION CIRCUIT



(*) R is necessary only with V_c greater than 5.5V.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction ambient	max	120	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 5V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4.5		5.5	V
I_s	Quiescent supply current	V_s= 5.5V			20	28	mA
V_{IH}	High level input voltage	T_{amb}= 0 to 70°C		2			V
V_{IL}	Low level input voltage	T_{amb}= 0 to 70°C				0.8	V
I_{IH}	High level input current	T_{amb}= 0 to 70°C V_s = 5.5V	V_{IH}= 2V			100	nA
I_{IL}	Low level input current		V_{IL}= 0.8V		-50	-200	μA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{out}	Output voltage	I_o= 15 mA	2			V
V_{AV}	AV output voltage (pin 20)	(All the binary inputs high) I_{AV}= 1.6 mA		50	260	mV
I_B	Pin 23 input current (Brightness control)	R_{ext}= 3.3 KΩ		-375		μA
		R_{ext}= 5.6 KΩ		-225		
I_o	Output current (*)	R_{ext}= 3.3 K	13.5	15	16.5	mA
		R_{ext}= 5.6 K	8	9	10	
I_{DP}	Output current for decimal point (pin 21)(**)			12.5		mA
$\frac{\Delta I_o}{I_o}/\Delta V_s$	Segment current stability	I_o = 15 mA V_s= 4.5 to 5.5V		0.2		%

(*) $I_o = 40 \cdot I_B$
(**) I_{DP} is fixed and independent of R_{ext} value.

FUNCTION TABLE

INPUTS						OUTPUTS														
							ten's digit (MSD)						unit's digit (LSD)							
A	B	C	D	E	Standby	Number displayed	a	b	c	d	e	g	a	b	c	d	e	f	g	DP	$\overline{AV}$*
L	L	L	L	L	L	1								on	on						
H	L	L	L	L	L	2							on	on		on	on		on		
L	H	L	L	L	L	3							on	on	on	on			on		
H	H	L	L	L	L	4								on	on			on	on		
L	L	H	L	L	L	5							on		on	on		on	on		
H	L	H	L	L	L	6							on		on	on	on	on	on		
L	H	H	L	L	L	7							on	on	on						
H	H	H	L	L	L	8							on	on	on	on	on	on	on		
L	L	L	H	L	L	9							on	on	on	on		on	on		
H	L	L	H	L	L	10		on	on				on	on	on	on	on	on			
L	H	L	H	L	L	11		on	on					on	on						
H	H	L	H	L	L	12		on	on				on	on		on	on		on		
L	L	H	H	L	L	13		on	on				on	on	on	on			on		
H	L	H	H	L	L	14		on	on					on	on			on	on		
L	H	H	H	L	L	15		on	on				on		on	on		on	on		
H	H	H	H	L	L	16		on	on				on		on	on	on	on	on		
L	L	L	L	H	L	17		on	on				on	on	on						
H	L	L	L	H	L	18		on	on				on	on	on	on	on	on	on		
L	H	L	L	H	L	19		on	on				on	on	on	on		on	on		
H	H	L	L	H	L	20	on	on		on	on	on	on	on	on	on	on	on			
L	L	H	L	H	L	21	on	on		on	on	on		on	on						
H	L	H	L	H	L	22	on	on		on	on	on	on	on		on	on		on		
L	H	H	L	H	L	23	on	on		on	on	on	on	on	on	on			on		
H	H	H	L	H	L	24	on	on		on	on	on		on	on			on	on		
L	L	L	H	H	L	25	on	on		on	on	on	on		on	on		on	on		
H	L	L	H	H	L	26	on	on		on	on	on	on		on	on	on	on	on		
L	H	L	H	H	L	27	on	on		on	on	on	on	on	on						
H	H	L	H	H	L	28	on	on		on	on	on	on	on	on	on	on	on	on		
L	L	H	H	H	L	29	on	on		on	on	on	on	on	on	on		on	on		
H	L	H	H	H	L	30	on	on	on	on		on	on	on	on	on	on	on			
L	H	H	H	H	L	31	on	on	on	on		on		on	on						
H	H	H	H	H	L	32	on	on	on	on		on	on	on		on	on		on		on
X	X	X	X	X	H	none														on	**

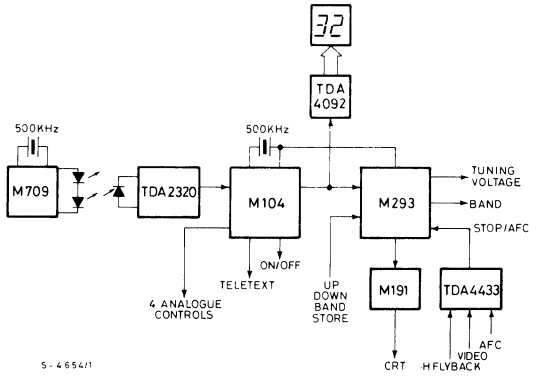
H = High L = Low X = Don't care

* $\overline{AV}$: open collector output.

** $\overline{AV}$ output is "on" whenever the input bits are all high, regardless of the standby input.

APPLICATION INFORMATION

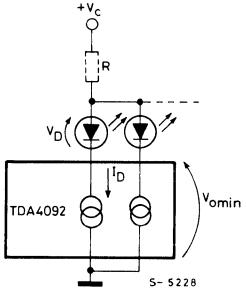
Fig. 1 - Remote controlled voltage synthesizer (up to 32 stations) for TV and radio



When operating with a supply voltage higher than 5.5V for LED elements, it is necessary to limit the IC power dissipation by means of one external resistance connected in series with the common point of the digits (R in fig. 2).
Unused outputs must be connected to V_s taking into account the additional power dissipation.
The value of R must be chosen taking into account the worst working conditions.
The maximum number of ON segments is 12 (number 28 displayed), so,

$$R = \frac{V_C - V_D - V_{out\ min}}{12 \cdot I_D}$$

Fig. 2 - Schematic diagram for LED driving.



I_D, depending on R_{ext} (see Table of Electrical characteristics), can be fixed to the most suitable value to minimize the power dissipation in the IC. Since the worst condition for the device is with seven outputs active, it follows that:

$P_{d\ out} = 7 \cdot I_D\ (V_C - V_D - 7R \cdot I_D)$	Power dissipation in the output stage
$P_d = V_s \cdot I_{s\ max}$	Power drained from the supply
$P_{tot} = P_{d\ out} + P_D$	Total power dissipation

P_{tot} must not exceed the Absolute Maximum Ratings of 800 mW, at $T_{amb} = 55°C$.
Otherwise the maximum operating ambient temperature can be fixed by:

$$T_{amb\ max} = T_{j\ max} - R_{th\ j\text{-}amb}\ P_{tot}$$

Example:

$V_c = 18V$; $I_D = 10$ mA (fixed by means of $R_{ext} = 5.6\ K\Omega$); $V_{out\ min} = 2V$; $I_{s\ max} = 28$ mA; $T_{j\ max} = 150°C$; $V_D = 2V$; $V_s = 5.5V$.

Applying the previous formulae, it follows that: $R \cong 120\Omega$; $P_{d\ out} = 0.532W$; $P_d = 0.154W$; $P_{tot} = 0.686W$; $T_{amb\ max} \cong 68°C$.

TDA4420

LINEAR INTEGRATED CIRCUIT

VISION IF SYSTEM WITH AFC

- HIGH GAIN-HIGH STABILITY
- VERY LOW INTERMODULATION PRODUCTS
- MINIMUM DIFFERENTIAL ERROR
- CONSTANT INPUT IMPEDANCE INDEPENDENT OF AGC
- FAST AGC GATING-ACTION, LARGELY INDEPENDENT OF PULSE SHAPE AND AMPLITUDE
- ADJUSTABLE WHITE LEVEL
- LARGE AFC OUTPUT CURRENT SWING (PUSH-PULL OUTPUT)
- SWITCHABLE AFC

The TDA4420 is a monolithic integrated circuit in 18 lead dual in-line plastic package. The functions incorporated are:

– gain controlled vision IF amplifier
– video demodulator controlled by picture carrier
– AGC detector with gating facility
– AGC amplifier for tuner drive with variable delay
– phase comparator for AFC current generation
– electronic AFC switch, controlled by a DC threshold detector
– thermally compensated push-pull AFC output stage.

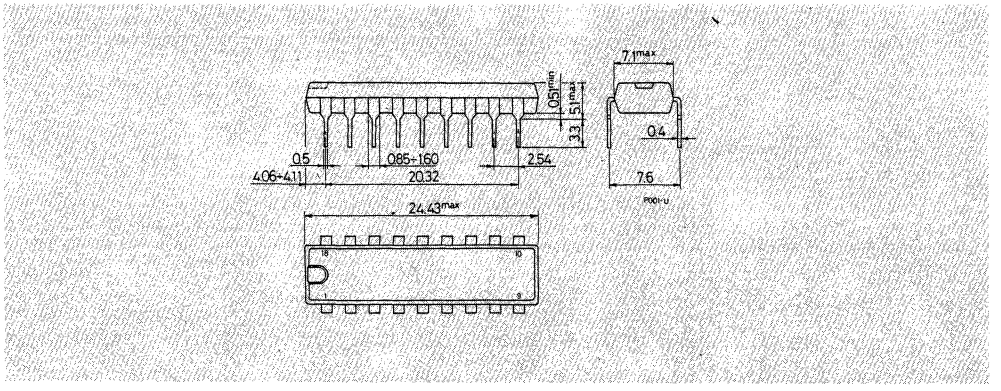
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 15)	15	V
V_5	Voltage at pin 5	15	V
I_{13}, I_{14}	Video DC output current	5	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

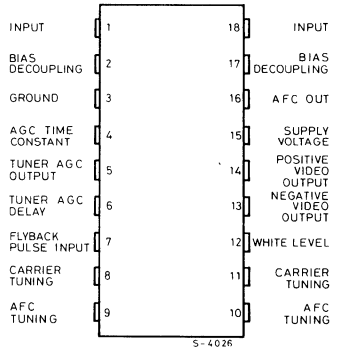
ORDERING NUMBER: TDA 4420

MECHANICAL DATA

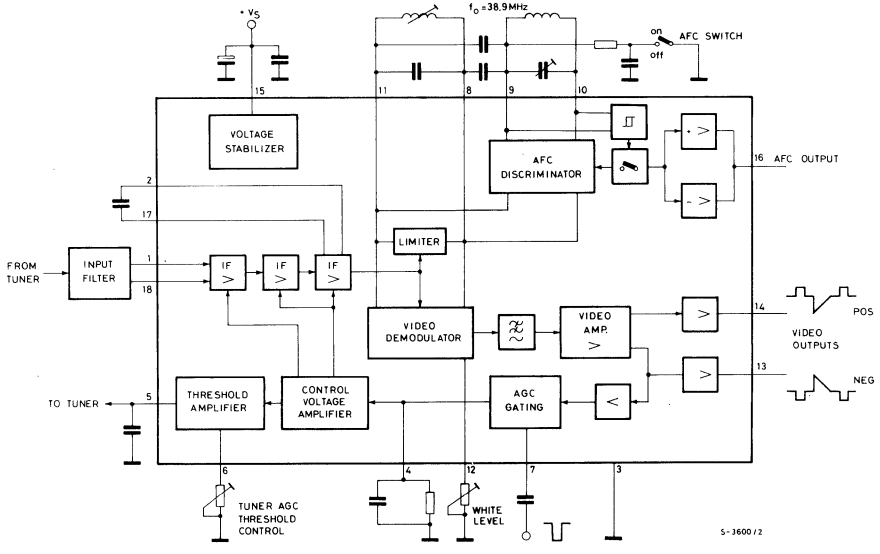
Dimensions in mm



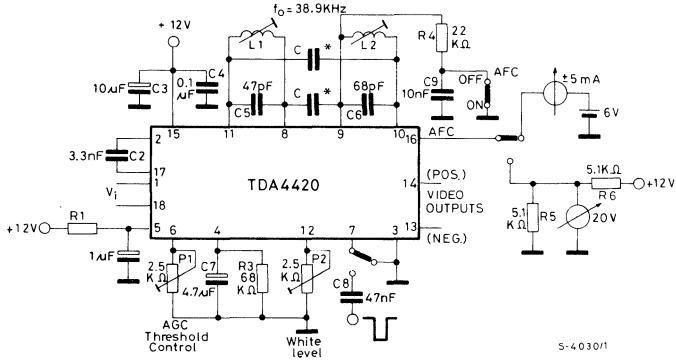
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST CIRCUIT



Note: (*) C ≅ 1.5 pF (pin and lead capacitance).

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; V_s = 12V, f_o = 38.9 MHz; P_1 = 2.5 KΩ; pin 7 connected to GND; P_2 adjusted for V_{13}= 3.3Vpp; AFC off; T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
V_s	Supply voltage range (pin 15)		10	12	15	V
I_s	Supply current (pin 15)			52		mA
V_{14}	Video output DC voltage	V_{13}= 5.5V (1)		5.6		V
V_{13}	Video output DC voltage	pin 12 open (1)			4.5	V
		pin 12 grounded (1)	7			V
V_{13}	Peak black clamping level at negative video output		1.75	1.9	2.15	V
I_{13}	Output DC current (pin 13)	V_s = 15V V_{13}= 8V		1.6		mA
I_9, I_{10}	DC control current for AFC off		150	300		μA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
I_5	Available tuner AGC current	(2)		10		mA
V_7	AGC gating pulse input peak voltage	f pulse = 15625 Hz (3)	-1.5	-3	-5	V
V_o	Peak to peak video output signal (pin 13)	V_{13}= 5.5V (4), (5)		3.3		V
		V_{13}= 6.4V (4), (5)		4.2		V
ΔV_i	AGC range	(6)	50	60		dB
B	Frequency response (-3 dB)	(4)	8	10		MHz
V_i	Input sensitivity	(7), (8)	100	150	200	μV
V_{13}, V_{14}	Video carrier and video carrier 2nd harmonic leakage at video output	V_i = 30 dB f_o = 38.9 MHz (4) 2 f_o= 77.8 MHz			30 50	mV mV
V_{14}	Sound IF at positive video output (5.5 MHz)	(4), (9)	30			mV
d	Differential distortion of negative video output signal	V_i = 30 dB (standard staircase modulating signal)		3		%
d_{im}	Intermodulation product at video outputs (1.07 MHz)	(4), (10)		-50		dB
R_i	Input resistance between pins 1 and 18	(4)		1.4		KΩ
C_i	Input capacitance between pins 1 and 18			2		pF
V_{16}	AFC voltage range	(11)	1		V_s-1.5	V
I_{16}	Maximum available AFC current	(12)			± 3	mA
$\frac{\Delta I_{16}}{\Delta f}$	AFC slope	(13)		±0.01		$\frac{mA}{KHz}$

Notes:

(1) V_{13} and V_{14} are simultaneously adjustable by means of the resistance connected between pin 12 and ground (P_2).
(2) ΔV_i = +60 dB (see note 7); f_m = 100 KHz; m = 0.82.
(3) Input at pin 7 through C8.
(4) The input voltage V_i can have any value within the AGC range.
(5) P_2 adjusted for V_{13}= 5.5V or V_{13}= 6.4V; f_m= 100 KHz; m = 0.82.
(6) ΔV_o = 1 dB; f_m= 100 KHz; m = 0.82.

(7) The measured amplitude is assumed as 0 dB reference level of V_i that is the rms value of the unmodulated video carrier (modulation down).

(8) P_2 is adjusted in order to have V_{13}= 3Vpp at V_i = 4 mV, then the sensitivity is obtained as the minimum input voltage that maintains this output level. f_m= 100 KHz; m = 82%.

(9) f_o= 38.9 MHz (video carrier); f_a = 33.4 MHz (sound carrier); the amplitude of the sound carrier is 30 dB below the amplitude of the video carrier.

(10) V_i at f_o = 38.9 MHz (video carrier); f_a = 33.4 MHz, 6 dB below V_i (sound carrier); f_b = 34.47 MHz, 24 dB below V_i (Chroma subcarrier).

(11) V_i = 40 dB; R_5 = R_6 = 5.1 KΩ; AFC on; f_o = 39.9 MHz; f_o = 37.9 MHz.

(12) V_i = 40 dB; f_o = 39.2 MHz; AFC on; V_{16}= 6V.

(13) V_i = 40 dB; f_o = 38.9 MHz; f_2 = 39.2 MHz; AFC on; V_{16}= 6V.

Fig. 1 - Set-up for measurement of d_{im}

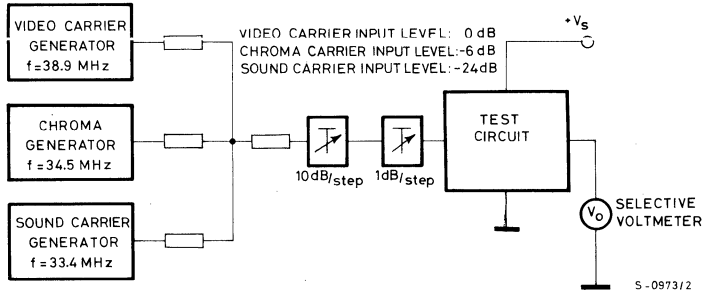
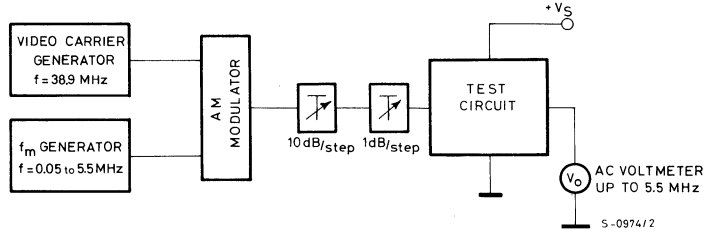
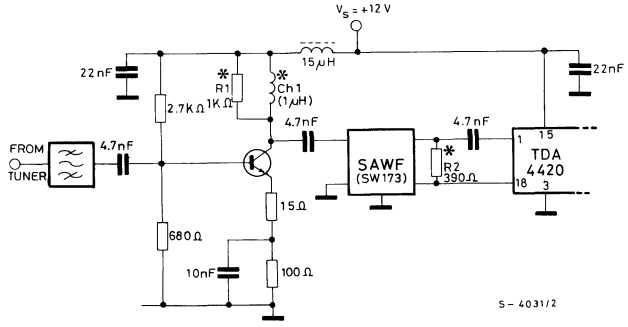


Fig. 2 - Set-up for measurement of ΔV_o



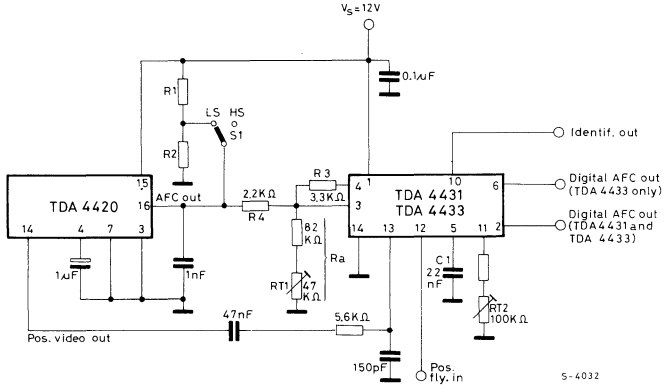
APPLICATION INFORMATION

Fig. 3 - Application circuit



* R_1; R_2; Ch_1, depend from the SAWF characteristics

Fig. 4 - TV Signal identification circuit



TV signal identification circuit:

The suggested application circuit is shown in fig. 4.
The passive components are chosen as follows:

R_1 and R_2 : these define the AFC response slope. For $R_1 = R_2 = 5.1$ KΩ, the typical slope is 750/11 KHz/V (with AFC output unloaded).

S_1 : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

APPLICATION INFORMATION (continued)

R_3 and R_4 : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width (δf) calculated from the linear AFC width ($2\Delta f$). With $V_s = 12V$, the relation is:

$$\delta f = 0.036\ (2\Delta f)\ \frac{R_3 + R_4}{R_3}$$

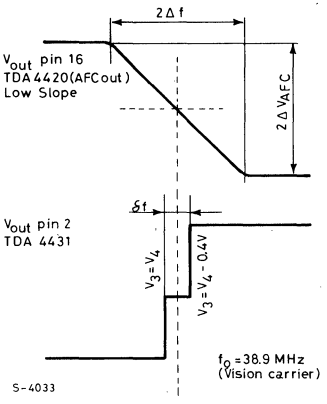
R_{T1} : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is:

$$R_a = 33\ R_3$$

with $R_3 = 3.3\ K\Omega$, R_a can be a fixed resistor of 110 $K\Omega$.

To make better sensitivity adjustment of trimmer R_{T2}, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.
In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Fig. 5 - Linear and digital AFC characteristics (TDA 4420 and TDA 4431)



TDA4431
TDA4433

TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

The TDA4431 and the TDA4433 are monolithic integrated circuits in a 14 lead dual-in-line plastic package. They integrate the following functions:

– TV signal identificator – Sync. separator – Threshold detector – Digital Interface – Voltage regulator

They are intended for use in Electronic Program Memory tuning systems, the TDA4431 in conjunction with M193B1, while the TDA4433 with M293B1. The circuits features are:

– Identification of true TV stations only.
– Low impedance output of the identification signal.
– Digital control signal for automatic search and AFC operation.
– Thermal compensation of the voltage regulator.

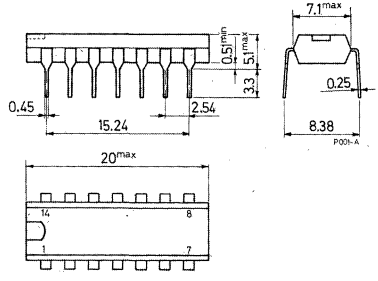
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage (pin 1)	16	V
V_3	Voltage at pin 3	16	V
V_{13}	Voltage at pin 13	-5 to +6	V
I_2	Pin 2 current (TDA4431)	± 1	mA
I_6 ; I_2	Pin 6 and pin 2 current (TDA4433)	1	mA
I_{10}	Pin 10 current	2	mA
I_{11}	Pin 11 current	2	mA
I_{12}	Pin 12 current	± 2	mA
P_{tot}	Total power dissipation at $T_{amb} \leqslant 70°C$	800	mW
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBERS: TDA 4431
TDA 4433

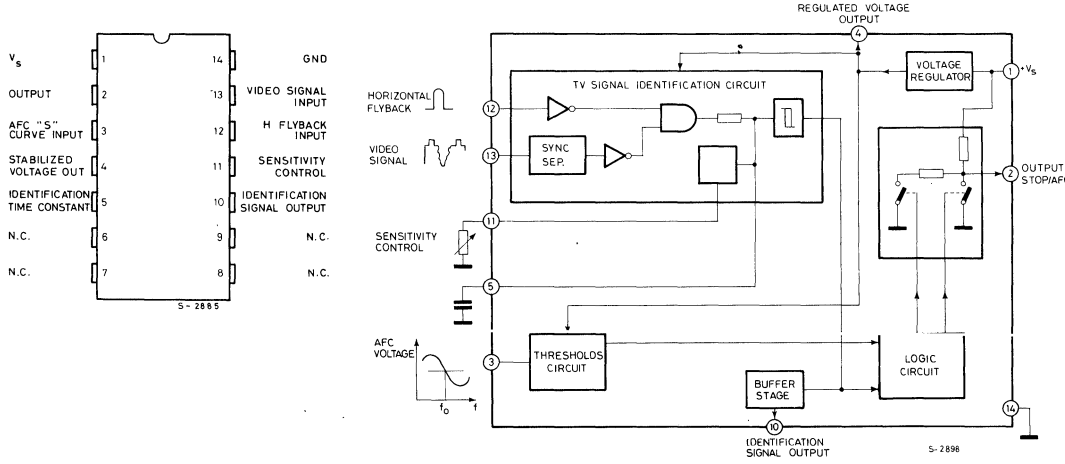
MECHANICAL DATA

Dimensions in mm



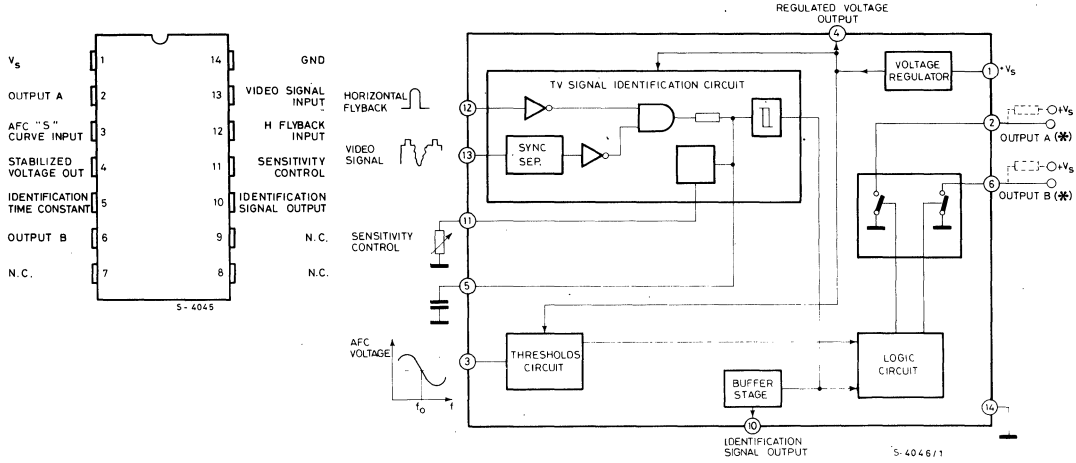
CONNECTION AND BLOCK DIAGRAM (TDA4431)

(Top view)



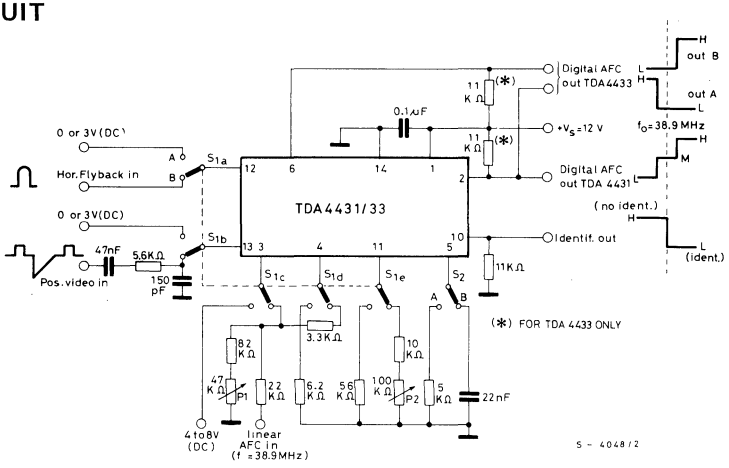
CONNECTION AND BLOCK DIAGRAM (TDA4433)

(Top view)



* Open collector outputs

TEST CIRCUIT



S_1 A : Static tests
B : Functional tests

S_2 A : DC or pulses width
B : Functional tests

P_1 Digital AFC perfect tuning
P_2 Sensitivity control

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit; V_s = 12V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage range (pin 1)		10.8		14.5	V
I_s	Supply current (pin 1)	V_s = 14.5V			30	mA
V_2	Output voltage: low	$f_{tuning} < f_o$			0.8	V
	medium	$f_{tuning} = f_o$ V_s = 10.8 to 14.5	5.5		8.5	V
	high (TDA4431)	$f_{tuning} > f_o$	V_s-0.5			V
V_2	Output voltage	$f_{tuning} < f_o$ I_2 = 1mA	V_s-0.5			V
		$f_{tuning} = f_o$			0.8	V
	(TDA4433)	$f_{tuning} > f_o$			0.8	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter			Test conditions	Min.	Typ.	Max.	Unit
V_6	Output voltage		$f_{tuning} < f_o$ $I_6 = 1mA$			0.8	V
			$f_{tuning} = f_o$ $I_6 = 1mA$			0.8	V
	(TDA4433)		$f_{tuning} > f_o$	V_s-0.5			V
I_2	Output current (TDA4431)					± 25	μA
V_3	Input voltage range			4		8	V
V_{3U}	Upper threshold voltage (see fig. 2)			V_4-25	V_4	V_4+25	mV
V_{3L}	Lower threshold voltage (see fig. 2)			V_4-425	V_4-400	V_4-375	mV
R_3	Input resistance		$V_3 = V_4$	1.4			MΩ
V_4	Regulated voltage		$I_4 = 1mA$		6.6		V
I_4	Output current					1	mA
R_4	Output differential resistance				60		Ω
$\frac{\Delta V_4}{\Delta T_s}$	Regulated voltage thermal drift					± 2	mV/°C
V_{10}	Identification output voltage	no identification	$I_{10} = 1mA$	V_s-1.3			V
		identification				20	mV
R_{10}	Output resistance				100		Ω
V_{12}	Switch off threshold voltage					1	V
I_{12}	Input flyback current			0.5		1.5	mA
R_{12}	Input resistance		$V_{12} = 3V$		10		KΩ
t_{fly}	Flyback pulse duration			10		17	μsec.
t	Time delay between leading edges of flyback pulse and sync. pulse			0		3.5	μ sec.
V_{13}	Video input signal (peak to peak)			2.5		4.5	V
V_{13}	Sync. pulse amplitude (above black level)			0.52			V
R_{13}	Input resistance					1.5	KΩ

Fig. 1 - Medium output voltage Vs. Supply voltage.

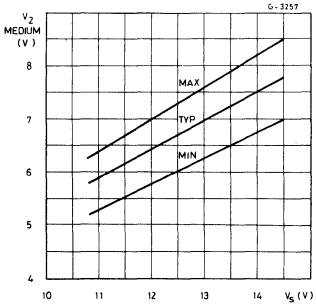
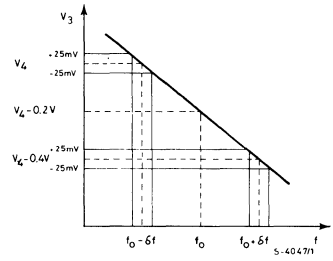


Fig. 2 - Digital AFC threshold voltage vs. frequency.



Input Voltage (V_3)	TDA4431	TDA4433	
	Output voltage (V_2)	Output voltage (V_2)	Output voltage (V_6)
$V_3 > V_4$	Low level	High level	Low level
V_4-0.4V $< V_3 < V_4$	Medium level	Low level	Low level
$V_3 < V_4$-0.4V	High level	Low level	High level

APPLICATION INFORMATION (refer to the block diagram)

TV signal identification circuit:

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.
The signal identification is carried out by charging the capacitor connected to pin 5; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.
When the identification has been made, a signal (level L) is available at pin 10.

Threshold circuit:

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.
With a correct TV signal, the output levels corresponding to the 3 ranges are:

	TDA4431 (V_2)	TDA4433	
		(V_2)	(V_6)
$f_o - \delta f$	L	H	L
f_o	M	L	L
$f_o + \delta f$	H	L	H

L = Low level
M = Medium level
H = High level

Note that the output levels are different for the two devices.

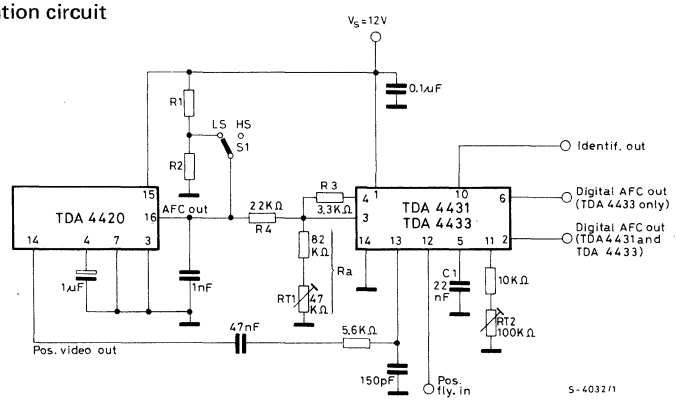
The TDA4431 provides three output levels: low (L), medium (M) and high (H). The output at pin 2 remains at medium level if no video signal is applied at the input or if a video signal is applied but is not identified as a true TV signal.

The TDA 4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

Voltage Regulator

The circuit can deliver 1mA and it can be used as D/A converter reference to supply fine tuning voltage.

Fig. 3 - Application circuit



The passive components should be chosen as follows:

R_1 and R_2 : these define the AFC response slope. For $R_1 = R_2 = 5.1K\Omega$, the typical slope is 750/11 KHz/V (with AFC output unloaded).

S_1 : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

R_3 and R_4 : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width (δf) calculated from the linear AFC width ($2\Delta f$). With $V_s = 12V$, the relation is:

$$\delta f = 0.036\,(2\Delta f)\,\frac{R_3 + R_4}{R_3}$$

R_{T1} : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is:

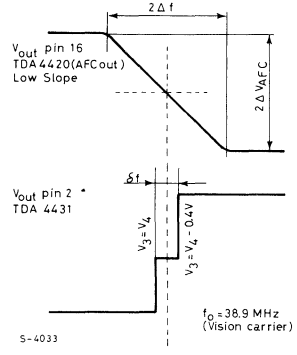
$$R_a = 33\,R_3$$

with $R_3 = 3.3K\Omega$, R_a can be a fixed resistor of $110K\Omega$.

R_{T2} : by means of this trimmer it is possible to choose the better sensitivity. It is possible to put a fixed resistor at pin 11 in the range of 68 KΩ to 100 KΩ.

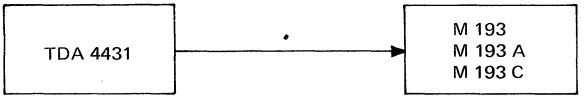
To make a better sensitivity adjustment of trimmer R_{T2}, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.
In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Fig. 4 – Linear and digital AFC

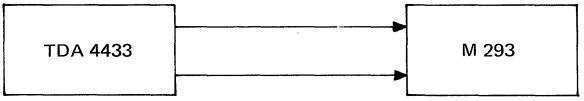


EPM SYSTEM CONFIGURATIONS

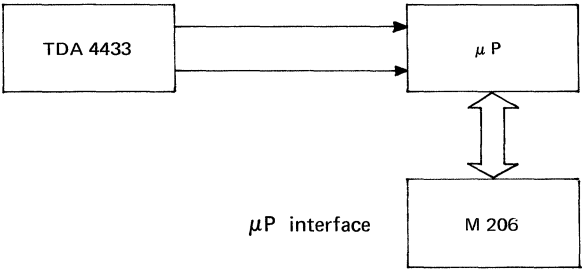
1) For 16 channels



2) For 32 channels



3) With microprocessor



LINEAR INTEGRATED CIRCUIT

TDA7270S

MULTIFUNCTION SYSTEM FOR TAPE PLAYERS

The TDA 7270S is a multifunction monolithic integrated circuit in a 16-lead dual in-line plastic package specially designed for use in car radios cassette players, but suitable for all applications requiring tape playback.
It has the following functions:

- Motor speed regulator
- Automatic stop
- Manual stop
- Pause
- Cassette ejection
- Radio – Playback automatic switching.

The circuit incorporates also:

- Thermal protection
- Short circuit protection to ground (all the pins)

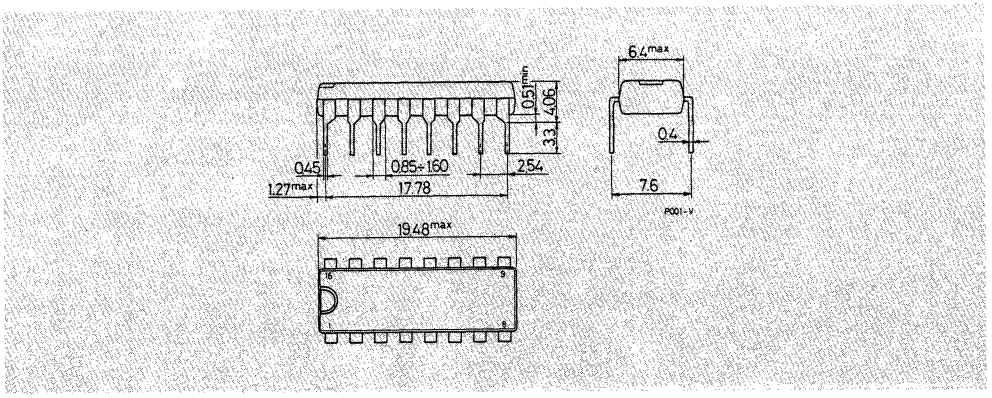
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	20	V
I_1	Sink peak current at pin 1	2	A
I_5	Sink peak current at pin 5	2	A
P_{tot}	Power dissipation at $T_{amb} \leqslant 80°C$	1	W
T_{stg} ; T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 7270 S

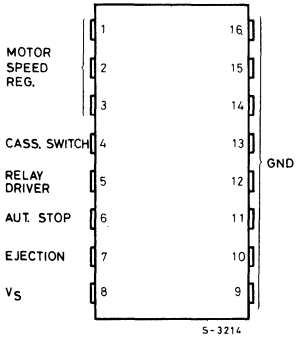
MECHANICAL DATA

Dimensions in mm

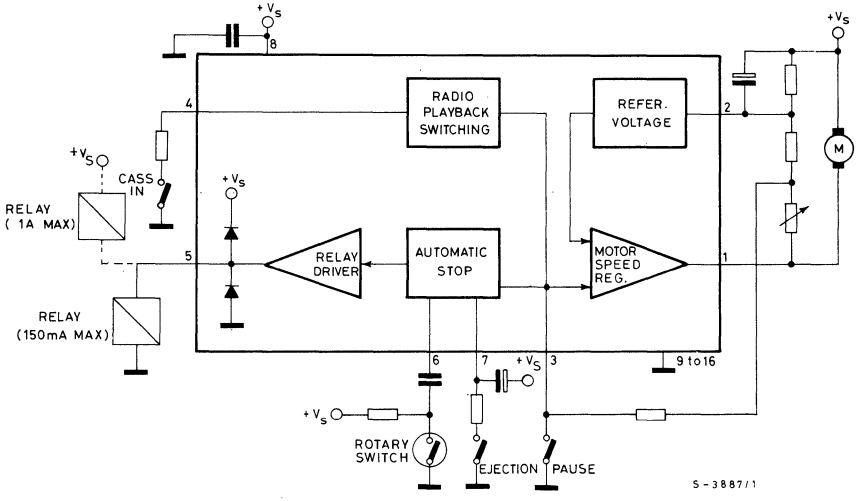


CONNECTION DIAGRAM

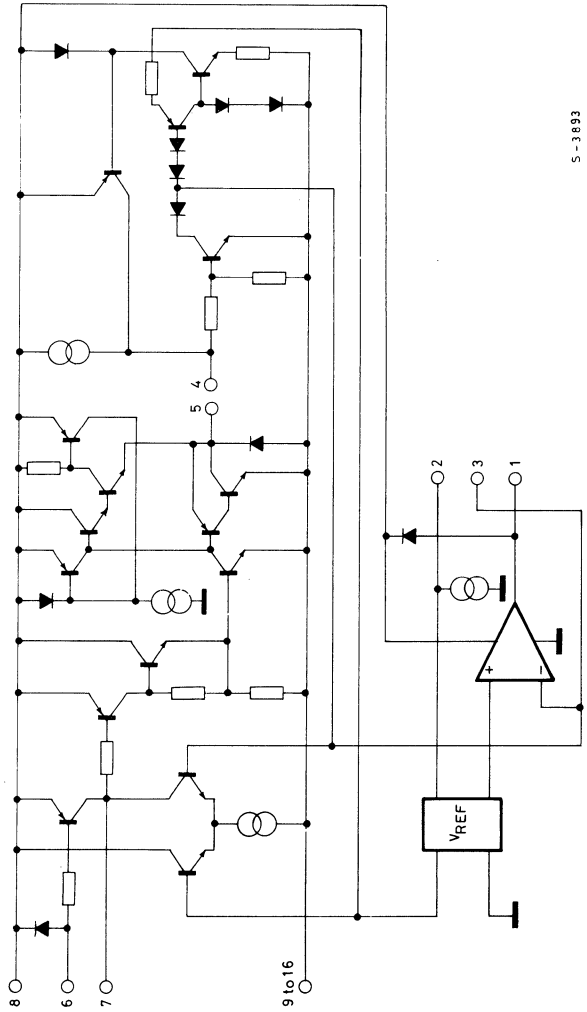
(top view)



BLOCK DIAGRAM

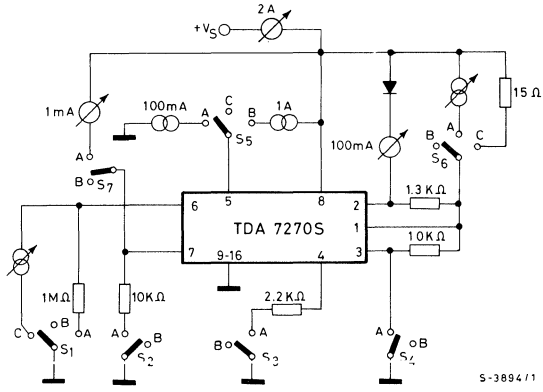


SCHEMATIC DIAGRAM



S-3893

TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit; T_{amb}= 25°C; V_s = 14V; S_7 at B, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		6		18	V
I_d	Quiescent drain current	Automatic stop-S_3 at B S_4 at B		5	10	mA
		Pause - S_3 at A; S_4 at A		9	15	
I_5	Maximum output current for relay driving		150			mA
T_{sd}	Thermal shut-down case temperature	P_{tot} = 1W $(\frac{\Delta V_{ref}}{V_{ref}} = -5\%)$	105	125		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MOTOR SPEED CONTROL						
I_{MS}	Starting current (pin 1)		1			A
V_{ref}	Reference voltage (pin 2-3)	I_M= 100 mA	1.15	1.25	1.35	V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$		I_M= 100 mA V_s = 8 to 18V		0.1	0.4	%/V
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$		I_M= 50 to 400 mA		0.01	0.03	%/mA
$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$		I_M= 100 mA T_{amb}= -20 to 70°C		0.01		%/°C
V_2	Operating voltage	I_M= 100 mA $\frac{\Delta V_{ref}}{V_{ref}}$ = -5%	2.4			V
K	Reflection coeff.(K= I_M/I_T see fig. 12)	I_M= 100 mA	18	20	22	—
$\frac{\Delta K}{K}/\Delta V_s$		I_M= 100 mA V_s= 8V to 18V		0.3	1	%/V
$\frac{\Delta K}{K}/\Delta I_M$		I_M= 50 to 400 mA		0.005	0.02	%/mA
$\frac{\Delta K}{K}/\Delta T$		I_M= 100 mA T_{amb}= -20 to 70°C		0.01		%/°C
PAUSE						
I_3	Current consumption	S_4 at A	1.4			mA
V_{8-1}		S_4 at A			0.2	V
EJECTION						
I_7		S_2 in A	20			μA
V_{5-8}	Saturation voltage	I_5 = 100 mA		2.1	3	V
V_5	Saturation voltage	I_{5-8}= 1.5A		2.2	3	V
V_4	(Pause condition)	S_1 at A S_3 at A S_4 at A	6			V
V_4	(Radio)	S_1 at A S_3 at B S_4 at B	6	9		V
V_4	(Tape)	S_1 at A S_3 at A S_4 at B			1.7	V
R_o	Output impedance at pin 4	S_3 at B		16	22	KΩ
AUTOMATIC STOP						
V_{8-1}	Saturation voltage	S_1 at B S_2 at B S_3 at B			1	μA
I_6	Minimum current to avoid stop	S_1 at C			1	μA
I_{7-8}	Load current for delay circuit	I_6= 0 S_7 at A S_2 at B	10.5	15	19.5	μA

Fig. 1 - Reference voltage vs. supply voltage.

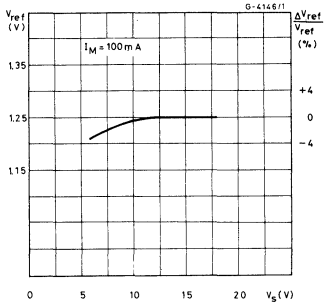


Fig. 2 - Reference voltage vs. motor current.

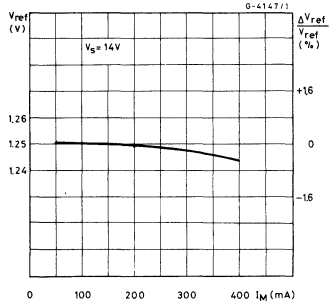


Fig. 3 - Reference voltage vs. ambient temperature.

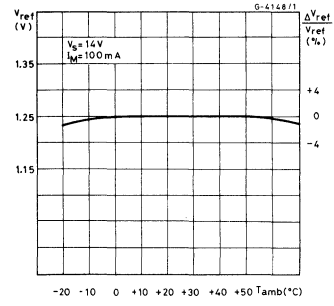


Fig. 4 - Saturation voltage (pins 5-8) vs. pin 5 current.

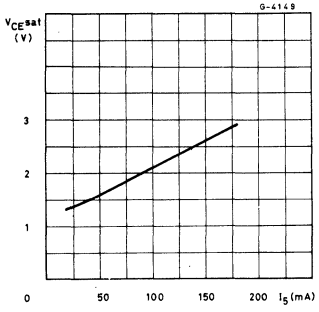


Fig. 5 - Reflection coefficient vs. supply voltage.

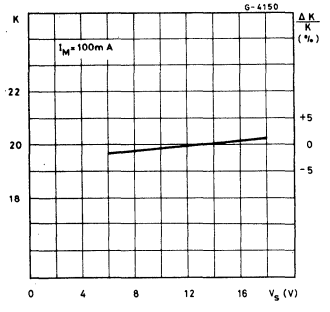


Fig. 6 - Reflection coefficient vs. motor current.

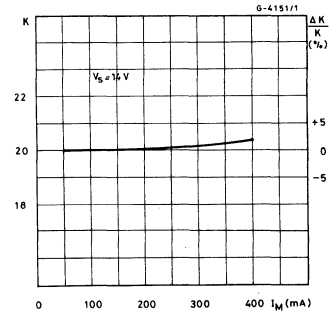


Fig. 7 - Reflection coefficient vs. ambient temperature.

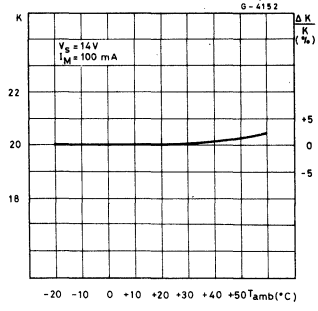
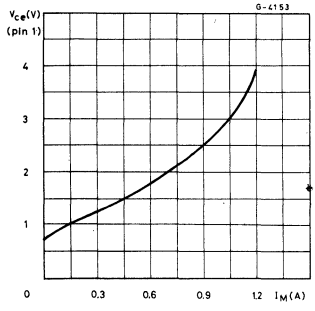


Fig. 8 - Pin 1 saturation voltage vs. motor current.



APPLICATION INFORMATION

The TDA 7270S incorporates four different functional blocks:

1) Motor speed control.
2) Autostop circuit.
3) Radio/Playback switching
4) Relay driver.

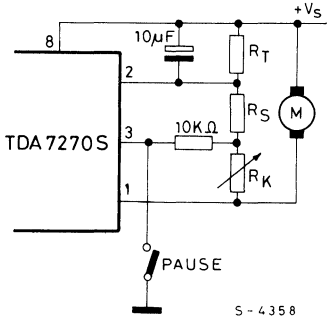
The motor speed control is a conventional circuit providing correction for the internal losses of the motor. Fig. 9 shows the external circuit.
The values of R_T, R_S and R_K determine the regulation characteristics and motor speed.

$$R_T = K \cdot R_M$$

where K = the IC regulator reflection coefficient and R_M = motor internal resistance.
The following condition must be always satisfied

$$R_S \leqslant 4\, R_T$$

Fig. 9



The voltage applied across the motor is given by

$$V_{8-1} = V_{ref}\ [\,1 + \frac{R_T}{R_S}\ (\,1 + \frac{1}{K}) + \frac{R_K}{R_S}]$$

and this is proportional to R_K which therefore adjusts the speed.
The voltage between pin 2 and the supply must not fall below 0.3V and so

$$[\,V_{ref\ min}\ (\frac{R_T}{R_S}) + I_{M\ min}\ (\frac{R_T}{K_{max}})\ ] > 0.3V$$

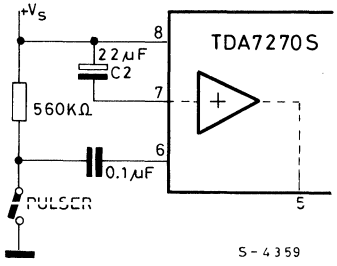
The "pause" condition corresponds to $V_3 < 50$ mV; in this condition the motor will stop ($V_{1-8} < 0.2V$), the capacitor C_2 on the autostop circuit (see below) will no longer be charged and the pin 4 (cassette/radio switch output) will be pulled high.

APPLICATION INFORMATION (continued)

The autostop circuit is shown in fig. 10.
In normal operation the capacitor C_2 (22 μF) is slowly charged by a constant current drawn by pin 7 of 15 μA, and each time the pulser (a switch on the cassette take-up speed shaft) closes, C_2 is discharged. If the cassette stops, and the pulse stops, the voltage on pin 7 falls.
This switches the power amplifier state and pin 5 goes low. Pin 5 can be used for one of two purposes:

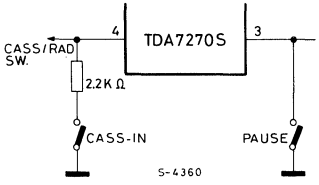
1) to drive a stop warning light connected from pin 5 supply V_s.
2) to actuate a solenoid wired either to ground (to release the cassette) or to supply (to eject the cassette).

Fig. 10



The **pause and/or cassette/radio switching** shown in fig. 11 has an input/output on pin 4.
If pin 4 is not used it should be grounded.

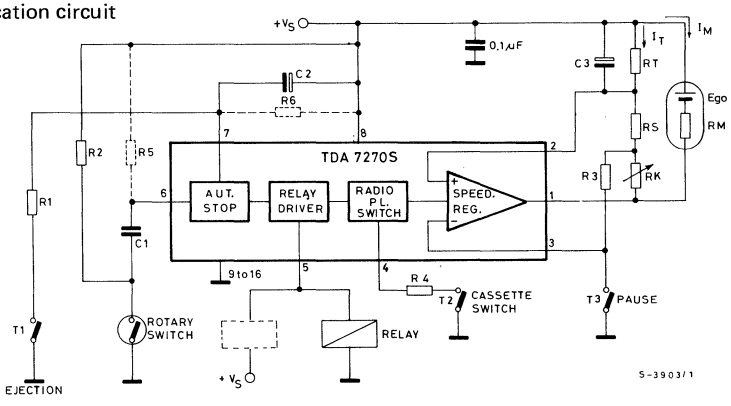
Fig. 11



This pin has the following logic.

Cass IN	Pause	Pin 4	Function
Open	Open	> 6V	motor off/radio on
Open	Close	> 6V	motor off/radio on
Close	Open	< 1.7V	motor on/cass. on
Close	Close	> 6V	pause/radio on

Fig. 12 - Application circuit



DESCRIPTION OF OPERATION (Refer to fig. 12)

When the cassette is introduced the switch T_2 closes, the motor start to turn and the rotary switch generates the pulses which keep the levels of pin 5 and pin 7 high. A relay between pin 5 and ground holds the cassette. If there are no pulses at pin 6 (because tape stopped) or if the ejection switch T_1 is closed, the voltages at pin 5 and pin 7 drop; the relay is thus de-energized and the cassette ejected; as soon as the cassette is ejected, the switch T_2 opens and the motor stops. The capacitor at pin 7 discharges allowing the system to start again when another cassette is inserted. In other types of mechanical systems the cassette is ejected by energizing a relay; in this case the relay must be connected between pin 5 and the supply; the sequence of operations is then the same as described above. If the pause switch T_3 is closed, the motor stops even though there are no pulses at pin 6, the voltage levels at pins 7 and 5 remain high so the cassette is not ejected and the motor is ready to start again as soon as the pause key is released. A voltage for driving the radio-tape switching is available at pin 4. This voltage level is high ($> 6V$) with stopped motor and is low ($< 1.7V$) with running motor.

APPLICATION SUGGESTION (See figure 12)

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range	
					Min.	Max.
R_1	10 KΩ	Limits current from pin 7	Delayed ejection. Possibility that ejection does not work	High driving current at pin 7	0	100KΩ
R_2	560 KΩ	By rotary switch it produces pulses which disable the automatic stop	Undesired operation of automatic switch	Possibility of audio interference spikes	100KΩ	2MΩ
R_3	10 KΩ	Limits the motor current during pause (T_3 closed)	Reference voltage variation	Higher motor current during pause (T_3 closed) with delayed stop of motor	1KΩ	47KΩ
R_4	2.2 KΩ	Fixes voltage of pin 4 during pause and playback	Voltage at pin 4 increases	Voltage at pin 4 decreases. Radio-Playback switching could not work	1.5KΩ	2.7KΩ
R_5	560 KΩ	Compensates for current loss between pin 6 and ground	Limited compensation	Necessity to increase C_1 and decrease R_2	100KΩ	∞
R_6	1 MΩ	Compensates for current loss between pin 7 and ground. Also reduces recovery time	Limited compensation	Possibility that automatic stop will not work	560KΩ	∞
R_T	$K \cdot R_M$ (typical values)	Compensates for voltage drops at motor terminals vs. ΔI_M	Danger of oscillations	Poor speed regulation versus ΔI_M	See note on next page	

APPLICATION SUGGESTION (continued)

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value	Allowed range Min.	Allowed range Max.
R_S	See Note (*)	Fixes the current value in R_T and and R_K for $I_M = 0$	Danger of saturation of non inverting input of regulator (pin 2). Considerable speed variation for small variation of R_K	Impossibility to obtain a low motor speed		$4\,R_T$
R_K	See Note (*)	Fixes the requested V_{8-1}	Wide speed variation versus ΔR_K	Limited speed variation versus ΔR_K		
C_1	0.1 μF	DC isolation	Electrolytic capacitors cannot be used	Undesired automatic stop	0.047 μF	
C_2	22 μF	Integrates the pulses of the rotary switch	High recovery time	Low recovery time. Undesired automatic stop	3.3 μF	
C_3	10 μF	By pass	Wow and flutter problems	Instability at low temperature	5 μF	22 μF
Rotary switch frequency	20 Hz	Keeps automatic stop off	Possibility of audio interference spikes	Necessity to increase C_1 and C_2		

NOTE (*):

– $V_{8-1} = V_{ref}\left[1 + \frac{R_T}{R_S}\left(1 + \frac{1}{K}\right) + \frac{R_K}{R_S}\right]$ from which it can be seen that V_{8-1} varies linearly with R_K.

– The voltage between pin 2 and the supply must not fall below 0.5V, so the following expression must be verified

$$\left[V_{ref\,min}\left(\frac{R_T}{R_S}\right) + I_{M\,min}\left(\frac{R_T}{K_{max}}\right)\right] > 0.3V$$

– During the pause, the voltage between pin 3 and ground must be lower than 1.3V.

Fig. 13 - Speed variation vs. supply voltage

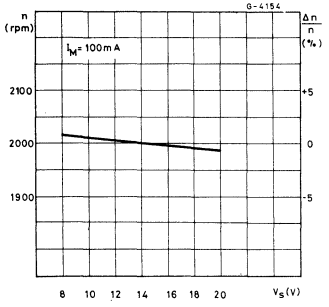


Fig. 14 - Speed variation vs. motor current

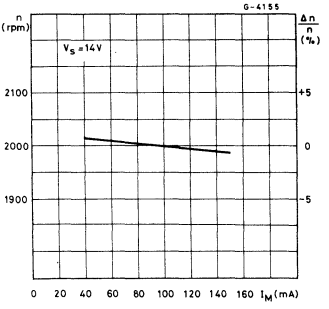
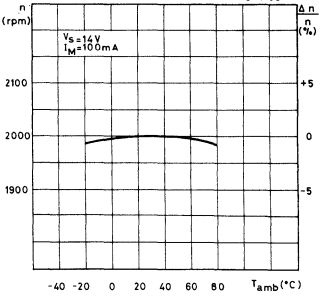


Fig. 15 - Speed variation vs. ambient temperature



APPLICATION SUGGESTION (continued)

Fig. 16 - Delay time of the relay driver (C_2= 2.2 μF)

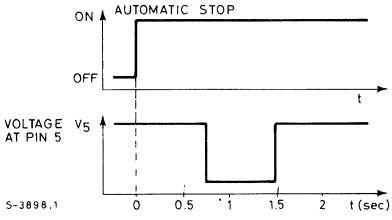
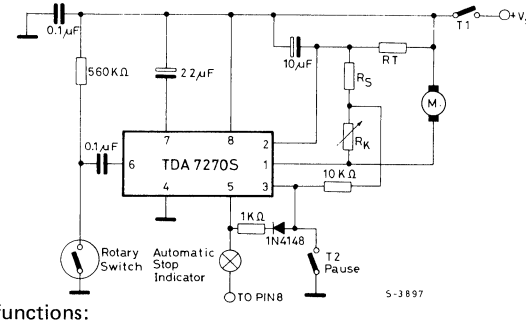


Fig. 17 - Low cost application circuit



The circuit shown in fig. 17 offers the following functions:

1) motor speed regulation
2) automatic stop
3) autostop warning light
4) pause.

The circuit incorporates an additional resistor/diode from pin 3 to pin 5. When the cassette stops, and the pulser no longer generates pulses, pin 5 falls to a low level and the stop indicator is on.
Pin 3 is pulled low through the 1 KΩ resistor and the diode, however pin 3 must not be pulled lower than 1.3V since this would cause pin 5 to go high again. The current of about 1 mA out of pin 3 causes V_{3-5} to be about 1.5V.
In this way the motor remains stopped and pin 5 remains low.

MOUNTING INSTRUCTIONS

Fig. 18 - Example of heatsink using PC board copper

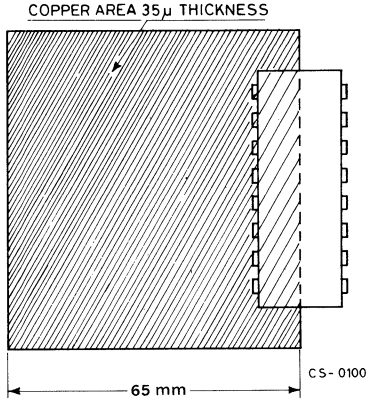
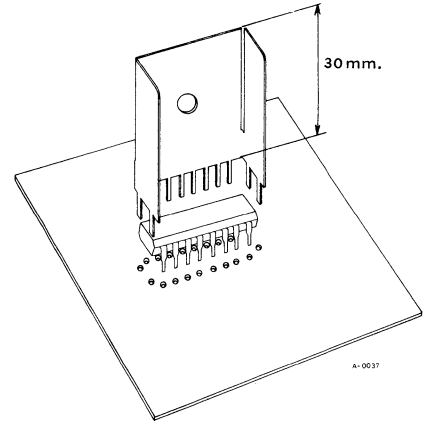


Fig. 19 - Example of external heatsink



Figures 18 and 19 show two ways to make the device dissipate.
In both cases, R_{th}= 35°C/W.

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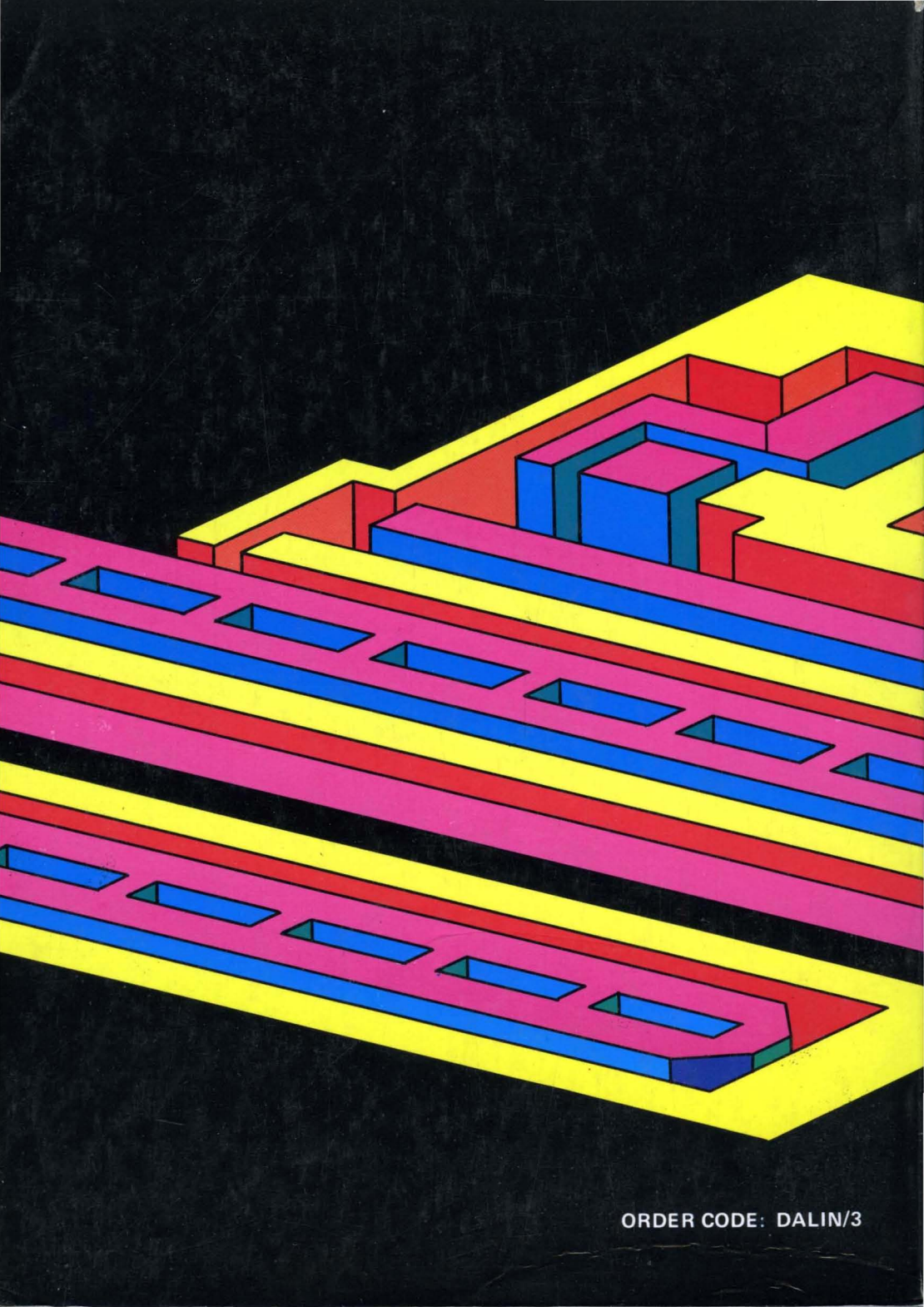

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