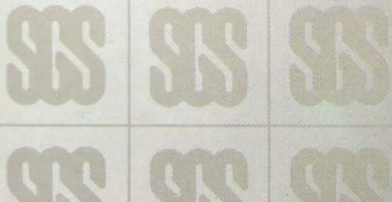
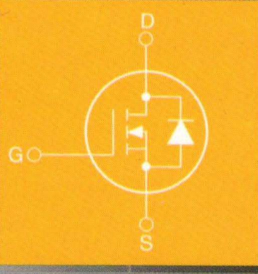
SGS

DATABOOK

POWER MOS DEVICES

1st EDITION





SGS Technology and Service

POWER MOS DEVICES

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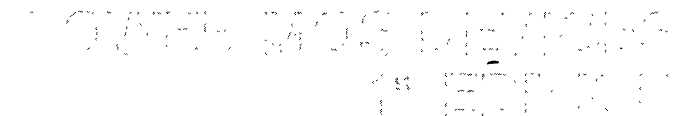

ISSUED OCTOBER 1985

INTRODUCTION

This databook contains data sheets and technical notes on the SGS range of POWER MOS devices for professional, industrial and consumer applications.
Selection guides are provided in the following pages to facilitate rapid identification of the most suitable device for the intended use.
The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.

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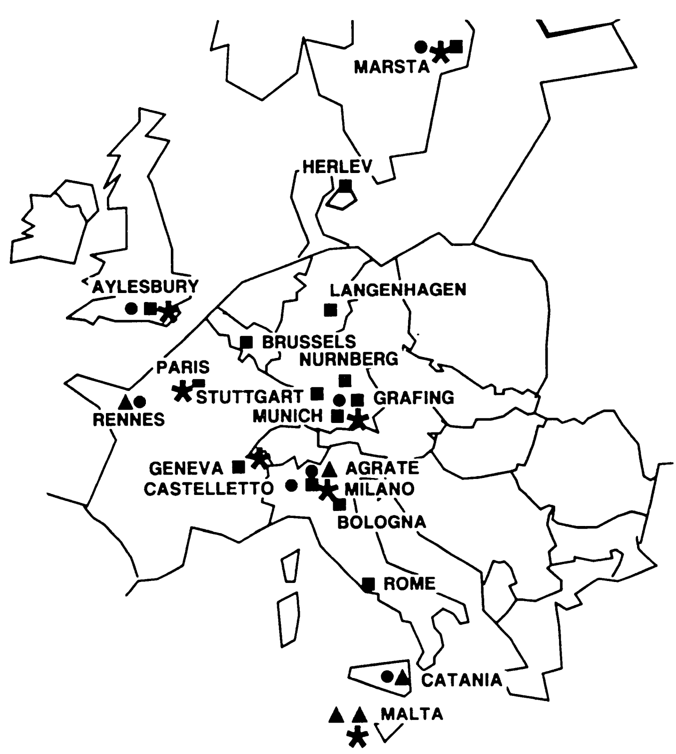
IDENTITY

Late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with billings well over a quarter billion dollars and employing over 10000 people.

The SGS Group of Companies has now reached a total of 12 subsidiaries, located in Brazil, France, Germany, Italy, Malta, Malaysia, Singapore, Spain, Sweden, Switzerland, United Kingdom and the USA.

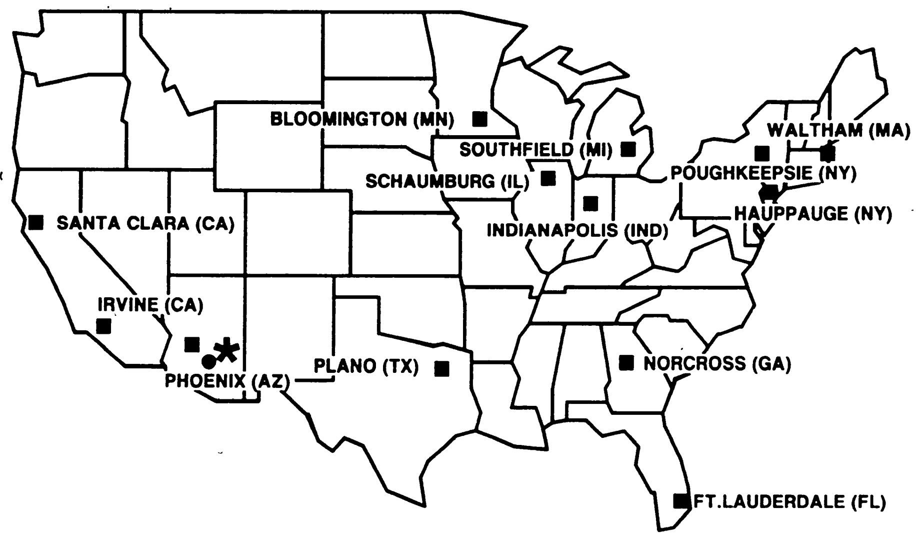
To go with its logo, the company takes the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

SGS LOCATIONS - EUROPE



- * HEADQUARTERS
- ▲ FACTORIES
- ■ SALES OFFICES
- ● DESIGN CENTERS

SGS LOCATIONS - NORTH AMERICA



* HEADQUARTERS

■ SALES OFFICES

● DESIGN CENTERS

SGS LOCATIONS - ASIA/PACIFIC

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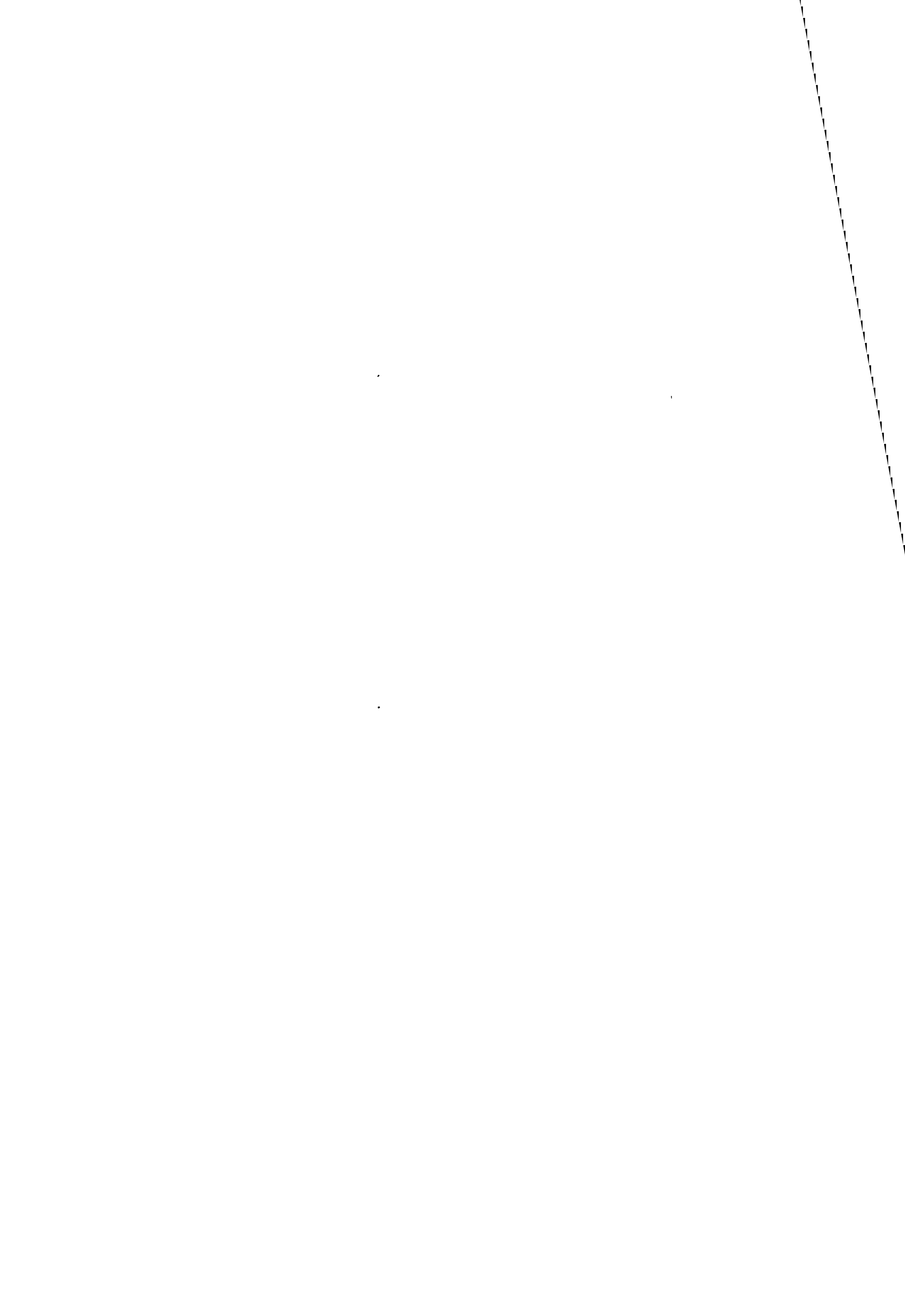
* ▲ FACTORIES
* ■ SALES OFFICES
* ● DESIGN CENTERS

INTRODUCTION A

TECHNICAL NOTES B

DATA SHEETS C



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INTRODUCTION A

HIGH VOLTAGE POWER MOS PRODUCT RANGE

I_D max (A)	$R_{DS(on)}$ (Ω)	V_{DS} (V) 350	400	450	500	550	C_{iss} (pF)	gfs (mho)
12.0	0.55	SGSP476 SGSP576	SGSP475 SGSP575				2100	6
	0.7			SGSP474 SGSP574				
10.0	0.7				SGSP479 SGSP579		1900	5
	1					SGSP478 SGSP578		
6.0	1.0	SGSP366 SGSP466 SGSP566	SGSP365 SGSP465 SGSP565				1000	3
	1.5			SGSP364 SGSP464 SGSP564				
	1.5				SGSP369 SGSP469 SGSP569		1000	3
	2.5					SGSP368 SGSP468 SGSP568		
3.0	2.5	SGSP132 SGSP232 SGSP332 SGSP532	SGSP131 SGSP231 SGSP331 SGSP531				450	1.5
	3.0			SGSP130 SGSP230 SGSP330 SGSP530				
2.0	3.8				SGSP119 SGSP219 SGSP319 SGSP519		380	1.2
	4.5					SGSP118 SGSP218 SGSP318 SGSP518		
1.5	5.0	SGSP156 SGSP256 SGSP356	SGSP155 SGSP255 SGSP355				220	0.65
	6.5			SGSP154 SGSP254 SGSP354				
1.2	8.5				SGSP139 SGSP239 SGSP339			
	11.0					SGSP138 SGSP238 SGSP338		
0.6	20.0	SGSP142 SGSP242 SGSP342	SGSP141 SGSP241 SGSP341				105	0.2
	25.0			SGSP140 SGSP240 SGSP340				
0.5	30.0				SGSP149 SGSP249 SGSP349		95	0.18
	40.0					SGSP148 SGSP248 SGSP348		

Die size (relative areas)

16 8 4 2 1

LOW VOLTAGE POWER MOS PRODUCT RANGE

I_D max (A)	$R_{DS(on)}$ (Ω)	V_{DS} (V)						C_{iss} (pF)	gfs (mho)
		50	60	80	100	200	250		
40	0.03	SGSP492 SGSP592	SGSP491 SGSP591					2400	10
30	0.05			SGSP472 SGSP572				2200	9
	0.075				SGSP471 SGSP571				
24	0.06	SGSP382 SGSP482 SGSP582	SGSP381 SGSP481 SGSP581					1400	5
20	0.17					SGSP477 SGSP577		2500	8
	0.22						SGSP473 SGSP573		
15	0.1			SGSP362 SGSP462 SGSP562				1200	4.5
	0.15				SGSP361 SGSP461 SGSP561				
12	0.15	SGSP3055						460	3
10	0.13	SGSP122(*) SGSP222 SGSP322 SGSP422 SGSP522	SGSP121(*) SGSP221 SGSP321 SGSP421 SGSP521					500	2.5
	0.33					SGSP367 SGSP467 SGSP567		1200	3
	0.45						SGSP363 SGSP463 SGSP563		
7.0	0.3	SGSP158(*) SGSP258 SGSP358	SGSP157(*) SGSP257 SGSP357	SGSP112(*) SGSP212 SGSP312 SGSP412 SGSP512	SGSP111(*) SGSP211 SGSP311 SGSP411 SGSP511			480 270	2 1.5
6.0	0.75					SGSP117(*) SGSP217 SGSP317 SGSP517		465	1.5
	1.2						SGSP116(*) SGSP216 SGSP316 SGSP516		
5.0	0.45			SGSP152 SGSP252 SGSP352	SGSP151 SGSP251 SGSP351			250	1.5
1.5	1.4			SGSP102 SGSP202 SGSP302	SGSP101 SGSP201 SGSP301			125	0.5

Note: For TO-39 DEVICES MARKED (*), $I_D$max IS DERATED BY ABOUT 30% REFER TO THE DATASHEET

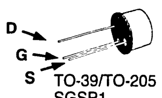
Die size (relative areas)

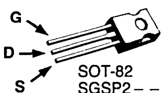
16 8 4 2 1

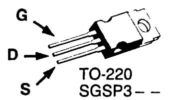
POWER MOS POWER DISSIPATION PACKAGE VS DIE SIZE AT T_{case} 25°C

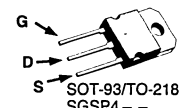
PACKAGE	DIE SIZE (relative areas) 1	2	4	8	16
TO-39 SGSP1——	15W	15W	15W	—	—
SOT-82 SGSP2——	18W	40W	50W	—	—
TO-220 SGSP3——	18W	50W	75W	100W	—
SOT-93 SGSP4——	—	—	75W	125W	150W
TO-3 SGSP5——	—	—	75W	125W	150W

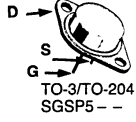
Package-Pin configuration









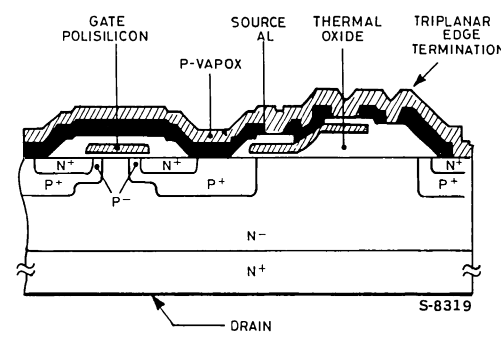


N-CHANNEL POWER MOS TRANSISTORS

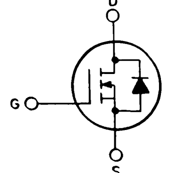
VERY FAST SWITCHING AND/OR EASY DRIVING

Very fast switching and/or easy driving:

- SMPS
- DC-DC CONVERTERS
- SYNCHRONOUS RECTIFIERS
- DRIVERS



INTERNAL SCHEMATIC DIAGRAM



SEF ≡ IRF
SEFP ≡ MTP
SEFM ≡ MTM

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω)	@ I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
50	0.6	2.5	TO-220	**SEFP5N05**	5.0	50	0.75	250
50	0.3	3.5	SOT-82	**SGSP258**	7.0	40	1.5	270
50	0.3	3.5	TO-220	**SGSP358**	7.0	50	1.5	270
50	0.3	3.5	TO-39	**SGSP158**	5.0	15	1.5	270
50	0.28	5.0	TO-220	**SEFP10N05**	10.0	75	2.5	550
50	0.28	5.0	TO-3	**SEFM10N05**	10.0	75	2.5	550
50	0.2	6.0	TO-220	**SEFP12N05**	12.0	75	3.0	550
50	0.2	6.0	TO-3	**SEFM12N05**	12.0	75	3.0	550
50	0.16	7.5	TO-220	**SEFP15N05**	15.0	75	3.5	550
50	0.16	7.5	TO-3	**SEFM15N05**	15.0	75	3.5	550
50	0.13	5.0	SOT-82	**SGSP222**	10.0	50	3.0	550
50	0.13	5.0	SOT-93	**SGSP422**	10.0	75	3.0	550
50	0.13	5.0	TO-220	**SGSP322**	10.0	75	3.0	550
50	0.13	5.0	TO-3	**SGSP522**	10.0	75	3.0	550
50	0.13	3.5	TO-39	**SGSP122**	7.0	15	2.5	550
50	0.12	6.0	TO-220	**BUZ10A**	12.0	75	3.0	550
50	0.12	6.0	TO-220	**BUZ71A**	12.0	40	3.0	550
50	0.1	6.0	TO-220	**BUZ10**	12.0	75	3.0	550
50	0.1	6.0	TO-220	**BUZ71**	12.0	40	3.0	550
50	0.08	12.5	TO-220	**SEFP25N05**	25.0	100	5.0	1400
50	0.08	12.5	TO-3	**SEFM25N05**	25.0	100	5.0	1400
50	0.06	12.0	SOT-93	**SGSP482**	24.0	125	5.0	1400
50	0.06	12.0	TO-220	**SGSP382**	24.0	100	5.0	1400

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
50	0.06	12.0	TO-3	**SGSP582**	24.0	125	5.0	1400
50	0.055	17.5	SOT-93	**SEFH35N05**	35.0	150	8.0	2500
50	0.055	17.5	TO-3	**SEFM35N05**	35.0	150	8.0	2500
50	0.033	20.0	SOT-93	**SGSP492**	40.0	150	10.0	2400
50	0.033	20.0	TO-3	**SGSP592**	40.0	150	10.0	2400
60	0.8	2.0	TO-220	**SEF513**	3.5	20	1.0	250
60	0.6	2.0	TO-220	**SEF511**	4.0	20	1.0	250
60	0.6	2.5	TO-220	**SEFP5N06**	5.0	50	0.75	250
60	0.4	4.0	TO-220	**SEF523**	7.0	40	1.5	480
60	0.4	4.0	TO-3	**SEF123**	7.0	40	1.5	480
60	0.4	3.0	TO-39	**SEFF123**	5.0	20	1.5	480
60	0.3	3.5	SOT-82	**SGSP257**	7.0	40	1.5	270
60	0.3	4.0	TO-220	**SEF521**	8.0	40	1.5	480
60	0.3	3.5	TO-220	**SGSP357**	7.0	50	1.5	270
60	0.3	4.0	TO-3	**SEF121**	8.0	40	1.5	480
60	0.3	3.0	TO-39	**SEFF121**	6.0	20	1.5	480
60	0.3	3.5	TO-39	**SGSP157**	5.0	15	1.5	270
60	0.28	5.0	TO-220	**SEFP10N06**	10.0	75	2.5	550
60	0.28	5.0	TO-3	**SEFM10N06**	10.0	75	2.5	550
60	0.25	8.0	TO-220	**SEF533**	12.0	75	3.0	1200
60	0.25	8.0	TO-3	**SEF133**	12.0	75	4.0	1200
60	0.2	6.0	TO-220	**SEFP12N06**	12.0	75	3.0	550
60	0.2	6.0	TO-3	**SEFM12N06**	12.0	75	3.0	550
60	0.18	8.0	TO-220	**SEF531**	14.0	75	3.0	1200
60	0.18	8.0	TO-3	**SEF131**	14.0	75	4.0	1200
60	0.16	7.5	TO-220	**SEFP15N06**	15.0	75	3.5	1200
60	0.16	7.5	TO-3	**SEFM15N06**	15.0	75	3.5	550
60	0.13	5.0	SOT-82	**SGSP221**	10.0	50	3.0	550
60	0.13	5.0	SOT-93	**SGSP421**	10.0	75	3.0	550
60	0.13	5.0	TO-220	**SGSP321**	10.0	75	3.0	550
60	0.13	5.0	TO-3	**SGSP521**	10.0	75	3.0	550
60	0.13	3.5	TO-39	**SGSP121**	7.0	15	2.5	550
60	0.11	12.0	TO-220	**SEF543**	24.0	125	5.0	1600
60	0.11	15.0	TO-3	**SEF143**	24.0	125	6.0	2200
60	0.085	15.0	TO-220	**SEF541**	27.0	125	5.0	1600
60	0.085	15.0	TO-3	**SEF141**	27.0	125	6.0	2200
60	0.08	12.5	TO-220	**SEFP25N06**	25.0	100	5.0	1400
60	0.08	20.0	TO-3	**SEF153**	33.0	150	9.0	2200
60	0.08	12.5	TO-3	**SEFM25N06**	25.0	100	5.0	1400
60	0.06	12.0	SOT-93	**SGSP481**	24.0	125	5.0	1400
60	0.06	12.0	TO-220	**SGSP381**	24.0	100	5.0	1400
60	0.06	12.0	TO-3	**SGSP581**	24.0	125	5.0	1400
60	0.055	17.5	SOT-93	**SEFH35N06**	35.0	150	8.0	2500
60	0.055	20.0	TO-3	**SEF151**	40.0	150	9.0	2200

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
60	0.055	17.5	TO-3	**SEFM35N06**	35.0	150	8.0	2500
60	0.05	20.0	SOT-93	**SGSP491**	40.0	150	10.0	2400
60	0.05	20.0	TO-3	**SGSP591**	40.0	150	10.0	2400
80	1.4	0.75	SOT-82	**SGSP202**	1.5	18	0.5	125
80	1.4	0.75	TO-220	**SGSP302**	1.5	18	0.5	125
80	1.4	0.75	TO-39	**SGSP102**	1.5	15	0.5	125
80	0.45	2.5	SOT-82	**SGSP252**	5.0	40	1.5	250
80	0.45	2.5	TO-220	**SGSP352**	5.0	50	1.5	250
80	0.45	2.5	TO-39	**SGSP152**	5.0	15	1.5	250
80	0.33	5.0	TO-220	**SEFP10N08**	10.0	75	2.5	480
80	0.33	5.0	TO-3	**SEFM10N08**	10.0	75	2.5	480
80	0.3	3.5	SOT-82	**SGSP212**	7.0	50	2.0	480
80	0.3	3.5	TO-220	**SGSP312**	7.0	75	2.0	480
80	0.3	3.5	TO-3	**SGSP512**	7.0	75	2.0	480
80	0.3	2.5	TO-39	**SGSP112**	5.0	15	2.0	480
80	0.25	6.0	TO-220	**SEFP12N08**	12.0	75	3.0	1200
80	0.25	6.0	TO-3	**SEFM12N08**	12.0	75	3.0	1200
80	0.1	8.0	SOT-93	**SGSP462**	16.0	125	4.5	1200
80	0.1	8.0	TO-220	**SGSP362**	16.0	100	4.5	1200
80	0.1	8.0	TO-3	**SGSP562**	16.0	125	4.5	1200
80	0.075	12.5	SOT-93	**SEFH25N08**	25.0	150	5.0	2200
80	0.075	12.5	TO-3	**SEFM25N08**	25.0	150	5.0	2200
80	0.05	15.0	SOT-93	**SGSP472**	30.0	150	9.0	2200
80	0.05	15.0	TO-3	**SGSP572**	30.0	150	9.0	2200
100	1.4	0.75	SOT-82	**SGSP201**	1.5	18	0.5	125
100	1.4	0.75	TO-220	**SGSP301**	1.5	18	0.5	125
100	1.4	0.75	TO-39	**SGSP101**	1.5	15	0.5	125
100	0.8	2.0	TO-220	**SEF512**	3.5	20	1.0	250
100	0.6	2.0	TO-220	**SEF510**	4.0	20	1.0	250
100	0.45	2.5	SOT-82	**SGSP251**	5.0	40	1.5	250
100	0.45	2.5	TO-220	**SGSP351**	5.0	50	1.5	250
100	0.45	2.5	TO-39	**SGSP151**	5.0	15	1.5	250
100	0.4	4.0	TO-220	**SEF522**	7.0	40	1.5	480
100	0.4	4.0	TO-3	**SEF122**	7.0	40	1.5	480
100	0.4	3.0	TO-39	**SEFF122**	5.0	20	1.5	480
100	0.33	5.0	TO-220	**SEFP10N10**	10.0	75	2.5	480
100	0.33	5.0	TO-3	**SEFM10N10**	10.0	75	2.0	480
100	0.3	3.5	SOT-82	**SGSP211**	7.0	50	2.0	480
100	0.3	4.0	TO-220	**SEF520**	8.0	40	1.5	480
100	0.3	3.5	TO-220	**SGSP311**	7.0	75	2.0	480
100	0.3	4.0	TO-3	**SEF120**	8.0	40	1.5	480
100	0.3	3.5	TO-3	**SGSP511**	7.0	75	2.0	480
100	0.3	3.0	TO-39	**SEFF120**	6.0	20	1.5	480

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
100	0.3	2.5	TO-39	SGSP111	5.0	15	2.0	480
100	0.25	5.0	TO-220	BUZ72A	9.0	40	2.7	480
100	0.25	8.0	TO-220	SEF532	12.0	75	4.0	1200
100	0.25	6.0	TO-220	SEFP12N10	12.0	75	3.0	1200
100	0.25	8.0	TO-3	SEF132	12.0	75	4.0	1200
100	0.25	6.0	TO-3	SEFM12N10	12.0	75	3.0	1200
100	0.18	8.0	TO-220	SEF530	14.0	75	4.0	1200
100	0.18	8.0	TO-3	SEF130	14.0	75	4.0	1200
100	0.15	8.0	SOT-93	SGSP461	16.0	125	4.5	1200
100	0.15	8.0	TO-220	SGSP361	16.0	100	4.5	1200
100	0.15	8.0	TO-3	SGSP561	16.0	125	4.5	1200
100	0.11	15.0	TO-220	SEF542	24.0	125	5.0	1600
100	0.11	15.0	TO-3	SEF142	24.0	125	6.0	2200
100	0.085	15.0	TO-3	SEF140	27.0	125	6.0	2200
100	0.08	20.0	TO-3	SEF152	33.0	150	9.0	2200
100	0.075	12.5	SOT-93	SEFH25N10	25.0	150	5.0	2200
100	0.075	15.0	SOT-93	SGSP471	30.0	150	9.0	2200
100	0.075	12.5	TO-3	SEFM25N10	25.0	150	5.0	2200
100	0.075	15.0	TO-3	SGSP571	30.0	150	9.0	2200
100	0.055	20.0	TO-3	SEF150	40.0	150	9.0	2200
150	1.2	2.5	TO-220	SEF623	4.0	40	1.3	500
150	1.2	2.5	TO-3	SEF223	4.0	40	1.3	500
150	0.8	2.5	TO-220	SEF621	5.0	40	1.3	500
150	0.8	2.5	TO-3	SEF221	5.0	40	1.3	500
150	0.6	5.0	TO-220	SEF633	8.0	75	3.0	1200
150	0.6	5.0	TO-3	SEF233	8.0	75	3.0	1200
150	0.4	5.0	TO-220	SEF631	9.0	75	3.0	1200
150	0.4	5.0	TO-3	SEF231	9.0	75	3.0	1200
150	0.22	10.0	TO-3	SEF243	16.0	125	6.0	2200
150	0.18	10.0	TO-3	SEF241	18.0	125	6.0	2200
180	1.0	2.5	TO-220	SEFP5N18	5.0	75	1.5	500
180	1.0	2.5	TO-3	SEFM5N18	5.0	75	1.5	500
180	0.4	4.0	TO-220	SEFP8N18	8.0	75	3.0	1200
180	0.4	4.0	TO-3	SEFM8N18	8.0	75	3.0	1200
180	0.16	7.5	SOT-93	SEFH15N18	15.0	150	4.0	2500
180	0.16	7.5	TO-3	SEFM15N18	15.0	150	4.0	2500
200	1.2	2.5	TO-220	SEF622	4.0	40	1.3	500
200	1.2	2.5	TO-3	SEF222	4.0	40	1.3	500
200	1.0	2.5	TO-220	SEFP5N20	5.0	75	1.5	500
200	1.0	2.5	TO-3	SEFM5N20	5.0	75	1.5	500
200	0.8	2.5	TO-220	SEF620	5.0	40	1.3	500
200	0.8	2.5	TO-3	SEF220	5.0	40	1.3	500
200	0.75	3.0	SOT-82	SGSP217	6.0	50	1.5	500

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
200	0.75	3.0	TO-220	**SGSP317**	6.0	75	1.5	500
200	0.75	3.0	TO-3	**SGSP517**	6.0	75	1.5	500
200	0.75	2.0	TO-39	**SGSP117**	4.0	15	1.5	500
200	0.6	5.0	TO-220	**SEF632**	8.0	75	3.0	1200
200	0.6	5.0	TO-3	**SEF232**	8.0	75	3.0	1200
200	0.4	5.0	TO-220	**SEF630**	9.0	75	3.0	1200
200	0.4	4.0	TO-220	**SEFP8N20**	8.0	75	3.0	1200
200	0.4	5.0	TO-3	**SEF230**	9.0	75	3.0	1200
200	0.4	4.0	TO-3	**SEFM8N20**	8.0	75	3.0	1200
200	0.33	5.0	SOT-93	**SGSP467**	10.0	100	3.0	1200
200	0.33	5.0	TO-220	**SGSP367**	10.0	100	3.0	1200
200	0.33	5.0	TO-3	**SGSP567**	10.0	125	3.0	1200
200	0.22	10.0	TO-3	**SEF242**	16.0	125	6.0	2200
200	0.18	10.0	TO-3	**SEF240**	18.0	125	6.0	2200
200	0.17	10.0	SOT-93	**SGSP477**	20.0	150	8.0	2200
200	0.17	10.0	TO-3	**SGSP577**	20.0	150	8.0	2200
200	0.16	7.5	SOT-93	**SEFH15N20**	15.0	150	4.0	2500
200	0.16	7.5	TO-3	**SEFM15N20**	15.0	150	4.0	2500
250	1.2	3.0	SOT-82	**SGSP216**	6.0	50	1.5	500
250	1.2	3.0	TO-220	**SGSP316**	6.0	75	1.5	500
250	1.2	3.0	TO-3	**SGSP516**	6.0	75	1.5	500
250	1.2	2.0	TO-39	**SGSP116**	4.0	15	1.5	500
250	0.45	5.0	SOT-93	**SGSP463**	10.0	100	3.0	1200
250	0.45	5.0	TO-220	**SGSP363**	10.0	100	3.0	1200
250	0.45	5.0	TO-3	**SGSP563**	10.0	125	3.0	1200
250	0.22	10.0	SOT-93	**SGSP473**	20.0	150	8.0	2200
250	0.22	10.0	TO-3	**SGSP573**	20.0	150	8.0	2200
350	20.0	0.3	SOT-82	**SGSP242**	0.6	18	0.2	105
350	20.0	0.3	TO-220	**SGSP342**	0.6	18	0.2	105
350	20.0	0.3	TO-39	**SGSP142**	0.6	15	0.2	105
350	5.0	0.75	SOT-82	**SGSP256**	1.5	40	0.85	250
350	5.0	0.8	TO-220	**SEF713**	1.3	20	0.5	450
350	5.0	0.75	TO-220	**SGSP356**	1.5	50	0.85	250
350	5.0	0.75	TO-39	**SGSP156**	1.5	15	0.85	250
350	3.6	0.8	TO-220	**SEF711**	1.5	20	0.5	450
350	3.3	1.5	TO-220	**SEFP3N35**	3.0	75	0.75	450
350	3.3	1.5	TO-3	**SEFM3N35**	3.0	75	0.75	450
350	2.5	1.5	SOT-82	**SGSP232**	3.0	50	1.5	450
350	2.5	1.5	TO-220	**SEF723**	2.5	40	1.0	1000
350	2.5	1.5	TO-220	**SGSP332**	3.0	75	1.5	450
350	2.5	1.5	TO-3	**SEF323**	2.5	40	1.0	1000
350	2.5	1.5	TO-3	**SGSP532**	3.0	75	1.5	450
350	2.5	1.5	TO-39	**SGSP132**	3.0	15	1.5	450

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
350	2.0	2.5	TO-220	**SEFP5N35**	5.0	75	2.0	1000
350	1.8	1.5	TO-220	**SEF721**	3.0	40	1.0	1000
350	1.8	1.5	TO-3	**SEF321**	3.0	40	1.0	1000
350	1.5	3.0	TO-220	**SEF733**	4.5	75	3.0	1000
350	1.5	3.0	TO-3	**SEF333**	4.5	75	3.0	1000
350	1.0	3.0	SOT-93	**SGSP466**	6.0	125	3.0	1000
350	1.0	3.0	TO-220	**SEF731**	5.5	75	3.0	1000
350	1.0	3.0	TO-220	**SGSP366**	6.0	100	3.0	1000
350	1.0	3.0	TO-3	**SEF331**	5.5	75	3.0	1000
350	1.0	2.5	TO-3	**SEFM5N35**	5.0	75	2.0	1000
350	1.0	3.0	TO-3	**SGSP566**	6.0	125	3.0	1000
350	0.8	4.0	SOT-93	**SEFH8N35**	8.0	150	3.0	2100
350	0.8	5.0	TO-3	**SEF343**	8.0	125	4.0	2100
350	0.8	4.0	TO-3	**SEFM8N35**	8.0	150	3.0	2100
350	0.55	6.0	SOT-93	**SGSP476**	12.0	150	6.0	2100
350	0.55	5.0	TO-3	**SEF341**	10.0	125	4.0	2100
350	0.55	6.0	TO-3	**SGSP576**	12.0	150	6.0	2100
400	20.0	0.3	SOT-82	**SGSP241**	0.6	18	0.2	105
400	20.0	0.3	TO-220	**SGSP341**	0.6	75	0.2	105
400	20.0	0.3	TO-39	**SGSP141**	0.6	15	0.2	105
400	5.0	0.75	SOT-82	**SGSP255**	1.5	40	0.85	250
400	5.0	0.75	TO-220	**SGSP355**	1.5	50	0.85	250
400	5.0	0.75	TO-39	**SGSP155**	1.5	15	0.85	250
400	5.0	0.8	TO-220	**SEF712**	1.3	20	0.5	450
400	3.6	0.8	TO-220	**SEF710**	1.5	20	0.5	450
400	3.3	1.5	TO-220	**SEFP3N40**	3.0	75	0.75	450
400	3.3	1.5	TO-3	**SEFM3N40**	3.0	75	0.75	450
400	2.5	1.5	SOT-82	**SGSP231**	3.0	50	1.5	450
400	2.5	1.5	TO-220	**BUZ76A**	2.6	40	2.0	450
400	2.5	1.5	TO-220	**SEF722**	2.5	40	1.0	1000
400	2.5	1.5	TO-220	**SGSP331**	3.0	75	1.5	450
400	2.5	1.5	TO-3	**SEF322**	2.5	40	1.0	1000
400	2.5	1.5	TO-3	**SGSP531**	3.0	75	1.5	450
400	2.5	1.5	TO-39	**SGSP131**	3.0	15	1.5	450
400	1.8	1.5	TO-220	**BUZ76**	3.0	40	2.0	450
400	1.8	1.5	TO-220	**SEF720**	3.0	40	1.0	1000
400	1.8	1.5	TO-3	**SEF320**	3.0	40	1.0	1000
400	1.5	3.0	TO-220	**SEF732**	4.5	75	3.0	1000
400	1.5	3.0	TO-3	**SEF332**	4.5	75	3.0	1000
400	1.0	3.0	SOT-93	**SGSP465**	6.0	125	3.0	1000
400	1.0	3.0	TO-220	**SEF730**	5.5	75	3.0	1000
400	1.0	2.5	TO-220	**SEFP5N40**	5.0	75	2.0	1000
400	1.0	3.0	TO-220	**SGSP365**	6.0	100	3.0	1000
400	1.0	3.0	TO-3	**SEF330**	5.5	75	3.0	1000

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
400	1.0	2.5	TO-3	**SEFM5N40**	5.0	75	2.0	1000
400	1.0	3.0	TO-3	**SGSP565**	6.0	125	3.0	1000
400	0.8	5.0	TO-3	**SEF342**	8.0	125	4.0	2100
400	0.55	4.0	SOT-93	**SEFH8N40**	8.0	150	3.0	2100
400	0.55	6.0	SOT-93	**SGSP475**	12.0	150	6.0	2100
400	0.55	5.0	TO-3	**SEF340**	10.0	125	4.0	2100
400	0.55	4.0	TO-3	**SEFM8N40**	8.0	150	3.0	2100
400	0.55	6.0	TO-3	**SGSP575**	12.0	150	6.0	2100
450	20.0	0.3	SOT-82	**SGSP240**	0.6	18	0.2	105
450	20.0	0.3	TO-220	**SGSP340**	0.6	18	0.2	105
450	20.0	0.3	TO-39	**SGSP140**	0.6	15	0.2	105
450	6.5	0.75	SOT-82	**SGSP254**	1.5	40	0.85	250
450	6.5	0.75	TO-220	**SGSP354**	1.5	50	0.85	250
450	6.5	0.75	TO-39	**SGSP154**	1.5	15	0.85	250
450	4.0	1.0	TO-220	**SEF823**	2.0	40	1.0	800
450	4.0	1.0	TO-220	**SEFP2N45**	2.0	75	1.0	500
450	4.0	1.0	TO-3	**SEF423**	2.0	40	1.0	800
450	4.0	1.0	TO-3	**SEFM2N45**	4.0	75	1.0	500
450	3.0	1.5	SOT-82	**SGSP230**	3.0	50	1.5	450
450	3.0	1.0	TO-220	**SEF821**	2.5	40	1.0	800
450	3.0	1.5	TO-220	**SGSP330**	3.0	75	1.5	450
450	3.0	1.0	TO-3	**SEF421**	2.5	40	1.0	800
450	3.0	1.5	TO-3	**SGSP530**	3.0	75	1.5	450
450	3.0	1.5	TO-39	**SGSP130**	3.0	15	1.5	450
450	2.0	2.5	TO-220	**SEF833**	4.0	75	2.5	1200
450	2.0	2.5	TO-3	**SEF433**	4.0	75	2.5	1200
450	1.5	3.0	SOT-93	**SGSP464**	6.0	125	3.0	1000
450	1.5	2.5	TO-220	**SEF830**	4.5	75	2.5	1200
450	1.5	2.5	TO-220	**SEF831**	4.5	75	2.5	1200
450	1.5	2.0	TO-220	**SEFP4N45**	4.0	75	1.5	1000
450	1.5	3.0	TO-220	**SGSP364**	6.0	100	3.0	1000
450	1.5	2.5	TO-3	**SEF431**	4.5	75	2.5	1200
450	1.5	2.0	TO-3	**SEFM4N45**	4.0	75	1.5	1000
450	1.5	3.0	TO-3	**SGSP564**	6.0	125	3.0	1000
450	1.1	4.0	TO-3	**SEF443**	7.0	125	4.0	2100
450	0.85	4.0	TO-3	**SEF441**	8.0	125	4.0	2100
450	0.8	3.5	SOT-93	**SEFH7N45**	7.0	150	2.0	2100
450	0.7	6.0	SOT-93	**SGSP474**	12.0	150	6.0	2100
450	0.8	3.5	TO-3	**SEFM7N45**	7.0	150	2.0	2100
450	0.7	6.0	TO-3	**SGSP574**	12.0	150	6.0	2100
500	40.0	0.3	SOT-82	**SGSP249**	0.5	18	0.18	95
500	40.0	0.3	TO-220	**SGSP349**	0.5	18	0.18	95
500	40.0	0.3	TO-39	**SGSP149**	0.5	15	0.18	95

N-CHANNEL POWER MOS TRANSISTORS

VERY FAST SWITCHING AND/OR EASY DRIVING (continued)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	I_D (max) (A)	P_{tot} (W)	g_{fs} (min) (℧)	C_{iss} (max) (pF)
500	8.5	0.6	SOT-82	**SGSP239**	1.2	40	0.65	220
500	8.5	0.6	TO-220	**SGSP339**	1.2	50	0.65	220
500	8.5	0.6	TO-39	**SGSP139**	1.2	15	0.65	220
500	4.0	1.0	TO-220	**SEF822**	2.0	40	1.0	800
500	4.0	1.0	TO-3	**SEF422**	2.0	40	1.0	800
500	3.8	1.0	SOT-82	**SGSP219**	2.0	50	1.2	380
500	3.8	1.0	TO-220	**SGSP319**	2.0	75	1.2	380
500	3.8	1.0	TO-3	**SGSP519**	2.0	75	1.2	380
500	3.8	1.0	TO-39	**SGSP119**	2.0	15	1.2	380
500	3.0	1.0	TO-220	**SEF820**	2.5	40	1.0	800
500	3.0	1.0	TO-3	**SEF420**	2.5	40	1.0	800
500	2.0	2.5	TO-220	**SEF832**	4.0	75	2.5	1200
500	2.0	2.5	TO-3	**SEF432**	4.0	75	2.5	1200
500	1.5	2.5	SOT-93	**SGSP469**	5.0	125	3.0	800
500	1.5	2.5	TO-220	**SGSP369**	5.0	100	3.0	800
500	1.5	2.5	TO-3	**SGSP569**	5.0	125	3.0	800
500	1.5	2.0	TO-220	**SEFP4N50**	4.0	75	1.5	1200
500	1.5	2.5	TO-3	**SEF430**	4.5	75	2.5	1200
500	1.5	2.0	TO-3	**SEFM4N50**	4.0	75	1.5	1200
500	1.1	4.0	TO-3	**SEF442**	7.0	125	4.0	2100
500	0.85	4.0	TO-3	**SEF440**	8.0	125	4.0	2100
500	0.8	3.5	SOT-93	**SEFH7N50**	7.0	150	2.0	1900
500	0.8	3.5	TO-3	**SEFM7N50**	7.0	150	2.0	1900
500	0.7	5.0	SOT-93	**SGSP479**	10.0	150	5.0	1900
500	0.7	5.0	TO-3	**SGSP579**	10.0	150	5.0	1900
550	40.0	0.3	SOT-82	**SGSP248**	0.5	18	0.18	95
550	40.0	0.3	TO-220	**SGSP348**	0.5	18	0.18	95
550	40.0	0.3	TO-39	**SGSP148**	0.5	15	0.18	95
550	11.0	0.6	SOT-82	**SGSP238**	1.2	40	0.65	220
550	11.0	0.6	TO-220	**SGSP338**	1.2	50	0.65	220
550	11.0	0.6	TO-39	**SGSP138**	1.2	15	0.65	220
550	4.5	1.0	SOT-82	**SGSP218**	2.0	50	1.2	380
550	4.5	1.0	TO-220	**SGSP318**	2.0	75	1.2	380
550	4.5	1.0	TO-3	**SGSP518**	2.0	75	1.2	380
550	4.5	1.0	TO-39	**SGSP118**	2.0	15	1.2	380
550	2.5	2.5	SOT-93	**SGSP468**	5.0	125	3.0	800
550	2.5	1.5	TO-220	**SEFP3N55**	3.0	75	1.5	1200
550	2.5	2.5	TO-220	**SGSP368**	5.0	100	3.0	800
550	2.5	1.5	TO-3	**SEFM3N55**	2.5	75	1.5	1600
550	2.5	2.5	TO-3	**SGSP568**	5.0	125	3.0	800
550	1.5	3.0	SOT-93	**SEFH6N55**	6.0	150	2.0	1900
550	1.5	3.0	TO-3	**SEFM6N55**	6.0	150	2.0	1900
550	1.0	5.0	SOT-93	**SGSP478**	10.0	150	5.0	1900
550	1.0	5.0	TO-3	**SGSP578**	10.0	150	5.0	1900

SHORTFORM CATALOGUE (Sorted by part number)

Device	$V_{(BR)DSS}$ V	I_D (MAX) A	$R_{DS(on)}$ max (Ω) @	I_D (A)	P_{tot} (W)	g_{fs} min (℧)	C_{ISS} max (pF)	Package
SGSP101	100	1.5	1.4	0.75	15	0.5	125	TO-39
SGSP102	80	1.5	1.4	0.75	15	0.5	125	TO-39
SGSP111	100	5	0.3	2.5	15	2	480	TO-39
SGSP112	80	5	0.3	2.5	15	2	480	TO-39
SGSP116	250	4	1.2	2	15	1.5	500	TO-39
SGSP117	200	4	0.75	2	15	1.5	500	TO-39
SGSP118	550	2	4.5	1	15	1.2	380	TO-39
SGSP119	500	2	3.8	1	15	1.2	380	TO-39
SGSP121	60	7	0.13	3.5	15	2.5	550	TO-39
SGSP122	50	7	0.13	3.5	15	2.5	550	TO-39
SGSP130	450	3	3	1.5	15	1.5	450	TO-39
SGSP131	400	3	2.5	1.5	15	1.5	450	TO-39
SGSP132	350	3	2.5	1.5	15	1.5	450	TO-39
SGSP138	550	1.2	11	0.6	15	0.65	220	TO-39
SGSP139	500	1.2	8.5	0.6	15	0.65	220	TO-39
SGSP140	450	0.6	20	0.3	15	0.2	105	TO-39
SGSP141	400	0.6	20	0.3	15	0.2	105	TO-39
SGSP142	350	0.6	20	0.3	15	0.2	105	TO-39
SGSP148	550	0.5	40	0.3	15	0.18	95	TO-39
SGSP149	500	0.5	40	0.3	15	0.18	95	TO-39
SGSP151	100	5	0.45	2.5	15	1.5	250	TO-39
SGSP152	80	5	0.45	2.5	15	1.5	250	TO-39
SGSP154	450	1.5	6.5	0.75	15	0.85	250	TO-39
SGSP155	400	1.5	5	0.75	15	0.85	250	TO-39
SGSP156	350	1.5	5	0.75	15	0.85	250	TO-39
SGSP157	60	5	0.3	3.5	15	1.5	270	TO-39
SGSP158	50	5	0.3	3.5	15	1.5	270	TO-39
SGSP201	100	1.5	1.4	0.75	18	0.5	125	SOT-82
SGSP202	80	1.5	1.4	0.75	18	0.5	125	SOT-82
SGSP211	100	7	0.3	3.5	50	2	480	SOT-82
SGSP212	80	7	0.3	3.5	50	2	480	SOT-82
SGSP216	250	6	1.2	3	50	1.5	500	SOT-82
SGSP217	200	6	0.75	3	50	1.5	500	SOT-82
SGSP218	550	2	4.5	1	50	1.2	380	SOT-82
SGSP219	500	2	3.8	1	50	1.2	380	SOT-82
SGSP221	60	10	0.13	5	50	3	550	SOT-82
SGSP222	50	10	0.13	5	50	3	550	SOT-82
SGSP230	450	3	3	1.5	50	1.5	450	SOT-82
SGSP231	400	3	2.5	1.5	50	1.5	450	SOT-82
SGSP232	350	3	2.5	1.5	50	1.5	450	SOT-82
SGSP238	550	1.2	11	0.6	40	0.65	220	SOT-82
SGSP239	500	1.2	8.5	0.6	40	0.65	220	SOT-82
SGSP240	450	0.6	20	0.3	18	0.2	105	SOT-82
SGSP241	400	0.6	20	0.3	18	0.2	105	SOT-82
SGSP242	350	0.6	20	0.3	18	0.2	105	SOT-82
SGSP248	550	0.5	40	0.3	18	0.18	95	SOT-82
SGSP249	500	0.5	40	0.3	18	0.18	95	SOT-82
SGSP251	100	5	0.45	2.5	40	1.5	250	SOT-82
SGSP252	80	5	0.45	2.5	40	1.5	250	SOT-82
SGSP254	450	1.5	6.5	0.75	40	0.85	250	SOT-82
SGSP255	400	1.5	5	0.75	40	0.85	250	SOT-82
SGSP256	350	1.5	5	0.75	40	0.85	250	SOT-82
SGSP257	60	7	0.3	3.5	40	1.5	270	SOT-82
SGSP258	50	7	0.3	3.5	40	1.5	270	SOT-82
SGSP301	100	1.5	1.4	0.75	18	0.5	125	TO-220
SGSP302	80	1.5	1.4	0.75	18	0.5	125	TO-220
SGSP311	100	7	0.3	3.5	75	2	480	TO-220
SGSP312	80	7	0.3	3.5	75	2	480	TO-220
SGSP316	250	6	1.2	3	75	1.5	500	TO-220
SGSP317	200	6	0.75	3	75	1.5	500	TO-220

SHORTFORM CATALOGUE (Sorted by part number)

Device	$V_{(BR)DSS}$ V	I_D (MAX) A	$R_{DS(on)}$ max (Ω)	@ I_D (A)	P_{tot} (W)	g_{fs} min (℧)	C_{ISS} max (pF)	Package
SGSP318	550	2	4.5	1	75	1.2	380	TO-220
SGSP319	500	2	. 3.8	1	75	1.2	380	TO-220
SGSP321	60	10	0.13	5	75	3	550	TO-220
SGSP322	50	10	0.13	5	75	3	550	TO-220
SGSP330	450	3	3	1.5	75	1.5	450	TO-220
SGSP331	400	3	2.5	1.5	75	1.5	450	TO-220
SGSP332	350	3	2.5	1.5	75	1.5	450	TO-220
SGSP338	550	1.2	11	0.6	50	0.65	220	TO-220
SGSP339	500	1.2	8.5	0.6	50	0.65	220	TO-220
SGSP340	450	0.6	20	0.3	18	0.2	105	TO-220
SGSP341	400	0.6	20	0.3	75	0.2	105	TO-220
SGSP342	350	0.6	20	0.3	18	0.2	105	TO-220
SGSP348	550	0.6	40	0.3	18	0.18	95	TO-220
SGSP349	500	0.5	40	0.3	18	0.18	95	TO-220
SGSP351	100	5	0.45	2.5	50	1.5	250	TO-220
SGSP352	80	5	0.45	2.5	50	1.5	250	TO-220
SGSP354	450	1.5	6.5	0.75	50	0.85	250	TO-220
SGSP355	400	1.5	5	0.75	50	0.85	250	TO-220
SGSP356	350	1.5	5	0.75	50	0.85	250	TO-220
SGSP357	60	7	0.3	3.5	50	1.5	270	TO-220
SGSP358	50	7	0.3	3.5	50	1.5	270	TO-220
SGSP361	100	16	0.15	8	100	4.5	1200	TO-220
SGSP362	80	16	0.1	8	100	4.5	1200	TO-220
SGSP363	250	10	0.45	5	100	3	1200	TO-220
SGSP364	450	6	1.5	3	100	3	1000	TO-220
SGSP365	400	6	1	3	100	3	1000	TO-220
SGSP366	350	6	1	3	100	3	1000	TO-220
SGSP367	200	10	0.33	5	100	3	1200	TO-220
SGSP368	550	5	2.5	2.5	100	3	1000	TO-220
SGSP369	500	5	1.5	2.5	100	3	1000	TO-220
SGSP381	60	24	0.06	12	100	5	1400	TO-220
SGSP382	50	24	0.06	12	100	5	1400	TO-220
SGSP421	60	10	0.13	5	75	3	550	SOT-93*
SGSP422	50	10	0.13	5	75	3	550	SOT-93*
SGSP461	100	16	0.15	8	125	4.5	1200	SOT-93*
SGSP462	80	16	0.1	8	125	4.5	1200	SOT-93*
SGSP463	250	10	0.45	5	100	3	1200	SOT-93*
SGSP464	450	6	1.5	3	125	3	1000	SOT-93*
SGSP465	400	6	1	3	125	3	1000	SOT-93*
SGSP466	350	6	1	3	125	3	1000	SOT-93*
SGSP467	200	10	0.33	5	100	3	1200	SOT-93*
SGSP468	550	5	2.5	2.5	125	3	1000	SOT-93*
SGSP469	500	5	1.5	2.5	125	3	1000	SOT-93*
SGSP471	100	30	0.075	15	150	9	2200	SOT-93*
SGSP472	80	30	0.05	15	150	9	2200	SOT-93*
SGSP473	250	20	0.22	10	150	8	2200	SOT-93*
SGSP474	450	12	0.7	6	150	6	2100	SOT-93*
SGSP475	400	12	0.55	6	150	6	2100	SOT-93*
SGSP476	350	12	0.55	6	150	6	2100	SOT-93*
SGSP477	200	20	0.17	10	150	8	2200	SOT-93*
SGSP478	550	10	1	5	150	5	1900	SOT-93*
SGSP479	500	10	0.7	5	150	5	1900	SOT-93*
SGSP481	60	24	0.06	12	125	5	1400	SOT-93*
SGSP482	50	24	0.06	12	125	5	1400	SOT-93*
SGSP491	60	40	0.05	20	150	10	2400	SOT-93*
SGSP492	50	40	0.033	20	150	10	2400	SOT-93*
SGSP511	100	7	0.3	3.5	75	2	480	TO-3
SGSP512	80	7	0.3	3.5	75	2	480	TO-3
SGSP516	250	6	1.2	3	75	1.5	500	TO-3
SGSP517	200	6	0.75	3	75	1.5	500	TO-3

(*) JEDEC number: TO-218

SHORTFORM CATALOGUE (Sorted by part number)

Device	$V_{(BR)DSS}$ V	I_D (MAX) A	$R_{DS(on)}$ max (Ω)	@ I_D (A)	P_{tot} (W)	g_{fs} min	C_{ISS} max (pF)	Package
SGSP518	550	2	4.5	1	75	1.2	380	TO-3
SGSP519	500	2	3.8	1	75	1.2	380	TO-3
SGSP521	60	10	0.13	5	75	3	550	TO-3
SGSP522	50	10	0.13	5	75	3	550	TO-3
SGSP530	450	3	3	1.5	75	1.5	450	TO-3
SGSP531	400	3	2.5	1.5	75	1.5	450	TO-3
SGSP532	350	3	2.5	1.5	75	1.5	450	TO-3
SGSP561	100	16	0.15	8	125	4.5	1200	TO-3
SGSP562	80	16	0.1	8	125	4.5	1200	TO-3
SGSP563	250	10	0.45	5	125	3	1200	TO-3
SGSP564	450	6	1.5	3	125	3	1000	TO-3
SGSP565	400	6	1	3	125	3	1000	TO-3
SGSP566	350	6	1	3	125	3	1000	TO-3
SGSP567	200	10	0.33	5	125	3	1200	TO-3
SGSP568	550	5	2.5	2.5	125	3	1000	TO-3
SGSP569	500	5	1.5	2.5	125	3	1000	TO-3
SGSP571	100	30	0.075	15	150	9	2200	TO-3
SGSP572	80	30	0.05	15	150	9	2200	TO-3
SGSP573	250	20	0.22	10	150	8	2200	TO-3
SGSP574	450	12	0.7	6	150	6	2100	TO-3
SGSP575	400	12	0.55	6	150	6	2100	TO-3
SGSP576	350	12	0.55	6	150	6	2100	TO-3
SGSP577	200	20	0.17	10	150	8	2200	TO-3
SGSP578	550	10	1	5	150	5	1900	TO-3
SGSP579	500	10	0.7	5	150	5	1900	TO-3
SGSP581	60	24	0.06	12	125	5	1400	TO-3
SGSP582	50	24	0.06	12	125	5	1400	TO-3
SGSP591	60	40	0.05	20	150	10	2400	TO-3
SGSP592	50	40	0.033	20	150	10	2400	TO-3
BUZ10	50	12	0.1	6	75	3	550	TO-220
BUZ10A	50	12	0.12	6	75	3	550	TO-220
BUZ71	50	12	0.1	6	40	3	550	TO-220
BUZ71A	50	12	0.12	6	40	3	550	TO-220
BUZ72A	100	9	0.25	5	40	2.7	480	TO-220
BUZ76	400	3	1.8	1.5	40	2	450	TO-220
BUZ76A	400	2.6	2.5	1.5	40	2	450	TO-220
SEF120	100	8	0.3	4	40	1.5	480	TO-3
SEF121	60	8	0.3	4	40	1.5	480	TO-3
SEF122	100	7	0.4	4	40	1.5	480	TO-3
SEF123	60	7	0.4	4	40	1.5	480	TO-3
SEF130	100	14	0.18	8	75	4	1200	TO-3
SEF131	60	14	0.18	8	75	4	1200	TO-3
SEF132	100	12	0.25	8	75	4	1200	TO-3
SEF133	60	12	0.25	8	75	4	1200	TO-3
SEF140	100	27	0.085	15	125	6	2200	TO-3
SEF141	60	27	0.085	15	125	6	2200	TO-3
SEF142	100	24	0.11	15	125	6	2200	TO-3
SEF143	60	24	0.11	15	125	6	2200	TO-3
SEF150	100	40	0.055	15	150	9	2200	TO-3
SEF151	60	40	0.055	15	150	9	2200	TO-3
SEF152	100	33	0.08	15	150	9	2200	TO-3
SEF153	60	33	0.08	15	150	9	2200	TO-3
SEF220	200	5	0.8	2.5	40	1.3	500	TO-3
SEF221	150	5	0.8	2.5	40	1.3	500	TO-3
SEF222	200	4	1.2	2.5	40	1.3	500	TO-3
SEF223	150	4	1.2	2.5	40	1.3	500	TO-3
SEF230	200	9	0.4	5	75	3	1200	TO-3
SEF231	150	9	0.4	5	75	3	1200	TO-3
SEF232	200	9	0.6	5	75	3	1200	TO-3
SEF233	150	8	0.6	5	75	3	1200	TO-3

SHORTFORM CATALOGUE (Sorted by part number)

Device	$V_{(BR)DSS}$ V	I_D (MAX) A	$R_{DS(on)}$ max (Ω) @	I_D (A)	P_{tot} (W)	g_{fs} min (℧)	C_{ISS} max (pF)	Package
SEF240	200	18	0.18	10	125	6	2200	TO-3
SEF241	150	18	0.18	10	125	6	2200	TO-3
SEF242	200	16	0.22	10	125	6	2200	TO-3
SEF243	150	16	0.22	10	125	6	2200	TO-3
SEF320	400	3	1.8	1.5	40	1	1000	TO-3
SEF321	350	3	1.8	1.5	40	1	1000	TO-3
SEF322	400	2.5	2.5	1.5	40	1	1000	TO-3
SEF323	350	2.5	2.5	1.5	40	1	1000	TO-3
SEF330	400	5.5	1	3	75	3	1000	TO-3
SEF331	350	5.5	1	3	75	3	1000	TO-3
SEF332	400	4.5	1.5	3	75	3	1000	TO-3
SEF333	350	4.5	1.5	3	75	3	1000	TO-3
SEF340	400	10	0.55	5	125	4	2100	TO-3
SEF341	350	10	0.55	5	125	4	2100	TO-3
SEF342	400	8	0.8	5	125	4	2100	TO-3
SEF343	350	8	0.8	5	125	4	2100	TO-3
SEF420	500	2.5	3	1	40	1	1000	TO-3
SEF421	450	2.5	3	1	40	1	1000	TO-3
SEF422	500	2	4	1	40	1	1000	TO-3
SEF423	450	2	4	1	40	1	1000	TO-3
SEF430	500	4.5	1.5	2.5	75	2.5	1200	TO-3
SEF431	450	4.5	1.5	2.5	75	2.5	1200	TO-3
SEF432	500	4	2	2.5	75	2.5	1200	TO-3
SEF433	450	4	2	2.5	75	2.5	1200	TO-3
SEF440	500	8	0.85	4	125	4	2100	TO-3
SEF441	450	8	0.85	4	125	4	2100	TO-3
SEF442	500	7	1.1	4	125	4	2100	TO-3
SEF443	450	7	1.1	4	125	4	2100	TO-3
SEF510	100	4	0.6	2	20	1	250	TO-220
SEF511	60	4	0.6	2	20	1	250	TO-220
SEF512	100	3.5	0.8	2	20	1	250	TO-220
SEF513	60	3.5	0.8	2	20	1	250	TO-220
SEF520	100	8	0.3	4	40	1.5	480	TO-220
SEF521	60	8	0.3	4	40	1.5	480	TO-220
SEF522	100	7	0.4	4	40	1.5	480	TO-220
SEF523	60	7	0.4	4	40	1.5	480	TO-220
SEF530	100	14	0.18	8	75	4	1200	TO-220
SEF531	60	14	0.18	5	75	3	1200	TO-220
SEF532	100	12	0.25	8	75	4	1200	TO-220
SEF533	60	12	0.25	5	75	3	1200	TO-220
SEF541	60	27	0.085	12	125	5	1600	TO-220
SEF542	100	24	0.11	12	125	5	1600	TO-220
SEF543	60	24	0.11	12	125	5	1600	TO-220
SEF620	200	5	0.8	2.5	40	1.3	500	TO-220
SEF621	150	5	0.8	2.5	40	1.3	500	TO-220
SEF622	200	4	1.2	2.5	40	1.3	500	TO-220
SEF623	150	4	1.2	2.5	40	1.3	500	TO-220
SEF630	200	9	0.4	5	75	3	1200	TO-220
SEF631	150	9	0.4	5	75	3	1200	TO-220
SEF632	200	8	0.6	5	75	3	1200	TO-220
SEF633	150	8	0.6	5	75	3	1200	TO-220
SEF710	400	1.5	3.6	0.8	20	0.5	450	TO-220
SEF711	350	1.5	3.6	0.8	20	0.5	450	TO-220
SEF712	400	1.3	5	0.8	20	0.5	450	TO-220
SEF713	350	1.3	5	0.8	20	0.5	450	TO-220
SEF720	400	3	1.8	1.5	40	1	1000	TO-220
SEF721	350	3	1.8	1.5	40	1	1000	TO-220
SEF722	400	2.5	2.5	1.5	40	1	1000	TO-220
SEF723	350	2.5	2.5	1.5	40	1	1000	TO-220
SEF730	400	5.5	1	3	75	3	1000	TO-220

SHORTFORM CATALOGUE (Sorted by part number)

Device	$V_{(BR)DSS}$ V	I_D (MAX) A	$R_{DS(on)}$ max (Ω) @	I_D (A)	P_{tot} (W)	g_{fs} min (℧)	C_{ISS} max (pF)	Package
SEF731	350	5.5	1	3	75	3	1000	TO-220
SEF732	400	4.5	1.5	3	75	3	1000	TO-220
SEF733	350	4.5	1.5	3	75	3	1000	TO-220
SEF820	500	2.5	3	1	40	1	1000	TO-220
SEF821	450	2.5	3	1	40	1	1000	TO-220
SEF822	500	2	4	1	40	1	1000	TO-220
SEF823	450	2	4	1	40	1	1000	TO-220
SEF830	450	4.5	1.5	2.5	75	2.5	1200	TO-220
SEF831	450	4.5	1.5	2.5	75	2.5	1200	TO-220
SEF832	500	4	2	2.5	75	2.5	1200	TO-220
SEF833	450	4	2	2.5	75	2.5	1200	TO-220
SEFF120	100	6	0.3	3	20	1.5	480	TO-39
SEFF121	60	6	0.3	3	20	1.5	480	TO-39
SEFF122	100	5	0.4	3	20	1.5	480	TO-39
SEFF123	60	5	0.4	3	20	1.5	480	TO-39
SEFH6N55	550	6	1.5	3	150	2	1900	SOT-93*
SEFH7N45	450	7	0.8	3.5	150	2	2100	SOT-93*
SEFH7N50	500	7	0.8	3.5	150	2	1900	SOT-93*
SEFH8N35	350	8	0.8	4	150	3	2100	SOT-93*
SEFH8N40	400	8	0.55	4	150	3	2100	SOT-93*
SEFH15N18	180	15	0.16	7.5	150	4	2500	SOT-93*
SEFH15N20	200	15	0.16	7.5	150	4	2500	SOT-93*
SEFH25N08	80	25	0.075	12.5	150	5	2200	SOT-93*
SEFH25N10	100	25	0.075	12.5	150	5	2200	SOT-93*
SEFH35N05	50	35	0.055	17.5	150	8	2500	SOT-93*
SEFH35N06	60	35	0.055	17.5	150	8	2500	SOT-93*
SEFM2N45	450	4	4	1	75	1	500	TO-3
SEFM3N35	350	3	3.3	1.5	75	0.75	450	TO-3
SEFM3N40	400	3	3.3	1.5	75	0.75	450	TO-3
SEFM3N55	550	2.5	2.5	1.5	75	1.5	1600	TO-3
SEFM4N45	450	4	1.5	2	75	1.5	1000	TO-3
SEFM4N50	50	4	1.5	2	75	1.5	1200	TO-3
SEFM5N18	180	5	1	2.5	75	1.5	500	TO-3
SEFM5N20	200	5	1	2.5	75	1.5	500	TO-3
SEFM5N35	350	5	1	2.5	75	2	1000	TO-3
SEFM5N40	400	5	1	2.5	75	2	1000	TO-3
SEFM6N55	550	6	1.5	3	150	2	1900	TO-3
SEFM7N45	450	7	0.8	3.5	150	2	2100	TO-3
SEFM7N50	500	7	0.8	3.5	150	2	1900	TO-3
SEFM8N18	180	8	0.4	4	75	3	1200	TO-3
SEFM8N20	200	8	0.4	4	75	3	1200	TO-3
SEFM8N35	350	8	0.8	4	150	3	2100	TO-3
SEFM8N40	400	8	0.55	4	150	3	2100	TO-3
SEFM10N05	50	10	0.28	5	75	2.5	550	TO-3
SEFM10N06	60	10	0.28	5	75	2.5	550	TO-3
SEFM10N08	80	10	0.33	5	75	2.5	480	TO-3
SEFM10N10	100	10	0.33	3.5	75	2	480	TO-3
SEFM12N05	50	12	0.2	6	75	3	550	TO-3
SEFM12N06	60	12	0.2	6	75	3	550	TO-3
SEFM12N08	80	12	0.25	6	75	3	1200	TO-3
SEFM12N10	100	12	0.25	6	75	3	1200	TO-3
SEFM15N05	50	15	0.16	7.5	75	3.5	550	TO-3
SEFM15N06	60	15	0.16	7.5	75	3.5	550	TO-3
SEFM15N18	180	15	0.16	7.5	150	4	2500	TO-3
SEFM15N20	200	15	0.16	7.5	150	4	2500	TO-3
SEFM25N05	50	25	0.08	12.5	100	5	1400	TO-3
SEFM25N06	60	25	0.08	12.5	100	5	1400	TO-3
SEFM25N08	80	25	0.075	12.5	150	5	2200	TO-3
SEFM25N10	100	25	0.075	12.5	150	5	2200	TO-3
SEFM35N05	50	35	0.055	17.5	150	8	2500	TO-3

(*) JEDEC number: TO-218

SHORTFORM CATALOGUE (Sorted by part number)

Device	$V_{(BR)DSS}$ V	I_D (MAX) A	$R_{DS(on)}$ max (Ω) @	I_D (A)	P_{tot} (W)	g_{fs} min (℧)	C_{ISS} max (pF)	Package
SEFM35N06	60	35	0.055	17.5	150	8	2500	TO-3
SEFP2N45	450	2	4	1	75	1	500	TO-220
SEFP3N35	350	3	3.3	1.5	75	0.75	450	TO-220
SEFP3N40	400	3	3.3	1.5	75	0.75	450	TO-220
SEFP3N55	550	3	2.5	1.5	75	1.5	1200	TO-220
SEFP4N45	450	4	1.5	2	75	1.5	1000	TO-220
SEFP4N50	500	4	1.5	2	75	1.5	1200	TO-220
SEFP5N05	50	5	0.6	2.5	50	0.75	270	TO-220
SEFP5N06	60	5	0.6	2.5	50	0.75	270	TO-220
SEFP5N18	180	5	1	2.5	75	1.5	500	TO-220
SEFP5N20	200	5	1	2.5	75	1.5	500	TO-220
SEFP5N35	350	5	2	2.5	75	2	1000	TO-220
SEFP5N40	400	5	1	2.5	75	2	1000	TO-220
SEFP8N18	180	8	0.4	4	75	3	1200	TO-220
SEFP8N20	200	8	0.4	4	75	3	1200	TO-220
SEFP10N05	50	10	0.28	5	75	2.5	550	TO-220
SEFP10N06	60	10	0.28	5	75	2.5	550	TO-220
SEFP10N08	80	10	0.33	5	75	2.5	480	TO-220
SEFP10N10	100	10	0.33	5	75	2.5	480	TO-220
SEFP12N05	50	12	0.2	6	75	3	550	TO-220
SEFP12N06	60	12	0.2	6	75	3	550	TO-220
SEFP12N08	80	12	0.25	6	75	3	1200	TO-220
SEFP12N10	100	12	0.25	6	75	3	1200	TO-220
SEFP15N05	50	15	0.16	7.5	75	3.5	550	TO-220
SEFP15N06	60	15	0.16	7.5	75	3.5	550	TO-220
SEFP25N05	50	25	0.08	12.5	100	5	1400	TO-220
SEFP25N06	60	25	0.08	12.5	100	5	1400	TO-220

INDUSTRY TYPE VS. SGS POWER MOS CROSS REFERENCE AND SGS DESIGN IN TYPE

Industry Type	SGS Equivalent	SGS Design in	Industry Type	SGS Equivalent	SGS Design in
BUZ10	BUZ10	SGSP322	IRF221	SEF221	SGSP517
BUZ10A	BUZ10A	SGSP322	IRF222	SEF222	SGSP517
BUZ11		SGSP492	IRF223	SEF223	SGSP517
BUZ11A	SGSP382	SGSP482	IRF230	SEF230	SGSP567
BUZ14	SGSP591	SGSP491	IRF231	SEF231	SGSP567
BUZ15	SGSP591	SGSP491	IRF232	SEF232	SGSP567
BUZ17		SGSP482	IRF233	SEF233	SGSP567
BUZ18		SGSP492	IRF240	SEF240	SGSP577
BUZ20	SGSP361	SGSP461	IRF241	SEF241	SGSP577
BUZ21	SGSP361	SGSP461	IRF242	SEF242	SGSP577
BUZ23		SGSP361	IRF243	SEF243	SGSP577
BUZ24	SGSP571	SGSP471	IRF320	SEF320	SGSP565
BUZ25	SGSP561	SGSP461	IRF321	SEF321	SGSP566
BUZ27		SGSP471	IRF322	SEF322	SGSP565
BUZ28		SGSP471	IRF323	SEF323	SGSP566
BUZ31		SGSP477	IRF330	SEF330	SGSP565
BUZ32	SGSP367	SGSP467	IRF331	SEF331	SGSP566
BUZ33	SGSP517	SGSP317	IRF332	SEF332	SGSP565
BUZ34	SGSP577	SGSP477	IRF333	SEF333	SGSP566
BUZ35	SGSP567	SGSP467	IRF340	SEF340	SGSP575
BUZ36		SGSP477	IRF341	SEF341	SGSP576
BUZ37		SGSP477	IRF342	SEF342	SGSP575
BUZ38		SGSP477	IRF343	SEF343	SGSP576
BUZ41A	SGSP369	SGSP469	IRF352	SGSP575	SGSP475
BUZ42	SGSP569	SGSP469	IRF353	SGSP576	SGSP476
BUZ44A		SGSP369	IRF420	SEF420	SGSP569
BUZ45		SGSP479	IRF421	SEF421	SGSP569
BUZ45A	SGSP579	SGSP479	IRF422	SEF422	SGSP569
BUZ46	SGSP569	SGSP369	IRF423	SEF423	SGSP569
BUZ48		SGSP479	IRF430	SEF430	SGSP569
BUZ48A		SGSP479	IRF431	SEF431	SGSP569
BUZ60	SGSP365	SGSP465	IRF432	SEF432	SGSP569
BUZ60B	SGSP365	SGSP465	IRF433	SEF433	SGSP569
BUZ63		SGSP365	IRF440	SEF440	SGSP579
BUZ63B		SGSP365	IRF441	SEF441	SGSP579
BUZ64		SGSP575	IRF442	SEF442	SGSP579
BUZ67		SGSP475	IRF443	SEF443	SGSP579
BUZ71	BUZ71	SGSP322	IRF451	SGSP574	SGSP474
BUZ71A	BUZ71A	SGSP322	IRF453	SGSP574	SGSP474
BUZ72A	BUZ72A	SGSP311	IRF510	SEF510	SGSP351
BUZ73A	SGSP367	SGSP467	IRF511	SEF511	SGSP352
BUZ74	SGSP369	SGSP469	IRF512	SEF512	SGSP351
BUZ74A	SGSP319	SGSP219	IRF513	SEF513	SGSP352
BUZ76	BUZ76	SGSP365	IRF520	SEF520	SGSP311
BUZ76A	BUZ76A	SGSP365	IRF521	SEF521	SGSP312
IRF120	SEF120	SGSP511	IRF522	SEF522	SGSP311
IRF121	SEF121	SGSP512	IRF523	SEF523	SGSP312
IRF122	SEF122	SGSP511	IRF530	SEF530	SGSP361
IRF123	SEF123	SGSP512	IRF531	SEF531	SGSP562
IRF130	SEF130	SGSP561	IRF532	SEF532	SGSP361
IRF131	SEF131	SGSP562	IRF533	SEF533	SGSP562
IRF132	SEF132	SGSP561	IRF541	SEF541	SGSP381
IRF133	SEF133	SGSP562	IRF542	SEF542	SGSP361
IRF140	SEF140	SGSP571	IRF543	SEF543	SGSP362
IRF141	SEF141	SGSP581	IRF610	SGSP317	SGSP217
IRF142	SEF142	SGSP571	IRF611	SGSP317	SGSP217
IRF143	SEF143	SGSP581	IRF612	SGSP317	SGSP217
IRF150	SEF150	SGSP571	IRF613	SGSP317	SGSP217
IRF151	SEF151	SGSP572	IRF620	SEF620	SGSP317
IRF152	SEF152	SGSP571	IRF621	SEF621	SGSP317
IRF153	SEF153	SGSP572	IRF622	SEF622	SGSP317
IRF220	SEF220	SGSP517	IRF623	SEF623	SGSP317

INDUSTRY TYPE VS. SGS POWER MOS CROSS REFERENCE AND SGS DESIGN IN TYPE

Industry Type	SGS Equivalent	SGS Design in	Industry Type	SGS Equivalent	SGS Design in
IRF630	SEF630	SGSP367	MTH20N12	SGSP477	SGSP461
IRF631	SEF631	SGSP367	MTH20N15	SGSP477	SGSP471
IRF632	SEF632	SGSP367	MTH25N08	SEFH25N08	SGSP472
IRF633	SEF633	SGSP367	MTH25N10	SEFH25N10	SGSP471
IRF640		SGSP477	MTH35N05	SEFH35N05	SGSP492
IRF641		SGSP477	MTH35N06	SEFH35N06	SGSP491
IRF642		SGSP477	MTM2N45	SEFM2N45	SGSP519
IRF643		SGSP477	MTM2N50	SGSP519	SGSP319
IRF710	SEF710	SGSP331	MTM3N35	SEFM3N35	SGSP332
IRF711	SEF711	SGSP332	MTM3N40	SEFM3N40	SGSP331
IRF712	SEF712	SGSP331	MTM4N45	SEFM4N45	SGSP464
IRF713	SEF713	SGSP332	MTM4N50	SEFM4N50	SGSP469
IRF720	SEF720	SGSP365	MTM5N18	SEFM5N18	SGSP517
IRF721	SEF721	SGSP366	MTM5N20	SEFM5N20	SGSP517
IRF722	SEF722	SGSP365	MTM5N35	SEFM5N35	SGSP466
IRF723	SEF723	SGSP366	MTM5N40	SEFM5N40	SGSP465
IRF730	SEF730	SGSP365	MTM6N55	SEFM6N55	SGSP578
IRF731	SEF731	SGSP366	MTM7N12	SGSP517	SGSP217
IRF732	SEF732	SGSP365	MTM7N15	SGSP517	SGSP217
IRF733	SEF733	SGSP366	MTM7N18	SGSP517	SGSP317
IRF740		SGSP475	MTM7N20	SGSP517	SGSP317
IRF741		SGSP475	MTM7N45	SEFM7N45	SGSP474
IRF742	SGSP365	SGSP475	MTM7N50	SEFM7N50	SGSP479
IRF743	SGSP365	SGSP475	MTM8N08	SGSP512	SGSP312
IRF820	SEF820	SGSP369	MTM8N10	SGSP511	SGSP311
IRF821	SEF821	SGSP369	MTM8N12	SGSP567	SGSP517
IRF822	SEF822	SGSP369	MTM8N15	SGSP567	SGSP367
IRF823	SEF823	SGSP369	MTM8N18	SEFM8N18	SGSP567
IRF830	SEF830	SGSP469	MTM8N20	SEFM8N20	SGSP567
IRF831	SEF831	SGSP364	MTM8N35	SEFM8N35	SGSP576
IRF832	SEF832	SGSP369	MTM8N40	SEFM8N40	SGSP575
IRF833	SEF833	SGSP369	MTM10N05	SEFM10N05	SGSP422
IRF840		SGSP479	MTM10N06	SEFM10N06	SGSP521
IRF841		SGSP474	MTM10N08	SEFM10N08	SGSP312
IRF842	SGSP369	SGSP479	MTM10N10	SEFM10N10	SGSP511
IRF843	SGSP364	SGSP474	MTM10N12	SGSP567	SGSP467
IRFF110	SGSP151	SGSP251	MTM10N15	SGSP567	SGSP467
IRFF111	SGSP152	SGSP252	MTM10N25	SGSP563	SGSP463
IRFF112	SGSP151	SGSP252	MTM12N05	MTM12N05	SGSP522
IRFF113	SGSP152	SGSP252	MTM12N06	SEFM12N06	SGSP521
IRFF120	SEFF120	SGSP111	MTM12N08	SEFM12N08	SGSP562
IRFF121	SEFF121	SGSP112	MTM12N10	SEFM12N10	SGSP561
IRFF122	SEFF122	SGSP111	MTM12N18	SGSP567	SGSP467
IRFF123	SEFF123	SGSP112	MTM12N20	SGSP567	SGSP467
IRFF130		SGSP361	MTM15N05	SEFM15N05	SGSP522
IRFF131	SGSP121	SGSP221	MTM15N06	SEFM15N06	SGSP521
IRFF132	SGSP111	SGSP361	MTM15N12		SGSP567
IRFF133	SGSP157	SGSP121	MTM15N15		SGSP567
MTA4N18		SGSP216	MTM15N18	SEFM15N18	SGSP477
MTA4N20	SGSP216		MTM15N20	SEFM15N20	SGSP477
MTA5N12		SGSP217	MTM15N35	SGSP576	SGSP476
MTA5N15		SGSP217	MTM15N40	SGSP575	SGSP475
MTA6N08	SGSP212		MTM15N45	SGSP574	SGSP474
MTA6N10	SGSP211		MTM15N50	SGSP579	SGSP479
MTA7N06	SGSP257		MTM20N08	SGSP572	SGSP472
MTH6N55	SEFH6N55	SGSP478	MTM20N10	SGSP571	SGSP471
MTH7N45	SEFH7N45	SGSP474	MTM20N12	SGSP577	SGSP561
MTH7N50	SEFH7N50	SGSP479	MTM20N15	SGSP577	SGSP561
MTH8N35	SEFH8N35	SGSP476	MTM25N05	SEFM25N05	SGSP482
MTH8N40	SEFH8N40	SGSP475	MTM25N06	SEFM25N06	SGSP481
MTH15N18	SEFH15N18	SGSP477	MTM25N08	SEFM25N08	SGSP472
MTH15N20	SEFH15N20	SGSP477	MTM25N10	SEFM25N10	SGSP471

INDUSTRY TYPE VS. SGS POWER MOS CROSS REFERENCE AND SGS DESIGN IN TYPE

Industry Type	SGS Equivalent	SGS Design in	Industry Type	SGS Equivalent	SGS Design in
MTM35N05	SEFM35N05	SGSP492	RFL1N12	SGSP117	SGSP151
MTM35N06	SEFM35N06	SGSP491	RFL1N15	SGSP117	SGSP151
MTP1N45	SGSP354	SGSP254	RFL1N18	SGSP117	SGSP217
MTP1N50	SGSP339	SGSP239	RFL1N20	SGSP117	SGSP217
MTP1N55	SGSP338	SGSP238	RFL2N05	SGSP158	SGSP258
MTP2N35	SGSP356	SGSP256	RFL2N06	SGSP157	SGSP257
MTP2N40	SGSP355	SGSP255	RFM3N45	SGSP530	
MTP2N45	SEFP2N45	SGSP230	RFM3N50	SGSP519	
MTP2N50	SGSP319	SGSP219	RFM4N35	SGSP532	
MTP3N35	SEFP3N35	SGSP232	RFM4N40	SGSP531	
MTP3N40	SEFP3N40	SGSP231	RFM6N45	SGSP564	
MTP3N55	SEFP3N55	SGSP468	RFM6N50	SGSP569	
MTP4N08	SGSP352	SGSP252	RFM7N35	SGSP566	
MTP4N10	SGSP351	SGSP251	RFM7N40	SGSP565	
MTP4N45	SEFP4N45	SGSP464	RFM8N18	SGSP567	SGSP367
MTP4N50	SEFP4N50	SGSP569	RFM8N20	SGSP567	SGSP467
MTP5N05	SEFP5N05	SGSP352	RFM10N12	SGSP567	
MTP5N06	SEFP5N06	SGSP352	RFM10N15	SGSP567	
MTP5N18	SEFP5N18	SGSP317	RFM12N08	SGSP562	SGSP462
MTP5N20	SEFP5N20	SGSP317	RFM12N10	SGSP561	SGSP461
MTP5N35	SEFP5N35	SGSP466	RFM12N18	SGSP577	
MTP5N40	SEFP5N40	SGSP465	RFM12N20	SGSP577	
MTP7N12	SGSP317	SGSP217	RFM15N05	SGSP522	SGSP322
MTP7N15	SGSP317	SGSP217	RFM15N06	SGSP521	SGSP321
MTP7N18	SGSP317	SGSP217	RFM15N12	SGSP577	
MTP7N20	SGSP317	SGSP217	RFM15N15	SGSP577	
MTP8N08	SGSP312	SGSP212	RFM18N08	SGSP562	SGSP362
MTP8N10	SGSP311	SGSP211	RFM18N10	SGSP561	SGSP361
MTP8N12		SGSP367	RFM25N05	SGSP582	SGSP382
MTP8N15		SGSP367	RFM25N06	SGSP581	SGSP381
MTP8N18	SEFP8N18	SGSP367	RFM35N08	SGSP572	SGSP472
MTP8N20	SEFP8N20	SGSP367	RFM35N10	SGSP571	SGSP471
MTP10N05	SEFP10N05	SGSP322	RFP1N35	SGSP356	SGSP256
MTP10N06	SEFP10N06	SGSP321	RFP1N40	SGSP355	SGSP255
MTP10N08	SEFP10N08	SGSP212	RFP2N08	SGSP302	SGSP202
MTP10N10	SEFP10N10	SGSP211	RFP2N10	SGSP301	SGSP201
MTP10N12	SGSP367	SGSP467	RFP2N18	SGSP317	SGSP217
MTP10N15	SGSP367	SGSP467	RFP2N20	SGSP317	SGSP217
MTP10N25	SGSP363	SGSP463	RFP3N45	SGSP330	SGSP230
MTP12N05	SEFP12N05	SGSP222	RFP3N50	SGSP319	SGSP219
MTP12N06	SEFP12N06	SGSP222	RFP4N05	SGSP358	SGSP258
MTP12N08	SEFP12N08	SGSP362	RFP4N06	SGSP357	SGSP257
MTP12N10	SEFP12N10	SGSP361	RFP4N35	SGSP366	SGSP466
MTP12N18	SGSP367	SGSP467	RFP4N40	SGSP365	SGSP465
MTP12N20	SGSP367	SGSP467	RFP6N45	SGSP364	SGSP464
MTP15N05	SEFP15N05	SGSP322	RFP6N50	SGSP369	SGSP469
MTP15N06	SEFP15N06	SGSP321	RFP7N35	SGSP366	SGSP466
MTP15N12	SGSP367	SGSP467	RFP7N40	SGSP365	SGSP465
MTP15N15	SGSP367	SGSP467	RFP8N18	SGSP367	SGSP467
MTP20N08		SGSP472	RFP8N20	SGSP367	SGSP467
MTP20N10		SGSP471	RFP10N12	SGSP367	SGSP311
MTP25N05	SEFP25N05	SGSP482	RFP10N15	SGSP367	SGSP311
MTP25N06	SEFP25N06	SGSP482	RFP12N08	SGSP362	SGSP462
RFK10N45	SGSP574		RFP12N10	SGSP361	SGSP461
RFK10N50	SGSP579		RFP15N05	SGSP322	SGSP222
RFK12N35	SGSP576		RFP15N06	SGSP321	SGSP221
RFK12N40	SGSP575		RFP18N08	SGSP362	SGSP462
RFK25N18	SGSP577		RFP18N10	SGSP361	SGSP461
RFK25N20	SGSP577		RFP25N05	SGSP382	SGSP482
RFL1N08	SGSP102	SGSP202	RFP25N06	SGSP381	SGSP481
RFL1N10	SGSP101	SGSP201			

ALPHABETICAL LIST OF SYMBOLS

Symbol	Meaning
C_{DB}	Parasitic capacitance between drain and body
C_{DS}	Parasitic capacitance between drain and source
C_{GD}	Parasitic capacitance between gate and drain
C_{GS}	Parasitic capacitance between gate and source
C_{iss}	Input capacitance
C_{oss}	Output capacitance
C_{rss}	Reverse transfer capacitance
D.U.T.	Device under test
I_D	Drain current
I_{DLM}	Drain peak current, inductive
I_{DM}	Drain peak current
I_{DSS}	Zero gate voltage drain current
I_G	Gate current
I_{GSS}	Gate-body leakage with drain short circuited to source
I_{SD}	Source-drain diode current
I_{SDM}	Source-drain diode peak current
L	Load inductance of a specified circuit
P_W	Pulse width
P_{tot}	Total power dissipation
$R_{DS\,(on)}$	Static drain-source on resistance
R_i	Generator internal resistance
R_L	Load resistance of a specified circuit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient
$R_{th\ j\text{-}case}$	Thermal resistance junction-case
T_l	Maximum lead temperature for soldering purpose
T_{amb}	Ambient temperature
T_{case}	Case temperature
T_j	Junction temperature
T_{stg}	Storage temperature
$V_{(BR)\,DSS}$	Drain-source breakdown voltage
V_{DG}	Drain-gate voltage
V_{DGR}	Drain-gate voltage with specified resistance between gate and source
V_{DS}	Drain-source voltage
$V_{DS\,(on)}$	Drain-source on state voltage

ALPHABETICAL LIST OF SYMBOLS

V_{GS}	Gate-source-voltage
$V_{GS\,(th)}$	Gate threshold voltage
V_{SD}	Source-drain diode forward on voltage
V_{clamp}	Drain clamping voltage
V_i	Input voltage of a specified circuit
f	Frequency
g_{fs}	Forward transconductance
$t_{d\,(off)}$	Turn-off delay time
$t_{d\,(on)}$	Turn-on delay time
t_f	Fall time
t_{on}	Turn-on time
t_r	Rise time
t_{rr}	Reverse recovery time

RATING SYSTEMS FOR ELECTRONIC DEVICES

A. DEFINITIONS OF TERMS USED

a. **Electronic device.** An electronic tube or valve, transistor or other semiconductor device.
Note: This definition excludes inductors, capacitors, resistors and similar components.

b. **Characteristic.** A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

c. **Bogey electronic device.** An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

d. **Rating.** A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determinated for specified values of environment and operation, and may be stated in any suitable terms.
Note: Limiting conditions may be either maxima or minima.

e. **Rating system.** The set of principles upon which ratings are established and which determines their interpretation.
Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

B. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.
These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.
The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

RATING SYSTEMS FOR ELECTRONIC DEVICES

C. DESIGN - MAXIMUM RATING SYSTEM

Design-maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.
These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.
The equipment manufacturer should design so that, initially and throughout life, no design-maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply-voltage variation, equipment, component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

D. DESIGN - CENTRE RATING SYSTEM

Design-centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.
These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.
The equipment manufacturer should design so that, initially, no design-centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply-voltage.

The Absolute Maximum Rating System is commonly used for semiconductor devices.

HANDLING OF POWER PLASTIC TRANSISTORS

PRECAUTIONS FOR PHYSICAL HANDLING OF POWER PLASTIC TRANSISTOR [TO-220, SOT-93, TO-126 (SOT-32), SOT-82]

When mounting power transistors certain precautions must be taken in operations such as bending of leads, mounting of heatsink, soldering and removal of flux residue. If these operations are not carried out correctly, the device can be damaged or reliability compromised.

1. **Bending and cutting leads**
   The bending or cutting of the leads requires the following precautions:

1.1. When bending the leads they must be clamped tightly between the package and the bending point to avoid strain on the package (in particular in the area where the leads enter the resin) (fig. 1). This also applies to cutting the leads (fig. 2).

1.2. The leads must be bent at a minimum distance of 3 mm from the package (fig. 3a).

1.3. The leads should not be bent at an angle of more than 90° and they must be bent only once (fig. 3b).

1.4. The leads must never be bent laterally (fig. 3c).

1.5. Check that the tool used to cut or form the leads does not damage them or ruin their surface finish.

Fig. 1 - Bending the leads

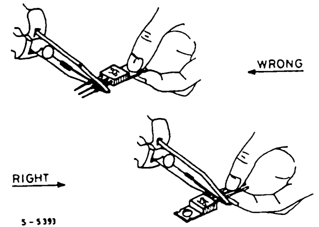


Fig. 2 - Lead forming or cutting mechanism

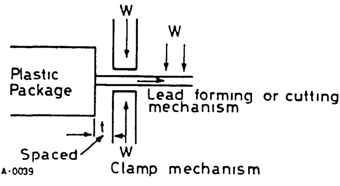
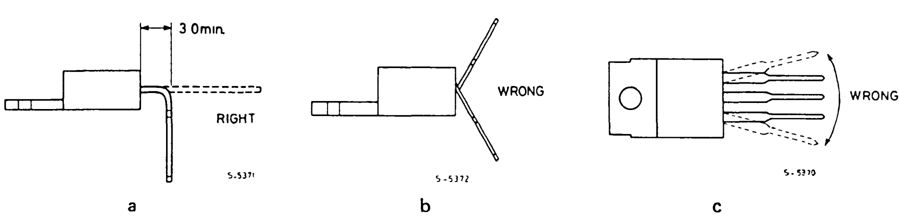


Fig. 3 - Angles for lead wire bending



HANDLING OF POWER PLASTIC TRANSISTORS

2. Mounting on printed circuit
During mounting operations be careful not to apply stress to the power transistor.

2.1. Adhere strictly to the pin spacing of the transistor to avoid forcing the leads.

2.2. Leave a suitable space between printed circuit and transistor, if necessary use a spacer.

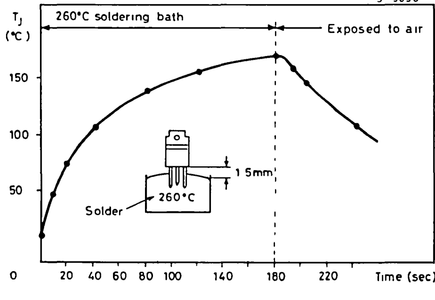
2.3. When fixing the device to the printed circuit do not put mechanical stress on the transistor. For this purpose the device should be soldered to the printed circuit board after the Transistor has been fixed to the heatsink and the heatsink to the printed circuit board.

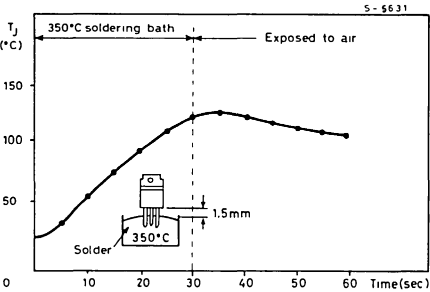
3. Soldering
In general a transistor should never be exposed to high temperature for any length of time. It is therefore preferable to use soldering methods where the transistor is exposed to the lowest possible temperatures for a short time.

3.1. Tolerable conditions are 260°C for 10 sec or 350°C for 3 sec. The graphs in fig. 4 give an idea of the excess junction temperature during the soldering process for a TO-220 (Versawatt). It is also important to use suitable fixes for the tin baths to avoid deterioration of the leads or of the package resin.

3.2. An excess of residual flux between the pins of the transistor or in contact with the resin can reduce the long-term reliability of the device. The solvent for removing excess flux must be chosen with care. The use of solvents derived from trichloroethylene is not recommended on plastic packages because the residue can cause corrosion.

Fig. 4 – Junction temperatures during soldering



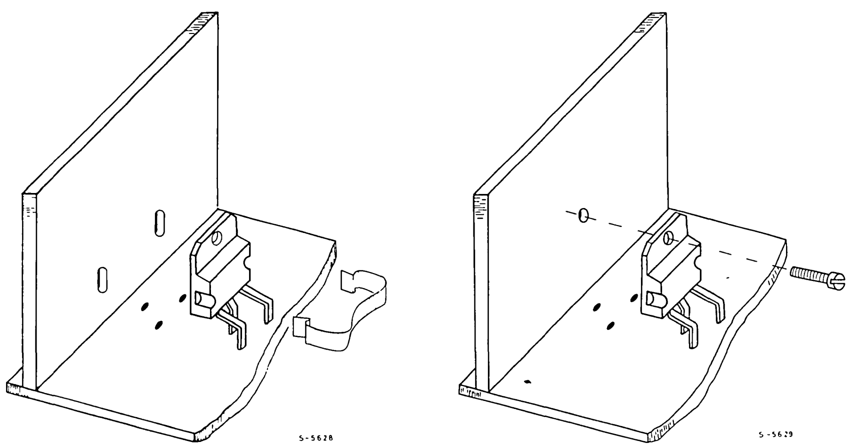


HANDLING OF POWER PLASTIC TRANSISTORS

4. **Mounting at heatsink**
   To exploit best the performance of power transistors a heatsink with R_{th} suitable for the power that the transistor will dissipate must be used.

4.1. The plastic packages used by SGS for its power transistors (SOT-32, SOT-82, SOT-93, Versawatt) provide for the use of a single screw to fix the package to the heatsink. A compression spring (clip) can be sufficient as an alternative (fig. 5).

Fig. 5 - SOT-93 mounting examples

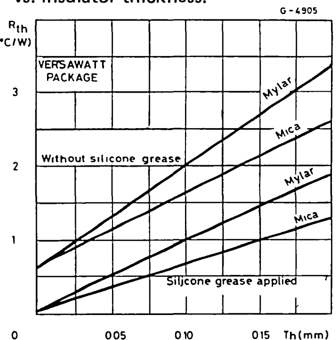


The screw should be properly tightened to ensure good contact between the back of the package and the heatsink but should not be too tight to avoid deformation of the copper part (tab) of the package causing breaking of the die or separation of the resin from the tab.

4.2. The contact R_{th} between device and heatsink can be improved by inserting a thin layer of silicone grease with fluidity sufficient to guarantee perfectly uniform distribution on the surface of the tab. The thermal resistance with and without silicone grease is given in fig. 6. An excessively thick layer or an excessive viscosity of the grease can degrade the R_{th}.

5. **Heatsink problems**
   The most important aspect from the point of view of reliability of a power transistor is that the heatsink should be dimensioned to keep the T_j of the device as low as possible. From the mechanical point of view, however, the heatsink must be realized so that it does not damage the device.

Fig. 6 - Contact thermal resistance vs. insulator thickness.



HANDLING OF POWER PLASTIC TRANSISTORS

5.1. The planarity of the contact surface between device and heatsink must be $< 25\ \mu m$ for TO-220, SOT-93, TO-126 (SOT-32), SOT-82.

5.2. If self threading screws are used there must be an outlet for the material that is deformed during formation of the thread. The diameter ϕ 1 (fig. 7) must be large enough to avoid distortion of the tab during tightening. For this purpose it may be useful to insert a washer or use screws of the type shown in fig. 8 where the pressure on the tab is distributed on a much larger surface. Sometimes when the hole in the heatsink is formed with a punch, around the hole or hollow there may be a ring which is lower than the heatsink surface. This is dangerous because it may lead to distortion of the tab as mentioned before.

Fig. 7 - Device mounting

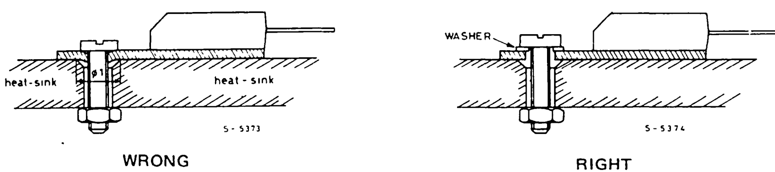
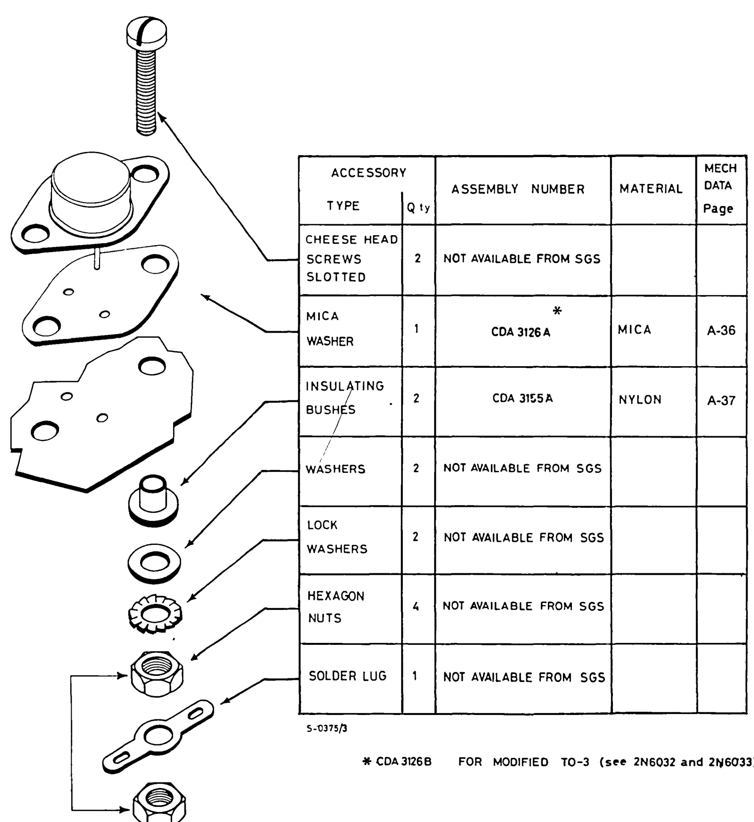


Fig. 8 - Suggested screw

5.3. A very serious problem is that of the rigidity between heatsink, device and printed circuit board. Once the device and the heatsink are mechanically connected, and the heatsink is fixed to the apparatus frame, the device and the PCB are bound together by the leads of the devices. A solution of this type is extremely dangerous.

ACCESSORIES AND MOUNTING INSTRUCTIONS

TO-3



ACCESSORY TYPE	Q ty	ASSEMBLY NUMBER	MATERIAL	MECH DATA Page
CHEESE HEAD SCREWS SLOTTED	2	NOT AVAILABLE FROM SGS		
MICA WASHER	1	* CDA 3126 A	MICA	A-36
INSULATING BUSHES	2	CDA 3155 A	NYLON	A-37
WASHERS	2	NOT AVAILABLE FROM SGS		
LOCK WASHERS	2	NOT AVAILABLE FROM SGS		
HEXAGON NUTS	4	NOT AVAILABLE FROM SGS		
SOLDER LUG	1	NOT AVAILABLE FROM SGS		

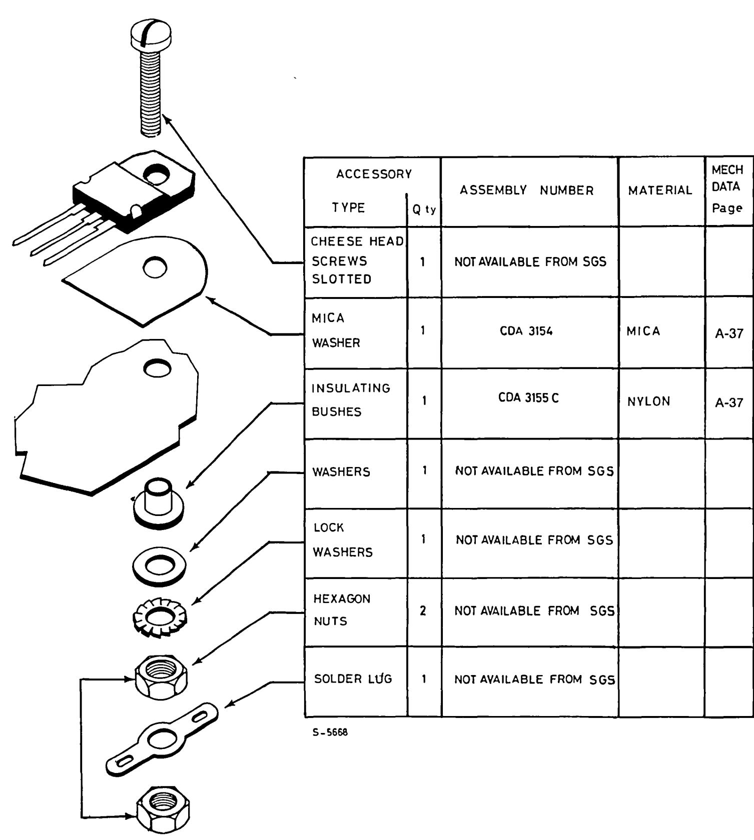
S-0375/3

* CDA 3126B FOR MODIFIED TO-3 (see 2N6032 and 2N6033)

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 1 Nm.

ACCESSORIES AND MOUNTING INSTRUCTIONS

SOT-93

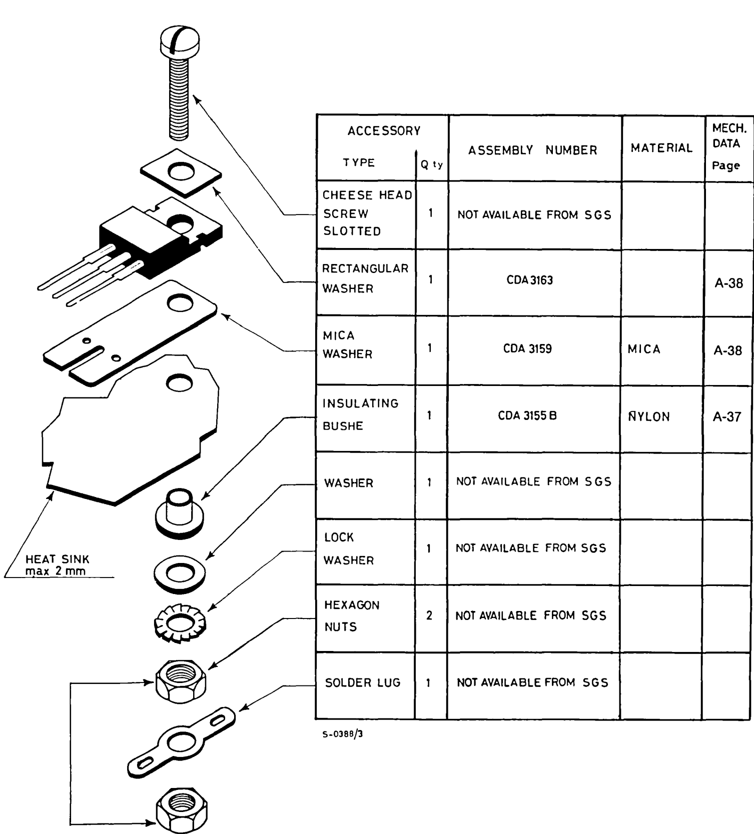


ACCESSORY TYPE	Q ty	ASSEMBLY NUMBER	MATERIAL	MECH DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS		
MICA WASHER	1	CDA 3154	MICA	A-37
INSULATING BUSHES	1	CDA 3155 C	NYLON	A-37
WASHERS	1	NOT AVAILABLE FROM SGS		
LOCK WASHERS	1	NOT AVAILABLE FROM SGS		
HEXAGON NUTS	2	NOT AVAILABLE FROM SGS		
SOLDER LUG	1	NOT AVAILABLE FROM SGS		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 1 Nm.

ACCESSORIES AND MOUNTING INSTRUCTIONS

TO-220

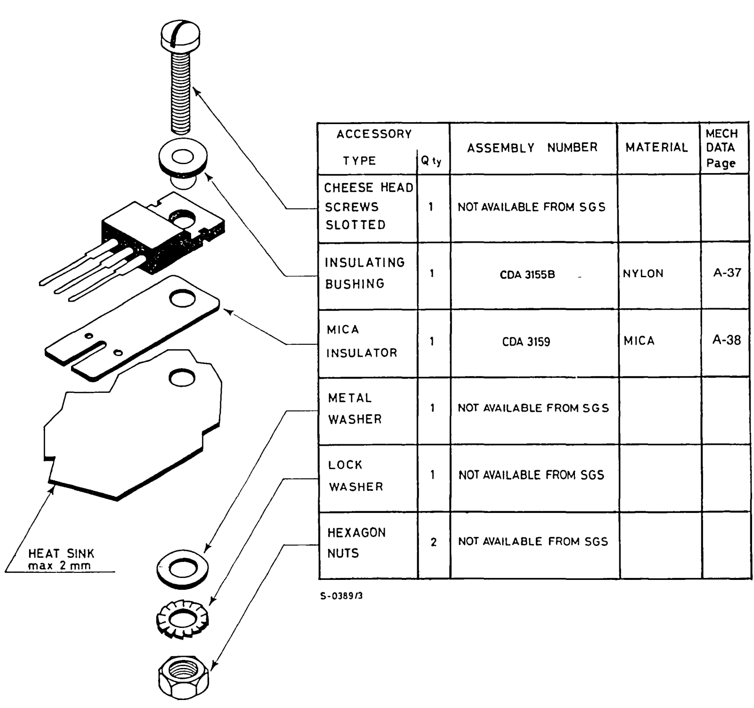


ACCESSORY TYPE	Q ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREW SLOTTED	1	NOT AVAILABLE FROM SGS		
RECTANGULAR WASHER	1	CDA 3163		A-38
MICA WASHER	1	CDA 3159	MICA	A-38
INSULATING BUSHE	1	CDA 3155 B	NYLON	A-37
WASHER	1	NOT AVAILABLE FROM SGS		
LOCK WASHER	1	NOT AVAILABLE FROM SGS		
HEXAGON NUTS	2	NOT AVAILABLE FROM SGS		
SOLDER LUG	1	NOT AVAILABLE FROM SGS		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 0.7 Nm.

ACCESSORIES AND MOUNTING INSTRUCTIONS

TO-220

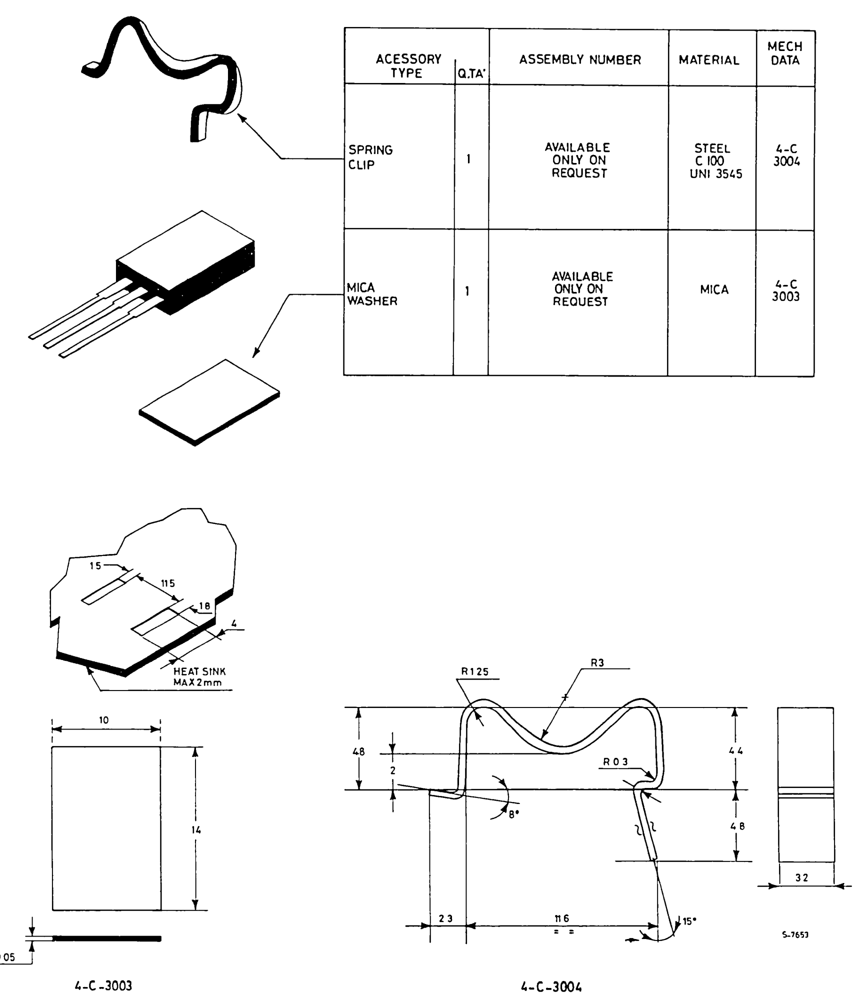


ACCESSORY TYPE	Q ty	ASSEMBLY NUMBER	MATERIAL	MECH DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS		
INSULATING BUSHING	1	CDA 3155B	NYLON	A-37
MICA INSULATOR	1	CDA 3159	MICA	A-38
METAL WASHER	1	NOT AVAILABLE FROM SGS		
LOCK WASHER	1	NOT AVAILABLE FROM SGS		
HEXAGON NUTS	2	NOT AVAILABLE FROM SGS		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 0.7 Nm.

ACCESSORIES AND MOUNTING INSTRUCTIONS

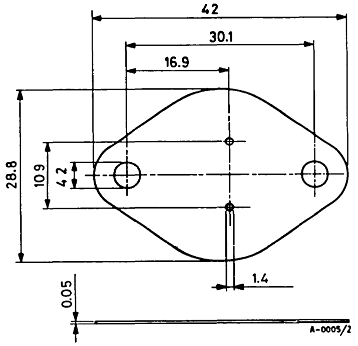
SOT-82 and TO-126



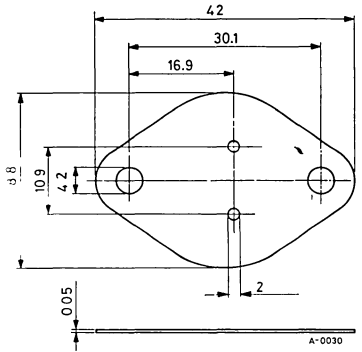
ACESSORY TYPE	Q.TA'	ASSEMBLY NUMBER	MATERIAL	MECH DATA
SPRING CLIP	1	AVAILABLE ONLY ON REQUEST	STEEL C 100 UNI 3545	4-C 3004
MICA WASHER	1	AVAILABLE ONLY ON REQUEST	MICA	4-C 3003

ACCESSORIES AND MOUNTING INSTRUCTIONS

CDA 3126A

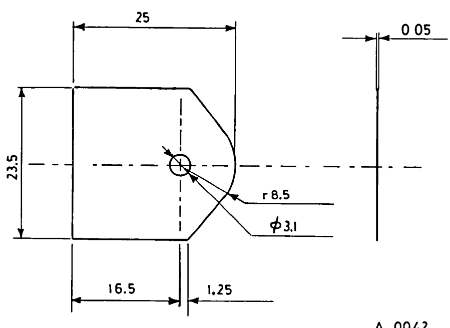


CDA 3126B

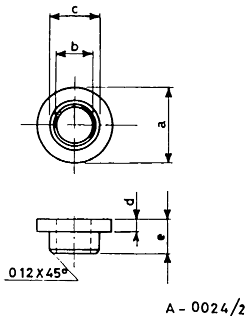


ACCESSORIES AND MOUNTING INSTRUCTIONS

CDA 3154



CDA 3155

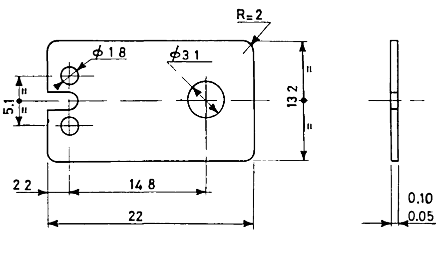


Suffix	Package	a	b	c	d	e
A	TO-3	6.40 to 6.60	3.00 to 3.10	4.00 to 4.05	1.1 max	1.55 to 1.65
B	TO-220	5.30 to 5.50	3.00 to 3.10	3.83 to 3.88	0.60 to 0.65	1.70 to 1.80
C	SOT-93	6.40 to 6.60	3.00 to 3.10	4,00 to 4,05	1.3 to 1.4	2.7 to 2.9

Material: Nylon; Dimensions: mm.

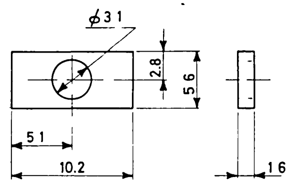
ACCESSORIES AND MOUNTING INSTRUCTIONS

CDA 3159



TYPE	MATERIAL	NOTE
CDA 3159	MICA	

CDA 3163

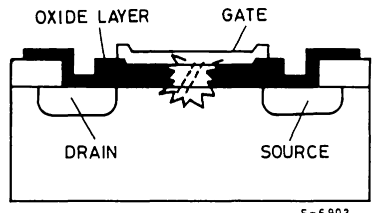


TYPE	MATERIAL	NOTE
CDA 3163	Steel nickel plated	

ELECTROSTATIC DISCHARGE PROTECTION

Electronic components have to be protected from the hazard of static electricity, from the manufacturing stage down to where they are utilized. MOS devices are typically voltage and field sensitive; the thin oxide layers can be destroyed by the electric field.

Fig. 1 -



This happens mostly because a charged conductor, typically a person, is rapidly discharged through the device.

There will be no net charge on any portion of the MOS structure; when the induced high field exceeds the breakdown voltage of the MOS capacitor structure we may have a self-healing breakdown, degradation or catastrophic failure.

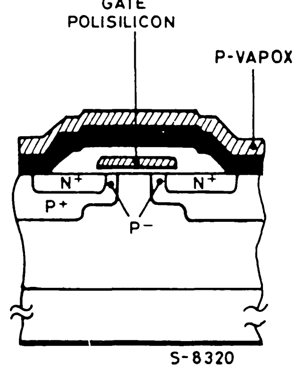
The failure hazard is not limited to the gate region but it could occur wherever two conductive areas are separated by a thin insulator.

SGS POWER MOS devices can generally be considered less ESD sensitive than MOS I/Cs.

The input capacitances are typically 10 to 200 times larger, and the gate oxide thickness is similar in size to that of the largest MOS I/Cs used.

As a result, it is common practice not to consider the ESD as dangerous for SGS POWER MOS, this is not always true, even though they are less sensitive than MOS I/Cs.

Fig. 2 -



HANDLING

SGS has choosen a no-compromise strategy in the MOS ESD protection. From the wafer level to the shipping of finished units, we fully guarantee each work station and processing of the parts. This is achieved thru total adoption of shielding and grounding media. Our final shipping is performed in antistatic tubes or bags or boxes.

The supplier best commitment is useless if the end user does not provide the same level of protection and care in application.

Here are the basic static control protection rules:

A - Handle all components in a static-safe work area.

B - Transport all components in static shielding containers.

To comply with the rules the following procedures must be set up.

1 - Static control wrist strap (from a qualified source) used and connected properly.

2 - Each table top must be protected with a conductive mat, properly grounded.

3 - Extended use of conductive floor mats.

4 - Static control shoe straps, wearing typically insulating footwear, such as with crepe or thick rubber soles.

5 - Ionized air blowers are a necessary part of the protective system, to neutralize static charges on conductive items.

6 - Use only the grounded tip variety of soldering iron.

7 - Single components, tubes, printed circuit cards should always be contained in static shielding bags; keep out parts in the original bags up to the very last point in your operation line.

8 - If bigger containers (tote box) are used for in-plant transport of devices or PC boards they must be electrically conductive, like the carbon loaded ones.

9 - All tools, persons, testing machines, which could contact device leads must be conductive and grounded.

10 - Avoid using high dielectric materials (like polystyrene) for subassembly construction, storing, trasportation.

11 - Follow a proper power supply sequence in testing and application. Supply voltage should be applied before and removed after input signals; insertion and removal from sockets should be done with no power applied.

12 - Filtration, noise suppression, slow voltage surges should be guaranteed on the supply lines.

13 - Any open (floating) input pin is a potential hazard to your circuit: ground or short them to V_{DD} whenever possible.

TECHNICAL NOTES B

AN INTRODUCTION TO POWER MOS

A POWER MOS transistor is a power transistor produced with MOS, and not the usual bipolar technology.

Special characteristics are higher switching speeds and easier driving. This introductory note describes the essential points of the MOS structure when used for power devices.

WHAT DOES MOS MEAN ?

It means that the essential part (the silicon chip) of the device is made up of three layers:

- one conductive layer (M for metal) that is the control (drive) electrode
- one isolating layer (O for oxide) that prevents any current flow from the drive electrode to the other two electrodes, but does not block the electric field
- one semiconductor layer (S for semiconductor) which switches on or off depending on the electrical field imposed on it by the control electrode through the opening in the P zone of a conductive channel between the two zones.

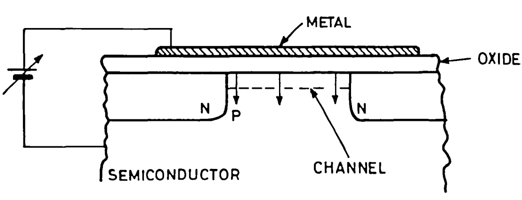
WHAT DOES POWER MOS MEAN ?

Fig. 1 shows that the device is totally implemented on the chip surface. In other words both the on and off states are implemented in a horizontal plane:

- the ON STATE i.e. the residual resistance when in the on state corresponds to conduction on the top surface of the silicon
- the OFF STATE i.e. the depletion region of one of the two PN junctions, with its resistivity and length, gives the device its voltage rating.

With the present technology the "on the surface" approach allows the production of MOS transistors

Fig. 1 - MOS basic structure



that can handle tens of volts and miliamperes (as in MOS microprocessors or in MOS memories). A power transistor must be able to handle no less than a few amperes at voltages of 50-100V or higher. The approach of several devices "on the surface" connected in parallel is unsuitable due to the problems of excessive connections, as each cell would have three terminals.

The best solution is to exploit the semiconductor both vertically as well horizontally. The paralleling of one of the two N doped regions of all the elementary structures in parallel occurs on the bottom face of the semiconductor.

At the same time, the PN junction that implements the off performance (its length corresponds to the voltage rating of the device) can be positioned vertically, and so avoiding the waste of horizontal space. The channel must be short (1 to 2 microns) to obtain characteristics of practical interest.

As a result, the POWER MOS device consists of multi - MOS basic cells, with all the N^+ type SOURCE zones connected in parallel on the top side of the semiconductor chip, as are the cell GATES. The common substrate of the chip forms the DRAIN.

THE POSSIBLE STRUCTURES

Figures 2, 3 and 4 show the chronological progression of the different solutions used in the industry to implement the elementary POWER MOS structures.

The P doped semiconductor area that appears on the surface of the semiconductor in front of the metal electrode is the channel. There is an N^-

Fig. 2 - V-Groove structure

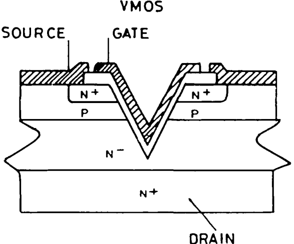


Fig. 3 - U-Groove structure

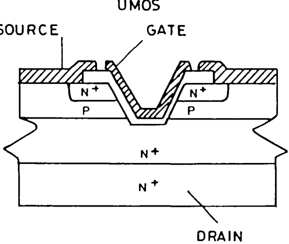


Fig. 4 - D-MOS structure

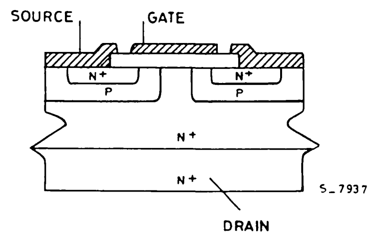
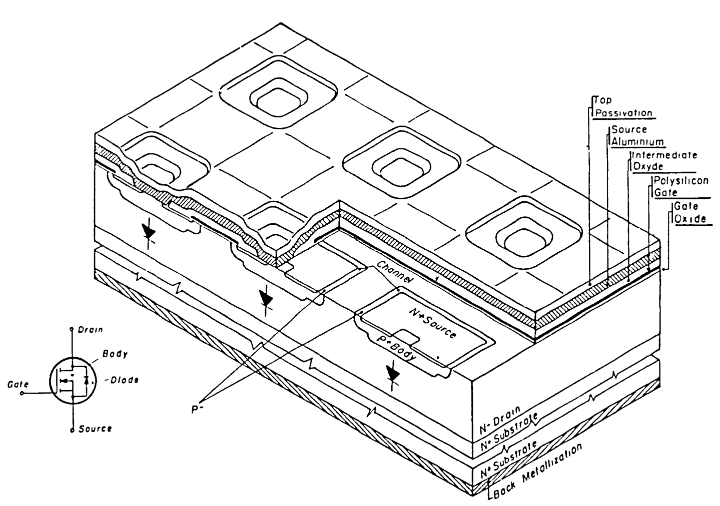


Fig. 5 - SGS POWER MOS cell structure



layer with low doping (high resistivity) on one side of the channel. This N layer becomes depleted when the voltage is applied to the device, and consequently allows the device to sustain applied voltages without reaching too high an electric field at any point of the chip.

Reaching the critical field means reaching the point of voltage breakdown (primary breakdown).

"V" and "U" type structures have been abandoned because the production process is both difficult and critical. Nowadays practically all POWER MOS are of the D type as shown in Fig. 4. D as a prefix means that the channel is produced by diffusion.

All the devices have in common the fact that the current traverses the device vertically, as a consequence two electrodes appear on the surface:

- SOURCE
- GATE

and one electrode appears on the bottom:

- DRAIN

Fig. 5 shows the actual structure of an SGS POWER MOS in an expanded view of a piece of the chip. All the important elements can be located in the figure.

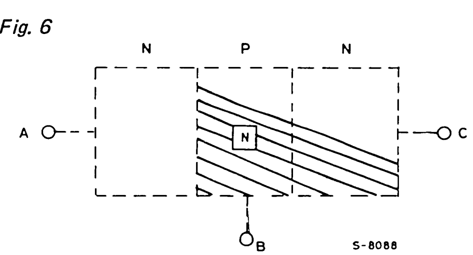
HIGH VOLTAGE POWER MOS

One of the most important questions the circuit designers ask POWER MOS manufactures is: "Why do you have very high voltage bipolar devices but not high voltage POWER MOS?".

To answer this question it is useful to remember an important phenomenon that appears in a bipolar device and not in a POWER MOS device.

Fig. 6 shows the schematic diagram of a bipolar device in the saturation region.

Fig. 6



The N collector is invaded by the N carriers coming from the base and its resistivity is modulated. The resistivity of the N collector layer is greatly reduced due to the invasion of these minority carriers.

A bipolar transistor is fully saturated when the minority carriers from the base have totally invaded the collector. For both bipolar and SGS POWER MOS devices the collector is an epitaxial silicon layer of high resistivity. Its thickness, and consequently its no-current resistance, corresponds to the voltage rating of the device.

Since a SGS POWER MOS device is a unipolar (majority carrier) by definition it is very fast in switching.

As a consequence in a POWER MOS there is no modulation of the conductivity and the drain resistivity remains at the same value as its epitaxial specification implies.

The current flows through two resistances:

1) Resistance of channel (R-channel)

2) Resistance of drain (R-drain)

So, if the two devices have:

- similar epitaxial spec, to guarantee the same breakdown voltage (BV_{CES} for BIPOLAR, $V_{(BR)DSS}$ for POWER MOS)
- same chip area, to guarantee the same current flow they will show the following output characteristics (Fig. 7).

Fig. 7a - POWER MOS SGSP361 $V_{(BR)DSS}$ = 100V

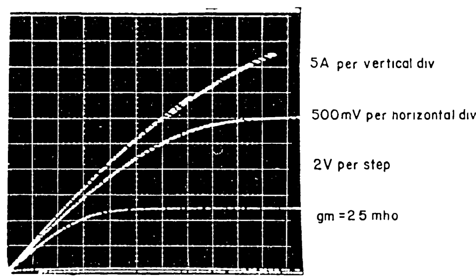
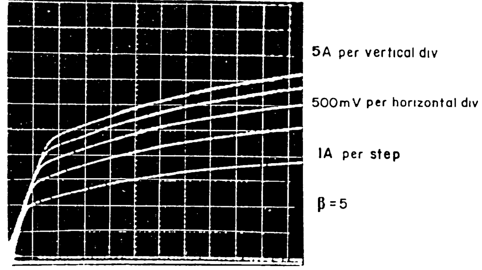
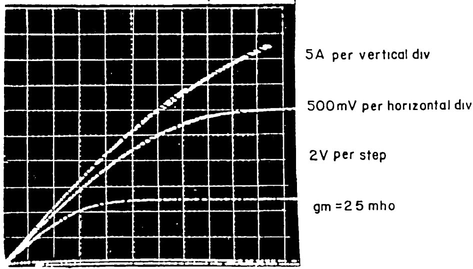


Fig. 7b - BIPOLAR 2N5039 (BV_{CEO} = 75V, BV_{CES} = 120V, same die size)



The voltage drop in SGS POWER MOS is greater than in bipolar devices. If the thickness of the epitaxial layer is increased to raise the breakdown voltage, this is partially compensated by the conductivity modulation phenomenon in the bipolar devices while in POWER MOS this cannot occur.

Fig. 8 - Shows the output characteristics for POWER MOS: SGSP361 $V_{(BR)DSS}$ = 100V SGSP367, $V_{(BR)DSS}$ = 200V, same die size.



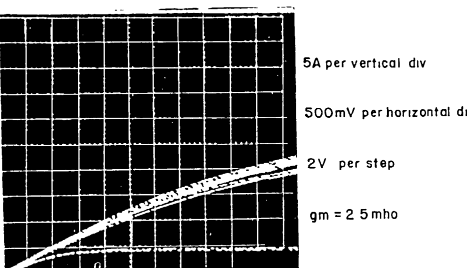
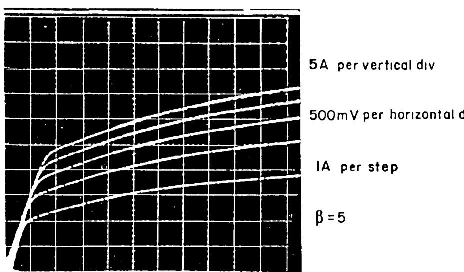
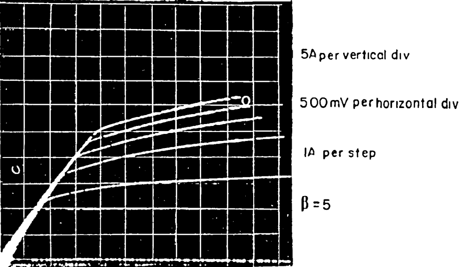


Fig. 9 - Shows the output characteristic for BIPOLAR: 2N5039 (BV_{CEO} = 75V, BV_{CES} = 120V), BUX41N (BV_{CEO} = 160V, BV_{CES} = 220V, same die size)





In an SGS POWER MOS the increase of the voltage drop - due to the increase of $R_{DS(on)}$ is much more accentuated than in a bipolar device. It is possible to describe the increase of $R_{DS(on)}$ versus the breakdown voltage using the following law:

$$R_{DS(on)}(V) = R_{DS(on)}(Vo) \times \left(\frac{V}{Vo}\right)^{k}$$

where K is a coefficient whose value depends on the voltage values at which the comparison is made:

K = 1.8 at low voltage (50-100V)

K = 2.5 at high voltage (500V)

K = 2.7 at voltages higher than 500V

To increase the SGS POWER MOS breakdown voltage from 500V to 1000V we have to compute:

$$R_{DS(on)}(1000V) = R_{DS(on)}(500V) \times$$
$$\times \left(\frac{1000V}{500V}\right)^{2.7} = 7.3 \times R_{DS(on)}(500V)$$

To compensate for the increase of $R_{DS(on)}$ it is necessary to increase the chip area at least two or three times. This leads to the following problems:

1) The chip is much more expensive. For the same chip area a SGS POWER MOS is more expensive than a bipolar, it is easy to understand that if the die size were increased the SGS POWER MOS would be even more expensive.
2) The above solution could only be used for small chips, because if big chips were further enlarged they would be too big to produce and assemble.
3) The device would be difficult to drive. In fact the greater the chip area the greater the input capacitance of the device. To charge and discharge this capacitance, it is necessary to supply high current peaks at the gate.

So in the range of high voltage applications bipolar devices will continue to be used in the future, while SGS POWER MOS will be used much more frequently in low to medium voltages and very fast switching applications where the benefits of lower switching losses compensate the higher device cost.

THE WHY AND WHERE OF POWER MOS

The POWER MOS technology is yet another addition to the several technologies already well established in the power transistor family. To understand why this technology has certain advantages over the existing ones some comparison must be made about performance and cost - the two basic points that fundamentally determine the choice of a component:

PERFORMANCE

POWER MOS technology differs primarily in two ways from that of the power bipolar:

— MOS conduction control

— Unipolar conduction

MOS INPUT

The MOS structure implies that the drive terminal is electrically insulated from the rest of the device. Parasitic capacitances are the only load that the POWER MOS represents for the driving circuit. The lack of a drive current of any significant value is certainly a major advantage. To understand the extent of this advantage a practical case where the power supply is the same for the load and for the driving circuit can be considered. A typical case using automotive electronics is considered for 100V, 5A rated devices:

Table 1

PARAMETER	TRANSISTOR	DARLINGTON	POWER MOS
Rated voltage	100V	100V	100V
Operating current	5A	5A	5A
Saturated gain	10	100	—
Drive power required in Fig. 1	0.5A x 12V = 6W	50mA x 12V = 600mW	0mW
Losses on the device at 5A in Fig. 1	3.5W (V_{BE} = 0.7V)	7.5W (V_{BE} = 0.7V)	6W (V_{GS} = 1.2V)

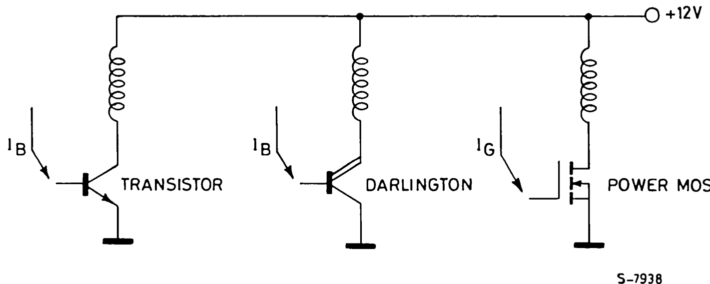
Table 1: relative performances (comparison based on same silicon chip area)

It is clearly evident how in some cases, a simple drive configuration can compensate for higher losses on the device itself, not to mention the driving circuit simplification.

In practice POWER MOS are driven by a voltage source, giving 0V or + 10V drive, which may even have a relatively high (KΩ) internal resistance.

Drive power is needed (apart from leakages in the nA range) to charge and discharge input parasitic capacitances during the switching transition.

Fig. 1 – Circuit under examination



UNIPOLAR CONDUCTION

Inside the silicon chip of a POWER MOS device, only majority carriers are used for conduction. This has two major consequences:

1) When in the charging state, there is no need to wait for minority carriers to disappear or to fully invade a certain silicon area.

POWER MOS devices are, by at least one order of magnitude, faster than their bipolar conterparts, because they do not make use of minority carriers for conduction.

Phenomena like the storage time (the minority carriers must evacuate the base area) or the dynamic V_{CEsat} (the minority carriers must invade and settle in the collector area) are completely absent in POWER MOS devices.

2) As there is no "h_{FE}" to be increased with a rise in temperature ("h_{FE}" is a description of the minority carrier behaviour) there is not possibility of a direct secondary breakdown (FBSOA limitation) neither of a reverse (RBSOA limitation).

A POWER MOS transistor is able to safely absorb power pulses, and this ability is not reduced by "power focusing" anywhere in the die. There is no secondary breakdown in POWER MOS.

Another important consequency of unipolar conduction, is the absence of "conductivity modulation". In a bipolar device, the carriers can, (in the fully saturated state) invade the collector region, and significantly reduce its resistivity.

The drain region is thick and more resistive to sustain the voltage in the off-state. When the device is turned on, this region is responsible for the on-state voltage drop ($V_{DS(on)}$).

The higher voltage a device is built for the more the resistance of the drain region contributes to the total on-state resistance. As a rough indication, it can be said that:

– for devices rated 60V or less, the drain resistivity is not the prime factor responsible for its on-state characteristics.

– for devices rated 200V or more, drain resistivity is the major cause of its on-state characteristics.

As a result, conductivity modulation makes bipolar devices more efficient (smaller chips and lower costs) than POWER MOS in the high voltage area.

The higher the voltage the more pronounced are the effects of the lack of conductivity modulation.

POWER MOS of similar current capability, versus power bipolars of the same voltage capability:

– require similar silicon area in the chip in the 60-100V range

– require 2 to 5 times more silicon area in the chip in the 200-500V range

– are hardly competitive at 800V and above

COST

POWER MOS technology is more sophisticated than that of standard power bipolar devices for example: finer geometries, more processing steps etc.

As a result a silicon chip of the same area has a higher cost due to the:

– higher equipment costs

– longer process time (more operations)

– lower production yields

A comparison based on cost per unit area of silicon is the simplest to make but a comparison between the performances is much more accurate as it reveals the advantages in a specific application.

POWER MOS VERSUS BIPOLAR

1) The high voltage range -800V or more.

POWER MOS is hardly competitive. The chip would have to be enormous in size for any significant current. For high voltages the technology must be that of a conductivity modulation device. In addition the typical applications (motor controls, high power convertors) imply physical dimensions which are not compatible with very high switching speeds, the parasitic elements such as inductances and capacitances make high frequencies impossible.

2) The medium voltage range -200 -600V

POWER MOS and power bipolar are fairly competitive. POWER MOS allows lower switching losses traded off with higher d.c. losses. A reduced cost of the driving circuit tends to compensate the high cost of the device itself. The higher the switching speed and the lower the maximum voltage, the more competitive POWER MOS becomes.

3) The low voltage range -60 -100V

In low voltage POWER MOS, conductivity modulation is not a problem. There is no significant difference between the drive supply voltage and the voltage applied to the drain. But unlike bipolar devices the drive power required by POWER MOS transistors is very small (the power gain is very high) and there is negligible power loss. Hence POWER MOS are certainly going to find their stronghold in this range.

EVOLUTION OF SGS POWER MOS TRANSISTORS

The vertical double diffused MOS silicon gate technology represents the final evolution of the development of a process to obtain SGS POWER MOS devices, started in SGS in 1977.

The principal steps of this development have passed through the study of these structures (fig. 1);

1) V groove MOS
2) U groove MOS
3) Double diffused MOS metal gate
4) Double diffused MOS silicon gate

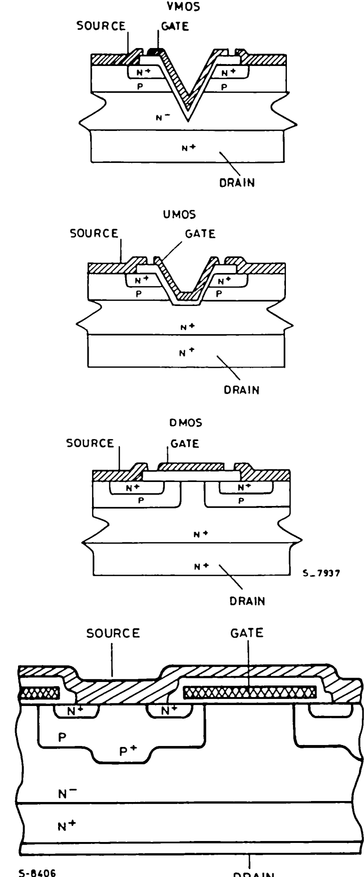
Nowadays the VDMOS silicon gate structure is used while the other three structures have become obsolete.

All these structures have as a common point the fact that the current flows through a vertical path like bipolar power devices and, as a consequence the devices have two electrodes on the top (gate and source) and one on the bottom (drain) in electrical and thermal contact with the header.

Another common point is the fact that the starting material is made of an epitaxial lightly N^- doped layer grown on a heavily N^+ doped substrate (for N-channel devices).

The N^- region largely supports the applied drain potential because its doping level is much smaller than the P^- body region.

Fig. 1 - Evolution of POWER MOS devices



VDMOS SILICON GATE

STRUCTURE

In the VDMOS silicon gate structure the best features of earlier technologies and design are combined with new fabrication techniques to achieve much better performance. The VDMOS silicon gate structure needs a more sophisticated technology, very similar to that of the VLSI.

VDMOS (fig. 2) is a two level structure where the lower level is the gate made of doped polycrystalline silicon and the upper level is the source metallization.

It is a self aligned structure since the polysilicon holes are the mask for the P^- well and N^+ source diffusion.

In this way the MOS channel regions are obtained by difference in lateral diffusion of the two impurity distributions. The use of double diffusion achieves very short channels ($\leqslant 1.5\mu$).

With the VDMOS silicon gate structure the resulting increase in packing density directly reduces the cost and improves the performance of the device. In fact the use of a polycrystalline gate reduces the possibility of sodium ion contamination in the gate oxide (with high stability of threshold voltage $V_{GS(th)}$). Also the full surface source metallization allows a better heat dissipation.

Fig. 2a - VDMOS structure

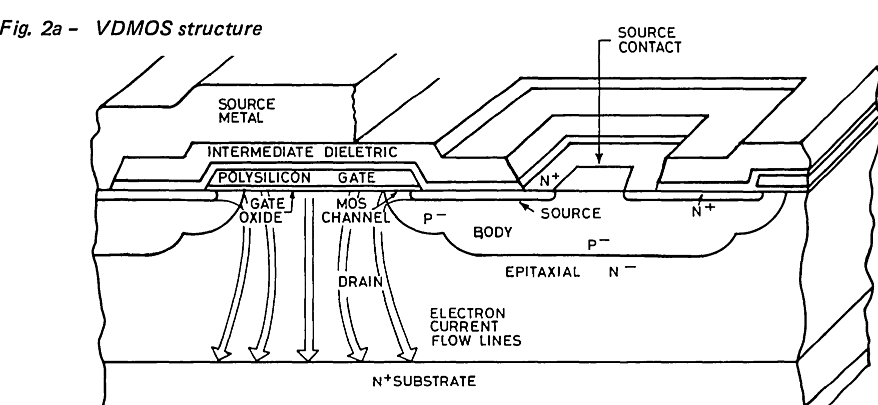
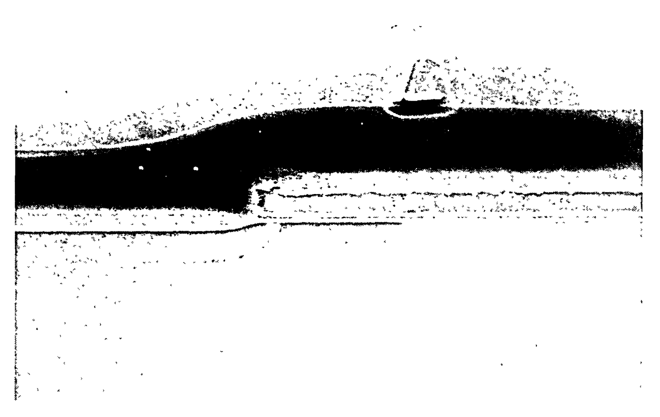


Fig. 2b - SEM microphoto of the VDMOS structure



L (channel)	≅	1.75μ
t (gate ex)	≅	830 Å
t (gate poly)	≅	3330 Å
t (ox → poly-As)	≅	2500 Å
t (p-vapox)	≅	9580 Å
x_j (source	≅	0.50μ
xj (body)	≅	2.58μ

HOW IT WORKS

The structure is switched on by applying a voltage between the drain and the source and positively biasing the gate (for a N-channel device) with respect to the source. This biasing creates an electric field in the channel region which reverses the polarity of the material in the body region to create a majority carrier path from the source to the drain. Electron current flows from the source metal to the source contact, laterally through the channel and then vertically through the drain and substrate to the drain metal.

The body source together with the drain creates an internal parasitic diode in inverse parallel connection. This diode conducts when the source is positive with respect to the drain and it can handle forward current equal to the drain current rating (fig. 3).

Fig. 3 – Schematic representation of POWER MOS structure

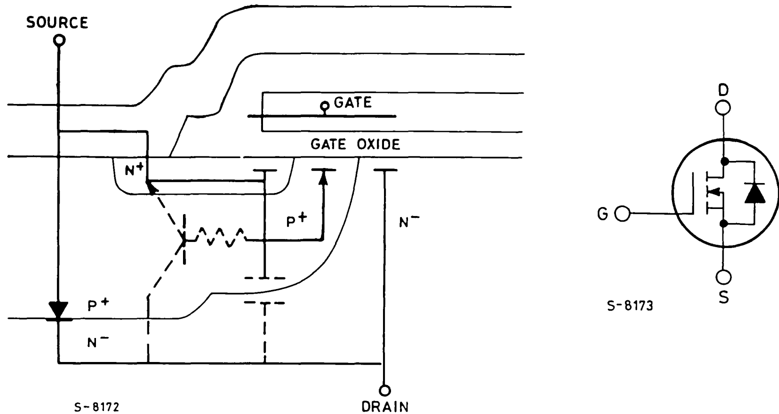
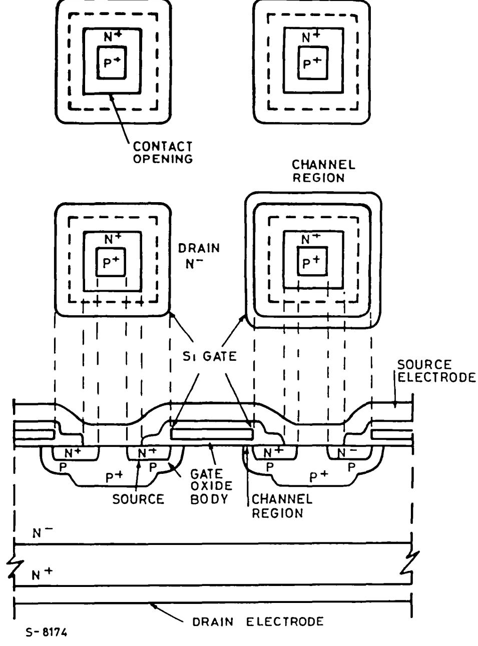


Fig. 4 – Horizontal layour and vertical structure



DESIGN OF SGS POWER MOS

In the design of a SGS POWER MOS transistor the parameters of interest are the device on resistance $R_{DS(on)}$, for a given chip area and the breakdown voltage.

ON RESISTANCE

The vertical power DMOS consists of a large number of cells interconnected in a parallel on a single die (fig. 4).

$R_{DS(on)}$ parameter is strictly dependent on the topological layout, that is the shape and size of the cells and the packing density.

In order to optimize this parameter, a comparison between different geometrical solutions at both low and high voltages was made.

If the behaviour of the $R_{DS(on)}$ components is analysed (fig. 5) it can be seen that for low voltage applications the channel has a greater effect in determining the $R_{DS(on)}$ value. To optimize the $R_{DS(on)}$. It is necessary to maximize the SGS POWER MOS channel perimeter per unit area with a high packing density.

Low voltage devices have a packing density of about 560,000 cells per square inch.

For high voltage devices the epitaxial layer resistance has a greater effect than the overall on resistance (fig. 6). To optimize $R_{DS(on)}$ it is necessary to minimize bulk resistance choosing a low packing density layout which increases the area of the epitaxial drift region.

High voltage devices have a packing density of about 280,000 cells per square inch (fig. 7).

Fig. 5 – Low voltage case

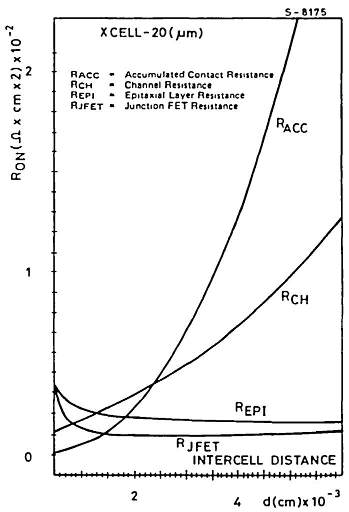


Fig. 6 – High voltage case

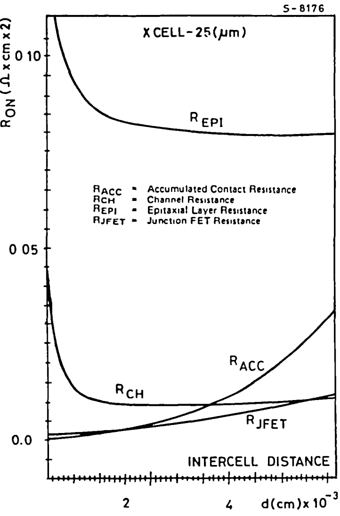
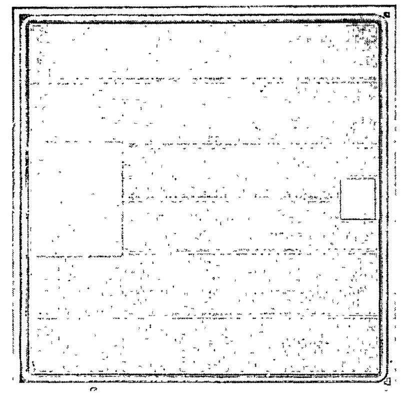
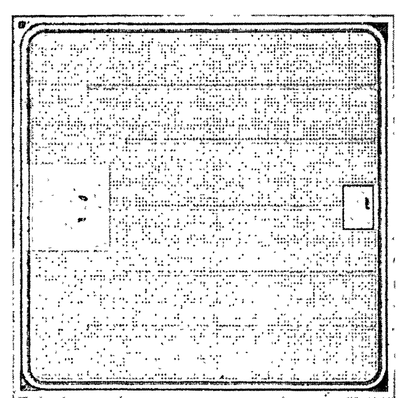


Fig. 7 – a) (100V) -- b) (400V)



a)



b)

BREAKDOWN VOLTAGE $V_{(BR)DSS}$

The ideal breakdown voltage is bulk avalanche breakdown which corresponnds to a minimum epitaxial bulk resistance requirement.

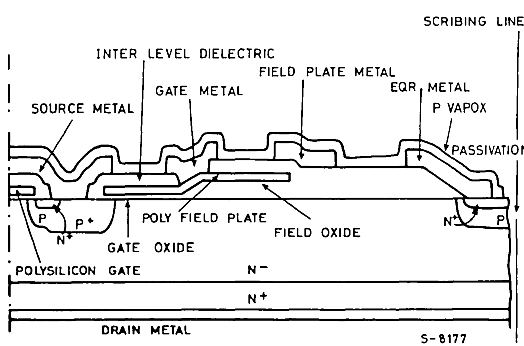
At high voltages however, the maximum drain potential is limited by junction edge breakdown below the ideal value. This is due to the effects of curvature and surface electrical field crowding.

Therefore to fulfil a certain breakdown requirement the epitaxial layer doping must exceed that specified by the minimum epitaxial bulk resistance requirement and this will increase the device on resistance.

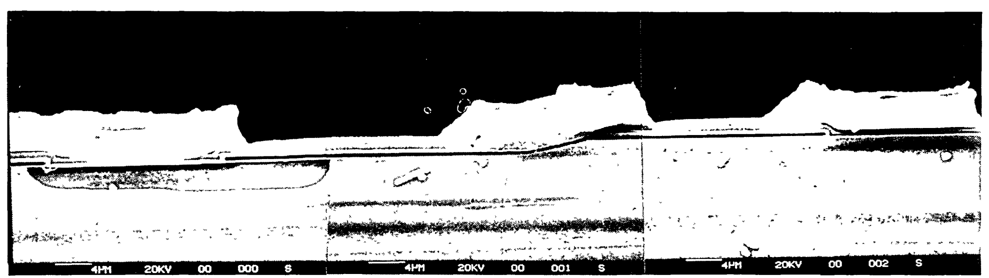
To reduce the surface electrical field and thus reach the bulk breakdown voltage, an edge structure has been developed.

This edge termination contains a field plate surrounding the silicon dioxide of three increasing thicknesses forming a triplanar structure (fig. 8).

Fig. 8 - POWER MOS Edge Structure



A SEM microphoto of the POWER MOS Edge Termination



The field plate allows higher breakdown voltages by spreading the field laterally along the surface of the device.

Gradual increase of the oxide thickness at a very low angle (10 degrees to 15 degrees) from the gate oxide to the field oxide allows distribution of the voltage so that the electrical field is as uniform as possible along the surface and is below the critical electrical field (fig. 9).

This edge termination has been implemented in SGS POWER MOS allowing breakdown voltages up to 550V with stable characteristics.

THRESHOLD VOLTAGE

The value of the threshold voltage is related to the thickness of the gate oxide and to N_A, maximum peak impurity concentration in the laterally diffused body in the region between the source and the drain (fig. 10).

Channel punch-through can occur as the result of insufficient impurity charge in the channel, under strong reverse bias. To avoide punch through a trade off between $V_{GS(th)}$ and channel length must be made.

For a fixed gate oxide thickness a shorter channel length implies a greater N_A maximum peak and a higher $V_{GS(th)}$. However, a lower $V_{GS(th)}$ sets a lower limit to the channel length in relation to the punch through problem.

Due to the negative temperature co-efficient of $V_{GS(th)}$ its value cannot be too low. Also, if it is too high, the devices cannot be driven directly by low voltage logic circuits.

Consequently the value of $V_{GS(th)}$ is in the range from 2 to 4V with an oxide thickness of 850Å.

Fig. 9 - Computer simulation of the equipotential lines of the Edge of a high voltage POWER MOS device

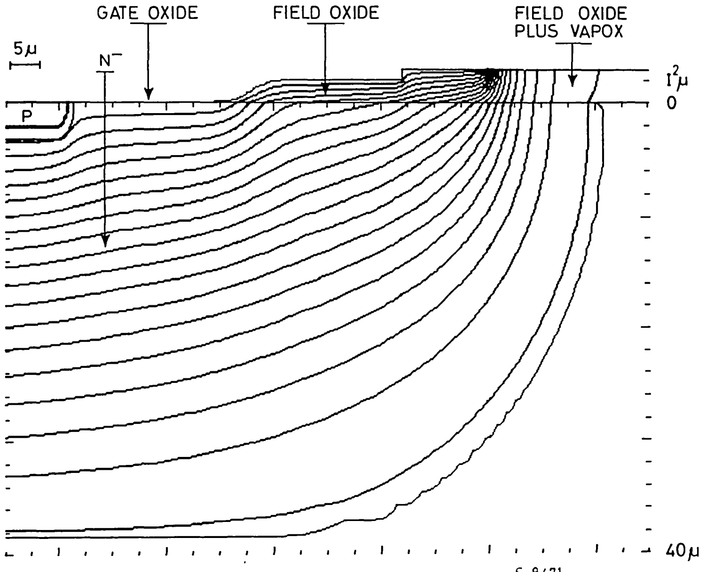
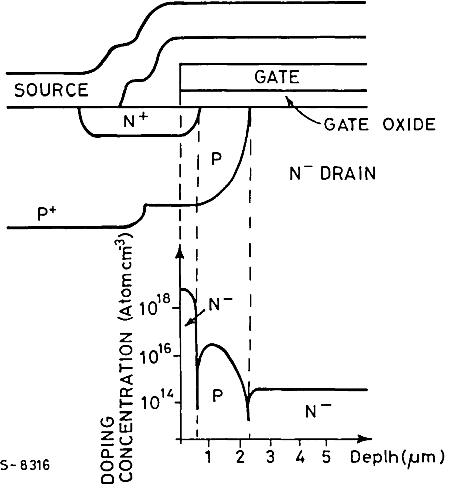


Fig. 10 -



SGS POWER MOS IN SWITCHING
AN EVALUATION METHOD AND A PRACTICAL EXAMPLE

INTRODUCTION

SGS POWER MOS are used in switch mode power supplies, H.F. welding systems, industrial ovens, relay drivers and other similar applications. These diverse applications of SGS POWER MOS in the field of control is due largely to their ability to handle high power at very high switching speeds up to hundreds of kHz.

The great improvement in the ability to switch power using SGS POWER MOS is due to the recent progress made in the manufacture and technology of semiconductors. This ability to produce power devices using MOS technology has opened up a new fields of applications. In POWER MOS devices the flow of current from the drain to the source is voltage controlled. Consequently the energy consumed in driving the device is much less than for a bipolar device. SGS POWER MOS devices are unipolar and do not make use of minority carriers for conduction. This makes them very attractive to use in power switching at very high frequencies.

SWITCHING PHASE

In pratical working conditions three main phases can be distinguished:

On state

When the device is on and the channel open, the dissipated power is:

$$P_{on} = V_{DS\,(on)} \times I_D \quad (P_{on} = V_{CEsat} \times I_C \text{ for bipolar transistors})$$

It can be reduced optimizing the technology (metal back, epitaxial thickness) and the design (cell dimensions and layout).

Off state

When the device is off and the drain is at the battery voltage, the power dissipation is:

$$P_{off} = V_{DD} \times I_{DSS} \quad (P_{off} = V_{CC} \times I_{CEX} \text{ for bipolar transistors})$$

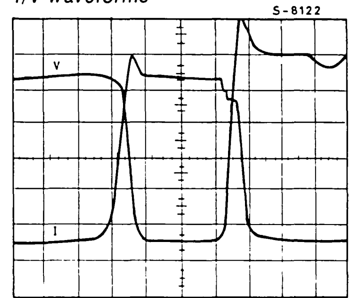
"TRANSITIONS"

During switching the dissipated power instant by instant is:

$$P = V_{DS} \times I_D$$

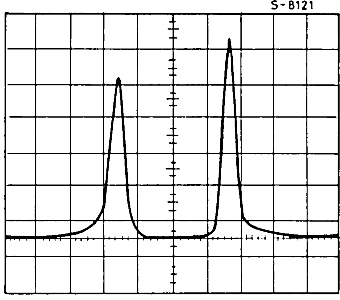
and depends on the on/of switching speed of the device as can be seen in Figs. 1 and 2.

Fig. 1 - I/V waveforms



t: 100 ns/div, V: 45V/div, I: 1.2A/div, Vg=10V, Rg=25Ω

Fig. 2 - Power dissipation waveforms.



t: 100 ns/div, P: 200 W/div, Vg=10V, Rg=25Ω.

Q. THE EFFICIENCY FACTOR

The performance of an SGS POWER MOS device can therefore be rated as the ratio between the total power in switching-on and off and the energy dissipated per cycle. It can be expressed as:

$$Q = \frac{P_t}{E_{on} + E_{off} + E_p}$$

Where:

E_{on} - is the energy lost in the turning-on and on phases

E_{off} - is the energy lost in the turning-off and off phases

E_p - is the energy lost to drive the circuit.

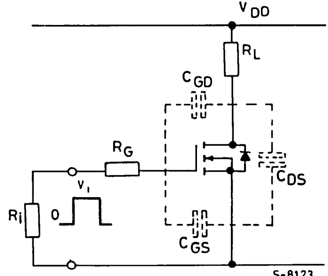
The quantity Q is a frequency and is an index of the maximum frequency at which the device can most efficiently operate, considering P_t as the maximum power that the device can dissipate in practical working conditions.

To fully understand this equation a brief analysis of switching phenomena is essential. As previously mentioned, SGS POWER MOS do not make use of minority carriers for conduction. The recombination of these minority carriers is a switching speed limitation. In SGS POWER MOS devices the majority carrier flow is simply controlled by the gate voltage and therefore its switching speed is limited only by the time needed to charge and discharge the parasitic input capacitances. Consequently the switching behaviour is a function only of the ability of the driving circuit to charge and discharge some hundreds of picofarads. This is why SGS POWER MOS can switch so fast - in the range of tens of nanoseconds.

INPUT

SGS POWER MOS devices behave quite differently from bipolar power devices, as far as the driving energy is concerned. SGS POWER MOS require driving power during the charge and the discharge phases of the input capacitances. Fig. 3 shows an SGS POWER MOS driven by a voltage generator with an internal resistance R_i and an open circuit voltage V_i, where R_L is the load.

Fig. 3 - SGS POWER MOS equivalent circuit.



The input capacitance $C_{iss} = C_{GS} + C_{GD}$ during the switching cycle is not constant for two reasons.

1) C_{GD} can be seen as the capacitance between the gate electrode and the drain, where the dielectric is the depleted drain layer. The drain epi-layer is fixed, but its depleted part varies according to V_{DS}. The higher V_{DS}, the thicker the depleted layer and consequently the lower the associated capacitance.
2) A more pronounced effect comes from the fact that the voltage across C_{GD}, when the gate source voltage rises from zero to its final value, V_{DS} must go down from V_{DD} to $V_{DS(on)}$. In particular C_{GD} is seen as a higher equivalent capacitance during the drain 'on' transitions. The input must be fed a charge:

$$Q = C_{GD} (V_{DD} - V_{DS(on)})$$

to account for the voltage variation across C_{GD}. This happens when the gate voltage reaches $V_{GS(th)}$, the threshold voltage, and the drain voltage starts falling. It is not until the required charge Q is provided that V_{GS} can increase. This is called the Miller Effect. For a while the equivalent input capacitance appears infinite and V_{GS} remains at $V_{GS(th)}$ while C_{GD} absorbs the whole input current. From the moment V_{DS} reaches $V_{DS(on)}$ the input equivalent capacitance is:

$$Ceq = C_{GS} + C_{GD} \text{ (low voltage)}$$

and the transition of the output is completed. V_{GS} increases again, tending towards V_i.

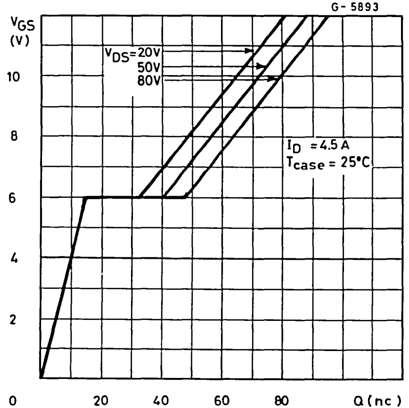
These two phenomena become apparent when looking at the gate charge versus gate source voltage diagram in the data sheets.

The diagram for SGSP471 in fig. 4 can be taken as an example.

A true capacitor would appear as a straight line starting from the origin. In fact the first segment corresponds to an equivalent capacitance:

$$C_{eq} = C_{GS} + C_{GD} \text{ (high voltage)}$$

Fig. 4 - Gate charge vs, gate-source voltage SGSP471



The horizontal segment corresponds to an equivalent infinite capacitance i.e. the charging of C_{GD} with the gate at V_{th} and the drain falling from V_{DD} to $V_{DS(on)}$. The last segment has a slope corresponding to a capacitance:

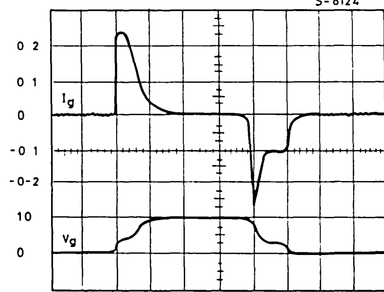
$$C_{eq} = C_{GS} + C_{GD} \text{ (low voltage)}$$

The difference in slope of the first and third segment shows how C_{GS} differs in the two cases.
The behaviour at turn off of the input capacitances is exactly opposite, where the described phenomena occur in reverse order. At this point the energy drive required to make the SGS POWER MOS switch can be calculated as:

$$E_p = 1/2C_{eq} \times V_{GS}^2 = 1/2Q_G \times V_{GS}$$

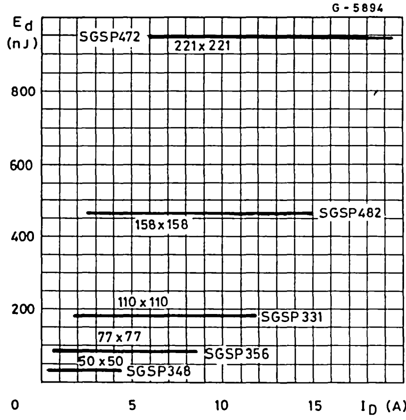
Q_G and V_{GS} can be obtained from fig. 4.
The input energy can also be obtained in a more direct manner by calculating the integral of the I_G wavefrom during the turn-on or turn-off phase, the two areas being equal (see fig. 5). In fact this integral represents the quantity Q_G (gate charge) which in turn permits the calculation of E_p.
The values of E_p have been calculated for all SGS POWER MOS in the present product range. They are a function of the die area only, for a given supply voltage V_{DD}, and have been represented for different die areas as a function of I_D in Fig. 6.

Fig. 5 - Ig - Vg waveforms



t: 0.5 μs/div, I: 0.1 A/div, V: 10 V/div

Fig. 6 - Ep vs I_D at $V_{DD} = BV_{DSS}/2$



The driving energy does not vary for devices with the same die area but different breakdown voltages, if their drive supply voltage has a constant ratio to their breakdown voltage.
In brief E_p can be plotted as a function of the die area, for a supply voltage equal to half the rated V_{DSS} of the device (see fig. 7). The method used here to calculate Q_G is different from that in the data sheet where Q_G is plotted as a function of V_{GS}.
As the results obtained in both methods were in good agreement the validity of the method used here is confirmed.
The driving circuit itself dissipates power to drive the SGS POWER MOS device. Current only flows in the gate circuit during turn-on and turn-off periods. This current flowing through the drive circuit will dissipated energy.
With reference to fig. 8, where the 50 ohm resistor is inserted to match the cable and the device, during the on phase, there is a constant power dissipation in the resistor R_1.

$$(V^2_{GS} / R_1) \cdot t/T$$

Where:

$R_1 = 50$ ohm (typical value)
$t/T =$ duty cycle

Fig. 7 - E_p versus die side (S_q·mil)

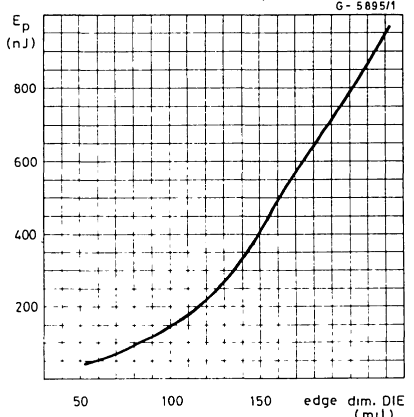


Fig. 8 - Driving circuit. A laboratory implementation

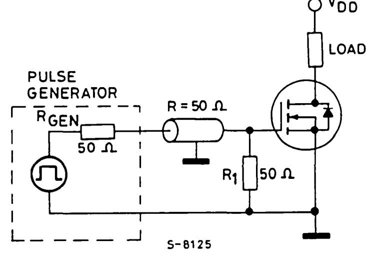


Fig. 9 - Driving circuit. A practical implementation.

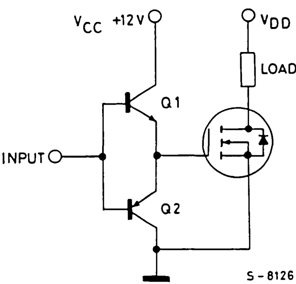


Fig. 9 shows a possible implementation that avoids steady state dissipation in the driver. The NPN transistor, Q1, only conducts at the beginning of the on phase when charging the input capacitances. Conversely the PNP transistor, Q2, only conducts at the beginning of the off phase when discharging the input capacitances. They never conduct at the same time. No conduction occurs during steady state. In addition, when either of the two transistors conduct their output impedance is very low thus improving the switching of the POWER MOS device. The total energy dissipated per cycle, in the input stage (including the SGS POWER MOS input) is:

$$E_p = Q_G \times V_{CC}$$

V_{CC} = input supply to driving stage voltage, + 12V in Fig. 7
This energy is actually dissipated in the two driving transistors, because the parasitic input capacitances of the SGS POWER MOS act as a non-dissipating element, storing energy from Q1 at turn-on, and giving it back to Q2 at turn-off.

OUTPUT

Switching times for resistive load

Fig. 10 shows the circuit used to measure the switching times of a resistive load.

Fig. 10 - Test circuit

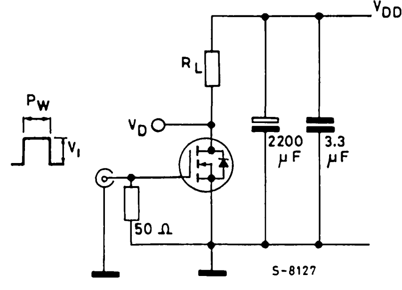
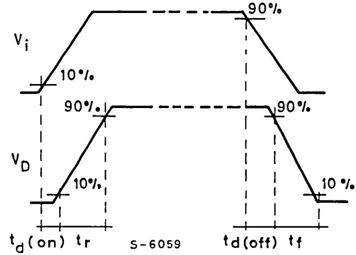


Fig. 11 - V_{GS} and V_{DS} waveforms



Turn on delay time

Turn on delay time ($t_{d(on)}$ in fig. 11) represents the time necessary for V_{GS} to reach the threshold

level V_{th} at which the device begins to conduct. The smaller the threshold voltage and the bigger the V_i value, with respect to V_{th}, the smaller the $t_{d(on)}$ value. In fact from the equation:

Eq.1 $$V_{GS} = V_i\,(1 - e^{-t/Ri.\,Ciss}).$$

where Ri. Ciss is a time constant and by substituting V_{GS} with V_{th} in Eq.1 we obtain:

Eq.2 $$t_{d(on)} = Ri.\,Ciss\,\ln\frac{V_i}{V_i - V_{th}}$$

Considering typical values for V_i and V_{th} we have:

$$t_{d(on)} = 0.35 \times Ri.\,Ciss$$

In pratice this time is negligible (10 - 20ns) when compared to others. During this time the device is off and the energy dissipated is therefore in the order of pJ and compared with the total energy loss it can be completely neglected in this analysis.

t-RISE AND t-FALL TIMES

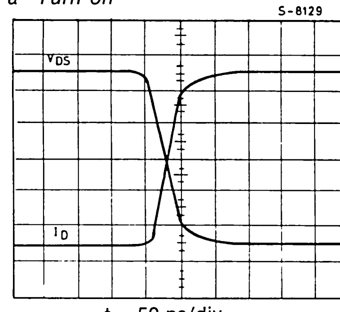
t-rise and t-fall are defined by the slopes of V_{DS} as shown in fig. 11.

Turn-off delay time

$t_{d(off)}$ can be referred to as the delay time since it represents the time necessary to remove the excess charge from the gate and channel, due to the input overvoltage.

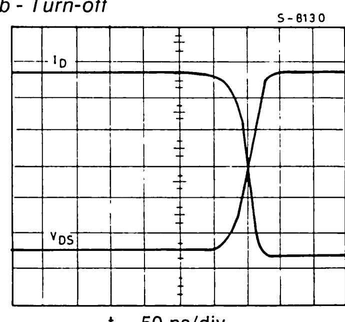
Typical drain current and voltage waveforms (t = 50ns / div.)

Fig. 12 a - Turn-on



t = 50 ns/div

Fig. 12 b - Turn-off



t = 50 ns/div

PARASITIC CAPACITANCES DURING SWITCHING CYCLES

As already mentioned the switching of an SGS POWER MOS device consists fundamentally in the loading and unloading of the input capacitor.

$$C_{iss} = C_{GS} + C_{GD}$$

From Eq.1 where $R_i.C_{iss}$ is the time constant R_i includes:

R_{gen} - the internal resistance of the generator,

R_1 - the resistor between gate and source to match the driving circuit,

R_G - the internal resistance of the gate.

Fig. 13 a - Equivalent circuit

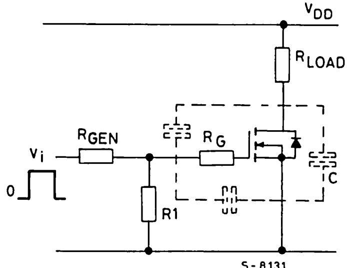
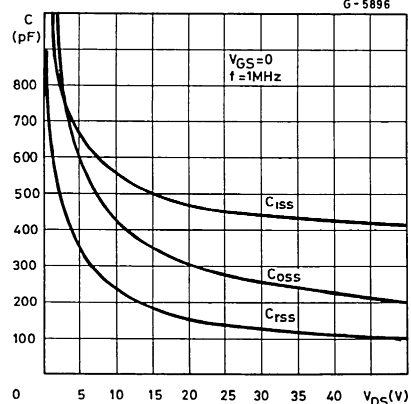


Fig. 13 b - Capacity values as a function of V_{DS}

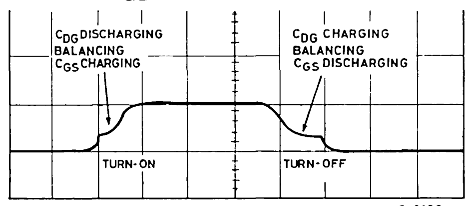


Obviously the smaller the value of Ri. C_{iss} the faster V_{GS} reaches its final value, and switches the device. To minimize this time constant the user can act on R_{gen} and R_1 and the device designer on C_{iss}.

C_{iss}, being a function of C_{GD}, varies as a function of the drain voltage as shown in the waveforms in fig. 13b and during switching it is subjected to the Miller effect. Consequently during the $t_{d(on)}$ and $t_{d(off)}$, C_{iss} remains constant, as

does the value of V_{DS}. $t_{d(on)}$ and $t_{d(off)}$ are obtained from the charging and discharging laws of a RC circuit, while during the off / on and on / off transitions, C_{iss} varies. In other words, when V_{DS} decreases during turn-on to a very low value $V_{DS(on)}$, and C_{GD} increases, there is a delay in the increase of the value of V_{GS} since the capacitor, as long as it is not charged to $V_{GS(on)}$, will absorb the gate current.
During turn-off due to V_{DS} rising the discharge current of C_{GS} will be balanced by the charging current of C_{GD}, flattening the V_{GS} curve and making it similar to that at turn-on (Fig. 13c).

Fig. 13 c - An annotated extract from fig. 5 showing the discharging and charging of C_{GD}



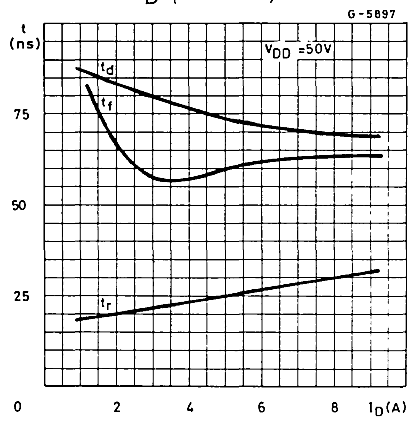
t: 0.5μs/div, I: 0.1A/div, V: 10V/div

Variations in the supply voltage V_{DD} influence these effects: the higher the supply voltage the greater the charge and therefore the t_f and driving energy required (see fig. 8 in the section OUTPUT).
Figs. 14, 15, 16 and 17 show the switching time waveforms as a function of both the supply voltage V_{DD} and the load current I_D, for two devices with different voltages and die sizes.

SGSP311 100V 7A 0.3 ohm 110 × 110 mils²

SGSP369 500V 5A 1.75 ohm 156 × 156 mils²

Fig. 14 - Time measurement t_d, t_f, and t_r as functions of I_D. (SGSP311)



The t_r and t_f waveforms versus V_{DD} are similar to those of E_p versus V_{DD} since they are both caused by the same phenomena. t_d is independet of V_{DD} as it is a function of C_{iss} only (which, since the Miller effect is not present, is constant during this phase).
t_d = delay time
t_f = fall time
t_r = rise time

Fig. 15 - Time measurements t_d, t_f and t_r as functions of the drain voltage for a low voltage SGS POWER MOS. (SGSP311)

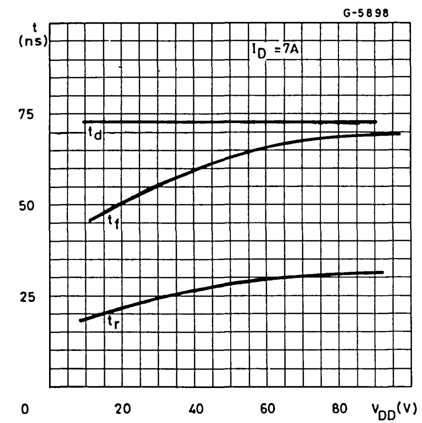


Fig. 16 - Time measurements t_d, t_f and t_r as functions of the drain current for high voltage SGS POWER MOS (SGSP365)

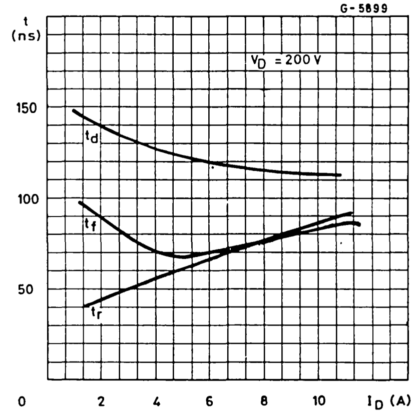
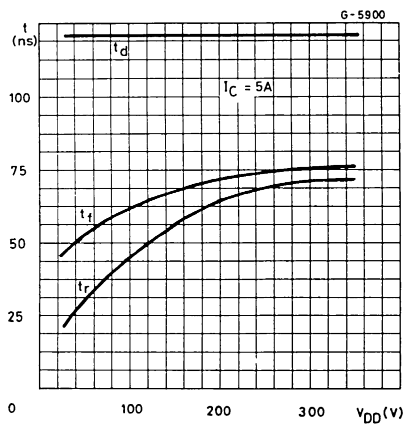


Fig. 17 - Time measurements t_d, t_f and t_r as functions of the drain voltage for high voltage SGS POWER MOS



Switching times for inductive loads

In the majority of applications SGS POWER MOS are used in switching power through inductive loads (motor control, switching power supply etc.).

The fundamental objective of the device is to switch high quantities of power very quickly, in other words to maximize the ratio:

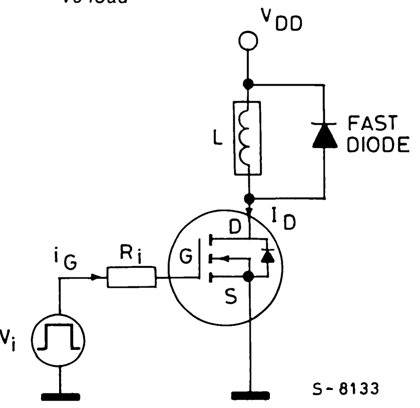
$$\frac{\text{total power switched}}{\text{energy dissipated per cycle}}$$

which depends principally on the switching times.

Understanding switching with SGS POWER MOS requires consideration of both the physical phenomenon and the energy dissipation occuring during each switching cycle.

The typical clamped inductive load circuit shown in fig. 18 is used as an example.

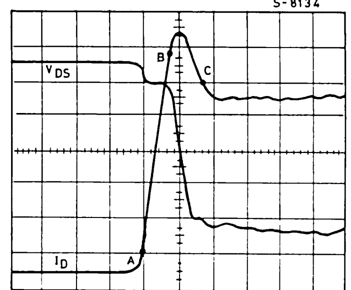
Fig. 18 - SGS POWER MOS with clamped inductive load



TURN - ON

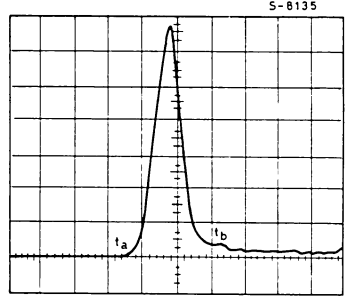
A detailed explaination of the turn-on phenomena in a SGS POWER MOS device when the load is inductive is given by Fig. 19 and 20.

Fig. 19 - Current and voltage waveforms during turn - on



t: 50ns/div, I: 1.2A/div, V: 40V/div, R=25Ω

Fig. 20 - Output energy consumption during turn-on



t: 50ns/div, P: 200W/div, E: 67.5 µJ

Before the turn-on phase the diode is freewheeling the load current.

Turn-on can be divided into two subphases:

1) point A to point B (Fig. 19).

Part of the current in the load (constant during the switching operations) starts to flow in the SGS POWER MOS device. The diode is recovering its reverse state. The voltage across the SGS POWER MOS device is almost equal to that of the supply since the diode still acts as a short circuit for the load at this point. There is a small step in V_{DS} waveform due to the voltage drops on the parasitic inductances L_D and L_S. The size of this step depends on the current slope dI_D/dT (L_S and L_D depend on the circuit layout).

2) point B to point C (Fig. 19).

In this phase the diode is reverse biased. The current in the SGS POWER MOS device is the sum of the current in the load plus that in the diode, which causes the peak in the I_D waveform. (see fig. 24)

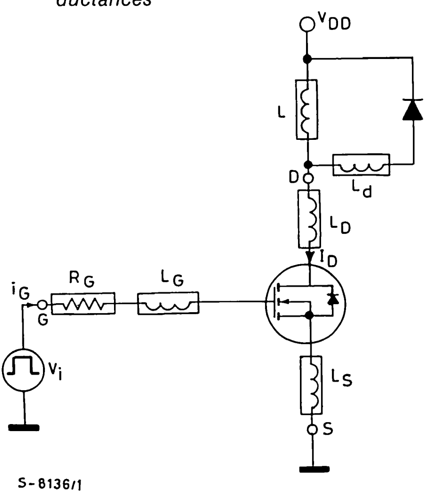
The V_{DS} voltage falls to $V_{DS(on)}$ as the freewheeling diode, being reverse biased, is no longer a short circuit. However the fall of V_{DS} is delayed by the Miller effect, which increases Ciss.

All these phenomena cause a high crossover between the I_D and the V_{DS} waveforms even if the switching is very fast. In Fig. 20 the output energy consumption per turn-on phase is represented. To decrease this energy, the d_{ID}/dt (A-B phase) and the reverse recovery of the freewheeling diode (B-C phase) must be improved.

- IMPROVING d_{ID}/dt

Reference to the circuit in Fig. 21 shows the controlling parameters for d_{ID}/dt.

Fig. 21 - Circuit which includes the parasitic inductances



In this circuit the following elements have been taken into consideration:

L_d - is the parasitic inductance due to the connections between the clamping diode and the load.

L_D - is the parasitic inductance between the drain of the SGS POWER MOS device and the load.

L_G - is the parasitic inductance between the gate and the driving circuit.

L_S - is the parasitic inductance between the source and the ground.

The equation that applies to the input loop is:

$$V_i = R_i \times i_G + L_G\, di_G/dt + V_{GS} + L_S\, dI_D/dt$$

Where R_i is the equivalent resistance of the driving circuit. When considering the phase when I_D increases it is possible to neglect the term L_G di_G/dt as $di_G/dt = 0$.

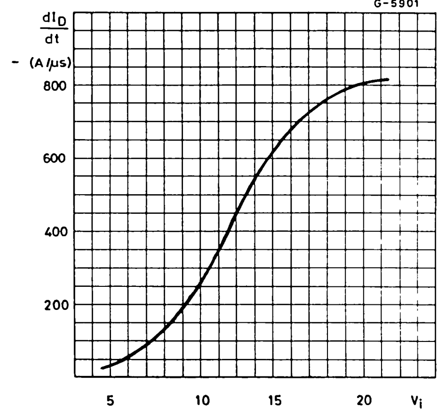
During this phase the threshold voltage has already been overcome, i_G is constant. In addition V_{GS} follows the law of charging a constant capacitance. The Miller effect is not present as V_{DS} is constant.

It follows that:

$$dI_D/dt = \frac{V_i - R_i \cdot I_G - V_{GS}}{L_S}$$

and dI_D/dt can be improved by increasing V_i and decreasing R_G and L_S.

Fig. 22 - dI_D/dt as a function of V_i (R_G=25Ω) for SGSP369



Improving the reverse recovery of the diode

As previously mentioned, the clamping diode plays an important role in determining the waveforms of I_D at turn-on; the faster the diode, the lower the current peak in the SGS POWER MOS, the lower the reverse recovery time of the diode (t_{rr}) and the energy consumption. For this reason fast recovery diodes are typically used in these circuits.

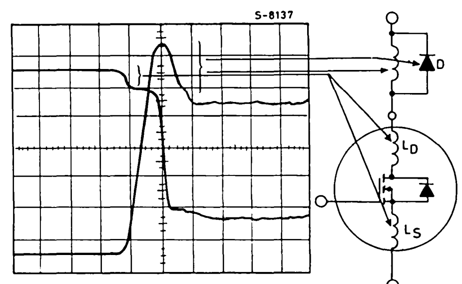
SGS is developing a wide range of fast recovery diodes whose target characteristics are shown below (fig. 23).

Fig. 23 - SGS Fast recovery diodes

DEVICE	$V_{REVERSE}$	$I_{FORWARD}$	t_{rr}	PACKAGE
SGS8R05-->20	50V/200V	8 A	35 ns	DO-220
SGS15R05-->20	50V/200V	15 A	35 ns	DO-220
SGS30R05-->20	50V/200V	30 A	35 ns	SOD- 93
SGS35R120	1200 V	35 A	100 ns	SOD- 93
SGS45R80	800 V	45 A	100 ns	SOD- 93
SGS60R40	400 V	60 A	100 ns	SOD- 93

The effect of parasitic inductances L_D and L_S and of the diode connections respectively on V_{DS} and I_D are shown in Fig. 24.

Fig. 24 - Shows the effects of the parasitic inductances L_D and L_S and of the diode connections respectively on V_{DS} and I_D waveforms



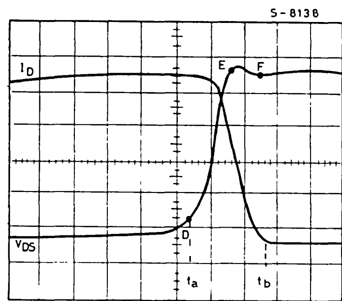
TURN-OFF

The circuit in Fig. 18 is still useful in evaluating the behaviour of an SGS POWER MOS device turning off an inductive load. The initial conditions can be assumed to be:

1) $I_D = I_{LOAD}$
2) $V_{DS} = V_{DS\ (on)} = R_{DS\ (on)} \times I_D$
3) Freewheeling diode reverse biased.

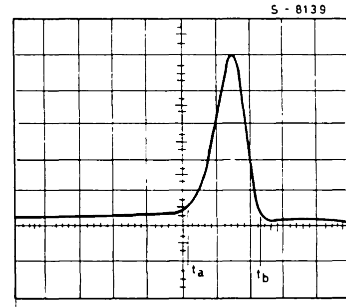
In fig. 25 typical waveforms for V_{DS} and I_D during turn-off phase are represented

Fig. 25 - V_{DS} and I_D during turn-off



t: 50ns/div, V: 40V/div, I: 1.2A/div, Rg=25Ω, Vg=10 V

Fig. 26 - Output Energy during turn-off phase.



t: 50ns/div, P: 200 W/div, E=70.6μJ

It is possible to distinguish two phases:

1) From point D to point E (Fig. 25).

During this phase V_{DS} increases while I_D , the diode being reversed biased, remains constant and equal to I_{LOAD}.

2) From point E to point F (Fig. 26).

During this phase the diode begins conducting allowing the current in the load to flow through itself and I_D of the POWER MOS device to fall. In Fig. 26 the output energy consumption during the turn-off phase is represented.

Also in this case a high cross over between V_{DS} and I_D occurs, even if there is no reverse recovery of the diode as during the turn-on phase. The Miller effect in the SGS POWER MOS device delays the rise of V_{DS} and therefore the switch-on of the freewheeling diode D.

Energy in switching

From the energy point of view there are four distinct phases, each contributing in a different way to the total dissipated energy per cycle. They are:

1) ON - STATE
2) OFF-STATE
3) Transition ON-OFF
4) Transition OFF-ON

The ON-STATE

In the ON-STATE, when the channel is completely open, SGS POWER MOS devices have a minimun $R_{DS\ (ON)}$ which is temperature dependent. The power dissipation at a given instant is obtained from the equation:

$$P_{D(ON\text{-}STATE)} = R_{DS(ON)}(T_j) \times I_D^2$$

$$= R_{DS(ON)} \times [1 + \alpha(T_j - 25°C)] \times I_D^2$$

where $\alpha = 8 \times 10^{-3}\ °C^{-1}$, a positive coefficient.

The lower $R_{DS(ON)}$ the lower the power dissipation. The manufacturers can control $R_{DS(ON)}$:

1) by improving the back metalization of the chip and its attachment to the case.
2) by controlling the epitaxial growth of the DRAIN.
3) by optimizing the horizontal lay-out of the Power Mos structure (high cell density).

Fig. 27 - Can be used to calculate the energy consumption during the ON phase

Fig. 27 - I_D waveform during the working cycle

t_1 τ t_2

S-8140/1

The slope of I_D during the conduction phase is given by $dI_D/dt = V_{DD}/L$ (see Fig. 19).
The lost energy per cycle is given by:

$$E_{on} = \int_{0}^{\tau} I_D^2(t) \times R_{DS(ON)} \times dt$$

where τ is the pulse width.

In most cases the slope of I_D is quite gentle so if we call I the average I_D between t_1 and t_2, ($t_1 - t_2 = \tau$) in Fig. 27, this energy can be calculated with good approximation as follows:

$$E_{on} = R_{DS(ON)} \left(T_j\right) \times I^2 \times \tau$$

In Fig. 28, 29, and 30 the curves of E_{on} are shown for three different devices. Each curve is characterized by different values of τ.

Fig. 28 - On state energy values as a function of the drain current for SGSP301

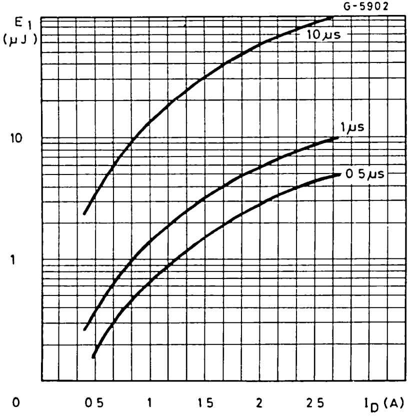


Fig. 29 - On-state energy waveforms as a function of the drain current SGSP575.

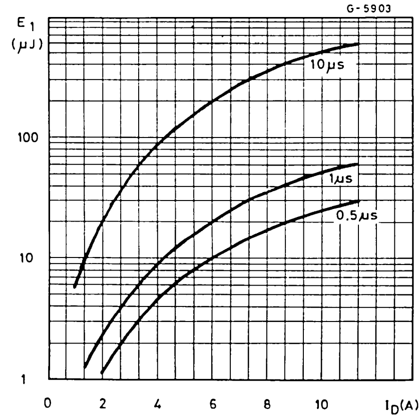
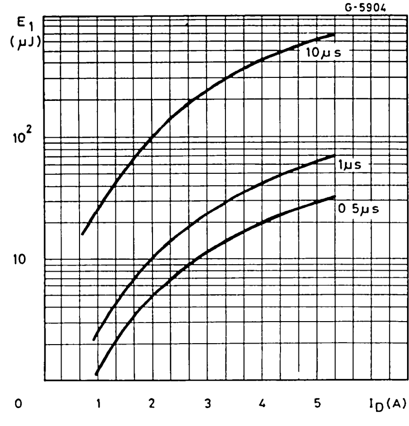


Fig. 30 - On-state energy values a function of the drain current SGSP531



OFF-STATE

When the device is switched off the V_{DS} voltage is equal to V_{DD} (see Fig. 25). Only the leakage current I_{DSS} flows through the device. The energy consumption during this period is given by:

$$E_o = V_{DD} \times I_{DSS} \times t_{off}$$

This energy is in the range of pJ and it is negligible in comparison to that dissipated during the switching and the ON-STATE.

Transitions

During transitions the dissipated power, instant by instant, is:

$$P(t) = V_{DS}(t) \times I_D(t)$$

The power waveform is triangular in shape (see Fig. 20 and Fig. 26). Integrating P(t) the energy consumption per cycle during OFF-ON and ON-OFF transitions can be obtained by:

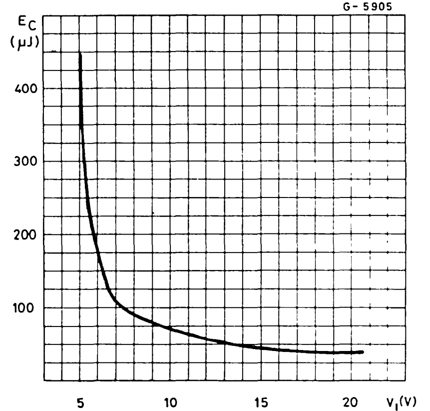
$$E = \int_{t_a}^{t_b} P(t)dt = \int_{t_a}^{t_b} V_{DS}(t)\, I_D(t)dt$$

Where t_a and t_b respectively represent the begining and the end of transitions. These amounts of energy principally depend on the intersecting point between voltage and current, and on the switching speed.
In both transitions the intersecting points are very high and occur at a voltage value close to that of the supply. The intersecting points represent the power to be switched, consequently in order to optimize the energy consumption the time interval $t_a - t_b$ must be reduced by acting on different driving and lay-out parameters (V_{GS}, R_{GS}, parasitic inductances).

Fig. 31 - Shows the energy lost per cycle during

the ON/OFF transition, as a function of V_i for an SGSP369 switching 4A at 200 V.

Fig. 31 - Values of the energy lost per cycle as a function of the gate voltage



Computing the total energy consumption per cycle

The previous analysis allows us to calculate the total energy dissipated per cycle in an SGS POWER MOS device. In fact the total energy can be expressed as:

Eq.3 $E_{TOT} = E_{on} + E_{off} + E_{off/on} + E_{on/off} + E_p$

where:

E_{TOT} = total energy dissipated per cycle
E_{on} = energy dissipated during the on-state
E_{off} = energy dissipated during the off-state
$E_{off/on}$ = energy dissipated during the turn-on
$E_{on/off}$ = energy dissipated during the turn-off
E_p = total energy dissipated by the drive circuit

Neglecting E_{off} (= pJ) and E_p (= nJ) Eq. 3 can be re-written as:

Eq.4 $E_{TOT} = E_{on} + E_{off/on} + E_{on/off}$

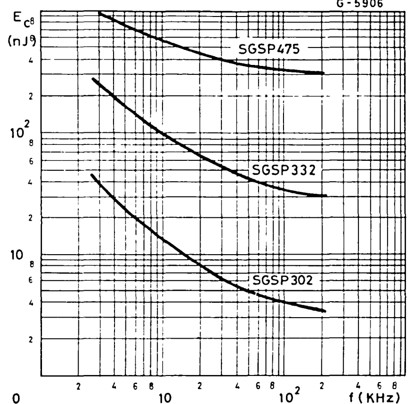
These three terms in Eq. 4 depend in differing amounts on the operating conditions of the device I_D, V_{DD} and the duty cycle.
To give some idea of the total energy dissipated per switching cycle the following operating conditions have been fixed and the results of energy measurements made shown in Fig. 32.

$V_{DD} = 1/2\ BV_{DSS}$ of the device under test

$I_D = 3/4\ I_{DMAX}$ of the device under test

duty cycle = 50%

Fig. 32 - Total energy lost per cycle as a function of the frequency with a fixed duty eycle of 50%



The curves tend towards a horizontal asyntote that represents the cross-over energy (turn-on + turn-off, which is frequency independent).
It is clear that the effect of E_{on} is of great importance at low frequencies, and the higher the $R_{DS(ON)}$ the greatest the effect.

REVERSE RECOVERY TIME (t_{rr}) OF THE BODY-DRAIN DIODE IN SGS POWER MOS TRANSISTORS

ABSTRACT

The parasitic damper diode in SGS POWER MOS transistors is actually designed to work at the same current rating of the transistor itself. The test circuit for that diode recovery time is described; the typical results for several SGS POWER MOS transistors are compared with competition parts, standard rectifiers, fast rectifiers and damper diodes of some significant bipolar SGS darlingtons.

THE BODY-DRAIN DIODE

SGS POWER MOS have got, in their internal structure a diode between source and drain. It can be used as such, from an external point of view. The dimensioning of it is usually such that it can easily carry d. c. current equal to the rated I_{DM} of the transistor.

Fig. 1 shows the SGS POWER MOS N-channel symbol and the internal structure of a bias element of it. As source and body are short circuited by the source metallization, the body-drain diode appears externally in between source and drain.

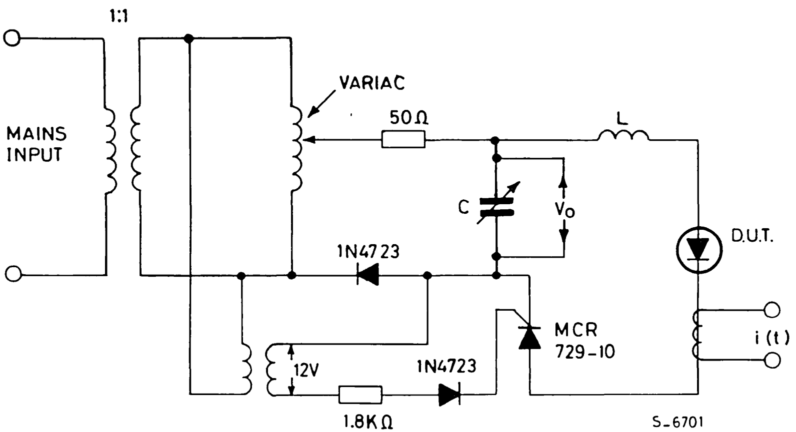
As SGS POWER MOS are devices used in application as motor control bridges or switching converters where the damper diode can conduct, it's of prime importance to characterize the damper diode switching parameters.

One of the most important parameter of a diode for switching applications is t_{rr} (reverse recovery time). The t_{rr} is the time that the diode needs to get rid of the charge (stored during ON period) at the moment when it is switched off.

That charge makes the diode act as an undesirable short circuit, possibly affecting the overall performances or reliability of the equipment. Consequently for high speed switching applications (almost always the case with SGS POWER MOS)its switching behaviour (t_{rr}) needs characterizing and the shorter it is, the better.

Fig. 1 - SGS POWER MOS Cell structure

Fig. 2 - Test circuit



THE TEST CIRCUIT

The circuit used for t_{rr} measurements is the one well known in the industry, and is schematically described in fig. 2.

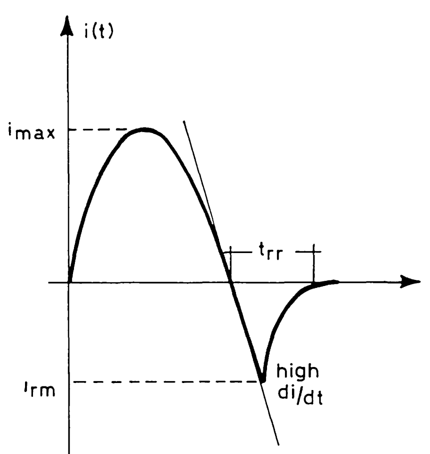
Capacitor C is charged, via the 50 ohm resistor, by the sinusoidal half wave available from the variac. The same waveform will allow for syncronus triggering of the SCR, during the half wave in the opposite phase (the measuring circuit is decoupled by the diode during that time).

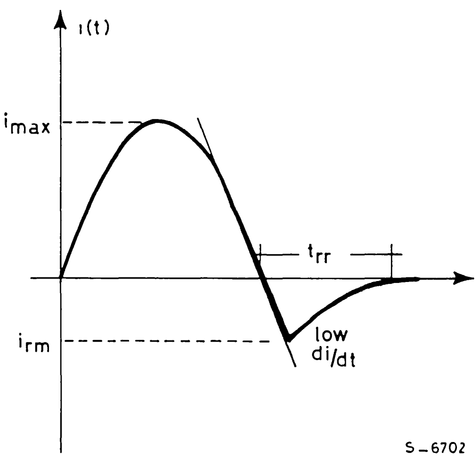
The turn on of the SCR will make the capacitor discharge via the diode under test (D.U.T.) and the inductor (actually almost only the stray-inductance of the circuit).

As a result a current pulse of a sinusoidal shape will be flowing via the D.U.T. due to the LC resonant circuit.

By adjusting both the capacitor peak voltage V_O and the capacitance value, both peak and zero crossing slope of the current pulse can be adjusted. See figure 3

Fig. 3





These are the most relevant conditions because:

1. peak current value is related to the stored charge in the diode, wich increases with it and consequently takes more time to recover at switch-off.
2. Current slope at zero crossing (di/dt) is also heavily influencing t_{rr} readings, and t_{rr} is higher with lower di/dt.

The test conditions must be clearly specified, and any comparison between different devices must be based on the same test conditions in order to be significant.
It can be verified that, properly setting V_O and C, both i_{max} and di/dt can be adjusted to the desired values. In particular, the stray inductance must be kept small in order to achieve high di/dt with low V_O.

THE RESULTS OBTAINED

To understand whether the source-drain diode is similar to a fast-recovery one, the comparison has been made against:

- general purpose rectifiers (e. g. 1N004)
- integrated damper diodes in low voltage (e. g. BDX53C) and medium voltage (e. g. BU911) SGS darlingtons
- fast recovery rectifiers (e. g. MR856, FE5D, FE8D)
- competition Power Mos.

CONCLUSIONS

Following conclusions can be drawn:

1. SGS POWER MOS damper diodes in low voltage parts (60 to 100V) are fairly fast, even through not reaching the best fast recovery diodes on the market.
2. SGS POWER MOS damper diodes in medium voltage parts (400V) are relatively slow, and their t_{rr} is similar to:
   - general purpose rectifiers on the market
   - integrated damper diodes inside SGS monolithic darlingtons and transistors (BU806, BU931, BDX33C, BU911, BU406D, etc.)
3. Damper diodes of competition Power Mos we tested:
   - have got equivalent t_{rr} in medium voltage parts
   - have got higher t_{rr} in low voltage parts than SGS POWER MOS parts.

Note:

All measurements hereunder have been performed at I_F = 10A. But 400V parts (SGSP311, IRF722) are not likely to used in actual applications at I_F = 10A. A value of I_F = 2A is the most probable, and the t_{rr} will be appreciably lower in that case.

STANDARD RECOVERY RECTIFIER

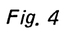
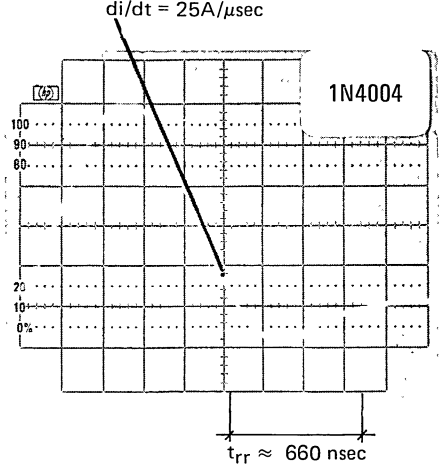
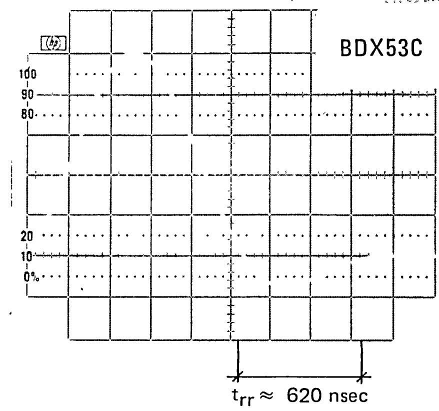


Fig. 4



DAMPER DIODES INTEGRATED INTO MONOLITHIC BIPOLAR DARLINGTONS

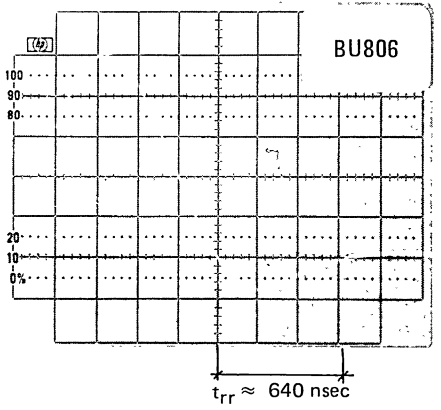
Fig. 5



Hor : 200 nsec/div

Vert : 2A/div

Fig. 6



Almost Equal Values for
SGS Bipolars BU931, TIP122,
TIP142, SGSD100, BU406D

FAST RECOVERY RECTIFIERS

Fig. 7

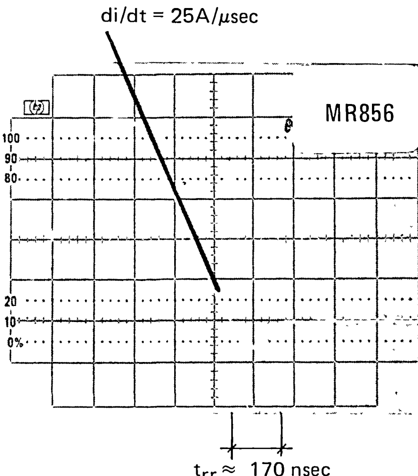
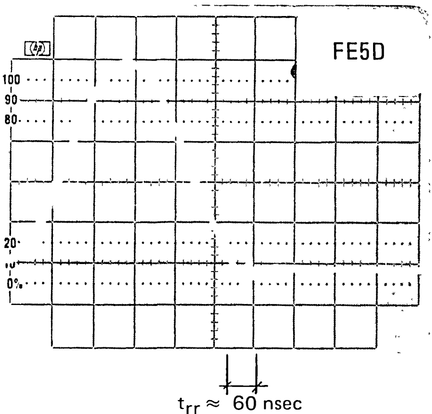


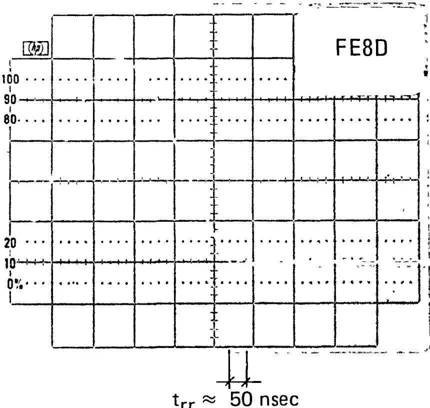
Fig. 8



Hor : 200 nsec/div

Vert : 2A/div

Fig. 9



SGS POWER MOS BODY-DRAIN DIODE

Note:

SGSP321 and SGSP521 are intrinsically the same device. Remark how different test conditions lead to different t_{rr} readings.

Fig. 10

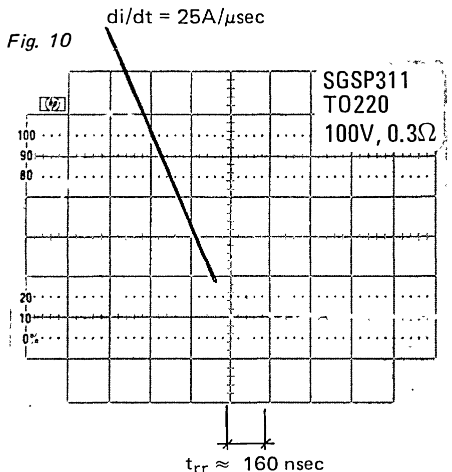
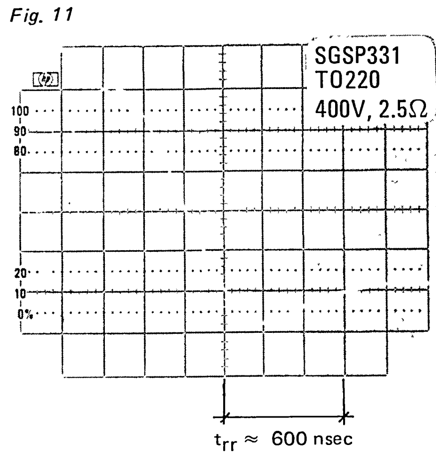


Fig. 11



Hor : 200 nsec/div

Vert : 2A/div

Fig. 12

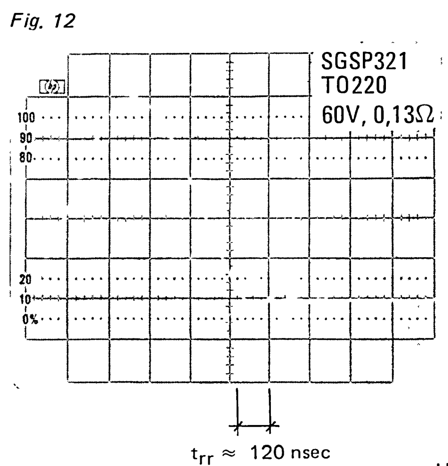
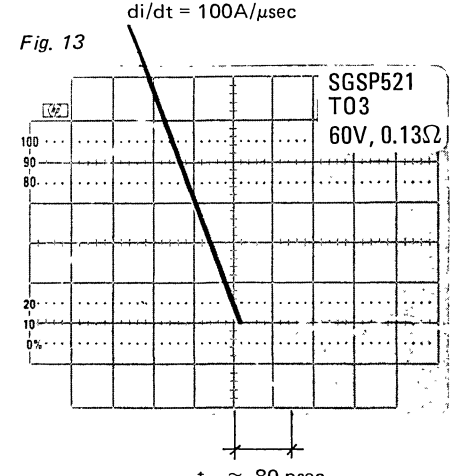


Fig. 13

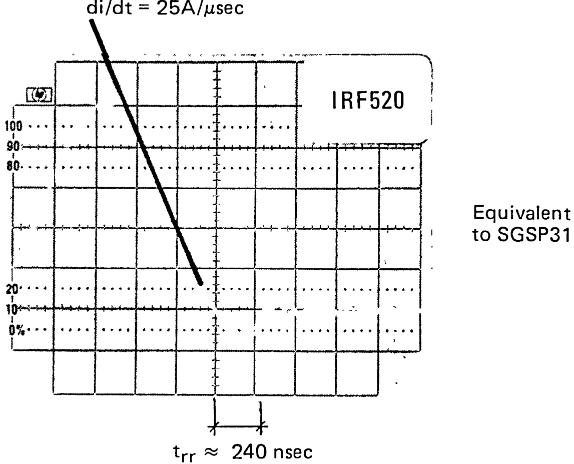


Hor : 50 nsec/div

Vert : 2A/div

COMPETITION POWER MOS BODY-DRAIN DIODE

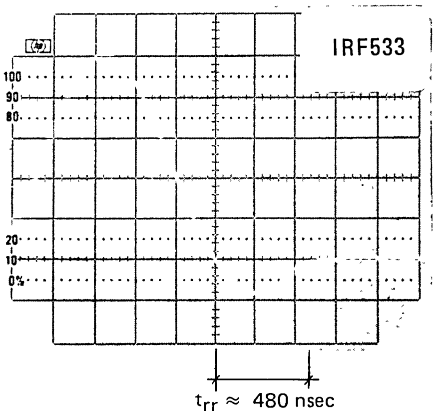
Fig. 14



$t_{rr} \approx$ 240 nsec

Equivalent to SGSP311

Fig. 15



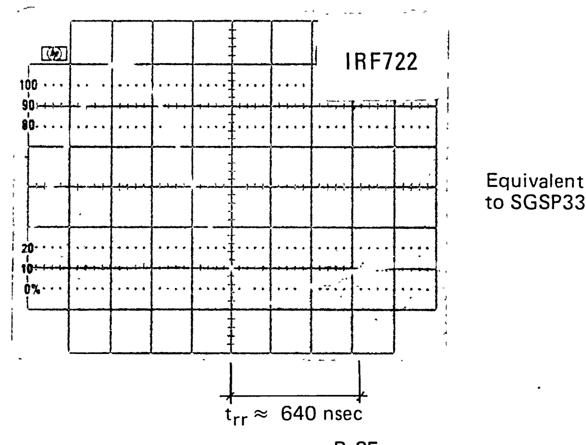
$t_{rr} \approx$ 480 nsec

Equivalent to SGSP321

Hor : 200 nsec/div

Vert : 2A/div

Fig. 16



$t_{rr} \approx$ 640 nsec

Equivalent to SGSP331

THE BODY DRAIN DIODE IN BRIDGE CONFIGURATIONS

INTRODUCTION

The parasitic body - drain diode can be used as the recirculating element when implementing a bridge with four SGS POWER MOS.

The circuit designer is given all the relevant parameters in order to evaluate their behaviour with respect standard rectifiers and fast rectifiers produced by SGS.

The characterization is made assuming a bridge battery voltage of 10V. This voltage represents one of the most promising application fields area for SGS POWER MOS, that is the automotive environment, where the 12V automotive battery is the source for all power applications.

GENERAL INFORMATION

A power device, MOS or bipolar, is practically always used as a switch, and in the majority of cases, on inductive loads.

To avoid overstresses due to the overvoltages induced by the inductive kick at the turn-off of the loads, protective networks are utilized.

POWER MOS devices in particular can hardly sustain an overvoltage associated with any significant energy.

The configurations in figure 1 make use of diodes to protect the transistors. The energy stored in the inductive loads are diverted from the transistor to the diodes (and to the battery in cases c and d) when the transistor switches off.

Although the diode topologically represents the simplest solution for the protective network, its choice is not that simple, because its characteristics greatly influence the stress that the transistors must sustain at turn-on and turn-off.

Fig. 2 shows the current and voltage waveforms for a SGS POWER MOS used in the circuit shown in figure 1a.

When the transistor turns on, due to the recovery of the diode, the locus of the working points describes a curve as in figure 3a.

It is evident that, for a short while, the transistor is made to carry a peak current I_{DP} that can be much greater than the maximum current I_{Dmax} stated in the Safe Operating Area (S.O.A.) diagram.

The peak current is created by the recovery of the diode, and is only limited by the gain h_{fe} (of g_{fs}) of the transistor and by its driving current (or voltage).

Fig. 1 - Usual configuration to drive the inductive load

+V

D

G

DUT

S

S-8192

(a)

+V

C

B

DUT

E

S-8193

(b)

S-8194

(c)

Q1

D3

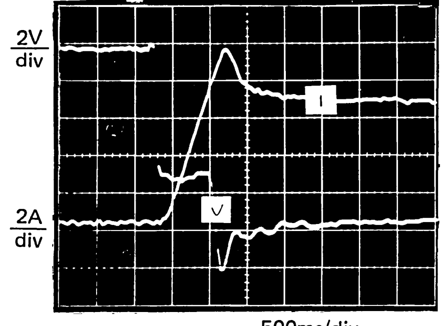
D2

Q4

S-8195

(d)

Fig. 2 - Current and voltage waveforms across switching device



As a result, for a given gain of the device (h_{fe} if it is a bipolar, g_{fs} if it is a SGS POWER MOS), it is important:

— to use a driving not in excess of what strictly needed (for bipolar only)

— to use fast recovery rectifiers

Figures 3b shows how a fast diode implies a lower current peak, everything else being equal.

The two suggestions given have substantial drawbacks, as for instance, the on-state voltage drop and the cost.

Fig. 3a - Operating points locus

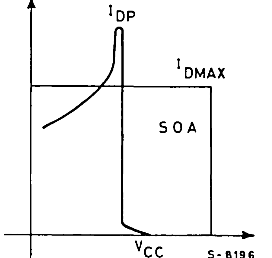
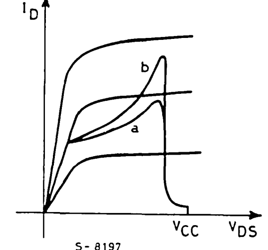


Fig. 3b - Comparison between fast and slow diodes



In conclusion, a detailed knowledge of the electrical characteristics of the body-drain diode - that is always available free - is mandatory in order to decide whether it can be used as a circuit element, or an external diode is needed.

For the characterization, a half bridge configuration has been chosen and, the circuit behaviour has been investigated in conditions as close as possible to the expected practical applications.

In particular the $\left(\frac{dI^2}{dt}\right)_{on}$ are different from the ones normally used when characterizing the discrete rectifiers (in the application they are lower).

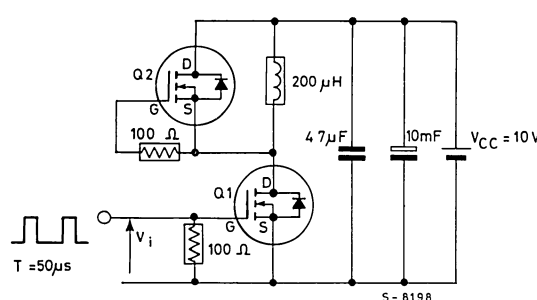
On the other hand, the transistor at its turn-off creates a dI/dt that varies greatly with the driving conditions, its technology and its specific characteristics.

Typically a SGS POWER MOS exhibits a much shorter t_{fall} than a bipolar, which turns to be a much higher dI/dt and consequently creates the possibility of oscillations, spikes and high V_f (peak forward voltage).

The testing circuit and the performances of the body-drain diode.

To characterize the diode performance the testing circuit of figure 4 has been used.

Fig. 4 - Test circuit



The switching frequency is 20kHz, and the freewheeling diode is the integrated SGS POWER MOS body-drain diode.

The following pictures show the waveforms obtained in some of the most significant measurements, and comparisons made between standard and fast rectifiers.

Table 1 resumes a series of measurements on several of the most representative devices in the SGS POWER MOS catalogue, obtained in the test set-up of figure 4.

It is important to take into account that:

- the interconnecting layout has been chosen in order to be representative of real applications neither very sophisticated nor too coarse (approximately 10cm from drain 1 to source 2 - see figure 4 - and 10cm from drain 1 to the power supply);
- the supply voltage (10V) is typical in applications (e.g. automotive electronics) of high volume SGS POWER MOS;
- had higher supply voltages been used, dI/dt would not have been significantly higher;
- dI/dt depends on the parasitic inductances (that is the physical lay-out) and on the switching speed of the SGS POWER MOS (that is the driving circuit).

However if higher supply voltages were associated to a sophisticated, fast driving circuit, the inductive overvoltages could reach dangerous levels.

CONCLUSIONS

The purpose of this note is to give the circuit designer an evaluation base to compare the body-drain diodes of the SGS POWER MOS with the discrete alternatives.

It is evident that the discrete fast recovery diodes certainly represent a faster, through more expensive, alternative.

Whether to make use of the integrated diode or not can be decided according to the information in table 1.

It characterizes the SGS POWER MOS as far as the internal diode in concerned for applications where:

- the supply voltage is in the 10V range;
- the physical lay-out is similar to what can be expected in practical implementations (connections of about 10cm in length between the SGS POWER MOS and the inductive load and the clamping diode, and those between two SGS POWER MOS in the same bridge leg).

Table 1

DEVICE	I_{FM} (A)	t_{rr} (ns)	I_{RM} (A)	t_{on} (ns)	dI/dt(on) (A/μs)	V_{FP} (V)	t_{fr} (ns)	V_{DSS}
SGSP531	1.5	800	1.4	40	10	9	20	400V
SGSP511	3.5	200	1	20	12	5	75	100V
SGSP567	5	350	2.1	60	10	8	45	200V
SGSP474-SGSP574	6	1100	4	40	8	18	40	450V
SGSP561	8	200	1	60	20	7	80	100V
SGSP573-SGSP577	10	700	2.8	30	9	12	60	250V 200V
SGSP571	15	300	1.5	280	10	6	150	100V

Fig. 5 - (SGSP573) I_D drain current

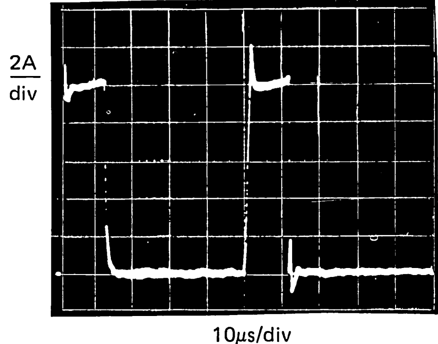


Fig. 7 - (SGSP561)

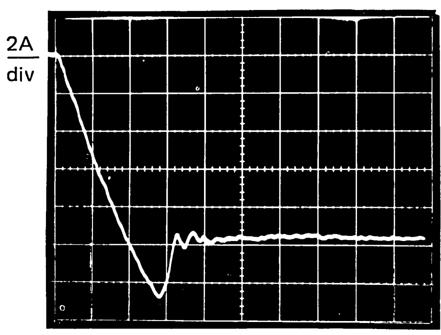


Fig. 6 - Current in the body-drain diode

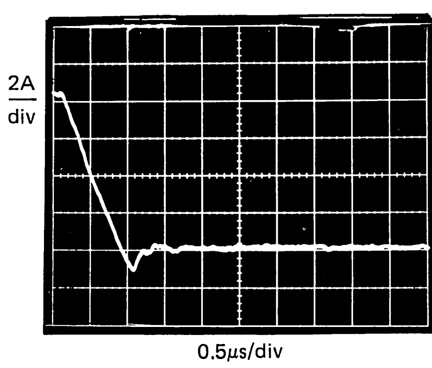


Fig. 8 - (SGSP571)

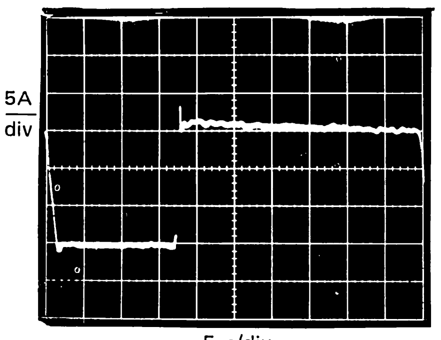
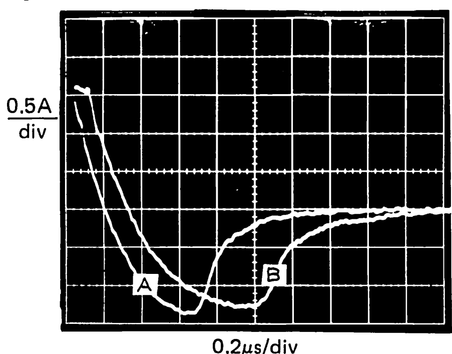


Fig. 9 – SGSP321 body-drain diode (A)



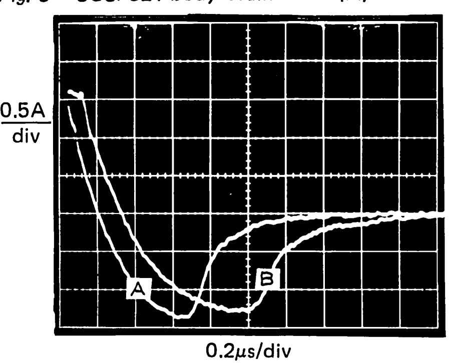


Fig. 11 – (SGSP474)

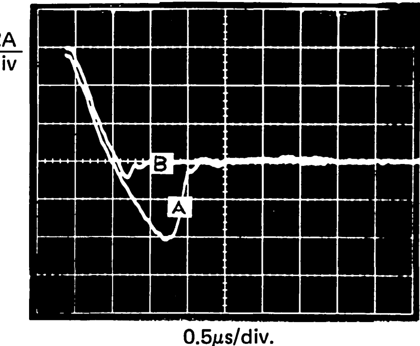
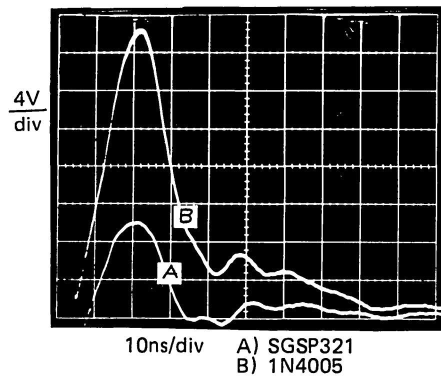


Fig. 10 – V_{fp} overvoltage (I_{fm} = 1.5A)



10ns/div A) SGSP321
B) 1N4005

2A
div

C

0.5μ s/div.

trr : A) D-S diode SGSP474
B) Fast recovery diode SGS
C) Diode 1N4005

STATIC dV/dt IN POWER MOS

INTRODUCTION

The use of POWER MOS in high frequency switching circuits is possible due to the rapid switching times of the device. Unfortunately in extremely high dV/dt conditions, secondary effects can occur. This has the unwanted (and possibly destructive) effect of switching on the device according to the mechanisms described later.

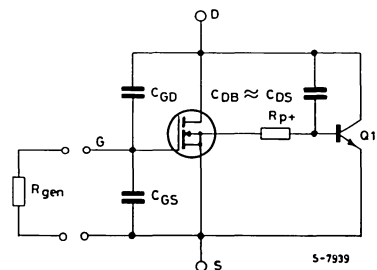
Static dV/dt means that a voltage variation with respect to time is produced on the device by an external electrical circuit. However when it is the device itself that produces the voltage variation, dynamic dV/dt, there are no practical problems of anomolous conduction.

The aim of this paper is to give a brief theoretical introduction, an idea of how this phenomenon is produced, and especially to discuss the order of magnitude of dV/dt that triggers it.

STATIC dV/dt IN POWER MOS

dV/dt is a phenomenon which limits the performance of POWER MOS in switching. It is also typical of SCR and other similar devices. In the case of POWER MOS it can easily be understood by analysing the following equivalent circuit:

Fig. 1 - Simplified equivalent circuit

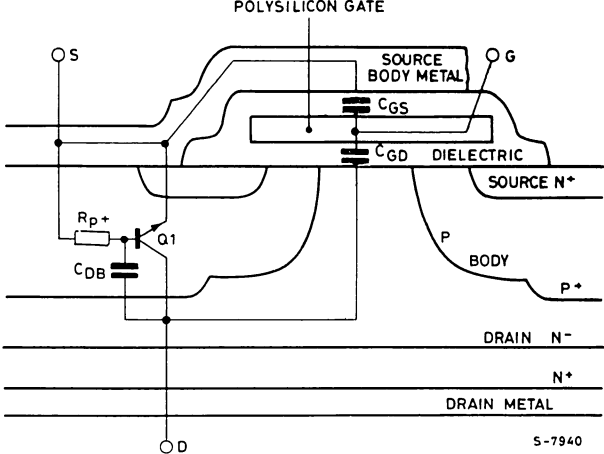


where:

- C_{GS} = parasitic capacitance between gate and source
- C_{GD} = parasitic capacitance between gate and drain
- R_{P^+} = parasitic resistance of the P^+ body region
- C_{DB} = parasitic capacitance between drain and body
- Q_1 = parasitic NPN transistor

This circuit can be located in the physical structure of the devices as shown in fig. 2.

Fig. 2 - Equivalent circuit outlined on the phisical structure



In this circuit all other parasitic elements of no concern in this analysis, have been neglected (body-drain diode, parasitic J-FET other resistance ect.).

Examining the equivalent circuit, we can see that essentially two mechanisms can trigger an anomalous conduction as a consequence of creating a V_{DS} variation with a very high dV/dt.

1) Effect of the parasitic input capacitances (C_{GD} and C_{GS})
2) Effect of output parasitic elements (C_{DB} and the parasitic bipolar transistor)

Let us analyse these two phenomena individually

1) EFFECT OF C_{GD} AND C_{GS}

In the input circuit a voltage ramp V_{DS} creates a current flow in the C_{GD} capacitor, according to the equation:

$$I_{CGD} = C_{GD} \times dV/dt$$

This current passes through the external resistor R_{gen}, in parallel with the C_{GS} capacitor, causing a voltage drop.
If there is a high dV/dt a voltage V_{GS} greater than the device threshold voltage may be created, so that the device is activated in the forward mode (the channel opens).
Such a phenomenon not only depends on the dV/dt but also on the following parameters:

a) R_{gen} generator resistance. A high output impedance of the driving circuit increases the possibility of anomolous conduction occuring.
b) C_{GD}, the reverse capacitance (in which the phenomenon can occur more easily) in large devices with a low $V_{(BR)DSS}$.
c) $V_{GS(th)}$ the threshold voltage, since the devices with a high $V_{GS(th)}$ need a greater V_{GS} to open the channel
d) V_{DS}, the applied voltage, because the capacitance varies with the change in the depletion area, the wider the depletion layer the lower the capacitance
   Therefore the phenomenon is more probable with a lower V_{DS}.

In general once this phenomenon has occured it does not damage the device. It is the unwanted current in the transistor that could cause very high frequency disturbances and interfere with the surrounding circuitry.

From a practical point of view, considering the first mechanism, what are the dV/dt levels which could theoretically trigger the phenomenon? To answer this question let us consider four SGS POWER MOS devices with different characteristics:

Devices	Ratings	Die size	$C_{iss} = C_{GS}+C_{GS}$	$C_{rss} = C_{GD}$	$C_{oss} = C_{DS}+C_{GD}$
SGSP511	100V 7A 0.3Ω	110x110mils²	375pF	90pF	180pF
SGSP571	100V 30A 0.075Ω	221x221mils²	1800pF	300pF	650pF
SGSP531	400V 3A 2.5Ω	110x110mils²	340pF	30pF	60pF
SGSP575	400V 12A 0.55Ω	221x221mils²	1600pF	200pF	300pF

Where the capacitance are measured at V_{DS} = 25V, f = 1MHz, V_{GS} = 0. The conditions necessary for the POWER MOS to conduct are:

$$I_{CGD} \times R_{gen} > V_{GS(th)}$$

Substituting for I_{CGD} we get

$$C_{GD} \times dV/dt \times R_{gen} > V_{GS(th)}$$

which by rearrangement becomes

$$dV/dt = \frac{V_{GS(th)}}{R_{gen} \cdot C_{GD}}$$

The threshold voltage value of SGS POWER MOS is between 2V and 4V, so if we consider an average value of $V_{GS(th)}$ = 3V, we have:

$$\left(\frac{dV}{dt}\right)_{min} = \frac{3}{90 \cdot 10^{-6}\ R_{gen}} \frac{V}{\mu s} \quad \text{(SGSP511)}$$

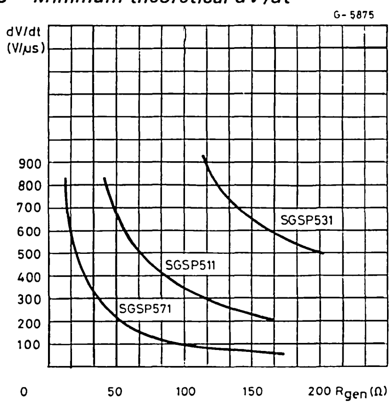
$$\left(\frac{dV}{dt}\right)_{min} = \frac{3}{300 \cdot 10^{-6}\ R_{gen}} \frac{V}{\mu s} \quad \text{(SGSP571)}$$

$$\left(\frac{dV}{dt}\right)_{min} = \frac{3}{30 \cdot 10^{-6}\ R_{gen}} \frac{V}{\mu s} \quad \text{(SGSP531)}$$

$$\left(\frac{dV}{dt}\right)_{min} = \frac{3}{200 \cdot 10^{-6}\ R_{gen}} \frac{V}{\mu s} \quad \text{(SGSP575)}$$

The following graph gives an idea of the range of dV/dt for which an indirect turn-on of the device is possible.

Fig. 3 – Minimum theoretical dV/dt



2) EFFECT OF C_{DS} AND THE PARASITIC TRANSISTORS

A voltage ramp with a high dV/dt, as in the previous case causes the flow of current in the capacitor C_{DS} (see equivalent circuit of fig. 2). This current also flows in the R_P resistance of the body (located between the base and the emitter of the parasitic bipolar transistor) causing a voltage drop. If this voltage is greater than the threshold level of the base-emitter junction (about 0.65V), the transistor will conduct passing from a condition of short-circuited base (V_{CES}) to a forward biased one (where V_{CES} describes the breakdown limit).

Therefore if the applied V_{DS} is very close to $V_{(BR)DSS}$ (almost identical to BV_{CES} of the parasitic transistor) then it will certainly be greater than V_{CEO}, and so the bipolar parasitic transistor will undergo a breakdown condition.

To protect the devices the effects of the parasitic transistor are minimized by:

a) a short circuit, by metalization (in practice a very low resistance) between body and source

b) a large body area so that the parasitic transistor has a very low h_{FE} (35 at I_B = 5mA)

Let us now quantitively describe the phenomenon:

The current passing through the capacitor C_{DB} is:

$$I_{CDB} = C_{DB} \times \frac{dV}{dt}$$

Furthermore, for the parasitic transistor to conduct, we need:

$$I_{CDB} \times R_{body} > 0.65V$$

hence:

$$\frac{dV}{dt} > \frac{0.65}{R_{body} \times C_{DB}}$$

From this data we can obtain the following values:

SGSP511	C_{DB}	≅	C_{DS} = 90pF
SGSP571	C_{DB}	≅	C_{DS} = 350pF
SGSP531	C_{DB}	≅	C_{DS} = 30pF
SGSP575	C_{DB}	≅	C_{DS} = 100pF

However the calculation of R_P⁺ with a reasonable approximation is the biggest problem. One suitable method to confirm the theoretical calculation is the "snap-back" current. This is the current that creates the breakdown in SGS POWER MOS.

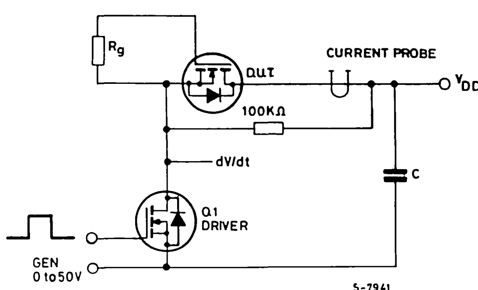
From the results in the appendix the following minimum dV/dt values for conduction to occur can be obtained.

SGSP511	dV/dt	>	8V/ns
SGSP571	dV/dt	>	3.5V/ns
SGSP531	dV/dt	>	4V/ns
SGSP575	dV/dt	>	2.5V/ns

EXPERIMENTAL RESULTS

The following circuit was set up to obtain high dV/dt values on the device under test (D.U.T.).

Fig. 4 - Measurement circuit



In this circuit the faster the Q_1 device switches, the faster the power supply voltage is applied to the D.U.T. To achieve this, the Q_1 POWER MOS is driven by a generator (TEK 109 MWR GENERATOR), which allows Q_1 to switch with a very low ton. It is during this phase that the high dV/dt needed to investigate the phenomenon is applied to the D.U.T.

As a driving transistor (Q_1 in the circuit diagram) a SGSP365 (400V, 6A, 1Ω) is used in order to obtain very high V_{DD} and short switching times. Particular samples were chosen to have V_{GS} = 50V to reduce the danger of damaging the gate oxide.

By increasing the generator voltage a lower ton of the driver device is achieved and therefore the value of dV/dt increases.

From these measurements the values of dV/dt shown in the graph were obtained. It is in this range of dV/dt that the phenomenon becomes evident.

The analysis was carried out in two principal steps:

1) V_{GS} of D.U.T. = 0V (R_{gen} = 0)

In this case the first triggering mechanism does not take part, so the unwanted current pulses or any eventual damage to the device must be due to the interference of the bipolar parasitic transistor (second mechanism). The tests showed this to be a very critical condition for the devices. At or above the following dV/dt values the presence of the current pulse caused by the triggering of the parasitic transistor can be observed:

Type	dV/dt minimum (I_{peak} = 1A)
SGSP511	5V/ns
SGSP571	1V/ns
SGSP531	5V/ns
SGSP575	4V/ns

The above values are in approximate agreement with the theoretical analysis. By increasing the value of dV/dt to the maximum permitted by the circuit, the analysis showed a high percentage of failures (see following table).

The damaged devices show a short circuit in $V_{(BR)DSS}$. The devices which passed the test have the following peak current values for the maximum dV/dt obtained.

Type	I_{peak}	V_{DD}	dV/dt
SGSP511	3.5A	100V	10V/ns
SGSP571	12A	100V	10V/ns
SGSP531	6A	400V	20V/ns
SGSP575	13A	400V	20V/ns

Fig. 5 - dV/dt obtained without D.U.T.

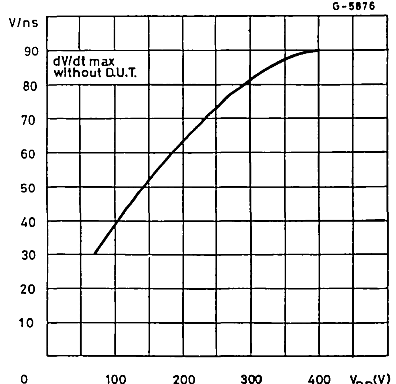
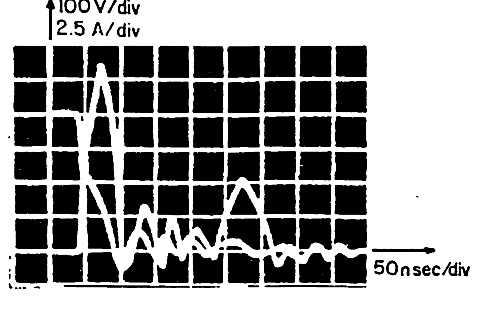


Photo 1 - The behaviour of a SGSP575 device



2) $R_{gen} = 0$

In this case besides the effect of the parasitic transistor there is also the effect of the input current. In general more failures occur with the increase of R_{gen}, because the current peak is heightened by the contribution of the first mechanism.
It is important to realize that the reject number increases if the R_{gen} of the D.U.T. increases while dV/dt remains unchanged.
In practice however, if the external circuit remains unchanged an increase of R_{gen} means:

- conduction of the current
- the operation of the D.U.T. in less dangerous conditions (fewer or no failures)
- a reduction of dV/dt

Photo 2 - The behaviour of a SGSP575 with $R_{gen} = 100\Omega$

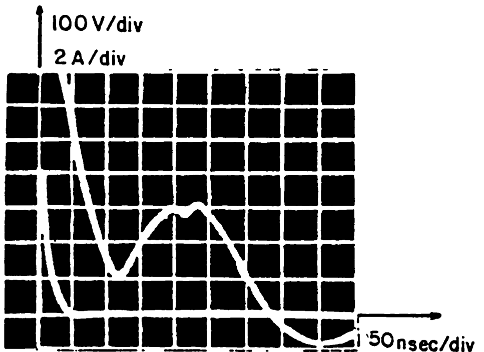
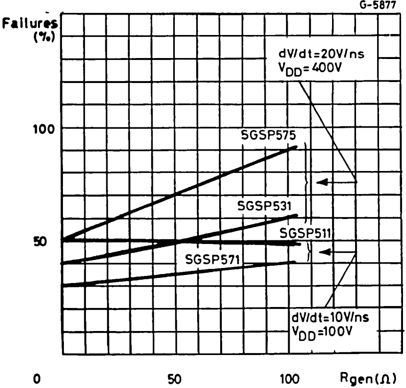


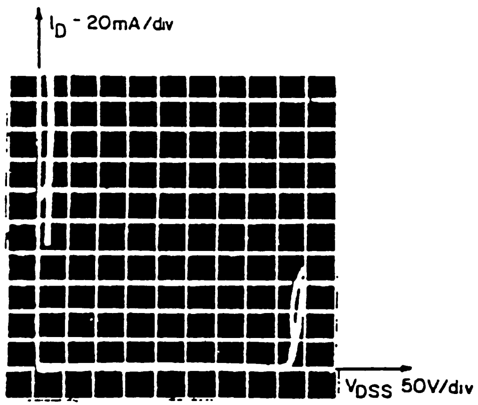
Fig. 6 - The test results obtained



APPENDIX

The breakdown of POWER MOS at high current values shows the phenomenon of "snap-back" which is also called secondary breakdown. This phenomenon is due to the effect of the parasitic bipolar transistor. A high current flow might make the voltage drop in the resistor R_p^+ so high that the parasitic bipolar transistor is turned on. This phenomenon is often catastrophic for the devices. The current value at which this phenomenon takes effect can give an idea of the R_p^+ value.

Fig. 3 - Snap-back characteristics



The tests give the important result that this current is not the same for similar devices, even if they are of the same type. This means the snap-back current is highly process dependent and does not depend on the design characteristics alone. The following results were obtained:

SGSP511	I snap-back	=	500-900mA
SGSP571	I snap-back	=	1.2A
SGSP531	I snap-back	=	50-200mA
SGSP575	I snap-back	=	250mA

These figures give the following R_{body} values:

	SGSP511	SGSP571	SGSP531	SGSP575
R_{body} (Ω)	0.93	< 0.54	5	< 2.6

from the formula:

$$R_{body} = \frac{0.65}{I \text{ snap-back}}$$

There is a good agreement with the theoretically estimated results.

CONCLUSION

The static dV/dt phenomenon is highly complex and affects POWER MOS devices both at a design level - reduction of the parasitic capacitances, - reduction of the R_{body} resistance, - minimization of the effect of the parasitic transistors etc.) and at a process level - reduction of the internal contact resistance etc.

Obviously the analysis was carried out on a limited number of devices, but it can give an idea on how the phenomenon originates and above all on the dV/dt order of magnitude needed to trigger it.

This order of magnitude was found to be at least 10 times greater than those in the most common applications or those which trigger the same phenomenon in SCR or in other similar devices.

However it can be expected that the phenomenon may give serious problems when using the device in some switching applications, especially with high impedance driving, eg. from integrated circuits.

COMPARISON OF SGS POWER MOS AND BIPOLAR POWER TRANSISTORS

It is highly predictable that in the near future SGS POWER MOS will, in many applications, gradually replace power bipolar devices due to the numerous advantages they offer.

Table 1 lists the principal differences between SGS POWER MOS and bipolar transistors. In addition to their inherent high switching speed resulting from the lack of minority carrier injection during operation, SGS POWER MOS with their insulated gates require negligible input gate-drive current. Other advantages are related to the negative temperature coefficient of their current, which prevents the formation of thermal instabilities and makes the paralleling of devices much more reliable. In contrast, bipolar transistors require ballasting or careful device matching to prevent thermal runway.

Only in high voltage cases is SGS POWER MOS on-resistance higher than in bipolar transistors.

This leads to slightly larger steady state power dissipation and could offset the advantages. The prospects for SGS POWER MOS appear bright in many high frequency applications where switching losses become very high for bipolar devices.

Table 1 - Comparison of MOS and bipolar power transistors

MOS	BIPOLAR
Majority-carrier device	Minority-carrier device
No charge-storage effects	Charge stored in the base and collector
High switching speed less temperature sensitive than bipolar devices	Low switching speed temperature sensitive
Drift current (fast process)	Diffusion current (slow process)
Voltage driven	Current driven
Purely capacitive input impedance; no dc current required	Low input impedance; dc current required
Simple drive circuitry	Complex drive circuitry (resulting from high base-current requirements)
Predominatly negative temperature coefficient of drain current	Positive temperature coefficient of collector current
No thermal runaway	Thermal runaway
Devices can be paralleled with some precautions	Devices cannot be easily paralleled because of V_{BE} matching problems and local current concentration
Less susceptible to second breakdown	Susceptible to second breakdown
Square-law I-V characteristics at low current; linear I-V features at high current	Exponential I-V characteristics
Greater linear operation and fewer harmonics	More intermodulation and cross-modulation products
High-on resistance and, therefore, larger conduction loss	Low on-resistance (low saturation voltage) because of conductivity modulation of high resistivity drift region
Drain current proportional to channel width	Collector current approximately proportional to emitter stripe length and area
Low transconductance	High transconductance
High breakdown voltage as the result of a lightly doped region of a channel-drain blocking junction.	High breakdown voltage as the result of a lightly doped region of a base collector blocking junction.

PERFORMANCE COMPARISON

At this point a comparison between SGS POWER MOS and bipolar devices can be made in order to evaluate their switching speeds which give an indication of the energy consumption during transitions, and their different values of $V_{DS(on)}$ and V_{CEsat} related to energy consumption during the on state.

The two devices used in the comparison are:

SGSP565: SGS POWER MOS; 400V; 6A
$R_{DS(on)} = 1\Omega$

SGSD00036: SGS BIPOLAR; 400V; 6A
(very fast switching)

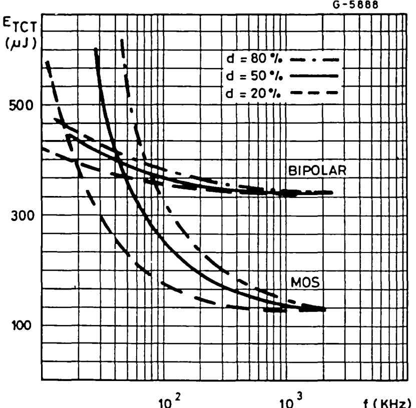
$V_{DD}/V_{CC} = 200V$
$I_L = 5A$ (average value)

Since the input losses were neglected the bipolar devices have an advantage in this comparison.

E_{TOT} (the energy losses per cycle) as a function of

the operation frequency, for different values of the duty cycle can be seen in Fig. 1. For a bipolar device, the energy used during the on phase has only a slight influence with frequency variation. SGS POWER MOS however are influenced by these variations, and as a result two curves, relative to the same duty cycle, are obtained. The intersecting points of these curves can be considered as a guideline to the use of the devices.

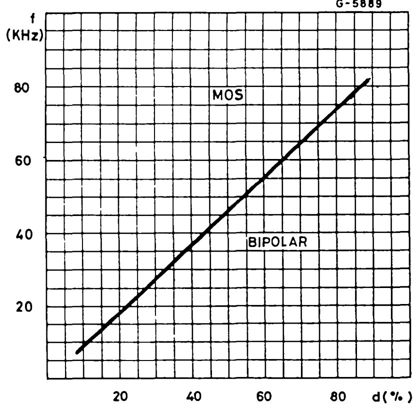
Fig. 1 - ETOT versus frequency (kHz)



In other words if both the duty cycle and the power to be switched are fixed there is a frequency value above which the dissipated energy per cycle for an SGS POWER MOS transistor is less than for a bipolar device. This means the higher the frequency the more advantageous it is to use a SGS POWER MOS.

Under relatively low frequency conditions the value of the duty cycle "d" is fundamental in determining the advantages of both bipolar and SGS POWER MOS technologies. From the graph in Fig. 2 the best working conditions for both devices can be seen.

Fig. 2

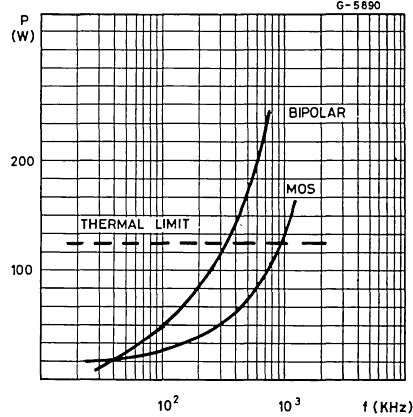


A SGS POWER MOS is most suited to high frequency conditions (> 100KHz) for any given value of "d". Maximum frequency limitations are of a thermal nature only and depend on the die size.

For the SGS POWER MOS under consideration the maximum power dissipated is 100W when $R_{th\,j\text{-}case} = 1°C/W$ and $T_{j\,max} = 150°C$.

By plotting the power dissipated as a function of the frequency, when d = 50% the actual limits of the two technologies can be seen (Fig. 3).

Fig. 3



THERMAL STABILITY

The greater thermal stability of SGS POWER MOS with respect to bipolar devices is essentially due to the different response that the two devices exhibit when they are subjected to external power pulses.

The intrinsic mechanism which could lead to thermal runway in a bipolar and in a SGS POWER MOS device, are as follows.

In a bipolar device an external power pulse results in an increase in the junction temperature (T_j). This causes V_{BE} to decrease and h_{FE} to increase. Both cause the collector current to increase and this consequently further increases T_j. This positive feedback is compensated only by the base widening effect at high currents (that is a higher recombination of the minority carriers). At high voltages the base widening effect is not present so that any hot spots lead to thermal runaway.

These phenomena, if not controlled, could seriously damage a bipolar device.

A power pulse in an SGS POWER MOS device would cause:

1) an increase in temperature of the device
2) a decrease in the threshold voltage

$$V_{GS(th)} = V_{GS(th)}\ (25°C) \times [1 - \alpha\,(T_j - 25°C)]$$

where alpha is a positive coefficient of temperature ($\alpha = 2.10^{-3}\ °C^{-1}$).

This is positive feedback, similar to a decrease of V_{BE} in bipolar devices.

But in a SGS POWER MOS device there is also a very important negative feedback. That is an increase of $R_{DS(on)}$ with temperature:

$$R_{DS(on)}(T) = R_{DS(on)}(25°C) \times$$
$$\times [1 + \alpha(T-25°C)]$$

where alpha 'is the temperature coefficient (alpha $= 8 \cdot 10^{-3}$ $°C^{-1}$). The effect of a increase in $R_{DS(on)}$ is greater than the variation in $V_{GS(th)}$. As a result SGS POWER MOS devices are thermally stable. The difference in behaviour of the two devices is even more exaggerated when dealing with paralleled chips.

Two comparisons between bipolar and SGS POWER MOS devices have been made.

The first deals with the behaviour of single chips in SOT-93 (TO-218) package.

The SGS POWER MOS used in this test is the SGSP475 (400V, 12A, 0.55Ω).

The power bipolar device used in the BUV48 (400A, 10A).

The parameter used to measure the thermal unbalance of the devices is the variation of the thermal resistance $R_{thj-case}$ due to an external power pulse.

In fact an increase of $R_{thj-case}$ implies a decrease of the active area of the chip and therefore a disuniformity in the spreading of the heat, with a creation of hot spot and thermal and electrical unbalancing. The devices have been tested under several conditions, with respect to the power dissipation and the voltage across them (V_{DS} for SGSP471, V_{CE} for BUV48). The results are shown in Fig. 4 and Fig. 5).

SGSP475 shows optimum thermal stability under all conditions while bipolars, with $V_{CE} = 45V$ and $P > 45W$, show a degrading of the thermal performances.

The best electrical and thermal performances of the SGS POWER MOS are confirmed by the thermal maps which show a uniform distribution of heat under different working conditions (Fig. 6 and 7).

Fig. 4 - Variation of $R_{thj-case}$ vs. P (POWER MOS) SGSP475 SOT-93

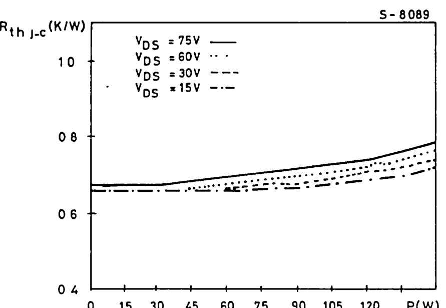


Fig. 5 - Variation of $R_{thj-case}$ vs. P (BIPOLAR) BUV48 SOT-93

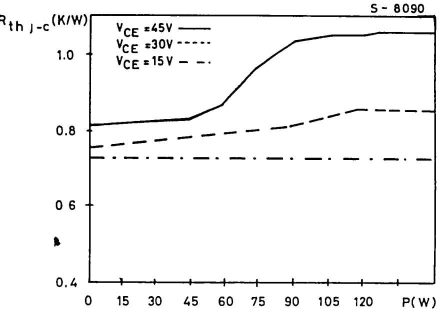


Fig. 6

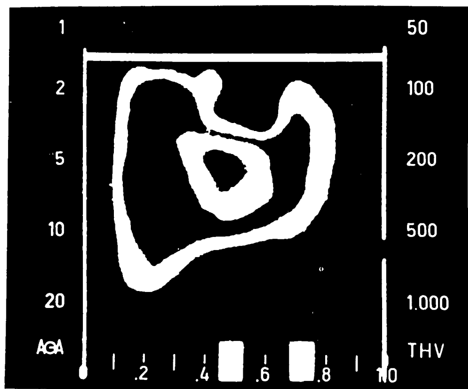
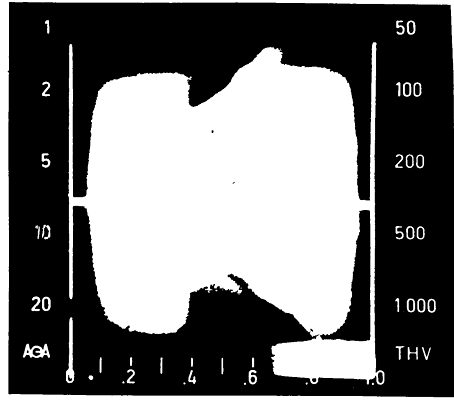


Fig. 7



It is only at $V_{DS} = 75V$ that is it possible to notice a slight variation in the working temperature.

The thermal instability has a greater effect when the die are assembled in parallel since any unconformity would be enhanced leading to an overloading of some of the die.

The second thermal comparison was made between SGS POWER MOS and bipolar devices in multiple chips mounted in a parallel configuration.

The SGS POWER MOS device under test was:

SGS30MA050D1: four SGS POWER MOS chips paralleled in TO-240 a package I_{DMAX} = 30A, V_{DSS} = 500V, $R_{DS(on)}$ = 0.250Ω

The bipolar device under test was:

SGS40TA045D: four bipolar chips paralleled in TO-240 package I_C = 40A, V_{CEO} = 450V

The results are shown in Fig. 8 and 9 and reveal a much better thermal stability for the SGS POWER MOS than for the bipolar device.

Fig. 8 - Variation of $R_{thj\text{-}case}$ vs. P (POWER MOS) SGS30MA050D TO-240

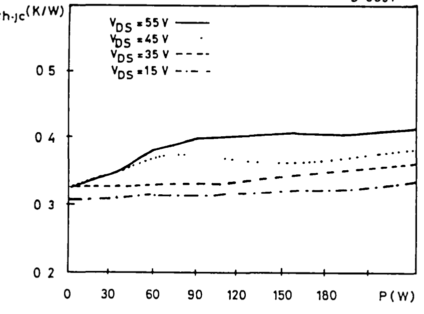
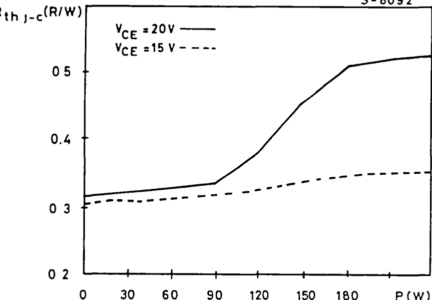


Fig. 9 - Variation of $R_{thj\text{-}case}$ vs. P (BIPOLAR) SGS400TA045D TO-240



HIGH VOLTAGE TRANSISTORS WITH POWER MOS EMITTER SWITCHING

INTRODUCTION

This paper summarizes the results of an investigation carried out on power devices with both MOS and BIPOLAR parts working together in the same circuit. The "emitter drive" configuration was considered, with switching power supply applications in mind.

The devices used are:

Power MOS:	SGSP321, SGSP352
Bipolar transistors:	BUV48, BU508A
Ultrafast bipolar transistors:	SGSD00035,
(Hollow Emitter)	SGSD00039
Fast darlingtons:	SGSD00031, BU810

In the case of flyback switching power supplies a practical example is also described.

CIRCUIT DESCRIPTION

The term "emitter switching" describes a circuit configuration where a low voltage transistor (MOS or Bipolar) switches off the emitter current of a high voltage transistor, and consequently the transistor itself.

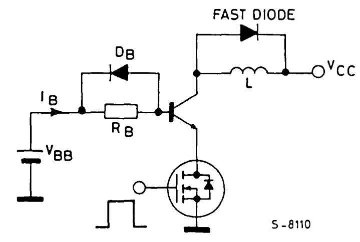
This configuration combines the fast switching of a low voltage device with the high power switching of a high voltage device, since:

high current x high voltage = high power switching.

The combination of a high voltage bipolar and a low voltage Power MOS is preferable due to the high switching speed and the low driving energy of the combined power switch.

The base of the high voltage bipolar device is driven by a constant voltage source. The energy dissipated to drive the high voltage bipolar device depends on the losses that the forward bias current I_{B1} generates in the resistance in series with R_B, $I_{B1}^2 \cdot R_B \cdot t$. This power dissipation can only be reduced by using high gain transistors of darlingtons. (See Fig. 1)

Fig. 1 - The basic circuit used for the evaluation of the emitter switching system. The base drive circuit used is shown for comparison



The diode in series with the base serves to clamp the base overvoltage at turn-off.

The two transistor stage is driven by the gate of the low voltage Power MOS. Very low driving energies, about 180nJ per cycle, are involved in the charging and discharging of the input capacitances.

Consequently the stage can be directly driven by the output of suitable linear integrated circuits.

The possibility of direct driving by an IC output together with the excellent switching speed make this configuration extremely suitable for switching power supplies at frequencies of 50KHz or even higher.

CIRCUIT OPERATION

As we have seen, the forward base current I_{B1} is fixed by the external circuitry:

$$I_{B1} = \frac{V_{BB} - V_{BEsat} - V_{DSon}}{R_B}$$

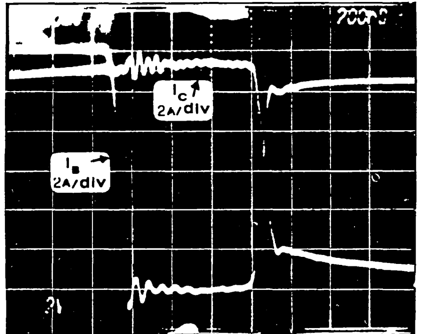
The collector current instead depends on the load, and in general, varies with the time.

The turn-on and turn-off phases can be analyzed separately.

TURN-OFF

When the driving signal to the Power MOS is low the drain current is interrupted and the emitter current of the high voltage bipolar falls to zero. The emitter reaches the base voltage and won't carry any more current. As a result the collector current can only flow through the base, becoming a reverse base current that depletes the base to collector junction. This reverse base current I_{B2}, from the moment when the emitter current disappears, coincides with the collector current. See photo 1. The stored charge is removed in a typically very violent, and consequently rapid manner.

Photo 1 - Base and collector current at turn-off



As a result the storage time is substabtially reduced. The fall time, which is related to the recombination under the emitter, is also generally reduced.

Typical values for the fall and storage time of the SGS devices used in the test are shown in Table 1, for both emitter and the base drive circuits.

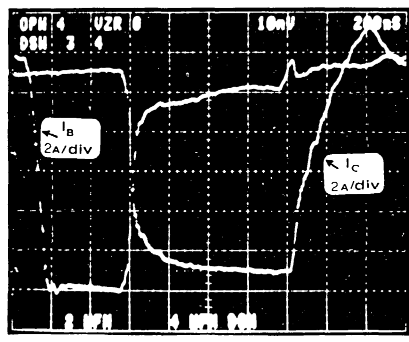
Table 1 - Typical t_f and t_s on inductive load

Device	IC(A)	EMITTER SWITCHING		BASE SWITCHING	
		tstorage	tfall	tstorage	tfall
BUX48	10	500ns	100ns	2µs	200ns
BU508A	5	800ns	300ns	6µs	400ns
SGSD00031	10	400ns	100ns	1.2µs	100ns
BU810	5	300ns	150ns	800ns	150ns
SGSD00035	10	300ns	50ns	800ns	50ns
SGSD00039	5	300ns	40ns	700ns	50ns

TURN-ON

When the Power MOS is in the ON state, the bipolar device also starts conducting. The dynamic behaviour (See Photo 2) does not differ in any substantial way from the usual case of the base drive.

Photo 2 - Base and collector current at turn-on



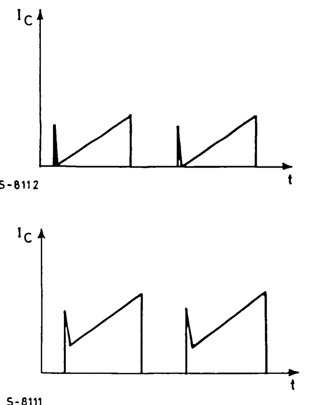
The dynamic saturation transient $V_{CEsat\,dyn}$ is also practically the same with a base drive as with an emitter drive. The collector current, when the collector load is the primary winding of a switching transformer, can vary according to two possibilities. (See Fig. 2)

a) After the initial peak due to the recovery of the diode present on the secondary winding, the collector current increases linearly starting from zero

b) After the same initial peak, the collector cur-

rent increases linearly starting from the value memorized in the magnetic circuit at the end of the previous cycle.

Fig. 2 - Collector current waveforms with varying load



REVERSE BIAS SAFE OPERATING AREA

A problem that occurs in bipolar transistors is damage caused by "current crowding".

Fig. 3a illustrates current flowing in a typical bipolar device. Fig. 3b shows how, when the device is turned off and the current begins to die away, the current focuses with a high concentration under the emitter. This high current density can damage or destroy the transistor.

Fig. 3a

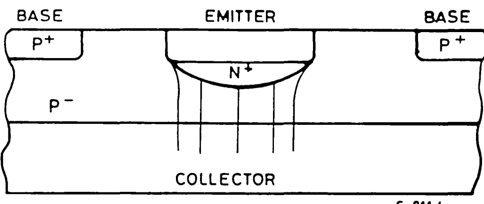


Fig. 3b -

BASE EMITTER BASE P+ P+ N+ P− COLLECTOR S-8114

The energy dissipated within a bipolar power transistor at turn-off can be found graphically from a plot of I_C versus V_{CE} at turn-off. Three cases are shown in Figures 4a, b and c. The shaded area is proportional to the energy that is dissipated in the device during turn-off.

Fig. 4a - Slow turn-off. No crowding but high average heating

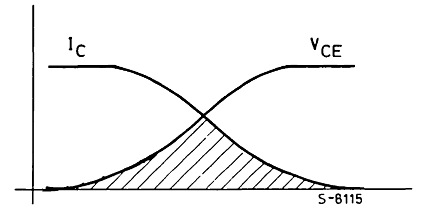


Fig. 4b - Fast turn-off. Crowding with low average heating but possible high peak power

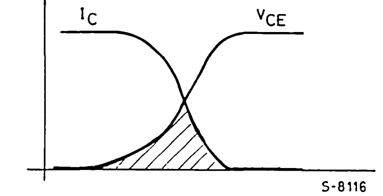
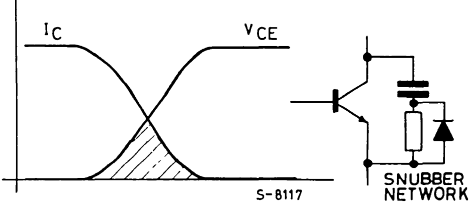


Fig. 4c - Fast turn-off (with V_{CE} delayed by snubber network)



Consequently turn-off times affect the SOA of the device, (Fig. 5b). These problems can be overcome using emitter switching.

The way the stored charge is swept away in the high voltage bipolar device when it is driven by the emitter, produces some interesting consequences.

The stored charges are evacuated through the base contact when the emitter current is zeroed and not later than a few tens of ns after the beginning of the storage interval. Consequently, during the turn-off, no charge is injected from the emitter into the base. Although the reverse base current is quite relevant, no focusing of the current in the centre of the emitter fingers takes place.

The bipolar device therefore exhibits an energy absorbing ability at the turn-off RBSOA that is substantially higher than if a normal base drive were used. With a base drive the emitter would inject charges and the voltage drop across the distributed base resistence would induce the "emitter crowding" phenomenon.

The practical evidence for all the transistors investigated (BUV48, BU508A, SGSD00035, SGSD00039) shows that the reverse bias safe operating area (RBSOA) extends right up to the BV_{CES}! (See fig. 5)

This extreme effect is unfortunately much less pronunced when using fast darlingtons. The higher complexity of the charge extraction mechanism and the charge injection from the emitter into the base in the driver transistor imply that the RBSOA extension is almost irrelevant.

Fig. 5a - Reverse bias safe operating area

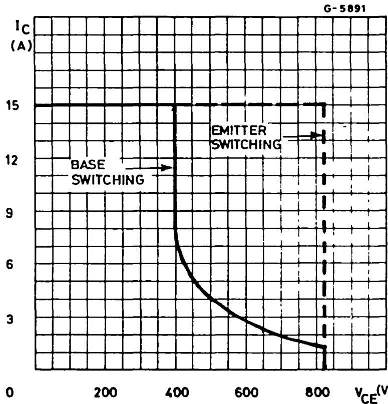
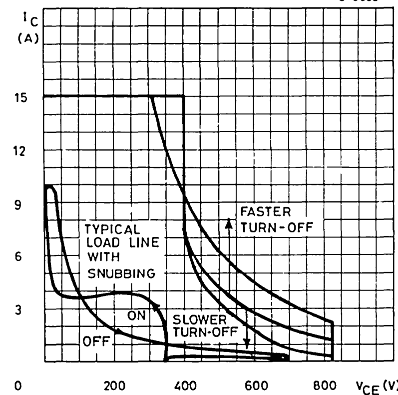


Fig. 5b - How reverse bias safe operating area changes for:
i) slow turn-off
ii) fast turn-off



A POSSIBLE APPLICATION

A possible application of the "emitter switching" configuration is shown in Figure 6, where a switching power supply operating in a "flyback" mode has been implemented.

The basic criteria used in choosing the values of the circuit elements are given below. The purpose of the study was to demostrate the feasibility and to evaluate the advantages. Exact circuit element values can be further optimized, especially in the case of the transformer.

The power source is the mains singlephase, 220V a.c.), and the switching frequency can be set to 50KHz or more.

The devices used were:

Q1: Fast darlingtons with $BV_{CES} \geqslant 600V$ for 110V line
- SGS BU810 for current up to 5A
- SGSD00031 for current above 5A

Fast transistor with $BV_{CES} \geqslant 800V$ for 220V line
- SGSD00039 for currents up to 5A
- SGSD00035 for currents up to 10A

Q2: Low voltage POWER MOS (BV_{DSS}=50V)
- SGSP352 for currents up to 5A
- SGSP322 for currents above 5A

Q3: High voltage, low current POWER MOS ($BV_{DSS} < = 450V$)
- SGSP354

Control IC: SGS UC3842

DZ2: Zener diode 2W/20V

D1: 25V diode, with I_c peak rating as high as 10A for 500ns

C6: Electrolytic capacitor, 1000µF, 25V. It absorbs possible variations of V_{BB}.

R3: Resistor setting the forward bias base current of the darlington:

$$R3 = \frac{V_{CE} - V_{BEsat} - V_{DSon} - R7\, I_D}{I_{B1}}$$

Its power rating must exceed $R3 \cdot I_B^2 \cdot t$ (in practice 3W)

R7: Shunt resistor to sense the switch current. The over current I_{Smax} protection is set according to

$$R7 = \frac{1V}{I_{Smax}}$$

C4, R6: RC network, filtering the disturbances induced by the switching transients on the I_{Smax} protection input.

C3, R5: RC network, setting the switching frequency and the maximum duty cycle, according to the UC3842 data sheet.

$t_{charge} = 0.55\ R_5\ C_3$
$t_{discharge} = R_5 \times C_3\ \ln\ [(6.3\ R_5 - 2.7)/6.3\ R_5 - 4)]$
$f = 1/(t_c + t_d)$

R8, R9: Resistive divider, of the feedback voltage, from a secondary sense winding, rectified by D5 and C5. The divided voltage is compared by the control IC to an interval reference of 2.5V.

C2, R4: Compensating network in the error amplifier of the feed-back voltage.

R1: Resistor biasing the Q3 gate (1.2MΩ, 1/4W)

R2: Resistor that limits the inrush current through the POWER MOS Q3 at the turn-on (1.2KΩ, 2W)

D4: Fast recovery diode
Its voltage/current ratings depend on the particular secondary winding it rectifies.

D5: Low current/low voltage diode

D3, R10, C8: Snubber network (Fig. 6 shows just one of the possible configurations).

$$C8 = \frac{L_d\ I_c^2}{V_{os}^2}$$

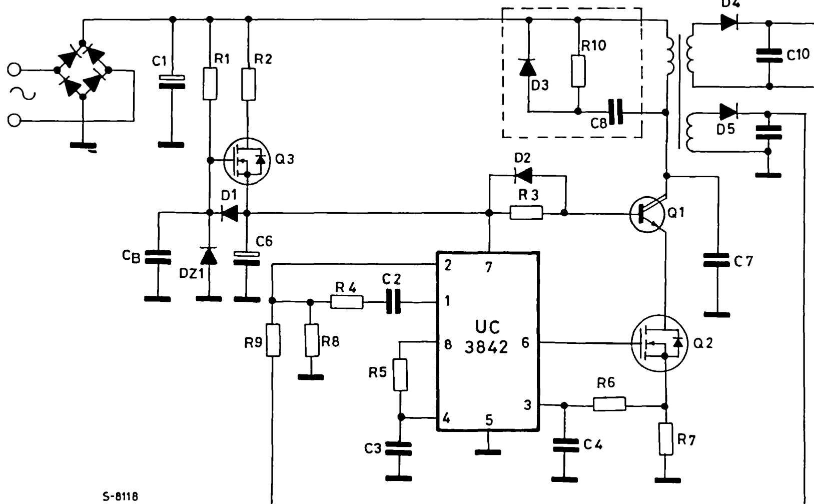
$R10 = 1/4fC8$
$P\ (R_{10}) = 1/2\ L_d\ I_d^2 f$

where:

f = switching frequency
L_d = stray inductance of the transformer
V_{os} = maximum voltage overshoot admitted
D_3: is a 400V fast recovery diode
C_7: Possible capacitor reduces the cross-over of the Darlington (3 to 6nF)

It is important to note that, the power transistor Q3 acts only at the turn-on of the power supply and when the capacitor C6 supplies more energy to the base of the darlington and to the supply input of the IC than is returned to C6 during the turn-off of the darlington, Q1.

Fig. 6 - "Emitter switching" circuit



CONCLUSION

The "emitter drive" configuration exhibits some clear differences with respect to the usual "base drive" configuration, and they can be particularly useful in switching power supply applications:

– Substantial reduction of the storage time and improvement of the fall time

Switching frequencies of 50KHz and higher are possible

– The dynamic drive circuitry is simplified. The negative voltage supply is not required to remove the stored charge from the base. The energy needed to drive the gate of the POWER MOS is very low (180nJ per cycle).

– Extremely high ruggedness at the turn-off of the inductive load (i.e. very large RBSOA) if the high voltage bipolar part is a transistor.

– Higher power dissipation in the on-stage, due to the additional losses in the POWER MOS ($I_D^2\ R_{DSon}\ t_{on}$)

This last point is the only disadvantage, but it is more than compensated for if switching at high frequencies. The lower switching losses (a saving each cycle) can justify the higher on-state losses (a fixed expenditure) as soon as the switching frequency is high enough, which is often the case in switching power supplies.

SGS POWER MOS:
SUGGESTIONS ON HOW TO PROTECT POWER MOS IN SMPS APPLICATIONS

The rapid growth in the power supply market has led to a new generation of power supplies - **switch mode power supplies** (SMPS). This in turn requires critical selection of power devices to give improved efficiency and reliability. A switching device for SMPS must possess the following characteristics:

- HIGH VOLTAGE BREAKDOWN CAPABILITY TO WITHSTAND TRANSIENTS AND THE MAXIMUM PEAK REVERSE VOLTAGE
- FAST SWITCHING TIMES TO MINIMIZE TRANSIENT SWITCHING POWER DISSIPATION
- LOW SATURATION VOLTAGE TO MINIMIZE STATIC POWER DISSIPATION
- RUGGED - ABLE TO WITHSTAND ADVERSE BIAS CONDITIONS

Many manufactures of power supplies have been recently evaluating the use of POWER MOS because they represent a good choice for SMPS. They offer: simplified drive circuitry, higher operating frequencies and enable the size of magnetic components to be reduced.

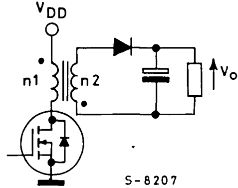
In order to evaluate the main features of POWER MOS and BIPOLAR devices, some qualitative comparisons are shown in table 1.

TABLE 1

PARAMETER	BIPOLAR	POWER MOS
$V_{(BR)DSS}$ BV_{CES}	up to 1000V	up to 550V
t_{fall}	up to 200ns temperature sensitive	up to 30ns not very temp. sensitive
Ability to withstand operation in second breakdown	fairly tolerant	high ruggedness
Driving power	high	low
Operating frequencies	up to 50KHz	up to 200KHz

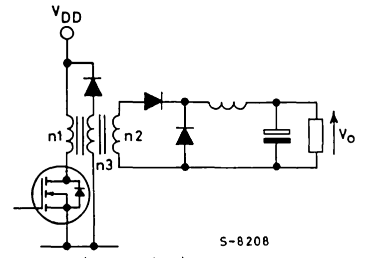
From table 1 it is evident that POWER MOS SMPS are highly suitable for the low and medium voltage ranges. Fig. 1-4 show some popular configurations and their voltage ratings.

Fig. 1 - Flyback converter



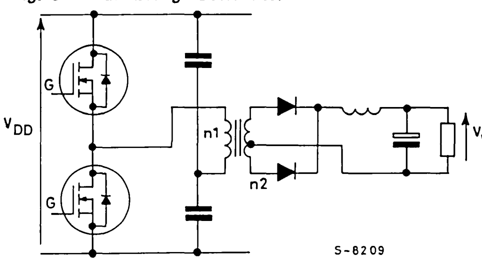
$V_{DS} = V_{CC} + n1/n2\ V_o$

Fig. 2 - Forward converter



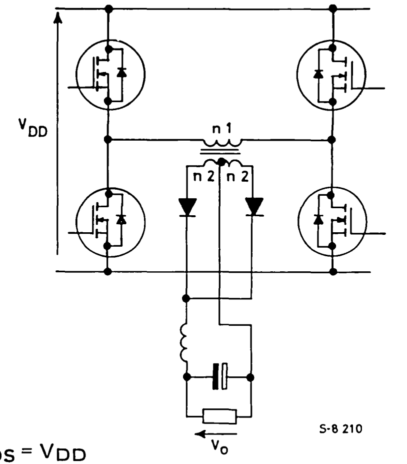
$V_{DS} = V_{DD}\ (1 + n1/n2)$

Fig. 3 - Half bridge converter



$V_{DS} = V_{DD}$

Fig. 4 - Full bridge converter



$V_{DS} = V_{DD}$

Flyback is the most useful configuration in a switching power supply handling up to 150W. It is possible to use POWER MOS devices in this configuration up to V_{DSS} equal to 200V. In the USA the line voltage level (110V) allows the design of SMPS from the line voltage while elsewhere flyback converters using POWER MOS are limited to low and medium voltages.

Despite this limitation, the use of POWER MOS in the low and medium voltage ranges is increasing rapidly so an accurate evaluation of the performance and reliability of these systems using POWER MOS is necessary.

POWER MOS are very rugged in forward mode operation, they can handle high currents without problems. The only problem area is during turn-off. At this point I_D changes abruptly and the slope $(di/dt)_{off}$ is very steep. This sharp rate of change of current with time creates ringing and spikes with amplitudes that can exceed the maximum ratings of the device. This creates a potential problem as POWER MOS are sensitive to voltage variations.

Particularly:

- **POWER MOS ARE OFTEN DESTROYED WHEN THEIR BREAKDOWN VOLTAGE IS EXCEEDED**
- **THE BREAKDOWN VOLTAGE DISTRIBUTION OF POWER MOS HAS A VERY LOW STATISTICAL SPREAD COMPARED TO THAT OF BIPOLAR TRANSISTORS**
- **IT IS VERY RISKY TO DESIGN SMPS WHICH OPERATE AT THE LIMITS OF THE RBSOA**

It is therefore necessary to protect them more carefully if we want to increase system reliability.

Safe operating area - a discussion

The circuit shown in fig. 5 is used to characterize the ruggedness of POWER MOS during turn-off. The V_{DS} maximum voltage is controlled by the diode and the V_{clamp}.

- **the diode forward voltage is very low.**
- **the diode is physically near to POWER MOS drain to minimize layout inductance.**

$V_{DSmax} = V_{fp} + V_{clamp}$

The V_{DS} and I_D waveforms for a POWER MOS SMPS are shown in fig. 6. If the V_{DS} voltage spikes increase above the $V_{(BR)DSS}$ rating the device will be destroyed.

In this application spikes and ringing can often occur due to non-optimized layout.

To protect POWER MOS it is common to use particular devices.

Table 2 compares the common protection devices; it can be seen that some devices are not suitable to protect the POWER MOS.

In the following note we propose to show the most serious stresses and give some suggestions of protection.

Fig. 5 -

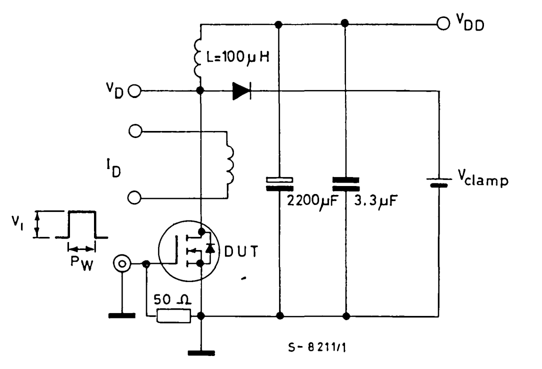


Fig. 6 -

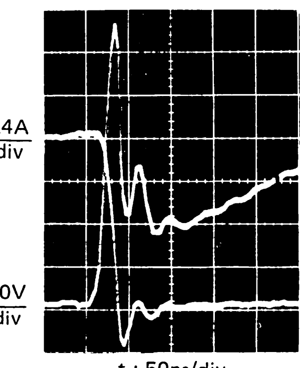


TABLE 2

DEVICE	MOV	ZENER	TVS
RANGE OF VOLTAGE	12-4700	3-200	4-400
VOLTAGE INCREMENTS	10 - 25%	5 - 10%	10%
TOLERANCE	10%	5%	5%
CLAMP RATIO @ 10A	1.85 (13J)	1.65	1.25 (15J)
CAPACITANCE	150pF	30pF	1.2pF
PRICE	MEDIUM	LOW	MEDIUM
STEADY STATE POWER DISSIPATION CAPABILITY	VERY LOW 1/2W FOR 10J DEVICE	GOOD TO 50W	GOOD TO 10W
FAILURE MODE	GRADUAL SHIFT IN BREAKDOWN	OPEN OR SHORT CIRCUIT	SHORT CIRCUIT
PROPERTIES	GOOD FOR MAINS USE, NOT SUITABLE POWER MOS PROTECTION	NO SPEC FOR TRANSIENT USE	IDEAL FOR SMPS

CIRCUIT DESCRIPTION

This analysis deals with SMPS in flyback configuration, shown in fig. 7, which is the most common SMPS configuration. The suggested protection procedures can be employed in other configurations as well.

When the POWER MOS is 'on', energy is stored in the primary coil of the transformer; in the 'off' state this energy is transferred to the secondary coil and is available for the load.

The pulse width of V_{GS} is varied in response to the voltage across the load to achieve regulation.

The V_{DS} and I_D waveforms are shown in fig. 8.

In the 'on' phase the drain current increases with a slope, which depends only on the inductance of the primary coil, because the secondary circuitry is open (diode not conducting): in this phase the energy is stored in the primary coil.

When the POWER MOS turns off the energy is transferred to the secondary coil and V_{DS} increases until it reaches the value:

$V_{LOAD}/n + V_{DD}$

where n is the turns ratio of the transformer.

Although this phenomenon acts as a clamp it cannot be used to proctect POWER MOS as this clamp value strictly depends on the load, which can accidentally be disconnected or shorted. Also, voltage spikes and ringing can cause voltage that exceed the maximum voltage ratings and can damage the POWER MOS device.

In addition a high dV_{DS}/dt can also destroy the POWER MOS (ref. static dV/dt in POWER MOS).

Therefore some form of protective network is required in order to protect POWER MOS devices from being subjected to these conditions.

Fig. 7 -

S-8212 PROTECTION NETWORK

Fig. 8 -

V_{DS}: 20V/div

I_D: 0.2A/div

t (5µs/div)

R C D (SNUBBER) NETWORK DESIGN FOR PROTECTION AGAINST dV_{DS}/dt

Switching times are very short in POWER MOS operations and they can cause rapid rate of change of voltage with time. (dV_{DS}/dt) in the device. This phenomenon can damage the device and can be avoided by a protection network (see fig. 7), which is analyzed below.

The most critical phase is in the POWER MOS turn off and the proposed network acts as follows.

In the off phase the capacitor C_{PN} of fig. 7 stores part of the energy of the leakage inductance that cannot be transferred to the secondary coil; the voltage V_{DS} increases more slowly.

The capacitor is rated according to the desired dV_{DS}/dt.

The waveforms of I_D, V_{DS} and I_C can be described by the following formulas which are relate to figs. 9, 10 and 11.

(1) $I_D = I_{D(end)} \times (1 - t/t_f)$ for $0 < t < t_f$
$I_D = 0$ for $t > t_f$
t = instantaneous value of time
t_f = fall time
$I_{D(end)}$ = current before I_D turn-off
I_C = current through C_{PN}
C_{PN} = capacitance of C_{PN}

(2) $I_C = I_{D(end)} \times t/t_f$ for $0 < t < t_f$
$I_C = I_{D(end)}$ for $t > t_f$

(3) $V_{DS} = I_{D(end)} \times t^2/(2\, t_f\, C)$ for $0 < t < t_f$
$V_{DS} = I_{D(end)} \times (t - t_f/2)/C$ for $t > t_f$

From equation (3) it follows that:

$$(4) \quad \left(\frac{dV_{DS}}{dt}\right)_{t = t_f} = \frac{I_{D(end)}}{C}$$

Although (1) and (2) are sufficiently valid in practice (see fig. 12) expression (4) applies only if C is much greater than the equivalent C_{DS} of the POWER MOS.

Fig. 9 -

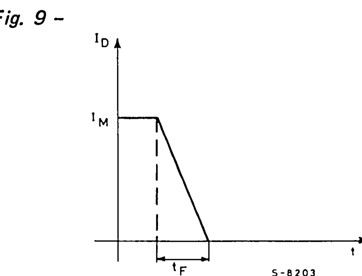
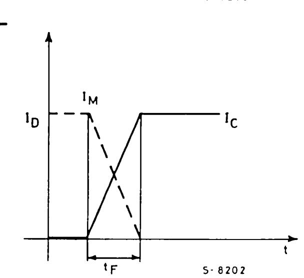


Fig. 10 -



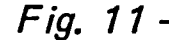


Fig. 11 -

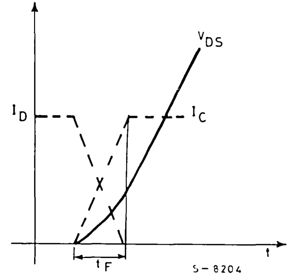
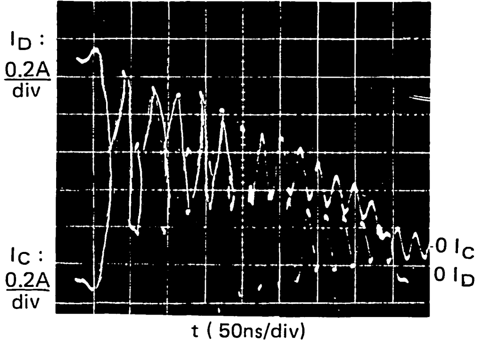


Fig. 12 - Complementary behaviour of I_D and I_C currents



Expression (5) can always be used for design purposes.

$$\left(\frac{dV_{DS}}{dt}\right)_{t = tf} < \frac{I_{D(end)}}{C} \qquad (5)$$

Expression (4) holds if the value C also includes the equivalent capacities of the POWER MOS from drain to source.

(6) $C = C_{DS} + C_{PN}$

The following expression can be used to calculate C_{DS}.

(7) $C_{DS} = I_{D(end)} / (dV_{DS}/dt)_o$

where $(dV_{DS}/dt)_o$ is that without protection network.

Using formulas (6) (7), expression (4) can be rewritten

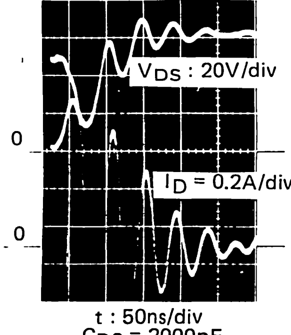
$$\frac{dV_{DS}}{dt} = \frac{I_{D(end)}}{C_{PN}} + \left(\frac{dV_{DS}}{dt}\right)_o \qquad (8)$$

The formula has been verified with different capacitor values in the protection network (see figs. 13, 14).

The resistor R of fig. 7 has a value that takes into account the fact that in the on phase the capacitor must discharge with a peak current which depends on the I_{Dmax} of the device and a time constant which depends on the t_{ON} time duration and the I_{Dmax} of the device.

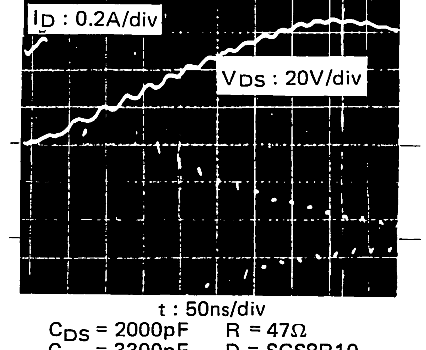
In practice the resistor and the diode can be removed because in the on phase the POWER MOS can easily handle high peak currents.

Fig. 13 - V_{DS} and I_D shapes in the turn-off phase without RCD network



t : 50ns/div
C_{DS} = 2000pF

Fig. 14 - V_{DS} and I_D shapes in the turn-off phase with RCD network



t : 50ns/div
C_{DS} = 2000pF R = 47Ω
C_{PN} = 3300pF D = SGS8R10

V_{DS} VOLTAGE OVERSHOOT

POWER MOS reliability strictly depends on the V_{DS} maximum value which must no exceed the $V_{(BR)DSS}$ of the device.

This may occur when the leakage inductance of the transformer (primary coil) is not a negligible amount and the layout inductance is not properly minimized.

In order to emphasize this condition a transformer with the following characteristics was made:

- L_{D1} = 2μH
- L_{D2} = 258μH
- L_S = 4.64mH
- L_P = 30μH

In addition a high operating frequency (60KHz) was chosen and layout inductance was introduced. In fig. 15 V_{DS} and I_D waveforms are shown in the turn-off phase; it should be noted the initial V_{DS} spike due to the extremely low t_f and I_D and the high value of the total leakage inductance. In fig. 16 the relative V_{DS} - I_D locus for a SGSP351 device is shown.

Fig. 15 -

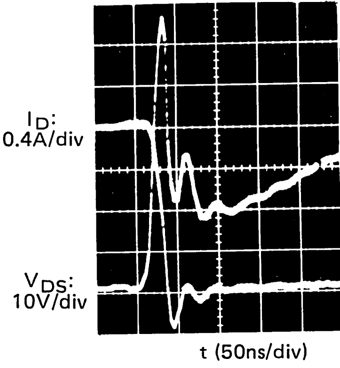
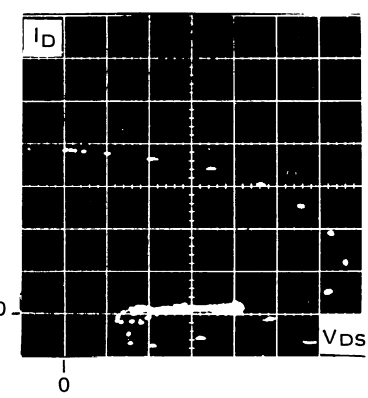


Fig. 16 -



In order to prevent this effect some specific suggestions can be considered, such as:

1) minimize the interconnection wiring of the primary circuitry.
2) choose the proper capacitor C_{PN} (fig. 7) and put is as near as possible to the primary circuitry.
3) minimize the leakage inductance of the transformer primary coil.
4) increase, if it is practicable for the application, t_f by increasing the discharge time constant of the gate course capacitance.

Fig. 17 shows the V_{DS} - I_D locus of the device in the turn off phase with the layout inductance reduced at minimum.

Fig. 18 shows the V_{DS} - I_D locus in the turn off phase of an SGSP351 device when t_f is increased by adding a 9300pF capacitor in parallel to the gate source intrinsic capacitor.

The behaviour of t_f with respect to the discharge time constant of the equivalent gate to source capacitance is shown in fig. 19.

Fig. 17 - V_{DS} - I_D locus of SGSP351 type

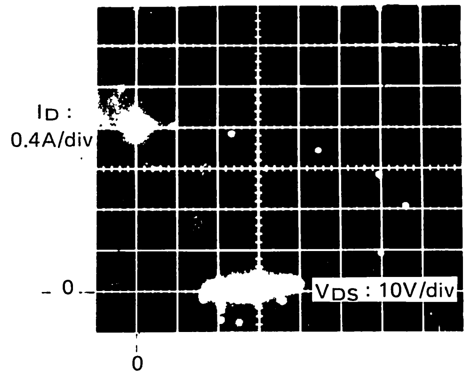


Fig. 18 - V_{DS} - I_D locus of SGSP351 type with a 9300pF capacitor between gate and source

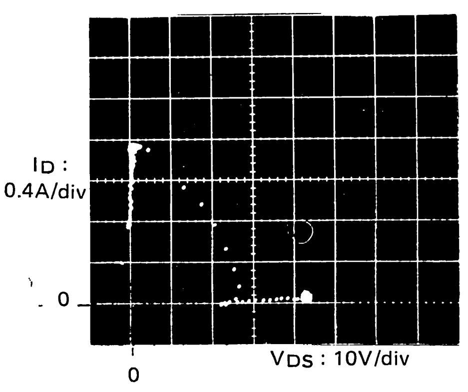
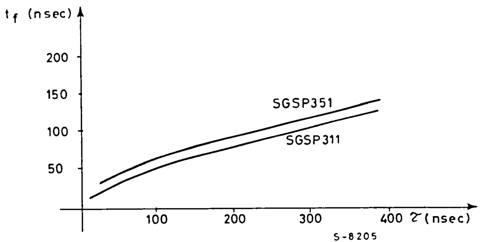


Fig. 19 - t_f variation vs. discharge time constant of the intrinsic gate source capacitor



SYSTEM START-UP

Two of the most critical states for SMPS are:

1) the system start-up

and:

2) accidental short circuit of the output.

Both these conditions submit the devices to similar stresses.

Fig. 20 –

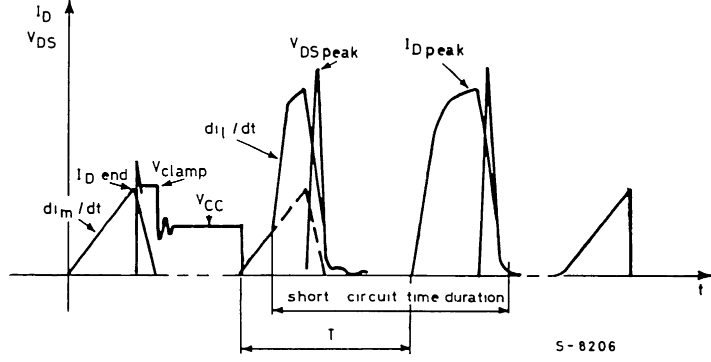


Fig. 20 shows what happens qualitatively when a short circuit produced in the SMPS output. It can be seen that:

1) the current increases until it reaches I_{Dmax} which depends on V_{GS} and the relative transfer of the device.
2) the V_{DS} peak increases due to increased energy stored in the leakage inductance.

In order to protect the devices and permit short circuit analysis the V_{GS} voltage is reduced as specified below.

Fig. 21 shows the V_{DS} - I_D locus for SGSP311 type in normal and in output short circuit operations with V_{GS} = 5V.

Fig. 21 – V_{DS} – I_D locus of SGSP311 type

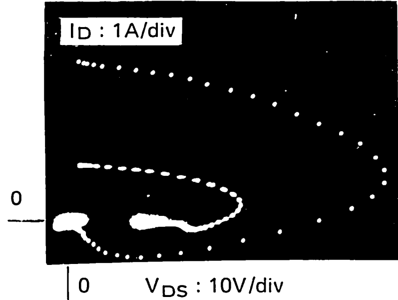
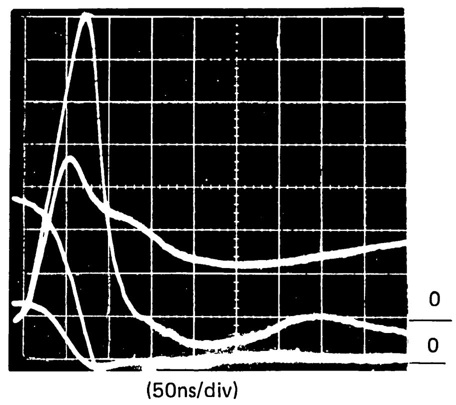


Fig. 23 shows the V_{DS} - I_D locus of the SGSP351 type in the turn off phase in short circuit operation with V_{GS} = 5V.

It is important to note that the SGSP351 reaches a greater V_{DSmax} with a lower I_{Dmax} because its t_f is lower.

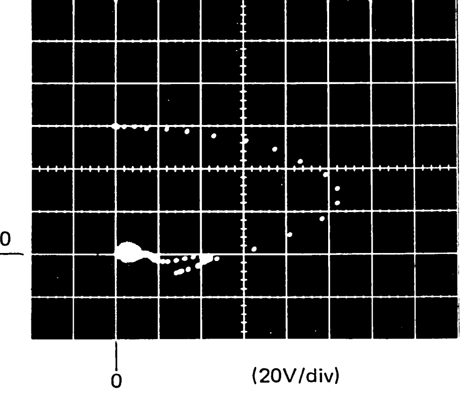
The same test performed on an SGSP311 device with V_{GS} = 4V is illustrated in fig. 24 and 25. It shows a more limited V_{DS} - I_D locus.

Fig. 22 – V_{DS} and I_D shapes for SGSP311 type



(50ns/div)

Fig. 23



(20V/div)

Fig. 24 - V_{DS} - I_D locus of SGSP311 type during short circuit with V_{GS} = 4V

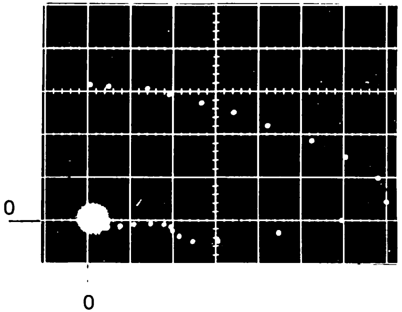


Fig. 27 -

A/div
V/div
t (50ns/div)

Fig. 25 - V_{DS} and I_D shapes vs. time in short circuit operation

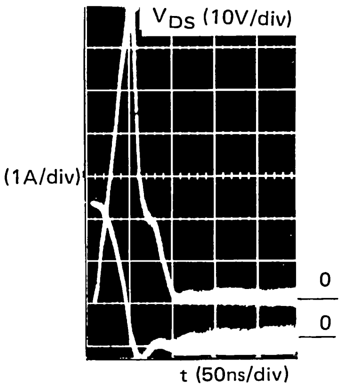
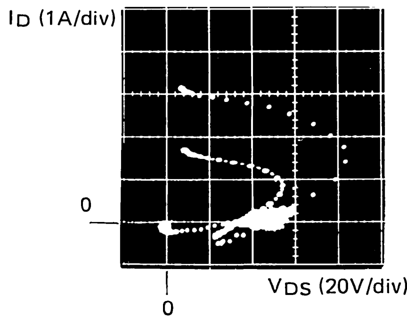


Fig. 26 -



This shows that die size and the V_{GS} voltage play an important role in the stresses that occur in SMPS during start-up and under output circuit conditions.

Fortunately these effects can be avoided by choosing the proper capacitor value between drain and source. In this way this capacitor performs two functions:

- reducing dV_{DS}/dt
- overload protection

Fig. 26 and 27 how V_{DS} - I_D locus of the SGSP311 in short circuit and normal operations with a 3300pF capacitor between drain and source.

CONCLUSION

This note shows how vulnerable POWER MOS devices are if the $V_{(BR)DSS}$ voltage rating are exceeded and a high dV_{DSS}/dt is generated.

The dV_{DS}/dt analysis in this note is quantitatively correct and it provides good agreement between theoretical and practical results.

Accidental overload and short circuit analysis high light one of the most important causes of failure. The protection criteria must be evaluated using the particular environmental conditions leakage inductances, transformer parameters, driving circuitry).

The protective suggestions analyzed are not conclusive because the design engineer cannot always optimize the environmental conditions. Therefore, if the application is critical, the use of the protective devices listed in table 2 is necessary.

DATA SHEETS C

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SGSP141	C-39
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SGSP149	C-47
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SGSP152	C-51
SGSP154	C-58
SGSP155	C-58
SGSP156	C-58
SGSP157	C-66
SGSP158	C-66
SGSP201	C-5
SGSP202	C-5
SGSP211	C-70
SGSP212	C-70
SGSP216	C-78
SGSP217	C-78
SGSP218	C-20
SGSP219	C-20
SGSP221	C-86
SGSP222	C-86
SGSP230	C-27
SGSP231	C-27
SGSP232	C-27
SGSP238	C-35
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SGSP101/P102
SGSP201/P202
SGSP301/P302

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

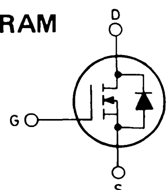
V_{DSS}	$R_{DS(ON)}$	I_D
80V/100V	1.4Ω	1.5A

ABSOLUTE MAXIMUM RATINGS

		TO-39 / SOT-82 / TO-220	SGSP101 / SGSP201 / SGSP301	SGSP102 / SGSP202 / SGSP302
V_{DS}	Drain-source voltage ($V_{GS} = 0$)		100V	80V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)		100V	80V
V_{GS}	Gate-Source voltage		± 20V	
I_D	Drain current (continuous) at $T_{case} = 25°C$		1.5A	
	at $T_{case} = 100°C$		0.95A	
I_{DM} (•)	Drain current (pulsed)		6A	
I_{DLM} (•)	Drain inductive current, clamped		6A	
			TO-39	SOT-82/TO-220
P_{tot}	Total power dissipation at $T_{case} \leq 25°C$		15W	18W
	Derating factor		0.12W/°C	0.14W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Junction temperature		150°C	

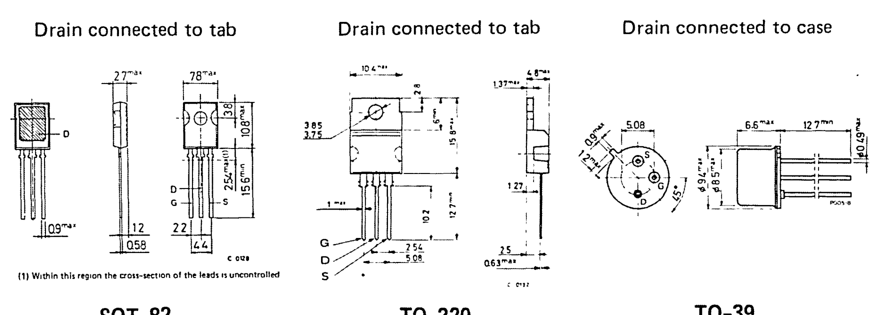
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



SOT-82 TO-220 TO-39

THERMAL DATA		TO-39	TO-220/SOT-82
$R_{thj-case}$	Thermal resistance junction-case	max. 8.3 °C/W	max. 6.8 °C/W
T_L	Maximum lead temperature for soldering purpose	275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP101/201/301** for **SGSP102/202/302**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			100	nA
ON*						
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μA	2		4	V
$V_{DS(on)}$	Drain-source voltage	V_{GS} = 10V I_D = 0.75A I_D = 1.5A (T_{case} = 100°C) I_D = 0.75A			1.05 2.2 2.1	V V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 0.75A			1.4	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 0.75A	0.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1MHz V_{GS} = 0		87	125 46 28	pF pF pF

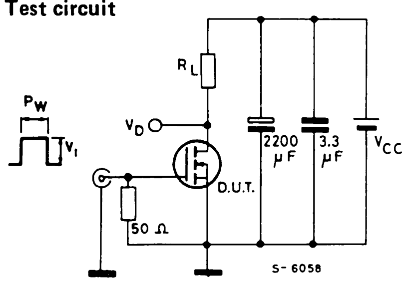
ELECTRICAL CHARACTERISTICS* (Continued)

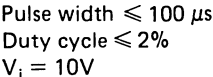
Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d(on)}$	Turn-on delay time	V_{CC} = 25V V_i = 10V		25		ns
t_r	Rise time	I_D = 0.75A R_i = 50 Ω		20		ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)		25		ns
t_f	Fall time			25		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				1.5	A
I_{SDM}(•)	Source drain current (pulsed)				6	A
V_{SD}	Forward on voltage	I_{SD} = 1.5A V_{GS} = 0			1.35	V
t_{on}	Turn-on time	I_{SD} = 1.5A V_{GS} = 0		90		ns
t_{rr}	Reverse recovery time	di/dt = 25A/µs		40		ns

* Pulsed: pulse duration ⩽ 300 µs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area

SWITCHING TIMES RESISTIVE LOAD

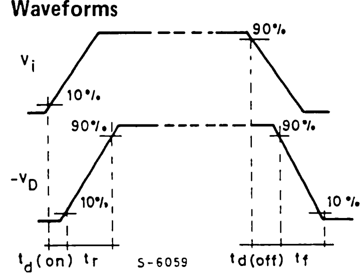
Test circuit





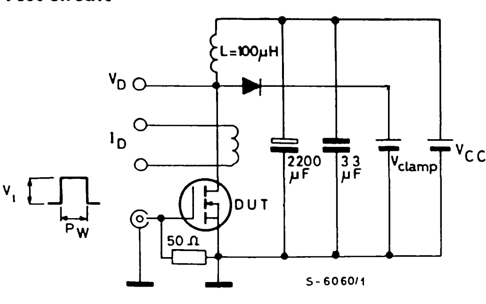
Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
V_i = 10V

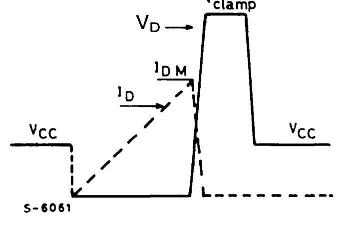
Waveforms



CLAMPED INDUCTIVE LOAD

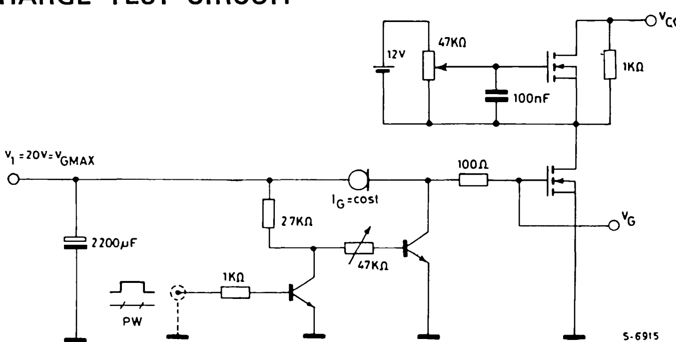
Test circuit **Waveforms**





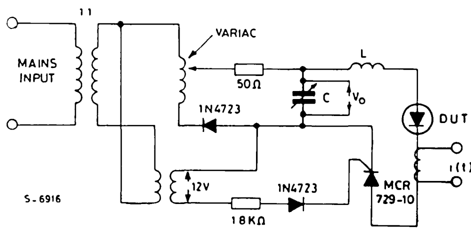
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



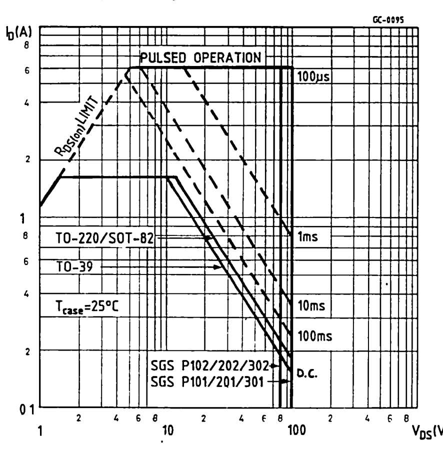
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

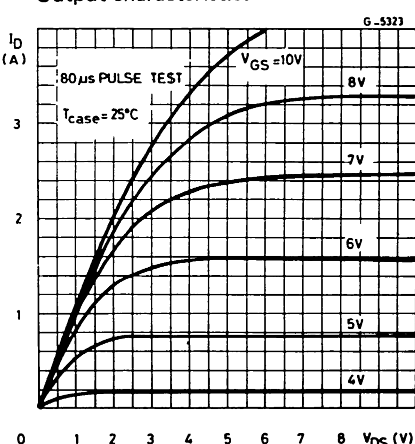


Jedec test circuit

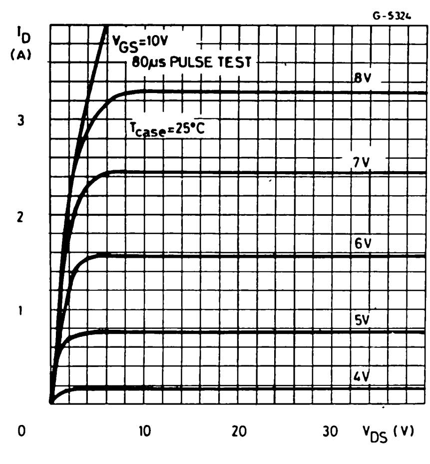
Safe operating areas



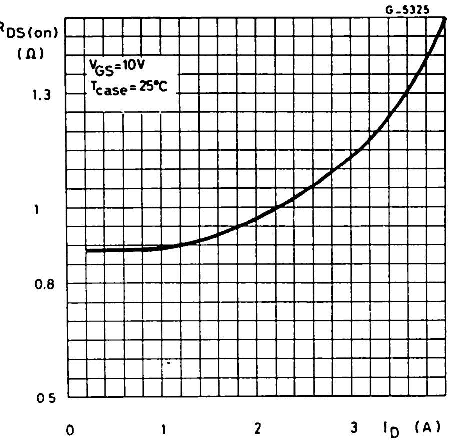
Output characteristics



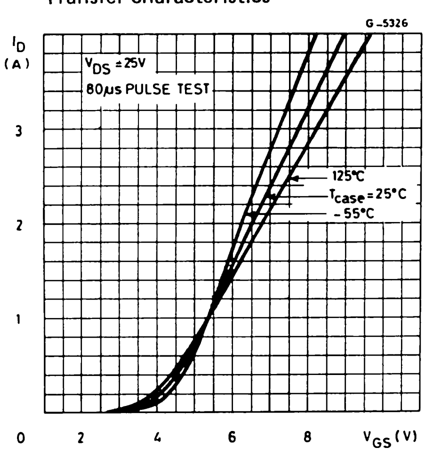
Output characteristics



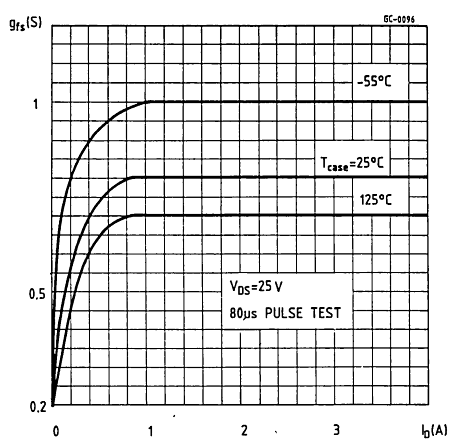
Static drain-source on resistance



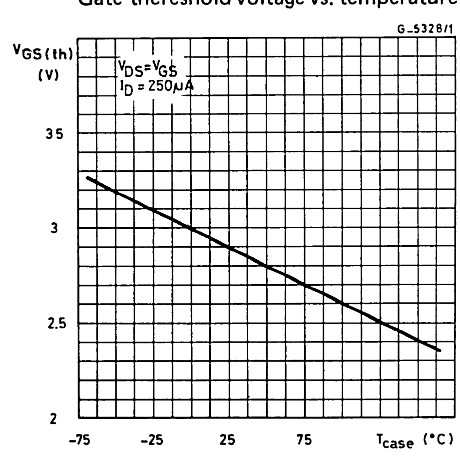
Transfer characteristics



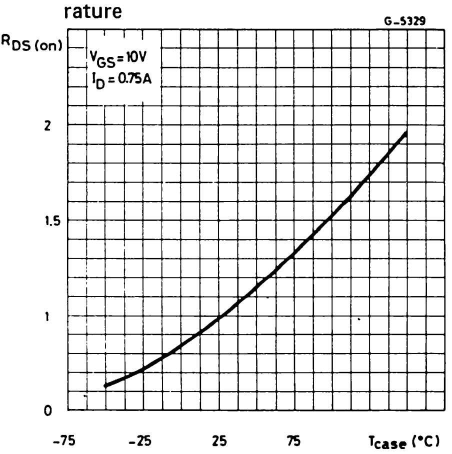
Transconductance



Gate thereshold voltage vs. temperature



Normalized on resistance vs. temperature



Gate charge vs. gate-source voltage

G-5333

V_{GS} (V)

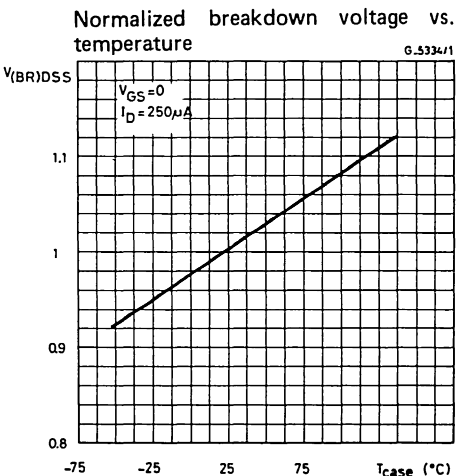
I_D = 2.5A
T_{case} = 25°C

20V
V_{DS} = 50V
80V

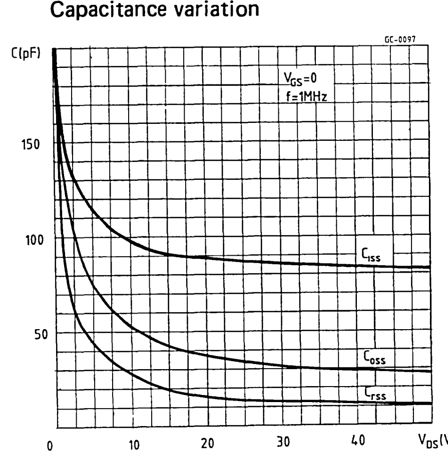
0 1 2 3 4 Q (nC)

16 14 12 10 8 6 4 2

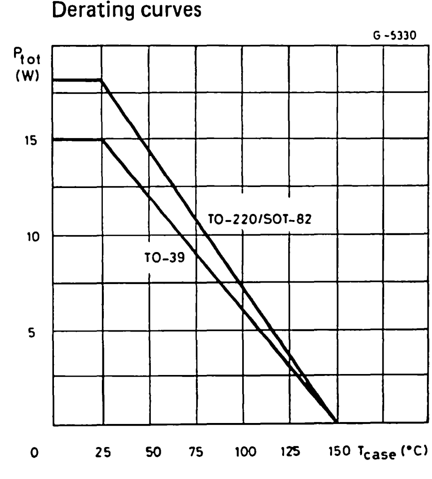
Normalized breakdown voltage vs. temperature



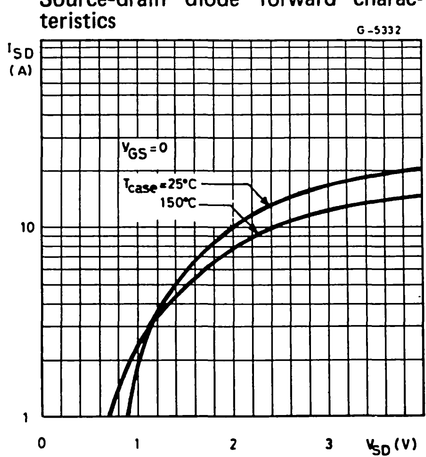
Capacitance variation



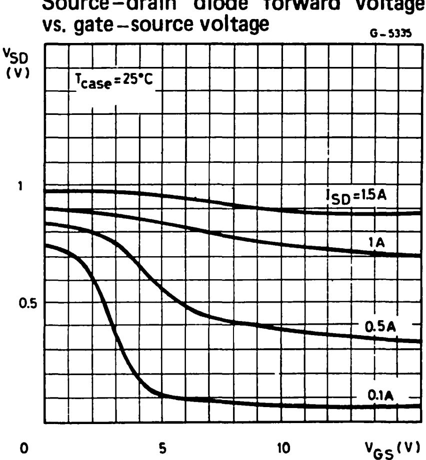
Derating curves



Source-drain diode forward characteristics



Source-drain diode forward voltage vs. gate-source voltage



SGSP111
SGSP112

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

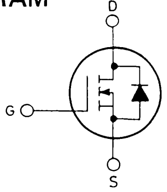
V_{DSS}	$R_{DS(ON)}$	I_D
80V/100V	0.3Ω	5A

ABSOLUTE MAXIMUM RATINGS

		SGSP111	SGSP112
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	80V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	80V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
	T_{case} = 100°C	3.2A	
I_{DM}(•)	Drain current (pulsed)	20A	
I_{DLM}(•)	Drain inductive current, clamped	20A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

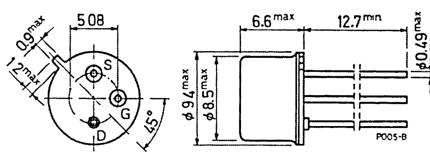
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-39

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3 °C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP111** for **SGSP112**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2.5A I_D = 5A T_C = 100°C I_D = 2.5A			0.75 1.65 1.50	V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5A			0.3	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 2.5A	2			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		375	480 230 110	pF pF pF

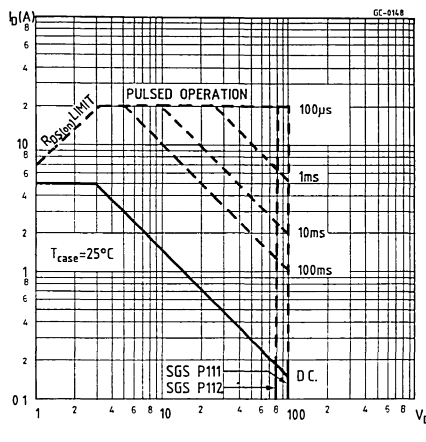
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25V I_D = 2.5A		35		ns
t_r	Rise time	V_i = 10V R_i = 50Ω		80		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				5	A
I_{SDM}(•)	Source drain current (pulsed)				20	A
V_{SD}	Forward on voltage	I_{SD} = 5A V_{GS} = 0			1.8	V
t_{on}	Turn-on time	I_{SD} = 5A V_{GS} = 0		150		ns
t_{rr}	Reverse recovery	di/dt = 25A/μs		150	200	ns

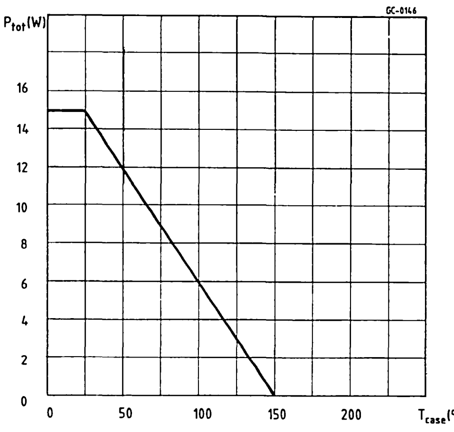
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

For typical curves switching times resistive load, clamped inductive load, gate charge, body drain diode trr measurement, test circuits see SGSP211 Datasheet.

Safe operating areas



Derating curve



SGSP116
SGSP117

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

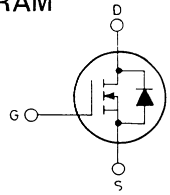
V_{DSS}	$R_{DS(ON)}$	I_D
200V	0.75Ω	4A
250V	1.2 Ω	4A

ABSOLUTE MAXIMUM RATINGS

		SGSP116	SGSP117
V_{DS}	Drain-source voltage (V_{GS} = 0)	250V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	250V	200V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	4A	
	T_{case} = 100°C	2.5A	
I_{DM}(•)	Drain current (pulsed)	16A	
I_{DLM} (•)	Drain inductive current, clamped	16A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

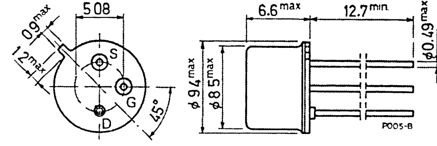
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-39

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3 °C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

OFF

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0				
		for **SGSP116**	250			V
		for **SGSP117**	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA

ON*

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2A				
		for **SGSP116**			2.4	V
		for **SGSP117**			1.5	V
		V_{GS} = 10V I_D = 4A				
		for **SGSP116**			5.4	V
		for **SGSP117**			3.5	V
		V_{GS} = 10V I_D = 2A T_{case} = 100°C				
		for **SGSP116**			4.8	V
		for **SGSP117**			3.0	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 2A				
		for **SGSP116**			1.20	Ω
		for **SGSP117**			0.75	Ω
gfs	Forward transconductance	V_{DS} = 25V I_D = 2A	1.5			mho

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25V f = 1 MHz		380	500	pF
C_{oss}	Output capacitance	V_{GS} = 0		100	130	pF
C_{rss}	Reverse transfer capacitance			50	65	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 100V I_D = 2A		27		ns
t_r	Rise time	V_i = 10V R_i = 50Ω		27		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				4	A
I_{SDM}(•)	Source drain current (pulsed)				16	A
V_{SD}	Forward on voltage	I_{SD} = 4A V_{GS} = 0			1.8	V
t_{on}	Turn-on time	I_{SD} = 4A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery	di/dt = 100A/μs		180		ns

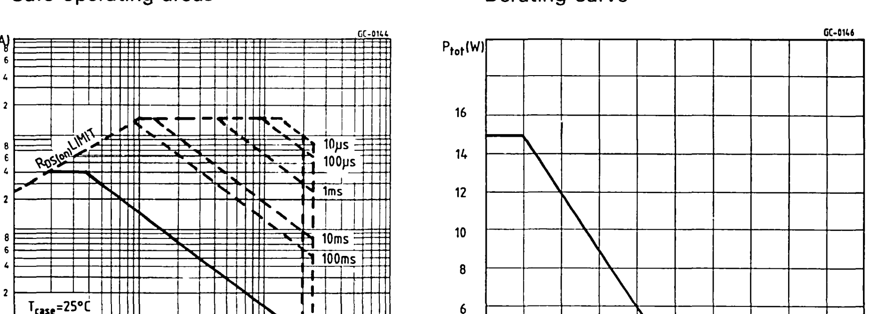
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

For typical curves and switching times resistive load, clamped inductive load, gate charge, body drain diode trr measurement, test circuits see SGSP216 Datasheet

Safe operating areas

Derating curve



SGSP118/P119
SGSP218/P219
SGSP318/P319
SGSP518/P519

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	$R_{DS(ON)}$	I_D
500V	**3.8Ω**	**2A**
550V	**4.5Ω**	**2A**

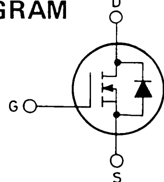
ABSOLUTE MAXIMUM RATINGS

	TO-39 SOT-82 TO-220 TO-3	SGSP118 SGSP218 SGSP318 SGSP518	SGSP119 SGSP219 SGSP319 SGSP519
V_{DS}	Drain-source voltage (V_{GS} = 0)	550V	500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	550V	500V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	2 A	
	at T_{case} = 100°C	1.3 A	
I_{DM}(•)	Drain current (pulsed)	8 A	
I_{DLM} (•)	Drain inductive current, clamped	8 A	

		TO-39	SOT-82	TO-220	TO-3
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	50W	75W	75W
	Derating factor	0.12W/°C	0.4W/°C	0.6W/°C	0.6W/°C
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

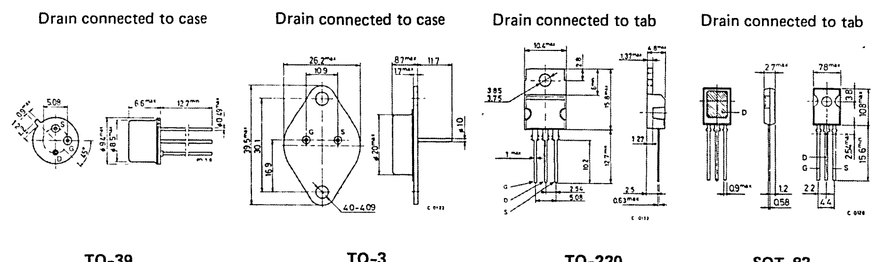
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



TO-39 TO-3 TO-220 SOT-82

THERMAL DATA

			TO-39	SOT-82	TO-220/TO3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8.3°C/W	2.5°C/W	1.67°C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 V for **SGSP118/218/318/518** for **SGSP119/219/319/519**	 550 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	for **SGSP118/218/318/518** V_{GS} = 10 V I_D = 1 A for **SGSP119/219/319/519** V_{GS} = 10 V I_D = 1 A			 4.5 3.8	 V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A for **SGSP118/218/318/518** for **SGSP119/219/319/519**			 4.5 3.8	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 1 A	1.2			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f= 1MHz V_{GS} = 0 V		340	380 70 32	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 250V I_D = 1 A		40		ns
t_r	Rise time	V_i = 10V R_i = 10Ω		20		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			10		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				2	A
I_{SDM}(•)	Source drain current (pulsed)				8	A
V_{SD}	Forward on voltage	I_{SD} = 2 A V_{GS} = 0			1.15	V
t_{on}	Turn-on time	I_{SD} = 2 A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery	di/dt = 25 A/μs		200		ns

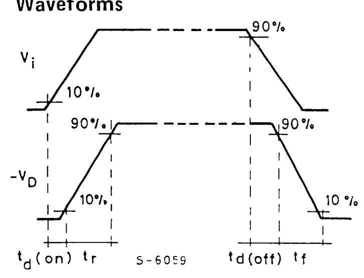
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit

P_W V_i R_L V_D D.U.T. 10 Ω 2200 μF 3.3 μF V_{CC} S-6058

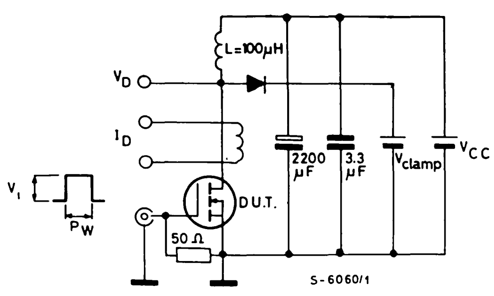
Waveforms



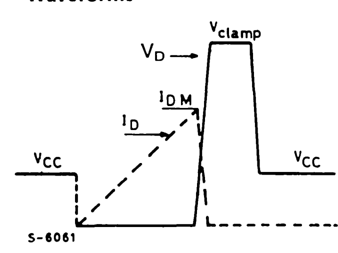
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

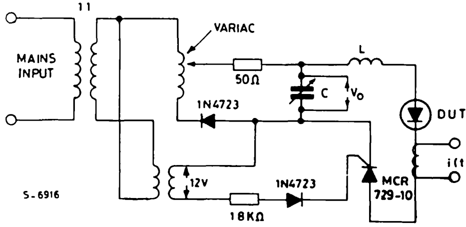


Waveforms



V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

DIODE BODY-DRAIN t_{rr} MEASUREMENT



Jedec test circuit

SGSP121
SGSP122

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

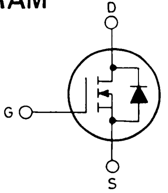
V_{DSS}	$R_{DS(ON)}$	I_D
50V/60V	0.13Ω	7A

ABSOLUTE MAXIMUM RATINGS

		SGSP121	SGSP122
V_{DS}	Drain-source voltage (V_{GS} = 0)	60V	50V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	60V	50V
V_{GS}	Gate-source voltage	± 20V	
I_D	Drain current (continuous) T_{case} = 25°C	7A	
	T_{case} = 100°C	4.5A	
I_{DM}(•)	Drain current (pulsed)	28A	
I_{DLM} (•)	Drain inductive current, clamped	28A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

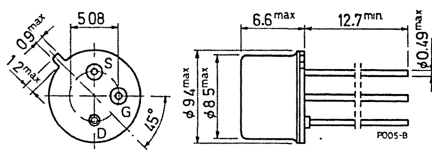
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-39

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3 °C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP121** for **SGSP122**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 3.5A I_D = 7A T_C = 100°C I_D = 3.5A			0.45 1 0.90	V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D =3.5A			0.13	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D =3.5A	2.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

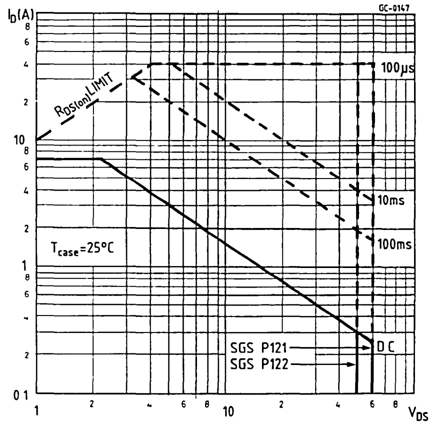
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25V I_D = 3.5A		30		ns
t_r	Rise time	V_i = 10V R_i = 50Ω		130		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			130		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				7	A
I_{SDM}(•)	Source drain current (pulsed)				28	A
V_{SD}	Forward on voltage	I_{SD} = 7A V_{GS} = 0			1.8	V
t_{on}	Turn-on time	I_{SD} = 7A V_{GS} = 0		60		ns
t_{rr}	Reverse recovery	di/dt = 25A/μs		100	150	ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

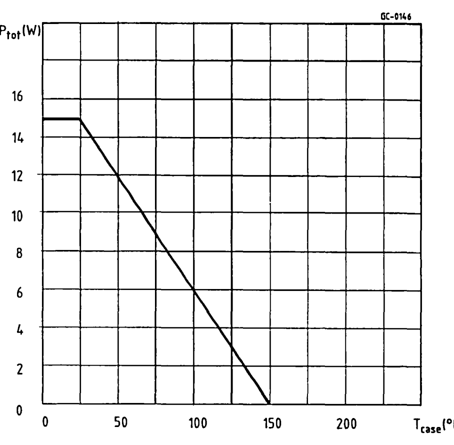
(•) Pulse width limited by safe operating area.

For typical curves and switching times resistive load, clamped inductive load, gate charge, body drain diode trr measurement, test circuits see SGSP221 Datasheet.

Safe operating areas



Derating curve



N-CHANNEL POWER MOS TRANSISTORS

SGSP130/P131/P132
SGSP230/P231/P232
SGSP330/P331/P332
SGSP530/P531/P532

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

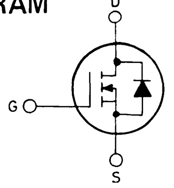
V_{DSS}	$R_{DS(ON)}$	I_D
350V/400V	2.5Ω	3A
450V	3 Ω	3A

ABSOLUTE MAXIMUM RATINGS

	TO-39	SGSP130	SGSP131	SGSP132
	SOT-82	SGSP230	SGSP231	SGSP232
	TO-220	SGSP330	SGSP331	SGSP332
	TO-3	SGSP530	SGSP531	SGSP532
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	450V	400V	350V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	450V	400V	350V
V_{GS}	Gate-source voltage		± 20V	
I_D	Drain current (continuous)		3A	
I_D	Drain current at $T_{case} = 100°C$		1.9A	
I_{DM} (•)	Drain current (pulsed)		12A	
I_{DLM} (•)	Drain inductive current, clamped		12A	
		TO-39	SOT-82	TO-220/TO-3
P_{tot}	Total power dissipation at $T_{case} \leq 25°$ C	15W	50W	75W
	Derating factor	0.12W/°C	0.4W/°C	0.6W/°C
T_{stg}	Storage temperature		−55 to 150°C	
T_j	Junction temperature		150°C	

(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM

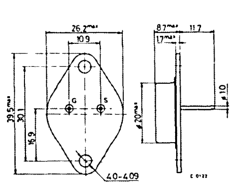


MECHANICAL DATA

Dimensions in mm

Drain connected to case

TO-39

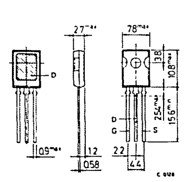


Drain connected to case

TO-3

Drain connected to tab

TO-220



Drain connected to tab

SOT-82

THERMAL DATA

		TO-220/TO-3	SOT-82	TO-39
$R_{th\ j-case}$	Thermal resistance junction-case	1.67°C/W	2.5°C/W	8.3°C/W
T_L	Maximum lead temperature for soldering purpose		275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown	I_D = 250 μA V_{GS} = 0				
		for **SGSP130/230/330/530**	450			V
		for **SGSP131/231/331/531**	400			V
		for **SGSP132/232/332/532**	350			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_{DS} = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	for **SGSP130/230/330/530**				
		V_{GS} = 10V I_D = 1.5A			4.5	V
		(T_{case} = 100°C) I_D = 1.5A			9	V
		for **SGSP131/231/331/531**				
		for **SGSP132/232/332/532**				
		V_{GS} = 10V I_D = 1.5A			3.75	V
		(T_{case} = 100°C) I_D = 1.5A			7.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 1.5A				
		for **SGSP130/230/330/530**			3	Ω
		for **SGSP131/231/331/531**			2.5	Ω
		for **SGSP132/232/332/532**			2.5	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 1.5A	1.5			mho
DYNAMICN						
C_{iss}	Input capacitance	V_{DS} = 25V f = 1MHz		340	450	pF
C_{oss}	Output capacitance			60	95	pF
C_{tss}	Reverse transfer capacitance	V_{GS} = 0		30	50	pF

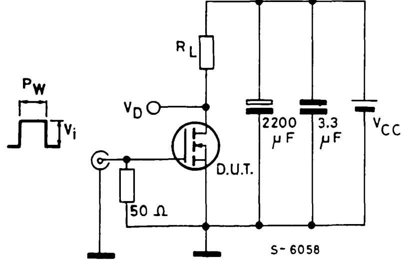
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d(on)}$	Turn-on delay time	V_{CC} = 25V V_i = 10V		30		ns
t_r	Rise time	I_D = 1.5A R_i = 50Ω		35		ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			80		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current				3	A
I_{SDM} (·)	Source-drain current (pulsed)				12	A
V_{SD}	Forward on voltage	I_{SD} = 3A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 3A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery time	di/dt = 25A/μs		200		ns

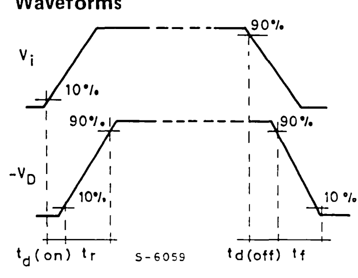
* Pulsed: pulse duration ⩽ 300 μs, duty cycle ⩽ 2%
(·) Pulsed width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



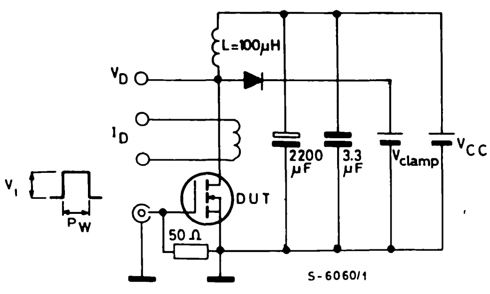
Waveforms



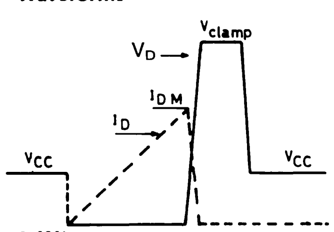
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

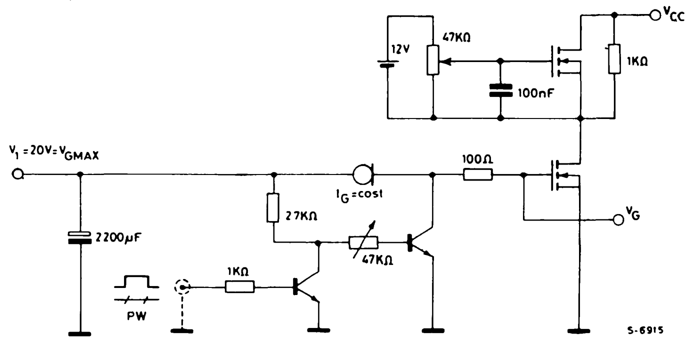


Waveforms



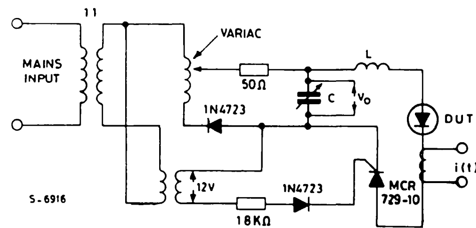
V_i = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



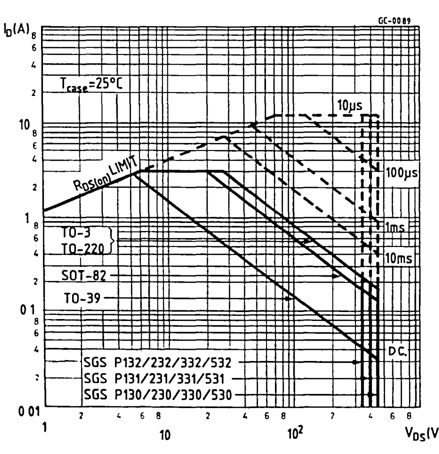
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

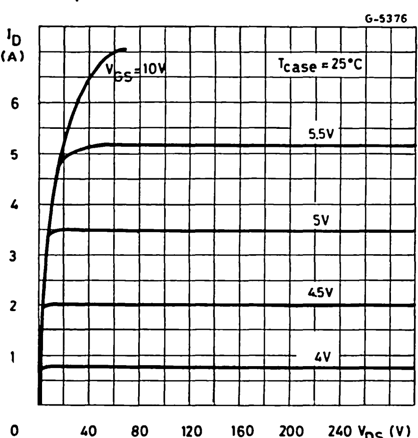


Jedec test circuit

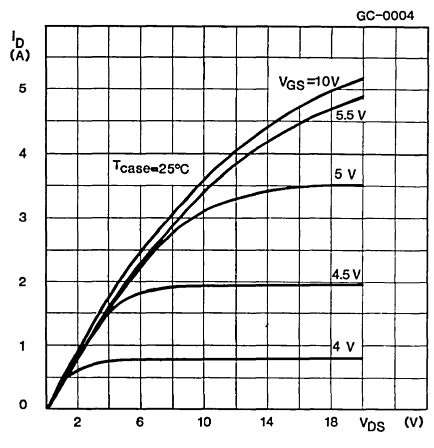
Safe operating areas



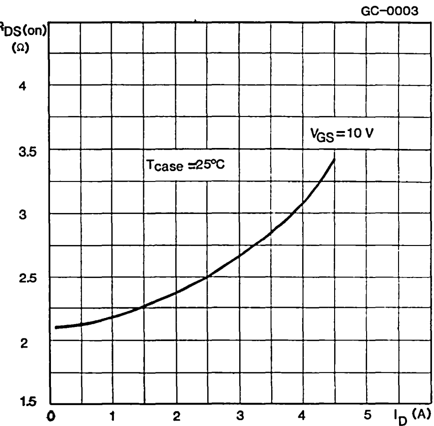
Output characteristics



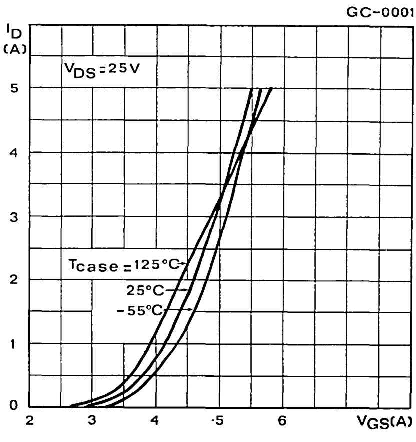
Output characteristics



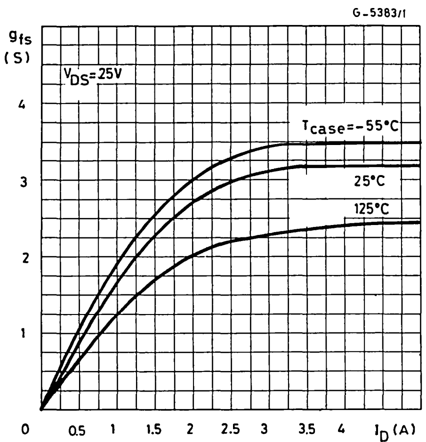
Static drain-source on resistance



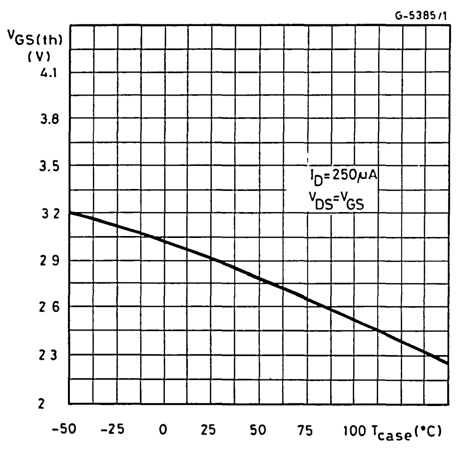
Transfer characteristics



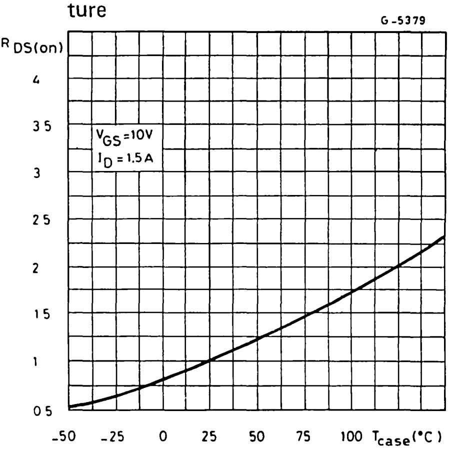
Transconductance



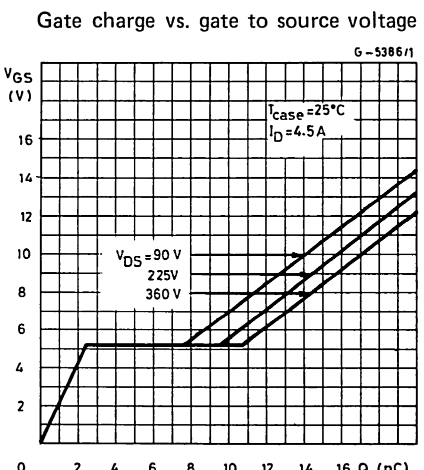
Gate threshold voltage vs. temperature



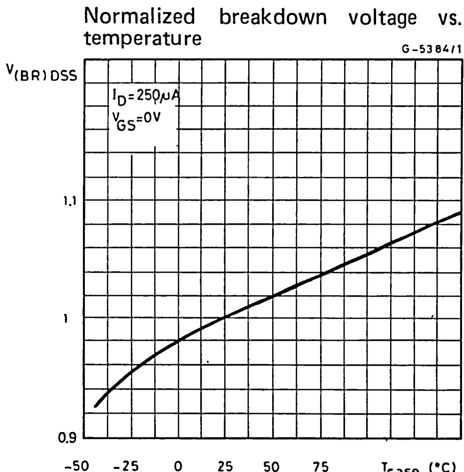
Normalized on resistance vs. temperature



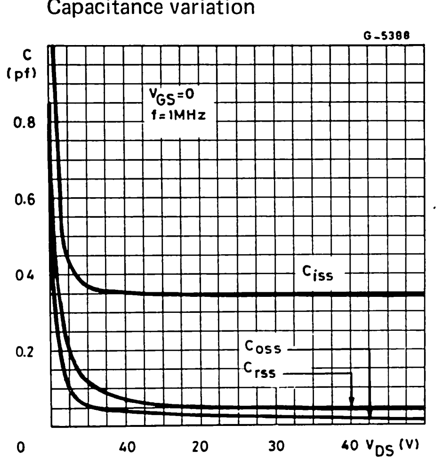
Gate charge vs. gate to source voltage



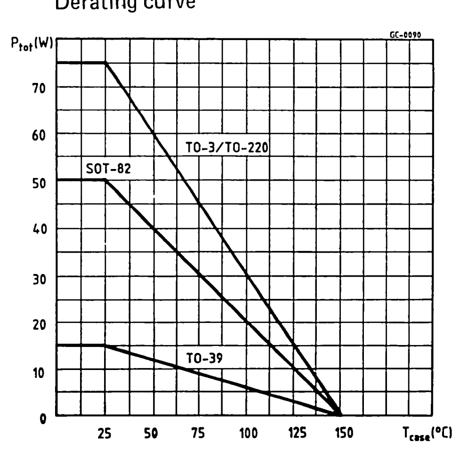
Normalized breakdown voltage vs. temperature

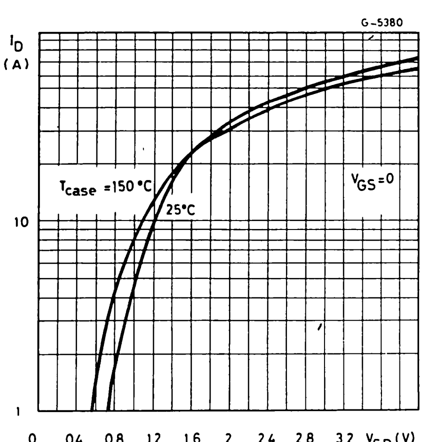


Capacitance variation

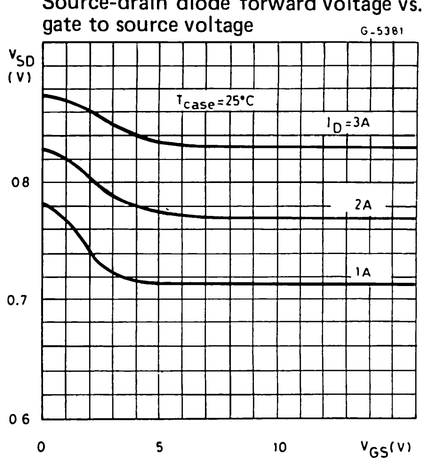


Derating curve





Source-drain diode forward voltage vs. gate to source voltage



N-CHANNEL POWER MOS TRANSISTORS

SGSP138/P139
SGSP238/P239
SGSP338/P339

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

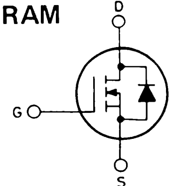
V_{DSS}	$R_{DS(ON)}$	I_D
500V	8.5Ω	1.2A
550V	11 Ω	1.2A

ABSOLUTE MAXIMUM RATINGS

		TO-39 SOT-82 TO-220	SGSP138 SGSP238 SGSP338		SGSP139 SGSP239 SGSP339
V_{DS}	Drain-source voltage (V_{GS} = 0)		550V		500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		550V		500V
V_{GS}	Gate-source voltage			±20V	
I_D	Drain current (continuous) T_{case} = 25°C			1.2A	
	at T_{case} = 100°C			0.8A	
I_{DM}(•)	Drain current (pulsed)			4.8A	
I_{DLM} (•)	Drain inductive current, clamped			4.8A	
			TO-39	SOT-82	TO-220
P_{tot}	Total power dissipation at T_{case} = 25°C		15W	40W	50W
	Derating factor		0.12W/°C	0.32W/°C	0.4W/°C
T_{stg}	Storage temperature			-55 to 150°C	
T_j	Max. operating junction temperature			150°C	

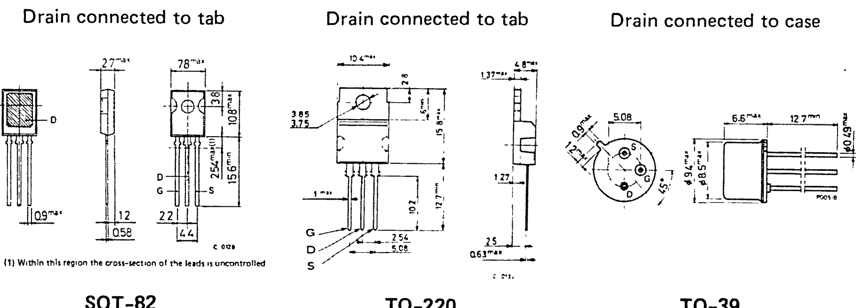
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



SOT-82 TO-220 TO-39

THERMAL DATA

			TO-39	SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8.3°C/W	3.12°C/W	2.5°C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit

OFF

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$ Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP138/P238/P338** for **SGSP139/P239/P339**	 550 500			 V V
I_{DSS} Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS} Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA

ON*

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$ Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$ Drain-source voltage	V_{GS} = 10V I_D = 0.6 A for **SGSP138/P238/P338** for **SGSP139/P239/P339**			 6.6 5.1	 V V
$R_{DS\ (on)}$ Static drain-source on resistance	V_{GS} = 10 V I_D = 0.6 A for **SGSP138/P238/P338** for **SGSP139/P239/P339**			 11 8.5	 Ω Ω
g_{fs} Forward transconductance	V_{DS} = 25V I_D = 0.6 A	0.65			mho

DYNAMIC

Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} Input capacitance C_{oss} Output capacitance C_{rss} Reverse transfer capacitance	V_{DS} = 25 V f= 1 MHz V_{GS} = 0		170 60 30	220 80 40	pF pF pF

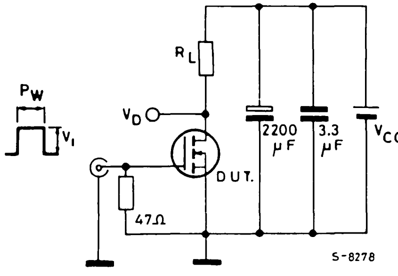
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 250V I_D = 0.6 A		15		ns
t_r	Rise time	V_i = 10 V R_i = 4.7Ω		15		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				1.2	A
I_{SDM}(•)	Source drain current (pulsed)				4.8	A
V_{SD}	Forward on voltage	I_{SD} = 1.2 A V_{GS} = 0			1.15	V
t_{on}	Turn-on time	I_{SD} = 1.2 A V_{GS} = 0		100		ns
t_{rr}	Reverse recovery time	di/dt = 25 A/μs		70		ns

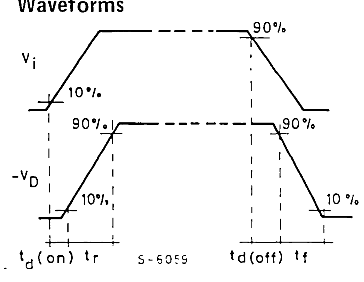
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



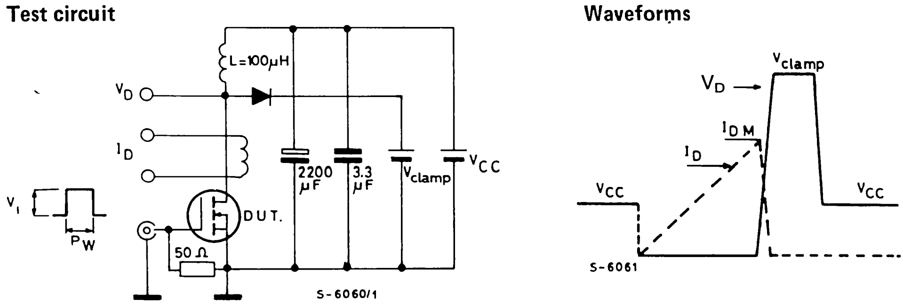
Waveforms



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_I = 10V

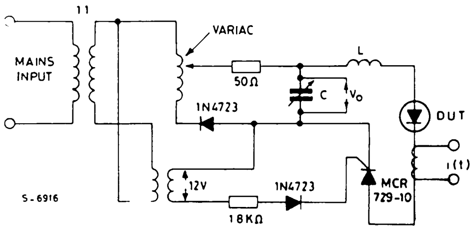
CLAMPED INDUCTIVE LOAD

Test circuit **Waveforms**



V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

DIODE BODY-DRAIN t_{rr} MEASUREMENT



Jedec test circuit

SGSP140/P141/P142
SGSP240/P241/P242
SGSP340/P341/P342

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

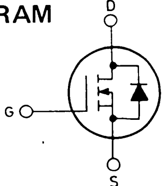
V_{DSS}	$R_{DS(ON)}$	I_D
350V/400V	20Ω	0.6A
450V	25Ω	0.6A

ABSOLUTE MAXIMUM RATINGS

		TO-39 / SOT-82 / TO-220	SGSP140 / SGSP240 / SGSP340	SGSP141 / SGSP241 / SGSP341	SGSP142 / SGSP242 / SGSP342
V_{DS}	Drain-source voltage (V_{GS} = 0)		450V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		450V	400V	350V
V_{GS}	Gate-source voltage			±20V	
I_D	Drain current (continuous) T_{case} = 25°C			0.6A	
	at T_{case} = 100°C			0.4A	
I_{DM} (•)	Drain current (pulsed)			2.4A	
I_{DLM} (•)	Drain inductive current, clamped			2.4A	
			TO-39	**SOT-82**	**TO-220**
P_{tot}	Total dissipation at T_{case} = 25°C		15W	18W	18W
	Derating factor		0.12W/°C	0.14W/°C	0.14W/°C
T_{stg}	Storage temperature			-55 to 150°C	
T_j	Max operating junction temperature			150°C	

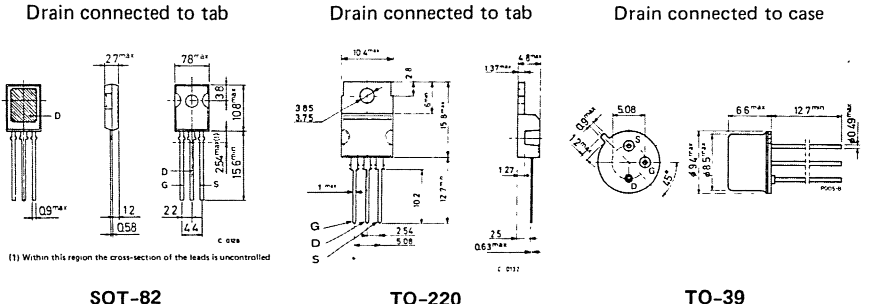
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

			TO-39	SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8.3°C/W	6.8°C/W	6.8°C/W
T_L	Maximum lead temperature for soldering purpose			275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP140/P240/P340** for **SGSP141/P241/P341** for **SGSP142/P242/P342**	 450 400 350			 V V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D =0.3 A for **SGSP140/P240/P340** for **SGSP141/P241/P341** for **SGSP142/P242/P342**			 7.5 6 6	 V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D =0.3 A for **SGSP140/P240/P340** for **SGSP141/P241/P341** for **SGSP142/P242/P342**			 25 20 20	 Ω Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D =0.3 A	0.2			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f= 1MHz V_{GS} = 0 V		80	105 20 12	pF pF pF

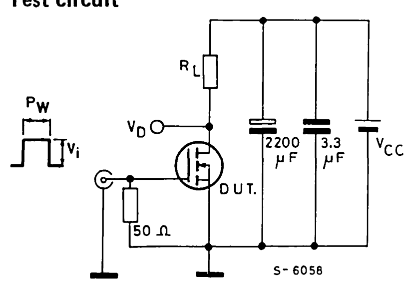
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 25V I_D = 0.3 A		22		ns
t_r	Rise time	V_i = 10 V R_i = 50Ω		10		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		35		ns
t_f	Fall time			10		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				0.6	A
I_{SDM}(•)	Source drain current (pulsed)				2.4	A
V_{SD}	Forward on voltage	I_{SD} = 0.6A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 0.6 A V_{GS} = 0		24		ns
t_{rr}	Reverse recovery	di/dt = 25 A/μs		30		ns

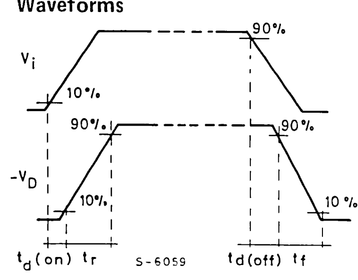
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



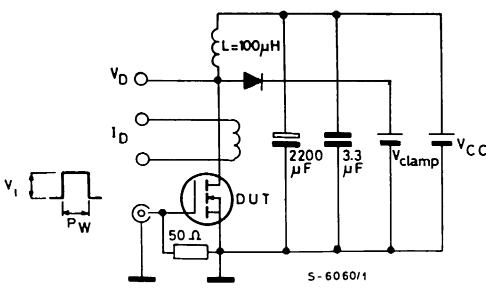
Waveforms



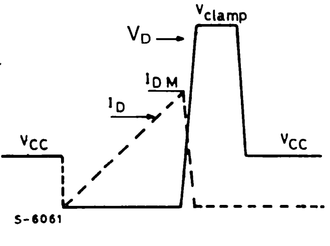
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

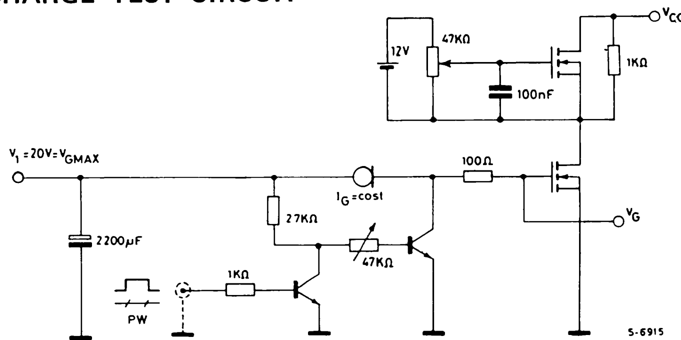


Waveforms



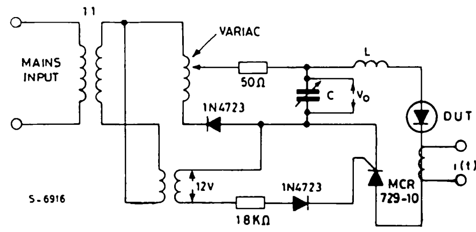
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



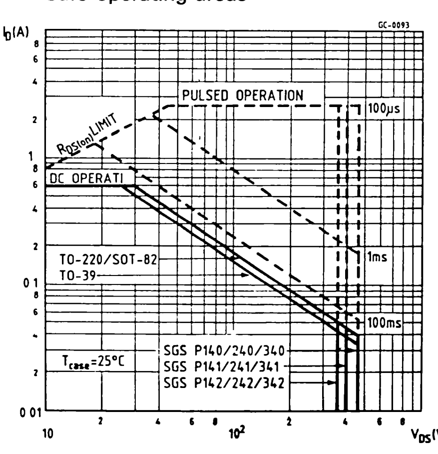
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

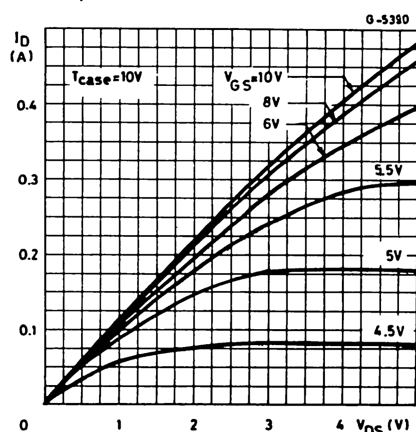


Jedec test circuit

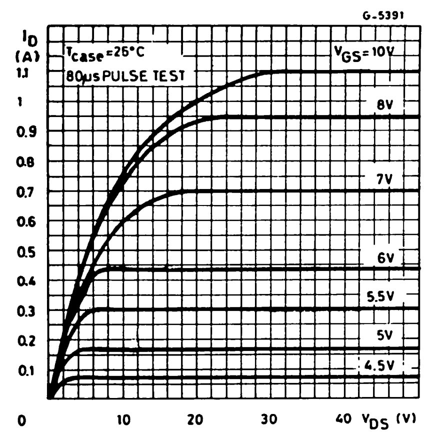
Safe operating areas



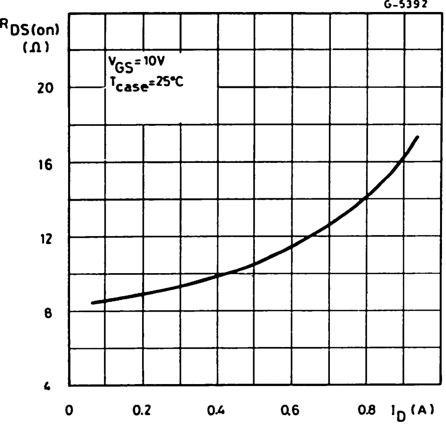
Output characteristics



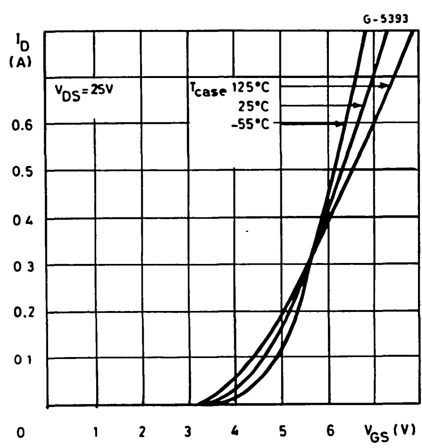
Output characteristics



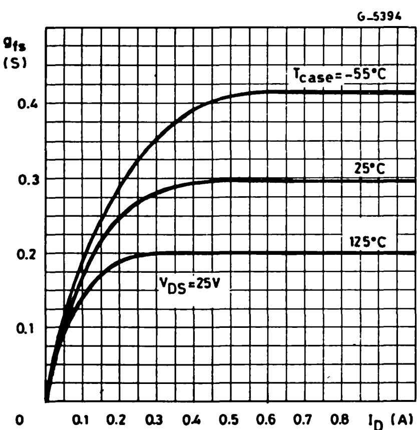
Static drain-source on resistance



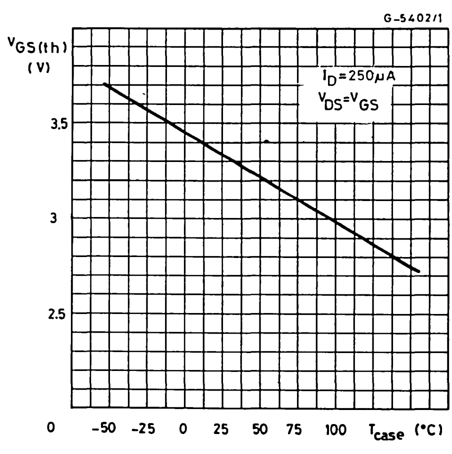
Transfer characteristics



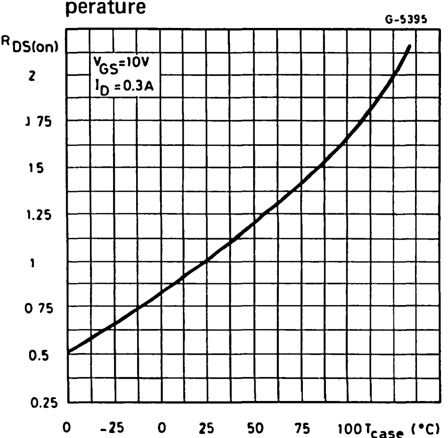
Transconductance



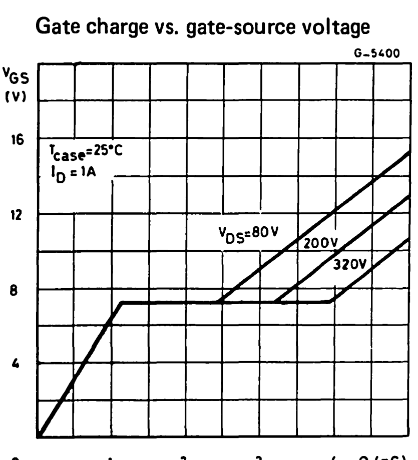
Gate threshold voltage vs, temperature



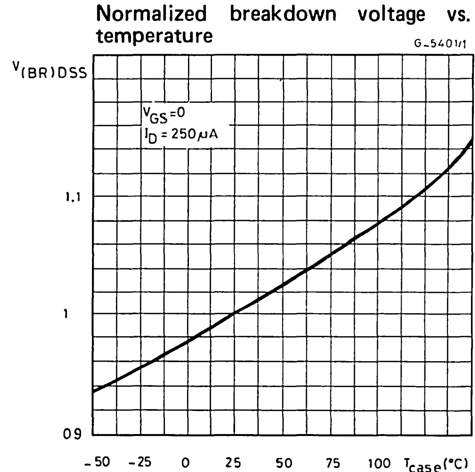
Normalized on resistance vs. temperature



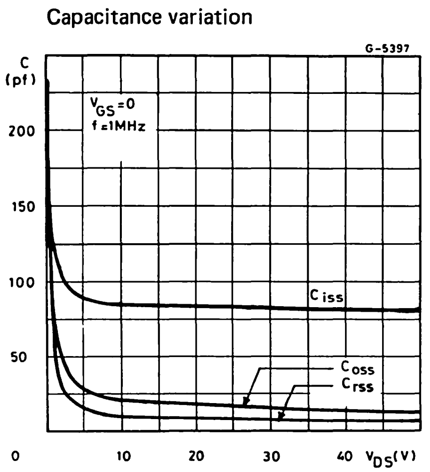
Gate charge vs. gate-source voltage



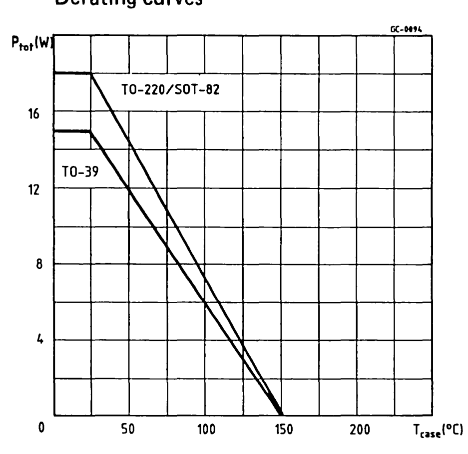
Normalized breakdown voltage vs. temperature



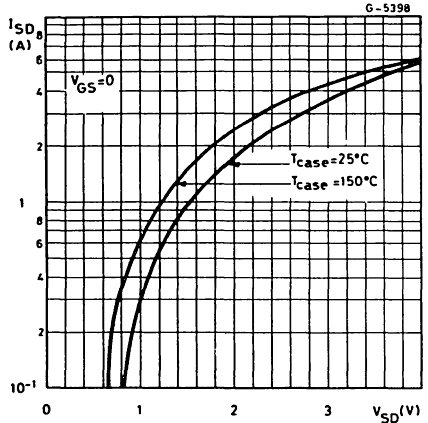
Capacitance variation



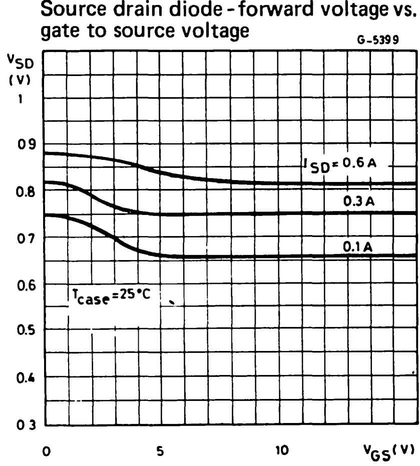
Derating curves



Source drain diode - forward voltage



Source drain diode - forward voltage vs. gate to source voltage



SGSP148/P149
SGSP248/P249
SGSP348/P349

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

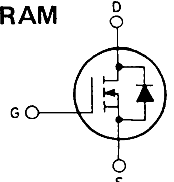
V_{DSS}	$R_{DS(ON)}$	I_D
500V	30Ω	0.5A
550V	40Ω	0.5A

ABSOLUTE MAXIMUM RATINGS

	TO-39 SOT-82 TO-220	SGSP148 SGSP248 SGSP348		SGSP149 SGSP249 SGSP349
V_{DS}	Drain-source voltage (V_{GS} = 0)	550V		500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	550V		500V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		0.5 A	
	at T_{case} = 100°C		0.35A	
I_{DM}(•)	Drain current (pulsed)		2 A	
I_{DLM} (•)	Drain inductive current, clamped		2 A	
		TO-39	SOT-82	TO-220
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	18W	18W
	Derating factor	0.12W/°C	0.14W/°C	0.14W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab

(1) Within this region the cross-section of the leads is uncontrolled

SOT-82

Drain connected to tab

TO-220

Drain connected to case

TO-39

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THERMAL DATA

			TO-39	SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3°C/W	6.8°C/W	
T_L	Maximum lead temperature for soldering purpose		275°C		

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit

OFF

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$ Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP148/248/348** for **SGSP149/249/349**	 550 500			 V V
I_{DSS} Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS} Gate-body leakage current (V_{DS} = 0)	V_{GS} = $\pm$20 V			100	nA

ON*

Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$ Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$ Drain-source	V_{GS} = 10V I_D = 0.25 A for **SGSP148/248/348** for **SGSP149/249/341**			 10 7.5	 V V
$R_{DS\ (on)}$ Static drain-source	V_{GS} = 10 V I_D = 0.25A for **SGSP148/248/348** for **SGSP149/249/349**			 30 40	 Ω Ω
g_{fs} Forward transconductance	V_{DS} = 25V I_D = 0.25A	0.18			mho

DYNAMIC

Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} Input capacitance C_{oss} Output capacitance C_{rss} Reverse transfer capacitance	V_{DS} = 25 V f= 1 MHz V_{GS} = 0		70 15 10	95 20 13	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.

SWITCHING

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$t_{d\,(on)}$	Turn-on time	V_{CC} = 25V I_D = 0.25A		10		ns
t_r	Rise time	V_I = 10 V R_I = 50Ω		10		ns
$t_{d\,(off)}$	Turn-off delay time	(see test circuit)		15		ns
t_f	Fall time			10		ns

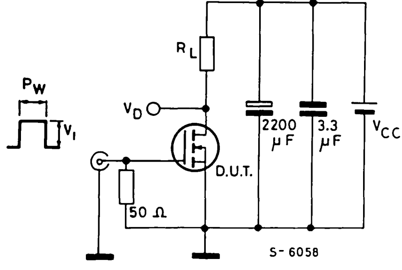
SOURCE DRAIN DIODE

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
I_{SD}	Source drain current				0.5	A
I_{SDM}(•)	Source drain current (pulsed)				2	A
V_{SD}	Forward on voltage	I_{SD} = 0.5A V_{GS} = 0			1.15	V
t_{on}	Turn-on time	I_{SD} = 5A V_{GS} = 0		24		ns
t_{rr}	Reverse recovery	di/dt = 25 A/μs		30		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

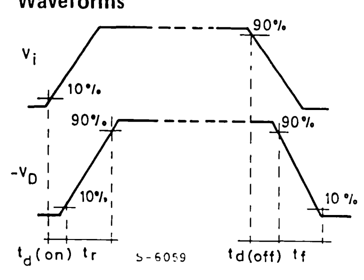
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

Waveforms

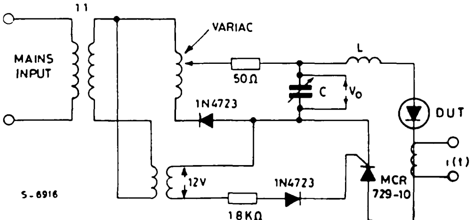


CLAMPED INDUCTIVE LOAD

Test circuit **Waveforms**

V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

DIODE BODY-DRAIN t_{rr} MEASUREMENT



Jedec test circuit

N-CHANNEL POWER MOS TRANSISTORS

SGSP151/P152
SGSP251/P252
SGSP351/P352

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

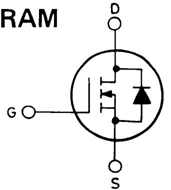
V_{DSS}	$R_{DS(ON)}$	I_D
80V/100V	0.45Ω	5A

ABSOLUTE MAXIMUM RATINGS

	TO-39 SOT-82 TO-220	SGSP151 SGSP251 SGSP351		SGSP152 SGSP252 SGSP352
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100V		80V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	100V		80V
V_{GS}	Gate-Source voltage		± 20V	
I_D	Drain current (continuous) at $T_{case} = 25°C$		5A	
	at $T_{case} = 100°C$		3.2A	
I_{DM} (•)	Drain current (pulsed)		20A	
I_{DLM} (•)	Drain inductive current, clamped		20A	
		TO-39	SOT-82	TO-220
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$	15W	40W	50W
	Derating factor	0.12W/°C	0.32W/°C	0.4W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Junction temperature		150°C	

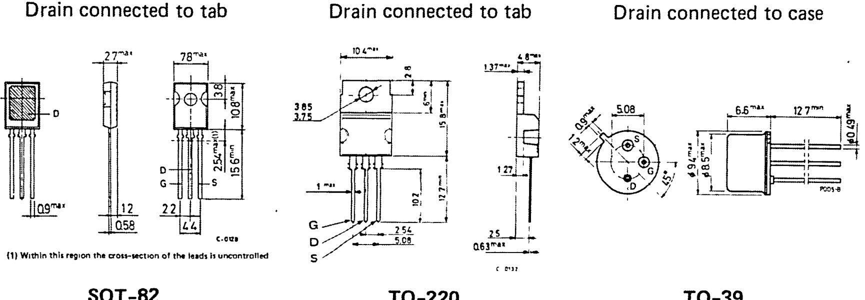
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



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THERMAL DATA

			TO-39	SOT-82	TO-220
$R_{th\ j-case}$	Thermal resistance junction-case	max	8.3°C/W	3.12°C/W	2.5°C/W
T_L	Maximum lead temperature for soldering purpose			275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP151/251/351** for **SGSP152/252/352**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			100	nA
ON *						
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ I_D = 250 μA	2		4	V
$V_{DS(on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2.5A I_D = 5A (T_{case} = 100°C) I_D = 2.5A			1.12 2.3 2.24	V V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 2.5A			0.45	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 2.5A	1.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capaticance Reverse transfer capacitance	V_{DS} = 25V f = 1MHz V_{GS} = 0		180	250 100 40	pF pF pF

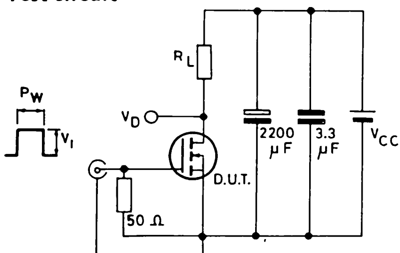
ELECTRICAL CHARACTERISTICS (Continued)

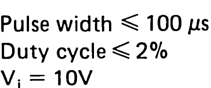
Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 25V$ $V_i = 10V$		30		ns
t_r	Rise time	$I_D = 2.5A$ $R_i = 50\ \Omega$		50		ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)		50		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				5	A
I_{SDM} (•)	Source drain current (pulsed)				20	A
V_{SD}	Forward on voltage	$I_{SD} = 5A$ $V_{GS} = 0$			1.35	V
t_{on}	Turn-on time	$di/dt = 25A/\mu s$		80		ns
t_{rr}	Reverse recovery time	$I_{SD} = 5A$ $V_{GS} = 0$		120		ns

* Pulsed: pulse duration $\leqslant 300\ \mu s$, duty cycle $\leqslant 2\%$
(•) Pulse width limited by safe operating area

SWITCHING TIMES RESISTIVE LOAD

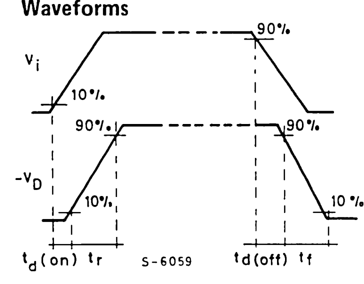
Test circuit





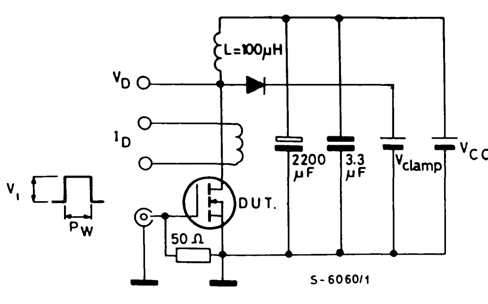
Pulse width $\leqslant 100\ \mu s$
Duty cycle $\leqslant 2\%$
$V_i = 10V$

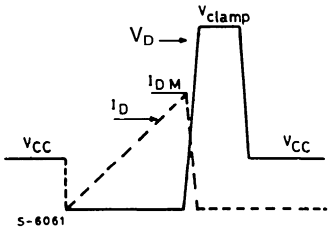
Waveforms



CLAMPED INDUCTIVE LOAD

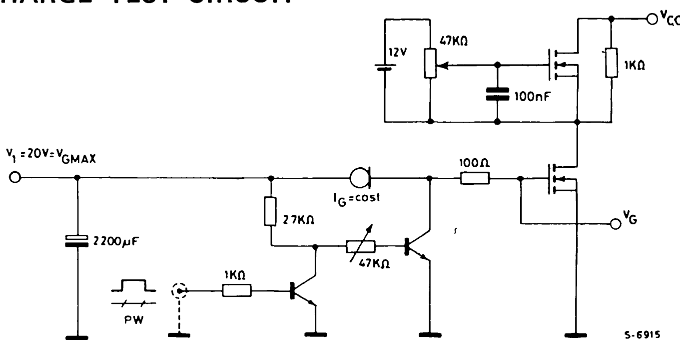
Test circuit **Waveforms**





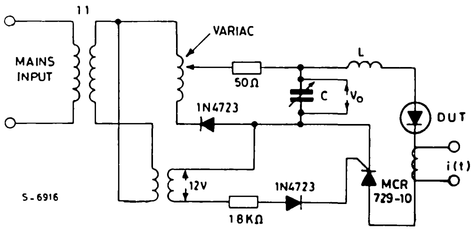
$V_I = 12V$
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



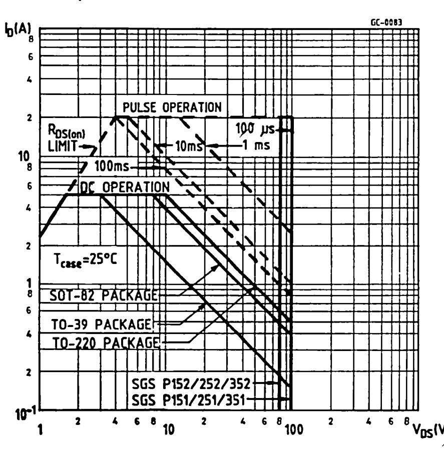
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

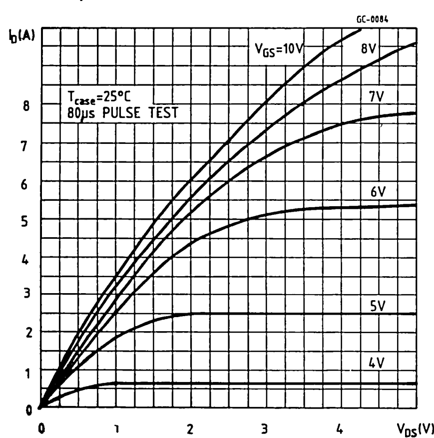


Jedec test circuit

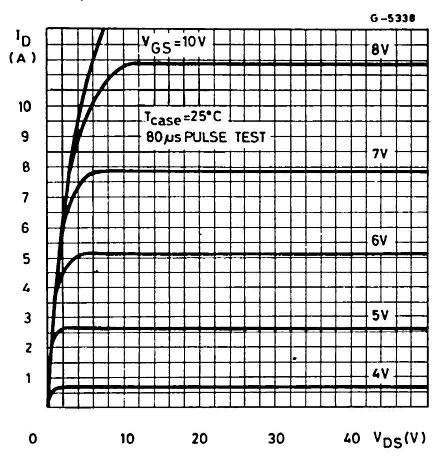
Output characteristics



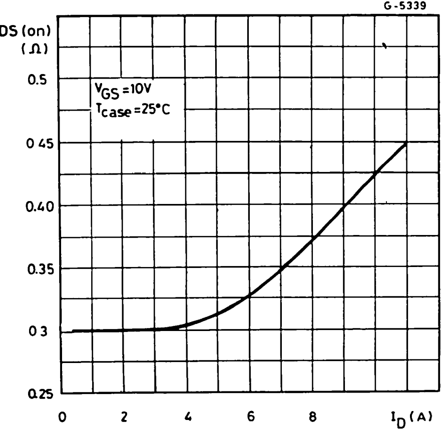
Output characteristics



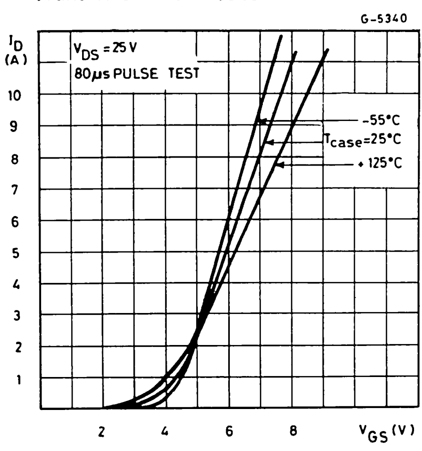
Output characteristics



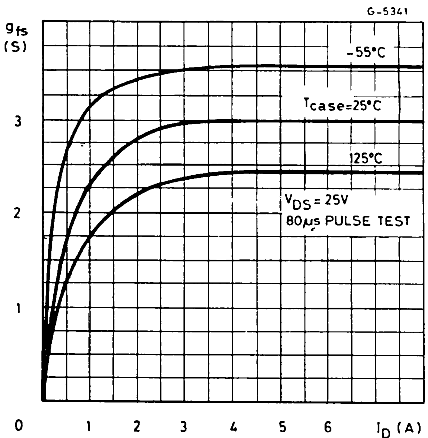
Static drain-source on resistance.



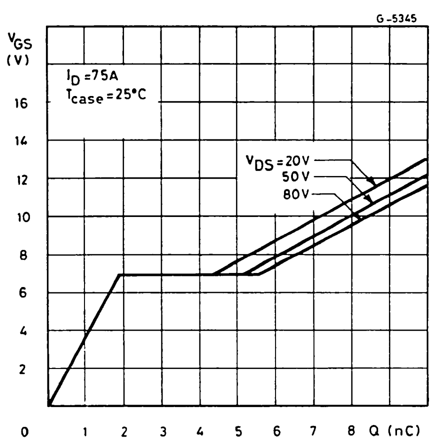
Transfer characteristics



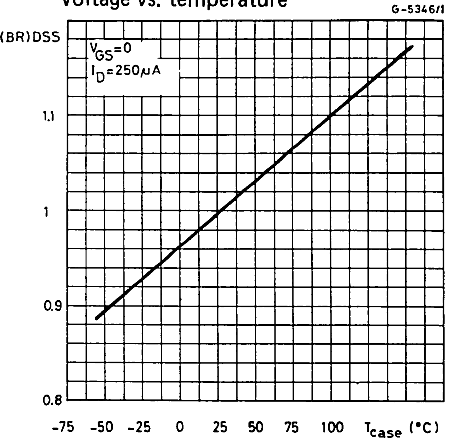
Transconductance



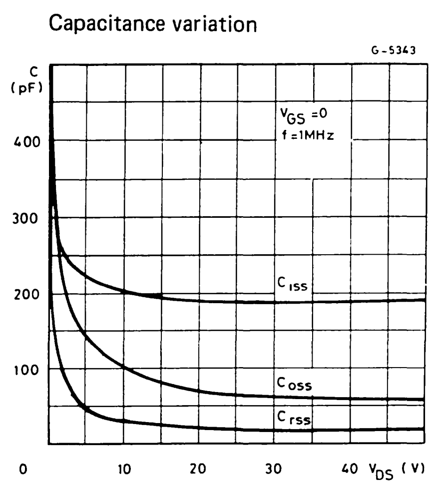
Gate charge vs. gate-source voltage



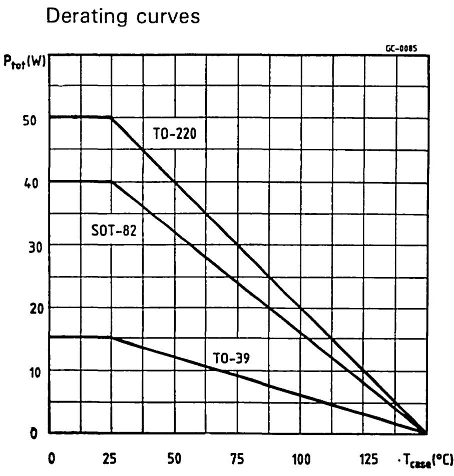
Normalized drain-source breakdown voltage vs. temperature



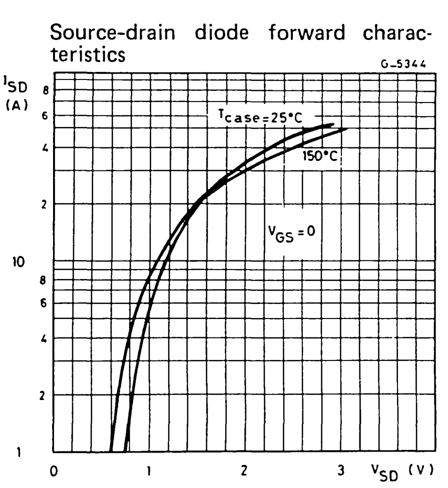
Capacitance variation



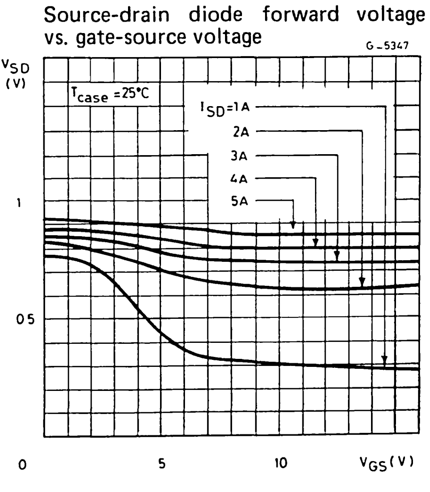
Derating curves



Source-drain diode forward characteristics



Source-drain diode forward voltage vs. gate-source voltage



SGSP 154/155/156
SGSP254/255/256
SGSP354/355/356

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

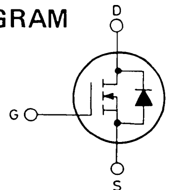
V_{DSS}	$R_{DS(ON)}$	I_D
350V/400V	5 Ω	1.5A
450V	6.5Ω	1.5A

ABSOLUTE MAXIMUM RATINGS

		TO-39 SOT-82 TO-220	SGSP154 SGSP254 SGSP354	SGSP155 SGSP255 SGSP355	SGSP156 SGSP256 SGSP356
V_{DS}	Drain-source voltage ($V_{GS} = 0$)		450V	400V	350V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)		450V	400V	350V
V_{GS}	Gate-source voltage			±20V	
I_D	Drain current (continuous) $T_{case} = 25°C$			1.5A	
	$T_{case} = 100°C$			1A	
I_{DM} (•)	Drain current (pulsed)			6A	
I_{DLM} (•)	Drain inductive current, clamped			6A	
			TO-39	SOT-82	TO-220
P_{tot}	Total power dissipation at $T_{amb} = 25°C$		15W	40W	50W
	Derating factor		0.4W/°C	0.32W/°C	0.12W/°C
T_{stg}	Storage temperature			-55 to 150°C	
T_j	Junction temperature			150°C	

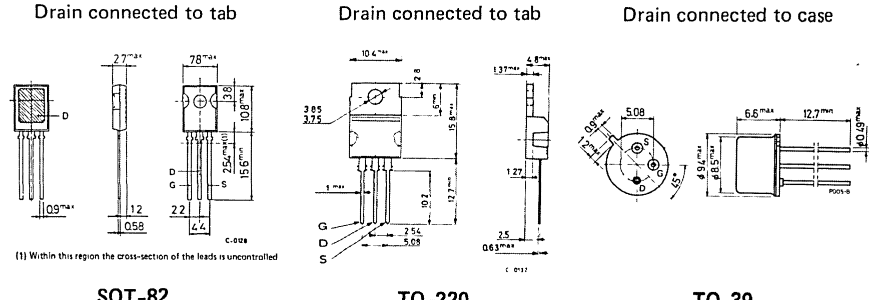
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



SOT-82 TO-220 TO-39

THERMAL DATA

			TO-39	SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8.3°C/W	2.5°C/W	3.12°C/W
T_L	Maximum lead temperature for soldering purpose			275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\,DSS}$	Drain-source breakdown voltage	I_D = 250 µA V_{GS} = 0				
		for **SGSP154/254/354**	450			V
		for **SGSP155/255/355**	400			V
		for **SGSP156/256/356**	350			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. rating			250	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
ON *						
$V_{GS\,(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	2		4	V
$V_{DS\,(on)}$	Drain-source voltage	V_{GS} = 10V I_D = 0.75A				
		for **SGSP154/254/354**			4.9	V
		for **SGSP155/255/355**			3.75	V
		for **SGSP156/256/356**			3.75	V
		T_{case} = 100°C				
		V_{GS} = 10V I_D = 0.75A				
		for **SGSP154/254/354**			9.8	V
		for **SGSP155/255/355**			7.5	V
		for **SGSP156/256/356**			7.5	V
$R_{DS\,(on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 0.75A				
		for **SGSP154/254/354**			6.5	Ω
		for **SGSP155/255/355**			5	Ω
		for **SGSP156/256/356**			5	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 0.75A	0.85			mho
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25V f = 1MHz		180	250	pF
C_{oss}	Output capacitance			30	45	pF
C_{rss}	Reverse transfer	V_{GS} = 0		15	25	pF

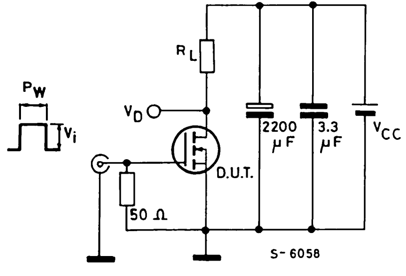
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 25V$ $V_G = 10V$		60		ns
t_r	Rise time	$I_D = 0.75A$ $R_i = 50\Omega$		60		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		60		ns
t_f	Fall time			80		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current				1.5	A
I_{SDM} (●)	Source-drain current (pulsed)				6	A
V_{SD}	Forward on voltage	$I_{SD} = 1.5A$ $V_{GS} = 0$			1.2	V
t_{on}	Turn-on time	$I_{SD} = 1.5A$ $V_{GS} = 0$		100		ns
t_{rr}	Reverse recovery time	$di/dt = 25A/\mu s$		70		ns

* Pulsed: pulse duration $\leqslant 300\mu s$, duty cycle $< 2\%$
(●) Pulse width limited by safe operating area

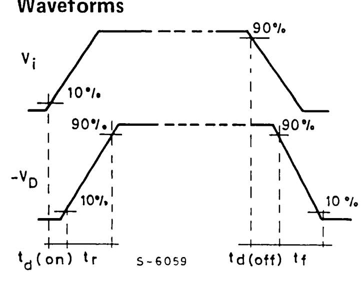
SWITCHING TIMES RESISTIVE LOAD

Test circuit



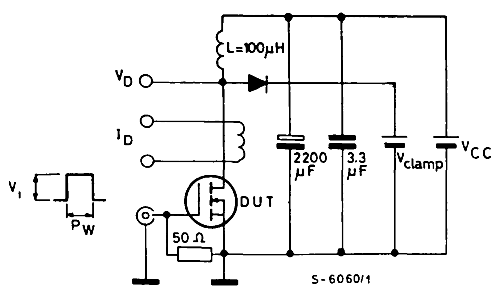
Pulse width $\leqslant 100\ \mu s$
Duty cycle $\leqslant 2\%$
$V_i = 10V$

Waveforms

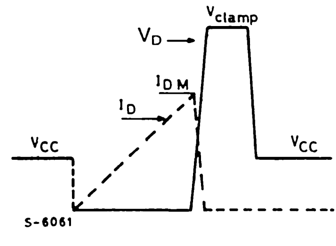


CLAMPED INDUCTIVE LOAD

Test circuit

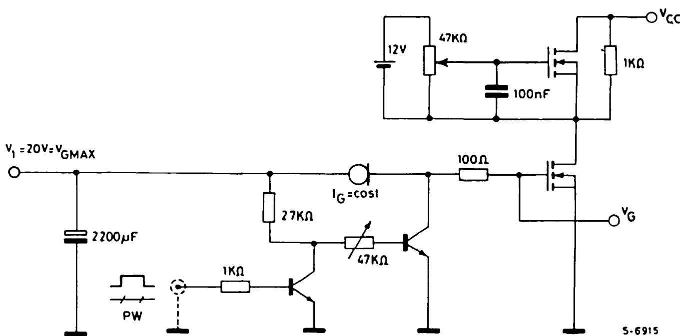


Waveforms



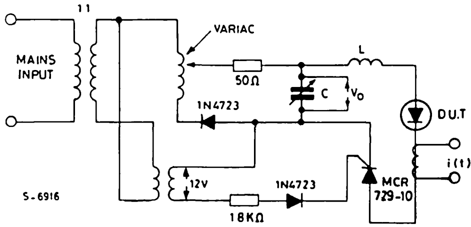
$V_I = 12V$
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



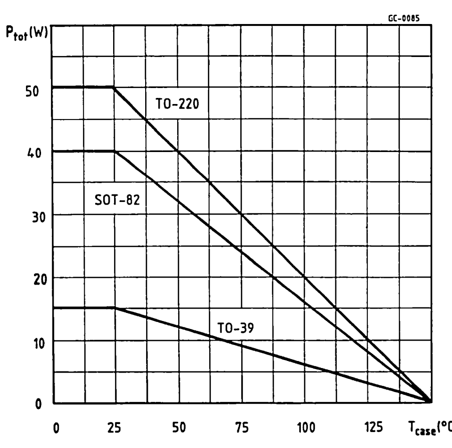
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

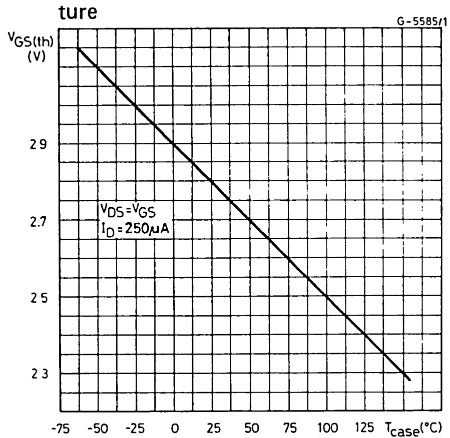


Jedec test circuit

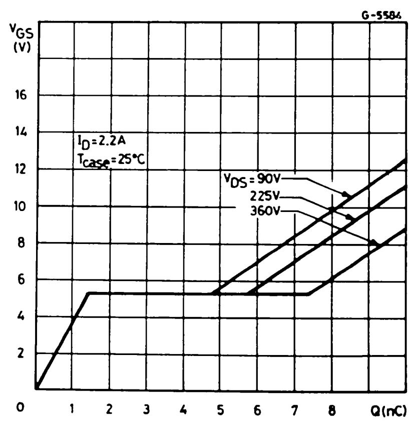
Derating curve



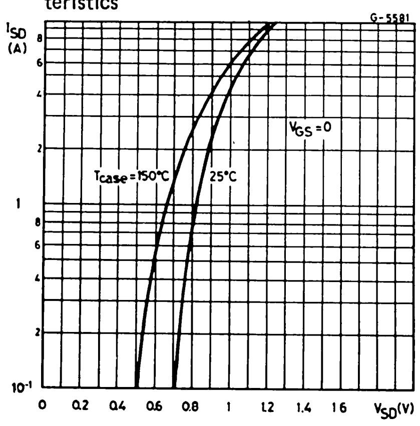
Gate threshold voltage vs. temperature



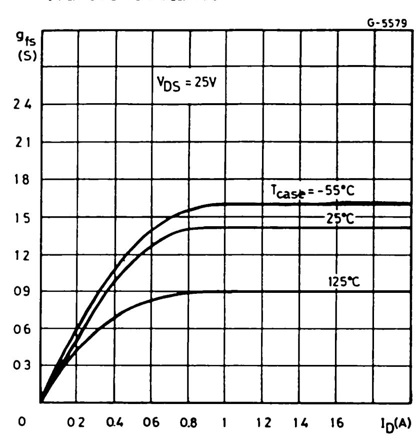
Gate charge vs. gate-source voltage



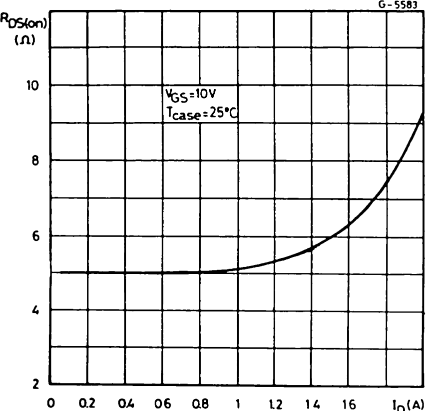
Source-drain diode forward characteristics



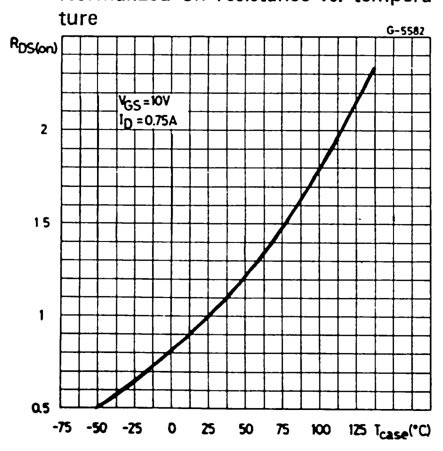
Transconductance

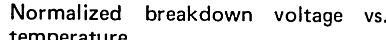


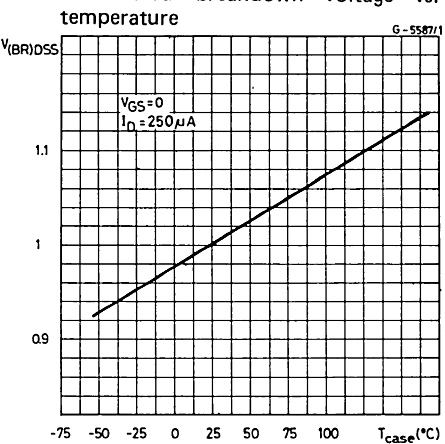
Static drain-source on resistance



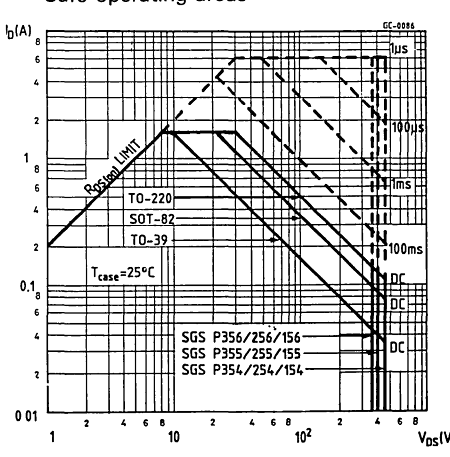
Normalized on resistance vs. temperature



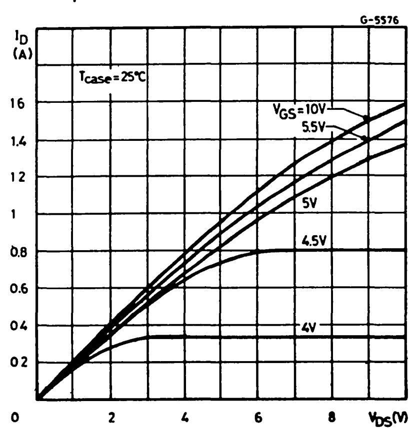

Normalized breakdown voltage vs. temperature



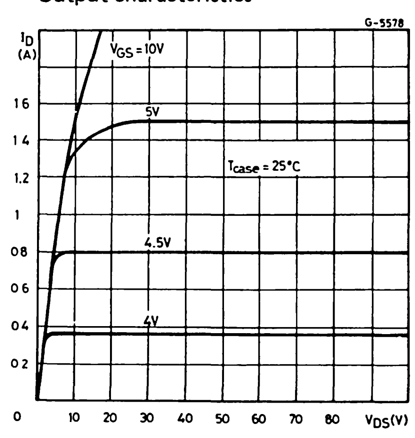
Safe operating areas



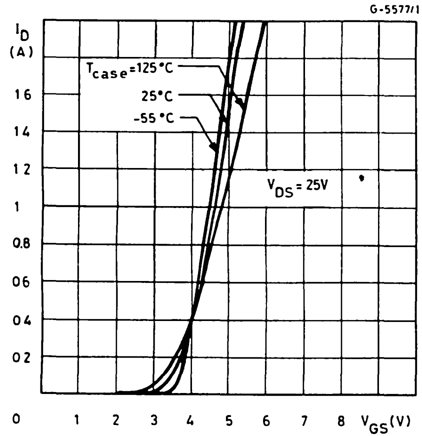
Output characteristics

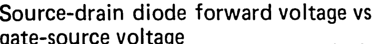


Output characteristics

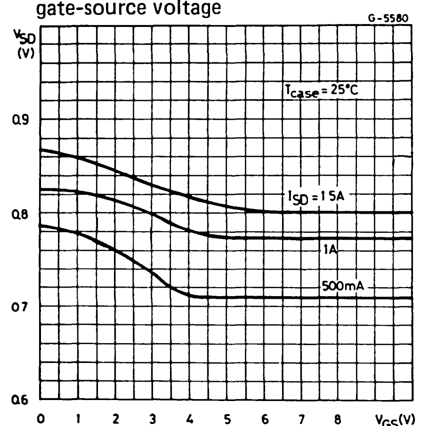


Transfer characteristics

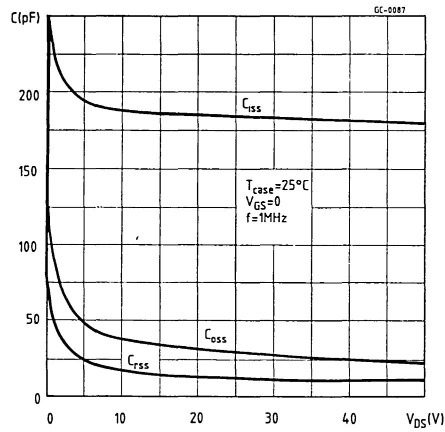




Source-drain diode forward voltage vs. gate-source voltage



Capacitance variation



SGSP157
SGSP158

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

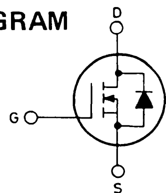
V_{DSS}	$R_{DS(ON)}$	I_D
50V/60V	0.3Ω	5A

ABSOLUTE MAXIMUM RATINGS

		SGSP157	SGSP158
V_{DS}	Drain-source voltage (V_{GS} = 0)	60V	50V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	60V	50V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
	T_{case} = 100°C	3.2A	
I_{DM}(•)	Drain current (pulsed)	20A	
I_{DLM} (•)	Drain inductive current, clamped	20A	
P_{tot}	Total power dissipation at T_{case} = 25°C	15W	
	Derating factor	0.12W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

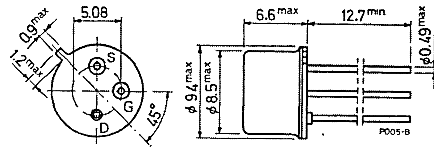
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-39

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	8.3 °C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP157** for **SGSP158**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2.5A I_D = 5A T_C = 100°C I_D = 2.5A			0.75 1.65 1.50	V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5A			0.3	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 2.5A	1.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		210 115 54	270 150 70	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

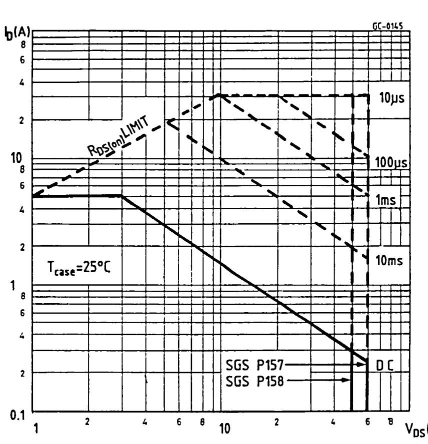
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25V I_D = 2.5A		10		ns
t_r	Rise time	V_i = 10V R_i = 4.7 Ω		25		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		15		ns
t_f	Fall time			10		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				5	A
I_{SDM}(•)	Source drain current (pulsed)				20	A
V_{SD}	Forward on voltage	I_{SD} = 5A V_{GS} = 0			1.80	V
t_{on}	Turn-on time	I_{SD} = 5A V_{GS} = 0		90		ns
t_{rr}	Reverse recovery	di/dt = 25A/μs		120		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

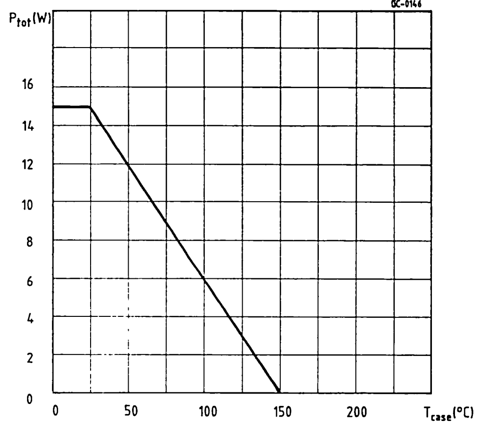
(•) Pulse width limited by safe operating area.

For typical curves and switching times resistive load, clamped inductive load, gate cherge, body drain diode trr measurement test circuits, see SGSP257 Datasheet.

Safe operating areas



Derating curve



SGSP211/P212
SGSP311/P312
SGSP511/P512

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

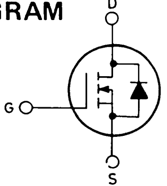
V_{DSS}	$R_{DS(ON)}$	I_D
80V/100V	0.3Ω	7A

ABSOLUTE MAXIMUM RATINGS

	SOT-82 TO-220 TO-3	SGSP211 SGSP311 SGSP511	SGSP212 SGSP312 SGSP512
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	100V	80V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	100V	80V
V_{GS}	Gate-source voltage	± 20V	
I_D	Drain current (continuous) at $T_{case} = 25°C$	7A	
	at $T_{case} = 100°C$	4.5A	
I_{DM} (•)	Drain current (pulsed)	28A	
I_{DLM} (•)	Drain inductive current, clamped	28A	
		SOT-82	TO-220/TO-3
P_{tot}	Total power dissipation at $T_{case} \leqslant 25°C$	50W	75W
	Derating factor	0.4W/ °C	0.6W/°C
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Junction temperature	150°C	

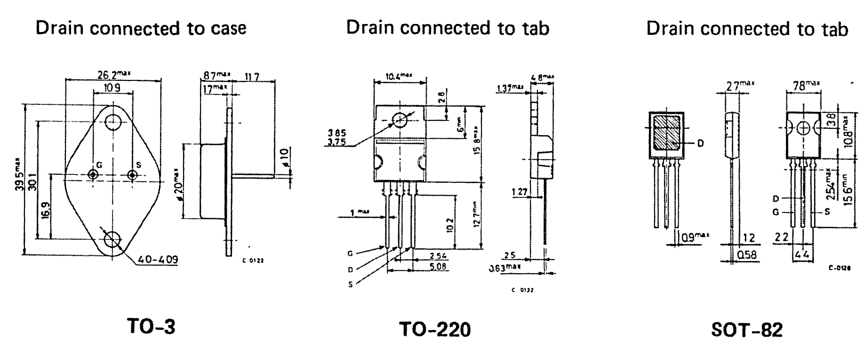
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

			TO-3/TO-220	SOT-82
$R_{th\ j-case}$	Thermal resistance junction-case	max	1.67°C/W	2.5°C/W
T_L	Maximum lead temperature for soldering purpose		275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA V_{GS} = 0 for **SGSP211/311/511** for **SGSP212/312/512**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
ON *						
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	2		4	V
$V_{DS(on)}$	Drain-source voltage	V_{GS} = 10V I_D = 3.5A I_D = 7A (T_{case} = 100°C) I_D = 3.5A			1.05 2.3 2.1	V V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 3.5A			0.3	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 3.5A	2			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1MHz V_{GS} = 0		375	480 230 110	pF pF pF

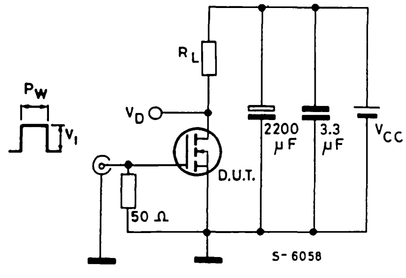
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 25V$ $V_i = 10V$		35		ns
t_r	Rise time	$I_D = 3.5A$ $R_i = 50\ \Omega$		80		ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				7	A
I_{SDM} (•)	Source drain current (pulsed)				28	A
V_{SD}	Forward on voltage	$I_{SD} = 7A$ $V_{GS} = 0$			1.35	V
t_{on}	Turn-on time	$I_{SD} = 7A$ $V_{GS} = 0$		150		ns
t_{rr}	Reverse recovery time	$di/dt = 25A/\mu s$		150		ns

* Pulsed: pulse duration ⩽ 300 μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area

SWITCHING TIMES RESISTIVE LOAD

Test circuit



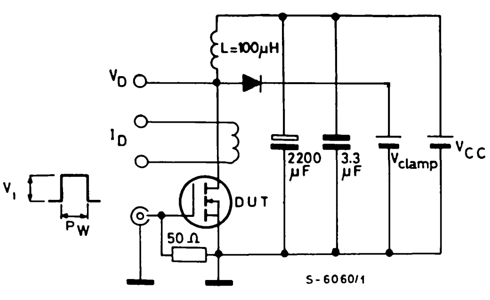
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10V$

Waveforms

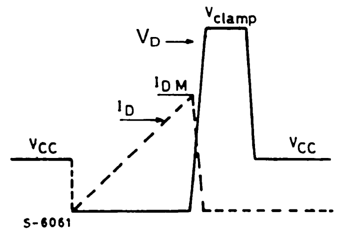
Vi
90%
10%
90%
90%
-VD
10%
10%
td(on) tr
S-6059
td(off) tf

CLAMPED INDUCTIVE LOAD

Test circuit

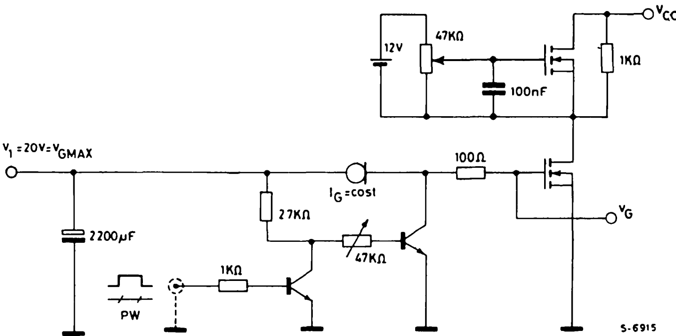


Waveforms



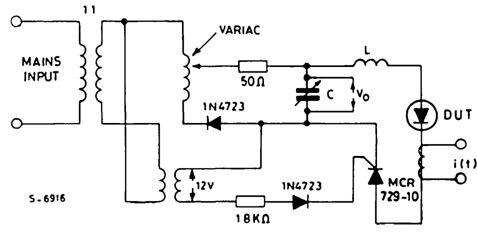
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



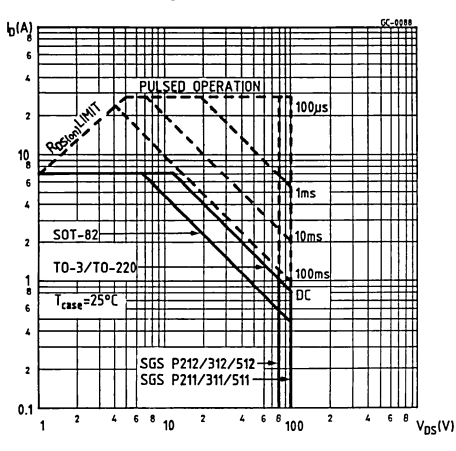
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

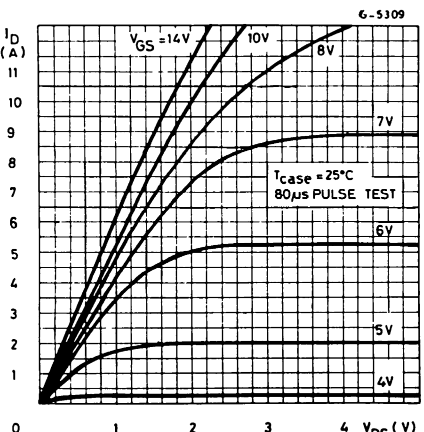


Jedec test circuit

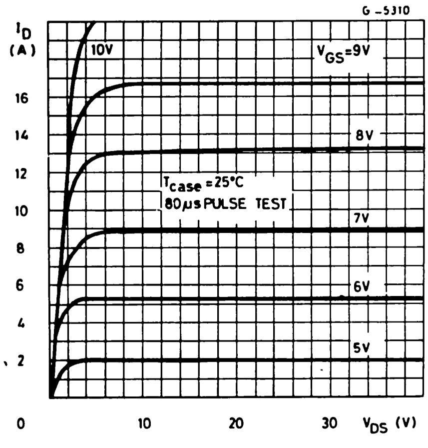
Safe operating areas



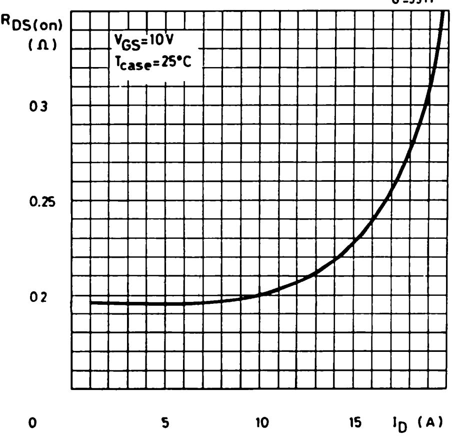
Output characteristics



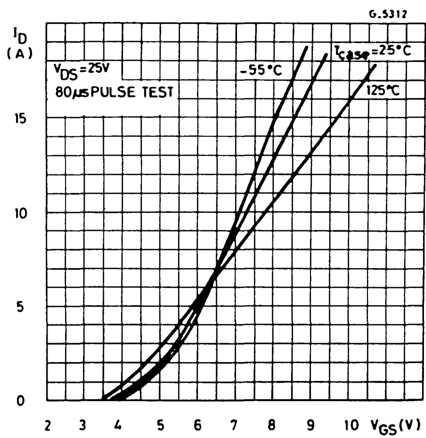
Output characteristics



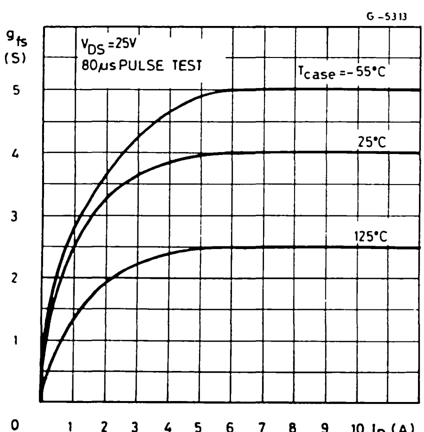
Static drain-source on resistance



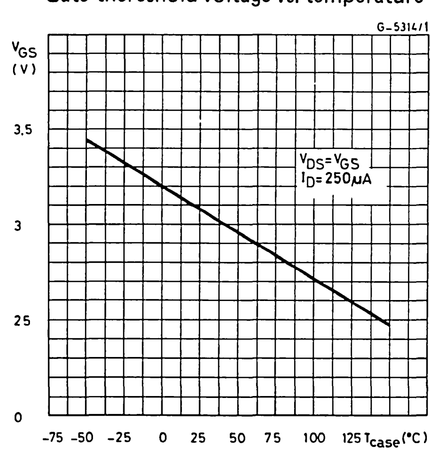
Transfer characteristics



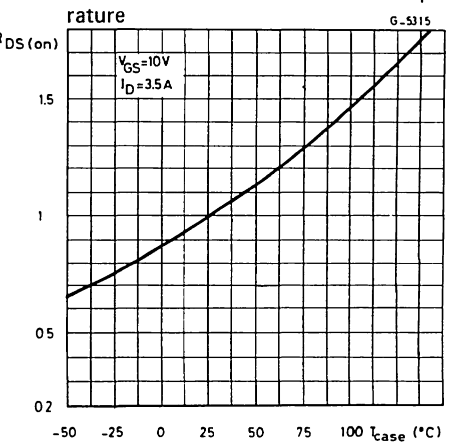
Transconductance



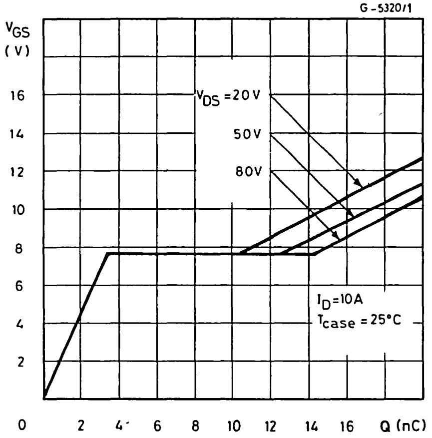
Gate thereshold voltage vs. temperature



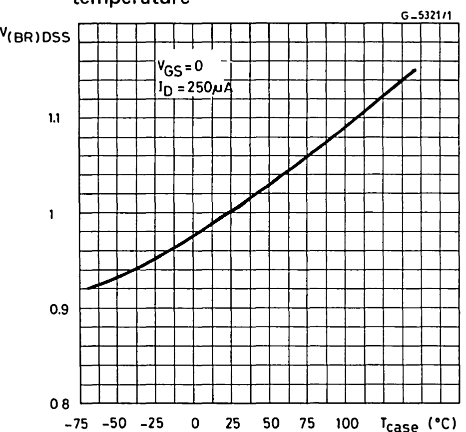
Normalized on resistance vs. temperature



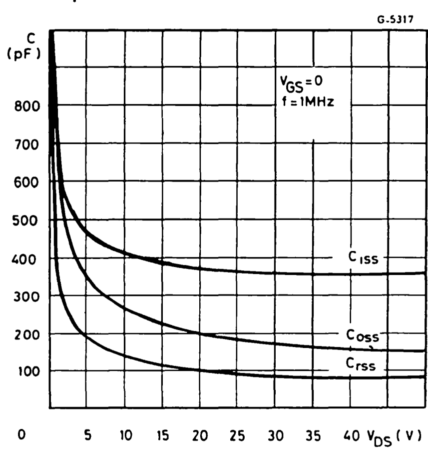
Gate charge vs. gate-source voltage



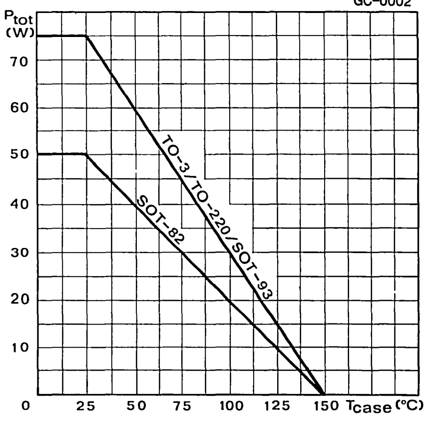
Normalized breakdown voltage vs. temperature



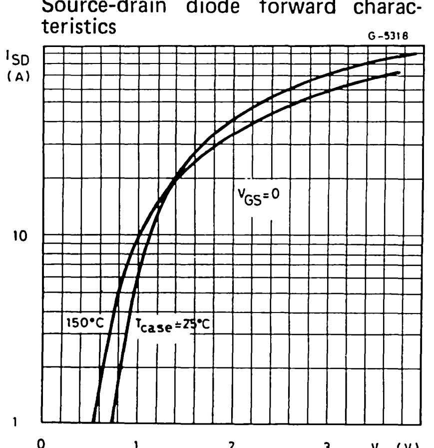
Capacitance variation



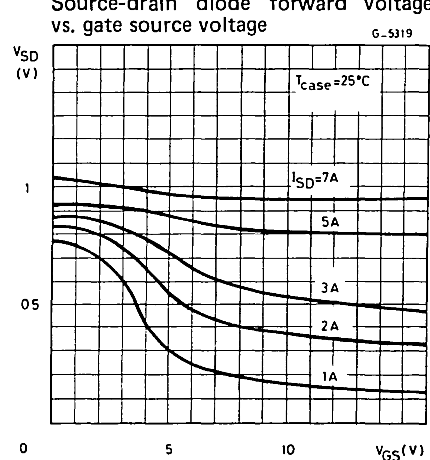
Derating curve



Source-drain diode forward characteristics



Source-drain diode forward voltage vs. gate source voltage



SGSP216/P217
SGSP316/P317
SGSP516/P517

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

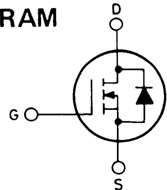
V_{DSS}	$R_{DS(ON)}$	I_D
200V	0.75Ω	6A
250V	1.2 Ω	6A

ABSOLUTE MAXIMUM RATINGS

	SOT-82 TO-220 TO-3	SGSP216 SGSP316 SGSP516		SGSP217 SGSP317 SGSP517
V_{DS}	Drain-source voltage (V_{GS} = 0)	250V		200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	250V		200V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		6A	
	at T_{case} = 100°C		3.8A	
I_{DM}(•)	Drain current (pulsed)		24A	
I_{DLM} (•)	Drain inductive current, clamped		24A	
		SOT-82	TO-220	TO-3
P_{tot}	Total dissipation at T_{case} = 25°C	50W	75W	75W
	Derating factor	0.4W/°C	0.6W/°C	0.6W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



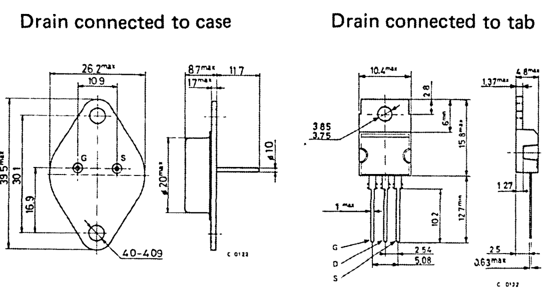
MECHANICAL DATA

Dimensions in mm

Drain connected to case

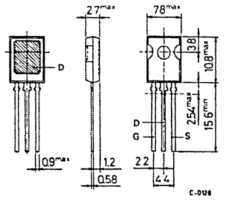
Drain connected to tab

Drain connected to tab



TO-3

TO-220



SOT-82

THERMAL DATA

			SOT-82	TO-220	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	2.5°C/W	1.6°C/W	1.6°C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP216/P316/P516** for **SGSP217/P317/P517**	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 3 A for **SGSP216/P316/P516** for **SGSP217/P317/P517** V_{GS} = 10 V I_D= 6 A for **SGSP216/P316/P516** for **SGSP217/P317/P517** V_{GS} = 10 V I_D = 3 A T_{case} =100°C for **SGSP216/P316/P516** for **SGSP217/P317/P517**			 3.60 2.25 8.10 5.00 7.20 4.50	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D =3 A for **SGSP216/P316/P516** for **SGSP217/P317/P517**			 1.20 0.75	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D =3 A	1.5			mho

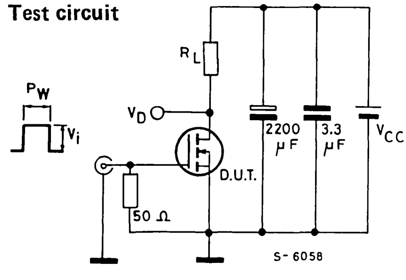
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25 V f= 1 MHz V_{GS} = 0		380	500	pF
C_{oss}	Output capacitance			100	130	pF
C_{rss}	Reverse transfer capacitance			50	65	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 100 V I_D = 2.5 A V_i = 10 V R_i = 50Ω (see test circuit)		27		ns
t_r	Rise time			27		ns
$t_{d\ (off)}$	Turn-off delay time			30		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				6	A
I_{SDM}(•)	Source drain current (pulsed)				24	A
V_{SD}	Forward on voltage	I_{SD} = 6 A V_{GS} = 0			1.3	V
t_{on}	Turn-on time	I_{SD} = 6 A V_{GS} = 0 di/dt = 100 A/μs		100		ns
t_{rr}	Reverse recovery time			180		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

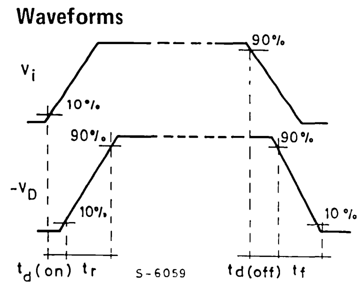
SWITCHING TIMES RESISTIVE LOAD

Test circuit



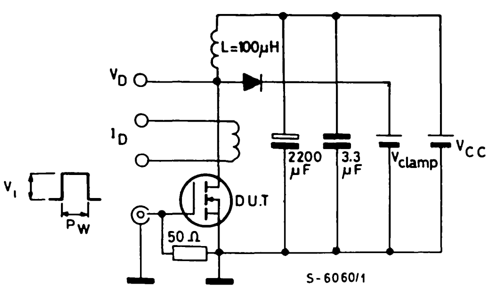
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

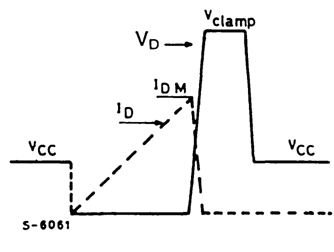
Waveforms



CLAMPED INDUCTIVE LOAD

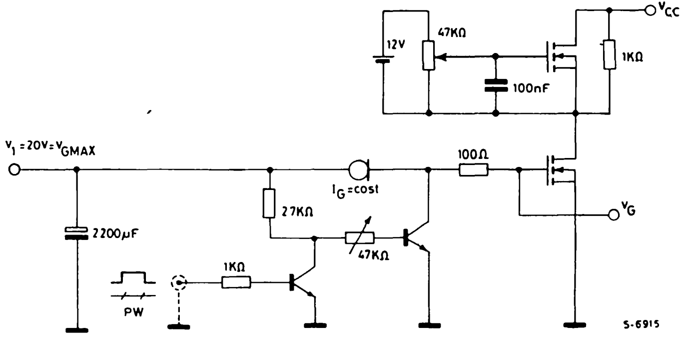
Test circuit **Waveforms**





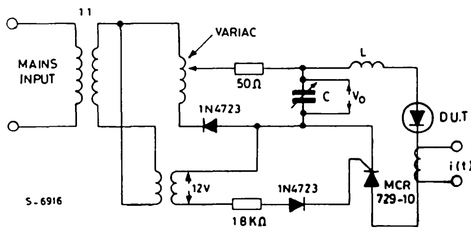
$V_i = 12V$
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



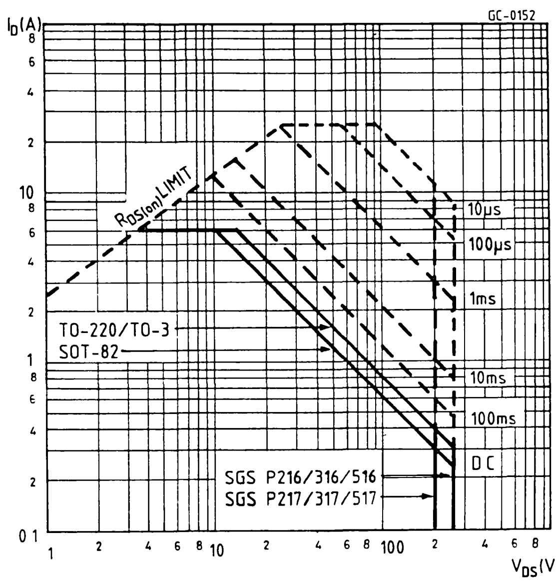
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

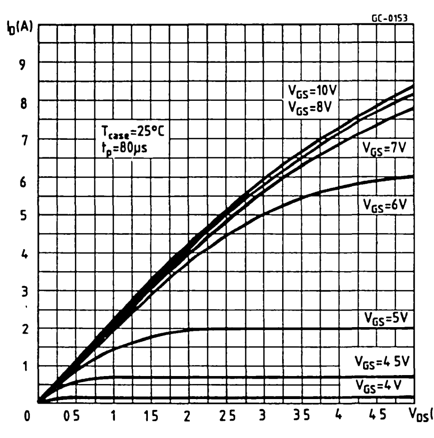


Jedec test circuit

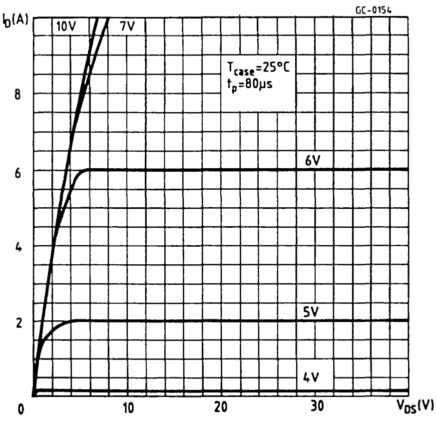
Safe operating areas



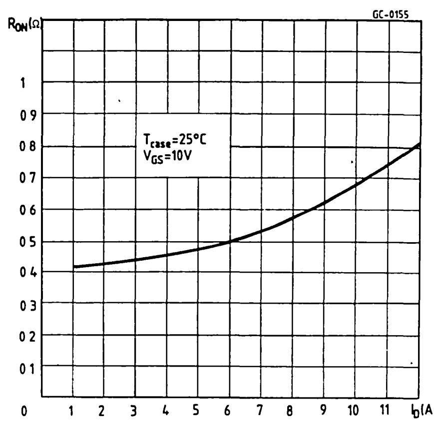
Output characteristics



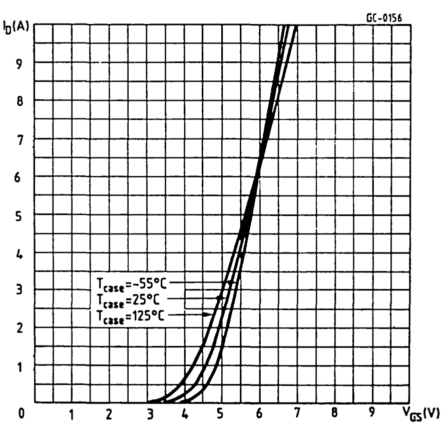
Output characteristics



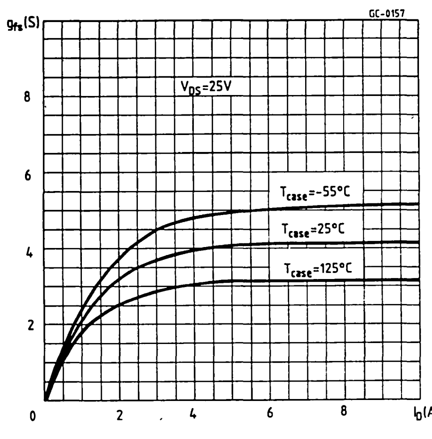
Static drain-source on resistance



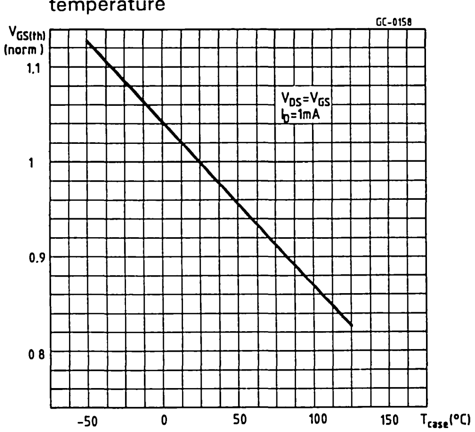
Transfer characteristics

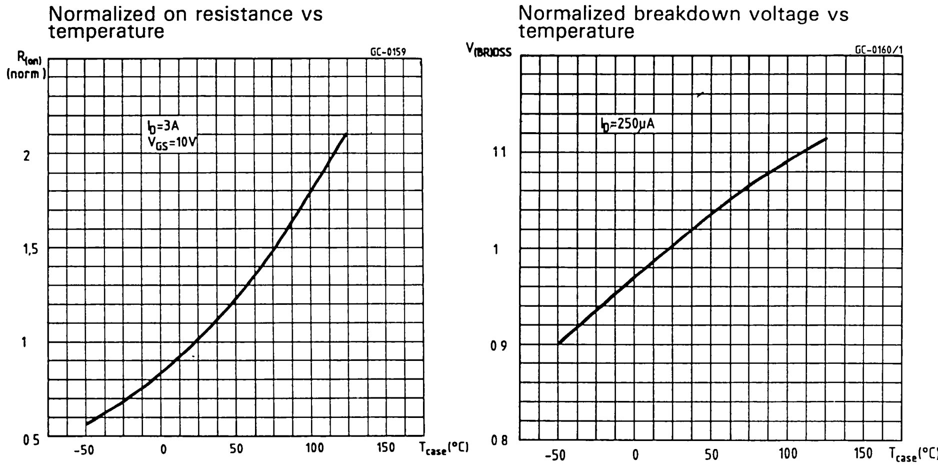


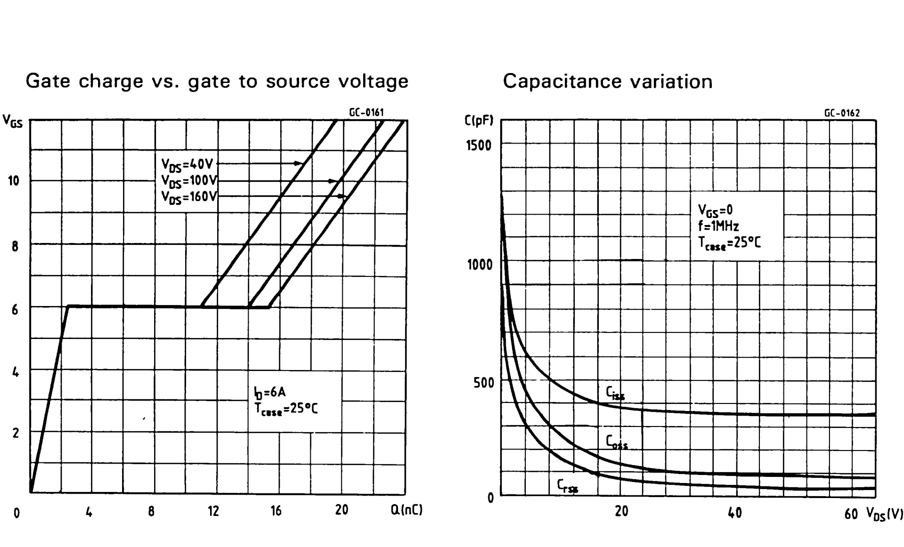
Transconductance



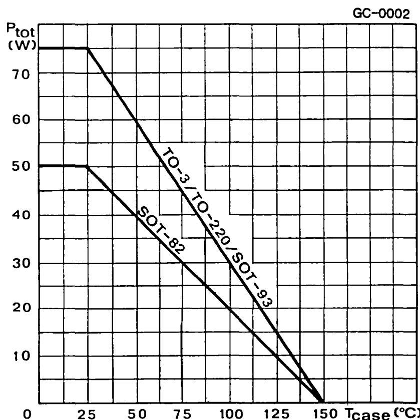
Normalized gate thereshold vs. temperature



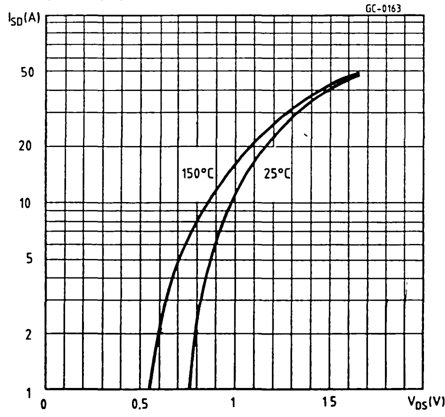

Normalized on resistance vs temperature
GC-0159
R(on) (norm)
ID=3A
VGS=10V
2
1,5
1
0 5
-50
0
50
100
150
Tcase(°C)
Normalized breakdown voltage vs temperature
GC-0160/1
V(BR)DSS
ID=250μA
1 1
1
0 9
0 8
-50
0
50
100
150
Tcase(°C)


Gate charge vs. gate to source voltage
GC-0161
VGS
VDS=40V
VDS=100V
VDS=160V
ID=6A
Tcase=25°C
10
8
6
4
2
0
4
8
12
16
20
Q(nC)
Capacitance variation
GC-0162
C(pF)
1500
1000
500
0
VGS=0
f=1MHz
Tcase=25°C
Ciss
Coss
Crss
20
40
60
VDS(V)

Derating curve



Source-drain diode forward characteristics



SGSP221/P222
SGSP321/P322
SGSP421/P422
SGSP521/P522

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

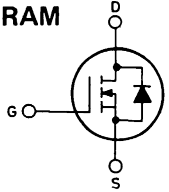
V_{DSS}	$R_{DS(ON)}$	I_D
50V/60V	0.13Ω	10A

ABSOLUTE MAXIMUM RATINGS

		SOT-82 TO-220 SOT-93 TO-3	SGSP221 SGSP321 SGSP421 SGSP521	SGSP222 SGSP322 SGSP422 SGSP522
V_{DS}	Drain-source voltage (V_{GS} = 0)		60V	50V
V_{DGR}	Drain gate voltage (R_{GS} = 20KΩ)		60V	50V
V_{GS}	Gate-source voltage		± 20V	
I_D	Drain current (continuous) at T_{case} = 25°C		10A	
	at T_{case} = 100°C		6.5A	
I_{DM} (•)	Drain current (pulsed)		40A	
I_{DLM} (•)	Drain inductive current, clamped		40A	
			SOT-82	TO-220/SOT93/TO-3
P_{tot}	Total power dissipation at $T_{case} \leqslant 25$°C		50W	75W
	Derating factor		0.4W/°C	0.6W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Junction temperature		150°C	

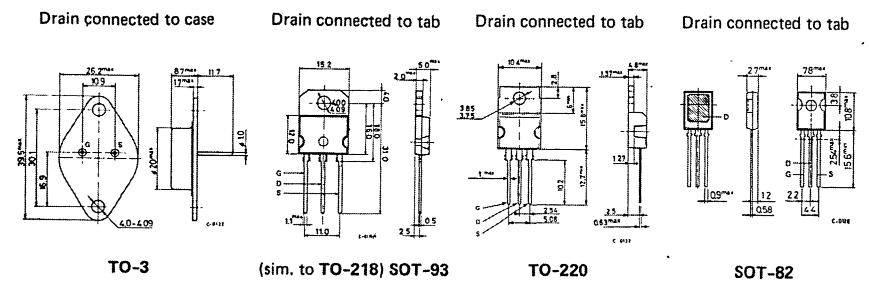
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



TO-3 | (sim. to TO-218) SOT-93 | TO-220 | SOT-82

THERMAL DATA

			TO220/SOT-93/TO-3	SOT-82
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1.67°C/W	2.5°C/W
T_L	Max. lead temp. for soldering purpose		275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP221/321/421/521** for **SGSP222/322/422/522**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
ON *						
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ I_D = 250 μA	2		4	V
$V_{DS(on)}$	Drain-source voltage	V_{GS} = 10V I_D = 5A $I_D \doteq$ 10A (T_{case} = 100°C) I_D = 5A			0.65 1.4 1.3	V V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 5A			0.13	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 5A	3			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1MHz		460	550 350 180	pF pF pF

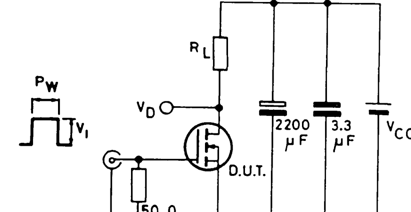
ELECTRICAL CHARACTERISTICS (Continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d(on)}$	Turn-on delay time	V_{cc} = 25V V_i = 10V		30		ns
t_r	Rise time	I_D = 5A R_i = 50 Ω		130		ns
$t_{d(off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			130		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current				10	A
I_{SDM} (•)	Source-drain current (pulsed)				40	A
V_{SD}	Forward on voltage	I_{SD} = 10A V_{GS} = 0			1.4	V
t_{on}	Turn-on time	di/dt = 25A/μs		60		ns
t_{rr}	Reverse recovery time	I_{SD} = 10A V_{GS} = 0		100		ns

* Pulsed: pulse duration ⩽ 300 μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area

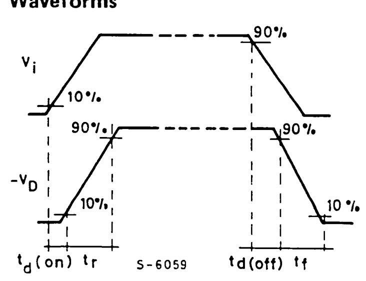
SWITCHING TIMES RESISTIVE LOAD

Test circuit



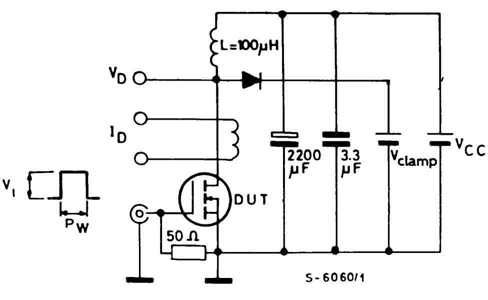
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms

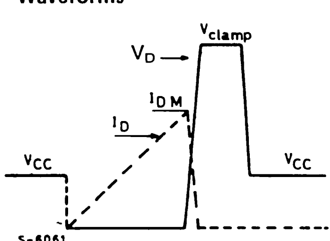


CLAMPED INDUCTIVE LOAD

Test circuit

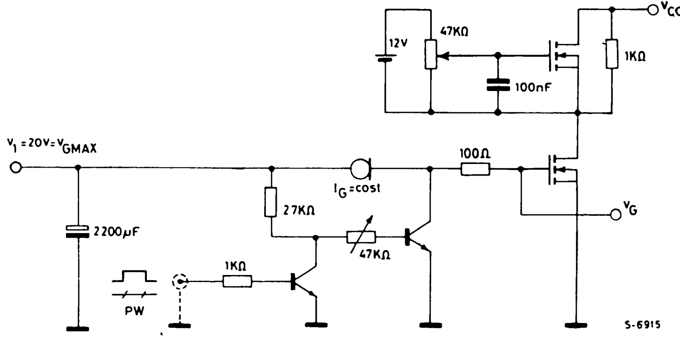


Waveforms



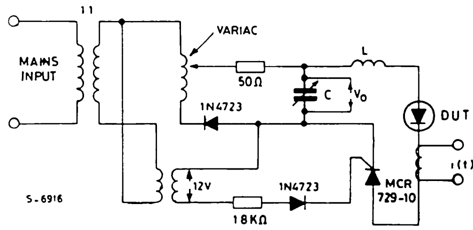
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



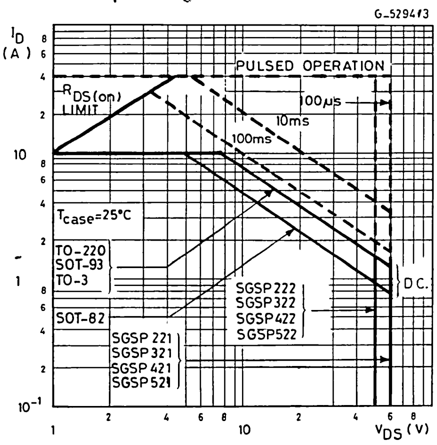
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

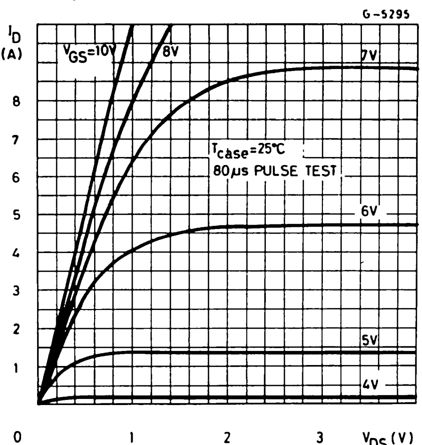


Jedec test circuit

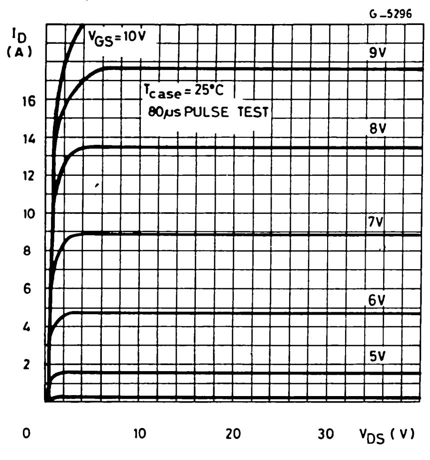
Safe operating areas



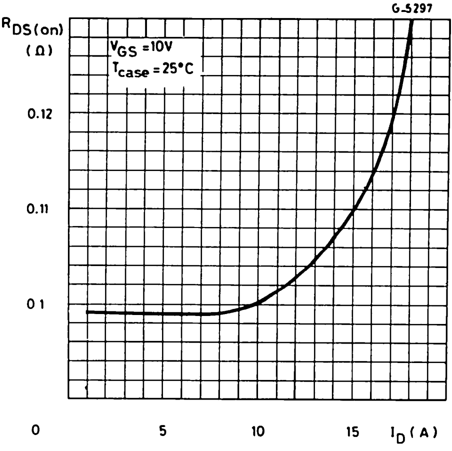
Output characteristics



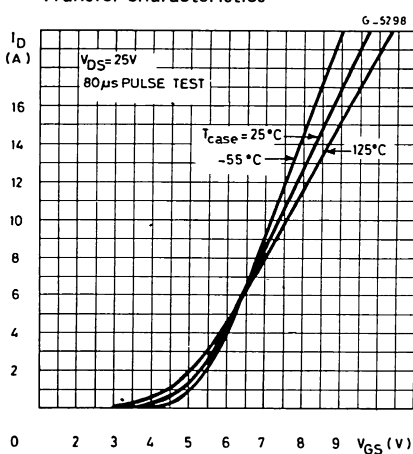
Output characteristics



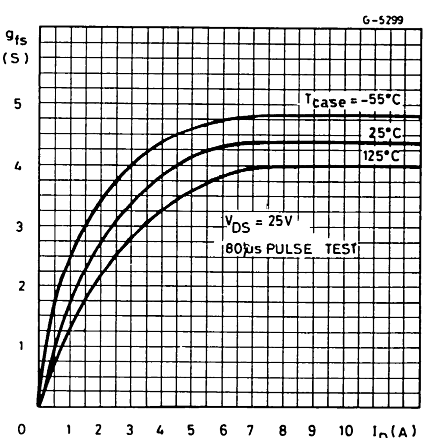
Static drain-source on resistance



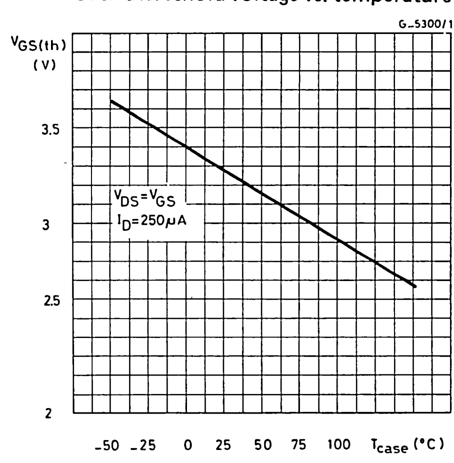
Transfer characteristics



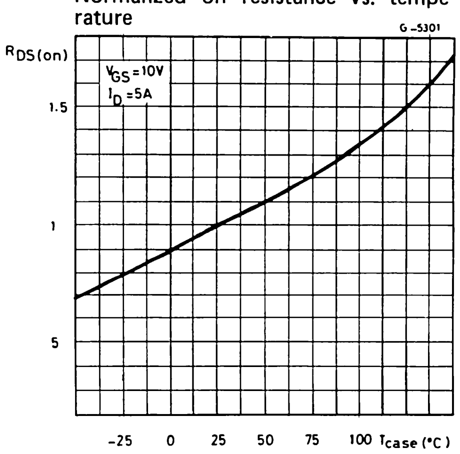
Transconductance



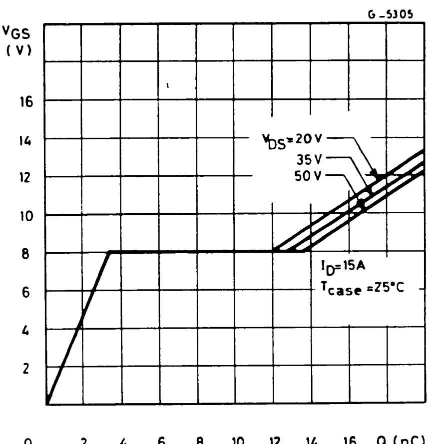
Gate thereshold voltage vs. temperature



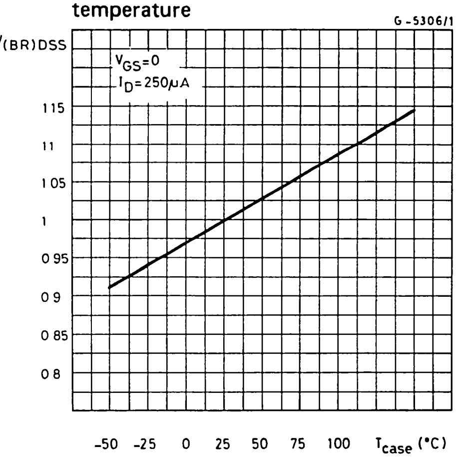
Normalized on resistance vs. temperature



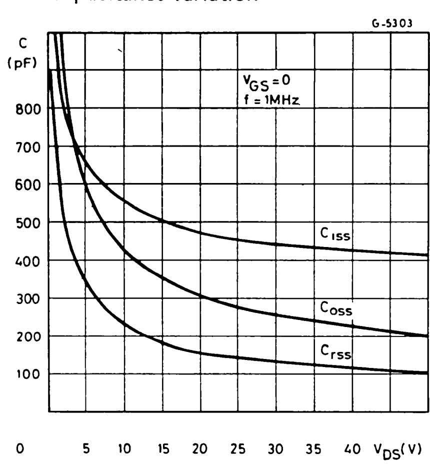
Gate charge vs. gate-source voltage



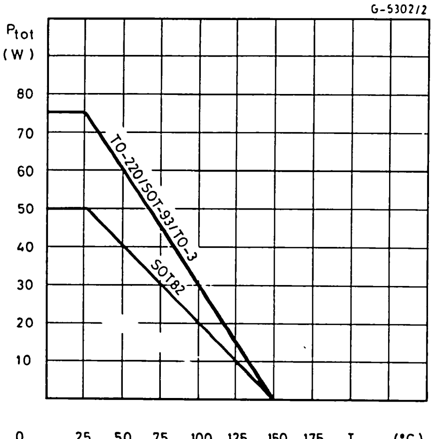
Normalized breakdown voltage vs. temperature



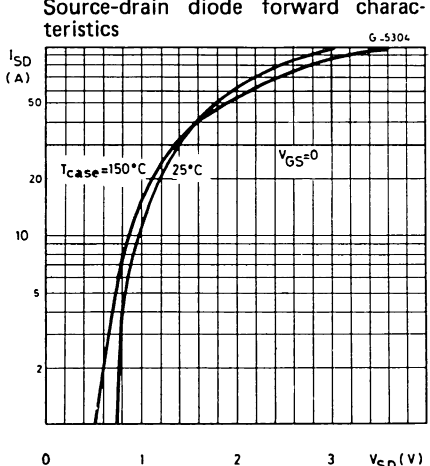
Capacitance variation



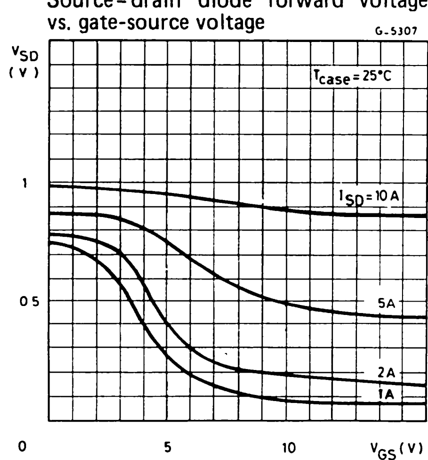
Derating curve



Source-drain diode forward characteristics



Source-drain diode forward voltage vs. gate-source voltage



SGSP257/P258
SGSP357/P358

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

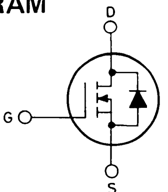
V_{DSS}	$R_{DS(ON)}$	I_D
50V/60V	0.3Ω	7A

ABSOLUTE MAXIMUM RATINGS

	SOT-82 TO-220	SGSP257 SGSP357	SGSP258 SGSP358
V_{DS}	Drain-source voltage (V_{GS} = 0)	60V	50V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	60V	50V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	7A	
	at T_{case} = 100°C	4.4A	
I_{DM}(•)	Drain current (pulsed)	28A	
I_{DLM} (•)	Drain inductive current, clamped	28A	
		SOT-82	TO-220
P_{tot}	Total power dissipation at T_{case} = 25°C	40W	50W
	Derating factor	0.32W/°C	0.40W/°C
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

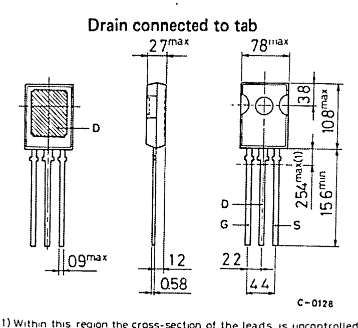
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM

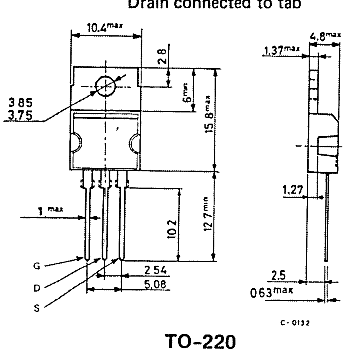


MECHANICAL DATA

Dimensions in mm



SOT-82



TO-220

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W	2.5°C/W
T_L	Maximum lead temperature for soldering purpose		275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP257/P357** for **SGSP258/P358**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 3.5A I_D = 7 A T_{case} = 100°C I_D = 3.5 A			1.05 2.30 2.10	 V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 3.5 A			0.3	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 3.5 A	1.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f= 1 MHz V_{GS} = 0		210 115 54	270 150 70	pF pF pF

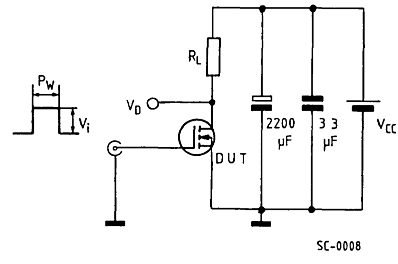
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 25 V I_D = 3.5 A		10		ns
t_r	Rise time	V_i = 10 V R_i = 4.7Ω		25		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		15		ns
t_f	Fall time			10		ns
SOURCE DRAIN DIODE						
I_{SD}	Source-Drain current				7	A
I_{SDM}(•)	Source drain current (pulsed)				28	A
V_{SD}	Forward on voltage	I_{SD} = 7 A V_{GS} = 0			1.4	V
t_{on}	Turn-on time	I_{SD} = 7 A V_{GS} = 0		90		ns
t_{rr}	Reverse recovery time	di/dt = 25 A/μs		120		ns

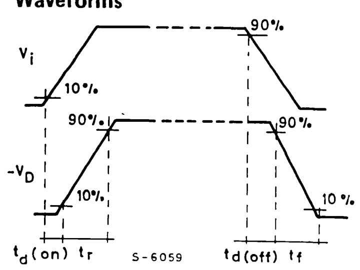
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



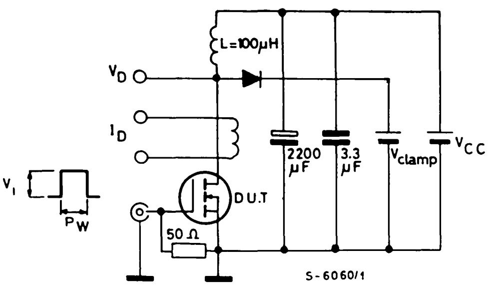
Waveforms



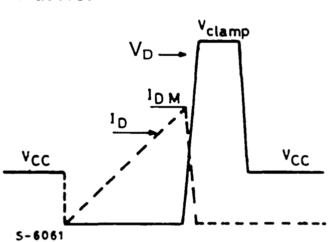
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

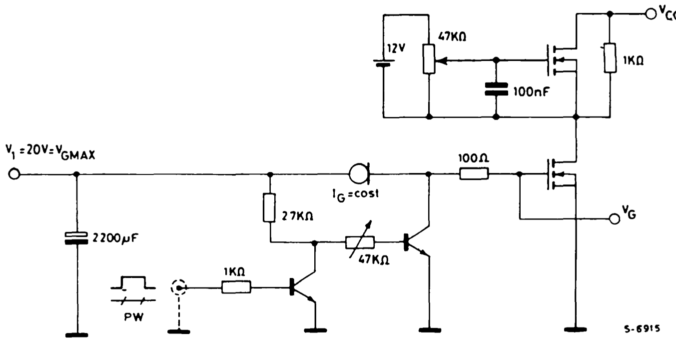


Waveforms



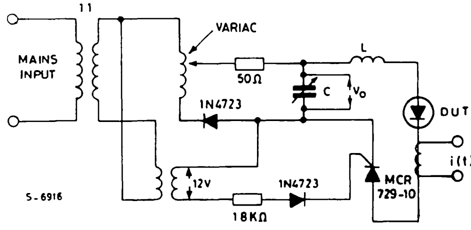
$V_I = 12V$
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



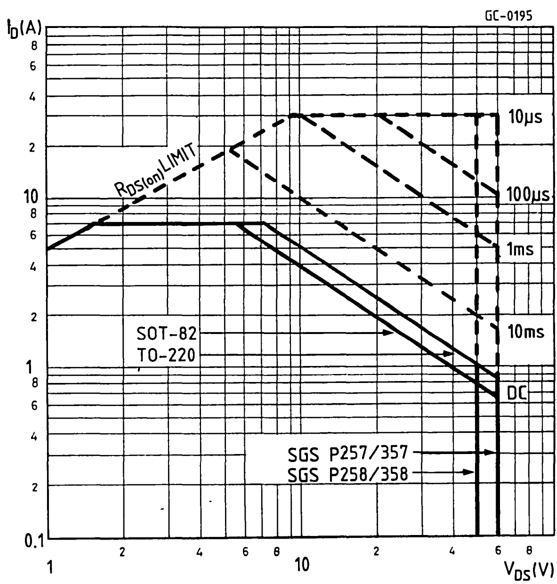
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

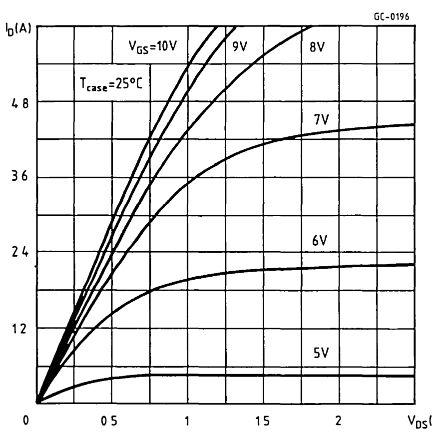


Jedec test circuit

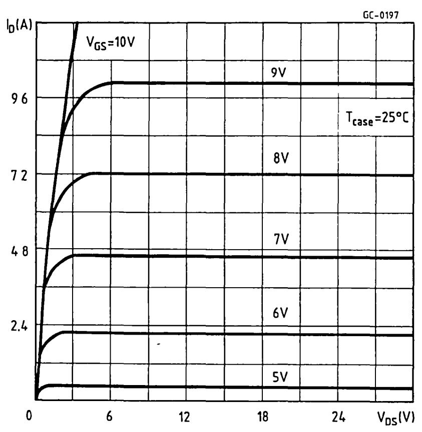
Safe operating areas



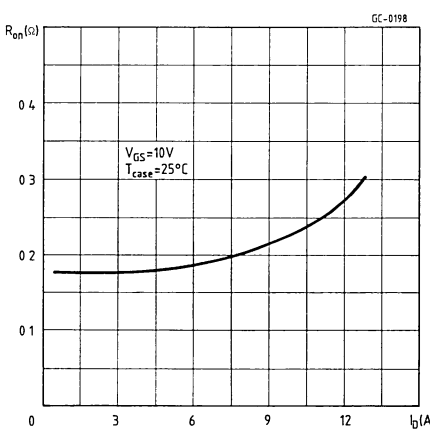
Output characteristics.



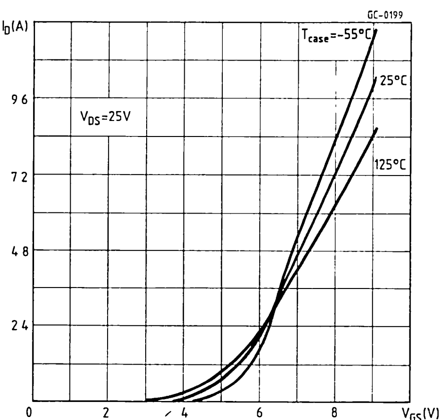
Output characteristics.



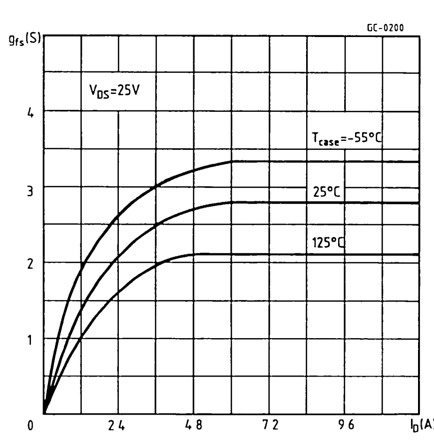
Static drain source on resistance.



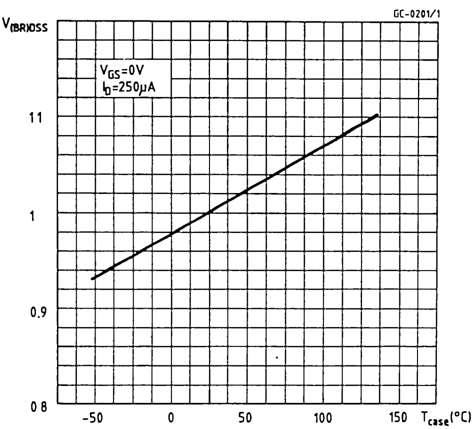
Transfer characteristics.



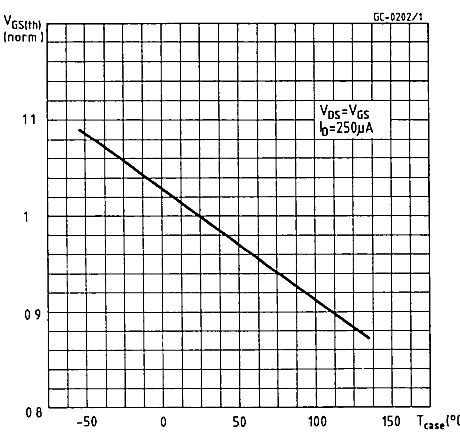
Transconductance.



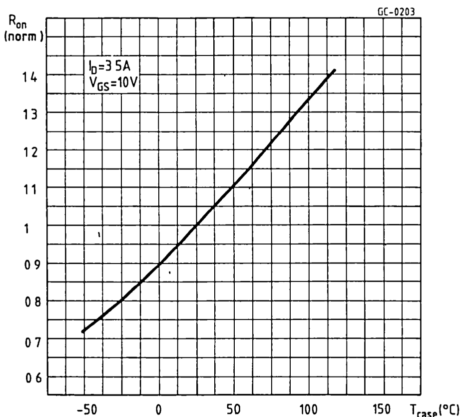
Normalized breakdown voltage vs. temp.



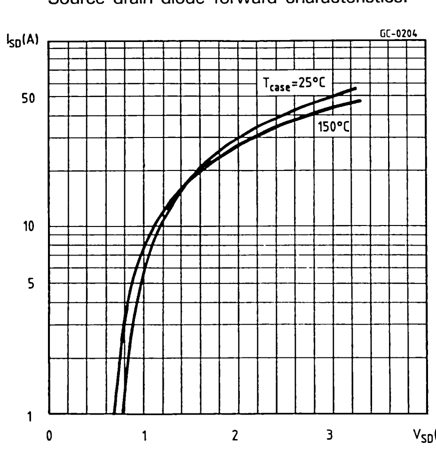
Normalized gate threshold voltage vs. temp.



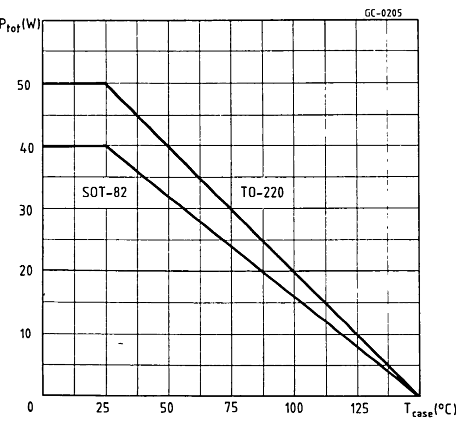
Normalized on resistance vs temperature.



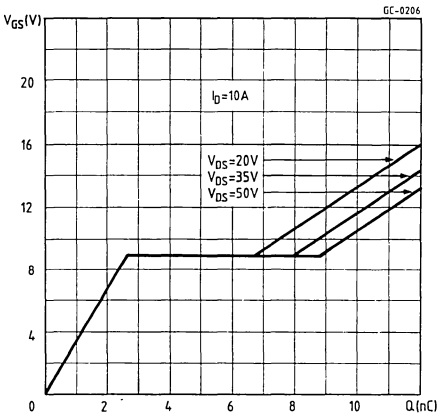
Source drain diode forward characteristics.



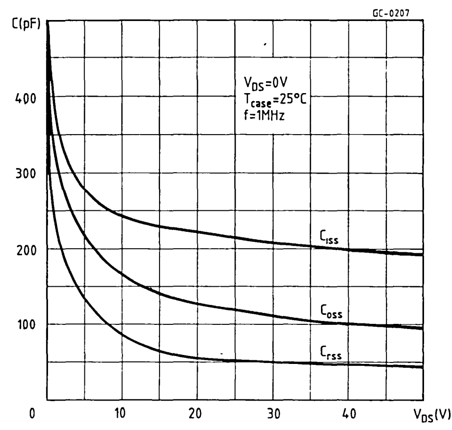
Derating curves.



Gate charge vs. gate to source voltage.



Capacitances variation.



SGSP361/P461/P561
SGSP362/P462/P562

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

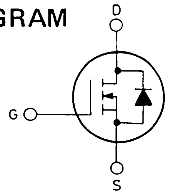
V_{DSS}	$R_{DS(ON)}$	I_D
80V	0.1 Ω	16A
100V	0.15Ω	16A

ABSOLUTE MAXIMUM RATINGS

TO-220 SOT-93 TO-3		SGSP361 SGSP461 SGSP561	SGSP362 SGSP462 SGSP562
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	80V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	100V	80V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	16A	
	T_{case} = 100°C	10A	
I_{DM} (•)	Drain current (pulsed)	64A	
I_{DLM} (•)	Drain inductive current, clamped	64A	
		TO-220	SOT-93/TO-3
P_{tot}	Total power dissipation at T_{case} = 25°C	100 W	125W
	Derating factor	0,8W/°C	1W/°C
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Junction temperature	150°C	

(•) Pulsed width limited by safe operating area.

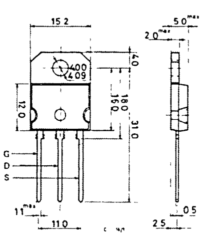
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

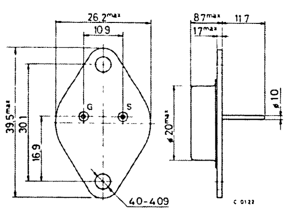
Dimensions in mm

Drain connected to tab



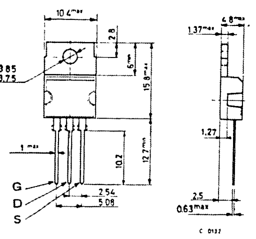
(sim. to TO-218) SOT-93

Drain connected to case



TO-3

Drain connected to tab



TO-220

THERMAL DATA

			TO-220	SOT-93/TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.25°C/W	1°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP361/461/561** for **SGSP362/462/562**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{DS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 8A for **SGSP362/462/562** for **SGSP361/461/561** V_{GS} = 10V I_D = 16A for **SGSP362/462/562** for **SGSP361/461/561** T_{case}= 100°C I_D = 8A for **SGSP362/462/562** for **SGSP361/461/561**			 0.80 1.20 1.70 2.50 1.60 2.40	 V V V V V V
$R_{DS\ (on)}$	Static drain-source	V_{GS} = 10 V I_D =8A for **SGSP362/462/562** for **SGSP361/461/561**			 0.10 0.15	 Ω Ω
g_{fs}	Forward transconduc.	V_{DS} = 25V I_D =8A	4.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V f=1MHz V_{GS} =0		950 370 180	1200 480 230	pF pF pF

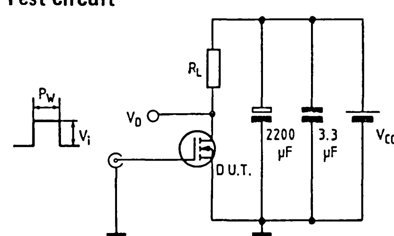
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 36V V_i = 10V		25		ns
t_r	Rise time	I_D = 8A R_i = 4.7Ω		30		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		40		ns
t_f	Fall time			15		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				16	A
I_{SDM}(•)	Source drain current (pulsed)				64	A
V_{SD}	Forward on voltage	I_{SD} = 16A V_{GS} = 0			1.35	V
t_{on}	Turn-on time	I_{SD} = 16A V_{GS} = 0		140		ns
t_{rr}	Reverse recovery	di/dt = 100A/μs		150		ns

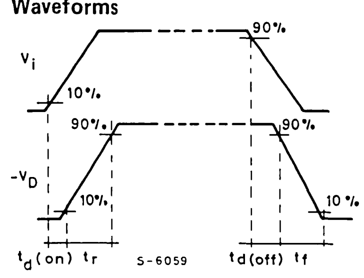
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



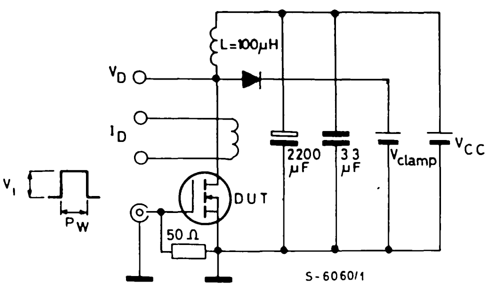
Waveforms



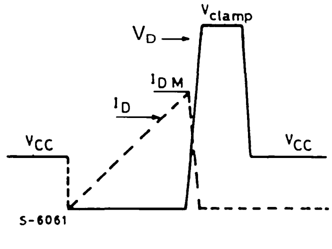
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit



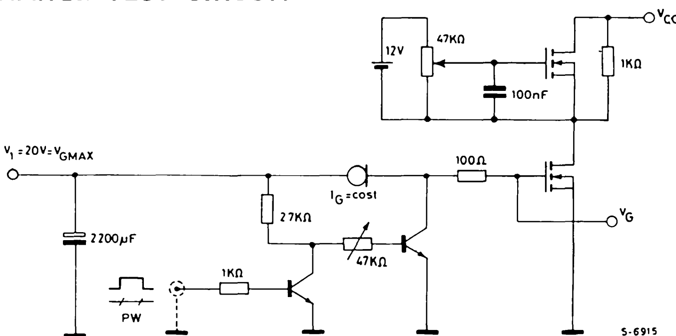
Waveforms



$V_I = 12V$

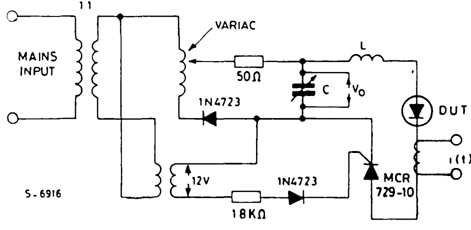
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



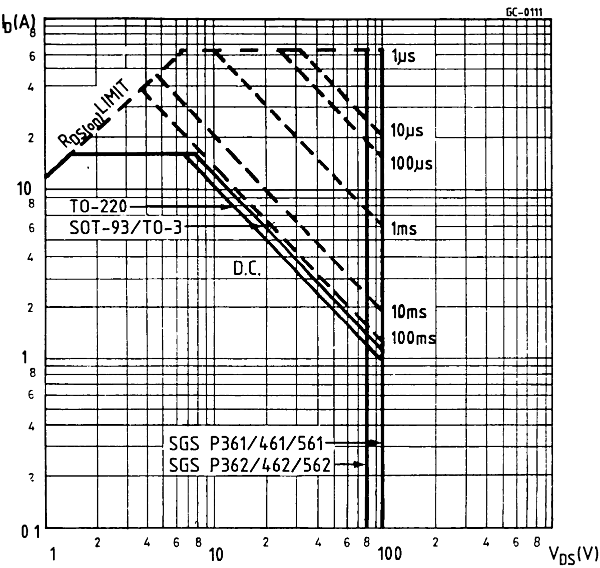
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

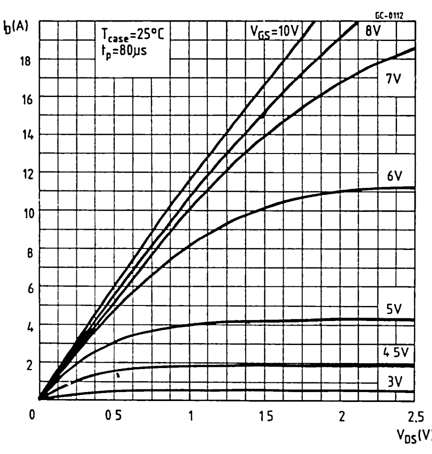


Jedec test circuit

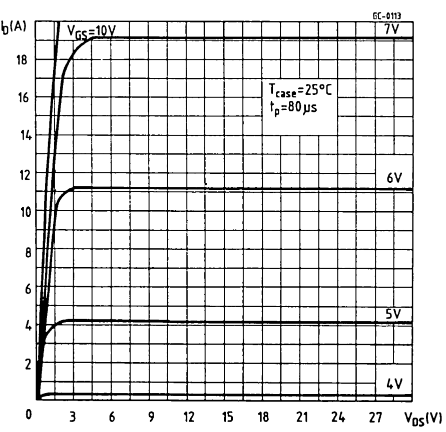
Safe operating areas



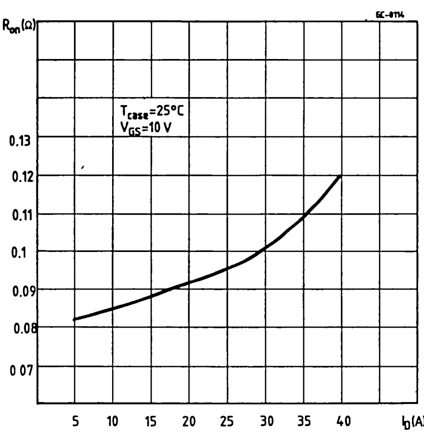
Output characteristics



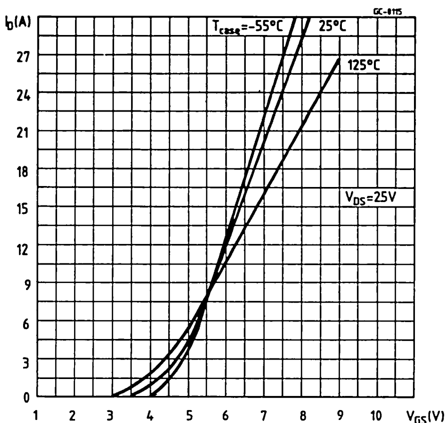
Output characteristics



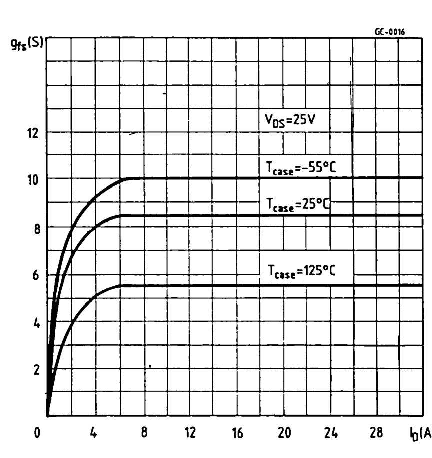
Static drain-source on resistance



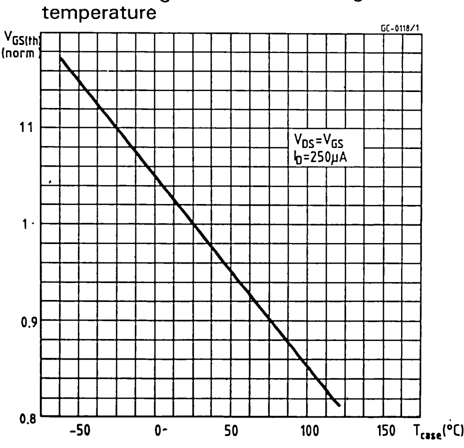
Transfer characteristics

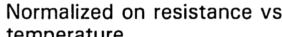


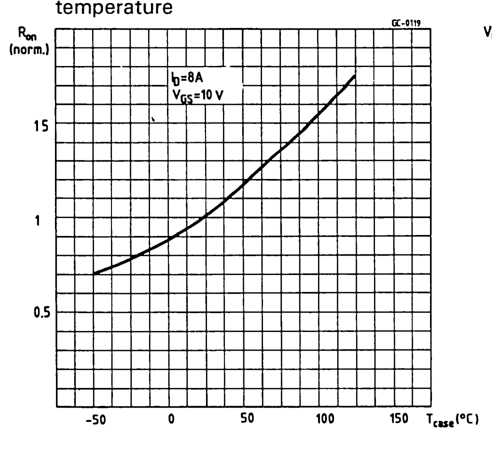
Transconductance

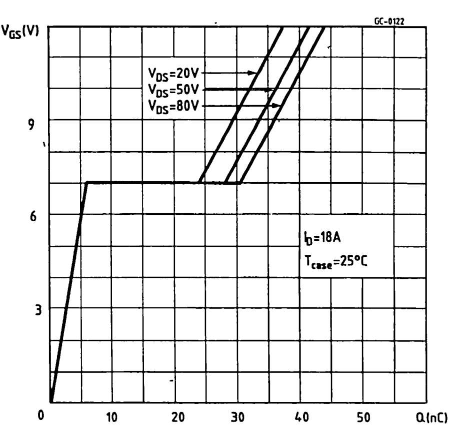


Normalized gate threshold voltage vs. temperature









Normalized breakdown voltage vs. temperature

GC-0117/1

V(BR)DSS

ID=250μA

11

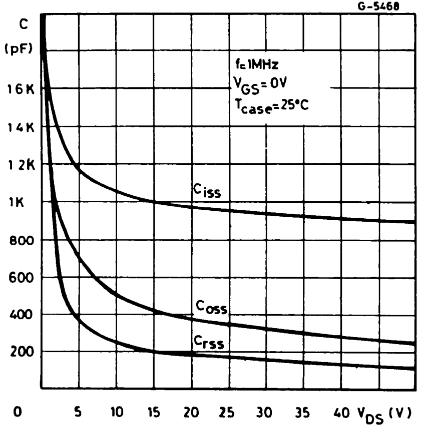
1

0.9

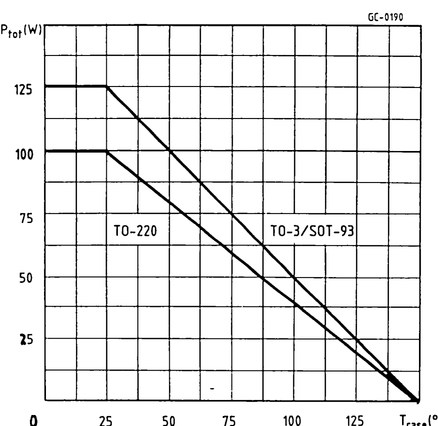
0.8

-50 0 50 100 150 Tcase(°C)

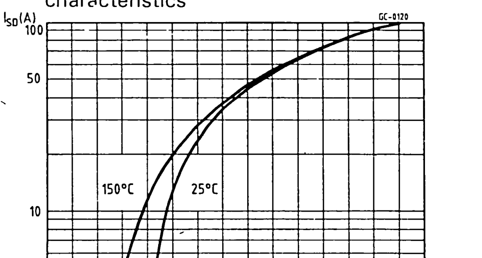
Capacitance variation



Derating curves



Source-drain diode forward characteristics



SGSP363/P367
SGSP463/P467
SGSP563/P567

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	$R_{DS(ON)}$	I_D
200V	0.33Ω	10A
250V	0.45Ω	10A

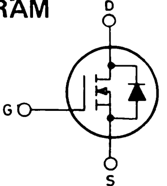
ABSOLUTE MAXIMUM RATINGS

	TO-220 SOT-93 TO-3	SGSP363 SGSP463 SGSP563	SGSP367 SGSP467 SGSP567
V_{DS}	Drain-source voltage (V_{GS} = 0)	250V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	250V	200V
V_{GS}	Gate-source voltage	± 20V	
I_D	Drain current (continuous) T_{case} = 25°C	10A	
	T_{case} = 100°C	6.4A	
I_{DM} (•)	Drain current (pulsed)	40A	
I_{DLM} (•)	Drain inductive current, clamped	40A	

		TO-220	SOT-93/TO-3	
P_{tot}	Total power dissipation T_{case} = 25°C	100W	125W	125W
	Derating factor	0.8W/°C	1W/°C	1W/°C
T_{stg}	Storage temperature	– 55 to 150° C		
T_j	Junction temperature	150°C		

(•) Pulse width limited by safe operating area

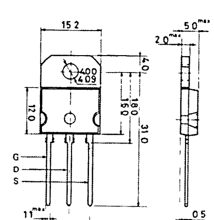
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

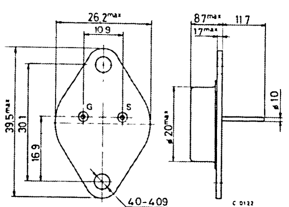
Dimensions in mm

Drain connected to tab



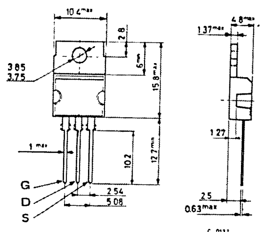
(sim. to TO-218) SOT-93

Drain connected to case



TO-3

Drain connected to tab



TO-220

THERMAL DATA

			TO-220	SOT-93	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1.25°C/W	1°C/W	1°C/W
T_L	Maximum lead temperature for soldering purpose			275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP363/463/563** for **SGSP367/467/567**	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{GS} = 0)	V_{GS} = ± 20V			100	nA
ON *						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 5A for **SGSP363/463/563** for **SGSP367/467/567** V_{GS} = 10V I_D = 10A for **SGSP363/463/563** for **SGSP367/467/567** T_{case} = 100°C I_D = 5A for **SGSP363/463/563** for **SGSP367/467/567**			 2.25 1.65 4.75 3.50 4.5 3.3	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 5A for **SGSP363/463/563** for **SGSP367/467/567**			 0.45 0.33	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 5A	3			mho

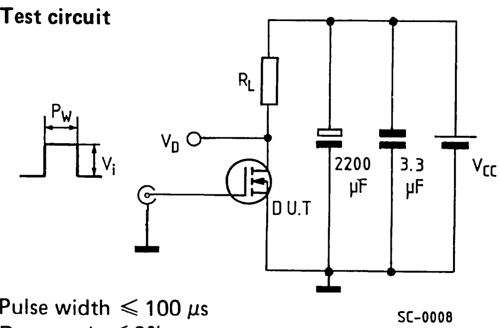
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
DYNAMIC						
C_{iss}	Input capacitance	$V_{DS} = 25V$ f = 1MHz		980	1200	pF
C_{oss}	Output capacitance	$V_{GS} = 0$		200	260	pF
C_{rss}	Reverse transfer Capacitance			80	100	pF
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	$V_{CC} = 25V$ $V_i = 10V$		10		ns
t_r	Rise time	$I_D = 5A$ $R_i = 15\,\Omega$		25		ns
$t_{d\,(off)}$	Turn-off delay time	(see test circuit)		50		ns
t_f	Fall time			32		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				10	A
I_{SDM} (·)	Source drain current (pulsed)				40	A
V_{SD}	Forward on voltage	$I_{SD} = 10A$ $V_{GS} = 0$			1.3	V
t_{on}	Turn-on time	$I_{SD} = 10A$ $V_{GS} = 0$		130		ns
t_{rr}	Reverse recovery time	$di/dt = 100A/\mu s$		250		ns

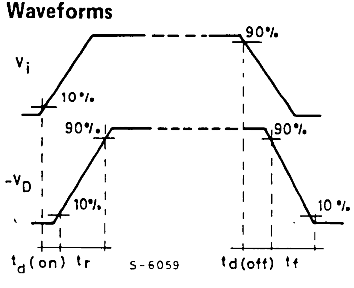
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 0.2%
(·) Pulse width limited by safe operating area

SWITCHING TIMES RESISTIVE LOAD

Test circuit



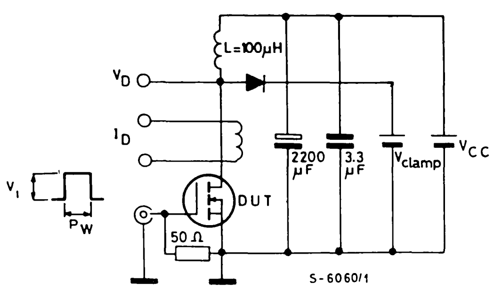
Waveforms



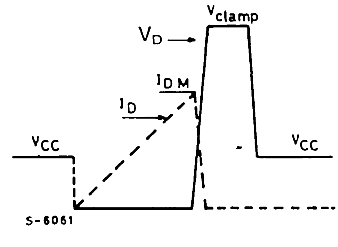
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10V$

CLAMPED INDUCTIVE LOAD

Test circuit

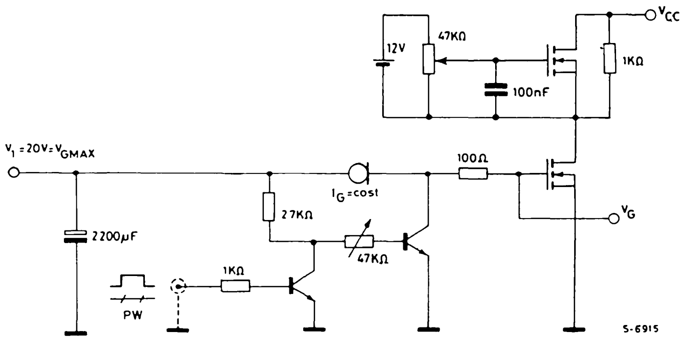


Waveforms



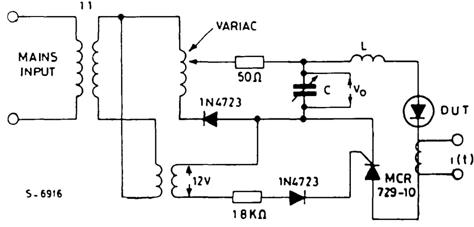
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



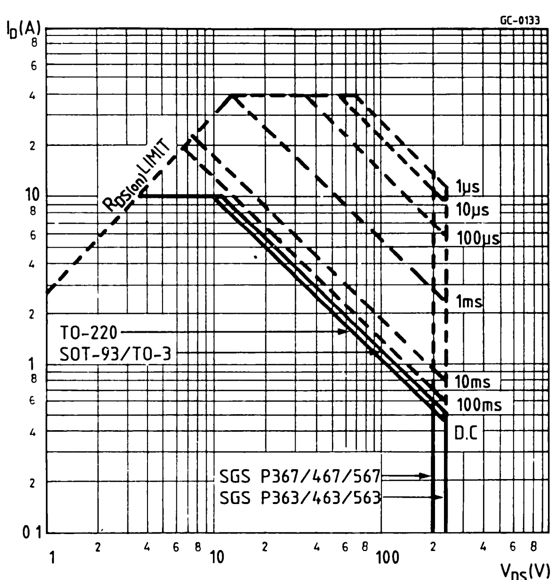
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

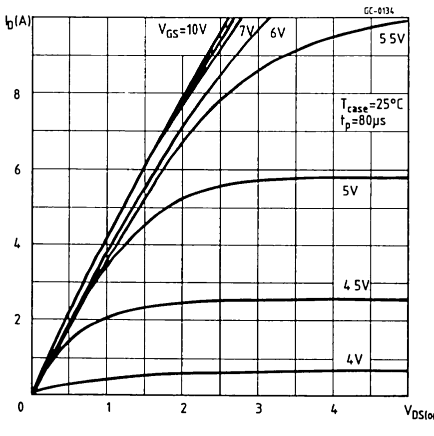


Jedec test circuit

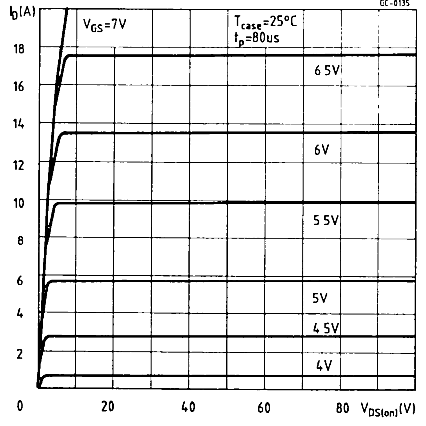
Safe operating areas



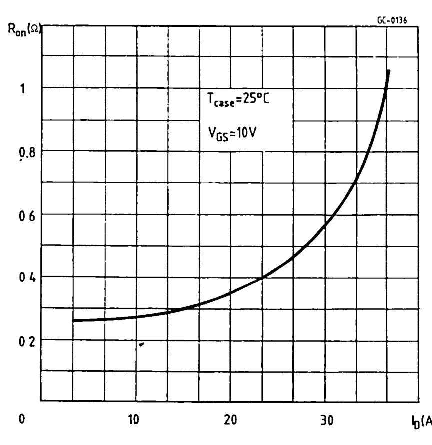
Output characteristics



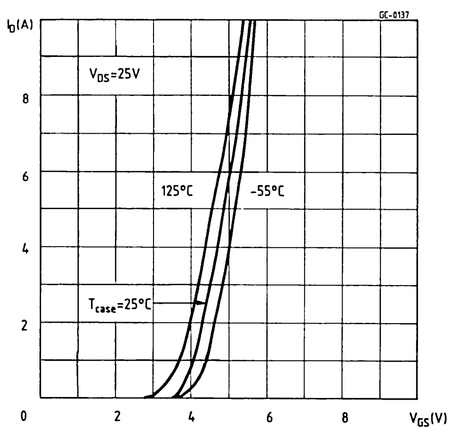
Output characteristics



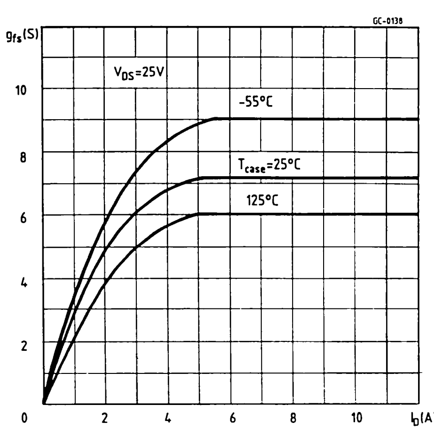
Static drain-source on resistance



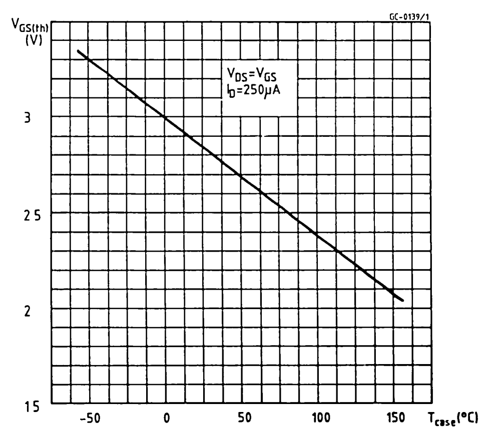
Transfer characteristics



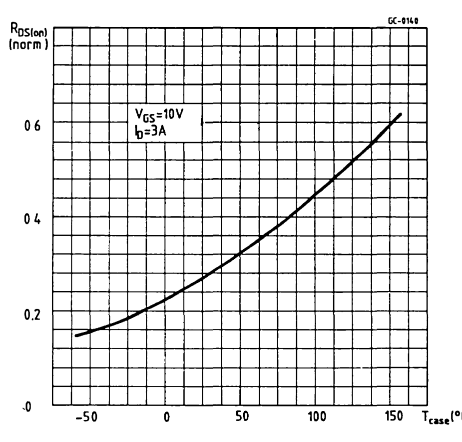
Transconductance



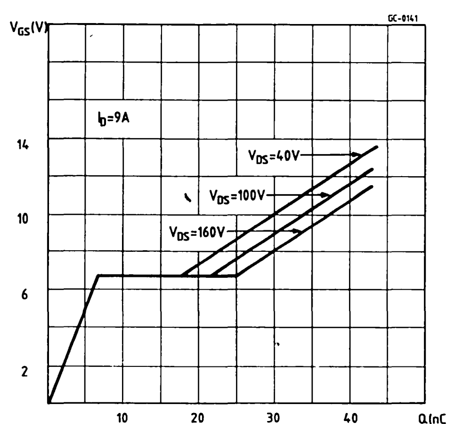
Gate thereshold voltage vs. temperature



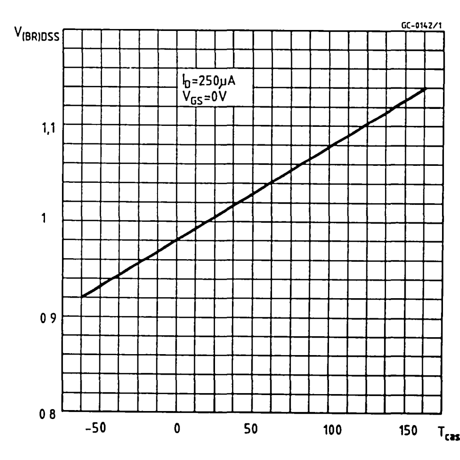
Normalized on resistance vs. temperature



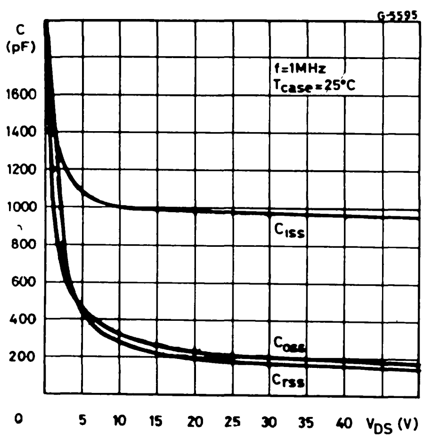
Gate charge vs gate to source voltage



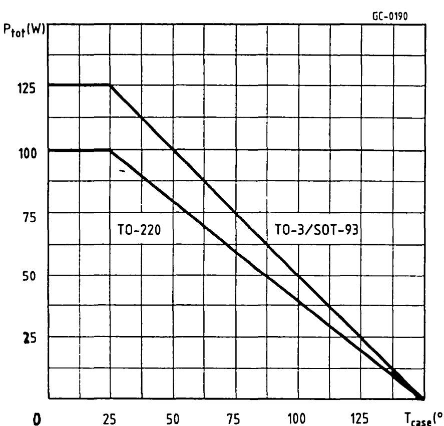
Normalized breakdown voltage vs. temperature



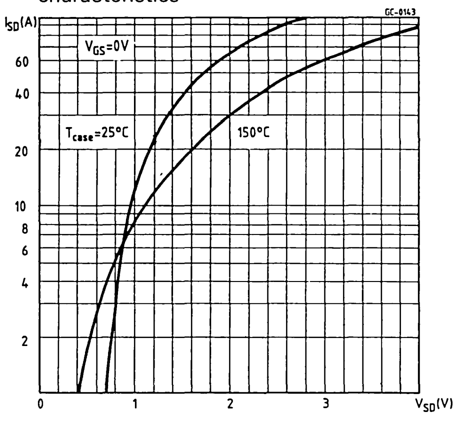
Capacitance variation



Derating curves



Source-drain diode forward characteristics



SGSP364/P365/P366
SGSP464/P465/P466
SGSP564/P565/P566

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

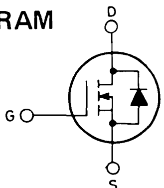
V_{DSS}	$R_{DS(ON)}$	I_D
350V/400V	1 Ω	6A
450V	1.5Ω	6A

ABSOLUTE MAXIMUM RATINGS

		TO-220 / SOT-93 / TO-3	SGSP364 / SGSP464 / SGSP564	SGSP365 / SGSP465 / SGSP565	SGSP366 / SGSP466 / SGSP566
V_{DS}	Drain-source voltage ($V_{GS} = 0$)		450V	400V	350V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)		450V	400V	350V
V_{GS}	Gate-source voltage			± 20V	
I_D	Drain current (continuous)	$T_{case} = 25°C$		6A	
		$T_{case} = 100°C$		4A	
I_{DM} (•)	Drain current (pulsed)			24A	
I_{DLM} (•)	Drain inductive current, clamped			24A	
			TO-220	SOT-93/TO-3	
P_{tot}	Total power dissipation at	$T_{case} = 25°C$	100W	125W	
	Derating factor		0.8W/°C	1W/°C	
T_{stg}	Storage temperature			-55 to 150°C	
T_j	Junction temperature			150°C	

(•) Pulse width limited by safe operating area

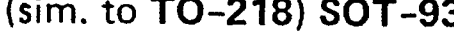
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

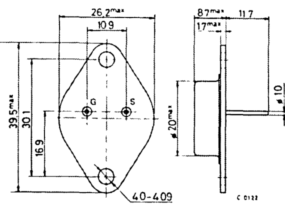
Dimensions in mm

Drain connected to tab



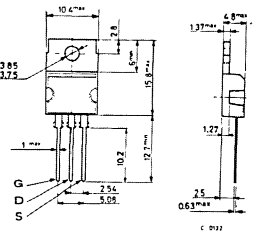
(sim. to TO-218) SOT-93

Drain connected to case



TO-3

Drain connected to tab



TO-220

THERMAL DATA

			TO-220	SOT-93	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1.25°C/W	1°C/W	
T_L	Maximum lead temperature for soldering purpose		275°C		

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdowin voltage	I_D = 250μA V_{GS} = 0				
		for **SGSP364/464/564**	450			V
		for **SGSP365/465/565**	400			V
		for **SGSP366/466/566**	350			V
I_{DSS}	Zero gate voltage drain current (V_{GS}=0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leak. (V_{DS}=0)	V_{GS} = ± 20V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μA	2		4	V
$V_{DS\ (on)}$	Drain source voltage	V_{GS} = 10V I_D = 3A				
		for **SGSP364/464/564**			4.5	V
		for **SGSP365/465/565**			3	V
		for **SGSP366/466/566**			3	V
		V_{GS} = 10V I_D = 6A				
		for **SGSP364/464/564**			10	V
		for **SGSP365/465/565**			6.7	V
		for **SGSP366/466/566**			6.7	V
		I_D = 3A T_{case} = 100°C V_{GS} = 10V				
		for **SGSP364/464/564**			9	V
		for **SGSP365/465/565**			6	V
		for **SGSP366/466/566**			6	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} 10V I_D = 3A				
		for **SGSP364/464/564**			1.5	Ω
		for **SGSP365/465/565**			1	Ω
		for **SGSP366/466/566**			1	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 3A	3			mho
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25V f = 1MHZ		780	1000	pF
C_{oss}	Output capacitance	V_{GS} = 0		150	200	pF
C_{rss}	Reverse transfer capacitance			100	130	pF

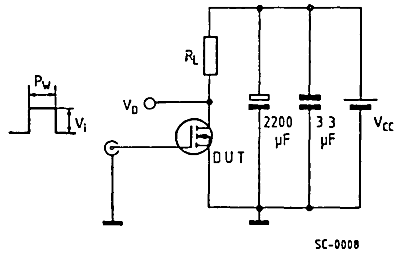
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	V_{CC} = 250V V_i = 10V		30		ns
t_r	Rise time			30		ns
$t_{d\,(off)}$	Turn-off delay time	I_D = 3A R_i = 10Ω		100		ns
t_f	Fall time	(see test circuit)		50		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				6	A
I_{SDM} (·)	Source drain current pulsed				24	A
V_{SD}	Forward on voltage	I_{SD} = 6A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 6A V_{GS} = 0		250		ns
t_{rr}	Reverse recovery time	di/dt = 25A/μs		350		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%.
(·) Pulse width limited bu safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit

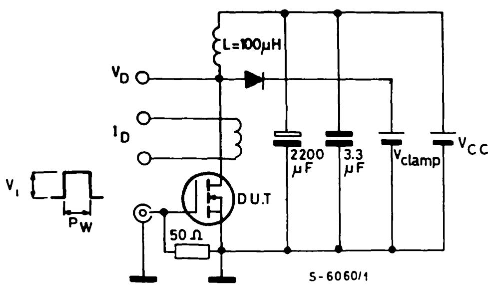


Waveforms

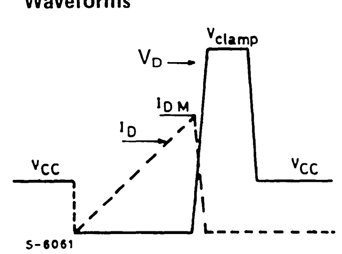
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

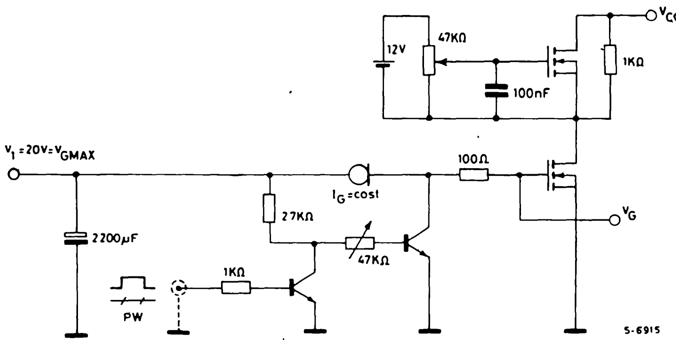


Waveforms



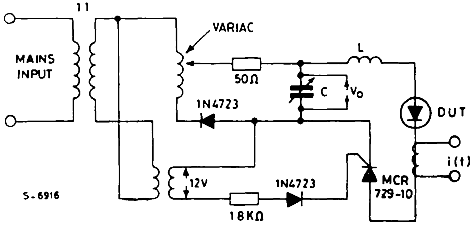
$V_i = 12V$
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



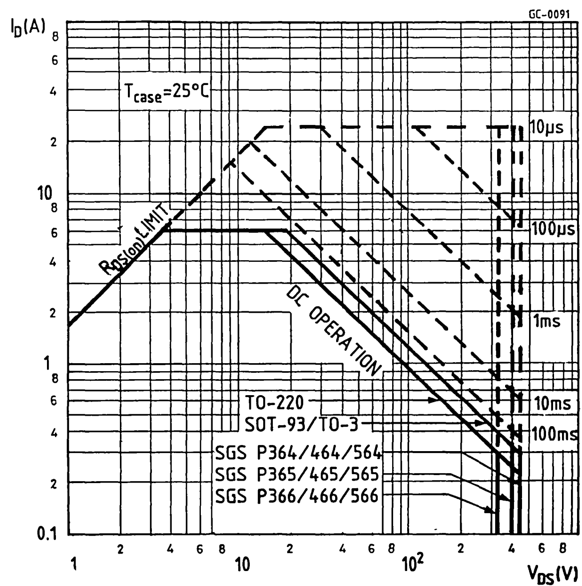
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

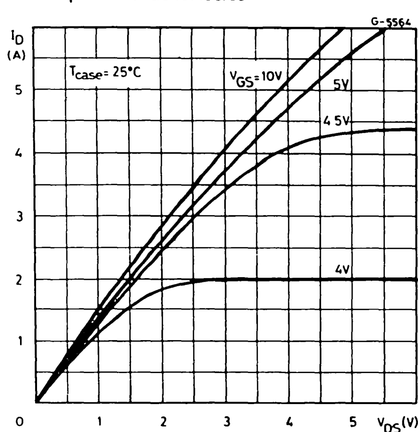


Jedec test circuit

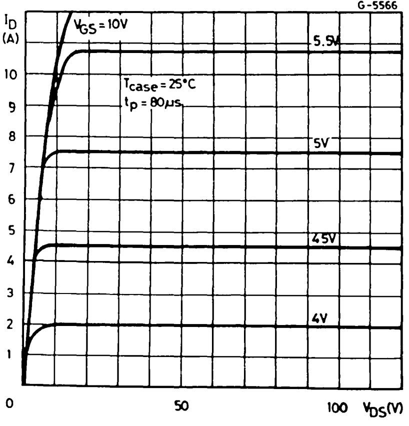
Safe operating areas



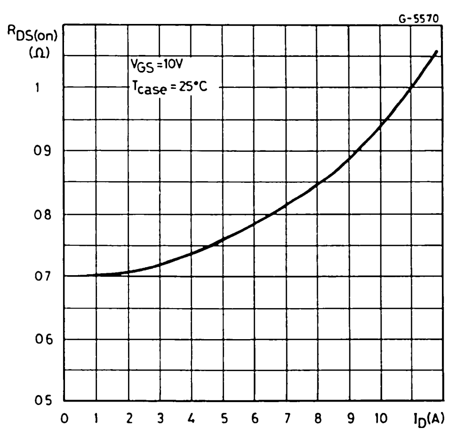
Output characteristics



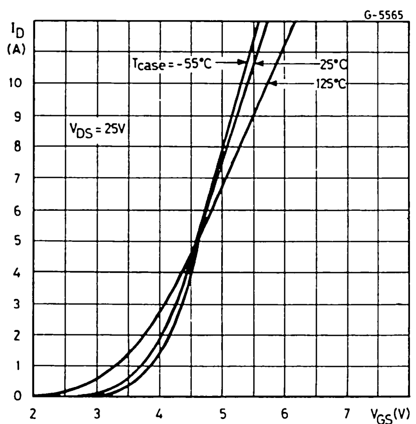
Output characteristics



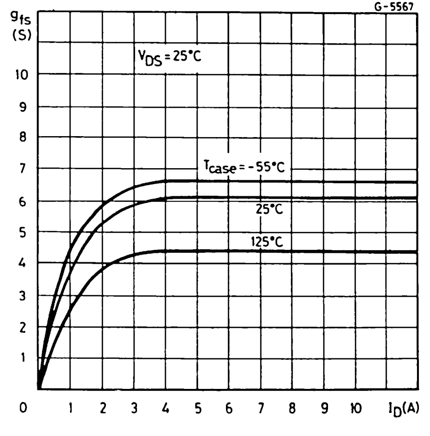
Static drain-source on resistance



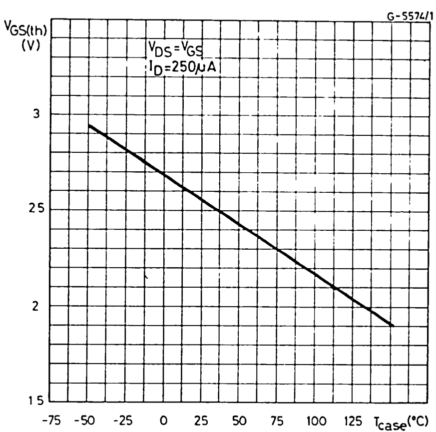
Transfer characteristics



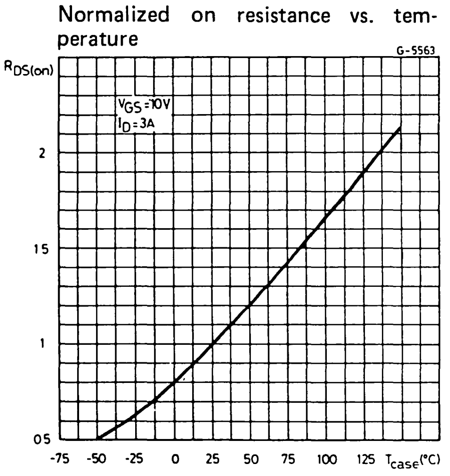
Transconductance



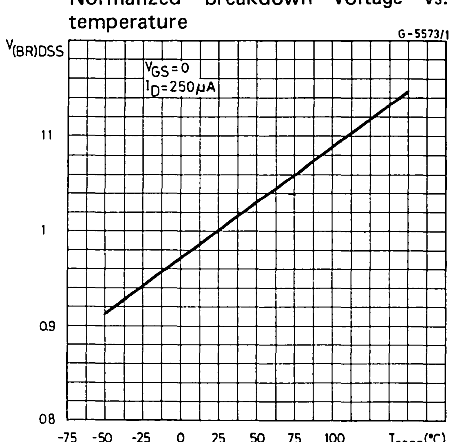
Gate threshold voltage vs. temperature



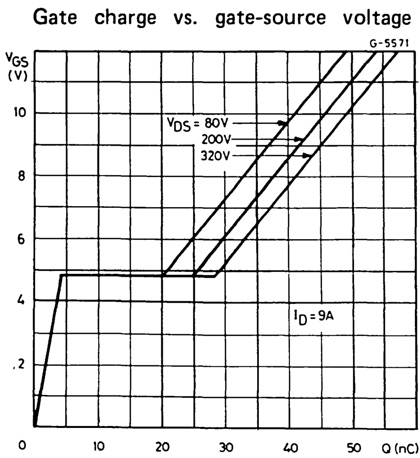
Normalized on resistance vs. temperature



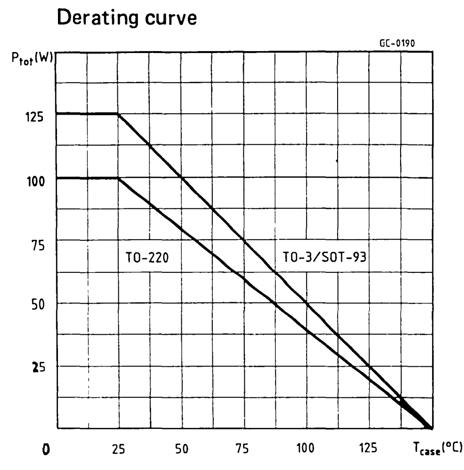
Normalized breakdown voltage vs. temperature



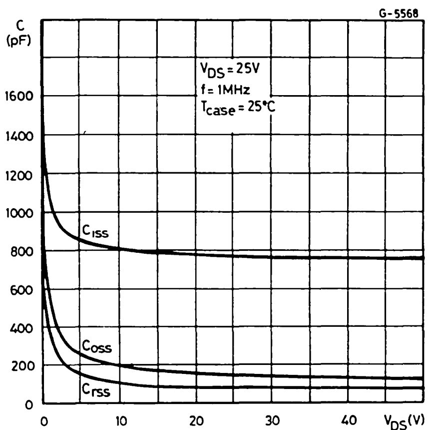
Gate charge vs. gate-source voltage



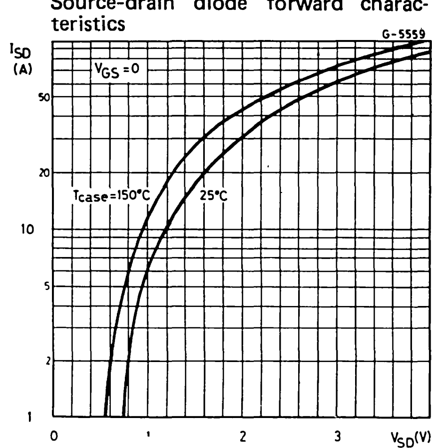
Derating curve



Capacitance variation



Source-drain diode forward characteristics



SGSP368/P369
SGSP468/P469
SGSP568/P569

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

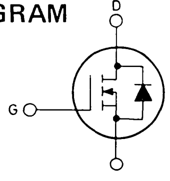
V_{DSS}	$R_{DS(ON)}$	I_D
500V	**1.5 Ω**	**5A**
550V	**2.5 Ω**	**5A**

ABSOLUTE MAXIMUM RATINGS

		TO-220 SOT-93 TO-3	SGSP368 SGSP468 SGSP568	SGSP369 SGSP469 SGSP569
V_{DS}	Drain-source voltage (V_{GS} = 0)		550V	500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		550V	500V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		5A	
	T_{case} = 100°C		3.2A	
I_{DM}(•)	Drain current (pulsed)		20A	
I_{DLM} (•)	Drain inductive current, clamped		20A	
		TO-220	**SOT-93**	**TO-3**
P_{tot}	Total power dissipation at T_{case} = 25°C	100W	125W	125W
	Derating factor	0.8W/°C	1W/°C	1W/°C
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

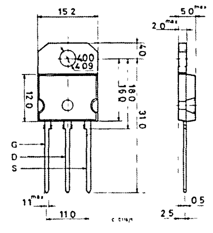
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

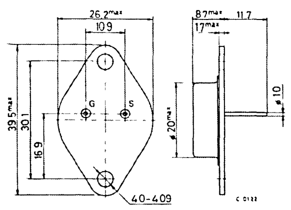
Dimensions in mm

Drain connected to tab



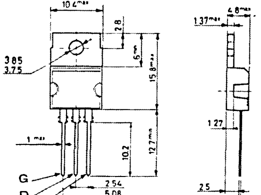
(sim. to **TO-218**) **SOT-93**

Drain connected to case



TO-3

Drain connected to tab



TO-220

THERMAL DATA

			TO-220	SOT-93	TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1.25°C/W	1°C/W	1°C/W
T_L	Maximum lead temperature for soldering purpose			275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP368/P468/P568** for **SGSP369/P469/P569**	 550 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 2.5 A for **SGSP368/P468/P568** for **SGSP369/P469/P569**			 6.25 3.75	 V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **SGSP368/P468/P568** for **SGSP369/P469/P569**			 2.5 1.5	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 2.5 A	3			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f= 1MHz V_{GS} = 0		780 150 80	1000 190 100	pF pF pF

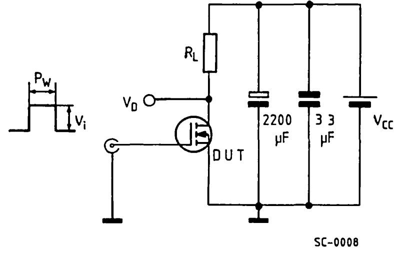
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 250 V I_D = 2.5 A		30		ns
t_r	Rise time	V_i = 10 V R_i = 10Ω		15		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				5	A
I_{SDM}(•)	Source drain current (pulsed)				20	A
V_{SD}	Forward on voltage	I_{SD} = 5 A V_{GS} = 0			1.15	V
t_{on}	Turn-on time	I_{SD} = 5 A V_{GS} = 0		85		ns
t_{rr}	Reverse recovery	di/dt = 100A/μs		320		ns

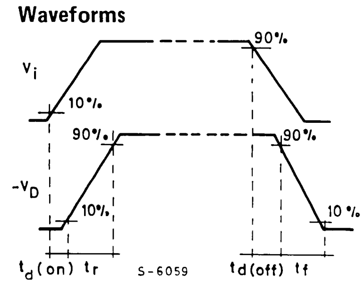
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



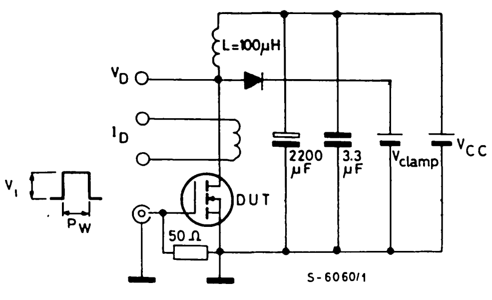
Waveforms



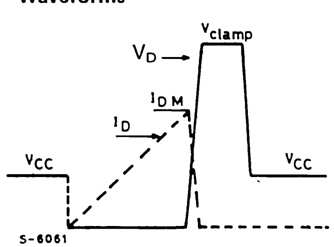
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

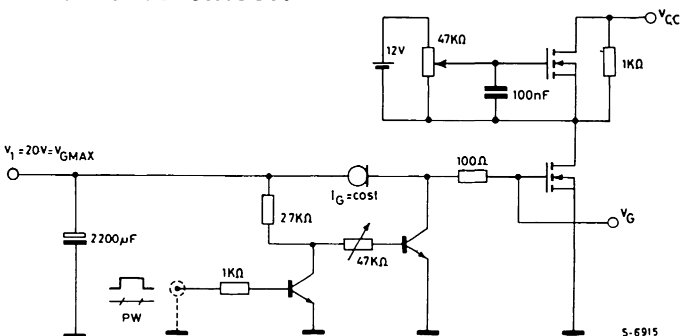


Waveforms



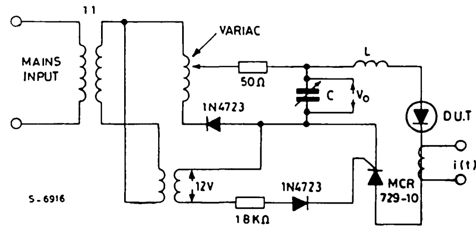
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



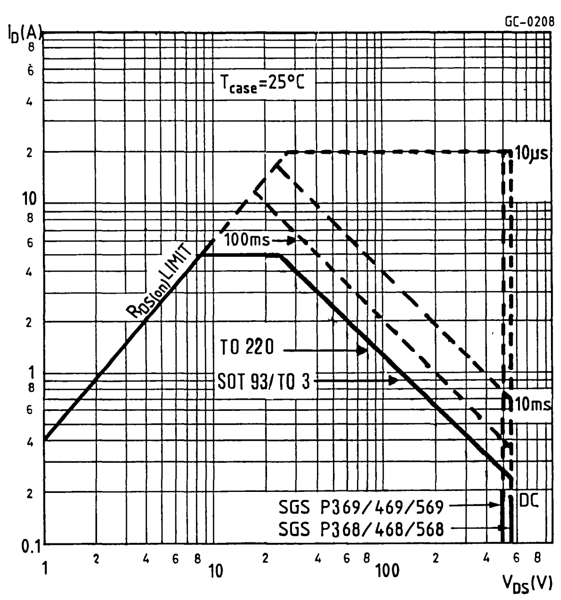
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

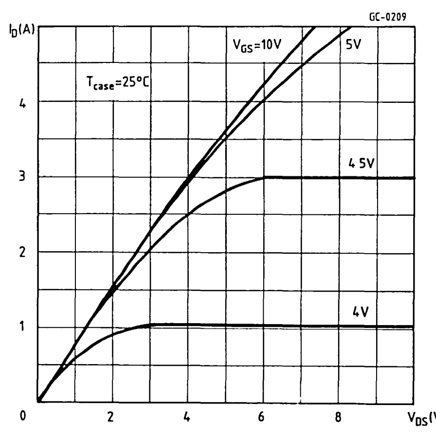


Jedec test circuit

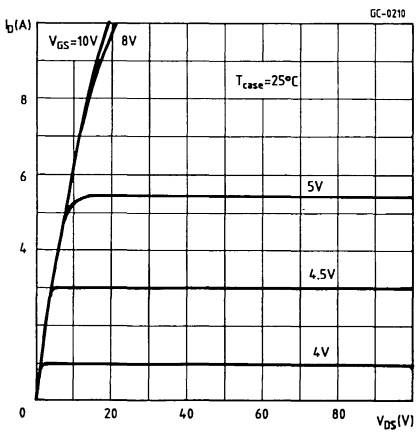
Safe operating areas



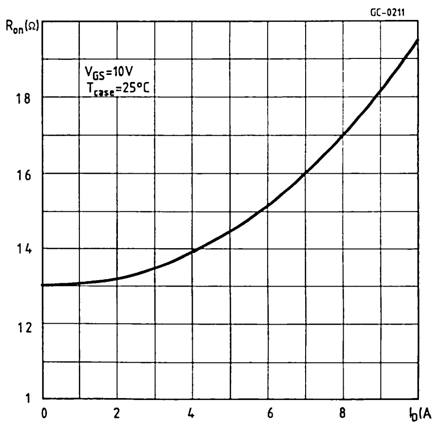
Output characteristics.



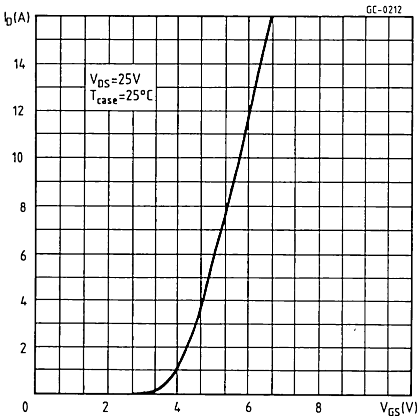
Output characteristics.



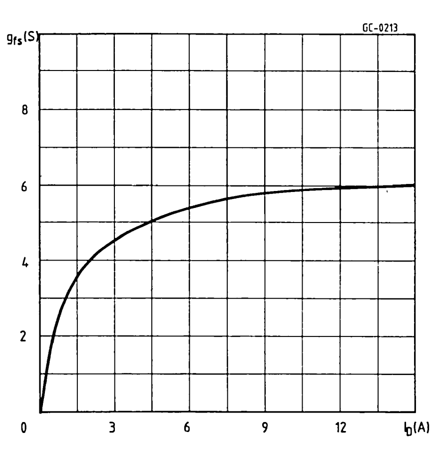
Static drain-source on resistance.



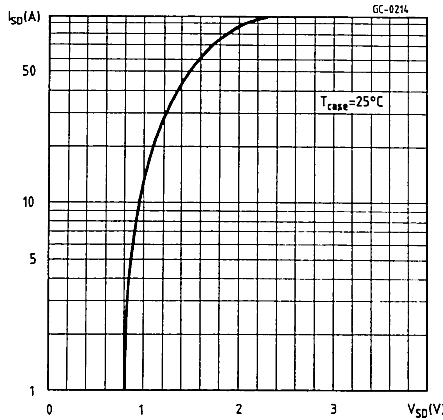
Transfer characteristics.



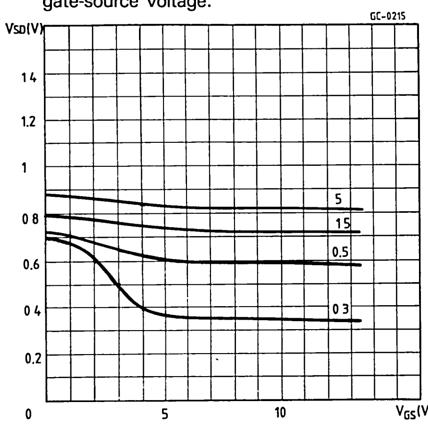
Transconductance.



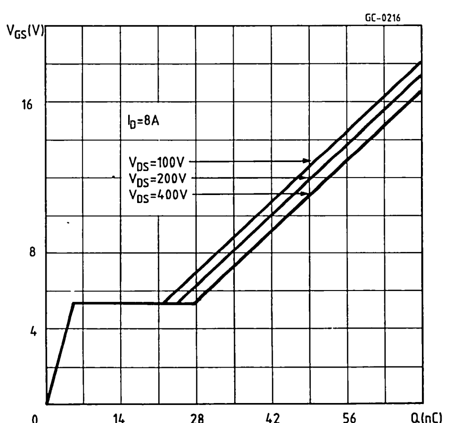
Source-drain diode forward characteristic.



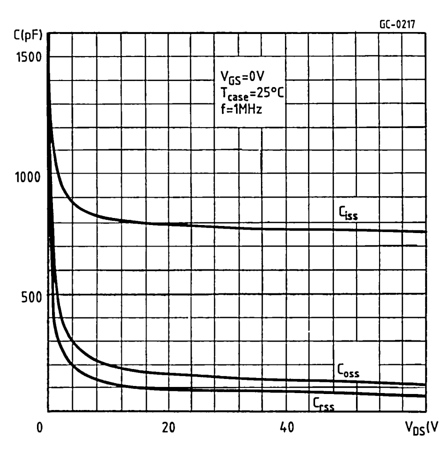
Source-drain diode forward voltage vs. gate-source voltage.



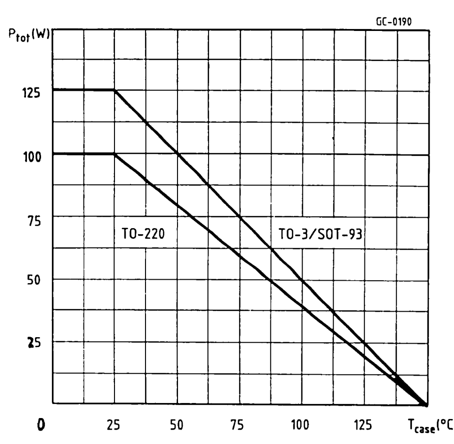
Gate charge vs. gate to source voltage.



Capacitances variation.



Derating curve.



N-CHANNEL POWER MOS TRANSISTORS

SGSP381/P382
SGSP481/P482
SGSP581/P582

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

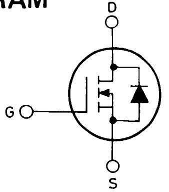
V_{DSS}	$R_{DS(ON)}$	I_D
50V/60V	0.06Ω	24A

ABSOLUTE MAXIMUM RATINGS

		TO-220 / SOT-93 / TO-3	SGSP381 / SGSP481 / SGSP581	SGSP382 / SGSP482 / SGSP582	
V_{DS}	Drain-source voltage (V_{GS} = 0)		60V	50V	
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		60V	50V	
V_{GS}	Gate-source voltage		±20V		
I_D	Drain current (continuous) T_{case} = 25°C		24A		
	at T_{case} = 100°C		15A		
I_{DM}(•)	Drain current (pulsed)		96A		
I_{DLM} (•)	Drain inductive current, clamped		96A		
			TO-220	**SOT-93**	**TO-3**
P_{tot}	Total power dissipation at T_{case} = 25°C		100W	125W	125W
	Derating factor		0.8W/°C	1W/°C	1W/°C
T_{stg}	Storage temperature		-55 to 150°C		
T_j	Max. operating junction temperature		150°C		

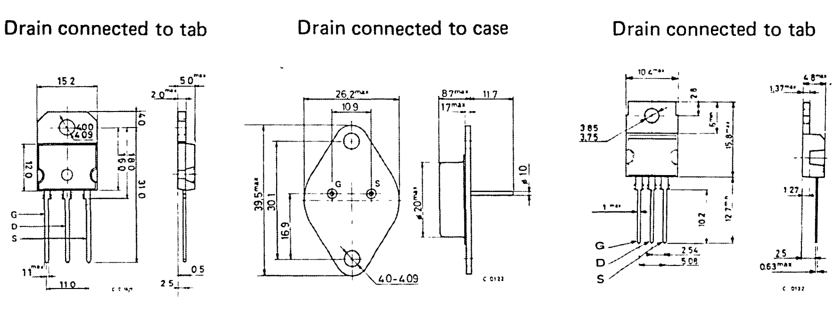
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



(sim. to TO-218) SOT-93

TO-3

TO-220

THERMAL DATA

			TO-220	SOT-93/TO-3
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	1.25°C/W	1°C/W
T_L	Maximum lead temperature for soldering purpose		275°C	

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SGSP381/P481/P581** for **SGSP382/P482/P582**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = 20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 12 A I_D = 24 A T_{case} = 100°C I_D = 12 A			0.8 1.72 1.60	V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 12 A			0.06	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 12 A	5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1100 600 300	1400 800 400	pF pF pF

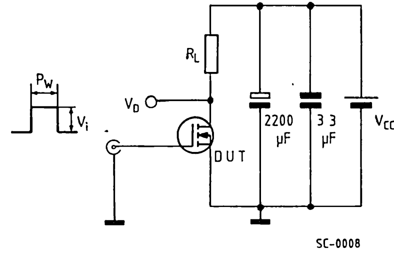
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 25 V I_D = 12 A		20		ns
t_r	Rise time	V_i = 10 V R_i = 4.7Ω		30		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		30		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				24	A
I_{SDM}(•)	Source drain current (pulsed)				96	A
V_{SD}	Forward on voltage	I_{SD} = 24 A V_{GS} = 0			1.4	V
t_{on}	Turn-on time	I_{SD} = 24 A V_{GS} = 0		300		ns
t_{rr}	Reverse recovery time	di/dt = 100 A/μs		130		ns

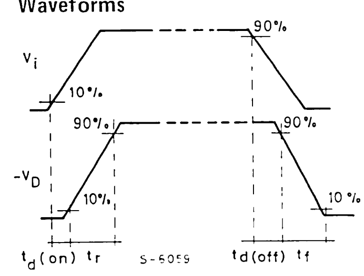
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



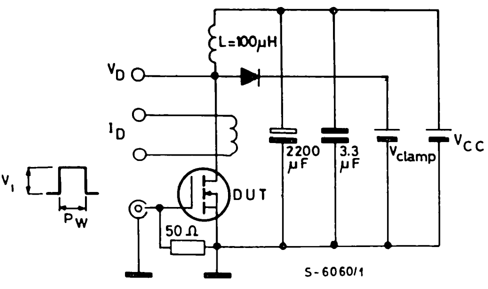
Waveforms



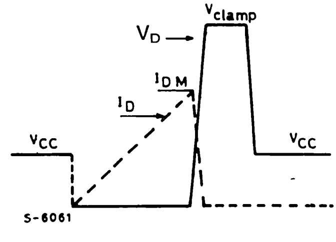
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

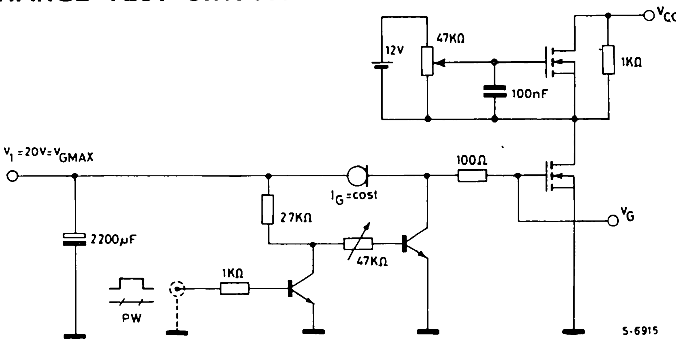


Waveforms



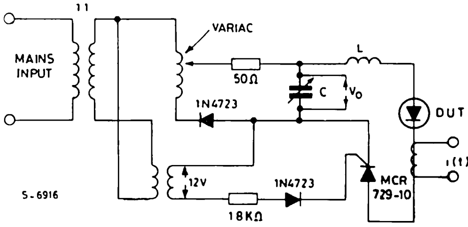
V_i = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



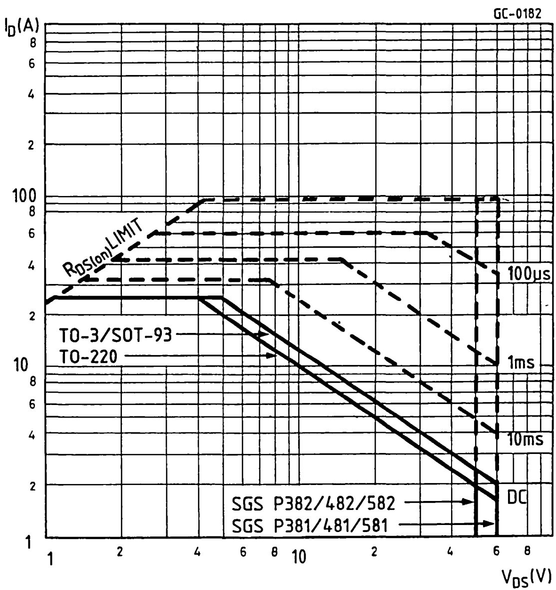
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

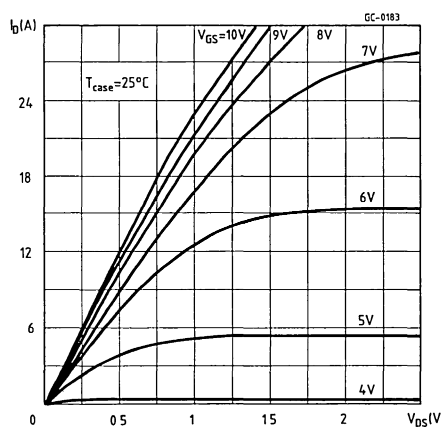


Jedec test circuit

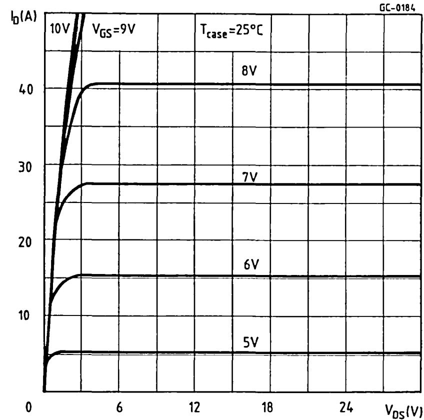
Safe operating areas



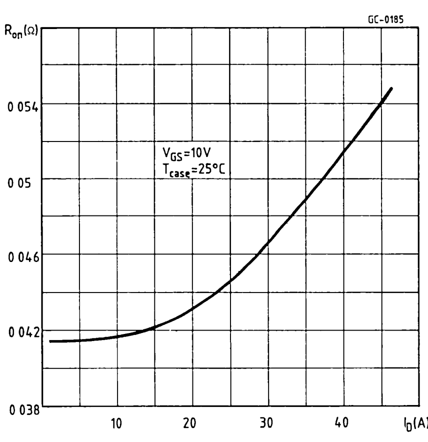
Output characteristics



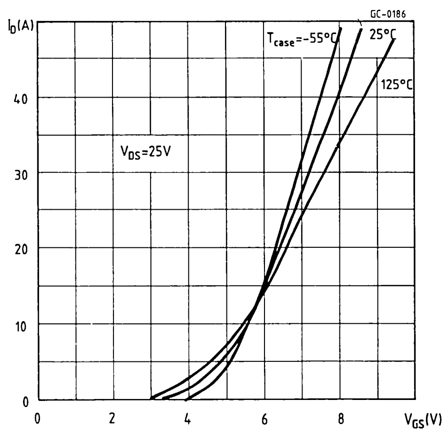
Output characteristics



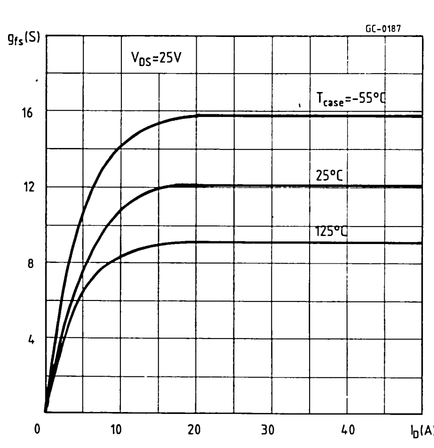
Static drain-source on resistance.



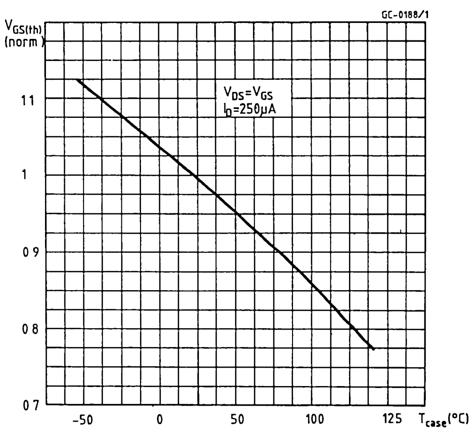
Transfer characteristics.



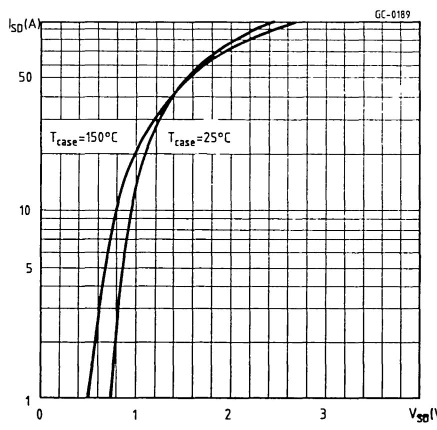
Transconductance.



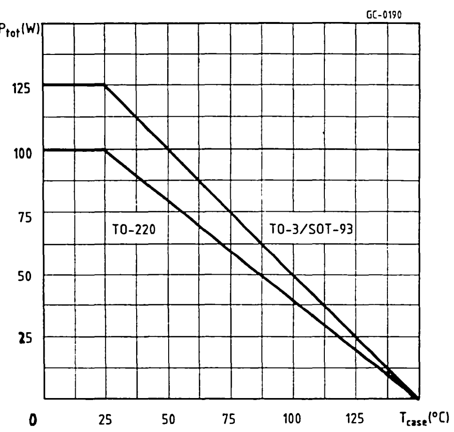
Normalized gate threshold voltage vs. temp.



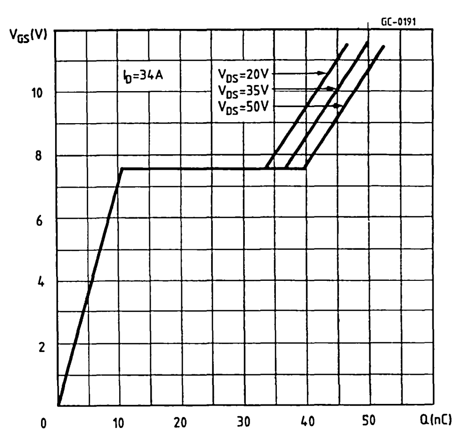
Source-drain diode forward characteristics.



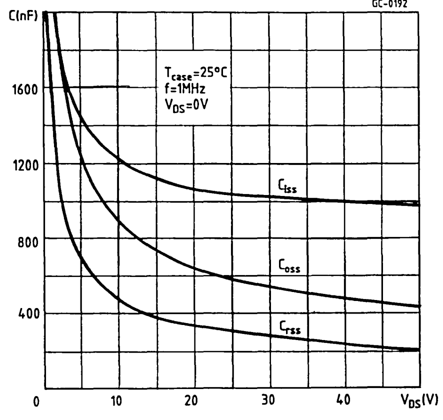
Derating curves.



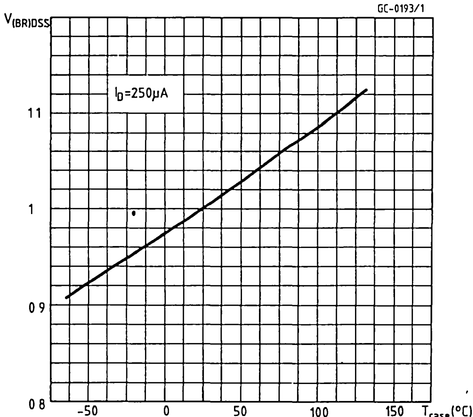
Gate charge vs. gate to source voltage.



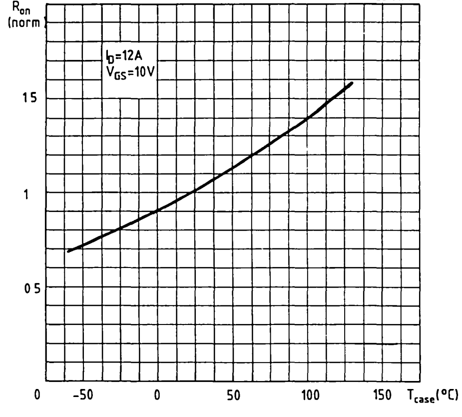
Capacitances variation.



Normalized breakdown voltage vs. temp.



Normalized on resistance vs. temperature.



SGSP471/P472
SGSP571/P572

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

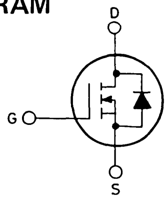
V_{DSS}	$R_{DS(ON)}$	I_D
80V	0.05 Ω	30A
100V	0.075Ω	30A

ABSOLUTE MAXIMUM RATINGS

		SOT-93 TO-3	SGSP471 SGSP571	SGSP472 SGSP572
V_{DS}	Drain-source voltage (V_{GS} = 0)		100V	80V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)		100V	80V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		30A	
	T_{case} = 100°C		19A	
I_{DM} (•)	Drain current (pulsed)		120A	
I_{DLM} (•)	Drain inductive current, clamped		120A	
P_{tot}	Total power dissipation at T_{case} = 25°C		150W	
	Derating factor		1.2W/°C	
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Junction temperature		150°C	

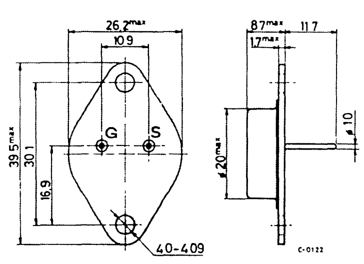
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM

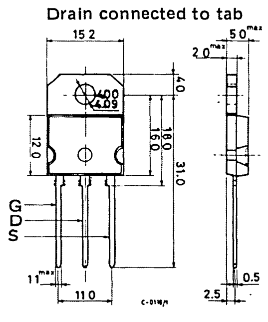


MECHANICAL DATA

Dimension in mm



TO-3



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA V_{GS} = 0 for **SGSP471/571** for **SGSP472/572**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS}=0)	V_{DS} = Max. Rating			250	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
ON *						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 µA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 15A for **SGSP472/572** for **SGSP471/571** V_{GS} = 10V I_D = 30A for **SGSP472/572** for **SGSP471/571** T_{case} = 100°C I_D = 15A for **SGSP472/572** for **SGSP471/571**			 0.75 1.12 1.60 2.40 1.50 2.25	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 15A for **SGSP472/572** for **SGSP471/571**			 0.05 0.075	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 15A	9			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V f = 1MHz V_{GS} = 0		1800 650 300	2200 810 375	pF pF pF

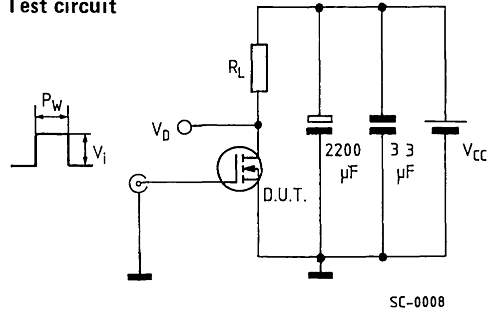
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	V_{DS} = 50V V_i = 10V		30		ns
t_r	Rise time	I_D = 15A R_i = 4.7Ω		60		ns
$t_{d\,(off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				30	A
I_{SDM} (·)	Source drain current (pulsed)				120	A
V_{SD}	Forward on voltage	I_{SD} = 30A V_{GS} = 0			1.35	V
t_{on}	Turn-on time	I_{SD} = 30A V_{GS} = 0		500		ns
t_{rr}	Reverse recovery time	di/dt = 100A/μs		1000		ns

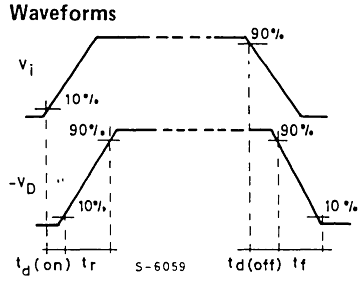
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(·) Pulse width limited by safe operating area

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms

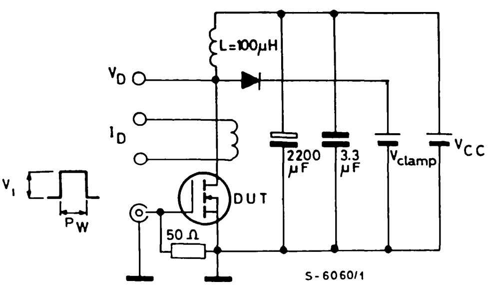


Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

SGSP471/P472
SGSP571/P572

CLAMPED INDUCTIVE LOAD

Test circuit



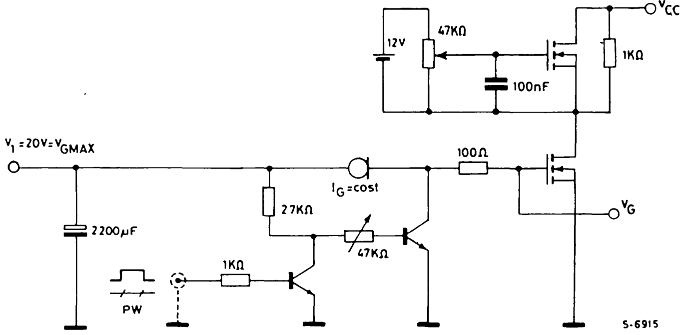
Waveforms

V_{clamp}
V_D
I_{DM}
I_D
V_{CC}
V_{CC}
S-6061

V_I = 12V

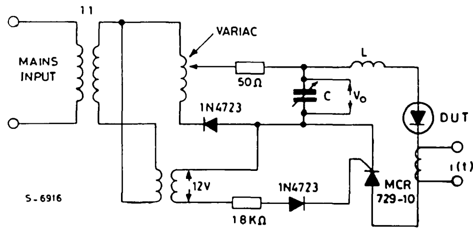
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



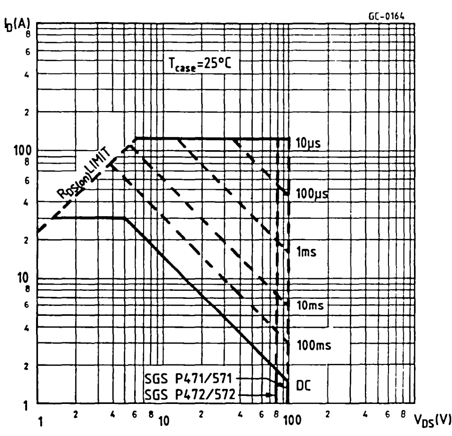
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

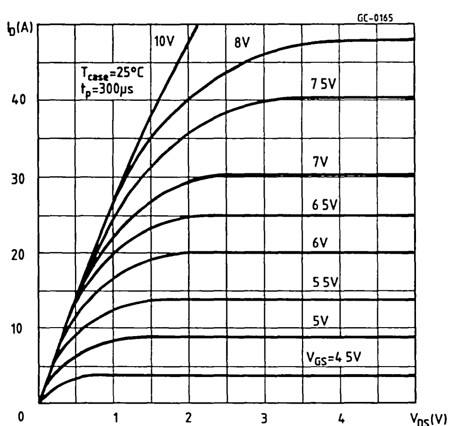


Jedec test circuit

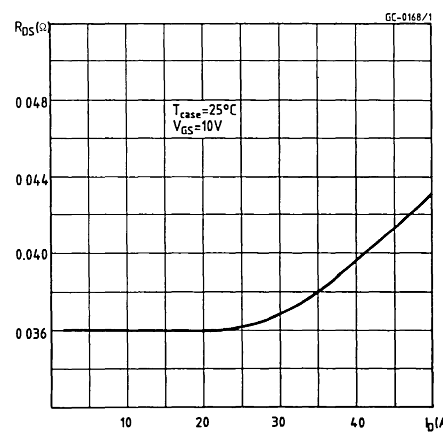
Safe operating areas



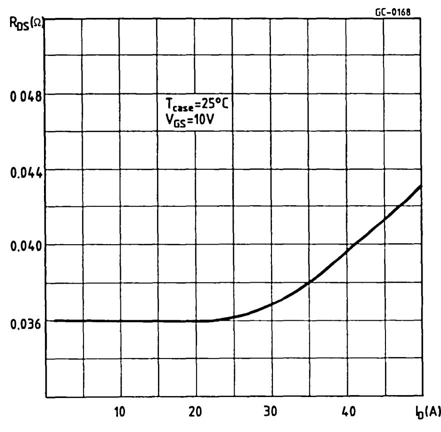
Output characteristics



Output characteristics

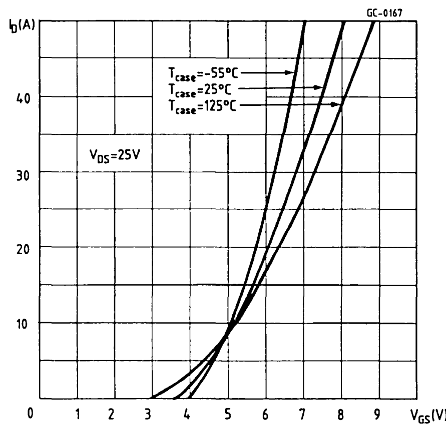


Static drain-source on resistance

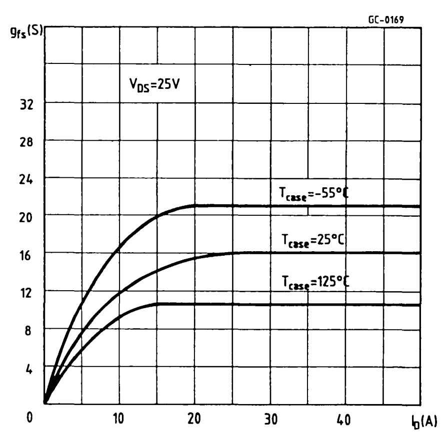


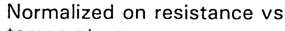
SGSP471/P472
SGSP571/P572

Transfer characteristics

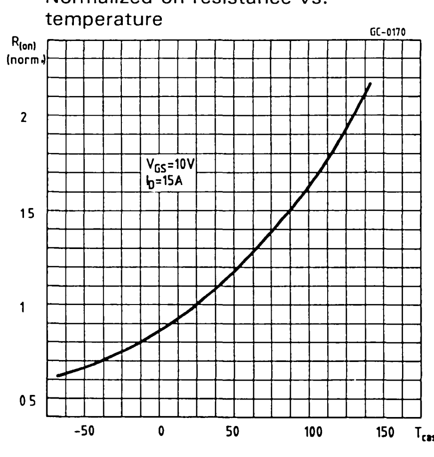


Transconductance

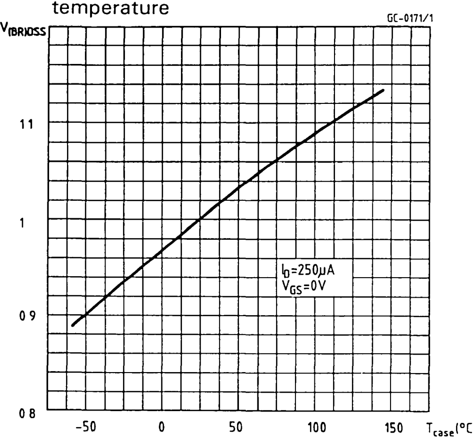




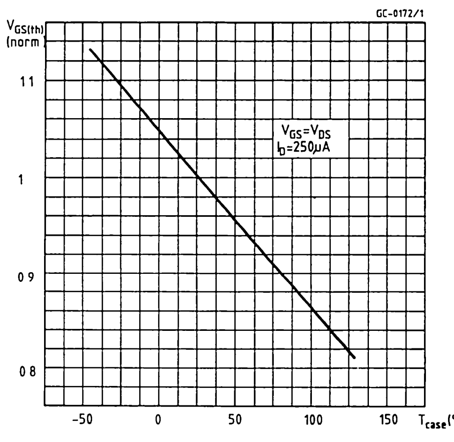
Normalized on resistance vs. temperature



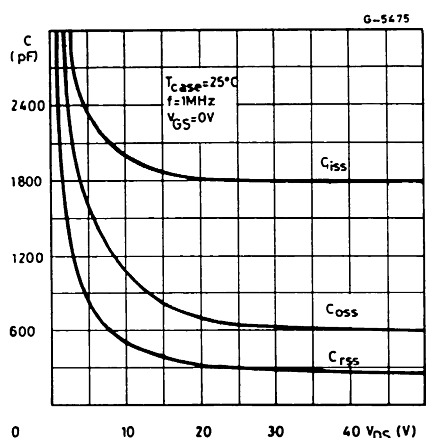
Normalized breakdown voltage vs. temperature



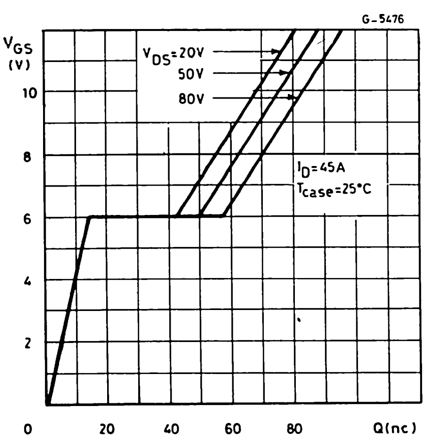
Normalized thereshold voltage vs. temp



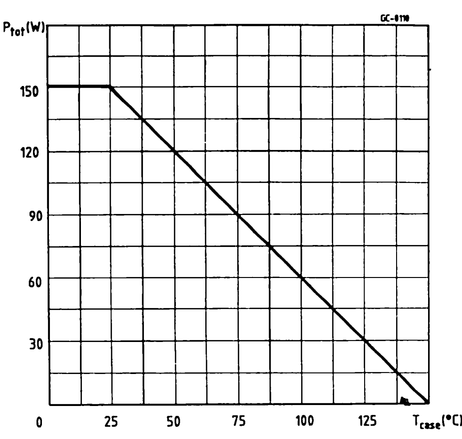
Capacitance variation

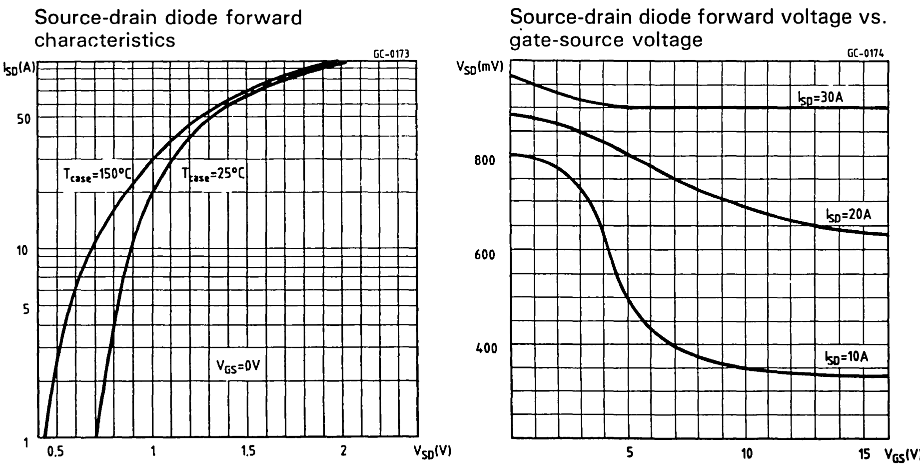


Gate charge vs. gate-source voltage



Derating curve




Source-drain diode forward characteristics
GC-0173
I_{SD}(A)
50
10
5
1
0.5
1
1.5
2
V_{SD}(V)
T_{case}=150°C
T_{case}=25°C
V_{GS}=0V
Source-drain diode forward voltage vs. gate-source voltage
GC-0174
V_{SD}(mV)
800
600
400
5
10
15
V_{GS}(V)
I_{SD}=30A
I_{SD}=20A
I_{SD}=10A

SGSP473/P573
SGSP477/P577

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

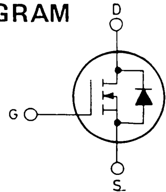
V_{DSS}	$R_{DS(ON)}$	I_D
200V	0.17Ω	20A
250V	0.22Ω	20A

ABSOLUTE MAXIMUM RATINGS

		SOT-93 TO-3	SGSP473 SGSP573	SGSP477 SGSP577
V_{DS}	Drain-source voltage (V_{GS} = 0)		250V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		250V	200V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		20A	
	at T_{case} = 100°C		13A	
I_{DM}(•)	Drain current (pulsed)		80A	
I_{DLM} (•)	Drain inductive current, clamped		80A	
P_{tot}	Total power dissipation at T_{case} = 25°C		150W	
	Derating factor		1.2W/°C	
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

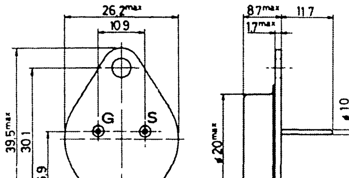
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

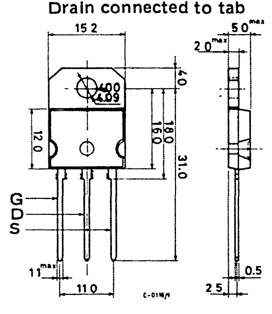
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.84	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit

OFF

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP473/P573** for **SGSP477/P577**	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA

ON*

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 10A for **SGSP473/P573** for **SGSP477/P577** V_{GS} = 10V I_D =20A for **SGSP473/P573** for **SGSP477/P577** V_{GS} =10V I_D = 10A T_c = 100°C for **SGSP473/P573** for **SGSP477/P577**			 2.2 1.7 4.7 3.6 4.4 3.4	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D =10A for **SGSP473/P573** for **SGSP477/P577**			 0.22 0.17	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 10A	8			mho

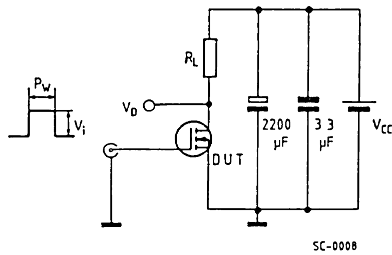
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		1900	2200	pF
C_{oss}	Output capacitance			450	550	pF
C_{rss}	Reverse transfer capacitance			220	260	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 75V I_D = 10A V_i = 10V R_i = 4.7Ω (see test circuit)		30		ns
t_r	Rise time			25		ns
$t_{d\ (off)}$	Turn-off delay time			90		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				20	A
I_{SDM}(•)	Source drain current (pulsed)				80	A
V_{SD}	Forward on voltage	I_{SD} = 20A V_{GS} = 0			1.3	V
t_{on}	Turn-on time	I_{SD} = 18A V_{GS} = 0 di/dt = 100A/μS		300		ns
t_{rr}	Reverse recovery time			300		ns

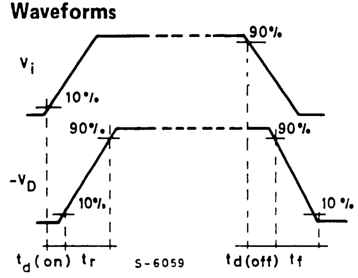
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



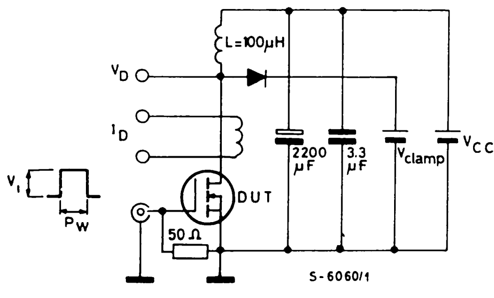
Waveforms



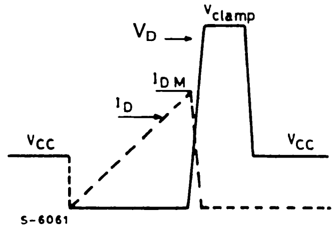
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit

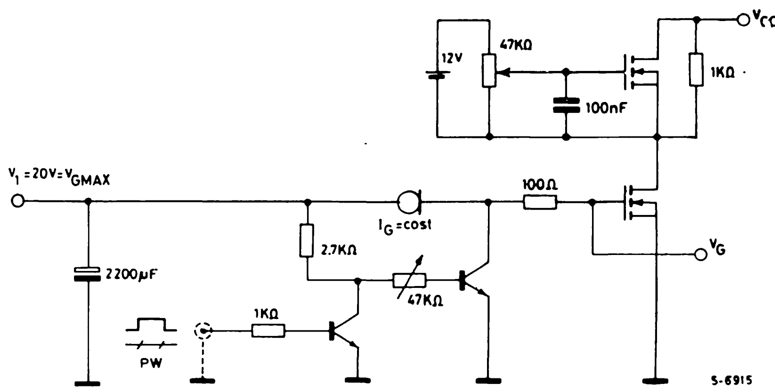


Waveforms



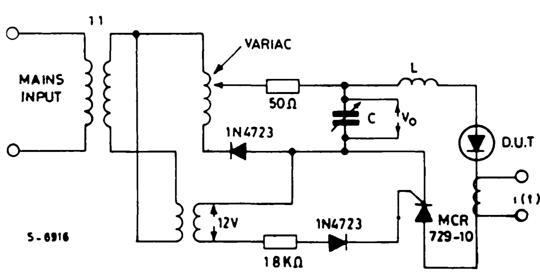
V_i = 12V
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



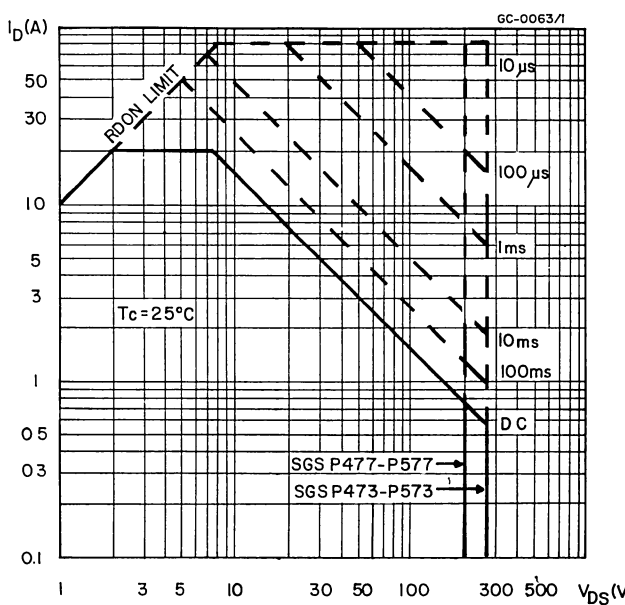
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

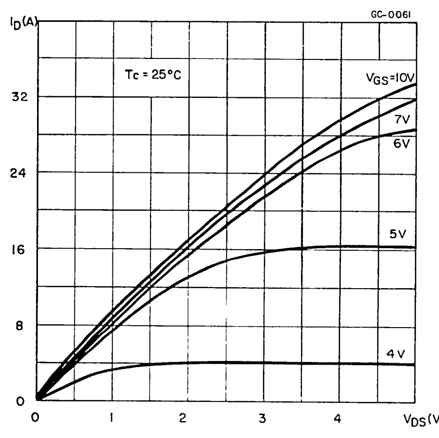


Jedec test circuit

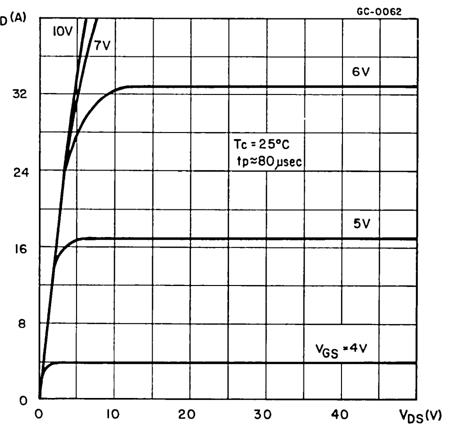
Safe operating areas



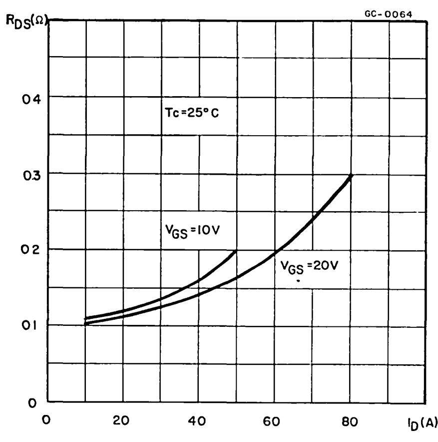
Output characteristics



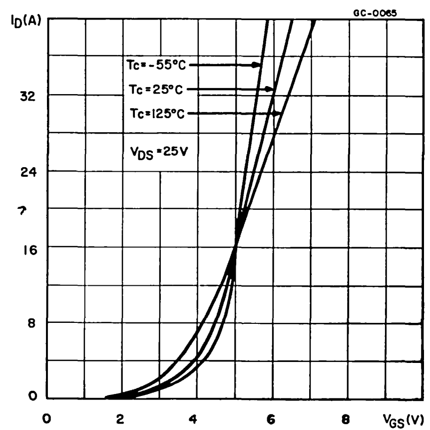
Output characteristics



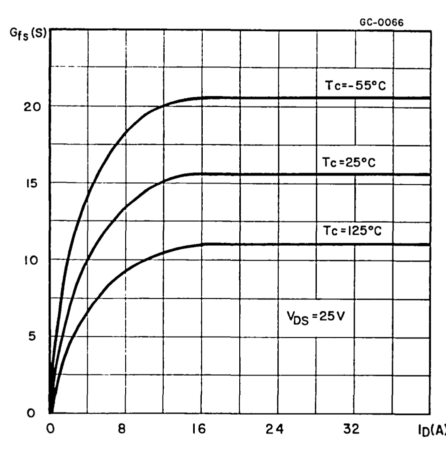
Static drain-source on resistance



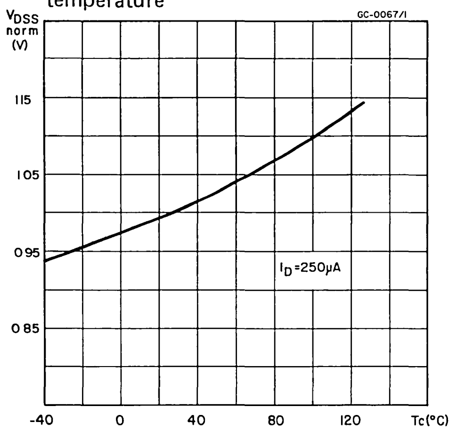
Transfer characteristics



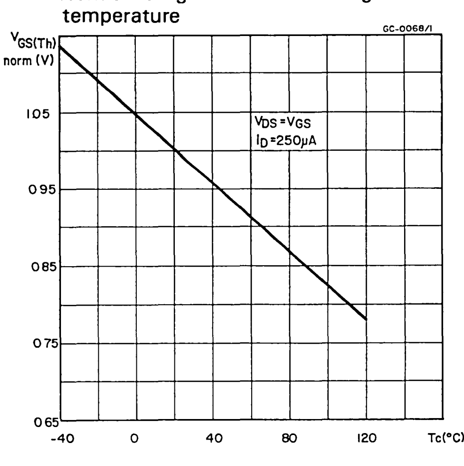
Transconductance



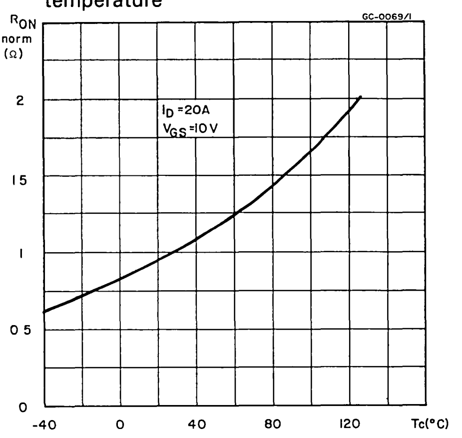
Normalized breakdown voltage vs. temperature



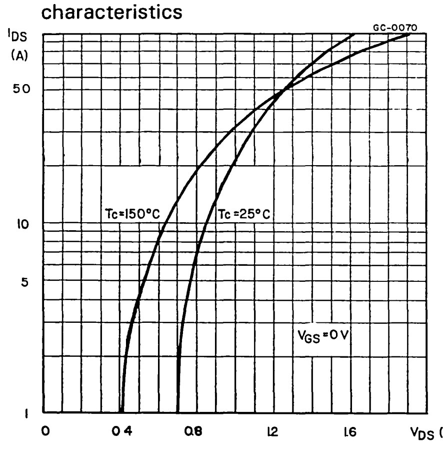
Normalized gate treshold voltage vs. temperature



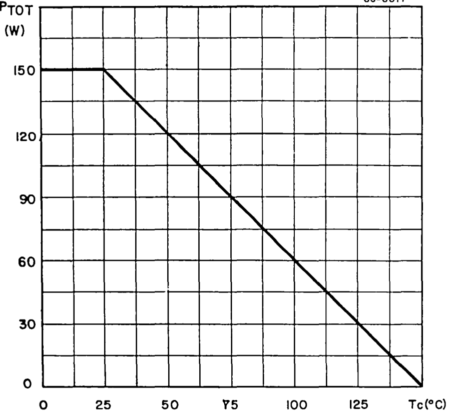
Normalized on resistance vs. temperature



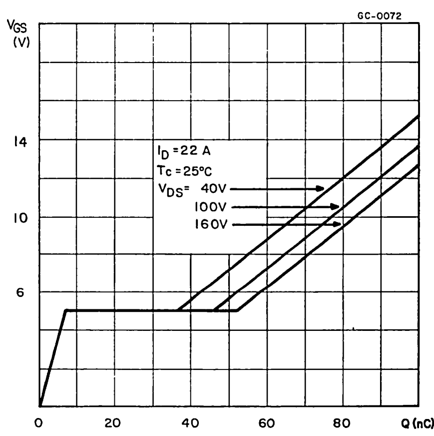
Source-drain diode forward characteristics



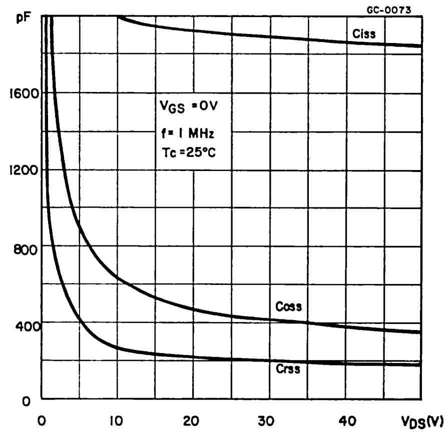
Derating curve



Gate charge vs gate to source voltage



Capacitance variation



SGSP474/P475/P476
SGSP574/P575/P576

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

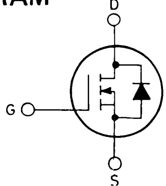
V_{DSS}	$R_{DS(ON)}$	I_D
350V/400V	0.55Ω	12A
450V	0.7 Ω	12A

ABSOLUTE MAXIMUM RATINGS

	SOT-93 TO-3	SGSP474 SGSP574	SGSP475 SGSP575	SGSP476 SGSP576
V_{DS}	Drain-source voltage (V_{GS} = 0)	450V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	450V	400V	350V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C		12A	
	T_{case} = 100°C		7.6A	
I_{DM}(•)	Drain current (pulsed)		48A	
I_{DLM} (•)	Drain inductive current, clamped		48A	
P_{tot}	Total power dissipation at T_{case} = 25°C		150W	
	Derating factor		1.2W/°C	
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Junction temperature		150°C	

(•) Pulse width limited by safe operating area

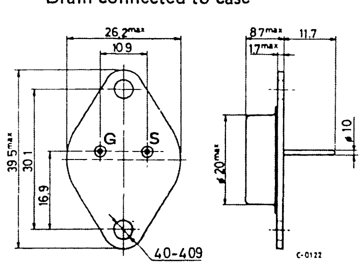
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

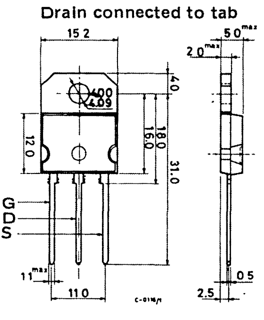
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0				
		for **SGSP474/574**	450			V
		for **SGSP475/575**	400			V
		for **SGSP476/576**	350			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold volt	V_{DS} = V_{GS} I_D = 250μ A	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 6A				
		for **SGSP474/574**			4.2	V
		for **SGSP475/575/476/576**			3.3	V
		I_D = 12A				
		for **SGSP474/574**			9.3	V
		for **SGSP475/575/476/576**			7.1	V
		T_{case} = 100°C I_D = 6A				
		for **SGSP474/574**			8.4	V
		for **SGSP475/575/476/576**			6.6	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D =6A				
		for **SGSP474/574**			0.70	Ω
		for **SGSP475/575/476/576**			0.55	Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D =6A	6			mho
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} =25V f=1MHz		1600	2100	pF
C_{oss}	Output capacitance	V_{GS} =0		300	390	pF
C_{rss}	Reverse transfer capacitance			200	260	pF

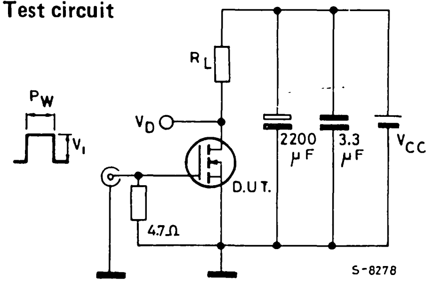
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 100V V_i = 10V		20		ns
t_r	Rise time	I_D = 6A R_i = 4.7Ω		25		ns
$t_{d\ (off)}$	Turn-off delay time			70		ns
t_f	Fall time	(see test circuit)		20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				12	A
I_{SDM}(•)	Source drain current (pulsed)				48	A
V_{SD}	Forward on voltage	I_{SD} = 12A V_{GS} = 0			1.2	V
t_{on}	Turn-on time	I_{SD} = 12A V_{GS} = 0		700		ns
t_{rr}	Reverse recovery	di/dt = 25A/μs		800		ns

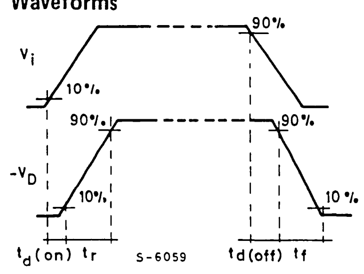
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width inited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



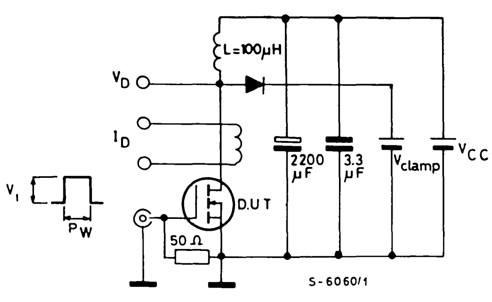
Waveforms



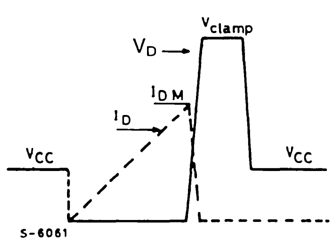
Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

CLAMPED INDUCTIVE LOAD

Test circuit



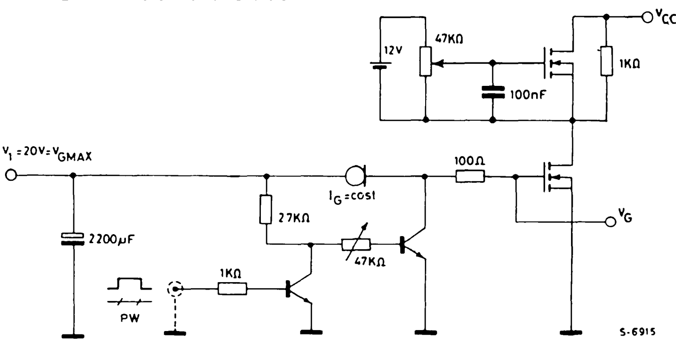
Waveforms



$V_I = 12V$

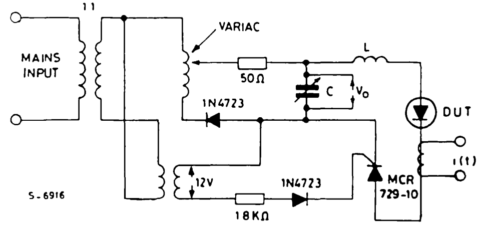
Pulse width: adjusted to obtain specified I_{DM}, $V_{clamp} = 0.75\ V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



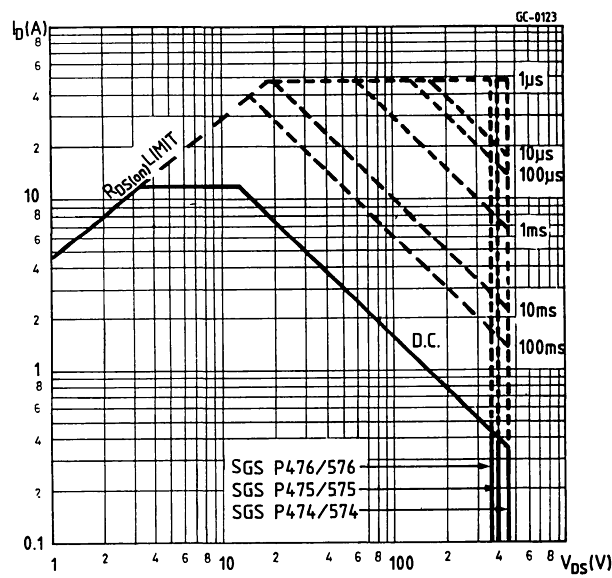
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

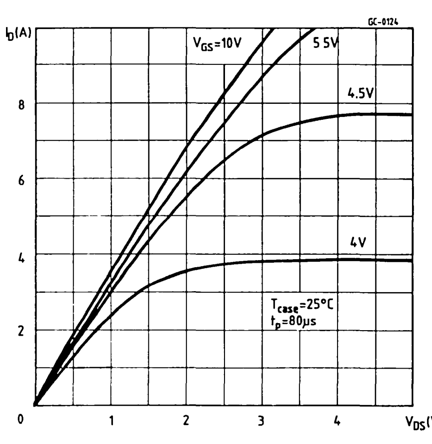


Jedec test circuit

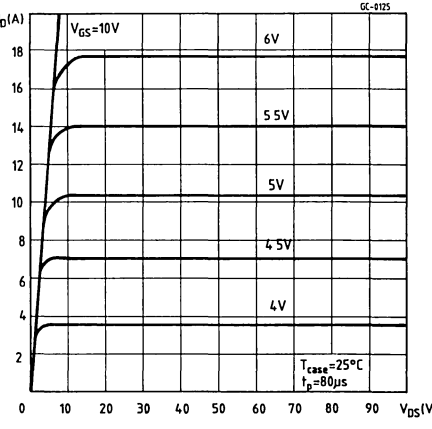
Safe operating areas



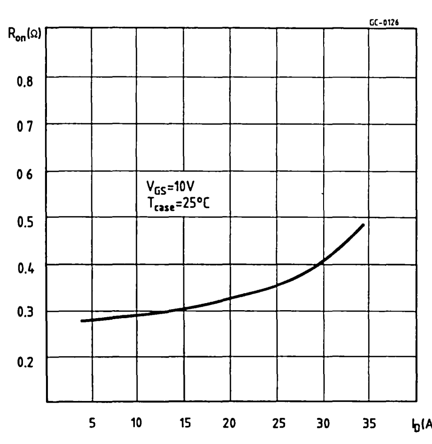
Output characteristics



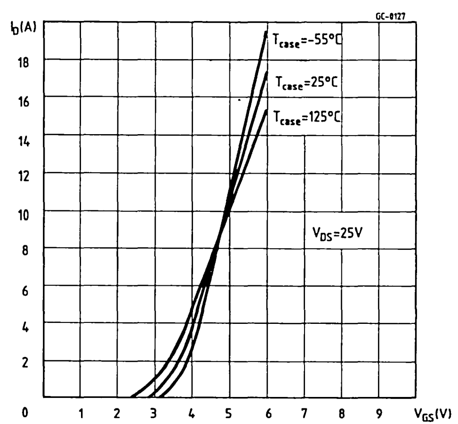
Output characteristics



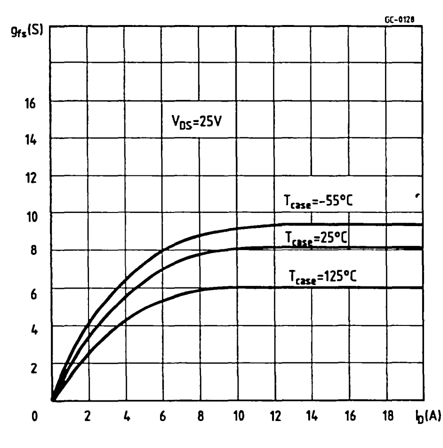
Static drain-source on resistance



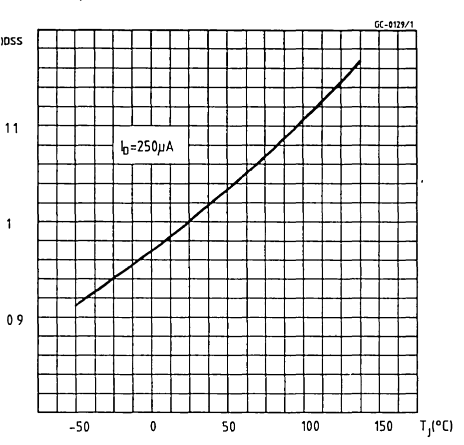
Transfer characteristics

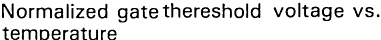


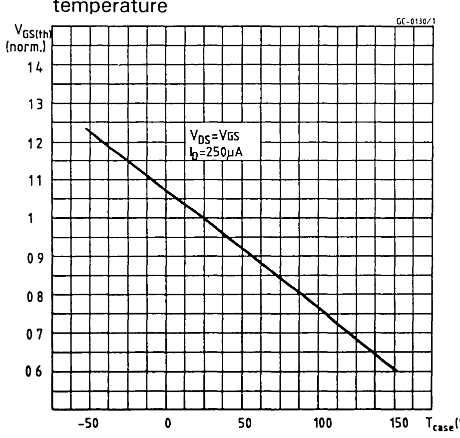
Transconductance



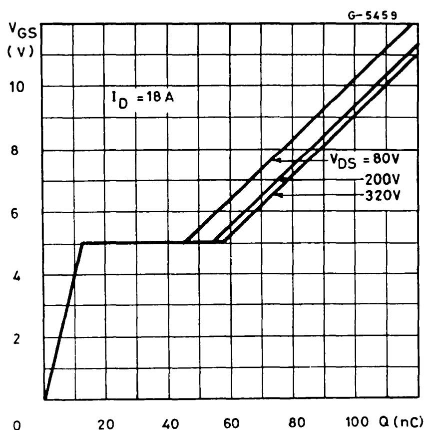
Normalized breakdown voltage vs. temperature



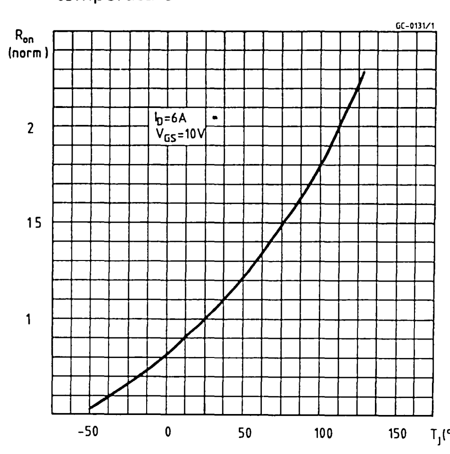

Normalized gate thereshold voltage vs. temperature



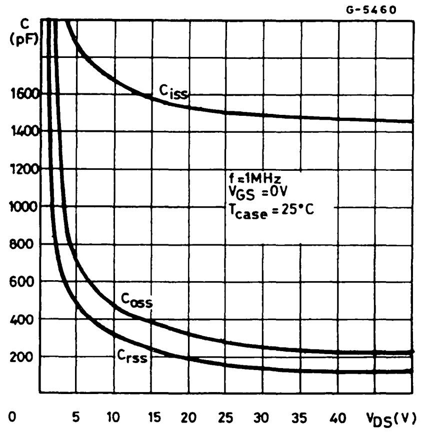
Gate charge vs. gate-source voltage



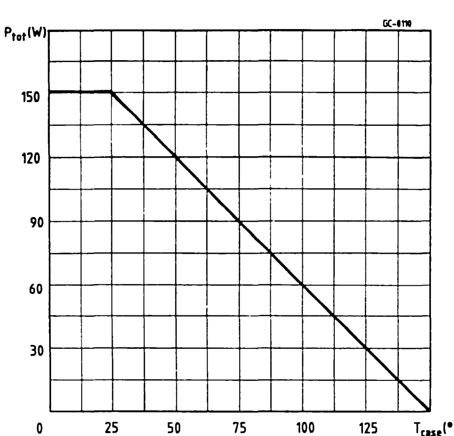
Normalized on resistance vs. temperature



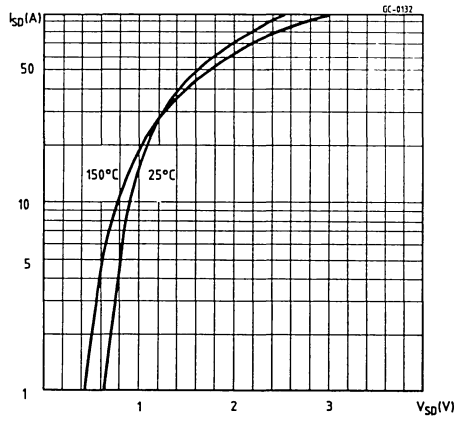
Capacitance variation



Derating curves



Source-drain diode forward characteristics



SGSP478/P479
SGSP578/P579

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

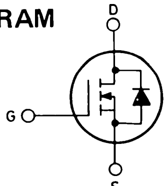
V_{DSS}	$R_{DS(ON)}$	I_D
500V	0.70Ω	10A
550V	1.00Ω	10A

ABSOLUTE MAXIMUM RATINGS

	SOT-93 TO-3	SGSP478 SGSP578	SGSP479 SGSP579
V_{DS}	Drain-source voltage (V_{GS} = 0)	550V	500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	550V	500V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	10A	
	T_{case} = 100°C	6.3A	
I_{DM}(•)	Drain current (pulsed)	40A	
I_{DLM} (•)	Drain inductive current, clamped	40A	
P_{tot}	Total dissipation at T_{case} = 25°C	150W	
	Derating factor	1.2W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

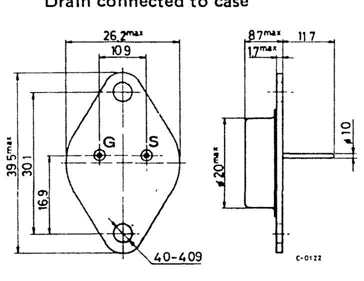
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

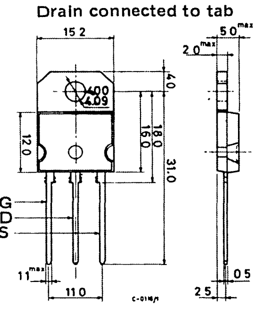
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.84 °C/W
T_L	Maximum lead temperature for soldering purpose		275 °C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit

OFF

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP478/P578** for **SGSP479/P579**	 550 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA

ON*

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 5A for **SGSP478/P578** for **SGSP479/P579**			 5 3.5	 V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5 A for **SGSP478/P578** for **SGSP479/P579**			 1.0 0.7	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 5 A	5			mho

DYNAMIC

Parameter		Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	1900	pF
C_{oss}	Output capacitance			230	280	pF
C_{rss}	Reverse transfer capacitance			140	170	pF

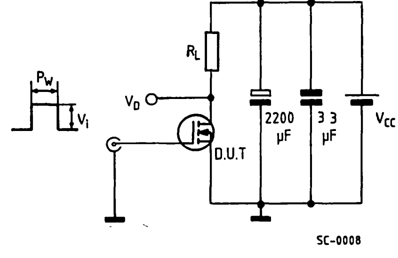
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 250 V I_D = 5 A		25		ns
t_r	Rise time	V_i = 10 V R_l = 10Ω		30		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				10	A
I_{SDM}(•)	Source drain current (pulsed)				40	A
V_{SD}	Forward on voltage	I_{SD} = 10 A V_{GS} = 0			1.15	V
t_{on}	Turn-on time	I_{SD} = 10 A V_{GS} = 0		75		ns
t_{rr}	Reverse recovery time	di/dt = 100 A/μs		500		ns

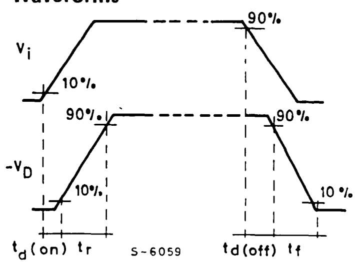
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

SWITCHING TIMES RESISTIVE LOAD

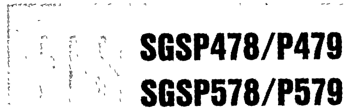
Test circuit



Waveforms

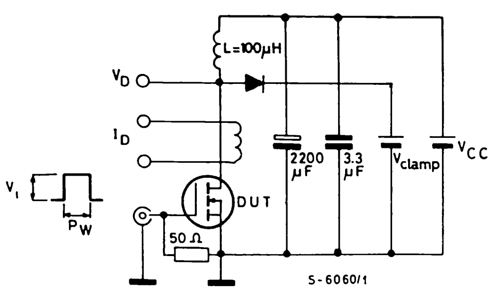


Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

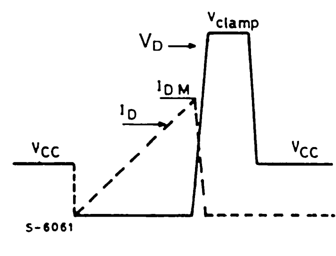


CLAMPED INDUCTIVE LOAD

Test circuit



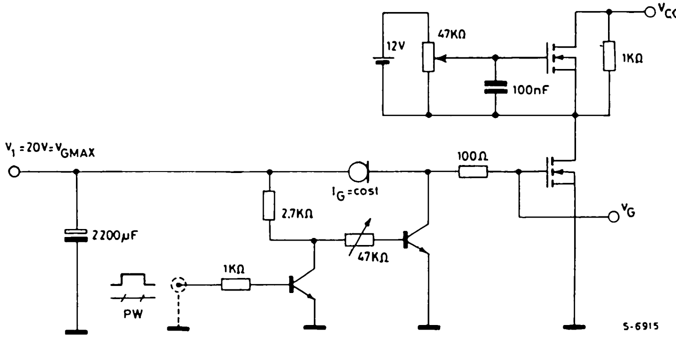
Waveforms



V_I = 12V

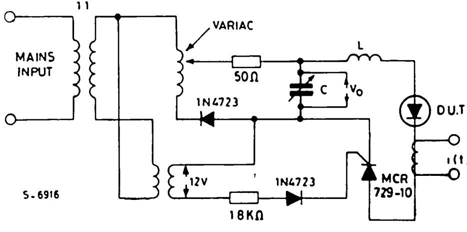
Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$

GATE CHARGE TEST CIRCUIT



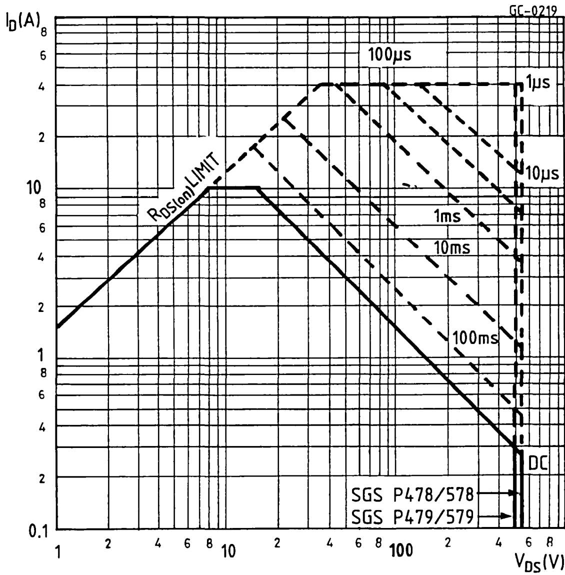
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

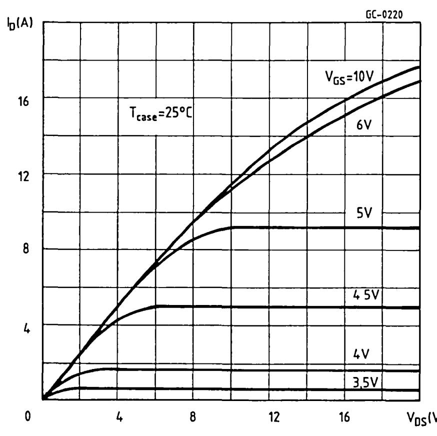


Jedec test circuit

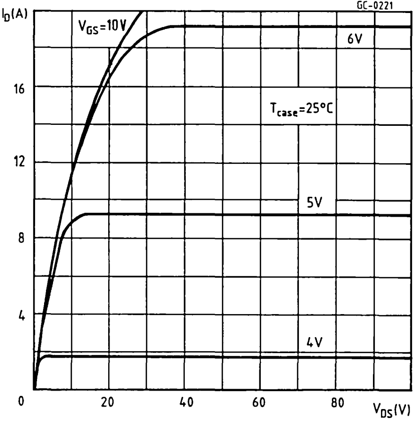
Safe operating areas



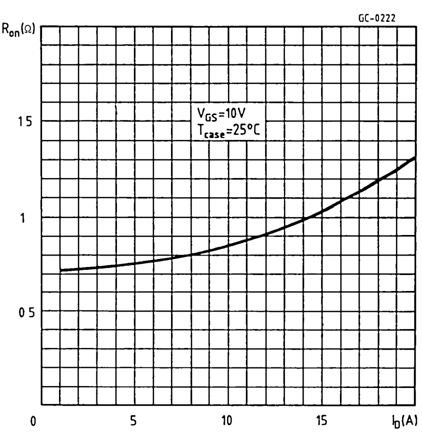
Output characteristics.



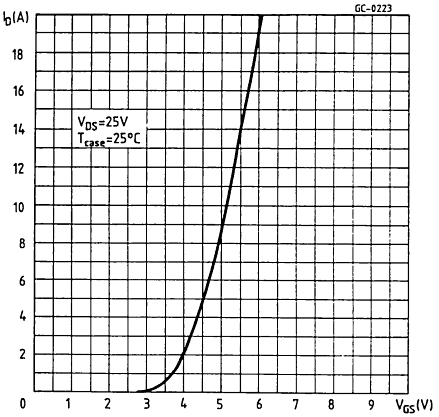
Output characteristics.



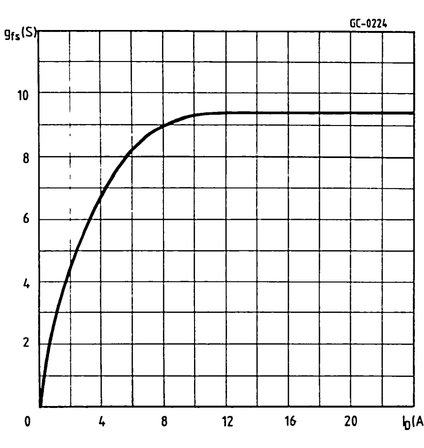
Static drain-source on resistance.



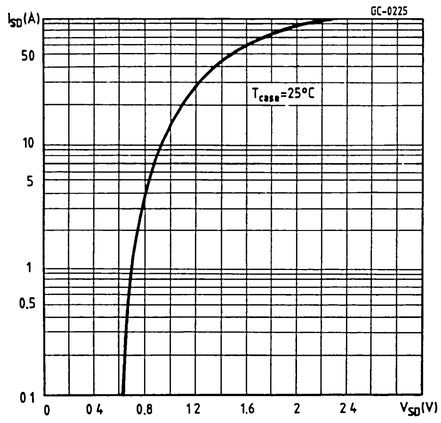
Transfer characteristic.



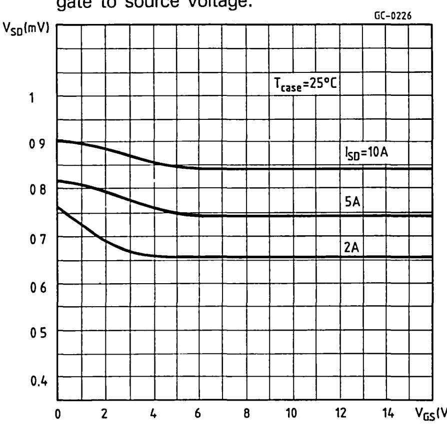
Transconductance.



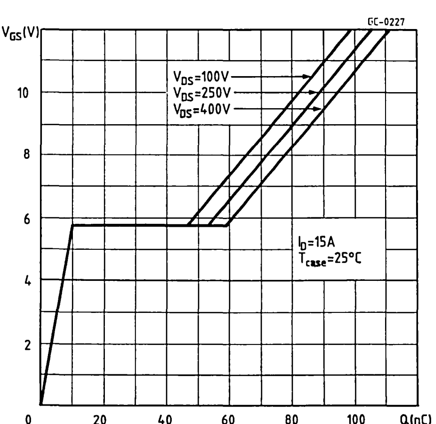
Source-drain diode forward voltage.



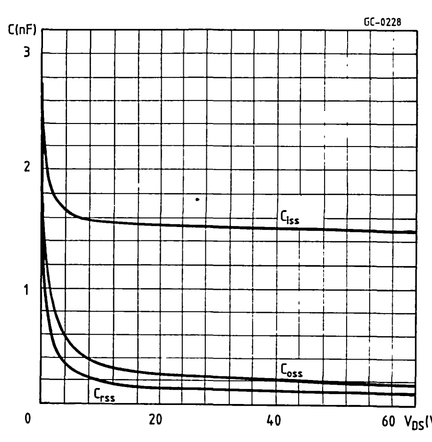
Source-drain diode forward voltage vs. gate to source voltage.



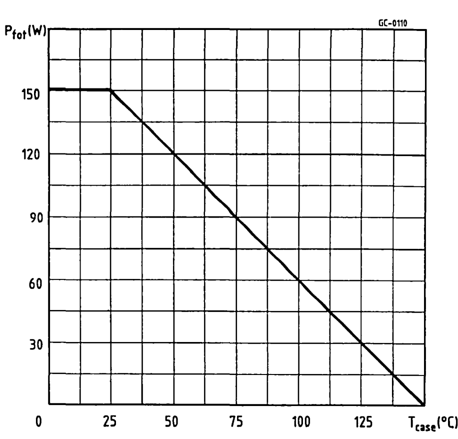
Gate charge vs. gate to source voltage.



Capacitances variation.



Derating curve.



SGSP491/P492
SGSP591/P592

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

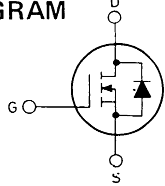
V_{DSS}	$R_{DS(ON)}$	I_D
50V	0.050Ω	40A
60V	0.033Ω	40A

ABSOLUTE MAXIMUM RATINGS

	SOT-93 TO-3	SGSP491 SGSP591	SGSP492 SGSP592
V_{DS}	Drain-source voltage (V_{GS} = 0)	60V	50V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	60V	50V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	40A	
	at T_{case} = 100°C	25A	
I_{DM}(•)	Drain current (pulsed)	120A	
I_{DLM} (•)	Drain inductive current, clamped	120A	
P_{tot}	Total dissipation at T_{case} = 25°C	150W	
	Derating factor	1.2W/°C	
T_{stg}	Storage temperature	-55 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

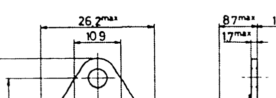
INTERNAL SCHEMATIC DIAGRAM

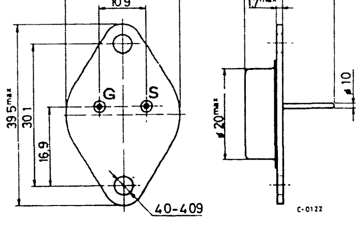


MECHANICAL DATA

Dimension in mm

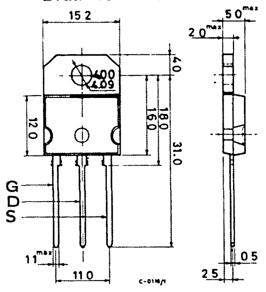
Drain connected to case





TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		275 °C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit

OFF

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 V for **SGSP491/P591** for **SGSP492/P592**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating			250	μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA

ON*

Parameter		Test conditions	Min.	Typ.	Max.	Unit
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 10V I_D = 20A for **SGSP491-P591** for **SGSP492/P592** V_{GS} = 10V I_D = 40 A for **SGSP491-P591** for **SGSP492-P592** V_{GS} = 10V I_D = 20 A T_{case} = 100°C for **SGSP491-P591** for **SGSP492-P592**			 1 0.66 2.2 1.6 2 1.33	 V V V V V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A for **SGSP491-591** for **SGSP492-P592**			 50 33	 mΩ mΩ
g_{fs}	Forward transconductance	V_{DS} = 25V I_D = 20 A	10			mho

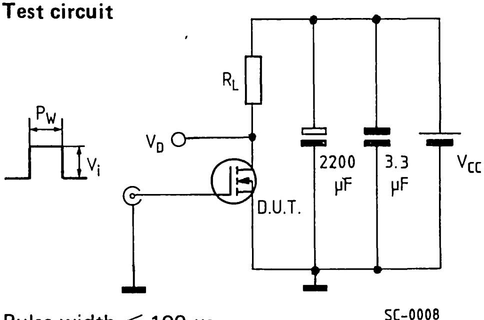
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz		1900	2500	pF
C_{oss}	Output capacitance	V_{DS} = 0		1200		pF
C_{rss}	Reverse transfer capacitance			600		pF
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{CC} = 30V I_D = 20A		35		ns
t_r	Rise time	V_i = 10 V R_i = 4.7Ω		40		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		60		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current				40	A
I_{SDM}(•)	Source drain current (pulsed)				120	A
V_{SD}	Forward on voltage	I_{SD} = 40 A V_{GS} = 0			1.4	V
t_{on}	Turn-on time	I_{SD} = 40 A V_{GS} = 0		200		ns
t_{rr}	Reverse recovery time	di/dt = 100 A/μS		120		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.

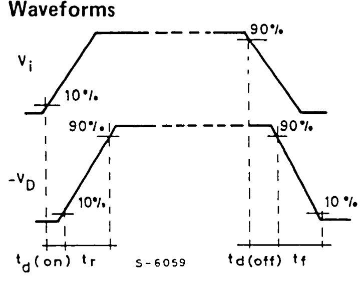
SWITCHING TIMES RESISTIVE LOAD

Test circuit



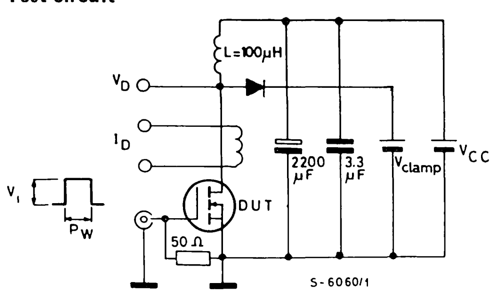
Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_I = 10V

Waveforms

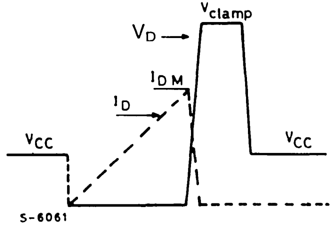


CLAMPED INDUCTIVE LOAD

Test circuit

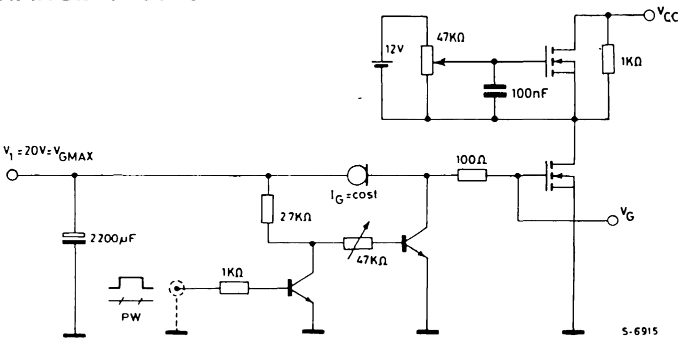


Waveforms



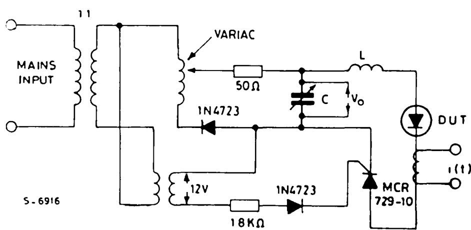
V_I = 12V
Pulse width: adjusted to obtain specified I_{DM}

GATE CHARGE TEST CIRCUIT



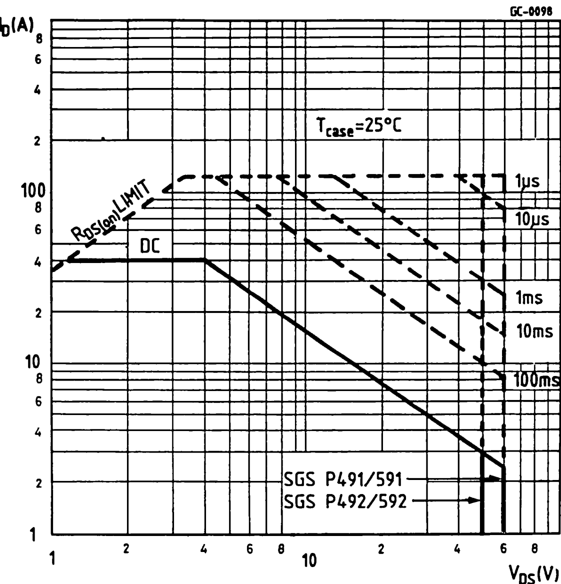
PW adjusted to obtain required V_G

DIODE BODY-DRAIN t_{rr} MEASUREMENT

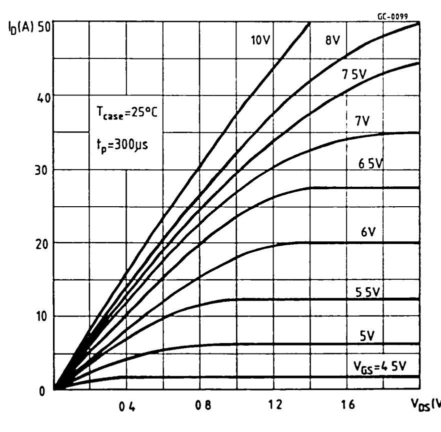


Jedec test circuit

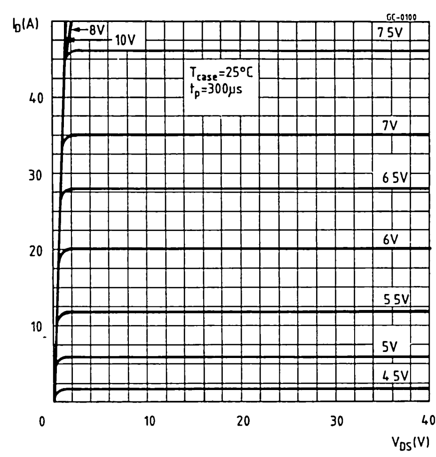
Safe operating areas



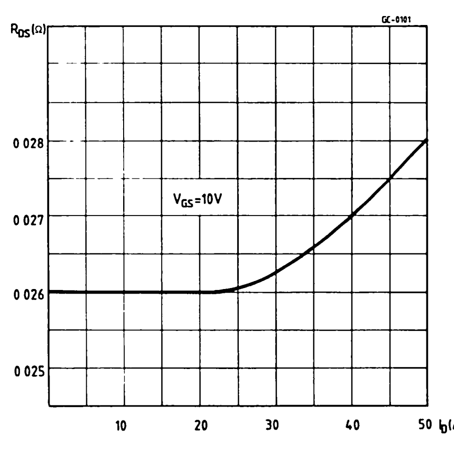
Output characteristics



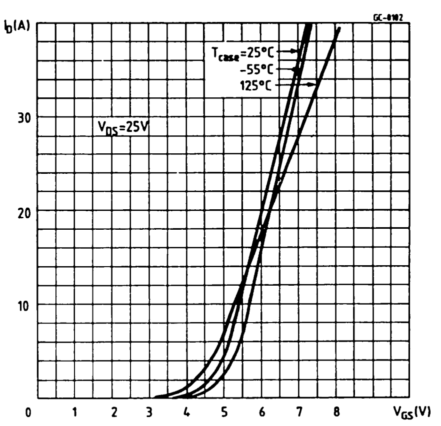
Output characteristics



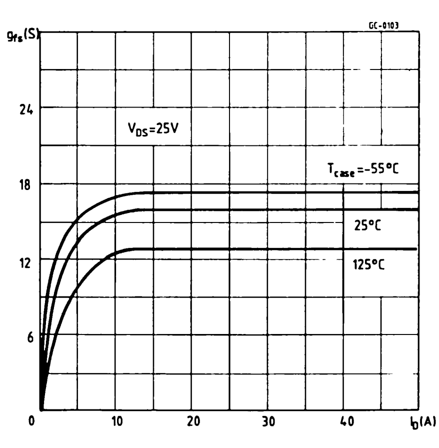
Static drain-source on resistance



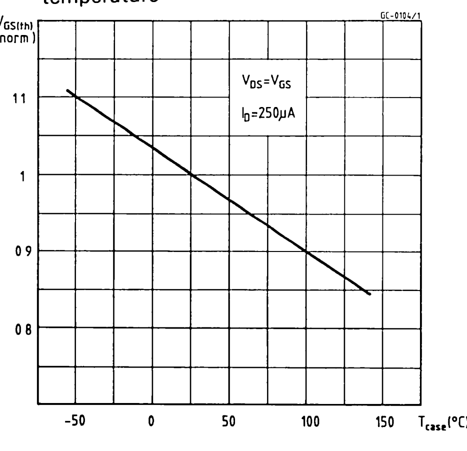
Transfer characteristics

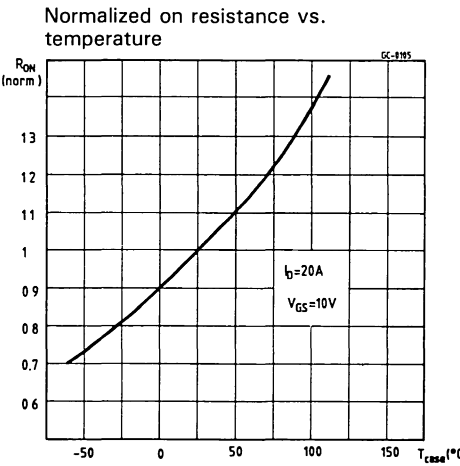


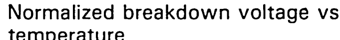
Transconductance



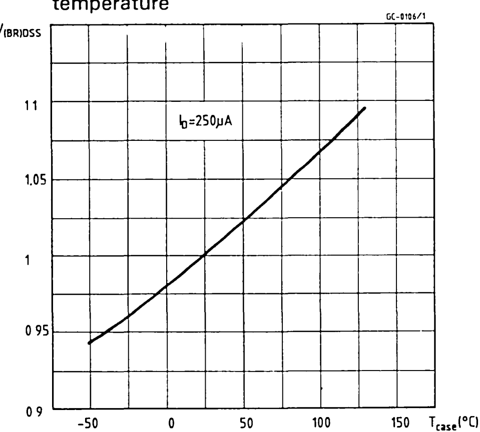
Normalized gate treshold voltage vs. temperature



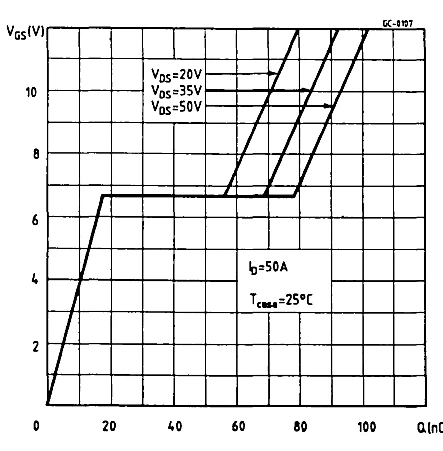




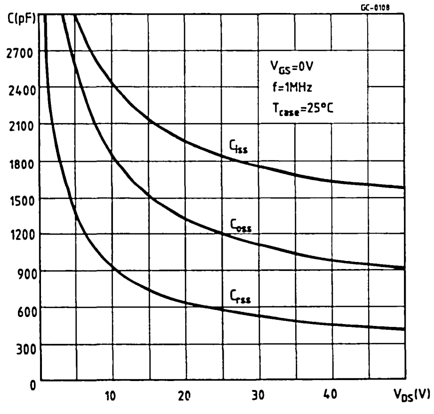
Normalized breakdown voltage vs. temperature



Gate charge vs. gate to source voltage

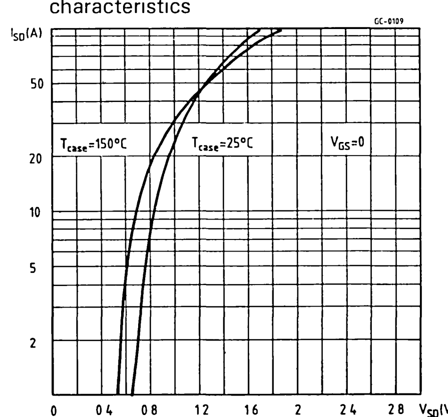


Capacitance variation

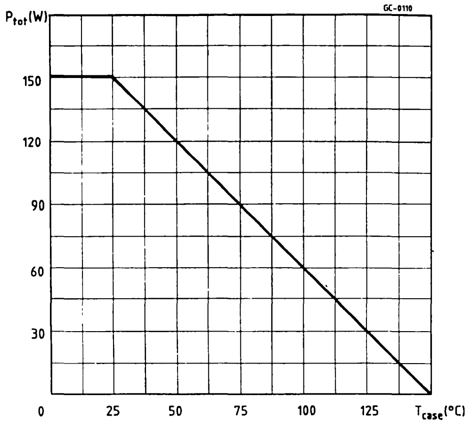


SGSP491/P492
SGSP591/P592

Source-drain diode forward characteristics



Derating curves



SEF120
SEF121
SEF122
SEF123

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

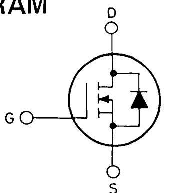
V_{DSS}	$R_{DS\,(ON)}$	I_D
100V/60V	**0.3 Ω**	**8A**
100V/60V	**0.4 Ω**	**7A**

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	SEF120	SEF121	SEF122	SEF123
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	8A	8A	7A	7A
	at T_{case} = 100°C	5A	5A	4A	4A
I_{DM}(•)	Drain current (pulsed)	32A	32A	28A	28A
I_{DLM}(•)	Drain inductive current, clamped	32A	32A	28A	28A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

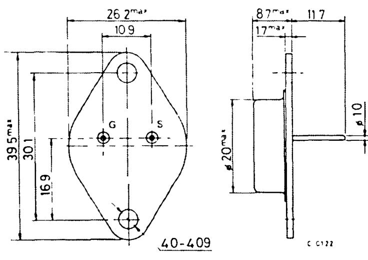
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

SEF120
SEF121
SEF122
SEF123

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF120/SEF122** for **SEF121/SEF123**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF120/SEF121** for **SEF122/SEF123**	 8 7			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A for **SEF120/SEF121** for **SEF122/SEF123**		 0.2 0.2	 0.3 0.4	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 4A	1.5	3.7		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		375 180 90	480 230 110	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$			40	ns
t_r	Rise time	I_D = 4 A			70	ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω			100	ns
t_f	Fall time	(see test circuit)			70	ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF120/SEF121**			8	A
		for **SEF122/SEF123**			7	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF120/SEF121**			32	A
		for **SEF122/SEF123**			28	A
V_{SD}	Forward on voltage	for **SEF120/SEF121** I_{SD} = 8 A V_{GS} = 0			2.5	V
		for **SEF122/SEF123** I_{SD} = 7 A V_{GS} = 0			2.3	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A T_j = 150°C di/dt = 100 A/μs		280		ns
Q_{rr}	Reverse recovered charge			1.6		μC

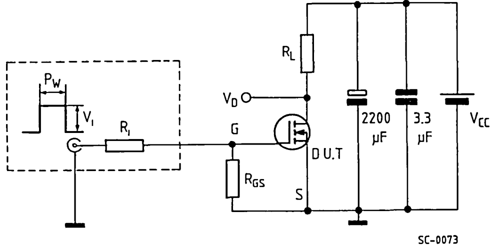
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

(•) Pulse width limited by safe operating area.

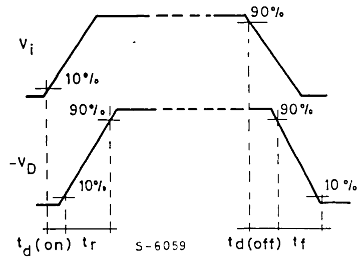
For typical curves, clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP311 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
$V_i = 10V$

SEF130
SEF131
SEF132
SEF133

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

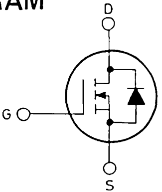
V_{DSS}	$R_{DS\ (ON)}$	I_D
100V/60V	0.18 Ω	14A
100V/60V	0.25 Ω	12A

ABSOLUTE MAXIMUM RATINGS

		SEF130	SEF131	SEF132	SEF133
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	14A	14A	12A	12A
	at T_{case} = 100°C	9A	9A	8A	8A
I_{DM}(•)	Drain current (pulsed)	56A	56A	48A	48A
I_{DLM}(•)	Drain inductive current, clamped	56A	56A	48A	48A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

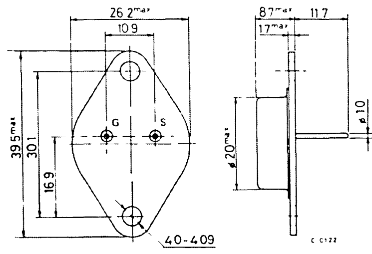
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF130/SEF132** for **SEF131/SEF133**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF130/SEF131** for **SEF132/SEF133**	 14 12			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 8 A for **SEF130/SEF131** for **SEF132/SEF133**		 0.085 0.085	 0.18 0.25	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 8 A	4	8.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950 370 180	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 36 V I_D = 8 A		25		ns
t_r	Rise time	R_l = 15 Ω R_{GS} = 15 Ω		30		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		40		ns
t_f	Fall time			15		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF130/SEF131**			14	A
		for **SEF132/SEF133**			12	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF130/SEF131**			56	A
		for **SEF132/SEF133**			48	A
V_{SD}	Forward on voltage	for **SEF130/SEF131** I_{SD} = 14 A V_{GS} = 0			2.5	V
		for **SEF132/SEF133** I_{SD} = 12 A V_{GS} = 0			2.3	V
t_{rr}	Reverse recovery time	I_{SD} = 14 A T_j = 150°C		360		ns
Q_{rr}	Reverse recovered charge	di/dt = 100 A/μs		2.1		μC

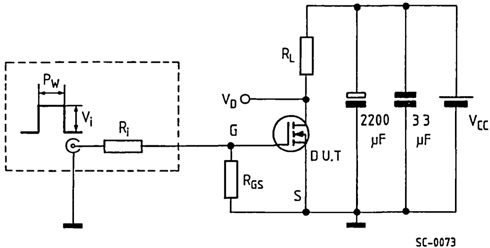
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

(•) Pulse width limited by safe operating area.

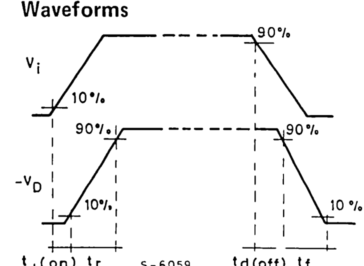
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP361 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
$V_i = 10V$

SEF140
SEF141
SEF142
SEF143

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

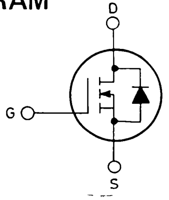
V_{DSS}	$R_{DS\ (ON)}$	I_D
100V/60V	0.085 Ω	27A
100V/60V	0.11 Ω	24A

ABSOLUTE MAXIMUM RATINGS

		SEF140	SEF141	SEF142	SEF143
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	27A	27A	24A	24A
	at T_{case} = 100°C	17A	17A	15A	15A
I_{DM}(•)	Drain current (pulsed)	108A	108A	96A	96A
I_{DLM}(•)	Drain inductive current, clamped	108A	108A	96A	96A
P_{tot}	Total power dissipation at T_{case} = 25°C	125W			
	Derating factor	1W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

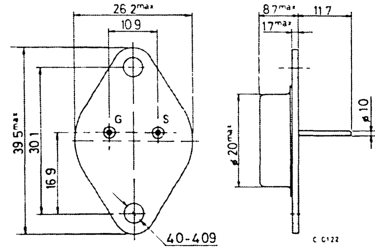
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF140/SEF142** for **SEF141/SEF143**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	$V_{DS} > I_{D\ (on)} X R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF140/SEF141** for **SEF142/SEF143**	 27 24			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 15 A for **SEF140/SEF141** for **SEF142/SEF143**		 36 36	 85 110	 mΩ mΩ
g_{fs}	Forward transconductance	$V_{DS} > I_{D\ (on)} X R_{DS\ (on)\ max}$ I_D = 15 A	6	14		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1800 650 300	2200 810 375	pF pF pF

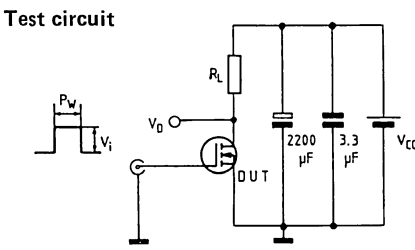
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 30 V I_D = 15 A		30		ns
t_r	Rise time	R_i = 4.7 Ω		60		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF140/SEF141**			27	A
		for **SEF142/SEF143**			24	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF140/SEF141**			108	A
		for **SEF142/SEF143**			96	A
V_{SD}	Forward on voltage	for **SEF140/SEF141** I_{SD} = 27 A V_{GS} = 0			2.5	V
		for **SEF142/SEF143** I_{SD} = 24 A V_{GS} = 0			2.3	V
t_{rr}	Reverse recov. time	I_{SD} = 27 A T_j = 150°C di/dt = 100 A/μs		500		ns
Q_{rr}	Reverse recovered charge			2.9		μC

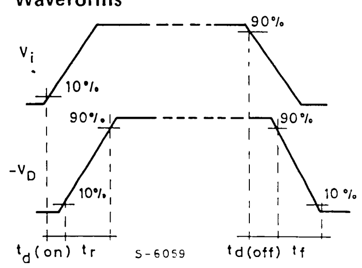
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP571 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
V_i = 10V

SEF150
SEF151
SEF152
SEF153

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

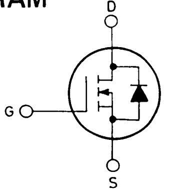
V_{DSS}	$R_{DS\ (ON)}$	I_D
100V/60V	0.055 Ω	40A
100V/60V	0.08 Ω	33A

ABSOLUTE MAXIMUM RATINGS

		SEF150	SEF151	SEF152	SEF153
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20K Ω)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	40A	40A	33A	33A
	at T_{case} = 100°C	25A	25A	20A	20A
I_{DM}(•)	Drain current (pulsed)	160A	160A	132A	132A
I_{DLM}(•)	Drain inductive current, clamped	160A	160A	132A	132A
P_{tot}	Total power dissipation at T_{case} = 25°C	150W			
	Derating factor	1.2W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

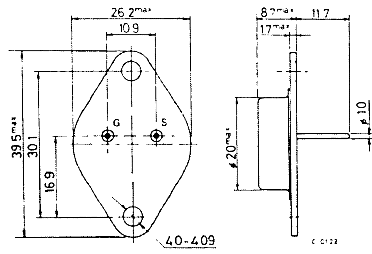
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF150/SEF152** for **SEF151/SEF153**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF150/SEF151** for **SEF152/SEF153**	 40 33			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A for **SEF150/SEF151** for **SEF152/SEF153**		 35 35	 55 80	 mΩ mΩ
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 20 A	9	17		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{DS} = 0		1800 650 300	2200 810 375	pF pF pF

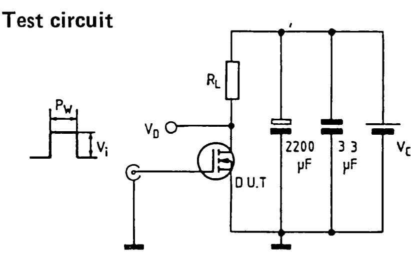
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	V_{CC} = 24 V I_D = 20 A			35	ns
t_r	Rise time	R_l = 10 Ω			100	ns
$t_{d\,(off)}$	Turn-off delay time	(see test circuit)			125	ns
t_f	Fall time				100	ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF150/SEF151**			40	A
		for **SEF152/SEF153**			33	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF150/SEF151**			160	A
		for **SEF152/SEF153**			132	A
V_{SD}	Forward on voltage	for **SEF150/SEF151** I_{SD} = 40 A V_{GS} = 0			2.5	V
		for **SEF152/SEF153** I_{SD} = 33 A V_{GS} = 0			2.3	V
t_{rr}	Reverse recov. time	I_{SD} = 40 A T_j = 150°C di/dt = 100 A/μs		600		ns
Q_{rr}	Reverse recovered charge			3.3		μC

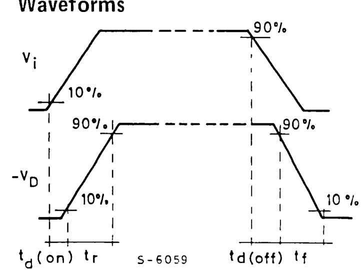
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP571 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

SEF220
SEF221
SEF222
SEF223

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

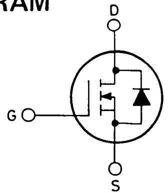
V_{DSS}	$R_{DS\,(ON)}$	I_D
200V/150V	0.8 Ω	5A
200V/150V	1.2 Ω	4A

ABSOLUTE MAXIMUM RATINGS

		SEF220	SEF221	SEF222	SEF223
V_{DS}	Drain-source voltage (V_{GS} = 0)	200V	150V	200V	150V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	200V	150V	200V	150V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	5A	5A	4A	4A
	at T_{case} = 100°C	3A	3A	2.5A	2.5A
I_{DM}(•)	Drain current (pulsed)	20A	20A	16A	16A
I_{DLM}(•)	Drain inductive current, clamped	20A	20A	16A	16A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

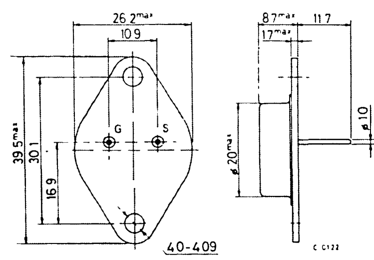
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

9/85

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF220/SEF222** for **SEF221/SEF223**	 200 150			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF220/SEF221** for **SEF222/SEF223**	 5 4			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **SEF220/SEF221** for **SEF222/SEF223**		 0.43 0.43	 0.8 1.2	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 2.5 A	1.3	3		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		380 100 50	500 130 65	pF pF pF

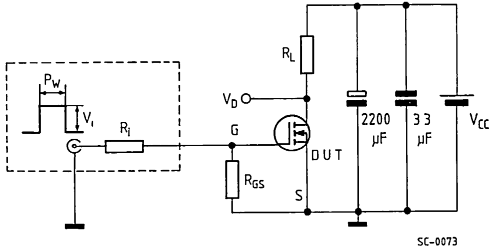
ELECTRICAL CHARACTERISTICS (continued)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	$V_{CC} = 0.5\ V_{(BR)DSS}$			80	ns
t_r	Rise time	$I_D = 2.5$ A			40	ns
$t_{d\,(off)}$	Turn-off delay time	$R_{GS} = 50\ \Omega$ $R_i = 50\ \Omega$			100	ns
t_f	Fall time	(see test circuit)			60	ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF220/SEF221**			5	A
		for **SEF222/SEF223**			4	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF220/SEF221**			20	A
		for **SEF222/SEF223**			16	A
V_{SD}	Forward on voltage	for **SEF220/SEF221** $I_{SD} = 5$ A $V_{GS} = 0$			2	V
		for **SEF222/SEF223** $I_{SD} = 4$ A $V_{GS} = 0$			1.8	V
t_{rr}	Reverse recovery time	$I_{SD} = 5$ A $T_j = 150°C$ di/dt = 100 A/μs		350		ns
Q_{rr}	Reverse recoved charge			2.3		μC

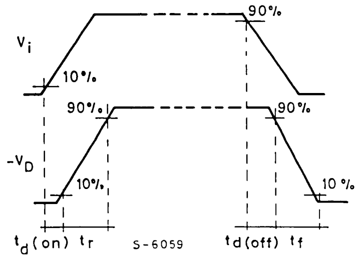
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP517 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10V$

N-CHANNEL POWER MOS TRANSISTORS

SEF230
SEF231
SEF232
SEF233

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

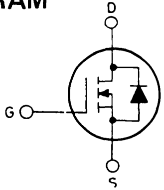
V_{DSS}	$R_{DS\ (ON)}$	I_D
200V/150V	**0.4 Ω**	**9A**
200V/150V	**0.6 Ω**	**8A**

ABSOLUTE MAXIMUM RATINGS

		SEF230	SEF231	SEF232	SEF233
V_{DS}	Drain-source voltage (V_{GS} = 0)	200V	150V	200V	150V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	200V	150V	200V	150V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	9A	9A	8A	8A
	at T_{case} = 100°C	6A	6A	5A	5A
I_{DM}(•)	Drain current (pulsed)	36A	36A	32A	32A
I_{DLM}(•)	Drain inductive current, clamped	36A	36A	32A	32A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

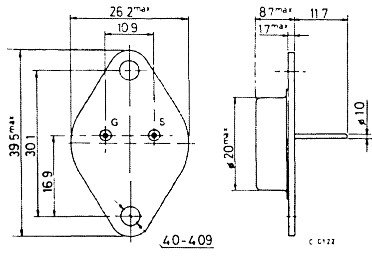
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF230/SEF232** for **SEF231/SEF233**	 200 150			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	$V_{DS} > I_{D\ (on)} X R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF230/SEF231** for **SEF232/SEF233**	 9 8			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5 A for **SEF230/SEF231** for **SEF232/SEF233**		 0.25 0.25	 0.4 0.6	 Ω Ω
g_{fs}	Forward transconductance	$V_{DS} > I_{D\ (on)} X R_{DS\ (on)\ max}$ I_D = 5 A	3	7		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		980 200 80	1200 260 100	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 90 V I_D = 5 A		30		ns
t_r	Rise time	R_{GS} = 15 Ω R_l = 15 Ω		50		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		50		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF230/SEF231**			9	A
		for **SEF232/SEF233**			8	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF230/SEF231**			36	A
		for **SEF232/SEF233**			32	A
V_{SD}	Forward on voltage	for **SEF230/SEF231** I_{SD} = 9 A V_{GS} = 0			2	V
		for **SEF232/SEF233** I_{SD} = 8 A V_{GS} = 0			1.8	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A T_j = 150°C di/dt = 100 A/μs		450		ns
Q_{rr}	Reverse recoved charge			3		μC

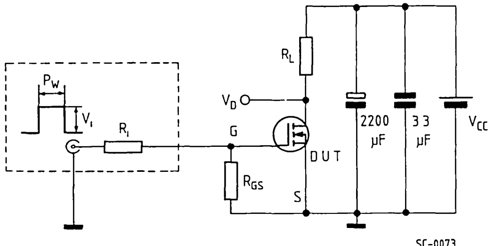
* Pulsed: pulse duration ⩽ 300μs duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

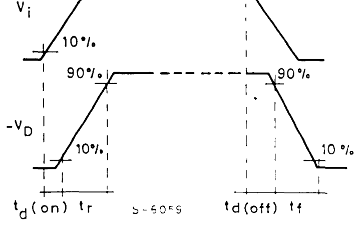
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP563 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

SEF240
SEF241
SEF242
SEF243

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

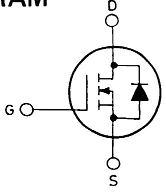
V_{DSS}	$R_{DS\,(ON)}$	I_D
200V/150V	0.18 Ω	18A
200V/150V	0.22 Ω	16A

ABSOLUTE MAXIMUM RATINGS

		SEF240	SEF241	SEF242	SEF243
V_{DS}	Drain-source voltage (V_{GS} = 0)	200V	150V	200V	150V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	200V	150V	200V	150V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	18A	18A	16A	16A
	at T_{case} = 100°C	11A	11A	10A	10A
I_{DM}(•)	Drain current (pulsed)	72A	72A	64A	64A
I_{DLM}(•)	Drain inductive current, clamped	72A	72A	64A	64A
P_{tot}	Total power dissipation at T_{case} = 25°C	125W			
	Derating factor	1W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

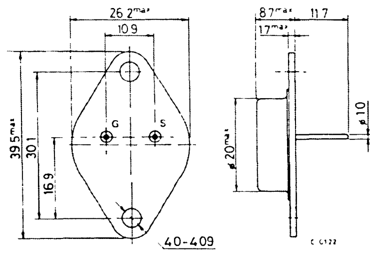
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1 °C/W
T_L	Maximum lead temperature for soldering purpose		300 °C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SEF240/SEF242** for **SEF241/SEF243**	 200 150			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25 °C V_{DS} = Max. Rating X0.8 T_{case} = 125 °C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X $R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF240/SEF241** for **SEF242/SEF243**	 18 16			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A for **SEF240/SEF241** for **SEF242/SEF243**		 0.11 0.11	 0.18 0.22	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X $R_{DS\ (on)\ max}$ I_D = 10 A	6	14		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1800 450 220	2200 550 260	pF pF pF

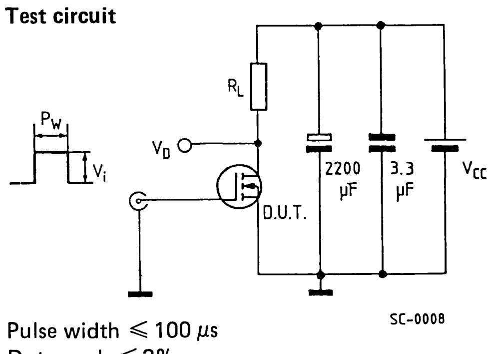
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 75 V I_D = 10 A		30		ns
t_r	Rise time	R_i = 4.7 Ω		60		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			60		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF240/SEF241**			18	A
		for **SEF242/SEF243**			16	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF240/SEF241**			72	A
		for **SEF242/SEF243**			64	A
V_{SD}	Forward on voltage	for **SEF240/SEF241** I_{SD} = 18 A V_{GS} = 0			2	V
		for **SEF242/SEF243** I_{SD} = 16 A V_{GS} = 0			1.9	V
t_{rr}	Turn-on time	I_{SD} = 18 A T_j = 150°C		650		ns
Q_{rr}	Reverse recovered charge	di/dt = 100 A/μs		4.1		μC

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP573 Datasheet.

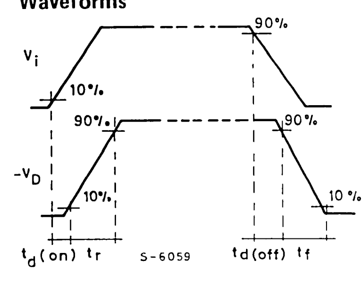
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEF320
SEF321
SEF322
SEF323

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

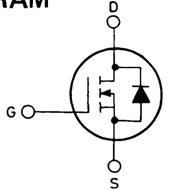
V_{DSS}	$R_{DS\ (ON)}$	I_D
400V/350V	1.8 Ω	3 A
400V/350V	2.5 Ω	2.5A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	SEF320	SEF321	SEF322	SEF323
V_{DS}	Drain-source voltage (V_{GS} = 0)	400V	350V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	400V	350V	400V	350V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	3A	3A	2.5A	2.5A
	at T_{case} = 100°C	2A	2A	1.5A	1.5A
$I_{DM}(\bullet)$	Drain current (pulsed)	12A	12A	10A	10A
$I_{DLM}(\bullet)$	Drain inductive current, clamped	12A	12A	10A	10A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

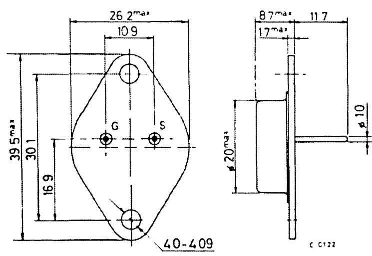
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF320/SEF322** for **SEF321/SEF323**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF320/SEF321** for **SEF322/SEF323**	 3 2.5			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.5 A for **SEF320/SEF321** for **SEF322/SEF323**		 0.7 0.7	 1.8 2.5	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 1.5 A	1	5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 100	1000 200 130	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

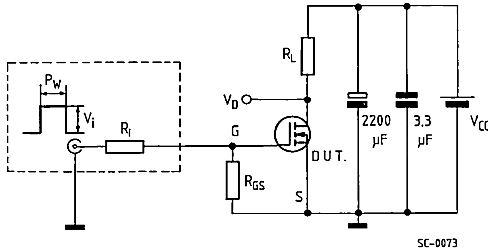
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		40		ns
t_r	Rise time	I_D = 1.5 A		50		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		100		ns
t_f	Fall time	(see test circuit)		50		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF320/SEF321**			3	A
		for **SEF322/SEF323**			2.5	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF320/SEF321**			12	A
		for **SEF322/SEF323**			10	A
V_{SD}	Forward on voltage	for **SEF320/SEF321** I_D = 3 A V_{GS} = 0			1.6	V
		for **SEF322/SEF323** I_D= 2.5 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 3 A di/dt = 100 A/μs T_j = 150°C		450		ns
Q_{rr}	Reverse recovered charge			3.1		μC

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

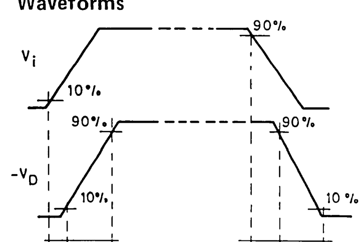
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP564 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
V_i = 10V

SEF330
SEF331
SEF332
SEF333

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

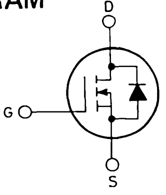
These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	$R_{DS\ (ON)}$	I_D
400V/350V	1 Ω	5.5A
400V/350V	1.5 Ω	4.5A

ABSOLUTE MAXIMUM RATINGS

		SEF330	SEF331	SEF332	SEF333
V_{DS}	Drain-source voltage (V_{GS} = 0)	400V	350V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	400V	350V	400V	350V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	5.5A	5.5A	4.5A	4.5A
	at T_{case} = 100°C	3.5A	3.5A	3A	3A
I_{DM}(•)	Drain current (pulsed)	22A	22A	18A	18A
I_{DLM}(•)	Drain inductive current, clamped	22A	22A	18A	18A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

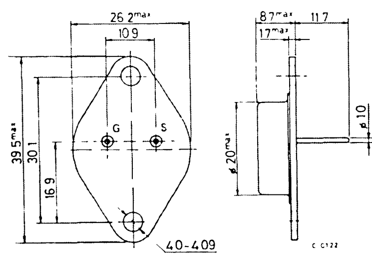
(•) Pulse width limited by safe operating area



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

9/85

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF330/SEF332** for **SEF331/SEF333**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF330/SEF331** for **SEF332/SEF333**	 5.5 4.5			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.5 A for **SEF330/SEF331** for **SEF332/SEF333**		 0.7 0.7	 1 1.5	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 1.5 A	3	5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 100	1000 200 130	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$t_{d\,(on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		30		ns
t_r	Rise time	I_D = 1.5 A		35		ns
$t_{d\,(off)}$	Turn-off delay time	R_{GS} = 15 Ω R_i = 15 Ω		55		ns
t_f	Fall time	(see test circuit)		35		ns

SOURCE DRAIN DIODE

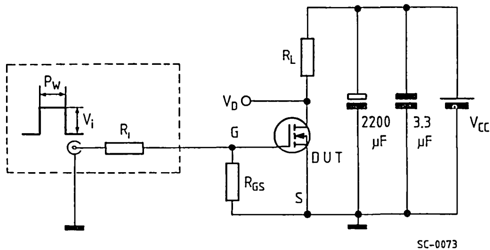
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
I_{SD}	Source drain current	for **SEF330/SEF331**			5.5	A
		for **SEF332/SEF333**			4.5	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF330/SEF331**			22	A
		for **SEF332/SEF333**			18	A
V_{SD}	Forward on voltage	for **SEF330/SEF331** I_D = 3 A V_{GS} = 0			1.6	V
		for **SEF332/SEF333** I_D = 2.5 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A di/dt = 100 A/μs		600		ns
Q_{rr}	Reverse recovered charge	T_j = 150°C		4		μC

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP564 Datasheet.

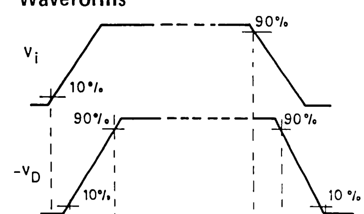
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEF340
SEF341
SEF342
SEF343

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

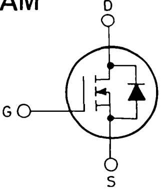
V_{DSS}	$R_{DS(ON)}$	I_D
400V/350V	0.55 Ω	10A
400V/350V	0.80 Ω	8 A

ABSOLUTE MAXIMUM RATINGS

		SEF340	SEF341	SEF342	SEF343
V_{DS}	Drain-source voltage (V_{GS} = 0)	400V	350V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	400V	350V	400V	350V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	10A	10A	8A	8A
	at T_{case} = 100°C	6A	6A	5A	5A
I_{DM}(•)	Drain current (pulsed)	40A	40A	32A	32A
I_{DLM}(•)	Drain inductive current, clamped	40A	40A	32A	32A
P_{tot}	Total power dissipation at T_{case} = 25°C	125W			
	Derating factor	1W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

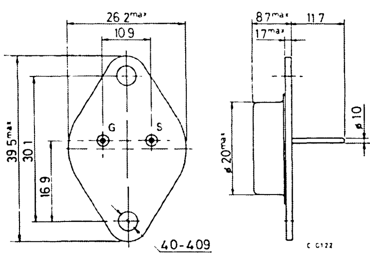
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

9/85

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1 °C/W
T_L	Maximum lead temperature for soldering purpose		300 °C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF340/SEF342** for **SEF341/SEF343**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25 °C V_{DS} = Max. Rating X0.8 T_{case} = 125 °C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF340/SEF341** for **SEF342/SEF343**	 10 8			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} > 10 V I_D = 5 A for **SEF340/SEF341** for **SEF342/SEF343**			 0.55 0.80	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} = $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 5 A	4	6.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600 300 200	1000 390 260	pF pF pF

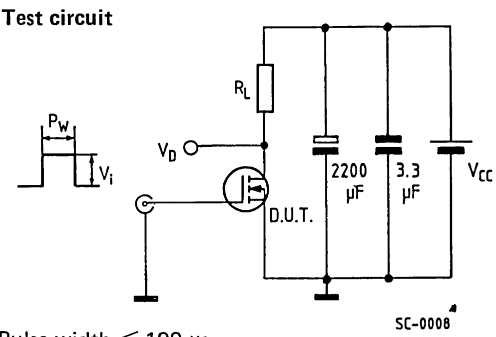
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 175 V I_D = 5 A		35		ns
t_r	Rise time	R_l = 4.7 Ω		15		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		90		ns
t_f	Fall time			35		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF340/SEF341**			10	A
		for **SEF342/SEF343**			8	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF340/SEF341**			40	A
		for **SEF342/SEF343**			32	A
V_{SD}	Forward on voltage	for **SEF340/SEF341** I_{SD} = 10 A V_{GS} = 0			2.0	V
		for **SEF342/SEF343** I_{SD}=8 A V_{GS} = 0			1.9	V
t_{rr}	Reverse recov. time	I_{SD} = 10 A T_j = 150°C di/dt = 100 A/μs		800		ns
Q_{rr}	Reverse recovered charge			5.7		μC

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP475 Datasheet.

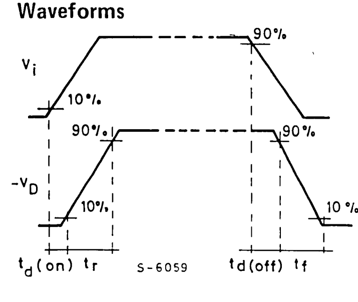
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



N-CHANNEL POWER MOS TRANSISTORS

SEF420
SEF421
SEF422
SEF423

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

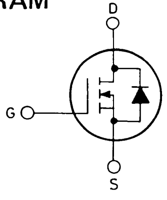
V_{DSS}	$R_{DS\,(ON)}$	I_D
500V/450V	3 Ω	2.5A
500V/450V	4 Ω	2 A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	SEF420	SEF421	SEF422	SEF423
V_{DS}	Drain-source voltage (V_{GS} = 0)	500V	450V	500V	450V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500V	450V	500V	450V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	2.5A	2.5A	2A	2A
	at T_{case} = 100°C	1.5A	1.5A	1A	1A
I_{DM}(•)	Drain current (pulsed)	10A	10A	8A	8A
I_{DLM}(•)	Drain inductive current, clamped	10A	10A	8A	8A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

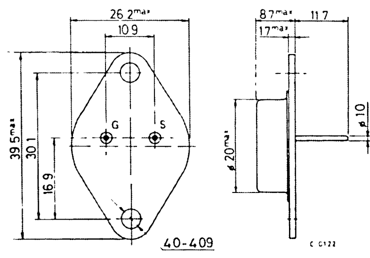
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF420/SEF422** for **SEF421/SEF423**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF420/SEF421** for **SEF422/SEF423**	 2.5 2			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A for **SEF420/SEF421** for **SEF422/SEF423**		 1.33 1.33	 3 4	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 2.5 A	1	3.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 80	1000 190 100	pF pF pF

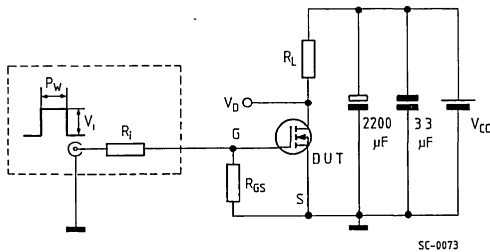
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		60		ns
t_r	Rise time	I_D = 1 A		50		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_l = 50 Ω		60		ns
t_f	Fall time	(see test circuit)		30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF420/SEF421**			2.5	A
		for **SEF422/SEF423**			2	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF420/SEF421**			10	A
		for **SEF422/SEF423**			8	A
V_{SD}	Forward on voltage	for **SEF420/SEF421**			1.4	V
		I_{SD} = 2.5 A V_{GS} = 0				
		for **SEF422/SEF423**				
		I_{SD} = 2 A V_{GS} = 0			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 2.5A T_j = 150°C di/dt = 100A/μs		600		ns
Q_{rr}	Reverse recovered charge			3.5		μC

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP569 Datasheet.

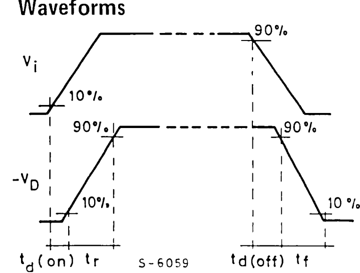
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEF430
SEF431
SEF432
SEF433

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

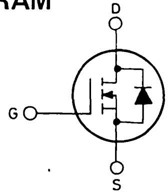
V_{DSS}	$R_{DS\,(ON)}$	I_D
500V/450V	1.5 Ω	4.5A
500V/450V	2 Ω	4 A

ABSOLUTE MAXIMUM RATINGS

		SEF430	SEF431	SEF432	SEF433
V_{DS}	Drain-source voltage (V_{GS} = 0)	500V	450V	500V	450V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500V	450V	500V	450V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	4.5A	4.5A	4A	4A
	at T_{case} = 100°C	3A	3A	2.5A	2.5A
I_{DM}(•)	Drain current (pulsed)	18A	18A	16A	16A
I_{DLM}(•)	Drain inductive current, clamped	18A	18A	16A	16A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

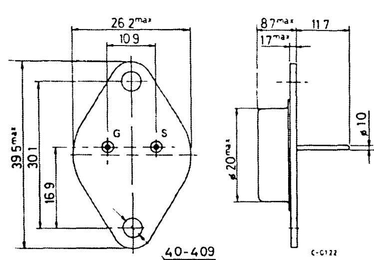
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF430/SEF432** for **SEF431/SEF433**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF430/SEF431** for **SEF432/SEF433**	 4.5 4.0			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **SEF430/SEF431** for **SEF432/SEF433**		 1.33 1.33	 1.5 2	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 2.5 A	2.5	3.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 80	1000 190 100	pF pF pF

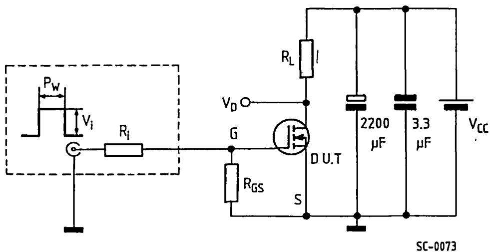
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 225 V I_D = 2.5 A		30		ns
t_r	Rise time	R_{GS} = 15 Ω R_i = 15 Ω		30		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		55		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF430/SEF431**			4.5	A
		for **SEF432/SEF433**			4	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF430/SEF431**			18	A
		for **SEF432/SEF433**			16	A
V_{SD}	Forward on voltage	for **SEF430/SEF431** I_{SD} = 4.5 A V_{GS} = 0			1.4	V
		for **SEF432/SEF433** I_{SD} = 4 A V_{GS} = 0			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A T_j = 150°C di/dt = 100 A/μs		800		ns
Q_{rr}	Reverse recoved charge			4.6		μC

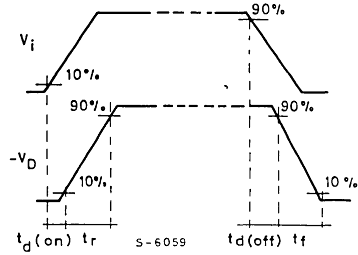
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP368 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ≤ 100 µs
Duty cycle ≤ 2%
$V_i = 10V$

SEF440
SEF441
SEF442
SEF443

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

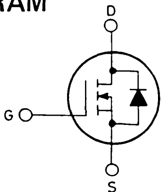
V_{DSS}	$R_{DS\ (ON)}$	I_D
500V/450V	0.85 Ω	8A
500V/450V	1.10 Ω	7A

ABSOLUTE MAXIMUM RATINGS

		SEF440	SEF441	SEF442	SEF443
V_{DS}	Drain-source voltage (V_{GS} = 0)	500V	450V	500V	450V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500V	450V	500V	450V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	8A	8A	7A	7A
	at T_{case} = 100°C	5A	5A	4A	4A
I_{DM}(•)	Drain current (pulsed)	32A	32A	28A	28A
I_{DLM}(•)	Drain inductive current, clamped	32A	32A	28A	28A
P_{tot}	Total power dissipation at T_{case} = 25°C	125W			
	Derating factor	1W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

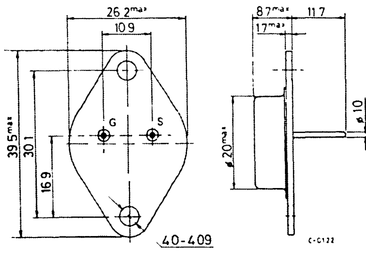
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1 °C/W
T_L	Maximum lead temperature for soldering purpose		300 °C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SEF440/SEF442** for **SEF441/SEF443**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25 °C V_{DS} = Max. Rating X0.8 T_{case} = 125 °C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X $R_{DS\ (on)\ max}$ V_{GS} = 10 V for **SEF440/SEF441** for **SEF442/SEF443**	 8 7			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4 A for **SEF440/SEF441** for **SEF442/SEF443**		 0.75 0.75	 0.85 1.10	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X $R_{DS\ (on)\ max}$ I_D = 4 A	4	7.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600 230 140	1900 280 170	pF pF pF

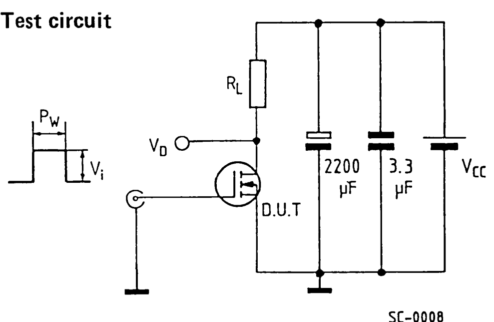
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 200 V I_D = 4 A		35		ns
t_r	Rise time	R_l = 4.7 Ω		15		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		90		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF440/SEF441**			8	A
		for **SEF442/SEF443**			7	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF440/SEF441**			32	A
		for **SEF442/SEF443**			28	A
V_{SD}	Forward on voltage	for **SEF440/SEF441** I_{SD} = 8 A V_{GS} = 0			2	V
		for **SEF442/SEF443** I_{SD}=7 A V_{GS} = 0			1.9	V
t_{rr}	Reverse recov. time	I_{SD} = 8 A T_j = 150°C di/dt = 100 A/μs		1100		ns
Q_{rr}	Reverse recovered charge			6.4		μC

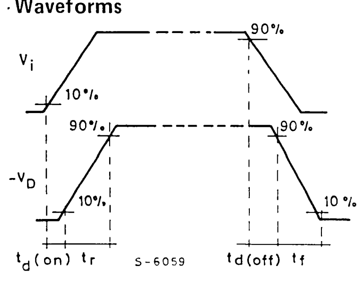
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP578 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

SEF510
SEF511
SEF512
SEF513

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

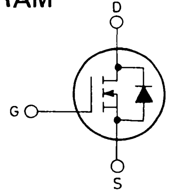
V_{DSS}	$R_{DS\ (ON)}$	I_D
100V/60V	0.6 Ω	4 A
100V/60V	0.8 Ω	3.5A

ABSOLUTE MAXIMUM RATINGS

		SEF510	SEF511	SEF512	SEF513
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	4A	4A	3.5A	3.5A
	at T_{case} = 100°C	2.5A	2.5A	2A	2A
I_{DM}(•)	Drain current (pulsed)	16A	16A	14A	14A
I_{DLM}(•)	Drain inductive current, clamped	16A	16A	14A	14A
P_{tot}	Total power dissipation at T_{case} = 25°C	20W			
	Derating factor	0.16W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

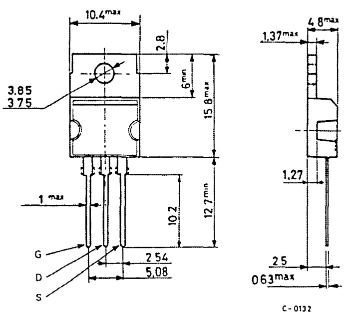
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	6.4°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF510/SEF512** for **SEF511/SEF513**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF510/SEF511** for **SEF512/SEF513**	 4 3.5			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2 A for **SEF510/SEF511** for **SEF512/SEF513**			 0.6 0.8	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 2 A	1	2.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		180 60 30	250 100 40	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		20		ns
t_r	Rise time	I_D = 2A		25		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_l = 50 Ω		25		ns
t_f	Fall time	(see test circuit)		20		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF510/SEF511**			4	A
		for **SEF512/SEF513**			3.5	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF510/SEF511**			16	A
		for **SEF512/SEF513**			14	A
V_{SD}	Forward on voltage	for **SEF510/SEF511** I_{SD} = 4 A V_{GS} = 0			2.5	V
		for **SEF512/SEF513** I_{SD}=3.5 A V_{GS} = 0			2	V
t_{rr}	Reverse recov. time	I_{SD} = 4 A T_j = 150°C di/dt = 100 A/μs		230		ns
Q_{rr}	Reverse recovered charge			1.4		μC

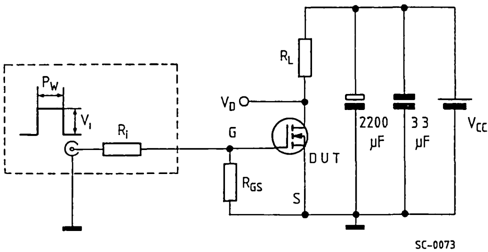
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

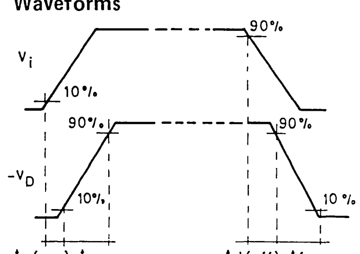
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP351 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ≤ 100 µs
Duty cycle ≤ 2%
$V_i = 10V$

SEF520
SEF521
SEF522
SEF523

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

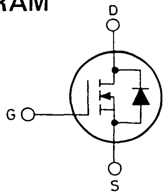
V_{DSS}	$R_{DS\ (ON)}$	I_D
100V/60V	0.3 Ω	8A
100V/60V	0.4 Ω	7A

ABSOLUTE MAXIMUM RATINGS

		SEF520	SEF521	SEF522	SEF523
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	8A	8A	7A	7A
	at T_{case} = 100°C	5A	5A	4A	4A
I_{DM}(•)	Drain current (pulsed)	32A	32A	28A	28A
I_{DLM}(•)	Drain inductive current, clamped	32A	32A	28A	28A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

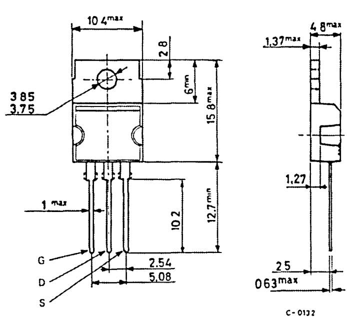
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



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THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF520/SEF522** for **SEF521/SEF523**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF520/SEF521** for **SEF522/SEF523**	 8 7			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4 A for **SEF520/SEF521** for **SEF522/SEF523**		 0.2 0.2	 0.3 0.4	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 4 A	1.5	3.7		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		375 180 90	480 230 110	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 0.5\ V_{(BR)\ DSS}$			40	ns
t_r	Rise time	$I_D = 4\ A$			70	ns
$t_{d\ (off)}$	Turn-off delay time	$R_{GS} = 50\ \Omega$ $R_l = 50\ \Omega$			100	ns
t_f	Fall time	(see test circuit)			70	ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF520/SEF521**			8	A
		for **SEF522/SEF523**			7	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF520/SEF521**			32	A
		for **SEF522/SEF523**			28	A
V_{SD}	Forward on voltage	for **SEF520/SEF521** $I_D = 7\ A$ $V_{GS} = 0$			2.5	V
		for **SEF522/SEF523** $I_D = 8\ A$ $V_{GS} = 0$			2.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 8\ A$ $T_j = 150°C$ di/dt = 100 A/μs		280		ns
Q_{rr}	Reverse recovered charge			1.6		μC

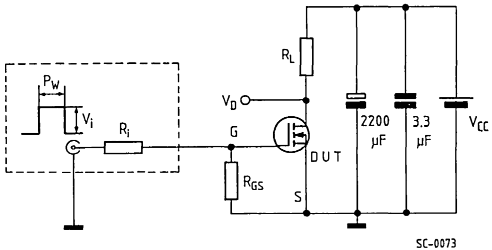
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP311 Datasheet.

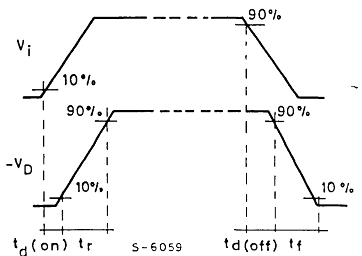
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEF530
SEF531
SEF532
SEF533

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

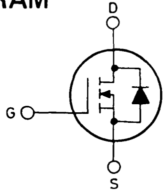
V_{DSS}	$R_{DS\ (ON)}$	I_D
100V/60V	0.18 Ω	14A
100V/60V	0.25 Ω	12A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	SEF530	SEF531	SEF532	SEF533
V_{DS}	Drain-source voltage (V_{GS} = 0)	100V	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100V	60V	100V	60V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	14A	14A	12A	12A
	at T_{case} = 100°C	9A	9A	8A	8A
I_{DM}(•)	Drain current (pulsed)	56A	56A	48A	48A
I_{DLM}(•)	Drain inductive current, clamped	56A	56A	48A	48A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6/W°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

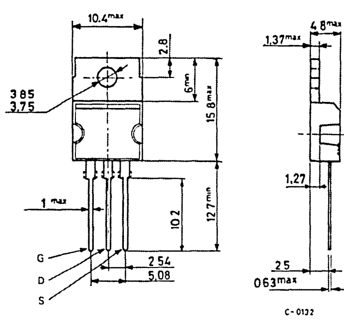
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF530/SEF532** for **SEF531/SEF533**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF530/SEF531** for **SEF532/SEF533**	 14 12			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 8 A for **SEF530/SEF531** for **SEF532/SEF533**		 0.085 0.085	 0.18 0.25	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 8 A	4	8.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950 180 370	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 36 V I_D = 8 A		30		ns
t_r	Rise time	R_{GS} = 15 Ω R_i = 15 Ω		75		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		40		ns
t_f	Fall time			45		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF530/SEF531**			14	A
		for **SEF532/SEF533**			12	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF530/SEF531**			56	A
		for **SEF532/SEF533**			48	A
V_{SD}	Forward on voltage	for **SEF530/SEF531** I_{SD} = 14 A V_{GS} = 0			2.5	V
		for **SEF532/SEF533** I_{SD} = 12 A V_{GS} = 0			2.3	V
t_{rr}	Reverse recovery time	I_{SD} = 14 A T_j = 150°C di/dt = 100 A/μs		360		ns
Q_{rr}	Reverse recovered charge			2.1		μC

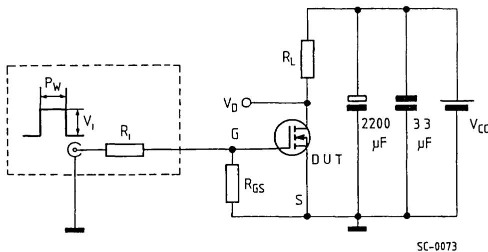
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

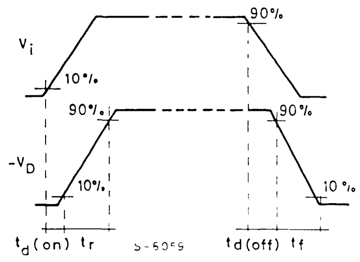
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP361 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
V_i = 10V

SEF541
SEF542
SEF543

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

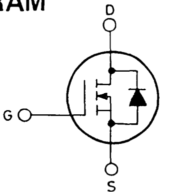
V_{DSS}	$R_{DS\ (ON)}$	I_D
60V	0.085 Ω	27A
100V/60V	0.11 Ω	24A

ABSOLUTE MAXIMUM RATINGS

		SEF541	SEF542	SEF543
V_{DS}	Drain-source voltage (V_{GS} = 0)	60V	100V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	60V	100V	60V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C	27A	24A	24A
	at T_{case} = 100°C	17A	15A	15A
I_{DM}(•)	Drain current (pulsed)	108A	96A	96A
I_{DLM}(•)	Drain inductive current, clamped	108A	96A	96A
P_{tot}	Total power dissipation at T_{case} = 25°C		125W	
	Derating factor		1W/°C	
T_{stg}	Storage temperature		-55 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

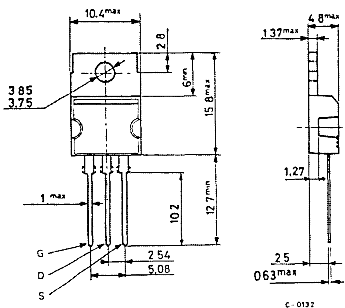
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



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SEF541
SEF542
SEF543

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF542** for **SEF541/SEF543**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF541** for **SEF542/SEF543**	 27 24			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 15 A for **SEF541** for **SEF542/SEF543**		 42 87	 85 110	 mΩ mΩ
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 15 A	6	8.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1100 600 300	1400 800 400	pF pF pF

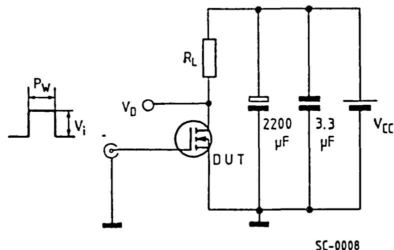
ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 30 V I_D = 15 A		30		ns
t_r	Rise time	R_i = 4.7 Ω		60		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		80		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF541**			27	A
		for **SEF542/SEF543**			24	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF541**			108	A
		for **SEF542/SEF543**			96	A
V_{SD}	Forward on voltage	for **SEF541** I_{SD} = 27 A V_{GS} = 0			2.5	V
		for **SEF542/SEF543** I_{SD} = 24 A V_{GS} = 0			2.3	V
t_{rr}	Reverse recovery time	I_{SD} = 27 A T_j = 150°C di/dt = 100 A/μs		500		ns
Q_{rr}	Reverse recovered charge			2.9		μC

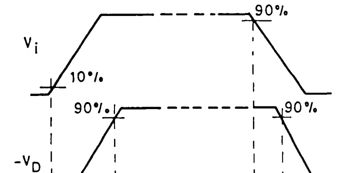
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%
(•) Pulse width limited by safe operating area.
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see:
for SEF541, SGSP381 Datasheet.
for SEF542/SEF543, SGSP361 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width $\leqslant 100\ \mu s$
Duty cycle $\leqslant 2\%$
$V_i = 10V$

SEF620
SEF621
SEF622
SEF623

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

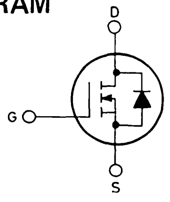
V_{DSS}	R_{DS}	I_D
200V/150V	0.8 Ω	5A
200V/150V	1.2 Ω	4A

ABSOLUTE MAXIMUM RATINGS

		SEF620	SEF621	SEF622	SEF623
V_{DS}	Drain-source voltage (V_{GS} = 0)	200V	150V	200V	150V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	200V	150V	200V	150V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	5A	5A	4A	4A
	at T_{case} = 100°C	3A	3A	2.5A	2.5A
I_{DM}(•)	Drain current (pulsed)	20A	20A	16A	16A
I_{DLM}(•)	Drain inductive current, clamped	20A	20A	16A	16A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

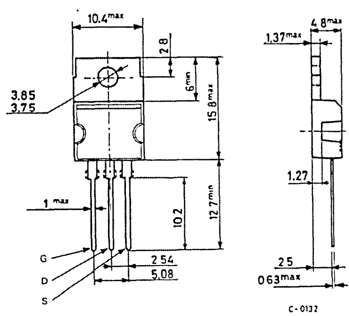
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

9/85

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF620/SEF622** for **SEF621/SEF623**	 200 150			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF620/SEF621** for **SEF622/SEF623**	 5 4			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **SEF620/SEF621** for **SEF622/SEF623**		 0.43 0.43	 0.8 1.2	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 2.5 A	1.3	3		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		380 100 50	500 130 65	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$			40	ns
t_r	Rise time	I_D = 2.5 A			60	ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω			100	ns
t_f	Fall time	(see test circuit)			60	ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF620/SEF621**			5	A
		for **SEF622/SEF623**			4	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF620/SEF621**			20	A
		for **SEF622/SEF623**			16	A
V_{SD}	Forward on voltage	for **SEF620/SEF621** I_{SD} = 5 A V_{GS} = 0			2	V
		for **SEF622/SEF623** I_{SD} = 4 A V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A T_j = 150°C di/dt = 100 A/μs		350		ns
Q_{rr}	Reverse recoved charge			2.3		μC

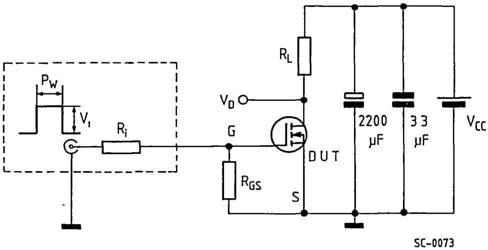
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

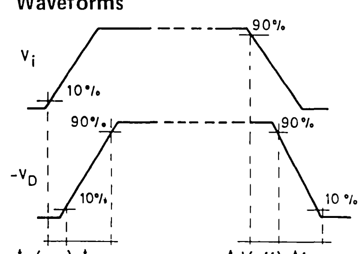
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP317 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

SEF630
SEF631
SEF632
SEF633

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

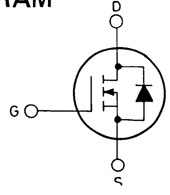
V_{DSS}	$R_{DS\ (ON)}$	I_D
200V/150V	0.4 Ω	9A
200V/150V	0.6 Ω	8A

ABSOLUTE MAXIMUM RATINGS

		SEF630	SEF631	SEF632	SEF633
V_{DS}	Drain-source voltage (V_{GS} = 0)	200V	150V	200V	150V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	200V	150V	200V	150V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	9A	9A	8A	8A
	at T_{case} = 100°C	6A	6A	5A	5A
I_{DM}(•)	Drain current (pulsed)	36A	36A	32A	32A
I_{DLM}(•)	Drain inductive current, clamped	36A	36A	32A	32A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

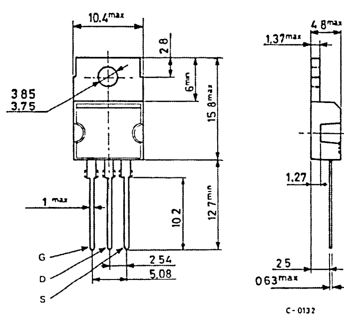
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF630/SEF632** for **SEF631/SEF633**	 200 150			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X $R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF630/SEF631** for **SEF632/SEF633**	 9 8			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5 A for **SEF630/SEF631** for **SEF632/SEF633**		 0.25 0.25	 0.4 0.6	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X $R_{DS\ (on)\ max}$ I_D = 5 A	3			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		980 200 80	1200 260 100	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 90 V I_D = 5 A		30		ns
t_r	Rise time	R_{GS} = 15 Ω R_l = 15 Ω		50		ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		50		ns
t_f	Fall time			40		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF630/SEF631**			9	A
		for **SEF632/SEF633**			8	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF630/SEF631**			36	A
		for **SEF632/SEF633**			32	A
V_{SD}	Forward on voltage	for **SEF630/SEF631** I_{SD} = 9 A V_{GS} = 0			2	V
		for **SEF632/SEF633** I_{SD}= 8 A V_{GS} = 0			1.8	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A T_j = 150°C di/dt = 100 A/μs		450		ns
Q_{rr}	Reverse recoved charge			3		μC

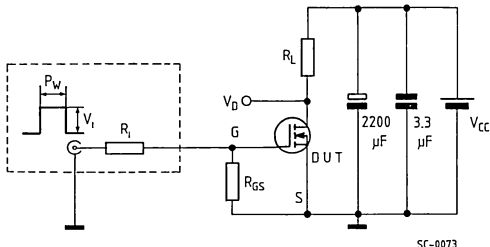
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

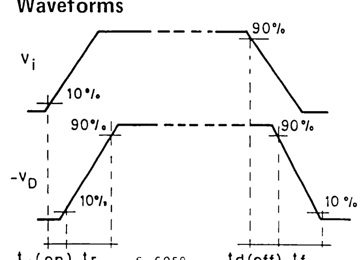
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP574 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ≤ 100 µs
Duty cycle ≤ 2%
V_i = 10V

N-CHANNEL POWER MOS TRANSISTORS

SEF710
SEF711
SEF712
SEF713

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

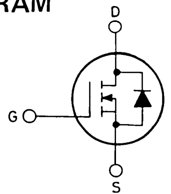
V_{DSS}	$R_{DS\,(ON)}$	I_D
400V/350V	3.6 Ω	1.5A
400V/350V	5 Ω	1.3A

ABSOLUTE MAXIMUM RATINGS

		SEF710	SEF711	SEF712	SEF713
V_{DS}	Drain-source voltage (V_{GS} = 0)	400V	350V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	400V	350V	400V	350V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	1.5A	1.5A	1.3A	1.3A
	at T_{case} = 100°C	1A	1A	0.8A	0.8A
I_{DM}(•)	Drain current (pulsed)	6A	6A	5A	5A
I_{DLM} (•)	Drain inductive current, clamped	6A	6A	5A	5A
P_{tot}	Total power dissipation at T_{case} = 25°C	20W			
	Derating factor	0.16W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

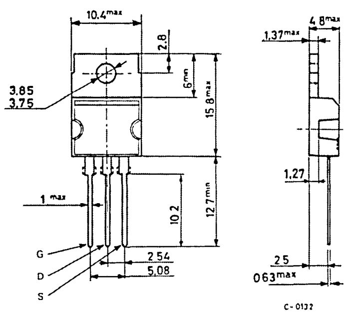
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	6.4°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 V for **SEF710/SEF712** for **SEF711/SEF713**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF710/SEF711** for **SEF712/SEF713**	 1.5 1.3			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 0.8 A for **SEF710/SEF711** for **SEF712/SEF713**		 2.1 2.1	 3.6 5	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 0.8 A	0.5	1.25		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{DS} = 0 V		340 60 30	450 95 50	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

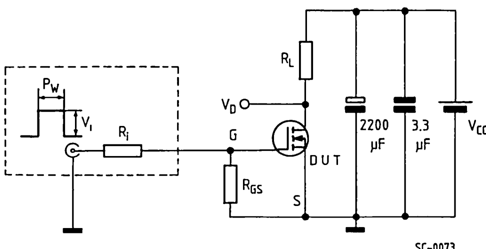
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)\ DSS}$		10		ns
t_r	Rise time	I_D = 0.8 A		20		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_l = 50 Ω		10		ns
t_f	Fall time	(see test circuit)		15		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF710/SEF711**			1.5	A
		for **SEF712/SEF713**			1.3	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF710/SEF711**			6	A
		for **SEF712/SEF713**			5	A
V_{SD}	Forward on voltage	for **SEF710/SEF711** I_{SD} = 1.5 A V_{GS} = 0			1.6	V
		for **SEF712/SEF713** I_{SD} = 1.3 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recov. time	I_{SD} = 1.5 A T_j = 150°C di/dt = 100 A/μs		380		ns
Q_{rr}	Reverse recovered charge			2.7		μC

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%
(•) Pulse width limited by safe operating area.

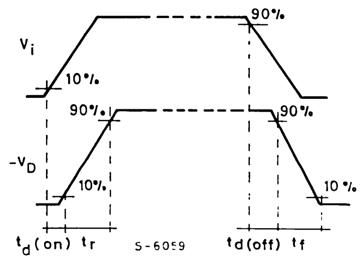
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP331 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
$V_i = 10V$

SEF720
SEF721
SEF722
SEF723

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

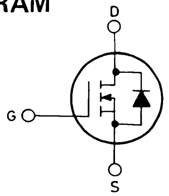
V_{DSS}	$R_{DS\,(ON)}$	I_D
400V/350V	1.8 Ω	3 A
400V/350V	2.5 Ω	2.5A

ABSOLUTE MAXIMUM RATINGS

		SEF720	SEF721	SEF722	SEF723
V_{DS}	Drain-source voltage (V_{GS} = 0)	400V	350V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	400V	350V	400V	350V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	3A	3A	2.5A	2.5A
	at T_{case} = 100°C	2A	2A	1.5A	1.5A
I_{DM}(•)	Drain current (pulsed)	12A	12A	10A	10A
I_{DLM}(•)	Drain inductive current, clamped	12A	12A	10A	10A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

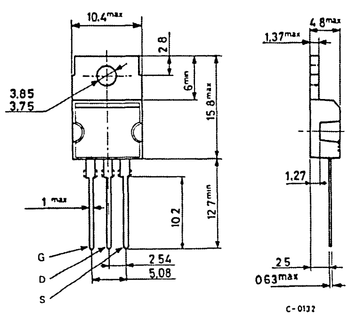
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

SEF720
SEF721
SEF722
SEF723

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF720/SEF722** for **SEF721/SEF723**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250μ A	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF720/SEF721** for **SEF722/SEF723**	 3 2.5			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.5 A for **SEF720/SEF721** for **SEF722/SEF723**		 0.7 0.7	 1.8 2.5	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 1.5 A	1	5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 100	1000 200 130	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		40		ns
t_r	Rise time	I_D = 1.5 A		50		ns
$t_{d\,(off)}$	Turn-off delay time	R_{GS} = 50Ω R_l = 50Ω		100		ns
t_f	Fall time	(see test circuit)		50		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF720/SEF721**			3	A
		for **SEF722/SEF723**			2.5	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF720/SEF721**			12	A
		for **SEF722/SEF723**			10	A
V_{SD}	Forward on voltage	for **SEF720/SEF721** I_D = 3 A V_{GS} = 0			1.6	V
		for **SEF722/SEF723** I_D = 2.5 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 3 A di/dt = 100 A/µs T_j = 150°C		450		ns
Q_{rr}	Reverse recovered charge			3.1		µC

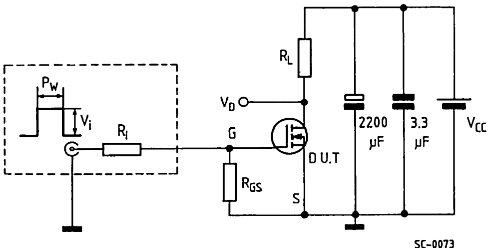
* Pulsed: pulse duration ≤ 300µs, duty cycle ≤ 2%

(•) Pulse width limited by safe operating area.

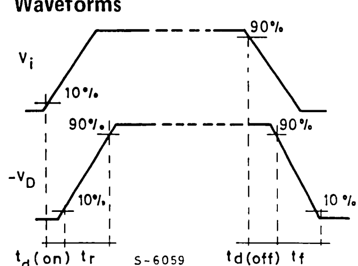
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP364 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%
V_i = 10V

N-CHANNEL POWER MOS TRANSISTORS

SEF730
SEF731
SEF732
SEF733

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

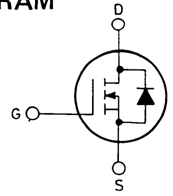
V_{DSS}	$R_{DS\ (ON)}$	I_D
400V/350V	1 Ω	5.5A
400V/350V	1.5 Ω	4.5A

ABSOLUTE MAXIMUM RATINGS

		SEF730	SEF731	SEF732	SEF733
V_{DS}	Drain-source voltage (V_{GS} = 0)	400V	350V	400V	350V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	400V	350V	400V	350V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	5.5A	5.5A	4.5A	4.5A
	at T_{case} = 100°C	3.5A	3.5A	3A	3A
I_{DM}(•)	Drain current (pulsed)	22A	22A	18A	18A
I_{DLM}(•)	Drain inductive current, clamped	22A	22A	18A	18A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

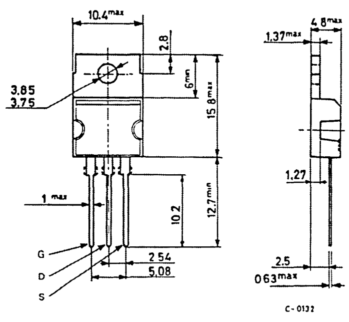
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF730/SEF732** for **SEF731/SEF733**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF730/SEF731** for **SEF732/SEF733**	 5.5 4.5			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3 A for **SEF730/SEF731** for **SEF732/SEF733**		 0.7 0.7	 1 1.5	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 3 A	3	5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 100	1000 200 130	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		30		ns
t_r	Rise time	I_D = 3 A		35		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 15 Ω R_l = 15 Ω		55		ns
t_f	Fall time	(see test circuit)		35		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF730/SEF731**			5.5	A
		for **SEF732/SEF733**			4.5	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF730/SEF731**			22	A
		for **SEF732/SEF733**			18	A
V_{SD}	Forward on voltage	for **SEF730/SEF731** I_D = 5.5 A V_{GS} = 0			1.6	V
		for **SEF732/SEF733** I_D = 4.5 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 5.5 A di/dt = 100 A/μs T_j = 150°C		600		ns
Q_{rr}	Reverse recovered charge			4		μC

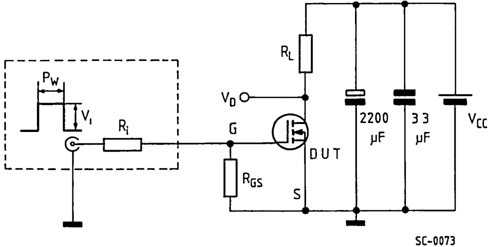
* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

(•) Pulse width limited by safe operating area.

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP364 Datasheet.

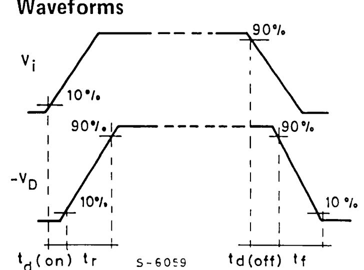
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10V$

Waveforms



SEF820
SEF821
SEF822
SEF823

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

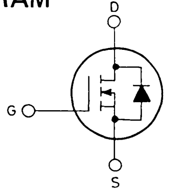
V_{DSS}	$R_{DS\ (ON)}$	I_D
500V/450V	3 Ω	2.5A
500V/450V	4 Ω	2 A

ABSOLUTE MAXIMUM RATINGS

		SEF820	SEF821	SEF822	SEF823
V_{DS}	Drain-source voltage (V_{GS} = 0)	500V	450V	500V	450V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500V	450V	500V	450V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	2.5A	2.5A	2A	2A
	at T_{case} = 100°C	1.5A	1.5A	1A	1A
I_{DM}(•)	Drain current (pulsed)	10A	10A	8A	8A
I_{DLM}(•)	Drain inductive current, clamped	10A	10A	8A	8A
P_{tot}	Total power dissipation at T_{case} = 25°C	40W			
	Derating factor	0.32W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

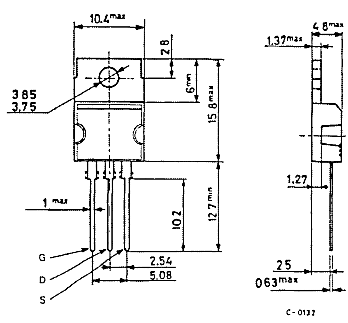
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	3.12°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF820/SEF822** for **SEF821/SEF823**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF820/SEF821** for **SEF822/SEF823**	 2.5 2			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A for **SEF820/SEF821** for **SEF822/SEF823**		 1.33 1.33	 3 4	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 1 A	1	3.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 80	1000 190 100	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 0.5 $V_{(BR)DSS}$		60		ns
t_r	Rise time	I_D = 1 A		50		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_l = 50 Ω		60		ns
t_f	Fall time	(see test circuit)		30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF820/SEF821**			2.5	A
		for **SEF822/SEF823**			2	A
I_{SDM}(•)	Source drain current* (pulsed)	for **SEF820/SEF821**			10	A
		for **SEF822/SEF823**			8	A
V_{SD}	Forward on voltage	for **SEF820/SEF821** I_{SD} = 2.5 A V_{GS} = 0			1.6	V
		for **SEF822/SEF823** I_{SD} = 2 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A T_j = 150°C di/dt = 100 A/μs		600		ns
Q_{rr}	Reverse recovered charge			3.5		μC

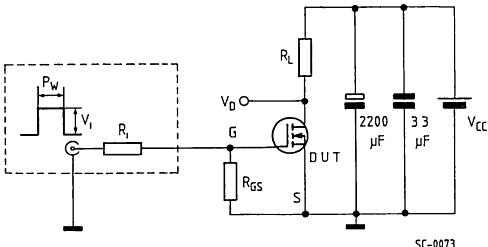
* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

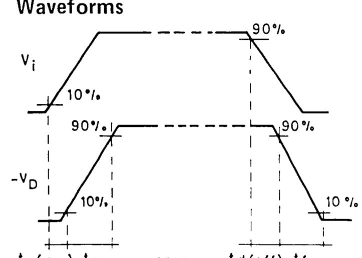
For typical curves, and switching times resistive load, clamping inductive load, gate charge, body drain diode trr measurament test circuits see SGSP368 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

SEF830
SEF831
SEF832
SEF833

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

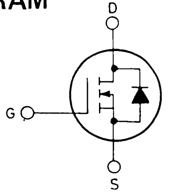
V_{DSS}	$R_{DS\ (ON)}$	I_D
500V/450V	**1.5 Ω**	**4.5A**
500V/450V	**2 Ω**	**4 A**

ABSOLUTE MAXIMUM RATINGS

		SEF830	SEF831	SEF832	SEF833
V_{DS}	Drain-source voltage (V_{GS} = 0)	500V	450V	500V	450V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500V	450V	500V	450V
V_{GS}	Gate-source voltage	±20V			
I_D	Drain current (continuous) T_{case} = 25°C	4.5A	4.5A	4A	4A
	at T_{case} = 100°C	3A	3A	2.5A	2.5A
I_{DM}(•)	Drain current (pulsed)	18A	18A	16A	16A
I_{DLM}(•)	Drain inductive current, clamped	18A	18A	16A	16A
P_{tot}	Total power dissipation at T_{case} = 25°C	75W			
	Derating factor	0.6W/°C			
T_{stg}	Storage temperature	-55 to 150°C			
T_j	Max. operating junction temperature	150°C			

(•) Pulse width limited by safe operating area

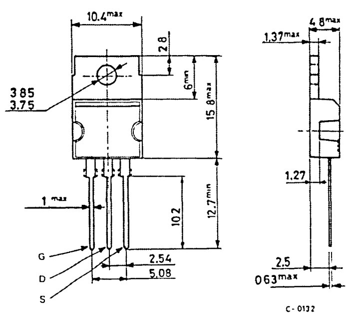
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		300°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250μA V_{GS} = 0 for **SEF830/SEF832** for **SEF831/SEF833**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max. Rating T_{case} = 25°C V_{DS} = Max. Rating X0.8 T_{case} = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			100	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ V_{GS} = 10V for **SEF830/SEF831** for **SEF832/SEF833**	 4.5 4			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **SEF830/SEF831** for **SEF832/SEF833**		 1.33 1.33	 1.5 2	 Ω Ω
g_{fs}	Forward transconductance	V_{DS} > $I_{D\ (on)}$ X$R_{DS\ (on)\ max}$ I_D = 2.5 A	2.5	3.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780 150 80	1000 190 100	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 225V I_D = 2.5A		30		ns
t_r	Rise time	R_{GS} = 15Ω R_i = 15Ω		30		ns
$t_{d\ (off)}$	Turn-off delay time	(sse test circuit)		55		ns
t_f	Fall time			30		ns
SOURCE DRAIN DIODE						
I_{SD}	Source drain current	for **SEF830/SEF831**			4.5	A
		for **SEF832/SEF833**			4	A
I_{SDM}(•)	Source drain current (pulsed)	for **SEF830/SEF831**			18	A
		for **SEF832/SEF833**			16	A
V_{SD}	Forward on voltage	for **SEF830/SEF831** I_{SD} = 4.5 A V_{GS} = 0			1.6	V
		for **SEF832/SEF833** I_{SD} = 4 A V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A T_j = 150°C di/dt = 100 A/μs		800		ns
Q_{rr}	Reverse recoved charge			4.6		μC

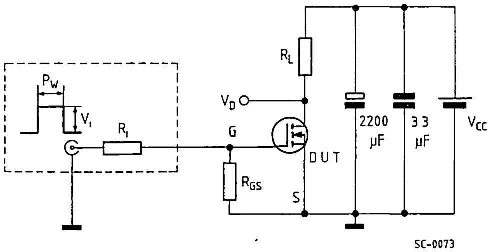
* Pulsed: pulse duration ⩽ 300μs, dutv cycle ⩽ 2%

(•) Pulse width limited by safe operating area.

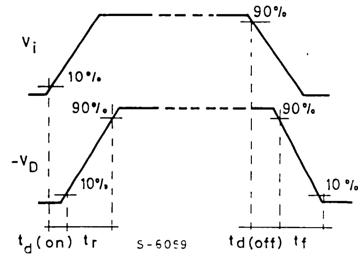
For typical curves, and switching times resistive load, clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP368 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ≤ 100 µs
Duty cycle ≤ 2%
V_i = 10V

SEFH6N55
SEFH7N50
SEFM6N55
SEFM7N50

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

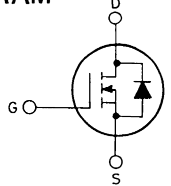
V_{DSS}	$R_{DS\ (ON)}$	I_D
500 V	0.8 Ω	7 A
550 V	1.2 Ω	6 A

ABSOLUTE MAXIMUM RATINGS

		SEFH or SEFM 6N55	SEFH or SEFM 7N50
V_{DS}	Drain-source voltage (V_{GS} = 0)	550V	500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	550V	500V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	6A	7A
I_{DM}(•)	Drain current (pulsed)	30A	40A
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	150W	
	Derating factor	1.2W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

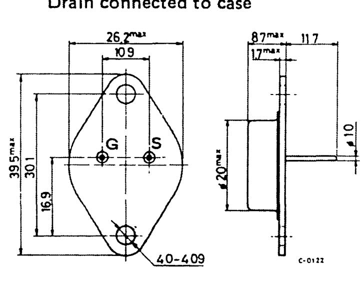
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

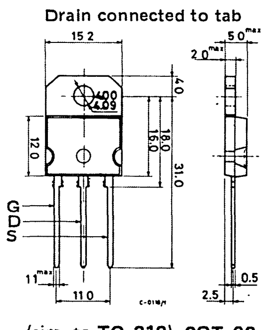
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFH6N55/SEFM6N55** for **SEFH7N50/SEFM7N50**	 550 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance (V_{GS} = 10V)	for **SEFH6N55/SEFH6N55** I_D = 3A for **SEFH7N50/SEFM7N50** I_D = 3.5 A			1.2 0.8	Ω Ω
$V_{DS(on)}$	Drain-source On-voltage (V_{GS} = 10V)	for**SEFH6N55/SEFM6N55** I_D = 6 A for **SEFH7N50/SEFM7N50** I_D = 7 A T_j = 100°C for **SEFH6N55/SEFM6N55** I_D = 3 A for **SEFH7N50/SEFM7N50** I_D =3.5 A			9 7 7.2 5.6	V V V V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
g_{fs}	Forward transconductance	for **SEFH6N55/SEFM6N55** V_{DS} = 15 V I_D = 3 A	2			mho
		for **SEFH7N50/SEFM7N50** V_{DS} = 10V I_D = 3.5 A	2			mho

DYNAMIC

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	1900	pF
C_{oss}	Output capacitance			230	280	pF
C_{rss}	Reverse transfer capacitance			140	170	pF

SWITCHING

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		60		ns
t_r	Rise time	I_D = 0.5 Rated I_D		150		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		200		ns
t_f	Fall time	(see test circuit)		120		ns

SOURCE DRAIN DIODE

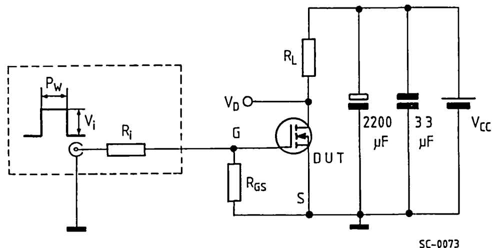
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.3		V
t_{on}	Forward Turn-on time			175		ns
t_{rr}	Reverse recovery time			600		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

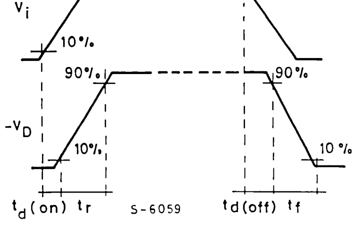
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP478 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10V$

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

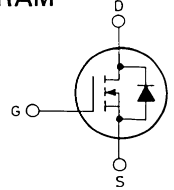
V_{DSS}	$R_{DS\ (ON)}$	I_D
350/400V	0.55 Ω	8 A
450V	0.8 Ω	7 A

ABSOLUTE MAXIMUM RATINGS

		SEFH or SEFM 7N45	SEFH or SEFM 8N35	SEFH or SEFM 8N40
V_{DS}	Drain-source voltage (V_{GS} = 0)	450V	350V	400V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ	450V	350V	400V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C	7A	8A	8A
I_{DM}(•)	Drain current (pulsed)	40A	48A	48A
I_{GM}	Gate current (pulsed)		1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C		150W	
	Derating factor		1.2W/°C	
T_{stg}	Storage temperature		-65 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

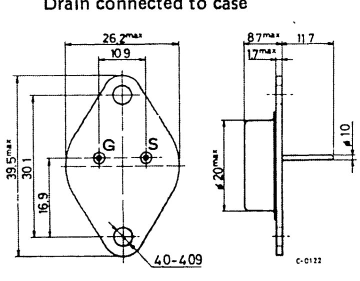
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

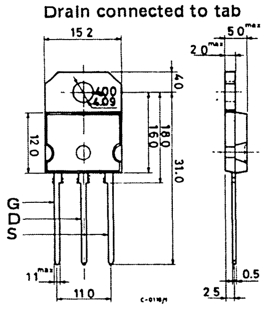
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to **TO-218**) **SOT-93**

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFH7N45/SEFM7N45** for **SEFH8N40/SEFM8N40** for **SEFH8N35/SEFM8N35**	 450 400 350			 V V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance (V_{GS} = 10V)	for **SEFH7N45/SEFM7N45** I_D = 3.5A for **SEFH8N40/SEFM8N40** I_D = 4 A for **SEFH8N35/SEFM8N35** I_D = 4A			0.80 0.55 0.55	Ω Ω Ω
$V_{DS(on)}$	Drain-source On-voltage (V_{GS} = 10V)	for **SEFH7N45/SEFM7N45** I_D = 7 A for **SEFH8N40/SEFM8N40** I_D = 8 A for **SEFH8N35/SEFM8N35** I_D = 8 A for **SEFH7N45/SEFM7N45** I_D = 3.5 A T_j = 100°C for **SEFH8N40/SEFM8N40** I_D = 4 A T_j = 100°C for **SEFH8N35/SEFM8N35** I_D = 4 A T_j = 100°C			7 5.3 5.3 5.6 4.4 4.4	V V V V V V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
g_{fs}	Forward transconductance (V_{DS} = 10V)	for **SEFH7N45/SEFM7N45** I_D = 3.5 A	2			mho
		for **SEFH8N40/SEFM8N40** I_D = 4 A	3			mho
		for **SEFH8N35/SEFM8N35** I_D = 4 A	3			mho

DYNAMIC

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	2100	pF
C_{oss}	Output capacitance			300	390	pF
C_{rss}	Reverse transfer capacitance			200	260	pF

SWITCHING

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		60		ns
t_r	Rise time	I_D = 0.5 Rated I_D		150		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		200		ns
t_f	Fall time	(see test circuit)		120		ns

SOURCE DRAIN DIODE

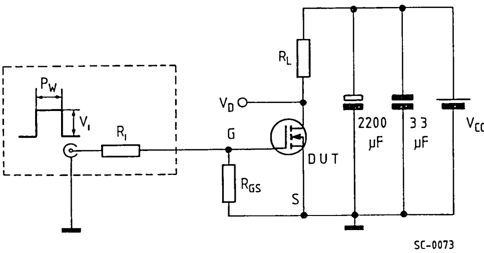
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.3		V
t_{on}	Forward Turn-on time			175		ns
t_{rr}	Reverse recovery time	V_{GS} = 0		600		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

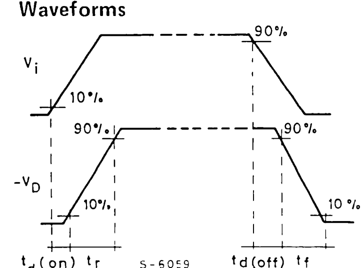
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP474 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%
V_i = 10V

SEFH15N18
SEFH15N20
SEFM15N18
SEFM15N20

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

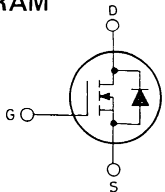
V_{DSS}	$R_{DS (ON)}$	I_D
180V/200V	0.16 Ω	15 A

ABSOLUTE MAXIMUM RATINGS

		SEFH or SEFM 15N18	SEFH or SEFM 15N20
V_{DS}	Drain-source voltage (V_{GS} = 0)	180V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	180V	200V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	15A	
I_{DM}(•)	Drain current (pulsed)	80A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	150W	
	Derating factor	1.2W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

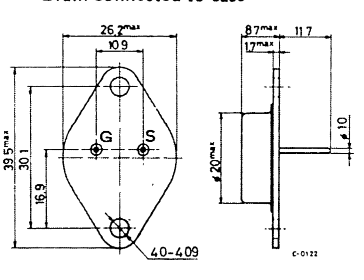
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

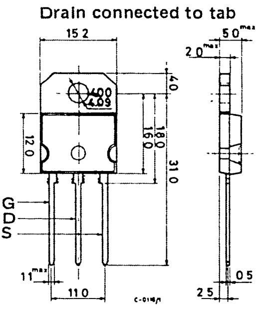
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFH15N18/SEFM15N18** for **SEFH15N20/SEFM15N20**	 180 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	µA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 7.5 A		0.11	0.16	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 15 A V_{GS} = 10V I_D = 7.5 A T_j = 100°C			3 2.4	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 7.5 A	4			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900 450 220	2200 550 260	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

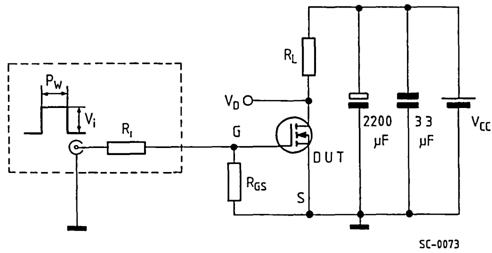
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		60		ns
t_r	Rise time	I_D = 0.5 Rated I_D		300		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		220		ns
t_f	Fall time	(see test circuit)		250		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = O		2		V
t_{on}	Forward Turn-on time			50		ns
t_{rr}	Reverse recovery time			450		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP473 Datasheet.

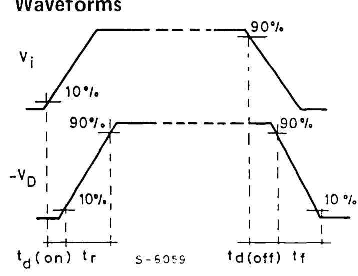
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEFH25N08
SEFH25N10
SEFM25N08
SEFM25N10

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	$R_{DS\,(ON)}$	I_D
80V/100V	0.075Ω	25 A

ABSOLUTE MAXIMUM RATINGS

		SEFH or SEFM 25N08	SEFH or SEFM 25N10
V_{DS}	Drain-source voltage (V_{GS} = 0)	80V	100V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	80V	100V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	25A	
I_{DM}(•)	Drain current (pulsed)	125A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	150W	
	Derating factor	1.2W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM

D

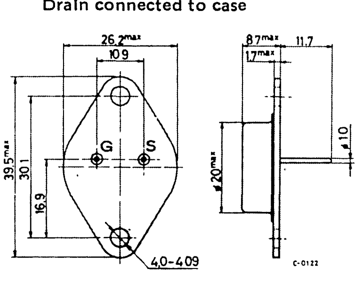
G

S

MECHANICAL DATA

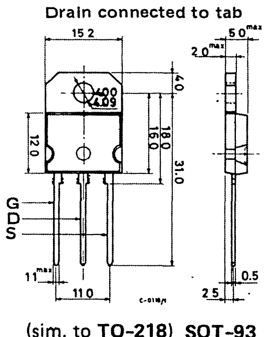
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to **TO-218**) **SOT-93**

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFH25N08/SEFM25N08** for **SEFH25N10/SEFM25N10**	 80 100			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 12.5 A		36	75	mΩ
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10 V I_D = 25 A V_{GS} = 10 V I_D = 12.5 A T_j = 100°C			2.25 1.8	V V
g_{fs}	Forward transconductance	V_{DS} = 10 V I_D = 12.5 A	5	12		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1800 650 300	2200 810 375	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

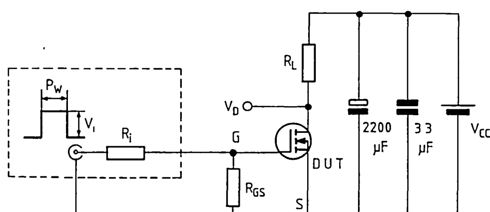
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V			60	ns
t_r	Rise time	I_D = 0.5 Rated I_D			450	ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω			150	ns
t_f	Fall time	(see test circuit)			300	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.5		V
t_{on}	Forward Turn-on time			50		ns
t_{rr}	Reverse recovery time			450		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP471 Datasheet.

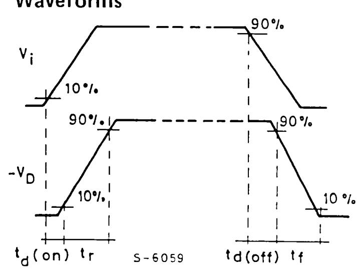
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEFH35N05
SEFH35N06
SEFM35N05
SEFM35N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

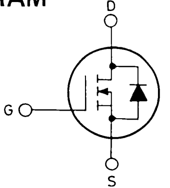
V_{DSS}	$R_{DS\ (ON)}$	I_D
50V/60V	0.055Ω	35 A

ABSOLUTE MAXIMUM RATINGS

		SEFH or SEFM 35N05	SEFH or SEFM 35N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	35A	
I_{DM}(•)	Drain current (pulsed)	150A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	150W	
	Derating factor	1.2W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

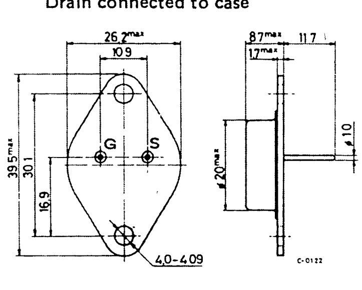
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

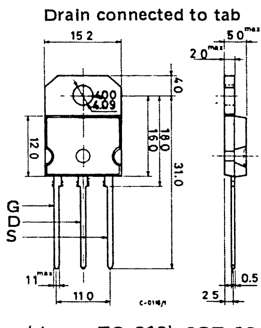
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to TO-218) SOT-93

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	0.83°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFH35N05/SEFM35N05** for **SEFH35N06/SEFM35N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 17.5 A		30	55	mΩ
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 35 A V_{GS} = 10V I_D = 17.5 A T_j = 100°C			2.3 1.9	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 17.5 A	8	15		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900 1200 600	2500 1600 800	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

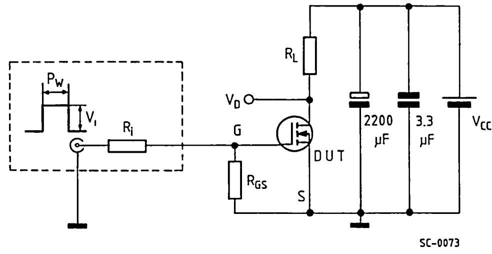
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		60		ns
t_r	Rise time	I_D = 0.5 Rated I_D		450		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		150		ns
t_f	Fall time	(see test circuit)		300		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.5		V
t_{on}	Forward Turn-on time			50		ns
t_{rr}	Reverse recovery time			450		ns

* Pulsed: pulse duration ≤ 300µs, duty cycle ≤ 2%

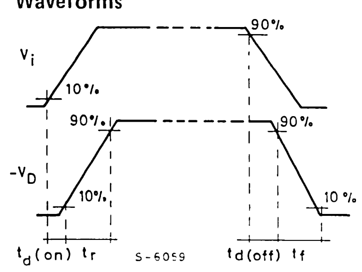
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP491 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ≤ 100 µs
Duty cycle ≤ 2%
V_i = 10V

SEFM2N45/SEFP2N45
SEFM3N35/SEFP3N35
SEFM3N40/SEFP3N40

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

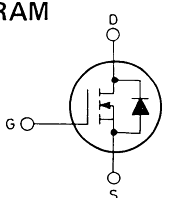
V_{DSS}	$R_{DS\ (ON)}$	I_D
350/400V	3.3 Ω	3 A
450V	4 Ω	2 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 2N45	SEFM or SEFP 3N35	SEFM or SEFP 3N40
V_{DS}	Drain-source voltage (V_{GS} = 0)	450V	350V	400V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	450V	350V	400V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C	2A	3A	3A
I_{DM}(•)	Drain current (pulsed)	7A	8A	8A
I_{GM}	Gate current (pulsed)		1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C		75W	
	Derating factor		0.6W/°C	
T_{stg}	Storage temperature		-65 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

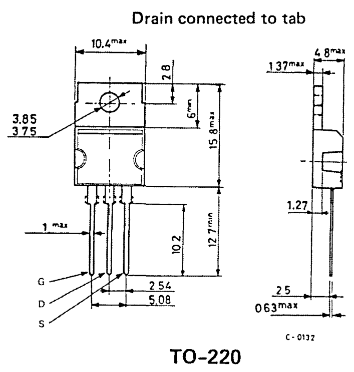
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

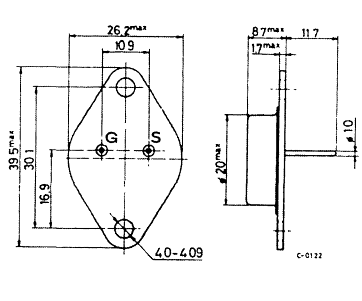
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM2N45/SEFP2N45** for **SEFM3N40/SEFP3N40** for **SEFM3N35/SEFP3N35**	 450 400 350			 V V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance (V_{GS} = 10V)	for **SEFM2N45/SEFP2N45** I_D = 1A for **SEFM3N40/SEFP3N40** I_D = 1.5 A for **SEFM3N35/SEFP3N35** I_D = 1.5A			4.0 3.3 3.3	Ω Ω Ω
$V_{DS(on)}$	Drain-source On-voltage (V_{GS} = 10V)	for**SEFM2N45/SEFP2N45** I_D = 2 A for **SEFM3N40/SEFP3N40** I_D = 3 A for SEFM3N35/SEFP3N35 I_D = 3 A for **SEFM2N45/SEFP2N45** I_D = 1 A T_j = 100°C for **SEFM3N40/SEFP3N40** I_D =1.5 A T_j = 100°C for **SEFM3N35/SEFP3N35** I_D = 1.5 A T_j = 100°C			10 12 12 8 10 10	V V V V V V

ELECTRICAL CHARACTERISTICS (continued)

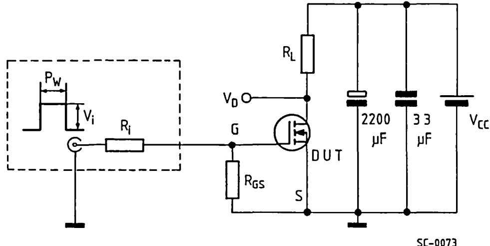
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
g_{fs}	Forward transconductance (V_{DS} = 15V)	for **SEFM2N45/SEFP2N45** I_D = 1A	1			mho
		for **SEFM3N40/SEFP3N40** I_D = 1.5 A	0.75			mho
		for **SEFM3N35/SEFP3N35** I_D = 1.5 A	0.75			mho
DYNAMIC						
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		340	450	pF
C_{oss}	Output capacitance			60	95	pF
C_{rss}	Reverse transfer capacitance			30	50	pF
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 125 V I_D = 0.5 Rated I_D R_{GS} = 50Ω R_i = 50Ω (see test circuit)			40	ns
t_r	Rise time				60	ns
$t_{d\ (off)}$	Turn-off delay time				60	ns
t_f	Fall time				30	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1		V
t_{on}	Forward Turn-on time			150		ns
t_{rr}	Reverse recovery time			200		ns

* Pulsed: pulse duration $\leqslant$ 300μs, duty cycle $\leqslant$ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP130 Datasheet.

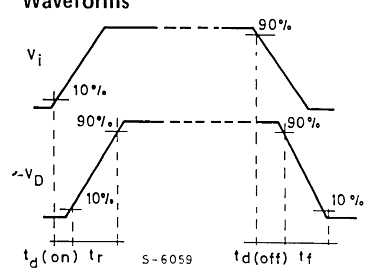
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

Waveforms



SEFM3N55
SEFM4N50
SEFP3N55
SEFP4N50

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

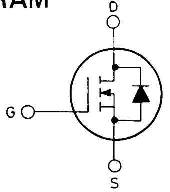
V_{DSS}	$R_{DS\ (ON)}$	I_D
500 V	**1.5 Ω**	**4 A**
550 V	**2.5 Ω**	**3 A**

ABSOLUTE MAXIMUM RATINGS

		SEFH or SEFM 3N55		SEFH or SEFM 4N50
V_{DS}	Drain-source voltage (V_{GS} = 0)	550V		500V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	550V		500V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C	3A		4A
I_{DM}(•)	Drain current (pulsed)		10A	
I_{GM}	Gate current (pulsed)		1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C		75W	
	Derating factor		0.6W/°C	
T_{stg}	Storage temperature		-65 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

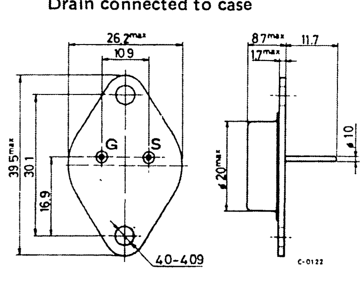
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

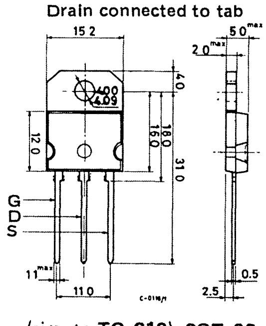
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to **TO-218**) **SOT-93**

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM3N55/SEFP3N55** for **SEFM4N50/SEFP4N50**	 550 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance (V_{GS} = 10V)	for **SEFM3N55/SEFP3N55** I_D = 1.5A for **SEFM4N50/SEFP4N50** I_D = 2 A		1.33 1.33	2.5 1.5	Ω Ω
$V_{DS(on)}$	Drain-source On-voltage (V_{GS} = 10V)	for**SEFM3N55/SEFP3N55** I_D = 3 A for **SEFM4N50/SEFP4N50** I_D = 4 A for **SEFM3N55/SEFP3N55** I_D = 1.5 A T_j = 100°C for **SEFM4N50/SEFP4N50** I_D =2 A T_j = 100°C			9 7.5 7.5 6	V V V V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
g_{fs}	Forward transconductance	for **SEFM3N55/SEFP3N55** V_{DS} = 15 V I_D = 1.5A	1.5			mho
		for **SEFM4N50/SEFP4N50** V_{DS} = 15 V I_D = 2 A	1.5			mho

DYNAMIC

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz		780	1000	pF
C_{oss}	Output capacitance	V_{GS} = 0		150	190	pF
C_{rss}	Reverse transfer capacitance			80	100	pF

SWITCHING

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		50		ns
t_r	Rise time	I_D = 0.5 Rated I_D		100		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		200		ns
t_f	Fall time	(see test circuit)		100		ns

SOURCE DRAIN DIODE

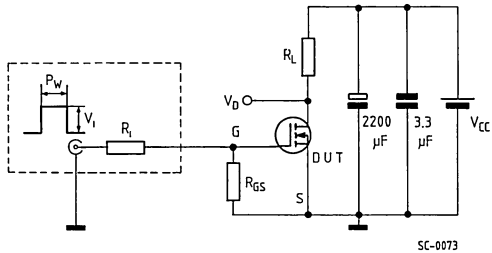
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.1		V
t_{on}	Forward Turn-on time			250		ns
t_{rr}	Reverse recovery time			420		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP368 Datasheet.

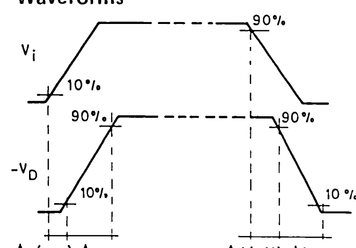
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEFM4N45/SEFP4N45
SEFM5N35/SEFP5N35
SEFM5N40/SEFP5N40

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

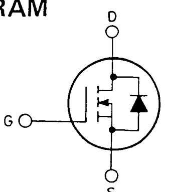
V_{DSS}	$R_{DS\ (ON)}$	I_D
350/400V	1 Ω	5 A
450V	1.5 Ω	4 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 4N45	SEFM or SEFP 5N35	SEFM or SEFP 5N40
V_{DS}	Drain-source voltage (V_{GS} = 0)	450V	350V	400V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	450V	350V	400V
V_{GS}	Gate-source voltage		±20V	
I_D	Drain current (continuous) T_{case} = 25°C	4A	5A	5A
I_{DM}(•)	Drain current (pulsed)	10A	12A	12A
I_{GM}	Gate current (pulsed)		1.5A	
P_{tot}	Total power dissipation at T_{case} < 25°C		75W	
	Derating factor		0.6W/°C	
T_{stg}	Storage temperature		-65 to 150°C	
T_j	Max. operating junction temperature		150°C	

(•) Pulse width limited by safe operating area

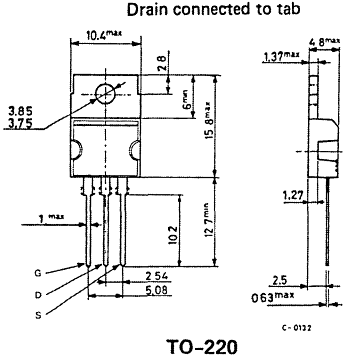
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

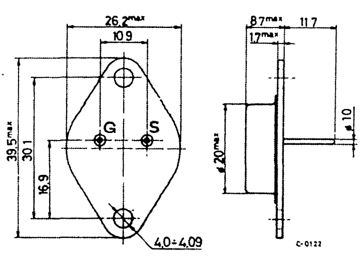
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM4N45/SEFP4N45** for **SEFM5N40/SEFP5N40** for **SEFM5N35/SEFP5N35**	 450 400 350			 V V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance (V_{GS} = 10V)	for **SEFM4N45/SEFP4N45** I_D = 2A for **SEFM5N40/SEFP5N40** I_D = 2.5 A for **SEFM5N35/SEFP5N35** I_D = 2.5 A			1.5 1 1	Ω Ω Ω
$V_{DS(on)}$	Drain-source On-voltage (V_{GS} = 10V)	for**SEFM4N45/SEFP4N45** I_D = 4 A for **SEFM5N40/SEFP5N40** I_D = 5 A for **SEFM5N35/SEFP5N35** I_D = 5 A for **SEFM4N45/SEFP4N45** I_D = 2 A T_j = 100°C for **SEFM5N40/SEFP5N40** I_D =2.5 A T_j = 100°C for **SEFM5N35/SEFP5N35** I_D = 2.5 A T_j = 100°C			7.5 6.2 6.2 6 5 5	V V V V V V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
g_{fs}	Forward transconductance (V_{DS} = 15V)	for **SEFM4N45/SEFP4N45** I_D = 2 A	1.5			mho
		for **SEFM5N40/SEFP5N40** I_D = 2.5 A	2.0			mho
		for **SEFM5N35/SEFP5N35** I_D = 2.5 A	2.0			mho

DYNAMIC

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
C_{iss}	Input capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780	1000	pF
C_{oss}	Output capacitance			150	200	pF
C_{rss}	Reverse transfer capacitance			100	130	pF

SWITCHING

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V I_D = 0.5 Rated I_D R_{GS} = 50 Ω R_i = 50 Ω (see test circuit)		50		ns
t_r	Rise time			100		ns
$t_{d\ (off)}$	Turn-off delay time			200		ns
t_f	Fall time			100		ns

SOURCE DRAIN DIODE

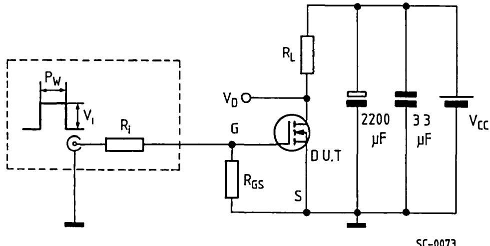
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.1		V
t_{on}	Forward Turn-on time			250		ns
t_{rr}	Reverse recovery time			420		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

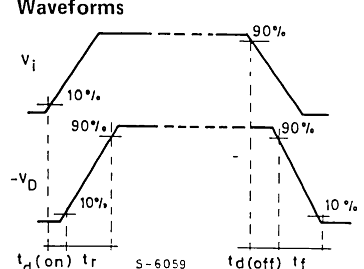
For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP364 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms



Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%
V_i = 10V

SEFM5N18
SEFM5N20
SEFP5N18
SEFP5N20

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

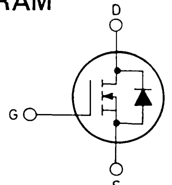
V_{DSS}	$R_{DS\ (ON)}$	I_D
180V/200V	1 Ω	5 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 5N18	SEFM or SEFP 5N20
V_{DS}	Drain-source voltage (V_{GS} = 0)	180V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	180V	200V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
I_{DM}(•)	Drain current (pulsed)	15A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

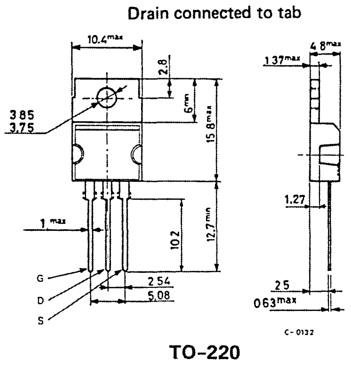
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

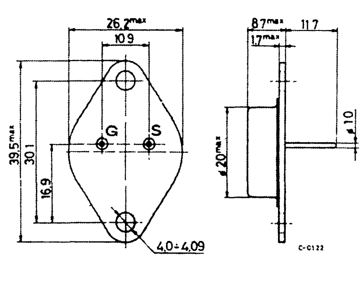
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM5N18/SEFP5N18** for **SEFM5N20/SEFP5N20**	 180 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 2.5 A		0.45	1	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10 V I_D = 5 A V_{GS} = 10V I_D = 2.5 A T_j = 100°C			6 5	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 2.5 A	1.5	3.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		380 100 50	500 130 65	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

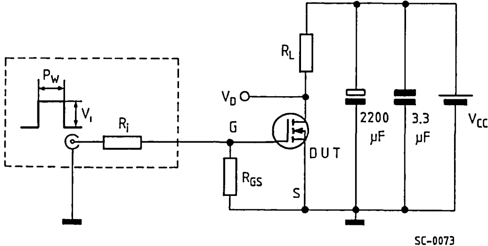
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 25$ V		20		ns
t_r	Rise time	$I_D = 0.5$ Rated I_D		150		ns
$t_{d\ (off)}$	Turn-off delay time	$R_{GS} = 50\ \Omega$ $R_i = 50\ \Omega$		50		ns
t_f	Fall time	(see test circuit)		50		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D $V_{GS} = 0$		2.0		V
t_{on}	Forward Turn-on time			200		ns
t_{rr}	Reverse recovery time			300		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP216 Datasheet.

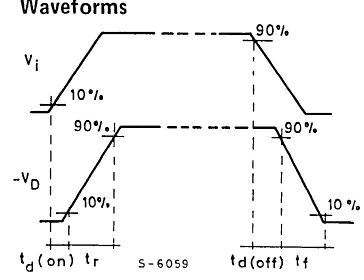
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10$V

Waveforms



SEFM8N08
SEFM8N10
SEFP8N08
SEFP8N10

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

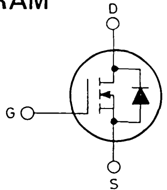
V_{DSS}	$R_{DS\ (ON)}$	I_D
80V/100V	0.5 Ω	8 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 8N08	SEFM or SEFP 8N10
V_{DS}	Drain-source voltage (V_{GS} = 0)	80V	100V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	80V	100V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	8A	
I_{DM}(•)	Drain current (pulsed)	20A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

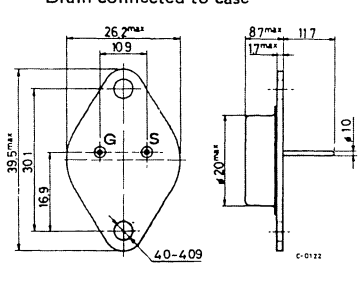
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

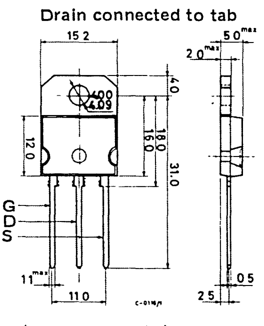
Dimension in mm

Drain connected to case



TO-3

Drain connected to tab



(sim. to **TO-218**) **SOT-93**

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM8N08/SEFP8N08** for **SEFM8N10/SEFP8N10**	 80 100			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 4 A		0.2	0.5	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 8 A V_{GS} = 10V I_D = 4 A T_j = 100°C			4.8 4	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 4 A	1.5	4		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		375	480 230 110	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

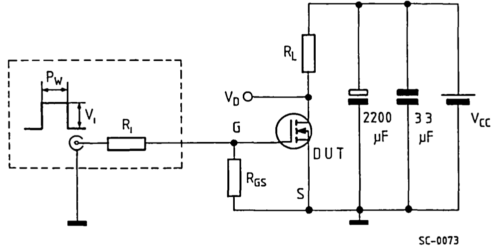
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		50		ns
t_r	Rise time	I_D = 0.5 Rated I_D		120		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		50		ns
t_f	Fall time	(see test circuit)		60		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.9		V
t_{on}	Forward Turn-on time			200		ns
t_{rr}	Reverse recovery time			300		ns

* Pulsed: pulse duration ≤ 300µs, duty cycle ≤ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP311 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

Test circuit



Waveforms

Pulse width ≤ 100 µs
Duty cycle ≤ 2%
V_i = 10V

SEFM8N18
SEFMN820
SEFP8N18
SEFP8N20

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

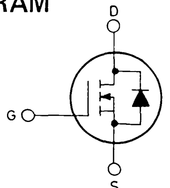
V_{DSS}	$R_{DS\ (ON)}$	I_D
180V/200V	0.4 Ω	8 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 8N18	8N20
V_{DS}	Drain-source voltage (V_{GS} = 0)	180V	200V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	180V	200V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	8A	
I_{DM}(•)	Drain current (pulsed)	25A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

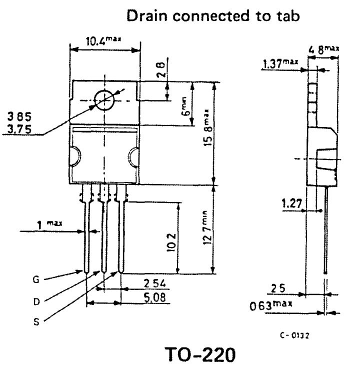
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

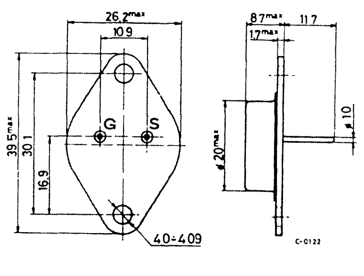
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM8N18/SEFP8N18** for **SEFM8N20/SEFP8N20**	 180 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 4 A		0.27	0.4	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 8 A V_{GS} = 10V I_D = 4 A T_j = 100°C			4 3.2	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 4 A	3			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		980 200 80	1200 260 100	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

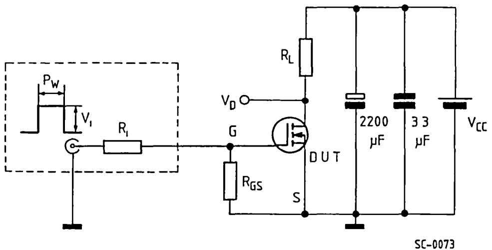
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		40		ns
t_r	Rise time	I_D = 0.5 Rated I_D		150		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		100		ns
t_f	Fall time	(see test circuit)		100		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		2.0		V
t_{on}	Forward Turn-on time			250		ns
t_{rr}	Reverse recovery time			325		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP363 Datasheet.

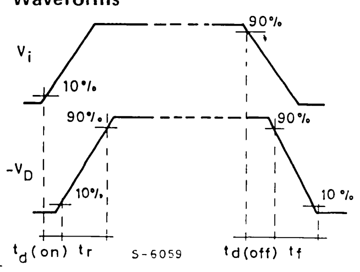
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEFM10N05
SEFM10N06
SEFP10N05
SEFP10N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

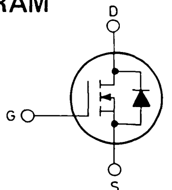
V_{DSS}	$R_{DS\ (ON)}$	I_D
50V/60V	0.28 Ω	10 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 10N05	SEFM or SEFP 10N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	10A	
I_{DM}(•)	Drain current (pulsed)	28A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

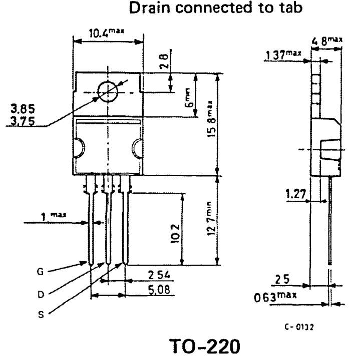
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

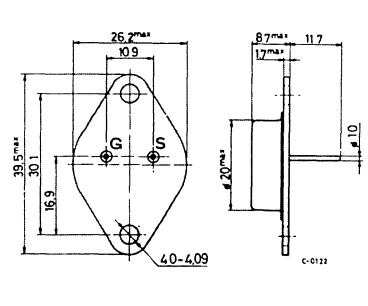
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

SEFM10N05
SEFM10N06
SEFP10N05
SEFP10N06

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM10N05/SEFP10N05** for **SEFM10N06/SEFP10N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 5 A		0.1	0.28	mΩ
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 10 A V_{GS} = 10V I_D = 5 A T_j = 100°C			3.4 2.8	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 5 A	2.5	3.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		30		ns
t_r	Rise time	I_D = 0.5 Rated I_D		130		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		80		ns
t_f	Fall time	(see test circuit)		130		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.9		V
t_{on}	Forward Turn-on time			200		ns
t_{rr}	Reverse recovery time			300		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP321 Datasheet.

SWITCHING TIMES RESISTIVE LOAD

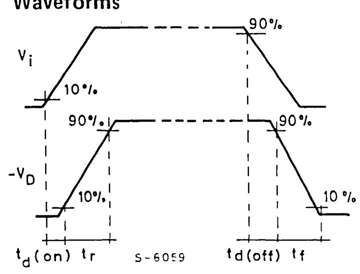
Test circuit

P_W V_i R_i V_D G R_{GS} S R_L DUT 2200 μF 33 μF V_{CC}

SC-0073

Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
V_i = 10V

Waveforms



SEFM10N08
SEFM10N10
SEFP10N08
SEFP10N10

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

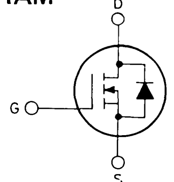
V_{DSS}	$R_{DS\ (ON)}$	I_D
80V/100V	**0.33 Ω**	**10 A**

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 10N08	SEFM or SEFP 10N10
V_{DS}	Drain-source voltage (V_{GS} = 0)	80V	100V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	80V	100V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	10A	
I_{DM}(•)	Drain current (pulsed)	25A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

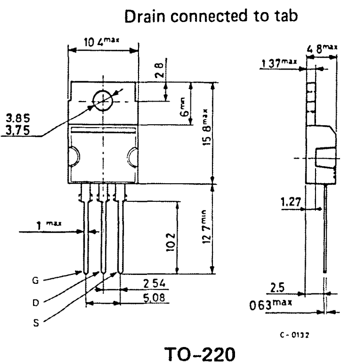
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

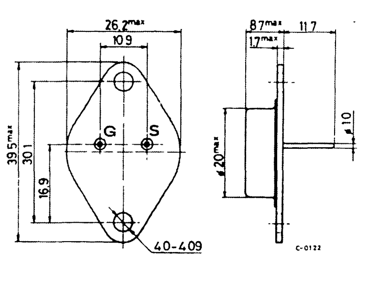
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM10N08/SEFP10N08** for **SEFM10N10/SEFP10N10**	 80 100			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 5 A		0.2	0.33	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 10 A V_{GS} = 10V I_D = 5 A T_j = 100°C			4 3.3	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 5 A	2.5	4		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		375	480 230 110	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

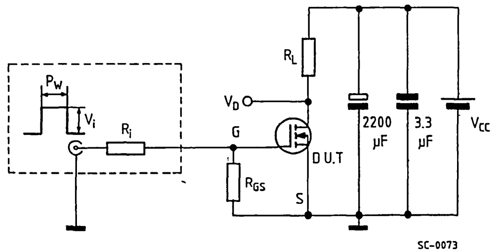
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 25$ V		50		ns
t_r	Rise time	$I_D = 0.5$ Rated I_D		150		ns
$t_{d\ (off)}$	Turn-off delay time	$R_{GS} = 50\ \Omega$ $R_i = 50\ \Omega$		100		ns
t_f	Fall time	(see test circuit)		50		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D $V_{GS} = 0$		2		V
t_{on}	Forward Turn-on time			80		ns
t_{rr}	Reverse recovery time			700		ns

* Pulsed: pulse duration $\leqslant 300\mu s$, duty cycle $\leqslant 2\%$

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP311 Datasheet.

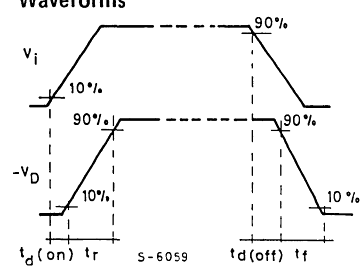
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width $\leqslant 100\ \mu s$
Duty cycle $\leqslant 2\%$
$V_i = 10V$

Waveforms



SEFM12N05
SEFM12N06
SEFP12N05
SEFP12N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

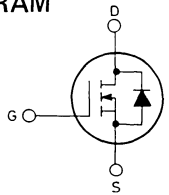
V_{DSS}	$R_{DS\ (ON)}$	I_D
50V/60V	**0.2 Ω**	**12 A**

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 12N05	SEFM or SEFP 12N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	12A	
I_{DM}(•)	Drain current (pulsed)	30A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

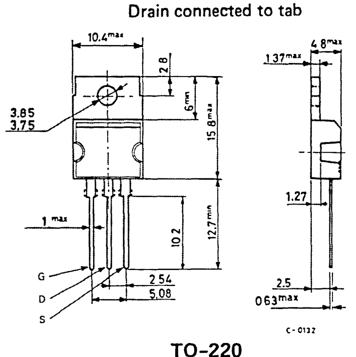
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

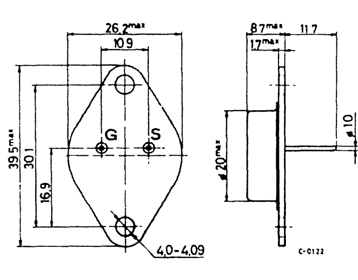
Dimensions in mm

Drain connected to tab



TO-220

Drain connected to case



TO-3

SEFM12N05
SEFM12N06
SEFP12N05
SEFP12N06

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM12N05/SEFP12N05** for **SEFM12N06/SEFP12N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 6 A		0.1	0.2	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 12 A V_{GS} = 10V I_D = 6 A T_j = 100°C			3.2 2.4	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 6 A	3			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

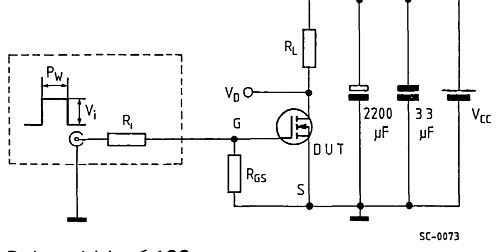
	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V		30		ns
t_r	Rise time	I_D = 0.5 Rated I_D		130		ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		80		ns
t_f	Fall time	(see test circuit)		130		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage			2		V
t_{on}	Forward Turn-on time	I_{SD} = Rated I_D V_{GS} = 0		80		ns
t_{rr}	Reverse recovery time			700		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP321 Datasheet.

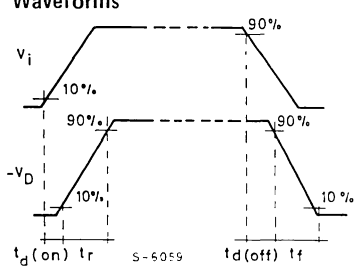
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

Waveforms



SEFM12N08
SEFM12N10
SEFP12N08
SEFP12N10

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

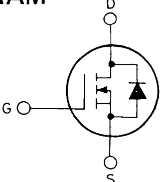
V_{DSS}	$R_{DS\ (ON)}$	I_D
80V/100V	0.18 Ω	12 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 12N08	SEFM or SEFP 12N10
V_{DS}	Drain-source voltage (V_{GS} = 0)	80V	100V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	80V	100V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	12A	
I_{DM}(•)	Drain current (pulsed)	30A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

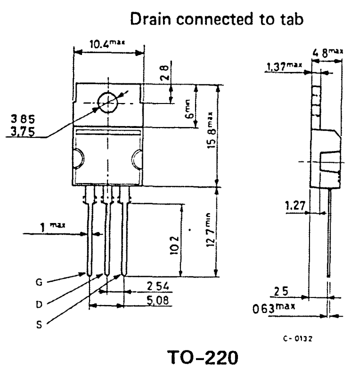
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM

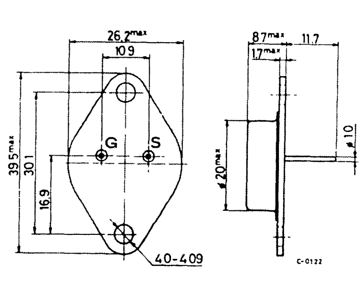


MECHANICAL DATA

Dimensions in mm



TO-220



TO-3

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM12N08/SEFP12N08** for **SEFM12N10/SEFP12N10**	 80 100			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 6 A		0.09	0.18	Ω Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10 V I_D = 12 A V_{GS} = 10 V I_D = 6 A T_j = 100°C			2.6 2.16	V V
g_{fs}	Forward transconductance	V_{DS} = 10 V I_D = 6 A	3	8.5		mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{DS} = 0 V		950 370 180	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

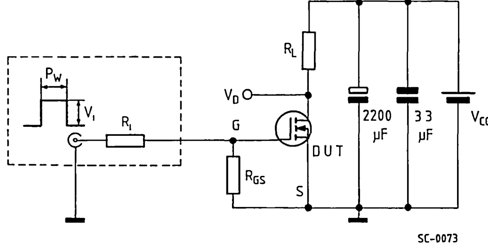
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 25$ V			50	ns
t_r	Rise time	$I_D = 0.5$ Rated I_D			150	ns
$t_{d\ (off)}$	Turn-off delay time	$R_{GS} = 50\ \Omega$ $R_i = 50\ \Omega$			200	ns
t_f	Fall time	(see test circuit)			100	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D $V_{GS} = 0$		1.4		V
t_{on}	Forward Turn-on time			250		ns
t_{rr}	Reverse recovery time			325		ns

* Pulsed: pulse duration $\leqslant 300\mu s$, duty cycle $\leqslant 2\%$

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP361 Datasheet.

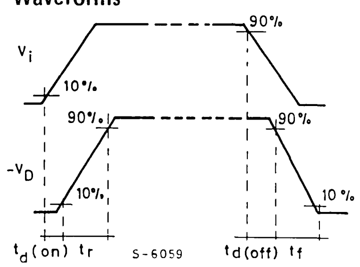
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width $\leqslant 100\ \mu s$
Duty cycle $\leqslant 2\%$
$V_i = 10V$

Waveforms



SEFM15N05
SEFM15N06
SEFP15N05
SEFP15N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate. N-Channel enhancement mode Power-Mos field effect transistors.

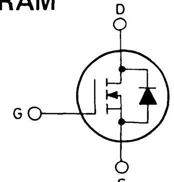
V_{DSS}	$R_{DS\,(ON)}$	I_D
50V/60V	0.16 Ω	15 A

ABSOLUTE MAXIMUM RATINGS

		SEFM or SEFP 15N05	SEFM or SEFP 15N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	15A	
I_{DM}(•)	Drain current (pulsed)	40A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 75°C	75W	
	Derating factor	0.6W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

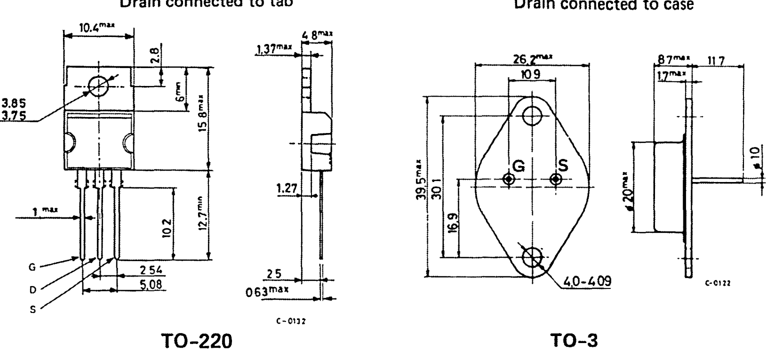
(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.67°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM15N05/SEFP15N05** for **SEFM15N06/SEFP15N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 7.5 A			0.16	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 15 A V_{GS} = 10V I_D = 7.5 A T_j = 100°C			2.9 2.4	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 7.5 A	3.5			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

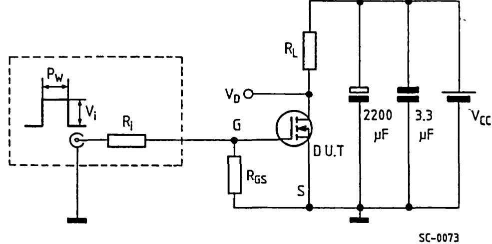
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	V_{CC} = 25 V			50	ns
t_r	Rise time	I_D = 0.5 Rated I_D			150	ns
$t_{d\ (off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω			200	ns
t_f	Fall time	(see test circuit)			100	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		1.4		V
t_{on}	Forward Turn-on time			250		ns
t_{rr}	Reverse recovery time			325		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP321 Datasheet.

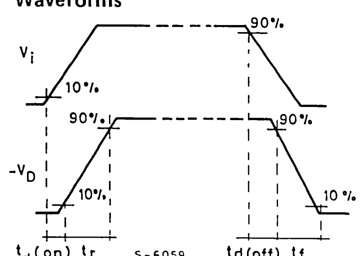
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

Waveforms



SEFM25N05
SEFM25N06
SEFP25N05
SEFP25N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

V_{DSS}	$R_{DS\ (ON)}$	I_D
50V/60V	0.08 Ω	25 A

ABSOLUTE MAXIMUM RATINGS

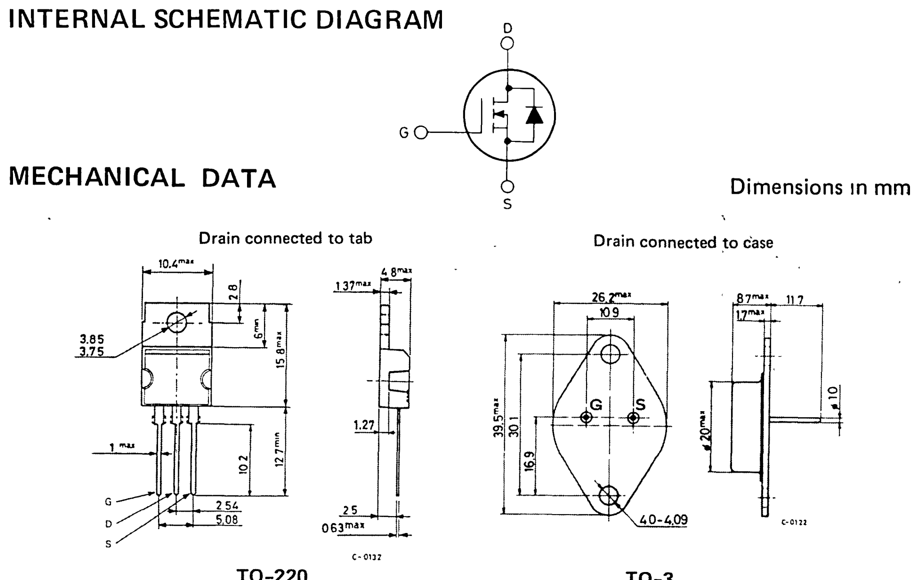
		SEFM or SEFP 25N05	SEFM or SEFP 25N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	25A	
I_{DM}(•)	Drain current (pulsed)	80A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	100W	
	Derating factor	0.8W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

INTERNAL SCHEMATIC DIAGRAM

MECHANICAL DATA

Dimensions in mm



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	1.25°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 for **SEFM25N05/SEFP25N05** for **SEFM25N06/SEFP25N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 12.5 A			0.08	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10V I_D = 25 A V_{GS} = 10V I_D = 12.5 A T_j = 100°C			2.4 2.0	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 12.5 A	6			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1100 600 300	1400 800 400	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

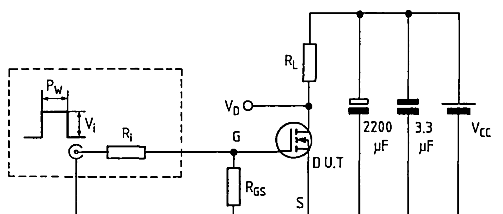
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\ (on)}$	Turn-on delay time	$V_{CC} = 25$ V			50	ns
t_r	Rise time	$I_D = 0.5$ Rated I_D			450	ns
$t_{d\ (off)}$	Turn-off delay time	$R_{GS} = 50\ \Omega$ $R_i = 50\ \Omega$			100	ns
t_f	Fall time	(see test circuit)			200	ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D $V_{GS} = 0$		2.5		V
t_{on}	Forward Turn-on time			50		ns
t_{rr}	Reverse recovery time			300		ns

* Pulsed: pulse duration ⩽ 300μs, duty cycle ⩽ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP381 Datasheet.

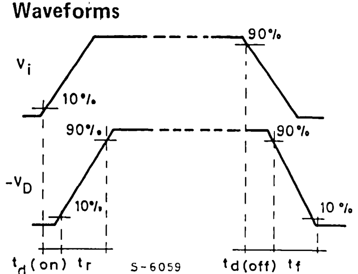
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ⩽ 100 μs
Duty cycle ⩽ 2%
$V_i = 10V$

Waveforms



SEFP5N05
SEFP5N06

N-CHANNEL POWER MOS TRANSISTORS

HIGH SPEED SWITCHING APPLICATIONS

These products are diffused multi-cell silicon gate N-Channel enhancement mode Power-Mos field effect transistors.

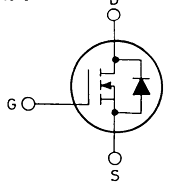
V_{DSS}	$R_{DS\ (ON)}$	I_D
50V/60V	0.6 Ω	5 A

ABSOLUTE MAXIMUM RATINGS

		SEFP 5N05	SEFP 5N06
V_{DS}	Drain-source voltage (V_{GS} = 0)	50V	60V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	50V	60V
V_{GS}	Gate-source voltage	±20V	
I_D	Drain current (continuous) T_{case} = 25°C	5A	
I_{DM}(•)	Drain current (pulsed)	10A	
I_{GM}	Gate current (pulsed)	1.5A	
P_{tot}	Total power dissipation at T_{case} = 25°C	50W	
	Derating factor	0.4W/°C	
T_{stg}	Storage temperature	-65 to 150°C	
T_j	Max. operating junction temperature	150°C	

(•) Pulse width limited by safe operating area

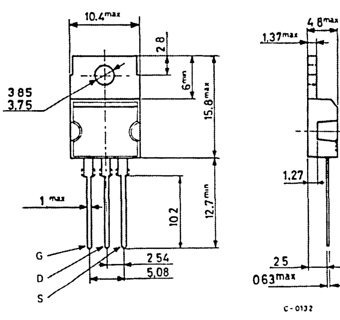
INTERNAL SCHEMATIC DIAGRAM



MECHANICAL DATA

Dimensions in mm

Drain connected to tab



TO-220

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max.	2.5°C/W
T_L	Maximum lead temperature for soldering purpose		275°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 5 mA V_{GS} = 0 V for **SEFP5N05** for **SEFP5N06**	 50 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 0.85 Rated V_{DSS} T_j = 100°C			250 2.5	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			500	nA
ON*						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA T_j = 100°C	2 1.5		4.5 4.0	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10V I_D = 2.5 A			0.6	Ω
$V_{DS\ (on)}$	Drain-source On voltage	V_{GS} = 10 V I_D = 5 A V_{GS} = 10V I_D = 2.5 A T_j = 100°C			3.75 3	V V
g_{fs}	Forward transconductance	V_{DS} = 15V I_D = 2.5 A	0.75			mho
DYNAMIC						
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		180	250 100 40	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

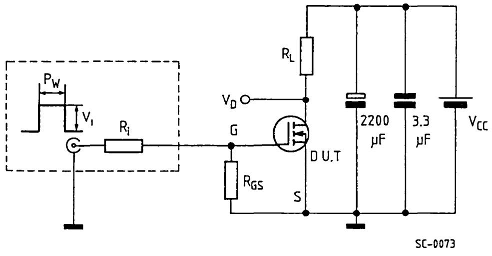
Parameter		Test conditions	Min.	Typ.	Max.	Unit.
SWITCHING						
$t_{d\,(on)}$	Turn-on delay time	V_{CC} = 25 V		30		ns
t_r	Rise time	I_D = 0.5 Rated I_D		50		ns
$t_{d\,(off)}$	Turn-off delay time	R_{GS} = 50 Ω R_i = 50 Ω		50		ns
t_f	Fall time	(see test circuit)		30		ns
SOURCE DRAIN DIODE						
V_{SD}	Forward on voltage	I_{SD} = Rated I_D V_{GS} = 0		2.5		V
t_{on}	Forward Turn-on time			150		ns
t_{rr}	Reverse recovery time			250		ns

* Pulsed: pulse duration ≤ 300μs, duty cycle ≤ 2%

For typical curves, and clamping inductive load, gate charge, body drain diode trr measurement test circuits see SGSP351 Datasheet.

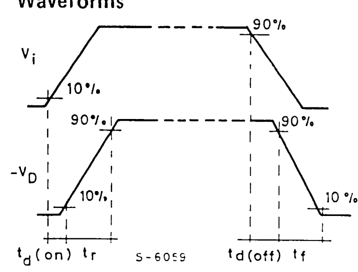
SWITCHING TIMES RESISTIVE LOAD

Test circuit



Pulse width ≤ 100 μs
Duty cycle ≤ 2%
V_i = 10V

Waveforms



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