POWER MOS DEVICES

DATABOOK

1st EDITION

SGS-THOMSON MICROELECTRONICS

POWER MOS DEVICES

DATABOOK

1st EDITION

JUNE 1988

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1 - Life support devices or systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2 - A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

POWER MOS devices are made using well proven SGS-THOMSON technology. POWER MOS technology stands, with equal stature, firmly alongside the company's POWER BIPOLAR technologies. This DATABOOK has been produced to complement the advances in silicon technology and isolated packaging.

The DATABOOK contains data sheets and technical notes on the range of POWER MOS devices for applications in industrial, automotive, computer, telecommunication, professional, and consumer equipment.

Selection guides are provided in the following pages to facilitate rapid identification of the most suitable device for the intended use.

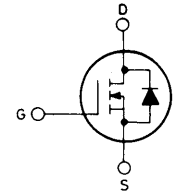
The extensive information makes it easy to evaluate the performance of the product within any required equipment design.

N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

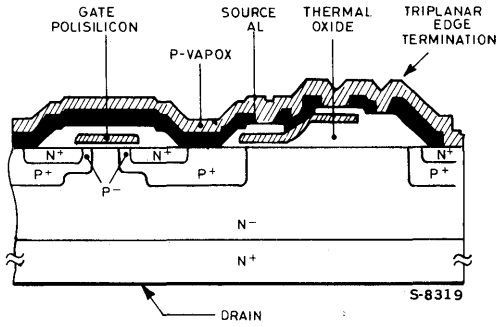
MAIN FEATURES:

- ULTRA FAST SWITCHING
- EASY DRIVE
- VERY LOW STORAGE TIME
- LOW SWITCHING LOSSES
- NO SECONDARY BREAKDOWN

INTERNAL SCHEMATIC DIAGRAM



Standard structure



POWER MOS is a technology used to produce power devices featuring easy drive and high switching speed.

POWER MOS transistors are produced using a DMOS structure where the channel is obtained by lateral diffusion. The surface has a two tier structure; the lower level is the polysilicon gate, and the upper level is the source metallization. The structure is self-aligning as the polysilicon holes are used as a mask for the P^- well and the N^+ source diffusion. The MOS channel is created by the difference in lateral diffusion of the two impurity distributions.

The resulting accuracy of this process controls the channel length to $\leqslant$ 1.5 microns and the use of a polycrystalline gate maintains a high stability of threshold voltage.

POWER MOS devices are available in a low voltage group, 50-250 volts V_{DSS} and high voltage range 250 to 1000 volt V_{DSS}. Devices with a maximum drain current of 52 A per chip are currently available. When used in a pulse mode, $I_{DSS\ max} \simeq 4 \times I_{DSS}$ or more.

Applications are in the field of power control and include, DC-DC converters, switching power supplies, actuator drivers, motor control, robotics etc. The latest development in POWER MOS technology has generated high density cell structures which for the same surface area increase the current density of these devices. High density POWER MOS devices are designed for breakdown voltages up to 100V, which is the maximum voltage where increasing the cell density can give real advantages in current capability (or RDSon).

Type	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
BUZ10	50	0.08	13.00	TO-220	20.00	70	8.00	700typ	159
BUZ10A	50	0.12	10.00	TO-220	17.00	75	3.00	2000	163
BUZ11	50	0.04	15.00	TO-220	30.00	75	4.00	2000	167
BUZ11A	50	0.06	15.00	TO-220	25.00	75	4.00	2000	173
BUZ11FI	50	0.04	15.00	ISOWATT220	20.00	35	4.00	2000	167
BUZ11S2	60	0.04	15.00	TO-220	30.00	75	4.00	2000	177
BUZ11S2FI	60	0.04	15.00	ISOWATT220	20.00	35	4.00	2000	177
BUZ20	100	0.20	6.00	TO-220	12.00	75	2.70	2000	183
BUZ21	100	0.10	9.00	TO-220	19.00	75	4.00	2000	187
BUZ25	100	0.10	9.00	TO-3	19.00	78	4.00	2000	191
BUZ32	200	0.40	4.50	TO-220	9.50	75	2.20	2000	195
BUZ41A	500	1.50	2.50	TO-220	4.50	75	1.50	2000	199
BUZ42	500	2.00	2.50	TO-220	4.00	75	1.50	2000	203
BUZ45	500	0.60	5.00	TO-3	9.60	125	2.70	4900	207
BUZ45A	500	0.80	5.00	TO-3	8.30	125	2.70	4900	211
BUZ60	400	1.00	2.50	TO-220	5.50	75	1.70	2000	215
BUZ60B	400	1.50	2.50	TO-220	4.50	75	1.70	2000	219
BUZ71	50	0.10	9.00	TO-220	14.00	40	3.00	650	223
BUZ71A	50	0.12	9.00	TO-220	13.00	40	3.00	650	229
BUZ71FI	50	0.10	9.00	ISOWATT220	12.00	30	3.00	650	223
BUZ72A	100	0.25	5.00	TO-220	9.00	40	2.70	600	233
BUZ74	500	3.00	1.20	TO-220	2.40	40	0.80	500	237
BUZ74A	500	4.00	1.20	TO-220	2.00	40	0.80	500	241
BUZ76	400	1.80	1.50	TO-220	3.00	40	0.80	500	245
BUZ76A	400	2.50	1.50	TO-220	2.60	40	0.80	500	249
BUZ353	500	0.60	5.50	TO-220	9.50	125	2.70	4900	253
BUZ354	500	0.80	5.50	TO-218	8.00	125	2.70	4900	257
IRF140	100	0.077	17.00	TO-3	28.00	125	8.70	1600	261
IRF141	80	0.077	17.00	TO-3	28.00	125	8.70	1600	261
IRF142	100	0.10	17.00	TO-3	25.00	125	8.70	1600	261
IRF143	80	0.10	17.00	TO-3	25.00	125	8.70	1600	261
IRF150	100	0.055	20.00	TO-3	40.00	150	9.00	3000	267
IRF151	60	0.055	20.00	TO-3	40.00	150	9.00	3000	267
IRF152	100	0.08	20.00	TO-3	33.00	150	9.00	3000	267
IRF153	60	0.08	20.00	TO-3	33.00	150	9.00	3000	267
IRF350	400	0.30	8.00	TO-3	15.00	150	8.00	3000	273
IRF450	500	0.40	7.20	TO-3	13.00	150	8.70	3000	279
IRF451	450	0.40	7.20	TO-3	13.00	150	8.70	3000	279
IRF452	500	0.50	7.20	TO-3	11.00	150	8.70	3000	279
IRF453	450	0.50	7.20	TO-3	11.00	150	8.70	3000	279
IRF520	100	0.27	5.60	TO-220	9.20	60	2.70	600	285
IRF520FI	100	0.27	5.60	ISOWATT220	7.00	30	2.70	600	285
IRF521	80	0.27	5.60	TO-220	9.20	60	2.70	600	285
IRF521FI	80	0.27	5.60	ISOWATT220	7.00	30	2.70	600	285
IRF522	100	0.36	5.60	TO-220	8.00	60	2.70	600	285

Type	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
IRF522FI	100	0.36	5.60	ISOWATT220	6.00	30	2.70	600	285
IRF523	80	0.36	5.60	TO-220	8.00	60	2.70	600	285
IRF523FI	80	0.36	5.60	ISOWATT220	6.00	30	2.70	600	285
IRF530	100	0.16	8.30	TO-220	14.00	79	5.10	800	291
IRF530FI	100	0.16	8.30	ISOWATT220	9.00	35	5.10	800	291
IRF531	80	0.16	8.30	TO-220	14.00	79	5.10	800	291
IRF531FI	80	0.16	8.30	ISOWATT220	9.00	35	5.10	800	291
IRF532	100	0.23	8.30	TO-220	12.00	79	5.10	800	291
IRF532FI	100	0.23	8.30	ISOWATT220	8.00	35	5.10	800	291
IRF533	80	0.23	8.30	TO-220	12.00	79	5.10	800	291
IRF533FI	80	0.23	8.30	ISOWATT220	8.00	35	5.10	800	291
IRF540	100	0.077	17.00	TO-220	28.00	125	8.70	1600	295
IRF540FI	100	0.077	17.00	ISOWATT220	15.00	40	8.70	1600	295
IRF541	80	0.077	17.00	TO-220	28.00	125	8.70	1600	295
IRF541FI	80	0.077	17.00	ISOWATT220	15.00	40	8.70	1600	295
IRF542	100	0.10	17.00	TO-220	25.00	125	8.70	1600	295
IRF542FI	100	0.10	17.00	ISOWATT220	14.00	40	8.70	1600	295
IRF543	80	0.10	17.00	TO-220	25.00	125	8.70	1600	295
IRF543FI	80	0.10	17.00	ISOWATT220	14.00	40	8.70	1600	295
IRF620	200	0.80	2.50	TO-220	5.00	40	1.30	600	301
IRF620FI	200	0.80	2.50	ISOWATT220	4.00	30	1.30	600	301
IRF621	150	0.80	2.50	TO-220	5.00	40	1.30	600	301
IRF621FI	150	0.80	2.50	ISOWATT220	4.00	30	1.30	600	301
IRF622	200	1.20	2.50	TO-220	4.00	40	1.30	600	301
IRF622FI	200	1.20	2.50	ISOWATT220	3.50	30	1.30	600	301
IFR623	150	1.20	2.50	TO-220	4.00	40	1.30	600	301
IRF623FI	150	1.20	2.50	ISOWATT220	3.50	30	1.30	600	301
IRF720	400	1.80	1.80	TO-220	3.30	50	1.00	600	307
IRF720FI	400	1.80	1.80	ISOWATT220	2.50	30	1.00	600	307
IRF721	350	1.80	1.80	TO-220	3.30	50	1.00	600	307
IRF721FI	350	1.80	1.80	ISOWATT220	2.50	30	1.00	600	307
IRF722	400	2.50	1.80	TO-220	2.80	50	1.00	600	307
IRF722FI	400	2.50	1.80	ISOWATT220	2.00	30	1.00	600	307
IRF723	350	2.50	1.80	TO-220	2.80	50	1.00	600	307
IRF723FI	350	2.50	1.80	ISOWATT220	2.00	30	1.00	600	307
IRF730	400	1.00	3.00	TO-220	5.50	74	2.90	800	313
IRF730FI	400	1.00	3.00	ISOWATT220	3.50	35	2.90	800	313
IRF731	350	1.00	3.00	TO-220	5.50	74	2.90	800	313
IRF731FI	350	1.00	3.00	ISOWATT220	3.50	35	2.90	800	313
IRF732	400	1.50	3.00	TO-220	4.50	74	2.90	800	313
IRF732FI	400	1.50	3.00	ISOWATT220	3.00	35	2.90	800	313
IRF733	350	1.50	3.00	TO-220	4.50	74	2.90	800	313
IRF733FI	350	1.50	3.00	ISOWATT220	3.00	35	2.90	800	313
IRF740	400	0.55	5.20	TO-220	10.00	125	4.00	1600	319
IRF740FI	400	0.55	5.20	ISOWATT220	5.50	40	4.00	1600	319

Type	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
IRF741	350	0.55	5.20	TO-220	10.00	125	4.00	1600	319
IRF741FI	350	0.55	5.20	ISOWATT220	5.50	40	4.00	1600	319
IRF742	400	0.80	5.20	TO-220	8.30	125	4.00	1600	319
IRF742FI	400	0.80	5.20	ISOWATT220	4.50	40	4.00	1600	319
IRF743	350	0.80	5.20	TO-220	8.30	125	4.00	1600	319
IRF743FI	350	0.80	5.20	ISOWATT220	4.50	40	4.00	1600	319
IRF820	500	3.00	1.40	TO-220	2.50	50	1.00	400	325
IRF820FI	500	3.00	1.40	ISOWATT220	2.00	30	1.00	400	325
IRF821	450	3.00	1.40	TO-220	2.50	50	1.00	400	325
IRF821FI	450	3.00	1.40	ISOWATT220	2.00	30	1.00	400	325
IRF822	500	4.00	1.40	TO-220	2.20	50	1.00	400	325
IRF822FI	500	4.00	1.40	ISOWATT220	1.50	30	1.00	400	325
IRF823	450	4.00	1.40	TO-220	2.20	50	1.00	400	325
IRF823FI	450	4.00	1.40	ISOWATT220	1.50	30	1.00	400	325
IRF830	500	1.50	2.50	TO-220	4.50	74	2.70	800	331
IRF830FI	500	1.50	2.50	ISOWATT220	3.00	35	2.70	800	331
IRF831	450	1.50	2.50	TO-220	4.50	74	2.70	800	331
IRF831FI	450	1.50	2.50	ISOWATT220	3.00	35	2.70	800	331
IRF832	500	2.00	2.50	TO-220	4.00	74	2.70	800	331
IRF832FI	500	2.00	2.50	ISOWATT220	2.50	35	2.70	800	331
IRF833	450	2.00	2.50	TO-220	4.00	74	2.70	800	331
IRF833FI	450	2.00	2.50	ISOWATT220	2.50	35	2.70	800	331
IRF840	500	0.85	4.40	TO-220	8.00	125	4.90	1600	337
IRF840FI	500	0.85	4.40	ISOWATT220	4.50	40	4.90	1600	337
IRF841	450	0.85	4.40	TO-220	8.00	125	4.90	1600	337
IRF841FI	450	0.85	4.40	ISOWATT220	4.50	40	4.90	1600	337
IRF842	500	1.10	4.40	TO-220	7.00	125	4.90	1600	337
IRF842FI	500	1.10	4.40	ISOWATT220	4.00	40	4.90	1600	337
IRF843	450	1.10	4.40	TO-220	7.00	125	4.90	1600	337
IRF843FI	450	1.10	4.40	ISOWATT220	4.00	40	4.90	1600	337
IRFP150	100	0.055	22.00	TO-218	40.00	150	13.00	3000	343
IRFP150FI	100	0.055	22.00	ISOWATT218	26.00	65	13.00	3000	343
IRFP151	60	0.055	22.00	TO-218	40.00	150	13.00	3000	343
IRFP151FI	60	0.055	22.00	ISOWATT218	26.00	65	13.00	3000	343
IRFP152	100	0.08	22.00	TO-218	34.00	150	13.00	3000	343
IRFP152FI	100	0.08	22.00	ISOWATT218	21.00	65	13.00	3000	343
IRFP153	60	0.08	22.00	TO-218	34.00	150	13.00	3000	343
IRFP153FI	60	0.08	22.00	ISOWATT218	21.00	65	13.00	3000	343
IRFP350FI	400	0.30	8.00	ISOWATT218	10.00	70	8.00	3000	349
IRFP450	500	0.40	7.20	TO-218	14.00	180	8.70	3000	355
IRFP450FI	500	0.40	7.20	ISOWATT218	9.00	70	8.70	3000	355
IRFP451	450	0.40	7.20	TO-218	14.00	180	8.70	3000	355
IRFP451FI	450	0.40	7.20	ISOWATT218	9.00	70	8.70	3000	355
IRFP452	500	0.50	7.20	TO-218	12.00	180	8.70	3000	355
IRFP452FI	500	0.50	7.20	ISOWATT218	8.00	70	8.70	3000	355

Type	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
IRFP453	450	0.50	7.20	TO-218	12.00	180	8.70	3000	355
IRFP453FI	450	0.50	7.20	ISOWATT218	8.00	70	8.70	3000	355
IRFZ20	50	0.10	9.00	TO-220	15.00	40	5.00	850	361
IRFZ20FI	50	0.10	9.00	ISOWATT220	12.50	30	5.00	850	361
IRFZ22	50	0.12	9.00	TO-220	14.00	40	5.00	850	361
IRFZ22FI	50	0.12	9.00	ISOWATT220	12.00	30	5.00	850	361
IRFZ40	50	0.028	29.00	TO-220	35.00	125	17.00	3000	367
IRFZ42	50	0.035	29.00	TO-220	35.00	125	17.00	3000	367
MTH6N60FI	600	1.20	3.00	ISOWATT218	3.50	40	2.00	1800	373
MTH40N06	60	0.028	20.00	TO-218	40.00	150	10.00	5000	379
MTH40N06FI	60	0.028	20.00	ISOWATT218	26.00	65	10.00	5000	379
MTP3N60	600	2.50	1.50	TO-220	3.00	75	1.50	1000	385
MTP3N60FI	600	2.50	1.50	ISOWATT220	2.50	35	1.50	1000	385
MTP6N60	600	1.20	3.00	TO-220	6.00	125	2.00	1800	391
MTP15N05L	50	0.15	7.50	TO-220	15.00	75	5.00	900	397
MTP15N05LFI	50	0.15	7.50	ISOWATT220	10.00	30	5.00	900	397
MTP15N06L	60	0.15	7.50	TO-220	15.00	75	5.00	900	397
MTP15N06LFI	60	0.15	7.50	ISOWATT220	10.00	30	5.00	900	397
MTP3055A	60	0.15	6.00	TO-220	12.00	40	4.50	500	403
MTP3055AFI	60	0.15	6.00	ISOWATT220	10.00	30	4.50	500	403
SGS30MA050D1	500	0.20	15.00	TO-240	30.00	400	15.00	9100	409
SGS35MA050D1	500	0.16	17.50	TO-240	35.00	400	15.00	12000	415
SGS100MA010D1	100	0.014	50.00	TO-240	120.00	400	20.00	11200	421
SGS150MA010D1	100	0.009	75.00	TO-240	150.00	400	20.00	14000	427
SGSP201	100	1.40	1.20	SOT-82	2.50	18	0.50	125	433
SGSP222	50	0.13	5.00	SOT-82	10.00	50	3.00	550	439
SGSP230	450	3.00	1.20	SOT-82	2.50	50	0.80	450	445
SGSP239	500	8.50	0.60	SOT-82	1.20	40	0.65	300	451
SGSP301	100	1.40	1.20	TO-220	2.50	18	0.50	125	457
SGSP311	100	0.30	5.50	TO-220	11.00	75	2.00	480	463
SGSP316	250	1.20	2.50	TO-220	5.00	75	1.50	500	469
SGSP317	200	0.75	3.00	TO-220	6.00	75	1.50	500	469
SGSP319	500	3.80	1.40	TO-220	2.80	75	0.80	380	475
SGSP321	60	0.13	8.00	TO-220	16.00	75	3.00	550	481
SGSP322	50	0.13	8.00	TO-220	16.00	75	3.00	550	481
SGSP330	450	3.00	1.50	TO-220	3.00	75	0.80	450	487
SGSP341	400	20.00	0.30	TO-220	0.60	18	0.10	105	493
SGSP351	100	0.60	3.00	TO-220	6.00	50	1.00	250	499
SGSP358	50	0.30	3.50	TO-220	7.00	50	1.50	270	505
SGSP361	100	0.15	9.00	TO-220	18.00	100	4.50	1200	511
SGSP362	80	0.10	11.00	TO-220	22.00	100	4.50	1200	511
SGSP363	250	0.45	5.00	TO-220	10.00	100	3.00	1200	517
SGSP364	450	1.50	2.50	TO-220	5.00	100	3.00	1000	523
SGSP367	200	0.33	6.00	TO-220	12.00	100	3.00	1200	517
SGSP369	500	1.50	2.50	TO-220	5.00	100	3.00	1000	523

Type	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
SGSP381	60	0.06	14.00	TO-220	28.00	100	5.00	1400	529
SGSP382	50	0.06	14.00	TO-220	28.00	100	5.00	1400	529
SGSP461	100	0.15	10.00	TO-218	20.00	125	4.50	1200	535
SGSP462	80	0.10	12.50	TO.218	25.00	125	4.50	1200	535
SGSP471	100	0.075	15.00	TO-218	30.00	150	9.00	2200	541
SGSP472	80	0.05	17.50	TO-218	35.00	150	9.00	2200	541
SGSP474	450	0.70	4.50	TO-218	9.00	150	6.00	2100	547
SGSP475	400	0.55	5.00	TO-218	10.00	150	6.00	2100	547
SGSP477	200	0.17	10.00	TO-218	20.00	150	8.00	2200	553
SGSP479	500	0.70	4.50	TO-218	9.00	150	5.00	1900	559
SGSP481	60	0.06	15.00	TO-218	30.00	125	5.00	1400	565
SGSP482	50	0.06	15.00	TO-218	30.00	125	5.00	1400	565
SGSP491	60	0.033	20.00	TO-218	40.00	150	10.00	2800	571
SGSP492	50	0.033	20.00	TO-218	40.00	150	10.00	2800	571
SGSP574	450	0.70	4.50	TO-3	9.00	150	6.00	2100	577
SGSP575	400	0.55	5.00	TO-3	10.00	150	6.00	2100	577
SGSP577	200	0.17	10.00	TO-3	20.00	150	8.00	2200	583
SGSP579	500	0.70	4.50	TO-3	9.00	150	5.00	1900	589
SGSP591	60	0.033	20.00	TO-3	40.00	150	10.00	2800	595
SGSP592	50	0.033	20.00	TO-3	40.00	150	10.00	2800	595
STHV82	800	2.00	2.00	TO-218	5.50	125	2.00	1000	601
STHV102	1000	3.50	2.00	TO-218	4.20	125	2.00	1200	607
STLT19	50	0.15	7.50	TO-220	15.00	75	5.00	480	611
STLT19FI	50	0.15	7.50	ISOWATT220	10.00	30	5.00	480	611
STLT20	60	0.15	7.50	TO-220	15.00	75	5.00	480	611
STLT20FI	60	0.15	7.50	ISOWATT220	10.00	30	5.00	480	611
STLT29	50	0.08	12.50	TO-220	25.00	100	9.00	1200	617
STLT30	60	0.08	12.50	TO-220	25.00	100	9.00	1200	617
STVHD90	50	0.023	30.00	TO-220	52.00	125	30.00	3000	621

HIMOS (IGBT)

Type	$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
STHI07N50	500	2.70	7.00	TO-220	7.00	100	2.50	950	627
STHI07N50FI	500	2.70	7.00	ISOWATT220	7.00	35	2.50	950	627
STHI10N50	500	2.70	10.00	TO-220	10.00	100	2.50	950	633
STHI10N50FI	500	2.70	10.00	ISOWATT220	10.00	35	2.50	950	633

SELECTION GUIDE BY VOLTAGE

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.30	3.50	TO-220	SGSP358	7.00	50	1.50	270	505
50	0.15	7.50	TO-220	MTP15N05L	15.00	75	5.00	900	397
50	0.15	7.50	ISOWATT220	MTP15N05LFI	10.00	30	5.00	900	397
50	0.15	7.50	TO-220	STLT19	15.00	75	5.00	480	611
50	0.15	7.50	ISOWATT220	STLT19FI	10.00	30	5.00	480	611
50	0.13	5.00	SOT-82	SGSP222	10.00	50	3.00	550	439
50	0.13	8.00	TO-220	SGSP322	16.00	75	3.00	550	481
50	0.12	10.00	TO-220	BUZ10A	17.00	75	3.00	2000	163
50	0.12	9.00	TO-220	BUZ71A	13.00	40	3.00	650	229
50	0.12	9.00	TO-220	IRFZ22	14.00	40	5.00	850	361
50	0.12	9.00	ISOWATT220	IRFZ22FI	12.00	30	5.00	850	361
50	0.10	9.00	TO-220	BUZ71	14.00	40	3.00	650	223
50	0.10	9.00	ISOWATT220	BUZ71FI	12.00	30	3.00	650	223
50	0.10	9.00	TO-220	IRFZ20	15.00	40	5.00	850	361
50	0.10	9.00	ISOWATT220	IRFZ20FI	12.50	30	5.00	850	361
50	0.08	13.00	TO-220	BUZ10	20.00	70	8.00	700 typ	159
50	0.08	12.50	TO-220	STLT29	25.00	100	9.00	1200	617
50	0.06	15.00	TO-220	BUZ11A	25.00	75	4.00	2000	173
50	0.06	14.00	TO-220	SGSP382	28.00	100	5.00	1400	529
50	0.06	15.00	TO-218	SGSP482	30.00	125	5.00	1400	565
50	0.04	15.00	TO-220	BUZ11	30.00	75	4.00	2000	167
50	0.04	15.00	ISOWATT220	BUZ11FI	20.00	35	4.00	2000	167
50	0.035	29.00	TO-220	IRFZ42	35.00	125	17.00	3000	367
50	0.033	20.00	TO-218	SGSP492	40.00	150	10.00	2800	571
50	0.033	20.00	TO-3	SGSP592	40.00	150	10.00	2800	595
50	0.028	29.00	TO-220	IRFZ40	35.00	125	17.00	3000	367
50	0.023	30.00	TO-220	STVHD90	52.00	125	30.00	3000	621
60	0.15	7.50	TO-220	MTP15N06L	15.00	75	5.00	900	397
60	0.15	7.50	ISOWATT220	MTP15N06LFI	10.00	30	5.00	900	397
60	0.15	6.00	TO-220	MTP3055A	12.00	40	4.50	500	403
60	0.15	6.00	ISOWATT220	MTP3055AFI	10.00	30	4.50	500	403
60	0.15	7.50	TO-220	STLT20	15.00	75	5.00	480	611
60	0.15	7.50	ISOWATT220	STLT20FI	10.00	30	5.00	480	611
60	0.13	8.00	TO-220	SGSP321	16.00	75	3.00	550	481
60	0.08	20.00	TO-3	IRF153	33.00	150	9.00	3000	267
60	0.08	22.00	TO-218	IRFP153	34.00	150	13.00	3000	343
60	0.08	22.00	ISOWATT218	IRFP153FI	21.00	65	13.00	3000	343
60	0.08	12.50	TO-220	STLT30	25.00	100	9.00	1200	617
60	0.06	14.00	TO-220	SGSP381	28.00	100	5.00	1400	529
60	0.06	15.00	TO-218	SGSP481	30.00	125	5.00	1400	565
60	0.055	20.00	TO-3	IRF151	40.00	150	9.00	3000	267
60	0.055	22.00	TO-218	IRFP151	40.00	150	13.00	3000	343
60	0.055	22.00	ISOWATT218	IRFP151FI	26.00	65	13.00	3000	343
60	0.04	15.00	TO-220	BUZ11S2	30.00	75	4.00	2000	177
60	0.04	15.00	ISOWATT220	BUZ11S2FI	20.00	35	4.00	2000	177

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
60	0.033	20.00	TO-218	SGSP491	40.00	150	10.00	2800	571
60	0.033	20.00	TO-3	SGSP591	40.00	150	10.00	2800	595
60	0.028	20.00	TO-218	MTH40N06	40.00	150	10.00	5000	379
60	0.028	20.00	ISOWATT218	MTH40N06FI	26.00	65	10.00	5000	379
80	0.36	5.60	TO-220	IRF523	8.00	60	2.70	600	285
80	0.36	5.60	ISOWATT220	IRF523FI	6.00	30	2.70	600	285
80	0.27	5.60	TO-220	IRF521	9.20	60	2.70	600	285
80	0.27	5.60	ISOWATT220	IRF521FI	7.00	30	2.70	600	285
80	0.23	8.30	TO-220	IRF533	12.00	79	5.10	800	291
80	0.23	8.30	ISOWATT220	IRF533FI	8.00	35	5.10	800	291
80	0.16	8.30	TO-220	IRF531	14.00	79	5.10	800	291
80	0.16	8.30	ISOWATT220	IRF531FI	9.00	35	5.10	800	291
80	0.10	17.00	TO-3	IRF143	25.00	125	8.70	1600	261
80	0.10	17.00	TO-220	IRF543	25.00	125	8.70	1600	295
80	0.10	17.00	ISOWATT220	IRF543FI	14.00	40	8.70	1600	295
80	0.10	11.00	TO-220	SGSP362	22.00	100	4.50	1200	511
80	0.10	12.50	TO-218	SGSP462	25.00	125	4.50	1200	535
80	0.077	17.00	TO-3	IRF141	28.00	125	8.70	1600	261
80	0.077	17.00	TO-220	IRF541	28.00	125	8.70	1600	295
80	0.077	17.00	ISOWATT220	IRF541FI	15.00	40	8.70	1600	295
80	0.05	17.50	TO-218	SGSP472	35.00	150	9.00	2200	541
100	1.40	1.20	SOT-82	SGSP201	2.50	18	0.50	125	433
100	1.40	1.20	TO-220	SGSP301	2.50	18	0.50	125	457
100	0.60	3.00	TO-220	SGSP351	6.00	50	1.00	250	499
100	0.36	5.60	TO-220	IRF522	8.00	60	2.70	600	285
100	0.36	5.60	ISOWATT220	IRF522FI	6.00	30	2.70	600	285
100	0.30	5.50	TO-220	SGSP311	11.00	75	2.00	480	463
100	0.27	5.60	TO-220	IRF520	9.20	60	2.70	600	285
100	0.27	5.60	ISOWATT220	IRF520FI	7.00	30	2.70	600	285
100	0.25	5.00	TO-220	BUZ72A	9.00	40	2.70	600	233
100	0.23	8.30	TO-220	IRF532	12.00	79	5.10	800	291
100	0.23	8.30	ISOWATT220	IRF532FI	8.00	35	5.10	800	291
100	0.20	6.00	TO-220	BUZ20	12.00	75	2.70	2000	183
100	0.16	8.30	TO-220	IRF530	14.00	79	5.10	800	291
100	0.16	8.30	ISOWATT220	IRF530FI	9.00	35	5.10	800	291
100	0.15	9.00	TO-220	SGSP361	18.00	100	4.50	1200	511
100	0.15	10.00	TO-218	SGSP461	20.00	125	4.50	1200	535
100	0.10	9.00	TO-220	BUZ21	19.00	75	4.00	2000	187
100	0.10	9.00	TO-3	BUZ25	19.00	78	4.00	2000	191
100	0.10	17.00	TO-3	IRF142	25.00	125	8.70	1600	261
100	0.10	17.00	TO-220	IRF542	25.00	125	8.70	1600	295
100	0.10	17.00	ISOWATT220	IRF542FI	14.00	40	8.70	1600	295
100	0.08	20.00	TO-3	IRF152	33.00	150	9.00	3000	267
100	0.08	22.00	TO-218	IRFP152	34.00	150	13.00	3000	343
100	0.08	22.00	ISOWATT218	IRFP152FI	21.00	65	13.00	3000	343

SELECTION GUIDE BY VOLTAGE

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
100	0.077	17.00	TO-3	IRF140	28.00	125	8.70	1600	261
100	0.077	17.00	TO-220	IRF540	28.00	125	8.70	1600	295
100	0.077	17.00	ISOWATT220	IRF540FI	15.00	40	8.70	1600	295
100	0.075	15.00	TO-218	SGSP471	30.00	150	9.00	2200	541
100	0.055	20.00	TO-3	IRF150	40.00	150	9.00	3000	267
100	0.055	22.00	TO-218	IRFP150	40.00	150	13.00	3000	343
100	0.055	22.00	ISOWATT218	IRFP150FI	26.00	65	13.00	3000	343
100	0.014	50.00	TO-240	SGS100MA010D1	120.00	400	20.00	11200	421
100	0.009	75.00	TO-240	SGS150MA010D1	150.00	400	20.00	14000	427
150	1.20	2.50	TO-220	IRF623	4.00	40	1.30	600	301
150	1.20	2.50	ISOWATT220	IRF623FI	3.50	30	1.30	600	301
150	0.80	2.50	TO-220	IRF621	5.00	40	1.30	600	301
150	0.80	2.50	ISOWATT220	IRF621FI	4.00	30	1.30	600	301
200	1.20	2.50	TO-220	IRF622	4.00	40	1.30	600	301
200	1.20	2.50	ISOWATT220	IRF622FI	3.50	30	1.30	600	301
200	0.80	2.50	TO-220	IRF620	5.00	40	1.30	600	301
200	0.80	2.50	ISOWATT220	IRF620FI	4.00	30	1.30	600	301
200	0.75	3.00	TO-220	SGSP317	6.00	75	1.50	500	469
200	0.40	4.50	TO-220	BUZ32	9.50	75	2.20	2000	195
200	0.33	6.00	TO-220	SGSP367	12.00	100	3.00	1200	517
200	0.17	10.00	TO-218	SGSP477	20.00	150	8.00	2200	553
200	0.17	10.00	TO-3	SGSP577	20.00	150	8.00	2200	583
250	1.20	2.50	TO-220	SGSP316	5.00	75	1.50	500	469
250	0.45	5.00	TO-220	SGSP363	10.00	100	3.00	1200	517
350	2.50	1.80	TO-220	IRF723	2.80	50	1.00	600	307
350	2.50	1.80	ISOWATT220	IRF723FI	2.00	30	1.00	600	307
350	1.80	1.80	TO-220	IRF721	3.30	50	1.00	600	307
350	1.80	1.80	ISOWATT220	IRF721FI	2.50	30	1.00	600	307
350	1.50	3.00	TO-220	IRF733	4.50	74	2.90	800	313
350	1.50	3.00	ISOWATT220	IRF733FI	3.00	35	2.90	800	313
350	1.00	3.00	TO-220	IRF731	5.50	74	2.90	800	313
350	1.00	3.00	ISOWATT220	IRF731FI	3.50	35	2.90	800	313
350	0.80	5.20	TO-220	IRF743	8.30	125	4.00	1600	319
350	0.80	5.20	ISOWATT220	IRF743FI	4.50	40	4.00	1600	319
350	0.55	5.20	TO-220	IRF741	10.00	125	4.00	1600	319
350	0.55	5.20	ISOWATT220	IRF741FI	5.50	40	4.00	1600	319
400	20.00	0.30	TO-220	SGSP341	0.60	18	0.10	105	493
400	2.50	1.50	TO-220	BUZ76A	2.60	40	0.80	500	249
400	2.50	1.80	TO-220	IRF722	2.80	50	1.00	600	307
400	2.50	1.80	ISOWATT220	IRF722FI	2.00	30	1.00	600	307
400	1.80	1.50	TO-220	BUZ76	3.00	40	0.80	500	245
400	1.80	1.80	TO-220	IRF720	3.30	50	1.00	600	307
400	1.80	1.80	ISOWATT220	IRF720FI	2.50	30	1.00	600	307
400	1.50	2.50	TO-220	BUZ60B	4.50	75	1.70	2000	219
400	1.50	3.00	TO-220	IRF732	4.50	74	2.90	800	313

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Package	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
400	1.50	3.00	ISOWATT220	IRF732FI	3.00	35	2.90	800	313
400	1.00	2.50	TO-220	BUZ60	5.50	75	1.70	2000	215
400	1.00	3.00	TO-220	IRF730	5.50	74	2.90	800	313
400	1.00	3.00	ISOWATT220	IRF730FI	3.50	35	2.90	800	313
400	0.80	5.20	TO-220	IRF742	8.30	125	4.00	1600	319
400	0.80	5.20	ISOWATT220	IRF742FI	4.50	40	4.00	1600	319
400	0.55	5.20	TO-220	IRF740	10.00	125	4.00	1600	319
400	0.55	5.20	ISOWATT220	IRF740FI	5.50	40	4.00	1600	319
400	0.55	5.00	TO-218	SGSP475	10.00	150	6.00	2100	547
400	0.55	5.00	TO-3	SGSP575	10.00	150	6.00	2100	577
400	0.30	8.00	TO-3	IRF350	15.00	150	8.00	3000	273
400	0.30	8.00	ISOWATT218	IRFP350FI	10.00	70	8.00	3000	349
450	4.00	1.40	TO-220	IRF823	2.20	50	1.00	400	331
450	4.00	1.40	ISOWATT220	IRF823FI	1.50	30	1.00	400	331
450	3.00	1.40	TO-220	IRF821	2.50	50	1.00	400	331
450	3.00	1.40	ISOWATT220	IRF821FI	2.00	30	1.00	400	331
450	3.00	1.20	SOT-82	SGSP230	2.50	50	0.80	450	445
450	3.00	1.50	TO-220	SGSP330	3.00	75	0.80	450	487
450	2.00	2.50	TO-220	IRF833	4.00	74	2.70	800	331
450	2.00	2.50	ISOWATT220	IRF833FI	2.50	35	2.70	800	331
450	1.50	2.50	TO-220	IRF831	4.50	74	2.70	800	331
450	1.50	2.50	ISOWATT220	IRF831FI	3.00	35	2.70	800	331
450	1.50	2.50	TO-220	SGSP364	5.00	100	3.00	1000	523
450	1.10	4.40	TO-220	IRF843	7.00	125	4.90	1600	337
450	1.10	4.40	ISOWATT220	IRF843FI	4.00	40	4.90	1600	337
450	0.85	4.40	TO-220	IRF841	8.00	125	4.90	1600	337
450	0.85	4.40	ISOWATT220	IRF841FI	4.50	40	4.90	1600	337
450	0.70	4.50	TO-218	SGSP474	9.00	150	6.00	2100	547
450	0.70	4.50	TO-3	SGSP574	9.00	150	6.00	2100	577
450	0.50	7.00	TO-3	IRF453	11.00	150	8.70	3000	279
450	0.50	7.20	TO-218	IRFP453	12.00	150	8.70	3000	355
450	0.50	7.20	ISOWATT218	IRFP453FI	8.00	70	8.70	3000	355
450	0.40	7.20	TO-3	IRF451	13.00	150	8.70	3000	279
450	0.40	7.20	TO-218	IRFP451	14.00	150	8.70	3000	355
450	0.40	7.20	ISOWATT218	IRFP451FI	9.00	70	8.70	3000	355
500	8.50	0.60	SOT-82	SGSP239	1.20	40	0.65	300	451
500	4.00	1.20	TO-220	BUZ74A	2.00	40	0.80	500	241
500	4.00	1.40	TO-220	IRF822	2.20	50	1.00	400	325
500	4.00	1.40	ISOWATT220	IRF822FI	1.50	30	1.00	400	325
500	3.80	1.40	TO-220	SGSP319	2.80	75	0.80	380	475
500	3.00	1.20	TO-220	BUZ74	2.40	40	0.80	500	237
500	3.00	1.40	TO-220	IRF820	2.50	50	1.00	400	325
500	3.00	1.40	ISOWATT220	IRF820FI	2.00	30	1.00	400	325
500	2.00	2.50	TO-220	BUZ42	4.00	75	1.50	2000	203
500	2.00	2.50	TO-220	IRF832	4.00	74	2.70	800	325

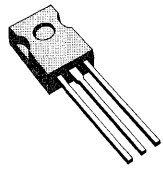
SELECTION GUIDE BY VOLTAGE

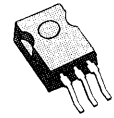
$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Package	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
500	2.00	2.50	ISOWATT220	IRF832FI	2.50	35	2.70	800	325
500	1.50	2.50	TO-220	BUZ41A	4.50	75	1.50	2000	199
500	1.50	2.50	TO-220	IRF830	4.50	74	2.70	800	331
500	1.50	2.50	ISOWATT220	IRF830FI	3.00	35	2.70	800	331
500	1.50	2.50	TO-220	SGSP369	5.00	100	3.00	1000	523
500	1.10	4.40	TO-220	IRF842	7.00	125	4.90	1600	337
500	1.10	4.40	ISOWATT220	IRF842FI	4.00	40	4.90	1600	337
500	0.85	4.40	TO-220	IRF840	8.00	125	4.90	1600	337
500	0.85	4.40	ISOWATT220	IRF840FI	4.50	40	4.90	1600	337
500	0.80	5.50	TO-218	BUZ354	8.00	125	2.70	4900	249
500	0.80	5.00	TO-3	BUZ45A	8.30	125	2.70	4900	211
500	0.70	4.50	TO-218	SGSP479	9.00	150	5.00	1900	559
500	0.70	4.50	TO-3	SGSP579	9.00	150	5.00	1900	589
500	0.60	5.50	TO-218	BUZ353	9.50	125	2.70	4900	253
500	0.60	5.00	TO-3	BUZ45	9.60	125	2.70	4900	207
500	0.50	7.20	TO-3	IRF452	11.00	150	8.70	3000	279
500	0.50	7.20	TO-218	IRFP452	12.00	150	8.70	3000	355
500	0.50	7.20	ISOWATT218	IRFP452FI	8.00	70	8.70	3000	355
500	0.40	7.20	TO-3	IRF450	13.00	150	8.70	3000	279
500	0.40	7.20	TO-218	IRFP450	14.00	150	8.70	3000	355
500	0.40	7.20	ISOWATT218	IRFP450FI	9.00	70	8.70	3000	355
500	0.20	15.00	TO-240	SGS30MA050D1	30.00	400	15.00	9100	409
500	0.16	17.50	TO-240	SGS35MA050D1	35.00	400	15.00	12000	415
600	2.50	1.50	TO-220	MTP3N60	3.00	75	1.50	1000	385
600	2.50	1.50	ISOWATT220	MTP3N60FI	2.50	35	1.50	1000	385
600	1.20	3.00	ISOWATT218	MTH6N60FI	3.50	40	2.00	1800	367
600	1.20	3.00	TO-220	MTP6N60	6.00	125	2.00	1800	391
800	2.00	2.00	TO-218	STHV82	5.50	125	2.00	1000	601
1000	3.50	2.00	TO-218	STHV102	4.20	125	2.00	1200	607

HIMOS (IGBT)

$V_{(BR)DSS}$ (V)	$V_{DS(on)}$ (max) (V) @	I_D (A)	Package	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
500	2.70	7.00	TO-220	STH107N50	7.00	100	2.50	950	627
500	2.70	7.00	ISOWATT220	STH10N50	7.00	35	2.50	950	627
500	2.70	10.00	TO-220	STHI10N50	10.00	100	2.50	950	633
500	2.70	10.00	ISOWATT220	STHI10N50FI	10.00	35	2.50	950	633

SOT-82

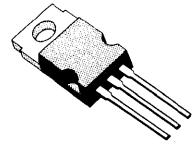




OPTION
SOT-194

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.13	5.00	SGSP222	10.00	50	3.00	550	439
100	1.40	1.20	SGSP201	2.50	18	0.50	125	433
450	3.00	1.20	SGSP230	2.50	50	0.80	450	445
500	8.50	0.60	SGSP239	1.20	40	0.65	300	451

TO-220



$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.30	3.50	SGSP358	7.00	50	1.50	270	505
50	0.15	7.50	MTP15N05L	15.00	75	5.00	900	397
50	0.15	7.50	STLT19	15.00	75	5.00	480	611
50	0.13	8.00	SGSP322	16.00	75	3.00	550	481
50	0.12	10.00	BUZ10A	17.00	75	3.00	2000	163
50	0.12	9.00	BUZ71A	13.00	40	3.00	650	229
50	0.12	9.00	IRFZ22	14.00	40	5.00	850	361
50	0.10	9.00	BUZ71	14.00	40	3.00	650	223
50	0.10	9.00	IRFZ20	15.00	40	5.00	850	361
50	0.08	12.50	STLT29	25.00	100	9.00	1200	617
50	0.08	13.00	BUZ10	20.00	70	8.00	700 typ	159
50	0.06	15.00	BUZ11A	25.00	75	4.00	2000	173
50	0.06	14.00	SGSP382	28.00	100	5.00	1400	529
50	0.04	15.00	BUZ11	30.00	75	4.00	2000	167
50	0.035	29.00	IRFZ42	35.00	125	17.00	3000	367

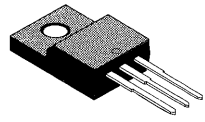
TO-220 (continueed)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.028	29.00	IRFZ40	35.00	125	17.00	3000	367
50	0.023	30.00	STVHD90	52.00	125	30.00	3000	621
60	0.15	7.50	MTP15N06L	15.00	75	5.00	900	397
60	0.15	6.00	MTP3055A	12.00	40	4.50	500	403
60	0.15	7.50	STLT20	15.00	75	5.00	480	611
60	0.13	8.00	SGSP321	16.00	75	3.00	550	481
60	0.08	12.50	STLT30	25.00	100	9.00	1200	617
60	0.06	14.00	SGSP381	28.00	100	5.00	1400	529
60	0.04	15.00	BUZ11S2	30.00	75	4.00	2000	177
80	0.36	5.60	IRF523	8.00	60	2.70	600	285
80	0.27	5.60	IRF521	9.20	60	2.70	600	285
80	0.23	8.30	IRF533	12.00	79	5.10	800	291
80	0.16	8.30	IRF531	14.00	79	5.10	800	291
80	0.10	17.00	IRF543	25.00	125	8.70	1600	295
80	0.10	11.00	SGSP362	22.00	100	4.50	1200	511
80	0.077	17.00	IRF541	28.00	125	8.70	1600	295
100	1.40	1.20	SGSP301	2.50	18	0.50	125	457
100	0.60	3.00	SGSP351	6.00	50	1.00	250	499
100	0.36	5.60	IRF522	8.00	60	2.70	600	285
100	0.30	5.50	SGSP311	11.00	75	2.00	480	463
100	0.27	5.60	IRF520	9.20	60	2.70	600	285
100	0.25	5.00	BUZ72A	9.00	40	2.70	600	233
100	0.23	8.30	IRF532	12.00	79	5.10	800	291
100	0.20	6.00	BUZ20	12.00	75	2.70	2000	183
100	0.16	8.30	IRF530	14.00	79	5.10	800	291
100	0.15	9.00	SGSP361	18.00	100	4.50	1200	511
100	0.10	9.00	BUZ21	19.00	75	4.00	2000	187
100	0.10	17.00	IRF542	25.00	125	8.70	1600	295
100	0.077	17.00	IRF540	28.00	125	8.70	1600	295
150	1.20	2.50	IRF623	4.00	40	1.30	600	301
150	0.80	2.50	IRF621	5.00	40	1.30	600	301
200	1.20	2.50	IRF622	4.00	40	1.30	600	301
200	0.80	2.50	IRF620	5.00	40	1.30	600	301
200	0.75	3.00	SGSP317	6.00	75	1.50	500	469
200	0.40	4.50	BUZ32	9.50	75	2.20	2000	195
200	0.33	6.00	SGSP367	12.00	100	3.00	1200	517
250	1.20	2.50	SGSP316	5.00	75	1.50	500	469
250	0.45	5.00	SGSP363	10.00	100	3.00	1200	517
350	2.50	1.80	IRF723	2.80	50	1.00	600	307
350	1.80	1.80	IRF721	3.30	50	1.00	600	307
350	1.50	3.00	IRF733	4.50	74	2.90	800	313
350	1.00	3.00	IRF731	5.50	74	2.90	800	313
350	0.80	5.20	IRF743	8.30	125	4.00	1600	319
350	0.55	5.20	IRF741	10.00	125	4.00	1600	319
400	20.00	0.30	SGSP341	0.60	18	0.10	105	493

TO-220 (continueed)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
400	2.50	1.50	BUZ76A	2.60	40	0.80	500	249
400	2.50	1.80	IRF722	2.80	50	1.00	600	307
400	1.80	1.50	BUZ76	3.00	40	0.80	500	245
400	1.80	1.80	IRF720	3.30	50	1.00	600	307
400	1.50	2.50	BUZ60B	4.50	75	1.70	2000	219
400	1.50	3.00	IRF732	4.50	74	2.90	800	313
400	1.00	2.50	BUZ60	5.50	75	1.70	2000	215
400	1.00	3.00	IRF730	5.50	74	2.90	800	313
400	0.80	5.20	IRF742	8.30	125	4.00	1600	319
400	0.55	5.20	IRF740	10.00	125	4.00	1600	319
450	4.00	1.40	IRF823	2.20	50	1.00	400	325
450	3.00	1.40	IRF821	2.50	50	1.00	400	325
450	3.00	1.50	SGSP330	3.00	75	0.80	450	487
450	2.00	2.50	IRF833	4.00	74	2.70	800	331
450	1.50	2.50	IRF831	4.50	74	2.70	800	331
450	1.50	2.50	SGSP364	5.00	100	3.00	1000	523
450	1.10	4.40	IRF843	7.00	125	4.90	1600	337
450	0.85	4.40	IRF841	8.00	125	4.90	1600	337
500	4.00	1.20	BUZ74A	2.00	40	0.80	500	241
500	4.00	1.40	IRF822	2.20	50	1.00	400	325
500	3.80	1.40	SGSP319	2.80	75	0.80	380	475
500	3.00	1.20	BUZ74	2.40	40	0.80	500	237
500	3.00	1.40	IRF820	2.50	50	1.00	400	325
500	2.00	2.50	BUZ42	4.00	75	1.50	2000	203
500	2.00	2.50	IRF832	4.00	74	2.70	800	331
500	1.50	2.50	BUZ41A	4.50	75	1.50	2000	199
500	1.50	2.50	IRF830	4.50	74	2.70	800	331
500	1.50	2.50	SGSP369	5.00	100	3.00	1000	523
500	1.10	4.40	IRF842	7.00	125	4.90	1600	337
500	0.85	4.40	IRF840	8.00	125	4.90	1600	337
600	2.50	1.50	MTP3N60	3.00	75	1.50	1000	385
600	1.20	3.00	MTP6N60	6.00	125	2.00	1800	391

ISOWATT220

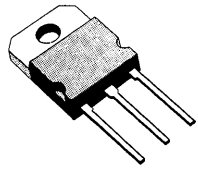


$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.15	7.50	MTP15N05LFI	10.00	30	5.00	900	397
50	0.15	7.50	STLT19FI	10.00	30	5.00	480	611
50	0.12	9.00	IRFZ22FI	12.00	30	5.00	850	361
50	0.10	9.00	BUZ71FI	12.00	30	3.00	650	223
50	0.10	9.00	IRFZ20FI	12.50	30	5.00	850	361
50	0.04	15.00	BUZ11FI	20.00	35	4.00	2000	167
60	0.15	7.50	MTP15N06LFI	10.00	30	5.00	900	397
60	0.15	6.00	MTP3055AFI	10.00	30	4.50	500	403
60	0.15	7.50	STLT20FI	10.00	30	5.00	480	611
60	0.04	15.00	BUZ11S2FI	20.00	35	4.00	2000	177
80	0.36	5.60	IRF523FI	6.00	30	2.70	600	285
80	0.27	5.60	IRF521FI	7.00	30	2.70	600	285
80	0.23	8.30	IRF533FI	8.00	35	5.10	800	291
80	0.16	8.30	IRF531FI	9.00	35	5.10	800	291
80	0.10	17.00	IRF543FI	14.00	40	8.70	1600	295
80	0.077	17.00	IRF541FI	15.00	40	8.70	1600	295
100	0.36	5.60	IRF522FI	6.00	30	2.70	600	285
100	0.27	5.60	IRF520FI	7.00	30	2.70	600	285
100	0.23	8.30	IRF532FI	8.00	35	5.10	800	291
100	0.16	8.30	IRF530FI	9.00	35	5.10	800	291
100	0.10	17.00	IRF542FI	14.00	40	8.70	1600	295
100	0.077	17.00	IRF540FI	15.00	40	8.70	1600	295
150	1.20	2.50	IRF623FI	3.50	30	1.30	600	301
150	0.80	2.50	IRF621FI	4.00	30	1.30	600	301
200	1.20	2.50	IRF622FI	3.50	30	1.30	600	301
200	0.80	2.50	IRF620FI	4.00	30	1.30	600	301
350	2.50	1.80	IRF723FI	2.00	30	1.00	600	307
350	1.80	1.80	IRF721FI	2.50	30	1.00	600	307
350	1.50	3.00	IRF733FI	3.00	35	2.90	800	313
350	1.00	3.00	IRF731FI	3.50	35	2.90	800	313
350	0.80	5.20	IRF743FI	4.50	40	4.00	1600	319
350	0.55	5.20	IRF741FI	5.50	40	4.00	1600	319
400	2.50	1.80	IRF722FI	2.00	30	1.00	600	307
400	1.80	1.80	IRF720FI	2.50	30	1.00	600	307
400	1.50	3.00	IRF732FI	3.00	35	2.90	800	313

ISOWATT220 (continueed)

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
400	1.00	3.00	IRF730FI	3.50	35	2.90	800	313
400	0.80	5.20	IRF742FI	4.50	40	4.00	1600	319
400	0.55	5.20	IRF740FI	5.50	40	4.00	1600	319
450	4.00	1.40	IRF823FI	1.50	30	1.00	400	325
450	3.00	1.40	IRF821FI	2.00	30	1.00	400	325
450	2.00	2.50	IRF833FI	2.50	35	2.70	800	331
450	1.50	2.50	IRF831FI	3.00	35	2.70	800	331
450	1.10	4.40	IRF843FI	4.00	40	4.90	1600	337
450	0.85	4.40	IRF841FI	4.50	40	4.90	1600	337
500	4.00	1.40	IRF822FI	1.50	30	1.00	400	325
500	3.00	1.40	IRF820FI	2.00	30	1.00	400	325
500	2.00	2.50	IRF832FI	2.50	35	2.70	800	331
500	1.50	2.50	IRF830FI	3.00	35	2.70	800	331
500	1.10	4.40	IRF842FI	4.00	40	4.90	1600	337
500	0.85	4.40	IRF840FI	4.50	40	4.90	1600	337
600	2.50	1.50	MTP3N60FI	2.50	35	1.50	1000	385

TO-218

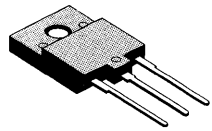


$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.06	15.00	SGSP482	30.00	125	5.00	1400	565
50	0.033	20.00	SGSP492	40.00	150	10.00	2800	571
60	0.08	22.00	IRFP153	34.00	150	13.00	3000	343
60	0.06	15.00	SGSP481	30.00	125	5.00	1400	565
60	0.055	22.00	IRFP151	40.00	150	13.00	3000	343
60	0.033	20.00	SGSP491	40.00	150	10.00	2800	571
60	0.028	20.00	MTH40N06	40.00	150	10.00	5000	379
80	0.10	12.50	SGSP462	25.00	125	4.50	1200	535
80	0.05	17.50	SGSP472	35.00	150	9.00	2200	541
100	0.15	10.00	SGSP461	20.00	125	4.50	1200	535

TO-218 (continueed)

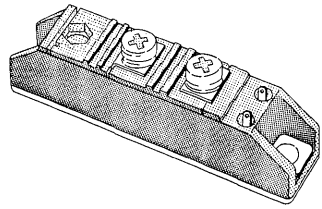
$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
100	0.08	22.00	IRFP152	34.00	150	13.00	3000	343
100	0.075	15.00	SGSP471	30.00	150	9.00	2200	541
100	0.055	22.00	IRFP150	40.00	150	13.00	3000	343
200	0.17	10.00	SGSP477	20.00	150	8.00	2200	553
400	0.55	5.00	SGSP475	10.00	150	6.00	2100	547
450	0.70	4.50	SGSP474	9.00	150	6.00	2100	547
450	0.50	7.20	IRFP453	12.00	150	8.70	3000	355
450	0.40	7.20	IRFP451	14.00	150	8.70	3000	355
500	0.80	5.50	BUZ354	8.00	125	2.70	4900	257
500	0.70	4.50	SGSP479	9.00	150	5.00	1900	559
500	0.60	5.50	BUZ353	9.50	125	2.70	4900	253
500	0.50	7.20	IRFP452	12.00	150	8.70	3000	355
500	0.40	7.20	IRFP450	14.00	150	8.70	3000	355
800	2.00	2.00	STHV82	5.50	125	2.00	1000	601
1000	3.50	2.00	STHV102	4.20	125	2.00	1200	607

ISOWATT218



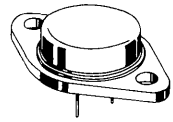
$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
60	0.08	22.00	IRFP153FI	21.00	65	13.00	3000	343
60	0.055	22.00	IRFP151FI	26.00	65	13.00	3000	343
60	0.028	20.00	MTH40N06FI	26.00	65	10.00	5000	379
100	0.08	22.00	IRFP152FI	21.00	65	13.00	3000	343
100	0.055	22.00	IRFP150FI	26.00	65	13.00	3000	343
400	0.30	8.00	IRFP350FI	10.00	70	8.00	3000	349
450	0.50	7.20	IRFP453FI	8.00	70	8.70	3000	355
450	0.40	7.20	IRFP451FI	9.00	70	8.70	3000	355
500	0.50	7.20	IRFP452FI	8.00	70	8.70	3000	355
500	0.40	7.20	IRFP450FI	9.00	70	8.70	3000	355
600	1.20	3.00	MTH6N60FI	3.50	40	2.00	1800	373

TO-240



$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
100	0.016	50.00	SGS100MA010D1	120.00	400	20.00	11200	421
100	0.009	75.00	SGS150MA010D1	150.00	400	20.00	14000	427
500	0.20	15.00	SGS30MA050D1	30.00	400	15.00	9100	409
500	0.16	17.50	SGS35MA050D1	35.00	400	15.00	12000	415

TO-3

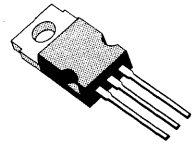


$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ @ (max) (Ω)	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
50	0.033	20.00	SGSP592	40.00	150	10.00	2800	595
60	0.08	20.00	IRF153	33.00	150	9.00	3000	267
60	0.055	20.00	IRF151	40.00	150	9.00	3000	267
60	0.033	20.00	SGSP591	40.00	150	10.00	2800	595
80	0.10	17.00	IRF143	25.00	125	8.70	1600	261
80	0.077	17.00	IRF141	28.00	125	8.70	1600	261
100	0.10	9.00	BUZ25	19.00	78	4.00	2000	191
100	0.10	17.00	IRF142	25.00	125	8.70	1600	261
100	0.08	20.00	IRF152	33.00	150	9.00	3000	267
100	0.077	17.00	IRF140	28.00	125	8.70	1600	261
100	0.055	20.00	IRF150	40.00	150	9.00	3000	267
200	0.17	10.00	SGSP577	20.00	150	8.00	2200	583
400	0.55	5.00	SGSP575	10.00	150	6.00	2100	577
400	0.30	8.00	IRF350	15.00	150	8.00	3000	273
450	0.70	4.50	SGSP574	9.00	150	6.00	2100	577

TO-3 (continueed)

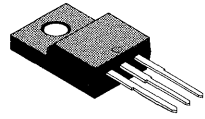
$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (Ω) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
450	0.50	7.20	IRF453	11.00	150	8.70	3000	279
450	0.40	7.20	IRF451	13.00	150	8.70	3000	279
500	0.80	5.00	BUZ45A	8.30	125	2.70	4900	211
500	0.70	4.50	SGSP579	9.00	150	5.00	1900	589
500	0.60	5.00	BUZ45	9.60	125	2.70	4900	207
500	0.50	7.20	IRF452	11.00	150	8.70	3000	279
500	0.40	7.20	IRF450	13.00	150	8.70	3000	279

TO-220 (HIMOS)



$V_{(BR)DSS}$ (V)	$V_{DS(on)}$ (max) (V) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
500	2.70	7.00	STHI07N50	7.00	100	2.50	9.50	627
500	2.70	10.00	STHI10N50	10.00	100	2.50	9.50	633

ISOWATT220 (HIMOS)



$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (max) (V) @	I_D (A)	Type	$I_{D(max)}$ (A)	P_{tot} (W)	g_{fs} min (mho)	C_{iss} max (pF)	Page
500	2.70	7.00	STHI07N50FI	7.00	35	2.50	9.50	627
500	2.70	10.00	STHI10N50FI	10.00	35	2.50	9.50	633

INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE	INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE
2SK295		SGSP351	499	BUZ11A	BUZ11A		173
2SK296		IRF723	307	BUZ11FI	BUZ11FI		167
2SK308		IRF142	261	BUZ11P	BUZ11FI		167
2SK310		IRF722	307	BUZ11S2	BUZ11S2		177
2SK311		IRF833	331	BUZ11S2FI	BUZ11S2FI		177
2SK312		SGSP575	577	BUZ14		SGSP591	595
2SK313		IRF453	279	BUZ15		SGSP591	595
2SK319		IRF730	313	BUZ20	BUZ20		183
2SK320		IRF843	337	BUZ21	BUZ21		187
2SK324		SGSP575	577	BUZ24	BUZ24		*
2SK345		SGSP358	505	BUZ25	BUZ25		191
2SK346		IRF523	285	BUZ32	BUZ32		195
2SK349		IRFP453	355	BUZ34	BUZ34		*
2SK350		IRFP453	355	BUZ41A	BUZ41A		199
2SK357		SGSP317	469	BUZ42	BUZ42		203
2SK382		IRF822	325	BUZ45	BUZ45		207
2SK383		IRF530	291	BUZ45A	BUZ45A		211
2SK399		SGSP461	535	BUZ60	BUZ60		215
2SK403		SGSP474	547	BUZ60B	BUZ60B		219
2SK428		SGSP321	481	BUZ64		SGSP575	577
2SK440		SGSP367	517	BUZ71	BUZ71		223
2SK512		IRF452	279	BUZ71A	BUZ71A		229
2SK527		MTP3055AFI	403	BUZ71FI	BUZ71FI		223
2SK528		IRF722FI	307	BUZ71P	BUZ71FI		223
2SK532		IRF540FI	295	BUZ72A	BUZ72A		233
2SK549		MTP3055A	403	BUZ73A		SGSP367	517
2SK552		IRF843	337	BUZ74	BUZ74		237
2SK553		IRF842	337	BUZ74A	BUZ74A		241
2SK554		IRF841	337	BUZ76	BUZ76		245
2SK555		IRF840	337	BUZ76A	BUZ76A		249
2SK556		IRFP453	355	BUZ353	BUZ353		253
2SK557		IRFP452	355	BUZ354	BUZ354		257
2SK560		IRFP450	355	IRF140	IRF140		261
2SK643		SGSP474	547	IRF141	IRF141		261
2SK644		SGSP479	559	IRF142	IRF142		261
2SK672		BUZ72A	233	IRF143	IRF143		261
2SK673		MTP3055A	403	IRF150	IRF150		267
2SK674		SGSP381	529	IRF151	IRF151		267
2SK708		IRFP453FI	355	IRF152	IRF152		267
2SK788		IRFP452	355	IRF153	IRF153		267
2SK789		IRFP451	355	IRF240	IRF240		*
2SK790		IRFP450	355	IRF241	IRF241		*
BUZ10	BUZ10		159	IRF242	IRF242		*
BUZ10A	BUZ10A		163	IRF243	IRF243		*
BUZ11	BUZ11		167	IRF340		SGSP575	577

* Datasheet available on request.

INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE	INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE
IRF342		SGSP575	577	IRF541FI	IRF541FI		295
IRF350	IRF350		273	IRF541P	IRF541FI		295
IRF351		IRF350	273	IRF542	IRF542		295
IRF352		IRF350	273	IRF542FI	IRF542FI		295
IRF353		IRF350	273	IRF542P	IRF542FI		295
IRF440		SGSP579	589	IRF543	IRF543		295
IRF441		SGSP579	589	IRF543FI	IRF543FI		295
IRF442		SGSP579	589	IRF543P	IRF543FI		295
IRF443		SGSP579	589	IRF610		SGSP317	469
IRF450	IRF450		279	IRF611		SGSP317	469
IRF451	IRF451		279	IRF612		SGSP317	469
IRF452	IRF452		279	IRF613		SGSP317	469
IRF453	IRF453		279	IRF620	IRF620		301
IRF510	IRF510		*	IRF620FI	IRF620FI		301
IRF511	IRF511		*	IRF620P	IRF620FI		301
IRF512	IRF512		*	IRF621	IRF621		301
IRF513	IRF513		*	IRF621FI	IRF621FI		301
IRF520	IRF520		285	IRF621P	IRF621FI		301
IRF520FI	IRF520FI		285	IRF622	IRF622		301
IRF520P	IRF520FI		285	IRF622FI	IRF622FI		301
IRF521	IRF521		285	IRF622P	IRF622FI		301
IRF521FI	IRF521FI		285	IRF623	IRF623		301
IRF521P	IRF521FI		285	IRF623FI	IRF623FI		301
IRF522	IRF522		285	IRF623P	IRF623FI		301
IRF522FI	IRF522FI		285	IRF630		SGSP367	517
IRF522P	IRF522FI		285	IRF631		SGSP367	517
IRF523	IRF523		285	IRF632		SGSP367	517
IRF523FI	IRF523FI		285	IRF633		SGSP367	517
IRF523P	IRF523FI		285	IRF640		SGSP477	553
IRF530	IRF530		291	IRF641		SGSP477	553
IRF530FI	IRF530FI		291	IRF642		SGSP477	553
IRF530P	IRF530FI		291	IRF643		SGSP477	553
IRF531	IRF531		291	IRF720	IRF720		307
IRF531FI	IRF531FI		291	IRF720FI	IRF720FI		307
IRF531P	IRF531FI		291	IRF720P	IRF720FI		307
IRF532	IRF532		291	IRF721	IRF721		307
IRF532FI	IRF532FI		291	IRF721FI	IRF721FI		307
IRF532P	IRF532FI		291	IRF721P	IRF721FI		307
IRF533	IRF533		291	IRF722	IRF722		307
IRF533FI	IRF533FI		291	IRF722FI	IRF722FI		307
IRF533P	IRF533FI		291	IRF722P	IRF722FI		307
IRF540	IRF540		295	IRF723	IRF723		307
IRF540FI	IRF540FI		295	IRF723FI	IRF723FI		307
IRF540P	IRF540FI		295	IRF723P	IRF723FI		307
IRF541	IRF541		295	IRF730	IRF730		313

* Datasheet available on request.

INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE	INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE
IRF730FI	IRF730FI		313	IRF833FI	IRF833FI		331
IRF730P	IRF730FI		313	IRF833P	IRF833FI		331
IRF731	IRF731		313	IRF840	IRF840		337
IRF731FI	IRF731FI		313	IRF840FI	IRF840FI		337
IRF731P	IRF731FI		313	IRF840P	IRF840FI		337
IRF732	IRF732		313	IRF841	IRF841		337
IRF732FI	IRF732FI		313	IRF841FI	IRF841FI		337
IRF732P	IRF732FI		313	IRF841P	IRF841FI		337
IRF733	IRF733		313	IRF842	IRF842		337
IRF733FI	IRF733FI		313	IRF842FI	IRF842FI		337
IRF733P	IRF733FI		313	IRF842P	IRF842FI		337
IRF740	IRF740		319	IRF843	IRF843		337
IRF740FI	IRF740FI		319	IRF843FI	IRF843FI		337
IRF740P	IRF740FI		319	IRF843P	IRF843FI		337
IRF741	IRF741		319	IRFP140	IRFP140		*
IRF741FI	IRF741FI		319	IRFP140FI	IRFP140FI		*
IRF741P	IRF741FI		319	IRFP140P	IRFP140FI		*
IRF742	IRF742		319	IRFP150	IRFP150		343
IRF742FI	IRF742FI		319	IRFP150FI	IRFP150FI		343
IRF742P	IRF742FI		319	IRFP150P	IRFP150FI		343
IRF743	IRF743		319	IRFP151	IRFP151		343
IRF743FI	IRF743FI		319	IRFP151FI	IRFP151FI		343
IRF743P	IRF743FI		319	IRFP151P	IRFP151FI		343
IRF820	IRF820		325	IRFP152	IRFP152		343
IRF820FI	IRF820FI		325	IRFP152FI	IRFP152FI		343
IRF820P	IRF820FI		325	IRFP152P	IRFP152FI		343
IRF821	IRF821		325	IRFP153	IRFP153		343
IRF821FI	IRF821FI		325	IRFP153FI	IRFP153FI		343
IRF821P	IRF821FI		325	IRFP153P	IRFP153FI		343
IRF822	IRF822		325	IRFP350FI	IRFP350FI		349
IFR822FI	IRF822FI		325	IRFP350P	IRFP350FI		349
IRF822P	IRF822FI		325	IRFP450	IRFP450		355
IRF823	IRF823		325	IRFP450FI	IRFP450FI		355
IRF823FI	IRF823FI		325	IRFP450P	IRFP450FI		355
IRF823P	IRF823FI		325	IRFP451	IRFP451		355
IRF830	IRF830		331	IRFP451FI	IRFP451FI		355
IRF830	IRF830		331	IRFP451P	IRFP451FI		355
IRF830P	IRF830FI		331	IRFP452	IRFP452		355
IRF831	IRF831		331	IRFP452FI	IRFP452FI		355
IRF831FI	IRF831FI		331	IRFP452P	IRFP452FI		355
IRF831P	IRF831FI		331	IRFP453	IRFP453		355
IRF832	IRF832		331	IRFP453FI	IRFP453FI		355
IRF832FI	IRF832FI		331	IRFP453P	IRFP453FI		355
IRF832P	IRF832FI		331	IRFZ20	IRFZ20		361
IRF833	IRF833		331	IRFZ20FI	IRFZ20FI		361

* Datasheet available on request.

INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE	INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE
IRFZ20P	IRFZ20FI		361	MTP3N50		IRF832	331
IRFZ22	IRFZ22		361	MTP3N60	MTP3N60		385
IRFZ22FI	IRFZ22FI		361	MTP3N60FI	MTP3N60FI		385
IRFZ22P	IRFZ22FI		361	MTP4N08		SGSP351	499
IRFZ40	IRFZ40		367	MTP4N10		SGSP351	499
IRFZ42	IRFZ42		367	MTP4N18		SGSP317	469
MTH6N60FI	MTH6N60FI		379	MTP4N20		SGSP317	469
MTH7N45		SGSP474	547	MTP4N35		IRF733	313
MTH7N50		SGSP479	559	MTP4N40		IRF732	313
MTH8N35		SGSP475	547	MTP4N45		IRF831	331
MTH8N40		SGSP475	547	MTP4N50		IRF830	331
MTH15N18		SGSP477	583	MTP5N05		SGSP351	499
MTH15N20		SGSP477	583	MTP5N06		SGSP351	499
MTH25N08		SGSP472	541	MTP5N12		IRF620	301
MTH25N10		SGSP471	541	MTP5N15		IRF620	301
MTH35N05		SGSP492	595	MTP5N18		IRF620	301
MTH35N06		SGSP491	595	MTP5N20		IRF620	301
MTH40N06	MTH40N06		379	MTP5N35		IRF731	313
MTH40N06FI	MTH40N06FI		379	MTP5N40		IRF730	313
MTH40N06P	MTH40N06FI		379	MTP6N08		SGSP311	463
MTM7N45		SGSP574	577	MTP6N10		SGSP311	463
MTM7N50		SGSP579	589	MTP6N60	MTP6N60		391
MTM8N35		SGSP575	577	MTP7N05		SGSP358	505
MTM8N40		SGSP575	577	MTP7N12		SGSP317	469
MTM15N18		SGSP577	583	MTP7N15		SGSP317	469
MTM15N20		SGSP577	583	MTP7N18		SGSP317	469
MTM15N35		IRF350	273	MTP7N20		SGSP317	469
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MTM15N50		IRF450	279	MTP8N12		SGSP367	517
MTM20N08		IRF142	261	MTP8N15		SGSP367	517
MTM20N10		IRF142	261	MTP8N18		SGSP367	517
MTM25N05		IRF141	261	MTP8N20		SGSP367	517
MTM25N06		IRF141	261	MTP8N45		IRF841	337
MTM25N08		IRF140	261	MTP8N50		IRF840	337
MTM25N10		IRF140	261	MTP10N05		SGSP322	481
MTM35N05		SGSP592	595	MTP10N06		SGSP321	481
MTM35N06		SGSP591	595	MTP10N08		IRF532	291
MTP2N35		IRF721	307	MTP10N10		IRF532	291
MTP2N40		IRF720	307	MTP10N12		SGSP367	517
MTP2N45		SGSP330	487	MTP10N15		SGSP367	517
MTP2N50		SGSP319	475	MTP10N25		SGSP363	517
MTP3N35		IRF721	307	MTP10N35		IRF741	319
MTP3N40		IRF720	307	MTP10N40		IRF740	319
MTP3N45		SGSP330	487	MTP12N05		SGSP322	481

* Datasheet available on request.

INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE	INDUSTRY STANDARD	SGS-THOMSON	SGS-THOMSON NEAREST	PAGE
MTP12N06		SGSP321	481	RFM12N40		IRF451	279
MTP12N08		SGSP362	511	RFM15N12		SGSP577	583
MTP12N10		SGSP361	511	RFM15N15		SGSP577	583
MTP15N05		SGSP382	529	RFM18N08		IRF142	261
MTP15N05L	MTP15N05L		397	RFM18N10		IRF142	261
MTP15N05LFI	MTP15N05LFI		397	RFM25N05		IRF141	261
MTP15N06		SGSP381	529	RFM25N06		IRF141	261
MTP15N06L	MTP15N06L		397	RFP2N08		SGSP351	499
MTP15N06LFI	MTP15N06LFI		397	RFP2N10		SGSP351	499
MTP20N08		IRF542	295	RFP2N18		SGSP317	469
MTP20N10		IRF542	295	RFP2N20		SGSP317	469
MTP25N05		IRF543	295	RFP3N45		IRF821	325
MTP25N06		IRF543	295	RFP3N50		IRF820	325
MTP25N08		IRF540	295	RFP4N05		SGSP358	505
MTP25N10		IRF540	295	RFP4N35		IRF733	313
MTP3055A	MTP3055A		403	RFP4N40		IRF732	313
MTP3055AFI	MTP3055AFI		403	RFP6N45		IRF831	331
MTP3055AP	MTP3055AFI		403	RFP6N50		IRF830	331
RFH10N45		SGSP474	547	RFP7N35		IRF743	319
RFH10N50		SGSP479	559	RFP7N40		IRF742	319
RFH12N35		IRFP451	355	RFP8N18		SGSP367	517
RFH12N40		IRFP451	355	RFP8N20		SGSP367	517
RFH25N18		SGSP477	553	RFP10N12		SGSP367	517
RFH25N20		SGSP477	553	RFP10N15		SGSP367	517
RFH35N08		IRFP150	343	RFP12N08		SGSP362	511
RFH35N10		IRFP150	343	RFP12N10		SGSP361	511
RFH45N05		SGSP492	571	RFP15N05		SGSP322	481
RFH45N06		SGSP491	571	RFP15N06		SGSP321	481
RFK10N45		SGSP574	577	RFP18N08		IRF542	295
RFK10N50		SGSP579	589	RFP18N10		IRF542	295
RFK12N35		SGSP575	577	RFP25N05		SGSP382	529
RFK12N40		SGSP575	577	RFP25N06		SGSP381	529
RFK25N18		SGSP577	583	SGSP201	SGSP201		433
RFK25N20		SGSP577	583	SGSP202	SGSP201		433
RFK35N08		IRF150	267	SGSP221		SGSP222	439
RFK35N10		IRF150	267	SGSP222	SGSP222		439
RFK45N05		SGSP592	595	SGSP230	SGSP230		445
RFK45N06		SGSP591	595	SGSP231	SGSP230		445
RFM10N12		SGSP577	583	SGSP232	SGSP230		445
RFM10N15		SGSP577	583	SGSP238		SGSP239	451
RFM10N45		SGSP579	589	SGSP239	SGSP239		451
RFM10N50		SGSP579	589	SGSP301	SGSP301		457
RFM12N18		SGSP577	583	SGSP302	SGSP301		457
RFM12N20		SGSP577	583	SGSP311	SGSP311		463
RFM12N35		IRF451	279	SGSP312	SGSP311		463

* Datasheet available on request.

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SGSP316	SGSP316		469	SGSP578		SGSP579	589
SGSP317	SGSP317		469	SGSP579	SGSP579		589
SGSP319	SGSP319		475	SGSP591	SGSP591		595
SGSP321	SGSP321		481	SGSP592	SGSP592		595
SGSP322	SGSP322		481	SGSP3055		MTP3055A	403
SGSP330	SGSP330		487	STHV82	STHV82		601
SGSP331		IRF722	307	STHV102	STHV102		607
SGSP332		IRF723	307	STLT19	STLT19		611
SGSP340		SGSP341	493	STLT19FI	STLT19FI		611
SGSP341	SGSP341		493	STLT20	STLT20		611
SGSP342	SGSP341		493	STLT20FI	STLT20FI		611
SGSP351	SGSP351		499	STVHD90	STVHD90		621
SGSP357		SGSP358	505				
SGSP358	SGSP358		505				
SGSP361	SGSP361		511				
SGSP362	SGSP362		511				
SGSP363	SGSP363		517				
SGSP364	SGSP364		523				
SGSP367	SGSP367		517				
SGSP368		IRF830	331				
SGSP369	SGSP369		523				
SGSP381	SGSP381		529				
SGSP382	SGSP382		529				
SGSP461	SGSP461		535				
SGSP462	SGSP462		535				
SGSP471	SGSP471		541				
SGSP472	SGSP472		541				
SGSP473		SGSP477	553				
SGSP474	SGSP474		547				
SGSP475	SGSP475		547				
SGSP476	SGSP475		547				
SGSP477	SGSP477		553				
SGSP478		SGSP479	559				
SGSP479	SGSP479		559				
SGSP481	SGSP481		565				
SGSP482	SGSP482		565				
SGSP491	SGSP491		571				
SGSP492	SGSP492		571				
SGSP571		IRF152	267				
SGSP572		IRF150	267				
SGSP573		SGSP577	583				
SGSP574	SGSP574		577				
SGSP575	SGSP575		577				
SGSP576	SGSP575		577				
SGSP577	SGSP577		583				

* Datasheet available on request.

C_{DB}	Parasitic capacitance between drain and body
C_{DS}	Parasitic capacitance between drain and source
C_{GD}	Parasitic capacitance between gate and drain
C_{GS}	Parasitic capacitance between gate and source
C_{iss}	Input capacitance
C_{oss}	Output capacitance
C_{rss}	Reverse transfer capacitance
D.U.T.	Device under test
I_D	Drain current
I_{DLM}	Drain peak current, inductive
I_{DM}	Drain peak current
I_{DSS}	Zero gate voltage drain current
I_G	Gate current
I_{GSS}	Gate-body leakage with drain short circuited to source
I_{SD}	Source-drain diode current
I_{SDM}	Source-drain diode peak current
I_{UIS}	Unclamped inductive switching current
L	Load inductance of a specified circuit
PW	Pulse width
P_{tot}	Total power dissipation
$R_{DS\ (on)}$	Static drain-source on resistance
R_i	Generator internal resistance
R_L	Load resistance of a specified circuit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient
$R_{th\ j\text{-}case}$	Thermal resistance junction-case
T_l	Maximum lead temperature for soldering purpose
T_{amb}	Ambient temperature
T_{case}	Case temperature
T_j	Junction temperature
T_{stg}	Storage temperature
$V_{(BR)\ DSS}$	Drain-source breakdown voltage
V_{DG}	Drain-gate voltage
V_{DGR}	Drain-gate voltage with specified resistance between gate and source
V_{DS}	Drain-source voltage
$V_{DS\ (on)}$	Drain-source on state voltage

ALPHABETICAL LIST OF SYMBOLS

V_{GS}	Gate-source-voltage
$V_{GS\ (th)}$	Gate threshold voltage
V_{SD}	Source-drain diode forward on voltage
V_{clamp}	Drain clamping voltage
V_i	Input voltage of a specified circuit
f	Frequency
g_{fs}	Forward trasconductance
$t_{d\ (off)}$	Turn-off delay time
$t_{d\ (on)}$	Turn-on delay time
t_f	Fall time
t_{on}	Turn-on time
t_r	Rise time
t_{rr}	Reverse recovery time

A. DEFINITIONS OF TERMS USED

a. **Electronic device.** An electronic tube or valve, transistor or other semiconductor device. Note: This definition excludes inductors, capacitors, resistors and similar components.

b. **Characteristic.** A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

c. **Bogey electronic device.** An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

d. **Rating.** A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determinate for specified values of environment and operation, and may be stated in any suitable terms.
Note: Limiting conditions may be either maxima or minima.

e. **Rating system.** The set of principles upon which ratings are established and which determines their interpretation.
Note: The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

B. ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.
These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristcs of the device under consideration and of all other electronic devices in the equipment.
The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variation in characteristics of the device under consideration and of all other electronic devices in the equipment.

C. DESIGN - MAXIMUM RATING SYSTEM

Design-maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.
These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.
The equipment manufacturer should design so that, initially and throughout life, no design-maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply-voltage variation equipment, component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

D. DESIGN - CENTRE RATING SYSTEM

Design-centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.
These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibilty for normal changes in operating conditions due to rated supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.
The equipment manufacturer should design so that, initially, no design-centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply-voltage.

The Absolute Maximum Rating System is commonly used for semiconductor devices.

PRECAUTIONS FOR PHYSICAL HANDLING OF POWER PLASTIC TRANSISTOR [TO-220, ISOWATT220, TO-218 (SOT-93), ISOWATT218, TO-126 (SOT-32), SOT-82, SOT-194]

When mounting power transistors certain precautions must be taken in operations such as bending of leads, mounting of heatsink, soldering and removal of flux residue. If these operations are not carried out correctly, the device can be damaged or reliability compromised.

1. Bending and cutting leads

The bending or cutting of the leads requires the following precautions:

1.1. When bending the leads they must be clamped tightly between the package and the bending point to avoid strain on the package (in particular in the area where the leads enter the resin) (fig. 1). This also applies to cutting the leads (fig. 2).

1.2. The leads must be bent at a minimum distance of 3 mm from the package (fig. 3a).

1.3. The leads should not be bent at an angle of more than 90° and they must be bent only once (fig. 3b).

1.4. The leads must never be bent laterally (fig. 3c).

1.5. Check that the tool used to cut or form the leads does not damage them or ruin their surface finish.

2. Mounting on printed circuit

During mounting operations be careful not to apply stress to the power transistor.

2.1. Adhere strictly to the pin spacing of the transistor to avoid forcing the leads.

2.2. Leave a suitable space between printed circuit and transistor, if necessary use a spacer.

2.3. When fixing the device to the printed circuit do not put mechanical stress on the transistor. For this purpose the device should be soldered to the printed circuit board after the transistor has been fixed to the heatsink and the heatsink to the printed circuit board.

Fig. 1 - Bending the leads

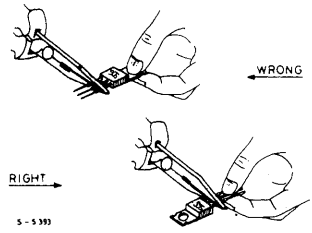


Fig. 2 - Lead forming or cutting mechanism

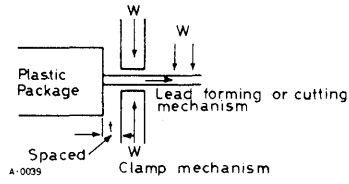
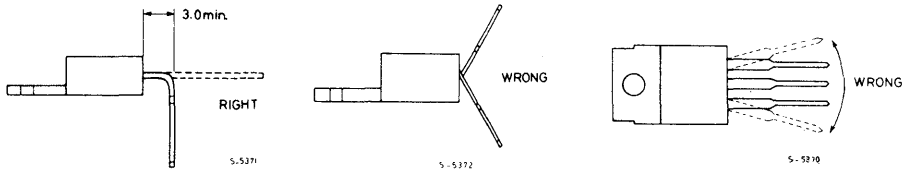


Fig. 3 - Angles for lead wire bending



a *b* *c*

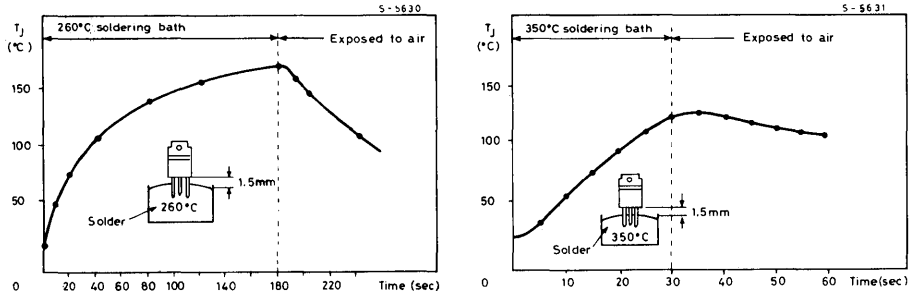
3. Soldering

In general a transistor should never be exposed to high temperature for any length of time. It is therefore preferable to use soldering methods where the transistor is exposed to the lowest possible temperatures for a short time.

3.1. Tolerable conditions are 260°C for 10 sec or 350° for 3 sec. The graphs in fig. 4 give an idea of the excess junction temperature during the soldering process for a TO-220 (Versawatt). It is also important to use suitable fixes for the tin baths to avoid deterioration of the leads or of the package resin.

3.2. An excess of residual flux between the pins of the transistor or in contact with the resin can reduce the long-term reliability of the device. The solvent for removing excess flux must be chosen with care. The use of solvents derived from trichloroethylene is not recommended on plastic packages because the residue can cause corrosion.

Fig. 4 - Junction temperatures during soldering



4. Mounting at heatsink

To exploit best the performance of power transistor a heatsink with R_{th} suitable for the power that the transistor will dissipate must be used.

4.1. The plastic packages used by SGS-THOMSON for its power transistor (SOT-32, SOT-82, SOT-194, TO-220, ISOWATT220, TO-218, ISOWATT218) provide for the use of a single screw to fix the package to the heatsink. A compression spring (clip) can be sufficient as an alternative (fig. 5).

The screw should be properly tightened to ensure good contact between the back of the package and the heatsink but should not be too tight to avoid deformation of the copper part (tab) of the package causing breaking of the die or separation of the resin from the tab.

4.2. The contact R_{th} between device and heatsink can be improved by inserting a thin layer of silicone grease with fluidity sufficient to guarantee perfectly uniform distribution on the surface of the tab. The thermal resistance with and without silicone grease is given in fig. 6. An excessively thick layer or an excessive viscosity of the grease can degrade the R_{th}.

Fig. 5 - SOT-93 mounting examples

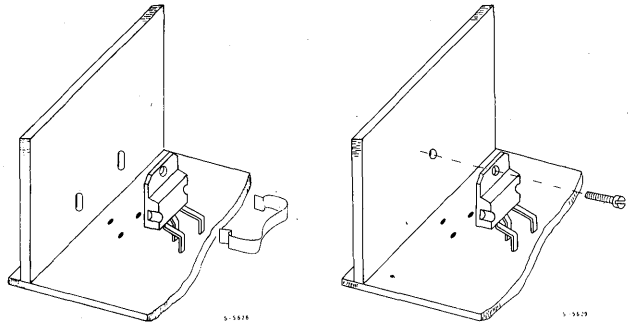
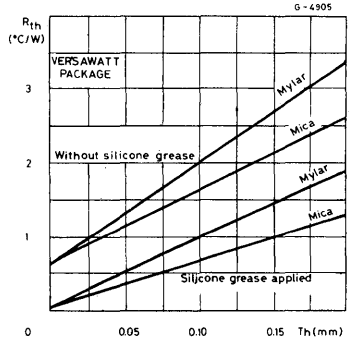


Fig. 6 - Contact thermal resistance vs. insulator thickness.



5. Heatsink problems

The most important aspect from the point of view of reliability of a power transistor is that the heatsink should be dimensioned to keep the T_j of the device as low as possible. From the mechanical point of view, however, the heatsink must be realized so that it does not damage the device.

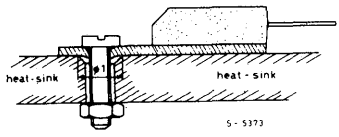
5.1. The planarity of the contact surface between device and heatsink must be $<25\mu m$ for TO-220, ISOWATT220, TO-218, ISOWATT218, TO-126 (SOT-32), SOT-82, SOT-194.

5.2. If self threading screws are used there must be an outlet for the material that is deformed during formation of the thread. The diameter ∅ 1 (fig. 7) must be large enough to avoid distortion of the tab during tightening. For this purpose it may be useful to insert a washer or use of the type shown in fig. 8 where the pressure on the tab is distributed on a much larger surface. Sometimes when the hole in the heatsink is formed with a punch, around the hole or hollow there may be a ring which is lower than the heatsink surface.
This is dangerous because it may lead to distortion of the tab as mentioned before.

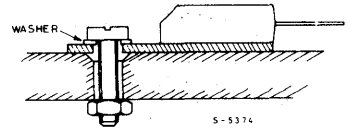
5.3. A very serious problem is that of the rigidity between heatsink, device and printed circuit board. Once the device and the heatsink are mechanically connected, and the heatsink is fixed to the apparatus frame, the device and the PCB are bound together by the leads of the devices. A solution of this type is extremely dangerous.

Fig. 8 - Suggested screw

Fig. 7 - Device mounting

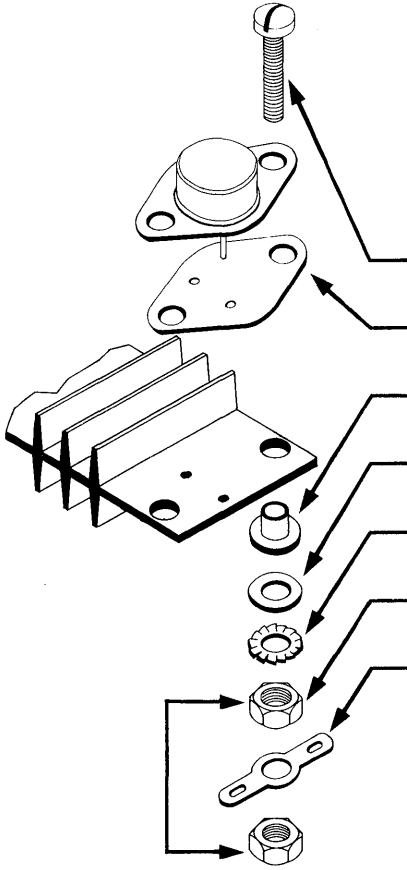


WRONG



RIGHT

TO-3

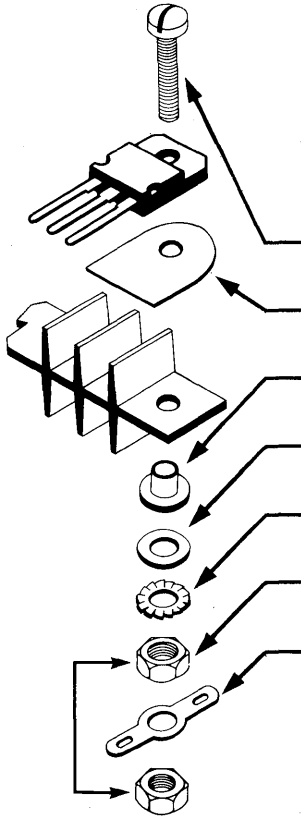


ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREWS SLOTTED	2	NOT AVAILABLE FROM SGS-THOMSON		
MICA WASHER	1	CDA 3126 A*	MICA	46
INSULATING BUSHES	2	CDA 3155 A	NYLON	47
WASHERS	2	NOT AVAILABLE FROM SGS-THOMSON		
LOCK WASHERS	2	NOT AVAILABLE FROM SGS-THOMSON		
HEXAGON NUTS	4	NOT AVAILABLE FROM SGS-THOMSON		
SOLDER LUG	1	NOT AVAILABLE FROM SGS-THOMSON		

CDA 3126 B FOR MODIFIED TO-3

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 1 Nm.

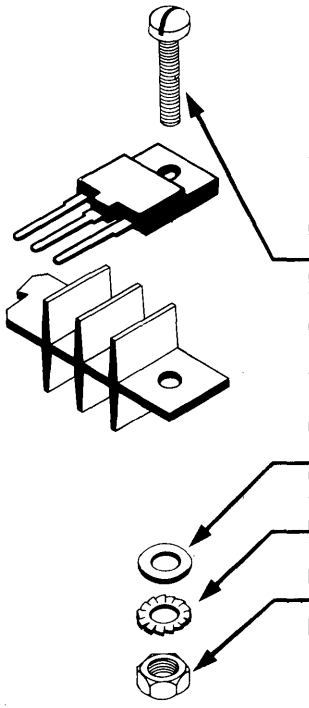
TO-218 (SOT-93)



ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS-THOMSON		
MICA WASHER	1	CDA 3154	MICA	47
INSULATING BUSHES	1	CDA 3155 C	NYLON	47
WASHERS	1	NOT AVAILABLE FROM SGS-THOMSON		
LOCK WASHERS	1	NOT AVAILABLE FROM SGS-THOMSON		
HEXAGON NUTS	2	NOT AVAILABLE FROM SGS-THOMSON		
SOLDER LUG	1	NOT AVAILABLE FROM SGS-THOMSON		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 1 Nm.

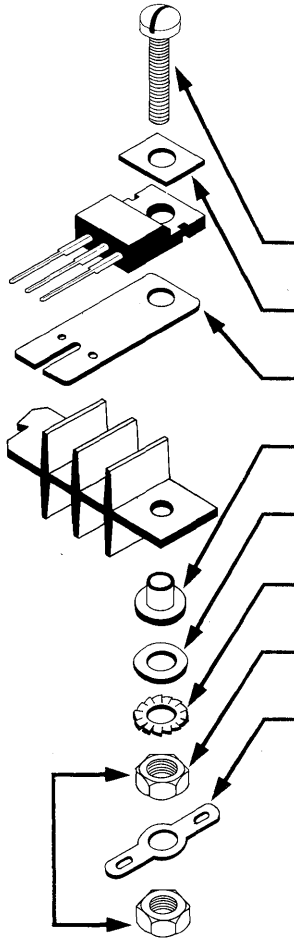
ISOWATT218



ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS-THOMSON		
WASHERS	1	NOT AVAILABLE FROM SGS-THOMSON		
LOCK WASHERS	1	NOT AVAILABLE FROM SGS-THOMSON		
HEXAGON NUTS	1	NOT AVAILABLE FROM SGS-THOMSON		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 1 Nm.

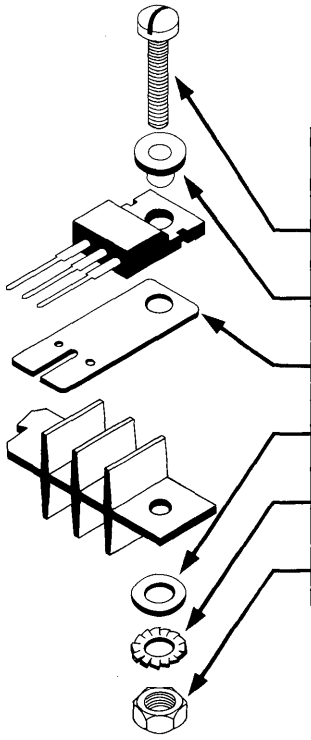
TO-220



ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS-THOMSON		
RECTANGULAR WASHER	1	CDA 3163		48
MICA WASHER	1	CDA 3159	MICA	48
INSULATING BUSHES	1	CDA 3155 B	NYLON	47
WASHER	1	NOT AVAILABLE FROM SGS-THOMSON		
LOCK WASHER	1	NOT AVAILABLE FROM SGS-THOMSON		
HEXAGON NUTS	2	NOT AVAILABLE FROM SGS-THOMSON		
SOLDER LUG	1	NOT AVAILABLE FROM SGS-THOMSON		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 0.7 Nm.

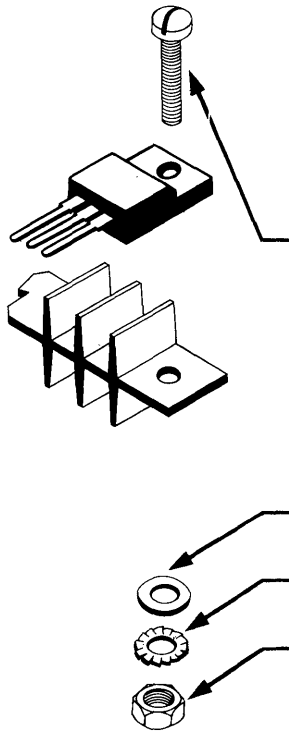
TO-220



ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS-THOMSON		
INSULATING BUSHES	1	CDA 3155 B	NYLON	47
MICA WASHER	1	CDA 3159	MICA	48
WASHER	1	NOT AVAILABLE FROM SGS-THOMSON		
LOCK WASHER	1	NOT AVAILABLE FROM SGS-THOMSON		
HEXAGON NUTS	1	NOT AVAILABLE FROM SGS-THOMSON		

Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 0.7 Nm.

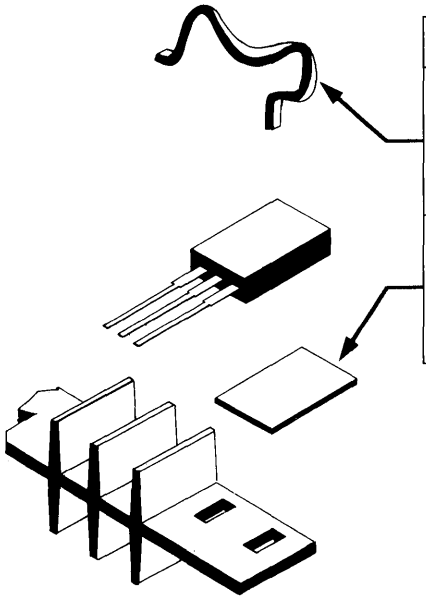
ISOWATT220



ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA Page
CHEESE HEAD SCREWS SLOTTED	1	NOT AVAILABLE FROM SGS-THOMSON		
WASHER	1	NOT AVAILABLE FROM SGS-THOMSON		
LOCK WASHER	1	NOT AVAILABLE FROM SGS-THOMSON		
HEXAGON NUTS	1	NOT AVAILABLE FROM SGS-THOMSON		

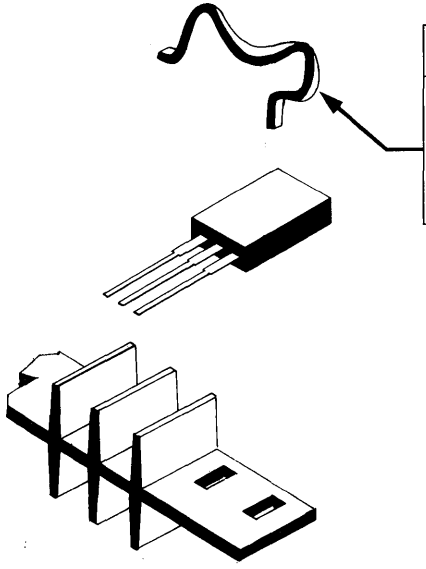
Maximum torque (applied to mounting flange)
Recommended: 0.55 Nm
Maximum: 0.7 Nm.

TO-126, SOT-82, SOT-194, TO-220, TO-218



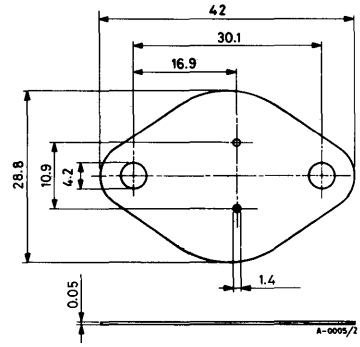
ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA
SPRING CLIP	1	NOT AVAILABLE FROM SGS-THOMSON		
MICA WASHER	1	TO-126, SOT-82, SOT-194: NOT AVAILABLE FROM SGS-THOMSON TO-220: CDA3159 TO-218: CDA3154	MICA	 48 47

ISOWATT220, ISOWATT218

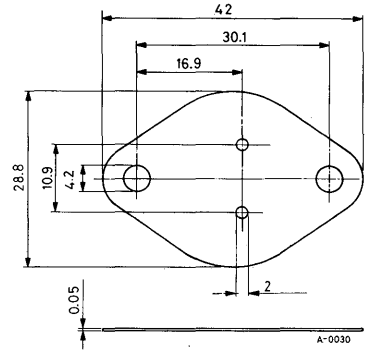


ACCESSORY TYPE	Q.ty	ASSEMBLY NUMBER	MATERIAL	MECH. DATA
SPRING CLIP	1	NOT AVAILABLE FROM SGS-THOMSON		

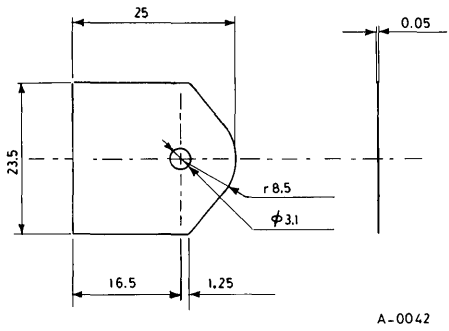
CDA 3126A



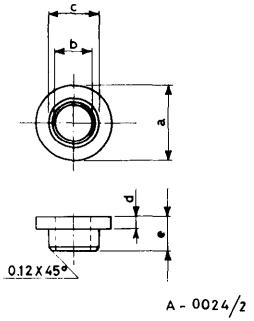
CDA 3126B



CDA 3154



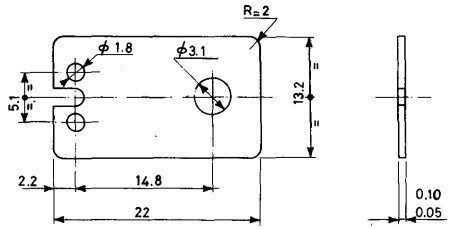
CDA 3155



Suffix	Package	a	b	c	d	e
A	TO-3	6.40 to 6.60	3.00 to 3.10	4.00 to 4.05	1.1 max	1.55 to 1.65
B	TO-220	5.30 to 5.50	3.00 to 3.10	3.83 to 3.88	0.60 to 0.65	1.70 to 1.80
C	SOT-93	6.40 to 6.60	3.00 to 3.10	4.00 to 4.05	1.3 to 1.4	2.7 to 2.9

Material: Nylon Dimensions: mm

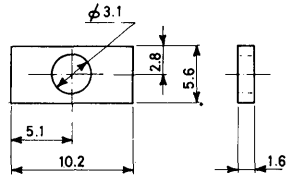
CDA 3159



A-0026/3

TYPE	MATERIAL	NOTE
CDA3159	MICA	

CDA 3163



A-0023/3

TYPE	MATERIAL	NOTE
CDA3163	Steel nickel plated	

Electronic components have to be protected from the hazard of static electricity, from the manufacturing stage down to where they are utilized.

MOS devices are typically voltage and electrical field sensitive; the thin oxide layers can be destroyed by an electric field.

Fig. 1

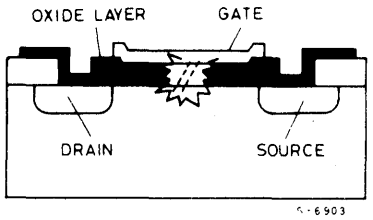
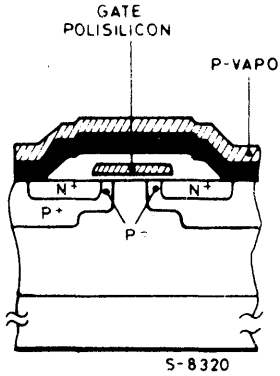


Fig. 2



This happens mostly because a charged conductor, typically a person, is rapidly discharged through the device.

There will be no net charge on any portion of the MOS structure when the induced high field exceeds the breakdown voltage of the MOS capacitor we may have a self-healing break-down, degradation or catastrophic failure.

The failure hazard is not limited to the gate region but it could occur wherever two conductive areas are separated by a thin insulator.

POWER MOS devices can generally be considered less ESD sensitive than MOS I/Cs.

The input capacitance of a POWER MOS device is typically 10 to 200 times larger, and the gate oxide thickness is similar in size to that of the largest MOS I/Cs used.

As a result, it is common practice not to consider the ESD as dangerous for POWER MOS, but this is not alway true, even though they are less sensitive than MOS I/Cs

HANDLING

SGS-THOMSON has chosen a no-compromise strategy in the MOS ESD protection. From the wafer level to the shipping of finished units, each work station and processing of the parts is guaranteed. This is achieved through total adoption of shielding and grounding media. Our final shipping of the parts is performed in antistatic tubes, bags or boxes. The suppliers greatest efforts are in vain if the end user does not provide the same level of protection and care in application.

Here are the basic static control protection rules:

A - Handle all components in a static-safe work area.

B - Transport all components in static shielding containers.

To comply with the rules the following procedures must be set up.

1 - Static control wrist strap (from a qualified source) used and connected properly.

2 - Each table top must be protected with a conductive mat, properly grounded.

3 - Extensive use of conductive floor mats.

4 - Static control shoe straps, wearing typically insulating footwear, such as with crepe or thick rubber soles.

5 - Ionized air blowers are a necessary part of the protective system, to neutralize static charges on conductive items.

6 - Use only the grounded tip variety of soldering iron.

7 - Single components, tubes, printed circuit cards should always be contained in static shielding bags; keep our parts in the original bags up to the very last moment on the production line.

8 - If bigger containers (tote box) are used for in-plant transport of devices or PC boards they must be electrically conductive, like the carbon loaded ones.

9 - All tools, persons, testing machines, which could contact device leads must be conductive and grounded.

10 - Avoid using high dielectric materials (like polystyrene) for sub-assembly construction, storing and transportation.

11 - Follow a proper power supply sequence in testing and application. Supply voltage should be applied before and removed after input signals; insertion and removal from sockets should be done with no power applied.

12 - Filtration, noise suppression, slow voltage surges should be guaranteed on the supply lines.

13 - Any open (floating) input pin is a potential hazard to your circuit: ground or short them to V_{DD} whenever possible.

TECHNICAL NOTES

AN INTRODUCTION TO POWER MOS

A POWER MOS transistor is a power transistor produced with MOS, and not the usual bipolar technology.

Special characteristics are high switching speeds and easy driving. This introductory note describes the essential points of the MOS structure when used for power devices.

WHAT DOES MOS MEAN?

It means that the essential part (the silicon chip) of the device is made up of three layers:

- one conductive layer (M for metal) that is the control (drive) electrode
- one isolating layer (O for oxide) that prevents any current flow from the drive electrode to the other two electrodes, but does not block the electric field
- one semiconductor layer (S for semiconductor) which switches on or off depending on the electrical field imposed on it by the control electrode through the opening in the P zone of a conductive channel between the two zones.

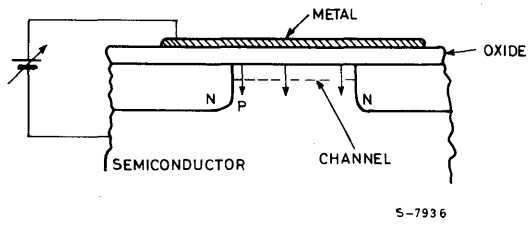
WHAT DOES POWER MOS MEAN?

Fig. 1 shows that the device is totally implemented on the chip surface. In other words both the on and off states are implemented in a horizontal plane:

- the ON STATE i.e. the residual resistance when in the on state corresponds to conduction on the top surface of the silicon
- the OFF STATE i.e. the depletion region of one of the two PN junctions, with its resistivity and length, gives the device its voltage rating.

With the present technology the "on the surface" approach allows the production of MOS transistors that can handle tens of volts and milliamperes (as in MOS microprocessors or in MOS memories). A power transistor must be able to handle no less than a few amperes at voltages of 50-100V or higher. The approach of several devices "on the surface" connected in parallel is unsuitable due to problems of excessive connections, as each cell would have three terminals.

Fig. 1 - MOS basic structure



The best solution is to exploit the semiconductor both vertically as well horizontally. The paralleling of one of the two N doped regions of all the elementary structures in parallel occurs on the bottom face of the semiconductor.

At the same time, the PN junction that implements the off performance (its length corresponds to the voltage rating of the device) can be positioned vertically, and so avoiding the waste of horizontal space. the channel must be short (1 to 2 microns) to obtain characteristics of practical interest.

As a result, the POWER MOS device consists of multi - MOS basic cells, with all the N^+ type SOURCE zones connected in parallel on the top side of the semiconductor chip, as are the cell GATES. The common substrate of the chip forms the DRAIN.

THE POSSIBLE STRUCTURES

Figures 2, 3 and 4 show the chronological progression of the different solutions used in the industry to implement the elementary POWER MOS structures.

The P doped semiconductor area that appears on the surface of the semiconductor in front of the metal electrode is the channel. There is an N^-.

Fig. 2 - V-Groove structure

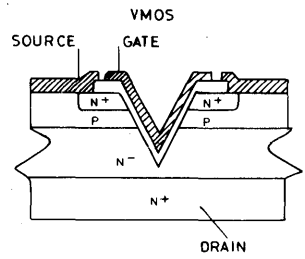


Fig. 3 - U-Groove structure

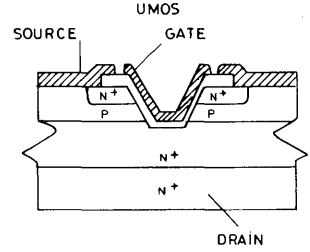


Fig. 4 - D-MOS structure

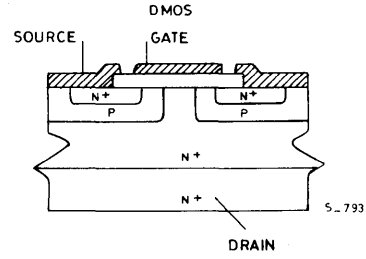
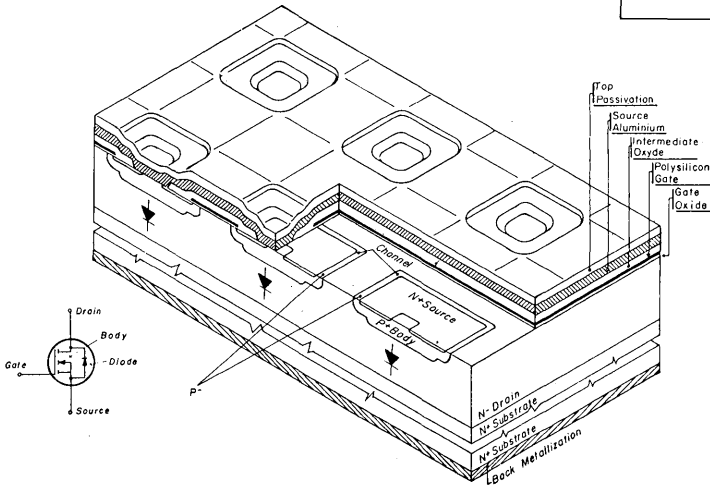


Fig. 5 - POWER MOS cell structure



layer with low doping (high resistivity) on one side of the channel. This N layer becomes depleted when the voltage is applied to the device, and consequently allows the device to sustain applied voltages without reaching too high an electric field at any point of the chip.

Reaching the critical field means reaching the point of voltage breakdown (primary breakdown).

"V" and "U" type structures have been abandoned because the production process is both difficult and critical. Nowadays practically all POWER MOS are of the D type as shown in Fig. 4, D as a prefix means that the channel is produced by diffusion.

All the devices have in common the fact that the current traverses the device vertically, as a consequence two electrodes appear on the surface:
- SOURCE
- GATE

and one electrode appears on the bottom:
- DRAIN

Fig. 5 shows the actual structure of an POWER MOS in an expanded view of a piece of the chip. All the important elements can be located in the figure.

EVOLUTION OF POWER MOS TRANSISTORS

The vertical double diffused MOS silicon gate technology represents the final evolution of the development of a process to obtain POWER MOS devices, started in SGS in 1977.

The principal steps of this development have passed through the study of these structures (fig. 1);

1) V groove MOS
2) U groove MOS
3) Double diffused MOS metal gate
4) Double diffused MOS silicon gate

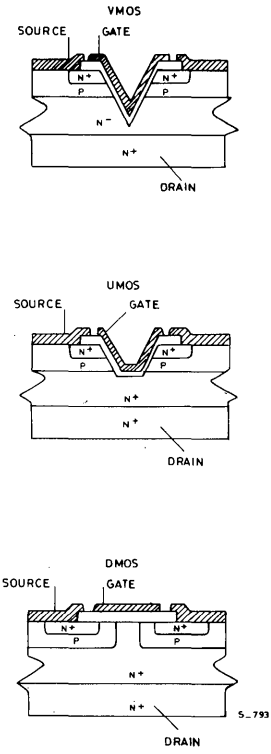
Nowadays the VDMOS silicon gate structure is used while the other three structure have become obsolete.

All these structures have as a common point the fact that the current flows through a vertical path like bipolar power devices and, as a consequence the devices have two electrodes on the top (gate and source) and one on the bottom (drain) in electrical and thermal contact with the header.

Another common point is the fact that the starting material is made of an epitaxial lightly N^- doped layer grown on a heavily N^+ doped substrate (for N-channel devices).

The N^- region largely supports the applied drain potential because its doping level is much smaller than the P^- body region.

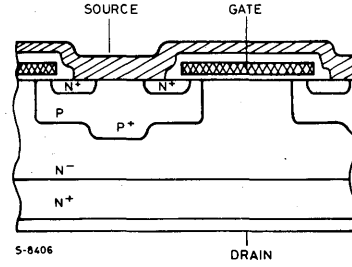
Fig. 1 - Evolution of POWER MOS devices



VDMOS SILICON GATE

STRUCTURE

In the VDMOS silicon gate structure the best features of earlier technologies and design are combined with new fabrication techniques to achieve much better performance. The VDMOS silicon gate structure needs a more sophisticated technology, very similar to that of the VLSI.



VDMOS (fig. 2) is a two level structure where the lower level is the gate made of doped polycrystalline silicon and the upper level is the source metallization.

It is a self aligned structure since the polysilicon holes are the mask for the P^- well and N^+ source diffusion.

In this way MOS channel regions are obtained by difference in lateral diffusion of the two impurity distributions. The use of double diffusion achieves very short channels ($\leqslant 1.5\mu$).

With the VDMOS silicon gate structure the resulting increase in packing density directly reduces the cost and improves the performance of the device. In fact the use of a polycrystalline gate reduces the possibility of sodium ion contamination in the gate oxide (with high stability of threshold voltage $V_{GS(th)}$). Also the full surface source metallization allows a better heat dissipation.

Fig. 2a - VDMOS structure

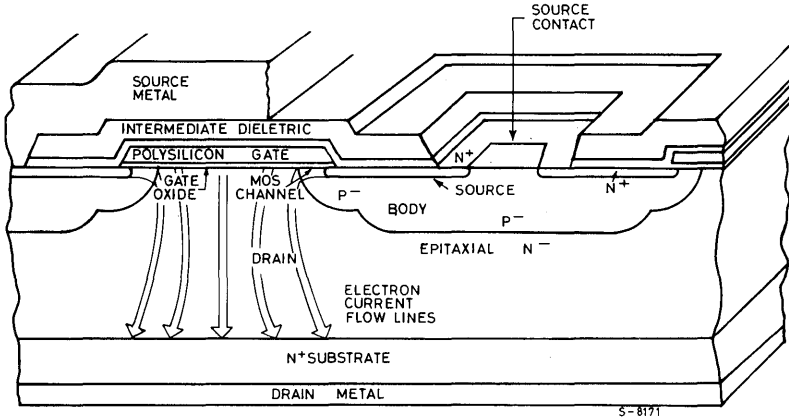
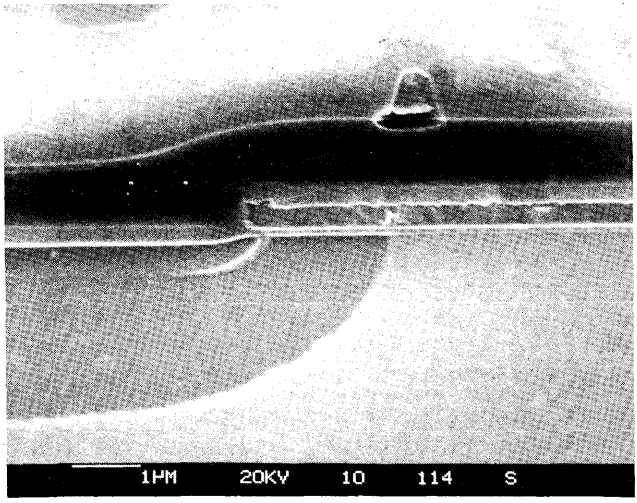


Fig. 2b - SEM microphoto of the VDMOS structure



L (channel)	≅	1.75μ
t (gate ex)	≅	830 Å
t (gate poly)	≅	3330 Å
t (ox→poly-As)	≅	2500 Å
t (p-vapox)	≅	9580 Å
x_j (source)	≅	0.50 μ
x_j (body)	≅	2.58 μ

HOW IT WORKS

The structure is switched on by applying a voltage between the drain and the source and positively biasing the gate (for a N-channel device) with respect to the source. This biasing creates an electric field in the channel region which reverses the polarity of the material in the body region to create a majority carrier path from the source to the drain. Electron current flows from the source metal to the source contact, laterally through the channel and then vertically through the drain and substrate to the drain metal.

The body source together with the drain creates an internal parasitic diode in inverse parallel connection. This diode conducts when the source is positive with respect to the drain and it can handle forward current equal to the drain current rating (fig. 3).

Fig. 3 - Schematic representation of POWER MOS structure

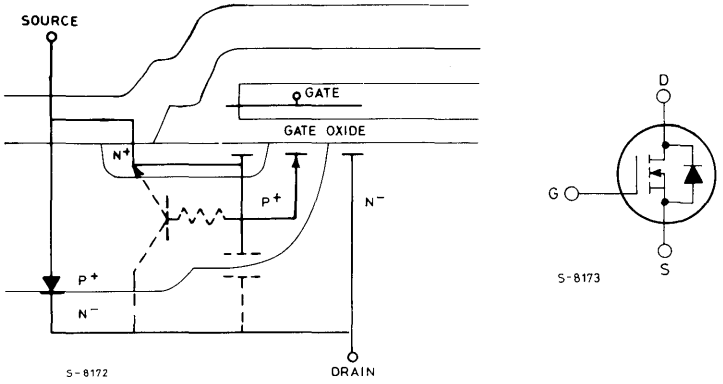
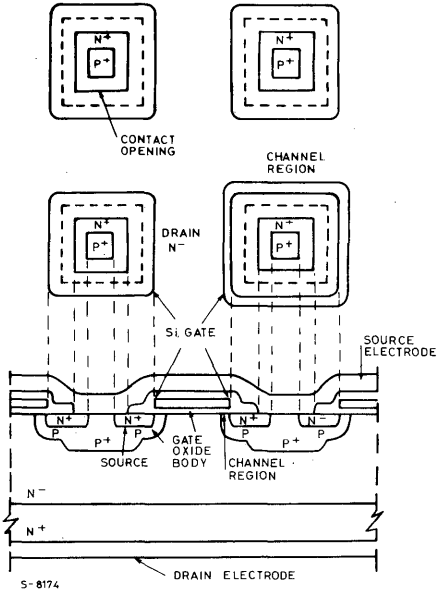


Fig. 4 - Horizontal layout and vertical structure



DESIGN OF POWER MOS

In the design of a POWER MOS transistor the parameters of interest are the device on resistance $R_{DS(on)}$, for a given chip area and the breakdown voltage.

ON RESISTANCE

The vertical power DMOS consists of a large number of cells inteconnected in parallel on a single die (fig. 4).

$R_{DS(on)}$ parameter is strictly dependent on the topological layout, that is the shape and size of the cells and the packing density.

In order to optimize this parameter, a comparison between different geometrical solutions at both low and high voltages was made.

If the behaviour of the $R_{DS(on)}$ components is analysed (fig. 5) it can be seen that for low voltage applications the channel has a greater effect in determining the $R_{DS(on)}$ value. To optmize the $R_{DS(on)}$ it is necessary to maxmize the POWER MOS channel perimeter per unit area with a high packing density. Low voltage devices have a packing density of about 550 K per square inch.

For high voltage devices the epitaxial layer resistance has a greater effect than the overall on resistance (fig. 6). To optimize $R_{DS(on)}$ it is necessary to minimize bulk resistance choosing a low packing density layout which increases the area of the epitaxial drift region. High voltage devices have a packing density of about 280.000 cells per square inch (fig. 7).

Fig. 5 - Low voltage case

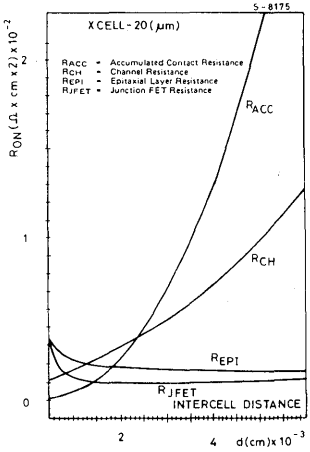


Fig. 6 - High voltage case

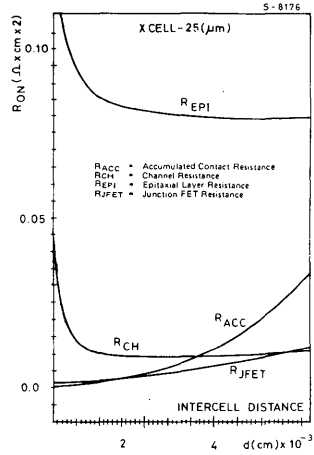
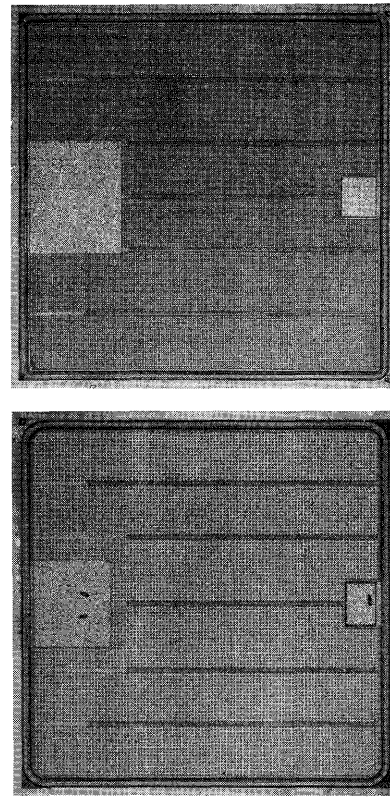


Fig. 7 - a- (100V) b- (400V)



a)

b)

BREAKDOWN VOLTAGE $V_{(BR)DSS}$

The ideal breakdown voltage is bulk avalanche breakdown which corresponds to a minimum epitaxial bulk resistance requirement.

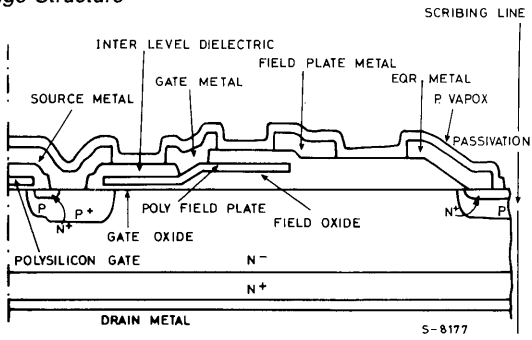
At high voltages however, the maximum drain potential is limited by junction edge breakdown below the ideal value. This is due to the effects of curvature and surface electrical field crowding.

Therefore to meet a certain breakdown requirement the epitaxial layer doping must exceed that specified by the minimum epitaxial bulk resistance requirement and this will increase the device on resistance.

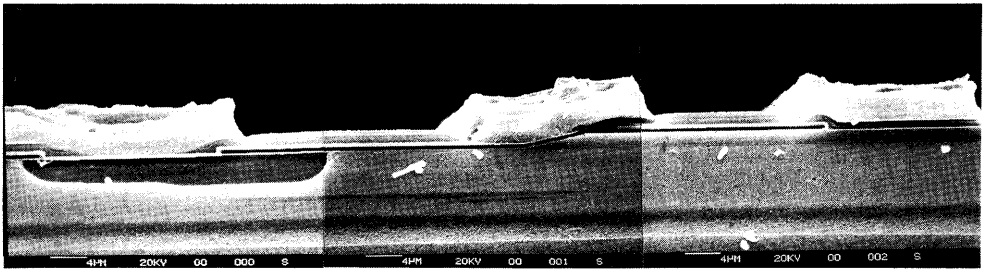
To reduce the surface electrical field and thus reach the bulk breakdown voltage, an edge structure has been developed.

This edge termination contains a field plate surrounding the silicon dioxide of three increasing thicknesses forming a triplanar structure (fig. 8).

Fig. 8 POWER MOS Edge Structure



A SEM microphoto of the POWER MOS Edge Termination



The field plate allows higher breakdown voltages by spreading the field laterally along the surface of the device.

Gradual increase of the oxide thickness at a very low angle (10 degrees to 15 degrees) from the gate oxide to the field oxide allows distribution of the voltage so that the electrical field is as uniform as possible along the surface and is below the critical electrical field (fig. 9).

This edge termination has been implemented in POWER MOS allowing breakdown voltages up to 600V with stable characteristics. A new edge termination structure allows a $V_{(BR)DSS}$ of up to 1000V.

THRESHOLD VOLTAGE

The value of the threshold voltage is related to the thickness of the gate oxide and to N_A, maximum peak impurity concentration in the laterally diffused body in the region between the source and the drain (fig. 10).

Channel punch-through can occur as the result of insufficient impurity charge in the channel, under strong reverse bias. To avoid punch through a trade off between $V_{GS\,(th)}$ and length must be made.

For a fixed gate oxide thickness a shorter channel length implies a greater N_A maximum peak and a higher $V_{GS(th)}$. However, a lower $V_{GS(th)}$ sets a lo-

wer limit to the channel length in relation to the punch through problem.

Due to the negative temperature coefficient of $V_{GS(th)}$ its value cannot be too low. Also, if it is too high, the devices cannot be driven directly by low voltage logic circuits.

Consequently the value of $V_{GS(th)}$ is in the range from 2 to 4V with an oxide thickness of 850 Å.

Fig. 9 - Computer simulation of the equipotential lines of the Edge of a high voltage POWER MOS device

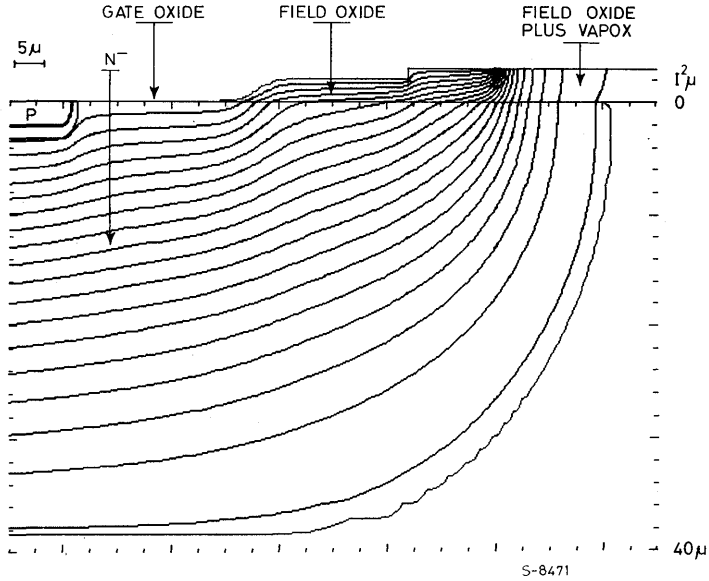
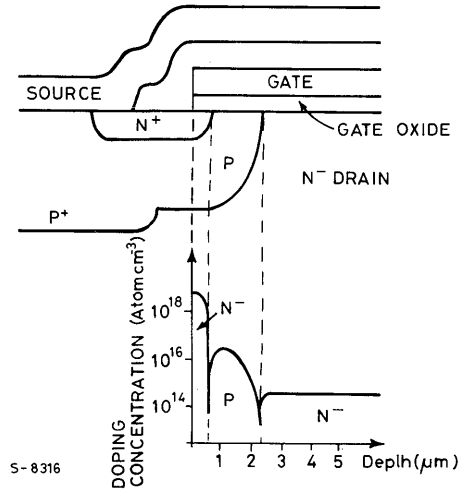


Fig. 10



POWER MOS IN SWITCHING AN EVALUATION METHOD AND A PRACTICAL EXAMPLE

INTRODUCTION

POWER MOS are used in switch mode power supplies. H.F. welding systems, industrial ovens, relay drivers and other similar applications. These diverse applications of POWER MOS in the field of control is due largely to their ability to handle high power at very high switching speeds up to hundreds of kHz.

The great improvement in the ability to switch power using POWER MOS is due to the recent progress made in the manufacture and technology of semiconductors. This ability to produce power devices using MOS technology has opened up new fields of applications. In POWER MOS devices the flow of current from the drain to the source is voltage controlled. Consequently the energy consumed in driving the device is much less than for a bipolar device. POWER MOS devices are unipolar and do not make use of minority carriers for conduction. This makes them very attractive to use in power switching at very high frequencies.

SWITCHING PHASE

In practical working conditions three main phases can be distingushed:

On state

When the device is on and the channel open, the dissipated power is:

$P_{(on)} = V_{DS\ (on)} \times I_D$

$P_{(on)} = V_{CE\ (sat)} \times I_C$ for bipolar transistors

It can be reduced optimising the technology (metal back, epitaxial thickness) and the design (cell dimensions and layout).

Off state

When the devices is off and the drain is at the supply voltage, the power dissipation is:

$P_{off} = V_{DD} \times I_{DSS}$

$P_{off} = V_{CC} \times I_{CEX}$ for bipolar transistors

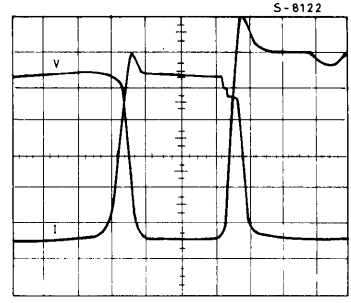
"TRANSITIONS"

During switching the dissipated power instant by instant is:

$$P = V_{DS} \times I_D$$

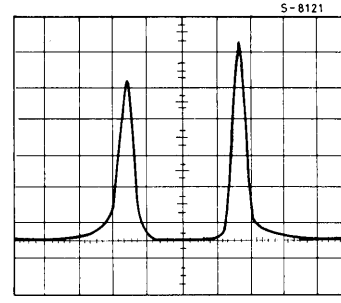
and depends on the on/off switching speed of the device as can can be seen in Figs. 1 and 2.

Flg. 1 - I/V waveforms



t: 100 ns/div, V: 45V/div, I: 1.2A/div, Vg = 10V, Rg = 25Ω

Fig. 2 - Power dissipation waveforms.



t: 100 ns/div, P: 200W/div, Vg = 10V, Rg = 25Ω.

Q. THE EFFICIENCY FACTOR

The performance of POWER MOS device can therefore be rated as the ratio between the total power in switching-on and off and the energy dissipated per cycle. It can be expressed as:

$$Q = \frac{P_t}{E_{on} + E_{off} + E_p}$$

Where:

E_{on} -is the energy lost in the turning-on and on phases

E_{off} -is the energy lost in the turning-off and off phases

E_p - is the energy lost in driving the circuit.

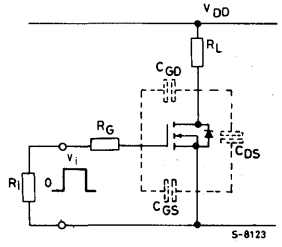
The quantity Q is a frequency and is an index of the maximum frequency at which the device can most efficiently operate, considering P_t as the maximum power that the device can dissipate in practical working conditions.

To fully understand this equation a brief analysis of switching phenomena is essential. As previously mentioned, POWER MOS do not make use of minority carriers for conduction. The recombination of these minority carriers is a switching speed limitation. In POWER MOS devices the majority carrier flow is simply controlled by the gate voltage and therefore its switching speed is limited only by the time needed to charge and discharge the parasitic input capacitances. Consequently the switching behaviour is a function only of the ability of the driving circuit to charge and discharge some hundreds of picofarads. This is why POWER MOS can switch so fast - in the range of tens of nanoseconds.

INPUT

POWER MOS devices behave quite differently from bipolar power devices, as far as the driving energy is concerned. POWER MOS require driving power during the charge and the discharge phases of the input capacitances. Fig. 3 shows a POWER MOS driven by a voltage generator with an internal resistance R_i and an open circuit voltage V_i, where R_L is the load.

Fig. 3 - POWER MOS equivalent circuit.



The input capacitance $C_{iss} = C_{GS} + C_{GD}$ during the switching cycle is not constant for two reasons.

1) C_{GD} can be seen as the capacitance between the gate electrode and the drain, where the dielectric is the depleted drain layer. The drain epilayer is fixed, but its depleted part varies according to V_{DS}. The higher V_{DS}, the thicker the depleted layer and consequently the lower the associated capacitance.

2) A more pronounced effect comes from the fact that the voltage across C_{GD}, when the gate source voltage rises from zero to its final value, V_{DS} must go down from V_{DD} to $V_{DS(on)}$. In particular C_{GD} is seen as a higher equivalent capacitance during the drain "on" transitions. The input must be fed a charge:

$$Q = C_{GD}(V_{DD}-V_{DS(on)})$$

to account for the voltage variation across C_{GD}. This happens when the gate voltage reaches $V_{GS}(th)$, the threshold voltage, and the drain voltage starts falling. It is not until the required charge Q is provided that V_{GS} can increase. This is called the Miller Effect. For a while the equivalent input capacitance appears infinite and V_{GD} absorbs the whole input current.
From the moment V_{DS} reaches $V_{DS(on)}$ the input equivalent capacitance is:

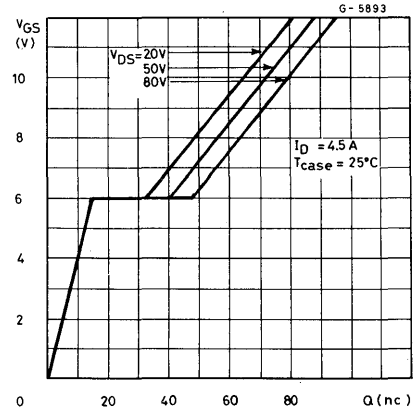
$$C_{eq} = C_{GS} + C_{GD}(\text{low voltage})$$

and the transition of the output is completed. V_{GS} increases again, tending towards V_i.
These two phenomena become apparent when looking at the gate charge versus gate source voltage diagram in the data sheets.
The diagram for SGSP471 in fig. 4 can be taken as an example.

A true capacitor would appear as a straight line starting from the origin. In fact the first segment corresponds to an equivalent capacitance:

$$C_{eq} = C_{GS} + C_{GD}\ (\text{high voltage})$$

Fig. 4 - Gate charge vs, gate-source voltage SGSP471



The horizontal segment corresponds to an equivalent infinite capacitance i.e. the charging of C_{GD} with the gate at V_{th} and the drain falling from V_{DD} to $V_{DS(on)}$. The last segment has a slope corresponding to a capacitance:

$$C_{eq} = C_{GS} + G_{GD} \text{ (low voltage)}$$

The difference in slope of the first and third segment shows how C_{GS} differs in the two cases.

The behaviour at turn-off of the input capacitance is exactly opposite, where the described phenomena occur in reverse order. At this point the drive energy required to make the POWER MOS switch can be calculated as:

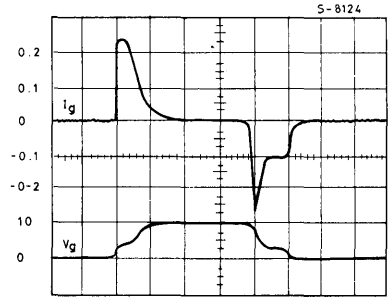
$$E_p = 1/2\ C_{eq} \times V_{GS}^2 = 1/2 Q_G \times V_{GS}$$

Q_G and V_{GS} can be obtained from fig. 4

The input energy can also be obtained in a more direct manner by calculating the integral of the I_G waveform during the turn-on or turn-off phase, the two areas being equal (see fig. 5). In fact this integral represents the quantity Q_G (gate charge) which in turn permits the calculation of E_p.

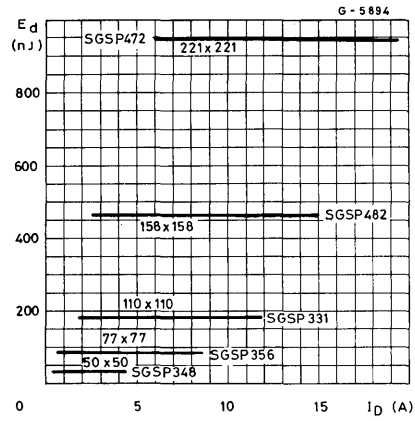
The values of E_p have been calculated for all POWER MOS in the present product range. They are a function of the die area only, for a given supply voltage V_{DD}, and have been represented for different die areas as a function of I_D in Fig. 6.

Fig. 5 - Ig. - Vg waveforms.



t: 0.5 μs/div, I: 0.1 A/div, V:10 $V/_{div}$

Fig. 6 - Ep vs I_D at $V_{DD} = V_{(BR)\ DSS}/2$



The driving energy does not vary for devices with the same die area but different breakdown voltages, if their drive supply voltage has a constant ratio to their breakdown voltage.

In brief E_p can be plotted as a function of the die area, for a supply voltage equal to half the rated V_{DSS} of the device (see fig. 7). The method used here to calculate Q_G is different from that in the data sheet where Q_G is plotted as a function of V_{GS}.

As the results obtained in both methods were in good agreement the validity of the method used here is confirmed.

The driving circuit itself dissipates power to drive the POWER MOS device. Current only flows in the gate circuit during turn-on and turn-off periods. This current flowing through the drive circuit will dissipated energy.

With reference to fig. 8, where the 50 ohm resistor is inserted to match the cable and the device, during the on phase, there is a constant power dissipation in the resistor R_1.

$$(V^2_{GS}/R_1) \cdot t/T$$

Where:

R_1 = 50 ohm (typical value)
t/T = duty cycle

Fig. 7 - E_p versus die side (Sq·mil)

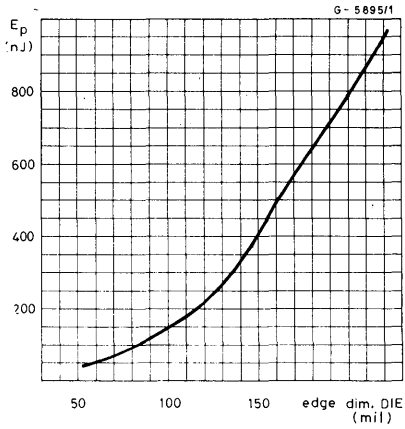


Fig. 8 - Driving circuit. A laboratory implementation

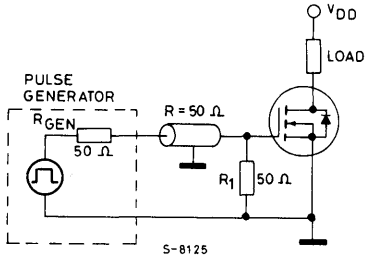


Fig. 9 - Driving circuit. A practical implementation.

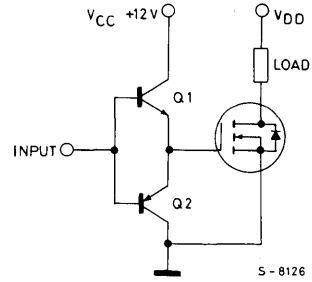


Fig. 9 shows a possible implementation that avoids steady state dissipation in the driver.

The NPN transistor, Q1, only conducts at the beginning of the on phase when charging the input capacitances. Conversely the PNP transistor, Q2, only conducts at the beginning of the off phase when discharging the input capacitances. They never conduct at the same time. No conduction occurs during steady state. In addition, when either of the two transistors conduct their output impedance is very low thus improving the switching of the POWER MOS device. The total energy dissipated per cycle, in the input stage (including the POWER MOS input) is:

$$E_p = Q_G \times V_{CC}$$

Where: V_{CC} = input supply to driving stage voltage. This is +12V in Fig. 7.

This energy is actually dissipated in the two driving transistors, because the parasitic input capacitance of the POWER MOS acts as a non-dissipating element, storing energy from Q1 at turn-on, and giving it back to Q2 at turn-off.

OUTPUT

Switching times for resistive load

Fig. 10 shows the circuit used to measure the switching times of a resistive load.

Fig. 10 - test circuit

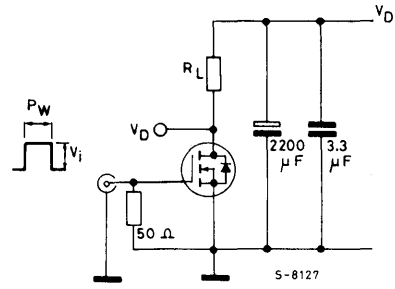
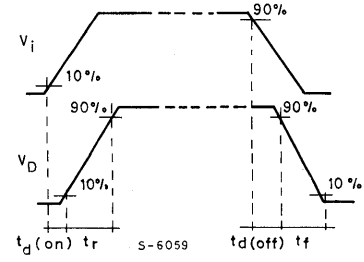


Fig. 11 - V_{GS} and V_{DS} waveforms



Turn on delay time

Turn on delay time ($t_{d(on)}$ in fig. 11) represents the time necessary for V_{GS} to reach the threshold le

vel V_{th} at which the device begins to conduct. The smaller the threshold voltage and the bigger the V_i value, with respect to V_{th}, the smaller the $t_{d(on)}$ value. In fact from the equation:

Eq.1 $$V_{GS} = V_i(1 - e^{-t/R_i C_{iss}}).$$

where Ri. C_{iss} is a time constant and by substituting V_{GS} with V_{th} in Eq.1 we obtain:

Eq.2 $$t_{d(on)} = Ri.\ C_{iss}\ \ln \frac{V_i}{V_i - V_{th}}$$

considering typical values for V_i and V_{th} we have:

$$t_{d(on)} = 0.35 \times Ri.Ciss$$

In practice this time is negligible (10 - 20 ns) when compared to others. During this time the device is off and the energy dissipated is therefore in the order of pJ and compared with the total energy loss it can be completely neglected in this analysis.

t-RISE AND t-FALL TIMES

t-rise and t-fall are defined by the slopes of V_{DS} as shown in fig. 11.

Turn-off delay time

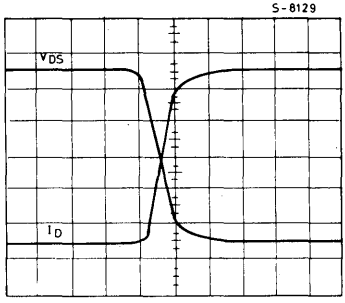
$t_{d(off)}$ can be referred to as the delay time since it represents the time necessary to remove the excess charge from the gate and channel, due to the input overvoltage.

Typical drain current and voltage waveforms (t = 50ns/div.) are shown in fig. 12a and b.

PARASITIC CAPACITANCES DURING SWITCHING CYCLES

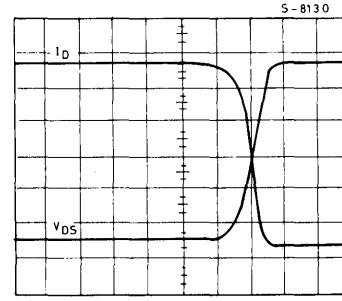
As already mentioned the switching of a POWER MOS device consists fundamentally in the loading and unloading of the input capacitor.

Fig. 12a - Turn-on



t = 50 ns/div

Fig. 12b - Turn-off



t = 50 ns/div

$C_{iss} = C_{GS} + C_{GD}$

From Eq.1 where $R_i \cdot C_{iss}$ is the time constant R_i includes:

R_{gen} - the internal resistance of the generator.

R_1 - the resistor between gate and source to match the driving circuit.

R_G - the internal resistance of the gate.

Fig. 13a - Equivalent circuit

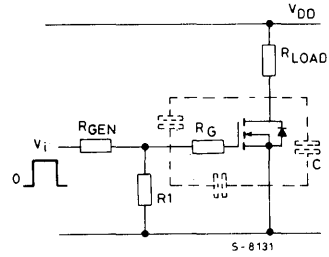
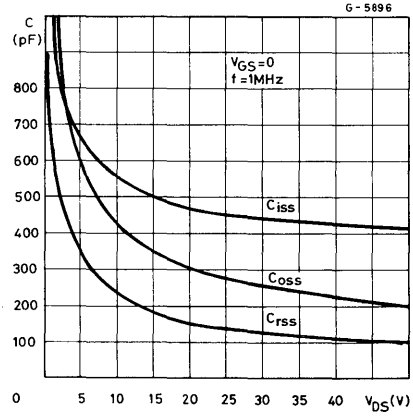


Fig. 13b - Capacitance values as a function of V_{DS}

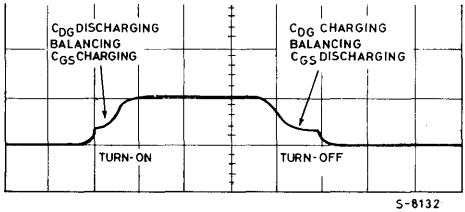


Obviously the smaller the value of $Ri.C_{iss}$ the faster V_{GS} reaches its final value, and switches the device. To minimize this time constant the user can act on R_{gen} and R_1 and the device designer on C_{iss}.

C_{iss}, being a function of C_{GD}, varies as a function of the drain voltage as shown in the waveforms in fig. 13b and during switching it is subjected to the Miller effect. Consequently during the $t_{d(on)}$ and $t_{d(off)}$, C_{iss} remains constant, as does the value of V_{DS}. $t_{d(on)}$ and $t_{d\ (off)}$ are obtained from the charging and discharging laws of a an RC circuit, while during the off/on and on/off transitions, C_{iss} varies. In other words, when V_{DS} decreases during turn-on to a very low value $V_{DS(on)}$, and C_{GD} increases, there is a delay in the increase of the value of V_{GS} since the capacitor, as long as it is not charged to $V_{GS(on)}$, will absorb the gate current.

During turn-off, due to V_{DS} rising, the discharge current of C_{GS}will be balanced by the charging current of C_{GD}, flattening the V_{GS} curve and making it similar to that at turn-on (Fig. 13c).

Fig. 13 c - An annotated extract from fig. 5 showing the discharging and charging of C_{GD}



t: 0.5µs/div, I: 0.1A/div, V: 10V/div

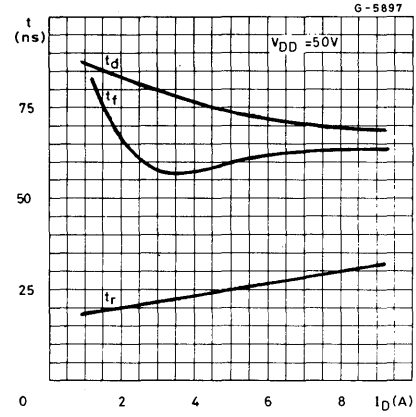
Variations in the supply voltage V_{DD} influence these effects: the higher the supply voltage the greater the charge and therefore the t_f and driving energy required (see fig. 8 in the section OUTPUT).

Figs. 14, 15, 16 and 17 show the switching time waveform as a function of both the supply voltage V_{DD} and the load current I_D, for two devices with different voltages and die sizes.

SGSP311 110V 7A 0.3 ohm $110 \times 110 mils^2$

SGSP369 500V 5A 1.75ohm $156 \times 156 mils^2$

Fig. 14 - Time measurement t_d, t_f, and t_r as functions of I_D. (SGSP311)



The t_r and t_f waveforms versus V_{DD} are similar to those of E_p versus V_{DD} since they are both caused by the same phenomena. t_d is independent of V_{DD} as it is a function of C_{iss} only (which, since the Miller effect is not present, is constant during this phase).

t_d = delay time

t_d = fall time

t_r = rise time

Fig. 15 - Time measurements t_d, t_f and t_r as functions of the drain voltage for a low voltage POWER MOS. (SGSP311)

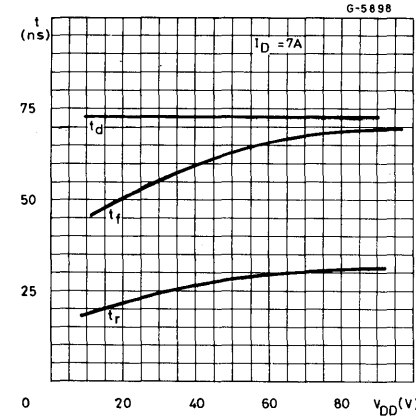


Fig. 16 - Time measurement t_d, t_f and t_r as functions of the drain current for high voltage POWER MOS (SGSP365)

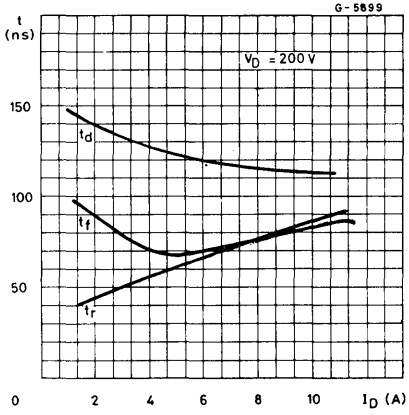
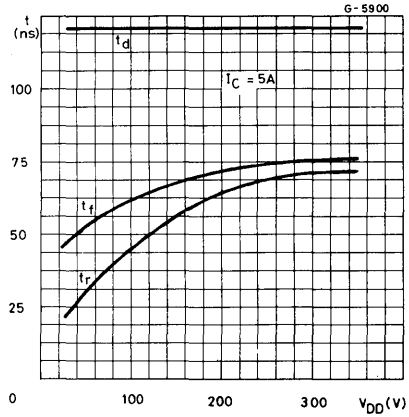


Fig. 17 - Time measurements t_d, t_f and t_r as functions of the drain voltage for high voltage POWER MOS.



Switching times for inductive loads

In the majority of applications POWER MOS are used in switching power through inductive loads (motor control, switching power supply etc.).

The fundamental objective of the device is to switch high quantities of power very quickly, in other words to maximize the ratio:

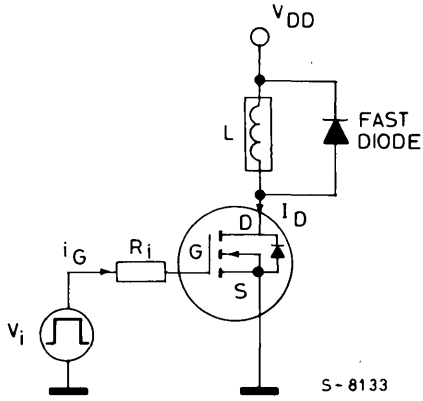
$$\frac{\text{total power switched}}{\text{energy dissipated per cycle}}$$

which depends principally on the switching times.

Understanding switching with POWER MOS requires consideration of both the physical phenomenon and the energy dissipation occuring during each switching cycle.

The typical clamped inductive load circuit shown in fig. 18 is used as an example.

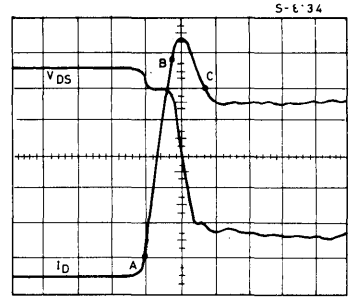
Fig. 18 - POWERMOS with clamped inductive load.



TURN - ON

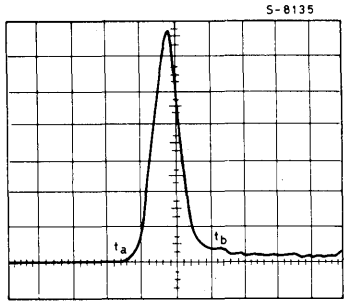
A detailed explanation of the turn-on phenomena in a POWER MOS device when the load is inductive is given by Fig. 19 and 20.

Fig. 19 - Current and voltage waveforms during turn-on



t: 50ns/div, I: 1.2A/div, V: 40V/dir, R = 25Ω

Fig. 20 - Output energy consumption during turn-on.



t: 50ns/div, P: 200W/div, E:67.5 μJ

Before the turn-on phase the diode is freewheeling the load current.
Turn-on can be divided into two subphases:

1) point A to point B (Fig. 19).

Part of the current in the load (constant during the switching operations) starts to flow in the POWER MOS device. The diode is recovering its reverse state. The voltage across the POWER MOS device is almost equal to that of the supply since the diode still acts as a short circuit for the load at this point. There is a small step in V_{DS} waveform due to the voltage drops on the parasitic inductances L_D and L_S. The size of this step depends on the current slope dI_D/dt (L_S and L_D depend on the circuit layout).

2) point B to point C (Fig. 19).

In this phase the diode is reverse biased. The current in the POWER MOS device is the sum of the current in the load plus that in the diode, which causes the peak in the I_D waveform. (see fig. 24)

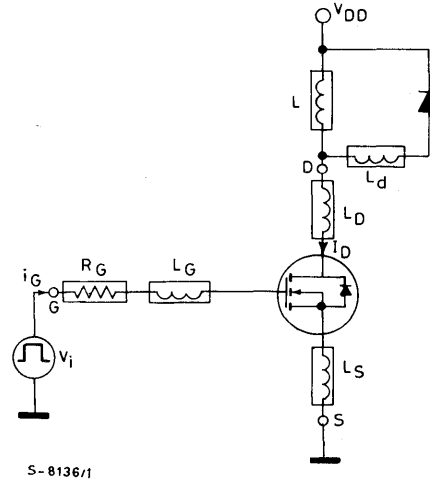
The V_{DS} voltage falls to $V_{DS(on)}$ as the freewheeling diode, being reverse biased, is no longer a short circuit. However the fall of V_{DS} is delayed by the Miller effect, which increases C_{iss}.

All these phenomena cause a high crossover between the I_D and the V_{DS} waveforms even if the switching is very fast. In fig. 20 the output energy consumption per turn-on phase is represented. To decrease this energy, the d_{ID}/dt (A-B phase) and the reverse recovery of the freewheeling diode (B-C phase) must be improved.

IMPROVING dI_D/dt

Reference to the circuit in Fig. 21 shows the controlling, parameters for d_{ID}/dt.

Fig. 21 - Circuit which includes the parasitic inductances.



In this circuit the following elements have been taken into consideration:

L_d - is the parasitic inductance due the connections between the clamping diode and the load.

L_D - is the parasitic inductance between the drain of the POWER MOS device and the load.

L_G - is the parasitic inductance between the gate and the driving circuit.

L_S - is the parasitic inductance between the source and the ground.

The equation that applies to the input loop is:

$$V_i = R_i \times i_G + L_G di_G/dt + V_{GS} + L_S dI_D/dt$$

Where R_i is the equivalent resistance of the driving circuit. When considering the phase when I_D increases it is possible to neglect the term $L_G\, di_G/dt$ as $di_G/dt = 0$.

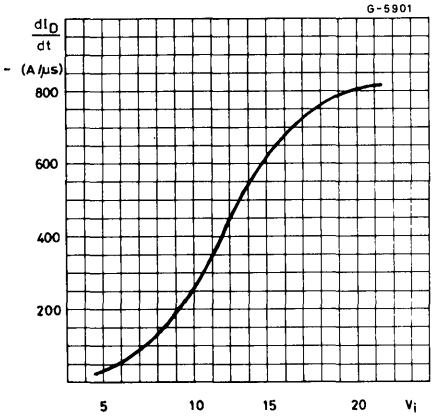
During this phase the threshold voltage has already been overcome, i_G is constant. In addition V_{GS} follows the law of charging a constant capacitance. The Miller effect is not present as V_{DS} is constant.

It follows that:

$$dI_D/dt = \frac{V_i - R_i \cdot I_G - V_{GS}}{L_S}$$

and dI_D/dt can be improved by increasing V_i and decreasing R_G and L_S.

Fig. 22 - dI_D/dt as a function of V_i ($R_G = 25\Omega$) for SGSP369



IMPROVING THE REVERSE RECOVERY OF THE DIODE

As previously mentioned, the clamping diode plays an important role in determining the waveforms of I_D at turn-on; the faster the diode, the lower the current peak in the POWER MOS, the lower the reverse recovery time of the diode (t_{rr}) and the energy consumption. For this reason fast recovery diodes are typically used in these circuits.

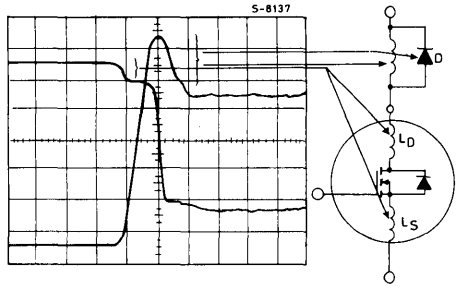
SGS-THOMSON has developed a wide range of fast recovery diodes some of whose characteristics are shown below (fig. 23).

Fig. 23 - SGS-THOMSON Fast recovery diodes.

DEVICE	$V_{reverse}$	$I_{forward}$	t_{rr}	PACKAGE
BYW80-50/200	50/200V	8A	35 ns	DO-220AB
BYW51-50/200	50/200V	2 x 10A	35 ns	TO-220
BYT30P 400/1000	400/1000V	30A	50/70 ns	DOP-3
BYT60P 200/400	200/400V	60A	70 ns	DOP-3

The effect of parasitic inductances L_D and L_S and of the diode connections respectively on V_{DS} and I_D are shown in Fig. 24.

Fig. 24 - Shows the effect of the parasitic inductances L_D and L_S and of the diode connections respectively on V_{DS} and I_D waveforms



TURN-OFF

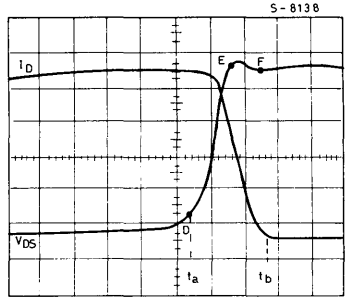
The circuit in Fig. 18 is still useful in evaluating the behaviour of an POWER MOS device turning off an inductive load. The initial conditions can be assumed to be:

1) $I_D = I_{LOAD}$

2) $V_{DS} = V_{DS(on)} = R_{DS(on)} \times I_D$

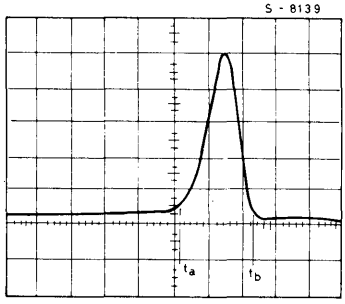
3) Freewheeling diode reverse biased. In fig. 25 typical waveforms for V_{DS} and I_D during turn-off phase are represented

Fig. 25 - V_{DS} and I_D during turn-off



t: 50ns/div, V:40V/div, I:1.2A/div, Rg = 25Ω, Vg = 10V

Fig. 26 - Output Energy during turn-off phase.



t: 50ns/div, P:200W/div, E = 70.6μJ

It is possible to distinguish two phases:
1) From point D to point E (Fig. 25).
During this phase V_{DS} increases while I_D, the diode being reversed biased, remains constant and equal to I_{LOAD}.
2) From point E to point F (Fig. 25).
During this phase the diode begins conducting allowing the current in the load to flow through itself and I_D of the POWER MOS device to fall. In Fig. 26 the output energy consumption during the turn-off phase is represented.

Also in this case a high cross over between V_{DS} and I_D occurs, even if there is no reverse recovery of the diode as during the turn-off phase. The Miller effect in the POWER MOS device delays the rise of V_{DS} and therefore the switch-on of the freewheeling diode D.

ENERGY IN SWITCHING

From the energy point of view there are four distinct phases, each contributing in a different way to the total dissipated energy per cycle. They are:

1) ON-STATE
2) OFF-STATE
3) Transition ON-OFF
4) Transition OFF-ON

The ON-STATE

In the ON-STATE, when the channel is completely open, POWER MOS devices have a minimun $R_{DS(on)}$ which is temperature dependent.
The Power dissipation at a given instant is obtained from the equation:.

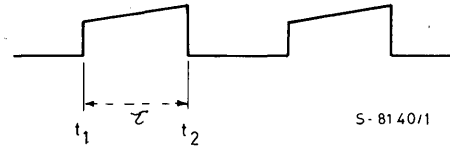
$$P_{D(ON\text{-}STATE)} = R_{DS(on)}(T_j) \times I_D{}^2$$
$$= R_{DS(on)} \times [1 + \alpha(T_J\text{-}25°C)] \times I_D{}^2$$

where $\alpha = 8 \times 10^{-3} °C^{-1}$, a positive coefficient.

The lower $R_{DS(on)}$ the lower the power dissipation. The manufacturers can control $R_{DS(on)}$:
1) by improving the back metalization of the chip and its attachment to the case.
2) by controlling the epitaxial growth of the DRAIN.
3) by optimizing the horizontal lay-out of the POWER MOS structure (high cell density).

Fig. 27 - Can be used to calculate the energy consumption during the ON phase

Fig. 27 - i_D waveform during the working cycle



The slope of I_D during the conduction phase is given by $dI_D = V_{DD}/L$ (see Fig. 19).

The lost energy per cycle is given by:

$$E_{on} = \int_{\phi}^{\tau} I_D{}^2(t) \times R_{DS(on)} \times dt$$

where τ is the pulse width.

In most cases the slope of I_D is quite gentle so if we call I the average I_D between t_1 and t_2, (t_1-t_2 = τ) in Fig. 27, this energy can be calculated with good approximation as follows:

$$E_{on} = R_{DS(on)}(T_j) \times I^2 \times \tau$$

In Fig. 28, 29, and 30 the curves of E_{on} are shown for three different devices. Each curve is characterized by different values of τ.

Fig. 28 - On state energy values as a function of the drain current for SGSP301

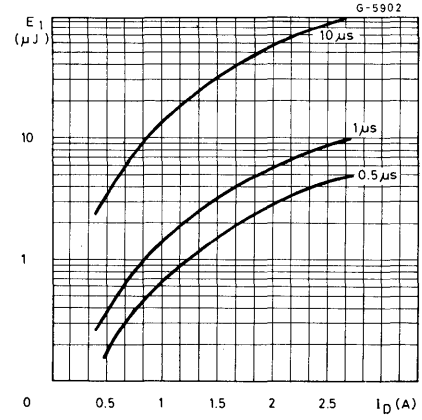


Fig. 29 - On-state energy waveforms as a function of the drain current SGSP575.

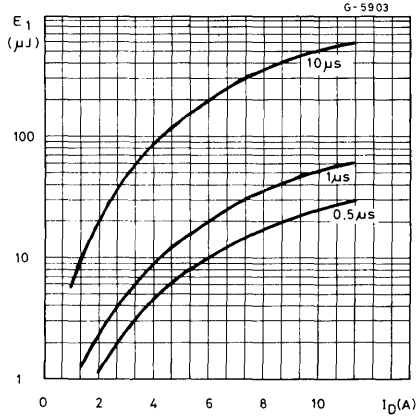
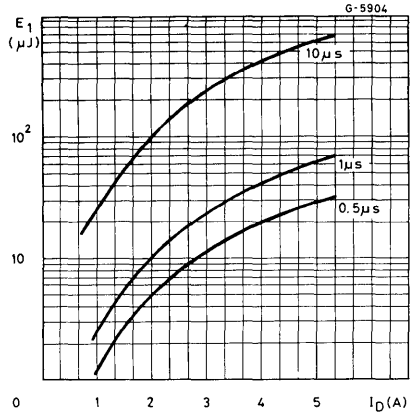


Fig. 30 On-state energy values a function of the drain current SGSP531



OFF-STATE

When the device is switched off the V_{DS} voltage is equal to V_{DD} (see Fig. 25). Only the leakage current I_{DSS} flows through the device. The energy consumption during this period is given by:

$$E_o = V_{DD} \times I_{DSS} \times t_{off}$$

This energy is the range of pJ and it is negligible in comparison to that dissipated during the switching and the ON-STATE.

Transitions

During transitions the dissipated power, instant by instant, is:

$$P(t) = V_{DS}(t) \times I_D(t)$$

The power waveform is triangular in shape (see Fig. 20 and Fig. 26).

Integrating P(t), the energy consumption per cycle during OFF-ON and ON-OFF transitions can be obtained by:

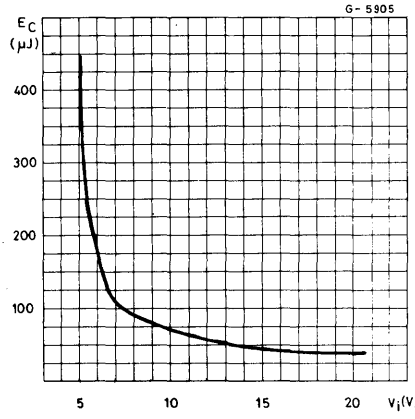
$$E = \int_{ta}^{tb} P(t)dt = \int_{ta}^{tb} V_{DS}(t)\ I_D(t)$$

Where t_a and t_b respectively represent the begining and the end of transitions . These amounts of enegy principally depend on the intersecting point between voltage and current, and on the switching speed.

In both transitions the intersecting points are very high and occur at a voltage value close to that of the supply. The intersecting points represent the power to be switched, consequently in order to optimise the energy consumption the time interval t_a - t_b must be reduced by acting on different driving and lay-out parameters (V_{GS}, R_{GS}, parasitic inductances).

Fig. 31 - Shows the energy lost per cycle during the ON/OFF transition, as a function of V_i for an SGSP369 switching 4A at 200 V.

Fig. 31 - Values of the energy lost per cycle as a function of the gate voltage



COMPUTING THE TOTAL ENERGY CONSUMPTION PER CYCLE

The previous analysis allows us to calculate the total energy dissipated per cycle in an POWER MOS device. In fact the total energy can be expressed as:

Eq.3 $E_{TOT} = E_{On} + E_{off} + E_{off/on} + E_{on/off} + E_p$

where:

E_{TOT} = total energy dissipated per cycle

E_{on} = energy dissipated during the on-state

E_{off} = energy dissipated during the off-state

$E_{off/on}$ = energy dissipated during the turn-on

$E_{on/off}$ = energy dissipated during the turn-off

E_p = total energy dissipated by the drive circuit

Neglecting E_{off} (= pJ) and E_p (= nJ) Eq.3 can be rewritten as:

Eq. 4 $E_{TOT} = E_{on} + E_{off/on} + E_{on/off}$

These three terms in Eq.4 depend in differing amounts on the operating conditions of the device I_D, V_{DD} and the duty cycle.

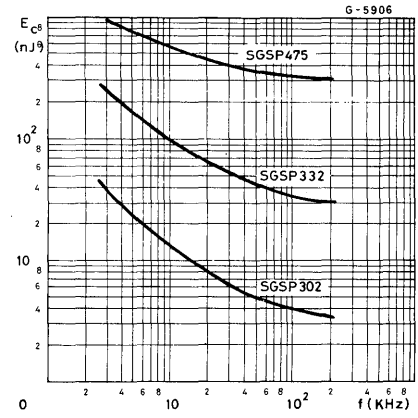
To give some idea of the total energy dissipated per switching cycle the following operating conditions have been fixed and the results of energy measurements made shown in Fig. 32.

V_{DD} = 1/2 $V_{(BR)\ DSS}$ of the device under test

I_D = 3/4 I_{Dmax} of the device under test

duty cycle = 50%

Fig. 32 - Total energy lost per cycle as a function of the frequency with a fixed duty cycle of 50%



The curves tend towards a horizontal asyntote that represents the cross-over energy (turn-on + turn-off, which is frequency independent).

It is clear that the effect of E_{on} is of great importance at low frequencies, and the higher the $R_{DS(on)}$ the greatest the effect.

STUDY OF A MODEL FOR POWER MOSFET GATE-CHARGE

INTRODUCTION

The increasing interest in POWER MOSFET devices is due especially to their ability to switch power at high frequencies and the simple drive requirements needed to achieve this.

Fast switching requires low energy loss during voltage-current cross-over. Easy driving requires only a very simple circuit and low drive energy.

Optimising these advantages requires a sound knowledge of the physical phenomenon which controls their operation.

A valid guide for this purpose is given by the gate charge curve which allows simple evaluation of the drive energy and the switching times.

The influence of the electrical parameters, both external to the device (e.g. I_D, V_{DD}) and the internal ones (V_{TH}, G_M, C_{iss}, C_{rss}, C_{oss}) have been analysed. This analysis of the shape of the gate charge curve, shows its influence on the behaviour of the device.

An analytical expression has been derived that gives a good approximation to the total gate charge and relates it to the internal and external parameters controlling POWER MOSFETs.

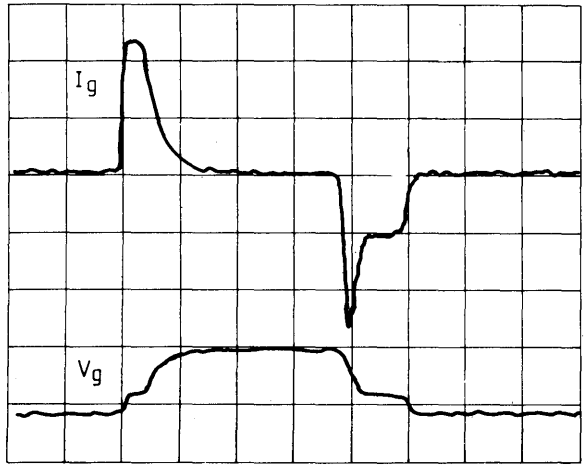
It is interesting to note that this analytical expression represents a valid aid in optimising design when using a software tool.

GATE CHARGE MEASUREMENT

During the switching of a POWER MOSFET, the gate current has the typical behaviour of current in an RC circuit, see figure 1.

The transient lasts for some tens of nanoseconds or more, due essentially to the RC time constant

Fig. 1 - I_G - V_G waveforms

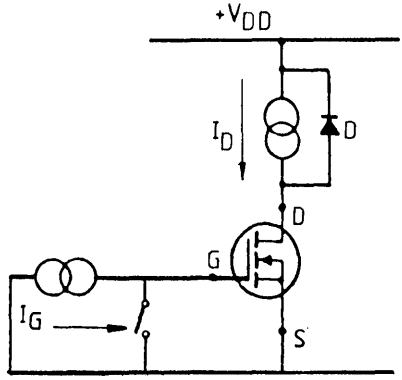


and the maximum current available in the generator. If the current in the gate, I_G, is constant and small enough, the switching time can be increased to a level where the voltage and the current waveforms are free from the parasitic effects caused by the stray inductances that are usually associated with high frequency power switching.

In this way it is possible to isolate the influence of the external factors and analyse just the internal parameters.

The measurement is made as shown in the circuit in figure 2.

Fig. 2 - Test circuit



THEORETICAL ANALYSIS OF THE GATE CHARGE

To get a better understanding of the phenomena which occur during switching it is useful to refer to the model of the POWER MOSFET shown in figure 3. The fig. 3a shows a cross section of a single cell illustrating the parasitic capacitances.

These capacitances correspond to the capacitances quoted in the POWER MOS databook as follows:

$$C_{iss} = C1 + (C2 \cdot C4)/(C2 + C4) + + (C3 \cdot C5)/(C3 + C5)$$

$$C_{rss} = (C3 \cdot C5)/(C3 + C5)$$

$$C_{oss} = (C3 \cdot C5)/(C3 + C5) + C6$$

If we take into account the actual test conditions (V_{GS} = 0, f = 1MHz, V_{DS} = 25V) the above equations are well approximated as follows:

$$C_{iss} = C1 + C2 + C5$$

$$C_{rss} = C5$$

$$C_{oss} = C5 + C6$$

This approximation is correct since $C2 << C4$ and $C5 << C3$.

During the switching phase the value of these capacitances change as a fuction of V_{GS} and this approximation no longer holds.

Fig. 3 - Simplified cross section of a POWER MOSFET cell (a) and its electrical equivalent (b).

Fig. 3a

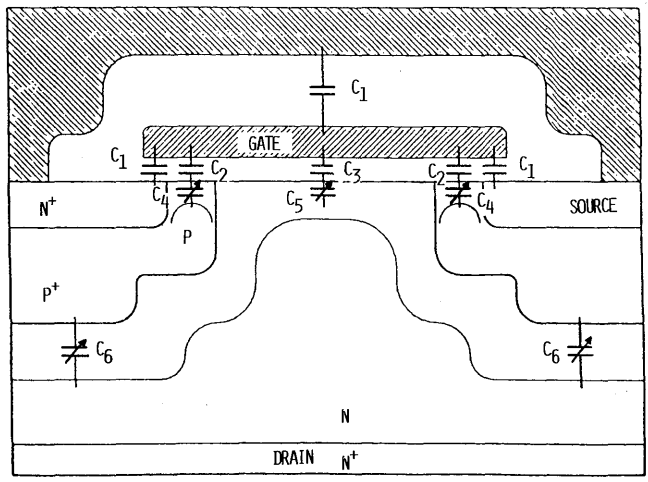
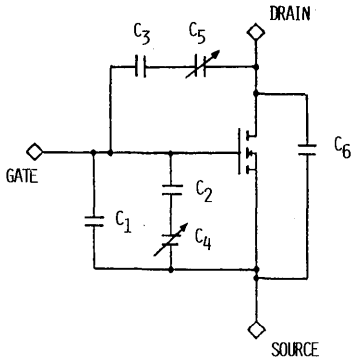


Fig. 3b)



C_1 : Capacitance between gate and source (both N^+ and metal)

C_2 : Capacitance between gate and P zone.

C_3 : Capacitance between gate and epi N.

C_4 : Capacitance of the channel depletion zone.

C_5 : Capacitance of the depletion zone in the superficial epi.

C_6 : Capacitance of the body-drain junction.

Referring to figure 4 and 5 and distinguishing the load line during turn-on we can identify the following phases:

0: the device is off (I_D = I leakage, $V_{DS} = V_{DD}$) and the capacitances C_{GS} and C_{GD} are respectively equal to C_{iss} and C_{rss} measured with $V_{DS} = V_{DD}$.

0 → 1: the gate voltage reaches V_{TH} by charging C_{GS} from (C1 + C2 + C5) to (C1 + C4 + C5).

Fig. 4 - Load line during turn-on

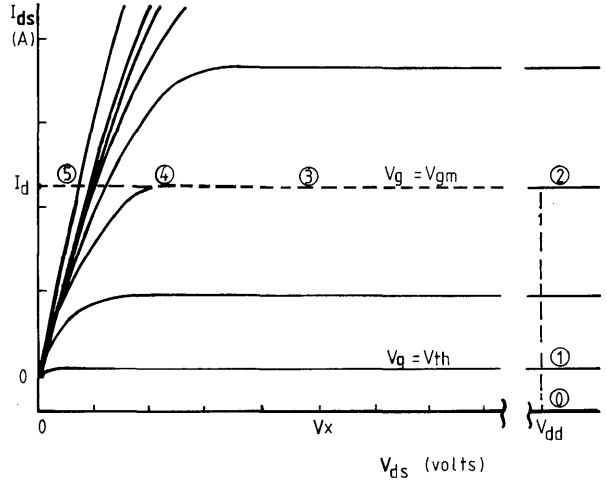
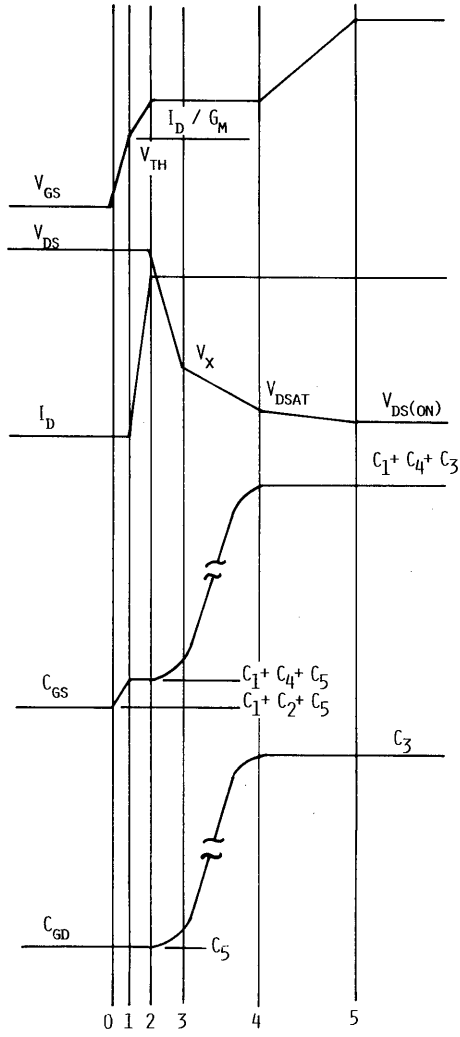


Fig. 5 - Switching waveforms and capacitance modulation



The total increase, is due to modulation of the depletion layer between the body and drain close to the channel. This is caused by the small drain current flowing when the gate voltage is near to V_{TH}. The variation is about 10%.

1 → 2: in this phase C_{GS} and C_{GD} are almost constant. V_{DS} is clamped to V_{DD} by the diode until I_{DS} reaches its final value. In this phase the device exhibits typical pentode characteristics (see figure 4) with V_{DS} constant.

During this phase, modulation of the depeletion zone is due solely to the increasing drain current.

Figure 6a shows how the current flux spreads inside the drain.

Fig. 6a - Depletion layer and current distribution for a POWER MOSFET in the pentode region

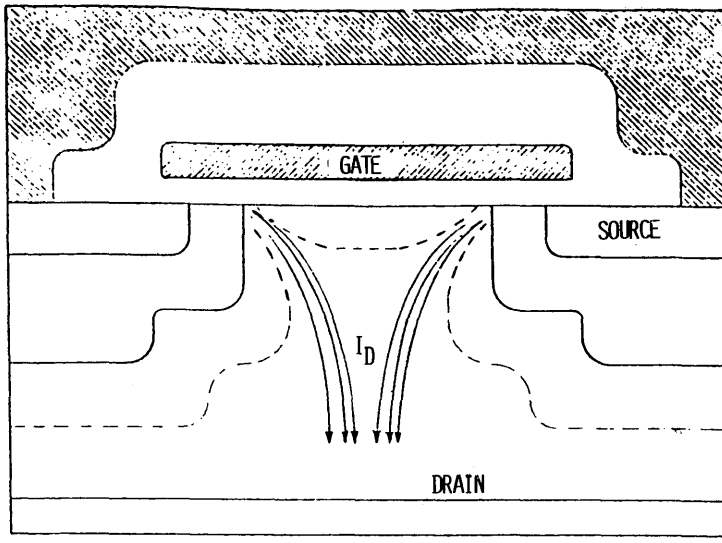
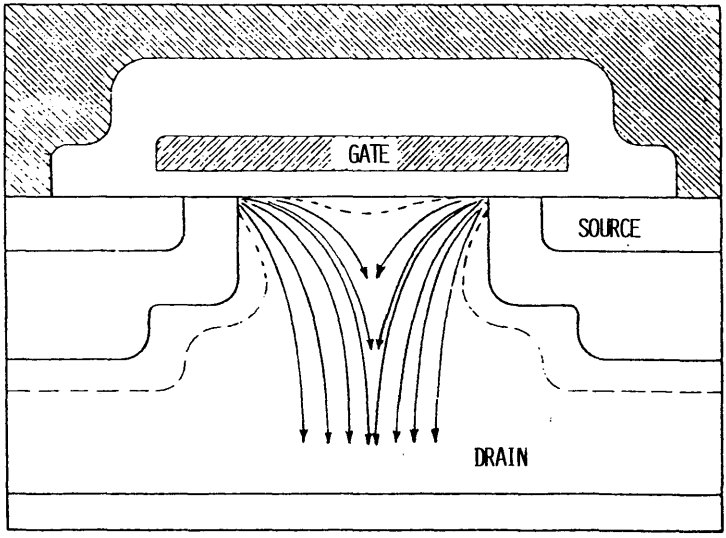


Fig. 6b - Depletion layer and current distribution for a POWER MOSFET in the linear region



The gate voltage, starting from the V_{TH}, reaches the value $V_G = V_{TH} + I_D/G_M$, where G_M is the large signal transconductance.

The variation of the gate voltage slope, due to the the high current density under the gate region in the N zone is in reality much less pronounced than that shown in figure 5.

The actual increase of the capacitance, both during the first and second phase, due to this modulation effect, happens gradually and is more evident near the threshold voltage.

Since, in these two phases, the average increase of the capacitance has been evaluated as about 10%, the charge supplied to the gate can be approximated using the following equation:

$$Q1 + Q2 = 1.1 \cdot C_{iss} \cdot (V_{TH} + I_D/G_M)$$

2 → 4: during this phase the drain voltage decreases, with consequent modulation of the depletion zone and increase in capacitance of C5.

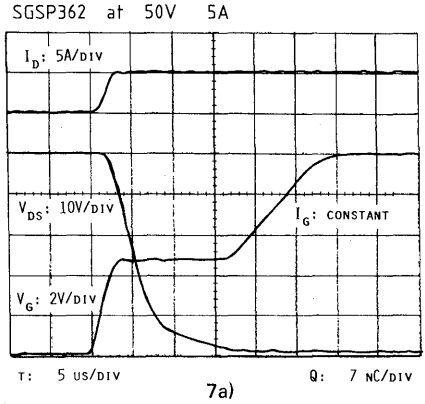
This phenomenon, known as the Miller effect, has a specific action on the gate voltage. As charge is supplied to the gate, the voltage remains constant, the capacitance appearing to be infinite during this phase. Also V_{DS} has two different slopes; first there is little variation in C5, therefore of both C_{GS} and C_{GD}, and second, the variation in C5 is very high.

The variation of C5 as a function of V_{DS} is typical of a MOSFET structure. The only difference is due to the fact that modulation of the depletion zone is caused not only by the voltage but also by lateral injection of the charges coming from the channel.

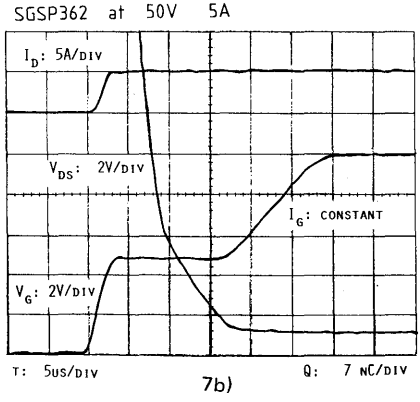
At the end of this transition C_{GD} will have the value of C3 and consequently C_{GS} the value (C1 + C4 + C3).

The drain voltage, on the slope, is indicated as V_X, in figure 4.

Figs. 7a) and 7b) - V_G, I_D, V_{DS} waveforms for SGSP362

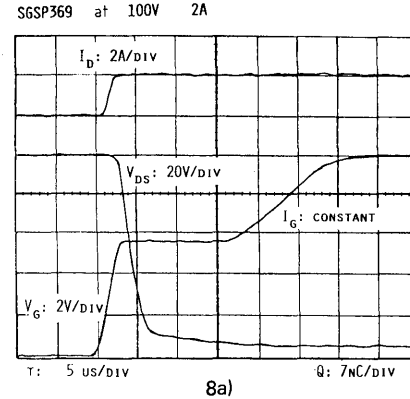


7a)

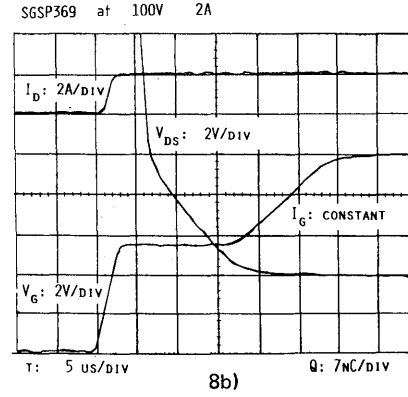


7b)

Figs. 8a) and 8b) - V_G, I_D, V_{DS} waveforms for SGSP369



8a)



8b)

Physically this point indicates the transition from a highly charged P zone to simple depletion of the MOSFET capacitor that exists between the deep body cells. We can state:

$$V_X = V_{TH} + V_{TH\text{-}epi} + (R_{epi} \cdot I_D)$$

Figure 7a/7b and 8a/8b show test measurements carried out on both low and high voltage POWER MOSFET devices.

At the end of this phase V_{DS} has reached $V_{D\ sat}$. This is illustrated in figure 5 and figure 6b.

The charge supplied to the gate is:

$$Q3 = 1.1 \cdot C_{rss} \cdot (V_{DD} - V_X)$$

$$Q4 = C3 \cdot (V_X - V_{D\ sat})$$

Where Q3 and Q4 are the transitions across phase 3 and phase 4 respectively.

The coefficient introduced in the formula for Q3 is derived as follows: V_{DS}, starting at V_{DD} reaches V_X; C_{rss} undergoes a slight variation (as described earlier). This variation has been evaluated as about 10% to 15%.

4 → 5: as soon as the Miller effect finishes, the gate voltage can increase again and reach its final value. The rate of this increase is controlled by C_{GS} where C_{GS} = C1 + (C4 + dC4) + C3, a constant from this point on.

Referring to figure 4 again, I_D crosses the characteristic curves, as I_D is constant, until $V_{DS\ on}$ is reached. The charge supplied during the final phase is:

$$Q5 = (C1 + C3 + dC4) \cdot (V_{G\ max} - V_{TH} - I_D/G_M).$$

The total charge supplied to the gate during turn-on can now be derived from the sum of the single contributions of the five phases:

EFFECTS OF THE PHYSICAL AND ELECTRICAL PARAMETERS ON Q_{tot}

The previous discussion has shown that the total charge supplied to the gate is influenced by several parameters, which are essentially:

a) electrical parameters (V_{DD}, I_D, $V_{G\ max}$)

b) structural parameters (capacitances, V_{TH}, G_M, $V_{D\ sat}$).

The electrical parameters are imposed by the external circuit and depend on the application; the structural parameters are typical of the device and can be adjusted during the device design stage in order to optimise its performance.

Figure 9 shows the influence of I_D and V_{DD} on the shape of the gate charge curve. Figure 10 and 11 show the influence of the capacitances and the transconductance, G_M on the same curve.

The following discussion shows the consequence of varying a single parameter, on the performance of the device.

Fig. 9 - Gate charge curves as a fuction on I_D and V_{DD}

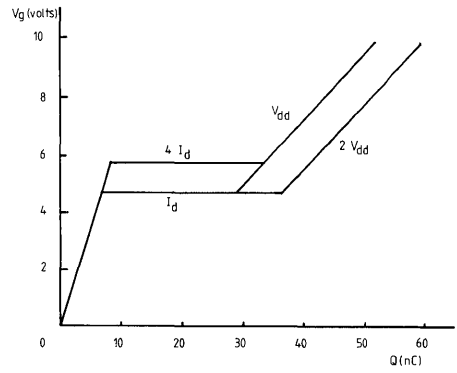


Fig. 10 - Gate charge curves a as function C_r and G_M

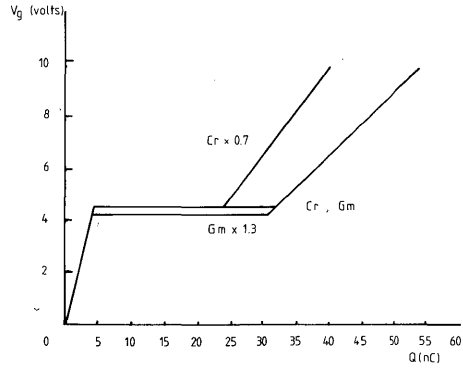
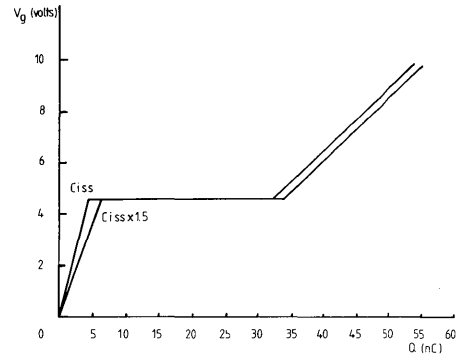


Fig. 11 - Gate charge curves as a function of C_{iss}



The horizontal axes of these graphs are in nanocoulombs ($Q = I_G \cdot t$, I_G = const.) while the vertical axes are in volts.

— the area under the gate-charge curve represents the driving energy of the device, E_p:

$$E_p = \int V_G\,(Q) \cdot dQ$$

— the energy lost during the cross-over period determined by measuring t_{rise} and t_{fall}, is proportional to the amplitude and length of the 'flat' region - (Miller), of the gate charge curve.

From these figures it can easily be seen than in order to obtain fast switching, and low energy dissipation during the cross-over, the optimum device should have:

— LOW C_{rss}
— HIGH G_M
— LOW C_{iss}

C_{iss} has less influence in comparison to C_{rss} and G_M. Consider two different devices showing the same characteristic but the C_{iss}, G_M and C_{rss} with:

$$C_{iss}2 = 2 \cdot C_{iss}1$$
$$G_M2 = 1.3 \cdot G_M1$$
$$C_{rss}2 = 0.7 \cdot C_{rss}1$$

figure 12 shows that device 2, despite higher input capacitances, shows better behaviour regarding both the switching times and the driving energy.

A merit coefficient commonly used to give a "measure" of performance is:

$$K = G_M/C_{rss}$$

Increasing this coefficient can be achieved at the design stage, by optimising the perimeter of the channel, W. This has the effect of increasing G_M (G_M is proportional to W/L). C_{rss} can be decreased by reducing the overlap area between gate and drain and by adjusting the doping of the epitaxial layer.

This latter solution, if we take into account that the doping in the epitaxial layer is controlled by the required BV_{DSS}, would require an epitaxial growth with a variable doping profile which decreases near the surface.

This would cause a slight increase in the accumulation resistance, which would require characterising.

The feasible solution is to decrease the inter cell distance; in this way, for the same active area, a greater channel perimeter and a smaller overlap area is obtained.

Figure 13 illustrates this by depicting K, for devices having the same chip-size, as a function of BV_{DSS} (N epi); the same figure shows the gain obtained for devices having greater cell density.

Fig. 12 - Comparison of gate charge curves of two devices with different values, of C_{iss}, G_M and C_{rss}

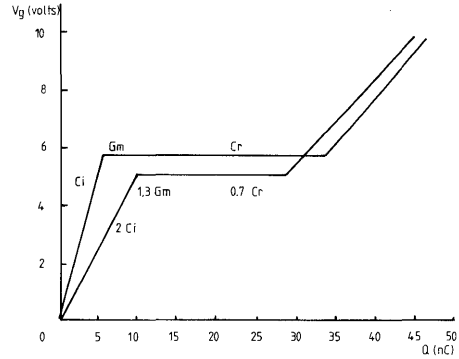
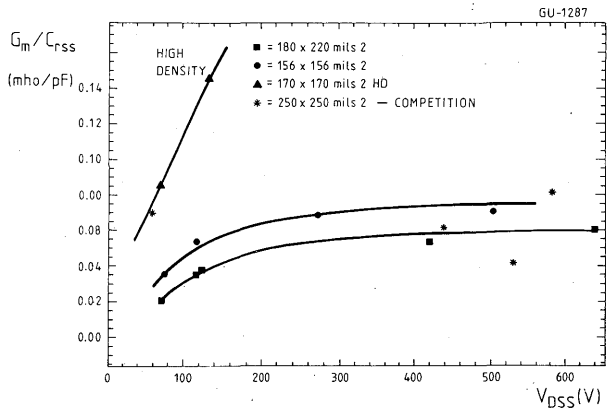


Fig. 13 - G_M/C_{rss} ratio vs breakdown



CONCLUSION

The gate charge curve supplies useful information about the actual behaviour when the device switches.

From the users point of view, these curves allow the correct design of the drive circuit and correct choice of the device which best satisfies the design criteria.

The use of a simulation of this model allows designers to evaluate the consequences of varying one or more of the parameters of the final characteristics of the devices.

Further research is being carried out to solve the problem caused when the capacitance is modulated by the injection of charge due to the drain current.

COMPARISON OF POWER MOS AND BIPOLAR POWER TRANSISTORS

It is highly predictable that in the near future POWER MOS will, in many applications, gradually replace power bipolar devices due to the numerous advantages they offer.
Table 1 lists the principal differences between POWER MOS and bipolar transistors. In addition to their inherent high switching speed resulting from the lack of minority carrier injection during operation, POWER MOS with their insulated gates require negligible input gate-drive current. Other

MOS	BIPOLAR
Majority-carrier device	Minority-carrier device
No charge-storage effects	Charge stored in the base and collector
High switching speeds less temperature sensitive than bipolar devices	Low switching speed temperature sensitive
Drift current (fast process)	Diffusion current (slow process)
Voltage driven	Current driven
Purely capacitive input impedance; no dc current required	Low input impedance; dc current required
Simple drive circuitry	Complex drive circuitry (resulting from high base-current requirements)
Predominatly negative temperature coefficient on resistance	Positive temperature coefficient of collector current
No Thermal runaway	Thermal runaway
Devices can be paralleled with some precautions	Devices cannot be easily paralleled because of V_{BE} matching problems and local current concentration
Less susceptible to second breakdown	Susceptible to second breakdown
Square-law I-V characteristics at low current; linear I-V features at high current	Exponential I-V characteristcs
Greater linear operating and fewer harmonics	More intermodulation and cross-modulation products
High-on resistance and, therefore, larger conduction loss	Low on-resistance (low saturation voltage) because of conductivity modulation of high resistivity drift region
Drain current proportional to channel width	Collector current approximately proportional to emitter stripe length and area
Low transconductance	High transconductance
High breakdown voltage as the result of a lightly doped region of a channel-drain blocking junction	High breakdown voltage as the result of a lightly doped region of a base collector blocking junction

advantages are related to the negative temperature coefficient of their current, which prevents the formation of thermal instabilities and makes the paralleling of devices much more reliable. In contrast, bipolar transistors require ballasting or careful device matching to prevent thermal runway.

Only in high voltage cases is POWER MOS on-resistance higher than in bipolar transistors.

This leads to slighty larger steady state power dissipation and could offset the advantages.

PERFORMANCE COMPARISON

At this point a comparison between POWER MOS and bipolar devices can be made in order to evaluate their switching speeds which give an indication of the energy consumption during transitions, and their different values of $V_{DS\ (on)}$ and $V_{CE\ sat}$ related to energy consumption during the on state. The two devices used in the comparison are:

SGSP565: POWER MOS; 400V; 6A
$R_{RD\ (on)} = 1\Omega$

SGSD00036: BIPOLAR; 400V; 6A (very fast switching)

$V_{DD}/V_{CC} = 200V$

$I_L = 5A$ (average value)

Since the input losses were neglected the bipolar devices have an advantages in this comparison.

E_{TOT} (the energy losses per cycle) as a function of the operation frequency, for different values of the duty cycle can be seen in fig. 1. For a bipolar device, the energy used during the on phase has only a slight influence with frequency variation. POWER MOS however are influenced by these variations, and as a result two curves, relative to the same duty cycle, are obtained. The intersecting points of these curves can be considered as a giudeline to the use of the devices.

In other words if both the duty cycle and the power to be switched are fixed there is a frequency value above which the dissipated energy per cycle for an POWER MOS transistor is less than for a bipolar device. This means the higher the frequency the more advantageous it is to use a POWER MOS.

Under relatively low frequency conditions the value of the duty cycle "d" is fundamental in determining the advantages of both bipolar and POWER MOS technologies. From the graph in Fig. 2 the best working condition for both devices can be seen.

Fig. 1 - E_{TOT} versus frequency (kKz)

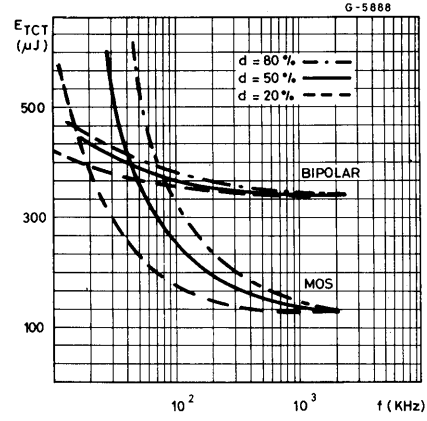
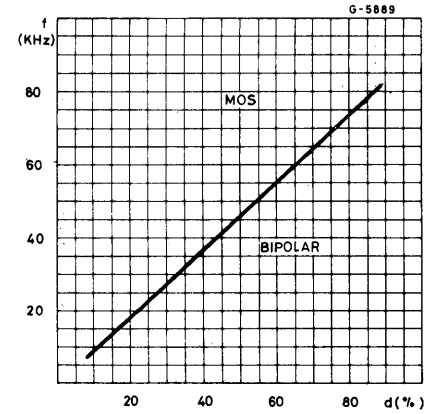


Fig. 2



A POWER MOS is most suited to high frequency conditions (> 100 KHz) for any given value of "d". Maximum frequency limitations are of a thermal nature only and depend on the die size.

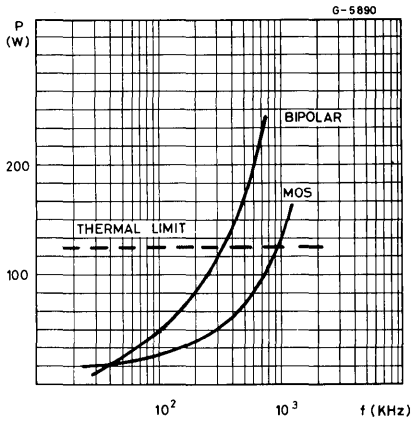
For the POWER MOS under consideration the maximum power dissipated is 100W when $R_{thj\text{-}case} = 1°C/W$ and $T_{j\ max} = 150°C$.

By plotting the power dissipated as a function of the frequency, when d = 50% the actual limits of the two technologies can be seen (Fig. 3).

THERMAL STABILITY

The greater thermal stability of SGS-THOMSON POWER MOS with respect to bipolar devices is essentially due to the different response that the two

Fig. 3



devices exhibit when they are subjected to external power pulses.

The intrinsic mechanism which could lead to thermal runway in bipolar and in a POWER MOS device, are as follows.

In a bipolar an external power pulse results in an increase in the junction temperature (T_j).

This causes the collector current to increase and this consequently further increases T_j. This positive feedback is compensated only by the base widening effect at high currents (that is a higher recombination of the minority carriers). At high voltages the base widening effect is not present so that any hot spots lead to thermal runaway.

These phenomena, if not controlled, could seriously damage a bipolar device.

A power pulse in a POWER MOS device would cause:

1) an increase in temperature of the device
2) a decrease in the threshold voltage

$V_{GS\,(th)} = V_{GS\,(th)}\,(25°C) \times (1 - \alpha\,[(T_j - 25°C)]$

where alpha is a positive coefficient of temperature ($\alpha = 2.10^{-3}$).

This is positive feedback and similar to a decrease of V_{BE} in bipolar devices.

But in a POWER MOS device there is also a very important negative feedback. That is an increase of $R_{DS\,(on)}$ with temperature:

$R_{DS\,(on)}(T) = R_{DS\,(on)}\,(25°C) \times [1 + \alpha\,(T - 25°C)]$

where alpha is the temperature coefficient (alpha $= 8{\cdot}10^{-3}{}^{\circ}C^{1}$). The effect of a increase in $R_{DS\,(on)}$ is greater than the variation in $V_{GS\,(th)}$. As a result POWER MOS devices are thermally stable. The difference in behaviour of the two devices is even more exaggerated when dealing with paralleled chips.

Two comparisons between bipolar and SGS-THOMSON POWER MOS devices have been made.

The first deals with the behaviour of single chips in SOT-93 (TO-218) package.

The SGS POWER MOS used in this test is the SGSP475 (400V, 12A, 0,55Ω).

The power bipolar device used in the BUV48 (400A, 10A).

The parameter used to measure the thermal unbalance of the devices is the variation of the thermal resistance $R_{thj\text{-}case}$ due to an external power pulse.

In fact an increase of $R_{thj\text{-}case}$ implies a decrease of the active area of the chip and therefore a disuniformity in the spreading of the heat, with a creation of hot spot and thermal and electrical unbalancing. The devices have been tested under several conditions, with respect to the power dissipation and the voltage across them (V_{DS} for SGSP471, V_{CE} for BUV48). The results are shown in Fig. 4 and Fig. 5).

SGSP475 shows optimum thermal stability under all conditions while bipolars, with V_{CE} = 45V and P > 45W, show a degrading of the thermal performances.

The best electrical and thermal performance of the SGS-THOMSON POWER MOS are confirmed by the thermal maps which show a uniform distribution of heat under different working conditions (Fig. 6 and 7).

Fig. 4 - Variation of $R_{thj\text{-}case}$ vs. P (POWER MOS) SGSP475 SOT-93

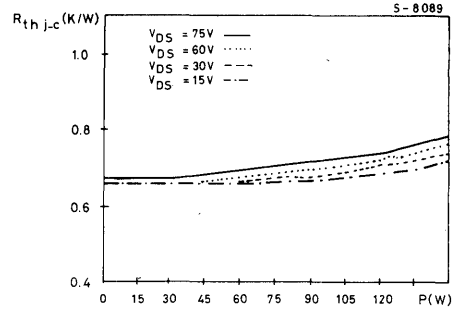


Fig. 5 - Variation of $R_{thj\text{-}case}$ vs. P (BIPOLAR) BUV48 SOT-93.

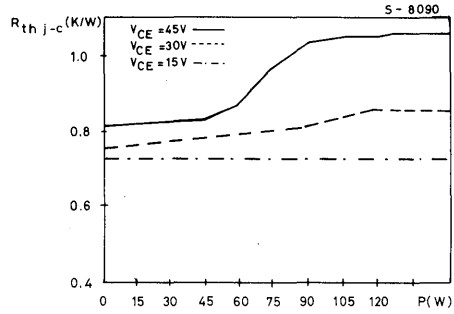
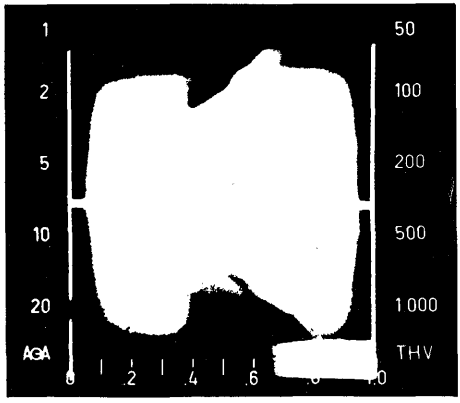


Fig. 6

Fig. 7



It is only at V_{DS} = 75V that is it possible to notice a slight variation in the working temperature.

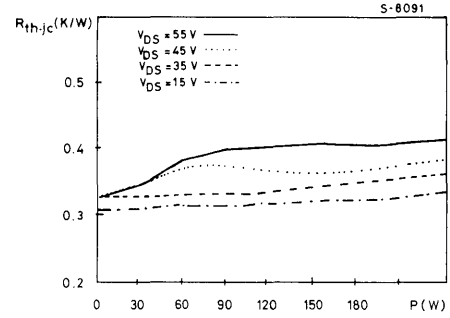
The thermal instability has a greater effect when the die are assembled in parallel since any unconformity would be enhanced leading to an overloading of some of the die.

The second thermal comparison was made between SGS-THOMSON POWER MOS and bipolar devices in multiple chips mounted in a parallel configuration.

The SGS-THOMSON POWER MOS device under test was:

SGS30MA050D1: four POWER MOS chips paralleled in TO-240 a package I_{Dmax} = 30A, V_{DSS} = 500V, $R_{DS\ (on)}$ = 0.250Ω

Fig. 8 - Variation of $T_{thj\text{-}case}$ vs. P (POWER MOS) SGS30M050D TO-240

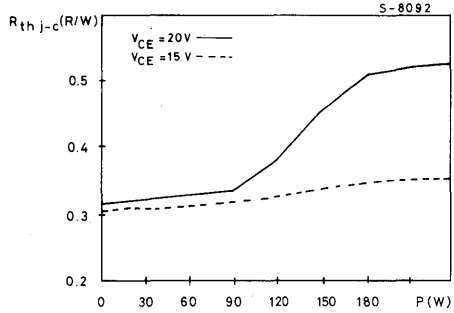


The bipolar device under test was:

SGS40TA045D: four bipolar chips paralleled in TO-240 package I_C = 40A V_{CEO} = 450V

The results are shown in Fig. 8 and 9 and reveal a much better thermal stability for the POWER MOS than for the bipolar device.

Fig. 9 - Variation of $R_{thj\text{-}case}$ vs. P (BIPOLAR) SGS400T045D TO-240



A BRIEF LOOK AT STATIC dV/dt IN POWER MOSFETS

INTRODUCTION

The normal safe operating area of POWER MOSFETS may be insufficient when used in very fast switching circuits, such as those required in SMPS push-pull applications. When there is a high slew rate between the drain and the source of a POWER MOSFET, it may go into breakdown at a voltage less than its breakdown voltage, $V_{(BR)\,DSS}$, due to the spurious turn on of its parasitic bipolar transistor. This in turn could damage its internal structure or cause a malfunction of the circuitry.

The critical values of dV/dt may vary with the operating conditions of the POWER MOSFET device used; when it is under stress and completely inactive, (static dV/dt) or when its intrinsic diode is conducting (dynamic dV/dt). This note discusses the safe operating conditions for POWER MOSFET transistors that experience static dV/dt stress.

The explanation of the measurement circuit describes the difficulty in attaining the value of destructive dV/dt.

STATIC dV/dt TURN-ON

Figures 1 and 2 show the simplified equivalent circuit for a POWER MOSFET when a high slew rate exists between the drain and the source. POWER MOSFETS initially in the off state, conduct in two different ways due to dV/dt:

— by spurious turn-on of the POWER MOSFET
— by spurious turn-on of the parastatic bipolar transistor.

Fig. 1 - Simplified electrical behaviour of POWER MOSFETS under the effect of dV/dt

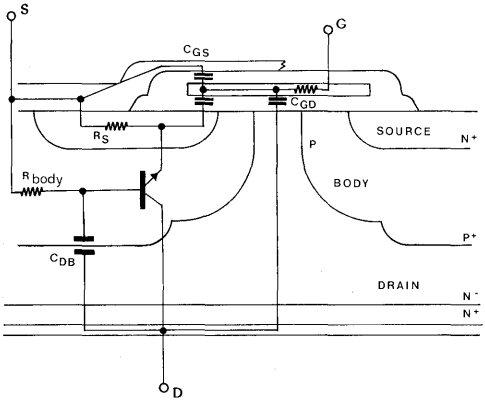


Fig. 2 - Simplified equivalent circuit

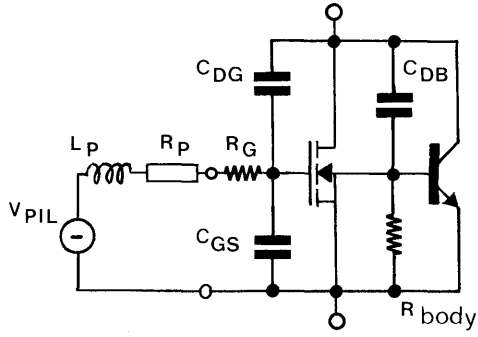


Figure 3 shows the equivalent circuit for conduction by spurious turn-on of the POWER MOSFET. Figure 4 shows current waveforms generated by a fast voltage variation across the POWER MOSFET capacitance. The current pulse passing through the external impedance (Zgs), positioned between the gate and source (driving impedance), creates a voltage pulse. If this voltage reaches the threshold voltage the POWER MOSFET switches on. This type of switching thrives on a high input impedance, Zgs, but is not normally destructive.

Fig. 3 - Equivalent circuit for conduction by spurious turn-on of POWER MOSFETS

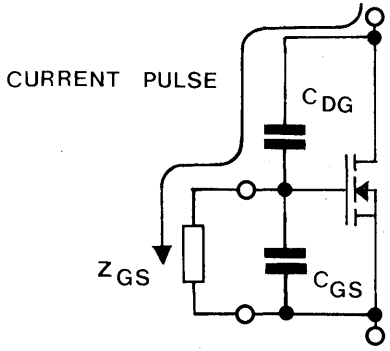
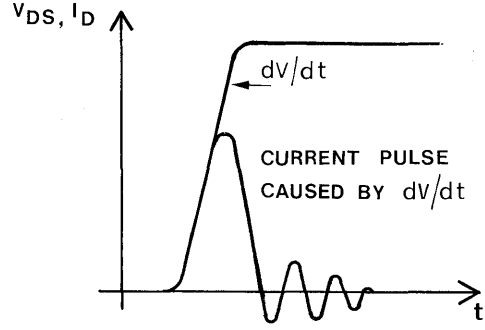


Fig. 4 - Equivalent waveforms for the fast voltage variation across the POWER MOSFET capacitances.



The equivalent circuit for conduction by spurious turn-on of the parasitic transistor, is shown in figure 5. A current pulse passes through the capacitance $C_{DB}$and the body. If the voltage drop across the body resistance rises above 0.65V, the body source junction is polarized, this produces current injection in the base of the parasitic transistor which consequently turns on. If V_{DS} is more than the breakdown voltage of the parasitic transistor, avalanche breakdown occurs. If the current, I_D, is not limited externally the device may be destroyed. Unlike the first mechanism the critical value of dV/dt depends only on the structure of the device (R_{body}, C_{DB} and the resistance between the base and the emitter of the parasitic transistor).

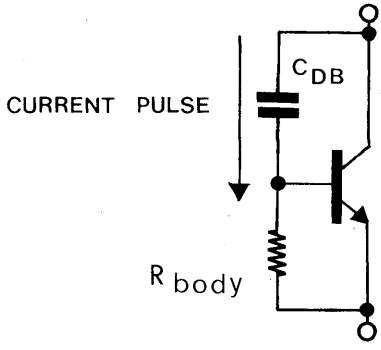


Fig. 5 - Eqivalent circuit for conduction by spurious turn-on of the parasitic transistor

This type of conduction may be destructive, depending on the value of the supply voltage, V_{DS}, applied and the collector-emitter breakdown, V_{CEX}, of the parasitic transistor. This value is between $V_{(BR)DSS}/2$ and $V_{(BR)DSS}$.

In SGS-THOMSON POWER MOSFETs V_{CEX} is near $V_{(BR)DSS}$, thanks to a large reduction of the emitter-base resistance of the parasitic transistor (body and source in short circuit).

Measurement Circuit

The circuit in fig. 6a is a hypothetical application where a POWER MOSFET could be stressed by static dV/dt. The POWER MOSFETs P_1, P_2 conduct alternately, and apply the voltage $+V_{DD}/2$ and $-V_{DD}/2$ on the transformer. During switching between P_1 and P_2 there is always a period in which one of the POWER MOSFETs is turned off. The load is therefore fed with AC.

Fig. 6a - Typical application where DMOS can be stresses in static dV/dt

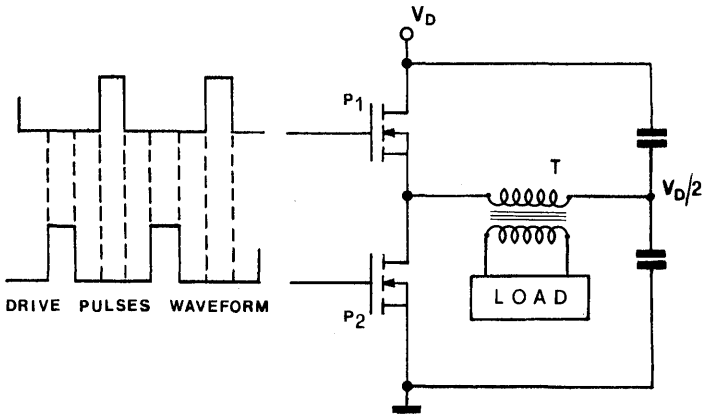
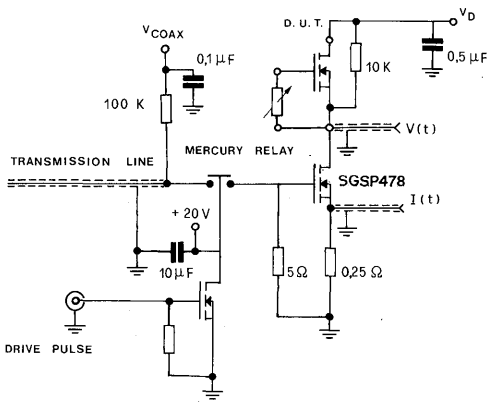


Fig. 6b - Test circuit for POWER MOSFETs stressed by static dV/dt

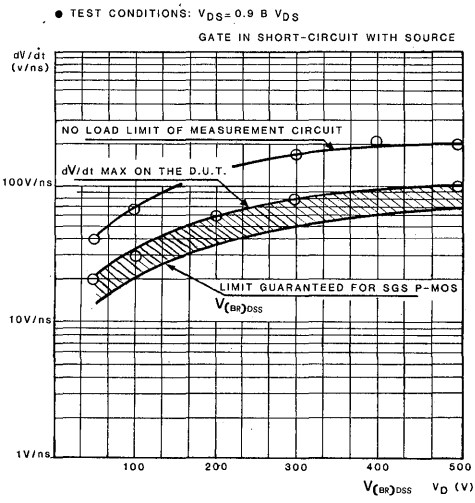


The dV/dt stress occurs when, for example, P_2 turns on and the source of P_1 decreases from the voltage V_D to zero with a speed equal to the switching speed of P_2.

The turn-on of the parasitic transistor occurs when the switching times are in the range of 3-5ns. This switching speed was obtained using the circuit in figure 6b where the active POWER MOSFET is driven by a low impedance pulse generator.

The pulse generator consists of a transmission line with a characteristic impedance of 5 ohm, which during the turn-on of the mercury relay creates a voltage waveform on the gate of the active POWER MOSFET. A mercury relay is used to obtain very steep edges. The transmission line consists of 10 coaxial cables in parallel with a characteristic impedance of 50ohm and infinite impedance load. Each cable is 6m. long in order to generate a pulse lasting about 50ns.

All the connections were made in order to reduce to a minimum the inductance and the parasitic capacitance.



Acting on the load voltage (V_{coax}) of the transmission lines the switching speed of the POWER MOSFET varies until it reaches the critical value of dV/dt; all the values measured are shown on the graph in fig. 7.

Fig. 7 - dV/dt for the test circuit with and without a POWER MOSFET load and limit guaranteed for POWER MOSFET versus breakdown voltage

TEST WITH GATE & SOURCE SHORT CIRCUITED

The measurement conditions of all the devices are:

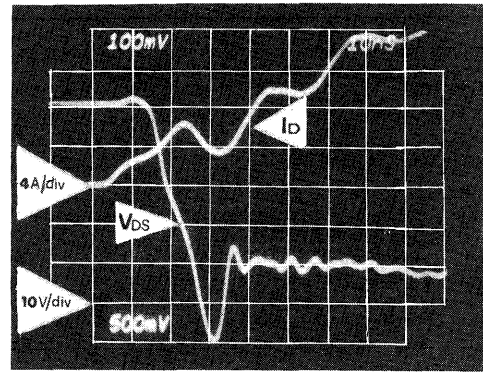
a) $Z_{GS} = 0$
b) $V_{DS} = 0.9\ V_{(BR)\ DSS}$
c) DUT = turned-off

The gate is short circuited to the source in order to switch-on only one of the parasitic bipolar transistors.

The maximum value of dV/dt reached when the DUT is connected in the circuit is shown by the upper limit of the shaded part of the graph in fig. 7. The part below it represents the safety limit of the SGS-THOMSON device.

Photograph 1 shows the voltage-current waveforms for SGSP221 when it switches on its parasitic transistor. In this case the device is not destroyed, as the V_{DS} is limited to a voltage of 40V, when $V_{(BR)DSS}$of the POWER MOSFETs is 65V.

Photo 1 - Drain current and voltage waveforms for SGSP221 on turn of its parasitic transistor



I_D = 10/A/div.; V_{DS} = 10V/div.; 5 ns/div.

It must also be mentioned that the large drain current also circulates in the active POWER MOSFET and could destroy it. Photo 2 shows the waveform of V_{DS}, I_D for SGSP478 under a dV_{DS}/dt of 50V/ns.

Fig. 8 - Turn-on of the parasitic transistor on SGSP221

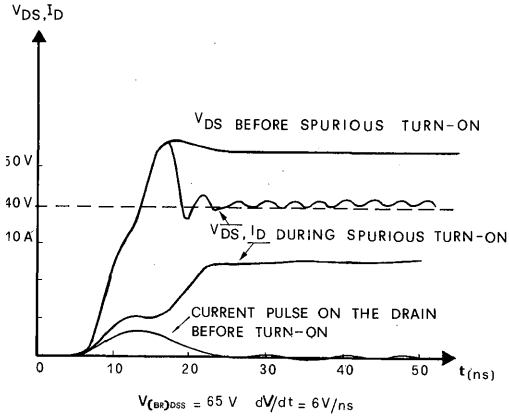
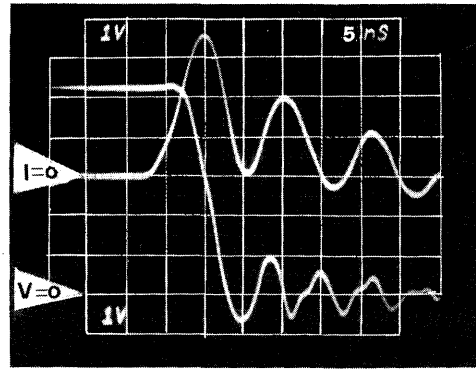


Photo 2 - Drain current and voltage waveforms for SGSP478



V_{DS} = 100V/div. I_D 5A/div. 5ns/div.

TEST WITH GATE & SOURCE NOT IN SHORT CIRCUIT

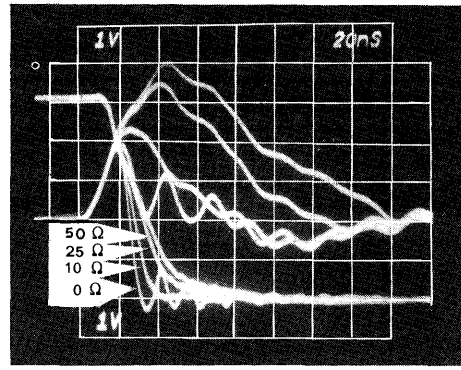
Photos 3 and 4 show the V_{DS} voltage and I_D current waveforms for both SGSP478 and SGSP221 when the impedance Zgs between the gate and source varies, while maintaining the driving conditions of the active POWER MOSFET constant and at the maximum V_{DS}.

With Zgs > 0 the D.U.T. can conduct as in the case of spurious turn-on of the POWER MOSFET transistor.

Conduction in POWER MOSFETS tends to limit the dV/dt which has caused the stray turn-on. Their switching time therefore increases and a large current passes during the transition, this avoids the turn-on of the parasitic transistor, due to the reduction of dV/dt, but unfortunately there is a large increase in the switching losses.

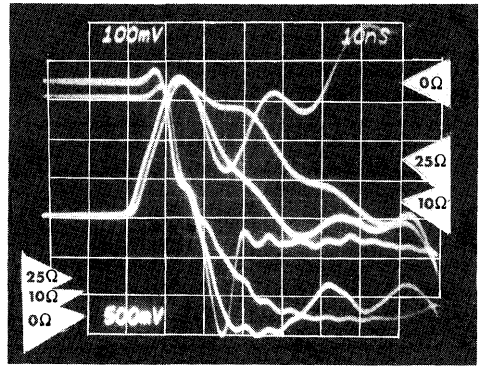
In photo 4 it can be seen that Zgs = 0, the parasitic transistor is turned on and that the insertion of Zgs = 10ohm eliminates this effect.

Photo 3 - Drain source voltage and drain current waveforms for SGSP478



V_{DS} = 100V/div.; I_D = 8A/div.; 20ns/div.

Photo 4 - Drain source voltage and drain current waveforms for SGSP221



V_{DS} = 10V/div.; I_D = 4A/div.; 10ns/div.

CONCLUSION

It has been seen that a POWER MOSFET stressed by a very fast slew rate can cause malfunction in the circuit or even destroy the device because of:

— stray turn-on of the POWER MOSFET itself

— turn-on of the POWER MOSFET parasitic transistor.

The critical value of dV_{DS}/dt at the turn-on of the parasitic bipolar transistor does not depend on the external circuit, but on the structure of the POWER MOSFET. SGS-THOMSON POWER MOSFETs resist dV/dt stress due to optimization of their design (resistance between base and emitter of the bipolar transistor reduced to a minimum). The destructive values of dV_{DS}/dt are difficult to attain in practical applications, since they exist when switching times are in the order of 5ns.

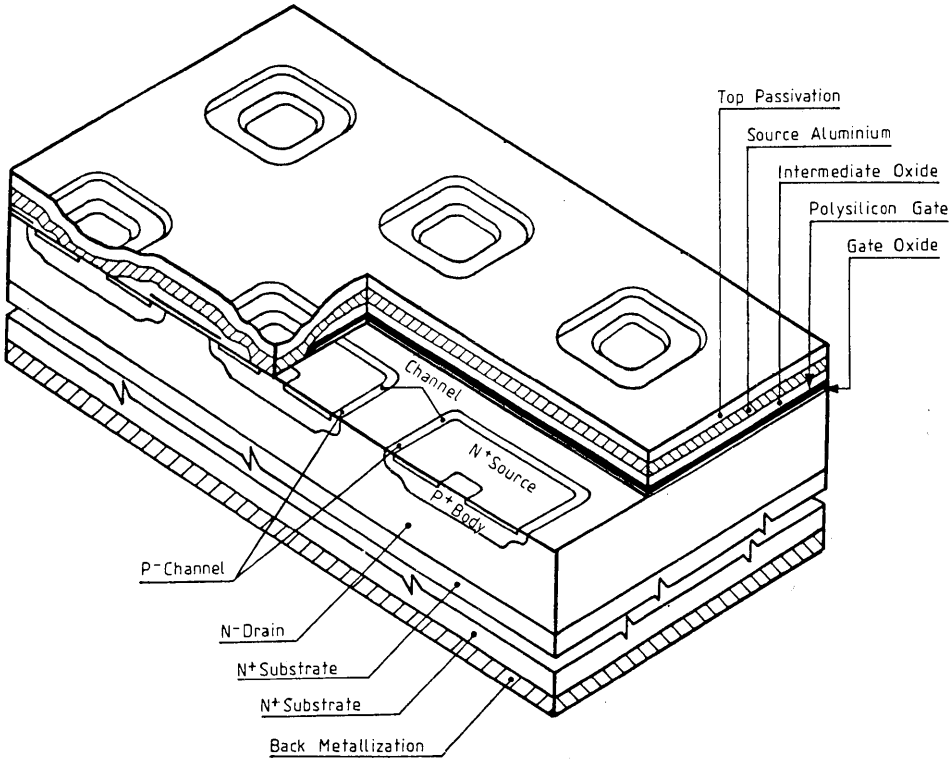
The stray turn-on of POWER MOSFET can occur at lower values of dV_{DS}/dt. These values depend on the values of impedance between the gate and source. This type of conduction does not damage the POWER MOSFET but increases losses in switching. This can be avoided by:

— Limiting the switching speed

— Driving the POWER MOSFET with a low input impedance.

HIGH DENSITY POWER MOSFETS

Fig. 1 - SGS POWER MOSFET structure

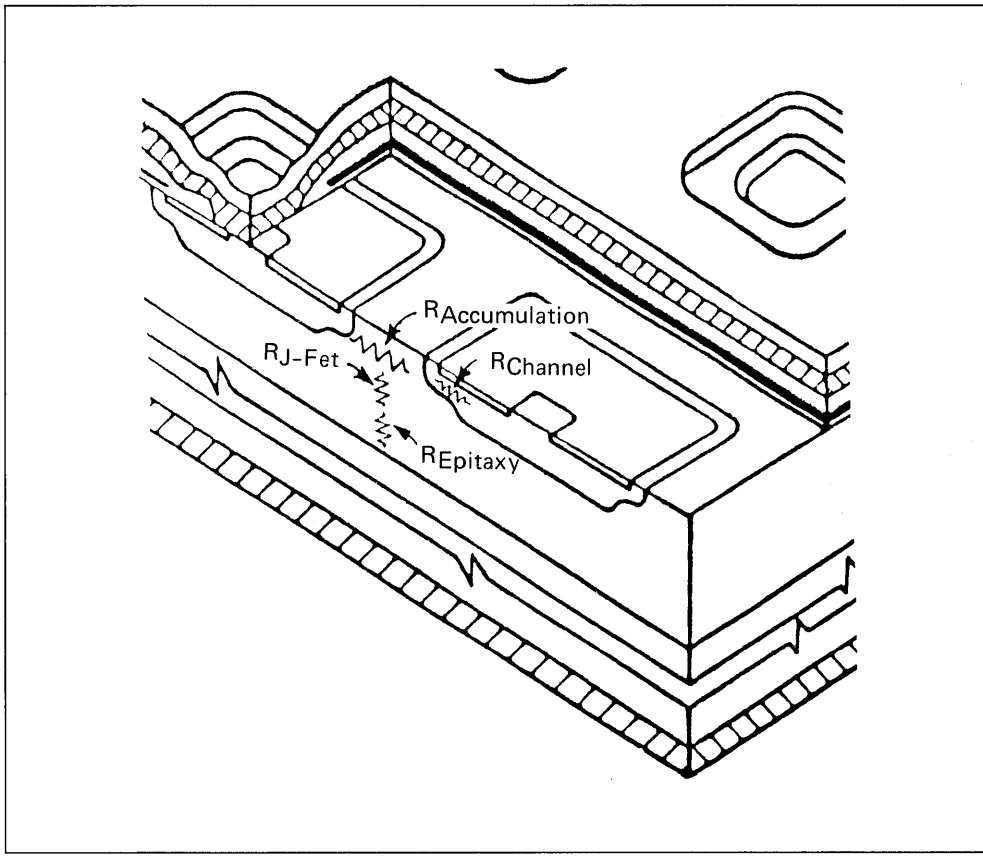


INTRODUCTION

POWER MOSFET transistor are fabricated using VLSI technology. A simple chip contains thousands of identical cells. By optimising the geometry of the VLSI design it is possible to achieve HIGH DENSITY POWER MOSFET transistors. An increase in cell density gives an improved operation together with a reduction of silicon area.

In order to fully appreciate high density POWER MOSFETS it is necessary to examine the factors controlling their output characteristics. Figure 2 shows the area associated with each resistive element contributing to the total on-resistance.

Fig. 2 - Resistive elements in SGS POWER MOSFETS structure



The on-resistance of a POWER MOSFET is made up of four separate terms:

$$R_{ON} = R_{CH} + R_{ACC} + R_{JFET} + R_{EPI}$$

where: R_{ON} = device on-resistance
R_{CH} = channel resistance
R_{ACC} = resistance of accumulated region
R_{JFET} = junction FET resistance
R_{EPI} = drain epitaxial layer resistance

R_{CH}, R_{ACC}, and R_{JF} depend primarily on the layout of the device. R_{EPI} depends on the structure of the drain.

Figures 3a and 3b show the relationship between the on resistance and the cell spacing for devices with a 100V and 500V breakdown voltage respectively.

It can clearly be seen that there is an optimum cell sapcing of about 12 μm for low voltage devices and 30μm for high voltage. Moreover, in high voltage devices the resistance of the drain epitaxial layer is the most significant of the four terms. The most effective way of obtaing a lower R_{ON} is to make the higher $V_{(BR)\,DSS}$ compatible with the drain resistivity. SGS-Thomson uses an edge termination structure that gives a breakdown voltage near the theoretical value.

For low voltage devices R_{ON} can be reduced by varying the channel and/or accumulation resistance.

Fig. 3 - Influence of the inter-cell spacing on the $R_{DS\ (on)}$ elements

Fig. 3a - Low voltage case $V_{(BR)\ DSS}$ = 100V

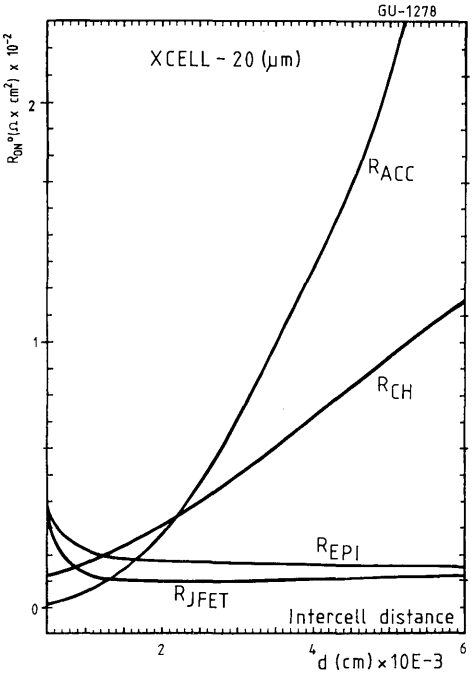
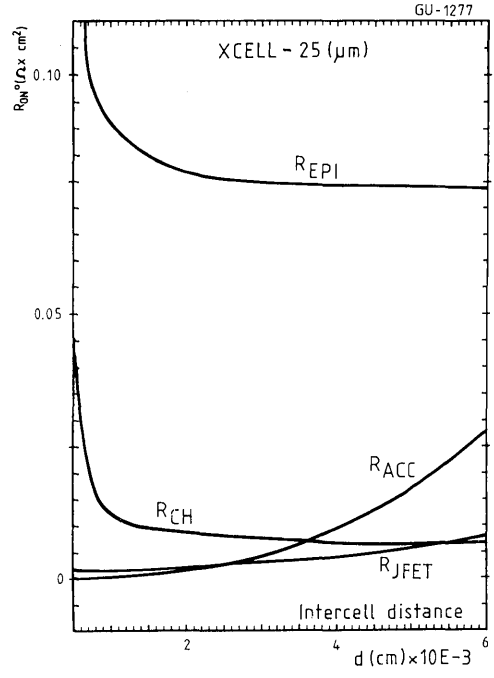


Fig. 3b - High voltage $V_{(BR)\ DSS}$ = 500V



From the expressions:

a) $$R_{CH} = \frac{L_{CH}}{\mu\,(V_G) \cdot W \cdot C_{OX} \cdot (V_G - V_T)}$$

b) $$R_{ACC} = \frac{D/2}{3 \cdot \mu\,(V_G) \cdot W \cdot C_{OX} \cdot (V_G - V_{TACC})}$$

where: μ = carrier mobility
W = channel perimeter
l_{CH} = channel length
C_{OX} = capacitance of oxide per area unit
D = Inter-cell distance

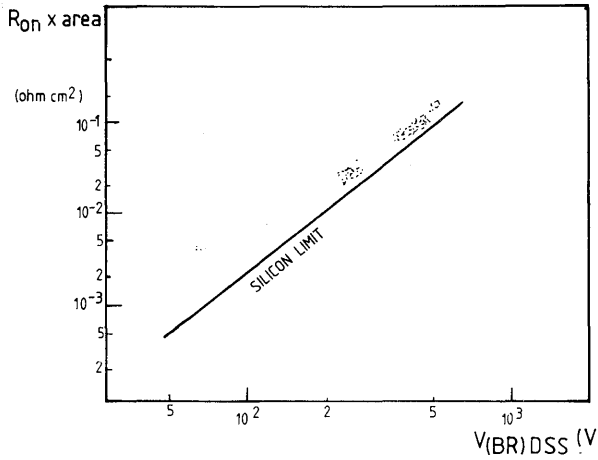
It follows that a reduction of dimensions L_{CH}, D, and the increase of W leads to a large reduction of both R_{ON} for cell densities from 500K cells/inch sq. to 10 milion cells/inch sq. for $V_{(BR)\ DSS}$ = 60V.

Table 1

Cell density (N. Cells/inch.sq.)	R_{CH}	R_{ACC}	R_{EPI}
558K	18.5	11.8	0.144
1.333M	11.9	4.9	0.125
3.82M	2.7	1.9	0.107
10M	1.42	0.59	0.09

VLSI technology offers the possibility of fabricating these high cell densities.
Fig. 4 shows on resistance per unit area for SGS-Thomson devices over a voltage range from 50V to 700V.
The continuous line represents the theoretical limit of silicon, without conductivity modulation.
For low voltage devices, where the divergence from the theoretical limit is the greatest, the performance can be improved by modifying the design rules of the horizontal geometry.

Fig. 4 - $R_{DS\ (on)}$ vs. breakdown voltage



SGS-Thomson STATE-OF-THE-ART

SGS-Thomson uses a cell density of 558K cells/inch sq. in its standard low voltage technology. Recently, another technology with a cell density as high as 1.33 milion cells/inch sq. been developed(1), and devices are now in production.

For comparison between the two technologies fig. 5 and photos 1 and 2 show two devices with breakdown voltages of about 60V and an on-resitance of about 0.04Ω, one with the standard cell and the other the high density structure.

The chips in the device produced with the standard technology are 180 x 220 $mils^2$ in area; those produced with the new technology are 170 x 170 $mils^2$.

There are both static and dynamic advantages to be gained from using high density devices. Their static characteristcs such as R_{ON}, capacity, and their dynamic characteristcs such as switching times, energy per cycle and gate charge are improved.

Photo 1 - SEM photo of high density POWER MOSFET - 1.33 million cells in^{-2}

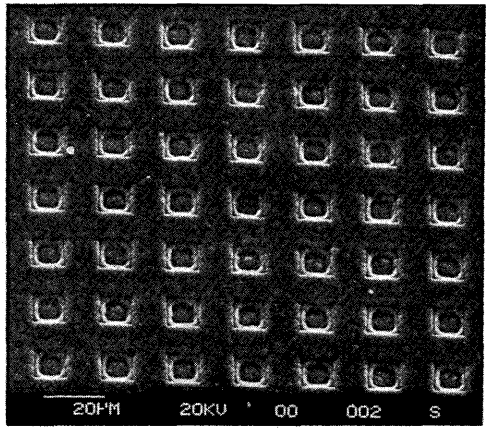
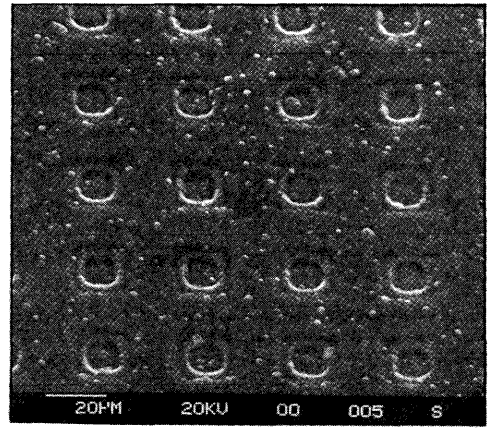


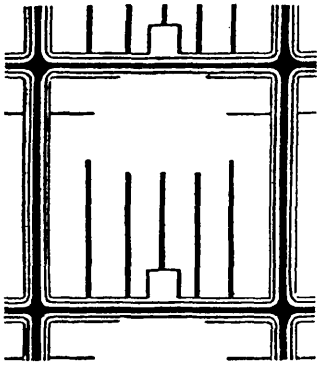
Photo 2 - SEM photo of standard POWER MOSFET - 550K cells in^{-2}



Note 1: See additional information on page 104

Fig. 5 - Dice comparison

a) High density POWER MOSFET



b) Standard POWER MOSFET

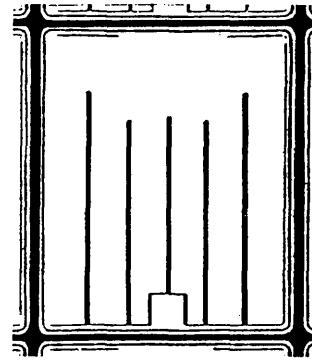
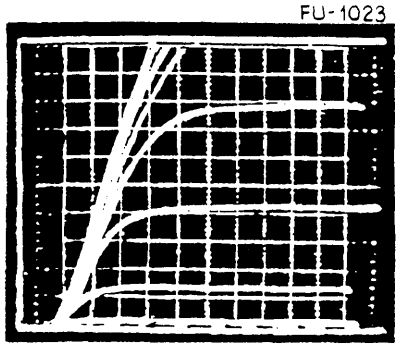
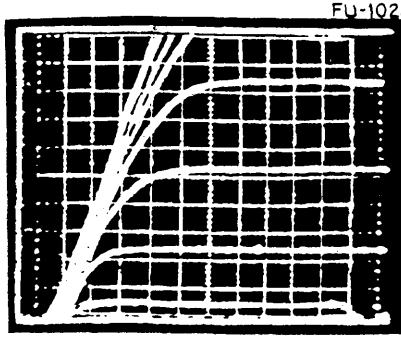


Fig. 6 - Output characteristics



I_{DS}
V_{DS}
V_{GS}

High density POWER MOSFET
5A/div
500mV/div
1V per step



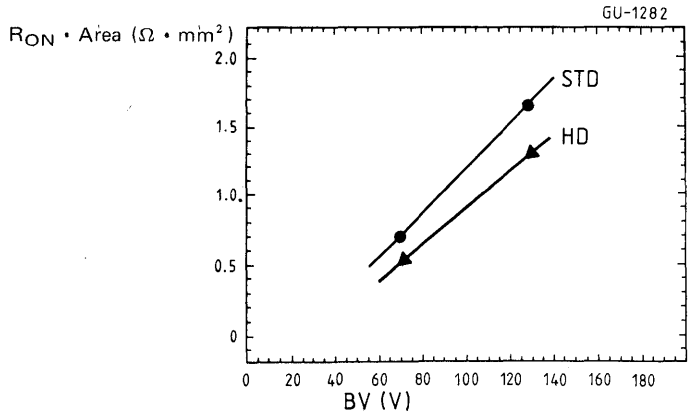
I_D
V_{DS}
V_{GS}

Standard POWER MOSFET
5A/div
500mV/div
1V per step

STATIC CHARACTERISTICS

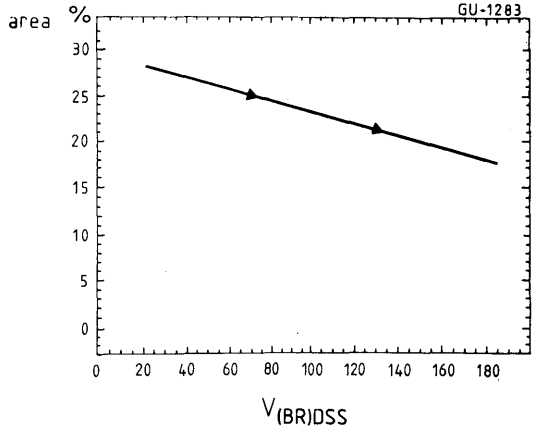
The on-resistance per unit area of a POWER MOSFET chip is an index of the optimization of the silicon; the channel perimeter and reducing the inter-cell distance are the most important factors in reducing the on-resistance.
A figure of merit, R_{ON} - AREA, allows a comparison of technologies. Fig. 7 compares the values of R_{ON} · AREA for both technologies.

Fig. 7 - Behaviour of R_{ON} area vs. breakdown voltage.



As predicted, the increase in efficiency, as the cell density increases, becomes less as the breakdown voltage increases. This is due to the increase in the resistance on the drain (R_{EPI}). The chip area for high density devices is reduced by 25% at 70V breakdown and 21% at 130V breakdown compared to standard POWER MOSFET devices. Figure 8 shows the decrease in chip efficiency whith the increase in voltage.

Fig. 8 - Decrease in efficiency as breakdown voltage rises



DYNAMIC CHARACTERISTICS

Although not as obvious the effect of the cell density on the dynamic characteristic is just as interesting. In switching applications, the gate charge in a POWER MOSFET device is of fundamental importance in evaluating both the driving energy and

the switching time. The total energy required by the gate for switching depends on various parameters, which are mainly electrical (supply voltage, drain current, gate voltage) or structural (reverse capacitance, gate thereshold voltage, transconductance).
The electrical parameters are external and depend on the type of application. The structural parameters, instead, depend on the device itself and can be varied by optimizing its design.
Using the electical configuration shown in fig. 9 it is possible to examine the device gate charge.
Fig. 10 shows the comparison between the gate charge curves of devices with the same static characteristics but with different cell densities.
The total gate charge for high density types is about half that of standard POWER MOSFETS.

Fig. 9 - Gate charge test circuit

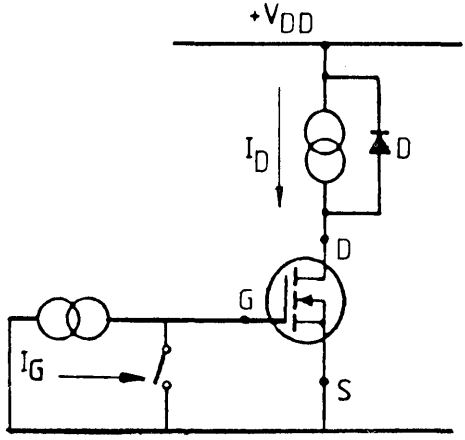
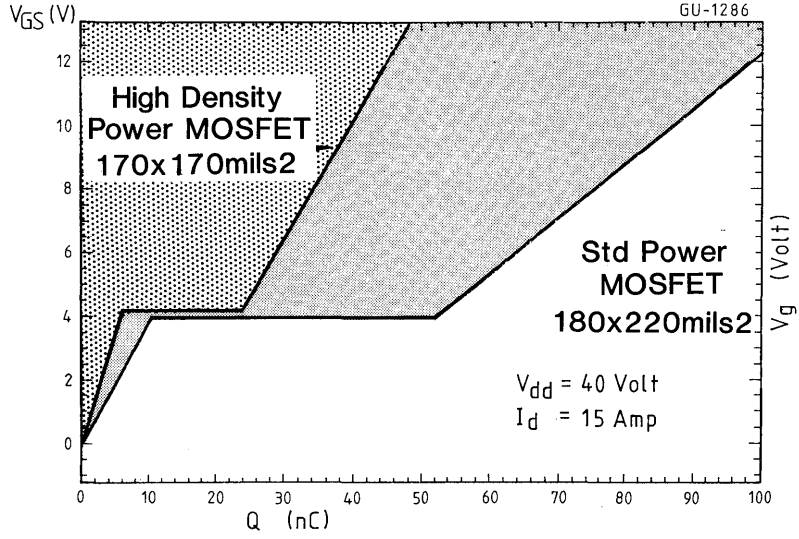


Fig. 10 - Gate charge curve



The relation between the gate charge curves and the dynamic characteristics of the devices is defined in figure 11. The $I_d - V_d$ characteristics in switching are strongly correlated to different slopes of the gate charge curves.
Analyzing the gate charge we can consider that:

1) the initial steep slope depends on the input capacitance C_{iss}. Reducing C_{iss}, the slope increases
2) the horizontal part of the curves depend on C_{RSS} and G_M
3) the third part of the slope is again due to C_{GS} which in turn is related to the geometry

Fig. 11 - Dynamic characteristics vs. gate charge

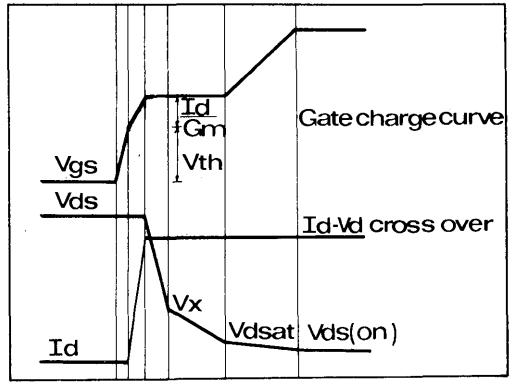
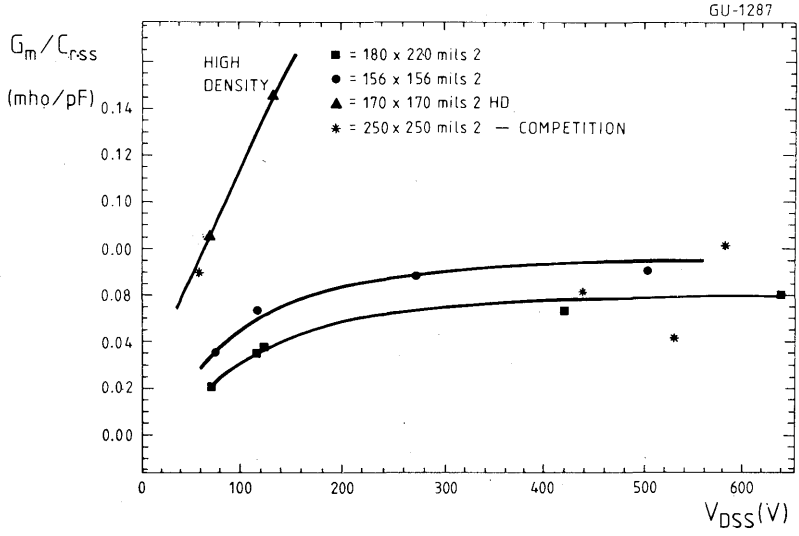


Fig. 12 - Quality factor K vs. breakdown voltage



It is obvious that for a given driving circuit resistance, the switching times and the cross-over energy losses are strongly defined by the gate charge curves. The most significant parameter for switching performance is C_{rss}.
The drive energy, ($Ep = \int V_G (Q) \cdot d_Q$), is represented by the area under the curve. The switching time and consequently the energy dissipated at cross-over, is related to the width of the flat section of the gate charge curve. From this it can be deduced that the optimum device must have a low C_{RSS} and a high G_M. By introducing a second merit coefficient $K = G_M/C_{RSS}$, the efficiency of the device in dynamic working conditions can be calculated.
In order to increase the merit factor K, is necessary to increase the transconductance and decrease the reverse capacitance. The best way to improve the transconductance is to increase the perimeter of the channel, i.e. by increasing the cell density.

C_{RSS} can be decreased by reducing the overlap area between the gate and drain, that is by reducing the distance between each cell.

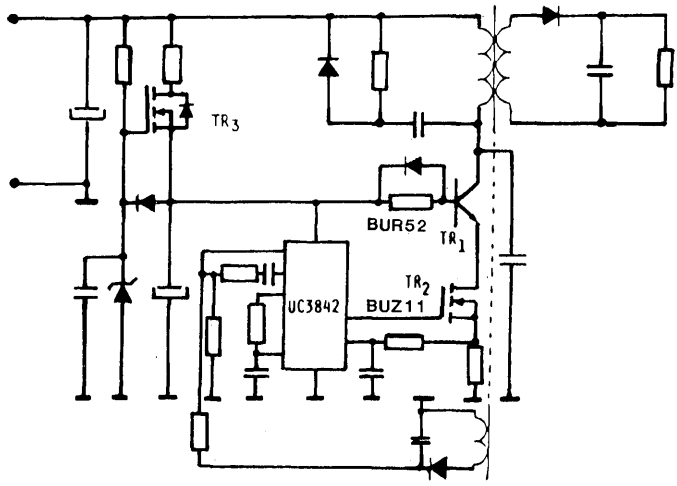
Both these actions lead to an increase in the cell density.

Fig. 12 shows the value of K (for equal areas) as a function of the breakdown voltage, $V_{(BR)\,DSS}$, for POWER MOSFET devices produced by both standard and high density technology.

Thermal measurements on both standards and high density POWER MOSFET were made using the circuit in Fig. 13.

The circuit is designed around an emitter switching configuration working at 100KHz with 50% duty cycle and I_D = 10A.

Fig. 13 - Emitter switching circuit



The power dissipation of the POWER MOSFETS devices were approx 8W for BUZ11 and 6W for high density BUZ11. The power dissipation depends on two factors:

$$P_{on-state}\ \text{loss} = I_d^2 \cdot R_{on}(T) \cdot d$$

$$P_{crossover}\ \text{loss} = f \cdot \int V_d \cdot I_d \cdot d_t \cdot$$

The on-state power dissipation is the same for both devices. The second term, depending on the cross-over point of the switching waveforms for the devices causes the difference in power dissipated. Considering that the junction to ambient, thermal resistance $R_{thj\text{-}amb}$, with heatsink, is 13°C/W, the devices reach a working junction temperature of 104°C + $T_{(amb)}$ and 78°C + $T_{(ambient)}$ respectively. Under conditions where T_{amb} = 50°C the standard device is operates outside the maximum thermal ratings while the high density device remains within the thermal safe operating area.

CONCLUSION

Table 2 lists some of the significant advantages the introduction of high cell density in SGS-Thomson POWER MOSFETS offer.

Table 2

	Standard	high density
Energy loss/cycle (μJ)	45	25
C_{rss} (pF)	420	140
G_m/C_{rss} (mho/pF)	0.028	0.085
Q_g (nC)	56	38

A reduction of the input capacitance decreases the driving energy with consequent cost reduction of the drive circuitry.

The improved dynamic characteristics, due to feedback capacitance reduction increases the maximum operating frequency.

An increase of the safe operating area is obtained by thermal improvement.

VERY HIGH DENSITY

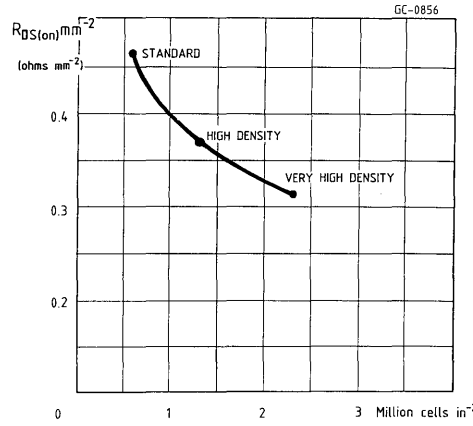
This article would not be complete without reference to this latest addition to the SGS-Thomson POWER MOSFET devices.

The most recent advance in our high density technology is the introduction of the very high density cell structure with a cell density of 2.3 million cells per square inch. This gives a further improvement in device static and dynamic performance and an even smaller chip area for a given current rating than chips with 1.3 million cells per square inch. The photographs show the very high density cell structure compared to the standard 550k cells in^{-2}

Table 3 compares the STVHD90 with 2.3 million cells/in^2 and chip size of 180 x 220 $mils^{-2}$ to a standard 550k cells in^{-2} with a chip size of 180 x 220 $mils^{-2}$.

	STVHD90	SGSP386
cell density/in^2	2.3	550
chip size ($mils_2$)	180 x 220	180 x 220
$R_{ds\ (on)}$ (milliohms)	23	40
C_{iss} (pF)	3000	1800
C_{oss} (pF)	1000	1100
C_{rss} (pF)	180	550
Gate charge (nC)	47	74

The static characteristics are very much improved as $R_{DS\ (on)}$ is reduced 23 milliohms, see figure 14.



Cell density versus $R_{DS\ (on)}$ mm^{-2}

Photo 1: 2.3 million cells in^{-2}

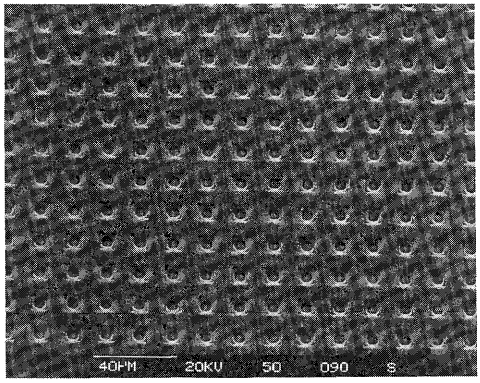
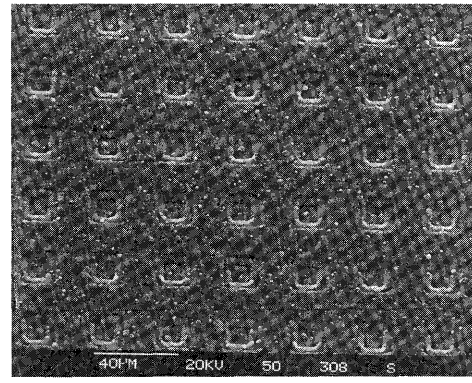
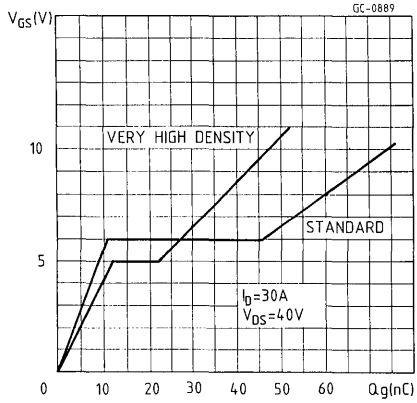


Photo 2: 550k cells in^{-2}





Gate charge: Very high density compared with an equal area chip with the same breakdown voltage

The dynamic characteristcs for switching are also improved in the STVHD90. This can easily be seen from the comparison of the gate charge curves, STVHD90 versus the standard type, figure 15. The flat section of the graph is very reduced hence reducing the switching time and gate drive energy. This is due do lower reverse capacitance, C_{RSS}, and higher trasconductance, g_{fs}, in the STVHD90.

HIGH VOLTAGE TRANSISTORS WITH POWER MOS EMITTER SWITCHING

INTRODUCTION

This paper summarizes the results of an investigation carried out on power devices with both MOS and BIPOLAR parts working together in the same circuit. The "emitter drive" configuration was considered, with switching power supply applications in mind.

The devices used are:

Power MOS:	SGSP321, SGSP352
Bipolar transistors:	BUV48, BU508A
Ultrafast bipolar transistors:	SGSD00035
(Hollow Emitter)	SGSD00039
Fast darlingtons:	SGSD00031, BU810

In the case of flyback switching power supplies a practical example is also described.

CIRCUIT DESCRIPTION

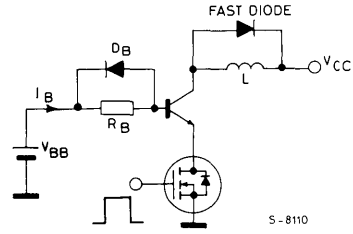
The term "emitter switching" describes a circuit configuration where a low voltage transistor (MOS or Bipolar) switches off the emitter current of a high voltage transistor, and consequently the transistor itself.

This configuration combines the fast switching of a low voltage device with the high power switching of a high voltage device, since:
high current × high voltage = high power switching.

The combination of a high voltage bipolar and a low voltage Power MOS is preferable due to the high switching speed and the low driving energy of the combined power switch.

The base of the high voltage bipolar device is driven by a constant voltage source. The energy dissipated to drive the high voltage bipolar device depends on the losses that the forward bias current I_{B1} generates in the resistance in series with R_B, $I_{B1}^2 \cdot R_B \cdot t$. This power dissipation can only be reduced by using high gain transistors or darlingtons.
(See fig. 1)

Fig. 1 - The basic circuit used for the evaluation of the emitter switching system. The base drive circuit used is shown for comparison



The diode in series with the base serves to clamp the base overvoltage at turn-off.

The two transistor stage is driven by the gate of the low voltage Power MOS. Very low driving energies, about 180nJ per cycle, are involved in the charging of the input capacitances.

Consequently the stage can be directly driven by the output of suitable linear integrated circuits.

The possibily of direct driving by an IC output together with the excellent switching speed make this configuration extremely suitable for switching power supplies at frequencies of 50kHz or higher.

CIRCUIT OPERATION

As we have seen, the forward base current I_{B1} is fixed by the external circuitry:

$$I_{B1} = \frac{V_{BB} - V_{BEsat} - V_{DSon}}{R_B}$$

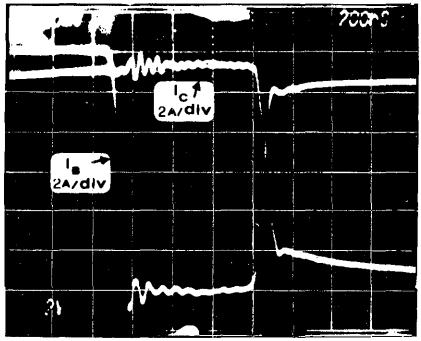
The collector current instead depends on the load, and in general, varies with the time.
The turn-on and turn-off phases can be analysed separately.

TURN-OFF

When the driving signal to the Power MOS is low the drain current is interrupted and the emitter cur-

rent of the high voltage bipolar falls to zero. The emitter reaches the base voltage and will not carry any more current. As a result the collector current can only flow through the base, becoming a reverse base current that depletes the base to collector junction. This reverse base current I_{B2}, from the moment when the emitter current disappears, coincides with the collector current. See photo 1. The stored charge is removed in a typically very violent, and consquently rapid manner.

Photo 1 - Base and collector current at turn-off



As a result the storage time is substantially reduced.
The fall time, which is related to the recombination under the emitter, is also generally reduced.
Typical values for the fall and storage time of the SGS-Thomson devices used in the test are shown in Table 1, for both emitter and the base drive circuits.

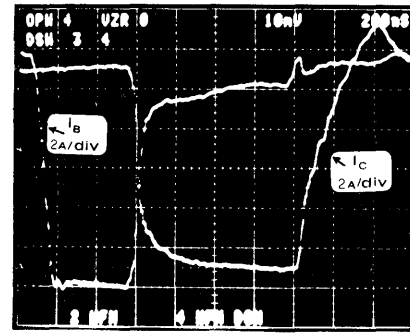
Table 1 - Typical t_f and t_s on inductive load

Device	I_C(A)	EMITTER SWITCHING		BASE SWITCHING	
		$t_{storage}$	t_{fall}	$t_{storage}$	t_{fall}
BUX48	10	500ns	100ns	2μs	200ns
BU508A	5	800ns	300ns	6μs	400ns
SGSD00031	10	400ns	100ns	1.2μs	100ns
BU810	5	300ns	150ns	800ns	150ns
SGSD00035	10	300ns	50ns	800ns	50ns
SGSD00039	5	300ns	40ns	700ns	50ns

TURN-ON

When the Power MOS is the on state, the bipolar device also starts conducting. The dynamic behaviour (See Photo 2) does not differ in any substantial way from the usual case of the base drive.

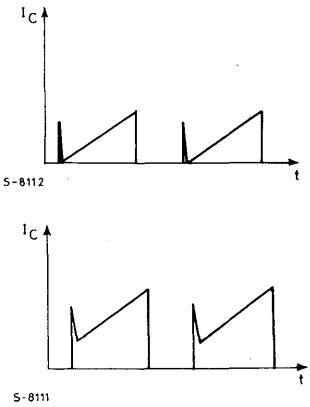
Photo 2 - Base and collector current at turn-on



The dynamic saturation transient $V_{CEsat\ dyn}$ is also practically the same with a base drive as with an emitter drive. The collector current, when the collector load is the primary winding of a switching transformer, can vary according to two possibilities. (See Fig. 2)

a) After the initial peak due to the recovery of the diode present on the secondary winding, the collector current increases linearly starting from zero
b) After the same initial peak, the collector current increases linearly starting from the value memorized in the magnetic circuit at the end of the previous cycle.

Fig. 2 - Collector current waveforms with varying load



REVERSE BIAS SAFE OPERATING AREA

A problem that occurs in bipolar transistors is damage caused by "current crowding".

Fig. 3a illustrates current flowing in a typical bipolar device. Fig. 3b shows how, when the device is turned off and the current begings to die away, the current focuses with a high concentration under the emitter. This high current density can damage or destroy the transistor.

Fig. 3a

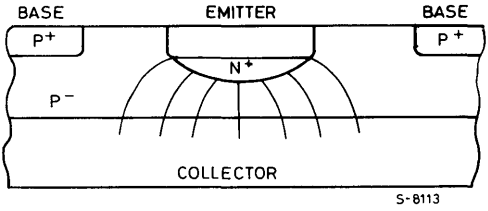
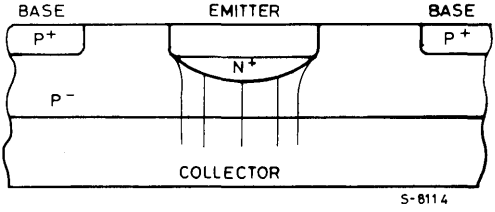


Fig. 3b



The energy dissipated within a bipolar power transistor at turn-off can be found graphically from a plot of I_C versus V_{CE} at turn-off. Three cases are shown in Fig. 4a, b and c. The shaded area is proportional to the energy that is dissipated in the device during turn-off.

Consequently turn-off times affect the SOA of the device, (Fig. 5b). These problems can be overcome using emitter switching.

Fig. 4a - Slow turn-off. No crowding but high average heating

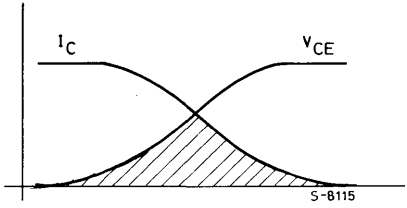


Fig. 4b - Fast turn-off. crowding with low average heating but possible high peak power

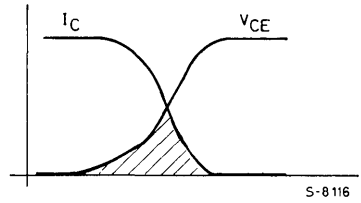
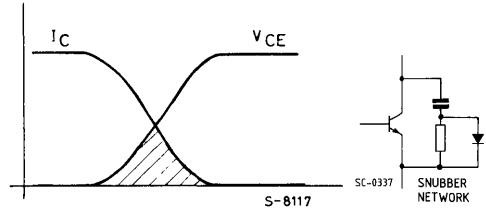


Fig. 4c - Fast turn-off (with V_{CE} delayed by snubber network)



The way the stored charge is swept away in the high voltage bipolar device when it is driven by the emitter, produces some interesting consequences.

The stored charges are evacuated through the base contact when the emitter current is zeroed and not later than a few tens of nanoseconds after the beginning of the storage interval. Consequently, during the turn-off, no charge is injected from the emitter into the base. Although the reverse base current is quite relevant, no focusing of the current in the centre of the emitter fingers takes place.

The bipolar device therefore exhibits an energy absorbing ability at the turn-off RBSOA that is substantially higher than if a normal base drive were used. With a base drive the emitter would inject charges and the voltage drop across the distributed base resistance would induce the "emitter crowding" phenomenon.

The practical evidence for all the transistors investigated (BUV48, BU508A, SGSD00035, SGSD00039) shows that the reverse bias operating area (RBSOA) extends righ up to the BV_{CES}! (See fig. 5).

This extreme effect is unfortunately much less pronunced when using fast darlingtons. The higher complexity of the charge extraction mechanism and the charge injection from the emitter into the base

in the driver transistor imply that the RBSOA extension is almost irrelevant

Fig. 5a - reverse bias safe operating area

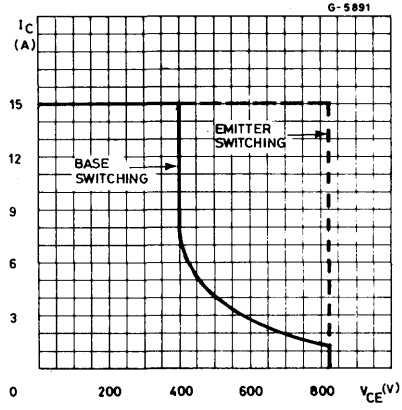
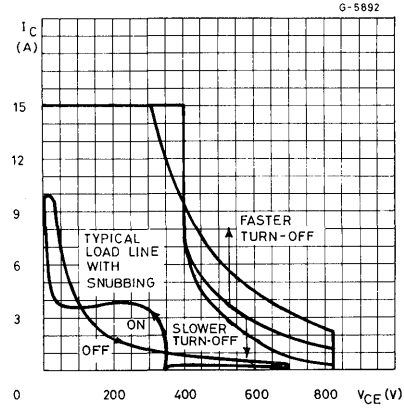


Fig. 5b - How reverse bias safe operating area changes for:
i) slow turn-off
ii) fast turn-off



A POSSIBLE APPLICATION

A possible application of the "emitter switching" configuration is shown in Figure 6, where a switching power supply operating in a "flyback" mode has been implemented.

The basic criteria used in choosing the value of the circuit elements are given below. The purpose of the study was to demonstrate the feasibility and to evaluate the advantages. Exact circuit element values can be further optimized, especially in the case of the transformer.

The power source in the mains singlephase, 220V a.c., and the switching frequency can be set to 50KHz or more.

The devices used were:

Q1: fast darlingtons with $BV_{CES} \geqslant 600V$ for 110V line
—SGSBU810 for current up to 5A
—SGSD0031 for current above 5A
Fast transistor with $BV_{CES} \geqslant 800V$ for 220V line
—SGSD00039 for currents up to 5A
—SGSD00035 for current up to 10A

Q2: Low voltage POWER MOS ($BV_{DSS} = 50V$)
—SGSP352 for currents up to 5A
—SGSP322 for currents over 5A

Q3: High voltage, low current POWER MOS $V_{(BR)\ DSS} < = 450V$)

Control IC: UC3842

DZ2: Zener diode 2W/20V

D1: 25V diode, with I_c peak rating as high as 10A for 500ns

C6: Electrolytic capacitor, 100μF, 25V. It absorbs possible variations of V_{BB}.

R3: Resistor setting the forward bias base current of the darlington:

$$R3 = \frac{V_{CE} - V_{BE\ sat} - V_{DSon} - R_7\ I_D}{I_{B1}}$$

Its power rating must exceed $R3 \cdot I_{B^2} \cdot t$ (in practice 3W)

R7: Shunt resistor to sense the switch current. The over current $I_{S\ max}$ protection is set according to

$$R7 = \frac{1V}{I_{Smax}}$$

C4,R6: RC network, filtering the disturbances induced by the switching transients on the I_{Smax} protection input.

C3,R5: RC network, setting the switching frequency and the maximum duty cycle, according to the UC3842 data sheet.

$t_{charge} = 0.55\ R_5\ C_3$

$t_{discharge} =$

$= R_5 \times C_3\ \ln [(6.3\ R_5 - 2.7)/(6.3\ R_5 - 4)]$

$f = 1/(t_c + t_d)$

R8,R9: Resistive divider of the feedback voltage from a secondary sense winding, recitified by D5 and C5. The divided voltage is compared by the control IC to an internal reference of 2.5V.

C2,R4: Compensating network in the error amplifier of the feed-back voltage.

R1: Resistor biasing the Q3 gate (1.2 MΩ, 1/4 W)

R2: Resistor that limits the inrush current through the POWER MOS, Q3, at the turn-off (1.2Ω, 2W)

D4: Fast recovery diode
Its voltage/current ratings depend on the particular secondary winding it rectifies.

D5: Low current/low voltage diode

D3,R10, C8: Snubber network (Fig. 6 shows just one of the possible configurations).

$$C8 = \frac{L_d \, I_c^2}{V_{DS}^2}$$

$R10 = 1/4fC8$

$P(R_{10}) = 1/2 \, L_d \, I_D^2 \cdot f$

where:

f = switching frequency

L_d = stray inductance of the transformer

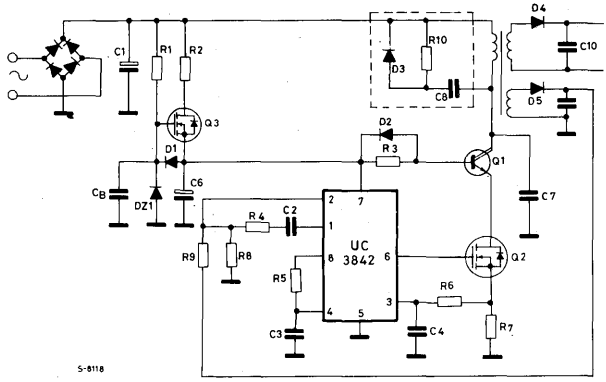
V_{OS} = maximum voltage overshoot admitted

D3: A 400V fast recovery diode

C7: The use of a capacitor reduces the crossover of the Darlington (3 to 6nF)

It is important to note that, the power transistor Q3 acts only at the turn-on of the power supply and when the capacitor C6 supplies more energy to the base of the darlington and to the supply input of the IC than is returned to C6 during the turn-off of the darlington, Q1.

Fig. 6 - "Emitter switching" circuit



CONCLUSION

The "emitter drive" configuration exhibts some clear differences with respect to the usual "base drive" configuration, and they can be particularly useful in switching power supply applications:

— Substantial reduction of the storage time and improvement of the fall time.

Switching frequencies of 50kHz and higher are possible

— The dynamic drive circuitry is simplified. The negative voltage supply is not required to remove the stored charge from the base. The energy needed to drive the gate of the POWER MOS is very low (180 nJ per cycle).

— Extremely high ruggedness at the turn-off of the inductive load (i.e. very large RBSOA) if the high voltage bipolar part is a transitor.

— Higher power dissipation in the on-stage, due to the additional losses in the POWER MOS ($I_D^2 \, R_{DS\,on} \, t_{on}$).

This last point is the only disadvantage, but it is more than compensated for if switching at high frequencies. The lower switching losses (a saving each cycle) can justfy the higher on-state losses (a fixed expenditure) as soon as the switching frequency is high enough, which is often the case in switching power supplies.

A WIDE RANGE INPUT DC-DC POWER CONVERTER

INTRODUCTION

This 300W DC-DC converter, shown in Fig. 1 has a flyback topology and works in continuous mode with single output and features primary side control.

The Power switch is designed around an emitter switching configuration. This arrangement uses three bipolar devices, BUX 12, and with POWER MOS device in cascode.

The pulse width modulation (PWM) controller is the SGSUC3840 linear integrated circuit. The characteristics of this IC are pulse by pulse current limiting with shut-down for short circuit protection, over and under voltage sensing with protective shut-down, soft start, voltage feed-forward for excellent line regulation (without regulation by feed back network). These facilities are used to advantage in this design.

CIRCUIT DESCRIPTION

A DC input voltage is chopped at a high frequency, 80KHz is possible.

This high switching frequency allows the use of a very small transformer with respect to the output power.

In the configuration, shown in Fig. 1, an additional low-voltage winding, N_B, (two turns on this transformer) is used to provide continuous operating power for the base of the bipolar power device.

The resulting base current is proportional to the load.

The polarity of the transformer windings is configured as a flyback converter. When transistor Q6 conducts, the output diodes are reverse biased and energy is stored in the primary inductance. When Q6 turns-off, the voltage polarity of the primary winding reverses and the stored energy is delivered to the output.

Fig. 1 300W DC-DC converter circuit diagram.

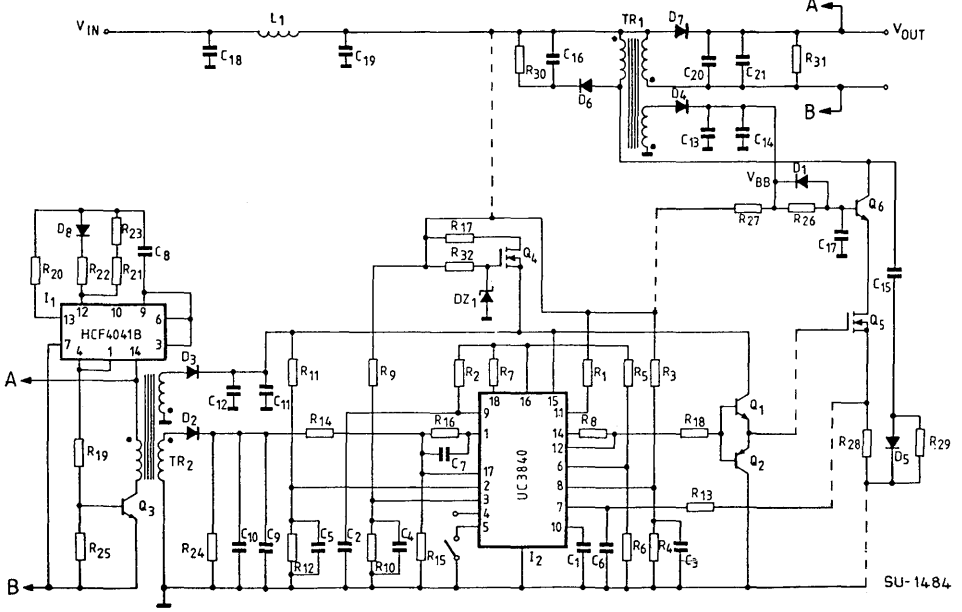


Table 1 - Power Supply Specifications

Operating mode	:	Flyback Contnuous Mode
DC Input Voltage	:	48V to 80V DC
Switching frequency	:	80KHz ± 10%
Output Power	:	300W
Output Voltage	:	12V ± 5%
Output Current	:	2 to 25A
Line Regulation	:	0.03%/V
Load regulation	:	0.17%/A (med. value)
Efficiency @ 300W		
V_{IN} = 48 V_{DC}	:	70%
V_{IN} = 80 V_{DC}	:	75%
Efficiency max @ 150W		
V_{IN} = 70 V_{DC}	:	80%
Output Ripple @ 25A	:	400mV

The power supply operates in continuous mode: the energy stored in the primary inductance is not completely transferred to the load during each cycle, for this reason the current in the primary winding has a trapezoidal waveform, Fig. 3.

The emitter switching configuration of the power switch allows the bipolar transistor to operate at higher frequencies since this technique gives a substantial reduction in the bipolar storage time. Other advantages are:

- The dynamic drive circuitry is simplified and the energy needed to drive the gate of the POWER MOS device is very low (800nJ per cycle).
- Greater ruggedness than in a single bipolar switch at turn-off with the inductive load. Consequently there can be smaller snubber networks and a higher leakage inductance in the transformer.
- The power dissipation during on time is lower than the on losses of a single POWER MOS device with the same characteristics (I_C, BV_{CE}) of the bipolar device.

For better load regulation with isolated output, a smaller converter (transformer Tr2 with a small signal transistor Q3, as a switch) is used instead of a feedback winding.

This converter, operating at a fixed frequency (160KHz) and duty-cycle, privides on the first secondary winding, N_f with forward polarity, a voltage proportional to the output regulating voltage, which is used as a feedback signal.

The other secondary winding of this converter (with flyback polarity) N_i, is used to provide continuous operating power for the UC3840 and the IRFZ42 gate drive.

Table 2 - Tr2 specifications

- Core	Siemens E20, N30
- Primary	N_p = 38 turns
- Feedback sec.	N_f = 30 turns
- Supply sec.	N_i = 56 turns

The start-up of the power supply is obtained by resistor R27 which supplies the transistor base and by the network (formed by POWER MOS device Q4, DZ1, R17, R32) which supplies the PWM circuit and IRFZ42 gate drive transistors Q1 and Q2. When the voltage on the secondary winding of Tr2 increases, the POWER MOS device, Q4, is automatically turned-off, Q4 a is low voltage, low current POWER MOS device: an SGSP301 was selected. It is interesting to note that the DC safe operating area of a POWER MOS transistor used under these conditions is greater than that of an equivalent bipolar device.

The circuit was mounted on two printed boards. Board 1 holds the control circuit and board 2 the power switch. Board 2 has a copper thickness of about 300μm. The high current areas are double sided.

TRANSFORMER

Designing the transformer leads to trade off decisions involving factors such as leakage inductance specifications, insulation, size, power dissipation, and cost.

The core selected for this power supply is a Siemens EC70-N27 with the following characteristics:

— Effective core Area A = 279 mm^2
— Saturation flux density @ 20°C = 470 mT
— Maximum working flux density B = 300 mT

The design starts with a calculation of the maximum duty cycle, Δ, and the maximum on time $T_{on\ max}$, Fig. 2.

With $V_{CC\ min}$ = 48V, V_{reset} = 45V, T = 12.5μs (80KHz).

The maximum duty cycle is;

$$\Delta = \frac{V_{reset}}{V_{reset} + V_{CC\ min}} = \frac{45}{45 + 48} = 48\%\ T_{on\ max} = 6\mu s$$

Eqn. 1

By equating the volts/second areas - the shaded areas in Fig. 2 the turns ratio can be calculated using the worst case as follows: (see Fig. 2).

$$n_{primary}\,(V_o + V_f) \cdot (T - T_{on\ max}) = n_{secondary}\,(v_{CC\ min} \cdot T_{on\ max})$$

$$n_{(p/s)} = \frac{V_{CC\ min} \cdot T_{on\ max}}{(V_o + V_f) \cdot (T - T_{on\ max})} = \frac{48 \cdot 6 \cdot 10^{-6}}{(12 + 1) \cdot 6.5 \cdot 10^{-6}} = 3.4$$

Eqn. 2

Fig. 2 - Switching waveforms at the collector of Q6

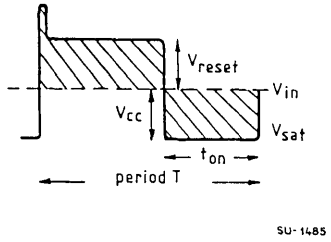


Fig. 3 - Current waveform in the primary inductance

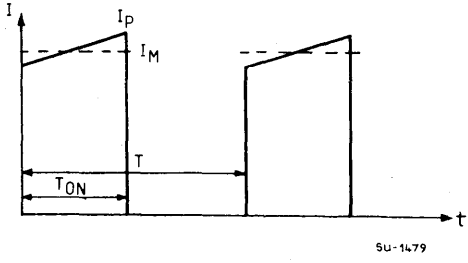


Fig. 3 shows the mean current value (I_{mean}) in the primary inductance during the on state. It can be calculated as follows using the minimum input voltage:

$$I_{mean} = \frac{P_{max} \cdot T}{\eta \cdot V_{CC\ min} \cdot T_{on\ max}} = \frac{300 \cdot 12.5}{0.7 \cdot 48 \cdot 6} = 18{,}6A$$

Eqn. 3

The primary inductance L_p can be calculated by fixing a maximum peak value for primary current I_p = 20A;

$$L_p = \frac{V_{CC\ min} \cdot T_{on\ max}}{2\,(I_p - I_{mean})} = \frac{48 \cdot 6 \cdot 10^{-10}}{2 \cdot 1.4} = 100\mu H$$

Eqn. 4

At full load and at $V_{CC\ max}$ we have

$$T_{on} = \frac{n \cdot (V_o + V_f) \cdot T}{V_{CC} + n\,(V_o + V_f)} = 4.4\ \mu s$$

Eqn. 5

The flux balance in the transformer core depends on equal volts-second products being applied during charge and reset phases.

$$I_{man}\ (@\ 80V) = \frac{P_{max} \cdot T}{n \cdot V_{max} \cdot T_{on\ min}} = 16A$$

I_p = 17.1A

With an air-gap, g = 3mm, then Al = 140nH, N_p can be calculated as follows:

$N_p = \sqrt{}$ L/Al (from manufactures data book)

Eqn. 6

$$N_p = \sqrt{100 \cdot 10^3\ nH/140nH} = 27\ turns$$

The minimum air gap with working flux density B = 250mT is:

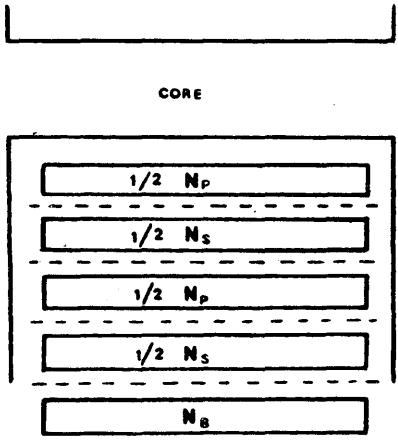
$$g = \frac{I \cdot N_p \cdot \mu_o}{B} = 2.7\ mA$$

$\mu_0 = 12.56 \cdot 10^{-7}\ Hm^{-1}$ (permeability of free space)

Since we have g = 3mm at all working conditions B< 250mT.

$N_s\ (+12) = N_p/n = 27/3.4 = 8$ turns

Fig. 4 - Transformer construction showing the winding pattern for reduced for leakage induction.



SU-1480

To reduce the skin effect in the transformer windings at 80KHz, multistrand conductors must be used. The prototype specifications are given in table 3.

Table 3 - Winding specifications

Primary N_p	=27 turns, 6 wires 0 = 0.8mm
Secondary out. N_s(+12)	=8 turns, 16 wires, 0 = 0.8mm
Secondary aux. N_B(+3)	=2 turns, 1 wire, 0 = 0.8mm

Fig. 4 shows the transformer construction.

POWER SWITCH

In this application the peak switching current is 20A and the correspondent peak collector voltage is approximately 280 volts including the 180 volts spike caused by leakage inductance, Fig. 2.

The bipolar transistors selected are 3 x BUX12 in parallel and the POWER MOS selected is the IRFZ42.

BUX12 x 3

BV_{CEO} = 250V
BV_{CES} = 300V
$I_{C\ CONT}$ = 50A

IRFZ42

BV_{DSS} = 50V
$R_{DS\ ON}$ = 35 mΩ
I_D = 35A

The emitter switching configuration gives very short storage time t_s for 3 x BUX12: at full load we have t_s = 300ns max, and fall time is 150ns maximum. (Photo n. 5).

When the voltage falls on pin 12 of the UC3840, Q1 is off and Q2 conducts. The POWER MOS Q5 is then off and interrupts the emitter current of Q6: at this time current, I_C, flows through the base, becoming a reverse base current I_{B2} that extracts the stored charge from the collector region. The voltage on the drain of Q5 is held at the same value as V_{BB}.

SNUBBERS

To protect the power switch we have two snubber networks .

The first network of C15, R29 and D5 is used to reduce the switch-off power losses of Q6 by delaying the transistor V_{CE} rise while the current falls at turn-off.

$$C15 = \frac{I_p \cdot t_f}{2 \cdot V_{VE\ max}} = \frac{20 \cdot 150 \cdot 10^{-10}}{2 \cdot 280} = 5.35nF$$

5.6nF was selected

R29 resistor is selected to discharge C15 with a time constant of 3μs (about $T_{on\ min}$).

$$R29 = \frac{3 \cdot 10^{-6}}{2C15} = 270\Omega$$

The power dissipated in this resistor is:

$$P = 1/2\ C15 \cdot (V_{CE\ max})^2 \cdot f = 17W$$

The second network, C16, R30 D6 is used to limit the overvoltage due to the transformer leakage inductance when Q6 turns-off.

$$C16 = \frac{L_d \cdot I_P^2}{(V_{res} + V_p)^2 - V_{res}^2}$$

Where: L_d = Leakage inductance (about 1μH)
V_{res} = Reset voltage 45V
V_p = Allowable voltage spike (180V)
C16 = 8.2nF
R30 value is selected so that the voltage across C16 is equal to the reset voltage at the end of the discharge period. Since D6 conducts for about 2.5μs C16 discharge period is about 10μs, then R30 value is calculated as follows:

$$R30 = \frac{(V_{reset} + V_p) \cdot 10 \cdot 10^{-6}}{V_p \cdot C16} = 1.5K$$

The power dissipated in this resistor is:

$$P = 1/2\ L_d \cdot I^2 \cdot f = 16W$$

Due to non-linear effects the power dissipated is about 100W.

PWM CONTROLLER

— Operating frequency is set by R2, C2:
With R2 = 8.2K, C2 = 1.5nF, f = 1/R2 · C2 = = 80KHz

— Start-up is achieved by the network of Q4, R17, R32, DZ1. With a start up current of 60mA we have:

$$R17 = \frac{V_{CC\ min}}{60 \cdot 10^{-3}} = 800\Omega \qquad R32 = 47K$$

— V_{start} and undervoltage threshold are set by R11, R12. These are calculated by equating the current through the node using Kirchoffs laws.

— $$V_{start} = \frac{3V(R11 + R12)}{R12} + 0.2mA \cdot R11 = 13V$$

similary:

— $$V_{uv}(fault) = \frac{3V\ (R11 + R12)}{R12} = 9.5V$$

solving these equation for R11 and R12 then we get the nearest preferred values of:

$$R11 = 18K \qquad R12 = 8.2K$$

— Over voltage fault:

Setting the overvoltage fault to V_{CC} = 100V we have:

$$100 = 3V\frac{R9+R10}{R10} \quad R9 = 33 \cdot R10,\ R9 = 220K \quad R10 = 6.8K$$

— Duty cycle clamp - soft start:

The duty clamp reduces the duty cycle value to below 48% when the input voltage V_{IN} falls belows 48V.

The divider R3, R4, is set to provide 3.9 volts at pin 8. With $V_{IN\ (min)}$ = 46V, R3 = 507K and R4 = 17K. With C3 = 47nF the soft start time is about 6ms.

The feed forward function provides a variable - slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. The ramp is proportional to the DC input voltage; in this way the pulse width is immediately reduced when the input voltage rises. The result will be a constant volt - second product delivered to the transformer primary resulting in good open-loop line regulation.
With T_{on} = 6μs @ 48V we have:

$$\frac{dV}{(dt)\ min} = \frac{V_p - V_{valley}}{6} = \frac{4.2 - 0.5}{6} = 0.616V/\mu s$$

using this value and $V_{DC\ min}$ = 48V with C1 = ⩽C2

$$\frac{dV}{dt} = \frac{V_{DC\ min}}{R1\ C1} \qquad R1\ C1 = 77.8\mu s \qquad R1 = 220K \qquad C1 = 350pF$$

— Current limit.

The resistive divider of R5 (18K) and R6 (1.5K) provides a V_{ref} = 0.38V on pin 7 which is the positive input of error amplifier. For a current limiting value $I_{short\ circuit}$ = 22A the R28 value is set as:

$$R28 = V_{ref}/I_{sc} = 18m\Omega$$

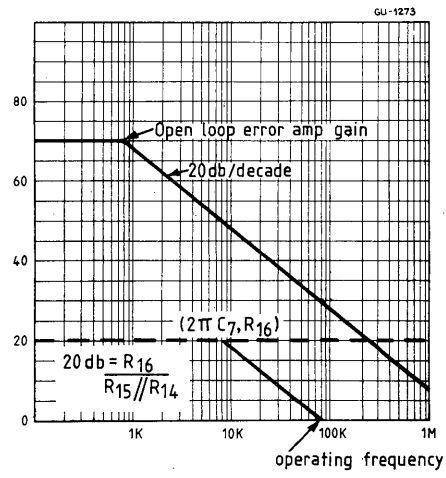
the shut down current value is defined as:

$$I_{SD} = \frac{V_{ref} + 0.4}{R28} = 44A$$

— Voltage control loop.

The error amplifier is set-up for an added DC gain of about 20dB and a second pole at 9KHz. The pole introduced by C17/R16 reduces the gain from 20dB at about 9KHz to 0dB at 80KHz to meet the loop stability criteria.

Fig. 5 - Gain setting for the error amplifier



OUTPUT CAPACITORS

For the high output current of this application the most important characteristics of an output capacitor is its equivalent series resistance, E.S.R. In fact the voltage output ripple is mainly due to losses on the capacitor equivalent series resistance.

E.S.R. specification is:

$$\text{E.S.R.} < V_o/I_c \quad \text{where:}$$

V_o = Allowable peak-to-peak output ripple voltage
I_c = Ripple current in the output capacitor

The mean current in the secondary winding of the transformer while the output diodes conduct is:

$$I_{mean} = I_{max\ output}/(1 - f \cdot t_{on\ max}) = 48A$$

The secondary peak current I_{pk} which corresponds to I_C is:

$$I_{pk} = I_C = I_{mean} + 1/2\ [\Delta I_{prim} \cdot n \cdot t_{on}/T - t_{on})] = 52.4A$$

With V_o = 0.4V we have:

$$\text{E.S.R.} < 0.4/52.4 = 0.0075\Omega$$

POWER OUTPUT RECTIFIER

The power output retifier must be of a fast recovery type in order to reduce losses and the current spike at turn-on of the power switch.

Power diodes with low forward voltages reduce the output filter losses.

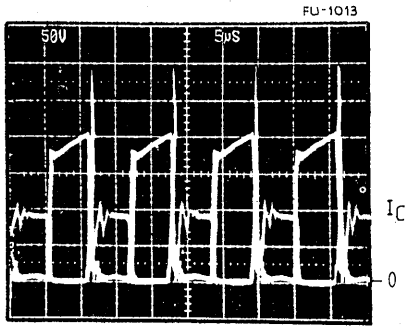
A BYV52 - 50A fast recovery low V_f diode is the solution chosen for this converter.

TESTS ON THE CIRCUIT

The power supply was tested in several operating conditions: with minimum, maximum and rated input voltage, and with various load configurations.

Photograph No. 1 shows the collector voltage and current waveform of the bipolar switch at maximum load (I_{out} = 25A) and at minimum input voltage.

Photo 1 - I_C, V_{CE}, on bipolar switch (I_C = 5A/div, V_{CE} = 50V/div)



This is the worst case because it has a higher primary current and consequently a higher voltage spike on bipolar collectors (due to leakage inductance).

Photograph Nos. 2 and 3 show the details of photograph No. 1 during turn-off and turn-on respectively.

Photograph No. 4 shows bipolar device base current and POWER MOS device gate voltage with the same operating conditions as Photograph No. 1.

Photograph No. 5 shows the collector current, I_C and the base current, I_b waveforms of the bipolar device at turn-off; we can see the high value of reverse base current I_{B2} and the very short storage time (about 300ns).

Photograph No. 6 shows the output ripple at maximum load with V_{IN} = 48V. (Worst case).

Photo 2 - Turn-off, bipolar switch (I_C = 5A/div, V_{CE} = 50V/div)

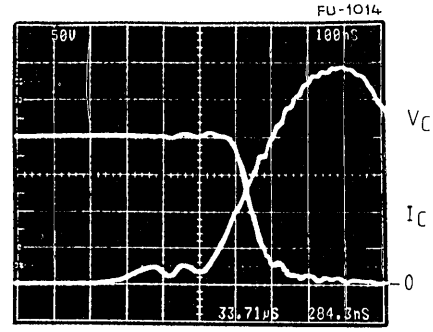


Photo 3 - Turn-on, bipolar switch (I_C = 5A/div, V_{CE} = 50V/div)

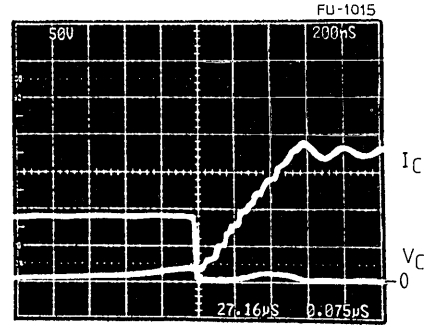


Photo 4 - I_B = 2A/div, V_{gate} = 5V/div

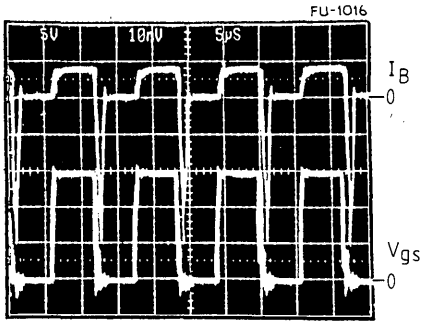


Photo 5 - Storage time bipolar switch (I_B = 5A/div, I_C = 5A/div)

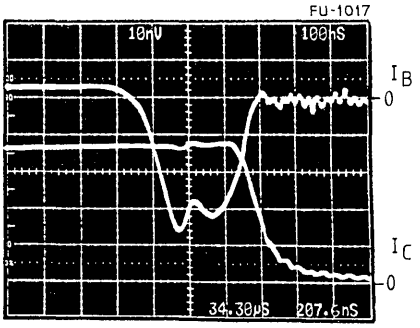
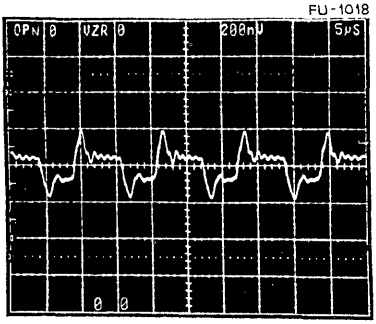


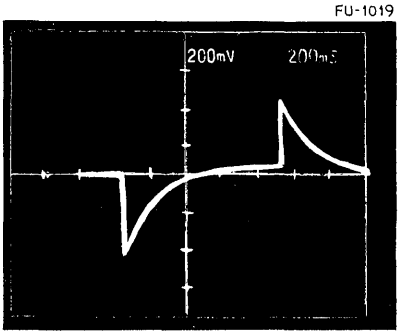
Photo 6 - Output ripple v = 200m V/div



V_O 200mV/div

Photograph No. 7 shows the transitory response of load regulation due to a load variation from 1A to 25A and from 25A to 1A.

Photo 7 - Transient response V = 200mV/div



V_O 200mV/div

Fig. 6 and fig. shows the line regulation and the load regulation (V_{IN} = 70V) respectively. The line regulation is 0.03%/V with an overall variation of 1.1% and the load regulation is 0.17%/A with an overall variation of 2.9% over the operating range.

Fig. No. 8 shows the efficiency of the DC-DC converter at V_{IN} = 70V. At full load (I_{out} = 25A) the efficiency is 75% and the power losses on the circuit are about 100W. The power losses are divided approximately as follows: (Table 4)

Table 4

—	25W	Losses on output diodes
—	27W	Losses on transformer
—	27W	Losses on the two snubbers
—	5W	Losses on IRFZ42
—	10W	Losses on bipolar devices
—	2W	Losses on resistor R26
—	2W	Losses on resistor R28
—	1.5W	Losses on resistor R31

Fig. 6 - Line regulation

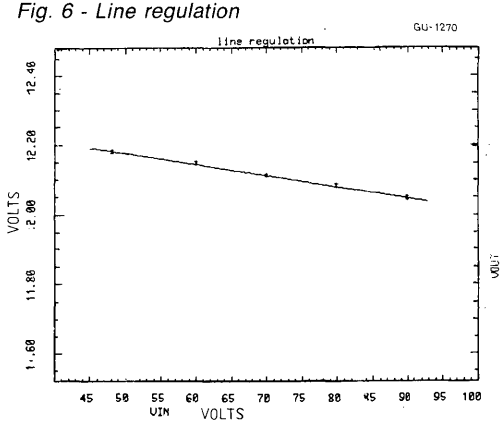


Fig. 7 - Line regulation

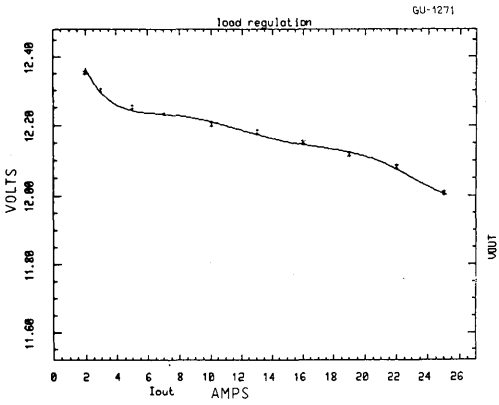
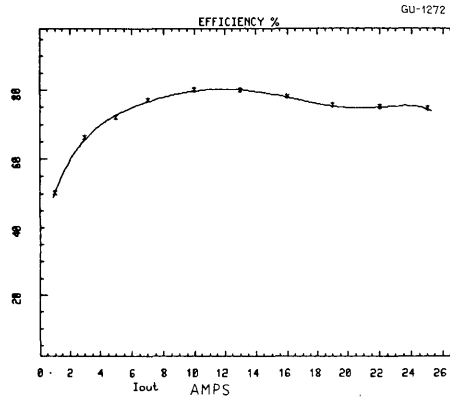


Fig. 8 - Efficiency



CONCLUSION

By using the emitter switching technique this DC-DC converter design uses its switching element to maximum advantage having a very rugged RBSOA and the ability to operate at high frequency. This allows the construction of a compact power supply. The technique also allows high frequency switching with a relatively simple driving circuit. In addition to these advantages the efficiency of the converter at half and full load under a wide range of input voltages, is acceptable as is the output ripple. The efficiency could be further improved by replacing the fast recovery epitaxial diodes in the secondary winding with Schottky diodes.

APPENDIX - Components list of the circuit diagram in fig. 7

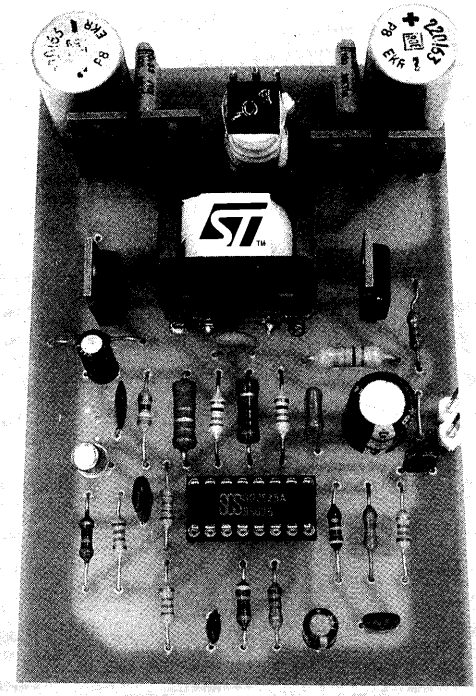
R1	=	220KΩ		R27	=	4.7KΩ	2W	C14	=	1.5μF	
R2	=	8.2KΩ		R28	=	18mΩ	5W	C15	=	5.6nF	300V
R3	=	507KΩ		R29	=	270Ω	20W	C16	=	8.2nF	300V
R4	=	47KΩ		R30	=	1.5KΩ	15W	C17	=	47nF	
R5	=	18KΩ		R31	=	100Ω	2W	C18	=	100μF	100V
R6	=	1.5KΩ		R32	=	47KΩ		C19	=	100μF	100V low E.S.R.
R7	=	15KΩ						C20	=	4.7μF	
R8	=	470Ω		Q1	=	SGS2N2222A		C21	=	5 x 4700μF	16V low E.S.R.
R9	=	220KΩ		Q2	=	SGS2N2907					
R10	=	6.8KΩ		Q3	=	SGS2N2222A		D1	=	BYW81 - 50A	
R11	=	18KΩ		Q4	=	SGSP301		D2	=	1N4148	
R12	=	8.2KΩ		Q5	=	IRFZ42		D3	=	1N4148	
R13	=	18KΩ		Q6	=	3 x BUX12		D4	=	BYW80 - 50A	
R14	=	19KΩ						D5	=	BYTO8P - 300A	
R15	=	28.9KΩ		C1	=	350pF		D6	=	BYV52 - 50A	
R16	=	82KΩ		C2	=	1.5nF		D7	=	4 x BYW81P - 100A	
R17	=	820Ω	1/2W	C3	=	47nF		D8	=	1N4148	
R18	=	82Ω		C4	=	6.8nF		DZ1	=	1N4112	
R19	=	560Ω		C5	=	6.8nF					
R20	=	47KΩ		C6	=	220pF		IC1	=	SGS HCFF 4041B	
R21	=	1.5KΩ		C7	=	220pF		IC2	=	SGS UC 3840	
R22	=	1.8KΩ		C8	=	330pF					
R23	=	2KΩ	potentiometer	C9	=	470pF		Tr1 core	:	Siemens EC 70 N27	
R24	=	820Ω		C10	=	220nF		Tr2 core	:	Siemens E 20 N30	
R25	=	82Ω		C11	=	47μF		L1 core	:	TDK P2616	
R26	=	1.8Ω	5W	C12	=	470nF					
				C13	=	47μF					

200KHz 15W PUSH PULL DC-DC CONVERTER

INTRODUCTION

The 15W DC-DC converter, shown in Fig. 1 has a push-pull topology and works in continuous mode with two outputs (+6V, -6V) and features primary side control with full protection against fault conditions. There is no insulation between the primary and secondary side.

Due to the high working frequency, the power switches used are the new SGS-THOMSON advanced POWER MOS type: IRFZ20 with high



density and bonding on the active area.

The PWM controller is the linear integrated circuit SGS3525A, with dual source/sink output drivers, internal soft-start, pulse by pulse shut-down and adjustable dead time control.

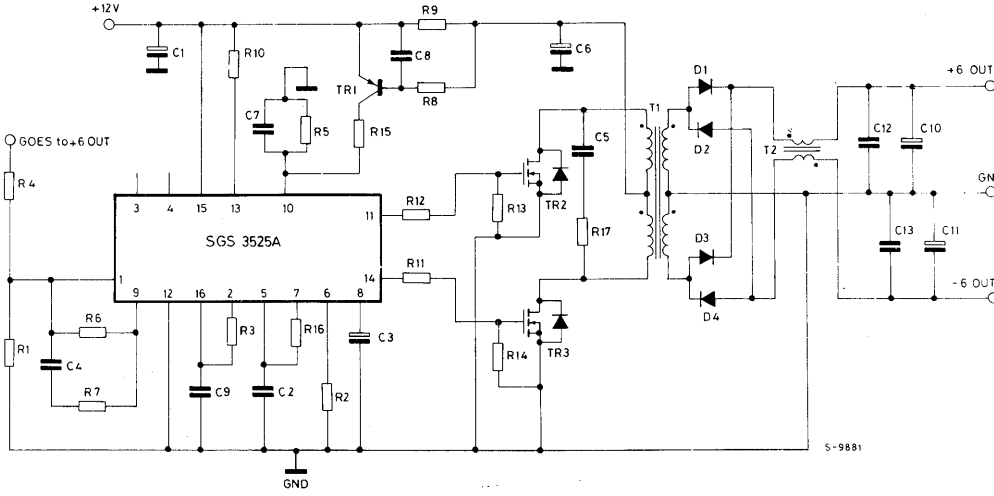
Table 1 shows the power supply specifications.

TABLE 1

Operating mode	:	push-pull
DC input voltage	:	10V DC to 18V DC
Switching frequency	:	200KHz ±10%
Total power output	:	15W
Outputs	:	+6V ±5% 0.1 to 1.3A
		−6V ±5% 0.1 to 1.3A
Line regulation (+6 output)	:	0.05%/V
Load regulation (+6 output)	:	0.2%/A
Efficiency (@ 1/2 load)	:	76%

Output ripple@ max load +6V, −6V outputs: 50mV peak to peak

Fig. 1



CIRCUIT DESCRIPTION

The DC input is chopped at a high frequency (200KHz). This high switching frequency allows the use of a very small transformer.

Due to the push-pull configuration of the converter the POWER MOS devices, the transformer and the diodes work at the frequency of 100KHz (photo 1, 2); the output filters and the oscillator of PWM controller work at a frequency of 200 KHz (photo 3).

When Tr2 is on and Tr3 is off, diodes D2, D3 conduct and diodes D1, D4 are off. When Tr3 is on and Tr2 is off diodes D1, D4 conduct and diodes D2, D3 are off.

The snubber formed by C5, R17 is used to clamp the voltage spikes on Tr2 and Tr3 drains. With a leakage inductance $L_d = 0.5\mu H$, a primary current $I_p = 2.8A$@ $V_{IN\ MIN}$ and maximum load and an allowable voltage spikes $V_p = 30V$ we can calculate

C5 as follows:

$$C5 = \frac{L_d \cdot I_p^2}{(2V_{MIN} + V_p)^2 - (2V_{IN})^2} = 1.8nF \quad \text{Eq. 1}$$

The PWM controller SGS352A has the two drive outputs in totem-pole configuration in order to drive the POWER MOS. The feedback signal for the PWM is directly connected to pin (inverted input of error amplifier) from +6V output by the resistive divider R4-R1. The maximum current protection was sensed by Tr1, R9, R8 and is connected to pin 10 (shut-down).

The magnetic coupling of the series inductance in the output filter is very important for good regulation of the voltages. In this way when the load is very different in the two outputs (+6V max load; −6V min load or viceversa) the indirectly regulated output (−6V) has a very stable output voltage (see fig. 2).

The efficiency is excellent: 70% over a wide range (Fig. 3).

The transient response is very fast: about 50ms. Photo 4 shows the transient response of load regulation due to a load variation from 100mA to 1.3A and from 1.3A to 100 mA (+6V output).

Fig. 4 shows the P.C. board (track layout) and the component positions.

Fig. 2

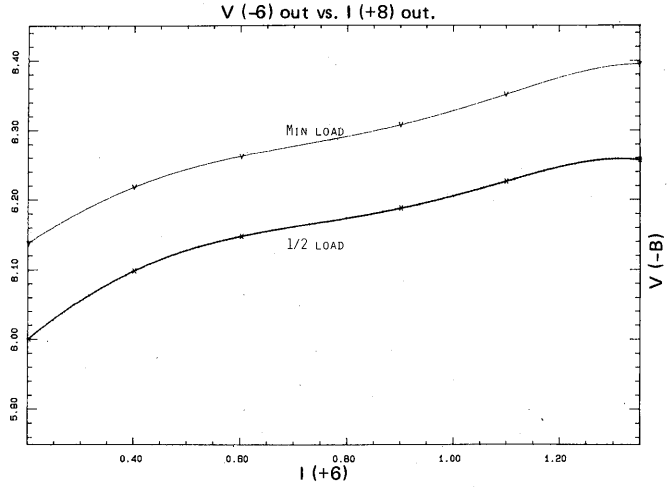


Fig. 3

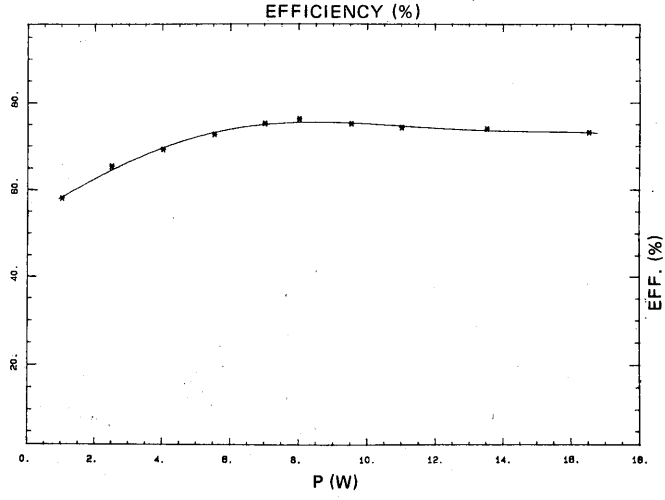
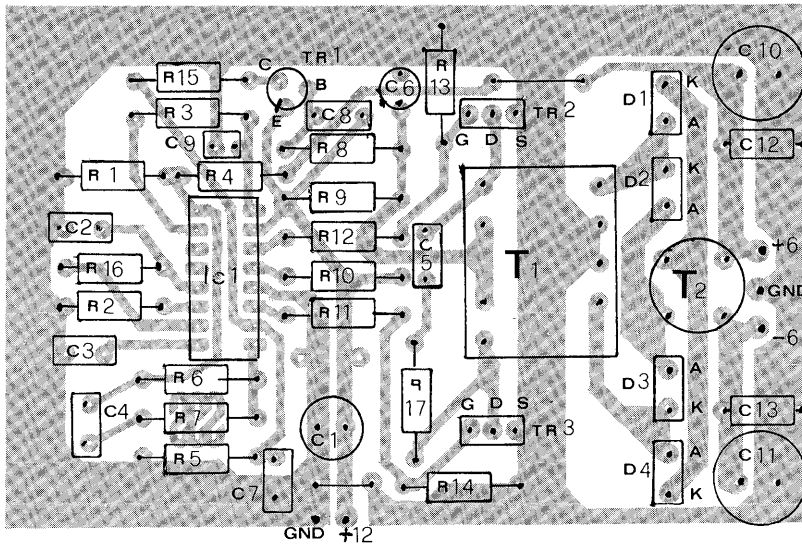


Fig. 4 - P.C. board and components layout (1:1 scale)



TRANSFORMER

For this design a Tominta E core of 2E 6 ferrite material was chosen. To calculate the core size we used the following equations:

$$A_e \cdot A_n > \frac{10^5 \cdot P_{OUT}}{1.16 \cdot \Delta B \cdot f \cdot d} = 0.143 cm^4$$

Eq. 2

where:

P_{OUT} = output 15 (W)
ΔB = flux density swing (T) we chose $\Delta B = 200mT$
d = current density we chose = $450A/cm^2$
f = working frequency of transformer
A_e = effective area of magnetic path [cm^2]
A_n = useful winding cross section [cm^2]

The core size is then EE 25 x 6.5 with $A_e = 0.42$ cm^2, A_n = 0.45 cm^2 and $A_e \cdot A_n = 0.189$ $cm^4 >$ 0.143 cm^4.

The maximum value of primary current at V_{MIN} is:

$$I_p = \frac{P_{OUT}}{\mu \cdot \delta_{MAX} \cdot (V_{MIN} - \Delta V)} = \frac{15}{0.75 \cdot 0.8 \cdot 9} = 2.8A$$

Eq. 3

Where ΔV is the voltage drop on the R9 resistor and on the POWER MOS , δ_{MAX} = maximum duty cycle, η = efficiency.

The turns ratio is given by the following equations:

$$n = \frac{V_{prim.}}{V_{sec.}} \cdot \delta_{MAX} = \frac{V_{MIN} - \Delta V}{V_{OUT} + V_f} \cdot \delta_{MAX} = 1.03$$

Eq. 4

The number of turns N_p is calculated as follows:

$$N_{p\,MIN} = \frac{V_{MIN}[V] \cdot \delta_{MAX}}{\Delta B[T] \cdot A_e[cm^2] \cdot f\,[Hz]} \cdot 10^4 = 9.5 turn$$

Eq. 5

The number of turns used was $N_p = 10$ and $N_s = 10$

The primary inductance is then the same as the secondary inductance.

$L_p = L_s = N_p^2 \cdot A_L = 100 \cdot 2400nH = 240\mu H$

The value of L_d (leakage inductance) was measured on the transformer:

$L_d = 0.5\mu H$

OUTPUT FILTER

The most interesting part of the output filter is the transformer T2 which, coupling the output series inductance of the two outputs, gives good regulation of the -6V output (magnetic regulator).

T2 construction is very simple because the two inductance are directly wound on the same cylindrical ferrite core. Each winding is made up up of 200 turns and is: L (+6V) = L (−6V) = 17μH.

The four fast recovery diodes used are BYW29-100 type.

Capacitors C10, C11 are 220μF Roederstein EKR low ESR type for application in switching power supplies.

The ripple value obtained is very low: 50mV peak to peak (photo 3).

Photo 1 - Tr2, Tr3, V_{ds} (V_{ds}= 20V/div.)

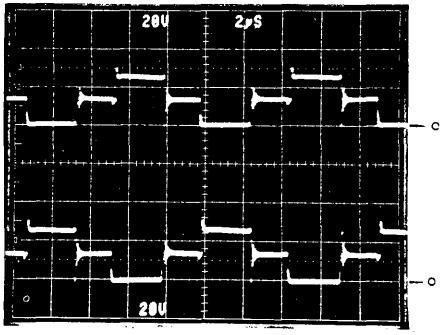
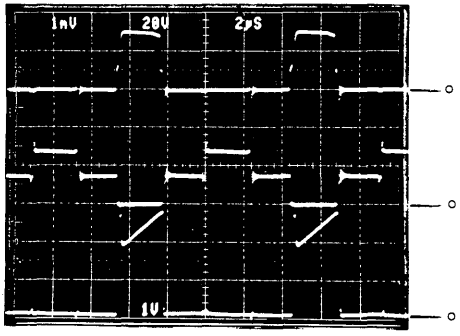


Photo 2 - Tr3 waveforms (V_G= 10V/div, V_{ds}= 20V/div, I_d= 1A/div.)



COMPONENT LIST

Resistors

R1	=	8.2K	1/4W
R2	=	5.6K	1/4W
R3	=	1.2K	1/4W
R4	=	1.5K	1/4W
R5	=	1.2K	1/4W
R6	=	470K	1/4W
R7	=	3.3K	1/4W
R8	=	390Ω	1/4W
R9	=	0.22Ω	1W
R10	=	10Ω	1/4W
R11	=	22Ω	1/4W
R12	=	22Ω	1/4W
R13	=	5.6K	1/4W
R14	=	5.6K	1/4W
R15	=	18Ω	1/4W
R16	=	47Ω	1/4W
R17	=	33Ω	1/2W

Capacitors

C1	=	100μF
C2	=	1nF
C3	=	1μF
C4	=	10nF
C5	=	1.8nF
C6	=	2.2μF
C7	=	10nF
C8	=	2.7nF
C9	=	10nF
C10	=	220μF
C11	=	220μF
C12	=	330nF
C13	=	330nF

Transistors

TR1	=	2N2907
TR2, TR3	=	IRFZ20

Diodes

D1,D2, D3,D4	=	BYW2929-100

IC_s

I1	=	SGS3525A

Transformers

T1 core	=	TOMITA EE 25 x 6.5 2E6 Material
T2 core	=	cylindrical 30 x 20mm

Photo 2a - Turn ON

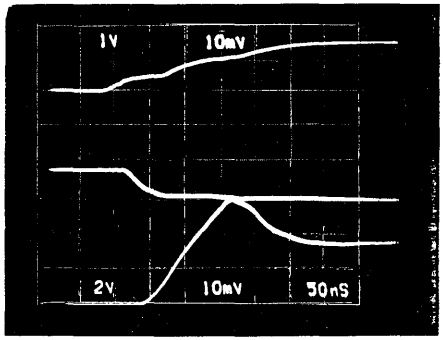


Photo 2b - Turn OFF

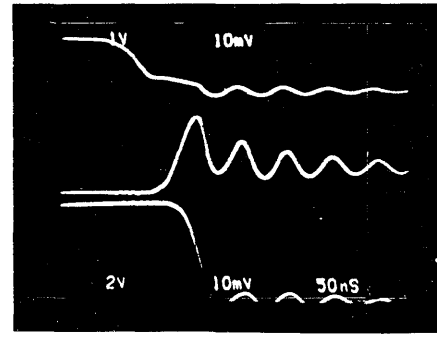


Photo 3 - Ripple on +6V and −6V outputs (20mV/div.)

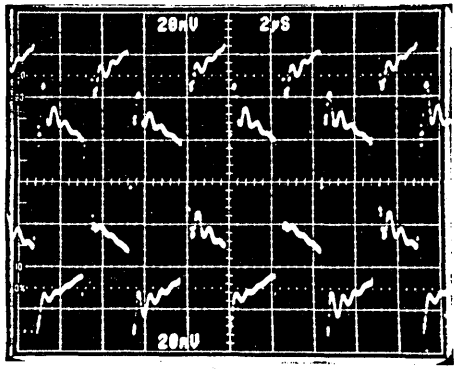
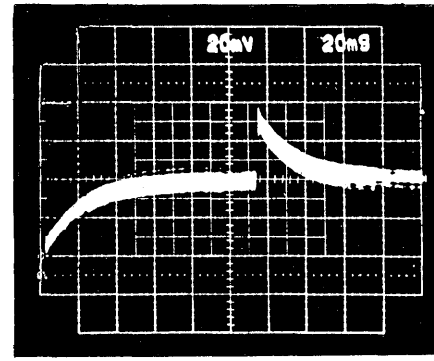


Photo 4 - Transient response (20mV/div)



DRIVE CIRCUIT FOR AN ELECTRIC FUEL CUT-OFF VALVE

INTRODUCTION

The circuit described in this application note has been designed to drive the solenoid of an electric valve. The solenoid has the following characteristics:

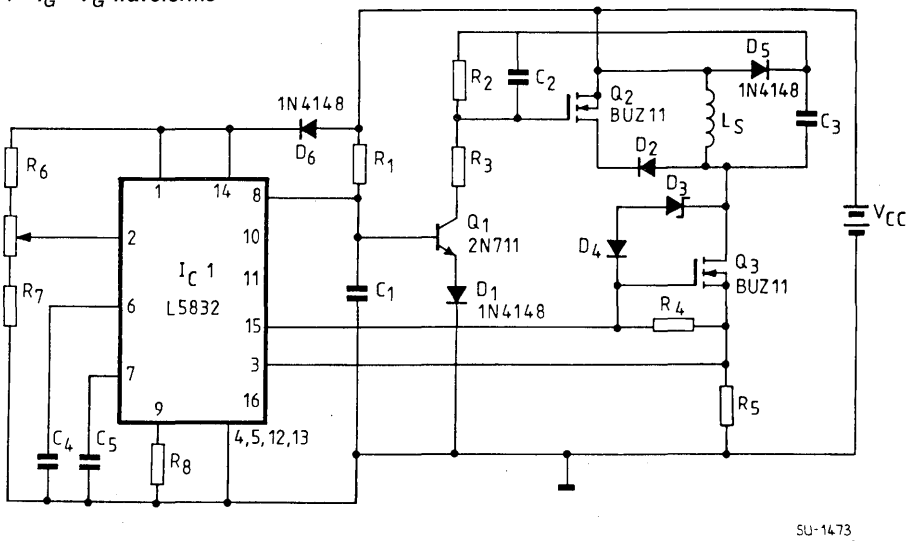
L_S	=	2mH @ 1 KHz
R_S	=	0.62 Ω
I_{pull}	=	38A per 100msec
I_{hold}	=	5A

CIRCUIT DESCRIPTION

The problem this circuit, figure 1, sets out to resolve is to produce an initial current peak of 38A for 100 milliseconds followed by a continuous reduced holding current of 5A.

This design note uses the features of the L5832 together with two external power transistors, both the peak and the holding current level are regulated by the switchmode circuitry of the L5832. The

Fig. 1 - I_G - V_G waveforms



COMPONENT LIST (See Fig. 1)

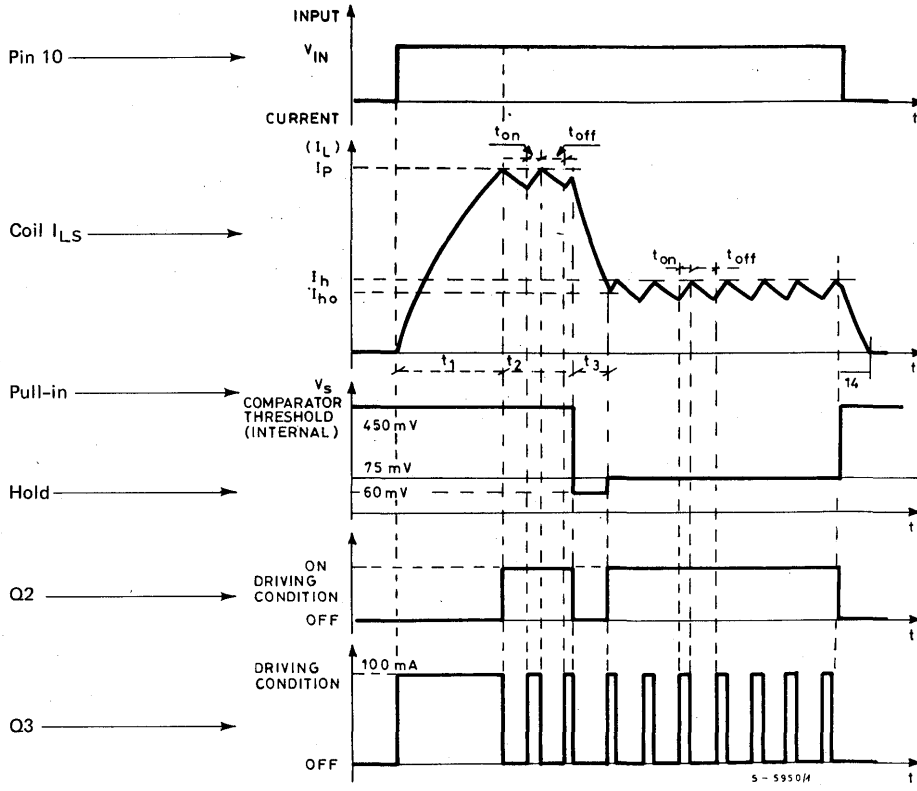
C1	4.7nF	D3	V_Z = 24V,1W	R5	0.01Ω
C2	15nF	I_{C1}	L5832	R6	15KΩ 1/2W
C3	1μF	P1	100Ω	R7	56Ω 1/2W
C4	8μF	R1	470Ω 1/2W	R8	1.2KΩ 1/2W
C5	27nF	R2	100Ω 1/2W	Q1	2N1711
D1-D2-D5-D6	1N4148	R3	68Ω 1/2W	Q2-Q3	BUZ11 or STVHD90
D2	BYV52PI-50	R4	470Ω 1/2W		

duration of the peak, the peak current level and holding current level are fixed by external components. The power stage consists of two BUZ11 POWER MOS transistors and one BYV52PI-50 high current fast recovery diode. The component list is given in table 1.

CIRCUIT BEHAVIOUR

The operating waveforms are shown in figure 2. Q3 energises the inductive load L_S. When the current through L_S reaches I_{pull}, the L5832 starts to regulate I_{LS}. During the regulation D2 and Q2 recirculate the L_S current with a slow di/dt. A fast transition from I_{pull} to I_{hold} is ensured by the action of the zener diode D3 turning on Q3. At I_{hold} the L5832 starts to regulate I_{LS} again. Q2 gate is driven by the bootstrap circuit C3, D5, R2 and C2. Q1 ensures that Q2 is off when the current decreases from I_{pull} to I_{hold}. The figures 4 and 5 show the circuit behaviour. Figure 5 has a faster time-base than figure 4 this enable it to show the PWM control of solenoid or coil current.

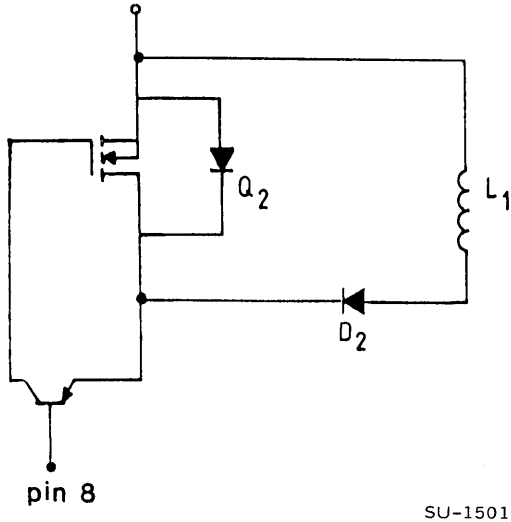
Fig. 2 - Operating waveforms



CONCLUSION

At high current, when the current supplied by the L5832 is insufficient to drive bipolar darlington transistors, the circuit proposed offers a solution to the dilema. If current regulation is not too important (steeper ramp, i.e. increased ripple) it is possible to simplify the driving of Q2 and reduce the number of external components as in figure 3.

Fig. 3 - Simplified driving of Q2



SU-1501

Figure 4

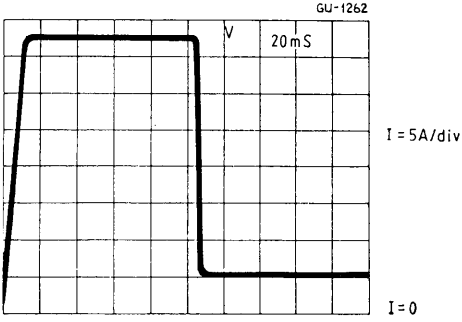
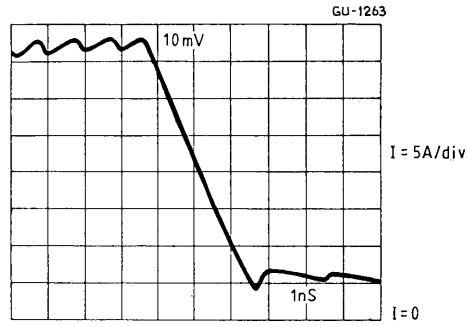


Figure 5



The power lost in power devices is:

At 38 Amp (I_{pull})

$P_{Q2} = 2 \times 38 = 76W$

$P_{D2} = 0.8 \times 38 = 30.4W$

$P_{Q3} = 2 \times 38 = 76W$

} per 100msec.

At 5Amp (I_{hold})

$P_{Q2} = 1.2 \times 5 = 6W$

$P_{D2} = 0.8 \times 5 = 4W$

$P_{Q3} = 0.4 \times 5 = 2W$

NOVEL PROTECTION AND GATE DRIVES FOR MOSFETs USED IN BRIDGE-LEG CONFIGURATIONS

INTRODUCTION

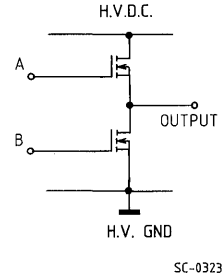
The bridge-leg is an important building block for many applications such as drives and switch-mode power supplies. Simple gate drives with protection for POWER MOSFETs need to be designed for the "low-side" and the "high-side" switches in the bridge-leg. The POWER MOSFET can conduct a peak drain current, I_D, which is more than three times its continuous current rating. The POWER MOSFET peak current capability and its linear operating mode are used to good effect in designing device protection circuitry.

Bridge-leg configurations have a direct bearing on the degree of protection that can be incorporated. Consequently, bridge-leg configurations, protection concepts and gate drives are created simultaneously to design optimised and reliable power electronic circuits.

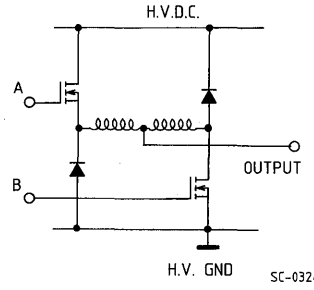
H-BRIDGE USING POWER MOSFETs

Three POWER MOSFET based bridge configurations are illustrated in figure 1. Figure 1a illustrates a bridge-leg which uses the internal parasitic diode as a free-wheeling diode thus reducing cost. However, since the reverse recovery of this parasitic diode is in the order of a microsecond, the turn-on switching times of the POWER MOSFET have to be increased in order to reduce the reverse recovery current. The turn-on time of the POWER MOSFET is controlled such that pulse current rating of the internal diode is not exceeded. Hence a compromise is made between maintaining the safe operating area of the MOSFET and reducing turn-on switching losses. For example, an SGSP477 MOSFET has a diode pulse current rating in excess or 80 A and a typical diode reverse time of 300 ns. A rate of change of current at turn-on, limited to 50A/μs, is a realistic compromise between reverse recovery current magnitude and turn-on losses. Consequently switching speed is sacrificed for cost. For switching frequencies up to 10kHz, when operating on a 400 V DC high voltage rail, this configuration can be chosen as switching losses are limited, thus enabling a realistic thermal design.

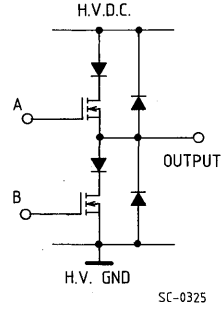
Fig. 1 - Bridge configurations



a) Bridge-leg using internal parasitic diode



b) Asymetrical bridge-leg providing di/dt protection



c) Bridge-leg with blocking diodes

The turn-off speed of the POWER MOSFET in this configuration has no restrictions. Thus a fast turn-off is desirable to reduce turn-off losses. As the rate of change of current is limited, radio frequency interference (RFI) and electromagnetic interference (EMI) are reduced.

An asymmetrical bridge-leg, illustrated in figure 1b; can be used to limit di/dt during a short-circuit condition thus providing sufficient time to switch-off the appropriate power devices. The inductors limit the rate of rise of output current. They also limit the free-wheeling current through the internal parasitic diodes of the MOSFETs. Adding external free-wheel diodes and inductors increases reliability at the cost of increased complexity. The inductors reduce RFI and EMI as the rate of change of current is limited.

The configuration illustrated in figure 1c has Schottky "blocking" diodes to prevent current going through the MOSFET internal parasitic diodes. Schottky diodes are often used since conduction losses are kept to a minimum.

Bridge configurations shown in figure 1b and 1c are considered for high frequency switching applications. The advantage of the asymmetrical bridge-leg configuration over the bridge configurations in figures 1a and 1c is that the bridge-leg is capable of withstanding simultaneous conduction of the two devices in the bridge-leg since there are series inductors which reduce the dI/dt under this condition. Hence the short-circuit detection loop time is not so critical and the devices are not stressed with high dI/dt and high pulse currents.

The choice of the bridge configuration depends on the technical specification of the application. For example, if the technical specification for a specific application can be met by using the configuration shown in figure 1a, then this configuration should be used as costs are lower than with the other two configurations shown in figures 1b and 1c.

GATE DRIVE CIRCUITS

The POWER MOSFET is a voltage controlled device, unlike the bipolar transistor which requires a continuous base drive. An application of a positive voltage between the gate and the source results in the device conducting a drain current. The gate to source voltage sets up an electric field which modulates the drain to source resistance. The following precautions should be considered when designing the gate drive;

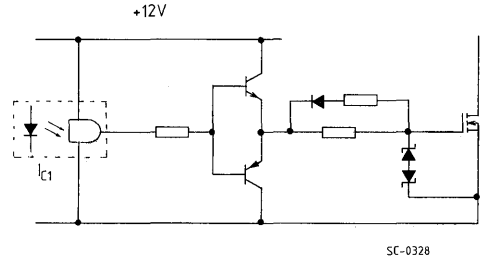
1 - Limit V_{GS} to ± 20V maximum. A gate to source voltage in excess of 16V has a marked effect on the lifetime of the device.

2 - Gate drive parasitic inductance can cause oscillations with the MOSFET input capacitance. This problem becomes more pronounced when connecting devices in parallel.

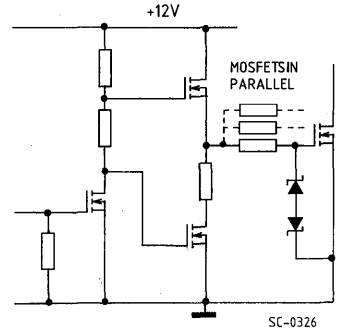
3 - There should be sufficient gate to source voltage for the transistor to be fully conducting.

Fig. 2 - Gate drive circuits

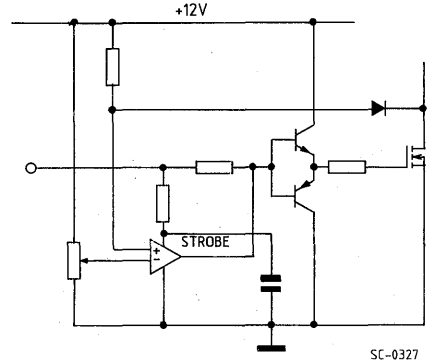
a) Isolated gate drive with controllable switching times



b) Simple gate drive for N-Channel MOSFETS in parallel



c) Gate drive with $V_{DS\ (on)}$ control for short-circuit protection



Bipolar. MOSFET, CMOS or open-collector TTL logic can be used in the design of simple high performance gate drives. Totem-pole buffers, (figure 2a), are often effectively used to control the turn-on and turn-off individually. Figure 2b illustrates a total MOSFET based gate drive with which the switching speeds at turn-off can be individually controlled. CMOS or open-collector TTL logic can be used to drive MOSFETs directly, provided an ultrafast switching speed ($\leqslant$50ns) is not necessary. In motor drive applications switching speeds of 100 to 200 nanoseconds are sufficient as switching frequency is seldom in excess of 50kHz. Discrete buffers are used to provide high current source and sinking capability when improved switching speeds are required or when MOSFETs are connected in parallel.

Short-circuit protection techniques similar to bipolar transistors may be considered for MOSFETs. $V_{DS\,(on)}$ monitoring permits the detection of short-circuit conditions which lead to device failure. The device can be switched off before the drain current reaches a value in excess of the peak pulse current capability of the MOSFET. This form of protection is very effective with MOSFETs as they can sustain a pulse current in excess of three times the nominal continuous current. Figure 2c illustrates a gate drive which incorporates $V_{DS\,(on)}$ monitoring and linear operating mode detection for the MOSFET in the case of short-circuit conditions. When the MOSFET is turned on the on-state voltage of the device ($V_{DS(on)}$) is compared with a fixed reference voltage. At turn-on, $V_{DS(on)}$ monitoring is inhibited for a period of approximately 400ns in order to allow the MOSFET to turn-on fully. After this period, if $V_{DS\,(on)}$ becomes greater than the reference value, the device is latched-off until the control signal is turned-off and turned-on again.

"HIGH-SIDE" SWITCH GATE DRIVES

The top transistor in a bridge-leg requires a "high-side" gate drive circuit with respect to the bridge ground. Three possible gate drive concepts are shown in figure 3:

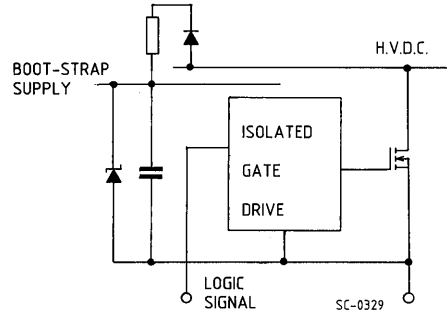
a) The "bootstrap" drive, requiring logic signal isolation, but no auxiliary floating supply.

b) The level shifting drive.

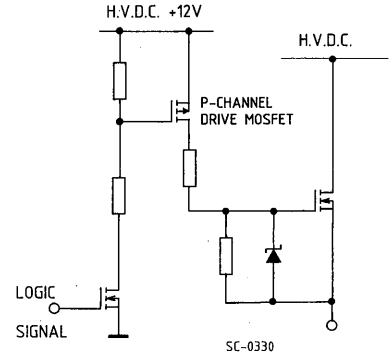
c) The floating gate drive with optically coupled isolators, pulse transformers or DC to DC chopper circuit with transformer isolation.

Fig. 3 - Gate drives for top transistor of inverter leg.

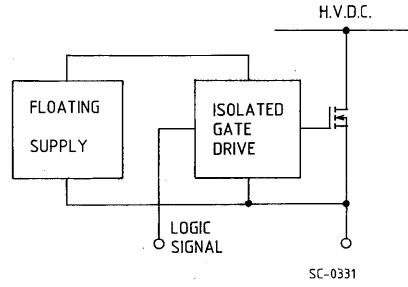
a) "Bootstrap" supply floating gate drive.



b) Level shifting gate drive.



c) Floating supply isolated gate drive.



Bootstrap supplies are particularly well suited fo POWER MOSFET gate drives which require low power consumption. Figure 4 illustrates two bootstrap supply techniques. Bootstrap supplies limit transistor duty cycle since they require a minimum transistor off time during which they are refreshed.

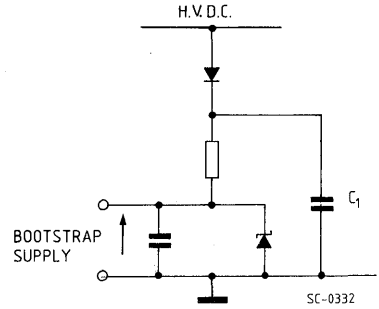
Supply efficiency and maximum duty-cycle are parameters which govern the design of the bootstrap. Figure 4a illustrates a conventional bootstrap with an additional capacitor, C1, which improves the maximum duty cycle as the supply is refreshed even during transistor on time by this capacitor. Figure 4b illustrates a high efficiency bootstrap supply which uses a small MOSFET, Q1, for requlation. In this design a low power bootstrap drives the gate of Q1.

The level shifting gate drive, (figure 3b), requires a high voltage p-channel MOSFET which drives the n-channel power device. The p-channel MOSFET is switched using a resistor divider network. No floating supplies are required. A power supply of 12V, referenced to the high voltage d.c., is used to provide positive gate source voltage for n-channel POWER MOSFET. This circuit eliminates the need for logic signal isolation and a floating supply. The disadvantage of this circuit is the high cost of the p-channel drive MOSFET.

Figure 3c illustrates a floating gate drive with a floating supply. This drive is the most expensive out of the three shown in figure 3. However, the floating supply need only have a low output power, since MOSFETs are voltage controlled devices. The advantages of this drive are its high efficiency and unrestricted transistor duty-cycle.

Fig. 4 - Bootstrap supply techniques

a) Conventional bootstrap with additional capacitor C1.



b) High efficiency bootstrap.

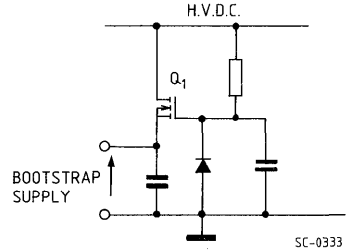
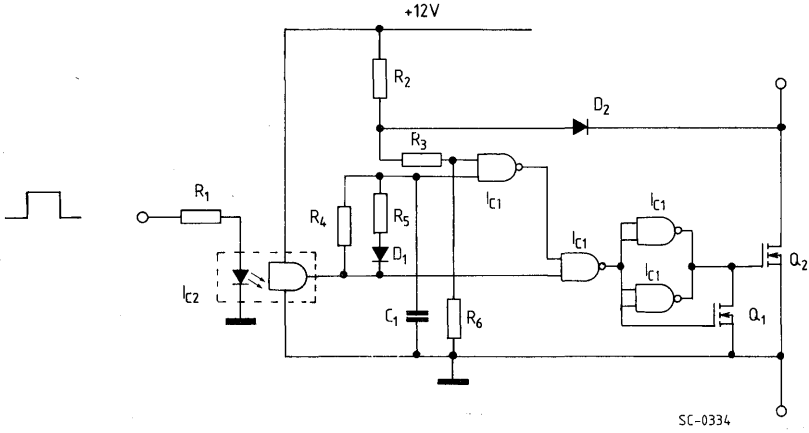


Fig 5 - Isolated CMOS drive with V_{DS} control for short-circuit protection.

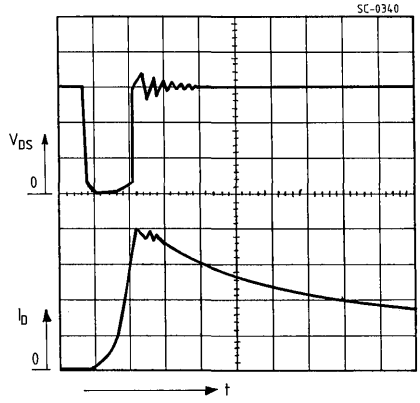


R1 = Dependent on application
R2 = 10kΩ
R3 = 22kΩ
R4 = 1kΩ
R5 = 120Ω
R6 = 56kΩ
I_{C1} = HCF4093
I_{C2} = HCPL2200
C1 = 560 pF
D1 = 1N41448
D2 = BYT11/600
Q1 = BSS100
Q2 = SGSP477

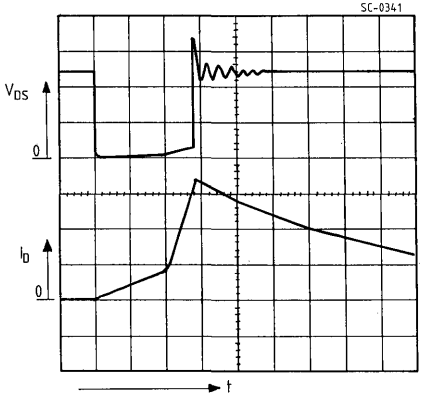
Fig. 6 - Short-circuit conditions for an SGSP477 V_{DS} & I_D

V_{DS}: 50V/DIV
I_D: 10A/DIV
t: 2us/DIV

a) Output to high voltage short-circuit



b) Output to output short circuit



PROTECTION

Power electronic circuits such as bridge-legs are often required to have protection against output to output short-circuit, over-temperature, simultaneous conduction of devices in series in a bridge-leg and output to high voltage supply or ground rail short-circuit. These power stages are generally part of an expensive system such as a machine-tool or a robot motor drive. Thus the additional cost of protection circuitry is commercially acceptable. A compromise is generally reached between equipment costs and the degree of protection required.

Short-circuit protection of a power MOSFET can be achieved by either $V_{DS\,(on)}$ monitoring or a current image. In the previous section gate drives using the $V_{DS\,(on)}$ monitoring technique were presented. Figure 6 illustrates the MOSFET drain to source voltage, V_{DS}, and the drain current, I_D, when short-circuits are experienced by the POWER MOSFET, SGSP477, driven by the gate drive illustrated in figure 5.

The MOSFET is turned-off when the drain current increases sufficiently and $V_{DS\,(on)}$ monitoring is inhibited for a period of 400ns to allow the device to turn-on fully.

An inductor is used in series with the device, as illustrated in figure 1b. This inductor saturates when a large short-circuit current flows. The rate of change of the short-circuit current due to the saturation of this inductor is illustrated in figure 6a and 6b. Figure 6a illustrates the POWER MOSFET drain to source voltage, V_{DS}, and the drain current, I_D, when a bridge-leg output to high voltage supply rail short-circuit occurs. Figure 6b illustrates an output to output short-circuit of two bridge-legs.

Another protection technique uses the "current mirror concept", (1). An image of drain current is obtained by having a small MOSFET, (integral or discrete), in parallel with the main power MOSFET as illustrated in figure 7.

Fig. 7: The current mirror.

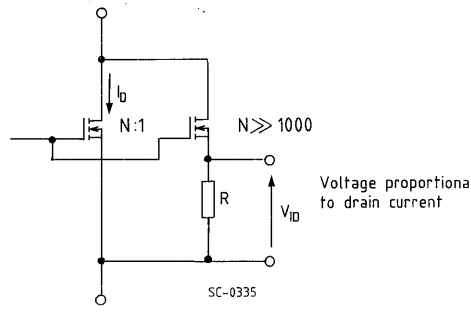
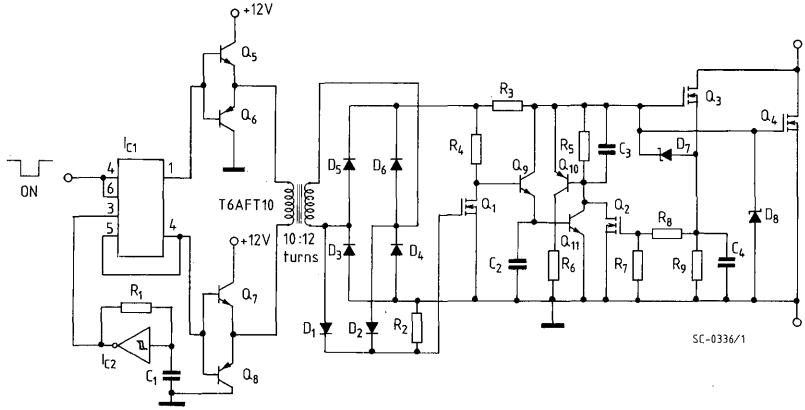


Figure 8 illustrates a floating gate drive which utilizes a pulse transformer for transmitting simultaneously the MOSFET on-signal together and the gate to source capacitance charging current. The current mirror technique is used to provide short-circuit and over-load current protection. The pulse transformer operates at an oscillating frequency of 1MHz when a turn-on control signal is present.

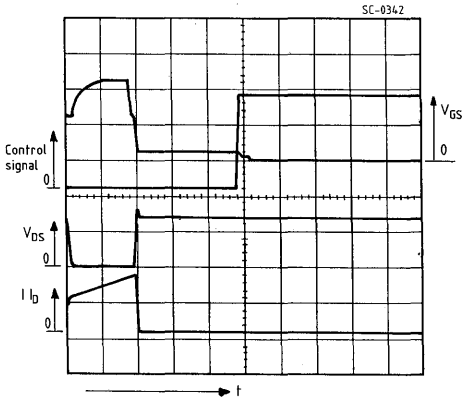
The secondary is rectified to provide the gate source capacitance charging voltage. The current mirror provides a voltage "image" of the main MOSFET drain current. This voltage is compared with a fixed reference voltage in order that the gate drive be latched-off when the drain current becomes in excess of a specificed value. Figure 9 illustrates how the MOSFET, SGSP477, is latched-off when the drain current exceeds 10A with this gate drive circuit.

Figure 8: Pulse transformer gate drive with current mirror protection for an SGSP477.



R1 = 470Ω	R9 = 100Ω	D4 = 1M4148	Q4 = SGS477
R2 = 1kΩ	C1 = 330pF	D5 = 1M4148	Q5 = BC337
R3 = 33Ω	C2 = 10nF	D6 = 1M4148	Q6 = BC327
R4 = 2kΩ	C3 = 10nF	D7 = BZX85C15	Q7 = BC337
R5 = 100Ω	C4 = 220pF	D8 = BZX85C15V	Q8 = BC327
R6 = 100Ω	D1 = 1M4148	Q1 = BSS100	Q9 = BC337
R7 = 100Ω	D2 = 1M4148	Q2 = BSS100	Q10 = BC327
R8 = 100Ω	D3 = 1M4148	Q3 = BSS100	Q11 = BC337

Fig. 9 - Overload current protection using current mirror concept with the gate drive of figure 8 for an SGSP477.



Time scale: 5μs/DIV - I_D: 5A/DIV - V_{DS}: 100V/DIV
Control signal: 5V/DIV - V_{GS}: 5V/DIV

CONCLUSION

MOSFET based bridge-leg configurations requiring protection and floating gate drives have been presented. Novel self-protecting gate drives for the "high-side" and "low-side" switching have been discussed. These drives provide protection against output to high voltage d.c., output to ground and output short-circuit. For the high-side switch "bootstrap" supply gate drive, level shifting gate drive and floating supply isolated gate drives have been compared.

Protection against short-circuit conditions has been demonstrated using $V_{DS(on)}$ monitoring and the current mirror concept. Both techniques are well suited for protection against short-circuit conditions. However, the current mirror concept also provides a sufficiently linear image of the current for regulation.

REFERENCES:

Fuy G.

Current-mirror FETs cut costs and sensing losses EDN September 4 th, 1986

HIGH VOLTAGE POWER MOSFET STHV102

INTRODUCTION

This note deals with the basic characteristics and the possible applications of STHV102 POWER MOSFET transistor, rated at 1000 V, 4A.

A completely new configuration for the edge structure has been designed in order to obtain a high breakdown device with characteristics of high reliability. The advantages offered by the static and dynamic characteristics of this device are demonstrated by two applications.

DEVICE DESCRIPTION

The very first problem to be solved in the design of a POWER MOSFET with $V_{(BR)DSS} > 1000V$ is to achieve a high breakdown efficiency as defined by the expression:

$$\mathcal{E} = \frac{V_{(BR)\ DSS}}{V_{(BR)DSS}\ \text{theoretical limit}} < 1$$

The ratio, $\mathcal{E}$, is the ratio between the actual breakdown voltage of the device and that of an idealised planar junction.

It is well known that the closer $\mathcal{E}$ is to 1, the more efficient is the edge structure.

The merit coefficient, $\mathcal{E}$, is important for any semiconductor device. When conduction occurs by majority carriers, the drain resistance is the output resistance of the POWER MOSFET. So a higher edge efficiency implies the use of a drain epitaxial structure having minimum resistivity and thickness and consequently a much improved $R_{DS(on)}$ compared with existing high voltage, POWER MOSFETs .

The edge structure designed for this class of device is shown in figure 1a - 1b (See page 2).

It is planar, having a graded impurity concentration in the silicon combined with a metal field plate on the surface.

When the device is subjected to a high voltage, the equi-potential lines are accurately spaced as a result of the graded p type region minimizing the electric field strength at the surface.

The very low value of the surface electric field makes the devices insensitive to the surface conditions, allowing significant reliability improvement (see fig. 1b).

The STHV102 is the first POWER MOSFET commercially produced using the structure described. Its dimensions are (180×220) mils^2; the photos 1 and 2 show its static characteristics: the resistance of this device is typically 2.5 ohm with a value of $R_{on} \times \text{Area} = 0.64$ ohm cm^2 which represents a notable achievement.

Photo 1 shows the breakdown characteristics after 1000 hours of HTRB testing, and is indicative of its highly reliable structure.
Fig. 2 shows the variation of the leakage current I_{DSS} after 1000 hours of HTRB test: the alignment to the line shows the high stability achieved using the graded ring structure.

Fig. 1a - Cross section of the new graded edge structure

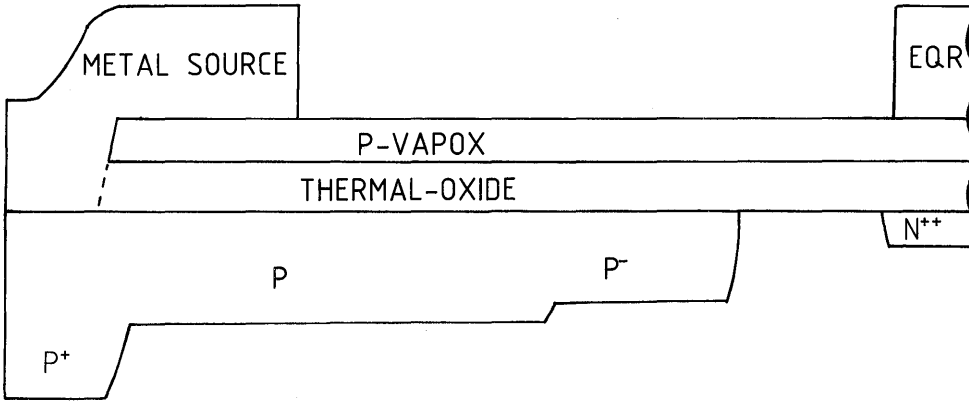


Fig. 1b - Electric field diagram illustrating the low surface electric field

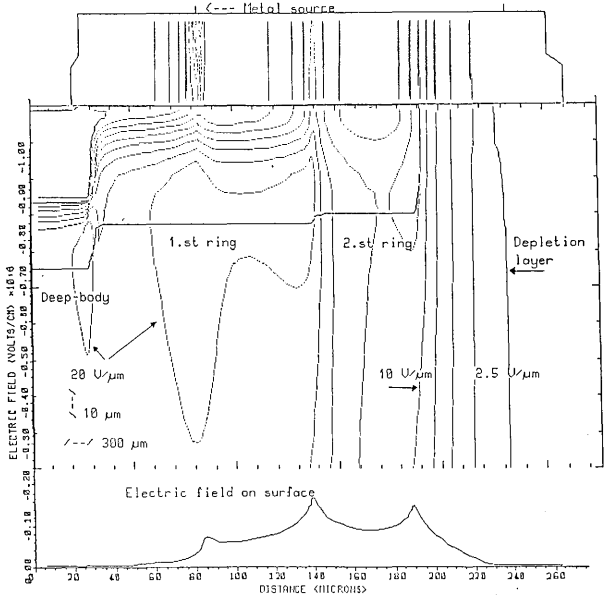


Photo 1 - Breakdown voltage after 1000hrs of HTRB. V_{DS} = 200V/div

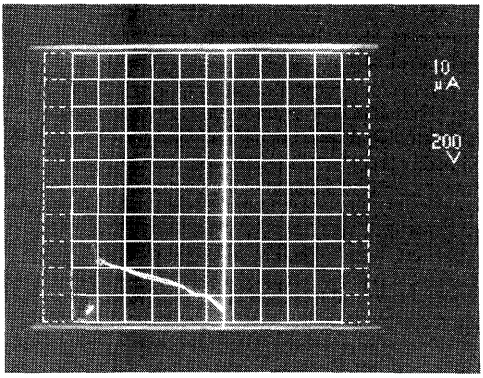


Photo 2 - Output characteristics I_D = 0.5A/div, V_{DS} = 2V/div. STHV102 static characteristics

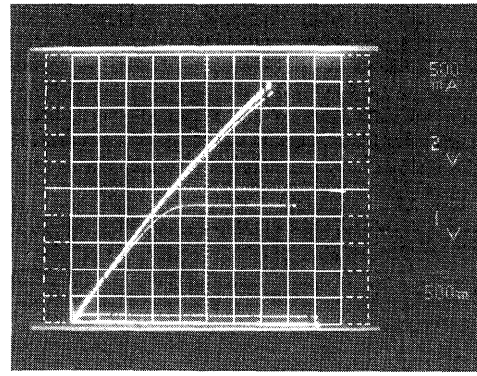


Fig. 2 - Graph showing the effect on drain source leakage current, I_{DSS} of 1000hrs HTRB testing

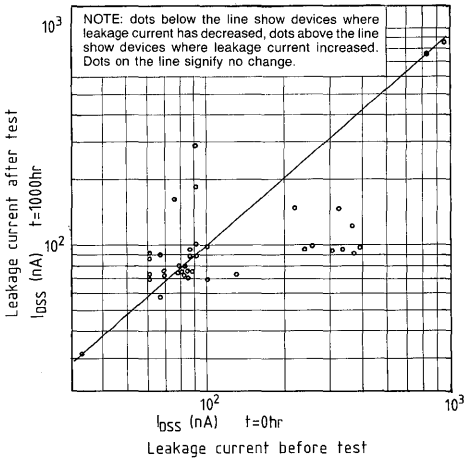
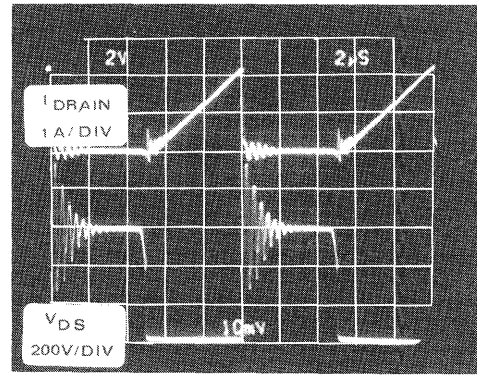


Photo 3 - Drain current and voltage waveforms with T_{case} = 80°C



APPLICATIONS

The STHV 102 is ideally suited to applications where high drain voltage, high switching speeds and low drive energy are needed. Typically in high frequency switch mode power supplies and in high resolution horizontal deflection circuits.

The low value of its input capacitance — a direct result of the optimised edge structure, allows the component to be used in high frequency applications, with very low switching and driving losses.

1. A 150W 100kHz FLYBACK SMPS

Figure 3 shows the SMPS electrical circuit and the photos 3, 4 and 4 show current and voltage waveforms for the POWER MOSFET.

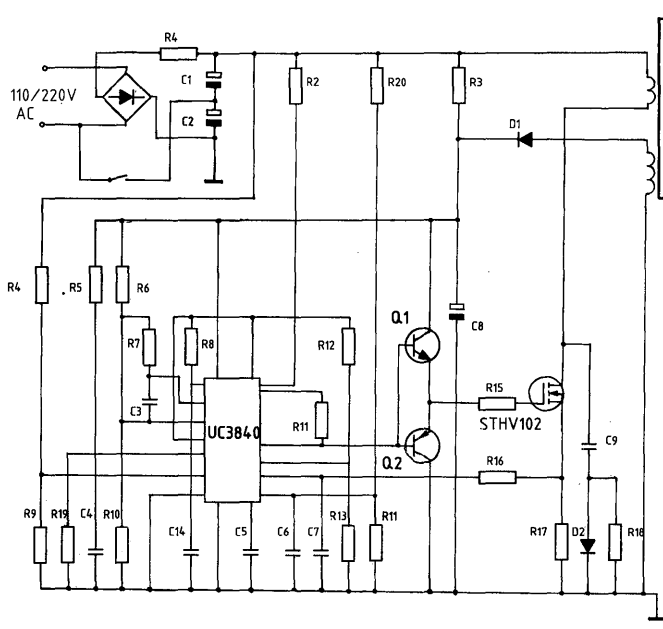
An analysis of the waveforms gives us a better appreciation of the advantages of this device:

a) The high drain voltage capability permits minimum snubbing even when the transformer exhibits a high leakage inductance (Photo 3).

b) The high working frequency shrinks the transformer size and the filter circuit dimensions. Photo 5 shows the small amount of charge needed to turn off the device (120nC), implying that the STHV102 can be easily used also at higher frequencies.

A high performance with a conversion efficiency of 87% at 150W has been achieved with this device.

Fig. 3 - Isolated fly-back Switch Mode Power Supply using a high voltage STHV102 Power MOSFET



SMPS COMPONENT LIST

R1	1	ohm	1	W
R2	68	K	1/4	W
R3	100	K	1	W
R4	750	K	1/4	W
R5	15	K	"	
R6	47	K	Trimmer	
R7	1.5	M	1/4	W
R8	2.7	K	"	
R9	5.6	K	"	
R10	15	K	"	
R11	1.5	K	"	
R12	39	K	"	
R13	10	K	"	
R14	15	K	"	
R15	10	ohm	"	
R16	2.7	K	"	
R17	0.3	ohm	2	W
R18	1.5	K	2	W
R19	9.1	K		
C1, C2	220	uF	250	V
C3	22	pF	25	V
C4, C6	10	pF	"	"
C5	370	pF	"	"
C7	1	nF	"	"
C8	200	uF	"	"
C9	250	pF	1500	V
C10	2200	uF	25	V
C11	4700	uF	10	V
C12, C13	100	nF	25	V
D1	1N4448			
D2	BYT11-1000			
D3	BYW77P-100			
D4	BYW81P-200			
Q1	2N2222			
Q2	2N2907			
IC	UC3840			
PMOS	STHV102			

Power output : 150W

Frequency : 100kHz

Photo 4 - Drain current at turn-off with T_{case} = 80°C

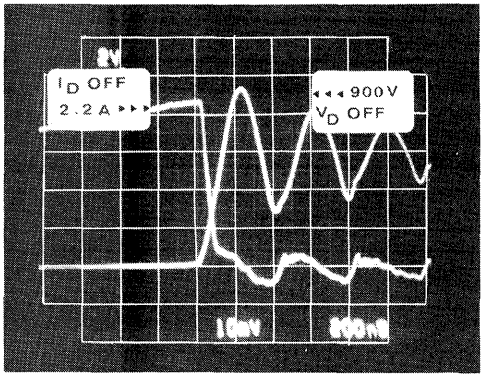
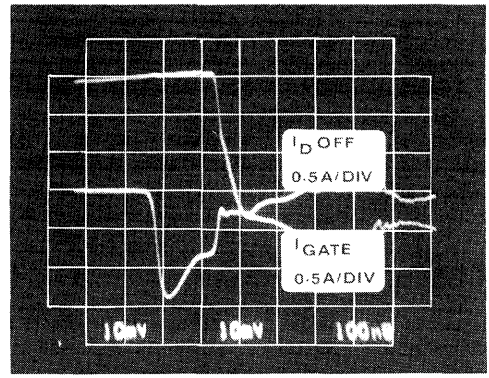


Photo 5 - An indication of gate charge (Q = it) for STHV102 turn-off



The importance of using high voltage POWER MOSFETs in SMPS designs is also illustrated by the reduced size and cost of other components and in lower power dissipation in the snubber network. By comparing similar flyback circuits using a power darlington in one and a POWER MOSFET in the other, as the switching element, shows the following savings.

	Darlington	POWER MOSFET
Switching frequency	30kHz	100kHz
Transformer volume	23.3 cm^3	6.5 cm^3
Filter capacitor	10,000μF	3000μF
Snubber capacitor	1800pF	250pF
Snubber losses	7W	3W
Relativecost of device	1	4

2. HIGH RESOLUTION HORIZONTAL DEFLECTION CIRCUIT.

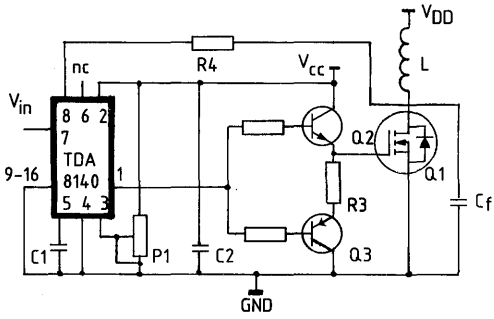
The use of advanced graphic monitors and the experimentation on telecast systems has resulted in the use of complex horizontal defelction circuits and the requirement for fast and reliable high voltage power transistors.

STHV102 represents a good solution, in fact, it brings together the speed of POWER MOSFET devices and a high voltage breakdown (1000 V). In viewof this, its application in a 64Khz horizontal deflection circuit has been studied.

Figure 4 shows the electrical circuit.

Photo 6 illustrates the drain current and the drain-source voltage waveforms.

The "negative" region of the drain current is that which flows in the internal source-drain diode of Q1. The fly-back voltage reaches 920V. During operation at T_c-80°C the device dissipates only 5.5W while generating a 64 KHz, 5A peak-to-peak deflection coil current.

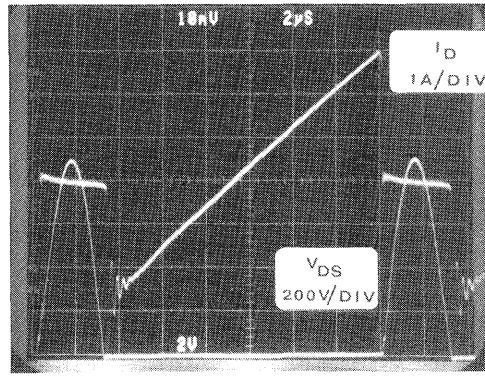


HIGH RESOLUTION DEFLECTION COMPONENT LIST

R1	47	ohm	1/4	W
R2	100	"	"	
R3	10	"	"	
R4	680	K	"	
C1	15	pF	"	
C2	470	uF	40	V
Q1	STHV102			
Q2	2N2222			
Q3	2N2907			
IC1	TDAB140			
L	250	uH		
cf	3.3	nF	1500	V
VDD	120	V		
VBB	12	V		

Fig. 4 - High resolution horizontal deflection circuit using a high voltage Power MOSFET transistor, STHV102

Photo 6 - Drain current and voltage waveforms at T_{case} = 80°C



AN INTRODUCTION TO HIMOS

INTRODUCTION

The structure and characteristics of HIMOS (High Injection MOS) devices, provide circuit designers with an INSULATED GATE BIPOLAR TRANSISTOR (IGBT) capable of handling high voltages at high current densities. The principle characteristics of these new devices are the simplicity with which they can be driven - similar to a POWER MOSFET - and their low conduction losses when switching high voltages. These characteristics, together with their excellent ruggedness make HIMOS a natural evolution of POWER MOS for high voltage applications. Typical uses for HIMOS transistors are switching circuits requiring high voltage and high current, with a switching frequency in the order of 10kHz to 20kHz.

THE BASIC STRUCTURE

Figure 1a shows a single cell of the multicell structure of a HIMOS device.

Figure 1b shows the structure of a POWER MOS for comparison. Figures 1c and 1d show two models for the HIMOS structure. The drain region of HIMOS represents the major difference in structure from that of POWER MOSFETs.

This region contains a P^+ doped layer. The presence of the P^+ N junction drastically reduces the on-resistance during conduction because conduction causes holes to be injected into the drain which, in turn, modulates the conductivity of this region. However, the addition of the P^+ layer to the drain also gives rise to a parasitic thyristor stucture PNPN, created by the NPN - PNP parasitic bipolar structure. In order to avoid the influence of this parasitic thyristor we have designed a modified structure for the device and a new process for its manufacture.

STATIC ELECTRICAL CHARACTERISTICS

Current flow in HIMOS devices during conduction is shown in figure 2a. The total current, I_{DS} is the sum of the two currents I_c (h) and I_b (h) where: -

- I_c (h) is the current due to holes injected from the substrate P^+ layer, which are collected on the surface of the source region and
- I_b (h) is the current due to holes that combine with electron current flowing through the MOS channel in the base region of the PNP bipolar junction transistor, (BJT).

Fig. 1a - HIMOS - Basic structure

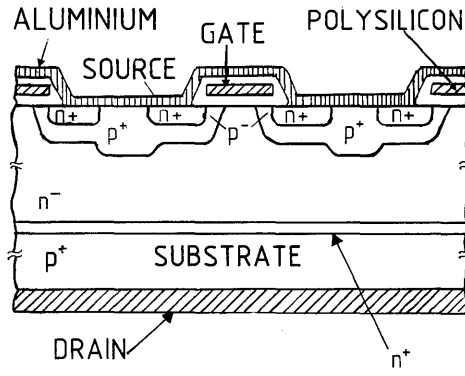


Fig. 1b - POWER MOSFET - Basic structure

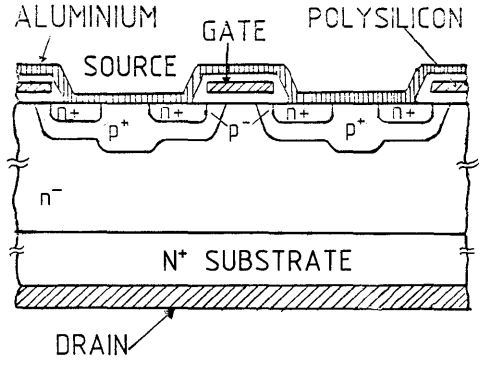
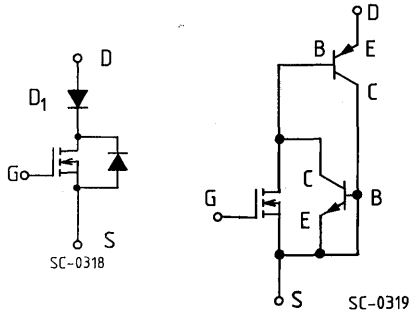
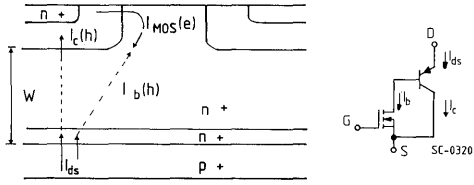


Fig. 1c and 1d - Two electrical models for the HI-MOS structure.



1c *1d*

Fig. 2a and 2b - Current flow in HIMOS during conduction



2a *2b*

Since MOS behave like a BJT whose base current is provided by a MOSFET, it follows that the drain current of the HIMOS is the sum of the bipolar base and collector currents.

$I_{ds} \simeq I_{mos}(1 + \beta PNP)$ Eq. 1

These features underlie the advantages of HIMOS devices particularly in respect of their current capability and low $R_{DS\ (on)}$ compared with POWER MOS devices. A comparison of the output characteristics of a HIMOS and three POWER MOS transistor with equal chip size but different breakdown voltages is shown in photographs 1-4

The comparison highlights two major points. The first is the difference in the current flowing for a given gate voltage. This shows that HIMOS have a greater current handling capability and a lower $V_{DS\ (on)}$ than the equivalent POWER MOS device. The low $R_{DS\ (on)}$ is due to conductivity modulation of the substrate caused by high injection of holes from the P^+ region.

The presence of the P^+N junction in the drain produces an offset in the output characteristics of 0.6V-0.8V. This diode exhibits a reverse breakdown voltage in the range 30V-70V, see Photograph 5.

Photo 1 - $V_{(BR)\ DSS}$ = 100V *SGSP361*

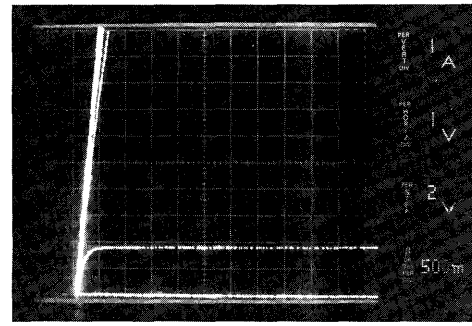


Photo 2 - $V_{(BR)\ DSS}$ = 250V *SGSP363*

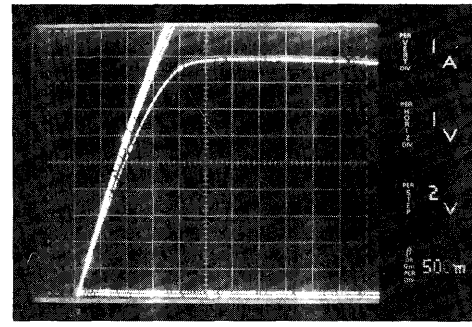


Photo 3 - $V_{(BR)\ DSS}$ = 500V *SGSP369*

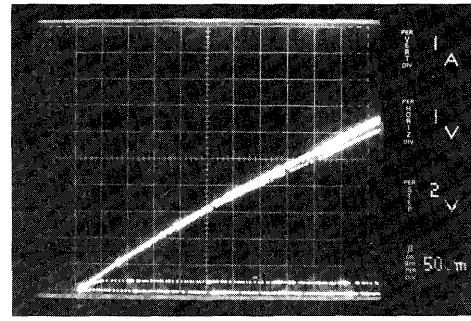


Photo 4 - $V_{(BR)\ DSS}$ = 500V *STHI10N50*

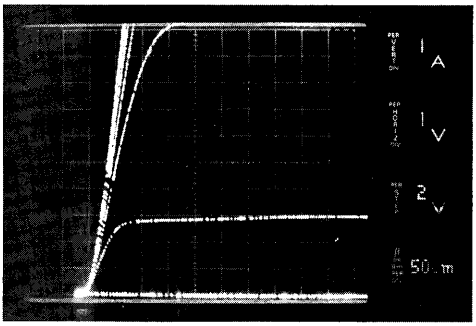


Fig. 3 - Test circuit for HIMOS transistors

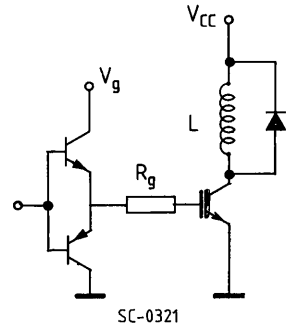
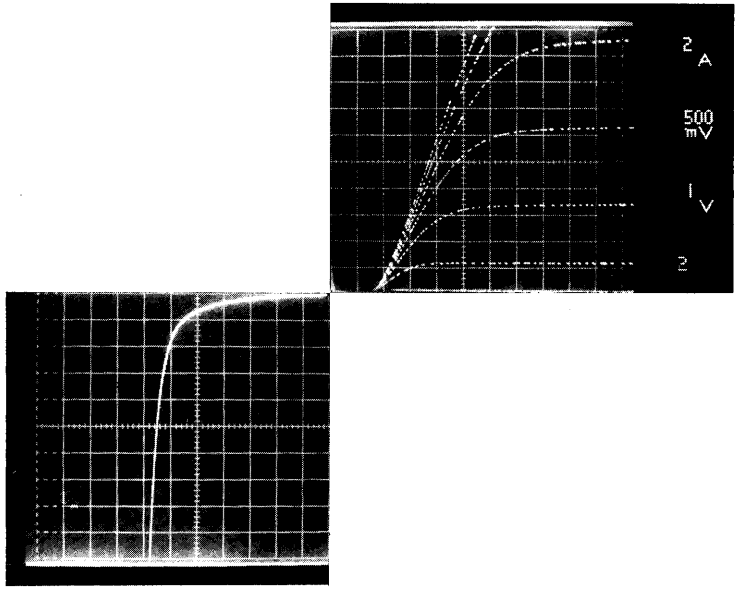


Photo 5 - Output characteristics of a HIMOS device



SWITCHING CHARACTERISTICS

Figures 1 and 3 show the HIMOS equivalent circuit and the test circuit for evaluating the switching characteristics. When the gate-source voltage, V_{GS}, is greater than the threshold voltage, V_{TH}, the MOS section of the structure turns on. The MOS drain current is the base current of the parasitic PNP transistor and it turns on the PNP transistor in about 10nsec. HIMOS turn-on time is a function of the impedance of the driver circuit and the applied gate voltage. Photograph 6 shows typical turn-on waveforms.

TURN-OFF

Turn-off in HIMOS has typical features of both POWER MOSFET and BJT turn-off due to the use of conductivity modulation for increased current density. Figure 4 shows how the turn-off can be divided into three regions.

During the first phase, I, the gate voltage decreases to a point where the Miller effect begins and V_{DS} begins to rise. In the second phase the gate voltage is constant - the Miller effect. During this period increasing V_{DS} decreases the gate capaci-

tance and an inversion of the gate polarity, with, respect to the drain voltage occurs as V_{DS} rises above the gate potential. V_{DS} increases to a maximum value with a rate controlled by the driver circuit. These two phases, I and II, are dependent on the MOS behaviour as the base collector junction of the PNP transistor is reverse biased. The last region, which defines t_{fall}, can be divided into two parts. The first part is the MOS turn-off and is very fast. The second is slow and starts when the MOS channel is closed and the PNP transistor has an open base. This terminates turn-off by recombination of excess carriers. The first part of the fall time can therefore be controlled by the gate drive circuit. The second part is dependent on the PNP transistor lifetime and gain.

Photo 6 - HIMOS turn-on wave form

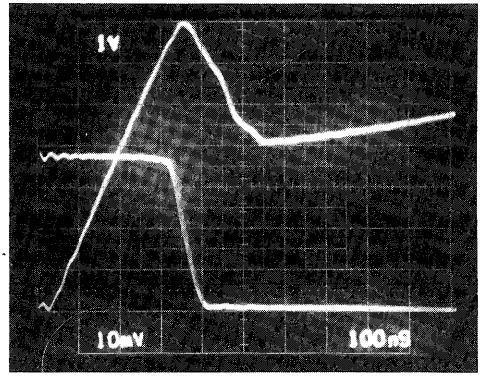


Fig. 4 HIMOS turn-off showing three turn-off regions

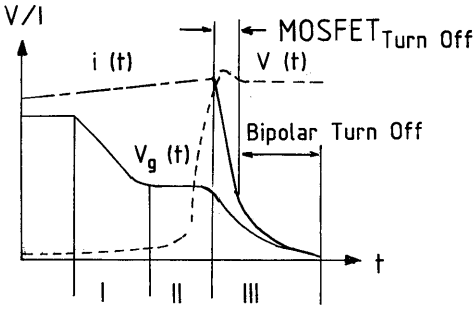


Figure 5 shows how t_{fall} varies with V_{DS}. As V_{DS} increases so the gain of the PNP transistor increases. This is due to the reduction of the base thickness caused by increasing the depletion region. The dependence of t_{fall} on temperature is shown in figure 6 and confirms the correlation between t_{fall} and the PNP transistor gain. The lifetime of the minority carriers in the N^- region versus t_{fall} is shown in figure 7.

Fig. 5 - Variation of t_{fall} with V_{ds}

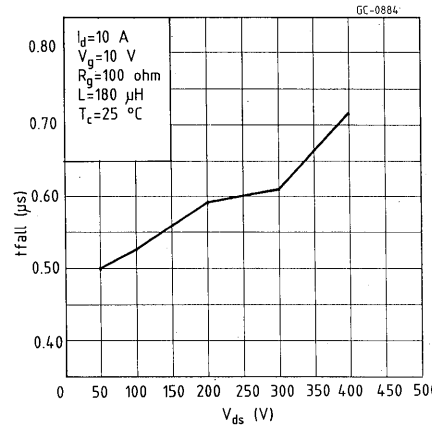
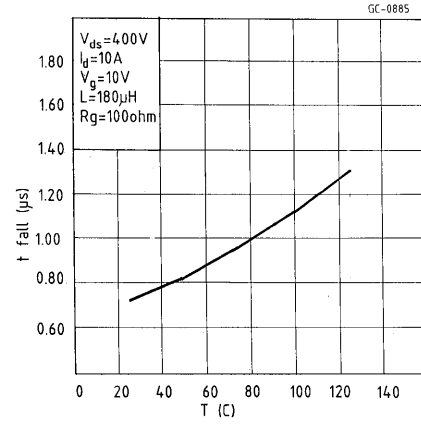


Fig. 6 - Variation of t_{fall} with temperature



LATCH-UP AND SAFE OPERATING AREA

The device current begins to loop regeneratively when the total current reaches the latch-up value, I_{latch}. If the current attains this value then gate control is lost. Looking at figure 1c we have:

$$I_s = [\alpha npn \cdot I_c] / [1 - (\alpha npn + \alpha pnp)]$$

where αpnp and αnpn are the gains of the transistor structures and I_i is the recombination current. The device enters into a regenerative loop and it fails when $\alpha pnp + \alpha npn \geqslant 1$. In order to redu-

ce αpnp and αnpn so that their sum is less than 1, some stuctural and processing changes in fabrication of the device are necessary. By using appropriate doping and shorting the base-emitter junction (POWER MOSFET body-souce) it is possible to reduce αPNP. αNPN is reduced by the introduction of a buffer heavily doped with N^+ and the introduction of lifetime killers.

Fig. 7 - Variation of t_{fall} with the lifetime of the minority carriers in the n^- region

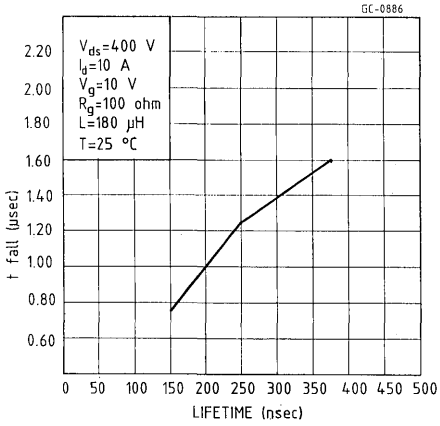
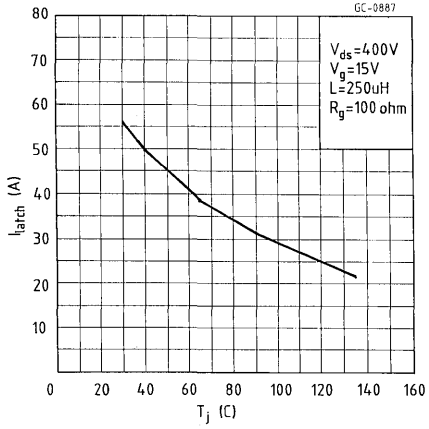


Fig. 8 - Variation of I_{latch} with temperature



I_{latch} decreasing with temperature, figure 7, or with increasing V_{DS} is correlated to the gain variations they cause in the two parasitic transistors. Externally, from an electrical point of view, latch-up can be seen in the safe operating area curve, figure 8, for a working temperature of 100°C.

Fig. 9 - HIMOS reverse bias operating area

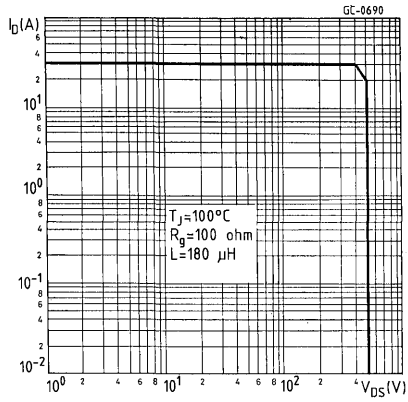
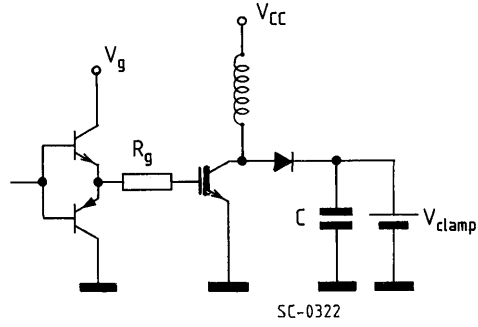


Fig. 10 - Test circuit HIMOS reverse bias safe operating area



CONCLUSION

HIMOS devices are a natural development of POWER MOSFET transistors for use in high voltage applications in the range of 500V - 1000V. They present the user with high current devices which have low $V_{DS\ (on)}$ typical of bipolar devices and the simplicity of drive typical of POWER MOSFETs.

Increasing the latch - up current and reducing the lifetime of the minority has opened up new field for HIMOS.

AN ECONOMIC MOTOR DRIVE WITH VERY FEW COMPONENTS

INTRODUCTION

The main objectives of this design are the economy and circuit simplicity which enable costs to be reduced to a minimum. For this reason the design is particulary suitable for domestic appliances powered by the 220 V AC mains. In this area, characteristics such as low cost, simplicity (and consequently greater reliability) have priority.

With these objectives the choice of the power switch is very important because the complexity of the drive circuit, the number and the power of the auxiliary supplies and the protection networks, depend on its characteristics. These factors lead to the decision to use a HIMOS device (an IGBT) as a power switch. The main characteristics of a HIMOS device are that:

- It switches high current with very low ON resistance, similar to a BJT (bipolar junction transistor).
- It is very rugged and has very large safe operating areas similar to Power MOSFETs.
- It has high overload current capability.
- It is easy to drive (like Power MOSFETs) consequently it is possible to drive it directly by means of popular linear IC.

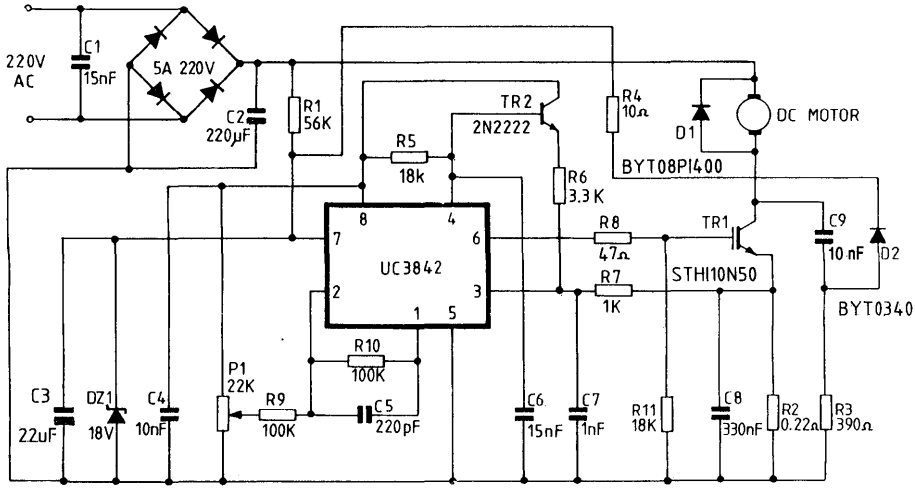
These characteristics are very suitable for motor drive applications in general and make HIMOS the new way of power switching in this area. An additional factor is that a HIMOS device has a smaller chip area than Power MOSFETs, or bipolar transistors with the same ratings ($V_{(BR)\,DSS}$ and $I_{DS\,max}$).

CIRCUIT DESCRIPTION

This DC motor drive circuit has a single switch topology and works in current mode; an STHI10N50 HIMOS is used as the power switch. The complete circuit schematic is shown in figure 1. Its main features are as follows:

- 300V, 4A DC permanent magnet step down motor drive
- Current mode PWM control
- Output current adjustable pulse by pulse from 0 to 4A
- 220 AC ± 10% supply voltage
- 6KHz switching frequency
- From 6% to 95% operating duty cycle

Fig. 1 - Circuit diagram of the HIMOS motor drive



The PWM controller IC used is STUC3842. It is a popular, economic eight pin IC widely used for off-line and DC to DC converters. STUC3842 provides the features necessary to implement fixed frequency current mode control scheme with a minimal external parts count.

Internally implemented circuits include under voltage lockout featuring start-up current less than 1mA, a precision reference, logic to insure latched operation, a PWM comparator which provides current limit control and a totem pole output stage. It can directly drive the gate of the 500V 10A HIMOS switch STHI10N50. The choice of this IC and its current mode working matches the requirements of economy and simplicity of this application.

Fig. 2 - STHI10N50 output characteristics (I step = 6V)

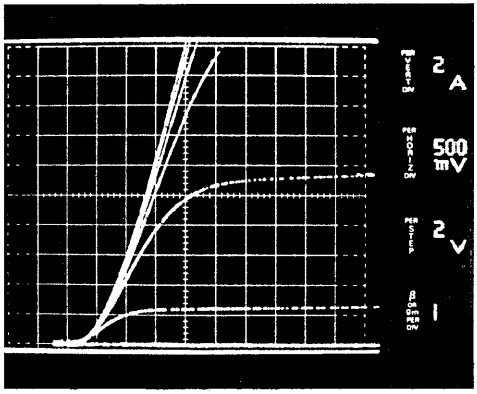
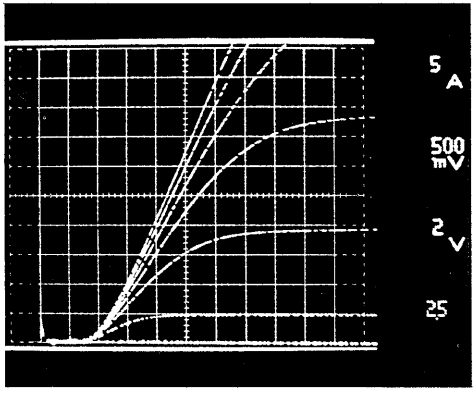


Fig. 3 - STHI20N50 output characteristics (I step = 6V)



The motor speed is controlled by the error voltage which is variable from OV to +5V, and is applied to pin 2 of the IC by means of R9. This voltage sets a constant current level at which the IC interrupts, pulse by pulse, the current in the power switch: the PWM control is therefore a "current mode" type. The HIMOS switch used is STHI10N50, for higher power motors STHI20N50 can be used simply by changing resistors R2 and R6 and free-wheeling diode D1. Figures 2 and 3 show respectively the output characteristics of STHI10N50 and STHI20N50 devices.

An important part of the circuit is the snubber consisting of R3, C9, D2. This accomplishes two functions:

a) it provides power for the UC3842 using the charge current of C9 during the STHI10N50 turn-off; infact the IC requires about 20 mA DC as supply current and cannot be biased simply through resistor R1 which should be 10Kohm 10W. Instead, using this active snubber, R1 can be set to a value of 56Kohm 2W in order to apply the start up power to the UC3842.

b) it reduces the energy dissipated in the power switch during turn-off; consequently a smaller heatsink can be used for STHI10N50 giving additional cost reduction.

To insure a continuous power supply to the IC, using the active snubber C9, R3, D2, it is necessary that the capacitor C9 must be completely discharged before turn-off. Because C9 is discharged by means of R3 during the ON phase of the power switch, there is a limit to the minimum ON time which cannot be less than 8 μs, consequently the minimum duty-cycle is 6%.

Considering a peak current I_p = 4A, a fall time t_f = 1.5 μs and the minimum ON time of 8 μs, the values of the snubber components are calculated as follows:

$C9 = (I_p \cdot t_f)/2V_{cc} = 10$ nF

$R3 = T_{on\ (min)}/2 \cdot C9 = 400$ohm

The power dissipated across R3 is:

$P = 1/2 \cdot C9 \cdot V^2 \cdot f = 3W$

The adoption of this snubber does not affect the efficiency of the circuit during normal operation because its power dissipation is very low and it has the additional benefit of using this energy to supply the IC so reducing the dissipation in the power switch. The extra cost is negligible with respect to the cost of a transformer for supplying the low voltage power to the IC.

The network of Tr2 and R6 adds a fraction of the ramp oscillator voltage to the "current sense" si-

gnal at pin 3 of the IC (via transistor Tr2 2N2222) to allow slope compensation. Consequently duty-cycles as high as 50% can be obtained.

Diodes D1 (BYT08PI400) and D2 (BYT03400) are fast recovery types and have been used in order to minimize stresses on the power switch.

MEASUREMENTS ON THE CIRCUIT

The DC motor drive was tested in several operating conditions. These were maximum and rated output current and in blocked rotor conditions.

The waveforms of the drain voltage, V_{DS}, drain current, I_D, and gate voltage, V_G, both with and without the snubber can be seen in figures 5 and 6 respectively.

Fig. 4 - STHI10N50 turn-off with snubber I_d= 1A/div, V_{ds}= V50/div, V_g=5V/div

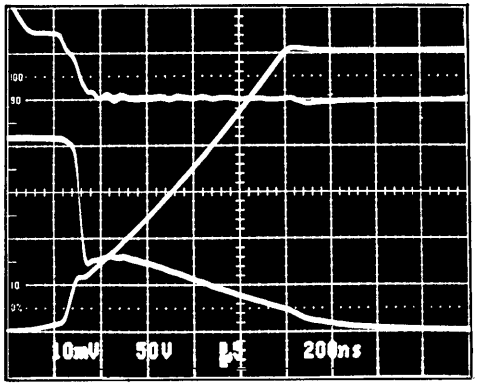
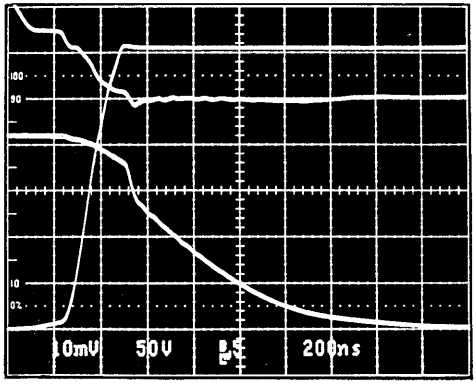


Fig. 5 - STHI10N50 turn-off without snubber I_d= 1A/div, V_{ds}= 50V/div, V_g= 5V/div



Here you can see the typical behaviour of a HIMOS device at the turn-off when typical features of both Power MOSFET and BJT are involved. The storage phase of the turn-off is dependent on the MOS behaviour as the base collector junction of the PNP transistor is reversed biased: the gate voltage decreases to a point where the Miller effect begins to control the current in the drain and V_{DS} start to rise. The fall time phase can be divided into two parts: the first part is the MOS turn-off and is very fast, the second is slow and starts when the MOS channel is closed and the PNP transistor has an open base turn-off and is dominated by recombination of excess carriers. Therefore the first part of the time is controlled by the gate drive circuit, the second part is dependent on the PNP transistor life-time and gain.

Since the PNP gain increases as V_{DS} increase, the fall time consequently varies with V_{DS}. Therefore, when the snubber is used and the V_{DS} slope is dominated by the capacitance, the fall time region due to the MOS is more evident (figure 6).

Figure 6 shows the turn-on behaviour of the HIMOS: it very fast (t-rise 30ns) and, as with Power MOS devices, is a function of the impedance of the driver circuit and the applied gate voltage.

Fig. 6 - STHI10N50 turn-on I_d= 1A/div, V_{ds}=50V/div

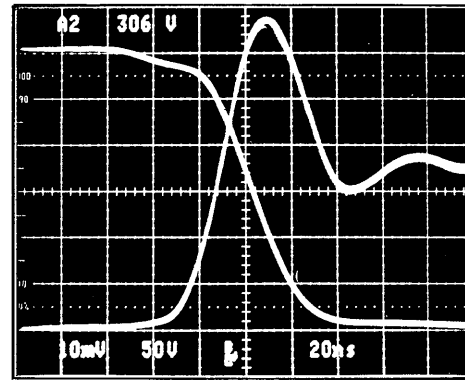
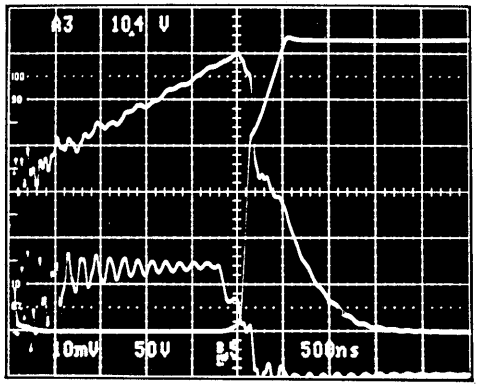


Figure 7 shows the behaviour in the case of a blocked rotor and with the current control set at the maximum 4A. This condition was simulated, as worst case, with and inductance of 300uH and a resistance of 1 Ω: the current does not exceed 6A. The overcurrent of 2A, with respect the control current of 4A, is due to the delay introduced by the network

of R7, C7 of about 2 μs. This filter network is necessary to suppress the leading edge spikes on the IC current sense comparator input.

Fig. 7 - Blocked rotor' beheaviour I_d= 1A/div, V_{ds}= 50V/div, V_g= 5V/div



The losses in the circuit, for the maximum rating of each component are approximately as follows: P(R1) = 2W, P(R3) = 3W, P(R2) = 3W, P(D1) = 4W, P(Tr1) = 7W.

CONCLUSION

A 300V 4A DC permanent magnet single quadrant motor drive was developed with objectives of maximum circuit simplicity and economy. Consequently a current mode PWM control with a popular IC was adopted and an STHI10N50 HIMOS (an IGBT) was used.

The low drive energy requirement due to the high input impedance of the HIMOS allows substantial cost reduction in the control circuit. Conductivity modulation of the drain produces a low ON resistance, an essential feature to work with high peak currents in the switching element. The ruggedness, due to the excellent safe operating areas, is especially relevant for motor control applications.

The easy drive, high current handling and excellent ruggedness make HIMOS the new way of power switching in the motor control field.

IMPROVED POWER MOSFET RUGGEDNESS IN UNCLAMPED INDUCTIVE SWITCHING

INTRODUCTION

Recent development work by SGS-Thomson has resulted in the production of POWER MOSFETs with improved performance in terms of unclamped inductive switching at high current values. This has lead to the production of a new class of POWER MOSFET device that operates reliably in application circuits even when accidental overvoltages may occur at high current, caused as a result of the high switching speed of POWER MOSFETs and random supply voltages.

POWER MOSFET devices have a clamped $E_{s/b}$ safe operating area that extends to the breakdown voltage. In some applications, such as SMPS and Motor Control, ruggedness of this nature can be insufficient because, during turn-off, the device can be stressed by random overvoltages at high drain current values so creating avalanche conditions.

SGS-Thomson is introducing this new POWER MOSFET generation guaranteed in terms of an unclamped inductive switching test (U.I.S.). The latter parameters meet real operating conditions found in Power applications.

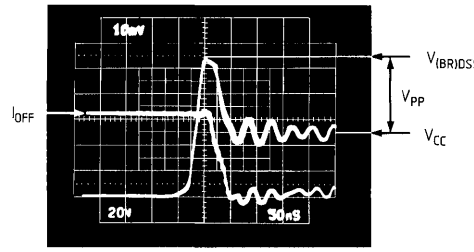
USEFUL PARAMETERS IN POWER MOSFET RUGGEDNESS

POWER MOSFETs are very fast switching devices and can generate high values of dI/dt (over 1000A/μs). For this reason, layout leakage inductance can create dangerous overvoltages. Photo 1 shows a POWER MOSFET drain current and voltage waveforms in a typical switching circuit (see figure 1). These current and voltage waveforms are typical in POWER MOSFET applications. It can be observed that the overvoltage exceeds the POWER MOSFET breakdown for very short times but at very high currents.

The energy dissipated in breakdown conditions in one cycle is very low,

$$E = 1/2\ LI^2 \frac{V_{(BR)\ DSS}}{V_{(BR)\ DSS} - V_{CC}} = 40\ \mu J,$$

Photo 1 - I = 5A/div, V = 20V/div
Turn-off with parasitic inductance ≃ 0.15uH e ≃ 40uJ



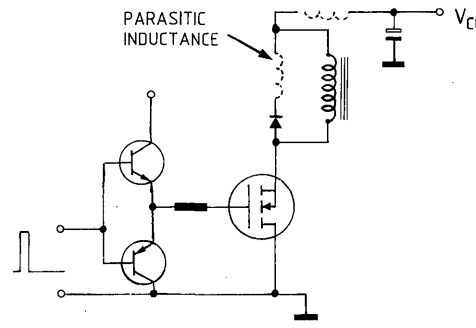
with a small duty cycle, but the initial breakdown currents are almost equal to those at turn-off.

It is important to test the device under actual operating conditions of voltage, current and working temperature typically found in actual applications.

THE FAILURE MECHANISM

Figure 2 shows possible current paths during breakdown. Current flows through the diffused body resistance and generates a voltage drop which

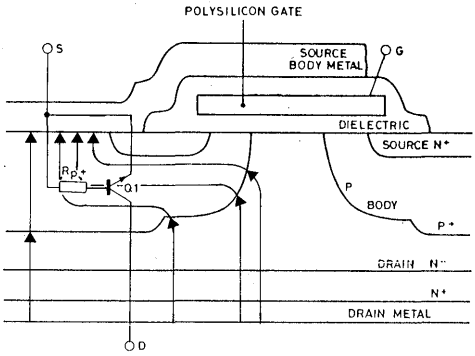
Fig. 1 - Typical circuit where breakdown can occur during turn-off



can be greater than the parasitic bipolar transistor threshold voltage. If turn-on of the parasitic bipo-

lar transistor occurs, the whole current is focused into a few cells destroying them. At increased temperature, this phenomenon happens at lower current values because the parasitic bipolar transistor threshold voltage decreases.

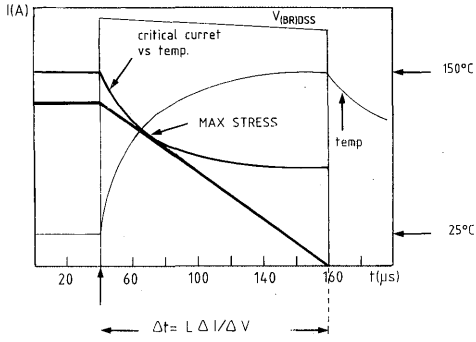
Fig. 2 - Cross section of a POWER MOSFET showing possible current paths during sustaining



Measurements show that failure current halves at $t_j = 150°C$ in comparison to the value of the current at $t_j = 25°C$.

The energy dissipated in the failure phenomenon is not important because if this were the case there would only be a thermal problem. Figure 3 shows current, voltage and temperature behaviour during turn-off with high inductive energy. The graph shows that at turn-off the temperature increases

Fig. 3 - Waveforms during turn-off, with a high energy value, L = 5mH

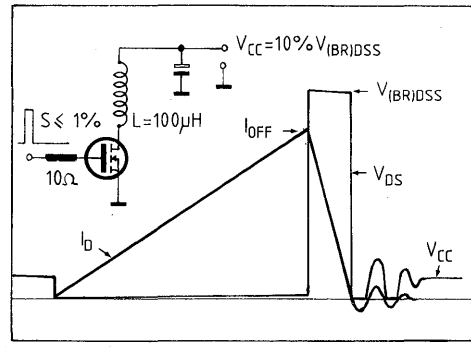


abruptly, and as a consequence, the critical current decreases so that, if critical current becomes less than the discharge current the device fails. Therefore it is possible to dissipate high inductive energy at a low current.

U.I.S. TEST

Fig. 4 shows the current and voltage diagrams for the U.I.S. test.

Fig. 4 - U.I.S. test waveforms and test circuit



Energy stored in the inductive load is dissipated in the device under test, D.U.T., during turn-off. Measurements are made bearing in mind the following criteria:

1) The energy is not the most important parameter causing device failure. Additionally, where the stored inductive energy has a high value, it is difficult to recognize the point at which maximum stress occurs during the discharge of the inductive load because there is an instantaneous increase of temperature, see figure 3.
2) In real application circuits, the device should only dissipate a little energy.
3) DUT's failure depends on initial breakdown current.
4) Junction temperature T_j is an important parameter.

For these reasons we chose a small value of inductive load - this avoids the device's failure being depend on thermal effects. The new generation of SGS-Thomson POWER MOSFETs are tested using the following test conditions:

for $T_j = 25°C$, $V_{dd} = 10\%\ V_{(BR)\ DSS}$ and L = 100uH and duty cycle $\leqslant 1\%$, $I_{off} = I_{nominal}$ (A) and $T_j = 100°C$, $V_{dd} = 10\%\ V_{(BR)\ DSS}$ and L = 100uH and duty cycle $\leqslant 1\%$, $I_{off} = O.7 \times I_{nominal}$ (A)

Fig. 5 - guaranteed breakdown current versus temperature, and failure point for IRF450, BUZ45, BUZ21

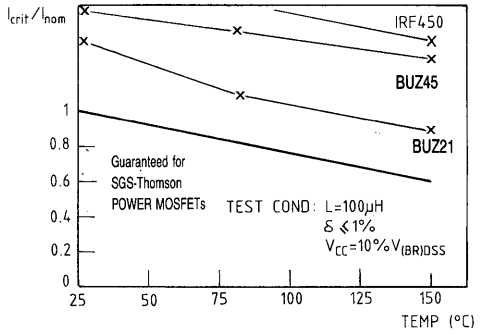


Figure 5 shows a temperature derating for guaranteed turn-off current (normalized at nominal current), where the three upper traces indicate the failure points for three different devices.

CONCLUSION

Usually an application circuit is designed in a way that avoids avalanche breakdown under normal operating conditions, for example using fast external clamping circuits. Occasional overvoltages, however, can stress the devices and create avalanche breakdown conditions.New SGS-Thomson POWER MOSFETs release circuit designers from this type of constraint.

DATASHEETS

SGS-THOMSON MICROELECTRONICS

BUZ10

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

ADVANCE DATA

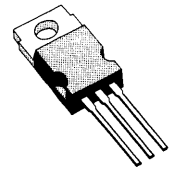
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ10	50 V	0.08 Ω	20 A

- HIGH SPEED SWITHING
- LOW $R_{DS\ (ON)}$
- EASY DRIVE FOR COST EFFECTIVE APPLICATIONS.

INDUSTRIAL APPLICATIONS:

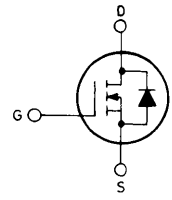
- AUTOMOTIVE POWER ACTUATOR DRIVES
- MOTOR CONTROLS
- DC-DC CONVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drives including brushless motors, hydraulic actuators and many other uses in automotive and automatic guided vehicle applications. It is also used in DC/DC converters and uninterruptible power supplies.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 30°C$	20	A
I_{DM}	Drain current (pulsed)	80	A
P_{tot}	Total dissipation at $T_c < 25°C$	70	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.78	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 13 A			0.1	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 13 A	8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		700 450 180		pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V		20 70 110 80		ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				20 20	A A
V_{SD}	Forward on voltage	I_{SD} = 40 A	V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time				150		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 20 A	di/dt = 100A/μs		1.0		μC

SGS-THOMSON MICROELECTRONICS

BUZ10A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

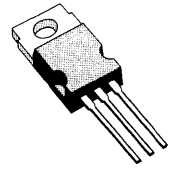
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ10A	50 V	0.12 Ω	17 A

- HIGH SPEED SWITCHING
- LOW $R_{DS\ (ON)}$
- EASY DRIVE FOR COST EFFECTIVE APPLICATIONS.

INDUSTRIAL APPLICATIONS:

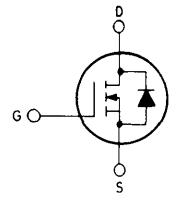
- AUTOMOTIVE POWER ACTUATOR DRIVES
- MOTOR CONTROLS
- DC-DC CONVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching circuits in applications such as power actuator driving, motor drives including brushless motors, hydraulic actuators and many other uses in automotive and automatic guided vehicle applications. It is also used in DC/DC converters and uninterruptible power supplies.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=30°C$	17	A
I_{DM}	Drain current (pulsed)	65	A
P_{tot}	Total dissipation at $T_c<25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

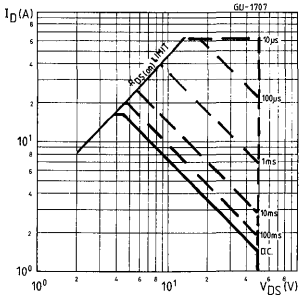
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 1 mA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 10 A			0.12	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 10 A	3.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 800 300	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3.0 A V_{GS} = 10 V			45 90 170 140	ns ns ns ns

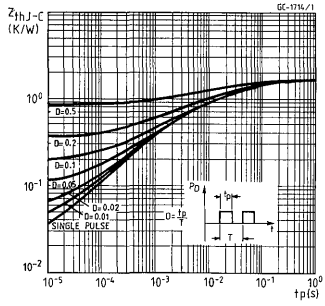
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				17 65	A A
V_{SD}	Forward on voltage	I_{SD} = 34 A	V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time				150		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 17 A	di/dt = 100A/μs		1.0		μC

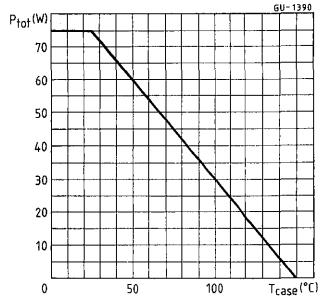
Safe operating areas



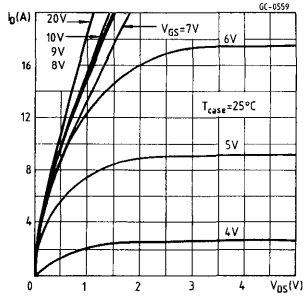
Thermal impedance



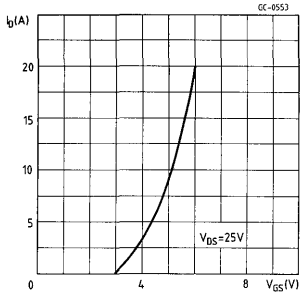
Derating curve



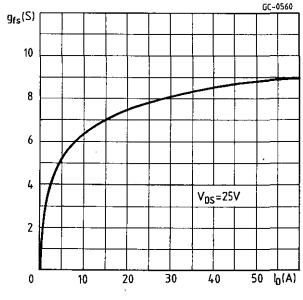
Output characteristics



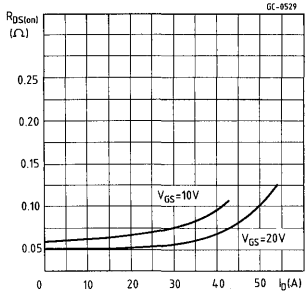
Transfer characteristics



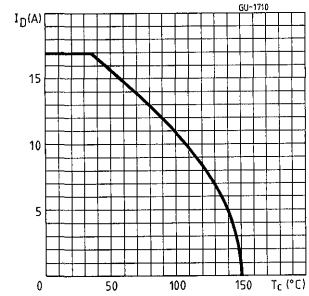
Transconductance



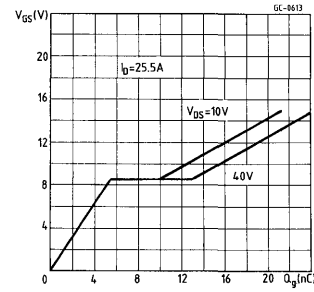
Static drain-source on resistance



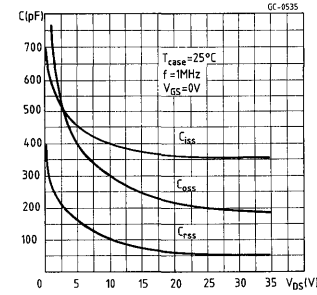
Maximum drain current vs temperature



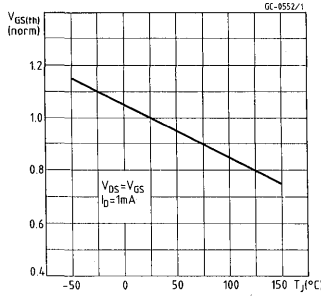
Gate charge vs gate-source voltage



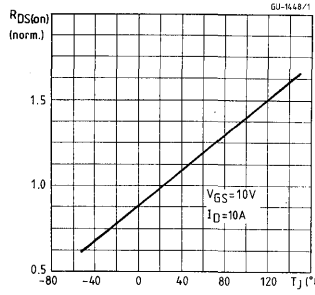
Capacitance variation



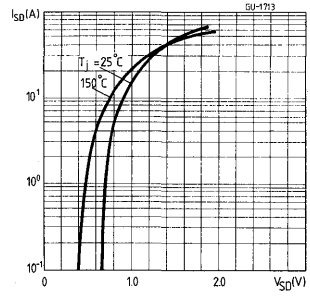
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ11
BUZ11FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

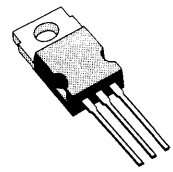
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ11	50 V	0.04 Ω	30 A
BUZ11FI	50 V	0.04 Ω	20 A

- HIGH SPEED SWITCHING
- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO

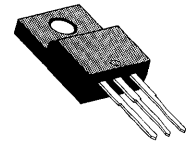
INDUSTRIAL APPLICATIONS:

- AUTOMATIVE POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. They also find use in DC/DC converters and uninterruptible power supplies.

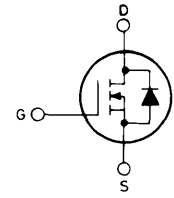


TO-220



ISOWATT 220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50		V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50		V
V_{GS}	Gate-source voltage	±20		V
I_{DM}	Drain current (pulsed) $T_c=25°C$	120		A
		BUZ 11	**BUZ11FI**	
I_D ■	Drain current (continuous) $T_c=30°C$	30	20	A
P_{tot} ■	Total dissipation at $T_c<25°C$	75	35	W
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C
	DIN humidity category (DIN 40040)	E		
	IEC climatic category (DIN IEC 68-1)	55/150/56		

■ See note on ISOWATT 220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT 220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 15 A			0.04	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 15 A	4			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 1100 400	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 110 230 170	ns ns ns ns

■ See note on ISOWATT 220 in this datasheet

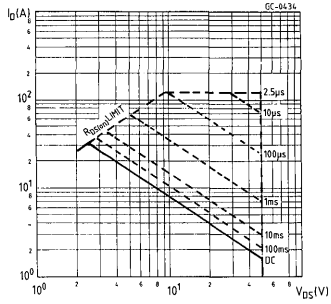
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

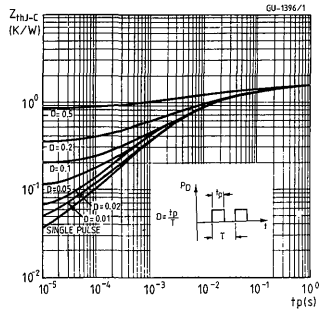
SOURCE DRAIN DIODE

I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C			30 120	A A
V_{SD}	Forward on voltage	I_{SD} = 60 A	V_{GS} = 0		2.6	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 30 A	di/dt = 100A/μs	200 0.25		ns μC

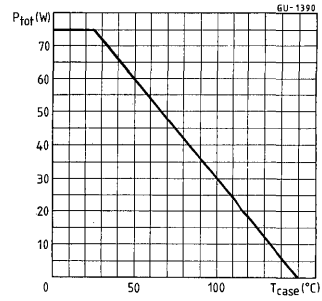
Safe operating areas (standard package)



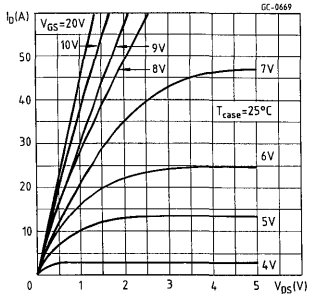
Thermal impedance (standard package)



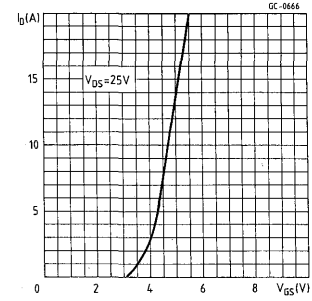
Derating curve (standard package)



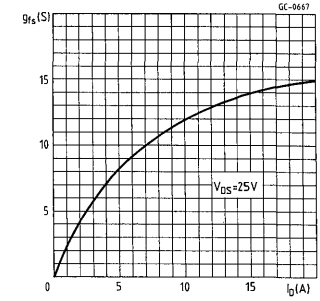
Output characteristics



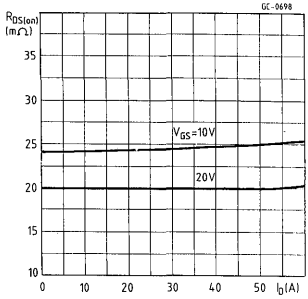
Transfer characteristics



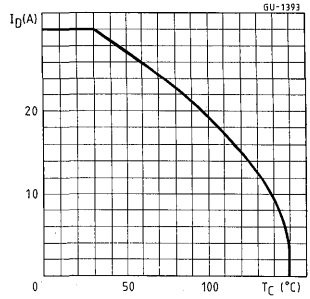
Transconductance



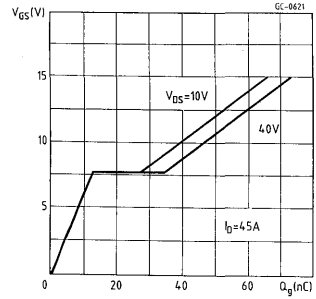
Static drain-source on resistance



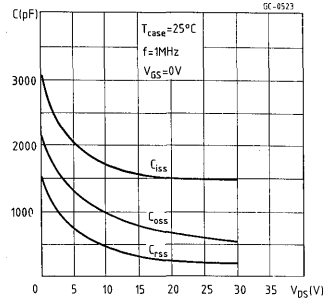
Maximum drain current vs temperature



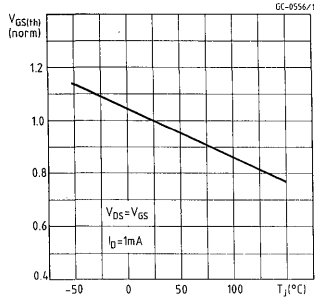
Gate charge vs gate-source voltage



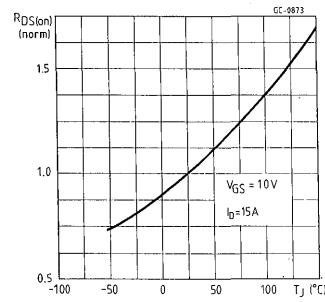
Capacitance variation



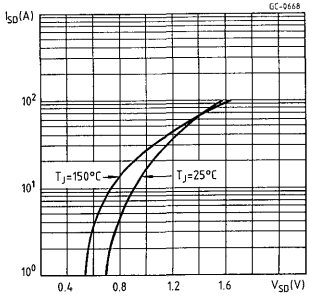
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

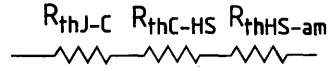
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

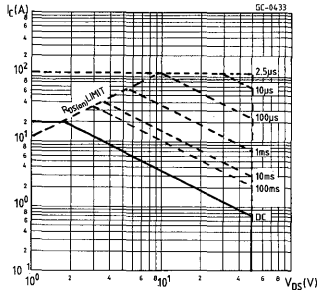
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

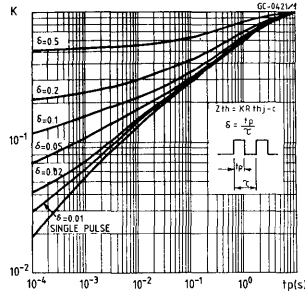


ISOWATT DATA

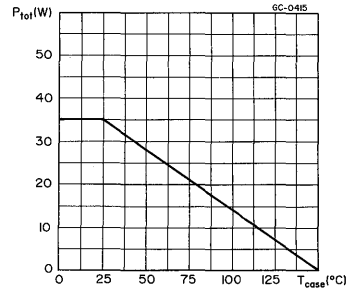
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

BUZ11A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

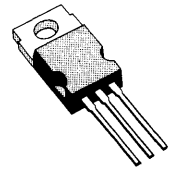
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ11A	50 V	0.06 Ω	25 A

- HIGH CURRENT
- ULTRA FAST SWITCHING
- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE

INDUSTRIAL APPLICATIONS:

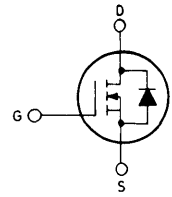
- AUTOMOTIVE POWER ACTUATORS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical uses include power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. It also finds use in DC/DC converters and uninteruptible power supplies.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=25°C$	25	A
I_{DM}	Drain current (pulsed)	100	A
P_{tot}	Total dissipation at $T_c<25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

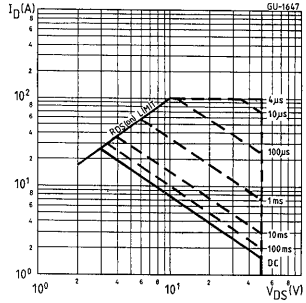
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 15 A			0.06	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 15 A	4.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 1100 400	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 110 230 170	ns ns ns ns

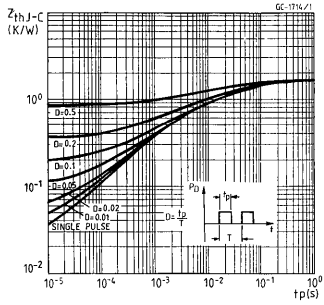
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)	T_c = 25°C			25 100	A A
V_{SD} Forward on voltage	I_{SD} = 50 A V_{GS} = 0			2.4	V
t_{rr} Reverse recovery time			200		ns
Q_{rr} Reverse recovered charge	I_{SD} = 25 A di/dt = 100A/μs		0.25		μC

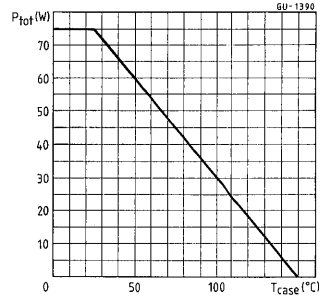
Safe operating areas



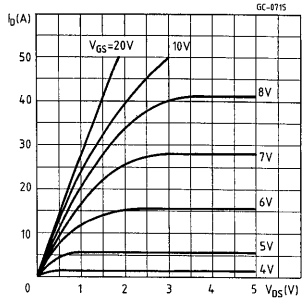
Thermal impedance



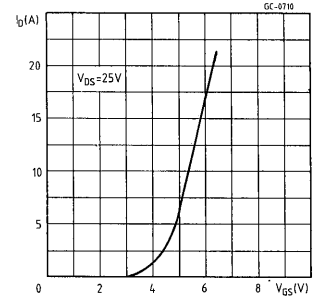
Derating curve



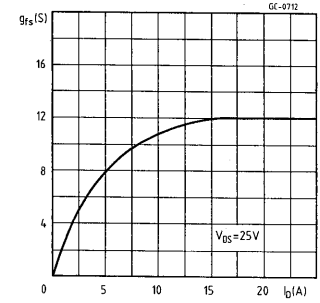
Output characteristics



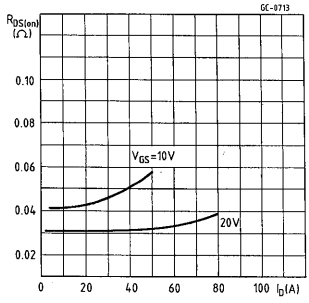
Transfer characteristics



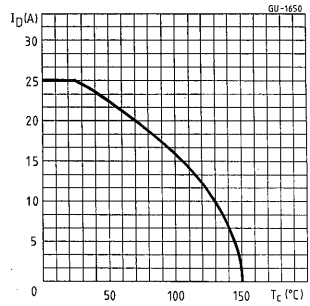
Transconductance



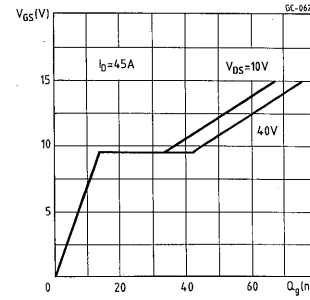
Static drain-source on resistance



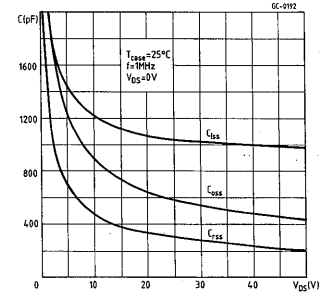
Maximum drain current vs temperature



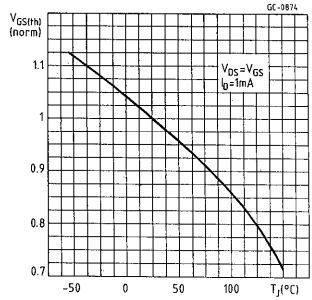
Gate charge vs gate-source voltage



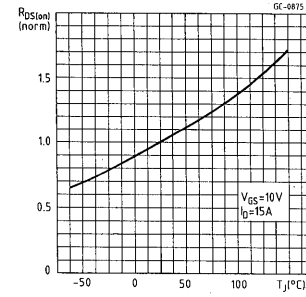
Capacitance variation



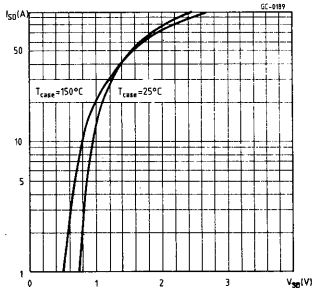
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ11S2
BUZ11S2FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

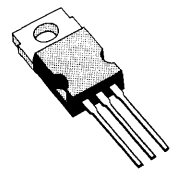
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ11S2	60 V	0.04 Ω	30 A
BUZ11S2FI	60 V	0.04 Ω	20 A

- VERY LOW ON-LOSSES
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO

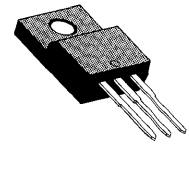
INDUSTRIAL APPLICATIONS:

- AUTOMATIVE POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications. They also find use in DC/DC converters and uninterruptible power supplies.

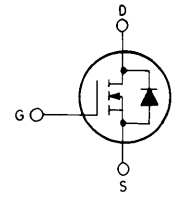


TO-220



ISOWATT 220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	60		V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60		V
V_{GS}	Gate-source voltage	±20		V
I_{DM}	Drain current (pulsed) $T_c=25°C$	120		A
		BUZ11S2	**BUZ11S2FI**	
I_D ■	Drain current (continuous) $T_c=30°C$	30	20	A
P_{tot} ■	Total dissipation at $T_c<25°C$	75	35	W
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C
	DIN humidity category (DIN 40040)	E		
	IEC climatic category (DIN IEC 68-1)	55/150/56		

■ See note on ISOWATT 220 in this datasheet

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	3.57	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

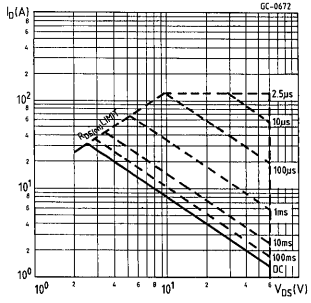
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 15 A			0.04	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 15 A	4			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 1100 400	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 110 230 170	ns ns ns ns

▪ See note on ISOWATT 220 in this datasheet

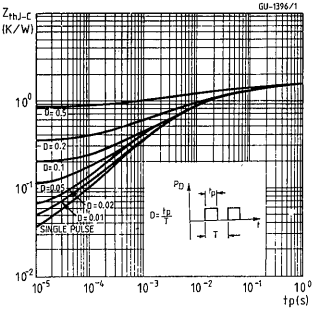
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				30 120	A A
V_{SD}	Forward on voltage	I_{SD} = 60 A	V_{GS} = 0			2.6	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A	di/dt = 100A/μs		200		ns
Q_{rr}	Reverse recovered charge				0.25		μC

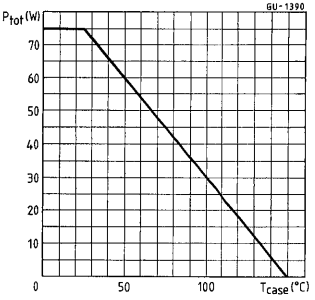
Safe operating areas (standard package)



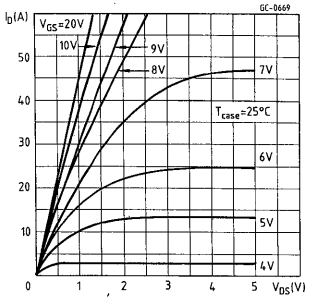
Thermal impedance (standard package)



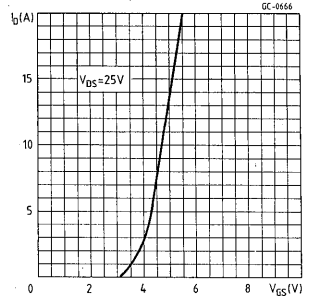
Derating curve (standard package)



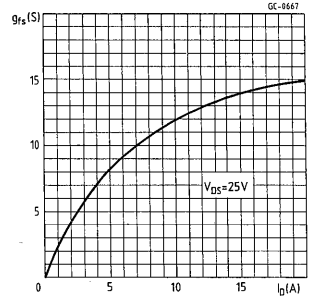
Output characteristics



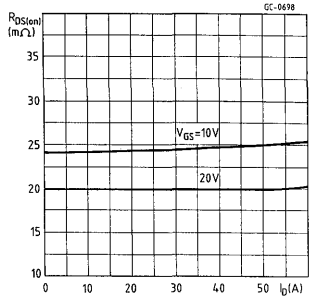
Transfer characteristics



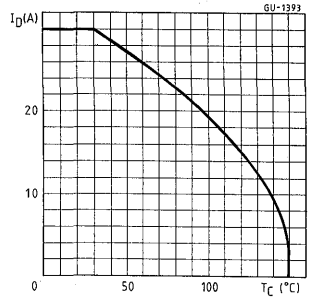
Transconductance



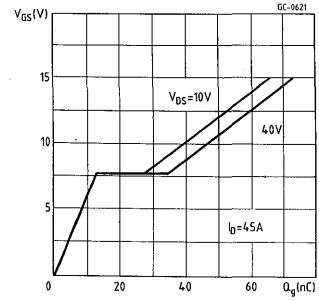
Static drain-source on resistance



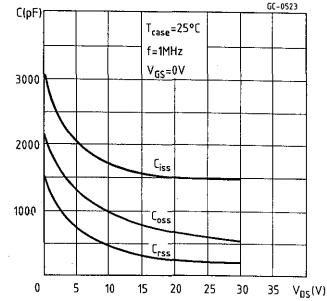
Maximum drain current vs temperature



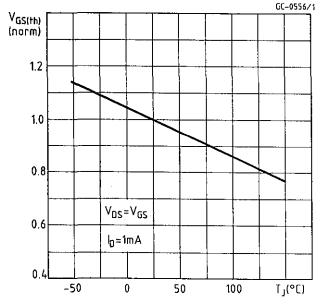
Gate charge vs gate-source voltage



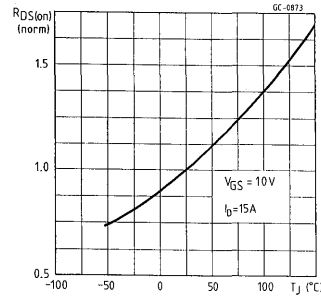
Capacitance variation



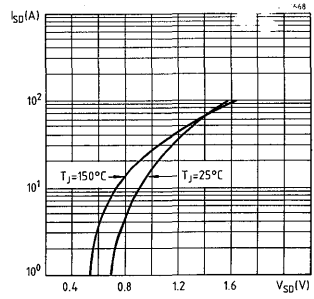
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better the that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

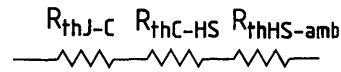
$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

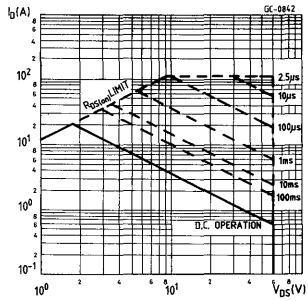
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

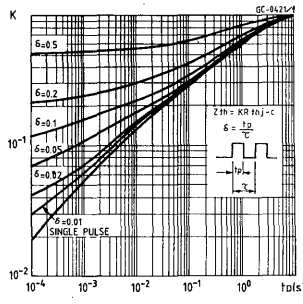


ISOWATT DATA

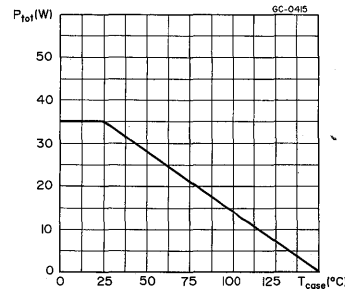
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

BUZ20

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

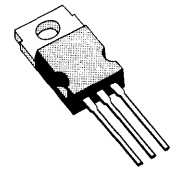
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ20	100 V	0.2 Ω	12 A

- 100 VOLTS - FOR UPS APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE - FOR REDUCED AND COST

INDUSTRIAL APPLICATIONS:

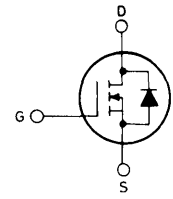
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) T_c = 25°C	12	A
I_{DM}	Drain current (pulsed)	48	A
P_{tot}	Total dissipation at T_c < 25°C	75	W
T_{stg}	Storage temperature	− 55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

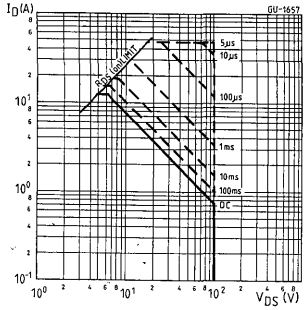
ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$	$V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating	 $T_j = 125°C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V				± 100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 1$ mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 10$ V	$I_D = 6$ A			0.2	Ω
ENERGY TEST							
I_{UIS}	Unclamped inductive switching current (single pulse)	$V_{DD} = 30$ V starting $T_j = 25°C$	$L = 100\ \mu H$	12			A
DYNAMIC							
g_{fs}	Forward transconductance	$V_{DS} = 25$ V	$I_D = 6$ A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V $V_{GS} = 0$	$f = 1$ MHz			2000 500 140	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 30$ V $R_{GS} = 50\ \Omega$	$I_D = 2.9$ A $V_{GS} = 10$ V			45 75 140 80	ns ns ns ns

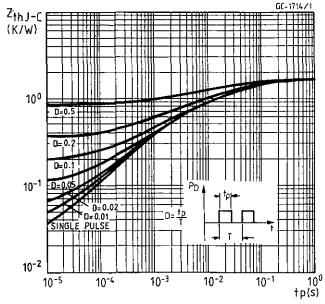
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				12 48	A A
V_{SD}	Forward on voltage	I_{SD} = 24 A	V_{GS} = 0			1.8	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A	di/dt = 100A/μs		200		ns
Q_{rr}	Reverse recovered charge				1.6		μC

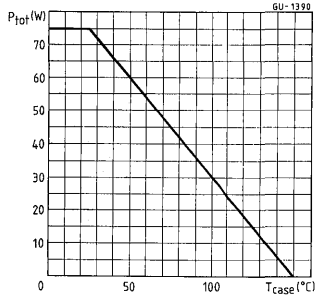
Safe operating areas



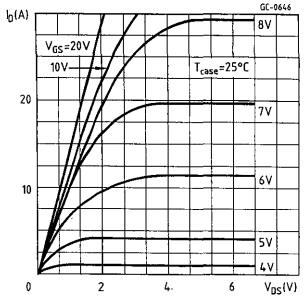
Thermal impedance



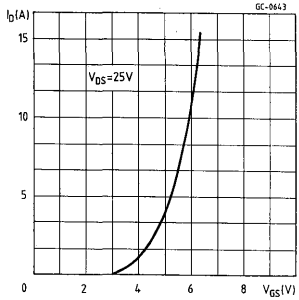
Derating curve



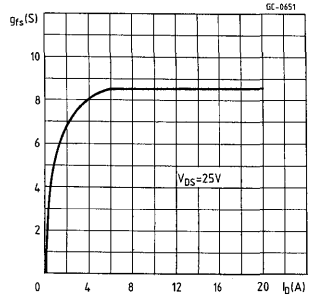
Output characteristics



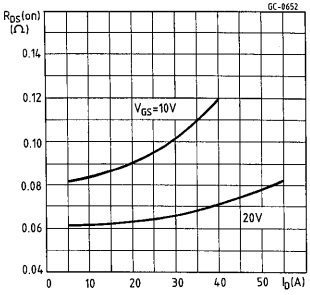
Transfer characteristics



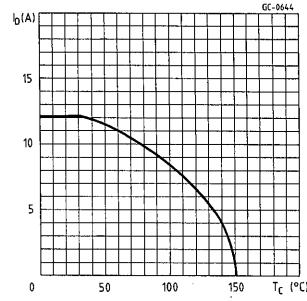
Transconductance



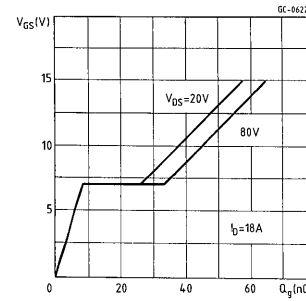
Static drain-source on resistance



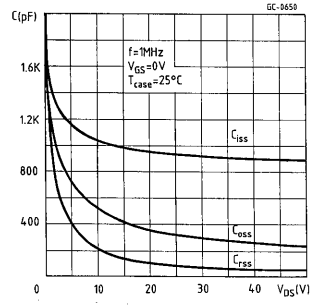
Maximum drain current vs temperature



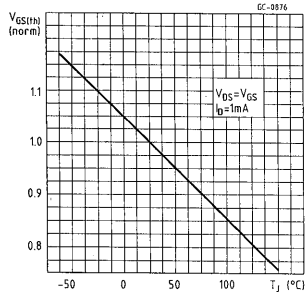
Gate charge vs gate-source voltage



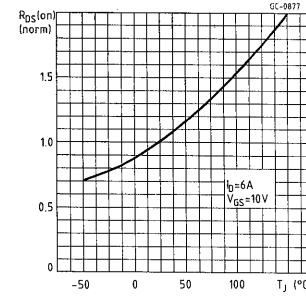
Capacitance variation



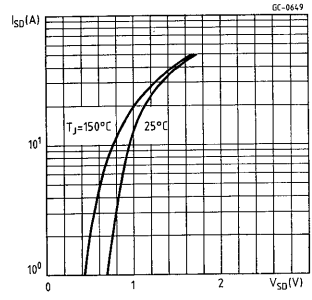
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ21

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

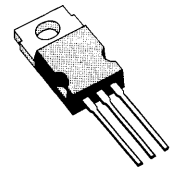
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ21	100 V	0.1 Ω	19 A

- 100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

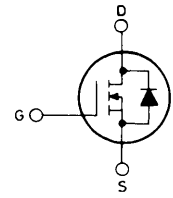
- UNINTERRUPTABLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include DC/DC converters, UPS, battery chargers, secondary regulators servo control, audio power amplifiers and robotics.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=30°C$	19	A
I_{DM}	Drain current (pulsed)	75	A
P_{tot}	Total dissipation at $T_c<25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

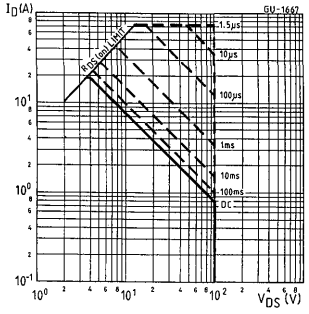
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 9 A			0.1	Ω
ENERGY TEST							
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V starting T_j = 25°C	L = 100 μH	19			A
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 9 A	4.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 700 240	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 75 220 110	ns ns ns ns

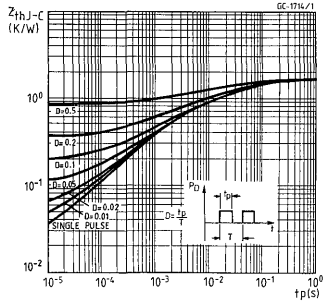
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)	T_c = 25°C			19 75	A A
V_{SD} Forward on voltage	I_{SD} = 38 A V_{GS} = 0			2.1	V
t_{rr} Reverse recovery time	I_{SD} = 19 A di/dt = 100A/μs		200		ns
Q_{rr} Reverse recovered charge			0.25		μC

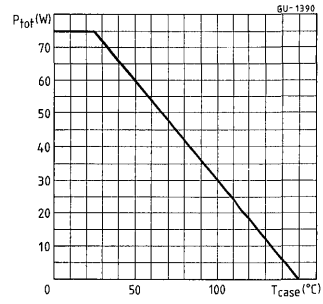
Safe operating areas



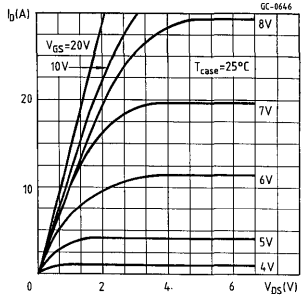
Thermal impedance



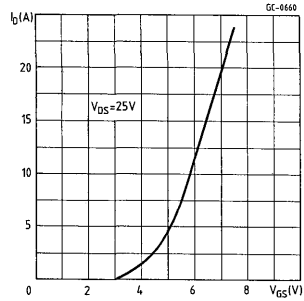
Derating curve



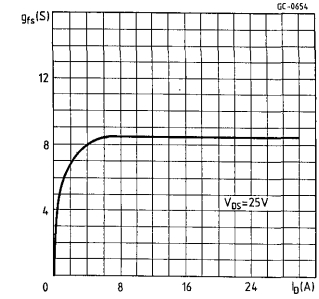
Output characteristics



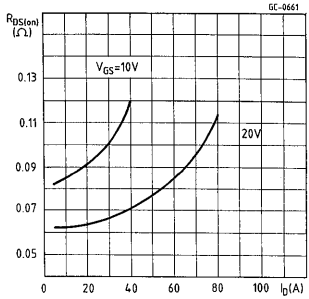
Transfer characteristics



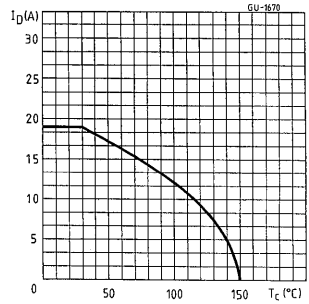
Transconductance



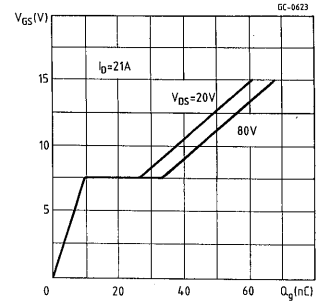
Static drain-source on resistance



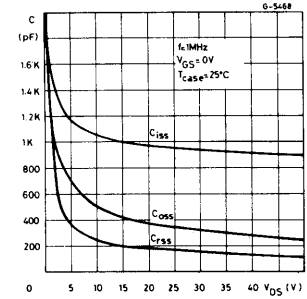
Maximum drain current vs temperature



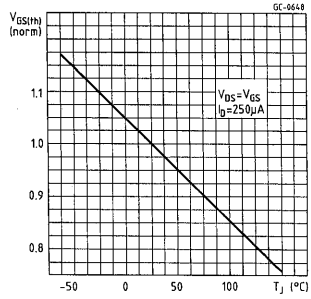
Gate charge vs gate-source voltage



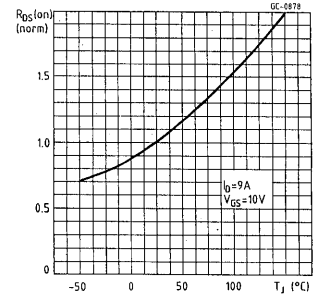
Capacitance variation



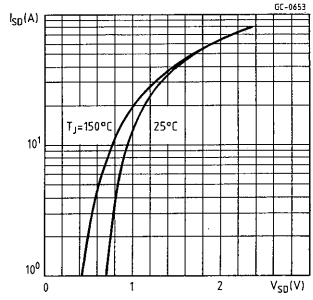
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ25

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

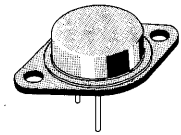
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ25	100 V	0.1 Ω	19 A

- 100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

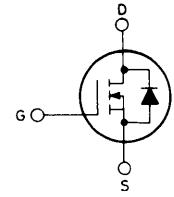
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power audio amplifiers and robotics.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=35°C$	19	A
I_{DM}	Drain current (pulsed)	75	A
P_{tot}	Total dissipation at $T_c<25°C$	78	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	C	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.6	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	35	°C/W

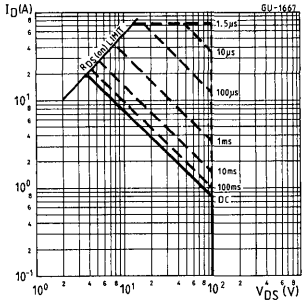
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 9 A			0.1	Ω
ENERGY TEST							
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V starting T_j = 25°C	L = 100 μH	19			A
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 9 A	4.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 700 240	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			45 75 220 110	ns ns ns ns

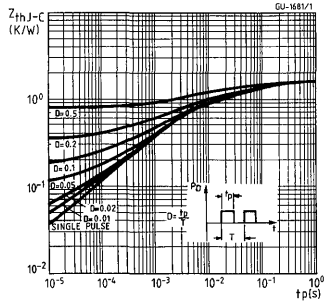
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)	T_c = 25°C			19 75	A A
V_{SD} Forward on voltage	I_{SD} = 38 A V_{GS} = 0			2.1	V
t_{rr} Reverse recovery time			200		ns
Q_{rr} Reverse recovered charge	I_{SD} = 19 A di/dt = 100A/μs		0.25		μC

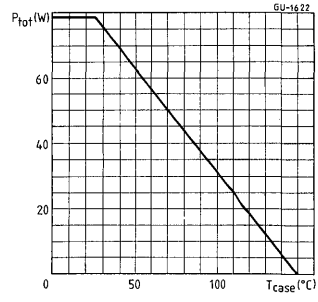
Safe operating areas



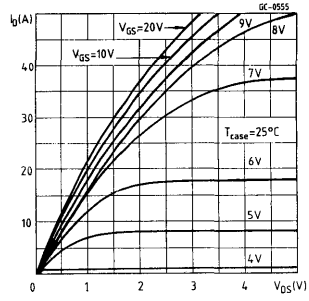
Thermal impedance



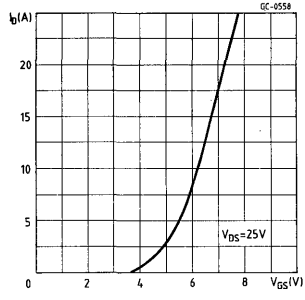
Derating curve



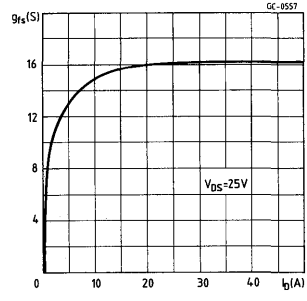
Output characteristics



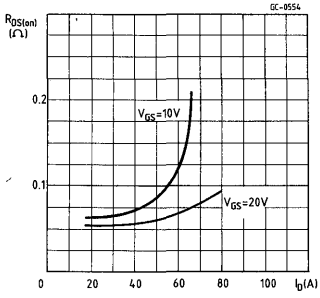
Transfer characteristics



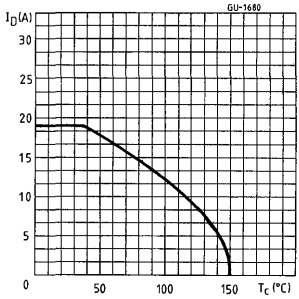
Transconductance



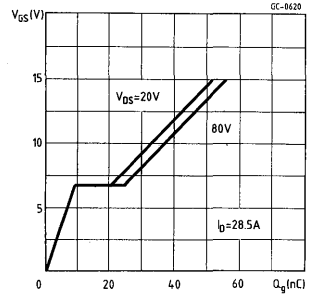
Static drain-source on resistance



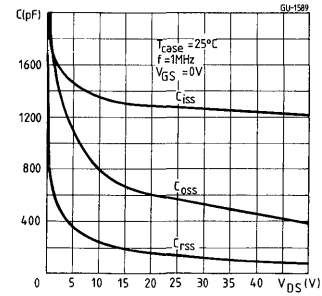
Maximum drain current vs temperature



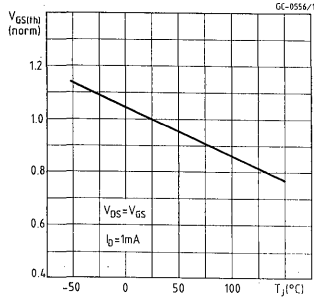
Gate charge vs gate-source voltage



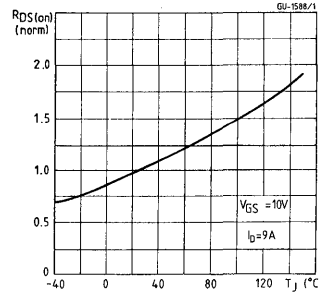
Capacitance variation



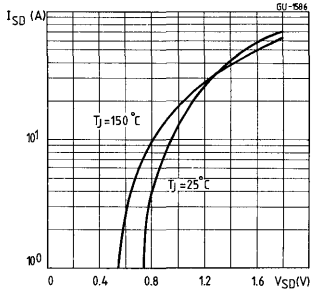
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ32

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

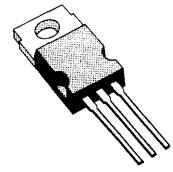
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ32	200 V	0.4 Ω	9.5 A

- 200 VOLTS FOR TELECOMS APPLICATIONS
- HIGH CURRENT - FOR PULSED LASER DRIVES
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS FOR ROBOTICS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical uses include robotcs, laser diode drives, UPS, SMPS, DC/DC, DC switch for telecomms and electric vehicle drives.



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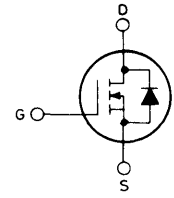
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 25°C$	9.5	A
I_{DM}	Drain current (pulsed)	38	A
P_{tot}	Total dissipation at $T_c < 25°C$	75	W
T_{stg}	Storage temperature	− 55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

◆ Introduced in 1989 week 1

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

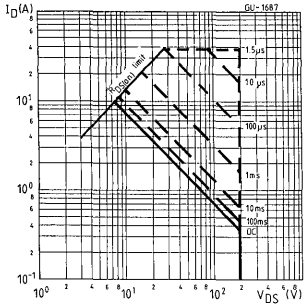
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 4.5 A			0.4	Ω
ENERGY TEST							
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V starting T_j = 25°C	L = 100 μH	9.5			A
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 4.5 A	2.2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 400 120	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.9 A V_{GS} = 10 V			45 60 140 80	ns ns ns ns

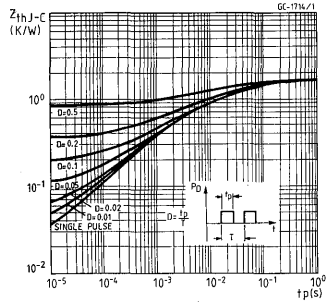
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				9.5 38	A A
V_{SD}	Forward on voltage	I_{SD} = 19 A	V_{GS} = 0			1.7	V
t_{rr}	Reverse recovery time	I_{SD} = 9.5 A	di/dt = 100A/μs		400		ns
Q_{rr}	Reverse recovered charge				6		μC

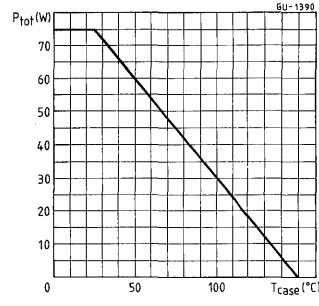
Safe operating areas



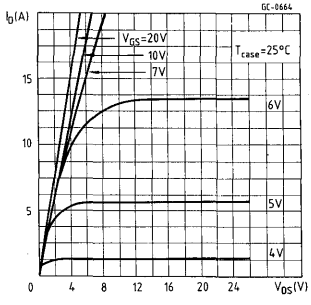
Thermal impedance



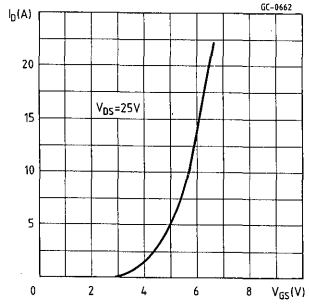
Derating curve



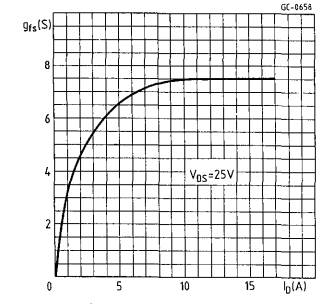
Output characteristics



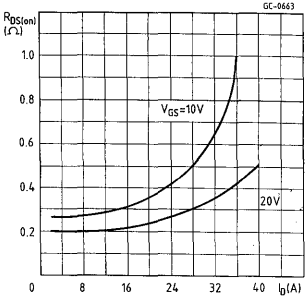
Transfer characteristics



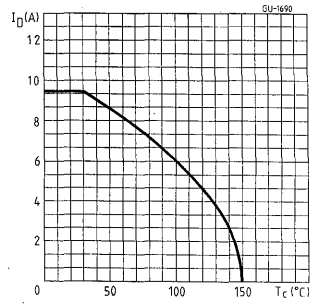
Transconductance



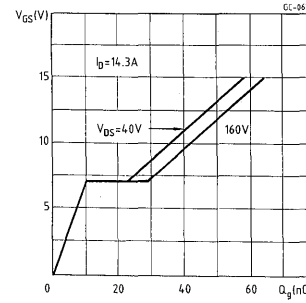
Static drain-source on resistance



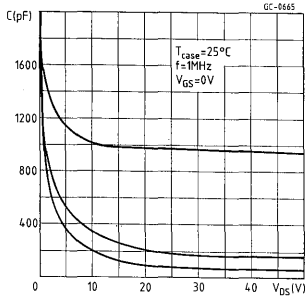
Maximum drain current vs temperature



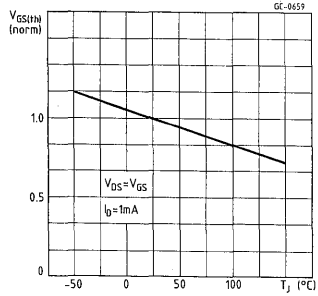
Gate charge vs gate-source voltage



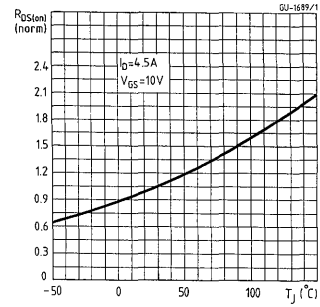
Capacitance variation



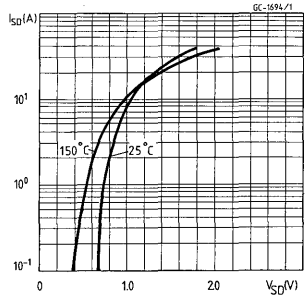
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ41A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

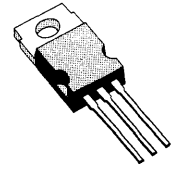
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ41A	500 V	1.5 Ω	4.5 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT < 100KHz
- EASY DRIVE - FOR REDUCED COST AND COST

INDUSTRIAL APPLICATIONS:

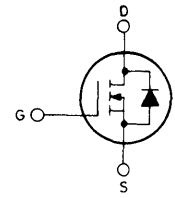
- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching power supplies and motor speed control.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) T_c = 35°C	4.5	A
I_{DM}	Drain current (pulsed)	18	A
P_{tot}	Total dissipation at T_c < 25°C	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - amb}}$	Thermal resistance junction-ambient	max	75	°C/W

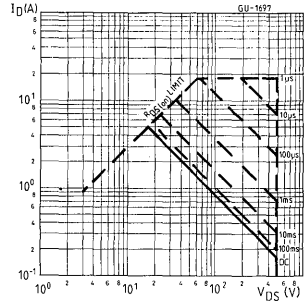
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2.5 A			1.5	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2.5 A	1.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 170 70	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.6 A V_{GS} = 10 V			45 60 140 65	ns ns ns ns

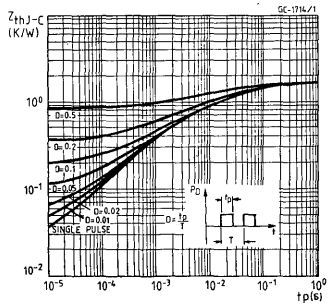
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				4.5 18	A A
V_{SD}	Forward on voltage	I_{SD} = 9 A	V_{GS} = 0			1.5	V
t_{rr} Q_{rr}	Reverve recovery time Reverse recovered charge	I_{SD} = 4.5 A	di/dt = 100A/μs		1200 6		ns μC

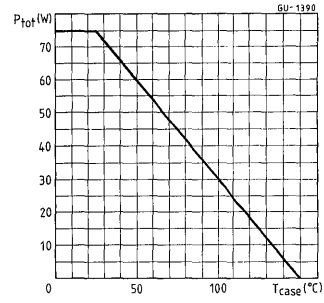
Safe operating areas



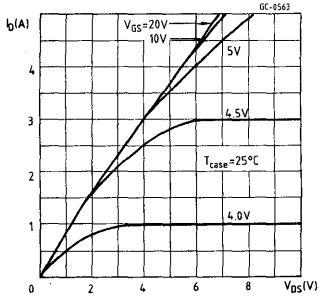
Thermal impedance



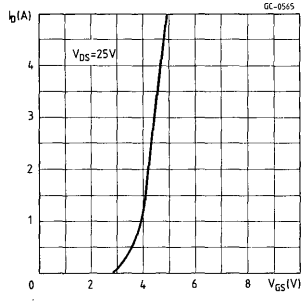
Derating curve



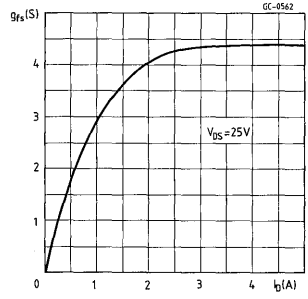
Output characteristics



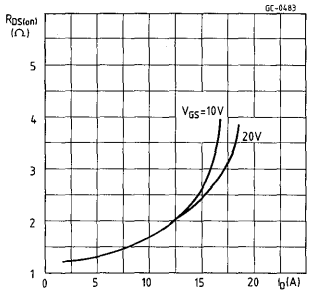
Transfer characteristics



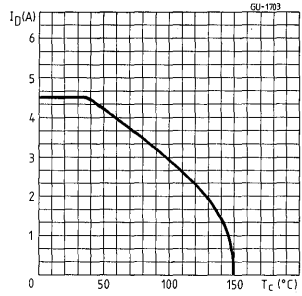
Transconductance



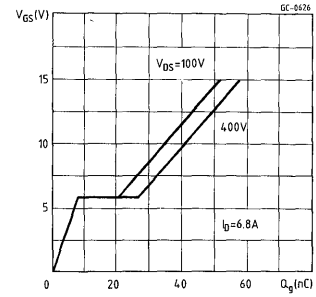
Static drain-source on resistance



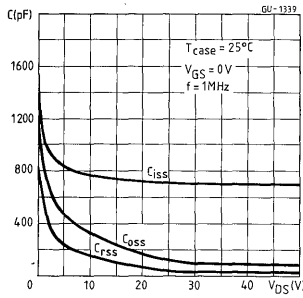
Maximum drain current vs temperature



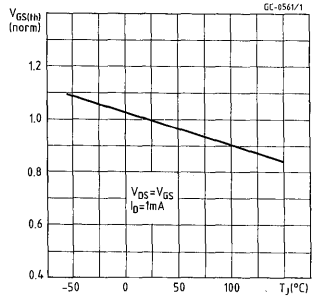
Gate charge vs gate-source voltage



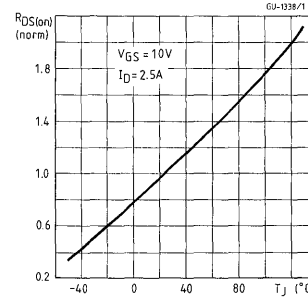
Capacitance variation



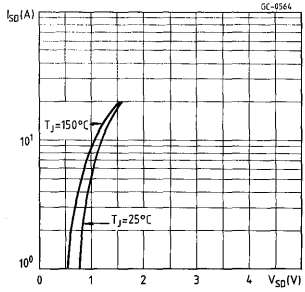
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ42

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

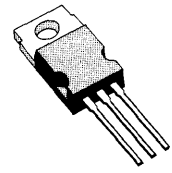
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ42	500 V	2 Ω	4 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT < 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching power supplies and motor speed control.



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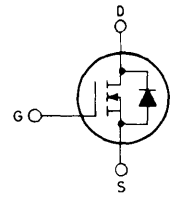
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 30°C$	4	A
I_{DM}	Drain current (pulsed)	16	A
P_{tot}	Total dissipation at $T_c < 25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

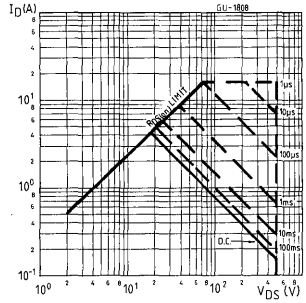
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2.5 A			2	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2.5 A	1.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 170 70	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.5 A V_{GS} = 10 V			45 60 140 65	ns ns ns ns

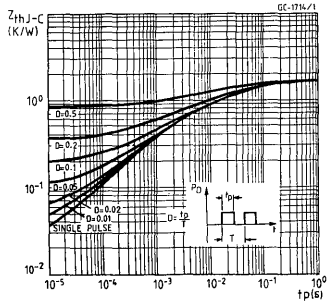
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				4 16	A A
V_{SD}	Forward on voltage	I_{SD} = 8 A	V_{GS} = 0			1.5	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 4 A	di/dt = 100A/μs		1200 6		ns μC

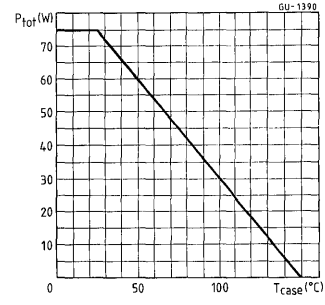
Safe operating areas



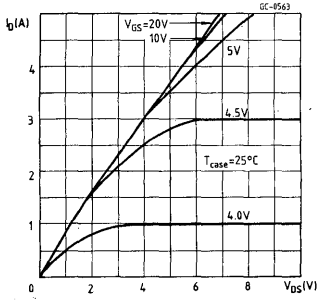
Thermal impedance



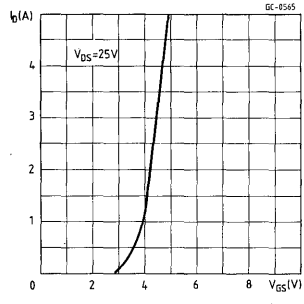
Derating curve



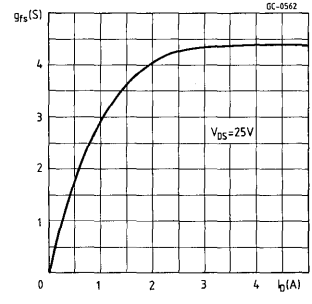
Output characteristics



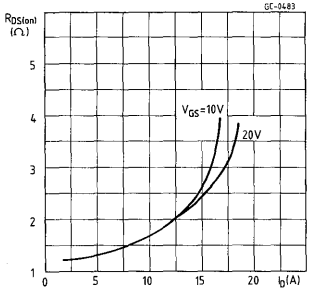
Transfer characteristics



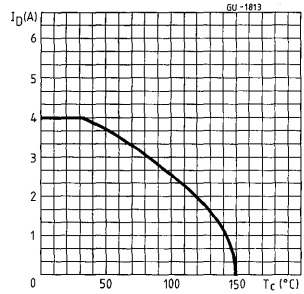
Transconductance



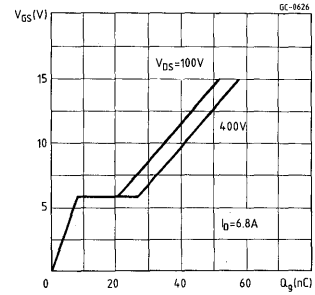
Static drain-source on resistance



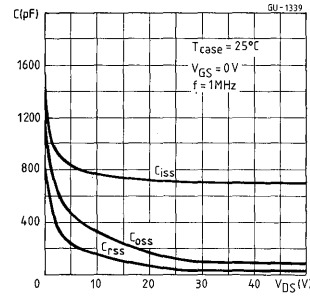
Maximum drain current vs temperature



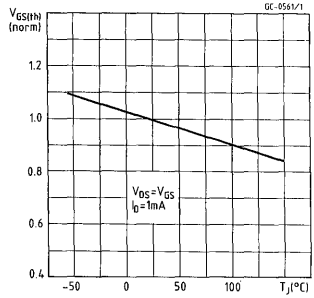
Gate charge vs gate-source voltage



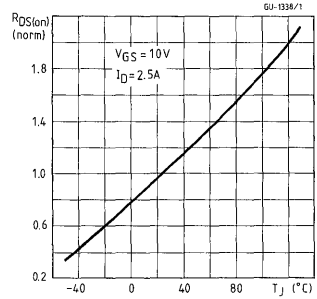
Capacitance variation



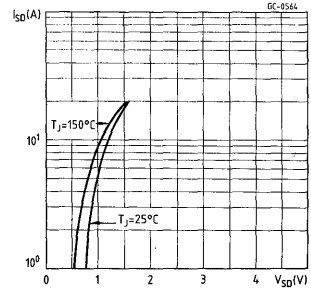
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ45

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

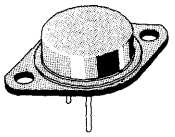
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ45	500 V	0.6 Ω	9.6 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT < 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

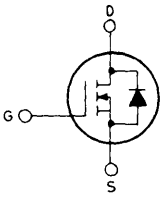
- SWITCH MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching power supplies and motor speed control.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 25°C$	9.6	A
I_{DM}	Drain current (pulsed)	38	A
P_{tot}	Total dissipation at $T_c < 25°C$	125	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	C	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.0	°C/W
$R_{thj\text{ - amb}}$	Thermal resistance junction-ambient	max	35	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$	$V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} =$ Max Rating $V_{DS} =$ Max Rating	 $T_j = 125°C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V				± 100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 1$ mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 10$ V	$I_D = 5$ A			0.6	Ω
DYNAMIC							
g_{fs}	Forward transconductance	$V_{DS} = 25$ V	$I_D = 5$ A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V $V_{GS} = 0$	$f = 1$ MHz			4900 400 170	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 30$ V $R_{GS} = 50\ \Omega$	$I_D = 2.8$ A $V_{GS} = 10$ V			75 120 430 140	ns ns ns ns

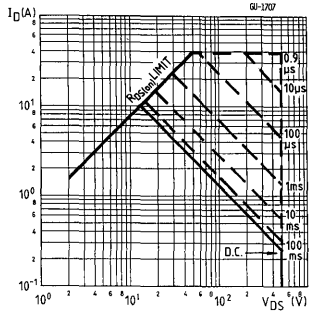
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

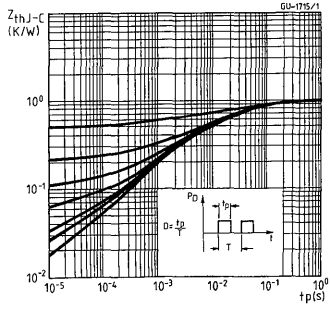
SOURCE DRAIN DIODE

I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C			9.6 38	A A
V_{SD}	Forward on voltage	I_{SD} = 19.2 A V_{GS} = 0			1.7	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 9.6 A di/dt = 100A/μs		1200 12		ns μC

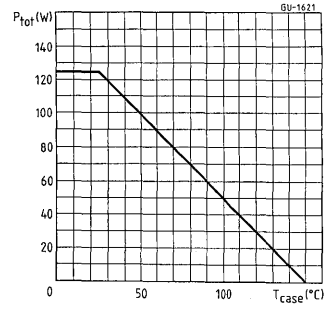
Safe operating areas



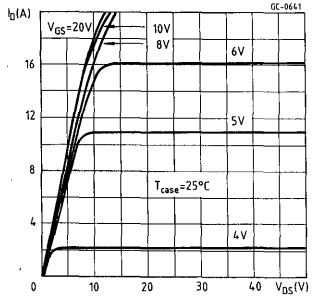
Thermal impedance



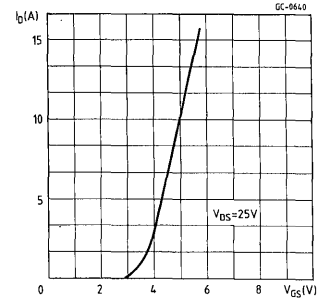
Derating curve



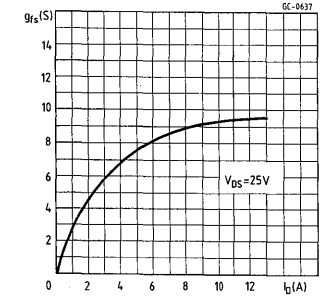
Output characteristics



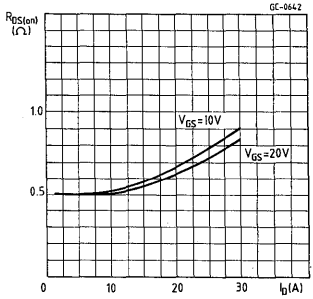
Transfer characteristics



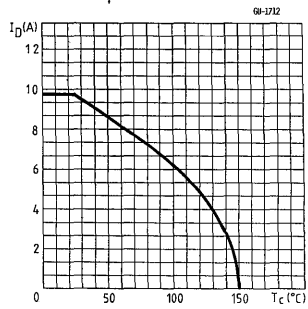
Transconductance



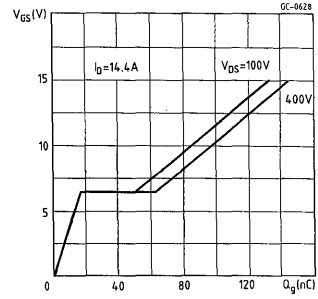
Static drain-source on resistance



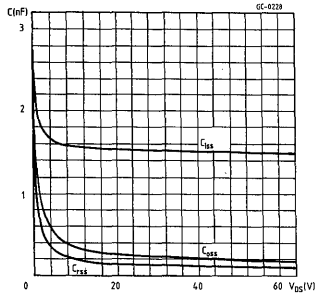
Maximum drain current vs temperature



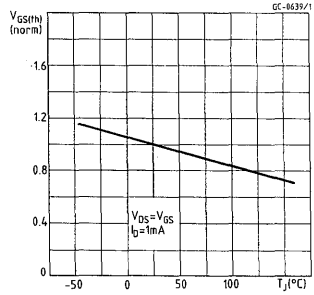
Gate charge vs gate-source voltage



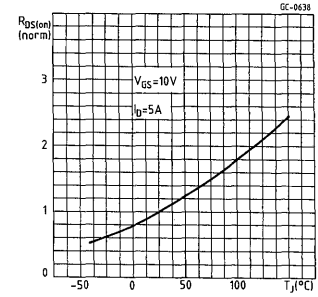
Capacitance variation



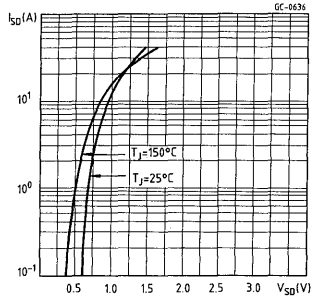
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ45A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

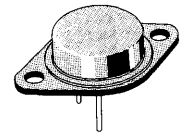
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ45A	500 V	0.8 Ω	8.3 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT < 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

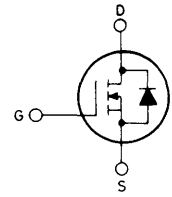
- SWITCH MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching power supplies, uninterruptable power supplies and motor speed control.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 25°C$	8.3	A
I_{DM}	Drain current (pulsed)	33	A
P_{tot}	Total dissipation at $T_c < 25°C$	125	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	C	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.0	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 5 A			0.8	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 5 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			4900 400 170	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.8 A V_{GS} = 10 V			75 120 430 140	ns ns ns ns

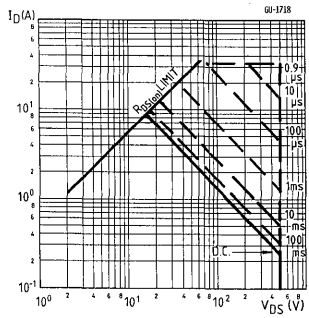
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

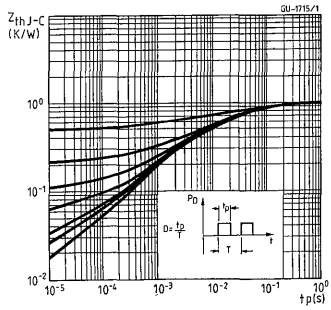
SOURCE DRAIN DIODE

I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C			8.3 33	A A
V_{SD}	Forward on voltage	I_{SD} = 16.6 A	V_{GS} = 0		1.6	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 8.3 A	di/dt = 100A/μs	1200 12		ns μC

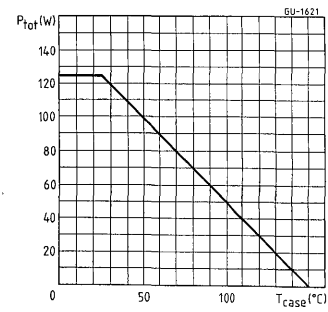
Safe operating areas



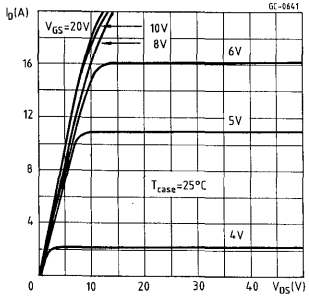
Thermal impedance



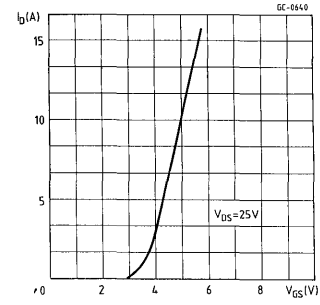
Derating curve



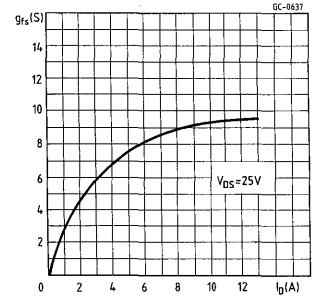
Output characteristics



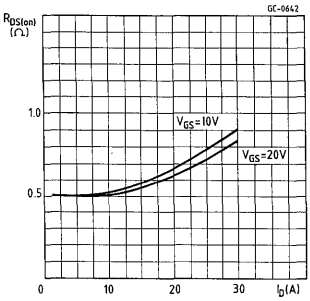
Transfer characteristics



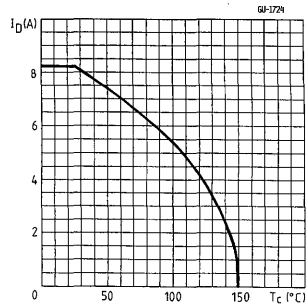
Transconductance



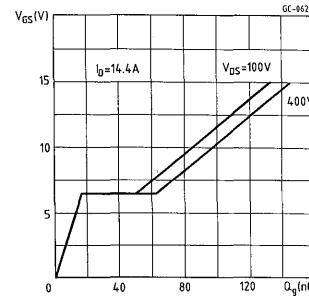
Static drain-source on resistance



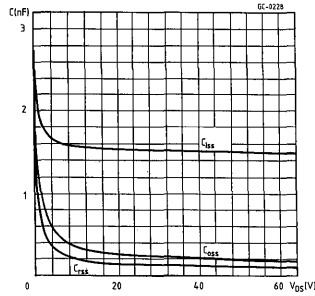
Maximum drain current vs temperature



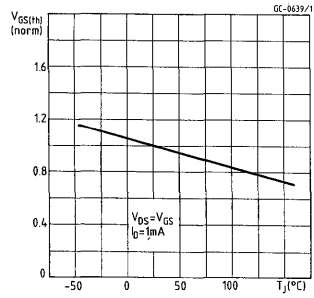
Gate charge vs gate-source voltage



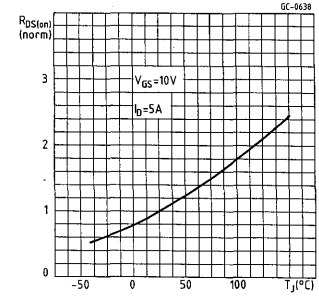
Capacitance variation



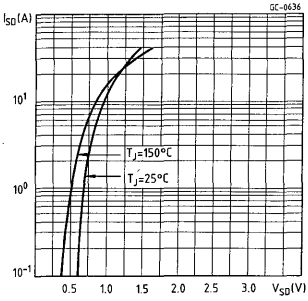
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ60

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

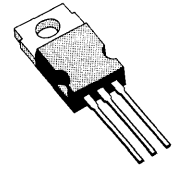
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ60	400 V	1.0 Ω	5.5 A

- HIGH VOLTAGE - FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

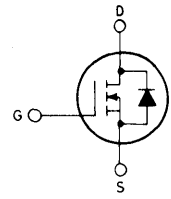
- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=35°C$	5.5	A
I_{DM}	Drain current (pulsed)	22	A
P_{tot}	Total dissipation at $T_c<25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2.5 A			1.0	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2.5 A	1.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 180 60	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.7 A V_{GS} = 10 V			45 60 140 65	ns ns ns ns

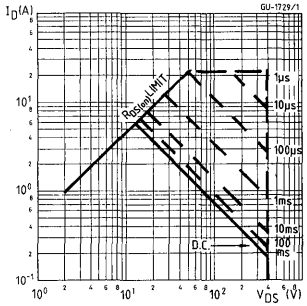
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

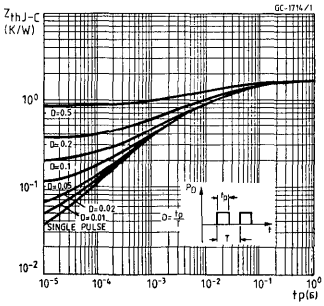
SOURCE DRAIN DIODE

I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				5.5 22	A A
V_{SD}	Forward on voltage	I_{SD} = 11 A	V_{GS} = 0			1.6	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 5.5 A	di/dt = 100A/μs		1000 5		ns μC

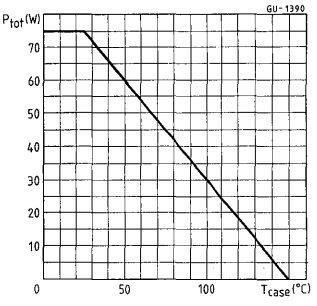
Safe operating areas



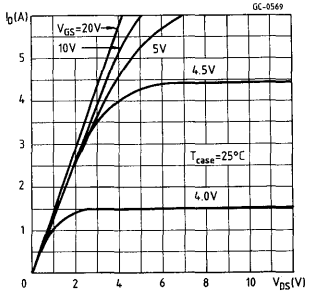
Thermal impedance



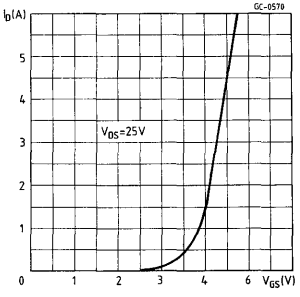
Derating curve



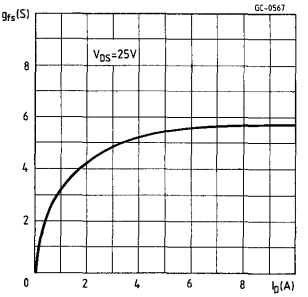
Output characteristics



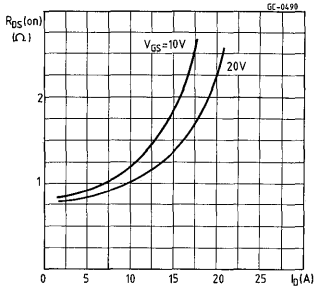
Transfer characteristics



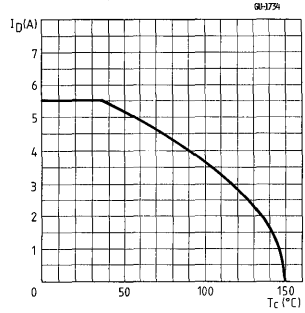
Transconductance



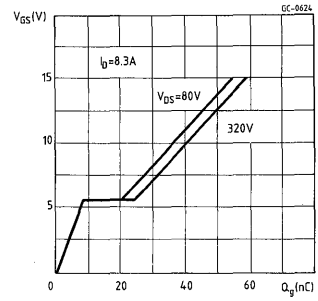
Static drain-source on resistance



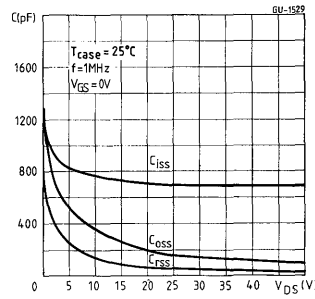
Maximum drain current vs temperature



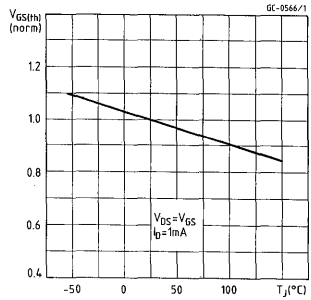
Gate charge vs gate-source voltage



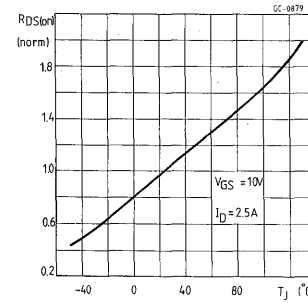
Capacitance variation



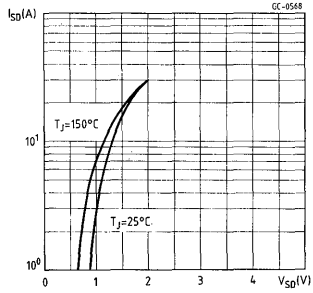
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ60B

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

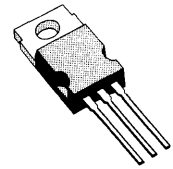
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ60B	400 V	1.5 Ω	4.5 A

- HIGH VOLTAGE - FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

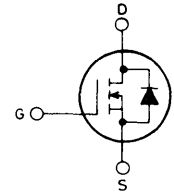
- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	400	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 25°C$	4.5	A
I_{DM}	Drain current (pulsed)	18	A
P_{tot}	Total dissipation at $T_c < 25°C$	75	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

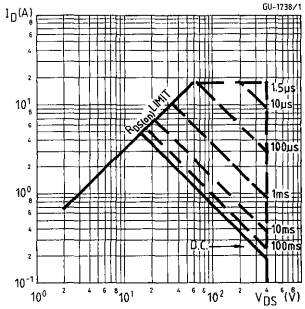
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2.5 A			1.5	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2.5 A	1.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			2000 180 60	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.5 A V_{GS} = 10 V			45 60 140 65	ns ns ns ns

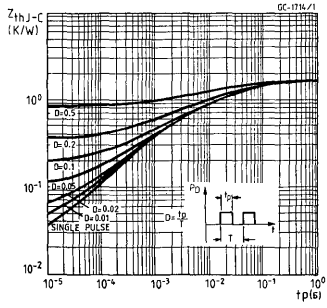
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				4.5 18	A A
V_{SD}	Forward on voltage	I_{SD} = 9 A	V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time				1000		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 4.5 A	di/dt = 100A/μs		5		μC

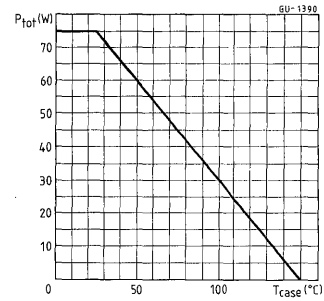
Safe operating areas



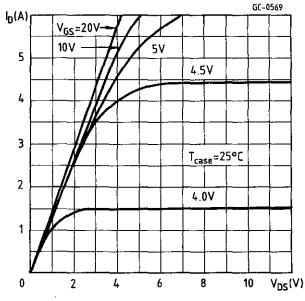
Thermal impedance



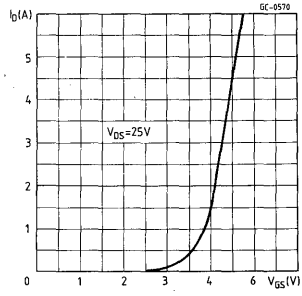
Derating curve



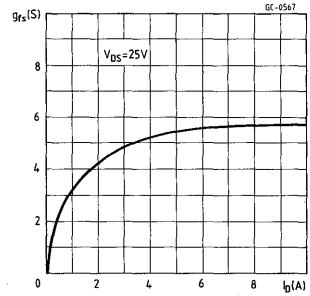
Output characteristics



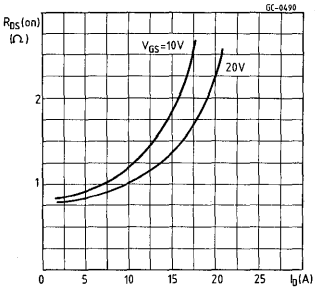
Transfer characteristics



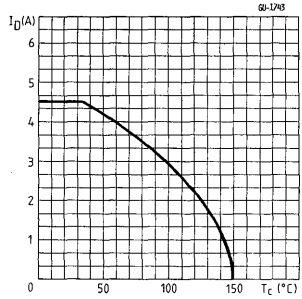
Transconductance



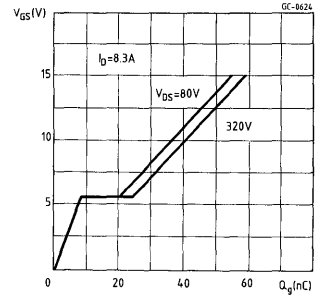
Static drain-source on resistance



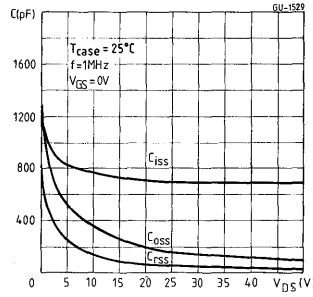
Maximum drain current vs temperature



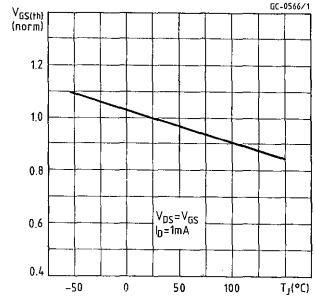
Gate charge vs gate-source voltage



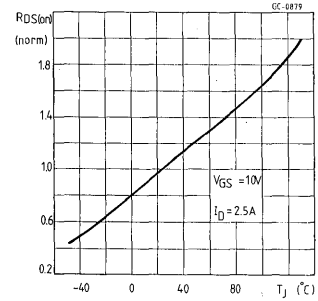
Capacitance variation



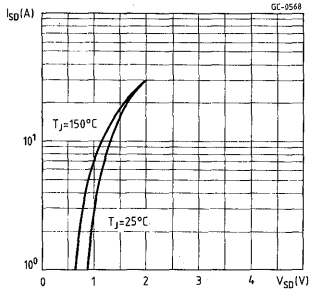
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ71
BUZ71FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

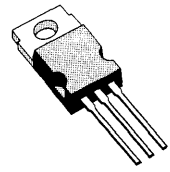
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
BUZ71	50 V	0.1 Ω	14 A
BUZ71FI	50 V	0.1 Ω	12 A

- VERY FAST SWITCHING
- LOW DRIVE ENERGY FOR EASY DRIVE, REDUCED SIZE AND COST
- HIGH PULSED CURRENT - 56A FOR POWER APPLICATIONS

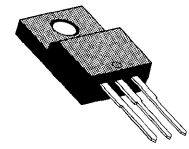
INDUSTRIAL APPLICATIONS:

- POWER ACTUATORS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators and many other uses in automotive control applications. They also find use in DC/DC converters and uninterruptible power supplies.

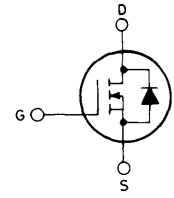


TO-220



ISOWATT 220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50		V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50		V
V_{GS}	Gate-source voltage	±20		V
I_{DM}	Drain current (pulsed) $T_c=25°C$	56		A
		BUZ71	**BUZ71FI**	
I_D ■	Drain current (continuous) $T_c=30°C$	14	12	A
P_{tot} ■	Total dissipation at $T_c<25°C$	40	30	W
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C
	DIN humidity category (DIN 40040)	E		
	IEC climatic category (DIN IEC 68-1)	55/150/56		

■ See note on ISOWATT 220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.1	4.16	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75		°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

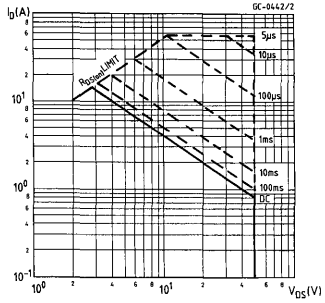
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 9 A			0.1	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 9 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			650 450 280	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			30 85 90 110	ns ns ns ns

■ See note on ISOWATT 220 in this datasheet

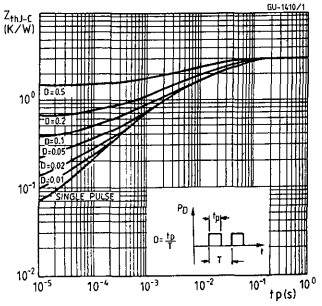
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					14 56	A A
V_{SD}	Forward on voltage	I_{SD} = 28 A	V_{GS} = 0			1.8	V
t_{rr}	Reverse recovery time				120		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 14 A	di/dt = 100A/μs		0.15		μC

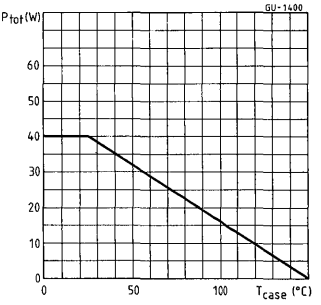
Safe operating areas



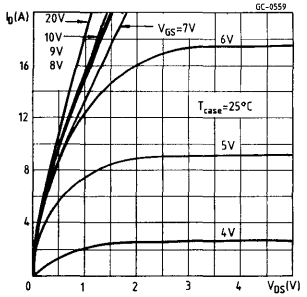
Thermal impedance



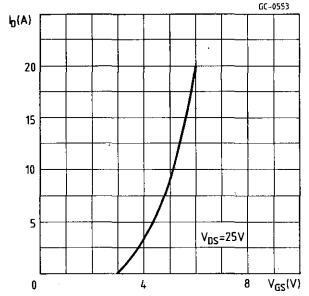
Derating curve



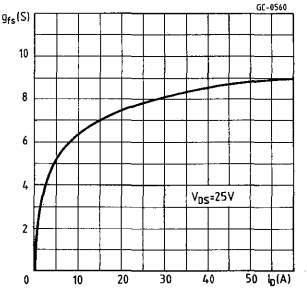
Output characteristics



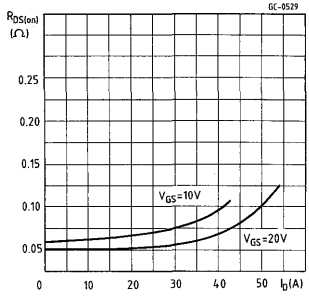
Transfer characteristics



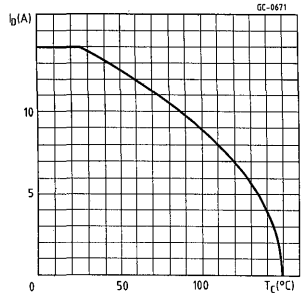
Transconductance



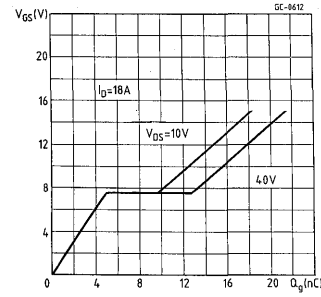
Static drain-source on resistance



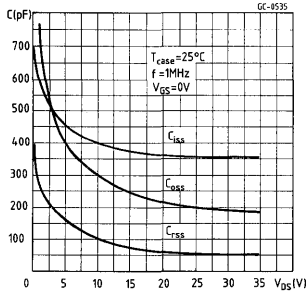
Maximum drain current vs temperature



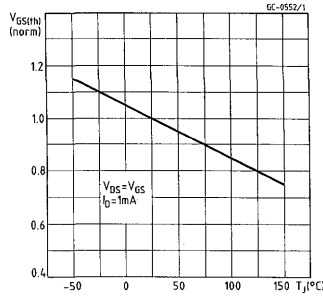
Gate charge vs gate-source voltage



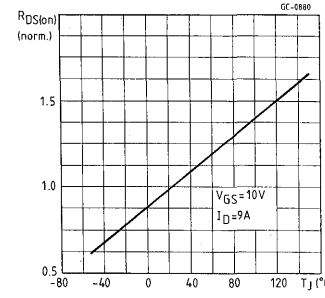
Capacitance variation



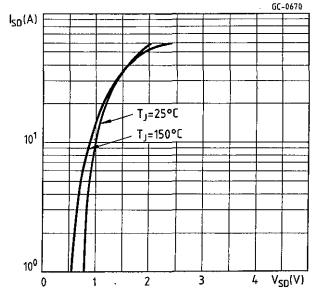
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

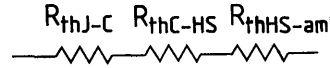
$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

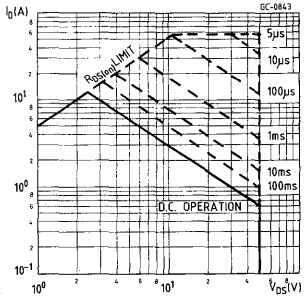
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

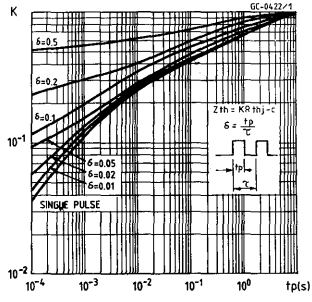


ISOWATT DATA

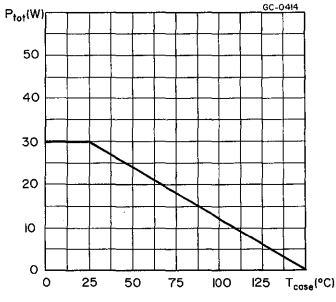
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

BUZ71A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

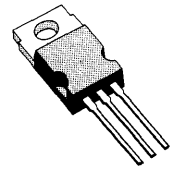
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ71A	50 V	0.12 Ω	13 A

- ULTRA FAST SWITCHING
- LOW DRIVE ENERGY FOR EASY DRIVE
- COST EFFECTIVE

INDUSTRIAL APPLICATIONS:

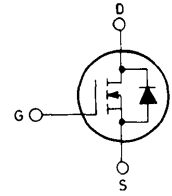
- AUTOMOTIVE POWER ACTUATORS
- MOTORS CONTROL
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive and automotive and automatic guided vehicle applications. It also finds use in DC/DC converters and uninteruptable power supplies.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=25°C$	13	A
I_{DM}	Drain current (pulsed)	52	A
P_{tot}	Total dissipation at $T_c<25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

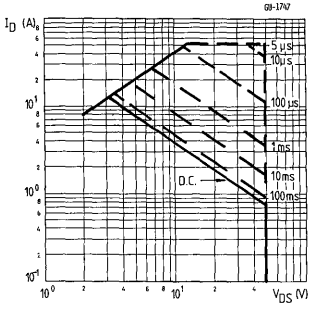
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			-	±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 9 A			0.12	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 9 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			650 450 280	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 3 A V_{GS} = 10 V			30 85 90 110	ns ns ns ns

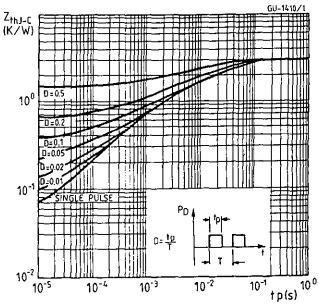
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD}	Source-drain current	T_c = 25°C				13	A
I_{SDM}	Source-drain current (pulsed)					52	A
V_{SD}	Forward on voltage	I_{SD} = 26 A	V_{GS} = 0			2.2	V
t_{rr}	Reverse recovery time				120		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 13 A	di/dt = 100A/μs		0.15		μC

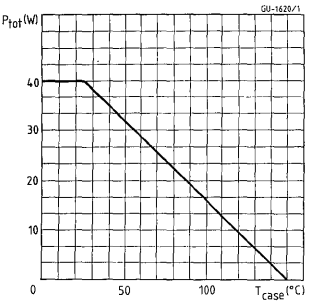
Safe operating areas



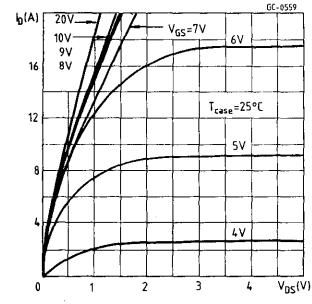
Thermal impedance



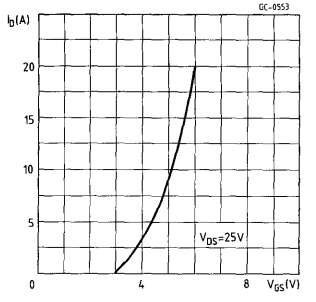
Derating curve



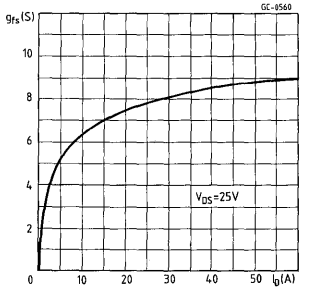
Output characteristics



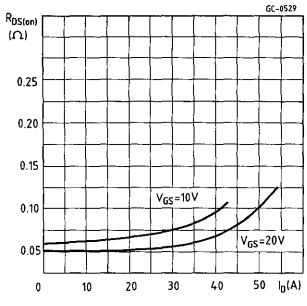
Transfer characteristics



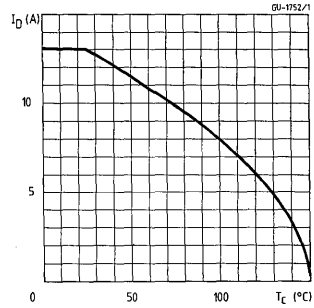
Transconductance



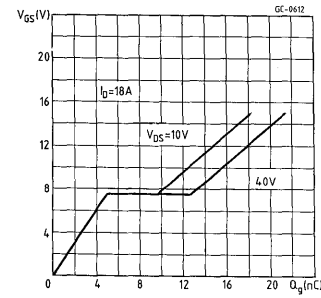
Static drain-source on resistance



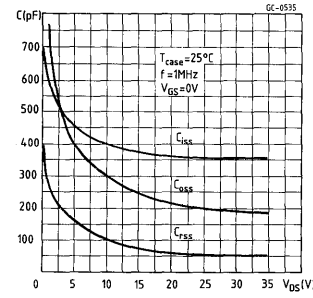
Maximum drain current vs temperature



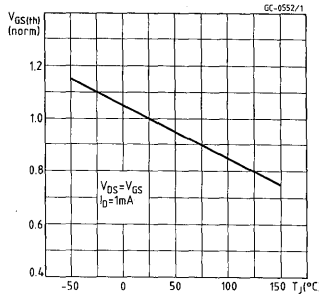
Gate charge vs gate-source voltage



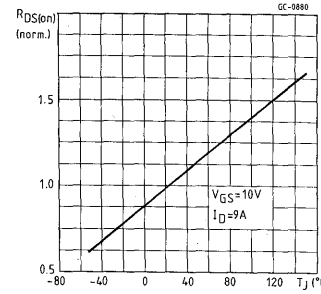
Capacitance variation



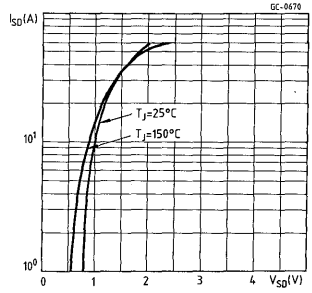
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ72A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

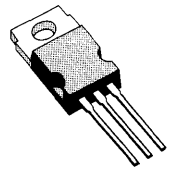
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ72A	100 V	0.25 Ω	9 A

- 100 VOLTS - FOR UPS APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ♦
- EASY DRIVE - FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

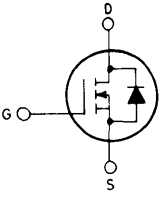
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching application.
Typical applications include UPS, battery changers, printer hammer drivers, solenoid drivers and motor control.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=25°C$	9	A
I_{DM}	Drain current (pulsed)	36	A
P_{tot}	Total dissipation at $T_c<25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

♦ Introduced in 1989 week 1

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 5 A			0.25	Ω
ENERGY TEST							
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V starting T_j = 25°C	L = 100 μH	9			A
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 5 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			600 240 130	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.9 A V_{GS} = 10 V			30 70 90 70	ns ns ns ns

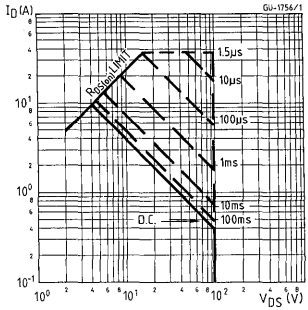
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

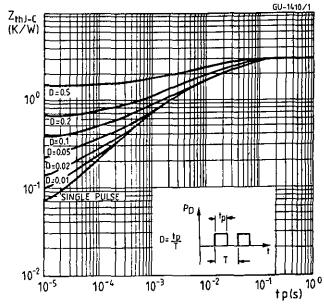
SOURCE DRAIN DIODE

I_{SD}	Source-drain current	T_c = 25°C				9	A
I_{SDM}	Source-drain current (pulsed)					36	A
V_{SD}	Forward on voltage	I_{SD} = 18 A	V_{GS} = 0			2	V
t_{rr}	Reverse recovery time				170		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 9 A	di/dt = 100A/μs		0.30		μC

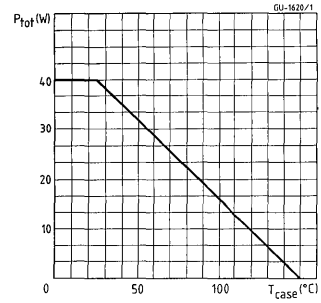
Safe operating areas



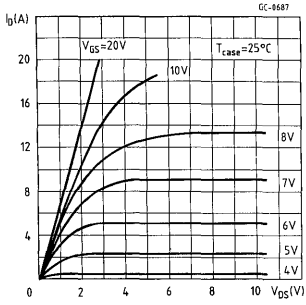
Thermal impedance



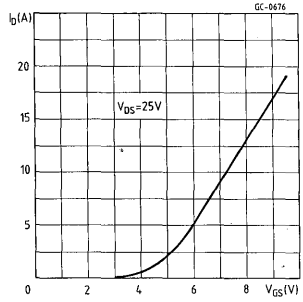
Derating curve



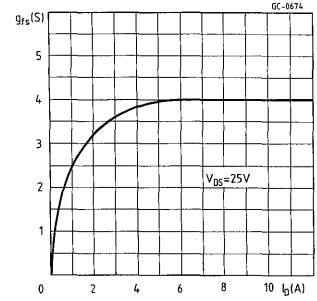
Output characteristics



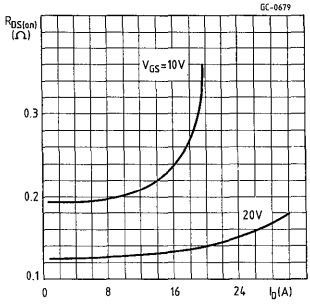
Transfer characteristics



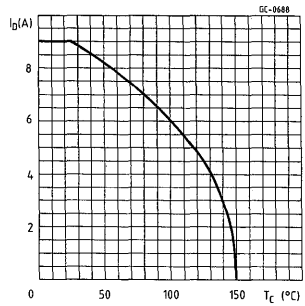
Transconductance



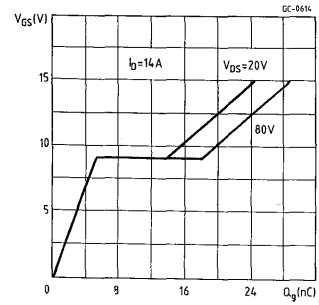
Static drain-source on resistance



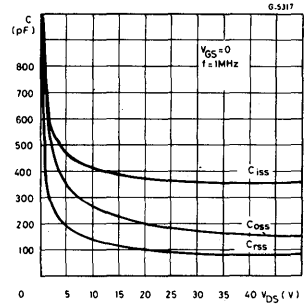
Maximum drain current vs temperature



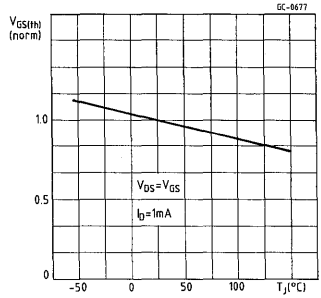
Gate charge vs gate-source voltage



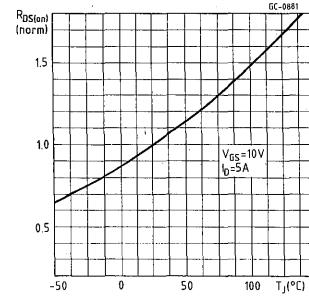
Capacitance variation



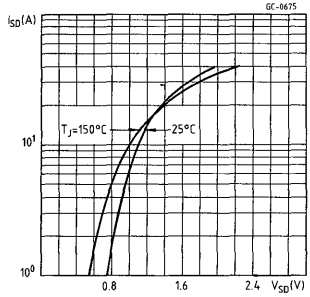
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ74

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

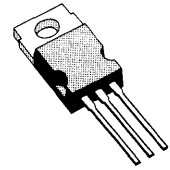
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ74	500 V	3.0 Ω	2.4 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 500V FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT > 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCH MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching power supplies, uninterruptible power supplies and motor speed control.



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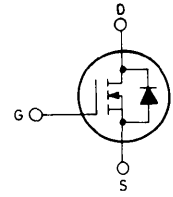
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 30°C$	2.4	A
I_{DM}	Drain current (pulsed)	9.6	A
P_{tot}	Total dissipation at $T_c < 25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

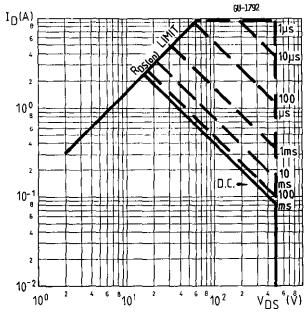
ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$	$V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} =$ Max Rating $V_{DS} =$ Max Rating	 $T_j = 125°C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V				± 100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 1$ mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 10$ V	$I_D = 1.2$ A			3.0	Ω
DYNAMIC							
g_{fs}	Forward transconductance	$V_{DS} = 25$ V	$I_D = 1.2$ A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V $V_{GS} = 0$	f = 1 MHz			500 80 55	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 30$ V $R_{GS} = 50\ \Omega$	$I_D = 2.3$ A $V_{GS} = 10$ V			20 60 65 40	ns ns ns ns

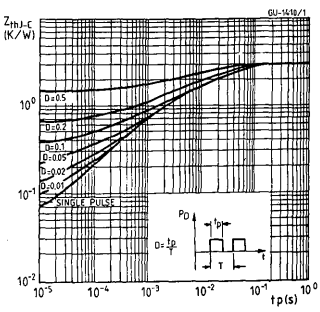
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				2.4 9.5	A A
V_{SD}	Forward on voltage	I_{SD} = 4.8 A	V_{GS} = 0			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 2.4 A	di/dt = 100A/μs		350		ns
Q_{rr}	Reverse recovered charge				3.5		μC

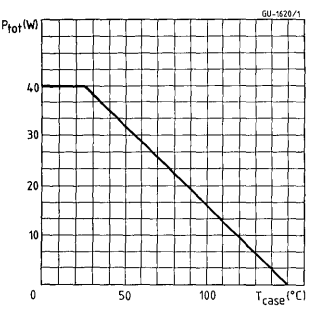
Safe operating areas



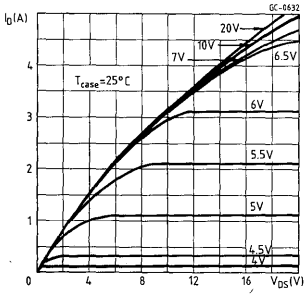
Thermal impedance



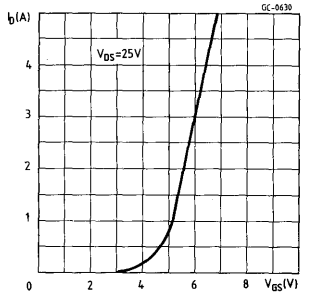
Derating curve



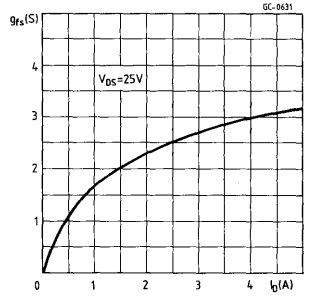
Output characteristics



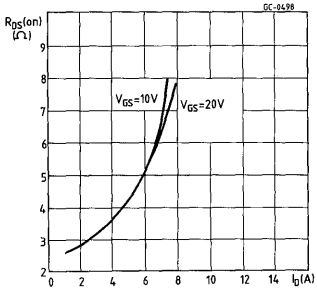
Transfer characteristics



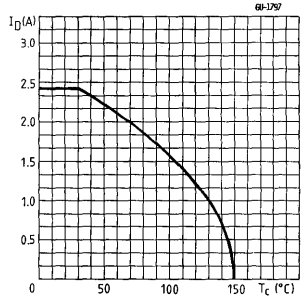
Transconductance



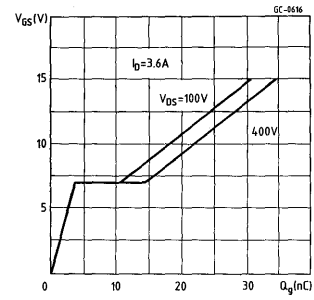
Static drain-source on resistance



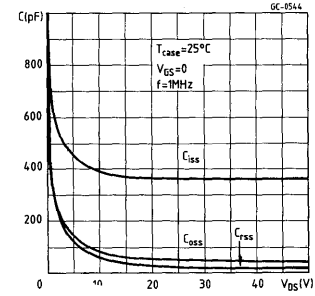
Maximum drain current vs temperature



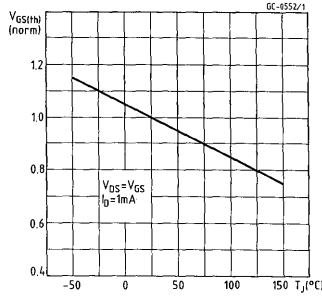
Gate charge vs gate-source voltage



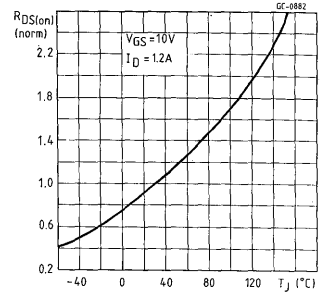
Capacitance variation



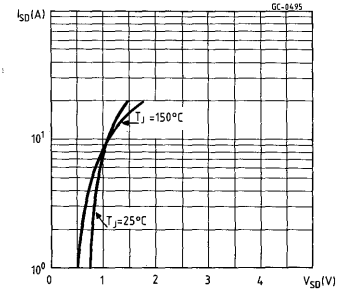
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ74A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

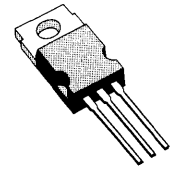
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ74A	500 V	4 Ω	2 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT > 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCH MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching power supplies, uninterruptible power supplies and motor speed control.



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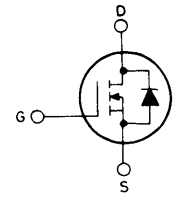
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c = 40°C$	2	A
I_{DM}	Drain current (pulsed)	8	A
P_{tot}	Total dissipation at $T_c < 25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	75	°C/W

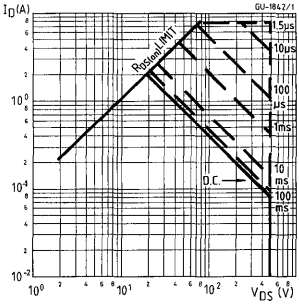
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 1.2 A			4.0	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 1.2 A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			500 80 55	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.1 A V_{GS} = 10 V			20 60 65 40	ns ns ns ns

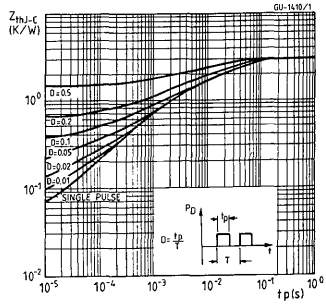
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)	T_c = 25°C			2 8	A A
V_{SD} Forward on voltage	I_{SD} = 4 A V_{GS} = 0			1.3	V
t_{rr} Reverse recovery time			350		ns
Q_{rr} Reverse recovered charge	I_{SD} = 2 A di/dt = 100A/μs		3.5		μC

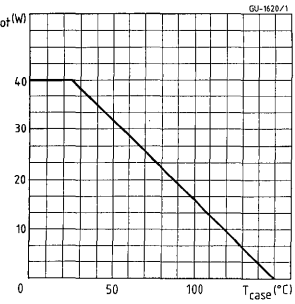
Safe operating areas



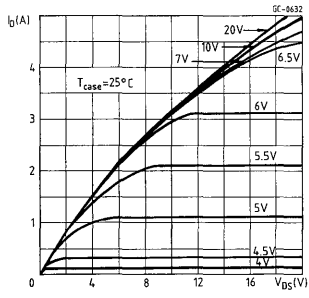
Thermal impedance



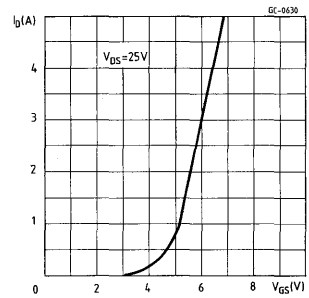
Derating curve



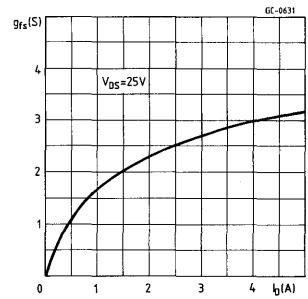
Output characteristics



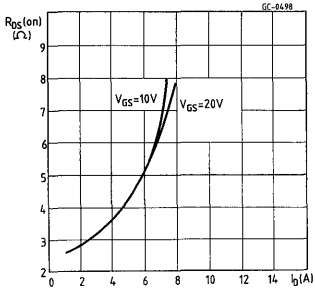
Transfer characteristics



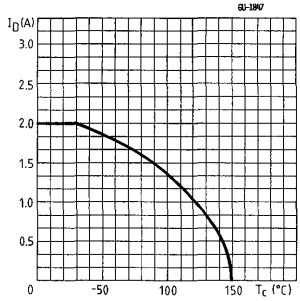
Transconductance



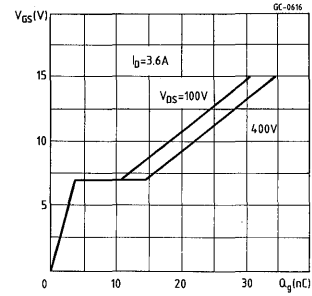
Static drain-source on resistance



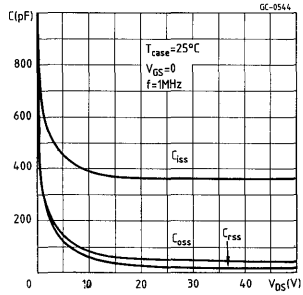
Maximum drain current vs temperature



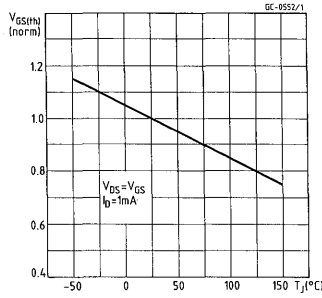
Gate charge vs gate-source voltage



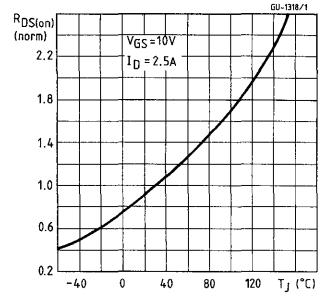
Capacitance variation



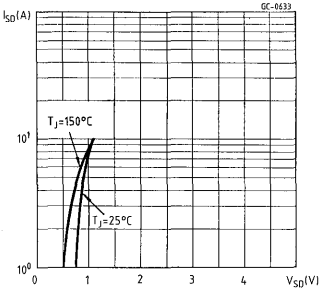
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ76

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

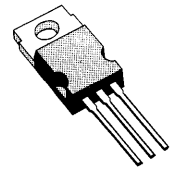
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ76	400 V	1.8 Ω	3 A

- HIGH VOLTAGE - FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

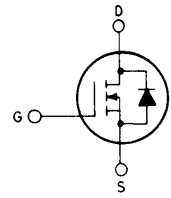
- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Applications include off-line use, constant current source, ultrasonic equipment and switching power supply start-up circuits.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=35°C$	3	A
I_{DM}	Drain current (pulsed)	12	A
P_{tot}	Total dissipation at $T_c<25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{ - amb}}$	Thermal resistance junction-ambient	max	75	°C/W

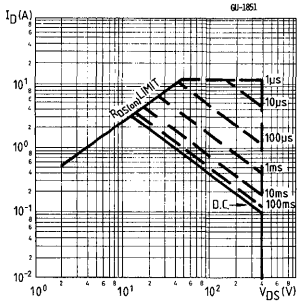
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 1.5 A			1.8	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 1.5 A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			500 80 60	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.5 A V_{GS} = 10 V			20 60 65 40	ns ns ns ns

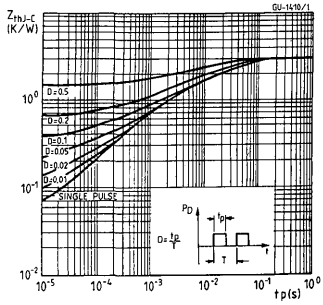
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				3 12	A A
V_{SD}	Forward on voltage	I_{SD} = 6 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time				300		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 3 A	di/dt = 100A/μs		2.5		μC

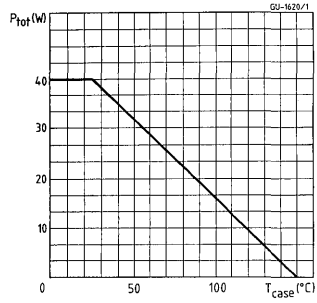
Safe operating areas



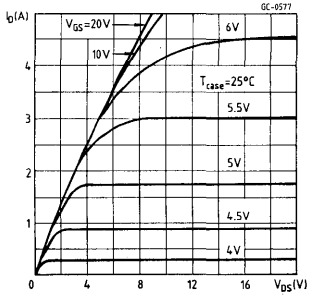
Thermal impedance



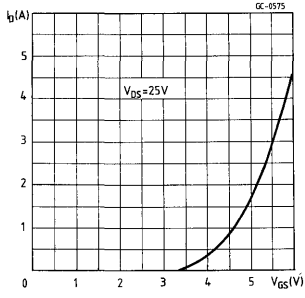
Derating curve



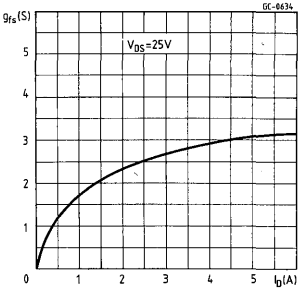
Output characteristics



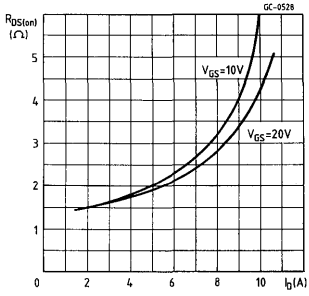
Transfer characteristics



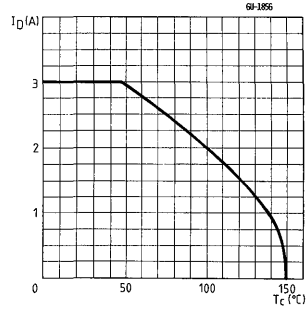
Transconductance



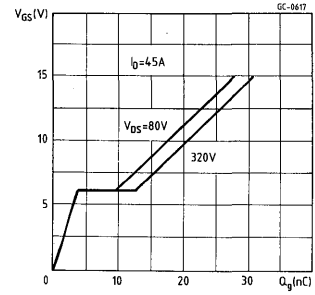
Static drain-source on resistance



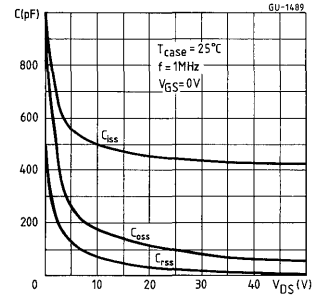
Maximum drain current vs temperature



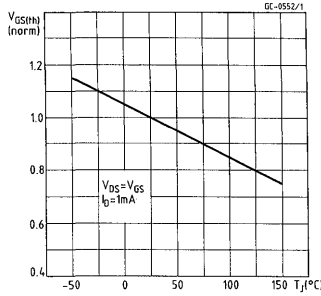
Gate charge vs gate-source voltage



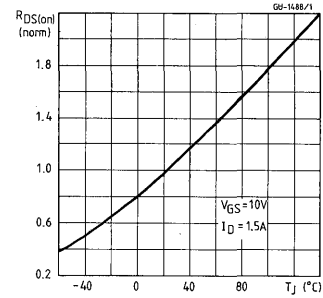
Capacitance variation



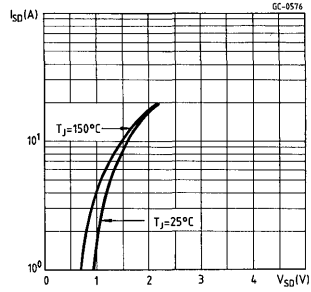
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ76A

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

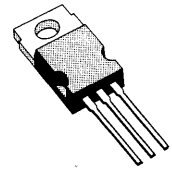
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ76A	400 V	2.5 Ω	2.6 A

- HIGH VOLTAGE - FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

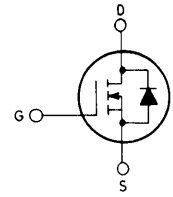
- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Applications include off-line use, constant current source, ultrasonic equipment and switching power supply start-up circuits.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) $T_c=30°C$	2.6	A
I_{DM}	Drain current (pulsed)	10	A
P_{tot}	Total dissipation at $T_c<25°C$	40	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	3.1	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	75	°C/W

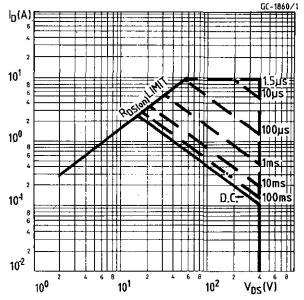
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 1.5 A			2.5	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 1.5 A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			500 80 60	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.4 A V_{GS} = 10 V			20 60 65 40	ns ns ns ns

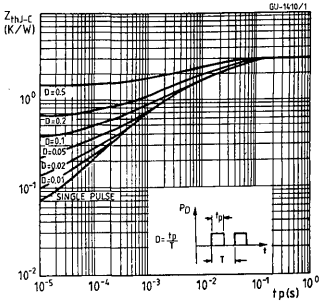
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				2.6 10	A A
V_{SD}	Forward on voltage	I_{SD} = 5.2 A	V_{GS} = 0			1.4	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 2.6 A	di/dt = 100A/μs		300 2.5		ns μC

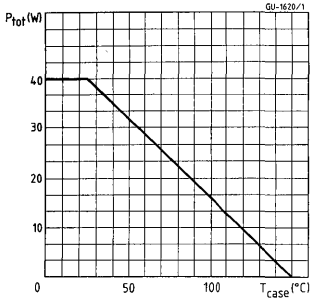
Safe operating areas



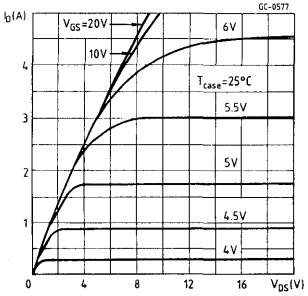
Thermal impedance



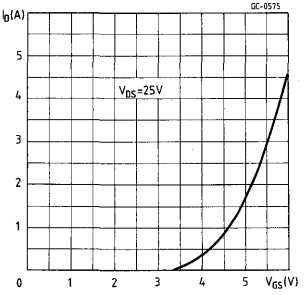
Derating curve



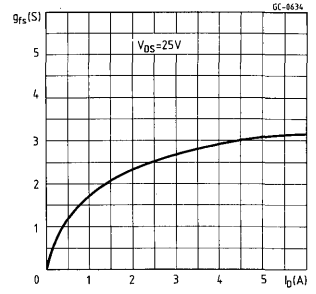
Output characteristics



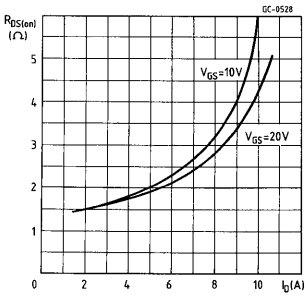
Transfer characteristics



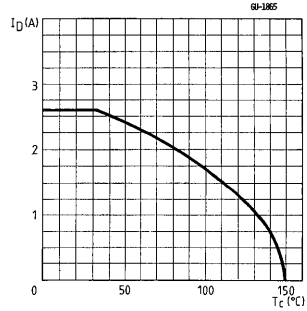
Transconductance



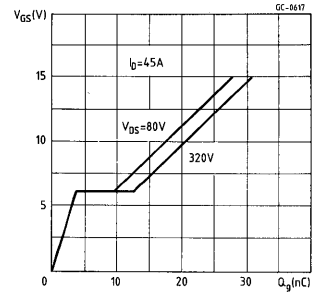
Static drain-source on resistance



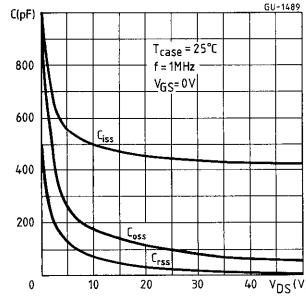
Maximum drain current vs temperature



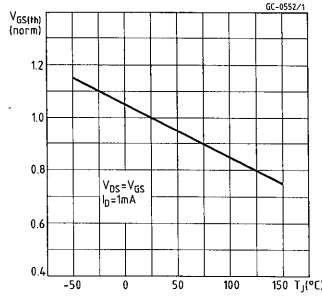
Gate charge vs gate-source voltage



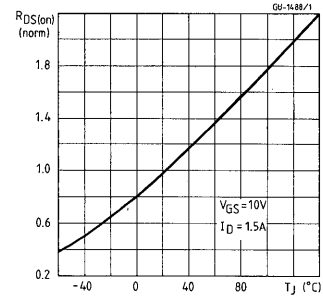
Capacitance variation



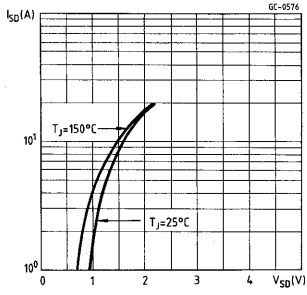
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ353

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

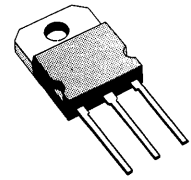
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ353	500 V	0.6 Ω	9.5 A

- HIGH SPEED SWITCHING
- HIGH VOLTAGE - 500V FOR OFF-LINE SMPS
- HIGH CURRENT - 9.5A FOR UP TO 250W SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT < 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

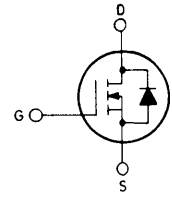
- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical applications include switching mode power supplies, uninterruptible power supplies and motor speed control.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) T_c = 25°C	9.5	A
I_{DM}	Drain current (pulsed)	38	A
P_{tot}	Total dissipation at T_c < 25°C	125	W
T_{stg}	Storage temperature	− 55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.0	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	45	°C/W

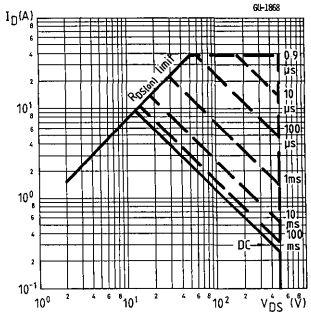
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 5.5 A			0.6	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 5.5 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			4900 400 170	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.8 A V_{GS} = 10 V			75 120 430 140	ns ns ns ns

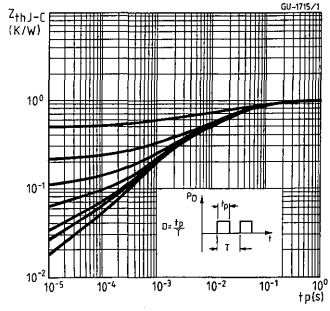
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				9.5 38	A A
V_{SD}	Forward on voltage	I_{SD} = 19 A	V_{GS} = 0			1.7	V
t_{rr}	Reverse recovery time				1200		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 9.5 A	di/dt = 100A/μs		12		μC

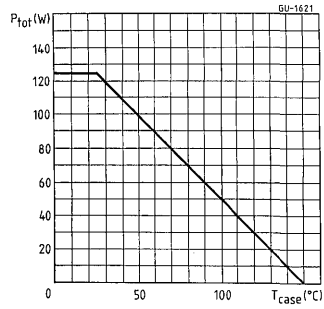
Safe operating areas



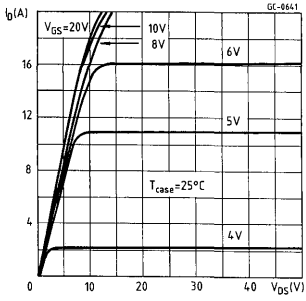
Thermal impedance



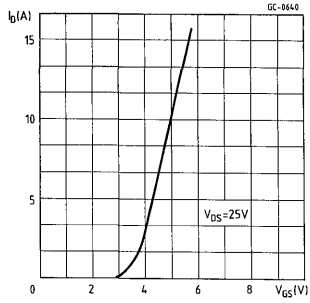
Derating curve



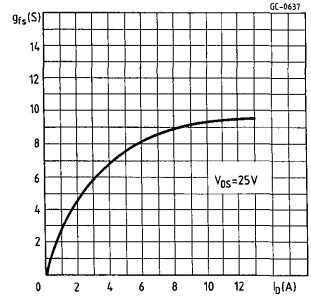
Output characteristics



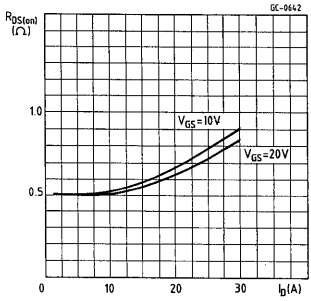
Transfer characteristics



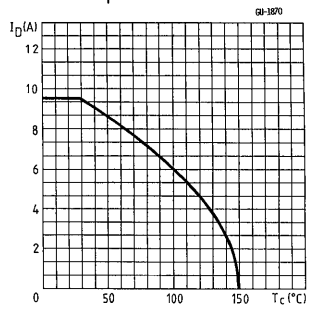
Transconductance



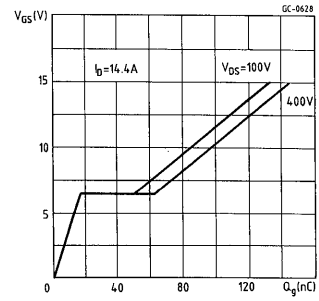
Static drain-source on resistance



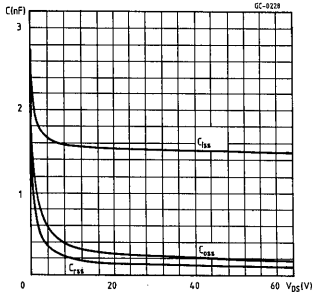
Maximum drain current vs temperature



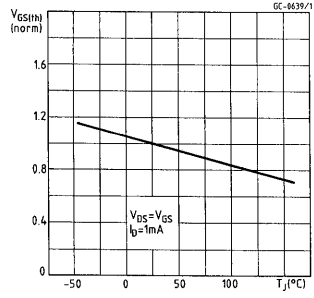
Gate charge vs gate-source voltage



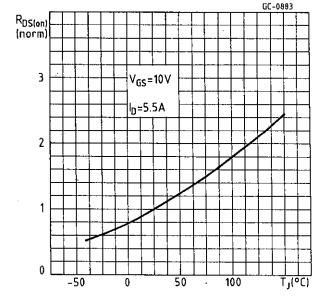
Capacitance variation



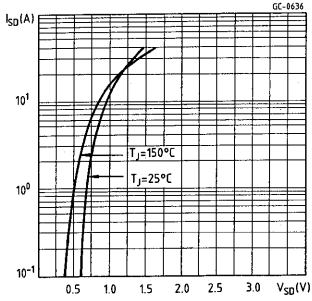
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

BUZ354

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

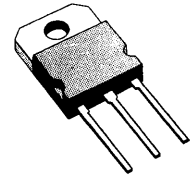
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
BUZ354	500 V	0.8 Ω	8 A

- HIGH SPEED SWITCHING
- HIGH VOLTAGE - 500V FOR OFF-LINE SMPS
- HIGH CURRENT - 8A FOR UP TO 200W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT < 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications.
Typical uses include switching mode power supplies, uninterruptible power supplies and motor speed control.



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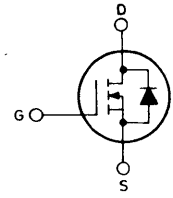
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) T_c = 25°C	8	A
I_{DM}	Drain current (pulsed)	32	A
P_{tot}	Total dissipation at T_c < 25°C	125	W
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C
	DIN humidity category (DIN 40040)	E	
	IEC climatic category (DIN IEC 68-1)	55/150/56	

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.0	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	45	°C/W

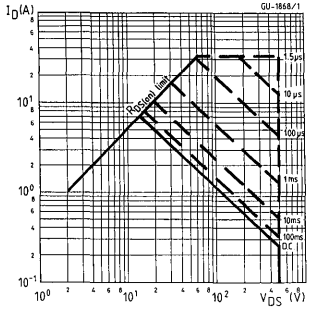
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 5.5 A			0.8	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 5.5 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			4900 400 170	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V R_{GS} = 50 Ω	I_D = 2.8 A V_{GS} = 10 V			75 120 430 140	ns ns ns ns

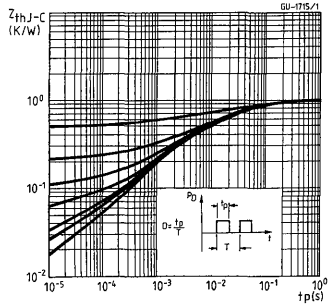
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)	T_c = 25°C				8 32	A A
V_{SD}	Forward on voltage	I_{SD} = 16 A	V_{GS} = 0			1.6	V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	I_{SD} = 8 A	di/dt = 100A/μs		1200 12		ns μC

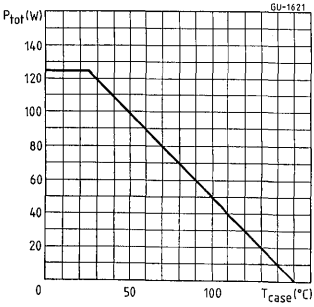
Safe operating areas



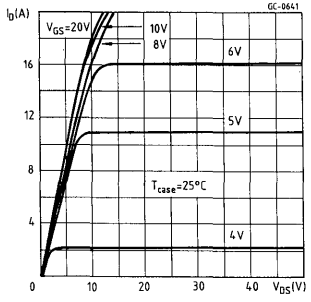
Thermal impedance



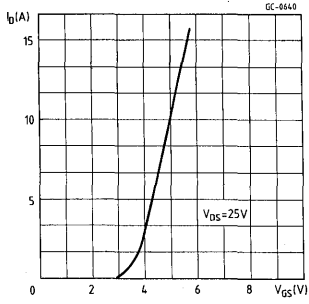
Derating curve



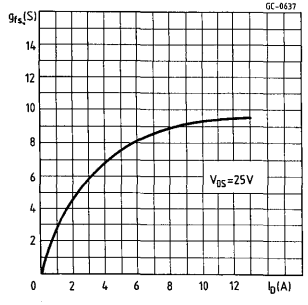
Output characteristics



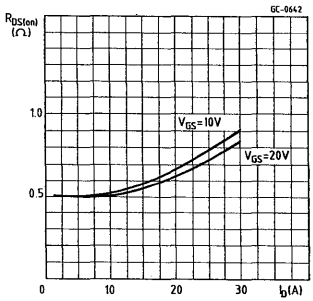
Transfer characteristics



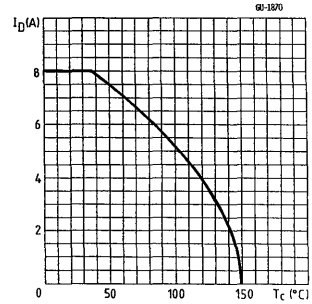
Transconductance



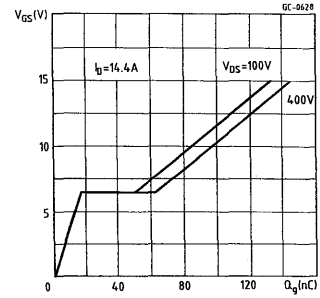
Static drain-source on resistance



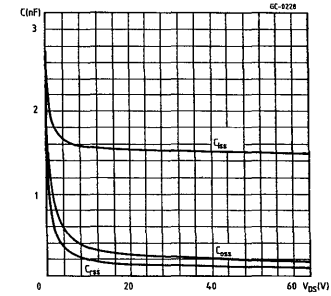
Maximum drain current vs temperature



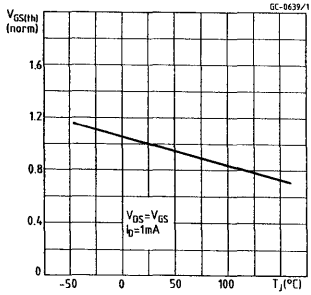
Gate charge vs gate-source voltage



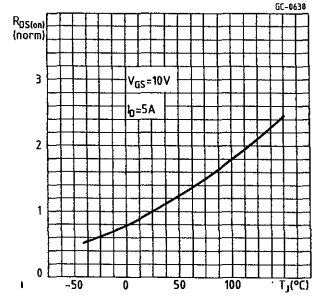
Capacitance variation



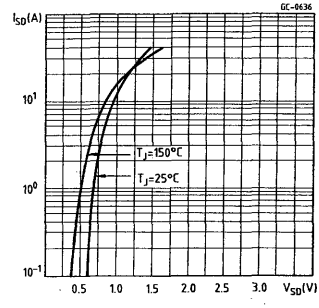
Gate threshold voltage vs temperature



Drain-source on resistance vs temperature



Source-drain diode forward characteristics



SGS-THOMSON MICROELECTRONICS

IRF 140 - 141
IRF 142 - 143

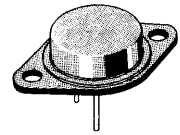
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF140	100 V	0.077 Ω	28 A
IRF141	80 V	0.077 Ω	28 A
IRF142	100 V	0.100 Ω	25 A
IRF143	80 V	0.100 Ω	25 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

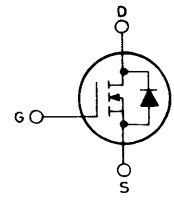
INDUSTRIAL APPLICATIONS:

- UINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS



TO-3

INTERNAL SCHEMATIC DIAGRAM



N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power audio amplifiers and robotics.

ABSOLUTE MAXIMUM RATINGS

		IRF 140	IRF 141	IRF 142	IRF 143	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	100	80	100	80	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	100	80	V
V_{GS}	Gate-source voltage		±20			V
I_D	Drain current (cont.) at $T_c=25°C$	28	28	25	25	A
I_D	Drain current (cont.) at $T_c=100°C$	20	20	17	17	A
I_{DM}(•)	Drain current (pulsed)	110	110	100	100	A
I_{DLM}	Drain inductive current, clamped (L= 100 μH)	110	110	100	100	A
P_{tot}	Total dissipation at $T_c<25°C$		125			W
	Derating factor		1			W/°C
T_{stg}	Storage temperature		−55 to 150			°C
T_j	Max. operating junction temperature		150			°C

* T_j= 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	30	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

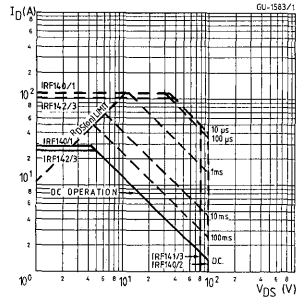
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF140/IRF142** for **IRF141/IRF143**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF140/IRF141** for **IRF142/IRF143**	 28 25			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 17 A for **IRF140/IRF141** for **IRF142/IRF143**			 0.077 0.100	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 17 A	8.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1600 800 300	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V I_D = 15 A R_i = 4.7 Ω (see test circuit)			30 60 80 30	ns ns ns ns
Q_g	Total gate charge	V_{GS} = 10 V I_D = 28 A V_{DS} = Max Rating × 0.8 (see test circuit)			59	nC

ELECTRICAL CHARACTERISTICS (Continued)

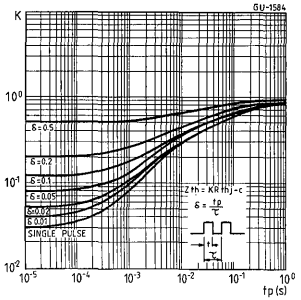
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				28 110	A A
V_{SD} ** Forward on voltage	I_{SD} = 28 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time	T_j = 150°C		500		ns
Q_{rr} Reverse recovered charge	I_{SD} = 28 A di/dt = 100 A/μs		2.9		μC

** Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%
(•) Repetitive Rating: Pulse width limited by max junction temperature

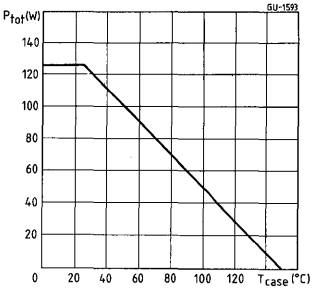
Safe operating areas



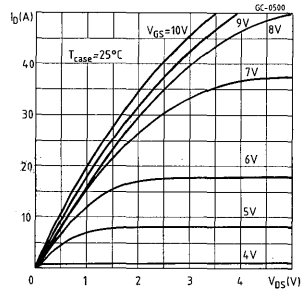
Thermal impedance



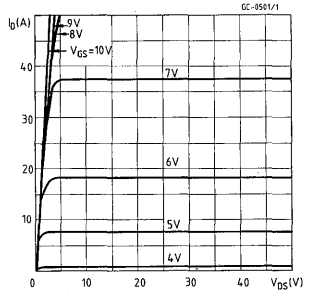
Derating curve



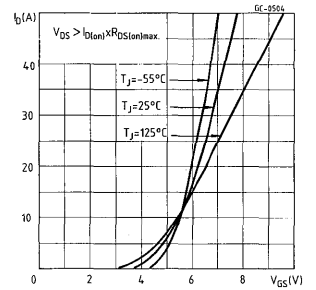
Output characteristics



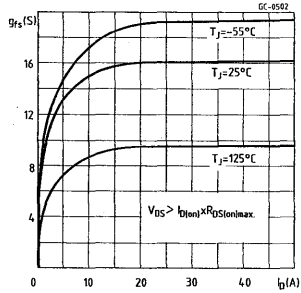
Output characteristics



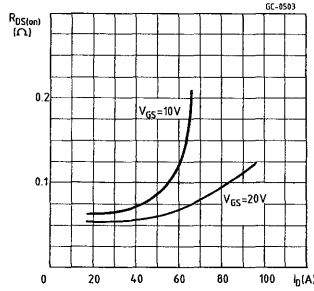
Transfer characteristics



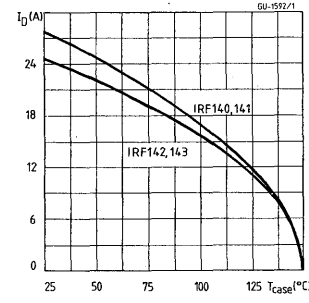
Transconductance



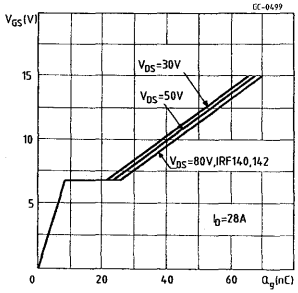
Static drain-source on resistance



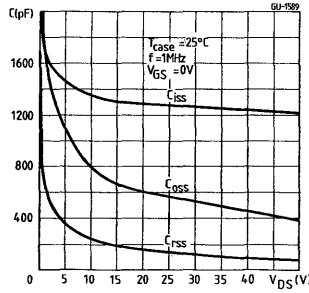
Maximum drain current vs temperature



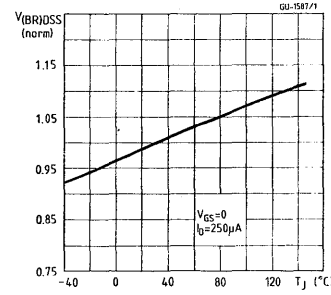
Gate charge vs gate-source voltage



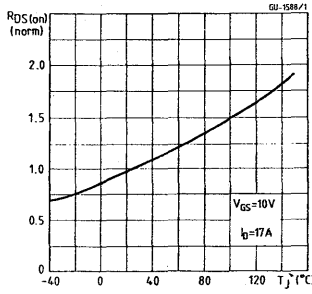
Capacitance variation



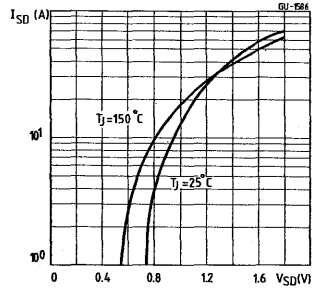
Normalized breakdown voltage vs temperature



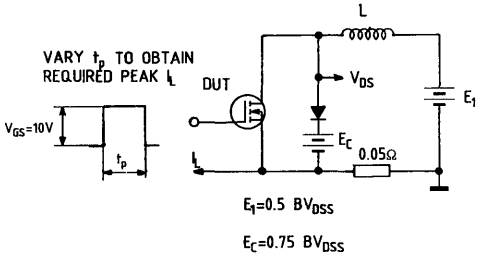
Normalized on resistance vs temperature



Source-drain diode forward characteristics



Clamped inductive test circuit



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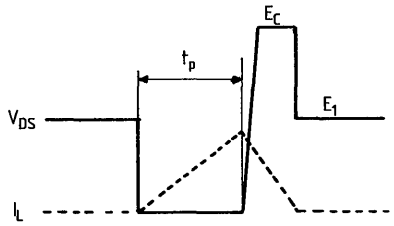
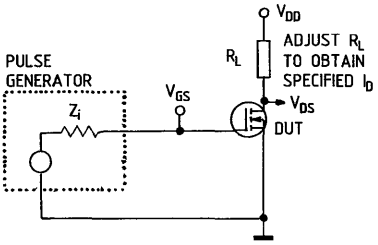
Clamped inductive waveforms



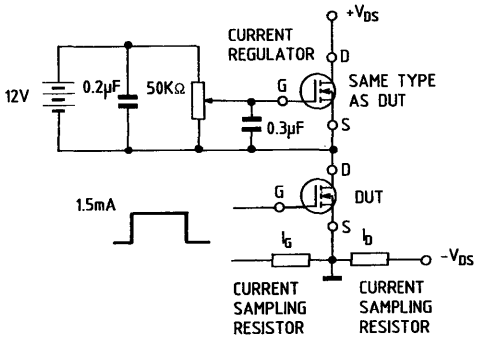
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

SGS-THOMSON MICROELECTRONICS

IRF 150 - 151
IRF 152 - 153

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

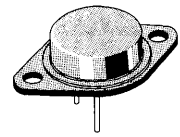
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF150	100 V	0.055 Ω	40 A
IRF151	60 V	0.055 Ω	40 A
IRF152	100 V	0.08 Ω	33 A
IRF153	60 V	0.08 Ω	33 A

- 60-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

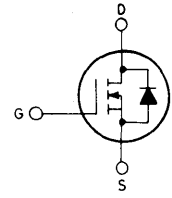
- UINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters,UPS, battery chargers, secondary regulators, servo control, power audio amplifiers and robotics.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		IRF 150	151	152	153	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	100	60	100	60	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	60	100	60	V
V_{GS}	Gate-source voltage		±20			V
I_D	Drain current (cont.) at $T_c=25°C$	40	40	33	33	A
I_D	Drain current (cont.) at $T_c=100°C$	25	25	20	20	A
I_{DM}(•)	Drain current (pulsed)	160	160	132	132	A
P_{tot}	Total dissipation at $T_c<25°C$		150			W
	Derating factor		1.2			W/°C
T_{stg}	Storage temperature		−55 to 150			°C
T_j	Max. operating junction temperature		150			°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	30	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF150/IRF152** for **IRF151/IRF153**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ x $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF150/IRF151** for **IRF152/IRF153**	 40 33			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A for **IRF150/IRF151** for **IRF152/IRF153**			0.055 0.08	Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **IRF150/IRF151** for **IRF152/IRF153**	 40 33			 A A
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ x $R_{DS\ (on)\ max}$ I_D = 20 A	9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 1500 500	pF pF pF

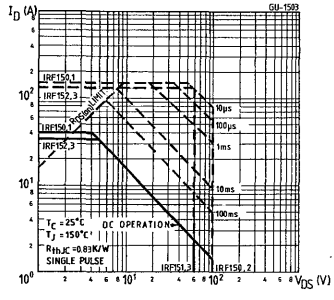
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 24 V I_D = 20 A R_i = 4.7 Ω (see test circuit)			35 100 125 100	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 50 A V_{DS} = Max Rating × 0.8 (see test circuit)			120	nC
SOURCE DRAIN DIODE						
I_{SD} I_{SDM} (•)	Source-drain current for **IRF150/IRF151** for **IRF152/IRF153** Source-drain current (pulsed) for **IRF150/IRF151** for **IRF152/IRF153**				40 33 160 132	A A A
V_{SD} **	Forward on voltage	V_{GS} = 0 for **IRF150/IRF151** I_{SD} = 40 A for **IRF152/IRF153** I_{SD} = 33 A			2.5 2.3	V V
t_{rr} Q_{rr}	Reverse recovery time Reverse recovered charge	T_j = 150°C I_{SD} = 40 A di/dt = 100 A/μs		600 3.3		ns μC

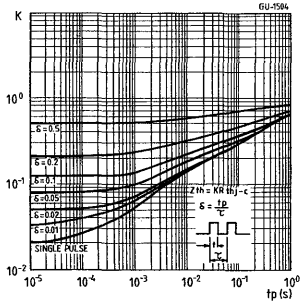
** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 2%

(•) Repetitive Rating: Pulse width limited by max junction temperature

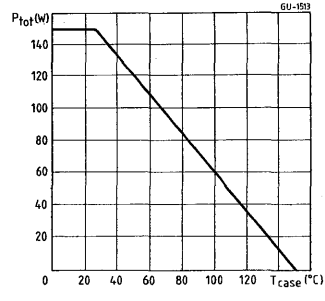
Safe operating areas



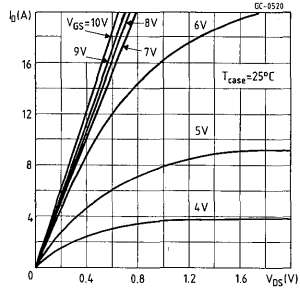
Thermal impedance



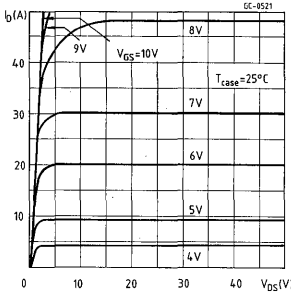
Derating curve



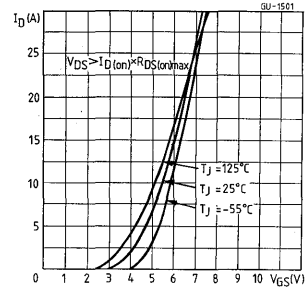
Output characteristics



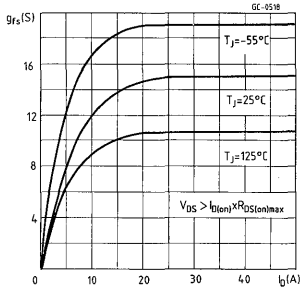
Output characteristics



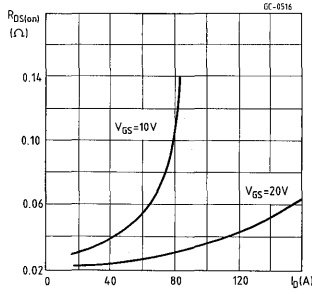
Transfer characteristics



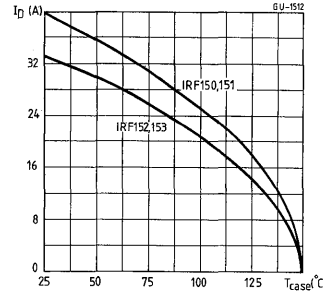
Transconductance



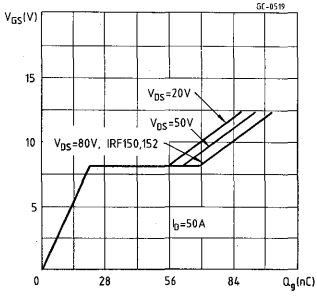
Static drain-source on resistance



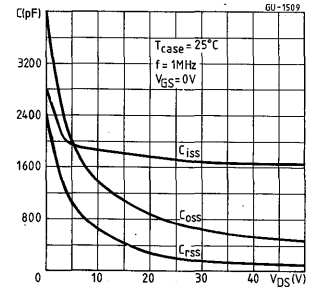
Maximum drain current vs temperature



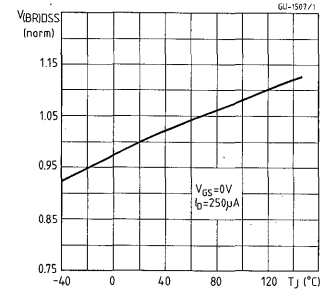
Gate charge vs gate-source voltage



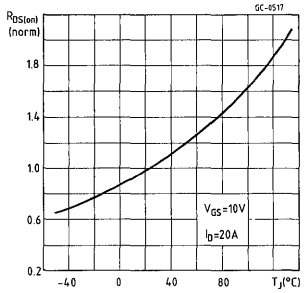
Capacitance variation



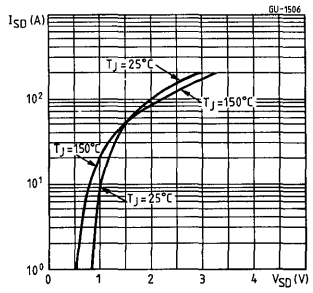
Normalized breakdown voltage vs temperature



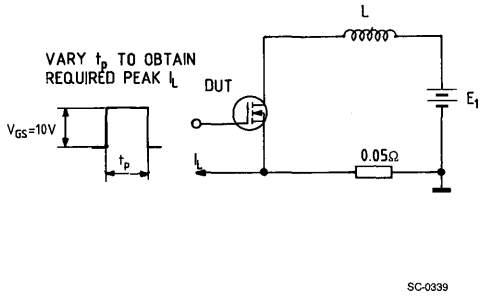
Normalized on resistance vs temperature



Source-drain diode forward characteristics



Unclamped inductive test circuit



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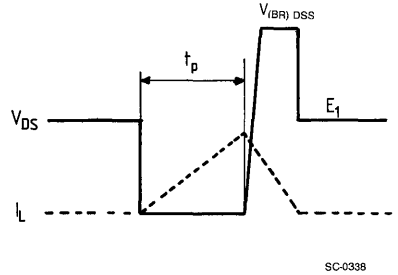
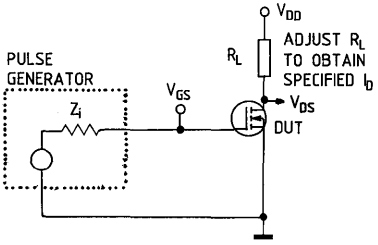
Unclamped inductive waveforms



SC-0338

Switching times test circuit



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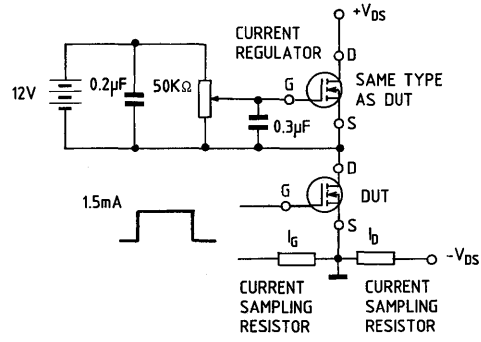
Gate charge test circuit



SC-0244

SGS-THOMSON MICROELECTRONICS

IRF350

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

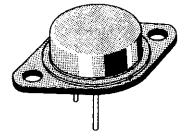
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF350	400 V	0.3 Ω	15 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR SMPS UP TO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - REDUCES SIZE AND COST

INDUSTRIAL APPLICATIONS:

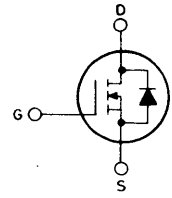
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Fast switching and easy drive make this POWER MOS transistor ideal for high voltage. Switching applications include electronic welders, switched mode power supplies and sonar equipment.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS} *	Drain-source voltage (V_{GS} = 0)	400	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at T_c = 25°C	15	A
I_D	Drain current (cont.) at T_c = 100°C	9	A
I_{DM}(•)	Drain current (pulsed)	60	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)	60	A
P_{tot}	Total dissipation at T_c < 25°C	150	W
	Derating factor	1.2	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	30	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

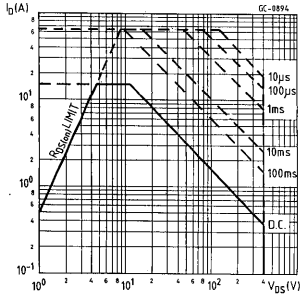
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu A$ $V_{GS} = 0$	400			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} =$ Max Rating $V_{DS} =$ Max Rating × 0.8 $T_j = 125°C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu A$	2		4	V
$I_{D\ (on)}$	On-state drain current	$V_{DS} > I_{D\ (on)} \times R_{DS\ (on)\ max}$, $V_{GS} = 10$ V	15			A
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 10$ V $I_D = 8$ A			0.3	Ω
DYNAMIC						
g_{fs} **	Forward transconductance	$V_{DS} > I_{D\ (on)} \times R_{DS\ (on)\ max}$ $I_D = 8$ A	8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V f = 1 MHz $V_{GS} = 0$			3000 600 200	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	$V_{DD} = 180$ V $I_D = 8$ A $R_i = 4.7\ \Omega$ (see test circuit)			35 65 150 75	ns ns ns ns
Q_g	Total Gate Charge	$V_{GS} = 10$ V $I_D = 18$ A $V_{DS} =$ Max Rating × 0.8 (see test circuit)			120	nC

ELECTRICAL CHARACTERISTICS (Continued)

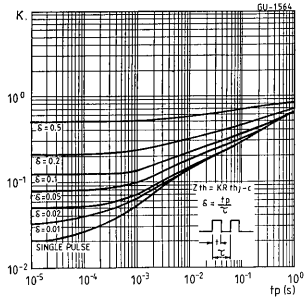
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				15 60	A A
V_{SD} ** Forward on voltage	I_{SD} = 15 A V_{GS} = 0			1.6	V
t_{rr} Reverse recovery time	T_j = 150°C		1000		ns
Q_{rr} Reverse recovered charge	I_{SD} = 15 A di/dt = 100 A/μs		6.6		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%
(•) Repetitive Rating: Pulse width limited by max junction temperature

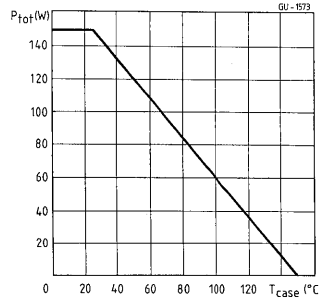
Safe operating areas



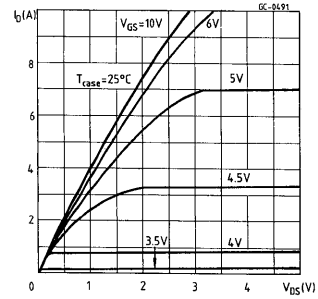
Thermal impedance



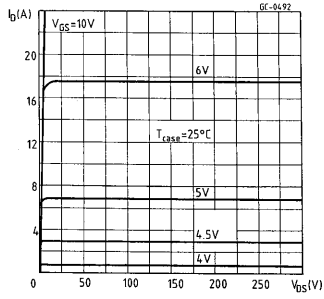
Derating curve



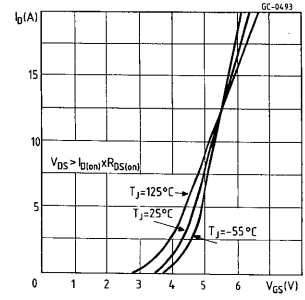
Output characteristics



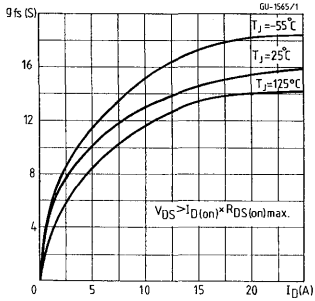
Output characteristics



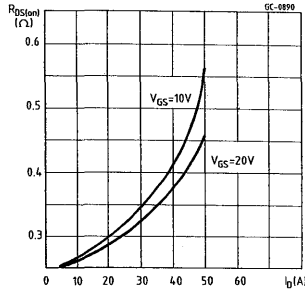
Transfer characteristics



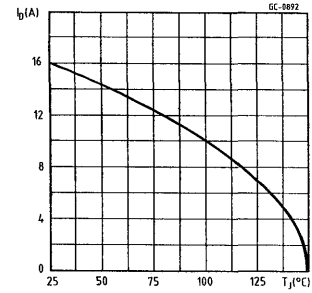
Transconductance



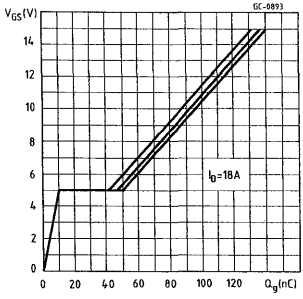
Static drain-source on resistance



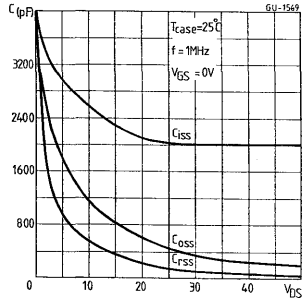
Maximum drain current vs temperature



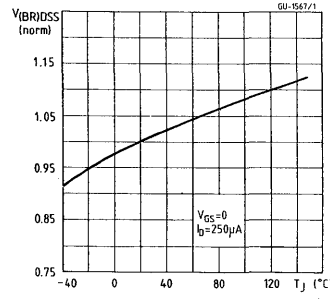
Gate charge vs gate-source voltage



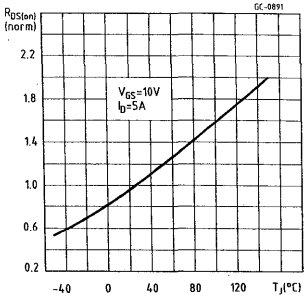
Capacitance variation



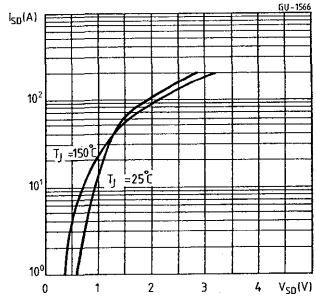
Normalized breakdown voltage vs temperature



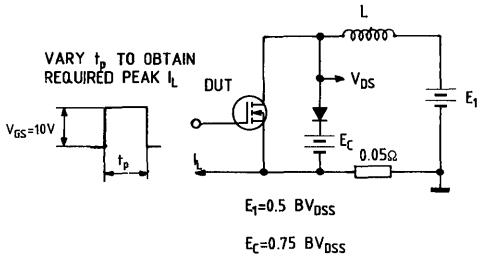
Normalized on resistance vs temperature



Source-drain diode forward characteristics

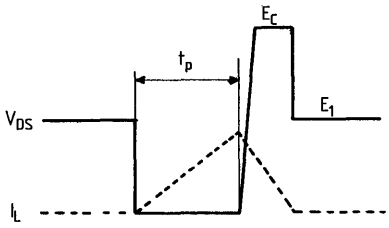


Clamped inductive test circuit



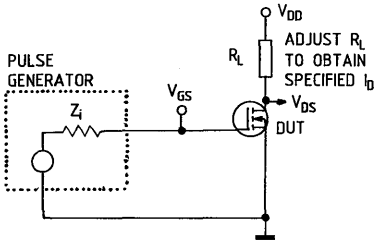
SC-0242

Clamped inductive waveforms



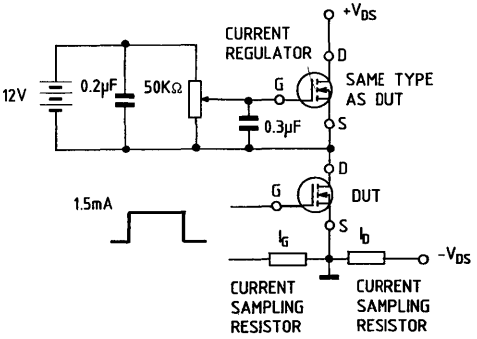
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

SGS-THOMSON MICROELECTRONICS

IRF 450 - 451
IRF 452 - 453

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

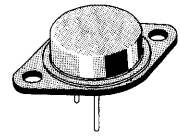
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF450	500 V	0.4 Ω	13 A
IRF451	450 V	0.4 Ω	13 A
IRF452	500 V	0.5 Ω	11 A
IRF453	450 V	0.5 Ω	11 A

- HIGH VOLTAGE - 450V FOR OFF LINE SMPS
- HIGH CURRENT - 11A FOR UP TO 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100 KHz
- EASY DRIVE - REDUCES COST AND SIZE
- HERMETIC PACKAGE TO-3

INDUSTRIAL APPLICATIONS:

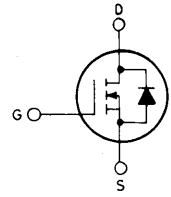
- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical applications include switched mode power supplies, uninterruptable power supplies and motor speed control.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		IRF 450	451	452	453	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	500	450	500	450	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	500	450	500	450	V
V_{GS}	Gate-source voltage		±20			V
I_D	Drain current (cont.) at $T_c=25°C$	13	13	11	11	A
I_D	Drain current (cont.) at $T_c=100°C$	8.1	8.1	7.2	7.2	A
I_{DM}(•)	Drain current (pulsed)	52	52	44	44	A
I_{DLM}	Drain inductive current, clamped (L= 100 μH)	52	52	44	44	A
P_{tot}	Total dissipation at $T_c<25°C$		150			W
	Derating factor		1.2			W/°C
T_{stg}	Storage temperature		−55 to 150			°C
T_j	Max. operating junction temperature		150			°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	30	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

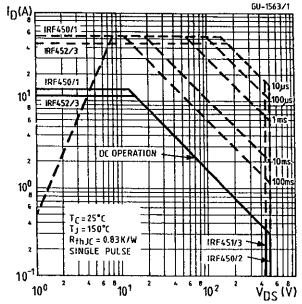
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF450/IRF452** for **IRF451/IRF453**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF450/IRF451** for **IRF452/IRF453**	 13 11			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 7.2 A for **IRF450/IRF451** for **IRF452/IRF453**			 0.4 0.5	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 7.2 A	8.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 600 200	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 210 V I_D = 7.0 A R_i = 4.7 Ω (see test circuit)			35 50 150 70	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 13 A V_{DS} = Max Rating × 0.8 (see test circuit)			120	nC

ELECTRICAL CHARACTERISTICS (Continued)

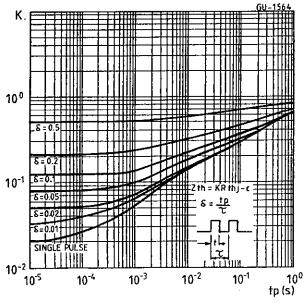
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD}	Source-drain current					13	A
I_{SDM} (•)	Source-drain current (pulsed)					52	A
V_{SD} **	Forward on voltage	I_{SD} = 13 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	T_j = 150°C			1300		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 13 A	di/dt = 100 A/μs		7.4		μC

** Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature

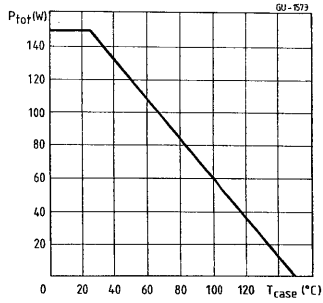
Safe operating areas



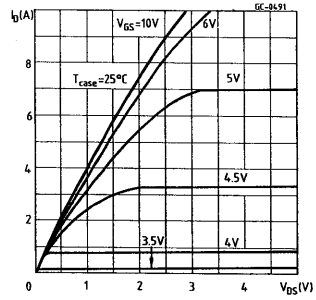
Thermal impedance



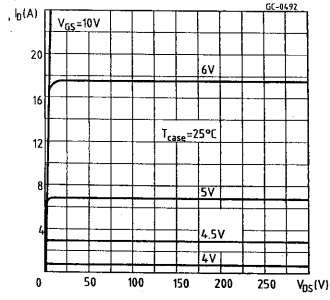
Derating curve



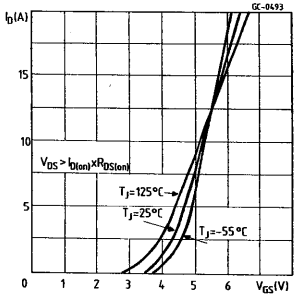
Output characteristics



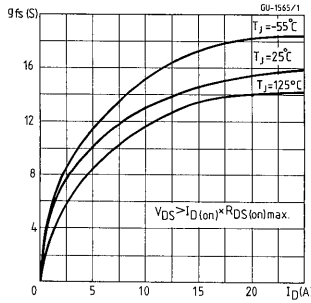
Output characteristics



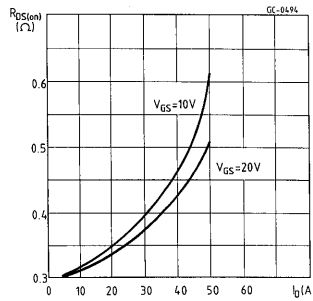
Transfer characteristics



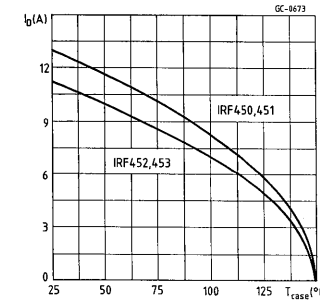
Transconductance



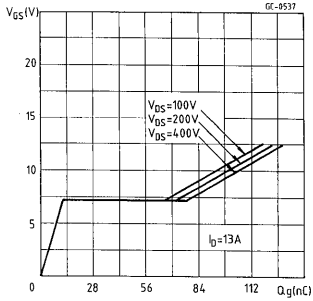
Static drain-source on resistance



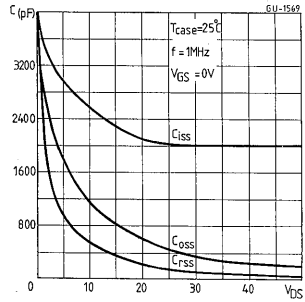
Maximum drain current vs temperature



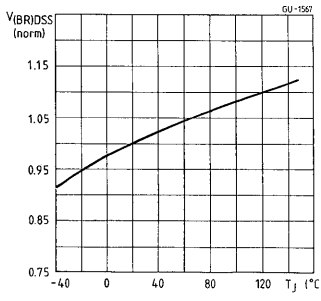
Gate charge vs gate-source voltage



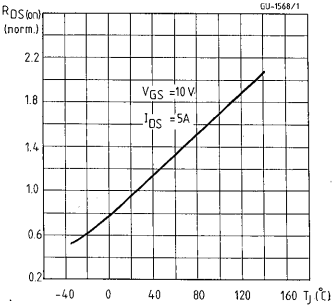
Capacitance variation



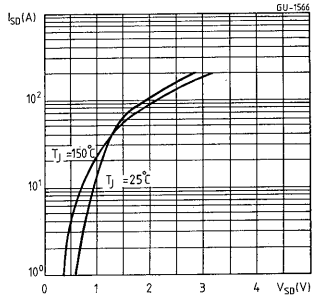
Normalized breakdown voltage vs temperature



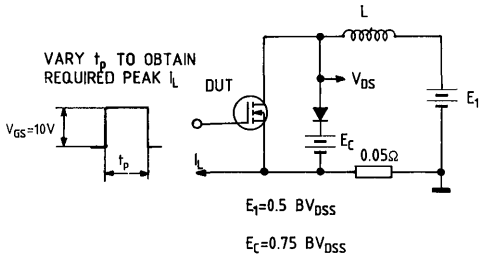
Normalized on resistance vs temperature



Source-drain diode forward characteristics

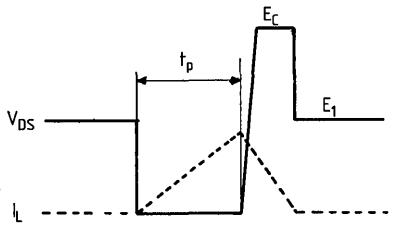


Clamped inductive test circuit



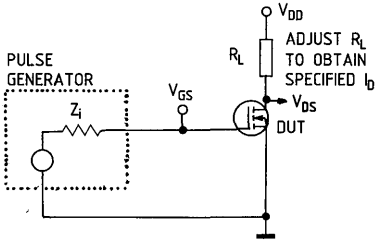
SC-0242

Clamped inductive waveforms



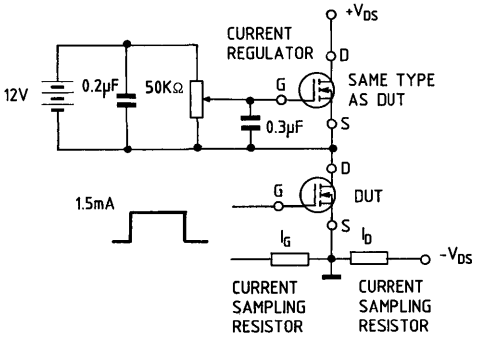
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

SGS-THOMSON MICROELECTRONICS

IRF 520/FI-521/FI
IRF 522/FI-523/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

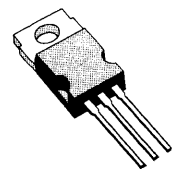
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF520	100 V	0.27 Ω	9.2 A
IRF520FI	100 V	0.27 Ω	7 A
IRF521	80 V	0.27 Ω	9.2 A
IRF521FI	80 V	0.27 Ω	7 A
IRF522	100 V	0.36 Ω	8 A
IRF522FI	100 V	0.36 Ω	6 A
IRF523	80 V	0.36 Ω	8 A
IRF523FI	80 V	0.36 Ω	6 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE- FOR REDUCED COST AND SIZE

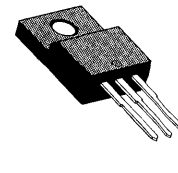
INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power-audio amplifiers and robotics.

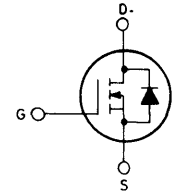


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 520 / 520FI	IRF 521 / 521FI	IRF 522 / 522FI	IRF 523 / 523FI	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)		100	80	100	80	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)		100	80	100	80	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		37	37	32	32	A
			520	**521**	**522**	**523**	
I_D	Drain current (cont.) at $T_c=$ 25°C		9.2	9.2	8	8	A
I_D	Drain current (cont.) at $T_c=$ 100°C		6.5	6.5	5.6	5.6	A
			520FI	**521FI**	**522FI**	**523FI**	
I_D ■	Drain current (cont.) at $T_c=$ 25°C		7	7	6	6	A
I_D ■	Drain current (cont.) at $T_c=$ 100°C		4	4	3.5	3.5	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c <25°C		60		30		W
■	Derating factor		0.48		0.24		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* $T_j=$ 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT220 on this datasheet.
◆ Introduced in 1988 week 44

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	2.08	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

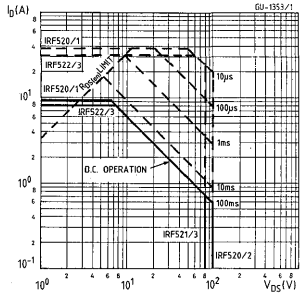
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF520/522/520FI/522FI** for **IRF521/523/521FI/523FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF520/521/520FI/521FI** for **IRF521/523/521FI/523FI**	 9.2 8			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5.6 A for **IRF520/521/520FI/521FI** for **IRF522/523/522FI/523FI**			 0.27 0.36	 Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **IRF520/521/520FI/521FI** for **IRF522/523/522FI/523FI**	 9.2 8			 A A
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 5.6 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			600 400 100	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

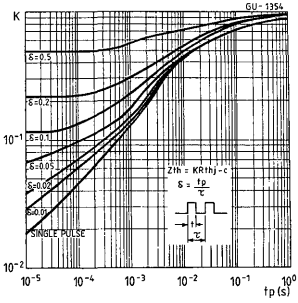
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING					
$t_{d(on)}$ Turn-on time t_r Rise time $t_{d(off)}$ Turn-off delay time t_f Fall time	V_{DD} = 40 V I_D = 4.0 A R_i = 50 Ω (see test circuit)			40 70 100 70	ns ns ns ns
Q_g Total Gate Charge	V_{GS} = 15 V I_D = 9.2 A V_{DS} = Max Rating × 0.8 (see test circuit)			15	nC
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				9.2 37	A A
V_{SD} ** Forward on voltage	I_{SD} = 9.2 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time	T_j = 150°C		280		ns
Q_{rr} Reverse recovered charge	I_{SD} = 9.2 A di/dt = 100 A/μs		1.6		μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.2%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

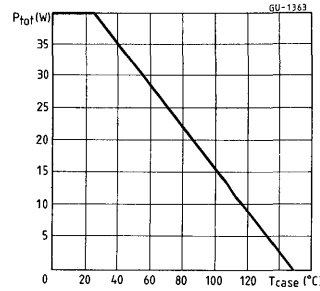
Safe operating areas (standard package)



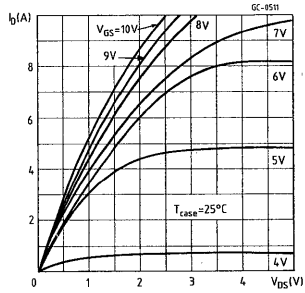
Thermal impedance (standard package)



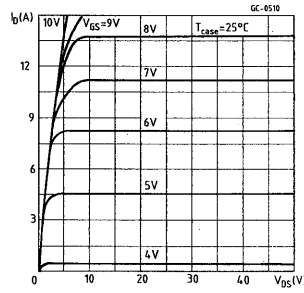
Derating curve (standard package)



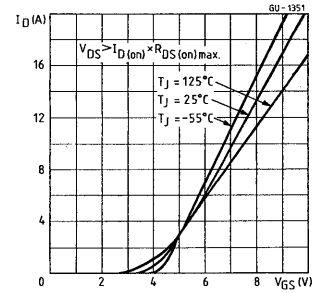
Output characteristics



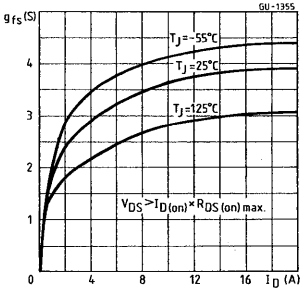
Output characteristics



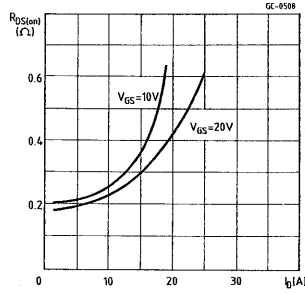
Transfer characteristics



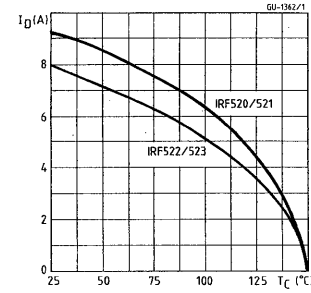
Transconductance



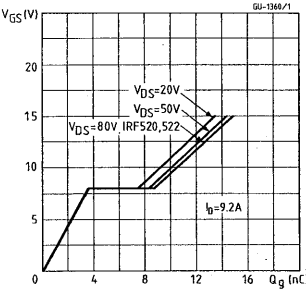
Static drain-source on resistance



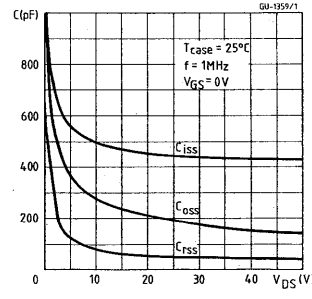
Maximum drain current vs temperature



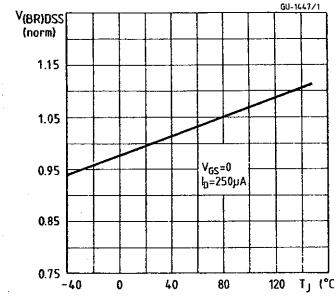
Gate charge vs gate-source voltage



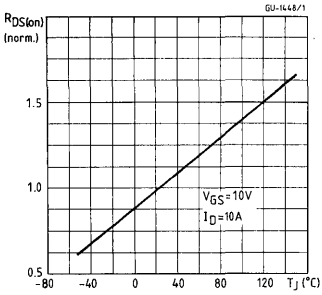
Capacitance variation



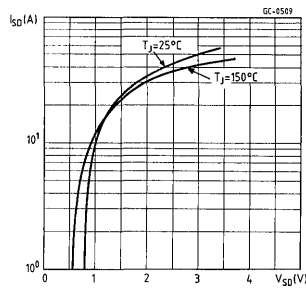
Normalized breakdown voltage vs temperature



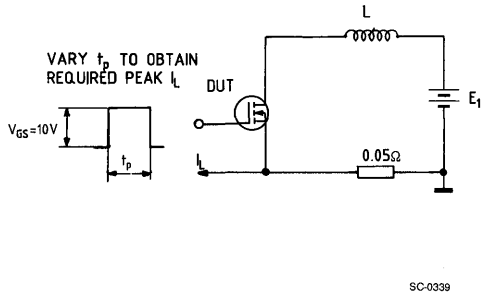
Normalized on resistance vs temperature



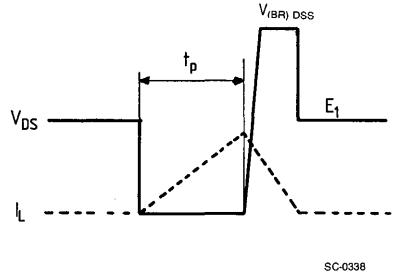
Source-drain diode forward characteristics



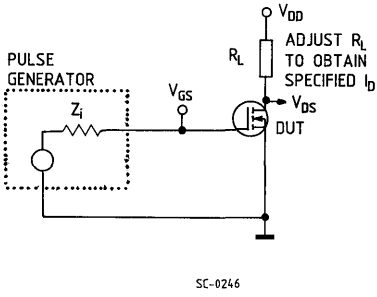
Unclamped inductive test circuit



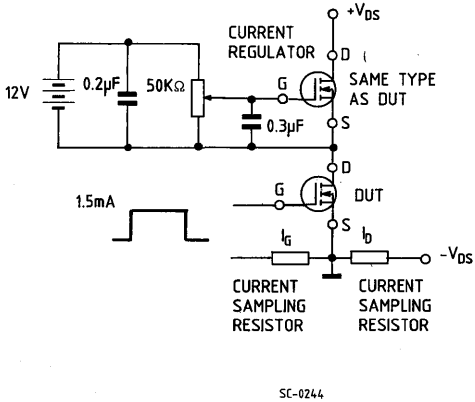
Unclamped inductive waveforms



Switching times test circuit



Gate charge test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

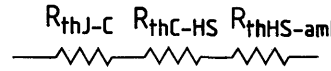
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

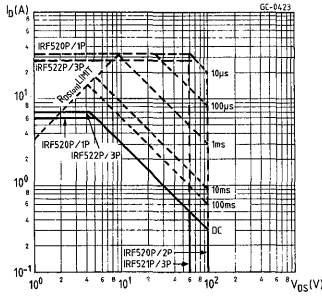
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

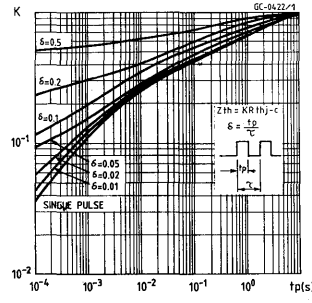


ISOWATT DATA

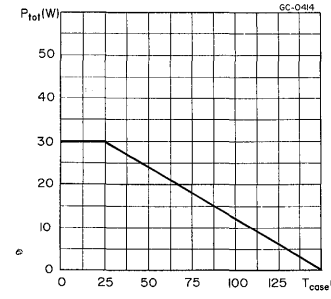
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 530/FI-531/FI
IRF 532/FI-533/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF530	100 V	0.16 Ω	14 A
IRF530FI	100 V	0.16 Ω	9 A
IRF531	80 V	0.16 Ω	14 A
IRF531FI	80 V	0.16 Ω	9 A
IRF532	100 V	0.23 Ω	12 A
IRF532FI	100 V	0.23 Ω	8 A
IRF533	80 V	0.23 Ω	12 A
IRF533FI	80 V	0.23 Ω	8 A

- 80-100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT
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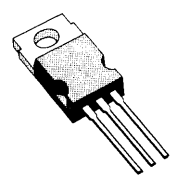
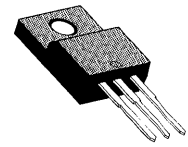
INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power-audio amplifiers and robotics.

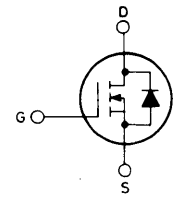


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 530 / 530FI	IRF 531 / 531FI	IRF 532 / 532FI	IRF 533 / 533FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		100	80	100	80	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		100	80	100	80	V
V_{GS}	Gate-source voltage				±20		V
I_{DM} (•)	Drain current (pulsed)		56	56	48	48	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		56	56	48	48	A
			530	**531**	**532**	**533**	
I_D	Drain current (cont.) at T_c = 25°C		14	14	12	12	A
I_D	Drain current (cont.) at T_c = 100°C		9	9	8	8	A
			530FI	**531FI**	**532FI**	**533FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		9	9	8	8	A
I_D ■	Drain current (cont.) at T_c = 100°C		5.5	5.5	5	5	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		79		35		W
■	Derating factor		0.63		0.28		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.58	3.57	°C/W
$R_{thc\text{-s}}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF530/532/530FI/532FI** for **IRF531/533/531FI/533FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF530/531/530FI/531FI** for **IRF532/533/532FI/533FI**	 14 12			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 8.3 A for **IRF530/531/530FI/531FI** for **IRF532/533/532FI/533FI**			 0.16 0.23	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 8.3 A	5.1			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			850 260 50	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 36 V I_D = 8.0 A R_i = 15 Ω (see test circuit)			30 75 40 45	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 14 A V_{DS} = Max Rating × 0.8 (see test circuit)			30	nC

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				14 56	A A
V_{SD} ** Forward on voltage	I_{SD} = 14 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time	T_j = 150°C		360		ns
Q_{rr} Reverse recovered charge	I_{SD} = 14 A di/dt = 100 A/μs		21		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leqslant \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

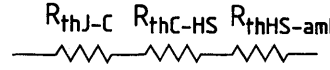
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1



SGS-THOMSON MICROELECTRONICS

IRF 540/FI-541/FI
IRF 542/FI-543/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF540	100 V	0.077 Ω	28 A
IRF540FI	100 V	0.077 Ω	15 A
IRF541	80 V	0.077 Ω	28 A
IRF541FI	80 V	0.077 Ω	15 A
IRF542	100 V	0.100 Ω	25 A
IRF542FI	100 V	0.100 Ω	14 A
IRF543	80 V	0.100 Ω	25 A
IRF543FI	80 V	0.100 Ω	14 A

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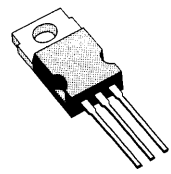
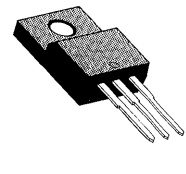
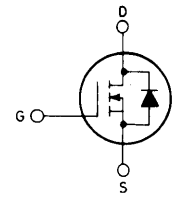


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 540 / 540FI	IRF 541 / 541FI	IRF 542 / 542FI	IRF 543 / 543FI	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)		100	80	100	80	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)		100	80	100	80	V
V_{GS}	Gate-source voltage				±20		V
I_{DM} (•)	Drain current (pulsed)		110	110	100	100	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		110	110	100	100	A
			540	**541**	**542**	**543**	
I_D	Drain current (cont.) at T_c = 25°C		28	28	25	25	A
I_D	Drain current (cont.) at T_c = 100°C		20	20	17	17	A
			540FI	**541FI**	**542FI**	**543FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		15	15	14	14	A
I_D ■	Drain current (cont.) at T_c = 100°C		9	9	8	8	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		125		40		W
	Derating factor		1		0.32		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1	3.12	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

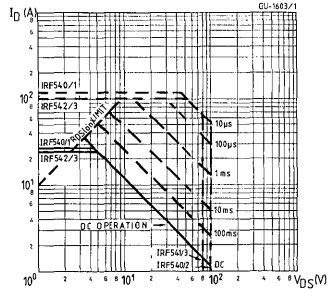
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF540/542/540FI/542FI** for **IRF541/543/541FI/543FI**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF540/541/540FI/541FI** for **IRF542/543/542FI/543FI**	 28 25			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 17 A for **IRF540/541/540FI/541FI** for **IRF542/543/542FI/543FI**			 0.077 0.100	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 17 A	8.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1600 800 300	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 30 V I_D = 15 A R_i = 4.7 Ω (see test circuit)			30 60 80 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 28 A V_{DS} = Max Rating × 0.8 (see test circuit)			59	nC

ELECTRICAL CHARACTERISTICS (Continued)

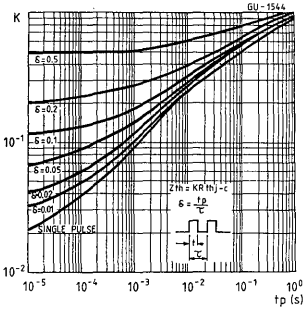
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				28 110	A A
V_{SD} ** Forward on voltage	I_{SD} = 28 A V_{GS} = 0			2.5	V
t_{rr} Reverse recovery time	T_j = 150°C		500		ns
Q_{rr} Reverse recovered charge	I_{SD} = 28 A di/dt = 100 A/μs		2.9		μC

** Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

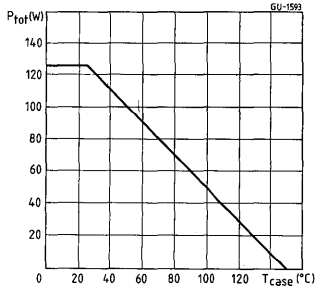
Safe operating areas (standard package)



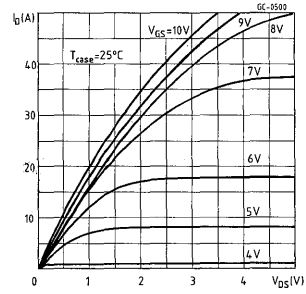
Thermal impedance (standard package)



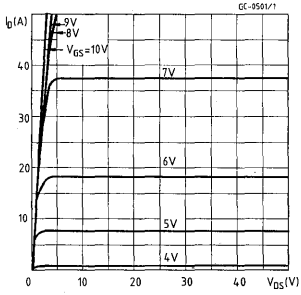
Derating curve (standard package)



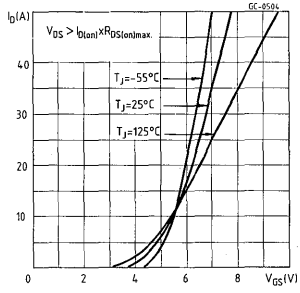
Output characteristics



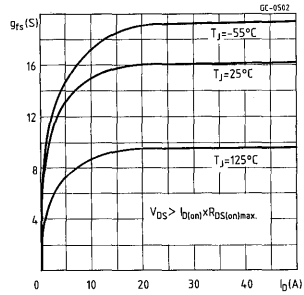
Output characteristics



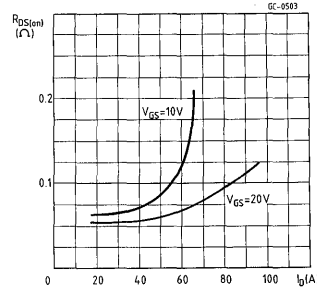
Transfer characteristics



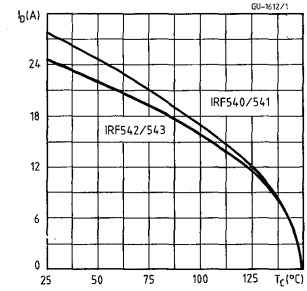
Transconductance



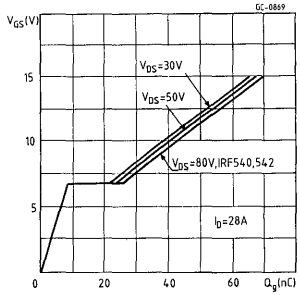
Static drain-source on resistance



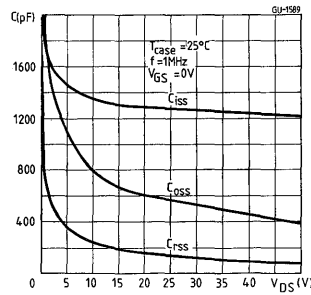
Maximum drain current vs temperature



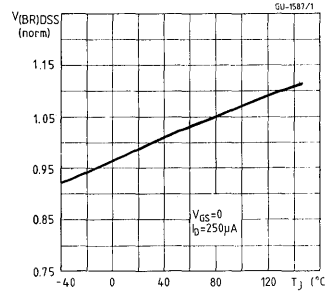
Gate charge vs gate-source voltage



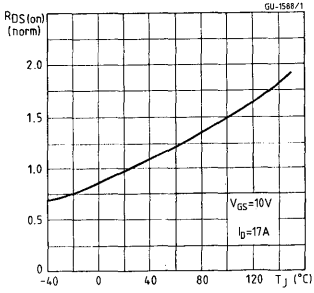
Capacitance variation



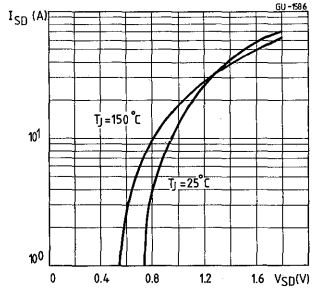
Normalized breakdown voltage vs temperature



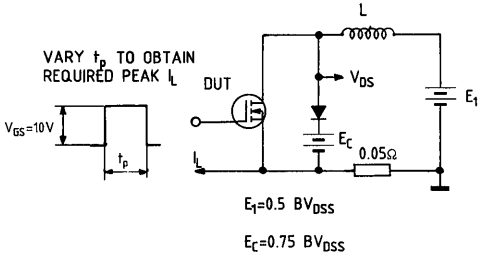
Normalized on resistance vs temperature



Source-drain diode forward characteristics

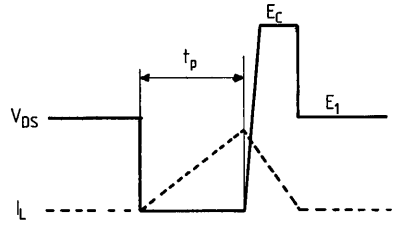


Clamped inductive test circuit



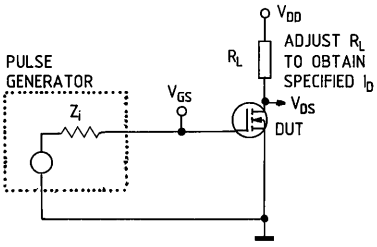
SC-0242

Clamped inductive waveforms



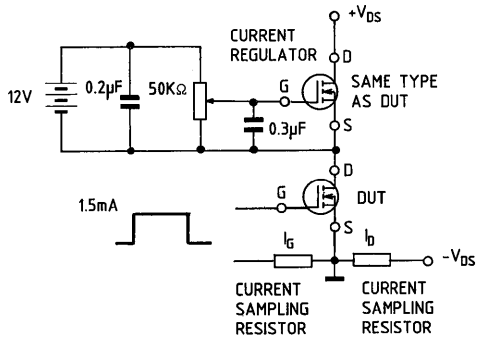
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

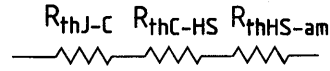
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

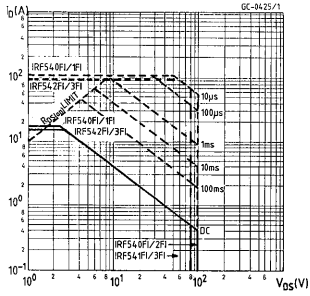
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

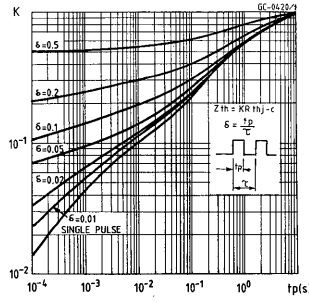


ISOWATT DATA

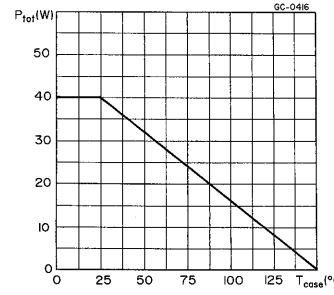
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 620/FI-621/FI
IRF 622/FI-623/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

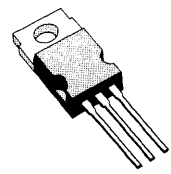
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF620	200 V	0.8 Ω	5 A
IRF620FI	200 V	0.8 Ω	4 A
IRF621	150 V	0.8 Ω	5 A
IRF621FI	150 V	0.8 Ω	4 A
IRF622	200 V	1.2 Ω	4 A
IRF622FI	200 V	1.2 Ω	3.5 A
IRF623	150 V	1.2 Ω	4 A
IRF623FI	150 V	1.2 Ω	3.5 A

- 200V FOR TELECOMMUNICATION APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE - REDUCES COST AND SIZE

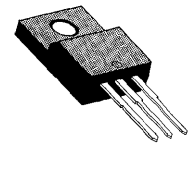
INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- DC SWITCH
- ROBOTCS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses are in telecommunications, robotics, switching power supplies and as a DC switch.

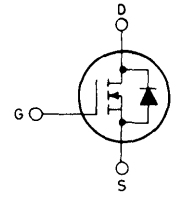


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 620 / 620FI	IRF 621 / 621FI	IRF 622 / 622FI	IRF 623 / 623FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		200	150	200	150	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		200	150	200	150	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		20	20	16	16	A
			620	**621**	**622**	**623**	
I_D	Drain current (cont.) at T_c = 25°C		5	5	4	4	A
I_D	Drain current (cont.) at T_c = 100°C		3	3	2.5	2.5	A
			620FI	**621FI**	**622FI**	**623FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		4	4	3.5	3.5	A
I_D ■	Drain current (cont.) at T_c = 100°C		2.5	2.5	2	2	A
			TO-220		**ISOWATT220**		
P_{tot}	Total dissipation at T_c < 25°C		40		30		W
	Derating factor		0.32		0.24		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

◆ Introduced in 1988 week 44

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

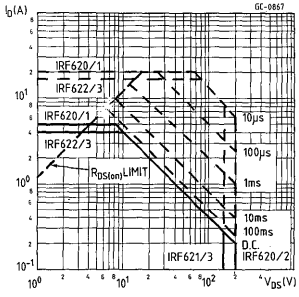
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF620/622/620FI/622FI** for **IRF621/623/621FI/623FI**	 200 150			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ x $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF620/621/620FI/621FI** for **IRF622/623/622FI/623FI**	 5 4			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **IRF620/621/620FI/621FI** for **IRF622/623/622FI/623FI**			 0.8 1.2	 Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **IRF620/621/620FI/621FI** for **IRF622/623/622FI/623FI**	 5 4			 A A
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ x $R_{DS\ (on)\ max}$ I_D = 2.5 A	1.3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			600 300 80	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

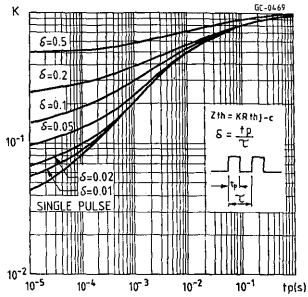
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 75 V I_D = 2.5 A			40	ns
t_r	Rise time	R_i = 50 Ω			60	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)			100	ns
t_f	Fall time				60	ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 6 A V_{DS} = Max Rating × 0.8 (see test circuit)			15	nC
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current				5	A
I_{SDM} (•)	Source-drain current (pulsed)				20	A
V_{SD} **	Forward on voltage	for **IRF620/621/620FI/621FI** I_{SD} = 5 A V_{GS} = 0			1.8	V
		for **IRF622/623/622FI/623FI** I_{SD} = 4 A V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time			350		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 5 A di/dt = 100 A/μs		2.3		μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 In this datasheet

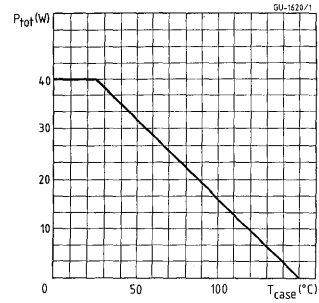
Safe operating areas (standard package)



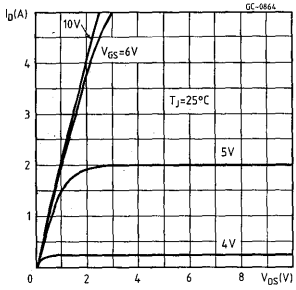
Thermal impedance (standard package)



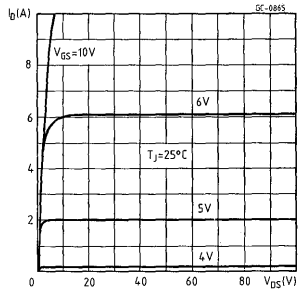
Derating curve (standard package)



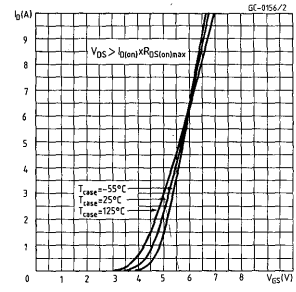
Output characteristics



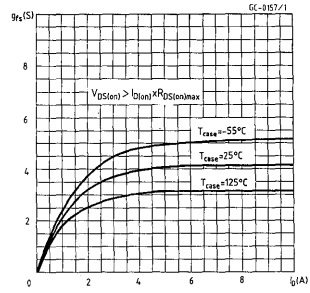
Output characteristics



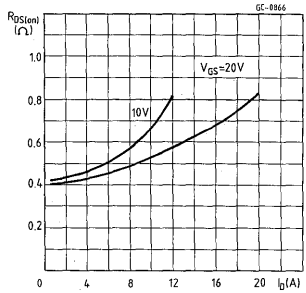
Transfer characteristics



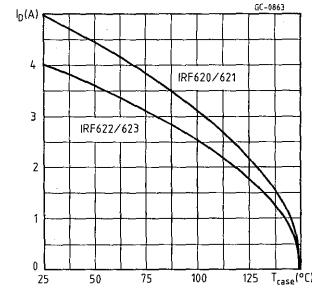
Transconductance



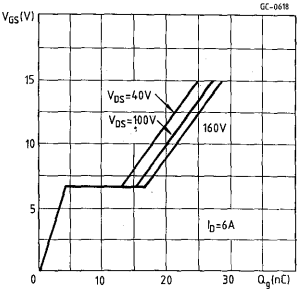
Static drain-source on resistance



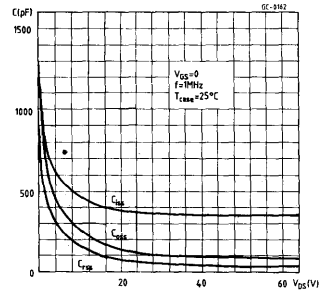
Maximum drain current vs temperature



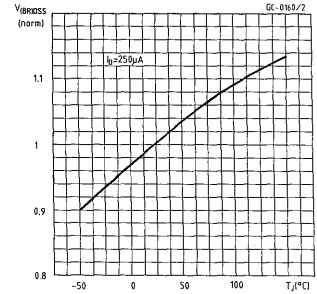
Gate charge vs gate-source voltage



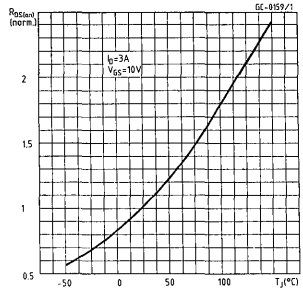
Capacitance variation



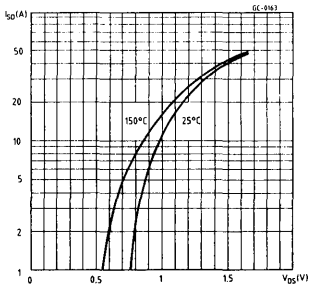
Normalized breakdown voltage vs temperature



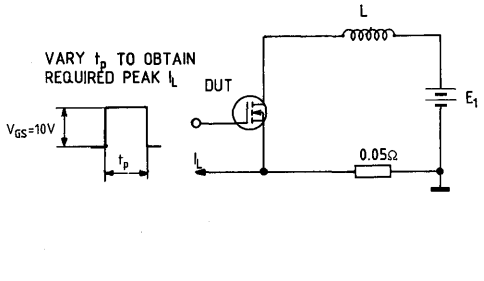
Normalized on resistance vs temperature



Source-drain diode forward characteristics

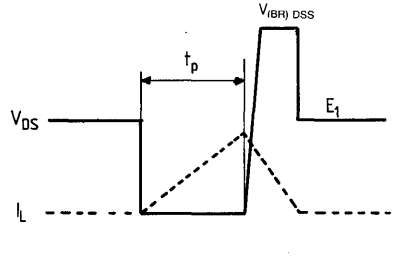


Unclamped inductive test circuit



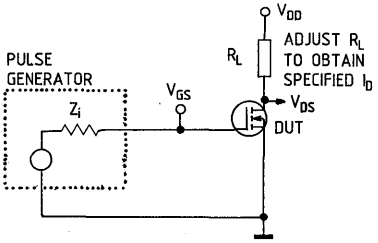
SC-0339

Unclamped inductive waveforms



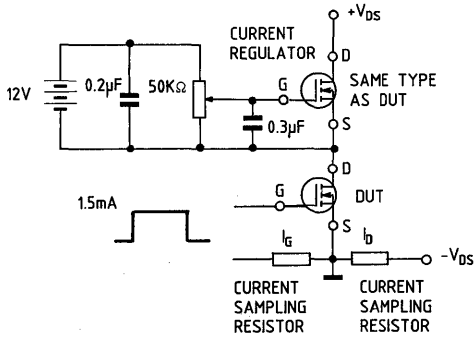
SC-0338

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

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ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\,(tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

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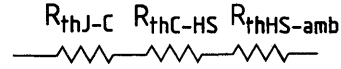
3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

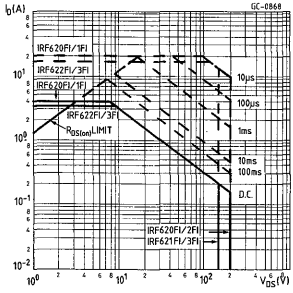
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

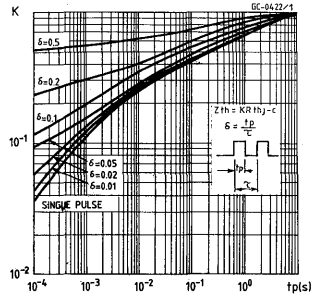


ISOWATT DATA

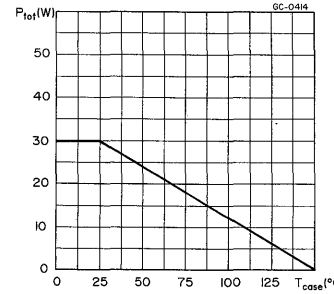
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 720/FI-721/FI
IRF 722/FI-723/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

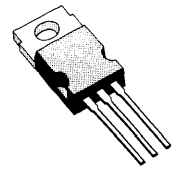
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF720	400 V	1.8 Ω	3.3 A
IRF720FI	400 V	1.8 Ω	2.5 A
IRF721	350 V	1.8 Ω	3.3 A
IRF721FI	350 V	1.8 Ω	2.5 A
IRF722	400 V	2.5 Ω	2.8 A
IRF722FI	400 V	2.5 Ω	2.0 A
IRF723	350 V	2.5 Ω	2.8 A
IRF723FI	350 V	2.5 Ω	2.0 A

- HIGH VOLTAGE - FOR OFF LINE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

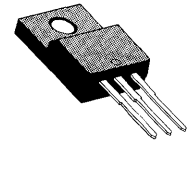
INDUSTRIAL APPLICATIONS:

- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include off-line use, constant current source, ultrasonic equipment and switching powers supplies start-up circuits.

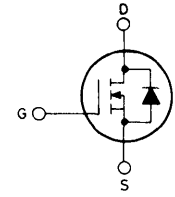


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 720 / 720FI	IRF 721 / 721FI	IRF 722 / 722FI	IRF 723 / 723FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		400	350	400	350	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		400	350	400	350	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		13	13	11	11	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		13	13	11	11	A
			720	721	722	723	
I_D	Drain current (cont.) at T_c = 25°C		3.3	3.3	2.8	2.8	A
I_D	Drain current (cont.) at T_c = 100°C		2.1	2.1	1.8	1.8	A
			720FI	721FI	722FI	723FI	
I_D ■	Drain current (cont.) at T_c = 25°C		2.5	2.5	2	2	A
I_D ■	Drain current (cont.) at T_c = 100°C		1.5	1.5	1.2	1.2	A
		TO-220	ISOWATT220				
P_{tot} ■	Total dissipation at T_c < 25°C	50	30				W
■	Derating factor	0.40	0.24				W/°C
T_{stg}	Storage temperature	−55 to 150					°C
T_j	Max. operating junction temperature	150					°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	2.50	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

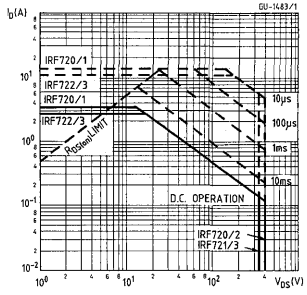
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF720/722/720FI/722FI** for **IRF721/723/721FI/723FI**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF720/721/720FI/721FI** for **IRF722/723/722FI/723FI**	 3.3 2.8			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.8 A for **IRF720/721/720FI/721FI** for **IRF722/723/722FI/723FI**			 1.8 2.5	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 1.8 A	1.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			600 200 40	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 175 V I_D = 1.5 A R_i = 50 Ω (see test circuit)			40 50 100 50	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 3.3 A V_{DS} = Max Rating × 0.8 (see test circuit)			15	nC

ELECTRICAL CHARACTERISTICS (Continued)

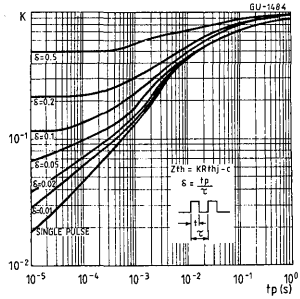
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				3.3 13	A A
V_{SD} Forward on voltage	I_{SD} = 3.3 A V_{GS} = 0			1.6	V
t_{rr} Reverse recovery time			450		ns
Q_{rr} Reverse recovered charge	I_{SD} = 3.3 A di/dt = 100 A/μs		3.1		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

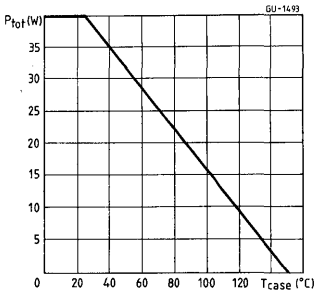
Safe operating areas (standard package)



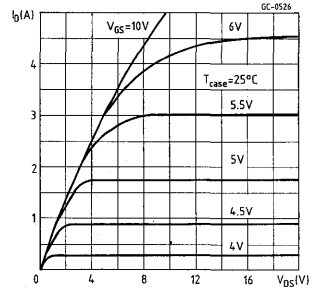
Thermal impedance (standard package)



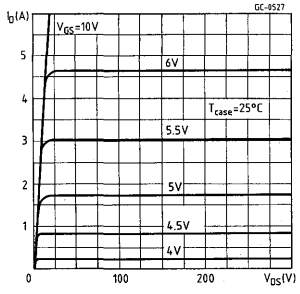
Derating curve (standard package)



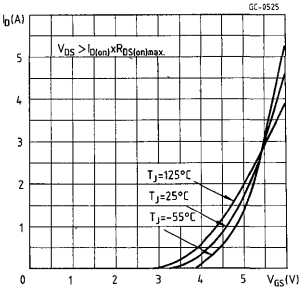
Output characteristics



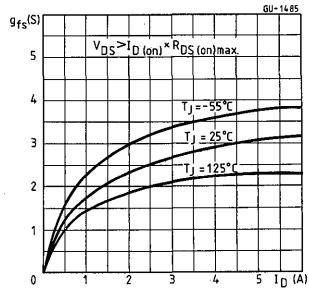
Output characteristics



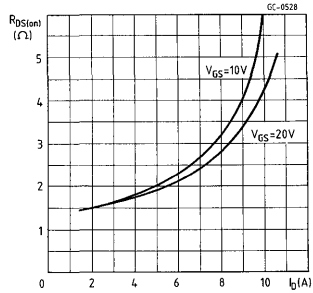
Transfer characteristics



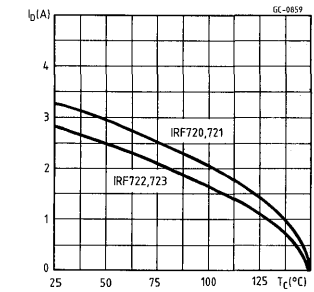
Transconductance



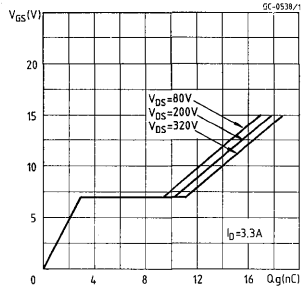
Static drain-source on resistance



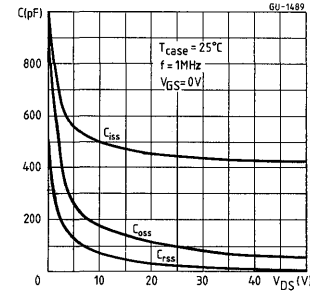
Maximum drain current vs temperature



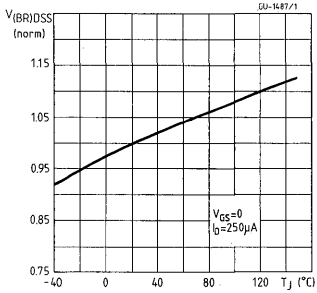
Gate charge vs gate-source voltage



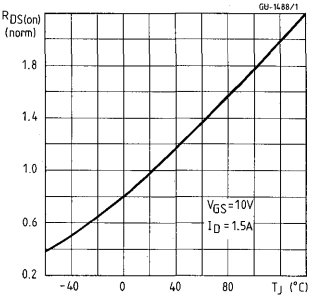
Capacitance variation



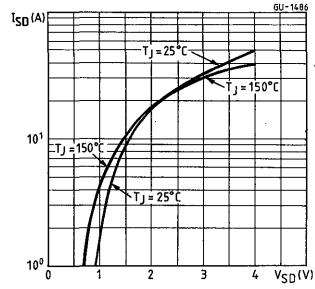
Normalized breakdown voltage vs temperature



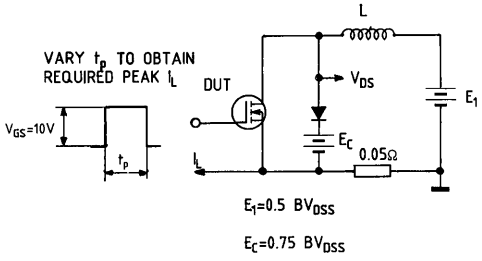
Normalized on resistance vs temperature



Source-drain diode forward characteristics

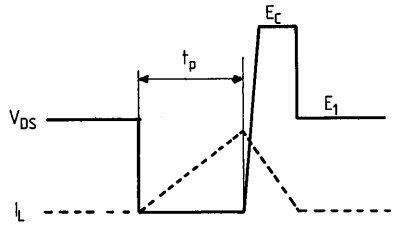


Clamped inductive test circuit



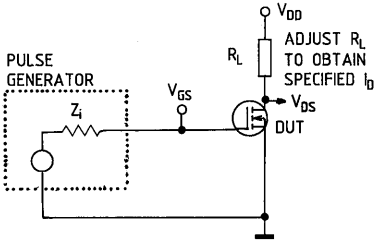
SC-0242

Clamped inductive waveforms



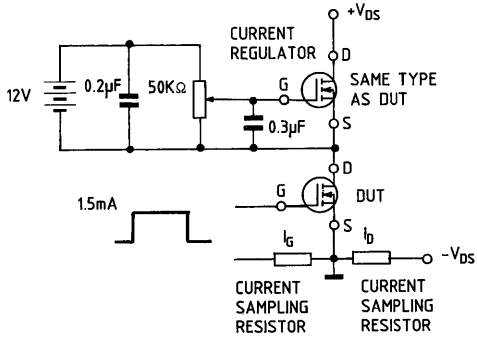
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

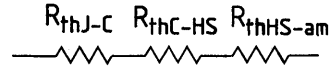
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

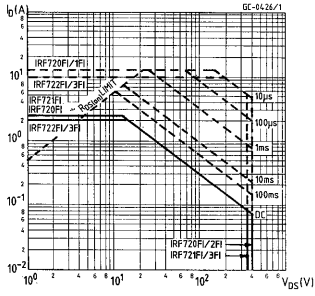
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

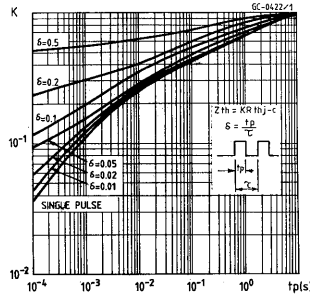


ISOWATT DATA

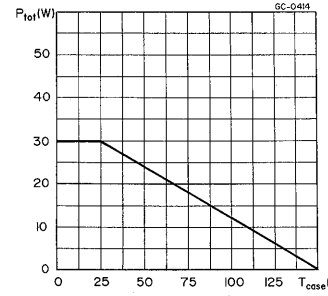
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 730/FI-731/FI
IRF 732/FI-733/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

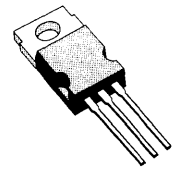
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF730	400 V	1.0 Ω	5.5 A
IRF730FI	400 V	1.0 Ω	3.5 A
IRF731	350 V	1.0 Ω	5.5 A
IRF731FI	350 V	1.0 Ω	3.5 A
IRF732	400 V	1.5 Ω	4.5 A
IRF732FI	400 V	1.5 Ω	3.0 A
IRF733	350 V	1.5 Ω	4.5 A
IRF733FI	350 V	1.5 Ω	3.0 A

- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

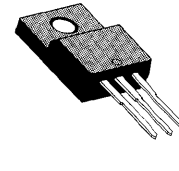
INDUSTRIAL APPLICATIONS:

- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps.

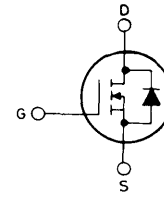


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 730 / 730FI	IRF 731 / 731FI	IRF 732 / 732FI	IRF 733 / 733FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		400	350	400	350	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		400	350	400	350	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		20	20	16	16	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		20	20	16	16	A
			730	**731**	**732**	**733**	
I_D	Drain current (cont.) at T_c = 25°C		5.5	5.5	4.5	4.5	A
I_D	Drain current (cont.) at T_c = 100°C		3.5	3.5	3	3	A
			730FI	**731FI**	**732FI**	**733FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		3.5	3.5	3	3	A
I_D ■	Drain current (cont.) at T_c = 100°C		2	2	1.8	1.8	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		74		35		W
■	Derating factor		0.59		0.28		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.69	3.57	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

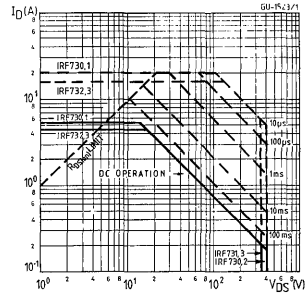
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF730/732/730FI/732FI** for **IRF731/733/731FI/733FI**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF730/731/730FI/731FI** for **IRF732/733/732FI/733FI**	 5.5 4.5			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3.0 A for **IRF730/731/730FI/731FI** for **IRF732/733/732FI/733FI**			 1.0 1.5	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 3.0 A	2.9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			800 300 80	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 175 V I_D = 3.0 A R_i = 15 Ω (see test circuit)			30 35 55 35	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 5.5 A V_{DS} = Max Rating × 0.8 (see test circuit)			35	nC

ELECTRICAL CHARACTERISTICS (Continued)

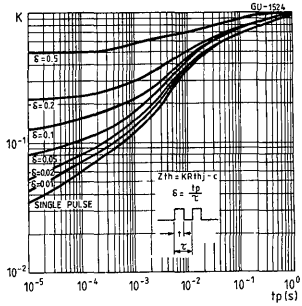
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				5.5 20	A A
V_{SD} Forward on voltage	I_{SD} = 5.5 A V_{GS} = 0			1.6	V
t_{rr} Reverse recovery time	T_j = 150°C		600		ns
Q_{rr} Reverse recovered charge	I_{SD} = 5.5 A di/dt = 100 A/μs		4		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

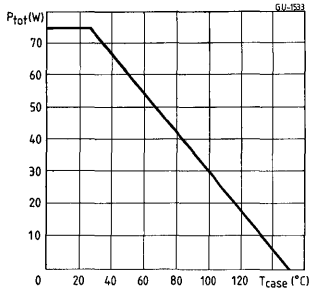
Safe operating areas (standard package)



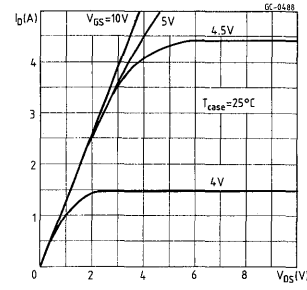
Thermal impedance (standard package)



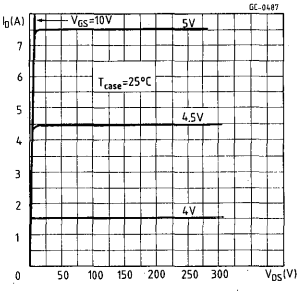
Derating curve (standard package)



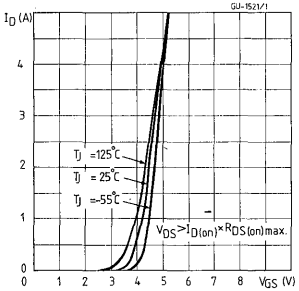
Output characteristics



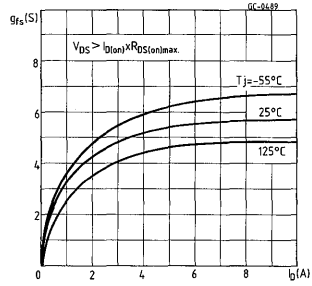
Output characteristics



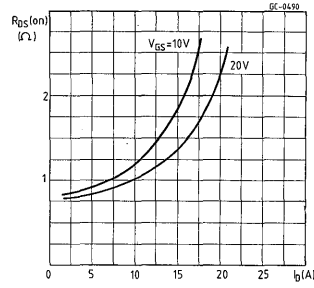
Transfer characteristics



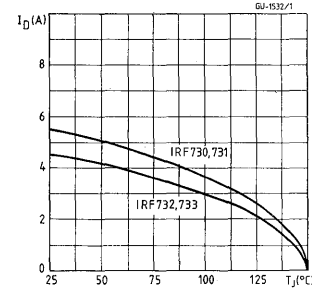
Transconductance



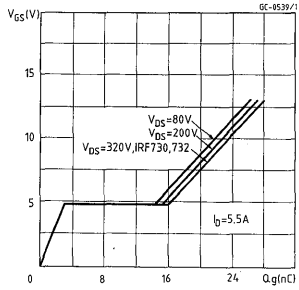
Static drain-source on resistance



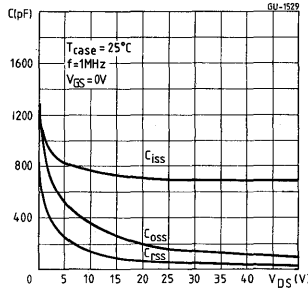
Maximum drain current vs temperature



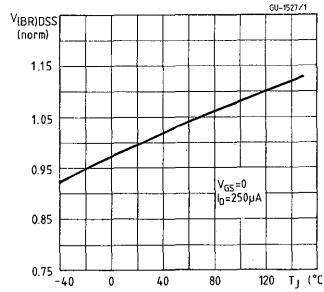
Gate charge vs gate-source voltage



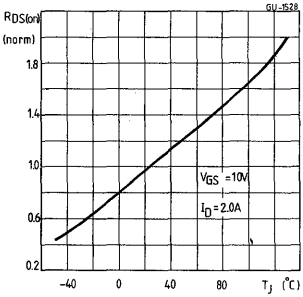
Capacitance variation



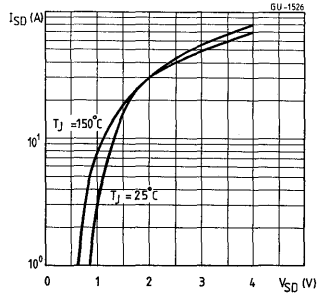
Normalized breakdown voltage vs temperature



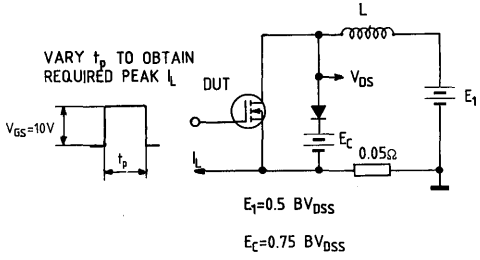
Normalized on resistance vs temperature



Source-drain diode forward characteristics

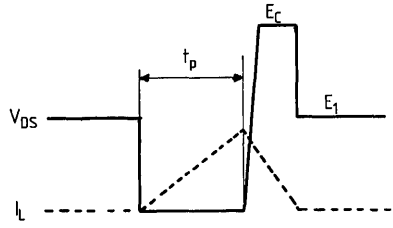


Clamped inductive test circuit



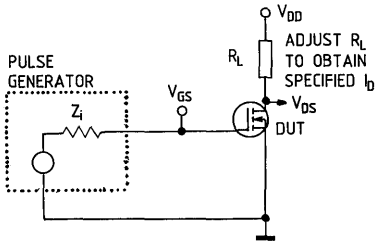
SC-0242

Clamped inductive waveforms



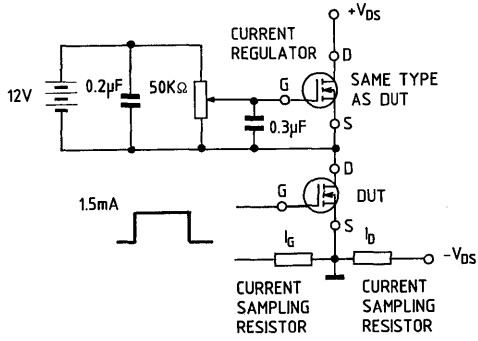
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

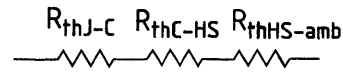
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

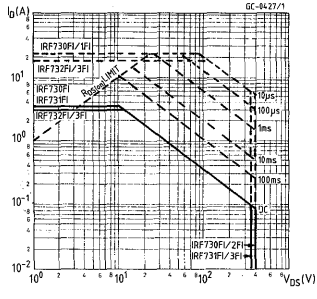
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

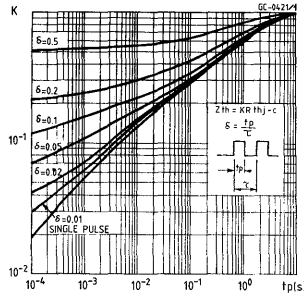


ISOWATT DATA

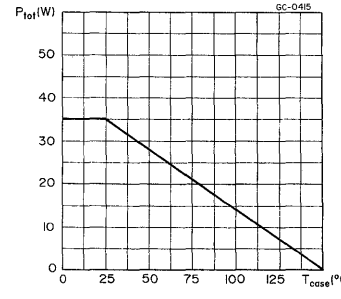
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 740/FI-741/FI
IRF 742/FI-743/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

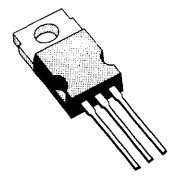
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF740	400 V	0.55 Ω	10 A
IRF740FI	400 V	0.55 Ω	5.5 A
IRF741	350 V	0.55 Ω	10 A
IRF741FI	350 V	0.55 Ω	5.5 A
IRF742	400 V	0.8 Ω	8.3 A
IRF742FI	400 V	0.8 Ω	4.5 A
IRF743	350 V	0.8 Ω	8.3 A
IRF743FI	350 V	0.8 Ω	4.5 A

- HIGH VOLTAGE - FOR SWITCHING POWER SUPPLIES
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCED COST AND SIZE

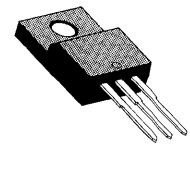
INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC switch, switching power supplies, ultrasonic equipment and electronic ballast for fluorescent lamps.

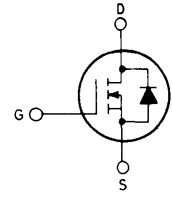


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 740 / 740FI	IRF 741 / 741FI	IRF 742 / 742FI	IRF 743 / 743FI	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)		400	350	400	350	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)		400	350	400	350	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		40	40	33	33	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		40	40	33	33	A
			740	**741**	**742**	**743**	
I_D	Drain current (cont.) at T_c = 25°C		10	10	8.3	8.3	A
I_D	Drain current (cont.) at T_c = 100°C		6.3	6.3	5.2	5.2	A
			740FI	**741FI**	**742FI**	**743FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		5.5	5.5	4.5	4.5	A
I_D ■	Drain current (cont.) at T_c = 100°C		3	3	2.5	2.5	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		125		40		W
■	Derating factor		1		0.32		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1	3.12	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

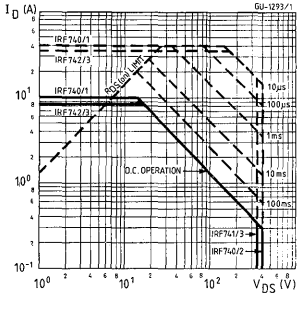
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF740/742/740FI/742FI** for **IRF741/743/741FI/743FI**	 400 350			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF740/741/740FI/741FI** for **IRF742/743/742FI/743FI**	 10 8.3			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5.2 A for **IRF740/741/740FI/741FI** for **IRF742/743/742FI/743FI**			0.55 0.8	Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 5.2 A	4.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1600 450 150	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 175 V I_D = 5.0 A R_i = 4.7 Ω (see test circuit)			35 15 90 35	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 10 A V_{DS} = Max Rating × 0.8 (see test circuit)			63	nC

ELECTRICAL CHARACTERISTICS (Continued)

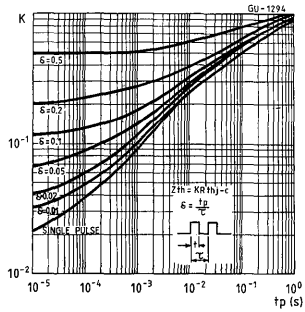
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				10 40	A A
V_{SD} Forward on voltage	I_{SD} = 10 A V_{GS} = 0			2.0	V
t_{rr} Reverse recovery time	T_j = 150°C		800		ns
Q_{rr} Reverse recovered charge	I_{SD} = 10 A di/dt = 100 A/μs		5.7		μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

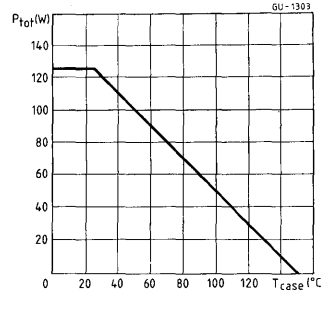
Safe operating areas (standard package)



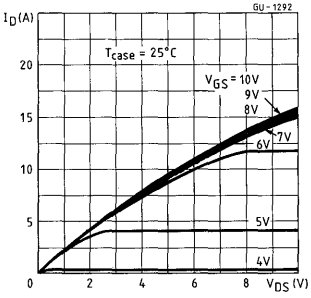
Thermal impedance (standard package)



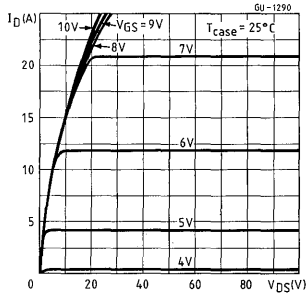
Derating curve (standard package)



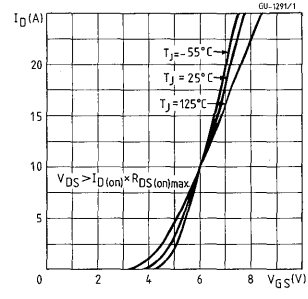
Output characteristics



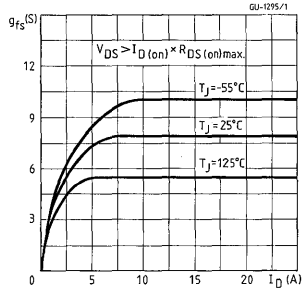
Output characteristics



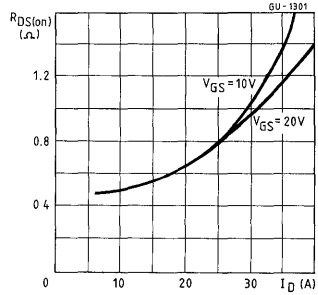
Transfer characteristics



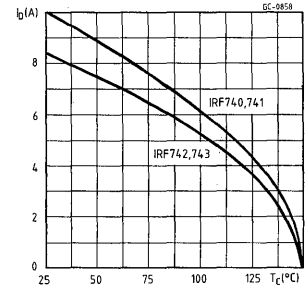
Transconductance



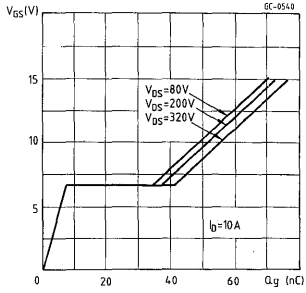
Static drain-source on resistance



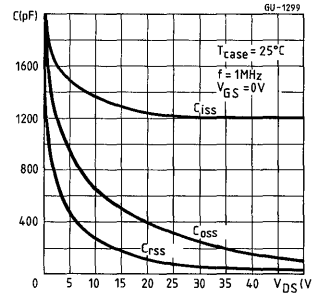
Maximum drain current vs temperature



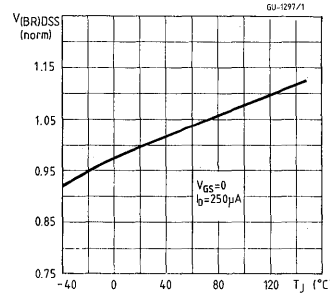
Gate charge vs gate-source voltage



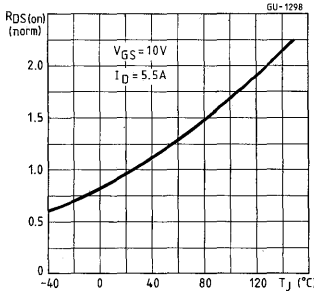
Capacitance variation



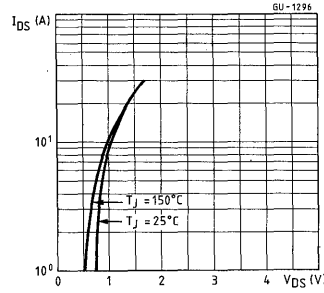
Normalized breakdown voltage vs temperature



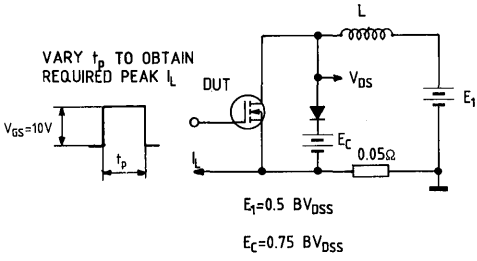
Normalized on resistance vs temperature



Source-drain diode forward characteristics



Clamped inductive test circuit



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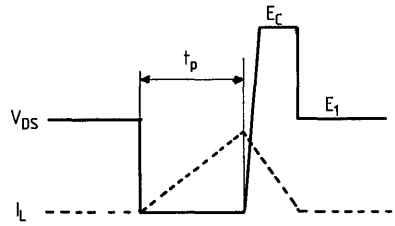
Clamped inductive waveforms



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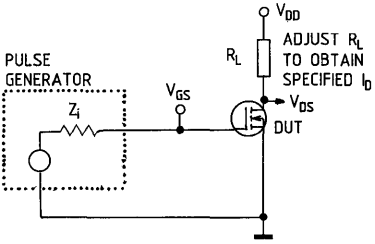
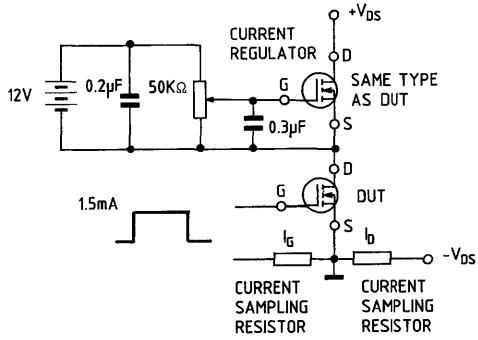
Switching times test circuit



SC-0246

Gate charge test circuit



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ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leqslant \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

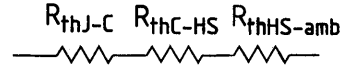
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

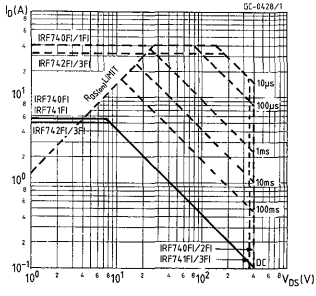
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

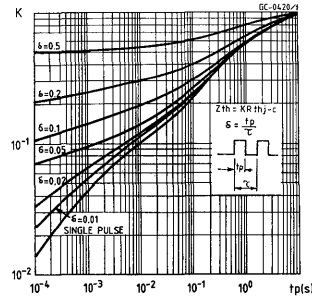


ISOWATT DATA

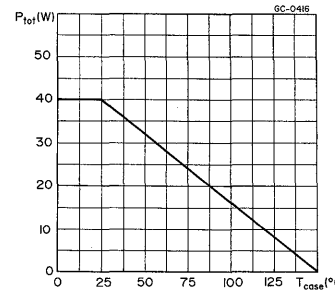
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 820/FI-821/FI
IRF 822/FI-823/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

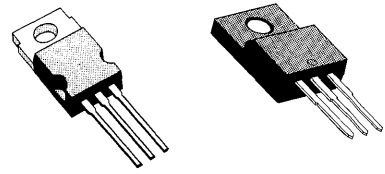
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF820	500 V	3.0 Ω	2.5 A
IRF820FI	500 V	3.0 Ω	2.0 A
IRF821	450 V	3.0 Ω	2.5 A
IRF821FI	450 V	3.0 Ω	2.0 A
IRF822	500 V	4.0 Ω	2.2 A
IRF822FI	500 V	4.0 Ω	1.5 A
IRF823	450 V	4.0 Ω	2.2 A
IRF823FI	450 V	4.0 Ω	1.5 A

- HIGH VOLTAGE - 450 V FOR OFF LINE SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > KHz
- EASY DRIVE- FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

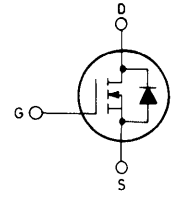
- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical applications include switching power supplies, uninterruptible power supplies and motor speed control.



TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 820 / 820FI	IRF 821 / 821FI	IRF 822 / 822FI	IRF 823 / 823FI	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)		500	450	500	450	V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)		500	450	500	450	V
V_{GS}	Gate-source voltage				±20		V
I_{DM} (•)	Drain current (pulsed)		8	8	7	7	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		8	8	7	7	A
			820	**821**	**822**	**823**	
I_D	Drain current (cont.) at T_c = 25°C		2.5	2.5	2.2	2.2	A
I_D	Drain current (cont.) at T_c = 100°C		1.6	1.6	1.4	1.4	A
			820FI	**821FI**	**822FI**	**823FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		2	2	1.5	1.5	A
I_D ■	Drain current (cont.) at T_c = 100°C		1.2	1.2	0.9	0.9	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		50		30		W
■	Derating factor		0.40		0.24		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	2.5	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

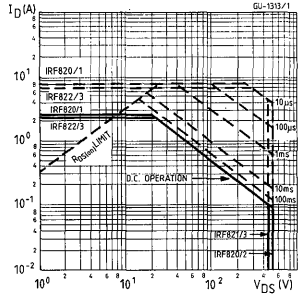
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF820/822/820FI/822FI** for **IRF821/823/821FI/823FI**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF820/821/820FI/821FI** for **IRF822/823/821FI/823FI**	 2.5 2.2			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.4 A for **IRF820/821/820FI/821FI** for **IRF822/823/822FI/823FI**			 3.0 4.0	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 1.4 A	1.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			400 150 40	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 1.0 A R_i = 50 Ω (see test circuit)			60 50 60 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 2.5 A V_{DS} = Max Rating × 0.8 (see test circuit)			19	nC

ELECTRICAL CHARACTERISTICS (Continued)

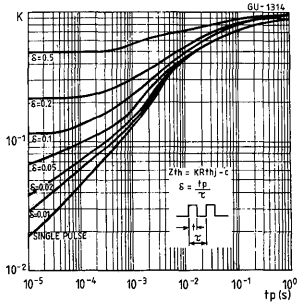
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				2.5 10	A A
V_{SD} ** Forward on voltage	I_{SD} = 2.5 A V_{GS} = 0			1.6	V
t_{rr} Reverse recovery time	T_j = 150°C		600		ns
Q_{rr} Reverse recovered charge	I_{SD} = 2.5 A di/dt = 100 A/μs		3.5		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

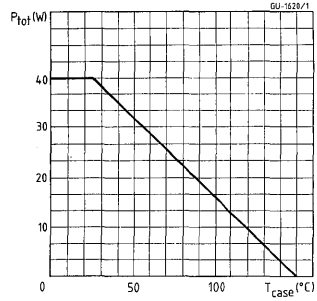
Safe operating areas (standard package)



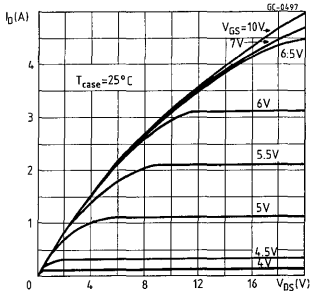
Thermal impedance (standard package)



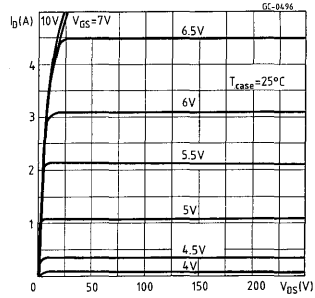
Derating curve (standard package)



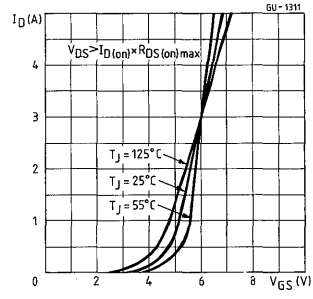
Output characteristics



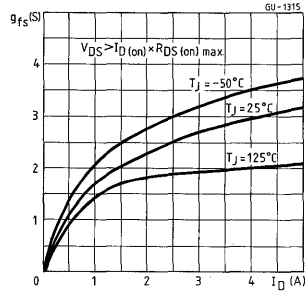
Output characteristics



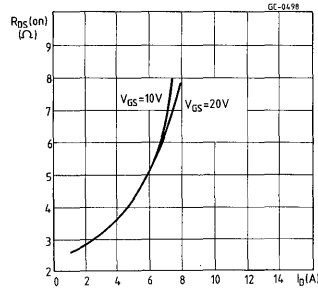
Transfer characteristics



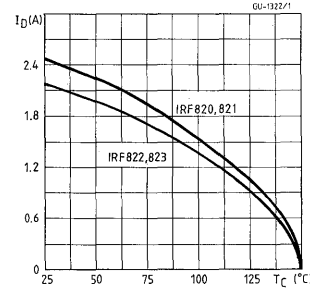
Transconductance



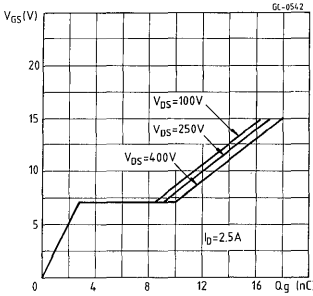
Static drain-source on resistance



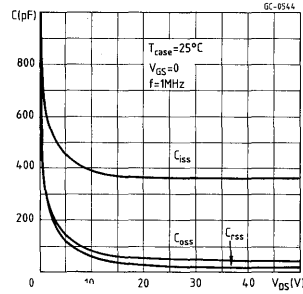
Maximum drain current vs temperature



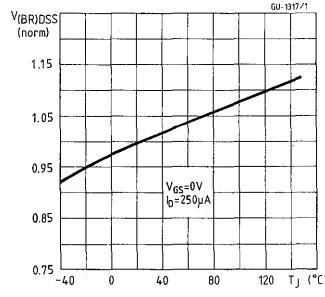
Gate charge vs gate-source voltage



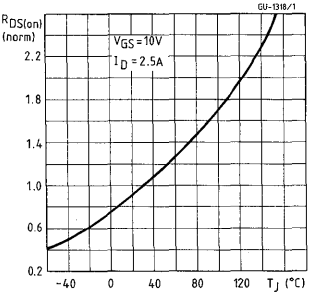
Capacitance variation



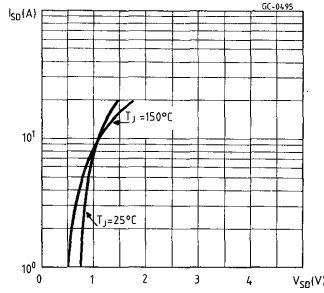
Normalized breakdown voltage vs temperature



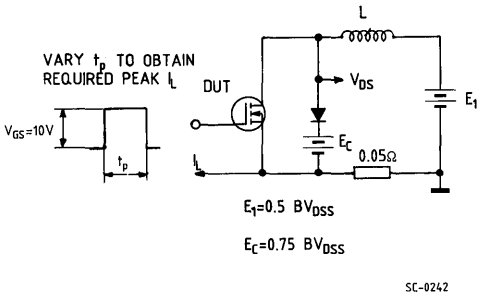
Normalized on resistance vs temperature



Source-drain diode forward characteristics



Clamped inductive test circuit



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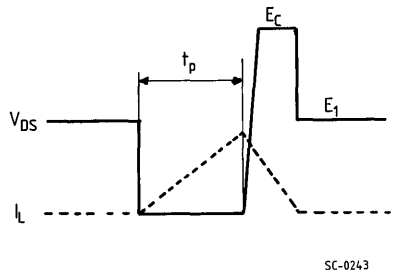
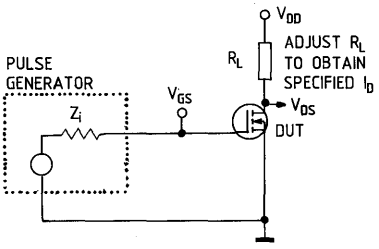
Clamped inductive waveforms



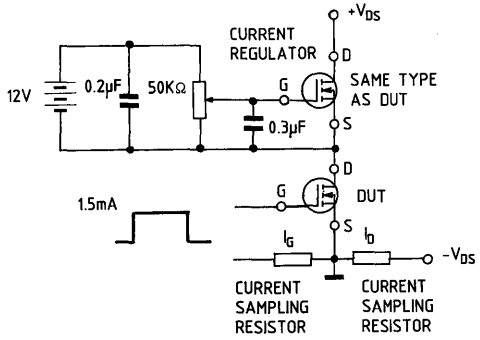
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

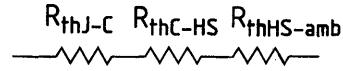
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

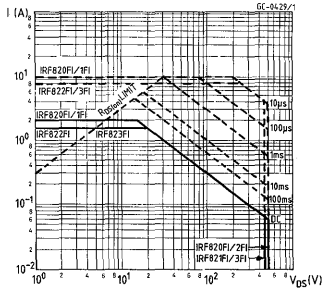
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

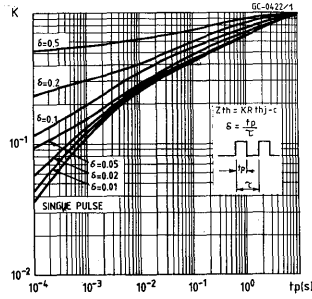


ISOWATT DATA

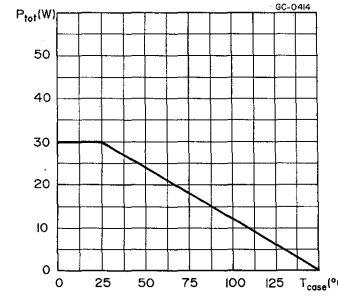
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 830/FI-831/FI
IRF 832/FI-833/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

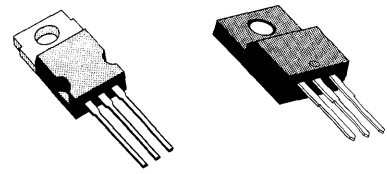
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF830	500 V	1.5 Ω	4.5 A
IRF830FI	500 V	1.5 Ω	3.0 A
IRF831	450 V	1.5 Ω	4.5 A
IRF831FI	450 V	1.5 Ω	3.0 A
IRF832	500 V	2.0 Ω	4.0 A
IRF832FI	500 V	2.0 Ω	2.5 A
IRF833	450 V	2.0 Ω	4.0 A
IRF833FI	450 V	2.0 Ω	2.5 A

- HIGH VOLTAGE - 450 V FOR OFF LINE SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE
- COST EFFECTIVE PLASTIC PACKAGE

INDUSTRIAL APPLICATIONS:

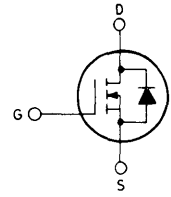
- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include SMPS, lamp ballast and motor control.



TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 830 / 830FI	IRF 831 / 831FI	IRF 832 / 832FI	IRF 833 / 833FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		500	450	500	450	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		500	450	500	450	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		15	15	13	13	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		15	15	13	13	A
			830	**831**	**832**	**833**	
I_D	Drain current (cont.) at T_c = 25°C		4.5	4.5	4	4	A
I_D	Drain current (cont.) at T_c = 100°C		3	3	2.5	2.5	A
			830FI	**831FI**	**832FI**	**833FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		3	3	2.5	2.5	A
I_D ■	Drain current (cont.) at T_c = 100°C		1.8	1.8	1.5	1.5	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		74		35		W
■	Derating factor		0.59		0.28		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.69	3.57	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF830/832/830FI/832FI** for **IRF831/833/831FI/833FI**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF830/831/830FI/831FI** for **IRF832/833/832FI/833FI**	 4.5 4.0			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **IRF830/831/830FI/831FI** for **IRF832/833/832FI/833FI**			 1.5 2.0	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 2.5 A	2.7			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			800 200 60	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 2.5 A R_i = 15 Ω (see test circuit)			30 30 55 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 4.5 A V_{DS} = Max Rating × 0.8 (see test circuit)			32	nC

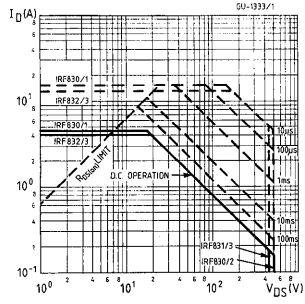
▪ See note on ISOWATT220 in this datasheet
** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽2%

ELECTRICAL CHARACTERISTICS (Continued)

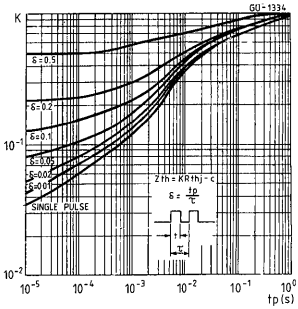
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				4.5 15	A A
V_{SD} ** Forward on voltage	I_{SD} = 4.5 A V_{GS} = 0			1.6	V
t_{rr} Reverse recovery time	T_j = 150°C		800		ns
Q_{rr} Reverse recovered charge	I_{SD} = 4.5 A di/dt = 100 A/μs		4.6		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%
(•) Repetive Rating: Pulse width limited by max junction temperature

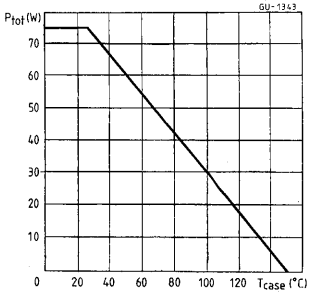
Safe operating areas (standard package)



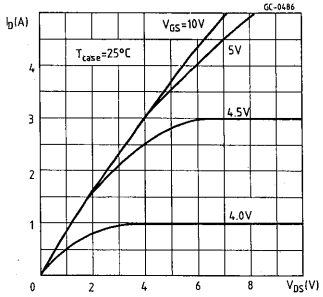
Thermal impedance (standard package)



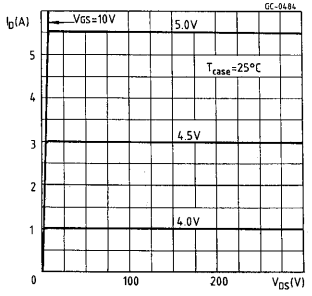
Derating curve (standard package)



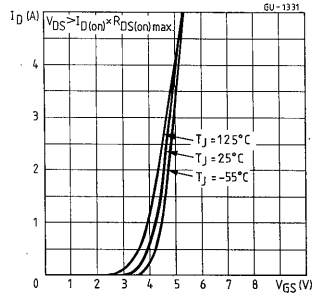
Output characteristics



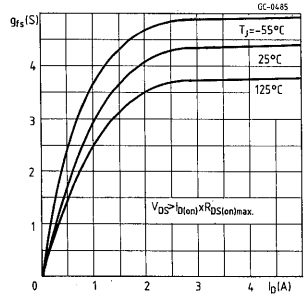
Output characteristics



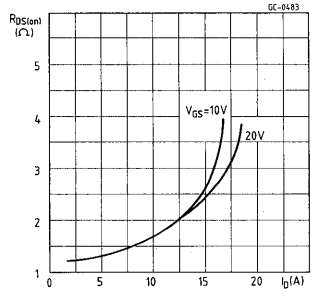
Transfer characteristics



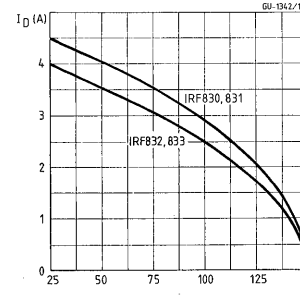
Transconductance



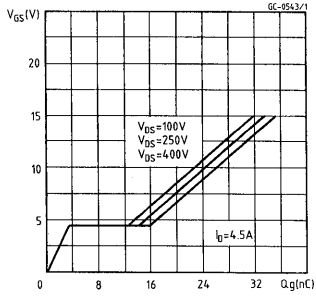
Static drain-source on resistance



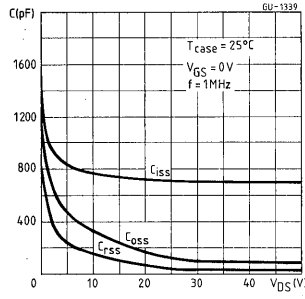
Maximum drain current vs temperature



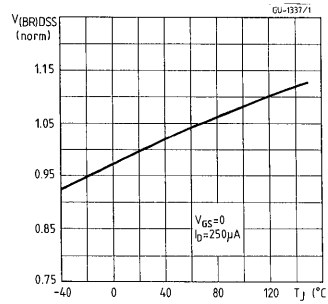
Gate charge vs gate-source voltage



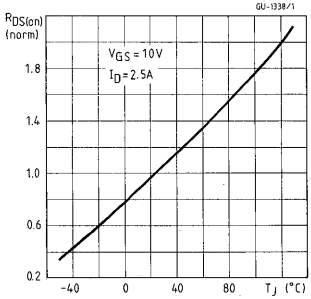
Capacitance variation



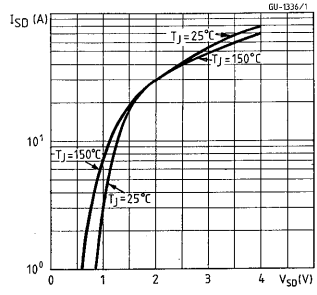
Normalized breakdown voltage vs temperature



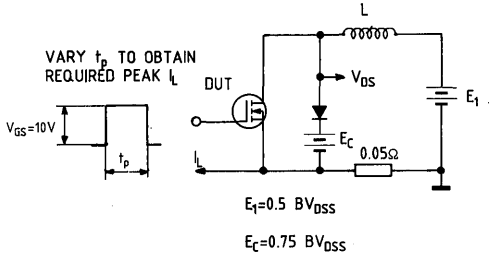
Normalized on resistance vs temperature



Source-drain diode forward characteristics

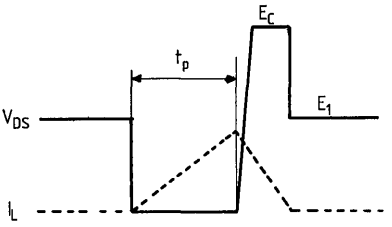


Clamped inductive test circuit



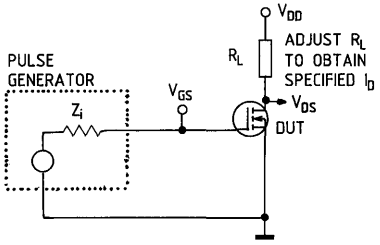
SC-0242

Clamped inductive waveforms



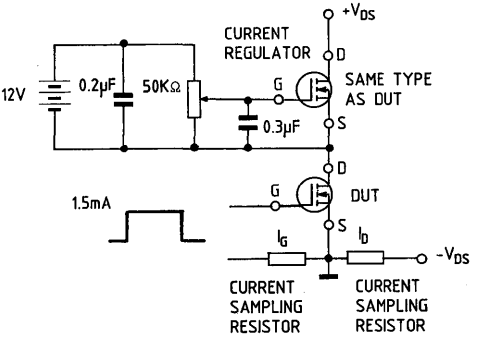
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

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THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

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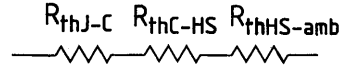
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

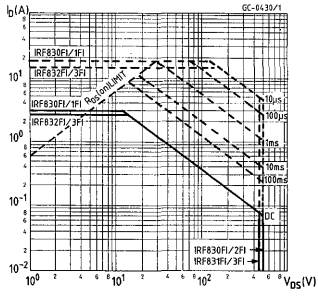
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

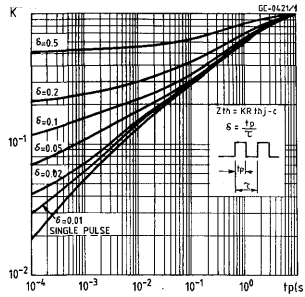


ISOWATT DATA

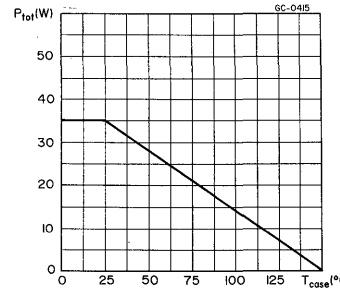
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRF 840/FI-841/FI
IRF 842/FI-843/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

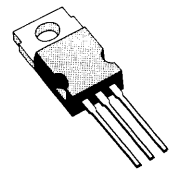
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRF840	500 V	0.85 Ω	8 A
IRF840FI	500 V	0.85 Ω	4.5 A
IRF841	450 V	0.85 Ω	8 A
IRF841FI	450 V	0.85 Ω	4.5 A
IRF842	500 V	1.1 Ω	7 A
IRF842FI	500 V	1.1 Ω	4 A
IRF843	450 V	1.1 Ω	7 A
IRF843FI	450 V	1.1 Ω	4 A

- HIGH VOLTAGE - 450 V FOR OFF LINE SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - FOR REDUCED COST AND SIZE
- COST EFFECTIVE PLASTIC PACKAGE

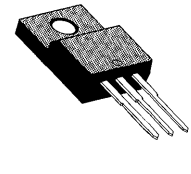
INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.

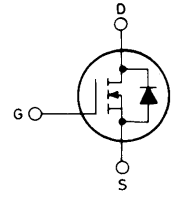


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	IRF 840 / 840FI	IRF 841 / 841FI	IRF 842 / 842FI	IRF 843 / 843FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		500	450	500	450	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		500	450	500	450	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		32	32	28	28	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		32	32	28	28	A
			840	**841**	**842**	**843**	
I_D	Drain current (cont.) at T_c = 25°C		8	8	7	7	A
I_D	Drain current (cont.) at T_c = 100°C		5.1	5.1	4.4	4.4	A
			840FI	**841FI**	**842FI**	**843FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		4.5	4.5	4	4	A
I_D ■	Drain current (cont.) at T_c = 100°C		2.8	2.8	2.5	2.5	A
			TO-220		**ISOWATT220**		
P_{tot} ■	Total dissipation at T_c < 25°C		125		40		W
■	Derating factor		1		0.32		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature.

■ See note on ISOWATT220 on this datasheet.

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	3.12	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

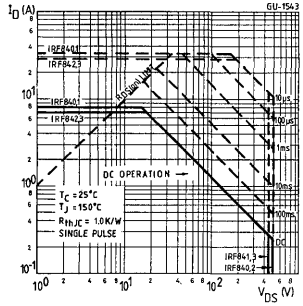
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRF840/842/840FI/842FI** for **IRF841/843/841FI/843FI**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRF840/841/840FI/841FI** for **IRF842/843/842FI/843FI**	 8 7			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4.4 A for **IRF840/841/840FI/841FI** for **IRF842/843/842FI/843FI**			 0.85 1.1	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 4.4 A	4.9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1600 350 150	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 200 V I_D = 4.0 A R_i = 4.7 Ω (see test circuit)			35 15 90 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 8 A V_{DS} = Max Rating × 0.8 (see test circuit)			63	nC

ELECTRICAL CHARACTERISTICS (Continued)

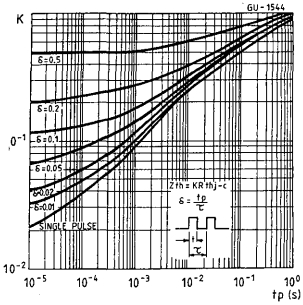
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				8 32	A A
V_{SD} ** Forward on voltage	I_{SD} = 8 A V_{GS} = 0			2	V
t_{rr} Reverse recovery time	T_j = 150°C		1100		ns
Q_{rr} Reverse recovered charge	I_{SD} = 8.0 A di/dt = 100 A/μs		6.4		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%
(•) Repetive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

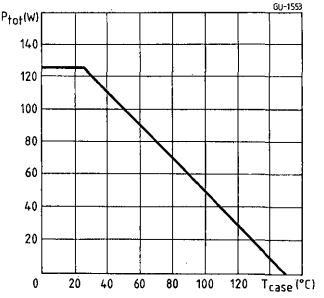
Safe operating areas (standard package)



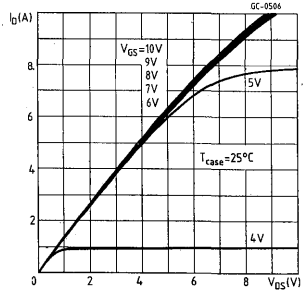
Thermal impedance (standard package)



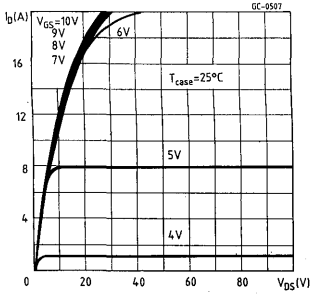
Derating curve (standard package)



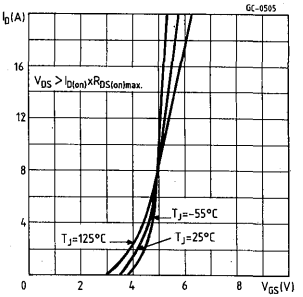
Output characteristics



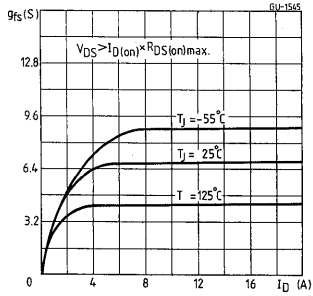
Output characteristics



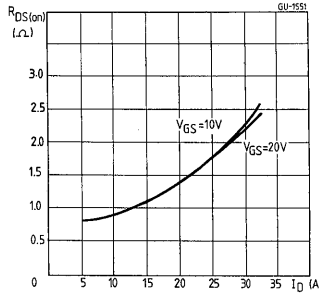
Transfer characteristics



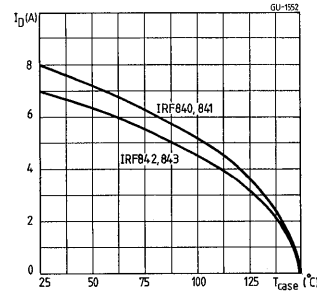
Transconductance



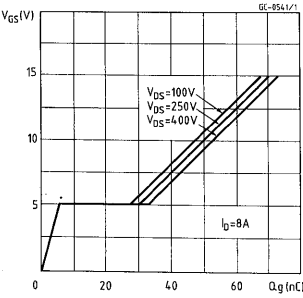
Static drain-source on resistance



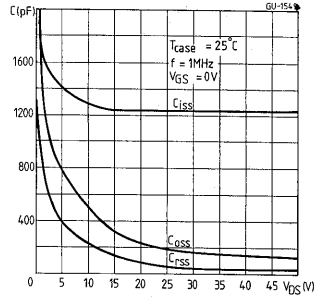
Maximum drain current vs temperature



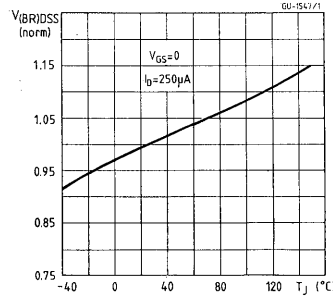
Gate charge vs gate-source voltage



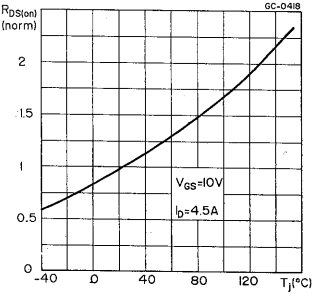
Capacitance variation



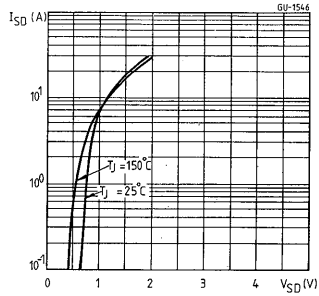
Normalized breakdown voltage vs temperature



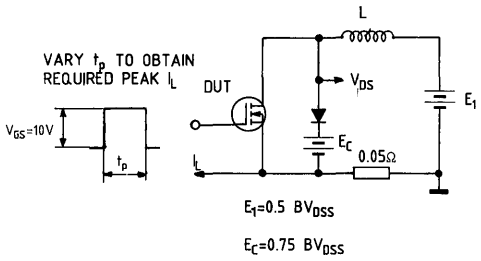
Normalized on resistance vs temperature



Source-drain diode forward characteristics

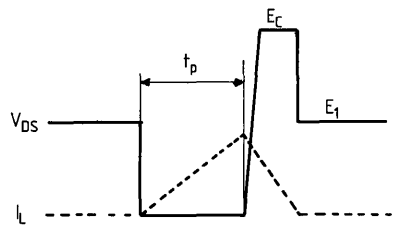


Clamped inductive test circuit



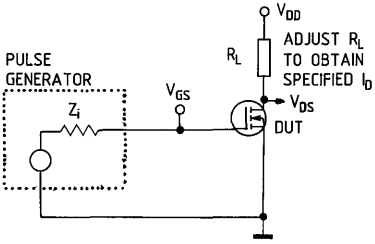
SC-0242

Clamped inductive waveforms



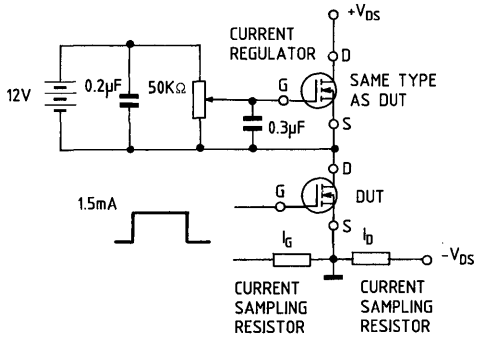
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

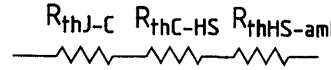
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

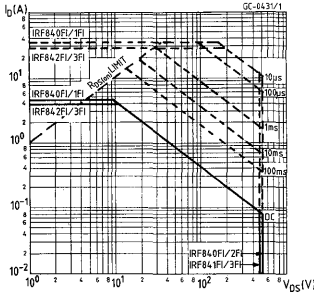
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

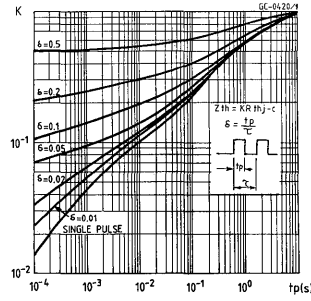


ISOWATT DATA

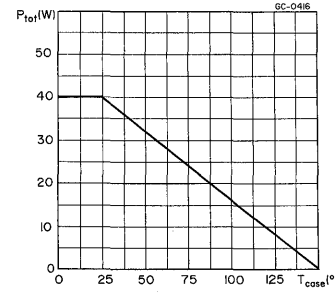
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRFP 150/FI-151/FI
IRFP 152/FI-153/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

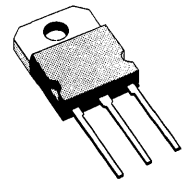
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRFP150	100 V	0.055 Ω	40 A
IRFP150FI	100 V	0.055 Ω	26 A
IRFP151	60 V	0.055 Ω	40 A
IRFP151FI	60 V	0.055 Ω	26 A
IRFP152	100 V	0.08 Ω	34 A
IRFP152FI	100 V	0.08 Ω	21 A
IRFP153	60 V	0.08 Ω	34 A
IRFP153FI	60 V	0.08 Ω	21 A

- 60 - 100 V FOR DC/DC CONVERTERS
- HIGH CURRENT
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE - FOR REDUCES COST AND SIZE

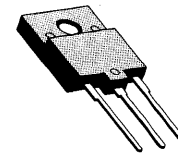
INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regulators, servo control, power audio amplifiers and robotics.

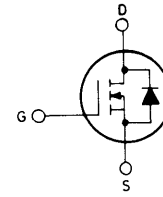


TO-218



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-218 / ISOWATT218	IRFP 150 / 150FI	IRFP 151 / 151FI	IRFP 152 / 152FI	IRFP 153 / 153FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		100	60	100	60	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		100	60	100	60	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		160	160	140	140	A
			150	**151**	**152**	**153**	
I_D	Drain current (cont.) at T_c = 25°C		40	40	34	34	A
I_D	Drain current (cont.) at T_c = 100°C		26	26	22	22	A
			150FI	**151FI**	**152FI**	**153FI**	
I_D ■	Drain current (cont.) at T_c = 25°C		26	26	21	21	A
I_D ■	Drain current (cont.) at T_c = 100°C		16	16	13	13	A
			TO-218		**ISOWATT218**		
P_{tot} ■	Total dissipation at T_c < 25°C		150		65		W
	Derating factor		1.2		0.52		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT218 on this datasheet.
◆ Introduced in 1988 week 44

THERMAL DATA ▪

			TO-218	ISOWATT218	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.83	1.92	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	30		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

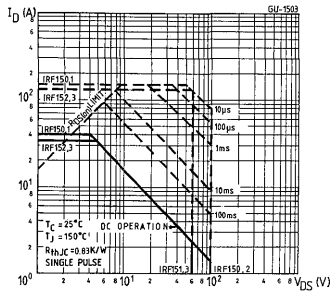
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRFP150/152/150FI/152FI** for **IRFP151/153/151FI/153FI**	 100 60			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRFP150/151/150FI/151FI** for **IRFP152/153/152FI/153FI**	 40 34			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 22 A for **IRFP150/151/150FI/151FI** for **IRFP152/153/152FI/153FI**			 0.055 0.08	 Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **IRFP150/151/150FI/151FI** for **IRFP152/153/152FI/153FI**	 40 34			 A A
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 22 A	13			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 1500 500	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

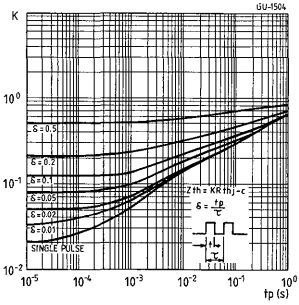
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 24 V I_D = 20 A			35	ns
t_r	Rise time	R_i = 4.7 Ω			100	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)			125	ns
t_f	Fall time				100	ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 50 A V_{DS} = Max Rating × 0.8 (see test circuit)			110	nC
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **IRFP150/151/150FI/151FI**			40	A
		for **IRFP152/153/152FI/153FI**			34	A
I_{SDM} (•)	Source-drain current (pulsed)	for **IRFP150/151/150FI/151FI**			160	A
		for **IRFP152/153/152FI/153FI**			140	A
V_{SD} **	Forward on voltage	I_{SD} = 40 A V_{GS} = 0			2.5	V
t_{rr}	Reverse recovery time	T_j = 150°C		600		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 40 A di/dt = 100 A/μs		3.3		μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

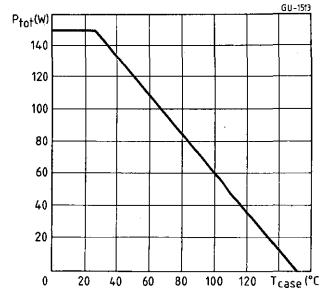
Safe operating areas (standard package)



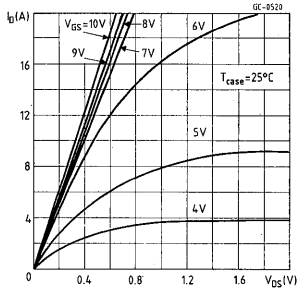
Thermal impedance (standard package)



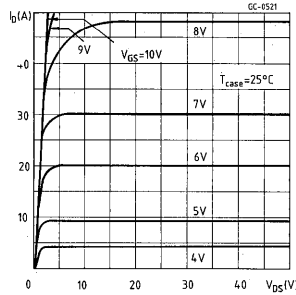
Derating curve (standard package)



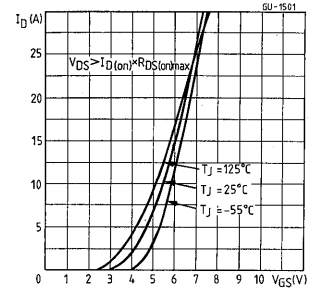
Output characteristics



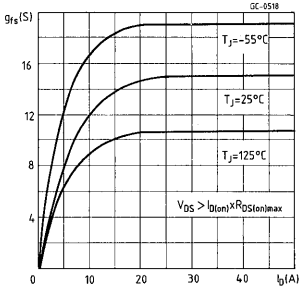
Output characteristics



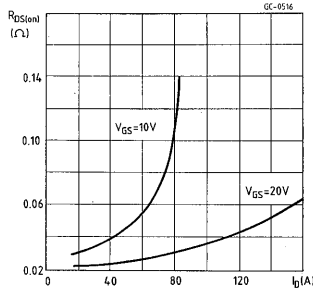
Transfer characteristics



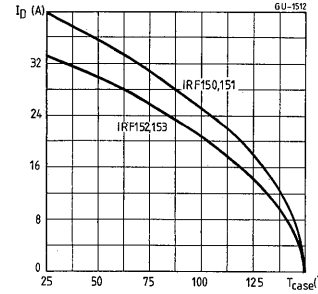
Transconductance



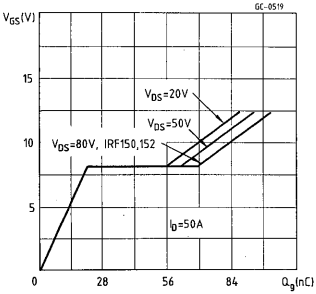
Static drain-source on resistance



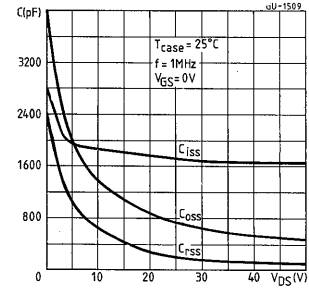
Maximum drain current vs temperature



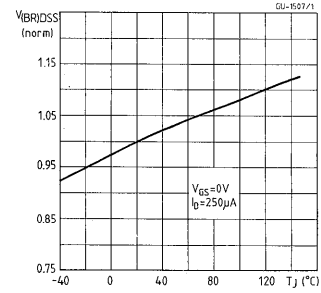
Gate charge vs gate-source voltage



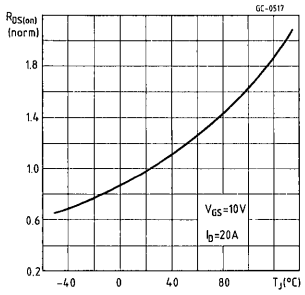
Capacitance variation



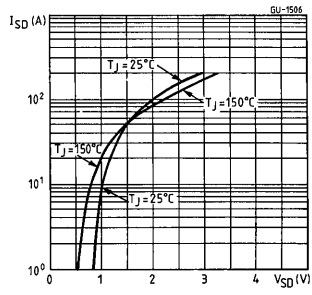
Normalized breakdown voltage vs temperature



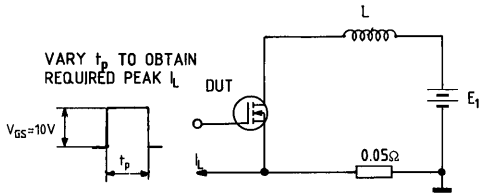
Normalized on resistance vs temperature



Source-drain diode forward characteristics

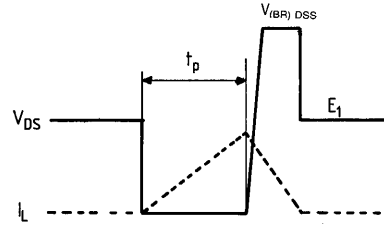


Unclamped inductive test circuit



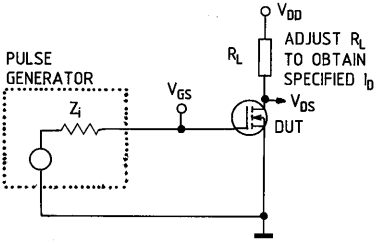
SC-0339

Unclamped inductive waveforms



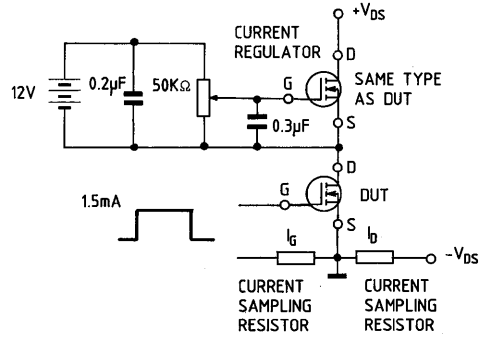
SC-0338

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT218 is fully isolated to 4000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.
The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs.
Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance
ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

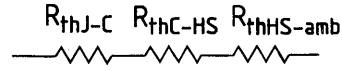
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

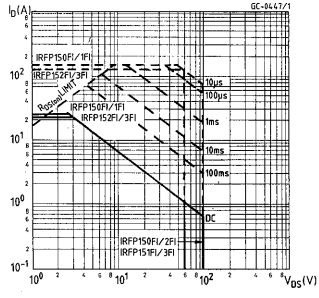
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

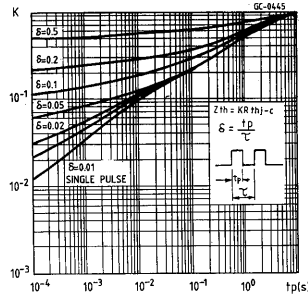


ISOWATT DATA

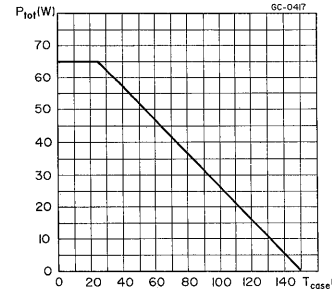
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRFP350FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

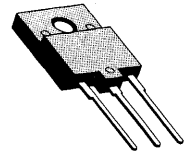
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFP350FI	400 V	0.3 Ω	10 A

- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR SMPS UPTO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - REDUCES SIZE AND COST

INDUSTRIAL APPLICATIONS:

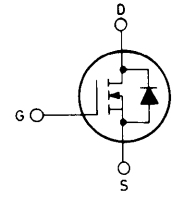
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Fast switching and easy drive make this POWER MOS transistor ideal for high voltage switching applications include electronic welders, switched mode power supplies and sonar equipment.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS} *	Drain-source voltage (V_{GS} = 0)	400	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at T_c = 25°C	10	A
I_D	Drain current (cont.) at T_c = 100°C	6.3	A
I_{DM}(•)	Drain current (pulsed)	60	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)	60	A
P_{tot}	Total dissipation at T_c < 25°C	70	W
	Derating factor	0.56	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C

* T_j = 25°C to 125°C

(•) Repetitive Rating: Pulse width limited by max junction temperature

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.78	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	30	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	/μA /μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D\ (on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$, V_{GS} = 10 V	10			A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 8.0 A			0.3	Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 8.0 A	8.0			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 600 200	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 180 V I_D = 8.0 A R_i = 4.7 Ω (see test circuit)			35 65 150 75	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 18 A V_{DS} = Max Rating × 0.8 (see test circuit)			120	nC

ELECTRICAL CHARACTERISTICS (Continued)

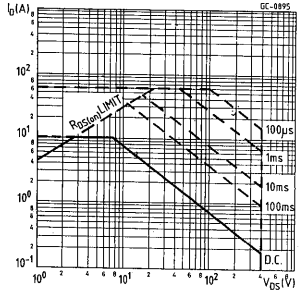
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

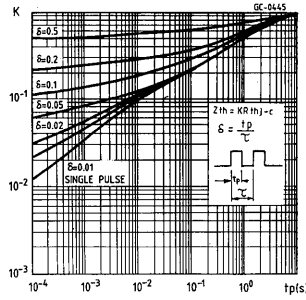
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				10 60	A A
V_{SD}**	Forward on voltage	I_{SD} = 15 A	V_{GS} = 0			1.6	V
t_{rr}	Reverse recovery time	T_j = 150°C			1000		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 15 A	di/dt = 100 A/μs		6.6		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature

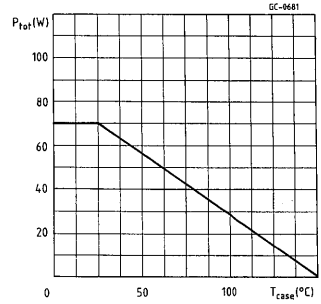
Safe operating areas



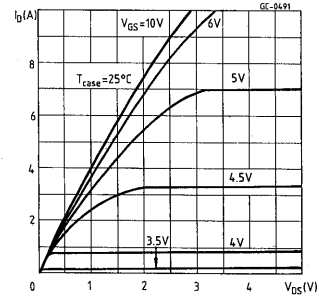
Thermal impedance



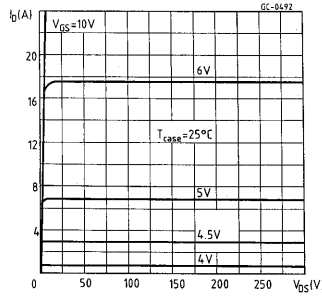
Derating curve



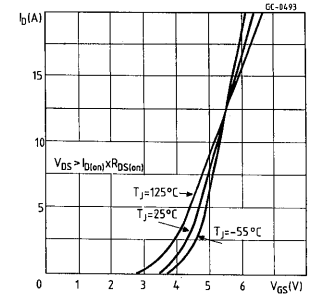
Output characteristics



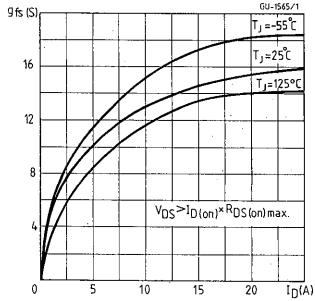
Output characteristics



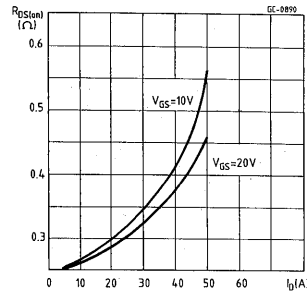
Transfer characteristics



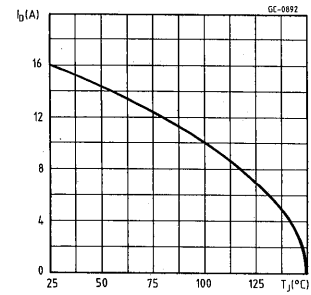
Transconductance



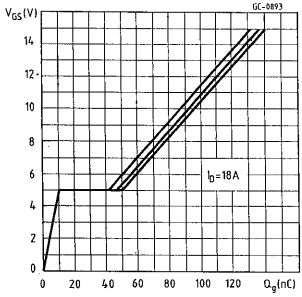
Static drain-source on resistance



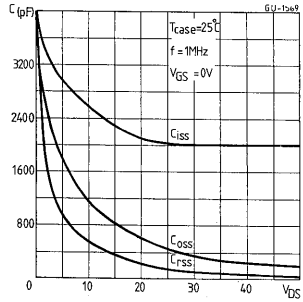
Maximum drain current vs temperature



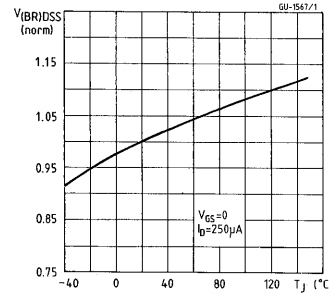
Gate charge vs gate-source voltage



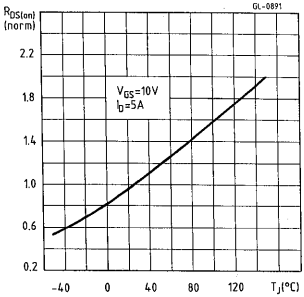
Capacitance variation



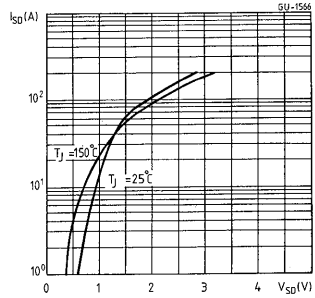
Normalized breakdown voltage vs temperature



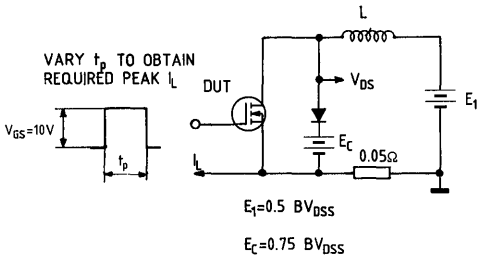
Normalized on resistance vs temperature



Source-drain diode forward characteristics

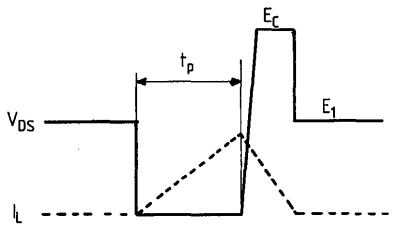


Clamped inductive test circuit



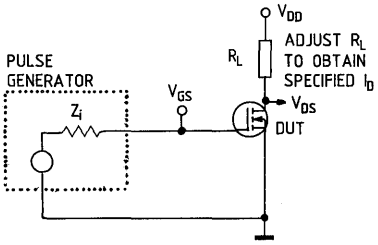
SC-0242

Clamped inductive waveforms



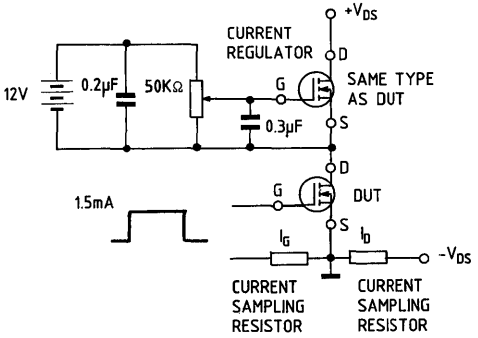
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

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$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

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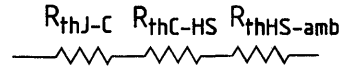
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1



SGS-THOMSON MICROELECTRONICS

IRFP 450/FI-451/FI
IRFP 452/FI-453/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

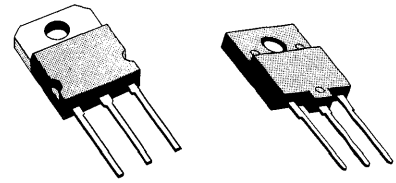
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
IRFP450	500 V	0.4 Ω	14 A
IRFP450FI	500 V	0.4 Ω	9 A
IRFP451	450 V	0.4 Ω	14 A
IRFP451FI	450 V	0.4 Ω	9 A
IRFP452	500 V	0.5 Ω	12 A
IRFP452FI	500 V	0.5 Ω	8 A
IRFP453	450 V	0.5 Ω	12 A
IRFP453FI	450 V	0.5 Ω	8 A

- HIGH VOLTAGE - 450V FOR OFF LINE SMPS
- HIGH CURRENT - 12A FOR UP TO 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100 KHz
- EASY DRIVE - REDUCES COST AND SIZE

INDUSTRIAL APPLICATIONS:

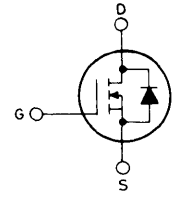
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications.



TO-218 **ISOWATT218**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-218 / ISOWATT218	IRFP 450 / 450FI	IRFP 451 / 451FI	IRFP 452 / 452FI	IRFP 453 / 453FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)		500	450	500	450	V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)		500	450	500	450	V
V_{GS}	Gate-source voltage		±20				V
I_{DM} (•)	Drain current (pulsed)		56	56	48	48	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)		56	56	48	48	A
			450	451	452	453	
I_D	Drain current (cont.) at T_c = 25°C		14	14	12	12	A
I_D	Drain current (cont.) at T_c = 100°C		8.8	8.8	7.9	7.9	A
			450FI	451FI	452FI	453FI	
I_D ■	Drain current (cont.) at T_c = 25°C		9	9	8	8	A
I_D ■	Drain current (cont.) at T_c = 100°C		5.6	5.6	5	5	A
			TO-218		ISOWATT218		
P_{tot} ■	Total dissipation at T_c < 25°C		180		70		W
	Derating factor		1.44		0.55		W/°C
T_{stg}	Storage temperature		−55 to 150				°C
T_j	Max. operating junction temperature		150				°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature.
■ See note on ISOWATT218 on this datasheet.

THERMAL DATA ▪

			TO-218	ISOWATT218	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.69	1.8	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.1		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	30		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

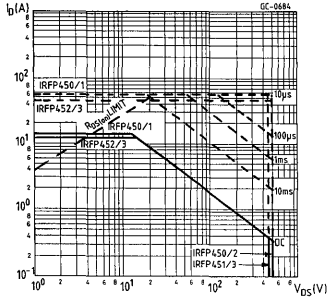
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **IRFP450/452/450FI/452FI** for **IRFP451/453/451FI/453FI**	 500 450			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRFP450/451/450FI/451FI** for **IRFP452/453/452FI/453FI**	 14 12			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 7.9 A for **IRFP450/451/450FI/451FI** for **IRFP452/453/452FI/453FI**			 0.4 0.5	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 7.9 A	9.3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 600 200	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 210 V I_D = 7.0 A R_i = 4.7 Ω (see test circuit)			35 50 150 70	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 13 A V_{DS} = Max Rating × 0.8 (see test circuit)			120	nC

ELECTRICAL CHARACTERISTICS (Continued)

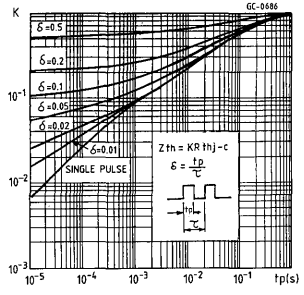
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				14 56	A A
V_{SD} Forward on voltage	I_{SD} = 14 A V_{GS} = 0			1.4	V
t_{rr} Reverse recovery time Q_{rr} Reverse recovered charge	T_j = 150°C I_{SD} = 14 A di/dt = 100 A/μs		1300 7.4		ns μC

** Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT218 in this datasheet.

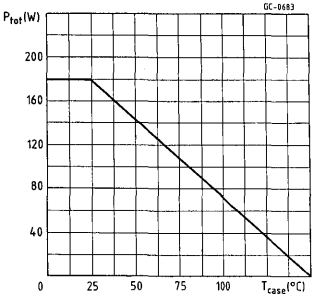
Safe operating areas (standard package)



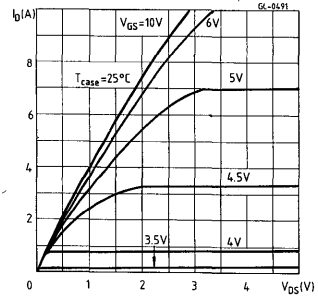
Thermal impedance (standard package)



Derating curve (standard package)



Output characteristics



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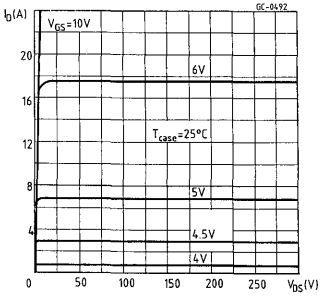
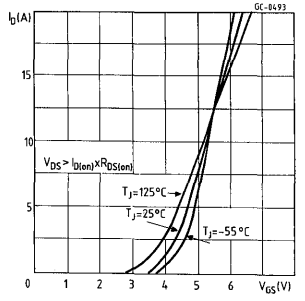
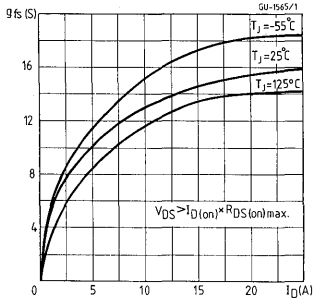


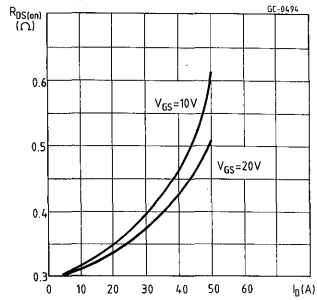
Transfer characteristics



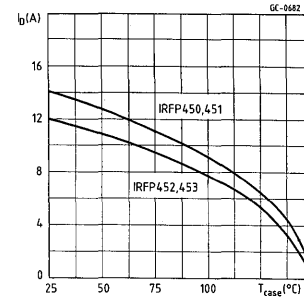
Transconductance



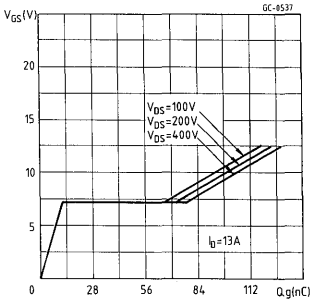
Static drain-source on resistance



Maximum drain current vs temperature



Gate charge vs gate-source voltage



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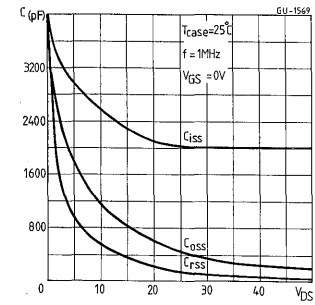

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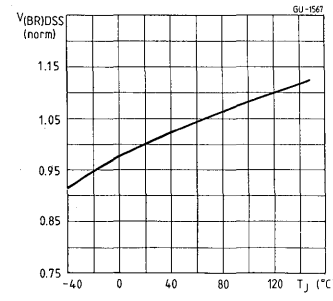
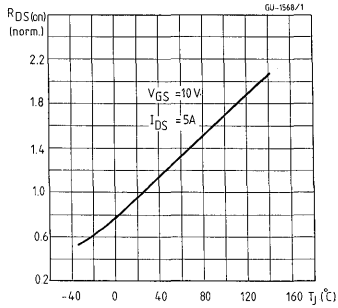


Normalized on resistance vs temperature



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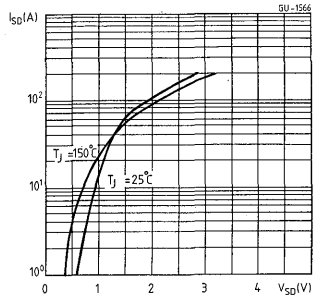

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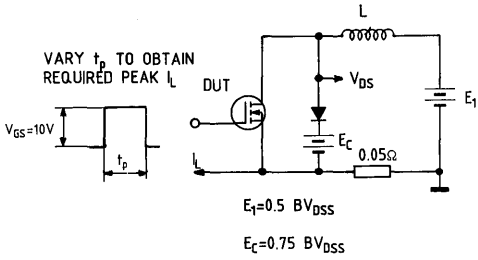
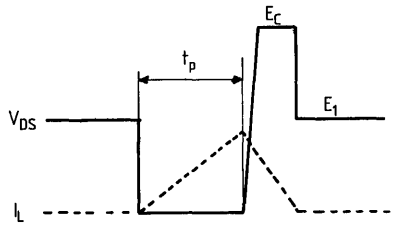


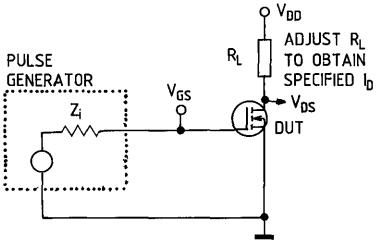
SC-0242

Clamped inductive waveforms



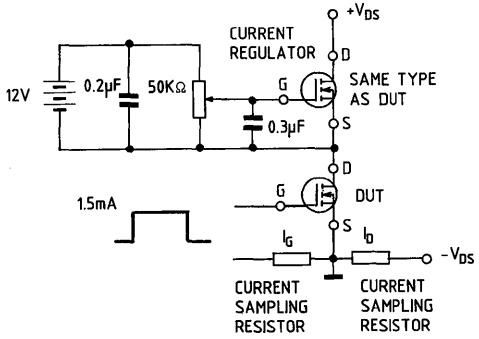
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

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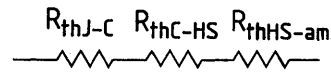
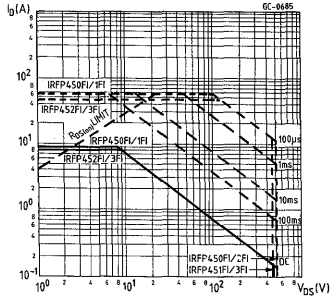
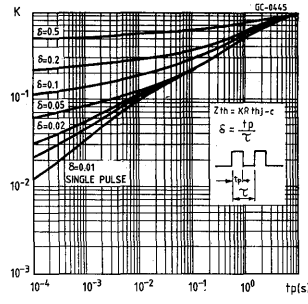


ISOWATT DATA

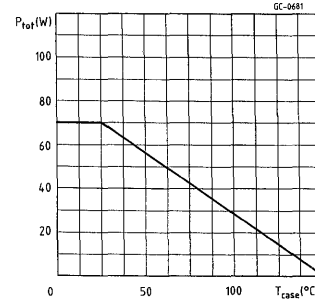
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRFZ20/FI
IRFZ22/FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

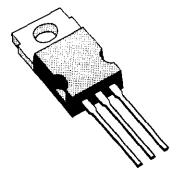
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFZ20	50 V	0.1 Ω	15 A
IRFZ20FI	50 V	0.1 Ω	12.5 A
IRFZ22	50 V	0.12 Ω	14 A
IRFZ20FI	50 V	0.12 Ω	12 A

- N-CHANNEL POWER MOS TRANSISTORS
- VERY LOW $R_{DS\ (on)}$
- LOW DRIVE ENERGY FOR EASY DRIVE
- COST EFFECTIVE

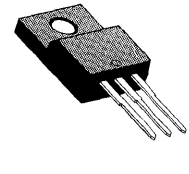
INDUSTRIAL APPLICATIONS:

- AUTOMOTIVE POWER ACTUATORS
- MOTOR CONTROLS
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits applications such as power actuators driving, motor drive including brushless motors, hydraulic actuator and many other in automotive and automatic guided vehicle applications. They also find use DC/DC converters and uninterruptible power supplies

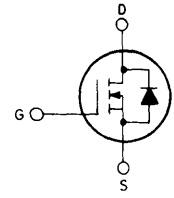


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		IRF Z20 Z20FI	IRF Z22 Z22FI	
V_{DS} *	Drain-source voltage (V_{GS} = 0)	50		V
V_{DGR} *	Drain-gate voltage (R_{GS} = 20 KΩ)	50		V
V_{GS}	Gate-source voltage	± 20		V
I_{DM} (•)	Drain current (pulsed)	60	56	A
I_{DLM}	Drain inductive current, clamped (L = 100 μH)	60	56	A
		Z20	**Z22**	
I_D	Drain current (cont.) at T_c = 25°C	15	14	A
I_D	Drain current (cont.) at T_c = 100°C	10	9	A
		Z20FI	**Z22FI**	
I_D ■	Drain current (cont.) at T_c = 25°C	12.5	12	A
I_D ■	Drain current (cont.) at T_c = 100°C	7.5	7	A
		TO-220	**ISOWATT220**	
P_{tot} ■	Total dissipation at T_c < 25°C	40	30	W
■	Derating factor	0.32	0.24	W/°C
T_{stg}	Storage temperature	− 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature
■ See note on ISOWATT220 in this datasheet

THERMAL DATA ▪

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80		°C/W
T_l	Maximum lead temperature for soldering purpose		300		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ x $R_{DS(on)\ max}$ V_{GS} = 10 V for **IRFZ20/IRFZ20FI** for **IRFZ22/IRFZ22FI**	 15 14			 A A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 9.0 A for **IRFZ20/IRFZ20FI** for **IRFZ20/IRFZ22FI**			 0.10 0.12	 Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ x $R_{DS\ (on)\ max}$ I_D = 9.0 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			850 350 100	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 9.0 A R_i = 50 Ω (see test circuit)			30 90 40 30	ns ns ns ns
Q_g	Total Gate Charge	V_{GS} = 10 V I_D = 20 A V_{DS} = Max Rating x 0.8 (see test circuit)			17	nC

ELECTRICAL CHARACTERISTICS (Continued)

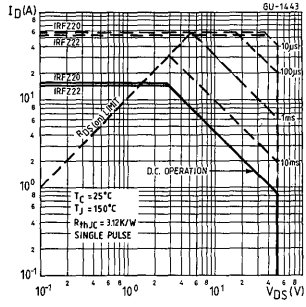
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current	for **IRFZ20/IRFZ20FI**			15	ns
	for **IRFZ22/IRFZ22FI**			14	ns
I_{SDM} (•) Source-drain current (pulsed)	for **IRFZ20/IRFZ20FI**			60	A
	for **IRFZ22/IRFZ22FI**			56	A
V_{SD} ** Forward on voltage	V_{GS} = 0				
	for **IRFZ20/IRFZ20FI** I_{SD} = 15 A			1.5	V
	for **IRFZ22/IRFZ22IF** I_{SD} = 14 A			1.4	V
t_{rr} Reverse recovery time	T_j = 150°C		100		ns
Q_{rr} Reverse recovered charge	I_{SD} = 15 A di/dt = 100 A/μs		0.4		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 1.5%

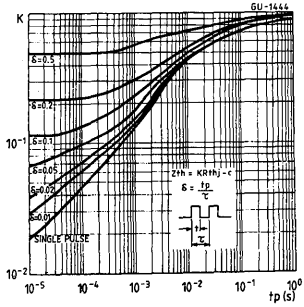
(•) Repetitive Rating: Pulse width limited by max junction temperature

■ See note on ISOWATT220 in this datasheet

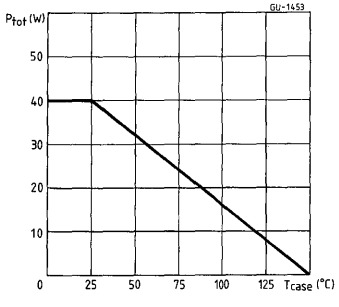
Safe operating areas (standard package)



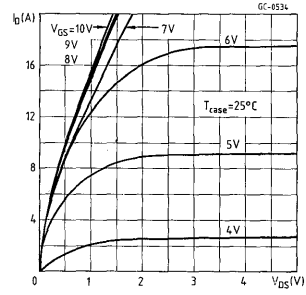
Thermal impedance (standard package)



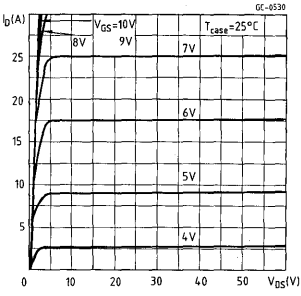
Derating curve (standard package)



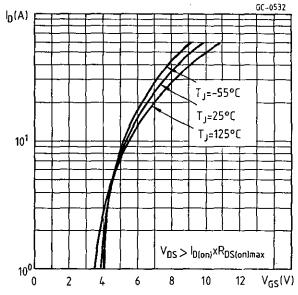
Output characteristics



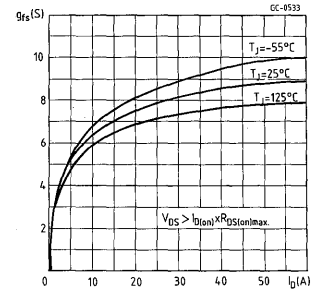
Output characteristics



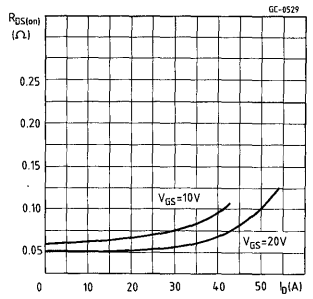
Transfer characteristics



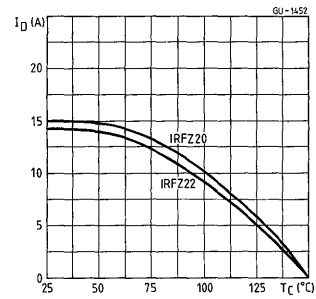
Transconductance



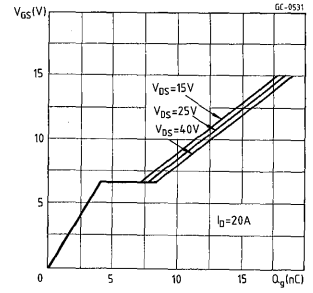
Static drain-source on resistance



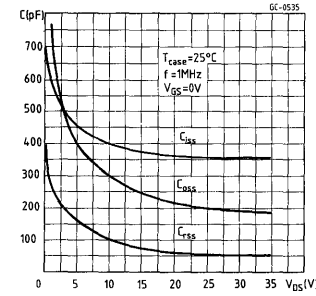
Maximum drain current vs temperature



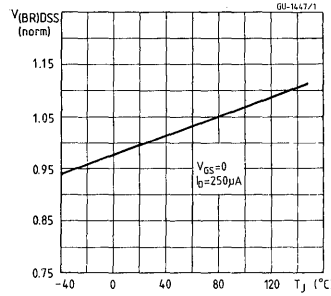
Gate charge vs gate-source voltage



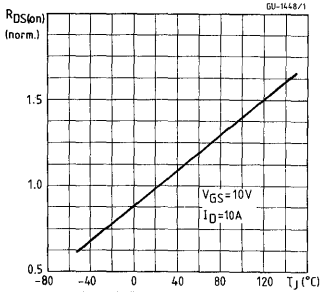
Capacitance variation



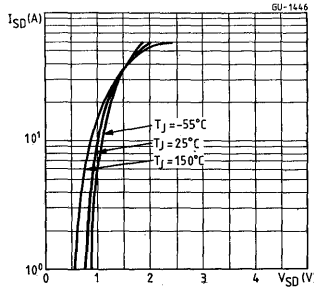
Normalized breakdown voltage vs temperature



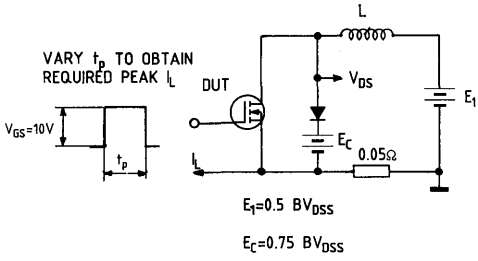
Normalized on resistance vs temperature



Source-drain diode forward characteristics

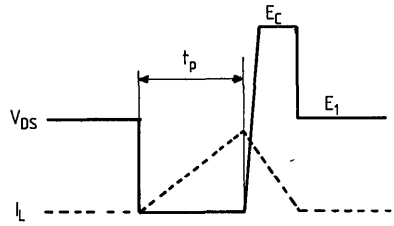


Clamped inductive test circuit



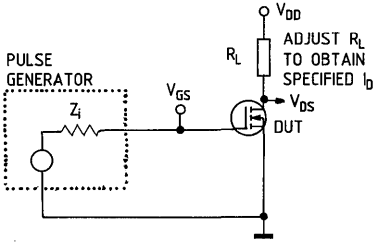
SC-0242

Clamped inductive waveforms



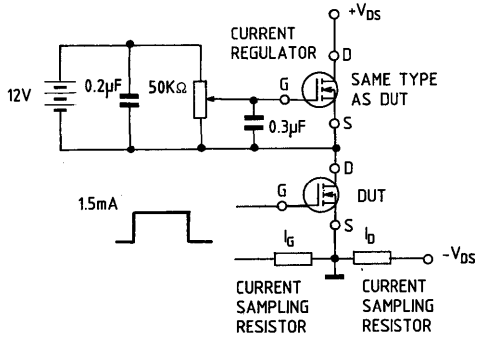
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

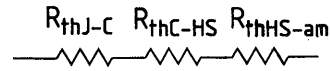
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

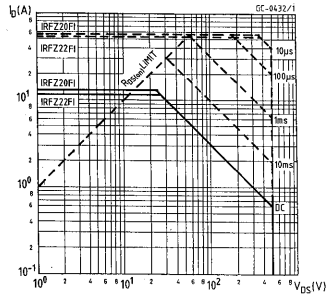
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

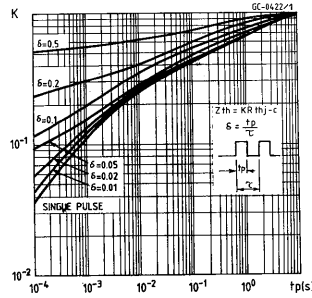


ISOWATT DATA

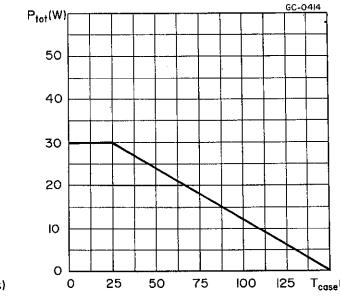
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

IRFZ40
IRFZ42

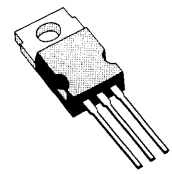
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFZ40	50 V	0.028 Ω	35 A
IRFZ42	50 V	0.035 Ω	35 A

- VERY LOW $R_{DS\ (on)}$
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE /C_{rss} RATIO

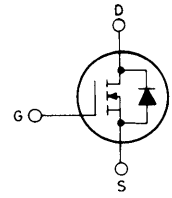
INDUSTRIAL APPLICATIONS:

- AUTOMOTIVE POWER ACTUATORS
- MOTOR CONTROLS
- INVERTERS



TO-220

INTERNAL SCHEMATIC DIAGRAM



N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits applications such as power actuators driving, motor drive including brushless motor, hydraulic actuators and many other in automotive and automatic guided vehicle applications. They also find use DC/DC converters and uninterruptible power supplies

ABSOLUTE MAXIMUM RATINGS		IRFZ40	IRFZ42	
V_{DS} *	Drain-source voltage ($V_{GS}=0$)	50		V
V_{DGR} *	Drain-gate voltage ($R_{GS}=20$ KΩ)	50		V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	35	35	A
I_D	Drain current (cont.) at $T_c=100°C$	32	29	A
I_{DM}(•)	Drain current (pulsed)	160	145	A
I_{DLM}	Drain inductive current, clamped (L= 100 μH)	160	145	A
P_{tot}	Total dissipation at $T_c<25°C$	125		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−55 to 150		°C
T_j	Max. operating junction temperature	150		°C

* T_j = 25°C to 125°C
(•) Repetitive Rating: Pulse width limited by max junction temperature

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.0	°C/W
$R_{thc\text{-}s}$	Thermal resistance case-sink	typ	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W
T_l	Maximum lead temperature for soldering purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

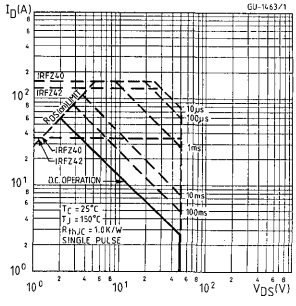
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON **						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$I_{D(on)}$	On-state drain current	V_{DS} > $I_{D\ (on)}$ × $R_{DS(on)\ max}$ V_{GS} = 10 V	35			A
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 29 A for **IRFZ40** for **IRFZ42**			0.028 0.035	Ω Ω
DYNAMIC						
g_{fs} **	Forward transconductance	V_{DS} > $I_{D\ (on)}$ × $R_{DS\ (on)\ max}$ I_D = 29 A	17			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			3000 1200 400	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 29 A Z_i = 4.7 Ω (see test circuit)			25 60 70 25	ns ns ns ns
Q_g	Total gate charge	V_{GS} = 10 V I_D = 64 A V_{DS} = Max Rating × 0.8 (see test circuit)			60	nC

ELECTRICAL CHARACTERISTICS (Continued)

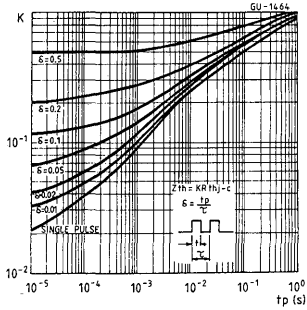
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current				35	A
I_{SDM} (•) Source-drain current (pulsed)	for **IRFZ40**			160	A
	for **IRFZ42**			145	A
V_{SD} ** Forward on voltage	V_{GS} = 0				
	for **IRFZ40** I_{SD} = 51 A			2.5	V
	for **IRFZ42** I_{SD} = 46 A			2.2	V
t_{rr} Reverse recovery time	T_j = 150°C		350		ns
Q_{rr} Reverse recovered charge	I_{SD} = 51 A di/dt = 100 A/μs		2.1		μC

** Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 1.5%
(•) Repetitive Rating: Pulse width limited by max junction temperature

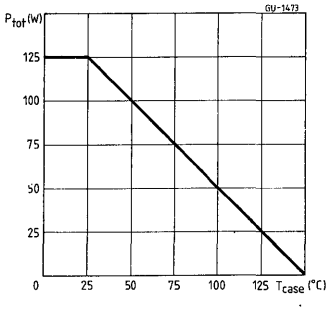
Safe operating areas



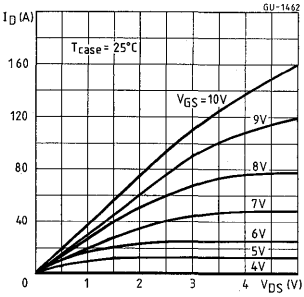
Thermal impedance



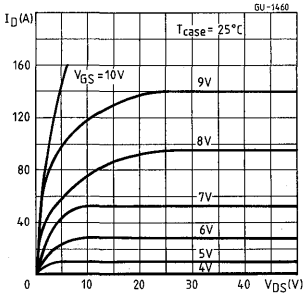
Derating curve



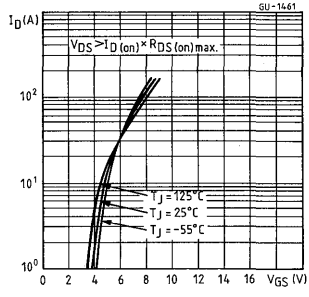
Output characteristics



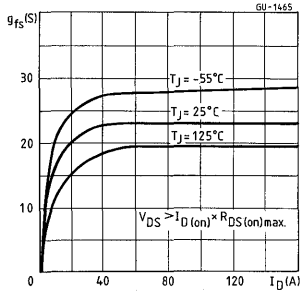
Output characteristics



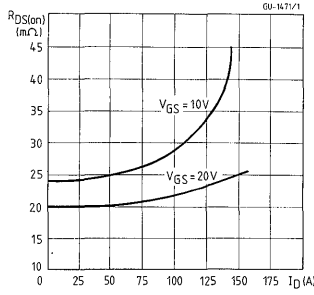
Transfer characteristics



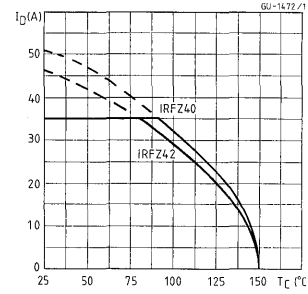
Transconductance



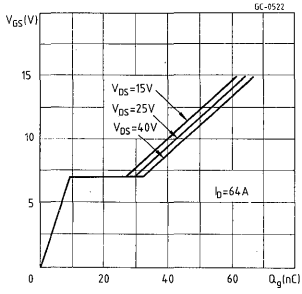
Static drain-source on resistance



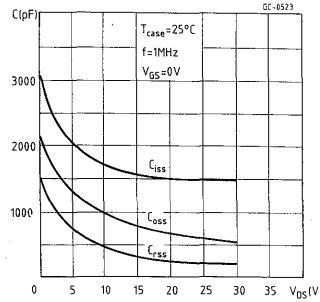
Maximum drain current vs temperature



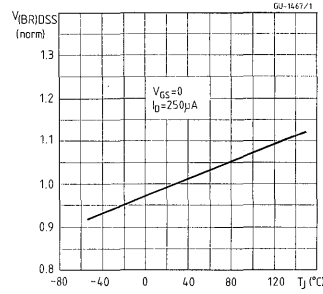
Gate charge vs gate-source voltage



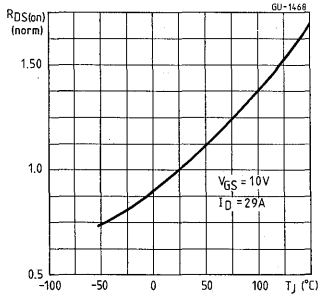
Capacitance variation



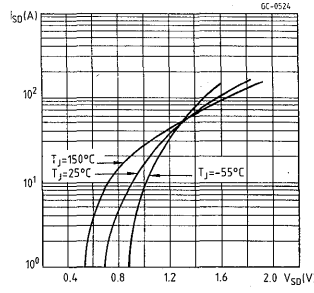
Normalized breakdown voltage vs temperature



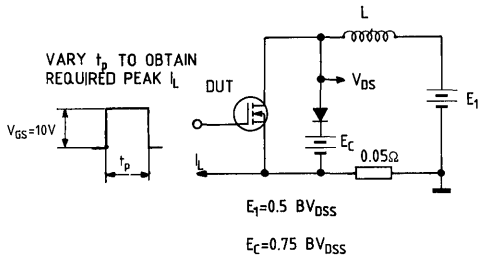
Normalized on resistance vs temperature



Source-drain diode forward characteristics

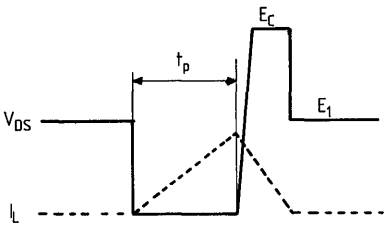


Clamped inductive test circuit



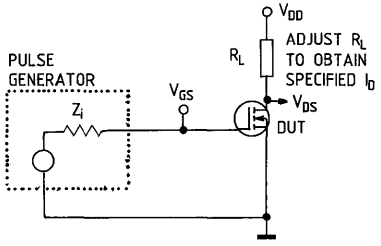
SC-0242

Clamped inductive waveforms



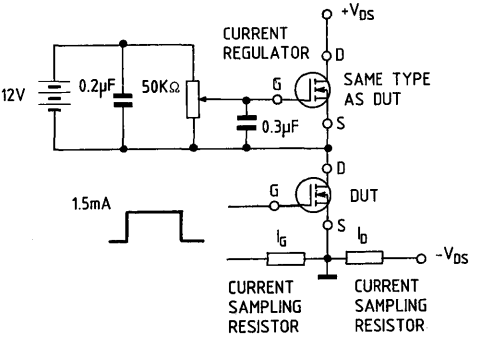
SC-0243

Switching times test circuit



SC-0246

Gate charge test circuit



SC-0244

SGS-THOMSON MICROELECTRONICS

MTH6N60FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

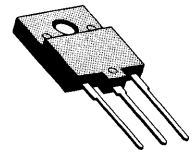
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTH6N60FI	600 V	1.2 Ω	3.5 A

- HIGH VOLTAGE - 600 V FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING TIMES FOR OPERATIONS AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

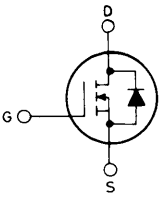
- SWITCHING POWER SUPPLY
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS ideal for very high speed switching applications. Typical uses include SMPS, uninterruptible power supplies and motor controls.



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	600	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	3.5	A
I_{DM}	Drain current (pulsed)	14	A
P_{tot}	Total dissipation at $T_c < 25°C$	40	W
	Derating factor	0.32	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	°C/W

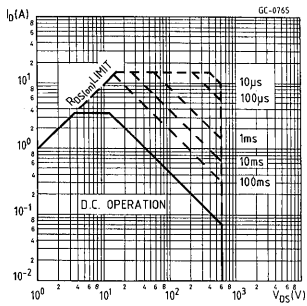
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			200 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3 A			1.2	Ω
$V_{DS(on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 6 A V_{GS} = 10 V I_D = 3 A T_c = 100°C			8 7.2	V V
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 10 V I_D = 3 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1800 350 150	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 3 A R_i = 50 Ω V_i = 10 V			60 150 200 120	ns ns ns ns

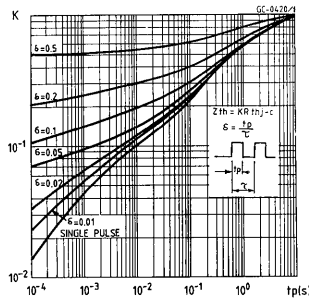
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} Source-drain current (pulsed)				3.5 14	A A
V_{SD} Forward on voltage	I_{SD} = 6 A V_{GS} = 0		1.3		V
t_{rr} Reverse recovery time	I_{SD} = 6 A di/dt = 100A/μs		600		ns

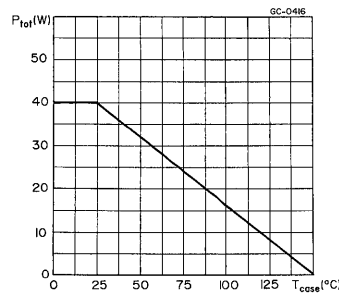
Safe operating areas



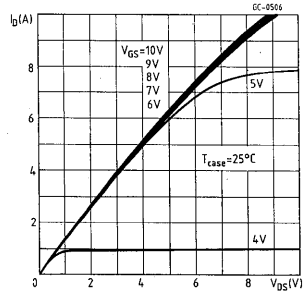
Thermal impedance



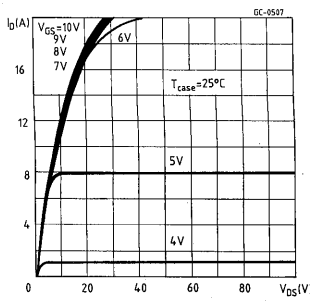
Derating curve



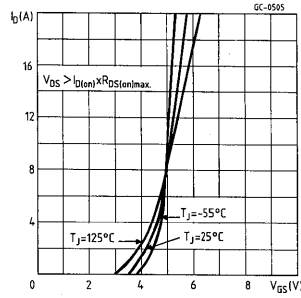
Output characteristics



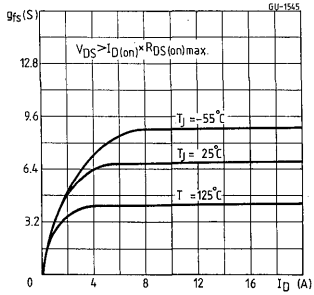
Output characteristics



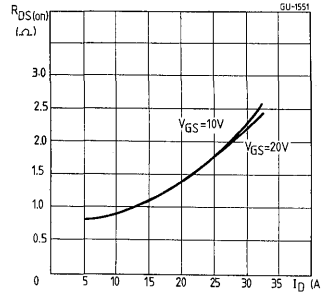
Transfer characteristics



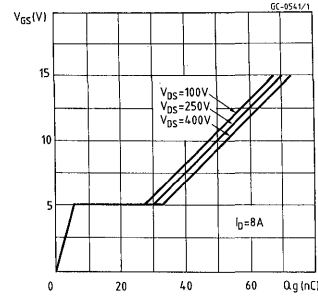
Transconductance



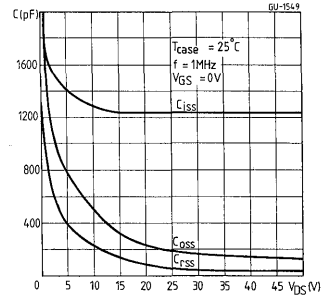
Static drain-source on resistance



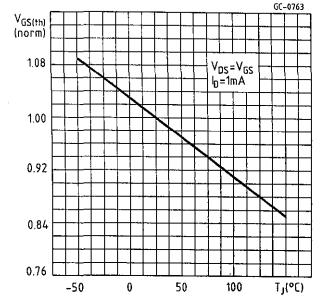
Gate charge vs gate-source voltage



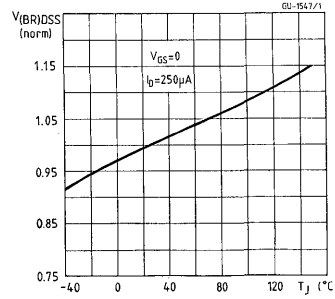
Capacitance variation



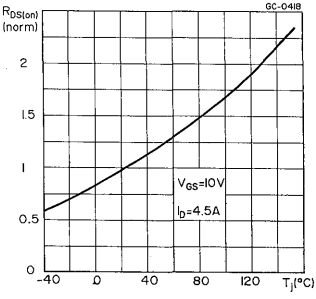
Normalized gate threshold voltage vs temperature



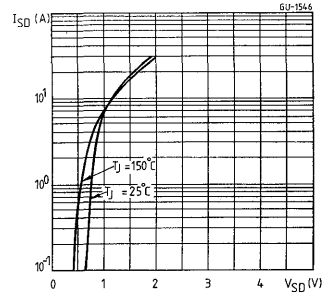
Normalized breakdown voltage vs temperature



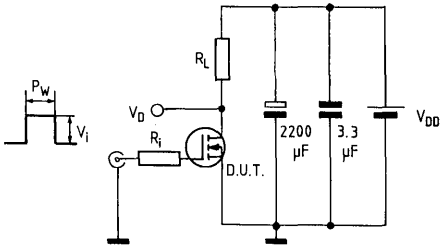
Normalized on resistance vs temperature



Source-drain diode forward characteristics

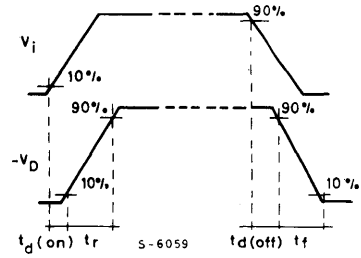


Switching times test circuit for resistive load

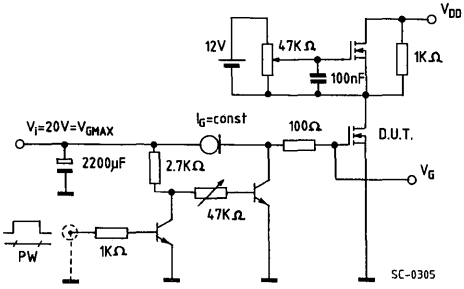


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

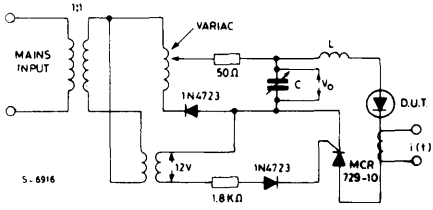


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT218 is fully isolated to 4000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. These distances are in agreement with VDE and UL creepage and clearance standards. The ISOWATT218 package eliminates the need for external isolation so reducing fixing hardware.
The package is supplied with leads longer than the standard TO-218 to allow easy mounting on pcbs.
Accurate moulding techniques used in manufacture assures consistent heat spreader-to-heatsink capacitance
ISOWATT218 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT218 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT218 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT218 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

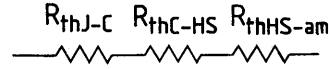
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1



SGS-THOMSON MICROELECTRONICS

MTH40N06
MTH40N06FI

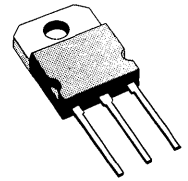
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTH40N06	60 V	0.028 Ω	40 A
MTH40N06FI	60 V	0.028 Ω	26 A

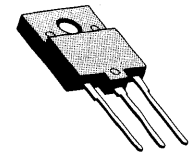
- VERY LOW ON-LOSSES
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- LOW DRIVE ENERGY FOR EASY DRIVE
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO

AUTOMOTIVE POWER APPLICATIONS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuit in applications such as power actuator driving, motor drive including brushless motors, hydraulic actuators and many other uses in automotive applications.
They also find use in DC/DC converters and uninterruptible power supplies.

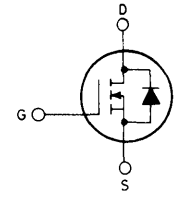


TO-218



ISOWATT218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-218 / ISOWATT218	MTH40N06 / MTH40N06FI	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	V
V_{DGR}	Drain-gate voltage ($R_{GS}=$ 1 MΩ)		60	V
V_{GS}	Gate-source voltage		±20	V
I_{DM}	Drain current (pulsed)		140	A
		TO-218	**ISOWATT218**	
I_D ■	Drain current (cont.) $T_c=$ 20°C	40	26	A
P_{tot} ■	Total dissipation at T_c <25°C	150	65	W
■	Derating factor	1.2	0.52	W/°C
T_{stg}	Storage temperature		−65 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT218 in this datasheet
◆ Introduced in 1988 week 44

THERMAL DATA ■

			TO-218	ISOWATT218	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.83	1.92	°C/W
T_l	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 100 μA V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating × 0.85 V_{DS} = Max Rating × 0.85 T_c = 100°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON *						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A			0.028	Ω
$V_{DS\ (on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 40 A V_{GS} = 10 V I_D = 20 A T_c = 100°C			1.4 1.12	V V
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	40			A
DYNAMIC						
g_{fs}*	Forward transconductance	V_{DS} = 15 V I_D = 20 A	10			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			5000 2500 1000	pF pF pF
Q_g	Total gate charge	V_{DS} = 50 V I_D = 40 A V_{GS} = 10 V			120	nC

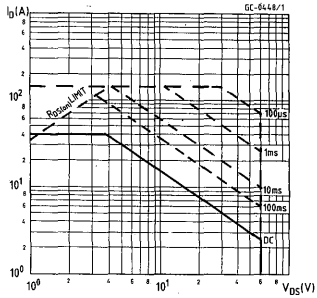
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SWITCHING							
$t_{d\ (on)}$	Turn-on time	V_{DD} = 25 V	I_D = 20 A			50	ns
t_r	Rise time	R_{gen} = 50 Ω				300	ns
$t_{d\ (off)}$	Turn-off delay time					150	ns
t_f	Fall time					100	ns
SOURCE DRAIN DIODE							
V_{SD}	Forward on voltage	I_{SD} = 40 A	V_{GS} = 0			3	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A	V_{GS} = 0		200		ns
t_{on}	Forward turn-on time				150		ns

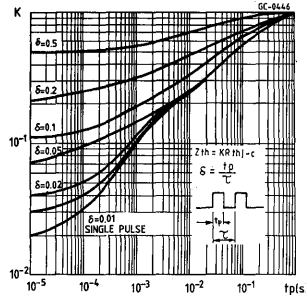
* Pulsed: Pulse duration ⩽ 300 μs, duty cycle ⩽ 2%

■ See note on ISOWATT218 in this datasheet

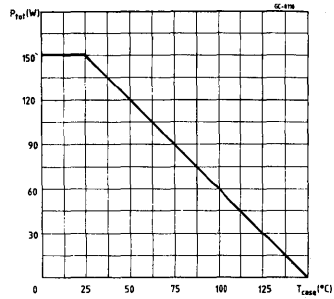
Safe operating areas (standard package)



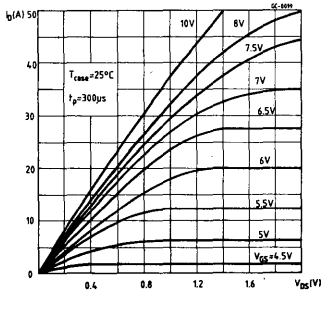
Thermal impedance (standard package)



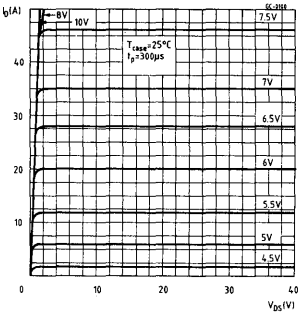
Derating curve (standard package)



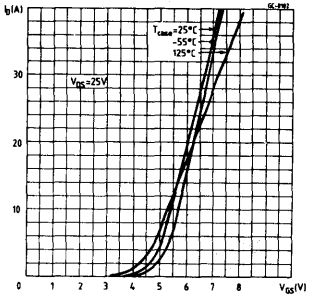
Output characteristics



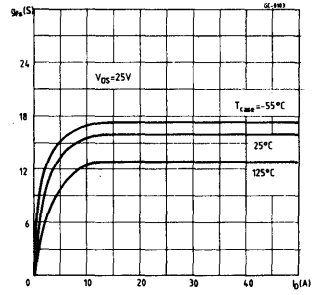
Output characteristics



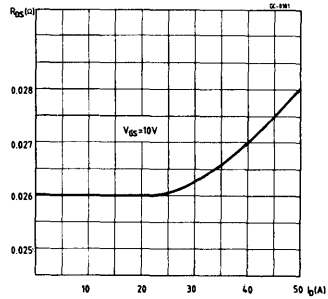
Transfer characteristics



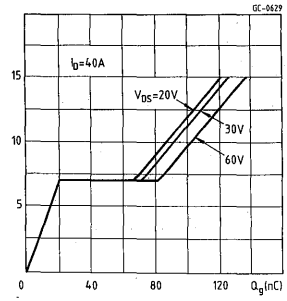
Transconductance



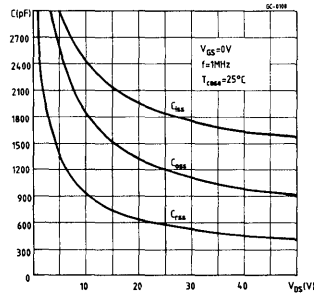
Static drain-source on resistance



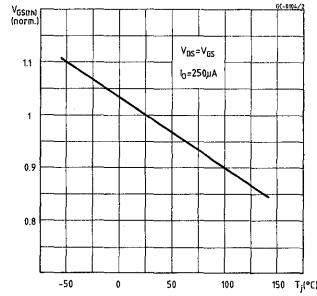
Gate charge vs gate-source voltage



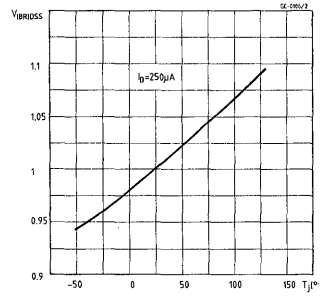
Capacitance variation



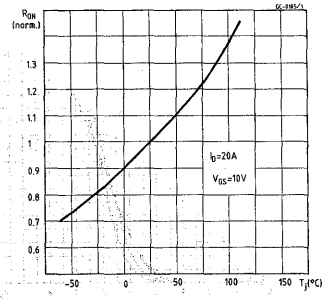
Normalized gate threshold voltage vs temperature



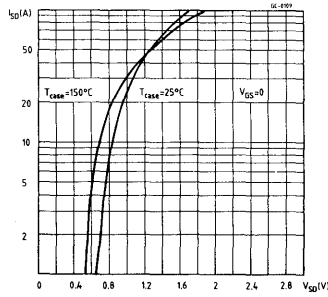
Normalized breakdown voltage vs temperature



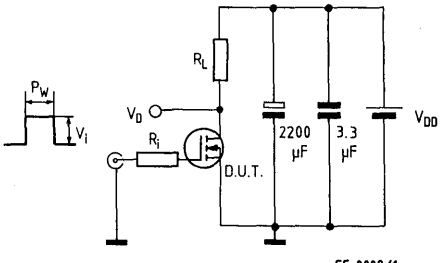
Normalized on resistance vs temperature



Source-drain diode forward characteristics

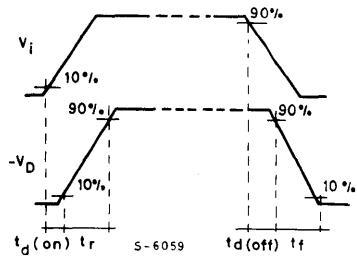


Switching times test circuit for resistive load

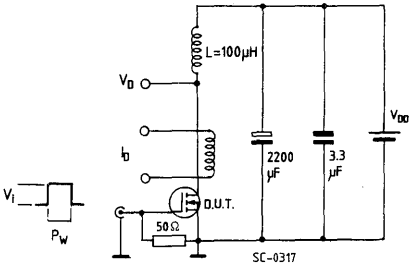


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

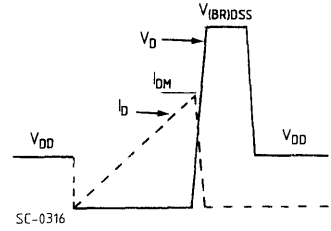


Unclamped inductive load test circuit

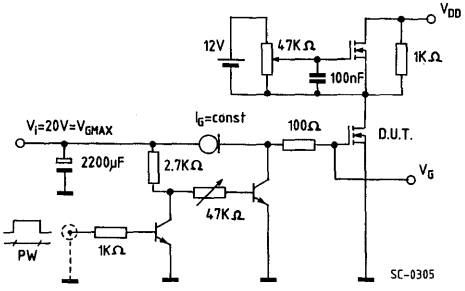


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

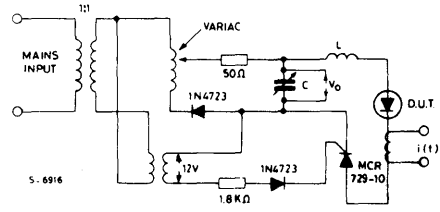


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT218 PACKAGE CHARACTERISTICS AND APPLICATION.

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$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

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2 - for an intermediate power pulse of 5ms to 50ms:

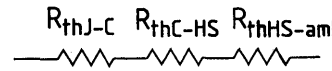
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

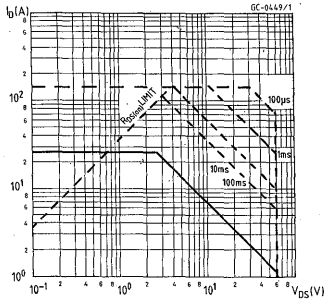
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

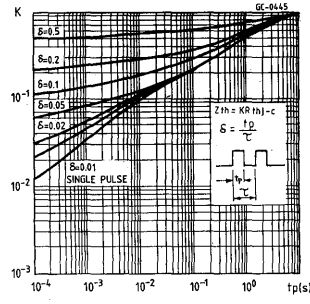


ISOWATT DATA

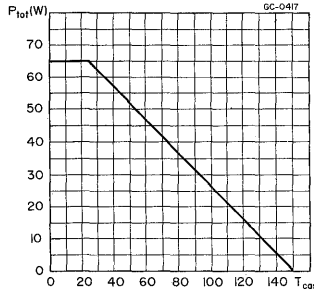
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

MTP3N60
MTP3N60FI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

PRELIMINARY DATA

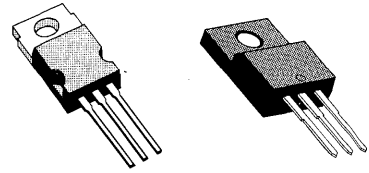
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTP3N60	600 V	2.5 Ω	3 A
MTP3N60FI	600 V	2.5 Ω	2.5 A

- HIGH VOLTAGE FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING TIMES FOR OPERATION AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS

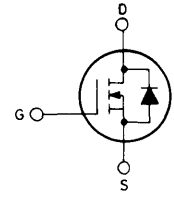
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and fast switching times make these POWER MOS ideal for very high speed switching applications. Typical uses include SMPS and uninterruptible power supplies.



TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	600		V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	600		V
V_{GS}	Gate-source voltage	±20		V
		TO-220	**ISOWATT220**	
I_D	Drain current (cont.) at T_c = 25°C	3	2.5	A
I_{DM}	Drain current (pulsed)	10	10	A
P_{tot}	Total dissipation at T_c < 25°C	75	35	W
	Derating factor	0.6	0.28	W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	3.57	°C/W
$R_{thj\text{ - }amb}$	Thermal resistance junction-ambient	max	62.5		°C/W

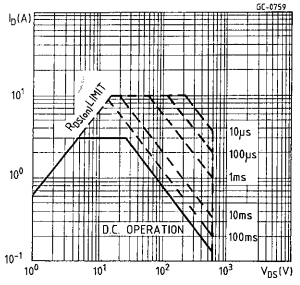
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			200 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.5 A			2.5	Ω
$V_{DS(on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 3 A V_{GS} = 10 V I_D = 1.5 A T_c = 100°C			9 7.5	V V
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 15 V I_D = 1.5 A	1.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1000 300 80	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 1.5 A R_i = 50 Ω V_i = 10 V			50 100 180 80	ns ns ns ns

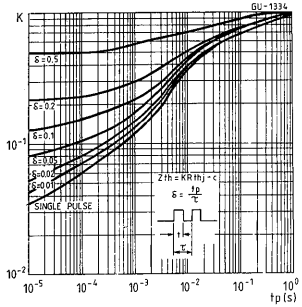
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					3 10	A A
V_{SD}	Forward on voltage	I_{SD} = 3 A	V_{GS} = 0		1.1		V
t_{rr}	Reverse recovery time	I_{SD} = 3 A	di/dt = 100A/μs		165		ns

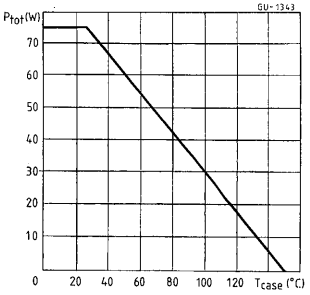
Safe operating areas (standard package)



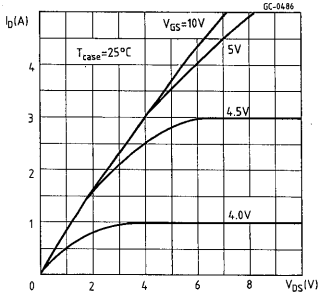
Thermal impedance (standard package)



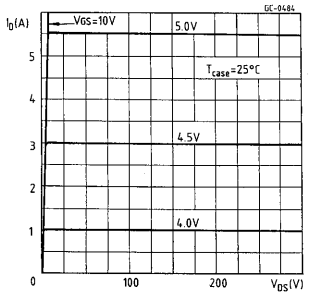
Derating curve (standard package)



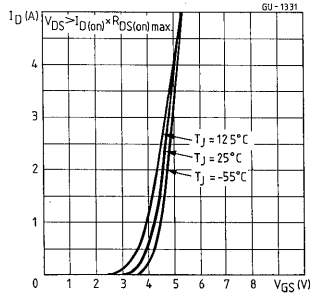
Output characteristics



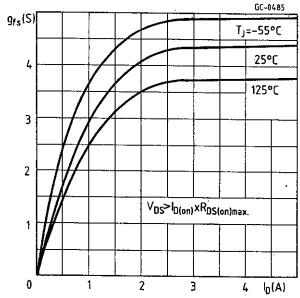
Output characteristics



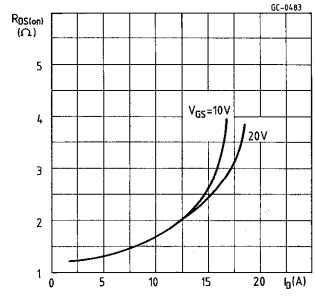
Transfer characteristics



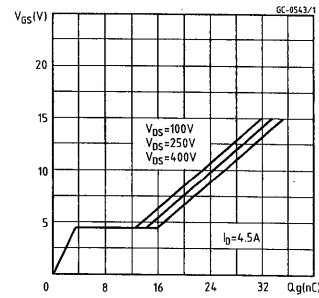
Transconductance



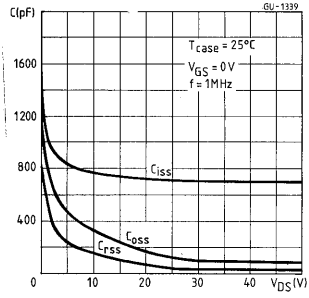
Static drain-source on resistance



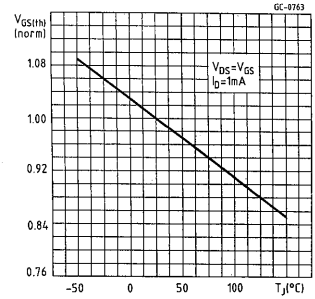
Gate charge vs gate-source voltage



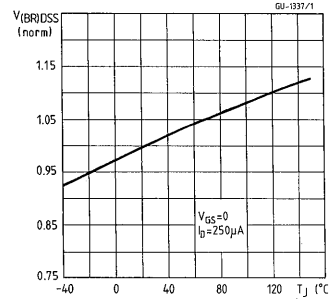
Capacitance variation



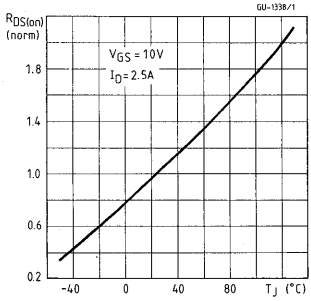
Normalized gate threshold voltage vs temperature



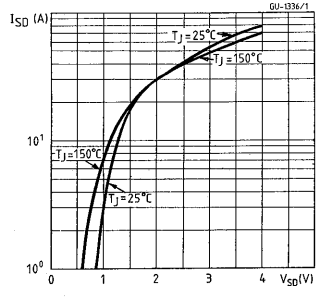
Normalized breakdown voltage vs temperature



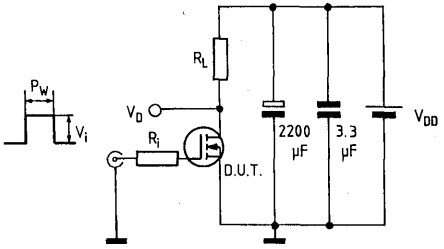
Normalized on resistance vs temperature



Source-drain diode forward characteristics

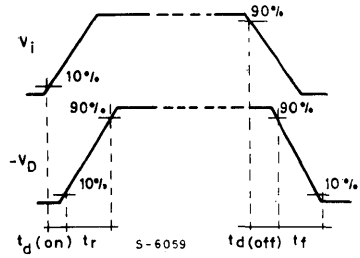


Switching times test circuit for resistive load

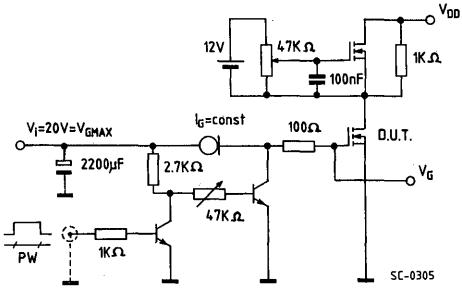


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

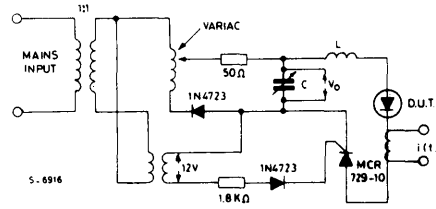


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

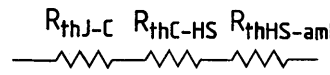
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

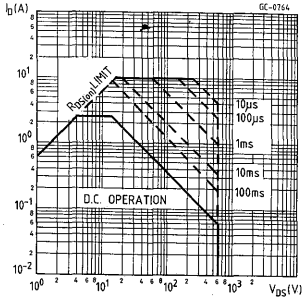
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

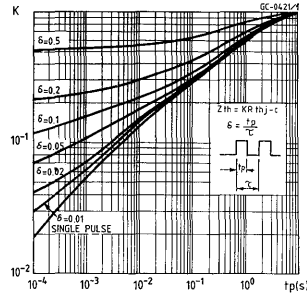


ISOWATT DATA

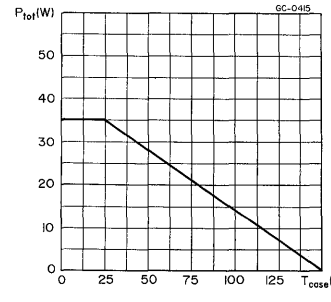
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

MTP6N60

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

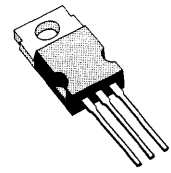
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTP6N60	600 V	1.2 Ω	6 A

- HIGH VOLTAGE - 600 V FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING TIMES FOR OPERATIONS AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

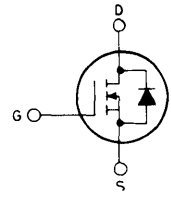
- SWITCHING POWER SUPPLY
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS ideal for very high speed switching applications. Typical uses include SMPS, uninterruptible power supplies and motor controls.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	600	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at T_c = 25°C	6	A
I_{DM}	Drain current (pulsed)	30	A
P_{tot}	Total dissipation at T_c < 25°C	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	62.5	°C/W

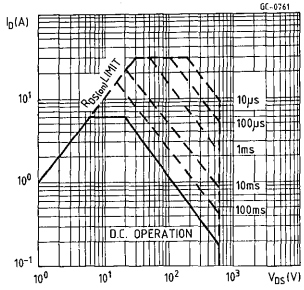
ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			200 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±500	nA
ON						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3 A			1.2	Ω
$V_{DS(on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 6 A V_{GS} = 10 V I_D = 3 A T_c = 100°C			8 7.2	V V
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 10 V I_D = 3 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			1800 350 150	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 3 A R_i = 50 Ω V_i = 10 V			60 150 200 120	ns ns ns ns

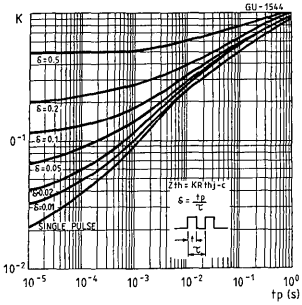
ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					6 30	A A
V_{SD}	Forward on voltage	I_{SD} = 6 A	V_{GS} = 0		1.3		V
t_{rr}	Reverse recovery time	I_{SD} = 6 A	di/dt = 100A/μs		600		ns

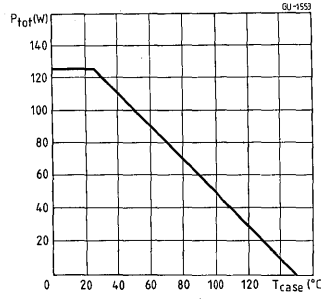
Safe operating areas



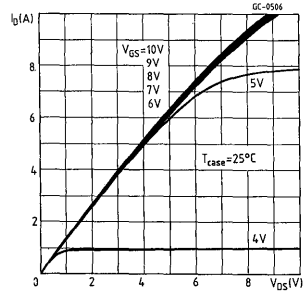
Thermal impedance



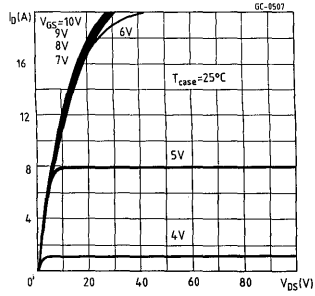
Derating curve



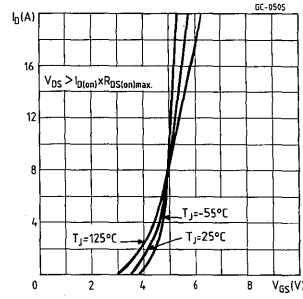
Output characteristics



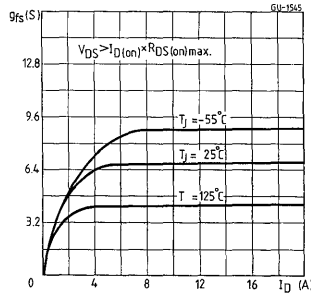
Output characteristics



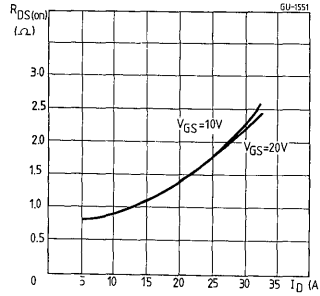
Transfer characteristics



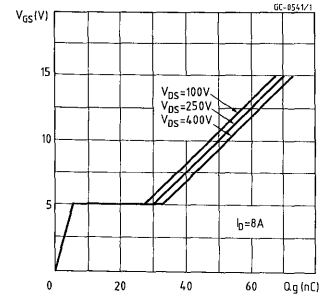
Transconductance



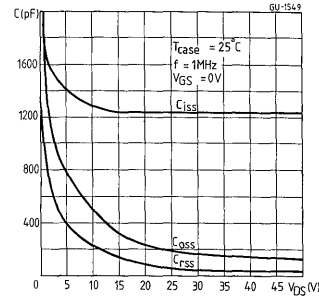
Static drain-source on resistance



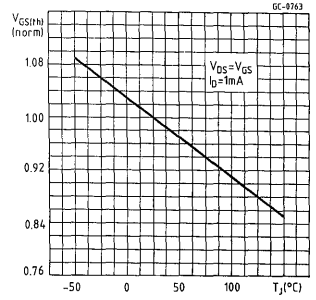
Gate charge vs gate-source voltage



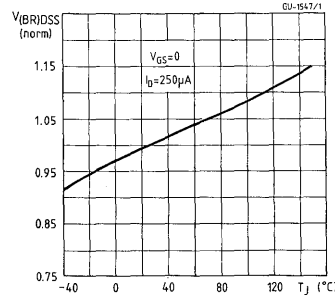
Capacitance variation



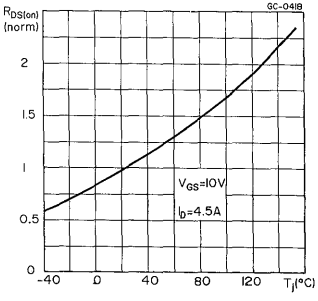
Normalized gate threshold voltage vs temperature



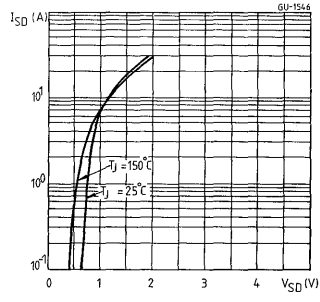
Normalized breakdown voltage vs temperature



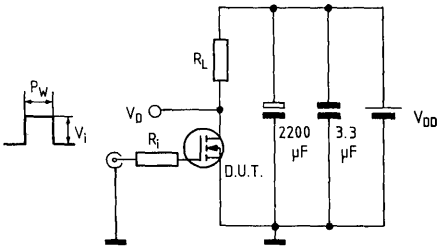
Normalized on resistance vs temperature



Source-drain diode forward characteristics

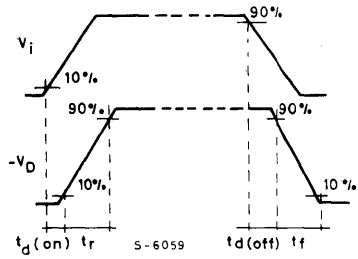


Switching times test circuit for resistive load

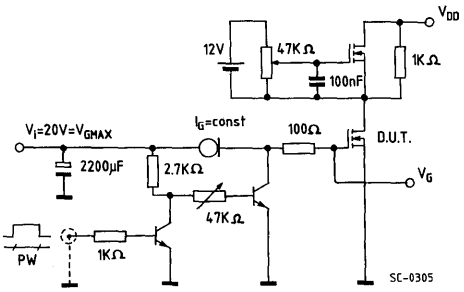


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

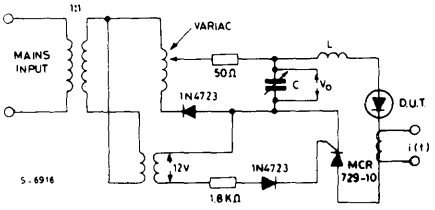


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

MTP15N05L/FI
MTP15N06L/FI

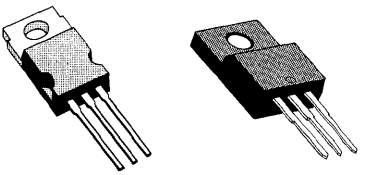
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTORS

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
MTP15N05L	50 V	0.15 Ω	15 A
MTP15N05LFI	50 V	0.15 Ω	10 A
MTP15N06L	60 V	0.15 Ω	15 A
MTP15N06LFI	60 V	0.15 Ω	10 A

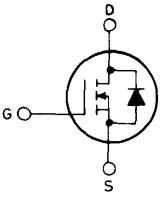
- LOGIC LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive enviroment.



TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	MTP15N06L / MTP15N06LFI	MTP15N05L / MTP15N05LFI	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)		60	50	V
V_{GS}	Gate-source voltage		±15		V
			TO-220	ISOWATT220	
I_D	Drain current (cont.) at $T_c=25°C$		15	10	A
I_D	Drain current (cont.) at $T_c=100°C$		9.5	6.3	A
I_{DM}(•)	Drain current (pulsed)		40	40	A
P_{tot}	Total dissipation at $T_c<25°C$		75	30	W
	Derating factor		0.6	0.24	W/°C
T_{stg}	Storage temperature		−65 to 150		°C
T_j	Max. operating junction temperature		150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	4.16	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	62.5		°C
T_L	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

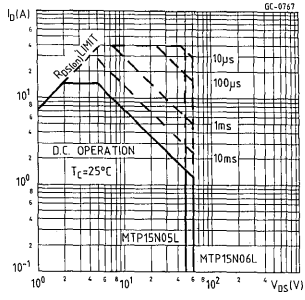
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 1 mA V_{GS} = 0 for **MTP15N06L/FI** for **MTP15N05L/FI**		60 50			V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating	T_c = 125°C			1 50	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±15 V			-	±100	nA
ON **							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA	T_c = 100°C	1 0.75		2 1.5	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 5 V I_D = 7.5 A				0.15	Ω
$V_{DS\ (on)}$	Drain-source on voltage	V_{GS} = 5 V I_D = 15 A V_{GS} = 5 V I_D = 7.5 A	T_c = 100°C			3 1.5	V V
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 15 V	I_D = 7.5 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			900 450 200	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V V_i = 5 V	I_D = 7.5 A R_i = 50 Ω			40 260 200 200	ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-source charge Gate-drain charge	V_{DD} = 48 V V_{GS} = 5 V	I_D = 15 A		14 7 7	22	nC nC nC

ELECTRICAL CHARACTERISTICS (Continued)

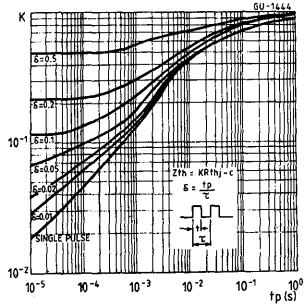
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM}(•) Source-drain current (pulsed)				15 60	A A
V_{SD} ** Forward on voltage	I_{SD} = 15 A V_{GS} = 0		1.8		V
t_{rr} Reverse recovery time	I_{SD} = 15 A di/dt = 100A/μs			300	ns

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%
(•) Pulse width limited by safe operating area

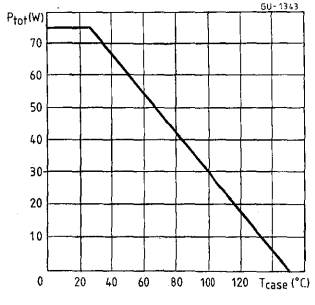
Safe operating areas (standard package)



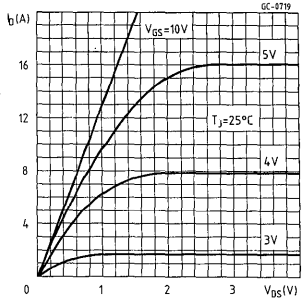
Thermal impedance (standard package)



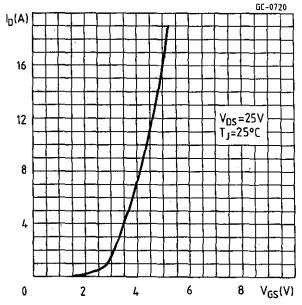
Derating curve (standard package)



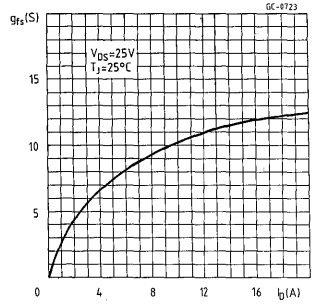
Output characteristics



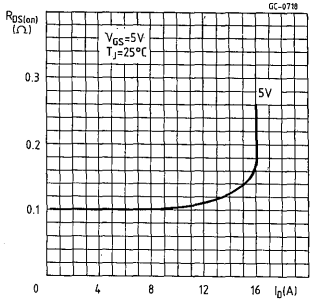
Transfer characteristics



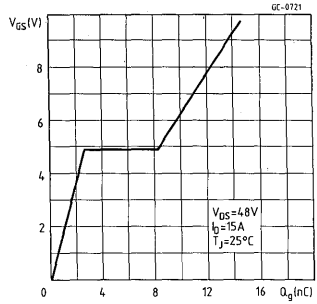
Transconductance



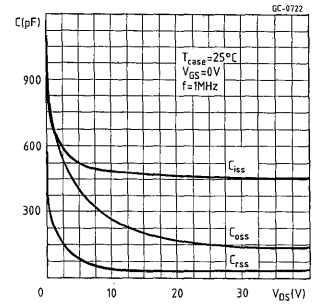
Static drain-source on resistance



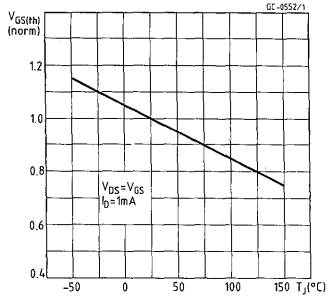
Gate charge vs gate-source voltage



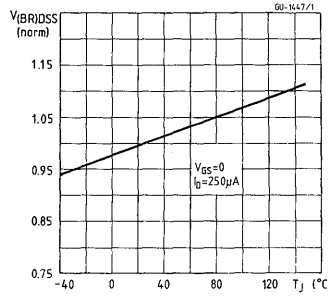
Capacitance variation



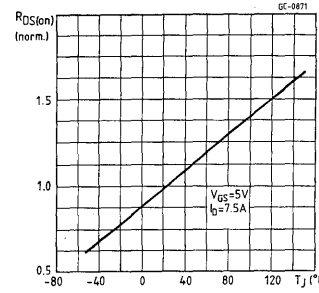
Normalized gate threshold voltage vs temperature



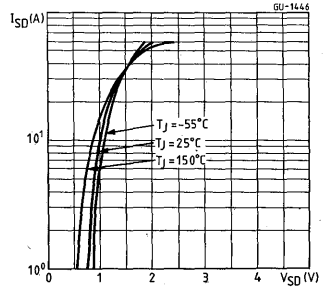
Normalized breakdown voltage vs temperature



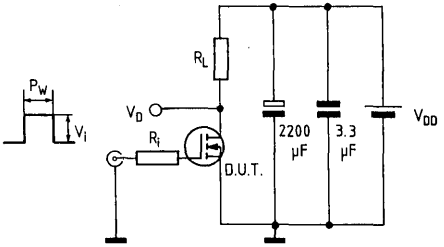
Normalized on resistance vs temperature



Source-drain diode forward characteristics

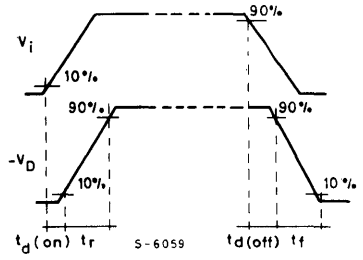


Switching times test circuit for resistive load

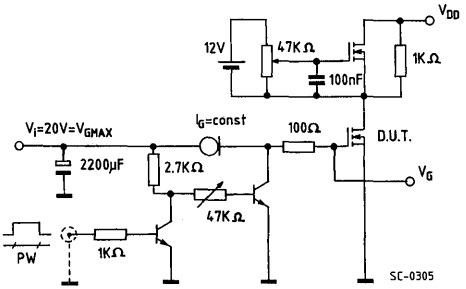


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

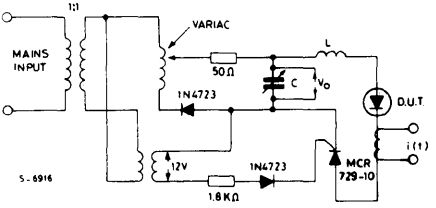


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)}\ (at\ 150°C)}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

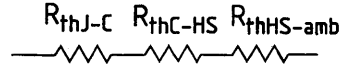
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

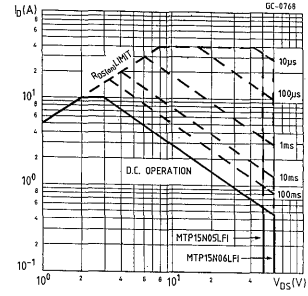
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

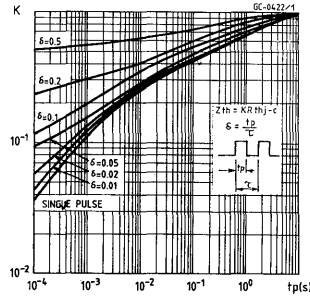


ISOWATT DATA

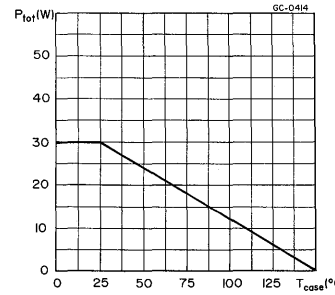
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

MTP3055A
MTP3055AFI

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

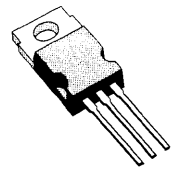
TYPE	V_{DSS}	$R_{DS(on)}$	I_D ■
MTP3055A	60 V	0.15 Ω	12 A
MTP3055AFI	60 V	0.15 Ω	10 A

- ULTRA FAST SWITCHING - UP TO > 100KHz
- LOW DRIVE ENERGY FOR EASY DRIVE REDUCES SIZE AND COST
- INTEGRAL SOURCE - DRAIN DIODE

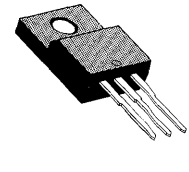
INDUSTRIAL APPLICATIONS:

- GENERAL PURPOSE SWITCH
- SERIES REGULATOR

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast times make these POWER MOS transistors ideal for high speed switching circuit in applications such as power actuator driving, motor drive including brushless motors, robotics, actuators lamp driving, series regulator and many other uses in industrial control applications. They also find use in DC/DC converters and uninterruptible power supplies.

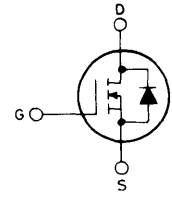


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 / ISOWATT220	MTP3055A / MTP3055AFI	
V_{DS}	Drain-source voltage (V_{GS} = 0)		60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)		60	V
V_{GS}	Gate-source voltage		±20	V
I_{DM}	Drain current (pulsed)		26	A
I_{GM}	Gate current (pulsed)		1.5	A
		TO-220	ISOWATT220	
I_D ■	Drain current (continuous)	12	10	A
P_{tot} ■	Total dissipation at T_c < 25°C	40	30	W
■	Derating factor	0.32	0.24	W/°C
T_{stg}	Storage temperature		−65 to 150	°C
T_j	Max. operating junction temperature		150	°C

■ See note on ISOWATT220 in this datasheet

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	3.12	4.16	°C/W
T_l	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			50 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON *						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA V_{DS} = V_{GS} I_D = 1 mA T_c = 100°C	2 1.5		4.5 4	V V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 6 A		0.15	Ω	
$V_{DS\ (on)}$	Drain-source on voltage	V_{GS} = 10 V I_D = 12 A V_{GS} = 10 V I_D = 6 A V_{GS} = 10 V I_D = 6 A T_c = 100°C			2.0 0.9 1.5	V V V
DYNAMIC						
g_{fs}*	Forward transconductance	V_{DS} = 10 V I_D = 6 A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0			500 200 100	pF pF pF
Q_g	Total gate charge	V_{DS} = 48 V I_D = 12A V_{GS} = 10 V			17	nC
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 6 A R_{gen} = 50 Ω			20 60 65 65	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit

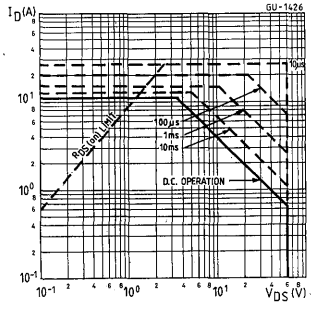
SOURCE DRAIN DIODE

V_{SD}	Forward on voltage	I_{SD} = 12 A	V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A	V_{GS} = 0			75	ns

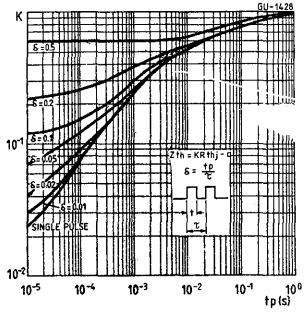
* Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%

■ See note on ISOWATT220 in this datasheet

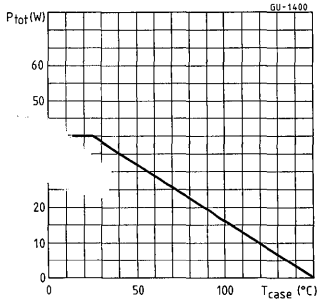
Safe operating areas (standard package)



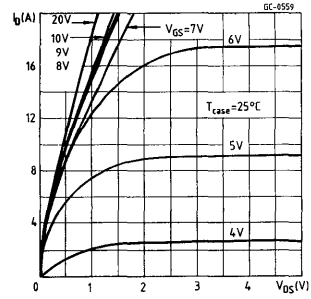
Thermal impedance (standard package)



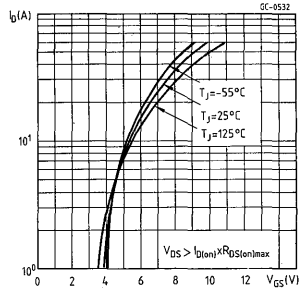
Derating curve (standard package)



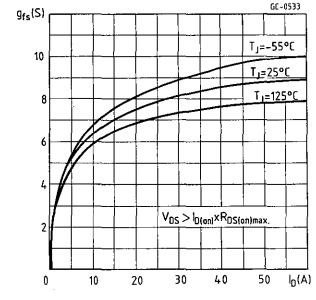
Output characteristics



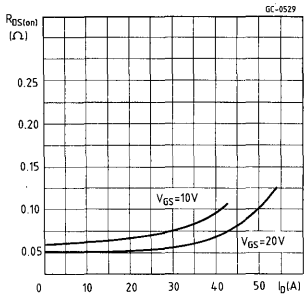
Transfer characteristics



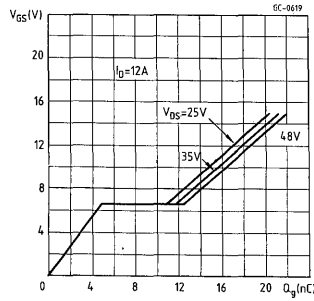
Transconductance



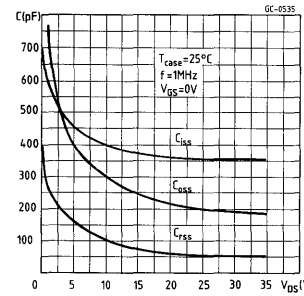
Static drain-source on resistance



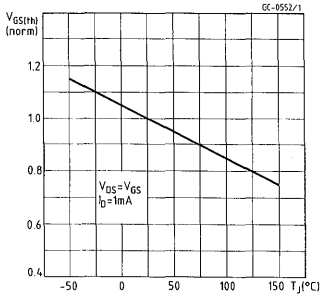
Gate charge vs gate-source voltage



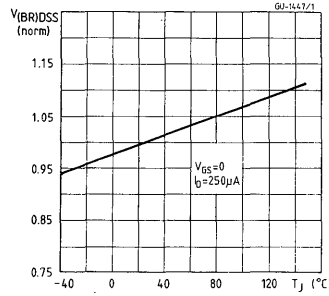
Capacitance variation



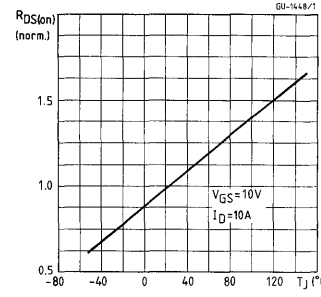
Normalized gate threshold voltage vs temperature



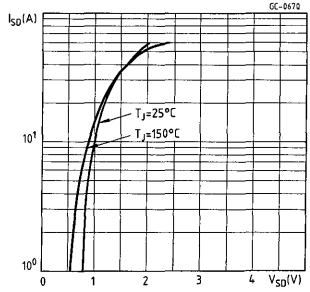
Normalized breakdown voltage vs temperature



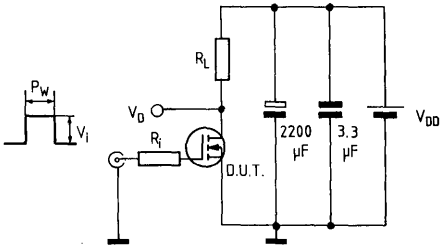
Normalized on resistance vs temperature



Source-drain diode forward characteristics

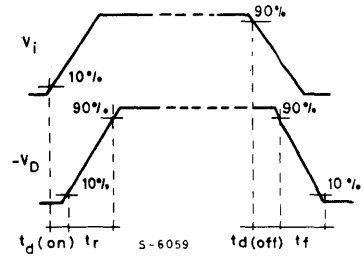


Switching times test circuit for resistive load

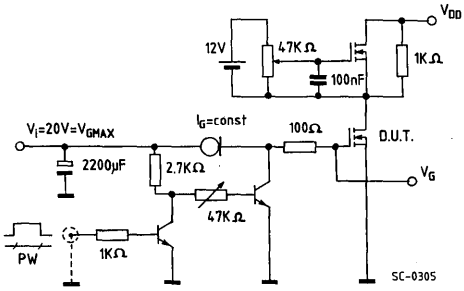


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

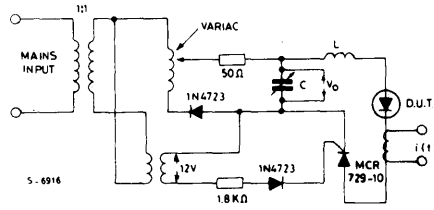


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

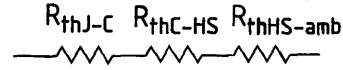
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

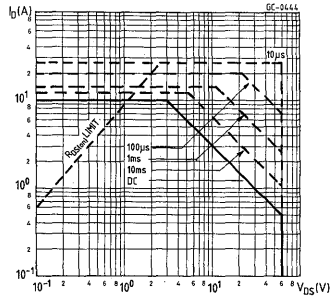
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

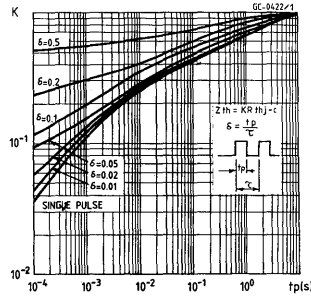


ISOWATT DATA

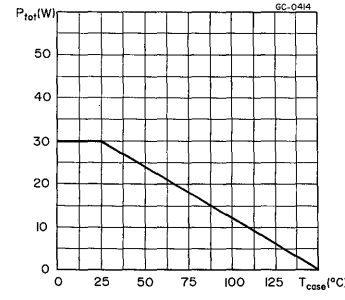
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

SGS30MA050D1

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR MODULE

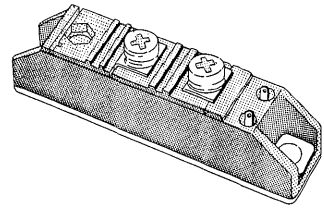
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGS30MA050D1	500 V	0.20 Ω	30 A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

INDUSTRIAL APPLICATIONS:

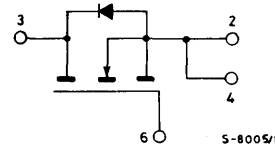
- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and fast switching of this TRANSPACK module make it ideal for high power, high speed switching applications. Typical applications include DC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment. The large RBSOA and absence of second breakdown in POWER MOS make this TRANSPACK module very rugged. This, together with the isolated package with its optimised thermal performance, make this module extremely effective in high power applications.



TO-240

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} =0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} =20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at T_c =25°C	30	A
I_D	Drain current (cont.) at T_c =100°C	19	A
I_{DM}	Drain current (pulsed)	120	A
P_{tot}	Total dissipation at T_c <25°C	400	W
	Derating factor	3.2	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C
V_{ISO}	Insulation withstand voltage (AC)	2500	V

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.31	°C/W
$R_{thc\text{ - }h}$	Thermal resistance case-heatsink	max	0.20	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 2 mA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8	 T_j = 125°C			500 2	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±400	nA
ON*							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 2 mA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 15 A			0.20	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 15 A	15			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			9100 1200 850	pF pF pF
SWITCHING							
	INDUCTIVE LOAD						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 250 V	I_D = 15 A		120		ns
$(di/dt)_{on}$	Turn-on current slope	R_i = 50 Ω	V_i = 10 V		100		A/μs
$t_{d\ (off)}$	Turn-off delay time				1.5		μs
t_f	Fall time				300		ns

ELECTRICAL CHARACTERISTICS (Continued)

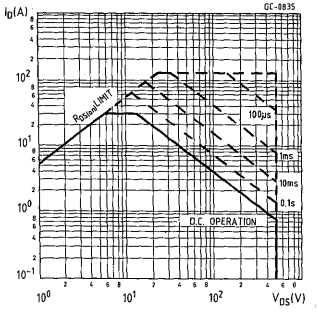
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

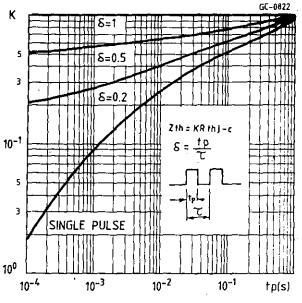
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					30 120	A A
V_{SD}	Forward on voltage	I_{SD} = 30 A	V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A	di/dt = 150A/μs		600		ns

* Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%

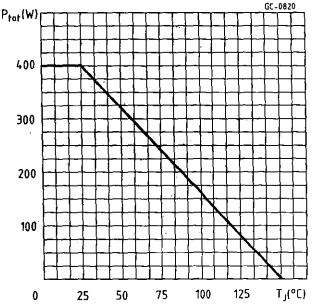
Safe operating areas



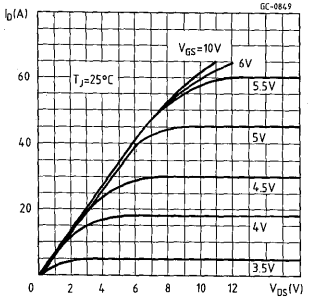
Thermal impedance



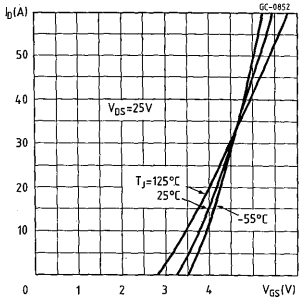
Derating curve



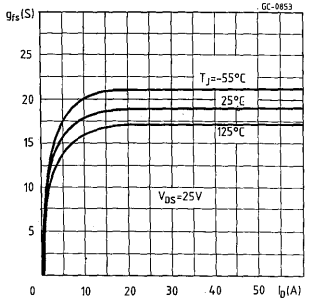
Output characteristics



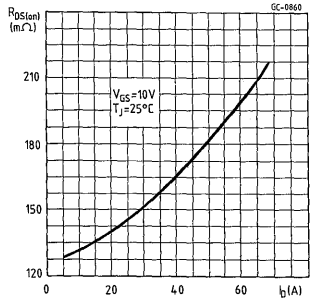
Transfer characteristics



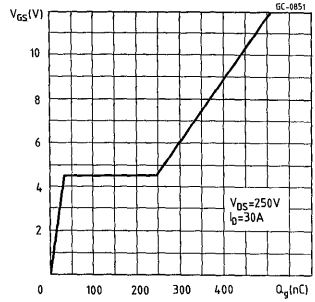
Transconductance



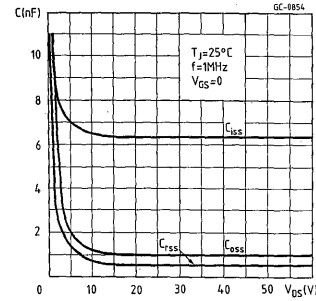
Static drain-source on resistance



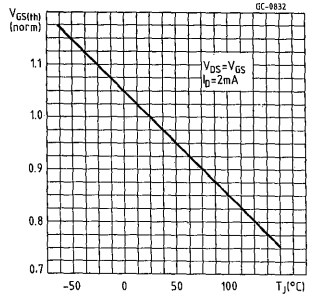
Gate charge vs gate-source voltage



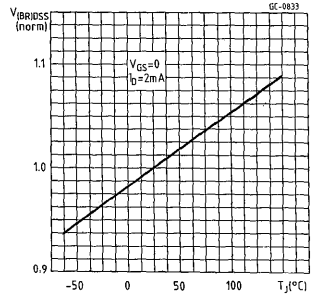
Capacitance variation



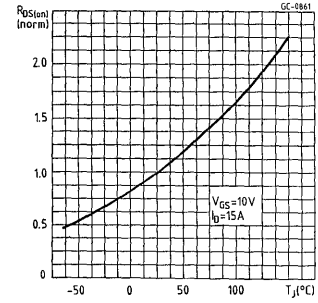
Normalized gate threshold voltage vs temperature



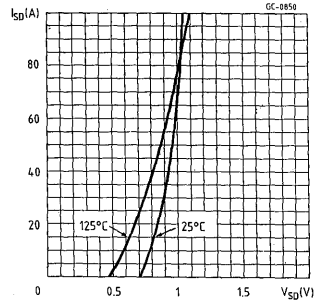
Normalized breakdown voltage vs temperature



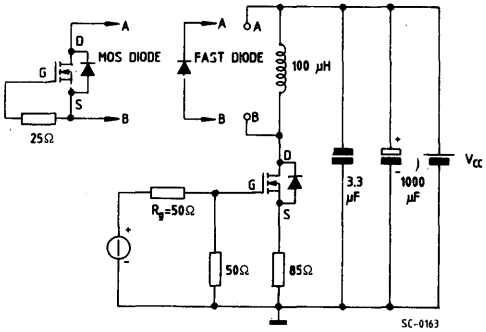
Normalized on resistance vs temperature



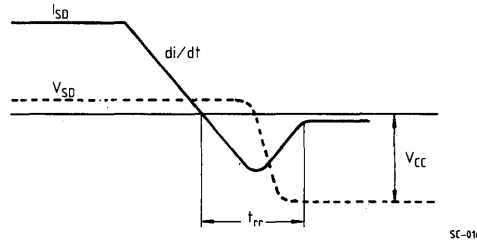
Source-drain diode forward characteristics



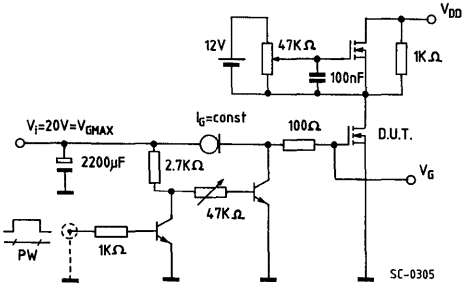
Test circuit for inductive load switching and diode reverse recovery times



Diode reverse recovery time waveform



Gate charge test circuit



PW adjusted to obtain required V_G

SGS-THOMSON MICROELECTRONICS

SGS35MA050D1

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR MODULE

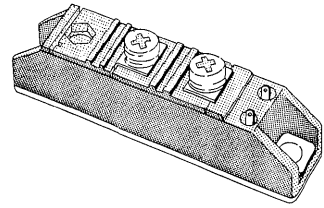
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGS35MA050D1	500 V	0.16 Ω	35 A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

INDUSTRIAL APPLICATIONS:

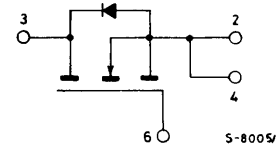
- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and fast switching of this TRANSPACK module make it ideal for high power, high speed switching applications. Typical applications include DC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment. The large RBSOA and absence of second breakdown in POWER MOS make this TRANSPACK module very rugged. This, together with the isolated package with its optimised thermal performance, make this module extremely effective in high power applications.



TO-240

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} =0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} =20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at T_c =25°C	35	A
I_D	Drain current (cont.) at T_c =100°C	22	A
I_{DM}	Drain current (pulsed)	140	A
P_{tot}	Total dissipation at T_c <25°C	400	W
	Derating factor	3.2	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C
V_{ISO}	Insulation withstand voltage (AC)	2500	V

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.31	°C/W
$R_{thc\text{-}h}$	Thermal resistance case-heatsink	max	0.20	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 2 mA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C				500 2	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±500	nA
ON*							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 2 mA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 17.5 A			0.16	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 17.5 A	15			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			12000 1500 1000	pF pF pF
SWITCHING							
$t_{d\ (on)}$ $(di/dt)_{on}$ $t_{d\ (off)}$ t_f	Turn-on time Turn-on current slope Turn-off delay time Fall time	V_{DD} = 250 V R_i = 50 Ω	I_D = 17.5 A V_i = 10 V		120 100 1.5 300		ns A/μs μs ns

ELECTRICAL CHARACTERISTICS (Continued)

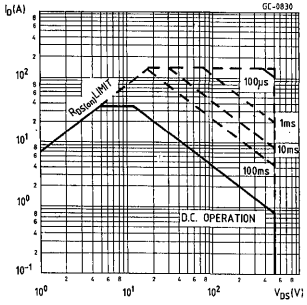
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

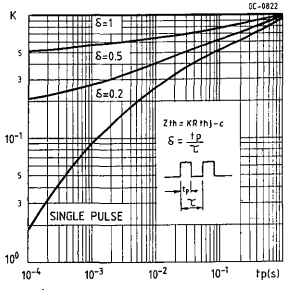
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					35 140	A A
V_{SD}	Forward on voltage	I_{SD} = 35 A	V_{GS} = 0			2	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A	di/dt = 150A/μs		600		ns

* Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%

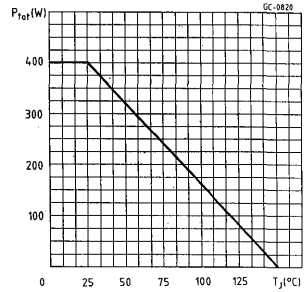
Safe operating areas



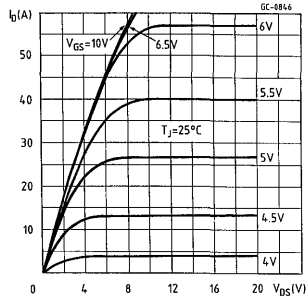
Thermal impedance



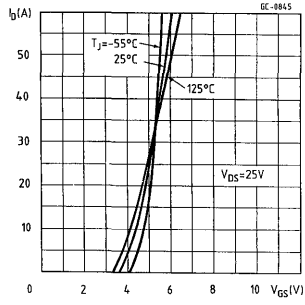
Derating curve



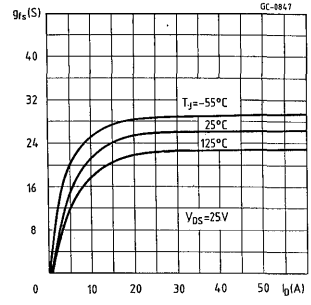
Output characteristics



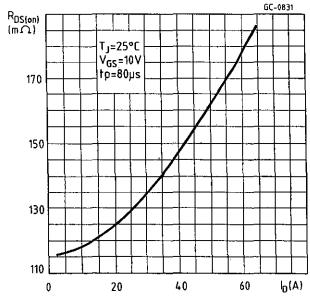
Transfer characteristics



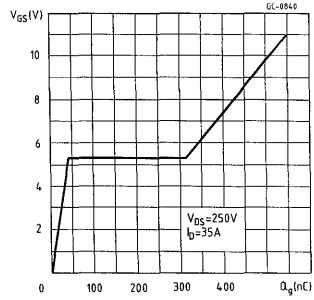
Transconductance



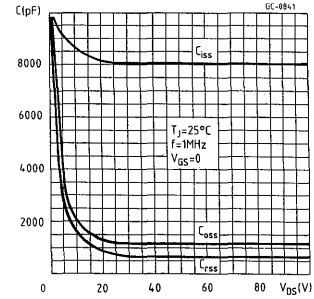
Static drain-source on resistance



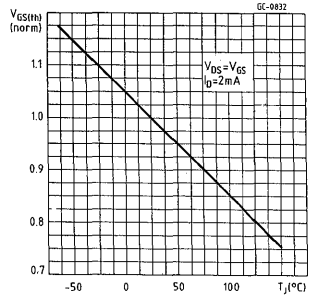
Gate charge vs gate-source voltage



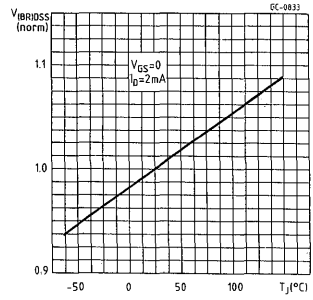
Capacitance variation



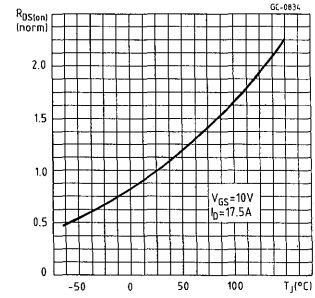
Normalized gate threshold voltage vs temperature



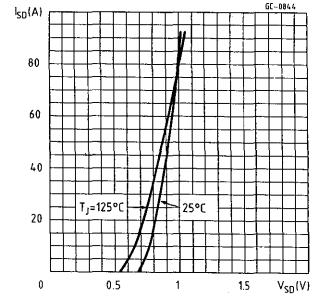
Normalized breakdown voltage vs temperature



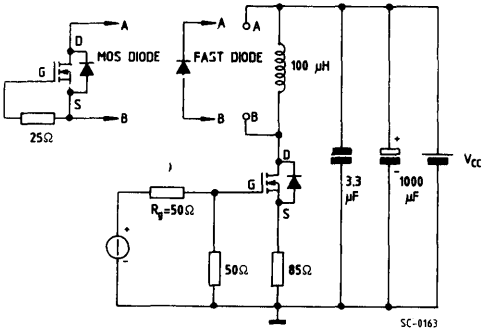
Normalized on resistance vs temperature



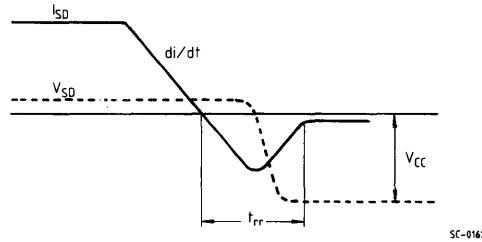
Source-drain diode forward characteristics



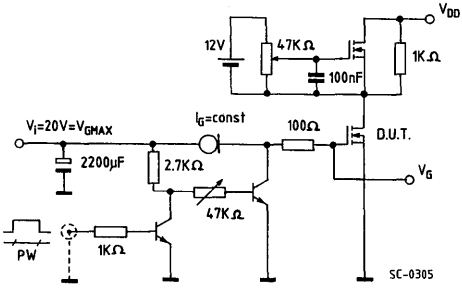
Test circuit for inductive load switching and diode reverse recovery times



Diode reverse recovery time waveform



Gate charge test circuit



PW adjusted to obtain required V_G

SGS-THOMSON MICROELECTRONICS

SGS100MA010D1

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR MODULE

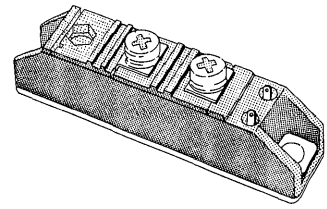
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGS100MA010D1	100 V	0.014 Ω	120 A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

INDUSTRIAL APPLICATIONS:

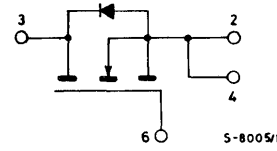
- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and fast switching of this TRANSPACK module make it ideal for high power, high speed switching applications. Typical applications include DC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment. The large RBSOA and absence of second breakdown in POWER MOS make this TRANSPACK module very rugged. This, together with the isolated package with its optimised thermal performance, make this module extremely effective in high power applications.



TO-240

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (cont.) at T_c = 25°C	120	A
I_D	Drain current (cont.) at T_c = 100°C	75	A
I_{DM}	Drain current (pulsed)	400	A
P_{tot}	Total dissipation at T_c < 25°C	400	W
	Derating factor	3.2	W/°C
T_{stg}	Storage temperature	− 65 to 150	°C
T_j	Max. operating junction temperature	150	°C
V_{ISO}	Insulation withstand voltage (AC)	2500	V

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.31	°C/W
$R_{thc\text{ - }h}$	Thermal resistance case-heatsink	max	0.20	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	$I_D = 2$ mA	$V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating	 $T_j = 125°C$			500 2	μA mA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20$ V			-	±400	nA
ON*							
$V_{GS\ (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 2$ mA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	$V_{GS} = 10$ V	$I_D = 50$ A			14	mΩ
DYNAMIC							
g_{fs}	Forward transconductance	$V_{DS} = 25$ V	$I_D = 50$ A	20			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25$ V $V_{GS} = 0$	$f = 1$ MHz			11200 4200 1700	pF pF pF
SWITCHING							
$t_{d\ (on)}$ $(di/dt)_{on}$ $t_{d\ (off)}$ t_f	Turn-on time Turn-on current slope Turn-off delay time Fall time	$V_{DD} = 50$ V $R_i = 50\ \Omega$	$I_D = 50$ A $V_i = 10$ V		120 100 2 300		ns A/μs μs ns

ELECTRICAL CHARACTERISTICS (Continued)

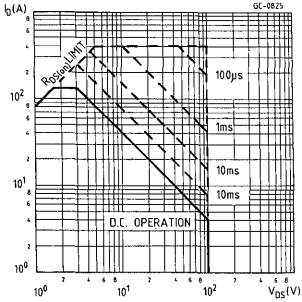
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

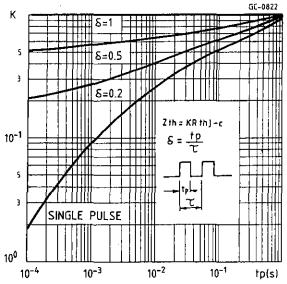
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				120 400	A A
V_{SD}	Forward on voltage	I_{SD} = 120 A	V_{GS} = 0		2	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A	di/dt = 100A/μs	400		ns

* Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%

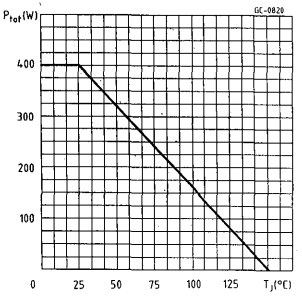
Safe operating areas



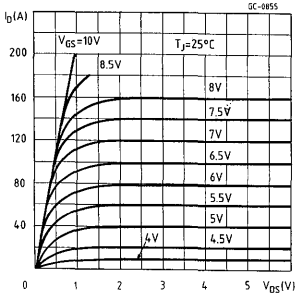
Thermal impedance



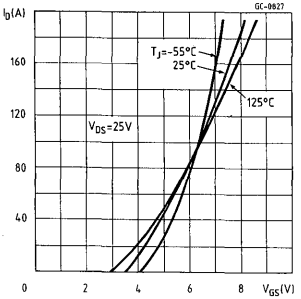
Derating curve



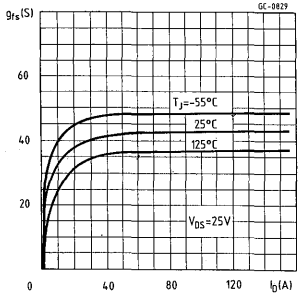
Output characteristics



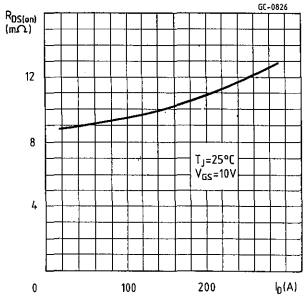
Transfer characteristics



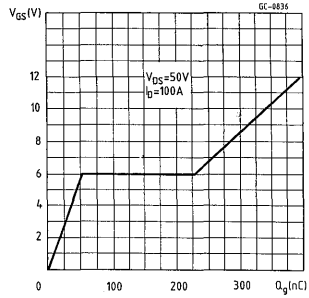
Transconductance



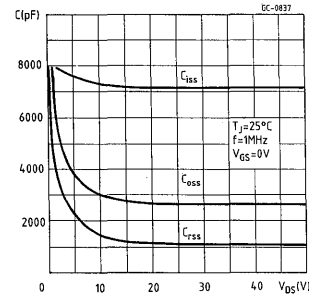
Static drain-source on resistance



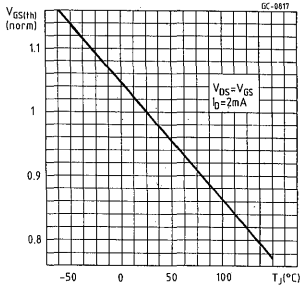
Gate charge vs gate-source voltage



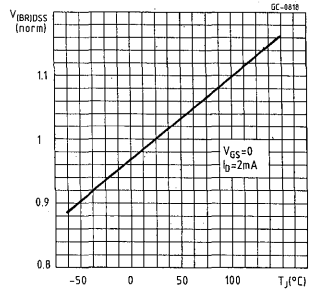
Capacitance variation



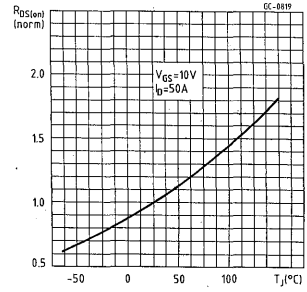
Normalized gate threshold voltage vs temperature



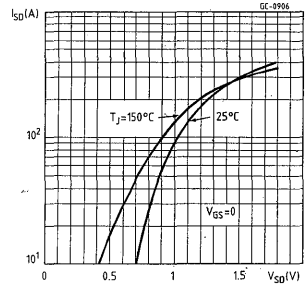
Normalized breakdown voltage vs temperature



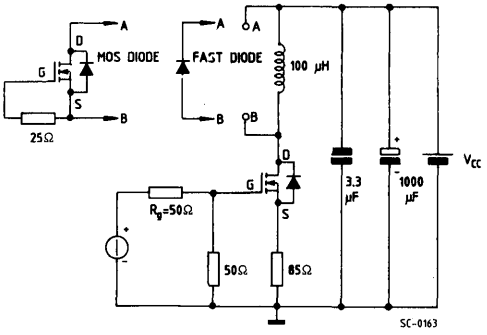
Normalized on resistance vs temperature



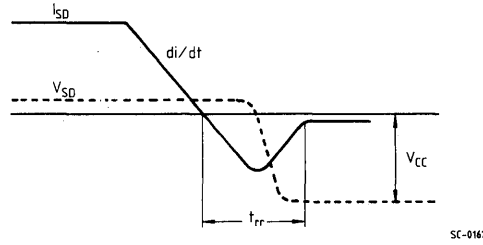
Source-drain diode forward characteristics



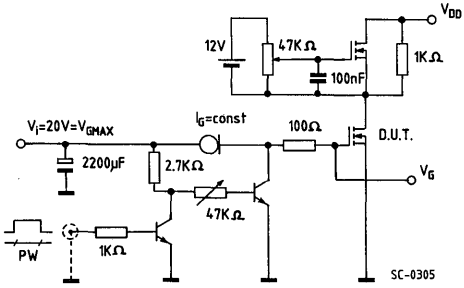
Test circuit for inductive load switching and diode reverse recovery times



Diode reverse recovery time waveform



Gate charge test circuit



PW adjusted to obtain required V_G

SGS-THOMSON MICROELECTRONICS

SGS150MA010D1

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR MODULE

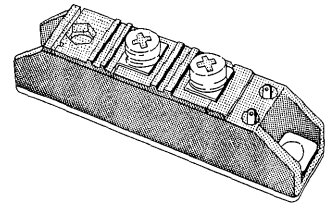
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGS150MA010D1	100 V	0.009 Ω	150 A

- ISOLATED POWERMOS MODULE
- HIGH POWER
- FAST SWITCHING
- EASY DRIVE
- EASY TO PARALLEL

INDUSTRIAL APPLICATIONS:

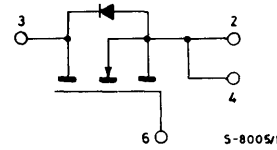
- SWITCHING MODE POWER SUPPLIES
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS
- INVERTERS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and fast switching of this TRANSPACK module make it ideal for high power, high speed switching applications. Typical applications include DC motor control (variable frequency control) switching mode power supplies, uninterruptible power supplies, DC/DC convertors and high frequency welding equipment. The large RBSOA and absence of second breakdown in POWER MOS make this TRANSPACK module very rugged. This, together with the isolated package with its optimised thermal performance, make this module extremely effective in high power applications.



TO-240

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	100	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (cont.) at T_c = 25°C	150	A
I_D	Drain current (cont.) at T_c = 100°C	95	A
I_{DM}	Drain current (pulsed)	600	A
P_{tot}	Total dissipation at T_c < 25°C	400	W
	Derating factor	3.2	W/°C
T_{stg}	Storage temperature	− 65 to 150	°C
T_j	Max. operating junction temperature	150	°C
V_{ISO}	Insulation withstand voltage (AC)	2500	V

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.33	°C/W
$R_{thc\text{ - }h}$	Thermal resistance case-heatsink	max	0.20	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 2 μA	V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8	 T_j = 125°C			500 2	μA mA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±500	nA
ON*							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 2 mA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 75 A			9	mΩ
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 75 A	20			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz			14000 5300 2200	pF pF pF
SWITCHING							
$t_{d\ (on)}$ $(di/dt)_{on}$ $t_{d\ (off)}$ t_f	Turn-on time Turn-on current slope Turn-off delay time Fall time	V_{DD} = 50 V R_i = 50 Ω	I_D = 75 A V_i = 10 V		120 100 2 300		ns A/μs μs ns

ELECTRICAL CHARACTERISTICS (Continued)

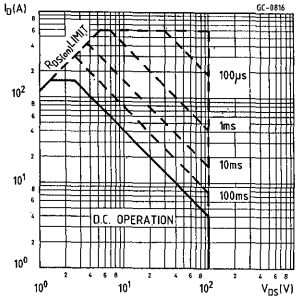
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

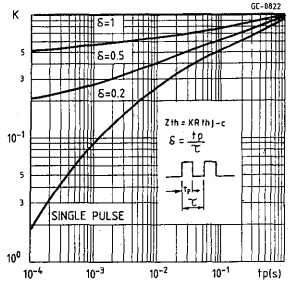
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				150 600	A A
V_{SD}	Forward on voltage	I_{SD} = 150 A	V_{GS} = 0		2	V
t_{rr}	Reverse recovery time	I_{SD} = 150 A	di/dt = 250A/μs	400		ns

* Pulsed: Pulse duration ≤ 300 μs, duty cycle ≤ 2%

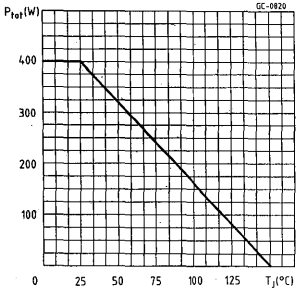
Safe operating areas



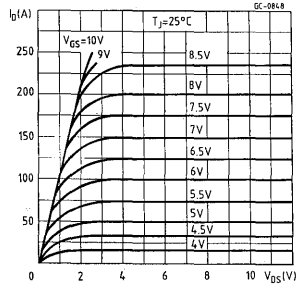
Thermal impedance



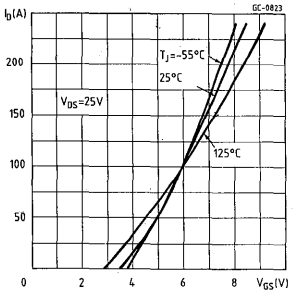
Derating curve



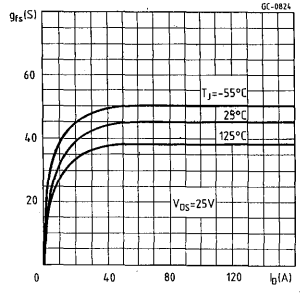
Output characteristics



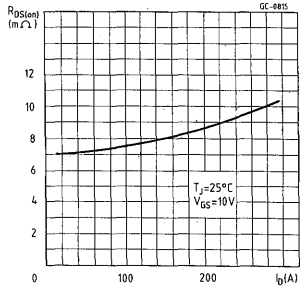
Transfer characteristics



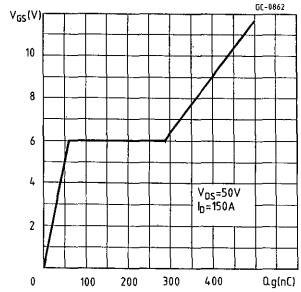
Transconductance



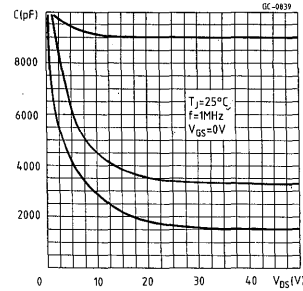
Static drain-source on resistance



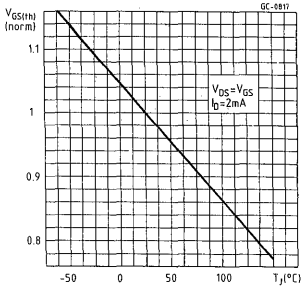
Gate charge vs gate-source voltage



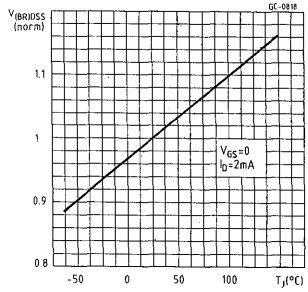
Capacitance variation



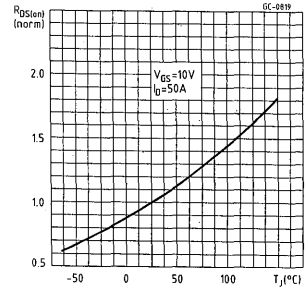
Normalized gate threshold voltage vs temperature



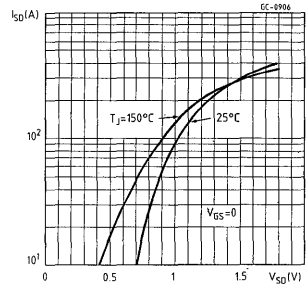
Normalized breakdown voltage vs temperature



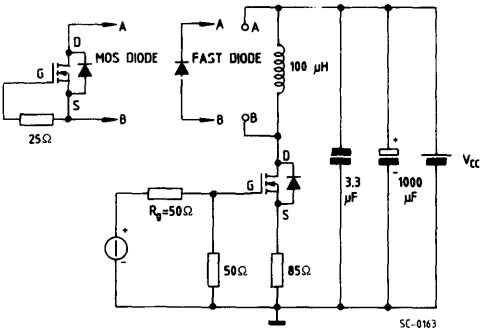
Normalized on resistance vs temperature



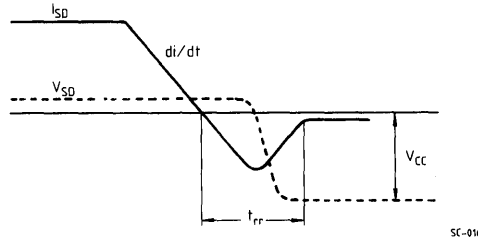
Source-drain diode forward characteristics



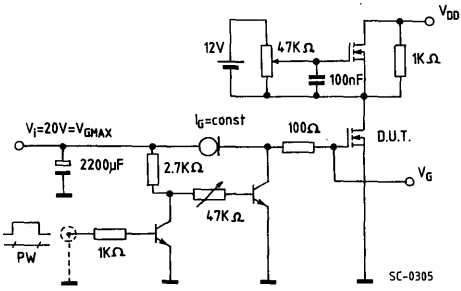
Test circuit for inductive load switching and diode reverse recovery times



Diode reverse recovery time waveform



Gate charge test circuit



PW adjusted to obtain required V_G

SGS-THOMSON MICROELECTRONICS

SGSP201

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

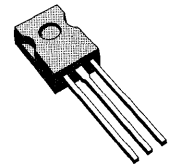
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP201	100 V	1.4 Ω	2.0 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

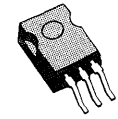
INDUSTRIAL APPLICATIONS:

- GENERAL PURPOSE SWITCHING

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include general purpose low voltage switching, solenoid driving, motor and lamp control, switching power supplies, and driving, bipolar power switching transistors.

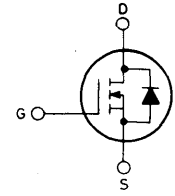


SOT-82



OPTION
SOT-194

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	2.0	A
I_D	Drain current (cont.) at $T_c=100°C$	1.2	A
I_{DM} (•)	Drain current (pulsed)	6	A
I_{DLM} (•)	Drain inductive current, clamped	6	A
P_{tot}	Total dissipation at $T_c<25°C$	18	W
	Derating factor	0.144	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	6.95	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

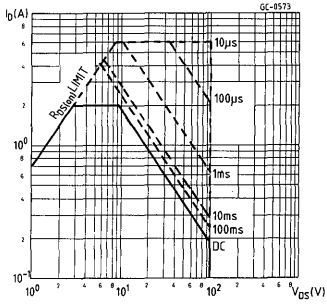
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.2 A V_{GS} = 10 V I_D = 1.2 A T_c = 100°C			1.4 2.8	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 1.2 A	0.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		90	125 45 30	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 50 V I_D = 1.2 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 20 15 15	15 30 20 20	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

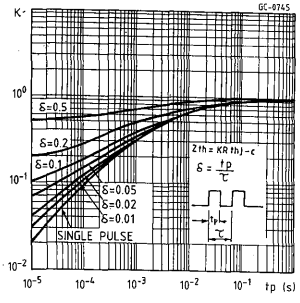
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				2.0 6	A A
V_{SD} Forward on voltage	I_{SD} = 2.0 A V_{GS} = 0			1.35	V
t_{rr} Reverse recovery time	I_{SD} = 2.0 A V_{GS} = 0 di/dt = 25 A/μs		90		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

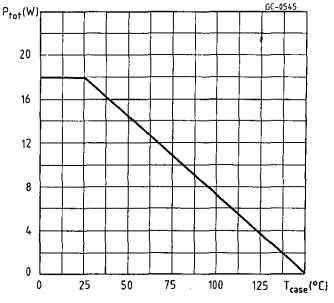
Safe operating areas



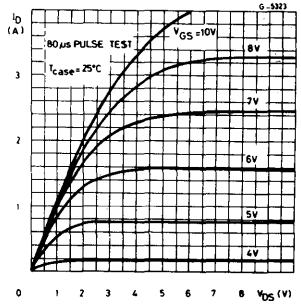
Thermal impedance



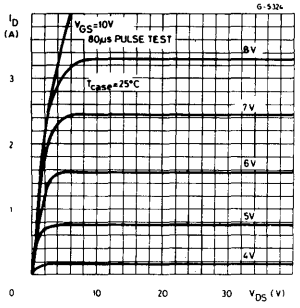
Derating curve



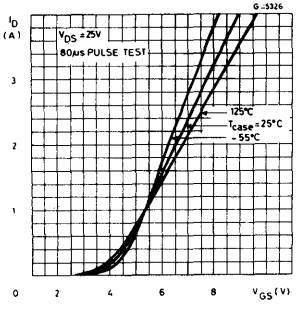
Output characteristics



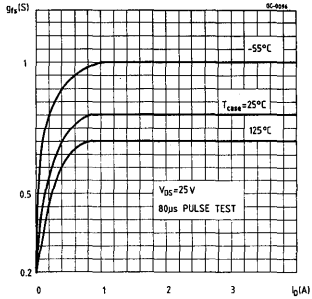
Output characteristics



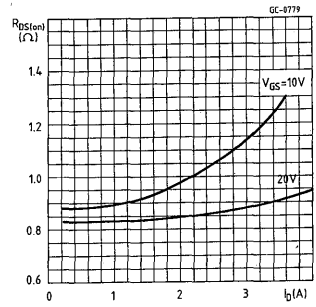
Transfer characteristics



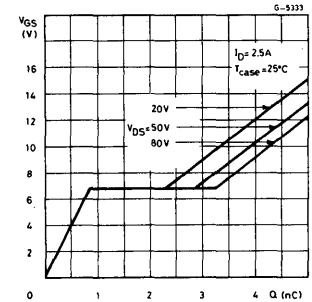
Transconductance



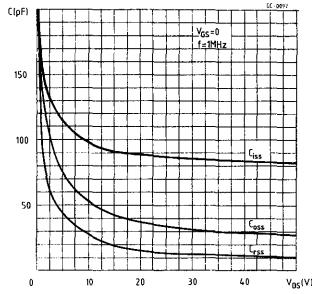
Static drain-source on resistance



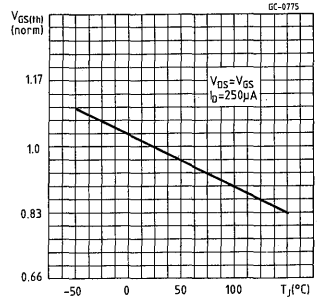
Gate charge vs gate-source voltage



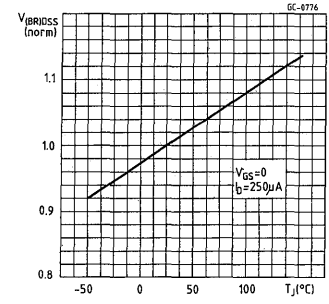
Capacitance variation



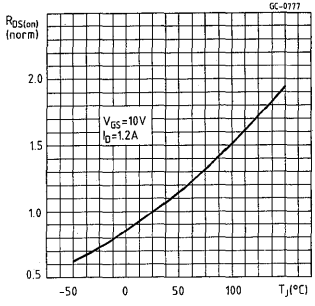
Normalized gate threshold voltage vs temperature



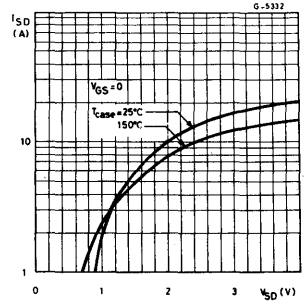
Normalized breakdown voltage vs temperature



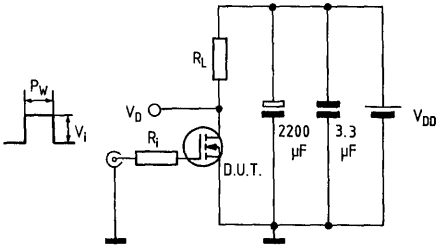
Normalized on resistance vs temperature



Source-drain diode forward characteristics

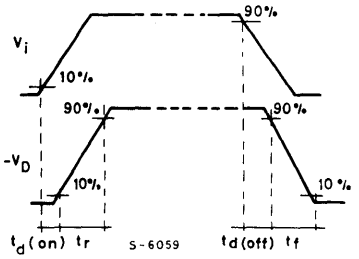


Switching times test circuit for resistive load

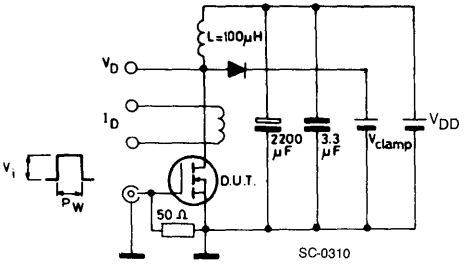


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

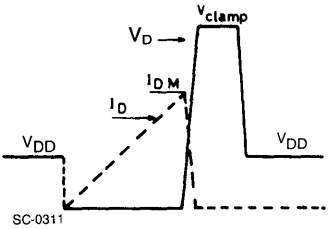


Clamped inductive load test circuit

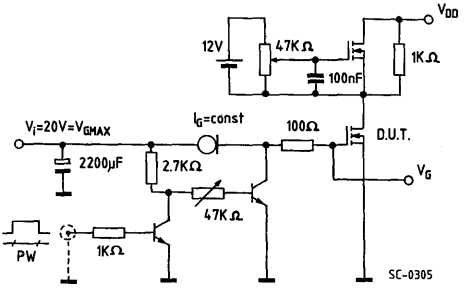


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

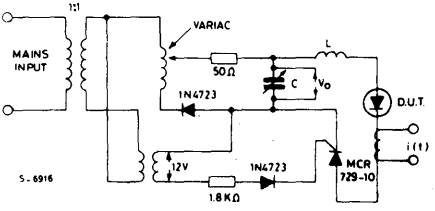


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP222

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

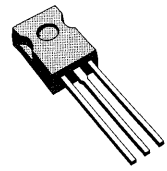
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP222	50 V	0.13 Ω	10 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

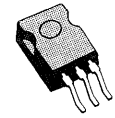
INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS.

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Uses include general motor speed control, low voltage DC/DC converters and solenoid driving.

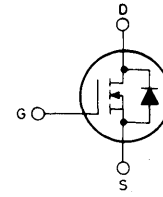


SOT-82



OPTION SOT-194

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	10	A
I_D	Drain current (cont.) at $T_c=100°C$	6.3	A
I_{DM} (•)	Drain current (pulsed)	40	A
I_{DLM} (•)	Drain inductive current, clamped	40	A
P_{tot}	Total dissipation at $T_c<25°C$	50	W
	Derating factor	0.4	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	2.5	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

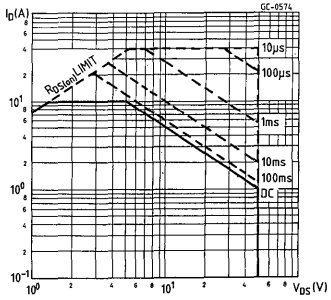
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5 A V_{GS} = 10 V I_D = 5 A T_c = 100°C			0.13 0.26	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		15 40 40 20	20 55 55 30	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

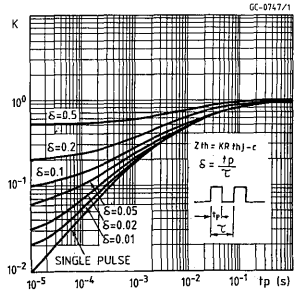
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				10 40	A A
V_{SD} Forward on voltage	I_{SD} = 10 A V_{GS} = 0			1.4	V
t_{rr} Reverse recovery time	I_{SD} = 10 A V_{GS} = 0 di/dt = 25 A/μs		100		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

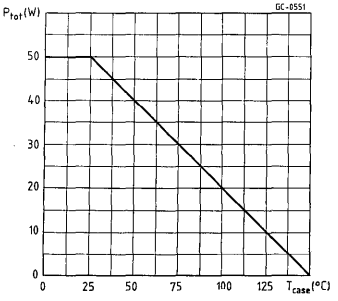
Safe operating areas



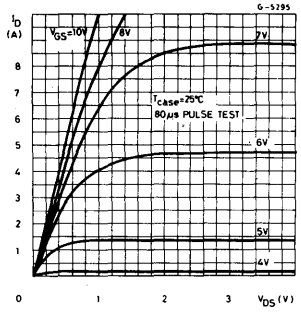
Thermal impedance



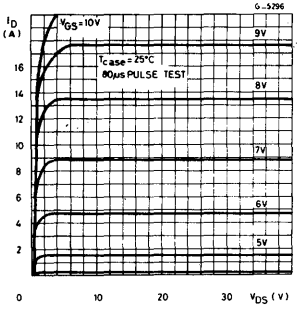
Derating curve



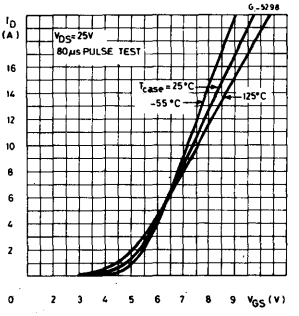
Output characteristics



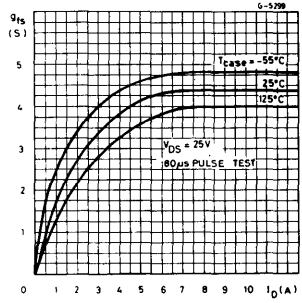
Output characteristics



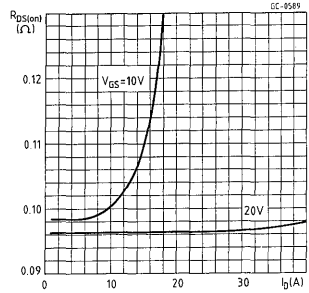
Transfer characteristics



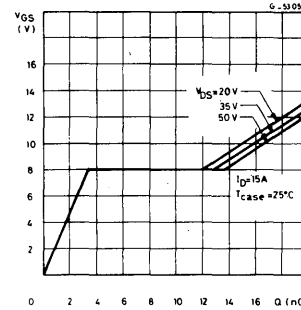
Transconductance



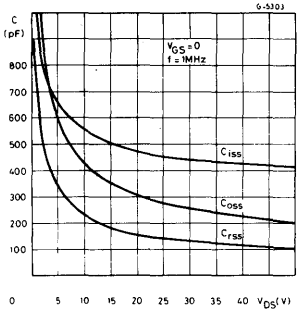
Static drain-source on resistance



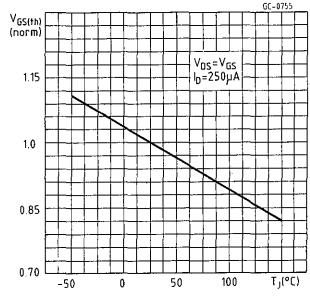
Gate charge vs gate-source voltage



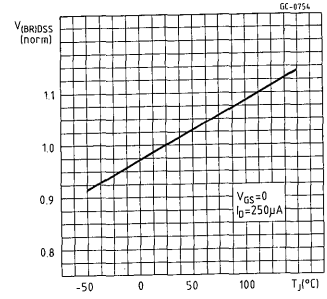
Capacitance variation



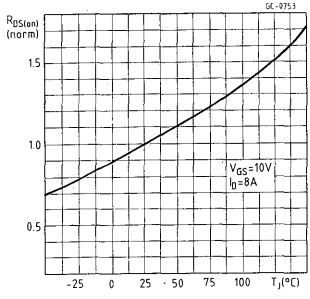
Normalized gate threshold voltage vs temperature



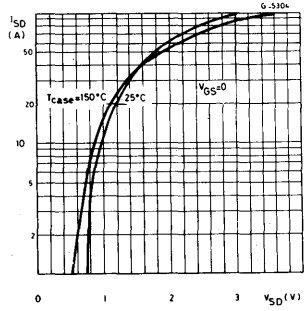
Normalized breakdown voltage vs temperature



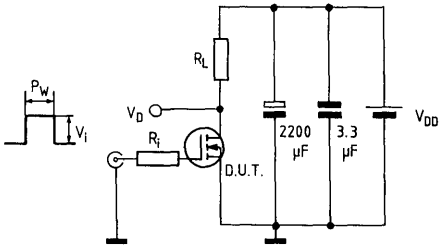
Normalized on resistance vs temperature



Source-drain diode forward characteristics

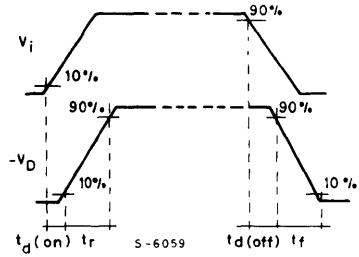


Switching times test circuit for resistive load

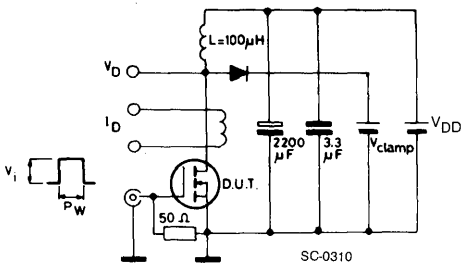


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

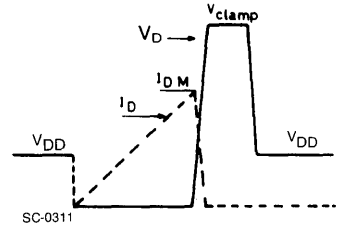


Clamped inductive load test circuit

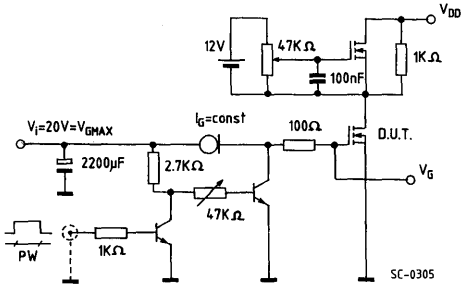


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

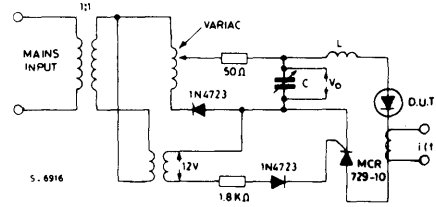


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP230

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

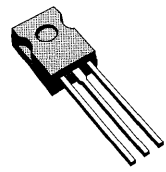
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP230	450 V	3 Ω	2.5 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 450V FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

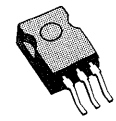
INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching power supplies, uninterruptible power supplies and motor speed control.

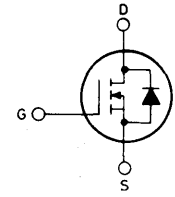


SOT-82



OPTION SOT-194

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	450	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	450	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	2.5	A
I_D	Drain current (cont.) at $T_c = 100°C$	1.5	A
I_{DM} (•)	Drain current (pulsed)	10	A
I_{DLM} (•)	Drain inductive current, clamped	10	A
P_{tot}	Total dissipation at $T_c < 25°C$	50	W
	Derating factor	0.4	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	2.5	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

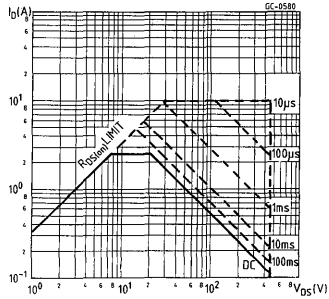
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	450			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.2 A V_{GS} = 10 V I_D = 1.2 A T_c = 100°C			3 6	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 1.2 A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		340	450 95 50	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 1.2 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 25 55 25	15 35 70 35	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

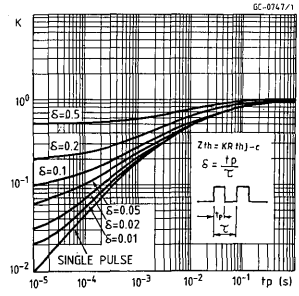
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (*) Source-drain current (pulsed)				2.5 10	A A
V_{SD} Forward on voltage	I_{SD} = 2.5 A V_{GS} = 0			1.2	V
t_{rr} Reverse recovery time	I_{SD} = 2.5 A V_{GS} = 0 di/dt = 100 A/μs		340		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

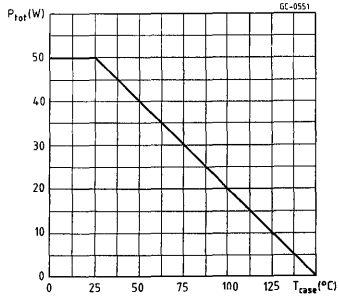
Safe operating areas



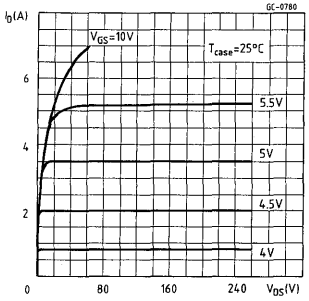
Thermal impedance



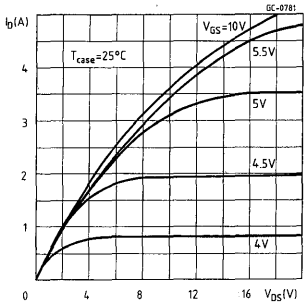
Derating curve



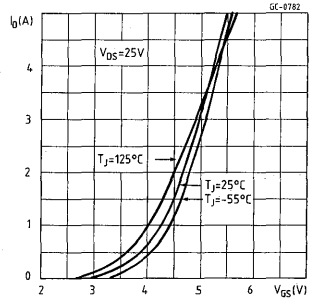
Output characteristics



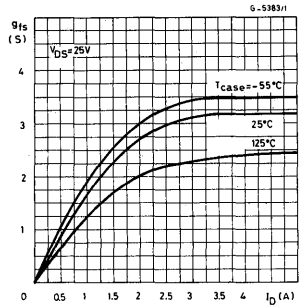
Output characteristics



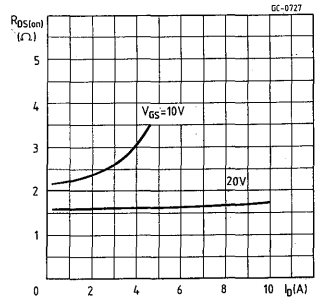
Transfer characteristics



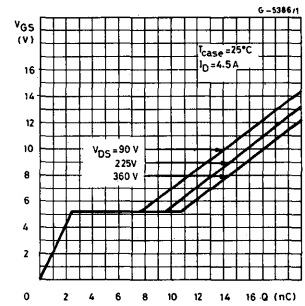
Transconductance



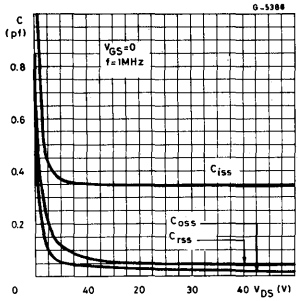
Static drain-source on resistance



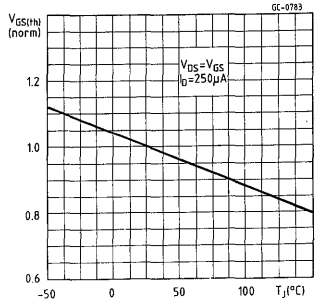
Gate charge vs gate-source voltage



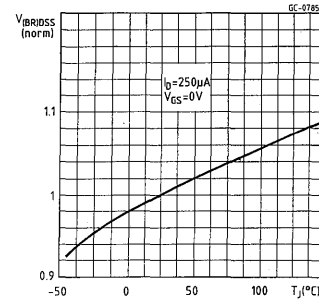
Capacitance variation



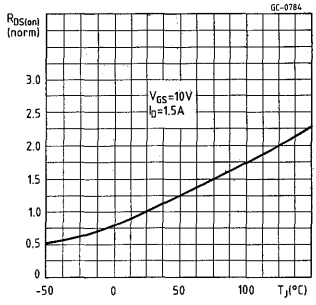
Normalized gate threshold voltage vs temperature



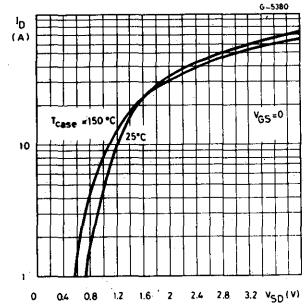
Normalized breakdown voltage vs temperature



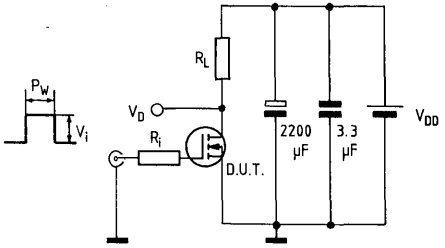
Normalized on resistance vs temperature



Source-drain diode forward characteristics

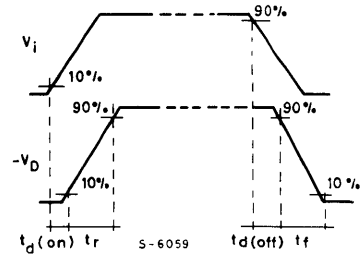


Switching times test circuit for resistive load

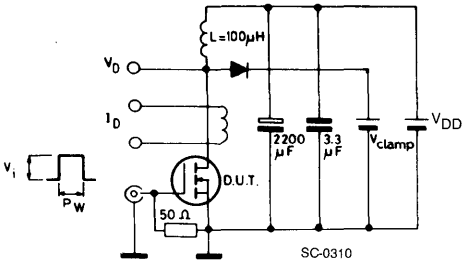


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

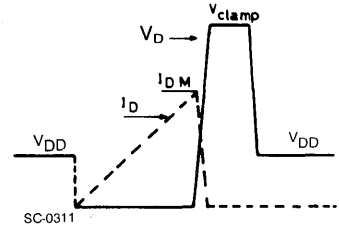


Clamped inductive load test circuit

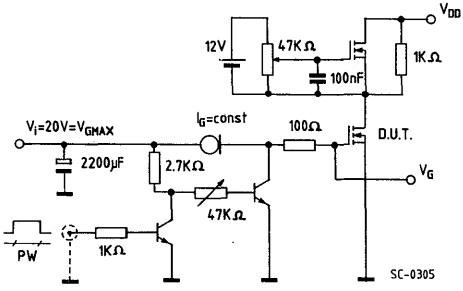


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

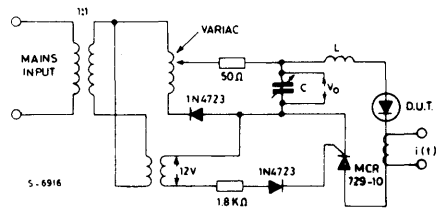


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP239

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

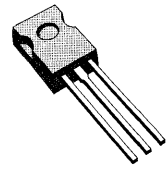
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP239	500 V	8.5 Ω	1.2 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

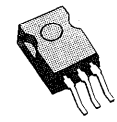
INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. These include switching power supplies, solenoid drivers and drive circuits for power bipolar transistors.

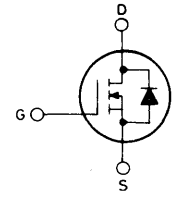


SOT-82



OPTION SOT-194

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	1.2	A
I_D	Drain current (cont.) at $T_c=100°C$	0.8	A
I_{DM} (•)	Drain current (pulsed)	4.8	A
I_{DLM} (•)	Drain inductive current, clamped	4.8	A
P_{tot}	Total dissipation at $T_c<25°C$	40	W
	Derating factor	0.32	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	3.12	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

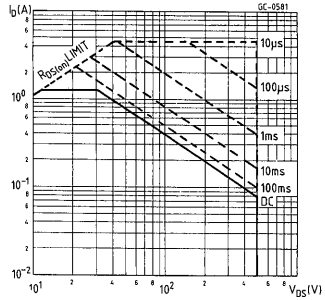
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 0.6 A V_{GS} = 10 V I_D = 0.6 A T_c = 100°C			8.5 17	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 0.6 A	0.65			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		260	300 80 40	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 250 V I_D = 0.6 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		15 15 30 20	20 30 60 45	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

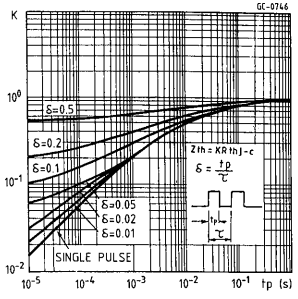
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				1.2 4.8	A A
V_{SD} Forward on voltage	I_{SD} = 1.2 A V_{GS} = 0			1.15	V
t_{rr} Reverse recovery time	I_{SD} = 1.2 A V_{GS} = 0 di/dt = 25 A/μs		350		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

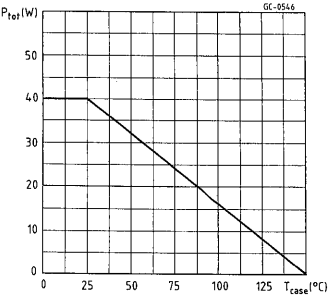
Safe operating areas



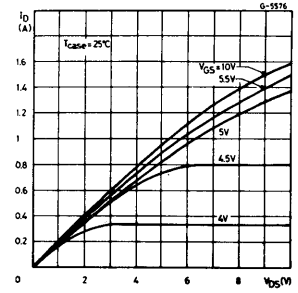
Thermal impedance



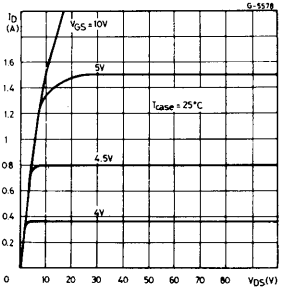
Derating curve



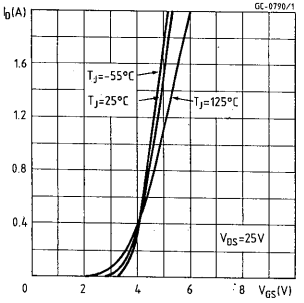
Output characteristics



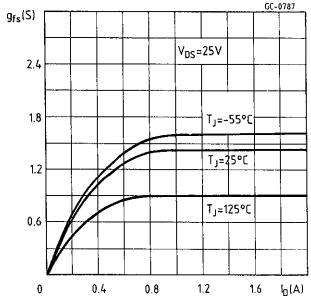
Output characteristics



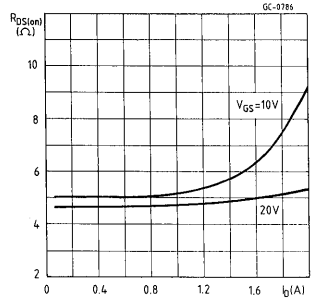
Transfer characteristics



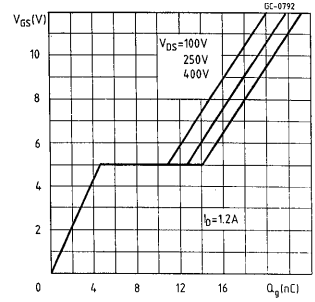
Transconductance



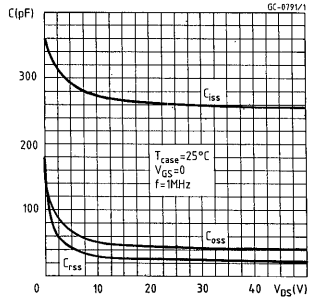
Static drain-source on resistance



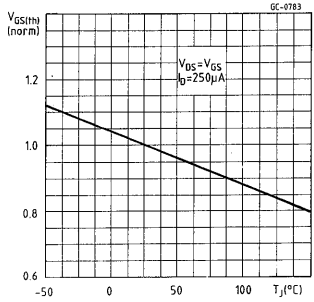
Gate charge vs gate-source voltage



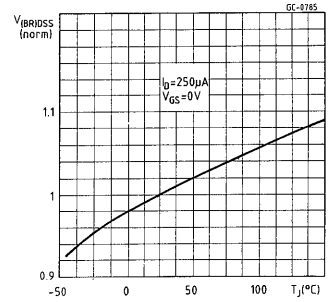
Capacitance variation



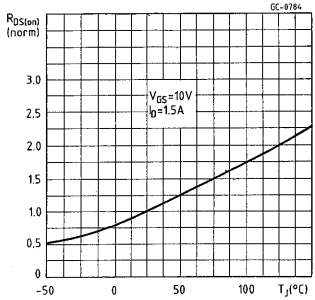
Normalized gate threshold voltage vs temperature



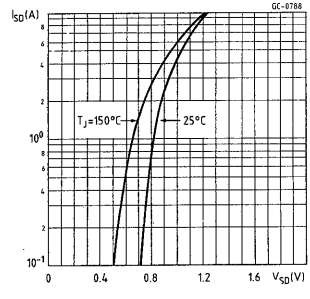
Normalized breakdown voltage vs temperature



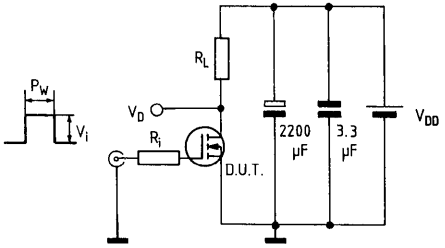
Normalized on resistance vs temperature



Source-drain diode forward characteristics

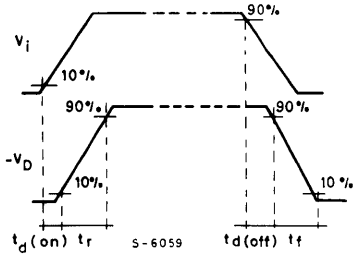


Switching times test circuit for resistive load

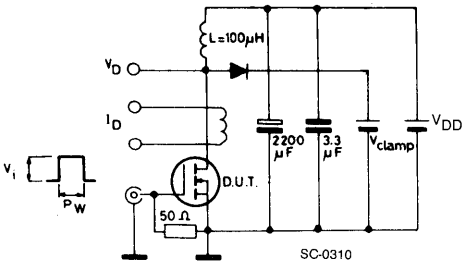


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

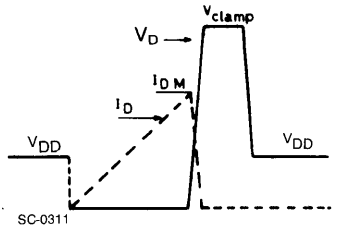


Clamped inductive load test circuit

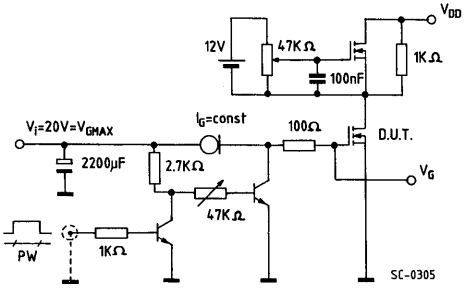


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

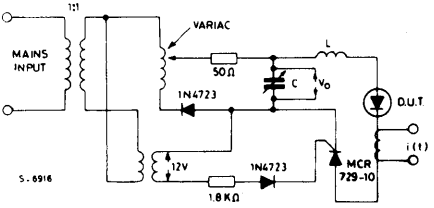


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP301

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

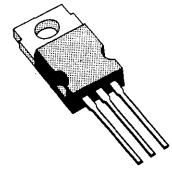
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP301	100 V	1.4 Ω	2.0 A

- HIGH SPEED SWITCHING APPLICATIONS
- GENERAL PURPOSE APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

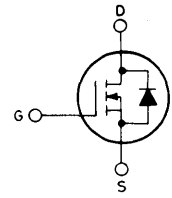
- GENERAL PURPOSE SWITCHING

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include general purpose low voltage switching, solenoid driving, motor and lamp control, switching power supplies, and driving, bipolar power switching transistors.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	2.0	A
I_D	Drain current (cont.) at $T_c=100°C$	1.2	A
I_{DM} (•)	Drain current (pulsed)	6	A
I_{DLM} (•)	Drain inductive current, clamped	6	A
P_{tot}	Total dissipation at $T_c<25°C$	18	W
	Derating factor	0.144	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	6.95	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

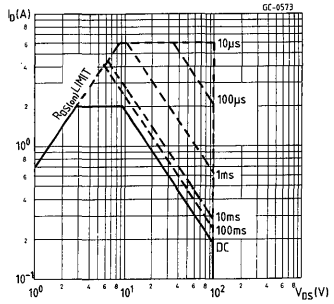
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.2 A V_{GS} = 10 V I_D = 1.2 A T_c = 100°C			1.4 2.8	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 1.2 A	0.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		90	125 45 30	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 50 V I_D = 1.2 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 20 15 15	15 30 20 20	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

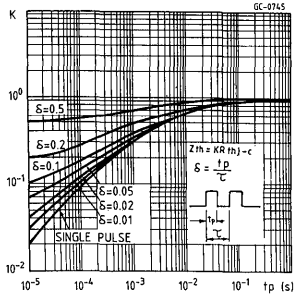
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				2.0 6	A A
V_{SD} Forward on voltage	I_{SD} = 2.5 A V_{GS} = 0			1.35	V
t_{rr} Reverse recovery time	I_{SD} = 2.5 A V_{GS} = 0 di/dt = 25 A/μs		90		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

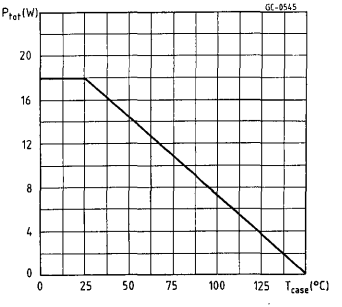
Safe operating areas



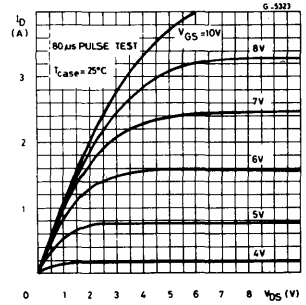
Thermal impedance



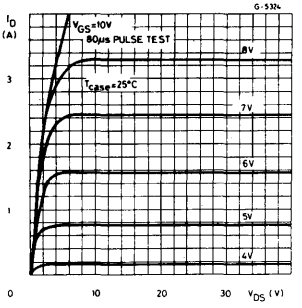
Derating curve



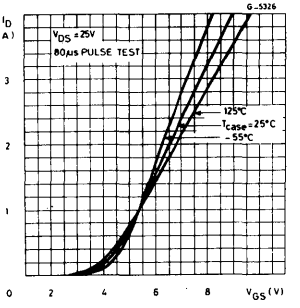
Output characteristics



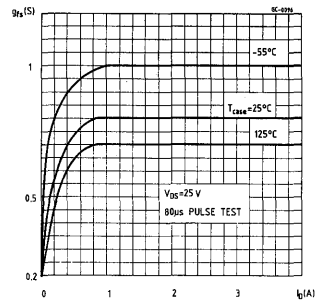
Output characteristics



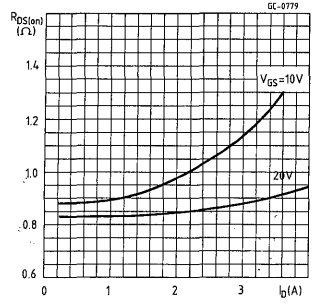
Transfer characteristics



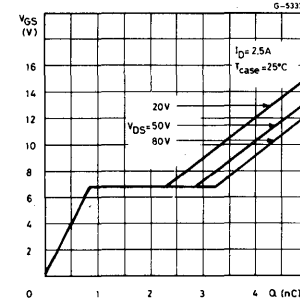
Transconductance



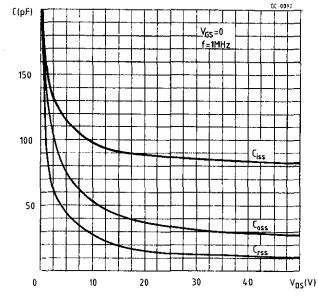
Static drain-source on resistance



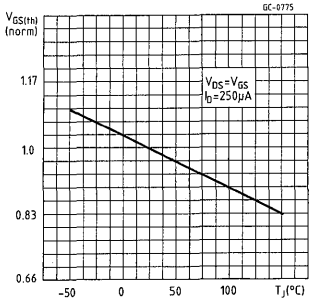
Gate charge vs gate-source voltage



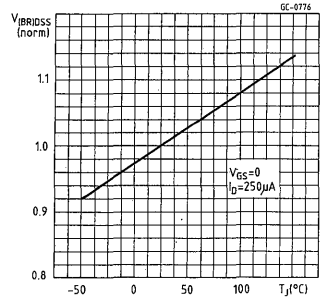
Capacitance variation



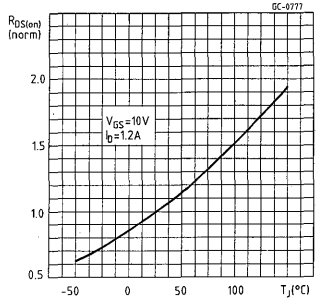
Normalized gate threshold voltage vs temperature



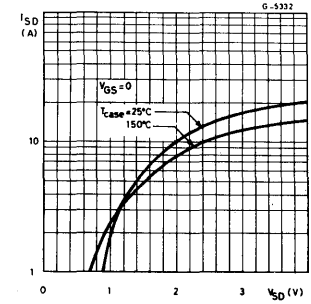
Normalized breakdown voltage vs temperature



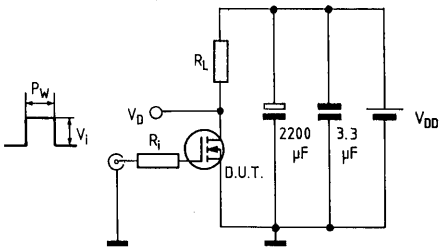
Normalized on resistance vs temperature



Source-drain diode forward characteristics

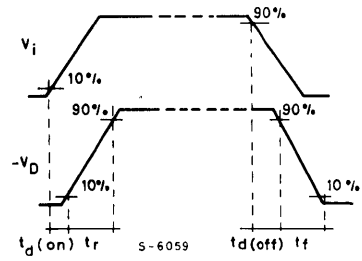


Switching times test circuit for resistive load

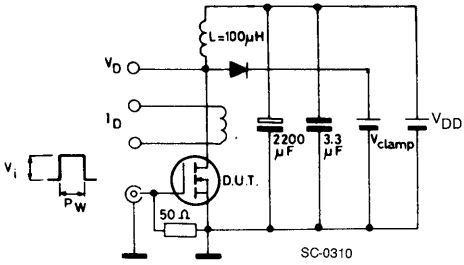


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

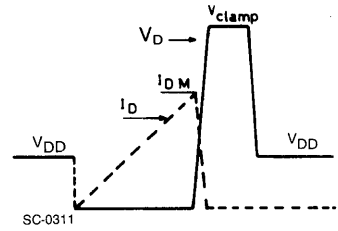


Clamped inductive load test circuit

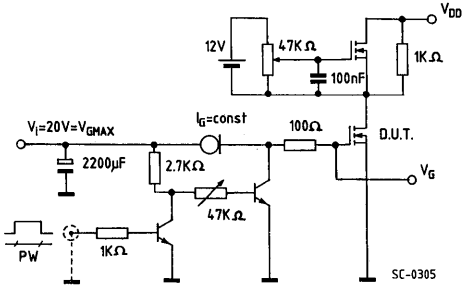


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

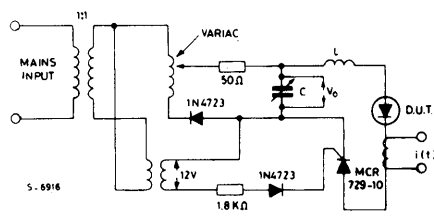


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP311

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

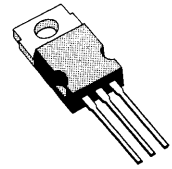
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP311	100 V	0.3 Ω	11 A

- HIGH SPEED SWITCHING APPLICATIONS
- 100V FOR DC/DC CONVERTERS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

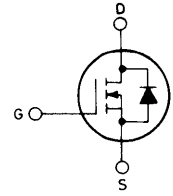
- SWITCHING MODE POWER SUPPLIES
- STEPPER MOTOR CONTROL

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical uses include DC/DC converters, stepper motors and solenoid drives.



T0-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	11	A
I_D	Drain current (cont.) at $T_c=100°C$	7	A
I_{DM} (•)	Drain current (pulsed)	30	A
P_{tot}	Total dissipation at $T_c<25°C$	75	W
	Derating factor	0.6	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1989 week 1

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.67	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

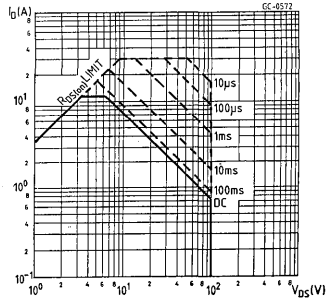
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5.5 A V_{GS} = 10 V I_D = 5.5 A T_c = 100°C			0.3 0.6	Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	11			A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5.5 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		375	480 230 110	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 50 V I_D = 5.5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		15 40 40 20	20 55 55 30	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

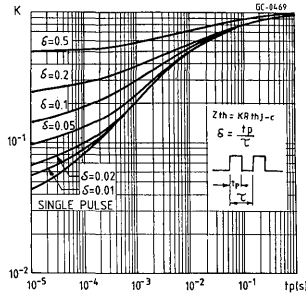
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				11 44	A A
V_{SD} Forward on voltage	I_{SD} = 11 A V_{GS} = 0			1.35	V
t_{rr} Reverse recovery time	I_{SD} = 11 A V_{GS} = 0 di/dt = 25 A/μs		140		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

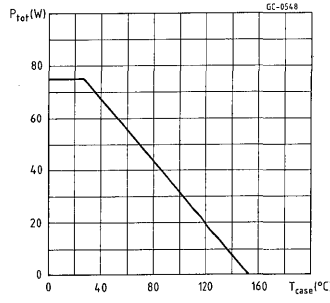
Safe operating areas



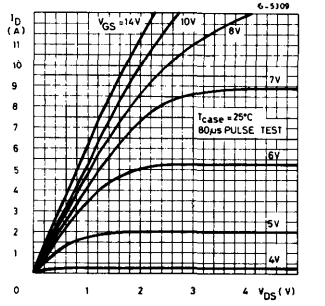
Thermal impedance



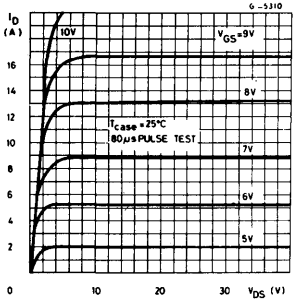
Derating curve



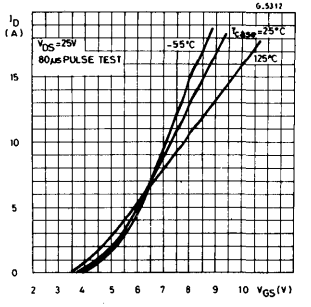
Output characteristics



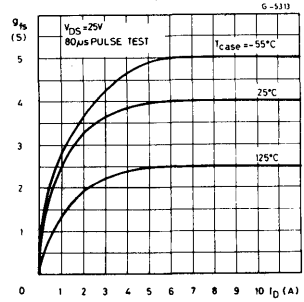
Output characteristics



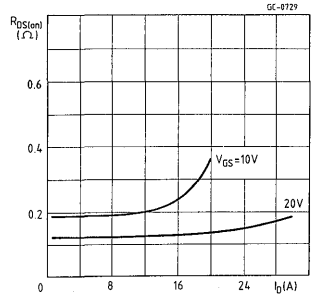
Transfer characteristics



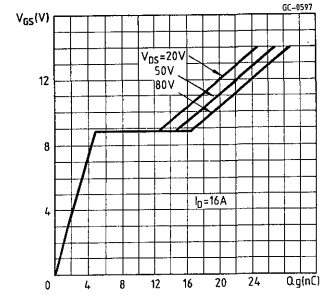
Transconductance



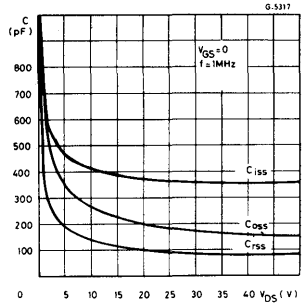
Static drain-source on resistance



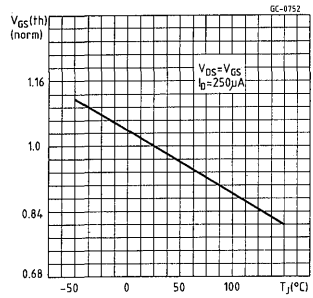
Gate charge vs gate-source voltage



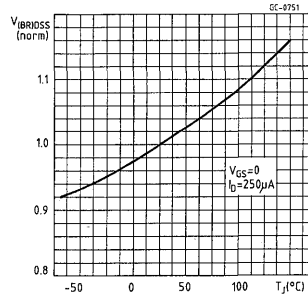
Capacitance variation



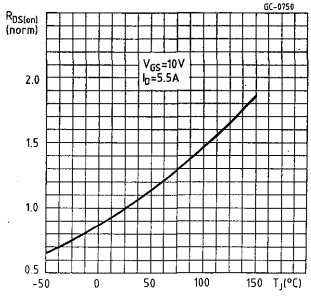
Normalized gate threshold voltage vs temperature



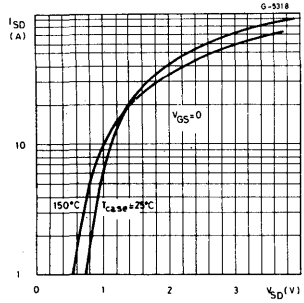
Normalized breakdown voltage vs temperature



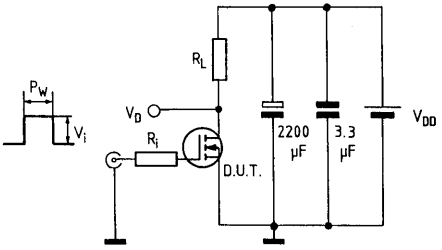
Normalized on resistance vs temperature



Source-drain diode forward characteristics

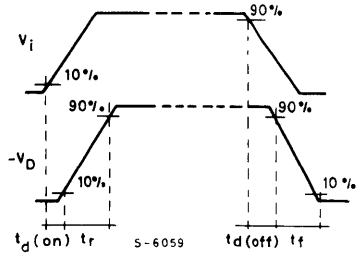


Switching times test circuit for resistive load

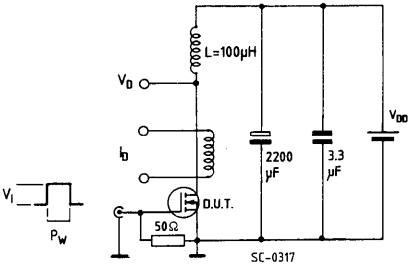


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

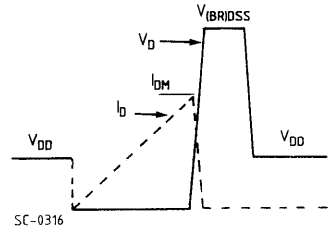


Unclamped inductive load test circuit

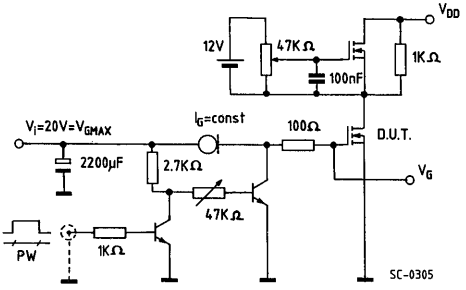


V_i= 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

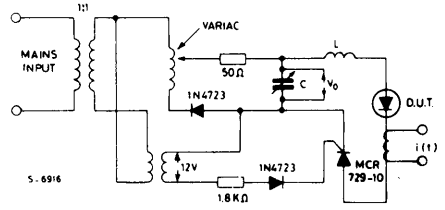


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP316
SGSP317

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

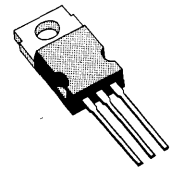
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP316	250 V	1.2 Ω	5 A
SGSP317	200 V	0.75 Ω	6 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE - REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

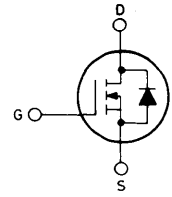
- SWITCHING POWER SUPPLIES
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses are in telecommunications, switching power supplies and as a DC switch.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP316	SGSP317	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	250	200	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	250	200	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	5	6	A
I_D	Drain current (cont.) at $T_c=100°C$	3.1	3.7	A
I_{DM} (•)	Drain current (pulsed)	20	24	A
P_{tot}	Total dissipation at $T_c<25°C$	75		W
	Derating factor	0.6		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.67	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

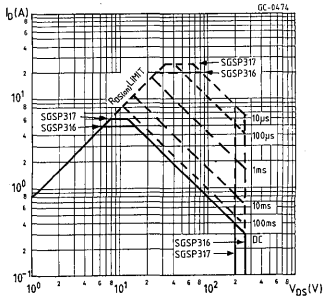
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP316** for **SGSP317**	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A for **SGSP316** I_D = 3 A for **SGSP317** V_{GS} = 10 V T_c = 100°C I_D = 2.5 A for **SGSP316** I_D = 3 A for **SGSP317**			 1.2 0.75 2.4 1.5	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP316** for **SGSP317**	 5 6			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 3 A	1.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		380	500 130 65	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

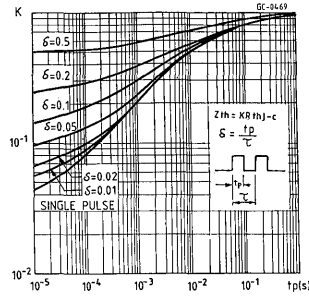
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 100 V I_D = 3 A		15	20	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		30	40	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		45	60	ns
t_f	Fall time			15	20	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP316**			5	A
		for **SGSP317**			6	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP316**			20	A
		for **SGSP317**			24	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 6 A for **SGSP316**			1.3	V
		I_{SD} = 5 A for **SGSP317**			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A V_{GS} = 0 di/dt = 100 A/μs		180		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

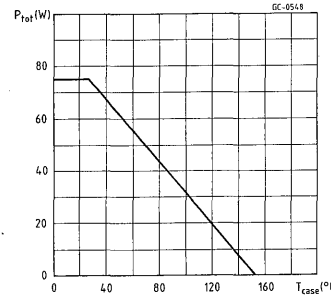
Safe operating areas



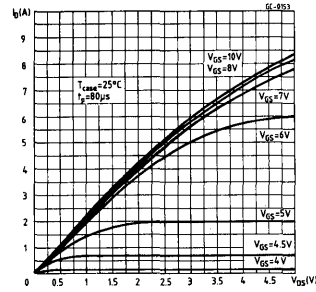
Thermal impedance



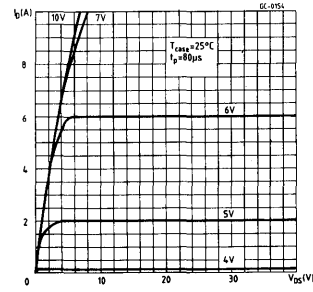
Derating curve



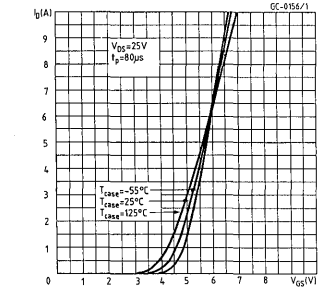
Output characteristics



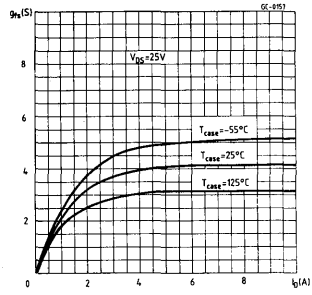
Output characteristics



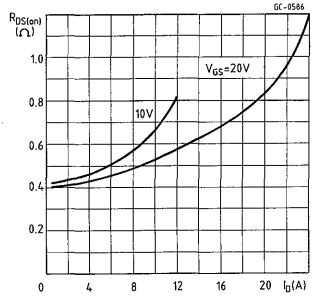
Transfer characteristics



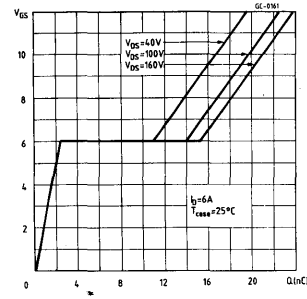
Transconductance



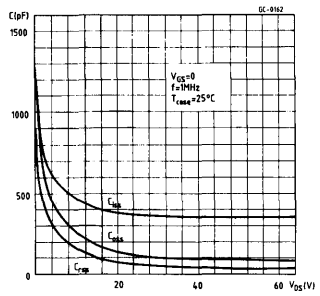
Static drain-source on resistance



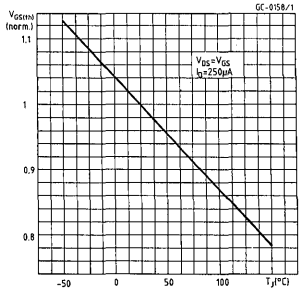
Gate charge vs gate-source voltage



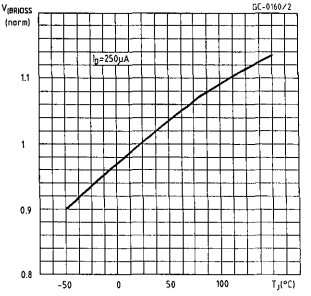
Capacitance variation



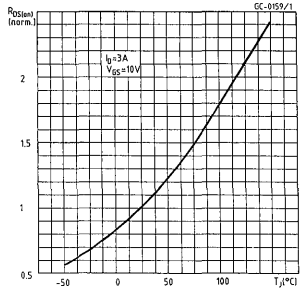
Normalized gate threshold voltage vs temperature



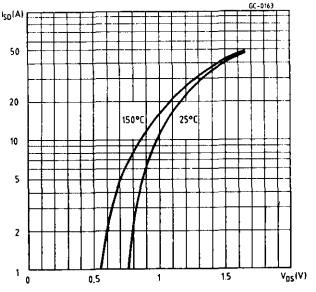
Normalized breakdown voltage vs temperature



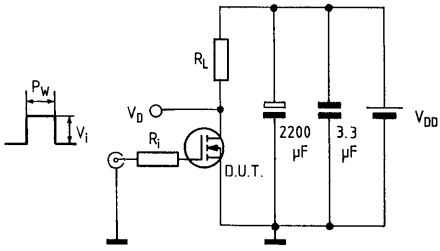
Normalized on resistance vs temperature



Source-drain diode forward characteristics

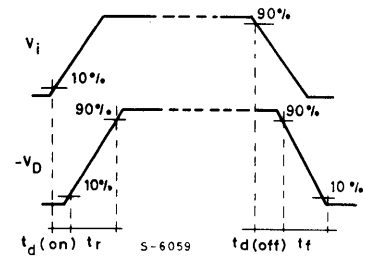


Switching times test circuit for resistive load

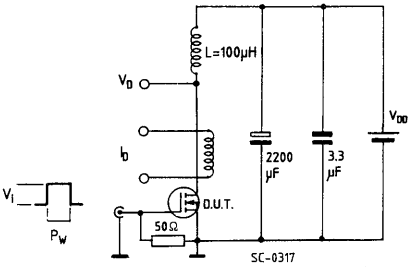


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

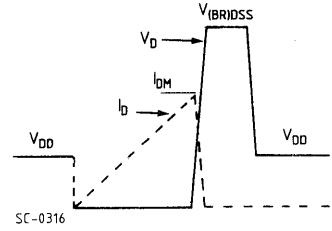


Unclamped inductive load test circuit

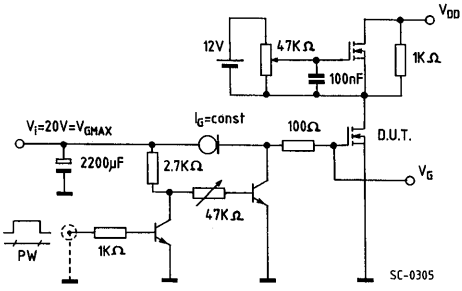


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

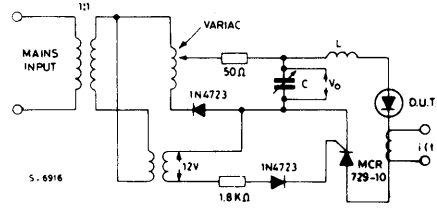


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP319

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

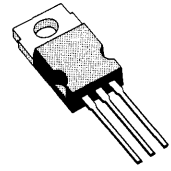
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP319	500 V	3.8 Ω	2.8 A

- HIGH SPEED SWITCHING APPLICATIONS
- 500V - HIGH VOLTAGE FOR SMPS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

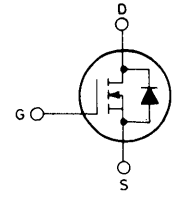
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching power supplies, battery chargers, motor speed control and solenoid drivers.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	2.8	A
I_D	Drain current (cont.) at $T_c = 100°C$	1.7	A
I_{DM} (•)	Drain current (pulsed)	11	A
I_{DLM} (•)	Drain inductive current, clamped	11	A
P_{tot}	Total dissipation at $T_c < 25°C$	75	W
	Derating factor	0.6	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

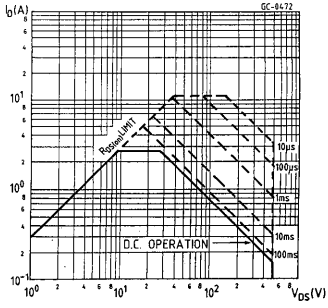
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.4 A V_{GS} = 10 V I_D = 1.4 A T_c = 100°C			3.8 7.2	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 1.4 A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		340	380 70 50	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 250 V I_D = 1.4 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		15 25 50 25	20 35 65 35	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

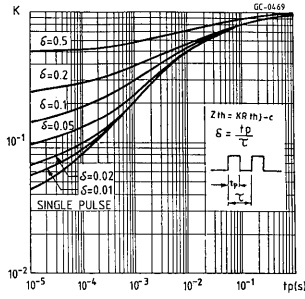
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				2.8 11	A A
V_{SD} Forward on voltage	I_{SD} = 2.8 A V_{GS} = 0			1.15	V
t_{rr} Reverse recovery time	I_{SD} = 2.8 A V_{GS} = 0 di/dt = 100 A/μs		360		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

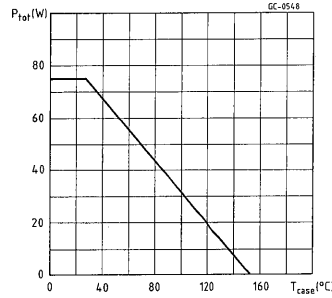
Safe operating areas



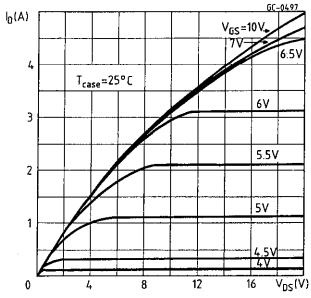
Thermal impedance



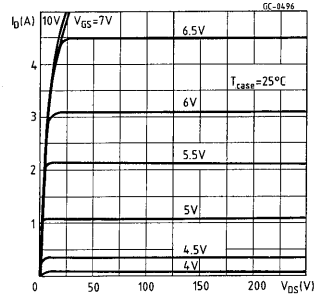
Derating curve



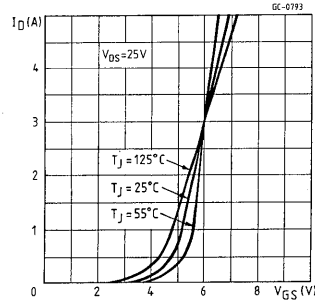
Output characteristics



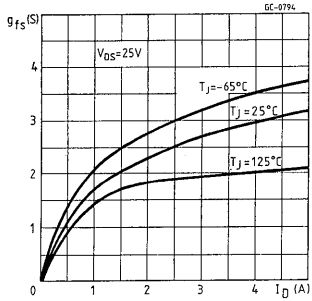
Output characteristics



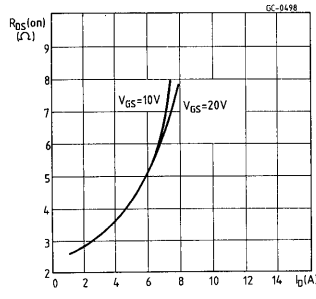
Transfer characteristics



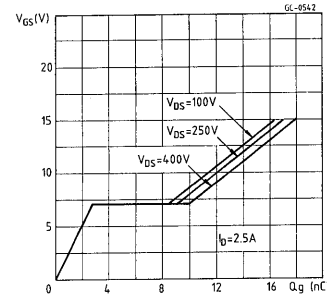
Transconductance



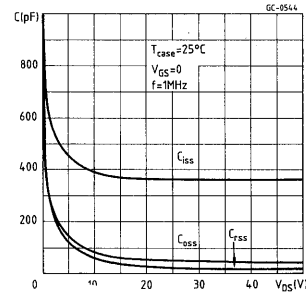
Static drain-source on resistance



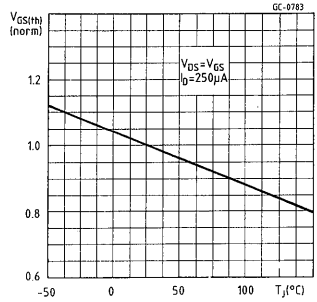
Gate charge vs gate-source voltage



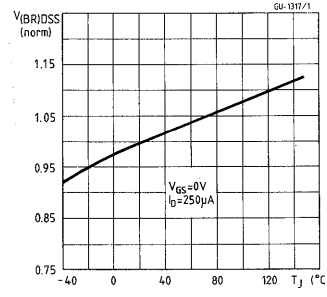
Capacitance variation



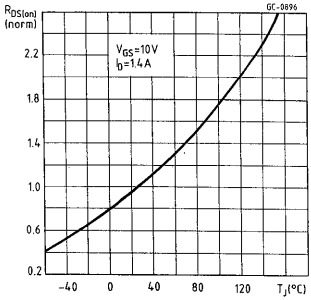
Normalized gate threshold voltage vs temperature



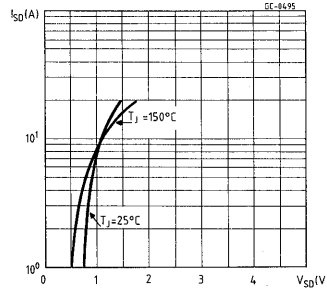
Normalized breakdown voltage vs temperature



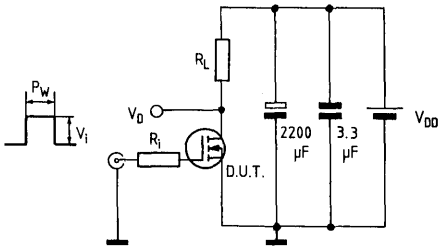
Normalized on resistance vs temperature



Source-drain diode forward characteristics

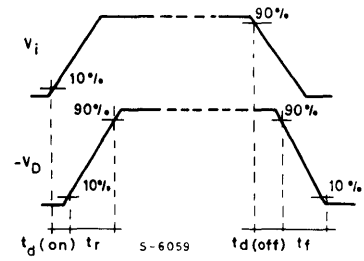


Switching times test circuit for resistive load

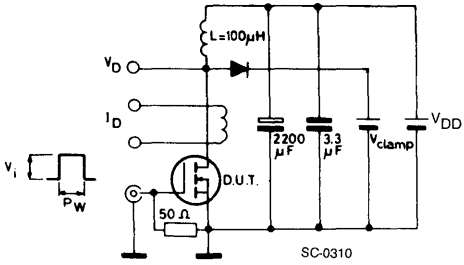


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

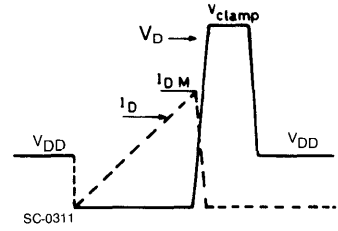


Clamped inductive load test circuit

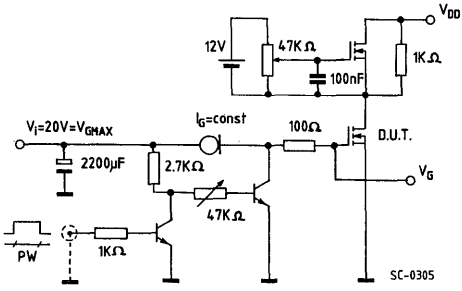


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

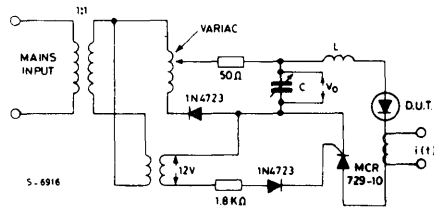


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP321
SGSP322

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

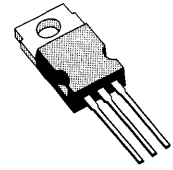
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP321	60 V	0.13 Ω	16 A
SGSP322	50 V	0.13 Ω	16 A

- HIGH SPEED SWITCHING APPLICATIONS
- LOW VOLTAGE DC/DC CONVERTERS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

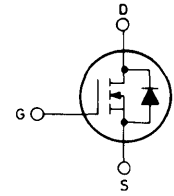
- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Uses include motor speed control, low voltage DC/DC converters and solenoid driving.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP321	SGSP322	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	16		A
I_D	Drain current (cont.) at $T_c=100°C$	10		A
I_{DM} (•)	Drain current (pulsed)	40		A
I_{DLM} (•)	Drain inductive current, clamped	40		A
P_{tot}	Total dissipation at $T_c<25°C$	75		W
	Derating factor	0.6		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

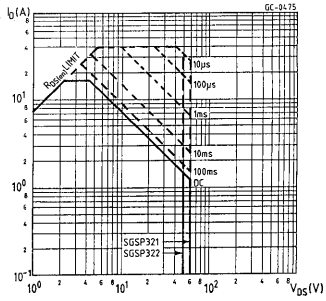
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP321** for **SGSP322**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 8 A V_{GS} = 10 V I_D = 8 A T_c = 100°C			0.13 0.26	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 8 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		460	550 350 180	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 8 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		15 45 40 25	20 60 55 35	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

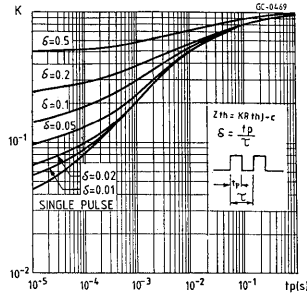
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					16 40	A A
V_{SD}	Forward on voltage	I_{SD} = 16 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A di/dt = 25 A/μs	V_{GS} = 0		100		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

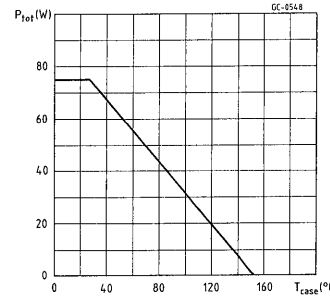
Safe operating areas



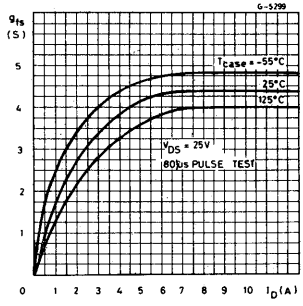
Thermal impedance



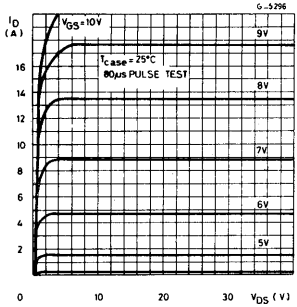
Derating curve



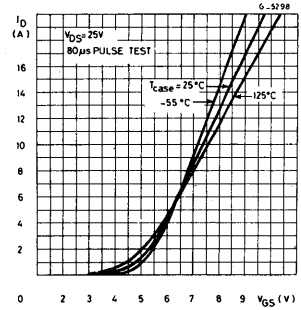
Output characteristics



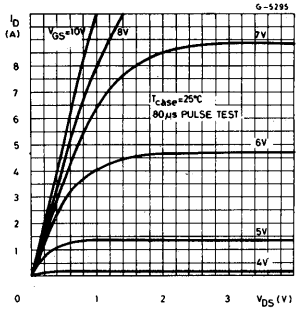
Output characteristics



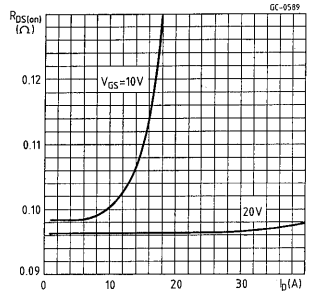
Transfer characteristics



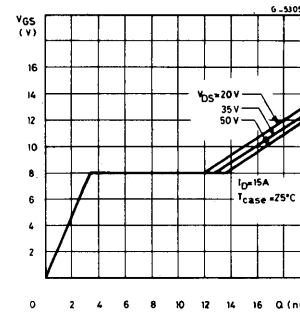
Transconductance



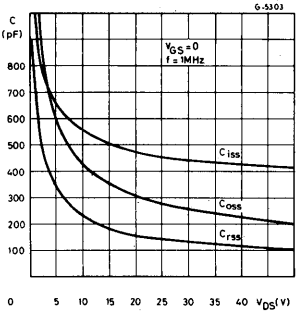
Static drain-source on resistance



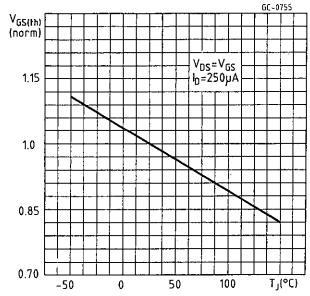
Gate charge vs gate-source voltage



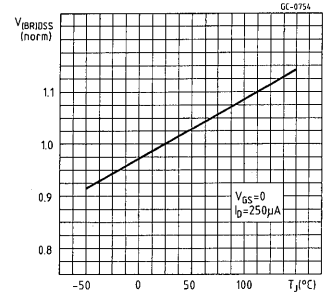
Capacitance variation



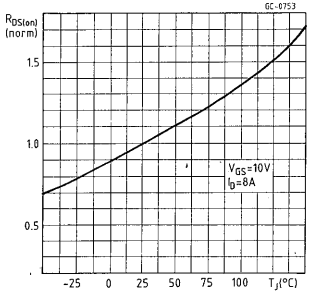
Normalized gate threshold voltage vs temperature



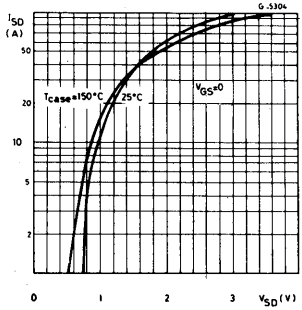
Normalized breakdown voltage vs temperature



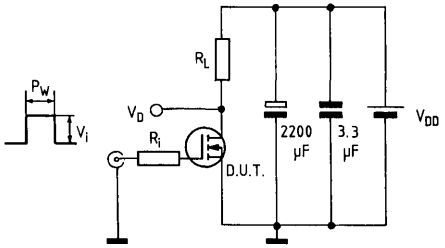
Normalized on resistance vs temperature



Source-drain diode forward characteristics

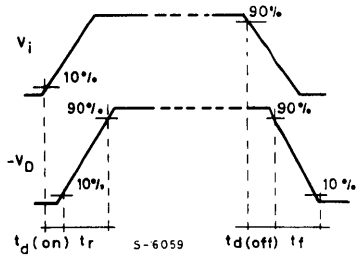


Switching times test circuit for resistive load

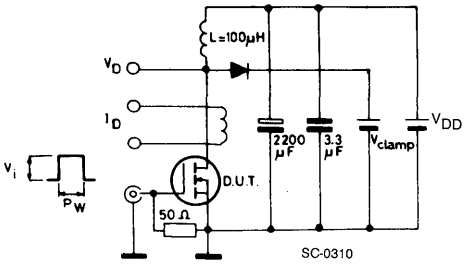


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

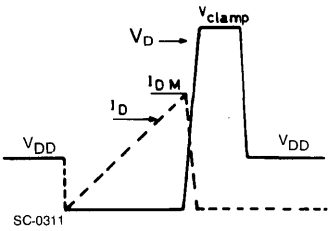


Clamped inductive load test circuit

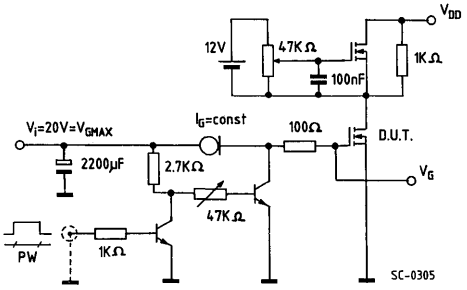


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

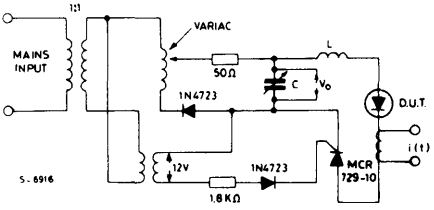


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP330

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

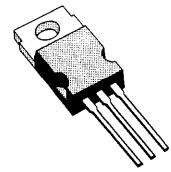
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP330	450 V	3 Ω	3 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 450V FOR OFF-LINE SMPS
- ULTRA FAST SWITCHING FOR OPERATION AT > 100KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching power supplies, uninterruptible power supplies and motor speed control.



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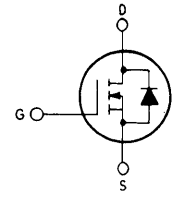
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	450	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	450	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	3	A
I_D	Drain current (cont.) at $T_c = 100°C$	1.9	A
I_{DM} (•)	Drain current (pulsed)	12	A
I_{DLM} (•)	Drain inductive current, clamped	12	A
P_{tot}	Total dissipation at $T_c < 25°C$	75	W
	Derating factor	0.6	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

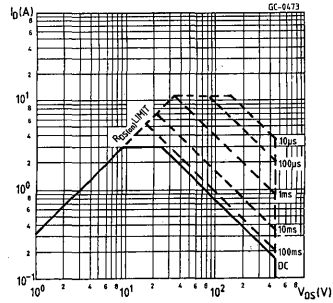
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	450			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1.5 A V_{GS} = 10 V I_D = 1.5 A T_c = 100°C			3 6	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 1.5 A	0.8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		340	450 95 50	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 1.5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 25 55 25	15 35 70 35	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

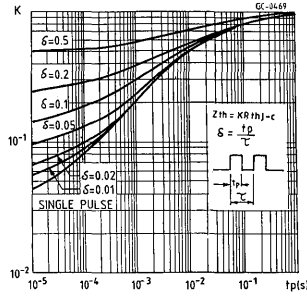
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				3 12	A A
V_{SD} Forward on voltage	I_{SD} = 3 A V_{GS} = 0			1.2	V
t_{rr} Reverse recovery time	I_{SD} = 3 A V_{GS} = 0 di/dt = 100 A/μs		360		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

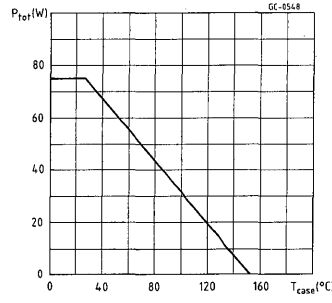
Safe operating areas



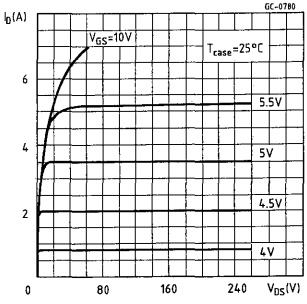
Thermal impedance



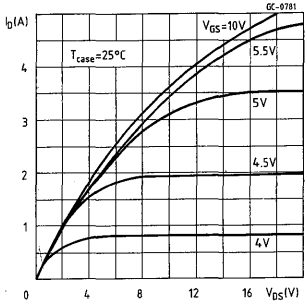
Derating curve



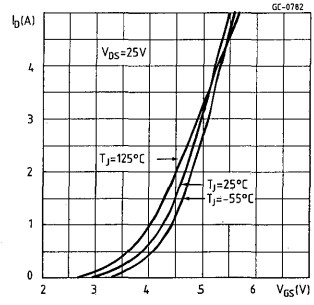
Output characteristics



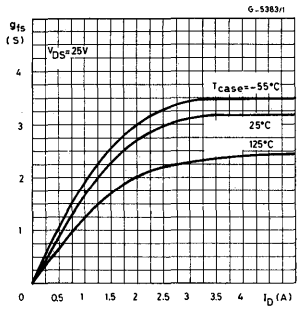
Output characteristics



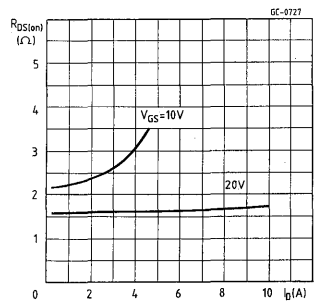
Transfer characteristics



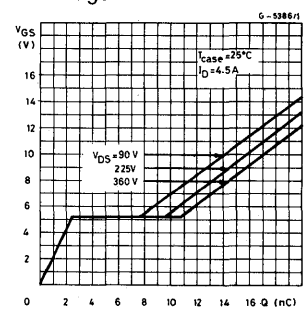
Transconductance



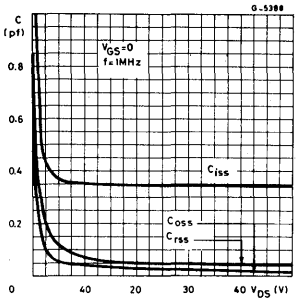
Static drain-source on resistance



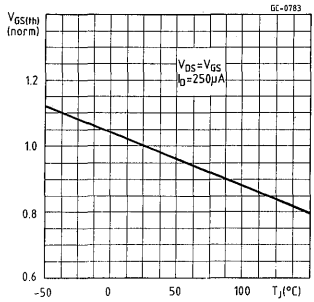
Gate charge vs gate-source voltage



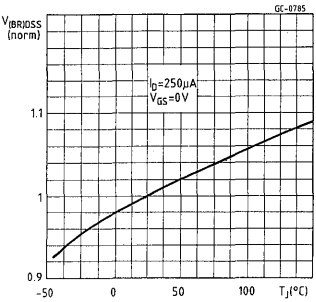
Capacitance variation



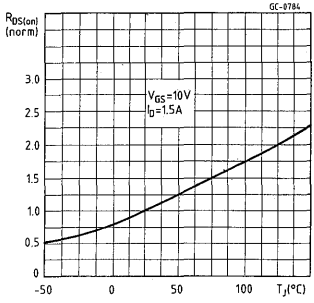
Normalized gate threshold voltage vs temperature



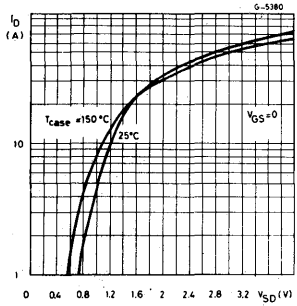
Normalized breakdown voltage vs temperature



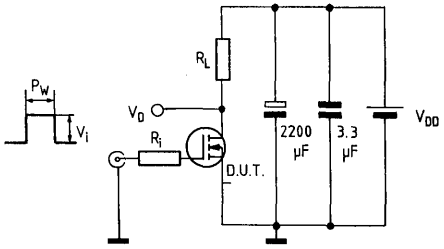
Normalized on resistance vs temperature



Source-drain diode forward characteristics

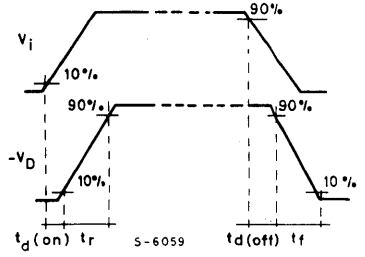


Switching times test circuit for resistive load

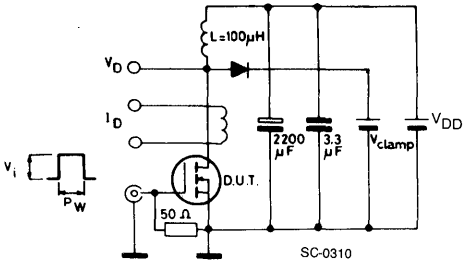


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

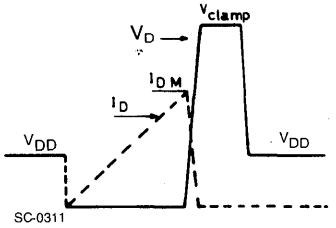


Clamped inductive load test circuit

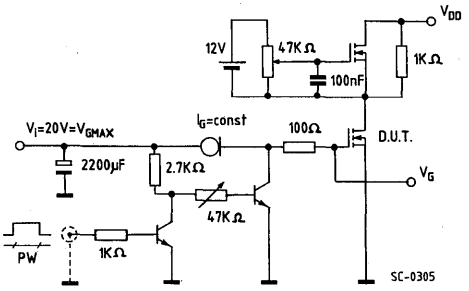


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

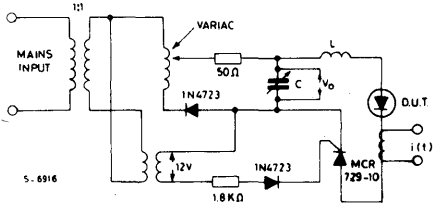


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP341

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

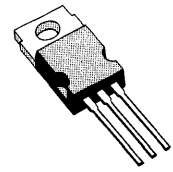
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP341	400 V	20 Ω	0.6 A

- HIGH SPEED SWITCHING APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

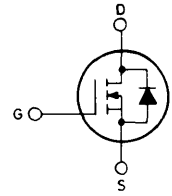
- GENERAL PURPOSE

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include motor starter and drive circuits for power bipolar transistors.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	400	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	0.6	A
I_D	Drain current (cont.) at $T_c=100°C$	0.4	A
I_{DM} (•)	Drain current (pulsed)	1.2	A
I_{DLM} (•)	Drain inductive current, clamped	1.2	A
P_{tot}	Total dissipation at $T_c<25°C$	18	W
	Derating factor	0.14	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	6.8	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

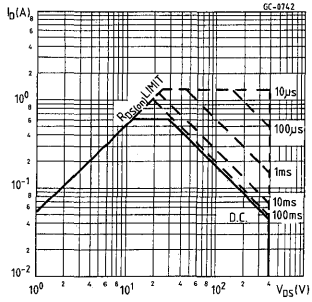
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 0.3 A V_{GS} = 10 V I_D = 0.3 A T_c = 100°C			20 40	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 0.3 A	0.1			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		80	105 20 15	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 200 V I_D = 0.3 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 15 25 40	15 20 35 55	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

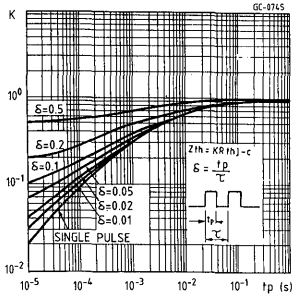
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				0.6 1.2	A A
V_{SD} Forward on voltage	I_{SD} = 0.6 A V_{GS} = 0			1.2	V
t_{rr} Reverse recovery time	I_{SD} = 0.6 A V_{GS} = 0 di/dt = 100 A/μs		140		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

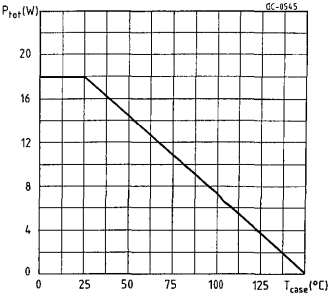
Safe operating areas



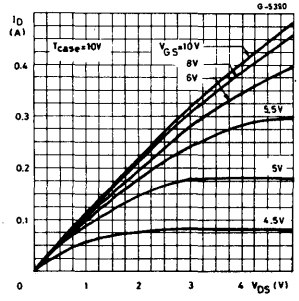
Thermal impedance



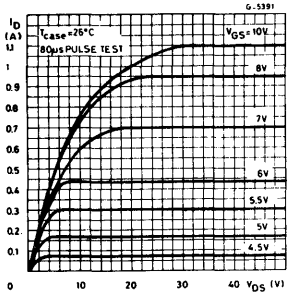
Derating curve



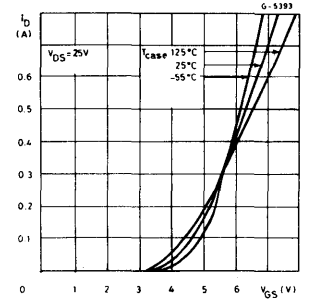
Output characteristics



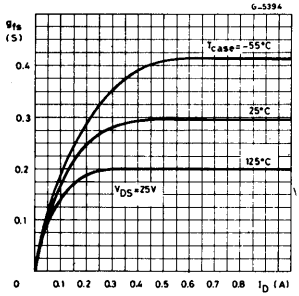
Output characteristics



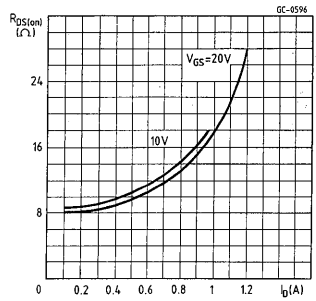
Transfer characteristics



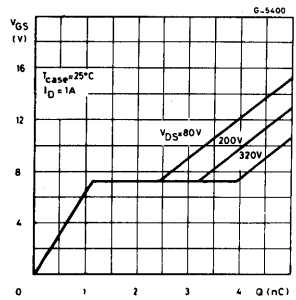
Transconductance



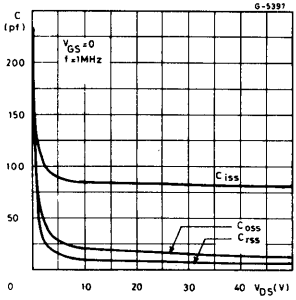
Static drain-source on resistance



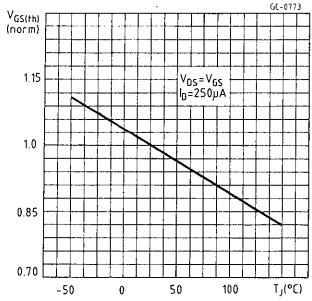
Gate charge vs gate-source voltage



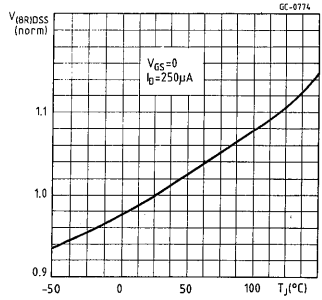
Capacitance variation



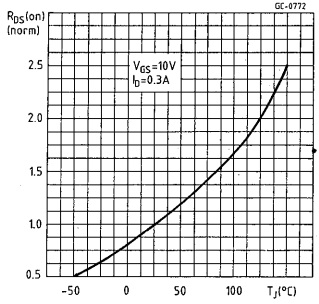
Normalized gate threshold voltage vs temperature



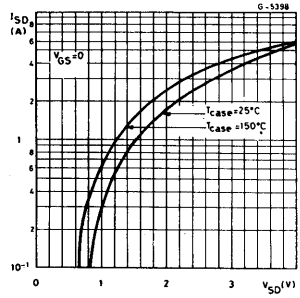
Normalized breakdown voltage vs temperature



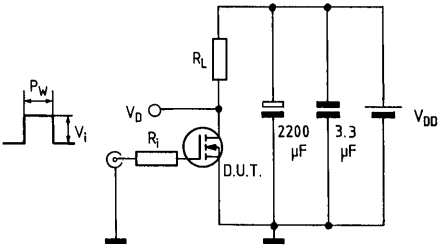
Normalized on resistance vs temperature



Source-drain diode forward characteristics

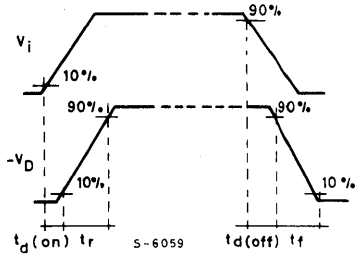


Switching times test circuit for resistive load

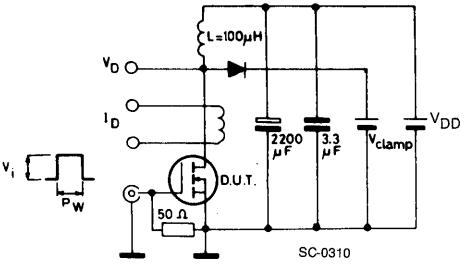


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

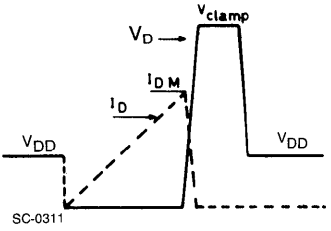


Clamped inductive load test circuit

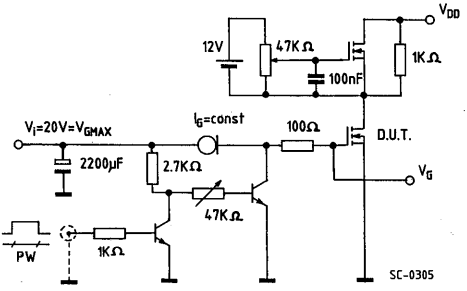


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

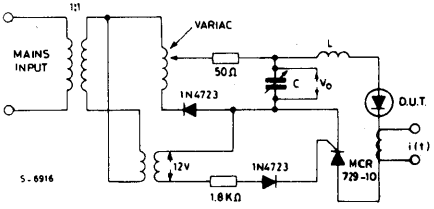


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP351

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

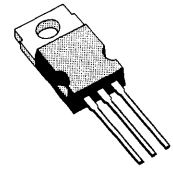
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP351	100 V	0.6 Ω	6 A

- HIGH SPEED SWITCHING APPLICATIONS
- DC/DC APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

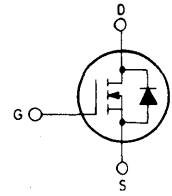
- SWITCHING POWER SUPPLIES
- MOTOR CONTROL

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include stepper motor and printer hammer drives and switching power supplies



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	6	A
I_D	Drain current (cont.) at $T_c=100°C$	4	A
I_{DM} (•)	Drain current (pulsed)	24	A
I_{DLM} (•)	Drain inductive current, clamped	24	A
P_{tot}	Total dissipation at $T_c<25°C$	50	W
	Derating factor	0.4	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	2.5	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

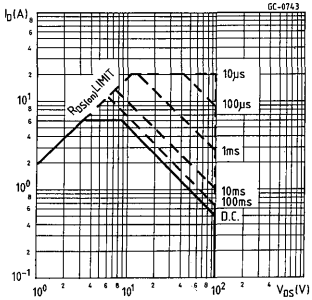
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3 A V_{GS} = 10 V I_D = 3 A T_c = 100°C			0.6 1.2	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 3 A	1			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		180	250 100 40	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 50 V I_D = 3 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 25 25 15	15 35 35 20	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

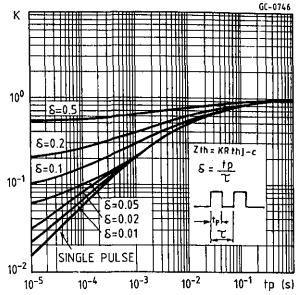
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				6 24	A A
V_{SD} Forward on voltage	I_{SD} = 6 A V_{GS} = 0			1.35	V
t_{rr} Reverse recovery time	I_{SD} = 6 A V_{GS} = 0 di/dt = 25 A/μs		120		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

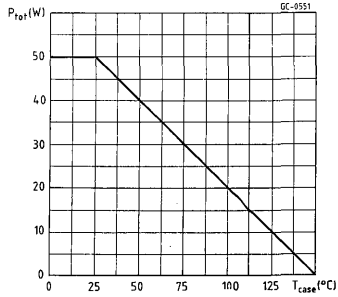
Safe operating areas



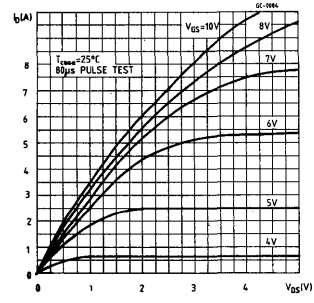
Thermal impedance



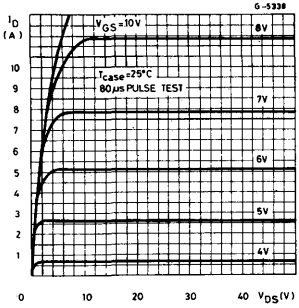
Derating curve



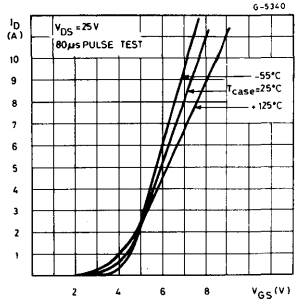
Output characteristics



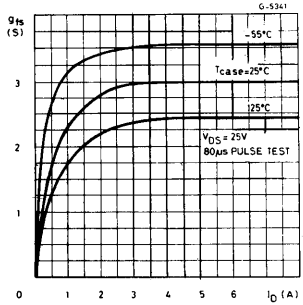
Output characteristics



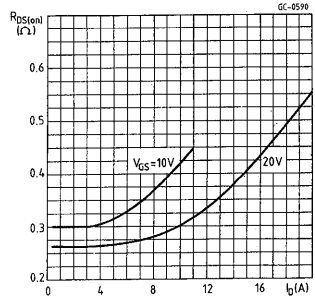
Transfer characteristics



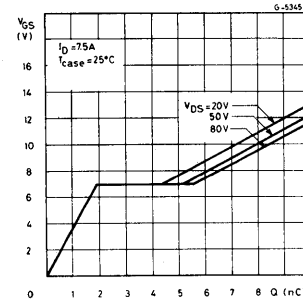
Transconductance



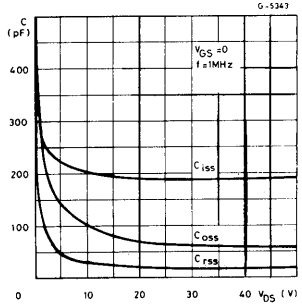
Static drain-source on resistance



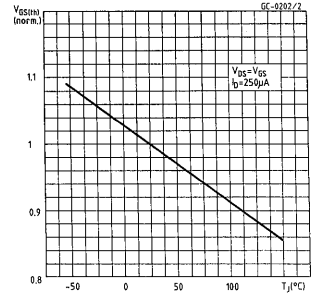
Gate charge vs gate-source voltage



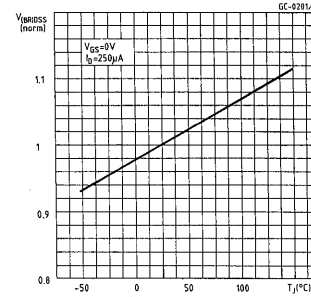
Capacitance variation



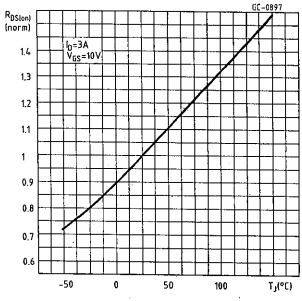
Normalized gate threshold voltage vs temperature



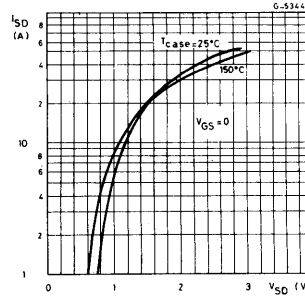
Normalized breakdown voltage vs temperature



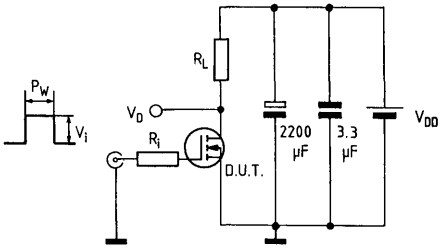
Normalized on resistance vs temperature



Source-drain diode forward characteristics

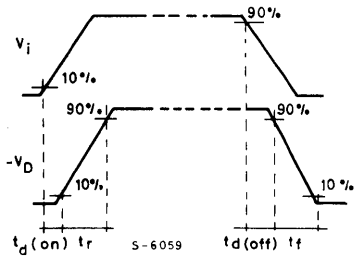


Switching times test circuit for resistive load

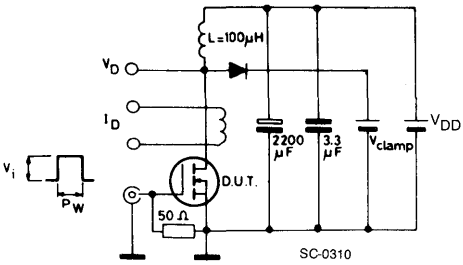


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

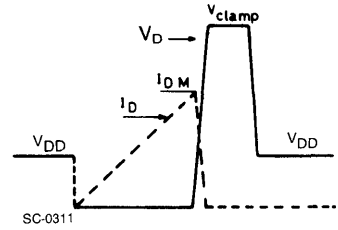


Clamped inductive load test circuit

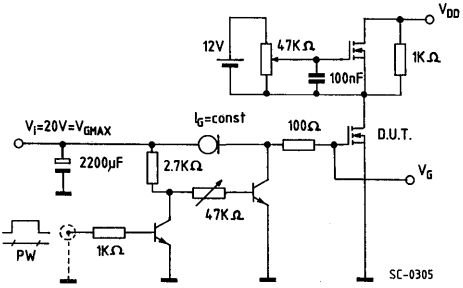


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

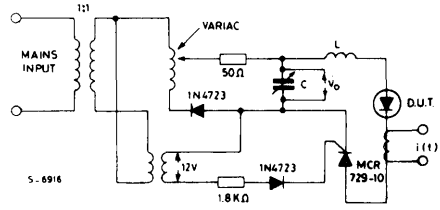


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP358

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

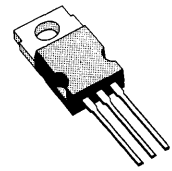
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP358	50 V	0.3 Ω	7 A

- HIGH SPEED SWITCHING APPLICATIONS
- GENERAL PURPOSE
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

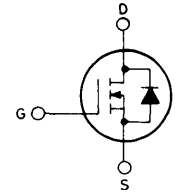
- D.C. SWITCH
- UNINTERRUPTIBLE POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include DC switching, uninterruptible power supplies and drive circuits for power bipolar transistor.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	7	A
I_D	Drain current (cont.) at $T_c=100°C$	4.4	A
I_{DM} (•)	Drain current (pulsed)	28	A
I_{DLM} (•)	Drain inductive current, clamped	28	A
P_{tot}	Total dissipation at $T_c<25°C$	50	W
	Derating factor	0.4	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	2.5	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

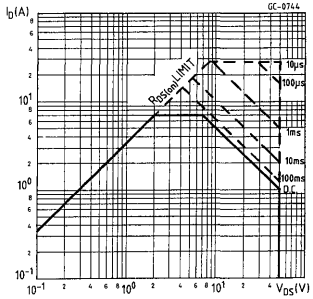
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 3.5 A V_{GS} = 10 V I_D = 3.5 A T_c = 100°C			0.3 0.6	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 3.5 A	1.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		210	270 150 70	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 3.5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		10 35 20 15	15 45 30 20	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

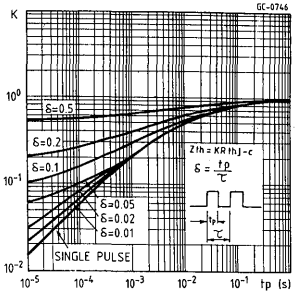
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				7 28	A A
V_{SD} Forward on voltage	I_{SD} = 7 A V_{GS} = 0			1.4	V
t_{rr} Reverse recovery time	I_{SD} = 7 A V_{GS} = 0 di/dt = 25 A/μs		65		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

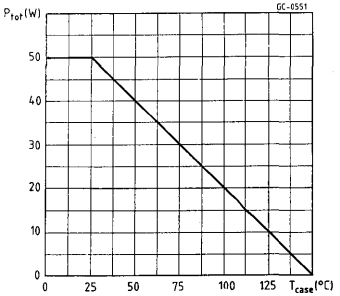
Safe operating areas



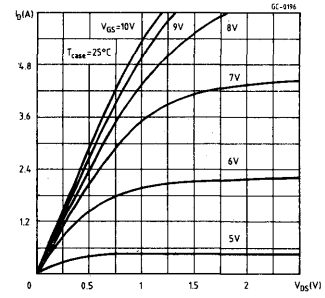
Thermal impedance



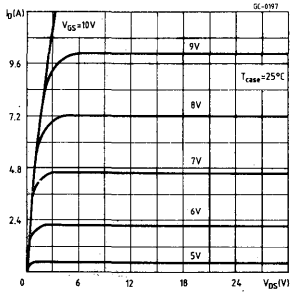
Derating curve



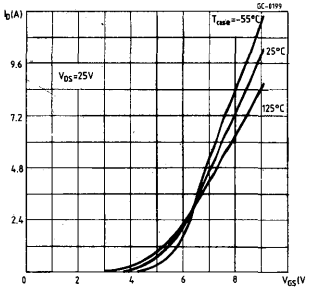
Output characteristics



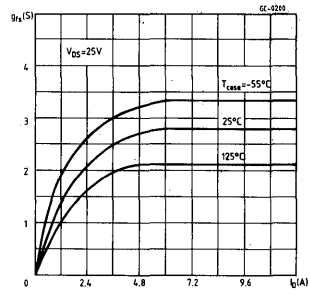
Output characteristics



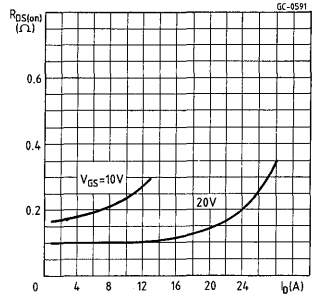
Transfer characteristics



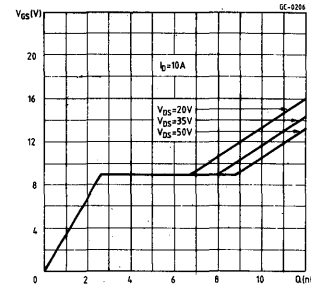
Transconductance



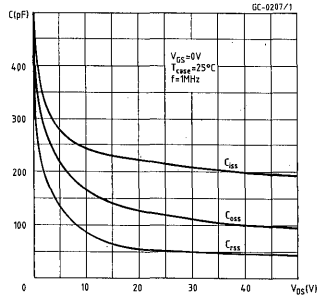
Static drain-source on resistance



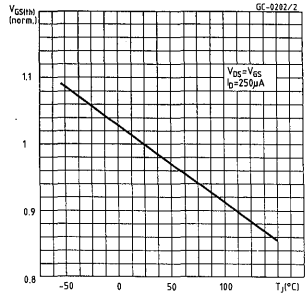
Gate charge vs gate-source voltage



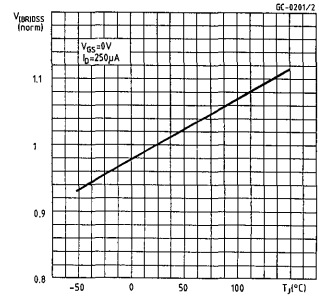
Capacitance variation



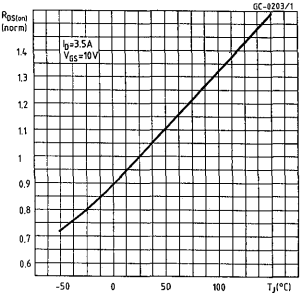
Normalized gate threshold voltage vs temperature



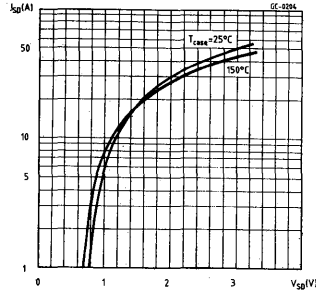
Normalized breakdown voltage vs temperature



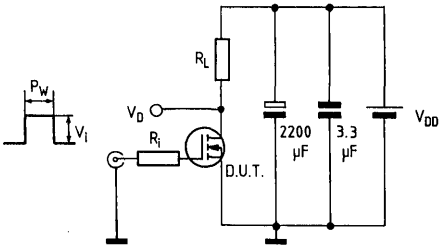
Normalized on resistance vs temperature



Source-drain diode forward characteristics

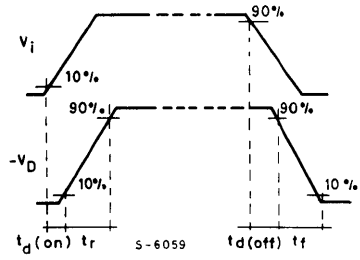


Switching times test circuit for resistive load

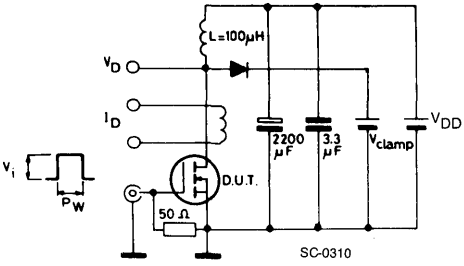


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

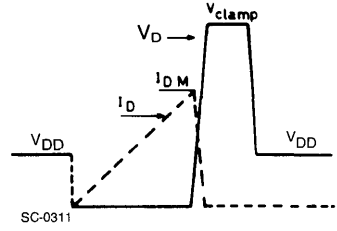


Clamped inductive load test circuit

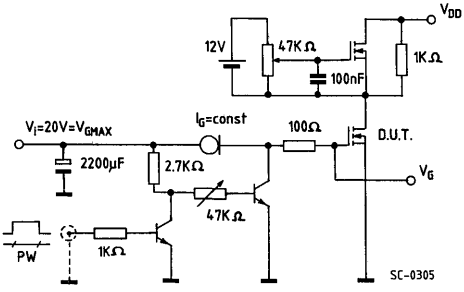


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

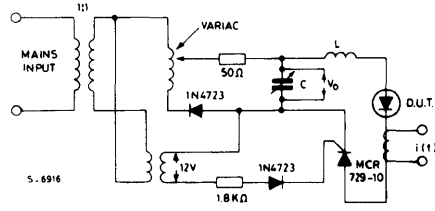


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP361
SGSP362

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

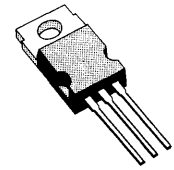
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP361	100 V	0.15 Ω	18 A
SGSP362	80 V	0.1 Ω	22 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- ULTRA FAST SWITCHING
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

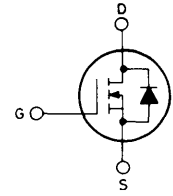
- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP361	SGSP362	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	18	22	A
I_D	Drain current (cont.) at $T_c=100°C$	11	14	A
I_{DM} (•)	Drain current (pulsed)	72	88	A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

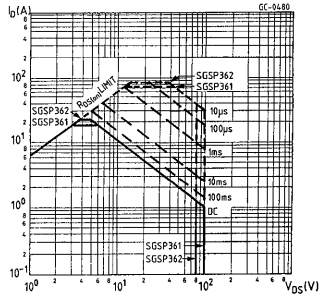
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP361** for **SGSP362**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 9 A for **SGSP361** I_D = 11 A for **SGSP362** V_{GS} = 10 V T_c = 100°C I_D = 9 A for **SGSP361** I_D = 11 A for **SGSP362**			 0.15 0.1 0.3 0.2	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP361** for **SGSP362**	 18 22			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 9 A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

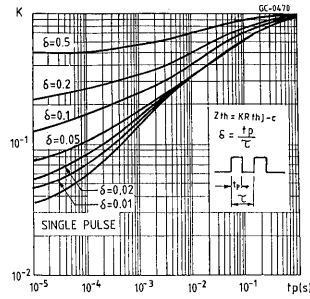
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 11 A		20	30	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		50	65	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			25	35	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP361**			18	A
		for **SGSP362**			22	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP361**			72	A
		for **SGSP362**			88	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 18 A for **SGSP361**			1.35	V
		I_{SD} = 22 A for **SGSP362**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 22 A V_{GS} = 0 di/dt = 25 A/μs		180		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

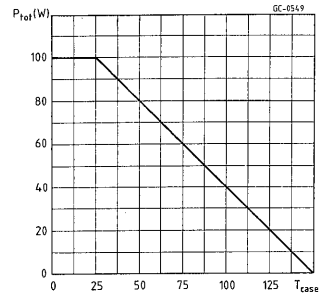
Safe operating areas



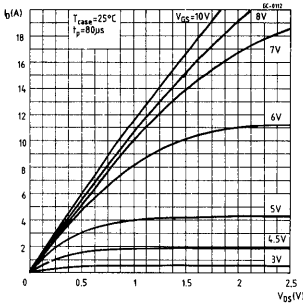
Thermal impedance



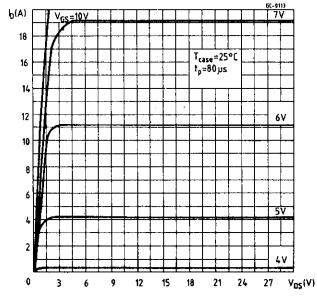
Derating curve



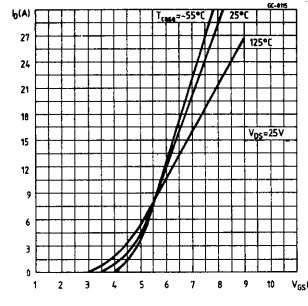
Output characteristics



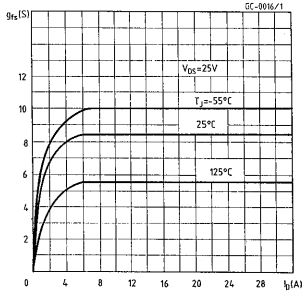
Output characteristics



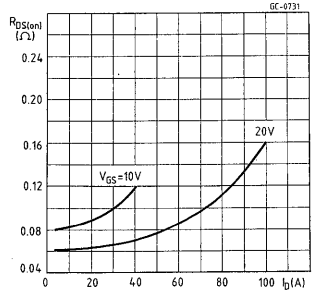
Transfer characteristics



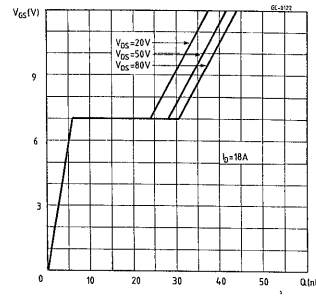
Transconductance



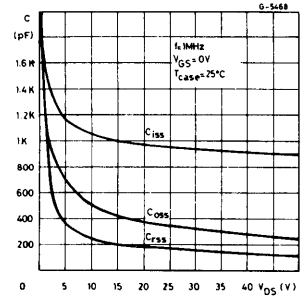
Static drain-source on resistance



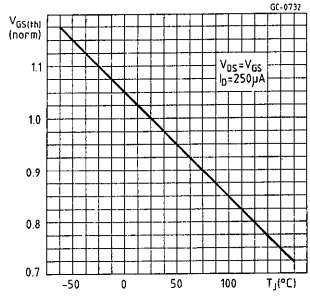
Gate charge vs gate-source voltage



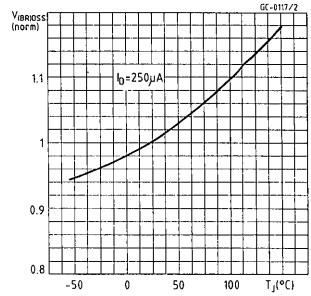
Capacitance variation



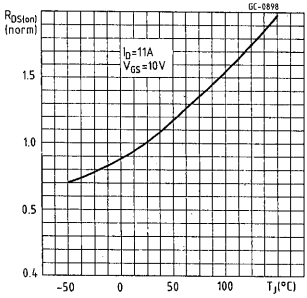
Normalized gate threshold voltage vs temperature



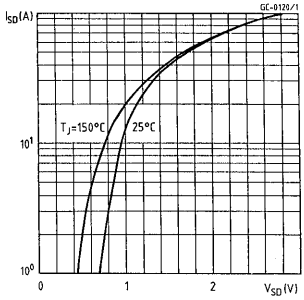
Normalized breakdown voltage vs temperature



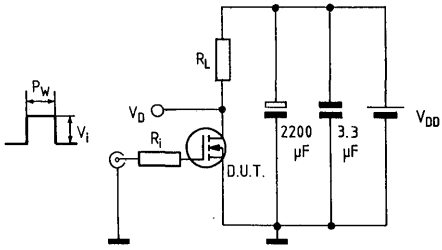
Normalized on resistance vs temperature



Source-drain diode forward characteristics

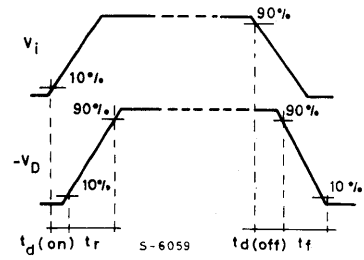


Switching times test circuit for resistive load

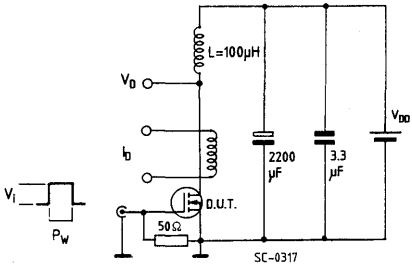


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

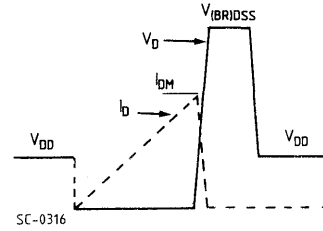


Unclamped inductive load test circuit

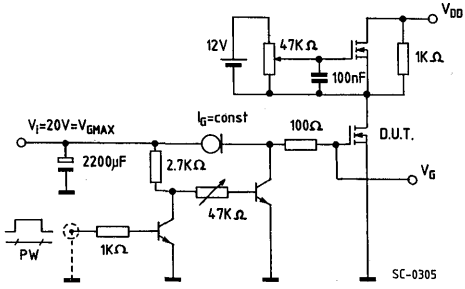


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

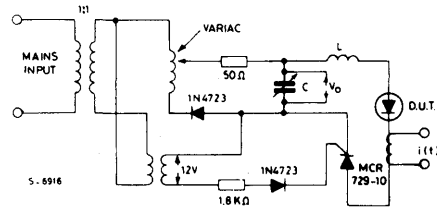


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP363
SGSP367

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

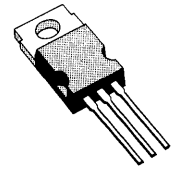
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP363	250 V	0.45 Ω	10 A
SGSP367	200 V	0.33 Ω	12 A

- HIGH SPEED SWITCHING APPLICATIONS
- TELECOMMUNICATION APPLICATIONS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- ROBOTICS
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include robotics, uninterruptible power supplies, motor control and solenoid drives.



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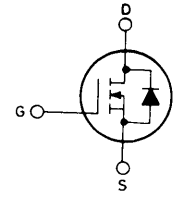
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP363	SGSP367	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	250	200	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	250	200	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	10	12	A
I_D	Drain current (cont.) at $T_c=100°C$	6.3	7.5	A
I_{DM} (•)	Drain current (pulsed)	40	48	A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1989 week 1

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

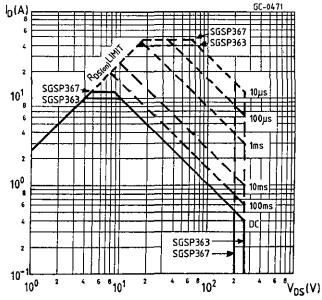
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP363** for **SGSP367**	 250 200			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 5 A for **SGSP363** I_D = 6 A for **SGSP367** V_{GS} = 10 V T_c = 100°C I_D = 5 A for **SGSP363** I_D = 6 A for **SGSP367**			 0.45 0.33 0.9 0.66	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP363** for **SGSP367**	 10 12			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 6 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		980	1200 260 100	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

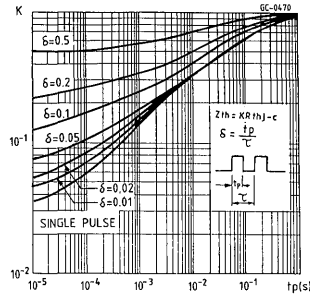
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 100 V I_D = 6 A		20	30	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		40	55	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			20	30	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP363**			10	A
		for **SGSP367**			12	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP363**			40	A
		for **SGSP367**			48	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 10 A for **SGSP363**			1.3	V
		I_{SD} = 12 A for **SGSP367**			1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A V_{GS} = 0 di/dt = 100 A/μs		250		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

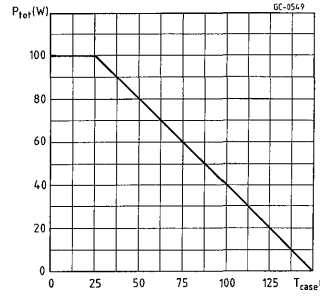
Safe operating areas



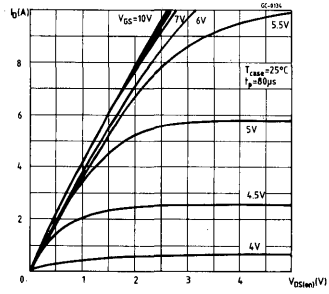
Thermal impedance



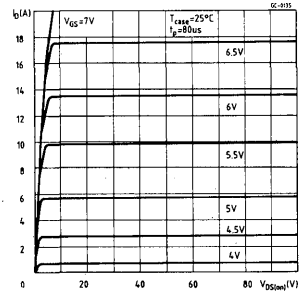
Derating curve



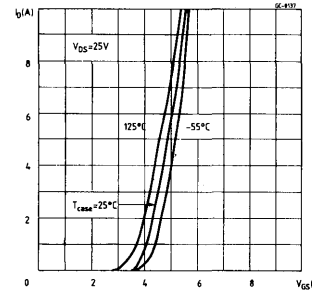
Output characteristics



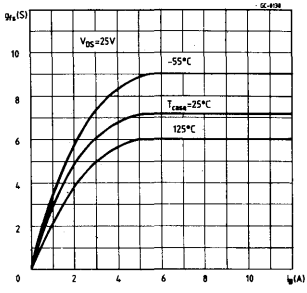
Output characteristics



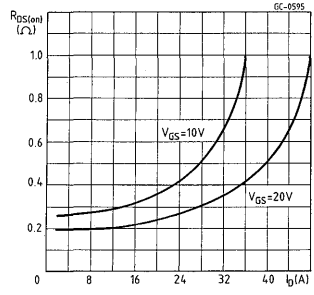
Transfer characteristics



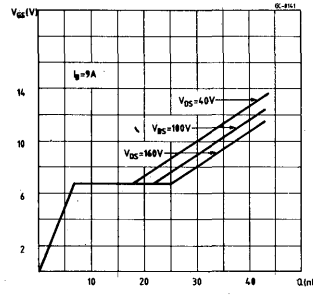
Transconductance



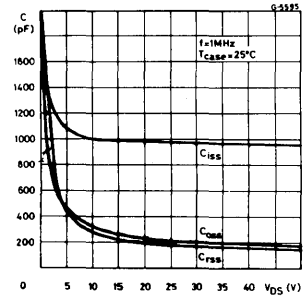
Static drain-source on resistance



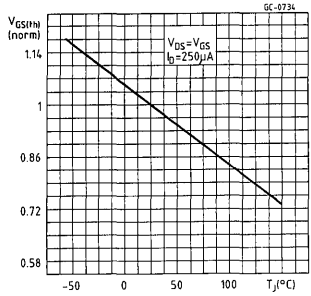
Gate charge vs gate-source voltage



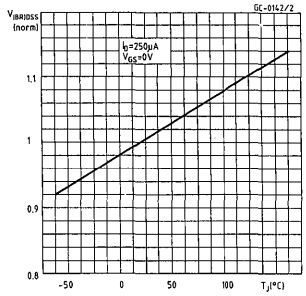
Capacitance variation



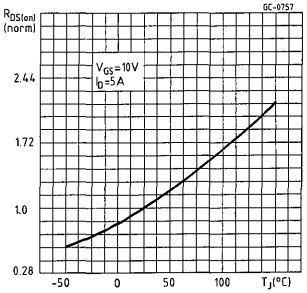
Normalized gate threshold voltage vs temperature



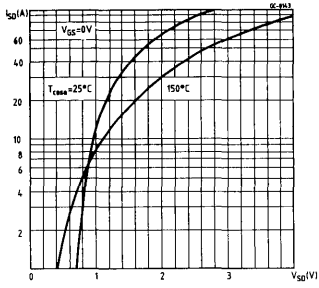
Normalized breakdown voltage vs temperature



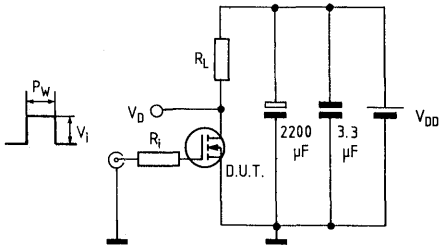
Normalized on resistance vs temperature



Source-drain diode forward characteristics

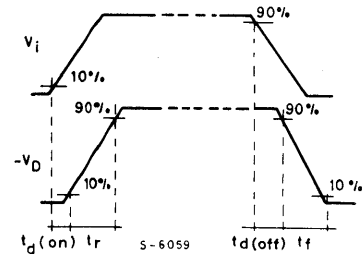


Switching times test circuit for resistive load

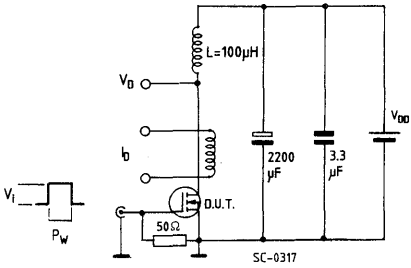


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

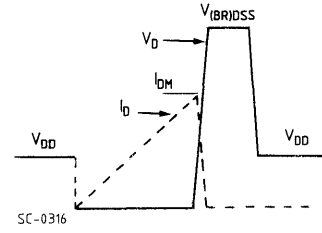


Unclamped inductive load test circuit

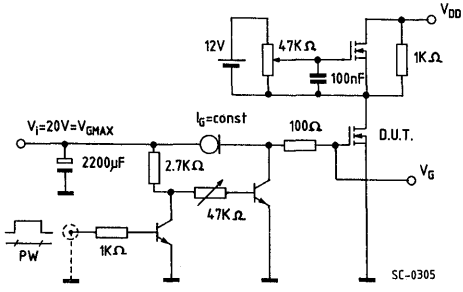


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

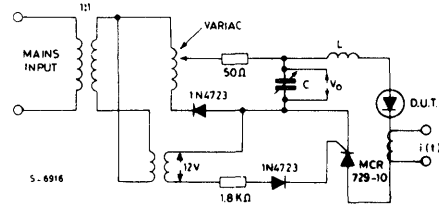


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP364
SGSP369

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

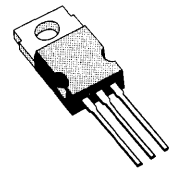
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP364	450 V	1.5 Ω	5 A
SGSP369	500 V	1.5 Ω	5 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - FOR ELECTRONIC LAMP BALLAST
- ULTRA FAST SWITCHING
- EASY DRIVE - REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

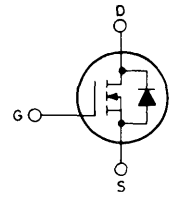
- ELECTRONIC LAMP BALLAST
- DC SWITCH

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC switch, constant current source, ultrasonic equipment and electronic ballast for fluorescent lamps.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP364	SGSP369	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	450	500	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	450	500	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	5		A
I_D	Drain current (cont.) at $T_c=100°C$	3		A
I_{DM} (•)	Drain current (pulsed)	20		A
I_{DLM} (•)	Drain inductive current, clamped	20		A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

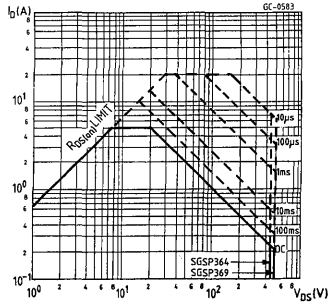
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP364** for **SGSP369**	 450 500			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 2.5 A V_{GS} = 10 V I_D = 2.5 A T_c = 100°C			1.5 3	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 2.5 A	3			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		780	1000 200 130	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 250 V I_D = 2.5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		20 30 85 25	30 40 110 35	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

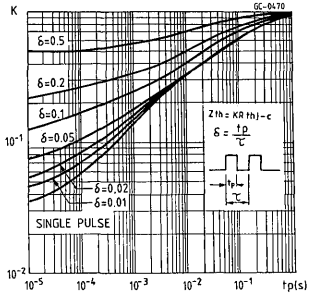
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				5 20	A A
V_{SD} Forward on voltage	I_{SD} = 5 A V_{GS} = 0			1.2	V
t_{rr} Reverse recovery time	I_{SD} = 5 A V_{GS} = 0 di/dt = 100 A/μs		470		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

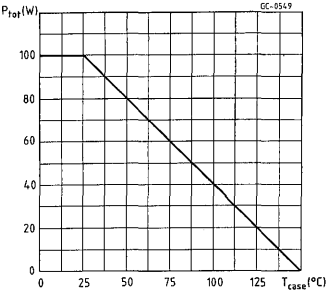
Safe operating areas



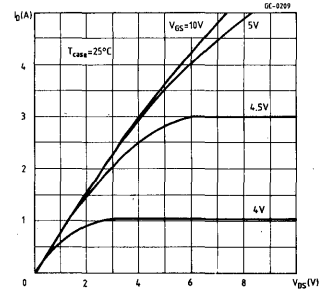
Thermal impedance



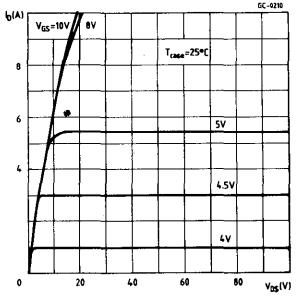
Derating curve



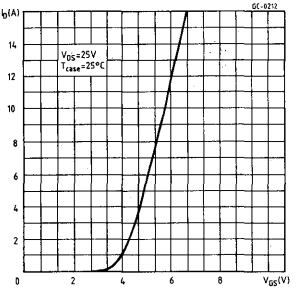
Output characteristics



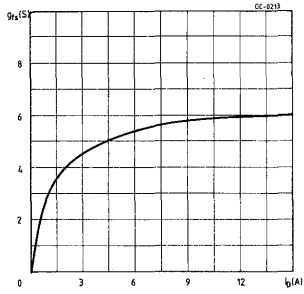
Output characteristics



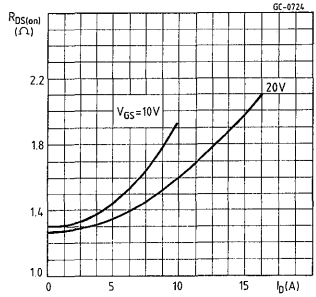
Transfer characteristics



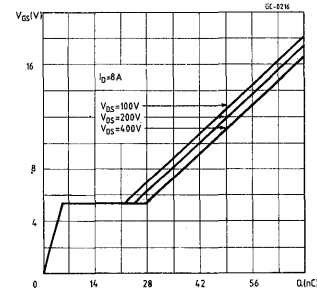
Transconductance



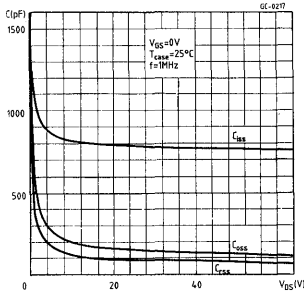
Static drain-source on resistance



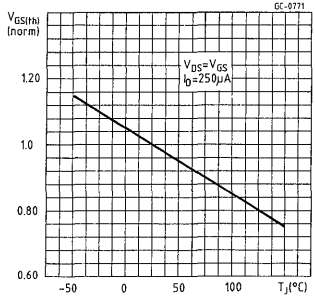
Gate charge vs gate-source voltage



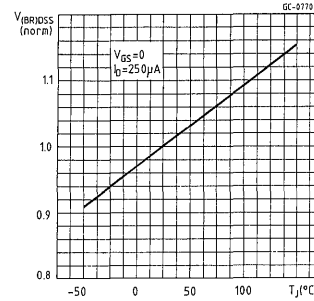
Capacitance variation



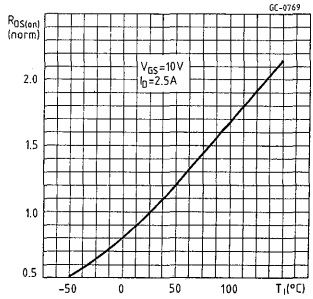
Normalized gate threshold voltage vs temperature



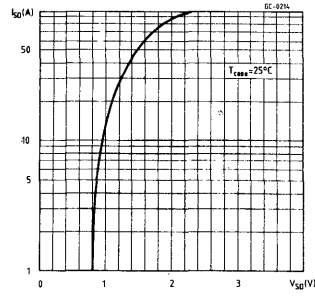
Normalized breakdown voltage vs temperature



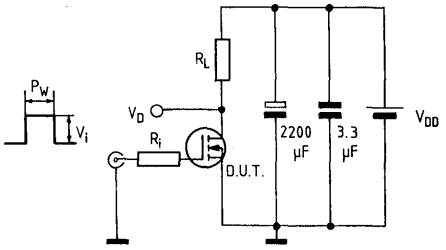
Normalized on resistance vs temperature



Source-drain diode forward characteristics

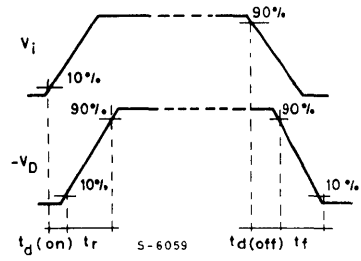


Switching times test circuit for resistive load

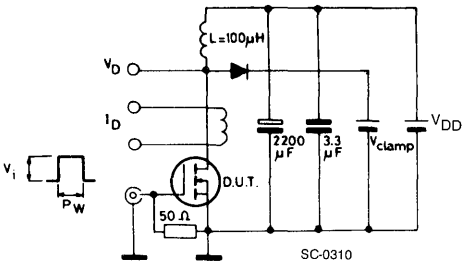


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

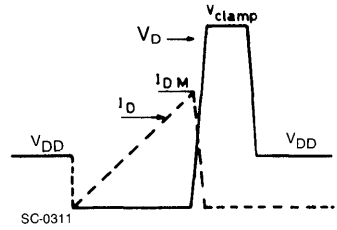


Clamped inductive load test circuit

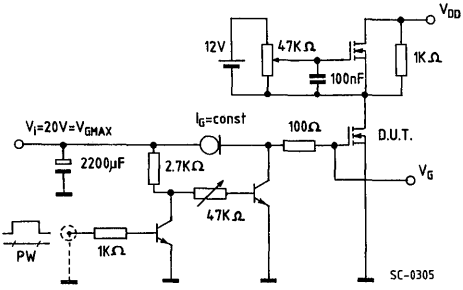


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

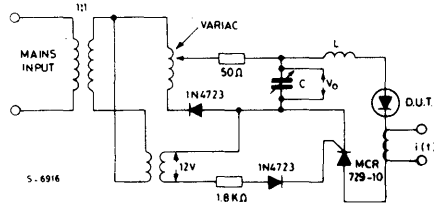


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP381
SGSP382

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

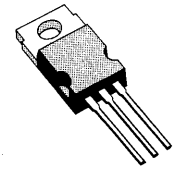
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP381	60 V	0.06 Ω	28 A
SGSP382	50 V	0.06 Ω	28 A

- HIGH SPEED SWITCHING APPLICATIONS
- 60 VOLTS - DC/DC AND UPS APPLICATIONS
- HIGH CURRENT
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

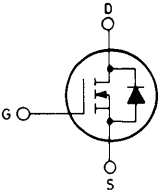
- DC/DC CONVERTERS AND UPS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include UPS, battery chargers, printer mechanism drives and motor speed control



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP381	SGSP382	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	28		A
I_D	Drain current (cont.) at $T_c=100°C$	17		A
I_{DM} (•)	Drain current (pulsed)	112		A
I_{DLM} (•)	Drain inductive current, clamped	112		A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.25	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

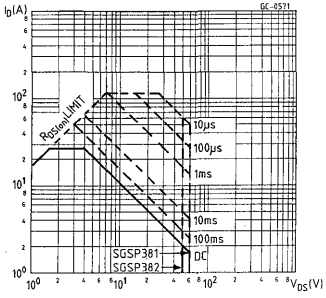
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP381** for **SGSP382**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 14 A V_{GS} = 10 V I_D = 14 A T_c = 100°C			0.06 0.12	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 14 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	 V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1100	1400 800 400	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 14 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		25 75 50 40	35 100 65 55	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

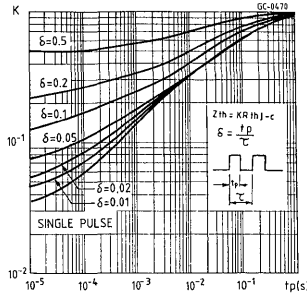
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				28 112	A A
V_{SD} Forward on voltage	I_{SD} = 28 A V_{GS} = 0			1.4	V
t_{rr} Reverse recovery time	I_{SD} = 28 A V_{GS} = 0 di/dt = 25 A/μs		125		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

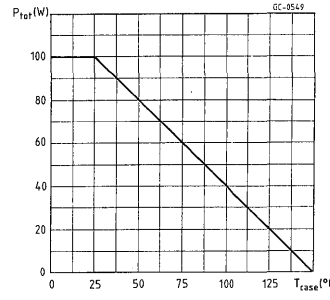
Safe operating areas



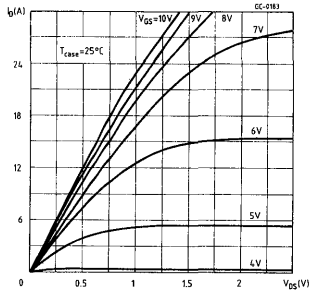
Thermal impedance



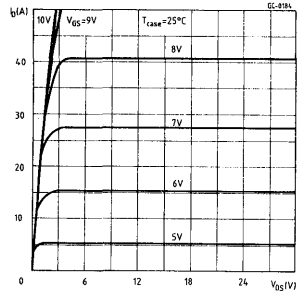
Derating curve



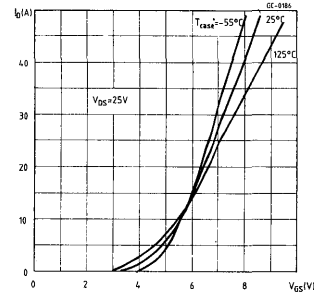
Output characteristics



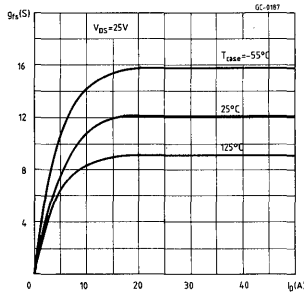
Output characteristics



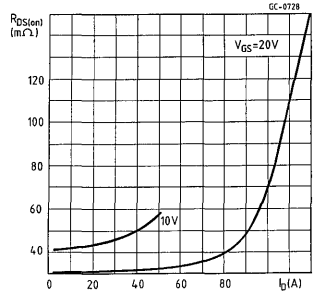
Transfer characteristics



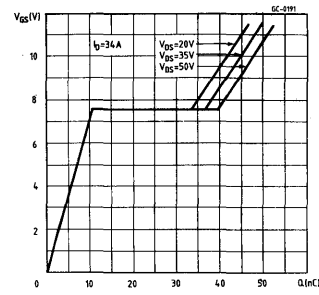
Transconductance



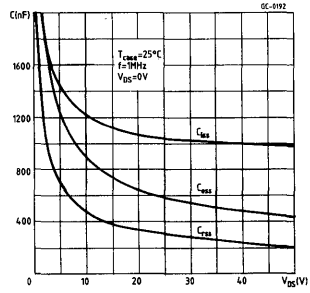
Static drain-source on resistance



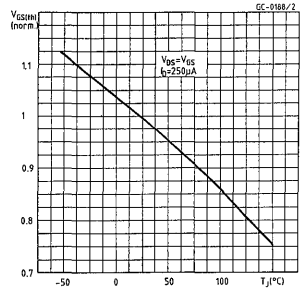
Gate charge vs gate-source voltage



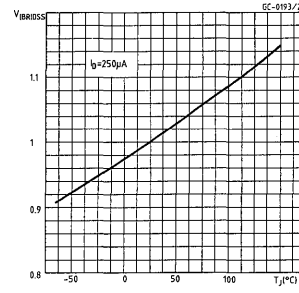
Capacitance variation



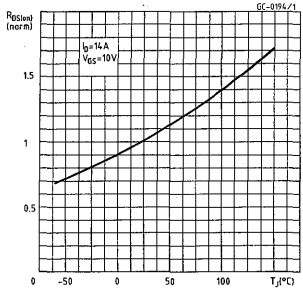
Normalized gate threshold voltage vs temperature



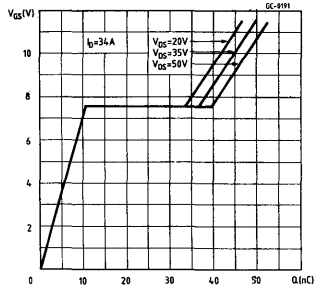
Normalized breakdown voltage vs temperature



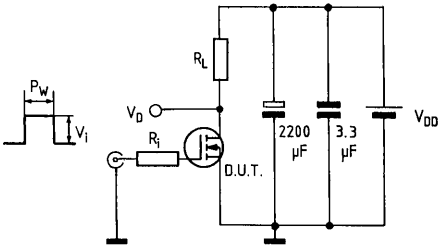
Normalized on resistance vs temperature



Source-drain diode forward characteristics

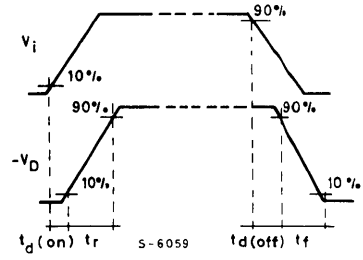


Switching times test circuit for resistive load

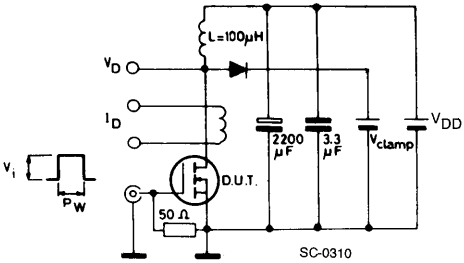


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

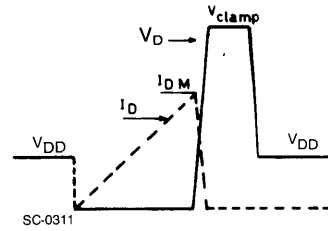


Clamped inductive load test circuit

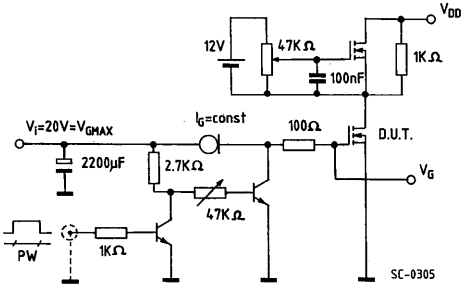


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

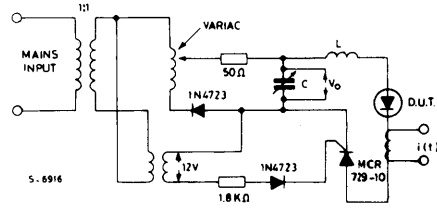


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP461
SGSP462

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

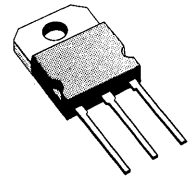
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP461	100 V	0.15 Ω	20 A
SGSP462	80 V	0.1 Ω	25 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR UPS APPLICATIONS
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical applications include UPS, battery chargers, printer hammer drivers, solenoid drivers and motor control.



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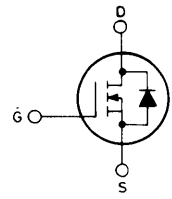
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP461	SGSP462	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	20	25	A
I_D	Drain current (cont.) at $T_c=100°C$	13	16	A
I_{DM} (•)	Drain current (pulsed)	80	100	A
P_{tot}	Total dissipation at $T_c<25°C$	125		W
	Derating factor	1		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

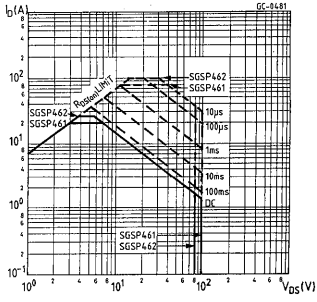
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP461** for **SGSP462**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A for **SGSP461** I_D = 12.5 A for **SGSP462** V_{GS} = 10 V T_c = 100°C I_D = 10 A for **SGSP461** I_D = 12.5 A for **SGSP462**			 0.15 0.1 0.3 0.2	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP461** for **SGSP462**	 20 25			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 12.5 A	4.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		950	1200 480 230	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

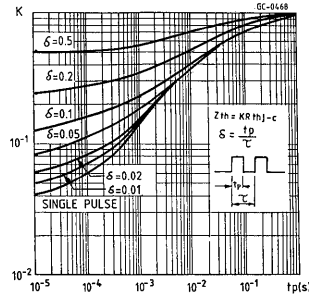
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 12.5 A		20	30	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		60	80	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		65	85	ns
t_f	Fall time			25	35	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP461**			20	A
		for **SGSP462**			25	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP461**			80	A
		for **SGSP462**			100	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 20 A for **SGSP461**			1.35	V
		I_{SD} = 25 A for **SGSP462**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 25 A V_{GS} = 0 di/dt = 25 A/μs		190		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

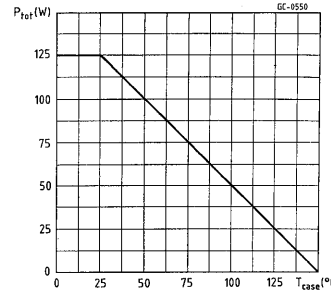
Safe operating areas



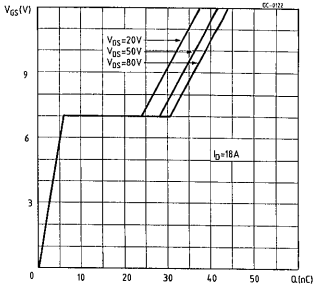
Thermal impedance



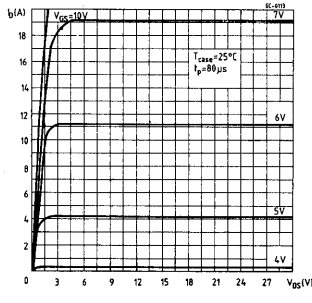
Derating curve



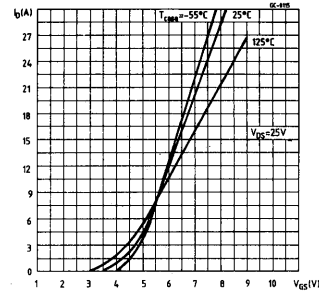
Output characteristics



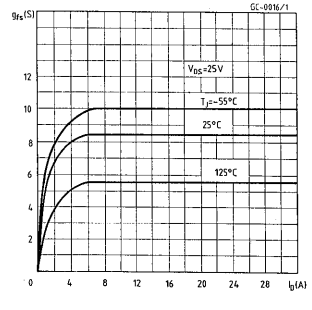
Output characteristics



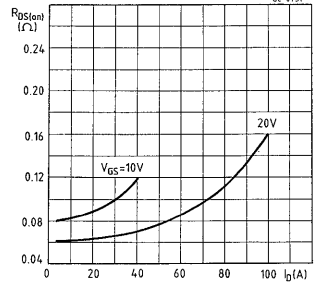
Transfer characteristics



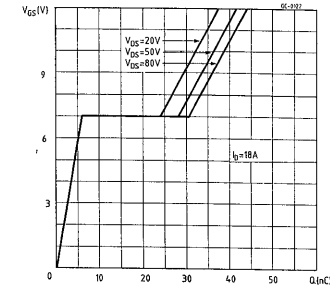
Transconductance



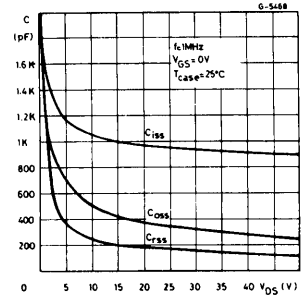
Static drain-source on resistance



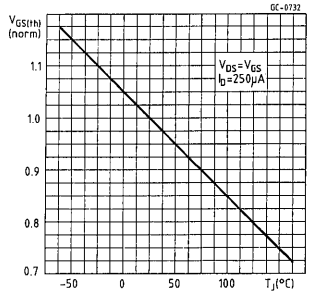
Gate charge vs gate-source voltage



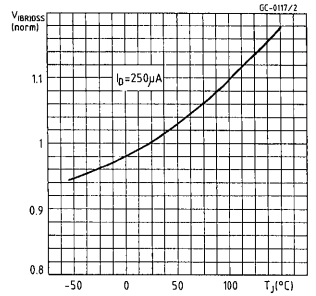
Capacitance variation



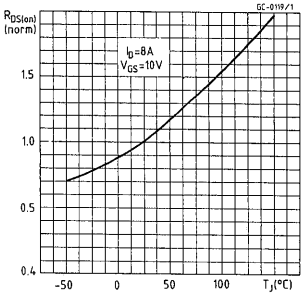
Normalized gate threshold voltage vs temperature



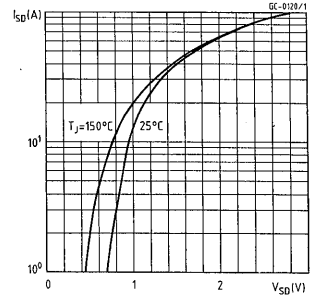
Normalized breakdown voltage vs temperature



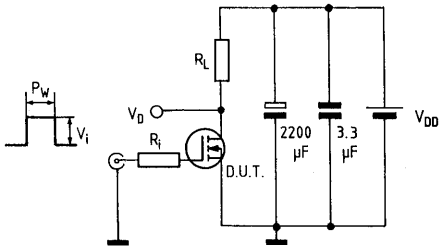
Normalized on resistance vs temperature



Source-drain diode forward characteristics

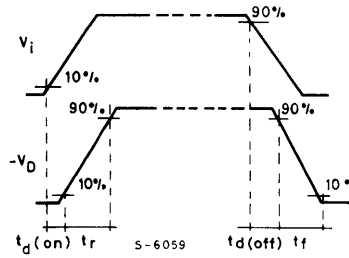


Switching times test circuit for resistive load

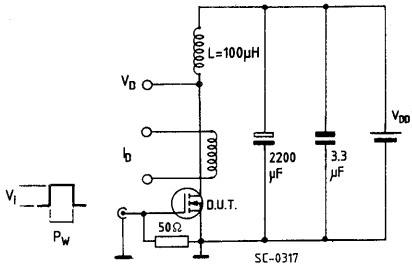


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

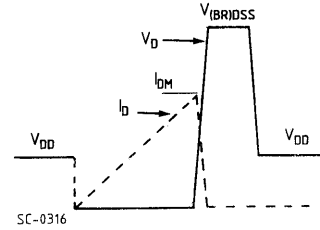


Unclamped inductive load test circuit

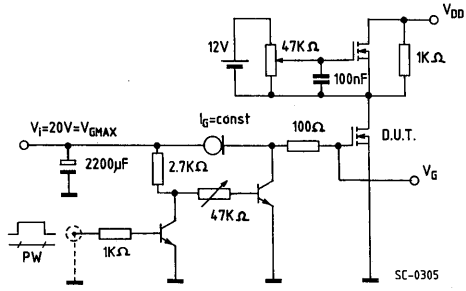


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

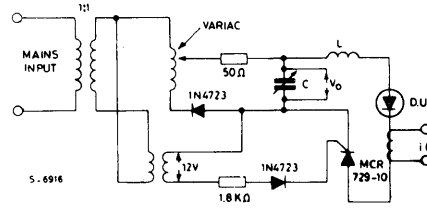


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP471
SGSP472

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

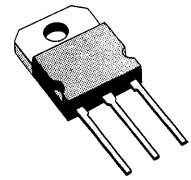
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP471	100 V	0.075 Ω	30 A
SGSP472	80 V	0.05 Ω	35 A

- HIGH SPEED SWITCHING APPLICATIONS
- 80 - 100 VOLTS - FOR DC/DC CONVERTERS
- HIGH CURRENT > 1V DROP AT 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- UNINTERRUPTIBLE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Applications include DC/DC converters, UPS, battery chargers, secondary regolators, servo control, power audio amplifiers and robotics.



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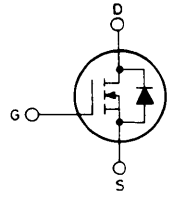
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP471	SGSP472	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	100	80	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	100	80	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	30	35	A
I_D	Drain current (cont.) at $T_c=100°C$	19	22	A
I_{DM} (•)	Drain current (pulsed)	120	140	A
P_{tot}	Total dissipation at $T_c<25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

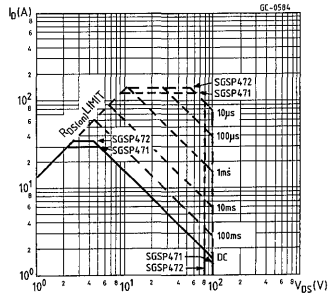
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP471** for **SGSP472**	 100 80			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 15 A for **SGSP471** I_D = 17.5 A for **SGSP472** V_{GS} = 10 V T_c = 100°C I_D = 15 A for **SGSP471** I_D = 17.5 A for **SGSP472**			 0.075 0.05 0.15 0.1	 Ω Ω Ω Ω
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C for **SGSP471** for **SGSP472**	 30 35			 A A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 17.5 A	9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1800	2200 810 375	pF pF pF

ELECTRICAL CHARACTERISTICS (Continued)

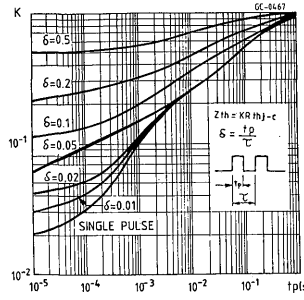
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING						
$t_{d\ (on)}$	Turn-on time	V_{DD} = 50 V I_D = 17.5 A		30	40	ns
t_r	Rise time	V_i = 10 V R_i = 4.7 Ω		85	110	ns
$t_{d\ (off)}$	Turn-off delay time	(see test circuit)		100	130	ns
t_f	Fall time			40	55	ns
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP471**			30	A
		for **SGSP472**			35	A
I_{SDM} (•)	Source-drain current (pulsed)	for **SGSP471**			120	A
		for **SGSP472**			140	A
V_{SD}	Forward on voltage	V_{GS} = 0				
		I_{SD} = 30 A for **SGSP471**			1.35	V
		I_{SD} = 35 A for **SGSP472**			1.35	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A V_{GS} = 0 di/dt = 25 A/μs		190		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

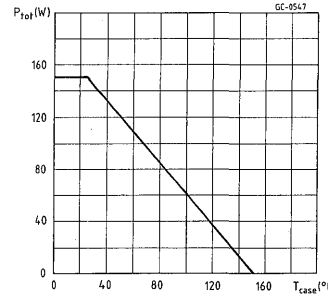
Safe operating areas



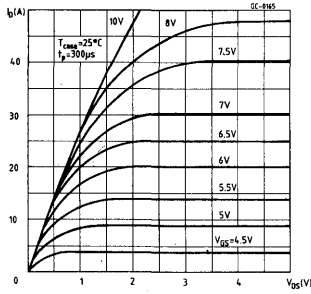
Thermal impedance



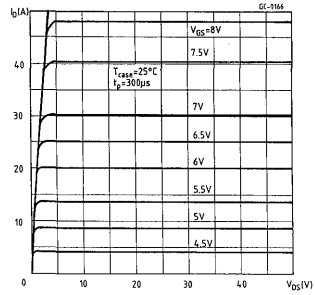
Derating curve



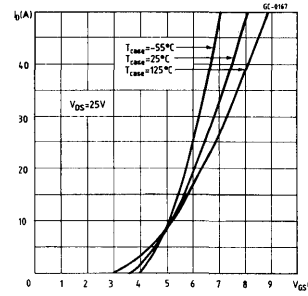
Output characteristics



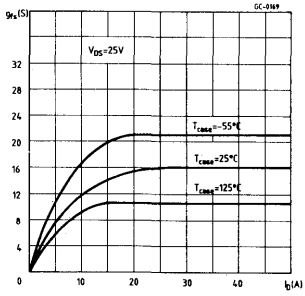
Output characteristics



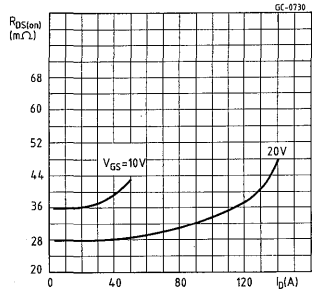
Transfer characteristics



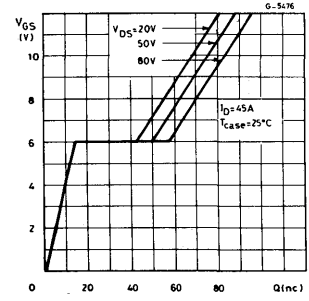
Transconductance



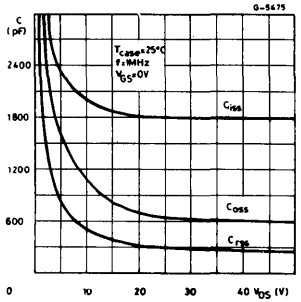
Static drain-source on resistance



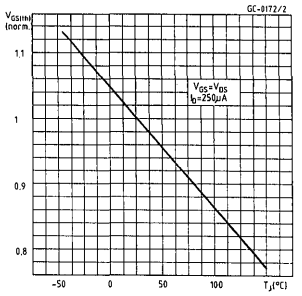
Gate charge vs gate-source voltage



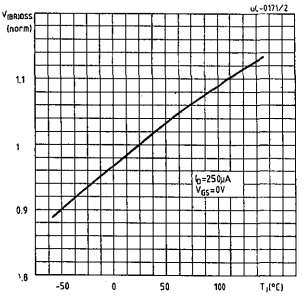
Capacitance variation



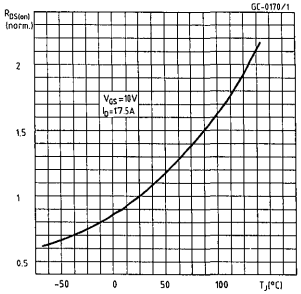
Normalized gate threshold voltage vs temperature



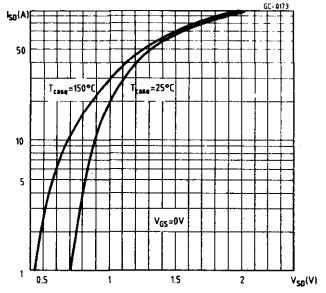
Normalized breakdown voltage vs temperature



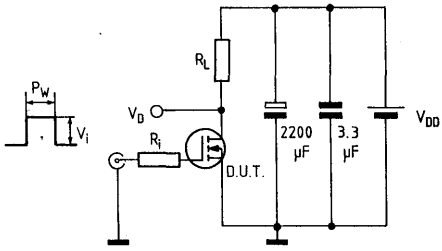
Normalized on resistance vs temperature



Source-drain diode forward characteristics

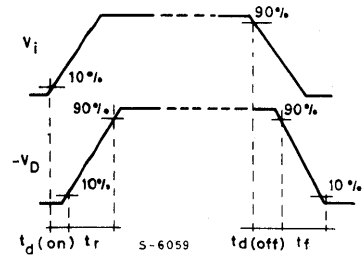


Switching times test circuit for resistive load

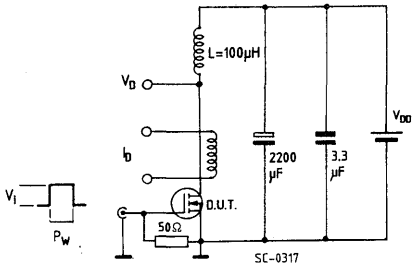


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

Switching time waveforms for resistive load

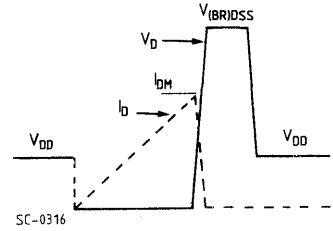


Unclamped inductive load test circuit

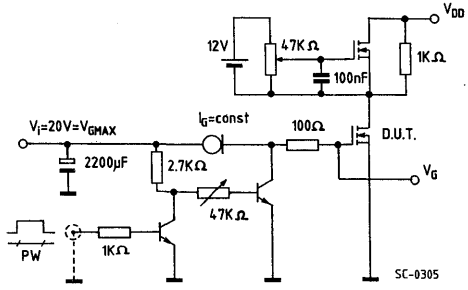


V_j = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

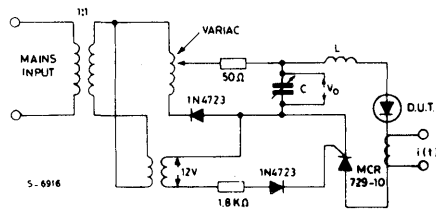


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP474
SGSP475

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

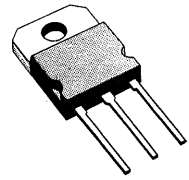
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP474	450 V	0.7 Ω	9 A
SGSP475	400 V	0.55 Ω	10 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR SMPS UP TO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT >100kHz
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Fast switching and easy drive make these POWER MOS transistors ideal for high voltage switching applications. These applications include electronic welders, switched mode power supplies and sonar equipment.



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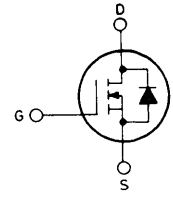
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP474	SGSP475	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	450	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	450	400	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	9	10	A
I_D	Drain current (cont.) at $T_c=100°C$	5.6	6.3	A
I_{DM} (•)	Drain current (pulsed)	40	40	A
I_{DLM} (•)	Drain inductive current, clamped	40	40	A
P_{tot}	Total dissipation at $T_c<25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

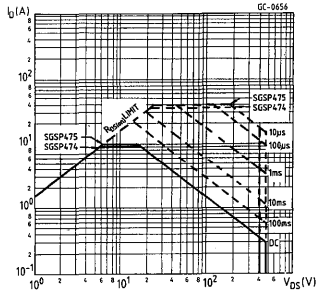
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP474** for **SGSP475**	 450 400			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4.5 A for **SGSP474** I_D = 5 A for **SGSP475** V_{GS} = 10 V T_c = 100°C I_D = 4.5 A for **SGSP474** I_D = 5 A for **SGSP475**			 0.7 0.55 1.4 1.1	 Ω Ω Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5 A	6			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	2100 390 260	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 45 125 30	40 60 165 40	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

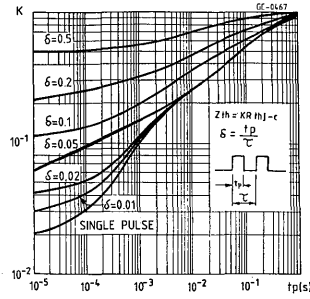
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP474** for **SGSP475**			9 10	A A
I_{SDM} (•)	Source-drain current (pulsed)				40	A
V_{SD}	Forward on voltage	V_{GS} = 0 I_{SD} = 9 A for **SGSP474** I_{SD} = 10 A for **SGSP475**			1.2 1.2	V V
t_{rr}	Reverse recovery time	I_{SD} = 10 A V_{GS} = 0 di/dt = 100 A/μs		420		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

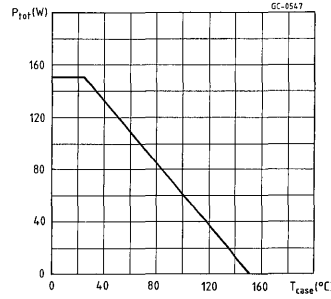
Safe operating areas



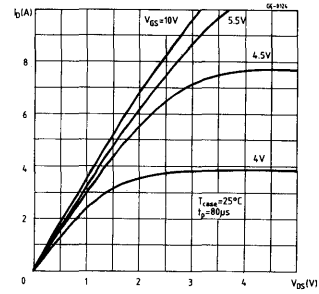
Thermal impedance



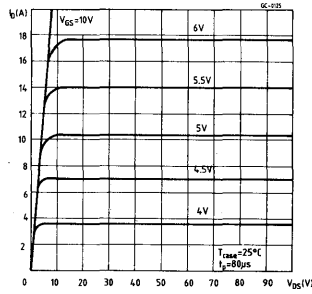
Derating curve



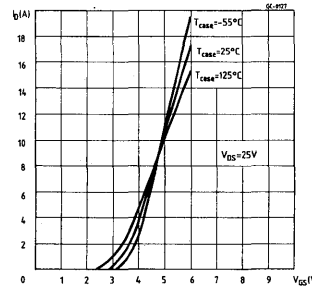
Output characteristics



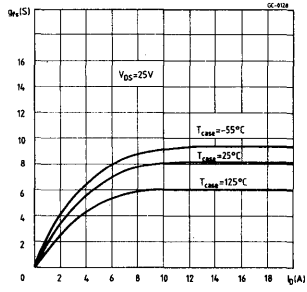
Output characteristics



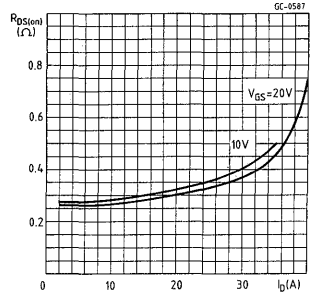
Transfer characteristics



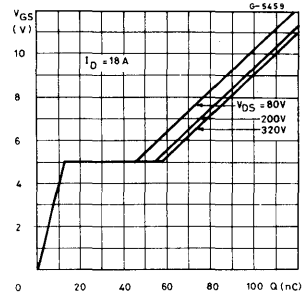
Transconductance



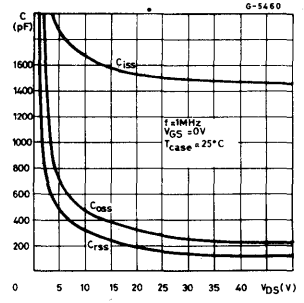
Static drain-source on resistance



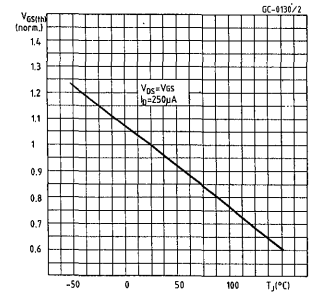
Gate charge vs gate-source voltage



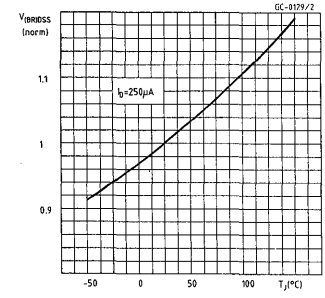
Capacitance variation



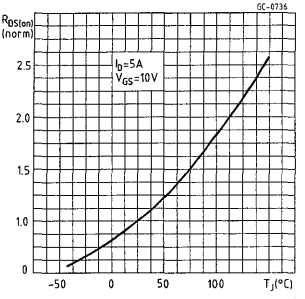
Normalized gate threshold voltage vs temperature



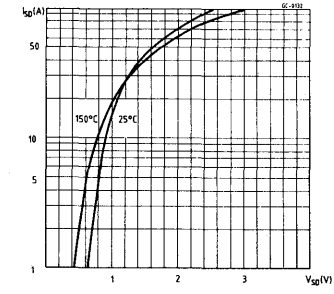
Normalized breakdown voltage vs temperature



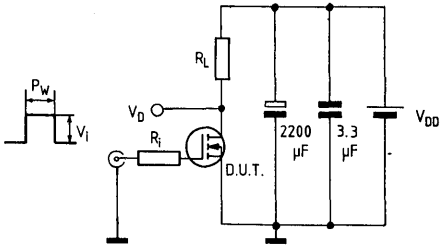
Normalized on resistance vs temperature



Source-drain diode forward characteristics

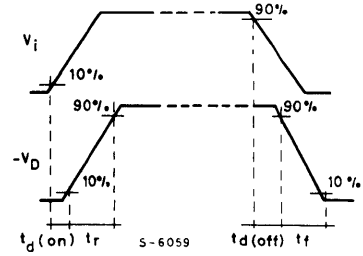


Switching times test circuit for resistive load

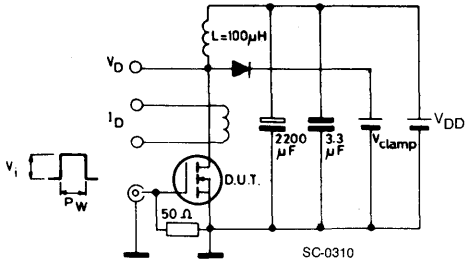


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

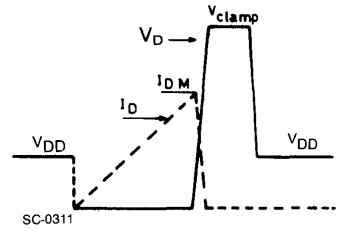


Clamped inductive load test circuit

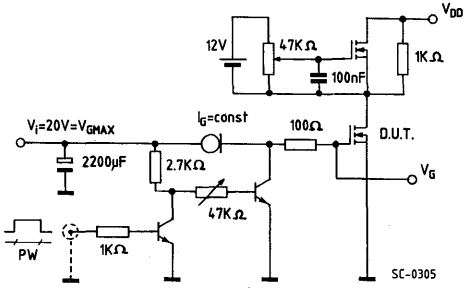


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

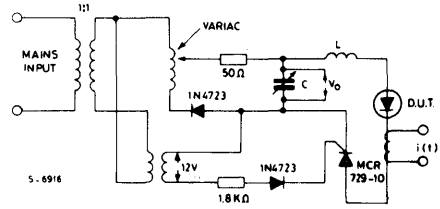


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP477

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

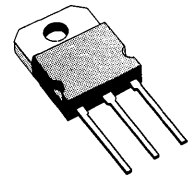
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP477	200 V	0.17 Ω	20 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH CURRENT - FOR TELECOMM POWER SUPPLIES
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS FOR ROBOTICS.

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include robotics, laser diode drives, UPS, SMPS and DC/DC converters, electric vehicle drives and a DC switch for telecommunications.



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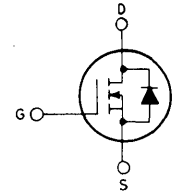
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	200	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	20	A
I_D	Drain current (cont.) at $T_c=100°C$	13	A
I_{DM} (•)	Drain current (pulsed)	80	A
I_{DLM} (•)	Drain inductive current, clamped	80	A
P_{tot}	Total dissipation at $T_c<25°C$	150	W
	Derating factor	1.2	W/°C
T_{stg}	Storage temperature	−55 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

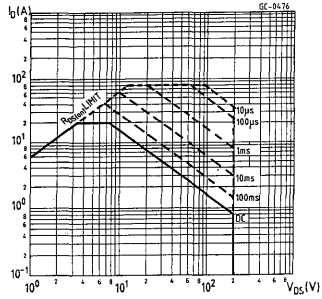
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A V_{GS} = 10 V I_D = 10 A T_c = 100°C			0.17 0.34	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 10 A	8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2200 550 260	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 100 V I_D = 10 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 50 110 35	40 65 145 45	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

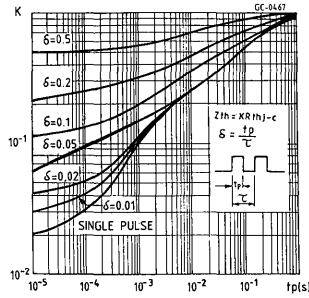
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				20 80	A A
V_{SD} Forward on voltage	I_{SD} = 20 A V_{GS} = 0			1.3	V
t_{rr} Reverse recovery time	I_{SD} = 20 A V_{GS} = 0 di/dt = 100 A/μs		320		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

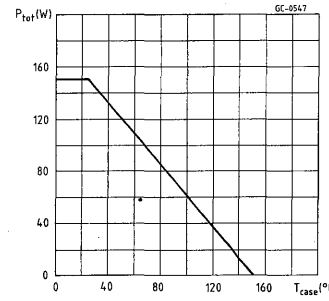
Safe operating areas



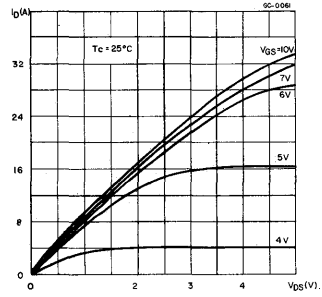
Thermal impedance



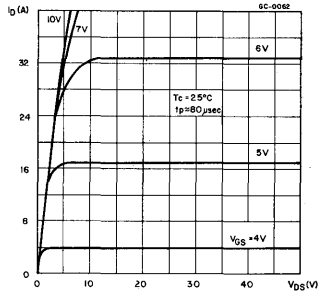
Derating curve



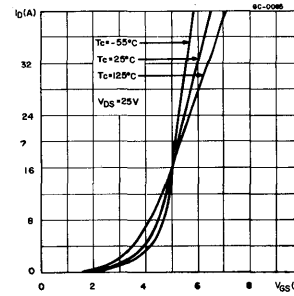
Output characteristics



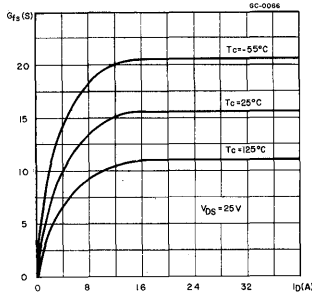
Output characteristics



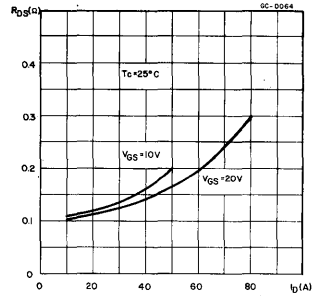
Transfer characteristics



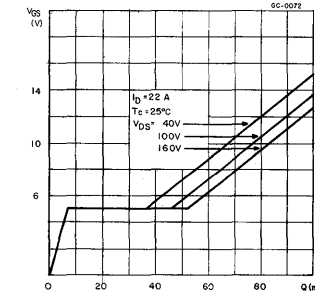
Transconductance



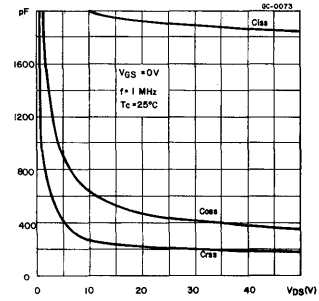
Static drain-source on resistance



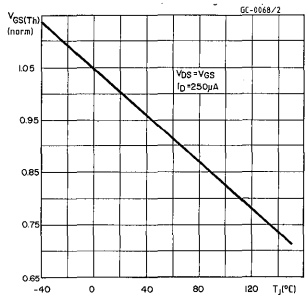
Gate charge vs gate-source voltage



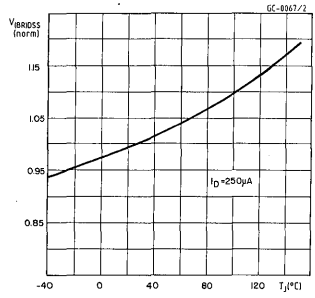
Capacitance variation



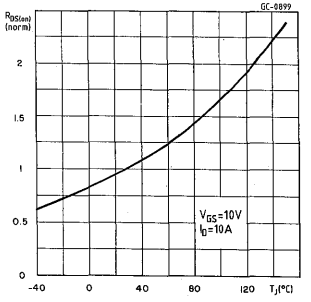
Normalized gate threshold voltage vs temperature



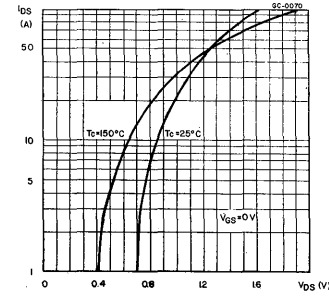
Normalized breakdown voltage vs temperature



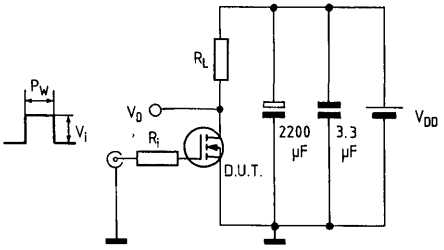
Normalized on resistance vs temperature



Source-drain diode forward characteristics

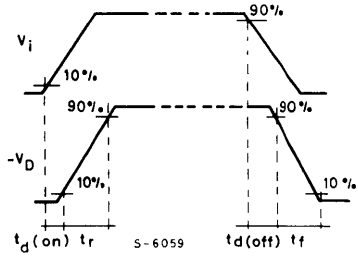


Switching times test circuit for resistive load

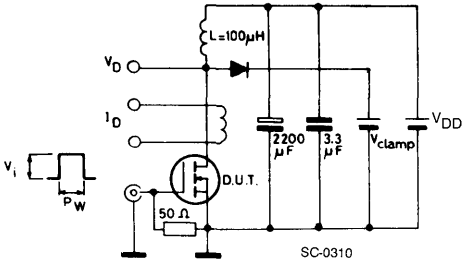


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

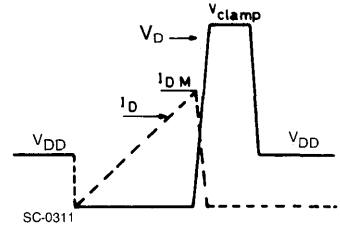


Clamped inductive load test circuit

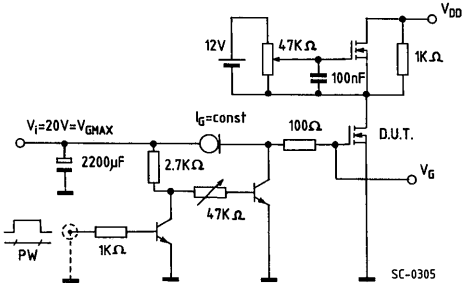


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

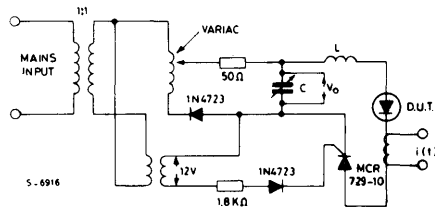


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP479

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

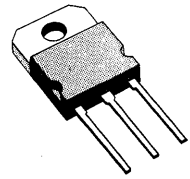
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP479	500 V	0.7 Ω	9 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 500V FOR OFF-LINE SMPS
- HIGH VOLTAGE - 9A FOR UP TO 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - REDUCES COST AND SIZE

INDUSTRIAL APPLICATIONS:

- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching mode power supplies, uninterruptible power supplies and motor speed control.



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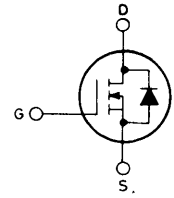
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at T_c = 25°C	9	A
I_D	Drain current (cont.) at T_c = 100°C	5.6	A
I_{DM} (•)	Drain current (pulsed)	36	A
I_{DLM} (•)	Drain inductive current, clamped	36	A
P_{tot}	Total dissipation at T_c < 25°C	150	W
	Derating factor	1.2	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

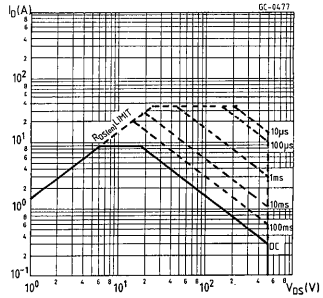
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4.5 A V_{GS} = 10 V I_D = 4.5 A T_c = 100°C			0.7 1.4	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 4.5 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	1900 280 170	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 250 V I_D = 4.5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 40 130 30	40 60 170 40	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

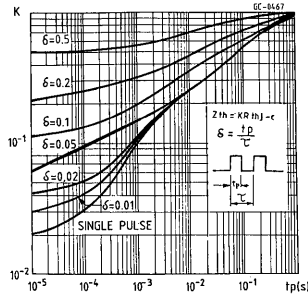
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				9 36	A A
V_{SD} Forward on voltage	I_{SD} = 9 A V_{GS} = 0			1.15	V
t_{rr} Reverse recovery time	I_{SD} = 9 A V_{GS} = 0 di/dt = 100 A/μs		420		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

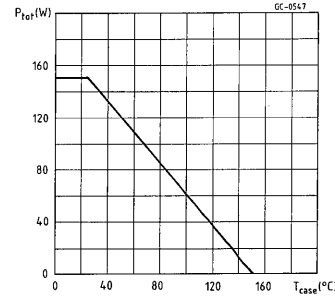
Safe operating areas



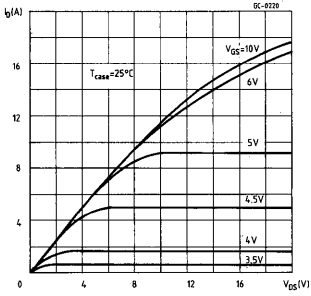
Thermal impedance



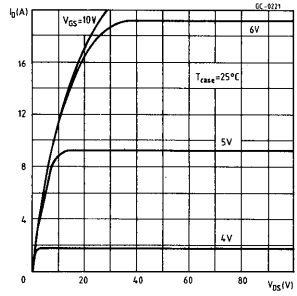
Derating curve



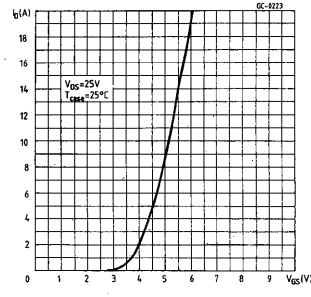
Output characteristics



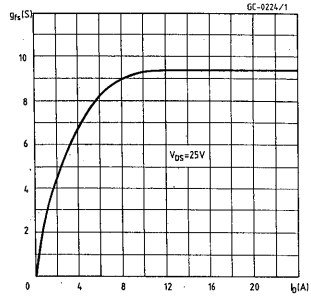
Output characteristics



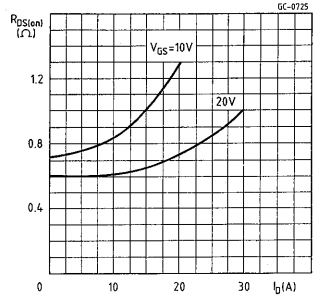
Transfer characteristics



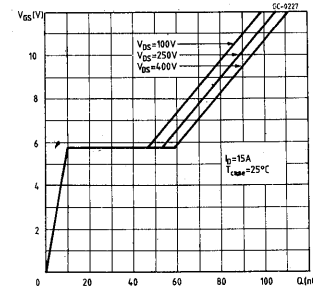
Transconductance



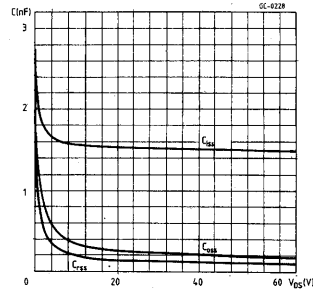
Static drain-source on resistance



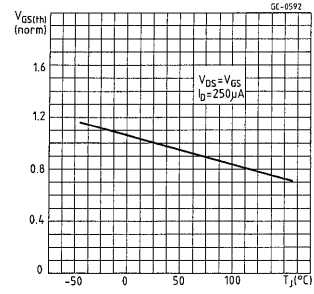
Gate charge vs gate-source voltage



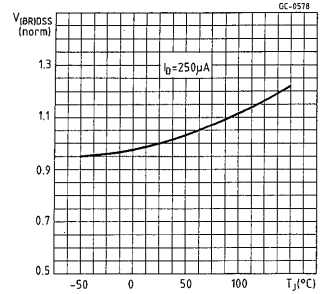
Capacitance variation



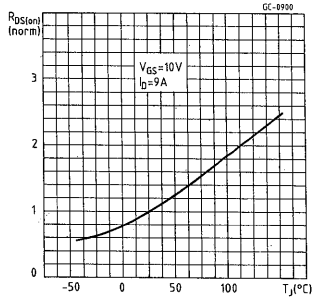
Normalized gate threshold voltage vs temperature



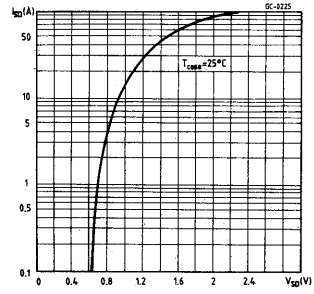
Normalized breakdown voltage vs temperature



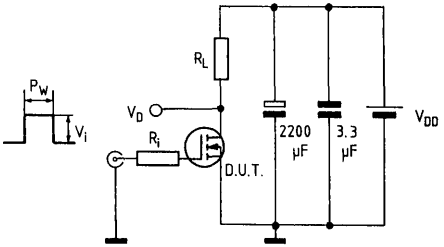
Normalized on resistance vs temperature



Source-drain diode forward characteristics

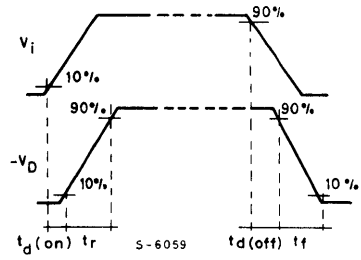


Switching times test circuit for resistive load

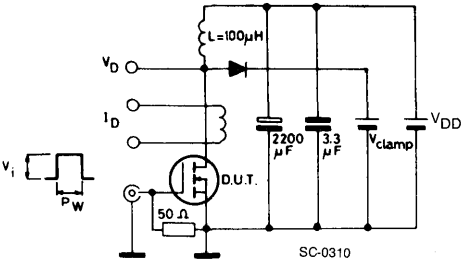


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

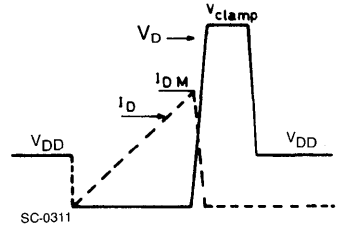


Clamped inductive load test circuit

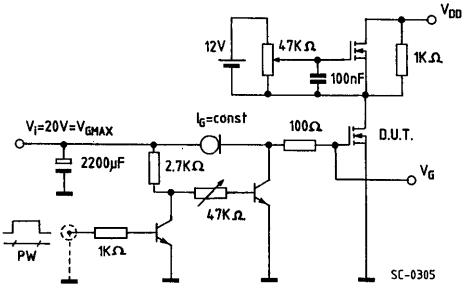


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

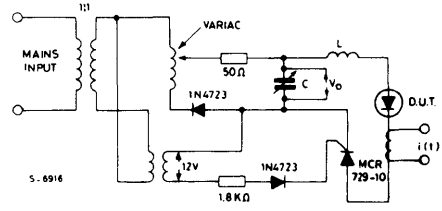


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP481
SGSP482

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

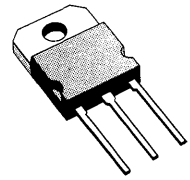
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP481	60 V	0.06 Ω	30 A
SGSP482	50 V	0.06 Ω	30 A

- HIGH SPEED SWITCHING APPLICATIONS
- 60 VOLTS - DC/DC AND UPS APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

- DC/DC CONVERTERS AND UPS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include UPS, battery chargers, printer mechanism drives and motor speed control.



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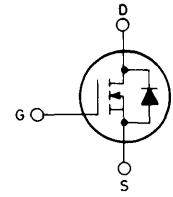
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP481	SGSP482	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	30		A
I_D	Drain current (cont.) at $T_c=100°C$	19		A
I_{DM} (•)	Drain current (pulsed)	120		A
I_{DLM} (•)	Drain inductive current, clamped	120		A
P_{tot}	Total dissipation at $T_c<25°C$	125		W
	Derating factor	1		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

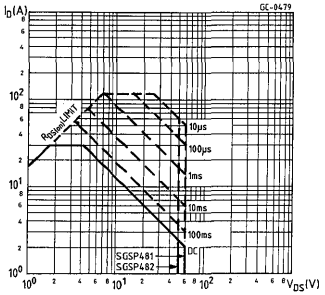
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP481** for **SGSP482**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 15 A V_{GS} = 10 V I_D = 15 A T_c = 100°C			0.06 0.12	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 15 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	 V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1100	1400 800 400	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 15 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		25 75 50 40	35 100 65 55	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

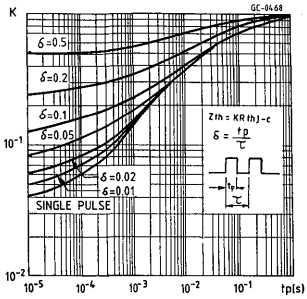
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (*)	Source-drain current Source-drain current (pulsed)					30 120	A A
V_{SD}	Forward on voltage	I_{SD} = 30 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A di/dt = 100 A/μs	V_{GS} = 0		125		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

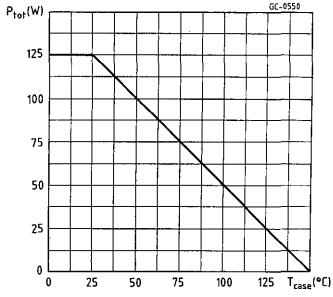
Safe operating areas



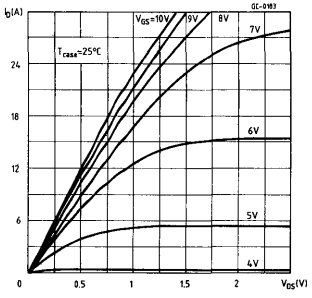
Thermal impedance



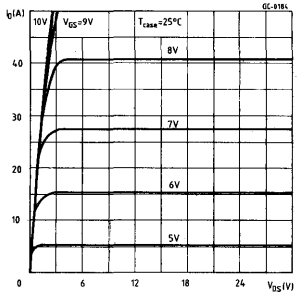
Derating curve



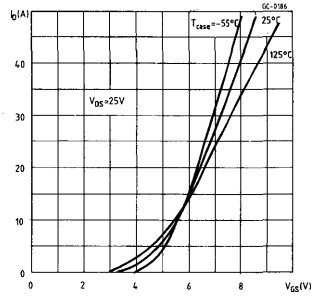
Output characteristics



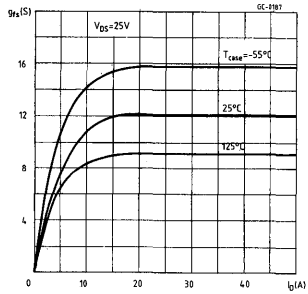
Output characteristics



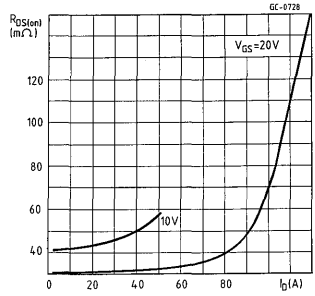
Transfer characteristics



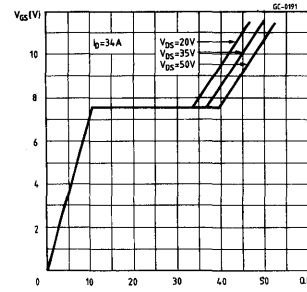
Transconductance



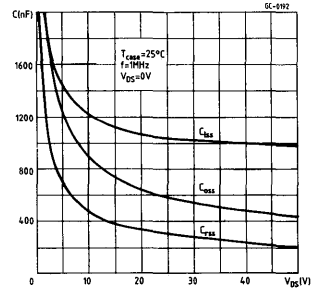
Static drain-source on resistance



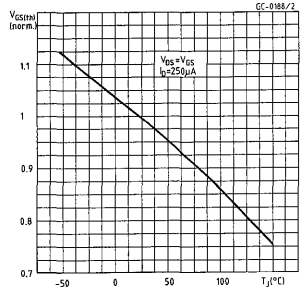
Gate charge vs gate-source voltage



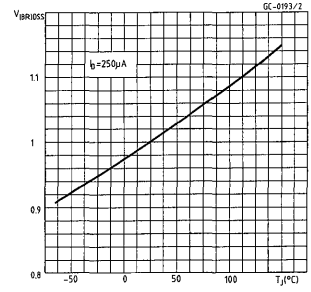
Capacitance variation



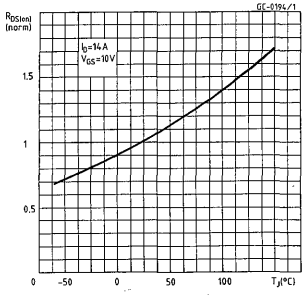
Normalized gate threshold voltage vs temperature



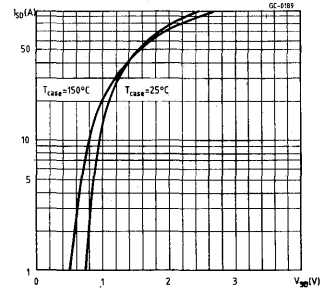
Normalized breakdown voltage vs temperature



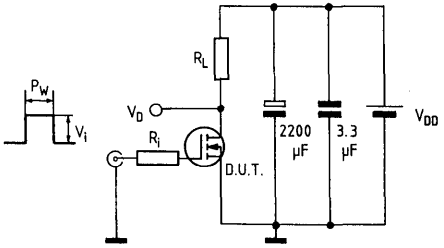
Normalized on resistance vs temperature



Source-drain diode forward characteristics

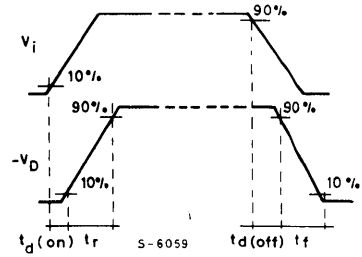


Switching times test circuit for resistive load

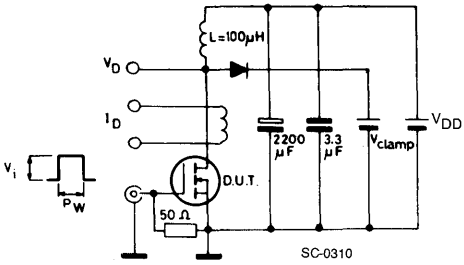


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

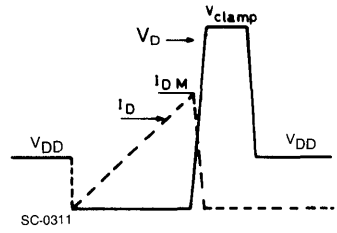


Clamped inductive load test circuit

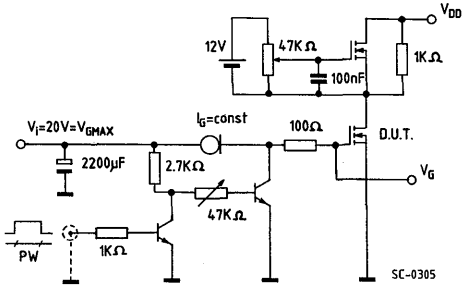


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

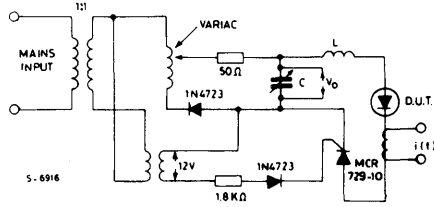


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP491
SGSP492

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

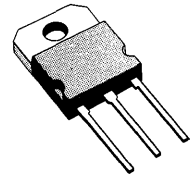
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP491	60 V	0.033 Ω	40 A
SGSP492	50 V	0.033 Ω	40 A

- HIGH SPEED SWITCHING APPLICATIONS
- 50 - 60 VOLTS FOR INVERTER AND UPS
- HIGH CURRENT - $V_{DS\ (on)} \leq 1V$ at 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ◆
- EASY DRIVE - REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

- DC/DC CONVERTERS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications such as DC/DC converters, UPS, inverters, battery changers and solar power converters.



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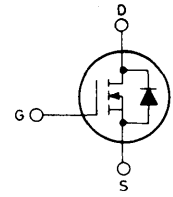
INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP491	SGSP492	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	40		A
I_D	Drain current (cont.) at $T_c=100°C$	25		A
I_{DM} (•)	Drain current (pulsed)	160		A
P_{tot}	Total dissipation at $T_c<25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
◆ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

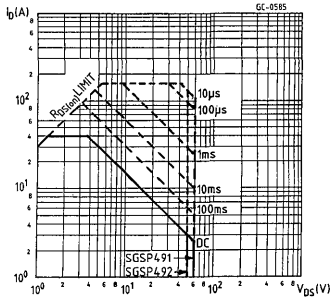
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP491** for **SGSP492**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A V_{GS} = 10 V I_D = 20 A T_c = 100°C			33 66	mΩ mΩ
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	40			A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 20 A	10			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	 V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2800 1500 850	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 20 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		35 110 90 55	45 145 120 70	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

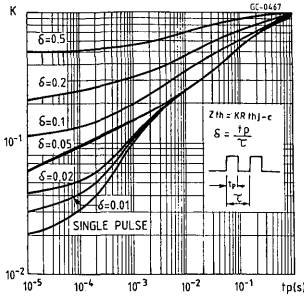
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					40 160	A A
V_{SD}	Forward on voltage	I_{SD} = 40 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A di/dt = 25 A/μs	V_{GS} = 0		140		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

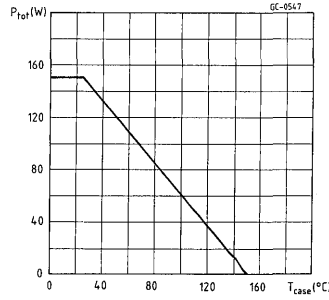
Safe operating areas



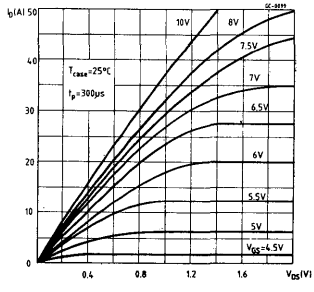
Thermal impedance



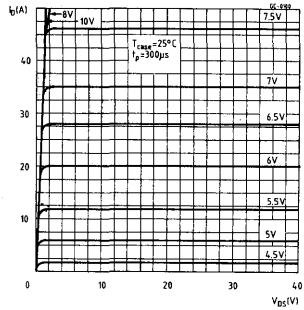
Derating curve



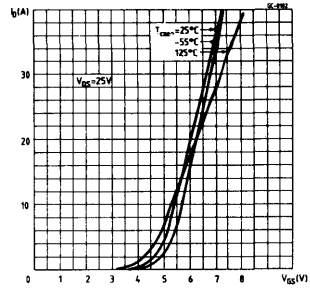
Output characteristics



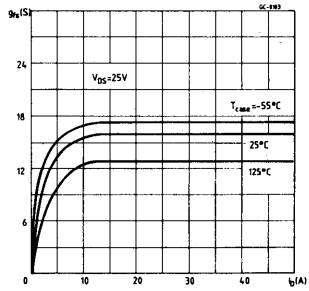
Output characteristics



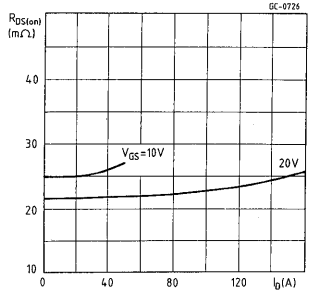
Transfer characteristics



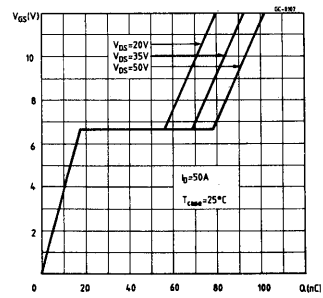
Transconductance



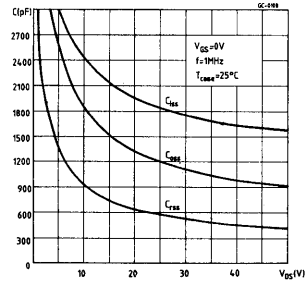
Static drain-source on resistance



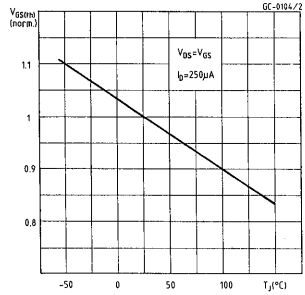
Gate charge vs gate-source voltage



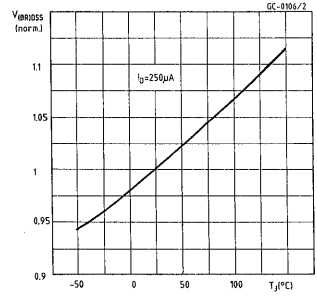
Capacitance variation



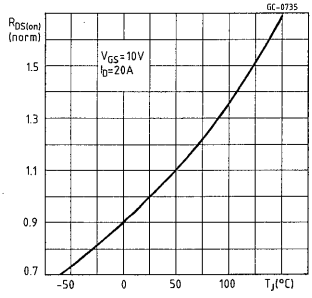
Normalized gate threshold voltage vs temperature



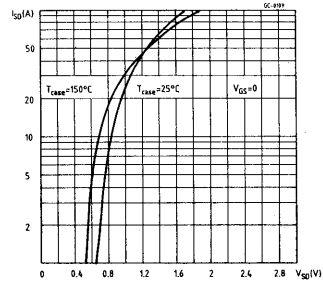
Normalized breakdown voltage vs temperature



Normalized on resistance vs temperature

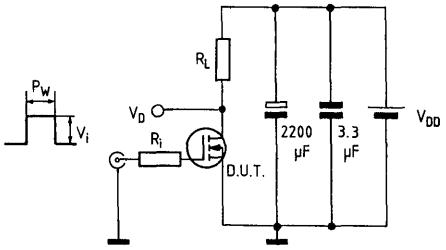


Source-drain diode forward characteristics



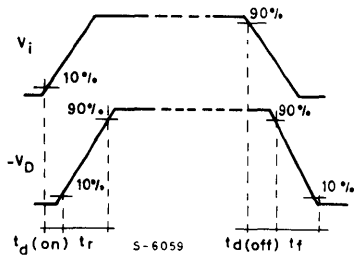
SGS-THOMSON MICROELECTRONICS

Switching times test circuit for resistive load

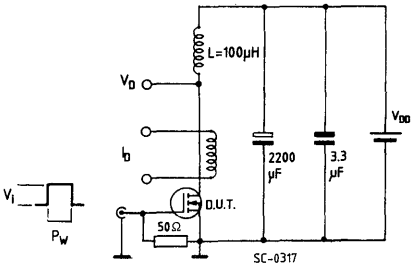


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

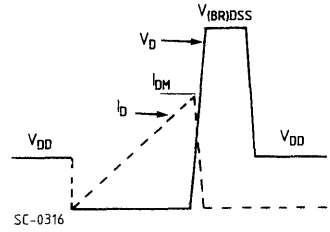


Unclamped inductive load test circuit

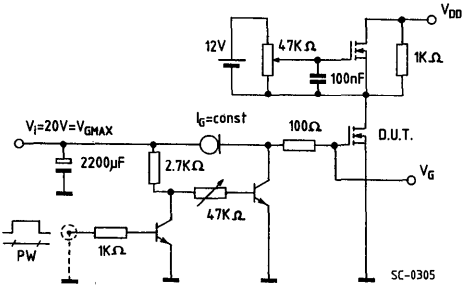


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

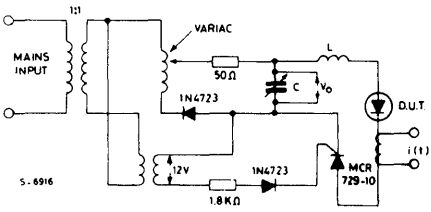


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP574
SGSP575

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

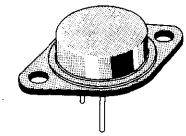
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP574	450 V	0.7 Ω	9 A
SGSP575	400 V	0.55 Ω	10 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - FOR OFF-LINE SMPS
- HIGH CURRENT - FOR SMPS UPTO 350W
- ULTRA FAST SWITCHING - FOR OPERATION AT >100kHz
- EASY DRIVE FOR REDUCED SIZE AND COST

INDUSTRIAL APPLICATIONS:

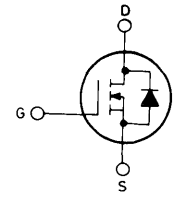
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Fast switching and easy drive make these POWER MOS transistors ideal for high voltage switching applications. These applications include electronic welders, switched mode power supplies and sonar equipment.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP574	SGSP575	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	450	400	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	450	400	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	9	10	A
I_D	Drain current (cont.) at $T_c=100°C$	5.6	6.3	A
I_{DM} (•)	Drain current (pulsed)	40	40	A
I_{DLM} (•)	Drain inductive current, clamped	40	40	A
P_{tot}	Total dissipation at T_c <25°C	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

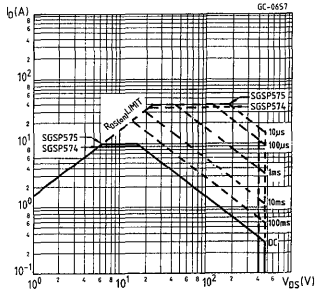
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP574** for **SGSP575**	 450 400			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4.5 A for **SGSP574** I_D = 5 A for **SGSP575** V_{GS} = 10 V T_c = 100°C I_D = 4.5 A for **SGSP574** I_D = 5 A for **SGSP575**			 0.7 0.55 1.4 1.1	 Ω Ω Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 5 A	6			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	2100 390 260	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 225 V I_D = 5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 45 125 30	40 60 165 40	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

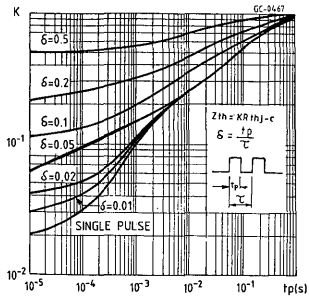
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE						
I_{SD}	Source-drain current	for **SGSP574** for **SGSP575**			9 10	A A
I_{SDM} (•)	Source-drain current (pulsed)				40	A
V_{SD}	Forward on voltage	V_{GS} = 0 I_{SD} = 9 A for **SGSP574** I_{SD} = 10 A for **SGSP575**			 1.2 1.2	 V V
t_{rr}	Reverse recovery time	I_{SD} = 10 A V_{GS} = 0 di/dt = 100 A/μs		420		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

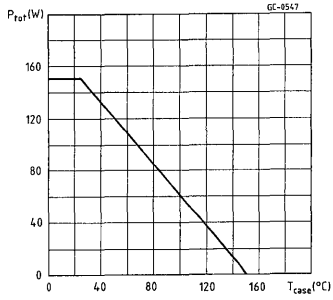
Safe operating areas



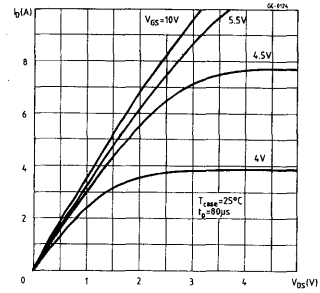
Thermal impedance



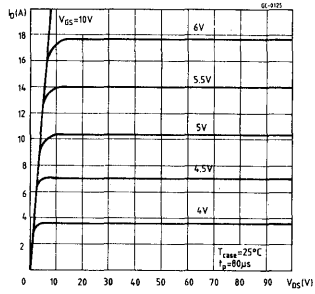
Derating curve



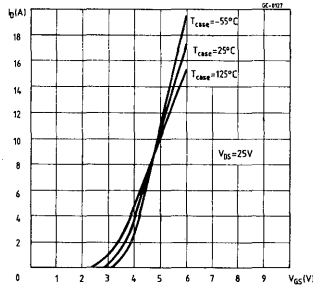
Output characteristics



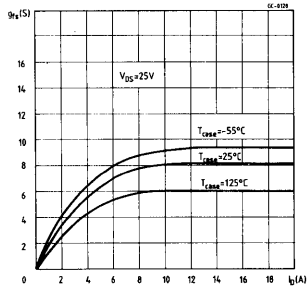
Output characteristics



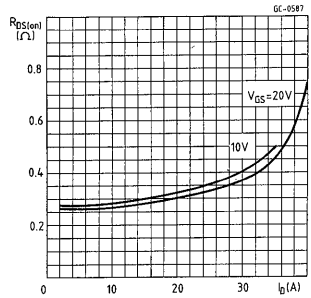
Transfer characteristics



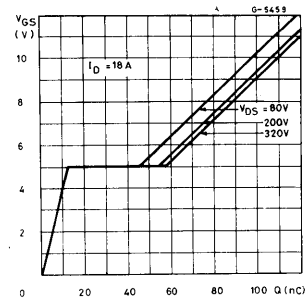
Transconductance



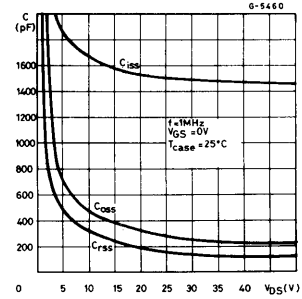
Static drain-source on resistance



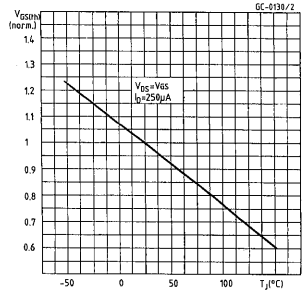
Gate charge vs gate-source voltage



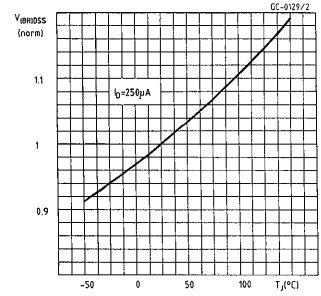
Capacitance variation



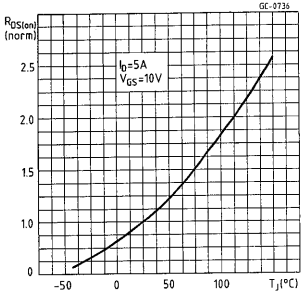
Normalized gate threshold voltage vs temperature



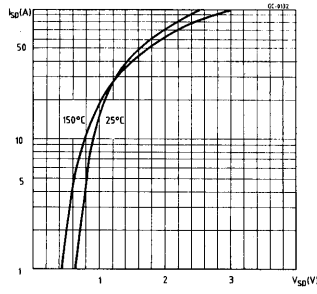
Normalized breakdown voltage vs temperature



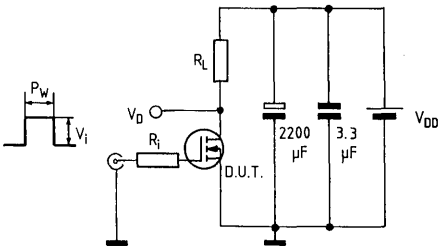
Normalized on resistance vs temperature



Source-drain diode forward characteristics

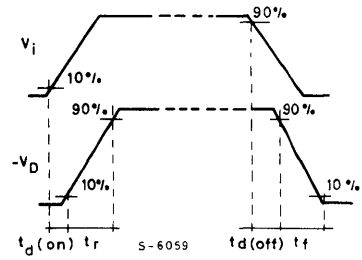


Switching times test circuit for resistive load

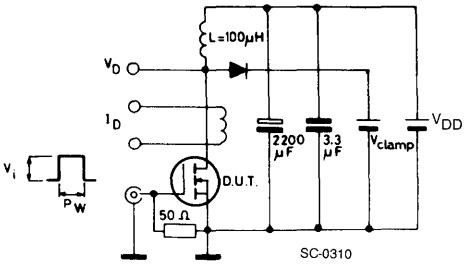


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

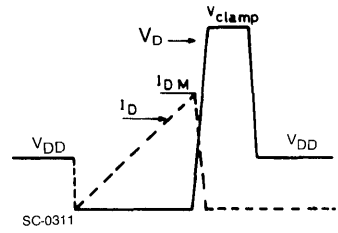


Clamped inductive load test circuit

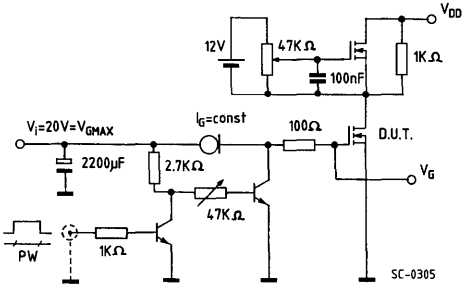


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

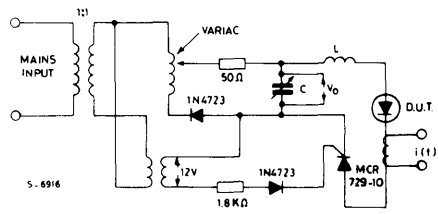


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP577

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

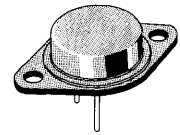
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP577	200 V	0.17 Ω	20 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH CURRENT - FOR TELECOMM POWER SUPPLIES
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

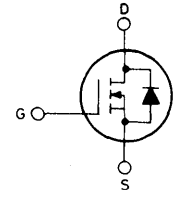
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS FOR ROBOTICS.

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include robotics, UPS, SMPS and DC/DC converters, electric vehicle drives and a DC switch for telecommunications.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	200	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	20	A
I_D	Drain current (cont.) at $T_c=100°C$	13	A
I_{DM} (•)	Drain current (pulsed)	80	A
I_{DLM} (•)	Drain inductive current, clamped	80	A
P_{tot}	Total dissipation at $T_c<25°C$	150	W
	Derating factor	1.2	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

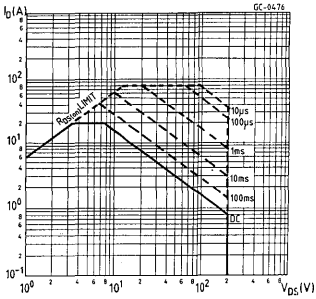
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 10 A V_{GS} = 10 V I_D = 10 A T_c = 100°C			0.17 0.34	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 10 A	8			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2200 550 260	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 100 V I_D = 10 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 50 110 35	40 65 145 45	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

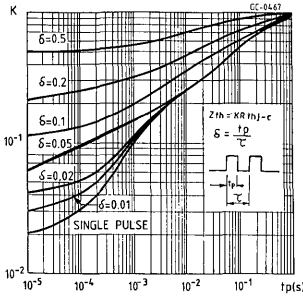
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				20 80	A A
V_{SD} Forward on voltage	I_{SD} = 20 A V_{GS} = 0			1.3	V
t_{rr} Reverse recovery time	I_{SD} = 20 A V_{GS} = 0 di/dt = 100 A/μs		320		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

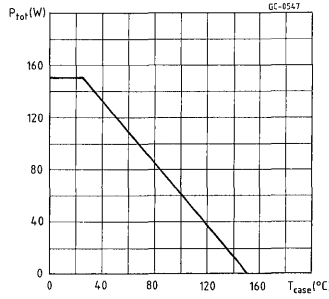
Safe operating areas



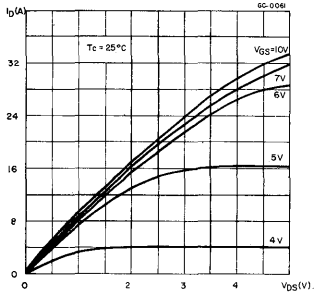
Thermal impedance



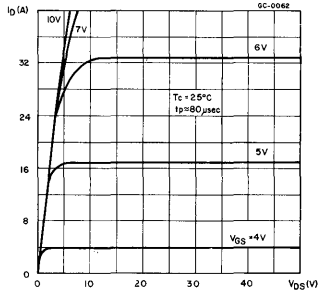
Derating curve



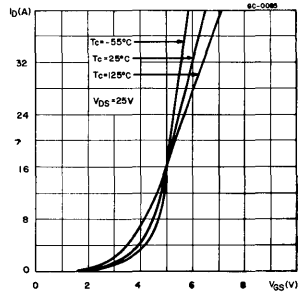
Output characteristics



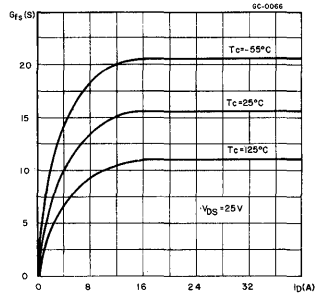
Output characteristics



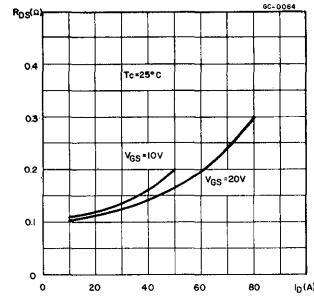
Transfer characteristics



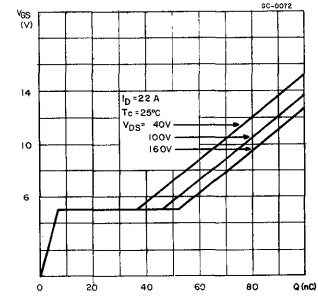
Transconductance



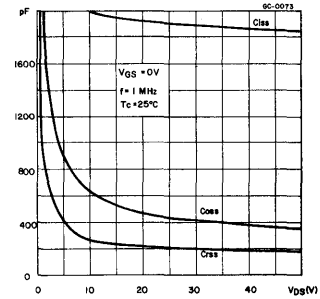
Static drain-source on resistance



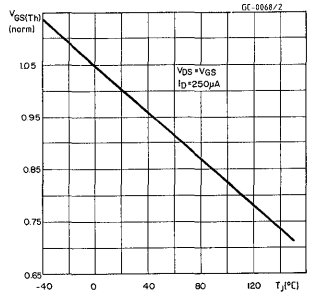
Gate charge vs gate-source voltage



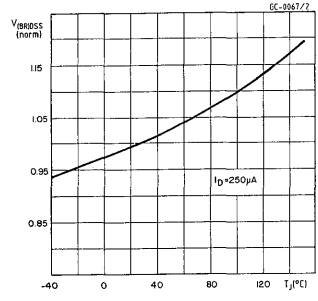
Capacitance variation



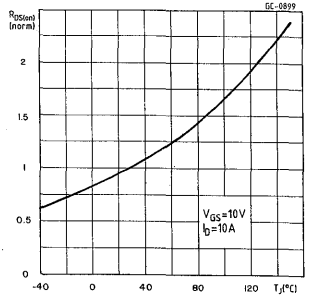
Normalized gate threshold voltage vs temperature



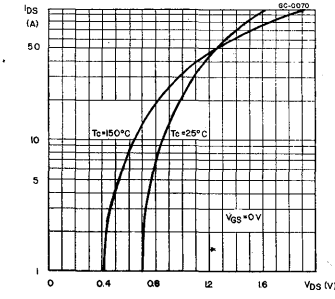
Normalized breakdown voltage vs temperature



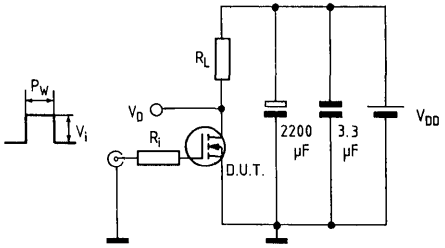
Normalized on resistance vs temperature



Source-drain diode forward characteristics

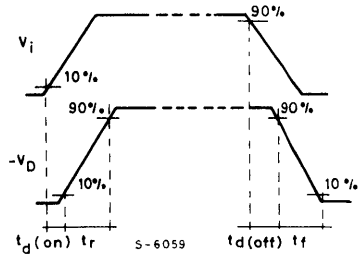


Switching times test circuit for resistive load

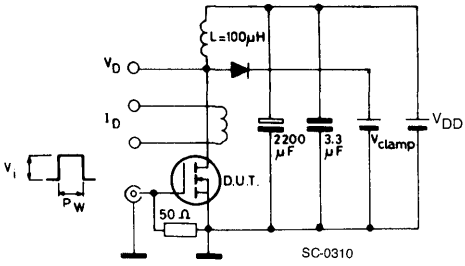


Pulse width ≤ 100 µs
Duty cycle ≤ 2%
V_i = 10 V

Switching time waveforms for resistive load

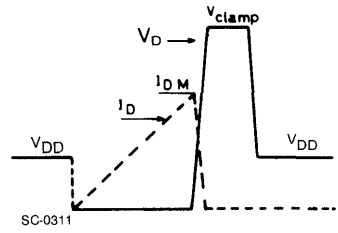


Clamped inductive load test circuit

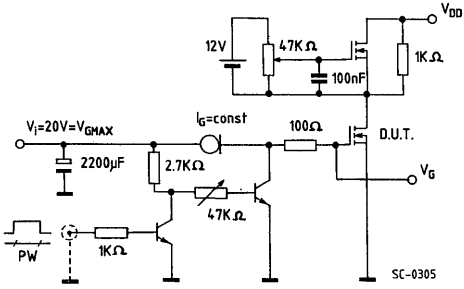


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

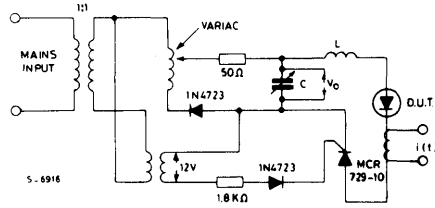


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP579

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

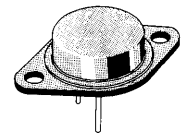
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP579	500 V	0.7 Ω	9 A

- HIGH SPEED SWITCHING APPLICATIONS
- HIGH VOLTAGE - 9A FOR UP TO 350W SMPS
- ULTRA FAST SWITCHING - FOR OPERATION AT > 100KHz
- EASY DRIVE - REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

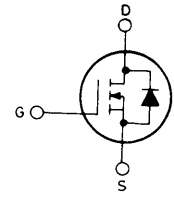
- SWITCHING MODE POWER SUPPLIES
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS transistor ideal for high speed switching applications. Typical applications include switching mode power supplies, uninterruptible power supplies and motor speed control.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20$ KΩ)	500	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	9	A
I_D	Drain current (cont.) at $T_c = 100°C$	5.6	A
I_{DM} (•)	Drain current (pulsed)	36	A
I_{DLM} (•)	Drain inductive current, clamped	36	A
P_{tot}	Total dissipation at $T_c < 25°C$	150	W
	Derating factor	1.2	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 4.5 A V_{GS} = 10 V I_D = 4.5 A T_c = 100°C			0.7 1.4	Ω Ω
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 4.5 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1600	1900 280 170	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 250 V I_D = 4.5 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		30 40 130 30	40 60 170 40	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

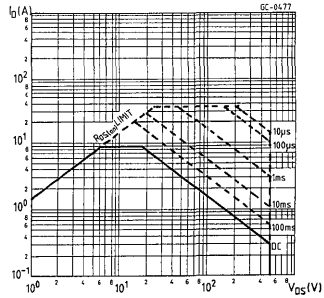
Parameters	Test Conditions	Min.	Typ.	Max.	Unit

SOURCE DRAIN DIODE

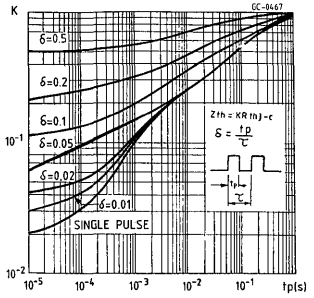
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)				9 36	A A
V_{SD}	Forward on voltage	I_{SD} = 9 A	V_{GS} = 0		1.15	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A di/dt = 100 A/μs	V_{GS} = 0	420		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

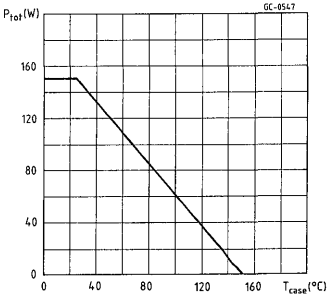
Safe operating areas



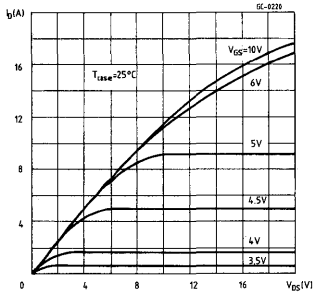
Thermal impedance



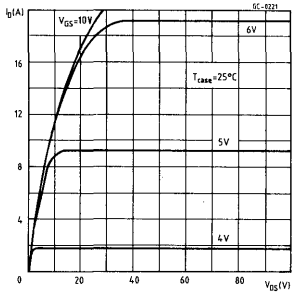
Derating curve



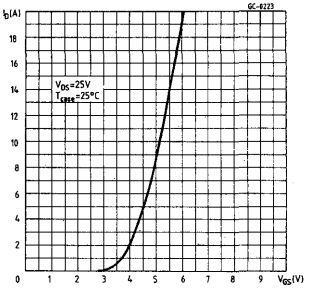
Output characteristics



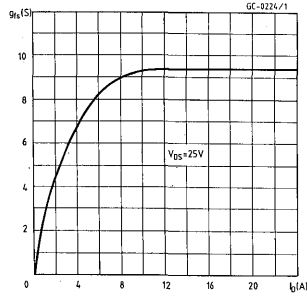
Output characteristics



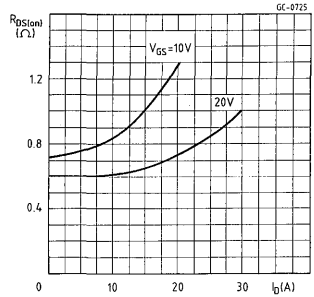
Transfer characteristics



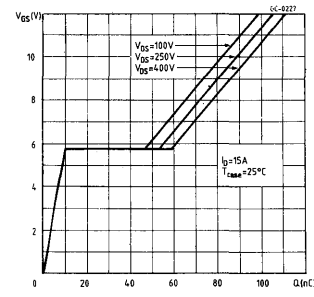
Transconductance



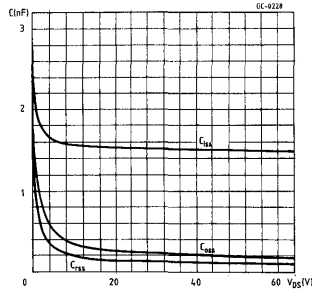
Static drain-source on resistance



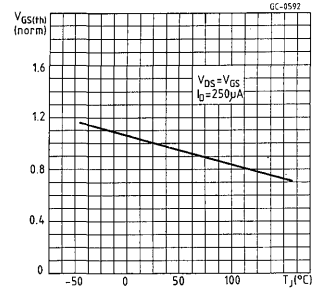
Gate charge vs gate-source voltage



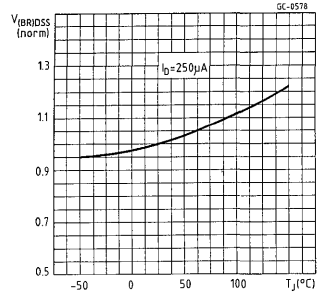
Capacitance variation



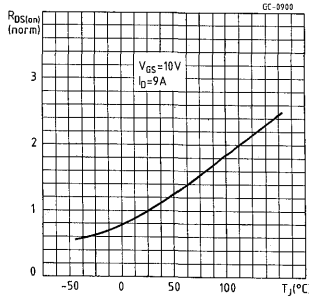
Normalized gate threshold voltage vs temperature



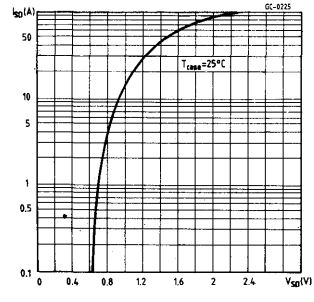
Normalized breakdown voltage vs temperature



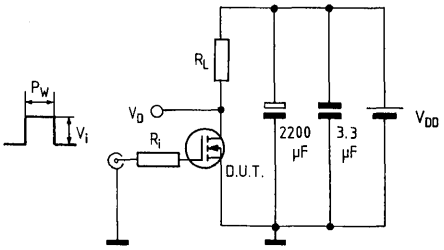
Normalized on resistance vs temperature



Source-drain diode forward characteristics

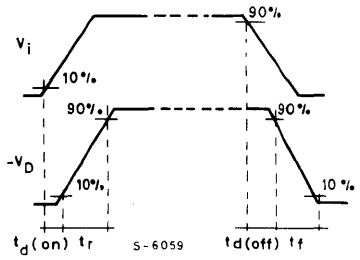


Switching times test circuit for resistive load

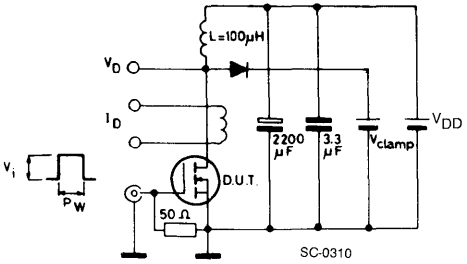


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

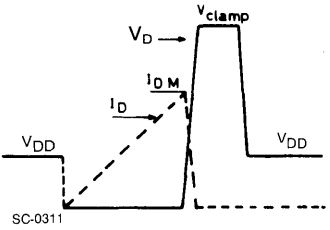


Clamped inductive load test circuit

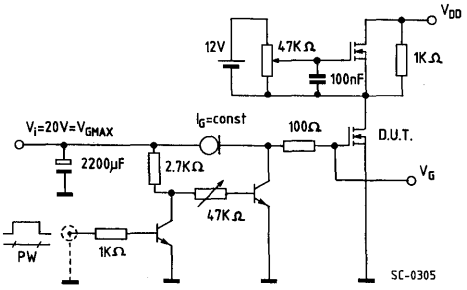


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

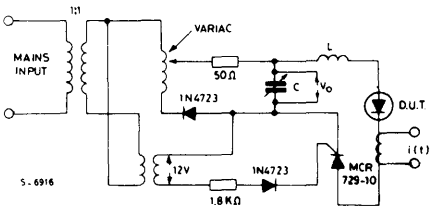


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

SGSP591
SGSP592

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

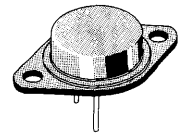
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
SGSP591	60 V	0.033 Ω	40 A
SGSP592	50 V	0.033 Ω	40 A

- HIGH SPEED SWITCHING APPLICATIONS
- 50 - 60 VOLTS FOR INVERTERS AND UPS
- HIGH CURRENT - $V_{DS(on)} \leq$ 1V at 20A
- RATED FOR UNCLAMPED INDUCTIVE SWITCHING (ENERGY TEST) ♦
- EASY DRIVE - REDUCES SIZE AND COST

INDUSTRIAL APPLICATIONS:

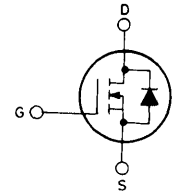
- DC/DC CONVERTERS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching circuits applications such as DC/DC converters, UPS, inverters, battery chargers and solar power converters.



TO-3

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		SGSP591	SGSP592	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±20		V
I_D	Drain current (cont.) at $T_c=25°C$	40		A
I_D	Drain current (cont.) at $T_c=100°C$	25		A
I_{DM} (•)	Drain current (pulsed)	160		A
P_{tot}	Total dissipation at $T_c<25°C$	150		W
	Derating factor	1.2		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area
♦ Introduced in 1988 week 44

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	0.83	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

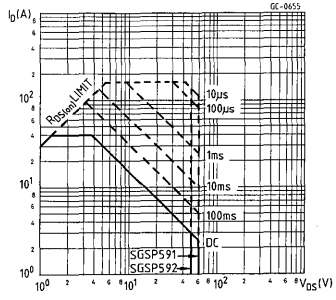
Parameters		Test Conditions	Min.	Typ.	Max.	Unit
OFF						
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0 for **SGSP591** for **SGSP592**	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
ON (*)						
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 20 A V_{GS} = 10 V I_D = 20 A T_c = 100°C			33 66	mΩ mΩ
ENERGY TEST						
I_{UIS}	Unclamped inductive switching current (single pulse)	V_{DD} = 30 V L = 100 μH starting T_j = 25°C	40			A
DYNAMIC						
g_{fs}	Forward transconductance	V_{DS} = 25 V I_D = 20 A	10			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	 V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1900	2800 1500 850	pF pF pF
SWITCHING						
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V I_D = 20 A V_i = 10 V R_i = 4.7 Ω (see test circuit)		35 110 90 55	45 145 120 70	ns ns ns ns

ELECTRICAL CHARACTERISTICS (Continued)

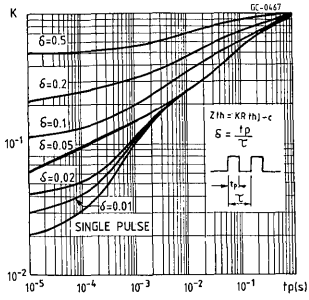
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					40 160	A A
V_{SD}	Forward on voltage	I_{SD} = 40 A	V_{GS} = 0			1.4	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A di/dt = 25 A/μs	V_{GS} = 0		140		ns

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

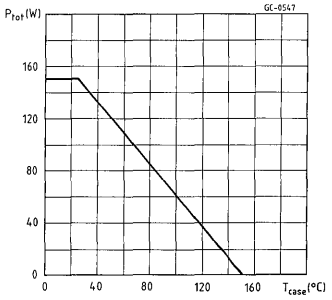
Safe operating areas



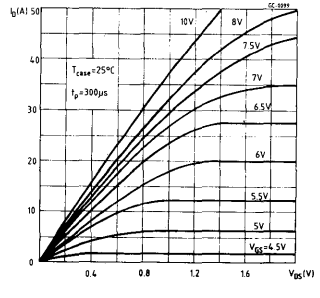
Thermal impedance



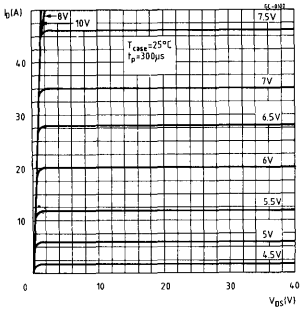
Derating curve



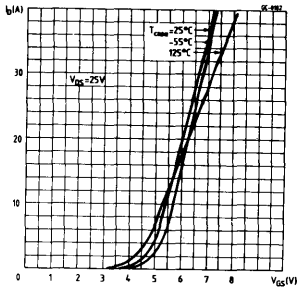
Output characteristics



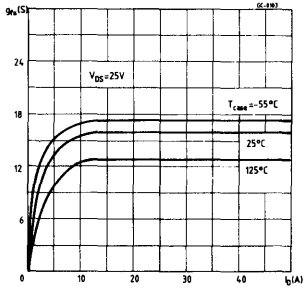
Output characteristics



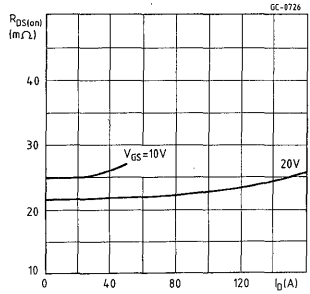
Transfer characteristics



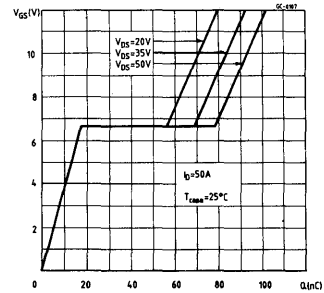
Transconductance



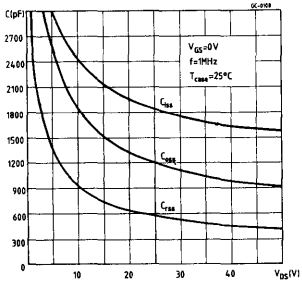
Static drain-source on resistance



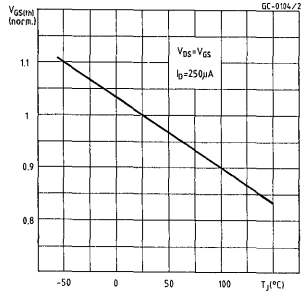
Gate charge vs gate-source voltage



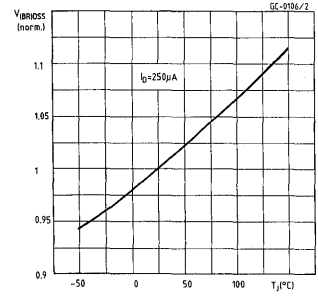
Capacitance variation



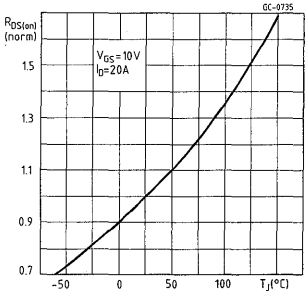
Normalized gate threshold voltage vs temperature



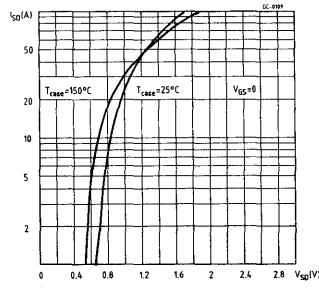
Normalized breakdown voltage vs temperature



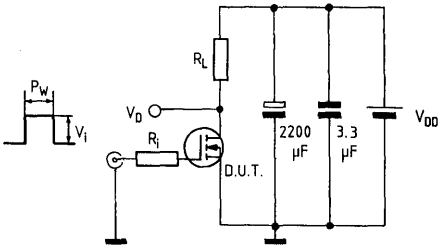
Normalized on resistance vs temperature



Source-drain diode forward characteristics

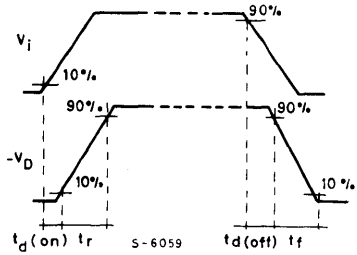


Switching times test circuit for resistive load

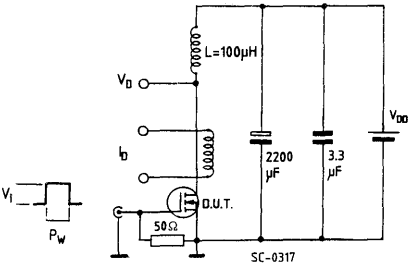


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

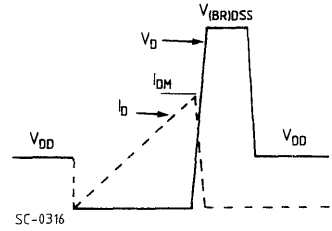


Unclamped inductive load test circuit

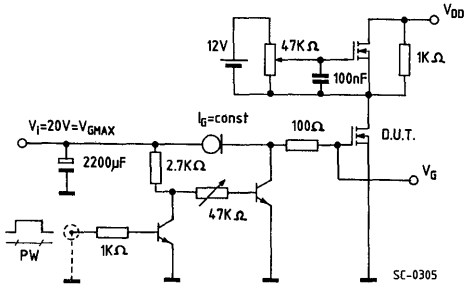


V_i= 12 V - Pulse width: adjusted to obtain specified I_{DM}

Unclamped inductive waveforms

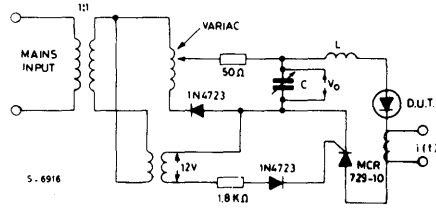


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

STHV82

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

ADVANCE DATA

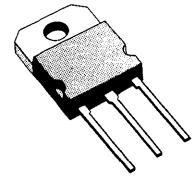
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STHV82	800 V	2 Ω	5.5 A

- 800 V - HIGH VOLTAGE FOR OFF-LINE APPLICATIONS
- ULTRA FAST SWITCHING FOR OPERATION AT 100 KHz
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

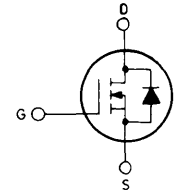
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for very high speed switching applications. It is ideal for off-line SMPS where a high breakdown voltage POWER MOS is required, particulary in single switch design such as flyback and forward converters.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	800	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at $T_c=25°C$	5.5	A
I_{DM}	Drain current (pulsed)	16	A
P_{tot}	Total dissipation at $T_c<25°C$	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

THERMAL DATA

$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2.5 A			2	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		1000 150 90		pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 400 V R_{GS} = 50 Ω	I_D = 2 A V_{GS} = 10 V		40 100 300 100		ns ns ns ns
Q_g	Total Gate Charge	V_{DD} = 500 V V_{GS} = 10 V	I_D = 6 A		70		nC

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE						
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				5.5 16	A A
V_{SD}	Forward on voltage	I_{SD} = 5.5 A V_{GS} = 0		1.4		V
t_{rr}	Reverse recovery time			1000		ns
Q_{rr}	Reverse recovery charge	I_{SD} = 5.5 A di/dt = 100A/μs		15		μC

SGS-THOMSON MICROELECTRONICS

STHV102

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

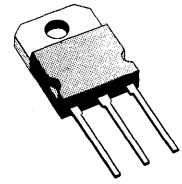
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STHV102	1000 V	3.5 Ω	4.2 A

- 1000 V - VERY HIGH VOLTAGE FOR SMPS
- EASY DRIVE - REDUCED COST AND SIZE
- ULTRA FAST SWITCHING
- HIGH RESOLUTION CTV DEFLECTION

INDUSTRIAL APPLICATIONS:

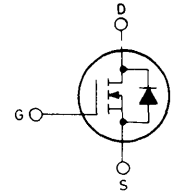
- SINGLE TRANSISTOR HIGH VOLTAGE SWITCH
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include single transistor forward and flyback converters and lamp ballast. They are also used in high voltage CTV EHT supplies, interfaces to thyristor and power transistors operating from 380V and 440V A.C. supplies and resonant converters operating up to 500kHz.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	1000	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c=25°C$	4.2	A
I_D	Drain current (cont.) at $T_c=100°C$	2.6	A
I_{DM} (•)	Drain current (pulsed)	16	A
P_{tot}	Total dissipation at $T_c<25°C$	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	−65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

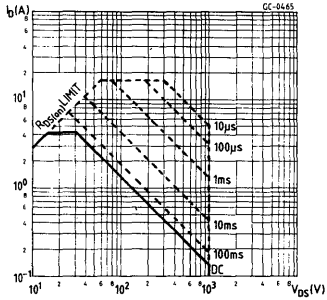
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	1000			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 2 A			3.5	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 2 A	2			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		900 150 90	1200 250 110	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 400 V V_i = 10 V (see test circuit)	I_D = 2 A R_i = 50 Ω		40 100 300 100		ns ns ns ns
Q_g	Total gate Charge	V_{DD} = 500 V V_{GS} = 10 V	I_D = 6 A			70	nC

ELECTRICAL CHARACTERISTICS (Continued)

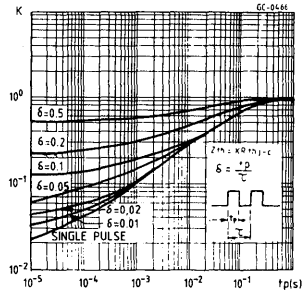
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM} (•)	Source-drain current Source-drain current (pulsed)					4.2 16	A A
V_{SD}	Forward on voltage	I_{SD} = 4.2 A	V_{GS} = 0			2.5	V
t_{rr}	Reverse recovery time	I_{SD} = 4.2 A di/dt = 100 A/μs	V_{GS} = 0		1000		ns
Q_{rr}	Reverse recovery charge				15		μC

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%
(•) Pulse width limited by safe operating area

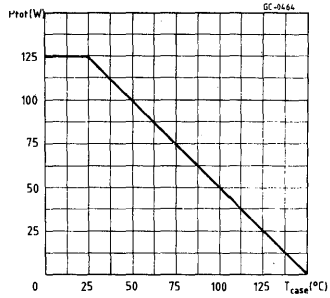
Safe operating areas



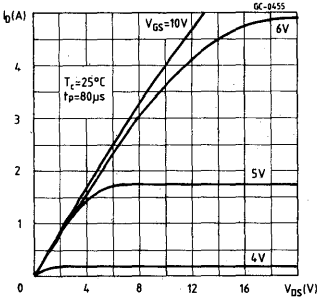
Thermal impedance



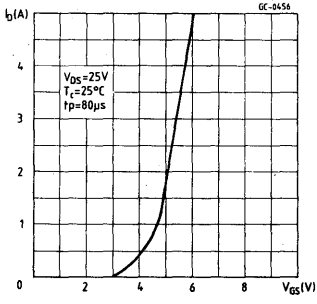
Derating curve



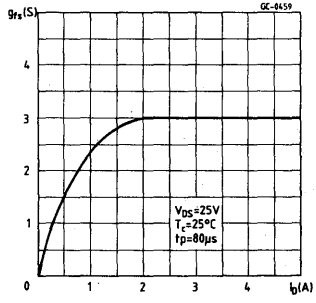
Output characteristics



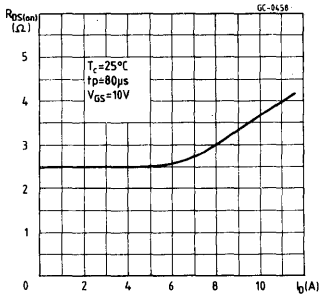
Transfer characteristic



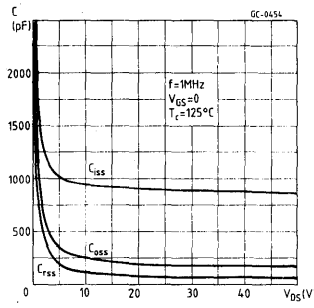
Transconductance



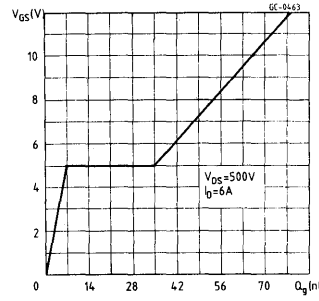
Static drain-source on resistance



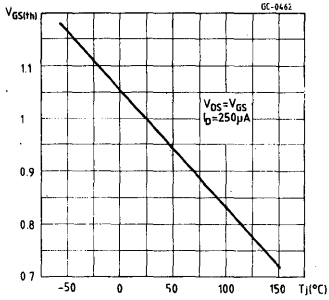
Capacitance variation



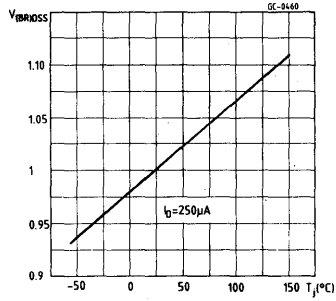
Gate charge vs gate-source voltage



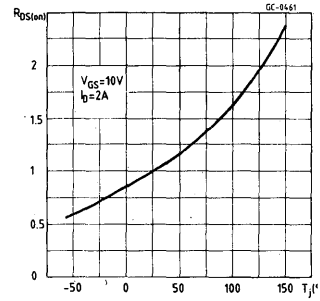
Normalized gate threshold voltage vs temperature



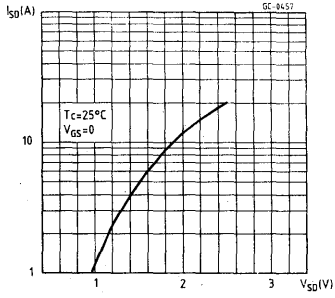
Normalized breakdown voltage vs temperature



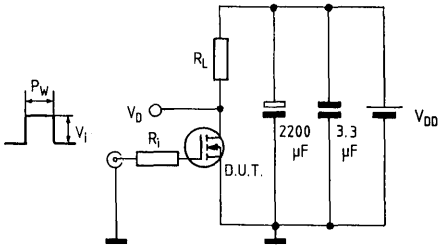
Normalized on resistance vs temperature



Static drain diode forward characteristic

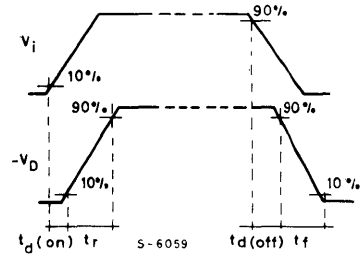


Switching times test circuit for resistive load

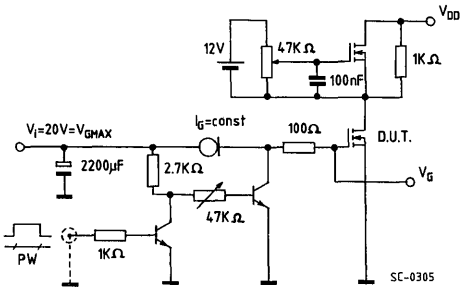


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

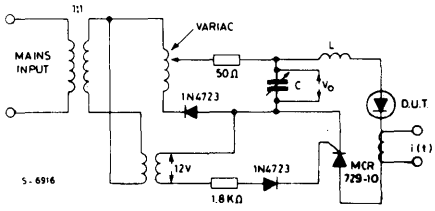


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

STLT20
STLT19

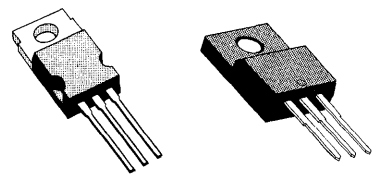
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTORS

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STLT20	60 V	0.15 Ω	15 A
STLT20FI	60 V	0.15 Ω	10 A
STLT19	50 V	0.15 Ω	15 A
STLT19FI	50 V	0.15 Ω	10 A

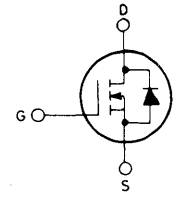
- LOGIC LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive enviroment.



TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		TO-220 ISOWATT220	STLT20 STLT20FI	STLT19 STLT19FI	
V_{DS}	Drain-source voltage ($V_{GS}=0$)		60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)		60	50	V
V_{GS}	Gate-source voltage		±15		V
			TO-220	**ISOWATT220**	
I_D	Drain current (cont.) at $T_c=25°C$		15	10	A
I_D	Drain current (cont.) at $T_c=100°C$		9.5	6.3	A
I_{DM}(•)	Drain current (pulsed)		40	40	A
P_{tot}	Total dissipation at $T_c<25°C$		75	30	W
	Derating factor		0.6	0.24	W/°C
T_{stg}	Storage temperature		−65 to 150		°C
T_j	Max. operating junction temperature		150		°C

•) Pulse width limited by safe operating area

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1.67	4.16	°C/W
T_l	Maximum lead temperature for soldering purpose	max	275		°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

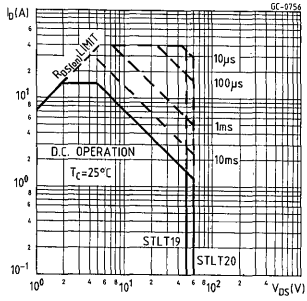
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA for **STLT20/FI** for **STLT19/FI**	V_{GS} = 0	60 50			V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±15 V				±100	nA
ON **							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	1		2.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 5 V	I_D = 7.5 A			0.15	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 15 V	I_D = 7.5 A	5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		480 170 40		pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V V_i = 5 V	I_D = 7.5 A R_i = 50 Ω		10 70 35 40		ns ns ns ns
Q_g	Total Gate Charge	V_{DD} = 48 V V_{GS} = 5 V	I_D = 15 A		8	13	nC

ELECTRICAL CHARACTERISTICS (Continued)

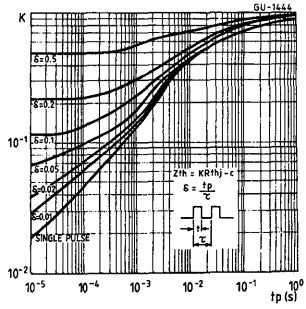
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD}	Source-drain current					15	A
I_{SDM}(•)	Source-drain current (pulsed)					60	A
V_{SD}**	Forward on voltage	I_{SD} = 15 A	V_{GS} = 0			1.25	V
t_{rr}	Reverse recovery time				80		ns
Q_{rr}	Reverse recovered charge	I_{SD} = 15 A	di/dt = 100A/μs		0.15		μC

** Pulsed: Pulse duration $\leqslant$ 300 μs, duty cycle $\leqslant$ 2%
(•) Pulse width limited by safe operating area

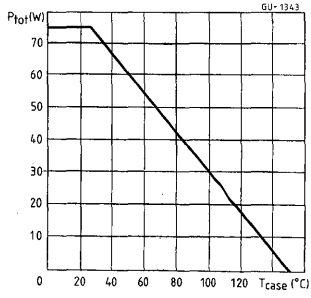
Safe operating areas (standard package)



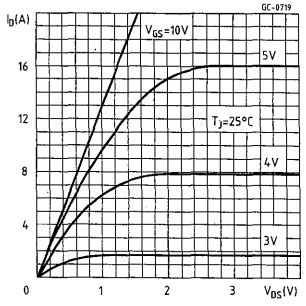
Thermal impedance (standard package)



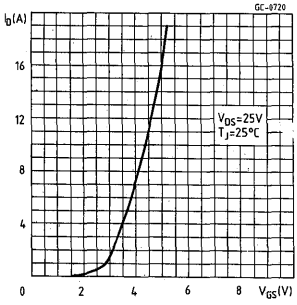
Derating curve (standard package)



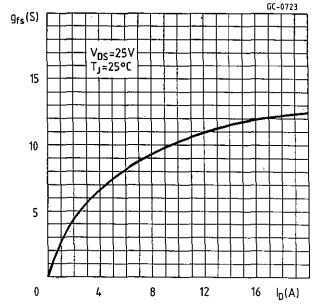
Output characteristics



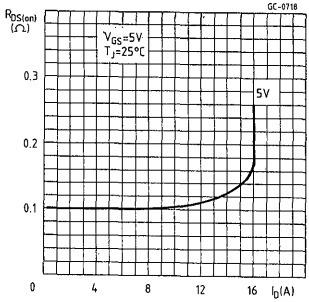
Transfer characteristics



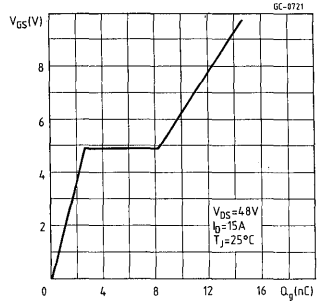
Transconductance



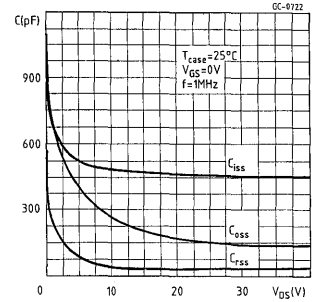
Static drain-source on resistance



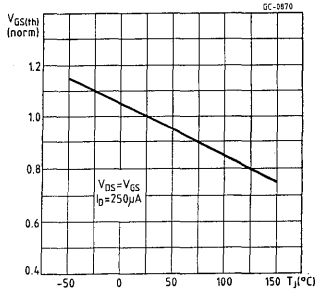
Gate charge vs gate-source voltage



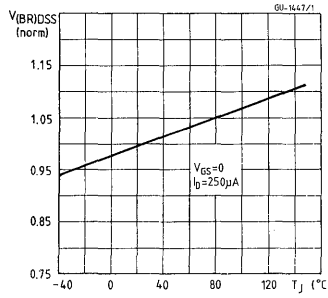
Capacitance variation



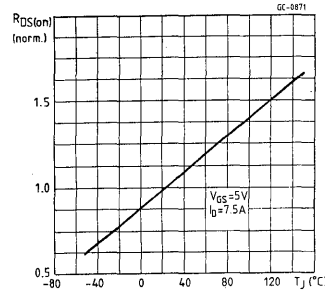
Normalized gate threshold voltage vs temperature



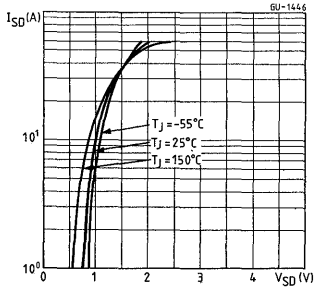
Normalized breakdown voltage vs temperature



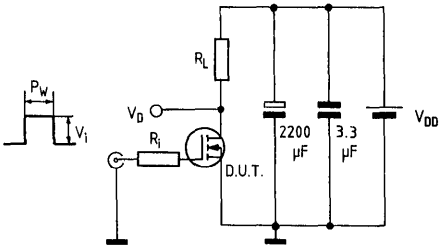
Normalized on resistance vs temperature



Source-drain diode forward characteristics

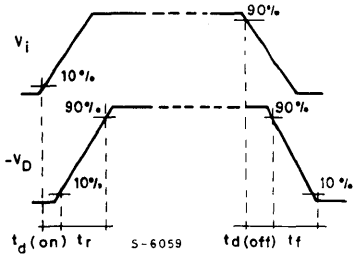


Switching times test circuit for resistive load

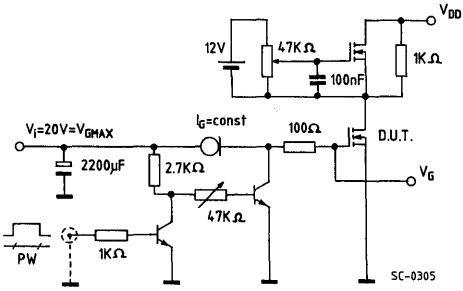


Pulse width $\leqslant$ 100 μs
Duty cycle $\leqslant$ 2%

Switching time waveforms for resistive load

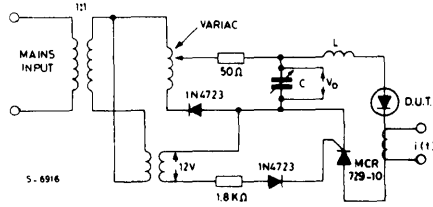


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this I_{Dmax} for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)\ (at\ 150°C)}}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

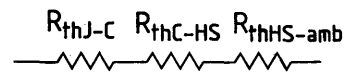
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

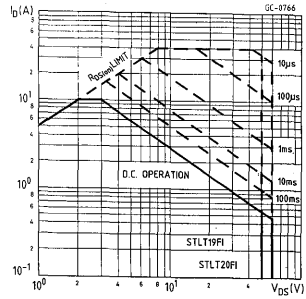
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

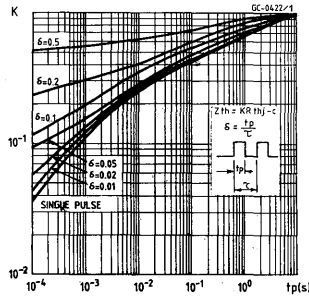


ISOWATT DATA

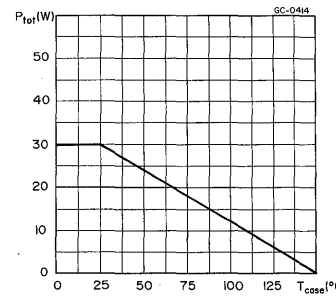
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

STLT30
STLT29

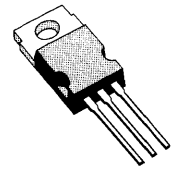
N - CHANNEL ENHANCEMENT MODE LOW THRESHOLD POWER MOS TRANSISTORS

ADVANCE DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STLT30	60 V	0.08 Ω	25 A
STLT29	50 V	0.08 Ω	25 A

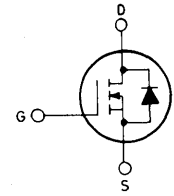
- LOGICAL LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive enviroment.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS		STLT30	STLT29	
V_{DS}	Drain-source voltage ($V_{GS}=0$)	60	50	V
V_{DGR}	Drain-gate voltage ($R_{GS}=20$ KΩ)	60	50	V
V_{GS}	Gate-source voltage	±15		V
I_D	Drain current (cont.) at $T_c=25°C$	25		A
I_D	Drain current (cont.) at $T_c=100°C$	15.7		A
I_{DM}	Drain current (pulsed)	80		A
P_{tot}	Total dissipation at $T_c<25°C$	100		W
	Derating factor	0.8		W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	1.25	°C/W
$R_{thj\text{ - amb}}$	Thermal resistance junction-ambient		75	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA for **STLT30** for **STLT29**	V_{GS} = 0	 60 50			 V V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±15 V				±100	nA
ON							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	1		2.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 5V	I_D = 12.5 A			0.08	Ω
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 15 V	I_D = 12.5 A	9			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		930	1200 600 130	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 25 V R_{GS} = 50 Ω	I_D = 12.5 A V_{GS} = 5 V		25 210 55 75		ns ns ns ns
Q_g	Total Gate Charge	V_{DS} = 25 V V_{GS} = 5 V	I_D = 25 A		19		nC

ELECTRICAL CHARACTERISTICS (Continued)

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE							
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)					25 80	A A
V_{SD}	Forward on voltage	I_{SD} = 25 A	V_{GS} = 0		1.5		V
t_{rr}	Reverse recovery time				300		ns
Q_{rr}	Reverse recovery charge	I_{SD} = 25 A	di/dt = 100A/μs		0.3		μC

SGS-THOMSON MICROELECTRONICS

STVHD90

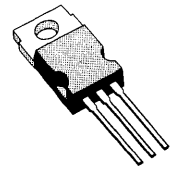
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STVHD90	50 V	0.023 Ω	52 A

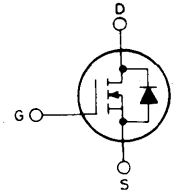
- VERY HIGH DENSITY
- VERY LOW $R_{DS\ (on)}$
- VERY HIGH CURRENT
- HIGH TRANSCONDUCTANCE/C_{rss} RATIO
- LOW DRIVE ENERGY
- ULTRA FAST SWITCHING

N - channel enhancement mode very high density POWER MOS transistors. Easy drive and low on voltage make this device ideal for automotive and industrial applications requiring high current and low on-losses. Typical uses are actuators lamp and motor control in the automotive and industrial enviroments. It can also be used in DC/DC converters.



TO-220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	50	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (cont.) at $T_c = 25°C$	52	A
I_D	Drain current (cont.) at $T_c = 125°C$	32	A
I_{DM} (•)	Drain current (pulsed)	200	A
I_{DLM}	Drain inductive current clamped	200	A
P_{tot}	Total dissipation at $T_c < 25°C$	125	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	− 65 to 150	°C
T_j	Max. operating junction temperature	150	°C

(•) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj\text{ - }case}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise specified)

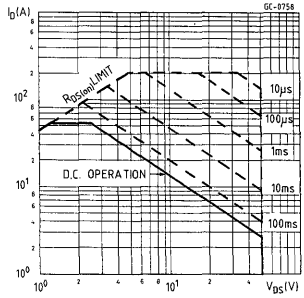
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8	T_c = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V	I_D = 30 A			23	mΩ
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 25 V	I_D = 30 A		30		mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		2500 850 120	3000 1000 150	pF pF pF
SWITCHING							
$t_{d\ (on)}$ t_r $t_{d\ (off)}$ t_f	Turn-on time Rise time Turn-off delay time Fall time	V_{DD} = 40 V V_i = 50 V (see test circuit)	I_D = 25 A R_i = 50 Ω			40 100 250 170	ns ns ns ns
Q_g	Total Gate Charge	V_{DD} = 25 V V_{GS} = 10 V	I_D = 30 A		56		nC

ELECTRICAL CHARACTERISTICS (Continued)

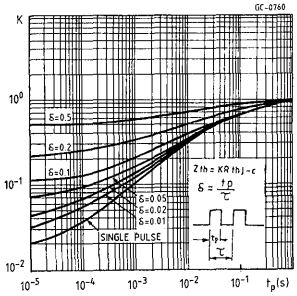
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DRAIN DIODE					
I_{SD} Source-drain current I_{SDM} (•) Source-drain current (pulsed)				52 200	A A
V_{SD} Forward on voltage	I_{SD} = 52 A V_{GS} = 0			1.5	V
t_{rr} Reverse recovery time Q_{rr} Reverse recovery charge	I_{SD} = 52 A V_{GS} = 0 di/dt = 100 A/μs		70 110		ns μC

(•) Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

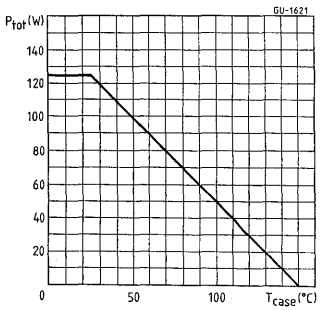
Safe operating areas



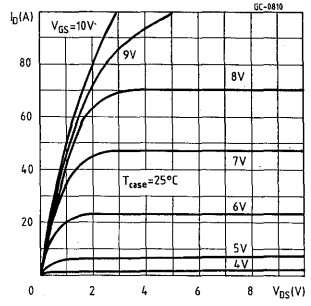
Thermal impedance



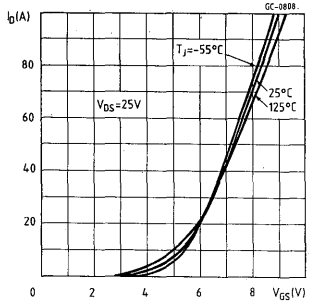
Derating curve



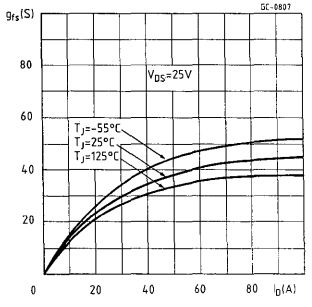
Output characteristics



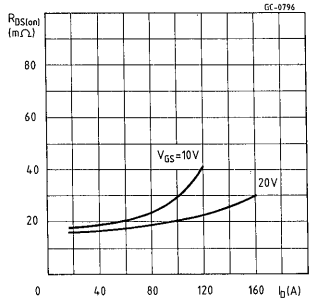
Transfer characteristics



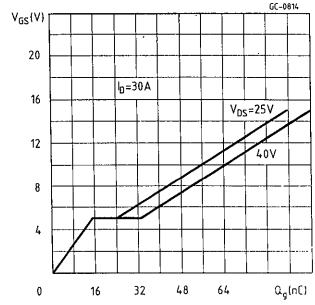
Transconductance



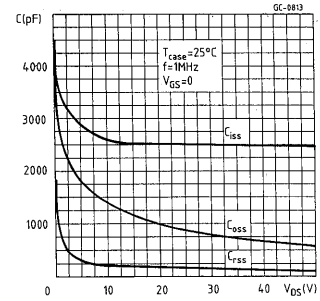
Static drain-source on resistance



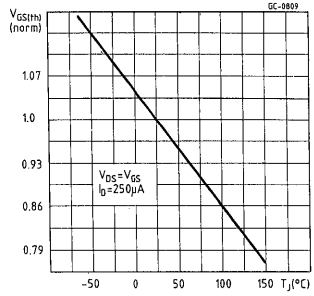
Gate charge vs gate-source voltage



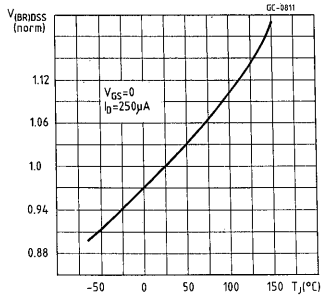
Capacitance variation



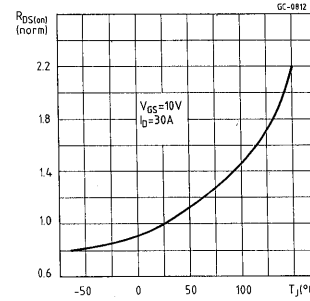
Normalized gate threshold voltage vs temperature



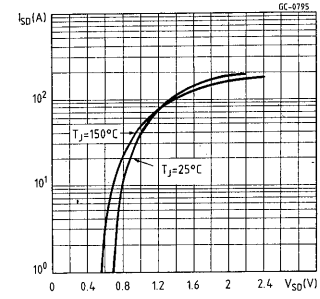
Normalized breakdown voltage vs temperature



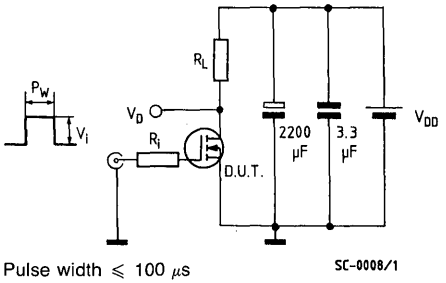
Normalized on resistance vs temperature



Static drain diode forward characteristics

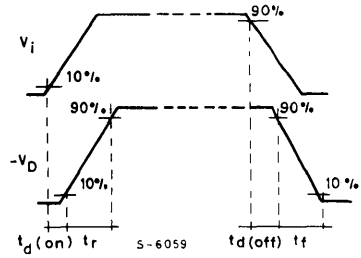


Switching times test circuit for resistive load

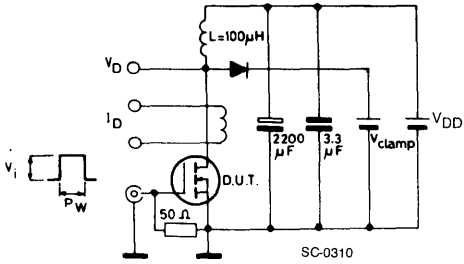


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

Switching time waveforms for resistive load

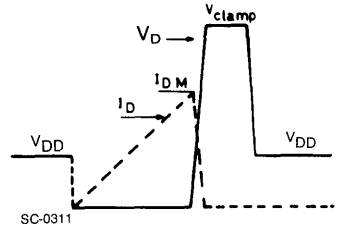


Clamped inductive load test circuit

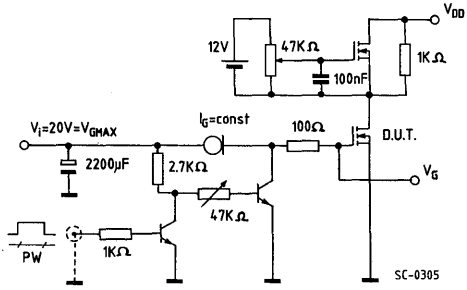


V_i = 12 V - Pulse width: adjusted to obtain specified I_{DM}, V_{clamp} = 0.75 $V_{(BR)\ DSS}$.

Clamped inductive waveforms

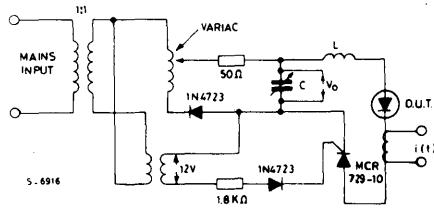


Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit



SGS-THOMSON MICROELECTRONICS

STHI07N50
STHI07N50FI

HIGH INJECTION N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS (IGBT)

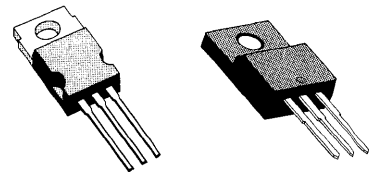
PRELIMINARY DATA

TYPE	V_{DSS}	I_D
STHI07N50	500 V	7 A
STHI07N50FI	500 V	7 A

- HIGH INPUT IMPEDANCE
- LOW ON-VOLTAGE
- HIGH CURRENT CAPABILITY

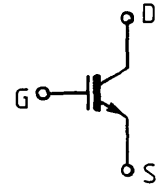
APPLICATIONS:
- AUTOMOTIVE IGNITION
- DRIVERS FOR SOLENOIDS AND RELAYS

N - channel High Injection POWER MOS transistors (IGBT) which features a high impedance insulated gate input and a low on-resistance characteristic of bipolar transistors. This low resistance is achieved by conductivity modulation of the drain. These devices are particularly suited to automative ignition switching. They can also be used as drivers for solenoids and relays.



TO-220 **ISOWATT220**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS}=0$)	500		V
V_{GS}	Gate-source voltage	±20		V
I_D(•)	Drain current (contin.) at $T_c=25°C$	7		A
I_{DM}	Drain current (pulsed)	20		A
		STHI07N50	**STHI07N50FI**	
P_{tot}	Total dissipation at $T_c<25°C$	100	35	W
	Derating factor	0.8	0.28	W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA ■

		TO-220	ISOWATT220	
$R_{thj\text{ - }case}$ Thermal resistance junction-case	max	1.25	3.6	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
OFF					
$V_{(BR)\ DSS}$ Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	500			V
I_{DSS} Zero gate voltage drain current ($V_{GS} = 0$)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS} Gate-body leakage current ($V_{DS} = 0$)	V_{GS} = ±20 V			±100	nA
ON (*)					
$V_{GS\ (th)}$ Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$V_{DS\ (on)}$ Drain-source voltage	V_{GS} = 10 V I_D = 7 A			2.7	V
DYNAMIC					
g_{fs} Forward transconductance	V_{DS} = 20 V I_D = 7 A	2.5			mho
C_{iss} Input capacitance C_{oss} Output capacitance C_{rss} Reverse transfer capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		850 90 40	950 140 80	pF pF pF
SWITCHING					
RESISTIVE LOAD $t_{d\ (on)}$ Turn-on delay time t_r Rise time $t_{d\ (off)}$ Turn-off delay time t_f Fall time	V_{DD} = 400 V I_D = 10 A V_g = 10 V R_g = 100 Ω		 100 700 500 800	 150 1000 700 1500	 ns ns ns ns

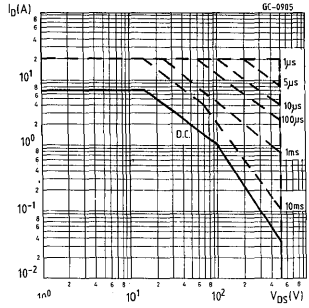
ELECTRICAL CHARACTERISTICS (Continued)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING (continued)					
INDUCTIVE LOAD $t_{d\ (off)}$ Turn-off delay time t_f Fall time	V_{DD} = 12 V $V_{DS\ clamp}$ = 350 V I_D = 7 A V_{GS} = 10 V R_g = 100 Ω L = 10 mH T_j = 100°C		1 1.1	1.4 1.5	μs μs
USE TEST	V_{CC} = 14 V $V_{DS\ clamp}$ = 400 V L = 7 mH	6			A

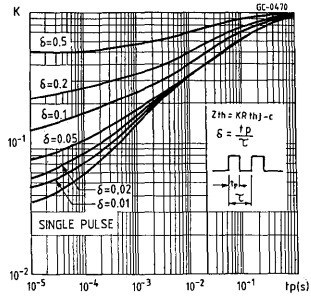
(*) Pulsed: Pulse duration = 300 μs, duty cycle 1,5%

■ See note on ISOWATT220 or this datasheet

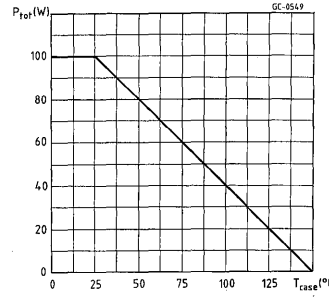
Safe operating areas (standard package)



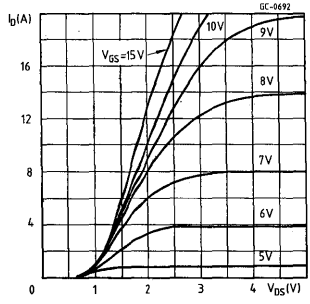
Thermal impedence (standard package)



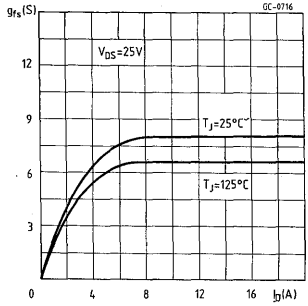
Derating curve (standard package)



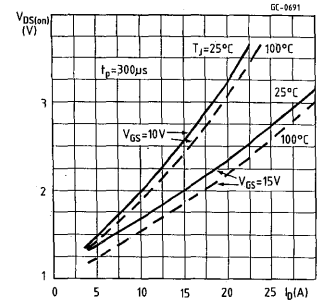
Output characteristics



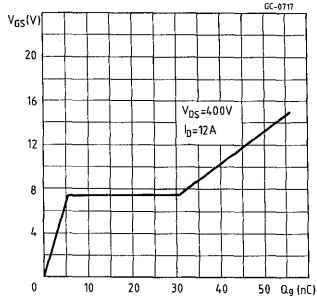
Transconductance



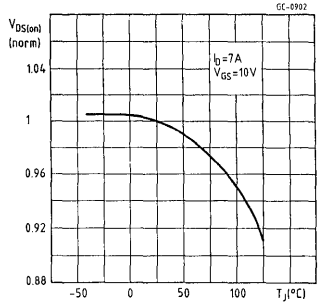
Static drain-souce on voltage



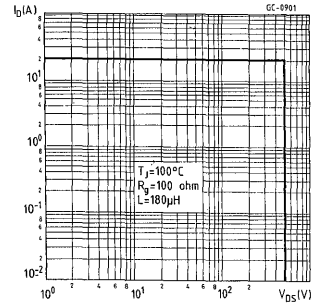
Gate charge vs gate-source voltage



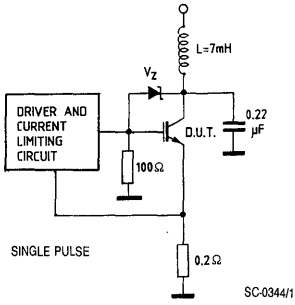
Normalized on voltage vs temperature



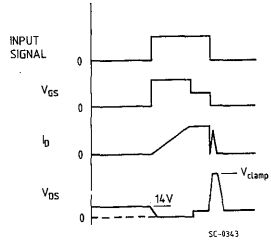
Reverse biased SOA



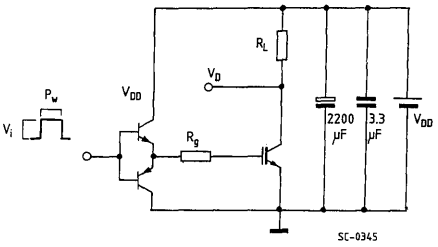
Functional test circuit



Functional test waveforms

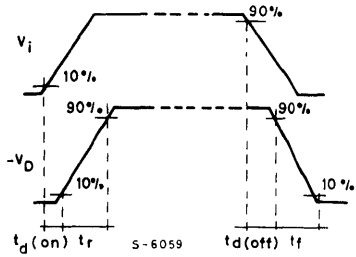


Switching times test circuit for resistive load

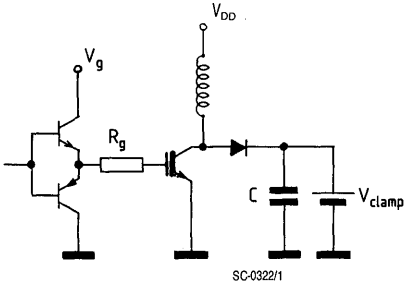


Pulse width ≤ 100 µs
Duty cycle ≤ 2%

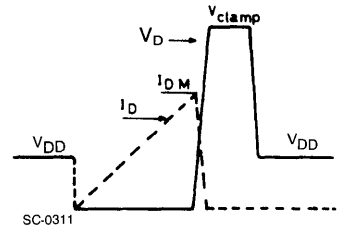
Switching time waveforms for resistive load



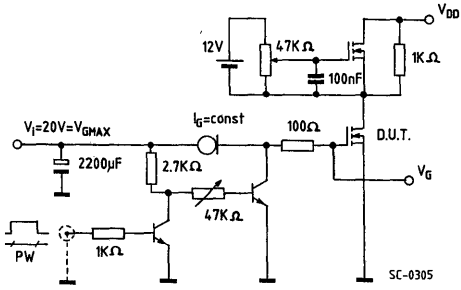
Clamped inductive load and RBSOA test circuit



Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

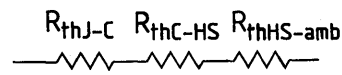
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

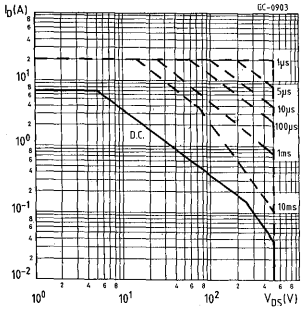
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

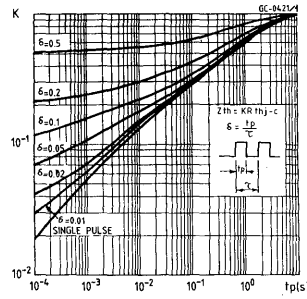


ISOWATT DATA

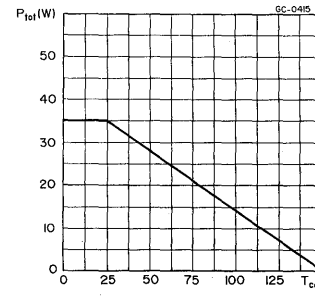
Safe operating areas



Thermal impedance



Derating curve



SGS-THOMSON MICROELECTRONICS

STHI10N50
STHI10N50FI

HIGH INJECTION N-CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS (IGBT)

PRELIMINARY DATA

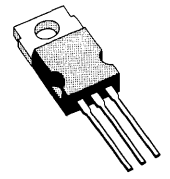
TYPE	V_{DSS}	I_D
STHI10N50	500 V	10 A
STHI10N50FI	500 V	10 A

- HIGH INPUT IMPEDANCE
- LOW ON-VOLTAGE
- HIGH CURRENT CAPABILITY
- FAST TURN-OFF: $t_f < 1.5\ \mu s$

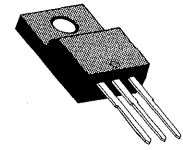
APPLICATIONS:

- MOTOR CONTROL

N - channel High Injection POWER MOS transistors (IGBT) which feature a high impedance insulated gate input and a low on-resistance characteristic of bipolar transistors. This low resistance is achieved by conductivity modulation of the drain. These devices are particularly suited to switching motor control applications in consumer equipment such as washing machines and tumble dryers and industrial equipment motor control.

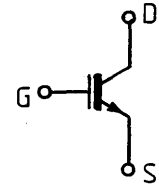


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500		V
V_{GS}	Gate-source voltage	±20		V
I_D(•)	Drain current (contin.) at $T_c = 25°C$	10		A
I_{DM}	Drain current (pulsed)	30		A
		STHI10N50	**STHI10N50FI**	
P_{tot}	Total dissipation at $T_c < 25°C$	100	35	W
	Derating factor	0.8	0.28	W/°C
T_{stg}	Storage temperature	−65 to 150		°C
T_j	Max. operating junction temperature	150		°C

(•) Pulse width limited by safe operating area

THERMAL DATA ■

			TO-220	ISOWATT220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	1.25	3.57	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

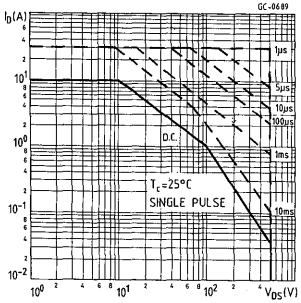
Parameters		Test Conditions		Min.	Typ.	Max.	Unit
OFF							
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA	V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C				250 1000	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V				±100	nA
ON (*)							
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS}	I_D = 250 μA	2		4	V
$V_{DS\ (on)}$	Drain-source voltage	V_{GS} = 15 V I_D = 10 A V_{GS} = 15 V I_D = 10 A T_j = 100°C				2.7 2.7	V V
DYNAMIC							
g_{fs}	Forward transconductance	V_{DS} = 20 V	I_D = 10 A	2.5			mho
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V V_{GS} = 0	f = 1 MHz		850 90 40	950 140 80	pF pF pF
SWITCHING							
	RESISTIVE LOAD						
$t_{d\ (on)}$	Turn-on delay time	V_{DD} = 400 V	I_D = 10 A		100	150	ns
t_r	Rise time	V_g = 15 V	R_g = 100 Ω		700	1000	ns
$t_{d\ (off)}$	Turn-off delay time				500	700	ns
t_f	Fall time				800	1500	ns

ELECTRICAL CHARACTERISTICS (Continued)

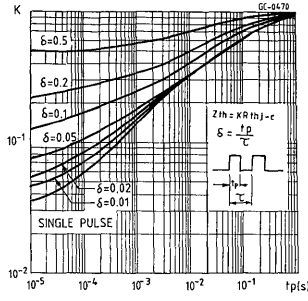
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
SWITCHING (continued)					
INDUCTIVE LOAD					
$t_{d\ (off)}$ Turn-off delay time	$V_{DS\ clamp}$ = 350 V I_D = 10 A		0.7	1.2	μs
t_f Fall time	V_g = 15 V R_g = 100 Ω		1.1	1.5	μs
t_{cross} Crossover time	L = 180 μH T_j = 100°C		1.7	2	μs
E_{off} Turn-off losses			4		mJ

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1,5%
(■) See note on ISOWATT220 in this datasheet

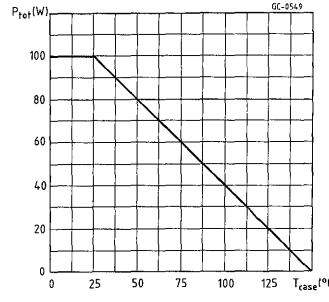
Safe operating areas (standard package)



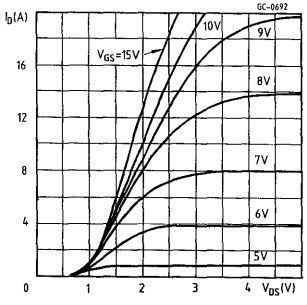
Thermal impedance (standard package)



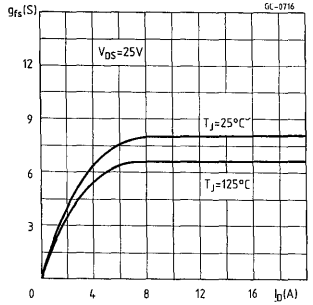
Derating curve (standard package)



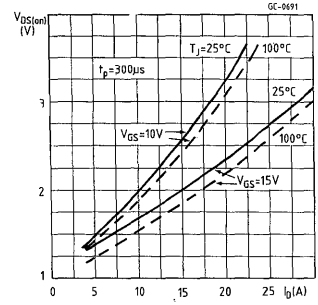
Output characteristics



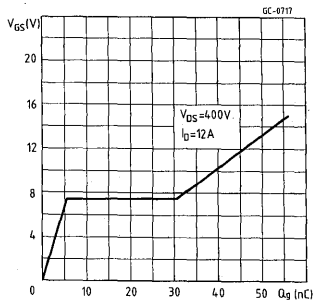
Transconductance



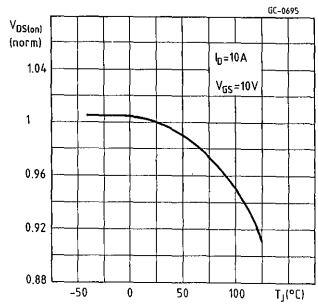
Static drain-souce on voltage



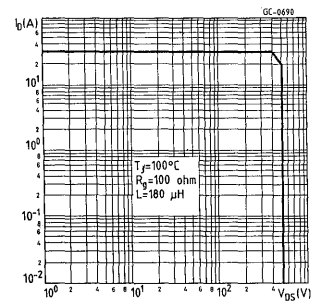
Gate charge vs gate-source voltage



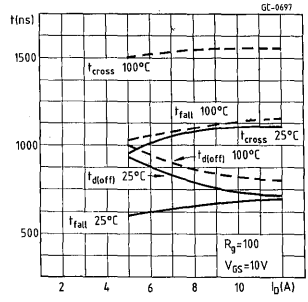
Normalized on voltage vs temperature



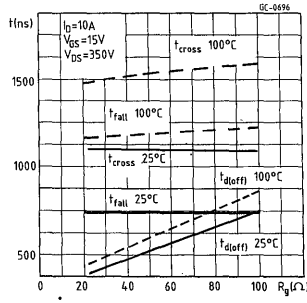
Reverse biased SOA



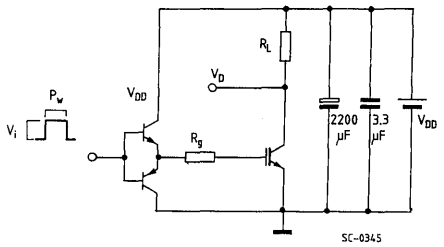
Switching times inductive load vs drain current



Switching times inductive load vs Rg

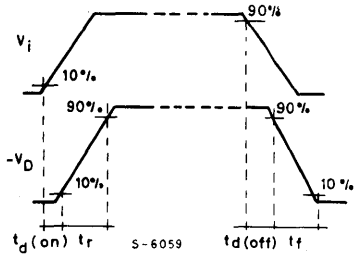


Switching times test circuit for resistive load

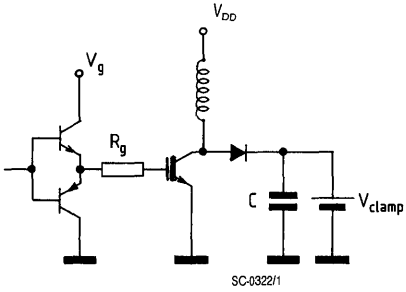


Pulse width ⩽ 100 µs
Duty cycle ⩽ 2%

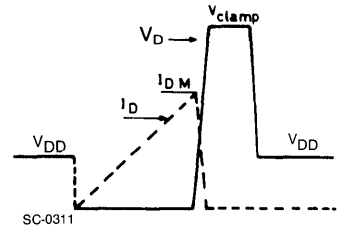
Switching time waveforms for resistive load



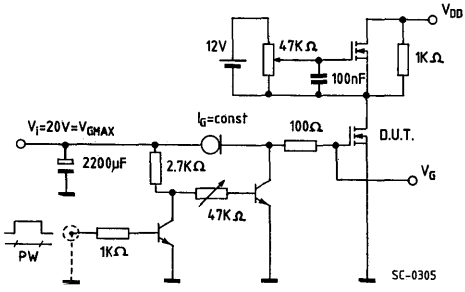
Clamped inductive load and RBSOA test circuit



Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.
The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.
ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

THERMAL IMPEDANCE OF ISOWATT220 PACKAGE

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.
The total thermal resistance $R_{th\ (tot)}$ is the sum of each of these elements.
The transient thermal impedance, Z_{th} for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ\text{-}C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

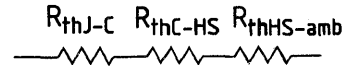
$$Z_{th} = R_{thJ\text{-}C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ\text{-}C} + R_{thC\text{-}HS} + R_{thHS\text{-}amb}$$

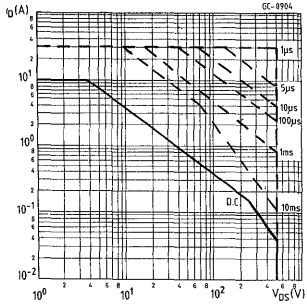
It is often possibile to discern these areas on transient thermal impedance curves.

Fig. 1

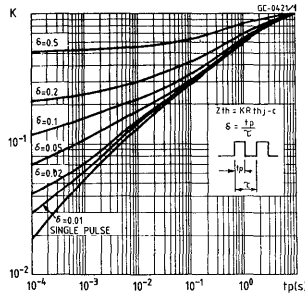


ISOWATT DATA

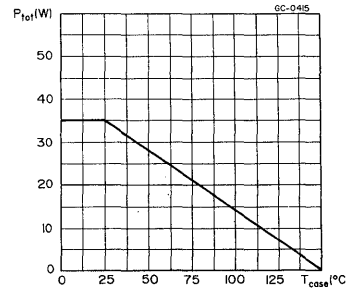
Safe operating areas



Thermal impedance



Derating curve



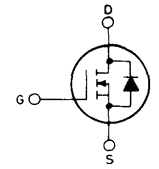
SGS-THOMSON MICROELECTRONICS

BUZ11 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 170 x 170 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 47 x 51 mils
  Gate: 15 x 18 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 20 mils
  Gate: Al - max 5 mils

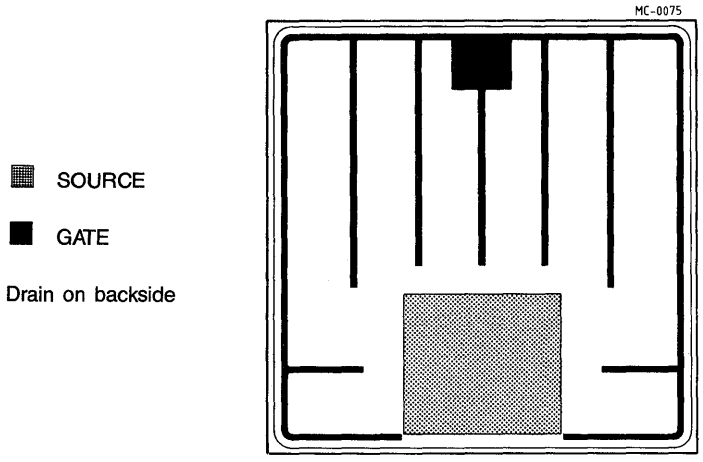
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
50 V	0.04 Ω	30 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 1.67°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.04	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

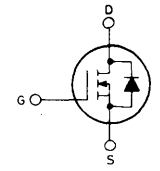
SGS-THOMSON MICROELECTRONICS

BUZ11A CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 156 x 156 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 40 x 34 mils
  Gate: 15 x 19 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 15 mils
  Gate: Al - max 7 mils

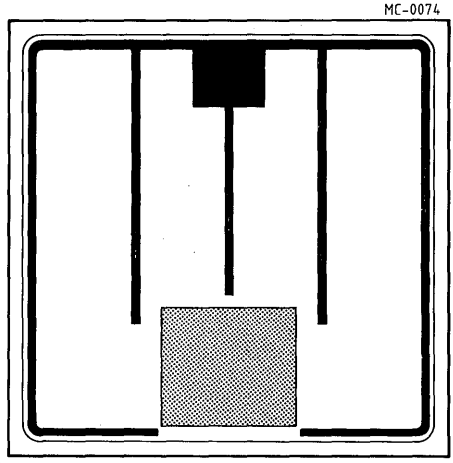
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
50 V	0.06 Ω	25 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



SOURCE

GATE

Drain on backside

* With $R_{thj\text{-}c}$ max. 1.67°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			60	mΩ

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

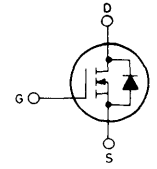
SGS-THOMSON MICROELECTRONICS

BUZ21 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 156 x 156 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 40 x 34 mils
  Gate: 15 x 19 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 15 mils
  Gate: Al - max 7 mils

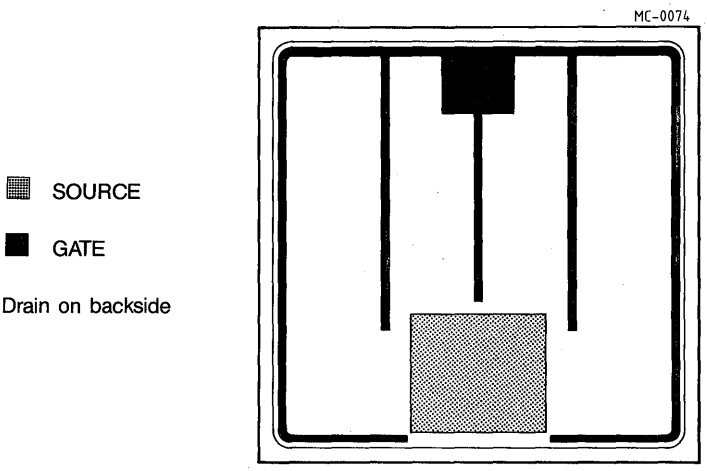
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
100 V	0.1 Ω	19 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 1.67°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.1	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width < 300 μs, duty cycle < 2%

2 - For detailed device characteristics please refer to the discrete device datasheet

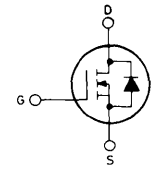
SGS-THOMSON MICROELECTRONICS

BUZ32 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 156 x 156 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 40 x 34 mils
  Gate: 15 x 19 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 10 mils
  Gate: Al - max 7 mils

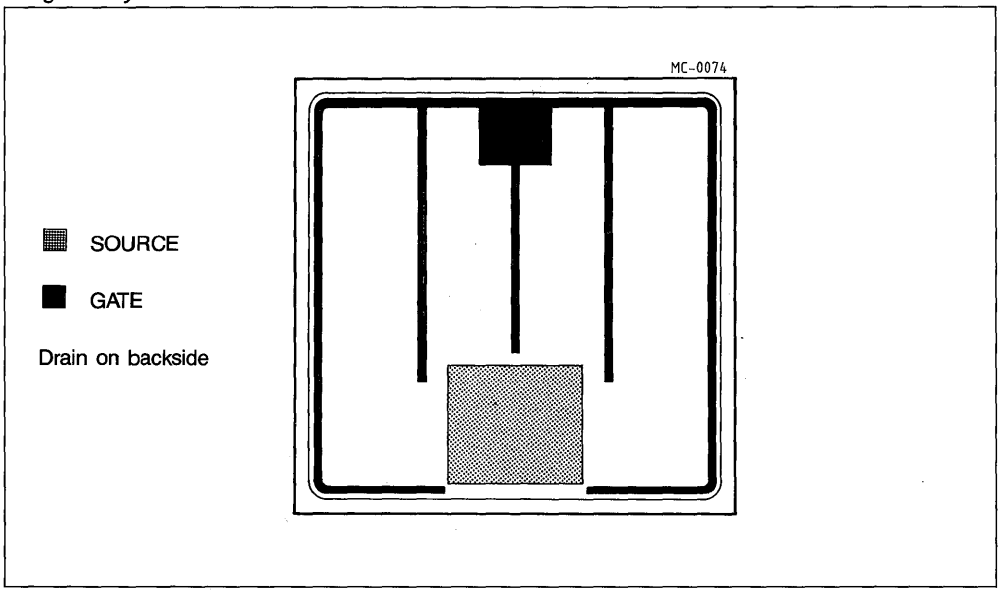
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
200 V	0.4 Ω	9.5 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 1.67°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.4	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

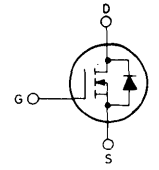
SGS-THOMSON MICROELECTRONICS

BUZ71 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 95 x 95 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 28 x 30 mils
  Gate: 16 x 18 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 10 mils
  Gate: Al - max 5 mils

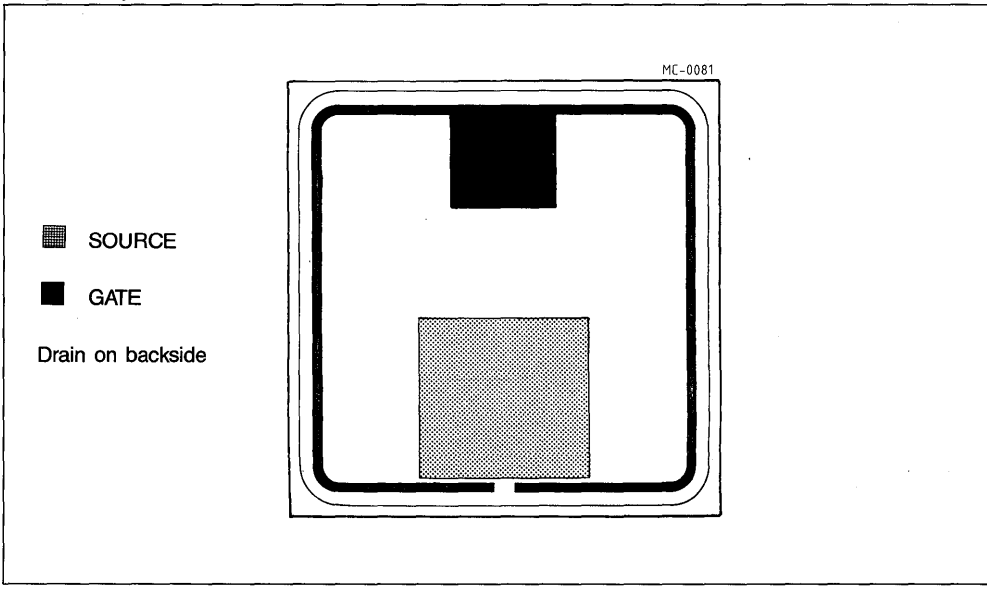
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
50 V	0.1 Ω	14 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 3.1°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2.1		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.1	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

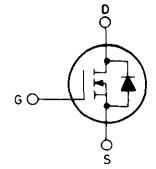
SGS-THOMSON MICROELECTRONICS

IRF151 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 221 x 221 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 56 x 43 mils
  Gate: 18 x 18 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 20 mils
  Gate: Al - max 7 mils

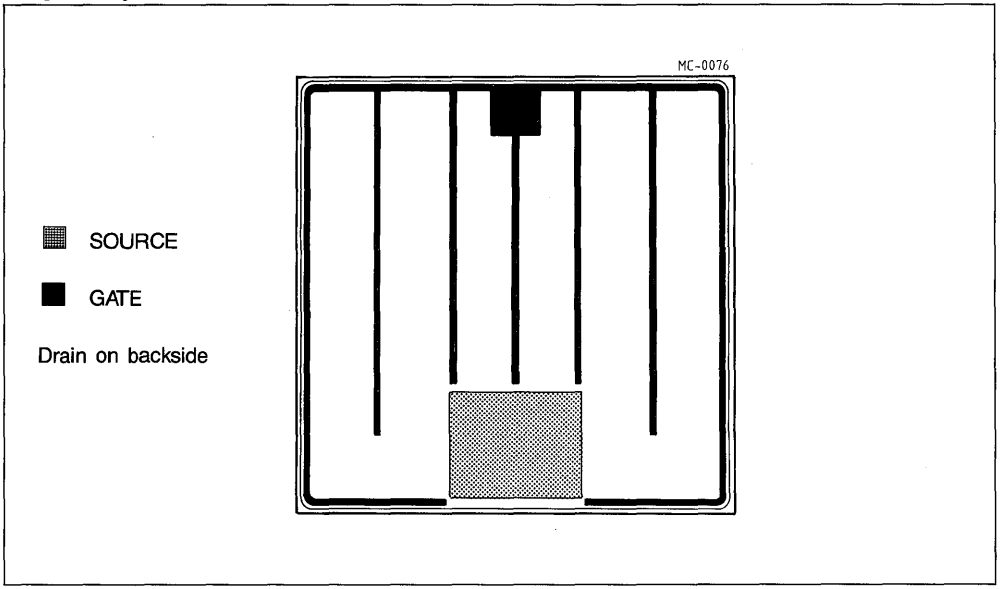
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
60 V	0.055 Ω	40 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 0.83°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			55	mΩ

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

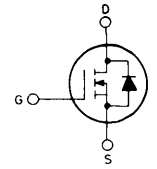
SGS-THOMSON MICROELECTRONICS

IRF520 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 95 x 95 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 28 x 30 mils
  Gate: 16 x 18 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 10 mils
  Gate: Al - max 5 mils

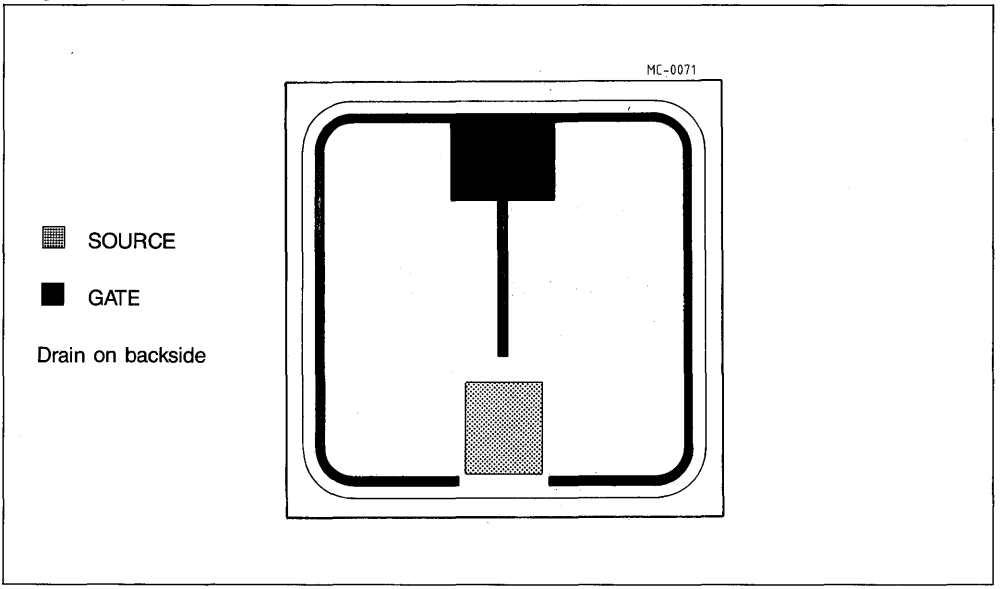
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
100 V	0.27 Ω	9.2 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 3.12°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.27	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

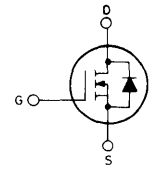
SGS-THOMSON MICROELECTRONICS

IRF540 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 170 x 170 mils
- METALLIZATION:
  - Top: Al
  - Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  - Source: 47 x 51 mils
  - Gate: 15 x 18 mils
- RECOMMENDED WIRE BONDING:
  - Source: Al - max 20 mils
  - Gate: Al - max 5 mils

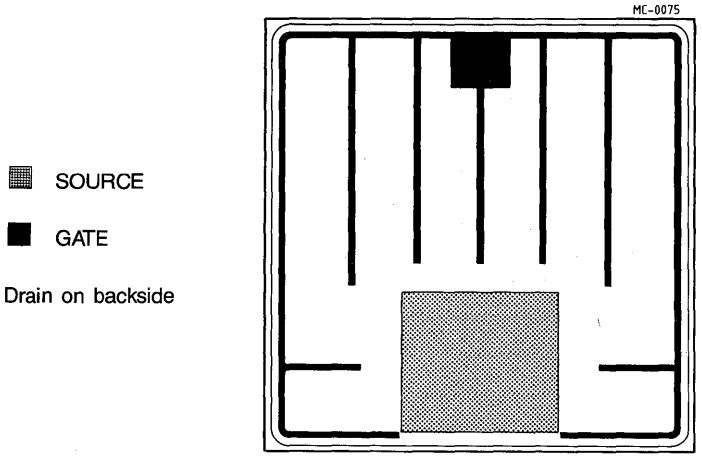
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
100 V	0.077 Ω	28 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 1°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			77	mΩ

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

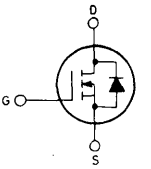
SGS-THOMSON MICROELECTRONICS

IRF620 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 110 x 110 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 19 x 27 mils
  Gate: 30 x 20 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 7 mils
  Gate: Al - max 7 mils

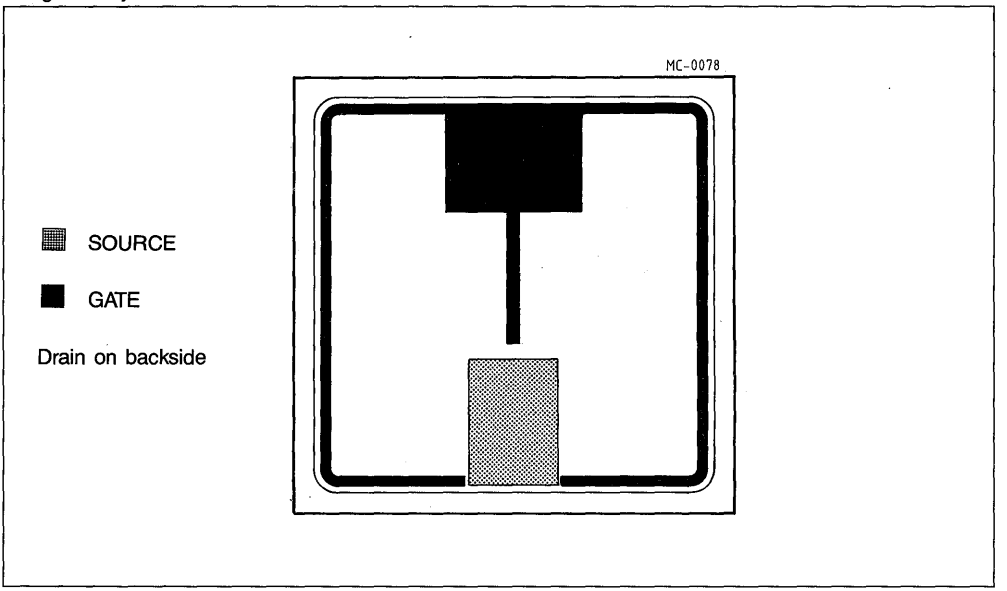
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
200 V	0.8 Ω	5 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 3.12°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating x 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.8	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

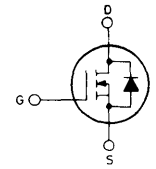
SGS-THOMSON MICROELECTRONICS

IRF720 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 110 x 110 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 16 x 21 mils
  Gate: 22 x 15 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 7 mils
  Gate: Al - max 7 mils

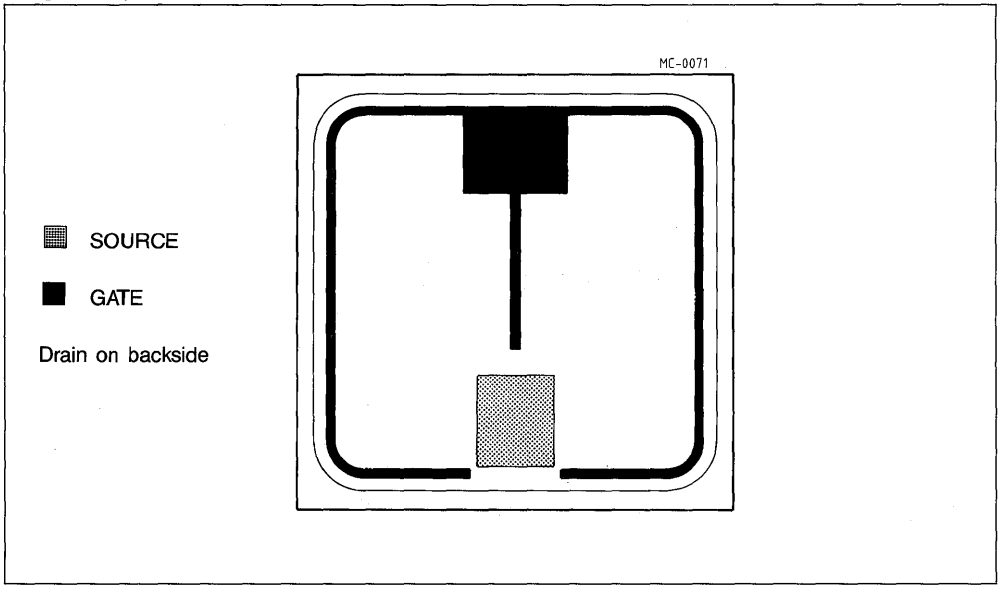
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
400 V	1.8 Ω	3.3 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 3.12°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			1.8	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

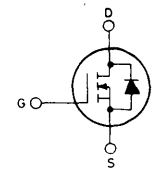
SGS-THOMSON MICROELECTRONICS

IRF730 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 156 x 156 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 30 x 24 mils
  Gate: 20 x 16 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 10 mils
  Gate: Al - max 7 mils

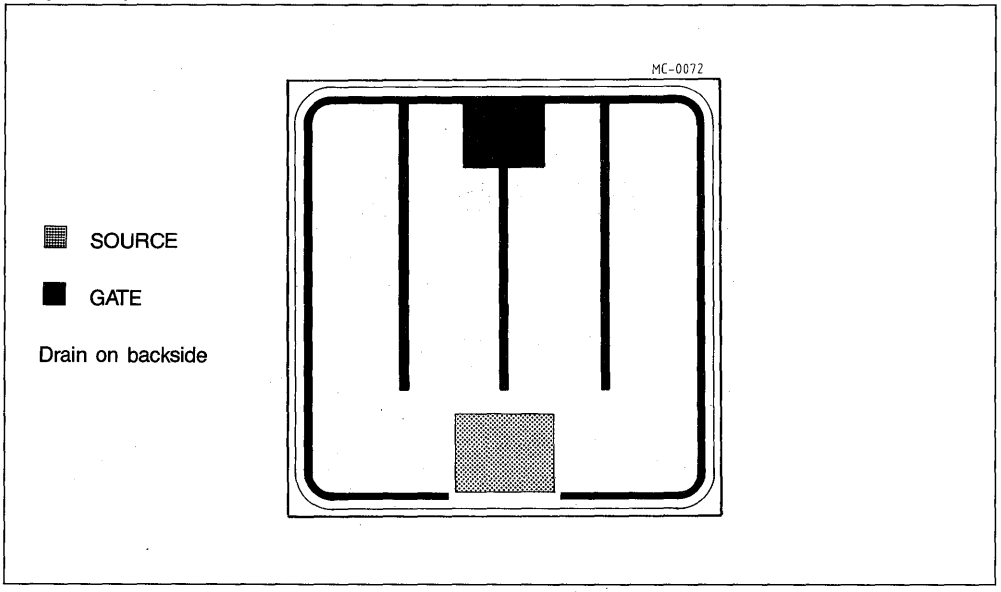
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
400 V	1 Ω	5.5 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 1.67°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			1	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

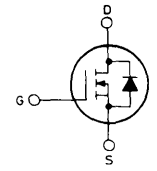
SGS-THOMSON MICROELECTRONICS

IRF740 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 180 x 220 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 29 x 23 mils
  Gate: 20 x 16 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 10 mils
  Gate: Al - max 6 mils

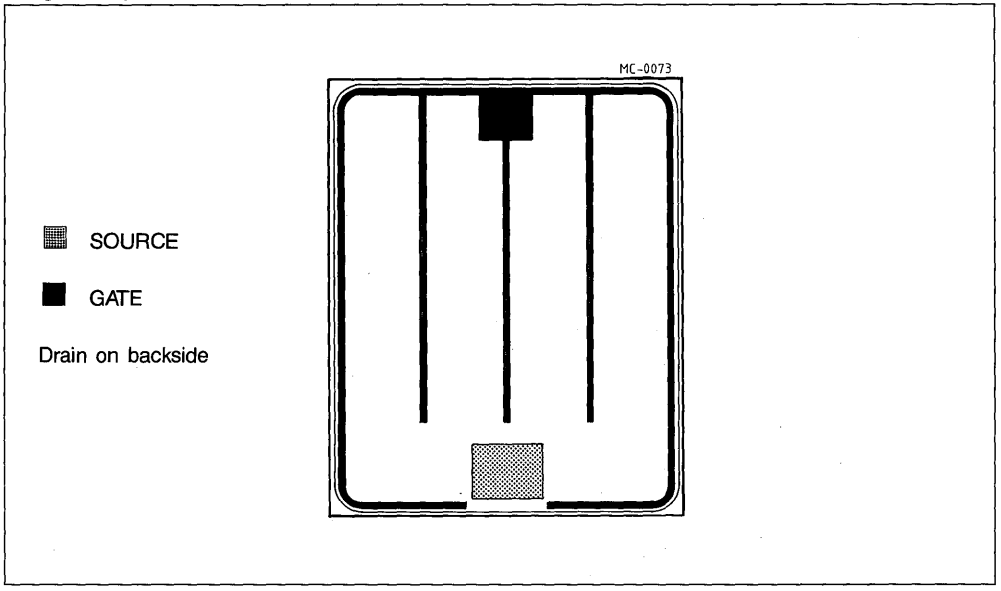
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
400 V	0.55 Ω	10 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 1°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.55	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

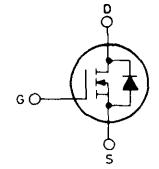
SGS-THOMSON MICROELECTRONICS

MTH40N06 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 221 x 221 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 56 x 43 mils
  Gate: 18 x 18 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 20 mils
  Gate: Al - max 7 mils

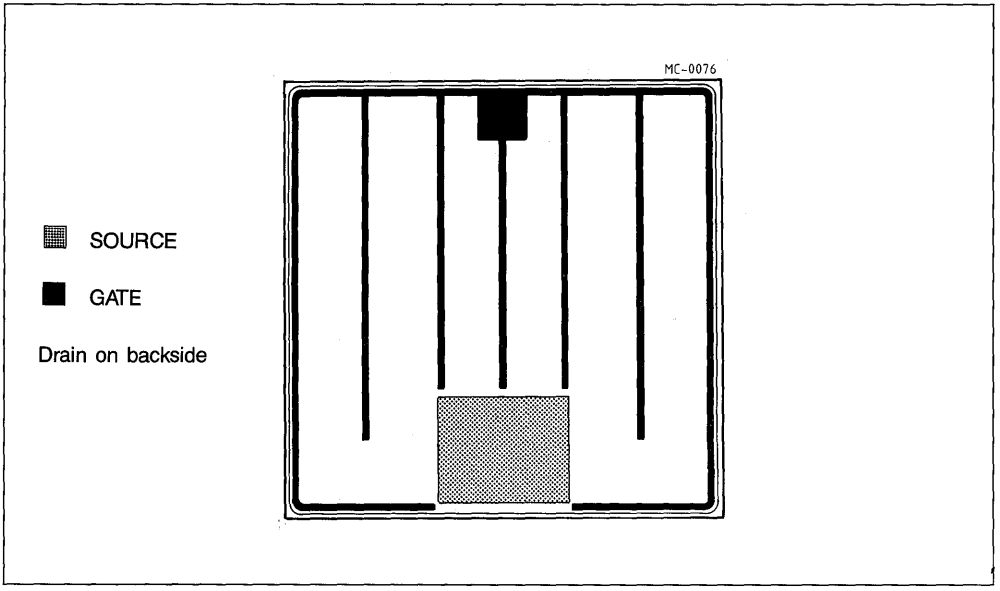
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
60 V	0.028 Ω	40 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 0.83°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 1 mA	2		4.5	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			28	mΩ

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

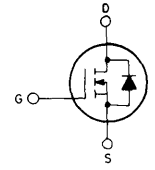
SGS-THOMSON MICROELECTRONICS

SGSP301 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 52 x 53 mils
- METALLIZATION:
  - Top: Al
  - Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  - Source: 4.4 x 6.5 mils
  - Gate: 4.4 x 6.5 mils
- RECOMMENDED WIRE BONDING:
  - Source: Au - max 2 mils
  - Gate: Au - max 2 mils

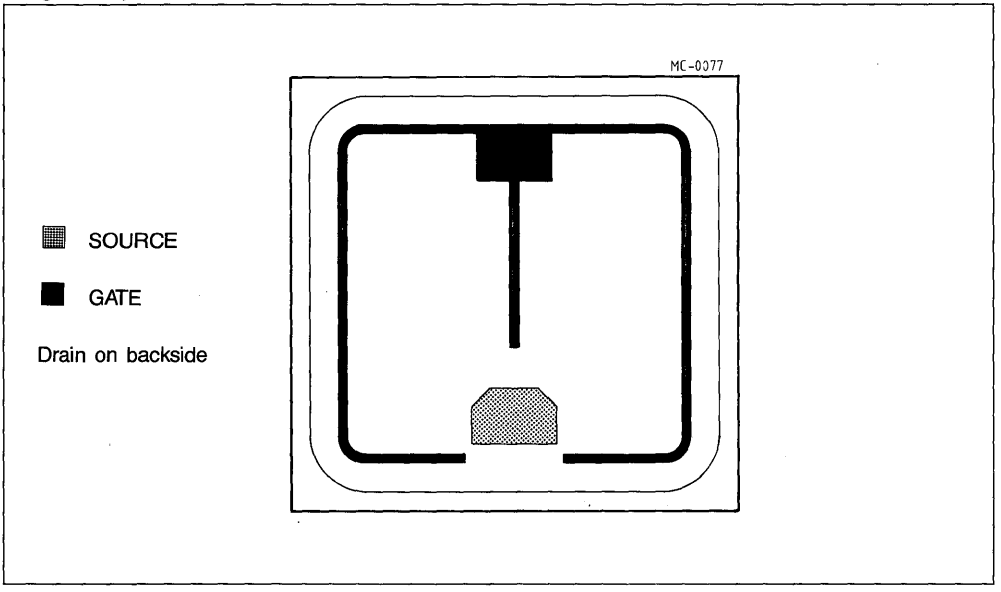
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
100 V	1.4 Ω	2.0 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 6.95°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			±100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			1.4	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

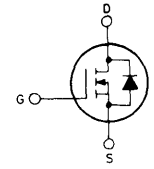
SGS-THOMSON MICROELECTRONICS

SGSP341 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 52 x 53 mils
- METALLIZATION:
  - Top: Al
  - Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  - Source: 10 x 5 mils
  - Gate: 5 x 6 mils
- RECOMMENDED WIRE BONDING:
  - Source: Au - max 2 mils
  - Gate: Au - max 2 mils

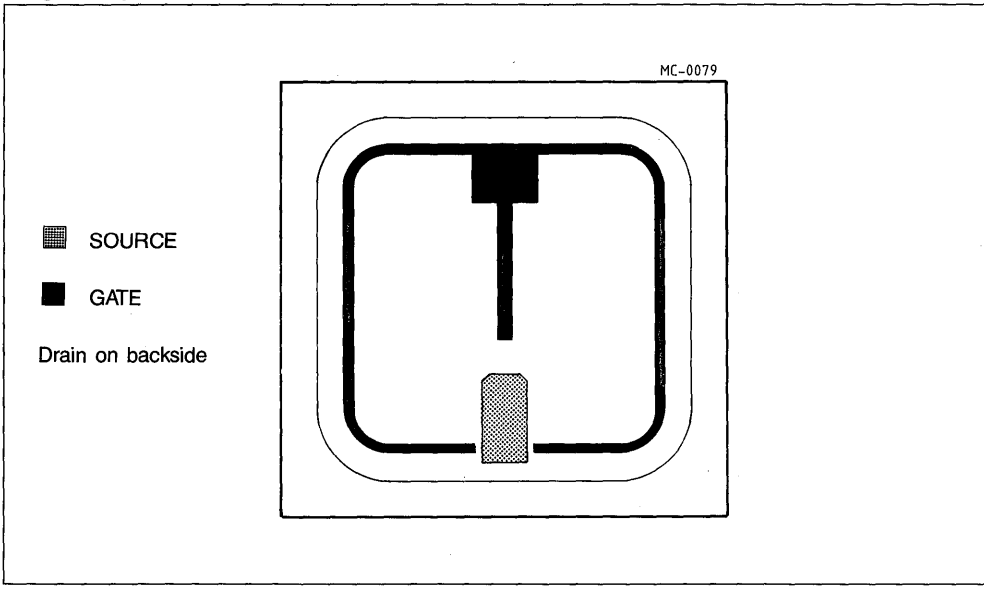
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
400 V	20 Ω	0.6 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 6.8°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	400			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			±100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 0.3 A			20	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

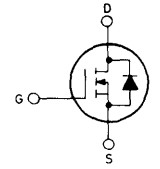
SGS-THOMSON MICROELECTRONICS

SGSP358 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 77 x 77 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 15 x 15 mils
  Gate: 17 x 19 mils
- RECOMMENDED WIRE BONDING:
  Source: Au - max 5 mils
  Gate: Au - max 2 mils

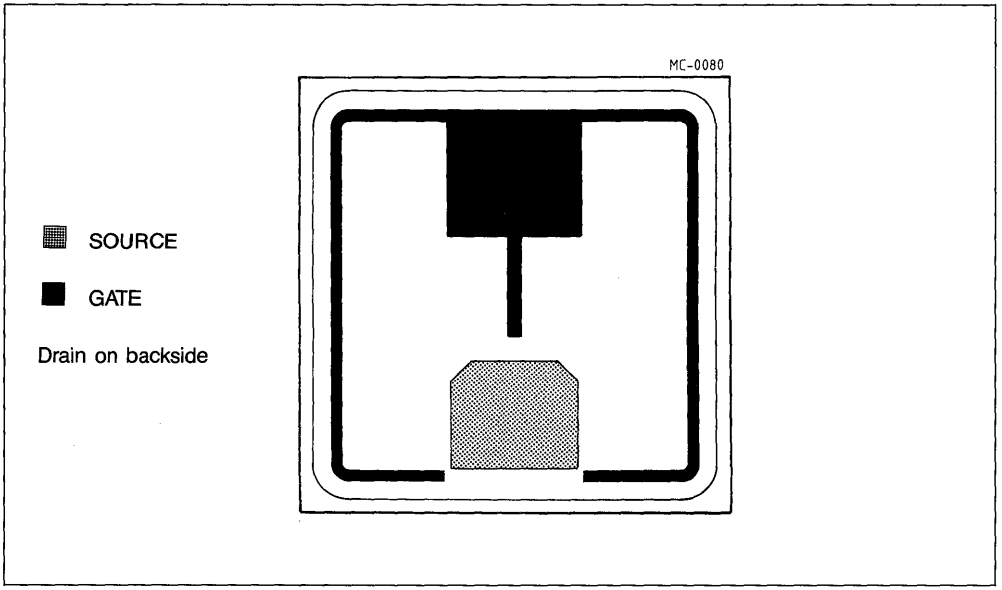
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
50 V	0.3 Ω	7 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 2.5°C/W

GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	50			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.3	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

2 - For detailed device characteristics please refer to the discrete device datasheet

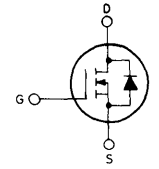
SGS-THOMSON MICROELECTRONICS

SGSP477 CHIP

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR IN DIE FORM

- DIE SIZE: 221 x 221 mils
- METALLIZATION:
  Top: Al
  Back: Au/Cr/Ni/Au
- BACKSIDE THICKNESS: 6100 Å
- DIE THICKNESS: 16 ± 2 mils
- PASSIVATION: P-Vapox
- BONDING PAD SIZE:
  Source: 56 x 43 mils
  Gate: 18 x 18 mils
- RECOMMENDED WIRE BONDING:
  Source: Al - max 20 mils
  Gate: Al - max 7 mils

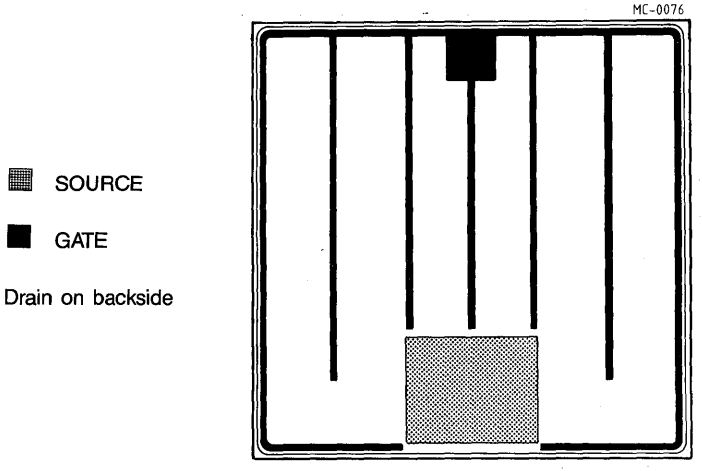
SCHEMATIC DIAGRAM



V_{DSS}	$R_{DS\ (on)}$	I_D*
200 V	0.17 Ω	20 A

N-channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make this POWER MOS ideal for high speed switching applications.

Die geometry



* With $R_{thj\text{-}c}$ max. 0.83°C/W

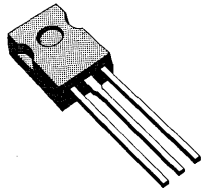
GUARANTEED PROBED ELECTRICAL CHARACTERISTICS (T_j = 25°C, Note 1)

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)\ DSS}$	Drain-source breakdown voltage	I_D = 250 μA V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = Max Rating V_{DS} = Max Rating × 0.8 T_j = 125°C			250 1000	μA μA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V			100	nA
$V_{GS\ (th)}$	Gate threshold voltage	V_{DS} = V_{GS} I_D = 250 μA	2		4	V
$R_{DS\ (on)}$	Static drain-source on resistance	V_{GS} = 10 V I_D = 1 A			0.17	Ω

NOTES: 1 - Due to probe testing limitations dc parameters only are tested. They are measured using pulse techniques: pulse width <300 μs, duty cycle <2%

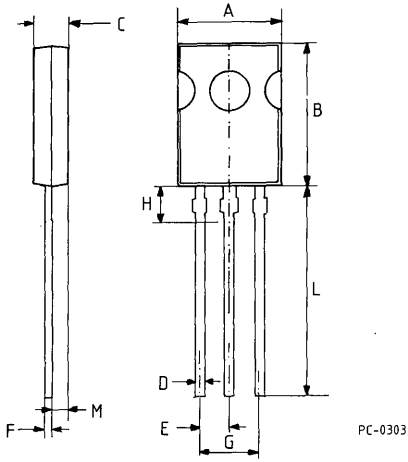
2 - For detailed device characteristics please refer to the discrete device datasheet

PACKAGES

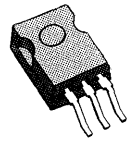


MINIATURE PACKAGE WITH SAME PINOUT AS TO-220 IDEAL FOR MOUNTING WITH CLIPS

MECHANICAL DATA

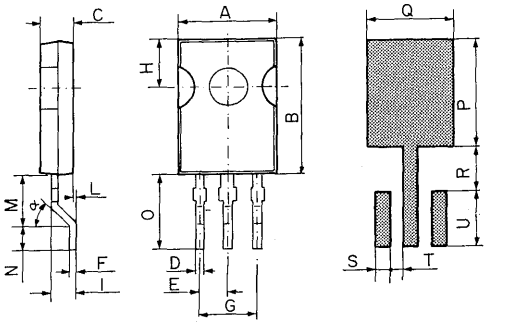


	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	7.4	7.8	0.295	0.307
B	10.5	10.8	0.413	0.425
C	2.4	2.7	0.094	0.106
D	0.7	0.9	0.027	0.035
E	2.2 typ.		0.087 typ.	
F	0.49	0.75	0.019	0.029
G	4.4 typ.		0.173 typ.	
H	2.54 typ.		0.100 typ.	
L	15.7 typ.		0.618 typ.	
M	1.2 typ.		0.047 typ.	



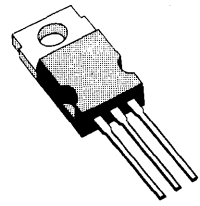
LEAD FORMED
SOT-82 FOR SURFACE
MOUNTING ASSEMBLY

MECHANICAL DATA

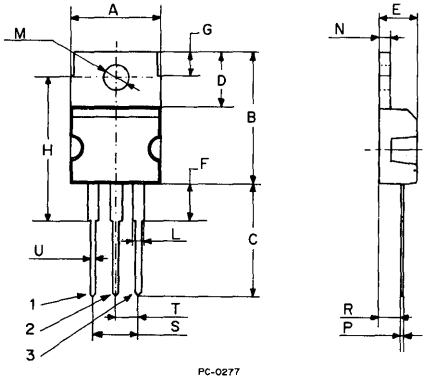


PC-0276

	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	7.4	7.8	0.295	0.307
B	10.5	10.8	0.413	0.425
C	2.4	2.7	0.094	0.106
D	0.7	0.9	0.027	0.035
E	2.2 typ.		0.087 typ.	
F	0.45	0.65	0.017	0.026
G	4.4 typ.		0.173 typ.	
H	3.8 typ.		0.149 typ.	
I	1.8 typ.		0.070 typ.	
L	0.1 typ.		0.004 typ.	
M	3.8	4.2	0.149	0.165
N	2 typ.		0.078 typ.	
O	6 typ.		0.236 typ.	
α	45°		45°	
P	8.5 typ.		0.334 typ.	
Q	6.7 typ.		0.263 typ.	
R	3.5 typ.		0.137 typ.	
S	1.2 typ.		0.047 typ.	
T	1 typ.		0.039 typ.	
U	4.5 typ.		0.177 typ.	

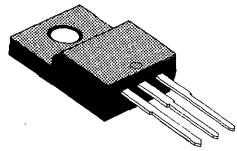


MECHANICAL DATA



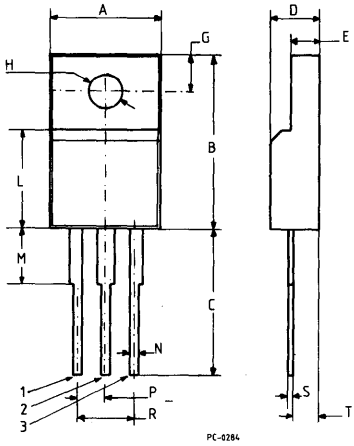
	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	10	10.4	0.393	0.409
B	15.2	15.9	0.598	0.626
C	12.7	13.7	0.500	0.539
D	6.2	6.6	0.244	0.260
E	4.4	4.6	0.173	0.181
F	3.5	5.5	0.137	0.216
G	2.65	2.95	0.104	0.116
H	17.6 typ.		0.692 typ.	
L	1.14	1.7	0.044	0.067
M	3.75	3.85	0.147	0.151
N	1.23	1.32	0.048	0.051
P	0.41	0.64	0.016	0.025
R	2.4	2.72	0.094	0.107
S	4.95	5.15	0.194	0.203
T	2.4	2.7	0.094	0.106
U	0.61	0.94	0.024	0.037

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE



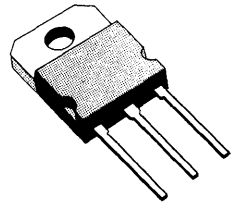
2000V DC FULLY ISOLATED VERSION OF THE TO-220 PACKAGE

MECHANICAL DATA

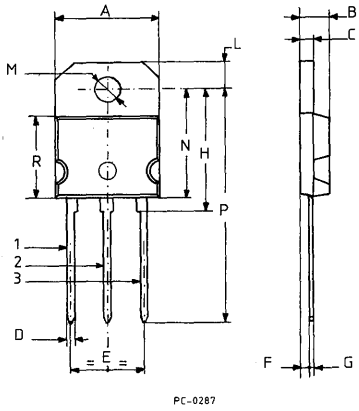


	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	9.8	10.6	0.386	0.417
B	15.7	16.5	0.618	0.649
C	12.7	14.1	0.500	0.555
D	4.18	4.82	0.164	0.189
E	2.3	2.9	0.090	0.114
G	3	3.8	0.118	0.149
H	3	3.2	0.118	0.126
L	9	9.4	0.354	0.370
M	—	6.35	—	0.250
N	0.63	1	0.024	0.039
P	2.29	2.79	0.090	0.109
R	4.83	5.33	0.190	0.209
S	0.33	0.66	0.013	0.026
T	2.28	2.9	0.089	0.114

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE

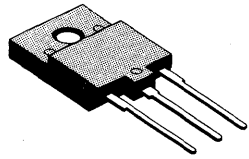


MECHANICAL DATA



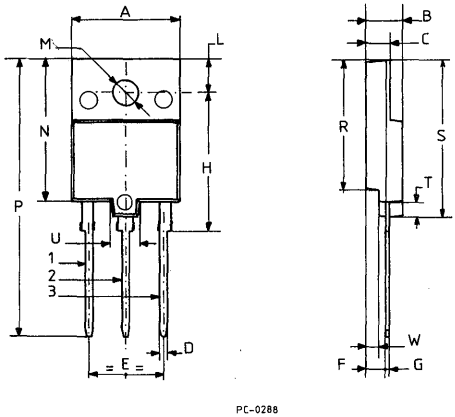
	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	14.7	15.2	0.578	0.598
B	4.7	4.9	0.185	0.193
C	1.9	2.1	0.075	0.082
D	1.1	1.3	0.043	0.051
E	10.8	11.1	0.425	0.437
F	2.5 typ		0.098 typ	
G	0.5	0.78	0.019	0.030
H	18 typ		0.708 typ	
L	3.95	4.15	0.155	0.163
M	4	4.1	0.157	0.161
N	—	16.2	—	0.637
P	31 typ		1.220 typ	
R	—	12.2	—	0.480

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE



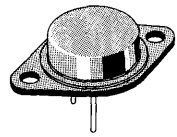
4000V DC FULLY ISOLATED VERSION OF THE TO-218 PACKAGE CONFORMS TO UL AND VDE SAFETY STANDARDS

MECHANICAL DATA

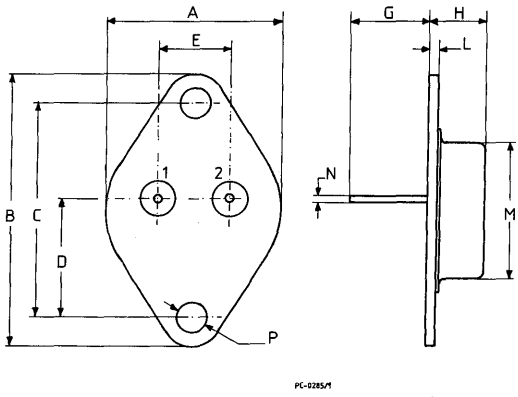


	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	15.8	16.2	0.622	0.637
B	5.35	5.65	0.210	0.222
C	3.3	3.8	0.130	0.149
D	1.05	1.25	0.041	0.049
E	10.8	11.2	0.425	0.441
F	2.9	3.1	0.114	0.122
G	0.45	1	0.017	0.039
H	20.25	20.75	0.797	0.817
L	4.85	5.25	0.190	0.206
M	3.5	3.7	0.137	0.145
N	20.8	21.2	0.818	0.834
P	40.5	42.5	1.594	1.673
R	19.1	19.9	0.752	0.783
S	22.8	23.6	0.897	0.929
T	2.1	2.3	0.082	0.090
U	4.6 typ.		0.181 typ.	
W	1.88	2.08	0.074	0.081

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE

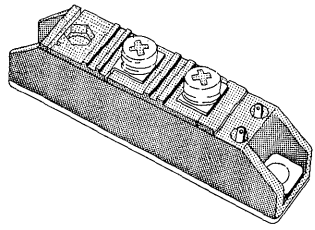


MECHANICAL DATA



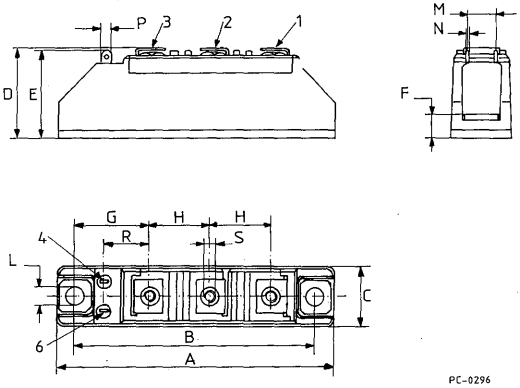
	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	25	26	0.984	1.023
B	38.5	39.3	1.515	1.547
C	30	30.3	1.181	1.193
D	16.5	17.2	0.649	0.677
E	10.7	11.1	0.421	0.437
G	11	13.1	0.433	0.515
H	8.32	8.92	0.327	0.351
L	1.5	1.65	0.059	0.065
M	19	20	0.748	0.787
N	0.97	1.15	0.038	0.045
P	4	4.09	0.157	0.161

pin 1: GATE - pin 2: DRAIN - pin 3: SOURCE

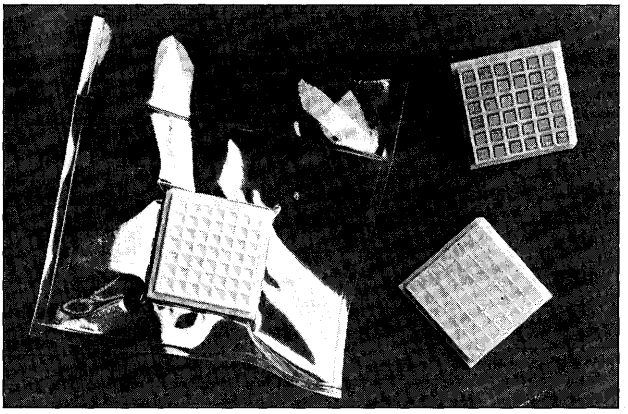


4000V DC
FULLY ISOLATED
INDUSTRY STANDARD MODULE
MEETS UL AND VDE
SAFETY STANDARDS

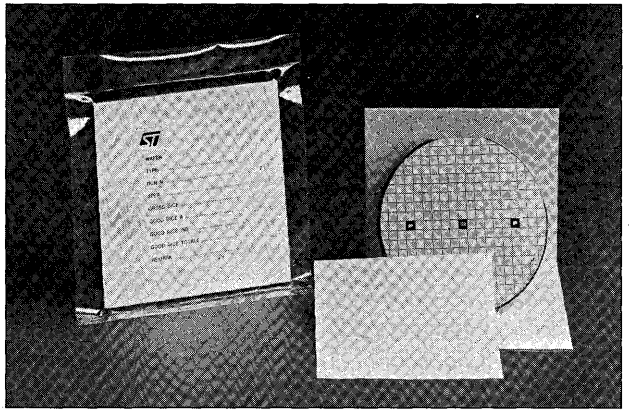
MECHANICAL DATA



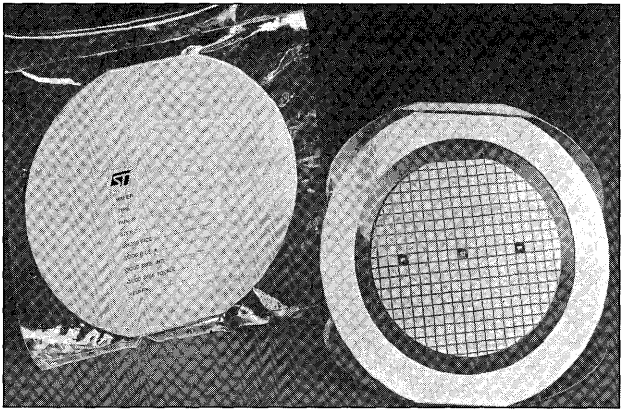
	DIMENSIONS			
	mm		inches	
	min	max	min	max
A	91.5	92.5	3.602	3.641
B	79.75	80.25	3.140	3.160
C	19.5	20.55	0.767	0.809
D	29.00	31.00	1.141	1.220
E	28.8	30	1.134	1.181
F	8.5 typ.		0.334 typ.	
G	24.4 typ.		0.960 typ.	
H	19.5	20.5	0.767	0.807
L	6.2 typ.		0.244 typ.	
M	8.95	11.05	0.352	0.435
N	0.78	0.84	0.030	0.033
P	2.72	2.87	0.107	0.113
R	14	—	0.551	—
S	M5			



Waffle pack (cavity plate)
Suffix D2: dice in cavity plate



Wafer pack
Suffix D1: wafer tested and inked
Suffix D3: wafer tested, inked and scribed at 70%



Circle pack
Suffix D4: wafer tested inked and scribed at 100%

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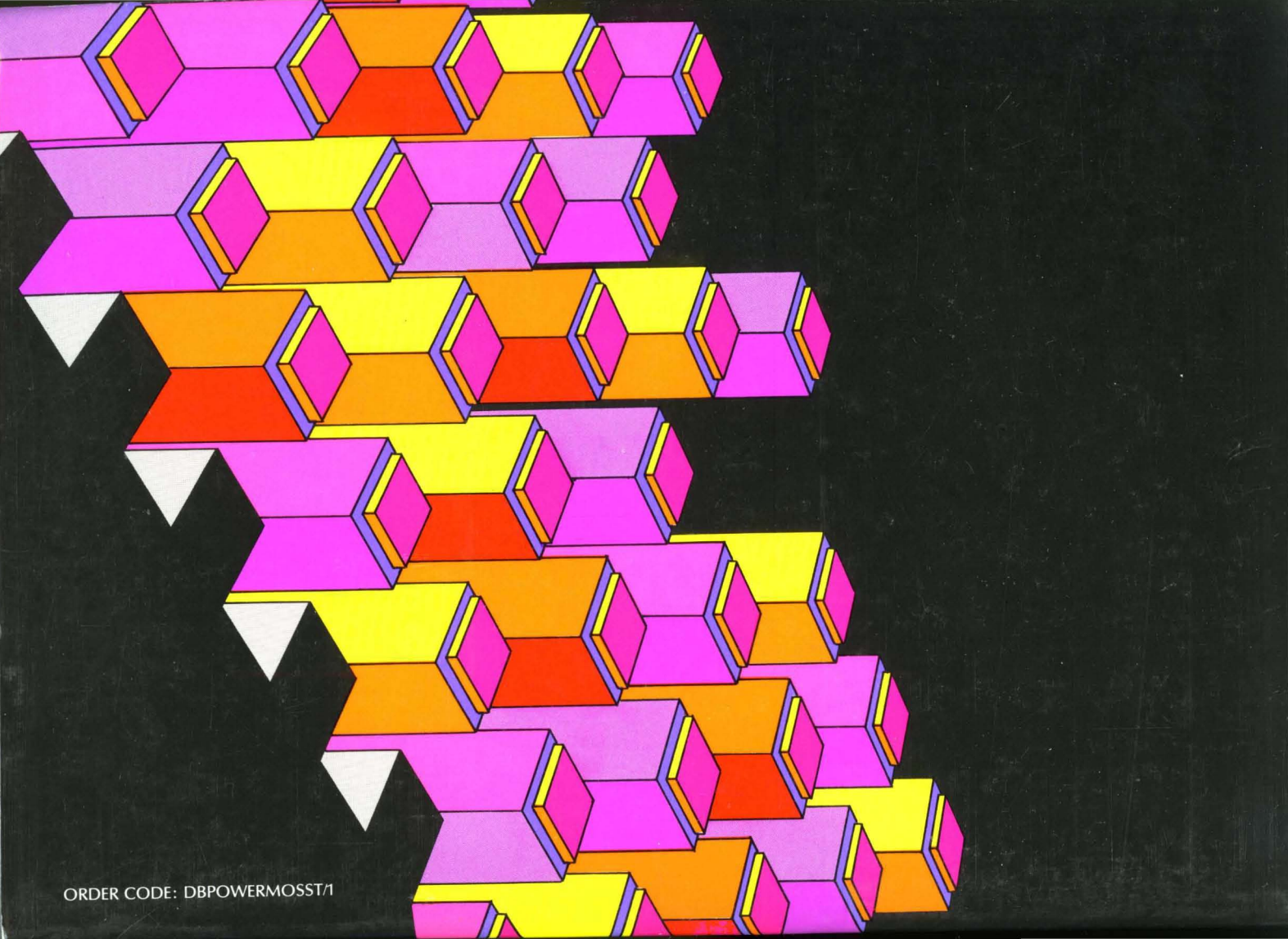

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