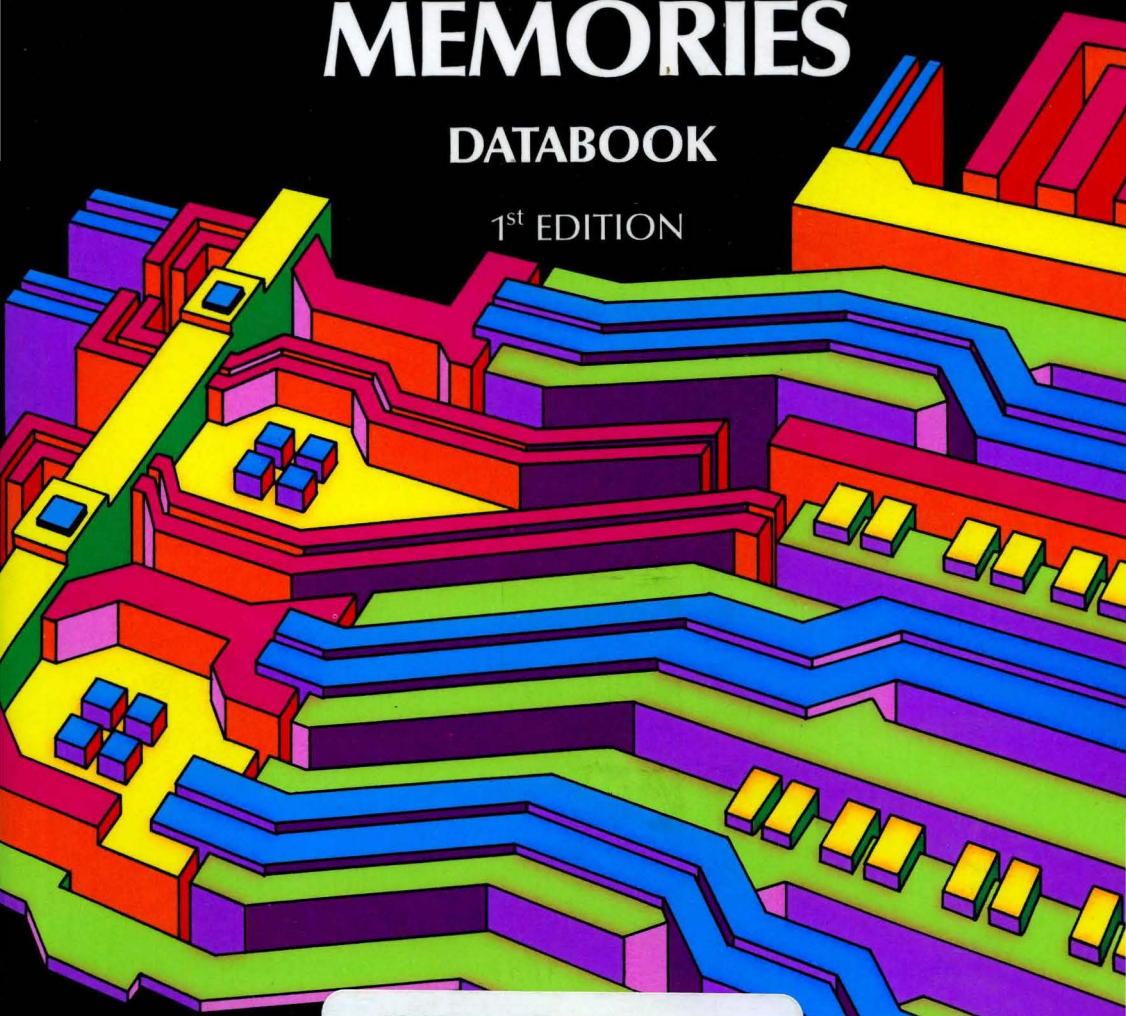
NON-VOLATILE MEMORIES

DATABOOK

1st EDITION



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SGS-THOMSON
MICROELECTRONICS

NON-VOLATILE MEMORIES

DATABOOK

1st EDITION

OCTOBER 1990

USE IN LIFE SUPPORT DEVICES FOR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INTRODUCTION

SGS-THOMSON Microelectronics manufacture an extensive range of non volatile memory products which satisfy the needs of a diverse range of applications.

This databook provides comprehensive, technical information on our four main families of advanced non volatile memory products to aid device selection for a defined use.

MASKED ROMs (Read Only Memories). Having the lowest cost per bit are ideally suited to very large volume applications. SGS-THOMSON's masked ROMs are characterized by their particularly high operating speed (the 1mb device has a typical access time of around 100ns), high noise immunity and low power consumption.

EPROMS (Electrically Programmable Read Only Memories). This family includes UV EPROMS which can be erased by exposure to Ultra Violet light through a quartz window and OTP ROMs (One Time Programmable) which are housed in a low cost plastic package, without a window. SGS-THOMSON's EPROMS are available in densities from 16k up to 4Mb in NMOS and advanced CMOS technologies. Pinout is standard JEDEC although some dedicated pinouts are supported including BIP PROM and ROM. Operating speeds vary between devices, although two main categories exist, high speed and very high speed. High speed devices offer a typical access time of 100ns compared to 45ns for very high speed devices. New developments in the programming algorithm have considerably reduced programming time and improved reliability.

FLASH EPROMs. These devices can be electrically programmed and electrically bulk (FLASH) erased in situ. As a result of this additional functionality they are suited to a wide range of applications where there is a requirement to periodically change the contents of the non volatile memory.

SGS THOMSON has adopted a process approach close to that of EPROMs, thus ensuring a similar evolution pattern of density and reliability characteristics.

Serial Access EEPROMs (Electrically Erasable and Programmable Read Only Memories) . These allow easy in-circuit updates of parameters or data configurations. SGS THOMSON offer a wide range of Serial EEPROM devices with out-standing features including a density range of 256 bits to 8k with both microwire and IC2 bus options and an endurance of 1,000,000 E/W cycles. These devices can be powered from a standard 5V or low 2.5V supply.

SELECTION GUIDE

NMOS EPROM DEVICES SELECTOR GUIDE

CAPACITY	ORGANIZATION	ACCESS TIME	PART NUMBER	PACKAGE	POWER SUPPLY	CONSUMPTION ACT / STANDBY	REMARK
16K Bits	2K x 8	350 ns 450 ns	M2716	FDIP 24	4,75 to 5,25V 4,5 to 5,5V	100 / 25 mA	
24K Bits	4K x 8	200 ns 250 ns 300 ns 450 ns	M2732A	FDIP 24	4,75 to 5,25V 4,5 to 5,5V	125 / 35 mA	
64K Bits	8K x 8	180 ns 200 ns 250 ns 300 ns 450 ns	M2764A	FDIP 28 PDIP 28	4,75 to 5,25V 4,5 to 5,5V	75 / 35 mA	
128K Bits	16K x 8	200 ns 250 ns 300 ns 450 ns	M27128A	FDIP 28 PDIP 28	4,75 to 5,25V 4,5 to 5,5V	85 / 40 mA	
256K Bits	32K x 8	170 ns 200 ns 250 ns 300 ns	M27256	FDIP 28 PDIP 28	4,75 to 5,25V 4,5 to 5,5V	100 / 40 mA	
256K Bits	64K x 8	200 ns 250 ns 300 ns	M27512	FDIP 24	4,75 to 5,25V 4,5 to 5,5V	125 / 40 mA	

FOR AVAILABILITY OF EXACT COMBINATIONS CONTACT THE NEAREST SGS THOMSON SALES OFFICE.

CMOS EPROM DEVICES SELECTOR GUIDE

CAPACITY	ORGANIZATION	ACCESS TIME	PART NUMBER	PACKAGE	POWER SUPPLY	CONSUMPTION ACT* / STANDBY	REMARK
64K Bits	8K x 8	200 ns 250 ns 300 ns	TS27C64A	FDIP 28 PDIP 28 PLCC 32	4,75 to 5,25V 4,5 to 5,5V 4,5 to 5,5V	30 / 0.1 mA	
64K Bits	8K x 8	35 ns 45 ns 55 ns	M27HC641	FDIP 24	4,75 to 5,25V 4,5 to 5,5V	60** / 20 mA	Ultra fast UVEPROM
256K Bits	32K x 8	100 ns 120 ns 150 ns 200 ns 250 ns	M27C256B	FDIP 28 PDIP 28 PLCC 32 PSO 28	4,75 to 5,25V 4,5 to 5,5V	30 / 0.2 mA	
256K Bits	32K x 8	100 ns 120 ns 150 ns 200 ns	M87C257	FDIP 28 PDIP 28 PLCC 32	4,75 to 5,25V 4,5 to 5,5V	30 / 0.2 mA	LATCHED ADDRESS
512K Bits	64K x 8	120 ns 150 ns 200 ns 250 ns	M27C512	FDIP 28 PDIP 28 PLCC 32 SO 28	4,75 to 5,25V 4,5 to 5,5V	30 / 0.2 mA	

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*** At 5MHz ** At 18MHz**

CMOS EPROM DEVICES SELECTOR GUIDE (2)

CAPACITY	ORGANIZATION	ACCESS TIME	PART NUMBER	PACKAGE	POWER SUPPLY	CONSUMPTION ACT* / STANDBY	REMARK
512K Bits	64K x 8	120 ns 150 ns	M27C513	FDIP 28	4,75 to 5,25V 4,5 to 5,5V	30 / 0.2 mA	PAGE ORGANIZATION
512K Bits	64K x 8	120 ns 150 ns	M87C512	FDIP 28	4,75 to 5,25V 4,5 to 5,5V	30/ 0.2 MA	LATCHED ADDRESS
512K Bits	32K x 16	120 ns 150 ns 200 ns	M27C516	FDIP 40 PLCC 44	4,75 to 5,25V 4,5 to 5,5V	30/ 0.2 MA	
1 M Bits	128K x 8	120 ns 150 ns 200 ns 250 ns	M27C1000	FDIP 32 PDIP 40 PLCC 32	4,75 to 5,25V 4,5 to 5,5V	35/ 0.2 MA	"ROM" PINOUT
1 M Bits	128K x 8	120 ns 150 ns 200 ns 250 ns	M27C1001	FDIP 32 PDIP 32 PLCC 32	4,75 to 5,25V 4,5 to 5,5V	35/ 0.2 MA	
1 M Bits	128K x 8	120 ns 150 ns	M27C1011	FDIP 28	4,75 to 5,25V 4,5 to 5,5V	35/ 0.2 MA	PAGE ORGANIZATION

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*** At 5MHz**

CMOS EPROM DEVICES SELECTOR GUIDE (3)

CAPACITY	ORGANIZATION	ACCESS TIME	PART NUMBER	PACKAGE	POWER SUPPLY	CONSUMPTION ACT* / STANDBY	REMARK
1 M Bits	64K x 16	120 ns 150 ns 200 ns 250 ns	M27C1024	FDIP 40 PLCC 44	4,75 to 5,25V 4,5 to 5,5V	35 / 0.2 mA	
2 M Bits	256K x 8	120 ns 150 ns 200 ns 250 ns	M27C2001	FDIP 32	4,75 to 5,25V 4,5 to 5,5V	35 / 0.2 mA	
4 M Bits	512K x 8	100 ns 120 ns 150 ns 200 ns 250 ns	M27C4001	FDIP 32	4,75 to 5,25V 4,5 to 5,5V	50 / 0.1 mA	
4 M Bits	256K x 16	100 ns 120 ns 150 ns 200 ns 250 ns	M27C4002	FDIP 40	4,75 to 5,25V 4,5 to 5,5V	50 / 0.1 mA	

FOR AVAILABILITY OF EXACT COMBINATIONS CONTACT THE NEAREST SGS THOMSON SALES OFFICE.

*** At 5MHz**

MASK ROM DEVICES SELECTOR GUIDE

CAPACITY	ORGANIZATION	ACCESS TIME	PART NUMBER	PACKAGE	POWER SUPPLY	CONSUMPTION ACT / STANDBY	REMARK
512K Bits	64K x 8	100 ns	M23C512	PDIP 28	4,5 to 5,5V	40 / 0.02 mA	
1M Bits	128K x 8	100 ns	M23C1000	PDIP 28	4,5 to 5,5V	40 /0.02 mA	
1M Bits	128K x 8	100 ns	M23C1001	PDIP 32	4,5 to 5,5V	40 /0.02 mA	EPROM PIN OUT
2M Bits	256K x 8	120 ns	M23C2001	PDIP 32	4,5 to 5,5V	50 / 0.02 mA	
4M Bits	512K x 8 256K x 16	120 ns	M23C4000	PDIP 40	4,5 to 5,5V	50 / 0.02 mA	SOFTWARE SELECT.
4M Bits	512K x 8	120 ns	M23C4001	PDIP 32	4,5 to 5,5V	50 / 0.02 mA	

FOR AVAILABILITY OF EXACT COMBINATIONS CONTACT THE NEAREST SGS THOMSON SALES OFFICE.

FLASH EPROM SELECTOR GUIDE

CAPACITY	ORGANIZATION	ACCESS TIME	PART NUMBER	PACKAGE	POWER SUPPLY	CONSUMPTION ACT* / STANDBY	PROG. VOLTAGE	TEMPERATURE RANGE
256K Bits	32K x 8	100 ns 120 ns 150 ns 200 ns	M28F256	PDIP 32 PLCC 32 FDIP 32	4,75V to 5,25V 4,5V to 5,5V 4,5V to 5,5V 4,5V to 5,5V	30 mA / 0.1mA	12V+/-5%	0 to 70 ° -40 to 125 °
1M Bits	128K x 8	100 ns 120 ns 150 ns 200 ns	M28F1001	PDIP 32 PLCC 32 FDIP 32	4,75V to 5,25V 4,5V to 5,5V 4,5V to 5,5V 4,5V to 5,5V	30 mA / 0.1mA	12V+/-5%	0 to 70 ° -40 to 125 °

FOR AVAILABILITY OF EXACT COMBINATIONS CONTACT THE NEAREST SGS THOMSON SALES OFFICE.

*** At 5MHz**

EEPROM SELECTOR GUIDE
I^2C® PRODUCT LINE

CAPACITY	ORGANIZATION	BUS TYPE	PART NUMBER	PACKAGE	POWER SUPPLY	OPERATING TEMP*	REMARK**
2 K Bits	256x8 SERIAL	I^2C	ST24C02AB*	PDIP 8	4,5 to 5,5 V	1,3,6	
		I^2C	ST24C02AM*	PSO 8	4,5 to 5,5 V	1,3,6	
		I^2C	ST25C02AB*	PDIP 8	2,5 to 5,5 V	1,3,6	
		I^2C	ST25C02AM*	PSO 8	2,5 to 5,5 V	1,3,6	
4 K Bits	512x8 SERIAL	I^2C	ST24C04B*	PDIP 8	4,5 to 5,5 V	1,3,6	Write Protection Feature
		I^2C	ST24C04ML*	PSO 14	4,5 to 5,5 V	1,3,6	Write Protection Feature
		I^2C	ST25C04B*	PDIP 8	2,5 to 5,5 V	1,3,6	Write Protection Feature
		I^2C	ST25C04ML*	PSO 14	2,5 to 5,5 V	1,3,6	Write Protection Feature
8 K Bits	1024x8 SERIAL	I^2C	ST24C08B*	PDIP 8	4,5 to 5,5 V	1,3,6	Write Protection Feature

TEMPERATURE SUFFIX

* = 1 = 0 C to 70 C

* = 3 = -40 C to 125 C

* = 6 = -40 C to 85 C

** USER DEFINED SIZE OF MEMORY SECTION PROTECTED AGAINST WRITE.

EEPROM SELECTOR GUIDE

MICROWIRE ® PRODUCT LINE

CAPACITY	ORGANIZATION	BUS TYPE	PART NUMBER	PACKAGE	POWER SUPPLY	OPERATING TEMP*	REMARK **
256 Bits	16x16 SERIAL	MICROWIRE	ST93C06B*	PDIP 8	4,5V to 5V	1,3,6	
		MICROWIRE	ST93C06M*	PSO 8	4,5V to 5V	1,3,6	
1 K Bits	64x16 SERIAL or 128x8 SERIAL	MICROWIRE	ST93C46AB*	PDIP 8	4,5V to 5V	1,3,6	
		MICROWIRE	ST93C46AM*	PSO 8	4,5V to 5V	1,3,6	
1 K Bits	64x16 SERIAL	MICROWIRE	ST93CS46AB*	PDIP 8	4,5V to 5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS46M*	PSO 8	4,5V to 5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS47B*	PDIP 8	2,5V to 5,5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS47M*	PSO 8	2,5V to 5,5V	1,3,6	Write Protection Feature
2 K Bits	128x16 SERIAL	MICROWIRE	ST93CS56B*	PDIP 8	4,5V to 5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS56M*	PSO 8	4,5V to 5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS56ML*	PSO 14	4,5V to 5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS57B*	PDIP 8	2,5V to 5,5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS57M*	PSO 8	2,5V to 5,5V	1,3,6	Write Protection Feature
		MICROWIRE	ST93CS57ML*	PSO 14	2,5V to 5,5V	1,3,6	Write Protection Feature

TEMPERATURE SUFFIX

* = 1 = 0 C to 70 C

* = 3 = -40 C to 125 C

* = 6 = -40 C to 85 C

** USER DEFINED SIZE OF MEMORY SECTION PROTECTED AGAINST WRITE.

EPROM DEVICES

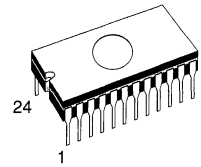
NMOS EPROM

SGS-THOMSON MICROELECTRONICS

ET2716
M2716

16K (2K x 8) NMOS UV EPROM

- 2048 x 8 ORGANIZATION.
- 525 MW MAX ACTIVE POWER, 132 MW MAX STANDBY POWER.
- ACCESS TIME M/ET2716-1, 350 ns ; M/ET2716, 450 ns.
- SINGLE 5V SUPPLY.
- STATIC-NO CLOCKS REQUIRED.
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING BOTH READ AND PROGRAM MODES.
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY.
- EXTENDED TEMPERATURE RANGE (F6).
- 25V PROGRAMMING VOLTAGE.



FDIP-24

(Ordering information at the end of the datasheet)

DESCRIPTION

The M/ET2716 is a high speed 16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M/ET2716 is housed in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN FUNCTIONS

A0-A10	ADDRESS INPUT
O0-O7 (Q0-Q7)	DATA OUTPUTS
$\overline{CE}$/PGM ($\overline{E}$/P)	CHIP ENABLE/PROGRAM
$\overline{OE}$ (G)	OUTPUT ENABLE
V_{PP}	READ 5V, PROGRAM 25V
V_{CC}	POWER (5V)
V_{SS}	GROUND

NOTE : Symbols in parentheses are proposed JEDEC standard.

Figure 1 : Pin Connection

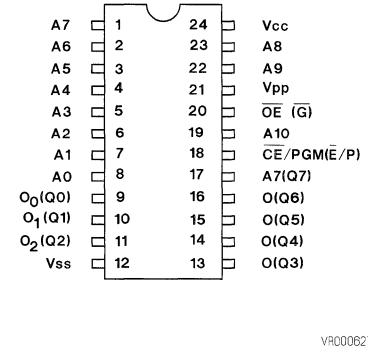
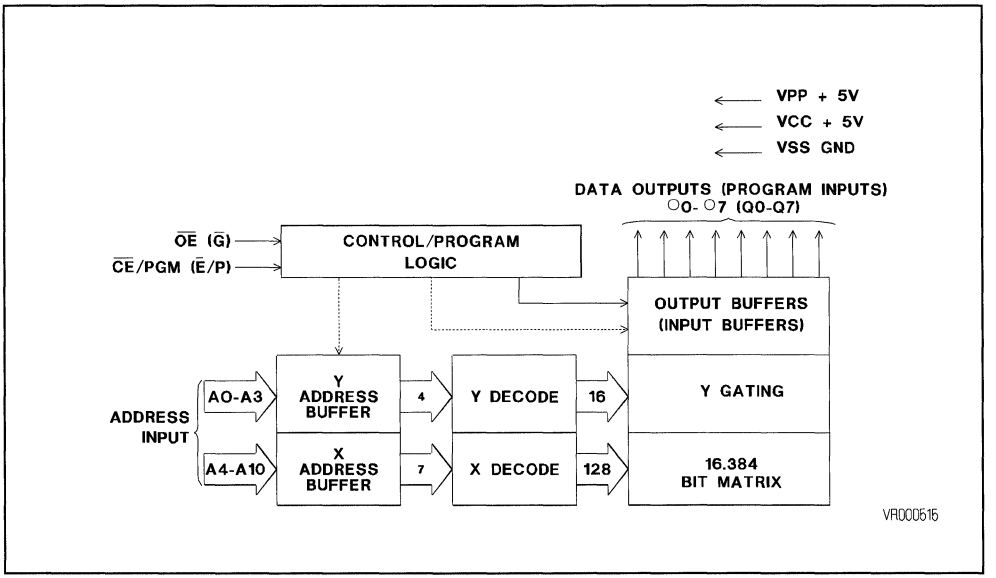


Figure 2 : Block Diagram



PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER				
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	V_{CC} 24	OUTPUTS 9-11, 13-17
READ	V_{IL}	V_{IL}	5	5	D_{OUT}
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}

* Symbols in parentheses are proposed JEDEC standard.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{AMB}	Temperature under bias (Extended temperature range)	-10 to +80 (-50 to +95)	°C °C
T_{STG}	Storage temperature	-65 to +125	°C
V_{PP}	V_{PP} Supply voltage with respect to V_{SS}	26.5V to -0.3	V
V_{IN}	All input or output voltages with respect to V_{SS}	6V to -0.3	V
P_D	Power dissipation	1.5	W
	Lead temperature (soldering 10 seconds)	+300	°C

NOTE : "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS (1)

T_A = 0°C to + 70°C (6), V_{CC} = 5V ± 5% for M/ET2716, V_{CC} = 5V ± 10% for M/ET2716-1 V_{PP} = V_{CC} (3), V_{SS} = 0V, (Unless otherwise specified).

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current	V_{IN} = 5.25V or V_{IN} = V_{IL}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.25V, $\overline{CE}$/PGM = 5V			10	µA
I_{PP1}	V_{PP} Supply Curent	V_{PP} = 5.25V			5	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{CE}$/PGM = V_{IH}, $\overline{OE}$ = V_{IL}		10	25	mA
I_{CC2}	V_{CC} Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = V_{IL}		57	100	mA
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OH}	Output high voltage	I_{OH} = -400 µA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA			0.45	V

AC CHARACTERISTICS

T_A = 0°C to + 70°C (6), V_{CC} = 5V ± 5% for M/ET2716, V_{CC} = 5V ± 10% for M/ET2716-1 V_{PP} = V_{CC} (3), V_{SS} = 0V, (Unless otherwise specified).

Symbols		Parameter	Test Condition	M/ET2716-1		M/ET2716		Unit
Stand	Jedec			Min	Max	Min	Max	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = V_{IL}		350		450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		350		450	ns
t_{OE}	TGLQV	$\overline{OE}$ to Output Delay	$\overline{CE}$/PGM = V_{IL}		120		120	ns
t_{DF} (5)	TGHQZ	$\overline{OE}$ or $\overline{CE}$ High to Output H_{I-Z}	$\overline{CE}$/PGM = V_{IL}	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = V_{IL}	0		0		ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output H_{I-Z}	$\overline{OE}$ = V_{IL}	0	100	0	100	ns

CAPACITANCE (4)

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Typical conditions are for operation at : T_A = 25°C, V_{CC} = 5V, V_{PP} = V_{CC} and V_{SS} = 0V.
3. V_{PP} may be connected to V_{CC} except during program.
4. Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1MHz.
5. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first. This parameter is only sampled and not 100% tested.
6. T_A = -40°C to +85°C for the F6 version (extended range).

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

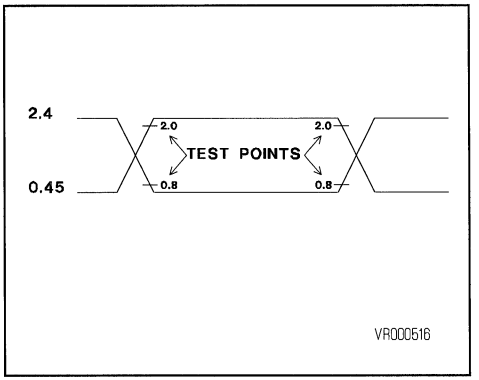


Figure 4 : AC Testing Load Circuit

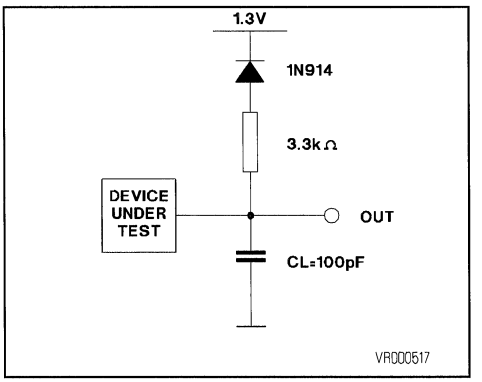
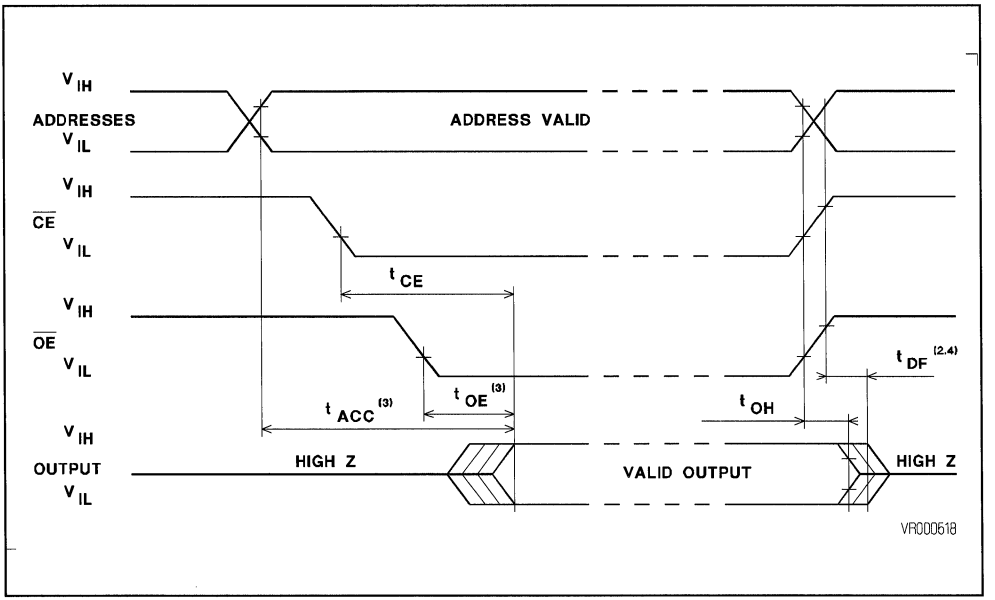


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The M/ET2716 has 3 modes of operation in the normal system environment. These are shown in Table 1.

READ MODE

The M/ET2716 read operation requires that $\overline{OE}$ = V_{IL}, $\overline{CE}$/PGM = V_{IL} and that addresses A0-A10 have been stabilized. Valid data will appear on the output pins after time t_{ACC}, t_{OE} or t_{CE} (see Switching Time Waveforms) depending on which is limiting.

DESELECT MODE

The M/ET2716 is deselected by making $\overline{OE}$ = V_{IH}. This mode is independent of $\overline{CE}$/PGM and the condition of the adresses. The outputs are Hi-Z when $\overline{OE}$ = V_{IH}. This allows OR-tying 2 or more M/ET2716's for memory expansion.

STANDBY MODE (Power Down)

The M/ET2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = V_{IH}. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. V_{CC} and V_{PP} must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The M/ET2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

PROGRAM MODE

The M/ET2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is :

Table 1 : Operating Modes (V_{CC} = V_{PP} = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9-11, 13-17
READ	V_{IL}	V_{IL}	D_{OUT}
DESELECT	Don't Care	V_{IH}	Hi-Z
STANDBY	V_{IH}	Don't Care	Hi-Z

With V_{PP} = 25V, V_{CC} = 5V, $\overline{OE}$ = V_{IH} and $\overline{CE}$/PGM = V_{IL}, an address is selected and the desired data word is applied to the output pins (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45 ms and 55 ms. Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. M/ET2716's may be programmed in parallel with the same in this mode.

PROGRAM VERIFY MODE

The programming of the M/ET2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with V_{PP} = 25V (or 5V) in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several M/ET2716's simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the M/ET2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = V_{IH} will put its outputs in the Hi-Z state.

Table 2 : Programming Modes (V_{CC} = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	OUTPUTS 9-11, 13-17
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	25 (5)	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	25	Hi-Z

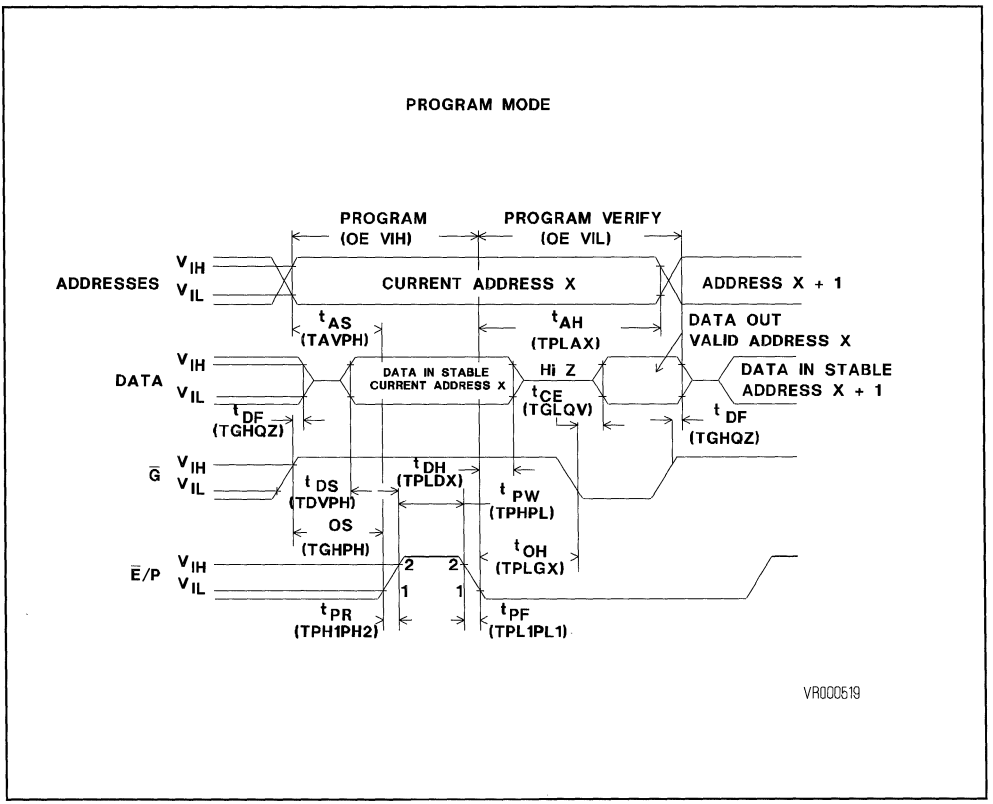
ERASING

The M/ET2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M/ET2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 A yielding a total integrated dosage of 15 watt-seconds/cm^2 power rating is used. The M/ET2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age, it is therefore important to periodically check that UV system is in good order. This will ensure that the EPROM programs are being completely erased. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Figure 6 : Timing Diagram



NOTE : Symbols in parentheses are proposed JEDEC standard.

PROGRAMMING OPERATION

DC AND OPERATING CHARACTERISTICS

(T_A = 25°C ± 5°C, V_{CC} = 5V ± 5V, V_{PP} = 25V ± 1V) Notes 1 and 2

Symbol	Parameter	Values			Unit
		Min	Typ	Max	
I_{LI} (3)	Input Leakage Current			10	µA
V_{IL}	Input Low Level	-0.1		0.8	V
V_{IH}	Input High Level	2.0		V_{CC}+1	V
I_{CC}	V_{CC} Power Supply Current			100	mA
I_{PP1}	V_{PP} Supply Current			5	mA
I_{PP2} (5)	V_{PP} Supply Current During Programming Pulse			30	mA

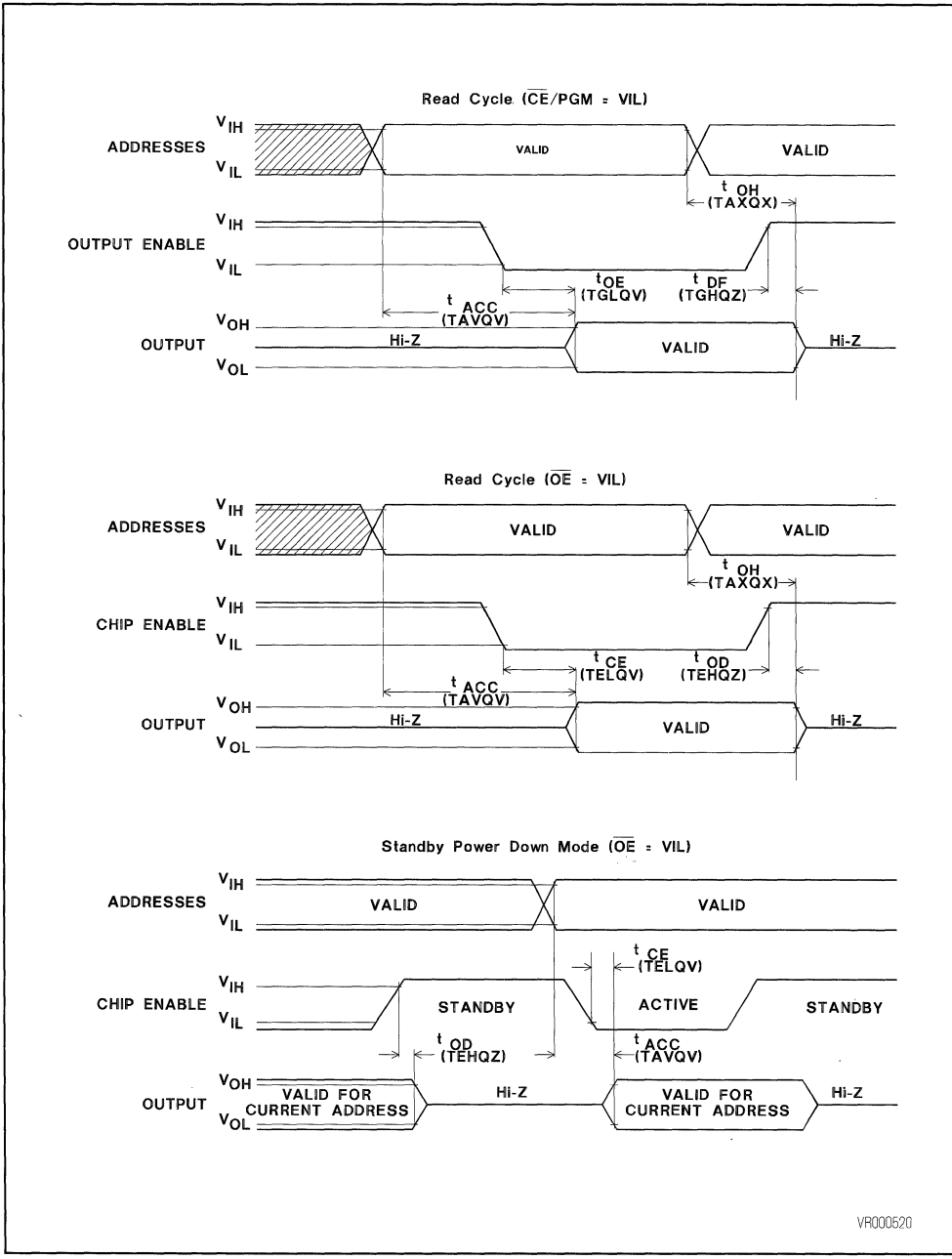
AC CHARACTERISTICS

(T_A = 25°C ± 5°C, V_{CC} = 5V ± 5 %, V_{PP} = 25V ± 1V) Notes 1, 2 and 6

Symbols		Parameter	Values			Unit
Stand	Jedec		Min	Typ	Max	
t_{AS}	TAVPH	Address Setup Time	2			µs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2			µs
t_{DS}	TDVPH	Data Setup Time	2			µs
t_{AH}	TPLAX	Address Hold Time	2			µs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			µs
t_{DH}	TPLDX	Data Hold Time	2			µs
t_{DF} (4)	TGHQZ	Chip disable to Output Float Delay	0		100	ns
t_{OE} (4)	TGLQV	Output Enable to Ouput Delay			120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

NOTES : 1. V_{CC} must be applied at the same time of before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with power applied.
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching + 25V.
3. $0.45V \leq V_{IN} < 5.25V$.
4. $\overline{CE}/PGM = V_{IL}$, $V_{PP} = V_{CC}$.
5. V_{PP} = 26V.
6. Transition times ≤ 20 ns unless otherwise noted.

Figure 7 : Switching Time Waveforms



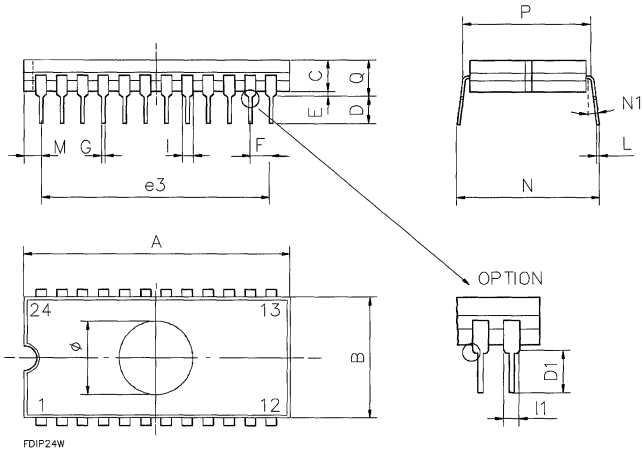
NOTE : Symbols in parentheses are proposed JEDEC standard.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ET2716Q	450 ns	5 V ± 5%	0 to +70°C	DIP-24
ET2716Q-1	350 ns	5 V ± 10%	0 to +70°C	DIP-24
M2716F1	450 ns	5 V ± 5%	0 to +70°C	DIP-24
M2716-1F1	350 ns	5 V ± 10%	0 to +70°C	DIP-24
M2716F6	450 ns	5 V ± 5%	-40 to +85°C	DIP-24
M2716-1F6	350 ns	5 V ± 10%	-40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

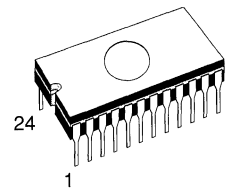
Figure 8 : 24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.00			1.259
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1	3.40			0.134		
E	0.50		1.78	0.020		0.070
e3		27.94			1.10	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

32K (4K x 8) NMOS UV EPROM

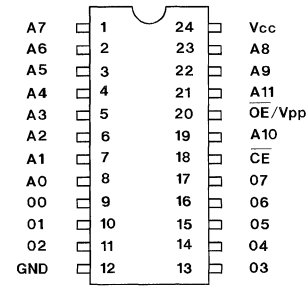
- FAST ACCESS TIME : 200 ns.
- 0 TO + 70 °C STANDARD TEMPERATURE RANGE.
- – 40 TO + 85 °C EXTENDED TEMPERATURE RANGE.
- SINGLE + 5V POWER SUPPLY.
- LOW STANDBY CURRENT (35mA MAX).
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING READ AND PROGRAM.
- COMPLETELY STATIC.
- 21V PROGRAMMING VOLTAGE.



FDIP-24

(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection



VR000864

DESCRIPTION

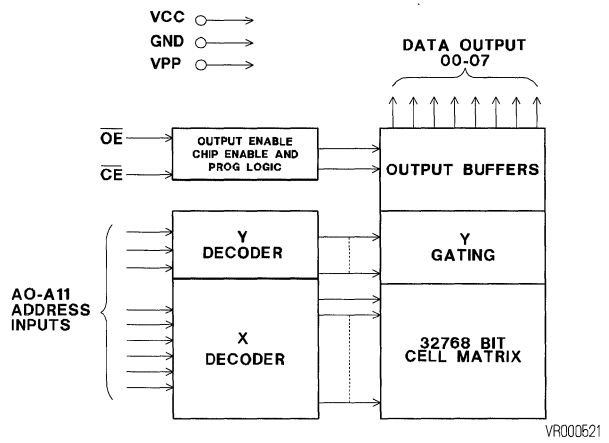
The M2732A is a 32,768-bits ultraviolet erasable and electrically programmable read-only memory (EPROM). It is organized as 4,096 words by 8 bits. The M2732A with its single + 5V power supply and with an access time of 200 ns, is ideal for use with the high performance + 5V microprocessors such as the Z8*, Z80* and Z8000*.

The M2732A is available in a 24-lead dual in-line ceramic package glass lens (Frit-Seal).

PIN FUNCTIONS

A0-A11	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Values	Units
V_I	All input or Output voltages with respect to ground	+6 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+22 to -0.6	V
T_{AMB}	Ambient temperature under bias F1/-2F1/-3F1/-4F1 F6/4F6	-10 to +80 -50 to +95	°C °C
T_{STG}	Storage temperature range	-65 to +125	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS			
	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+ 5	D_{OUT}
STANDBY	V_{IH}	Dont't Care	+ 5	HIGH Z
PROGRAM	V_{IL}	V_{PP}	+ 5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+ 5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	+ 5	HIGH Z

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0 to 70°C	-40 to 85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**2F1, F1, 3F1, 4F1**	**20F1, 25F1, 30F1, 45F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ (3)	Max	
I_{LI}	Input Leakage Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{CC1} (2)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL}			35	mA
I_{CC2} (3)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		70	125	mA
V_{IL}	Input low voltage		-0.1		+0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	2732A-2 2732A-20		2732A 2732A-25		2732A-3 2732A-30		2732A-4 2732A-45		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output delay	$\overline{OE}$=V_{IL}		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		100		100		150		150	ns
t_{DF} (4)	$\overline{OE}$ High to Output float	$\overline{CE}$=V_{IL}	0	60	0	60	0	130	0	130	ns
t_{OH}	Output hold from address, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE(4)

(T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN1}	Input Capacitance except $\overline{OE}$/V_{PP}	V_{IN} = 0V		4	6	pF
C_{IN2}	$\overline{OE}$/V_{PP} Input Capacitance	V_{IN} = 0V			20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

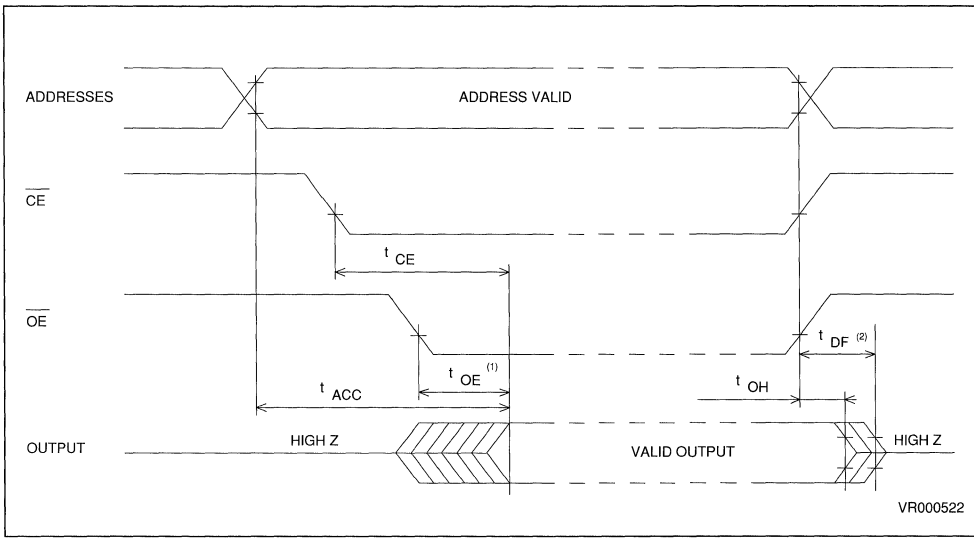
NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100 % tested.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Reference Levels :	
Input Pulse Levels	:	0.45 to 2.4V	Inputs : 0.8 and 2V - Outputs : 0.8 and 2V	

Figure 3 : AC Waveforms



NOTES : 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2732A has a standby mode which reduces the active power current by 70 %, from 125 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because M2732A's are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}[2] = 5 V ± 5 %, V_{PP}[2, 3] = 21 V± 0.5 V)

DC AND OPERATING CHARACTERISTICS

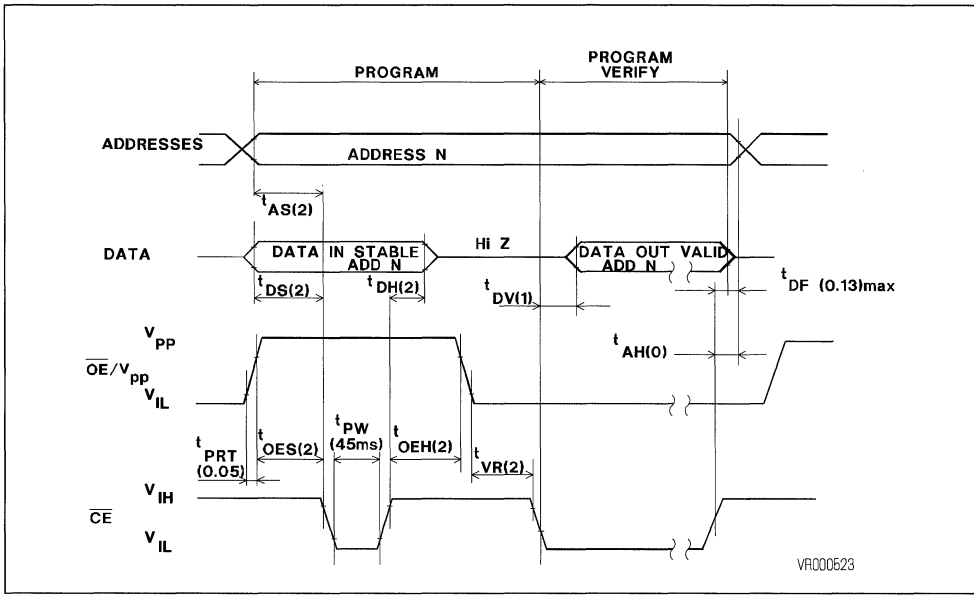
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}			10	µA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Verify)			70	125	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{PP}			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Chip Enable to Output Float Delay		0		130	ns
t_{DV}	Data valid from $\overline{CE}$	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}			1	µs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{CE}$ Pulse rise time During Programming		50			ns
t_{VR}	V_{PP} recovery time		2			µs

NOTES :
1. Product is guaranteed only if programmed within described specifications.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}. The M2732A must not be inserted into or removed from a board with V_{PP} at 21 ± 0.5V. Otherwise damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +22V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.

Figure 4 : Programming Waveforms



NOTES : 1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.

PROGRAMMING

Caution : Exceeding 22V on pin (V_{PP}) will damage the M2732A.

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. A 0.1µF capacitor must be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. Any location can be programmed at any time - either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

PROGRAM INHIBIT

Programming of multiple 2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel 2732As may be common. A TTL level program pulse applied to a 2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that 2732A. A high level $\overline{CE}$ input inhibits the other 2732As from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is curried out with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

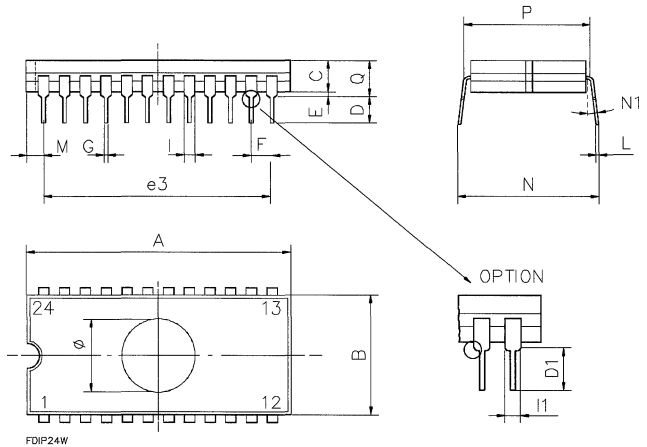
The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2732A-2F1	200 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732AF1	250 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732A-3F1	300 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732A-4F1	450 ns	5 V ± 5%	0 to + 70°C	FDIP24-W
M2732A-20F1	200 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732A-25F1	250 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732A-30F1	300 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732A-45F1	450 ns	5 V ± 10%	0 to + 70°C	FDIP24-W
M2732AF6	250 ns	5 V ± 5%	-40 to + 8 5°C	FDIP24-W
M2732A-4F1	450 ns	5 V ± 5 %	-40 to + 85°C	FDIP24-W

PACKAGE MECHANICAL DATA

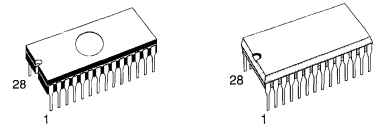
Figure 5 : 24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.00			1.259
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1	3.40			0.134		
E	0.50		1.78	0.020		0.070
e3		27.94			1.10	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

64K (8K x 8) NMOS UV EPROM - OTP ROM

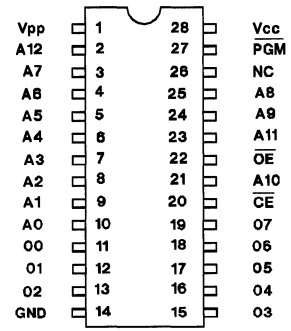
- FAST ACCESS TIME : 180 ns.
- 0 TO + 70 °C STANDARD TEMPERATURE RANGE.
- – 40 to + 85 °C EXTENDED TEMPERATURE RANGE.
- SINGLE + 5V POWER SUPPLY.
- ± 10 % V_{CC} TOLERANCE AVAILABLE.
- LOW STANDBY CURRENT (35mA max).
- TTL COMPATIBLE DURING READ AND PROGRAM.
- FAST PROGRAMMING ALGORITHM.
- ELECTRONIC SIGNATURE.



FDIP-28 PDIP-28

(Ordering information at the end of the datasheet)

Figure 1 : Pin connection



DESCRIPTION

The M2764A is a 65,536-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 8,192 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

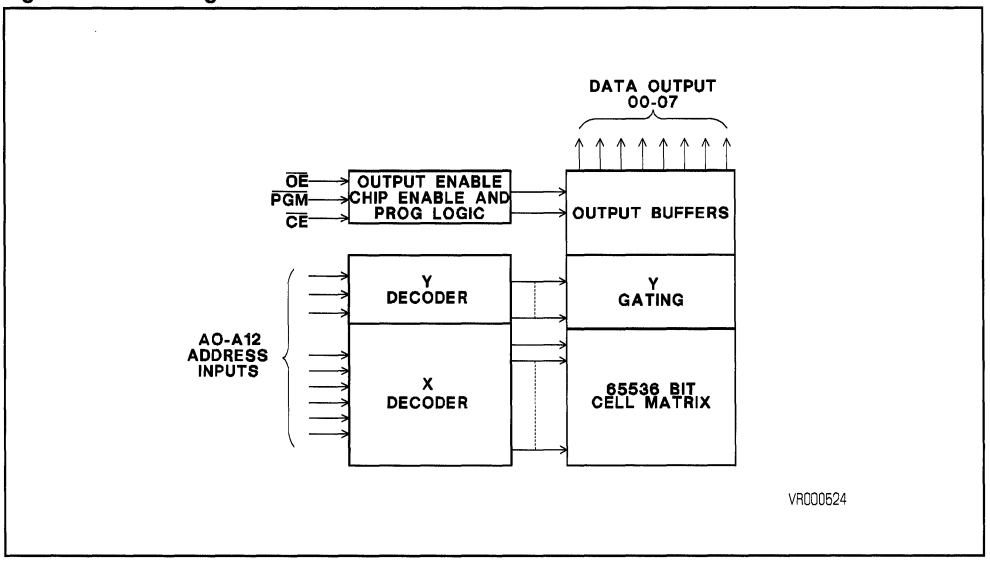
It is housed in a 28 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution, this product is also offered in a plastic DIL package).

PIN NAMES

A0-A12	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECTION
O0-O7	DATA INPUT/OUTPUT

Figure 2 : Block Diagram



Symbol	Parameters	Values	Units
V_I	All Input or Output voltages with respect to ground	+6.5 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to 0.6	V
T_{AMB}	Ambient temperature under bias /F1 /F6	-10 to +80 -50 to +95	°C °C
T_{STG}	Storage temperature range	-65 to +125	°C
VA9	Voltage on pin 24 with respect to ground	+13.5 to -0.6	V

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MODE	PINS						
	$\overline{CE}$	OE	A9	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	VIH	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE : X can be V_{IH} or V_{IL} . V_H = 12V ± 0.5V

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0°C to +70°C	-40°C to +85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**1F1, 2F1, F1** **3F1, 4F1**	**18F1, 20F1, 25F1** **30F1, 45F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ (3)	Max	
I_{LI}	Input Load Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{PP1}(2)	V_{PP} Current Read	V_{PP} = 5.5V			5	mA
I_{CC1}(2)	VCC Current Standby	$\overline{CE}$ = V_{IH}			35	mA
I_{CC2}(2)	VCC Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			75	mA
V_{IL}	Input Low Voltage		-0.1		+0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	IOL = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4			V
V_{PP}(2)	VPP Read Voltage	V_{CC} = 5V ± 0.25V	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} ± 5%	2764A-1		2764A-2		2764A		2764A-3		2764A-4		Unit
		V_{CC} ± 10%	2764A-18		2764A-20		2764A-25		2764A-30		2764A-45		
		Test Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		180		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		180		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		65		75		100		120		150	ns
t_{DF}(4)	$\overline{OE}$ High to output Float	$\overline{CE}$ = V_{IL}		55	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		0		0		ns

CAPACITANCE(5)

(T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ (2)	Max	Unit
C_{IN}	Input Capacitance	VIN = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).
5. This parameter is only sampled and is not 100% tested.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

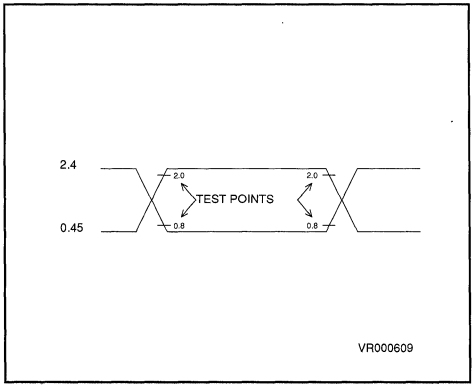


Figure 4 : AC Testing Load Circuit

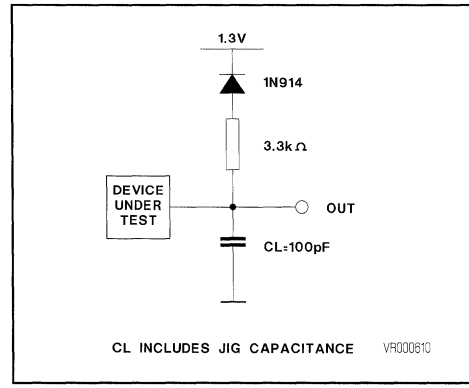
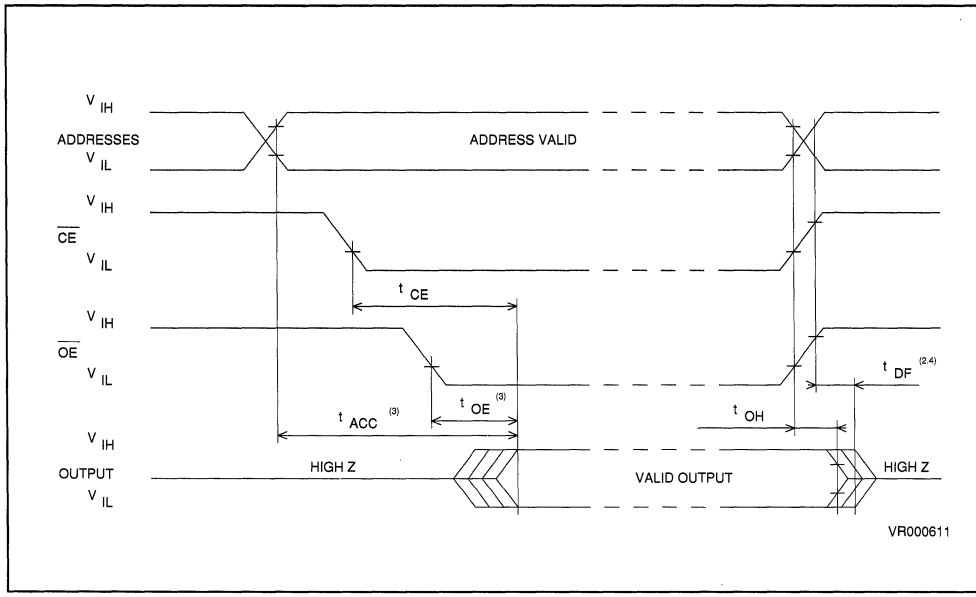


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the M2764A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M2764A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2764A has a standby mode which reduces the maximum active power current from 75 mA to 35 mA. The M2764A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND.

This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 13V on pin 1 (V_{PP}) will damage the M2764A.

When delivered (and after each erasure for UV EPROM), all bits of the M2764A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2764A is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied, 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M2764A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M2764A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram.

DEVICE OPERATION (Continued)

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M2764A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5V.

PROGRAM INHIBIT

Programming of multiple M2764A in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M2764A may be common. A TTL low pulse applied to a M2764A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M2764A. A high level $\overline{CE}$ input inhibits the other M2764A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5 °C ambient temperature range that is required when programming the M2764A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M2764A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M2764A, these two identifier bytes are given below.

ERASURE OPERATION (Applies for UV EPROM)

The erasure characteristic of the M2764A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M2764A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2764A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2764A window to prevent unintentional erasure. The recommended erasure procedure for the M2764A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2764A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	1	0	0	0	08

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[1] = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTICS

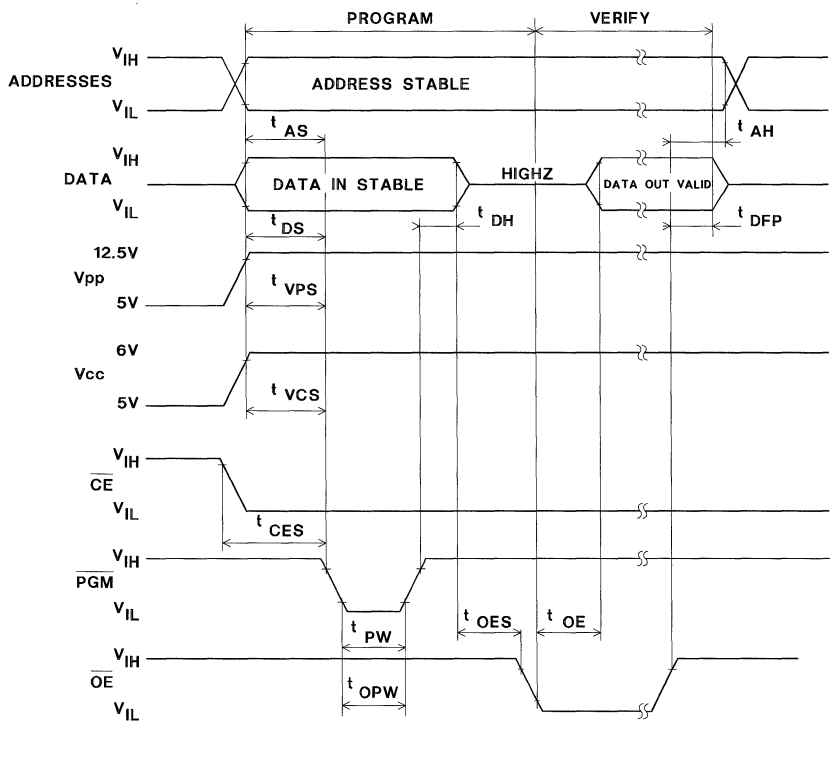
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				75	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(See Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

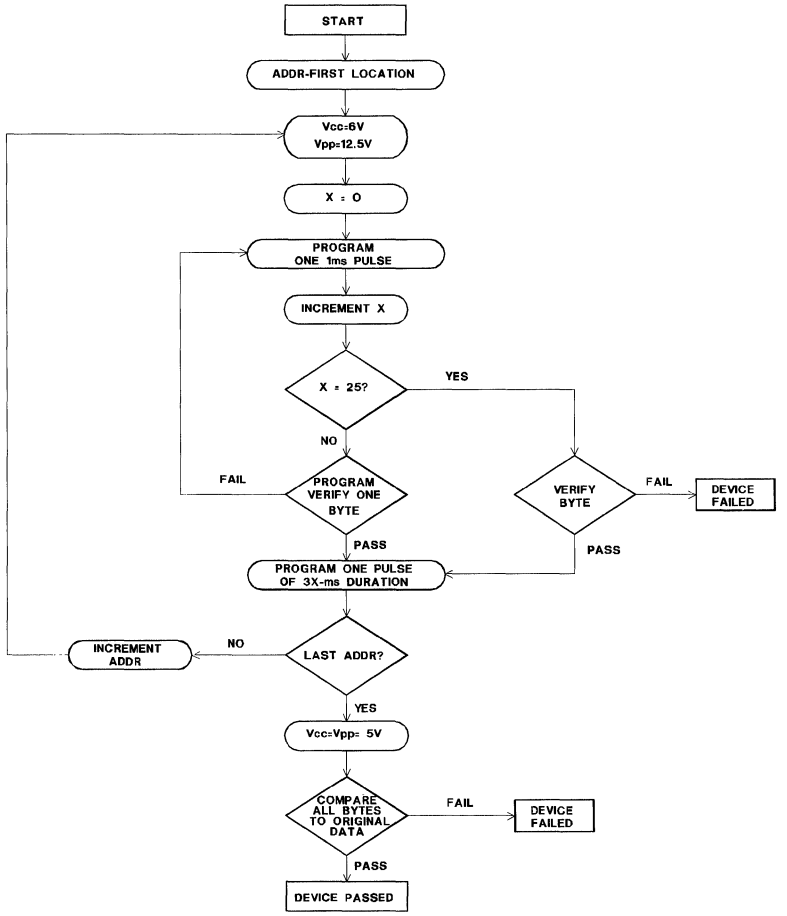
NOTES :
1. V_{CC} Must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ± 5%.
4. This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M2764A a 0.1µF capacitor is required across V_{PP} and GROUND to suppress voltage transients which can damage the device.

Figure 7 : Fast Programming Flowchart

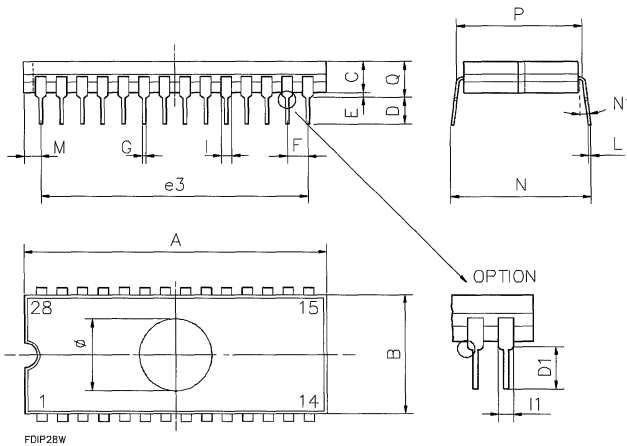


ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2764A-1F1	180 ns	5V ± 5%	0°C to +70°C	DIP-28
M2764A-2F1	200 ns	5V ± 5%	0°C to +70°C	DIP-28
M2764AF1	250 ns	5V ± 5%	0°C to +70°C	DIP-28
M2764A-3F1	300 ns	5V ± 5%	0°C to +70°C	DIP-28
M2764A-4F1	450 ns	5V ± 5%	0°C to +70°C	DIP-28
M2764A-18F1	180 ns	5V ± 10%	0°C to +70°C	DIP-28
M2764A-20F1	200 ns	5V ± 10%	0°C to +70°C	DIP-28
M2764A-25F1	250 ns	5V ± 10%	0°C to +70°C	DIP-28
M2764A-30F1	300 ns	5V ± 10%	0°C to +70°C	DIP-28
M2764A-45F1	450 ns	5V ± 10%	0°C to +70°C	DIP-28
M2764AF6	250 ns	5V ± 5%	-40°C to +85°C	DIP-28
M2764A-4F6	450 ns	5V ± 5%	-40°C to +85°C	DIP-28

PACKAGE MECHANICAL DATA

Figure 8 : 28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

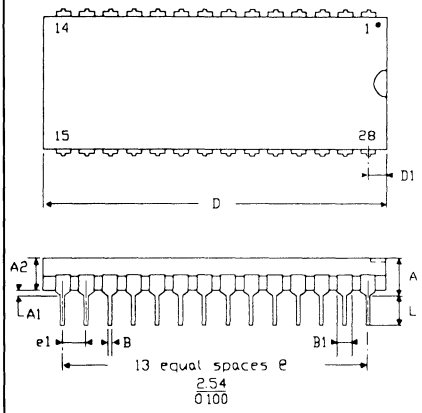
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST2764A-20 CP	200 ns	5V ± 10%	0°C to +70°C	DIP28
ST2764A-25 CP	250 ns	5V ± 10%	0°C to +70°C	DIP28

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA - OTP ROM

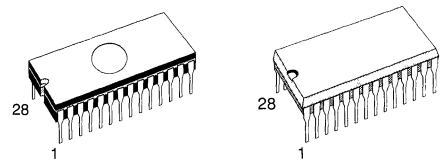
Figure 9 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

128K (16K x 8) NMOS UV EPROM - OTP ROM

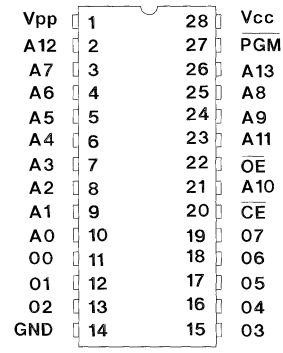
- FAST ACCESS TIME : 200 ns.
- 0 TO + 70 °C STANDARD TEMPERATURE RANGE.
- – 40 TO + 85 °C EXTENDED TEMPERATURE RANGE.
- SINGLE + 5 V POWER SUPPLY.
- ± 10 % V_{CC} TOLERANCE AVAILABLE.
- LOW STANDBY CURRENT (40mA MAX).
- TTL PROGRAM DURING READ AND PROGRAM.
- FAST PROGRAMMING ALGORITHM.
- ELECTRONIC SIGNATURE.



FDIP-28 PDIP-28

(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection



VR000644

DESCRIPTION

The M27128A is a 131,072-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 16,384 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

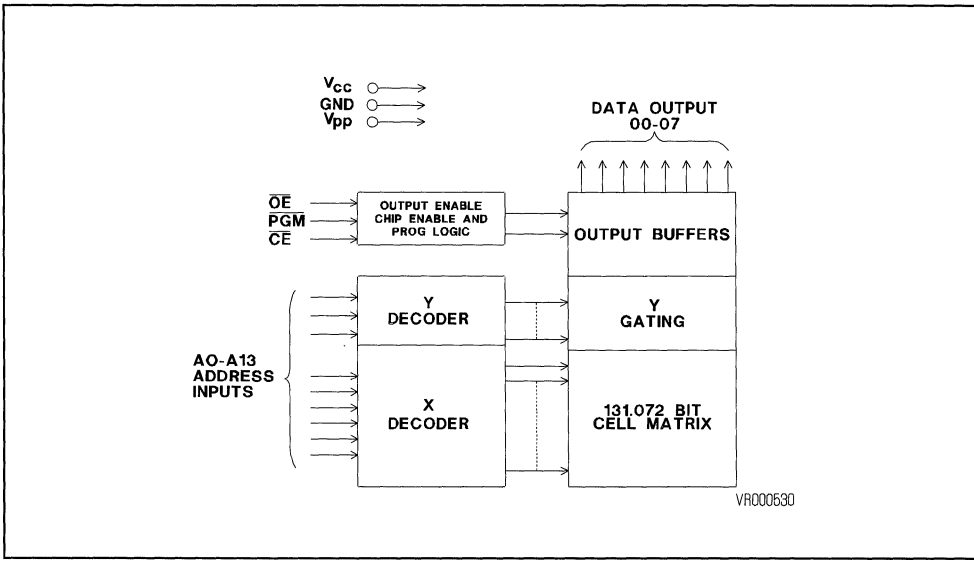
It is housed in a 28 Pin window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements cost effective solution, this product is also offered in a plastic DIL package.

PIN NAMES

A0-A13	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
O0-O7	DATA INPUT/OUTPUT

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Values	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.25 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to -0.6	V
T_{AMB}	Ambient temperature under bias /F1 /F6	-10 to +80 - 50 to +95	°C °C
T_{STG}	Storage temperature range	- 65 to +125	°C
VA9	Voltage on pin 24 with respect to ground	+13.5 to -0.6	V

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS						
	$\overline{CE}$	OE	A9	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	DIN
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE : X can be V_{IH} or V_{IL} . V_H = 12V ± 0.5V

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0°C to +70°C	-40°C to +85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**2F1, F1** **3F1, 4F1**	**20F1, 25F1** **30F1, 45F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ(3)	Max	
I_{LI}	Input Load Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{PP1}(2)	V_{PP} Current Read	V_{PP} = 5.5V			5	mA
I_{CC1}(2)	VCC Current Standby	$\overline{CE}$ = V_{IH}			40	mA
I_{CC2}(2)	VCC Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL} V_{PP} = V_{CC}			85	mA
V_{IL}	Input Low Voltage		-0.1		+0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	IOL = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4			V
V_{PP}(2)	VPP Read Voltage	V_{CC} = 5V ± 0.25V	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameters	V_{CC} ± 5%	27128A-2		27128A		27128A-3		27128A-4		Unit
		V_{CC} ± 10%	27128A-20		27128A-25		27128A-30		27128A-45		
		Test Condition	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		75		100		120		150	ns
t_{DF}(4)	$\overline{OE}$ High to output Float	$\overline{CE}$ = V_{IL}	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		0		ns

CAPACITANCE(5) (T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ(2)	Max	Unit
C_{IN}(2)	Input Capacitance	VIN = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).
5. This parameter is only sampled and is not 100% tested.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

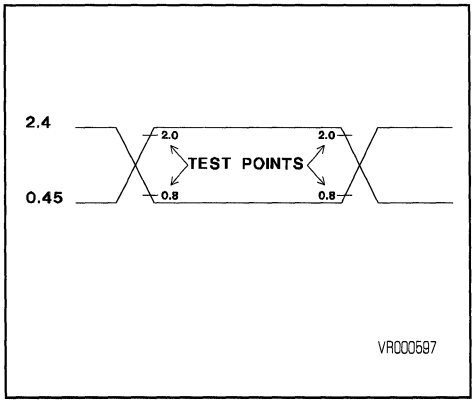


Figure 4 : AC Testing Load Circuit

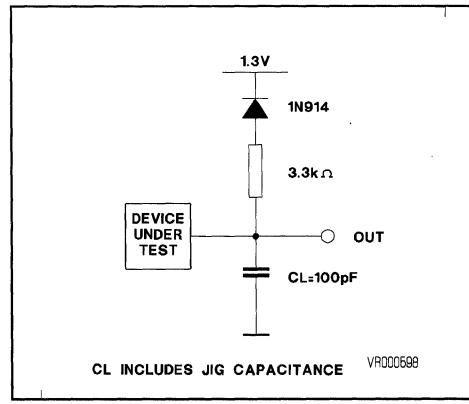
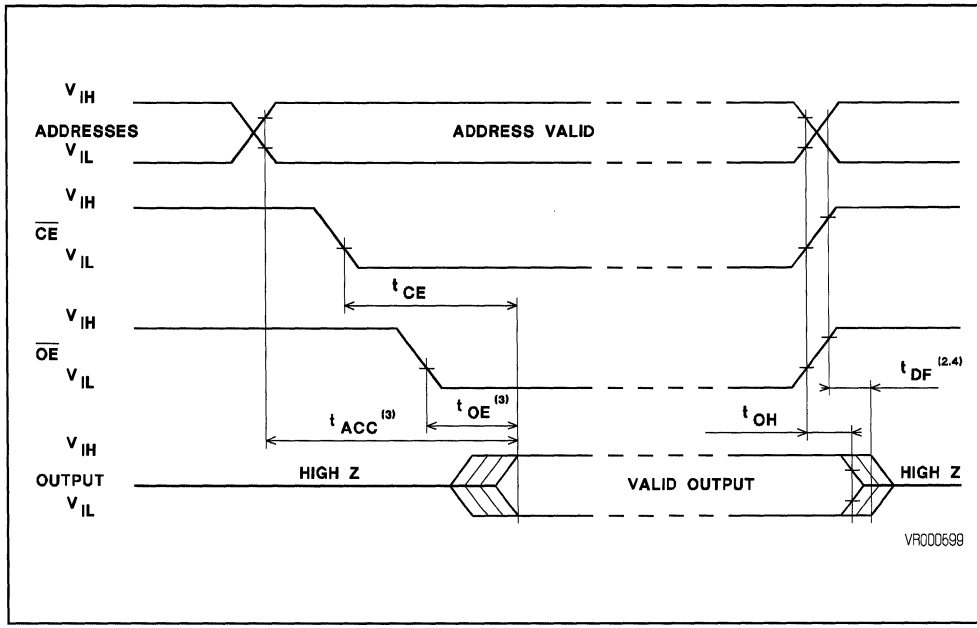


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.

2. This parameter is only sampled and not 100% tested.

3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.

4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the M27128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27128A has a standby mode which reduces the maximum active power current from 85 mA to 40 mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 13V on pin 1 (V_{PP}) will damage the M27128A.

When delivered (and after each erasure for UV EPPROM), all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram.

DEVICE OPERATION (Continued)

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5V.

PROGRAM INHIBIT

Programming of multiple M27128A's in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27128A. A high level $\overline{CE}$ input inhibits the other M27128A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5°C ambient temperature range that is required when programming the M27128A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27128A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27128A, these two identifier bytes are given below.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27128A should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	0	0	1	89

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[1] = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTICS

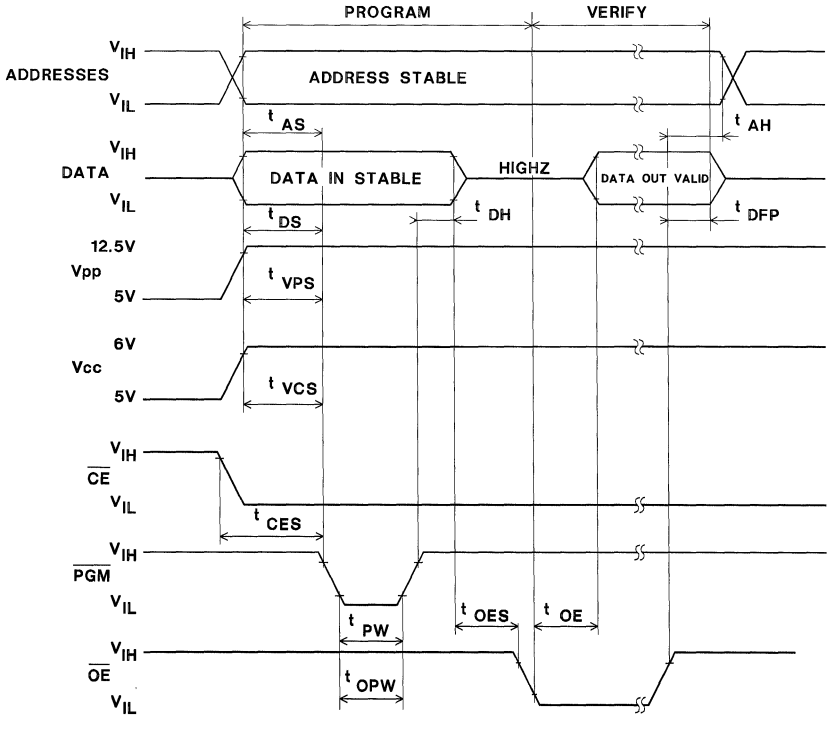
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min		Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(See Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

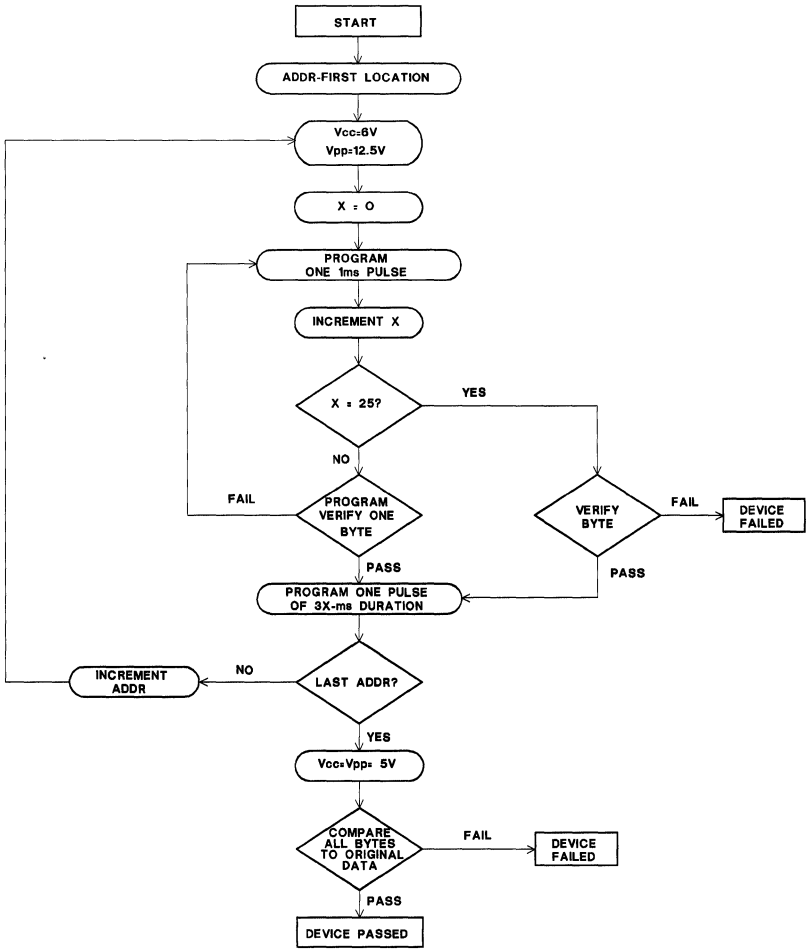
NOTES :
1. V_{CC} Must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ± 5%.
4. This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27128A a 0.1µF capacitor is required across V_{PP} and GROUND to absorb spurious voltage transients which can damage the device.

Figure 7 : Fast Programming Flowchart



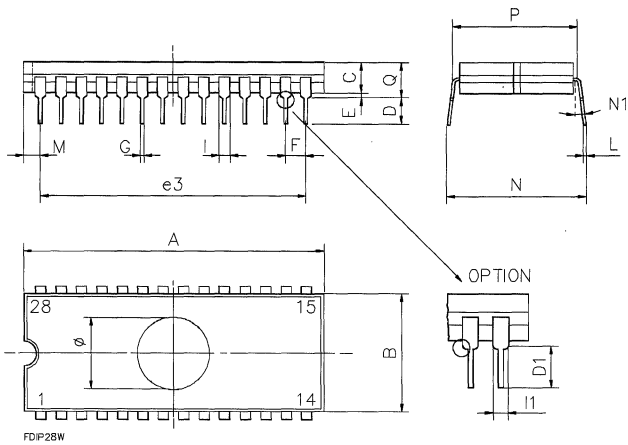
VR000541

ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27128A-2F1	200 ns	5V ± 5%	0°C to +70°C	DIP-28
M27128AF1	250 ns	5V ± 5%	0°C to +70°C	DIP-28
M27128A-3F1	300 ns	5V ± 5%	0°C to +70°C	DIP-28
M27128A-4F1	450 ns	5V ± 5%	0°C to +70°C	DIP-28
M27128A-20F1	200 ns	5V ± 10%	0°C to +70°C	DIP-28
M27128A-25F1	250 ns	5V ± 10%	0°C to +70°C	DIP-28
M27128A-30F1	300 ns	5V ± 10%	0°C to +70°C	DIP-28
M27128A-45F1	450 ns	5V ± 10%	0°C to +70°C	DIP-28
M27128AF6	250 ns	5V ± 5%	-40°C to + 85°C	DIP-28
M27128A-4F6	450 ns	5V ± 5%	40°C to + 85°C	DIP-28

PACKAGE MECHANICAL DATA

Figure 8 : 28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

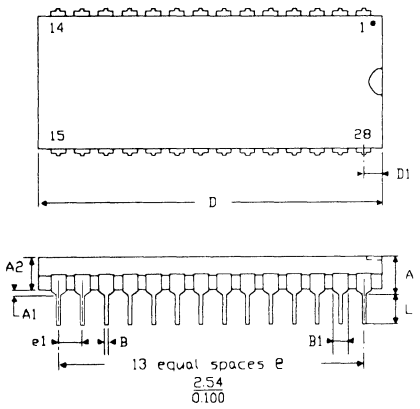
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST27128A-20 CP	200 ns	5V ± 10%	0°C to +70°C	DIP28
ST27128A-25 CP	250 ns	5V ± 10%	0°C to +70°C	DIP28

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA - OTP ROM

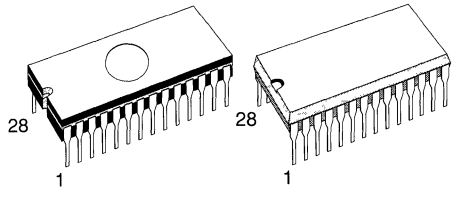
Figure 9 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

256K (32K x 8) NMOS UV EPROM - OTP ROM

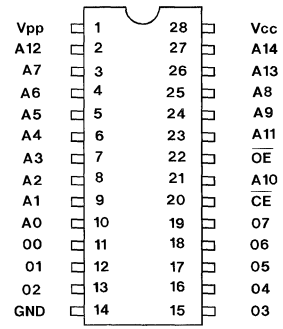
- FAST ACCESS TIME : 170 ns.
- 0 TO + 70°C STANDARD TEMP. RANGE.
- – 40 TO + 85°C EXTENDED TEMP. RANGE.
- SINGLE + 5V POWER SUPPLY.
- ± 10 % V_{CC} TOLERANCE AVAILABLE.
- LOW STANDBY CURRENT (40mA MAX).
- TTL COMPATIBLE DURING READ AND PROGRAM.
- FAST PROGRAMMING ALGORITHM.
- ELECTRONIC SIGNATURE.



FDIP-28 PDIP-28

(Ordering information at the end of the datasheet)

Figure 1 : Pin Configuration



DESCRIPTION

The M27256 is a 262,144-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 32.768 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

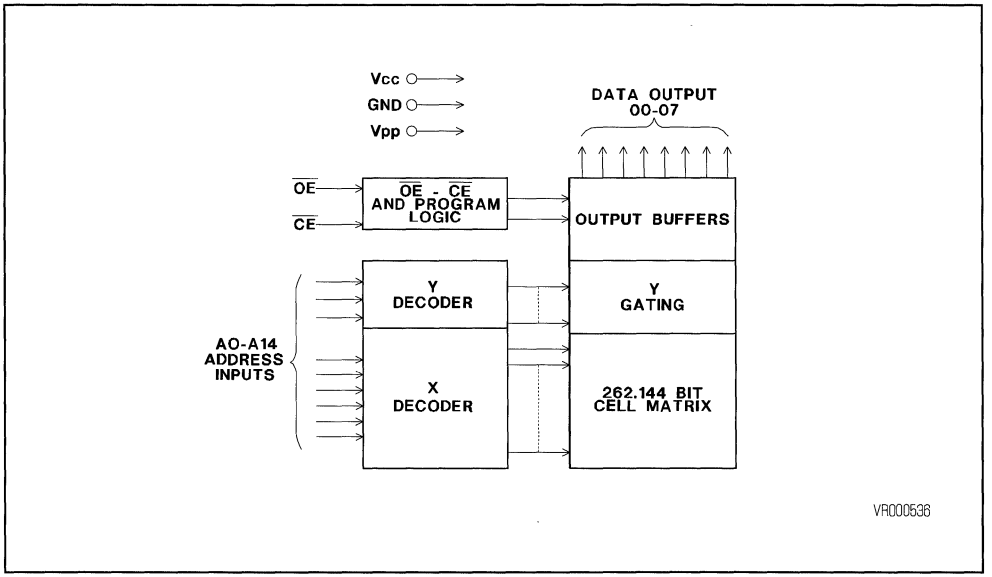
It is housed in a 28 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure

In order to meet production requirements (cost effective solution, this product is also offered in a plastic DIL package).

PIN NAMES

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Values	Unit
V_I	All input or Output voltages with respect to ground	+6.25 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to -0.6	V
T_{AMB}	Ambient temperature under bias /F1 /F6	-10 to +80 -50 to +95	°C °C
T_{STG}	Storage temperature range	-65 to +125	°C
VA9	Voltage on pin 24 with respect to ground	+13.5 to -0.6	V

OPERATING MODES

MODE	PINS						
	$\overline{CE}$	$\overline{OE}$	A9	A0	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
OPTIONAL VERIFY	V_{IL}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	V_{CC} V_{CC}	MAN.CODE DEV.CODE

NOTE : X can be V_{IH} or V_{IL} . V_H = 12V ± 0.5V

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0°C to 70°C	-40°C to 85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**1F1, 2F1, F1, 3F1, 4F1**	**20F1, 25F1, 30F1, 45F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ (3)	Max.	
I_{LI}	Input Leakage Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V			10	µA
I_{PP1} (2)	V_{PP} Current Read	V_{PP} = 5.5V			5	mA
I_{CC1} (2)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		20	40	mA
I_{CC2} (2)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL} ; V_{PP} = V_{CC}		45	100	mA
V_{IL}	Input low voltage		-0.1		+0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+ 1	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output high voltage	I_{OH} = -400 µA	2.4			V
V_{PP} (2)	V_{PP} Read Voltage	V_{CC} = 5V ± 0.25V	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} ± 5%	27256-1		27256-2		27256		27256-3		27256-4		Unit
		V_{CC} ± 10%			27256-20		27256-25		27256-30		27256-45		
		Test Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		170		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output delay	$\overline{OE}$=V_{IL}		170		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		70		75		100		120		150	ns
t_{DF} (4)	$\overline{OE}$ High to Output float	$\overline{CE}$=V_{IL}		35	0	55	0	60	0	105	0	130	ns
t_{OH}	Output hold from address $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE(5) (T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
4. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
5. Timing parameter is only sampled and not 100% tested.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

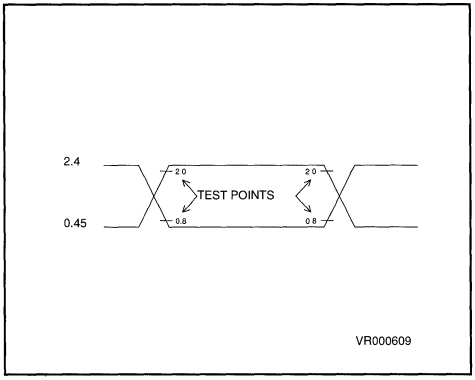


Figure 4 : AC Testing Load Circuit

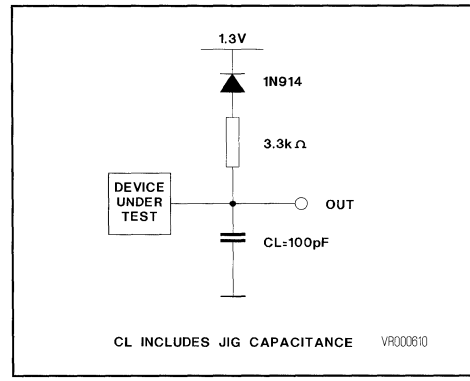
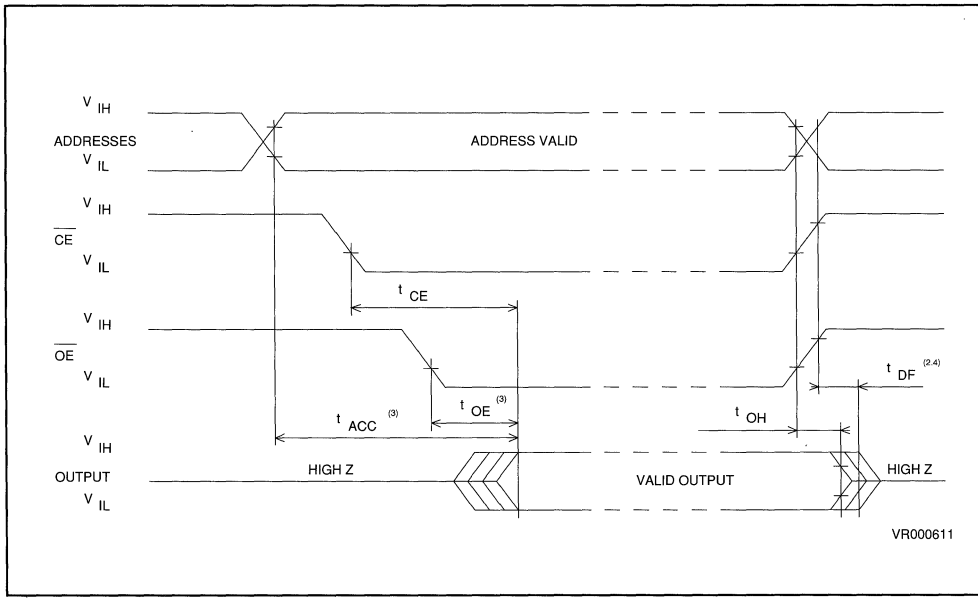


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes Table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27256 has a standby mode which reduces the maximum active power current from 100mA to 40mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 13V on pin 1 (V_{PP}) will damage the M27256.

When delivered, (and after each erasure for UV EPROM), all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V.

DEVICE OPERATION (continued)

When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = V_{PP} = 5V.

PROGRAM INHIBIT

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27256. A high level $\overline{CE}$ input inhibits the other M27256s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

OPTIONAL VERIFY

The optional verify may be performed instead of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at 12.5V. The outputs will three-state according to the signal presented to $\overline{OE}$. Therefore, all devices with V_{PP} = 12.5V and $\overline{OE}$ = V_{IL} will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (= 6V) and the normal read mode used to execute a program verify.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS-THOMSON M27256, these two identifier bytes are given below.

ERASURE OPERATION

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque lables be put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27256 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	0	1	0	0	04

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}[1] = 6V ± 0.25V, V_{PP}[1] = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTICS

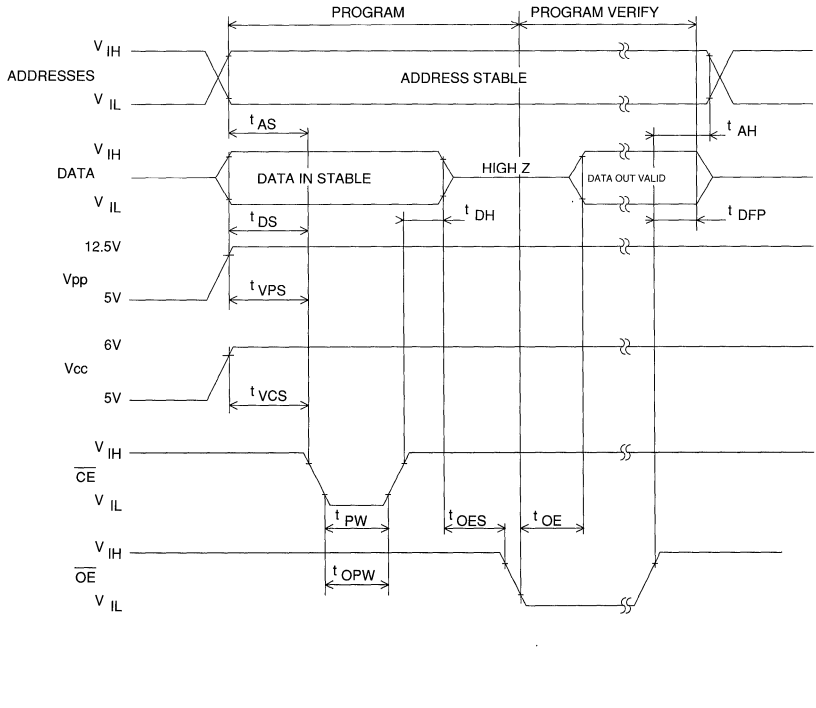
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

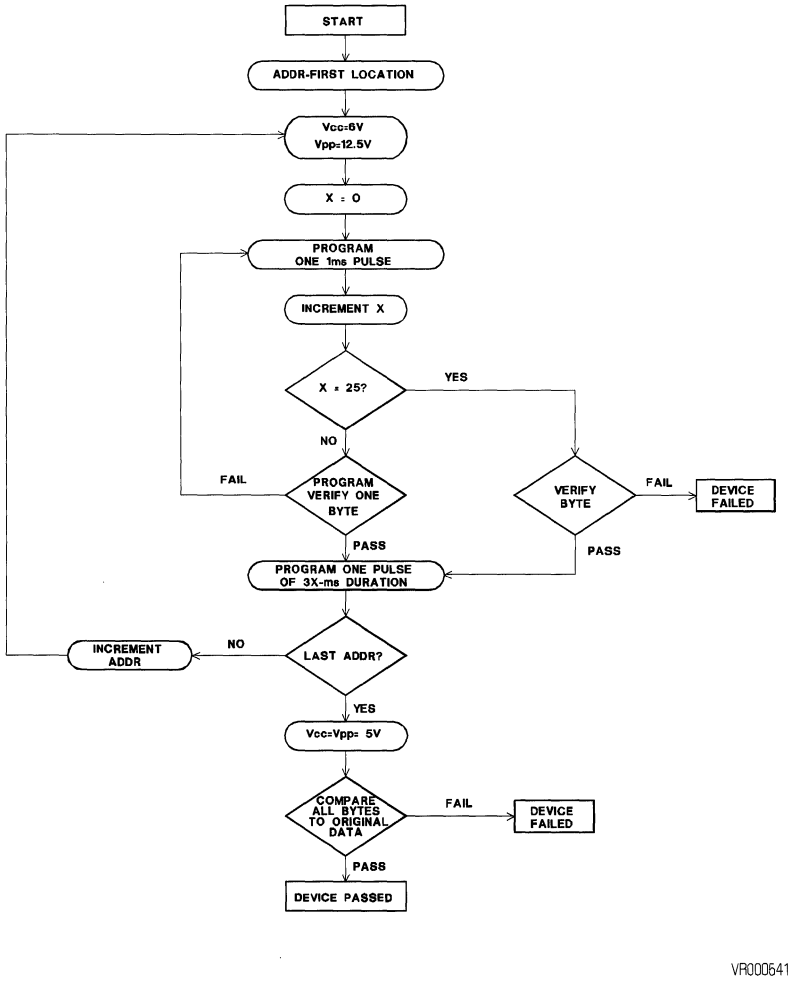
NOTES :
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1 msec ± 5%.
4. This parameter is only sampled and not 100 % tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27256 a 0.1µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

Figure 7 : Fast Programming Flowchart

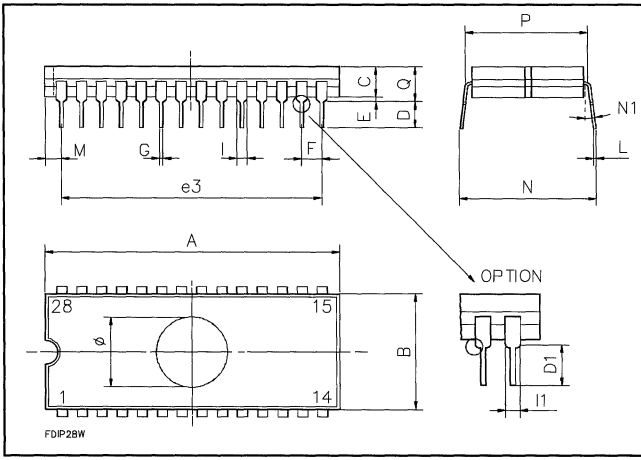


ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27256-1F1	170 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-2F1	200 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256F1	250 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-3F1	300 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-4F1	450 ns	5 V ± 5%	0 to +70°C	DIP-28
M27256-20F1	200 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256-25F1	250 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256-30F1	300 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256-45F1	450 ns	5 V ± 10%	0 to +70°C	DIP-28
M27256F6	250 ns	5 V ± 5%	-40 to + 85°C	DIP-28
M27256-4F6	450 ns	5 V ± 5%	-40 to + 85°C	DIP-28

PACKAGE MECHANICAL DATA

Figure 8 : 28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.199
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.027
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

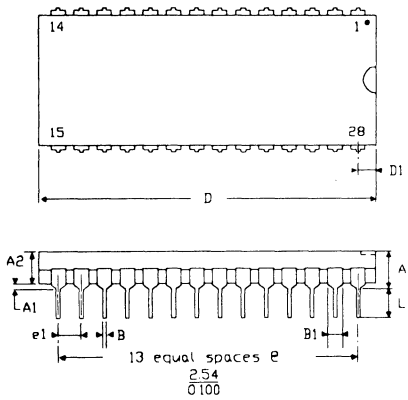
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST27256-20CP	200 ns	5 V ± 10%	0 to +70°C	DIP28
ST27256-25CP	250 ns	5 V ± 10%	0 to +70°C	DIP28

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA

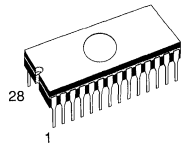
Figure 9 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			0.025	
B		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

512K (64K x 8) NMOS UV EPROM

- FAST ACCESS TIME : 200 ns.
- 0 TO + 70 °C STANDARD TEMP. RANGE.
- -40° TO 85°C EXTENDED TEMP. RANGE.
- SINGLE + 5V POWER SUPPLY.
- LOW STANDBY CURRENT (40mA Max).
- TTL COMPATIBLE.
- FAST PROGRAMMING.
- ELECTRONIC SIGNATURE.



FDIP-28

(Ordering information at the end of the datasheet)

DESCRIPTION

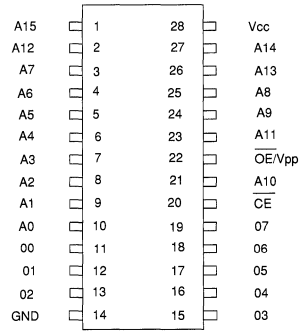
The M27512 is a 524,288-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 8 bits and manufactured using SGS-THOMSON' S NMOSE-E3 process.

It is housed in a 28 Pin Ceramic Frit Seal Window package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

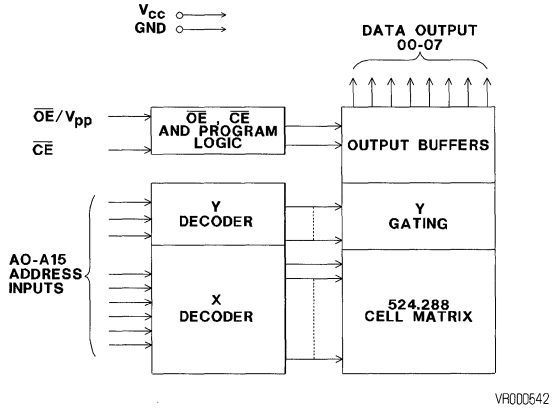
PIN FUNCTIONS

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}/V_{PP}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

Pin Connection



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameters	Values	Units
V_I	All Input or Output voltages with respect to ground	+6.5 to -0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to -0.6	V
T_{AMB}	Ambient temperature under bias /F1 /F6	-10 to + 80 -50 to + 95	°C °C
T_{STG}	Storage temperature range	-65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to -0.6	V

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS					
	$\overline{CE}$	OE/V_{PP}	A9	A0	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
PROGRAM INHIBIT	V_{IH}	V_{PP}	X	X	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	MAN.CODE DEV.CODE

NOTE : X can be V_{IH} or V_{IL} . V_H = 12V ± 0.5V

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1/-2F1/-3F1	-20F1/-25F1/-30F1	-2F6/F6
Operating Temperature Range	0 to 70°C	0 to 70°C	-40 to 85°C
V_{CC} Power Supply (1,2)	5V ± 5 %	5V ± 10 %	5V ± 5 %
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ (2)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{CC1}	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
I_{CC2}	V_{CC} Current Active	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		90	125	mA
V_{IL}	Input Low Voltage		-0.1		+0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	IOH = -400 µA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	V_{CC} ± 5%	27512-2		27512		27512-3		Unit
		V_{CC} ± 10%	27512-20		27512-25		27512-30		
		Test Condition	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$		200		250		300	ns
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{OE} = V_{IL}$		75		100		120	ns
t_{DF}(3)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	0		0		0		ns

CAPACITANCE(4)

(T_{AMB} = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ (2)	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for T_{AMB} = 25°C and nominal supply voltages.
3. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
4. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

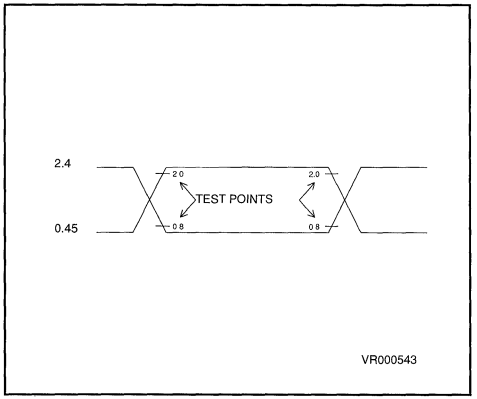
Input Rise and Fall Times : ≤ 20ns

Input Pulse Levels : 0.45 to 2.4V

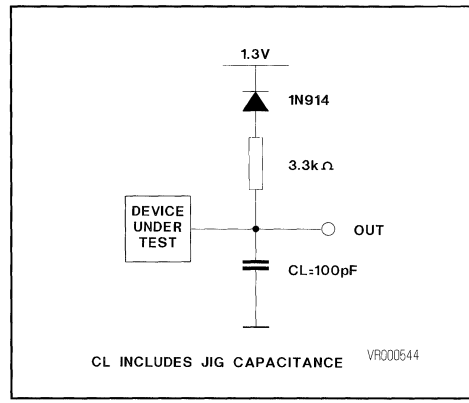
Timing Measurement Reference Levels :

Inputs 0.8 and 2V - Outputs 0.8 and 2V

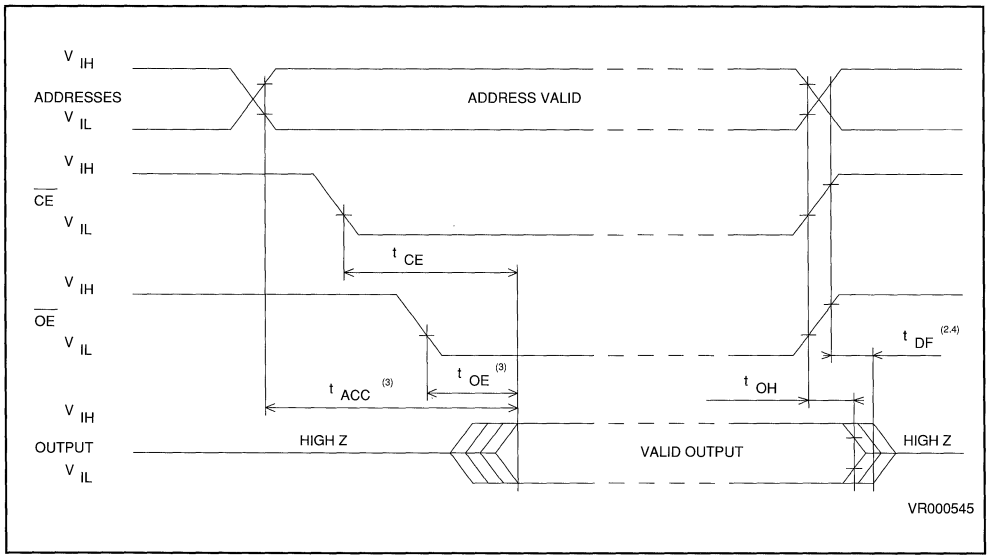
AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT



AC WAVEFORMS



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for Electronic Signature.

READ MODE

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{pp}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27512 has a standby mode which reduces the maximum active power current from 125 mA to 40 mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices.

The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommenced that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will permanently damage the M27512.

When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO* Programming Algorithm that drastically reduces the programming time (typically less than 50 seconds). Nevertheless to achieve compatibility with all programming equipment, the standard FAST Programming Algorithm may also be used.

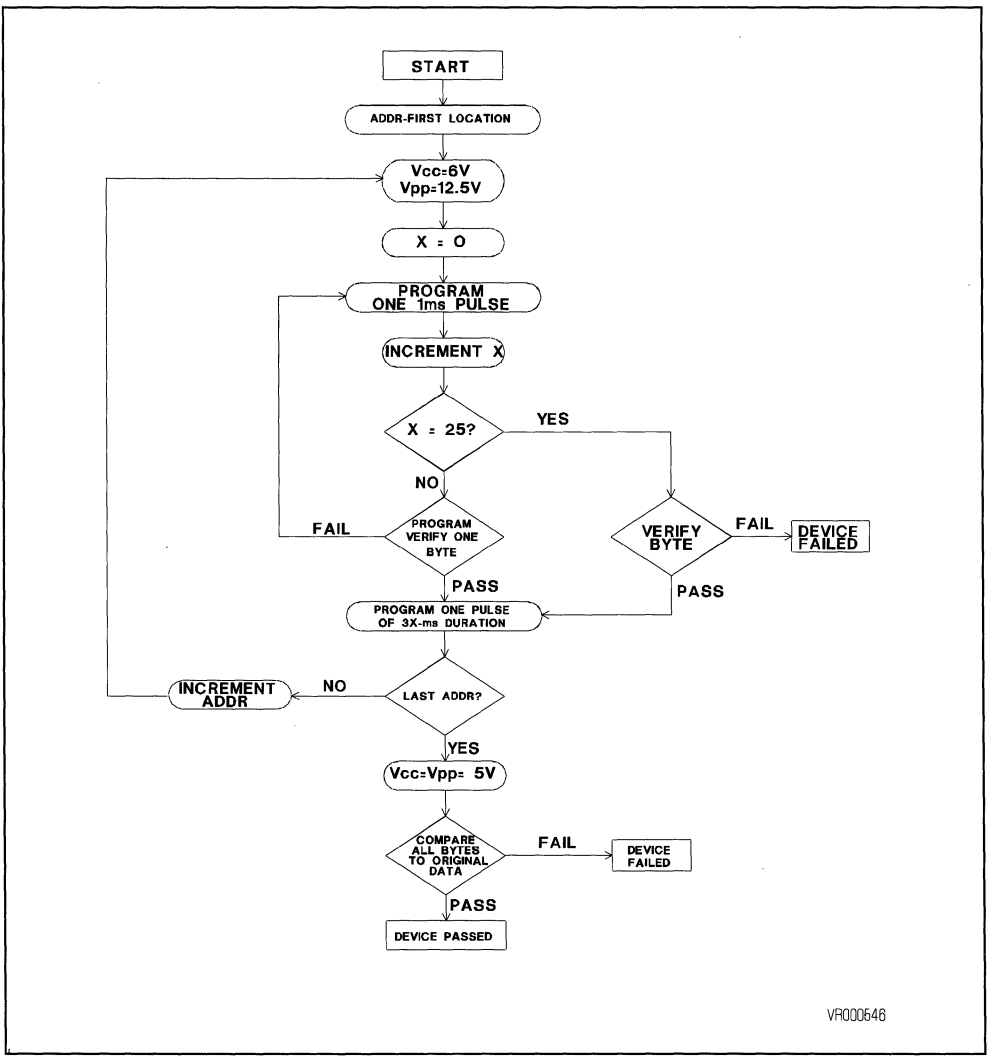
FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in the next page.

DEVICE OPERATION (Continued)

The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3 Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses is performed at V_{CC} = 6V and $\overline{OE}/V_{PP}$ = 12.5V (byte verifications at V_{CC} = 6 V and $\overline{OE}/V_{PP}$ = V_{IL}). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V.

FAST PROGRAMMING ALGORITHM FLOW CHART



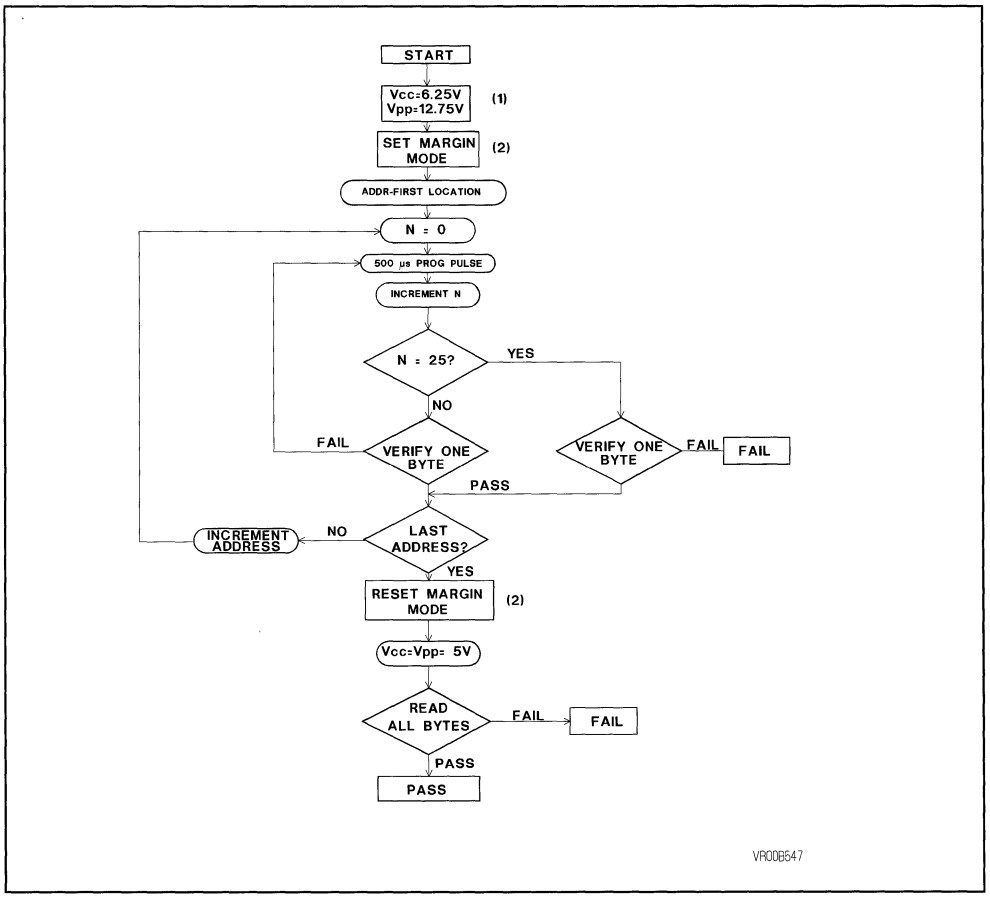
DEVICE OPERATION (Continued)

PRESTO PROGRAMMING ALGORITHM

PRESTO Programming Algorithm allows to program the whole array with a guaranted margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with the SGS-THOMSON M27512 due to several design innovations described in the next paragraph that improves programming efficiency and brings adequate margin for reliability. Before starting the programming the internal MARGIN MODE* circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 500 microseconds program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell. PRESTO programming algorithm is supported on the full line of DATA I/O programmers, for the most popular production equipment the firmware revision are :

- Series 1000 : revision V08.1
- Model 120 A and 121 A : revision V14.1

PRESTO PROGRAMMABLE ALGORITHM FLOW CHART

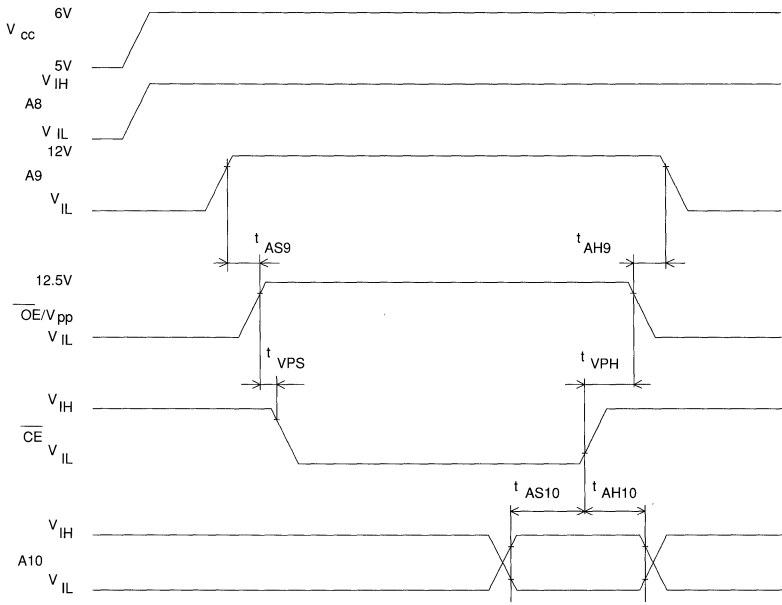


NOTES : 1. V_{CC} must be maintained at 6V during the whole programming algorithm between set and reset MARGIN MODE operation. A drop of V_{CC} below 4V could reset the internal MARGIN MODE flip-flop giving place to insufficient programming margins.

2. See MARGIN MODE set and reset waveforms.

DEVICE OPERATION (Continued)

MARGIN MODE SET AND RESET WAVEFORMS



NOTES : 1. Other addresses are don't care.
2. Set MARGIN MODE A10 = V_{IH}, Reset MARGIN MODE A10 = V_{IL}.

MARGIN MODE AC CHARACTERISTICS

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
t_{AS10}	A10 Setup Time		1			µs
t_{AH10}	A10 Hold Time		1			µs
t_{VPH}	V_{PP} Hold Time		2			µs
t_{VPS}	V_{PP} Setup Time		2			µs
t_{AS9}	A9 Setup Time		2			µs
t_{AH9}	A9 Hold Time		2			µs

DEVICES OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{CE}$ input, with $\overline{OE}/V_{pp}$ at 12.5V, will program that M27512. A high level $\overline{CE}$ input inhibits the other M27512s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{pp}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5 °C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A 15 which should be held high. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the SGS M27512, the two identifier bytes are given here below.

ERASURE OPERATION

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	01 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	1	1	0	1	0D

NOTE : A9 = 12V ± 0.5V ; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}/V_{PP}$ = V_{IL} ; A14, A15 = V_{IH}

PROGRAMMING OPERATION

(T_{AMB} = 25°C ± 5°C, V_{CC}(1) = 6V ± 0.25V, $\overline{OE}/V_{PP}$(1)= 12.5V ± 0.5V)

DC AND OPERATING CHARACTERISTICS

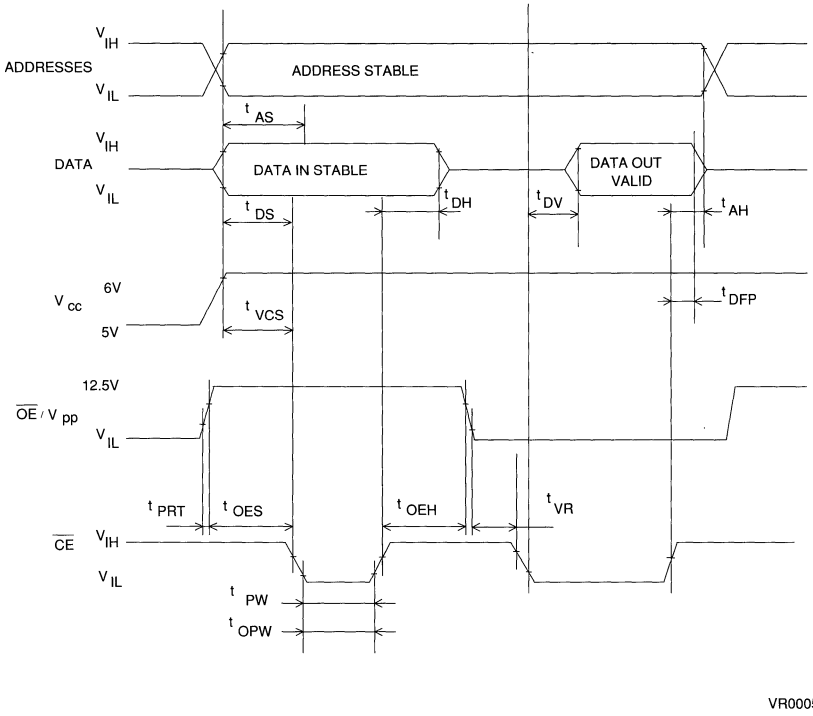
Symbol	Parameter	Test Condition (see note 1)	Values			Unit
			Min	Typ	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4			V
I_{CC2}	V_{CC} Supply Current				150	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (See note 1)	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2			µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VCS}	V_{CC} Setup Time		0			µs
t_{PW}(3)	$\overline{CE}$ Initial Program Pulse Width		0.95	1.0	1.05	ms
t_{OPW}(2)	$\overline{CE}$ Overprogram Pulse Width		2.85		78.75	ms
t_{DV}	Data Valid from $\overline{CE}$				1	ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns

NOTES :
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial program Pulse width tolerance is 1msec ± 5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

M27512 DESIGN INNOVATIONS FOR AN EFFICIENT PROGRAMMING (PRESTO)

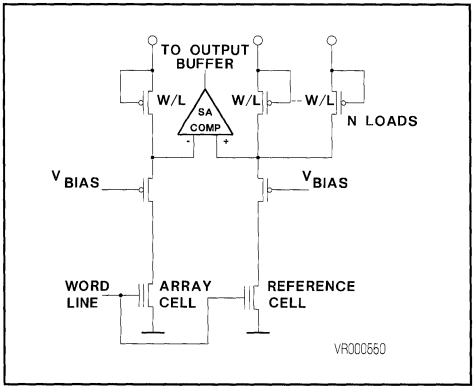
M27512 includes several design innovations which allows a very efficient programming :

- during programming the word line voltage is bootstrapped over the V_{PP} voltage by about 2V,
- the bit line voltage is regulated at the optimum value for fast write.

This allows a reduction of about one order of magnitude in the programming time. Programming is also independent on the V_{PP} voltage (from about 10V to 14V). The V_{CC} voltage (6V during the Algorithm) influences the programming speed since the cell drain voltage regulation uses V_{CC} as a reference.

The sensing scheme is also innovative in SGS-THOMSON M27512. Conventional sensing compares the addressed cell within the memory array with a reference cell (usually one reference cell for each word line) as shown in figure 1.

Figure 1 : Conventional Sensing Schematic



If the addressed cell is erased its current is the same as the reference cell's current and the unbalance at the inputs of the comparator (higher voltage on right side = 1) is obtained by connecting lower impedence load on the right side than on the left.

If the addressed cell is written (no current) the left input to the comparator will have a higher voltage than the right side (0 state).

The above approach has proved to be efficient and reliable but has a drawback in that V_{CC} is still dependent on the threshold shift of the written cell (at high V_{CC}).

This can be easily understood by looking at the cell transcharacteristics diagram : together with the characteristics of the erased and the written cell in the memory array, the "virtual" reference cell current can be drawn.

The "virtual" reference cell current is the current of the reference cell divided by the ratio between the impedance of the left side loads and the impedence of the right side loads (usually the ratio ranges from 2 to 5).

The figure 2 illustrates very well the dependance of V_{CC} (voltage on the addressed word line) on the threshold shift of the cell : the sensing of a written cell will not be correct where the "virtual" reference cell characteristic crosses and stays below the written cell characteristic (V_{CC} max).

The dependance of V_{CC} max on the threshold shift of a written cell can be illustrated as in figure 3, where the different lines are for different ratios between the impedance of the loads.

Figure 2 : Current relationship of reference and array cells (Conventional Technique)

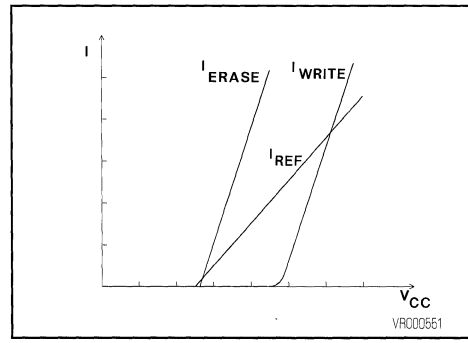
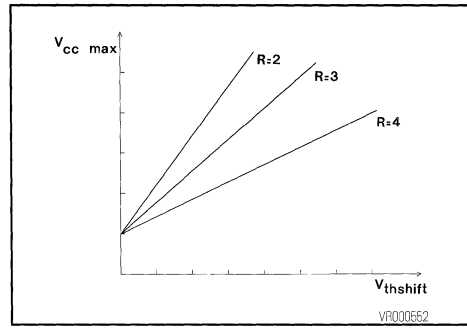


Figure 3 : Dependance of V_{CC} max on threshold shift (R = Loads impedance ratios-conventional techniques)

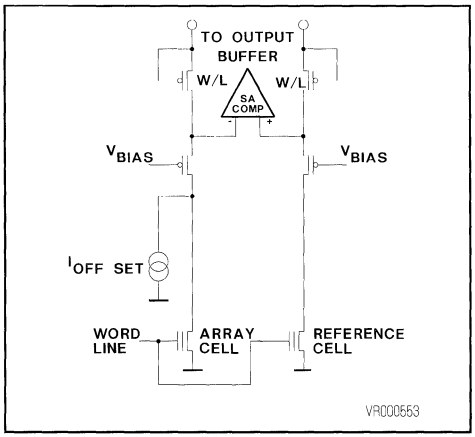


M27512 DESIGN INNOVATIONS FOR AN EFFICIENT PROGRAMMING (PRESTO) (Continued)

It can be concluded that a threshold shift of at least 2V to 3V is required by the program cell to guarantee a wide V_{CC} operation range and reliability.

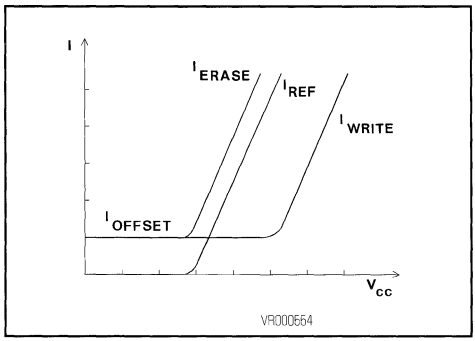
An innovative approach to sensing was implemented into the M27512 to remove the above described drawback. The sensing scheme is illustrated in figure 4 : the impedance of the loads is the same on both sides ; on the left side an offset current is added to the addressed cell's current - (patent pending).

Figure 4 = M27512 Sensing schematic



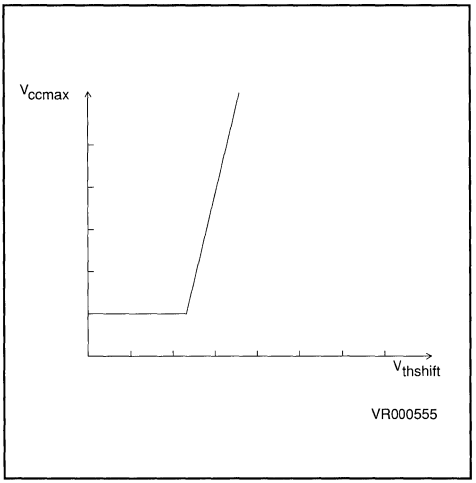
The improvement is easily pointed out in the diagram of the cell transcharacteristics (figure 5) : the difference in slope between the written cell and the reference cell is drastically reduced.

Figure 5 : Current relationship of reference and array cells (New Technique)



The final result is that a threshold shift of about 1V for a written cell is enough to allow proper sensing in a very wide V_{CC} operating range (figure 6).

Fgure 6 : Dependance of V_{CC} max on threshold Shift (M27512)



For better process margin and productibility the offset current is not fixed but tracks the matrix cell current. The improvement of both the programming speed and the sensing efficiency will reduce the typical programming time per byte to below 200 µsec.

In order to take full advantage of this the original PRESTO programming algorithm was developed as illustrated in the previous paragraph.

The similarity with the Fast Programming Algorithm is evident but several main differences exist :

- 500 µsec elementary pulses,
- no overprogram pulses are applied after correct verification of a byte,
- the existence of a sufficient margin for the written cells is guaranteed by making the program verify in a special test mode called MARGIN MODE*...

In order to read a cell in MARGIN MODE, the written cell must have a threshold shift of around 1V to 2V more than the required threshold shift for correct operation with wide V_{CC} range in normal operating mode. The circuit arrangement that allows to guarantee the margin is illustrated in figure 7.

The result in the transcharacteristic plan helps to understand the MARGIN MODE feature (figure 8). The threshold shift margin has been carefully tuned in order to guarantee that the V_{CC} operating range and the access time performance would not be reduced by a cell marginally written.

taking into account the temperature range, noise conditions, and data retention (intrinsic change loss).

The MARGIN MODE is set before starting the programming algorithm and reset after the completion.

Figure 7 : M27512 Sensing schematic with activated margin mode

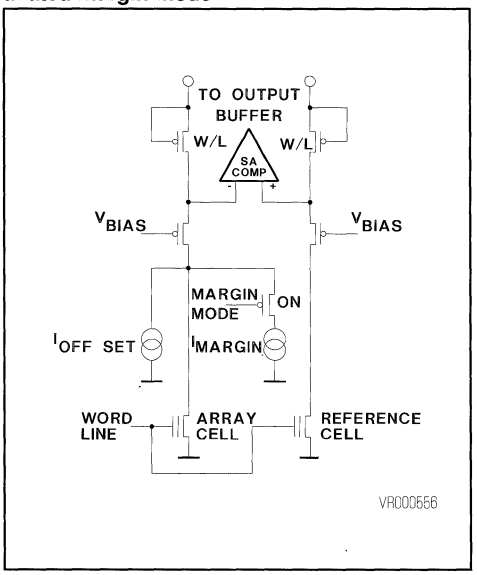
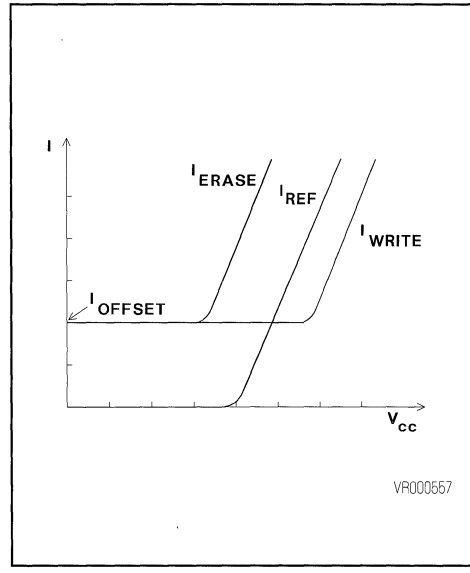


Figure 8 : Current relationship of reference and array cells with margin mode activated



CONCLUSION

M27512 has successfully achieved the goal of drastically reducing the programming time by :

- improving the programming efficiency,
- implementing an improved sensing scheme,
- guaranteeing by an innovative hardware approach an adequate margin for reliability.

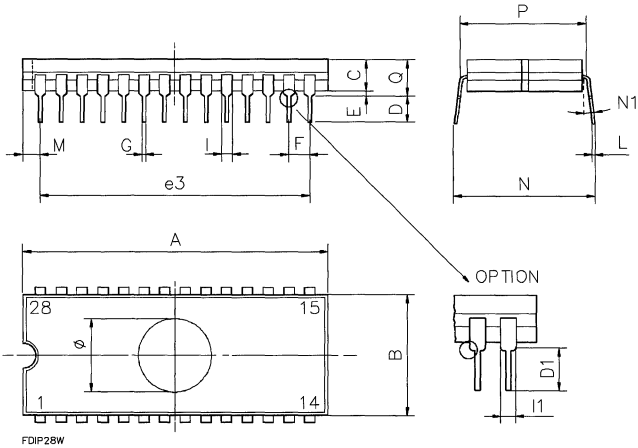
The goal has been achieved without any additional scaling of the well proven NMOS-E3 technology : further improvements can be foreseen, with the combination of the new scaled down technologies (CMOS-E4) with the above circuit techniques. Extensive characterization and life tests have demonstrated the efficiency and reliability of the solutions adopted.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27512-2F1	200 ns	5V ± 5%	0°C to +70°C	DIP28
M27512F1	250 ns	5V ± 5%	0°C to +70°C	DIP28
M27512-3F1	300 ns	5V ± 5%	0°C to +70°C	DIP28
M27512-20F1	200 ns	5V ± 10%	0°C to +70°C	DIP28
M27512-25F1	250 ns	5V ± 10%	0°C to +70°C	DIP28
M27512-30F1	300 ns	5V ± 10%	0°C to +70°C	DIP28
M27512-2F6	200 ns	5V ± 5%	-40°C to +85°C	DIP28
M27512F6	250 ns	5V ± 5%	-40°C to +85°C	DIP28

PACKAGE MECHANICAL DATA

Figure 9 : 28-PIN CERAMIC DIP BULL'S EYE



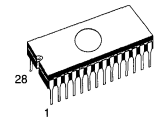
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	8.64		9.14	.340		.360

EPROM DEVICES

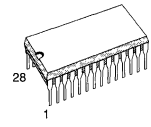
CMOS EPROM

64K (8K x 8) CMOS UV EPROM - OTPROM

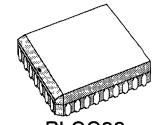
- FAST ACCESS TIME : 200 ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- 28-PIN JEDEC APPROVED PIN-OUT.
- LOW POWER CONSUMPTION :
  - ACTIVE 30mA Max
  - STANDBY 100µA Max
- PROGRAMMING VOLTAGE : 12.5V.
- HIGH SPEED PROGRAMMING (< 1 minute).
- ELECTRONIC SIGNATURE.



FDIP-28



PDIP-28



PLCC32

(Ordering information at the end of the datasheet)

DESCRIPTION

The TS27C64A is a high speed 65,536 bit UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The TS27C64A is housed in a 28 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIL or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A12	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O0-O7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NON CONNECTED

Figure 1 : Pin Connection

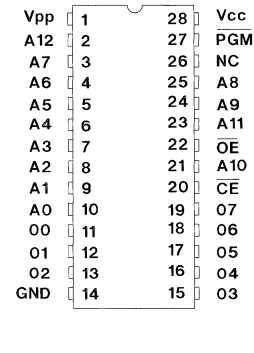
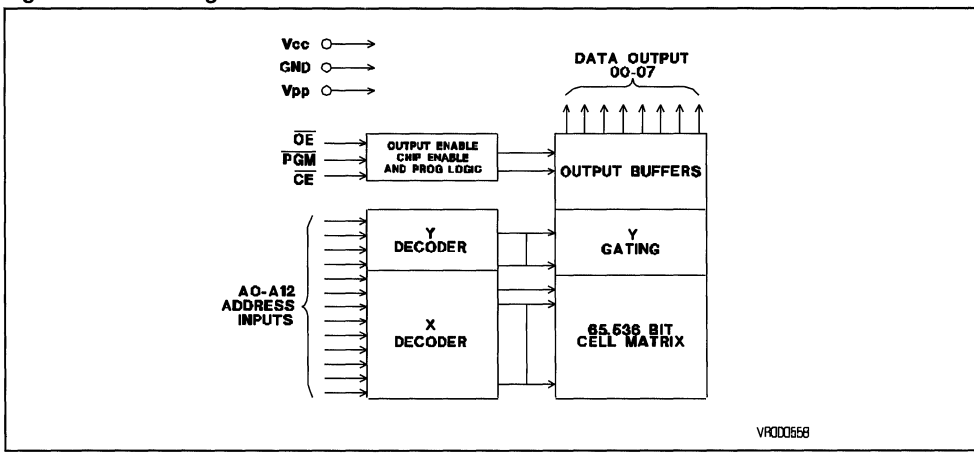


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Values	Unit
T_{AMB}	Operating temperature range TS27C64ACQ TS27C64AVQ	T_L to T_H 0 to +70 -40 to +85	°C
T_{STG}	Storage temperature range	-65 to +125	°C
V_{PP}(2)	Supply voltage	-0.6 to +14	V
V_{IN}(2)	Input voltages A9 Except V_{PP}, A9	-0.6 to +13.5 -0.6 to 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering : 10 seconds)	+300	°C

NOTES : 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except to "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to GND.

OPERATING MODES

MODE	PINS						
	$\overline{CE}$	OE	A9	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	CODE

NOTES : 1. X can be either V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code : 9B) to V_{IH} (type code : 08).

READ OPERATION

DC CHARACTERISTICS

(T_{AMB} = T_L to T_H, V_{CC} = 5V ± 10%, V_{SS} = 0V. Unless otherwise specified) (5)

Symbol	Parameter	Test Conditions	Values			Unit
			Min	Typ(1)	Max	
I_{LI}	Input Load Current	V_{IN} = V_{CC} or GND			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS} $\overline{CE}$ = V_{IH}			10	µA
V_{PP}	V_{PP} Read voltage		V_{CC} - 0.7		V_{CC}	V
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA I_{OL} = 0 µA			0.45 0.1	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = 0 µA	2.4 V_{CC}-0.1			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE}$=$\overline{OE}$=V_{IL}, Inputs=V_{IH} or V_{IL}, f = 5 MHz, I/O = 0mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	$\overline{CE}$ = V_{IH}		0.5	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$\overline{CE}$ = V_{CC}		10	100	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC} = 5.5V			100	µA

NOTE : 1. Typical conditions are for operation at : T_{AMB} = +25°C, V_{CC} = 5V, V_{PP} = V_{CC} and V_{SS} = 0V

AC CHARACTERISTICS(1)

(T_{AMB} = T_L to T_H)(5)

Symbol	Parameter	Test condition	27C64A						Unit
			-20		-25		-30		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$= $\overline{OE}$=V_{IL}		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		80		100		120	ns
t_{DF}(2,4)	$\overline{OE}$ or $\overline{CE}$ High to Output Float		0	50	0	60	0	105	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		ns

CAPACITANCE

T_{AMB} = +25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Test Condition	Min	Typ.(2)	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. V_{PP} may be connected to V_{CC} except during program.
2. The t_{DF} compare level is determined as follows :
High to THREE-STATE, the measured $V_{OH}^{(DC)}$ -0.1V
Low to THREE-STATE the measured $V_{OL}^{(DC)}$ + 0.1V.
3. Capacitance is guaranteed by periodic testing. T_{AMB} = +25°C, f=1MHz.
4. T_{DF}, is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first. This parameter is only sampled and not 100 % tested.
5. All parameters are specified at V_{CC} = 5V ± 5% for 27C64-20X, 27C64-25X and 27C64-30X.

READ OPERATION (Continued)

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20 ns

Input pulse levels : 0.45V to 2.4V

Timing Measurement Reference Level :

Inputs : 0.8V and 2V - Outputs : 0.8V and 2V

Figure 3 : AC Testing Input/Output Waveform

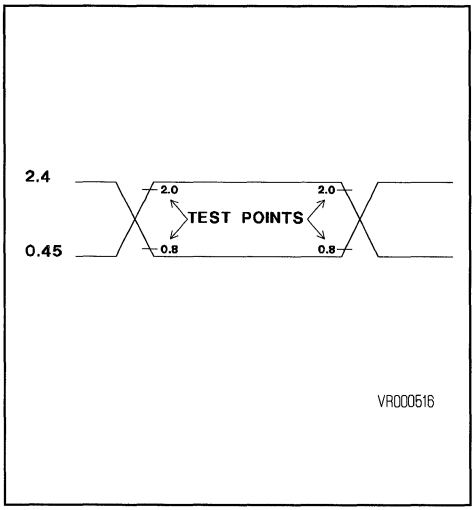


Figure 4 : AC Testing Load Circuit

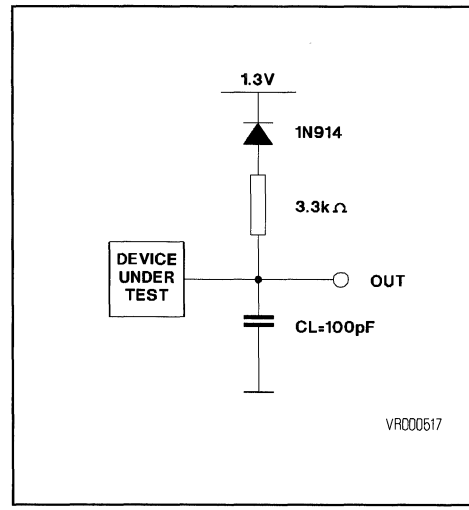
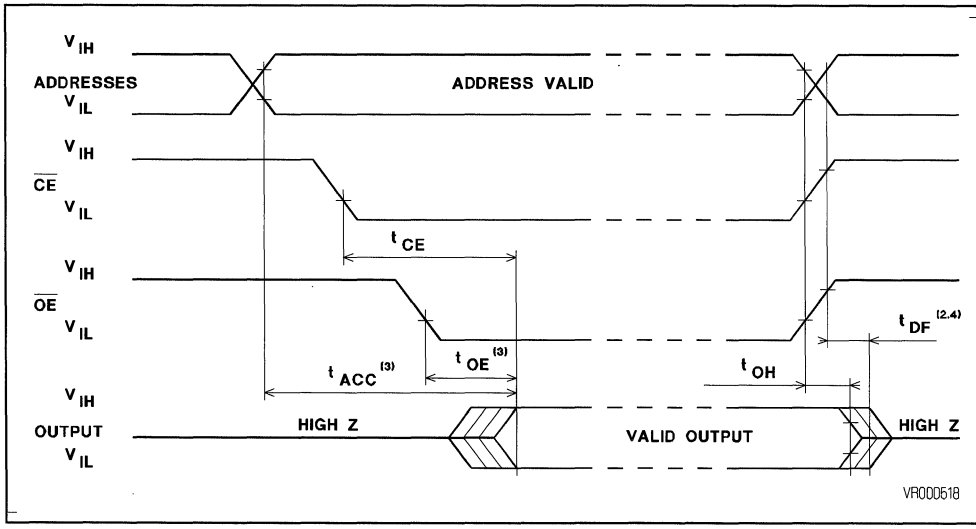


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{AMB} = 25°C and nominal supply voltage.

2. This parameter is only sampled and not 100% tested.

3. $\overline{OE}$ may be delayed up to t_{ACC} - $t\overline{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.

4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the TS27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 in electronic signature mode.

READ MODE

The TS27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The TS27C64A has a standby mode which reduces the maximum power dissipation to 5.5mW. The TS27C64A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accommodate this multiple memory connection. The two control lines allow for :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is required from a particular memory device.

PROGRAMMING MODES

Caution : Exceeding 14V on V_{PP} will damage the TS27C64A.

Initially, (and after each erasure for UV EPROM), all bits of the TS27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C64A is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. To avoid damage to the device from spurious voltage transients, a 0.1 µF filter capacitor must be placed accross V_{PP}, V_{CC} and ground. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled TS27C64As.

HIGH SPEED PROGRAMMING

The high speed programming algorithm described in the flowchart rapidly programs the TS27C64A using an efficient and reliable method particularly suited to the production programming environment. An individual device will take around 1 minute to program.

PROGRAM INHIBIT

Programming of multiple TS27C64As in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64As from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64As may be common. A TTL low-level pulse applied to a TS27C64A $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at 12.5V will program that TS27C64A.

PROGRAM VERIFY

A verify may be performed on the programmed bits to ensure that they were correctly programmed. The verify routine is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will identify the EPROM manufacturer and type.

This mode is intended for use with programming equipment in oder to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64A. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 of the TS27C64A. Two bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electronic signature mode.

ERASING (applies for UV EPROM)

The TS27C64A is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C64A be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces I_{CC} due to photodiode currents. An ultraviolet source of 2537A yielding a total integrated dosage of 15 watt seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 $\mu W/cm^2$ power rating is used. The TS27C64A to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PROGRAMMING OPERATIONS(1)

(T_{AMB} = 25 ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Values			Unit
			Min	Typ	Max	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (all inputs)		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low voltage during verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High voltage during verify	I_{OH} = -400 µA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				30	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values			Unit
			Min	Typ	Max	
t_{AS}	Address Set-up time		2			µs
t_{OES}	$\overline{OE}$ Set-up Time		2			µs
t_{DS}	Data Set-up Time		2			µs
t_{AH}	Address Hold time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			µs
t_{VCS}	V_{CC} set-up time		2			µs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}(2)	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{CES}	$\overline{CE}$ set-up time		2			µs
t_{OE}	Data valid from $\overline{OE}$				150	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

AC TEST CONDITIONS

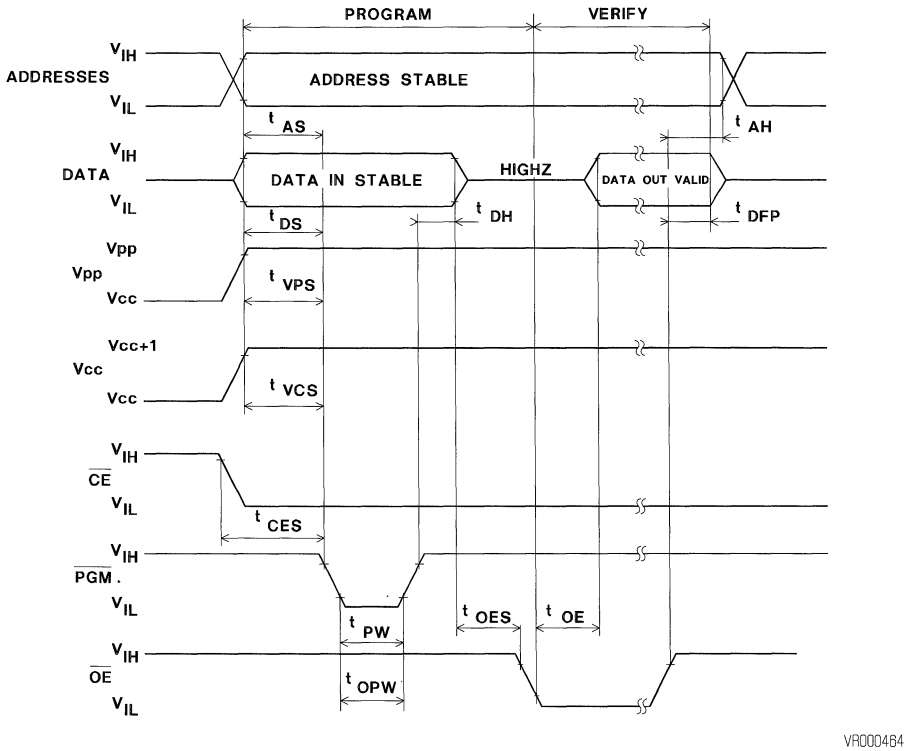
Input rise and fall times (10% to 90%) : ≤ 20ns

Input pulse levels : 0.45V to 2.4V

Timing reference levels :

Inputs : 0.8V and 2.0V - Outputs : 0.8V and 2.0V

Figure 6 : High Speed Programming Waveforms

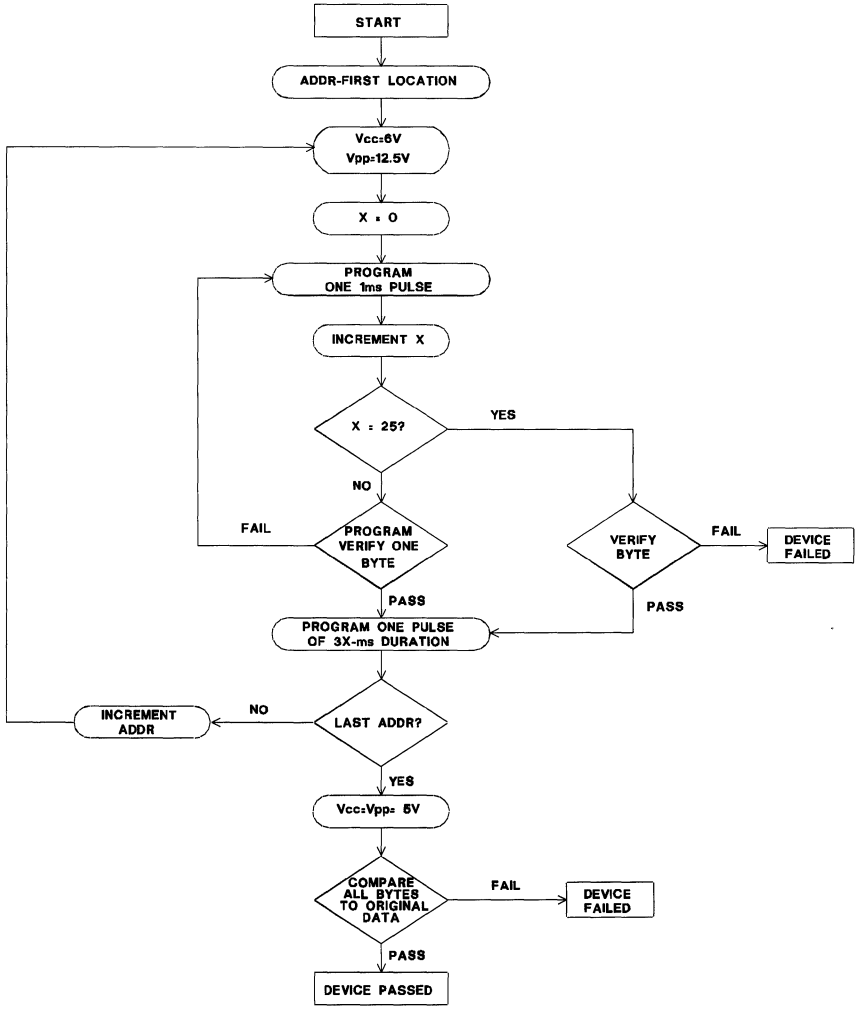


NOTES : 1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

3. When programming the TS27C64A, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 7 : High Speed Programming Flow Chart



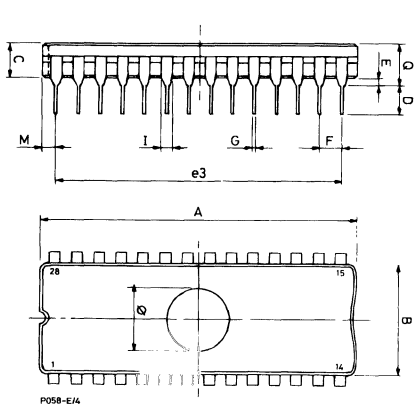
VR000563

ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-20XCQ	200 ns	5V ± 5%	0°C to + 70°C	FDIP-28
TS27C64A-25XCQ	250 ns	5V ± 5%	0°C to +70°C	FDIP-28
TS27C64A-30XCQ	300 ns	5V ± 5%	0°C to + 70°C	FDIP-28
TS27C64A-20CQ	200 ns	5V ± 10%	0°C to + 70°C	FDIP-28
TS27C64A-25CQ	250 ns	5V ± 10%	0°C to + 70°C	FDIP-28
TS27C64A-30CQ	300 ns	5V ± 10%	0°C to + 70°C	FDIP-28
TS27C64A-20VQ	200 ns	5V ± 10%	-40°C to + 85°C	FDIP-28
TS27C64A-25VQ	250 ns	5V ± 10%	-40°C to + 85°C	FDIP-28
TS27C64A-30VQ	300 ns	5V ± 10%	-40°C to + 85°C	FDIP-28

PACKAGE MECHANICAL DATA

Figure 8 : 28-PIN CERAMIC DIP BULL'S EYE



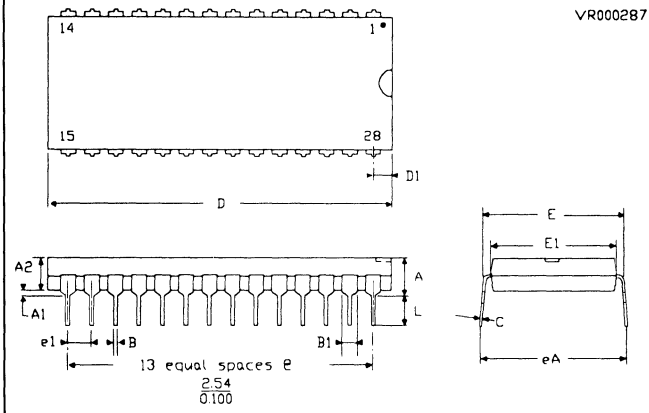
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-20CP	200 ns	5V ± 10%	0°C to + 70°C	PDIP28
TS27C64A-25CP	250 ns	5V ± 10%	0°C to + 70°C	PDIP28
TS27C64A-20VP	200 ns	5V ± 10%	-40°C to + 85°C	PDIP28
TS27C64A-25VP	250 ns	5V ± 10%	-40°C to + 85°C	PDIP28
TS27C64A-35TP(1)	350 ns	5V ± 10%	-40°C to + 105°C	PDIP28
TS27C64A-20CFN	200 ns	5V ± 10%	0°C to + 70°C	PLCC32
TS27C64A-25CFN	250 ns	5V ± 10%	0°C to + 70°C	PLCC32
TS27C64A-20VFN	200 ns	5V ± 10%	-40°C to + 85°C	PLCC32
TS27C64A-25VFN	250 ns	5V ± 10%	-40°C to + 85°C	PLCC32

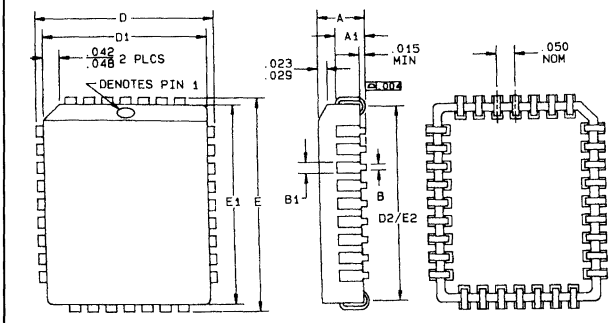
NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.
(1) Specification available upon request.

PACKAGE MECHANICAL DATA - OTP ROM
Figure 9 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	

Figure 10 : PLCC32 32-LEAD PLASTIC LEADED CHIP CARRIER

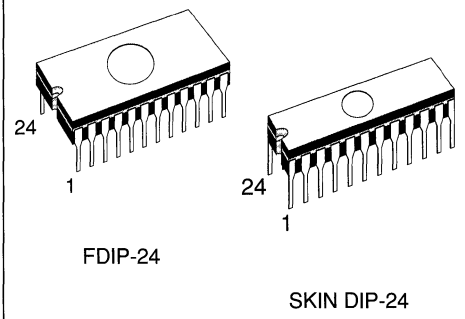


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04		3.55	.120		.140
A1	1.96		2.41	.078		.095
B	0.33		0.53	.013		.021
B1	0.66		0.81	.026		.032
D	12.31		12.57	.485		.495
D1	11.35		11.50	.447		.453
D2	9.90		10.92	.390		.430
E	14.85		15.11	.585		.595
E1	13.89		14.04	.547		.553
E2	12.44		13.46	.490		.530

64K (8K x 8) CMOS UV EPROM

PRELIMINARY DATA

- ULTRA FAST ACCESS TIME : 35, 45, 55 ns.
- A REPROGRAMMABLE DEVICE FOR DIRECT REPLACEMENT OF BIPOLAR PROM.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 60 mA Max
  - Standby current 30 mA Max
- PROGRAMMING VOLTAGE 12.50V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.



FDIP-24

SKIN DIP-24

(Ordering Information at the end of the datasheet)

DESCRIPTION

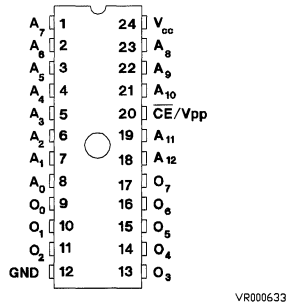
The M27HC641 is an ultra high speed 65,536 (organized 8,192 x 8) bit ultraviolet erasable and reprogrammable CMOS EPROM.

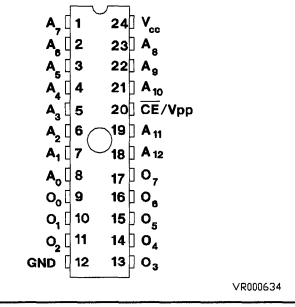
Access time value and pin out make it ideal for Bipolar PROM replacement, with the advantage of lower power consumption and reprogrammability.

It is housed in a 24 pin Ceramic Frit Seal Window package, either 300 or 600 mils wide.

The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1 : Pin Connection

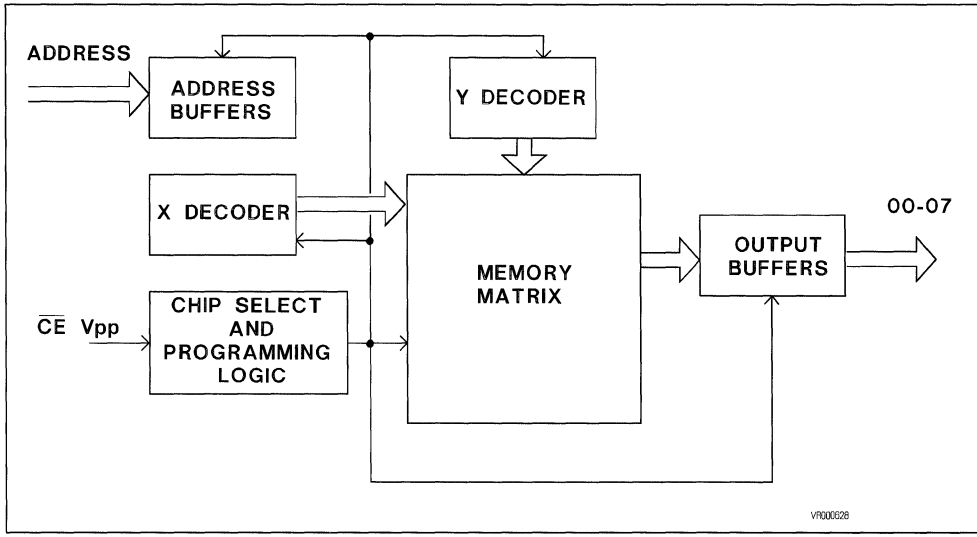




PIN FUNCTIONS

A0-A10	ADDRESS INPUT
O0-O7	DATA INPUT/OUTPUT
$\overline{CE}$ / V_{PP}	CHIP SELECT / V_{PP}
V_{CC}	+ 5V POWER SUPPLY
GND	GROUND

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
V_{A9}	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
T_{bias}	Temperature range under bias	-10 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$ / V_{PP}	A9	OUTPUT
READ / PROGRAM VERIFY	L	X	D_{OUT}
PROGRAM	V_{PP}	X	D_{IN}
STANDBY / PROGRAM INHIBIT	H	X	HIGH Z
ELECTRONIC SIGNATURE	L	V_H	CODE

NOTE : X = Don't care ; V_H = 12V ± 0.5V ; H = High ; L = Low. V_{PP} = 12.5V (see programming section).

READ OPERATION
DC AND AC CONDITIONS

SELECTION CODE	F1	F6
Operating Temperature Range	0°C to +70°C	-40°C to +85°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**35XF1, 45XF1, 55XF1**	**45F1, 55F1**
V_{CC} Power Supply (1)	5V ± 5%	5V ± 10%

NOTE : "F" stands for ceramic package.

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input leakage current	V_{IN} = 0 V to V_{CC}	- 10	10	uA
I_{LO}	Output leakage current	V_{IN} = 0 V to V_{CC}	- 10	10	uA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA (F = 20 MHz)		60	mA
I_{CC2}	V_{CC} Standby Current-TTL	$\overline{CE}$ = V_{IH}		20	mA
V_{IL}	Input Low Voltage		- 0.3	0.5	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 16.0 mA		0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4		V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27HC641						Unit
			-35		-45		-55		
			Min	Max	Min	Max	Min	Max	
T_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL}		35		45		55	ns
T_{CE}	$\overline{CE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		25	ns
T_{DF} (2)	$\overline{CE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	20	0	25	0	25	ns
T_{OH}	Output Hold from Address or $\overline{CE}$	$\overline{CE}$ = V_{IL}	0		0		0		

CAPACITANCE(3)

(TA = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Input Levels	:	0V and 3V
Reference Levels	:	1.5V

AC TESTING LOAD CIRCUIT

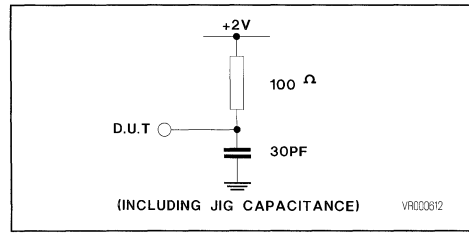
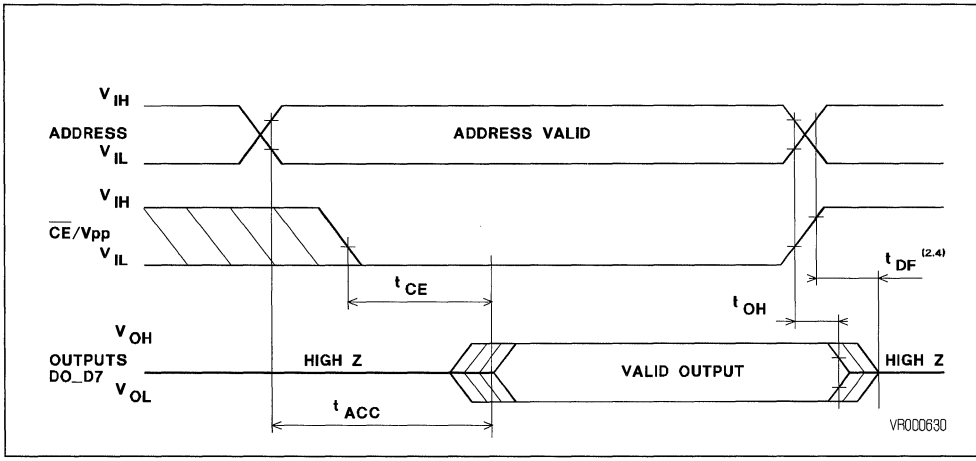


Figure 3 : AC Waveforms



DEVICE OPERATION

The modes of operation of the M27HC641 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp and 12V on A9 for Electronic Signature.

READ MODE

The M27HC641 has one control function which must be logically active in order to obtain data at the outputs : Chip Enable ($\overline{CE}/V_{PP}$), active low. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}).

STANDBY MODE

The M27HC641 has a standby mode which reduces the maximum active current from 60 mA to 20 mA. The M27HC641 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/V_{PP}$ input. When in the standby mode, the outputs are in a high impedance state.

PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M27HC641.

When delivered (and after each erasure for UV EPROM), all bits of the M27HC641 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27HC641 is in the programming mode when $\overline{CE}/V_{PP}$ input is at 12.50V. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.00V

FAST PROGRAMMING ALGORITHM

Fast programming algorithm rapidly programs M27HC641 using an efficient and reliable method. A flowchart is shown at the end of data sheet.

Two different pulses are used : Initial (1 ms) and overprogramming (3 X ms). A maximum of 25 "initial" pulses is allowed. A verify is done after each pulse, until a correct verify occurs. An overprogramming pulse is then applied, the lengh of which is 3 X ms, where X is the number of initial pulses reached. The entire sequence of programming and verification is done with V_{CC} at 6.0V (programming pulses with V_{PP} at 12.5V).

PROGRAM INHIBIT

Programming of multiple M27HC641s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel M27HC641 may be common. A 12.5V level pulse applied to a M27HC641's $\overline{CE}/V_{pp}$ input will program that M27HC641. A TTL high level $\overline{CE}$ input inhibits the other M27HC641s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ at V_{IL} and V_{CC} at 5.00V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27HC641. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27HC641. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27HC641, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27HC641 is such that erasure begins when the cells are exposed to light with a wavelength shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27HC641 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27HC641 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27HC641 window to prevent unintentional erasure. The recommended erasure procedure for the M27HC641 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm2 power rating. The M27HC641 should be placed within 2.5 cm (1inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	0	0	0	1	01

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$ = VIL ; A1 to A8 = A10 = V_{IL}

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC} = 6.00V ± 0.25V, V_{PP} = 12.50 ± 0.25V) (1)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
V_{IL}	Input Low Voltage		-0.1	0.5	V
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = - 400 uA	2.4		V
I_{CC2}	V_{CC} Active Current			60	mA
I_{PP2}	V_{PP} Active Current	$\overline{CE}$ = V_{IL}		60	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Chip Enable Output Float Delay		0	130	µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width		0.95	1.05	ms
t_{OPW}	Overprogram Pulse Width		2.85	78.75	ms
t_{CE}	Data Valid from $\overline{CE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 4 : Programming Flowchart

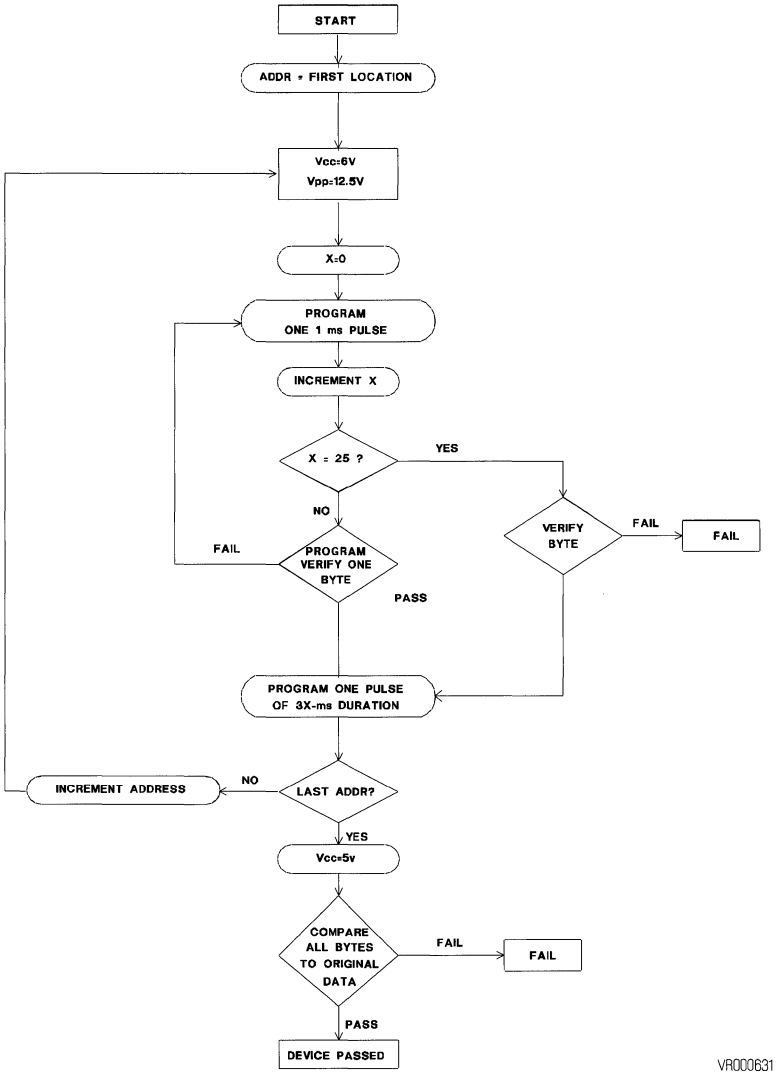
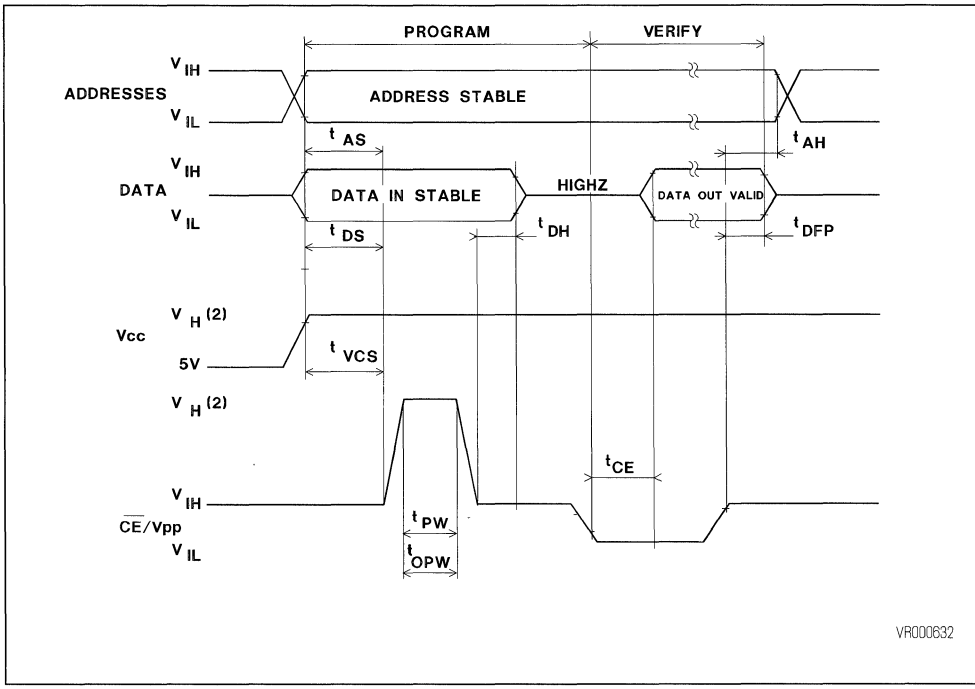


Figure 5 : Programming Waveforms



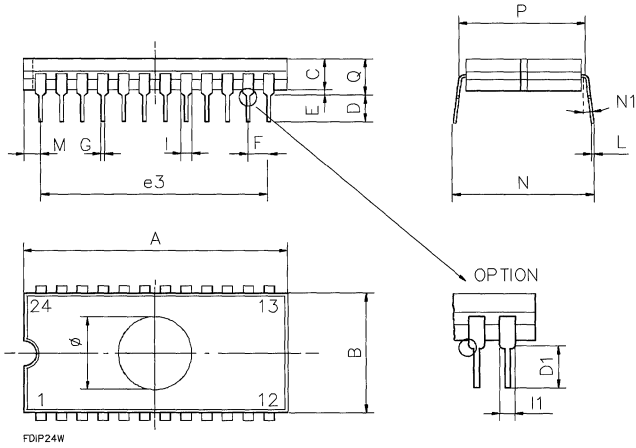
NOTES : 1. t_{DFP} is a characteristic of the device but must be accommodated by the programmer.
2. V_{CC} = 6.0 ± 0.25V, $\overline{CE}$ / V_{PP} = 12.5 ± 0. V for fast programming algorithm.

ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27HC641-45XF1	45 ns	5V ± 5%	0°C to +70°C	FDIP24-W 600 mils
M27HC641-35XFS1	35 ns	5V ± 5%	0°C to +70°C	FDIP24-W 300 mils
M27HC641-45XFS1	45 ns	5V ± 5%	0°C to +70°C	FDIP24-W 300 mils
M27HC641-45FS1	45 ns	5V ± 10%	0°C to +70°C	FDIP24-W 300 mils
M27HC641-55XFS1	55 ns	5V ± 5%	0°C to +70°C	FDIP24-W 300 mils

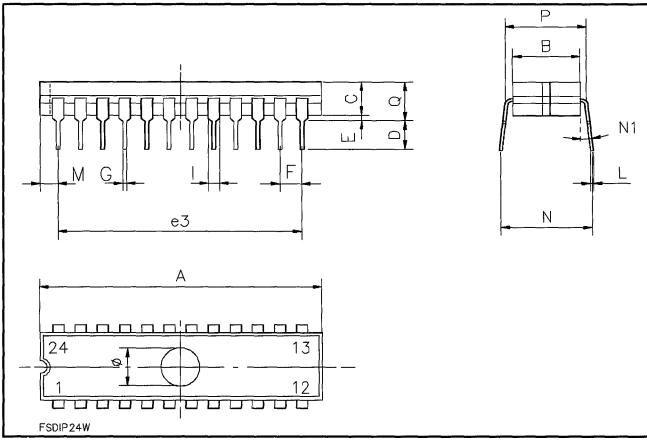
PACKAGE MECHANICAL DATA - UV EPROM

Figure 6 : 24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.00			1.259
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.200
D	3.00			.118		
D1	3.40			.134		
E	0.50		1.78	.020		.070
e3		27.94			1.10	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.022
I	1.17		1.42	.046		.056
I1	1.27		1.52	.050		.060
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

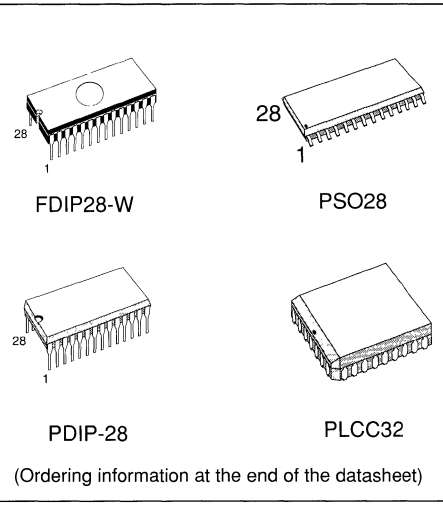
Figure 7 : 24-PIN CERAMIC DIP BULL'S EYE - SKINNY - 300 MILS



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.00			1.259
B			7.80			.307
C						
D	3.40			.134		
E	0.50		1.78	.020		.070
e3		27.94			1.10	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.022
I	1.27		1.52	.050		.060
L	0.22		0.31	.009		.012
M	0.51		1.27	.020		.050
M						
N1	0°		10°	0°		10°
P	7.90		8.13	.311		0.320
Q			5.71			.225
Ø	4.24		4.39	.167		.173

256K (32K x 8) CMOS UV EPROM - OTPROM

- VERY FAST ACCESS TIME : 100 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 30 mA
  - Stand by current 200 µA
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 3 SECONDS (PRESTO II ALGORITHM).



(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C256B is a high speed 262,144 bit ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

It is housed in a 28 pin Ceramic Frit Seal Window package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIL, SO or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O0-O7	DATA INPUT/OUTPUT
V_{PP}	PROGRAMMING VOLTAGE
V_{CC}	+5V POWER SUPPLY
GND	GROUND
DU	DON'T USE
NC	NON CONNECTED

Figure 1. Pin Connection

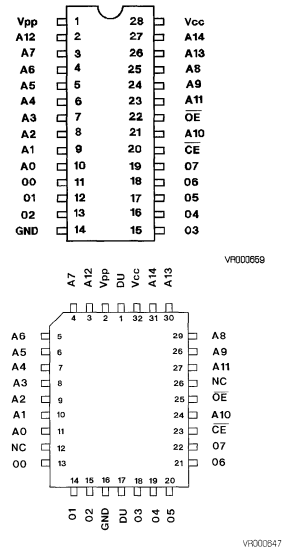
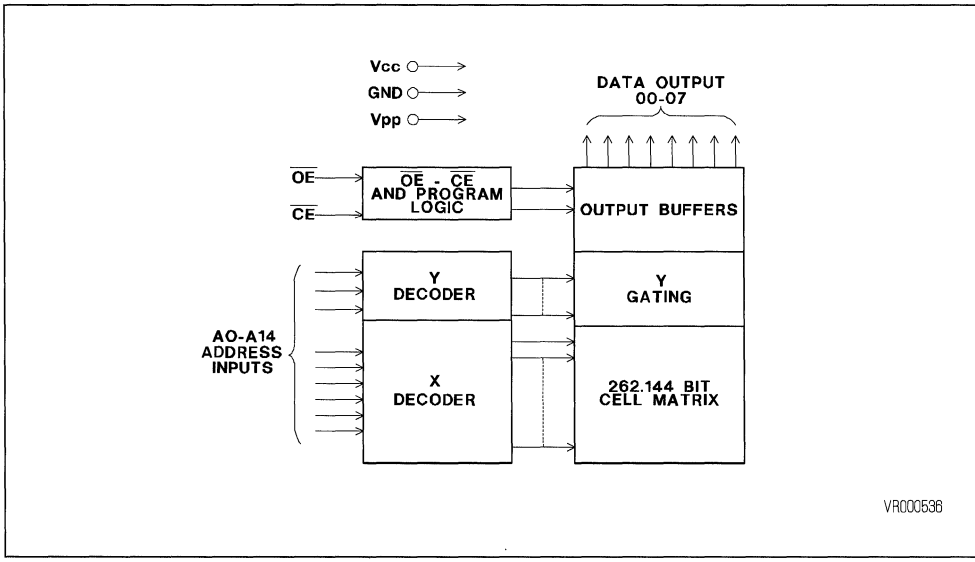


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltage with respect to Ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to Ground	-0.6 to +14.0	V
VA9	Voltage on A9 with respect to Ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to Ground	-0.6 to +7.0	V
T_{BIAS}	Temperature range under bias	-50 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS				
	$\overline{CE}$	OE	A9	V_{PP}	OUTPUT
READ	L	L	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	X	V_{CC}	HIGH Z
STANDBY	H	X	X	V_{CC}	HIGH Z
PROGRAM	L	H	X	V_{PP}	D_{IN}
PROGRAM VERIFY	H	L	X	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	H	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	V_{CC}	CODE

NOTE : X = Don't care ; V_H = 12V ± 0.5V; H = High ; L = Low

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to +70°C	-40°C to +85°C	-40°C to +105°C	-40°C to +125°C
SELECTION CODE (Example for O°C to 70°C Oper. Temp. Range)	**-10XF1, 12XF1, 15XF1, 20XF1, 25XF1**		**10F1, 12F1, 15F1, 20F1, 25F1**	
V_{CC}	5 V ± 5 %		5 V ± 10 %	

NOTE: "F" stands for ceramics package. Plastic packaged device code features B,M or C

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	VCC Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT}= 0 mA (F = 5MHz)		30	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3} (4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2 V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		100	µA
V_{IL}	Input Low Voltage		-0.3	+ 0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC} - 0.7		V

AC CHARACTERISTICS

Symbol	Parameter	Test condition	27C256B										Unit
			-10		-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$= $\overline{OE}$=V_{IL}		100		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		100		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		40		50		60		70		100	ns
t_{DF} (2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	30	0	40	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Address	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE (3)

(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES :
1. V_{CC} Must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From Date Code 9040.

READ OPERATION

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Levels :	
Input Pulse Levels	:	0.45 to 2.4V	Inputs : 0.8 and 2V - Outputs : 0.8 and 2V	

Figure 3 : AC TESTING INPUT/OUTPUT

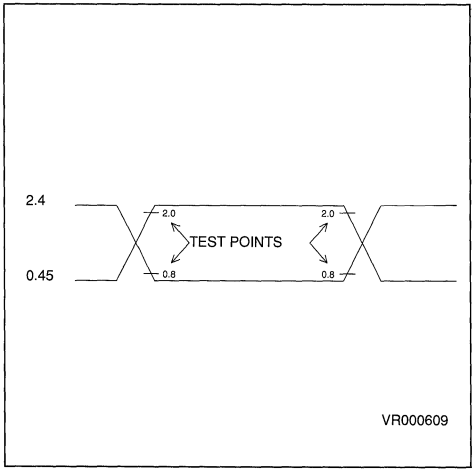


Figure 4 : AC TESTING LOAD CIRCUIT

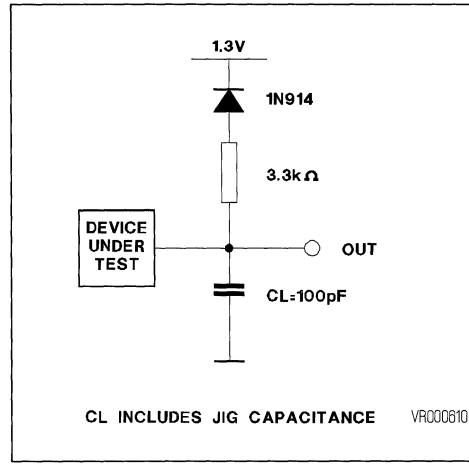
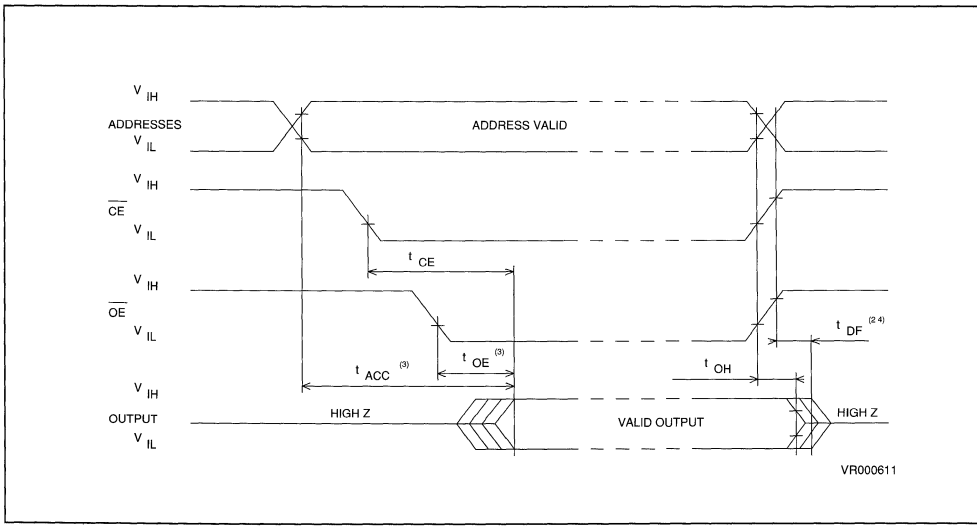


Figure 5 : AC WAVEFORMS



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operation of the M27C256B are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27C256B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C256B has a standby mode which reduces the active current from 30 mA to 0.2 mA (from date code 9040). The M27C256B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices.

The supply current, Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 µF ceramic capacitor be used on every device between Vcc and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M27C256B.

When delivered (and after each erasure for UV EPROM), all bits of the M27C256B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C256B is in the programming mode when V_{PP} input is at 12.75 V, and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of less than 3 seconds. Programming with PRESTO II involves the application of a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C256Bs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C256B may be common. A TTL low level pulse applied to a M27C256B's $\overline{CE}$ input, with V_{PP} at 12.75 V, will program that M27C256B. A high level $\overline{CE}$ input inhibits the other M27C256Bs from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C256B. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C256B, with V_{CC} = V_{PP} = 5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C256B, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C256B is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C256B in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C256B is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C256B window to prevent unintentional erasure. The recommended erasure procedure for the M27C256B is exposure to short wave ultraviolet light which has wavelength 2537Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C256B should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	1	0	1	8D

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$ = $\overline{OE}$ = V_{IL} , A1 - A8, A10 - A14 = V_{IL} ; V_{PP} = V_{CC} = 5V

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V.

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

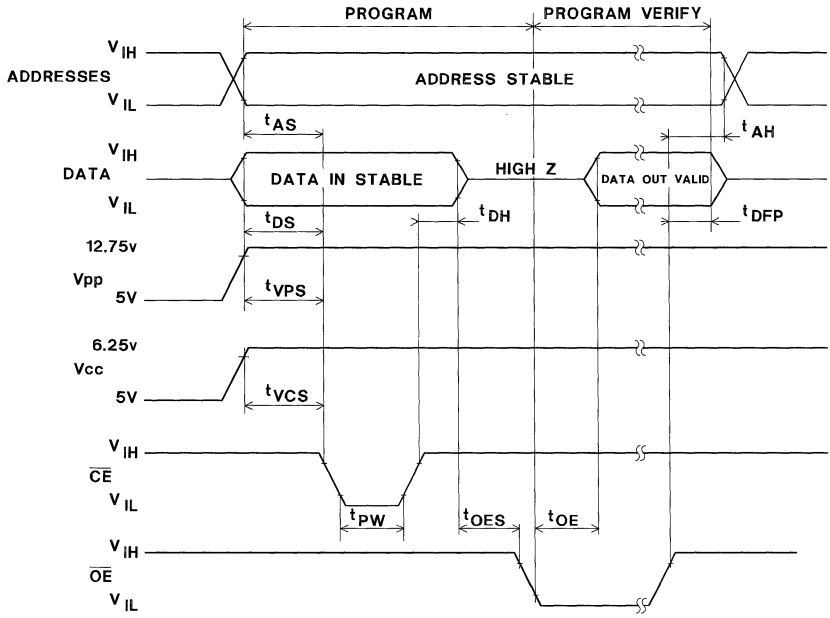
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

Figure 6 : Programming Waveforms



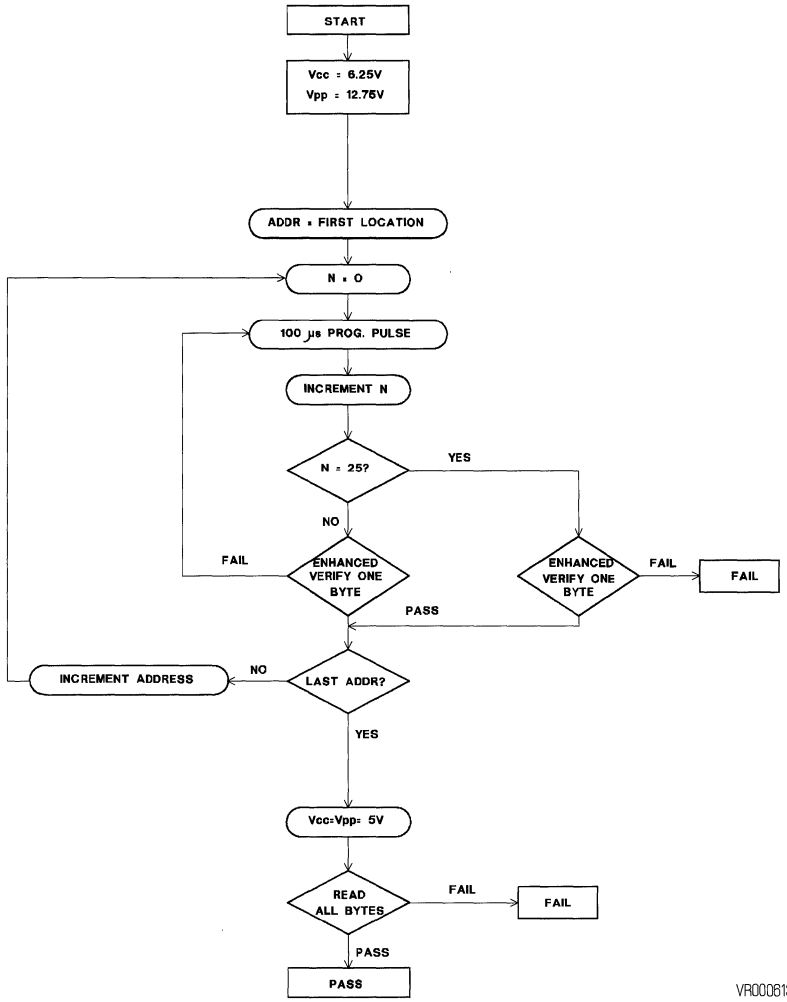
NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.

2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.

3. When programming the M27C256B a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm flow Chart



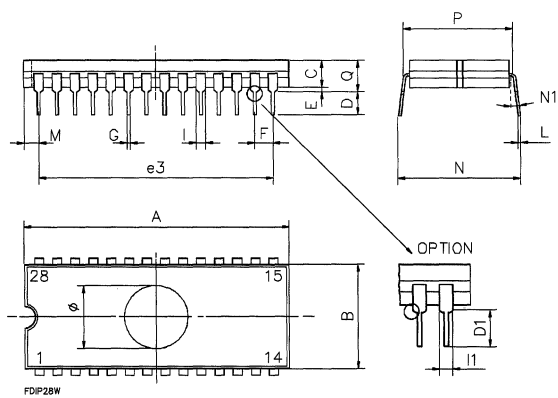
ORDERING INFORMATION - UV EPROM

Part Number	Access time	Supply Voltage	Temp. Range	Package
M27C256B-10XF1	100 ns	5V ± 5%	0°C to + 70°C	FDIP28-W
M27C256B-12XF1	120 ns	5V ± 5%	0°C to + 70°C	FDIP28-W
M27C256B-15XF1	150 ns	5V ± 5%	0°C to + 70°C	FDIP28-W
M27C256B-20XF1	200 ns	5V ± 5%	0°C to + 70°C	FDIP28-W
M27C256B-10F1	100 ns	5V ± 10%	0°C to + 70°C	FDIP28-W
M27C256B-12F1	120 ns	5V ± 10%	0°C to + 70°C	FDIP28-W
M27C256B-15F1	150 ns	5V ± 10%	0°C to + 70°C	FDIP28-W
M27C256B-20F1	200 ns	5V ± 10%	0°C to + 70°C	FDIP28-W
M27C256B-15XF6	150 ns	5V ± 5%	-40°C to + 85°C	FDIP28-W
M27C256B-15F6	150 ns	5V ± 10%	-40°C to + 85°C	FDIP28-W
M27C256B-20XF7	200 ns	5V ± 5%	-40°C to + 105°C	FDIP28-W
M27C256B-20XF3	200 ns	5V ± 5%	-40°C to + 105°C	FDIP28-W

NOTE : Consult your nearest SGS THOMSON sales office for availability or other combination.

PACKAGE MECHANICAL DATA - UV EPROM

Figure 8 : 28-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e 3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

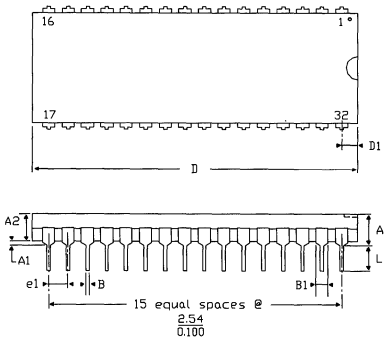
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C256B-12XB1	120 ns	5V ± 5%	0°C to + 70°C	DIP28
M27C256B-15XB1	150 ns	5V ± 5%	0°C to + 70°C	DIP28
M27C256B-15B1	150 ns	5V ± 10%	0°C to + 70°C	DIP28
M27C256B-15XB6	150 ns	5V ± 5%	-40°C to + 85°C	DIP28
M27C256B-15B6	150 ns	5V ± 10%	-40°C to + 85°C	DIP28
M27C256B-12XC1	120 ns	5V ± 5%	0°C to + 70°C	PLCC32
M27C256B-15XC1	150 ns	5V ± 5%	0°C to + 70°C	PLCC32
M27C256B-15C1	150 ns	5V ± 10%	0°C to + 70°C	PLCC32
M27C256B-15XC6	150 ns	5V ± 5%	-40°C to + 85°C	PLCC32
M27C256B-15C6	150 ns	5V ± 10%	-40°C to + 85°C	PLCC32
M27C256B-12XM1	120 ns	5V ± 5%	0°C to + 70°C	PSO28
M27C256B-15XM1	150 ns	5V ± 5%	0°C to + 70°C	PSO28
M27C256B-15M1	150 ns	5V ± 10%	0°C to + 70°C	PSO28
M27C256B-15XM6	150 ns	5V ± 5%	-40°C to + 85°C	PSO28
M27C256B-15M6	150 ns	5V ± 10%	-40°C to + 85°C	PSO28

NOTE : consult your nearest SGS THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA - OTP ROM

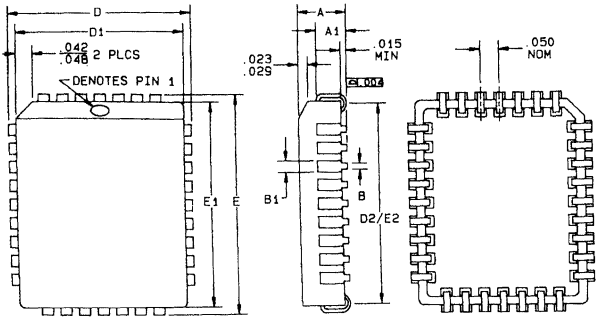
Figure 9 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.60			.025	
B		0.45			.018	
b1	0.23		0.31	.008		.012
b2		1.27			.060	
C						
D			37.34			1.470
E	15.20		16.08	.508		.057
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.556
I		4.45			.175	
L		3.30			.130	
K1						
K2						

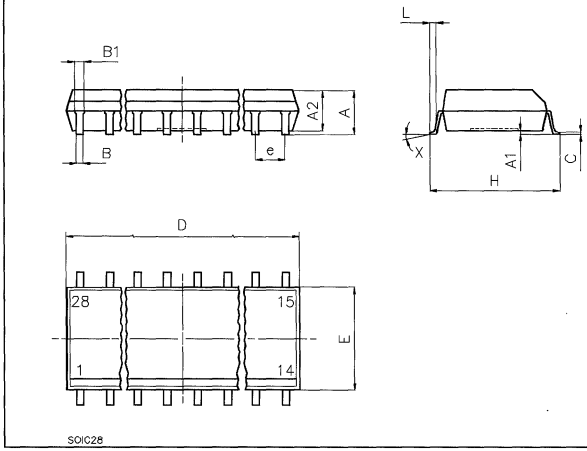
PACKAGE MECHANICAL DATA - OTP ROM (Continued)

Figure 10 : PLCC32-32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04		3.55	.120		.140
A1	1.96		2.41	.078		.095
B	0.33		0.53	.013		.021
B1	0.66		0.81	.026		.032
D	12.31		12.57	.485		.495
D1	11.35		11.50	.447		.453
D2	9.90		10.92	.390		.430
E	14.85		15.11	.585		.595
E1	13.89		14.04	.547		.553
E2	12.44		13.46	.490		.530

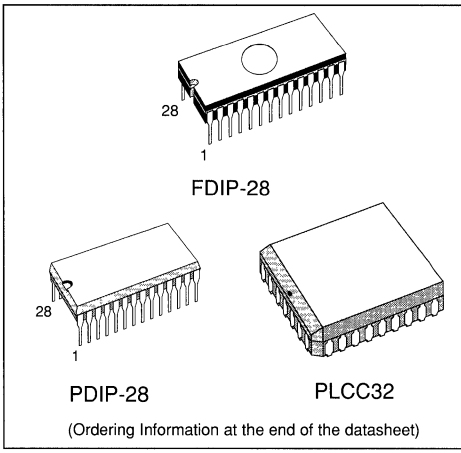
Figure 11 : PSO28-28 LEAD PLASTIC SMALL OUTLINE PACKAGE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.05			.120
A1	0.05		0.35	.002		.013
A2	2.34		2.69	.092		.105
B	0.35		0.51	.013		.020
B1	0.35		0.61	.013		.024
C	0.15		0.32	.006		.012
D	17.71		18.49	.697		.727
E	8.23		8.89	.324		.350
e		1.27			.050	
H	11.51		12.70	.453		.500
L	0.41		1.27	.016		.050
X		8°				8°

LATCHED 256K (32Kx8) CMOS UV EPROM - OTP ROM

- INTEGRATED ADDRESS LATCH.
- VERY FAST ACCESS TIME : 100 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Active Current 30mA
  - Standby Current 200µA
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIME OF AROUND 3 SECONDS (PRESTO II ALGORITHM).



(Ordering Information at the end of the datasheet)

DESCRIPTION

The M87C257 is a high speed 262,144 bit UV erasable and electrically reprogrammable EPROM. The M87C257 incorporates latches on all addresses input to minimize chip count, reduce cost, and simplify the design of multiplexed bus systems.

The M87C257 is housed in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIL or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A14	ADDRESS INPUTS
O0-O7	DATA INPUT/OUTPUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/V_{PP}	ADDRESS LATCH ENABLE/V_{PP}
NC	NON CONNECTED
V_{CC}	+ 5V POWER SUPLY
GND	GROUND
DU	DON'T USE

Figure 1 : Pin Connection

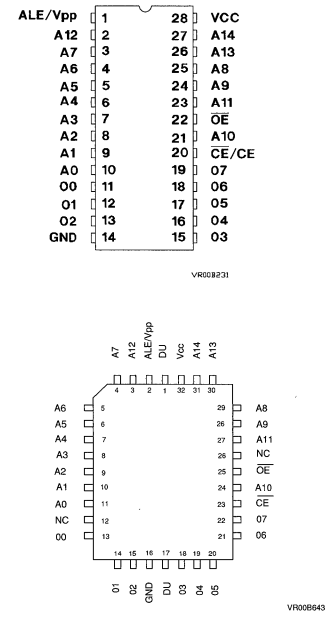
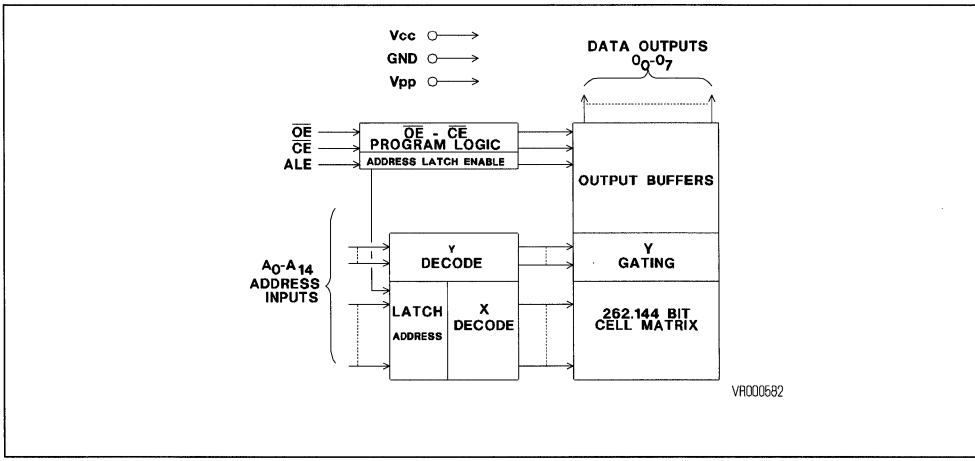


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltage with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
VA9	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
Tbias	Temperature range under bias	-50 to +125	°C
Tstg	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS				
	$\overline{CE}$	OE	A9	ALE/V_{PP}	OUTPUT
READ (LATCHED ADDRESS)	L	L	X	L	D_{OUT}
READ (CURRENT ADDRESS)	L	L	X	H	D_{OUT}
OUTPUT DISABLE	L	H	X	X	HIGH Z
STANDBY	H	X	X	X	HIGH Z
HIGH SPEED PROGRAMMING	L	H	X	V_{PP}	D_{IN}
PROGRAM VERIFY	H	L	X	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	H	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	X	CODE

NOTE : X Don't care ; V_H = 12V ± 0.5V; H = High ; L = Low

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**10XF1, 12XF1, 15XF1, 20XF1**		**10F1, 12F1, 15F1, 20F1**	
V_{CC} Power Supply (1)	5V ± 5%		5V ± 10%	

NOTE : "F" stands for ceramic package. Plastic packaged device code features B, M or C (see ordering information).

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} IOUT= 0 mA (F = 5MHz)		30	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH} - Stable Inputs		1	mA
I_{CC3}(4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2V - Stable Inputs		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC} - 0.8		V

AC CHARACTERISTICS

Symbol	Parameter	Test condition	87C257								Unit
			-10		-12		-15		-20		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address Output Delay	$\overline{CE}$= $\overline{OE}$=V_{IL}		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		100		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		40		50		60		70	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	30	0	40	0	40	0	40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		0		ns
t_{LL}	Latch deselect Width		35		35		35		50		ns
t_{AL}	Add to latch setup		7		7		7		15		ns
t_{LA}	Add Hold from latch		20		20		20		30		ns
t_{LOE}	ALE to Output Enable		20		20		20		30		ns

CAPACITANCE(3)

T_{AMB} = 25°C, f = 1 MHz

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From Date Code 9040.

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs 0.8 and 2V - Outputs 0.8 and 2V

AC TEST CONDITIONS

Figure 3 : AC Testing Input/Output Waveform

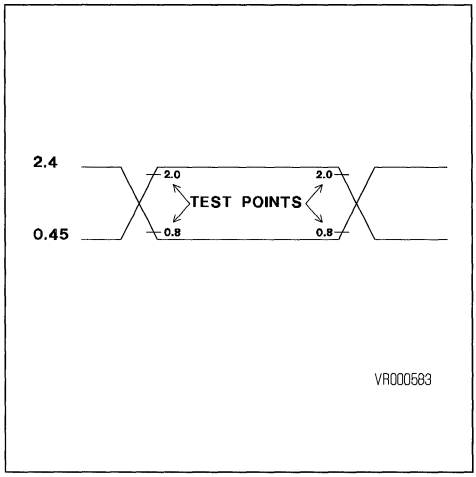


Figure 4 : AC Testing Load Circuit

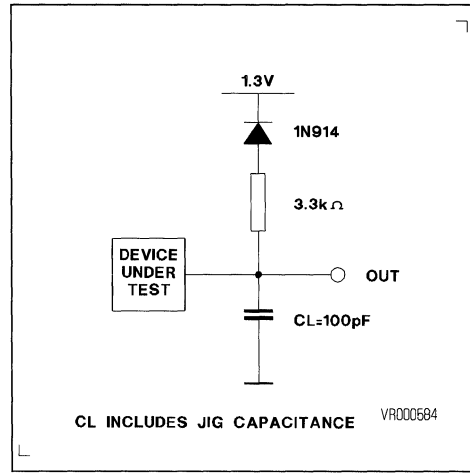
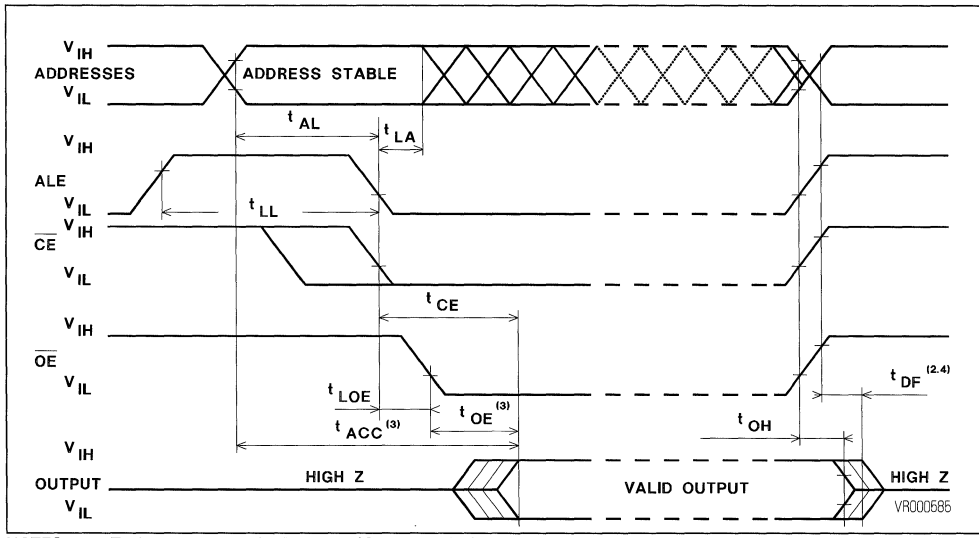


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ OPERATION

DEVICE OPERATION

The modes of operation of the M87C257 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for 12V on A9 for Electronic Signature.

READ MODE

The M87C257 has two control functions both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable (ALE=V_{IH}) or latched (ALE=V_{IL}), the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.
The M87C257 reduces the hardware interface in multiplexed address-data bus systems. Figure 6 shows a low power, small board space, minimal chip M87C257/microcontroller design. The processors multiplexed bus (AD0-7) is tied to the M87C257's address and data pins. No separate address latch is needed because the M87C257 latches all address inputs when ALE is low.

STANDBY MODE

The M87C257 has a standby mode which reduces the active current from 30mA to 0.2mA (from date code 9040). The M87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

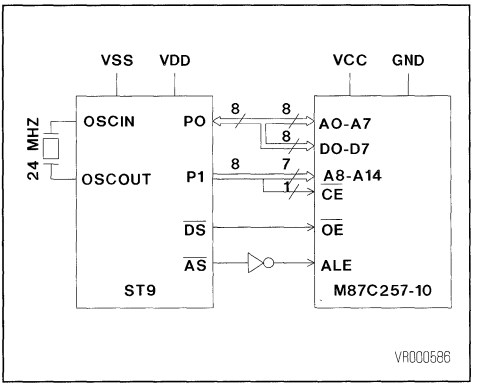
For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point.
The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Figure 6 : M87C257 / ST9 Microcontroller system lay out



PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M87C257.

When delivered, (and after each erasure for UV EPROM), all bits of the M87C257 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by exposure ultraviolet light. The M87C257 is in the programming mode when V_{PP} input is at 12.75V and $\overline{CE}$ is at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

VERY FAST AND RELIABLE PROGRAMMING ALGORITHM = PRESTO II

PRESTO II programming algorithm, available for the M87C257 is an enhancement of the PRESTO algorithm used for the M27512.

During programming and verify operation a MARGIN MODE™ circuit is automatically activated. It provides adequate margin for the threshold voltage of programmed cells, thus the writing margin is independent from V_{CC} in verify mode and an overprogram pulse is not necessary, thus reducing programming time down to a theoretical value of 3 seconds.

PROGRAM INHIBIT

Programming of multiple M87C257s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel M87C257 may be common. A TTL low level pulse applied to a M87C257s $\overline{CE}$ input, with V_{PP} at 12.75V will program that M87C257. A high level CE input inhibits the other M87C257s from being programmed.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M87C257. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M87C257 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. When $A9=V_H$, ALE need not be toggled to latch each identifier address. For the SGS-THOMSON M87C257, these two identifier bytes are given below, and can be read out on the outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristic of the M87C257 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M87C257 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M87C257 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M87C257 window to prevent unintentional erasure. The recommended erasure procedure for the M87C257 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M87C257 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	0	0	0	0	80

NOTE : A9 = 12V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$, A1 - A8, A10 - A14 = V_{IL} ; $V_{PP} = V_{CC} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.5V)

DC AND OPERATING CHARACTERISTICS

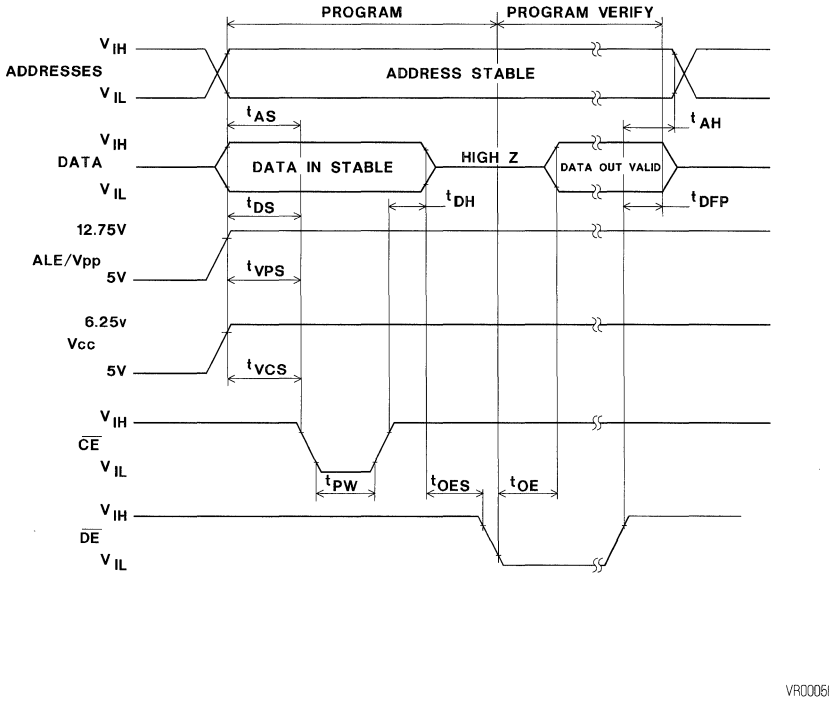
Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -1mA	V_{CC}-0.8		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	OE Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	µs
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from OE			100	ns

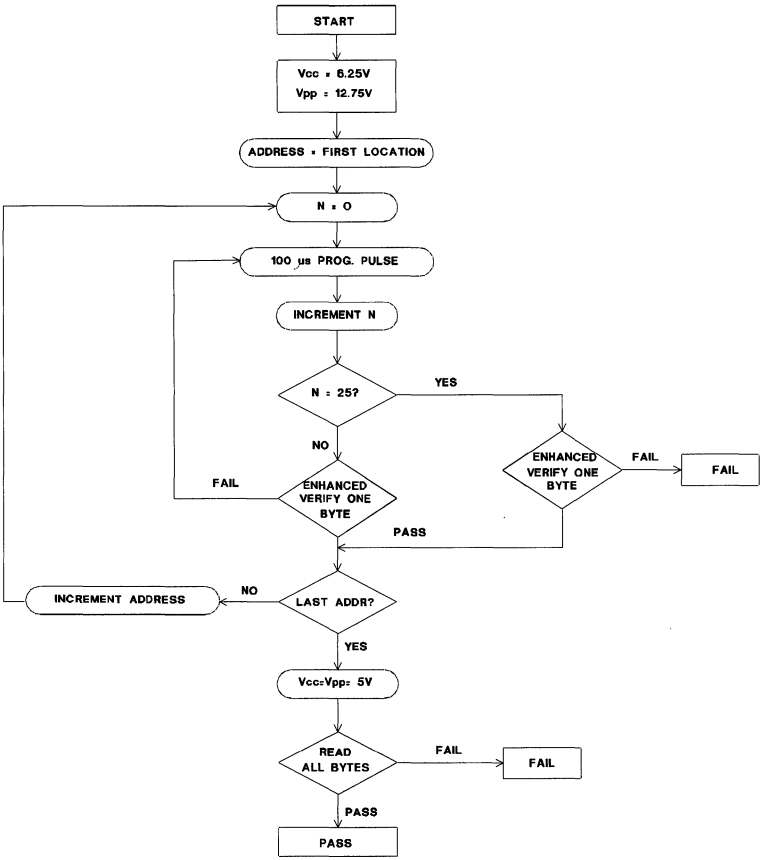
NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 7 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M87C257 a 0.1µF capacitor is required across V_{PP} and GROUND to supress spurious voltage transient which can damage the device.

Figure 8 : PRESTO II Programming Algorithm



VR000688

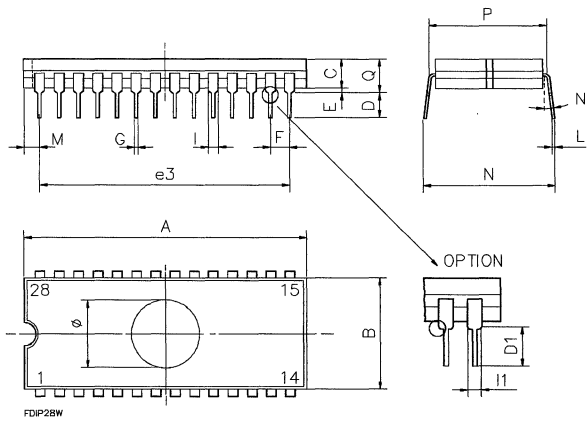
ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M87C257-10XF1	100 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-12XF1	120 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-15XF1	150 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-20XF1	200 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M87C257-10F1	100 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-12F1	120 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-15F1	150 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-20F1	200 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M87C257-15XF6	150 ns	5V ± 5%	-40°C to + 85°C	FDIP28-W
M87C257-15F6	150 ns	5V ± 10%	-40°C to + 85°C	FDIP28-W
M87C257-20XF7	200 ns	5V ± 5%	-40°C to + 105°C	FDIP28-W
M87C257-20XF3	200 ns	5V ± 5%	-40°C to + 125°C	FDIP28-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA - UV EPROM

Figure 9 : 28-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	.514		.526
C	3.90		5.08	.154		.199
D	3.00			.118		
E	0.50		1.78	.020		.070
e 3		33.02			1.300	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.027
I	1.17		1.42	.046		.056
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	6.86		7.36	.270		.290

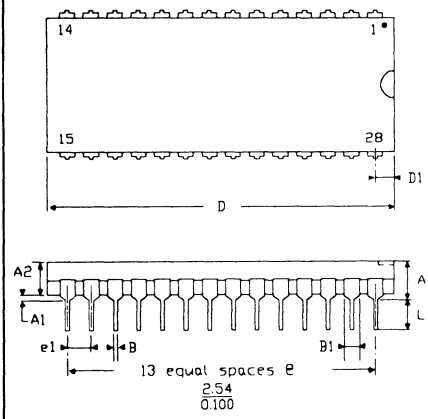
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M87C257-12XB1	120 ns	5V ± 5%	0°C to + 70°C	DIP28
M87C257-15XB1	150 ns	5V ± 5%	0°C to + 70°C	DIP28
M87C257-15B1	150 ns	5V ± 10%	0°C to + 70°C	DIP28
M87C257-15XB6	150 ns	5V ± 5%	-40°C to + 85°C	DIP28
M87C257-15B6	150 ns	5V ± 10%	-40°C to + 85°C	DIP28
M87C257-12XC1	120 ns	5V ± 5%	0°C to + 70°C	PLCC32
M87C257-15XC1	150 ns	5V ± 5%	0°C to + 70°C	PLCC32
M87C257-15C1	150 ns	5V ± 10%	0°C to + 70°C	PLCC32
M87C257-15XC6	150 ns	5V ± 5%	-40°C to + 85°C	PLCC32
M87C257-15C6	150 ns	5V ± 10%	-40°C to + 85°C	PLCC32

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

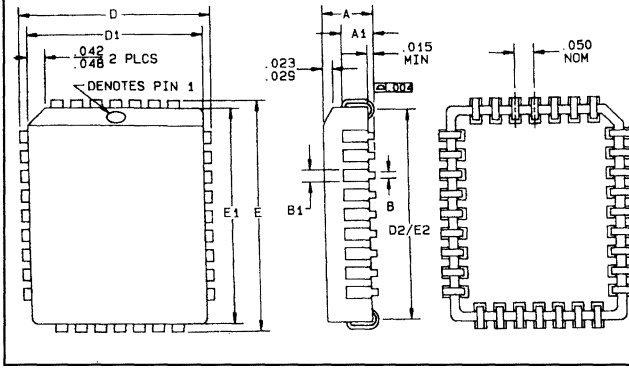
PACKAGE MECHANICAL DATA - OTP ROM

Figure 10 : 28-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

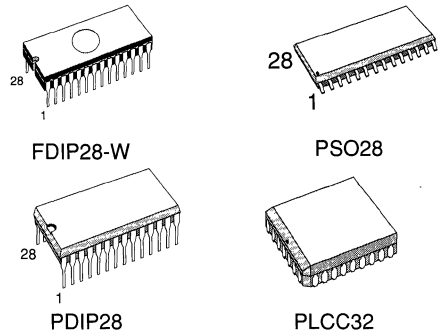
Figure 11 : PLCC32-32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04		3.55	.120		.140
A1	1.96		2.41	.078		.095
B	0.33		0.53	.013		.021
B1	0.66		0.81	.026		.032
D	12.31		12.57	.485		.495
D1	11.35		11.50	.447		.453
D2	9.90		10.92	.390		.430
E	14.85		15.11	.585		.595
E1	13.89		14.04	.547		.553
E2	12.44		13.46	.490		.530

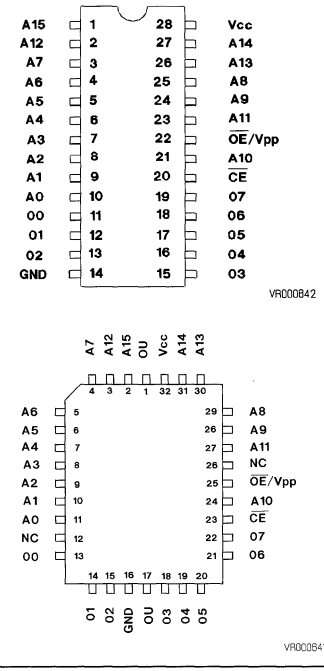
512K CMOS UV EPROM - OTP ROM

- VERY FAST ACCESS TIME : 100 ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 30mA
  - Stand by current 200µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 6 SECONDS (PRESTO IIB ALGORITHM).



(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection



DESCRIPTION

The M27C512 is a high speed 524,288 bit ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

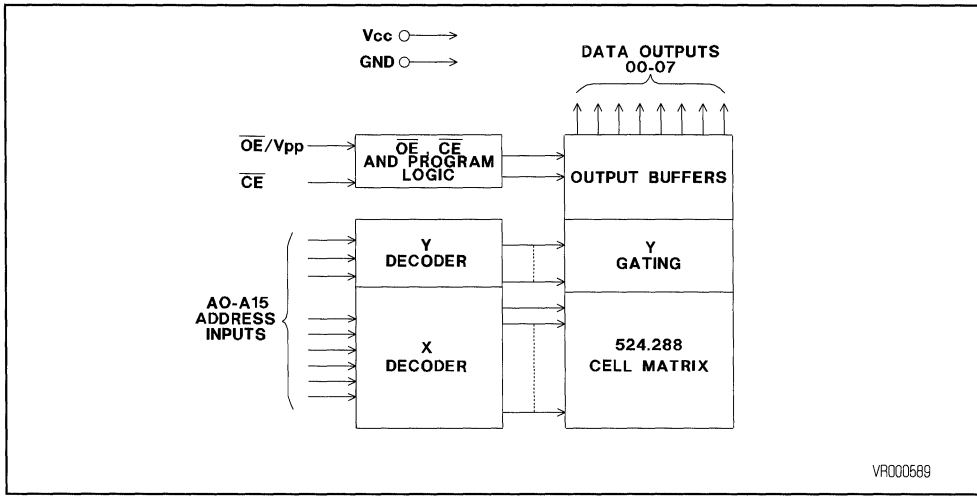
It is housed in a 28 pin Ceramic Frit Seal Window package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in plastic packages, either Plastic DIP, SO or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$ / V_{PP}	OUTPUT ENABLE / V_{PP}
O0-O7	DATA INPUT/OUTPUT
V_{CC}	+ 5V POWER SUPPLY
GND	GROUND
DU	DON'T USE
NC	NO CONNECTION

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
V_{A9}	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
T_{bias}	Temperature range under bias	-50 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$ / V_{PP}	A9	OUTPUT
READ	L	L	X	D_{OUT}
OUTPUT DISABLE	L	H	X	HIGH Z
STANDBY	H	X	X	HIGH Z
PROGRAM	L	V_{PP}	X	DIN
PROGRAM INHIBIT	H	V_{PP}	X	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	CODE

NOTE : X = Don't care ; V_H = 12V ± 0.5V ; H = High ; L = Low.

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**-10XF1, 12XF1, 15XF1, 20XF1, 25XF1**		**12F1,15F1,20F1, 25F1**	
V_{CC} Power Supply	5V ± 5%		5V ± 10%	

DC AND OPERATIONG CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I_{OUT}= 0 mA (F = 5MHz)		30	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3} (4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC}-0.7		V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C512										Unit
			-10		-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		100		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		100		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		40		50		60		70		100	ns
t_{DF} (2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	30	0	40	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Address	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE(3)

(T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From date code 9112.

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Reference Levels :	
Input Pulse Levels	:	0.45 to 2.4V	Inputs : 0.8 and 2V - Outputs : 0.8 and 2V	

Figure 3 : AC Testing Input/Output Waveform

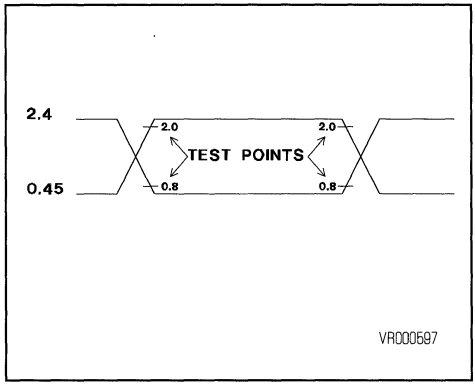


Figure 4 : AC Testing Load Circuit

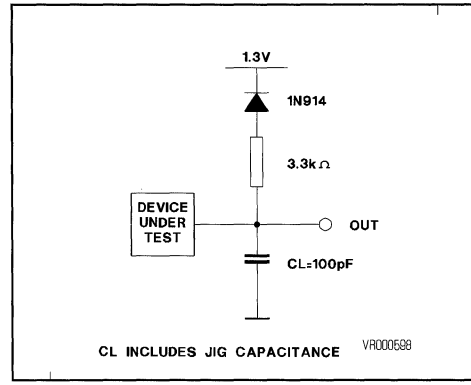
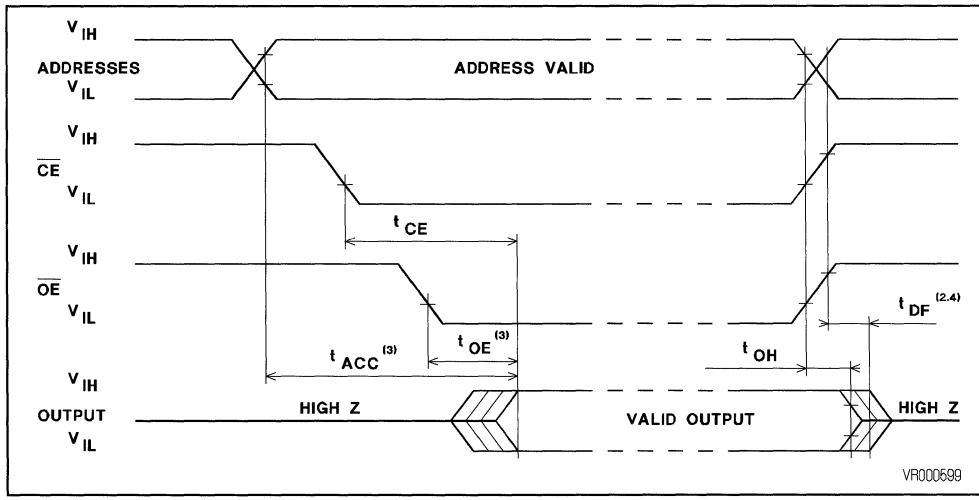


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for Electronic Signature.

READ MODE

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C512 has a standby mode which reduces the active current from 30mA to 0.2mA (from date code 9104). The M27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between Vcc and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and GND for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on OE/Vpp pin will permanently damage the M27C512.

When delivered (and after each erasure for UV EPROM), all bits of the M27C512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27C512 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB PROGRAMMING ALGORITHM

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 6 seconds. This can be achieved with SGS-THOMSON M27C512 due to several design innovations described in the M27C512 datasheet to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is pro-

grammed with enough margin. Then a sequence of 100 microsecond program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

PROGRAM INHIBIT

Programming of multiple M27C512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$/Vpp of the parallel M27C512 may be common. A TTL low level pulse applied to a M27C512's $\overline{CE}$ input, with $\overline{OE}/V_{PP}$ at 12.75V, will program that M27C512. A high level $\overline{CE}$ input inhibits the other M27C512s from being programmed. V_{CC} is specified to be 6.25V ± 0.25V.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL}. Data should be verified with t_{DV} after the following edge of $\overline{CE}$.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C512, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C512 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C512 window to prevent unintentional erasure. The recommended erasure procedure for the M27C512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

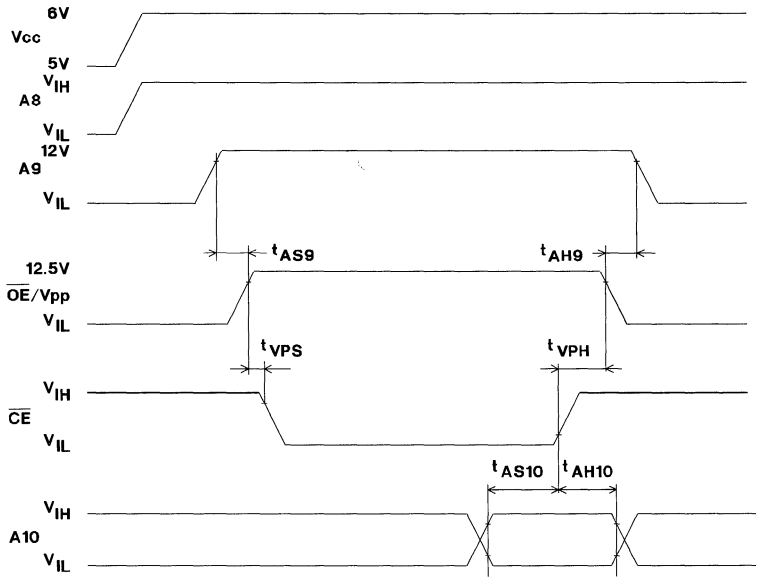
ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	1	1	1	1	0	1	3D

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL} ; A1 to A8 = A10 to A15 = V_{IL}

DEVICE OPERATION (Continued)

Figure 6 : MARGIN MODE Set and Reset Waveforms



NOTES: 1. Other addresses are don't care.
2. Set MARGIN MODE A10 = V_{IH}, Reset MARGIN MODE A10 = V_{IL}.

MARGIN MODE AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
t_{AS10}	A10 Setup Time		1		µs
t_{AH10}	A10 Hold Time		1		µs
t_{VPH}	V_{PP} Hold Time		2		µs
t_{VPS}	V_{PP} Setup Time		2		µs
t_{AS9}	A9 Setup Time		2		µs
t_{AH9}	A9 Hold Time		2		µs

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC} [1] = 6.25V ± 0.25V, V_{PP} [1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

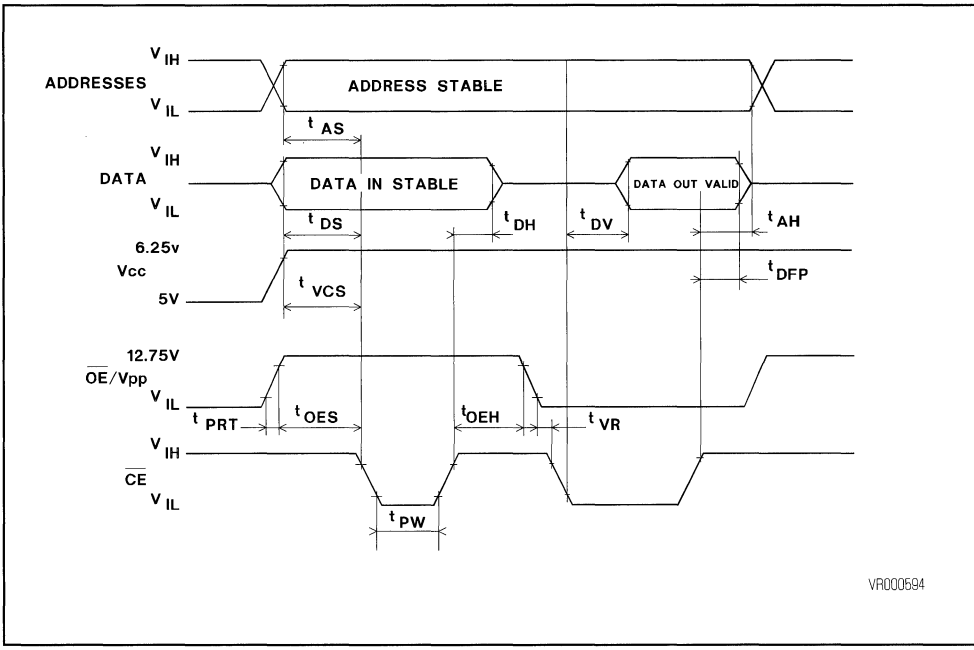
Symbol	Parameter	Test Condition (see Note 1)	Values		Unit
			Min	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = - 400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see Note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP} [2]	Chip Enable Output Float Delay		0	130	ns
t_{VCS}	V_{CC} Setup Time		0		µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width		95	105	µs
t_{DV}	Data Valid from $\overline{CE}$			1	ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

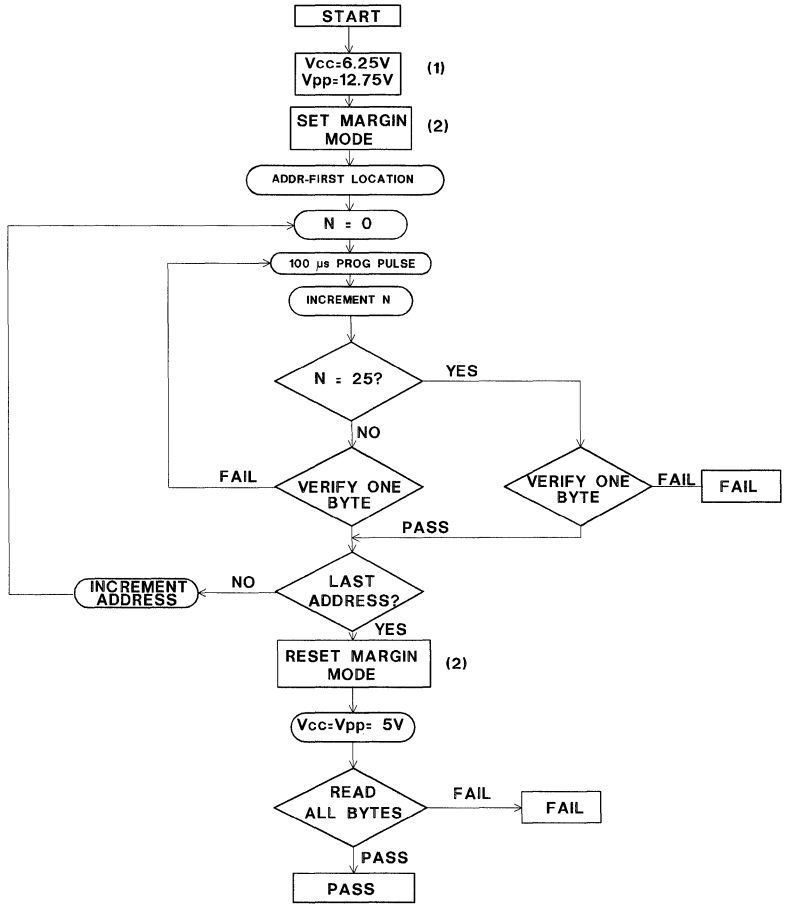
NOTES : 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 7 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Figure 8 : PRESTO IIB Programming Algorithm Flow Chart



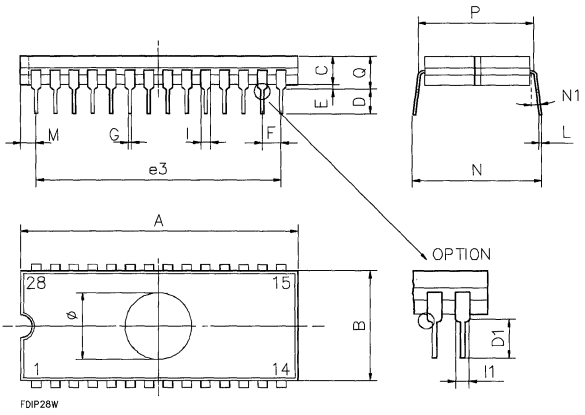
ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C512-10XF1	100 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-12XF1	120 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-15XF1	150 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-20XF1	200 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-25XF1	250 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-12F1	120 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-15F1	150 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-20F1	200 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-25F1	250 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-15XF6	150 ns	5V ± 5%	-40°C to +85°C	FDIP28-W
M27C512-15XF7	150 ns	5V ± 5%	-40°C to +105°C	FDIP28-W
M27C512-15XF3	150 ns	5V ± 5%	-40°C to +125°C	FDIP28-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combinations.

PACKAGE MECHANICAL DATA - UV EPROM

Figure 9 : 28-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.199
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.027
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	7.35		7.90	0.290		0.311

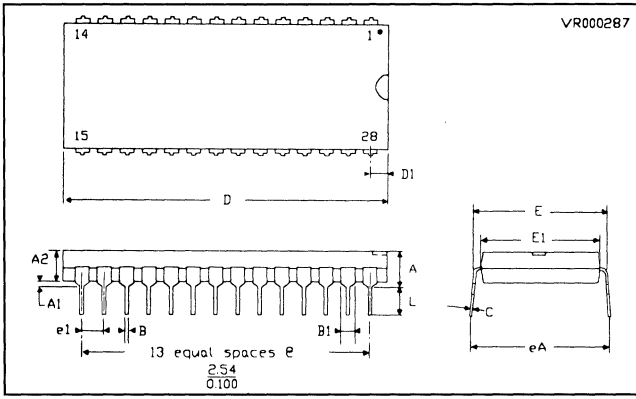
ORDERING INFORMATION (OTP ROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C512-15XB1	150 ns	5V ± 5%	0°C to +70°C	PDIP28
M27C512-20B1	200 ns	5V ± 10%	0°C to +70°C	PDIP28
M27C512-15XB6	150 ns	5V ± 5%	-40°C to +85°C	PDIP28
M27C512-15XC1	150 ns	5V ± 5%	0°C to +70°C	PLCC32
M27C512-20C1	200 ns	5V ± 10%	0°C to +70°C	PLCC32
M27C512-15XC6	150 ns	5V ± 5%	-40°C to +85°C	PLCC32
M27C512-15XM1	150 ns	5V ± 5%	0°C to +70°C	SO28
M27C512-20M1	200 ns	5V ± 10%	0°C to +70°C	SO28

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combinations.

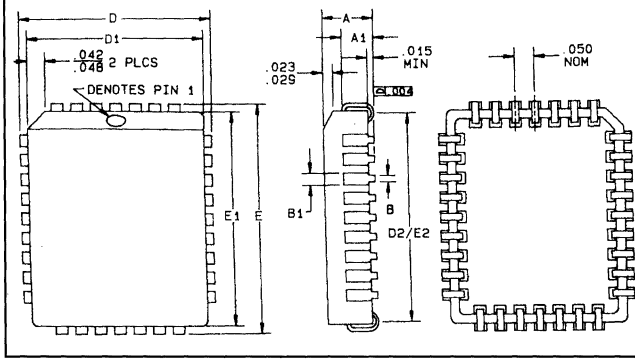
PACKAGE MECHANICAL DATA - OTP ROM

Figure 10 : 28-PIN PLASTIC DIP



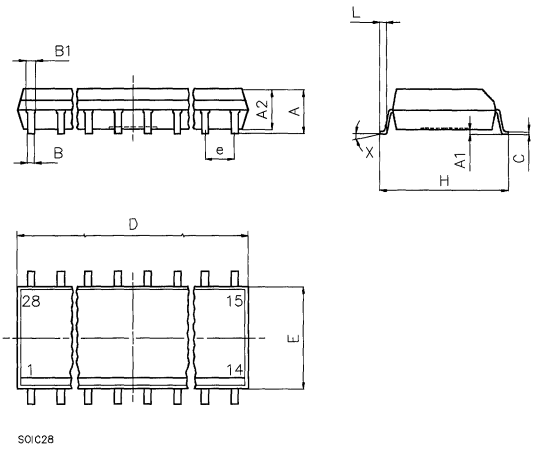
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

Figure 11 : 32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04	3.55	3.55	.120	.120	.140
A1	1.96	2.41	2.41	.078	.078	.095
B	0.33	0.53	0.53	.013	.013	.021
B1	0.66	0.81	0.81	.026	.026	.032
D	12.31	12.57	12.57	.485	.485	.495
D1	11.35	11.50	11.50	.447	.447	.453
D2	9.90	10.92	10.92	.390	.390	.430
E	14.85	15.11	15.11	.585	.585	.595
E1	13.89	14.04	14.04	.547	.547	.553
E2	12.44	13.46	13.46	.490	.490	.530

Figure 12 : SOIC28-28-LEAD SMALL OUTLINE PACKAGE



SOIC28

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.05			.120
A1	0.05		0.35	.002		.013
A2	2.34		2.69	.092		.105
B	0.35		0.51	.013		.020
B1	0.35		0.61	.013		.024
C	0.15		0.32	.006		.012
D	17.71		18.49	.697		.727
E	8.23		8.89	.324		.350
e		1.27			.050	
H	11.51		12.70	.453		.500
L	0.41		1.27	.016		.050
X		8°				8°

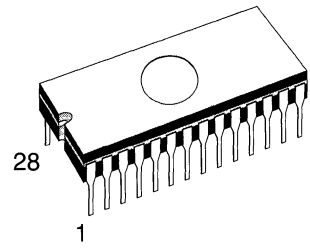
SGS-THOMSON MICROELECTRONICS

M27C513

512K (4 x 16K x 8) CMOS UV EPROM

PRODUCT PREVIEW

- PAGE ORGANIZED (M27128A FOOTPRINT).
- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 30 mA
  - Standby current 200 µA
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 6 SECONDS (PRESTO II B ALGORITHM).



FDIP28.W

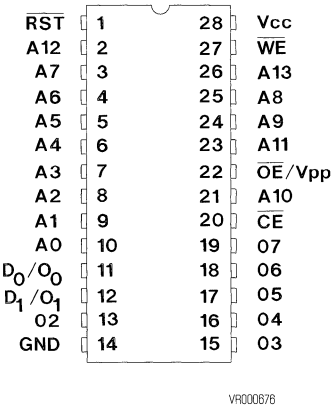
DESCRIPTION

The M27C513 is a high speed 524,288 bit ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements. Its "PAGE-ORGANIZATION" (based on 16K x 8 modules) allows easy up-grading of applications, as foot-print and addressing mode remain constant. It is housed in a 28 pin Window Ceramic Frit Seal Package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN NAMES

A0-A13	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$/VPP	OUTPUT ENABLE/VPP
$\overline{WE}$	PROGRAM/PAGE SELECT
$\overline{RST}$	RESET
O2-O7	OUTPUT
D0/O0-D1/O1	INPUT/OUTPUT
Vcc	+5V POWER SUPPLY
GND	GROUND

PIN CONNECTION

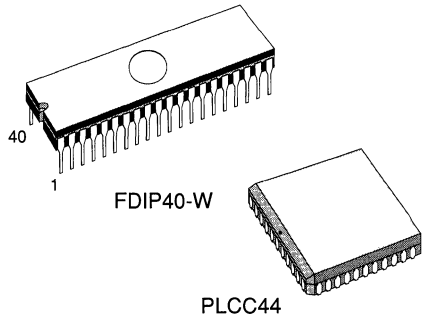


VR000676

512K 32K x 16 CMOS UV EPROM-OTP ROM

PRELIMINARY DATA

- DESIGNED FOR 16 BIT / 32 BIT SYSTEMS.
- VERY FAST ACCESS TIME : 100ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 35 mA
  - Stand by current 200 µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 3 SECONDS (PRSTO II ALGORITHM).



(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C516 is a high speed 524,288 bit (organized 32K x 16) ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.
It is housed in a 40 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.
In order to meet production requirements (cost effective solution or SMD), this product is also offered in a PLCC Plastic package, for one Time Programming only.

PIN FUNCTIONS

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O0-O15	DATA INPUT/OUTPUT
NC	NO CONNECTION
V_{PP}	PROGRAMMING VOLTAGE
V_{CC}	+5V POWER SUPPLY

Figure 1 : Pin Connection

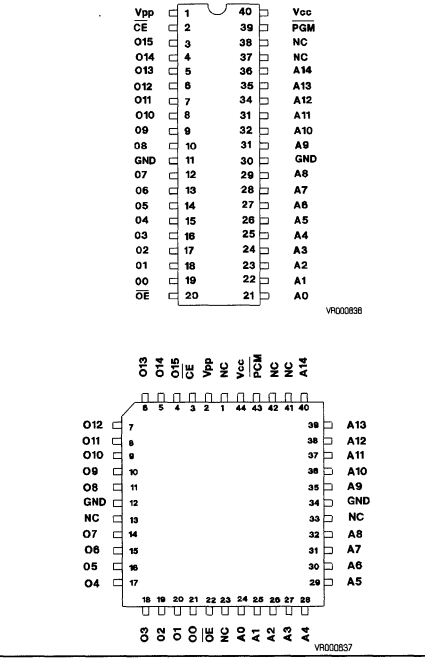
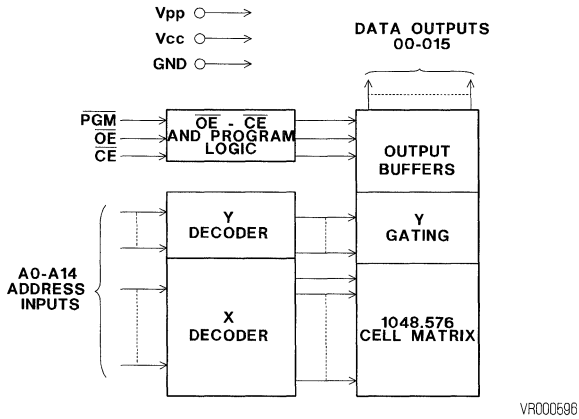


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to Ground	-0.6 to + 7.0	V
V_{PP}	Supply voltage with respect to Ground	-0.6 to + 14.0	V
V_{A9}	Voltage on A9 with respect to Ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to Ground	-0.6 to + 7.0	V
T_{bias}	Temperature range under bias	-50 to + 125	°C
T_{stg}	Storage temperature range	-65 to + 150	°C

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functionnal operation at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

OPERATING MODES

MODE	PINS					
	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUTS
READ	L	L	X	H	V_{CC}	D_{out}
OUTPUT DISABLE	L	H	X	X	V_{CC}	HIGH Z
STANDBY	H	X	X	X	V_{CC}	HIGH Z
PROGRAM	L	X	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTES : X = Don't care ; V_H = 12V ± 0.5 V ; H = High ; L = Low

DC AND AC CONDITIONS

SECTION CODE	F1	F6
Rating Temperature Range	0°C to +70°C	-40°C to +85°C
SELECTION CODE (Sample for 0°C to 70°C Oper. Temp. Range)	**10XF1, 12XF1, 15X F1, 20XF1**	**10F1, 12F1, 15F1, 20F1**
V_{CC} Power Supply	5V ± 5 %	5V ± 10 %

READ OPERATION
DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Value		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$= V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		30	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} -0.2V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input low Voltage		-0.3	0.8	V
V_{IH}	Input high Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high Voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC}-0.7		V V

AC CHARACTERISTICS

Symbol	parameter	Test Condition	27C516							
			-10		-12		-15		-20	
			Min	Max	Min	Max	Min	Max	Min	Max
T_{ACC}	Address to Output delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		100		120		150		200
T_{CE}	$\overline{CE}$ to output delay	$\overline{OE}$=V_{IL}		100		120		150		200
T_{OE}	$\overline{OE}$ to output delay	$\overline{CE}$=V_{IL}		40		50		60		70
T_{DF}(2)	$\overline{OE}$ high to output float	$\overline{CE}$=V_{IL}	0	30	0	40	0	50	0	60
T_{OH}	Output hold from address	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		0	

CAPACITANCE (3)
(TA = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{in} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output

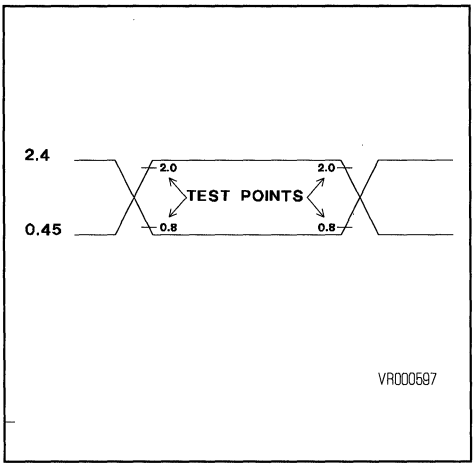


Figure 4 : AC Testing Load Circuit

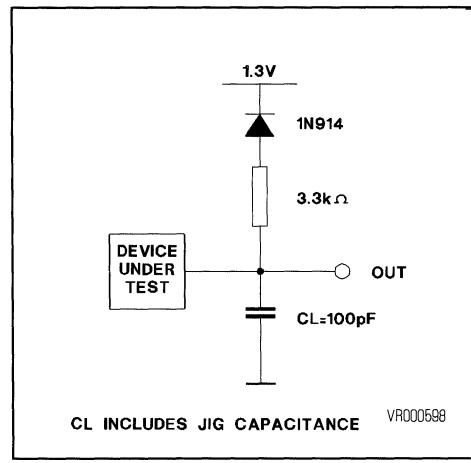
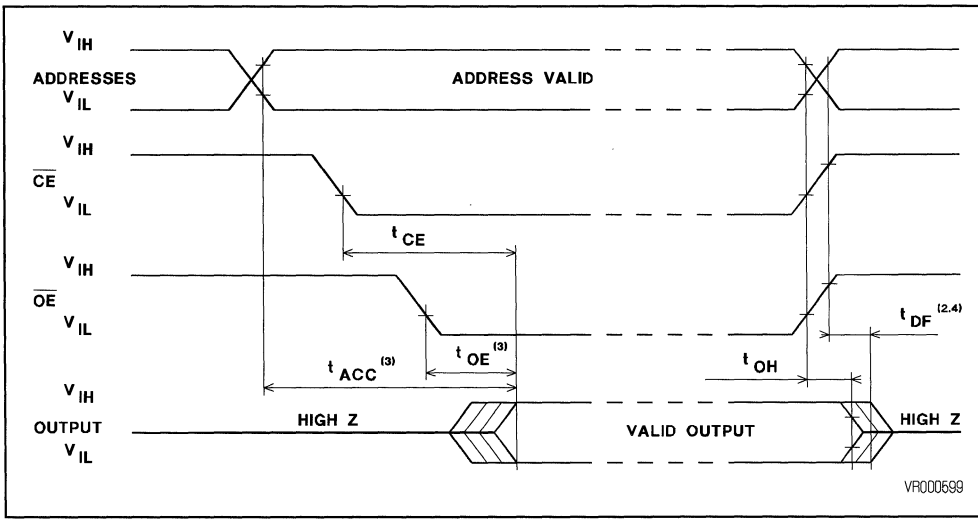


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C516 are listed in the Operating Modes. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12 V on A9 for Electronic Signature.

READ MODE

The M27C516 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C516 has a standby mode which reduces the active current from 35 mA to 0.2 mA. The M27C516 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices.

The supply current,Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 µF bulk electrolytic capacitor should be used between Vcc and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14 V on V_{pp} pin will permanently damage the M27C516.

When delivered (and after each erasure for UV EPROM), all bits of the M27C516 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C516 is in the programming mode when Vpp input is at 12.75 V, and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows to program the whole array with a guaranteed margin, in a typical time of less than 3 seconds. Programming with PRESTO II consists in applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C516s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C516 may be common. A TTL low level pulse applied to a M27C516's $\overline{CE}$ input, with $\overline{PGM}$ low and V_{PP} at 12.75 V, will program that M27C516. A high level $\overline{CE}$ input inhibits the other M27C516s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, V_{PP} at 12.75 V and V_{CC} at 6.25 V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. this mode is functional in the 25 C ± 5 C ambient temperature range that is required when programming the M27C516. To activate this mode, the programming equipment must force 11.5 V to 12.5 V on address line A9 of the M27C516 with $V_{PP} = V_{CC} = 5$ V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=VIL) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C516, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C516 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C516 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C516 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C516 window to prevent unintentional erasure. The recommended erasure procedure for the M27C516 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm2 power rating. The M27C516 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	AO	07	06	05	04	03	02	01	00	Hex.
MANUFACTURER CODE	VIL	0	0	1	0	0	0	0	0	20
DEVICE CODE	VIH	0	0	0	0	1	1	1	1	0F

NOTES : A9 = 12.0V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$; A1 to A8 = A10 to A14 = V_{IL} ; $V_{PP} = V_{CC} =$ 5V

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = - 400 uA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

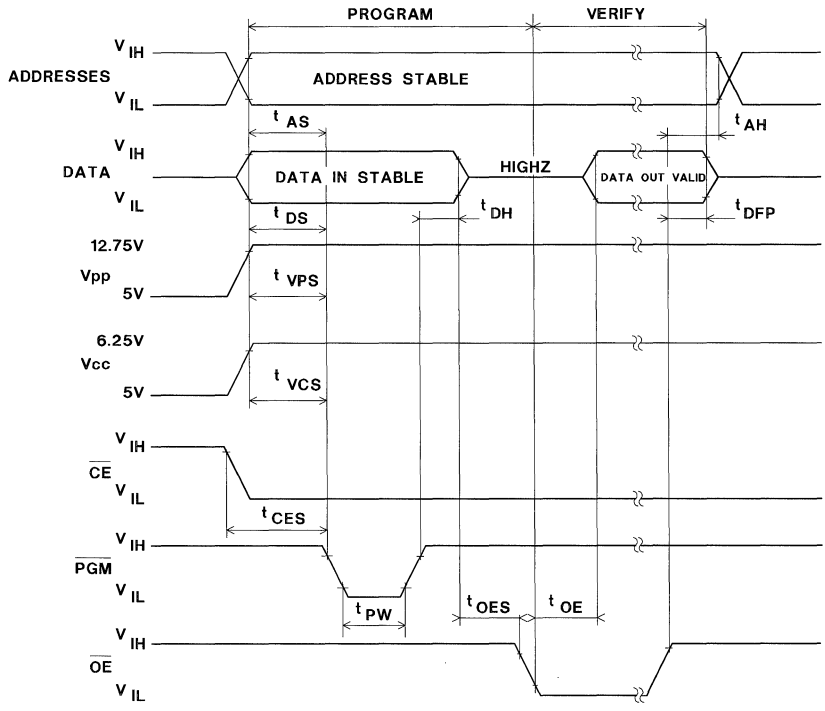
AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	nS
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{PW}	$\overline{PGM}$ initial Program Pulse Width		95	105	µS
T_{OE}	Data Valid from $\overline{OE}$			100	nS

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

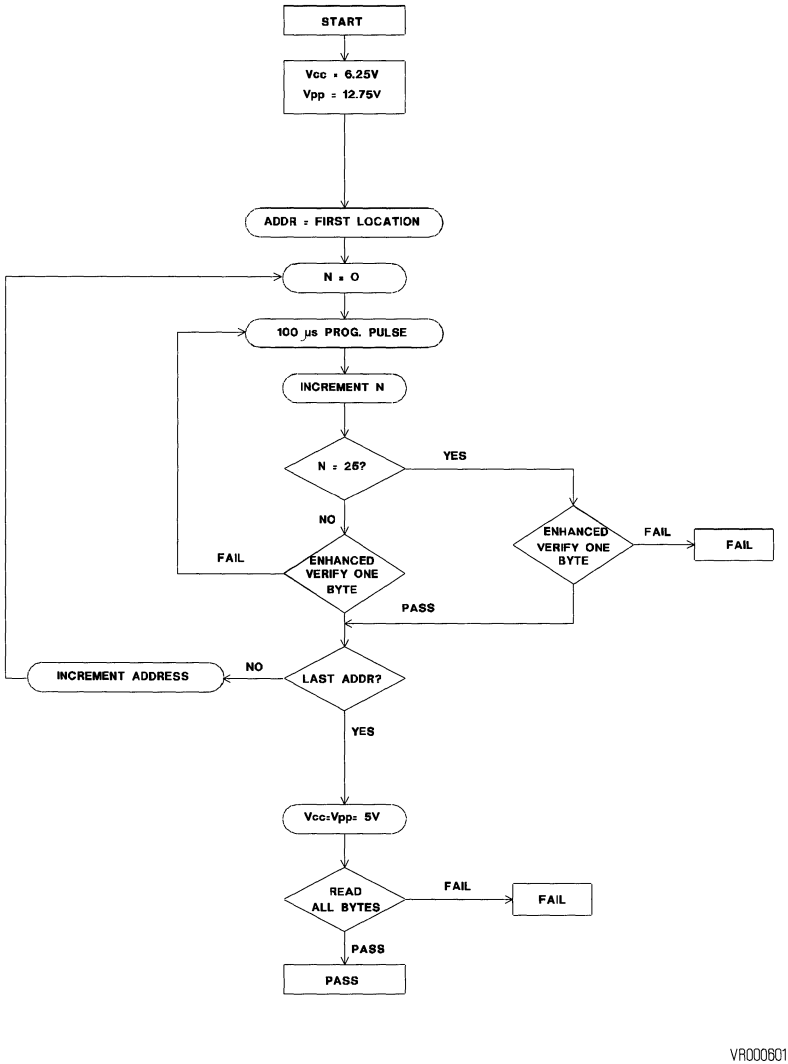
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. $t_{\overline{OE}}$ and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C516 a 0.1µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart

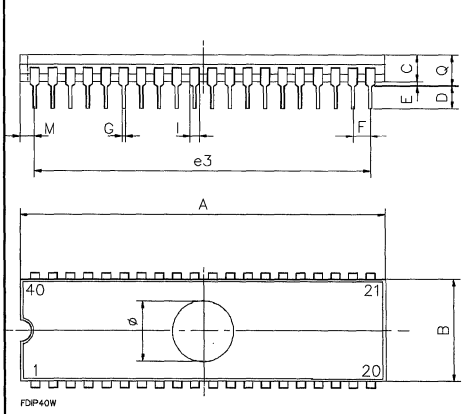


ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C516-10XF1	100 ns	5 V ± 5%	0 to +70°C	FDIP40-W
M27C516-12XF1	120 ns	5 V ± 5%	0 to +70°C	FDIP40-W
M27C516-15XF1	150 ns	5 V ± 5%	0 to +70°C	FDIP40-W
M27C516-20XF1	200 ns	5 V ± 5%	0 to +70°C	FDIP40-W
M27C516-10F1	100 ns	5 V ± 10%	0 to +70°C	FDIP40-W
M27C516-12F1	120 ns	5 V ± 10%	0 to +70°C	FDIP40-W
M27C516-15F1	150 ns	5 V ± 10%	0 to +70°C	FDIP40-W
M27C516-20F1	200 ns	5 V ± 10%	0 to +70°C	FDIP40-W

PACKAGE MECHANICAL DATA

Figure 8 : 40-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)



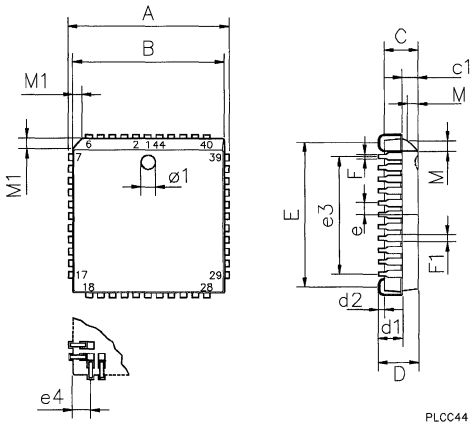
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			53.40			2.102
B	14.50		14.90	.571		.587
C	3.90		5.08	.154		.200
D	3.40			.134		
E	0.50		1.78	.020		.070
e3		48.26			1.900	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.022
I	1.27		1.52	.050		.060
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	9.45		9.85	.372		.388

ORDERING INFORMATION (OTP ROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C516-10XC1	100 ns	5 V ± 5%	0 to +70°C	PLCC44
M27C516-12XC1	120 ns	5 V ± 5%	0 to +70°C	PLCC44
M27C516-15XC1	150 ns	5 V ± 5%	0 to +70°C	PLCC44
M27C516-20XC1	200 ns	5 V ± 5%	0 to +70°C	PLCC44
M27C516-10C1	100 ns	5 V ± 10%	0 to +70°C	PLCC44
M27C516-12C1	120 ns	5 V ± 10%	0 to +70°C	PLCC44
M27C516-15C1	150 ns	5 V ± 10%	0 to +70°C	PLCC44
M27C516-20C1	200 ns	5 V ± 10%	0 to +70°C	PLCC44

PACKAGE MECHANICAL DATA

Figure 9 :



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	17.40		17.65	0.685		0.694
b	16.51		16.65	0.650		0.655
C	3.56		3.70	0.140		0.145
c1						
D	4.20		4.57	0.165		0.179
d1	2.59		2.74	0.101		0.107
d2		0.68			0.026	
E	14.99		16.00	0.590		0.629
e		1.27			0.050	
e 3		12.70			0.500	
e 4			1.98			0.077
F		0.46			0.018	
F1		0.71			0.027	
G			0.101		0.003	
M		1.16			0.045	
M1		1.14			0.044	
Ø1		1.57			0.061	

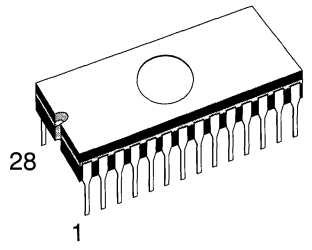
SGS-THOMSON MICROELECTRONICS

M87C512

LATCHED 512K (64K x 8)CMOS UV EPROM

PRODUCT PREVIEW

- INTEGRATED ACCESS LATCH.
- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 30 mA
  - Stand by current 200 µA
- PROGRAMMING VOLTAGE 12.75 V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 6 SECONDS (PRESTO II B ALGORITHM).



FDIP28.W

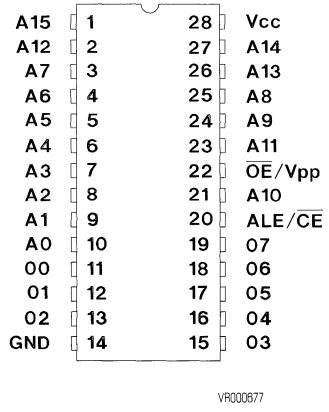
DESCRIPTION

The M87C512 is a high speed 524,288 bit ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.The M87C512 incorporates latches on all address inputs to minimize chip count, reduce cost and simplify design of multiplexed bus systems. It is housed in a 28 pin Window Ceramic Frit Seal Package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN NAMES

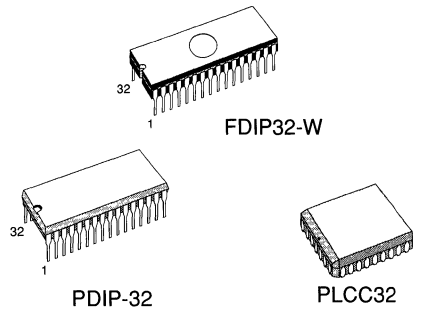
A0-A15	ADDRESSES
ALE/$\overline{CE}$	ADDRESS LATCH/CHIP ENABLE
$\overline{OE}$/$\overline{VPP}$	OUTPUT ENABLE/VPP
O0-O7	DATA INPUT/OUTPUT
Vcc	+ 5V POWER SUPPLY
GND	GROUND

PIN CONNECTION



1024K (128K x 8) CMOS UV EPROM - OTP ROM

- INTERCHANGEABLE WITH 1M BIT MASKED ROM (ROM PIN OUT).
- VERY FAST ACCESS TIME : 120ns.
- COMPATIBLE WITH HIGH SPEED MICRO-PROCESSORS, ZERO WAIT STATE.
- LOW "CMOS" POWER COMSUMPTION :
  - Active Current 35 mA
  - Standby Current 200 µA
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES AROUND 12 SECONDS (PRESTO II ALGORITHM).



(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C1000 is a high speed 1 Mbit ultraviolet erasable and electrically programmable EPROM ideally suited for 8-bit microprocessor systems requiring large programs.

It is pin compatible with 1Mbit Masked ROM version, when EPROM memory is only to be used for pre-production series.

It is organized as 131,072 words by 8 bits, and housed in a 32 pin window Ceramic Frit-Seal package.

The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.
In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIP or PLCC, for one time programming only.

PIN FUNCTIONS

A0-A16	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O0-O7	DATA INPUT/OUTPUT
NC	NO CONNECTION
V_{CC}	+5V POWER SUPPLY
V_{PP}	PROGRAMMING VOLTAGE

Figure 1 : Pin Connection

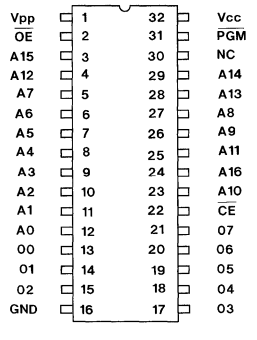
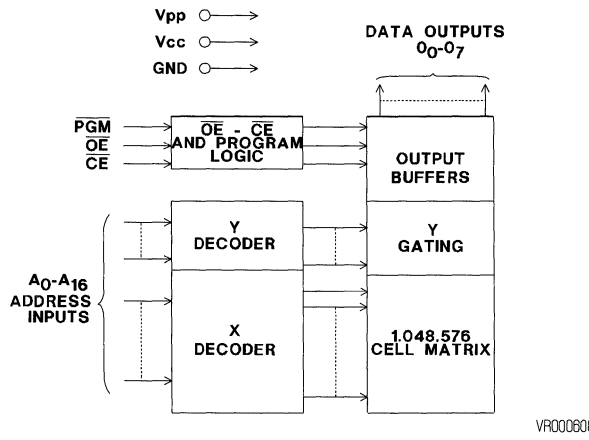


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
V_{A9}	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
T_{bias}	Temperature range under bias	-50 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS					
	$\overline{CE}$	OE	A9	$\overline{PGM}$	V_{PP}	OUTPUT
READ	L	L	X	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	X	X	V_{CC}	HIGH Z
STANDBY	H	X	X	X	V_{CC}	HIGH Z
PROGRAM	L	X	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE : X = Don't care ; V_H = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to +70°C	-40 to +85°C	-40 to +105°C	-40 to +125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC}	5 V ± 5 %		5 V ± 10 %	

NOTE : "F" stands for ceramic package. Plastic packaged device code features B,M or C

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		35	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3} (4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2 V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -100µA	2.4 V_{CC}-0.7		V

AC CHARACTERISTICS

Symbol	Parameter	Test condition	M27C1000								Unit
			-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		60		65		70		100	ns
t_{DF} (2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	40	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE (3) (T_A = 25°C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From date code 9112.

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

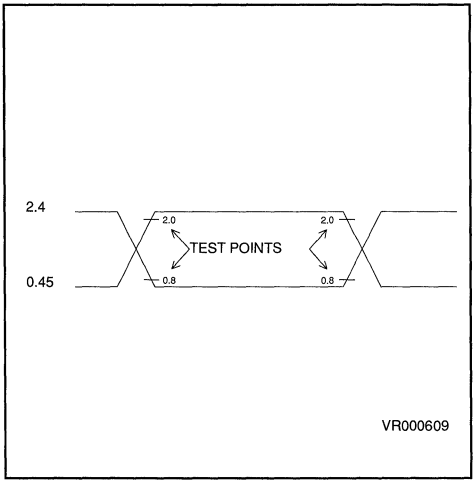


Figure 4 : AC Testing Load Circuit

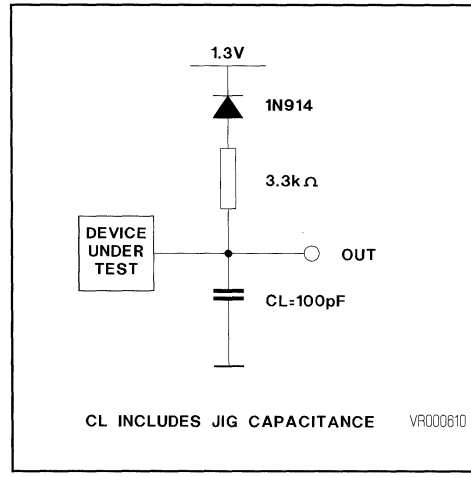
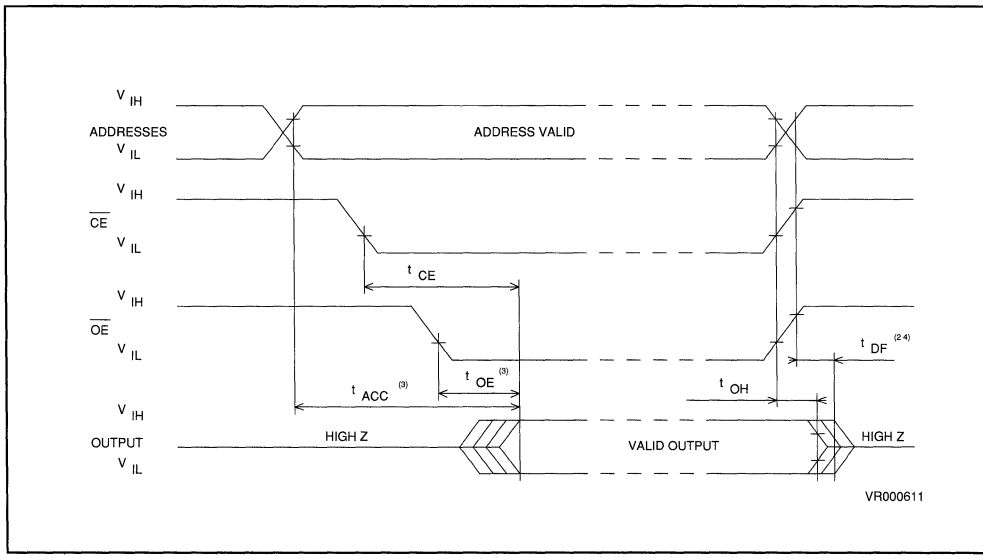


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C1000 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27C1000 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{E}$ to output (t_{CE}). Data is available at the output after delay of t_{OE} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C1000 has a standby mode which reduces the active current from 35 mA to 0.2 mA (from date code 9044). The M27C1000 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs requires careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M27C1000.

When delivered (and after each erasure for UV EPROM), all bits of the M27C1000 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C1000 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{E}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

VERY FAST AND RELIABLE PROGRAMMING ALGORITHM = PRESTO II

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 12 seconds. Programming with PRESTO II consists of applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C1000s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C1000 may be common. A TTL low level pulse applied to a M27C1000's $\overline{CE}$ input, with PGM low and V_{PP} at 12.75V, will program that M27C1000. A high level $\overline{CE}$ input inhibits the other M27C1000s from being programmed. V_{CC} is specified to be 6.25V ± 0.25V

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, PGM at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1000. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1000 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C1000, these two identifier bytes are given here below, and can be read out on outputs O0 to 07.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C1000 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1000 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1000 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1000 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1000 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C1000 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	0	1	1	0	86

NOTE : A9 = 12V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$, A1 - A8, A10 - A16 = V_{IL} ; $V_{PP} = V_{CC} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

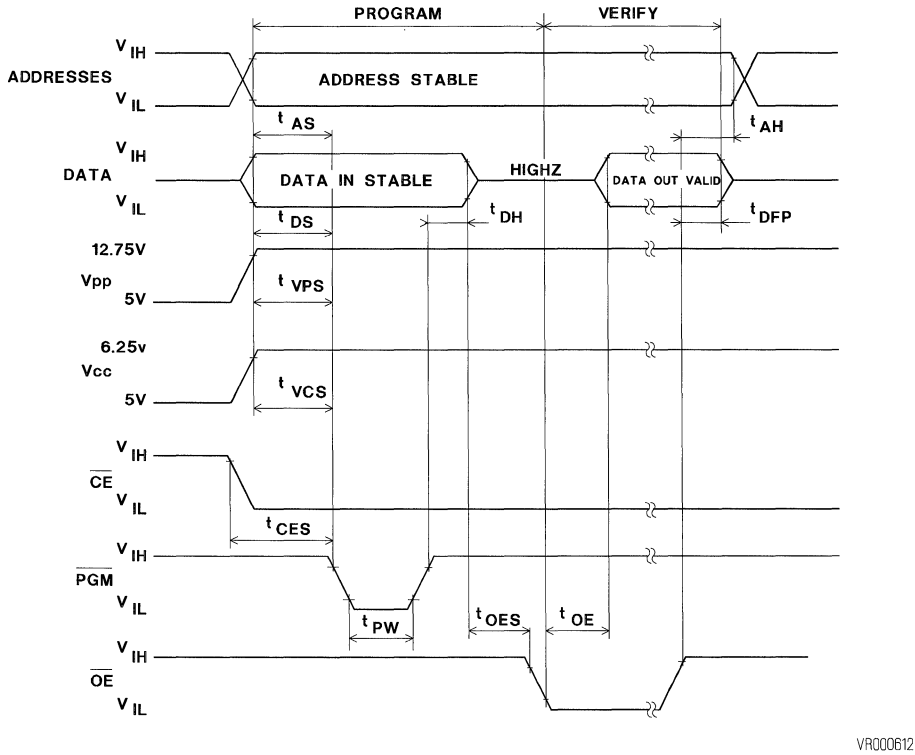
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

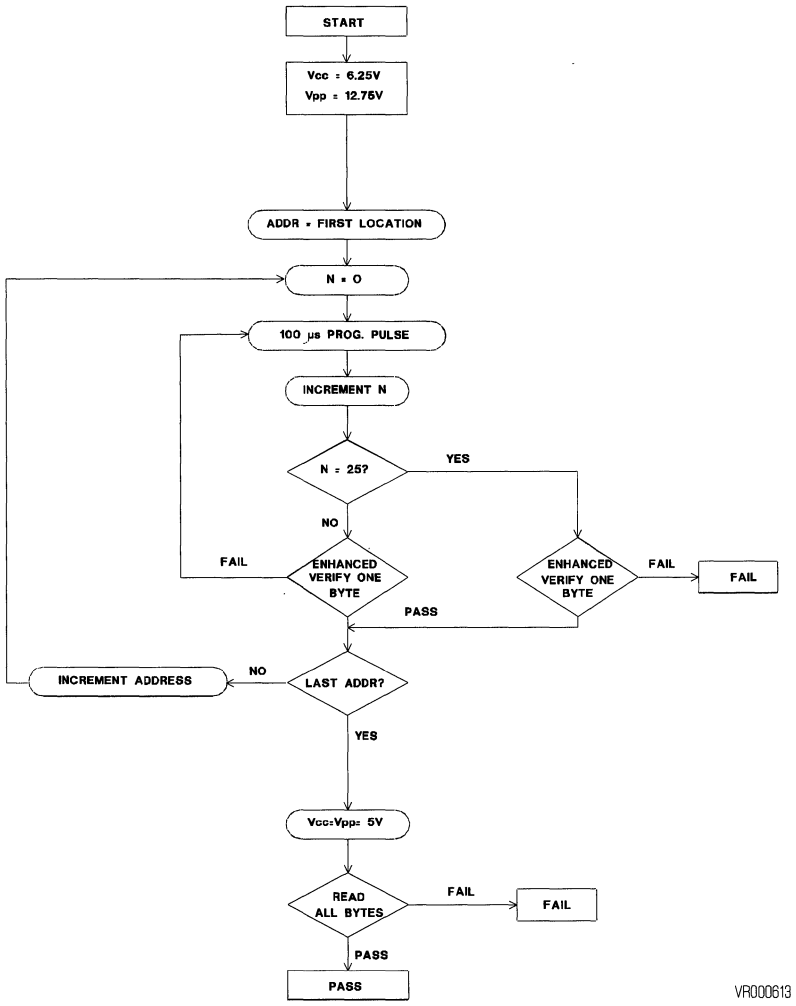
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C1000 a 0.1µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart



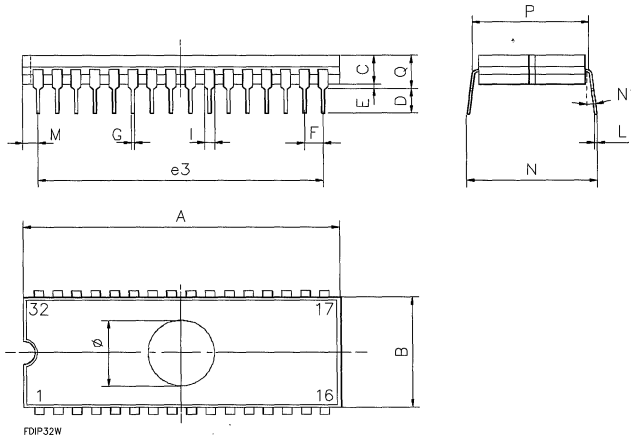
ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1000 - 12XF1	120 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1000 - 15XF1	150 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1000 - 20XF1	200 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1000 - 25XF1	250 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1000 - 12F1	120 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1000 - 15F1	150 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1000 - 20F1	200 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1000 - 25F1	250 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1000 - 12XF6	120 ns	5V ± 5%	-40°C to +85°C	FDIP32-W
M27C1000 - 15XF6	150 ns	5V ± 5%	-40°C to +85°C	FDIP32-W
M27C1000 - 15F6	150 ns	5V ± 10%	-40°C to +85°C	FDIP32-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA

Figure 8 : 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			42.78			1.684
B	14.50		14.90	0.570		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		38.10			1.500	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	9.45		9.85	0.372		0.388

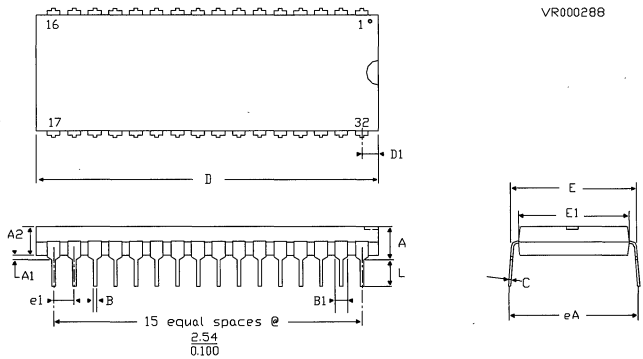
ORDERING INFORMATION (OTP ROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1000-15XB1	150 ns	5V ± 5%	0°C to +70°C	DIP32
M27C1000-20XB1	200 ns	5V ± 5%	0°C to +70°C	DIP32
M27C1000-15B1	150 ns	5V ± 10%	0°C to +70°C	DIP32
M27C1000-20B1	200 ns	5V ± 10%	0°C to +70°C	DIP32
M27C1000-15XB6	150 ns	5V ± 5%	-40°C to +85°C	DIP32
M27C1000-15XC1	150 ns	5V ± 5%	0°C to +70°C	PLCC32
M27C1000-20XC1	200 ns	5V ± 5%	0°C to +70°C	PLCC32
M27C1000-15C1	150 ns	5V ± 10%	0°C to +70°C	PLCC32
M27C1000-20C1	200 ns	5V ± 10%	0°C to +70°C	PLCC32
M27C1000-15XC6	150 ns	5V ± 5%	-40°C to +85°C	PLCC32

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

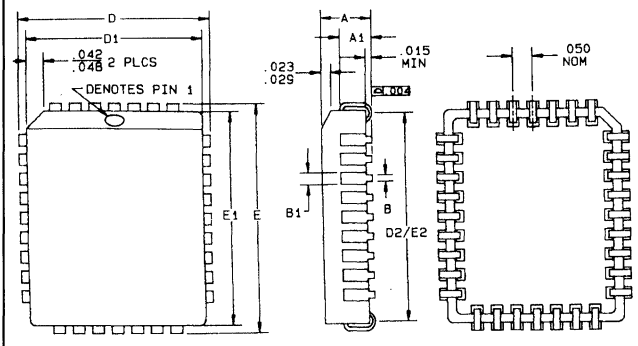
PACKAGE MECHANICAL DATA (Continued)

Figure 9 : PLASTIC DIL 32



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.38			0.015		
b		0.46			0.018	
b1	0.20		0.30	0.008		0.012
b2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e 3		35.60			1.400	
e 4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L			3.43	0.125		0.135

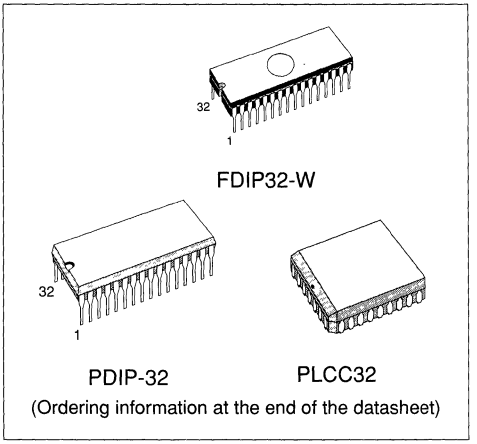
Figure 10 : PLCC32-32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04	3.55	3.55	.120	.120	.140
A1	1.96	2.41	2.41	.078	.078	.095
B	0.33	0.53	0.53	.013	.013	.021
B1	0.66	0.81	0.81	.026	.026	.032
D	12.31	12.57	12.57	.485	.485	.495
D1	11.35	11.50	11.50	.447	.447	.453
D2	9.90	10.92	10.92	.390	.390	.430
E	14.85	15.11	15.11	.585	.585	.595
E1	13.89	14.04	14.04	.547	.547	.553
E2	12.44	13.46	13.46	.490	.490	.530

1024K (128K x 8) CMOS UV EPROM - OTP ROM

- JEDEC PIN OUT.
- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Active Current 35mA
  - Standby Current 200 µA
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 12 SECONDS (PRESTO II ALGORITHM).



(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C1001 is a high speed 1 Mbit ultraviolet erasable and electrically programmable EPROM ideally suited for 8-bit microprocessor systems requiring large programs.

It is organized as 131,072 words by 8 bits, and housed in a 32 pin Window Ceramic Frit-Seal package.

The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.
In order to meet production requirements (cost effective solution or SMD), this product is also offered in a plastic package, either Plastic DIP or PLCC, for One Time Programming only.

PIN FUNCTIONS

AO-A16	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O0-O7	DATA INPUT/OUTPUT
NC	NON CONNECTED
V_{CC}	+5V POWER SUPPLY
V_{PP}	PROGRAMMING VOLTAGE

Figure 1. Pin Connection

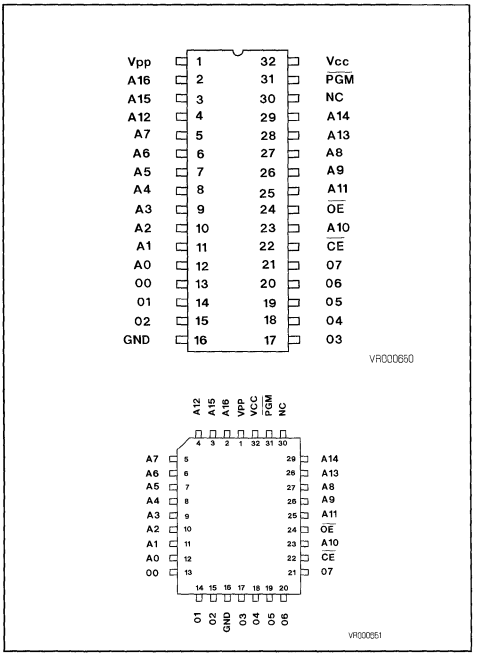
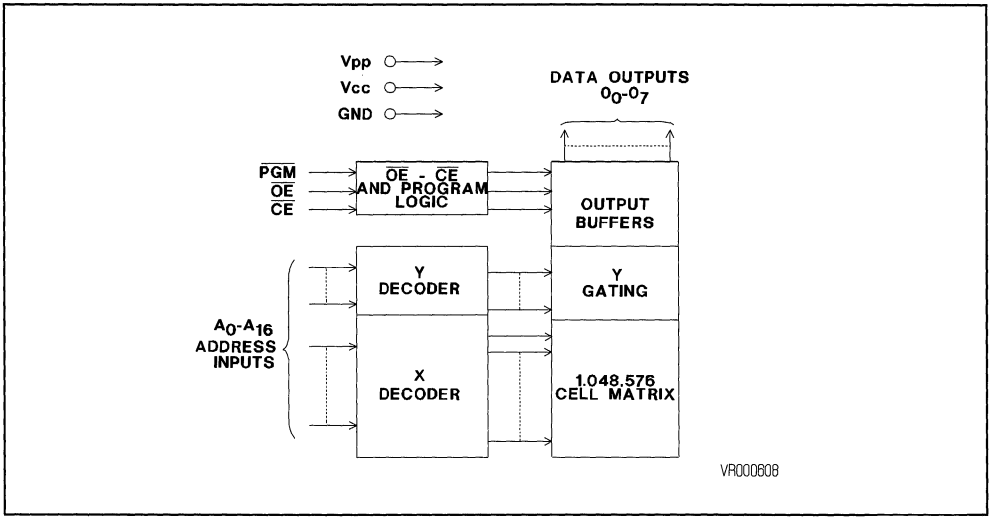


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
VA9	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
T_{bias}	Temperature range under bias	-50 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	PINS					
	$\overline{CE}$	OE	A9	$\overline{PGM}$	V_{PP}	OUTPUT
READ	L	L	X	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	X	X	V_{CC}	HIGH Z
STANDBY	H	X	X	X	V_{CC}	HIGH Z
PROGRAM	L	X	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE : X = Don't care ; V_H = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to +70°C	-40 to +85°C	-40 to +105°C	-40 to +125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC}	5 V ± 5 %		5 V ± 10 %	

NOTE : "F" stands for ceramic package. Plastic packaged device code features B,M or C.

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$=$\overline{OE}$=V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		35	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3} (4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2 V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -100µA	2.4 V_{CC}-0.7		V

AC CHARACTERISTICS

Symbol	Parameter	Test condition	M27C1001								Unit
			-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address Output Delay	$\overline{CE}$= $\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		60		65		70		100	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	40	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE(3)

(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From date code 9112.

AC TEST CONDITIONS

Input Rise and Fall Times : ≤ 20ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing Input/Output Waveform

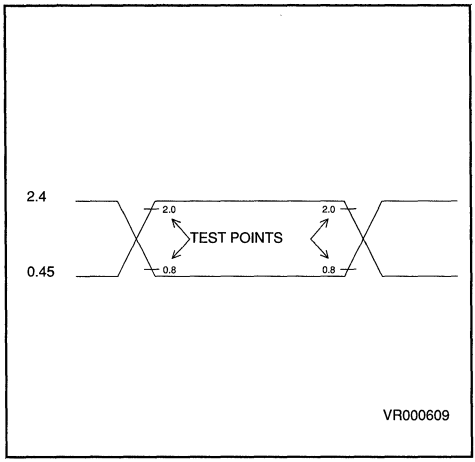


Figure 4 : AC Testing Load Circuit

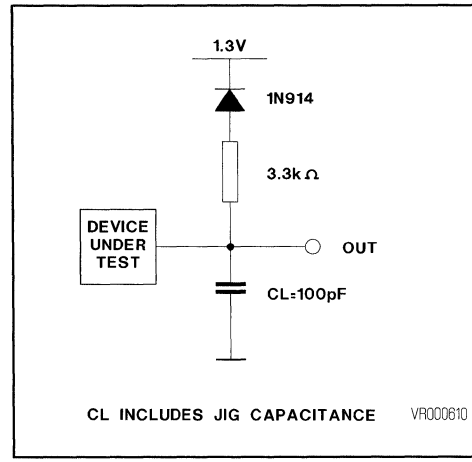
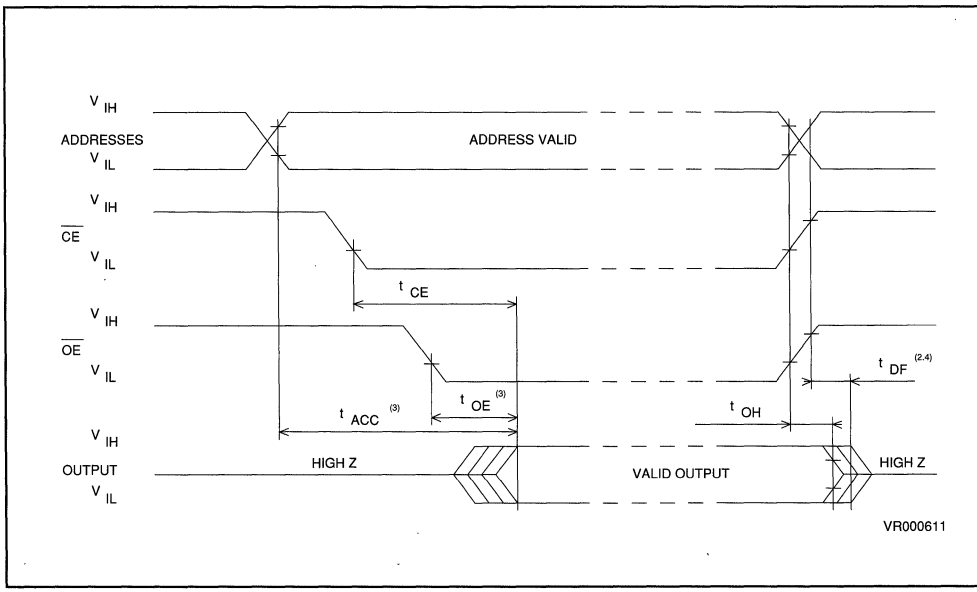


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. tDF is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operation of the M27C1001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27C1001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C1001 has a standby mode which reduces the active current from 35 mA to 0.2 mA (from date code 9044). The M27C1001 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices.

The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M27C1001.

When delivered (and after each erasure for UV EPROM), all bits of the M27C1001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C1001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. Vcc is specified to be 6.25V ± 0.25V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows the whole array to be programmed, with a guaranteed margin, in around 12 seconds. Programming with PRESTO II involves in applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C1001s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C1001 may be common. A TTL low level pulse applied to a M27C1001's $\overline{CE}$ input, with $\overline{PGM}$ low and V_{PP} at 12.75V, will program that M27C1001. A high level $\overline{CE}$ input inhibits the other M27C1001s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1001 with V_{PP} = V_{CC} = 5V. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1001, with V_{PP}=V_{CC}=5V. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C1001, these two identifier bytes are given here below, and can be read-out on outputs O0 to 07.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristics of the M27C1001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1001 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	0	1	0	1	05

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$ = $\overline{OE}$ = V_{IL} , A1 - A8, A10 - A16 = V_{IL} ; V_{PP} = V_{CC} = 5V

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

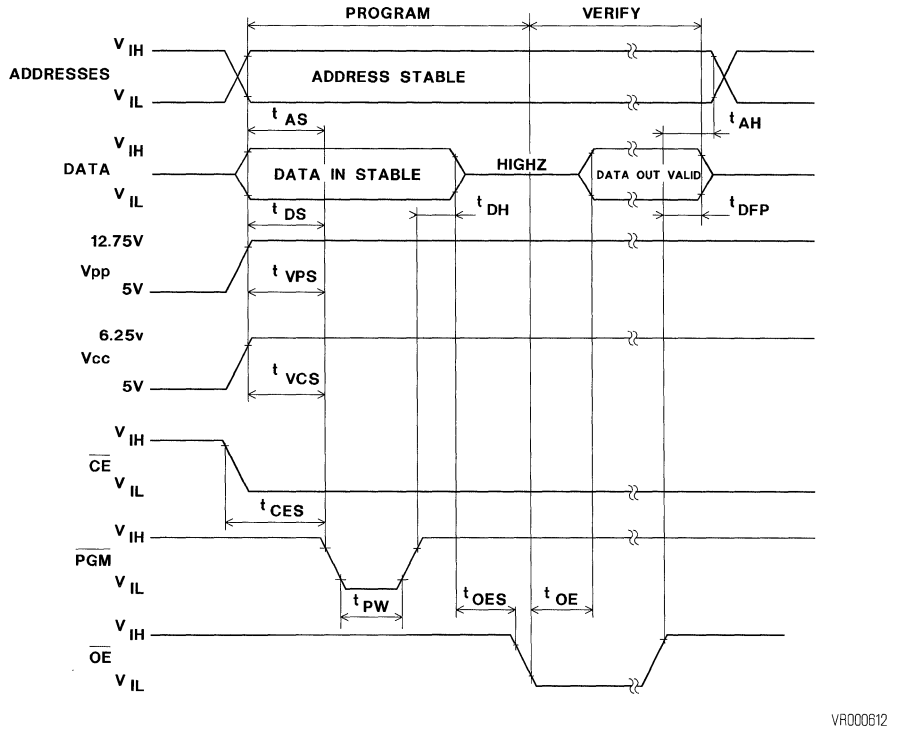
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

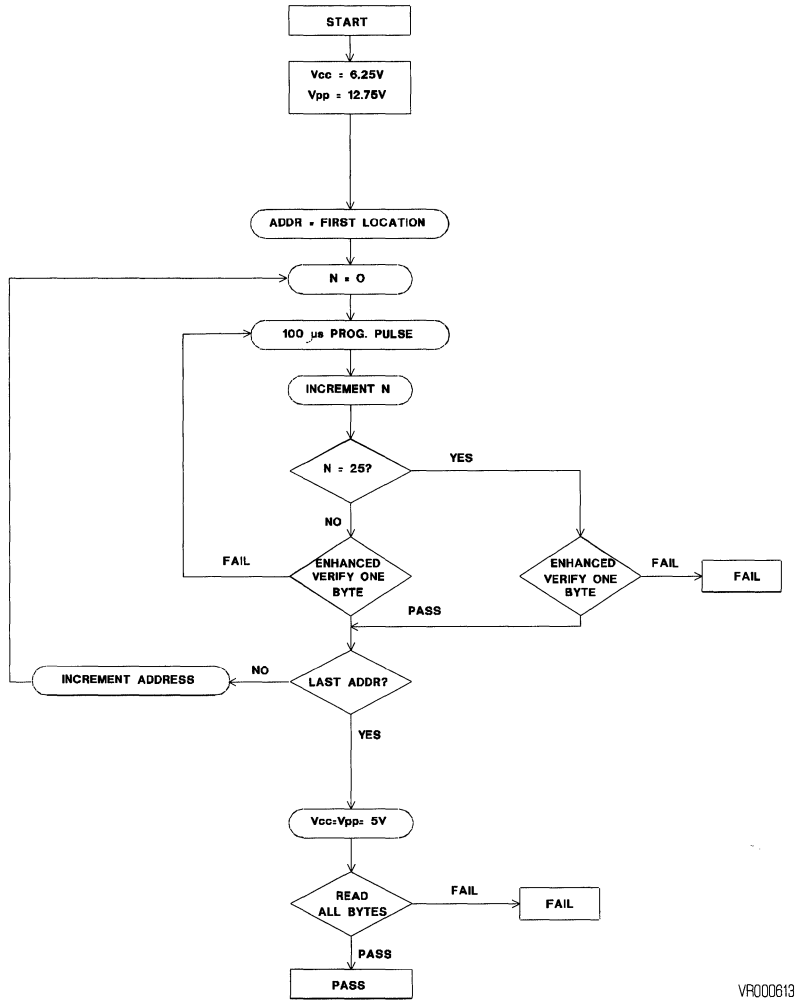
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C1001 a 0.1µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart



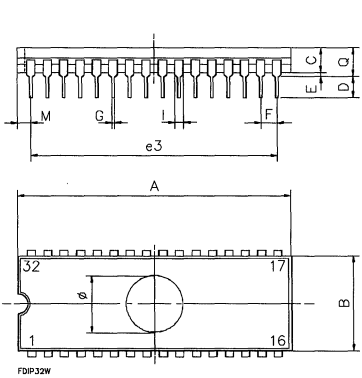
ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1001 - 12XF1	120 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1001 - 15XF1	150 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1001 - 20XF1	200 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1001 - 25XF1	250 ns	5V ± 5%	0°C to +70°C	FDIP32-W
M27C1001 - 12F1	120 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1001 - 15F1	150 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1001 - 20F1	200 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1001 - 25F1	250 ns	5V ± 10%	0°C to +70°C	FDIP32-W
M27C1001 - 12XF6	120 ns	5V ± 5%	-40°C to +85°C	FDIP32-W
M27C1001 - 15XF6	150 ns	5V ± 5%	-40°C to +85°C	FDIP32-W
M27C1001 - 15F6	150 ns	5V ± 10%	-40°C to +85°C	FDIP32-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA

Figure 8 : 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			42.78			1.684
B	14.50		14.90	.570		.587
C	3.90		5.08	.154		.200
D	3.40			.134		
E	0.50		1.78	.020		.070
e3		38.10			1.500	
F	2.29		2.79	.090		.110
G	0.40		0.55	.016		.022
I	1.27		1.52	.050		.060
L	0.22		0.31	.009		.012
M	1.52		2.49	.060		.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	.606		.622
Q			5.71			.225
Ø	9.45		9.85	.372		.388

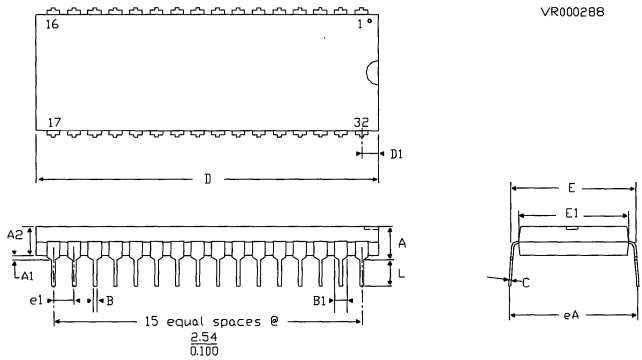
ORDERING INFORMATION - OTP ROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1001-15XB1	150 ns	5V ± 5%	0°C to +70°C	PDIP32
M27C1001-20XB1	200 ns	5V ± 5%	0°C to +70°C	PDIP32
M27C1001-15B1	150 ns	5V ± 10%	0°C to +70°C	PDIP32
M27C1001-20B1	200 ns	5V ± 10%	0°C to +70°C	PDIP32
M27C1001-15XB6	150 ns	5V ± 5%	-40°C to +85°C	PDIP32
M27C1001-15XC1	150 ns	5V ± 5%	0°C to +70°C	PLCC32
M27C1001-20XC1	200 ns	5V ± 5%	0°C to +70°C	PLCC32
M27C1001-15C1	150 ns	5V ± 10%	0°C to +70°C	PLCC32
M27C1001-20C1	200 ns	5V ± 10%	0°C to +70°C	PLCC32
M27C1001-15XC6	150 ns	5V ± 5%	-40°C to +85°C	PLCC32

Note : Consult your nearest SGS-THOMSON sales office for availability of other combination.

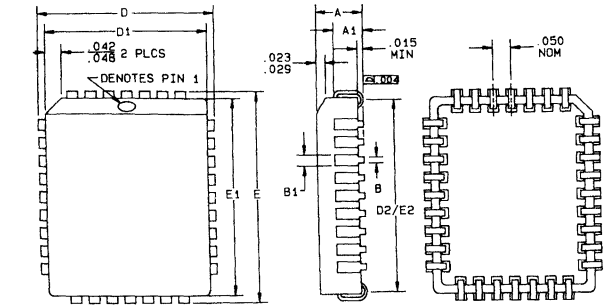
PACKAGE MECHANICAL DATA - OTP ROM

Figure 9 : 32-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
A1	0.38			0.015		
B		0.46			0.018	
B1	0.20		0.30	0.008		0.012
B2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e3		35.60			1.400	
e4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L	3.18		3.43	0.125		0.135

Figure 10 : 32-LEAD PLASTIC LEADED CHIP CARRIER

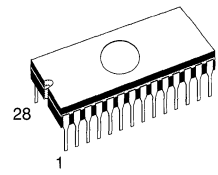


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04		3.55	.120		.140
A1	1.96		2.41	.078		.095
B	0.33		0.53	.013		.021
B1	0.66		0.81	.026		.032
D	12.31		12.57	.485		.495
D1	11.36		11.50	.447		.453
D2	9.90		10.92	.390		.430
E	14.85		15.11	.585		.595
E1	13.89		14.04	.547		.553
E2	12.44		13.46	.490		.530

1024K (8 x 16K x 8) CMOS UV EPROM - OTP ROM

PRODUCT PREVIEW

- PAGE ORGANIZED (M27128 FOOTPRINT).
- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE TO HIGH SPEED.
- MICROPROCESSORS ZERO WAIT STATE LOW POWER "CMOS" CONSUMPTION :
  - Operating current 35 mA.
  - Stand by current 200 µA.
- PROGRAMMING VOLTAGE 12.75 V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 12 SECONDS (PRESTO II ALGORITHM).



FDIP28-W

(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C1011 is a high speed 1,048,576 bit ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

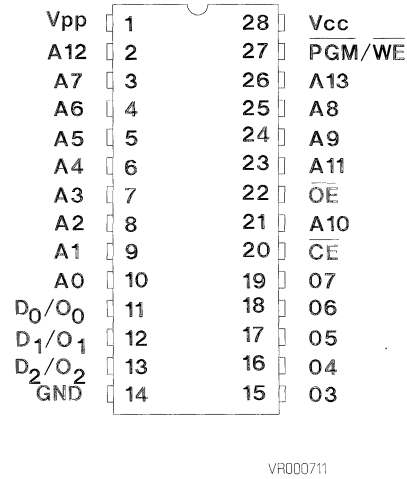
Its "PAGE-ORGANIZATION" (based on 16K x 8 module) allows an easy up-grading of applications, as foot-print and addressing mode remain constant.

It is housed in a 28 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN NAMES

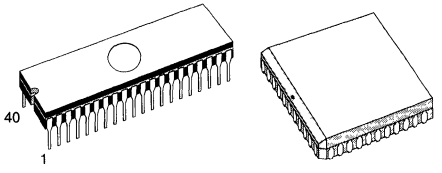
A0 - A13	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}/\overline{WE}$	PROGRAM/PAGE SELECT
O3 - O7	OUTPUT
D0/O0 - D2/O2	INPUT/OUTPUT
V_{PP}	PROGRAMMING VOLTAGE
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Configuration



1024K (64K x 16) CMOS UV EPROM - OTP ROM

- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW "CMOS" CONSUMPTION :
  - Active Current 35 mA
  - Standby Current 1 mA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIME OF AROUND 6 SECONDS (PRESTO II ALGORITHM).



FDIP40-W PLCC44

(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C1024 is a 1,048,576-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits.

It is housed in a 40 pin Ceramic Frit Seal Window package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), product is also offered in PLCC plastic package for One Time Programming only.

PIN FUNCTIONS

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O0-O15	DATA INPUT/OUTPUT
NC	NO CONNECTION
V_{CC}	+ 5V POWER SUPPLY
V_{PP}	PROGRAMMING VOLTAGE

Figure 1 : Pin Connection

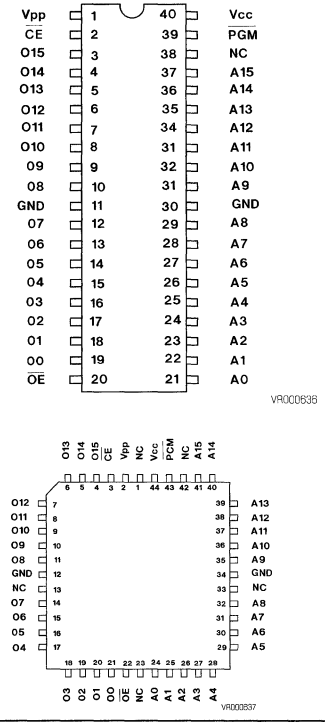
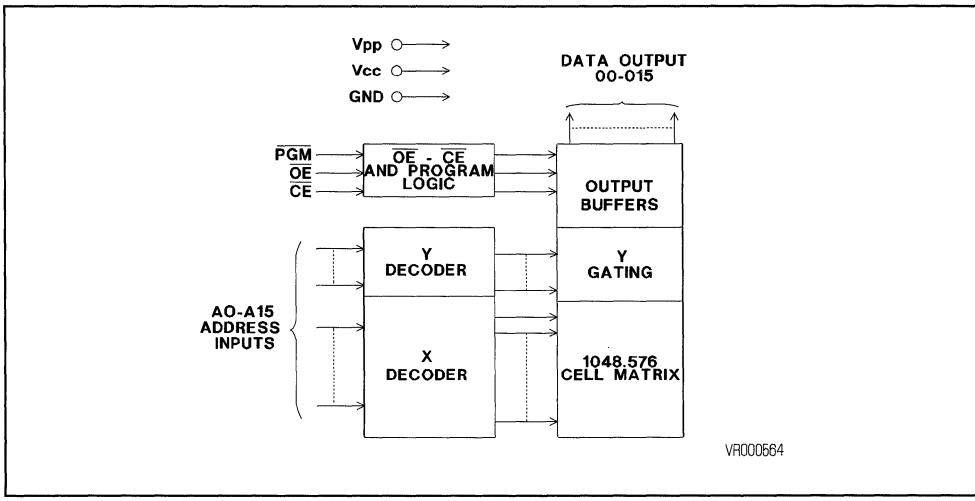


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output Voltages with respect to Ground	-0.6 to + 7.0	V
V_{PP}	Supply Voltage with respect to Ground	-0.6 to + 14.0	V
V_{A9}	Voltage on A9 with respect to Ground	-0.6 to + 13.5	V
V_{CC}	Supply Voltage with respect to Ground	-0.6 to + 7.0	V
T_{bias}	Temperature range under bias	-50 to + 125	°C
T_{stg}	Storage temperature range	- 65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUT
READ	L	L	X	H	V_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	X	X	V_{CC}	HIGH Z
STANDBY	H	X	X	X	V_{CC}	HIGH Z
PROGRAM	L	X	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE : X = Don't Care ; V_H = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC}	5V ± 5%		5V ± 10%	

NOTES : "F" stands for ceramic package. Plastic packaged device code features B, M or C.

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		35	mA
I_{CC2}	VCC Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{PP1}	V_{PP} Read Current	V_{PP}=V_{CC}		100	µA
V_{IL}	Input low voltage		-0.3	0.8	V
V_{IH}	Input high voltage		2.0	V_{CC}+ 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC} - 0.7		V V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C1024								Unit
			-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output delay	$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		60		65		70		100	ns
t_{DF}	$\overline{OE}$ High to Output float	$\overline{CE}$=V_{IL}	0	40	0	50	0	60	0	60	ns
t_{OH}	Output hold from address $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE (3)

(T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V			5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			5	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output float is defined as the point where data is no longer driver-seen.
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Reference Levels :	
Input Pulse Levels	:	0.45 to 2.4V	Inputs : 0.8 and 2 V - Outputs : 0.8 and 2 V	

Figure 3 : AC Testing Input/Output Waveform

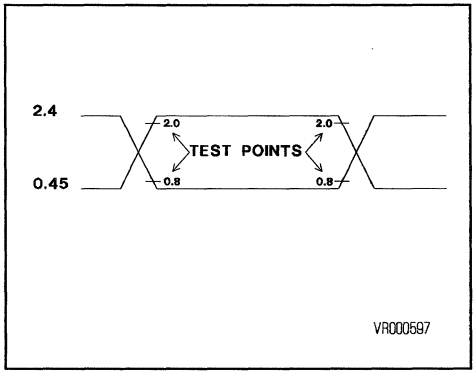


Figure 4 : AC Testing Load Circuit

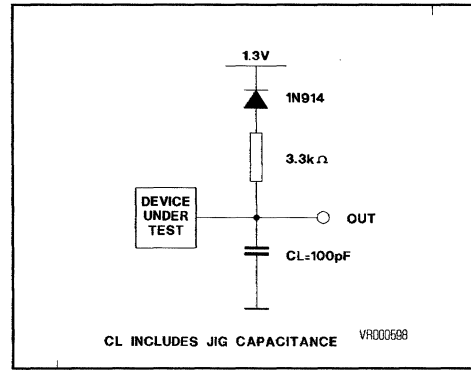
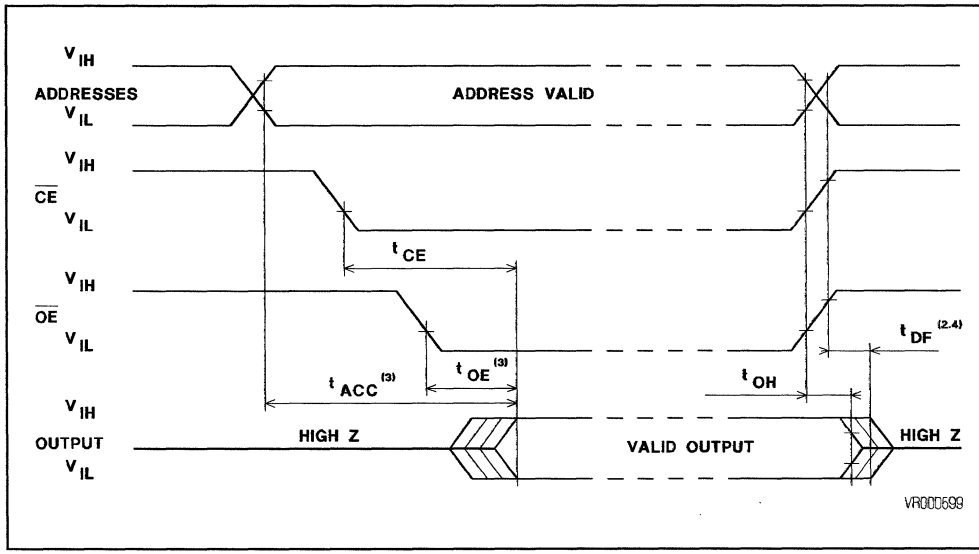


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for Vpp and 12V on A9 for Electronic Signature.

READ MODE

The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C1024 has a standby mode which reduces the active current from 35 mA to 1 mA. The M27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M27C1024.

When delivered (and after each erasure for UV EPROM), all bits of the M27C1024 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C1024 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied, 16 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

VERY FAST AND RELIABLE PROGRAMMING ALGORITHM = PRESTO II

PRESTO II Programming Algorithm allows programming of the whole array with a guaranteed margin, in a typical time of less than 6 seconds. Programming with PRESTO II consists of applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C1024 may be common. A TTL low level pulse applied to a M27C1024's $\overline{CE}$ input, with $\overline{PGM}$ low and V_{PP} at 12.75V, will program that M27C1024. A high level $\overline{CE}$ input inhibits the other M27C1024s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1024. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C1024 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C1024, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C1024 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	1	0	0	8C

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$, $\overline{OE}$ = V_{IL} ; A1-A8, A10-A15 = V_{IL} ; $V_{PP} = V_{CC} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

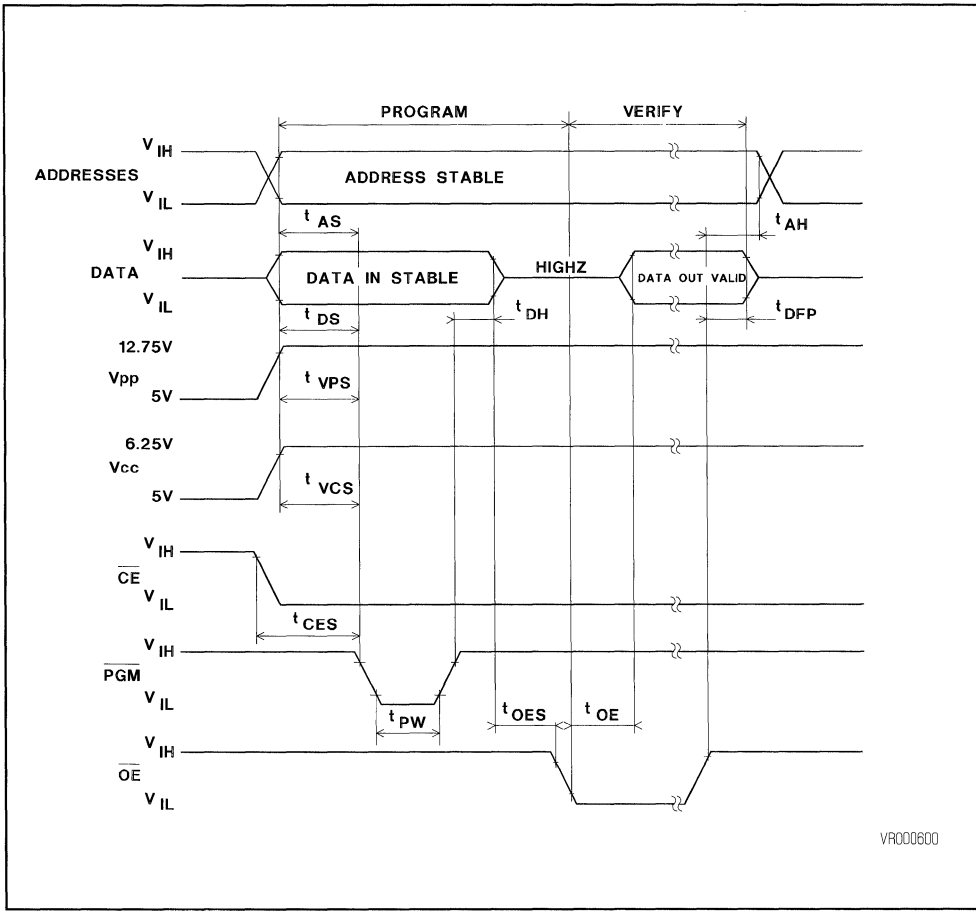
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP} [2]	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATING (Continued)

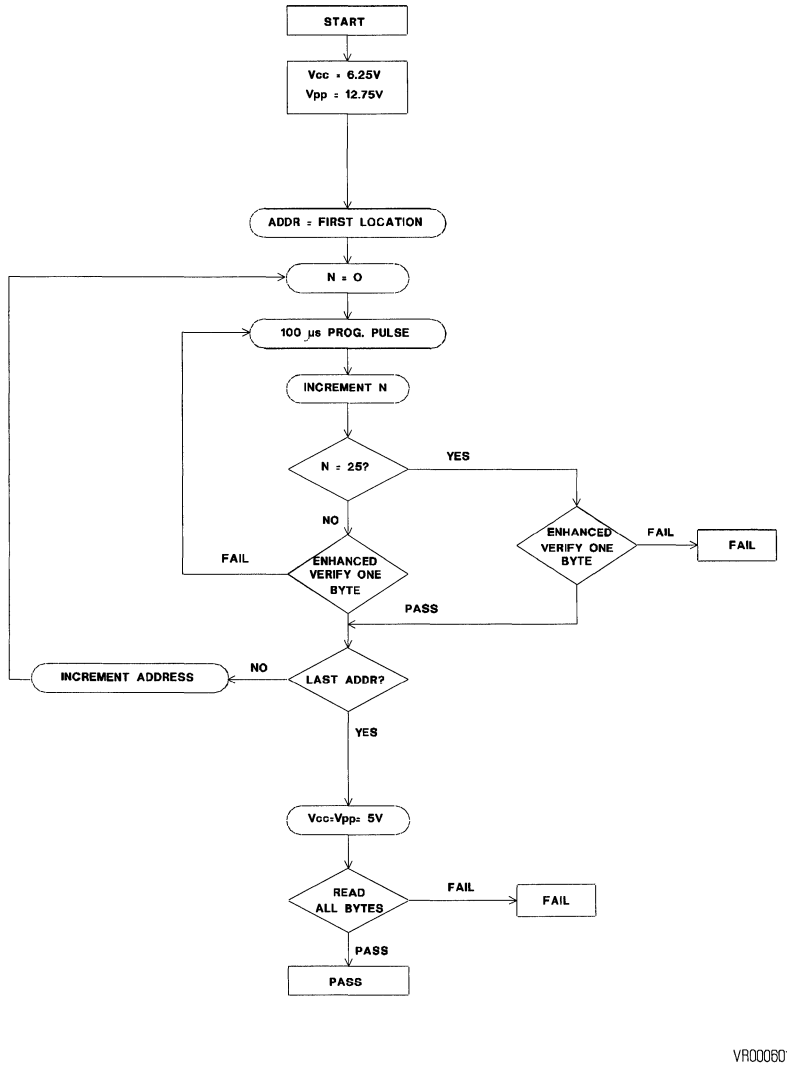
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C1024 a 0.1µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart



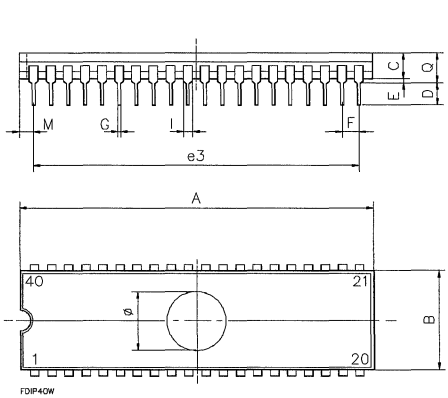
ORDERING INFORMATION - UV EPROM

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1024-12XF1	120 ns	5 V ± 5%	0 TO +70°C	FDIP40-W
M27C1024-15XF1	150 ns	5 V ± 5%	0 TO +70°C	FDIP40-W
M27C1024-20XF1	200 ns	5 V ± 5%	0 TO +70°C	FDIP40-W
M27C1024-25XF1	250 ns	5 V ± 5%	0 TO +70°C	FDIP40-W
M27C1024-12F1	120 ns	5 V ± 10%	0 TO +70°C	FDIP40-W
M27C1024-15F1	150 ns	5 V ± 10%	0 TO +70°C	FDIP40-W
M27C1024-20F1	200 ns	5 V ± 10%	0 TO +70°C	FDIP40-W
M27C1024-25F1	250 ns	5 V ± 10%	0 TO +70°C	FDIP40-W
M27C1024-12XF6	120 ns	5 V ± 5%	-40 TO +85°C	FDIP40-W
M27C1024-15XF6	150 ns	5 V ± 5%	-40 TO +85°C	FDIP40-W
M27C1024-15F6	150 ns	5 V ± 10%	-40 TO +85°C	FDIP40-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combination.

PACKAGE MECHANICAL DATA - UV EPROM

Figure 8 : 40-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			53.40			2.102
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		48.26			1.900	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	9.45		9.85	0.372		0.388

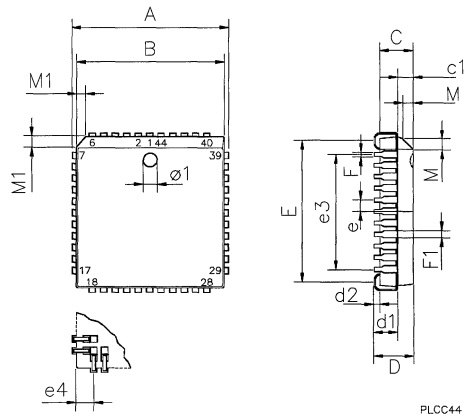
ORDERING INFORMATION (OTP ROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1024-15XC1	150 ns	5 V ± 5%	0 TO +70°C	PLCC44
M27C1024-20XC1	200 ns	5 V ± 5%	0 TO +70°C	PLCC44
M27C1024-15XC6	150 ns	5 V ± 5%	-40 TO +85°C	PLCC44

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combinations.

PACKAGE MECHANICAL DATA - OTP ROM

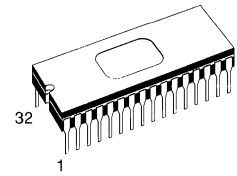
Figure 9 :



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	17.40		17.65	0.685		0.694
b	16.51		16.65	0.650		0.655
C	3.56		3.70	0.140		0.145
c1						
D	4.20		4.57	0.165		0.179
d1	2.59		2.74	0.101		0.107
d2		0.68			0.026	
E	14.99		16.00	0.590		0.629
e		1.27			0.050	
e 3		12.70			0.500	
e 4			1.98			0.077
F		0.46			0.018	
F1		0.71			0.027	
G			0.101		0.003	
M		1.16			0.045	
M1		1.14			0.044	
Ø1		1.57			0.061	

2048K (256K x 8) CMOS UV EPROM

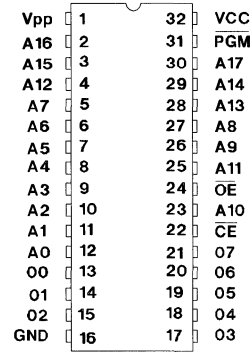
- VERY FAST ACCESS TIME : 120 ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 35 mA
  - Stand by current 200 µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 24 SECONDS (PRESTO II ALGORITHM).



FDIP32-W

(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection



DESCRIPTION

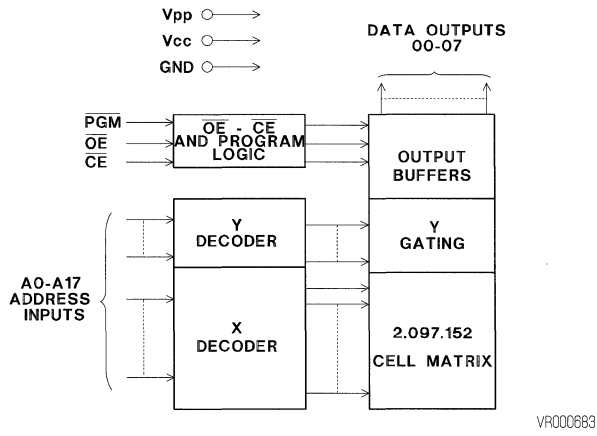
The M27C2001 is a high speed 2,097,152 (organized 262,144 X 8) bit ultraviolet erasable and programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

It is housed in a 32 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN FUNCTIONS

A0-A17	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
O0-O7	DATA INPUT/OUTPUT
NC	NO CONNECTION
V_{CC}	+5V POWER SUPPLY
V_{PP}	PROGRAMMING VOLTAGE

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output Voltages with respect to Ground	-0.6 to + 7.0	V
V_{PP}	Supply Voltage with respect to Ground	-0.6 to + 14.0	V
V_{A9}	Voltage on A9 with respect to Ground	-0.6 to + 13.5	V
V_{CC}	Supply Voltage with respect to Ground	-0.6 to + 7.0	V
T_{bias}	Temperature range under bias	-50 to + 125	°C
T_{stg}	Storage temperature range	- 65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	OUTPUT
READ	L	L	X	X	X	D_{OUT}
OUTPUT DISABLE	L	H	X	X	X	HIGH Z
STANDBY	H	X	X	X	X	HIGH Z
PROGRAM	L	H	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE : X = Don't Care ; VH = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION
DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for O°C to 70°C Oper. Temp. Range)	**12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC} Power Supply (1)	5V ± 5%		5V ± 10%	

DC AND OPERATING CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		35	mA
I_{CC2}	VCC Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	VCC Standby Current - CMOS	$\overline{CE}$ > V_{CC} -0.2 V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input low voltage		-0.3	0.8	V
V_{IH}	Input high voltage		2.0	V_{CC}+ 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC} - 0.7		V V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C2001								Unit
			-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		50		60		70		100	ns
t_{DF} (2)	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	40	0	50	0	60	0	60	ns
t_{OH}	Output hold from address	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		ns

CAPACITANCE (3)
(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} Must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Output Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2v - Outputs : 0.8 and 2v

Figure 3 : AC Testing input/Output Waveform

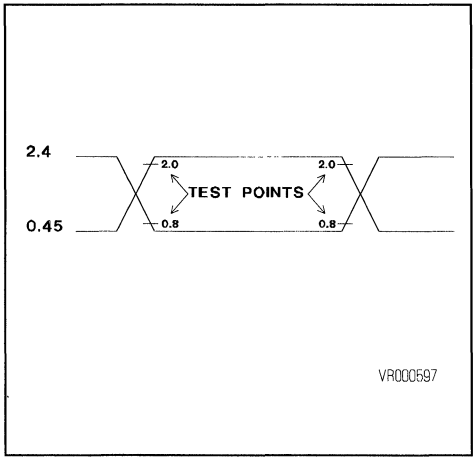


Figure 4 : AC Testing Load Circuit

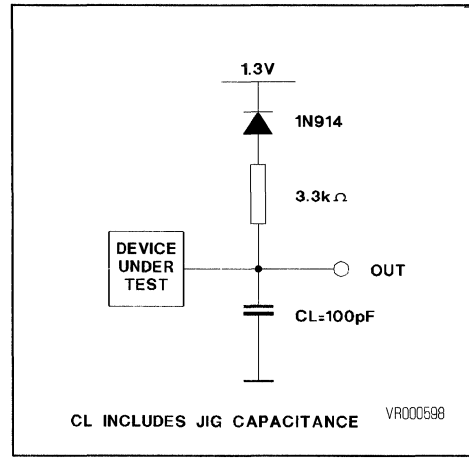
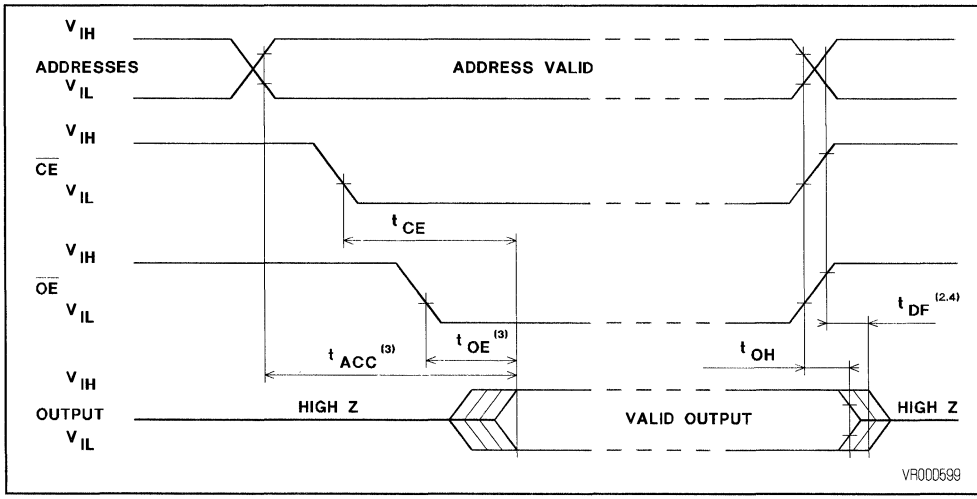


Figure 5 : AC Waveforms



NOTES :
1. Typical values are for TA = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t$\overline{CE}$ - t$\overline{OE}$ after the falling edge $\overline{CE}$ without impact on t$\overline{CE}$.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

READ MODE

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C2001 has a standby mode which reduces the active current from 35 mA to 0.2 mA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current,Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between Vcc and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and GND for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{pp} pin will permanently damage the M27C2001.

When delivered (and after each erasure for UV EPROM), all bits of the M27C2001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C2001 is in the programming mode when Vpp input is at 12.75V, and $\overline{CE}$ and PGM are at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. Vcc is specified to be 6.25V ± 0.25V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C2001s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C2001 may be common. A TTL low level pulse applied to a M27C2001's $\overline{CE}$ input, with PGM low and V_{PP} at 12.75V, will program that M27C2001. A high level $\overline{CE}$ input inhibits the other M27C2001s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, PGM at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. this mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C2001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C2001 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C2001, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C2001 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C2001 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C2001 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	1	1	0	0	0	0	1	61

NOTE : A9 = 12V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$; A1 to A8 = A10 to A17 = V_{IL} ; $V_{PP} = V_{CC} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = 0V to V_{CC}	-10	+10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

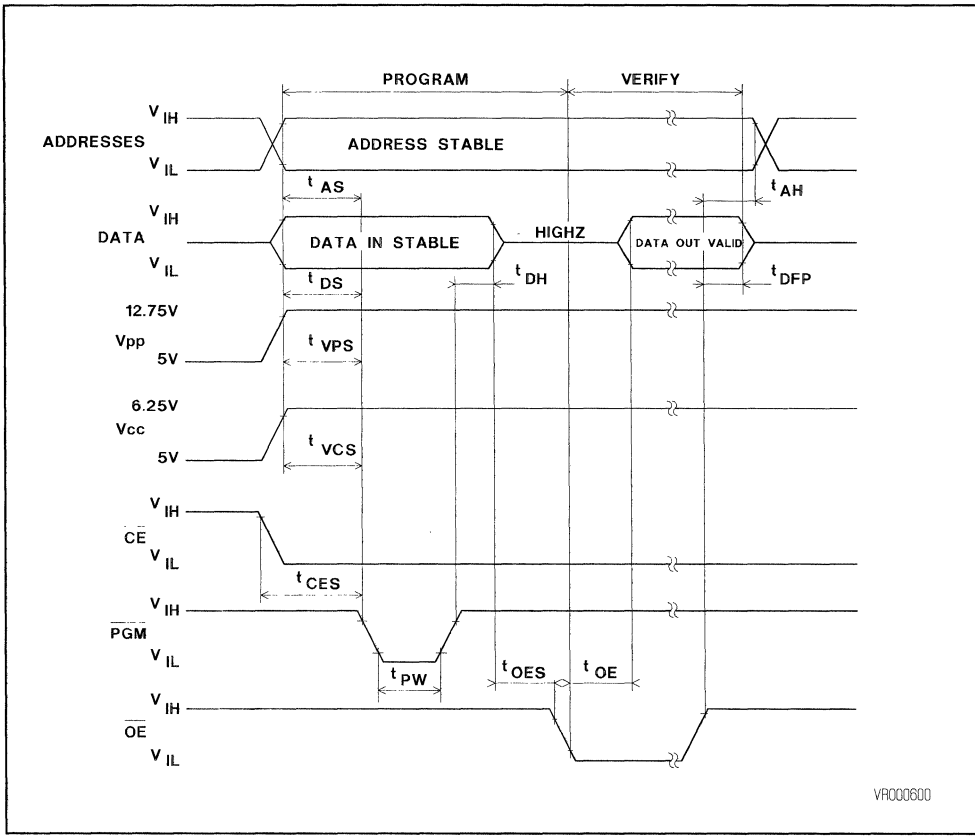
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

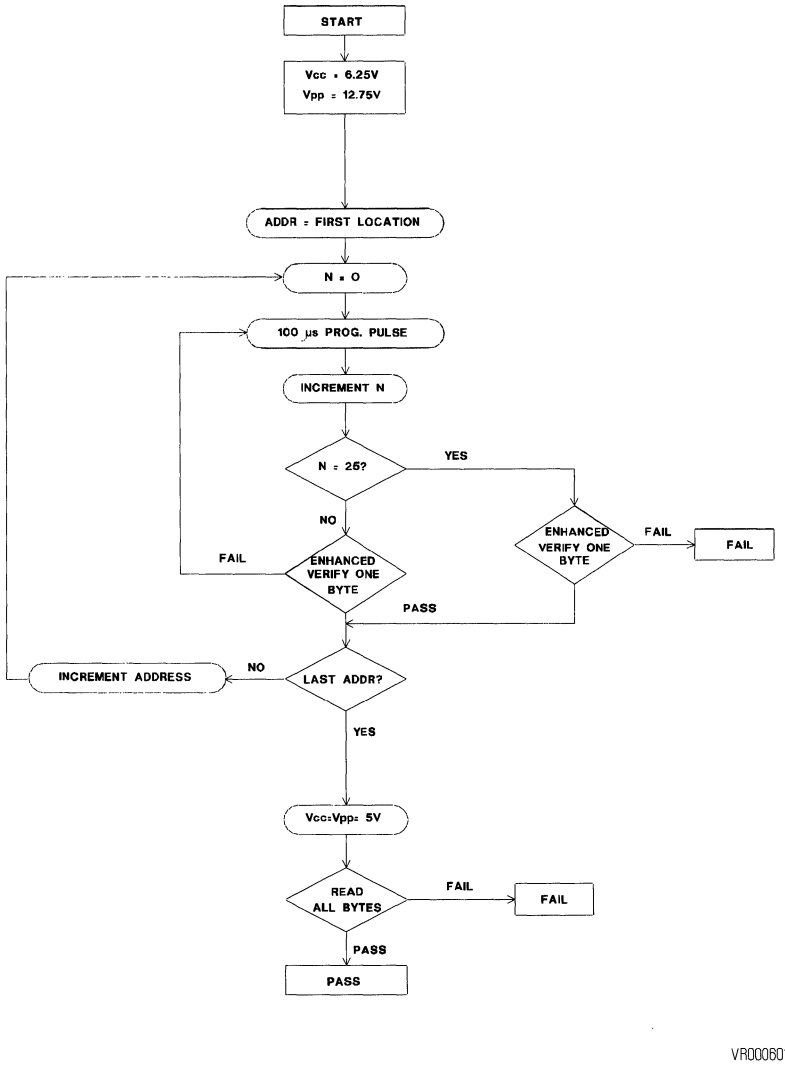
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C2001 a 0.1 µF capacitor is required accross V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart

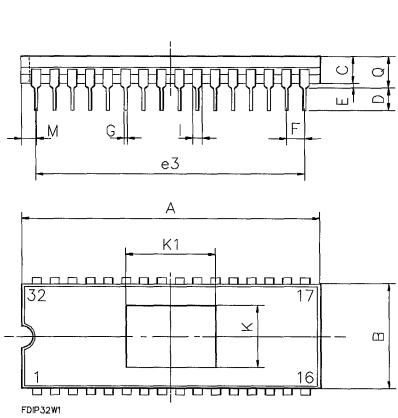


ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M27C2001-12XF1	120 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C2001-15XF1	150 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C2001-15F1	150 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C2001-20F1	200 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C2001-25F1	250 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C2001-15XF6	150 ns	5V ± 5 %	-40 to + 85°C	FDIP32-W

PACKAGE MECHANICAL DATA

Figure 8 : 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL

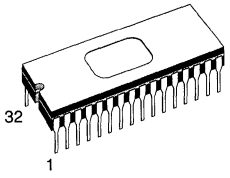


Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			42.78			1.684
B	14.50		14.90	0.570		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.20		0.070
e3		38.10			1.500	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
K	8.30		8.70	0.327		0.343
K1	12.30		12.70	0.484		0.504

4096K (512K x 8) CMOS UV EPROM

PRELIMINARY DATA

- VERY FAST ACCESS TIME : 100ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 70mA at 10 MHz
  - Standby current 100µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 48 SECONDS (PRESTO II ALGORITHM).



FDIP32-W

(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C4001 is a high speed 4,194,304 (organized as 524,288 x 8 bit) ultraviolet erasable and programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

It is housed in a 32 pin Ceramic Frit Seal Window package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

PIN FUNCTIONS

A0-A18	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
O0-O7	DATA INPUT/OUTPUT
V_{PP}	PROGRAMMING VOLTAGE
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Connection

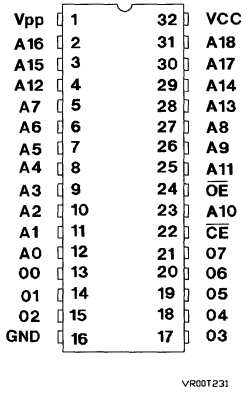
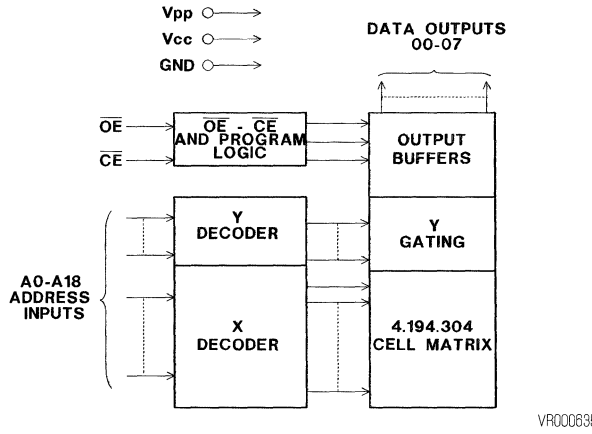


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output Voltages with respect to Ground	-0.6 to + 7.0	V
V_{PP}	Supply Voltage with respect to Ground	-0.6 to + 14.0	V
V_{A9}	Voltage on A9 with respect to Ground	-0.6 to + 13.5	V
V_{CC}	Supply Voltage with respect to Ground	-0.6 to + 7.0	V
T_{bias}	Temperature range under bias	-10 to + 125	°C
T_{stg}	Storage temperature range	- 65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$	A9	VPP	OUTPUT
READ	L	L	X	X	D_{OUT}
OUTPUT DISABLE	L	H	X	X	HIGH Z
STANDBY	H	X	X	X	HIGH Z
PROGRAM	L	H	X	V_{PP}	D_{IN}
PROGRAM VERIFY	H	L	X	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	H	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	V_{CC}	CODE

NOTE : X = Don't Care ; V_H = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION
DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**-10XF1, 12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC} Power Supply	5V ± 5%		5V ± 10%	

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-1	1	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} , I_{OUT}= 0 mA (F = 10MHz)		70	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		50	mA
I_{CC2}	VCC Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	VCC Standby Current - CMOS	$\overline{CE}$ > V_{CC} -0.2V		100	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC} - 0.7		V V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C4001										Unit
			-10		-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		100		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		100		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		50		60		60		70		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	30	0	40	0	50	0	80	0	80	ns
t_{OH}	Output hold from address	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE[3]
(T_A = 25°C 1, f = 1MHz)

Symbol	Parameter	Test Condition	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

NOTES : 1. V_{CC} Must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Output Rise and Fall Times : ≤ 20 ns
Input Pulse Levels : 0.45 to 2.4V
Timing Measurement Reference Levels :
Inputs : 0.8 and 2V- Outputs : 0.8 and 2V

Figure 3 : AC Testing input/Output Waveform

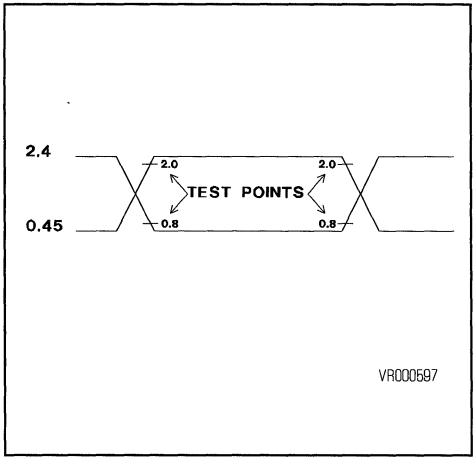


Figure 4 : AC Testing Load Circuit

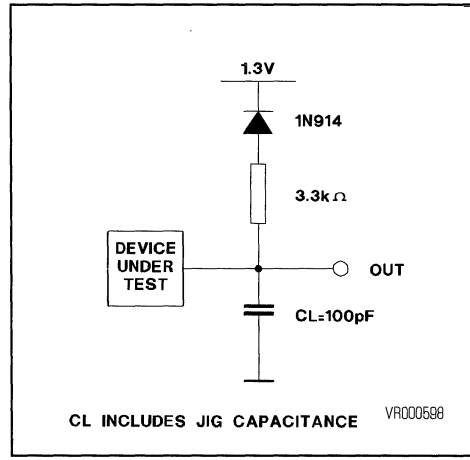
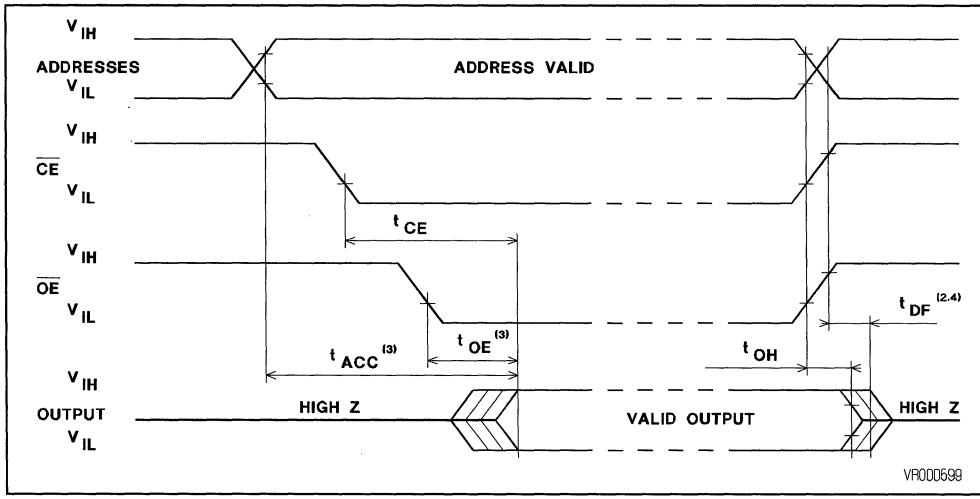


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to $t\overline{CE}$ - $t\overline{OE}$ after the falling edge $\overline{CE}$ without impact on $t\overline{CE}$.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C4001 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27C4001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C4001 has a standby mode which reduces the active current from 50mA to 0.1mA. The M27C4001 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices.

The supply current, Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between Vcc and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{PP} pin will permanently damage the M27C4001.

When delivered (and after each erasure for UV EPROM), all bits of the M27C4001 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C4001 is in the programming mode when V_{PP} input is at 12.75V, and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 48 seconds. Programming with PRESTO II consists of applying a sequence of 100 microseconds program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C4001s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C4001 may be common. A TTL low level pulse applied to a M27C4001's $\overline{CE}$ input, with V_{PP} at 12.75V, will program that M27C4001. A high level $\overline{CE}$ input inhibits the other M27C4001s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4001. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4001 with $V_{PP} = V_{CC} = 5V$. Two iden-tifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M27C4001, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C4001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C4001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4001 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4001 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm2 power rating. The M27C4001 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	1	0	0	0	0	0	1	41

NOTE : A9 = 12V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$; A1 to A8 = A10 to A18 = V_{IL} ; $V_{CC} = V_{PP} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25V, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = 0V to V_{CC}	-10	+10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

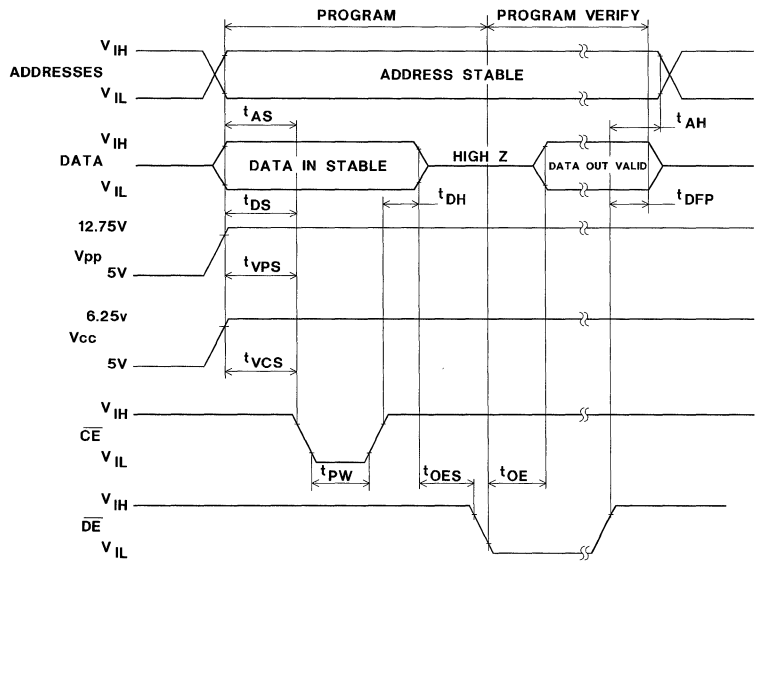
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from OE			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

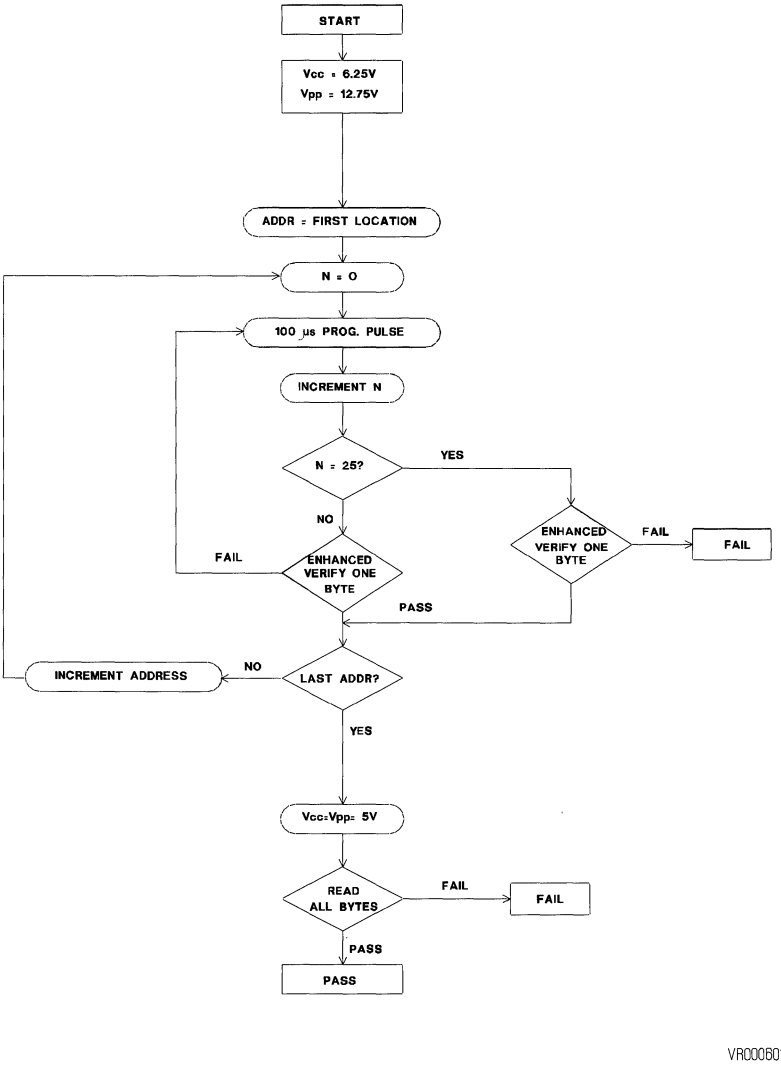
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C4001 a 0.1µF capacitor is required accross V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart

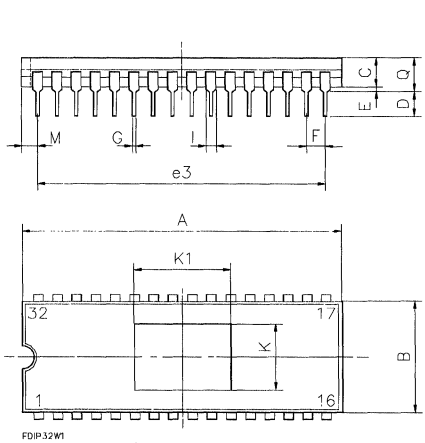


ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M27C4001-10XF1	100 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C4001-12XF1	120 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C4001-15XF1	150 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C4001-20XF1	200 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C4001-25XF1	250 ns	5V ± 5 %	0 to + 70°C	FDIP32-W
M27C4001-12F1	120 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C4001-15F1	150 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C4001-20F1	200 ns	5V ± 10 %	0 to + 70°C	FDIP32-W
M27C4001-25F1	250 ns	5V ± 10 %	0 to + 70°C	FDIP32-W

PACKAGE MECHANICAL DATA

Figure 8 : 32-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)

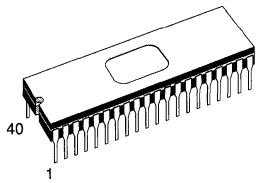


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			42.78			1.684
B	14.50		14.90	0.570		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		38.10			1.500	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
K	9.10		9.70	0.358		0.382
K1	10.6		11.3	0.417		0.445

4096K (256K x 16) CMOS UV EPROM

PRELIMINARY DATA

- VERY FAST ACCESS TIME : 100ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 70mA at 10 MHz
  - standby current 100µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 24 SECONDS (PRESTO II ALGORITHM).



FDIP40-W

(Ordering information at the end of the datasheet)

DESCRIPTION

The M27C4002 is a high speed 4,194,304 (organized 262,144 x 8) bit ultraviolet erasable and programmable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

It is housed in a 40 pin Window Ceramic Frit Seal package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written in the device by following the programming procedure.

PIN FUNCTIONS

A0-A17	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
O0-O15	DATA INPUT/OUTPUT
V_{PP}	PROGRAMMING VOLTAGE
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Connection

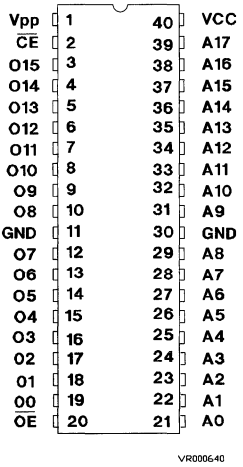
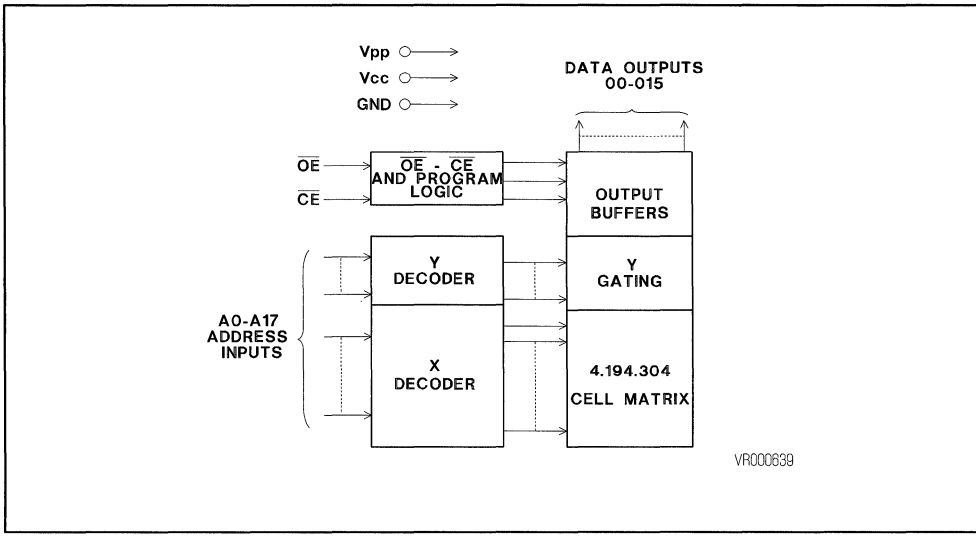


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output Voltages with respect to Ground	-0.6 to + 7.0	V
V_{PP}	Supply Voltage with respect to Ground	-0.6 to + 14.0	V
V_{A9}	Voltage on A9 with respect to Ground	-0.6 to + 13.5	V
V_{CC}	Supply Voltage with respect to Ground	-0.6 to + 7.0	V
T_{bias}	Temperature range under bias	-10 to + 125	°C
T_{stg}	Storage temperature range	- 65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	OUTPUT
READ	L	L	X	X	D_{OUT}
OUTPUT DISABLE	L	H	X	X	HIGH Z
STANDBY	H	X	X	X	HIGH Z
PROGRAM	L	H	X	V_{PP}	D_{IN}
PROGRAM VERIFY	H	L	X	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	H	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	VCC	CODE

NOTE : X = Don't Care ; VH = 12V ± 0.5V ; H = High ; L = Low

READ OPERATION
DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**10XF1, 12XF1, 15XF1, 20XF1, 25XF1**		**12F1, 15F1, 20F1, 25F1**	
V_{CC} Power Supply (1)	5V ± 5%		5V ± 10%	

NOTE : "F" Stands for Ceramic package.

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	1	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}	-1	1	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 10MHz)		70	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (F = 5 MHz)		50	mA
I_{CC2}	VCC Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	VCC Standby Current - CMOS	$\overline{CE}$ > V_{CC} -0.2 V		100	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC} - 0.7		V V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C4002										Unit
			-10		-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$=$\overline{OE}$=V_{IL}		100		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$=V_{IL}		100		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$=V_{IL}		50		60		60		70		100	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE}$=V_{IL}	0	30	0	40	0	50	0	80	0	80	ns
t_{OH}	Output hold from address	$\overline{CE}$=$\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE(3)
(T_A = 25°C f = 1MHz)

Symbol	Parameter	Test Condition	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output float is defined as the point where data is no longer driven (see timing table).
3. This parameter is only sampled and not 100 % tested.

AC TEST CONDITIONS

Output Rise and Fall Times : ≤ 20 ns

Input Pulse Levels : 0.45 to 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8 and 2V - Outputs : 0.8 and 2V

Figure 3 : AC Testing input/Output Waveform

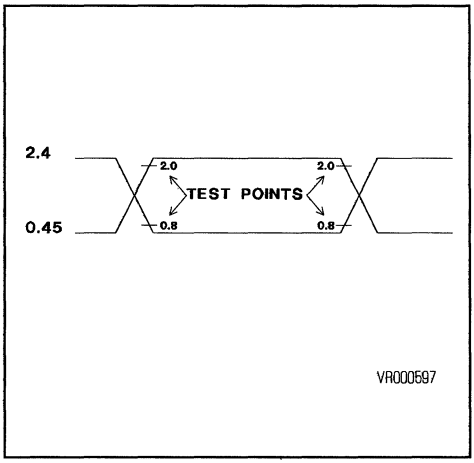


Figure 4 : AC Testing Load Circuit

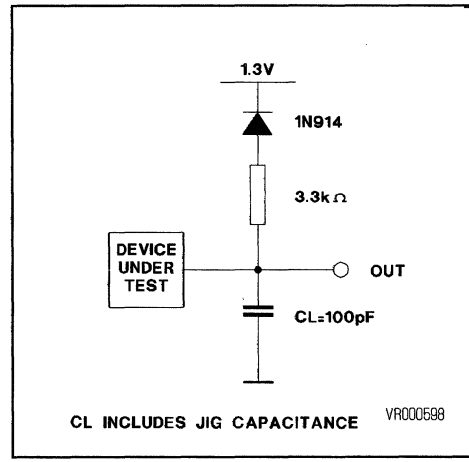
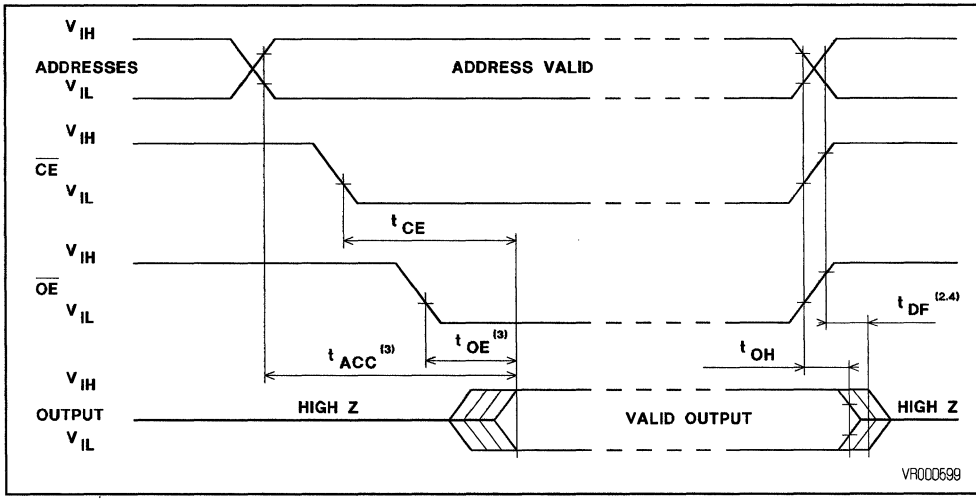


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for TA = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. OE may be delayed up to tCE - tOE after the falling edge CE without impact on tCE.
4. t_{DF} is specified from OE or CE whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C4002 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

READ MODE

The M27C4002 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C4002 has a standby mode which reduces the active current from 50mA to 0.1mA. The M27C4002 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices.

The supply current, Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of CE. The magnitude of the transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on V_{pp} pin will permanently damage the M27C4002.

When delivered (and after each erasure for UV EPROM), all bits of the M27C4002 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C4002 is in the programming mode when Vpp input is at 12.75V, and CE is at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. Vcc is specified to be 6.25V ± 0.25V.

PRESTO II PROGRAMMING ALGORITHM

PRESTO II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 24 seconds. Programming with PRESTO II consists of applying a sequence of 100 microsecond program pulses to each byte until a correct verify occurs. During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides necessary margin to each programmed cell.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27C4002s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}$ of the parallel M27C4002 may be common. A TTL low level pulse applied to a M27C4002's $\overline{CE}$ input, with V_{PP} at 12.75V, will program that M27C4002. A high level $\overline{CE}$ input inhibits the other M27C4002s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C4002. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C4002 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C4002, these two identifier bytes are given here below, and can be readout on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C4002 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C4002 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C4002 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C4002 window to prevent unintentional erasure. The recommended erasure procedure for the M27C4002 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm2 power rating. The M27C4002 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	1	0	0	0	1	0	0	44

NOTE : A9 = 12.0V ± 0.5V ; $\overline{CE} = \overline{OE} = V_{IL}$; A1 to A8 = A10 to A17 = V_{IL} ; $V_{CC} = V_{PP} = 5V$

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC}[1] = 6.25V ± 0.25, V_{PP}[1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
I_{LI}	Input Current (All Inputs)	V_{IN} = 0V to V_{CC}	-10	+10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = -400µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (program)	$\overline{CE}$ = V_{IL}		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

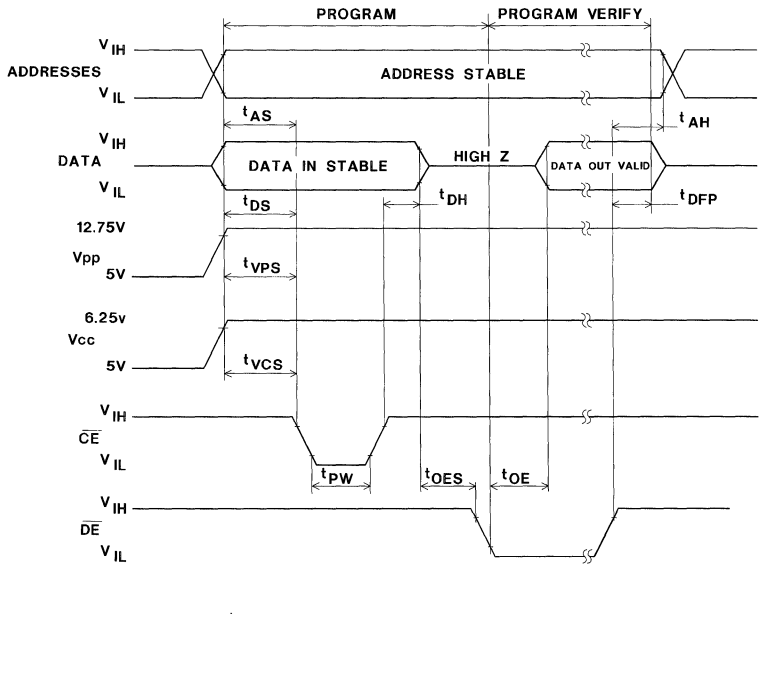
AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
$t_{DFP(2)}$	Outpout Enable Output Float Delay		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	Initial Program Pulse Width		95	105	µs
t_{OE}	Data Valid from OE			100	ns

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING OPERATION (Continued)

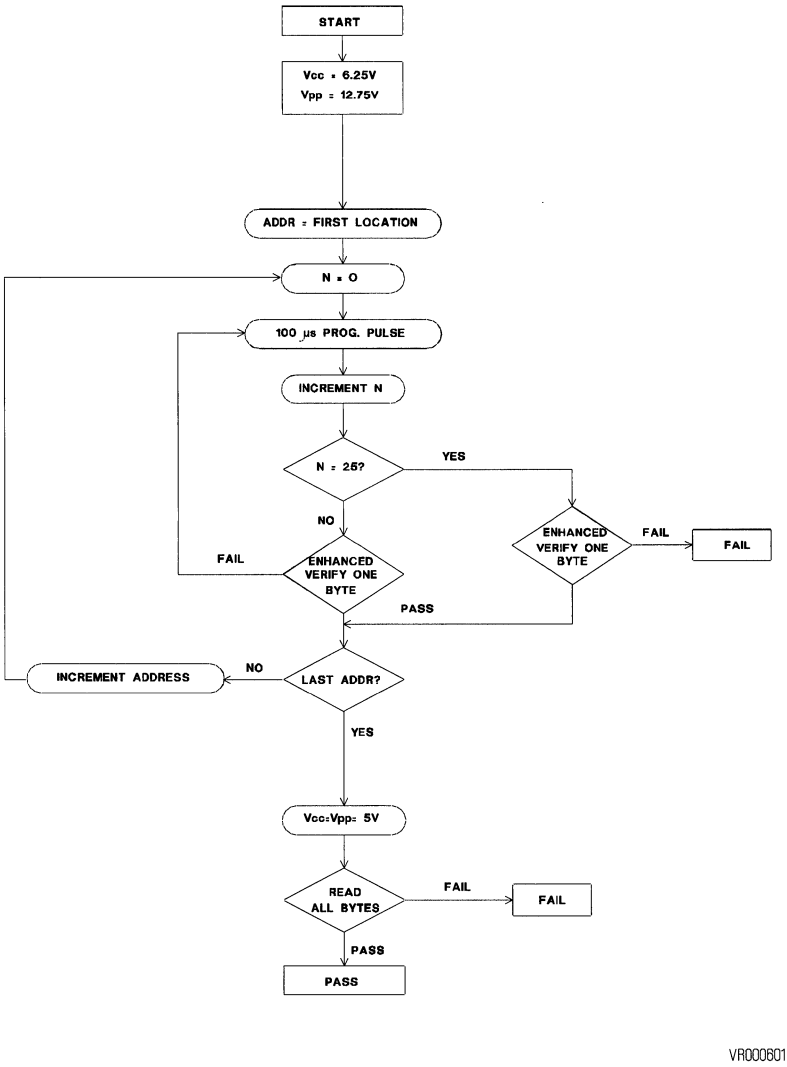
Figure 6 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C4002 a 0.1µF capacitor is required accross V_{PP} and GND to suppress spurious voltage transients which can damage the device.

PROGRAMMING OPERATION (Continued)

Figure 7 : PRESTO II Programming Algorithm Flow Chart

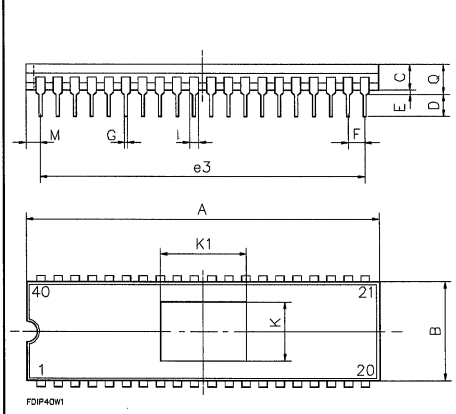


ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M27C4002-10XF1	100 ns	5V +/- 5 %	0 to + 70°C	FDIP40-W
M27C4002-12XF1	120 ns	5V +/- 5 %	0 to + 70°C	FDIP40-W
M27C4002-15XF1	150 ns	5V +/- 5 %	0 to + 70°C	FDIP40-W
M27C4002-20XF1	200 ns	5V +/- 5 %	0 to + 70°C	FDIP40-W
M27C4002-25XF1	250 ns	5V +/- 5 %	0 to + 70°C	FDIP40-W
M27C4002-12F1	120 ns	5V +/- 10 %	0 to + 70°C	FDIP40-W
M27C4002-15F1	150 ns	5V +/- 10 %	0 to + 70°C	FDIP40-W
M27C4002-20F1	200 ns	5V +/- 10 %	0 to + 70°C	FDIP40-W
M27C4002-25F1	250 ns	5V +/- 10 %	0 to + 70°C	FDIP40-W

PACKAGE MECHANICAL DATA

Figure 8 : 40-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL (F)



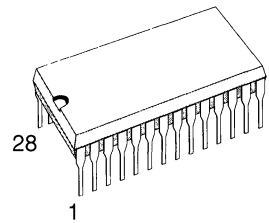
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			53.40			2.102
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	40			0.134		
E	1.50		1.78	0.020		0.070
e3		48.26			1.900	
F	2.29		2.79	0.090		0.110
G	.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N		–	–	–	–	–
N1	0 °		10 °	0 °		10 °
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
K	9.1		9.7	0.358		0.382
K1	10.6		11.3	0.417		0.445

FDIP40W1

MASK ROM

512K (64K x 8) CMOS ROM

- VERY FAST ACCESS TIME : 100 ns (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 40mA Max
  - Stand by current 20µA Max
- SINGLE +5V ± 10% POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH $\overline{CE}$.
- AUTOMATIC POWER DOWN.



PDIP-28

(Ordering information at the end of the datasheet)

DESCRIPTION

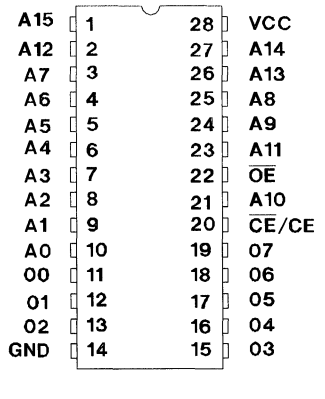
The M23C512 is a 524,288 bit, CMOS Masked Read Only Memory (ROM), organized as 65,536 x 8 bits. It is manufactured in 1.2 micron CMOS technology : Very fast access time of 100 ns makes it ideal for EPROM replacement on high performance, high volume running applications. This device features a Two Line Control system : Chip select line (CE) is active low or active high by mask programming, as per user's choice. When not active, it brings the device into standby mode, making it suitable for battery operated systems. Output Enable is to be used for Output control.

After cycle completion and 50ns without input change, the M23C512 automatically goes into power-down mode (I_{CC} = 1 mA), the data remaining latched on the output.

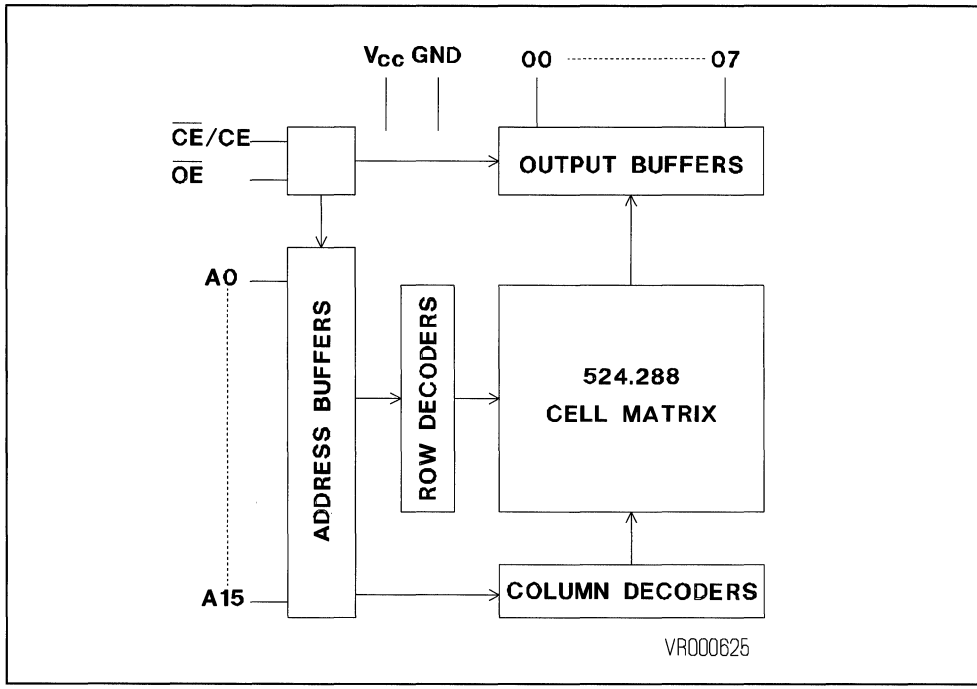
PIN FUNCTIONS

A0-A15	ADDRESS INPUTS
O0-O7	DATA OUTPUTS
$\overline{CE}$ / CE	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Connection



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage with respect to Ground	-0.5 to +7.0	V
Vi	Input or Output voltages with respect to Ground	-0.5 to +7.0	V
Tamb	Operating temperature range	0 to +70	°C
Tbias	Temperature range under bias	0 to + 125	°C
Tstg	Storage temperature	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation to these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

AC TEST CONDITIONS

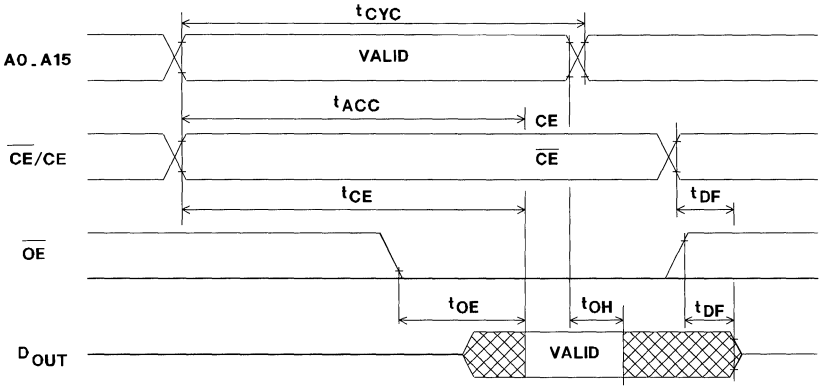
Input Rise and Fall Times : ≤ 10 ns

Input Levels : 0.45V and 2.4V

Timing Measurement Reference Levels :

Inputs : 0.8V and 2.0V - Outputs : 0.8V and 2.0V

TIMING WAVEFORMS



OPERATION MODES

MODE	$\overline{CE}$	or (CE)	$\overline{OE}$ (Note 1)	OUTPUT
READ	L	(H)	L	D_{OUT}
STANDBY	H	(L)	X	HIGH Z
OUTPUT DISABLE	L	(H)	H	HIGH Z

DC CHARACTERISTICS

T_{AMB} = 0°C to 70°C V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Value		Unit
			Min	Max	
I_{LI}	Input Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 10 MHz)		40	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 5 MHz)		20	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2V		20	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High voltage		2.0	V_{CC} + 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 3.2 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 uA	2.4		V

NOTE 1 : OE may be active high by mask programming.

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
T_{CYC}	Cycle Time			100	ns
T_{ACC}	Address Access Time	$\overline{CE} = V_{IL}$		100	ns
T_{CE}	Chip Enable Access Time	$\overline{CE} = V_{IL}$		100	ns
T_{OE}	Output Enable Access Time	$\overline{CE} = \overline{OE} = V_{IL}$		50	ns
T_{DF} (1)	$\overline{CE}$ High to Output float			30	ns
T_{OH}	Output Hold		10		ns

CAPACITANCE (1)

(T_{AMB} = 25°C f = 1 MHz)

Symbol	Parameter	Test Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5 pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5 pF

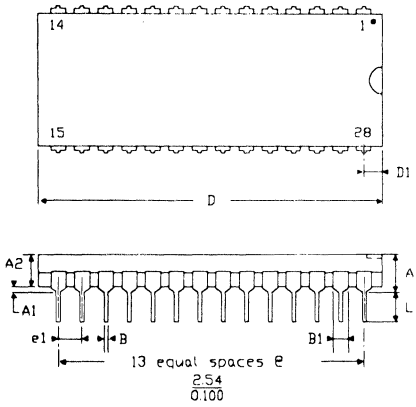
NOTE 1 : This parameter is only sampled and not 100 % tested

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M23C512B1	100 ns	5V ± 10%	0 to +70°C	PDIP28

PACKAGE MECHANICAL DATA

28-PIN -PLASTIC DIP

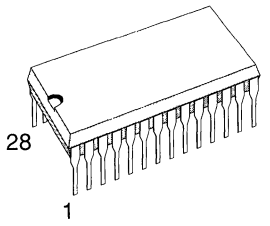


VR000287

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

1024K (128K x 8) CMOS ROM

- VERY FAST ACCESS TIME : 100 ns (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 40 mA Max.
  - Stand by current 20 µA Max.
- SINGLE +5V ± 10% POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH $\overline{CE}$.
- AUTOMATIC POWER DOWN.



PDIP-28

(Ordering information at the end of the datasheet)

DESCRIPTION

The M23C1000 Is a 1,048,576 bit, CMOS Masked Read Only Memory (ROM), organized as 131,072 x 8 bits. It is manufactured in 1.2 micron CMOS technology : Very fast access time of 100 ns makes it ideal for EPROM replacement on high performance, high volume running applications. Chip select line ($\overline{CE}$) is active low or active high by mask programming, as per user's choice. When not active, it brings the device into standby mode, suitable for battery operated systems.

After cycle completion and 50 ns without input change, the M23C1000 automatically goes in power-down mode (I_{CC} = 1 mA), the data remaining latched on the output.

PIN FUNCTIONS

A0-A16	ADDRESS INPUTS
00-07	DATA OUTPUTS
$\overline{CE}$ / CE	CHIP ENABLE INPUT
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Connection

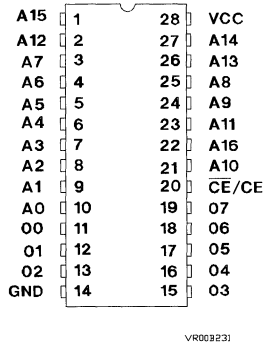
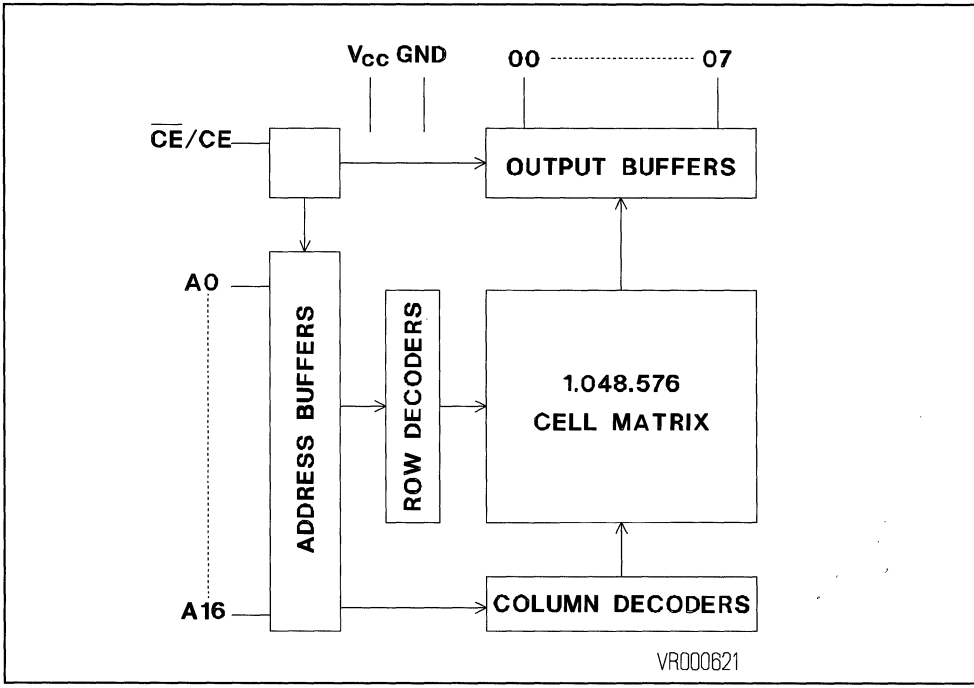


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage with respect to Ground	-0.5 to + 7.0	V
Vi	Input or Output voltage with respect to Ground	-0.5 to + 7.0	V
Tamb	Operating temperature range	0 to + 70	°C
Tbias	Temperature range under bias	0 to + 125	°C
Tstg	Storage temperature	-65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation to these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

AC TEST CONDITION

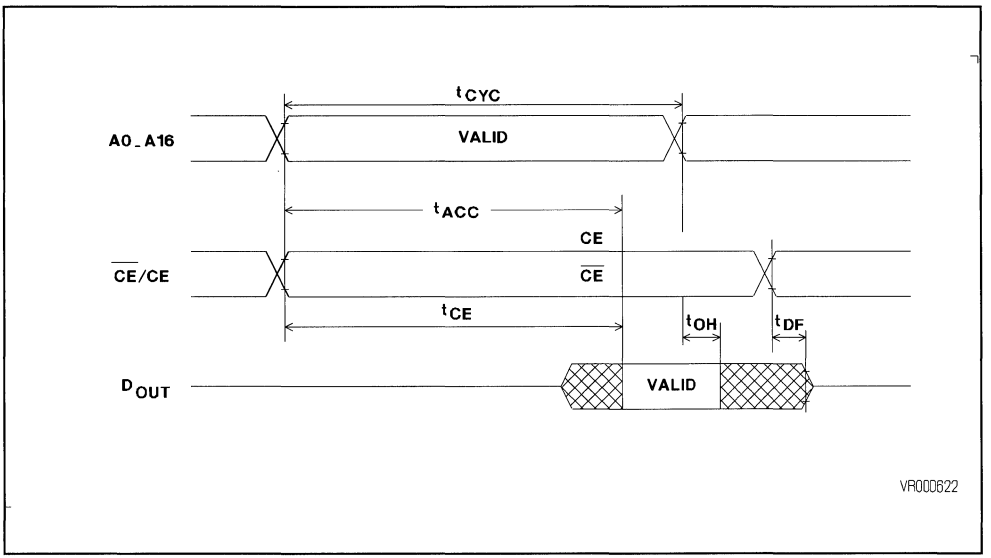
Input Rise and Fall times : ≤ 10 ns

Input Levels : 0.45V and 2.4V

Timing measurement Reference Levels :

Inputs : 0.8V and 2.0V - Outputs : 0.8V and 2.0V

Figure 3 : Timing Waveforms



OPERATION MODES

MODE	$\overline{CE}$	or (CE)	OUTPUTS
READ	L	(H)	D_{OUT}
STANDBY / OUTPUT DISABLE	H	(L)	HIGH Z

DC CHARACTERISTICS

T_{AMB} = 0°C to 70°C V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 10 MHz)		40	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 5 MHz)		20	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2 V		20	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High voltage		2.0	V_{CC} + 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 3.2 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 uA	2.4		V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
T_{CYC}	Cycle Time			100	ns
T_{ACC}	Address Access Time	$\overline{CE} = V_{IL}$		100	ns
T_{CE}	Chip Enable Access Time	$\overline{CE} = V_{IL}$		100	ns
T_{DF} (1)	$\overline{CE}$ High to Output float			30	ns
T_{DH}	Output Hold		10		ns

CAPACITANCE (1)

T_{AMB} = 25°C f = 1 MHz

Symbol	Parameter	Test Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V		5 pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		5 pF

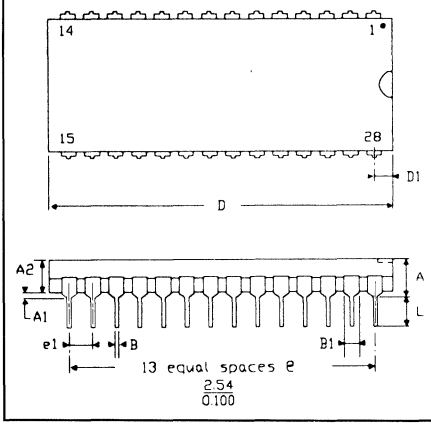
NOTE : (1) This parameter is only sampled and not 100 % tested

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M23C1000B1	100 ns	5 V ± 10%	0 to +70°C	PDIP28

PACKAGE MECHANICAL DATA

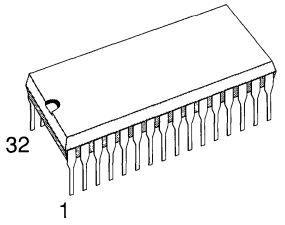
Figure 4 : 28-PIN - PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

1024K (128K x 8) CMOS ROM

- VERY FAST ACCESS TIME : 100 ns (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 40 mA Max.
  - Standby current 20 µA Max.
- SINGLE +5V ± 10% POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH $\overline{CE}$.
- AUTOMATIC POWER DOWN.



PDIP-32

(Ordering information at the end of the datasheet)

DESCRIPTION

The M23C1001 Is a 1, 048,576 bit, CMOS Masked Read Only Memory (ROM), organized as 131,072 x 8 bits. It is manufactured in 1.2 micron CMOS technology : Very fast access time of 100 ns makes it ideal for EPROM replacement on high performance, high volume running applications. Chip select line ($\overline{CE}$) is active low or active high by mask programming, as per user's choice When not active, it brings the device into standby mode making it suitable for battery operated systems.

After cycle completion and 50 ns without input change, the M23C1001 automatically goes into power-down mode (I_{CC} = 1 mA), the data remaining latched on the output.

PIN FUNCTIONS

A0-A16	ADDRESS INPUTS
00-07	DATA OUTPUTS
$\overline{CE}$ / CE	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Connection

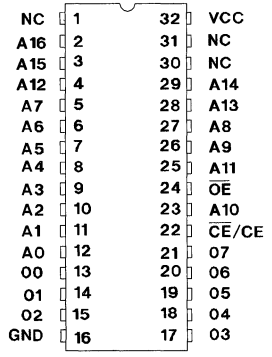
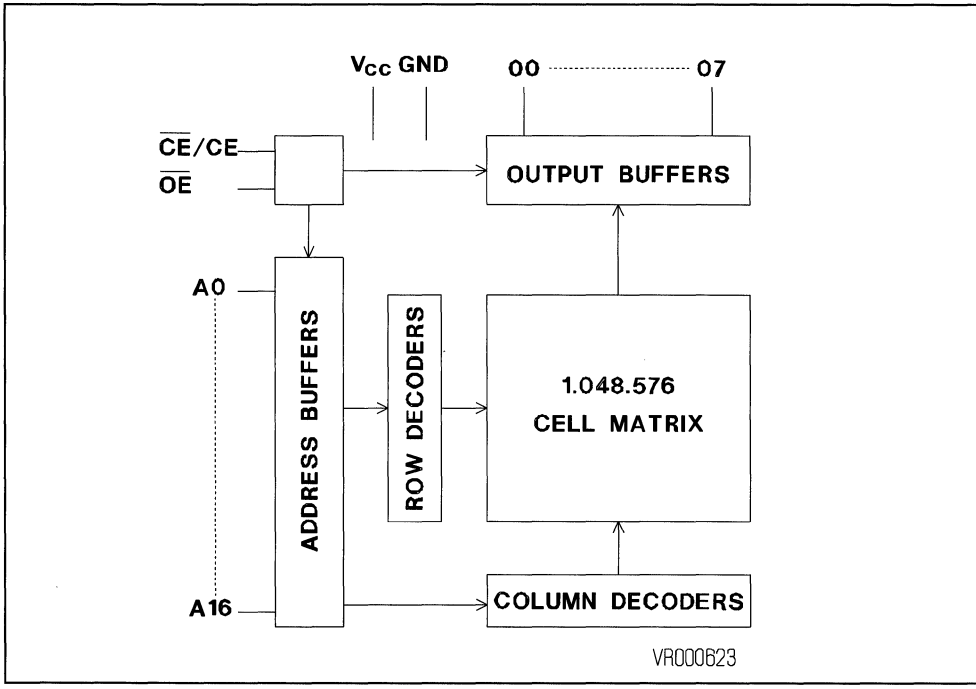


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage with respect to Ground	-0.5 to + 7.0	V
Vi	Input or Output voltage with respect to Ground	-0.5 to + 7.0	V
T_{amb}	Operating temperature range	0 to + 70	°C
T_{bias}	Temperature range under bias	0 to + 125	°C
T_{stg}	Storage temperature	-65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation to these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

AC TEST CONDITION

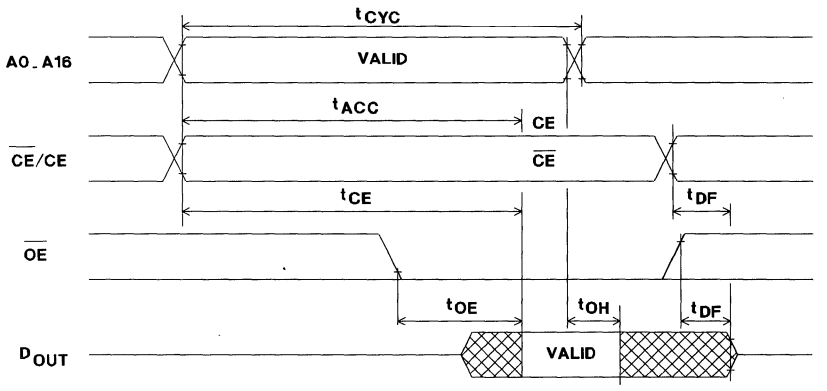
Input Rise and Fall Times : ≤ 10 ns

Input Levels : 0.45V and 2.4V

Timing measurement Reference Levels :

Inputs : 0.8V and 2.0V - Outputs : 0.8V and 2.0V

Figure 3 : Timing Waveforms



OPERATION MODES

MODE	$\overline{CE}$	or ($\overline{CE}$)	$\overline{OE}$ (Note 1)	OUTPUTS
READ	L	(H)	L	DOUT
STANDBY	H	(L)	X	HIGH Z
OUTPUT DISABLE	L	(H)	H	HIGH Z

DC CHARACTERISTICS

T_{AMB} = 0°C to 70°C V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 10 MHz)		40	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 5 MHz)		20	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2 V		20	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High voltage		2.0	V_{CC} + 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 3.2 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 uA	2.4		V

NOTE 1 : OE may be active high by mask programming.

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
T_{CYC}	Cycle Time			100	ns
T_{ACC}	Address Access Time	$\overline{CE}$ = V_{IL}		100	ns
T_{CE}	Chip Enable Access Time	$\overline{CE}$ = V_{IL}		100	ns
T_{OE}	Output Enable Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		50	ns
T_{DF} (1)	$\overline{CE}$ High to Output float			30	ns
T_{DH}	Output Hold		10		ns

CAPACITANCE (1)

T_{AMB} = 25°C f = 1 MHz

Symbol	Parameter	Test Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5 pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5 pF

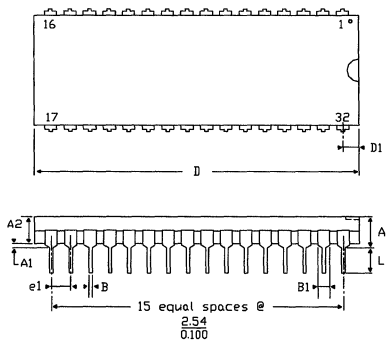
NOTE : (1) This parameter is only sampled and not 100 % tested

ORDERING INFORMATION

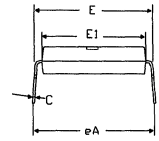
Part Number	Access Time	Supply Voltage	Temp.Range	Package
M23C1001 B1	100 ns	5 V ± -10%	0 to +70°C	PDIP32

PACKAGE MECHANICAL DATA

Figure 4 : 32-PIN - PLASTIC DIP



VR000288



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.38			0.015		
b		0.46			0.018	
b1	0.20		0.30	0.008		0.012
b2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e 3		35.60			1.400	
e 4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L	3.18		3.43	0.125		0.135

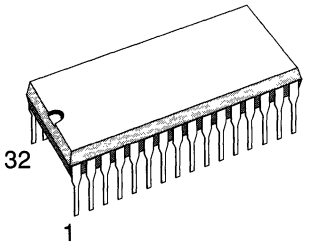
SGS-THOMSON MICROELECTRONICS

M23C2001

2048K (256K x 8) CMOS ROM

ADVANCE DATA

- VERY FAST ACCESS TIME : 120 ns (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 50 mA Max.
  - Stand by current 20 µA Max.
- SINGLE +5V ± 10 % POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH CE.
- AUTOMATIC POWER DOWN.

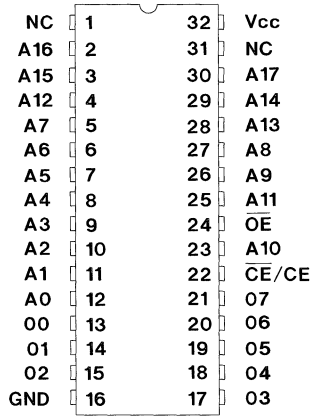


PDIP32
(Plastic Package)

DESCRIPTION

The M23C2001 is a 2,097,152 CMOS Masked Read Only Memory (ROM), organized as 262,144 x 8 bits. It is manufactured in 0.8 micron CMOS technology : Very fast access time of 120 ns makes it ideal for EPROM replacement on high performance, high volume running applications. Chip select line (CE) is active low or active high by mask programmation, as per user's choice. When not active, it brings the device in stand by mode, suitable on battery operated systems. Output Enable is to be used for Outputs control. After 50 ns without input change, the M23C2001 automatically goes in power-down (Icc1 = 1 mA), the data remaining latched on the outputs.

PIN CONNECTION



PIN NAMES

A0-A17	Address Inputs
O0-O7	Data Outputs
$\overline{CE}$/CE	Chip Enable Input
$\overline{OE}$	Output Enable
Vcc	+ 5V Power Supply
GND	Ground
NC	Not Connected

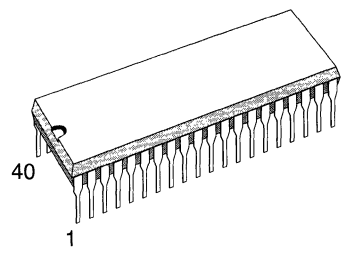
SGS-THOMSON MICROELECTRONICS

M23C4000

4096K (512K x 8 - 256K x 16) CMOS ROM

ADVANCE DATA

- BY 8 / BY 16 SOFTWARE CONFIGURATION.
- VERY FAST ACCESS TIME : 120 ns. (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 50 mA
  - Stand by current 20 µA
- SINGLE + 5V ± 10 % POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH CE.
- AUTOMATIC POWER DOWN.



PDIP40

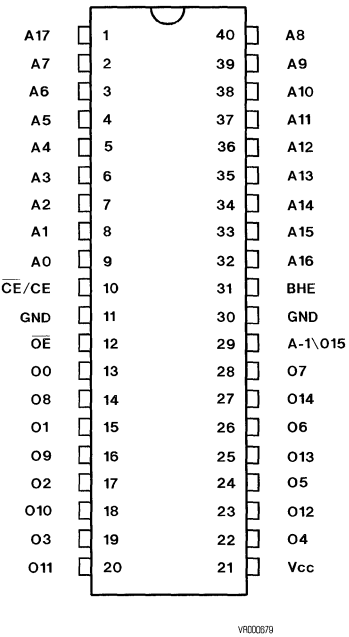
DESCRIPTION

The M23C4000 is a 4,194,304 CMOS Masked Read Only Memory (ROM), organized as 524,288 x 8 (BHE low, A-1/O15 is least significant address bit) or 262, 144 x 16 bits (BHE high, A-1/O15 is most significant data bit). It is manufactured in 0.8 micron CMOS technology : Very fast access time of 120 ns makes it ideal for EPROM replacement on high performance, high volume running applications. Chip select line (CE) is active low or active high by mask programmation, as per user's choice. When not active, it brings the device in stand by mode, suitable on battery operated systems. Output Enable is to be used for Outputs control. After cycle completion and 50 ns without input change, the M23C4000 automatically goes in power-down (Icc1 = 1 mA), the data remaining latched on the outputs.

PIN NAMES

A0-A17	ADDRESS INPUTS
A-1/O15	ADDRESS/DATA
O0-O14	DATA OUTPUTS
BHE	WORD/BYTE INPUT
$\overline{CE}$/CE	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
Vcc	+ 5V POWER SUPPLY
GND	GROUND

PIN CONNECTION



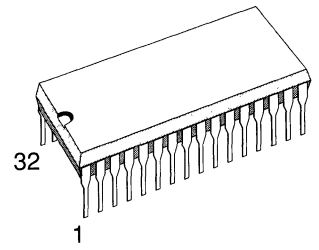
SGS-THOMSON MICROELECTRONICS

M23C4001

4096K (512K x 8) CMOS ROM

ADVANCE DATA

- VERY FAST ACCESS TIME : 120 ns.
  (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 50 mA
  - Stand by current 20 µA
- SINGLE + 5 V ± 10 % POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH CE.
- AUTOMATIC POWER DOWN.



PDIP 32

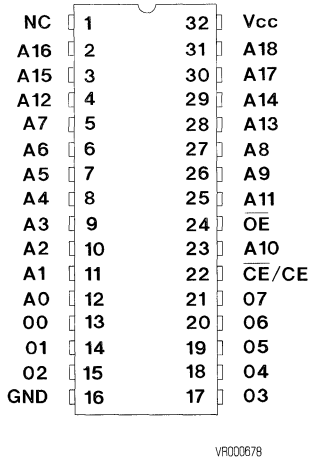
DESCRIPTION

The M23C4001 is a 4,194,304 CMOS Masked Read Only Memory (ROM), organized as 524,288 x 8 bits. It is manufactured in 0.8 micron CMOS technology : Very fast access time of 120ns makes it ideal for EPROM replacement on high performance, high volume running applications. Chip select line (CE) is active low or active high by mask programmation, as per user's choice. When not active, it brings the device in standby mode, suitable on battery operated systems. Output Enable is to be used for Outputs control. After cycle completion and 50 ns without input change, the M23C4001 automatically goes in power-down (Icc1 = 1 mA), the data remaining latched on the

PIN NAMES

A0-A18	ADDRESS INPUTS
O0-O7	DATA OUTPUTS
$\overline{CE}$/CE	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
Vcc	+ 5V POWER SUPPLY
GND	GROUND
NC	NON CONNECTED

PIN CONNECTION

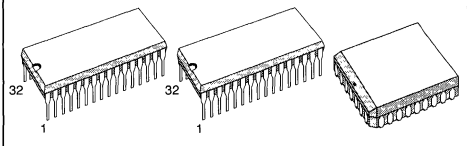


FLASH EPROM

256K (32 x 8) CMOS FLASH MEMORY

ADVANCE DATA

- FLASH ELECTRICAL CHIP ERASE IN 1 SECOND RANGE.
- PRESTO F PROGRAMMING TYPICAL BYTE PROGRAM TIME : 100 µs.
- 12 V VPP SUPPLY.
- 100 TO 10.000 ERASE/PROGRAM CYCLES.
- VERY FAST ACCESS TIME : 100 ns.
- LOW POWER CONSUMPTION : Maximum standby current : 100 µA.
- COMMAND REGISTER ARCHITECTURE FOR MICROPROCESSOR / MICROCONTROLLER COMPATIBLE WRITE INTERFACE.
- JEDEC STANDARD BYTE-WIDE EPROM PINOUTS.



FDIP 32 **PDIP32** **PLCC32**

(Ordering information at the end of the datasheet)

DESCRIPTION

SGS-THOMSON Microelectronics M28F256 FLASH Memory is an Electrically Chip-erasable and Reprogrammable non-volatile memory. Higher functionality and flexibility than EPROM come from the ability to be Chip-erased and reprogrammed in a test socket, in a PROM programmer socket, on board, or In-system. The M28F256 is suitable for applications where EEPROM functionality is not suitable or not cost effective, or for replacement of UV EPROM when UV erasure is impractical or time consuming. Pin assignment conforms to JEDEC standards for byte wide EPROMs. The High performance access time allows interface with most microcontrollers and microprocessors.

PIN NAMES

A0-A14	ADDRESS INPUT
O0-O7	DATA INPUT/OUTPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{PP}	ERASE/PROGRAM power supply
V_{CC}	5V ± 10 % POWER SUPPLY
GND	GROUND
NC (1)	NO INTERNAL CONNECTION

(1) Pin may be driven or left floating.

Figure 1: Pin Configuration

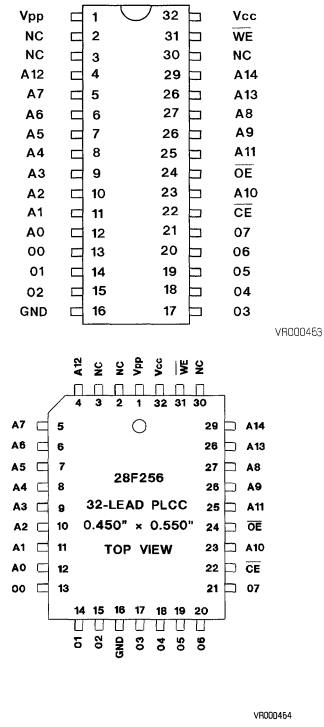


Figure 2 : M28F256 Block Diagram

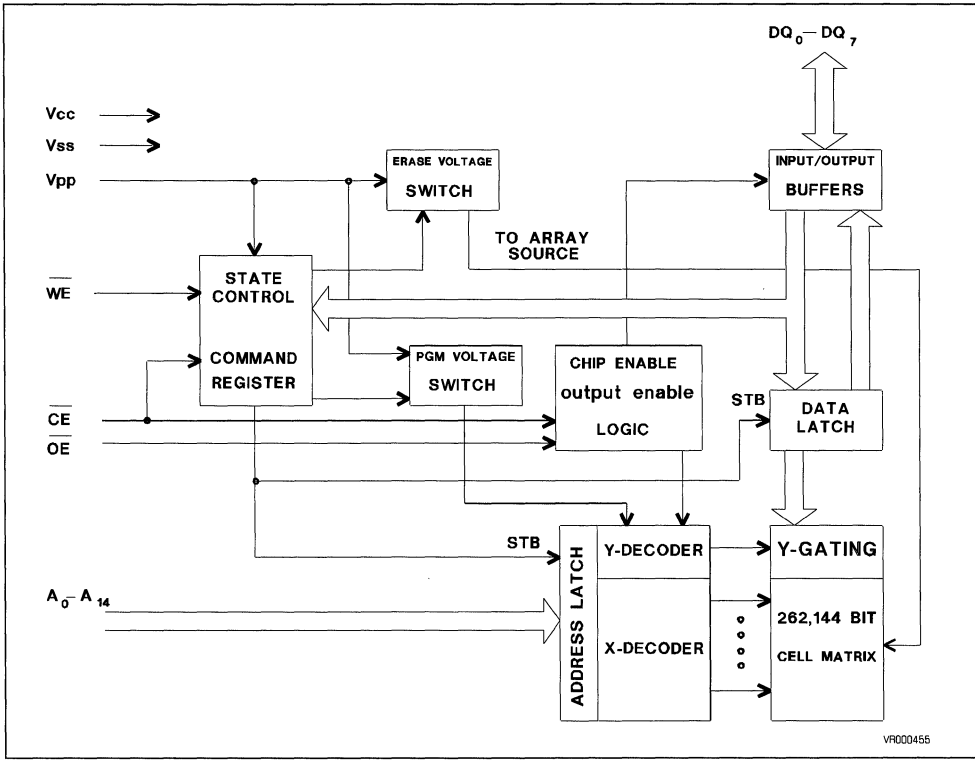


Table 3 : Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to 7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to 14	V
VA9	Voltage on A9 with respect to ground	-0.6 to 13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to 7.0	V
T_{bias}	Temperature Range under Bias	-10 to 80	°C
T_{stg}	Storage temperature range	-65 to 125	°C
TR_{op}	Operating Temperature during Read	0 to 70	°C
TEP_{op}	Operating Temperature during Erase / Program	0 to 70	°C

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4 : Bus Operation

PINS / OPERATIONS		V_{PP} (1)	A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	O0-O7
READ ONLY	READ	V_{PPL}	A0	A9	V_{IL}	V_{IL}	V_{IH}	DATA OUT
	OUTPUT DISABLE	V_{PPL}	X (7)	X	V_{IL}	V_{IH}	V_{IH}	TRI STATE
	STANDBY	V_{PPL}	X	X	V_{IH}	X	X	TRI STATE
	MANUFACTURER SIGNATURE (2)	V_{PPL}	VIL	V_{SI} (3)	V_{IL}	V_{IL}	V_{IH}	DATA = 20
	DEVICE SIGNATURE (2)	V_{PPL}	V_{IH}	V_{SI}	V_{IL}	V_{IL}	V_{IH}	DATA = A1 OR A8
READ/ WRITE	READ	V_{PPH}	A0	A9	VIL	V_{IL}	V_{IH}	DATA OUT (4)
	OUTPUT DISABLE	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	TRI STATE
	STANDBY (5)	V_{PPH}	X	X	V_{IH}	X	X	TRI STATE
	WRITE	V_{PPH}	A0	A9	V_{IL}	V_{IH}	V_{IL}	DATA IN (6)

Notes : (1) V_{PP} Low may be ground, a no connect with a resistor tied to ground, or < 8 volts. V_{PP} High is the programming voltage specified for the device. When $V_{PP} = V_{PPL}$ memory content can be read but not written or erased.
(2) Manufacturer and Device electronic Signature can be accessed also through Command Register (see table 5) Device code A8 requires V_{PPH} = 12V ± 5% . Device code A1 requires V_{PPH} = 12.75V ± 0.25V . All other addresses low.
(3) 11.5V < V_{SI} < 13V.
(4) When $V_{PP} = V_{PPH}$ read operation can be array data or Electronic Signature.
(5) When $V_{PP} = V_{PPH}$ Standby current is $I_{CC} + I_{PP}$ (Standby).
(6) Refer to table 5 for Data In during write.
(7) X can be V_{IL} or V_{IH}.

DEVICE OPERATION

PRINCIPLE

The added functionality of FLASH as compared to EPROM, is Electrical Erasure and Reprogramming. In order to manage this new functionality a command register is introduced. Some device functions are addressed via the command register, some not, depending on the V_{PP} pin voltage. When V_{PP} pin is at low voltage (< 8V), the M28F256 is a READ only memory. The command register is disabled. Manipulations of the external memory control pins yield the standard EPROM read, output disable, electronic signature and standby operations. Raising V_{PP} pin to High voltage, enables the command register for READ/WRITE operations. In addition, read, output disable, standby, electronic signature, ERASE and WRITE operations are allowed. At $V_{PP} = V_{PPH}$ the operating modes are addressed through the use of the command register.

Table 4 summarizes the Bus operations : at $V_{PP}=V_{PPL}$ only Read operations are allowed, at $V_{PP}=V_{PPH}$ Read operations and Erase/Write operations are allowed.

OPERATION MODES DESCRIPTION

A- OPERATION MODES WITH V_{PP} AT LOW VOLTAGE (< 8V)

READ MODE

The M28F256 has two control pins, both of which must be logically active in order to obtain data at the outputs.

Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Fig 7 illustrates read timing waveforms.

STANDBY MODE

The M28F256 has a standby mode which reduces the maximum active current from 30mA to 0.1mA. The device is placed in Standby mode by applying a high signal to the $\overline{CE}$ input. When in Standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input .

OUTPUT DISABLE

With $\overline{OE}$ at High level V_{IH}, output pins are placed in a high impedance state.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for use by programming equipment

to automatically match the device to be programmed or erased with its corresponding programming or erasing algorithm. This mode is activated by applying high voltage on address line A9 (11.5V - 13V) and by applying V_{IL} to CE and OE. Two identifier bytes may then be sequenced from the outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) represents the device identifier code. For the SGS-THOMSON Microelectronics M28F256, these two identifiers are given here below and can be read on outputs O0 to O7.

WRITE MODE

When V_{PP} is at low voltage, memory contents can not be written or erased. Write/Erased operations can only be accomplished via the command register when V_{PPH} is applied on V_{PP} pin.

ELECTRONIC SIGNATURE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE IDENTIFIER	V_{IH}	1	0	1	0	0	0	0	1	A1
	V_{IH}	1	0	1	0	1	0	0	0	A8

Notes : (1) A9 = 12.0V ± 0.5V ; $\overline{CE}$ = $\overline{OE}$ = V_{IL} ; V_{PP} = V_{PPL} ; A1 to A8= V_{IL} ; A10 to A14 = V_{IL}.
(2) Device code is either A8 if device requires V_{PP} = 12V ± 5% or A1 if device requires V_{PP} = 12.75V ± 0.25V.

Table 5 : COMMAND DEFINITIONS

COMMAND	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Operation (1)	Address (2)	Data (3)	Operation (1)	Address (2)	Data (3)
Read Memory	1	Write	X	00H			
Read Electronic Signature (4)	1	Write	X	90H	Read	IA	ID
Setup Erase/Erase (5)	2	Write	X	20H	Write	X	20H
Erase Verify (5)	2	Write	EA	A0H	Read	X	EVD
Setup program/Program (6)	2	Write	X	40H	Write	PA	PD
Program verify (6)	2	Write	X	C0H	Read	X	PVD
Reset (7)	2	Write	X	FFH	Write	X	FFH

Notes: (1) Bus operations are defined in table 4.
(2) IA = identifier address ; 0000H for manufacturer code and 0001H for device.
(3) EA = address of memory location to be read during erase verify.
PA = address of memory location to be programmed.
(4) ID = data read from location IA during electronic signature ; 20H = manuf ; A1H or A8H = device.
PD = data to be programmed at location PA. EVD = data read during from location EA during erase verify.
PVD Data read from location PA during program verify.
(5) See fig. 6 for erase algorithm.
(6) See fig. 4 for programming algorithm.
(7) The second bus cycle must be followed by the desired command register write.

B - OPERATION MODES WITH V_{PP} AT V_{PPH} - COMMAND REGISTER

At V_{PP} = V_{PPH}, Read/Write operations are enabled. Device operations are selected by writing specific data patterns into the command register using standard microprocessor write timings. The register contents are inputs for an internal state machine which controls erase and programming circuitry. Some commands require one write cycle, while others require two. The register is a latch used to store these commands and the data and address needed to execute the command.

(Note that the command register does not occupy an addressable memory location).

With this architecture, the device expects the first write cycle to be a command and does not corrupt data at specified address. The command register is written by bringing WE to V_{IL}, while CE is low. Addresses are latched on the falling edge of WE, while data are latched on the rising edge of WE pulse. Table 5 contains the list of register commands. The three high order register bits R7, R6 and R5 encode the control function. All other register bits R4-R0 must be at zero. Only exception is the reset command, when FFH is written into the command register. Register bits R7-R0 correspond to data inputs D7-D0. Note that when V_{PP} is at low voltage, the contents of the command register default to 00H enabling Read-Only operations. The command register is only alterable when V_{PP} is at high voltage. The system designer may choose to make the V_{PP} switchable or to make the V_{PP} constantly available. In the case of switchable V_{PP}, when V_{PP} is removed, the device defaults to Read Only memory. In the case of constantly available V_{PP}, all memory functions are performed via the command register.

READ MODE WITH V_{PP} = V_{PPH}

At V_{PP} = V_{PPH}, memory contents can be addressed via the read command 00H. Read mode is initiated by writing 00H into the command register. The microprocessor read cycles retrieve the array data. The device remains enabled for read operations until the command register contents are altered. The default contents of the command register upon power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. When V_{PP} is "Hardwired", the device powers-up and remains enabled for read operations until the command register contents are changed.

Refer to AC Read characteristics and waveforms for timing parameters (Fig 7,Table 9).

ELECTRONIC SIGNATURE WITH V_{PP} = V_{PPH}

In order for the M28F256 to be erased and programmed by the local CPU and thus to supplement the traditional PROM programming methodology, the manufacturer and device signature codes can be read via the command register. The operation is initiated by writing 90H to the register. Following the command write, a read cycle from address 0000H returns the manufacturer code of 20H. A read cycle from address 0001H returns the device code of A1 or A8. To terminate the operation, it is necessary to write another valid command into the register.

SET UP ERASE/ERASE MODE

Before erasure it is necessary to program all bytes to the same level (data 00H). Setup erase is a command-only operation that prepares the device for electrical erasure of all bytes in the array. The setup erase is performed by writing 20H to the command register. To begin chip erasure, the erase command (20H) must again be written to the register. The erase operation begins on the second command's rising edge of the WE pulse and terminates with the rising edge of the next WE pulse (i.e Erase Verify command). This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased. Refer to A.C Erase characteristics and waveforms for timing parameters (Fig 6, Fig 5, Table 10).

ERASE VERIFY MODE

The erase command erases all the bytes of the array in parallel. After each erase operation, all bytes must be verified to see if they are erased. The erase verify operation is initiated by writing A0H to the command register. The address of the byte to be verified must be supplied because the device latches this address on the falling edge of the WE and the actual command on the rising edge. The register write with the erase verify command terminates the erase operation. The device applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all the bits of the byte are erased. If the location is erased the erase verify operation is repeated for the next location. The command must be written before each byte verification to latch the byte address.This process continues for each byte of the array until a byte does not return FFH or the last address is accessed.

In the case where the data returned is not FFH , another setup Erase/Erase operation is performed. The verification starts then from the address of the last verified byte. Once the last address is accessed, erasure is complete and the erase verify is terminated by writing a valid command to the command register. See Fig.6, 6bis for Erase algorithm, Fig.5 for waveforms and Table 10 for erase timings.

SET UP PROGRAM/PROGRAM

Writing 40H to the command register performs the setup operation. The next WE pulse operation causes a transition to an active programming operation. The device latches address and data on the falling and rising edge of WE pulse respectively. The rising edge of this second WE pulse also begins programming operation. The programming operation is stopped on the next rising edge of WE used to write the program verify command into the command register. See A.C programming characteristics and waveforms for programming timings (Fig 4 ,Table 10).

PROGRAM VERIFY MODE

Flash memory device programs on a byte by byte basis. After each programming operation, the byte just programmed must be verified. The program verify command (C0H) stops programming and sets up verification. The device executes the command on the rising edge of WE. The program verify command prepares the device for verification of the byte last programmed. No new address information is latched. The device applies an internally generated margin voltage to the byte. After a 6µs delay the data is read at the address programmed and compared to the programmed data. Reading valid data indicates that the byte programmed successfully. See Fig.4 for programming algorithm, Fig.3 for waveforms and Table 10 for programming timings.

COMMAND REGISTER RESET

This command is used to safely abort erase- and program-command sequences. The reset operation is performed by writing twice the code FFH to the command register. The memory content is not altered. A valid command must be written to place the device in the desired state.

STANDBY MODE

If during Erasure, Programming, or Program/Erase verification, the device is deselected, it draws active current until operation is terminated.

PRESTO F PROGRAMMING ALGORITHM

Programming with PRESTO F consists in applying a sequence of 100 µs program pulses to each byte until a correct verify occurs. 25 programming operations are allowed for each byte. Each programming operation consists in a set-up program command through the command register (code 40H) ; the programming is then performed. Then a program verify command is written into the command register (code C0H) and read is performed which compares data output with data expected. During Programming and Verify operation a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. Figure 4 illustrates the PRESTO F programming algorithm.

PRESTO F ERASE ALGORITHM

Erasing with PRESTO F erase algorithm allows to erase electrically the entire memory in a reliable way. The algorithm starts by first programming all the bytes to 00H in order to perform an uniform erasure. This step is accomplished by using the PRESTO F Programming algorithm. All bytes being in the same state (00H), a set-up erase command is written into the command register (code 20H) followed by the erase command (code 20H). Erase is then performed. Erase verify command is written to the command register (code A0H), and data of the address to be verified is compared to FFH. The erase verify begins at address 0000H and continues until the last address is accessed or until the comparison of data to FFH fails. The address of the last byte verified can be stored and a new erase operation is performed. The erase verify then starts from the stored address location or from address 0000H. Figure 6 illustrates the PRESTO F erase algorithm.

Table 6 : OPERATING CONDITIONS

Symbol	Parameters	Ranges	Units
TA	Operating Temperature READ only operations ERASE/WRITE operations	 0 to 70 0 to 70	 °C °C
V_{CC}	Supply Voltage	4.5 to 5.5	V

Table 7 : DC CHARACTERISTICS

Symbol	Parameters	Limits		Units	Test Condition
		min	max		
I_{LI}	Input Leakage current		±1	µA	$V_{CC} = V_{CC}$max Vin = 0 to V_{CC}
I_{LO}	Output Leakage current		±10	µA	$V_{CC} = V_{CC}$max Vout = 0 to V_{CC}
I_{CCS1}	V_{CC} standby current TTL		1	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IH}$
I_{CCS2}	V_{CC} standby current CMOS		100	µA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{CC}$ ±0.2V
I_{PPS}	V_{PP} Leakage current		±10	µA	$V_{PP} = V_{PPL}$
I_{CC1}	V_{CC} active read current		30	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IL}$ f = 5 MHz Iout = 0mA
I_{CC1}	V_{CC} active read current		50	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IL}$ f = 10 MHz Iout = 0mA
I_{CC2}	V_{CC} programming current		30	mA	Programming in progress
I_{CC3}	V_{CC} erase current		30	mA	Erasure in progress
I_{PP2}	V_{PP} programming current		30	mA	$V_{PP} = V_{PPH}$ programming in progress
I_{PP3}	V_{PP} erase current		30	mA	$V_{PP} = V_{PPH}$ erasure in progress
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage TTL	2	V_{CC}+0.5	V	
	Input high voltage CMOS	0.7V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output low voltage		0.45	V	$V_{CC} = V_{CC}$min I_{OH} = 2.1 mA
V_{OH}	Output high voltage CMOS	4.1		V	$V_{CC} = V_{CC}$min I_{OH} = -100 µA
	Output high voltage TTL	V_{CC} -0.8		V	$V_{CC} = V_{CC}$min I_O = -2,5 mA
V_{PPH}	V_{PP} during Write/Read operations	11.4 12.5	12.6 13	V	Code A1H V_{PP} > +12V device Code A8H V_{PP} =12.75V Device
V_{PPL}	V_{PP} during read only operations	0	8	V	
V_{PPDV}	V_{PPH} difference between Erase/Program and Verify		0.2	V	V_{PP} = 12V Device
V_{SI}	A9 electronic signature voltage	11.5	13	V	A9 = V_{SI}

Note : Operating temperature is for Commercial Range.

DESIGN CONSIDERATIONS

TWO LINE OUTPUT CONTROL

Because Flash memories are usually used in large memory arrays, the M28F256 features a 2 line control function which accommodates the use of multiple memory connections. The two line control function allows :

a)the lowest possible memory power dissipation,
b)complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, CE should be decoded and used as the primary device selecting function, while OE should be made a common connection to all devices in the array and connected to the read line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode .

POWER SUPPLY DECOUPLING

The power switching characteristics of the M28F256 require careful decoupling of the devices. Supply current I_{CC} has three segments that are of interest to the system designer : the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of CE. The magnitude of this transient current peak is dependent on capacitive and inductive loading of the device, at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and GND, and V_{PP} and GND. This should be a High frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be placed near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effect of the printed-circuit-board traces.

POWER UP/DOWN SEQUENCING

The M28F256 is designed to offer protection against accidental erasure and programming caused by spurious system level signals that may exist during power transitions. The M28F256 powers up in its read only mode. With its command register two step command sequences are necessary to alter memory contents. While these precautions are sufficient in most applications, it is recommended that V_{CC} reachs its steady-state value before raising V_{PP} above V_{CC}+2V. In addition upon power down V_{PP} should be below V_{CC} + 2 V, before lowering V_{CC}.

In addition, upon powering-down, V_{PP} should be below V_{CC}+2V before lowering V_{CC}.

Table 8 : CAPACITANCE TA = 25°C, f = 1 MHz

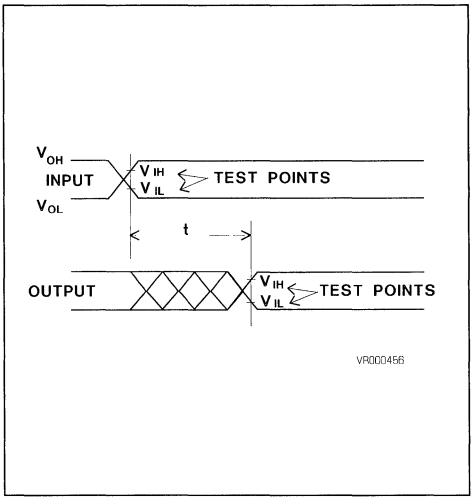
Symbol	Parameter	Test condition	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	12	pF

Note : (1) this parameter is only sampled and not 100% tested.

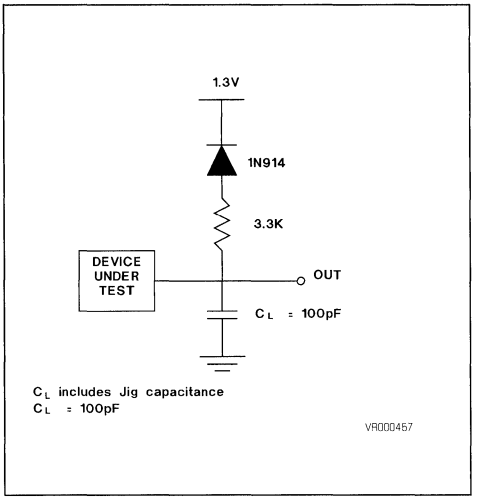
AC TEST CONDITIONS

Input Rise and Fall Times (10 % to 90 %)	10 ns
Input pulse Levels	V_{OH} and V_{OL}
Input timing reference Levels	V_{IL} and V_{IH}
Output timing Reference Levels	V_{IH} and V_{IL}

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. Testing : Inputs are driven at V_{OH} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

Table 9 : A.C CHARACTERISTICS Read Only Operations

Symbol	Characteristic	M28F256-100		M28F256-120		M28F256-150		M28F256-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{ACC}	Address to output delay		100		120		150		200	ns
T_{CE}	$\overline{CE}$ to output delay		100		120		150		200	ns
T_{OE}	$\overline{OE}$ to output delay		45		60		70		75	ns
T_{DF}	OE high to output float		30		30		35		45	ns
T_{OH}	Output hold from Address, $\overline{CE}$, or $\overline{OE}$ change (1)	0		0		0		0		ns
T_{WR}	Write recover time before read	6		6		6		6		µs
T_{CEL}	$\overline{CE}$ low to output in low Z	0		0		0		0		ns
T_{CDF}	$\overline{CE}$ high to output in high Z		40		40		55		60	ns
T_{OEL}	$\overline{OE}$ low to output in low Z	0		0		0		0		ns

(1) whichever occurs first.

Table 10 : A.C. CHARACTERISTICS Write/Erase/Program Operations (1)

Symbol	Characteristic	M28F256-100		M28F256-120		M28F256-150		M28F256-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{WC}	Write cycle time	100		120		150		200		ns
T_{AS}	Address setup time	0		0		0		0		ns
T_{AH}	Address hold time	40		50		60		75		ns
T_{DS}	Data setup time	50		50		50		50		ns
T_{DH}	Data hold time	10		10		10		10		ns
T_{WHGL}	Write recover time before read	6		6		6		6		µs
T_{GHWL}	Read recover time before write	0		0		0		0		µs
T_{CS}	$\overline{CE}$ setup time	20		20		20		20		ns
T_{CH}	$\overline{CE}$ hold time	0		0		0		0		ns
T_{WP}	Write pulse width	40		40		50		60		ns
T_{WPH}	Write pulse width high	40		40		50		60		ns
T_{WHWH1}	Duration of programming operation	95	150	95	150	95	150	95	150	µs
T_{WHWH2}	Duration of erase operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
T_{VPEL}	V_{PP} setup to $\overline{CE}$ low	100		100		100		100		ns
T_{ELEH}	Alternate write pulse width	40		40		50		60		ns

Notes : (1) Refer to read timing table for read timing characteristics during Write/Read operations.

Figure 3 : A.C. Waveforms for Programming Operations

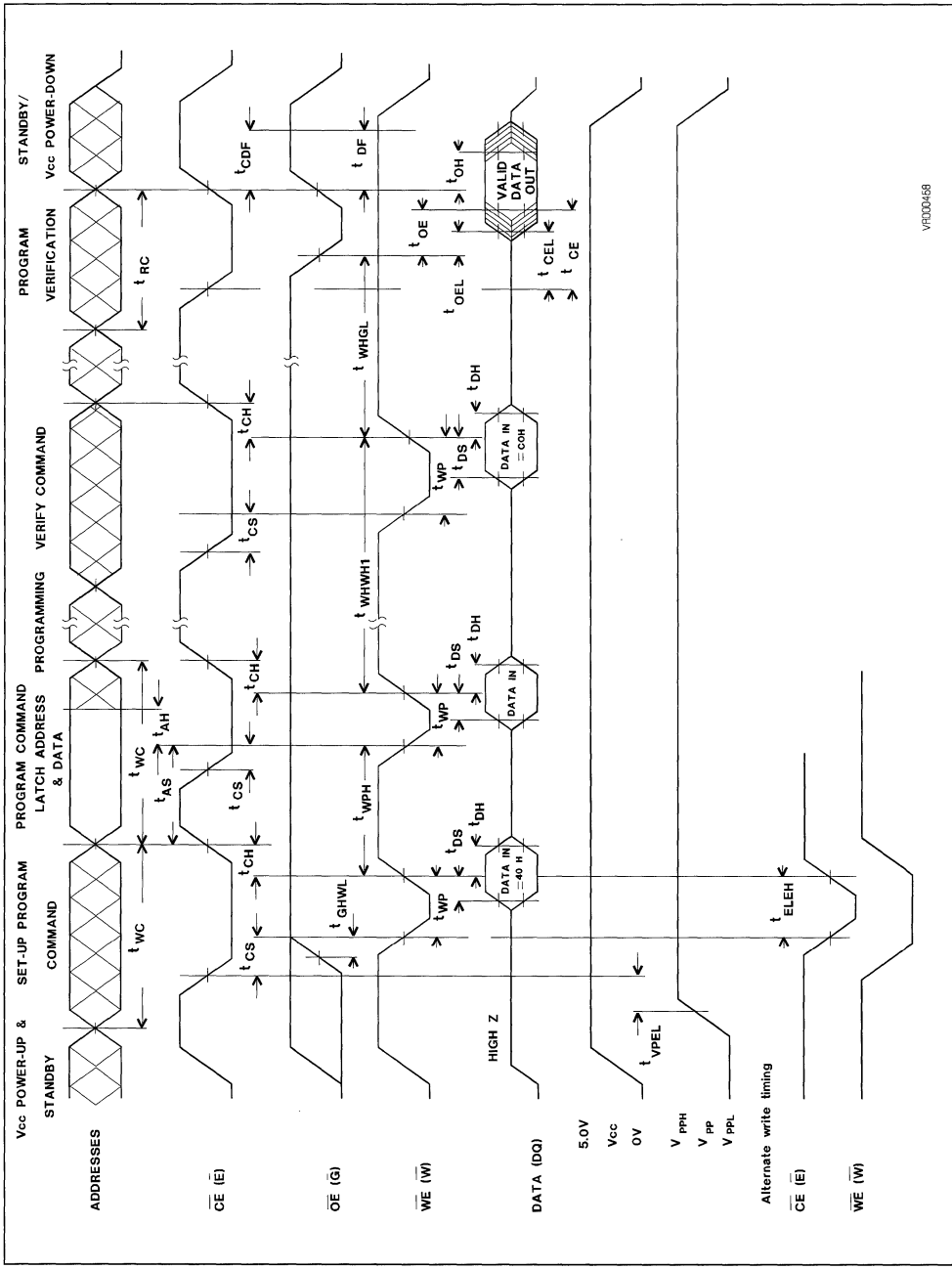
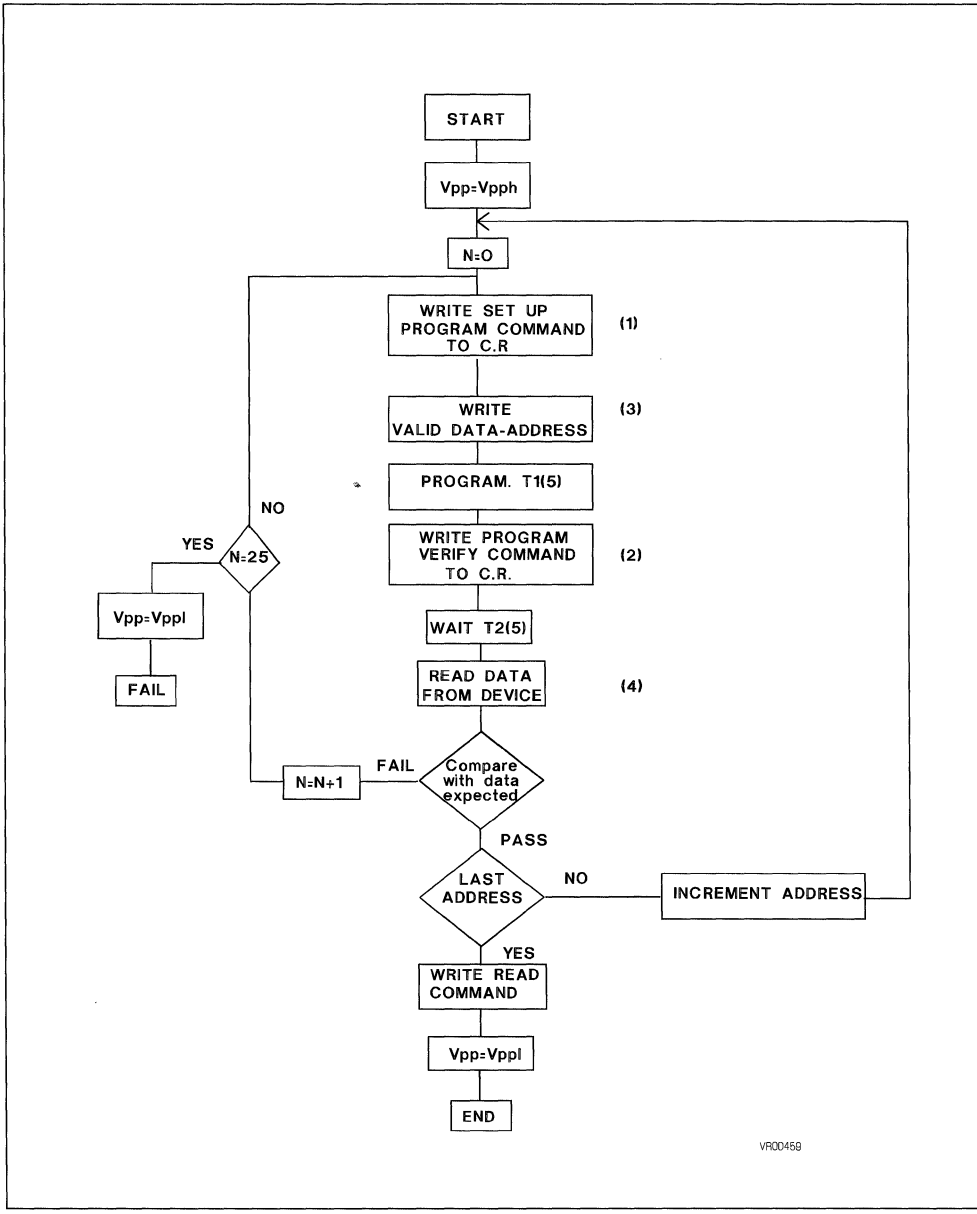


Figure 4 : Presto F Programming Algorithm



Notes : (1) C.R. = Command Register.
(2) STOPS program generation - program verify command is only performed after byte programming.
(3) Second bus cycle of the setup Program/Program command (See Table 5 and Fig 4) starts programming operation.
(4) Second bus cycle of the program verify command (See Table 5 and Fig 4).
(5) T1 = 100µs, T2 = 6µs

Figure 5 : A.C. Waveforms for Erase Operations

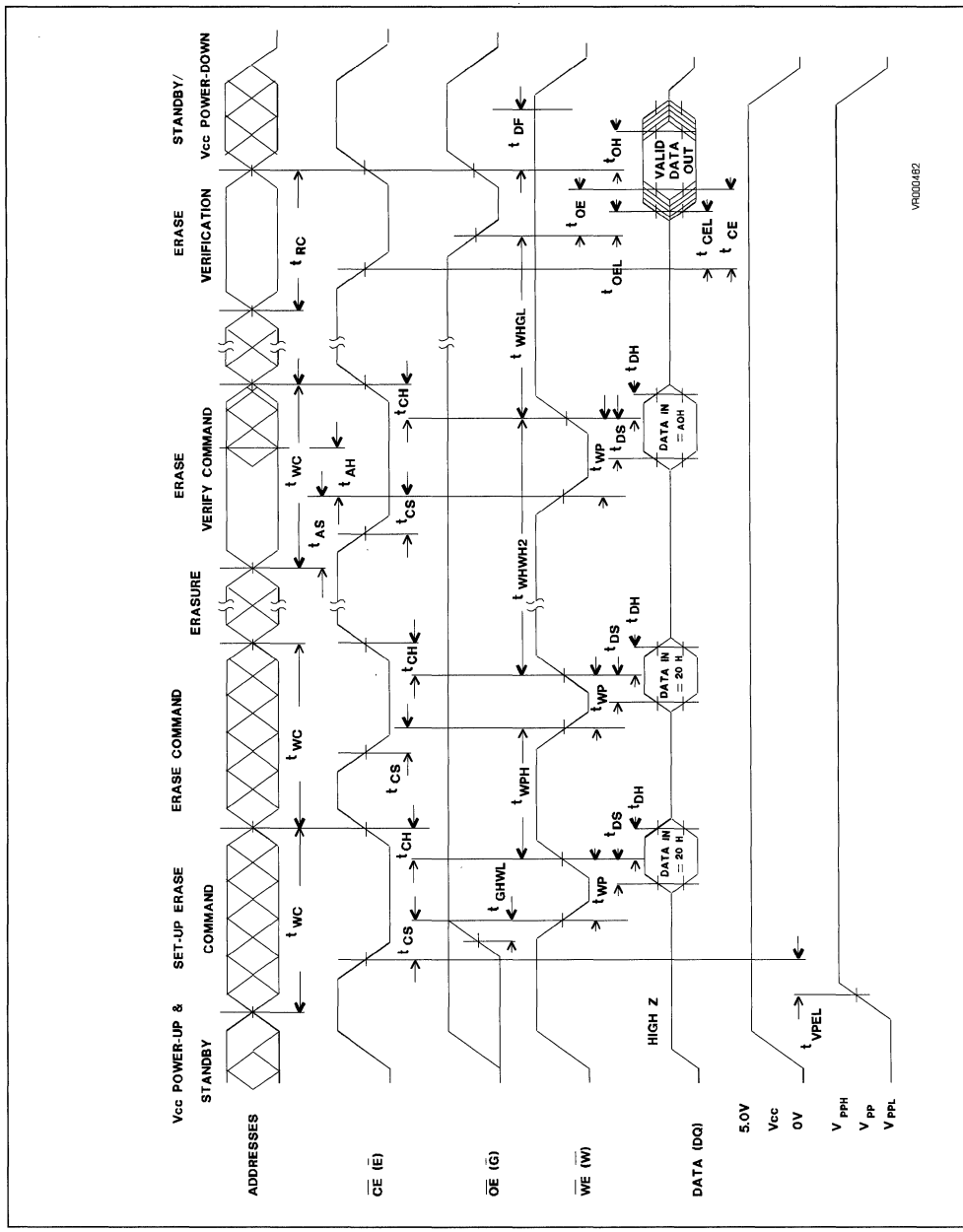
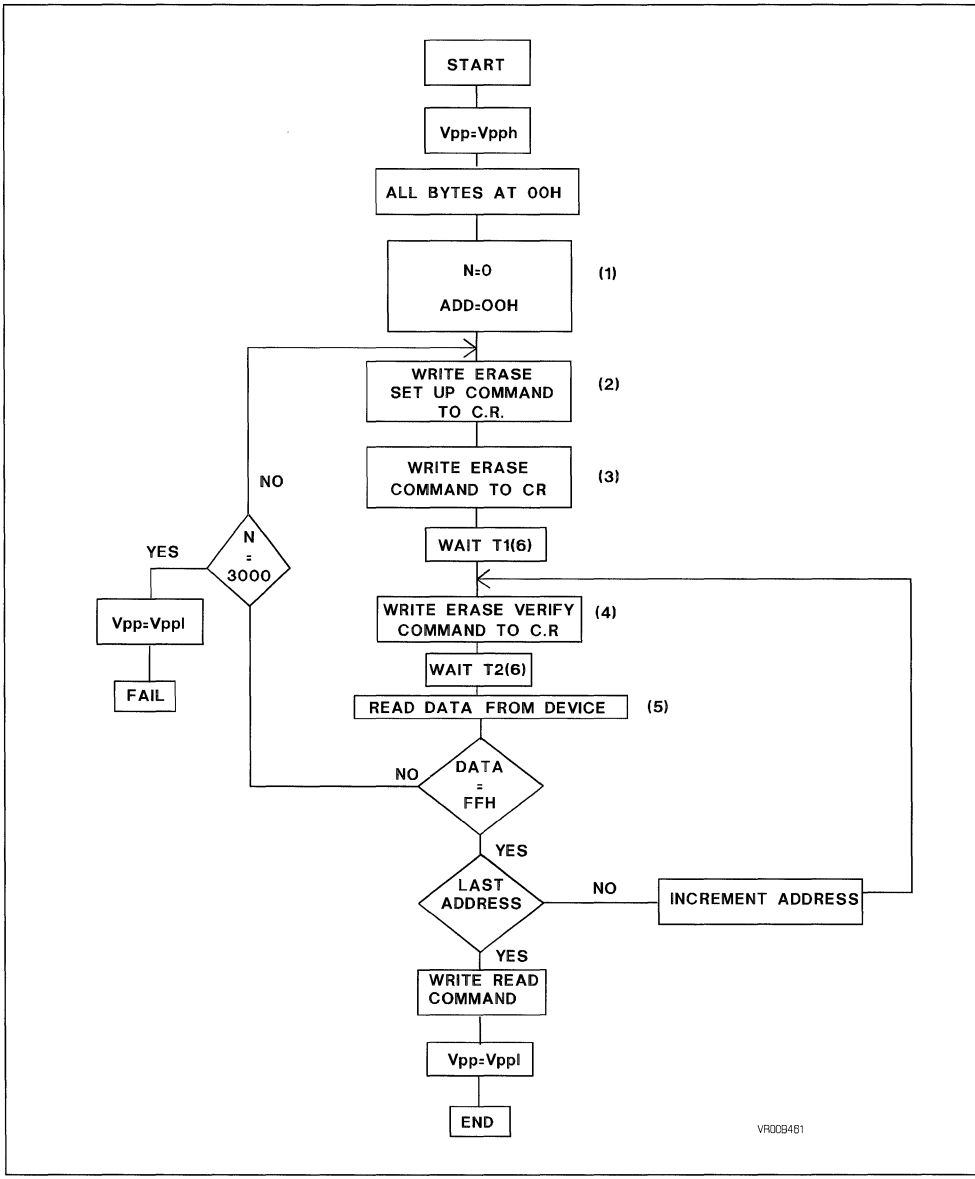
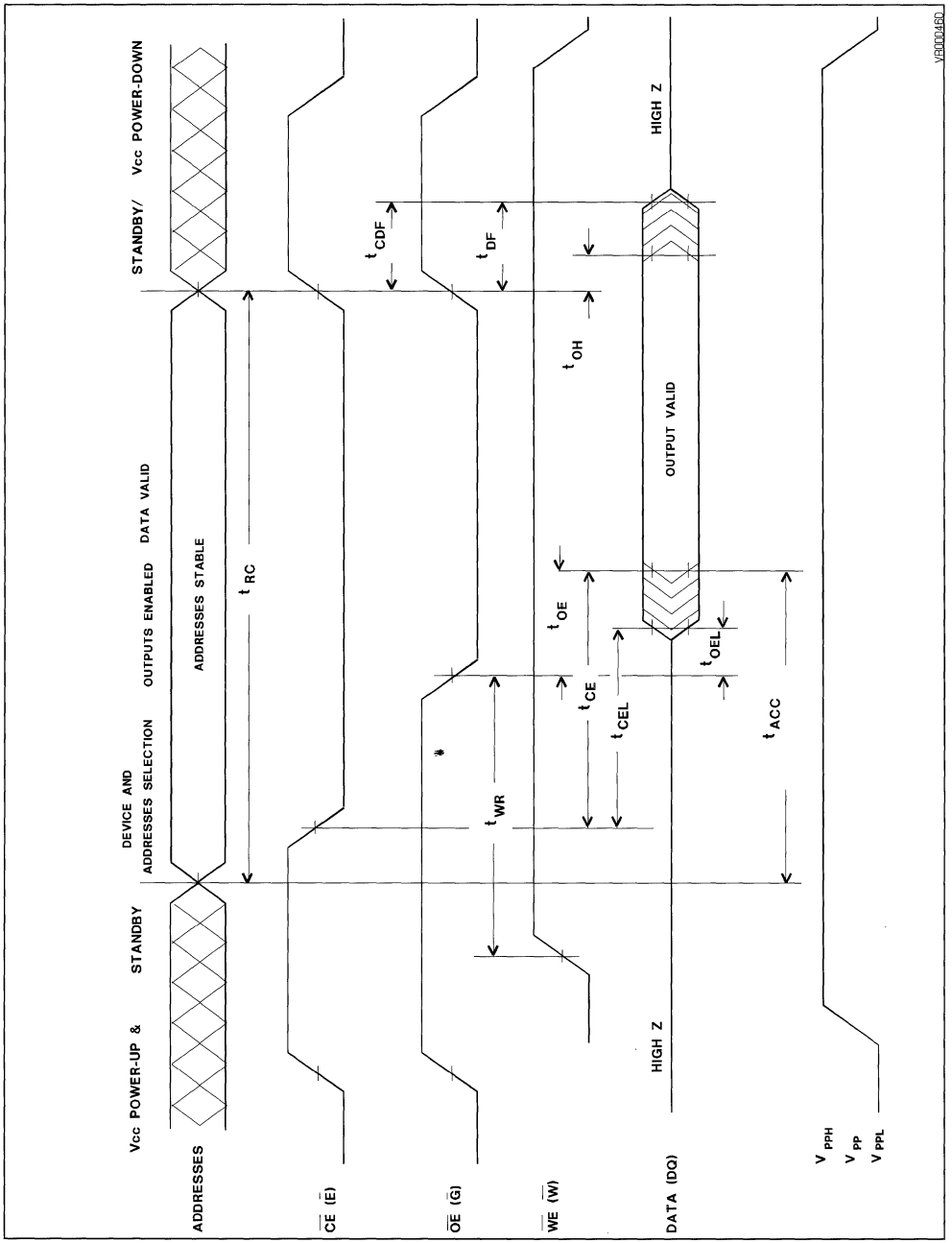


Figure 6 : Presto F Erase Algorithm



Notes : (1) N = Pulse Count.
(2) CR = Command Register.
(3) Second Bus Cycle of Setup Erase/Erase command (see Table 5 and Fig. 5).
(4) Address = byte to verify. Erase verify is only performed after chip Erasure.
(5) Second bus cycle of Erase verify command.
(6) T1 = 10ms, T2 = 6µs.

Figure 7 : A.C. Waveforms for Read Operations



PACKAGE MECHANICAL DATA

Figure 8 : 32 PIN CERAMIC DUAL IN LINE FREAT SEAL

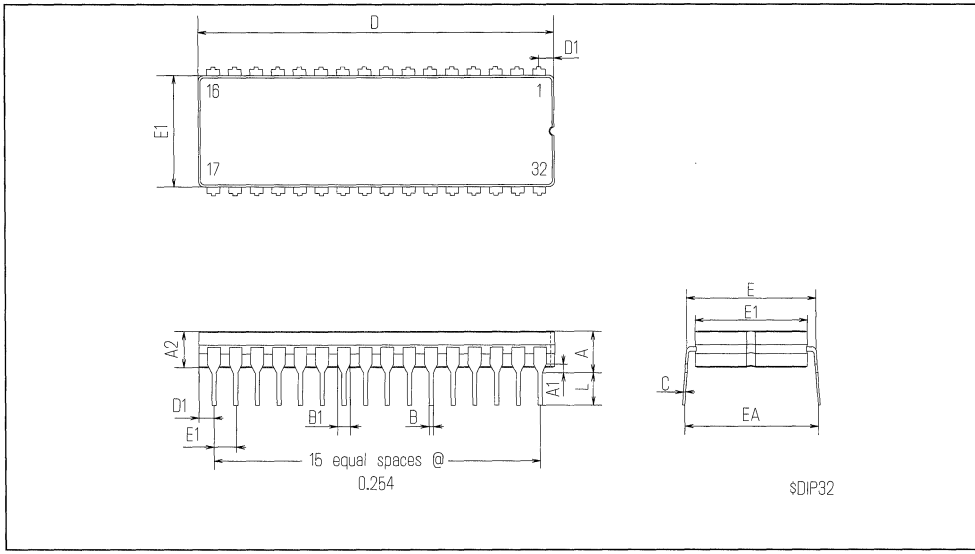
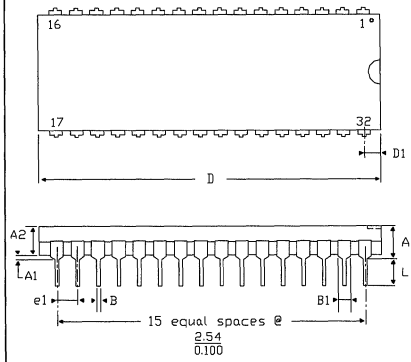
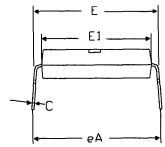


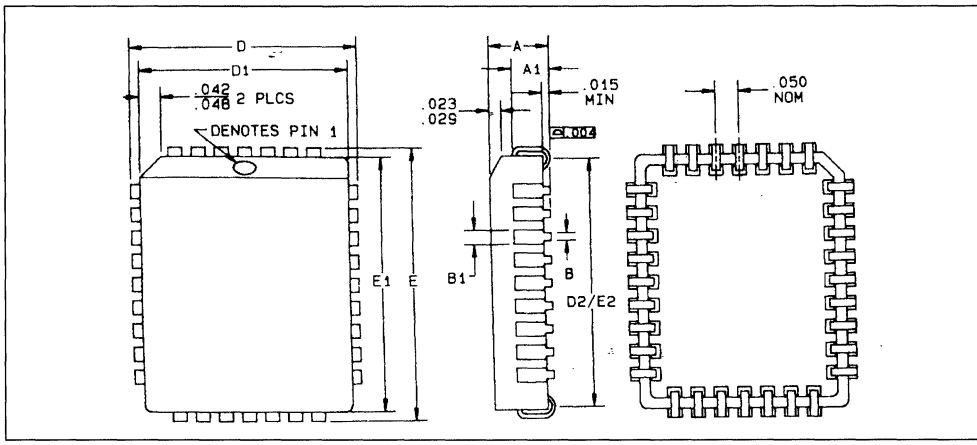
Figure 9 : 32 PIN PLASTIC DUAL IN LINE





Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.38					
a1	0.20			0.015		
B		0.46			0.018	
B1			0.30	0.008		0.012
B2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e3		35.60			1.400	
e4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L	3.18		3.43	0.125		0.135

Figure 10 : 32 PIN PLCC



ORDERING INFORMATION

M	2	8	F	2	5	6	-	1	2	X	C	1	1	2

REPROGRAM CYCLES 10^X
2 = 100 CYLES
3 = 1000 CYCLES
4 = 10000 CYCLES

SPEED/10

ERASE/PROGRAM VOLTAGE
1 = 12 ± 5% V

V_{CC} MARGIN
X= ± 5%
- = ± 10%

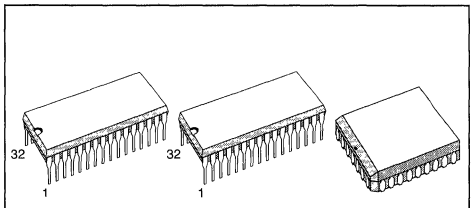
TEMPERATURE RANGE
1 = 0 TO 70°C
3 = -40 TO 125°C
6 = -40 TO 85°C
7 = -40 TO 105°C

PACKAGE
C = PLCC
B = PLASTIC DIL
F = CERAMIC FRIT SEAL

1024K (128 x 8) CMOS FLASH MEMORY

ADVANCE DATA

- FLASH ELECTRICAL CHIP ERASE IN 1 SECOND RANGE.
- PRESTO F PROGRAMMING TYPICAL BYTE PROGRAM TIME : 100 µs.
- 12 V VPP SUPPLY.
- 100 TO 10.000 ERASE/PROGRAM CYCLES.
- VERY FAST ACCESS TIME : 100 ns.
- LOW POWER CONSUMPTION : Maximum standby current : 100 µA.
- COMMAND REGISTER ARCHITECTURE FOR MICROPROCESSOR / MICROCONTROLLER COMPATIBLE WRITE INTERFACE.
- JEDEC STANDARD BYTE-WIDE EPROM PINOUTS.



FDIP 32 **PDIP32** **PLCC32**

(Ordering information at the end of the datasheet)

DESCRIPTION

SGS-THOMSON Microelectronics M28F1001 FLASH Memory is an Electrically Chip-erasable and Reprogrammable non-volatile memory. Higher functionality and flexibility than EPROM come from the ability to be Chip-erased and reprogrammed in a test socket, in a PROM programmer socket, on board, or In-system. The M28F1001 is suitable for applications where EEPROM functionality is not suitable or not cost effective, or for replacement of UV EPROM when UV erasure is impractical or time consuming. Pin assignment conforms to JEDEC standards for byte wide EPROMs. The High performance access time allows interface with most microcontrollers and microprocessors.

PIN NAMES

A0-A16	ADDRESS INPUT
O0-O7	DATA INPUT/OUTPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{PP}	ERASE/PROGRAM power supply
V_{CC}	5V ± 10 % POWER SUPPLY
GND	GROUND
NC (1)	NO INTERNAL CONNECTION

(1) Pin may be driven or left floating.

Figure 1: Pin Configuration

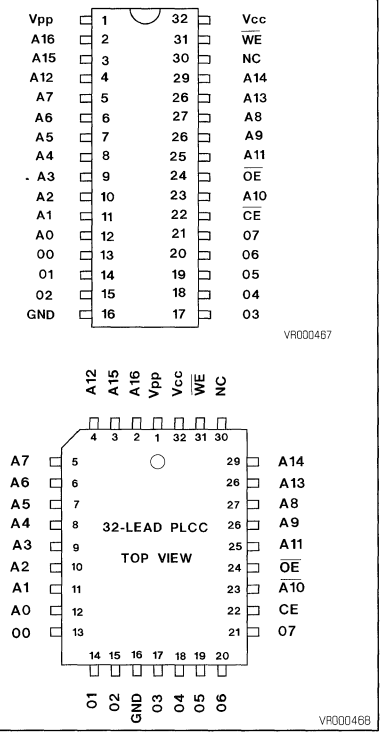


Figure 2 : M28F1001 Block Diagram

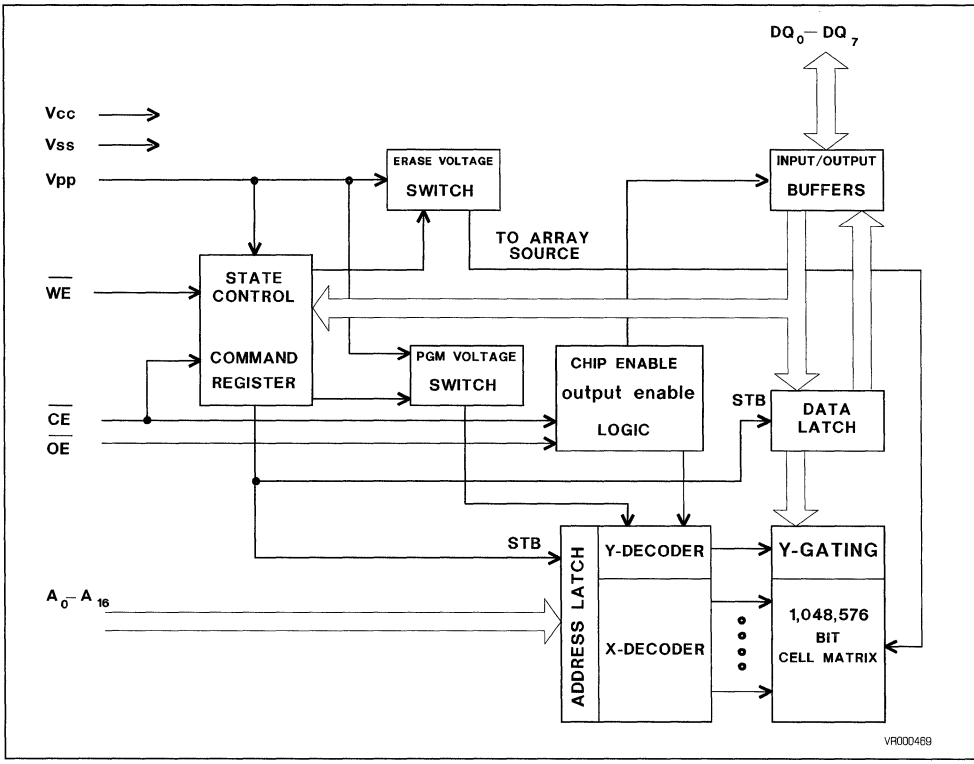


Table 3 : Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to 7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to 14	V
VA9	Voltage on A9 with respect to ground	-0.6 to 13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to 7.0	V
T_{bias}	Temperature Range under Bias	-10 to 80	°C
T_{stg}	Storage temperature range	-65 to 125	°C
TR_{op}	Operating Temperature during Read	0 to 70	°C
TEP_{op}	Operating Temperature during Erase / Program	0 to 70	°C

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4 : Bus Operation

PINS / OPERATIONS		V_{PP} (1)	A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	O0-O7
READ ONLY	READ	V_{PPL}	A0	A9	V_{IL}	V_{IL}	V_{IH}	DATA OUT
	OUTPUT DISABLE	V_{PPL}	X (7)	X	V_{IL}	V_{IH}	V_{IH}	TRI STATE
	STANDBY	V_{PPL}	X	X	V_{IH}	X	X	TRI STATE
	MANUFACTURER SIGNATURE (2)	V_{PPL}	VIL	V_{SI} (3)	V_{IL}	V_{IL}	V_{IH}	DATA = 20
	DEVICE SIGNATURE (2)	V_{PPL}	V_{IH}	V_{SI}	V_{IL}	V_{IL}	V_{IH}	DATA = 02
READ/ WRITE	READ	V_{PPH}	A0	A9	VIL	V_{IL}	V_{IH}	DATA OUT (4)
	OUTPUT DISABLE	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	TRI STATE
	STANDBY (5)	V_{PPH}	X	X	V_{IH}	X	X	TRI STATE
	WRITE	V_{PPH}	A0	A9	V_{IL}	V_{IH}	V_{IL}	DATA IN (6)

Notes : (1) V_{PP} Low may be ground, a no connect with a resistor tied to ground, or < 8 volts. V_{PP} High is the programming voltage specified for the device. When $V_{PP} = V_{PPL}$ memory content can be read but not written or erased.
(2) Manufacturer and Device electronic Signature can be accessed also through Command Register (see table 5)
(3) 11.5V < V_{SI} < 13V.
(4) When $V_{PP} = V_{PPH}$ read operation can be array data or Electronic Signature.
(5) When $V_{PP} = V_{PPH}$ Standby current is $I_{CC} + I_{PP}$ (Standby).
(6) Refer to table 5 for Data In during write.
(7) X can be V_{IL} or V_{IH}.

DEVICE OPERATION

PRINCIPE

The added functionality of FLASH as compared to EPROM, is Electrical Erasure and Reprogramming. In order to manage this new functionality a command register is introduced. Some device functions are addressed via the command register, some not, depending on the V_{PP} pin voltage. When V_{PP} pin is at low voltage (< 8V), the M28F1001 is a READ only memory. The command register is disabled. Manipulations of the external memory control pins yield the standard EPROM read, output disable, electronic signature and standby operations. Raising V_{PP} pin to High voltage, enables the command register for READ/WRITE operations. In addition, read, output disable, standby, electronic signature, ERASE and WRITE operations are allowed. At $V_{PP} = V_{PPH}$ the operating modes are addressed through the use of the command register.

Table 4 summarizes the Bus operations : at $V_{PP}=V_{PPL}$ only Read operations are allowed, at $V_{PP}=V_{PPH}$ Read operations and Erase/Write operations are allowed.

OPERATION MODES DESCRIPTION

A- OPERATION MODES WITH V_{PP} AT LOW VOLTAGE (< 8V)

READ MODE

The M28F1001 has two control pins, both of which must be logically active in order to obtain data at the outputs.

Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Fig 7 illustrates read timing waveforms.

STANDBY MODE

The M28F1001 has a standby mode which reduces the maximum active current from 30mA to 0.1mA. The device is placed in Standby mode by applying a high signal to the $\overline{CE}$ input. When in Standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input .

OUTPUT DISABLE

With $\overline{OE}$ at High level V_{IH}, output pins are placed in a high impedance state.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for use by programming equipment

to automatically match the device to be programmed or erased with its corresponding programming or erasing algorithm. This mode is activated by applying high voltage on address line A9 (11.5V - 13V) and by applying V_{IL} to $\overline{CE}$ and $\overline{OE}$. Two identifier bytes may then be sequenced from the outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) represents the device identifier code. For the SGS-THOMSON Microelectronics M28F1001, these two identifiers are given here below and can be read on outputs O0 to O7.

WRITE MODE

When V_{PP} is at low voltage, memory contents can not be written or erased. Write/Erased operations can only be accomplished via the command register when V_{PPH} is applied on V_{PP} pin.

ELECTRONIC SIGNATURE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE IDENTIFIER	V_{IH}	0	0	0	0	0	0	1	0	02

Notes : (1) A9 = 12.0V ± 0.5V ; $\overline{CE}$ = $\overline{OE}$ = V_{IL} ; V_{PP} = V_{PPL} ; A1 to A8= V_{IL} ; A10 to A16 = V_{IL}.

Table 5 : COMMAND DEFINITIONS

COMMAND	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Operation (1)	Address (2)	Data (3)	Operation (1)	Address (2)	Data (3)
Read Memory	1	Write	X	00H			
Read Electronic Signature (4)	1	Write	X	90H	Read	IA	ID
Setup Erase/Erase (5)	2	Write	X	20H	Write	X	20H
Erase Verify (5)	2	Write	EA	A0H	Read	X	EVD
Setup program/Program (6)	2	Write	X	40H	Write	PA	PD
Program verify (6)	2	Write	X	C0H	Read	X	PVD
Reset (7)	2	Write	X	FFH	Write	X	FFH

Notes:
(1) Bus operations are defined in table 4.
(2) IA = identifier address ; 00000H for manufacturer code and 00001H for device.
(3) EA = address of memory location to be read during erase verify.
PA = address of memory location to be programmed.
(4) ID = data read from location IA during electronic signature ; 20H = manuf ; 02H = device.
PD = data to be programmed at location PA. EVD = data read during from location EA during erase verify.
PVD Data read from location PA during program verify.
(5) See fig. 6 for erase algorithm.
(6) See fig. 4 for programming algorithm.
(7) The second bus cycle must be followed by the desired command register write.

B - OPERATION MODES WITH V_{PP} AT V_{PPH} - COMMAND REGISTER

At V_{PP} = V_{PPH}, Read/Write operations are enabled. Device operations are selected by writing specific data patterns into the command register using standard microprocessor write timings. The register contents are inputs for an internal state machine which controls erase and programming circuitry. Some commands require one write cycle, while others require two. The register is a latch used to store these commands and the data and address needed to execute the command.

(Note that the command register does not occupy an addressable memory location).

With this architecture, the device expects the first write cycle to be a command and does not corrupt data at specified address. The command register is written by bringing WE to V_{IL}, while CE is low. Addresses are latched on the falling edge of WE, while data are latched on the rising edge of WE pulse. Table 5 contains the list of register commands. The three high order register bits R7, R6 and R5 encode the control function. All other register bits R4-R0 must be at zero. Only exception is the reset command, when FFH is written into the command register. Register bits R7-R0 correspond to data inputs D7-D0. Note that when V_{PP} is at low voltage, the contents of the command register default to 00H enabling Read-Only operations. The command register is only alterable when V_{PP} is at high voltage. The system designer may choose to make the V_{PP} switchable or to make the V_{PP} constantly available. In the case of switchable V_{PP}, when V_{PP} is removed, the device defaults to Read Only memory. In the case of constantly available V_{PP}, all memory functions are performed via the command register.

READ MODE WITH V_{PP} = V_{PPH}

At V_{PP} = V_{PPH}, memory contents can be addressed via the read command 00H. Read mode is initiated by writing 00H into the command register. The microprocessor read cycles retrieve the array data. The device remains enabled for read operations until the command register contents are altered. The default contents of the command register upon power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. When V_{PP} is "Hardwired", the device powers-up and remains enabled for read operations until the command register contents are changed.

Refer to AC Read characteristics and waveforms for timing parameters (Fig 7,Table 9).

ELECTRONIC SIGNATURE WITH V_{PP} = V_{PPH}

In order for the M28F1001 to be erased and programmed by the local CPU and thus to supplement the traditional PROM programming methodology, the manufacturer and device signature codes can be read via the command register. The operation is initiated by writing 90H to the register. Following the command write, a read cycle from address 00000H returns the manufacturer code of 20H. A read cycle from address 00001H returns the device code of 02H. To terminate the operation, it is necessary to write another valid command into the register.

SET UP ERASE/ERASE MODE

Before erasure it is necessary to program all bytes to the same level (data 00H). Setup erase is a command-only operation that prepares the device for electrical erasure of all bytes in the array. The setup erase is performed by writing 20H to the command register. To begin chip erasure, the erase command (20H) must again be written to the register. The erase operation begins on the second command's rising edge of the WE pulse and terminates with the rising edge of the next WE pulse (i.e Erase Verify command). This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased. Refer to A.C Erase characteristics and waveforms for timing parameters (Fig 6, Fig 5, Table 10).

ERASE VERIFY MODE

The erase command erases all the bytes of the array in parallel. After each erase operation, all bytes must be verified to see if they are erased. The erase verify operation is initiated by writing A0H to the command register. The address of the byte to be verified must be supplied because the device latches this address on the falling edge of the WE and the actual command on the rising edge. The register write with the erase verify command terminates the erase operation. The device applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all the bits of the byte are erased. If the location is erased the erase verify operation is repeated for the next location. The command must be written before each byte verification to latch the byte address.This process continues for each byte of the array until a byte does not return FFH or the last address is accessed.

In the case where the data returned is not FFH , another setup Erase/Erase operation is performed. The verification starts then from the address of the last verified byte. Once the last address is accessed, erasure is complete and the erase verify is terminated by writing a valid command to the command register. See Fig.6, 6bis for Erase algorithm, Fig.5 for waveforms and Table 10 for erase timings.

SET UP PROGRAM/PROGRAM

Writing 40H to the command register performs the setup operation. The next WE pulse operation causes a transition to an active programming operation. The device latches address and data on the falling and rising edge of WE pulse respectively. The rising edge of this second WE pulse also begins programming operation. The programming operation is stopped on the next rising edge of WE used to write the program verify command into the command register. See A.C programming characteristics and waveforms for programming timings (Fig 4 ,Table 10).

PROGRAM VERIFY MODE

Flash memory device programs on a byte by byte basis. After each programming operation, the byte just programmed must be verified. The program verify command (C0H) stops programming and sets up verification. The device executes the command on the rising edge of WE. The program verify command prepares the device for verification of the byte last programmed. No new address information is latched. The device applies an internally generated margin voltage to the byte. After a 6µs delay the data is read at the address programmed and compared to the programmed data. Reading valid data indicates that the byte programmed successfully. See Fig.4 for programming algorithm, Fig.3 for waveforms and Table 10 for programming timings.

COMMAND REGISTER RESET

This command is used to safely abort erase- and program-command sequences. The reset operation is performed by writing twice the code FFH to the command register. The memory content is not altered. A valid command must be written to place the device in the desired state.

STANDBY MODE

If during Erasure, Programming, or Program/Erase verification, the device is deselected, it draws active current until operation is terminated.

PRESTO F PROGRAMMING ALGORITHM

Programming with PRESTO F consists in applying a sequence of 100 µs program pulses to each byte until a correct verify occurs. 25 programming operations are allowed for each byte. Each programming operation consists in a set-up program command through the command register (code 40H) ; the programming is then performed. Then a program verify command is written into the command register (code C0H) and read is performed which compares data output with data expected. During Programming and Verify operation a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. Figure 4 illustrates the PRESTO F programming algorithm.

PRESTO F ERASE ALGORITHM

Erasing with PRESTO F erase algorithm allows to erase electrically the entire memory in a reliable way. The algorithm starts by first programming all the bytes to 00H in order to perform an uniform erasure. This step is accomplished by using the PRESTO F Programming algorithm. All bytes being in the same state (00H), a set-up erase command is written into the command register (code 20H) followed by the erase command (code 20H). Erase is then performed. Erase verify command is written to the command register (code A0H), and data of the address to be verified is compared to FFH. The erase verify begins at address 00000H and continues until the last address is accessed or until the comparison of data to FFH fails. The address of the last byte verified can be stored and a new erase operation is performed. The erase verify then starts from the stored address location or from address 00000H. Figure 6 illustrates the PRESTO F erase algorithm.

Table 6 : OPERATING CONDITIONS

Symbol	Parameters	Ranges	Units
TA	Operating Temperature READ only operations ERASE/WRITE operations	 0 to 70 0 to 70	 °C °C
V_{CC}	Supply Voltage	4.5 to 5.5	V

Table 7 : DC CHARACTERISTICS

Symbol	Parameters	Limits		Units	Test Condition
		min	max		
I_{LI}	Input Leakage current		±1	µA	$V_{CC} = V_{CC}$max Vin = 0 to V_{CC}
I_{LO}	Output Leakage current		±10	µA	$V_{CC} = V_{CC}$max Vout = 0 to V_{CC}
I_{CCS1}	V_{CC} standby current TTL		1	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IH}$
I_{CCS2}	V_{CC} standby current CMOS		100	µA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{CC}$ ±0.2V
I_{PPS}	V_{PP} Leakage current		±10	µA	$V_{PP} = V_{PPL}$
I_{CC1}	V_{CC} active read current		30	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IL}$ f = 5 MHz Iout = 0mA
I_{CC1}	V_{CC} active read current		50	mA	$V_{CC} = V_{CC}$max $\overline{CE} = V_{IL}$ f = 10 MHz Iout = 0mA
I_{CC2}	V_{CC} programming current		30	mA	Programming in progress
I_{CC3}	V_{CC} erase current		30	mA	Erasure in progress
I_{PP2}	V_{PP} programming current		30	mA	$V_{PP} = V_{PPH}$ programming in progress
I_{PP3}	V_{PP} erase current		30	mA	$V_{PP} = V_{PPH}$ erasure in progress
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage TTL	2	V_{CC}+0.5	V	
	Input high voltage CMOS	0.7V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output low voltage		0.45	V	$V_{CC} = V_{CC}$min I_{OH} = 2.1 mA
V_{OH}	Output high voltage CMOS	4.1		V	$V_{CC} = V_{CC}$min I_{OH} = -100 µA
	Output high voltage TTL	V_{CC} -0.8		V	$V_{CC} = V_{CC}$min I_0 = -2,5 mA
V_{PPH}	V_{PP} during Write/Read operations	11.4	12.6	V	
V_{PPL}	V_{PP} during read only operations	0	8	V	
V_{PPDV}	V_{PPH} difference between Erase/Program and Verify		0.2	V	V_{PP} = 12V Device
V_{SI}	A9 electronic signature voltage	11.5	13	V	A9 = V_{SI}

Note : Operating temperature is for Commercial Range.

DESIGN CONSIDERATIONS

TWO LINE OUTPUT CONTROL

Because Flash memories are usually used in large memory arrays, the M28F1001 features a 2 line control function which accommodates the use of multiple memory connections. The two line control function allows :

a)the lowest possible memory power dissipation,
b)complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, CE should be decoded and used as the primary device selecting function, while OE should be made a common connection to all devices in the array and connected to the read line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode .

POWER SUPPLY DECOUPLING

The power switching characteristics of the M28F1001 require careful decoupling of the devices. Supply current I_{CC} has three segments that are of interest to the system designer : the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of CE. The magnitude of this transient current peak is dependent on capacitive and inductive loading of the device, at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and GND, and V_{PP} and GND. This should be a High frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be placed near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effect of the printed-circuit-board traces.

POWER UP/DOWN SEQUENCING

The M28F1001 is designed to offer protection against accidental erasure and programming caused by spurious system level signals that may exist during power transitions. The M28F1001 powers up in its read only mode. With its command register two step command sequences are necessary to alter memory contents. While these precautions are sufficient in most applications, it is recommended that V_{CC} reachs its steady-state value before raising V_{PP} above V_{CC}+2V. In addition upon power down V_{PP} should be below V_{CC} + 2 V, before lowering V_{CC}.

In addition, upon powering-down, V_{PP} should be below V_{CC}+2V before lowering V_{CC}.

Table 8 : CAPACITANCE TA = 25°C, f = 1 MHz

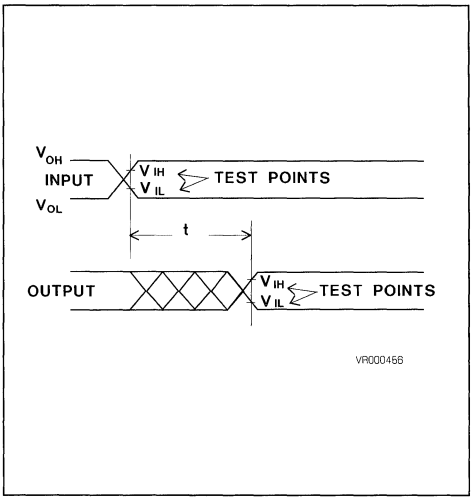
Symbol	Parameter	Test condition	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	12	pF

Note : (1) this parameter is only sampled and not 100% tested.

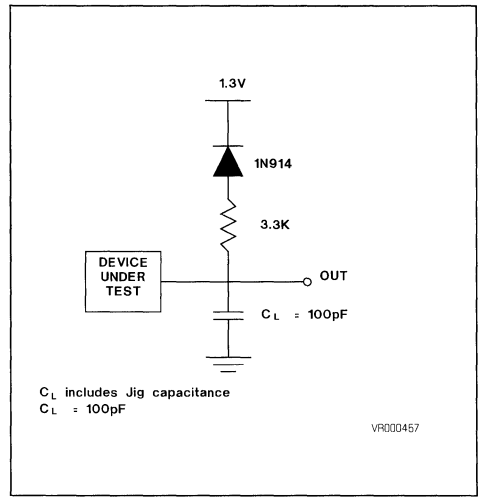
AC TEST CONDITIONS

Input Rise and Fall Times (10 % to 90 %)	10 ns
Input pulse Levels	V_{OH}(CMOS) and V_{OL}
Input timing reference Levels	V_{IL} and V_{IH}
Output timing Reference Levels	V_{IH} and V_{IL}

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. Testing : Inputs are driven at V_{OH} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

Table 9 : A.C CHARACTERISTICS Read Only Operations

Symbol	Characteristic	M281001-100		M28F1001-120		M28F1001-150		M28F1001-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{ACC}	Address to output delay		100		120		150		200	ns
T_{CE}	$\overline{CE}$ to output delay		100		120		150		200	ns
T_{OE}	$\overline{OE}$ to output delay		45		60		70		75	ns
T_{DF}	OE high to output float		30		30		35		45	ns
T_{OH}	Output hold from Address, $\overline{CE}$, or $\overline{OE}$ change (1)	0		0		0		0		ns
T_{WR}	Write recover time before read	6		6		6		6		µs
T_{CEL}	$\overline{CE}$ low to output in low Z	0		0		0		0		ns
T_{CDF}	$\overline{CE}$ high to output in high Z		40		40		55		60	ns
T_{OEL}	$\overline{OE}$ low to output in low Z	0		0		0		0		ns

(1) whichever occurs first.

Table 10 : A.C. CHARACTERISTICS Write/Erase/Program Operations (1)

Symbol	Characteristic	M28F1001-100		M28F21001-120		M28F1001-150		M28F1001-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{WC}	Write cycle time	100		120		150		200		ns
T_{AS}	Address setup time	0		0		0		0		ns
T_{AH}	Address hold time	40		50		60		75		ns
T_{DS}	Data setup time	50		50		50		50		ns
T_{DH}	Data hold time	10		10		10		10		ns
T_{WHGL}	Write recover time before read	6		6		6		6		µs
T_{GHWL}	Read recover time before write	0		0		0		0		µs
T_{CS}	$\overline{CE}$ setup time	20		20		20		20		ns
T_{CH}	$\overline{CE}$ hold time	0		0		0		0		ns
T_{WP}	Write pulse width	40		40		50		60		ns
T_{WPH}	Write pulse width high	40		40		50		60		ns
T_{WHWH1}	Duration of programming operation	95	150	95	150	95	150	95	150	µs
T_{WHWH2}	Duration of erase operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
T_{VPEL}	V_{PP} setup to $\overline{CE}$ low	100		100		100		100		ns
T_{ELEH}	Alternate write pulse width	40		40		50		60		ns

Notes : (1) Refer to read timing table for read timing characteristics during Write/Read operations.

Figure 3 : A.C. Waveforms for Programming Operations

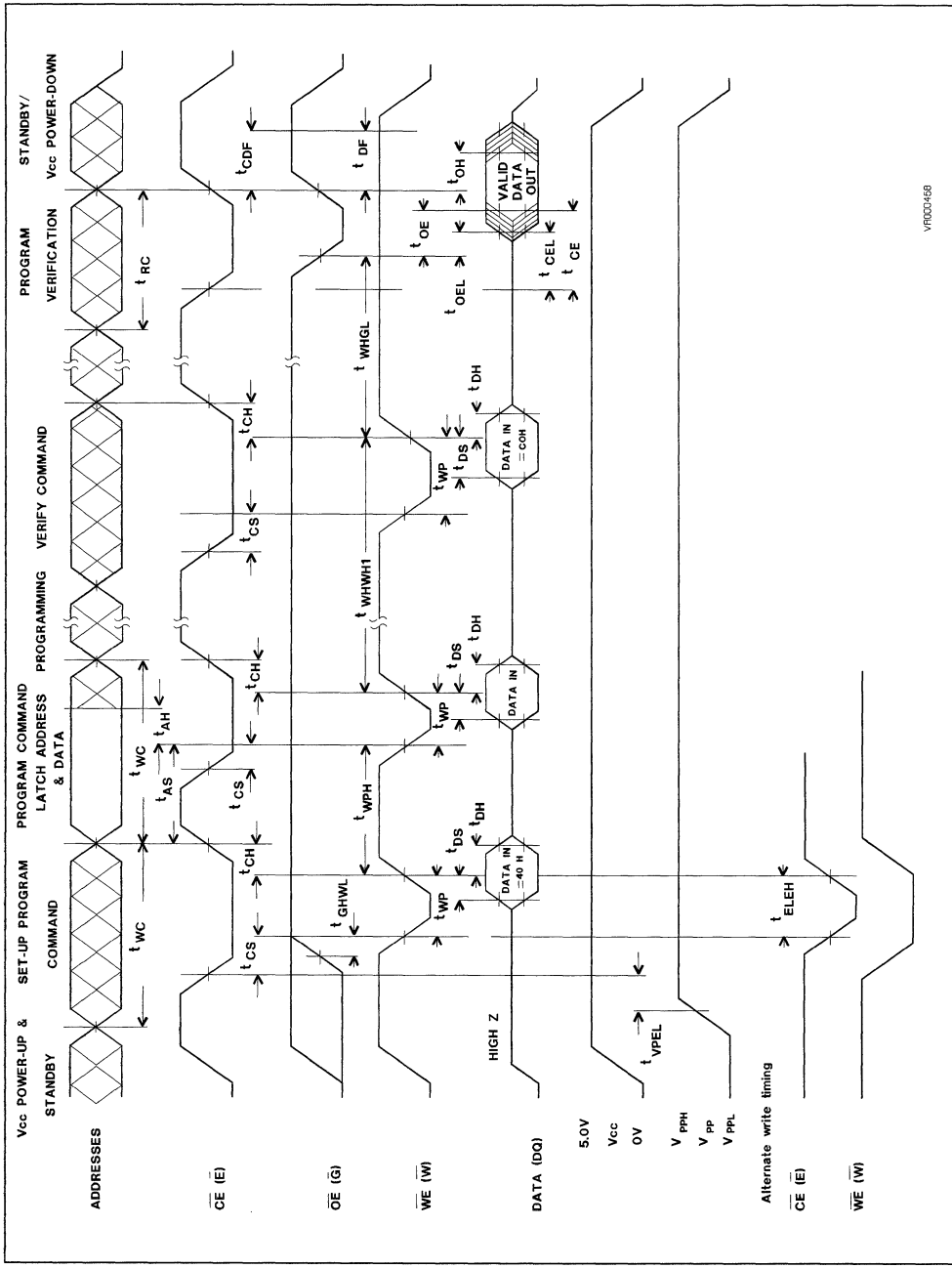
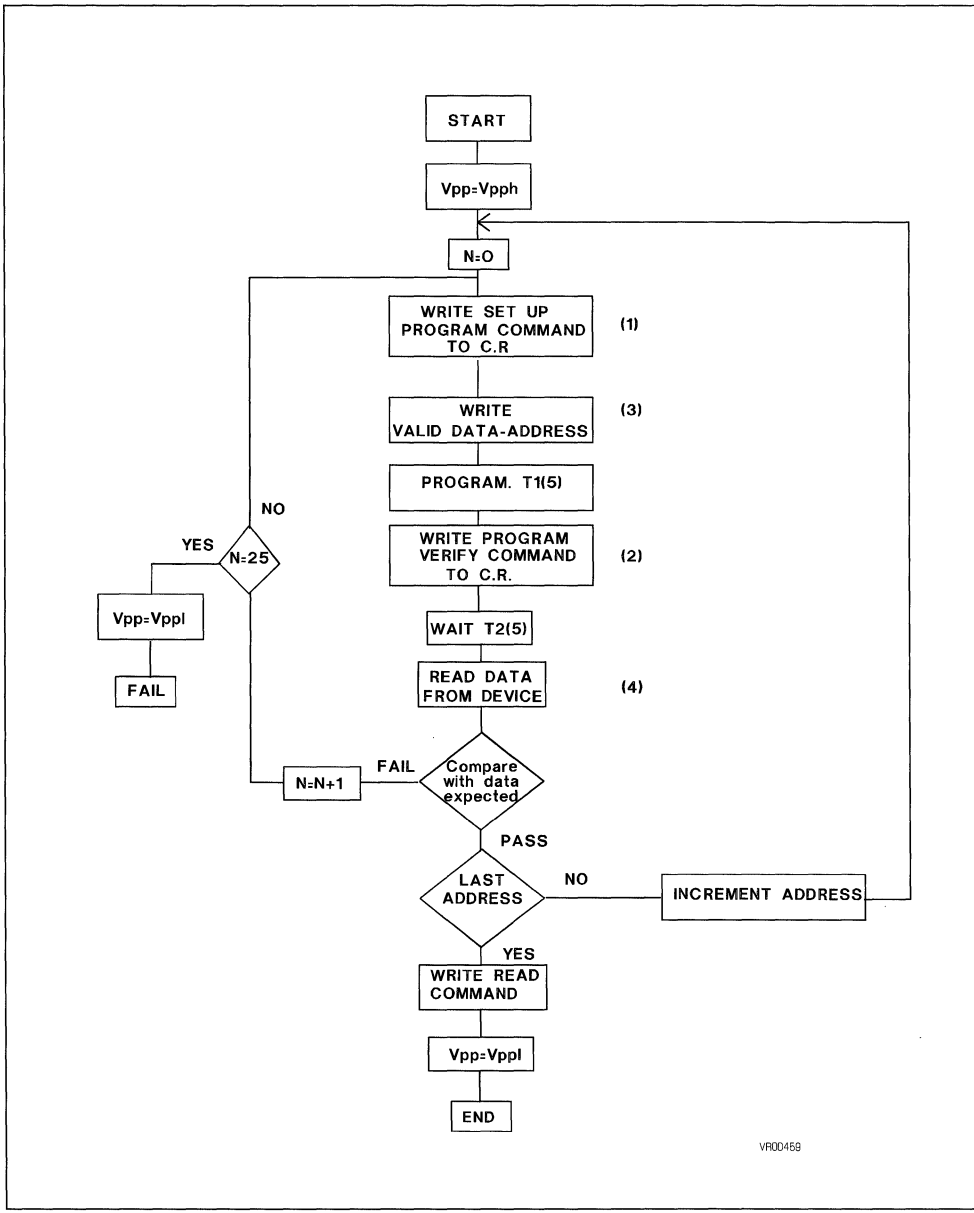


Figure 4 : Presto F Programming Algorithm



Notes : (1) C.R. = Command Register.
(2) STOPS program generation - program verify command is only performed after byte programming.
(3) Second bus cycle of the setup Program/Program command (See Table 5 and Fig 4) starts programming operation.
(4) Second bus cycle of the program verify command (See Table 5 and Fig 4).
(5) T1 = 100µs, T2 = 6µs

Figure 5 : A.C. Waveforms for Erase Operations

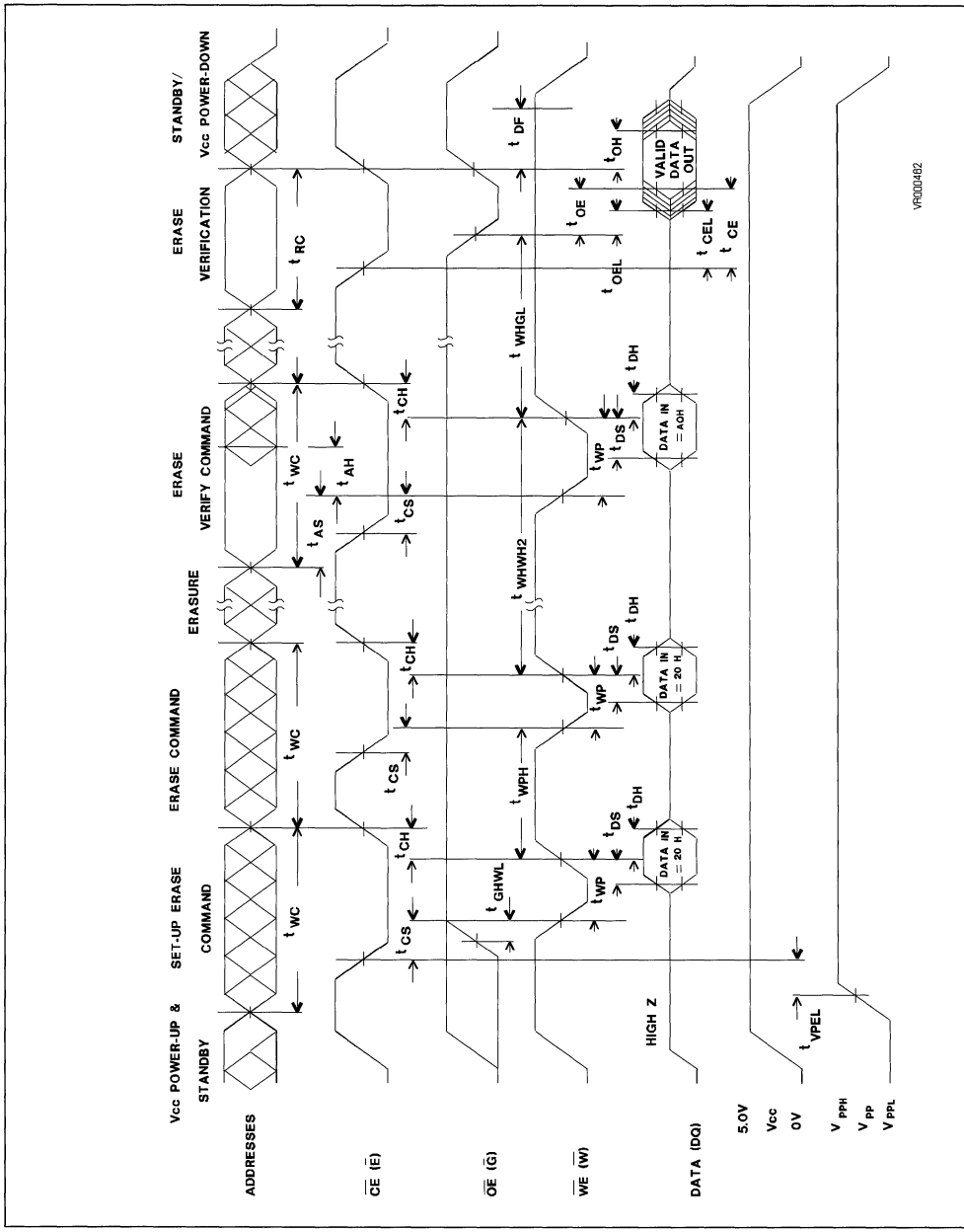
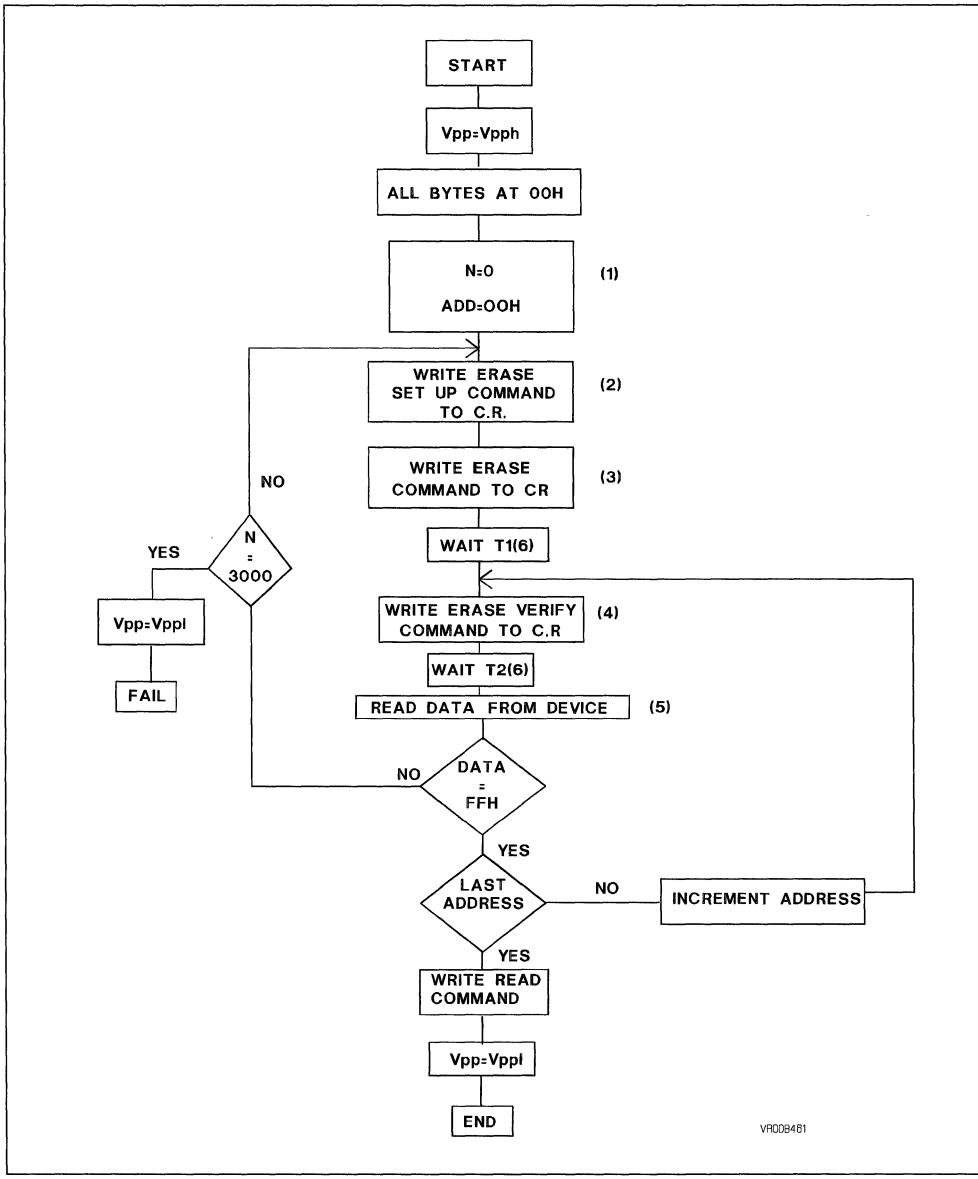
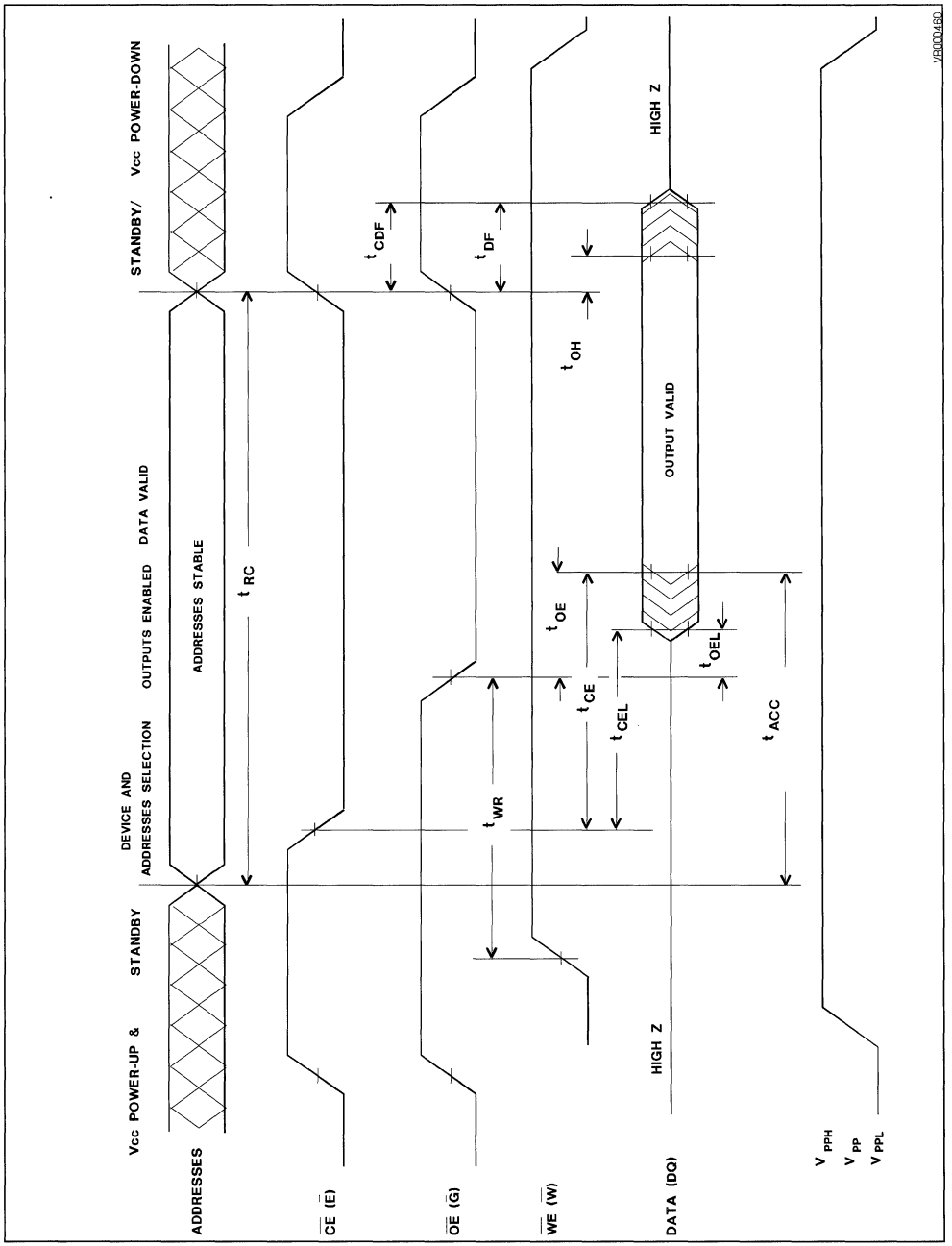


Figure 6 : Presto F Erase Algorithm



Notes : (1) N = Pulse Count.
(2) CR = Command Register.
(3) Second Bus Cycle of Setup Erase/Erase command (see Table 5 and Fig. 5).
(4) Address = byte to verify. Erase verify is only performed after chip Erasure.
(5) Second bus cycle of Erase verify command.
(6) T1 = 10ms, T2 = 6µs.

Figure 7 : A.C. Waveforms for Read Operations



PACKAGE MECHANICAL DATA

Figure 8 : 32 PIN CERAMIC DUAL IN LINE FREAT SEAL

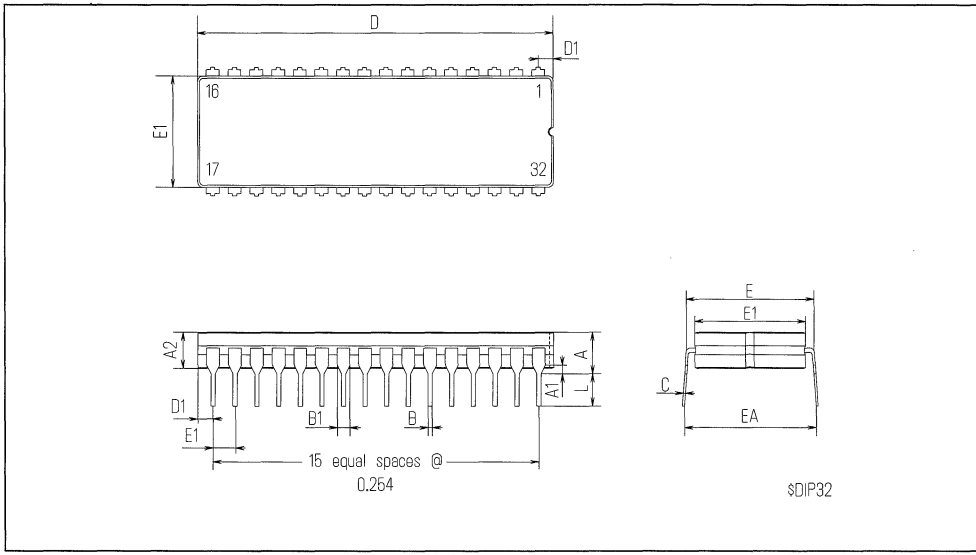
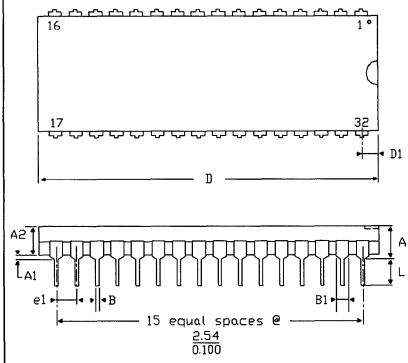
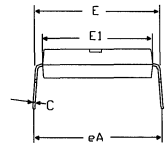


Figure 9 : 32 PIN PLASTIC DUAL IN LINE

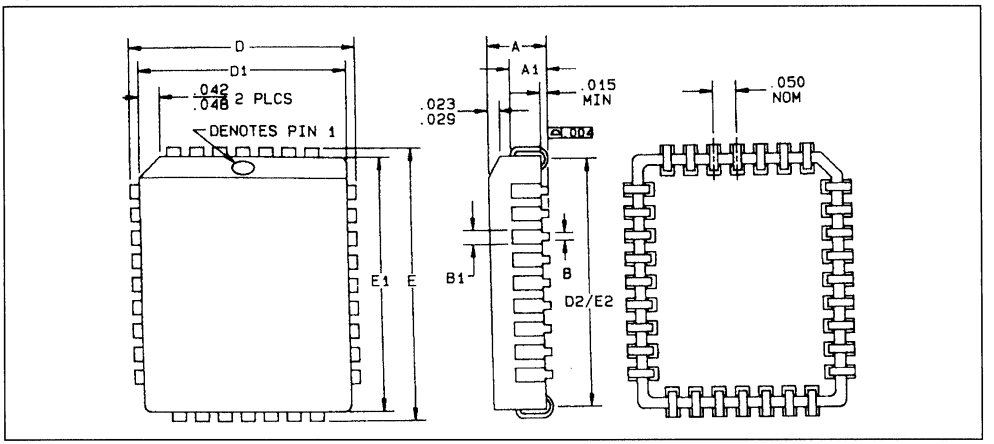


VR000288



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.38					
a1	0.20			0.015		
B		0.46			0.018	
B1			0.30	0.008		0.012
B2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e3		35.60			1.400	
e4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L	3.18		3.43	0.125		0.135

Figure 10 : 32 PIN PLCC



ORDERING INFORMATION

M	2	8	F	1	0	0	1	-	1	2	X	C	1	1	2

REPROGRAM CYCLES 10^X
2 = 100 CYLES
3 = 1000 CYCLES
4 = 10000 CYCLES

SPEED/10

ERASE/PROGRAM VOLTAGE
1 = 12 ± 5% V

V_{CC} MARGIN
X= ± 5%
- = ± 10%

TEMPERATURE RANGE
1 = 0 TO 70°C
3 = -40 TO 125°C
6 = -40 TO 85°C
7 = -40 TO 105°C

PACKAGE
C = PLCC
B = PLASTIC DIL
F = CERAMIC FRIT SEAL

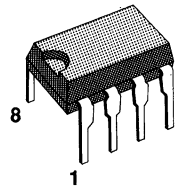
EEPROM DEVICES

IC2 PRODUCT LINE

2K BIT (256 X 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

- 256 X 8 BIT ORGANIZATION.
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- SINGLE POWER SUPPLY (READ AND WRITE)
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 4 BYTES)
- PAGE WRITE CAPABILITY
- SELF-TIMED PROGRAMMING CYCLE
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ
- LOW POWER CMOS
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY
- OVER 1 MILLION ERASE/WRITE CYCLES
- OVER 10 YEARS DATA RETENTION



PDIP8 PSO8

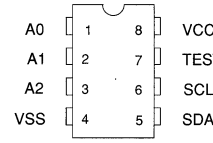
(Ordering information at the end of the datasheet)

PIN NAMES

A0-A1-A2	Address Inputs
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

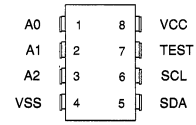
PIN CONNECTION

Dual-in-line Package - top view



VR00B224

SO Package - top view



VR00B232

DESCRIPTION

The ST24C02A is a 2048 read/write non volatile memory organized in 256 words of 8 bits and is manufactured in SGS-THOMSON highly reliable CMOS EEPROM technology.

It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

The 2K bits memory capacity is divided in 256 registers of 8 bits. All memory operations are synchronized on an external strobe: SCL bus. The Read and Write operations are initiated by a Start instruction sent on the SDA bus by the master device.

The Start instruction includes a Start condition followed by an 8 bit word : the seven first bits address the right EEPROM slave device and the last bit defines the kind of operation to follow - Read or Write. A Start instruction is ended by an acknowledge of the slave device.
The specific address of a given ST24C02A is hardwired through the 3 address pins A0,A1 and A2.
The ST24C02A features 3 kind of operations:

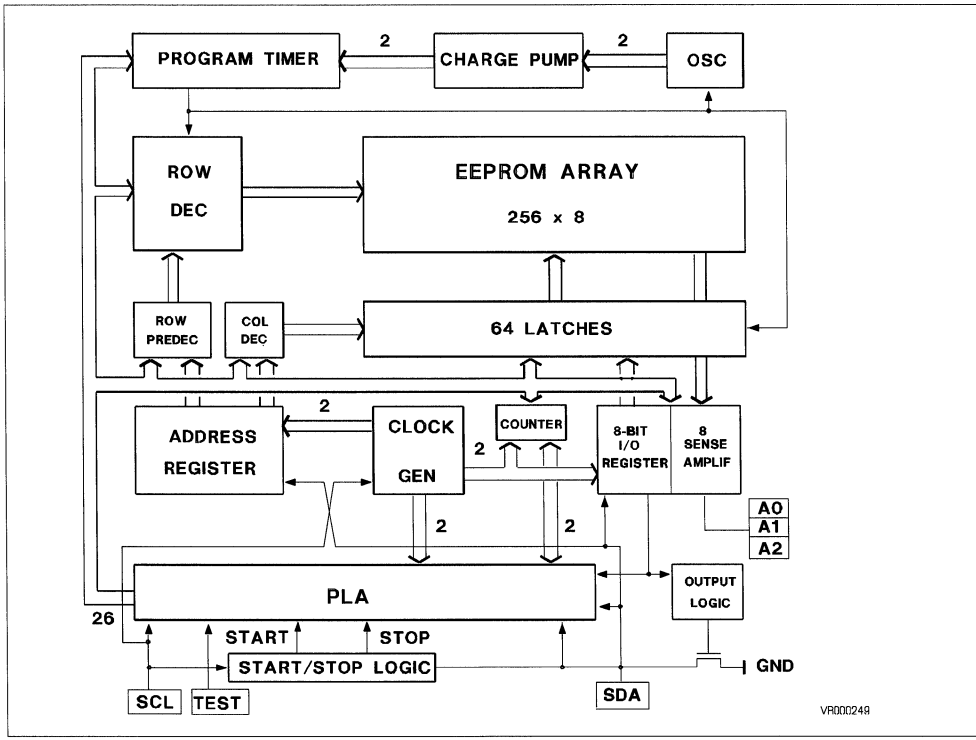
- Byte Write: 8 bits are written at the address previously defined in the byte write operation mode.
- Multibyte programming which allows to write consecutively up to 4 words in any location of the memory array in a single programming cycle.
- Page Write mode which allows to write from 2 to 8 bytes in a single programming cycle.

In Read Mode 3 read operations are available for the user:

- The Current Address read performs a read operation at the previously pointed address incremented by one.
- The Random Read realizes a read at the address defined in the random read instruction.
- The Sequential Read performs either a Current Address read or a Random Read, but reads consecutive words provided the master device acknowledges each string of 8 bits read from the memory without generating a STOP condition.

The design of the ST24C02A and its processing with a highly reliable technology yields to typical endurance better than 1 million cycles and Data Retention greater than 10 years.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	- 65 to 150	°C
Input or Output Voltage with respect to ground	- 0.3 to 6.5	V
Lead Temperature (soldering, 10 seconds)	+ 300	°C
ESD Rating	2000	V

OPERATING CONDITIONS

Ambient Operating Temperature		
ST24C02A-1	0 to + 70	°C
ST24C02A-6	- 40 to +85	°C
ST24C02A-3	- 40 to + 125	°C
POWER SUPPLY	4.5 to 5.5	V

D.C. OPERATING CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range V_{CC} = 5V ±10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC}	Power Supply Current			2	mA	f_{SCL} = 100kHZ
I_{SB}	Standby Current		100		µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND or V_{CC}
I_{LO}	Ouput Leakage Current			10	µA	V_{OUT} = GND or V_{CC}
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 0.7xV_{cc}		.3xV_{cc} V_{cc} + 1.0	V V	
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 V_{cc} - 0.5		+ 0.5 V_{cc} + 1.0	V V	A0, A1, A2 inputs A0, A1, A2 inputs
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

A.C. CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range
V_{CC} = 5V ±10%

SYMBOL		MIN.	TYP.	MAX.	UNITS
f_{SCL}	SCL Clock Frequency	0		100	kHZ
T_I	Noise Suppression Time Constant on SCL, SDA Inputs			100	ns
t_{AA}	SCL Low to SDA Data Valid	0.3		3.5	µs
t_{BUF}	Time the bus must be be free before a new transmission.	4.7			µs
$t_{HD:STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	Clock Low Period	4.7			µs
t_{HIGH}	Clock High Period	4.0			µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated START condition)	4.7			µs
$t_{HD:DAT}$	DATA IN Hold Time	0			ns
$t_{SU:DAT}$	DATA IN Setup Time	250			ns
t_R	SDA & SCL Rise Time			1	µs
t_F	SDA & SCL Fall Time			300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4.7			µs
t_{DH}	DATA OUT Hold Time	300			ns
t_{WR}	Programming Time (note 1)			10	ms
Endurance	W/E Cycles	1 million Cycles minimum			

NOTE 1 : In multibyte programming mode and only in this mode, if the accessed words are located in two consecutive rows the maximum programming time will be extended to two times t_{WR}.

FIGURE 1 : BUS TIMING

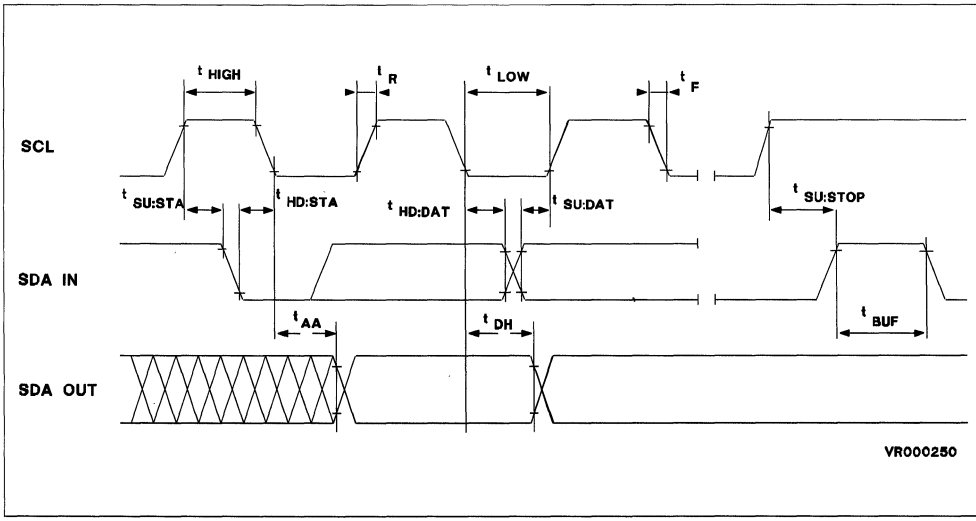
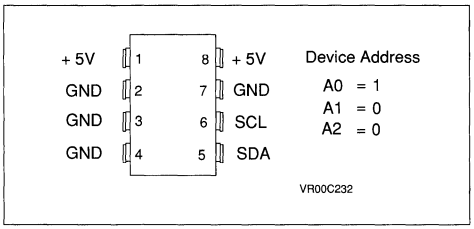


FIGURE 2 : TYPICAL INTERFACE



PIN DESCRIPTION

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into or out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into or out of the device. It is an open drain output that may be wired with any open drain or open collector outputs to formed the system SDA bus.

ADDRESSES (A0,A1,A2)

These three addresses inputs are used to set the least significant bits of the seven bit slave address.These inputs can be used static or seven. When used statically they must be tied to V_{CC} or V_{SS}. When used driven CMOS levels have to applied to the device.

TEST PIN (TEST)

For proper device operation this input must be tied to V_{SS} or V_{CC} According to the voltage on TEST pin up to four or eight bytes may be written in the ST24C02A in a single write operation (see "Write Operation" section.)

DEVICE OPERATION

The ST24C02A supports the I^2C (bidirectional bus oriented) protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being control-led is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. Therefore, the ST24C02A will be considered as a slave receiver or transmitter in all applications.

DATA TRANSITION

Data transition on the SDA line must only occur when the clock SCL is Low. SDA transitions while SCL is HIGH will be interpreted as START or STOP conditions. (See Fig 1).

START CONDITION

A START condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The ST24C02A continuously monitors the SDA and SCL lines for a START and will not respond to any command if this condition has not been met.

STOP CONDITION

A STOP condition is defined by a LOW to HIGH transition of the SDA line while the SCL is at a stable HIGH level. This condition terminates communication between devices and forces the ST24C02A in the standby power mode.

ACKNOWLEDGE

Acknowledge is used to indicate successfull data transfer. The transmitter (master or slave) will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line LOW to indicate it received the 8 bits of data.

DATA TRANSFER

During Data Transfer the ST24C02A samples the SDA line on the leading edge of SCL clock.Therefore,for proper device operation SDA line must be stable during the SCL LOW to HIGH transition.

NOTE

In the I^2C protocol ,the SDA bus must be connected to the positive power supply through a pull-up resistor.

DEVICE ADDRESSING

To start communication between two devices, the bus master must initiate a start instruction sequence; following a START condition the master sends onto the SDA bus an eight bit word correspondind to the address of the device it is addressing.

- The most significant 4 bits of the slave address, therefore the first bits sent onto the bus are the device type identifier. The ST24C02A memory device type is fixed as "1010".

- The next 3 significant bits are used to address a particular device of the previously defined type connected to the bus. The state of the hardwired A0,A1 and A2 pins defines the device address. Up to eight ST24C02A can be connected on the same bus.
- The last bit of the start instruction defines the type of operation to be performed:
  When set to "1" a read operation is selected
  When set to "0" a write operation is selected.

Chip selection is accomplished by setting the three bits of the chip address field to the corresponding levels of A0,A1 and A2 inputs. After a START condition is detected all ST24C02A connected to the bus will compare the slave address being transmitted with their own hardwired address (A0 to A2). After comparison , the selected ST24C02A will acknowledge on the SDA line and will perform the read or write operation according to the state of the R/W bit.

WRITE OPERATION

The standard operation mode is byte write or multibyte programming. If pin 7 is forced to VSS the ST24C02A switches to page mode.

BYTE WRITE

In this mode, following a START condition the master sends a slave address word with the R/W bit set to "0". The ST24C02A will acknowledge this first transmission and waits for a second word : the word address field.This 8 bit address field provides access to any of the 256 words of the memory array. Upon receipt of the word address the ST24C02A slave device will respond with an acknowledge.
At this time, all following words transmitted to the ST24C02A will be considered as Data.
In Byte Write mode the master sends one word which is acknowledged by the ST24C02A .

FIGURE 3 : SLAVE ADDRESS ALLOCATION

	Device type				Device Address			
START	1	0	1	0	A2	A1	A0	R/W
	Slave Address							

Then the master terminates the transfer by generating a STOP condition.
This STOP condition initiates the internal self-timed programming cycle.
While the internal programming cycle is in progress the ST24C02A will not respond to any request from the bus master.

MULTIBYTE PROGRAMMING

The ST24C02A is able to write consecutively up to 4 bytes in the multibyte programming mode.
As in the Byte Write programming mode,the multibyte programming can be started at any specified address and whithout any restriction of any kind.
This multibyte mode is started and performed in the same way as the Byte Write mode; but instead of terminating the write sequence after the first data word is transfered,the master does not generate a STOP condition and up to 3 additional words can be transmitted to the ST24C02A. After receipt of each word,the ST24C02A will respond with an acknowledge.
After the bytes to be written (4 bytes maximun) have been transfered, the master generates a STOP condition which starts the internal self-timed programming cycle.

PAGE WRITE (only available if pin 7 is grounded)

The ST24C02A is able to write up to 8 bytes in a Page Write operation. This mode allows to write 2 to 8 bytes in a single write cycle provided they are all topologically located in the same physical row(five most significant address bits identical.).
This mode is started and performed in the same way as the byte write operation, but instead of terminating the write sequence after the first data word is transfered, the master doesn't generate a STOP condition and can transmit up to seven additional words. After receipt of each word the ST24C02A will respond with an acknowledge.
After receipt of each data word the internal address counter is automatically incremented by one.
Only the three low order address bits are incremented, the high order five bits remain constant.
Therefore, a special attention has to be paid when using this feature in order to avoid any scrambling or over writing.
If more than 8 words are transmitted the address counter will "roll-over" and the previously written

data will be overwritten. As in byte write operation the master terminates the transfer by generating a stop condition that triggers the internal programming cycle. All inputs are disabled until completion of the internal write cycle.

READ OPERATION

Read operations are initiated in the same manner as the write operation with the exception that the R/W bit following the slave address in the start instruction is set to a logical "1". Three read operation modes are available:

. current address read
. random read
. sequential read

CURRENT ADDRESS READ

The ST24C02A has an internal address counter that points the address of the last word accessed incremented by one. Therefore if the last access (either read or write) was to address n, the next current read operation will access data from address n+1. To initiate this read mode the master generates a start instruction (START condition followed by the eight bit slave address word) with the R/W bit set to one. The ST24C02A will respond with an acknowledge and transmit the 8 bits of data. To terminate the transfer the master MUST not acknowledge the transfer but DOES generate a STOP condition.

RANDOM READ

The random read mode allows the master to access any memory location. In order to load into the device the word address the master must first performed a "dummy" write sequence.(START, slave address ,R/W bit set to "0",followed by the word address to be read). After the word address has been acknowledged,the master immediately reissues a START instruction whith the R/W bit set to "1". The ST24C02A will acknowledge the transfer and output the 8 bits of the addressed word. As in current address read to terminate the transfer the master MUST not acknowledge the transfer but DOES generate a STOP condition.

SEQUENTIAL READ

This mode can be initiated with either a current address read or random read. The first word read out of the memory is transmitted in the same way as in both previous modes,however the master must now acknowledge the transfer indicating it requires more data. The ST24C02A will output a string of eight bits for each acknowledge it received. As in the other read modes to terminate the transfer the master MUST not acknowledge the last transfer but DOES generate a STOP condition.

The data output is sequential;data from address n followed by data from address n+1. The internal address counter is automaticaly incremented allowing the entire content of the 256 word memory to be serially read in a single read operation. If more than 256 words are read the counter will "roll-over" and the ST24C02A will continue to output data from the memory.

SDA BUS IN READ MODE

In all read modes the ST24C02A is waiting for an acknowledge (SDA line low) on the 9th clock pulse of a data transfer. If an acknowledge is not detected,the ST24C02A terminates the data transfer and switches to a "receiver" state.

TIMING DIAGRAMS

FIGURE 4 : BYTE WRITE

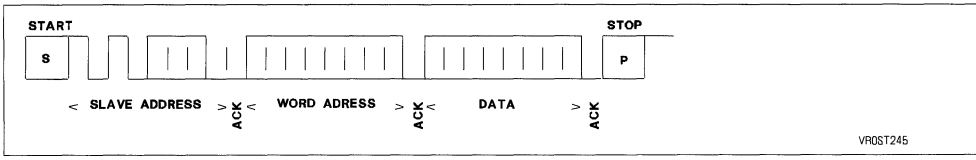


FIGURE 5 : PAGE WRITE

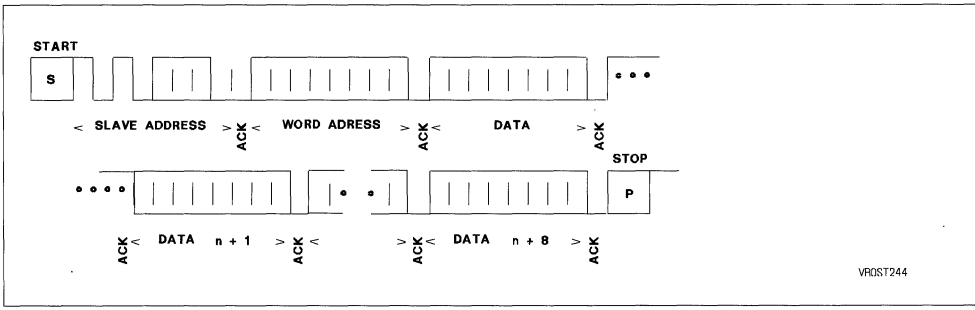


FIGURE 6 : CURRENT ADDRESS READ

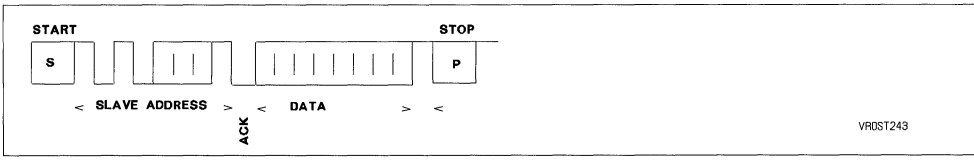


FIGURE 7 : RANDOM ADDRESS READ

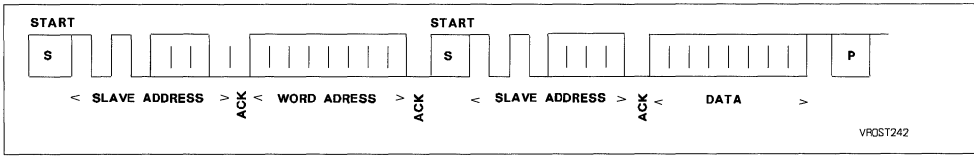
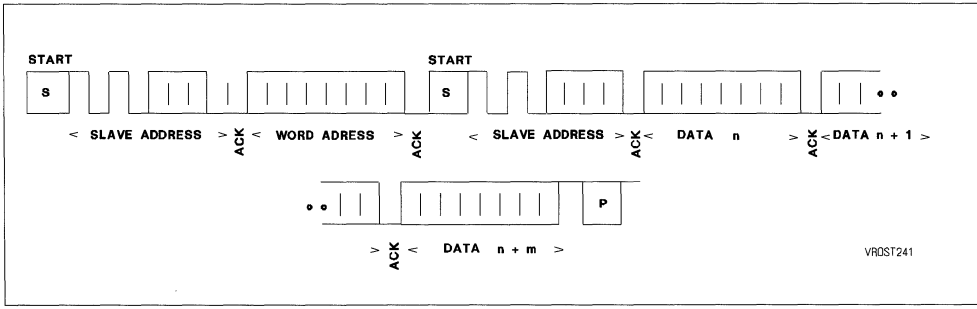


FIGURE 8 : SEQUENTIAL READ

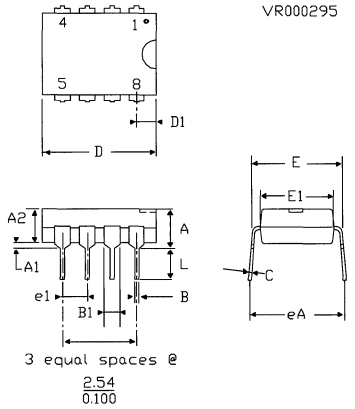


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST24C02AB1	Dual-in-line	0°C to 70°C	4.5V to 5.5V
ST24C02AM1	SO 8		
ST24C02AB6	Dual-in-line	-40°C to 85°C	
ST24C02AM6	SO 8		
ST24C02AB3	Dual-in-line	-40°C to 125°C	
ST24C02AM3	SO 8		

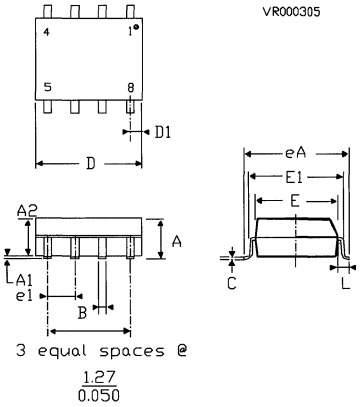
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)

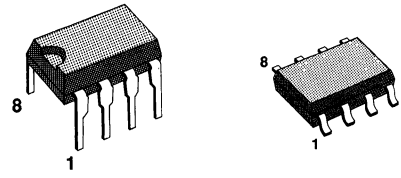


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

2K BIT (256 X 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

- 256 X 8 BIT ORGANIZATION.
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- 2.5V TO 5.5V POWER SUPPLY (READ AND WRITE)
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 4 BYTES)
- PAGE WRITE CAPABILITY
- SELF-TIMED PROGRAMMING CYCLE
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ
- LOW POWER CMOS
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY
- OVER 1 MILLION ERASE/WRITE CYCLES
- OVER 10 YEARS DATA RETENTION
- FUNCTIONAL COMPATIBILITY WITH ST24C02A



PDIP8 SO8

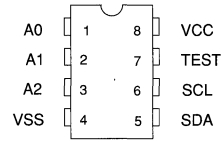
(Ordering information at the end of the datasheet)

PIN NAMES

A0-A1-A2	Address Inputs
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

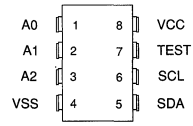
PIN CONNECTION

Dual-in-line Package - top view



VR00B224

SO Package - top view



VR00B232

DESCRIPTION

The ST25C02A is a 2048 read/write non volatile memory organized in 256 words of 8 bits and is manufactured in SGS-THOMSON highly reliable CMOS EEPROM technology. The ST25C02A works with a power supply as low as 2.5V.

It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

The 2K bits memory capacity is divided in 256 registers of 8 bits. All memory operations are synchronized on an external strobe: SCL bus. The Read and Write operations are initiated by a Start

instruction sent on the SDA bus by the master device.

The Start instruction includes a Start condition followed by an 8 bit word : the seven first bits address the right EEPROM slave device and the last bit defines the kind of operation to follow - Read or Write. A Start instruction is ended by an acknowledge of the slave device.

The specific address of a given ST25C02A is hardwired through the 3 address pins A0,A1 and A2.

The ST25C02A features 3 kind of operations:

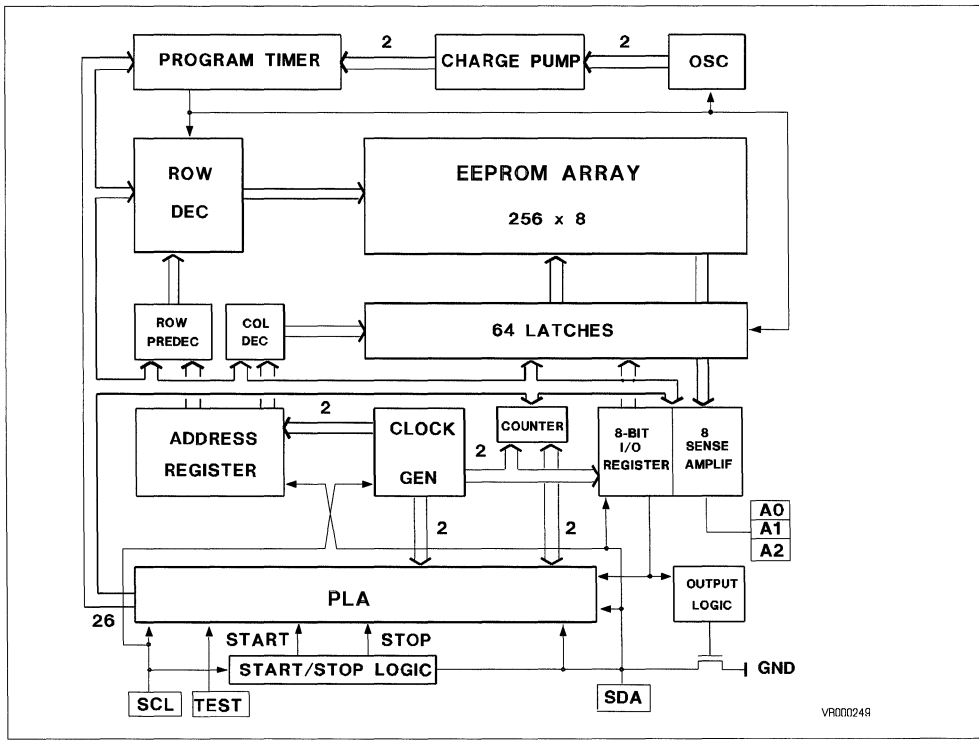
- Byte Write: 8 bits are written at the address previously defined in the byte write operation mode.
- Multibyte programming which allows to write consecutively up to 4 words in any location of the memory array in a single programming cycle.
- Page Write mode which allows to write from 2 to 8 bytes in a single programming cycle.

In Read Mode 3 read operations are available for the user:

- The Current Address read performs a read operation at the previously pointed address incremented by one.
- The Random Read realizes a read at the address defined in the random read instruction.
- The Sequential Read performs either a Current Address read or a Random Read, but reads consecutive words provided the master device acknowledges each string of 8 bits read from the memory without generating a STOP condition.

The design of the ST25C02A and its processing with a highly reliable technology yields to typical endurance better than 1 million cycles and Data Retention greater than 10 years.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	- 65 to 150	°C
Input or Output Voltage with respect to ground	- 0.3 to 6.5	V
Lead Temperature (soldering, 10 seconds)	+ 300	°C
ESD Rating	2000	V

OPERATING CONDITIONS

Ambient Operating Temperature		
ST25C02A-1	0 to + 70	°C
ST25C02A-6	- 40 to +85	°C
ST25C02A-3	- 40 to + 125	°C
POWER SUPPLY	2.5 to 5.5	V

D.C. OPERATING CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range V_{CC} =2.5V min, 5.5V maxi

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC}	Power Supply Current			2	mA	f_{SCL} = 100kHZ
I_{SB}	Standby Current		100		µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND or V_{CC}
I_{LO}	Ouput Leakage Current			10	µA	V_{OUT} = GND or V_{CC}
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 $0.7xV_{cc}$		$0.3xV_{cc}$ V_{cc}+1.0	V V	
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 V_{cc} - 0.5		+ 0.5 V_{cc} + 1.0	V V	A0, A1, A2 inputs A0, A1, A2 inputs
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA

A.C. CHARACTERISTICS Ta= -40°C to 125°C according to selected temperature range
V_{CC}=2.5V min, 5.5V maxi

SYMBOL		MIN.	TYP.	MAX.	UNITS
f_{SCL}	SCL Clock Frequency	0		100	kHZ
T_I	Noise Suppression Time Constant on SCL, SDA Inputs			100	ns
t_{AA}	SCL Low to SDA Data Valid	0.3		3.5	µs
t_{BUF}	Time the bus must be be free before a new transmission.	4.7			µs
$t_{HD:STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	Clock Low Period	4.7			µs
t_{HIGH}	Clock High Period	4.0			µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated START condition)	4.7			µs
$t_{HD:DAT}$	DATA IN Hold Time	0			ns
$t_{SU:DAT}$	DATA IN Setup Time	250			ns
t_R	SDA & SCL Rise Time			1	µs
t_F	SDA & SCL Fall Time			300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4.7			µs
t_{DH}	DATA OUT Hold Time	300			ns
t_{WR}	Programming Time (note 1)			10	ms
Endurance	W/E Cycles	1 million Cycles minimum			

NOTE 1 : In multibyte programming mode and only in this mode, if the accessed words are located in two consecutive rows the maximum programming time will be extended to two times t_{WR}.

FIGURE 1 : BUS TIMING

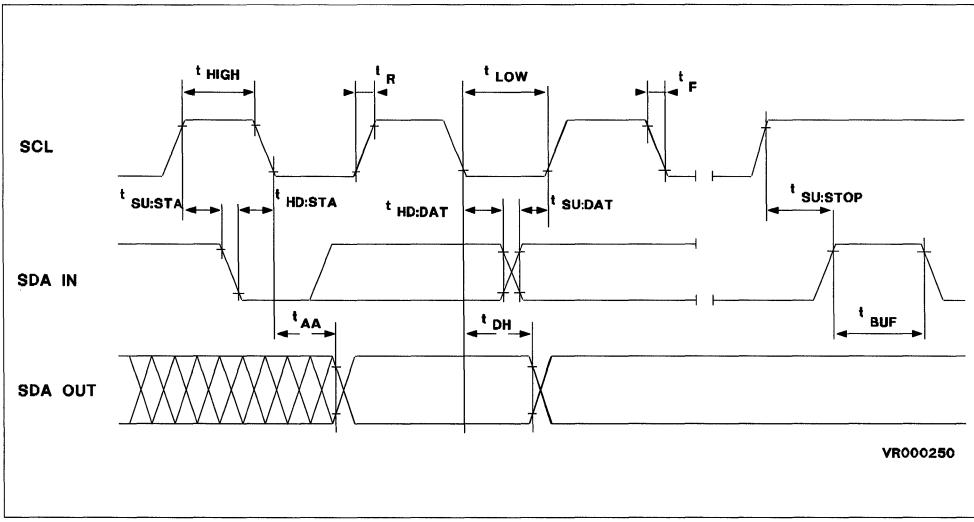
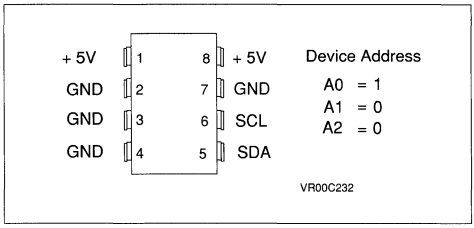


FIGURE 2 : TYPICAL INTERFACE



PIN DESCRIPTION

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into or out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into or out of the device. It is an open drain output that may be wired with any open drain or open collector outputs to formed the system SDA bus.

ADDRESSES (A0,A1,A2)

These three addresses inputs are used to set the least significant bits of the seven bit slave address.These inputs can be used static or seven. When used statically they must be tied to V_{CC} or V_{SS}. When used driven CMOS levels have to applied to the device.

TEST PIN (TEST)

For proper device operation this input must be tied to V_{SS} or V_{CC} According to the voltage on TEST pin up to four or eight bytes may be written in the ST25C02A in a single write operation (see "Write Operation" section.)

DEVICE OPERATION

The ST25C02A supports the I^2C (bidirectional bus oriented) protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being control-led is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. Therefore, the ST25C02A will be considered as a slave receiver or transmitter in all applications.

DATA TRANSITION

Data transition on the SDA line must only occur when the clock SCL is Low. SDA transitions while SCL is HIGH will be interpreted as START or STOP conditions. (See Fig 1).

START CONDITION

A START condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The ST25C02A continuously monitors the SDA and SCL lines for a START and will not respond to any command if this condition has not been met.

STOP CONDITION

A STOP condition is defined by a LOW to HIGH transition of the SDA line while the SCL is at a stable HIGH level. This condition terminates communication between devices and forces the ST25C02A in the standby power mode.

ACKNOWLEDGE

Acknowledge is used to indicate successfull data transfer. The transmitter (master or slave) will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line LOW to indicate it received the 8 bits of data.

DATA TRANSFER

During Data Transfer the ST25C02A samples the SDA line on the leading edge of SCL clock.Therefore,for proper device operation SDA line must be stable during the SCL LOW to HIGH transition.

NOTE

In the I^2C protocol ,the SDA bus must be connected to the positive power supply through a pull-up resistor.

DEVICE ADDRESSING

To start communication between two devices, the bus master must initiate a start instruction sequence; following a START condition the master sends onto the SDA bus an eight bit word correspondind to the address of the device it is addressing.

- The most significant 4 bits of the slave address, therefore the first bits sent onto the bus are the device type identifier. The ST25C02A memory device type is fixed as "1010".

- The next 3 significant bits are used to address a particular device of the previously defined type connected to the bus. The state of the hardwired A0,A1 and A2 pins defines the device address. Up to eight ST25C02A can be connected on the same bus.
- The last bit of the start instruction defines the type of operation to be performed:
  When set to "1" a read operation is selected
  When set to "0" a write operation is selected.

Chip selection is accomplished by setting the three bits of the chip address field to the corresponding levels of A0,A1 and A2 inputs. After a START condition is detected all ST25C02A connected to the bus will compare the slave address being transmitted with their own hardwired address (A0 to A2). After comparison , the selected ST25C02A will acknowledge on the SDA line and will perform the read or write operation according to the state of the R/W bit.

WRITE OPERATION

The standard operation mode is byte write or multibyte programming. If pin 7 is forced to VSS the ST25C02A switches to page mode.

BYTE WRITE

In this mode, following a START condition the master sends a slave address word with the R/W bit set to "0". The ST25C02A will acknowledge this first transmission and waits for a second word : the word address field.This 8 bit address field provides access to any of the 256 words of the memory array. Upon receipt of the word address the ST25C02A slave device will respond with an acknowledge.

At this time, all following words transmitted to the ST25C02A will be considered as Data.

In Byte Write mode the master sends one word which is acknowledged by the ST25C02A .

FIGURE 3 : SLAVE ADDRESS

	Device type				Device Address			
START	1	0	1	0	A2	A1	A0	R/W
	Slave Address							

Then the master terminates the transfer by generating a STOP condition.

This STOP condition initiates the internal self-timed programming cycle.

While the internal programming cycle is in progress the ST25C02A will not respond to any request from the bus master.

MULTIBYTE PROGRAMMING

The ST24C02A is able to write consecutively up to 4 bytes in the multibyte programming mode.

As in the Byte Write programming mode,the multibyte programming can be started at any specified address and whithout any restriction of any kind.

This multibyte mode is started and performed in the same way as the Byte Write mode; but instead of terminating the write sequence after the first data word is transfered,the master does not generate a STOP condition and up to 3 additional words can be transmitted to the ST25C02A. After receipt of each word,the ST25C02A will respond with an acknowledge.

After the bytes to be written (4 bytes maximun) have been transfered, the master generates a STOP condition which starts the internal self-timed programming cycle.

PAGE WRITE (only available if pin 7 is grounded)

The ST25C02A is able to write up to 8 bytes in a Page Write operation. This mode allows to write 2 to 8 bytes in a single write cycle provided they are all topologically located in the same physical row(five most significant address bits identical.).

This mode is started and performed in the same way as the byte write operation, but instead of terminating the write sequence after the first data word is transfered, the master doesn't generate a STOP condition and can transmit up to seven additional words. After receipt of each word the ST25C02A will respond with an acknowledge.

After receipt of each data word the internal address counter is automatically incremented by one.

Only the three low order address bits are incremented, the high order five bits remain constant.

Therefore, a special attention has to be paid when using this feature in order to avoid any scrambling or over writing.

If more than 8 words are transmitted the address counter will "roll-over" and the previously written

data will be overwritten. As in byte write operation the master terminates the transfer by generating a stop condition that triggers the internal programming cycle. All inputs are disabled until completion of the internal write cycle.

READ OPERATION

Read operations are initiated in the same manner as the write operation with the exception that the R/W bit following the slave address in the start instruction is set to a logical "1". Three read operation modes are available:

. current address read
. random read
. sequential read

CURRENT ADDRESS READ

The ST25C02A has an internal address counter that points the address of the last word accessed incremented by one. Therefore if the last access (either read or write) was to address n, the next current read operation will access data from address n+1. To initiate this read mode the master generates a start instruction (START condition followed by the eight bit slave address word) with the R/W bit set to one. The ST25C02A will respond with an acknowledge and transmit the 8 bits of data. To terminate the transfer the master MUST not acknowledge the transfer but DOES generate a STOP condition.

RANDOM READ

The random read mode allows the master to access any memory location. In order to load into the device the word address the master must first performed a "dummy" write sequence.(START, slave address ,R/W bit set to "0",followed by the word address to be read). After the word address has been acknowledged,the master immediately reissues a START instruction whith the R/W bit set to "1". The ST25C02A will acknowledge the transfer and output the 8 bits of the addressed word. As in current address read to terminate the transfer the master MUST not acknowledge the transfer but DOES generate a STOP condition.

SEQUENTIAL READ

This mode can be initiated with either a current address read or random read. The first word read out of the memory is transmitted in the same way as in both previous modes,however the master must now acknowledge the transfer indicating it requires more data. The ST25C02A will output a string of eight bits for each acknowledge it received. As in the other read modes to terminate the transfer the master MUST not acknowledge the last transfer but DOES generate a STOP condition.

The data output is sequential;data from address n followed by data from address n+1. The internal address counter is automaticaly incremented allowing the entire content of the 256 word memory to be serially read in a single read operation. If more than 256 words are read the counter will "roll-over" and the ST25C02A will continue to output data from the memory.

SDA BUS IN READ MODE

In all read modes the ST25C02A is waiting for an acknowledge (SDA line low) on the 9th clock pulse of a data transfer. If an acknowledge is not detected,the ST25C02A terminates the data transfer and switches to a "receiver" state.

TIMING DIAGRAMS

FIGURE 4 : BYTE WRITE

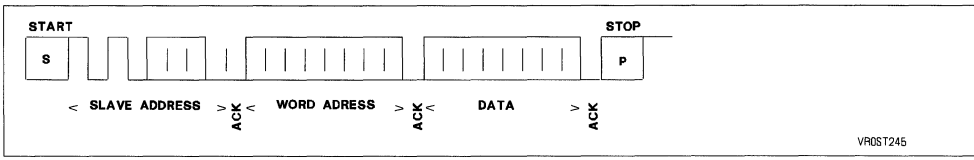


FIGURE 5 : PAGE WRITE

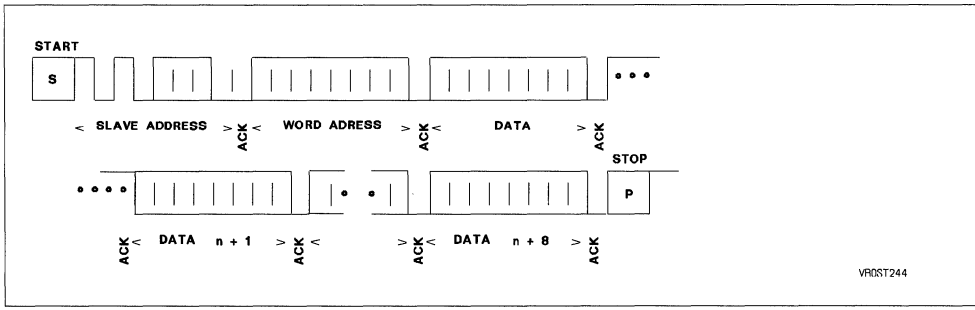


FIGURE 6 : CURRENT ADDRESS READ

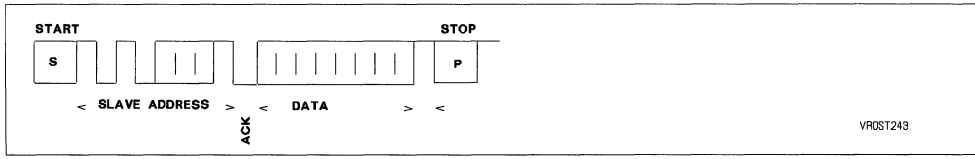


FIGURE 7 : RANDOM ADDRESS READ

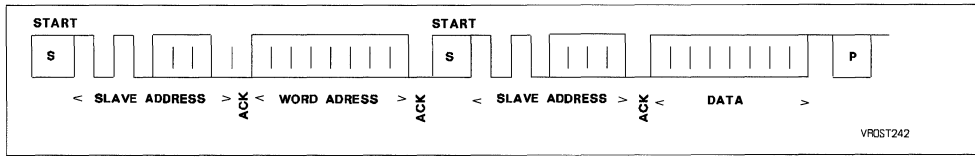
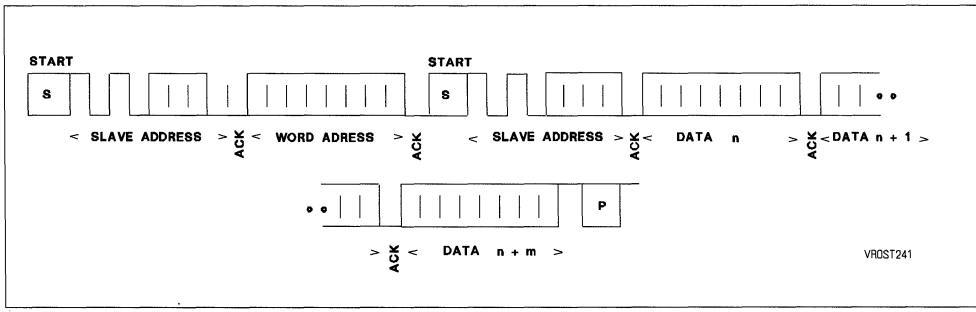


FIGURE 8 : SEQUENTIAL READ

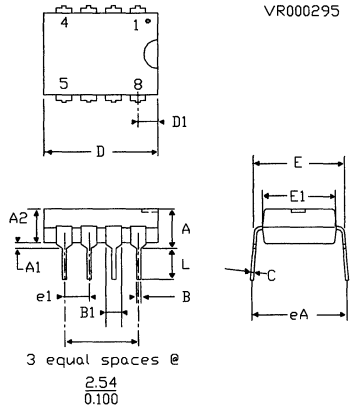


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST25C02AB1	Dual-in-line	0°C to 70°C	2.5V to 5.5V
ST25C02AM1	SO 8		
ST25C02AB6	Dual-in-line	-40°C to 85°C	
ST25C02AM6	SO 8		
ST25C02AB3	Dual-in-line	-40°C to 125°C	
ST25C02AM3	SO 8		

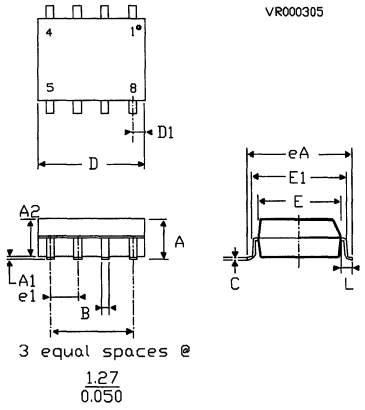
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)

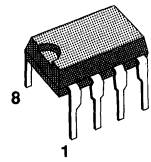


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

4K BIT (512 X 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

- 2 PAGES OF 256 X 8 BITS
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- SINGLE POWER SUPPLY (READ AND WRITE)
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 4 BYTES)
- PART OF MEMORY PROTECTION CAPABILITY
- PAGE WRITE CAPABILITY
- SELF-TIMED PROGRAMMING CYCLE
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ
- LOW POWER CMOS
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY
- OVER 1 MILLION ERASE/WRITE CYCLES
- OVER 10 YEARS DATA RETENTION



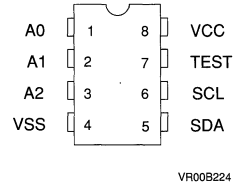
PDIP8 PSO14

(Ordering information at the end of the datasheet)

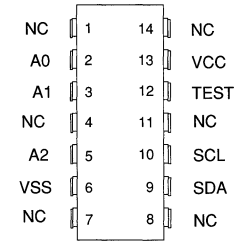
PIN NAMES

A0-A1-A2	Address Inputs
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

PIN CONNECTION



VR00B224



VR000233

DESCRIPTION

The ST24C04 is a 4096 bits read/write non volatile memory organized in 512 words of 8 bits and is manufactured in SGS-THOMSON highly reliable CMOS EEPROM technology.

It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

The 4K bits memory capacity is divided in two pages of 256 words of 8 bits. All memory operations are synchronized on an external strobe: SCL bus. The Read and Write operations are initiated by a Start instruction sent on the SDA bus by the master device.

The Start instruction includes a Start condition followed by an 8 bit word : the seven first bits address the right EEPROM slave device and the last bit defines the kind of operation to follow : Read or Write. A Start instruction is ended by an acknowledge of the slave device. The specific address of a given ST24C04 is hardwired through the 2 address pins A1 and A2.

The ST24C04 features 3 kind of operations:

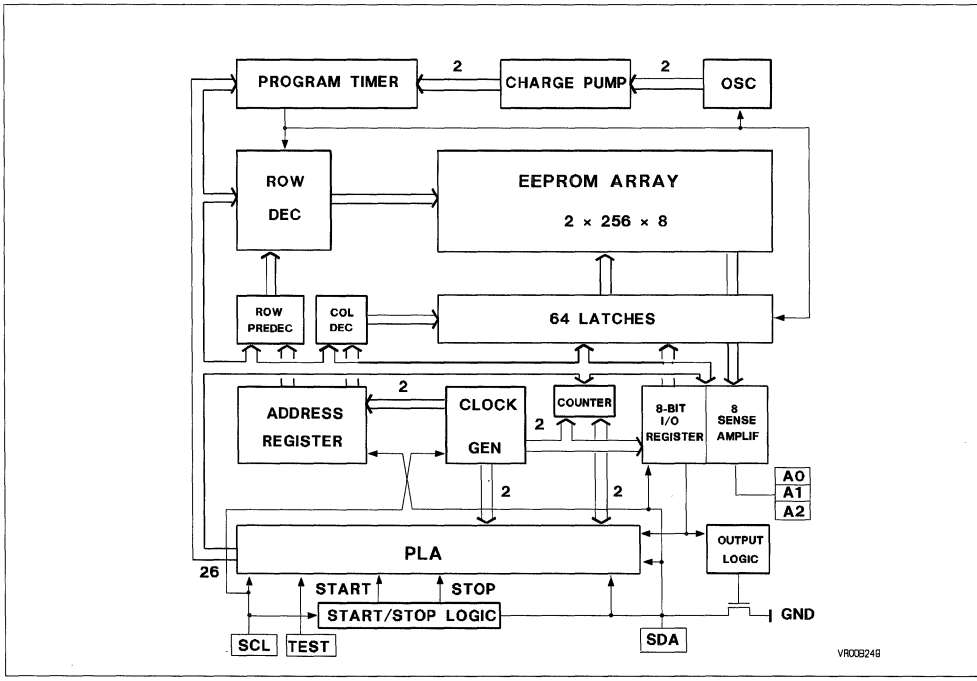
- Byte Write: 8 bits are written at the address previously defined in the byte write operation mode.
- Multibyte programming which allows to write consecutively up to 4 words in any location of the memory array in a single programming cycle.
- Page Write mode which allows to write from 2 to 8 bytes in a single programming cycle.

In Read Mode 3 read operations are available for the user:

- The Current Address read performs a read operation at the previously pointed address incremented by one.
- The Random Read performs a read operation at the address defined in the randon read instruction
- The Sequential Read performs either a Current Address read or a Random Read, but reads consecutive words provided the master device acknowledges each string of 8 bits read from the memory without generating a STOP condition.

The design of the ST24C04 and its processing with a highly reliable technology yields to typical endurance better than 1 million cycles and Data Retention greater than 10 years.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	- 65 to 150	°C
Input or Output Voltage with respect to ground	- 0.3 to 6.5	V
Lead Temperature (soldering, 10 seconds)	+ 300	°C
ESD Rating	2000	V

OPERATING CONDITIONS

Ambient Operating Temperature		
ST24C04-1	0 to 0.70	°C
ST24C04-6	- 40 to +85	°C
ST24C04-3	- 40 to +125	°C
POWER SUPPLY	4.5 to 5.5	V

D.C. OPERATING CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range VCC=5V ±10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC}	Power Supply Current			2	mA	f_{SCL} = 100kHZ
I_{SB}	Standby Current		100		µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND or V_{CC}
I_{LO}	Ouput Leakage Current			10	µA	V_{OUT} = GND or V_{CC}
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 .7xV_{CC}		.3xV_{CC} V_{CC}+1.0	V V	
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 V_{CC} - 0.5		+ 0.5 V_{CC} + 1.0	V V	A0, A1, A2 inputs A0, A1, A2 inputs
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

A.C. CHARACTERISTICS t_a=-40°C to 125°C according to selected temperature range
V_{CC}=5V ±10%, unless otherwise specified

SYMBOL		MIN.	TYP.	MAX.	UNITS
f_{SCL}	SCL Clock Frequency	0		100	kHZ
T_I	Noise Suppression Time Constant on SCL, SDA Inputs			100	ns
t_{AA}	SCL Low to SDA Data Valid	300			ns
t_{BUF}	Time the bus must be be free before a new transmission.	4.7			µs
$t_{HD:STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	Clock Low Period	4.7			µs
t_{HIGH}	Clock High Period	4.0			µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated START condition)	4.7			µs
$t_{HD:DAT}$	DATA IN Hold Time	0			ns
$t_{SU:DAT}$	DATA IN Setup Time	250			ns
t_R	SDA & SCL Rise Time			1	µs
t_F	SDA & SCL Fall Time			300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4.7			µs
t_{DH}	DATA OUT Hold Time	300			ns
t_{WR}	Programming Time (note 1)			10.	ms
Endurance	W/E Cycles	1 million Cycles minimum			

Note 1: in multibyte programming mode and only in this mode,if the accessed words are located in two consecutive rows the maximun programming time will be extended to two times tWR.

FIGURE 1 : BUS TIMING

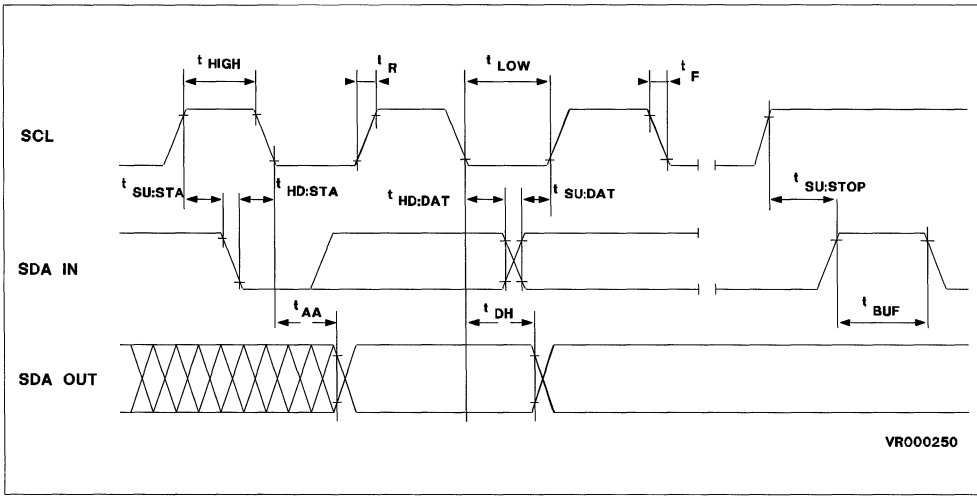
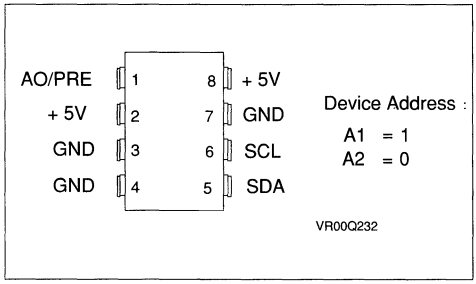


FIGURE 2 : TYPICAL INTERFACE



PIN DESCRIPTION

SERIAL CLOCK (SCL)
The SCL input is used to clock all data into or out of the device.

SERIAL DATA (SDA)
SDA is a bidirectional pin used to transfer data into or out of the device.It is an open drain output that may be wired with any open drain or open collector outputs to formed the system SDA bus.

ADDRESS (A0/PRE)
For proper device operation this pin must be tied to V_{SS} or V_{CC}

- When set to VSS all the memory array can be accessed in read or write mode.
- When set to VCC this pin is considered as a protection key, therefore allowing the upper portion of the memory to be protected in write mode. (See "PROTECT MODE" section in the following pages of the Data sheet).

ADDRESS (A1,A2)
These two addresses inputs are used to set the fifth and sixth bits of the seven bits slave address.These inputs can be used static or driven. When used statically they must be tied to V_{CC} or V_{SS}. When used driven CMOS levels have to applied to the device.

TEST PIN (TEST)
For proper device operation this input must be tied to V_{SS} or V_{CC} According to the voltage on TEST pin up to four or eight bytes may be written in the ST24C04 in a single write operation (see "Write Operation" section.)

DEVICE OPERATION

The ST24C04 supports the I^2C (bidirectional bus oriented) protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. Therefore, the ST24C04 will be considered as a slave receiver or transmitter in all applications.

DATA TRANSITION
Data transition on the SDA line must only occur when the clock SCL is Low. SDA transitions while SCL is HIGH will be interpreted as START or STOP conditions. See Fig 1.

START CONDITION
A START condition is defined by a HIGH to LOW transition of THE SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The ST24C04 continuously monitors the SDA and SCL lines for a START and will not respond to any command if this condition has not been met.

STOP CONDITION
A STOP condition is defined by a LOW to HIGH transition of the SDA line while the SCL is at a stable HIGH level. This condition terminates communication between devices and forces the ST24C04 in the standby power mode.

ACKNOWLEDGE
Acknowledge is used to indicate successfull data transfer. The transmitter (master or slave) will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line LOW to indicate it received the 8 bits of data.

DATA TRANSFER
During Data Transfer the ST24C04 samples the SDA line on the leading edge of SCL clock.Therefore,for proper device operation SDA line must be stable during the SCL LOW to HIGH transition.

Note In the I^2C protocol ,the SDA bus must be connected to the positive power supply through a pull-up resistor.

DEVICE ADDRESSING

To start communication between two devices, the bus master must initiate a start instruction sequence; following a START condition the master sends onto the SDA bus an eight bit word correspondind to the address of the device it is addressing.

- The most significant 4 bits of the slave address , therefore the first bits sent onto the bus are the device type identifier. The ST24C04 memory device type is fixed as "1010".
- The next 2 significant bits are used to address a particular device of the previously defined type connected to the bus. The state of the hardwired A1 and A2 pins defines the device address. Up to four ST24C04 can be connected on the same bus.
- The next bit of the slave address field is the most significant bit of the word address ; it is used as the page select bit.
- The last bit of the start instruction defines the type of operation to be performed:

- When set to "1" a read operation is selected
- When set to "0" a write operation is selected

Chip selection is accomplished by setting the two bits of the chip address field to the corresponding levels of A1 and A2 inputs. After a START condition is detected all ST24C04 connected to the bus will compare the slave address being transmitted with their own hardwired address (A1 and A2). After comparison , the selected ST24C04 will acknowledge on the SDA line and will perform the read or write operation according to the state of the R/W bit.

WRITE OPERATION

The standard operation mode is byte write or multibyte programming. If pin 7 is forced to V_{SS} the ST24C04 switches to page mode.

BYTE WRITE
In this mode, following a START condition the master sends a slave address word with the R/W bit set to "0". The ST24C04 will acknowledge this first transmission and waits for a second word : the word address field.This 8 bit address field provides access to any of the 256 words of the selected page. Upon receipt of the word address the ST24C04 slave device will respond with an acknowledge. At this time, all following words transmitted to the ST24C04 will be considered as Data. In Byte Write mode the master sends one word which is acknowledged by the ST24C04. Then the master terminates the transfer by generating a STOP condition. This STOP condition initiates the internal self-timed programming cycle.

While the internal programming cycle is in progress the ST24C04 will not respond to any request from the bus master.

FIGURE 3 : SLAVE ADDRESS ALLOCATION

	Device type				Device Address		Page	
START	1	0	1	0	A2	A1	A0	R/W
	Slave Address							

MULTIBYTE PROGRAMMING
The ST24C04 is able to write consecutively up to 4 bytes in the multibyte programming mode. As in the Byte Write programming mode,the multibyte programming can be started at any specified address and whithout any restriction of any kind. This multibyte mode is started and performed in the same way as the Byte Write mode; but instead of terminating the write sequence after the first data word is transfered,the master does not generate a STOP condition and up to 3 additional words can be transmitted to the ST24C04. After receipt of each word,the ST24C04 will respond with an acknowledge. After the bytes to be written (4 bytes maximun) have been transfered, the master generates a STOP condition which starts the internal self-timed programming cycle.

PAGE WRITE (only available if pin 7 is grounded)
The ST24C04 is able to write up to 8 bytes in a Page Write operation. This mode allows to write 2 to 8 bytes in a single write cycle provided they are all topologically located in the same physical row.(five most significant address bits identical.)

This mode is started and performed in the same way as the byte write operation, but instead of terminating the write sequence after the first data word is transfered, the master doesn't generate a STOP condition and can transmit up to seven additional words. After receipt of each word the ST24C04 will respond with an acknowledge.

After receipt of each data word the internal address counter is automatically incremented by one. Only the three low order address bits are incremented, the high order five bits remain constant.

Therefore, a special attention has to be paid when using this feature in order to avoid any scrambling or over writing. If more than 8 words are transmitted the address counter will "rollover" and the previously written data will be overwritten. As in byte write operation the master terminates the transfer by generating a stop condition that triggers the internal programming cycle.

All inputs are disabled until completion of the internal write cycle.

READ OPERATIONS

Read operations are initiated in the same manner as the write operation with the exception that the R/W bit following the slave address in the start instruction is set to a logical "1". Three read operation modes are available:

- current address read
- random read
- sequential read

CURRENT ADDRESS READ

The ST24C04 has an internal address counter that points the address of the last word accessed incremented by one. Therefore if the last access (either read or write) was to address n, the next current read operation will access data from address n+1. To initiate this read mode the master generates a start instruction (START condition followed by the eight bit slave address word) with the R/W bit set to one. The ST24C04 will respond with an acknowledge and transmit the 8 bits of data. To terminate the transfer the master MUST not acknowledge the transfer and DOES generate a STOP condition.

RANDOM READ

The random read mode allows the master to access any memory location. In order to load into the device the word address the master must first performed a "dummy" write sequence.(START, slave address ,R/W bit set to "0",followed by the word address to be read). After the word address has been acknowledged,the master immediately reissues a START instruction whith the R/W bit set to "1". The ST24C04 will acknowledge the transfer and output the 8 bits of the addressed word. As in current address read to terminate the transfer the master MUST not acknowledge the transfer and DOES generate a STOP condition.

SEQUENTIAL READ

This mode can be initiated with either a current address read or random read. The first word read out of the memory is transmitted in the same way as in both previous modes,however the master must now acknowledge the transfer indicating it requires more data. The ST24C04 will output a string of eight bits for each acknowledge it received. As in the other read modes to terminate the transfer the master MUST not acknowledge the last transfer and DOES generate a STOP condition.

The data output is sequential;data from address n followed by data from address n+1. The internal address counter is automaticaly incremented allowing the entire content of the 512 words page to be serially read in a single read operation.If more than 512 words are read the counter will "roll-over" and the ST24C04 will continue to output data for each acknowledge received.

SDA BUS IN READ MODE

In all read modes the ST24C04 is waiting for an acknowledge (SDA line low) on the 9th clock pulse of a data transfer.If an acknowledge is not detected,the ST24C04 terminates the data transfer and switches to a "receiver" state.

PROTECT MODE

This mode is activated only if pin AO/PRE is set to V_{CC}. In this mode the upper page of the memory (A_0=1) can be protected against spurrious or parasitic writes.

The depth of the protected zone is defined by the user when programming the last byte of the memory (address FF hex in the upper page (A_0=1))

This byte called PROTECT REGISTER defines the address of the first memory location to be protected.

To use properly the ST24C04 in this specific mode, the user must write first into the memory the pattern he wants to protect, then lock the access of this protected zone by writing into the PROTECT REGISTER (address FF Hex) the address of the first location to be protected.

As the Protect Register is included into the protected zone the only way to change the protected zone depth or content is to set pin 1 (AO/PRE) to ground and disable the protect mode.

Protect Register definitions :

The 5 most significant bits : first address to be protected. The first address to be protected is defined every 8 bytes thus a maximum of 256 bytes can be protected with a minimum of 8 bytes.

The 6th bit is the protection mode flag.

- When set to 1 : protection mode is disabled

- When set to 0 : protection mode is enabled

The 2 last bits are don't- care

A	A	A	A	A	F	X	X
<----		Adress		---->	Flag		

Example : Configuration register : 001010XX addresses ranging from 28 hex to FF hex are protected.

Remark :

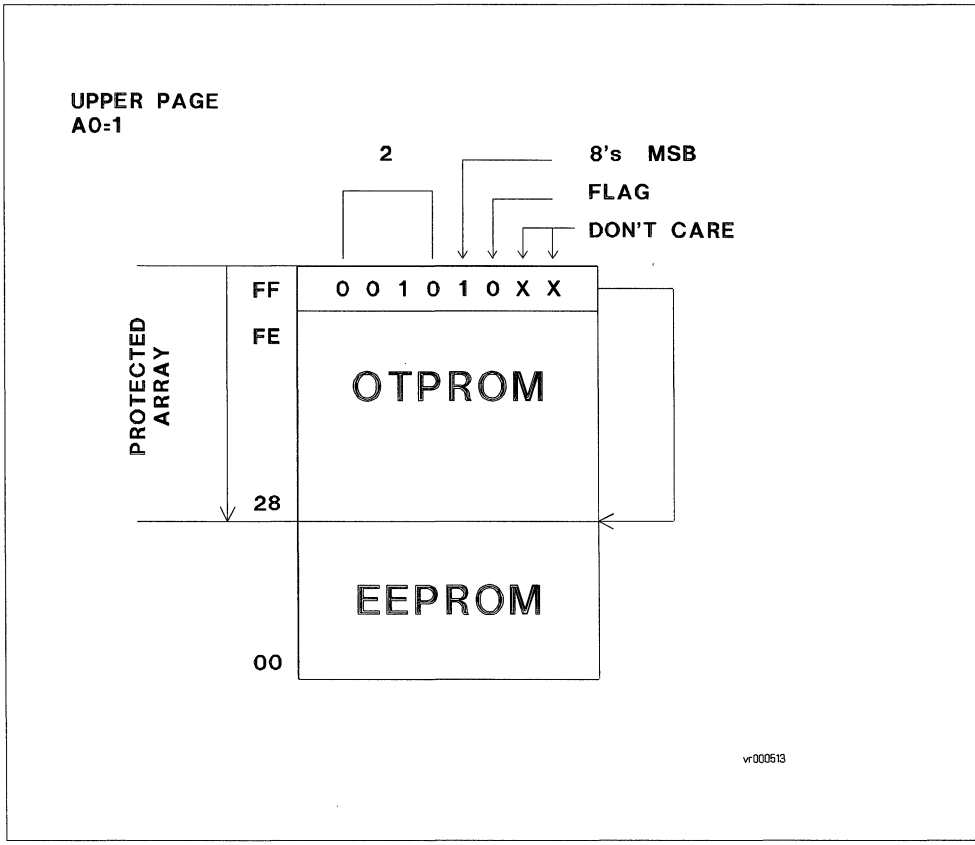
A special attention has to be paid when using this mode with TEST pin set to "1" (multibyte mode).

In this mode the ST24C04 doesn't roll over on the last 3 least significant bits of the address word, therefore is able to enter the protected portion as described previously.

In this case the first protected address is defined by the content of the PROTECT REGISTER plus 3 bytes .

Ex : if Protected Register content is 001010XX
Addresses 2B hex to FF are protected.
Addresses 28, 29, 2A hex are not protected.

FIGURE 3 BIS : MEMORY PROTECTION



TIMMING DIAGRAMS

FIGURE 4 : BYTE WRITE

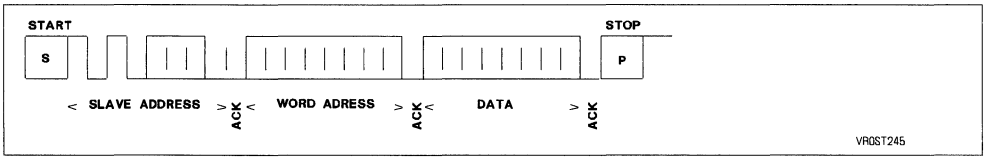


FIGURE 5 : PAGE WRITE

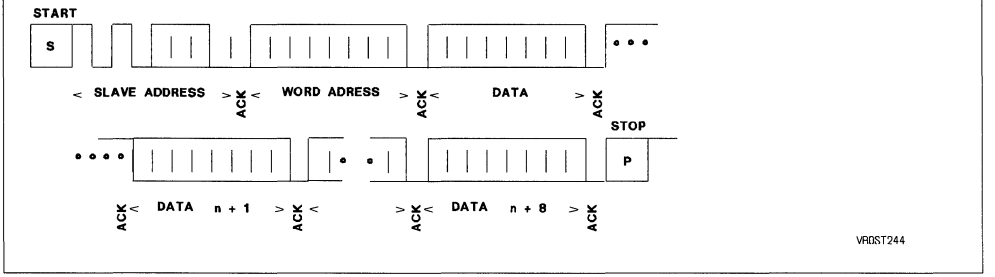


FIGURE 6 : CURRENT ADDRESS READ

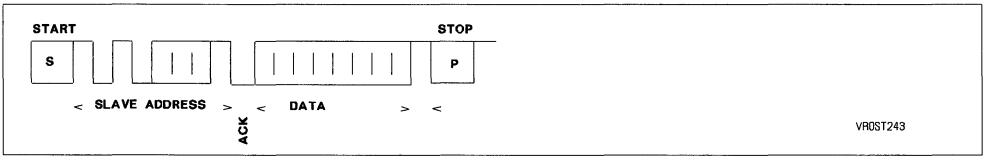


FIGURE 7 : RANDOM ADDRESS READ

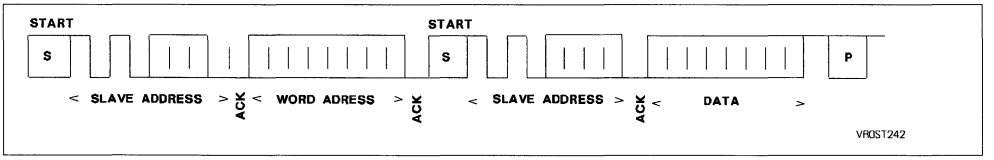
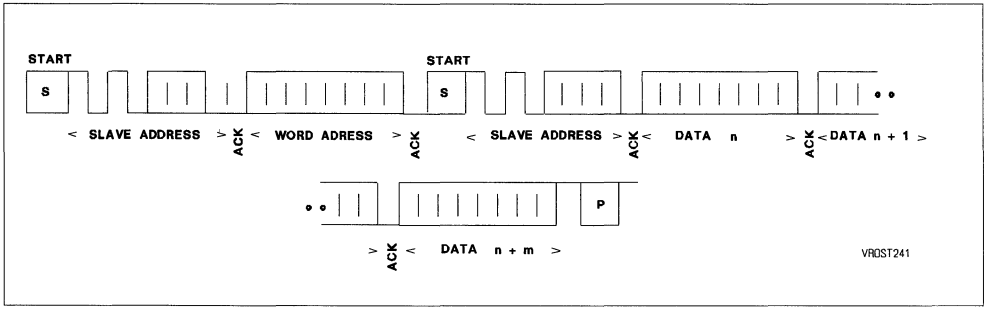


FIGURE 8 : SEQUENTIAL READ

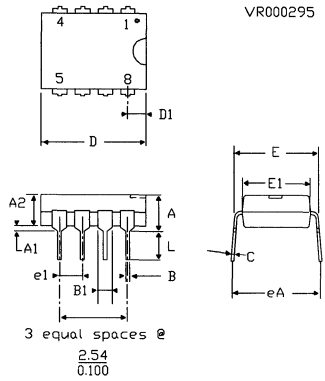


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST24C04B1	Dual-in-line	0°C to 70°C	4.5V to 5.5V
ST24C04ML1	SO 14		
ST24C04B6	Dual-in-line	-40°C to 85°C	
ST24C04ML6	SO 14		
ST24C04B3	Dual-in-line	-40°C to 125°C	
ST24C04ML3	SO 14		

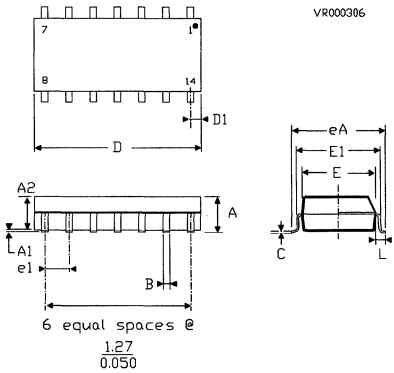
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO14 PACKAGE (ML)

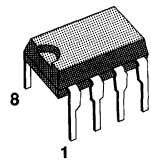


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10		0.20	.004		.008
A2			1.60			0.063
B	0.35		0.46	.014		.018
C	0.19		0.25	.007		.010
D	8.55		8.75	.337		.344
D1			0.68			.027
E	3.80		4.00	.150		.157
E1	4.60		5.30	.181		.209
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.50		1.27	.020		.050

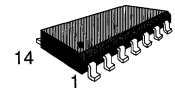
4K BIT (512 X 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

- 2 PAGES OF 256 X 8 BITS
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- 2.5 TO 5.5 VOLTS POWER SUPPLY (READ AND WRITE)
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 4 BYTES)
- PART OF MEMORY PROTECTION CAPABILITY
- PAGE WRITE CAPABILITY
- SELF-TIMED PROGRAMMING CYCLE
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ
- LOW POWER CMOS
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY
- OVER 1 MILLION ERASE/WRITE CYCLES
- OVER 10 YEARS DATA RETENTION
- FUNCTIONAL COMPATIBILTY WITH ST24C04



PDIP8



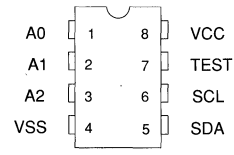
PSO14

(Ordering information at the end of the datasheet)

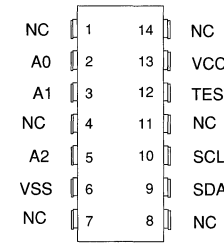
PIN NAMES

A0-A1-A2	Address Inputs
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

PIN CONNECTION



VR00B224



VR000233

DESCRIPTION

The ST25C04 is a 4096 bits read/write non volatile memory organized in 512 words of 8 bits and is manufactured in SGS-THOMSON highly reliable CMOS EEPROM technology. The ST25C04 works with a power supply voltage as low as 2.5V

It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

The 4K bits memory capacity is divided in two pages of 256 words of 8 bits. All memory operations are synchronized on an external strobe: SCL bus. The Read and Write operations are initiated by a Start instruction sent on the SDA bus by the master device.

The Start instruction includes a Start condition followed by an 8 bit word : the seven first bits address the right EEPROM slave device and the last bit defines the kind of operation to follow : Read or Write. A Start instruction is ended by an acknowledge of the slave device. The specific address of a given ST25C04 is hardwired through the 2 address pins A1 and A2.

The ST25C04 features 3 kind of operations:

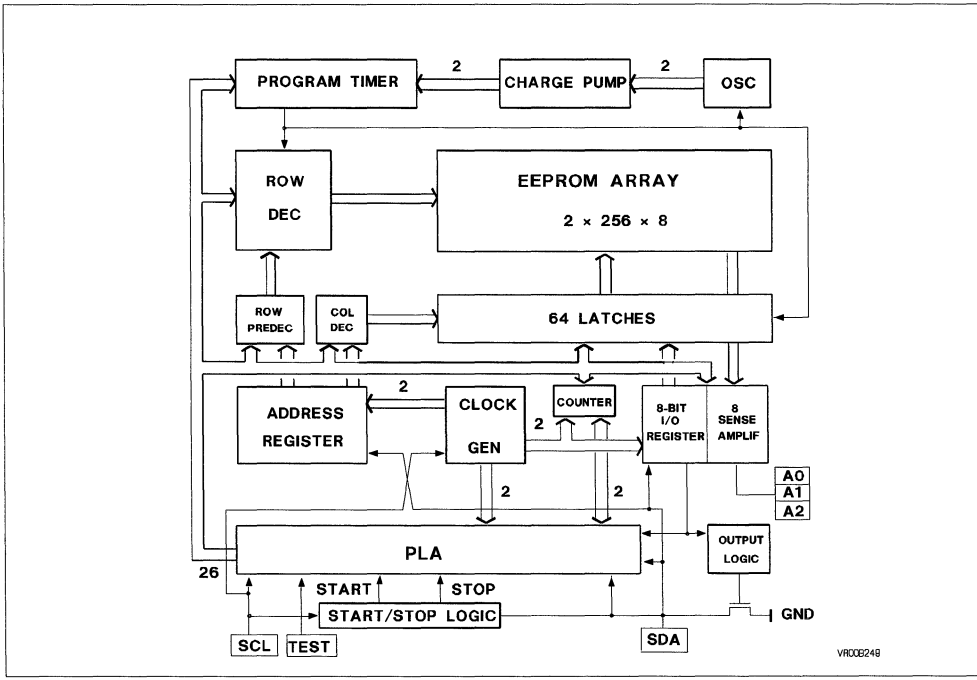
- Byte Write: 8 bits are written at the address previously defined in the byte write operation mode.
- Multibyte programming which allows to write consecutively up to 4 words in any location of the memory array in a single programming cycle.
- Page Write mode which allows to write from 2 to 8 bytes in a single programming cycle.

In Read Mode 3 read operations are available for the user:

- The Current Address read performs a read operation at the previously pointed address incremented by one.
- The Random Read performs a read operation at the address defined in the randon read instruction
- The Sequential Read performs either a Current Address read or a Random Read, but reads consecutive words provided the master device acknowledges each string of 8 bits read from the memory without generating a STOP condition.

The design of the ST25C04 and its processing with a highly reliable technology yields to typical endurance better than 1 million cycles and Data Retention greater than 10 years.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	- 65 to 150	°C
Input or Output Voltage with respect to ground	- 0.3 to 6.5	V
Lead Temperature (soldering, 10 seconds)	+ 300	°C
ESD Rating	2000	V

OPERATING CONDITIONS

Ambient Operating Temperature		
ST25C04-1	0 to 70	°C
ST25C04-6	- 40 to +85	°C
ST25C04-3	- 40 to +125	°C
POWER SUPPLY	2.5 to 5.5	V

D.C. OPERATING CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range VCC=2.5V Min, 5.5V Max

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC}	Power Supply Current			2	mA	f_{SCL} = 100kHZ
I_{SB}	Standby Current		100		µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND or V_{CC}
I_{LO}	Ouput Leakage Current			10	µA	V_{OUT} = GND or V_{CC}
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 .7xV_{cc}		.3xV_{cc} V_{cc}+1.0	V V	
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 V_{cc} - 0.5		+ 0.5 V_{cc} + 1.0	V V	A0, A1, A2 inputs A0, A1, A2 inputs
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA

A.C. CHARACTERISTICS t_a=-40°C to 125°C according to selected temperature range
V_{CC}=2.5V Min, 5.5V Max

SYMBOL		MIN.	TYP.	MAX.	UNITS
f_{SCL}	SCL Clock Frequency	0		100	kHZ
T_I	Noise Suppression Time Constant on SCL, SDA Inputs			100	ns
t_{AA}	SCL Low to SDA Data Valid	300			ns
t_{BUF}	Time the bus must be be free before a new transmission.	4.7			µs
$t_{HD:STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	Clock Low Period	4.7			µs
t_{HIGH}	Clock High Period	4.0			µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated START condition)	4.7			µs
$t_{HD:DAT}$	DATA IN Hold Time	0			ns
$t_{SU:DAT}$	DATA IN Setup Time	250			ns
t_R	SDA & SCL Rise Time			1	µs
t_F	SDA & SCL Fall Time			300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4.7			µs
t_{DH}	DATA OUT Hold Time	300			ns
t_{WR}	Programming Time (note 1)			10	ms
Endurance	W/E Cycles	1 million Cycles minimum			

Note 1: in multibyte programming mode and only in this mode,if the accessed words are located in two consecutive rows the maximun programming time will be extended to two times tWR.

FIGURE 1 : BUS TIMING

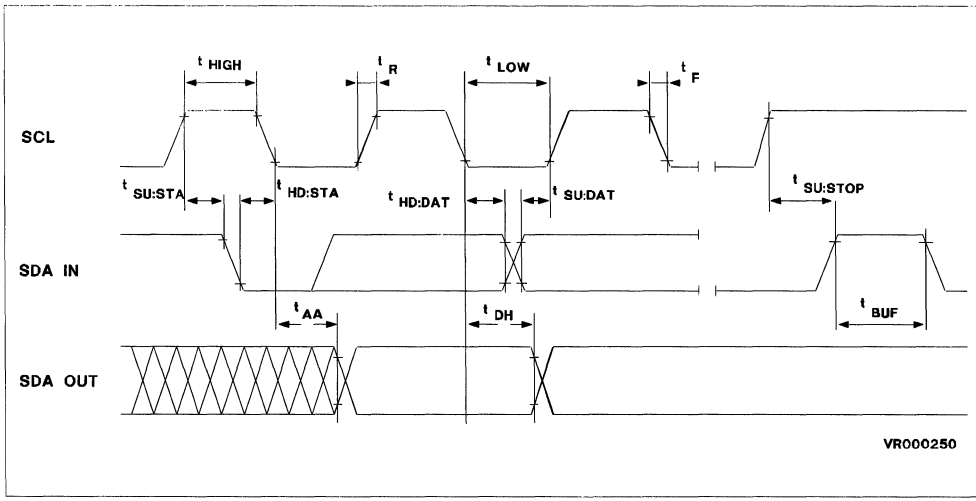
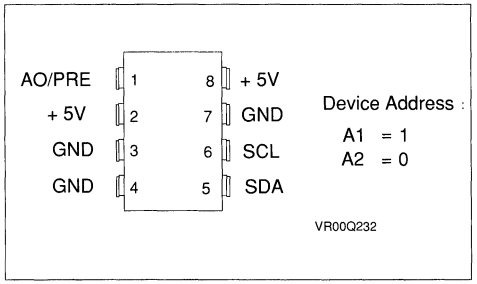


FIGURE 2 : TYPICAL INTERFACE



PIN DESCRIPTION

SERIAL CLOCK (SCL)
The SCL input is used to clock all data into or out of the device.

SERIAL DATA (SDA)
SDA is a bidirectional pin used to transfer data into or out of the device.It is an open drain output that may be wired with any open drain or open collector outputs to formed the system SDA bus.

ADDRESS (A0/PRE)
For proper device operation this pin must be tied to V_{SS} or V_{CC}

- When set to VSS all the memory array can be accessed in read or write mode.
- When set to VCC this pin is considered as a protection key, therefore allowing the upper portion of the memory to be protected in write mode. (See "PROTECT MODE" section in the following pages of the Data sheet).

ADDRESS (A1,A2)
These two addresses inputs are used to set the fifth and sixth bits of the seven bits slave address.These inputs can be used static or driven. When used statically they must be tied to V_{CC} or V_{SS}. When used driven CMOS levels have to applied to the device.

TEST PIN (TEST)
For proper device operation this input must be tied to V_{SS} or V_{CC} According to the voltage on TEST pin up to four or eight bytes may be written in the ST25C04 in a single write operation (see "Write Operation" section.)

DEVICE OPERATION

The ST25C04 supports the I^2C (bidirectional bus oriented) protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. Therefore, the ST25C04 will be considered as a slave receiver or transmitter in all applications.

DATA TRANSITION
Data transition on the SDA line must only occur when the clock SCL is Low. SDA transitions while SCL is HIGH will be interpreted as START or STOP conditions. See Fig 1.

START CONDITION
A START condition is defined by a HIGH to LOW transition of THE SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The ST25C04 continuously monitors the SDA and SCL lines for a START and will not respond to any command if this condition has not been met.

STOP CONDITION
A STOP condition is defined by a LOW to HIGH transition of the SDA line while the SCL is at a stable HIGH level. This condition terminates communication between devices and forces the ST25C04 in the standby power mode.

ACKNOWLEDGE
Acknowledge is used to indicate successfull data transfer. The transmitter (master or slave) will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line LOW to indicate it received the 8 bits of data.

DATA TRANSFER
During Data Transfer the ST25C04 samples the SDA line on the leading edge of SCL clock.Therefore,for proper device operation SDA line must be stable during the SCL LOW to HIGH transition.

Note In the I^2C protocol ,the SDA bus must be connected to the positive power supply through a pull-up resistor.

DEVICE ADDRESSING

To start communication between two devices, the bus master must initiate a start instruction sequence; following a START condition the master sends onto the SDA bus an eight bit word correspondind to the address of the device it is addressing.

- The most significant 4 bits of the slave address , therefore the first bits sent onto the bus are the device type identifier. The ST25C04 memory device type is fixed as "1010".
- The next 2 significant bits are used to address a particular device of the previously defined type connected to the bus. The state of the hardwired A1 and A2 pins defines the device address. Up to four ST25C04 can be connected on the same bus.
- The next bit of the slave address field is the most significant bit of the word address ; it is used as the page select bit.
- The last bit of the start instruction defines the type of operation to be performed:

- When set to "1" a read operation is selected
- When set to "0" a write operation is selected

Chip selection is accomplished by setting the two bits of the chip address field to the corresponding levels of A1 and A2 inputs. After a START condition is detected all ST25C04 connected to the bus will compare the slave address being transmitted with their own hardwired address (A1 and A2). After comparison , the selected ST25C04 will acknowledge on the SDA line and will perform the read or write operation according to the state of the R/W bit.

WRITE OPERATION

The standard operation mode is byte write or multibyte programming. If pin 7 is forced to V_{SS} the ST25C04 switches to page mode.

BYTE WRITE
In this mode, following a START condition the master sends a slave address word with the R/W bit set to "0". The ST25C04 will acknowledge this first transmission and waits for a second word : the word address field.This 8 bit address field provides access to any of the 256 words of the selected page. Upon receipt of the word address the ST25C04 slave device will respond with an acknowledge. At this time, all following words transmitted to the ST25C04 will be considered as Data. In Byte Write mode the master sends one word which is acknowledged by the ST25C04. Then the master terminates the transfer by generating a STOP condition. This STOP condition initiates the internal self-timed programming cycle.

While the internal programming cycle is in progress the ST25C04 will not respond to any request from the bus master.

FIGURE 3 : SLAVE ADDRESS ALLOCATION

	Device type				Device Address		Page	
START	1	0	1	0	A2	A1	A0	R/W
	Slave Address							

MULTIBYTE PROGRAMMING
The ST25C04 is able to write consecutively up to 4 bytes in the multibyte programming mode. As in the Byte Write programming mode,the multibyte programming can be started at any specified address and whithout any restriction of any kind. This multibyte mode is started and performed in the same way as the Byte Write mode; but instead of terminating the write sequence after the first data word is transfered,the master does not generate a STOP condition and up to 3 additional words can be transmitted to the ST25C04. After receipt of each word,the ST25C04 will respond with an acknowledge. After the bytes to be written (4 bytes maximun) have been transfered, the master generates a STOP condition which starts the internal self-timed programming cycle.

PAGE WRITE (only available if pin 7 is grounded)
The ST25C04 is able to write up to 8 bytes in a Page Write operation. This mode allows to write 2 to 8 bytes in a single write cycle provided they are all topologically located in the same physical row.(five most significant address bits identical.)

This mode is started and performed in the same way as the byte write operation, but instead of terminating the write sequence after the first data word is transfered, the master doesn't generate a STOP condition and can transmit up to seven additional words. After receipt of each word the ST25C04 will respond with an acknowledge.

After receipt of each data word the internal address counter is automatically incremented by one. Only the three low order address bits are incremented, the high order five bits remain constant.

Therefore, a special attention has to be paid when using this feature in order to avoid any scrambling or over writing. If more than 8 words are transmitted the address counter will "rollover" and the previously written data will be overwritten. As in byte write operation the master terminates the transfer by generating a stop condition that triggers the internal programming cycle.

All inputs are disabled until completion of the internal write cycle.

READ OPERATIONS

Read operations are initiated in the same manner as the write operation with the exception that the R/W bit following the slave address in the start instruction is set to a logical "1". Three read operation modes are available:

- current address read
- random read
- sequential read

CURRENT ADDRESS READ

The ST25C04 has an internal address counter that points the address of the last word accessed incremented by one. Therefore if the last access (either read or write) was to address n, the next current read operation will access data from address n+1. To initiate this read mode the master generates a start instruction (START condition followed by the eight bit slave address word) with the R/W bit set to one. The ST25C04 will respond with an acknowledge and transmit the 8 bits of data. To terminate the transfer the master MUST not acknowledge the transfer and DOES generate a STOP condition.

RANDOM READ

The random read mode allows the master to access any memory location. In order to load into the device the word address the master must first performed a "dummy" write sequence.(START, slave address ,R/W bit set to "0",followed by the word address to be read). After the word address has been acknowledged,the master immediately reissues a START instruction whith the R/W bit set to "1". The ST25C04 will acknowledge the transfer and output the 8 bits of the addressed word. As in current address read to terminate the transfer the master MUST not acknowledge the transfer and DOES generate a STOP condition.

SEQUENTIAL READ

This mode can be initiated with either a current address read or random read. The first word read out of the memory is transmitted in the same way as in both previous modes,however the master must now acknowledge the transfer indicating it requires more data. The ST25C04 will output a string of eight bits for each acknowledge it received. As in the other read modes to terminate the transfer the master MUST not acknowledge the last transfer and DOES generate a STOP condition.

The data output is sequential;data from address n followed by data from address n+1. The internal address counter is automaticaly incremented allowing the entire content of the 512 words page to be serially read in a single read operation.If more than 512 words are read the counter will "roll-over" and the ST25C04 will continue to output data for each acknowledge received.

SDA BUS IN READ MODE

In all read modes the ST25C04 is waiting for an acknowledge (SDA line low) on the 9th clock pulse of a data transfer.If an acknowledge is not detected,the ST25C04 terminates the data transfer and switches to a "receiver" state.

PROTECT MODE

This mode is activated only if pin AO/PRE is set to V_{CC}. In this mode the upper page of the memory (A_0=1) can be protected against spurrious or parasitic writes.

The depth of the protected zone is defined by the user when programming the last byte of the memory (address FF hex in the upper page (A_0=1))

This byte called PROTECT REGISTER defines the address of the first memory location to be protected.

To use properly the ST25C04 in this specific mode, the user must write first into the memory the pattern he wants to protect, then lock the access of this protected zone by writing into the PROTECT REGISTER (address FF Hex) the address of the first location to be protected.

As the Protect Register is included into the protected zone the only way to change the protected zone depth or content is to set pin 1 (AO/PRE) to ground and disable the protect mode.

Protect Register definitions :

The 5 most significant bits : first address to be protected. The first address to be protected is defined every 8 bytes thus a maximum of 256 bytes can be protected with a minimum of 8 bytes.

The 6th bit is the protection mode flag.

- When set to 1 : protection mode is disabled

- When set to 0 : protection mode is enabled

The 2 last bits are don't- care

A	A	A	A	A	F	X	X
<----		Adress		---->	Flag		

Example : Configuration register : 001010XX addresses ranging from 28 hex to FF hex are protected.

Remark :

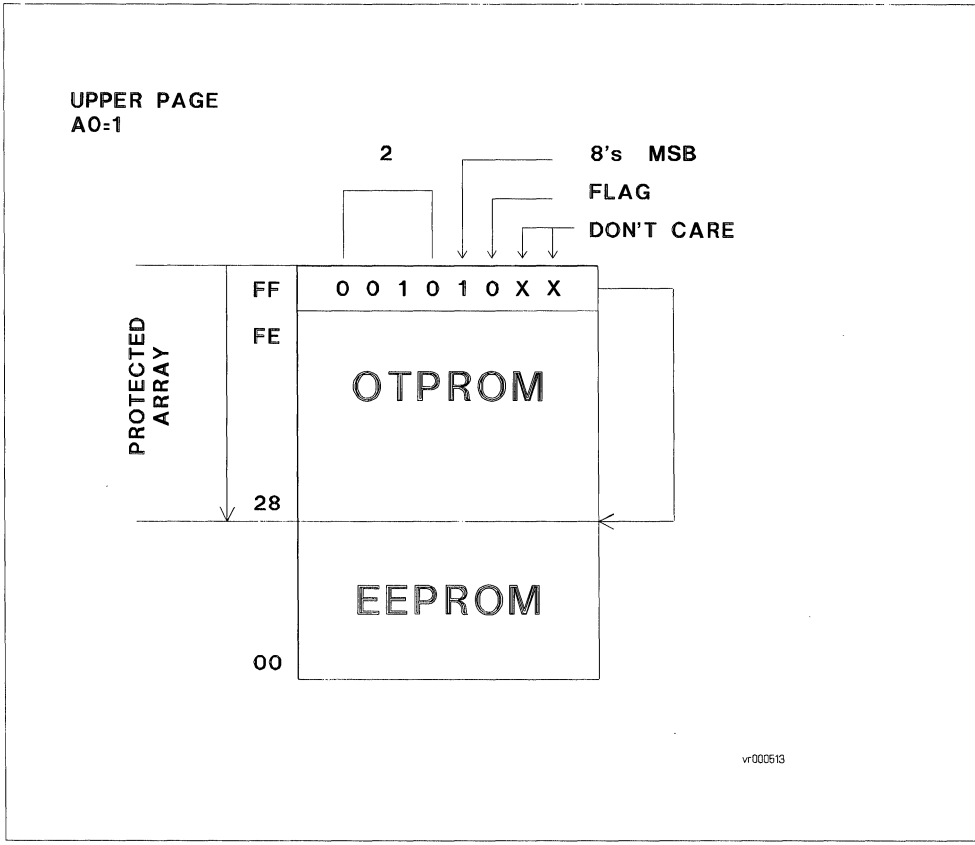
A special attention has to be paid when using this mode with TEST pin set to "1" (multibyte mode).

In this mode the ST24C04 doesn't roll over on the last 3 least significant bits of the address word, therefore is able to enter the protected portion as described previously.

In this case the first protected address is defined by the content of the PROTECT REGISTER plus 3 bytes .

Ex : if Protected Register content is 001010XX
Addresses 2B hex to FF are protected.
Addresses 28, 29, 2A hex are not protected.

FIGURE 3 BIS : MEMORY PROTECTION



TIMMING DIAGRAMS

FIGURE 4 : BYTE WRITE

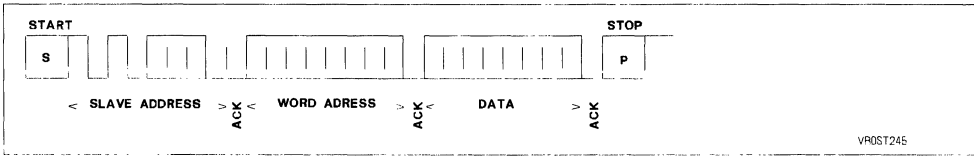


FIGURE 5 : PAGE WRITE

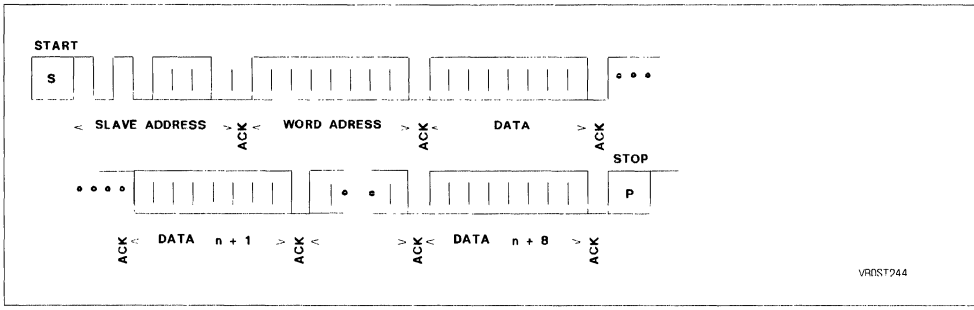


FIGURE 6 : CURRENT ADDRESS READ

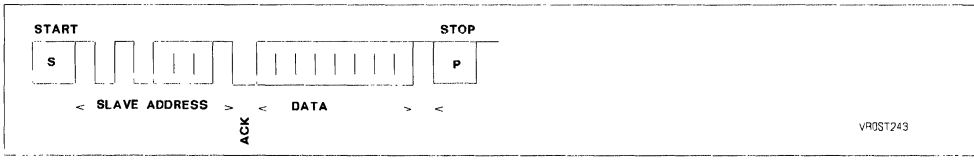


FIGURE 7 : RANDOM ADDRESS READ

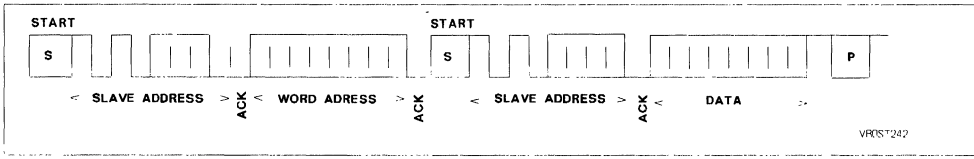
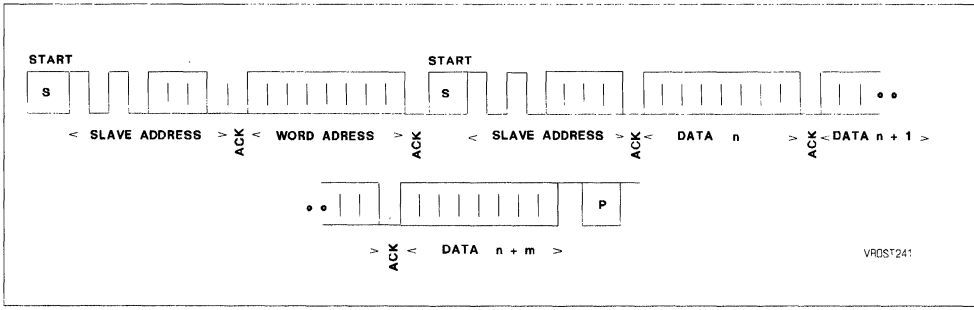


FIGURE 8 : SEQUENTIAL READ

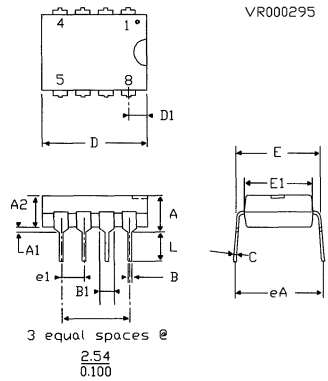


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST25C04B1	Dual-in-line	0°C to 70°C	2.5V to 5.5V
ST25C04ML1	SO 14		
ST25C04B6	Dual-in-line	-40°C to 85°C	
ST25C04ML6	SO 14		
ST25C04B3	Dual-in-line	-40°C to 125°C	
ST25C04ML3	SO 14		

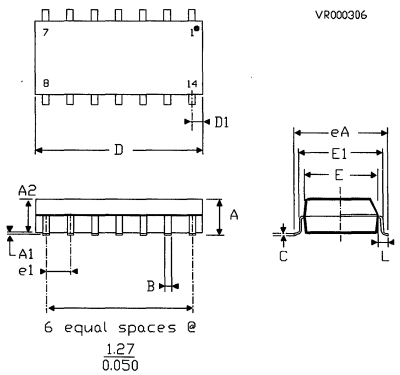
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO14 PACKAGE (ML)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10		0.20	.004		.008
A2			1.60			0.063
B	0.35		0.46	.014		.018
C	0.19		0.25	.007		.010
D	8.55		8.75	.337		.344
D1			0.68			.027
E	3.80		4.00	.150		.157
E1	4.60		5.30	.181		.209
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.50		1.27	.020		.050

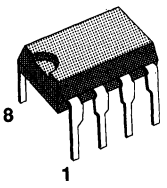
SGS-THOMSON MICROELECTRONICS

ST24C08

8 K BIT (1024 x 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRODUCT PREVIEW

- 4 PAGES OF 256 X 8 BITS.
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- SINGLE POWER SUPPLY (READ AND WRITE).
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 8 BYTES).
- PART OF MEMORY PROTECTION CAPABILITY.
- PAGE WRITE CAPABILITY (UP TO 16 BYTES).
- SELF-TIMED PROGRAMMING CYCLE.
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ.
- LOW POWER CMOS.
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- OVER 1 MILLION ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.



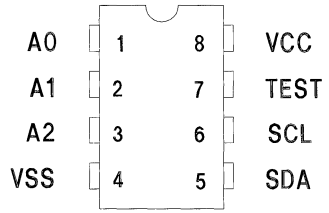
PDIP8

(Ordering information at the end of the datasheet)

DESCRIPTION

The ST24C08 is a 8192 bit read/write non volatile memory organized in 1024 words of 8 bits and is manufactured in SGS THOMSON highly reliable CMOS EEPROM technology. It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

PIN CONNECTION



VR00B224

PIN FUNCTIONS

A0-A1-A2	Address Inputs
V_{SS}	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

EEPROM DEVICES

MICROWIRE PRODUCT LINE

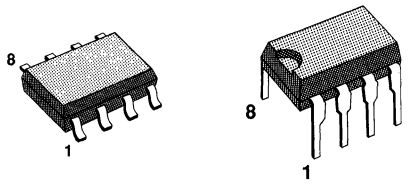
SGS-THOMSON MICROELECTRONICS

ST93C06

256 BITS (16x16 or 32x8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

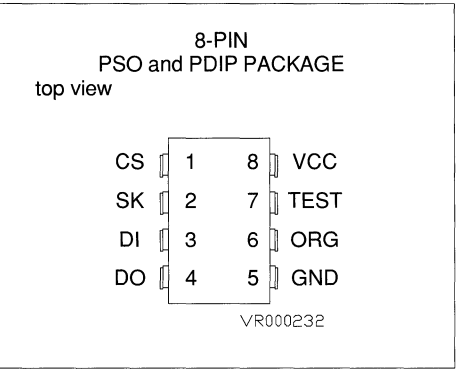
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- OVER 1 MILLION ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- 16 X 16 OR 32 X 8 MEMORY FORMAT USER SELECTABLE.
- WORD AND CHIP PROGRAMMING MODE.
- SELF TIMED PROGRAMMING CYCLE WITH AUTO ERASE.
- READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SINGLE POWER SUPPLY IN ALL MODES (5V ± 10%).
- SEQUENTIAL REGISTER READ.



PSO8 **PDIP8**

(Ordering information at the end of the datasheet)

PIN CONNECTION



DESCRIPTION

The ST93C06 is a 256 bits non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology. It is an external memory accessed via a simple serial interface.

The 256 bits memory capacity is divided in either 16 registers of 16 bits each or 32 registers of 8 bits each. The default memory organization is 16 by 16 but it can be switched to 32 by 8 thanks to the "ORG" pin.

The read instruction loads the address of the first register to be read into an 8 bits address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address, it is possible, if the "CS" is held high, to produce a serial data stream. In that case, the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 256 bits. Thus the ST93C06 can be viewed as a non volatile shift register.

In programming mode, the ST93C06 does not require an erase cycle prior to the write instructions. All programming cycles are completely self timed for simplified operations. The standard "write" cycle allows to write 16 bits (resp 8 bits) at a time into one of the 16 (resp 32) data registers.

Following the initiation of a programming cycle, the Ready/Busy status of the chip is available on the "D_O" pin if "CS" is brought high.

PIN FUNCTIONS

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
D_I	SERIAL DATA INPUT
D_O	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
ORG	ORGANIZATION SELECTION INPUT
GND	GROUND
TEST	THIS PIN IS FOR SGS-THOMSON INTERNAL USE ONLY

A special internal feature of the ST93C06, "Power on data protection", allows to inhibit all operating modes if V_{CC} is too low. This feature is particularly useful when powering up the chip. The design of the ST93C06 and its processing with a highly reliable technology yields to typical endurance over 1 million cycles and data retention greater than 10 years.

MEMORY ORGANIZATION

The ST93C06 is organized, by default, in 16 x 16. Thanks to the ORG pin this organization can be changed. If the ORG pin is connected to V_{CC} or left unconnected the ST93C06 will stay in the 16 by 16 organization. If the ORG pin is connected to ground, the 32 by 8 organization is selected.

POWER ON DATA PROTECTION

During power up, all modes of operations are inhibited until V_{CC} has reached a level between 2.5 and 3.5V. Reciprocally all modes were inhibited if V_{CC} falls below the voltage range 2.0 to 3.0V.

OPERATING MODES

The ST93C06 has 7 instructions as described in table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 2 bits carry the OP code and the following 6 bits (respectively 7 bits in 32 by 8 organization) the address for register selections.

READ

The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16 bits (resp. 8 bits) out shift register. A dummy bit (logical 0) precedes the 16 (resp. 8 bits) data output string. Output data changes are initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits (resp. 8 bits) are clocked out as long as CS is held high.

Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode, the dummy bit is suppressed and a continuous string of data is obtained.

ERASE / WRITE ENABLE (EWEN)

All programming modes must be preceded by an Erase/Write Enable instruction. Once an Erase/Write enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part (Note that after a powering up, the part is in the Erase/Write Disable state).

ERASE / WRITE DISABLE (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disable all programming modes and should follow all programming operations. Execution of a Read instruction is independent of both the EWEN and EWDS instructions.

ERASE (ERASE)

The Erase instruction is a programming instruction which sets all bits of the specified register to the logical "1" state. After the last address bit has been loaded, CS is brought low and this falling edge initiates the self timed programming cycle. The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs" (see section on Ready/Busy status).

WRITE (WRITE)

The Write instruction is followed by 16 (respectively 8) bits of data to be written into the specified address. After the last bit of data is clocked in on the data-in (D_I) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle.

The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs" (see section on Ready/Busy status).

ERASE ALL (ERAL)

This instruction is provided to erase the whole chip. With this instruction, each bit of all registers in the memory array is set to the logical "1" state. This programming cycle works in the same way as the ERASE cycle.

WRITE ALL (WRAL)

This instruction is provided to program simultaneously all registers with the data pattern specified in the instruction. All the registers must be erased before doing a WRAL operation ; then, the WRITE ALL programming instruction works in the same way as the WRITE instruction.

READY / BUSY STATUS

During every programming cycle (Erase, Write, Erase all, Write all), the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs". D_O = logical "0" indicates that the programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction (or all the memory array for ERAL and WRAL instructions) have been programmed, and the part is ready for another instruction. If the part is "ready", the logical "1" on the D_O pin will disappear as soon as the start bit of a new instruction is loaded on the D_I pin.

COMMON I/O SIGNAL

D_I and D_O pins can be connected together. However some precautions should be taken ; therefore it is advised to refer to the SGS-THOMSON application note : "Serial EEPROM Memories : A design guide for common I/O Application".

NOTE ABOUT PIN "TEST"

This pin does not affect the device functionality and it is reserved for SGS-THOMSON internal use. For the user, this pin can be either left unconnected or connected to any voltage between V_{SS} and V_{CC} (V_{SS} and V_{CC} included).

TABLE 1 : INSTRUCTION SET FOR ST93C06, ORGANIZATION : 16 x 16

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	COMMENTS
READ	1	10XX	A_3-A_0		Reads data stored in memory, starting at specified address.
EWEN	1	0011	XXXX		Erase/Write enable must precede all programming modes.
EWDS	1	0000	XXXX		Disables all programming instructions.
ERASE	1	11XX	A_3-A_0		Erase register defined by the specified address.
WRITE	1	01XX	A_3-A_0	D_{15}-D_0	Writes registers.
ERAL	1	0010	XXXX		Erase all registers.
WRAL	1	0001	XXXX	D_{15}-D_0	Write all registers.

TABLE 2 : INSTRUCTION SET FOR ST93C06 ORGANIZATION : 128 x 8 ("ORG" PIN CONNECTED TO GND)

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	COMMENTS
READ	1	10XX	A_3-A_0		Reads data stored in memory, starting at specified address.
EWEN	1	0011	XXXXX		Erase/Write enable must precede all programming modes.
EWDS	1	0000	XXXXX		Disables all programming instructions.
ERASE	1	11XX	A_3-A_0		Erase register defined by the specified address.
WRITE	1	01XX	A_3-A_0	D_7-D_0	Writes registers.
ERAL	1	0010	XXXXX		Erase all registers.
WRAL	1	0001	XXXXX	D_7-D_0	Write all registers.

Figure 1 : ST93C06 Block diagram

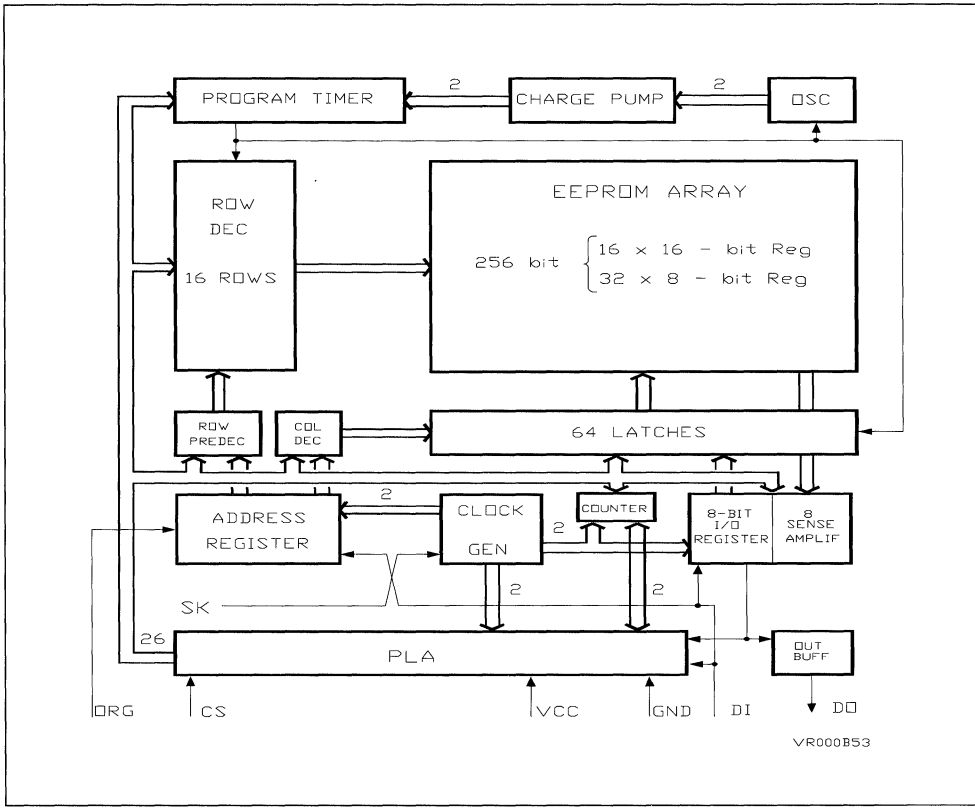


Figure 2 : Synchronous Timing

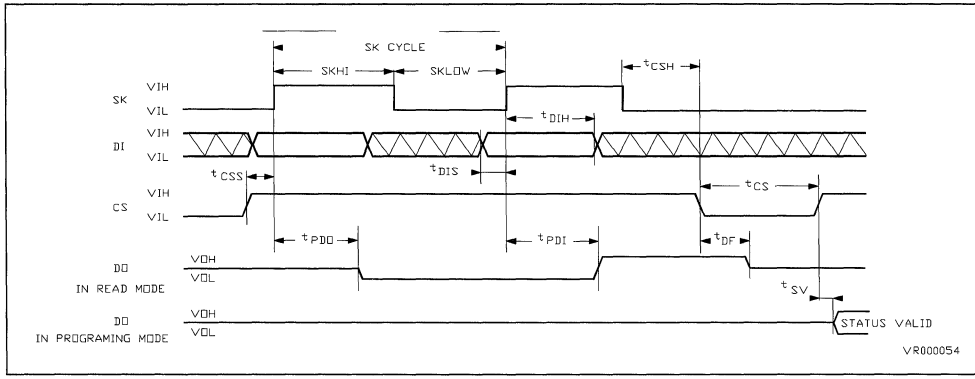


Figure 3 : READ

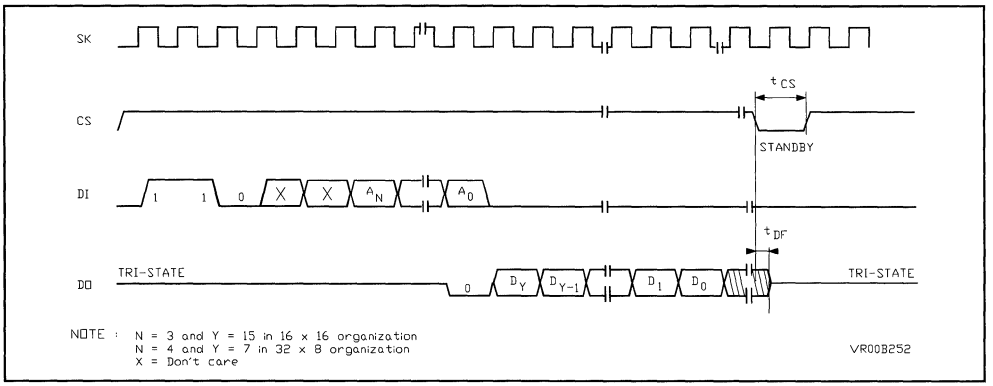


Figure 4 : WRITE

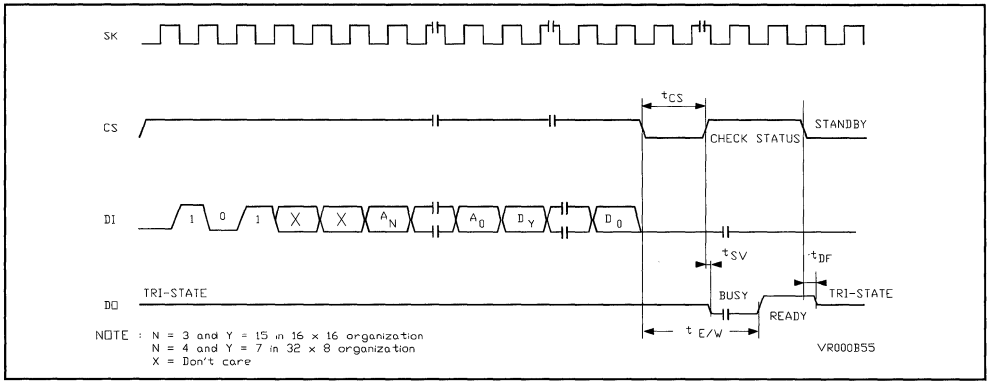


Figure 5 : EWEN/EWDS

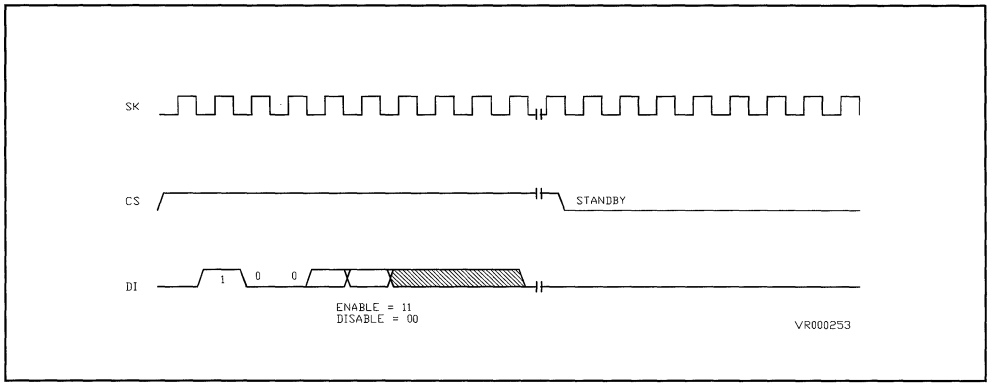


Figure 6 : ERASE

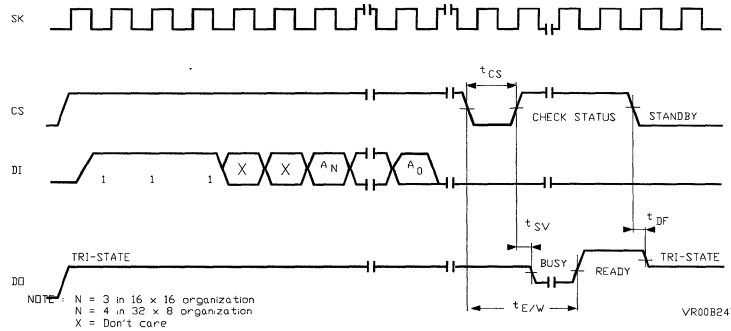


Figure 7 : ERAL

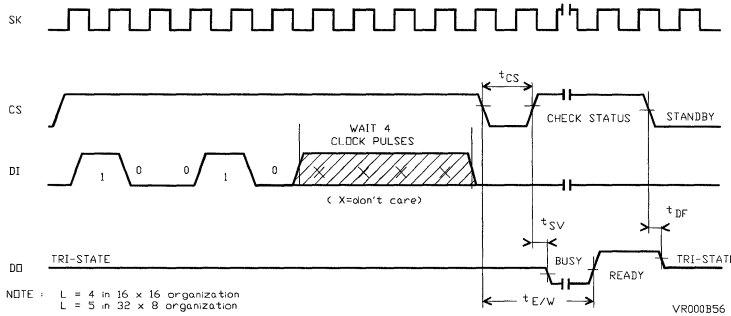
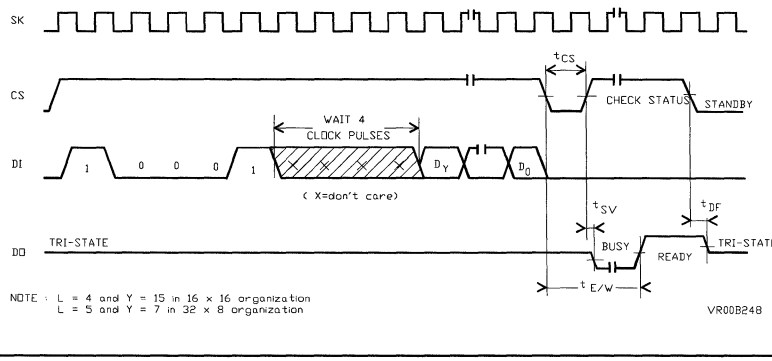


Figure 8 : WRAL



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Ambient storage temperature	:	-65 to 150°C
All input or output voltage with respect to ground	:	-0.3V to + 6.5V
Lead Temp (soldering, 10 sec.)	:	+300°C Max
ESD Rating	:	2000V Max

DC & AC Electrical characteristics V_{CC} = 5V ± 10% (unless otherwise specified).

OPERATING CONDITIONS

Ambient operating temperature

ST93C06 *1	:	0°C to 70°C
ST93C06 *6	:	-40°C to 85°C
ST93C06 *3	:	-40°C to 125°C

Positive power supply	:	4.5V to 5.5V

* = B = Dual in line package

* = M = PSO8 package

CAPACITANCE

(note 6) (T_A = 25°C, f = 1 Mhz)

SYMBOL	TEST	TYP	Max	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load 1TTL gate and CL = 100 pF

Input Pulse Levels	:	0.4V to 2.4V

Timing measurement Reference levels

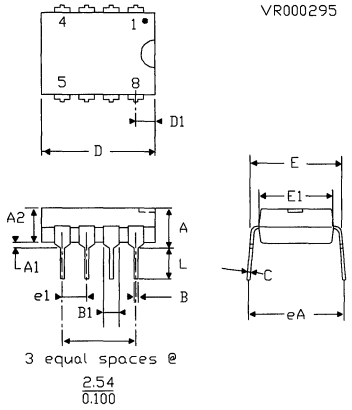
Output	:	0.8V and 2V
Input	:	1V and 2V

NOTES
1. Stress above those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extented periods may affect device reliability.
2. The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in SK clock cycle TSKH + TSKL must be greater or equal to 1 microsecond. For example if TSKL = 250 ns then the minimum TSKH = 750 ns in order to meet the SK frequency specification.
3. The SK frequency specification for extended temperature specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle TSKH + TSKL must be greater or equal to 2 microseconds. For example TSKL = 500 ns then the minimumTSK = 1.5 microsecond in order to meet the SK frequency specification.
4. For commercial parts : CS must be brought low for a minimum of 250 ns (TCS) between consecutive instruction cycles.
5. For extented temperature : CS must be brought for a minimum of 500 ns (TCS) between consecutive instruction cycles.
6. This parameter is periodically sampled and not 100 % tested.

SYMBOL	PARAMETER	PART NUMBER	CONDITION	MIN	MAX	UNIT
I_{CC1}	OPERATING CURRENT	ST93C06*1	CS=V_{IH},SK=1MHZ		2	mA
	CMOS INPUT LEVELS	ST93C06*6	SK=0.5MHZ		2	mA
		ST93C06*3	SK=0.5MHZ		2	mA
I_{CC2}	OPERATING CURRENT	ST93C06*1	CS=V_{IH},SK=1MHZ		3	mA
	TTL INPUT LEVELS	ST93C06*6	SK=0.5MHZ		3	mA
		ST93C06*3	SK=0.5MHZ		4	mA
I_{CC3}	STANDBY CURRENT	ST93C06*1	CS=0V		50	uA
		ST93C06*6			100	uA
		ST93C06*3			100	uA
I_{IL}	INPUT LEAKAGE	ST93C06*1	V_{IN}=0V TO V_{CC}	-2.5	2.5	uA
		ST93C06*6		-10	10	uA
		ST93C06*3		-10	10	uA
I_{OL}	OUTPUT LEAKAGE	ST93C06*1	V_{OUT}=0V TO V_{CC}	-2.5	2.5	uA
		ST93C06*6		-10	10	uA
		ST93C06*3		-10	10	uA
V_{IL}	INPUT LOW VOLTAGE			-0.1	0.8	V
V_{IH}	INPUT HIGH VOLTAGE			2	V_{CC}+1	V
V_{OL1}	OUTPUT LOW VOLTAGE		I_{OL} =2.1 mA		0.4	V
V_{OH1}	OUTPUT HIGH VOLTAGE		I_{OH} = - 400 uA	2.4		V
V_{OL2}	OUTPUT LOW VOLTAGE		I_{OL} =10 uA		0.2	V
V_{OH2}	OUTPUT HIGH VOLTAGE		I_{OH} = - 10 uA	V_{CC}-0.2		V
f_{SK}	SK CLOCK FREQUENCY	ST93C06*1		0	1	
		ST93C06*6		0	0.5	MHZ
		ST93C06*3		0	0.5	
t_{SKH}	SK HIGH TIME	ST93C06*1	(Note 2)	250		
		ST93C06*6	(Note 3)	500		ns
		ST93C06*3	(Note 3)	500		
t_{SKL}	SK LOW TIME	ST93C06*1	(Note 2)	250		
		ST93C06*6	(Note 3)	500		ns
		ST93C06*3	(Note 3)	500		
t_{CS}	MINIMUM CS	ST93C06*1	(Note 4)	250		
	LOW TIME	ST93C06*6	(Note 5)	500		ns
		ST93C06*3	(Note 5)	500		
t_{CSS}	CS SETUP TIME	ST93C06*1	Relative to SK	50		
		ST93C06*6		100		ns
		ST93C06*3		100		
t_{CSH}	CS HOLD TIME		Relative to SK	0		ns
t_{DIS}	DI SETUP TIME	ST93C06*1	Relative to SK	100		
		ST93C06*6		200		ns
		ST93C06*3		200		
t_{DIH}	DI HOLD TIME	ST93C06*1	Relative to SK	100		
		ST93C06*6		200		ns
		ST93C06*3		200		
t_{PD1}	Output Delay to "1"	ST93C06*1	AC Test		500	
		ST93C06*6			1000	ns
		ST93C06*3			1000	
t_{PD0}	Output Delay to "0"	ST93C06*1	AC Test		500	
		ST93C06*6			1000	ns
		ST93C06*3			1000	
t_{SV}	CS to STATUS VALID	ST93C06*1	AC Test		500	
		ST93C06*6			1000	ns
		ST93C06*3			1000	
t_{DF}	CS to DO in	ST93C06*1	AC Test		100	
	TRI-STATE	ST93C06*6	CS = V_{IL}		200	ns
		ST93C06*3			200	
t_{WP}	Write Cycle TIME				10	ms

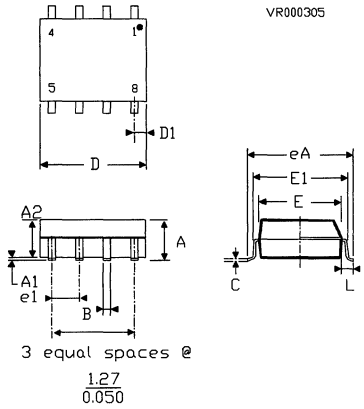
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

ORDERING INFORMATION

PART NUMBER	MAX FREQUENCY	SUPPLY VOLTAGE	TEMP. range	package
ST93C06B1	1 Mhz	5V ± 10 %	0° to + 70°C	PDIP8
ST93C06B6	0.5 Mhz	5V ± 10 %	- 40° to + 85°C	PDIP8
ST93C06B3	0.5 Mhz	5V ± 10 %	- 40° to + 125°C	PDIP8
ST93C06M1	1 Mhz	5V ± 10 %	0° to + 70°C	PSO8
ST93C06M6	0.5 Mhz	5V ± 10 %	- 40° to + 85°C	PSO8
ST93C06M3	0.5 Mhz	5V ± 10 %	- 40° to + 125°C	PSO8

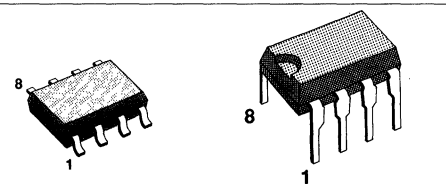
SGS-THOMSON MICROELECTRONICS

ST93C46A

1 K BITS (64x16 or 128x8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

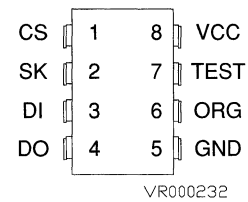
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- OVER 1 MILLION ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- 64 X 16 OR 128 X 8 MEMORY FORMAT USER SELECTABLE.
- WORD AND CHIP PROGRAMMING MODE.
- SELF TIMED PROGRAMMING CYCLE WITH AUTOERASE.
- READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SINGLE POWER SUPPLY IN ALL MODES (5V +/- 10%).
- SEQUENTIAL REGISTER READ.



PSO8 **PDIP8**

(Ordering information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION :

The ST93C46A is a 1024 bits non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology. It is an external memory accessed via a simple serial interface.

The 1K bits memory capacity is divided in either 64 registers of 16 bits each or 128 registers of 8 bits each. The default memory organization is 64 by 16 but it can be switched to 128 by 8 thanks to the "ORG" pin.

The read instruction loads the address of the first register to be read into an 8 bits address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address, it's possible, if the "CS" is held high, to produce a serial data stream. In that case, the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 1024 bits. Thus the ST93C46A can be viewed as a non volatile shift register.

In programming mode, the ST93C46A do not require an erase cycle prior to the write instructions. All programming cycles are completely self timed for simplified operations. The standard "write" cycle allows to write 16 bits (resp 8 bits) at a time into one of the 64 (resp 128) data registers.

Following the initiation of a programming cycle, the Ready/Busy status of the chip is available on the "D_O" pin if "CS" is brought high.

PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
D_I	SERIAL DATA INPUT
D_O	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
ORG	ORGANIZATION SELECTION INPUT
GND	GROUND
TEST	THIS PIN IS FOR SGS-THOMSON INTERNAL USE ONLY

A special internal feature of the ST93C46A, "Power on data protection", allows to inhibit all operating modes if Vcc is too low. This feature is particularily useful when powering up the chip.The design of the ST93C46A and its processing with a highly reliable technology yields to typical endurance over 1 million cycles and data retention greater than 10 years.

MEMORY ORGANIZATION :

The ST93C46A is organized, by default, in 64 X 16. Thanks to the ORG pin this organization can be changed. If the ORG pin is connected to Vcc or left unconnected the ST93C46A will stay in the 64 by 16 organization. If the ORG pin is conected to ground, the 128 by 8 organization is selected.

POWER ON DATA PROTECTION :

During power up, all modes of operations are inhibited until Vcc has reached a level between 2.5 and 3.5 v. Reciprocally all modes were inhibited if Vcc falls below the voltage range 2.0 to 3.0 v.

OPERATING MODES :

The ST93C46A has 7 instructions as described in table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 2 bits carry the OP code and the following 6 bits (respectively 7 bits in 128 by 8 organization) the address for register selections.

READ

The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16 bits (resp. 8 bits) out shift register. A dummy bit (logical 0) precedes the 16 (resp. 8 bits) data output string.. Output data changes are initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits (resp. 8 bits) are clocked out as long as CS is held high.

Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode, the dummy bit is suppressed and a continuous string of data is obtained.

ERASE / WRITE ENABLE (EWEN)

All programming modes must be preceded by an Erase/Write Enable instruction. Once an Erase/Write enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or Vcc is removed from the part.(Note that after a powering up, the part is in the Erase/Write Disable state).

ERASE / WRITE DISABLE (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disable all programming modes and should follow all programming operations. Execution of a Read instruction is independent of both the EWEN and EWDS instructions.

ERASE (ERASE)

The Erase instruction is a programming instruction which sets all bits of the specified register to the logical "1" state. After the last address bit has been loaded, CS is brought low and this falling edge initiates the self timed programming cycle. The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs" (see section on Ready/Busy status).

WRITE (WRITE)

The Write instruction is followed by 16 (respectively 8) bits of data to be written into the specified address. After the last bit of data is clocked in on the data-in (D_I) pin, CS must be brought low before the next rising edge of the SK clock.This falling edge of CS initiates the self-timed programming cycle.

The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs" (see section on Ready/Busy status).

ERASE ALL (ERAL)

This instruction is provided to erase the whole chip. With this instruction, each bit of all registers in the memory array is set to the logical "1" state.This programming cycle works in the same way as the ERASE cycle.

WRITE ALL (WRAL)

This instruction is provided to program simultaneously all registers with the data pattern specified in the instruction. All the registers must be erased before doing a WRAL operation; Then, the WRITE ALL programming instruction works in the same way as the WRITE instruction.

READY / BUSY STATUS

During every programming cycle (Erase, Write, Erase all, Write all), the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs". D_O = logical "0" indicates that the programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction (or all the memory array for ERAL and WRAL instructions) have been programmed, and the part is ready for another instruction. If the part is "ready", the logical "1" on the D_O pin will disappear as soon as the start bit of a new instruction is loaded on the D_I pin.

COMMON I/O SIGNAL

D_I and D_O pins can be connected together. However some precautions should be taken; Therefore it's advised to refer to the SGS-THOMSON application note : "Serial EEPROM Memories : A design guide for common I/O Application".

NOTE ABOUT PIN "TEST"

This pin doesn't affect the device functionality and it is reserved for SGS-THOMSON internal use. For the user, this pin can be either left unconnected or connected to any voltage between Vss and Vcc (Vss and Vcc included).

TABLE 1 : INSTRUCTION SET FOR ST93C46A, ORGANIZATION : 64 x 16

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	COMMENTS
READ	1	10	A_5-A_0		Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXX		Erase/Write enable must precede all programing modes.
EWDS	1	00	00XXXX		Disables all programming instructions.
ERASE	1	11	A_5-A_0		Erase register defined by the specified address.
WRITE	1	01	A_5-A_0	D_{15}-D_0	Writes registers.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D_{15}-D_0	Write all registers.

TABLE 2 : INSTRUCTION SET FOR ST93C46A, ORGANIZATION : 128 x 8 ("ORG" PIN CONNECTED TO GND)

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	COMMENTS
READ	1	10	A_6-A_0		Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXXX		Erase/Write enable must precede all programing modes.
EWDS	1	00	00XXXXX		Disables all programming instructions.
ERASE	1	11	A_6-A_0		Erase register defined by the specified address.
WRITE	1	01	A_6-A_0	D_7-D_0	Writes registers.
ERAL	1	00	10XXXXX		Erase all registers.
WRAL	1	00	01XXXXX	D_7-D_0	Write all registers.

Figure 1 : ST93C46A Block diagram

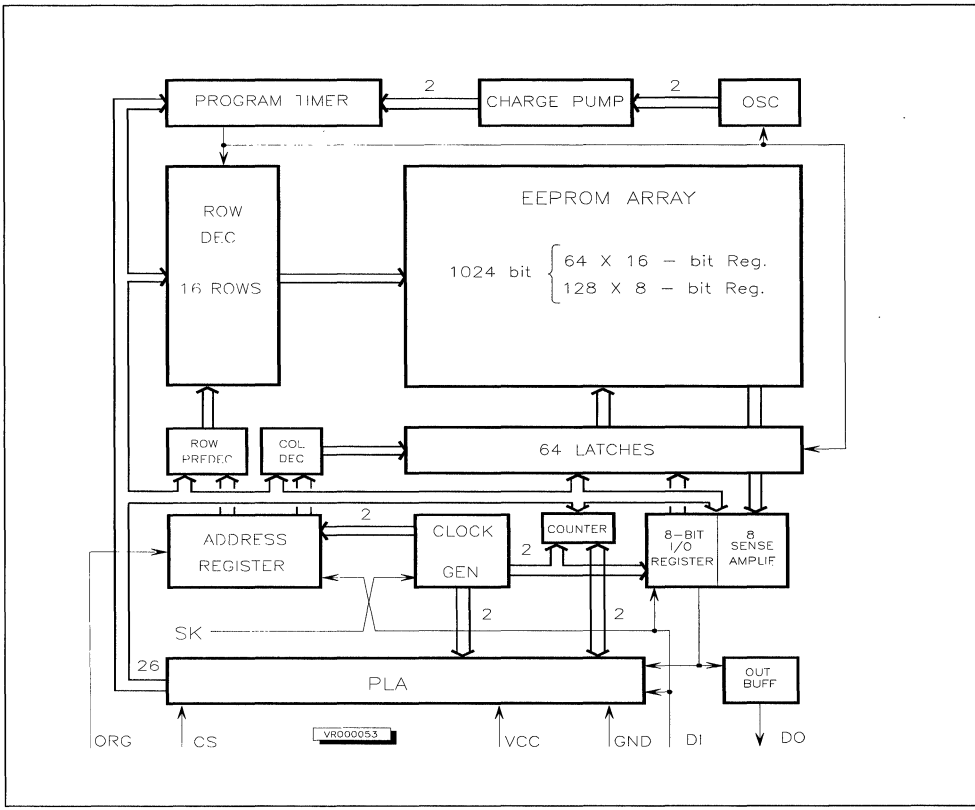


Figure 2 : Synchronous Timing

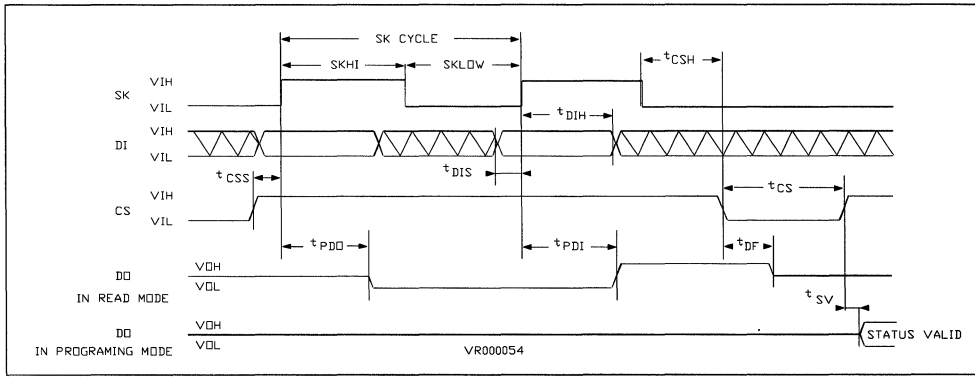


Figure 3 : READ

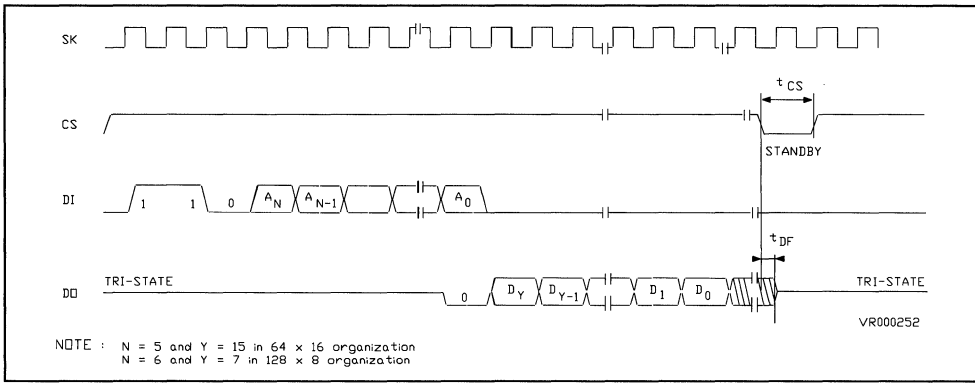


Figure 4 : WRITE

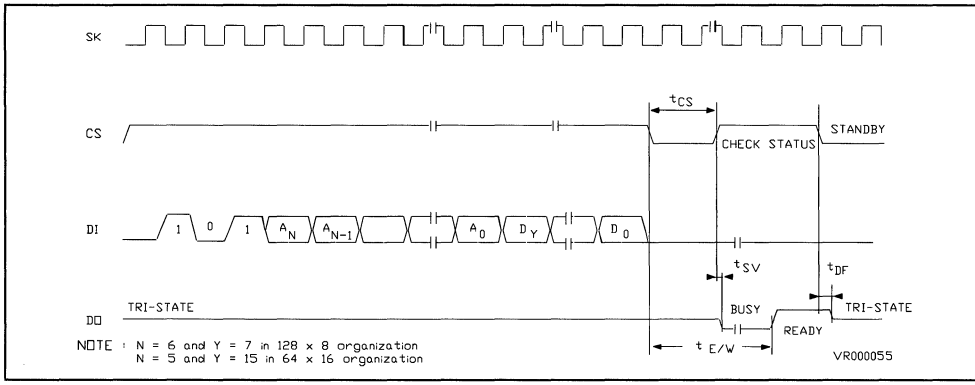


Figure 5 : EWEN/EWDS

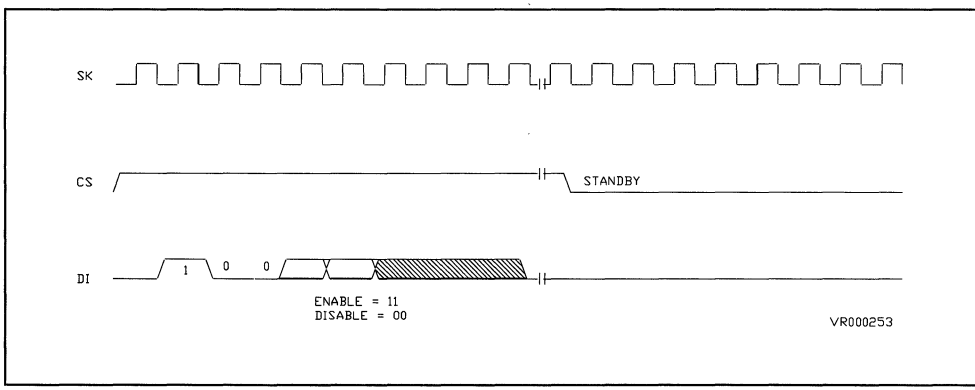


Figure 6 : ERASE

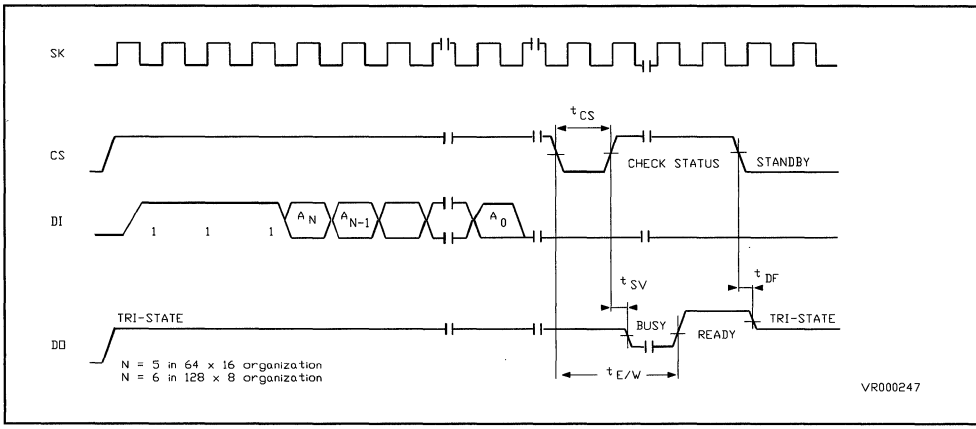


Figure 7 : ERAL

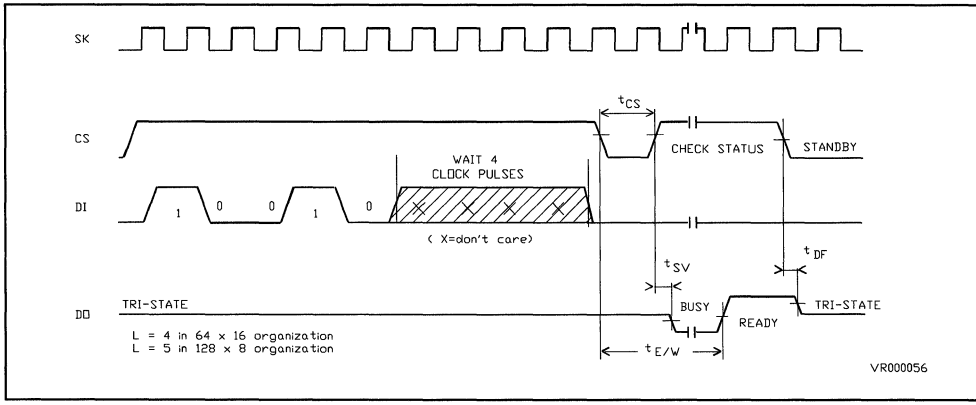
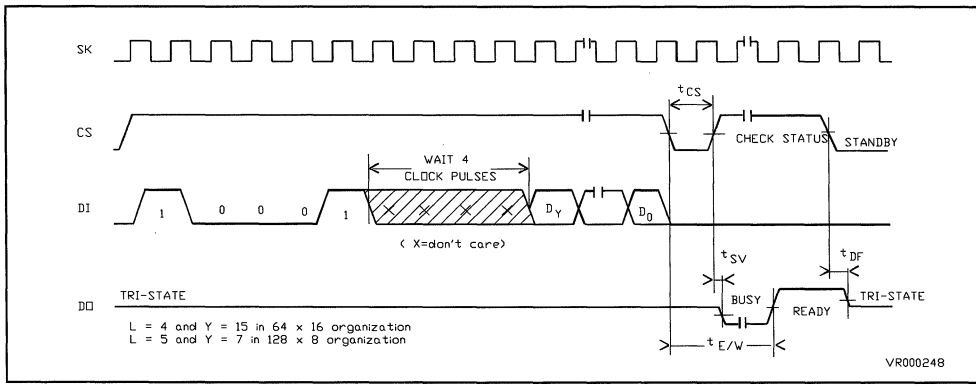


Figure 8 : WRAL



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Ambient storage temperature -65°C to +150°C

All input or output voltage whith respect to ground -0.3v to + 6.5v

Lead Temp (Soldering, 10 sec.) +300°C MAX.

ESD rating 2000v MAX.

DC & AC Electrical characteristics Vcc = 5v +/- 10% (unless otherwise specified)

OPERATINGS CONDITIONS

Ambient operating temperature

ST93C46A *1 0°C to +70°C

ST93C46A *6 -40°C to + 85°C

ST93C46A *3 -40°C to +125°C

Positive power supply 4.5v to 5.5v

* = B = Dual in line package

* = M = SO8 package

CAPACITANCE(note 6) (TA = 25°C, f = 1 Mhz)

SYMBOL	TEST	TYP	Max	Units
COUT	Output Capacitance		5	pF
CIN	Input Capacitance		5	pF

AC Test Conditions

Output Load 1TTL gate and CL= 1OOpF
Input Pulse Levels 0.4v to 2.4v
Timing mesurement Reference level
Input 1v and 2v
Ouput 0.8v and 2v

NOTE 1 : Stress above those listed under " Absolute Maximum ratings " may cause permanent dammage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2 : The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle tSKH + tSKL must be greater or equal to 1microsecond. For example if tSKL = 250 ns then the minimum tSKH = 750 ns in order to meet the SK frequency specification.

3 : The SK frequency specification for extended temperature specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle tSKH + tSKL must be greater or equal to 2 microseconds. For example tSKL = 500 ns then the minimum tSKH = 1.5 Microsecond in order to meet the SK frequency specification.

4 : For commercial parts : CS must be brought low for a minimum of 250ns (tCS) between consecutive instruction cycles.

5 : For extended temperature : CS must be brought for a minimum of 500ns (tCS) between consecutive instruction cycles.

6 : This parameter is periodically sampled and not 100 % tested.

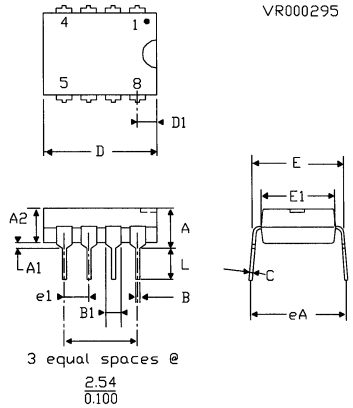
SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
I_{CC1}	OPERATING CURRENT	ST93C46A*1	CS=VIH,SK=1MHZ		2	mA
	CMOS INPUT LEVELS	ST93C46A*6	SK=0.5MHZ		2	mA
		ST93C46A*3	SK=0.5MHZ		2	mA
I_{CC2}	OPERATING CURRENT	ST93C46A*1	CS=VIH,SK=1MHZ		3	mA
	TTL INPUT LEVELS	ST93C46A*6	SK=0.5MHZ		3	mA
		ST93C46A*3	SK=0.5MHZ		4	mA
I_{CC3}	STANDBY CURRENT	ST93C46A*1	CS=0V		50	uA
		ST93C46A*6			100	uA
		ST93C46A*3			100	uA
I_{IL}	INPUT LEAKAGE	ST93C46A*1	VIN=0V TO VCC	-2.5	2.5	uA
		ST93C46A*6		-10	10	uA
		ST93C46A*3		-10	10	uA
I_{OL}	OUTPUT LEAKAGE	ST93C46A*1	VOUT=0V TO VCC	-2.5	2.5	uA
		ST93C46A*6		-10	10	uA
		ST93C46A*3		-10	10	uA
V_{IL}	INPUT LOW VOLTAGE			-0.1	0.8	V
V_{IH}	INPUT HIGH VOLTAGE			2	VCC+1	V
V_{OL1}	OUTPUT LOW VOLTAGE		IOL =2.1 mA		0.4	V
V_{OH1}	OUTPUT HIGH VOLTAGE		IOH = - 400 uA	2.4		V
V_{OL2}	OUTPUT LOW VOLTAGE		IOL =10 uA		0.2	V
V_{OH2}	OUTPUT HIGH VOLTAGE		IOH = - 10 uA	VCC-0.2		V
f_{SK}	SK CLOCK FREQUENCY	ST93C46A*1		0	1	
		ST93C46A*6		0	0.5	MHZ
		ST93C46A*3		0	0.5	
t_{SKH}	SK HIGH TIME	ST93C46A*1	(Note 2)	250		
		ST93C46A*6	(Note 3)	500		nS
		ST93C46A*3	(Note 3)	500		
t_{SKL}	SK LOW TIME	ST93C46A*1	(Note 2)	250		
		ST93C46A*6	(Note 3)	500		nS
		ST93C46A*3	(Note 3)	500		
t_{CS}	MINIMUM CS	ST93C46A*1	(Note 4)	250		
	LOW TIME	ST93C46A*6	(Note 5)	500		nS
		ST93C46A*3	(Note 5)	500		
t_{CSS}	CS SETUP TIME	ST93C46A*1	Relative to SK	50		
		ST93C46A*6		100		nS
		ST93C46A*3		100		
t_{CSH}	CS HOLD TIME		Relative to SK	0		nS
t_{DIS}	DI SETUP TIME	ST93C46A*1	Relative to SK	100		
		ST93C46A*6		200		nS
		ST93C46A*3		200		
t_{DIH}	DI HOLD TIME	ST93C46A*1	Relative to SK	100		
		ST93C46A*6		200		nS
		ST93C46A*3		200		
t_{PD1}	Output Delay to "1"	ST93C46A*1	AC Test		500	
		ST93C46A*6			1000	nS
		ST93C46A*3			1000	
t_{PD0}	Output Delay to "0"	ST93C46A*1	AC Test		500	
		ST93C46A*6			1000	nS
		ST93C46A*3			1000	
t_{SV}	CS to STATUS VALID	ST93C46A*1	AC Test		500	
		ST93C46A*6			1000	nS
		ST93C46A*3			1000	
t_{DF}	CS to DO in	ST93C46A*1	AC Test		100	
	TRI-STATE	ST93C46A*6	CS = VIL		200	nS
		ST93C46A*3			200	
t_{WP}	Write Cycle TIME				10	mS

ORDERING INFORMATION

PART NUMBER	MAX FREQUENCY	SUPPLY VOLTAGE	TEMP. range	package
ST93C46AB1	1 Mhz	5v +/- 10 %	0° to + 70°C	PDIP8
ST93C46AB6	0.5 Mhz	5v +/- 10 %	- 40° to + 85°C	PDIP8
ST93C46AB3	0.5 Mhz	5v +/- 10 %	- 40° to + 125°C	PDIP8
ST93C46AM1	1 Mhz	5v +/- 10 %	0° to + 70°C	PSO8
ST93C46AM6	0.5 Mhz	5v +/- 10 %	- 40° to + 85°C	PSO8
ST93C46AM3	0.5 Mhz	5v +/- 10 %	- 40° to + 125°C	PSO8

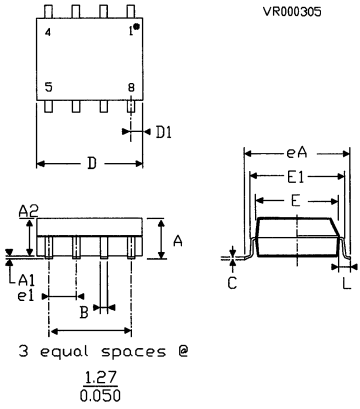
PACKAGE MECHANICAL DATA

PDIL8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

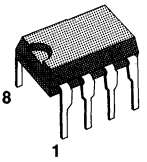
SGS-THOMSON MICROELECTRONICS

ST93CS46

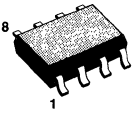
1 K BITS (64 x 16) SERIAL ACCESS CMOS EEPROM MEMORY

ADVANCE DATA

- USER DEFINED AREA OF WRITE PROTECTED MEMORY.
- WORD AND PAGE WRITE MODES.
- HIGH RELIABILITY CMOS EEPROM TECHNOLOGY.
- TYPICALLY OVER 1,000,000 ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- SINGLE POWER SUPPLY IN ALL MODES 5V ±10 %.
- SELF TIMED PROGRAMMING CYCLE WITH READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SEQUENTIAL REGISTER READ.



PDIP8



PSO8

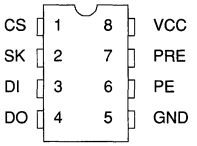
(Ordering information at the end of the datasheet)

PIN NAMES

CS	Chip Select
SK	Serial Data Clock
D_I	Serial Data Input
D_O	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

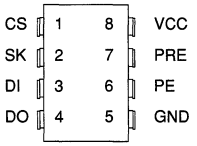
PIN CONNECTION

Dual-in-line Package (B) - top view



VR000224

SO Package (M) - top view



VR000232

DESCRIPTION

The ST93CS46 is a 1024 bit non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology.

The memory is accessed via a simple serial interface.

The 1K bit capacity is divided into 64 registers of 16 bits each. A special feature of this device allows the user to protect data against modification at and above a specified register, by programming the address of the first register, to be protected, into the specific on chip register called the "memory protect register".

It is also possible to protect permanently the data of these registers by using a one time only instruction (PRDS) after wich the address in the protect register cannot be altered.

Thereafter, all attemps to alter data in a register whose address is equal to or greater than the address stored in the "protected register" will be aborted.

The "read" instruction loads the address of the first register to be read in to an 6 bit address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address it is possible, if the "CS" is held high, to produce a serial data stream. In that case the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 1024 bits. Thus the ST93CS46 can be viewed as a non volatile shift register. In a programming mode the ST93CS46 does not require an erase cycle prior to the write instructions. All programming cycles are completely self-timed for simplified operations. The Ready/Busy status of the device is available on the "D_O" pin if "CS" is brought "high" following the initiation of "Write" cycle. The standard "Write" cycle allows to write 16 bits at a time into one of the 64 data registers. (If the address of the register to be written is less than the address of " Protect Register").

Another write instruction : "PAWRITE" (parallel write) makes possible to write up to 4 words of 16 bits each as the same time. The design of the ST93CS46 and the processing with the technology yields to typical endurance over 1 million cycles and data retention greater than 10 years after.

FUNCTIONAL DESCRIPTION

The ST93CS46 has 11 instructions described in the table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence.

The next 2 bits carry the OP code and the following 6 bits the address for the registers selection.

***Read (READ)** :

The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16 bits serial outshift register. A dummy bit (logical 0) precedes the 16 bits data output string. An ouput data change is initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits are clocked out. Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode the dummy bit is suppressed and continuous string of data is obtained.

*** Write Enable (WEN) :**

When V_{CC} is applied to the device, it powers up in the write Disable (WDS) state. Therefore all programming modes must be preceded by Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the device.

*** Write (WRITE) :** Note 1

The write instruction is followed by 16 bits of data to be written into the specified address. After the less bit of the data is put on the data- in "DI" pin, CS must be brought low before the next rising edge of the SK Clock. This falling edge of CS initiates the selftimed programming cycle. The PE pin MUST be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction, the PE pin becomes a "Don't care". The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}".

D_O = logical "0" indicates that programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction has been written with data pattern specified in the instruction and the part is ready for another instruction.

*** Parallel Write (PAWRITE) : Note 1**

The PAWRITE instruction is followed by up to 4 Words of 16 bits of data, to be written starting from the specified address. after the last bit of data (D_O) is put on the data-in (D_I) pin, CS must be brought low before the next rising edge SK clock. This falling edge of the CS initiates the self-timed programming cycle. The pin must be held "high" while loading the write instruction, however, after loading the write PE pin becomes a "don't care".

The D_O pin indicates the Ready/Busy status Chip if "CS" is brought high after a minimum of "T_{CS}". D_O = logical "0" indicates that programming is still in progress. D_O = Logical "1" indicates that the register(s) specified in the instruction as been written with the data pattern specified in the instruction and the part is ready for another instruction.

Note that only the address bits A_5 to A_2 will be compared with protect register content, and the PAWRITE operation will be aborted if (A_5, A_4, A_3, A_2) ≥ (A_5, A_4, A_3, A_2) stored in the protect register. Note also that, after the receipt of each data word, the 2 low order address bit (A_1, A_0) are internally incremented by one whereas, the high order five bits of the address remain constant. Therefore in order to avoid that the address rolls over and overwrite the written data, the user must take care in the software, that in the PAWRITE mode the final word address has the same five high order bits than the initial transmitted address.

*** Write All (WRALL) : Note 1**

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with a data pattern specified in the instruction. Like the write instruction the PE pin MUST be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}".

Note 1 : For any programming modes, the "1" status bit on the D_O pin will disappear as soon as the start bit of a new instruction is presented on the D_I pin.

*** Write Disable (WDS) :**

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of the both the WEN and WDS Instructions.

***Protect Register Read (PRREAD) :**

Prelimary note : Since the protect register content can be the same after a PRWRITE with the "111111" address and after a PRCLEAR instruction, a specific bit is added in the protect register in order to identify the status of the protect register. If the protect register has been cleared this status bit is set to "1" else it is set to "0".

The protect register Read (PRREAD) instruction outputs on the DO pin the address stored in the "protect register" and the "protect register status bit".

The PRE pin MUST be held "high" while loading the instruction. Following the PRREAD instruction the 8 bit address stored in the memory "protect register" and the "protect register status bit" are transfered to the serial-out shift register. Note that the "protect register status bit" immediately follows the 8 bit address string and that, as in the READ mode, a dummy bit (logical 0) precedes this 9 bits string.

***Protect Register Enable (PREN) :**

The protect register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE and PRDS modes. Before the PREN mode can be ENTERED. the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins MUST be held "high" while loading the instruction.

***Protect Register Clear (PRCLEAR) :**

The protect register clear (PRCLEAR) instruction clears the address stored in the protect register and therefore, enables all registers for the WRITE and WRALL instruction. The PRE and PE pins must be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRCLEAR instruction.

***Protect Register Write (PRWRITE) :**

The protect register write (PRWRITE) instruction is used to write into the protect register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the protect register are protected from the write operation.

The PRE and PE pins must be held "high" while loading the instruction. However, after loading the PRWRITE instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRWRITE instruction.

Since, as in the WRITE mode, an autoerase is performed there is no need that a PRCLEAR operation precedes a PRWRITE instruction.

*** Protect Register Disable (PRDS) :**

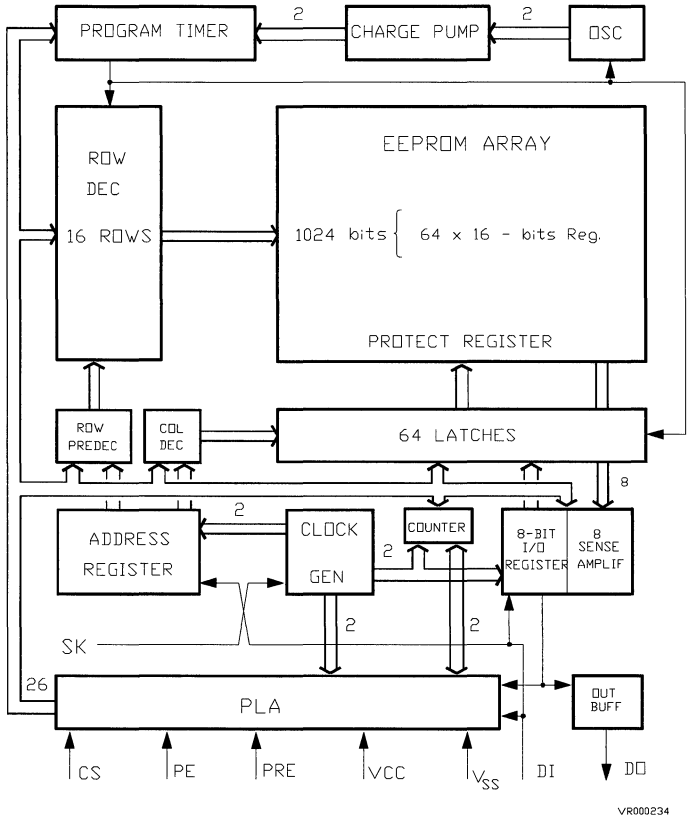
The protect register Disable (PRDS) instruction is a one time only instruction which renders the protect register unalterable in the future. Therefore, the specified registers become PERMANENTLY protected against data changes. As in the PRWRITE instruction the PRE and PE pins must be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRDS instruction.

INSTRUCTION SET INSTRUCTION FOR ST93CS46

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	PRE	PE	COMMENTS
READ	1	10	A_5-A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_5-A_0	D_{15}-D_0	0	1	Writes register if address is unprotected.
PAWRITE	1	11	A_5-A_0	D_{15}-D_0	0	1	Writes n registers (n≤4) if addresses are unprotected.
				n x (n ≤ 4)			
WRALL	1	00	01XXXX		0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the "protect register" so that no registers are protected from Write.
PRWRITE	1	01	A_5-A_0		1	1	Programs address into protect Register. Thereafter, memory address ≥ the address in protect register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after wich the address in the Protect Register cannot be altered.

Figure 1 : ST93CS46 Block Diagram



ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE	UNIT
Ambient Storage Temperature	-65 to +150	°C
All Input or Output Voltages Relative to GND	+6.5 to -0.3	V
Lead Temperature	+300	°C
ESD rating	2000	V

CAPACITANCE (note 6)

TA = 25°C, f = 1MHz

SYMBOL	TEST	TYP	MAX	MIN
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC TEST CONDITIONS

Ouput Load . . . . . 1 TTL GATE and C_L = 100 pF

Input Pulse Levels . . . . . .0.4V to 2.4V

Timing Measurement Reference Level :

Input . . . . . .1V and 2V

Output . . . . . 0.8V and 2V

OPERATING CONDITIONS

Ambient Operating Temperature

ST93C46-1 _____ 0°C 70°C

ST93C46-6 _____ -40°C to + 85°C

ST93C46-3 _____ -40°C to +125°C

-= B _____ Dual-in-line Package

-= M _____ SO8 Package

Positive Power Supply _____ 4.5V to 5.5V

DC & AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10 % unless otherwise specified)

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
I_{CC1}	Operating Current	ST93CS46-1	CS=V_{IH}, SK=1MHz		2	
	CMOS Input Levels	ST93CS46-6	SK=0.5 MHz		2	mA
		ST93CS46-3	SK=0.5 MHz		2	
I_{CC2}	Operating Current	ST93CS46-1	CS=V_{IH}, SK=1MHz		3	
	TTL Input Levels	ST93CS46-6	SK=0.5 MHz		3	mA
		ST93CS46-3	SK=0.5 MHz		4	
I_{CC3}	Standby Current	ST93CS46-1	CS = 0V		50	
		ST93CS46-6			100	µA
		ST93CS46-3			100	
I_{IL}	Input Leakage	ST93CS46-1	V_{IN} = 0V to V_{CC}	-2.5	2.5	
		ST93CS46-3		-10	10	µA
		ST93CS46-6		-10	10	µA
I_{OL}	Output Leakage	ST93CS46-1	V_{OUT} = 0V to V_{CC}	-2.5	2.5	
		ST93CS46-3		-10	10	µA
		ST93CS46-6		-10	10	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC}+1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -10 µA	V_{CC}-0.2		V
f_{SK}	SK Clock Frequency	ST93CS46-1		0	1	
		ST93CS46-3		0	0.5	MHz
		ST93CS46-6		0	0.5	
t_{SKH}	SK High Time	ST93CS46-1	(Note 2)	250		
		ST93CS46-3	(Note 3)	500		ns
		ST93CS46-6	(Note 3)	500		
t_{SKL}	SK Low Time	ST93CS46-1	(Note 2)	250		
		ST93CS46-3	(Note 3)	500		ns
		ST93CS46-6	(Note 3)	500		
t_{CS}	Minimum CS Low Time	ST93CS46-1	(Note 4)	250		
		ST93CS46-3	(Note 5)	500		ns
		ST93CS46-6	(Note 5)	500		
t_{CSS}	CS Set-up Time	ST93CS46-1	Relative to SK	50		
		ST93CS46-3		100		ns
		ST93CS46-6		100		
t_{PRES}	PRE Set-up Time	ST93CS46-1	Relative to SK	50		
		ST93CS46-3		100		ns
		ST93CS46-6		100		

DC & AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10 %) (continued)

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
t_{PES}	PE Set-up Time	ST93CS46-1	Relative to SK	50		ns
		ST93CS46-3		100		
		ST93CS46-6		100		
t_{DIS}	DI Set-up Time	ST93CS46-1	Relative to SK	100		
		ST93CS46-3		200		
		ST93CS46-6		200		
t_{CSH}	CS Hold Time		Relative to SK	0		
t_{PEH}	PE Hold Time	ST93CS46-1	Relative to CS	250		
		ST93CS46-3	Relative to CS	500		
		ST93CS46-6	Relative to CS	500		
t_{PREH}	PRE Hold Time		Relative to SK	0		
t_{DIH}	DI Hold Time	ST93CS46-1	Relative to SK	100		
		ST93CS46-3		200		
		ST93CS46-6		200		
t_{PD1}	Output Delay to "1"	ST93CS46-1	AC TEST		500	
		ST93CS46-3			1000	
		ST93CS46-6			1000	
t_{PD0}	Output Delay to "0"	ST93CS46-1	AC TEST		500	
		ST93CS46-3			1000	
		ST93CS46-6			1000	
t_{SV}	CS to Status Valid	ST93CS46-1	AC TEST		500	
		ST93CS46-3			1000	
		ST93CS46-6			1000	
t_{DF}	CS to DO in TRI STATE	ST93CS46-1	AC TEST		100	
		ST93CS46-3	CS = V_{IL}		200	
		ST93CS46-6			200	
t_{WP}	Write Cycle Time				10	ms
	Endurance		Typical : 1 000 000			cycles

NOTE: 1. Stress above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. **The Sk frequency specification for commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle** t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the maximum t_{SKH} = 750 ns in order to meet the SK frequency specification.
3. **The Sk frequency specification for Extended Temperature specifies a minimum SK clock period of 2 microsecond, therefore in an SK clock cycle** t_{SKH} + t_{SKL} must be greater than or equal to 2 microsecond. For example if t_{SKL} = 500 ns then the maximum t_{SKH} = 1.5 ns in order to meet the SK frequency specification.
4. **For commercial parts CS must be brought low for a minimum of 250 ns (**t_{CS}) between consecutive instruction cycles.
5. **For Extended Temperature CS must be brought low for a minimum of 500 ns (**t_{CS}) between consecutive instruction cycles.
6. **This parameter is periodically sampled and not 100% tested.**

Figure 2 : Synchronous Data Timing

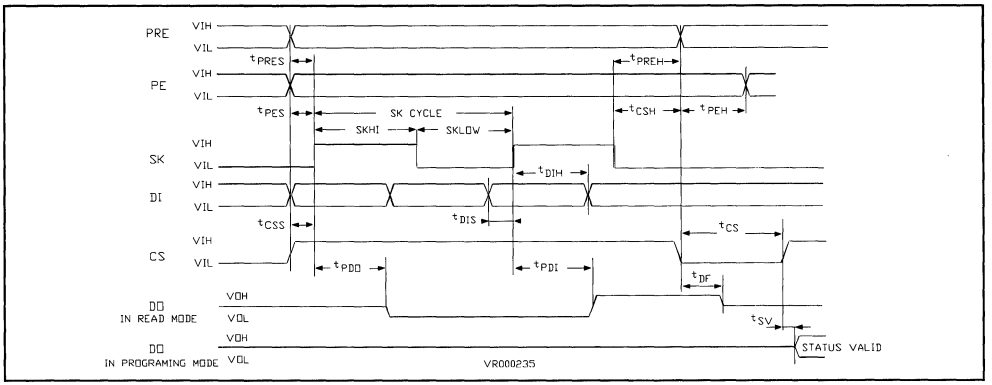


Figure 3 : READ

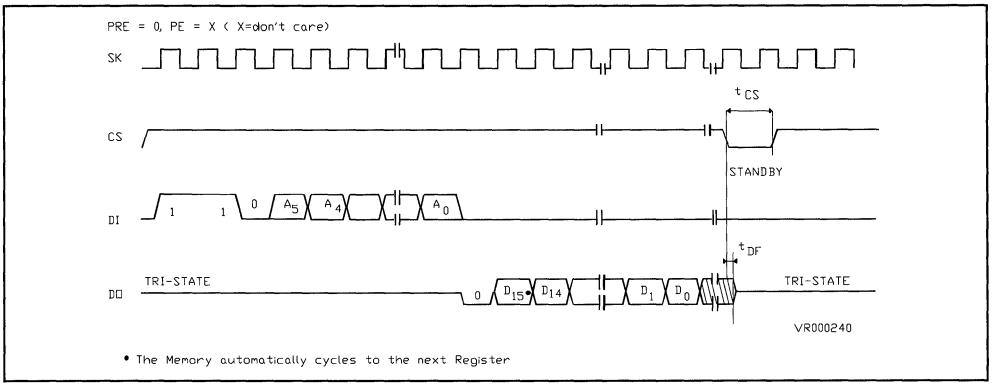


Figure 4 : WEN

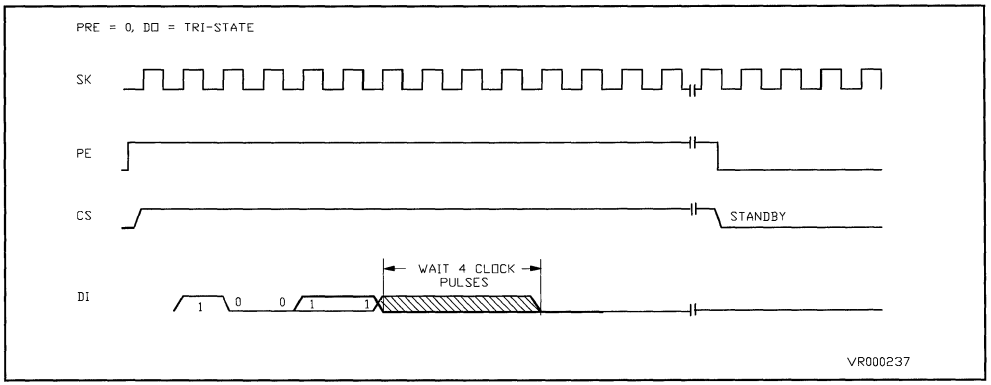


Figure 5 : WDS

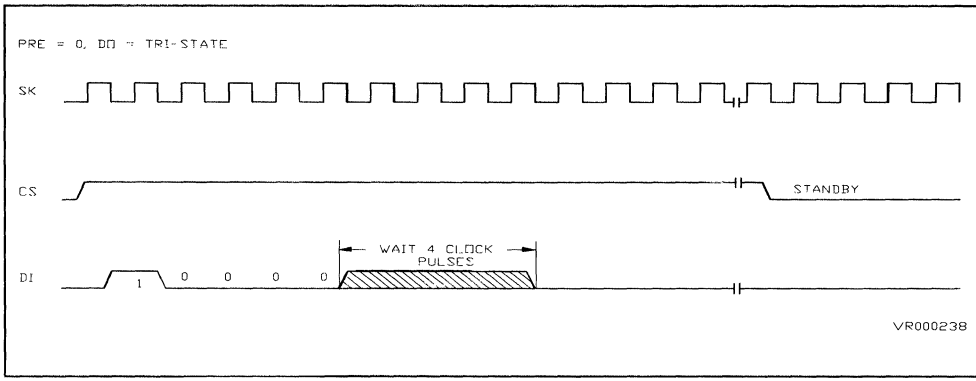


Figure 6 : WRITE

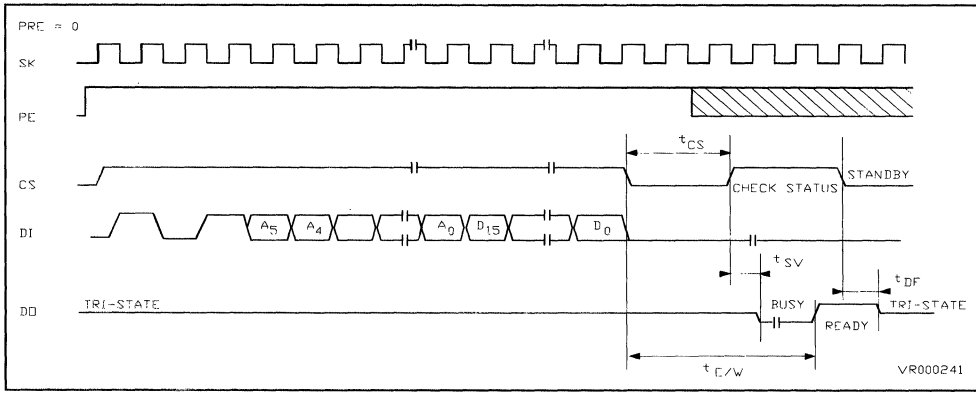


Figure 7 : PAWRITE

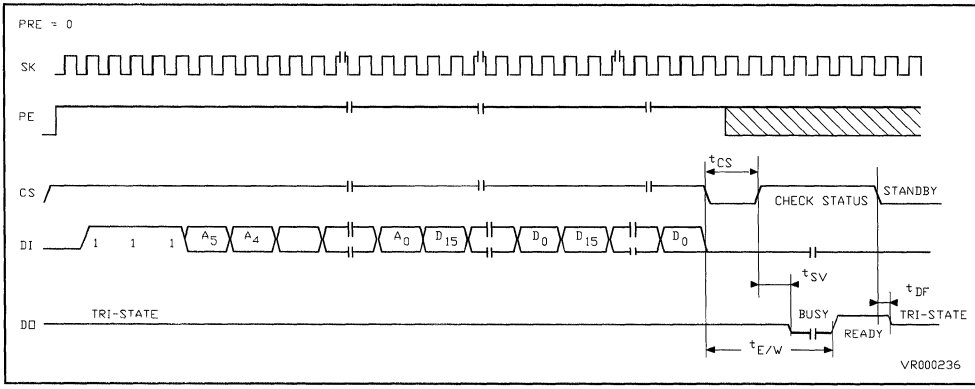


Figure 8 : PRDS

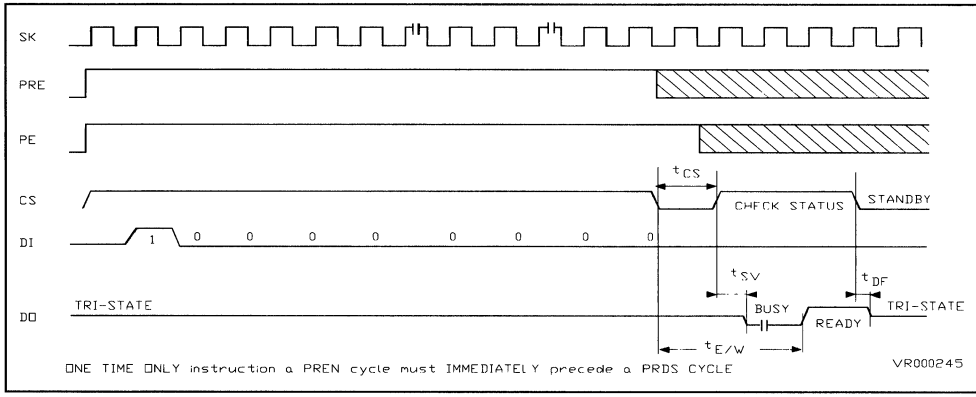


Figure 9 : WRALL

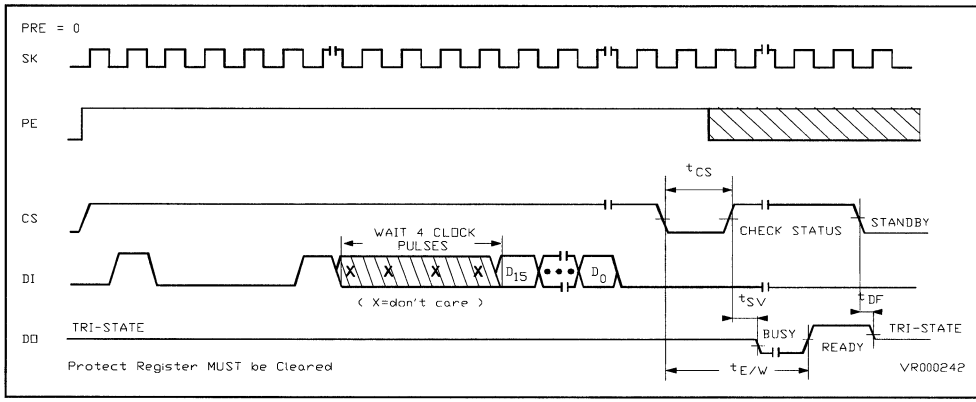


Figure 10 : PRREAD

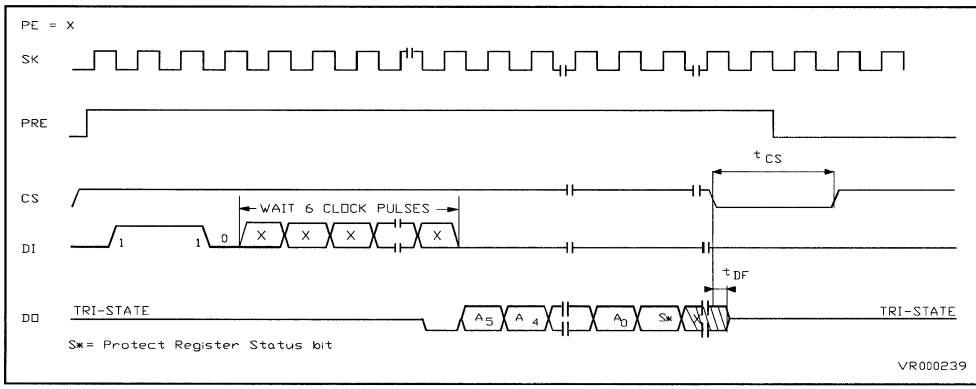


Figure 11 : PREN

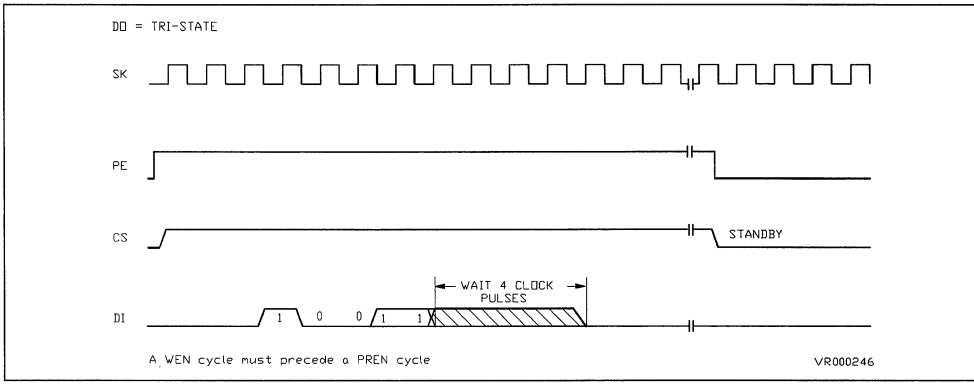


Figure 12 : PR CLEAR

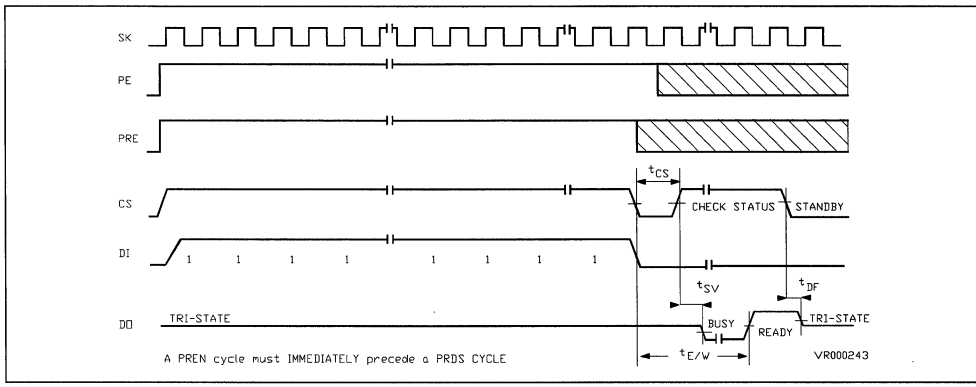
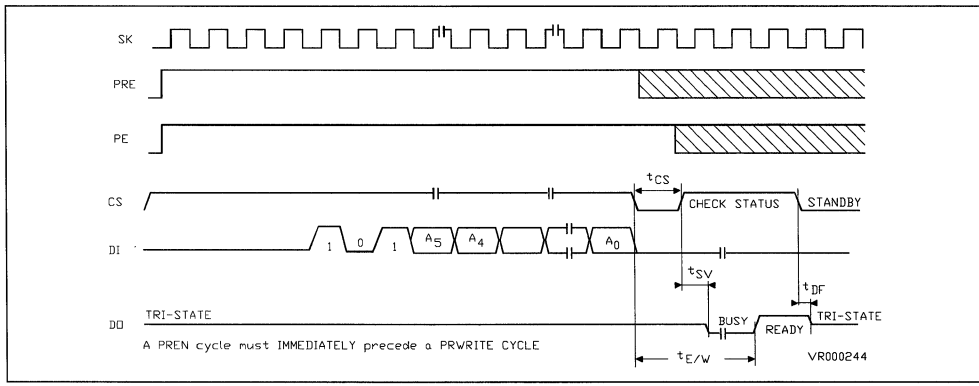


Figure 13 : PR WRITE

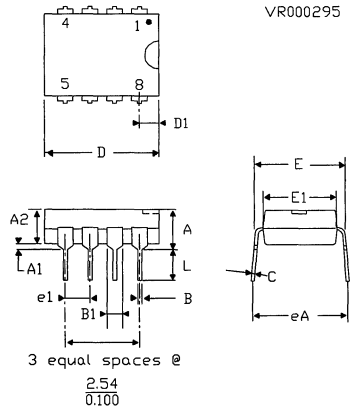


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST93CS46B1	Dual-in-line	0°C to 70°C	4.5V to 5.5V
ST93CS46M1	SO 8		
ST93CS46B6	Dual-in-line	-40°C to 85°C	
ST93CS46M6	SO 8		
ST93CS46B3	Dual-in-line	-40°C to 125°C	
ST93CS46M3	SO 8		

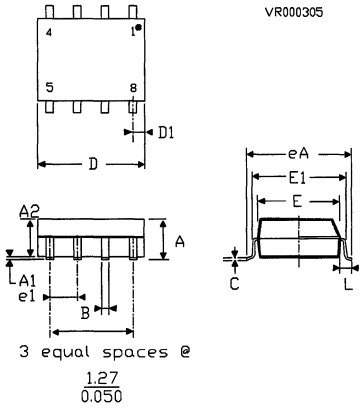
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

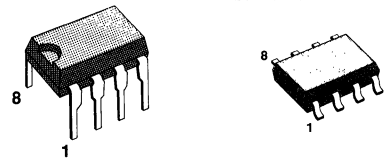
PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

1 K BITS (64 x 16) SERIAL ACCESS CMOS EEPROM MEMORY

- 2.5V - 5.5V SINGLE POWER SUPPLY IN ALL MODES
- USER DEFINED SIZE OF A MEMORY SECTION PROTECTED AGAINST WRITE.
- WORD AND PAGE WRITE MODES.
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- TYPICAL : OVER 1 000 000 ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- SELF TIMED PROGRAMMING CYCLE WITH
- READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SEQUENTIAL REGISTER READ.



PDIP8 PSO8

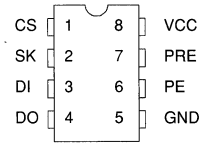
(Ordering information at the end of the datasheet)

PIN NAMES

CS	Chip Select
SK	Serial Data Clock
D_I	Serial Data Input
D_O	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply
NC	Not Connected

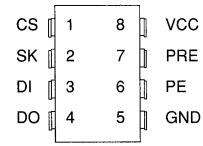
PIN CONNECTION

Dual-in-line Package (B) - top view



VR000224

SO Package (M) - top view



VR000232

DESCRIPTION

The ST93CS47 is a 1024 bits non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology

It is an external memory accessed via a simple serial interface and it works with a power supply voltage as low as 2.5V.

The 1K bits memory capacity is divided in 64 registers of 16 bits each. A special feature of this device allows the user to protect data against any modification in "N" register ($0 \leq N \leq 64$). Since these N registers are following each other, there is no other need to protect them than programming the address of the first register to be protected into specific on chip register called the "memory protect register".

It is also possible to protect permanently the data of these N registers by using a one time only instruction (PRDS) after wich the address in the protect register cannot be altered.

Thereafter, all attemps to alter data in a register whose address is equal to or greater than the address stored in the "protected register" will be aborted.

The "read" instruction loads the address of the first register to be read in to an 6 bits address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address it is possible, if the "CS" is held high, to produce a serial data stream. In that case the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 1024 bits. Thus the ST93CS47 can be viewed as a non volatile shift register. In a programming mode the ST93CS47 do not require an erase cycle prior to the write instructions. All programming cycles are completely self-timed for simplified operations. The Ready/Busy status of the shift is available on the "D_O" pin if "CS" is brought "high" following the initiation of "Write" cycle. The standard "Write" cycle allows to write 16 bits at a time into one of the 64 data registers. (If the address of the register to be written is less than the address of " Protect Register")

Another write instruction :"PAWRITE" (parallel write) makes possible to write up to 4 words of 16 bits each as the same time. The design of the ST93CS47 and the processing with the technology yields to typical endurance over 1 million cycles and data retention greater than 10 years after.

FUNCTIONAL DESCRIPTION :

The ST93CS47 has 11 instructions described in the table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence.

The next 2 bits carry the OP code and the following 6 bits the address for the registers selection.

***Read (READ)** :

The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the sellected memory register into a 16 bits serial outshift register. A dummy bit (logical 0) precedes the 16 bits data output string. An ouput data changes are initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits are clocked out. Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode the dummy bit is suppressed and continuous string of data is obtained.

*** Write Enable (WEN) :**

When V_{CC} is applied to a part, it powers up in the write Disable (WDS) state. Therefore all programming modes must be preceded by Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled untill a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

*** Write (WRITE) :** Note 1

The write instruction is followed by 16 bits of data to be written into the specified address. After the less bit of the data is put on the data- in "DI" pin , CS must be brought low before the next rising edge of the SK Clock. This following edge of CS initiates the selftimed programming cycle. The PE pin MUST be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction, the PE pin becomes a "Don't care". The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}".

D_O = logical "0" indicates that programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction has been written with data pattern specified in the instruction and the part is ready for another instruction.

*** Parallel Write (PAWRITE) :** Note 1

The PAWRITE instruction is followed by up to 4 Words of 16 bits of data, to be written starting from the specified address. after the last bit of data (D_O) is put on the data-in (D_I) pin, CS must be brought low before the next rising edge SK clock. This falling edge of the CS initiates the self-timed programming cycle. The pin must be held "high" while loading the write instruction, however, after loading the write PE pin becomes a "don't care".

The D_O pin indicates the Ready/Busy status Chip if "CS" is brought high after a minimum of "T_{CS}". D_O = logical "0" indicates that programming is still in progress. D_O = Logical "1" indicates that the register(s) specified in the instruction as been written with the data pattern specified in the instruction and the part is ready for another instruction.

Note that only the address bits (A_5, A_4, A_3, A_2) will be compared with protect register content, and the PAWRITE operation will be aborted if (A_5, A_4, A_3, A_2) ≥ (A_5, A_4, A_3, A_2) stored in the protect register. Note also that, after the recept of each data word, the 2 low order address bit (A_1, A_0) are internally incremented by one whereas, the high order five bits of the address remain constant. Therefore in order to avoid that the address rolls over and overwrite the written data, the user must take care in the software, that in the PAWRITE mode the final word address has the same five high order bits than the initial transmitted address.

*** Write All (WRALL) :** Note 1

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with a data pattern specified in the instruction. Like the write instruction the PE pin MUST be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}"

Note 1 : For any programming modes, the "1" status bit on the D_O pin will disappear as soon as the start bit of a new instruction is presented on the D_I pin.

*** Write Disable (WDS) :**

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of the both the WEN and WDS Instructions.

***Protect Register Read (PRREAD)**

Prelimary note : Since the protect register content can be the same after a PRWRITE with the "111111" address and after a PRCLEAR instruction, a specific bit is added in the protect register in order to identify the status of the protect register. If the protect register has been cleared this status bit is set to "1" else it is set to "0".

The protect register Read (PRREAD) instruction outputs on the DO pin the address stored in the "protect register" and the "protect register status bit".

The PRE pin MUST be held "high" while loading the instruction. Following the PRREAD instruction the 8 bit address stored in the memory "protect register" and the "protect register status bit" are transfered to the serial-out shift register. Note that the "protect register status bit" immediately follows the 8 bit address string and that, as in the READ mode, a dummy bit (logical 0) precedes this 9 bits string.

***Protect Register Enable (PREN)**

The protect register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE and PRDS modes. Before the PREN mode can be ENTERED. the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins MUST be held "high" while loading the instruction.

*Protect Register Clear (PRCLEAR)

The protect register clear (PRCLEAR) instruction clears the address stored in the protect register and therefore, enables all registers for the WRITE and WRALL instruction. The PRE and PE pins must be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRCLEAR instruction.

***Protect Register Write (PRWRITE):**

The protect register write (PRWRITE) instruction is used to write into the protect register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the protect register are protected from the write operation.

The PRE and PE pins must be held "high" while loading the instruction. However, after loading the PRWRITE instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRWRITE instruction.

Since, as in the WRITE mode, an autoerase is performed there is no need that a PRCLEAR operation precedes a PRWRITE instruction.

*** Protect Register Disable (PRDS):**

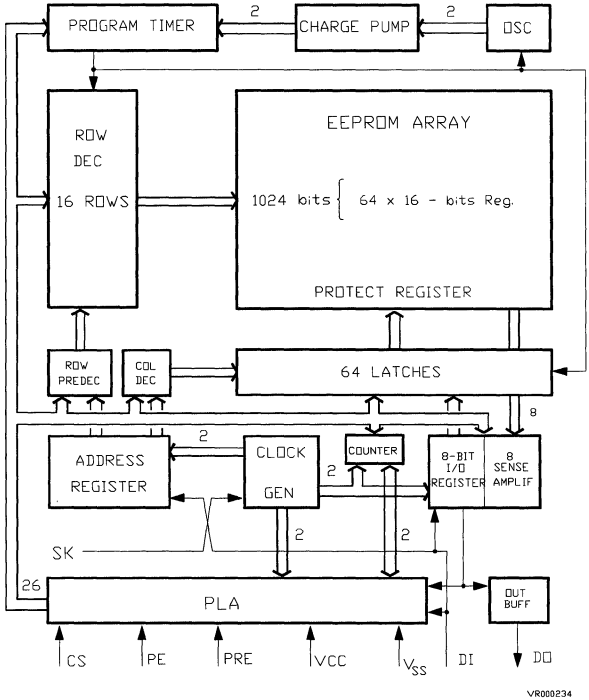
The protect register Disable (PRDS) instruction is a one time only instruction which renders the protect register unalterable in the future. Therefore, the specified registers become PERMANENTLY protected against data changes. As in the PRWRITE instruction the PRE and PE pins must be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRDS instruction.

INSTRUCTION SET INSTRUCTION FOR ST93CS47

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	PRE	PE	COMMENTS
READ	1	10	A_5-A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_5-A_0	D_{15}-D_0	0	1	Writes register if address is unprotected.
PAWRITE	1	11	A_5-A_0	D_{15}-D_0	0	1	Writes n registers (n≤4) if addresses are unprotected.
				n x (n ≤ 4)			
WRALL	1	00	01XXXX		0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the "protect register" so that no registers are protected from Write.
PRWRITE	1	01	A_5-A_0		1	1	Programs address into protect Register. Thereafter, memory address ≥ the address in protect register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after wich the address in the Protect Register cannot be altered.

Figure 1 : ST93CS47 Block Diagram



ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	-65 to +150	°C
All Input or Output Voltages Relative to GND	+6.5 to -0.3	V
Lead Temperature	+300	°C
ESD rating	2000	V

CAPACITANCE (note 6) TA = 25°C, f = 1MHz

SYMBOL	TEST	TYP	MAX	MIN
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC TEST CONDITIONS

Ouput Load . . . . . 1 TTL GATE and C_L = 100 pF

Input Pulse Levels . . . . . .0.4V to 2.4V

Timing Measurement Reference Level :

Input . . . . . .1V and 2V

Output . . . . . 0.8V and 2V

OPERATING CONDITIONS

Ambient Operating Temperature

ST93C47-1 _____ 0°C 70°C

ST93C47-6 _____ -40°C to + 85°C

ST93C47-3 _____ -40°C to +125°C

-= B _____ Dual-in-line Package

-= M _____ SO8 Package

Positive Power Supply _____ 2.5V to 5.5V

DC & AC ELECTRICAL CHARACTERISTICS (V_{CC} =

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
I_{CC1}	Operating Current	ST93CS47-1	CS=V_{IH}, SK=1MHz		2	
	CMOS Input Levels	ST93CS47-6	SK=0.5 MHz		2	mA
		ST93CS47-3	SK=0.5 MHz		2	
I_{CC2}	Operating Current	ST93CS47-1	CS=V_{IH}, SK=1MHz		3	
	TTL Input Levels	ST93CS47-6	SK=0.5 MHz		3	mA
		ST93CS47-3	SK=0.5 MHz		4	
I_{CC3}	Standby Current	ST93CS47-1	CS = 0V		50	
		ST93CS47-6			100	µA
		ST93CS47-3			100	
I_{IL}	Input Leakage	ST93CS47-1	V_{IN} = 0V to V_{CC}	-2.5	2.5	
		ST93CS47-3		-10	10	µA
		ST93CS47-6		-10	10	µA
I_{OL}	Output Leakage	ST93CS47-1	V_{OUT} = 0V to V_{CC}	-2.5	2.5	
		ST93CS47-3		-10	10	µA
		ST93CS47-6		-10	10	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	VCC +1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -10 µA	V_{CC}- 0.2		V
f_{SK}	SK Clock Frequecy	ST93CS47-1		0	1	
		ST93CS47-3		0	0.5	MHz
		ST93CS47-6		0	0.5	
t_{SKH}	SK High Time	ST93CS47-1	(Note 2)	250		
		ST93CS47-3	(Note 3)	500		ns
		ST93CS47-6	(Note 3)	500		
t_{SKL}	SK Low Time	ST93CS47-1	(Note 2)	250		
		ST93CS47-3	(Note 3)	500		ns
		ST93CS47-6	(Note 3)	500		
t_{CS}	Minimum CS Low Time	ST93CS47-1	(Note 4)	250		
		ST93CS47-3	(Note 5)	500		ns
		ST93CS47-6	(Note 5)	500		
t_{CSS}	CS Set-up Time	ST93CS47-1	Relative to SK	50		
		ST93CS47-3		100		ns
		ST93CS47-6		100		
t_{PRES}	PRE Set-up Time	ST93CS47-1	Relative to SK	50		
		ST93CS47-3		100		ns
		ST93CS47-6		100		

DC & AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.5V to 5.5V unless otherwise specified) continued

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
t_{PES}	PE Set-up TIme	ST93CS47-1	Relative to SK	50		
		ST93CS47-3		100		
		ST93CS47-6		100		
t_{DIS}	DI Set-up Time	ST93CS47-1	Relative to SK	100		
		ST93CS47-3		200		
		ST93CS47-6		200		
t_{CSH}	CS Hold Time		Relative to SK	0		
t_{PEH}	PE Hold Time	ST93CS47-1	Relative to CS	250		
		ST93CS47-3	Relative to CS	500		
		ST93CS47-6	Relative to CS	500		
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	ST93CS47-1	Relative to SK	100		
		ST93CS47-3		200		
		ST93CS47-6		200		
t_{PD1}	Output Delay to "1"	ST93CS47-1	AC TEST		500	
		ST93CS47-3			1000	
		ST93CS47-6			1000	
t_{PD0}	Output Delay to "0"	ST93CS47-1	AC TEST		500	
		ST93CS47-3			1000	
		ST93CS47-6			1000	
t_{SV}	CS to Status Valid	ST93CS47-1	AC TEST		500	
		ST93CS47-3			1000	
		ST93CS47-6			1000	
t_{DF}	CS to DO in TRI STATE	ST93CS47-1	AC TEST		100	
		ST93CS47-3	CS = V_{IL}		200	
		ST93CS47-6			200	
t_{WP}	Write Cycle Time				10	ms
	Endurance		Typical : 1 000 000			cycles

NOTE: 1. Stress above those listed under "absolute maximum ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. **The Sk frequency specification for commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle** t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the maximum t_{SKH} = 750 ns in order to meet the SK frequency specification.
3. **The Sk frequency specification for Extended Temperature specifies a a minimum SK clock period of 2 microsecond, therefore in an SK clock cycle** t_{SKH} + t_{SKL} must be greater than or equal to 2 microsecond. For example if t_{SKL} = 500 ns then the maximum t_{SKH} = 1.5 ns in order to meet the SK frequency specification.
4. **For commercial parts CS must be brought low for a minimum of 250 ns (t_{CS})** between consecutive instruction cycles.
5. **For Extended Temperature CS must be brought low for a minimum of 500 ns (t_{CS})** between consecutive instruction cycles.
6. **This parameter is periodically sampled and not 100% tested.**

Figure 2 : Synchronous Data Timing

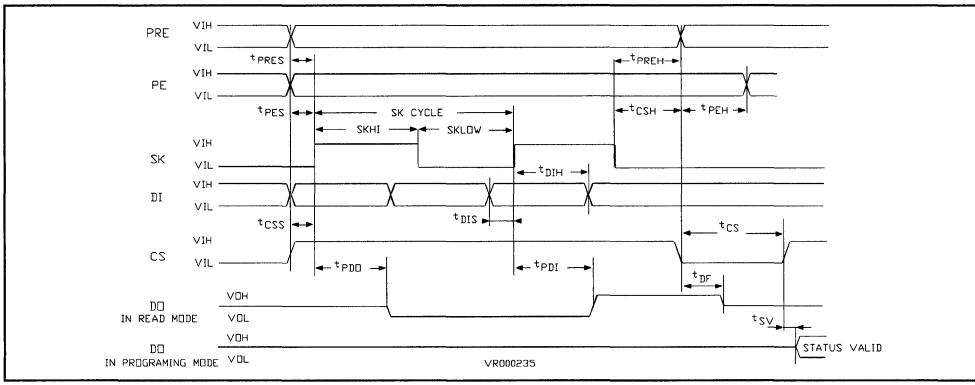


Figure 3 : READ

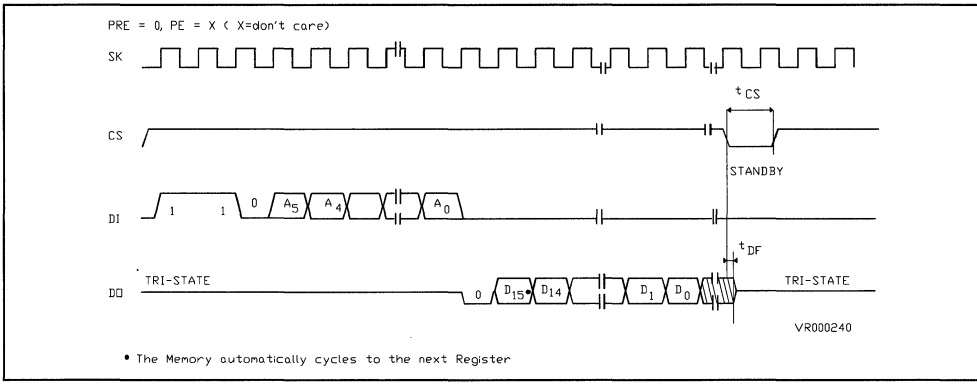


Figure 4 : WEN

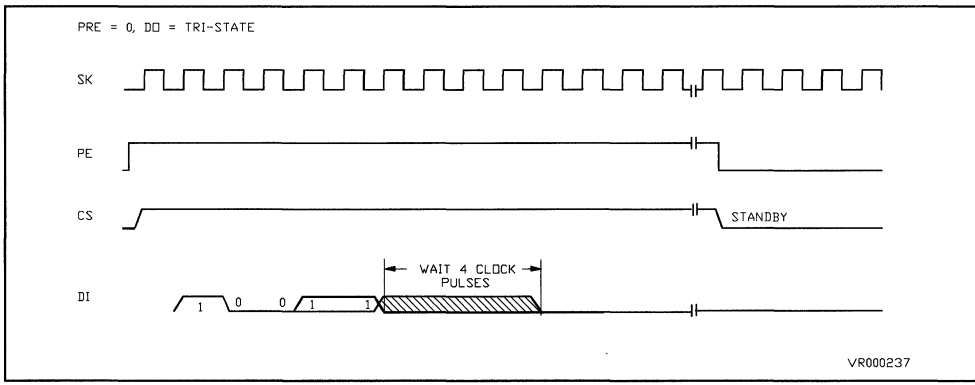


Figure 5 : WDS

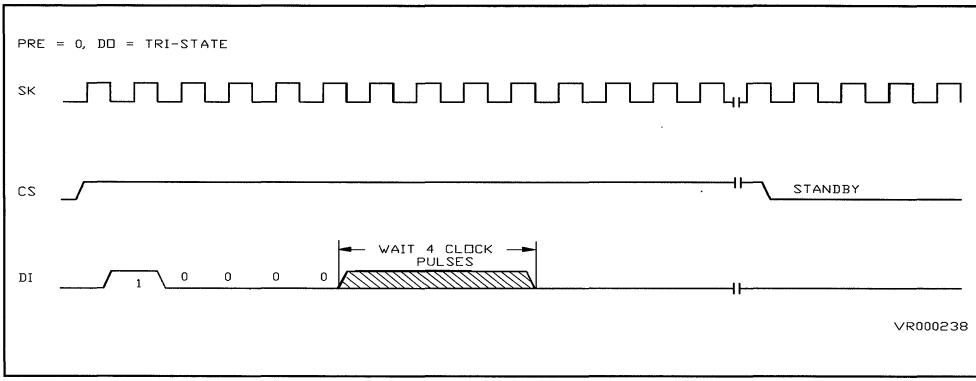


Figure 6 : WRITE

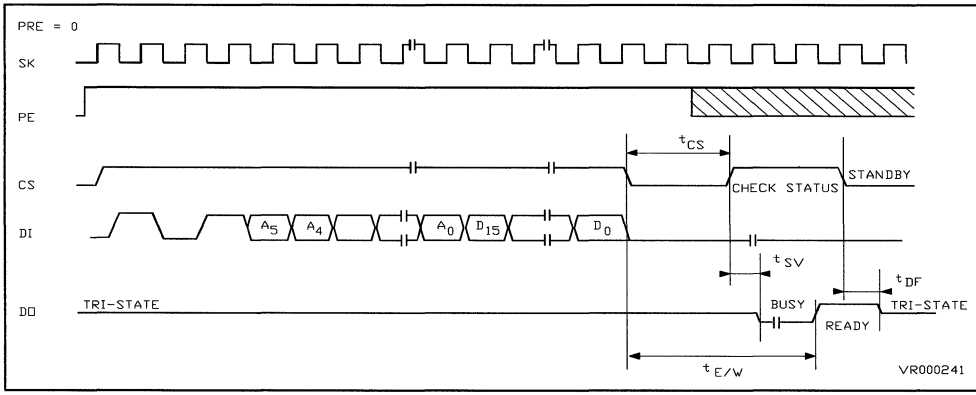


Figure 7 : PAWRITE

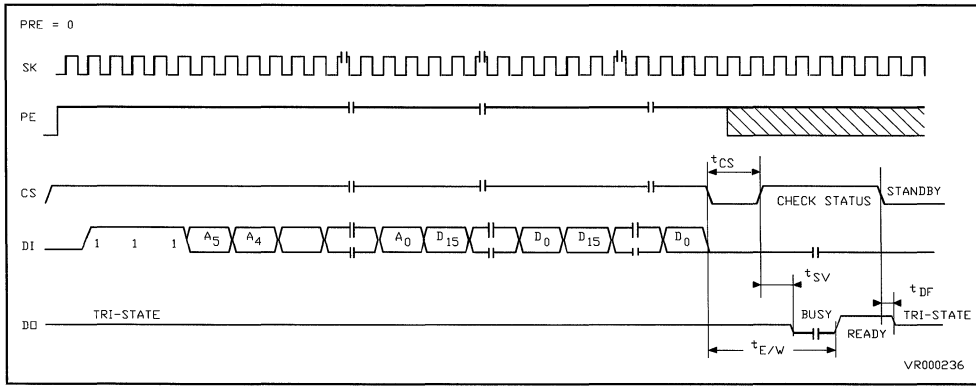


Figure 8 : PRDS

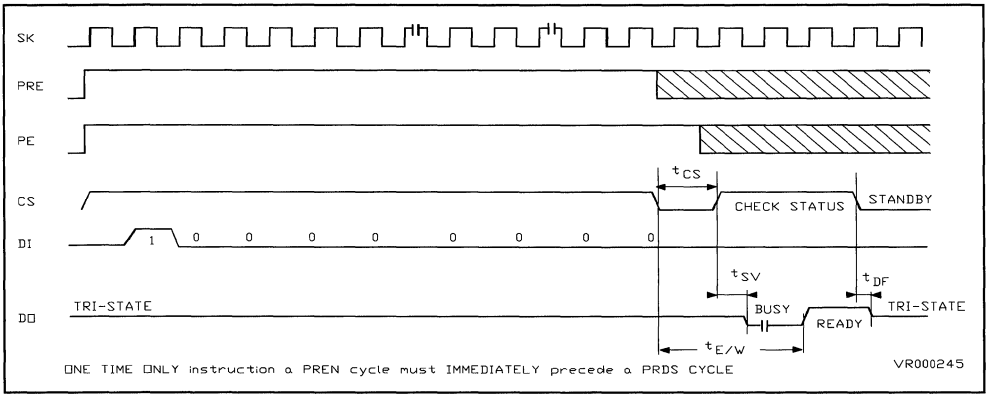


Figure 9 : WRALL

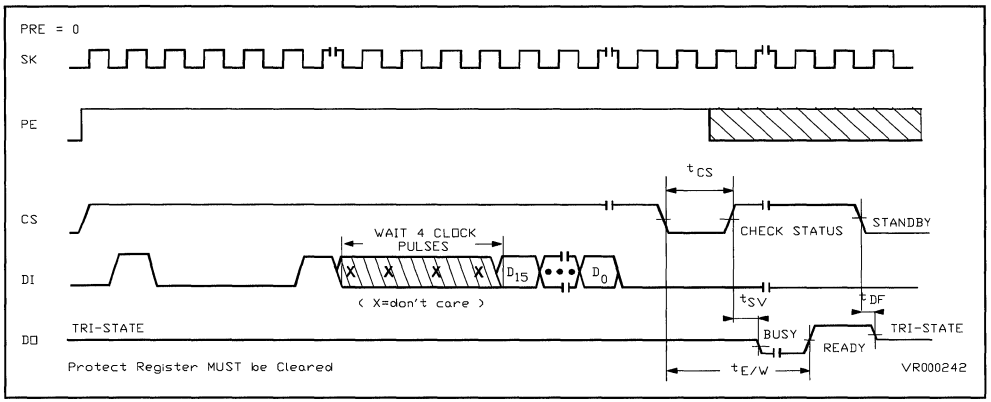


Figure 10 : PRREAD

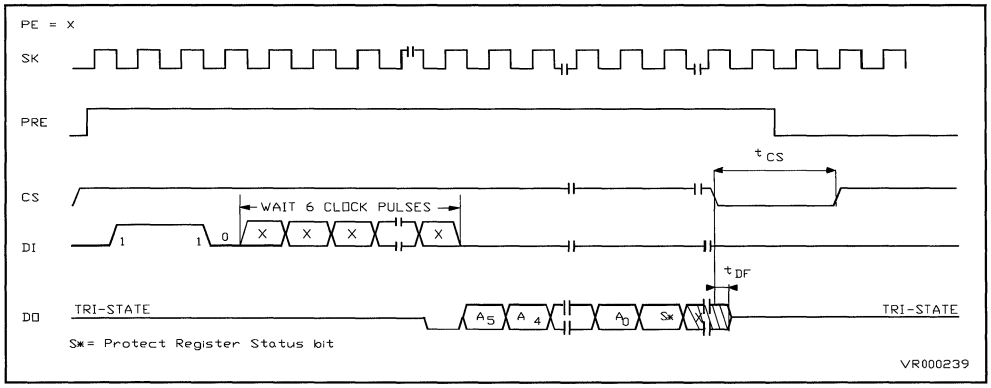


Figure 11 : PREN

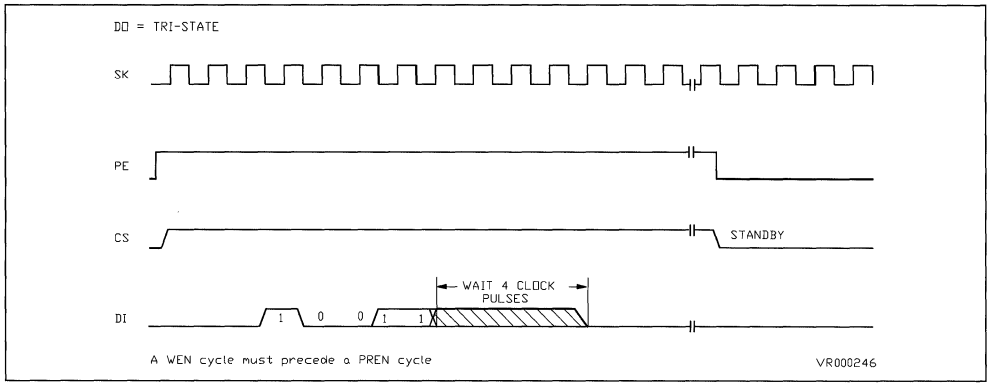


Figure 12 : PR CLEAR

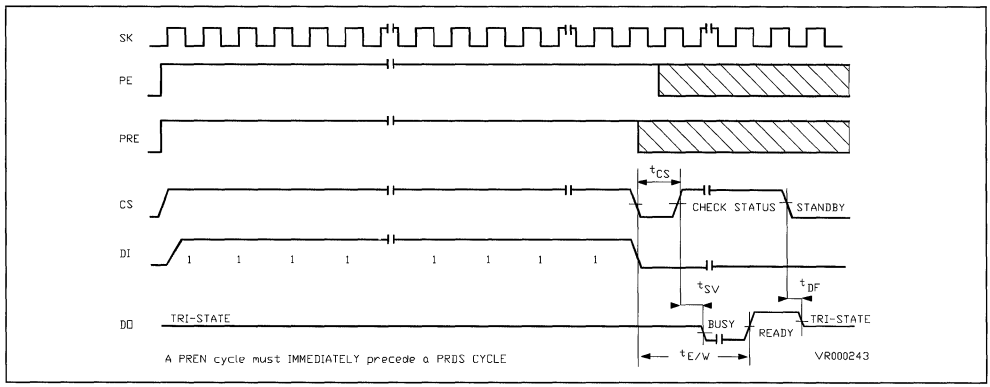
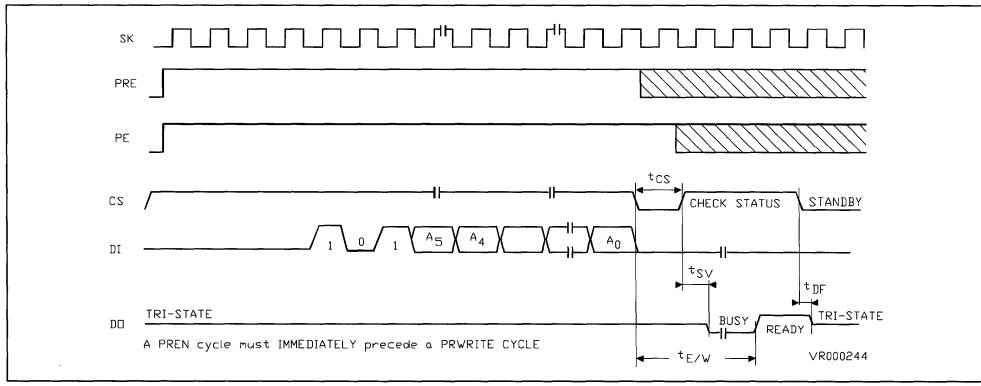


Figure 13 : PR WRITE

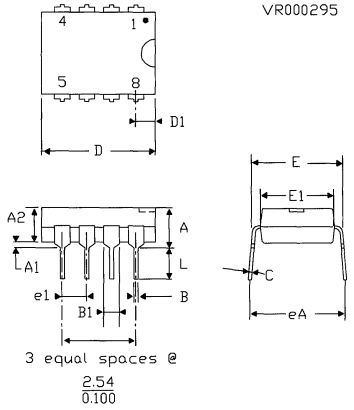


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST93CS47B1	Dual-in-line	0°C to 70°C	2.5V to 5.5V
ST93CS47M1	SO 8		
ST93CS47B6	Dual-in-line	-40°C to 85°C	
ST93CS47M6	SO 8		
ST93CS47B3	Dual-in-line	-40°C to 125°C	
ST93CS47M3	SO 8		

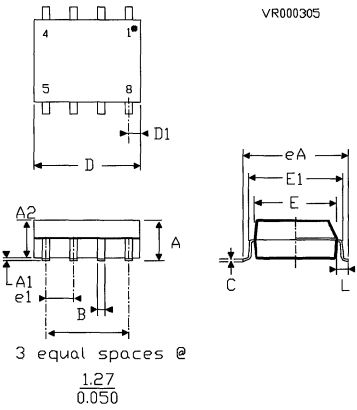
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

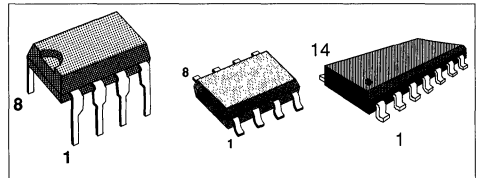
PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

2 K BITS (128 x 16) SERIAL ACCESS CMOS EEPROM MEMORY

- USER DEFINED SIZE OF A MEMORY SECTION PROTECTED AGAINST WRITE.
- WORD AND PAGE WRITE MODES.
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- TYPICAL : OVER 1 000 000 ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- SINGLE POWER SUPPLY IN ALL MODES 5V ±10 %
- SELF TIMED PROGRAMMING CYCLE WITH AUTOERASE
- READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SEQUENTIAL REGISTER READ.



PDIP8 PSO8 PSO14

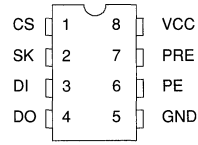
(Ordering information at the end of the datasheet)

PIN NAMES

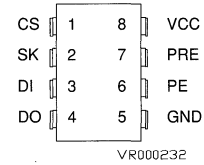
CS	Chip Select
SK	Serial Data Clock
D_I	Serial Data Input
D_O	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply
NC	Not Connected

PIN CONNECTION

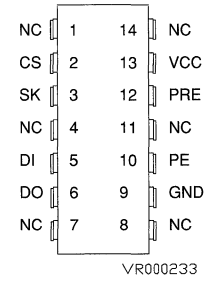
Dual-in-line Package (B) - top view



SO Package (M) - top view



SO Package (ML) - top view



DESCRIPTION

The ST93CS56 is a 2048 bits non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology.

It is an external memory accessed via a simple serial interface.

The 2K bits memory capacity is divided in 128 registers of 16 bits each. A special feature of this device allows the user to protect data against any modification in "N" register ($0 \leq N \leq 128$). Since these N registers are following each other, there is no other need to protect them than programming the address of the first register to be protected into specific on chip register called the "memory protect register".

It is also possible to protect permanently the data of these N registers by using a one time only instruction (PRDS) after wich the address in the protect register cannot be altered.
Thereafter, all attemps to alter data in a register whose address is equal to or greater than the address stored in the "protected register" will be aborted.
The "read" instruction loads the address of the first register to be read in to an 8 bits address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address it is possible, if the "CS" is held high, to produce a serial data stream. In that case the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 2048 bits. Thus the ST93CS56 can be viewed as a non volatile shift register. In a programming mode the ST93CS56 do not require an erase cycle prior to the write instructions. All programming cycles are completely self-timed for simplified operations. The Ready/Busy status of the shift is available on the "D_O" pin if "CS" is brought "high" following the initiation of "Write" cycle. The standard "Write" cycle allows to write 16 bits at a time into one of the 128 data registers. (If the address of the register to be written is less than the address of " Protect Register")
Another write instruction :"PAWRITE" (parallel write) makes possible to write up to 4 words of 16 bits each as the same time. The design of the ST93CS56 and the processing with the technology yields to typical endurance over 1 million cycles and data retention greater than 10 years after.

FUNCTIONAL DESCRIPTION :

The ST93CS56 has 11 instructions described in the table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence.
The next 2 bits carry the OP code and the following 8 bits the address for the registers selection. Note that the first address bit A7 is a "don't care" for this 2K memory.

***Read (READ) :**

The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the sellected memory register into a 16 bits serial outshift register. A dummy bit (logical 0) precedes the 16 bits data output string. An ouput data changes are initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits are clocked out. Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode the dummy bit is suppressed and continuous string of data is obtained.

*** Write Enable (WEN) :**

When V_{CC} is applied to a part, it powers up in the write Disable (WDS) state. Therefore all programming modes must be preceded by Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled untill a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

*** Write (WRITE) :**[Note 1]

The write instruction is followed by 16 bits of data to be written into the specified address. After the less bit of the data is put on the data- in "DI" pin , CS must be brought low before the next rising edge of the SK Clock. This following edge of CS initiates the selftimed programming cycle. The PE pin MUST be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction, the PE pin becomes a "Don't care". The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}".
D_O = logical "0" indicates that programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction has been written with data pattern specified in the instruction and the part is ready for another instruction.

*** Parallel Write (PAWRITE) : Note 1**

The PAWRITE instruction is followed by up to 4 Words of 16 bits of data, to be written starting from the specified address. after the last bit of data (D_O) is put on the data-in (D_I) pin, CS must be brought low before the next rising edge SK clock. This falling edge of the CS initiates the self-timed programming cycle. The pin must be held "high" while loading the write instruction, however, after loading the write PE pin becomes a "don't care".

The D_O pin indicates the Ready/Busy status Chip if "CS" is brought high after a minimum of "T_{CS}". D_O = logical "0" indicates that programming is still in progress. D_O = Logical "1" indicates that the register(s) specified in the instruction as been written with the data pattern specified in the instruction and the part is ready for another instruction.

Note that only the 5 address bits A_6 to A_2 will be compared with protect register content, and the PAWRITE operation will be aborted if (A_6, A_5, A_4, A_3, A_2) ≥ (A_6, A_5, A_4, A_3, A_2) stored in the protect register. Note also that, after the reciept of each data word, the 2 low order address bit (A_1, A_0) are internally incremented by one whereas, the high order five bits of the address remain constant. Therefore in order to avoid that the address rolls over and overwrite the written data, the user must take care in the software, that in the PAWRITE mode the final word address has the same five high order bits than the initial transmitted address.

* Write All (WRALL) : Note 1

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with a data pattern specified in the instruction. Like the write instruction the PE pin MUST be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}"

Note 1 : For any programming modes, the "1" status bit on the D_O pin will disappear as soon as the start bit of a new instruction is presented on the D_I pin.

*** Write Disable (WDS) :**

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of the both the WEN and WDS Instructions.

*Protect Register Read (PRREAD)

Prelimary note : Since the protect register content can be the same after a PRWRITE with the "111111" address and after a PRCLEAR instruction, a specific bit is added in the protect register in order to identify the status of the protect register. If the protect register has been cleared this status bit is set to "1" else it is set to "0".

The protect register Read (PRREAD) instruction outputs on the DO pin the address stored in the "protect register" and the "protect register status bit".

The PRE pin MUST be held "high" while loading the instruction. Following the PRREAD instruction the 8 bit address stored in the memory "protect register" and the "protect register status bit" are transfered to the serial-out shift register. Note that the "protect register status bit" immediately follows the 8 bit address string and that, as in the READ mode, a dummy bit (logical 0) precedes this 9 bits string.

*Protect Register Enable (PREN)

The protect register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE and PRDS modes. Before the PREN mode can be ENTERED. the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins MUST be held "high" while loading the instruction.

*Protect Register Clear (PRCLEAR)

The protect register clear (PRCLEAR) instruction clears the address stored in the protect register and therefore, enables all registers for the WRITE and WRALL instruction. The PRE and PE pins must be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRCLEAR instruction.

***Protect Register Write (PRWRITE):**
The protect register write (PRWRITE) instruction is used to write into the protect register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the protect register are protected from the write operation.
The PRE and PE pins must be held "high" while loading the instruction. However, after loading the PRWRITE instruction the PRE and PE pins become "don't care".
Note that a PREN instruction must immediately precede a PRWRITE instruction.

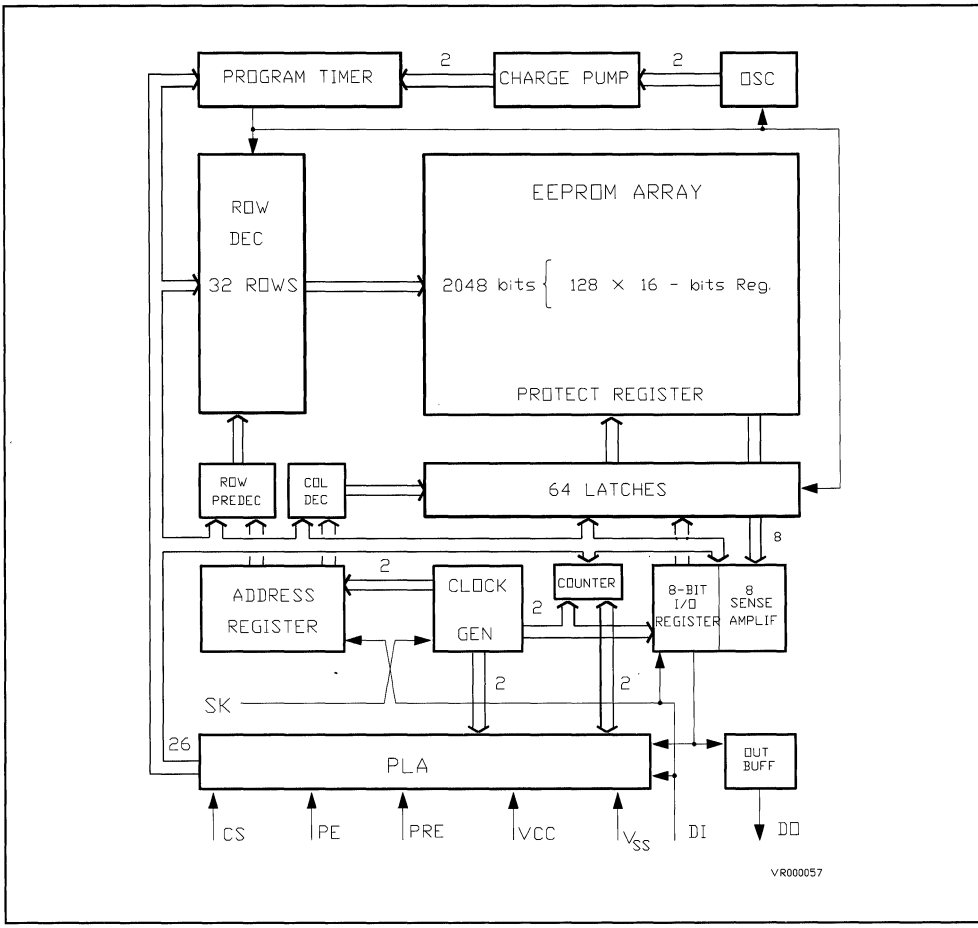
Since, as in the WRITE mode, an autoerase is performed there is no need that a PRCLEAR operation precedes a PRWRITE instruction.

*** Protect Register Disable (PRDS):**
The protect register Disable (PRDS) instruction is a one time only instruction which renders the protect register unalterable in the future. Therefore, the specified registers become PERMANENTLY protected against data changes. As in the PRWRITE instruction the PRE and PE pins must be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".
Note that a PREN instruction must immediately precede a PRDS instruction.

INSTRUCTION SET INSTRUCTION FOR ST93CS56

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	PRE	PE	COMMENTS
READ	1	10	A_7-A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_7-A_0	D_{15}-D_0	0	1	Writes register if address is unprotected.
PAWRITE	1	11	A_7-A_0	D_{15}-D_0	0	1	Writes n registers (n≤4) if addresses are unprotected.
				n x (n ≤ 4)			
WRALL	1	00	01XXXXXX	D_{15}-D_0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from Write.
PRWRITE	1	01	A_7-A_0		1	1	Programs address into protect Register. Thereafter, memory address ≥ the address in protect register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after wich the address in the Protect Register cannot be altered.

Figure 1 : ST93CS56 Block Diagram



ABSOLUTE MAXIMUM RATING (note 1)

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	-65 to +150	°C
All Input or Output Voltages Relative to GND	+6.5 to -0.3	V
Lead Temperature	+300	°C
ESD rating	2000	V

CAPACITANCE (note 6) TA = 25°C, f = 1 MHz

SYMBOL	TEST	TYP	MAX	MIN
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC TEST CONDITIONS

Ouput Load . . . . . 1 TTL GATE and C_L = 100 pF

Input Pulse Levels . . . . . .0.4V to 2.4V

Timing Measurement Reference Level :

Input . . . . . .1V and 2V

Output . . . . . 0.8V and 2V

OPERATING CONDITIONS

Ambient Operating Temperature

ST93C56-1 _____ 0°C 70°C

ST93C56-6 _____ -40°C to + 85°C

ST93C56-3 _____ -40°C to +125°C

-= B _____ Dual-in-line Package

-= M _____ SO8 Package

- = ML _____ SO14 Package

Positive Power Supply _____ 4.5V to 5.5V

DC & AC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10 % unless otherwise specified)

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
I_{CC1}	Operating Current	ST93CS56-1	CS=V_{IH}, SK=1MHz		2	
	CMOS Input Levels	ST93CS56-6	SK=0.5 MHz		2	mA
		ST93CS56-3	SK=0.5 MHz		2	
I_{CC2}	Operating Current	ST93CS56-1	CS=V_{IH}, SK=1MHz		3	
	TTL Input Levels	ST93CS56-6	SK=0.5 MHz		3	mA
		ST93CS56-3	SK=0.5 MHz		4	
I_{CC3}	Standby Current	ST93CS56-1	CS = 0V		50	
		ST93CS56-6			100	µA
		ST93CS56-3			100	
I_{IL}	Input Leakage	ST93CS56-1	V_{IN} = 0V to V_{CC}	-2.5	2.5	
		ST93CS56-3		-10	10	µA
		ST93CS56-6		-10	10	µA
I_{OL}	Output Leakage	ST93CS56-1	V_{OUT} = 0V to V_{CC}	-2.5	2.5	
		ST93CS56-3		-10	10	µA
		ST93CS56-6		-10	10	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	VCC+1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -10 µA	V_{CC}-0.2		V
f_{SK}	SK Clock Frequecy	ST93CS56-1		0	1	
		ST93CS56-3		0	0.5	MHz
		ST93CS56-6		0	0.5	
t_{SKH}	SK High Time	ST93CS56-1	(Note 2)	250		
		ST93CS56-3	(Note 3)	500		ns
		ST93CS56-6	(Note 3)	500		
t_{SKL}	SK Low Time	ST93CS56-1	(Note 2)	250		
		ST93CS56-3	(Note 3)	500		ns
		ST93CS56-6	(Note 3)	500		
t_{CS}	Minimum CS Low Time	ST93CS56-1	(Note 4)	250		
		ST93CS56-3	(Note 5)	500		ns
		ST93CS56-6	(Note 5)	500		
t_{CSS}	CS Set-up Time	ST93CS56-1	Relative to SK	50		
		ST93CS56-3		100		ns
		ST93CS56-6		100		
t_{PRES}	PRE Set-up Time	ST93CS56-1	Relative to SK	50		
		ST93CS56-3		100		ns
		ST93CS56-6		100		

DC & AC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10 %) continued

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
^tPES	PE Set-up TIme	ST93CS56-1	Relative to SK	50		
		ST93CS56-3		100		
		ST93CS56-6		100		
^tDIS	DI Set-up Time	ST93CS56-1	Relative to SK	100		
		ST93CS56-3		200		
		ST93CS56-6		200		
^tCSH	CS Hold Time		Relative to SK	0		
^tPEH	PE Hold Time	ST93CS56-1	Relative to CS	250		
		ST93CS56-3	Relative to CS	500		
		ST93CS56-6	Relative to CS	500		
^tPREH	PRE Hold Time		Relative to SK	0		ns
^tDIH	DI Hold Time	ST93CS56-1	Relative to SK	100		
		ST93CS56-3		200		
		ST93CS56-6		200		
$^tPD1$	Output Delay to "1"	ST93CS56-1	AC TEST		500	
		ST93CS56-3			1000	
		ST93CS56-6			1000	
$^tPD0$	Output Delay to "0"	ST93CS56-1	AC TEST		500	
		ST93CS56-3			1000	
		ST93CS56-6			1000	
^tSV	CS to Status Valid	ST93CS56-1	AC TEST		500	
		ST93CS56-3			1000	
		ST93CS56-6			1000	
^tDF	CS to DO in TRI STATE	ST93CS56-1	AC TEST		100	
		ST93CS56-3	CS = V_{IL}		200	
		ST93CS56-6			200	
^tWP	Write Cycle Time				10	ms
	Endurance		Typical : 1 000 000			cycles

NOTE : 1.Stress above those listed under "absolute maximum ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The Sk frequency specification for commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example if tSKL = 250 ns then the maximum t_{SKH} = 750 ns in order to meet the SK frequency specification.
3. The Sk frequency specification for Extended Temperature specifies a a minimum SK clock period of 2 microsecond, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 microsecond. For example if tSKL = 500 ns then the maximum t_{SKH} = 1.5 ns in order to meet the SK frequency specification.
4. For commercial parts CS must be brought low for a minimum of 250 ns (tCS) between consecutive instruction cycles.
5. For Extended Temperature CS must be brought low for a minimum of 500 ns (tCS) between consecutive instruction cycles.
6. This parameter is periodically sampled and not 100% tested.

Figure 2 : Synchronous Data Timing

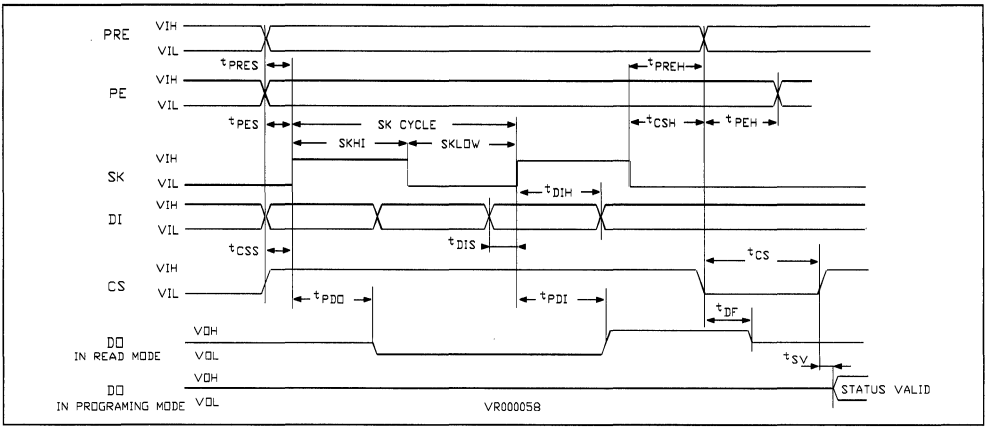


Figure 3 : READ

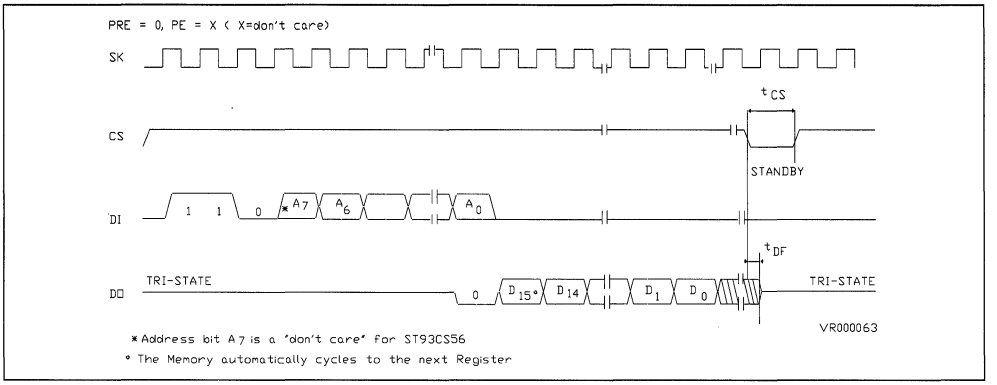


Figure 4 : WEN

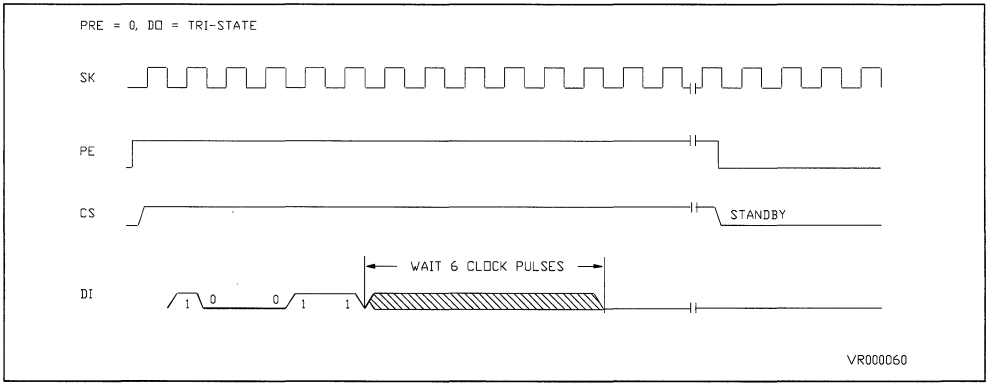


Figure 5 : WDS

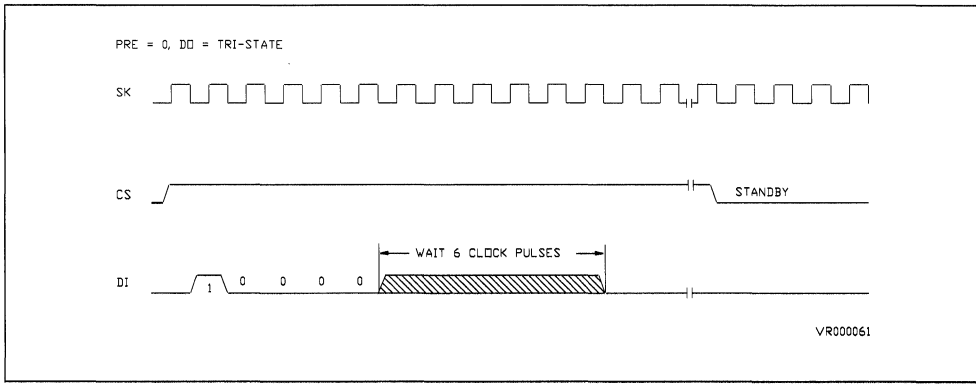


Figure 6 : WRITE

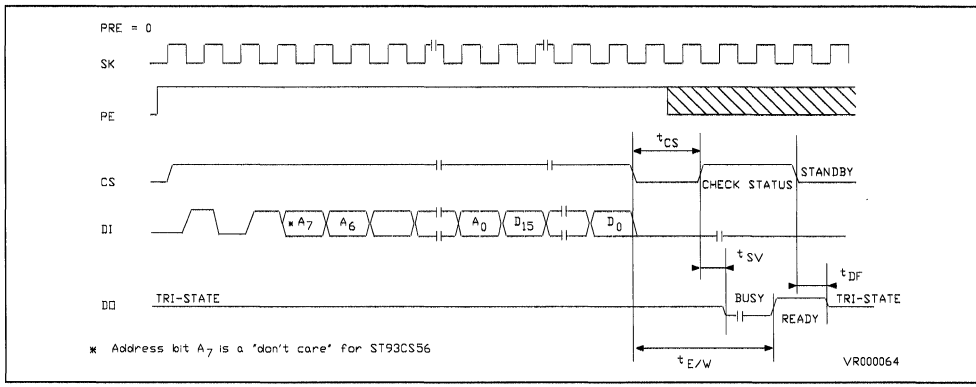


Figure 7 : PAWRITE

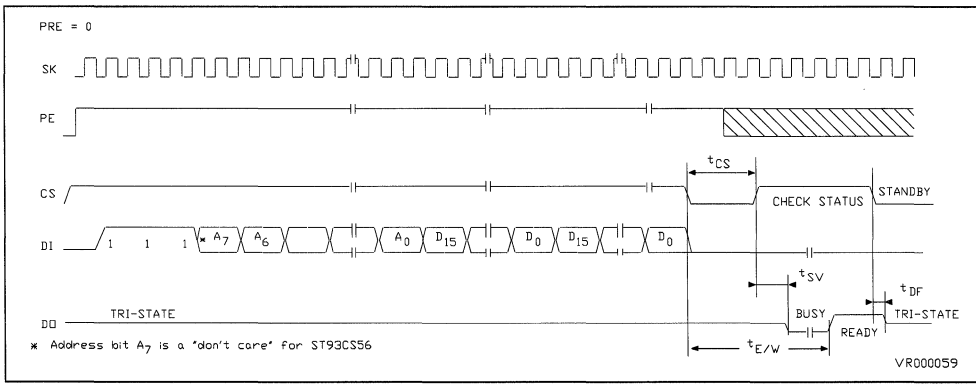


Figure 8 : PRDS

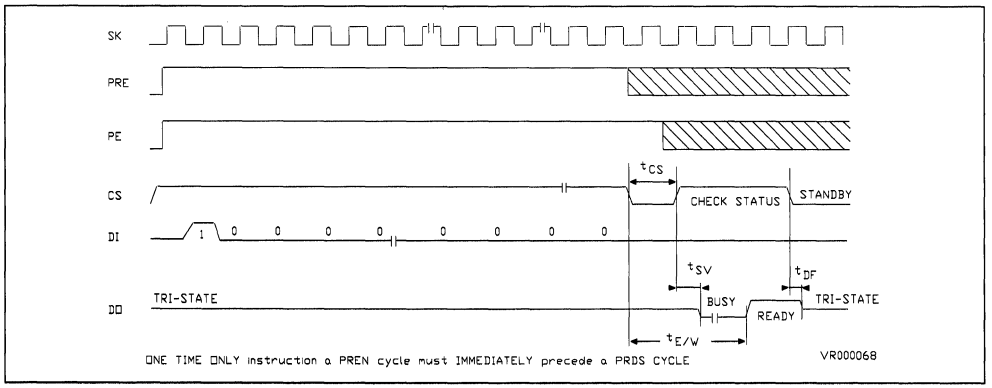


Figure 9 : WRALL

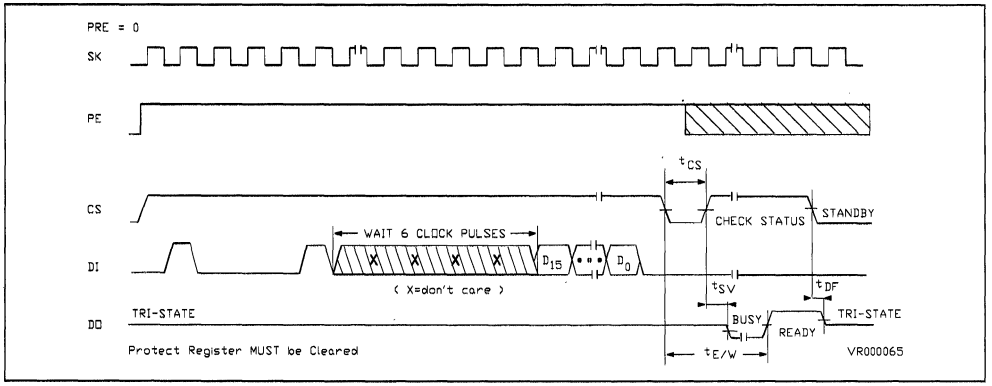


Figure 10 : PRREAD

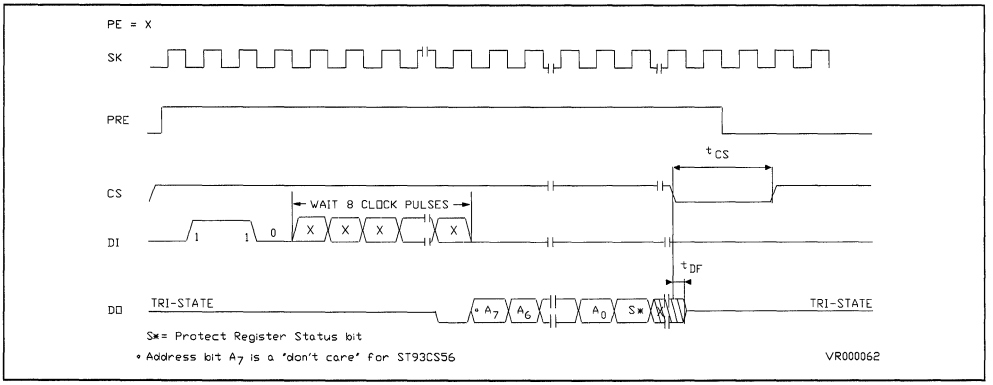


Figure 11 : PREN

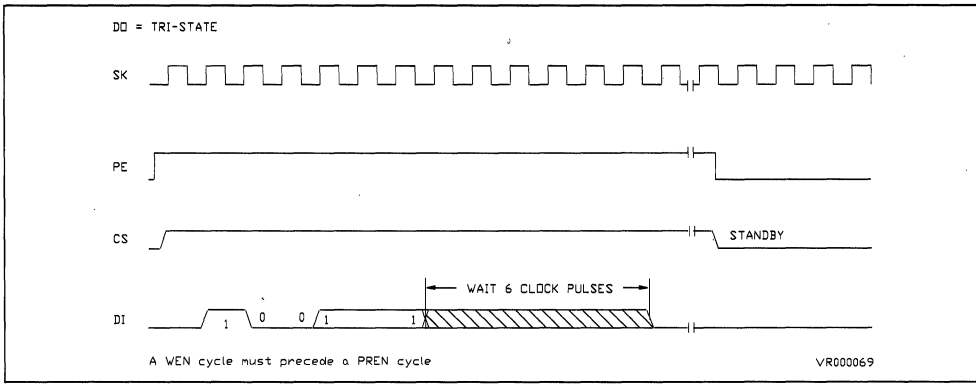


Figure 12 : PR CLEAR

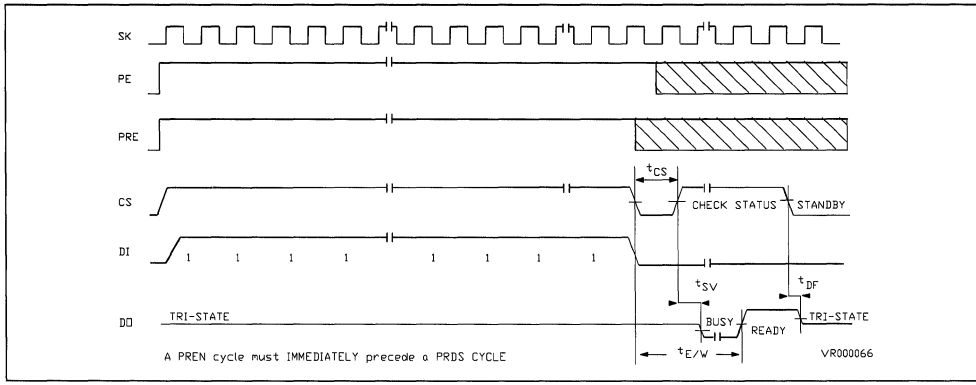
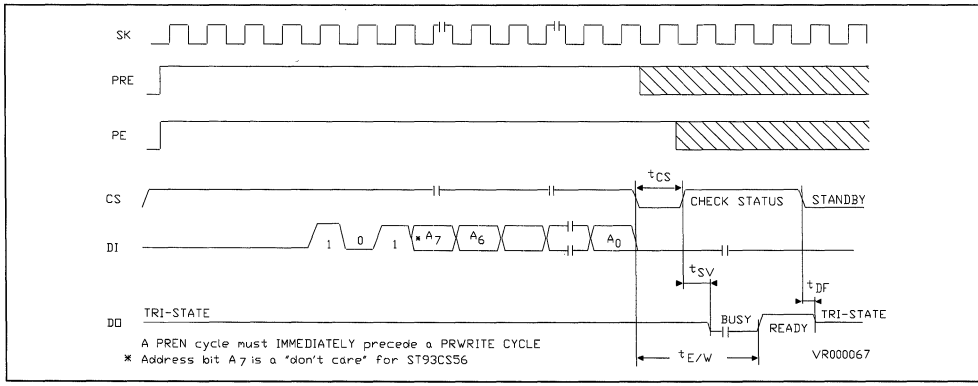


Figure 13 : PR WRITE

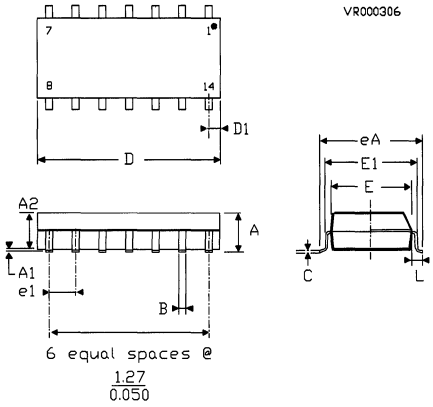


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST93CS56B1	Dual-in-line	0°C to 70°C	4.5V to 5.5V
ST93CS56M1	SO 8		
ST93CS56ML1	SO 14		
ST93CS56B6	Dual-in-line	-40°C to 85°C	
ST93CS56M6	SO 8		
ST93CS56ML6	SO 14		
ST93CS56B3	Dual-in-line	-40°C to 125°C	
ST93CS56M3	SO 8		
ST93CS56ML3	SO 14		

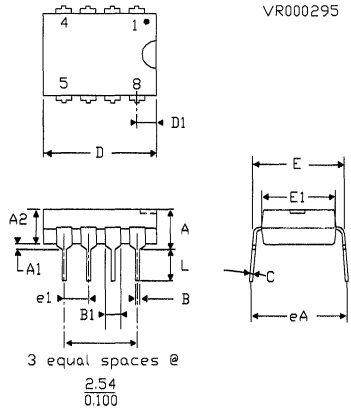
PACKAGE MECHANICAL DATA

PSO14 PACKAGE (ML)



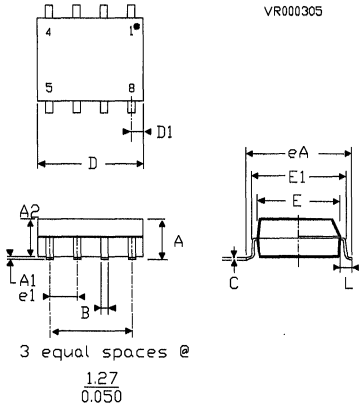
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10		0.20	.004		.008
A2			1.60			0.063
B	0.35		0.46	.014		.018
C	0.19		0.25	.007		.010
D	8.55		8.75	.337		.344
D1			0.68			.027
E	3.80		4.00	.150		.157
E1	4.60		5.30	.181		.209
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.50		1.27	.020		.050

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

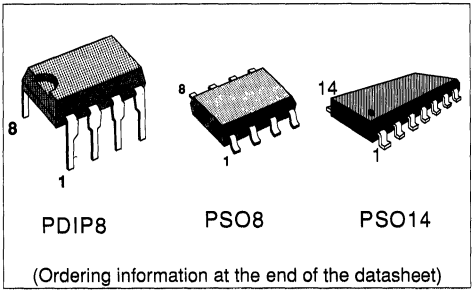
PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

2 K BITS (128 x16) SERIAL ACCESS CMOS EEPROM MEMORY

- 2.5V - 5.5V SINGLE POWER SUPPLY IN ALL MODES
- USER DEFINED SIZE OF A MEMORY SECTION PROTECTED AGAINST WRITE.
- WORD AND PAGE WRITE MODES.
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- TYPICAL : OVER 1 000 000 ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- SINGLE POWER SUPPLY IN ALL MODES 5V ±10 %
- SELF TIMED PROGRAMMING CYCLE WITH AUTOERASE
- READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SEQUENTIAL REGISTER READ.



PDIP8 PSO8 PSO14

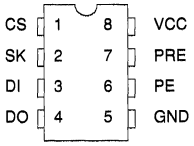
(Ordering information at the end of the datasheet)

PIN NAMES

CS	Chip Select
SK	Serial Data Clock
D_I	Serial Data Input
D_O	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply
NC	Not Connected

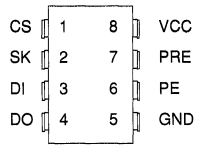
PIN CONNECTION

PDIP8 Package (B) - top view



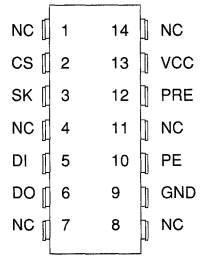
VR000224

PSO8 Package (M) - top view



VR000232

PSO14 Package (ML) - top view



VR000233

DESCRIPTION

The ST93CS57 is a 2048 bits non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology.

It is an external memory accessed via a simple serial interface.

The 2K bits memory capacity is divided in 128 registers of 16 bits each. A special feature of this device allows the user to protect data against any modification in "N" register ($0 \leq N \leq 128$). Since these N registers are following each other, there is no other need to protect them than programming the address of the first register to be protected into specific on chip register called the "memory protect register".

It is also possible to protect permanently the data of these N registers by using a one time only instruction (PRDS) after wich the address in the protect register cannot be altered.
Thereafter, all attemps to alter data in a register whose address is equal to or greater than the address stored in the "protected register" will be aborted.
The "read" instruction loads the address of the first register to be read in to an 8 bits address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address it is possible, if the "CS" is held high, to produce a serial data stream. In that case the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 2048 bits. Thus the ST93CS57 can be viewed as a non volatile shift register. In a programming mode the ST93CS57 do not require an erase cycle prior to the write instructions. All programming cycles are completely self-timed for simplified operations. The Ready/Busy status of the shift is available on the "D_O" pin if "CS" is brought "high" following the initiation of "Write" cycle. The standard "Write" cycle allows to write 16 bits at a time into one of the 128 data registers. (If the address of the register to be written is less than the address of " Protect Register")
Another write instruction :"PAWRITE" (parallel write) makes possible to write up to 4 words of 16 bits each as the same time. The design of the ST93CS57 and the processing with the technology yields to typical endurance over 1 million cycles and data retention greater than 10 years after.

FUNCTIONAL DESCRIPTION :
The ST93CS57 has 11 instructions described in the table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence.
The next 2 bits carry the OP code and the following 8 bits the address for the registers selection. Note that the first address bit A7 is a "don't care" for this 2K memory.

***Read (READ) :**
The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the sellected memory register into a 16 bits serial outshift register. A dummy bit (logical 0) precedes the 16 bits data output string. An ouput data changes are initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits are clocked out. Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode the dummy bit is suppressed and continuous string of data is obtained.

*** Write Enable (WEN) :**
When V_{CC} is applied to a part, it powers up in the write Disable (WDS) state. Therefore all programming modes must be preceded by Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled untill a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

*** Write (WRITE) :**[Note 1]
The write instruction is followed by 16 bits of data to be written into the specified address. After the less bit of the data is put on the data- in "DI" pin , CS must be brought low before the next rising edge of the SK Clock. This following edge of CS initiates the selftimed programming cycle. The PE pin MUST be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction, the PE pin becomes a "Don't care". The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}".
D_O = logical "0" indicates that programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction has been written with data pattern specified in the instruction and the part is ready for another instruction.

*** Parallel Write (PAWRITE) :** Note 1

The PAWRITE instruction is followed by up to 4 Words of 16 bits of data, to be written starting from the specified address. after the last bit of data (D_O) is put on the data-in (D_I) pin, CS must be brought low before the next rising edge SK clock. This falling edge of the CS initiates the self-timed programming cycle. The pin must be held "high" while loading the write instruction, however, after loading the write PE pin becomes a "don't care".

The D_O pin indicates the Ready/Busy status Chip if "CS" is brought high after a minimum of "T_{CS}". D_O = logical "0" indicates that programming is still in progress. D_O = Logical "1" indicates that the register(s) specified in the instruction as been written with the data pattern specified in the instruction and the part is ready for another instruction.

Note that only the 5 address bits A_6 to A_2 will be compared with protect register content, and the PAWRITE operation will be aborted if (A_6, A_5, A_4, A_3, A_2) ≥ (A_6, A_5, A_4, A_3, A_2) stored in the protect register. Note also that, after the reciept of each data word, the 2 low order address bit (A_1, A_0) are internally incremented by one whereas, the high order five bits of the address remain constant. Therefore in order to avoid that the address rolls over and overwrite the written data, the user must take care in the software, that in the PAWRITE mode the final word address has the same five high order bits than the initial transmitted address.

*** Write All (WRALL) :** Note 1

The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with a data pattern specified in the instruction. Like the write instruction the PE pin MUST be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "T_{CS}"

Note 1 : For any programming modes, the "1" status bit on the D_O pin will disappear as soon as the start bit of a new instruction is presented on the D_I pin.

*** Write Disable (WDS) :**

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of the both the WEN and WDS Instructions.

***Protect Register Read (PRREAD)**

Prelimary note : Since the protect register content can be the same after a PRWRITE with the "111111" address and after a PRCLEAR instruction, a specific bit is added in the protect register in order to identify the status of the protect register. If the protect register has been cleared this status bit is set to "1" else it is set to "0".

The protect register Read (PRREAD) instruction outputs on the DO pin the address stored in the "protect register" and the "protect register status bit".

The PRE pin MUST be held "high" while loading the instruction. Following the PRREAD instruction the 8 bit address stored in the memory "protect register" and the "protect register status bit" are transfered to the serial-out shift register. Note that the "protect register status bit" immediately follows the 8 bit address string and that, as in the READ mode, a dummy bit (logical 0) precedes this 9 bits string.

***Protect Register Enable (PREN)**

The protect register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE and PRDS modes. Before the PREN mode can be ENTERED. the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins MUST be held "high" while loading the instruction.

***Protect Register Clear (PRCLEAR)**

The protect register clear (PRCLEAR) instruction clears the address stored in the protect register and therefore, enables all registers for the WRITE and WRALL instruction. The PRE and PE pins must be held "high" while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must immediately precede a PRCLEAR instruction.

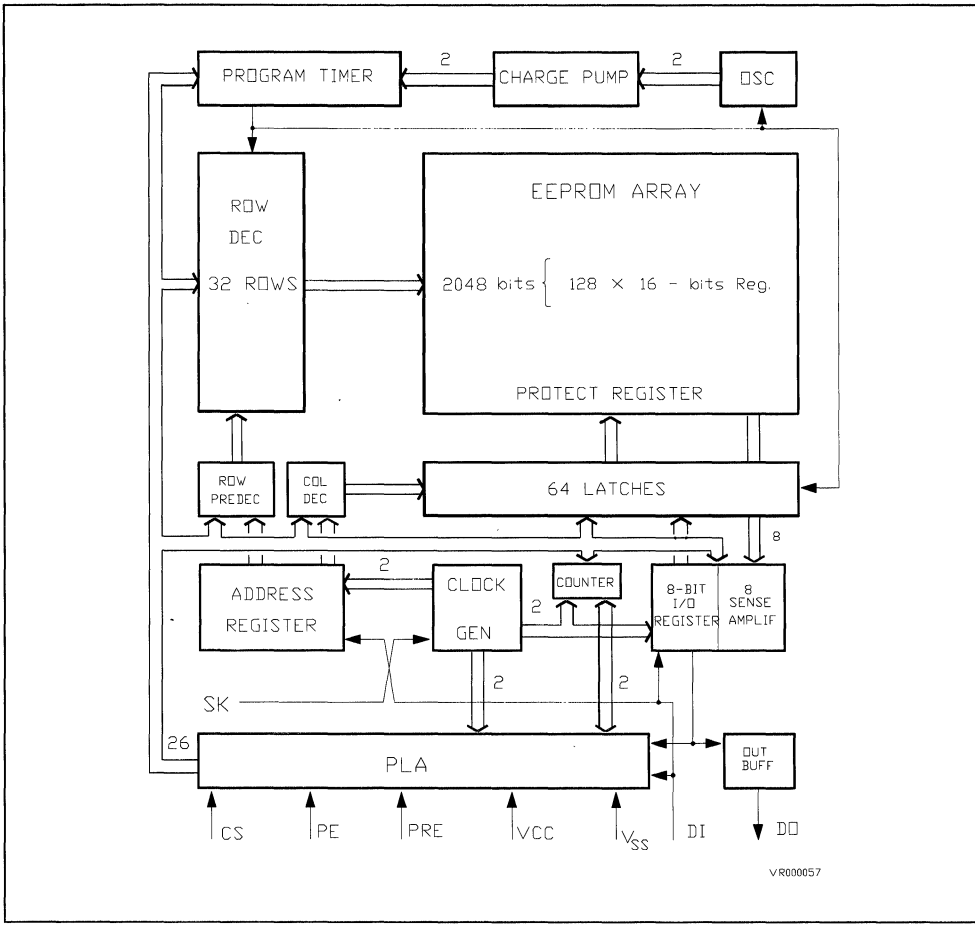
***Protect Register Write (PRWRITE):**
The protect register write (PRWRITE) instruction is used to write into the protect register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the protect register are protected from the write operation.
The PRE and PE pins must be held "high" while loading the instruction. However, after loading the PRWRITE instruction the PRE and PE pins become "don't care".
Note that a PREN instruction must immediately precede a PRWRITE instruction.
Since, as in the WRITE mode, an autoerase is performed there is no need that a PRCLEAR operation precedes a PRWRITE instruction.

*** Protect Register Disable (PRDS):**
The protect register Disable (PRDS) instruction is a one time only instruction which renders the protect register unalterable in the future. Therefore, the specified registers become PERMANENTLY protected against data changes. As in the PRWRITE instruction the PRE and PE pins must be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".
Note that a PREN instruction must immediately precede a PRDS instruction.

INSTRUCTION SET INSTRUCTION FOR ST93CS56

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	PRE	PE	COMMENTS
READ	1	10	A_7-A_0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A_7-A_0	D_{15}-D_0	0	1	Writes register if address is unprotected.
PAWRITE	1	11	A_7-A_0	D_{15}-D_0	0	1	Writes n registers (n≤4) if addresses are unprotected.
				n x (n ≤ 4)			
WRALL	1	00	01XXXXXX	D_{15}-D_0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from Write.
PRWRITE	1	01	A_7-A_0		1	1	Programs address into protect Register. Thereafter, memory address ≥ the address in protect register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after wich the address in the Protect Register cannot be altered.

Figure 1 : ST93CS57 Block Diagram



ABSOLUTE MAXIMUM RATING (note 1)

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	-65 to +150	°C
All Input or Output Voltages Relative to GND	+6.5 to -0.3	V
Lead Temperature	+300	°C
ESD rating	2000	V

CAPACITANCE (note 6) TA = 25°C, f = 1 MHz

SYMBOL	TEST	TYP	MAX	MIN
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC TEST CONDITIONS

Ouput Load . . . . . 1 TTL GATE and C_L = 100 pF

Input Pulse Levels . . . . . .0.4V to 2.4V

Timing Measurement Reference Level :

Input . . . . . .1V and 2V

Output . . . . . 0.8V and 2V

OPERATING CONDITIONS

Ambient Operating Temperature

ST93C57-1 _____ 0°C 70°C

ST93C57-6 _____ -40°C to + 85°C

ST93C57-3 _____ -40°C to +125°C

-= B _____ Dual-in-line Package

-= M _____ SO8 Package

- = ML _____ SO14 Package

Positive Power Supply _____ 2.5V to 5.5V

DC & AC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10 % unless otherwise specified)

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
I_{CC1}	Operating Current	ST93CS57-1	CS=V_{IH}, SK=1MHz		2	
	CMOS Input Levels	ST93CS57-6	SK=0.5 MHz		2	mA
		ST93CS57-3	SK=0.5 MHz		2	
I_{CC2}	Operating Current	ST93CS57-1	CS=V_{IH}, SK=1MHz		3	
	TTL Input Levels	ST93CS57-6	SK=0.5 MHz		3	mA
		ST93CS57-3	SK=0.5 MHz		4	
I_{CC3}	Standby Current	ST93CS57-1	CS = 0V		50	
		ST93CS57-6			100	µA
		ST93CS57-3			100	
I_{IL}	Input Leakage	ST93CS57-1	V_{IN} = 0V to V_{CC}	-2.5	2.5	
		ST93CS57-3		-10	10	µA
		ST93CS57-6		-10	10	µA
I_{OL}	Output Leakage	ST93CS57-1	V_{OUT} = 0V to V_{CC}	-2.5	2.5	
		ST93CS57-3		-10	10	µA
		ST93CS57-6		-10	10	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	VCC+1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = -400 µA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 µA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = -10 µA	V_{CC}-0.2		V
f_{SK}	SK Clock Frequecy	ST93CS57-1		0	1	
		ST93CS57-3		0	0.5	MHz
		ST93CS57-6		0	0.5	
t_{SKH}	SK High Time	ST93CS57-1	(Note 2)	250		
		ST93CS57-3	(Note 3)	500		ns
		ST93CS57-6	(Note 3)	500		
t_{SKL}	SK Low Time	ST93CS57-1	(Note 2)	250		
		ST93CS57-3	(Note 3)	500		ns
		ST93CS57-6	(Note 3)	500		
t_{CS}	Minimum CS Low Time	ST93CS57-1	(Note 4)	250		
		ST93CS57-3	(Note 5)	500		ns
		ST93CS57-6	(Note 5)	500		
t_{CSS}	CS Set-up Time	ST93CS57-1	Relative to SK	50		
		ST93CS57-3		100		ns
		ST93CS57-6		100		
t_{PRES}	PRE Set-up Time	ST93CS57-1	Relative to SK	50		
		ST93CS57-3		100		ns
		ST93CS57-6		100		

DC & AC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10 %) continued

SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
^tPES	PE Set-up TIme	ST93CS57-1	Relative to SK	50		
		ST93CS57-3		100		
		ST93CS57-6		100		
^tDIS	DI Set-up Time	ST93CS57-1	Relative to SK	100		
		ST93CS57-3		200		
		ST93CS57-6		200		
^tCSH	CS Hold Time		Relative to SK	0		
^tPEH	PE Hold Time	ST93CS57-1	Relative to CS	250		
		ST93CS57-3	Relative to CS	500		
		ST93CS57-6	Relative to CS	500		
^tPREH	PRE Hold Time		Relative to SK	0		ns
^tDIH	DI Hold Time	ST93CS57-1	Relative to SK	100		
		ST93CS57-3		200		
		ST93CS57-6		200		
$^tPD1$	Output Delay to "1"	ST93CS57-1	AC TEST		500	
		ST93CS57-3			1000	
		ST93CS57-6			1000	
$^tPD0$	Output Delay to "0"	ST93CS57-1	AC TEST		500	
		ST93CS57-3			1000	
		ST93CS57-6			1000	
^tSV	CS to Status Valid	ST93CS57-1	AC TEST		500	
		ST93CS57-3			1000	
		ST93CS57-6			1000	
^tDF	CS to DO in TRI STATE	ST93CS57-1	AC TEST		100	
		ST93CS57-3	CS = V_{IL}		200	
		ST93CS57-6			200	
^tWP	Write Cycle Time				10	ms
	Endurance		Typical : 1 000 000			cycles

NOTE : 1.Stress above those listed under "absolute maximum ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The Sk frequency specification for commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example if tSKL = 250 ns then the maximum t_{SKH} = 750 ns in order to meet the SK frequency specification.
3. The Sk frequency specification for Extended Temperature specifies a a minimum SK clock period of 2 microsecond, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 microsecond. For example if tSKL = 500 ns then the maximum t_{SKH} = 1.5 ns in order to meet the SK frequency specification.
4. For commercial parts CS must be brought low for a minimum of 250 ns (tCS) between consecutive instruction cycles.
5. For Extended Temperature CS must be brought low for a minimum of 500 ns (tCS) between consecutive instruction cycles.
6. This parameter is periodically sampled and not 100% tested.

Figure 2 : Synchronous Data Timing

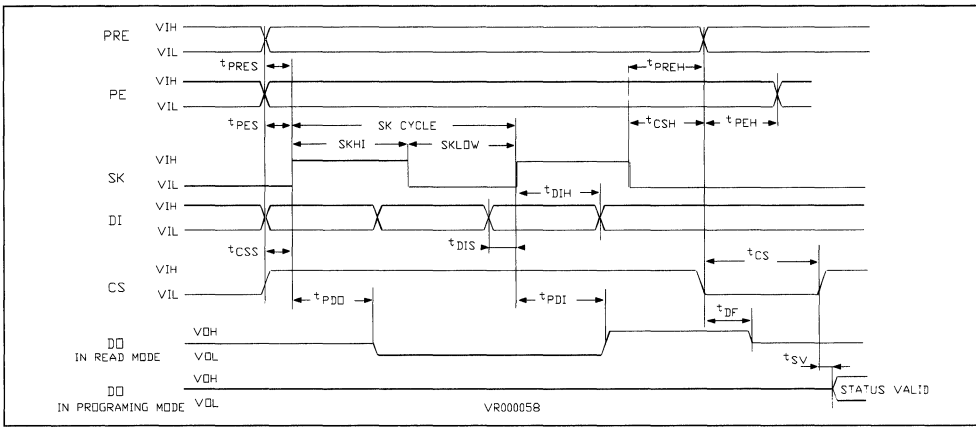


Figure 3 : READ

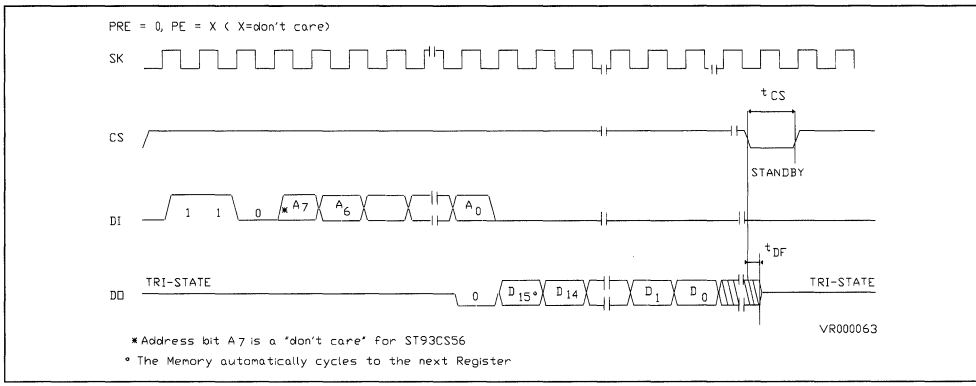


Figure 4 : WEN

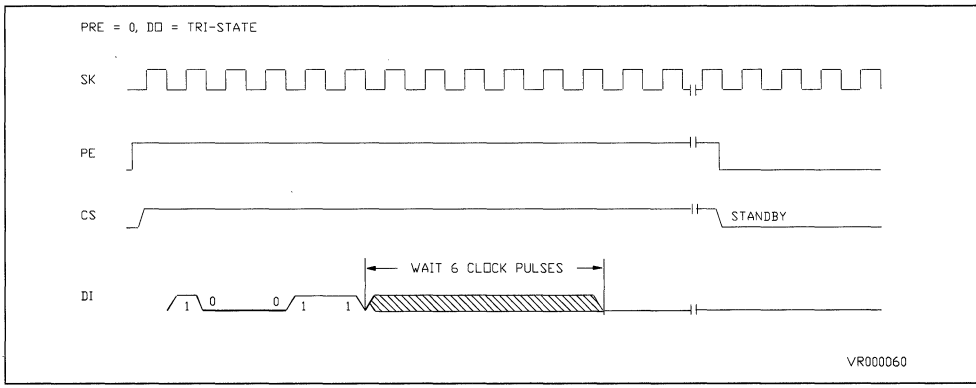


Figure 5 : WDS

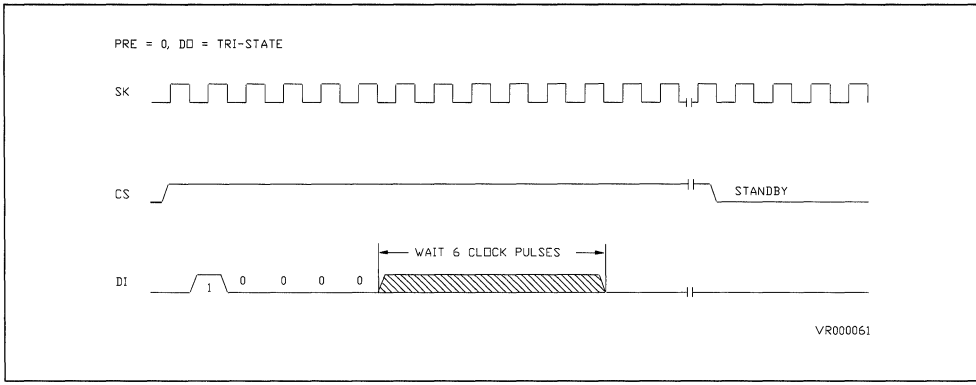


Figure 6 : WRITE

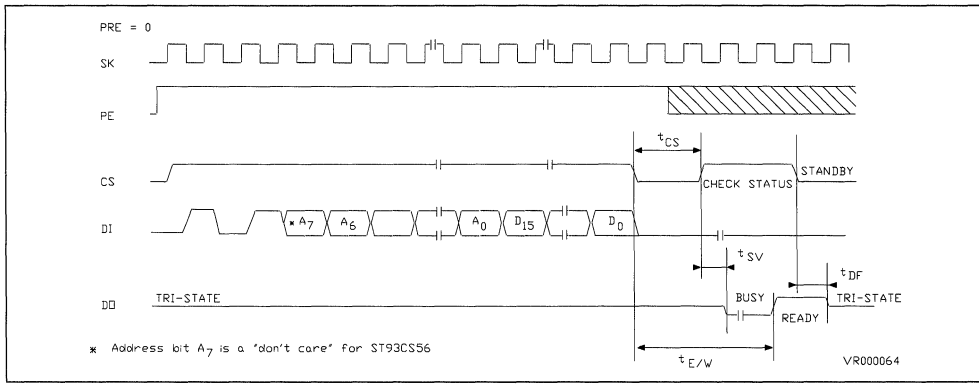


Figure 7 : PAWRITE

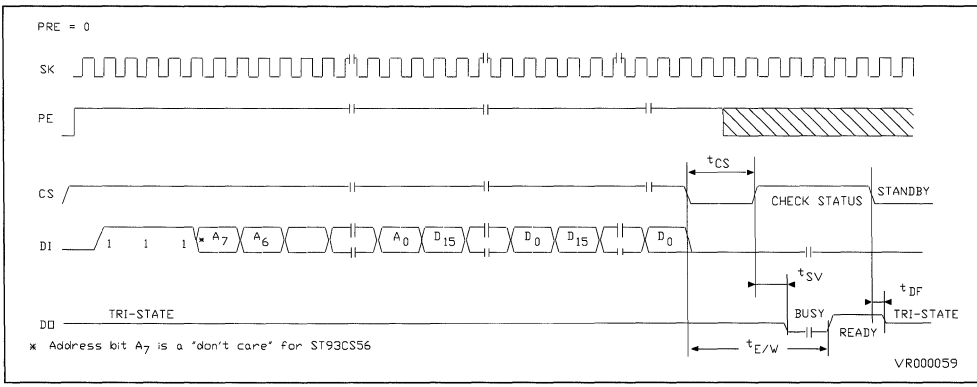


Figure 8 : PRDS

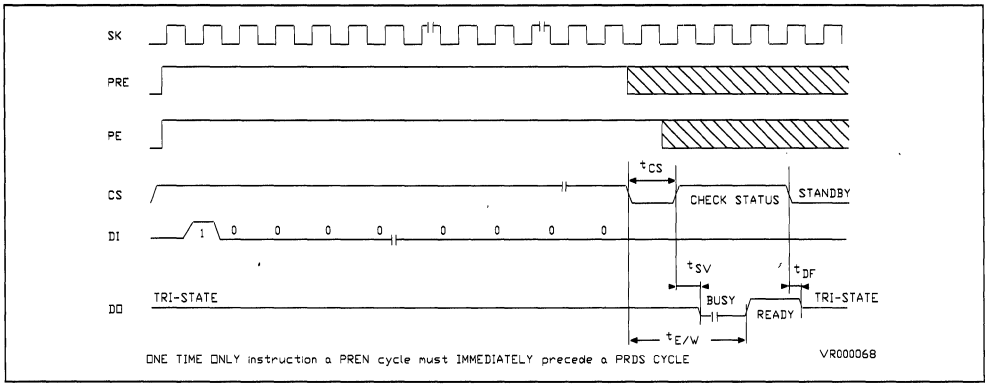


Figure 9 : WRALL

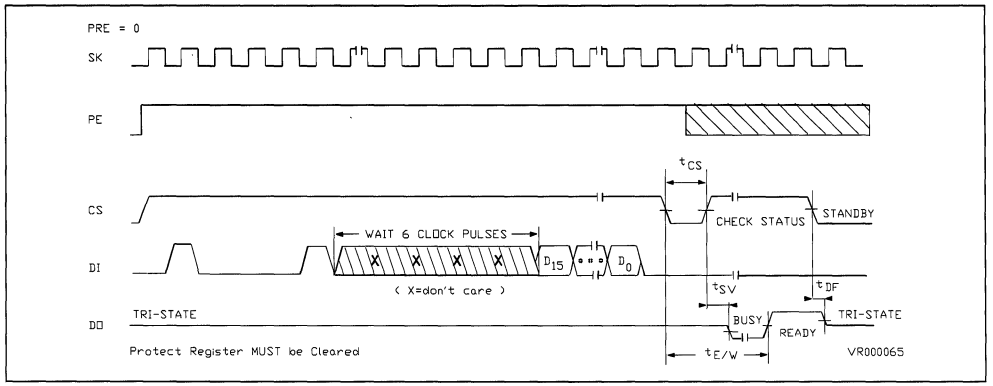


Figure 10 : PRREAD

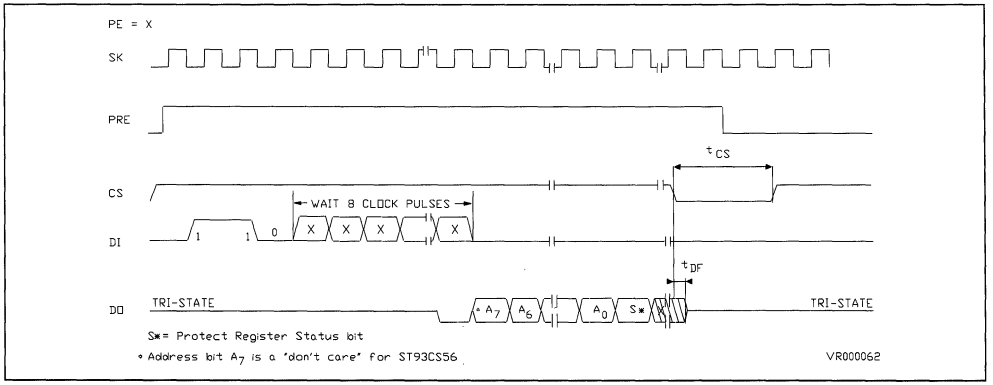


Figure 11 : PREN

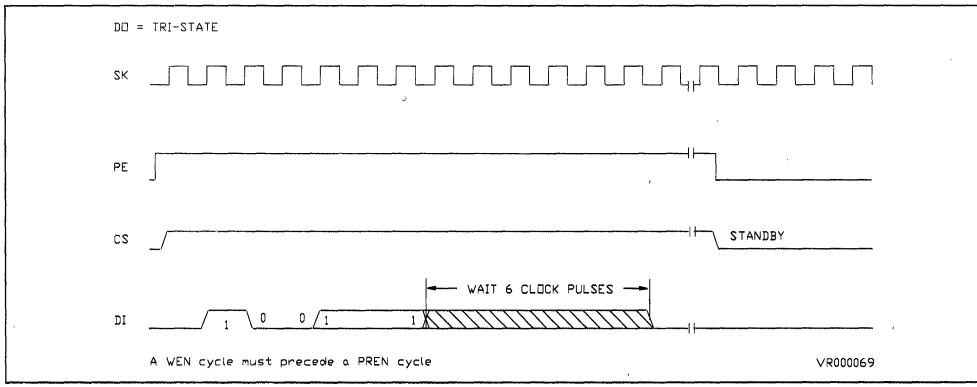


Figure 12 : PR CLEAR

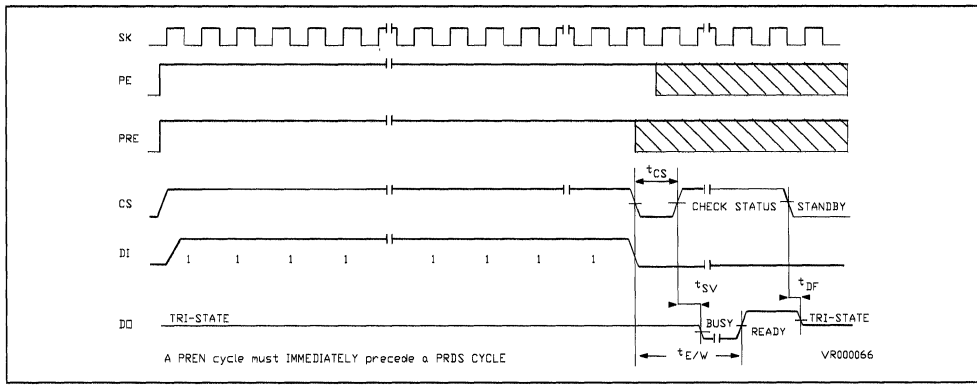
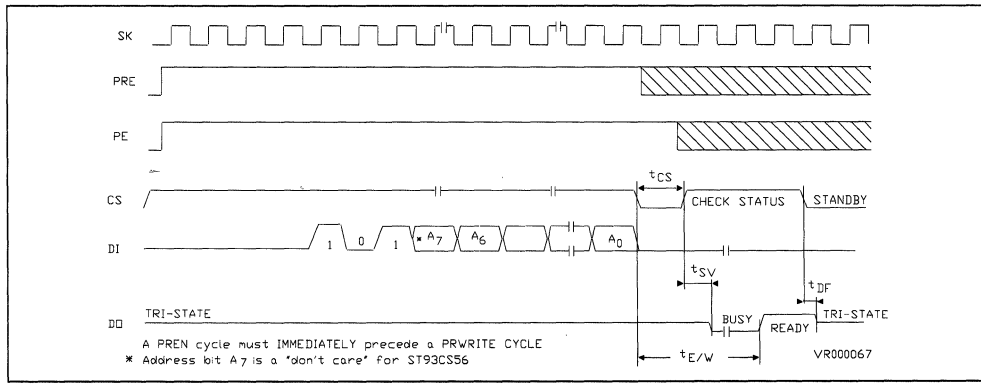


Figure 13 : PR WRITE

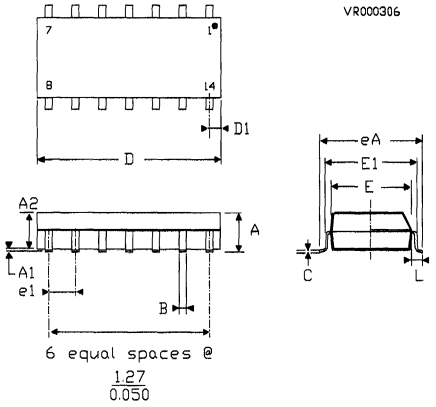


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST93CS57B1	Dual-in-line	0°C to 70°C	2.5V to 5.5V
ST93CS57M1	PSO 8		
ST93CS57ML1	PSO 14		
ST93CS57B6	Dual-in-line	-40°C to 85°C	
ST93CS57M6	PSO 8		
ST93CS57ML6	PSO 14		
ST93CS57B3	Dual-in-line	-40°C to 125°C	
ST93CS57M3	PSO 8		
ST93CS57ML3	PSO 14		

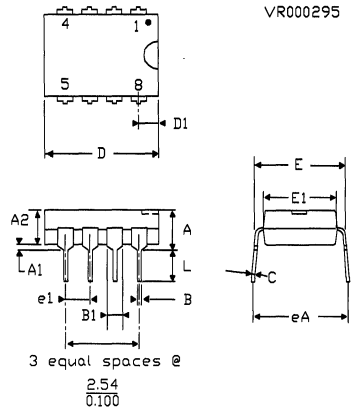
PACKAGE MECHANICAL DATA

PSO14 PACKAGE (ML)



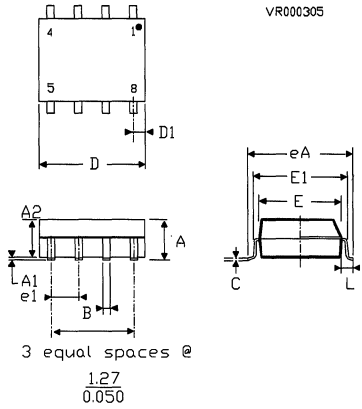
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10		0.20	.004		.008
A2			1.60			0.063
B	0.35		0.46	.014		.018
C	0.19		0.25	.007		.010
D	8.55		8.75	.337		.344
D1			0.68			.027
E	3.80		4.00	.150		.157
E1	4.60		5.30	.181		.209
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.50		1.27	.020		.050

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050

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