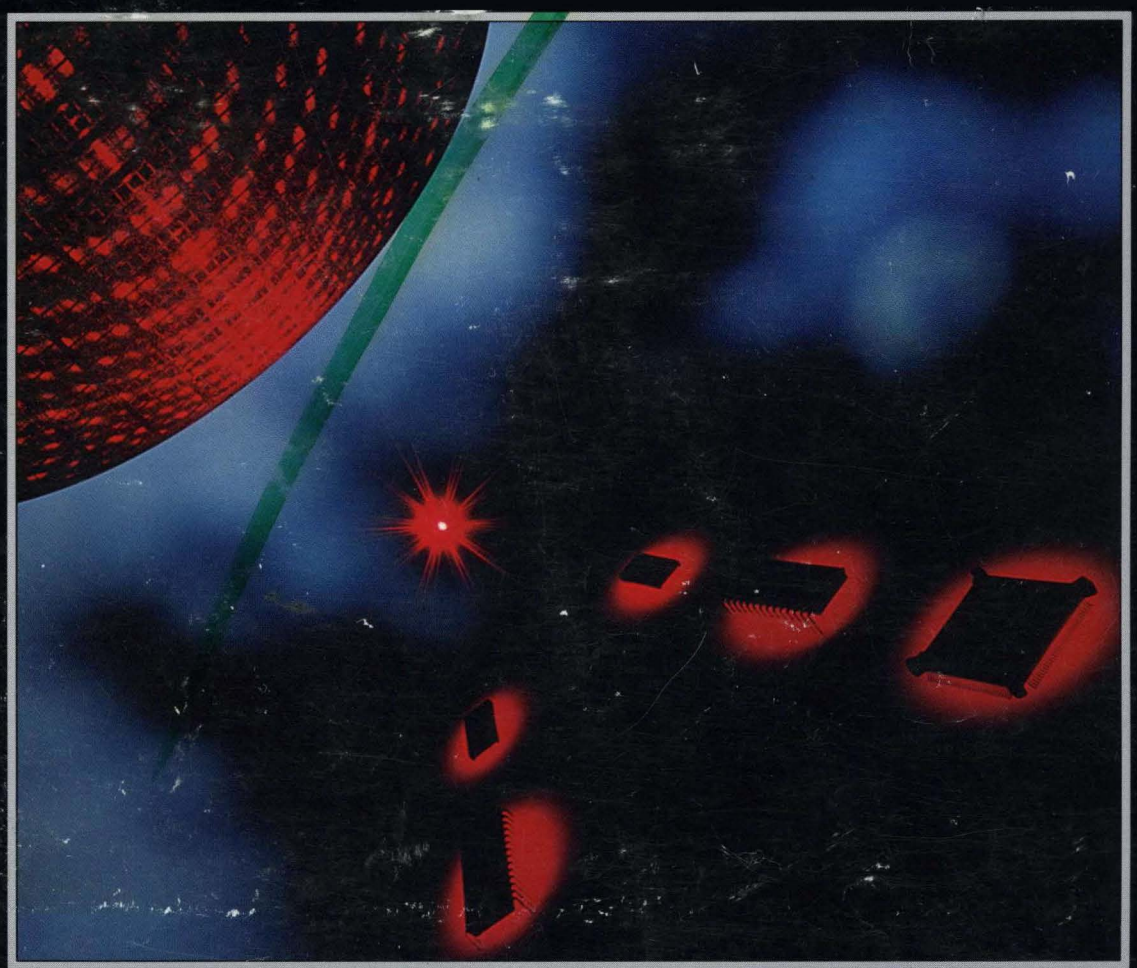
SHARP

Memory
Data Book

1991/1992



SHARP Memory Data Book 1991/1992

NOTICE

The specifications contained within this Sharp Memory Data Book are current as of the October, 1991 publication date.

The product data provided is classified and labeled as follows:

CLASSIFICATION *	DESCRIPTION
Product Preview	Contains information about a device that is in the planning stage or the soon to be in-development stage.
Advance Information	Contains information about a device that is in development. Includes design specifications for device development.
Preliminary	Contains information for device soon to be, or recently, released to production.
No label is used for this classification.	Contains information about a device that is in full production.

* Note: occasionally certain product data information may be classified and labeled differently than the main classification label. For example, a main label may be 'Preliminary', but the 15 ns version of that part may be labeled 'Advance Information.'

Sharp reserves the right to make changes in the circuitry or specifications described herein at any time without notice in order to improve design or reliability. The information in this Memory Data Book has been carefully checked to be accurate, however, Sharp makes no warranty for any errors which may appear in this document. Contact Sharp to obtain the latest version of device specifications before placing your order.

Sharp makes no representations that circuitry described herein is free from infringement of patent or other rights of third parties which may result from its use. No license is granted by implication under any patent rights or other rights of Sharp Corporation.

This is a newly revised 1991/92 Memory Data Book which can be used in place of the former edition (1989/1990).

PREFACE

As we become more and more an information-oriented society, memory products have come to play a major role in both home and office equipment. On the one hand, computer-related services are growing ever more sophisticated and diverse; on the other, they are becoming much more accessible to each of us in our daily lives. Along with this increase in the importance of the information processing in our lives, we are faced with a growing demand for memory products using the most advanced technology.

To keep pace with this rapid progress, we at Sharp will continue to direct our efforts at understanding the crucial trends of the moment in this area and supply our customers with products that truly meet their needs. In short, to contribute to a better life for all of us in this age of expanding technology.

Sharp has developed a wide range of memory units including SRAMs, DRAMs, EPROMs, OTPROMs, Mask Programmable ROMs, and FIFO Memories for use in numerous areas of application. Sharp memory units are used extensively in personal computers, advanced office automation and measuring control equipment, video games, as well as in character processing and dictionary ROMs.

This data book has been especially compiled for the use of our customers. Listed here is the entire range of memory products developed and manufactured by Sharp, with detailed explanations of their many functions and outstanding features. We hope that you find this book useful in determining which Sharp products are best suited to your needs. Please contact us directly if you have any further questions.

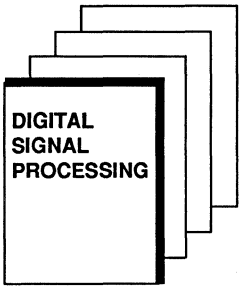
SHARP'S INTEGRATED CIRCUIT DOCUMENTATION

MICRO-COMPUTER

- 4-Bit Single-Chip Microcomputers
- 8-Bit Single-Chip Microcomputers
- 8-Bit Microprocessors/Peripherals
- 16-Bit Microprocessors/Peripherals
- Development Support Tools

MOS

- Gate Arrays/Standard Cells
- Display Drivers, Telecommunications
- MODEMs, CCDs/CCD Peripherals
- ICs for Audio/Visual Equipment
- Voice/Melody Generators, ICs for Clock, etc.



DIGITAL SIGNAL PROCESSING

24-Bit Real Time Digital Signal Processing

- Data Sheets
- User's Guides
- Simulator Guides
- Application Notes
- Evaluation Modules/Boards

BIPOLAR

- Operational Amplifiers/Comparators
- Transistor Arrays, Voltage Regulators
- A/D, D/A Converters, Bus Interfaces
- ICs for Audio/Visual Equipment
- CCD Peripherals, ICs for Telephone, etc.

MEMORY

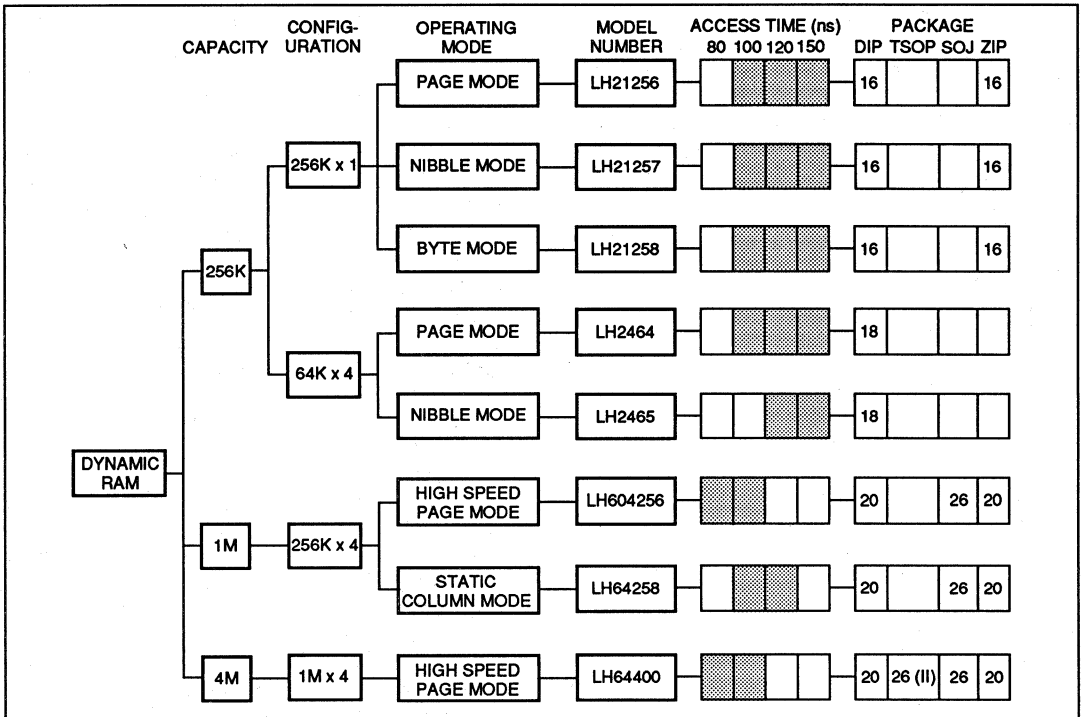
- Dynamic RAMs, Field Memories
- Static RAMs, Pseudo Static RAMSs
- EPROMs/OTPROMs
- Mask Programmable ROMs
- FIFO Memories

RELIABILITY HANDBOOK

- Quality and Reliability Assurance System
- How Sharp Views Semiconductor Device Reliability and Reliability Prediction
- Reliability Testing
- Failure Analysis
- Proper Handling of Semiconductor Devices

TABLE OF CONTENTS

DYNAMIC RAMs



NOTES:

☐ (Empty box) = Contact Sharp representative for availability.

▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book.

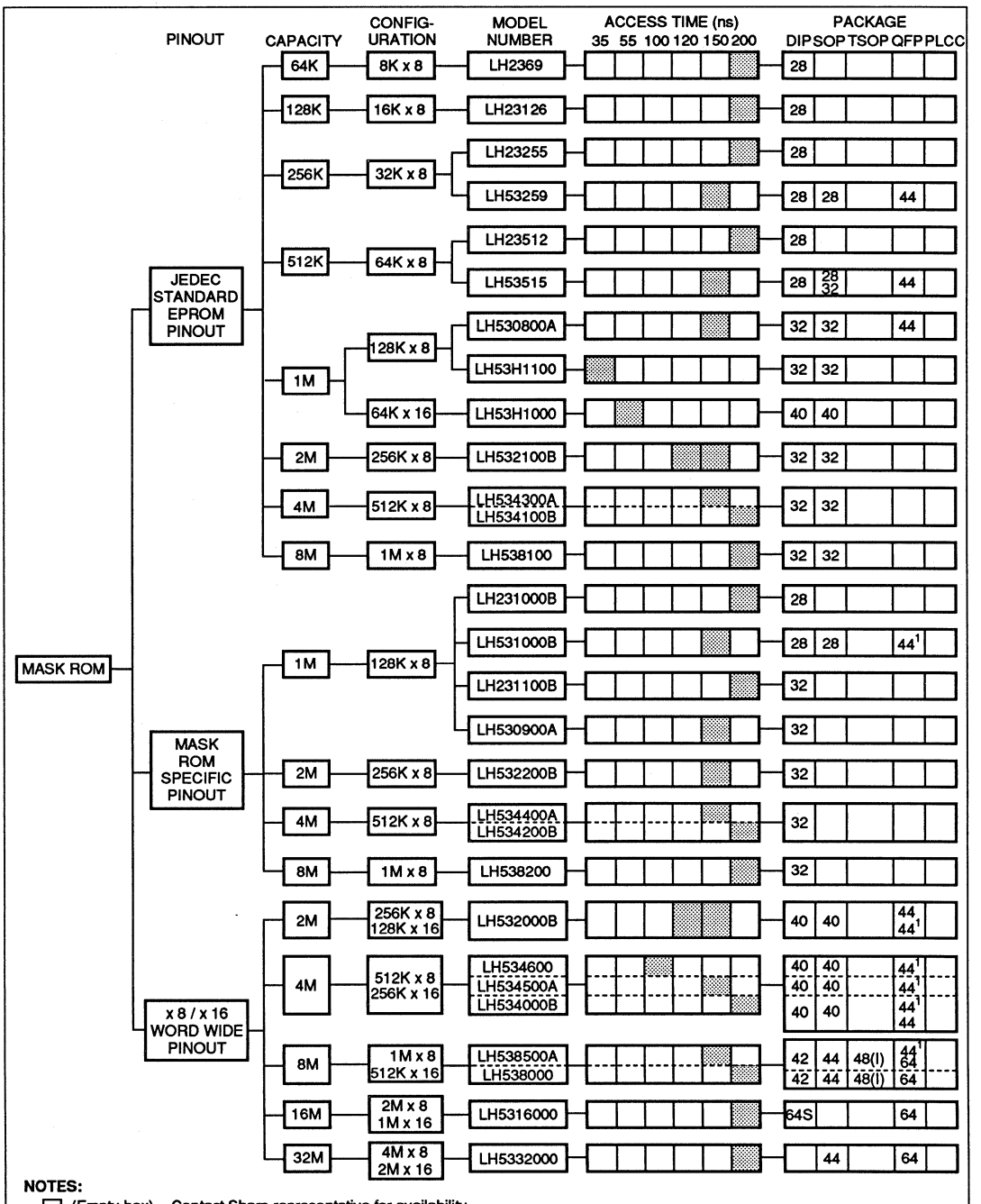
MD-2

DYNAMIC RAMs

CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUPTION OPERATING/ STANDBY (mW) MAX.	OPERATING MODE	PACKAGE
256K	262,144 × 1	LH21256	100	200	440/28	Page mode	16DIP/16ZIP
			120	230	440/28		
			150	260	385/28		
		LH21257	100	200	440/28	Nibble mode	16DIP/16ZIP
			120	230	440/28		
			150	260	385/28		
		LH21258	100	200	440/28	Byte Mode	16DIP/16ZIP
			120	230	440/28		
			150	260	385/28		
	65,536 × 4	LH2464	100	200	523/28	Page mode	18DIP
			120	220	457/28		
			150	260	413/28		
		LH2465	120	220	457/28	Nibble mode	18DIP
			150	260	413/28		
1M	262,144 × 4	LH604256	80	160 (50) [2]	413/11	High speed page mode	20DIP/20ZIP/26SOJ
			100	190 (55) [2]	358/11		
		LH64258	100 (50) [1]	160 (55) [1]	374/11	Static column mode	20DIP/20ZIP/26SOJ
			120 (60) [1]	190 (65) [1]	340/11		
4M	1,048,576 × 4	LH64400 [1]	80 (40) [2]	140 (50) [2]	523/5.5	High speed page mode	20DIP/20ZIP/26SOJ 26TSOP (II) [3]
			100 (50) [2]	160 (55) [2]	468/5.5		

NOTES:
1. Static column mode
2. High speed page mode
3. S: Type II: Forward bend
   SR: Type II: Reverse bend

MASK PROGRAMMABLE ROMs



NOTES:

- ☐ (Empty box) = Contact Sharp representative for availability.
- ▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book.

LH2XXX: NMOS LH5XXX: CMOS

1. 14 x 14 mm² package

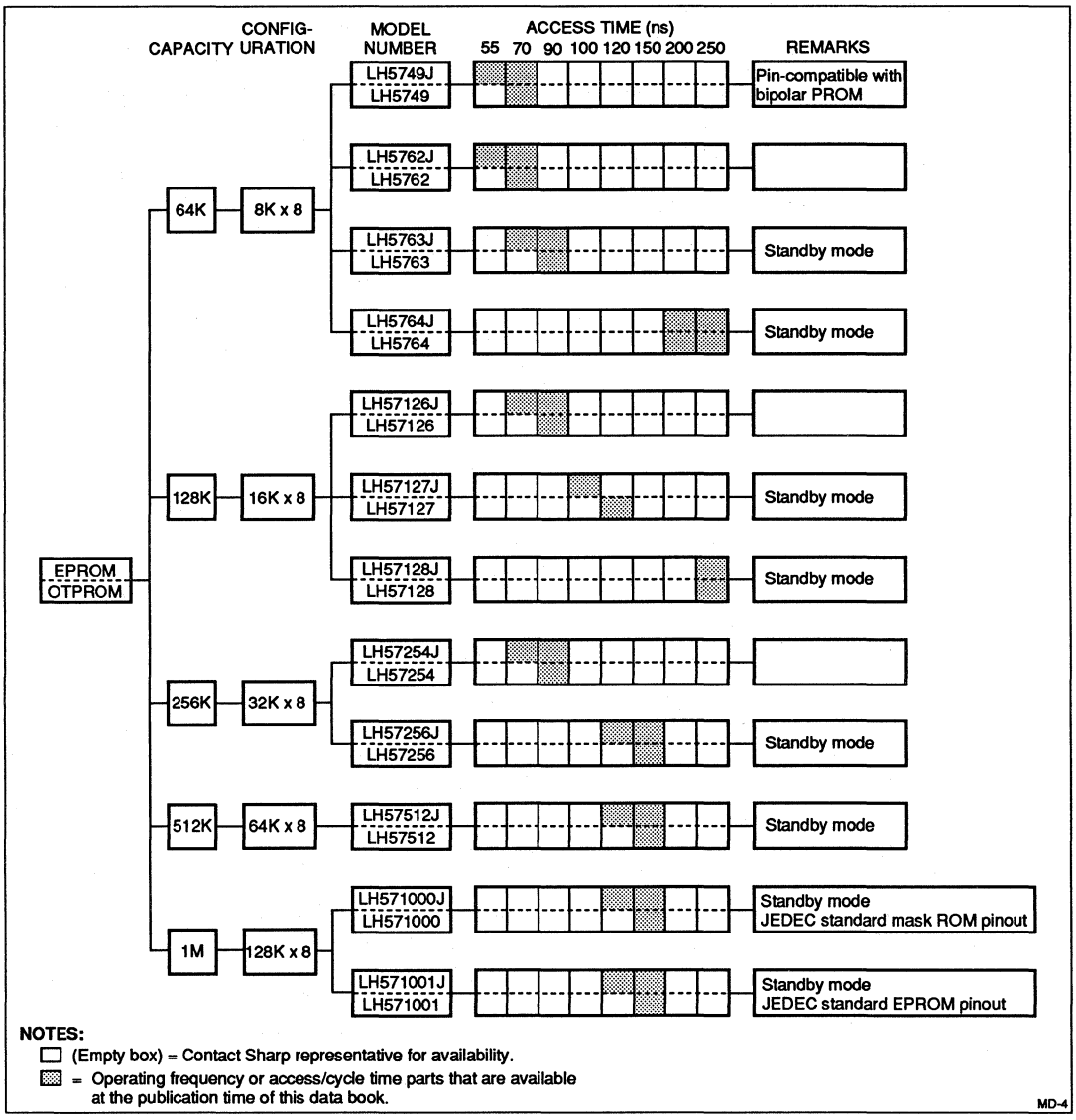
MD-5

MASK PROGRAMMABLE ROMs

PROCESS	CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	USERS NO.	ACCESS TIME (ns) MAX. CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX.	PACKAGE
NMOS	64K	8,192 × 8	LH2369	LH2369XX	200	330	28DIP
	128K	16,384 × 8	LH23126	LH2326XX	200	440	28DIP
	256K	32,768 × 8	LH23255	LH2355XX	200	440	28DIP
	512K	65,536 × 8	LH23512	LH2312XX	200	550	28DIP
	1M	131,072 × 8	LH231000B	LH231GXX	200	550	28DIP
			LH231100B	LH231JXX	200	550	32DIP
CMOS	256K	32,768 × 8	LH53259	LH5359XX	150	110	28DIP/28SOP/44QFP/32PLCC
	512K	65,536 × 8	LH53515	LH5315XX	150	195	28DIP/28SOP/44QFP/32PLCC/32SOP
	1M	131,072 × 8	LH53H1100	LH5H11XX	35	660	32DIP/32SOP
			LH530800A	LH531HXX	150	195	32DIP/32SOP/44QFP/32PLCC
			LH530900A	LH531JXX	150	195	32DIP
			LH531000B	LH531GXX	150	195	28DIP/28SOP/44QFP [1]
		65,536 × 16	LH53H1000	LH5H10XX	55	660	40DIP/40SOP
	2M	262,144 × 8	LH532100B	LH532HXX	120/150	275	32DIP/32SOP/32PLCC
			LH532200B	LH532JXX	150	275	32DIP
		262,144 × 8 131,072 × 16	LH532000B	LH532GXX	120/150	275	40DIP/40SOP/44QFP [1]/44QFP
	4M	524,288 × 8	LH534300A	LH534DXX	150	330	32DIP/32SOP/32PLCC
			LH534100B	LH534HXX	200	275	32DIP/32SOP/32PLCC
			LH534400A	LH534EXX	150	275	32DIP
			LH534200B	LH534JXX	200	275	32DIP
		524,288 × 8 262,144 × 16	LH534600	LH5346XX	100	550	40DIP/40SOP/44QFP [1]
			LH534500A	LH534FXX	150	275	40DIP/40SOP/44QFP [1]
			LH534000B	LH534GXX	200	275	40DIP/40SOP/44QFP [1]/44QFP
	8M	1,048,576 × 8	LH538100	LH5381XX	200	275	32DIP/32SOP
			LH538200	LH5382XX	200	275	32DIP
		1,048,576 × 8 524,288 × 16	LH538000	LH5380XX	200	275	42DIP/44SOP/48TSOP(I)/64QFP
			LH538500A	LH538FXX	150	275	42DIP/44SOP/48TSOP/44QFP [1]/64QFP
	16M	2,097,152 × 8 1,048,576 × 16	LH5316000	LH5316XX	200	275	64SDIP/64QFP
	32M	4,194,304 × 8 2,097,152 × 16	LH5332000	LH5332XX	200	275	44SOP/64QFP

NOTES:
1. 14 × 14 mm^2 package

EPROMs/OTPROMs



NOTES:

- ☐ (Empty box) = Contact Sharp representative for availability.
- ▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book.

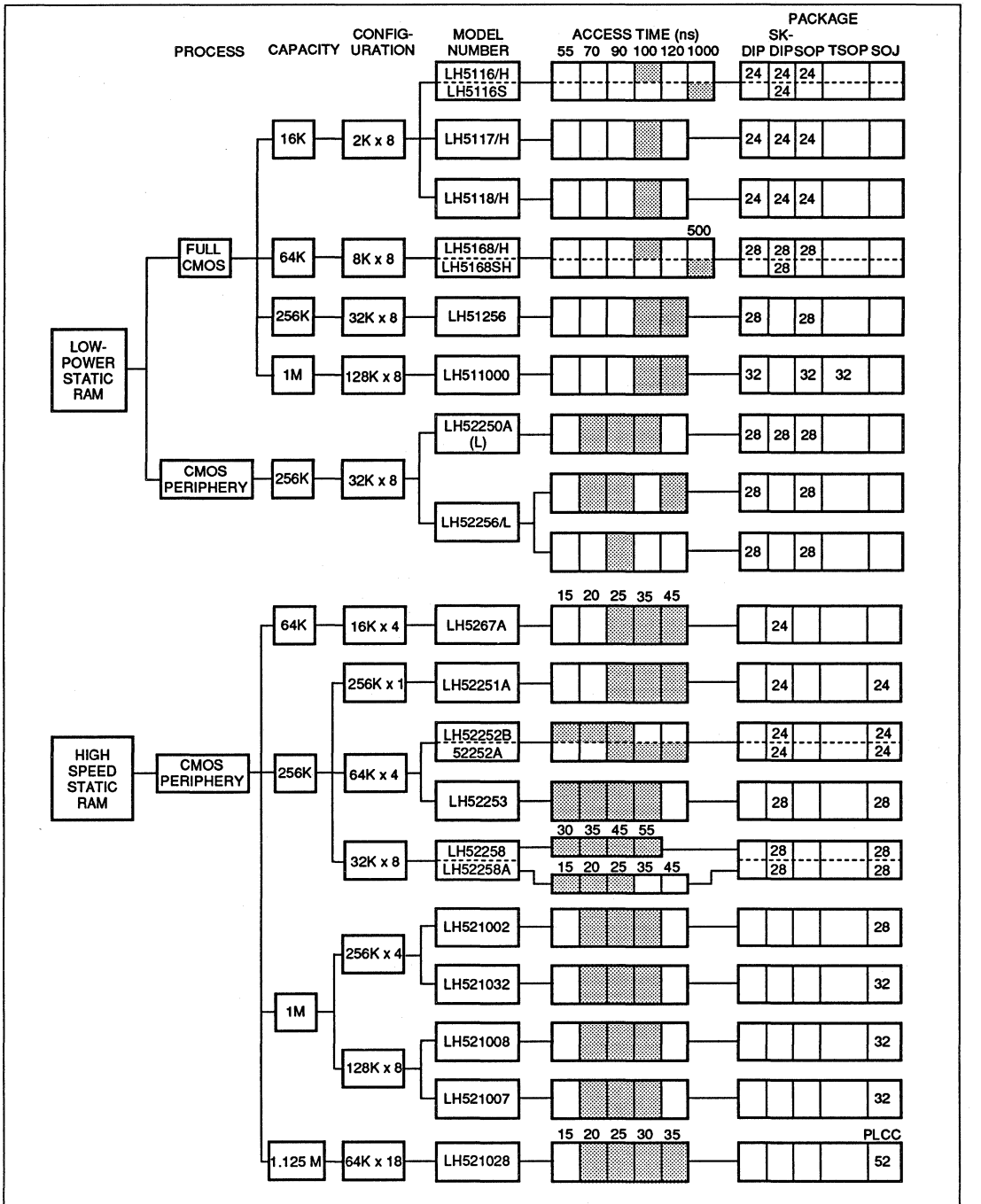
EPROMs/OTPROMs

PRODUCT	CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	STANDBY MODE	ACCESS TIME (ns) MAX.	POWER CONSUMPTION (mW) MAX.	PROGRAM VOLTAGE (V)	PACKAGE
EPROM	64K	8,192 × 8	LH5749/J		55	394	13	24CERDIP [1]
					70			
			LH5762J		55	394	12.5	28CERDIP
					70			
			LH5763J	•	70	315	12.5	28CERDIP
				•	90			
			LH5764J	•	200	165	12.75	28CERDIP
				•	250			
	128K	16,384 × 8	LH57126J		70	394	12.5	28CERDIP
					90			
			LH57127J	•	100	315	12.5	28CERDIP
			LH57128J	•	250	165	12.75	28CERDIP
	256K	32,768 × 8	LH57254J		70	420	12.5	28CERDIP
					90			
			LH57256J	•	120	165	12.75	28CERDIP
				•	150			
	512K	65,536 × 8	LH57512J	•	120	165	12.75	28CERDIP
				•	150			
	1M	131,072 × 8	LH571000J	•	120	220	12.75	32CERDIP [2]
				•	150			
			LH571001J	•	120	220	12.75	32CERDIP [3]
				•	150			
OTPROM	64K	8,192 × 8	LH5749		70	394	13	24DIP/24SK-DIP/ 24SDIP
			LH5762		70	394	12.5	28DIP
			LH5763	•	90	315	12.5	28DIP
			LH5764	•	200	165	12.75	28DIP/28SOP
				•	250			
	128K	16,384 × 8	LH57126		90	394	12.5	28DIP
			LH57127	•	120	315	12.5	28DIP
			LH57128	•	250	165	12.75	28DIP/28SOP
	256K	32,768 × 8	LH57254		90	420	12.5	28DIP
			LH57256	•	150	165	12.75	28DIP/28SK-DIP/ 28SOP
	512K	65,536 × 8	LH57512	•	150	165	12.75	28DIP/28SOP
	1M	131,072 × 8	LH571000	•	150	220	12.75	32DIP [2]
			LH571001	•	150	220	12.75	32DIP [3]

NOTES:
The model numbers of OTPROMs in this catalog are different from those programmed according to customers request.

1. Bipolar PROM pinout
2. JEDEC standard mask ROM pinout
3. JEDEC standard EPROM pinout

STATIC RAMs



NOTES:

- ☐ (Empty box) = Contact Sharp representative for availability.
- ▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book.

MD-3

STATIC RAMs

PROCESS	CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW/μW) MAX.	PACKAGE
FULL CMOS	16K	2,048 × 8	LH5116	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5116H [1]	100	100	220/5.5	
			LH5116S [4]	1000	1000	33/3.3	24SOP
			LH5117	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5117H [1]	100	100	220/5.5	
			LH5118	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5118H [1]	100	100	220/5.5	
	64K	8,192 × 8	LH5168	100	100	248/5.5	28DIP/28SOP/28SK-DIP
			LH5168H [1]	100	100	275/16.5	
			LH5168SH [1, 4]	500	500	150/9 (3V)	28SOP
	256K	32,768 × 8	LH51256 [1] (L)	100	100	248/16.5(5.5)	28DIP/28SOP
				120	120		
	1M	131,072 × 8	LH511000 [1] (L)	100	100	330/55(5.5)	32DIP/32SOP/32TSOP(I) [2]
				120	120		
CMOS PERIPHERY	64K	16,384 × 4	LH5267A [2]	25	25	660/5500	24SK-DIP
				35	35	660/5500	
				45	45	660/5500	
	256K	262,144 × 1	LH52251A	25	25	825/5500	24SK-DIP/24SOJ
				35	35	660/5500	
				45	45	550/5500	
		65,536 × 4	LH52252A	25	25	825/5500	24SK-DIP/24SOJ
				35	35	660/5500	
				45	45	550/5500	
			LH52252B	15	15	910/5500	24SK-DIP/24SOJ
				20	20	800/5500	
				25	25	745/5500	
			LH52253	15	15	910/5500	28SK-DIP/28SOJ
				20	20	800/5500	
				25	25	745/5500	
				35	35	745/5500	
		32,768 × 8	LH52250A(L)	70	70	440/5500 (550)	28DIP/28SOP/28SK-DIP
				90	90	385/5500 (550)	
				100	100	385/5500 (550)	
			LH52256/L	70	70	440/550	28DIP/28SOP
				90	90	385/550	
				120	120	385/550	
			LH52256LL	90	90	385/220	28DIP/28SOP
			LH52258	30	30	1020/5500	28SK-DIP/28SOJ
				35	35	715/5500	
				45	45	605/5500	
				55	55	855/5500	
			LH52258A	15	15	910/5500	28SK-DIP/28SOJ
				20	20	825/5500	
				25	25	745/5500	

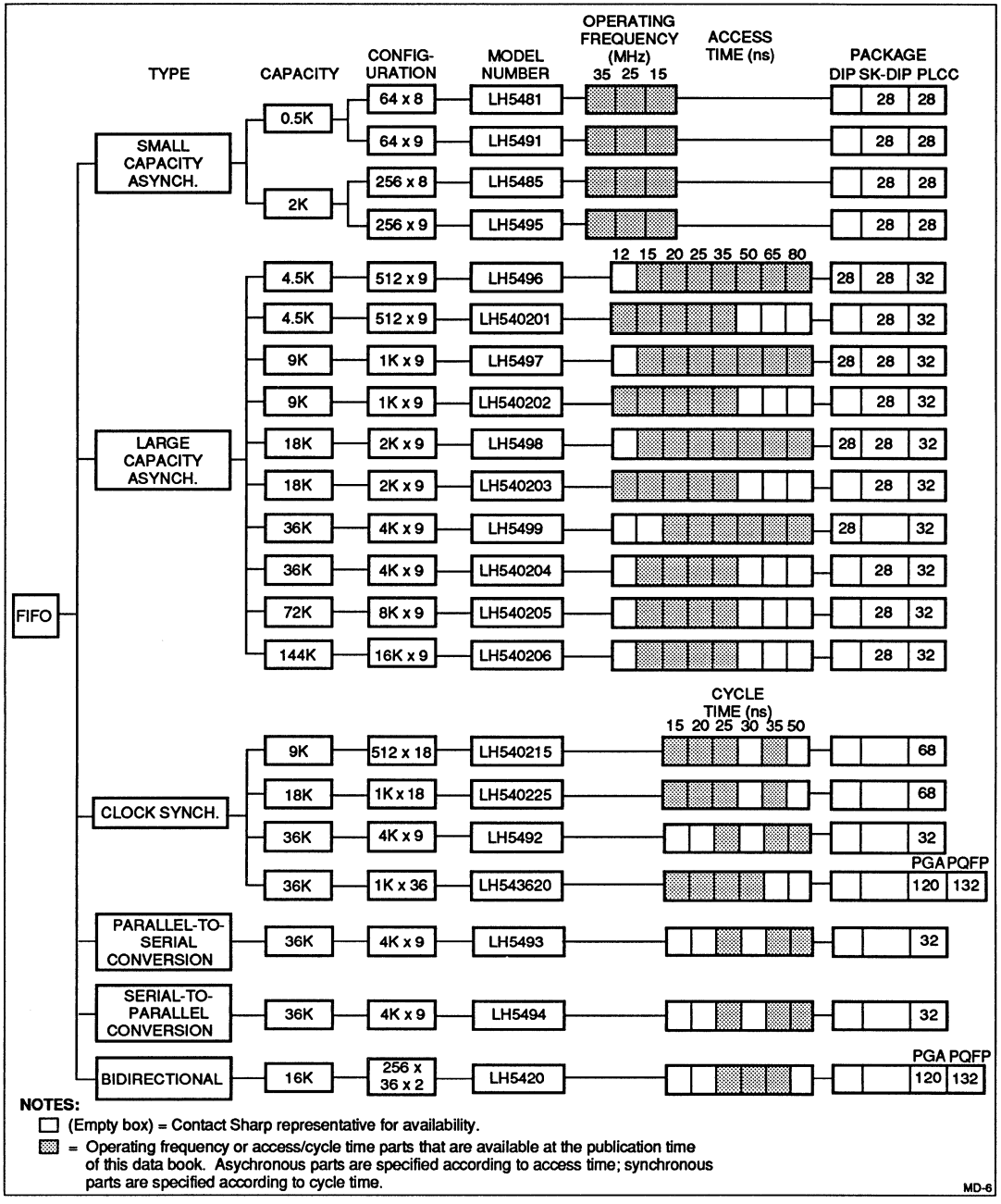
NOTES:

1. T_{OPR} = -40 to +85°C
2. T TSOP (Type I) Forward bend
   TR TSOP (Type I) Reverse bend
3. Supply Voltage (V) = 3 ± 10%
4. Supply Voltage (V) = 2.5 to 5.5

STATIC RAMs (cont'd)

PROCESS	CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW/μW) MAX.	PACKAGE
CMOS PERIPHERY	1M	262,144 × 4	LH521002	20	20	715/11000	28SOJ
				25	25	660/11000	
				35	35	550/11000	
			LH521032	20	20	TBD	32SOJ
				25	25	TBD	
				35	35	TBD	
		131,072 × 8	LH521008	20	20	825/11000	32SOJ
				25	25	770/11000	
				35	35	660/11000	
			LH521007	20	20	TBD	32SOJ
				25	25	TBD	
				35	35	TBD	
	1.125M	65,536 × 18	LH521028	20	20	TBD	52PLCC
				25	25	TBD	
				30	30	TBD	
				35	35	TBD	

FIFO MEMORIES



NOTES:

☐ (Empty box) = Contact Sharp representative for availability.

▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book. Asychronous parts are specified according to access time; synchronous parts are specified according to cycle time.

MD-6

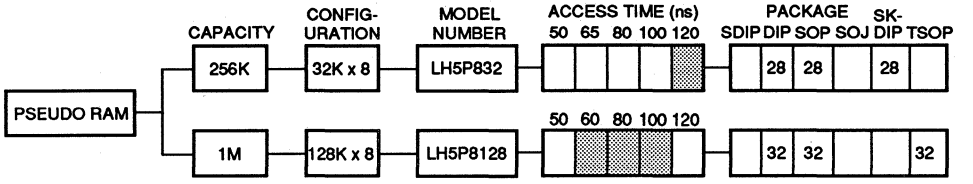
FIFO MEMORIES

CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	OPERATING FREQUENCY (MHz)	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX. ACTIVE/ STANDBY	PACKAGE
0.5K	64 × 8	LH5481	15	—	—	248/—	28SK-DIP/28PLCC
			25				
			35				
	64 × 9	LH5491	15	—	—	248/—	28SK-DIP/28PLCC
			25				
			35				
2K	256 × 8	LH5485	15	—	—	385/—	28SK-DIP/28PLCC
			25				
			35				
	256 × 9	LH5495	15	—	—	385/—	28SK-DIP/28PLCC
			25				
			35				
4.5K	512 × 9	LH5496	—	15	—	550/28	28DIP/28SK-DIP/32PLCC
				20			
				25			
				35			
				50			
				65			
				80			
		LH540201	—	12	—	550/28	28SK-DIP/32PLCC
				15			
				20			
				25			
				35			
9K	1,024 × 9	LH5497	—	15	—	550/28	28DIP/28SK-DIP/32PLCC
				20			
				25			
				35			
				50			
				65			
				80			
		LH540202	—	12	—	550/28	28SK-DIP/32PLCC
				15			
				20			
				25			
				35			
	512 × 18	LH540215	—	—	15	550/28	68PLCC
					20		
					25		
					35		
16K	256 × 36 × 2	LH5420	—	—	25	1540/—	120PGA/132PQFP
					30		
					35		

FIFO MEMORIES (cont'd)

CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX. ACTIVE/ STANDBY	PACKAGE
18K	2,048 × 9	LH5498	15	—	550/28	28DIP/28SK-DIP/32PLCC
			20			
			25			
			35			
			50			
			65			
			80			
		LH540203	12	—	550/28	28SK-DIP/32PLCC
			15			
			20			
			25			
			35			
	1,024 × 18	LH540225	—	15	550/28	68PLCC
				20		
				25		
				35		
36K	4,096 × 9	LH5499	20	—	550/44	28DIP/32PLCC
			25			
			35			
			50			
			65			
			80			
		LH540204	15	—	550/28	28SK-DIP/32PLCC
			20			
			25			
			35			
		LH5492	—	25	825/138	32PLCC
				35		
				50		
		LH5493	—	25	825/138	32PLCC
				35		
				50		
		LH5494	—	25	825/138	32PLCC
				35		
				50		
72K	8K × 9	LH540205	15	—	550/44	28SK-DIP/32PLCC
			20			
			25			
			35			
144K	16K × 9	LH540206	15	—	550/44	28SK-DIP/32PLCC
			20			
			25			
			35			

PSEUDO STATIC RAMs

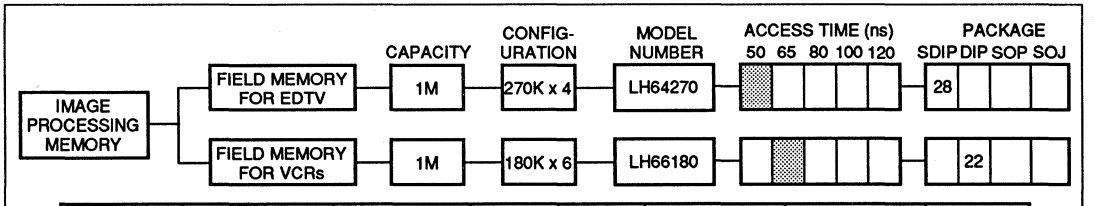


CAPACITY	CONFIG-URATION (WORDS x BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW) MAX.	OPERATING MODE	PACKAGE
256K	32,768 x 8	LH5P832	120	120	303/16.5	PSEUDO SRAM	28DIP/ 28SK-DIP/ 28SOP
1M	131,072 x 8	LH5P8128	60	100	572/5.5	PSEUDO SRAM	32DIP/ 32SOP/ 32TSOP
		LH5P8128	80	130	440/5.5		
		LH5P8128	100	160	376/5.5		

NOTES:
☐ (Empty box) = Contact Sharp representative for availability.
▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book.

7A

FIELD MEMORIES



CAPACITY	CONFIG-URATION (WORDS x BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW) MAX.	OPERATING MODE	PACKAGE
1M	276,480 x 4	LH64270	50	60	550/110	FIELD MEMORY FOR EDTV	28SDIP
1M	189,360 x 6	LH66180	65	88	413/83	FIELD MEMORY FOR VCRs	22DIP

NOTES:
☐ (Empty box) = Contact Sharp representative for availability.
▨ = Operating frequency or access/cycle time parts that are available at the publication time of this data book.

7B

QUALITY ASSURANCE

Quality Assurance System

Sharp develops and produces a wide range of consumer and industrial-use semiconductor products.

In recent years, the applications of ICs have expanded significantly, into fields where extremely high levels of quality are critical.

In response, Sharp has implemented a total quality assurance system that encompasses the entire production process from planning to after-sales service. This system ensures that quality is a priority in the planning development and production and guarantees product reliability through rigorous reliability testing. We compiled the "Sharp Semiconductor Reliability Handbook, IC Edition" to introduce you to the results of some of our research and to our quality and reliability philosophy and programs. We hope that it is informative and that it will help Sharp customers develop and refine their quality and reliability assurance and control activities. We will introduce a part of this system here.

Sharp's quality and reliability assurance activities are based on the following guidelines:

- All personnel should participate in quality assurance by continually cultivating a higher level of quality awareness.
- In the design and development stages of new products, create reliable designs that consider reliability in every respect.
- Quality control in all production processes, all working environments, materials, equipment, and measuring devices should be carefully monitored to ensure quality and reliability from the very beginning of the production process.
- Confirm long-term reliability and obtain a thorough understanding of practical limits through reliability testing.
- Continually work to improve quality through application of data from process inspections, reliability testing, and market surveys.

Quality Assurance During New Product Development

New product development ***(Figure 1)*** begins with an accurate grasp of the purpose, environment, and manners in which customers will use the product as well as the required reliability. A development plan is then drafted, clarifying the price, quantity, sales period and target reliability of the product to be manufactured.

Quality and reliability are built into the product from the beginning of the product cycle by introducing design review (DR) and reliability planning in the development and design stage. The first tasks undertaken in this stage are process development and circuitry design, by which a prototype, or technical sample (TS), is made. An evaluation of the technical sample is conducted, centering on the function and performance of the sample under conditions in which the final product will be used (TS evaluation).

Next, an engineering sample (ES) is made, based on the results of the TS evaluation, and it is subjected to ES evaluation. The ES evaluation consists of determining, under mass production conditions, whether the product functions and performs as intended during development and design. Reliability testing is also used to decide whether the engineering sample has the required degree of reliability.

In the final stage, the transfer of the product to mass production is discussed - based on the results of the TS and ES evaluations. Once TS and ES are accepted, preproduction begins. At this time, it is determined whether the quality and reliability obtained during development and design can be maintained, whether there are any discrepancies in the production process and what yields will be. The manufacturability of the product is determined, based on these results.

DR (Design Review) is performed to prevent faulty operation and to enhance the functions, usability, quality and reliability, upon completion of structural design, logic design, software design, circuit design, TS/ES evaluation and reliability tests.

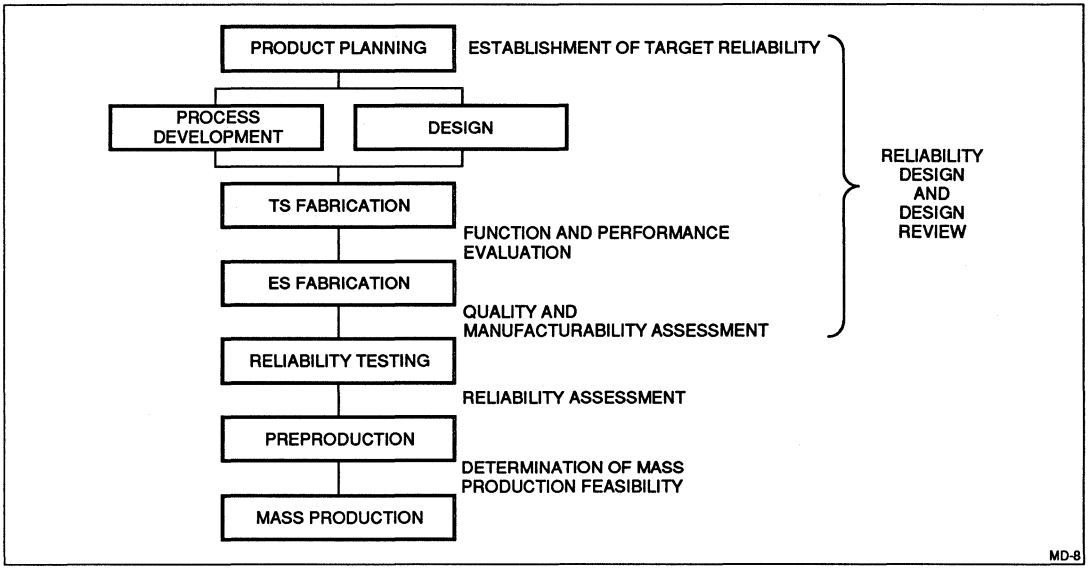


Figure 1. New Product Development Steps

PROCESS	CHARACTERISTIC(S) CONTROLLED	PURPOSE OF CONTROL
SILICON WAFER INCOMING INSPECTION	EXTERNAL APPEARANCE, DIMENSIONS, SHEET RESISTIVITY	REMOVE PRODUCTS HAVING IMPROPER DIMENSIONS, FLAWS AND CRYSTAL DEFECTS. ENSURE PROPER SHEET RESISTANCE VALUES
OXIDATION		
OXIDE INSPECTION MONITORING	EXTERNAL APPEARANCE, FILM THICKNESS, SURFACE CLEANLINESS	FIND PINHOLES, CHECK SURFACE CLEANLINESS AND CONTROL FILM THICKNESS
PHOTOLITHOGRAPHY		
VISUAL INSPECTION MONITORING	DEVELOPABILITY, ETCHABILITY, LINE WIDTH	CHECK FOR PROPER DEVELOPMENT AND ETCHING. CONTROL LINE WIDTH
ION IMPLANTATION		
ELECTRICAL INSPECTION OF CHIP MONITORING	ELECTRICAL CHARACTERISTICS, MAJOR DEVICE CHARACTERISTICS	REMOVE PRODUCTS HAVING POOR ELECTRICAL CHARACTERISTICS. ENSURE PROPER DEVICE CHARACTERISTICS
FRAME DICING		
BREAK, SORTING		
DIE INSPECTION	EXTERNAL APPEARANCE	REMOVE CRACKED AND CHIPPED ITEMS.
DIE BONDS		
WIRE DIE BOND INSPECTION MONITORING	EXTERNAL APPEARANCE ADHESIVE STRENGTH	ENSURE QUALITY OF DIE BONDS
WIRE BONDS		
MOLDING COMPOUNDS WIRE BOND INSPECTION MONITORING	EXTERNAL APPEARANCE TENSILE STRENGTH	CHECK POSITION AND SHAPE OF BONDS. ENSURE PROPER WIRE TENSILE STRENGTH
ENCAPSULATION/MOLD MONITORING	TEMPERATURE, TIME, STRESS WIRE CONDUCTIVITY	ENSURE MOLDABILITY. ENSURE PROPER WIRE CONFIGURATION
STABILIZED BAKE		
LEAD SURFACE FINISHING	INGREDIENTS, TEMPERATURE, CONTAMINATION	MAINTAIN FINISH QUALITY
FINISHING INSPECTION MONITORING	THICKNESS, UNIFORMITY (SOLDERABILITY) PLATED LAYER COMPOSITION PLATED LAYER THICKNESS	REMOVE PRODUCTS HAVING PLATING IRREGULARITIES. MAINTAIN PLATING QUALITY
MARKING	TEMPERATURE, TIME, MARKING MATERIAL	MAINTAIN MARK QUALITY
LEAD CUT FORMING	TOOLING SHARPNESS TOOLING DIMENSIONS	PREVENT ABNORMAL STRESS ON PLASTIC MOLD RESULTING IN DAMAGE

MD-9

Figure 2. Example of the Quality Control Process

Raw Materials Control

The level of product quality and reliability is largely governed by the quality of the materials originally making up the production process and environment.

It is the responsibility of the vendor to execute the quality assurance of basic materials purchased by Sharp. Raw material quality assurance is conducted according to the following system:

- Initial selections of a raw material manufacturer.
- Quality qualification for each new material put into use (quality and reliability assessments of devices in which such new materials are used).
- Periodic quality consultations based on quality information obtained during mass production.

Acceptance inspections are carried out as necessary based on acceptance criteria derived from product specifications and approved drawings.

Control of the Manufacturing Environment

Integrated circuit devices are manufactured in a clean room where there is minimal air-born particulates. The use of ultrapure water also aids cleanliness. Such conditions are necessary due to the adhesion of even small bits of foreign particles (0.1 μm or less), no more than 1/5 - 1/10 the size of the smallest IC pattern, can result in defects later in the process.

Particulates not only affects chip yields, but can also have a lethal affect on the quality and reliablity of a device. Therefore, the cleanliness of every piece of equipment and facility in the plant as well as that of work clothes and work articles are controlled. Degree of cleanliness is usually expressed numerically as the number of particles over 0.5 μm per cubic foot of air.

The degree of cleanliness maintained in Sharp clean rooms, where wafers come in direct contact with air, is Class 1. Temperature and humidity are maintained at constant levels by continuous computer-controlled monitoring ***(Table 1).***

The ultrapure de-ionized (DI) water used in the wafer process is manufactured with an ultrapurification equipment, employing ion-exchange treatment, ultraviolet irradiation and ultrafiltration systems.

Table 1.
Clean Room Temperature & Humidity Standards

Temperature	24 ± 0.5°C
Humidity	45 ± 5% RH

Control of Facilities and Instrumentation

Intregrated circuit device technology is experiencing rapid revolutionary change, and advances in IC production facilities and equipment are equally impressive.

Process automation is promoted by using the latest CIM (Computer Intregrated Manufacturing) system to create devices having stable quality and to reduce variance of characteristics. In addition, production facilities maintenance control, and precision control for various instrumentation devices are implemented by both daily and periodic spot inspections.

Facilities' control is conceptually based on Total Productive Maintenance (TPM), in which all concerned employees systematically participate in facilities maintenance activities. Sharp's goal is to create a highly skilled human resource through activities such as:

- operator-initiated maintenance;
- scheduled maintenance;
- corrective maintenance.

Control of instrumentation devices is in accordance with Japanese national standards. Regular calibration by overseeing public agencies also helps maintain a high level of accuracy in these devices.

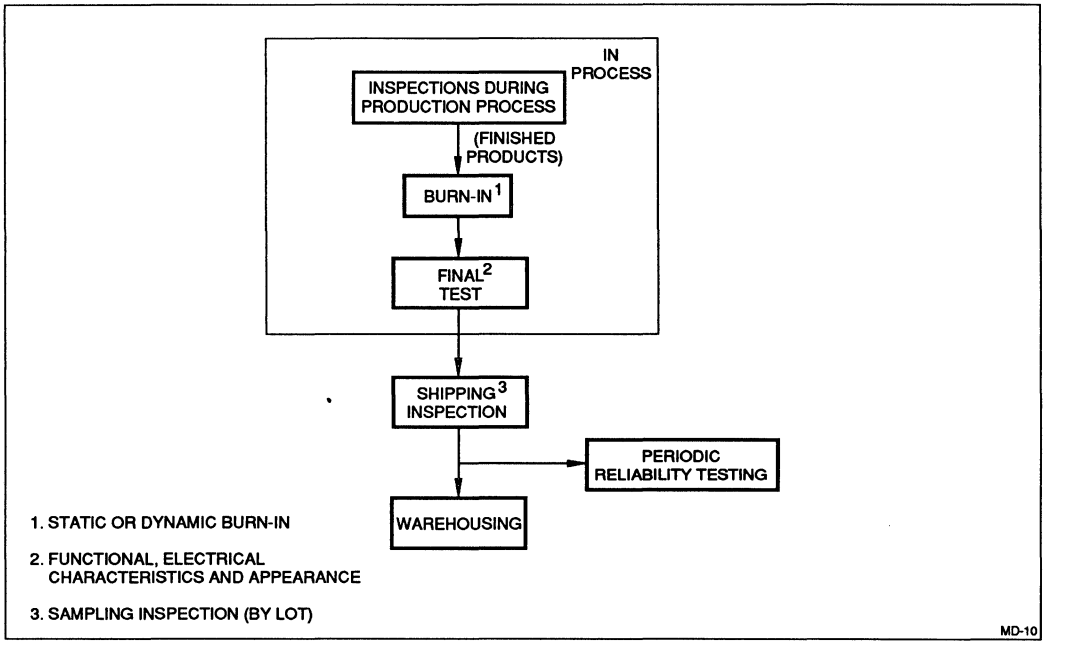


Figure 3. Product Inspection System

Quality Control During the Production Process

Designed-in quality and reliability must be faithfully built into a device during production to manufacture consistently high-quality and high-reliability products.

Production Operations are therefore based on specific, established operational standards. Checks are performed at each process step to decide whether specific characteristics have been obtained and quality has been built in. Each process is monitored to ensure that defectives are not sent to the next process. This is done by rigorously carrying out various standardized controls, appropriate to each process, such as monitoring, visual inspections and sampling inspections.

Sharp strongly promotes the automation of production facilities and equipment. Sharp works to prevent quality problems before they occur and to stabilize quality. Operations that required human skills in the past are now automated. Computer Integrated Manufacturing (CIM) is being introduced into the wafer process. CIM is used to implement comprehensive production control, including conveyance within a process, equipment monitoring and progress control. CIM enables several types of process data to be processed together. Control charts and process capacity index (Cpk) are computed in real time for individual pieces of equipment. Even minute fluctuations in characteristics are fed back to improve control.

Reliability is also being assessed by periodic sampling. This test is a long-term reliability assessment, and the results are fed back to the related divisions.

While quality assurance tests and inspections are conducted for improving and maintaining quality, they also are used to predict the probable reliability a product will have in the marketplace. They provide a multi-faceted approach to ensuring product quality.

Table 2.
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Thermal Environment Tests	Soldering Heat	To determine soldering heat resistance. Standard test conditions: Solder bath temperature: 260 ± 5°C Time: 10 ± 1 sec. Solder composition: Pb:Sn = 4:6	JIS C 7022: A-1 MIL-STD-750 C 2031 IEC Pub. 68 Test Tb
	Temperature Cycling	To determine resistance to high and low temperatures and to temperature changes between these extremes. Standard test conditions: $T_a = T_{stg\ MIN} \sim T_{stg\ MAX}$ [gas environment]	JIS C 7022: A-4 MIL-STD-883 C 1010 IEC Pub. 68 Test Na, Nb
	Thermal Shock	To determine resistance to sudden changes in temperature. Standard test conditions: $T_a = T_{stg\ MIN} \sim T_{stg\ MAX}$ [liquid environment]	JIS C 7022: A-3 MIL-STD-883 C 1011 IEC Pub. 68 Test Nc
	Temperature & Humidity Cycling	To determine resistance to conditions of high temperature and high humidity. Standard test conditions: -10 ~ 65°C, 90 ~ 95% RH, one (1) cycle every 24 hours	JIS C 7022: A-5 MIL-STD-883 C 1004 IEC Pub. 68 Test Z/AD
Mechanical Environment Tests	Variable Frequency Vibration	To determine resistance to vibration during transportation and use. Standard test conditions: Cycle: 100 ~ 2000 H_z in 4 min. Peak acceleration: 20 G Orientation: four (4) times in each of the orientations of ± X, ± Y and ± Z	JIS C 7022: A-10 MIL-STD-883 C 2007 IEC Pub. 68 Test Fc
	Mechanical Shock	To determine resistance to shocks during transportation & use. Standard test conditions: Peak acceleration: 1500 G Pulse duration: 0.5 ms Orientation: three (3) pulses in each of the orientations ± X, ± Y and ± Z	JIS C 7022: A-7 MIL-STD-883 C 2002 IEC Pub. 68 Test Ea
	Constant Acceleration	To determine resistance to constant acceleration. Standard test conditions: Stress level: 20,000 G, Orientation: applied for one (1) min. in each of the orientations ± X, ± Y and ± Z	JIS C 7022: A-9 MIL-STD-883 C 2001 IEC Pub. 68 Test Ga
	Lead Integrity	To determine resistance to installation and handling such as wiring. (1) Tensile strength. Standard test conditions: A specified load is applied in a direction parallel to the lead axis for 10 ± 1 sec. (2) Bending strength. Standard test conditions: A specified load is applied to the tip of each lead and the lead is bent once each through a + and - 90° arc and back. (The specified load is determined by nominal cross section or nominal section modulus.) *TCP (tape carrier package): N/A	JIS C 7002: A-11 IEC Pub. 68 Test U

Table 2. (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Mechanical Environment Tests	Solderability	To determine the solderability of leads which are connected by soldering. Standard test conditions: Solder bath temperature: 230 ± 5°C, Dip time: 5 ± 0.5 sec. Solder composition: Pb:Sn = 4:6, used with rosin flux.	JIS C 7022: A-2 MIL-STD-883 C 2003
	Seal (Hermeticity)	To determine the effectiveness of the seal of hermetically sealed devices. (1) Fine leak detection (helium): measured with a helium detector after storage in an He atmosphere at a prescribed pressure for a designated time period. (2) Gross leak observation (bubbles): observation of bubbles formed by a fluorocarbon or silicone oil.	JIS C 7022: A-6 MIL-STD-883 C 1014 IEC Pub. 68 Test Q
	Salt Atmosphere (Corrosion)	To determine resistance to corrosion in a salt fog. Standard test conditions: Exposure to salt spraying conditions of salt concentration, 5 ± 1%. Spray rate: 0.5 ~ 3 ml/80 cm^3/h Salt fog temperature: 35 ± 2°C for a designated period of time.	JIS C 7022: A-12 MIL-STD-883 C 1009 IEC Pub. 68 Test Ka
Life Tests	High Temperature Operation	To determine resistance to prolonged operating stress, electrical and thermal. Standard test conditions: $T_a = T_{op\ MAX}$ Operating source voltage = Max. operating voltage	JIS C 7022: B-1 MIL-STD-883 C 1005
	High Temperature Storage	To determine resistance to prolonged high temperature storage. Standard test conditions: $T_a = T_{stg\ MAX}$	JIS C 7022: B-3 MIL-STD-883 C 1008
	Low Temperature Storage	To determine resistance to prolonged low temperature storage. Standard test conditions: $T_a = T_{stg\ MIN}$	JIS C 7022: B-4 IEC Pub. 68 Test A
	High Temperature/ High Humidity Bias	To determine resistance to prolonged temperature, humidity and electrical stress. Standard test conditions: 85°C, 85% RH Applied voltage = $V_{TYPICAL}$	JIS C 7022: B-5 IEC Pub. 68 Test C
	High Temperature/ High Humidity Storage	To determine resistance to prolonged storage at high temperature and humidity. Standard test conditions: (1) 60°C, 90% RH (2) 85°C, 85% RH	JIS C 7022: B-5 IEC Pub. 68 Test C

Table 2. (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Miscellaneous	Pressure Cooker (PCT)	To evaluate moisture resistance in a short period of time. Standard test conditions: 121°C, 2atm, no electrical load. 100% RH	EIAJ IC-121: 18
	Composite Test	Several tests (selected from those listed above) performed in series to effectively evaluate product. Example: for a surface mount device: High-Temperature/High-Humidity Storage→Soldering Heat Resistance→Pressure cooker (PCT)	
	Electrostatic Discharge Strength	To determine resistance to electrostatic stress. Standard test conditions: (1) Human body model: Earth capacity C = 100 pF, equivalent Resistance R = 1.5 kΩ (2) Machine model: Earth capacity C = 200 pF, equivalent Resistance R = 0Ω	MIL-STD-883 C 3015 EIAJ IC-121:20
	Latch-Up Strength	To determine resistance to latch-up. Standard test conditions: (1) Condenser charge (2) Current application (3) V_{CC} overvoltage application	

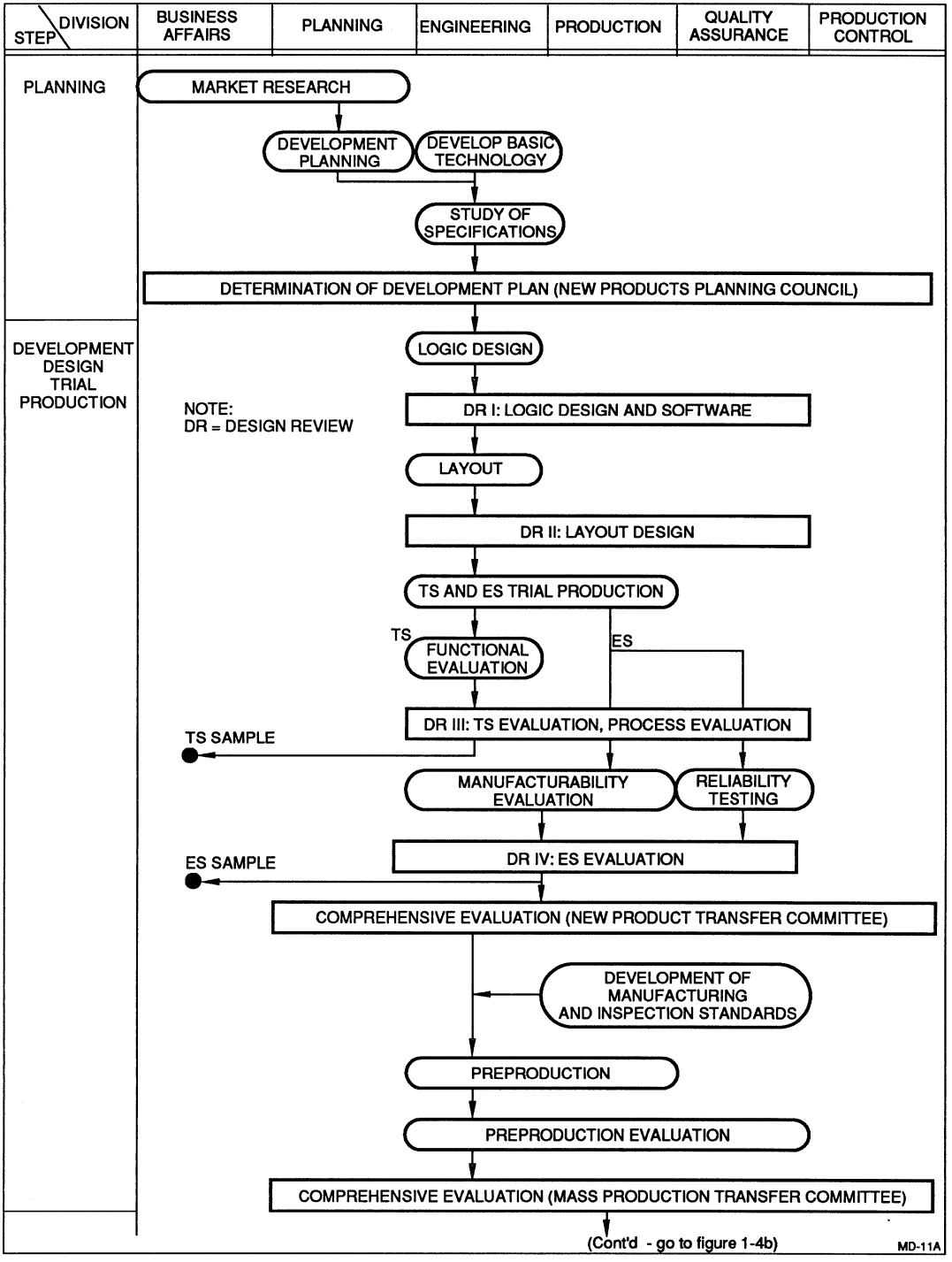


Figure 4a. Quality Assurance System

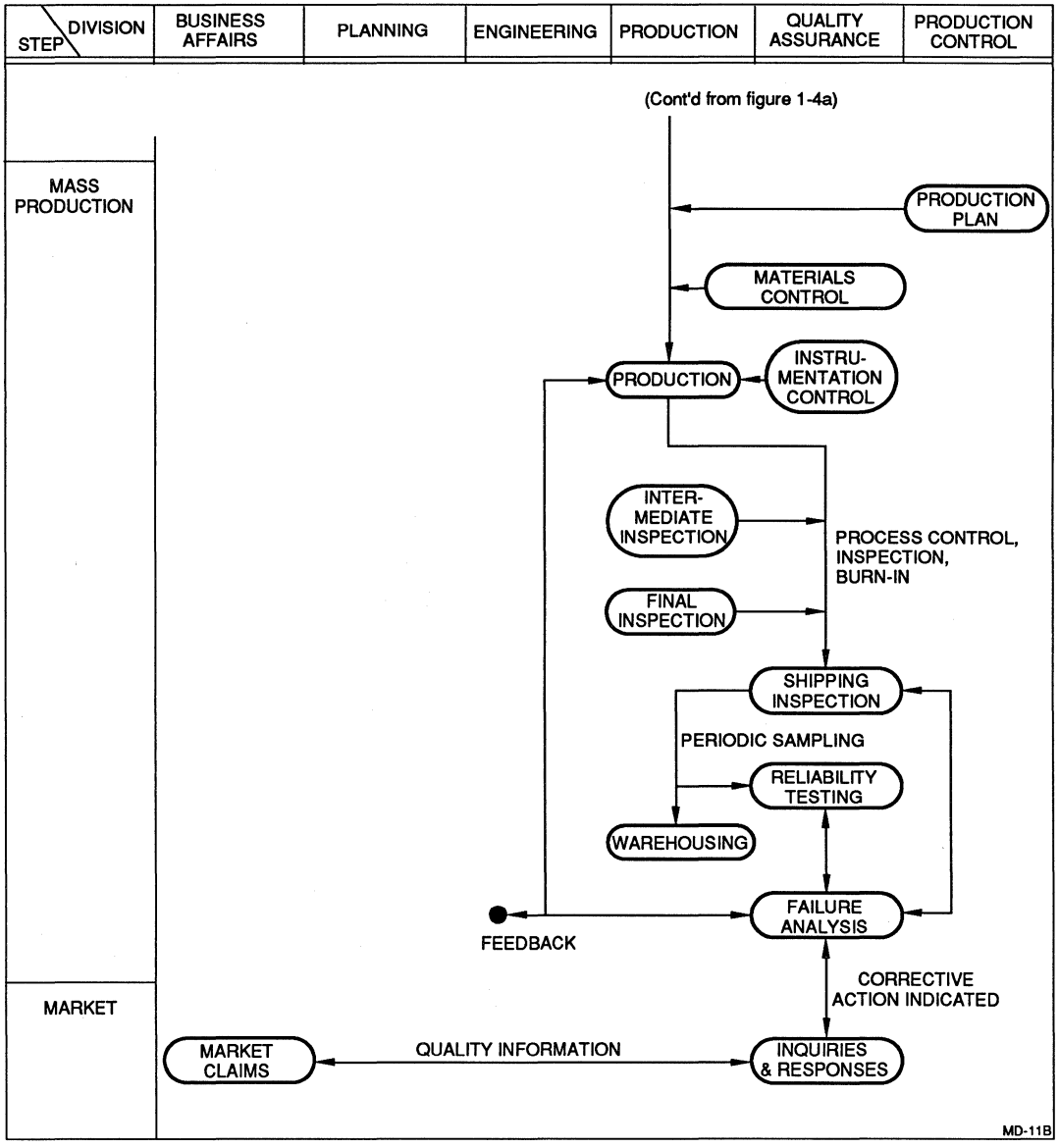


Figure 4b. Quality Assurance System

Reliability Tests

Reliability Test Methods

Reliability tests should always have good reproducibility. Thus, reliability tests for IC devices are based on standardized test methods. Such uniform testing standards include those established by JIS (Japanese Industrial Standard), MIL (U.S. MILitary Standard), EIAJ (Electronic Industries Association of Japan) and IEC (International Electrotechnical Commission). As indicated in ***Table 2***, however, Sharp has established its own testing method based on these standards.

Advances in semiconductor device technology are astonishing, and they call for higher quality and reliability standards. Improved failure analysis techniques are therefore necessary to ensure semiconductor device reliablity.

The causes of semiconductor device failure are becoming increasingly diverse. This diversity is the result of element and interconnect miniaturization required for higher integration. It is also due to an increasingly complex manufacturing process with an increased number of steps from the wafer fabrication process to the assembly process.

Failure analysis is the use of human, physical and electrical analytical procedures to clarify the failure mechanisms of defective parts. It is used to evaluate defective items appearing throughout the life of parts: during the semiconductor manufacturing process, outgoing inspections and reliability testing; during the user's incoming inspections, processing and reliability testing; and during operation in the field.

The ultimate goal of failure analysis is to prevent the recurrence of failure. It is necessary to establish various measures based on the results of failure analysis and to feed those measures back to the manufacturing process and product users.

Sharp has an on-going program of supplying users with our own quality data, reliability test data, etc., upon request. It is just one of Sharp's efforts to maintain a high degree of user service. ***Figure 5*** illustrates Sharp's Quality Information Routes.

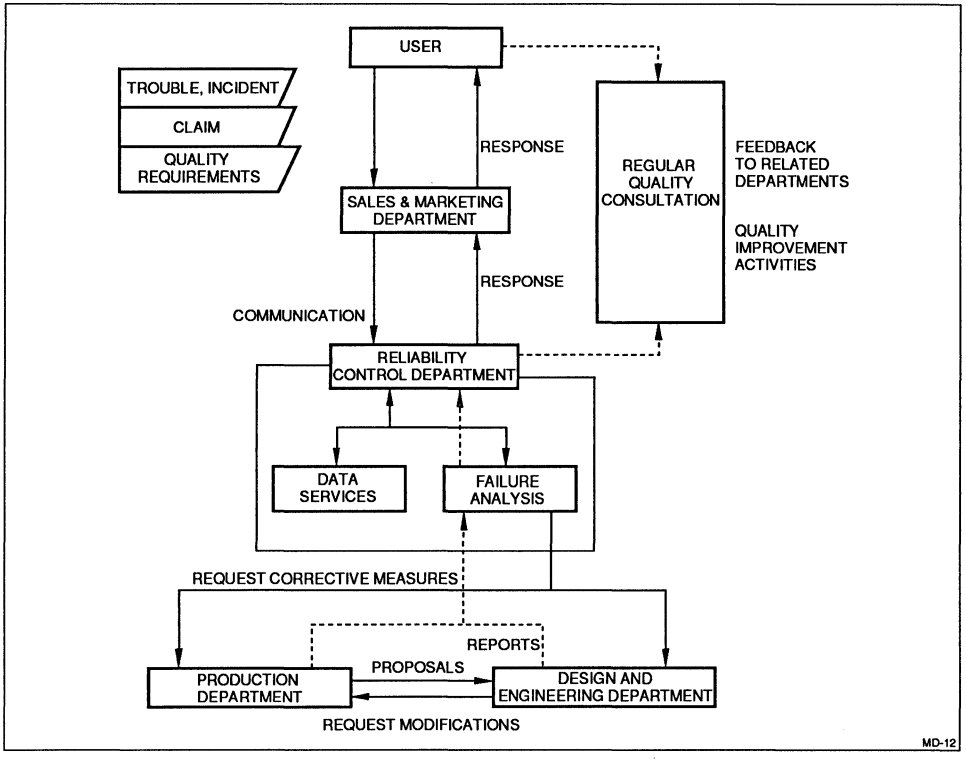


Figure 5. Routes through which malfunctions outside the company are handled.

Handling Precautions

All the semiconductor products listed in this data book are manufactured based on exacting designs and under comprehensive quality control. However, to take full advantage of the features offered and to assure each products' long-life service, please refer to the following items.

Maximum Ratings

It is generally known that the failure rate of semiconductor products increases as the temperature increases. It is therefore necessary that the ambient temperature be within the maximum rated temperature. Further, it is desirable from the stand-point of reliability that the ambient temperature be lowered as much as possible. The voltage, current, and electric power used are also factors that significantly influence the life of semiconductor products. Voltage or current that exceeds the rated level may damage the semiconductor product; even if applied only momentarily and the unit continues to operate properly, excessive voltage or current will likely increase the failure rate.

Therefore, in actual circuit design, it is important that the semiconductor products have an allowance with respect to the voltage, current and temperature conditions under which they will be used. The greater this allowance, the fewer the failures that will occur.

To keep failures to a minimum, the circuit should be designed so that under all conditions to absolute maximum, the ratings are not exceeded even momentarily and so that the maximum values for any two or more items are not achieved simultaneously. In addition, remember that the circuit functions of semiconductor products are guaranteed within the operating temperature range (Topr) or the absolute maximum ratings, but that storage temperature (Tstg) is the range in a nonoperating condition.

Storage Precautions

General Storage Precautions

a. Storing product in the packing in which it is shipped is recommended. If transferred to a different container, use one that will not readily carry an electrostatic charge.

b. Store at conditions of normal temperature (5 - 35°C) and normal humidity (45 - 75% RH).

c. Avoid storing product in the presence of corrosive gases or dusty areas.

d. Avoid storing product in areas of direct sunlight or where sudden temperature changes will occur.

e. Avoid stacking product or otherwise applying heavy loads.

f. In the case of extended storage, take particular care against corrosion and deterioration in lead solderability. Inspecting such product before use is recommended.

Basic Electrostatic Discharge Countermeasures

Semiconductor device mounting requires exacting precautions to avoid applying excessive static electricity to the semiconductor. Item (a) - (c) below are basic electrostatic discharge countermeasures.

a. Use humidifiers and the like to ensure against excessively low relative humidity in the work environment. (Maintaining relative humidity consistently above 50% is ideal).

b. To prevent sudden electrostatic discharge, spread high-resistance electroconductive mats (about $10^6\Omega$) over workbenches and have workers wear wrist (ground) straps.

Have workers wear clothing made of charge-resistant cotton, noncharging materials (10^9 - $10^{14}\Omega$) or static electricity dissipating materials (10^5 - $10^9\Omega$). Anti-static foot apparel is also effective.

c. Ionizers (ionized air blowers) are effective when it is difficult to discharge static electricity from mounting equipment, contacting dielectrics and semiconductors.

Sharp recommends using static electricity measuring devices to quantify electrostatic charges and develop effective countermeasures.

When forming the lead wires of semiconductor products to be mounted, forceps or a similar tool that will prevent stress from being applied to the base of the wires should be used.

To prevent the input terminals of semiconductor products on completed printed circuit boards from becoming open during storage or transport, the terminals of the circuit board should be shortcircuited or the entire circuit board itself should be wrapped in aluminium foil.

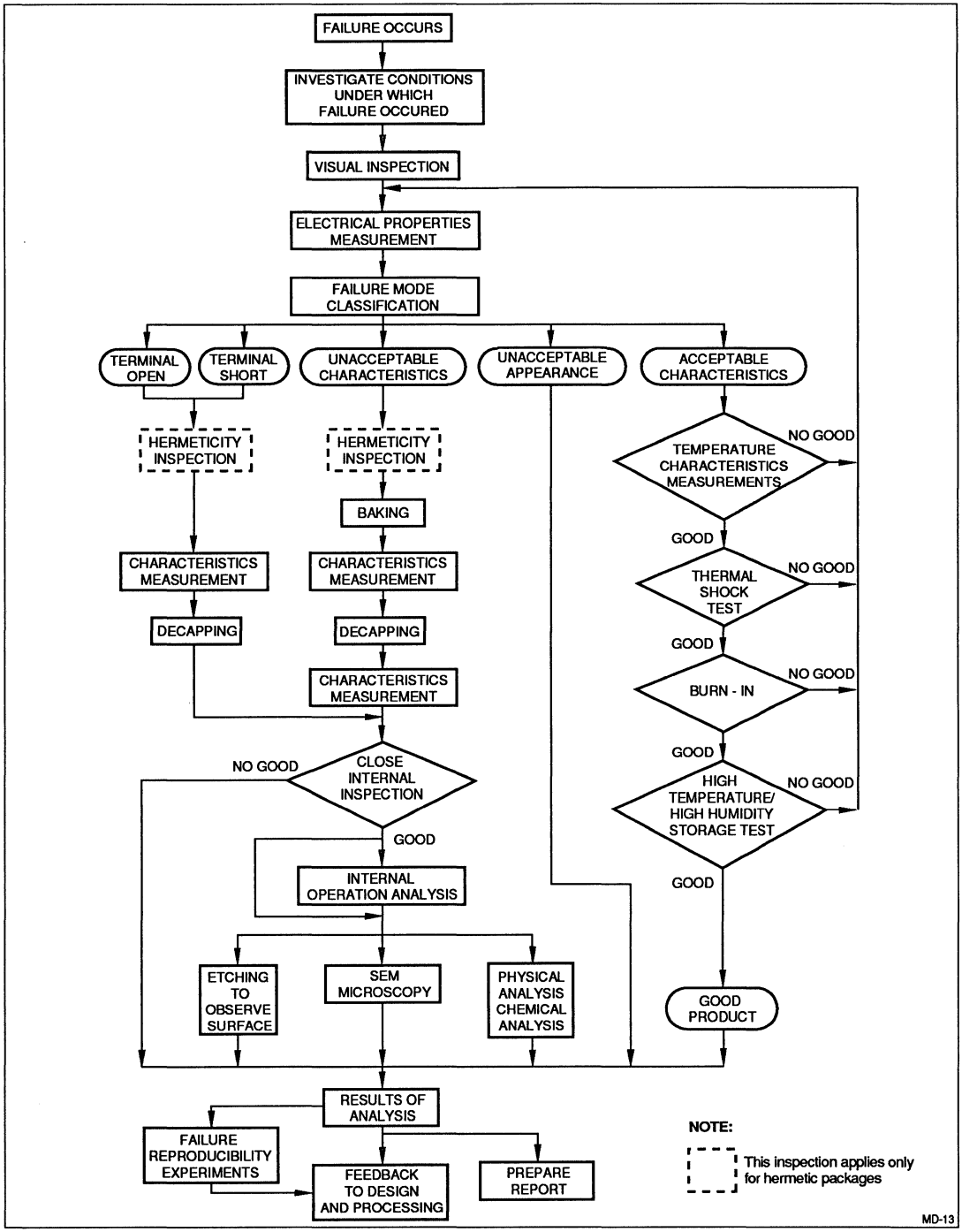


Figure 6. Failure Analysis Procedure

Soldering and Cleaning

When a semiconductor product is solder-bonded, specify the best conditions according to ***Table 4.*** If using a soldering iron, use one that doesn't leak from the soldering tip. An 'A Class' soldering iron with an insulation resistance of less than 10 MΩ is recommended. When using a solder bath, it should be grounded to prevent an unstable electric potential.

Using a strongly acidic or alkaline flux for soldering can cause corrosion of the lead wires. A rosin flux is ideal for this type of soldering.

To assure the reliability of a system, removal of the solder flux is generally required.

To prevent stress of semiconductor products and circuit boards when using ultrasonic cleaning, a cleaning method must be used that will shadow the main unit from the vibrator and specify the best conditions according to the following:

Table 3.
Recommended Conditions for PC Board Cleaning

Ultrasonic Power	less than 25 W/l
Cleaning Conditions	less than one minute total
Cleaning Solution Temperature	15 to 40°C

Adjustment and Tests

When the set is to be adjusted and tested upon completion of the printed circuit board, the printed circuit board must be checked to ensure that there are no solder bridges or cracks before the power is turned on. Also, if the market-rated voltage and current are to be used, it is wise to use a current limiter.

Whenever a printed circuit board is to be removed or mounted, or mounted on a socket, the power must be turned off.

When testing with a probe, care must be taken to assure that the probe does not come in contact with other signals or the power supply. If the test location has been decided beforehand, it is wise to set up a specially designed test-pin for testing.

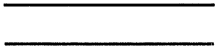
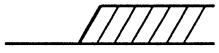
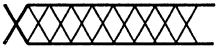
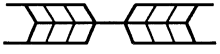
When testing in high and low temperatures, the constant-temperature bath must be grounded and measures taken to protect the set inside the bath from static electricity.

Table 4 outlines the semiconductor bonding and testing methods.

Table 4.
Semiconductor Bonding and Testing Methods

BONDING METHOD	TEMPERATURE AND TIME	TEST POSITION
Infrared reflow	Peak temp. 240°C or less 230°C or more within 15 sec. Heating speed: 1 to 4°C/sec.	Surface IC package
Flow dipping	245°C or less Within 3 sec./cycle Within 5 sec. in total	Solder bath
VPS	215°C or less 250°C or less, within 40 sec.	Steam
Hand soldering	260°C or less, within 10 sec.	IC outer lead

TIMING DIAGRAM CONVENTIONS

TIMING DIAGRAM	INPUT FUNCTIONS	OUTPUT FUNCTIONS
	HIGH or LOW	HIGH or LOW
	HIGH-to-LOW transitions allowed	HIGH-to-LOW transitions during designated interval
	LOW-to-HIGH transitions allowed	LOW-to-HIGH transitions during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Centerline is high-impedance

MD-14

LH21256/7/8

NMOS 256K (256K × 1) Dynamic RAM

FEATURES

- 262,144 × 1 bit organization
- Access times: 100/120/150 ns (MAX.)
- Cycle times: 200/230/260 ns (MIN.)
- Page mode operation (LH21256)
  Nibble mode operation (LH21257)
  Byte mode operation (LH21258)
- Power supply: +5 V ± 10%
- Power consumption:
  Operating: 440/440/385 mW (MAX.)
  Standby: 27.5 mW (MAX.)
- TTL compatible I/O
- Built-in gated $\overline{CAS}$ function
- Separate I/O allows Early-Write action
- Available for read modify write $\overline{RAS}$ only refresh, hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output bias generator circuit
- Packages:
  16-pin, 300-mil DIP
  16-pin, 325-mil ZIP

DESCRIPTION

The LH21256/7/8 is a 262,144 word × 1 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With mulitiplexed address inputs and standard 16-pin DIP/ZIP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH21256/7/8 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

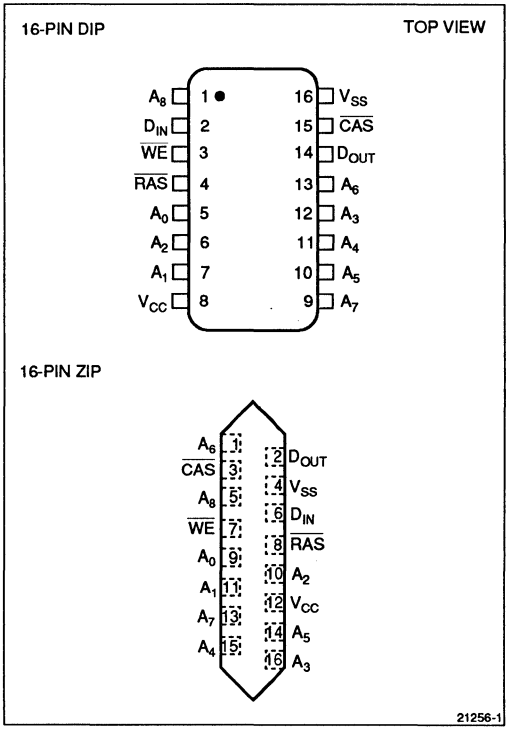


Fig. 1. Pin Connections for DIP & ZIP Packages

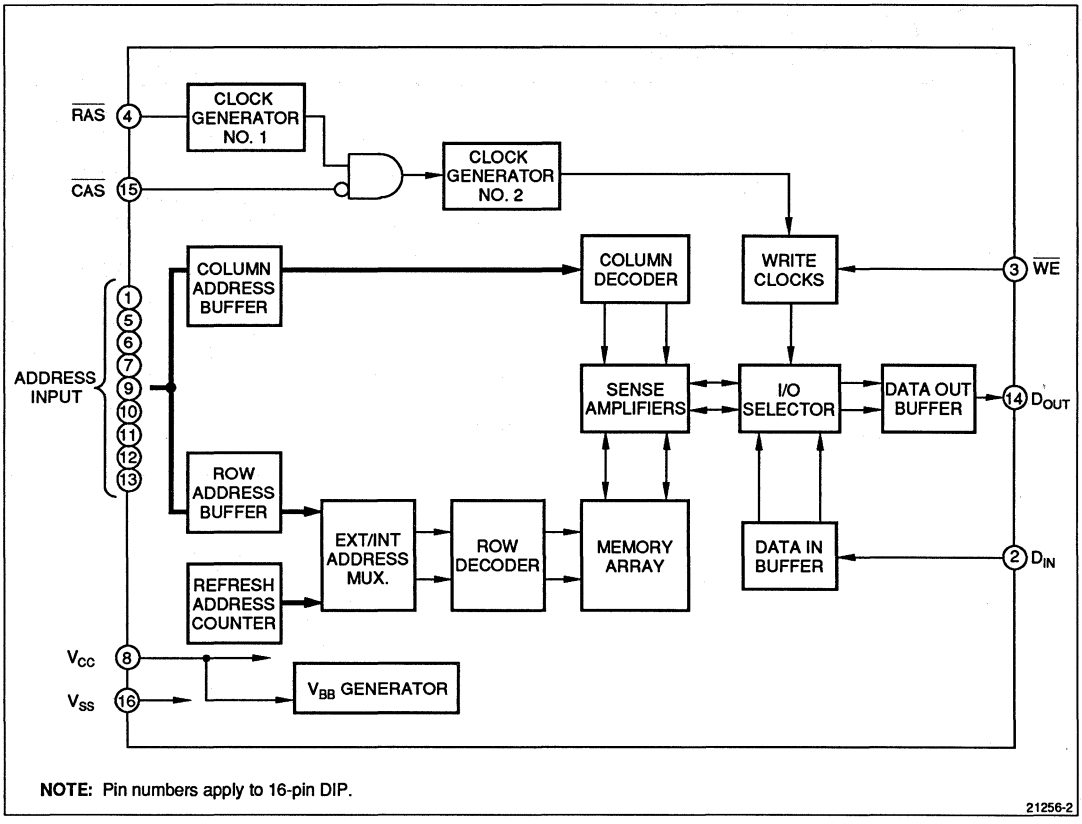


Figure 2. LH21256/7/8 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_8	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
D_{IN}	Data input
D_{OUT}	Data output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to 7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		

NOTE:
1. Referenced to V_{SS}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYPICAL	MAX.	UNIT
Input capacitance	A_0 - A_8, D_{IN}, $\overline{WE}$	C_{IN1}			5	pF
	$\overline{RAS}$, $\overline{CAS}$	C_{IN2}			7	pF
Output capacitance	D_{OUT}	C_{OUT}			7	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH21256/7/8-10	I_{CC1}	—	80	mA	1, 2
	LH21256/7/8-12		—	80		
	LH21256/7/8-15		—	70		
Average supply current in standby mode		I_{CC2}	—	5.0	mA	1
Average supply current in $\overline{RAS}$ only refresh time	LH21256/7/8-10	I_{CC3}	—	60	mA	1, 2
	LH21256/7/8-12		—	60		
	LH21256/7/8-15		—	55		
Average supply current in page mode	LH21256-10	I_{CC4}	—	50	mA	1, 2
	LH21256-12		—	45		
	LH21256-15		—	40		
Average supply current in nibble mode	LH21257-15	I_{CC4}	—	65	mA	1, 2
	LH21257-10		—	49		
	LH21257-12		—	49		
Average supply current in byte mode	LH21258-10	I_{CC4}	—	60	mA	1, 2
	LH21258-12		—	55		
	LH21258-15		—	50		
$\overline{CAS}$ before $\overline{RAS}$ average supply current in refresh cycle	LH21256/7/8-10	I_{CC5}	—	65	mA	1, 2
	LH21256/7/8-12		—	60		
	LH21256/7/8-15		—	55		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	$I_{I(L)}$	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	$I_{O(L)}$	-10	10	µA	
Output "High" voltage	I_{OUT} = -5 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on the cycle time.

AC CHARACTERISTICS[1, 2, 3] (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	LH21256/7/8-10		LH21256/7/8-12		LH21256/7/8-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	t_{RC}	200	—	230	—	260	—	ns	
Read write cycle time	t_{RWC}	240	—	275	—	310	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	5, 6
Output turn-off delay time	t_{OFF}	0	30	0	35	0	40	ns	
Rise and fall time	t_T	3	35	3	35	3	35	ns	3
$\overline{RAS}$ precharge time	t_{RP}	85	—	100	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	25	—	30	—	35	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ set up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	10	—	10	—	30	—	ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	30	75	ns	7, 8
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	30	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	25	—	25	—	45	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	—	90	—	120	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	11
Read command hold time from $\overline{RAS}$	t_{RRH}	10	—	10	—	20	—	ns	11
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	35	—	40	—	45	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	85	—	100	—	120	—	ns	
Write command pulse width	t_{WP}	35	—	40	—	45	—	ns	
Write command $\overline{RAS}$ read time	t_{RWL}	35	—	40	—	45	—	ns	
Write command $\overline{CAS}$ read time	t_{CWL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ write command delay time	t_{RWD}	95	—	120	—	150	—	ns	
$\overline{CAS}$ write command delay time	t_{CWD}	45	—	60	—	75	—	ns	
Data input setup time	t_{DS}	0	—	0	—	0	—	ns	9
Data input hold time	t_{DH}	30	—	30	—	35	—	ns	9
Data input hold time from $\overline{RAS}$	t_{DHR}	80	—	90	—	110	—	ns	
Refresh time	t_{REF}	—	4	—	4	—	4	ms	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

NOTES:

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristics assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. Only when $t_{RCD} \leq t_{RCD}$ (MAX.). If $t_{RCD} > t_{RCD}$ (MAX.), t_{RAC} will increase by (t_{RCD} - t_{RCD} (MAX.))
5. When $t_{RCD} \geq t_{RCD}$ (MAX.).
6. Load condition for 2TTL + 100 pF.
7. t_{RCD} (MAX.) is the maximum point for t_{RCD} where t_{RAC} (MAX.) is ensured, and does not represent a limit of operation. If t_{RCD} (MAX.) ≤ t_{RCD}, the access time is controlled by t_{CAC}.
8. t_{RCD} (MIN.) = t_{RAH} (MIN.) + 2t_T + t_{ASC} (MIN.).
9. t_{DS} and t_{DH} are given with respect to the fall of $\overline{CAS}$ in the Early-Write cycle and fall of $\overline{WE}$ in the read/write cycle and the Read-Modify-Write cycle.
10. t_{WCS}, t_{CWD} and t_{RWD} are the specified points of the operating mode, and do not represent a limit of operation. When $t_{WCS} \geq t_{WCS}$ (MIN.), it comes into early write cycle with D_{OUT} pin coming into high-impedance state. When $t_{CWD} \geq t_{CWD}$ (MIN.) and $t_{RWD} \geq t_{RWD}$ (MIN.), it comes into the read/write cycle with the output data becoming the information for the selection cell. Timing other than the above-mentions will give undefined value of output.
11. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.

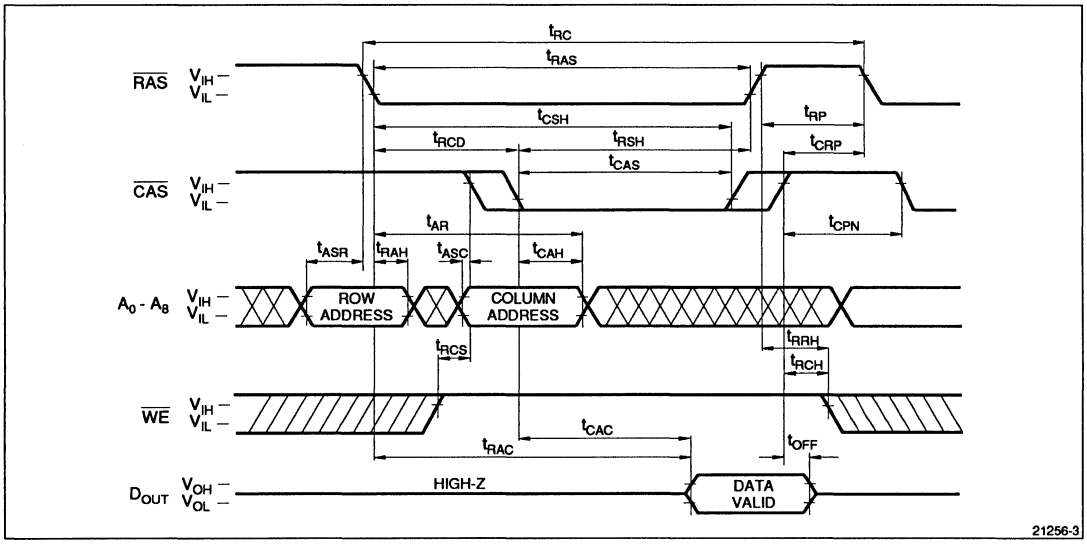


Figure 3. Read Cycle

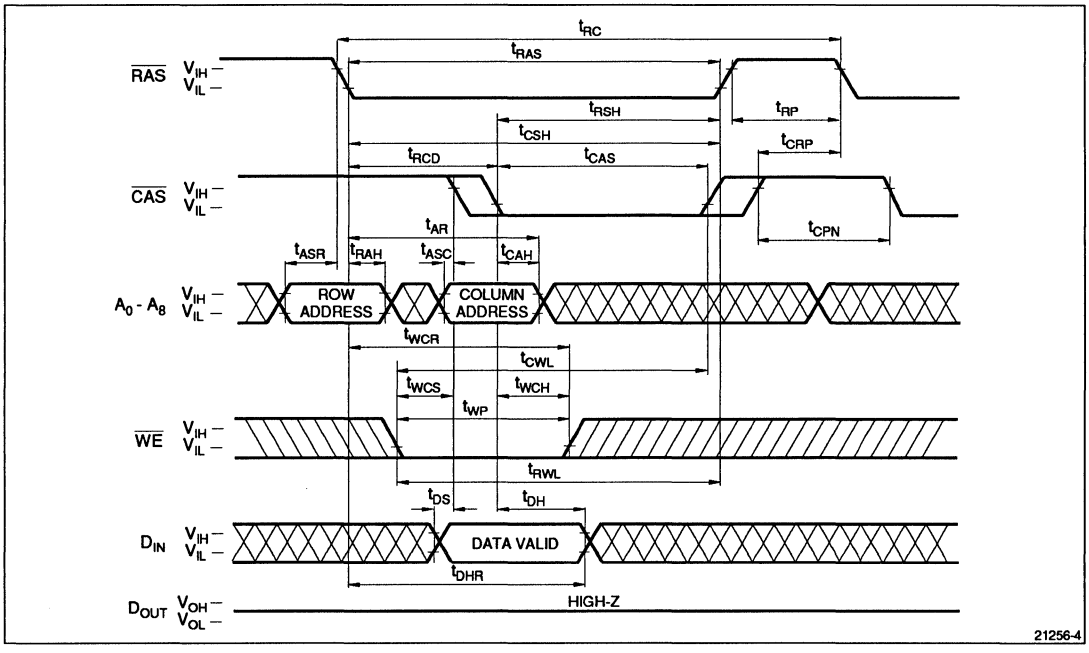


Figure 4. Write Cycle (Early Write)

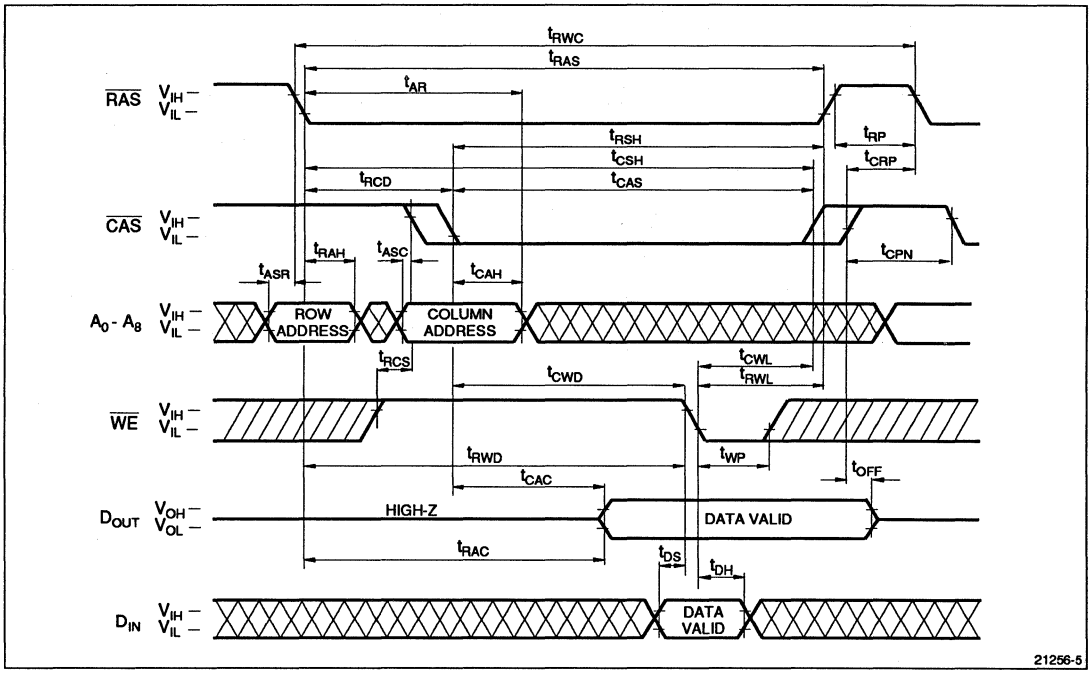


Figure 5. Read-Write/Read-Modify-Write Cycle

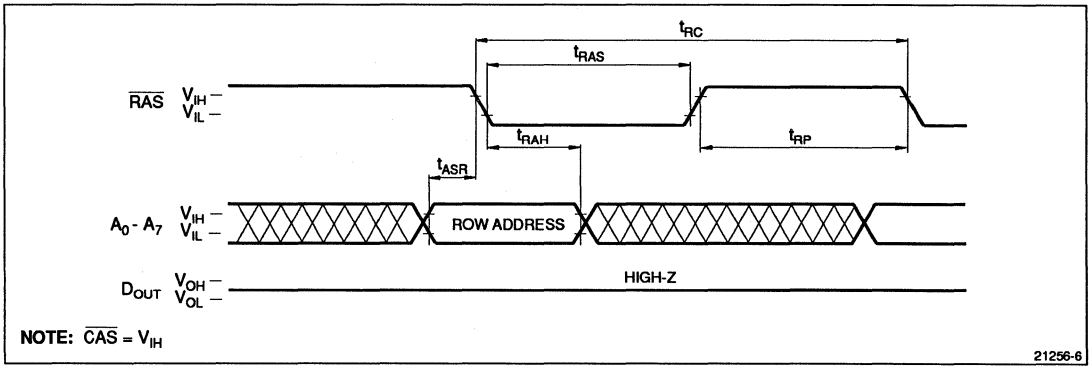


Figure 6. $\overline{RAS}$ Only Refresh Cycle

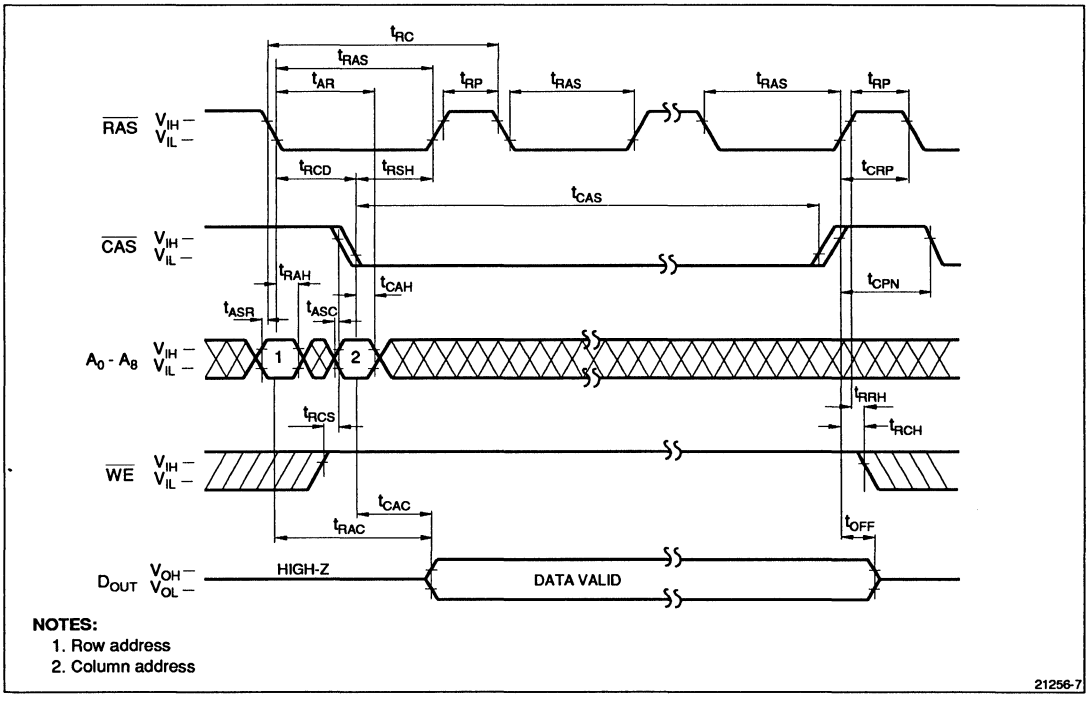


Figure 7. Hidden Refresh Cycle

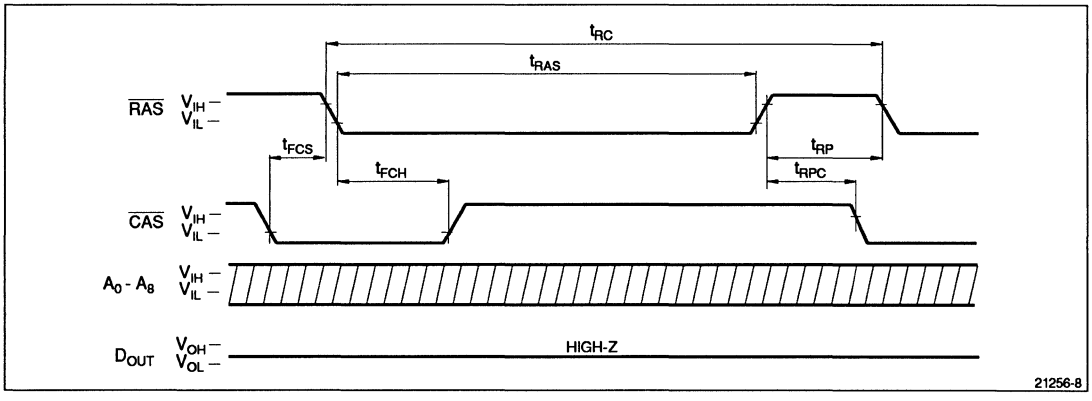
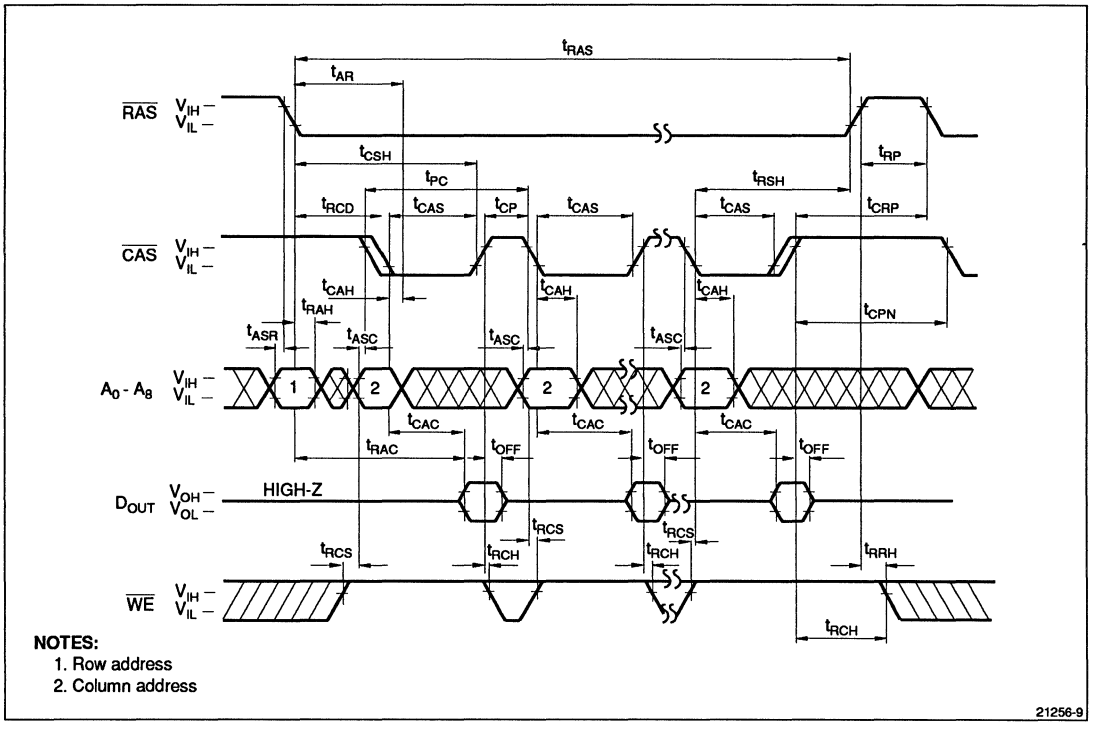


Figure 8. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

PAGE MODE CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH21256-10		LH21256-12		LH21256-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Page mode cycle time	t_{PC}	100	—	120	—	145	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	40	—	50	—	60	—	ns	



NOTES:
1. Row address
2. Column address

21256-9

Figure 9. Page Mode Read Cycle

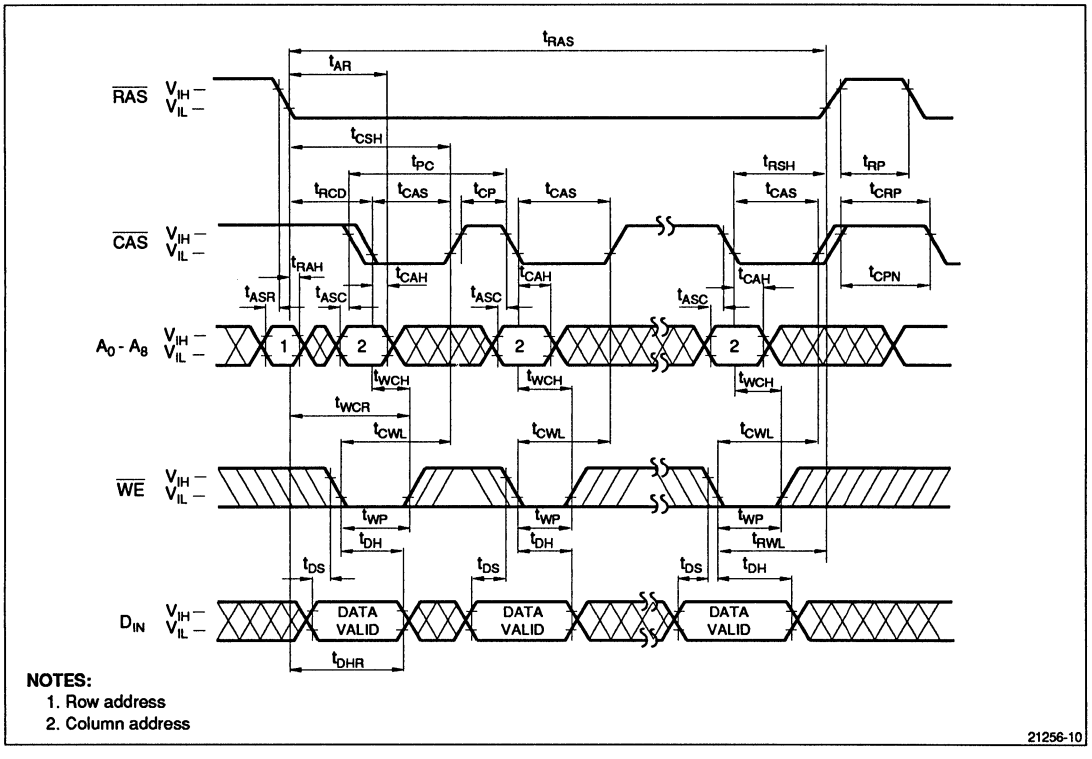
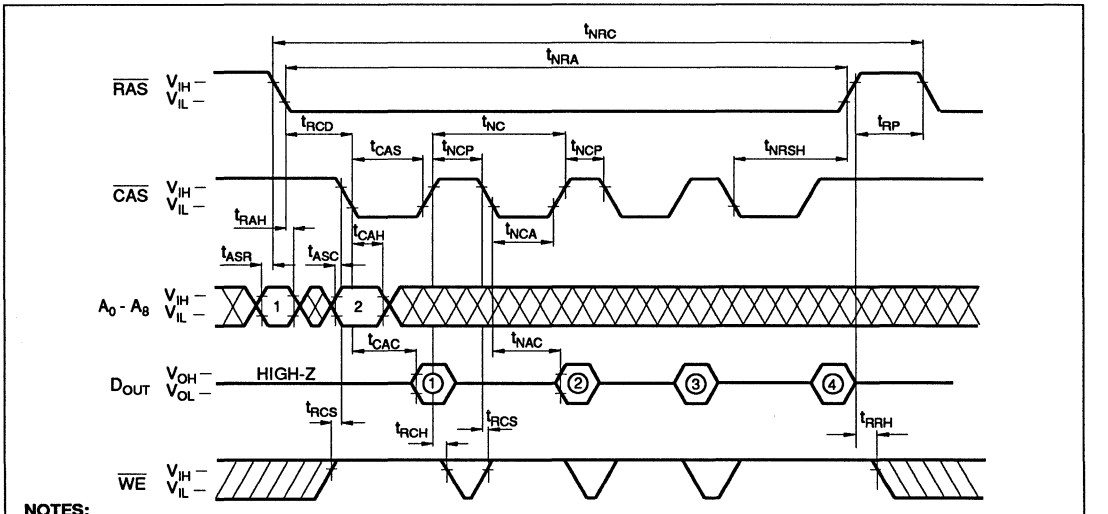


Figure 10. Page Mode Write Cycle

NIBBLE MODE CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH21257-10		LH21257-12		LH21257-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Nibble mode access time	t_{NAC}	—	25	—	30	—	35	ns	
Nibble mode $\overline{RAS}$ cycle time	t_{NRC}	400	—	460	—	520	—	ns	
Nibble mode $\overline{RAS}$ pulse width	t_{NRA}	300	—	350	—	410	—	ns	
Nibble mode cycle time	t_{NC}	60	—	65	—	80	—	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	25	—	25	—	35	—	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCA}	25	—	30	—	35	—	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	45	—	50	—	55	—	ns	
Nibble mode $\overline{CAS}$/$\overline{WE}$ delay	t_{NCWD}	15	—	20	—	25	—	ns	
Nibble mode write command $\overline{CAS}$ lead time	t_{NCWL}	20	—	25	—	25	—	ns	
Nibble mode write command $\overline{RAS}$ lead time	t_{NRWL}	40	—	45	—	55	—	ns	
Nibble mode write command pulse width	t_{NWP}	20	—	25	—	35	—	ns	



NOTES:
1. Row address
2. Column address
3. Nibble address: RA8, CA8

①, ②, ③, ④: Valid data-out number

21256-11

Figure 11. Nibble Mode Read Cycle

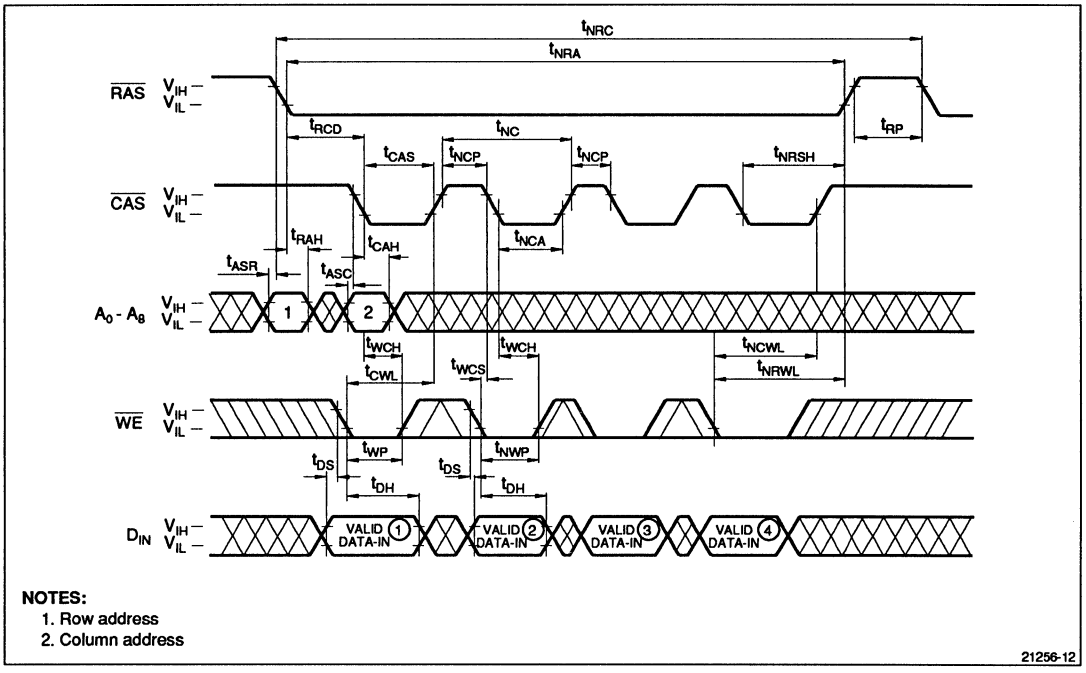


Figure 12. Nibble Mode Write Cycle

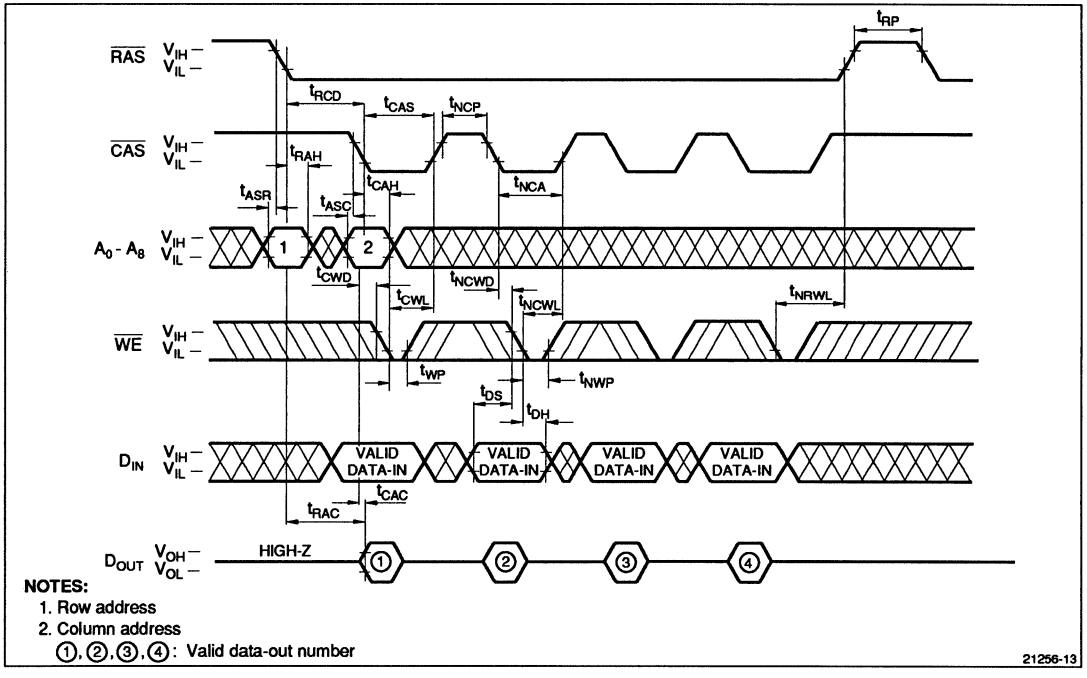


Figure 13. Nibble Mode Read-Modify-Write Cycle

BYTE MODE CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH21258-10		LH21258-12		LH21258-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Byte mode access time	t_{BAC}	—	25	—	30	—	35	ns	
Byte mode $\overline{RAS}$ cycle time	t_{BRC}	640	—	740	—	840	—	ns	
Byte mode $\overline{RAS}$ pulse width	t_{BRA}	540	—	630	—	730	—	ns	
Byte mode cycle time	t_{BC}	60	—	70	—	80	—	ns	
Byte mode $\overline{CAS}$ precharge time	t_{BCP}	25	—	30	—	35	—	ns	
Byte mode $\overline{CAS}$ pulse width	t_{BCA}	25	—	30	—	35	—	ns	
Byte mode $\overline{RAS}$ hold time	t_{BRSH}	45	—	50	—	55	—	ns	
Byte mode $\overline{CAS}$, $\overline{WE}$ delay	t_{BCWD}	15	—	20	—	25	—	ns	
Byte mode write command $\overline{CAS}$ lead time	t_{BCWL}	20	—	25	—	25	—	ns	
Byte mode write command $\overline{RAS}$ lead time	t_{BRWL}	40	—	45	—	55	—	ns	
Byte mode write command pulse width	t_{BWP}	20	—	25	—	35	—	ns	

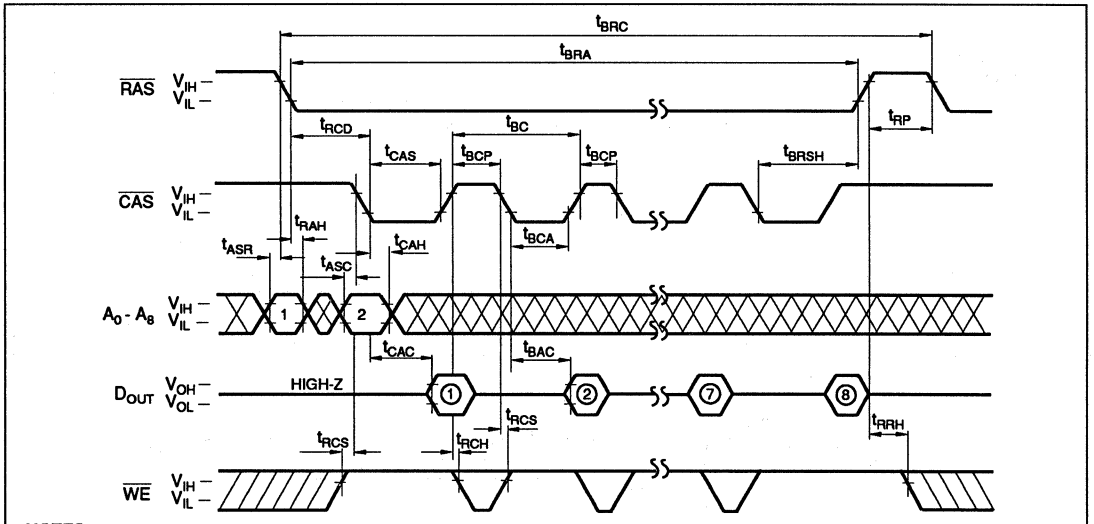
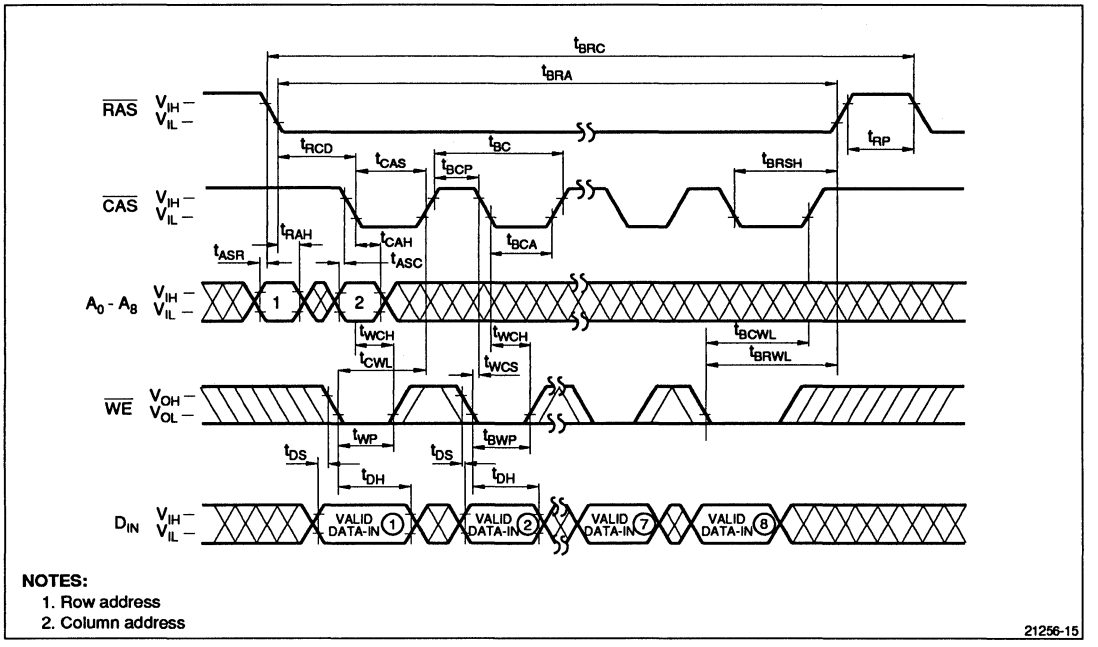


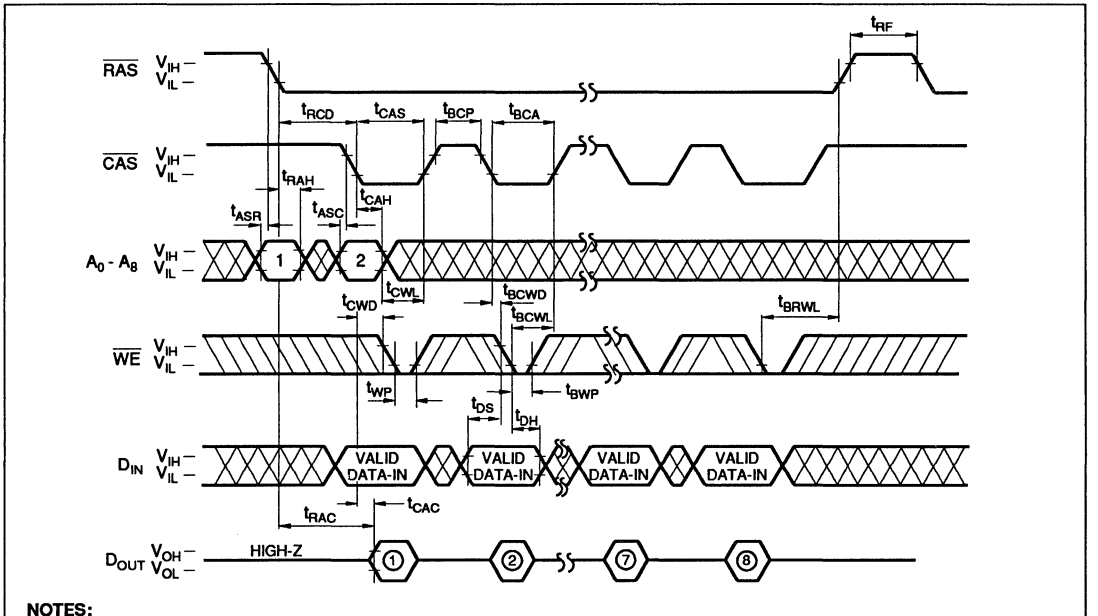
Figure 14. Byte Mode Read Cycle



NOTES:
1. Row address
2. Column address

21256-15

Figure 15. Byte Mode Write Cycle



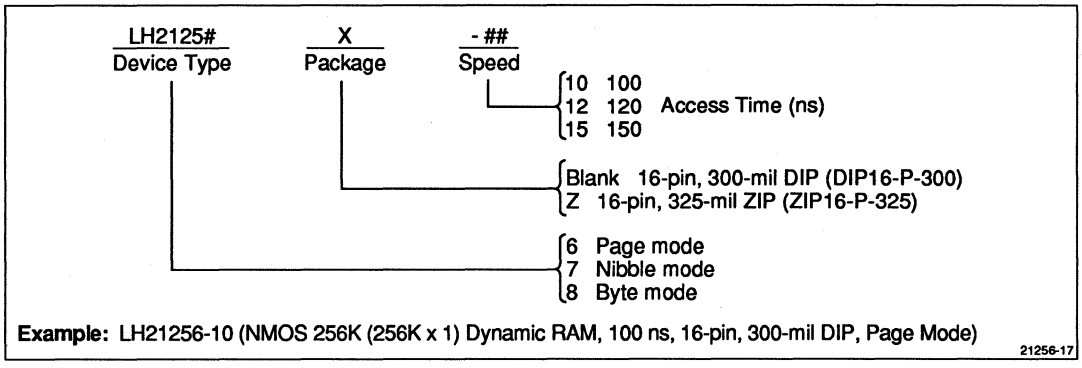
NOTES:
1. Row address
2. Column address

①, ② . . . ⑦, ⑧: Valid data-out number

21256-16

Figure 16. Byte Mode Read-Modify-Write Cycle

ORDERING INFORMATION



Example: LH21256-10 (NMOS 256K (256K x 1) Dynamic RAM, 100 ns, 16-pin, 300-mil DIP, Page Mode)

LH2464

NMOS 256K (64K × 4) Dynamic RAM

FEATURES

- 65,536 × 4 bit organization
- Access times: 100/120/150 ns (MAX.)
- Cycle times: 200/220/260 ns (MIN.)
- Page mode, Read-Modify-Write operation
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
  Operating: 523/457/413 mW (MAX.)
  Standby: 27.5 mW
- TTL compatible I/O
- Built-in gated $\overline{CAS}$ function
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output substrate bias generator circuit
- Package:
  18-pin, 300-mil DIP

DESCRIPTION

The LH2464 is a 65,536 × 4 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With multiplexed address inputs and a standard 18-pin DIP package, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH2464 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

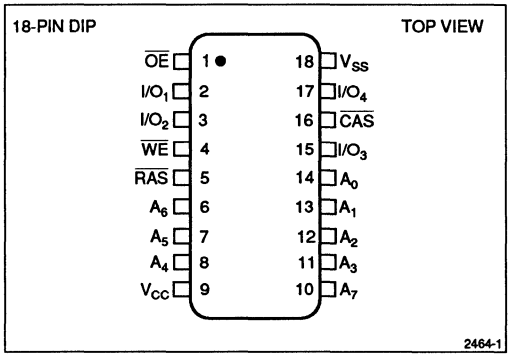


Figure 1. Pin Connections for DIP Package

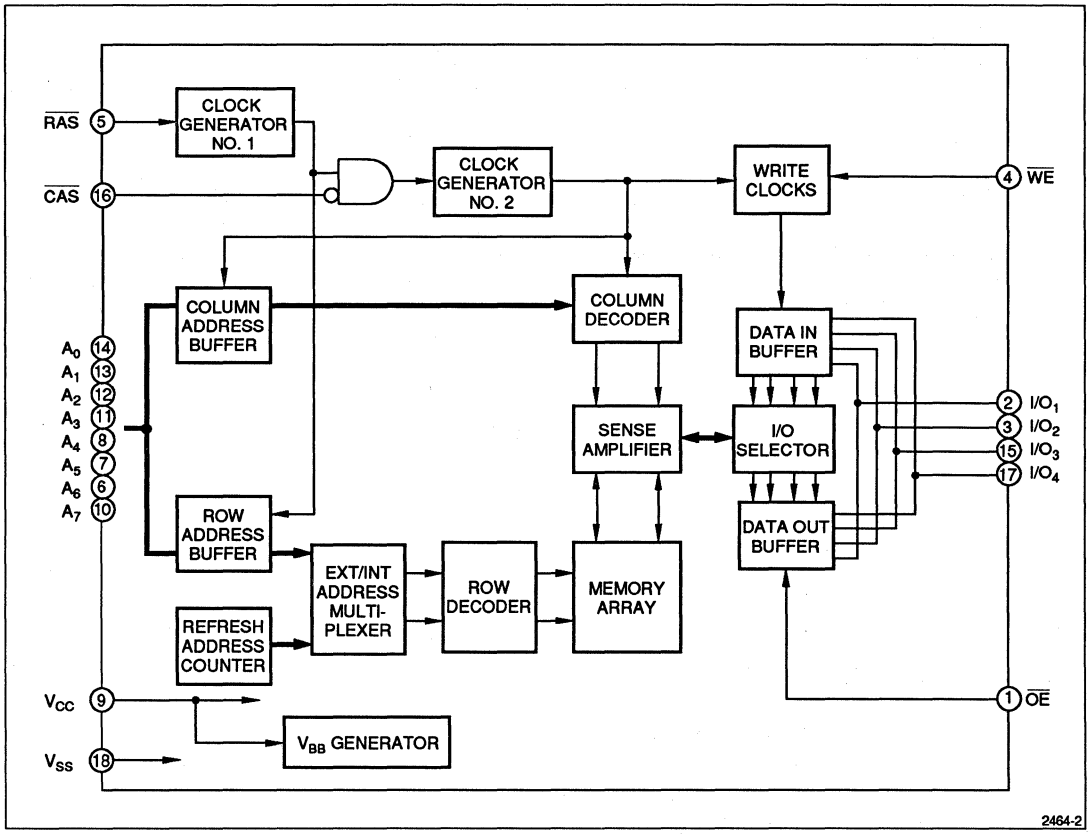


Figure 2. LH2464 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_7	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		

NOTE:
1. Referenced to V_{SS}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	A_0 - A_7	C_{IN1}			5	pF
	$\overline{OE}$, $\overline{WE}$	C_{IN2}			7	
	$\overline{RAS}$, $\overline{CAS}$	C_{IN2}			10	
Input/Output capacitance	I/O_1 - I/O_4	C_{IO}			8	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH2464-10	I_{CC1}	—	95	mA	1, 2
	LH2464-12		—	83		
	LH2464-15		—	75		
Average supply current in the standby mode		I_{CC2}	—	5.0	mA	1
Average supply current in $\overline{RAS}$ only refresh time	LH2464-10	I_{CC3}	—	85	mA	1, 2
	LH2464-12		—	63		
	LH2464-15		—	65		
Average supply current in page mode	LH2464-10	I_{CC4}	—	70	mA	1
	LH2464-12		—	60		
	LH2464-15		—	50		
$\overline{CAS}$ before $\overline{RAS}$ average supply current in refresh cycle	LH2464-10	I_{CC5}	—	85	mA	1, 2
	LH2464-12		—	70		
	LH2464-15		—	65		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	I_{L1}	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	I_{LO}	-10	10	µA	
Output "High" voltage	I_{OUT} = -2 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on the cycle time.

AC CHARACTERISTICS [1, 2, 3] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH2464-10		LH2464-12		LH2464-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	t_{RC}	200	—	220	—	260	—	ns	
Read write cycle time	t_{RWC}	280	—	305	—	360	—	ns	
Page mode cycle time	t_{PC}	100	—	120	—	145	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	5, 6
Output turn off delay time	t_{OFF}	0	30	0	30	0	40	ns	
Rise and fall time	t_T	3	35	3	35	3	35	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	—	60	—	75	—	ns	
Refresh counter test cycle time	t_{RTC}	385		445		520		ns	12
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	285		335		410		ns	12
$\overline{CAS}$ precharge time	t_{CP}	40	—	50	—	60	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	10	—	10	—	30	—	ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	30	75	ns	7, 8
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	30	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	45	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	—	80	—	120	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time from $\overline{RAS}$	t_{RRH}	10	—	10	—	20	—	ns	10
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	9
Write command hold time	t_{WCH}	35	—	40	—	45	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	85	—	100	—	120	—	ns	
Write command pulse width	t_{WP}	35	—	40	—	45	—	ns	
Write command $\overline{RAS}$ lead time	t_{RWL}	35	—	40	—	45	—	ns	
Write command $\overline{CAS}$ lead time	t_{CWL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ write command delay time	t_{RWD}	140	—	160	—	200	—	ns	
$\overline{CAS}$ write command delay time	t_{CWD}	90	—	100	—	125	—	ns	
Data input setup time	t_{DS}	0	—	0	—	0	—	ns	
Data input hold time from $\overline{CAS}$	t_{DHC}	35	—	40	—	45	—	ns	
Data input hold time from $\overline{RAS}$	t_{DHR}	85	—	100	—	120	—	ns	
Refresh interval	t_{REF}	—	4	—	4	—	4	ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{OE}$ command hold time	t_{OEH}	25	—	25	—	40	—	ns	11
$\overline{OE}$ access time	t_{OEA}	—	25	—	30	—	40	ns	
$\overline{OE}$ to data delay	t_{OED}	30	—	30	—	40	—	ns	
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	30	0	30	0	40	ns	
Data input hold time from $\overline{WE}$	t_{DHW}	35	—	40	—	45	—	ns	

NOTES:

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristic assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. Only when $t_{RCD} \leq t_{RCD}$ (MAX.). If $t_{RCD} > t_{RCD}$ (MAX.), t_{RAC} will increase by (t_{RCD} - t_{RCD} (MAX.)).
5. When $t_{RCD} \geq t_{RCD}$ (MAX.).
6. Load condition for 2TTL + 100 pF.
7. t_{RCD} (MAX.) is the max. point fo$_r$ t_{RCD} where t_{RAC} (MAX.) is ensured, and doesn't represent a limit of operation. If t_{RCD} (MAX.) ≤ t_{RCD}, the access time will come under the control of t_{CAC}.
8. t_{RCD} (MIN.) = t_{RAH} (MIN.) + 2t_T + t_{ASC} (MIN.).
9. When $t_{WCS} \geq t_{WCS}$ (MIN.), it comes into early write cycle.
10. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
11. Only when $t_{WCS} < t_{WCS}$ (MIN.), it must be satisfied.
12. Only when in $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle.

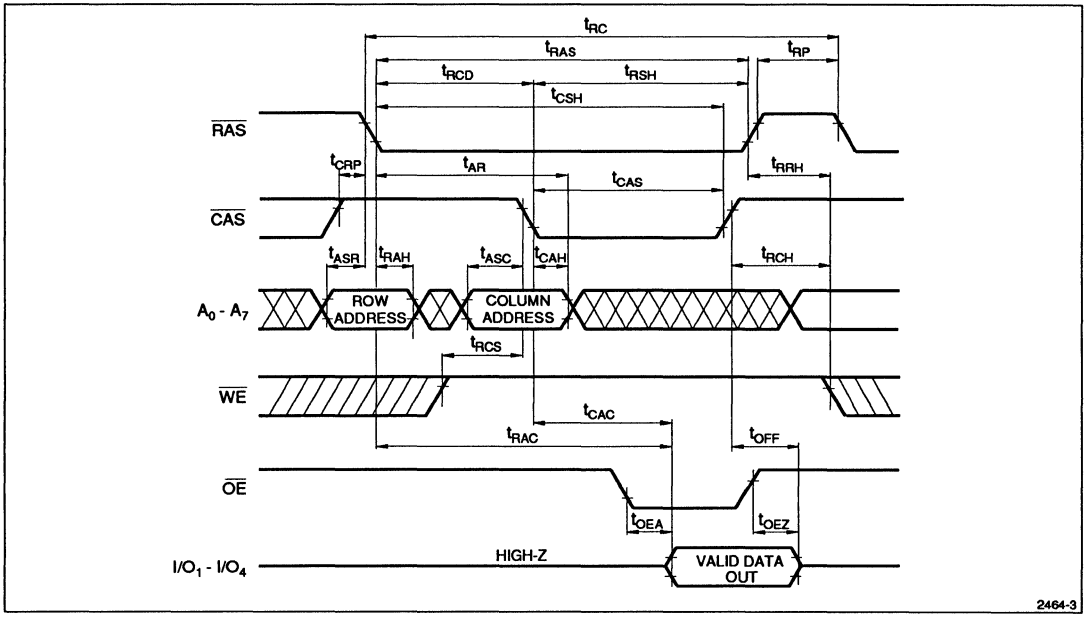


Figure 3. Read Cycle

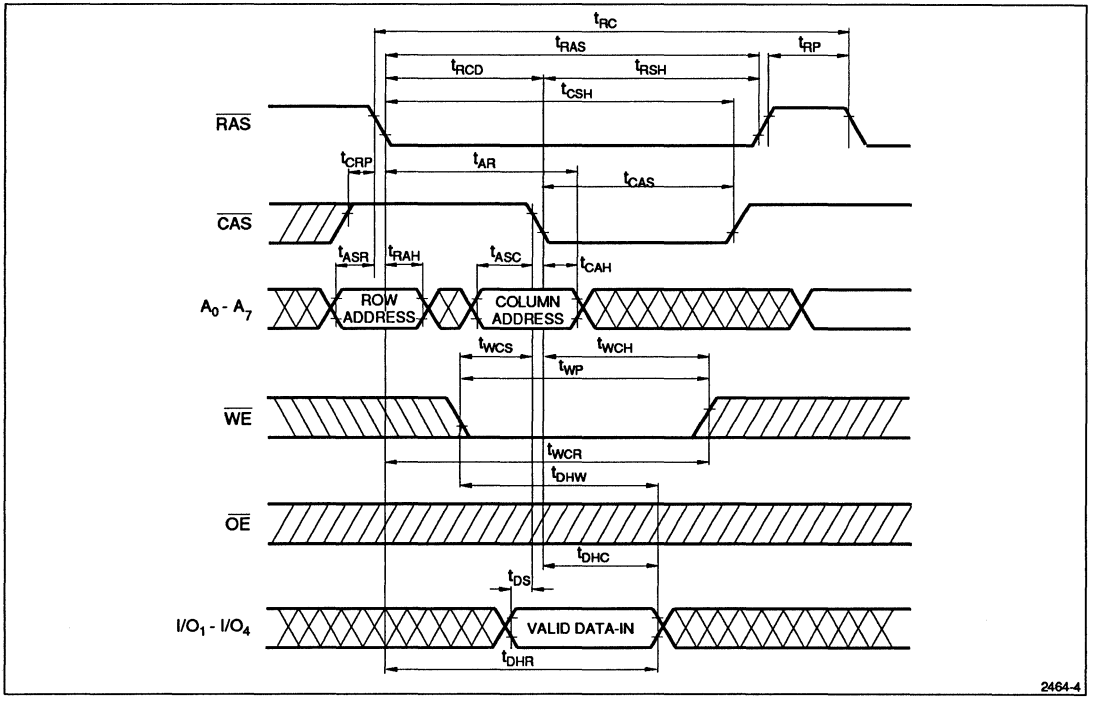


Figure 4. Write Cycle (Early Write)

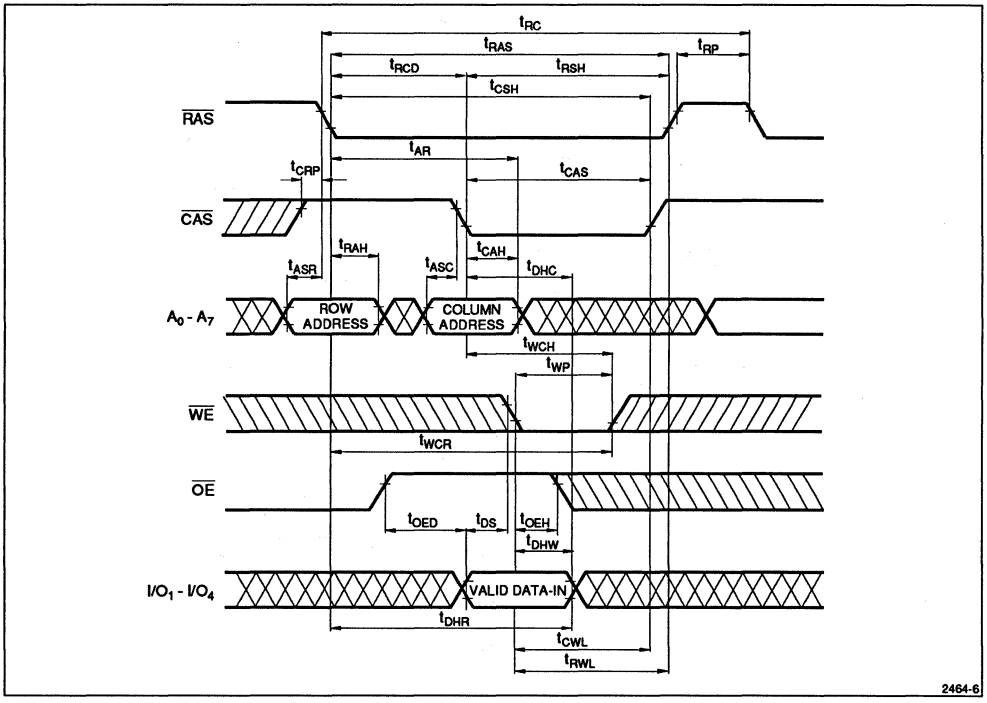


Figure 5. Write Cycle ($\overline{OE}$ Controlled Write)

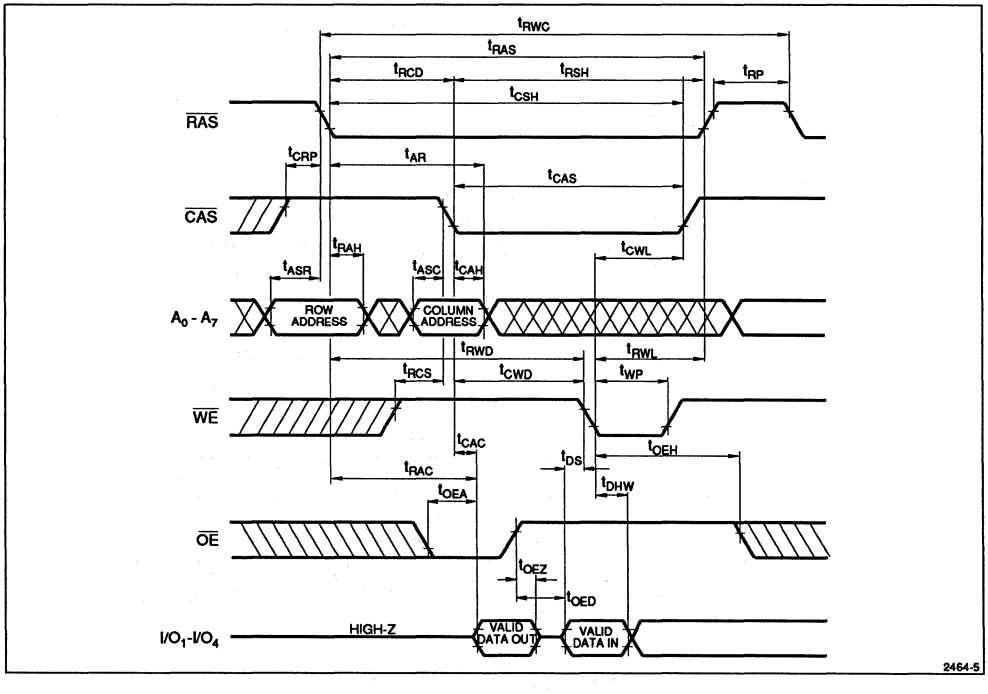


Figure 6. Read-Write/Read-Modify-Write Cycle

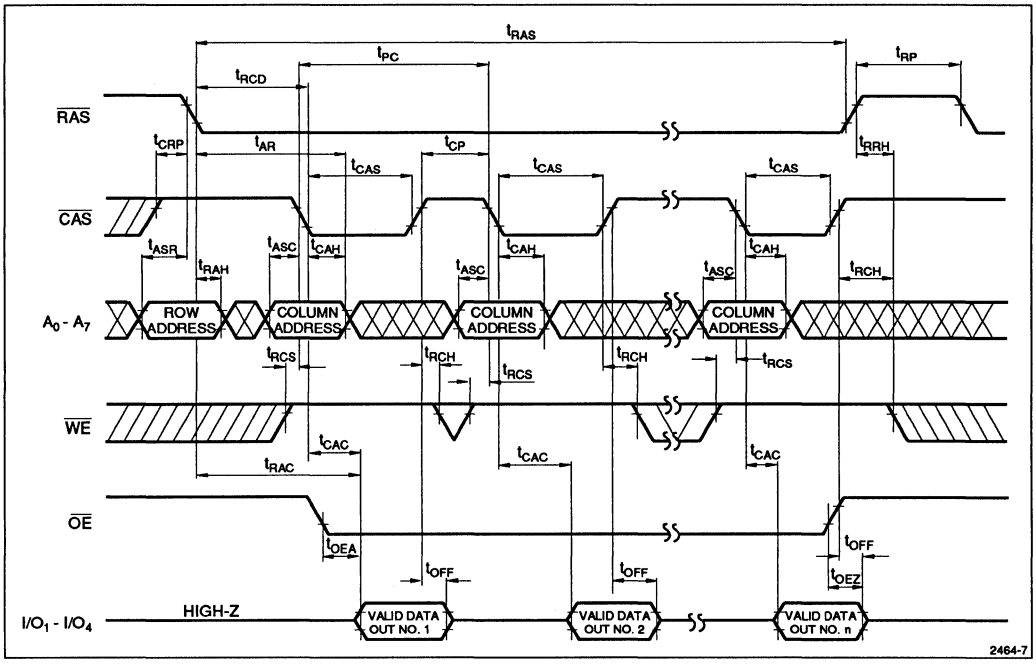


Figure 7. Page Mode Read Cycle

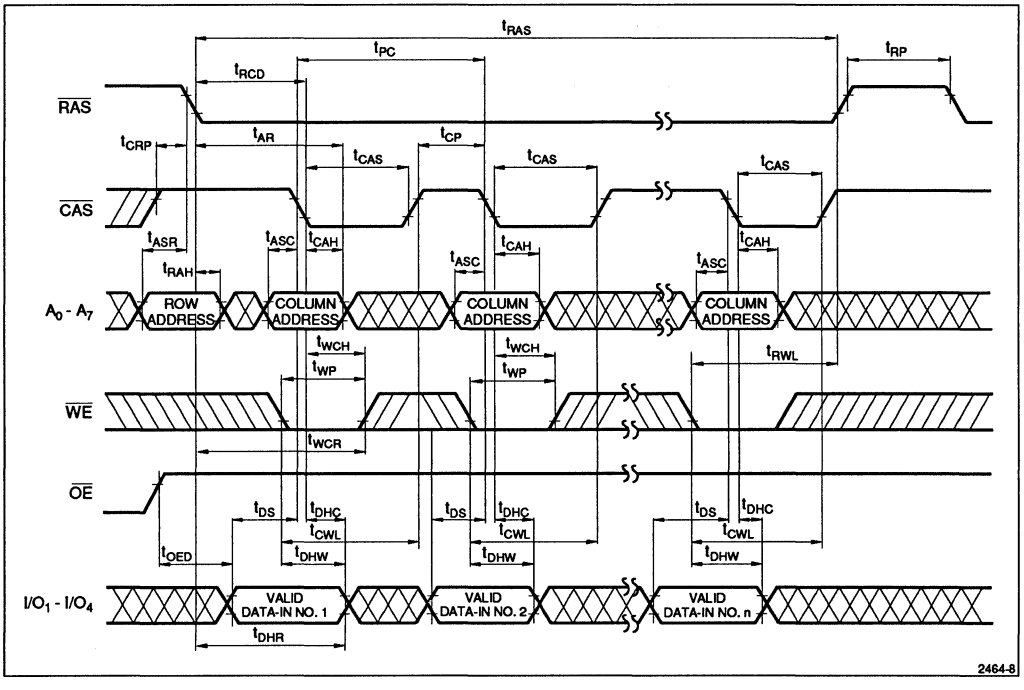


Figure 8. Page Mode Write Cycle

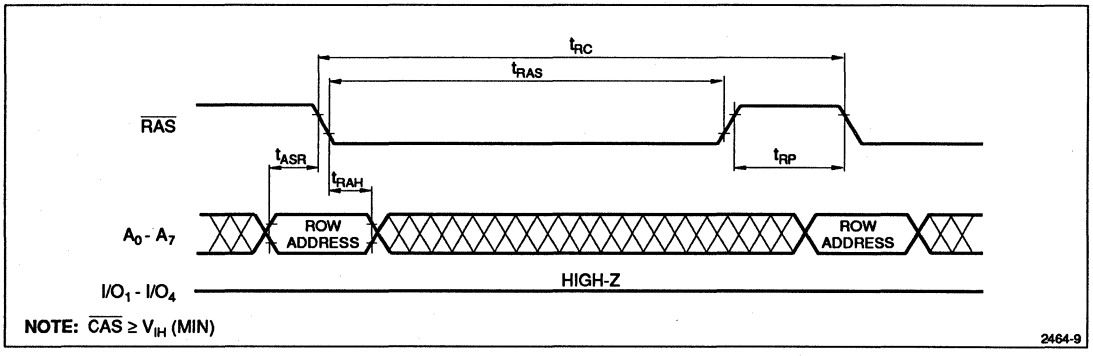


Figure 9. $\overline{RAS}$ Only Refresh Cycle

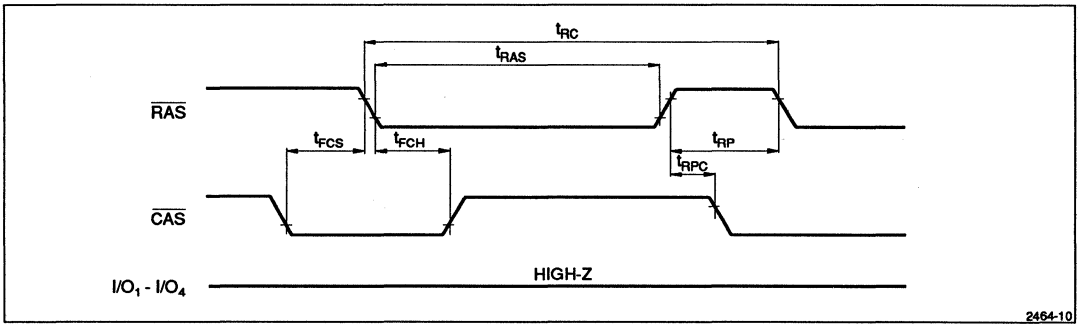


Figure 10. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

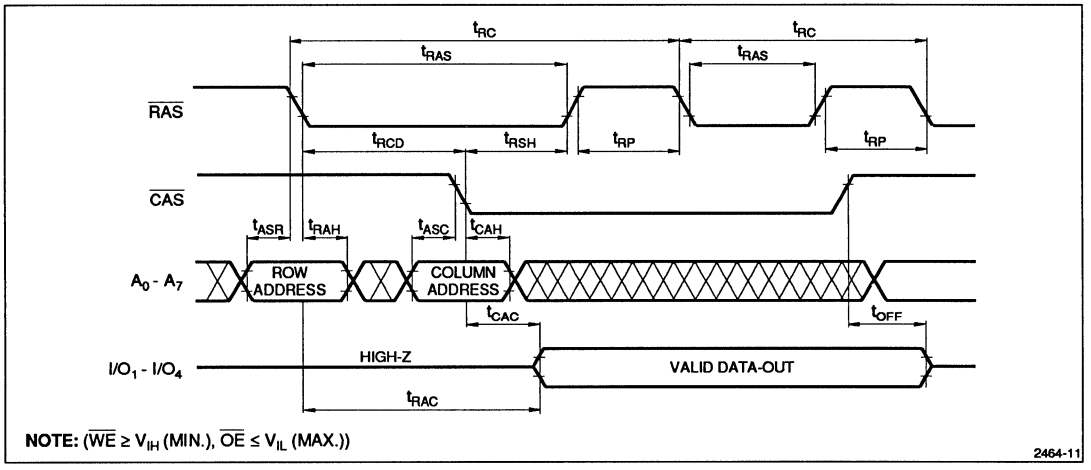


Figure 11. Hidden Refresh Cycle

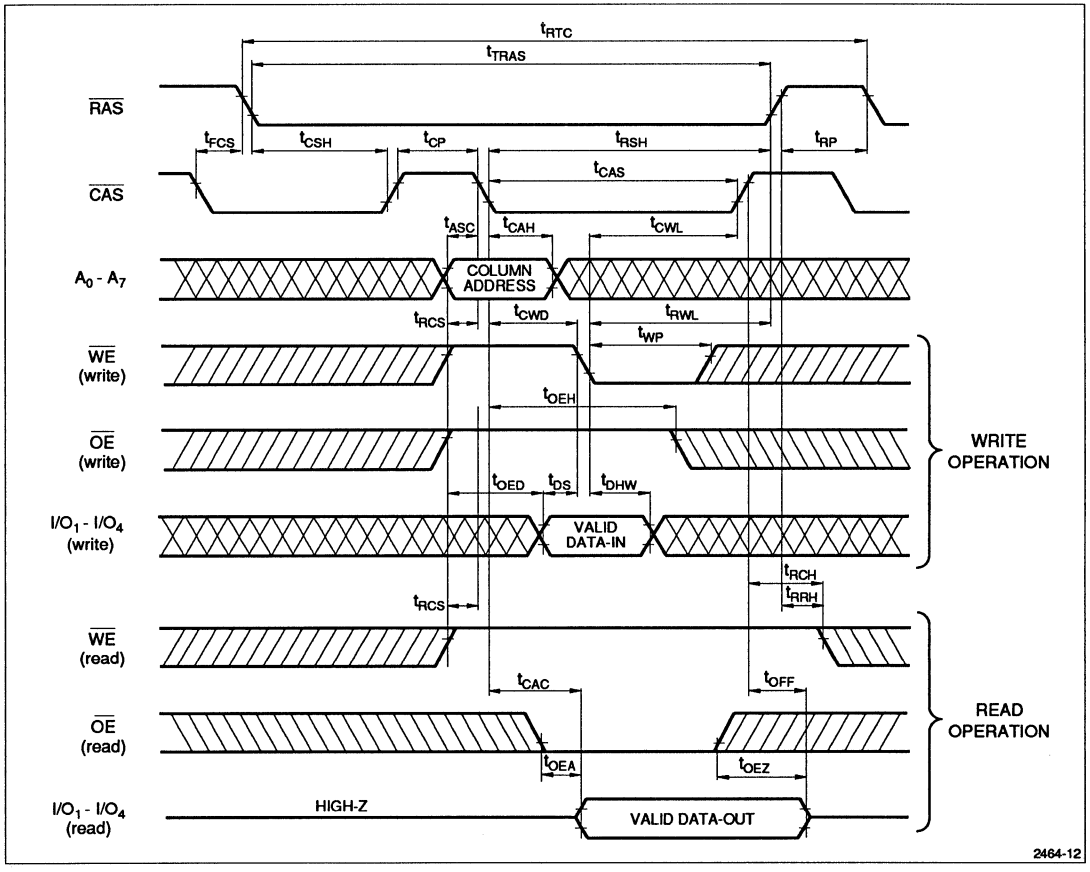


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle is used to verify the operation of the internal refresh counter. The verification can be done by following the steps as described below.

1. Write "0" into 256 row addresses on a particular column address, which are selected by the internal refresh counter, by the write operation of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle mode with any given column address.

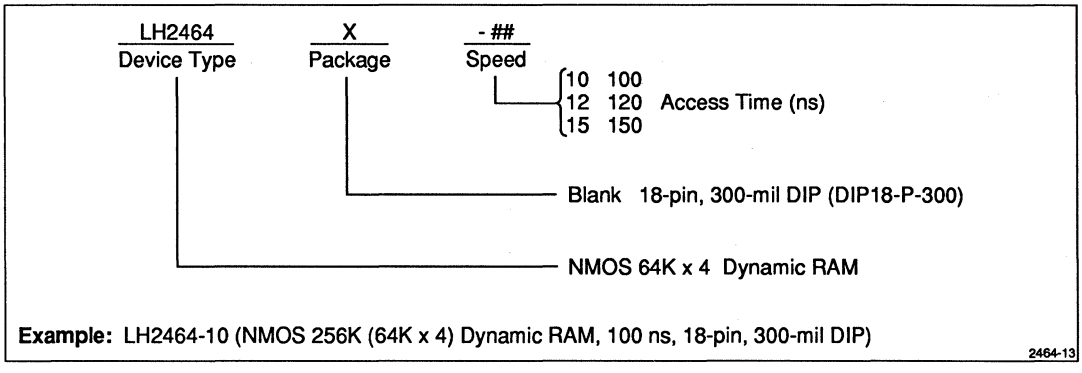
2. Read and verify "0" of the 256 row addresses on the same column in regular read mode by externally supplying address signals.

Then, write "1" into the above 256 row addresses in regular write mode.

3. Read and verify "1" of the 256 row addresses in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle mode.

Refer to timing chart (12) of the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle.

ORDERING INFORMATION



LH2465

NMOS 256K (64K × 4) Dynamic RAM

FEATURES

- 65,536 × 4 bit organization
- Access times: 120/150 ns (MAX.)
- Cycle times: 220/260 ns (MIN.)
- Nibble-Mode, Read-Modify-Write operation
- Power supply: +5 V ± 10%
- Power consumption:
  Operating: 457/413 mW (MAX.)
  Standby: 27.5 mW (MAX.)
- TTL compatible I/O
- Built-in gated $\overline{CAS}$ function
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output substrate bias generator circuit
- Package:
  18-pin, 300-mil DIP

DESCRIPTION

The LH2465 is a 65,536 × 4 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With multiplexed address inputs and a standard 18-pin DIP package, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH2465 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

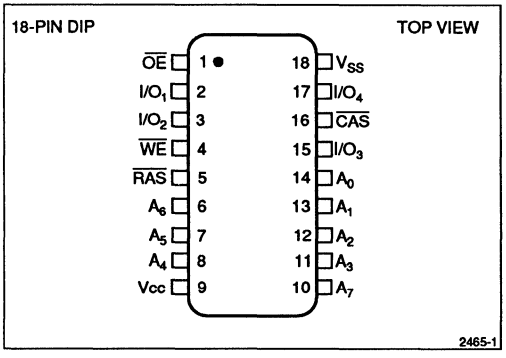


Figure 1. Pin Connections for DIP Package

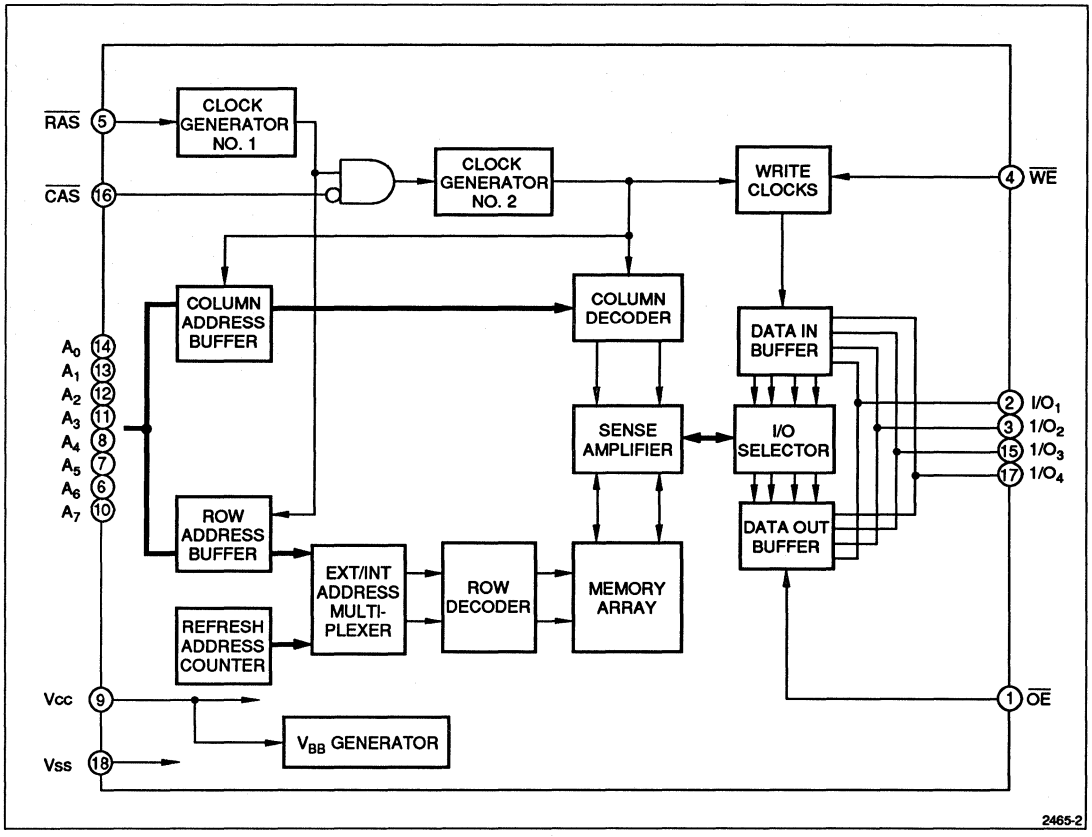


Figure 2. LH2465 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_7	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		

NOTE:
1. Referenced to V_{SS}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	A_0 - A_7	C_{IN1}			5	pF
	$\overline{OE}$, $\overline{WE}$	C_{IN2}			7	
	$\overline{RAS}$, $\overline{CAS}$	C_{IN3}			10	
Input/Output capacitance	I/O_1 - I/O_4	C_{IO}			8	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH2465-12	I_{CC1}	—	83	mA	1, 2
	LH2465-15		—	75		
Average supply current in standby mode		I_{CC2}	—	5.0	mA	1
Average supply current in $\overline{RAS}$ only refresh time	LH2465-12	I_{CC3}	—	63	mA	1, 2
	LH2465-15		—	65	mA	
Average supply current in nibble mode	LH2465-12	I_{CC4}	—	60	mA	1
	LH2465-15		—	55	mA	
$\overline{CAS}$ before $\overline{RAS}$ average supply current in refresh cycle	LH2465-12	I_{CC5}	—	70	mA	1, 2
	LH2465-15		—	65	mA	
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	$I_{I(L)}$	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	$I_{O(L)}$	-10	10	µA	
Output "High" voltage	I_{OUT} = -2 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on the cycle time.

AC CHARACTERISTICS [1, 2, 3] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH2465-12		LH2465-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	t_{RC}	220	—	260	—	ns	
Read write cycle time	t_{RWC}	305	—	360	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	120	—	150	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	—	60	—	75	ns	5, 6
Output turn off delay time	t_{OFF}	0	30	0	40	ns	
Rise and fall time	t_T	3	35	3	35	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60	—	75	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	50	—	60	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120	—	150	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	120	—	150	—	ns	
$\overline{CAS}$ setup time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	10	—	30	—	ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}	25	60	30	75	ns	7, 8
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	10	—	30	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	45	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	80	—	120	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	10
Read command hold time from $\overline{RAS}$	t_{RRH}	10	—	20	—	ns	10
Write command setup time	t_{WCS}	0	—	0	—	ns	9
Write command hold time	t_{WCH}	40	—	45	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	100	—	120	—	ns	
Write command pulse width	t_{WP}	40	—	45	—	ns	
Write command $\overline{RAS}$ lead time	t_{RWL}	40	—	45	—	ns	
Write command $\overline{CAS}$ lead time	t_{CWL}	40	—	45	—	ns	
$\overline{RAS}$ write command delay time	t_{RWD}	160	—	200	—	ns	
$\overline{CAS}$ write command delay time	t_{CWD}	100	—	125	—	ns	
Data input setup time	t_{DS}	0	—	0	—	ns	
Data input hold time from $\overline{CAS}$	t_{DHC}	40	—	45	—	ns	
Data input hold time from $\overline{RAS}$	t_{DHR}	100	—	120	—	ns	
Refresh interval	t_{REF}	—	4	—	4	ms	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	ns	
$\overline{OE}$ command hold time	t_{OEH}	25	—	40	—	ns	11
$\overline{OE}$ access time	t_{OEA}	—	30	—	40	ns	
$\overline{OE}$ to data delay	t_{OED}	30	—	40	—	ns	
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	30	0	40	ns	
Data input hold time from $\overline{WE}$	t_{DHW}	40	—	45	—	ns	
Refresh counter test cycle time	t_{RTC}	445		520		ns	12
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	335		410		ns	12

NOTES

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristic assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. Only when $t_{RCD} \leq t_{RCD}$ (MAX.). If $t_{RCD} > t_{RCD}$ (MAX.), t_{RAC} will increase by (t_{RCD} - t_{RCD} (MAX.)).
5. When $t_{RCD} \geq t_{RCD}$ (MAX.).
6. Load condition for 2TTL + 100 pF.
7. t_{RCD} (MAX.) is the maximum point for t_{RCD} where t_{RAC} (MAX.) is ensured, and does not represent a limit of operation. If t_{RCD} (MAX.) ≤ t_{RCD}, the access time will come under the control of t_{CAC}.
8. t_{RCD} (MIN.) = t_{RAH} (MIN.) + 2t_T + t_{ASC} (MIN.).
9. When $t_{WCS} \geq t_{WCS}$ (MIN.), it comes into early write cycle.
10. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
11. Only when $t_{WCS} < t_{WCS}$ (MIN.), it must be satisfied.
12. Only when in $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle.

NIBBLE MODE CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	LH2465-12		LH2465-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Nibble mode access time	t_{NAC}	—	30	—	35	ns	
Nibble mode $\overline{RAS}$ cycle time	t_{NRC}	460	—	520	—	ns	
Nibble mode $\overline{RAS}$ pulse width	t_{NRA}	350	—	410	—	ns	
Nibble mode cycle time	t_{NC}	70	—	80	—	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	30	—	35	—	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCA}	30	—	35	—	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	50	—	55	—	ns	
Nibble mode $\overline{CAS}$/$\overline{WE}$ delay	t_{NCWD}	70	—	85	—	ns	
Nibble mode write command $\overline{CAS}$ lead time	t_{NCWL}	30	—	35	—	ns	
Nibble mode write command hold time	t_{NWCH}	30	—	35	—	ns	
Nibble mode write command pulse width	t_{NWP}	30	—	35	—	ns	

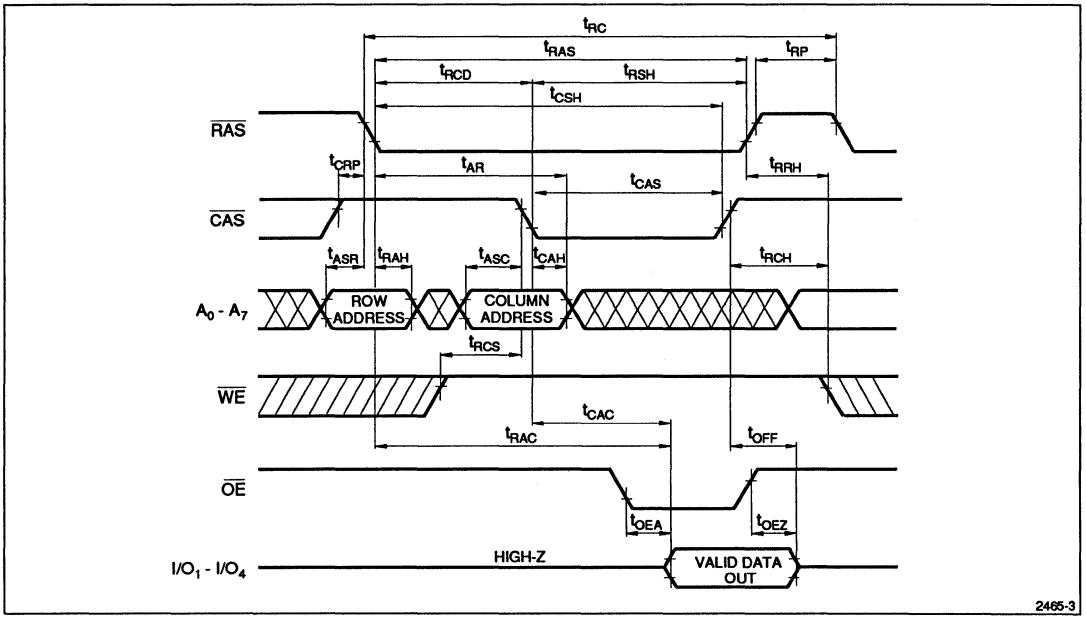


Figure 3. Read Cycle

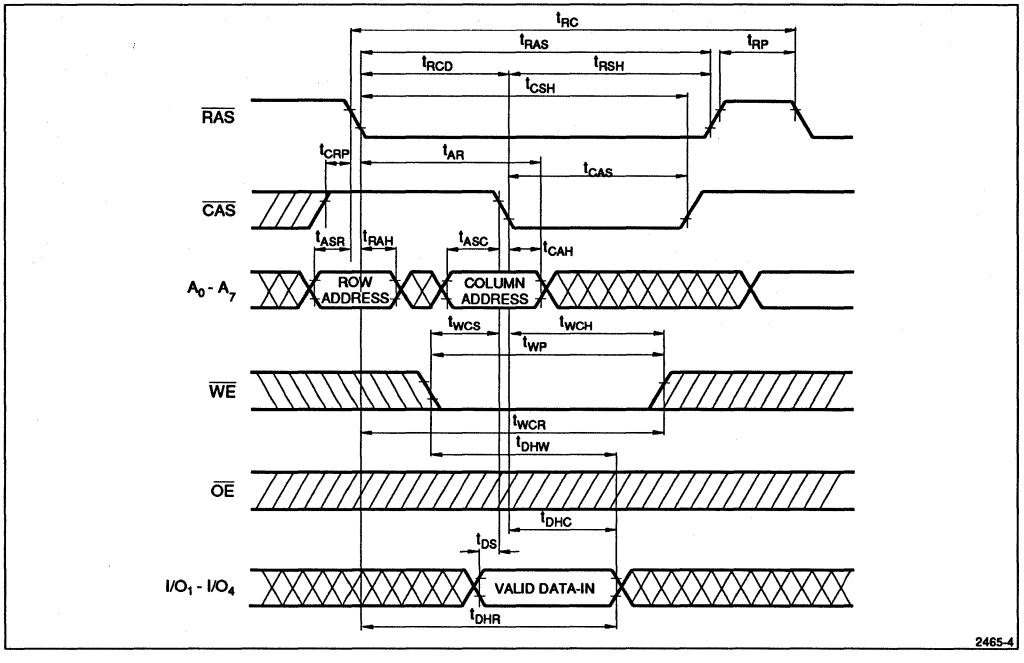


Figure 4. Write Cycle (Early Write)

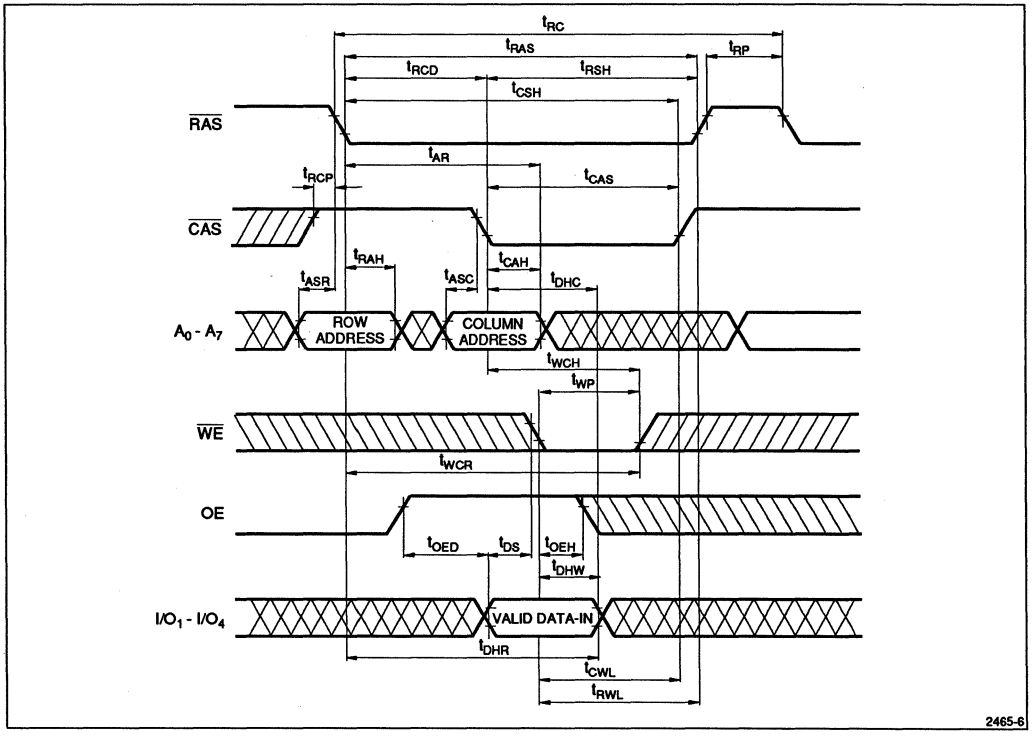


Figure 5. Write Cycle ($\overline{OE}$ Controlled Write)

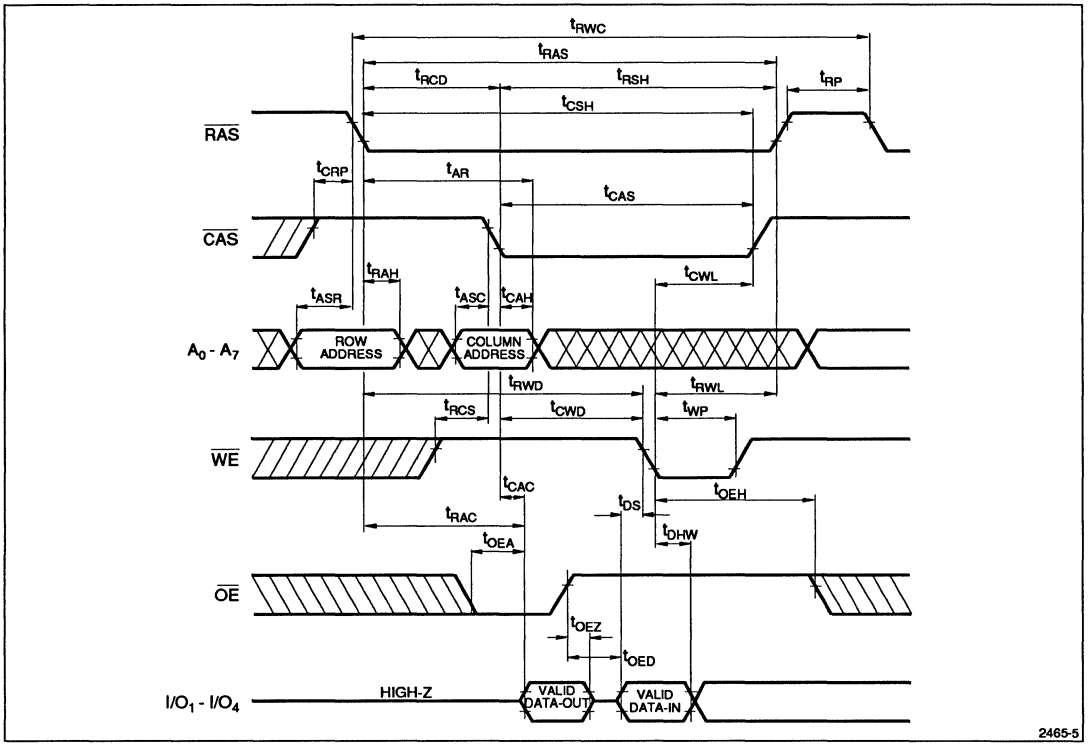


Figure 6. Read-Write/Read-Modify-Write Cycle

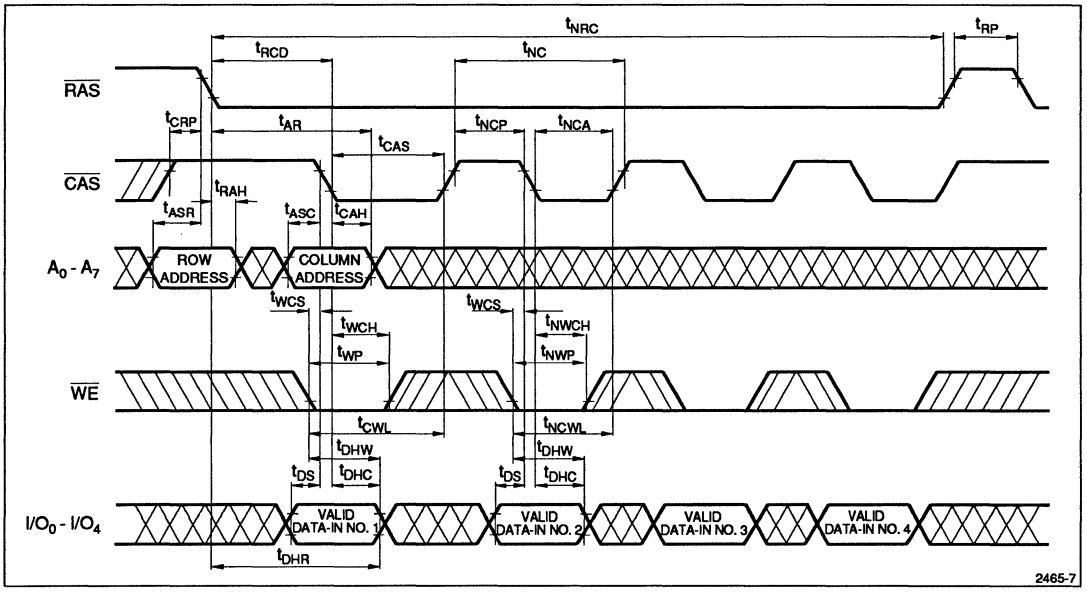


Figure 7. Nibble Mode Write Cycle

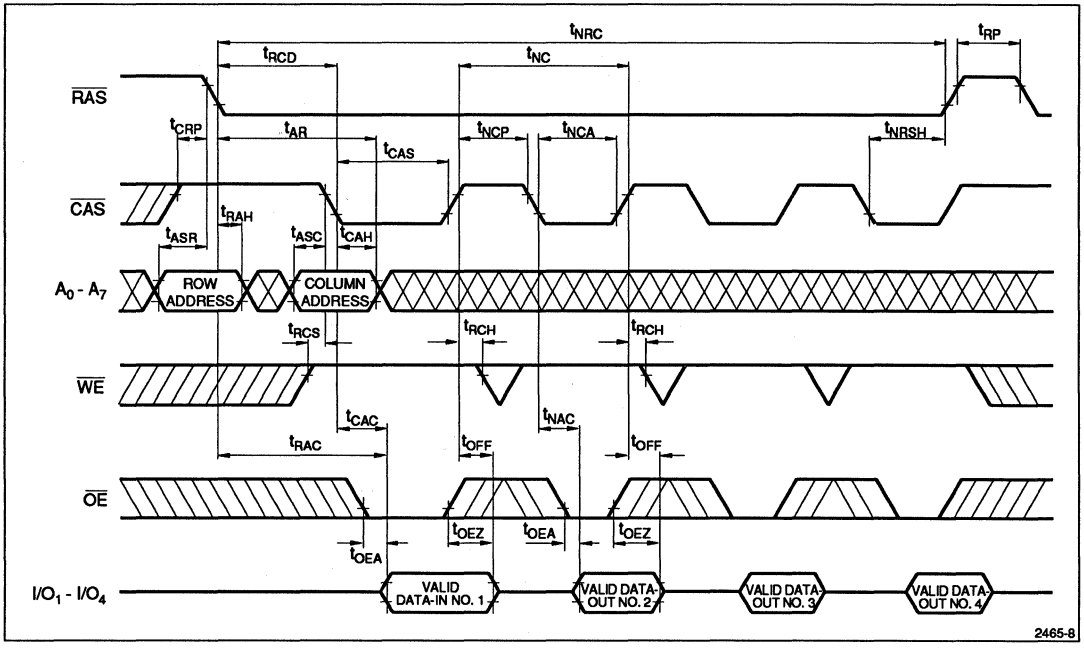


Figure 8. Nibble Mode Read Cycle

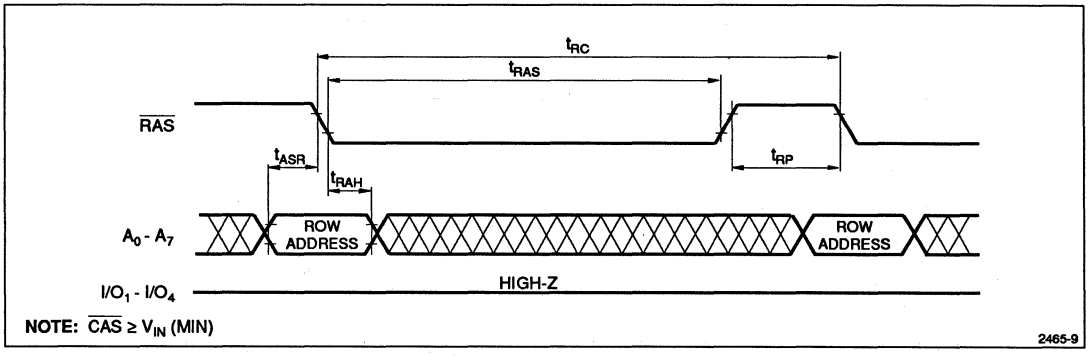


Figure 9. $\overline{RAS}$ Only Refresh Cycle

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle is used to verify the operation of the internal refresh counter. The verification can be done by following the steps as described below.

(1) Write "0" into 256 row addresses on a particular column address, which are selected by the internal refresh counter, by the write operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle mode with any given column address.

(2) Read and verify "0" of the 256 row addresses on the same column in regular read mode by externally supplying address signals.

Then, write "1" into the above 256 row addresses in regular write mode.

(3) Read and verify "1" of the 256 row addresses in the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle mode.

Refer to timing chart (Figure 12) of the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle.

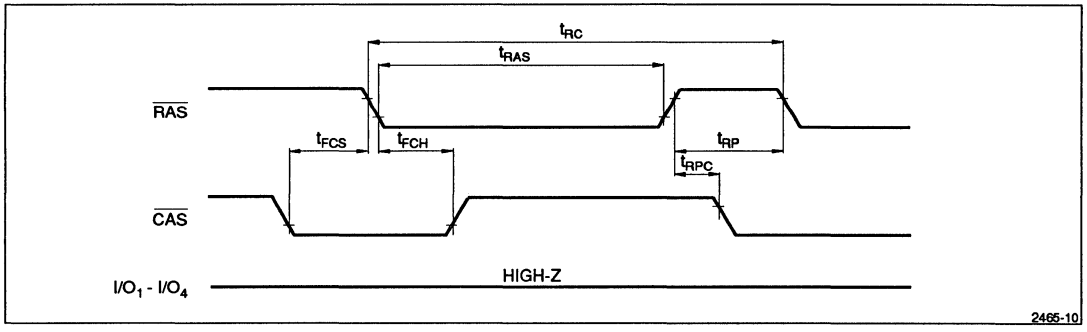


Figure 10. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

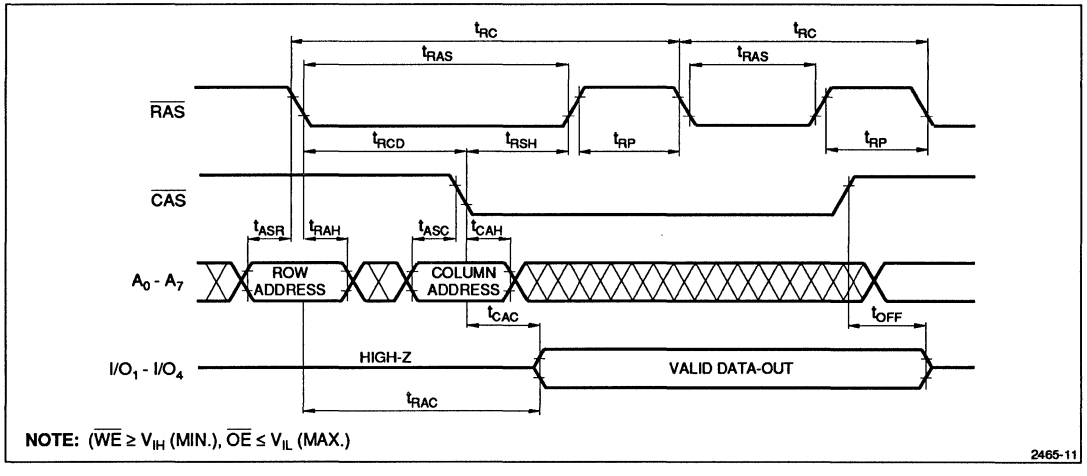


Figure 11. Hidden Refresh Cycle

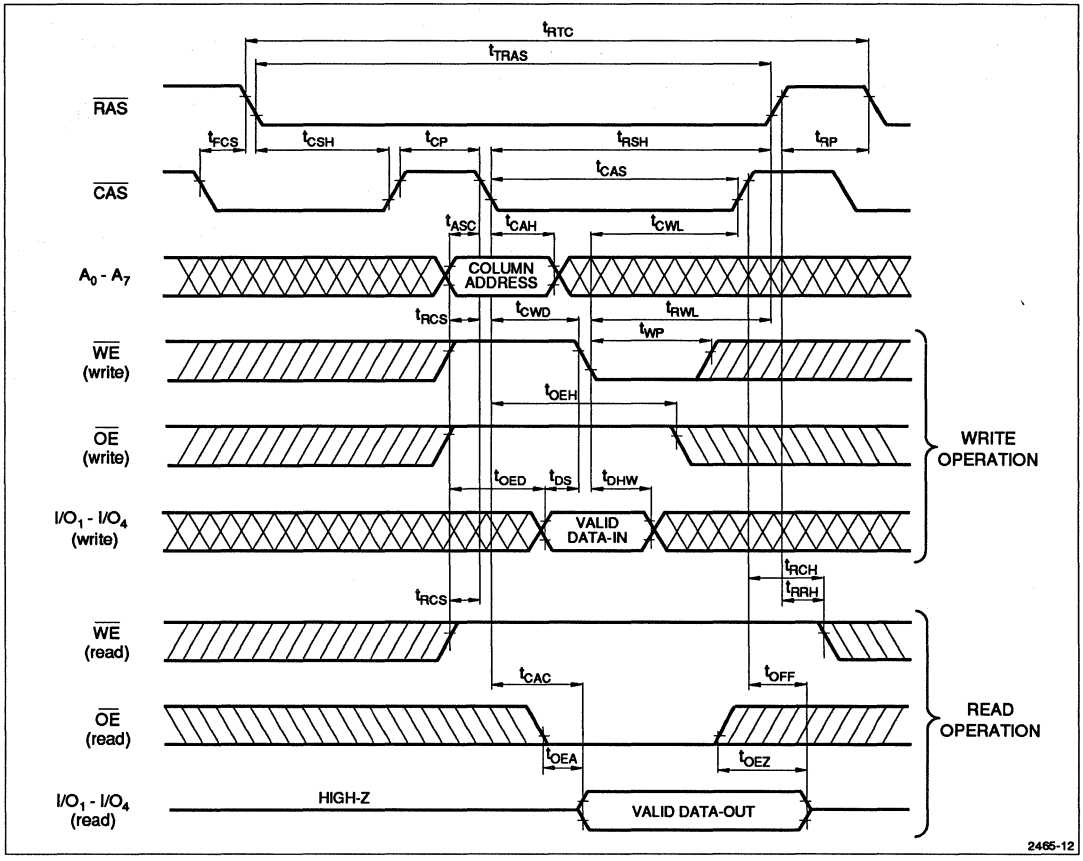
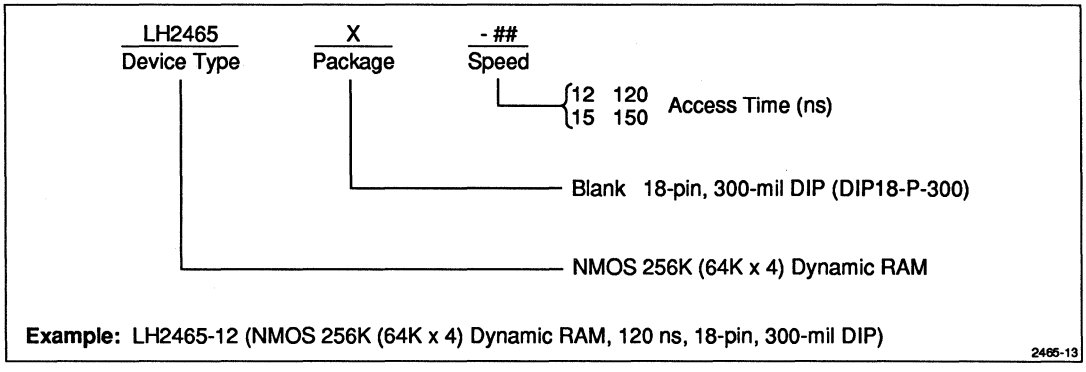


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

ORDERING INFORMATION



LH604256

CMOS 1M (256K × 4) Dynamic RAM

FUNCTION

- 262,144 Words × 4-Bit Dynamic RAM
- Access times: 80/100 ns (MAX.)
- Power supply: +5V ± 10%
- Power consumption (MAX.):
  Operating: 374/340 mW
  Standby: 374/340 mW
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- 512 refresh cycle
  (refresh period (MAX.) = 8 ms)
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP

DESCRIPTION

The LH604256 is a 262,144 word × 4 bit dynamic RAM which provides a high-speed page mode operation.

The LH604256 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ packages, it is easy to comprise memory systems with high speed, lower power consumption and large memory capacity. The LH604256 operates on a single 15 V power supply.

PIN CONNECTIONS

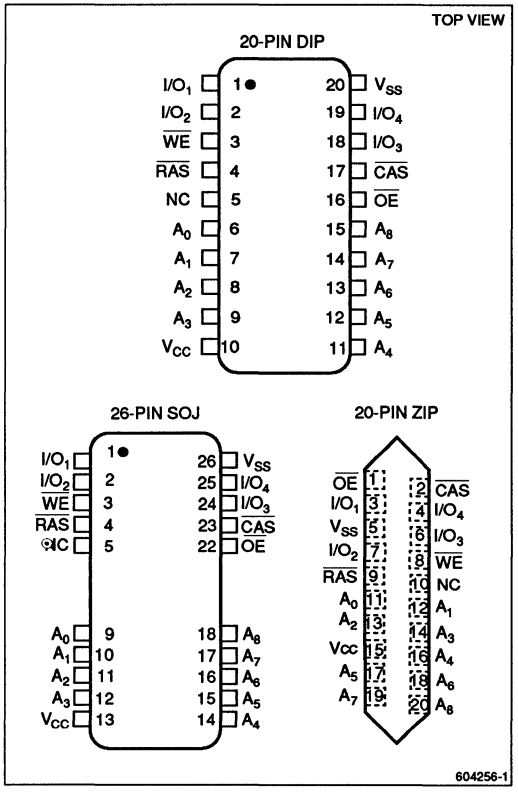


Figure 1. Pin Connections for DIP, SOJ, and ZIP Packages

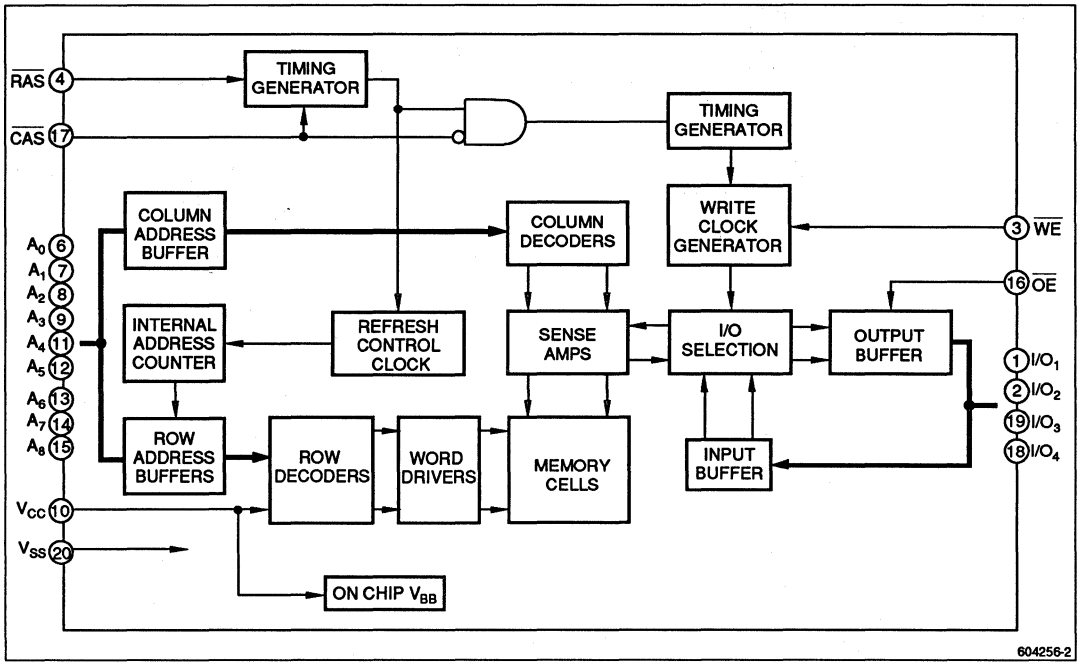


Figure 2. LH604256 Block Diagram

PIN DESCRIPTION

PIN NAME	FUNCTION
A_0 - A_8	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
DQ_1 - DQ_4	Data input/output
$\overline{OE}$	Output enable

PIN NAME	FUNCTION
$\overline{WE}$	Write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground (0 V)
NC	No connection

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	CONDITIONS	VALUE	UNIT
Voltatge on any pin relative to V_{SS}	V_T	T_A - 25°C	-1 to +7.0	V
Short circuit output current	I_{OS}	T_A - 25°C	50	mA
Power dissipation	P_D	T_A - 25°C	1	W
Operating temperature	Topr		0 to +70	°C
Strorage temperature	Tstg		-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}		4.5	5	5.5	V
	V_{SS}		0	0	0	V
Input high voltage	V_{IH}		2.4		6.5	V
Input low voltage	V_{IL}		-1		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		LH604256-80A		LH604256-10A		UNIT	NOTE
				MIN.	MAX.	MIN.	MAX.		
Output high voltage	V_{OH}	I_{OH} = -5 mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≤ V_I ≤ 6.5 V all other pins not under test = 0 V		-10	10	-10	10	µA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≤ V_O ≤ 5.5 V		-10	10	-10	10	µA	
Average power supply current (operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.			75		65	mA	1
Power supply current (standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IH} D_{OUT} = Hz	TTL		2		2	mA	1
			MOS		1		1	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} t_{RC} = min.			75		65	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC5}	$\overline{RAS}$ cycling $\overline{CAS}$ before $\overline{RAS}$			75		65	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ - V_{IL} $\overline{CAS}$ cycling t_{PC} - min.			65		60	mA	1

NOTE:

1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the outputs open.

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1MHz, T_A = 0 to 70°C)

PARAMETER		SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Input capacitance	A_0 - A_8	C_{IN1}	—	—	6	pF
	$\overline{RAS}$,$\overline{CAS}$,$\overline{OE}$,$\overline{WE}$	C_{IN2}	—	—	7	pF
Input/Output capacitance	I/O_1 - I/O_4	$C_{I/O}$		—	7	pF

AC CHARACTERISTICS [1,2,3] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH604256-80A		LH604256-10A		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	–	–	ns	
Read/write cycle time	t_{RWC}	215	–	–	–	ns	
Fast page mode cycle time	t_{PC}	50	–	–	–	ns	
Fast page mode read/write cycle time	t_{PRMW}	105	–	–	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4, 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse time	t_{WP}	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50	–	60	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110	–	135	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	85	–	ns	7
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time(Refresh counter test)	t_{CPT}	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	ns	
$\overline{OE}$ delay time	t_{OED}	20	–	25	–	ns	
$\overline{OE}$ to data output buffer turn-off delay	t_{OEZ}	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	ns	

See next page for notes.

NOTES:

1. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles. (Examples: $\overline{RAS}$ only Refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (MIN.) and V_{IL} (MAX.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (MAX.) limit insures that t_{RAC} (MAX.) can be met. t_{RCD} (MAX.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (MAX.) limit insures that t_{RAC} (MAX.) can be met. t_{RAD} (MAX.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX.) limit, then access time is controlled exclusiviely by t_{AA}.
7. t_{WCS}, t_{CWL}, t_{RWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle in an early write cycle and the data out pin will remain open circuit (high-impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (MIN.), $t_{RWD} \geq t_{RWD}$ (MIN.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

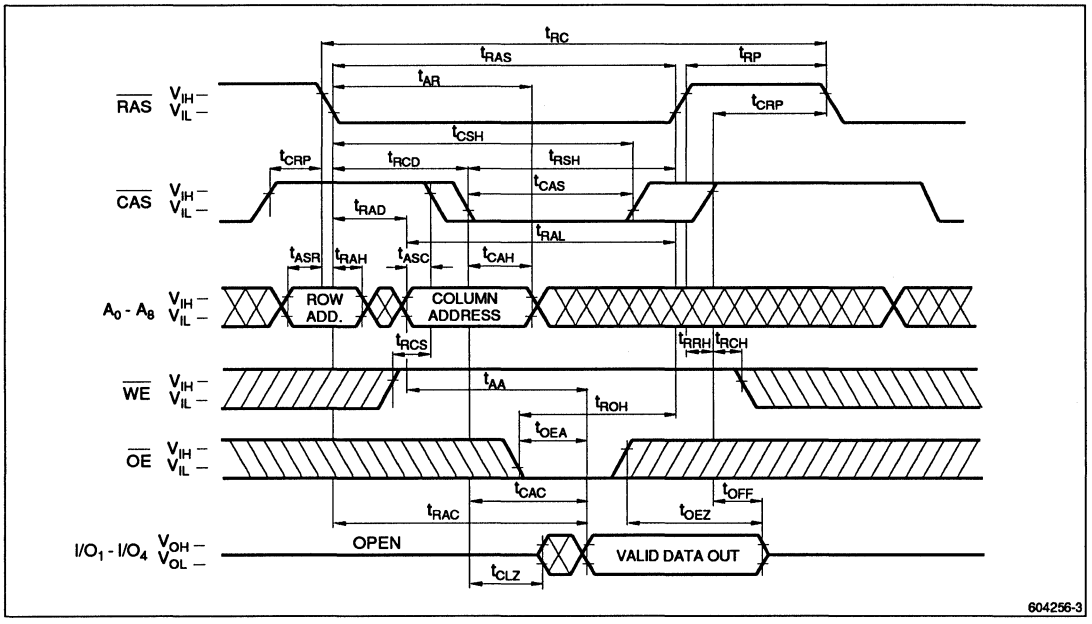


Figure 3. Read Cycle

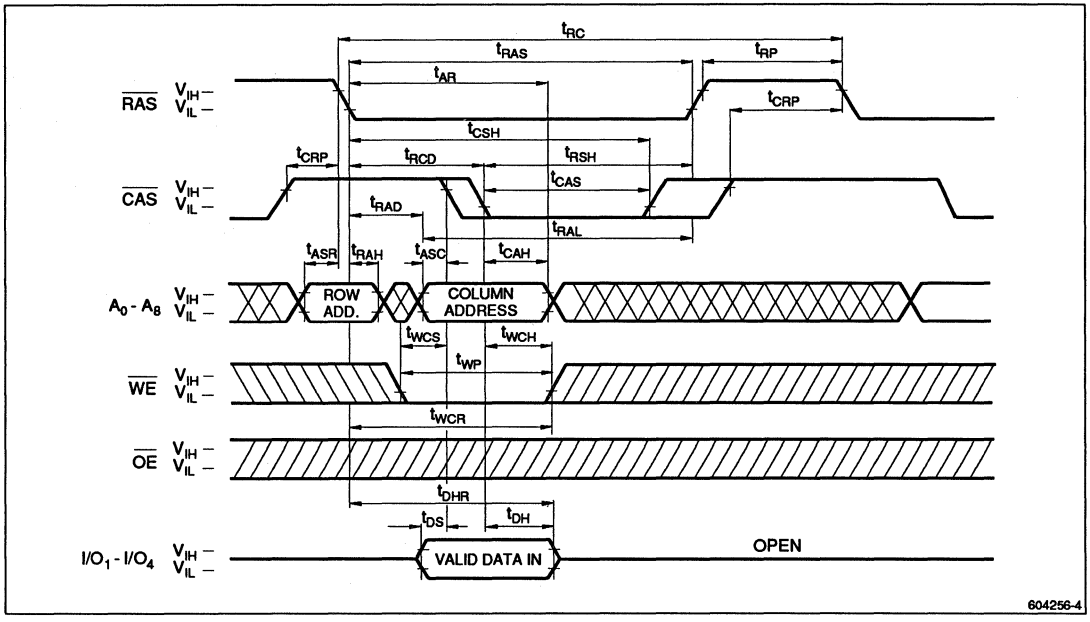


Figure 4. Write Cycle (Early Write)

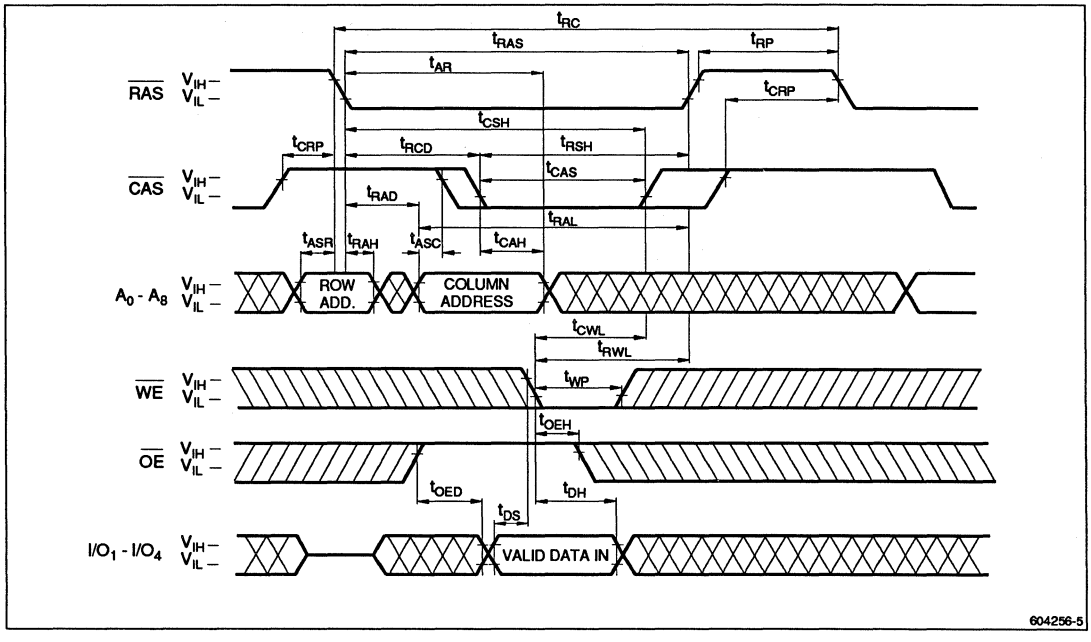


Figure 5. Write Cycle ($\overline{OE}$ Control)

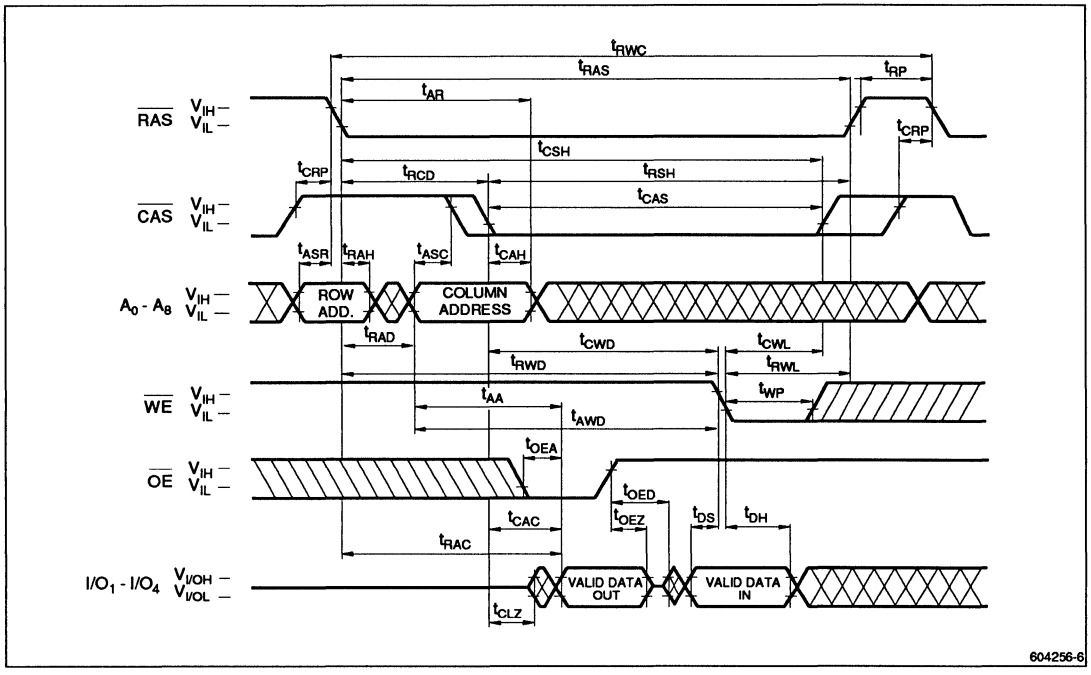


Figure 6. Read/Write, Read-Modify-Write Cycle

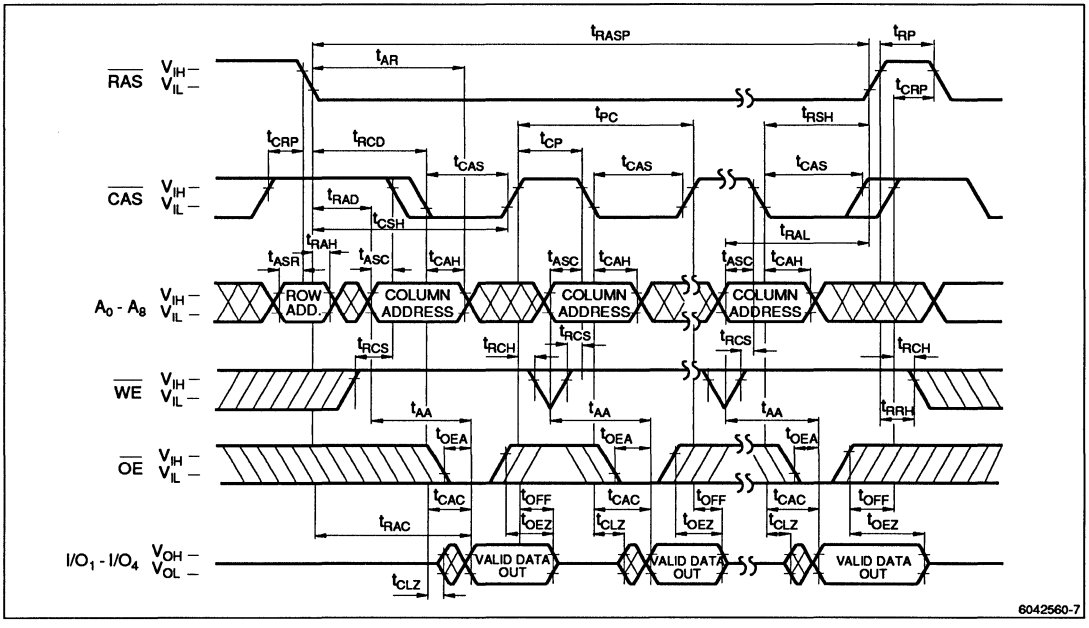


Figure 7. High Speed Page Mode Read Cycle

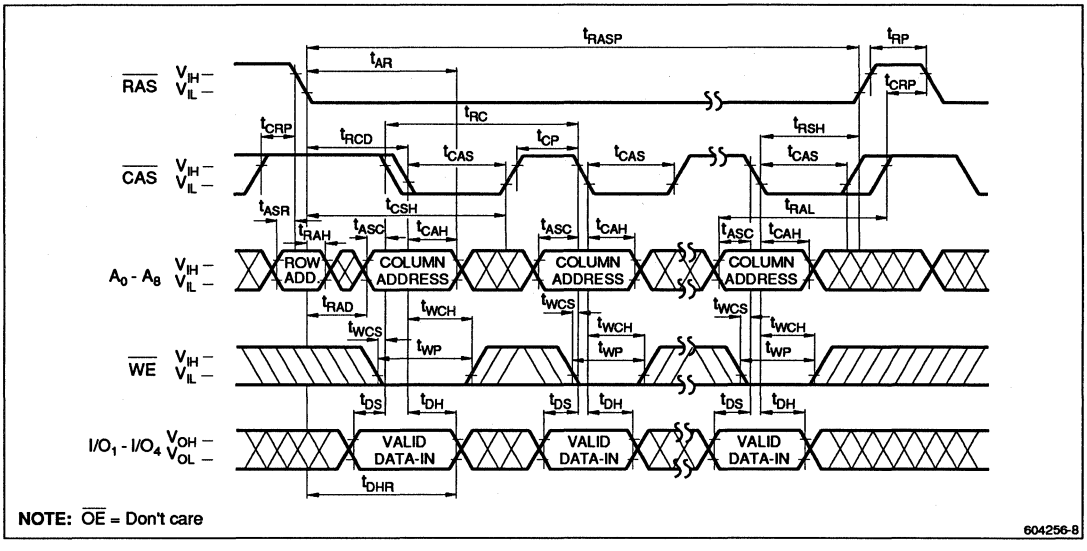


Figure 8. High Speed Page Mode Write Cycle (Early Write)

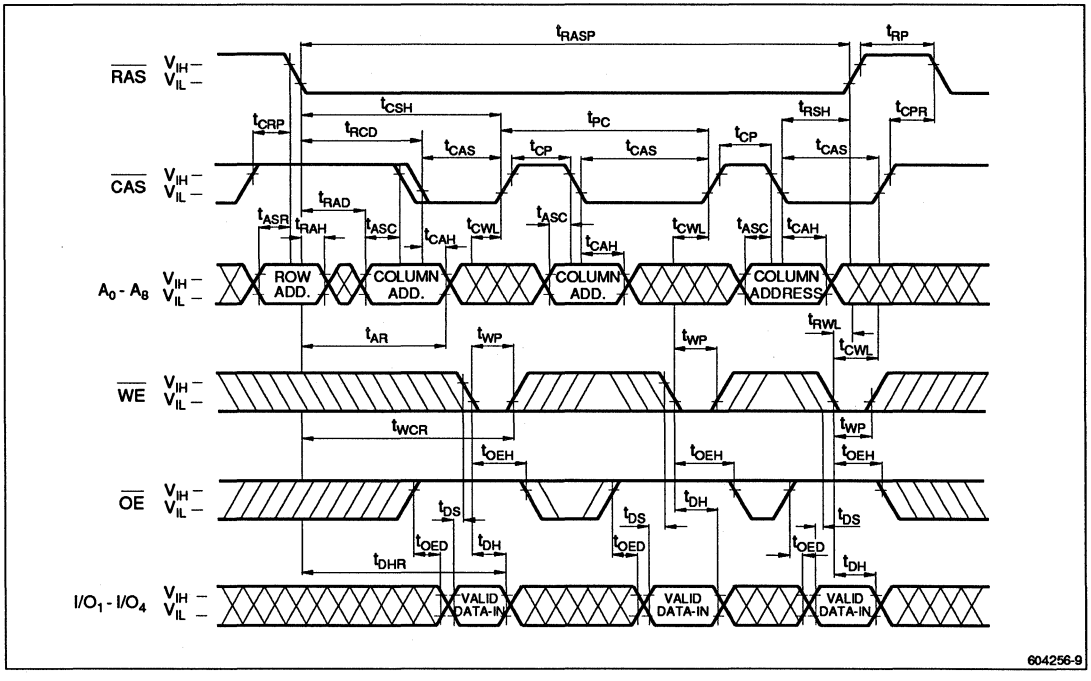


Figure 9. High Speed Page Mode Write Cycle (OE Control)

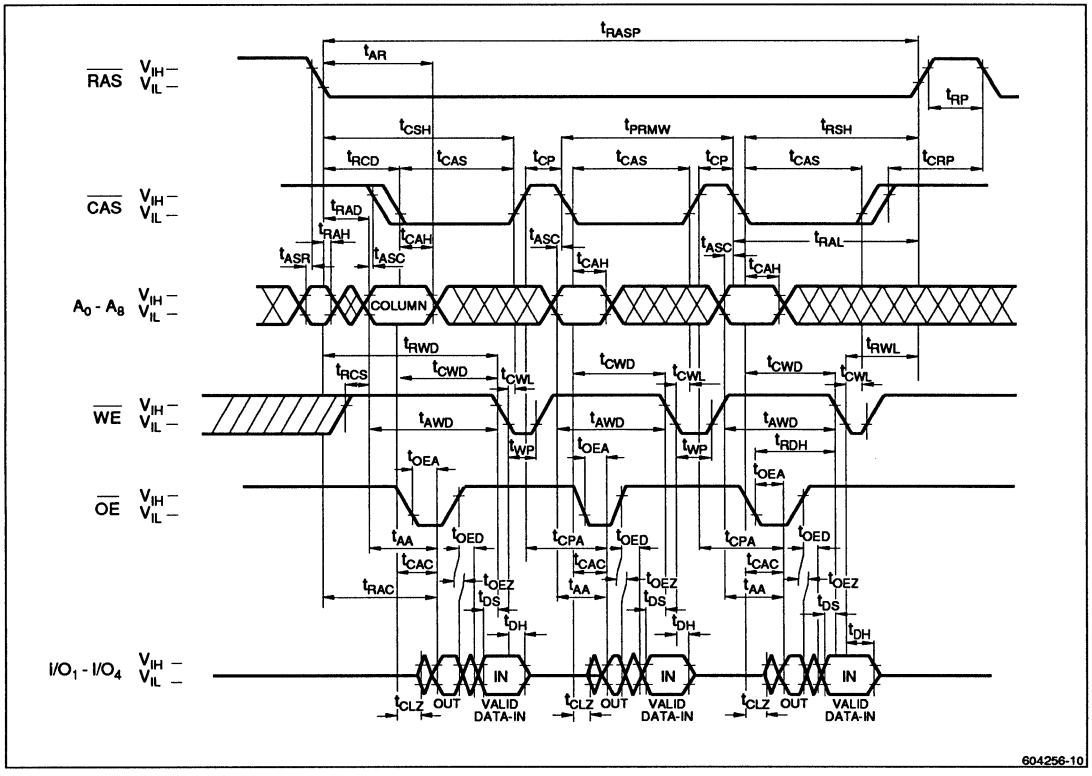


Figure 10. High Speed Page Mode Read/Write Cycle

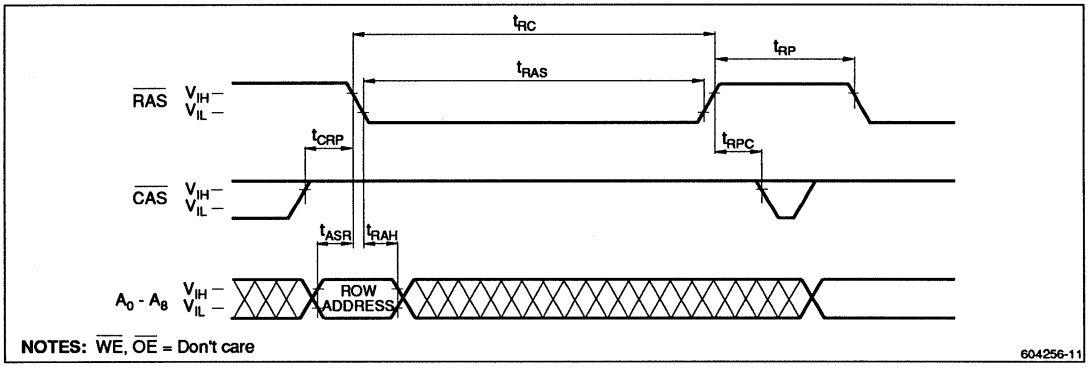


Figure 11. RAS Only Refresh Cycle

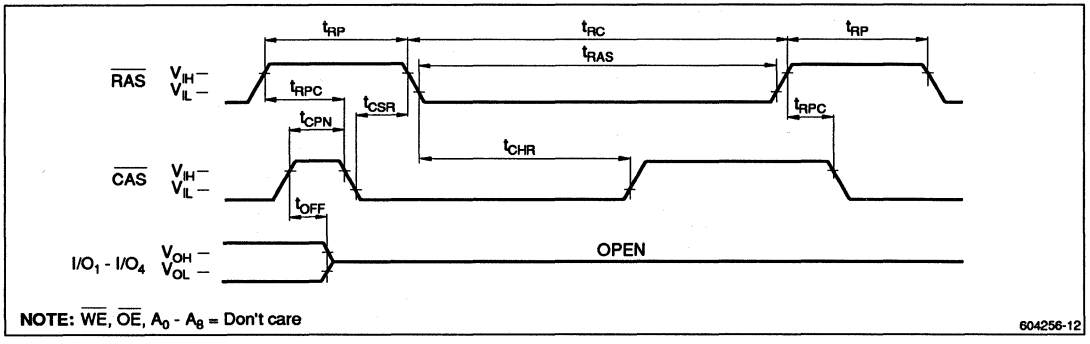


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

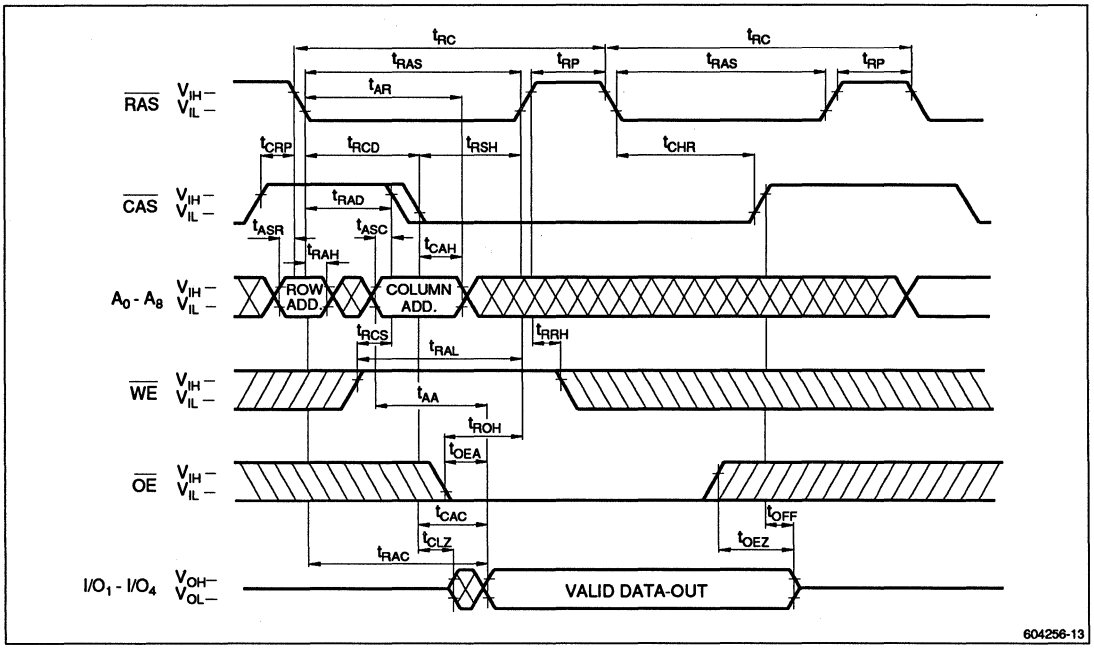


Figure 13. Hidden Refresh Read Cycle

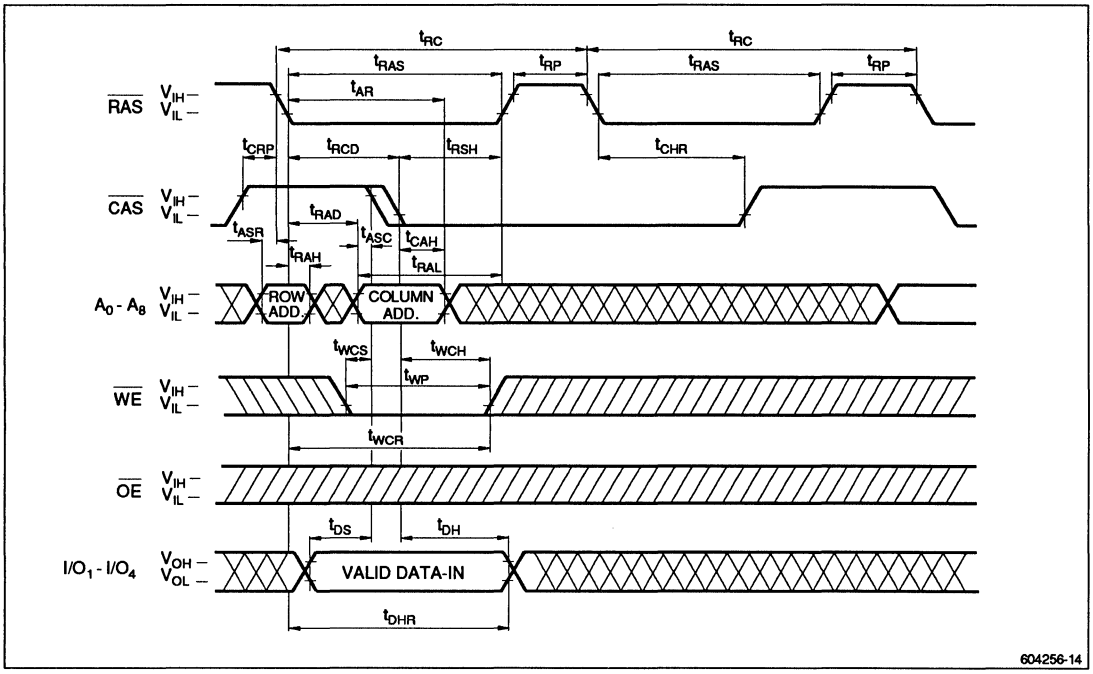


Figure 14. Hidden Refresh Write Cycle

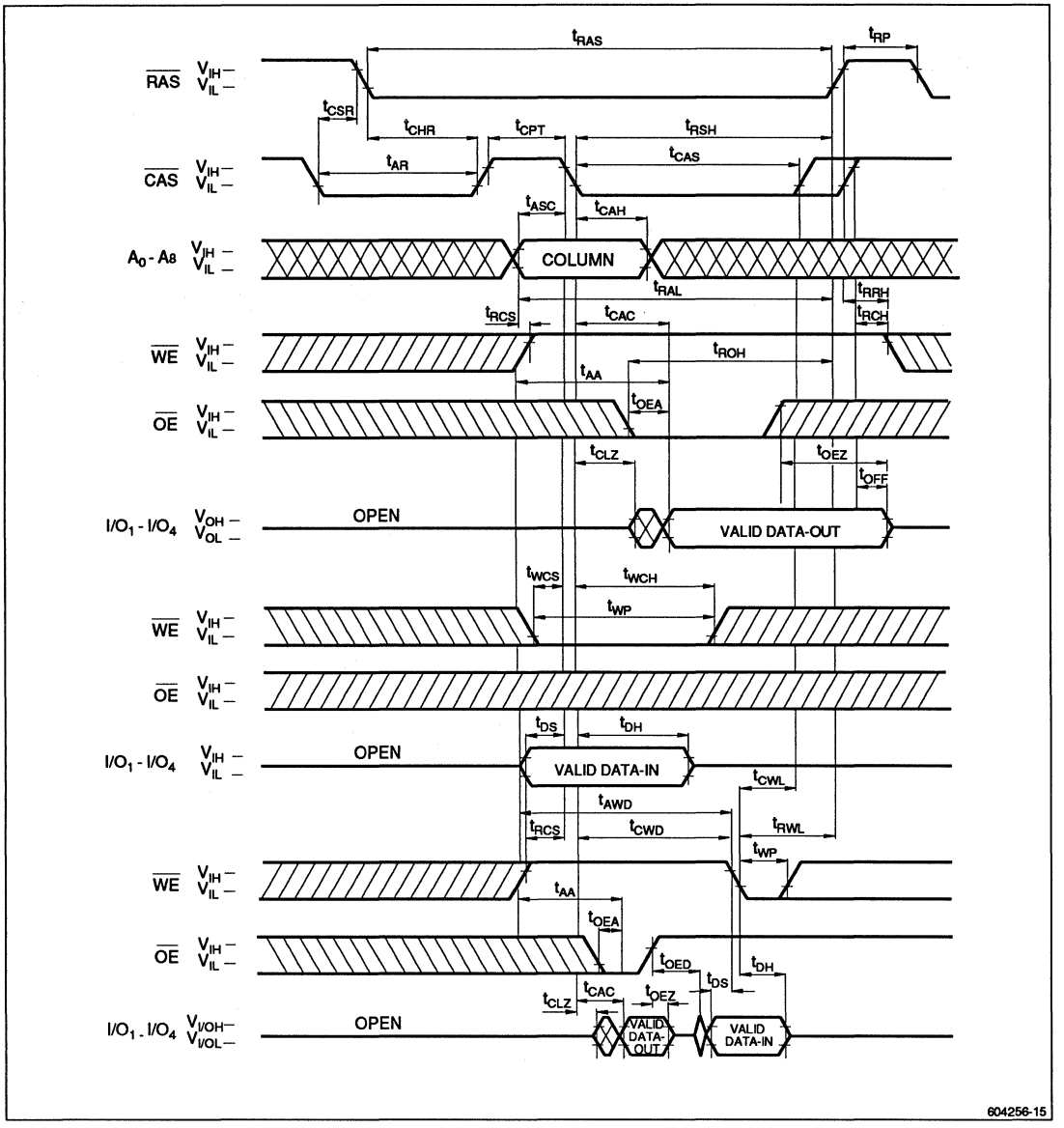
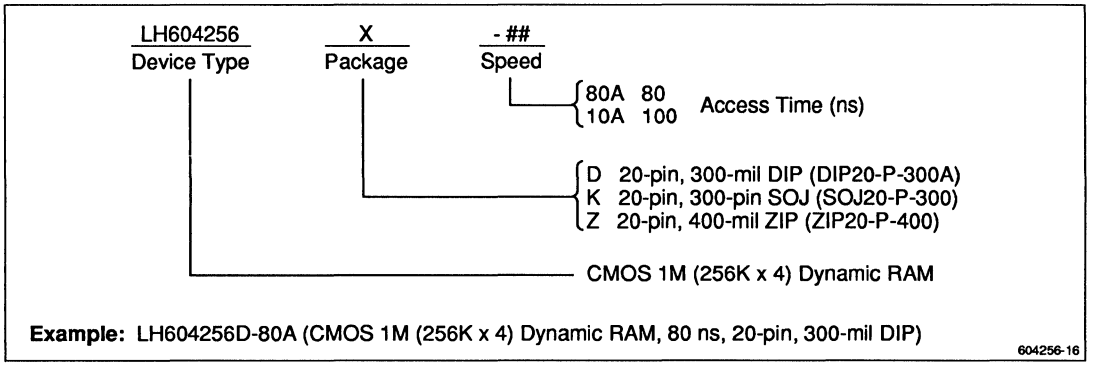


Figure 15. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

ORDERING INFORMATION



Example: LH604256D-80A (CMOS 1M (256K x 4) Dynamic RAM, 80 ns, 20-pin, 300-mil DIP)

604256-16

LH64258

CMOS 1M (256K × 4) Dynamic RAM

FEATURES

- 262,144 × 4 bit organization
- Access times: 100/120 ns (MAX.)
- Cycle times: 160/190 ns (MIN.)
- Cycle time in static column mode: 55/65 ns (MIN.)
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
  Operating: 374/340 mW
  Standby: 11 mW
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CS}$ before $\overline{RAS}$ refresh capability
- 512 refresh cycle
  (refresh period (MAX.) = 8 ms)
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP

DESCRIPTION

The LH64258 is a 262,144 word × 4 bit dynamic RAM which provides a static column mode operation.

The LH64258 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH64258 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

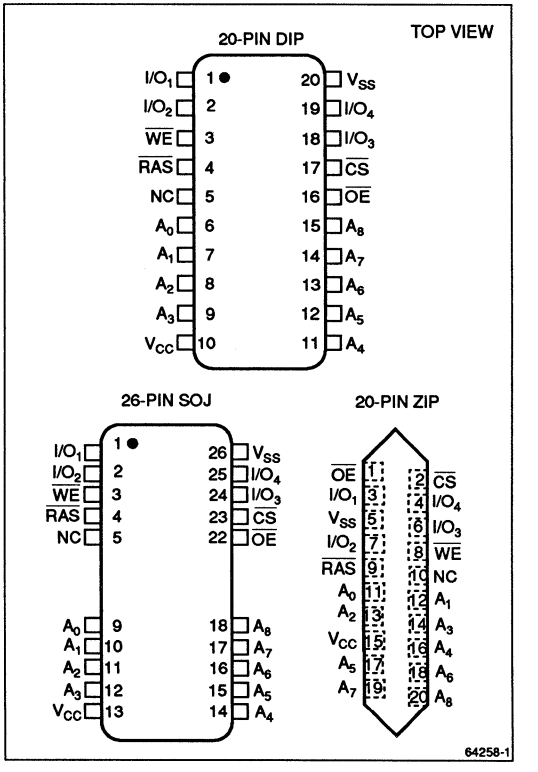


Figure 1. Pin Connections for DIP, SOJ, and ZIP Packages

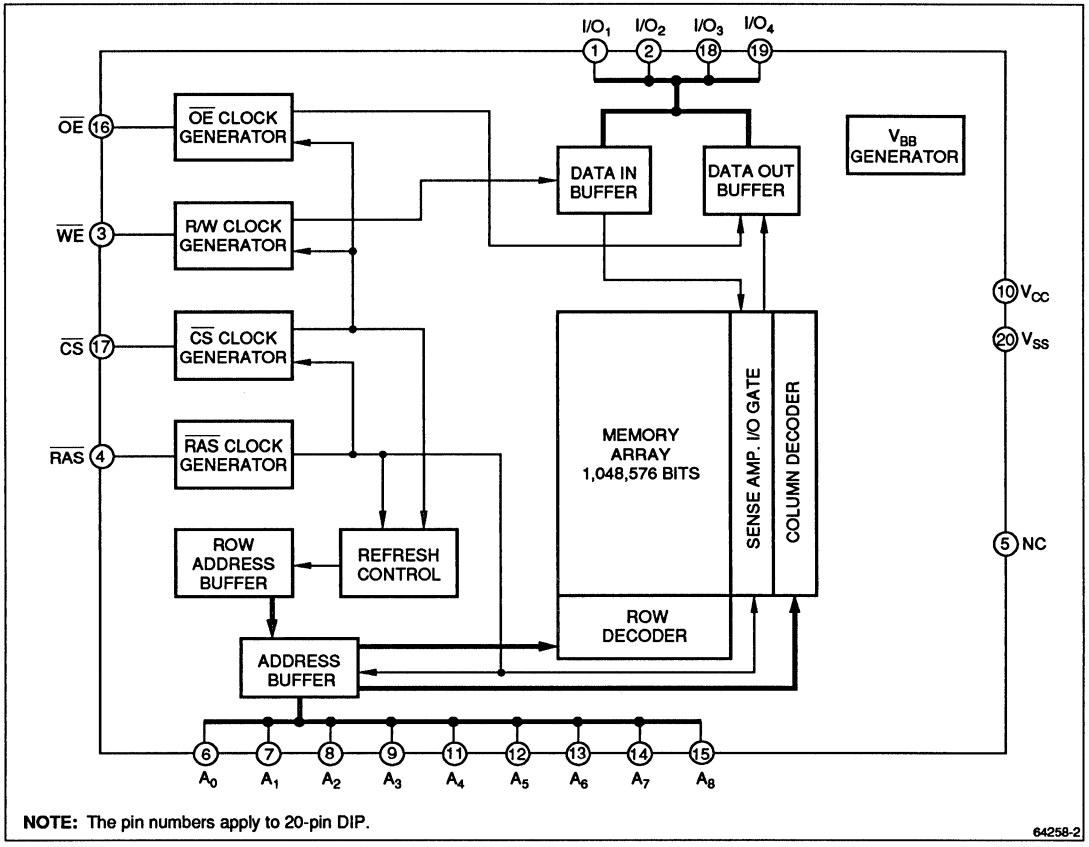


Figure 2. LH64258 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_8	Address input
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		1

NOTE:
1. Referenced to V_{SS}

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH64258-10	I_{CC1}	—	68(80)	mA	1, 2, 3
	LH64258-12		—	62(68)		
Average supply current in standby mode		I_{CC2}	—	2.0	mA	1
Average supply current in the static column mode	LH64258-10	I_{CC3}	—	60	mA	1, 2
	LH64258-12		—	55		
Average supply current in $\overline{CS}$ before $\overline{RAS}$ refresh cycle	LH64258-10	I_{CC4}	—	68(80)	mA	1, 2, 3
	LH64258-12		—	62(68)		
Average supply current in $\overline{RAS}$ only refresh cycle	LH64258-10	I_{CC5}	—	68(80)	mA	1, 2, 3
	LH64258-12		—	62(68)		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	I_{L1}	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	I_{LO}	-10	10	µA	
Output "High" voltage	I_{OUT} = -5 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on the cycle time.
3. Cycle time: 190 ns (LH64258-10), 220 ns (LH64258-12).
   Figures in parenthesis indicate current under minimum cycle time operation.
   Address transition is occurs when $\overline{RAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	A_1 - A_7	C_{IN1}	—		5	pF
	A_0, A_8	CIN2	—		8	pF
	$\overline{OE}$, $\overline{CS}$	C_{IN3}	—		8	pF
	$\overline{RAS}$,$\overline{WE}$	C_{IN4}	—		5	pF
Input/Output capacitance	I/O_1 - I/O_4	C_{OUT1}	—		10	pF

AC ELECTRICAL CHARACTERISTICS [1, 2, 3, 4] (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH64258-10		LH64258-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(1) READ CYCLE							
Random read or write cycle time	t_{RC}	160		190		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	7
Access time from $\overline{CS}$	t_{ACS}		25		30	ns	7
Access time from column address	t_{AA}		50		60	ns	7
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	7
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address delay time ($\overline{RAS}$)	t_{RAD}	20	50	20	60	ns	5
Column address lead time ($\overline{RAS}$)	t_{RAL}	50		60		ns	
Column address hold time ($\overline{RAS}$)	t_{AHR}	15		15		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		ns	
$\overline{CS}$ precharge time ($\overline{RAS}$ fall)	t_{CRP}	0		0		ns	
$\overline{CS}$ delay time ($\overline{RAS}$)	t_{RCD}	25	75	35	90	ns	6
$\overline{CS}$ lead time ($\overline{RAS}$)	t_{RSL}	25		30		ns	
$\overline{OE}$ command $\overline{RAS}$ lead time	t_{ROL}	0		0		ns	
Output data disable time ($\overline{CS}$)	t_{OFF}		25		30	ns	
Output data disable time ($\overline{OE}$)	t_{OEZ}		25		30	ns	
Output data hold time (address)	t_{AOH}	5		5		ns	
Output data hold time ($\overline{CS}$)	t_{SOH}	0		0		ns	
Output data hold time ($\overline{OE}$)	t_{OOH}	0		0		ns	
Read command set-up time ($\overline{CS}$)	t_{RCS}	0		0		ns	
Read command hold time ($\overline{CS}$)	t_{RCH}	10		10		ns	8
Read command hold time ($\overline{RAS}$ fall)	t_{RRHN}	110		130		ns	8
Read command hold time ($\overline{RAS}$ rise)	t_{RRHP}	10		10		ns	8
Transition time (rise and fall)	t_T	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8	ms	
(2) STATIC COLUMN MODE READ CYCLE							
Static column mode cycle time	t_{SC}	55		65		ns	
Column address hold time ($\overline{RAS}$)	t_{AR}	100		120		ns	
(3) WRITE CYCLE (EARLY WRITE)							
Column address set-up time ($\overline{CS}$)	t_{ASC}	0		0		ns	
Column address hold time ($\overline{CS}$)	t_{CAH}	20		20		ns	
Write command set-up time ($\overline{CS}$)	t_{WCS}	0		0		ns	9
Write command hold time ($\overline{CS}$)	t_{WCH}	15		20		ns	
Data input set-up time	t_{DS}	0		0		ns	
Data input hold time	t_{DH}	20		20		ns	
Write pulse width ($\overline{CS}$)	t_{WP}	15		20		ns	
($\overline{OE}$ CONTROL WRITE)							
$\overline{CS}$ set-up time ($\overline{WE}$)	t_{CWS}	0		0		ns	9
$\overline{CS}$ hold time ($\overline{WE}$)	t_{CWH}	15		20		ns	
Write command lead time ($\overline{RAS}$)	t_{RWL}	30		40		ns	
Write pulse width ($\overline{WE}$)	t_{WP}	15		20		ns	
$\overline{OE}$ hold time ($\overline{WE}$)	t_{OEH}	20		20		ns	10
Column address set-up time ($\overline{WE}$)	t_{ASW}	0		0		ns	
Column address hold time ($\overline{WE}$)	t_{WAH}	20		20		ns	

See next page for notes.

PARAMETER	SYMBOL	LH64258-10		LH64258-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(4) READ-WRITE CYCLE							
Read-write cycle time	t_{RWC}	225		270		ns	
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	135		160		ns	
Column address delay time ($\overline{WE}$)	t_{AWD}	85		100		ns	
$\overline{WE}$ delay time ($\overline{CS}$)	t_{CWD}	60		70		ns	
$\overline{OE}$ delay time	t_{OED}	25		30		ns	
(5) STATIC COLUMN MODE WRITE CYCLE							
$\overline{WE}$ inactive time	t_{WI}	10		15		ns	
$\overline{CS}$ inactive time	t_{CI}	10		15		ns	
$\overline{CS}$ set-up time ($\overline{WE}$)	t_{CWS}	15		20		ns	11
Write command delay time ($\overline{RAS}$)	t_{RWD2}	100		120		ns	
(6) $\overline{CS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE/HIDDEN REFRESH CYCLE							
$\overline{CS}$ set-up time ($\overline{RAS}$)	t_{CSR}	0		0		ns	
$\overline{CS}$ hold time ($\overline{RAS}$)	t_{CHR}	20		25		ns	
$\overline{CS}$ precharge time ($\overline{RAS}$ rise)	t_{RPCP}	10		10		ns	
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0		0		ns	
$\overline{CS}$ precharge time ($\overline{RAS}$ fall)	t_{RCPN}	100		120		ns	

NOTES:

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristics assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. I_{CC} when power on depends on $\overline{RAS}$ input level.
   If $\overline{RAS}$ = V_{IL} when power on, LSI goes into an active cycle and may have a large current I_{CC}. It is recommended to rise $\overline{RAS}$ with V_{CC} or fix at V_{IH}, when power on.
5. t_{RAD} (MAX.), is the maximum point for t_{RAD} where t_{AA} (MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RAD} \geq t_{RAD}$ (MAX.), the access time comes under the control of t_{AA}.
6. t_{RCD} (MAX.) is the maximum point for t_{RCD} where t_{ACS} (MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time comes under the control of t_{ACS}.
7. 2TTL + 100 pF load
8. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
9. t_{WCS}, t_{CWS} are not restrictive operating parameters. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out buffers remain inactive throughout entire cycle.
10. t_{OEH} is required to keep I/O pin floating.
    When $\overline{OE}$ goes "Low" with $\overline{CS}$ = "Low" and $\overline{WE}$ = "High", I/O pin is used to output data as written.
11. t_{CWS} is not restrictive operating parameter. When $t_{CWS} \leq t_{CWS}$ (MIN.), it may come into early write cycle.

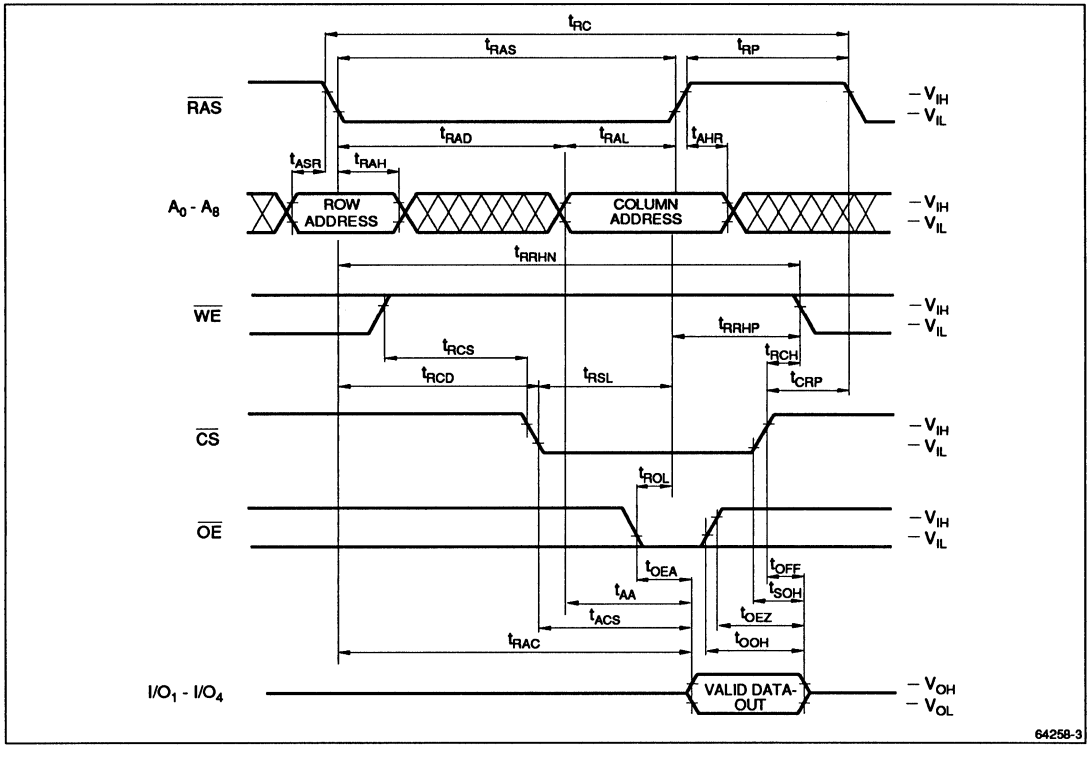


Figure 3. Read Cycle

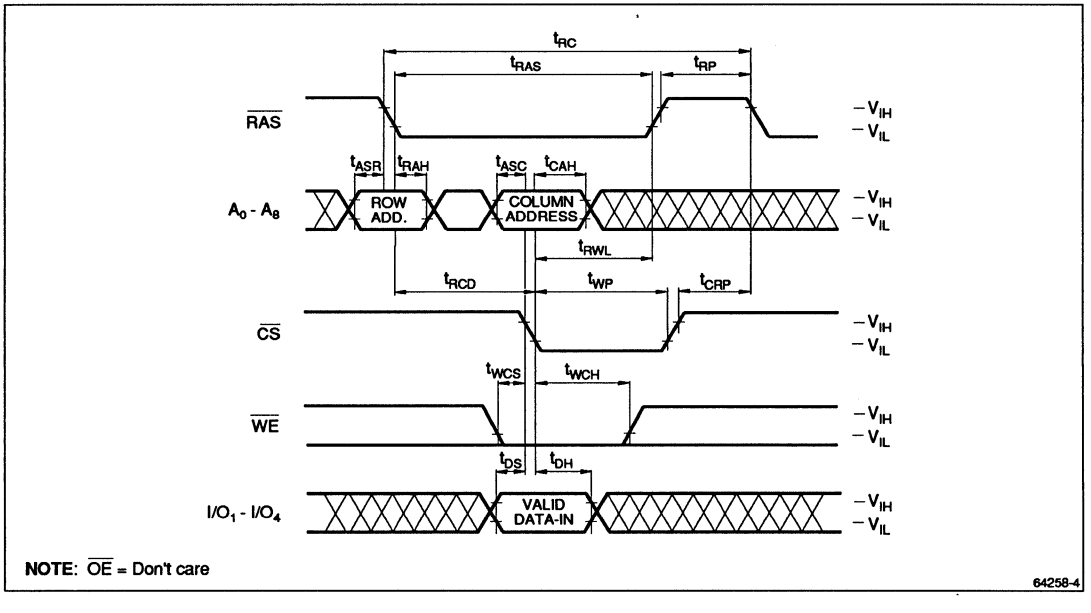


Figure 4. Write Cycle (Early Write)

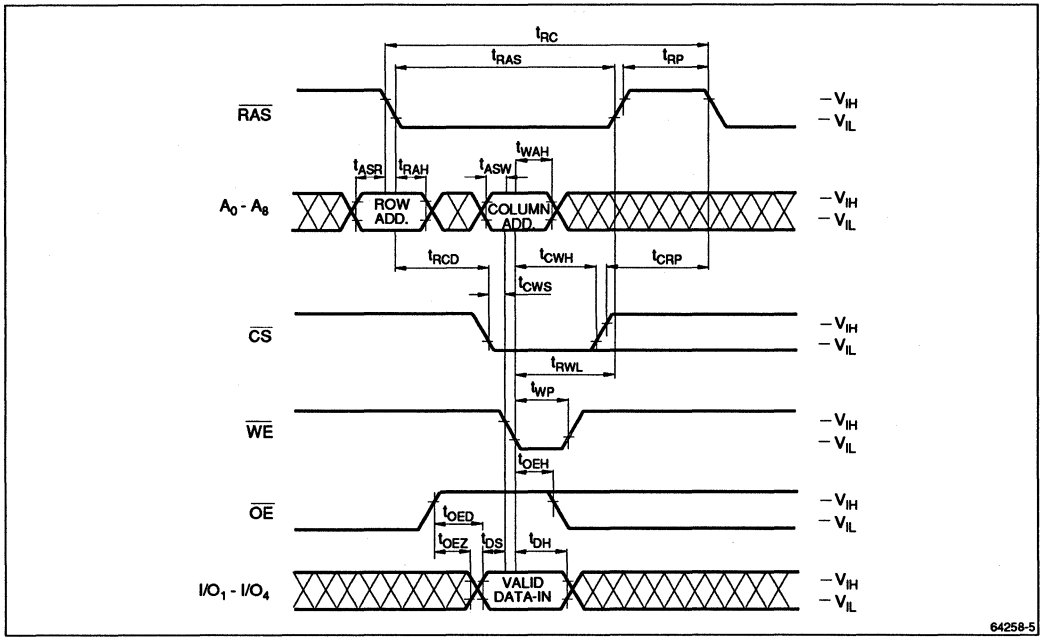


Figure 5. Write cycle ($\overline{OE}$ Controlled Write)

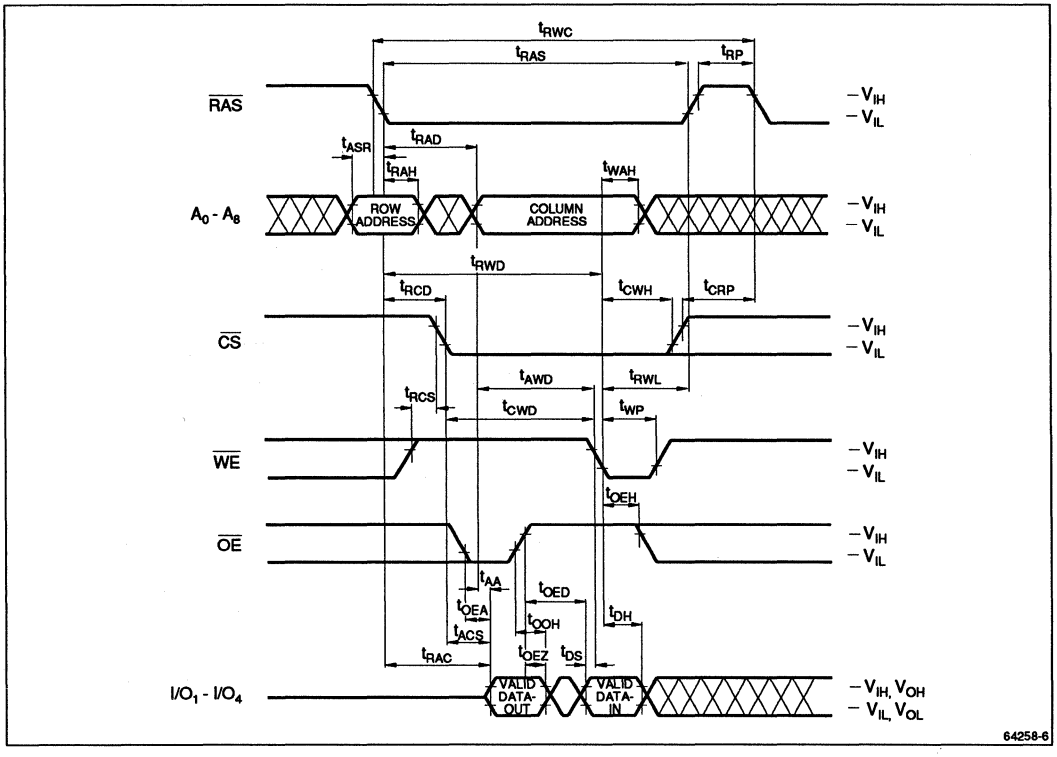


Figure 6. Read/Write Cycle

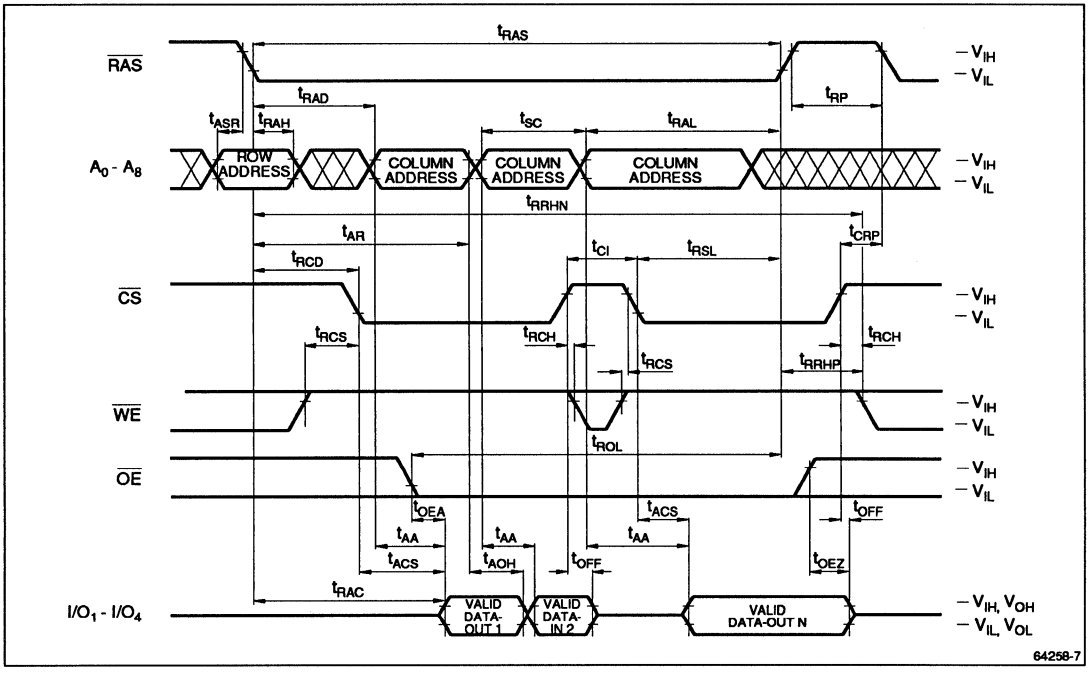


Figure 7. Static Column Mode Read Cycle

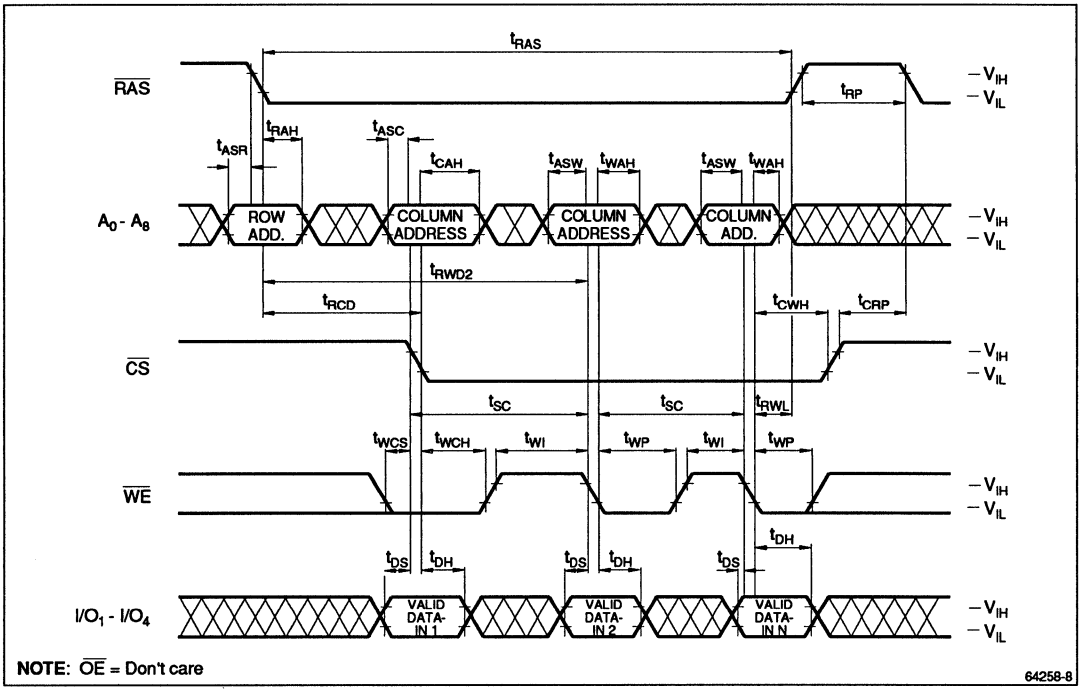


Figure 8. Static Column Mode Write Cycle (Early Write)

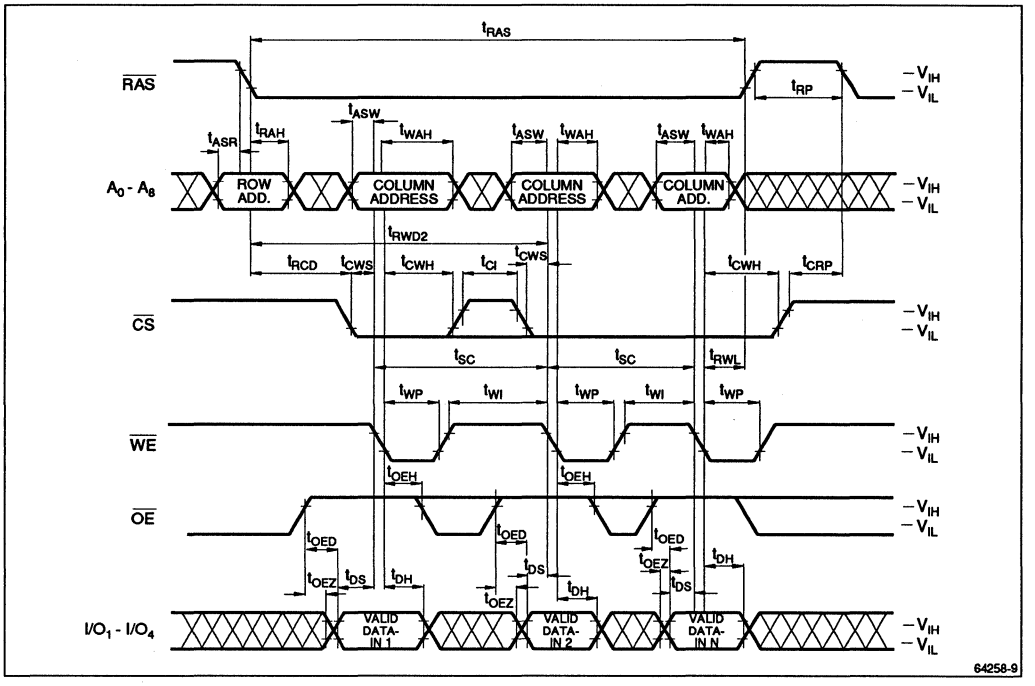


Figure 9. Static Column Mode Write Cycle ($\overline{OE}$ Control Write)

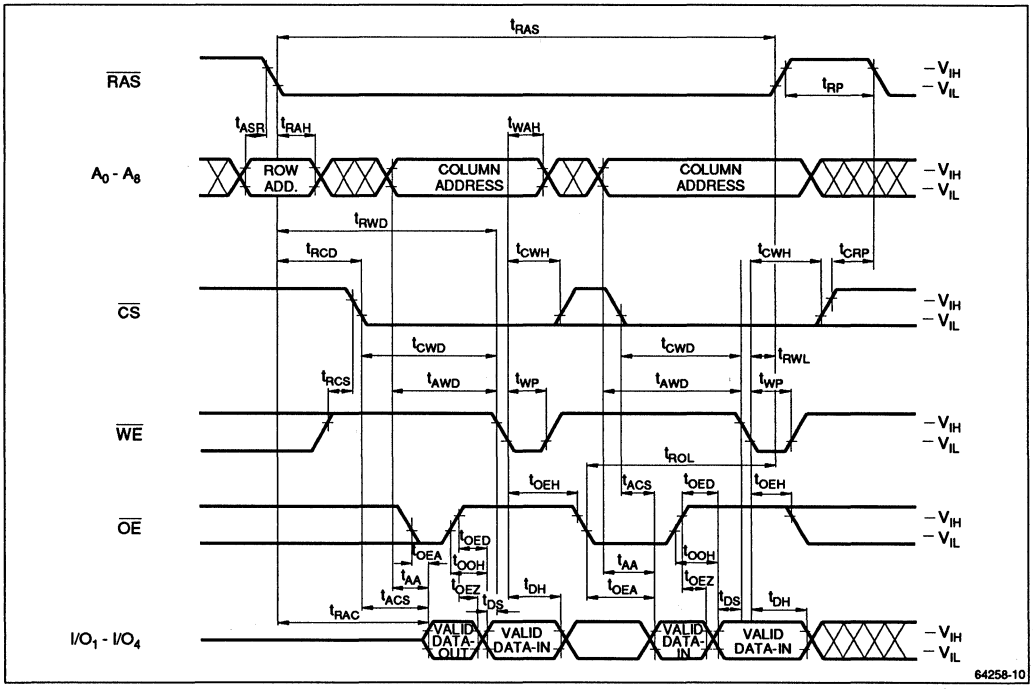


Figure 10. Static Column Mode Read/Write Cycle

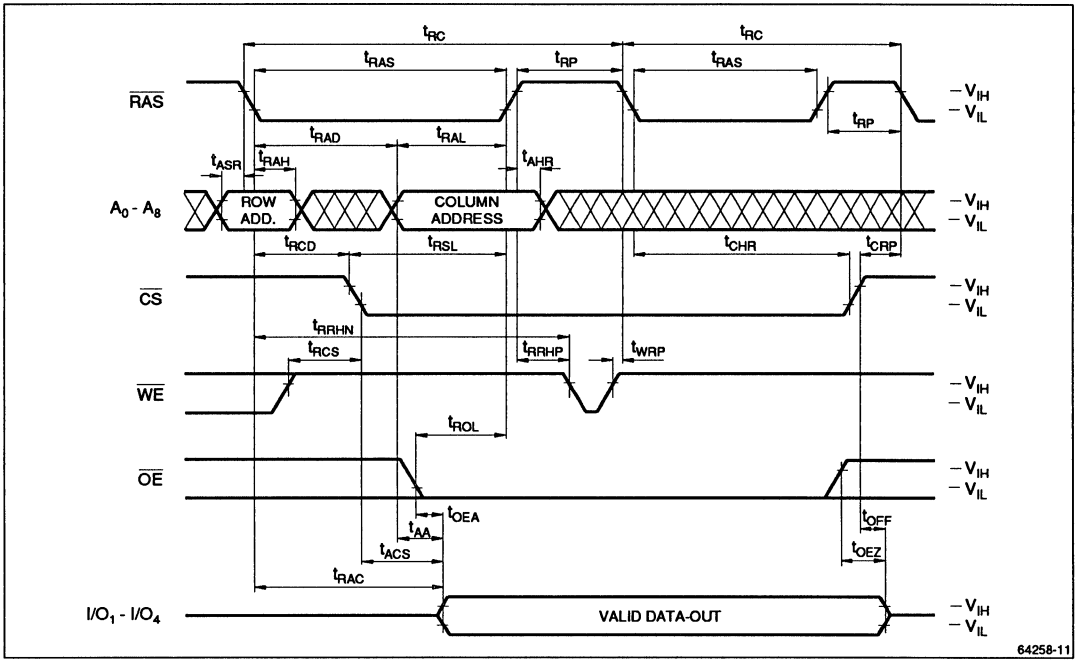


Figure 11. Hidden Refresh Cycle

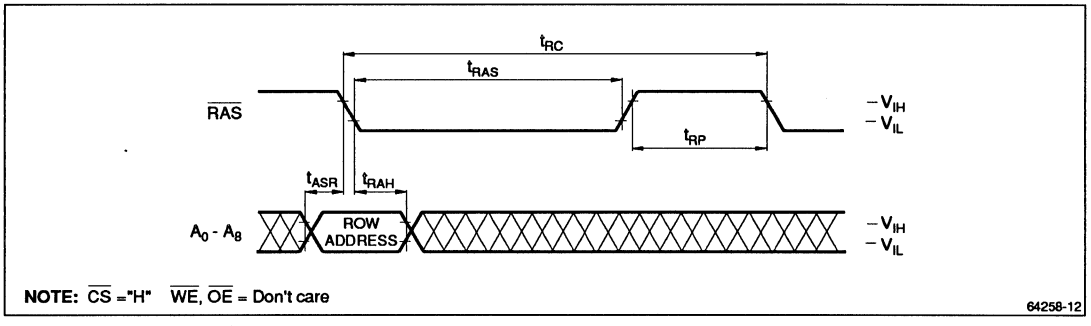


Figure 12. $\overline{RAS}$ Only Refresh Cycle

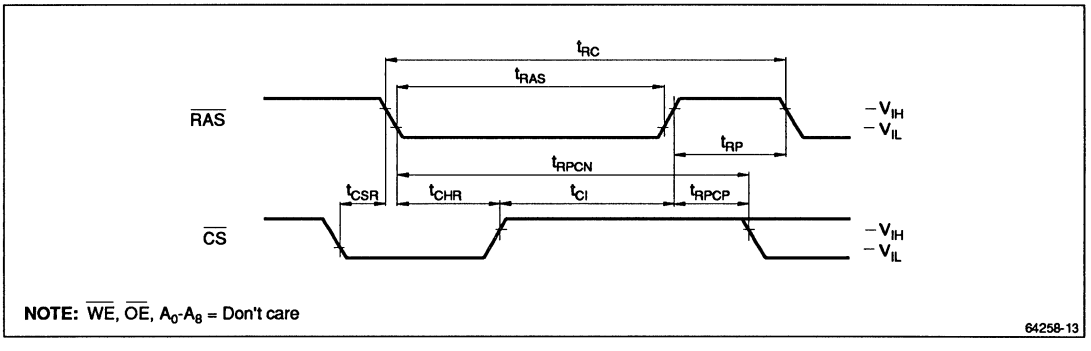
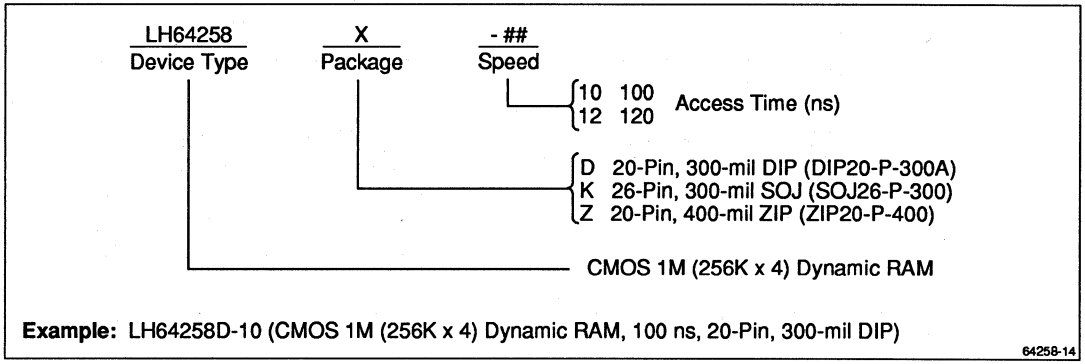


Figure 13. $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

ORDERING INFORMATION



LH64400

PRELIMINARY

CMOS 4M (1M × 4) Dynamic RAM

FEATURES

- 1,048,576 × 4 bit organization
- Access times: 80/100 ns (MAX.)
- Cycle times: 140/160 ns (MIN.)
- Cycle time in high speed page mode: 50/55 ns (MIN.)
- Power supply: +5 V ± 10%
- Power consumption (MAX.):
  Operating: 523/468 mW (MAX.)
  Standby: 5.5 mW (MAX.)
- TTL compatible I/O
- Early-write or $\overline{OE}$ control allows bus management of the data-out buffer
- $\overline{RAS}$ only refresh, Hidden refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- 8-bit parallel test mode
  (contact SHARP for details)
- 1,024 refresh cycle
  (refresh period (MAX.) = 16 ms)
- Packages:
  20-pin, 300-mil DIP
  26-pin, 300-mil SOJ
  20-pin, 400-mil ZIP
  26-pin, 300-mil TSOP
  (normal/reverse bend pins)

DESCRIPTION

The LH64400 is a 1,048,576 × 4 bit dynamic RAM which provides a high speed page mode operation.

The LH64400 is fabricated using advanced CMOS process technology. With multiplexed address inputs and standard 20-pin DIP/ZIP or 26-pin SOJ/TSOP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH64400 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

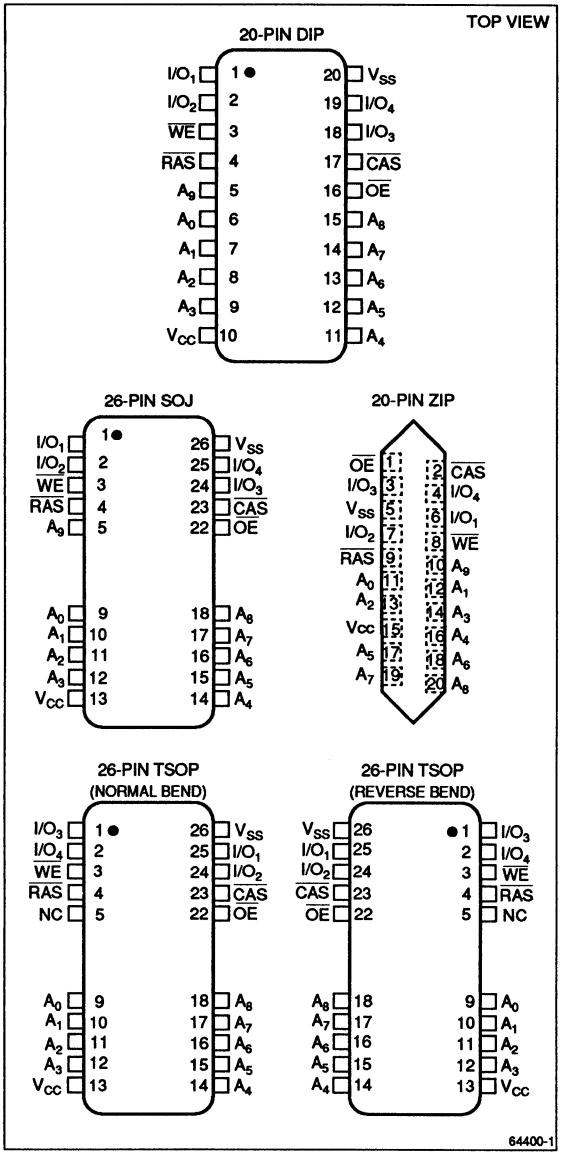


Figure 1. Pin Connections for DIP, SOJ, ZIP, and TSOP Packages

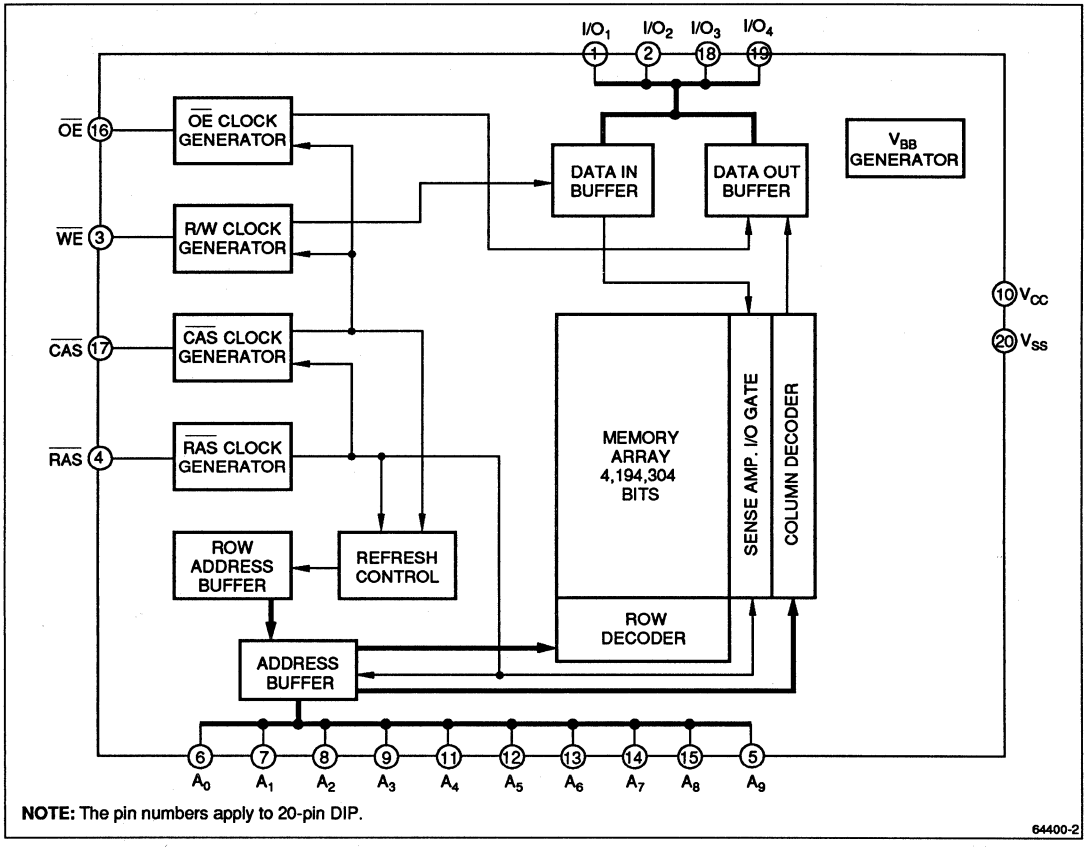


Figure 2. LH64400 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_9	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
$\overline{OE}$	Output enable
I/O_1 - I/O_4	Data input/output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_{OS}	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8	V	1

NOTE:
1. Referenced to V_{SS}

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH64400-80	I_{CC1}	—	95	mA	1, 2, 3
	LH64400-10		—	85		
Supply current in standby mode		I_{CC2}	—	1.0	mA	1
Average supply current in high speed page mode	LH64400-80	I_{CC3}	—	70	mA	1, 2
	LH64400-10		—	60		
Average supply current in $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	LH64400-80	I_{CC6}	—	95	mA	1, 2, 3
	LH64400-10		—	85		
Average supply current in $\overline{RAS}$ only refresh cycle	LH64400-80	I_{CC7}	—	95	mA	1, 2, 3
	LH64400-10		—	85		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	I_{LI}	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	I_{LO}	-10	10	µA	
Output "High" voltage	I_{OUT} = -5 mA	V_{OH}	2.4	—	V	
Output "Low" voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7} depend on the cycle time.
3. Address transition occurs when $\overline{RAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_9	C_{IN1}	—	5	pF
	$\overline{RAS}$, $\overline{CAS}$	C_{IN2}	—	5	pF
	$\overline{WE}$, $\overline{OE}$	C_{IN3}	—	5	pF
Input/output capacitance	I/O_1 - I/O_4	C_{OUT1}	—	7	pF

AC CHARACTERISTICS [1,2,3,4] (T_A = 0 to +70°C, V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	LH64400-80		LH64400-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
(1) READ CYCLE							
Random read/write cycle time	t_{RC}	140		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	7
Access time from $\overline{CAS}$	t_{CAC}		25		30	ns	7
Access time from column address	t_{AA}		40		50	ns	7
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	7
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address delay time ($\overline{RAS}$)	t_{RAD}	15	40	20	50	ns	5
Column address lead time ($\overline{RAS}$)	t_{RAL}	40		50		ns	
Column address hold time ($\overline{RAS}$)	t_{CAH}	15		20		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ precharge time	t_{RP}	50		50		ns	
$\overline{CAS}$ precharge time ($\overline{RAS}$ fall)	t_{CRP}	0		0		ns	
$\overline{CAS}$ delay time ($\overline{RAS}$)	t_{RCD}	20	55	25	70	ns	6
$\overline{CAS}$ lead time ($\overline{RAS}$)	t_{RSL}	25		30		ns	
$\overline{OE}$ command $\overline{RAS}$ lead time	t_{ROL}	0		0		ns	
Output data disable time ($\overline{CAS}$)	t_{OFF}		20		25	ns	
Output data disable time ($\overline{OE}$)	t_{OEZ}		20		25	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10,000	30	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
Output data hold time ($\overline{CAS}$)	t_{SOH}	0		0		ns	
Output data hold time ($\overline{OE}$)	t_{OOH}	0		0		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time ($\overline{CAS}$)	t_{RCH}	10		10		ns	8
Read command hold time ($\overline{RAS}$ rise)	t_{RRH}	10		10		ns	8
Transition time (rise and fall)	t_T	3	50	3	50	ns	
Refresh time interval	t_{REF}		16		16	ms	
(2) HIGH SPEED PAGE MODE READ CYCLE							
High speed page mode cycle time	t_{PC}	50		55		ns	
$\overline{CAS}$ precharge time	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge access time ($\overline{CAS}$ rise)	t_{CACP}	45		50		ns	7, 10
$\overline{RAS}$ pulse width	t_{RASP}	80	10,000	100	10,000	ns	
High speed page mode read write cycle time	t_{PRWC}	105		115		ns	11
(3) WRITE CYCLE EARLY WRITE)							
Data input setup time	t_{DS}	0		0		ns	
Data input hold time	t_{DH}	15		15		ns	
Write command set-up time	t_{WCS}	0		0		ns	9
Write command hold time	t_{WCH}	10		15		ns	
($\overline{OE}$ CONTROL)							
$\overline{CAS}$ set-up time ($\overline{WE}$)	t_{CWS}	0		0		ns	9
Write command lead time ($\overline{RAS}$)	t_{RWL}	20		25		ns	
Write command lead time ($\overline{CAS}$)	t_{CWL}	20		25		ns	
Write pulse width ($\overline{WE}$)	t_{WP}	15		15		ns	
OE hold time ($\overline{WE}$)	t_{OEH}	20		20		ns	
(4) READ-WRITE CYCLE							
Read-write cycle time	t_{RWC}	195		225		ns	11
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	110		135		ns	11
Column address delay time ($\overline{WE}$)	t_{AWD}	70		85		ns	11
$\overline{WE}$ delay time ($\overline{CAS}$)	t_{CWD}	55		65		ns	11
$\overline{OE}$ delay time	t_{OED}	20		25		ns	
(5) $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE/HIDDEN REFRESH CYCLE							
$\overline{CAS}$ set-up time ($\overline{RAS}$)	t_{CSR}	0		0		ns	
$\overline{CAS}$ hold time ($\overline{RAS}$)	t_{CHR}	20		20		ns	
$\overline{RAS}$/$\overline{CAS}$ precharge time ($\overline{RAS}$ rise)	t_{RPC}	10		10		ns	
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0		0		ns	
$\overline{WE}$/$\overline{RAS}$ hold time	t_{WRH}	10		10		ns	
$\overline{CAS}$ precharge time ($\overline{RAS}$ fall)	t_{CPN}	10		10		ns	

* See next page for notes.

NOTES:

1. For proper operation, at least 200 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristic assume t_T = 5 ns. (t_T refers to the transition time between V_{IH} and V_{IL}.)
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
4. I_{CC} when power on depends on $\overline{RAS}$ input level.
   If $\overline{RAS}$ = V_{IL} when power on, LSI goes into an active cycle and may have a large current I_{CC}. It is recommended to rise $\overline{RAS}$ with V_{CC} or fix at V_{IH} when power on.
5. t_{RCD} (MAX.), is the maximum point for t_{RAD} where t_{AA} (Max.) is ensured, and does not represent a limit of operation.
   If $t_{RAD} \geq t_{RAD}$ (MAX.), the access time comes under the control of t_{AA}.
6. t_{RCD} (MAX.), is the maximum point for t_{RAD} where t_{CAC} (MAX.) is ensured, and does not represent a limit of operation.
   If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time will come under the control of t_{CAC}.
7. 2TTL + 100 pF load.
8. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.
9. t_{WCS} is not a restrictive operating parameter. It comes into early write cycle with the WE = "Low" at the falling edge of $\overline{CAS}$. Then, I/O pins remain inactive until the $\overline{CAS}$ = "High" irrespective of $\overline{WE}$.
10. If $t_{CACP} \geq t_{CP} + t_{CAC} + t_T$, the access time depends upon t_{CACP}.
11. t_{RWC}, t_{RWD}, t_{AWD}, t_{CWD} and t_{PRWC} are not restrictive operating parameters.

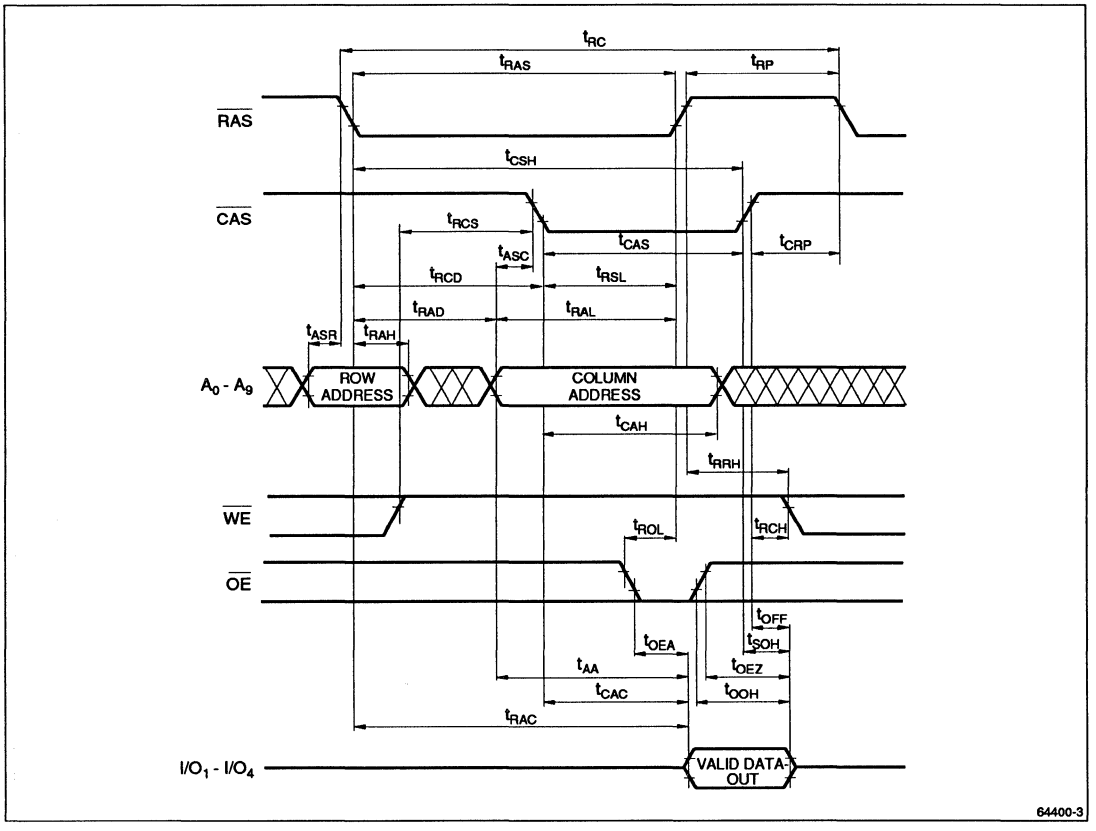


Figure 3. Read Cycle

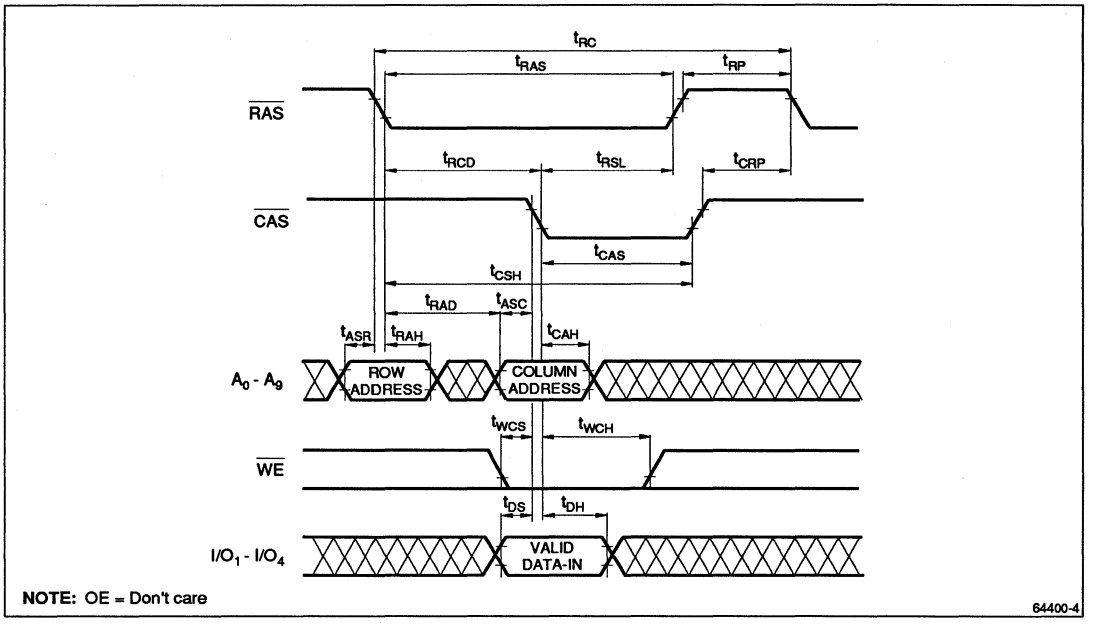


Figure 4. Write Cycle (Early Write)

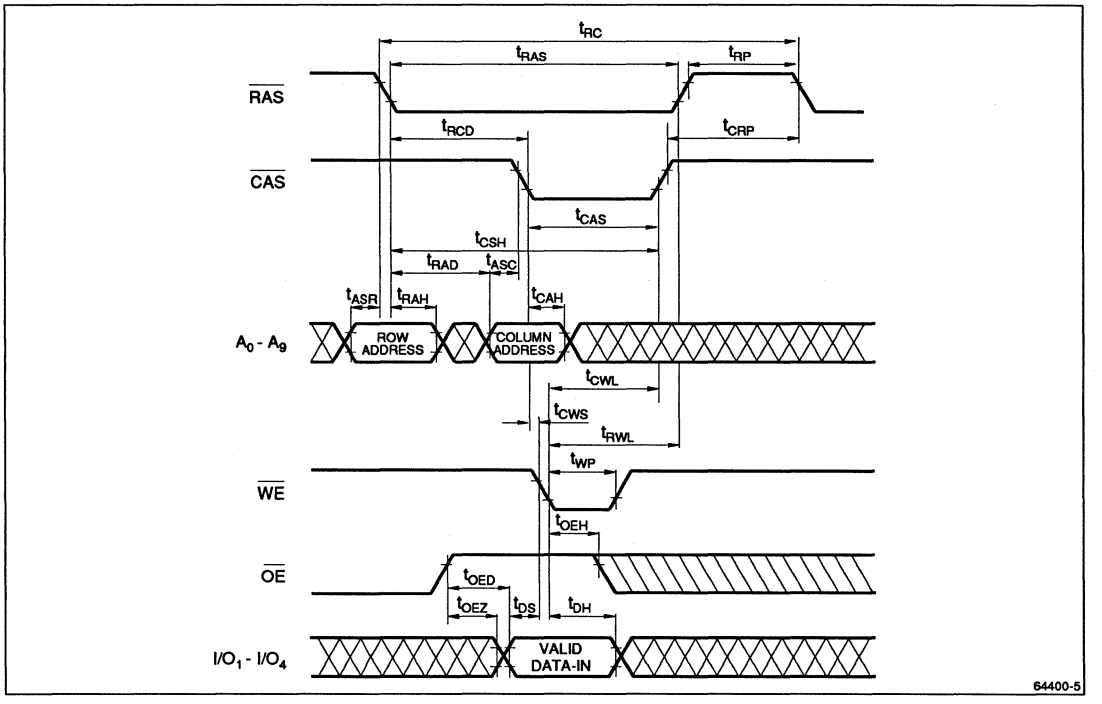


Figure 5. Write Cycle ($\overline{OE}$ Control)

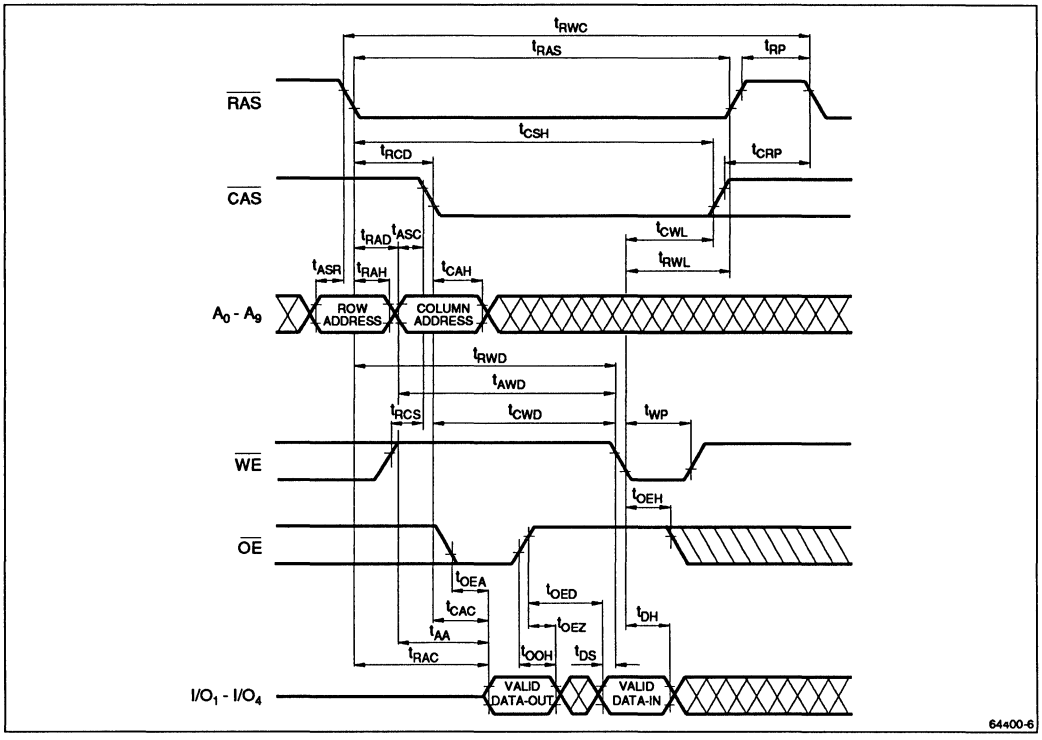


Figure 6. Read/Write Cycle

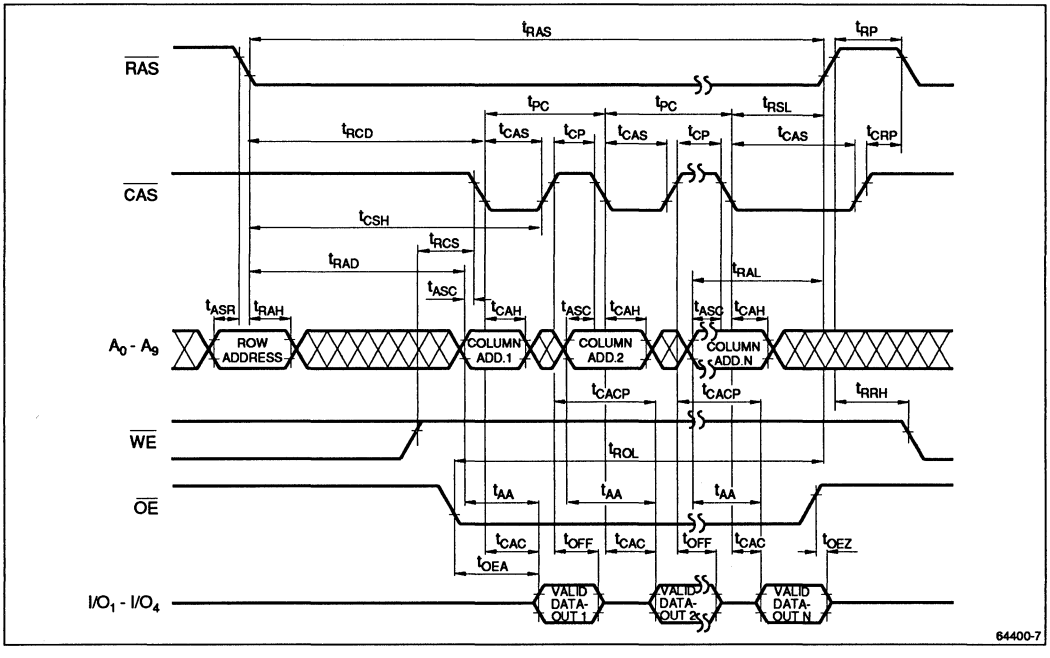


Figure 7. High Speed Page Mode Read Cycle

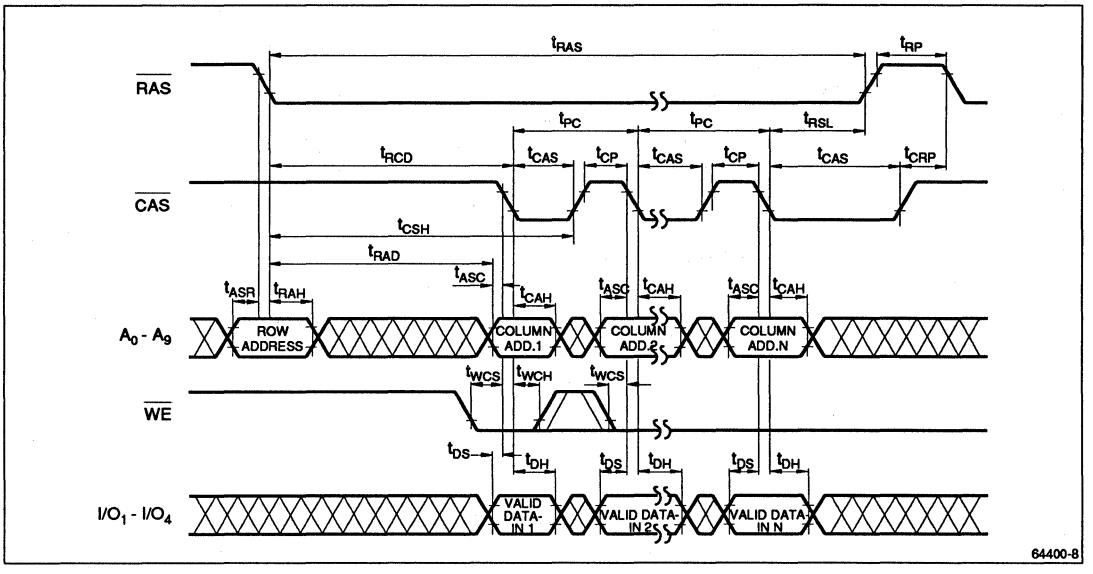


Figure 8. High Speed Page Mode Write Cycle

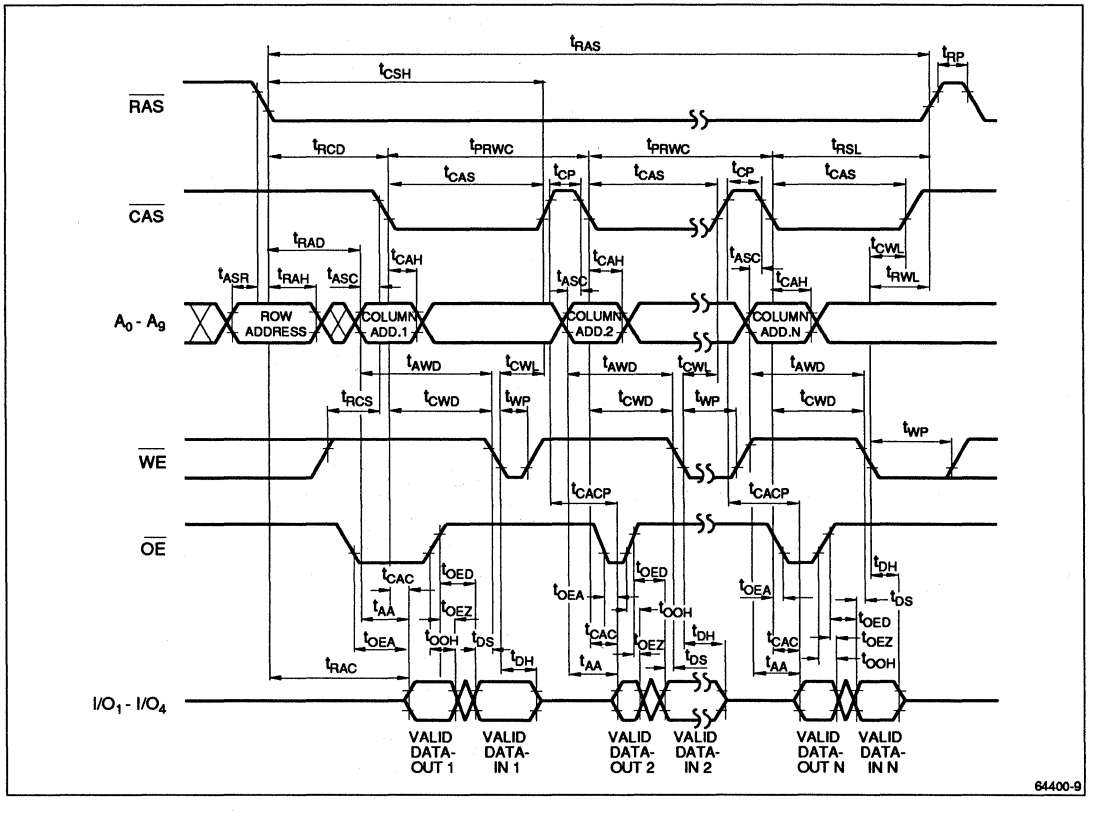


Figure 9. High Speed Page Mode Write Cycle

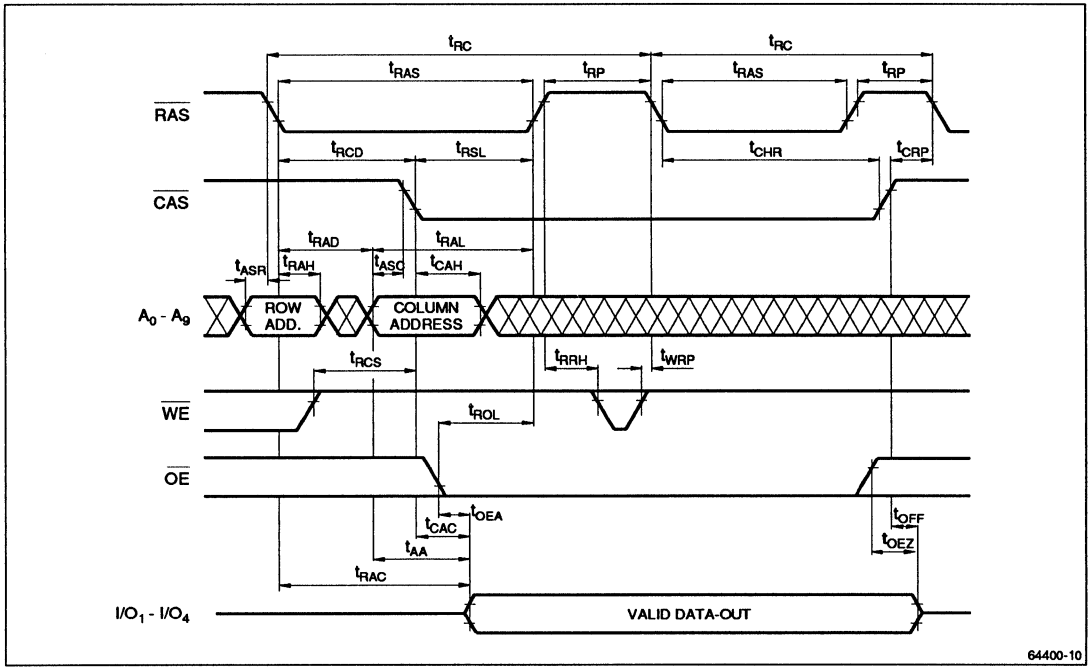


Figure 10. Hidden Refresh Cycle

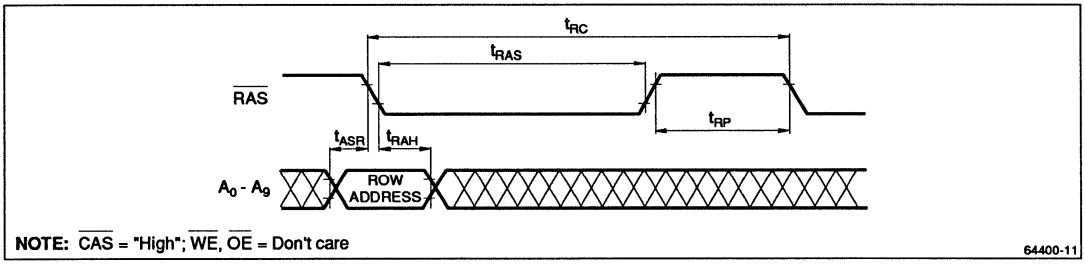


Figure 11. $\overline{RAS}$ Only Refresh Cycle

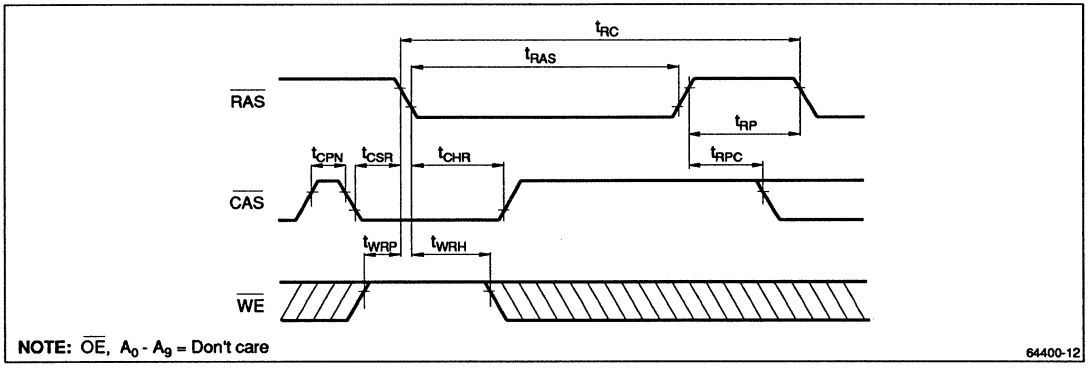
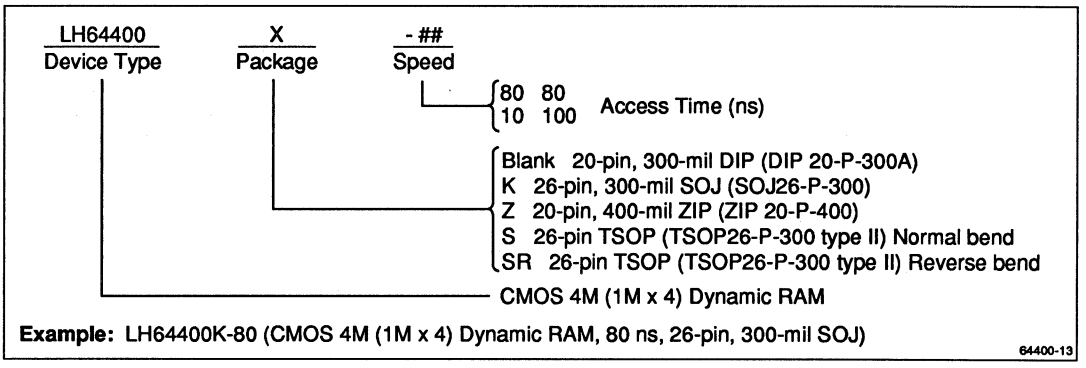


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

ORDERING INFORMATION



Example: LH64400K-80 (CMOS 4M (1M x 4) Dynamic RAM, 80 ns, 26-pin, 300-mil SOJ)

LH5P832

CMOS 256K (32K × 8) Pseudo-Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time:
  120 ns (MAX.)
- Cycle time:
  190 ns (MIN.)
- Power consumption:
  Operating: 303 mW
  Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycle/4 ms
- Auto refresh is executed by internal counter (controlled by $\overline{OE}$/$\overline{RFSH}$ pin)
- Self refresh is executed by internal timer
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH5P832 is a 256K bit Pseudo Static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5P832 uses convenient on-chip refresh circuitry with a DRAM memory cell for pseudo static operation. This simplifies external clock inputs, while providing the same simple, non-multiplexed pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, many 32K × 8 SRAM sockets can be filled with the LH5P832 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P832 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low standby power, and a simple interface.

Three methods of refresh control are provided for maximum versatility. A 'CE-Only' refresh cycle refreshes the addressed row of memory cells transparently. All 256 rows must be refreshed or accessed every four milliseconds. 'Auto Refresh' automatically cycles through a different row on every OE/RFSH clock pulse, accomplishing the row refreshes without the need to supply row addresses externally. 'Self Refresh' further simplifies the refresh requirements by eliminating the need for address inputs and clock pulses entirely. An automatic timer senses time periods when memory accesses have ceased, and provides full refresh of all rows of memory without any external assistance.

PIN CONNECTIONS

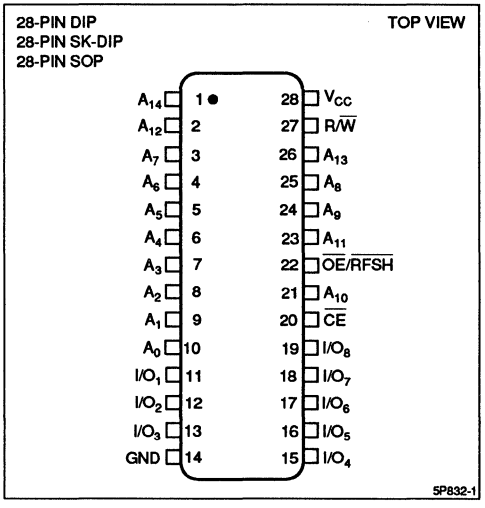


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

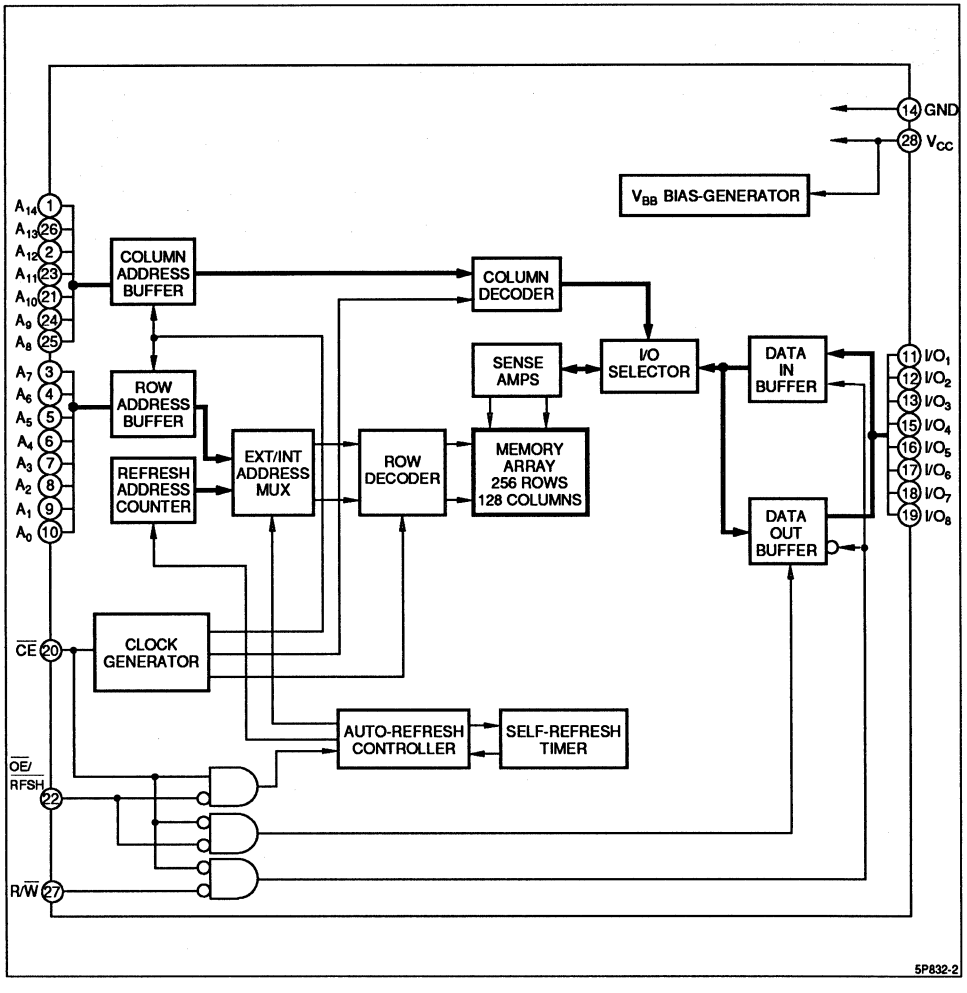


Figure 2. LH5P832 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
R/$\overline{W}$	Read/Write input
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh input
I/O_1 - I/O_8	Data inputs and outputs
A_0 - A_7	Row address inputs

SIGNAL	PIN NAME
A_8 - A_{14}	Column Address inputs
$\overline{CE}$	Chip Enable input
Vcc	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$/$\overline{RFSH}$	MODE	I/O_1 - I/O_8	Icc	NOTE
L	L	X	Write	Data in	Operating (Icc)	1
L	H	L	Read	Data out	Operating (Icc)	
L	H	H	$\overline{CE}$-Only Refresh	High-Z	Operating (Icc)	
H	X	L	Auto Refresh	High-Z	Operating	1, 2
H	X	L	Self Refresh	High-Z	Standby	1, 3

NOTES:
1. X = H or L 2. $\overline{OE}$ Pulsewidth < 8 µs 3. $\overline{OE}$ Pulsewidth ≥ 8 µs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		+0.8	V

CAPACITANCE (V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{14}, R/$\overline{W}$	C_{IN1}		8	pF
	$\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$	C_{IN2}		5	pF
Input/output capacitance	I/O_1 - I/O_8	C_{OUT1}		12	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	I_{CC1}	t_{RC} = 190 ns		55	mA	1
Standby current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IH}		3	mA	1
Self refresh average current	I_{CC3}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IL}		3	mA	
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V	-10	10	µA	1
Output High voltage	V_{OH}	I_{OUT} = -1 mA	2.4		V	
Output Low voltage	V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:
1. The output pins are in high-impedance state.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	5 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

AC CHARACTERISTICS

READ AND WRITE CYCLES [1,2] (V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Random read, write cycle time	t_{RC}	190		ns	
Read modify write cycle time	t_{RMW}	280		ns	
$\overline{CE}$ pulse width	t_{CE}	120	10,000	ns	
$\overline{CE}$ precharge time	t_P	60		ns	
Address setup time	t_{AS}	0		ns	
Address hold time	t_{AH}	30		ns	
Read command hold time	t_{RCH}	0		ns	
Read command setup time	t_{RCS}	0		ns	
$\overline{CE}$ access time	t_{CEA}		120	ns	
$\overline{OE}$ access time	t_{OEA}		50	ns	
$\overline{CE}$ to output in Low-Z	t_{CLZ}	10		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
Output enable from end of write	t_{WLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	35	ns	2
Output disable to output in High-Z	t_{OHZ}	0	35	ns	2
Write enable to output in High-Z	t_{WHZ}	0	35	ns	2
$\overline{OE}$ setup time	t_{OES}	10		ns	
$\overline{OE}$ hold time	t_{OEH}	0		ns	
$\overline{OE}$ lead time	t_{OEL}	10		ns	
Write command pulse width	t_{WCP}	85		ns	
Write command setup time	t_{WCS}	85		ns	
Write command hold time	t_{WCH}	85		ns	
Data setup time from write	t_{DSW}	50		ns	
Data setup time from $\overline{CE}$	t_{DSC}	50		ns	
Data hold time from write	t_{DHW}	0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		ns	
Transition time (rise and fall)	t_T	3	35	ns	
Refresh time interval	t_{REF}		4	ms	

REFRESH CYCLE

Auto refresh cycle time	t_{FC}	190		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	60		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	80	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	
$\overline{CE}$ delay time from refresh active (Auto refresh)	t_{FCE}	225		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	225		ns	

NOTES:

1. At least 1 ms of pause time after power on should be given for proper device operation. $\overline{CE}$ and $\overline{OE}$/RFSH must be fixed at V_{IH} for 1 ms from the V_{DD} reached to the specified voltage level.
2. Active output to high-Z and high-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

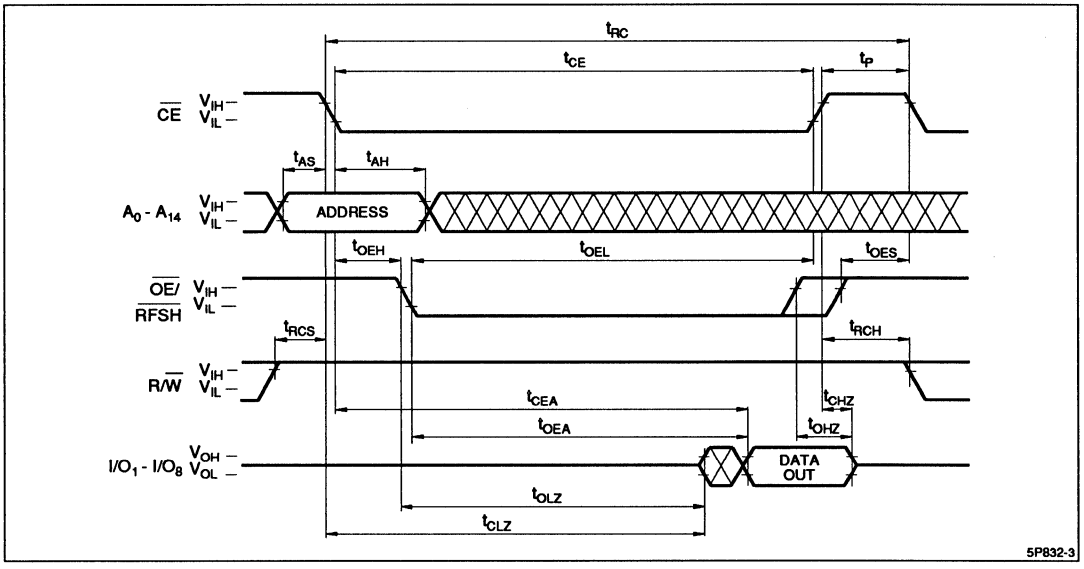


Figure 3. Read Cycle

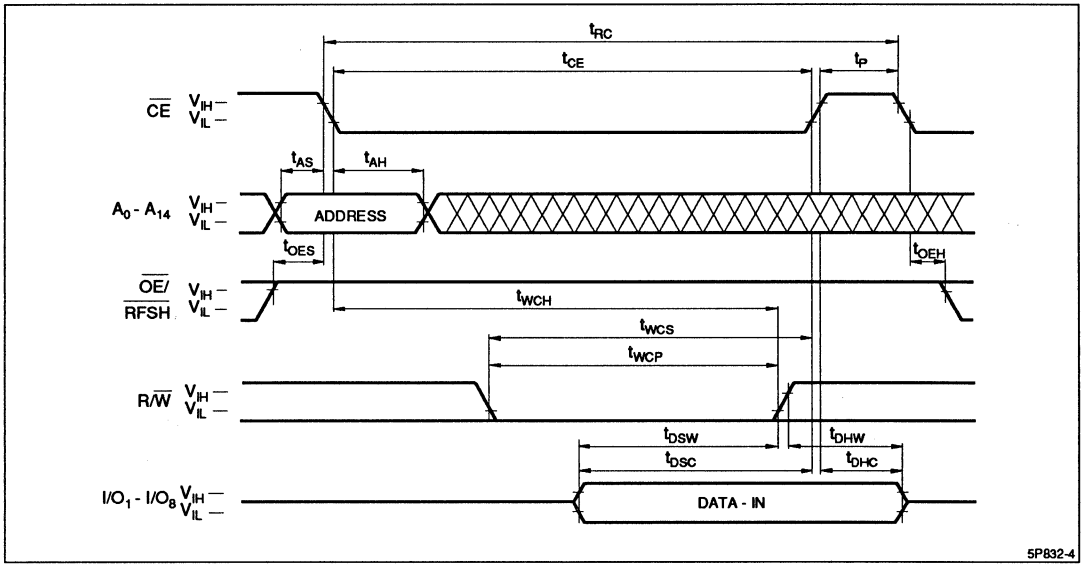


Figure 4. Write Cycle

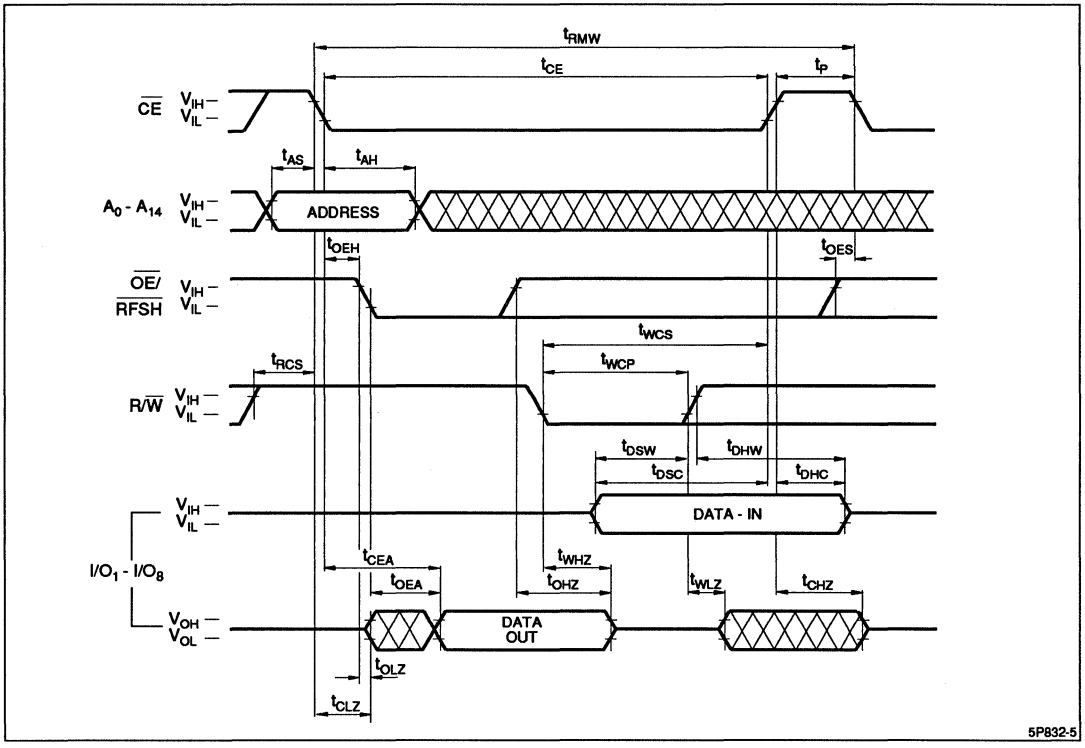


Figure 5. Read/Write Cycle

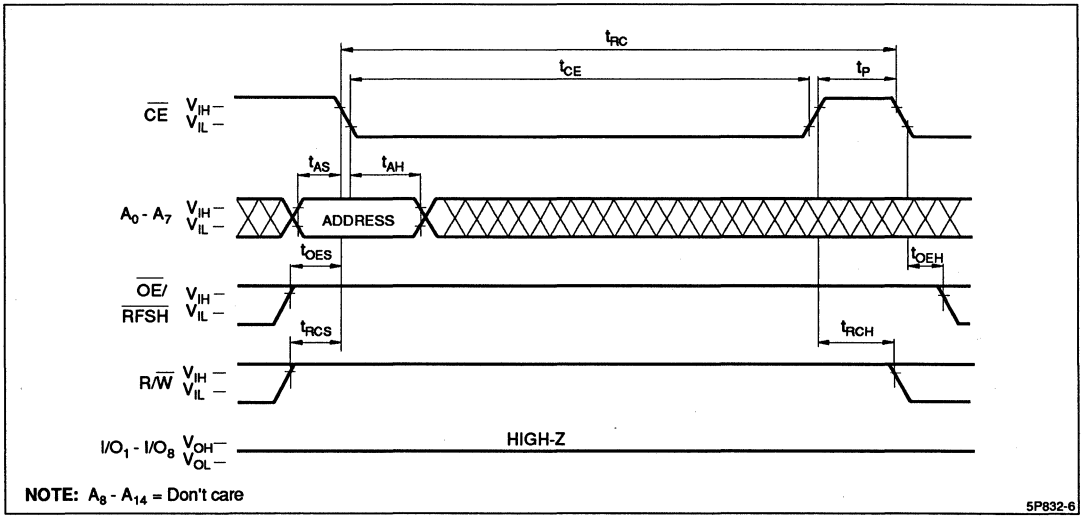


Figure 6. $\overline{CE}$ Only Refresh Cycle

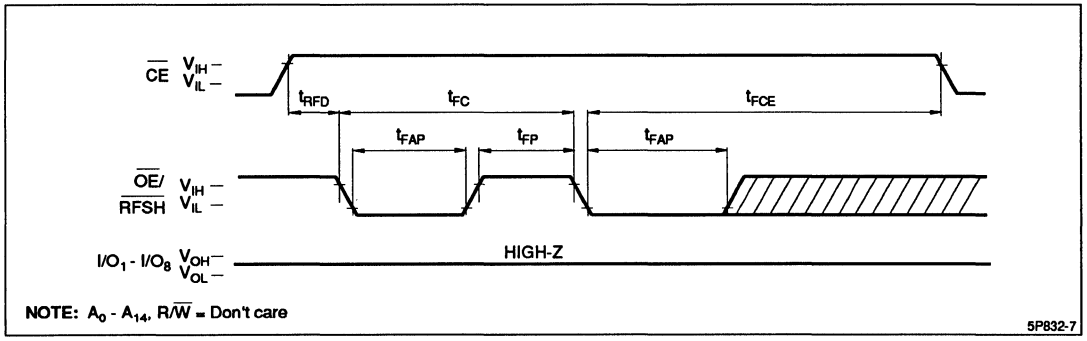


Figure 7. Auto Refresh Cycle

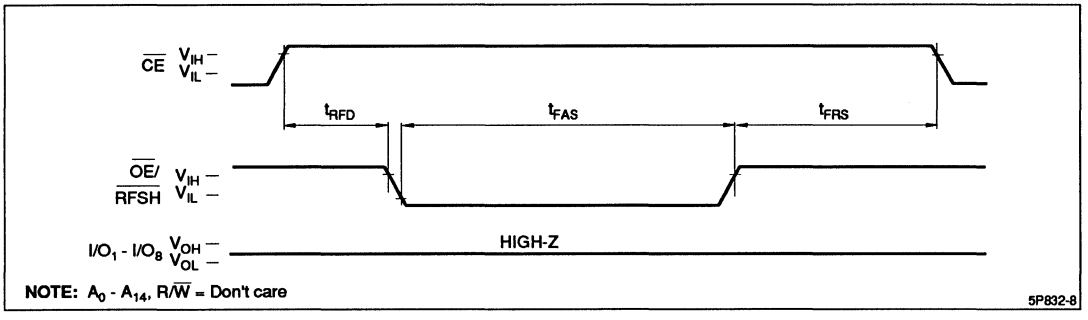
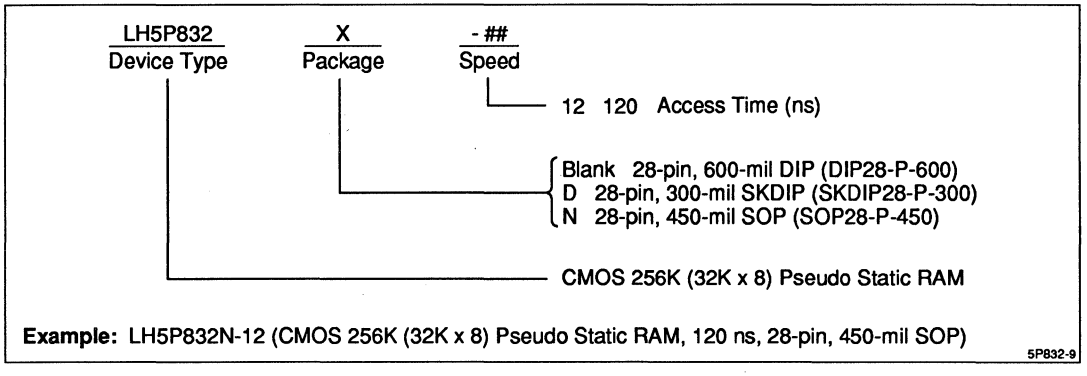


Figure 8. Self Refresh Cycle

ORDERING INFORMATION



LH5P8128

CMOS 1M (128K × 8) Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Power consumption:
  Operating: 572/440/358 mW (MAX.)
  Standby: 275 μW (MAX.) in self-refresh mode
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Compatible with JEDEC standard 1M SRAM pinout
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH5P8128 is a 1M bit Pseudo Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 128K × 8 SRAM sockets can be filled with the LH5P8128 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8128 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and a simple interface.

PIN CONNECTIONS

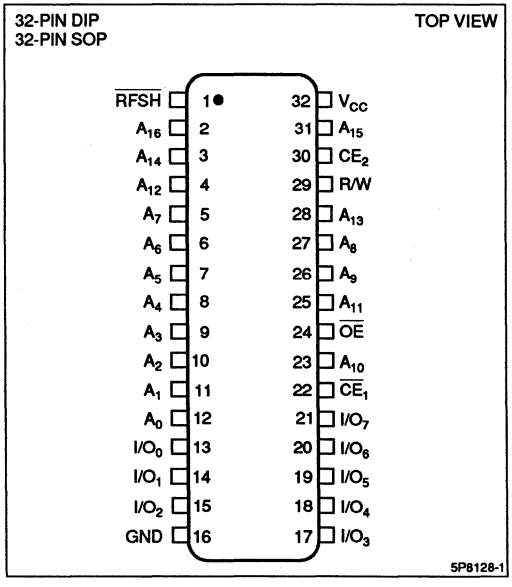


Figure 1. Pin Connections for DIP and SOP Packages

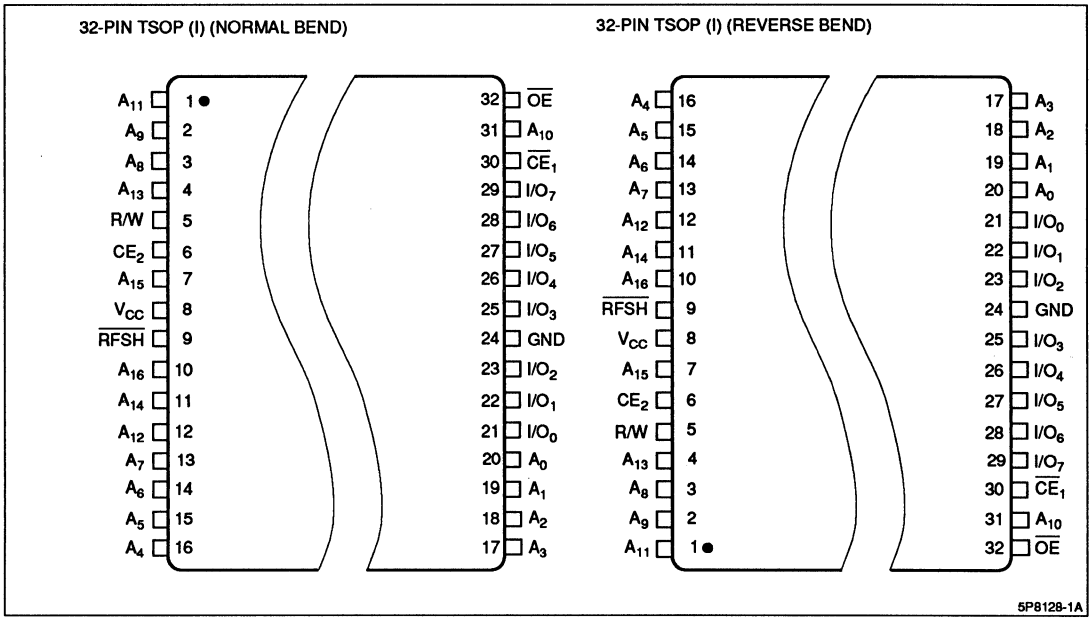


Figure 2. Pin Connections for TSOP Packages

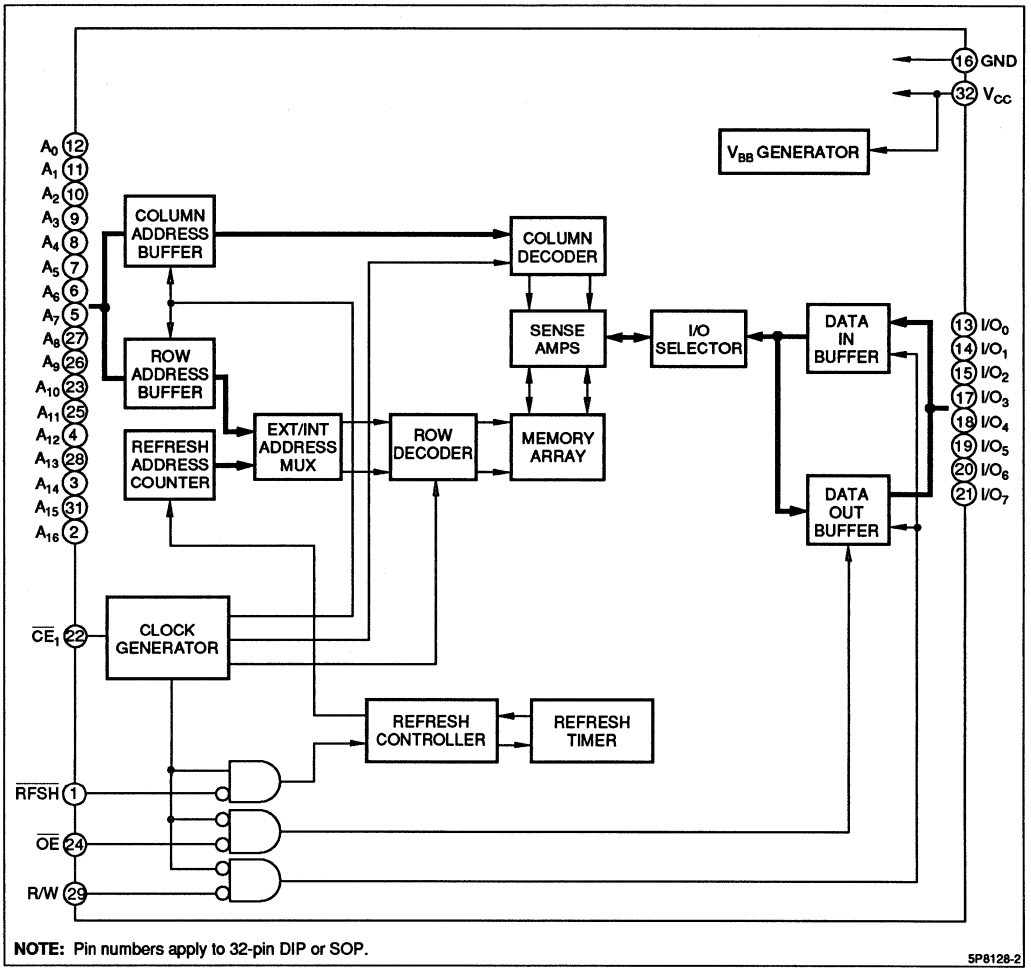


Figure 3. LH5P8128 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{OE}$	Output Enable Input

SIGNAL	PIN NAME
$\overline{CE}_1$, CE_2	Chip Enable input
$\overline{RFSH}$	Refresh input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1MHz, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, $\overline{OE}$	C_{IN2}		5	pF
	$\overline{CE_1}$, CE_2	C_{IN3}		5	pF
	$\overline{RFSH}$	C_{IN4}		5	pF
Input/output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8128-60	I_{CC1}	t_{RC} = t_{RC} (MIN)		104	mA	1, 2
	LH5P8128-80				80		
	LH5P8128-10				65		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.05		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.05		1, 6
CPU internal cycle average current	LH5P8128-60	I_{CC4}	(R/W = $\overline{OE}$ = V_{IH})		104	mA	1, 2
	LH5P8128-80				80		
	LH5P8128-10				65		
Input leakage current		I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other test pins	-10	10	µA	
I/O leakage current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = 1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:

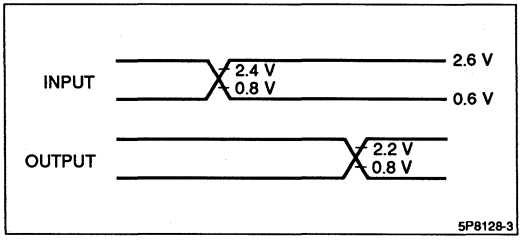
1. The output pins are in high-impedance state
2. I_{CC1} and I_{CC4} depend on the cycle time
3. $\overline{CE_1}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}
4. $\overline{CE_1}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = V_{CC} - 0.2 V
5. $\overline{CE_1}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}
6. $\overline{CE_1}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = 0.2 V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER	SYMBOL	LH5P8128-60		LH5P8128-80		LH5P8128-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	155		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
$\overline{CE}$ access time	t_{CEA}		60		80		100	ns	5
$\overline{OE}$ access time	t_{OEA}		25		30		35	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		20		20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
$\overline{OE}$ setup time	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time	t_{OEH}	10		10		10		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE_1}$ should be kept at V_{IH} or CE_2 should be kept at V_{IL} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE_1}$ or at the positive edge of CE_2.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of W/R or at the positive edge of $\overline{CE_1}$ or at the negative edge of CE_2.



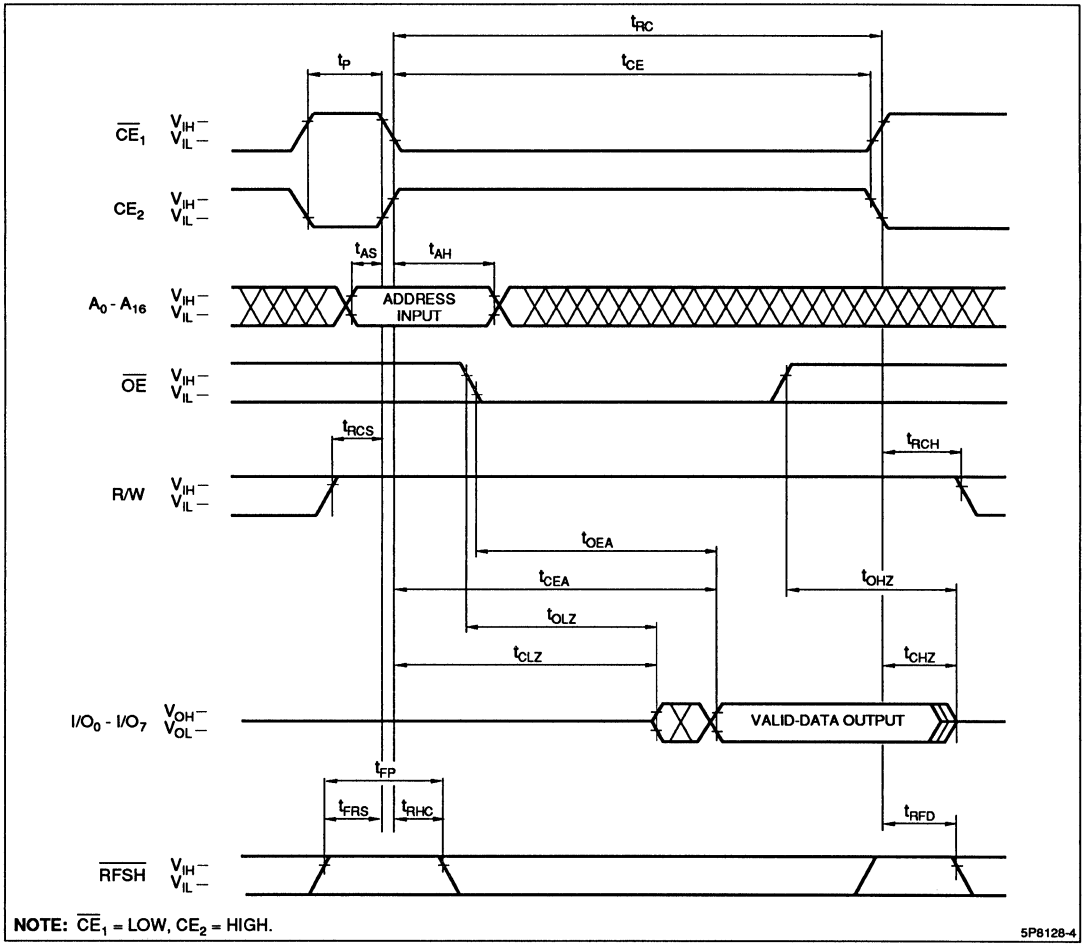


Figure 4. Read Cycle

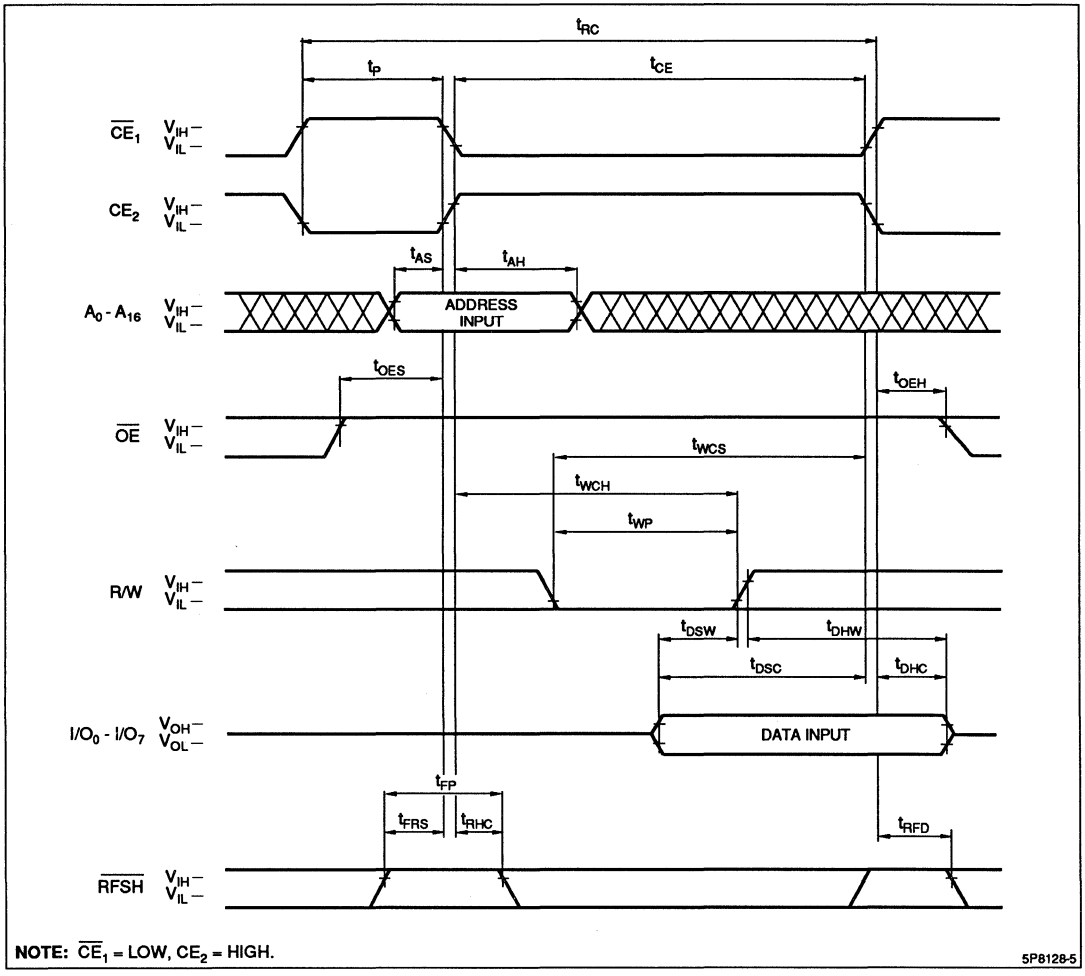


Figure 5. Write Cycle 1 ($\overline{OE}$ = HIGH)

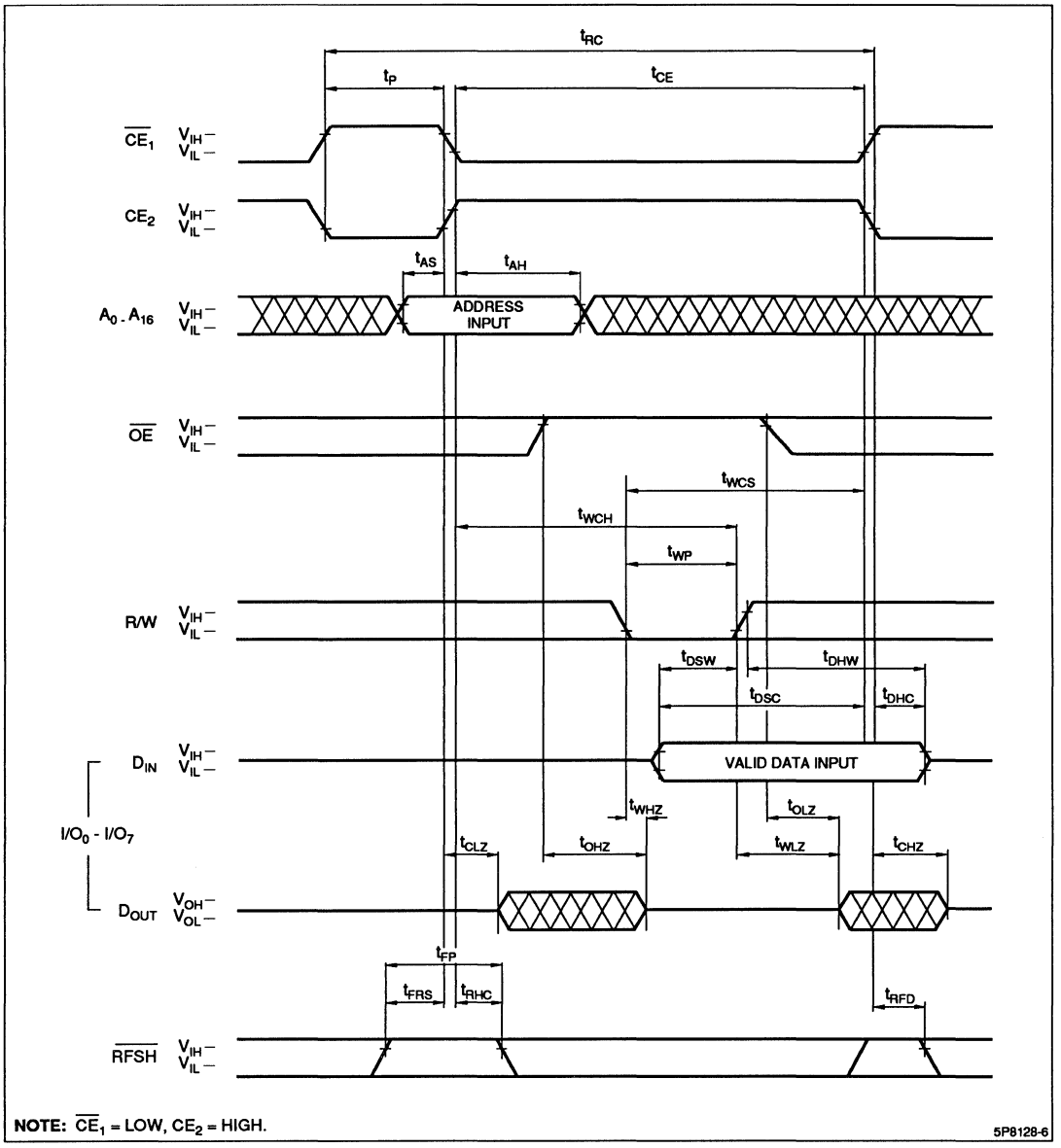


Figure 6. Write Cycle 2 ($\overline{OE}$ Clock)

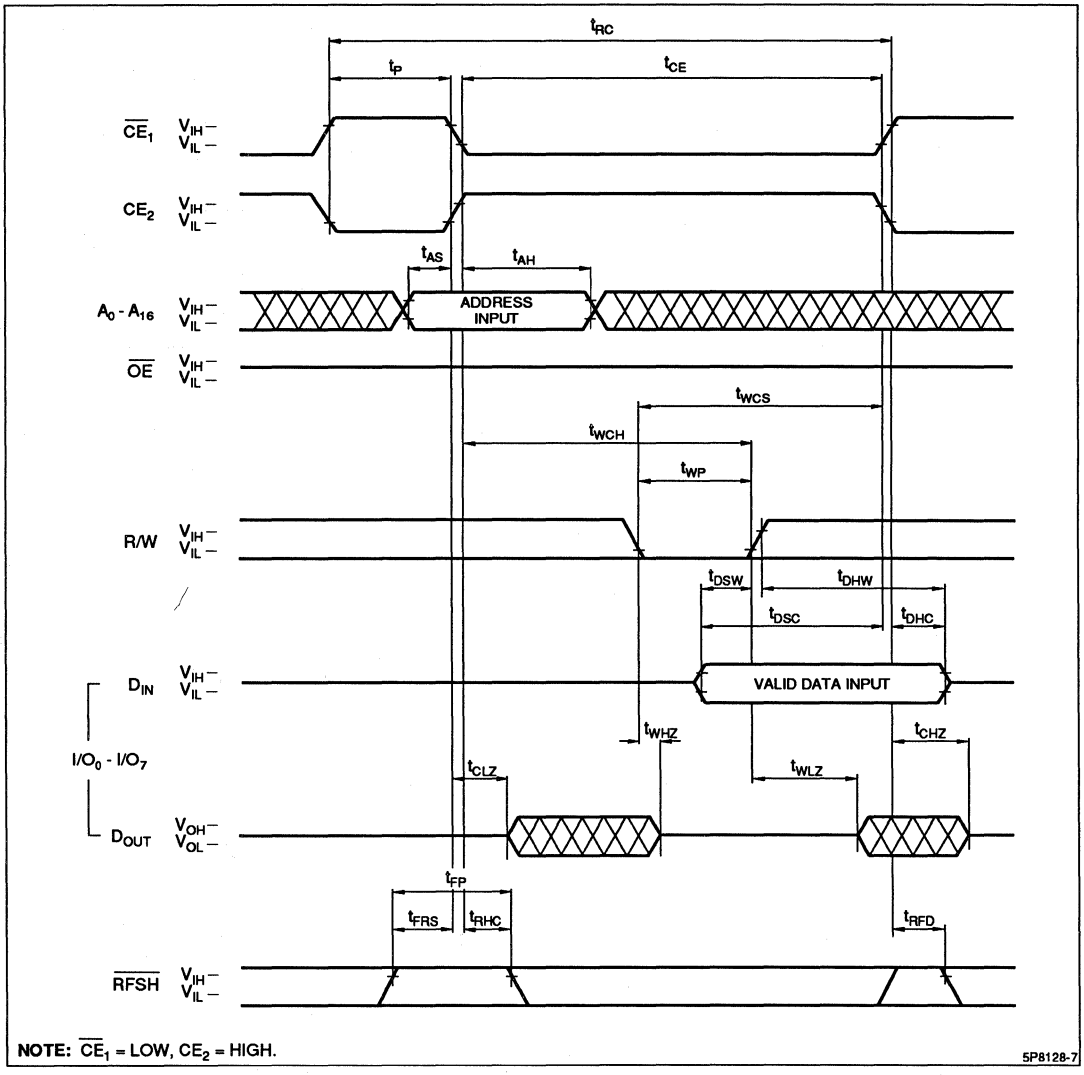


Figure 7. Write Cycle 3 ($\overline{OE}$ = LOW)

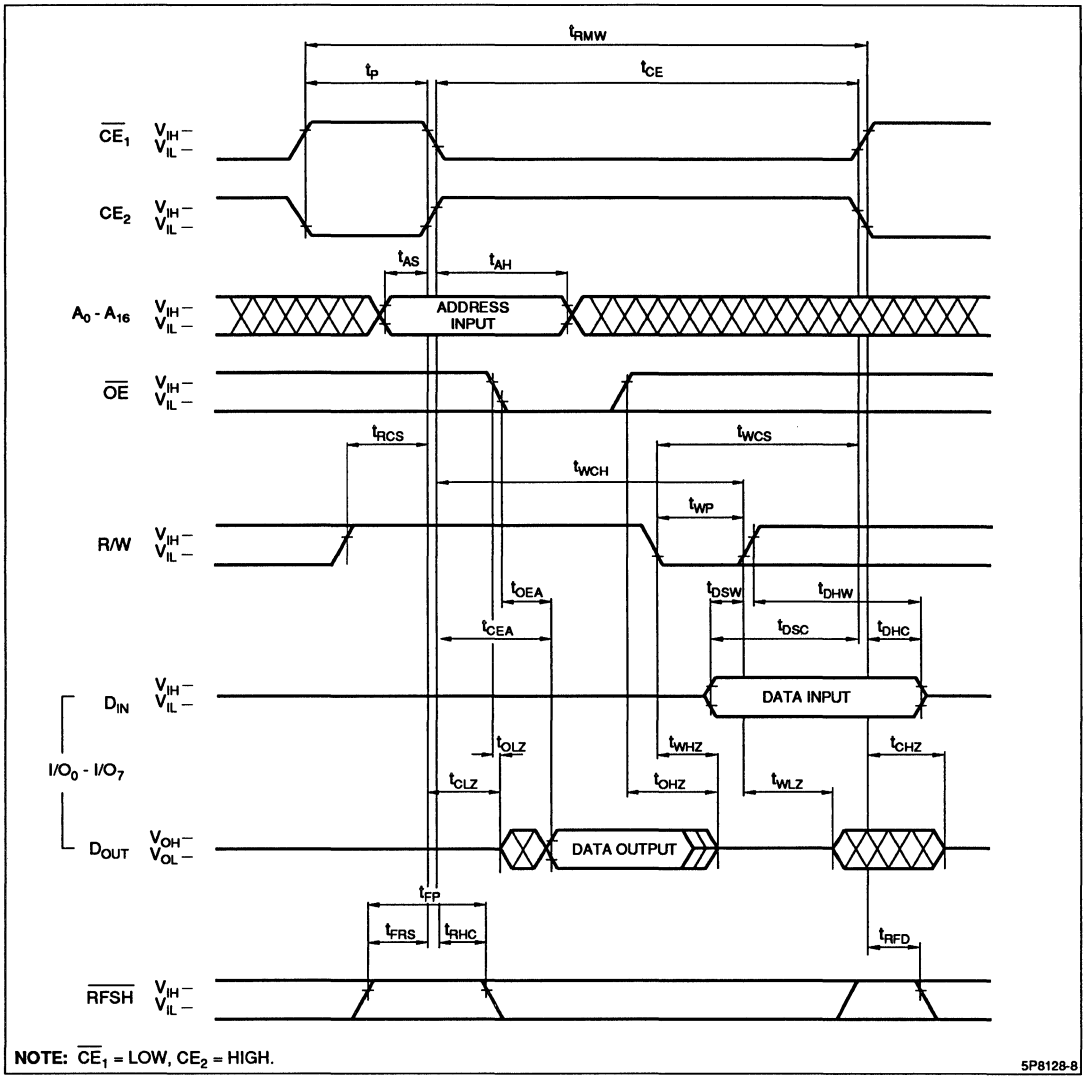


Figure 8. Read-Modify-Write Cycle

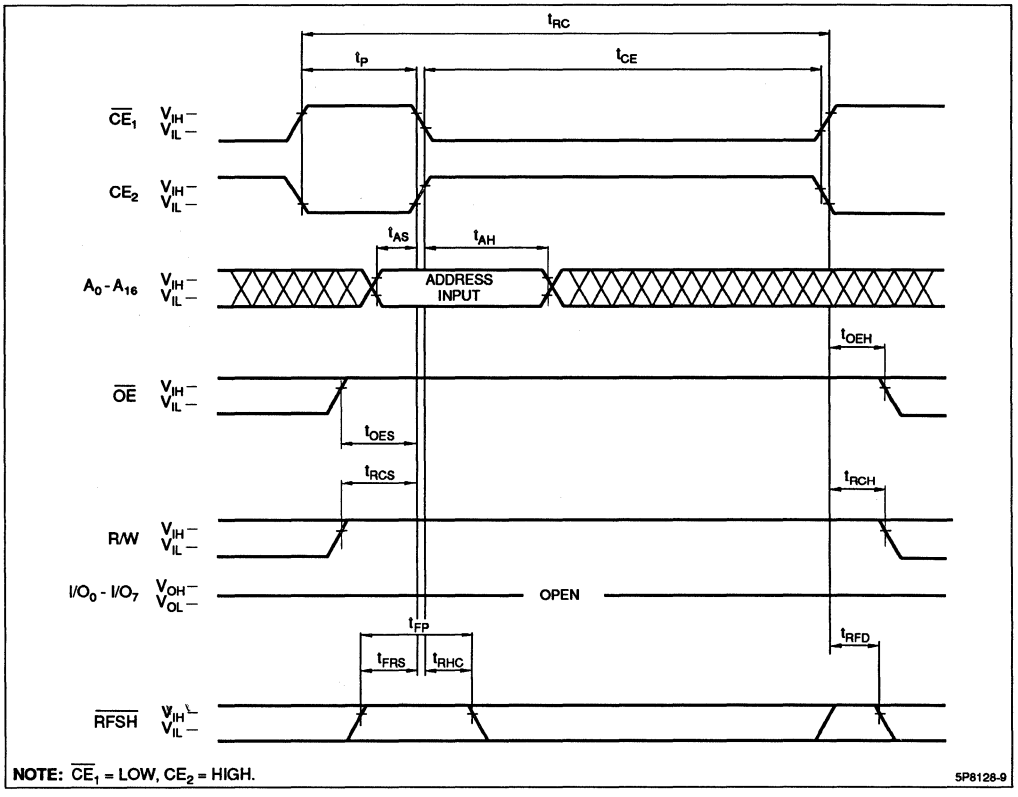


Figure 9. $\overline{CE}$ Only Refresh

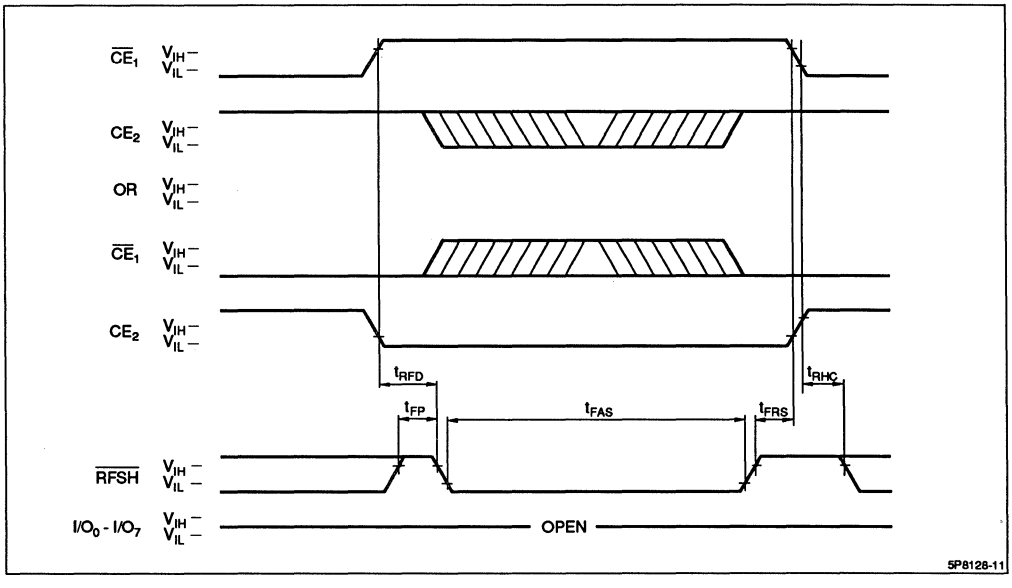


Figure 10. Auto Refresh Cycle

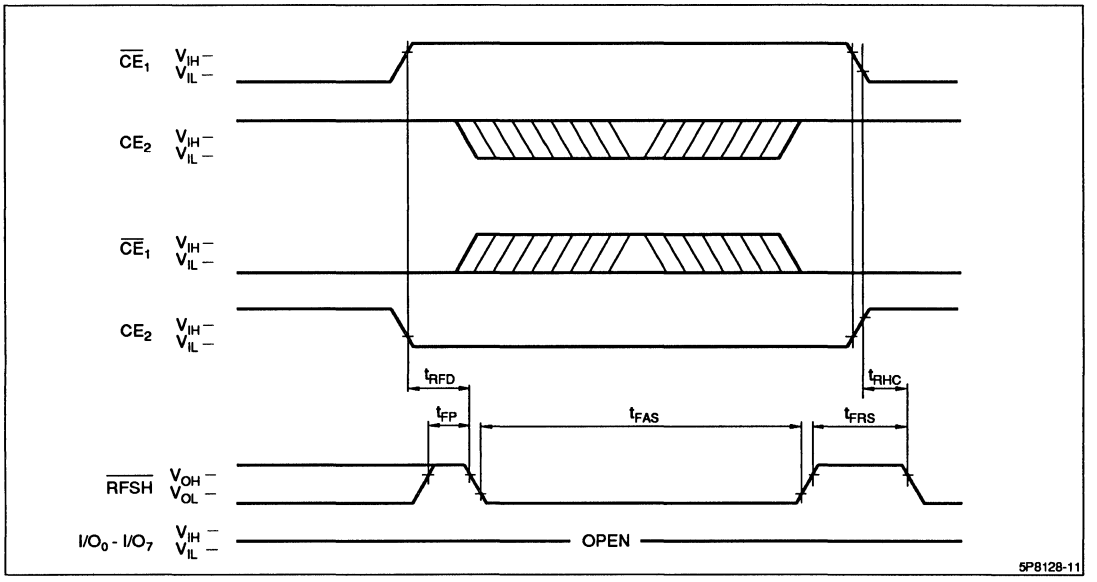
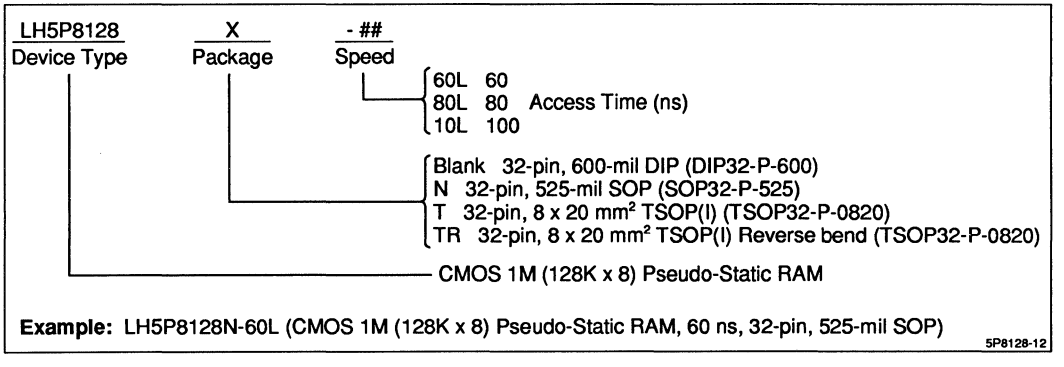


Figure 11. Self Refresh Cycle

ORDERING INFORMATION



LH5116

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5116H: -40 to +85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil, SOP
- Compatible with 16K EPROM and mask ROM pinout

DESCRIPTION

The LH5116 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It features high speed access in read mode using output enable (t_{OE}).

PIN CONNECTIONS

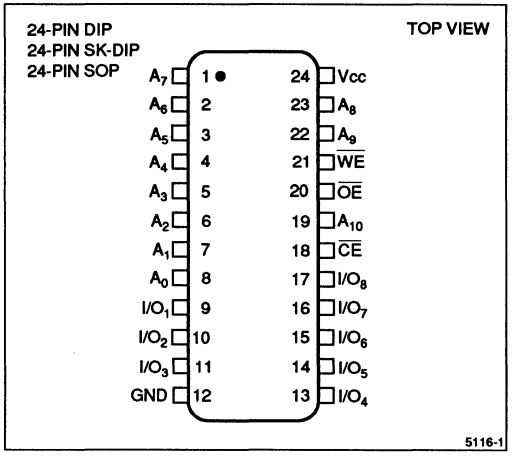


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

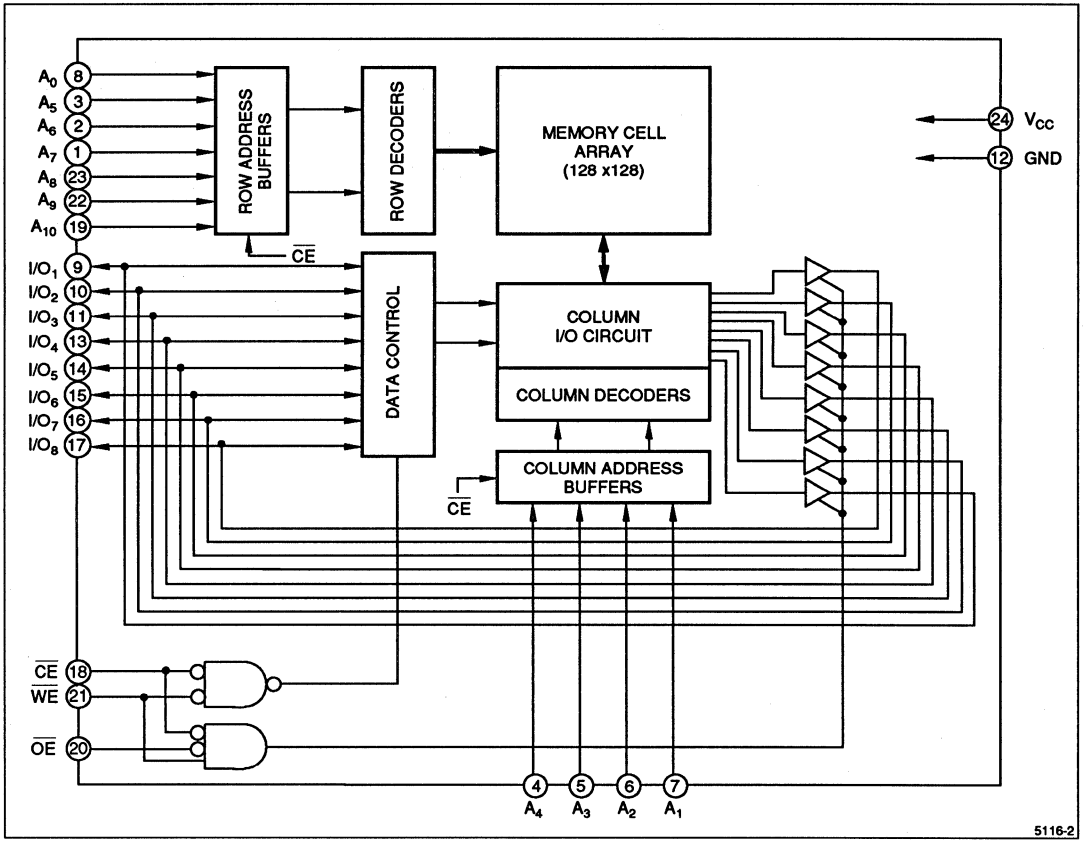


Figure 2. LH5116 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	X	Outputs disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5116/D/NA
3. Applied to the LH5116H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		30	40	mA	3
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	
					0.2		4

NOTES:
1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
$\overline{CE}$ Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			40	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output disable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
Output active from end of write	t_{OW}	10			ns	2
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output enable to output in High-Z	t_{OHZ}			40	ns	2
Output active from end of write	t_{OW}	10			ns	2

NOTE:
1. T_A = 0 to +70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCRC}$ - 0.2V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2V, V_{CCDR} = 3.0 V			1.0	µA	
					0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:
1. T_A = 0 to +70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

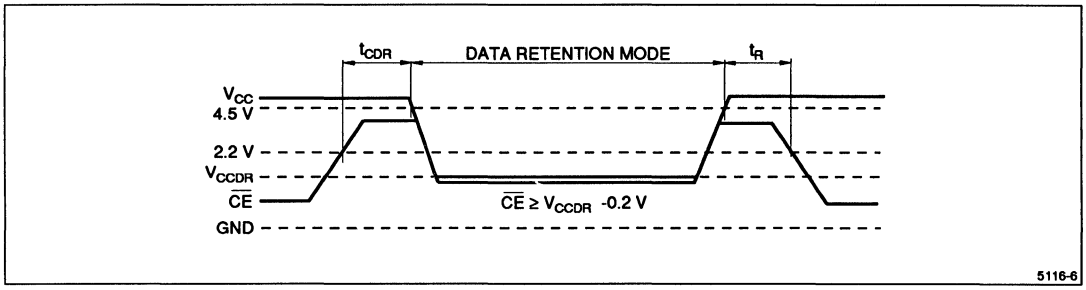


Figure 3. Low Voltage Data Retention

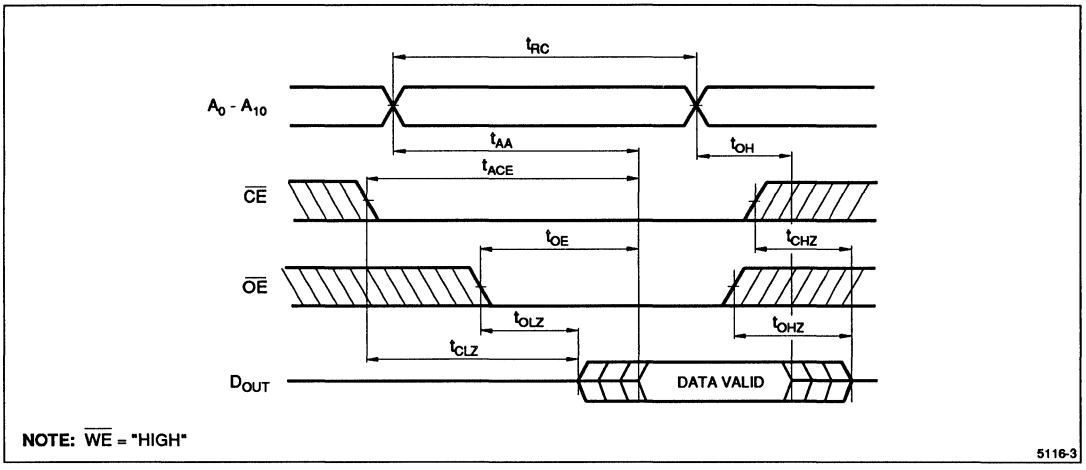
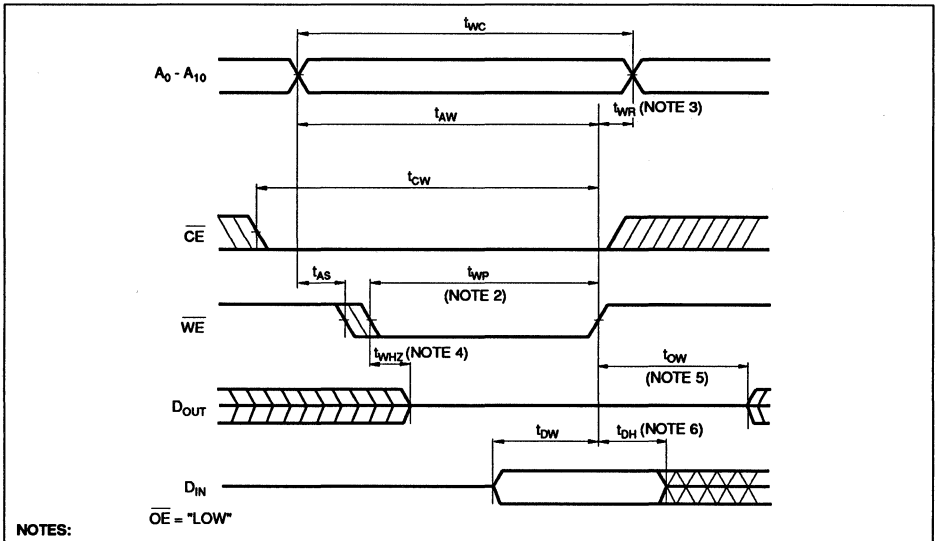


Figure 4. Read Cycle

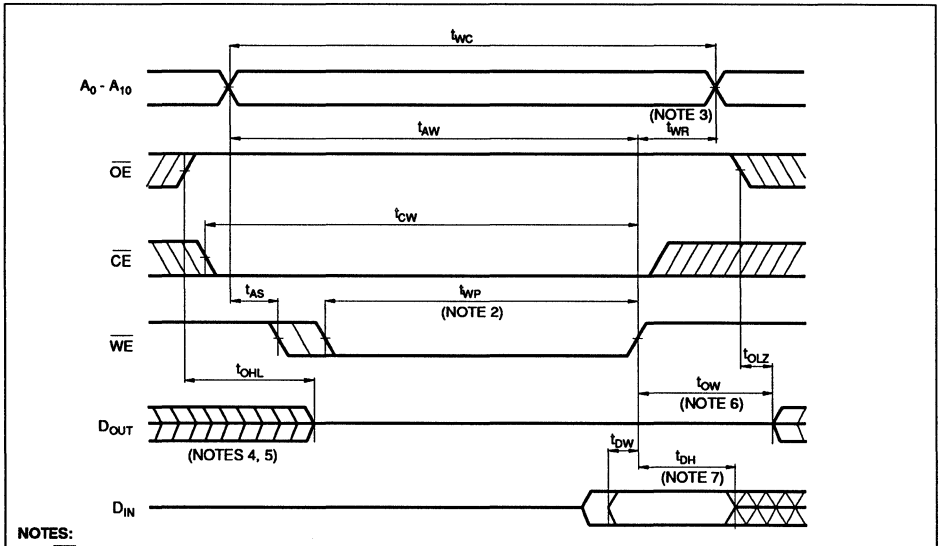


NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

5116-4

Figure 5. Write Cycle 1



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

5116-5

Figure 6. Write Cycle 2 (Note 1)

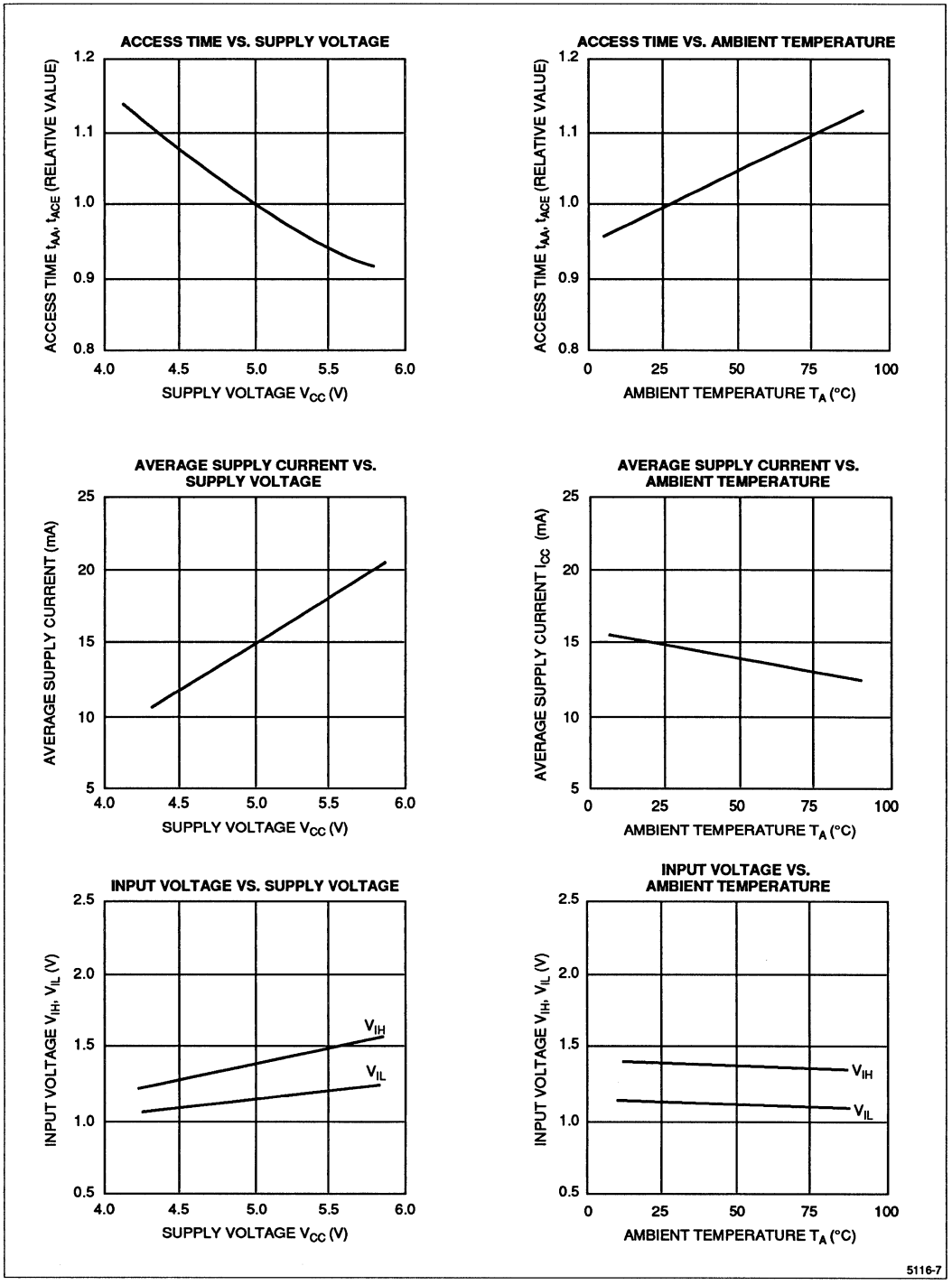
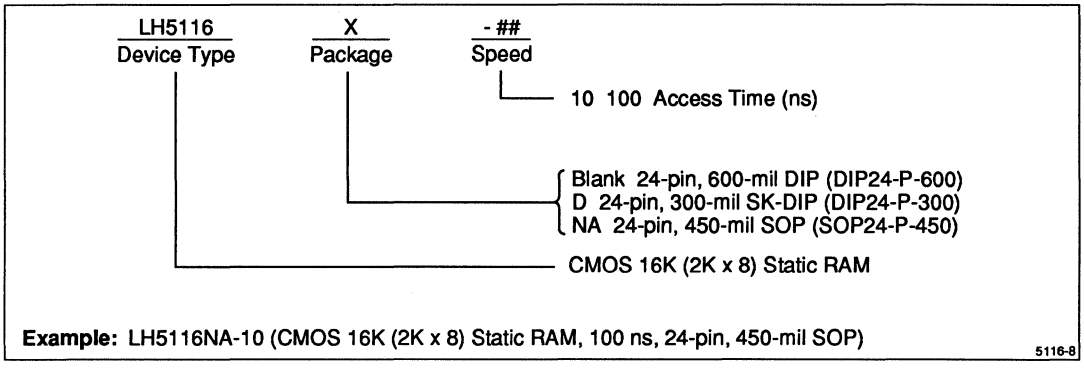


Figure 7. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C unless otherwise specified)

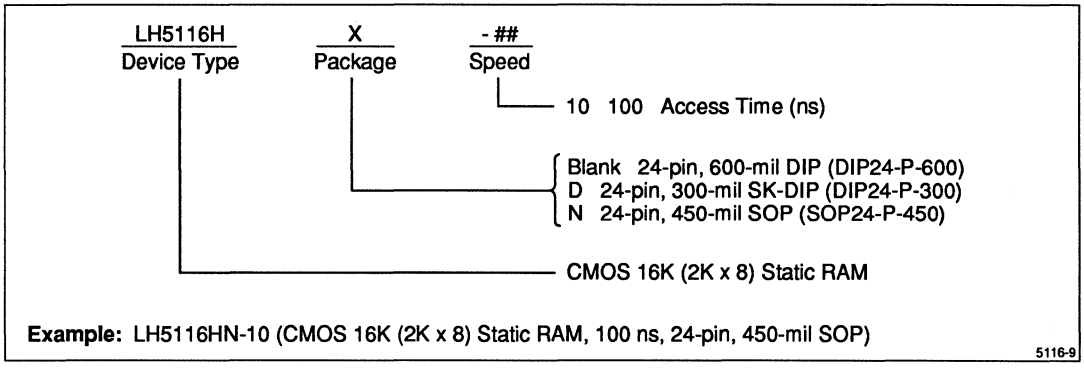
ORDERING INFORMATION (T_A = 0°C to 70°C)



Example: LH5116NA-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5116-8

ORDERING INFORMATION (T_A = -40°C to +85°C)



Example: LH5116HN-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5116-9

LH5116S

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  1000 ns (MAX.)
- Low power consumption:
  Operating: 33 mW (MAX.)
  Standby: 3.3 µW (MAX.)
- Fully static operation
- Three-state outputs
- Single +3 V power supply
- Package:
  24-pin, 450-mil SOP

DESCRIPTION

The LH5116S is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It operates at a low supply voltage of 3 V ± 10%.

PIN CONNECTIONS

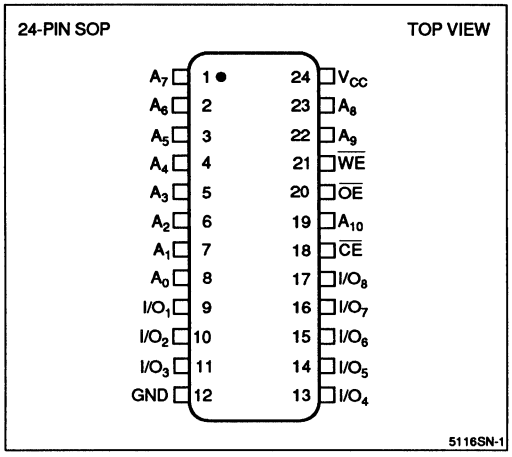


Figure 1. Pin Connections for SOP Package

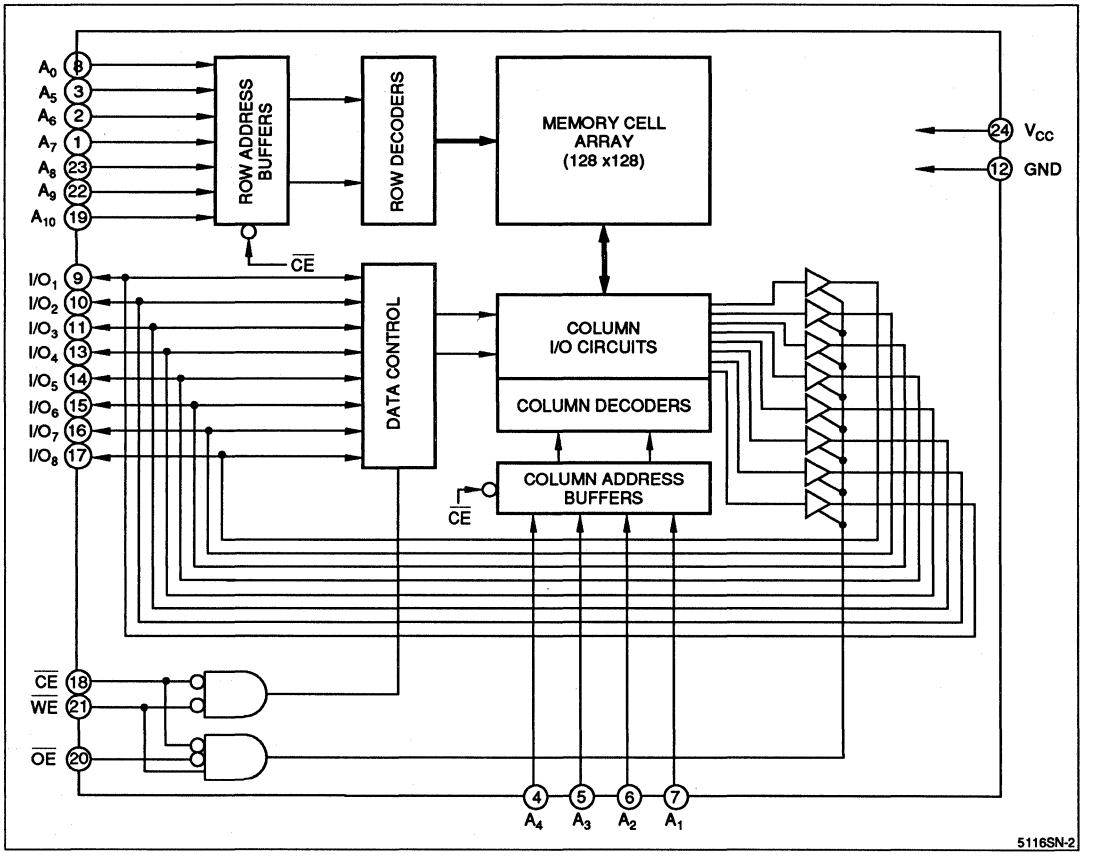


Figure 2. LH5116S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselected	High-Z	Standby (I_{SB})	1
L	H	X	Output disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +50	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 3 V ± 10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.5	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	V_{CC} - 0.5			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		8	10	mA	1
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		8	10	mA	2
Standby current	I_{CCL}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	

NOTES:
1. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
2. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}

AC CHARACTERISTICS (V_{CC} = 3 V ± 10%, T_A = 0 to +50°C)

(1) READ CYCLE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	1000			ns	
Address access time	t_{AA}			1000	ns	
Chip enable access time	t_{ACE}			1000	ns	
$\overline{CE}$ Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			100	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output enable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE (V_{CC} = 3 V ± 10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	1000			ns	
Chip enable to end of write	t_{CW}	100			ns	
Address valid time	t_{AW}	100			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	100			ns	
Write recovery time	t_{WR}	20			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	1
Data valid to end of write	t_{DW}	50			ns	
Data hold time	t_{DH}	20			ns	
Output active from end of write	t_{OW}	10			ns	1
Output enable to output in High-Z	t_{OHZ}			40	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 2.0 V			1.0	µA	
					0.2		1
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:
1. T_A = 25°C
2. t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

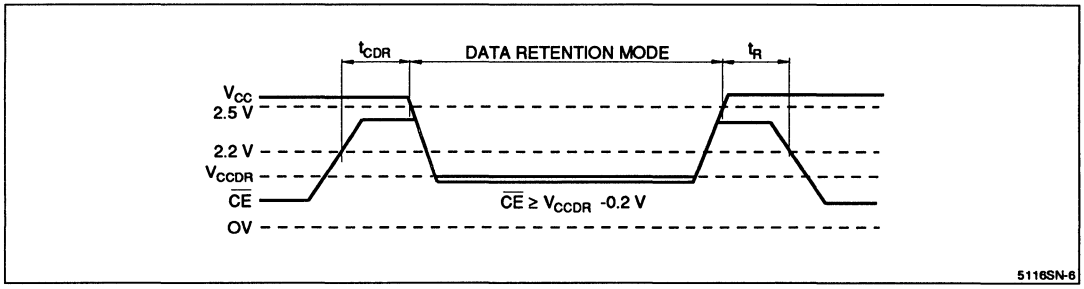


Figure 3. Low Voltage Data Retention

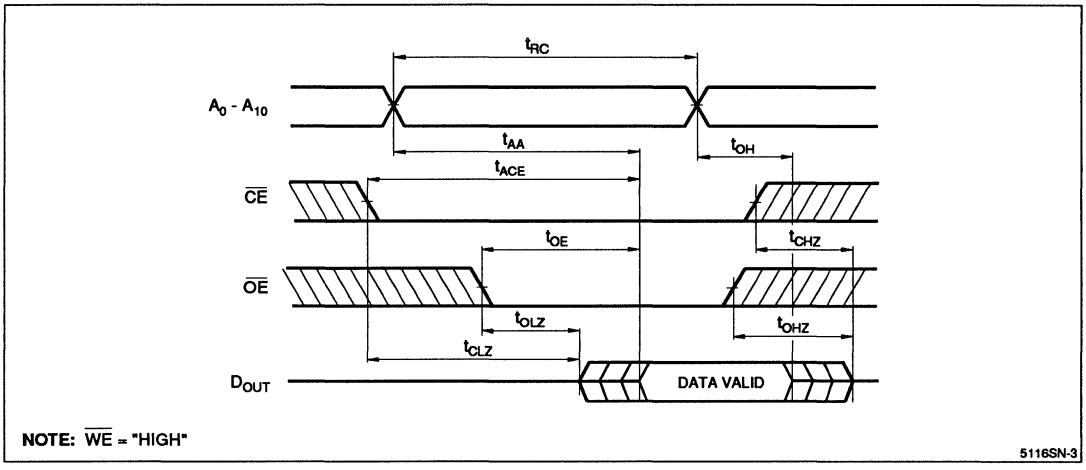
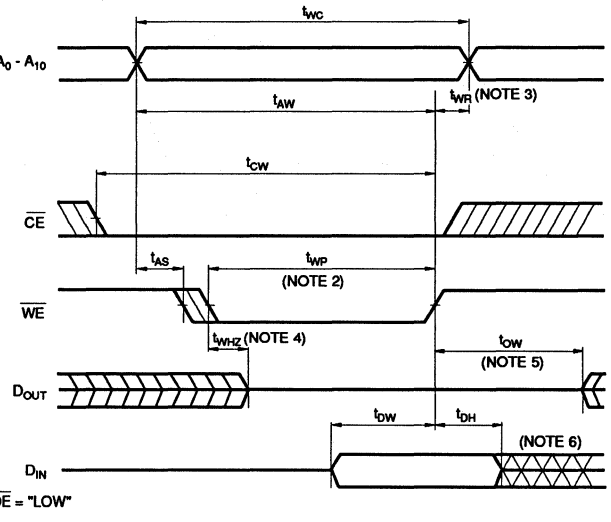


Figure 4. Read Cycle

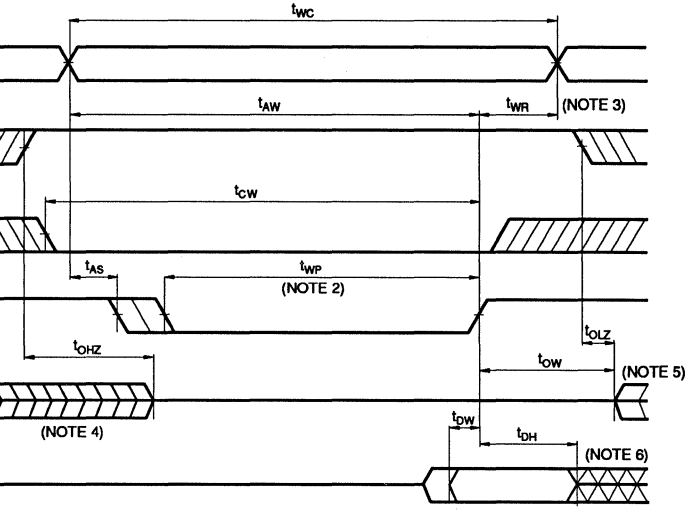


NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the output will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

5116SN-4

Figure 5. Write Cycle 1



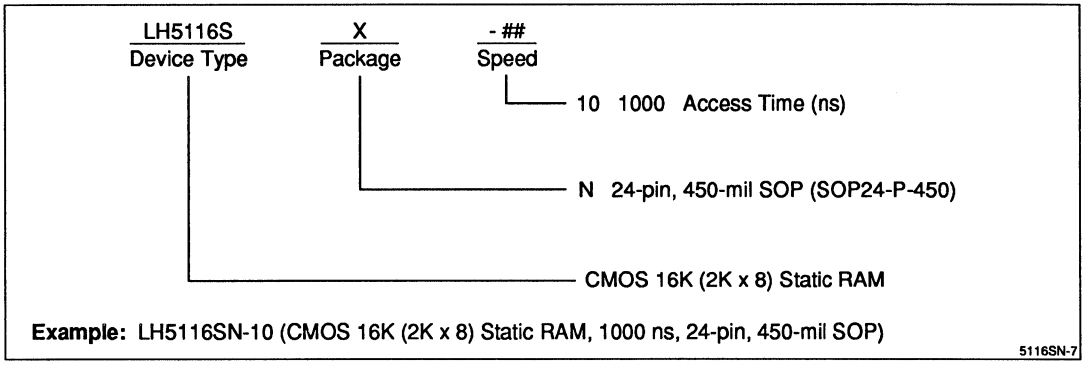
NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the output will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ and $\overline{OE}$ are LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

5116SN-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



LH5117

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 μW (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5117H: -40 to +85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil SOP

DESCRIPTION

The LH5117 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The chip select input provides high speed access in read mode.

PIN CONNECTIONS

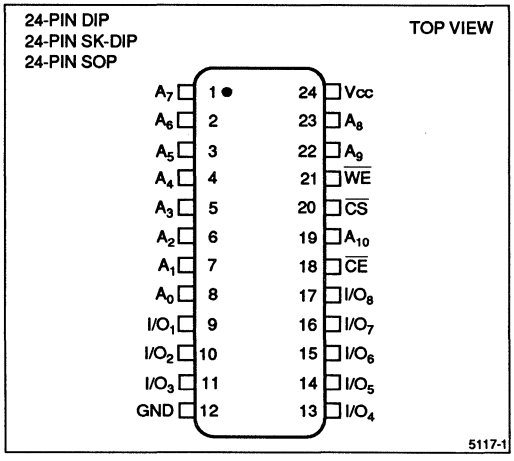


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

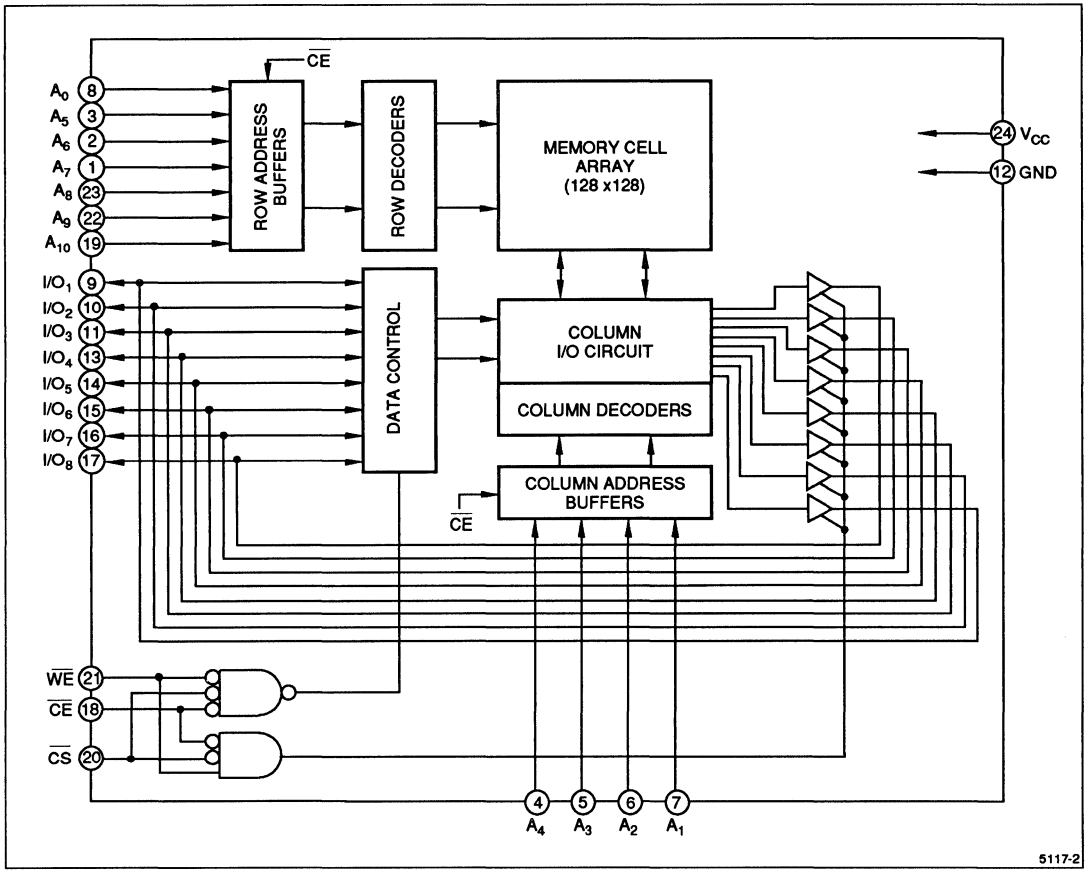


Figure 2. LH5117 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{CS}$	Chip Select input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{CS}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	L	L	Write	D_{IN}	Operating (I_{CC})	
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
L	H	X	Deselect	High-Z	Operating (I_{CC})	1
H	X	X	Deselect	High-Z	Standby (I_{SB})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5117/D/N
3. Applied to the LH5117H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to 70°C (LH5117/D/NA), T_A = -40 to +85°C (LH5117H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, $\overline{CS}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}			25	30	mA	2
	I_{CC2}			30	40	mA	3
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V, $\overline{CS}$ ≥ V_{CC} - 0.2 V or $\overline{CS}$ ≤ 0.2 V, All other input pins = 0 V to V_{CC}			1.0	µA	
					0.2		4

NOTES:
1. T_A = 0 to 70°C (LH5117/D/N), T_A = -40 to +85°C (LH5117H/HD/HN)
2. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}, outputs open
3. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}, outputs open
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Chip enable Low to output in Low-Z	t_{CLZ}	10			ns	2
Chip select access time	t_{ACS}			40	ns	
Chip select Low to output in Low-Z	t_{SLZ}	10			ns	2
Chip enable to output in High-Z	t_{CHZ}	0		40	ns	2
Chip select to output in High-Z	t_{SHZ}	0		40	ns	2
Output hold time	t_{OH}	10			ns	

(2) WRITE CYCLE [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
Write enable Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output active from end of write	t_{OW}	10			ns	2

NOTE:
1. T_A = 0 to +70°C (LH5117/D/N), T_A = -40 to +85°C (LH5117H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCRC}$ - 0.2V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2, $\overline{CS} \geq V_{CCDR}$ - 0.2 or $\overline{CS} \leq$ 0.2 V, V_{CCDR} = 3.0 V			1.0	µA	
					0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:
1. T_A = 0 to +70°C (LH5117/D/N), T_A = -40 to +85°C (LH5117H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

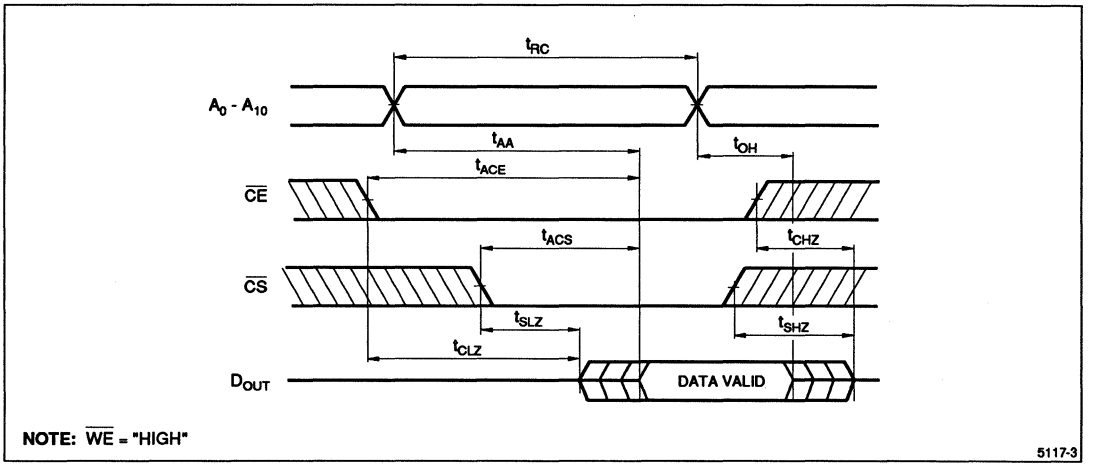


Figure 3. Read Cycle

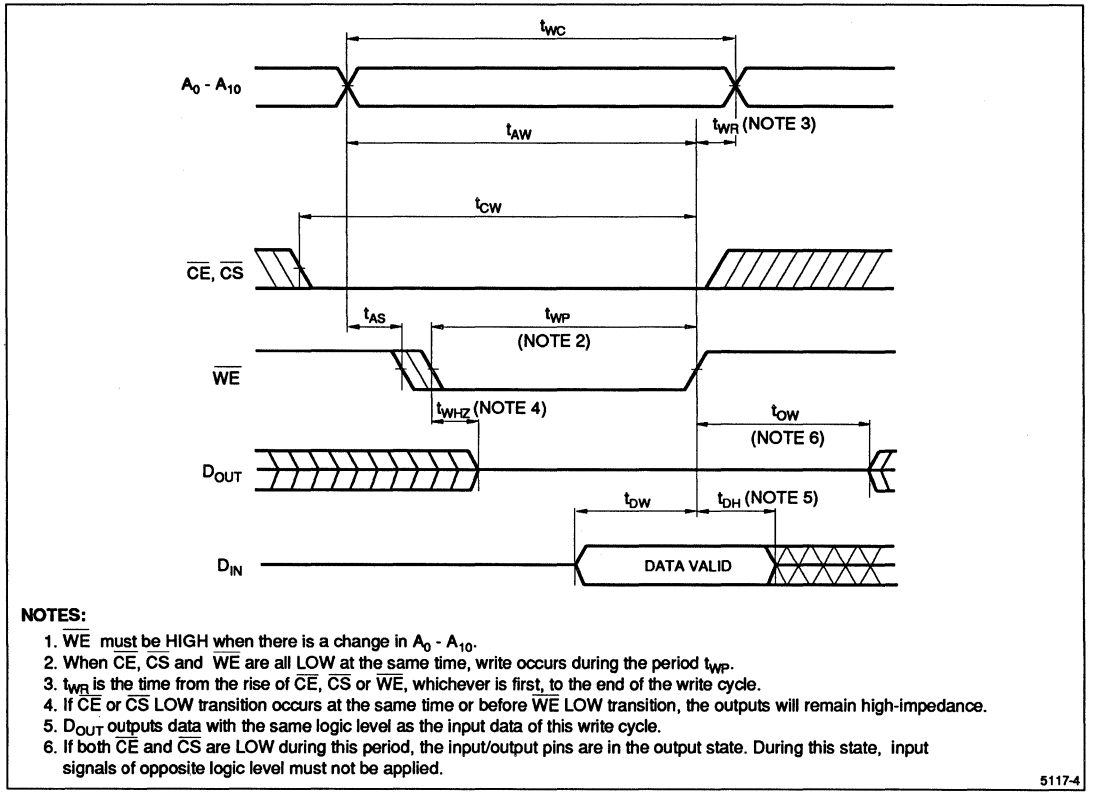


Figure 4. Write Cycle

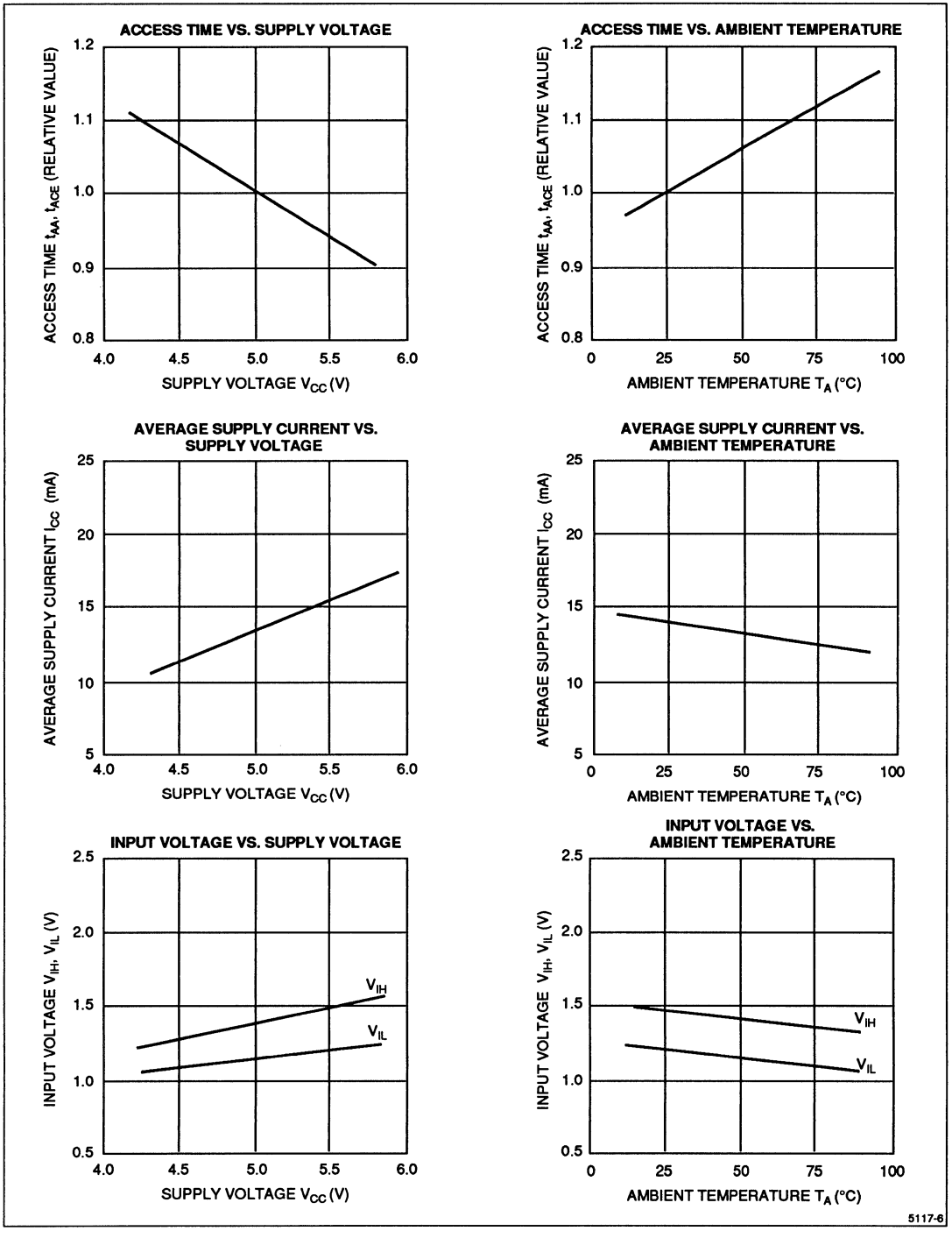


Figure 5. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C Unless Otherwise Specified)

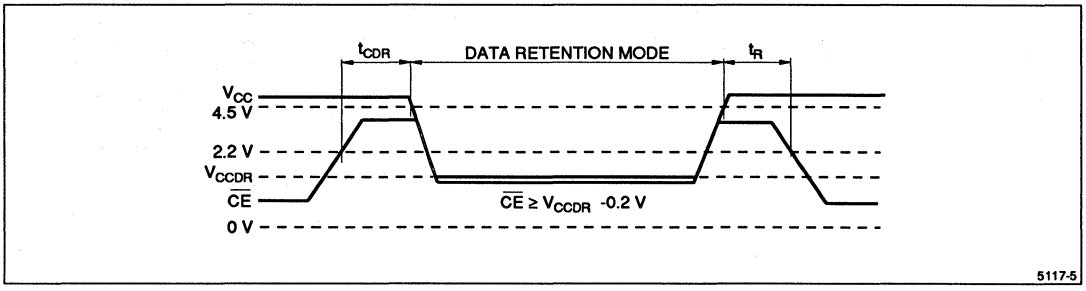
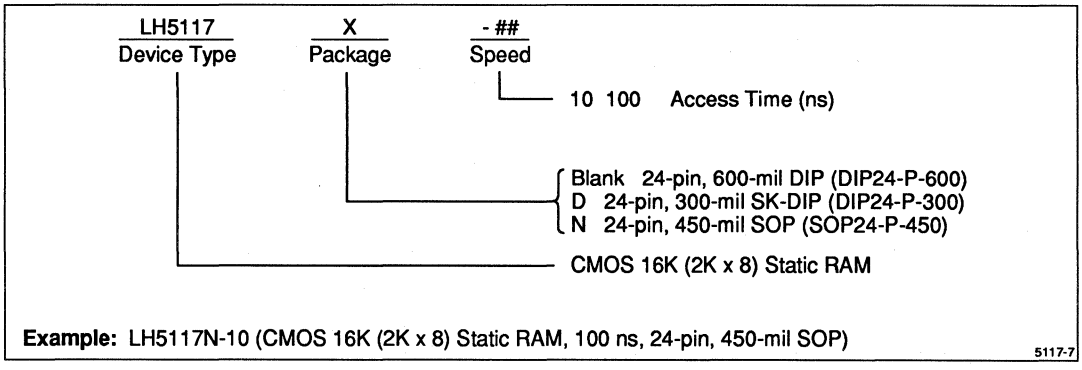
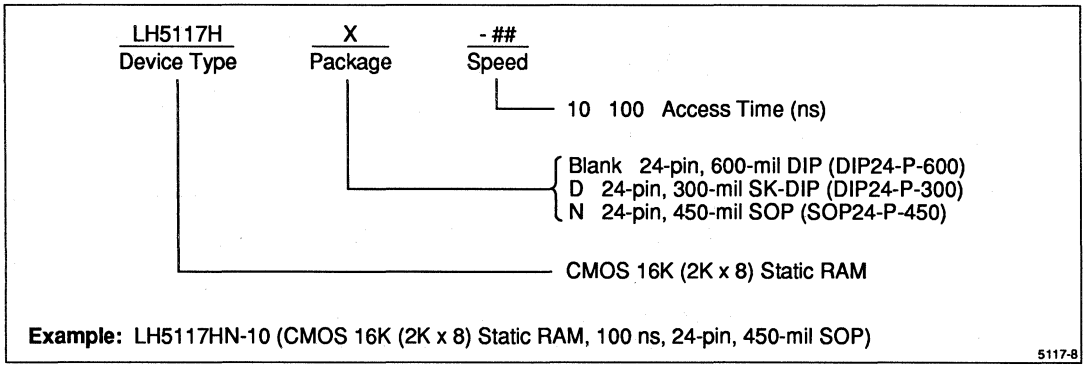


Figure 6. Low Voltage Data Retention

ORDERING INFORMATION (T_A = 0 to +70°C)



ORDERING INFORMATION (T_A = -40 to +85°C)



LH5118

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5118H: -40 to + 85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil SOP

DESCRIPTION

The LH5118 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5118 accepts two chip-enables. These allow data to be held with battery back-up for memory expansion (used in systems with multiple memory devices).

Low power mode (I_{SB}) is available with $\overline{CE}_1$ and $\overline{CE}_2$ deactivated.

PIN CONNECTIONS

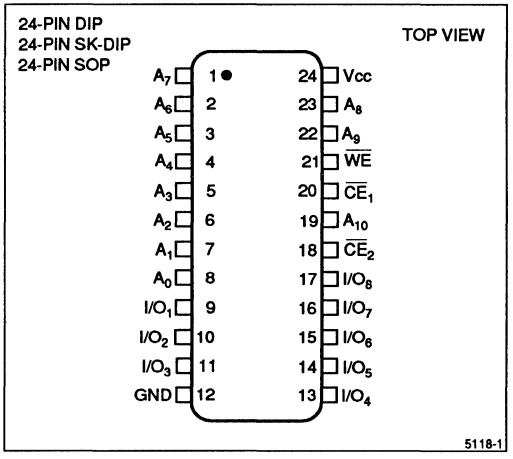


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

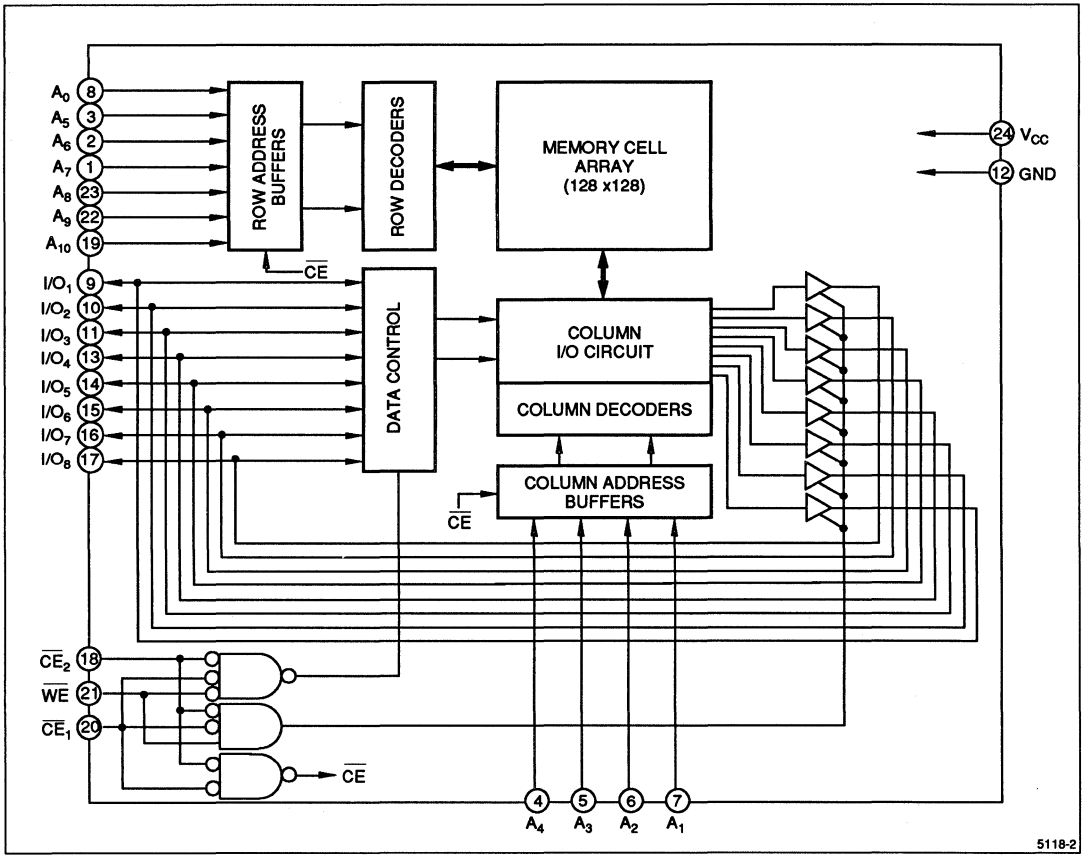


Figure 2. LH5118 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}_2$	Chip Enable input no. 2
$\overline{CE}_1$	Chip Enable input no. 1
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
X	H	X	Deselect	High-Z	Standby (I_{SB})	1
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	L	L	Write	D_{IN}	Operating (I_{CC})	
L	L	H	Read	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5118/D/N
3. Applied to the LH5118H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to +70°C (LH5118/D/NA), T_A = -40 to +85°C (LH5118H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_2}$ = V_{IH} or $\overline{CE_1}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{WE}$ = V_{CC})		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{WE}$ = V_{IH})		30	40	mA	3
Standby current	I_{SB}	(1) $\overline{CE_2} \geq V_{CC}$ - 0.2 V, and ($\overline{CE_1} \geq V_{CC}$ - 0.2 V or $\overline{CE_1} \leq$ 0.2 V) or			1.0	µA	
		(2) $\overline{CE_1} \geq V_{CC}$ - 0.2 V, and ($\overline{CE_2} \geq V_{CC}$ - 0.2 V or $\overline{CE_2} \leq$ 0.2 V) All other inputs = 0 V to V_{CC}			0.2	µA	4

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. $\overline{CE_2}$ = $\overline{CE_1}$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE_2}$ = $\overline{CE_1}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
$\overline{CE}_1$ access time	t_{ACE1}			100	ns	
$\overline{CE}_2$ access time	t_{ACE2}			100	ns	
$\overline{CE}_1$ Low to output in Low-Z	t_{CLZ1}	10			ns	2
$\overline{CE}_2$ Low to output in Low-Z	t_{CLZ2}	10			ns	2
$\overline{CE}_1$ to output in High-Z	t_{CHZ1}	0		40	ns	2
$\overline{CE}_2$ to output in High-Z	t_{CHZ2}	0		40	ns	2
Data hold time	t_{OH}	10			ns	

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output active from end of write	t_{OW}	10			ns	2

NOTE:

1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2V or $\overline{CE_2} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2V, and ($\overline{CE_2} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_2} \leq$ 0.2 V) or			1.0	µA	
		$\overline{CE_2} \geq V_{CCDR}$ - 0.2V, and ($\overline{CE_1} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_1} \leq$ 0.2 V) V_{CCDR} = 3.0 V			0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

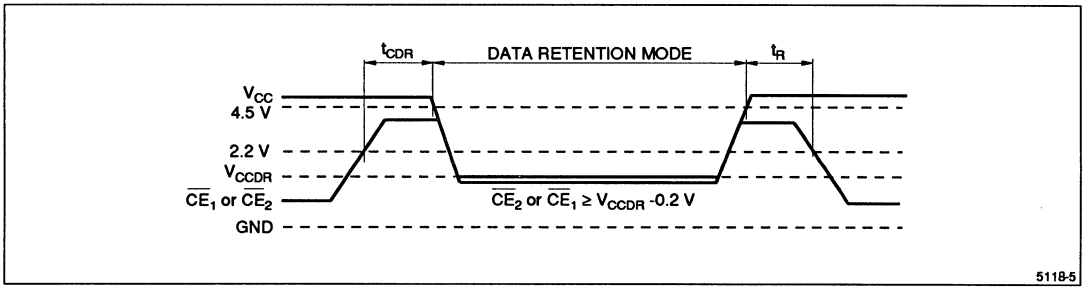
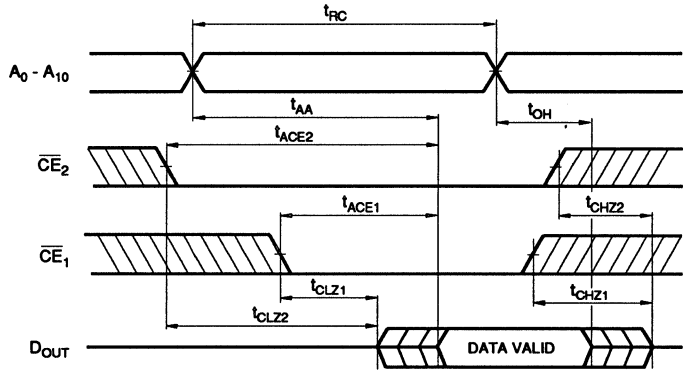


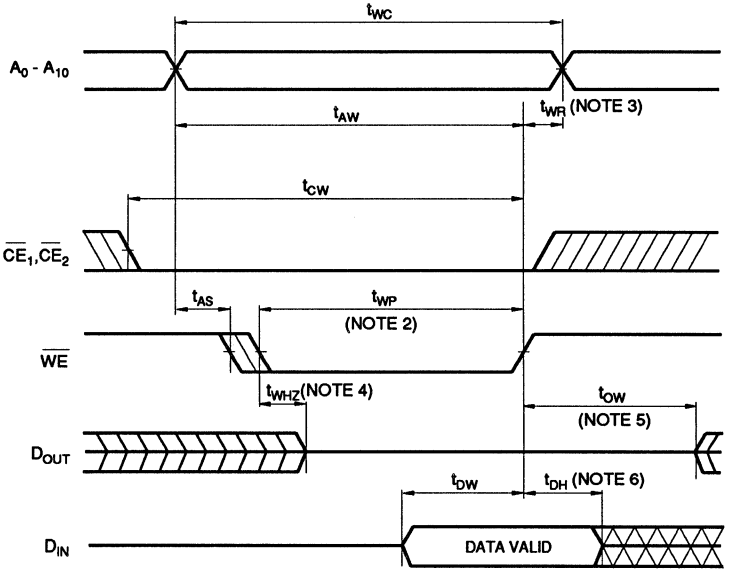
Figure 3. Low Voltage Data Retention



NOTE: $\overline{WE}$ = "HIGH"

5118-3

Figure 4. Read Cycle



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}_2$,$\overline{CE}_1$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}_2$,$\overline{CE}_1$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}_2$ or $\overline{CE}_1$ should drop at the same time as $\overline{WE}$ or later, the output buffer is maintained at high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If both $\overline{CE}_1$ and $\overline{CE}_2$ are LOW during this period, the input/output pin is in the output condition. During this condition, a data input signal with a logic level opposite that of the output is not permitted.

5118-4

Figure 5. Write Cycle (Note 1)

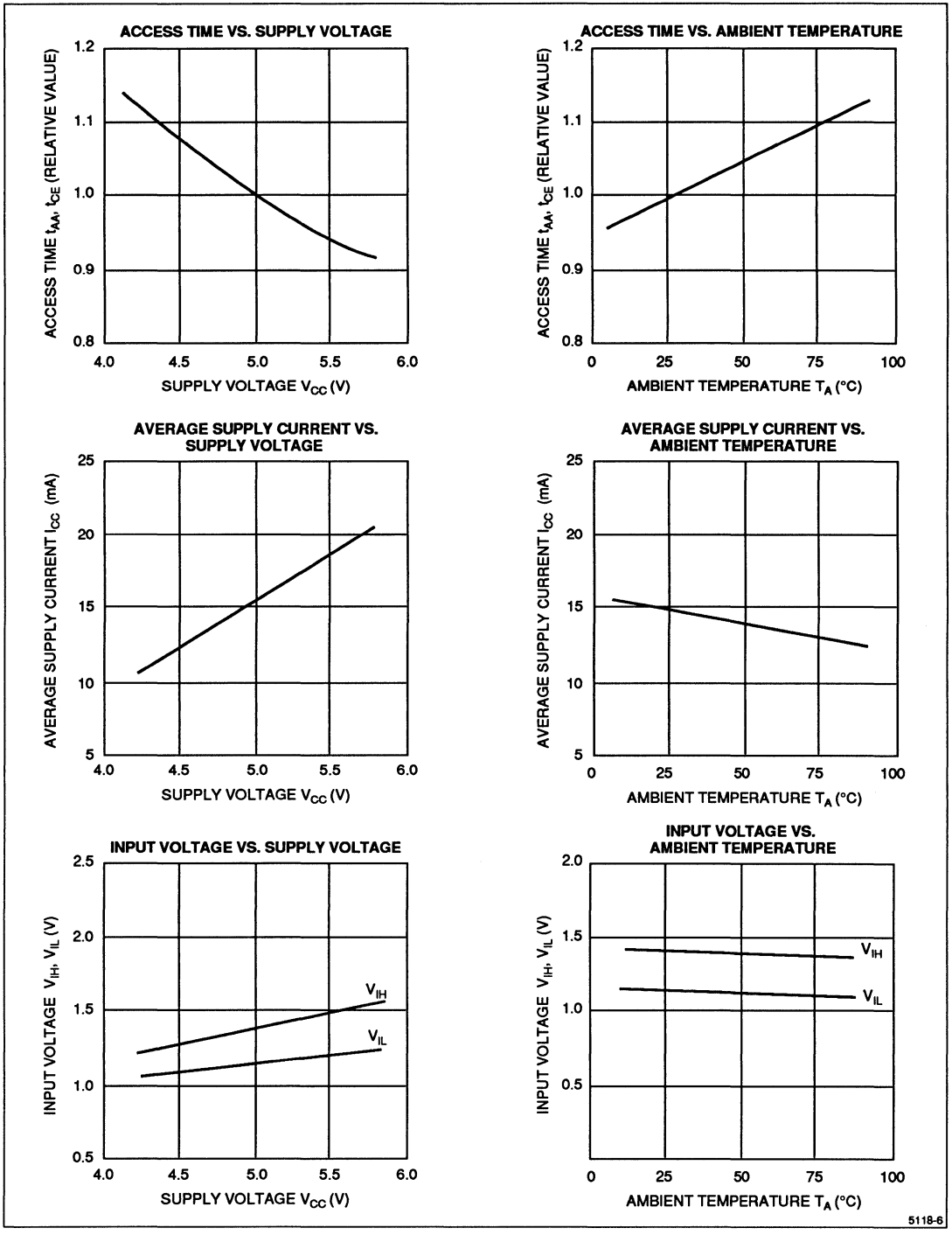
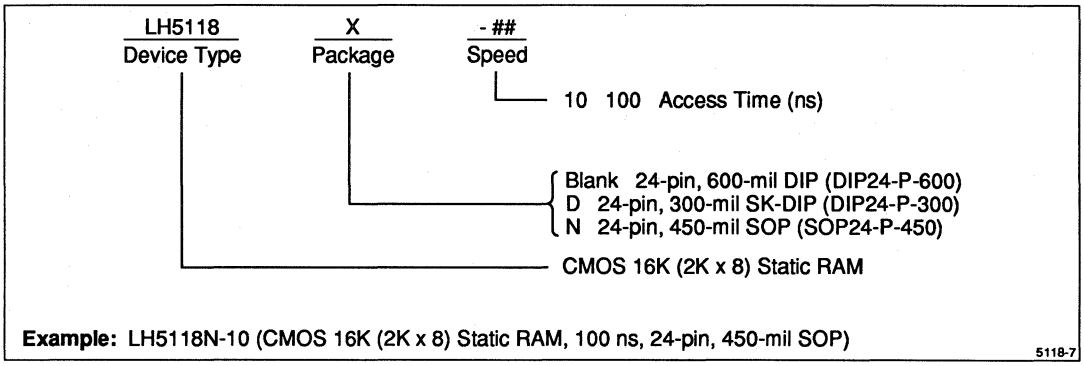


Figure 6. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C Unless Otherwise Specified)

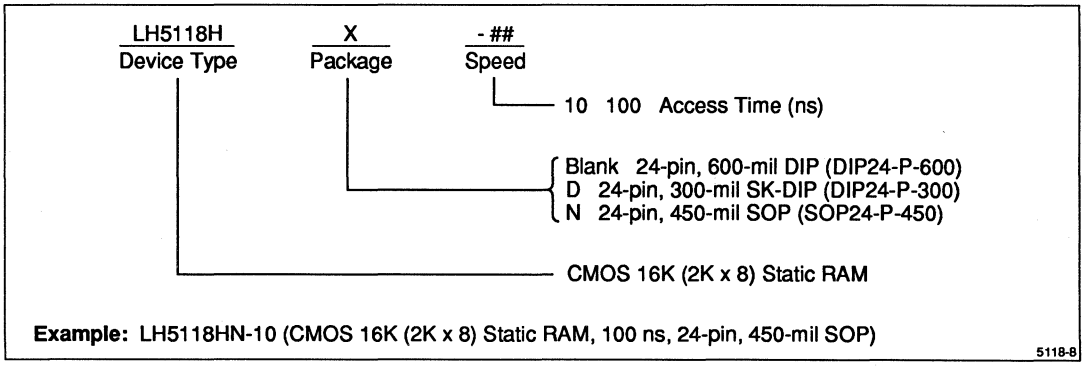
ORDERING INFORMATION (T_A = 0 to +70°C)



Example: LH5118N-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5118-7

ORDERING INFORMATION (T_A = -40 to +85°C)



Example: LH5118HN-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5118-8

LH5168

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- High speed access time:
  100 ns (MAX.)
- Low power consumption:
  Operating:
  248 mW (MAX.) LH5168/D/N
  275 mW (MAX.) LH5168H/HD/HN
  Standby:
  5.5 µW (MAX.) LH5168/D/N
  16.5 µW (MAX.) LH5168H/HD/HN
- Fully static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Pin compatible to 64K bit EPROM
- Wide temp. range available
  LH5168H: -40 to +85°C
- Packages:
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH5168 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5168H is designed for wide temperature range from -40 to +85°C.

PIN CONNECTIONS

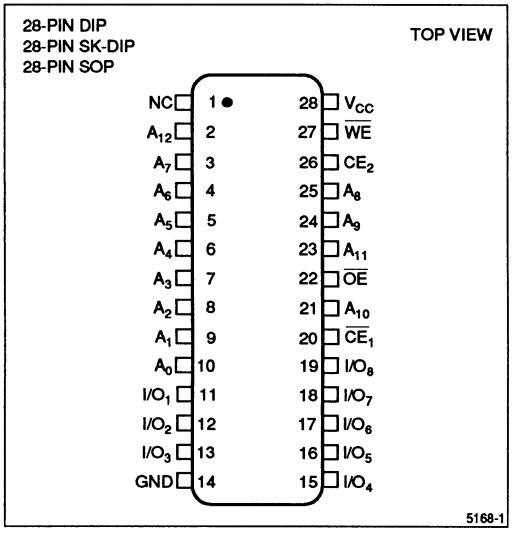


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

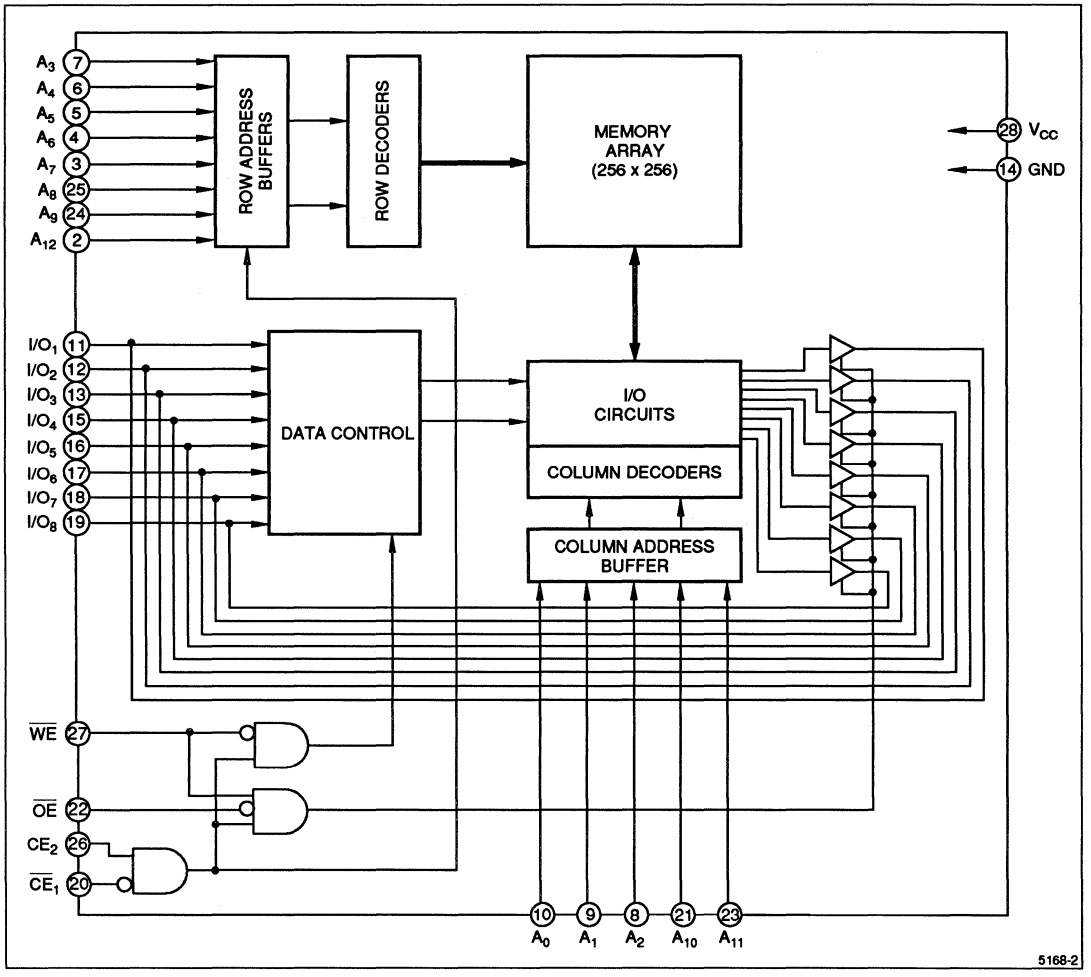


Figure 2. LH5168 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non-connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-10 to +70	°C	2
		-40 to +85	°C	3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. LH5168/D/N
3. LH5168H/HD/HN

RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN).

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			1.0	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}			1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 100 ns		45	mA	2
					50		3
		$\overline{CE_1}$ = V_{IL}, V_{IN} = 0.2 V to V_{CC} - 0.2 V CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 1.0 µs		10		
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			10	mA	
	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$, CE_2 ≥ V_{CC} - 0.2 V	T_A ≤ 70°C		1.0	µA	2
			T_A ≤ 85°C		3.0	µA	3
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
	V_{OH}	I_{OH} = -1 mA		2.4		V	

NOTES:
1. T_A = -10 to 70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N
3. LH5168H/HD/HN

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle		t_{RC}	100		ns	
Address access time		t_{AA}		100	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		100	ns	
	(CE_2)	t_{ACE2}		100	ns	
Output enable access time		t_{OE}		40	ns	
Output hold time		t_{OH}	10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	10		ns	2
	(CE_2)	t_{LZ2}	10		ns	2
Output enable to input in Low-Z		t_{OLZ}	5		ns	2
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	30	ns	2
	(CE_2)	t_{HZ2}	0	30	ns	2
Output disable to output in High-Z		t_{OHZ}	0	20	ns	2

NOTE:

1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100		ns	
Chip enable to end of write	t_{CW}	80		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	60		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	40		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	10		ns	1
$\overline{WE}$ to output in High-Z	t_{WZ}	0	30	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	20	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	(1TTL + C_L = 100 pF)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

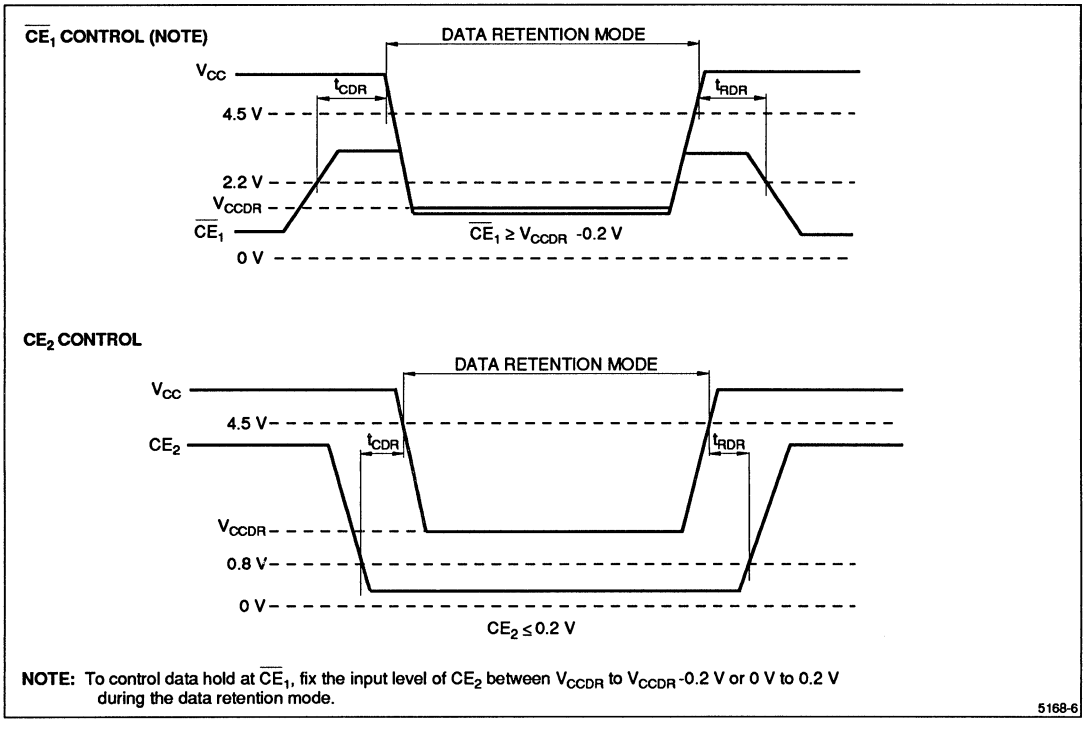
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE}_1$, $CE_2 \ge V_{CC}$ - 0.2 V	2.0		V	
Data retention current	I_{CCDR}	V_{CCDR} = 3 V, $CE_2 \le 0.2$ V or $\overline{CE}_1$, $CE_2 \ge V_{CCDR}$ - 0.2 V		0.6	µA	2
				1.5	µA	3
Chip disable to data retention	t_{CDR}		0		ns	
Recovery time	t_{RDR}		t_{RC}		ns	4

NOTES:
1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N at $T_A \le 70$°C
3. LH5168H/HD/HN at $T_A \le 85$°C
4. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE}_1$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention mode.

5168-6

Figure 3. Low Voltage Data Retention

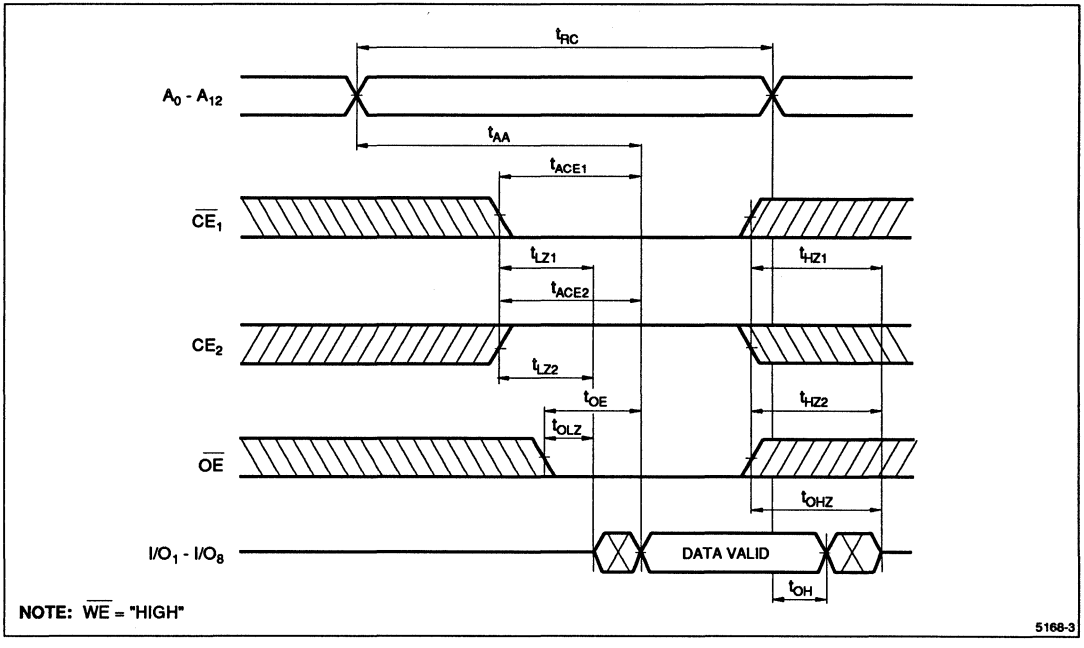
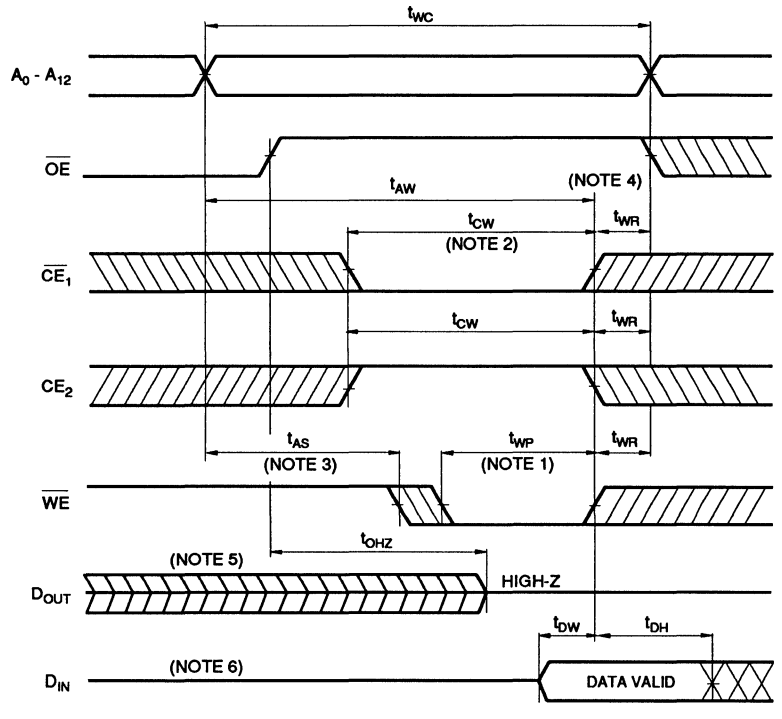


Figure 4. Read Cycle

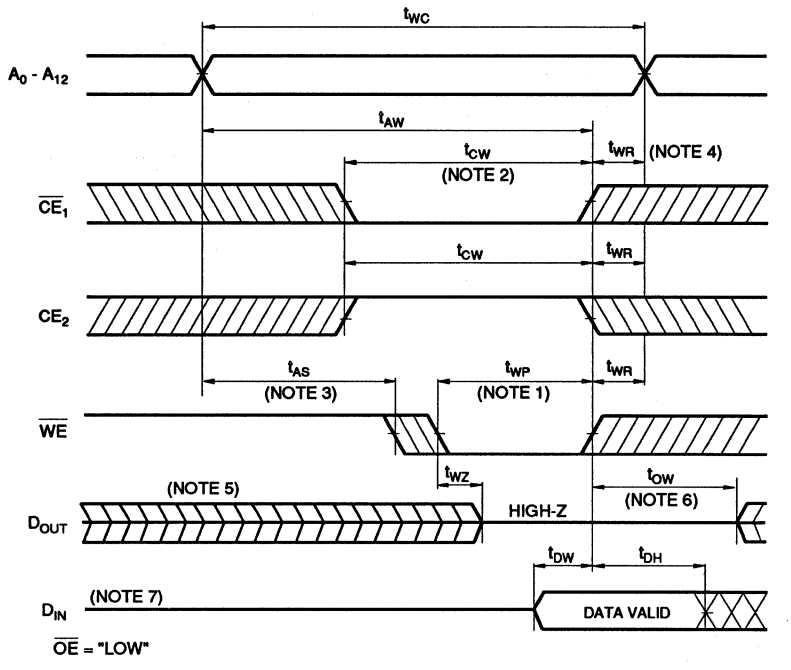


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-4

Figure 5. Write Cycle 1



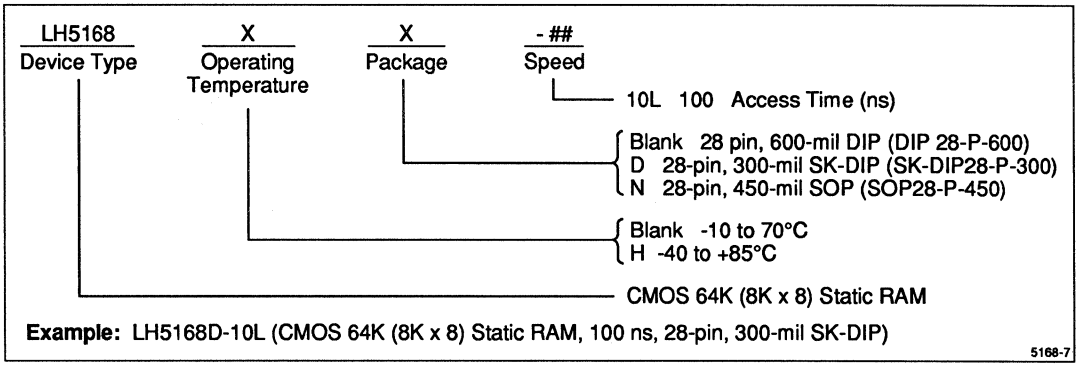
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH5168D-10L (CMOS 64K (8K x 8) Static RAM, 100 ns, 28-pin, 300-mil SK-DIP)

5168-7

LH5168SH

PRELIMINARY

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- Access time:
  500 ns (MAX.)
- Low current consumption:
  Operating: 50 mA (MAX.)
  Standby: 3 µA (MAX.)
- Fully static operation
- Three-state outputs
- Single 2.5 to 5.5 V power supply
- TTL compatible I/O
- Wide temp. range
  t_{OPR}: -40 to +85°C
- Package:
  28-pin, 450-mil SOP

DESCRIPTION

The LH5168SH is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

It is designed for 2.5 to 5.5 V low voltage operation and wide temperature range from -40 to +85°C.

PIN CONNECTIONS

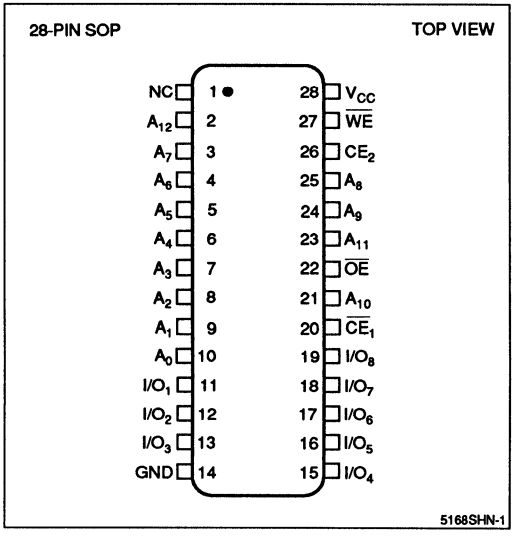


Figure 1. Pin Connections for SOP Package

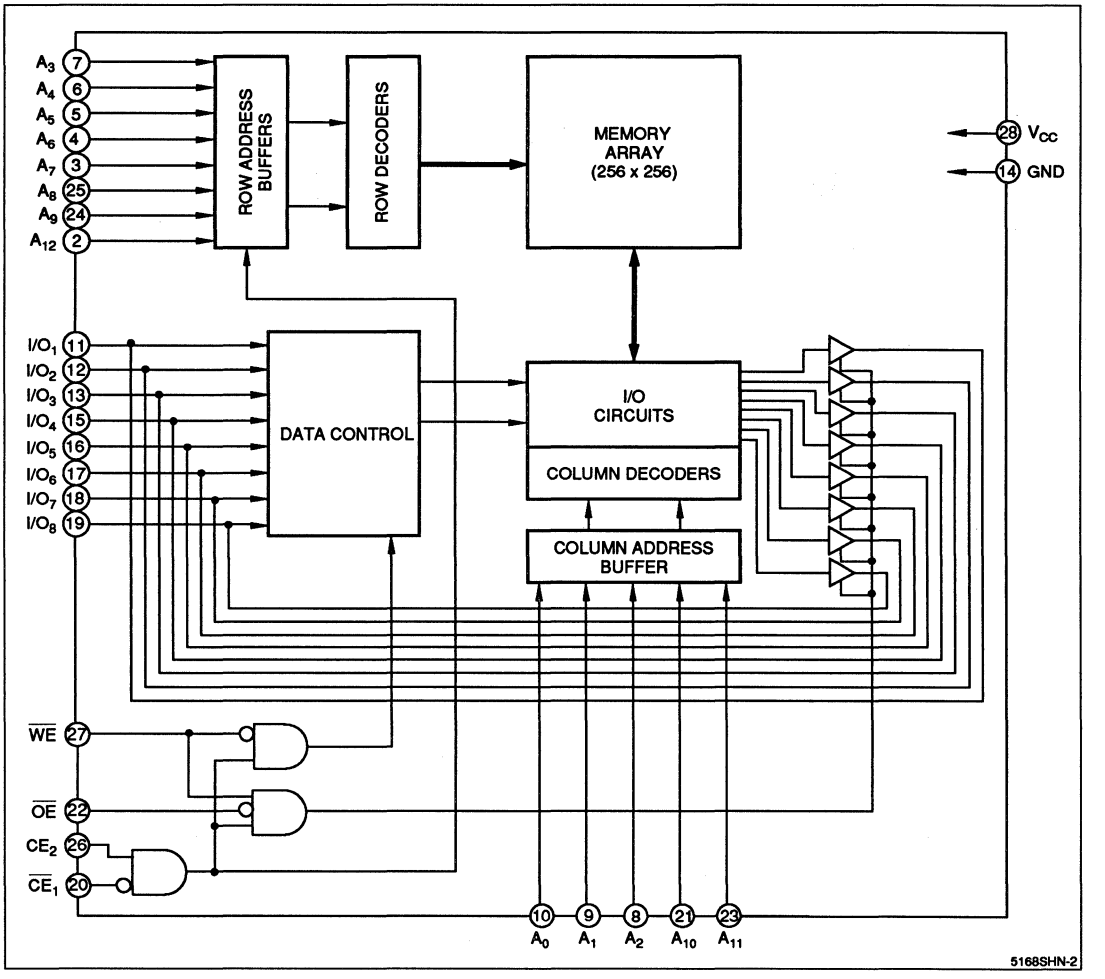


Figure 2. LH5168SH Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE}_1$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.5	3.0	5.5	V
Input voltage	V_{IH}	V_{CC} - 0.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.2	V

DC CHARACTERISTICS (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}		1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Outputs open		50	mA	
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}		10	mA	
	I_{SB}	$CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V		1.0	µA	1
				3.0	µA	2
Output Low voltage	V_{OL}	I_{OL} = 400 µA		0.5	V	
Output High voltage	V_{OH}	I_{OH} = -400 µA	V_{CC} - 0.5		V	

NOTE:
1. $T_A \le +70$°C
2. $T_A \le +85$°C

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle		t_{RC}	500		ns	
Address access time		t_{AA}		500	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		500	ns	
	(CE_2)	t_{ACE2}		500	ns	
Output enable access time		t_{OE}		100	ns	
Output hold time		t_{OH}	20		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns	1
	(CE_2)	t_{LZ2}	20		ns	1
Output enable to input in Low-Z		t_{OLZ}	10		ns	1
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns	1
	(CE_2)	t_{HZ2}	0	60	ns	1
Output disable to output in High-Z		t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	500		ns	
Chip enable to end of write	t_{CW}	250		ns	
Address valid to end of write	t_{AW}	250		ns	
Address setup time	t_{AS}	100		ns	
Write pulse width	t_{WP}	150		ns	
Write recovery time	t_{WR}	50		ns	
Data valid to end of write	t_{DW}	100		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	20		ns	
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE (T_A = 25°C, f = 1MHz)

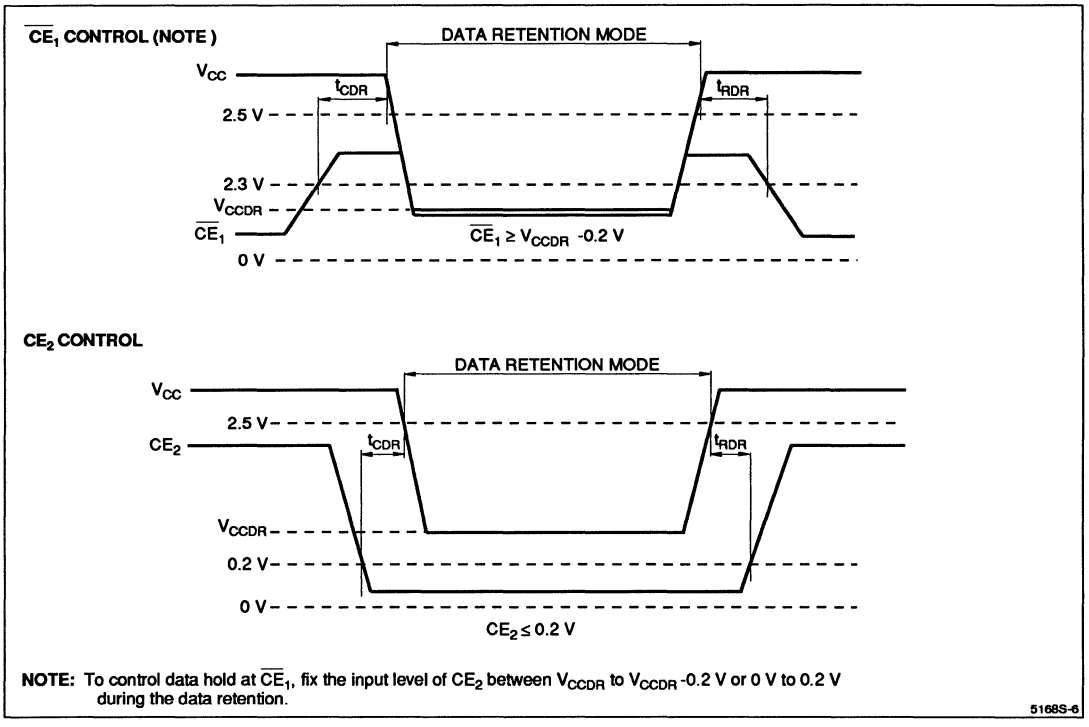
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CCDR}$ - 0.2 V	2.0		V	
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V, $CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CCDR}$ - 0.2 V		1.5	µA	
Chip disable to data retention	t_{CDR}		0		ns	
Recovery time	t_{RDR}		t_{RC}		ns	1

NOTE:
1. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention.

5168S-6

Figure 3. Low Voltage Data Retention

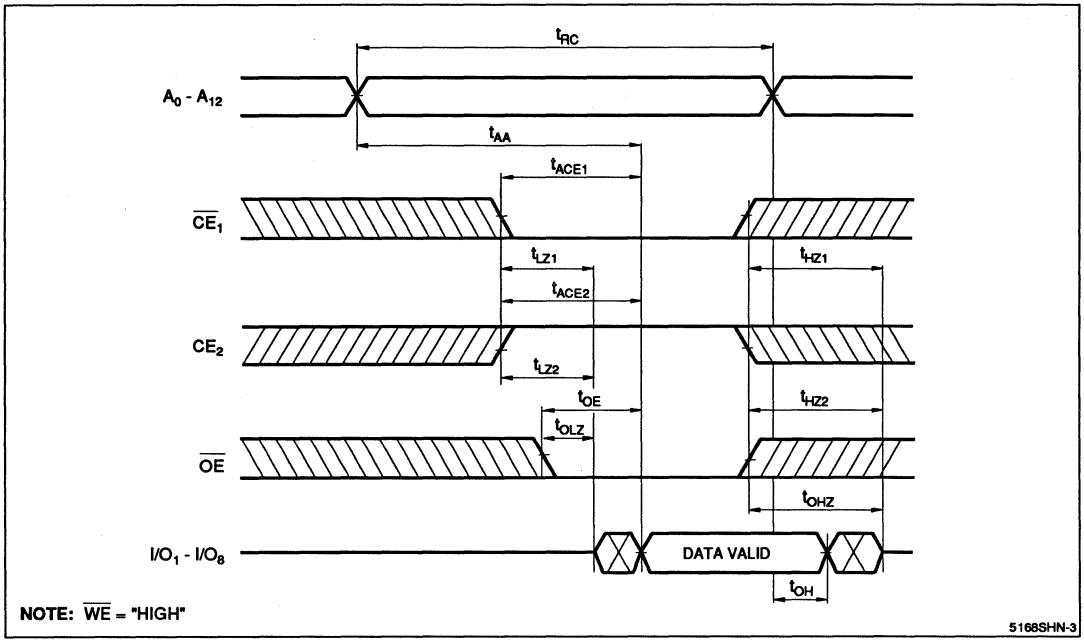
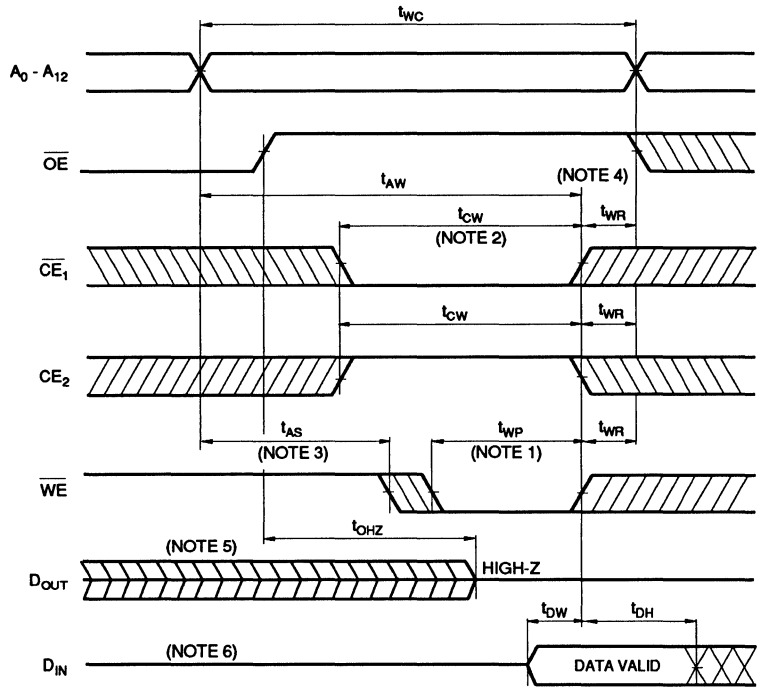


Figure 4. Read Cycle

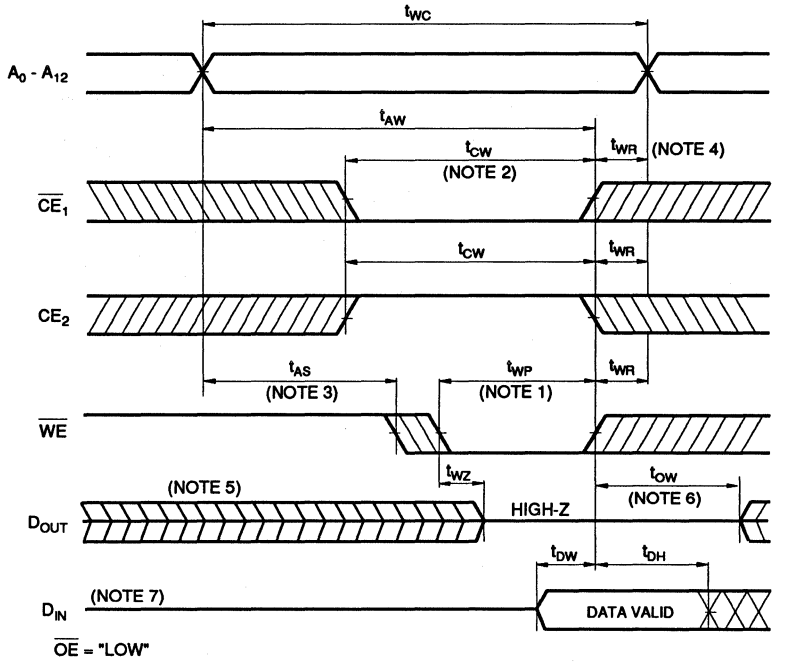


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168SHN-4

Figure 5. Write Cycle 1



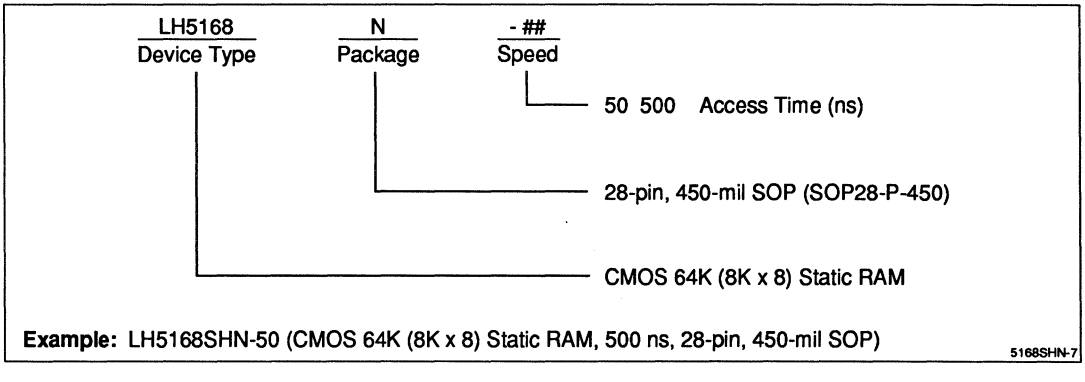
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168SHN-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH5168SHN-50 (CMOS 64K (8K x 8) Static RAM, 500 ns, 28-pin, 450-mil SOP)

5168SHN-7

LH51256

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 248 mW (MAX.)
  (T_A = -40 to 85°C, minimum cycle)
  Standby: 16.5 μW (MAX.)
  (T_A = 0 to 60°C)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH51256 is a 256K bit static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

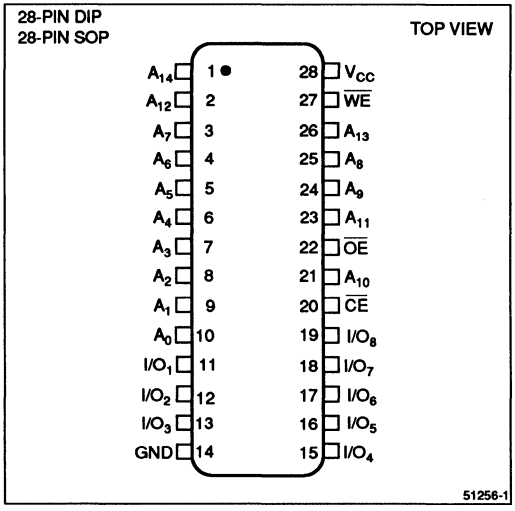


Figure 1. Pin Connections for DIP and SOP Packages

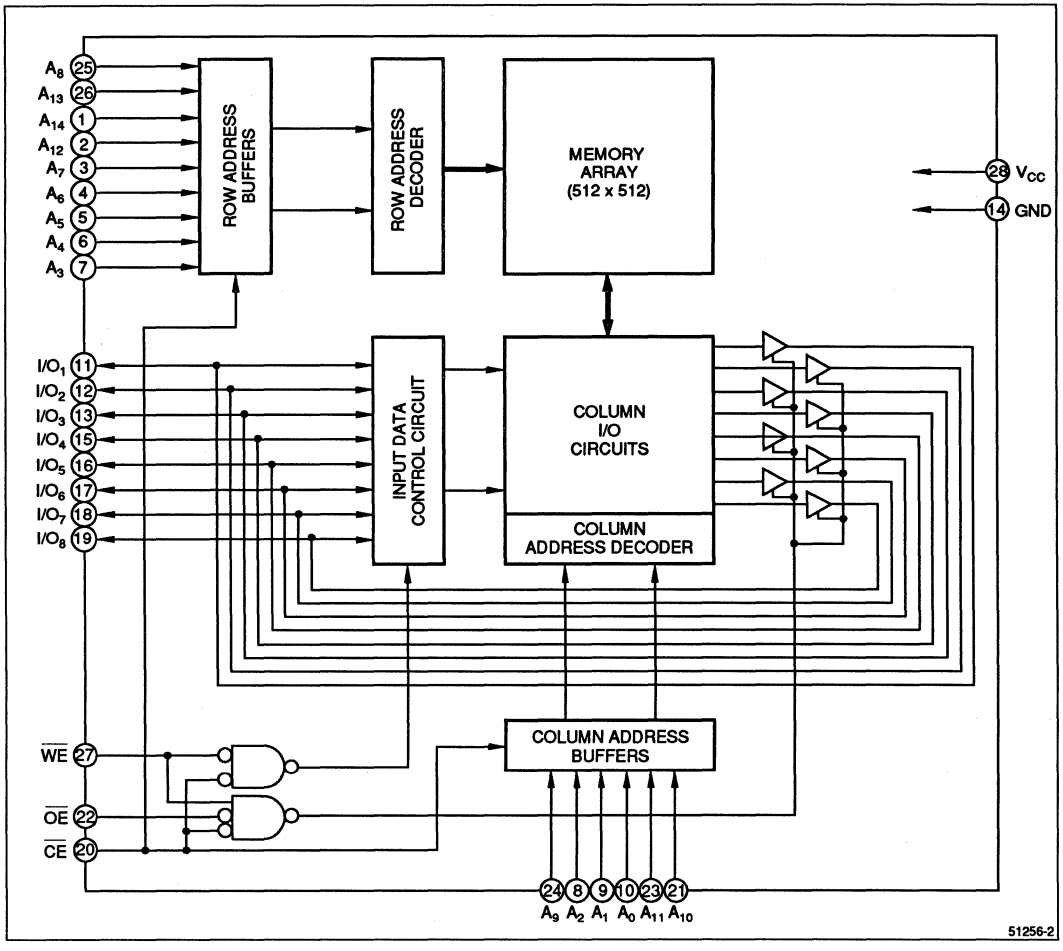


Figure 2. LH51256 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data I/O
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	I_{CC}	NOTE
H	X	X	Non selected	High-Z	Standby (I_{SB})	1
L	L	X	Write	Data in	Operating (I_{CC})	1
L	H	L	Read	Data out	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to + 85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} +0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			45	mA
Standby current	I_{SB1}	$\overline{CE}$= V_{IH}			10	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V, T_A = 0 to +60°C			3	µA
		$\overline{CE}$ ≥ V_{CC} - 0.2 V, T_A = -40 to +85°C			10	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10		LH51256/N-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	
$\overline{CE}$ access time	t_{ACE}		100		120	ns	
Output enable time	t_{OE}		50		60	ns	
Output hold time	t_{OH}	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10		LH51256/N-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
$\overline{CE}$ Low to end of write	t_{CW}	90		100		ns	
Address valid to end of write	t_{AW}	90		100		ns	
Address setup time	t_{AS}	5		5		ns	
Write recovery time	t_{WR}	15		15		ns	
Write pulse width	t_{WP}	50		50		ns	
Input data setup time	t_{DW}	30		30		ns	
Input data hold time	t_{DH}	10		10		ns	
$\overline{WE}$ High to output active	t_{OW}	0		0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C_L = 100 pF (Includes scope and jig capacitance)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C except as noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2V	2.0			V	
Data retention current	I_{CCDR}	V_{CCDR} = 3 V $\overline{CE} \geq V_{CCDR}$ - 0.2V, T_A = 0 to +60°C, V_{IN} = 0 to V_{CCDR}			1	µA	
		V_{CCDR} = 3 V $\overline{CE} \geq V_{CCDR}$ - 0.2V, T_A = -40 to +85°C, V_{IN} = 0 to V_{CCDR}			6	µA	
$\overline{CE}$ setup time	t_{CDR}		0			ns	
$\overline{CE}$ hold time	t_R		t_{RC}			ns	1

NOTE:
1. t_{RC} = Read cycle time

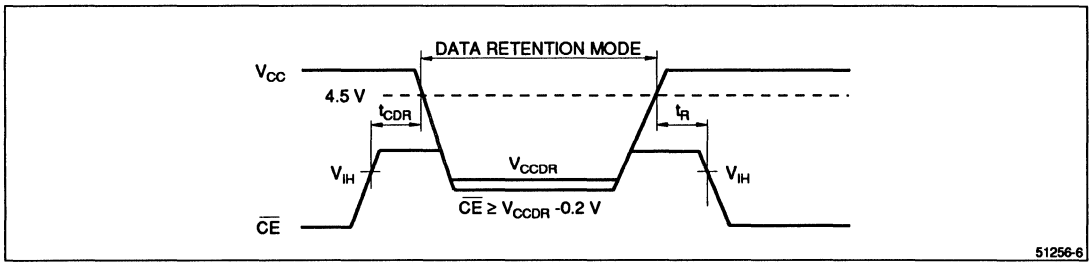


Figure 3. Low Voltage Data Retention

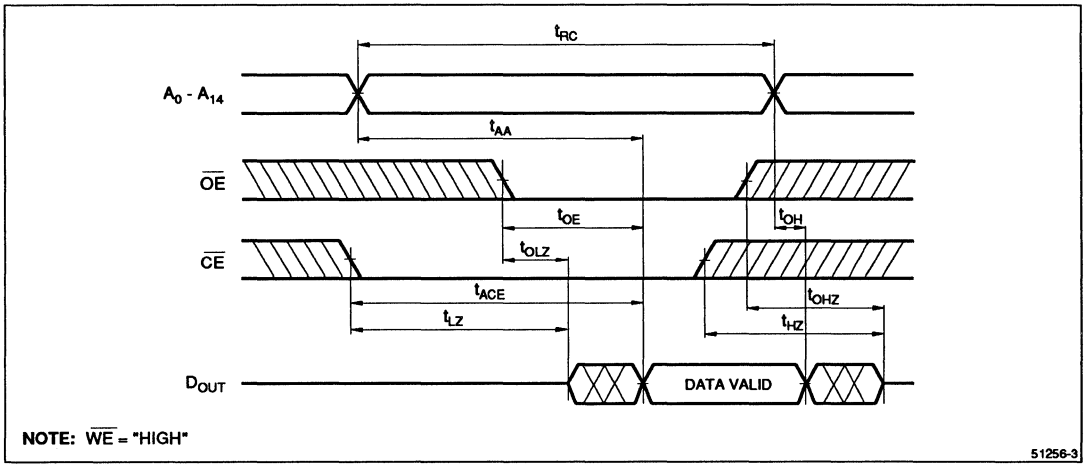
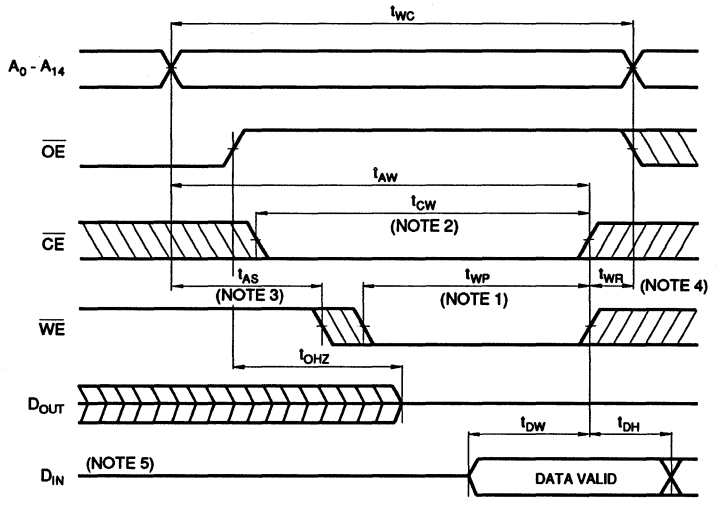


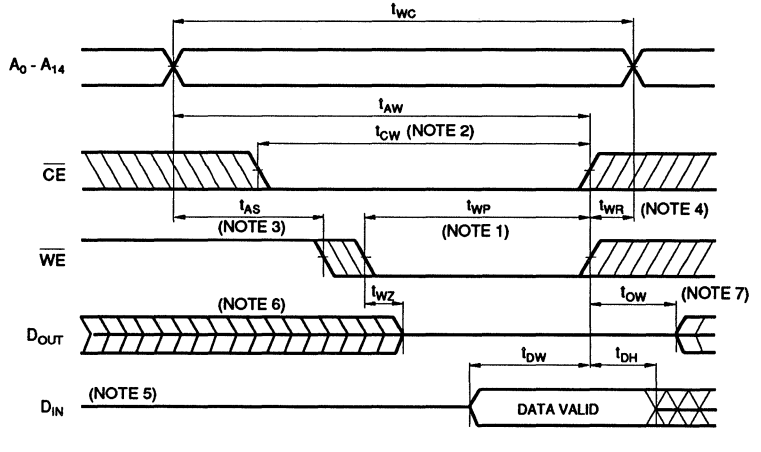
Figure 4. Read Cycle



NOTES:
1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from the $\overline{CE}$ low transition to the end of write.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

51256-4

Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)

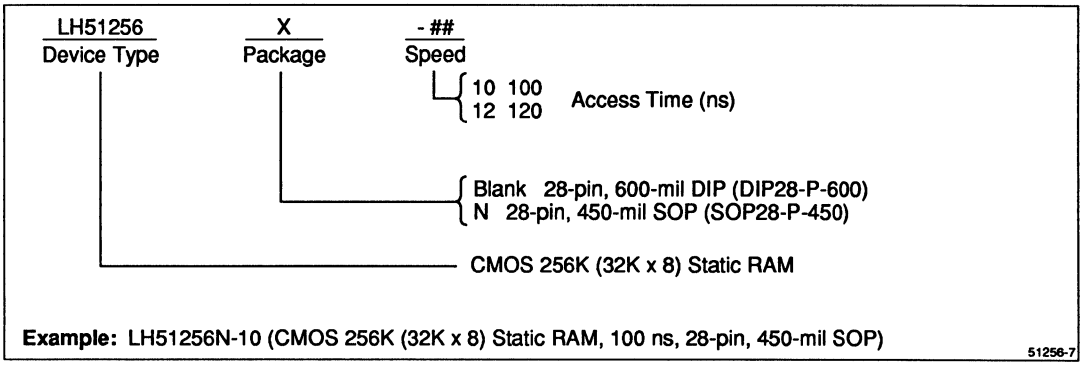


NOTES:
1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from the $\overline{CE}$ low transition to the end of write.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

51256-5

Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

ORDERING INFORMATION



Example: LH51256N-10 (CMOS 256K (32K x 8) Static RAM, 100 ns, 28-pin, 450-mil SOP)

51256-7

LH51256L

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 248 mW (MAX.)
  (T_A = -40 to 85°C, minimum cycle)
  Standby: 5.5 µW (MAX.)
  (T_A = 0 to 60°C)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH51256L is a 256K bit static RAM organized as 32,768 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

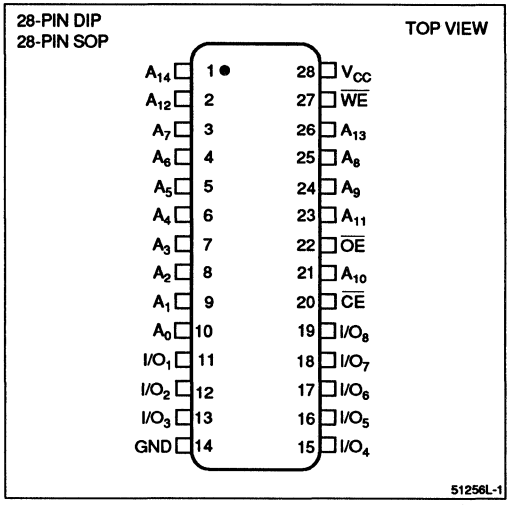


Figure 1. Pin Connections for DIP and SOP Packages

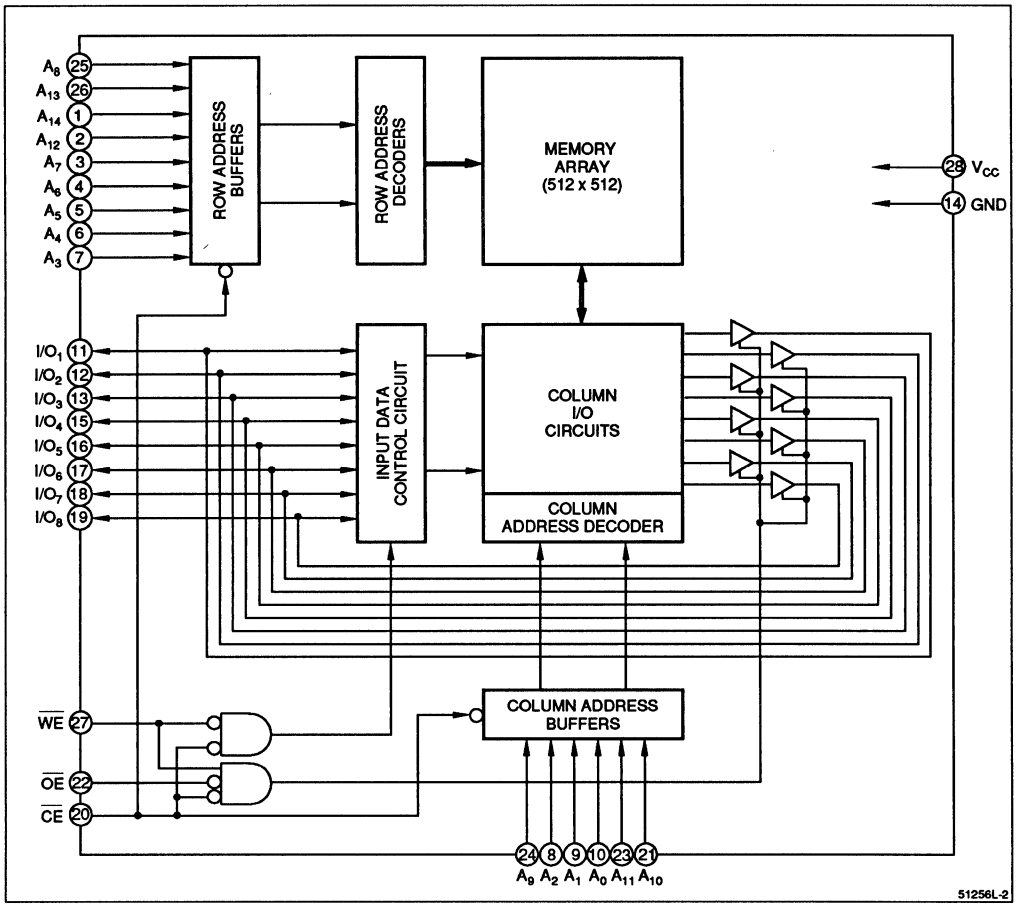


Figure 2. LH51256L Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Standby (I_{SB})	1
L	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			45	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			10	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = 0 to +60°C			1	µA
		$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = -40 to +85°C			5	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	
Chip enable access time	t_{ACE}		100		120	ns	
Output enable access time	t_{OE}		50		60	ns	
Output hold time	t_{OH}	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
$\overline{CE}$ Low to end of write	t_{CW}	90		100		ns	
Address valid to end of write	t_{AW}	90		100		ns	
Address setup time	t_{AS}	5		5		ns	
Write recovery time	t_{WR}	15		15		ns	
Write pulse width	t_{WP}	50		50		ns	
Input data setup time	t_{DW}	30		30		ns	
Input data hold time	t_{DH}	10		10		ns	
$\overline{WE}$ High to output in High-Z	t_{OW}	0		0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C_L = 100 pF (Includes scope and jig capacitance)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$= 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 TO +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V, $\overline{CE} \geq V_{CCDR}$ - 0.2 V, T_A = 0 to +60°C, V_{IN} = 0 to V_{CCDR}			0.6	µA	
		V_{CCDR} = 3.0 V $\overline{CE} \geq V_{CCDR}$ - 0.2 V, T_A = -40 to +85°C, V_{IN} = 0 to V_{CCDR}			3.0	µA	
$\overline{CE}$ setup time	t_{CDR}		0			ns	
$\overline{CE}$ hold time	t_{RDR}		t_{RC}			ns	1

NOTE:

1. t_{RC} = Read cycle time

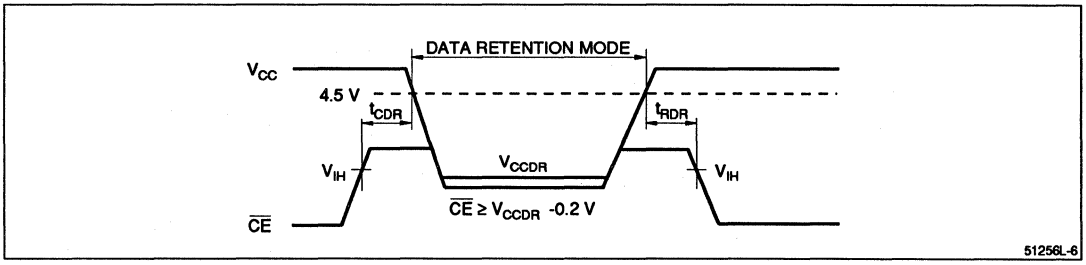


Figure 3. Data Retention Characteristics

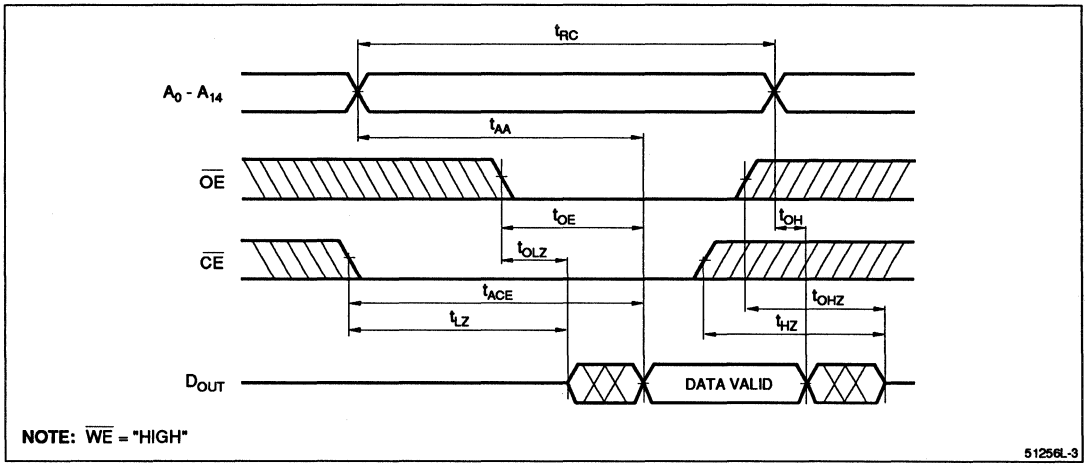
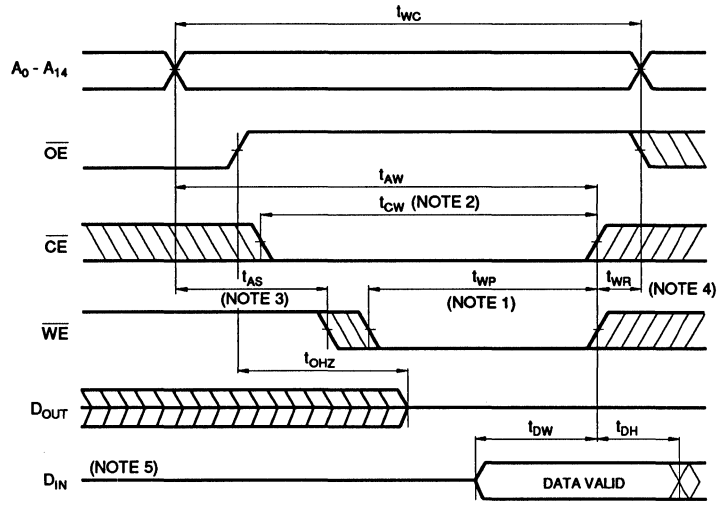


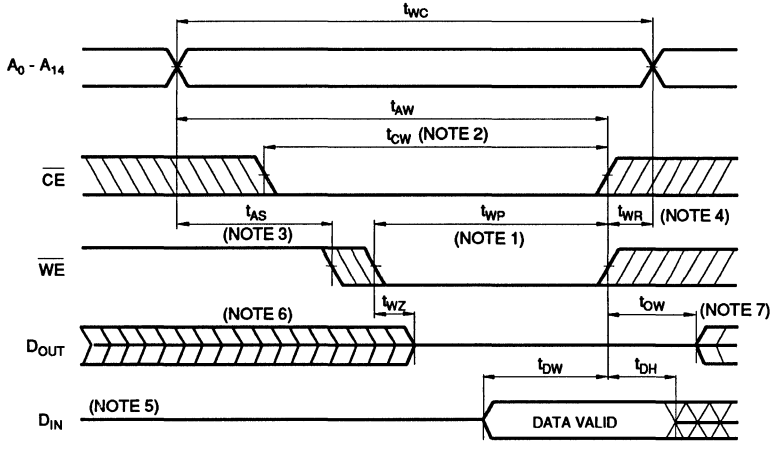
Figure 4. Read Cycle



NOTES:
1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

51256L-4

Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)

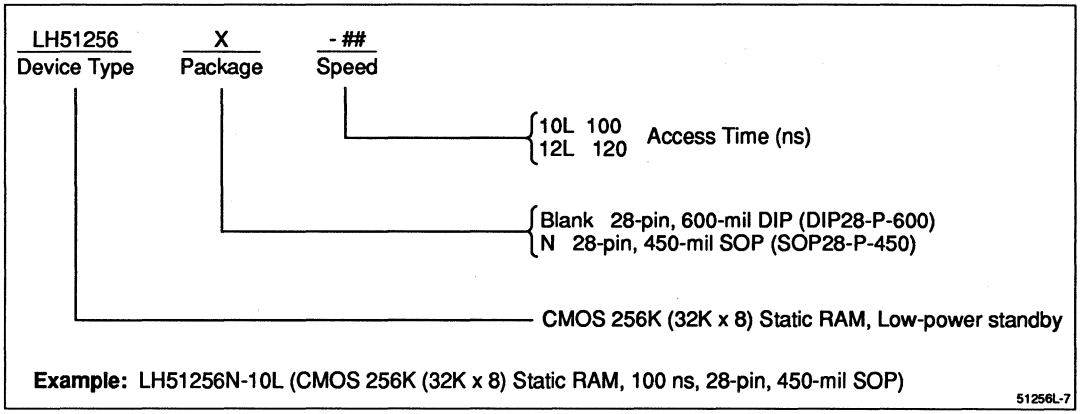


NOTES:
1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

51256L-5

Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

ORDERING INFORMATION



LH511000

PRELIMINARY

CMOS 1M (128K × 8) Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 330 mW (MAX.)
  Standby at T_A = 0 to 70°C
  220 µW (MAX.) ("L" version)
  110 µW (MAX.) ("LL" version)
  22 µW (MAX.) ("UL" version)
- Wide temperature range
  -40 to +85°C
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH511000 is a 1M bit static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

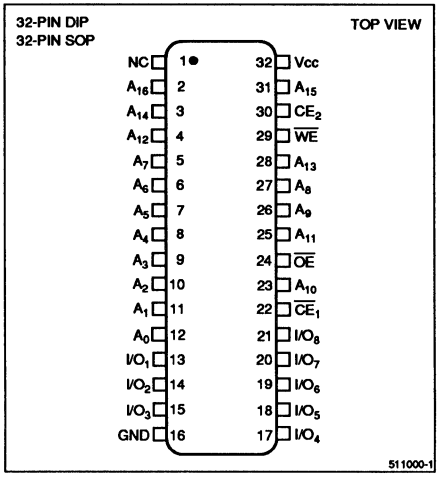


Figure 1. Pin Connections for DIP and SOP Packages

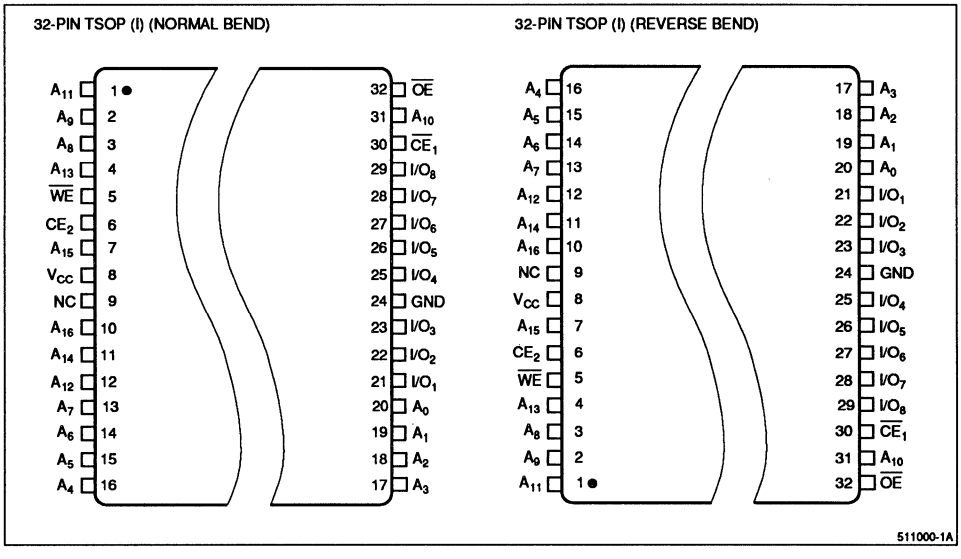


Figure 2. Pin Connections for TSOP Packages

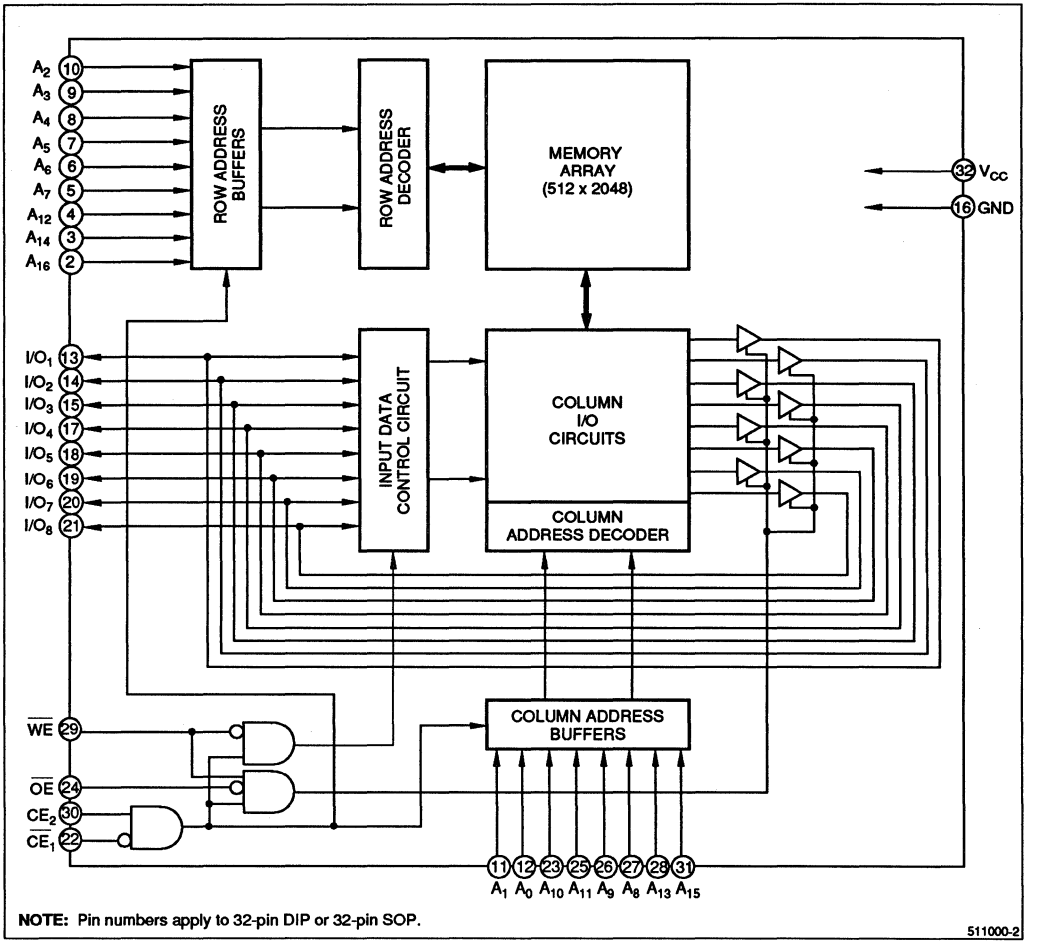


Figure 3. LH511000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	STANDBY CURRENT	NOTE
H	X	X	X	Non selected	High-Z	Standby (I_{SB1})	1
X	L	X	X	Non selected	High-Z	Standby (I_{SB1})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +80°C)

PARAMETER	SYMBOL	CONDITIONS	LH511000L			LH511000LL			LH511000UL			UNIT	NOTE
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Output LOW voltage	V_{OL}	I_{OL} = 2.0 mA			0.4			0.4			0.4	V	
Output HIGH voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			2.4			2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}			1			1			1	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}, or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 to V_{CC}			1			1			1	µA	
Operating current	I_{CC1}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Cycle = MIN. Outputs open			60			60			60	mA	
	I_{CC2}	$\overline{CE_1}$ ≤ 0.2 V or V_{CC} - 0.2 V V_{IN} ≤ 0.2 V or V_{CC} - 0.2 V, Cycle = 1 MHz, Outputs open		1	6		1	6		1	6	mA	1
				5	15		5	15		5	15		2
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			3			3			3	mA	
	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$, CE_2 ≥ V_{CC} - 0.2 V			40			20			4	µA	3
					120			60			12		4

NOTES:
1. Read cycle
2. Write cycle
3. T_A = 0 to 70°C
4. T_A = -40 to +85°C

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	100 ns		120 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	
Chip enable access time	t_{ACE1}		100		120	ns	
	t_{ACE2}		100		120	ns	
Output enable time	t_{OE}		50		60	ns	
Output hold time	t_{OH}	10		10		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ1}	5		5		ns	1
	t_{LZ2}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ1}	0	35	0	45	ns	1
	t_{HZ2}	0	35	0	45	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	35	0	45	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH511000/N-10,-10L		LH511000/N-12,-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
$\overline{CE}$ Low to end of write	t_{CW}	80		100		ns	
Address valid to end of write	t_{AW}	80		100		ns	
Address setup time	t_{AS}	0		0		ns	
Write recovery time	t_{WR}	0		0		ns	
Write pulse width	t_{WP}	75		85		ns	
Input data setup time	t_{DW}	40		50		ns	
Input data hold time	t_{DH}	0		0		ns	
$\overline{WE}$ High to output in High-Z	t_{OW}	0		0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	5		5		ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	35	0	45	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 to 2.2 V
Input rise/fall time	5 ns
Timing reference level	1.5 V
Output load conditions	1TTL + 100 pF (Includes scope and jig capacitance)

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF	1
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF	1

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V		2.0			V	
Data retention current	I_{CCDR}	$CE_2 \le 0.2$ V, V_{CC} = 2 V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V V_{CC} = 3 V	25°C			1	µA	1
						0.5		2
						0.1		3
			0 to 70°C			20	µA	1
						10		2
						2		3
			-40 to 85°C			60	µA	1
						30		2
						6		3
$\overline{CE}$ setup time	t_{CDR}			0			ns	
$\overline{CE}$ hold time	t_R			t_{RC}			ns	4

NOTE:
1. LH511000L
2. LH511000LL
3. LH511000UL
4. t_{RC} = Read cycle time

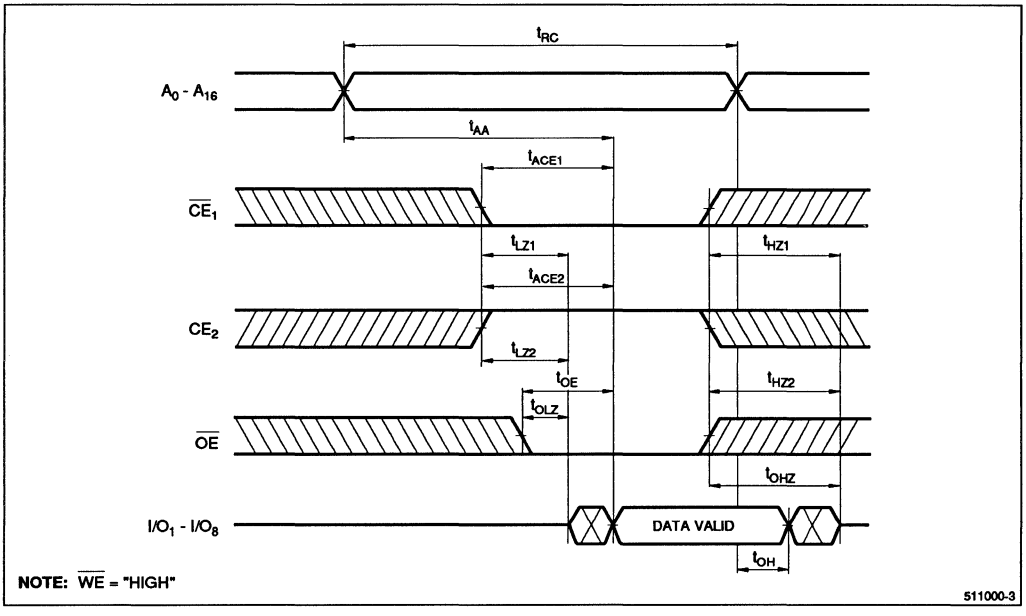
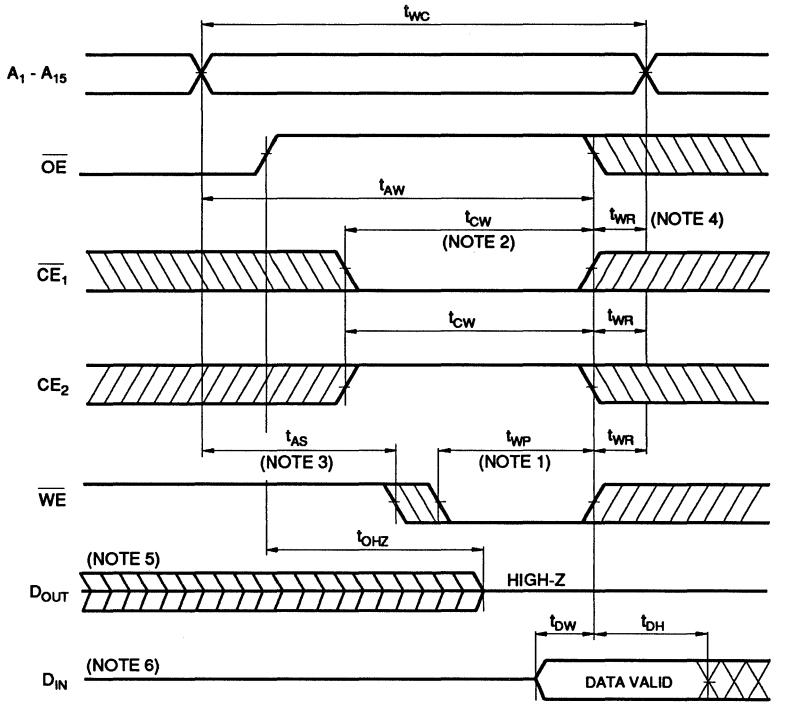


Figure 4. Read Cycle

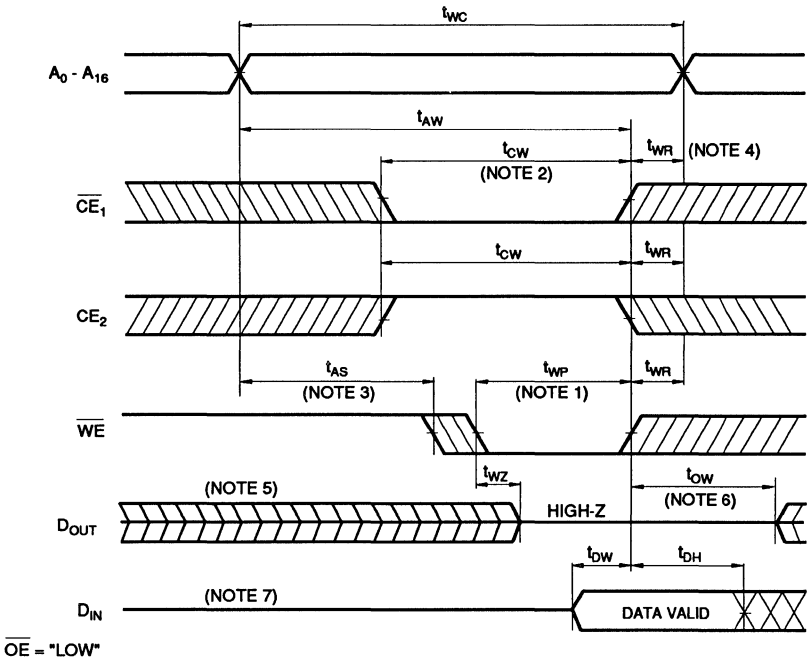


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

511000-4

Figure 5. Write Cycle 1



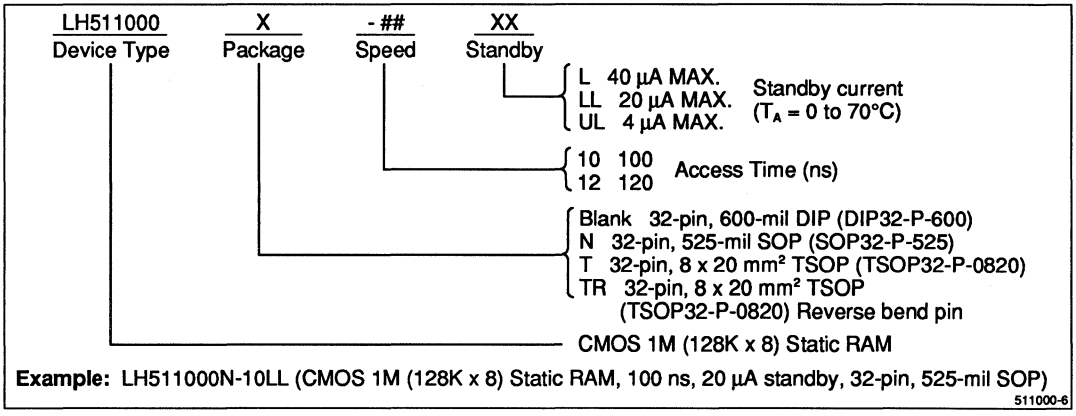
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

511000-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH511000N-10LL (CMOS 1M (128K x 8) Static RAM, 100 ns, 20 µA standby, 32-pin, 525-mil SOP)

511000-6

LH5267A

CMOS 16K × 4 Static RAM

FEATURES

- Fast Access Times: 25/35/45 ns
- Output Enable Control
- JEDEC Standard 24-Pin, 300-mil DIP
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count

FUNCTIONAL DESCRIPTION

The LH5267A is a high-speed 65,536 bit static RAM organized as 16K × 4. Fast, efficient designs are obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power when $\overline{E}$ is inactive (HIGH). Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 14 address lines. Bus contention during Write cycles may be easily avoided by using the output enable ($\overline{G}$) control.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new read cycles can be performed by simply changing the address. The LH5267A offers an Output Enable ($\overline{G}$) control.

High-frequency design techniques should be employed to obtain the best performance from these devices. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

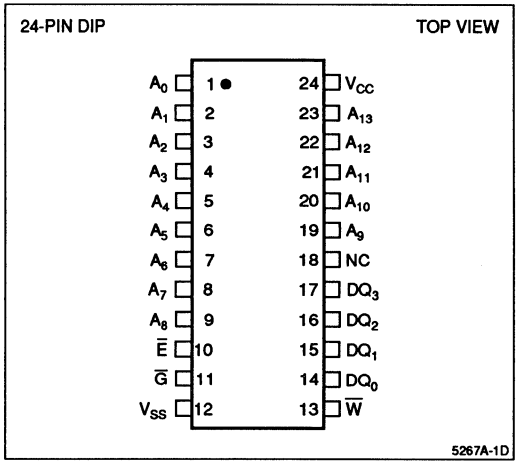


Figure 1. Pin Connections for DIP Package

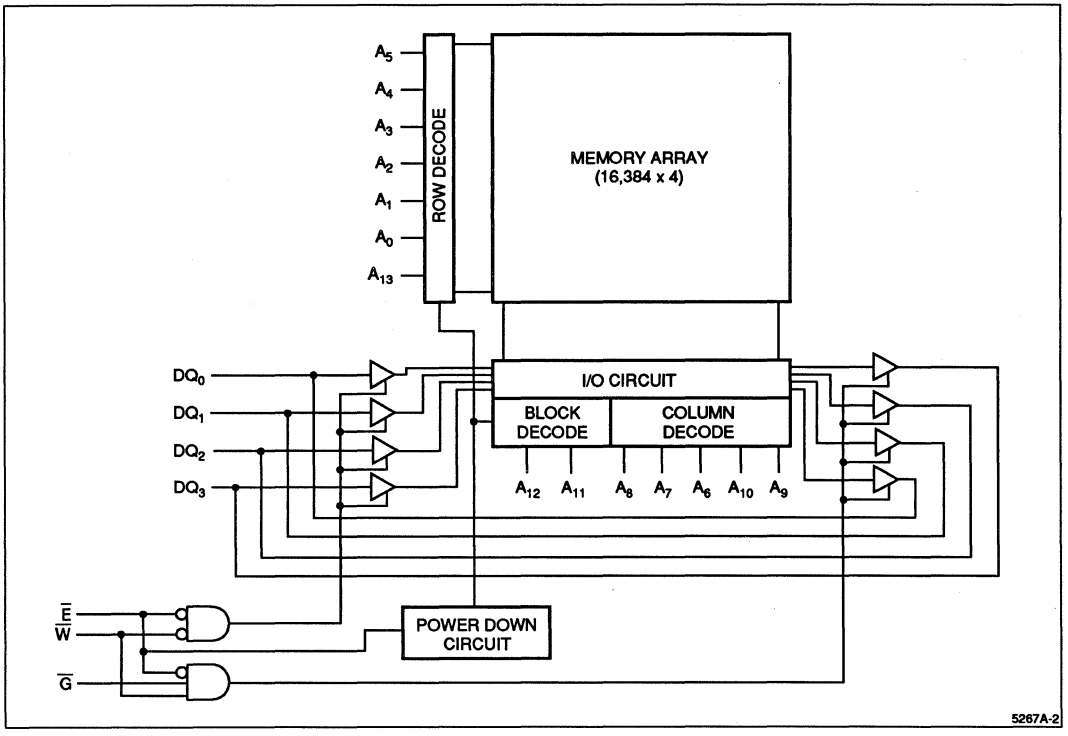


Figure 2. LH5267A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	DQ	I_{CC}
H	X	X	Not Selected	High-Z	Standby
L	H	L	Read	Data Out	Active
L	H	H	Read	High-Z	Active
L	L	X	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{13}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable Input
$\overline{W}$	Write Enable Input
$\overline{G}$	Output Enable Input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	I_{OUT} = 0 mA, t_{CYCLE} = t_{RC} or t_{WC} $\overline{E} \le V_{IL}$, $\overline{G} \ge V_{IH}$			120	mA
I_{SB1}	Standby Current	$\overline{E} \ge V_{CC}$ − 0.2 V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \ge V_{IH}$ min			5	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (Input/Output Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

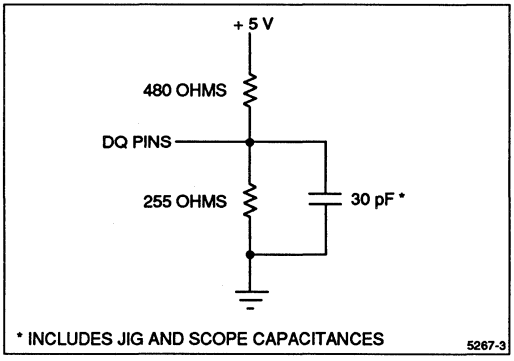


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		15		15	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		15		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	3		3		3		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		10		15		15	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		35		45	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	25		30		40		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		25		35		ns
t_{AW}	Address Valid to End of Write	20		25		35		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		25		30		ns
t_{DW}	Input Data Setup Time	13		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	7	0	10	0	15	ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. The test load has 5 pF capacitances.
3. Sample tested only.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition.

Read Cycle No. 2

Chip is in the Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid when $\overline{E}$ goes LOW. Data-out becomes valid at t_{EA} and may become active as soon as t_{ELZ}. Data-out is valid when both t_{EA} and t_{GA} are met.

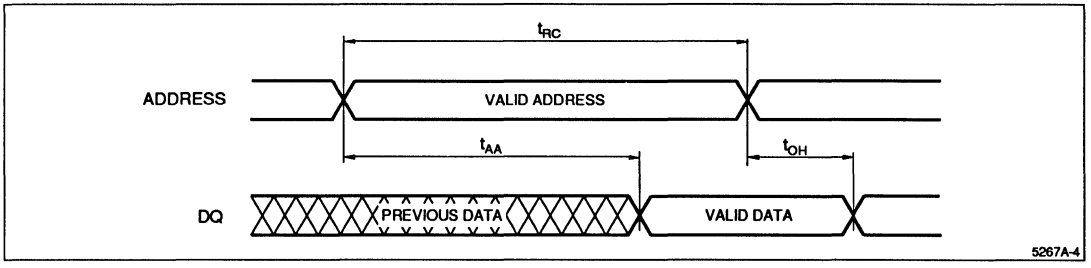


Figure 4. Read Cycle No. 1

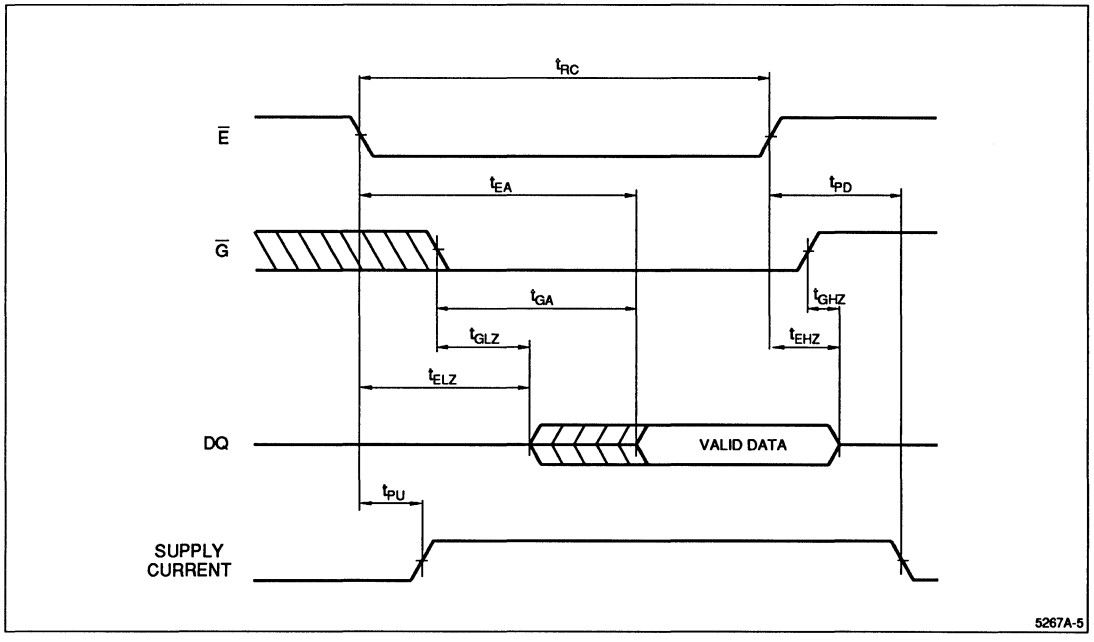


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise. Although these timing diagrams assume $\overline{G}$ is LOW, it is recommended that $\overline{G}$ be kept high during Write cycles to insure that the output drivers are disabled.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

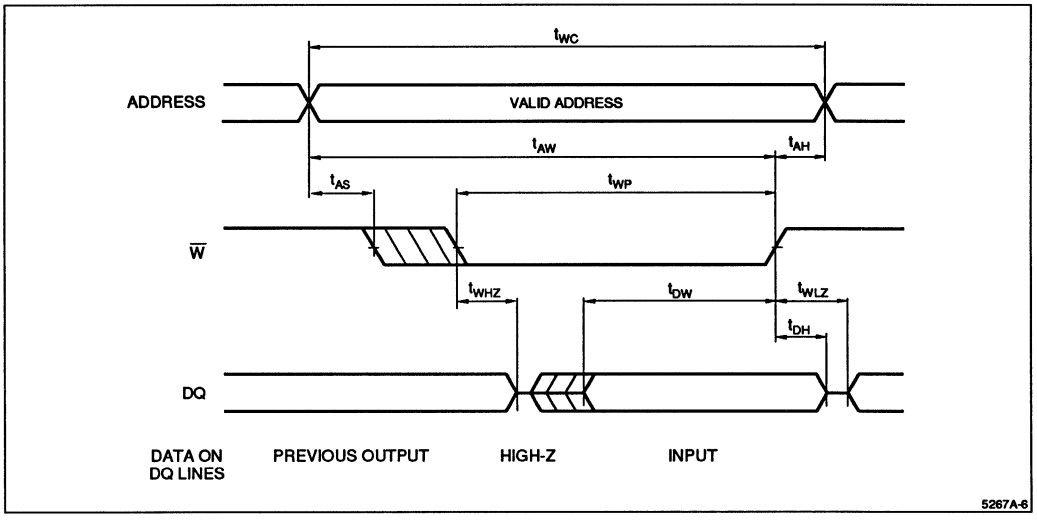


Figure 6. Write Cycle No. 1

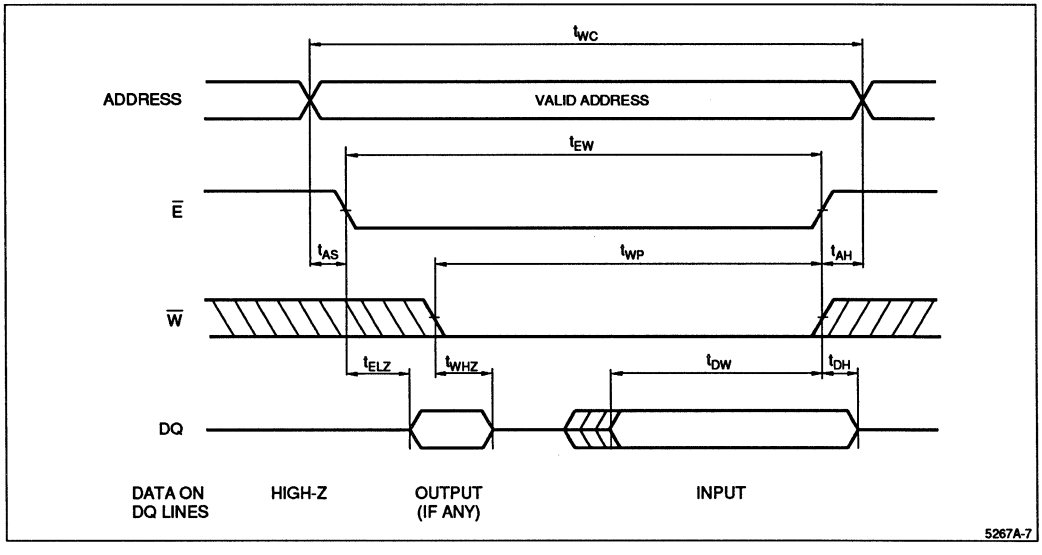
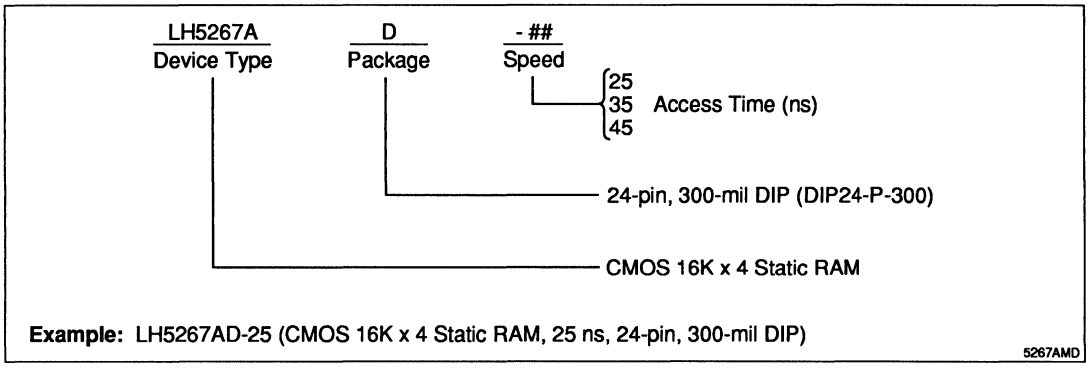


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52250A
LH52250AL

ADVANCE INFORMATION

CMOS 32K × 8 Static RAM

FEATURES

- Access Times: 70/90/100 ns
- Space Saving 28-Pin, 300-mil DIP
- Standard 28-Pin, 600-mil DIP
- Standard 28-Pin, 450-mil SOP Package
- Automatic Power Down During Long Read Cycles
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH52250A is a high-density 262,144 bit static RAM organized as 32K × 8. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address. An Automatic Power Down feature decreases current consumption when Read cycles extend beyond their minimum cycle time.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

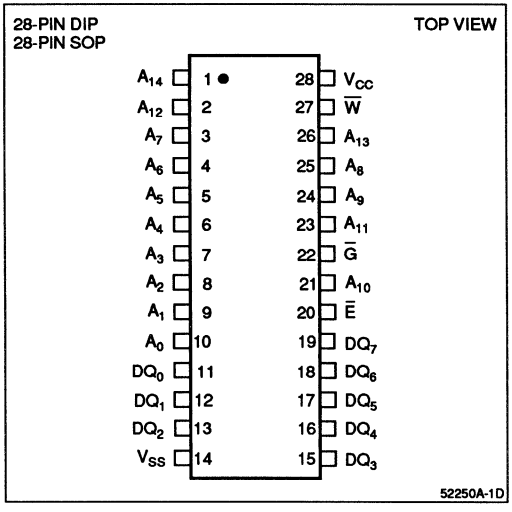


Figure 1. Pin Connections for DIP and SOP Packages

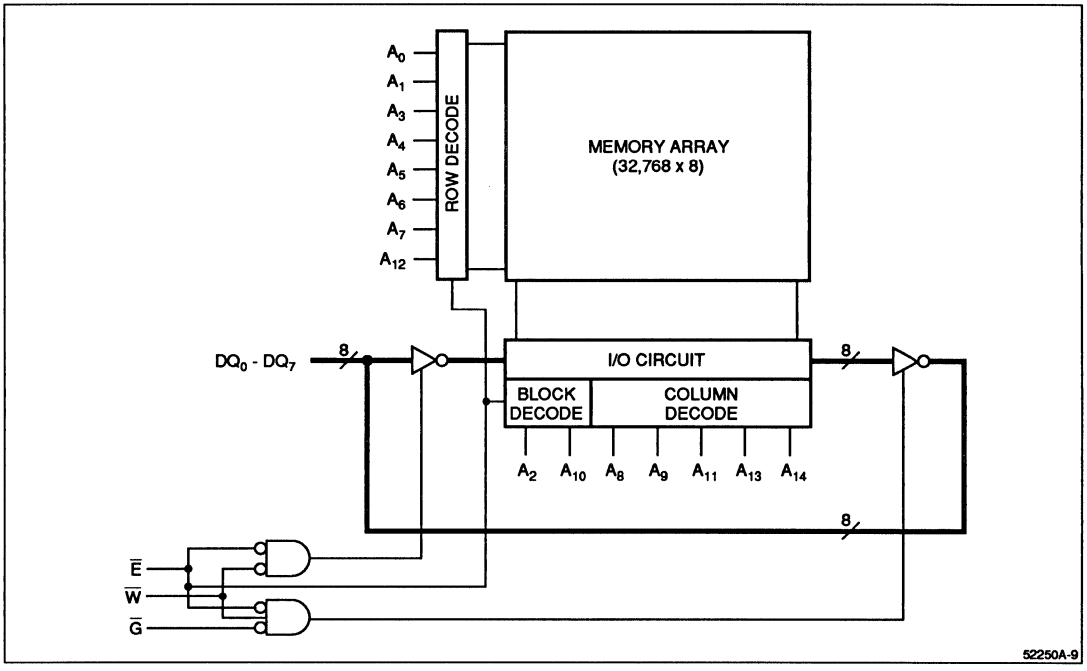


Figure 2. LH52250A/LH52250AL Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{RC} = 70 ns			80	mA
I_{CC1}	Operating Current [1]	t_{RC} = 90 ns			70	mA
I_{CC1}	Operating Current [1]	t_{RC} = 100 ns			70	mA
I_{SB1}	Standby Current: LH52250A	$\overline{E} \geq V_{CC} - 0.2$ V			1	mA
	Standby Current: LH52250AL				0.1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−10		10	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current: LH52250A	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			200	µA
	Data Retention Current: LH52250AL				50	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	0.6 to 2.4 V
Input Rise and Fall Times	10 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

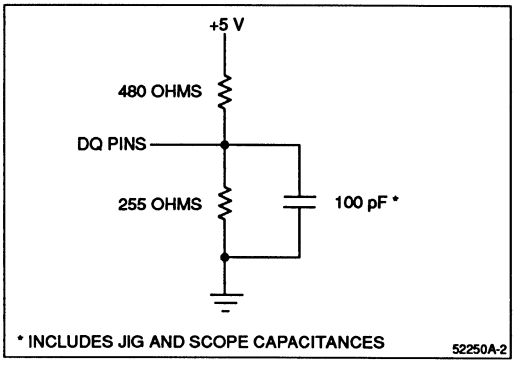


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTE:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

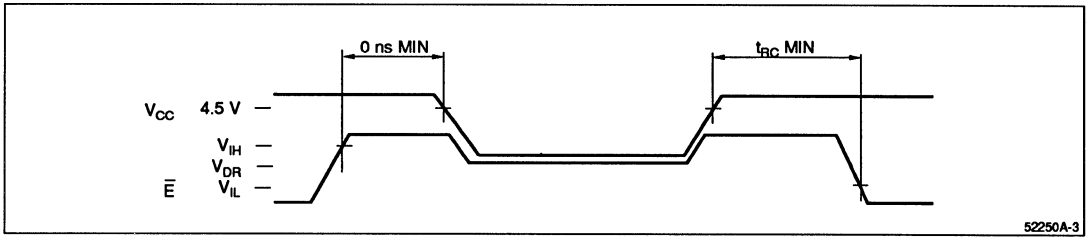


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-70		-90		-10		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Time	70		90		100		ns
t_{AA}	Address Access Time		70		90		100	ns
t_{OH}	Output Hold from Address Change	10		10		10		ns
t_{EA}	$\overline{E}$ Low to Valid Data		70		90		100	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		35		40		45	ns
t_{GA}	$\overline{G}$ Low to Valid Data		40		50		60	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	5		5		5		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		35		40		45	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		70		90		100	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	70		90		100		ns
t_{EW}	$\overline{E}$ Low to End of Write	45		55		65		ns
t_{AW}	Address Valid to End of Write	65		80		90		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	45		55		65		ns
t_{DW}	Input Data Setup Time	30		30		35		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		40		40		45	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	5		5		5		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read Cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid Data will be present following t_{GA} only if t_{EA} timing is met.

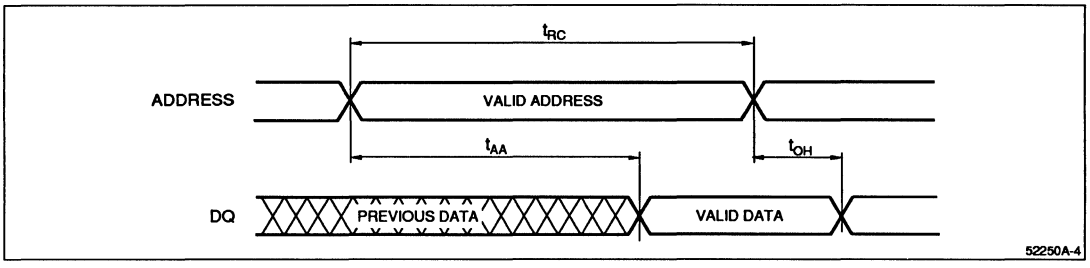


Figure 5. Read Cycle No. 1

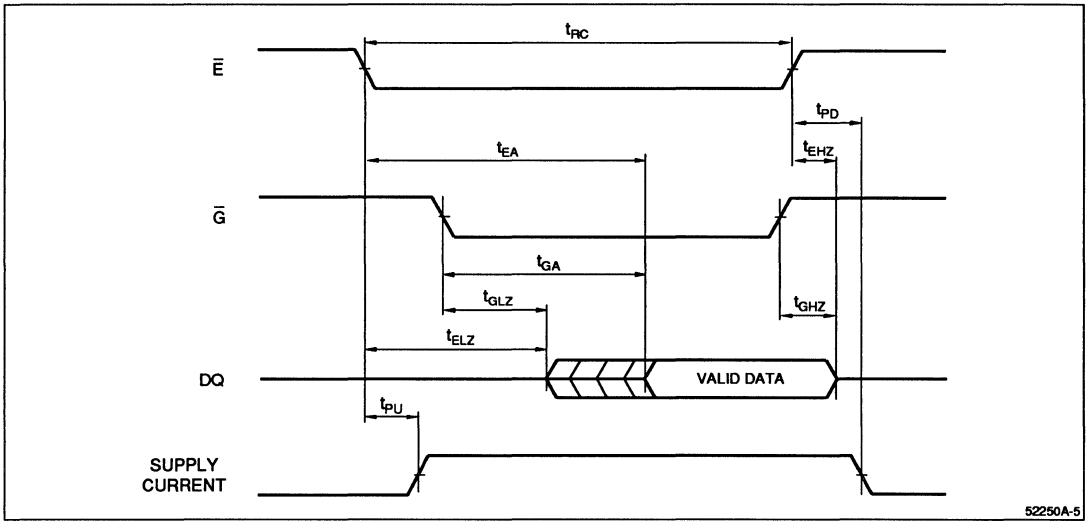


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52250A/LH52250AL's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write Cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

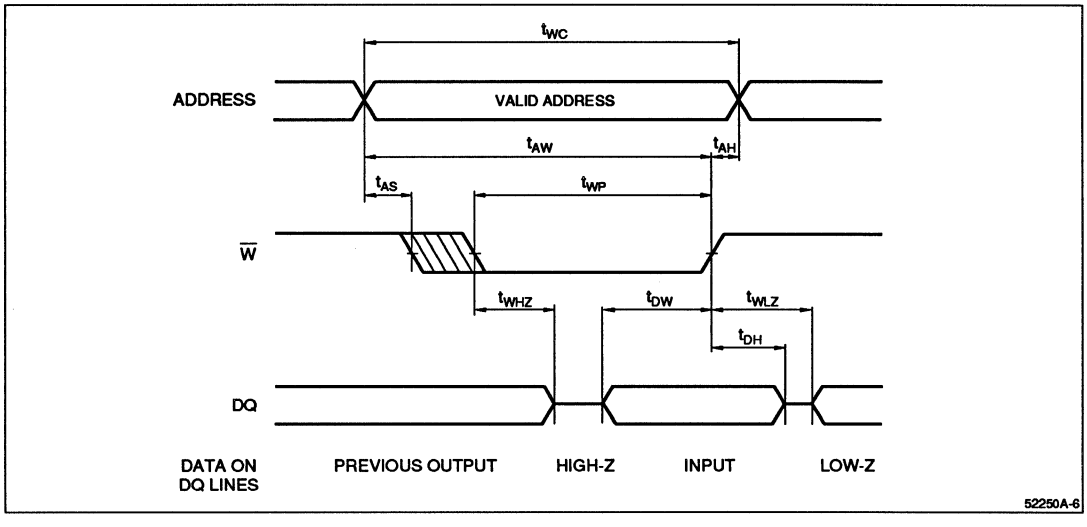


Figure 7. Write Cycle No. 1

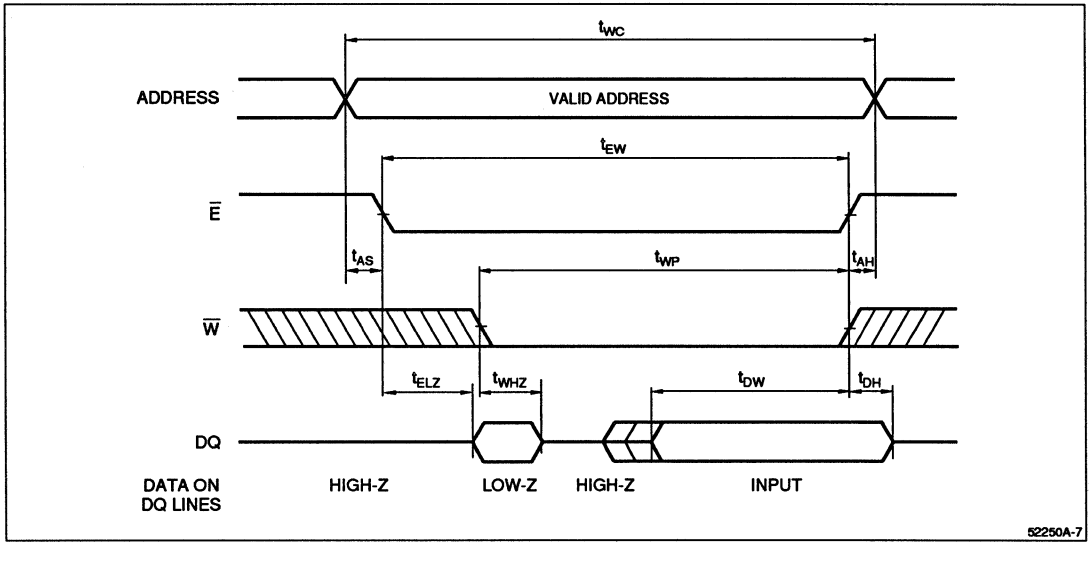
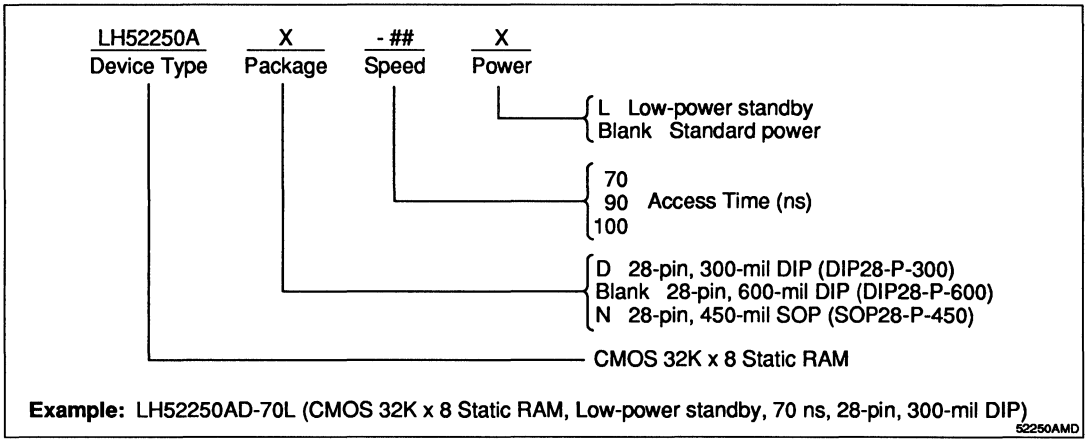


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



Example: LH52250AD-70L (CMOS 32K x 8 Static RAM, Low-power standby, 70 ns, 28-pin, 300-mil DIP)

52250AMD

FEATURES

- Fast Access Times: 25/35/45 ns
- Standard 24-Pin, 300-mil DIP
- Space Saving 24-Pin, 300-mil SOJ
- JEDEC Standard Pinout
- Separate Data Input and Output
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH52251A is a high-speed 262,144 bit static RAM organized as 256K × 1. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power drops to its lowest level (I_{SB1}) if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the D pin to the memory location specified by the 18 address lines. The Q pin goes into a High-Impedance state during Write cycles, allowing the user to connect D and Q together if desired.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

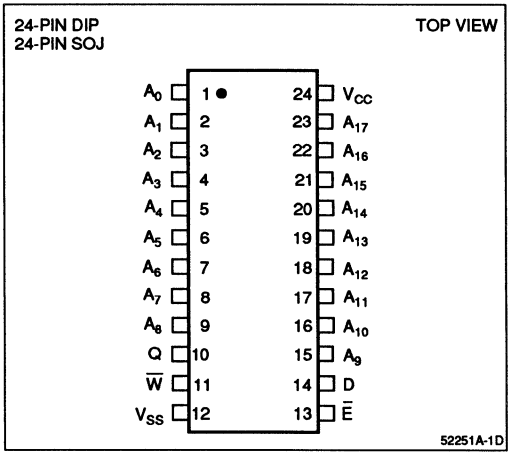


Figure 1. Pin Connections for DIP and SOJ Packages

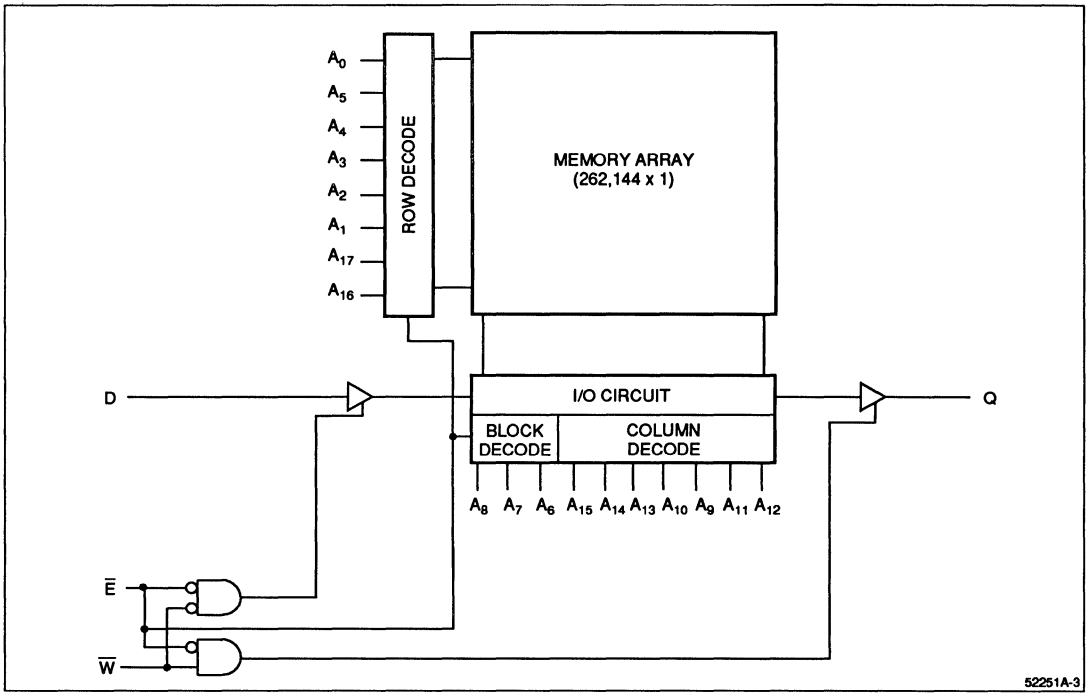


Figure 2. LH52251A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	D	Q	Icc
H	X	Not Selected	X	High-Z	Standby
L	H	Read	X	Data Out	Active
L	L	Write	Data In	High-Z	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
Operating Temperature	0 to 70°C

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Output should not be shorted for more than 30 seconds.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Output open, t_{CYCLE} = 25 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$ or V_{IL}			150	mA
I_{CC1}	Operating Current [1]	Output open, t_{CYCLE} = 35 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$ or V_{IL}			120	mA
I_{CC1}	Operating Current [1]	Output open, t_{CYCLE} = 45 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$ or V_{IL}			100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min			5	mA
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{IN} = 0 V to V_{CC}, V_{CC} = 5.5 V	−2		2	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{IN} = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{E} = V_{IH}$	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			250	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

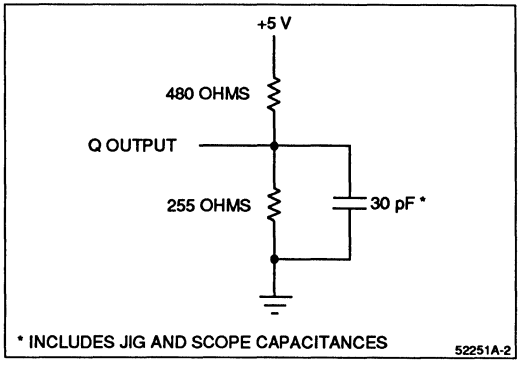


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_D (Input Capacitance)	5 pF
C_Q (Output Capacitance)	7 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

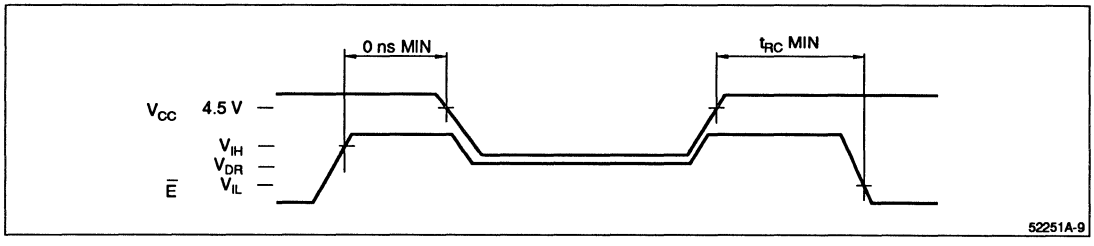


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		12		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		30		40		ns
t_{AW}	Address Valid to End of Write	20		30		40		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		30		40		ns
t_{DW}	Input Data Setup Time	13		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		10		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics measurements specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to active output tests specified for a ±200 mV transition from steady state levels into the test load.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Q implies that Data Out is in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

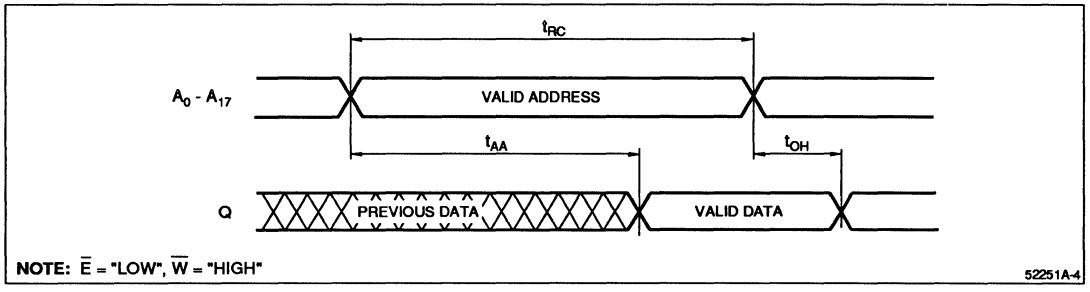


Figure 5. Read Cycle No. 1

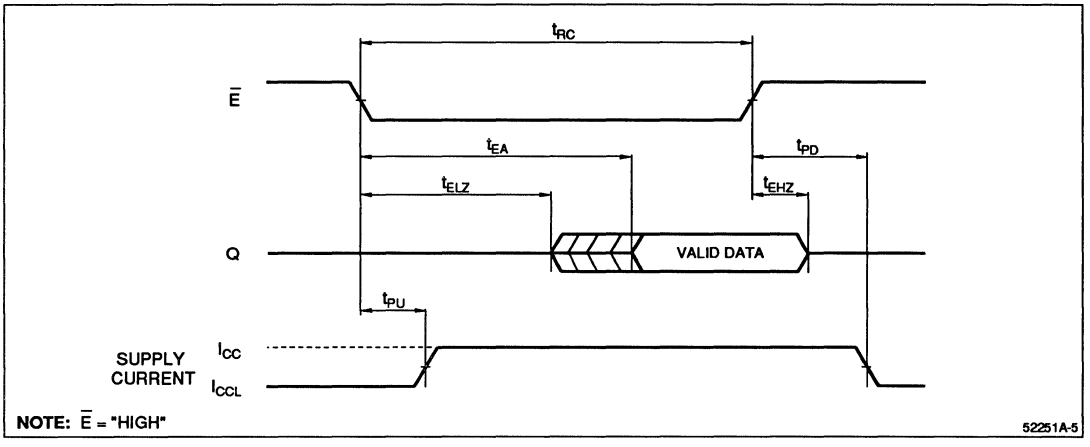


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write Cycles. The output will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW.

Write Cycle No. 2 ($\overline{E}$ Controlled)

Data-out may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

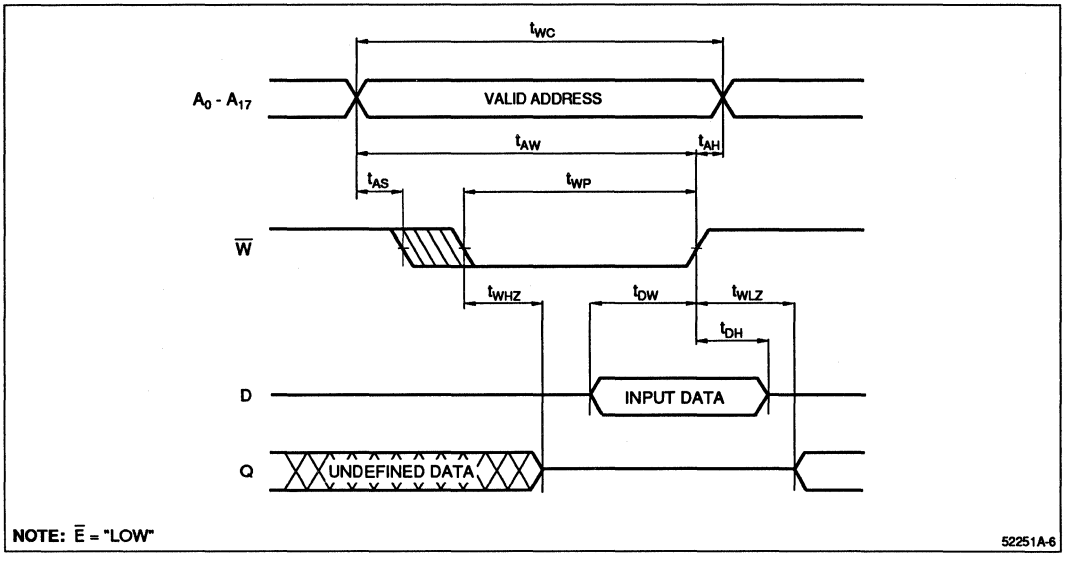


Figure 7. Write Cycle No. 1

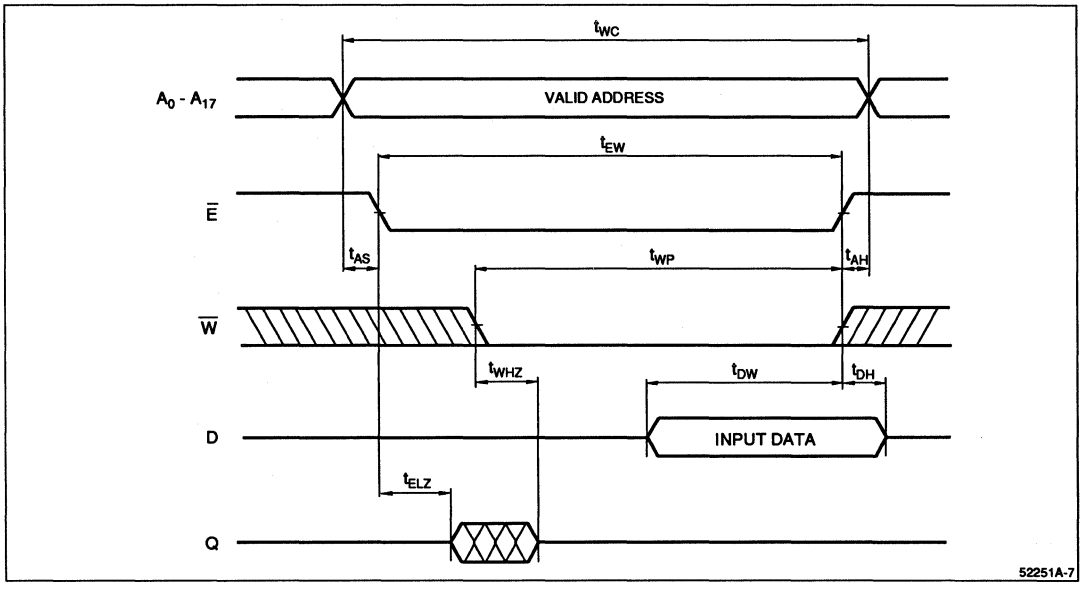
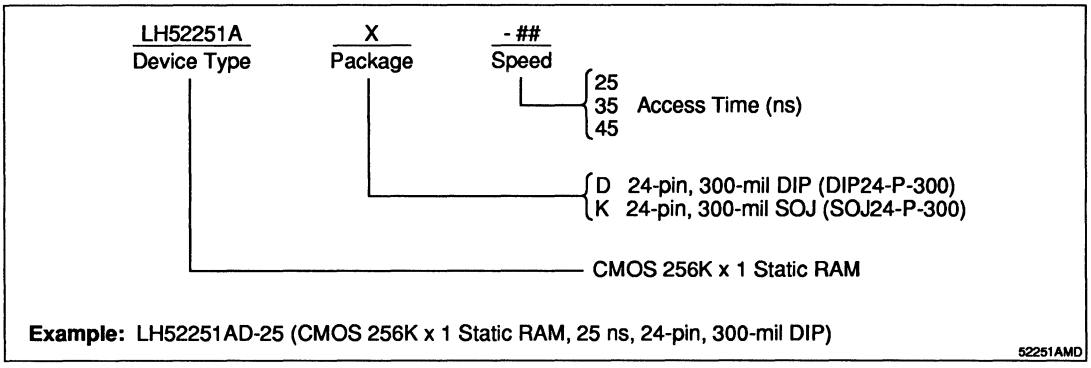


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



Example: LH52251AD-25 (CMOS 256K x 1 Static RAM, 25 ns, 24-pin, 300-mil DIP)

52251AMD

LH52252A

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 25/35/45 ns
- Standard 24-Pin, 300-mil DIP
- Space Saving 24-Pin, 300-mil SOJ
- JEDEC Standard Pinouts
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count

FUNCTIONAL DESCRIPTION

The LH52252A is a high-speed 262,144 bit static RAM organized as 64K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

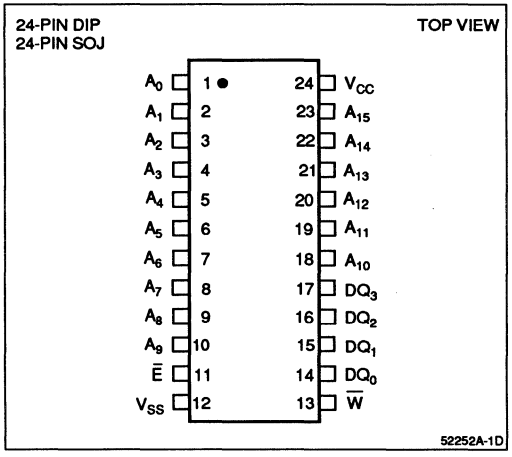


Figure 1. Pin Connections for DIP and SOJ Packages

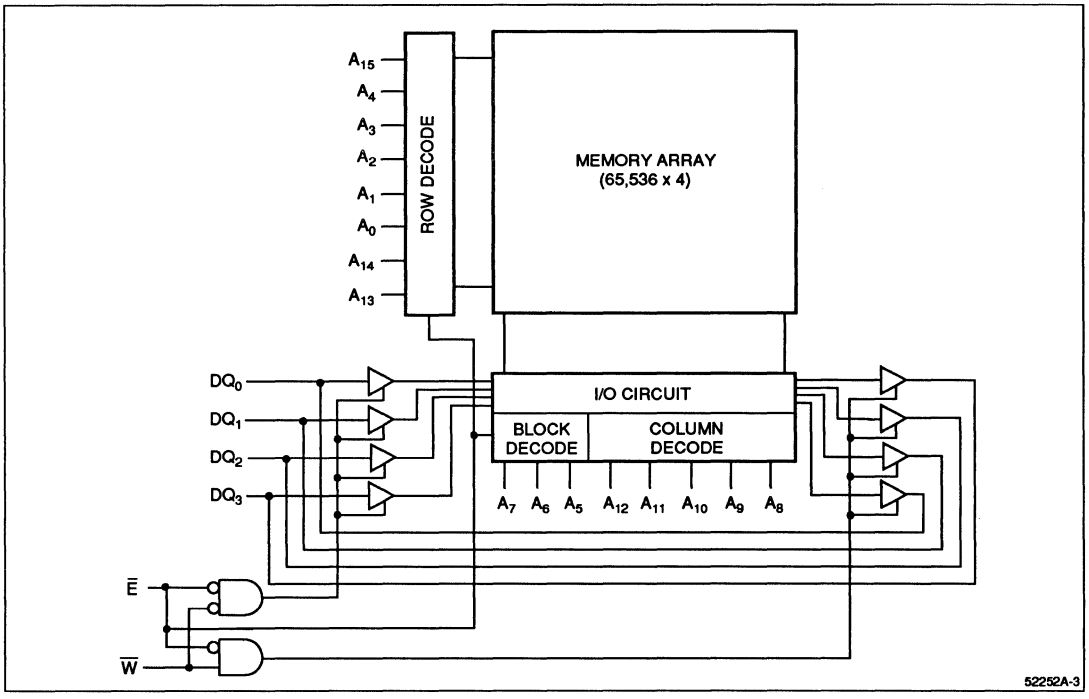


Figure 2. LH52252A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	DQ	Icc
H	X	Not Selected	High-Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE:
X = Don't, Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC}+0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = 25 ns			150	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = 35 ns			120	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = 45 ns			100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			5	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

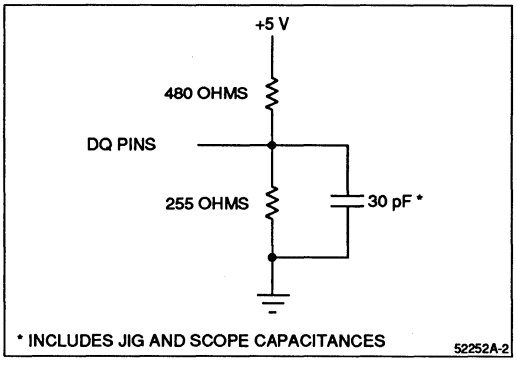


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		12		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [4]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [4]		30		35		40	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		30		35		ns
t_{AW}	Address Valid to End of Write	20		30		35		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		25		35		ns
t_{DW}	Input Data Setup Time	12		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.
4. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data Out.

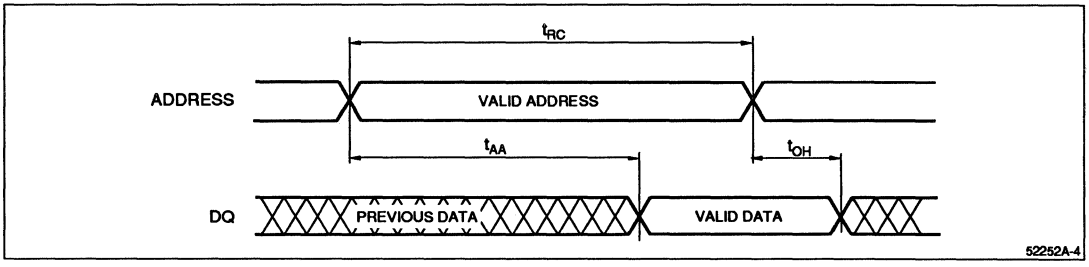


Figure 4. Read Cycle No. 1

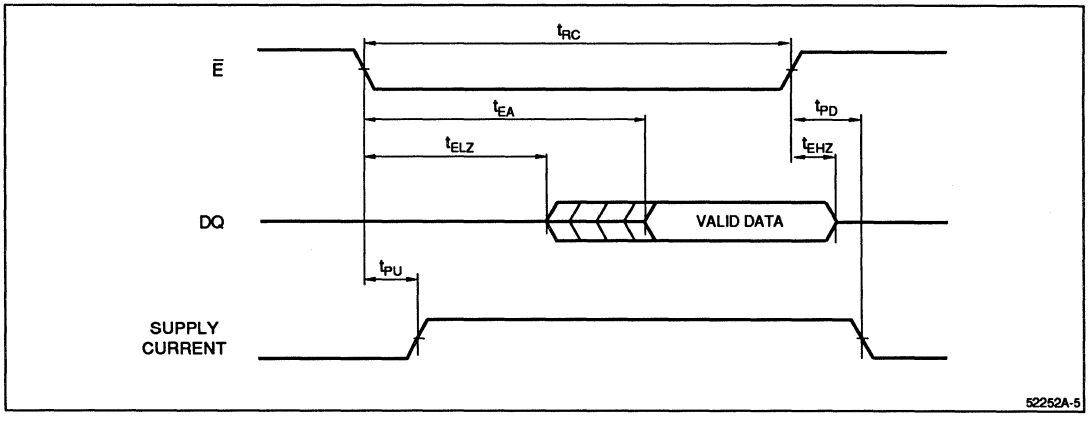


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

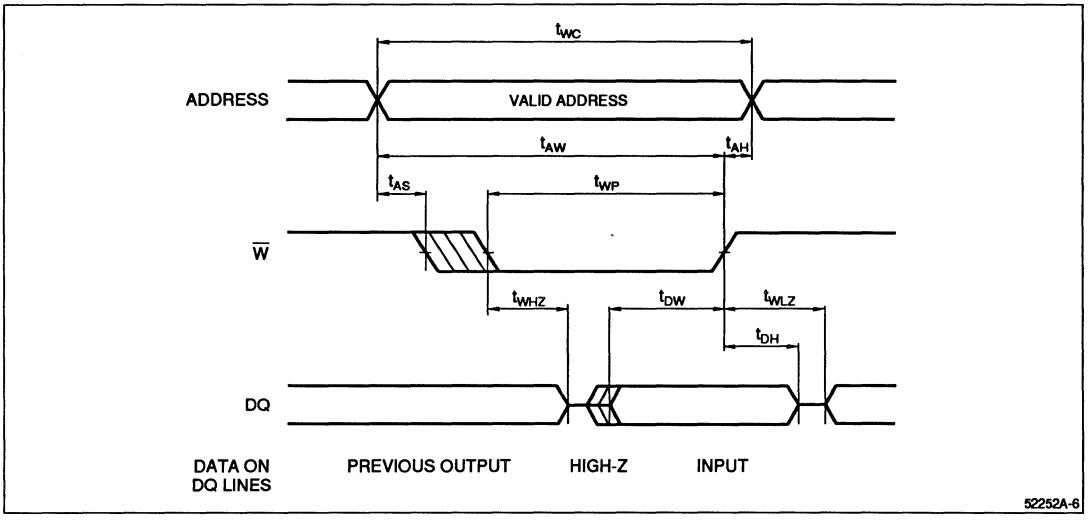


Figure 6. Write Cycle No. 1

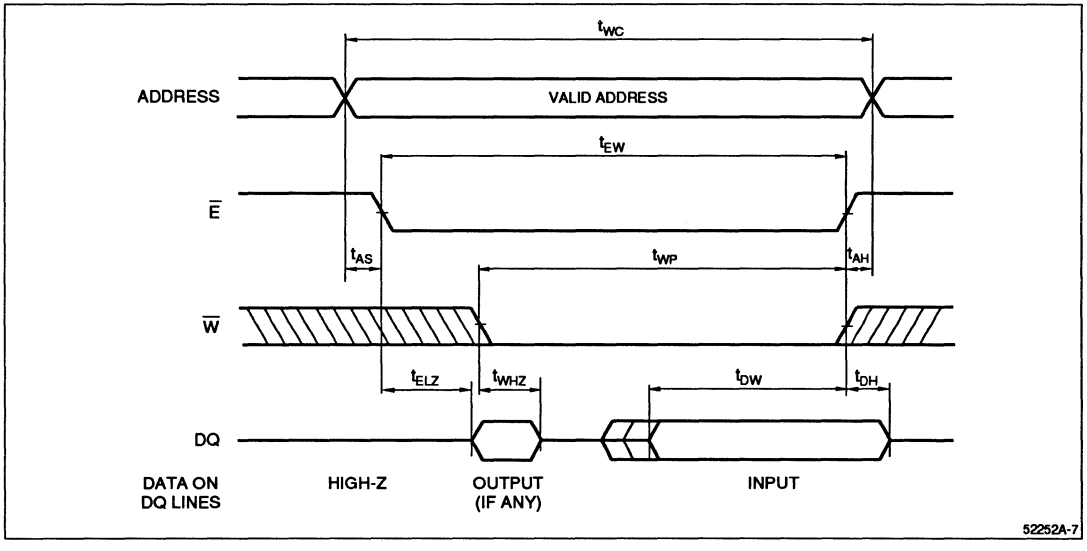
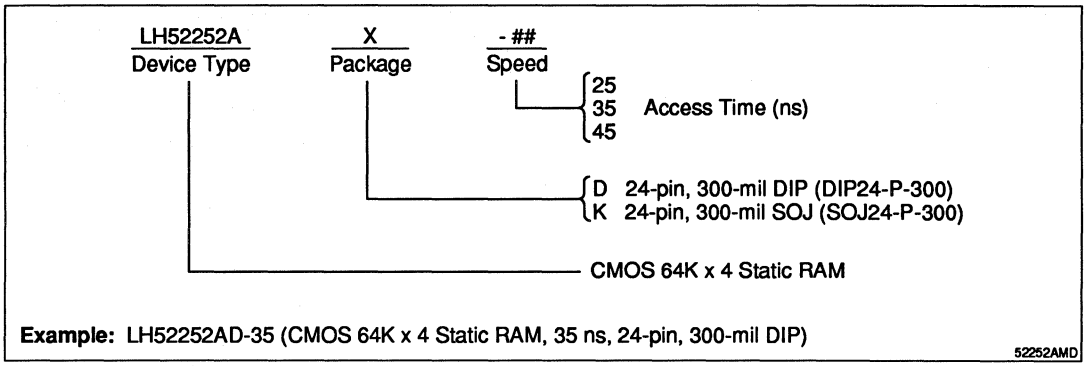


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52252B

ADVANCE INFORMATION

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 15/20/25 ns
- Standard 24-Pin, 300-mil DIP
- Space Saving 24-Pin, 300-mil SOJ
- JEDEC Standard Pinouts
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count

FUNCTIONAL DESCRIPTION

The LH52252B is a high-speed 262,144 bit static RAM organized as 64K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

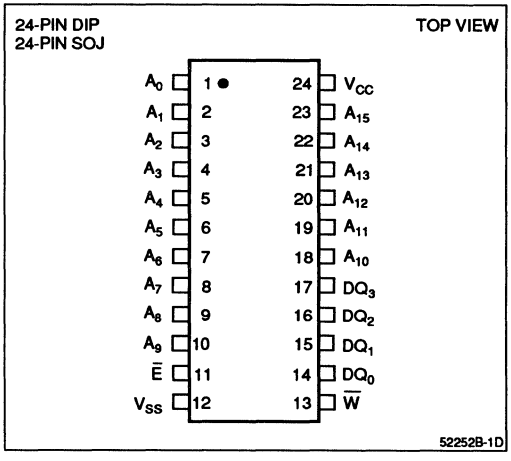


Figure 1. Pin Connections for DIP and SOJ Packages

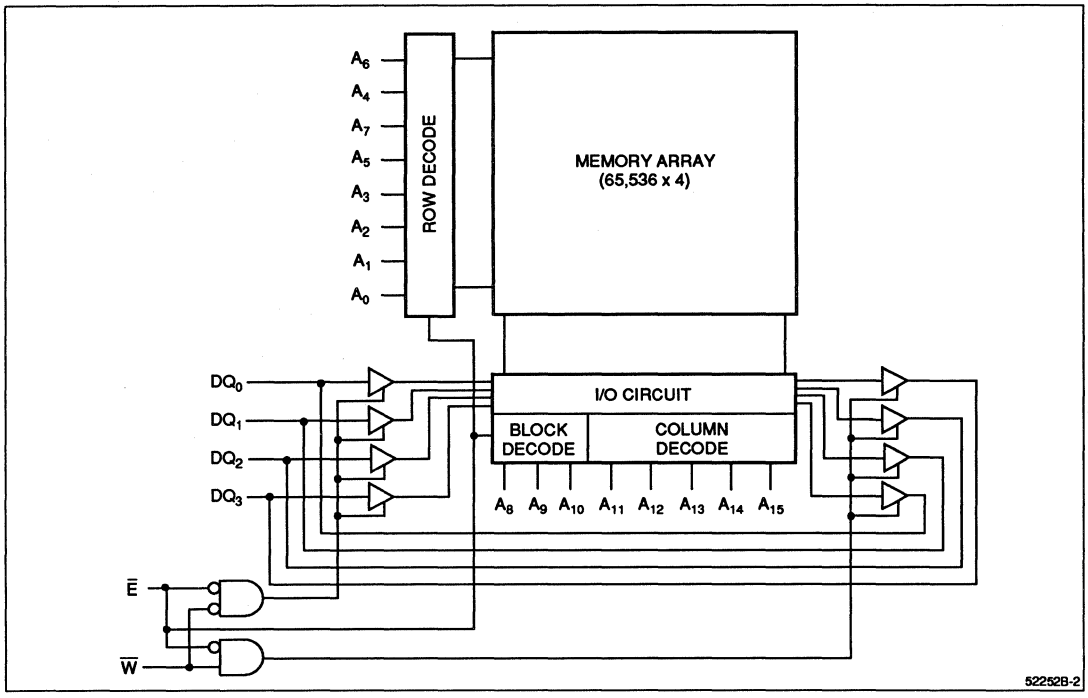


Figure 2. LH52252B Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	Not Selected	High-Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC}+0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 15 ns			165	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 20 ns			145	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 25 ns			135	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			10	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTES:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

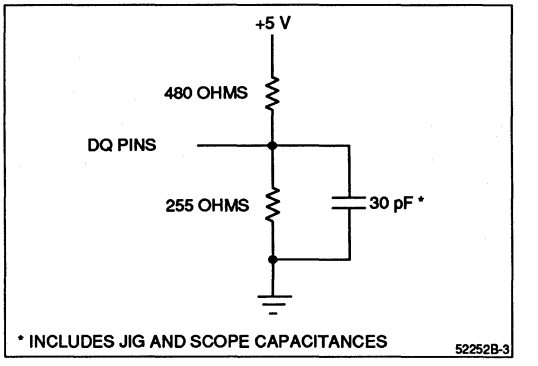


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-15		-20		-25		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	15		20		25		ns
t_{AA}	Address Access Time		15		20		25	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		15		20		25	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [3]	4		4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		8		10		12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		30	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	15		20		25		ns
t_{EW}	$\overline{E}$ Low to End of Write	12		15		20		ns
t_{AW}	Address Valid to End of Write	12		15		20		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	10		12		15		ns
t_{DW}	Input Data Setup Time	8		10		10		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		6		7		8	ns
t_{WLZ}	$\overline{W}$ High to Output Active [3]	4		4		4		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

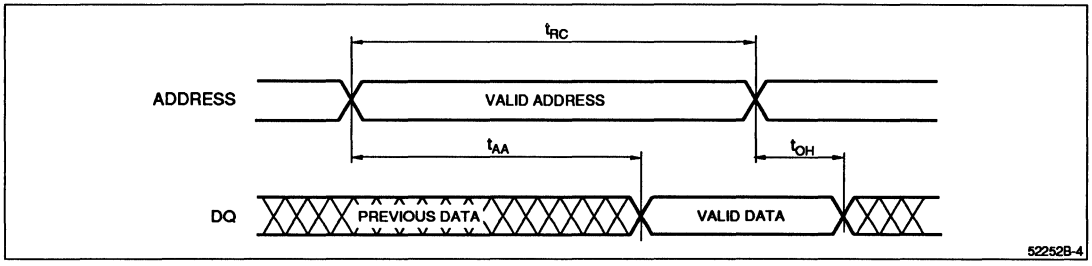


Figure 4. Read Cycle No. 1

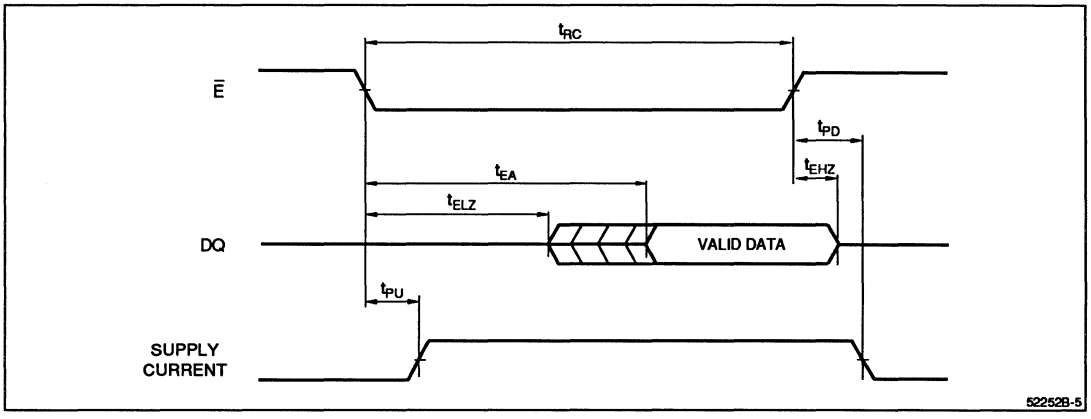


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

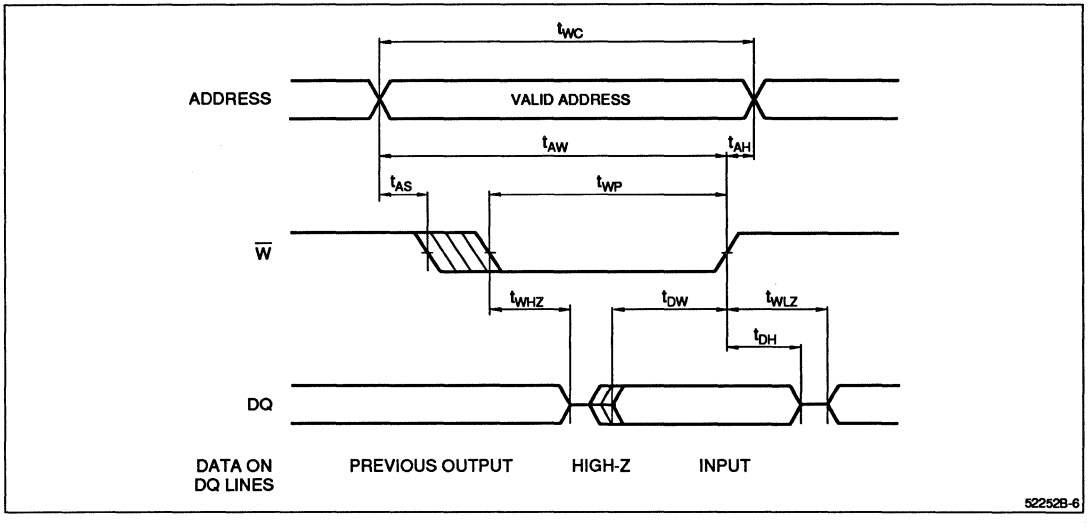


Figure 6. Write Cycle No. 1

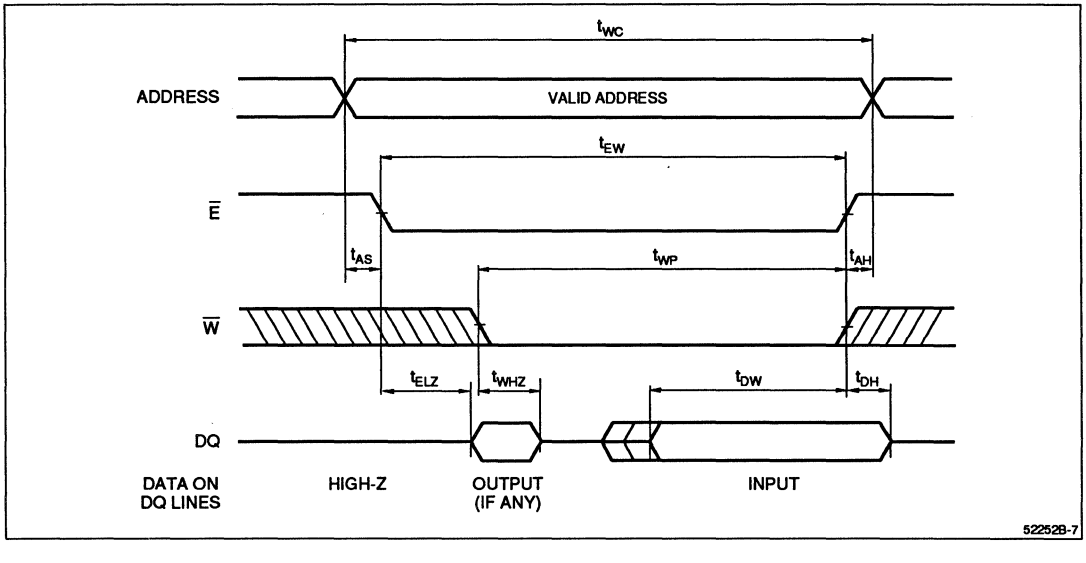
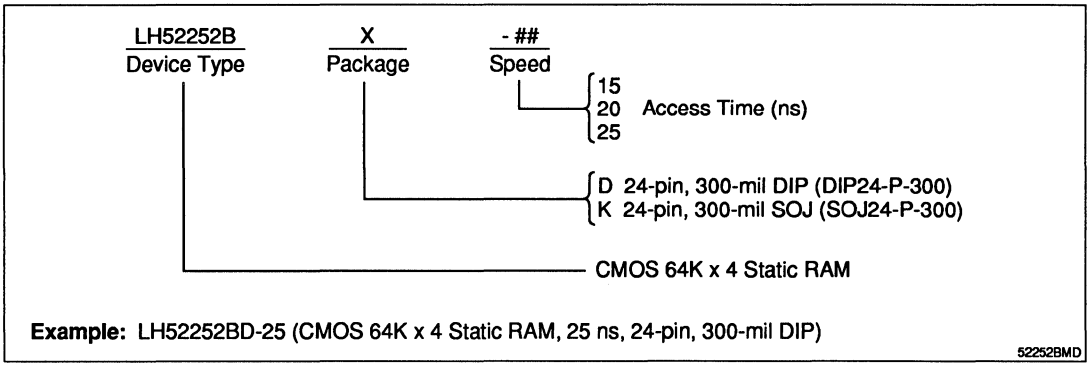


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52253

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 15 */20/25/35 ns
- Standard 28-Pin, 300-mil DIP
- Space Saving 28-Pin, 300-mil SOJ
- JEDEC Standard Pinouts
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count

FUNCTIONAL DESCRIPTION

The LH52253 is a very high-speed 256K-bit static RAM organized as 64K × 4. This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is inactive (HIGH). The combination of $\overline{E}$ and $\overline{W}$ control the mode of operation of the LH52253.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new read cycles can be performed by simply changing the address. An Automatic Power Down feature reduces the current consumption when Read and Write cycles extend beyond their minimum cycle times.

The LH52253 offers an Output Enable ($\overline{G}$) for use in managing the Data Bus. Bus contention during Write cycles may be easily avoided by using the $\overline{G}$ input in the LH52253.

High-frequency design techniques should be employed to obtain the best performance from these devices. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

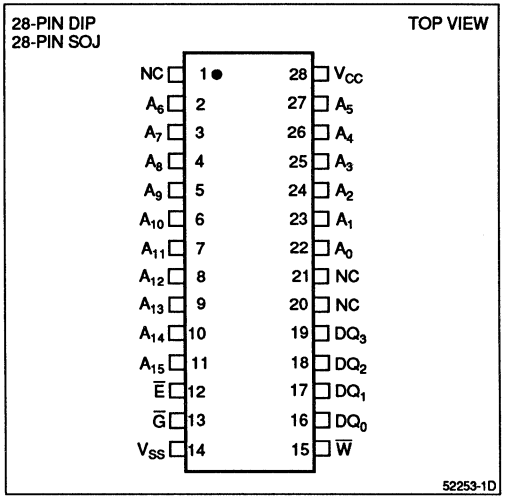


Figure 1. Pin Connections for DIP and SOJ

* Note: only the 15 ns access time part is Advance Information.

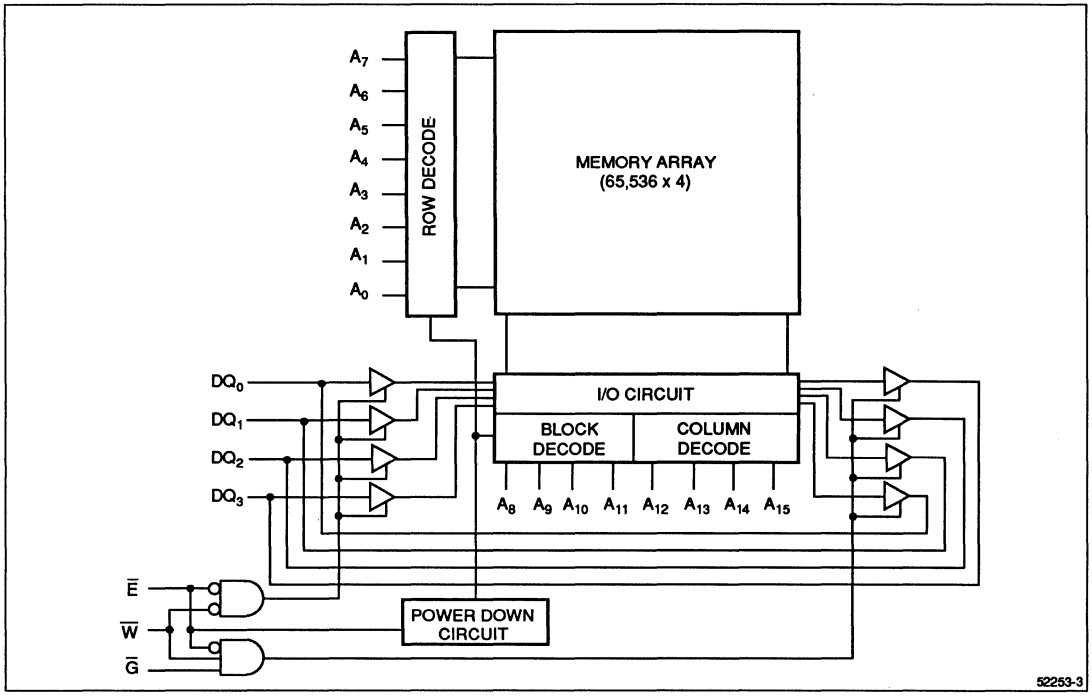


Figure 2. LH52253 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	L	Read	Data Out	Active
L	H	H	Read	High-Z	Active
L	L	X	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
$\overline{G}$	Output Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Function operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 15 ns [2] $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			165	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 20 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			145	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 25 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			135	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = 35 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			135	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V			1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min			10	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTES:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.
2. Note: only the 15 ns access time part is Advance Information.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{DQ} (Input/Output Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

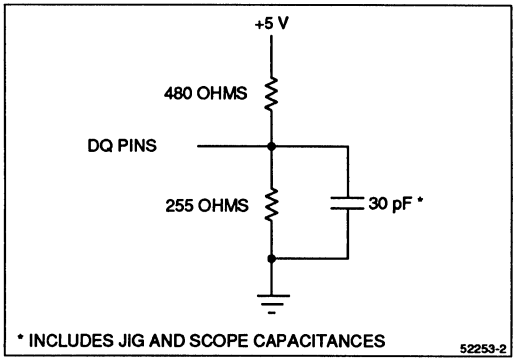


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-15 [4]		-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE									
t_{RC}	Read Cycle Timing	15		20		25		35		ns
t_{AA}	Address Access Time		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		15		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		8		10		10		12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		12		15	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	7	0	9	0	10	0	12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		30		35	ns
	WRITE CYCLE									
t_{WC}	Write Cycle Time	15		20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	12		15		20		25		ns
t_{AW}	Address Valid to End of Write	12		15		20		25		ns
t_{AS}	Address Setup	0		0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	10		12		15		20		ns
t_{DW}	Input Data Setup Time	8		10		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		0		ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	4		4		4		4		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		6		7		8		10	ns

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Guaranteed but not tested.
4. Note: only the 15 ns access time part is Advance Information.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in the Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid when $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Valid Data will be present following t_{GA} only if t_{EA} timing has been met.

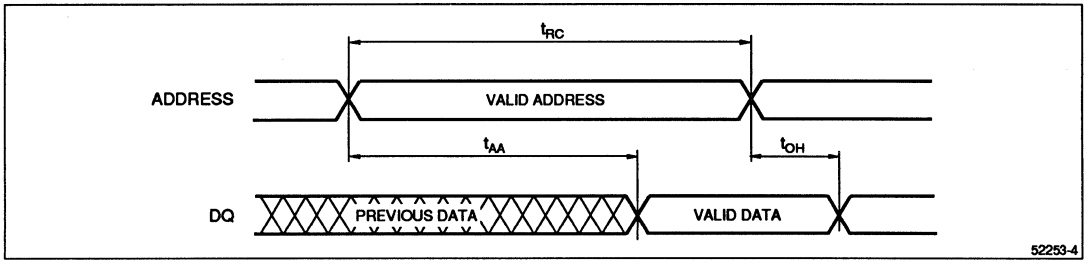


Figure 4. Read Cycle No. 1

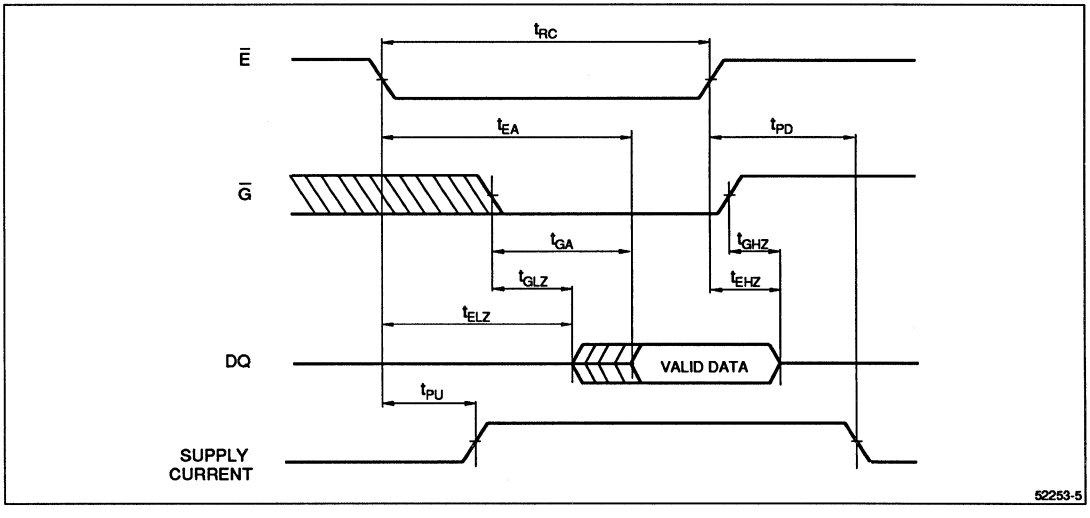


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise. These timing diagrams assume $\overline{G}$ is LOW, but it should be kept HIGH during Write cycles to insure that the output drivers are disabled.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

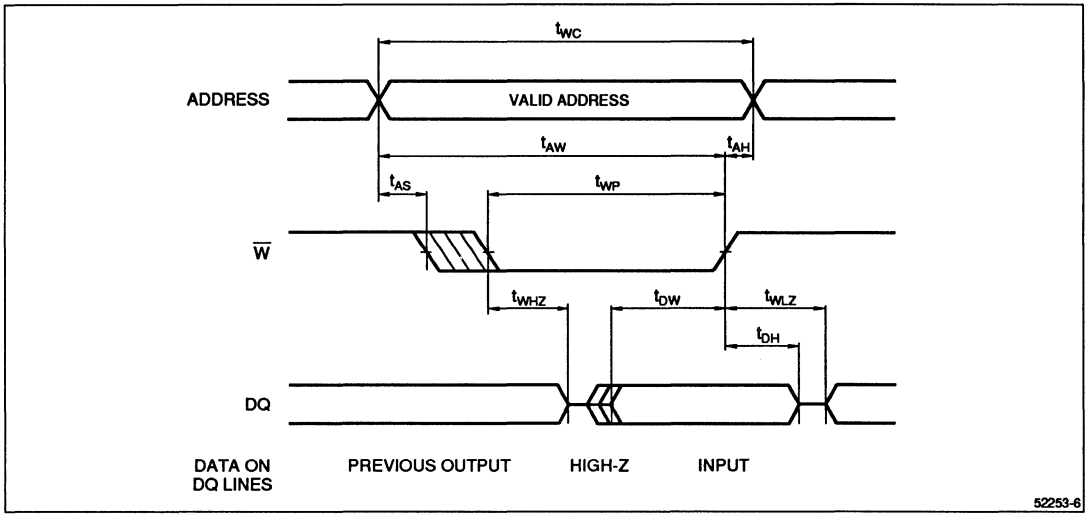


Figure 6. Write Cycle No. 1

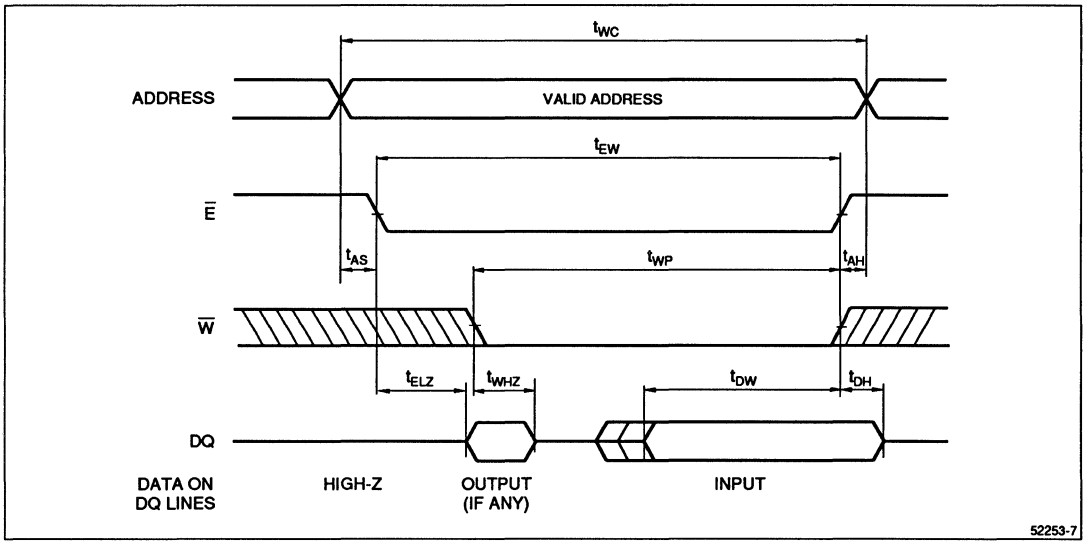
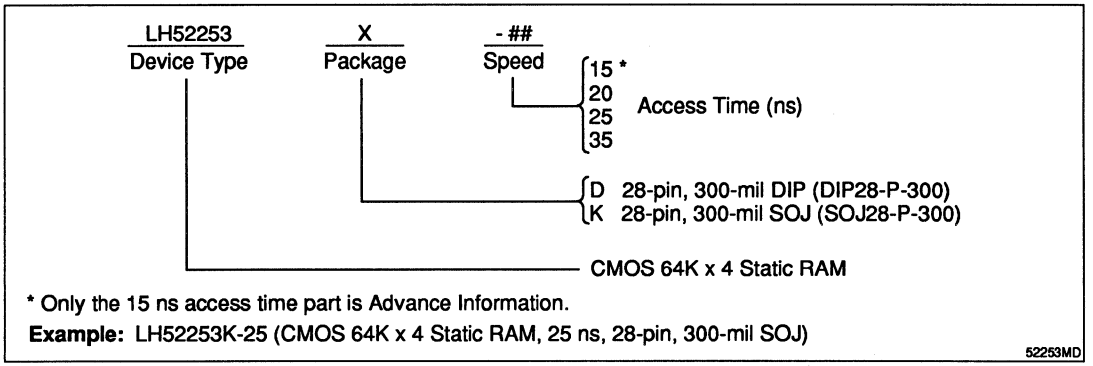


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



* Only the 15 ns access time part is Advance Information.

Example: LH52253K-25 (CMOS 64K x 4 Static RAM, 25 ns, 28-pin, 300-mil SOJ)

52253MD

LH52256
LH52256L

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  70/90/120 ns (MAX.)
- Low power consumption:
  Operating: 440/385/385 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH52256 is a low-power CMOS-periphery static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

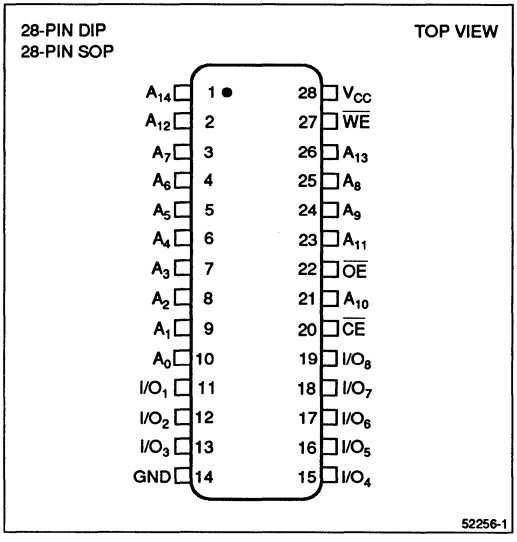


Figure 1. Pin Connections for DIP and SOP Packages

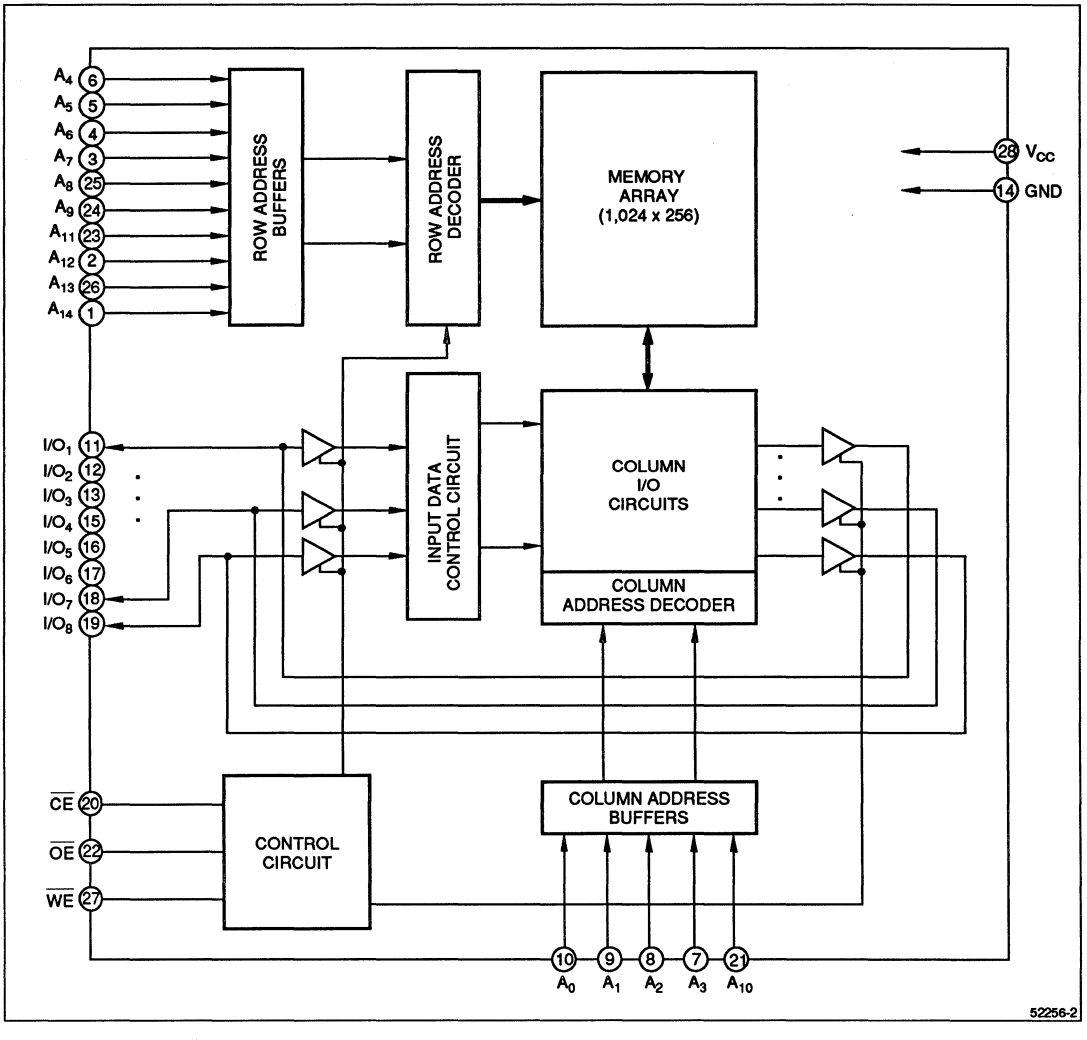


Figure 2. LH52256/LH52256L Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address inputs
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	
L	L	X	Write	D_{IN}	Operating (I_{CC})	1

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	3.5	V_{CC} + 0.3	V
	V_{IL}	-0.3		+0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	LH52256L-70 LH52256N-70L			LH52256L-90,-12 LH52256N-90L,-12L			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V_{IN} = 0 to V_{CC}			1			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			80			70	mA
	I_{CC1}	V_{IH} = 3.5 V, V_{IL} = 0.6 V Outputs open			70			65	mA
	I_{CC2}	V_{IH} = 2.2 V, V_{IL} = 0.8 V Outputs open			80			70	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3			3	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2			0.1			0.1	mA
Output voltage	V_{OL}	I_{OL} = 2 mA			0.4			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH52256L-70 LH52256N-70L		LH52256L-90 LH52256N-90L		LH52256L-12 LH52256N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		90		120		ns	
Address access time	t_{AA}		70		90		120	ns	
Chip enable access time	t_{ACE}		70		90		120	ns	
Output enable access time	t_{OE}		40		50		60	ns	
Output hold from address change	t_{OH}	10		10		10		ns	1
Chip enable Low to output in Low-Z	t_{LZ}	5		5		5		ns	1
Output enable Low to output in Low-Z	t_{OLZ}	5		5		5		ns	1
Chip disable to output in High-Z	t_{HZ}	0	35	0	40	0	45	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	35	0	40	0	45	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH52256L-70 LH52256N-70L		LH52256L-90 LH52256N-90L		LH52256L-12 LH52256N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		90		120		ns	
Chip enable to end of write	t_{CW}	45		55		65		ns	
Address valid to end of write	t_{AW}	65		80		90		ns	
Address setup time	t_{AS}	0		0		10		ns	
Write pulse width	t_{WP}	45		55		65		ns	
Write recovery time	t_{WR}	5		5		10		ns	
Data valid to end of write	t_{DW}	30		30		35		ns	
Data hold time	t_{DH}	0		0		10		ns	
Output active from end of write	t_{OW}	5		5		5		ns	1
Write Low to output in High-Z	t_{WZ}	0	40	0	40	0	45	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	35	0	40	0	45	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 3.0 V		6	50	µA
Chip disable to data retention	t_{CDR}		0			ns
Recovery time	t_R		t_{RC}*			ns

* t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V	8	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	10	pF

NOTE:
1. This parameter is sampled and not production tested.

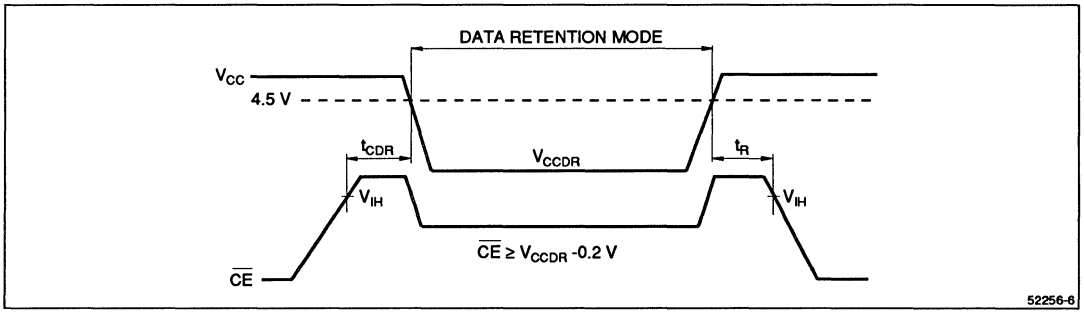


Figure 3. Low Voltage Data Retention

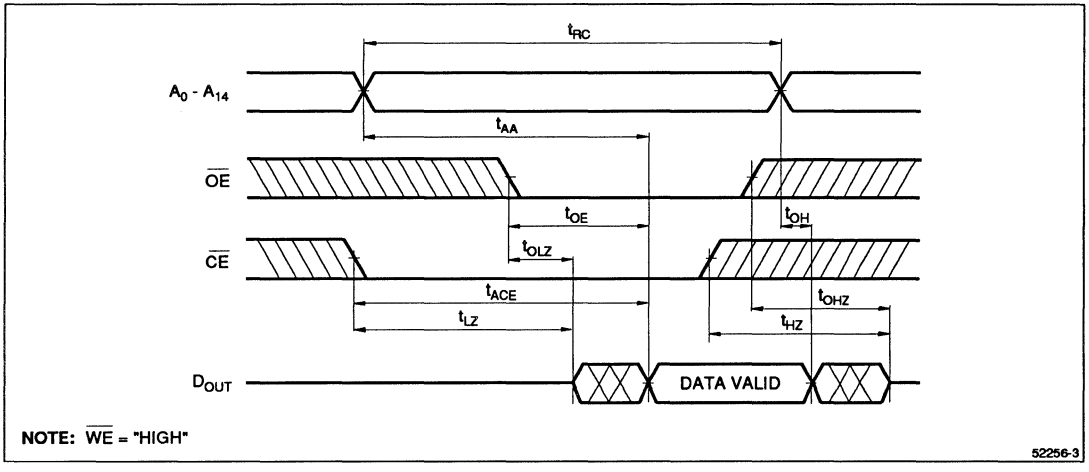
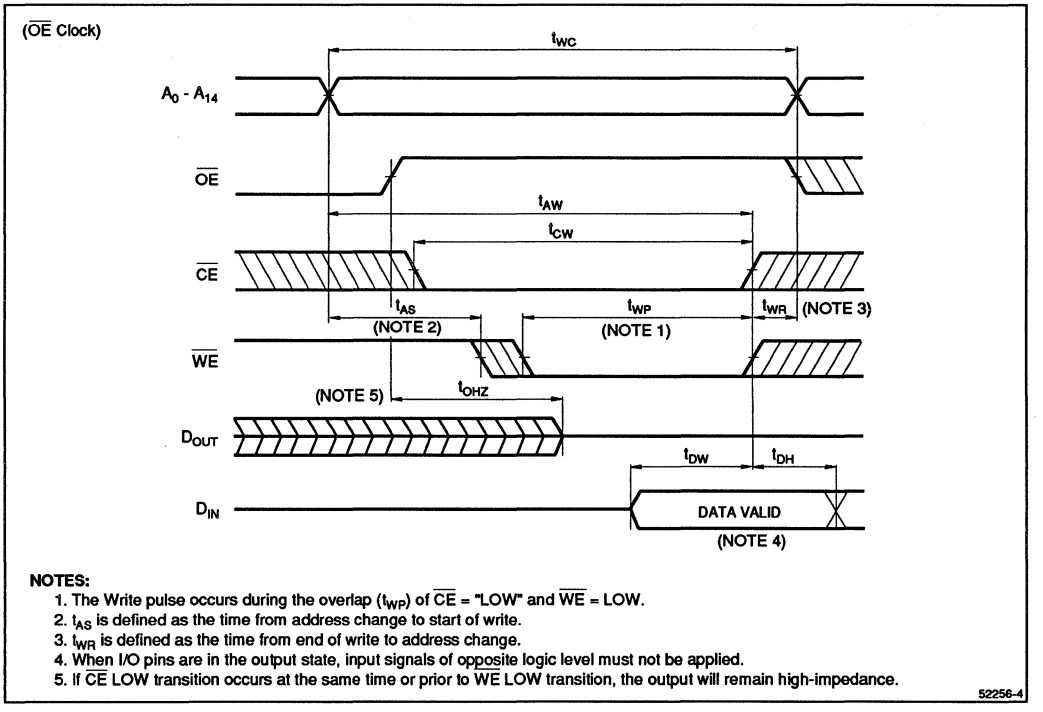


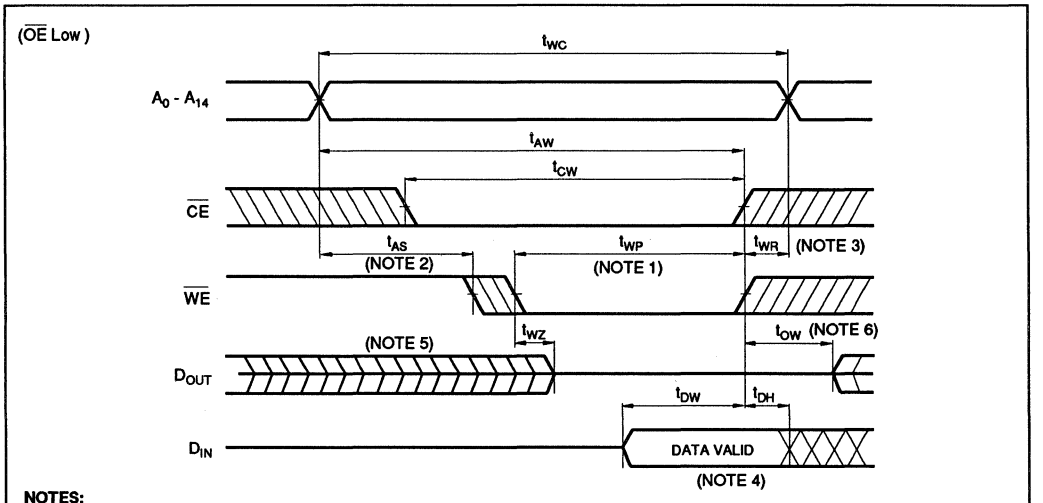
Figure 4. Read Cycle



NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = "LOW" and $\overline{WE}$ = LOW.
2. t_{AS} is defined as the time from address change to start of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in the output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.

52256-4

Figure 5. Write Cycle 1

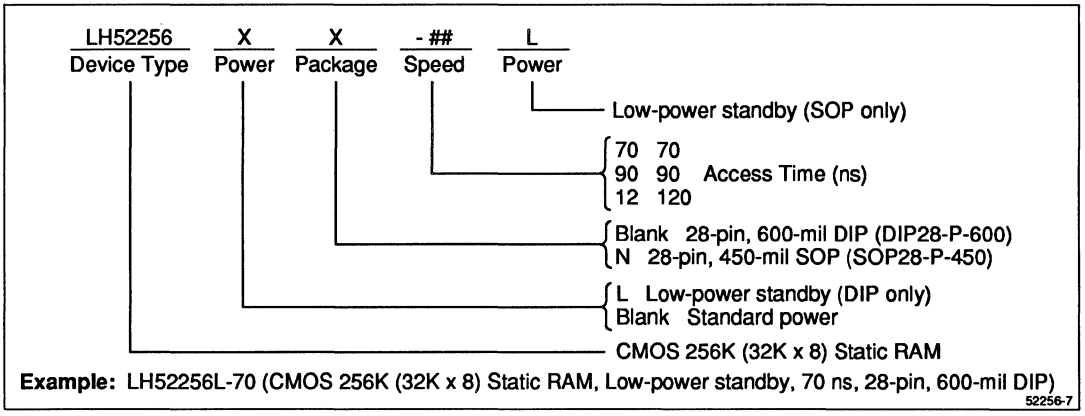


NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = "LOW" and $\overline{WE}$ = LOW.
2. t_{AS} is defined as the time from address to change to start of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in the output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

52256-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



LH52256LL

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time:
  90 ns (MAX.)
- Low power consumption:
  Operating: 385 mW (MAX.)
  Standby: 220 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH52256LL is an ultra-low power CMOS-periphery static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

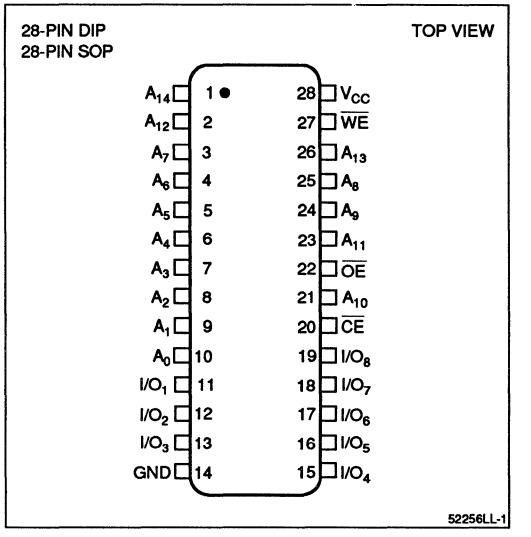


Figure 1. Pin Connections for DIP and SOP Packages

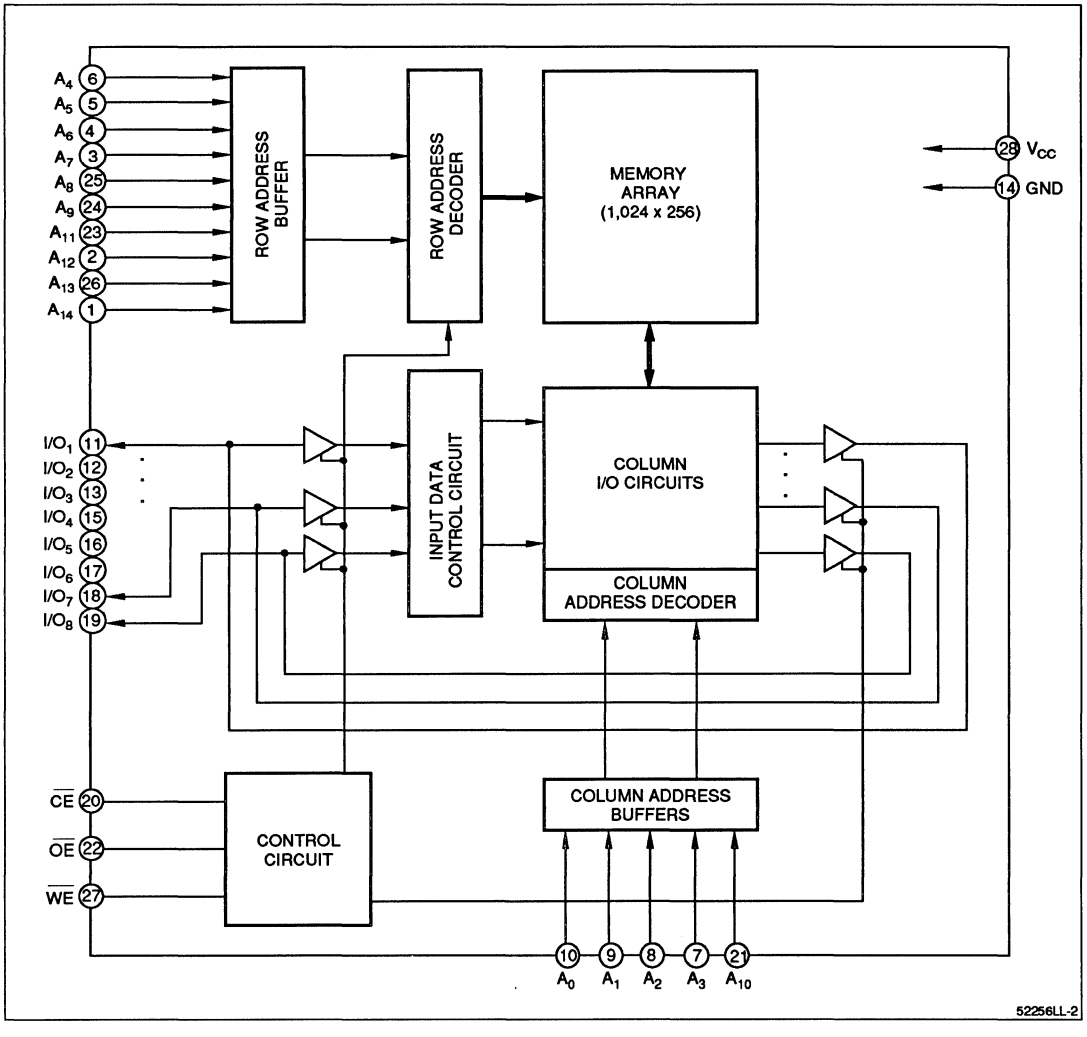


Figure 2. LH52256LL Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address inputs
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	
L	L	X	Write	D_{IN}	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	3.5	V_{CC} + 0.3	V
	V_{IL}	-0.3		+0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			70	mA
	I_{CC1}	V_{IH} = 3.5 V, V_{IL} = 0.6 V Outputs open			65	mA
	I_{CC2}	V_{IH} = 2.2 V, V_{IL} = 0.8 V Outputs open			70	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V		2	40	µA
Output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	90		ns	
Address access time	t_{AA}		90	ns	
Chip enable access time	t_{ACE}		90	ns	
Output enable access time	t_{OE}		50	ns	
Output hold from address change	t_{OH}	10		ns	
Chip enable Low to output in Low-Z	t_{LZ}	5		ns	1
Output enable Low to output in Low-Z	t_{OLZ}	5		ns	1
Chip disable to output in High-Z	t_{HZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	90		ns	
Chip enable to end of write	t_{CW}	55		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	55		ns	
Write recovery time	t_{WR}	5		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	5		ns	1
Write Low to output in High-Z	t_{WZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	1.0 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V		2.0			V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 3.0 V	T_A = 25°C			1	µA
			T_A = 0 to 40°C			3	
			T_A = 0 to 70°C			20	
Chip disable to data retention	t_{CDR}			0			ns
Recovery time	t_R			t_{RC}*			ns

* t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		8	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		10	pF

NOTE:
1. This parameter is sampled and not production tested.

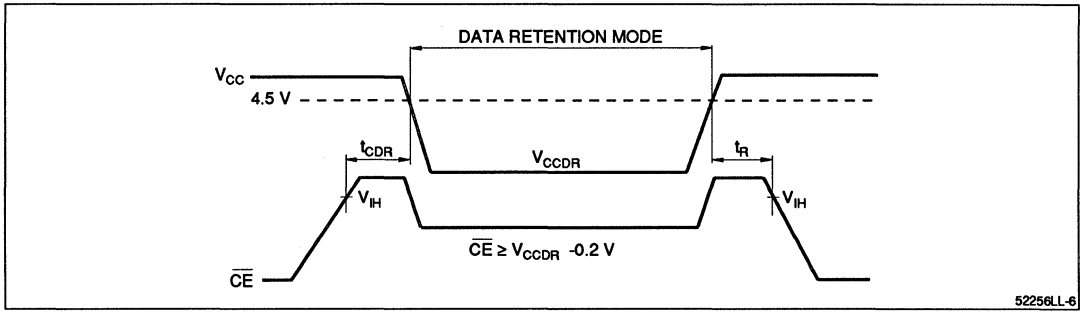


Figure 3. Low Voltage Data Retention

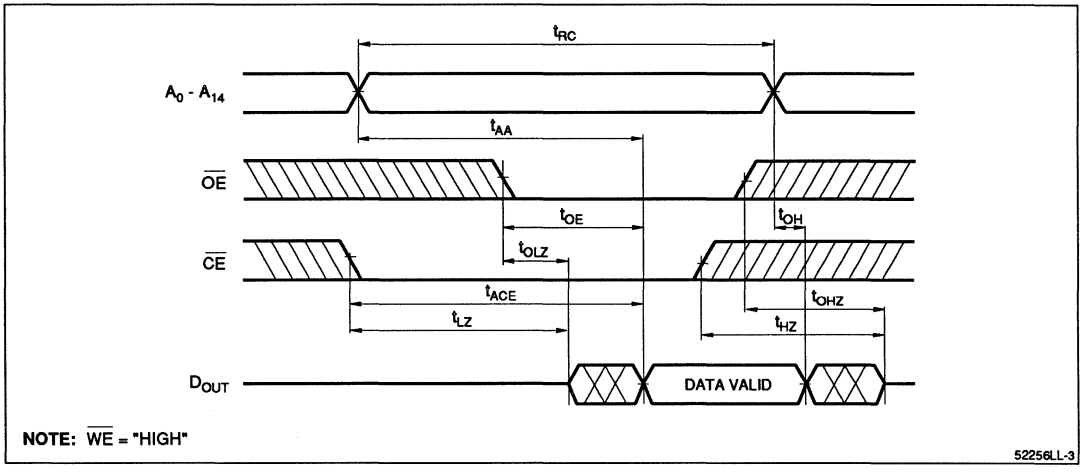
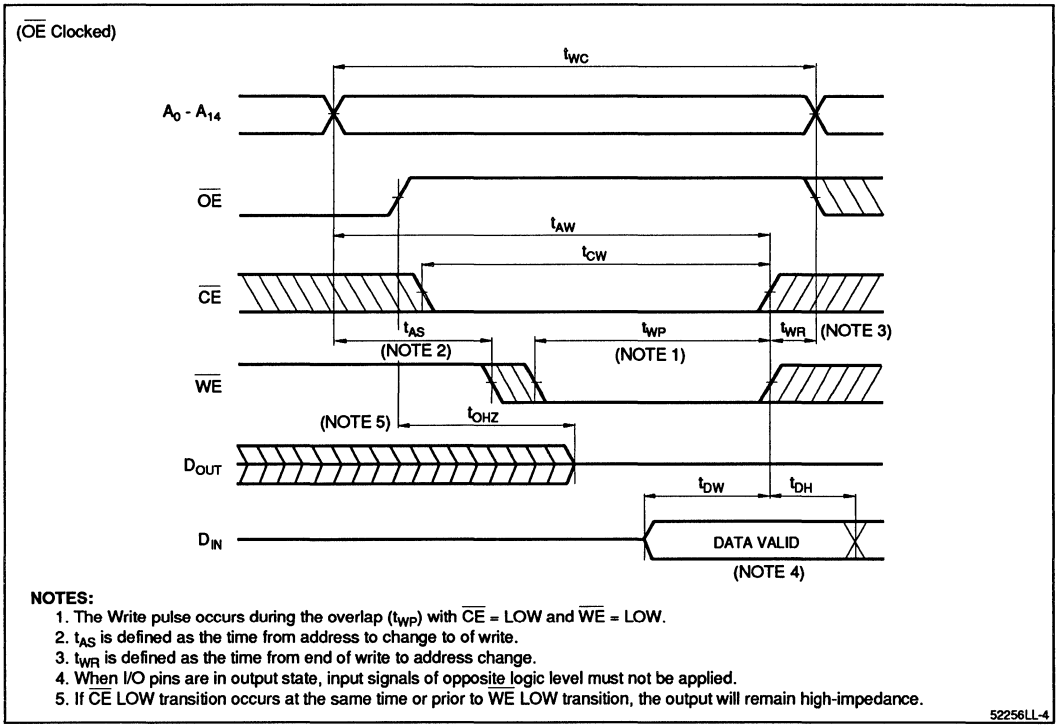


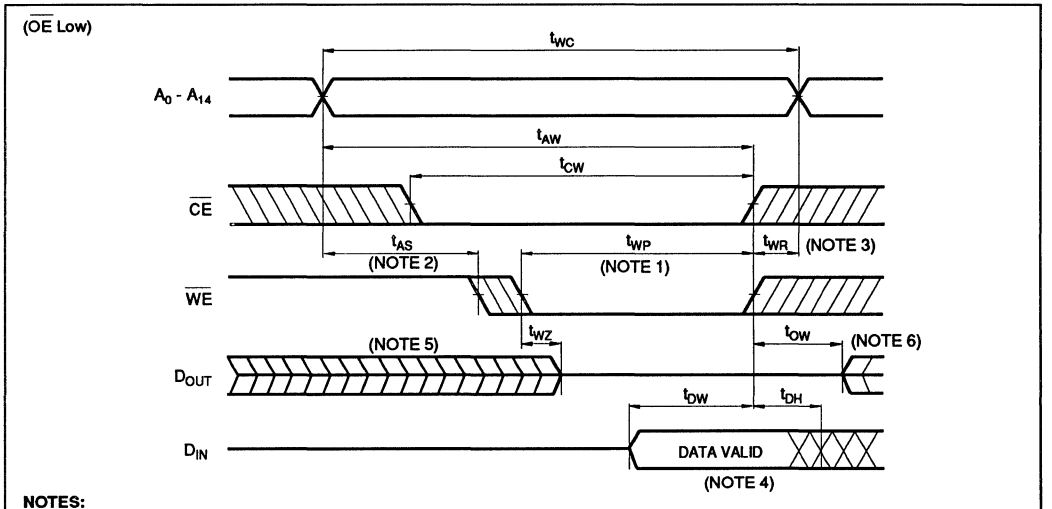
Figure 4. Read Cycle



NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) with $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{AS} is defined as the time from address to change to of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.

52256LL-4

Figure 5. Write Cycle 1

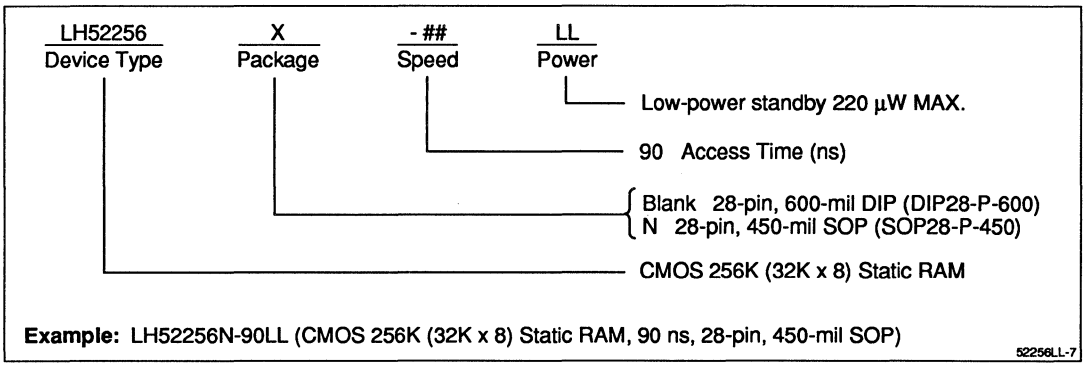


NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) with $\overline{CE}$ = LOW and $\overline{WE}$ = Low.
2. t_{AS} is defined as the time from address to change to of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

52256LL-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH52256N-90LL (CMOS 256K (32K x 8) Static RAM, 90 ns, 28-pin, 450-mil SOP)

52256LL-7

LH52258

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 30/35/45/55 ns
- Space Saving 28-Pin, 300-mil DIP
- High Density 28-Pin, 300-mil SOJ
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH52258 is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. Proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

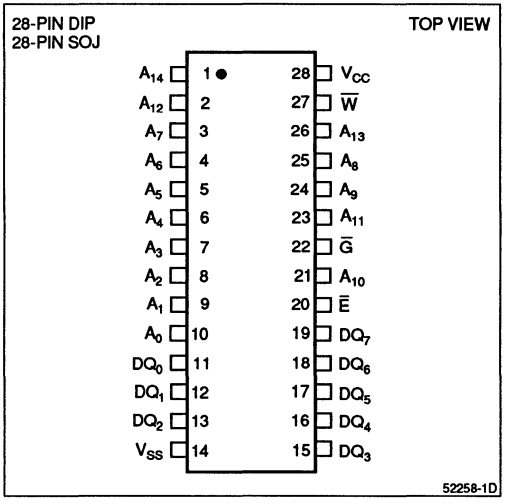


Figure 1. Pin Connections for DIP and SOJ Packages

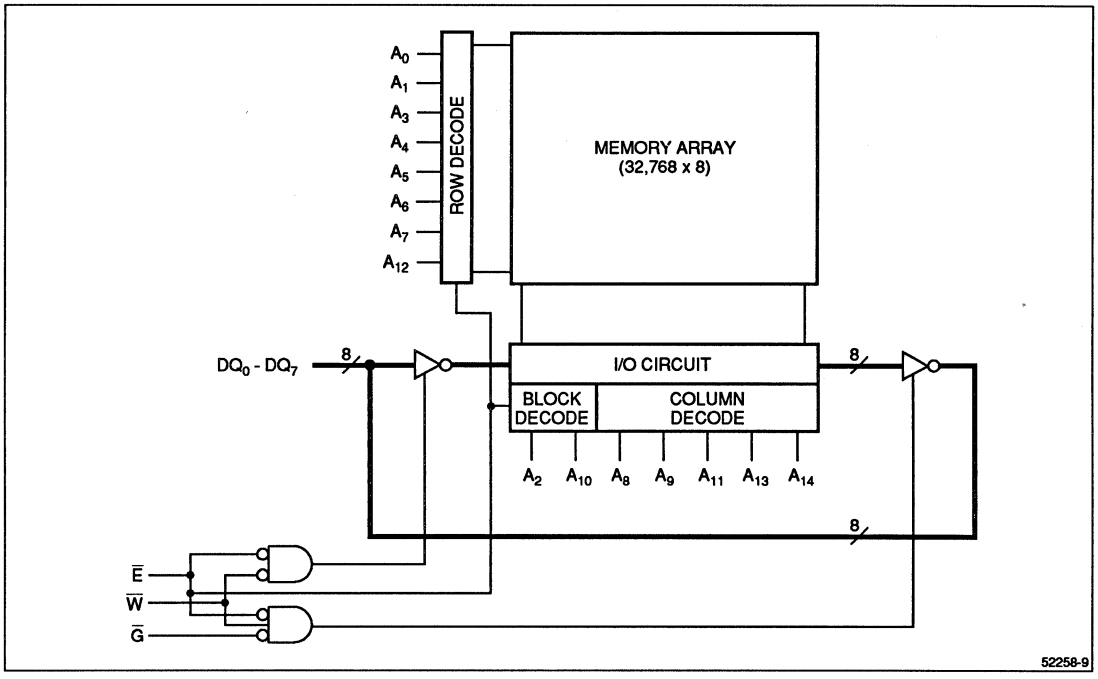


Figure 2. LH52258 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 30 ns			185	mA
I_{CC1}	Operating Current [1]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 35 ns			170	mA
I_{CC1}	Operating Current [1]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 45 ns			155	mA
I_{CC1}	Operating Current [1]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 55 ns			155	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			5	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			200	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

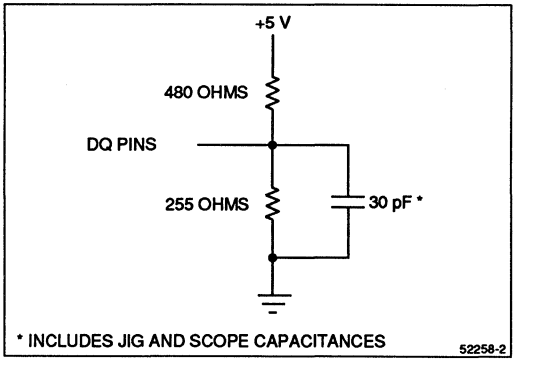


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

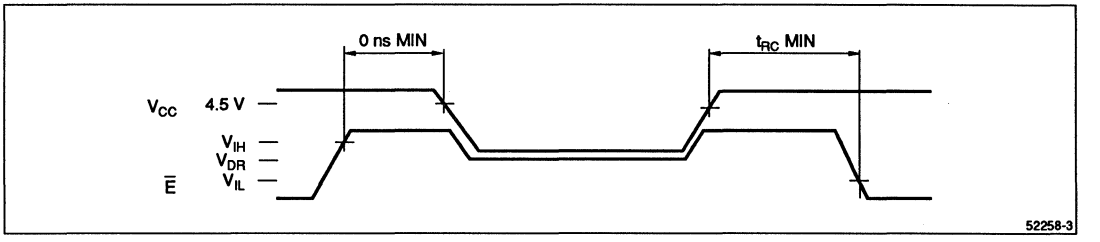


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-30		-35		-45		-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle Time	30		35		45		55		ns
t_{AA}	Address Access Time		30		35		45		55	ns
t_{OH}	Output Hold from Address Change	5		5		5		5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		30		35		45		55	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		15		20		25	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		15		20		25	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	3		3		3		3		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		10		15		20		25	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		30		35		45		55	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	30		35		45		55		ns
t_{EW}	$\overline{E}$ Low to End of Write	25		30		40		50		ns
t_{AW}	Address Valid to End of Write	25		30		40		50		ns
t_{AS}	Address Setup	0		0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		20		25		25		ns
t_{DW}	Input Data Setup Time	13		15		20		25		ns
t_{DH}	Input Data Hold Time	0		0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		13		15		15		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

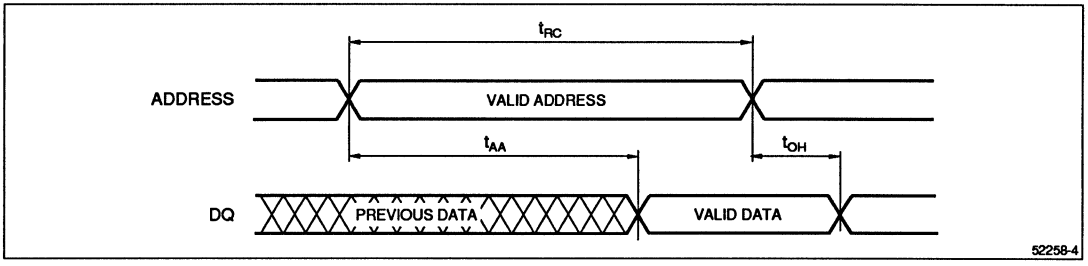


Figure 5. Read Cycle No. 1

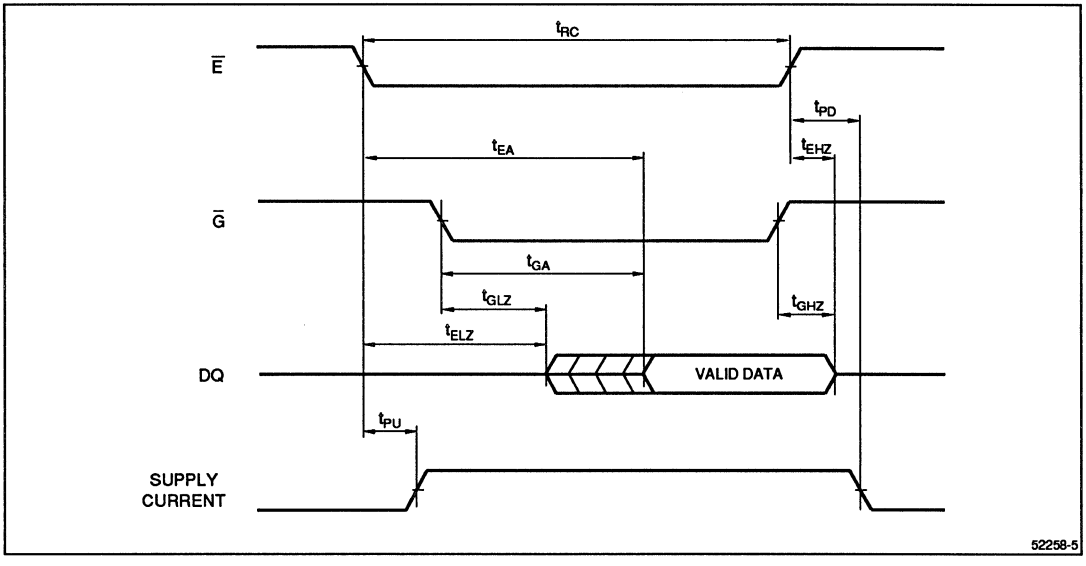


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

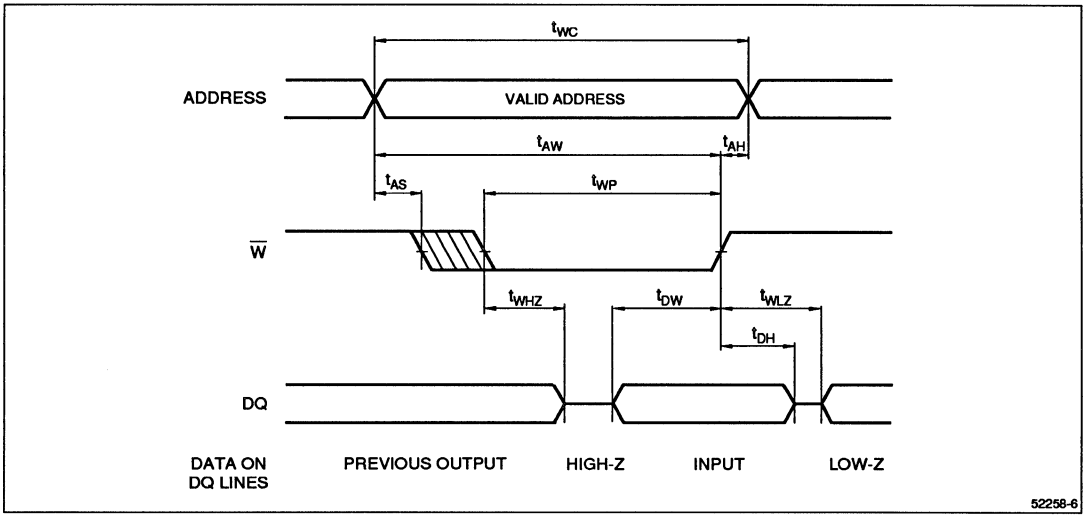


Figure 7. Write Cycle No. 1

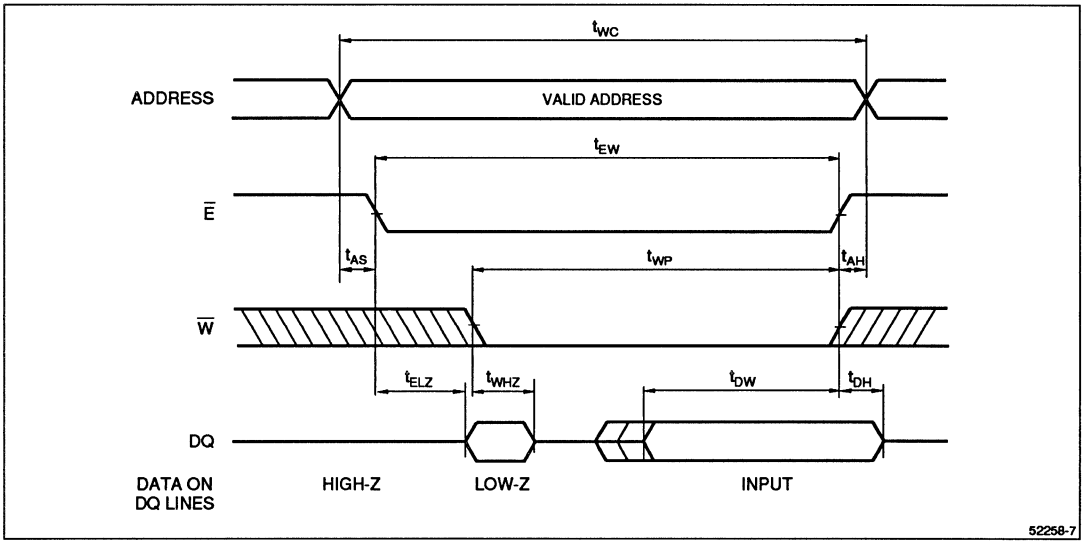
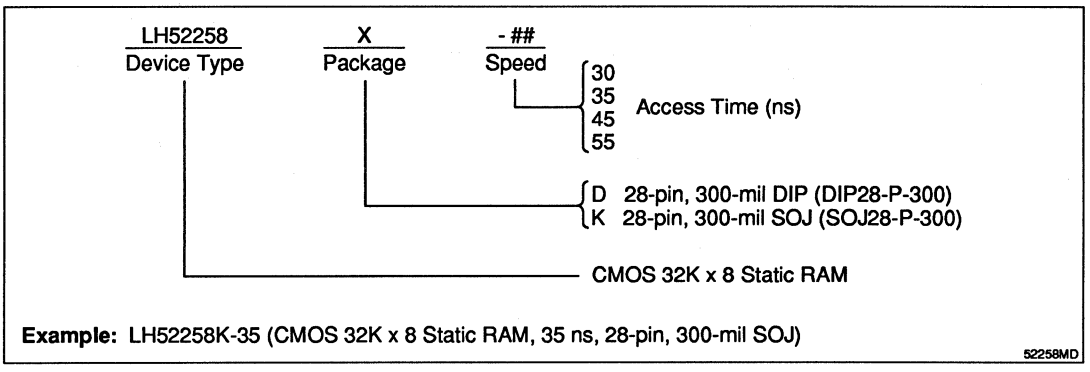


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH52258A

PRELIMINARY

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 15 */20/25/30 ns
- JEDEC Standard Pinout
- Space Saving 28-Pin, 300-mil DIP
- High Density 28-Pin, 300-mil SOJ
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation

FUNCTIONAL DESCRIPTION

The LH52258A is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

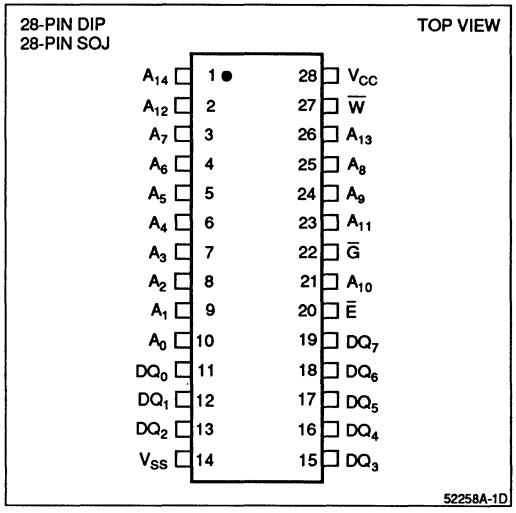


Figure 1. Pin Connections for DIP and SOJ Packages

* Note: only the 15 ns access time part is Advance Information.

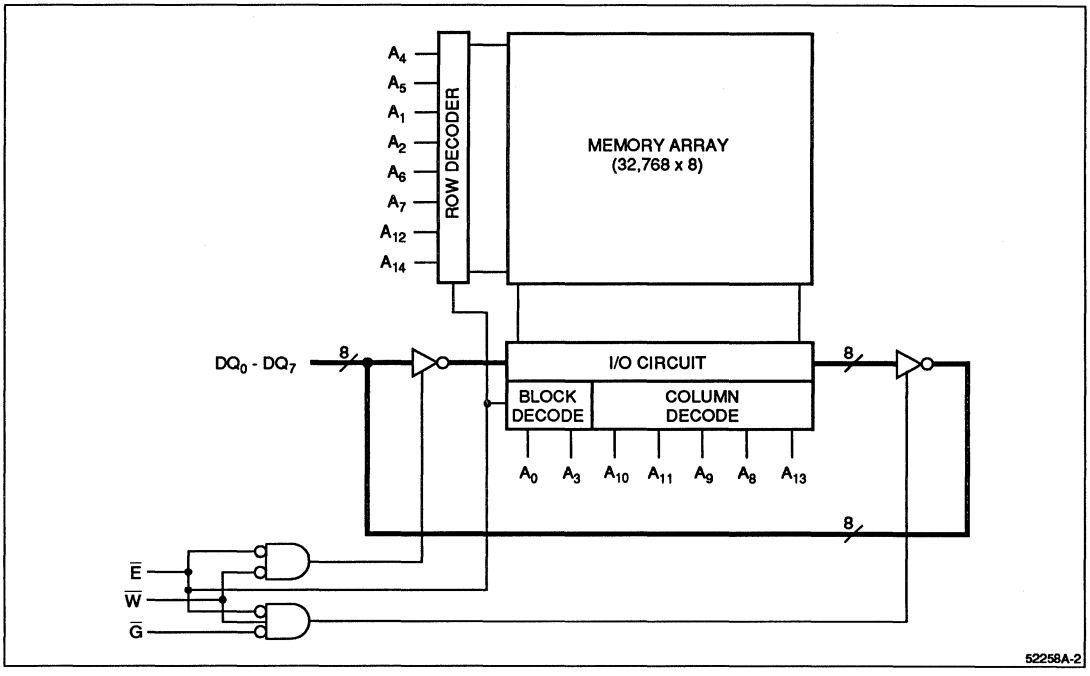


Figure 2. LH52258A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
Vcc	Positive Power Supply
Vss	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{RC} = 15 ns [2] $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 15 ns			165	mA
I_{CC1}	Operating Current [1]	t_{RC} = 20 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 20 ns			150	mA
I_{CC1}	Operating Current [1]	t_{RC} = 25 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 25 ns			140	mA
I_{CC1}	Operating Current [1]	t_{RC} = 30 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 30 ns			130	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$ − 0.2 V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			15	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 m A			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC}$ − 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC}$ − 0.2 V			200	µA

NOTES:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.
2. Note: only the 15 ns access time part is Advance Information.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

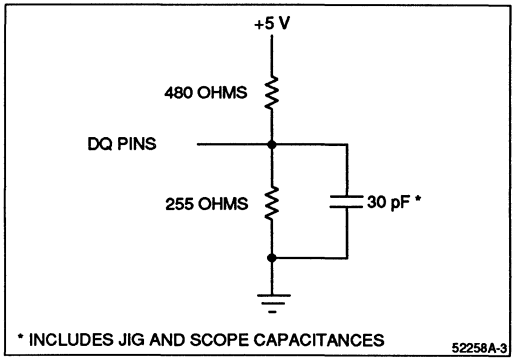


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

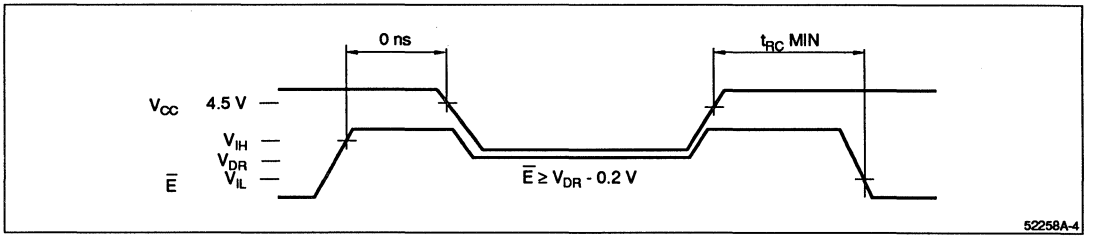


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-15 [4]		-20		-25		-30		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle Time	15		20		25		30		ns
t_{AA}	Address Access Time		15		20		25		30	ns
t_{OH}	Output Hold from Address Change	4		4		4		5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		15		20		25		30	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		4		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	8	0	10	0	12		12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		12		12	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		3		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	7	0	9	0	10		10	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		30		30	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	15		20		25		30		ns
t_{EW}	$\overline{E}$ Low to End of Write	12		15		20		25		ns
t_{AW}	Address Valid to End of Write	12		15		20		25		ns
t_{AS}	Address Setup	0		0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	10		12		15		20		ns
t_{DW}	Input Data Setup Time	8		10		12		13		ns
t_{DH}	Input Data Hold Time	0		0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		6		8		10		13	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. The test load has 5 pF capacitances.
3. Guaranteed by design but not tested.
4. Note: only the 15 ns access time part is Advance Information.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

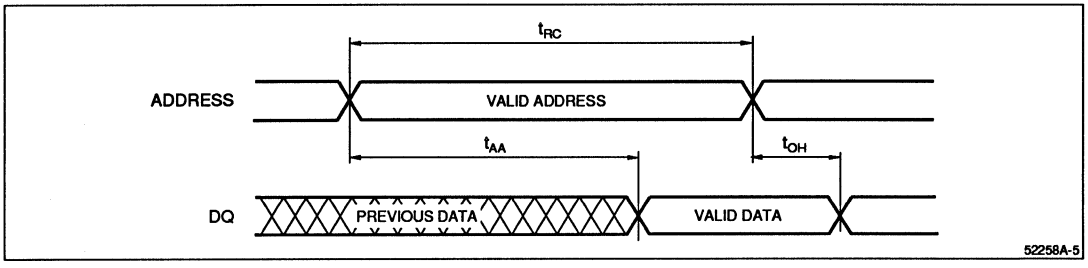


Figure 5. Read Cycle No. 1

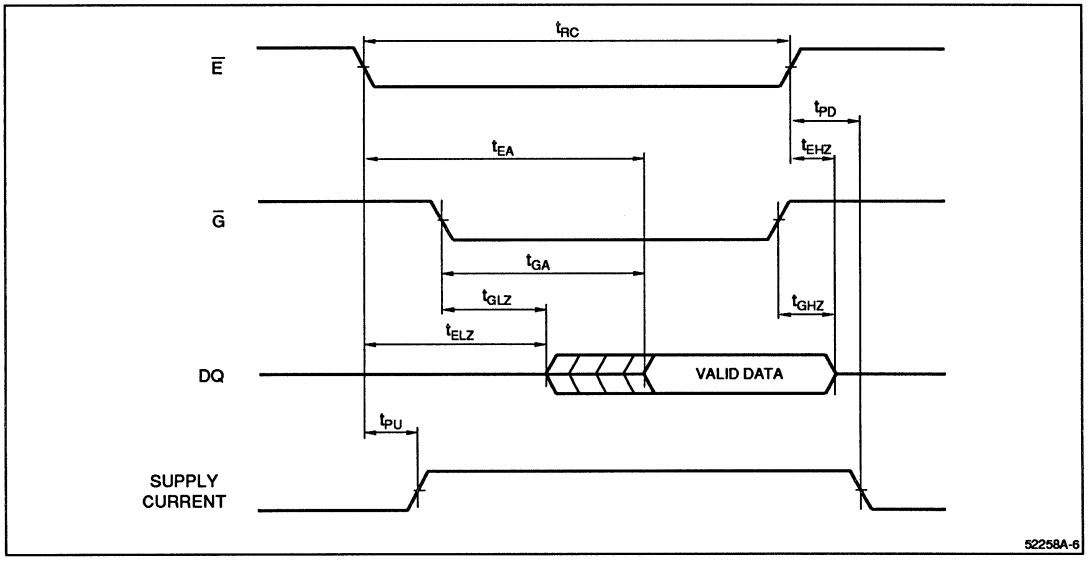


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258A's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

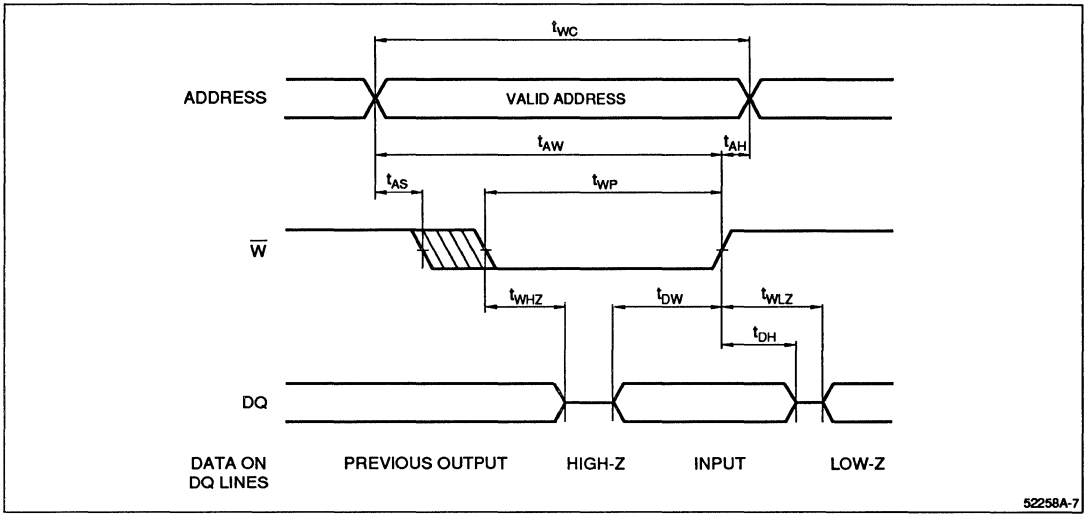


Figure 7. Write Cycle No. 1

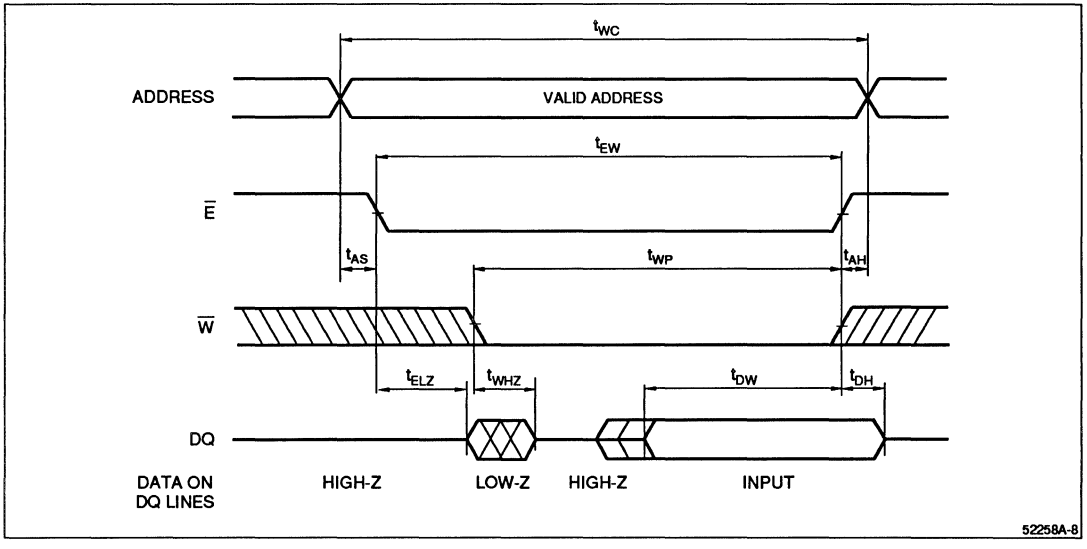
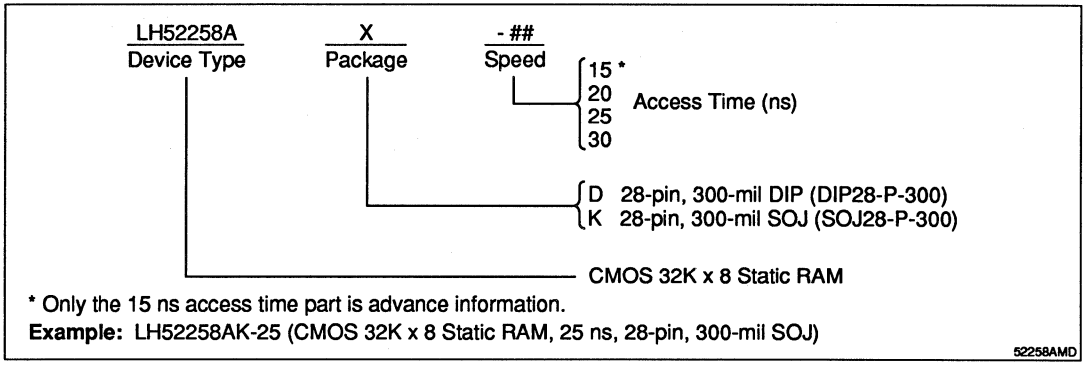


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521002

CMOS 256K × 4 Static RAM

FEATURES

- Fast Access Times: 20 */25/35 ns
- High Density 28-Pin, 400-mil SOJ
- JEDEC Standard Pinouts
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH521002 is a high speed 1,048,576-bit static RAM organized as 256K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 18 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

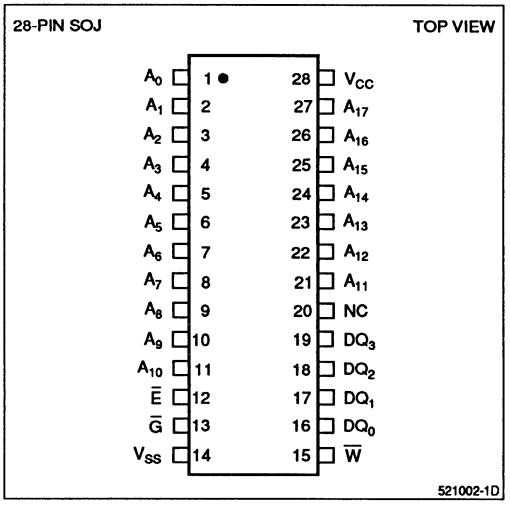


Figure 1. Pin Connections for SOJ Package

* Note: only the 20 ns access time part is Advance Information.

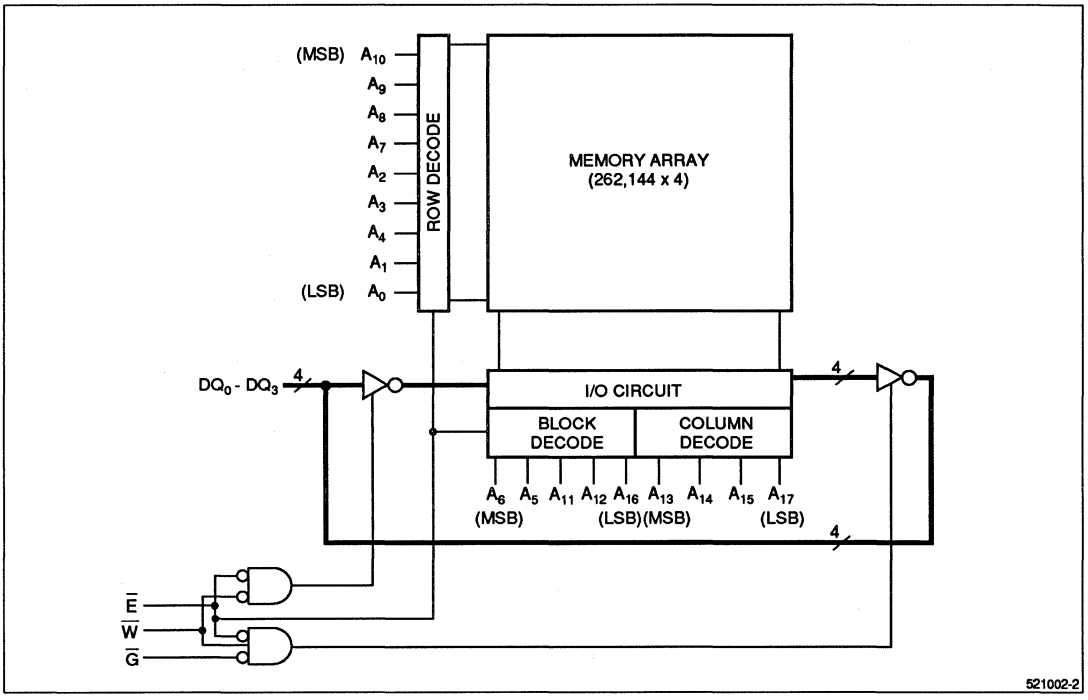


Figure 2. LH521002 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
$\overline{G}$	Output Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1,2]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage [2]	2.2		V_{CC} + 0.5	V

NOTES:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.
2. See Applications Note "Input/Output Level Testing" for test considerations.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = 20 ns [2] $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			180	mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 25 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			180	mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 35 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			150	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.4	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			500	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
2. Note: only the 20 ns access time part is Advance Information.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

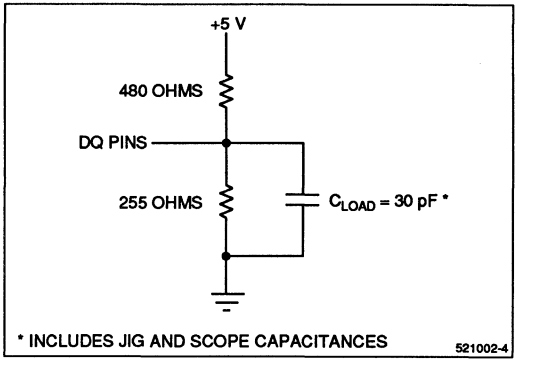


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. This parameter is sampled and not production tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

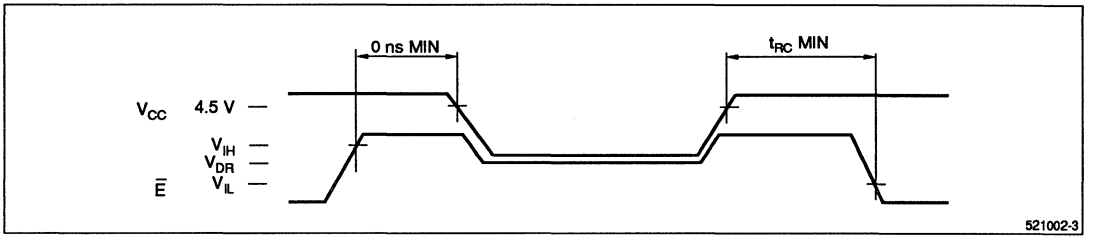


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.
4. Note: only the 20 ns access time part is Advance Information.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following an Address transition, Data Out is guaranteed valid at t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data Out. Data Out is valid after both t_{EA} and t_{GA} are met.

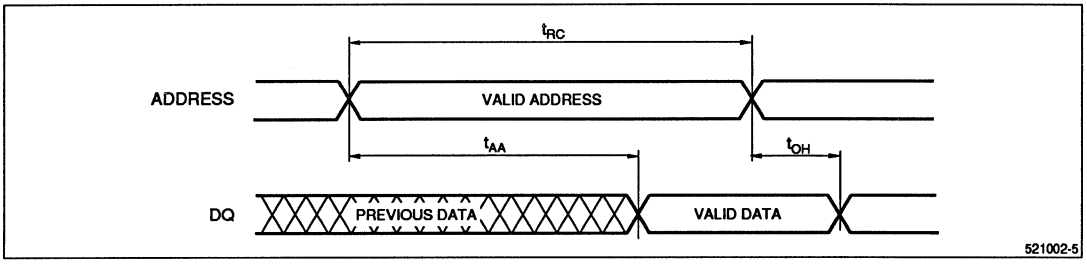


Figure 5. Read Cycle No. 1

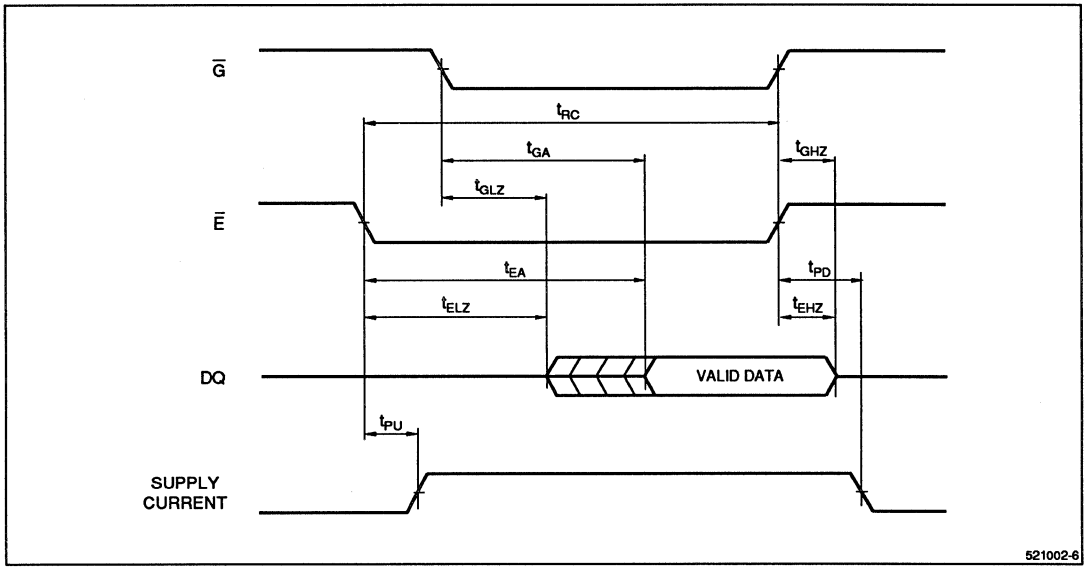


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

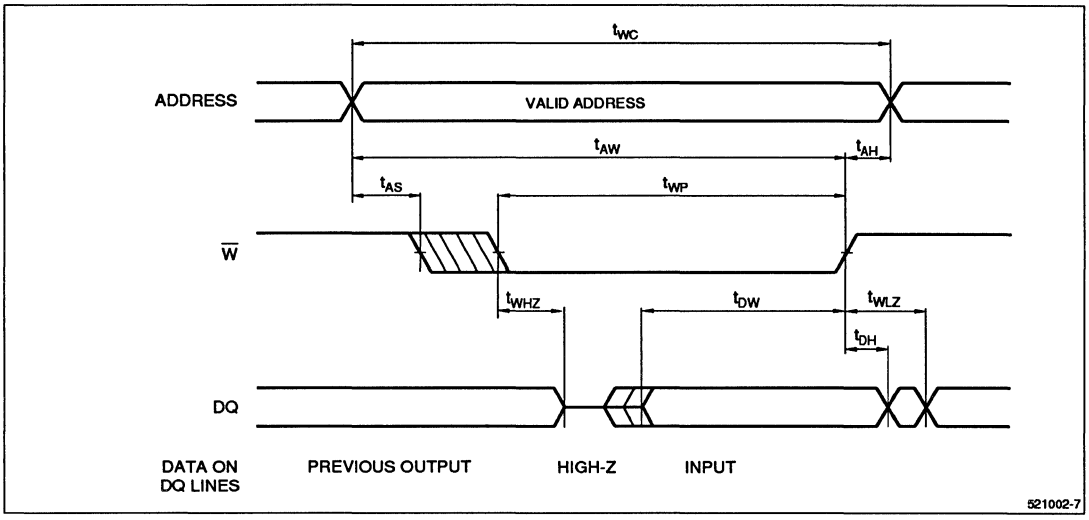


Figure 7. Write Cycle No. 1

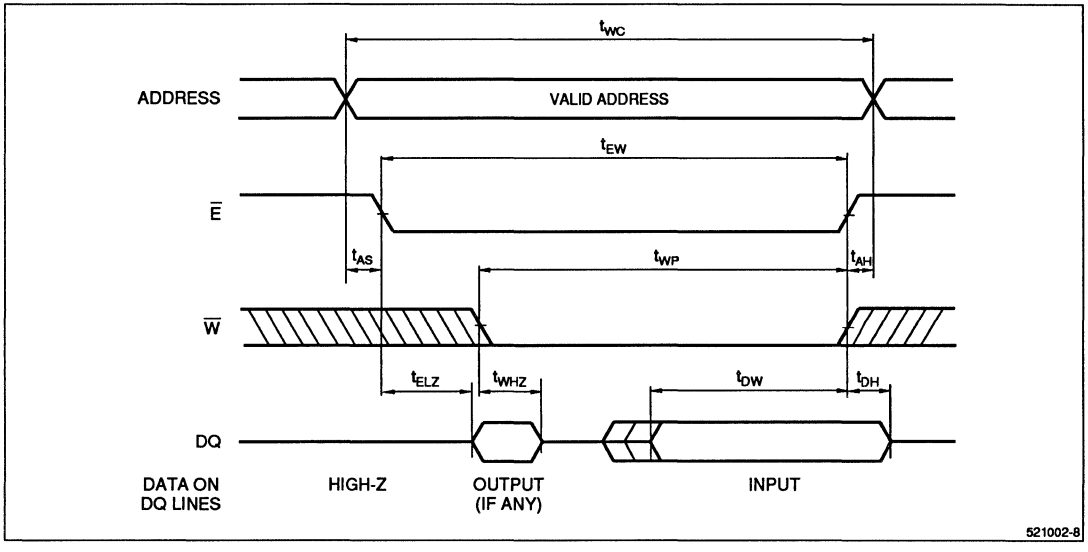
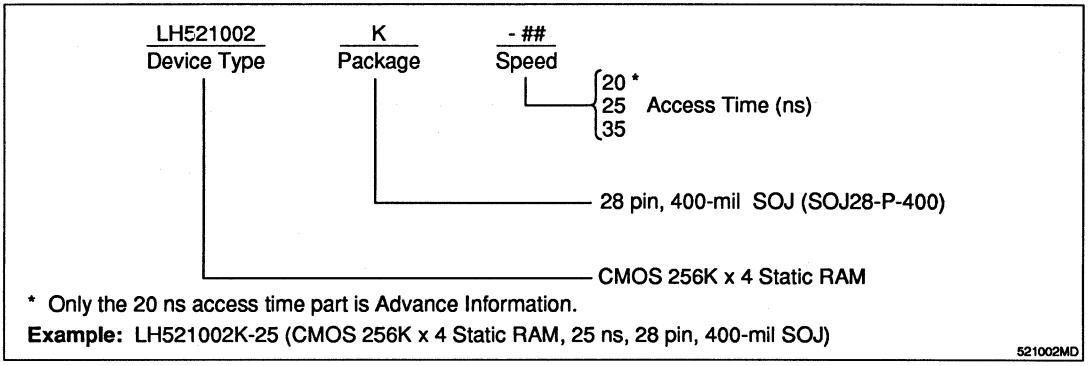


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



* Only the 20 ns access time part is Advance Information.

Example: LH521002K-25 (CMOS 256K x 4 Static RAM, 25 ns, 28 pin, 400-mil SOJ)

LH521007

PRELIMINARY

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 20 */25/35 ns
- Two Chip Enable Controls
- High Density 32-Pin, 400-mil SOJ
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH521007 is a high speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enables ($\overline{E}_1$, E_2) permit Read and Write operations when active ($\overline{E}_1$ = LOW and E_2 = HIGH) or place the RAM in a low-power standby mode when inactive ($\overline{E}_1$ = HIGH or E_2 = LOW). Standby power drops to its lowest level (I_{SB1}) if $\overline{E}_1$ is raised to within 0.2 V of V_{CC} and E_2 is lowered to less than 0.2 V.

Write cycles occur when both Chip Enables and Write Enable are active. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When both Chip Enables are active and $\overline{W}$ is inactive, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

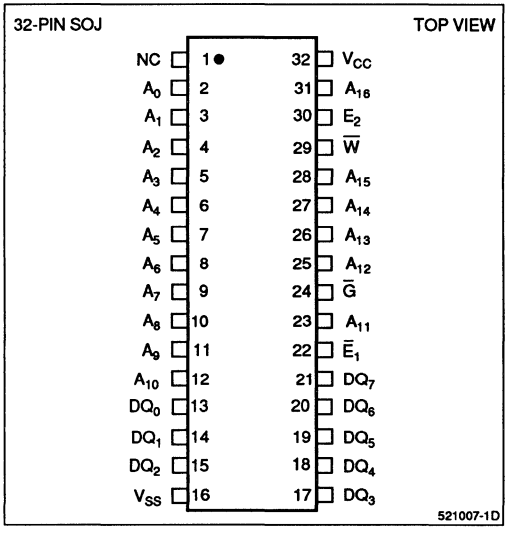


Figure 1. Pin Connections for SOJ Package

* Note: only the 20 ns access time part is Advance Information.

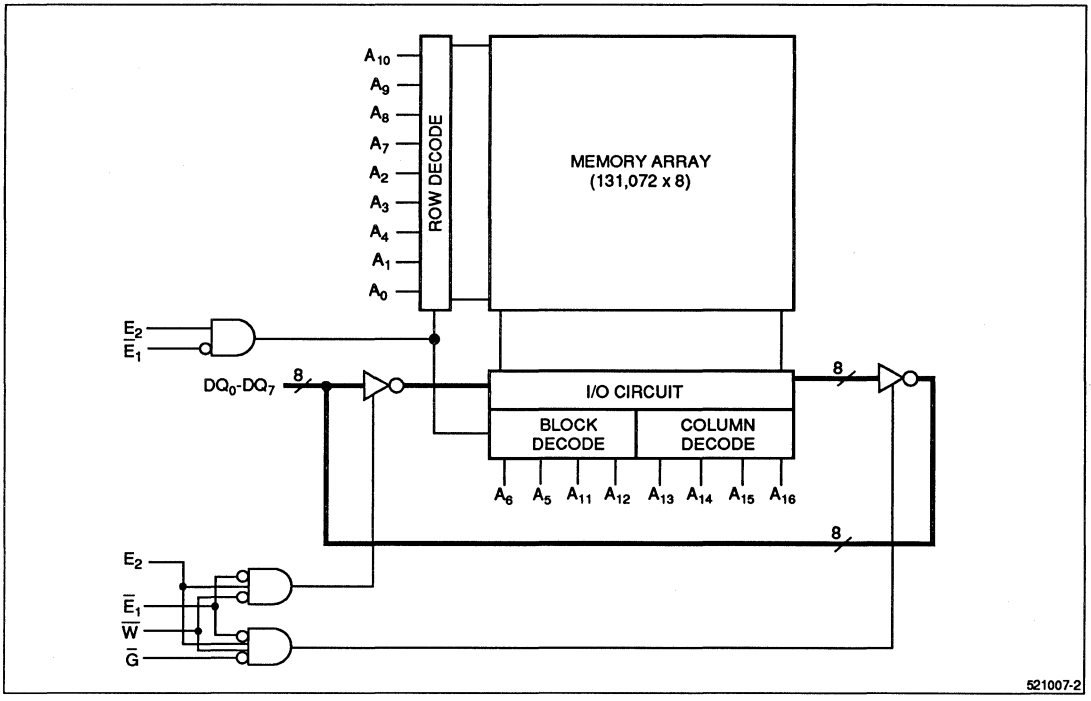


Figure 2. LH521007 Block Diagram

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	X	Standby	High-Z	Standby
X	L	X	X	Standby	High-Z	Standby
L	H	H	H	Read	High-Z	Active
L	H	L	H	Read	Data Out	Active
L	H	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}_1$, E_2	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = 20 ns [2]				mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 25 ns				mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 35 ns				mA
I_{SB1}	Standby Current	$\overline{E}_1 \geq V_{CC} - 0.2$ V [2], $E_2 \leq 0.2$ V, $V_{CC} - 0.2$ V ≤ All other inputs ≤ 0.2 V				mA
I_{SB2}	Standby Current	$\overline{E}_1 \geq V_{IH}$ [2] or $E_2 \leq V_{IL}$				mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E}_1 \geq V_{CC} - 0.2$ V and $E_2 \leq 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E}_1 \geq V_{CC} - 0.2$ V and $E_2 \leq 0.2$ V			500	µA

NOTES:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.
2. Note: only the 20 ns access time part is Advance Information.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

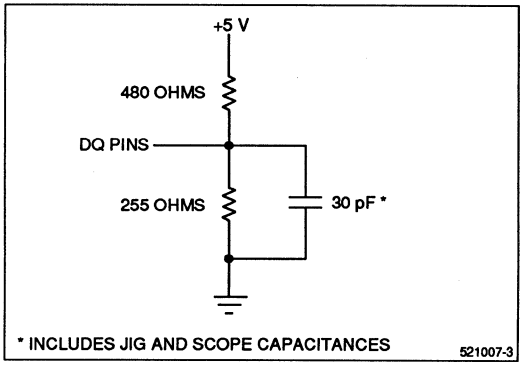


Figure 3. Output Load Circuit

DATA RETENTION TIMING

$\overline{E}_1$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}_1$ must be V_{CC} – 0.2 V or greater and E_2 must be ≤ 0.2 V to meet I_{DR} specification. All other inputs are "Don't Care."

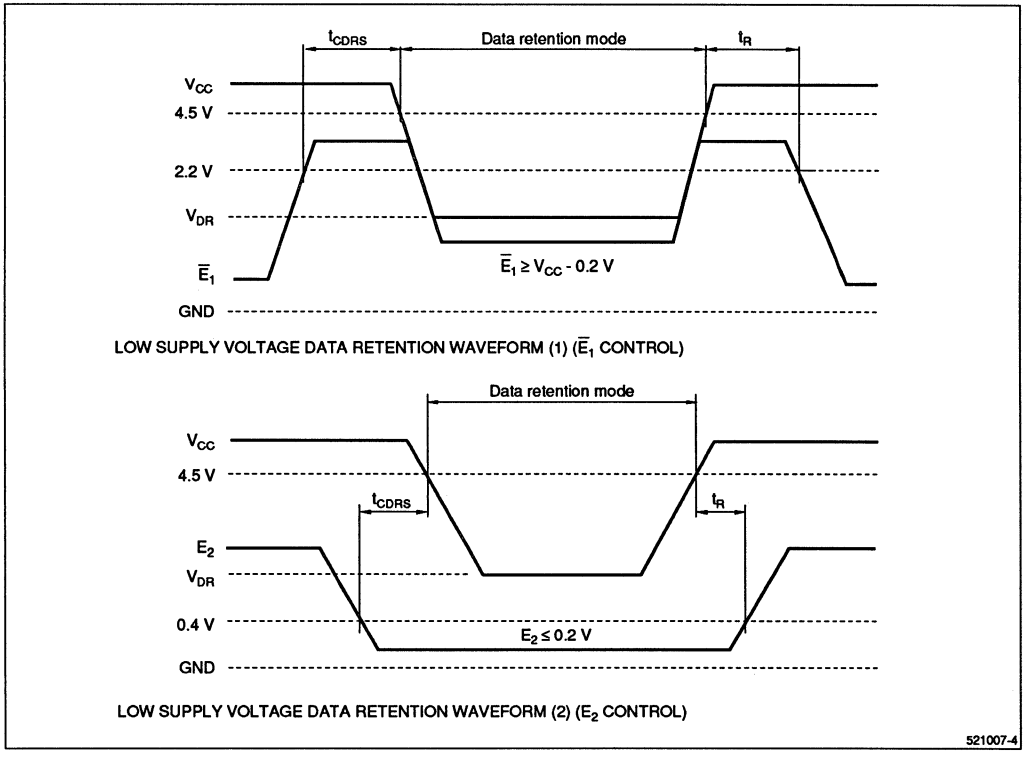


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20 [5]		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [4]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [4]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	10		12		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Sample tested only.
4. Guaranteed but not tested.
5. Note: only the 20 ns access time part is Advance Information.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ and E_2 are HIGH, $\overline{E}_1$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}_1$ and E_2 are both active. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

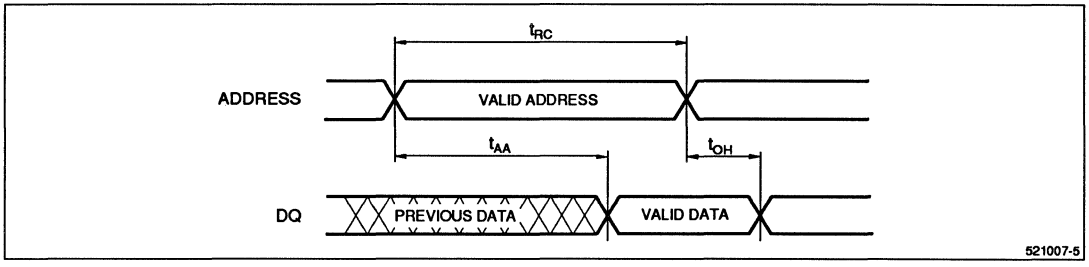


Figure 5. Read Cycle No. 1

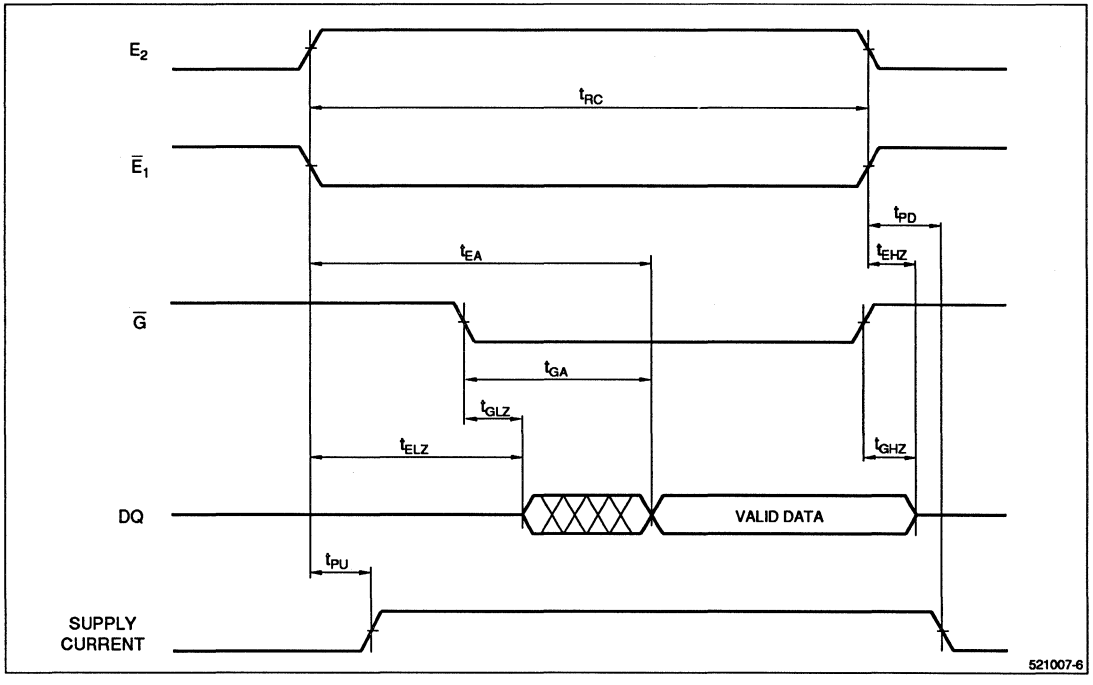


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when both $\overline{E}_1$ and E_2 are active. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}_1$ and $\overline{G}$ are LOW, E_2 is HIGH. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

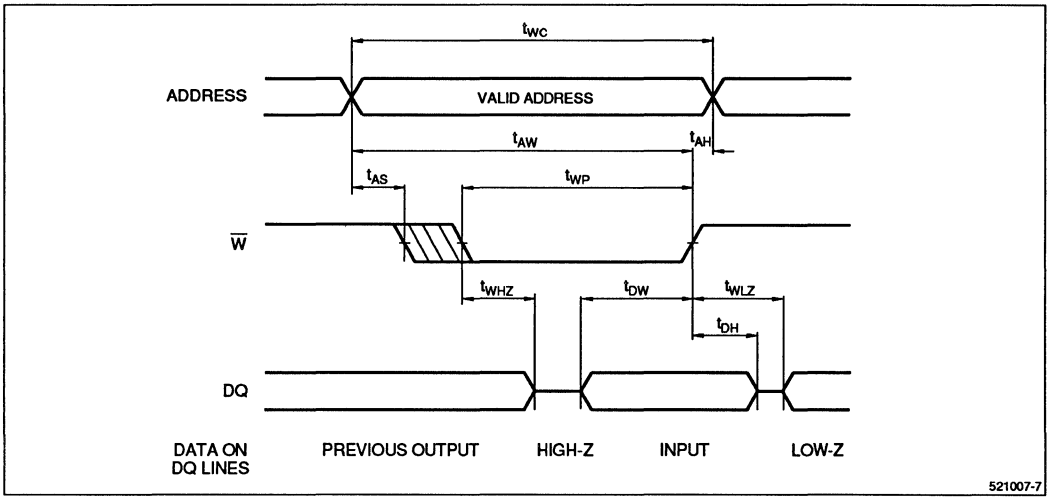


Figure 7. Write Cycle No. 1

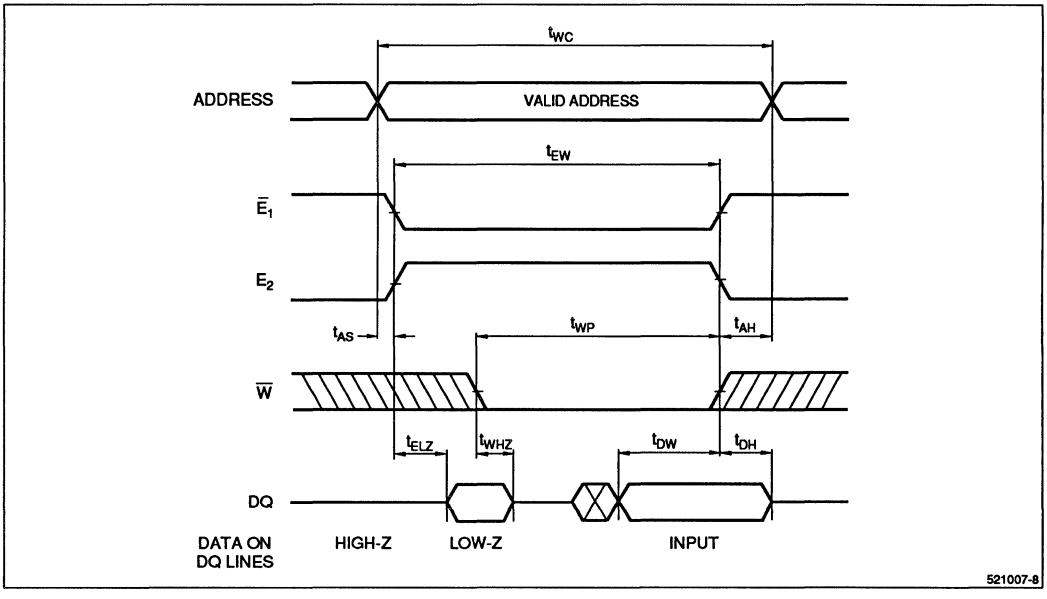
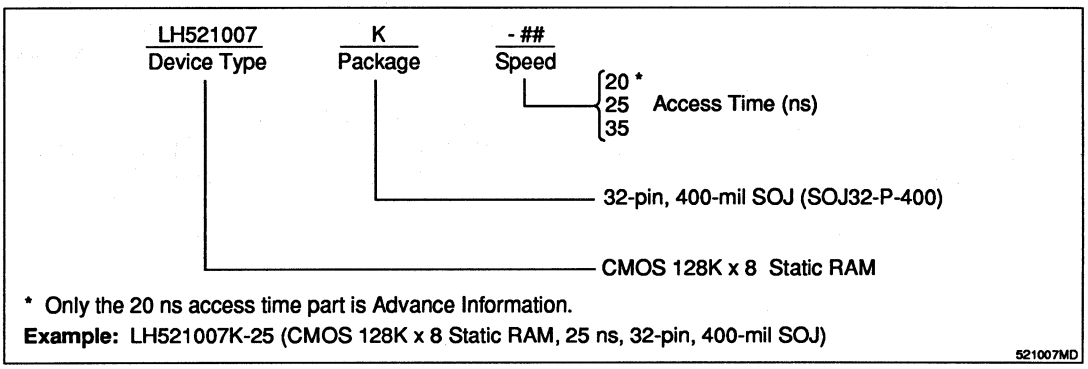


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521008

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- JEDEC Standard Pinout
- High Density 32-Pin, 400-mil SOJ Package
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH521008 is a high speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power drops to its lowest level (I_{SB1}) if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

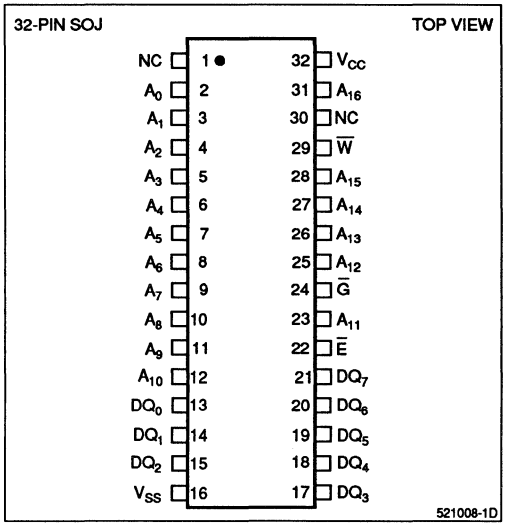


Figure 1. Pin Connections for SOJ Package

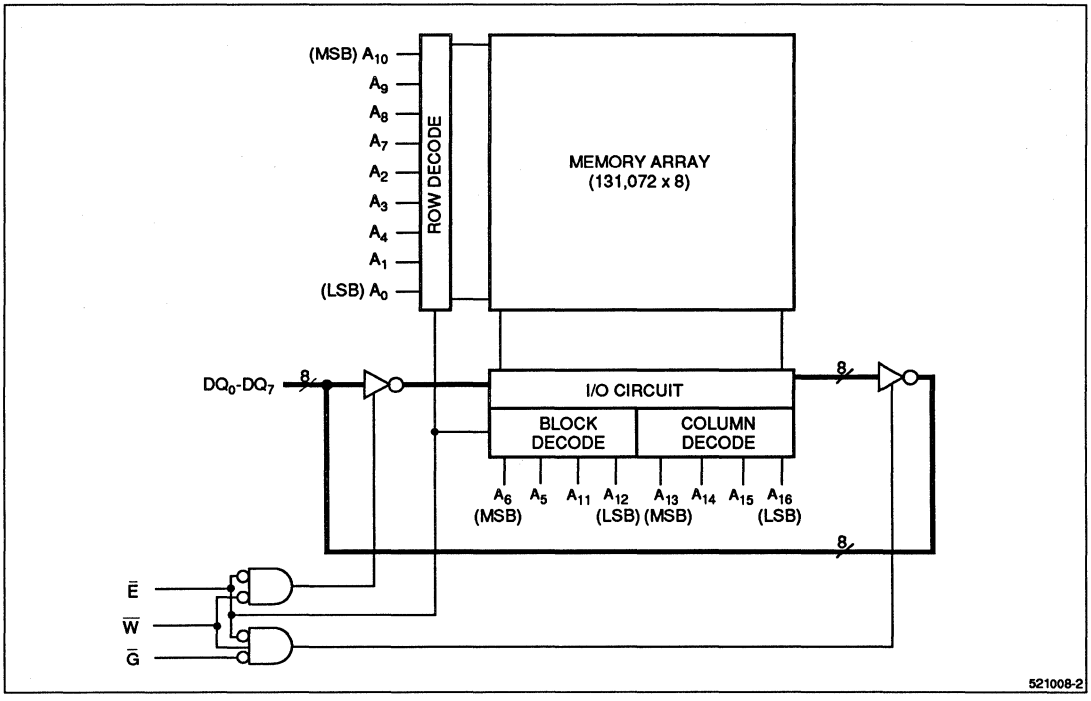


Figure 2. LH521008 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° C to 150° C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1,2]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage [2]	2.2		V_{CC} + 0.5	V

NOTES:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.
2. See Applications Note "Input/Output Level Testing" for test considerations.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = 20 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			180	mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 25 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			180	mA
I_{CC1}	Operating Current [1]	t_{CYCLE} = 35 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}			150	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.4	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			500	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

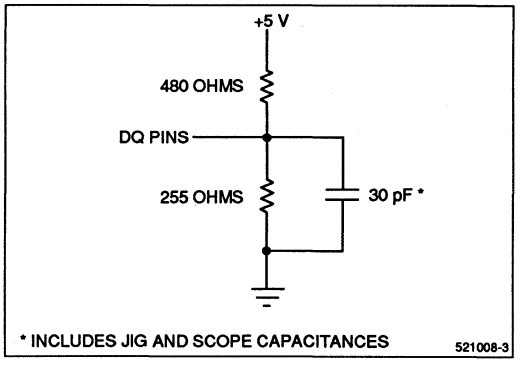


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

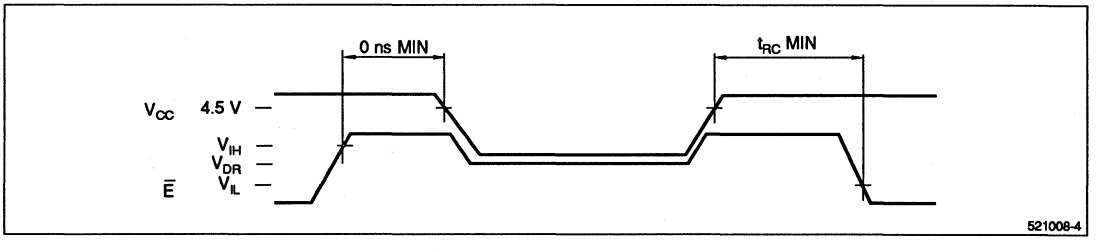


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present when both t_{GA} and t_{EA} timing are met.

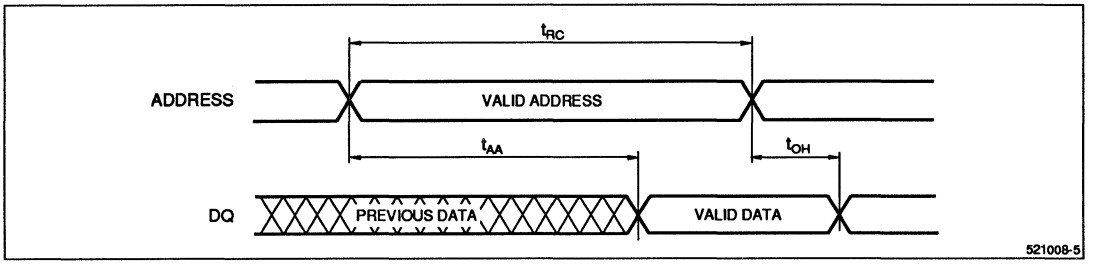


Figure 5. Read Cycle No. 1

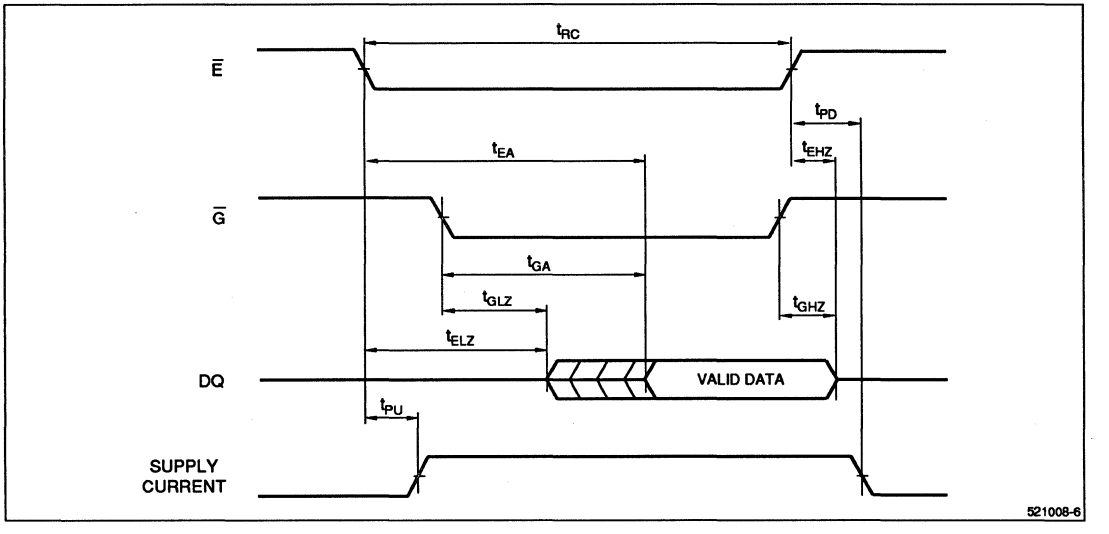


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

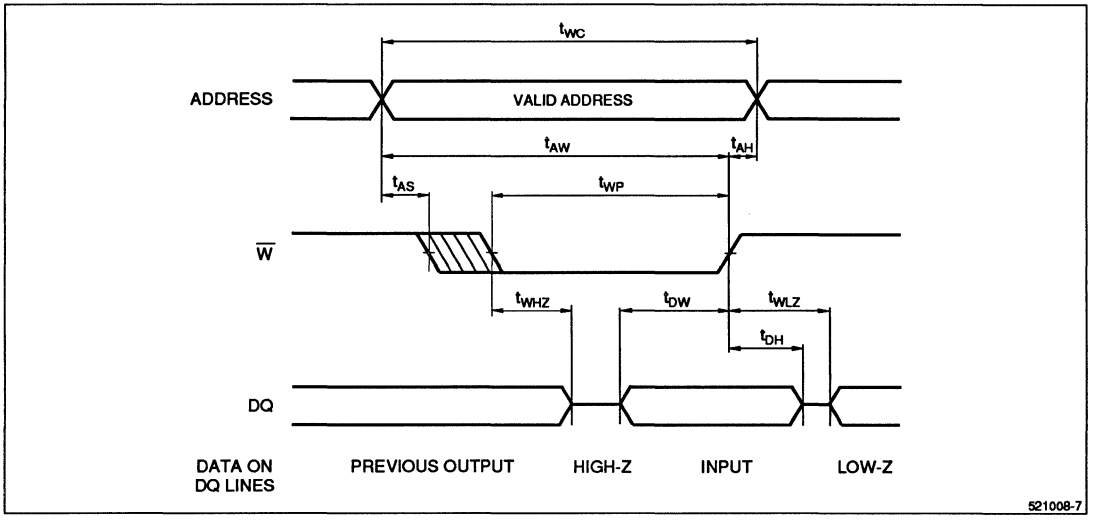


Figure 7. Write Cycle No. 1

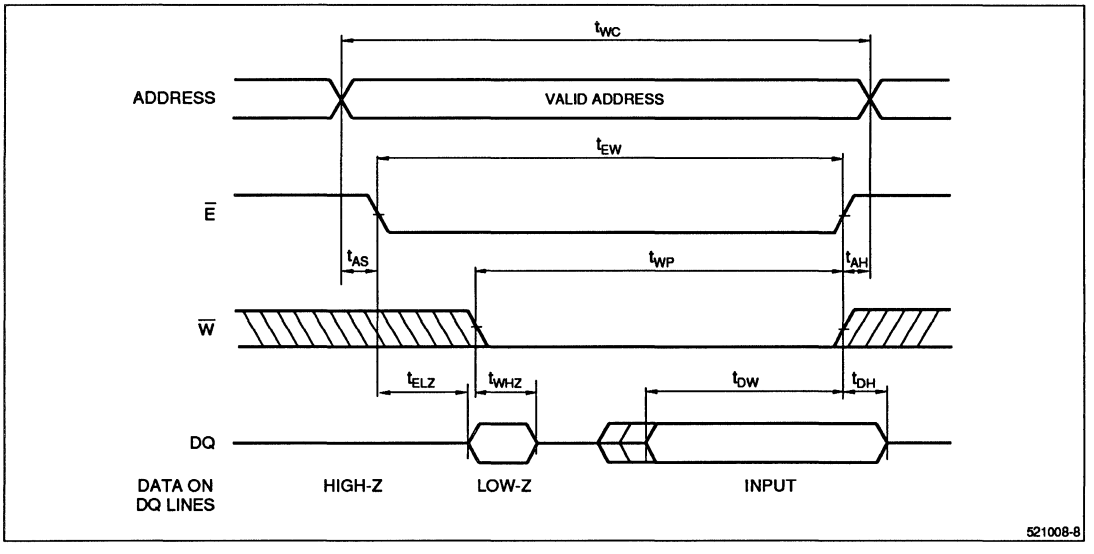
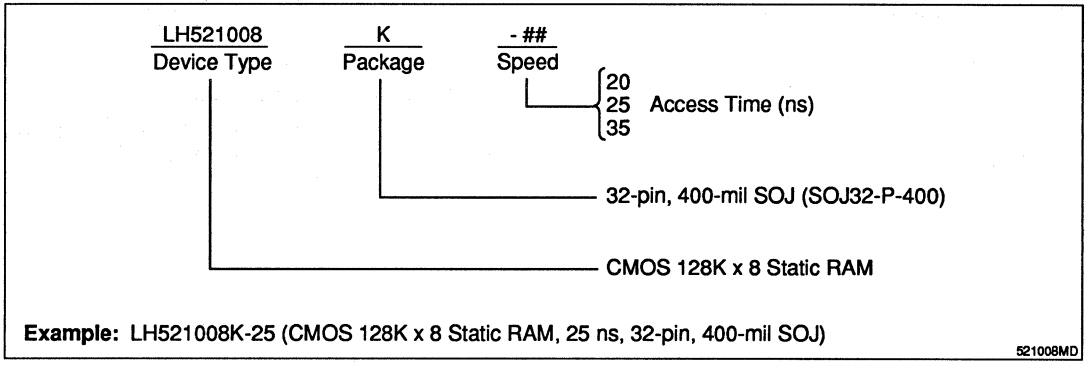


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



Example: LH521008K-25 (CMOS 128K x 8 Static RAM, 25 ns, 32-pin, 400-mil SOJ)

521008MD

LH521028

PRELIMINARY INFORMATION

CMOS 64K × 18 Static RAM

FEATURES

- Fast Access Times: 20/25/30/35 ns
- Space Saving 52-Pin PLCC
- JEDEC Standard Pinout
- Wide Word (18-Bits) for:
  – Improved Performance
  – Reduced Component Count
  – Nine-bit Byte for Parity
- Transparent Address Latch
- Reduced Loading on Address Bus
- Low Power Stand-by Mode when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH521028 is a high speed 1,179,648-bit CMOS SRAM organized as 64K × 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The LH521028 is available in a compact 52-Pin PLCC, which along with the six pairs of supply terminals, provide for reliable operation.

The control signals include Write Enable ($\overline{W}$), Chip Enable ($\overline{E}$), High and Low Byte Select ($\overline{S}_L$ and $\overline{S}_H$), Output Enable ($\overline{G}$) and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte-parity with no additional RAM required.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH).The Byte-select controls, $\overline{S}_H$ and $\overline{S}_L$, are also used to enable or disable Read and Write operations on the high and the low bytes. The Address Latches are transparent when ALE is HIGH (for applications not requiring a latch), and are latched when ALE is LOW. The Address Latches and the wide word help to eliminate the need for external Address bus buffers and/or latches.

Write cycles occur when Chip Enable ($\overline{E}$), $\overline{S}_H$ and/or $\overline{S}_L$, and Write Enable ($\overline{W}$) are LOW. The Byte-select signals can be used for Byte-write operations by disabling the other byte during the Write operation. Data is transferred from the DQ pins to the memory location specified by the 16 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ and either $\overline{S}_H$ or $\overline{S}_L$ are LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address with ALE HIGH.

PIN CONNECTIONS

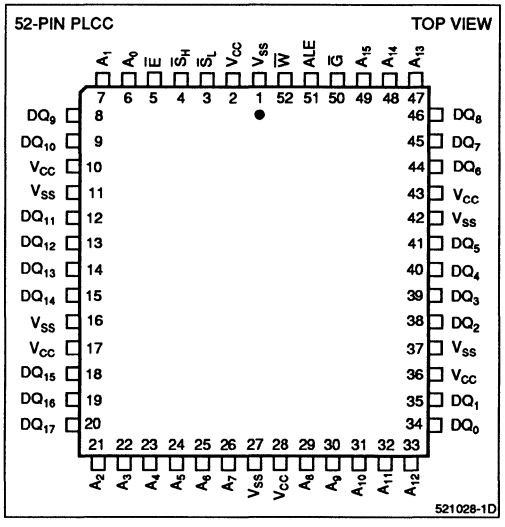


Figure 1. Pin Connections for PLCC Package

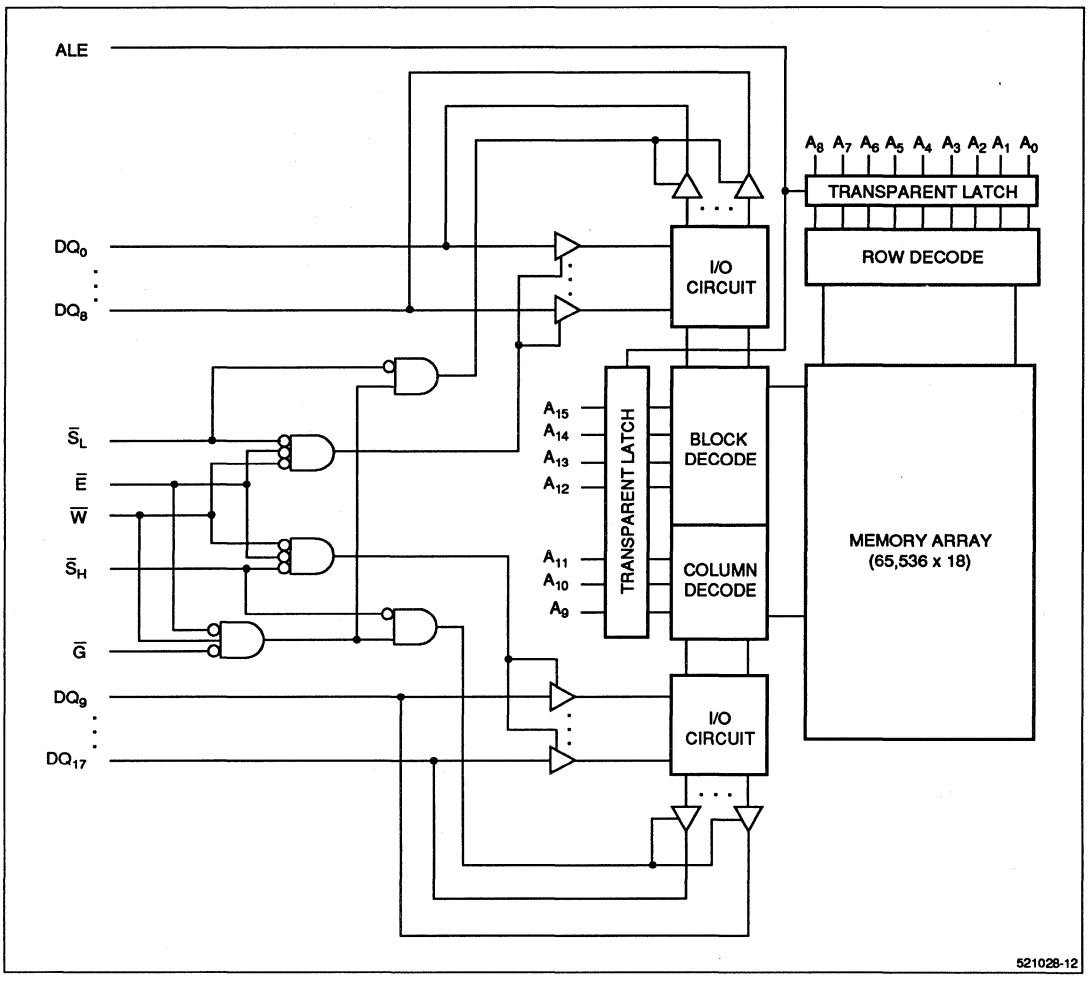


Figure 2. LH521028 Block Diagram

TRUTH TABLE

ADDRESS	$\overline{E}$	$\overline{S_H}$	$\overline{S_L}$	ALE	$\overline{G}$	$\overline{W}$	DQ_0-DQ_8	DQ_9-DQ_{17}	MODE	I_{CC}
Don't Care	H	X	X	H	X	X	High-Z	High-Z	Standby	I_{SB}
Valid	L	L	H	H	L	H	Active	High-Z	Read	I_{CC1}
Valid	L	H	L	H	L	H	High-Z	Active	Read	I_{CC1}
Valid	L	L	L	H	L	H	Active	Active	Read	I_{CC1}
Valid	L	L	L	H	H	H	High-Z	High-Z	Read	I_{CC1}
Don't Care	L	L	L	L	L	H	Data Out	Data Out	Read	I_{CC1}
Valid	L	L	H	H	X	L	Data In	Don't Care	Write, low byte	I_{CC1}
Valid	L	H	L	H	X	L	Don't Care	Data In	Write, high byte	I_{CC1}
Valid	L	L	L	H	X	L	Data In	Data In	Write, both bytes	I_{CC1}
Valid	L	H	H	H	X	L	Don't Care	Don't Care	Write, inhibited	I_{CC1}
Don't Care	L	L	L	L	X	L	Data In	Data In	Write, both bytes	I_{CC1}

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	SIGNAL
1	V_{SS}
2	V_{CC}
3	$\overline{S_L}$
4	$\overline{S_H}$
5	$\overline{E}$
6	A_0
7	A_1
8	DQ_9
9	DQ_{10}
10	V_{CC}
11	V_{SS}
12	DQ_{11}
13	DQ_{12}

PIN	SIGNAL
14	DQ_{13}
15	DQ_{14}
16	V_{SS}
17	V_{CC}
18	DQ_{15}
19	DQ_{16}
20	DQ_{17}
21	A_2
22	A_3
23	A_4
24	A_5
25	A_6
26	A_7

PIN	SIGNAL
27	V_{SS}
28	V_{CC}
29	A_8
30	A_9
31	A_{10}
32	A_{11}
33	A_{12}
34	DQ_0
35	DQ_1
36	V_{CC}
37	V_{SS}
38	DQ_2
39	DQ_3

PIN	SIGNAL
40	DQ_4
41	DQ_5
42	V_{SS}
43	V_{CC}
44	DQ_6
45	DQ_7
46	DQ_8
47	A_{13}
48	A_{14}
49	A_{15}
50	$\overline{G}$
51	ALE
52	$\overline{W}$

PIN DEFINITION

V_{CC} Positive Supply Voltage Terminals

V_{SS} Reference Terminals

$A_0 - A_{15}$ Address Bus Input

The Address bus is decoded to select one 18-bit word out of the total 64K words for Read and Write operations.

$\overline{E}$ Chip Enable Active LOW Input

Chip Enable is used to enable the device for Read and Write operations. When HIGH, both Read and Write operations are disabled and the device is in a reduced power state. When LOW, a Read or Write operation is enabled.

$\overline{W}$ Write Enable Active LOW Input

Write Enable is used to select either Read or Write operations when the device is enabled. When Write Enable is HIGH and the device is Enabled, a Read operation is selected. When Write Enable is LOW and the device is enabled, a Write operation is selected. A Byte-write operation is available by using the Byte-select controls.

$\overline{S}_H$, $\overline{S}_L$ Select High Select Low Active LOW Inputs

The Select High and Select Low signals, in conjunction with the Chip Enable and Write Enable signals, allow the selection of the individual bytes for Read and Write operations. When High, the Select signal will deselect its byte and prevent Read or Write operations. When the Select signal is LOW and Chip Enable is LOW, a Read or Write operation is performed at the location determined by the contents of the Address bus. When Chip Enable is HIGH, the Select signals are Don't Care. Select Low ($\overline{S}_L$) is assigned to $DQ_0 - DQ_8$ and Select High ($\overline{S}_H$) is assigned to $DQ_9 - DQ_{17}$.

ALE Address Latch Enable Active High Input

The Address Latch Enable signal is used to control the Transparent latches on the Address bus. The Latches are transparent when HIGH and are latched when LOW. If not required, Address Latch Enable may be tied HIGH, leaving the Address bus in a transparent condition.

$DQ_0 - DQ_{17}$ Data Bus Input/Output

$DQ_0 - DQ_8$ comprise the Low byte, selected by $\overline{S}_L$, and $DQ_9 - DQ_{17}$ comprise the High Data byte, selected by $\overline{S}_H$. The Data Bus is in a high impedance input mode during Write operations and standby. The Data bus is in a low-impedance output mode during Read operations.

$\overline{G}$ Output Enable Active LOW Input

The Output Enable signal is used to control the output buffers on the Data Input/Output bus. When $\overline{G}$ is HIGH, all output buffers are forced to a high impedance condition. When $\overline{G}$ is LOW, the output buffers will become active only during a Read operation ($\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ are LOW, $\overline{W}$ is HIGH).

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = minimum			300	mA
I_{SB1}	Standby Current	All Inputs ≥ V_{CC} − 0.2 V, $\overline{E} \geq V_{IH}$ (V_{CC} − 0.2 V) ≤ All Other Inputs ≤ 0.2 V			4	mA
I_{SB2}	Standby Current	$\overline{E} = V_{IH}$			40	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC}$ − 0.2 V All other inputs (V_{CC} − 0.2 V) ≤ V_{IN} ≤ (0.2 V)	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC}$ − 0.2 V All other inputs (V_{CC} − 0.2 V) ≤ V_{IN} ≤ (0.2 V)			500	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

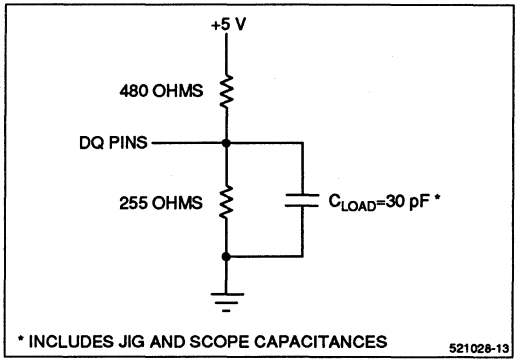


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{DQ} (I/O Capacitance)	7 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs must be held at CMOS input levels (V_{CC} – 0.2 V) ≤ V_{IN} ≤ (0.2V).

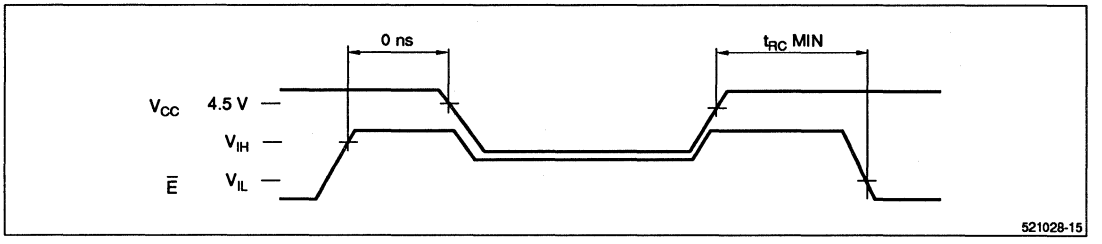


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-30		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE									
t_{RC}	Read Cycle Timing	20		25		30		35		ns
t_{AA}	Address Access Time		20		25		30		35	ns
t_{ASL}	Address Setup to Latch Enable	1		1		2		2		ns
t_{AHL}	Address Hold from Latch Enable	4		4		5		5		ns
t_{LEA}	Latch Enable to Data Valid		22		27		32		37	ns
t_{LHM}	Latch Enable High Pulse Width	5		6		6		6		ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{LH}	Output Hold from Latch High	3		3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		30		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		15		20	ns
t_{SA}	$\overline{S}$ Low to Valid Data		10		12		15		20	ns
t_{SLZ}	$\overline{S}$ Low to Output Active [2,3]	2		3		3		3		ns
t_{SHZ}	$\overline{S}$ High to Output High-Z [2,3]		10		12		15		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		15		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		15		20	ns
t_{RCS}	Read Setup from $\overline{W}$ High	0		0		0		0		ns
t_{RCH}	Read Hold from $\overline{W}$ Low	0		0		0		0		ns
t_{PU}	$\overline{E}$ LOW to Power Up Time [3]	0		0		0		0		ns
t_{PD}	$\overline{E}$ HIGH to Power Down Time [3]		20		25		30		35	ns
	WRITE CYCLE									
t_{WC}	Write Cycle Time	20		25		30		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		25		30		ns
t_{SW}	$\overline{S}$ LOW to End of Write	15		20		25		30		ns
t_{AW}	Address Valid to End of Write	15		20		25		30		ns
t_{AS}	Address Setup to Start of Write	0		0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		0		ns
t_{ASL}	Address Setup to Latch Enable	1		1		2		2		ns
t_{AHL}	Address Hold from Latch Enable	4		4		5		5		ns
t_{LHW}	Latch Hold from $\overline{W}$ High	0		0		0		0		ns
t_{LHM}	Latch Enable HIGH Pulse Width	5		6		6		6		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		30		ns
t_{DW}	Input Data Setup Time	9		10		12		15		ns
t_{DH}	Input Data Hold Time	0		0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		12		14	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1: (Unlatched Address Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode), $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2: (Unlatched Chip Enable Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode). Read cycle timing is referenced from when $\overline{E}$, $\overline{S}$, and $\overline{G}$ are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.

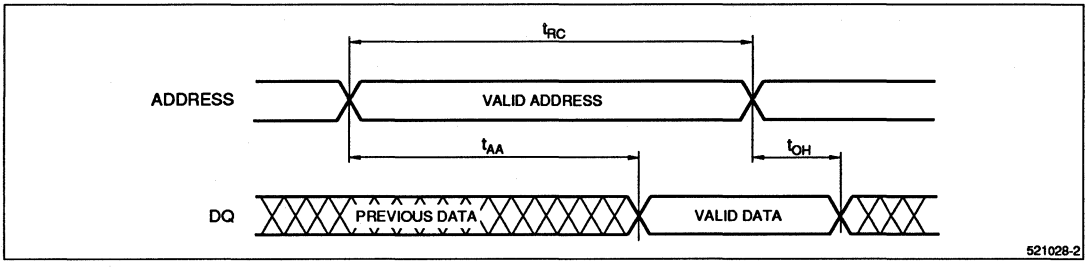


Figure 5. Read Cycle No. 1

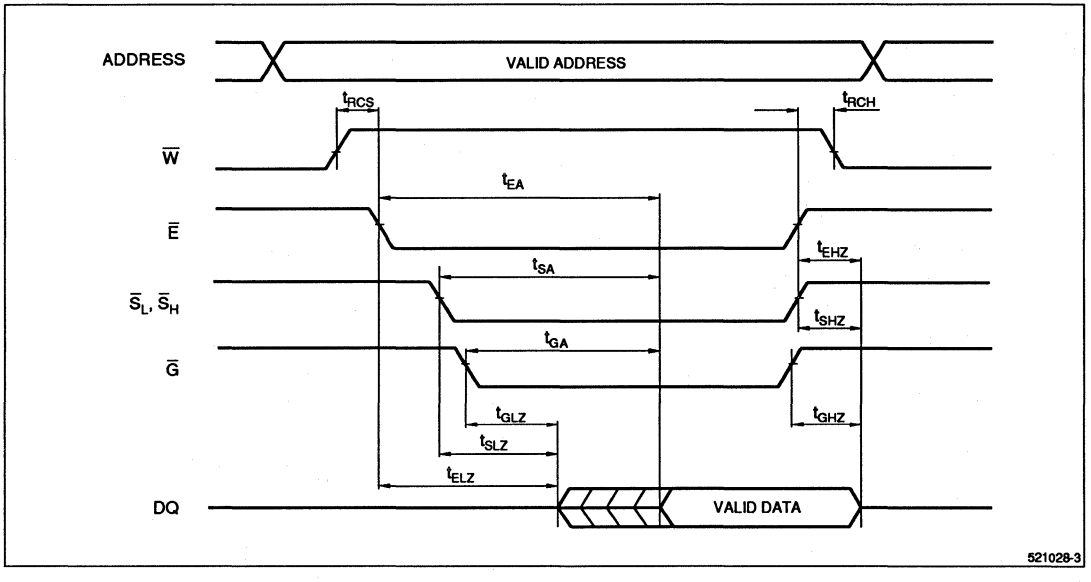


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 3 (Latched Address Controlled Read)

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$, $\overline{S}_H$, $\overline{S}_L$ and $\overline{G}$ are LOW. Both t_{AA} and t_{LEA} must be met before valid data is available. If the address is valid prior to the rising edge of ALE, then the access time is t_{LEA}. If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is t_{AA}. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

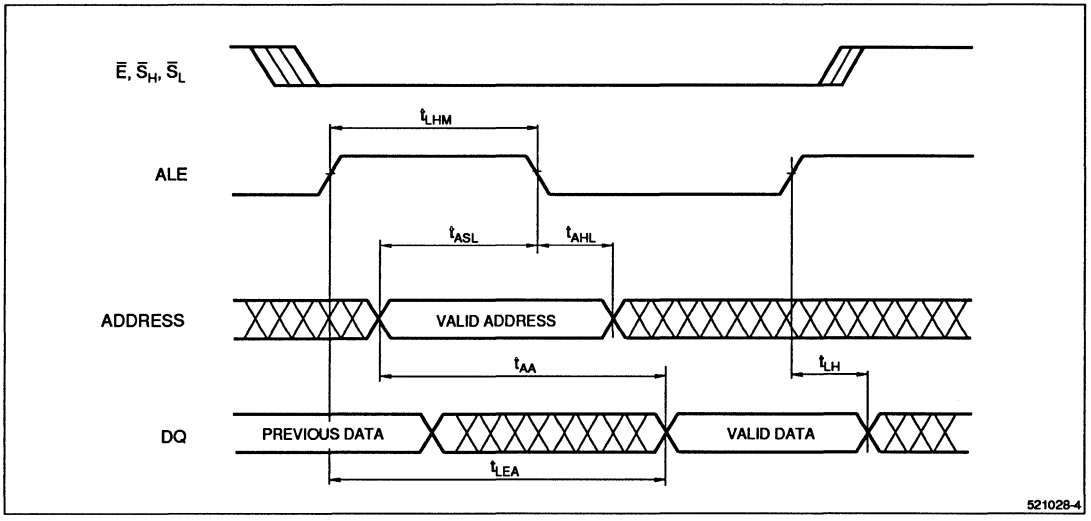


Figure 7. Read Cycle No. 3

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 4

Chip is in Read Mode: Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, t_{SA} and t_{GA}, but may become active as early as t_{ELZ}, t_{SLZ} or t_{GLZ}.

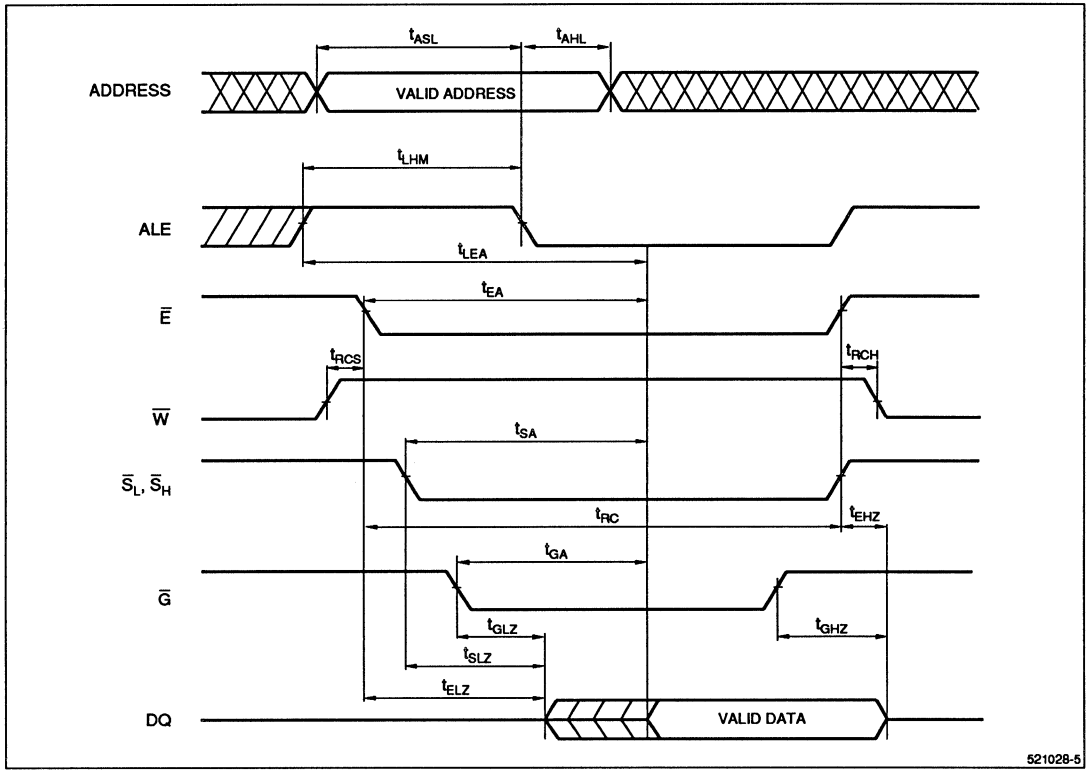


Figure 8. Read Cycle No. 4

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ go LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH521028's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 (Unlatched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW, ALE is High. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$, $\overline{S}_L$, $\overline{S}_H$ Controlled Write)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$, $\overline{S}_H$/$\overline{S}_L$ if $\overline{G}$ is LOW.

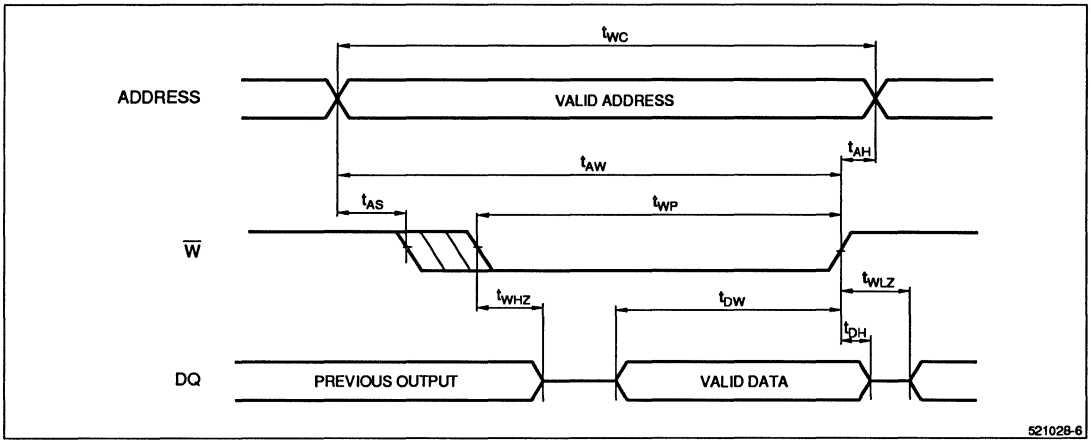


Figure 9. Write Cycle No. 1

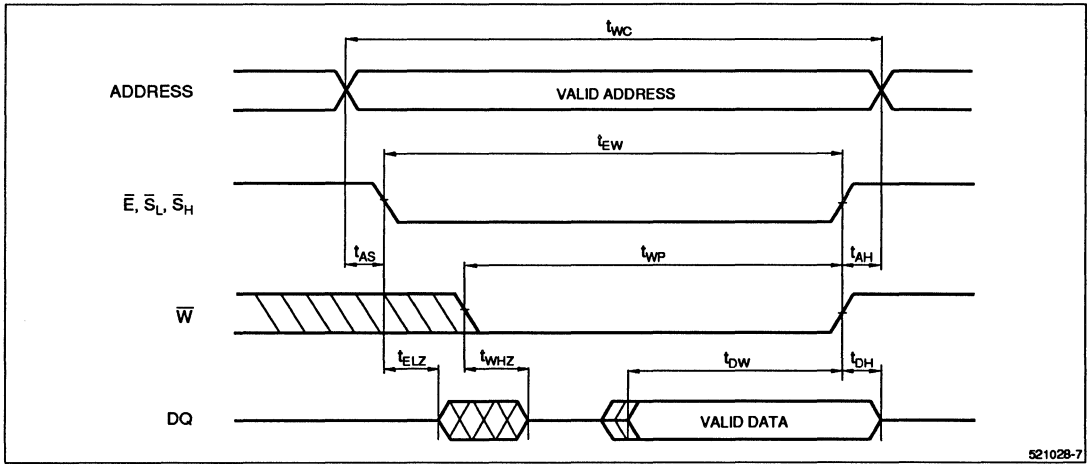


Figure 10. Write Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE (cont'd)

Write Cycle No. 3 (Latched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW.

Write Cycle No. 4 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edges of $\overline{E}$ and $\overline{S}_H/\overline{S}_L$.

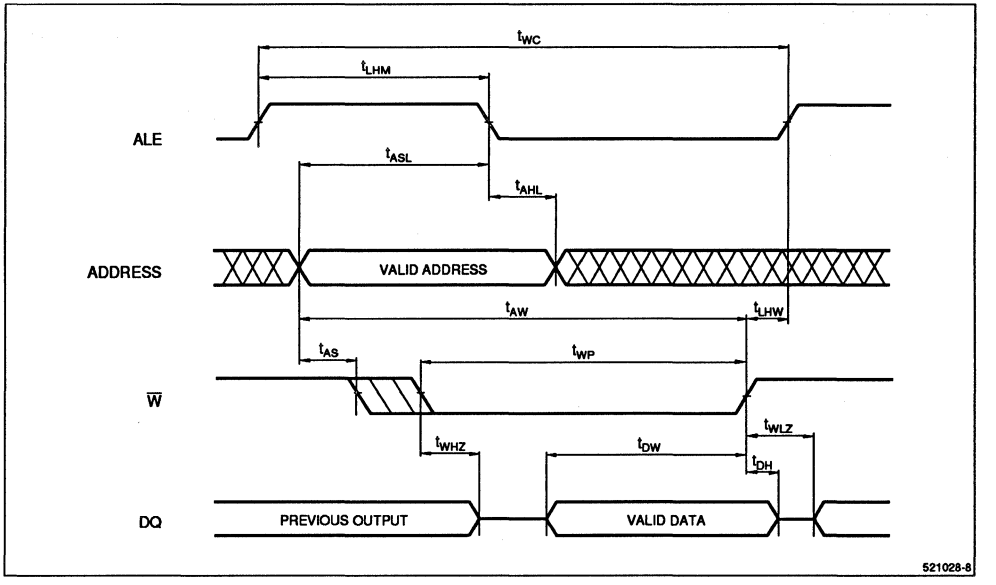


Figure 11. Write Cycle No. 3

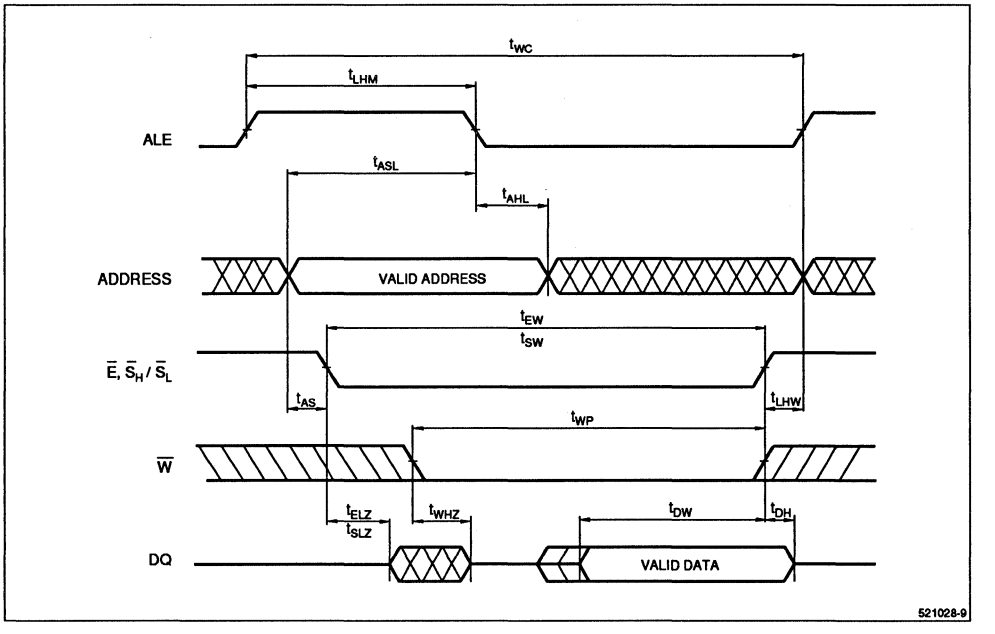


Figure 12. Write Cycle No. 4

BYTE OPERATIONS

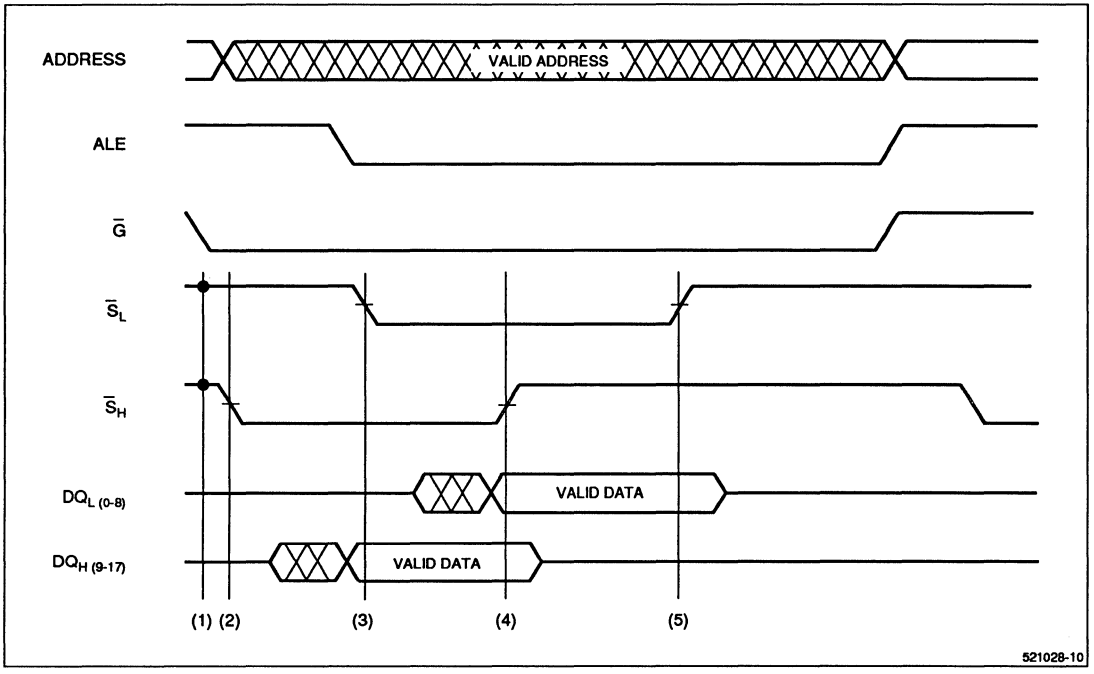


Figure 13. Byte Read: ($\overline{E}$ is LOW and $\overline{W}$ is HIGH)

Byte Read Description (Figure 13)

To read individual bytes, the device must be enabled ($\overline{E}$ is LOW), $\overline{W}$ must be HIGH, the outputs must be enabled ($\overline{G}$ is LOW) and the addresses must be either stable or latched with ALE. The above diagram is one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(1) At the beginning of the cycle both $\overline{S}_L$ and $\overline{S}_H$ are HIGH.

(2) $\overline{S}_H$ goes LOW initiating a Read on the upper byte $DQ_{H(9\text{-}17)}$. $\overline{S}_L$ remains HIGH keeping the lower byte $DQ_{L(0\text{-}8)}$ disabled and in a high-impedance mode.

(3) $\overline{S}_L$ goes LOW activating $DQ_{L(0\text{-}8)}$. Valid data is available in t_{SA} following $\overline{S}_L$ going LOW.

(4) When $\overline{S}_H$ goes HIGH, $DQ_{H(9\text{-}17)}$ remains valid for t_{SHZ} before returning to a high-impedance condition.

(5) Finally, the Read for the lower byte is terminated by deasserting $\overline{S}_L$ (HIGH). $DQ_{L(0\text{-}8)}$ remains active for t_{SHZ} following $\overline{S}_L$ going HIGH.

BYTE OPERATIONS (cont'd)

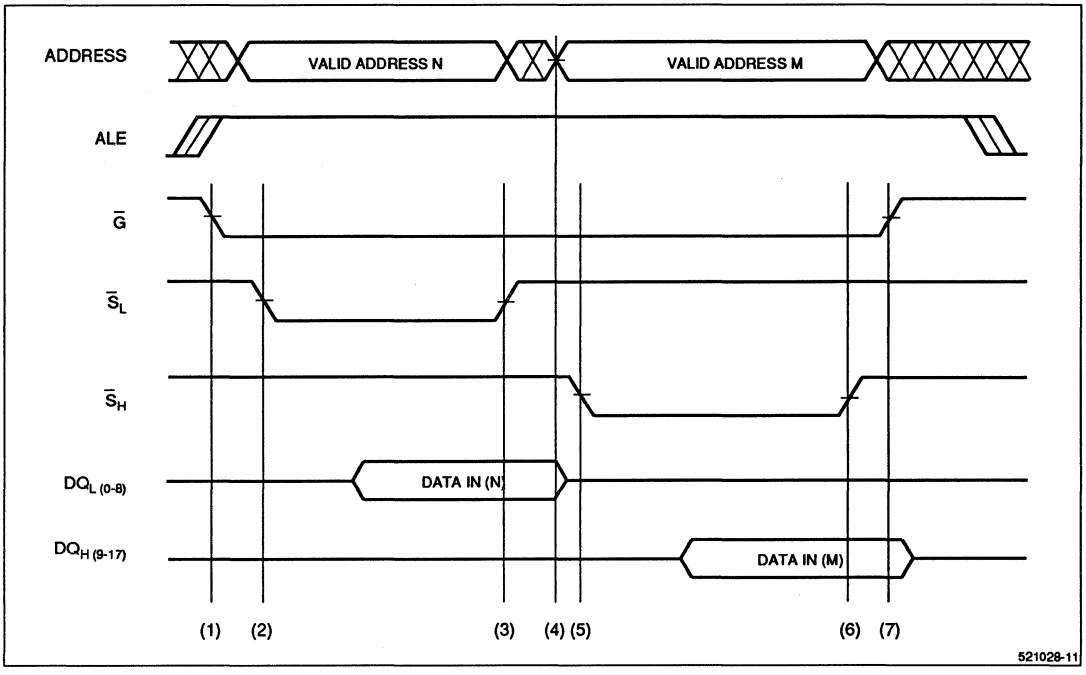


Figure 14. Byte Write: ($\overline{E}$ is LOW)

Byte Write Description (Figure 14)

To do individual byte-write operations, the device must be enabled ($\overline{E}$ is LOW, $\overline{G}$ is don't care) and addresses must be either stable or latched. The above diagram is one example of the byte-write capabilities of this device. The diagram shows two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

(1) $\overline{W}$ goes LOW while $\overline{S}_L$ and $\overline{S}_H$ remain HIGH.

(2) $\overline{S}_L$ goes LOW initiating a Write into the lower byte $DQ_{L(0\text{-}8)}$ of memory location N. $\overline{S}_H$ remains HIGH preventing a Write into the upper byte $DQ_{L(9\text{-}17)}$ of memory location N.

(3) $\overline{S}_L$ now goes HIGH terminating the Write operation on the lower byte of memory location N.

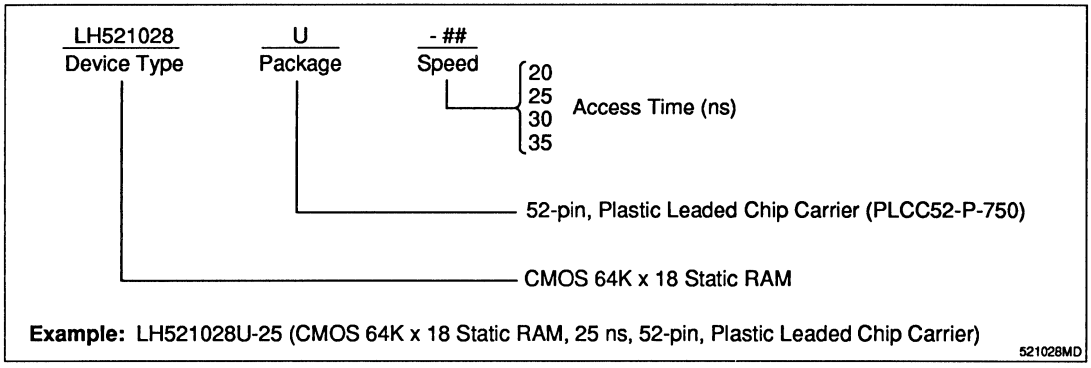
(4) Address N is changed to M.

(5) The Write operation is now initiated on the upper byte $DQ_{H(9\text{-}17)}$ by bringing $\overline{S}_H$ LOW. $\overline{S}_L$ remains HIGH preventing a Write operation from occurring in the lower byte $DQ_{L(0\text{-}8)}$ of memory location N+ 1.

(6) $\overline{S}_H$ now goes HIGH terminating the Write operation on the upper byte of address M.

(7) $\overline{W}$ goes HIGH, ending the Write operation.

ORDERING INFORMATION



LH521032

PRELIMINARY

256K × 4 Separate I/O Static RAM

FEATURES

- Separate Data In and Data Out
- Reduces Chip Count and Increases Performance
- Fast Access Times: 20/25/35 ns
- Space Saving 32-Pin, 400-mil SOJ
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation

FUNCTIONAL DESCRIPTION

The LH521032 is a high-speed 1,048,576-bit static RAM organized as 256K × 4 with separate Data Input and Output buses.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) gates power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the Data In pins to the memory location specified by the 18 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$. Data will be output on the Data Out pins. The Data Out pins become high-impedance during Write operations, with the contents of the Data In bus flowing-through to the Data Out bus.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

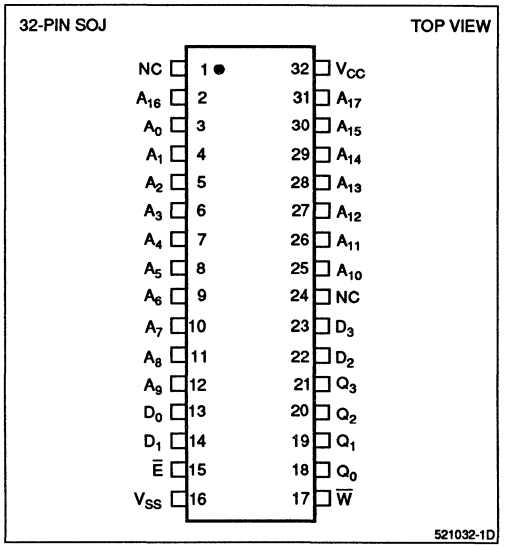


Figure 1. Pin Connections for SOJ Package

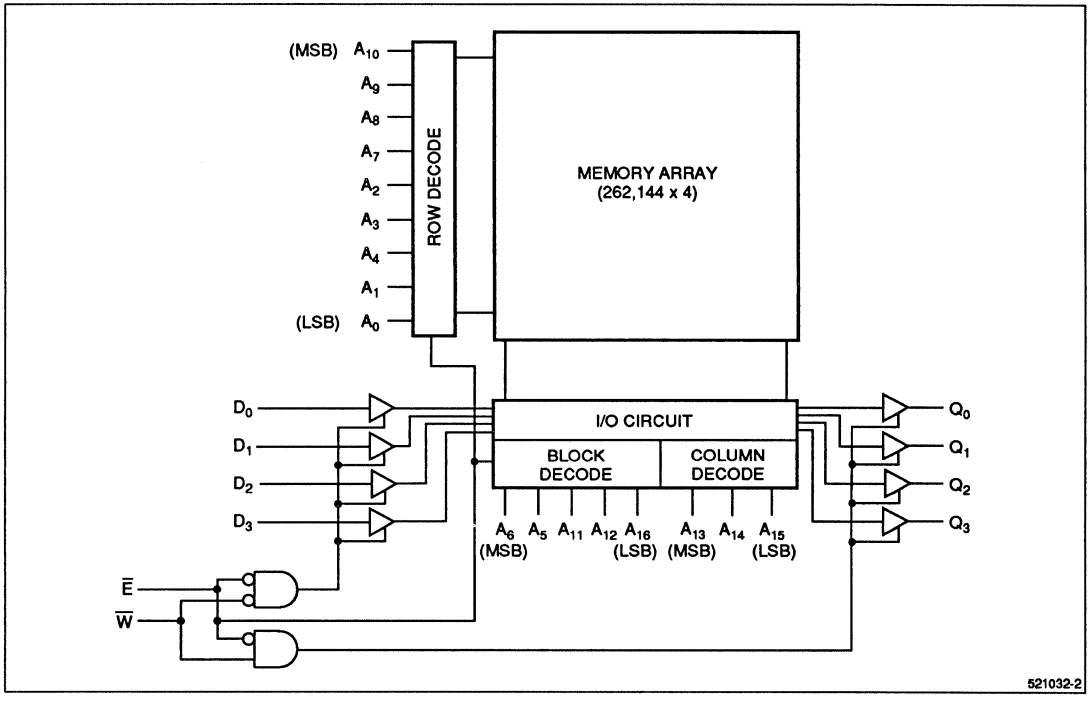


Figure 2. LH521032 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	$D_0 - D_3$	$Q_0 - Q_3$	I_{CC}
H	X	Not Selected	Don't Care	High-Z	Standby
L	H	Read	Don't Care	Data Out	Active
L	L	Write	Data In	High-Z	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
$D_0 - D_3$	Data Inputs
$Q_0 - Q_3$	Data Outputs
$\overline{E}$	Chip Enable input

PIN	DESCRIPTION
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = min				mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V				mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$				mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	
C_{DQ} (I/O Capacitance)	

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

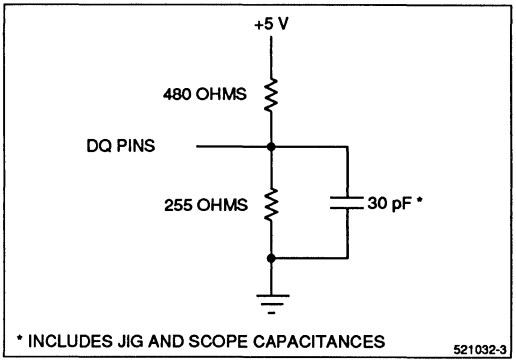


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		30		ns
t_{DW}	Input Data Setup Time	10		12		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		10		15		20	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Guaranteed but not tested.

TIMING DIAGRAMS — READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of $D_0 - D_3$ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

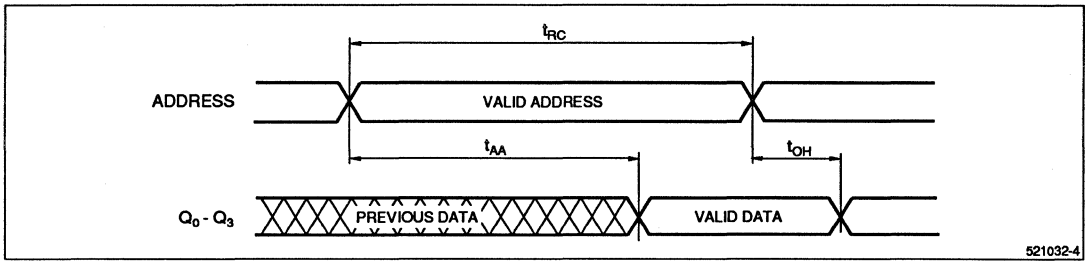


Figure 4. Read Cycle No. 1

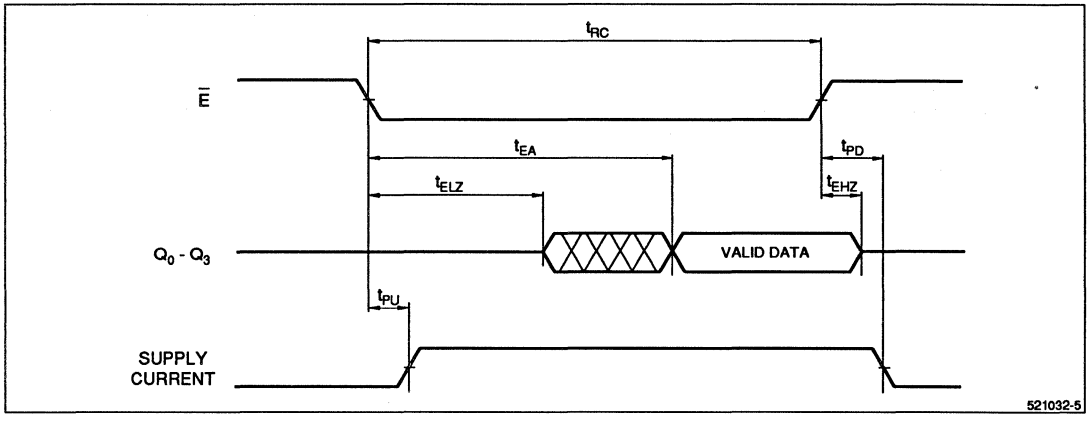


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS — WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

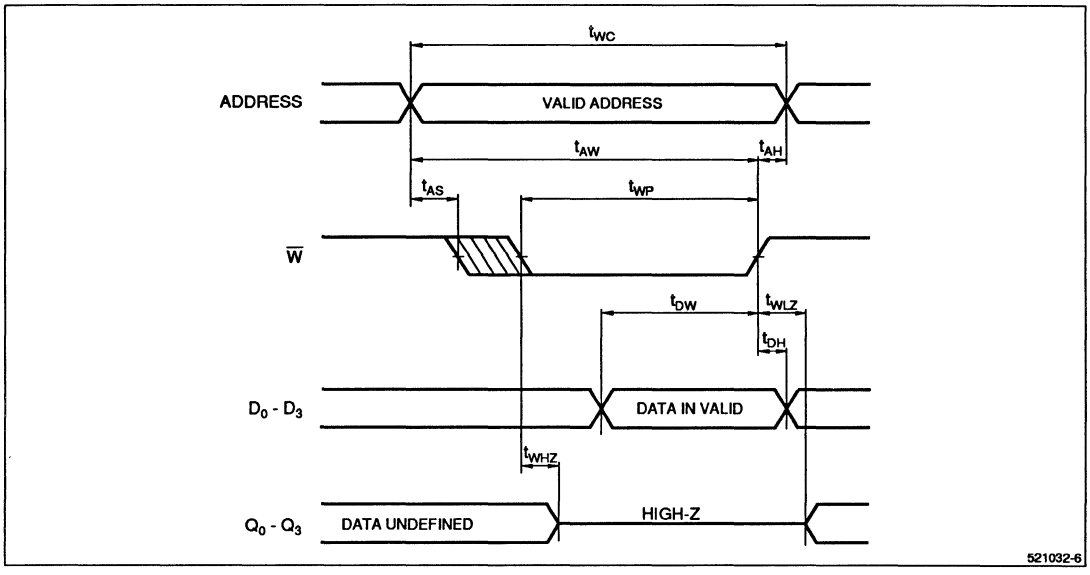


Figure 6. Write Cycle No. 1

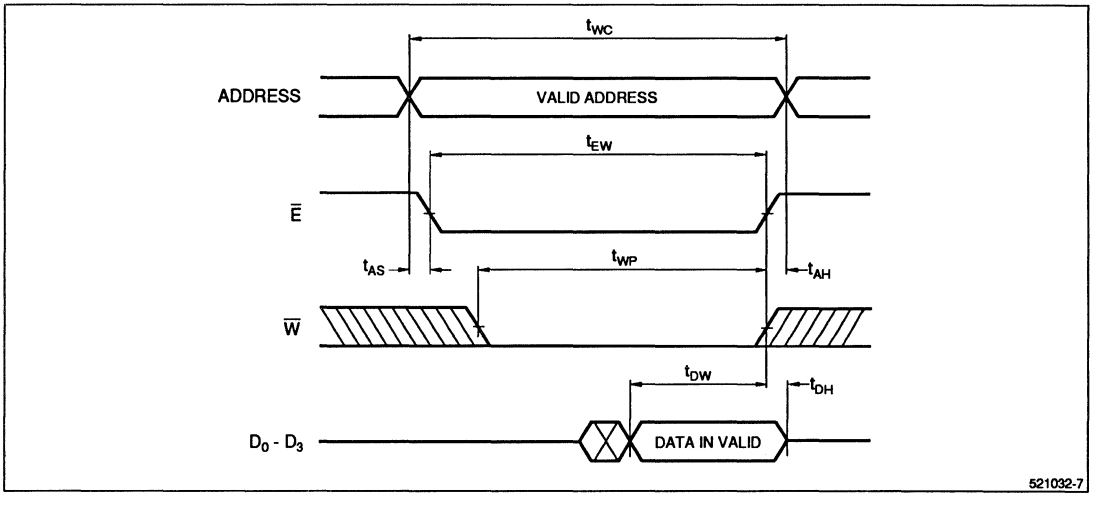
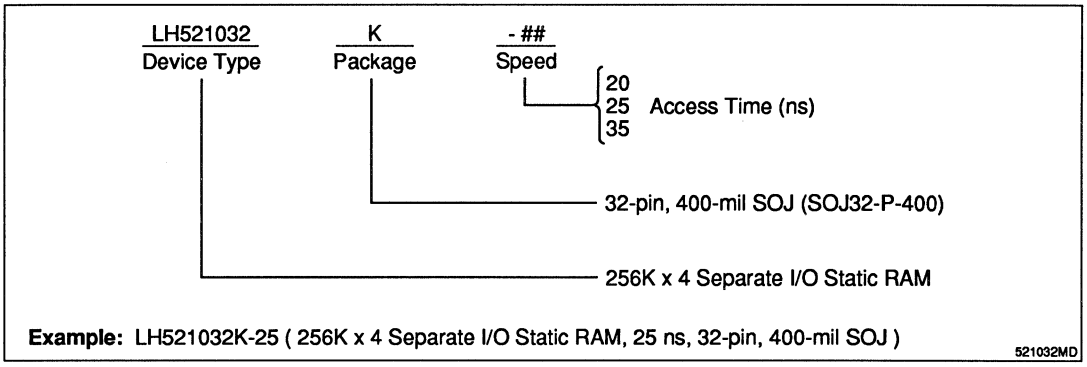


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



Example: LH521032K-25 (256K x 4 Separate I/O Static RAM, 25 ns, 32-pin, 400-mil SOJ)

LH5749/J

CMOS 64K (8K × 8) OTPROM/EPROM

FEATURES

- 8,192 × 8 bit organization
- Access times:
  LH5749J: 55/70 ns (MAX.)
  LH5749: 70 ns (MAX.)
- Low power consumption:
  394 mW/(MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- High speed programming:
  SHARP original programming algorithm
  (32 second programming)
- Pin compatible with Bipolar PROM
- Packages:
  EPROM
  24-pin, 600-mil CERDIP
  OTPROM
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 300-mil SDIP
- JEDEC standard pinout (CERDIP/DIP)

DESCRIPTION

The LH5749J is a high-performance 64K, UV erasable, electrically programmable read-only-memory, organized as 8,192 × 8 bits. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming only 75 mA.

The LH5749J is packaged in 24-pin CERDIP which is pin-compatible to bipolar PROM.

The LH5749 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

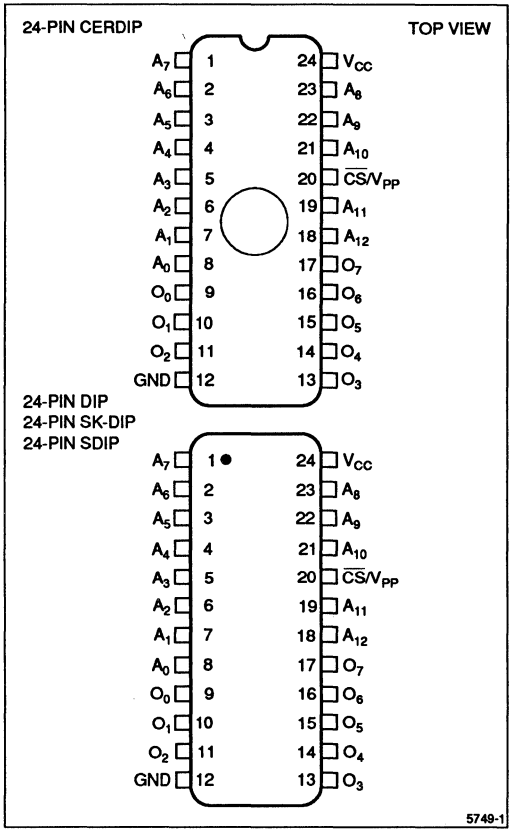


Figure 1. Pin Connections for CERDIP, DIP, SK-DIP and SDIP Packages

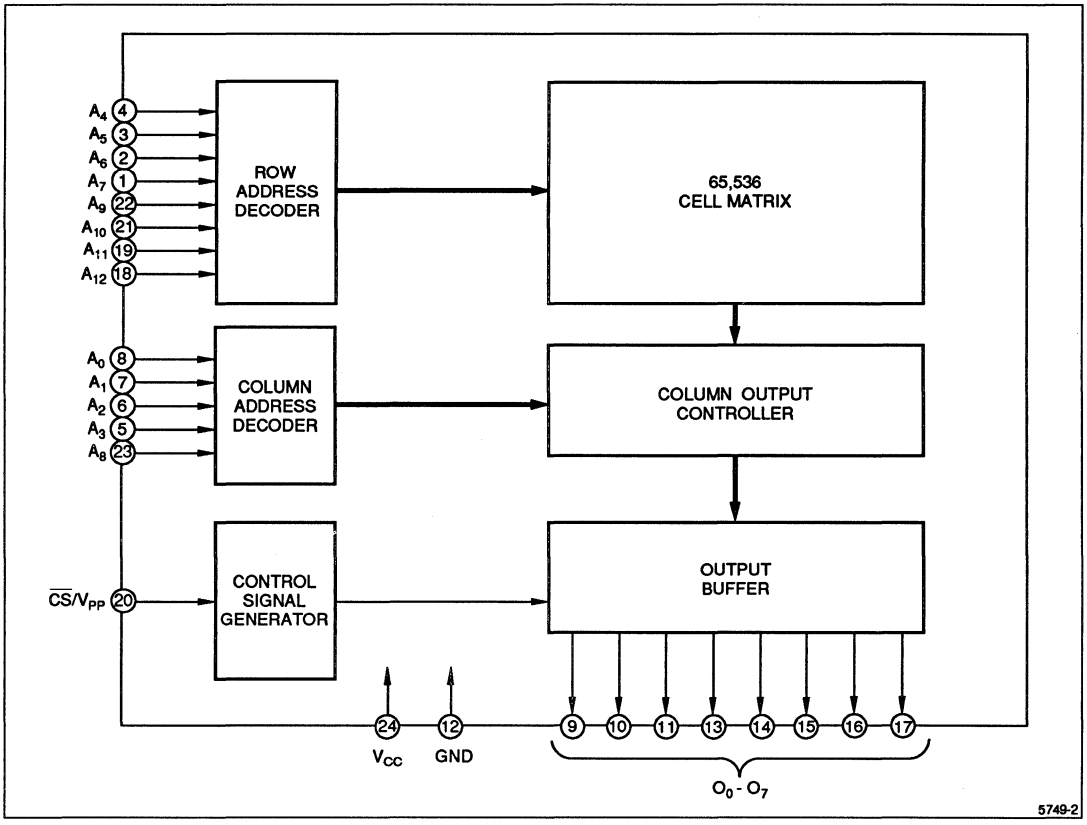


Figure 2. LH5749/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{12}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CS}/V_{PP}$	Chip Select/Program input	

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	CS/V_{PP}	V_{CC}	NOTE
Read	Read	Data out	L	+5 V	1
	Output disable	High-Z	H	+5 V	
Program	Program	Data in	+13 V	+6 V	
	Program inhibit	High-Z	H	+6 V	1
	Program verify	Data out	L	+6 V	

NOTE:
1. H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	$\overline{CS}/V_{PP}$	-0.6 to +14.0		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input "Low" voltage	V_{IL}	-0.1		0.8	
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	CMOS input			75	mA	1, 2
	I_{CC2}	TTL input			75	mA	1, 3
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} + 0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH5749J-55		LH5749J-70 LH5749/D/T-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address valid to output valid	t_{ACC}		55		70	ns
Chip select to output valid	t_{CS}		25		25	ns
Chip disable to output in High Z	t_{DF}	0	20	0	25	ns
Output hold from address	t_{OH}	10		10		ns

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

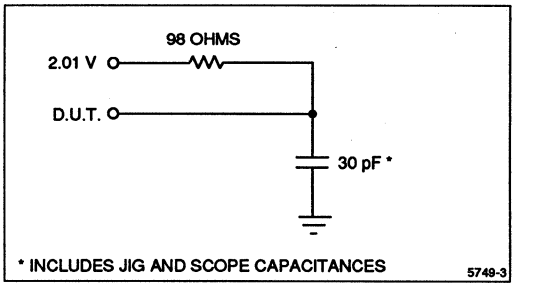


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

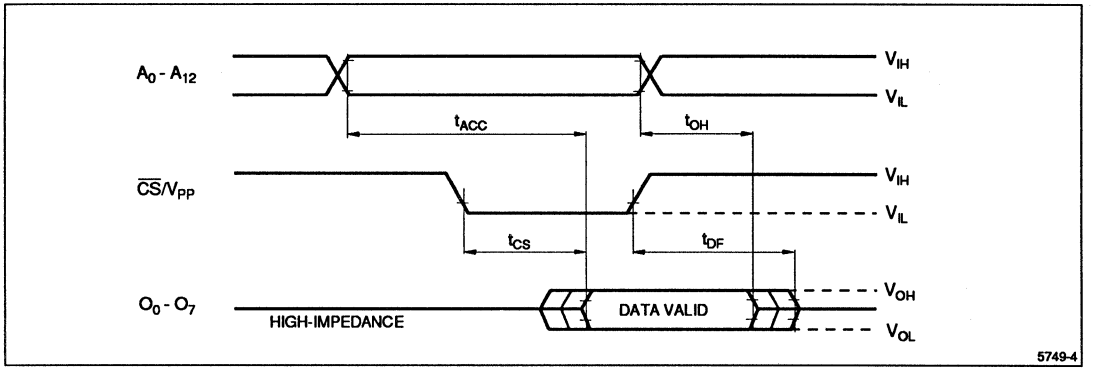


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
Program voltage	$\overline{CS}/V_{PP}$	12.7	13.0	13.3	V
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, $\overline{CS}/V_{PP}$ = 13.0 ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
$\overline{CS}/V_{PP}$ current	I_{PP}	Programming			75	mA
V_{CC} supply current	I_{CC}				75	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V

NOTES:
1. The program pulse $\overline{CS}/V_{PP}$ must be applied after V_{CC} is stable and inhibited before V_{CC} is turned off.
2. $\overline{CS}/V_{PP}$ must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (Program mode)

(V_{CC} = 6.0 V ± 0.25 V, $\overline{CS}/V_{PP}$ = 13.0 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
$\overline{CS}/V_{PP}$ rise time	t_R	1		100	µs
$\overline{CS}/V_{PP}$ fall time	t_F	1		100	µs
Data setup time	t_{DS}	2			µs
Chip select delay time	t_{CS}			30	ns
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Output disable time	t_{DF}			30	ns
V_{CC} setup time	t_{VCS}	2			µs
$\overline{CS}/V_{PP}$ pulse width	t_{PW}	0.95	1.0	1.05	ms
Add $\overline{CS}/V_{PP}$ pulse width *	t_{OPW}	2.85		78.75	ms
Program pulse count	N	1		25	TIMES

* This width is defined by the Program Flowchart (Figure 6).

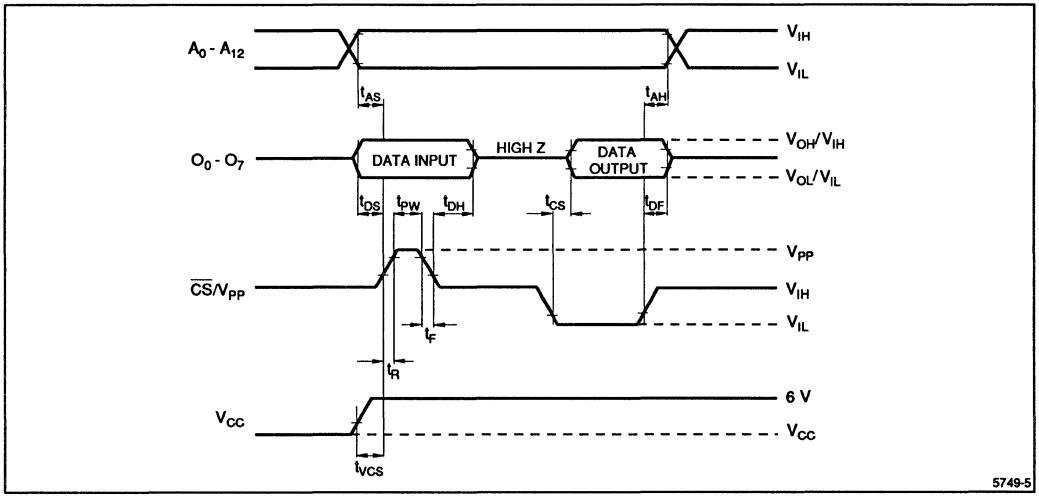


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see Erasure section), the LH5749 and LH5749J have all 8192 × 8 bits in the "1", or high state. "0's" are loaded into the LH5749 and LH5749J through the procedure of programming.

The programming mode is entered when +13.0 V is applied to the $\overline{CS}/V_{PP}$ pin. A 0.1 µF capacitor between $\overline{CS}/V_{PP}$ and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH5749J to an ultraviolet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH5749J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH5749J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH5749J and similar devices, will erase with light sources having wavelength shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH5749J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will gradually erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

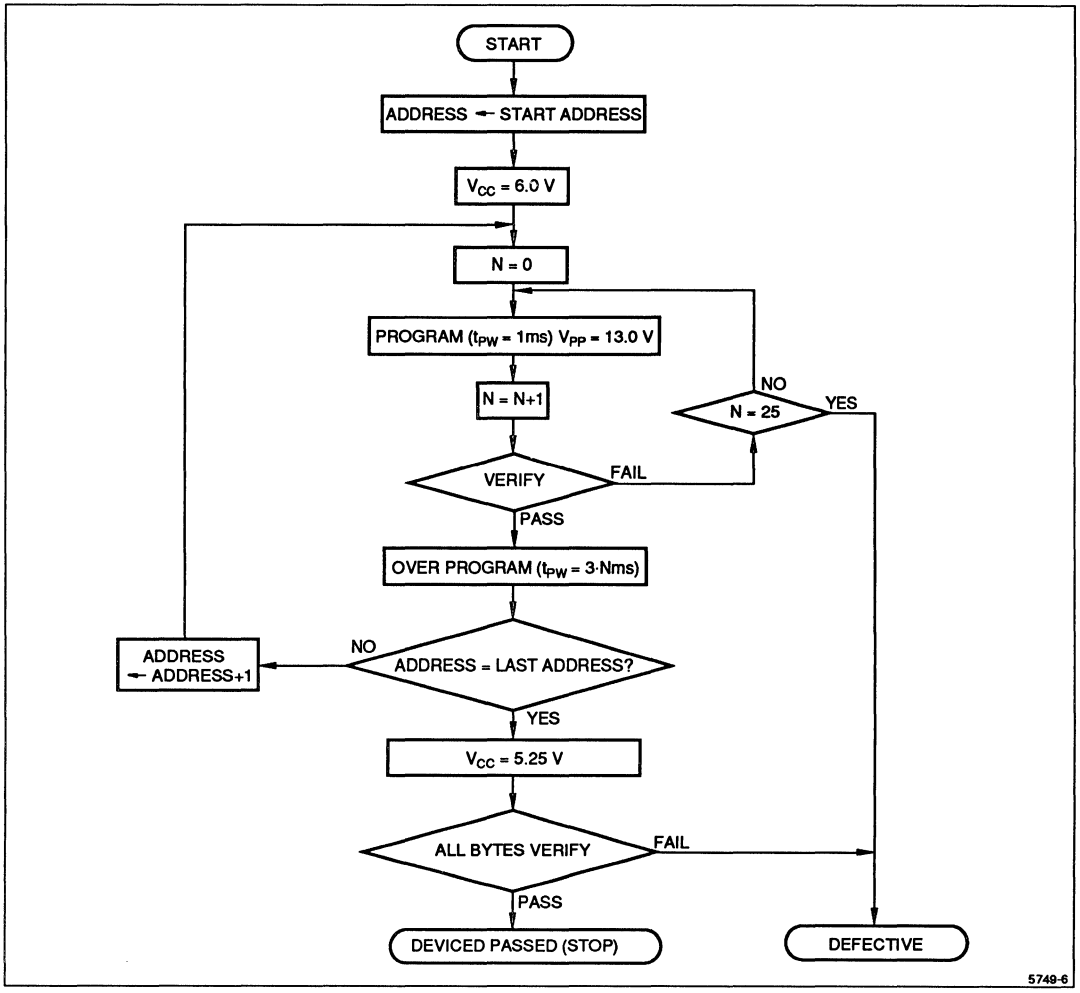
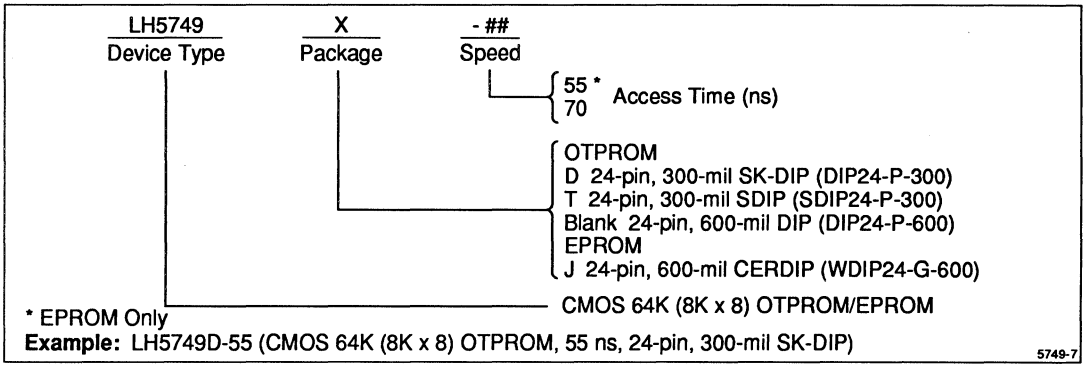


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH5762/J

CMOS 64K (8K × 8) OTPROM/EPROM

FEATURES

- 8,192 × 8 bit organization
- Access times:
  LH5762J: 55/70 ns (MAX.)
  LH5762: 70 ns (MAX.)
- Single +5 V power supply
- Low power consumption:
  Operating: 394 mW (MAX.)
  Standby: 78.75 mW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- High speed programming:
  Compatible to INTEL intelligent programming™ algorithm
  (32 second programming)
- Pin compatible with the i2764
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
- JEDEC standard pinout

DESCRIPTION

The LH5762J is a high-performance 64K, UV erasable, electrically programmable read-only-memory, organized as 8,192 × 8 bits. It is manufactured in an advanced CMOS technology, which allows it to operate at Bipolar speeds while consuming only 75 mA.

The LH5762J has very high output drive capability. It can source 4 mA and sink 16 mA per output.

The LH5762J is configured in the standard EPROM pinout which provides an easy upgrade path for systems that are currently using standard EPROMs.

The LH5762 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

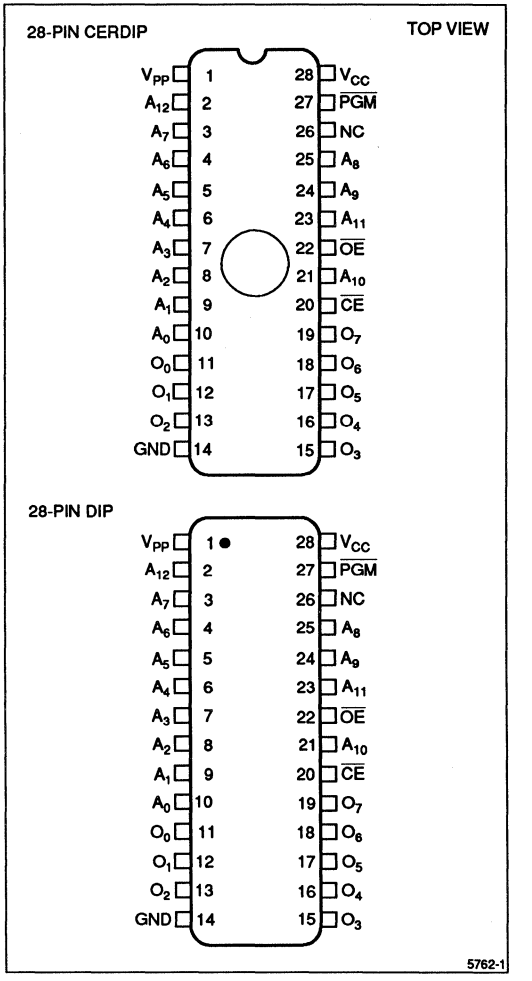


Figure 1. Pin Connections for CERDIP and DIP Packages

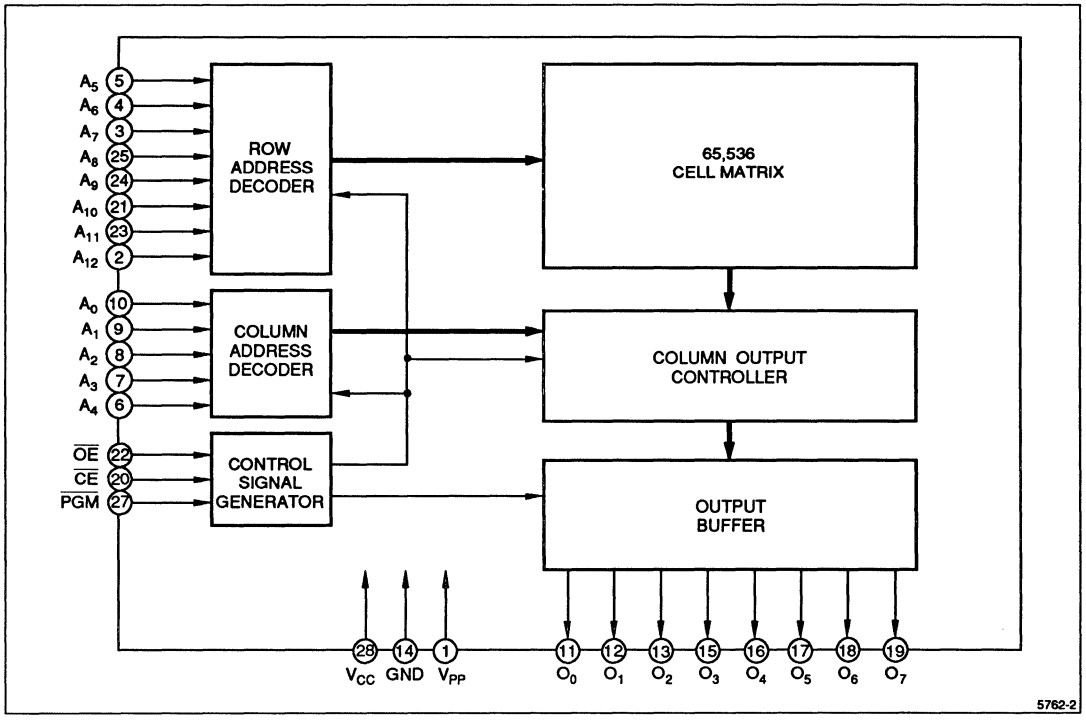


Figure 2. LH5762/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{12}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	
$\overline{PGM}$	Program input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	H	+5 V	+5 V
	Output disable	High-Z	L	H	H	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6 V	+12.5 V
	Program verify	Data out	L	L	H	+6 V	+12.5 V
	Program inhibit	High-Z	H	X	X	+6 V	+12.5 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75	5.0	5.25	V
	V_{PP}	4.75	5.0	5.25	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V, CMOS input			15	mA	
	I_{SB2}	$\overline{CE}$ = V_{IH}, TTL input			20	mA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			75	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			75	mA	1, 3
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} + 0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS input: V_{IN} = GND ± 0.3 V, or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 5%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH5762J-55		LH5762J-70 LH5762-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		55		70	ns
$\overline{CE}$ to output delay	t_{CE}		55		70	ns
$\overline{OE}$ to output delay	t_{OE}		25		25	ns
Output enable high to output float	t_{DF}	0	20	0	25	ns
Address to output hold	t_{OH}	10		10		ns

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

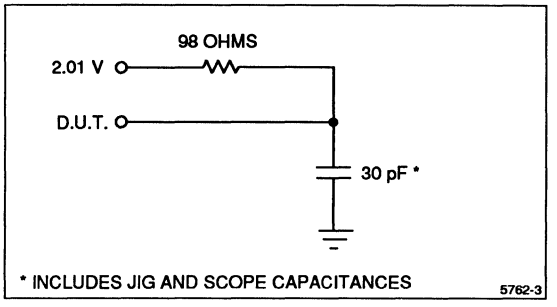


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

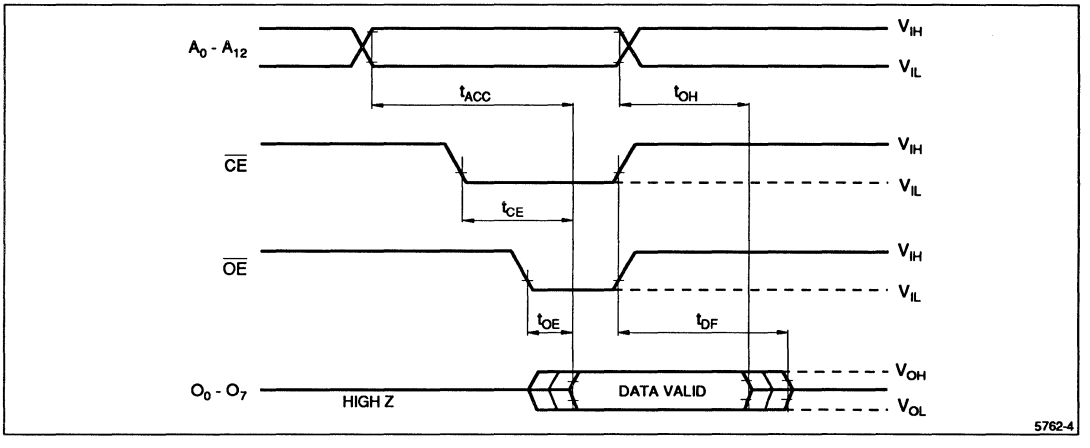


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
	V_{PP}	12.2	12.5	12.8	
Input voltage	V_{IL}	-0.1		0.45	V
	V_{IH}	2.4		V_{CC} + 0.3	

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				75	mA
V_{PP} supply current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}			50	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Address setup time	t_{AS}	2			µs	
Chip enable setup time	t_{CES}	2			µs	
Output enable setup time	t_{OES}	2			µs	
Data setup time	t_{DS}	2			µs	
Address hold time	t_{AH}	0			µs	
Data hold time	t_{DH}	2			µs	
Chip enable to output float delay	t_{DF}	0		150	ns	
Data valid from output enable	t_{OE}			150	ns	
V_{PP} setup time	t_{VPS}	2			µs	
V_{CC} setup time	t_{VCS}	2			µs	
$\overline{PGM}$ pulse width	t_{PW}	0.95	1.0	1.05	ms	
Add $\overline{PGM}$ pulse width	t_{OPW}	2.85		78.75	ms	1
Program pulse count	N	1		25	TIMES	

NOTE:
1. This width is defined by the Program Flowchart (Figure 6).

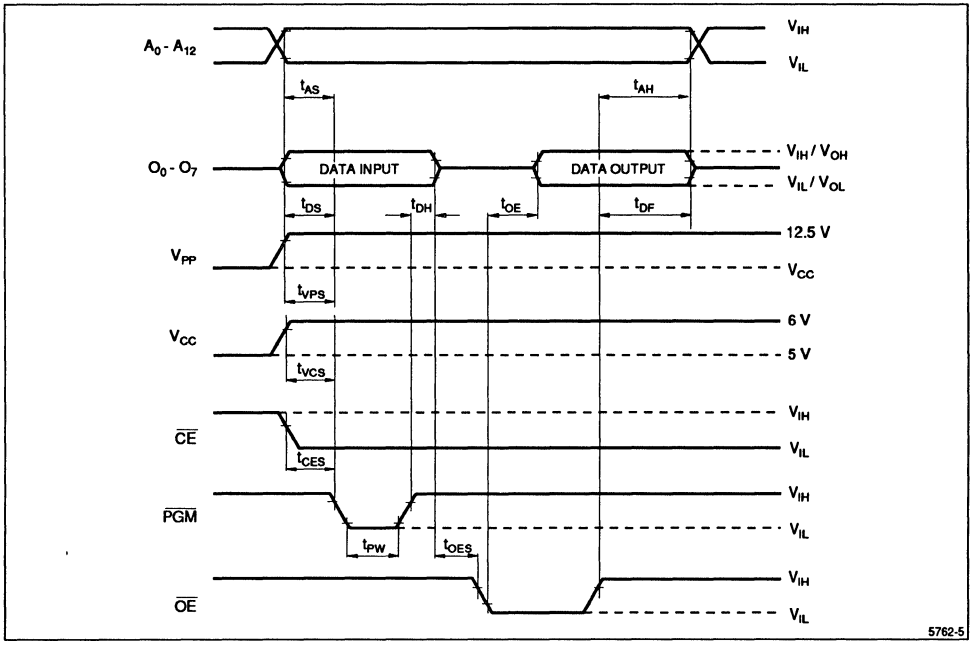


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH5762 and LH5762J have all 8,192 × 8 bits in the "1", or high state. "0's" are loaded into the LH5762 and LH5762J through the procedure of programming.

The programming mode is entered when +12.5 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH5762J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH5762J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH5762J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH5762J and similar devices, will erase with light sources having wavelength shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH5762J. Exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.

4. Removing or inserting the device while 12.5 volts is supplied may harm the reliability of the device.

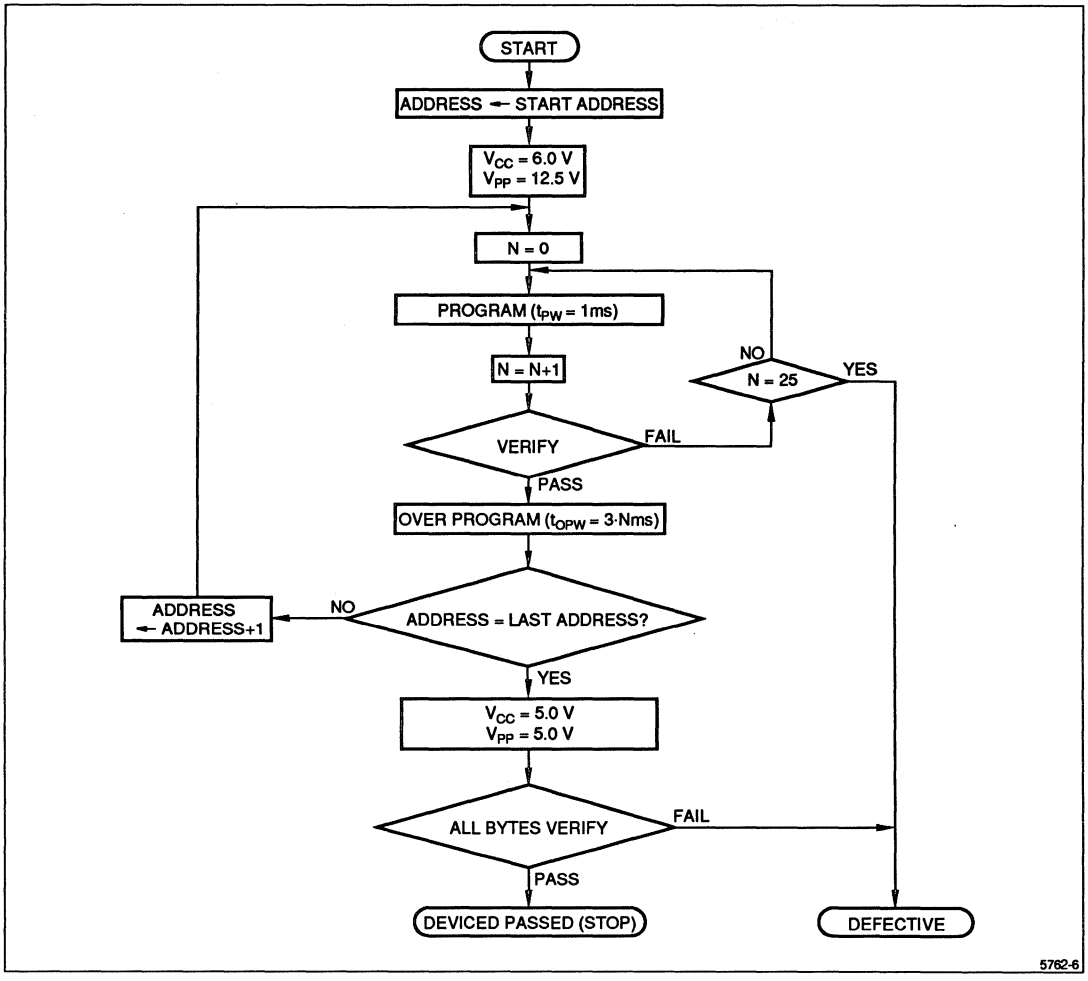
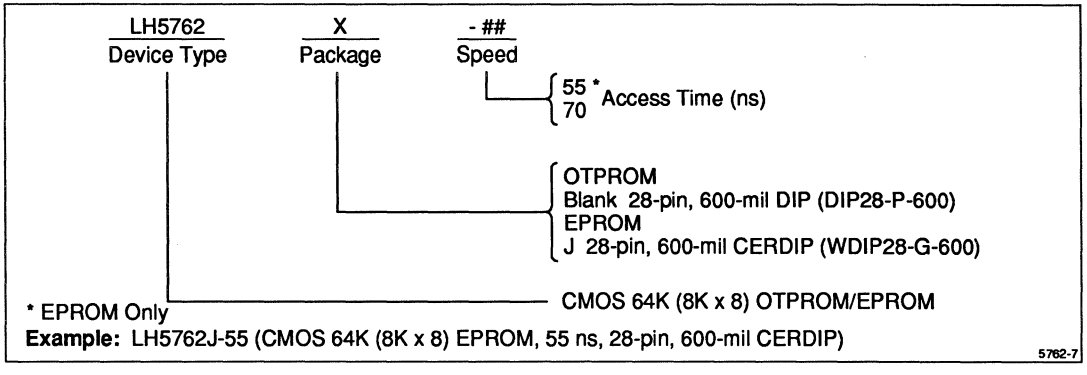


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH5763/J

CMOS 64K (8K × 8) OTPROM/EPROM

FEATURES

- 8,192 × 8 bit organization
- Access times:
  LH5763J: 70/90 ns (MAX.)
  LH5763: 90 ns (MAX.)
- Single +5 V power supply
- Low power consumption:
  Operating: 315 mW (MAX.)
  Standby: 1.05 mW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- High speed programming:
  Compatible to INTEL intelligent programming™ algorithm
  (32 second programming)
- Pin compatible with the i2764
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
- JEDEC standard pinout

DESCRIPTION

The LH5763J is a CMOS UV erasable and electrically programmable read-only-memory, organized as 8,192 × 8 bits. It is pin compatible with the Intel i2764 and the SHARP LH5764J, and designed to have fast access time.

The LH5763 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

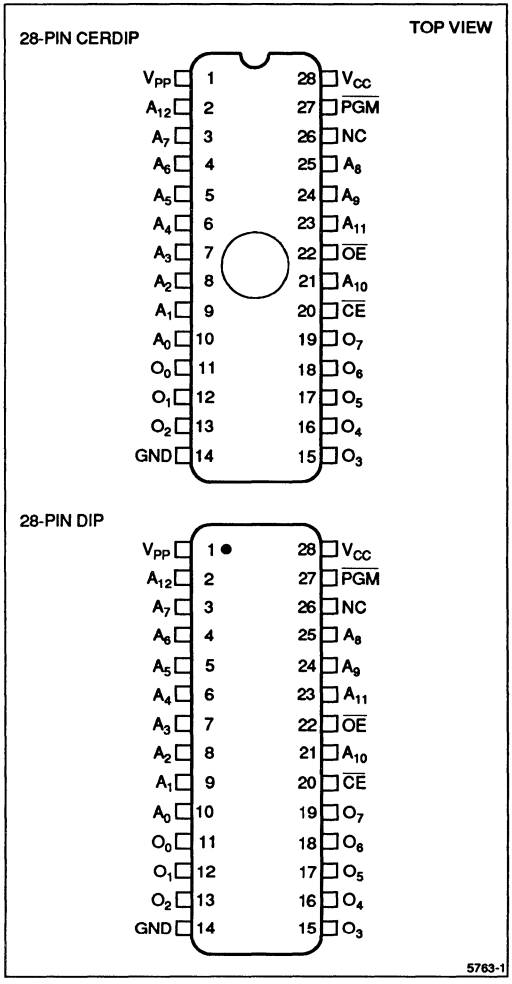


Figure 1. Pin Connections for CERDIP and DIP Packages

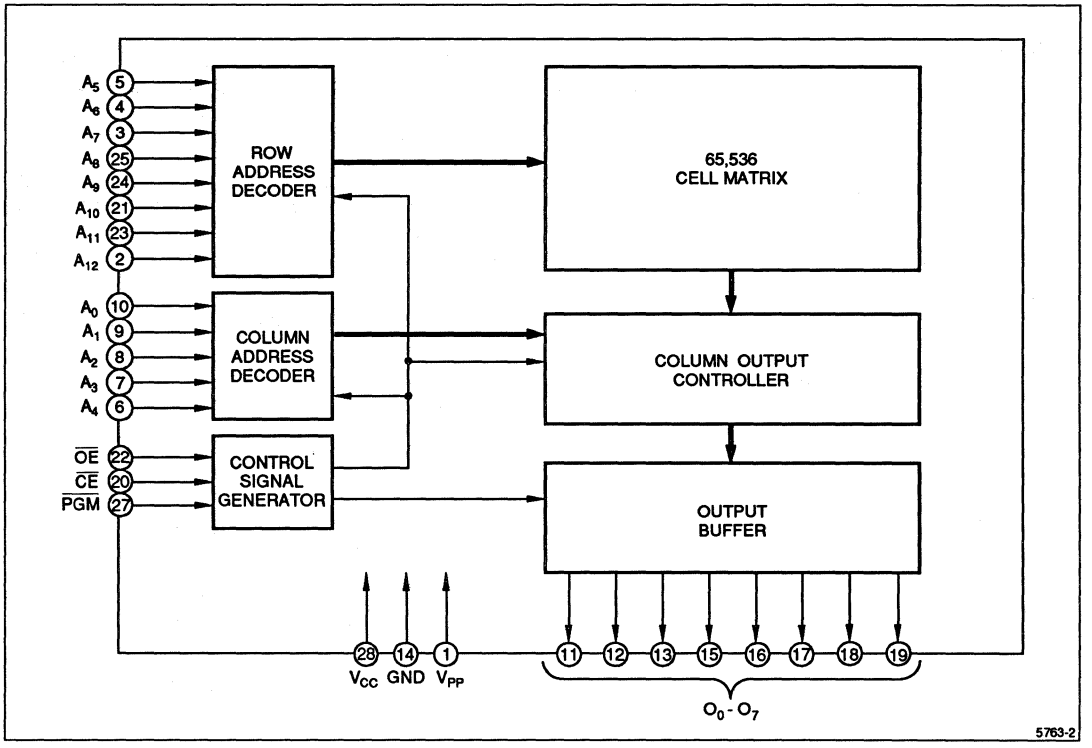


Figure 2. LH5763/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{12}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	
$\overline{PGM}$	Program input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	H	+5 V	+5 V
	Output disable	High-Z	L	H	H	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6 V	+12.5 V
	Program verify	Data out	L	L	H	+6 V	+12.5 V
	Program inhibit	High-Z	H	X	X	+6 V	+12.5 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75	5.0	5.35	V
	V_{PP}	4.75	5.0	5.25	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3V			60	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			60	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			200	µA	2
	I_{SB2}	$\overline{CE}$ = V_{IH}			10	mA	3

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS input: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 5%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH5763J-70		LH5763J-90 LH5763-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		70		90	ns
$\overline{CE}$ to output delay	t_{CE}		70		90	ns
$\overline{OE}$ to output delay	t_{OE}		25		30	ns
Output enable high to output float	t_{DF}	0	25	0	30	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	2.0 V, 1.0 V
Output reference level	2.0 V, 0.8 V

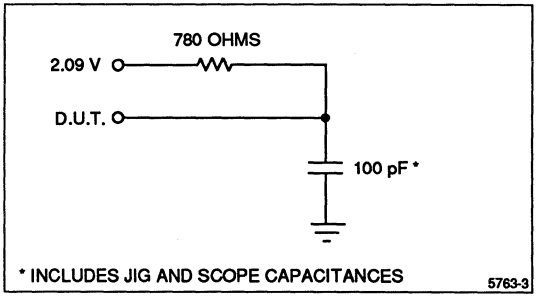


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

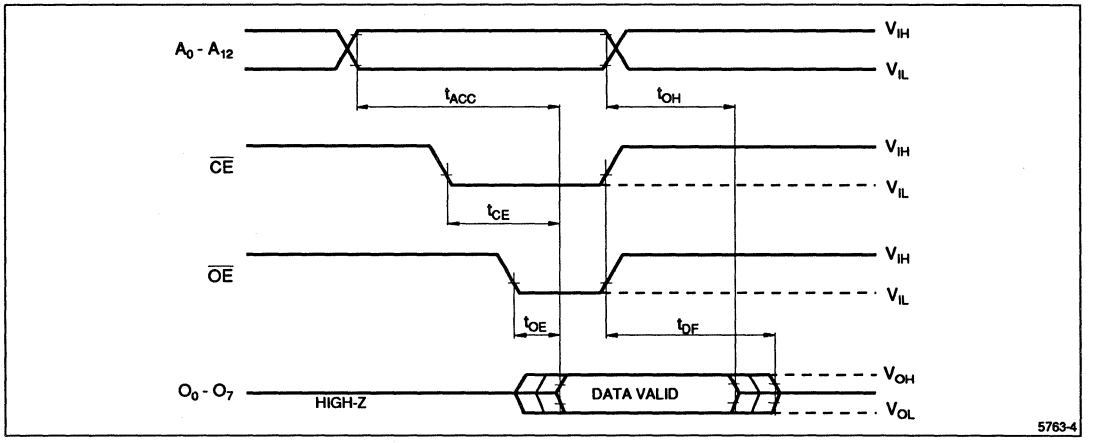


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
	V_{PP}	12.2	12.5	12.8	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = V_{CC}$ or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				60	mA
V_{PP} supply current	I_{PP}	$\overline{CE} = \overline{PGM} = V_{IL}$			50	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	$\overline{PGM}$ - Address	2			µs
Chip enable setup time	t_{CES}	$\overline{PGM}$ - $\overline{CE}$	2			µs
Output enable setup time	t_{OES}	Data - $\overline{CE}$	2			µs
Data setup time	t_{DS}	$\overline{PGM}$ - Data	2			µs
Address hold time	t_{AH}	$\overline{OE}$ - Address	0			µs
Data hold time	t_{DH}	$\overline{PGM}$ - Data	2			µs
Chip enable to output float delay	t_{DF}				150	ns
Data valid from output enable	t_{OE}				150	ns
V_{PP} setup time	t_{VPS}		2			µs
V_{CC} setup time	t_{VCS}		2			µs
Program pulse width	t_{PW}		0.95	1	1.05	ms
Add $\overline{PGM}$ pulse width *	t_{OPW}		2.85		78.75	ms
Program pulse count	N		1		25	TIMES

* This width is defined by the Program Flowchart (Figure 6).

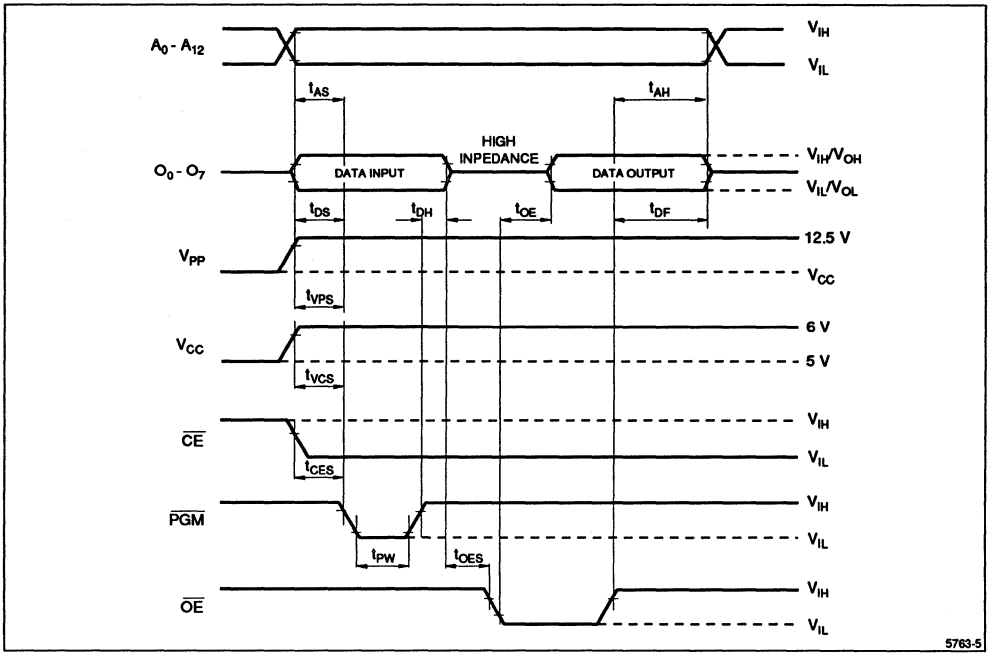


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH5763 and LH5763J have all 8,192 × 8 bits in the "1", or high state. "0's" are loaded into the LH5763 and LH5763J through the procedure of programming.

The programming mode is entered when +12.5 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH5763J to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase an LH5763J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH5763J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH5763J and similar devices will erase with light sources having wave-length shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH5763J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.

4. Removing or inserting the device while 12.5 volts is supplied may harm the reliability of the device.

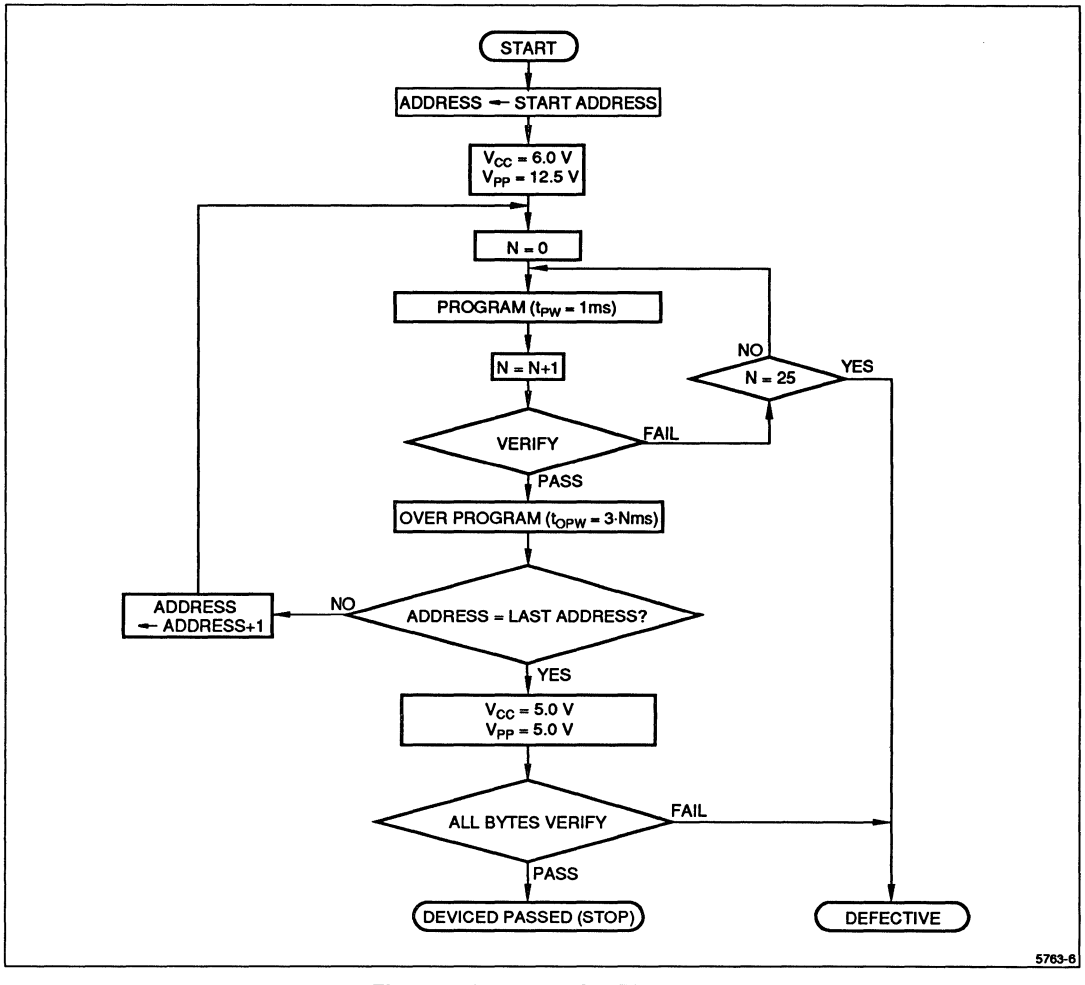
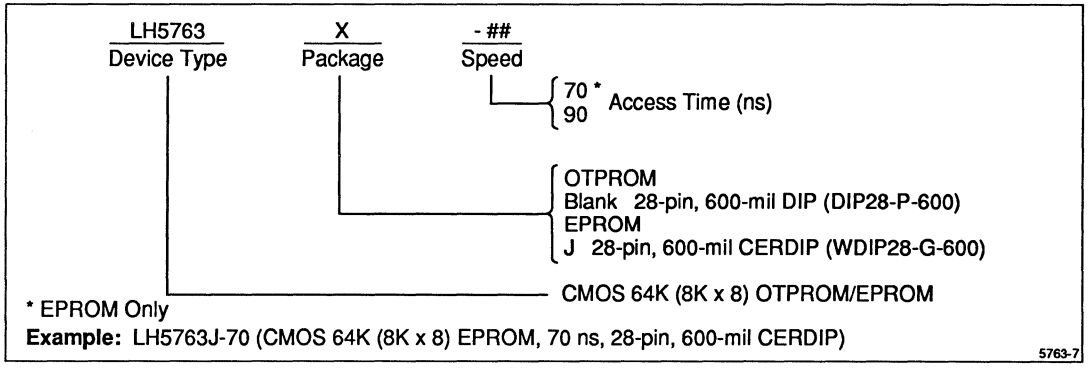


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH5764/J

CMOS 64K (8K × 8) OTPROM/EPROM

FEATURES

- 8,192 × 8 bit organization
- Access times:
  LH5764J: 200/250 ns (MAX.)
  LH5764: 200/250 ns (MAX.)
- Single +5 V power supply
- Low power consumption:
  Operating: 165 mW (MAX.)
  Standby: 550 μW (MAX.)
- High speed programming:
  t_{PW} = 0.1 ms (V_{PP} = 12.75 V) or
  t_{PW} = 1 ms (V_{PP} = 12.5 V)
  Compatible to INTEL quick pulse programming™ algorithm
  (1 second programming)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Pin compatible with the i2764
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
- JEDEC standard pinout (CERDIP/DIP)

DESCRIPTION

The LH5764J is a CMOS UV erasable and electrically programmable read-only-memory, organized as 8,192 × 8 bits. It provides low power consumption in standby mode.

The LH5764 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

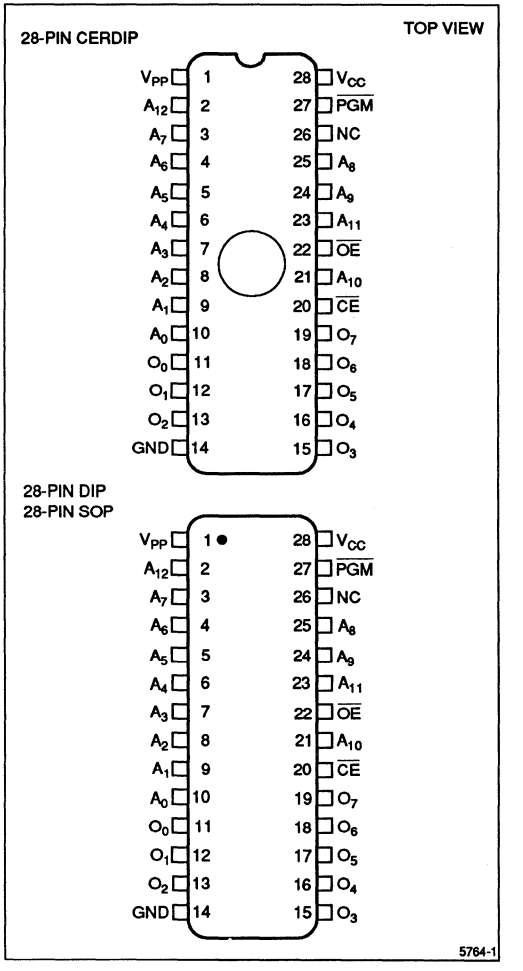


Figure 1. Pin Connections for CERDIP, DIP, and SOP Packages

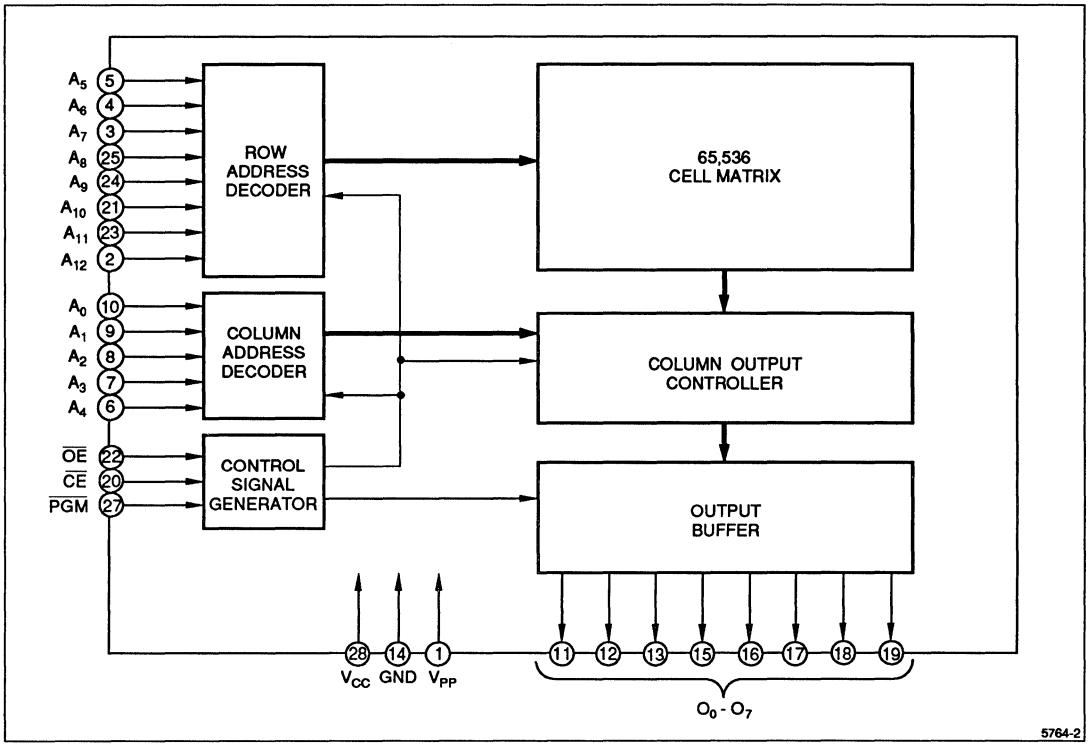


Figure 2. LH5764/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{12}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	
$\overline{PGM}$	Program input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	H	+5 V	+5 V
	Output disable	High-Z	L	H	H	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6.25 V	+12.75 V
	Program verify	Data out	L	L	H	+6.25 V	+12.75 V
	Program inhibit	High-Z	H	X	X	+6.25 V	+12.75 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	4.5	5.0	5.5	V
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			25	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			30	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA	
	I_{SB2}	$\overline{CE}$ = V_{IH}			1	mA	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS input: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH5764J-20		LH5764J-25 LH5764/N-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		200		250	ns
$\overline{CE}$ to output delay	t_{CE}		200		250	ns
$\overline{OE}$ to output delay	t_{OE}		55		65	ns
Output enable high to output float	t_{DF}	0	55	0	65	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

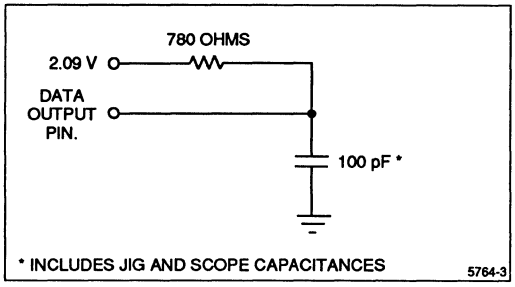


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

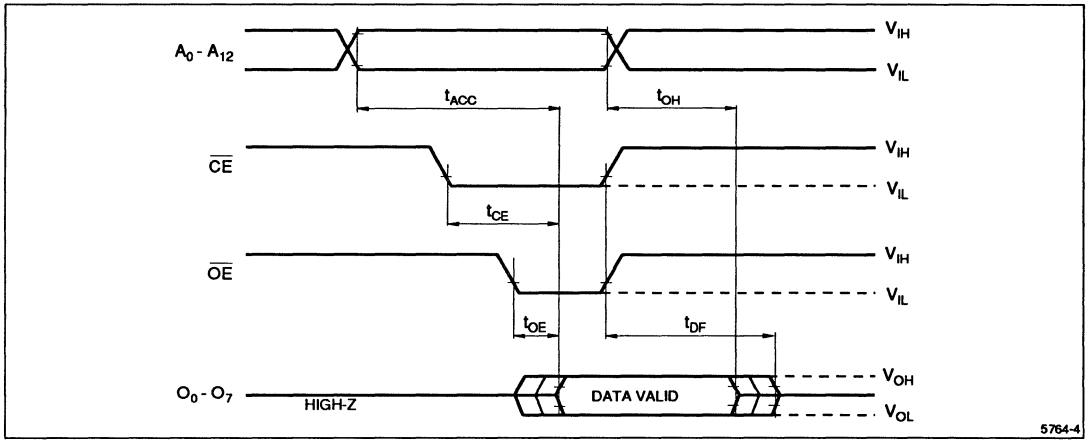


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.25	6.5	V
	V_{PP}	12.2	12.75	13.0	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 5.75 V to 6.5 V, V_{PP} = 12.2 V to 13.0 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				30	mA
V_{PP} supply current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}			30	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C) (Note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Chip enable setup time	t_{CES}	2			µs
Output enable setup time	t_{OES}	2			µs
Data setup time	t_{DS}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Chip enable to output float delay	t_{DF}	0		150	ns
Data valid from output enable	t_{OE}			150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
Program pulse width *1, *2	t_{PW}	95	100	105	µs
Program pulse count	N	1		25	TIMES

NOTES:

1. This width is defined by the Program Flowchart (Figure 6).
2. Programmable under conditions V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, t_{PW} = 1 ms ± 0.05 ms

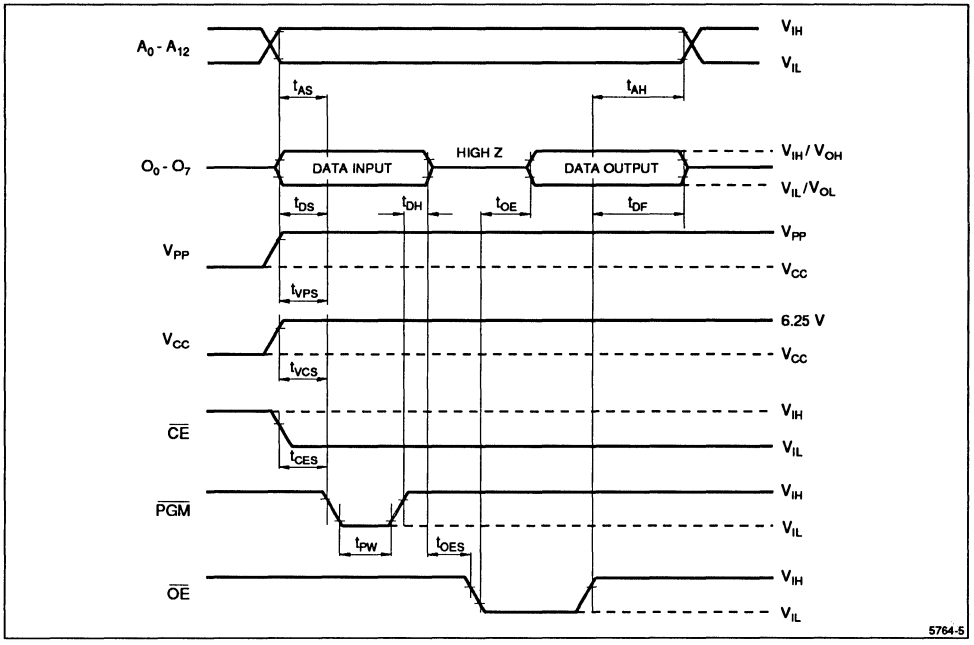


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH5764 and LH5764J have all 8,192 × 8 bits in the "1", or high state. "0's" are loaded into the LH5764 and LH5764J through the procedure of programming.

The programming mode is entered when +12.75 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH5764J to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase an LH5764J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH5764J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH5764J and similar devices will erase with light sources having wave-length shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH5764J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from V_{CC} to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

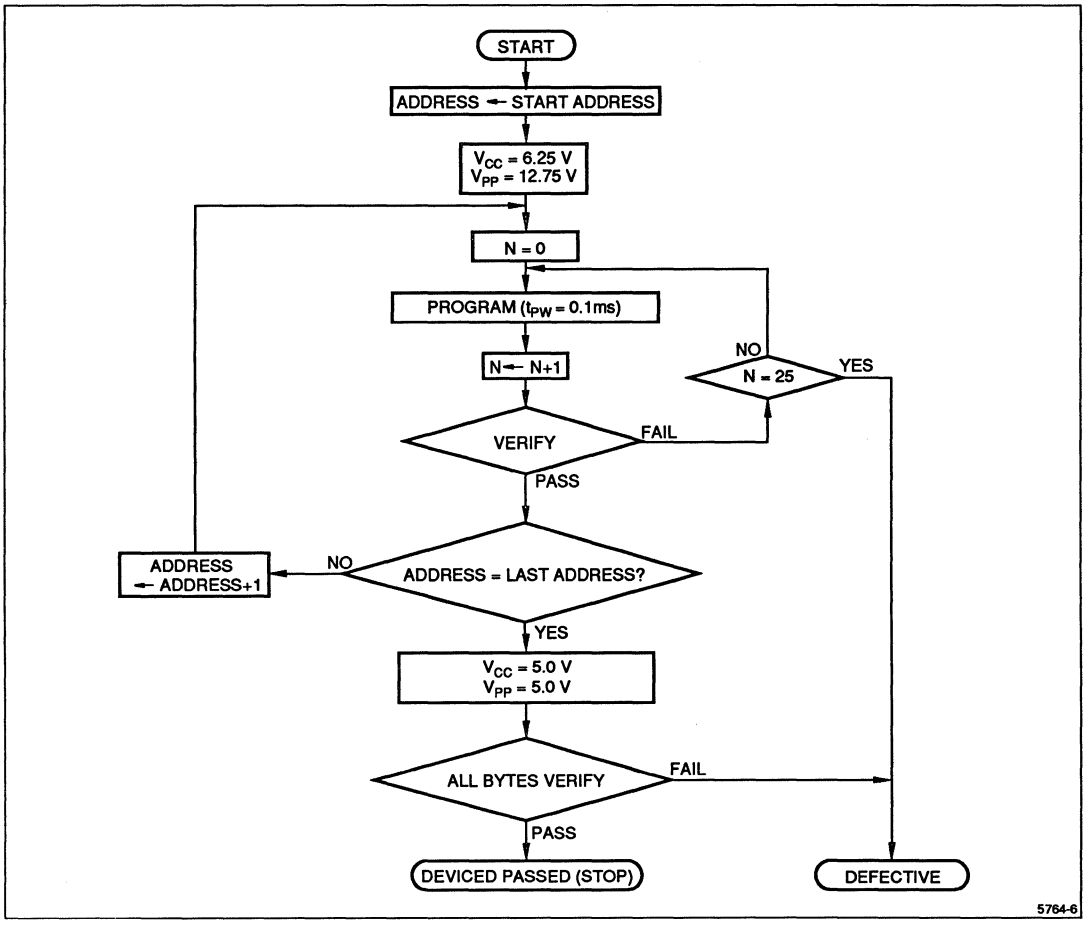
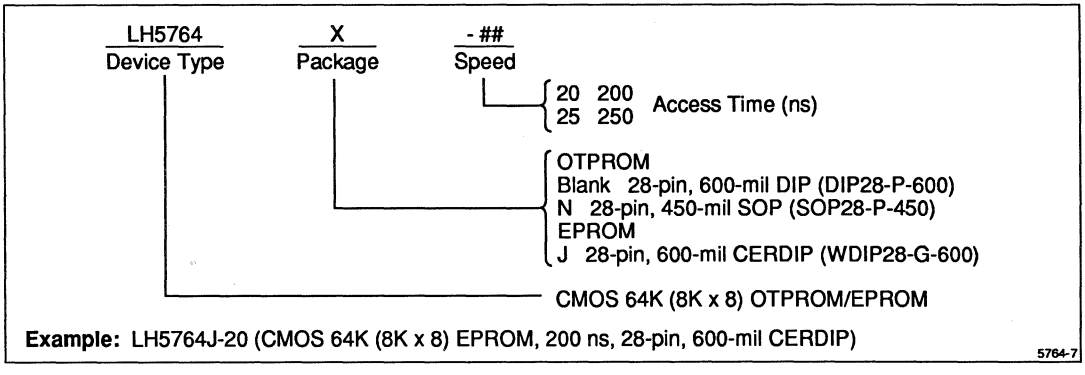


Figure 6. Programming Flowchart

ORDERING INFORMATION



Example: LH5764J-20 (CMOS 64K (8K x 8) EPROM, 200 ns, 28-pin, 600-mil CERDIP)

LH57126/J

CMOS 128K (16K × 8) OTPROM/EPROM

FEATURES

- 16,384 × 8 bit organization
- Access times:
  LH57126J: 70/90 ns
  LH57126: 90 ns
- Single +5 V power supply
- Low power consumption:
  Operating: 394 mW (MAX.)
  Standby: 78.75 mW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- High speed programming
  Compatible to INTEL intelligent programming™ algorithm
  (64 second programming)
- Pin compatible with the i27128
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
- JEDEC standard pinout

DESCRIPTION

The LH57126J is a high-performance 128K, UV erasable, electrically programmable read-only-memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming only 75 mA.

The LH57126J is pin compatible with the Intel i27128 and the SHARP LH57128J, and designed to have fast access time.

The LH57126J is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The LH57126 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

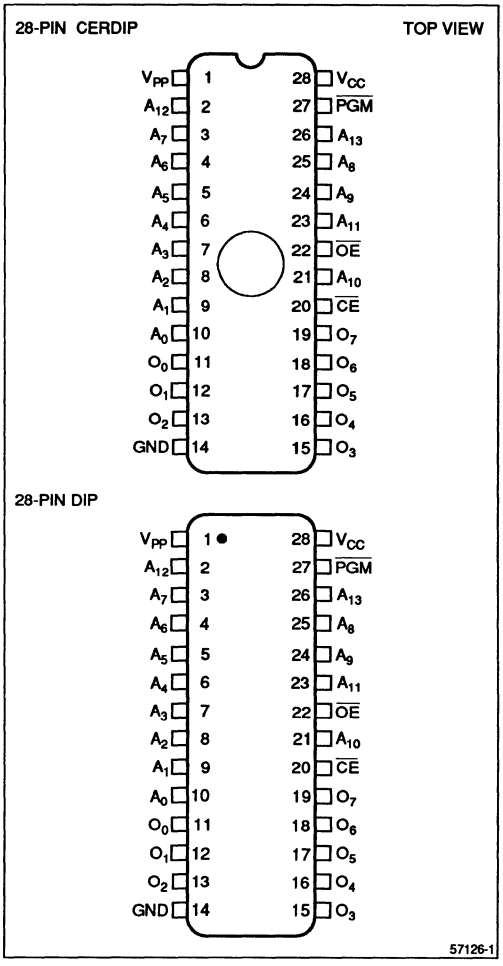


Figure 1. Pin Connections for CERDIP and DIP Packages

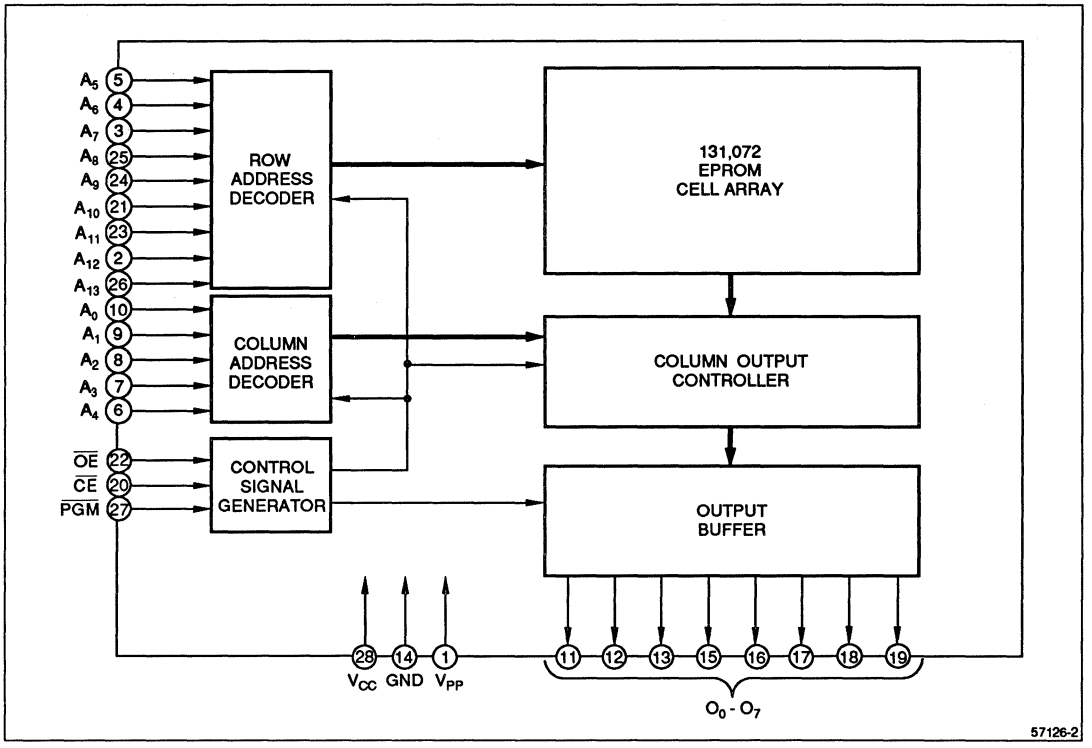


Figure 2. LH57126/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{13}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{PGM}$	Program input	
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	H	+5 V	+5 V
	Output disable	High-Z	L	H	H	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6 V	+12.5 V
	Program verify	Data out	L	L	H	+6 V	+12.5 V
	Program inhibit	High-Z	H	X	X	+6 V	+12.5 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Pin voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75	5.0	5.25	V
	V_{PP}	4.75	5.0	5.25	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3V			75	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			75	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3V			15	mA	4
	I_{SB2}	$\overline{CE}$ = V_{IH}			20	mA	5

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}
4. All inputs are fixed at CMOS level.
5. All inputs are fixed at TTL level.

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V + 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57126J-70		LH57126J-90 LH57126-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		70		90	ns
$\overline{CE}$ to output delay	t_{CE}		70		90	ns
$\overline{OE}$ to output delay	t_{OE}		25		30	ns
Output enable high to output float	t_{DF}	0	25	0	30	ns
Address to output hold	t_{OH}	10		10		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

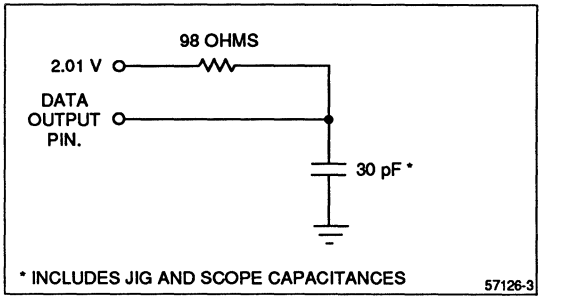


Figure 4. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

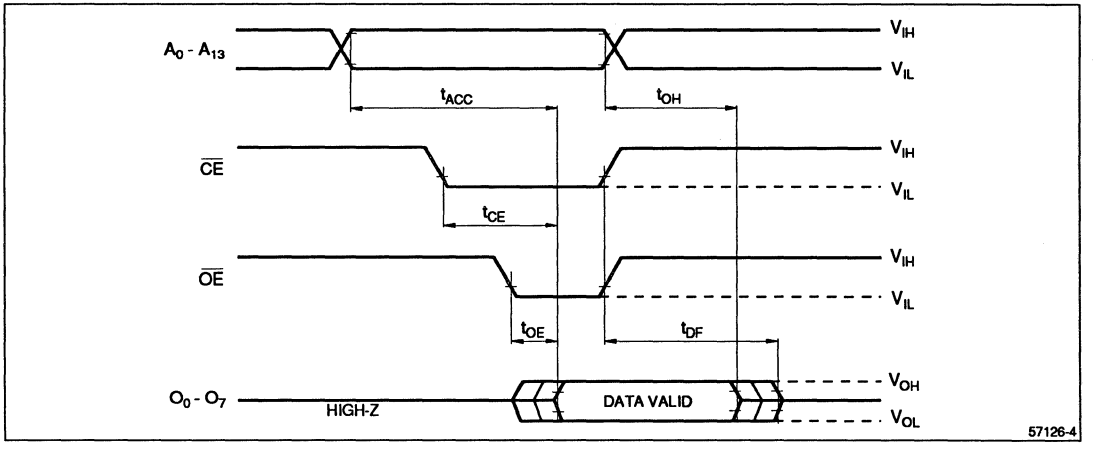


Figure 3. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
	V_{PP}	12.2	12.5	12.8	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V , T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				50	mA
V_{PP} supply current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}			75	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Chip enable setup time	t_{CES}	2			µs
Output enable setup time	t_{OES}	2			µs
Data setup time	t_{DS}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Chip enable to output float delay	t_{DF}	0		150	ns
Data valid from output enable	t_{OE}			150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
$\overline{PGM}$ pulse width	t_{PW}	0.95	1.0	1.05	ms
Add $\overline{PGM}$ pulse width*	t_{OPW}	2.85		78.75	ms
Program pulse count	N	1		25	TIMES

* This width is defined by the Program Flowchart (Figure 6).

PROGRAMMING

Upon delivery from SHARP or after each erasure (see Erasure section), the LH57126 and LH57126J have all 16,384 × 8 bits in the "1", or high state. "0's" are loaded into the LH57126 and LH57126J through the procedure of programming.

The programming mode is entered when +12.5 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57126J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57126J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH57126J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57126J and similar devices will erase with light sources having wave-length shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57126J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.

4. Removing or inserting the device while 12.5 volts is supplied may harm the reliability of the device.

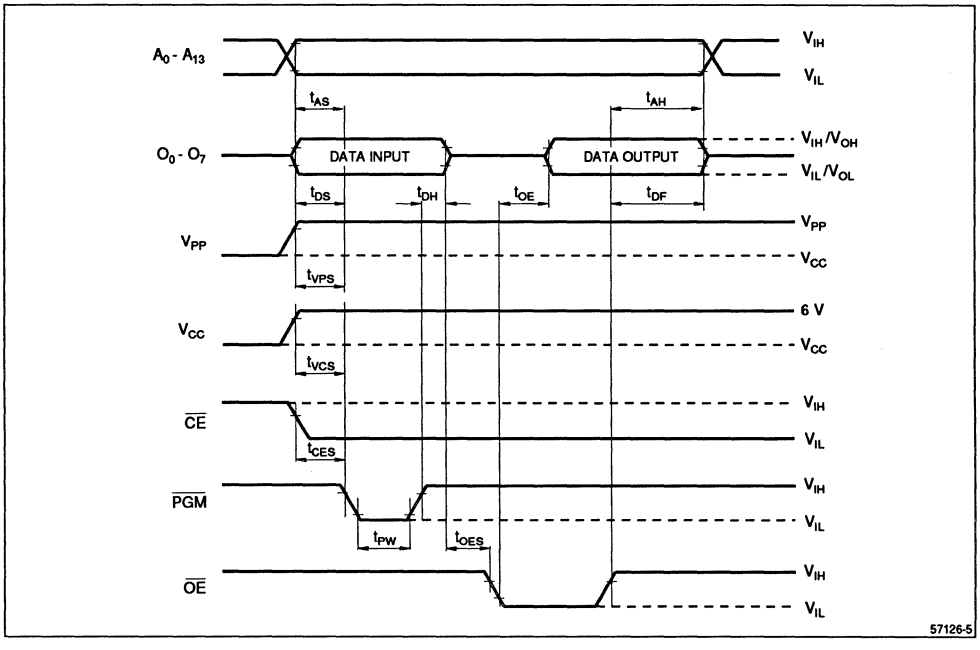


Figure 5. Timing Diagram (Program Mode)

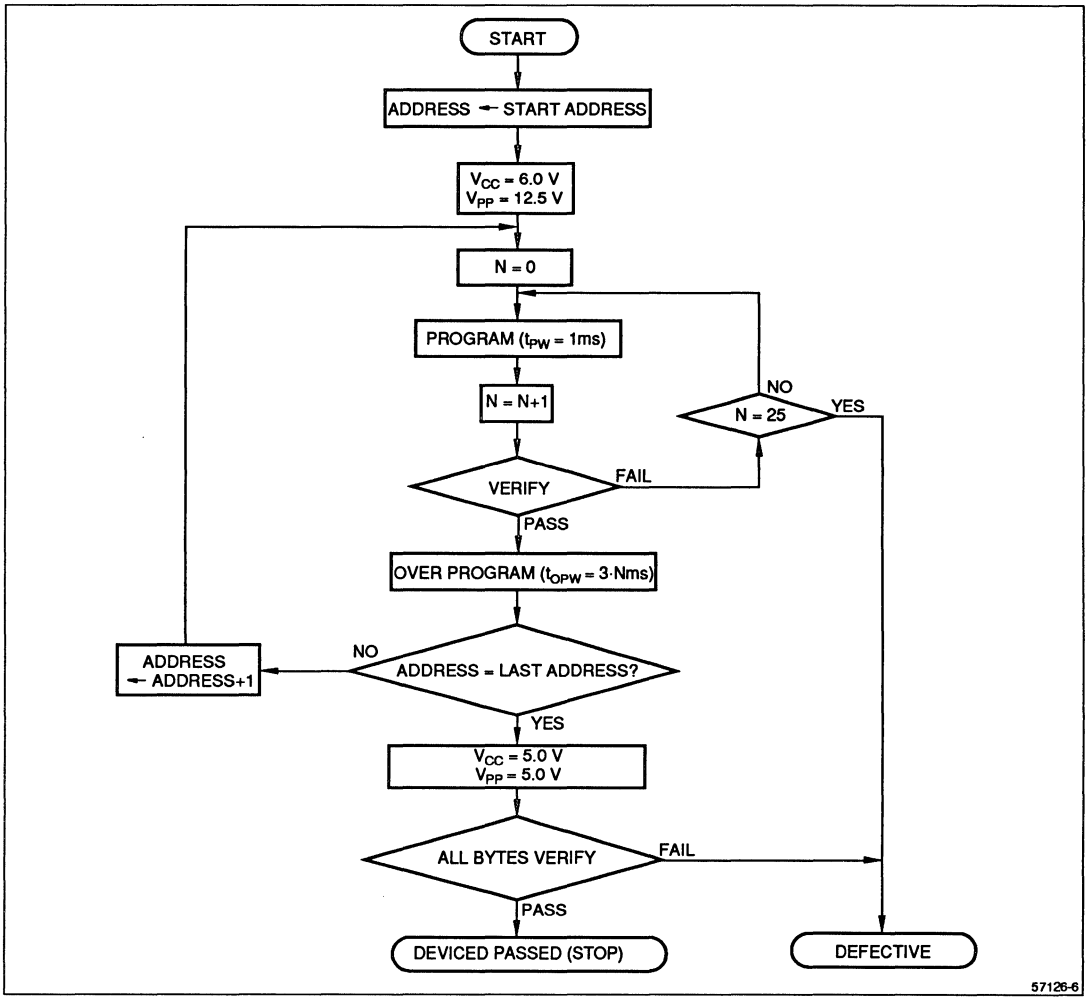
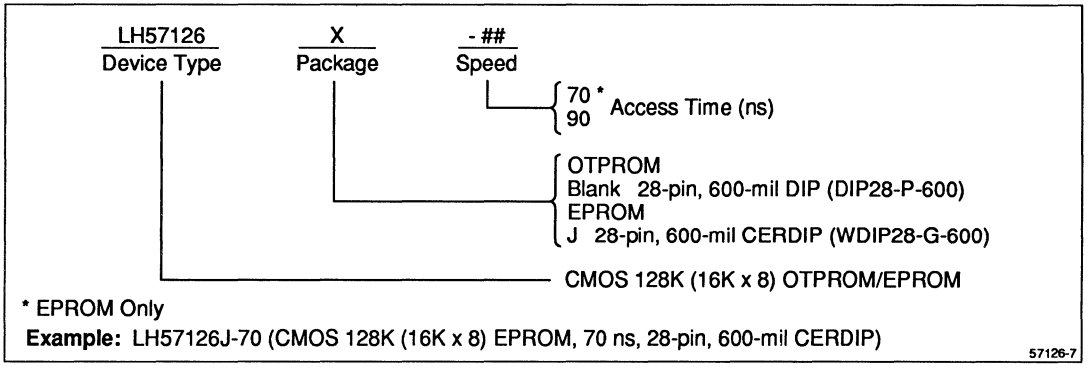


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH57127/J

CMOS 128K (16K × 8) OTPROM/EPROM

FEATURES

- 16,384 × 8 bit organization
- Access times:
  LH57127J: 100 ns (MAX.)
  LH57127: 120 ns (MAX.)
- Single +5 V power supply
- Low power consumption:
  Operating: 315 mW (MAX.)
  Standby: 1.05 mW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- High speed programming:
  Compatible to INTEL intelligent programming™ algorithm
  (64 second programming)
- Pin compatible with i27128
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
- JEDEC standard pinout

DESCRIPTION

The LH57127J is a CMOS UV erasable and electrically programmable read-only-memory, organized as 16,384×8 bits. It is pin compatible with the Intel i27128 and the SHARP LH57128J, and designed to have fast access time.

The LH57127 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

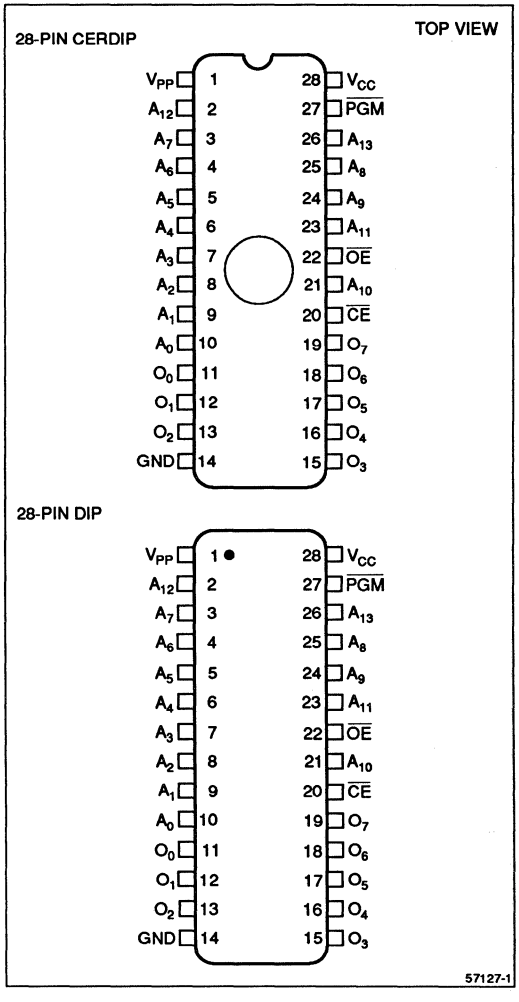


Figure 1. Pin Connections for CERDIP and DIP Packages

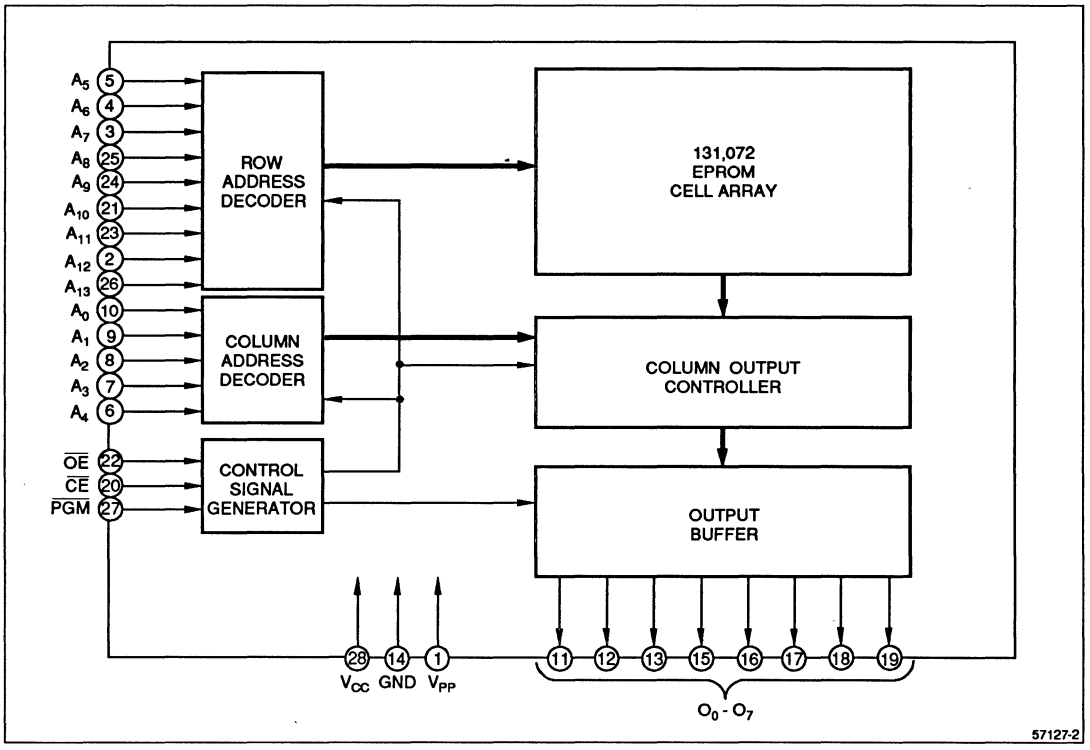


Figure 2. LH57127/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0-A_{13}	Address input	
O_0-O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{PGM}$	Program input	
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	H	+5 V	+5 V
	Output disable	High-Z	L	H	H	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6 V	+12.5 V
	Program verify	Data out	L	L	H	+6 V	+12.5 V
	Program inhibit	High-Z	H	X	X	+6 V	+12.5 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{PP}	4.75	5.0	5.25	V
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			60	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			60	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} Standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			200	µA	
	I_{SB2}	$\overline{CE}$ = V_{IH}			10	mA	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57127J-10		LH57127-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		100		120	ns
$\overline{CE}$ to output delay	t_{CE}		100		120	ns
$\overline{OE}$ to output delay	t_{OE}		30		30	ns
Output enable high to output float	t_{DF}	0	30	0	30	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

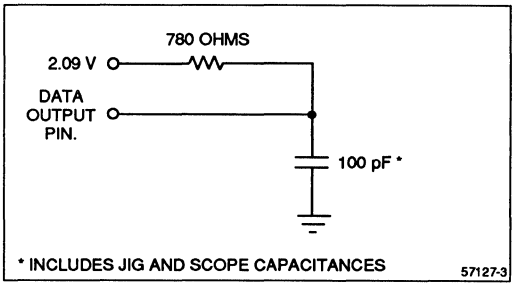


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

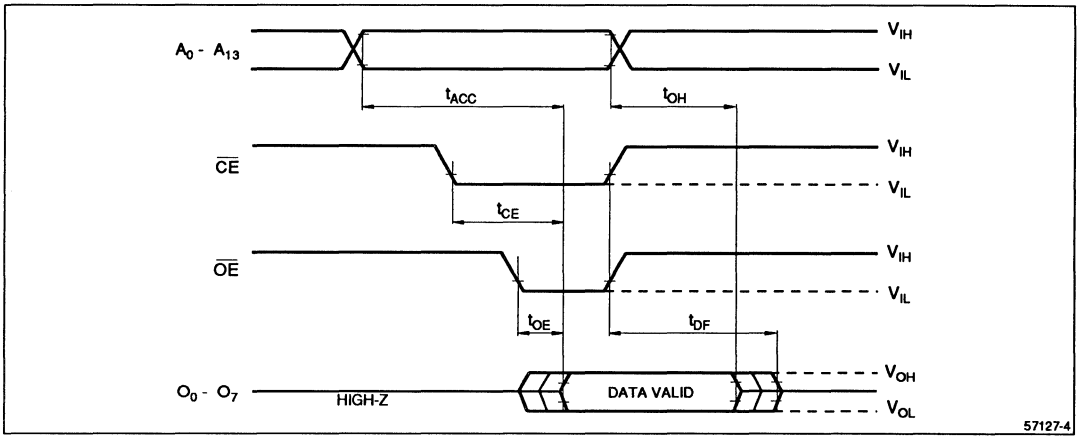


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
	V_{PP}	12.2	12.5	12.8	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				60	mA
V_{PP} supply current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}			50	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Chip enable setup time	t_{CES}	2			µs
Output enable setup time	t_{OES}	2			µs
Data setup time	t_{DS}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Chip enable to output float delay	t_{DF}	0		150	ns
Data valid from output enable	t_{OE}			150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
Program pulse width	t_{PW}	0.95	1	1.05	ms
Add $\overline{PGM}$ pulse width*	t_{OPW}	2.85		78.75	ms
Program pulse count	N	1		25	TIMES

* This width is defined by the Program Flowchart (Figure 6).

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH57127 and LH57127J have all 16,384 × 8 bits in the "1", or high state. "0's" are loaded into the LH57127 and LH57127J through the procedure of programming.

The programming mode is entered when +12.5 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57127J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57127J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH57127J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57127J and similar devices will erase with light sources having wave-length shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57127J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.

4. Removing or inserting the device while 12.5 volts is supplied may harm the reliability of the device.

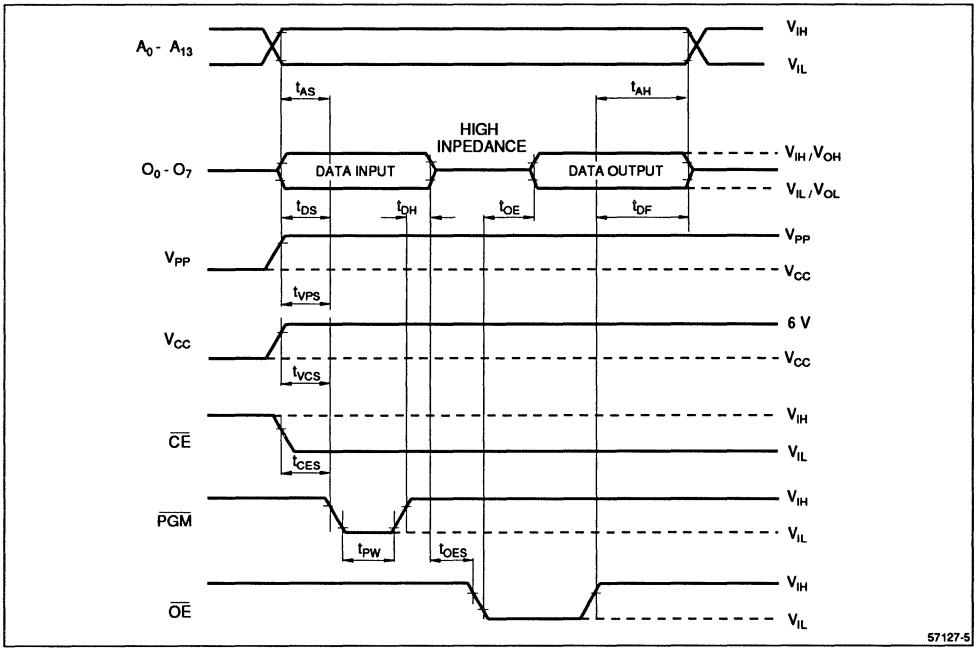


Figure 5. Timing Diagram (Program Mode)

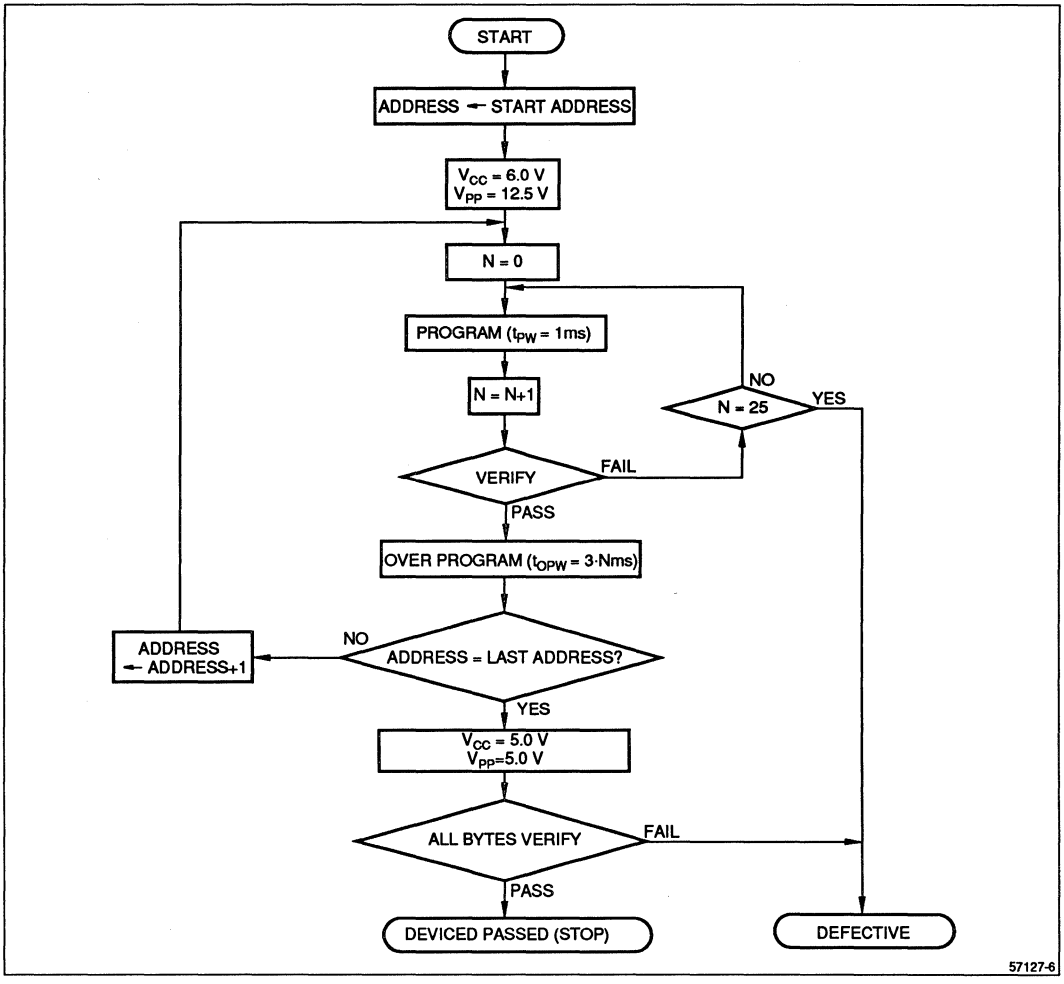
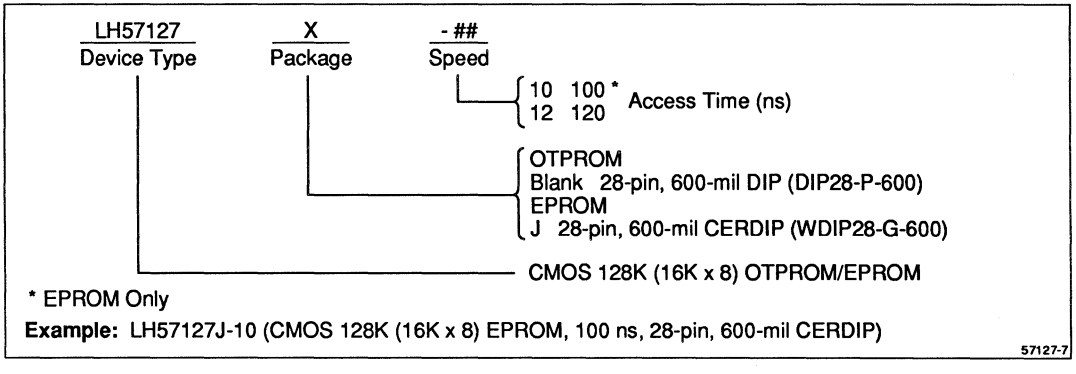


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH57128/J

CMOS 128K (16K × 8) OTPROM/EPROM

FEATURES

- 16,384 × 8 bit organization
- Access times:
  LH57128J: 250 ns
  LH57128: 250 ns
- Single +5 V power supply
- High speed programming:
  t_{PW} = 0.1 ms (V_{PP} = 12.75 V) or
  t_{PW} = 1 ms (V_{PP} = 12.5 V)
  Compatible to INTEL quick pulse programming™ algorithm
  (2 second programming)
- Low power consumption:
  Operating: 165 mW (MAX.)
  Standby: 550 μW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Pin compatible with i27128
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
- JEDEC standard pinout

DESCRIPTION

The LH57128J is a CMOS UV erasable and electrically programmable read-only-memory organized as 16,384 × 8 bits. It is pin compatible with the Intel i27128.

The LH57128 is a one-time PROM packaged in plastic DIP or SOP.

PIN CONNECTIONS

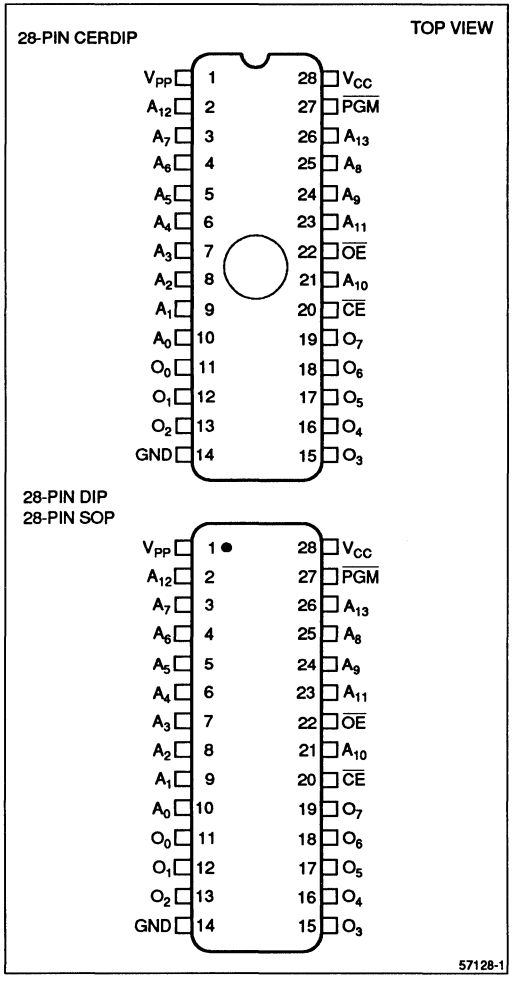


Figure 1. Pin Connections for CERDIP, DIP, and SOP Packages

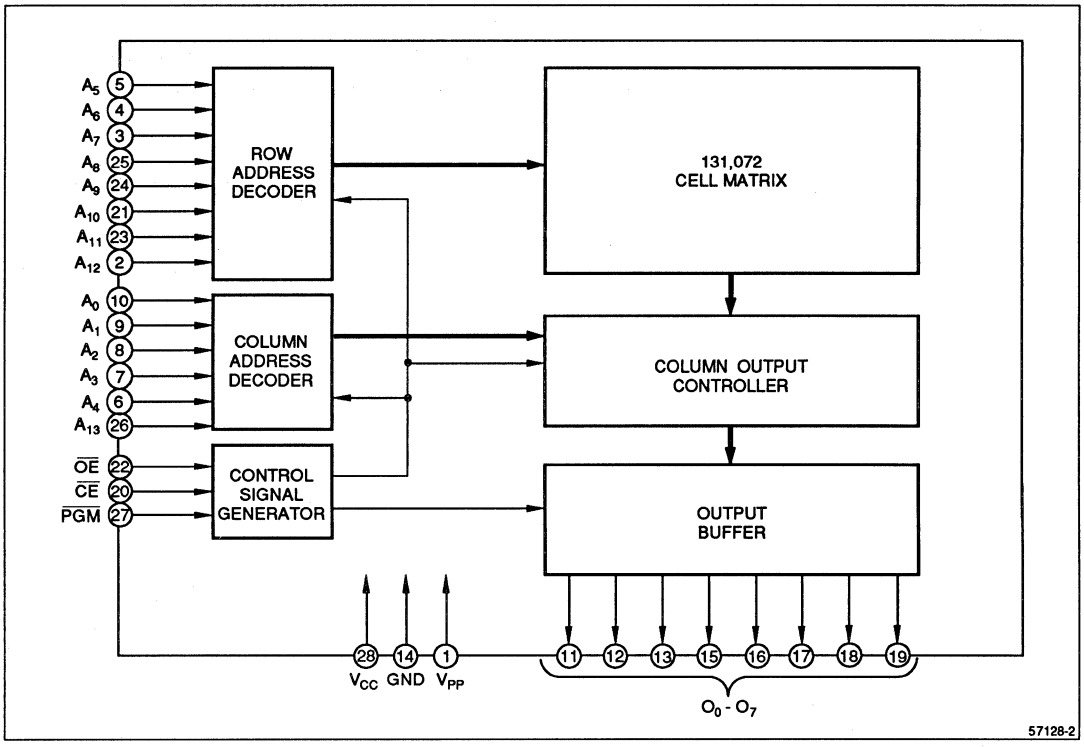


Figure 2. LH57128/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{13}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{PGM}$	Program input	
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	H	+5 V	+5 V
	Output disable	High-Z	L	H	H	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6.25 V	+12.75 V
	Program verify	Data out	L	L	H	+6.25 V	+12.75 V
	Program inhibit	High-Z	H	X	X	+6.25 V	+12.75 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150	°C	3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	4.5	5.0	5.5	V
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			25	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			30	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA	
	I_{SB2}	$\overline{CE}$ = V_{IH}			1	mA	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57128J-25 LH57128-25		UNIT
		MIN.	MAX.	
Address to output delay	t_{ACC}		250	ns
$\overline{CE}$ to output delay	t_{CE}		250	ns
$\overline{OE}$ to output delay	t_{OE}		75	ns
Output enable high to output float	t_{DF}	0	65	ns
Address to output hold	t_{OH}	0		ns

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

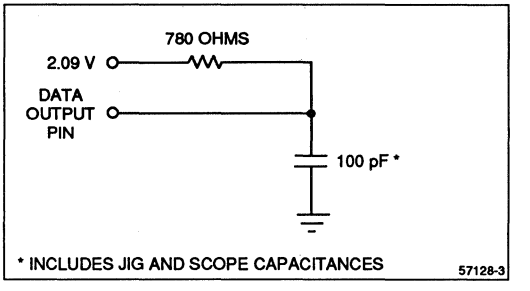


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

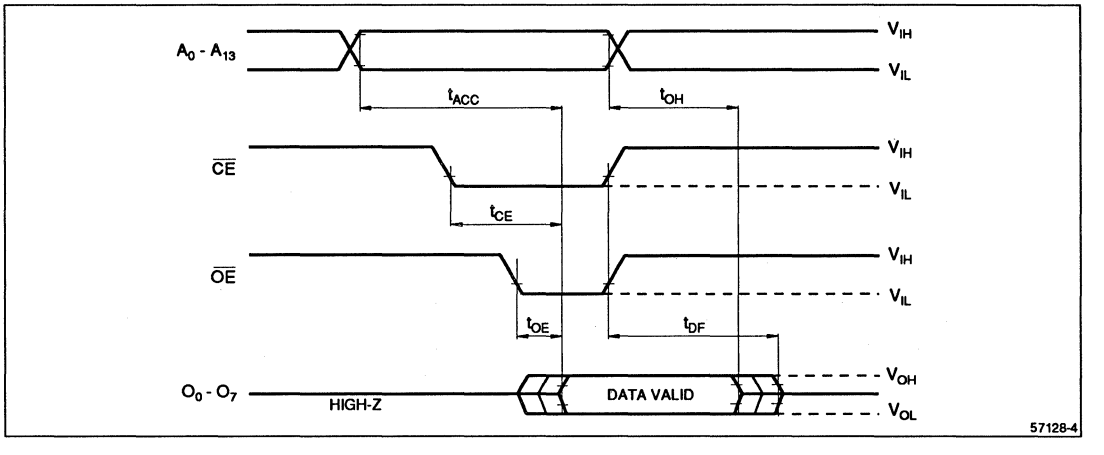


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.25	6.5	V
Program supply voltage	V_{PP}	12.2	12.75	13.0	V
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 5.75 V to 6.5 V, V_{PP} = 12.2 V to 13.0 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = V_{CC}$ or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				30	mA
V_{PP} supply current	I_{PP}	$\overline{CE} = \overline{PGM} = V_{IL}$			30	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Address setup time	t_{AS}	2			µs	
Chip enable setup time	t_{CES}	2			µs	
Output enable setup time	t_{OES}	2			µs	
Data setup time	t_{DS}	2			µs	
Address hold time	t_{AH}	0			µs	
Data hold time	t_{DH}	2			µs	
Chip enable to output float delay	t_{DF}	0		150	ns	
Data valid from output enable	t_{OE}			150	ns	
V_{PP} setup time	t_{VPS}	2			µs	
V_{CC} setup time	t_{VCS}	2			µs	
Program pulse width	t_{PW}	95	100	105	µs	1, 2
Program pulse count	N	1		25	TIMES	

NOTES:

1. This width is defined by the Program Flowchart (Figure 6).
2. Programmable under conditions of add. program pulse count 3-N, V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, t_{PW} = 1 ms ± 0.05 ms

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH57128 and LH57128J have all 16,384 × 8 bits in the "1", or high state. "0's" are loaded into the LH57128 and LH57128J through the procedure of programming.

The programming mode is entered when +12.75 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57128J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57128J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH57128J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57128J and similar devices will erase with light sources having wave-length shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57128J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

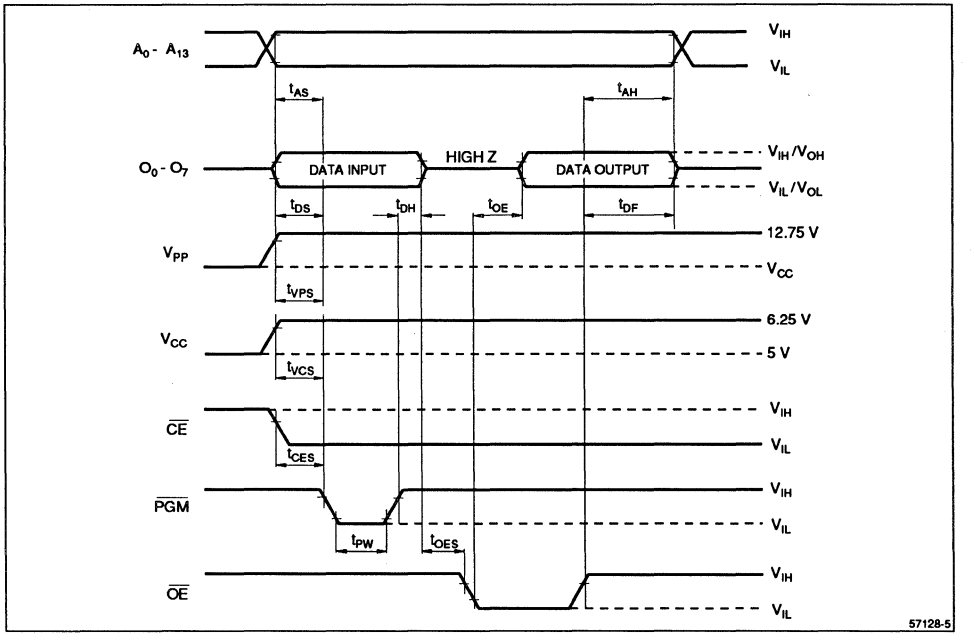


Figure 5. Timing Diagram (Program Mode)

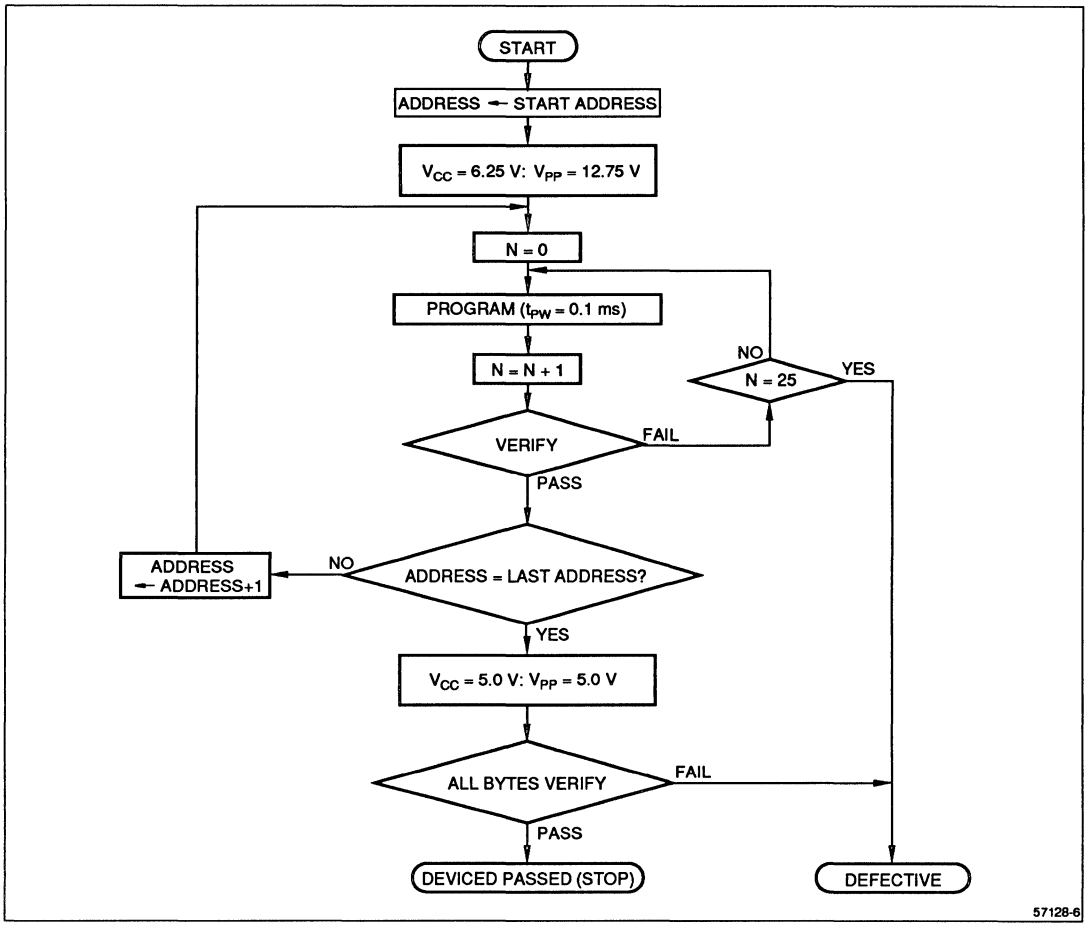
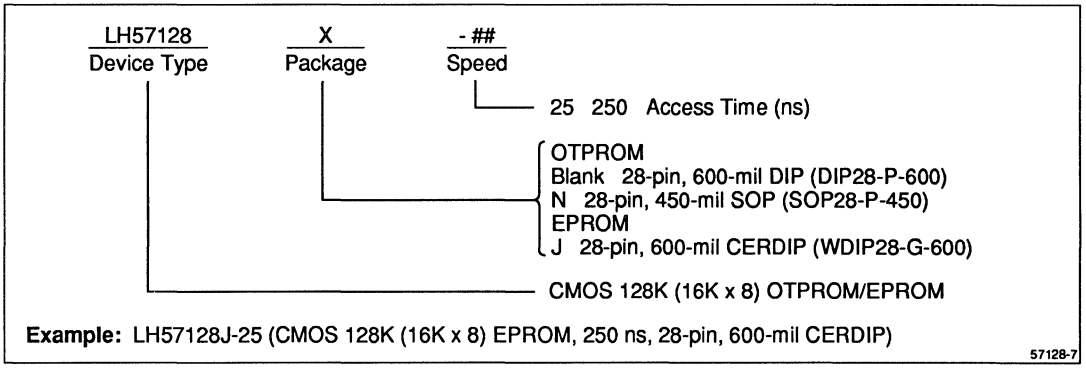


Figure 6. Programming Flowchart (V_{CC} = 6.25 V, V_{PP} = 12.75 V, t_{PW} = 0.1 ms)

ORDERING INFORMATION



LH57254/J

CMOS 256K (32K × 8) OTPROM/EPROM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  LH57254J: 70/90 ns
  LH57254: 90 ns
- Single +5 V power supply
- High speed programming:
  Compatible to INTEL intelligent programming™ algorithm
  (128 second programming)
- Low power consumption:
  Operating: 420 mW (MAX.)
  Standby: 78.8 mW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Pin compatible with i27256
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
- JEDEC standard pinout

DESCRIPTION

ThE LH57254J is a CMOS UV erasable and electrically programmable read-only-memory organized as 32,768×8 bits. It is pin compatible with the Intel i27256, and designed to have fast access time.

The LH57254 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

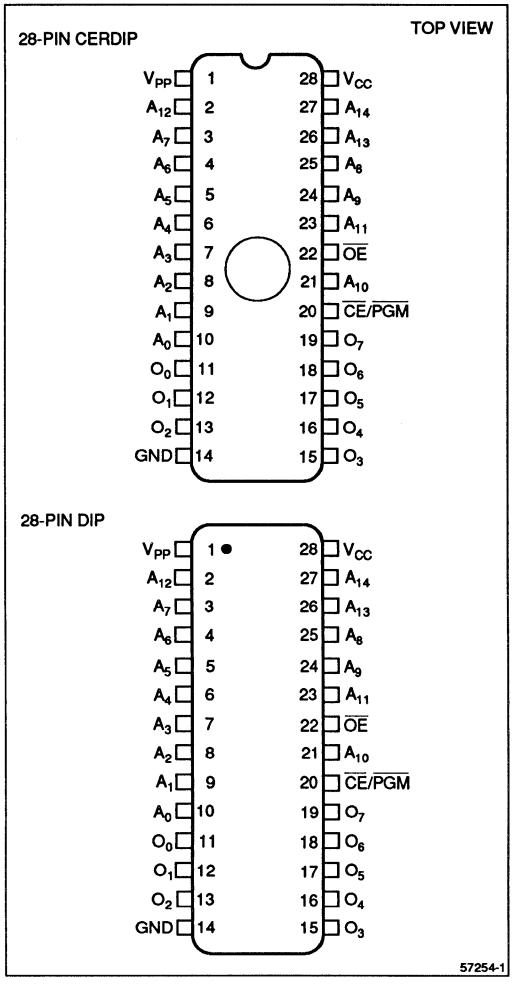


Figure 1. Pin Connections for CERDIP and DIP Packages

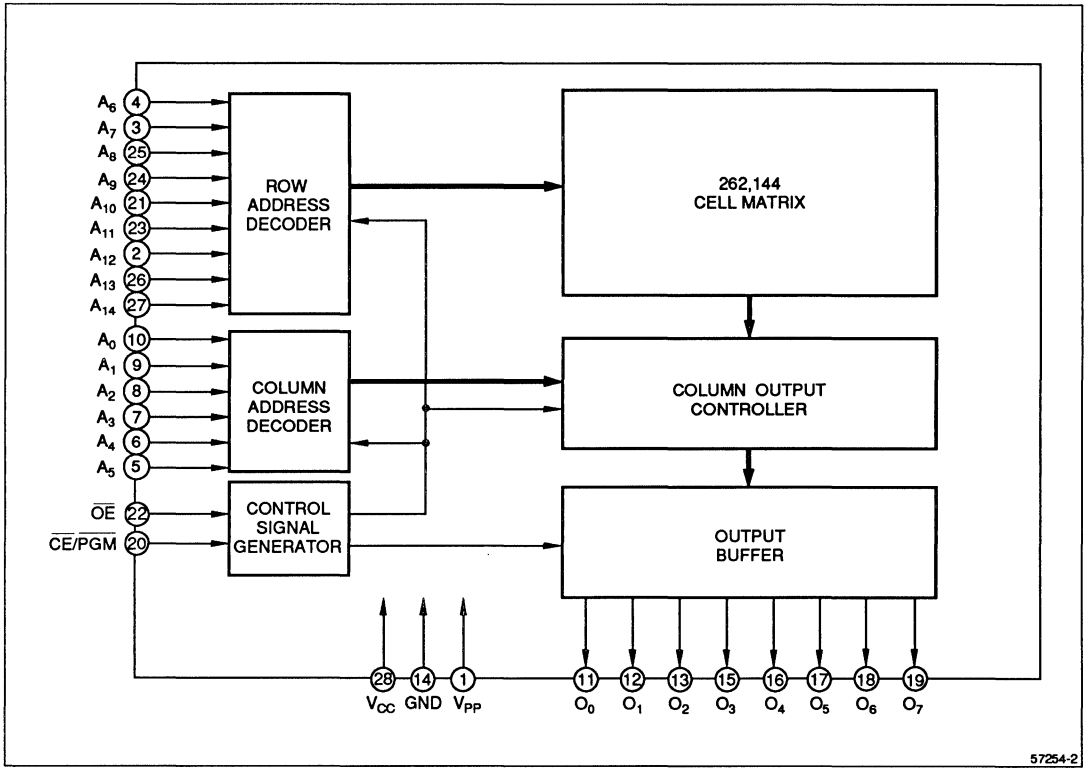


Figure 2. LH57254/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}/\overline{PGM}$	Chip Enable/Program input	
$\overline{OE}$	Output Enable	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	+5 V	+5 V
	Output disable	High-Z	L	H	+5 V	+5 V
	Standby	High-Z	H	X	+5 V	+5 V
Program	Program	Data in	L	H	+6 V	+12.5 V
	Program verify	Data out	H	L	+6 V	+12.5 V
	Program inhibit	High-Z	H	H	+6 V	+12.5 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{PP}	4.75	5.0	5.25	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}/\overline{PGM}$ = GND ± 0.3 V			80	mA	1, 2
	I_{CC2}	$\overline{CE}/\overline{PGM}$ = V_{IL}			80	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}/\overline{PGM}$ = V_{CC} ± 0.3 V			15	mA	4
	I_{SB2}	$\overline{CE}/\overline{PGM}$= V_{IH}			30	mA	5

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL level: V_{IL} or V_{IH}
4. All inputs are fixed at CMOS level.
5. All inputs inputs are fixed at TTL level.

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 5%. T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57254J-70		LH57254J-90 LH57254-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay ($\overline{CE}/\overline{PGM}$ = V_{IL})	t_{ACC}		70		90	ns
$\overline{CE}$ to output delay ($\overline{OE}$ = V_{IL})	t_{CE}		70		90	ns
$\overline{OE}$ to output delay ($\overline{CE}/\overline{PGM}$ = V_{IL})	t_{OE}		25		30	ns
Output enable high to output float	t_{DF}	0	25	0	30	ns
Address to output hold	t_{OH}	10		10		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

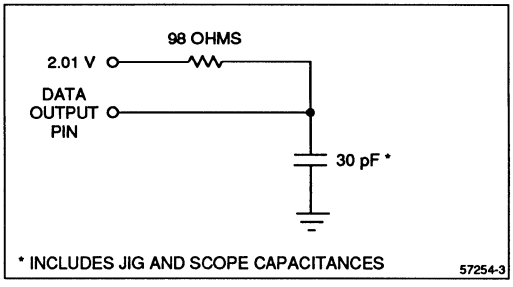


Figure 4. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

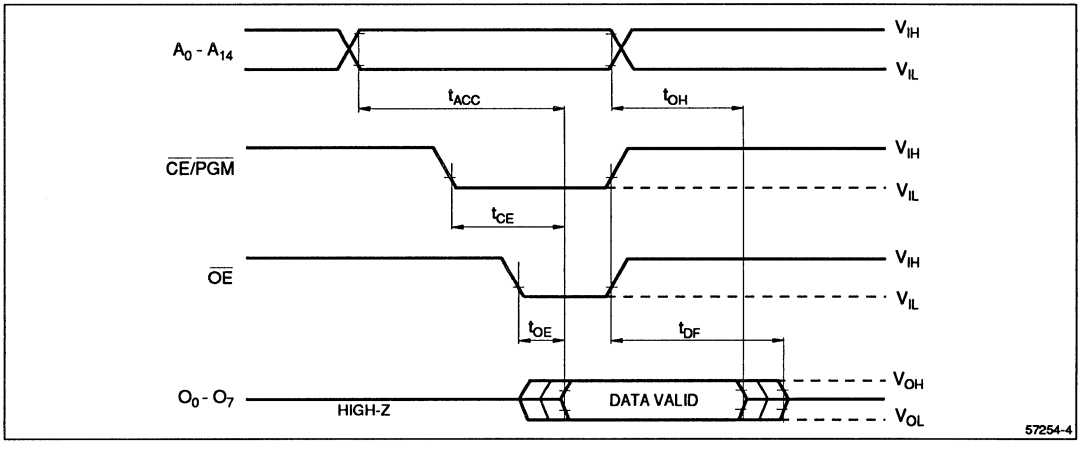


Figure 3. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
	V_{PP}	12.2	12.5	12.8	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				80	mA
V_{PP} supply current	I_{PP}	$\overline{CE}/\overline{PGM}$ = V_{IL}			50	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Data setup time	t_{DS}	2			µs
Output enable setup time	t_{OES}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Output enable time	t_{OE}			150	ns
Output disable time	t_{DF}	0		150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
Program pulse width	t_{PW}	0.95	1.0	1.05	µs
Add $\overline{PGM}$ pulse width *	t_{OPW}	2.85		78.75	ms
Program pulse count	N	1		25	TIMES

* This width is defined by the Program Flowchart (Figure 6).

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH57254 and LH57254J have all 32,768 × 8 bits in the "1", or high state. "0's" are loaded into the LH57254 and LH57254J through the procedure of programming.

The programming mode is entered when +12.5 V is applied to the V_{PP} pin and $\overline{CE}/\overline{PGM}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57254J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57254J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH57254J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57254J and similar devices will erase with light sources having wave-length shorter than 4,000 Å.

Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57254J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from V_{CC} to 12.5 volts or vice-versa.

4. Removing or inserting the device while 12.5 volts is supplied may harm the reliability of the device.

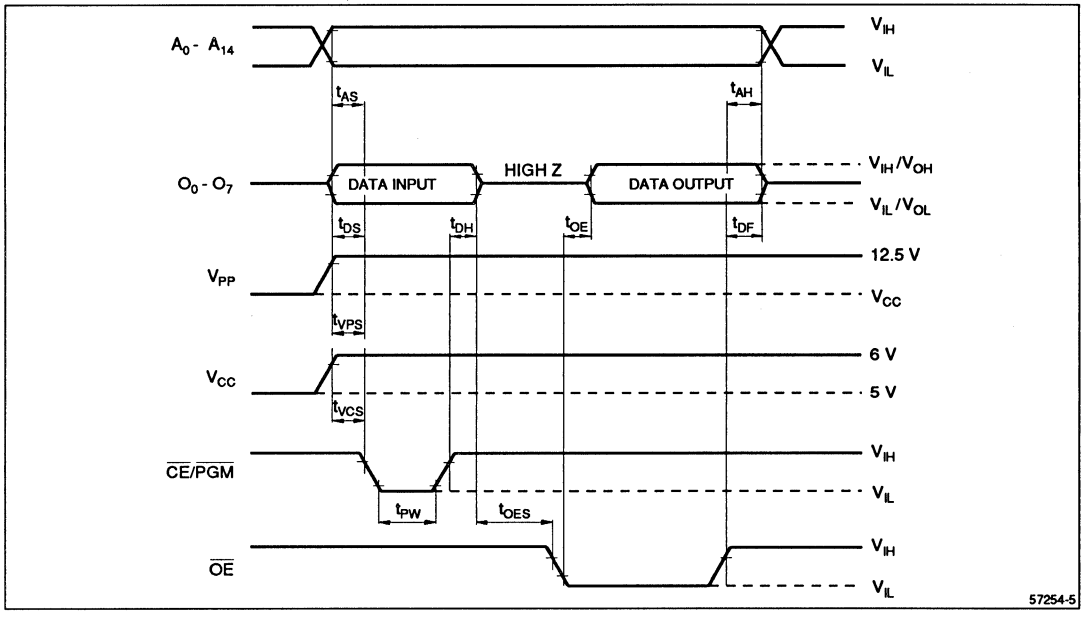


Figure 5. Timing Diagram (Program Mode)

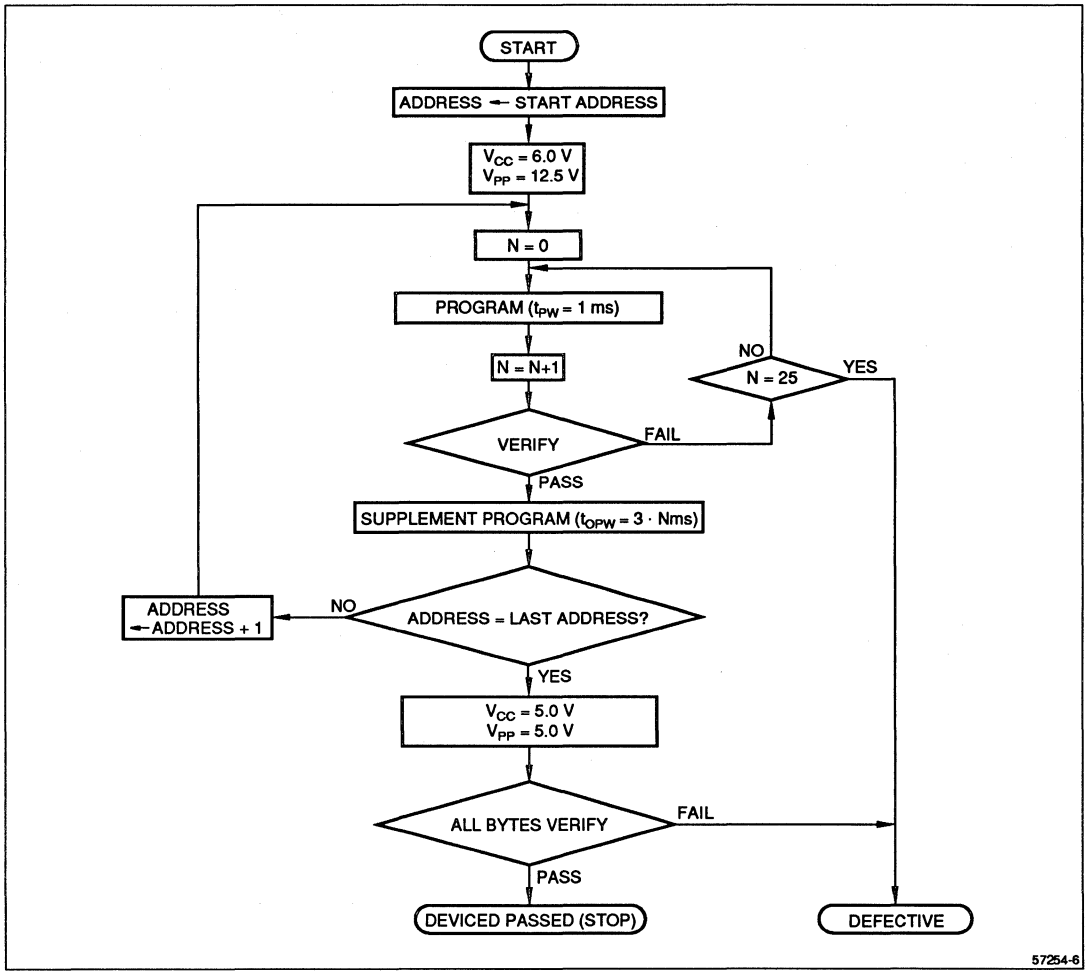
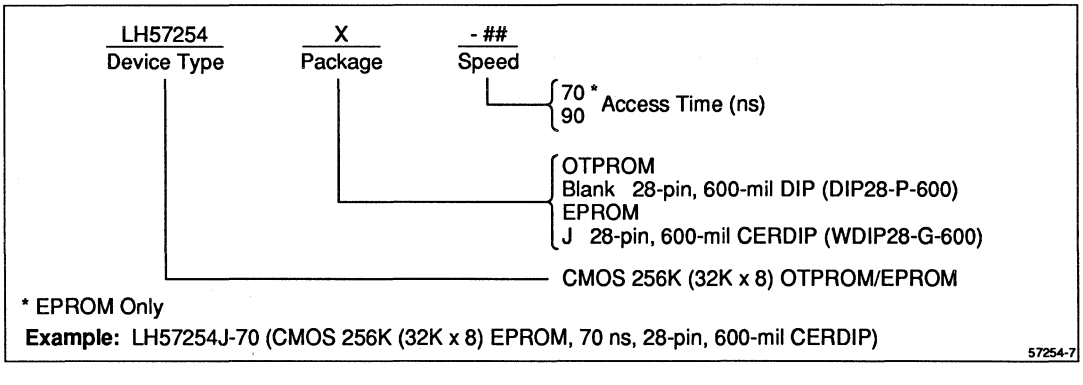


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH57256/J

CMOS 256K (32K × 8) OTPROM/EPROM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  LH57256J: 120/150 ns
  LH57256: 150 ns
- Single +5 V power supply
- High speed programming:
  t_{PW} = 0.1 ms (V_{PP} = 12.75 V) or
  t_{PW} = 1 ms (V_{PP} = 12.5 V)
  Compatible to INTEL quick pulse programming™ algorithm
  (4 second programming)
- Low power consumption :
  Operating: 165 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Pin compatible with i27256
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP
- JEDEC standard pinout (CERDIP/DIP)

DESCRIPTION

The LH57256J is a CMOS UV erasable and electrically programmable read-only-memory organized as 32,768 × 8 bits. It is pin compatible with the Intel i27256, and designed to have fast access time.

The LH57256 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

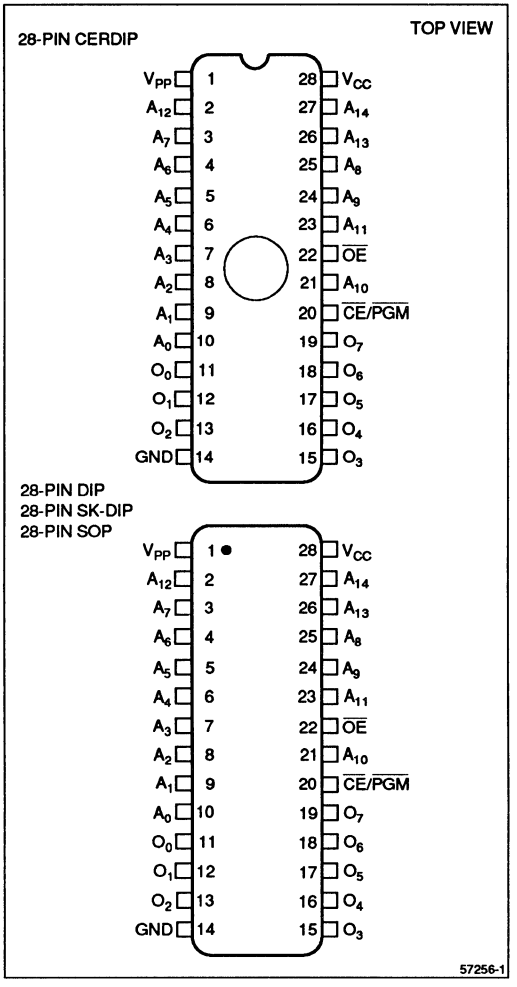


Figure 1. Pin Connections for CERDIP, DIP, SK-DIP, and SOP Packages

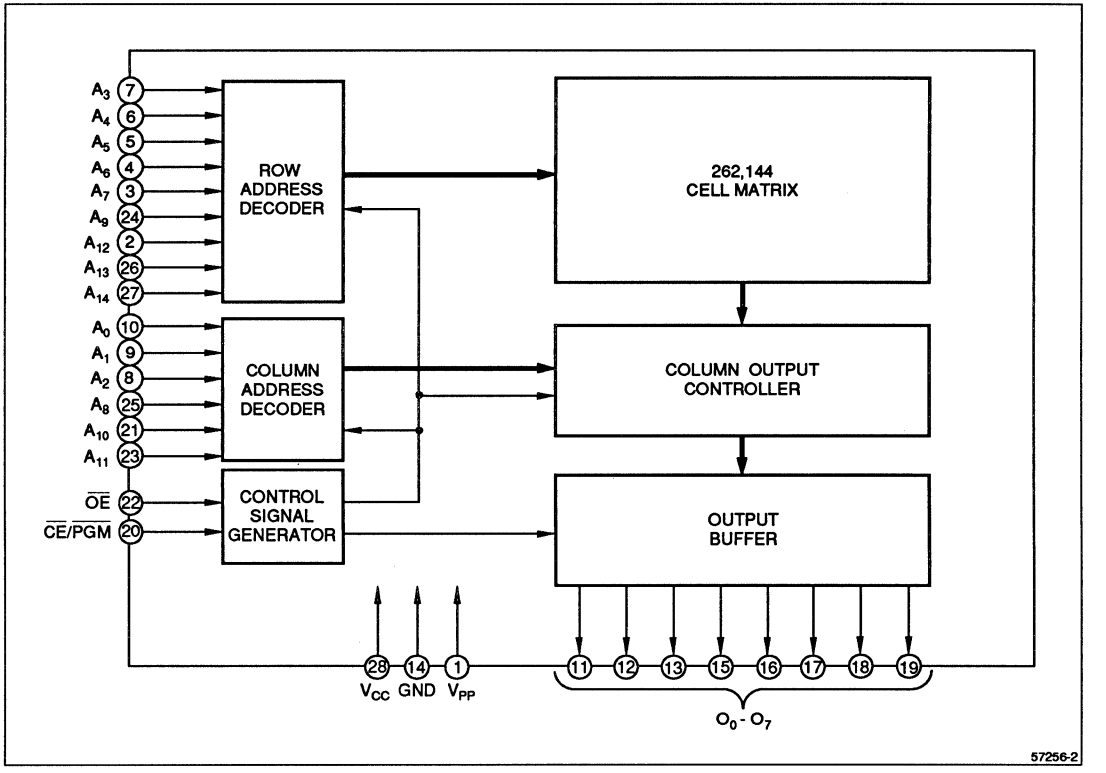


Figure 2. LH57256/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}/\overline{PGM}$	Chip Enable/Program input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	+5 V	+5 V
	Output disable	High-Z	L	H	+5 V	+5 V
	Standby	High-Z	H	X	+5 V	+5 V
Program	Program	Data in	L	H	+6.25 V	+12.75 V
	Program verify	Data out	H	L	+6.25 V	+12.75 V
	Program inhibit	High-Z	H	H	+6.25 V	+12.75 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	4.5	5.0	5.5	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}/\overline{PGM}$ = GND ± 0.3 V			30	mA	1, 2
	I_{CC2}	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}/\overline{PGM}$ = V_{CC} ± 0.3 V			100	µA	
	I_{SB2}	$\overline{CE}/\overline{PGM}$ = V_{IH}			2	mA	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL level: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 10%. T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57256J-12		LH57256J-15 LH57256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		120		150	ns
$\overline{CE}$ to output delay	t_{CE}		120		150	ns
$\overline{OE}$ to output delay	t_{OE}		25		30	ns
Output enable high to output float	t_{DF}	0	25	0	30	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.45 V to 2.4 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

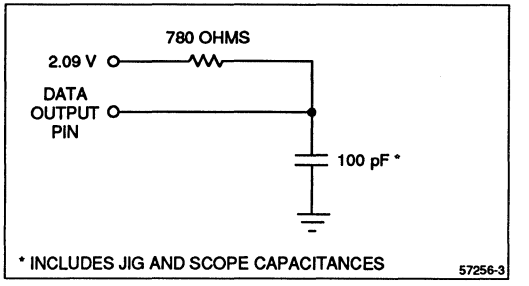


Figure 4. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

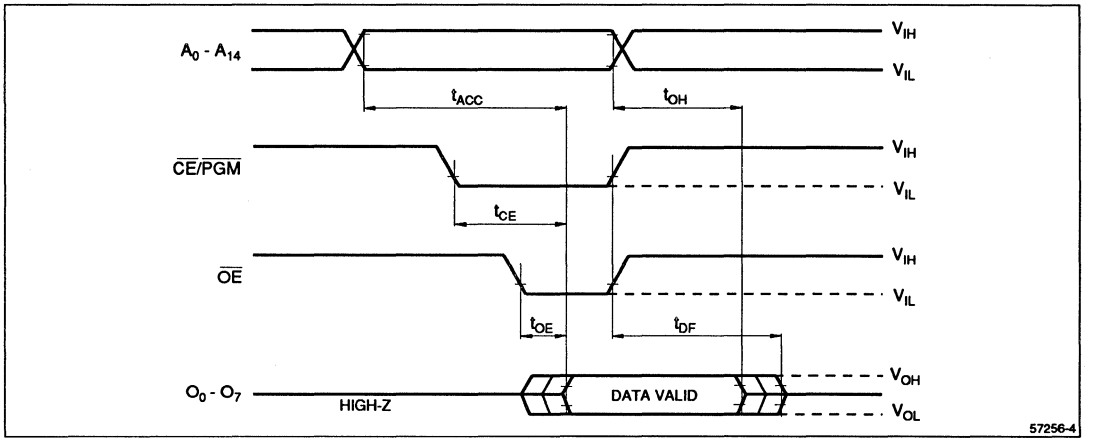


Figure 3. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.25	6.5	V
	V_{PP}	12.2	12.75	13.0	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 5.75 V to 6.5 V, V_{PP} = 12.2 V to 13 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				30	mA
V_{PP} supply current	I_{PP}	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program mode)

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Address setup time	t_{AS}	2			µs	
Data setup time	t_{DS}	2			µs	
Output enable setup time	t_{OES}	2			µs	
Address hold time	t_{AH}	0			µs	
Data hold time	t_{DH}	2			µs	
Output enable time	t_{OE}			150	ns	
Output disable time	t_{DF}	0		150	ns	
V_{PP} setup time	t_{VPS}	2			µs	
V_{CC} setup time	t_{VCS}	2			µs	
Program pulse width	t_{PW}	95	100	105	µs	1,2
Program pulse count	N	1		25	TIMES	

NOTES:

1. Programmable under conditions of add. program pulse count 3-N, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, t_{pw} = 1 ms ± 0.05 ms
2. This width is defined by the Program Flowchart (Figure 6).

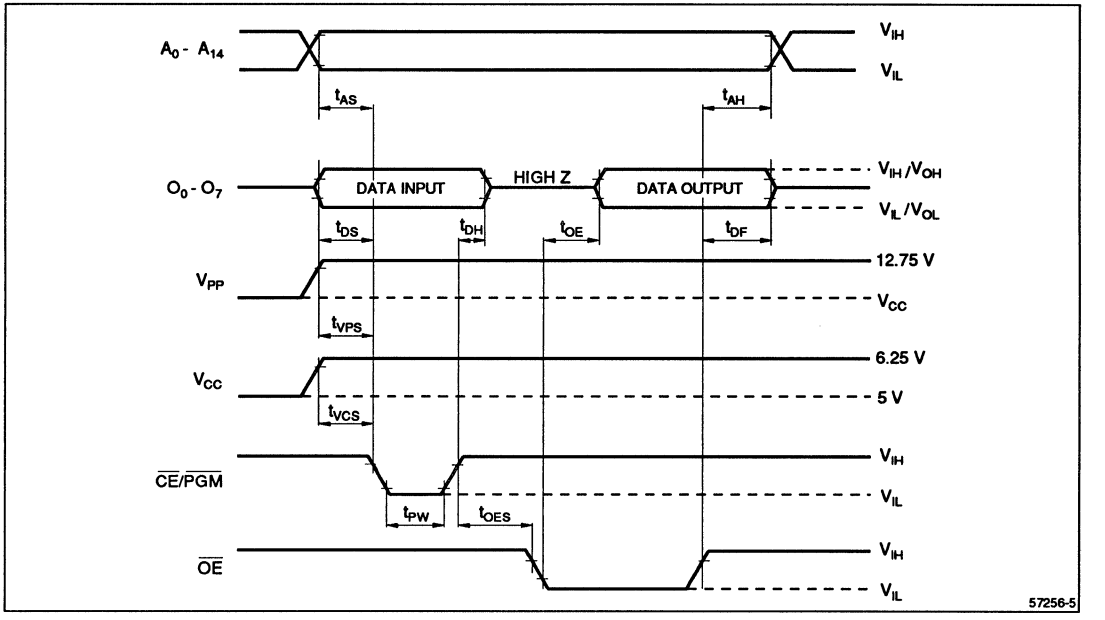


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH57256 and LH57256J have all 32,768 × 8 bits in the "1", or high state. "0's" are loaded into the LH57256 and LH57256J through the procedure of programming.

The programming mode is entered when +12.75 V is applied to the V_{PP} pin and $\overline{CE}/\overline{PGM}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57256J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57256J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH57256J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57256J and similar devices will erase with light sources having wave-length shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57256J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from V_{CC} to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

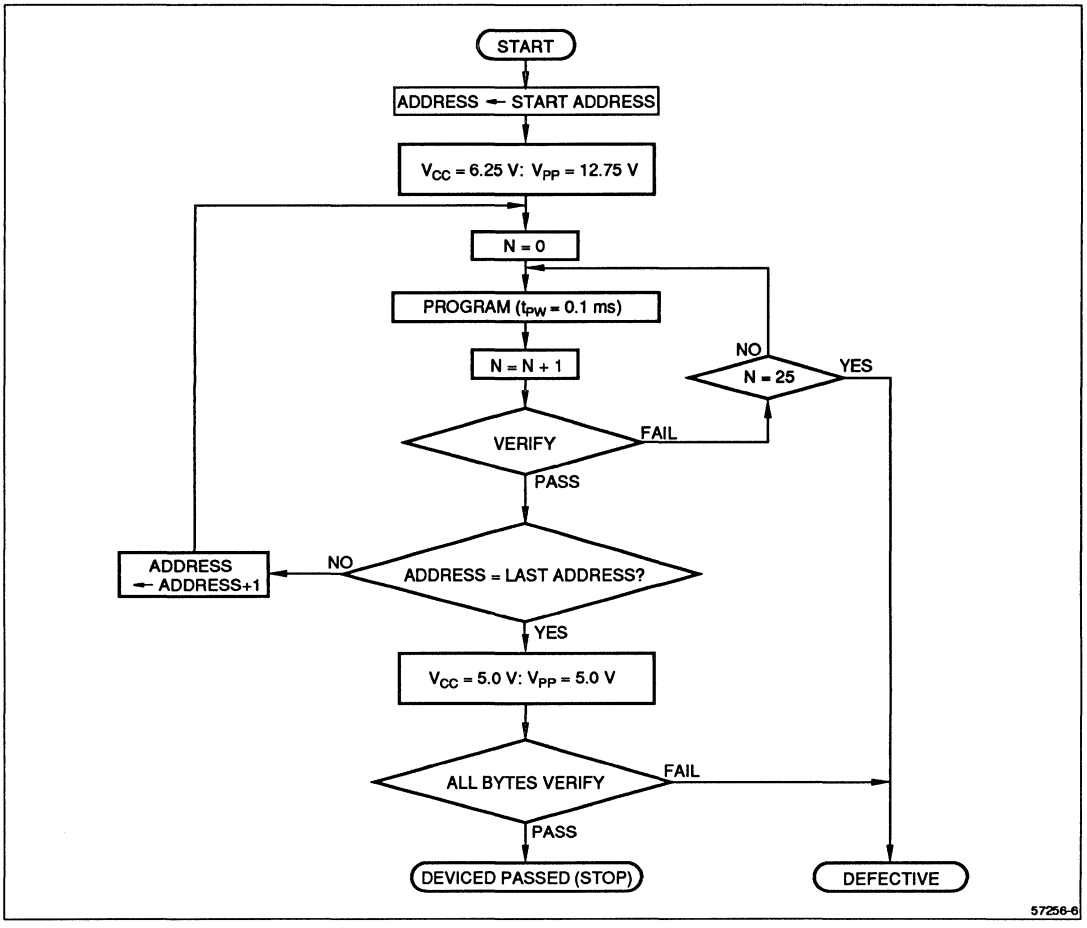
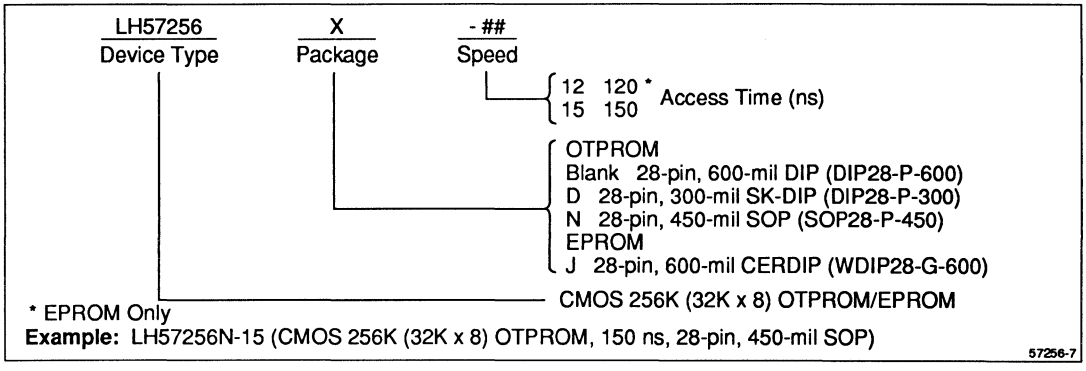


Figure 6. Programming Flowchart
(V_{CC} = 6.25 V, V_{PP} = 12.75 V, t_{PW} = 0.1 ms)

ORDERING INFORMATION



LH57512/J

CMOS 512K (64K × 8) OTPROM/EPROM

FEATURES

- 65,536 × 8 bit organization
- Access times:
  LH57512J: 120/150 ns
  LH57512: 150 ns
- Single +5 V power supply
- High speed programming:
  SHARP original programming algorithm
  (13 second programming)
- Low power consumption
  Operating: 165 mW (MAX.)
  Standby: 550 μW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Pin compatible with i27512
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
- JEDEC standard pinout (CERDIP/DIP)

DESCRIPTION

The LH57512J is a CMOS UV erasable and electrically programmable read-only-memory organized as 65,536 × 8 bits. It is pin compatible with the Intel i27512, and designed to have fast access time.

The LH57512 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

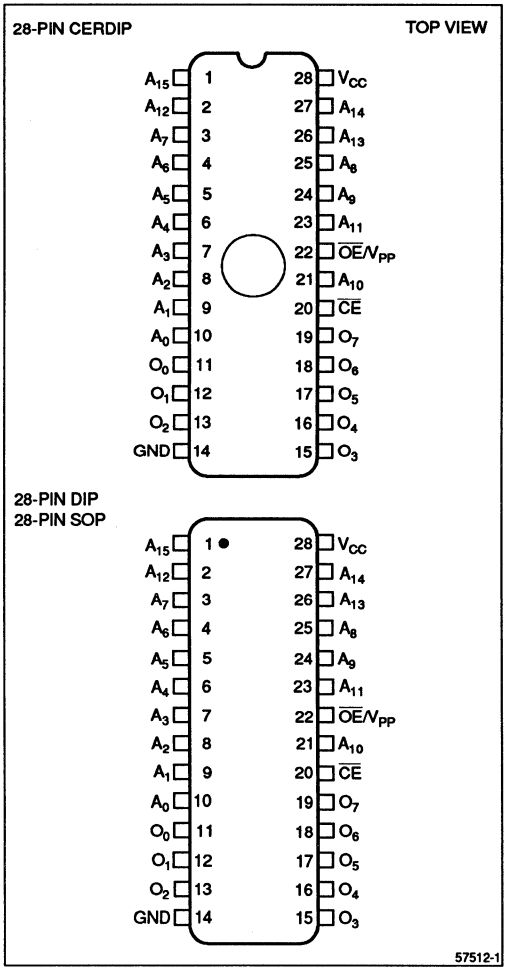


Figure 1. Pin Connections for CERDIP, DIP, and SOP Packages

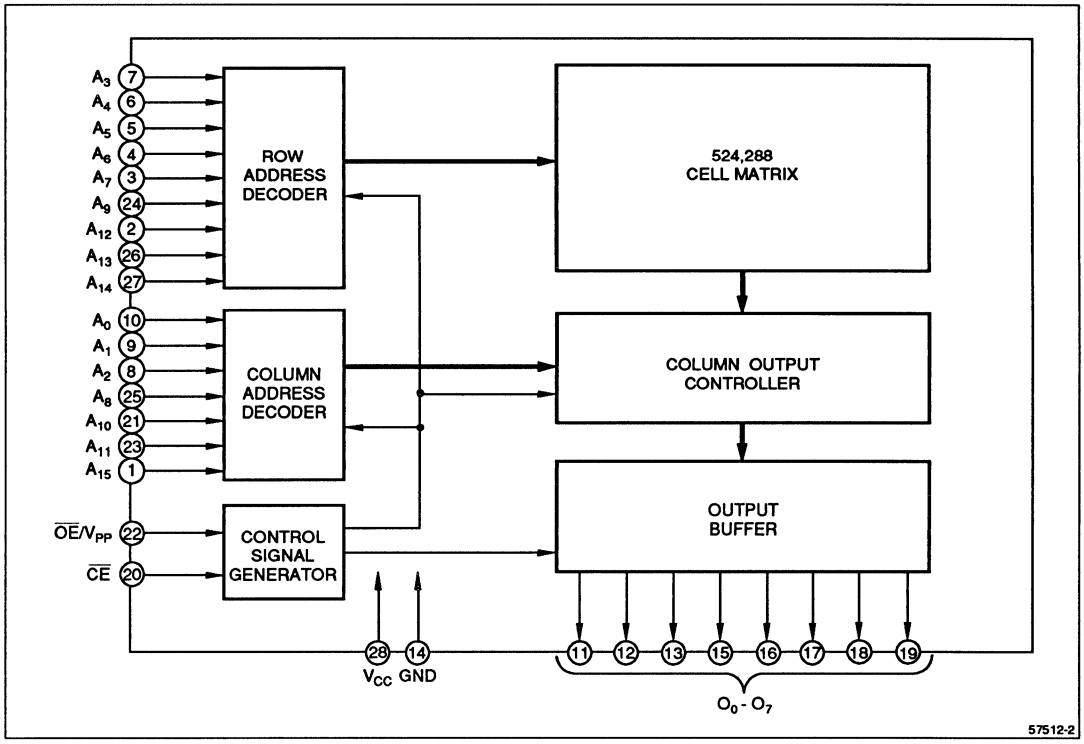


Figure 2. LH57512/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{15}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}/V_{PP}$	Output Enable/ Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}
Read	Read	Data out	L	L	+5 V
	Output disable	High-Z	X	H	+5 V
	Standby	High-Z	H	X	+5 V
Program	Program	Data in	L	+12.75	+6.5 V
	Program verify	Data out	L	L	+6.5 V
	Program inhibit	High-Z	H	+12.75	+6.5 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	$\overline{OE}/V_{PP}$	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			30	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			30	mA	1, 3
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA	
	I_{SB2}	$\overline{CE}$= V_{IH}			2	mA	

NOTES:
1. f = 5MHz, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL level: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57512J-12		LH57512J-15 LH57512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		120		150	ns
$\overline{CE}$ to output delay	t_{CE}		120		150	ns
$\overline{OE}$ to output delay	t_{OE}		40		50	ns
Output enable high to output float	t_{DF}	0	40	0	50	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.45 V to 2.4 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

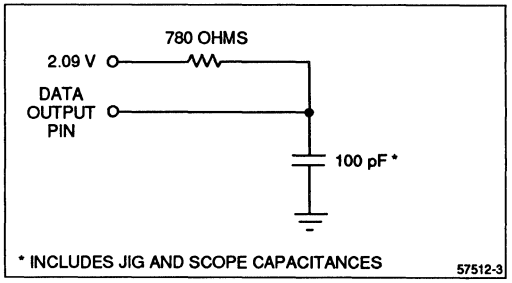


Figure 4. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

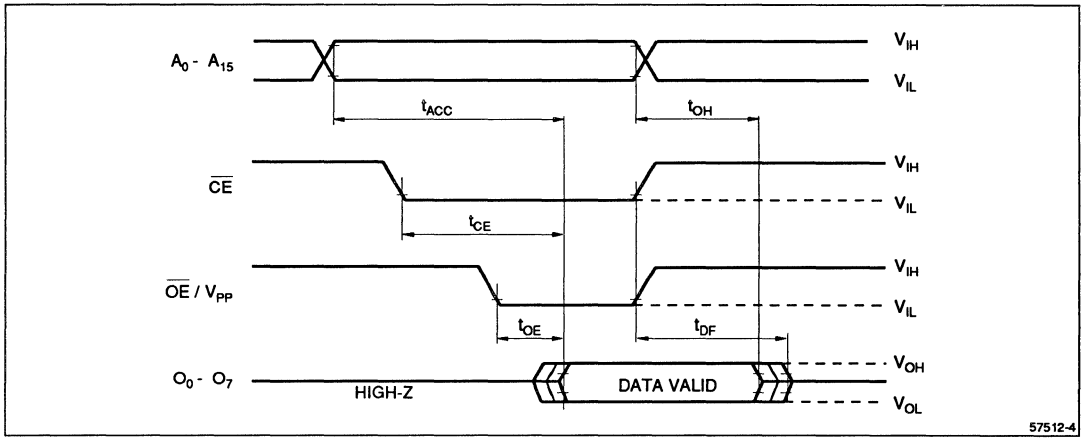


Figure 3. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75		6.75	V
Program supply voltage	V_{PP}	12.5		13.0	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 4.75 V to 6.75 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				30	mA
V_{PP} supply current	I_{PP}	$\overline{CE}$= V_{IL}			50	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 4.75 V to 6.75 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Data setup time	t_{DS}	2			µs
Output enable hold time	t_{OEH}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
$\overline{CE}$ to output delay	t_{DV}	0		1	µs
Output disable time	t_{DF}	0		150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{PP} recovery time	t_{VR}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
Program pulse width	t_{PW}	95	100	105	µs
Program pulse count	N	1		20	TIMES

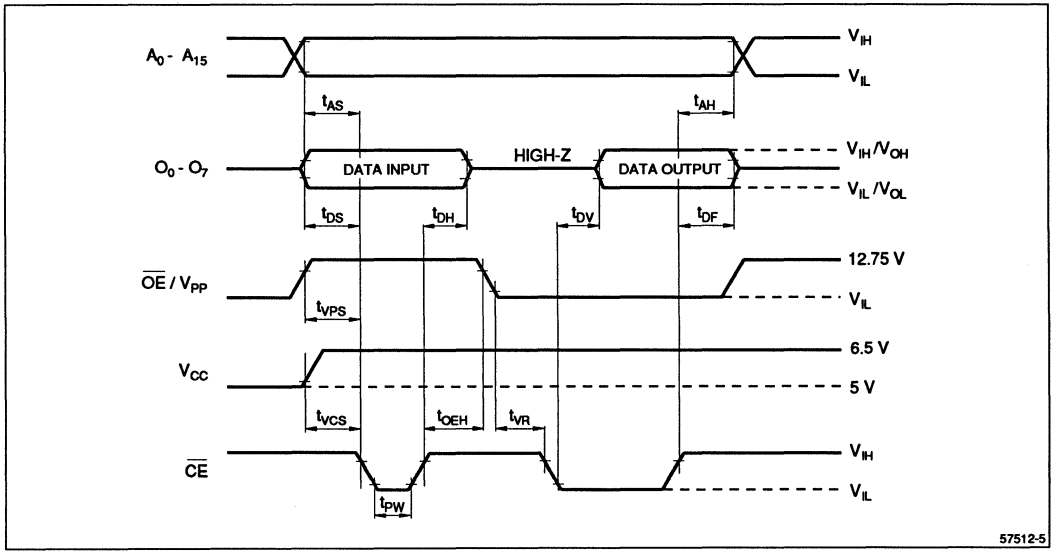


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP, the LH57512 and LH57512J have all 65,536 × 8 bits in the "1", or high state. "0's" are loaded into the LH57512 and LH57512J through the procedure of programming.

The programming mode is entered when appropriate pulses shown in the AC characteristics and timing diagram are applied to the $\overline{OE}/V_{PP}$ pin and $\overline{CE}$ pin. A 0.1 μF capacitor between $\overline{OE}/V_{PP}$ and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57512J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57512J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 μW/cm^2 for 20 to 30 minutes. The LH57512J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57512J and similar devices will erase with light sources having wave-length shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57512J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP}$ must not be switched from V_{CC} to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

PRODUCT IDENTIFICATION MODE

LH57512/J enters a product identification mode by applying 12 V (Note 1) on A9 pin during a Read mode. Maker code is output on data output pins when all other address pins and control pins are set at V_{IL} level (Note 2) during the product identification mode. Device code is output when A_0 pin is set at V_{IH} level. The programing condition or PROM writer can be set automatically by using this function.

Table 1. Product Identification Mode

SIGNAL	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX
PIN	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	DATA
MAKER CODE	V_{IL}	1	0	1	1	0	0	0	0	B0
DEVICE CODE	V_{IH}	1	1	0	0	0	0	1	0	C2

NOTES:
1. $A_9 = 12\ V \pm 0.5\ V$
2. A_1 - A_8, A_{10} - A_{15}, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$

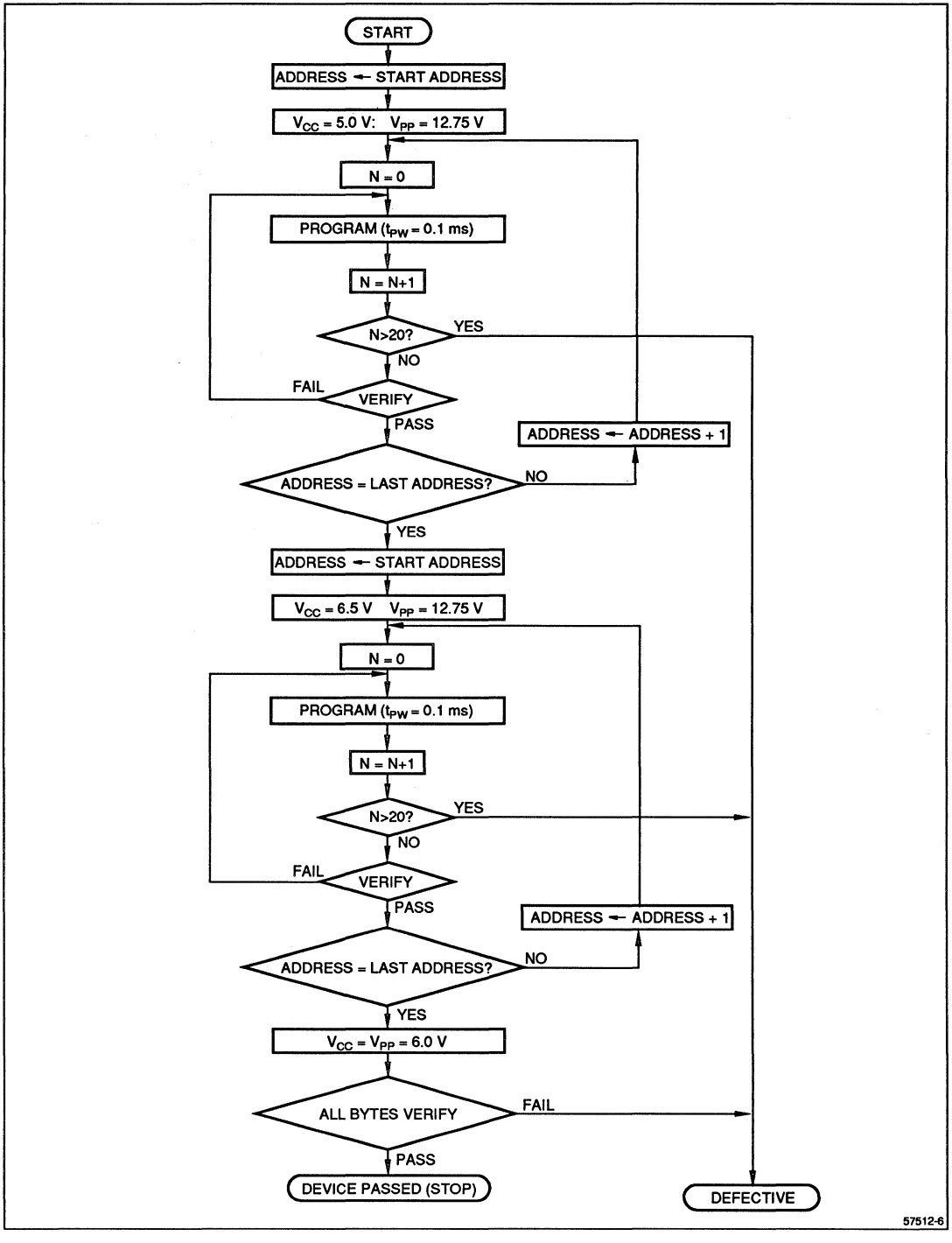
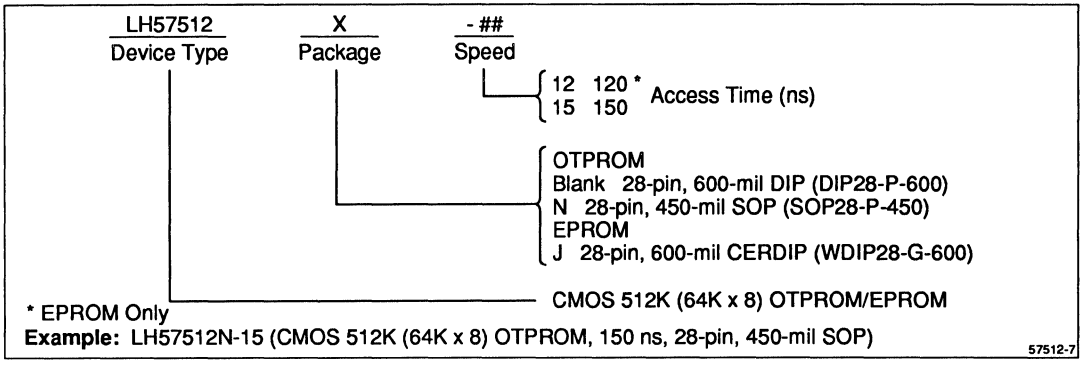


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH571000/J

CMOS 1M (128K × 8) OTPROM/EPROM

FEATURES

- 131,072 × 8 bit organization
- Access times:
  LH571000J: 120/150 ns (MAX.)
  LH571000: 150 ns (MAX.)
- Single +5 V power supply
- High speed programming:
  SHARP original programming algorithm
  (26 second programming)
- Low power consumption:
  Operating: 220 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Packages:
  EPROM
  32-pin, 600-mil CERDIP
  OTPROM
  32-pin, 600-mil DIP
- JEDEC standard 28-pin 1M mask ROM pinout

DESCRIPTION

The LH571000J is a CMOS UV erasable and electrically programmable read-only-memory organized as 131,072 × 8 bits.

The LH571000 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

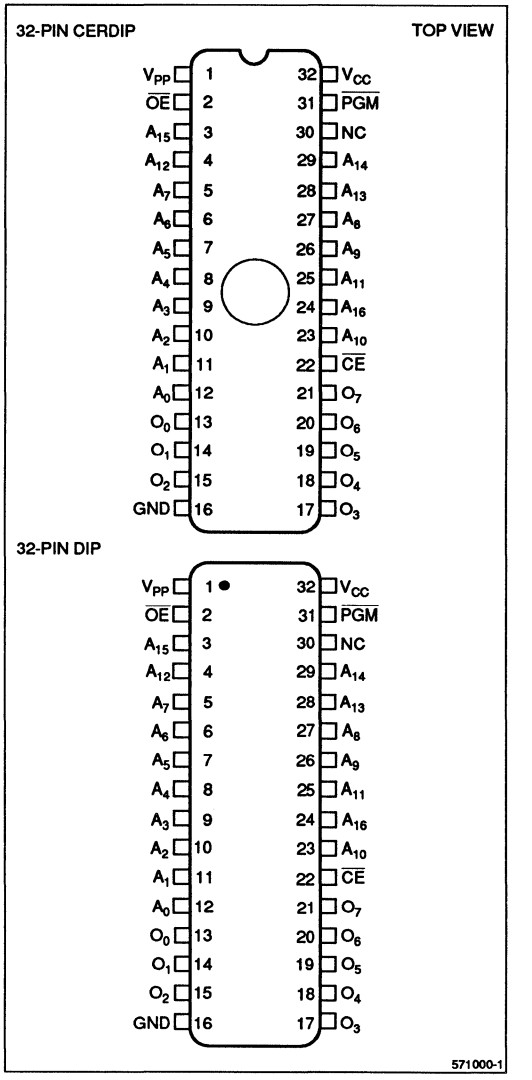


Figure 1. Pin Connections for CERDIP and DIP Packages

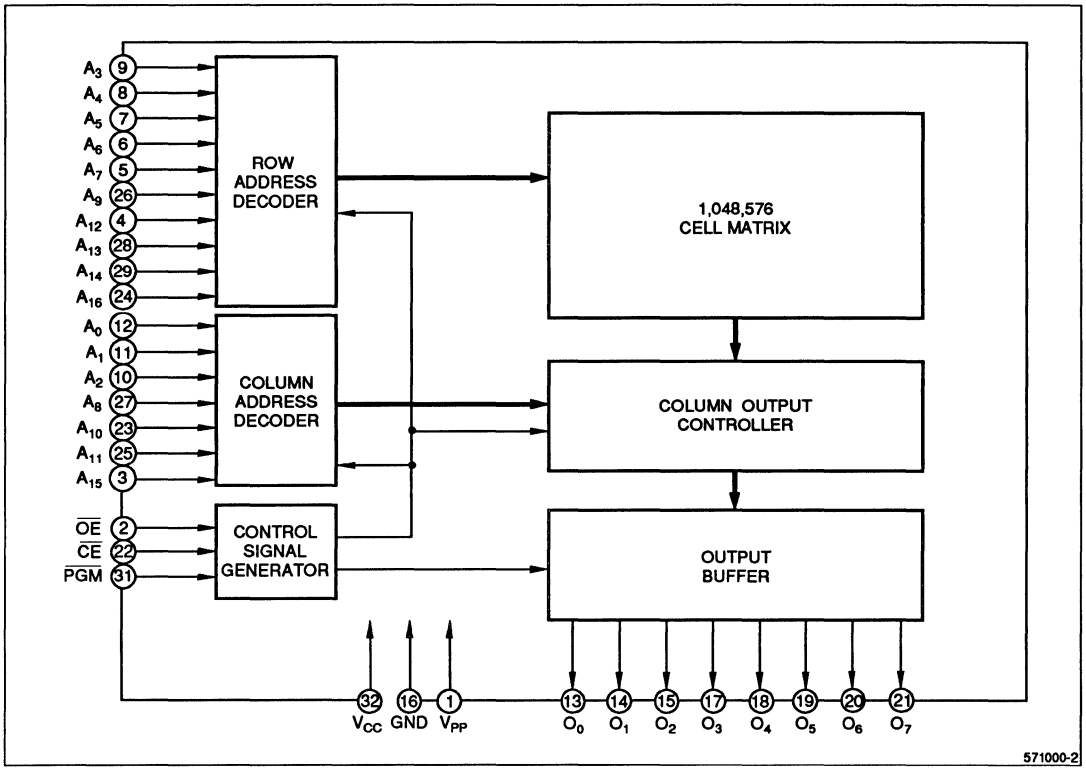


Figure 2. LH571000/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	
$\overline{PGM}$	Program input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	X	+5 V	+5 V
	Output disable	High-Z	L	H	X	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6.5 V	+12.75 V
	Program verify	Data out	L	L	H	+6.5 V	+12.75 V
	Program inhibit	High-Z	H	X	X	+6.5 V	+12.75 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	-0.1		5.5	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, $V_{PP} \leq V_{CC}$, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	Unit	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input load current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			40	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			40	mA	1, 3
V_{PP} supply current	I_{PP}	$V_{PP} \leq V_{CC}$			10	µA	
V_{PP} pin voltage	V_{PP}		0.1		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA	2
	I_{SB2}	$\overline{CE}$ = V_{IH}			2	mA	3

NOTES:
1. f = 5MHz, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH571000J-12		LH571000J-15 LH571000-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		120		150	ns
$\overline{CE}$ to output delay	t_{CE}		120		150	ns
$\overline{OE}$ to output delay	t_{OE}		40		50	ns
Output disable high to output float	t_{DF}	0	40	0	50	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.45 V to 2.4 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

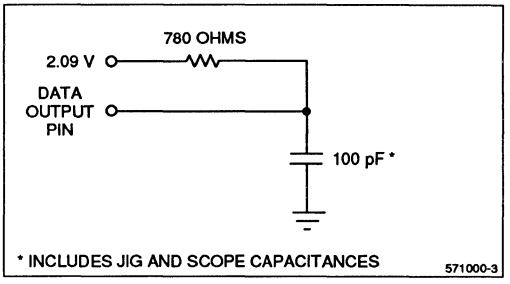


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

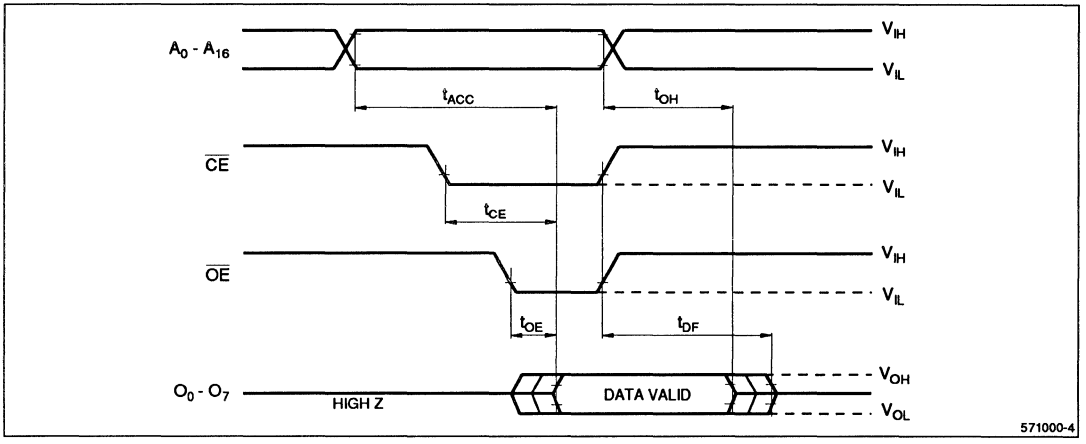


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75		6.75	V
	V_{PP}	12.5	12.75	13.0	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 4.75 V to 6.75 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				40	mA
V_{PP} supply current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}			50	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 4.75 to 6.75 V, V_{PP} = 12.75 ± 0.25 V, T_A = 25°C± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Data setup time	t_{DS}	2			µs
Output enable setup time	t_{OES}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Data valid from output enable	t_{OE}			150	ns
Chip enable to output float delay	t_{DF}	0		150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
Program pulse width *	t_{PW}	95	100	105	µs
Chip enable setup time	t_{CES}	2			µs

* The pulse width is defined by the Program Flowchart (Figure 6).

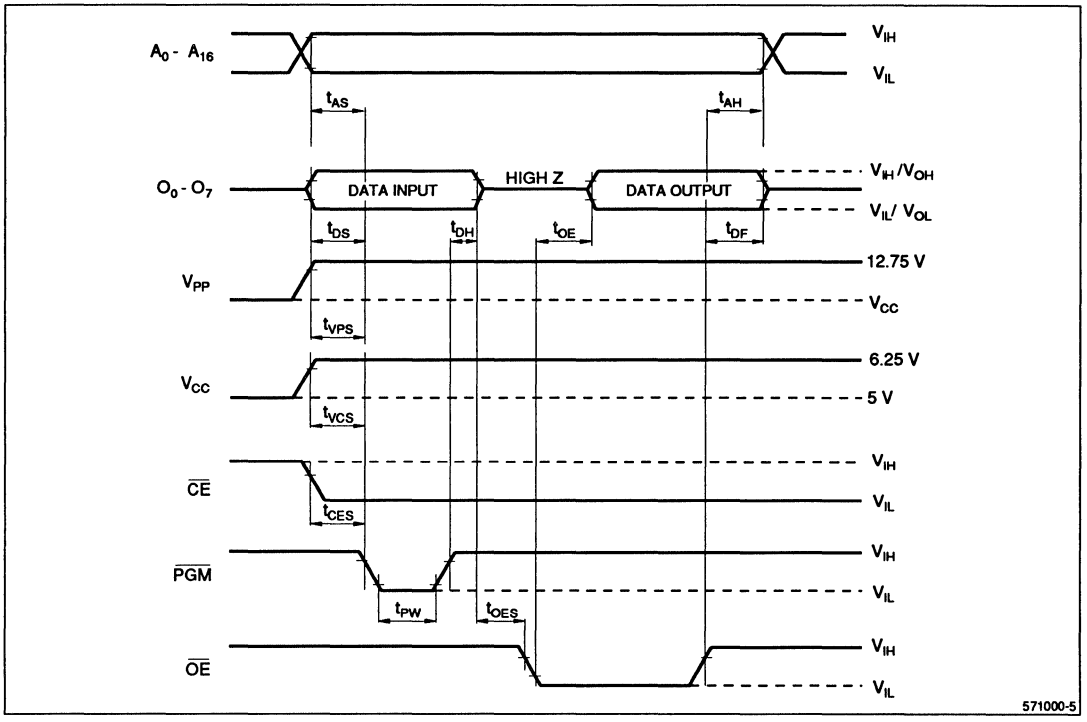


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see Erasure section), the LH571000 and LH571000J have all 131,072 × 8 bits in the "1", or high state. "0's" are loaded into the LH571000 and LH571000J through the procedure of programming.

The programming mode is entered when +12.75 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH571000J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH571000J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH571000J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH571000J and similar devices will erase with light sources having wave-length shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH571000J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

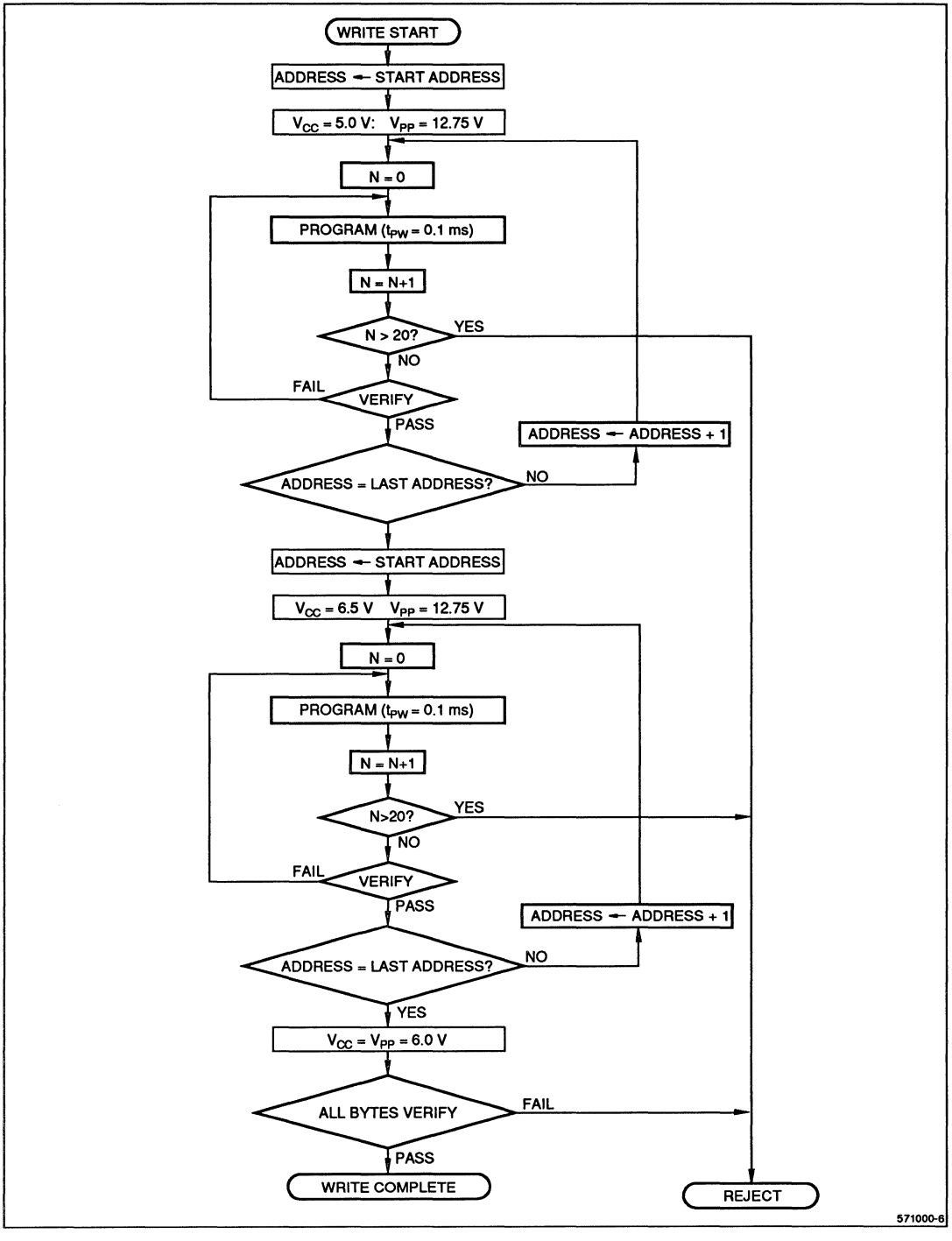
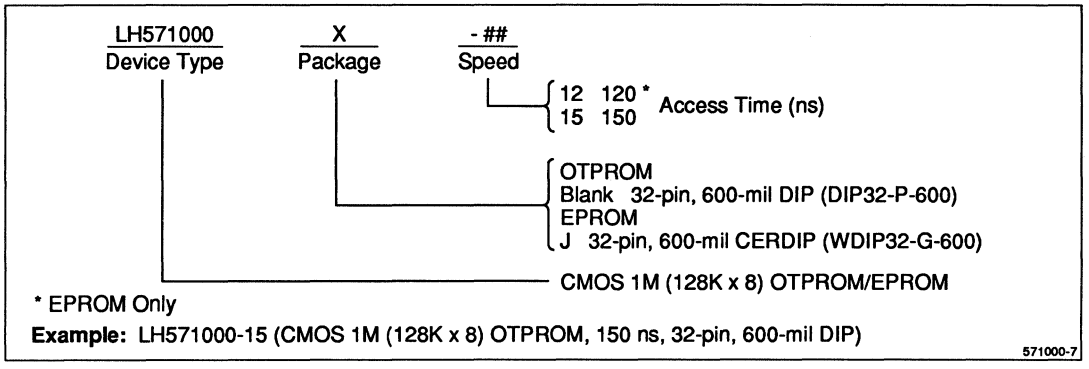


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH571001/J

CMOS 1M (128K × 8) OTPROM/EPROM

FEATURES

- 131,072 × 8 bit organization
- Access times:
  LH571001J: 120/150 ns (MAX.)
  LH571001: 150 ns (MAX.)
- Single +5 V power supply
- High speed programming:
  SHARP original programming algorithm
  (26 second programming)
- Low power consumption:
  Operating: 220 mW (MAX.)
  Standby: 550 μW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Packages:
  EPROM
  32-pin, 600-mil CERDIP
  OTPROM
  32-pin, 600-mil DIP
- JEDEC standard 28-pin 512K EPROM pinout

DESCRIPTION

The LH571001J is a CMOS UV erasable and electrically programmable read-only-memory organized as 131,072 × 8 bits.

The LH571001 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

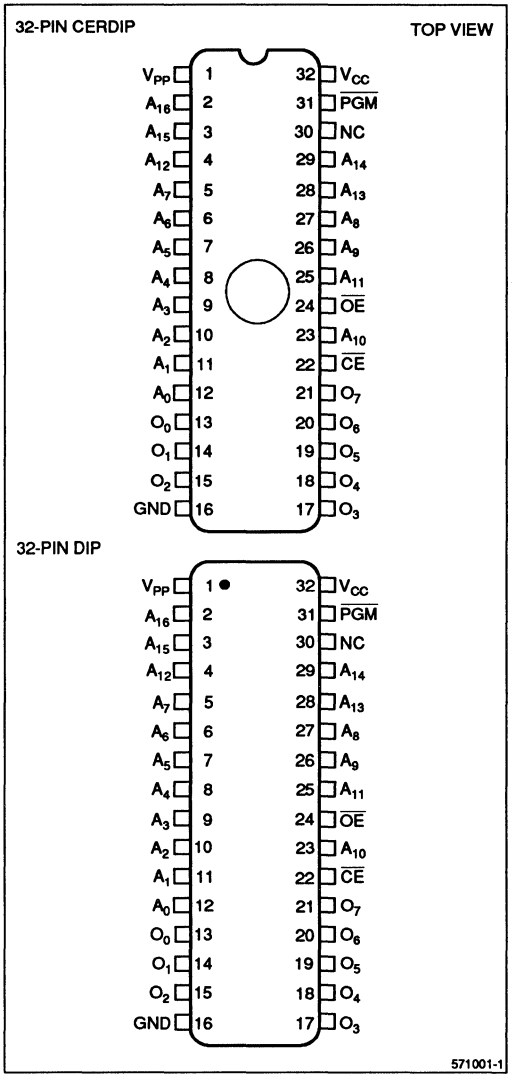


Figure 1. Pin Connections for CERDIP and DIP Packages

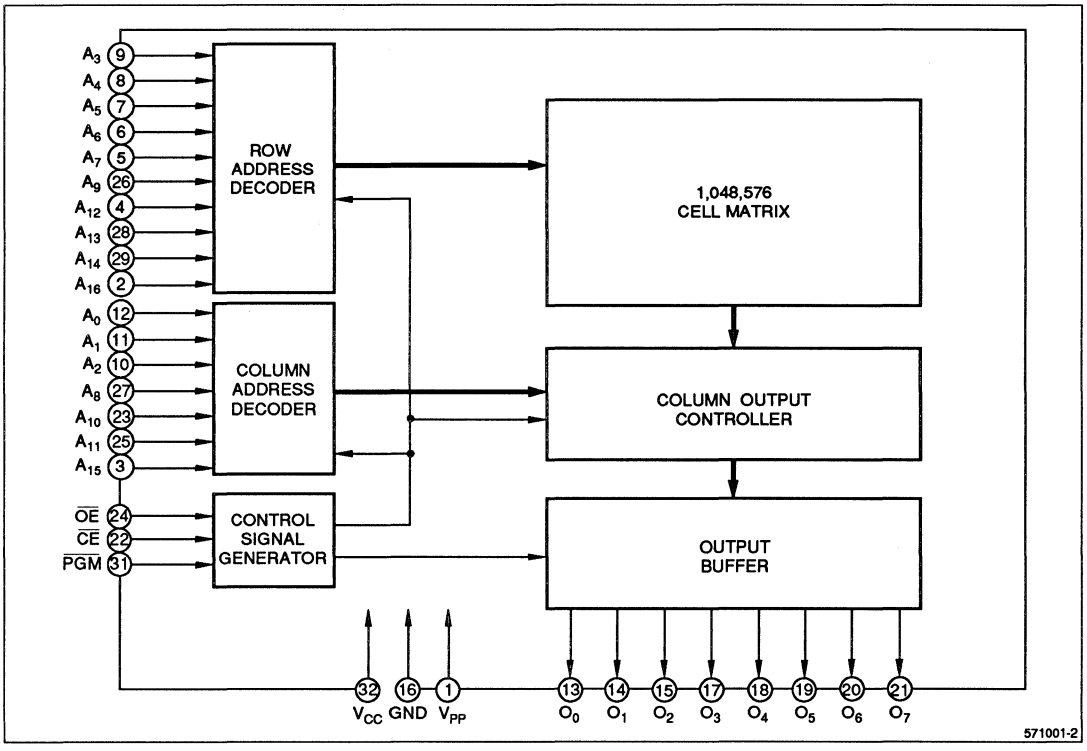


Figure 2. LH571001/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	
$\overline{PGM}$	Program input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	X	+5 V	+5 V
	Output disable	High-Z	L	H	X	+5 V	+5 V
	Standby	High-Z	H	X	X	+5 V	+5 V
Program	Program	Data in	L	H	L	+6.5 V	+12.75 V
	Program verify	Data out	L	L	H	+6.5 V	+12.75 V
	Program inhibit	High-Z	H	X	X	+6.5 V	+12.75 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	-0.1		5.5	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, $V_{PP} \leq V_{CC}$, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}$ = GND ± 0.3 V			40	mA	1, 2
	I_{CC2}	$\overline{CE}$ = V_{IL}			40	mA	1, 3
V_{PP} supply current	I_{PP}	$V_{PP} \leq V_{CC}$			10	µA	
V_{PP} pin voltage	V_{PP}		0.1		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}$ = V_{CC} ± 0.3 V			100	µA	2
	I_{SB2}	$\overline{CE}$ = V_{IH}			2	mA	3

NOTES:
1. f = 5MHz, I_{OUT} = 0 mA
2. CMOS input: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL input: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH571001J-12		LH571001J-15 LH571001-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		120		150	ns
$\overline{CE}$ to output delay	t_{CE}		120		150	ns
$\overline{OE}$ to output delay	t_{OE}		40		50	ns
Output disable high to output float	t_{DF}	0	40	0	50	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.45 V to 2.4 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

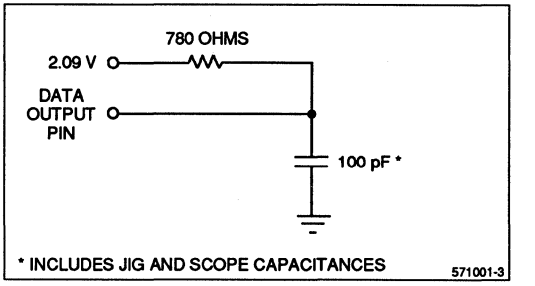


Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

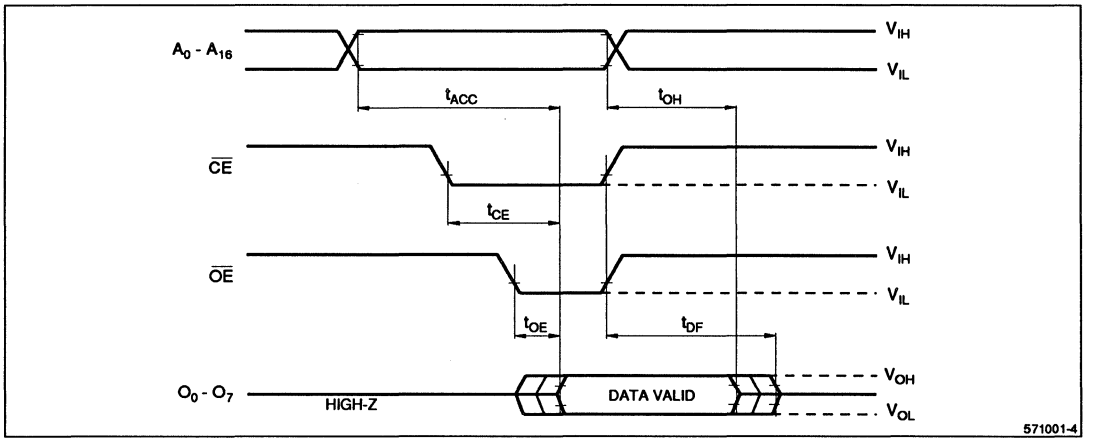


Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75		6.75	V
	V_{PP}	12.5	12.75	13.0	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 4.75 V to 6.75 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = V_{CC}$ or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				40	mA
V_{PP} supply current	I_{PP}	$\overline{CE} = \overline{PGM} = V_{IL}$			50	µA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program Mode)

(V_{CC} = 4.75 to 6.75 V, V_{PP} = 12.75 ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
Data setup time	t_{DS}	2			µs
Output enable setup time	t_{OES}	2			µs
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Data valid from output enable	t_{OE}			150	ns
Chip enable to output float delay	t_{DF}	0		150	ns
V_{PP} setup time	t_{VPS}	2			µs
V_{CC} setup time	t_{VCS}	2			µs
Program pulse width*	t_{PW}	95	100	105	µs
Chip enable setup time	t_{CES}	2			µs

* The pulse width is defined by the Program Flowchart (Figure 6).

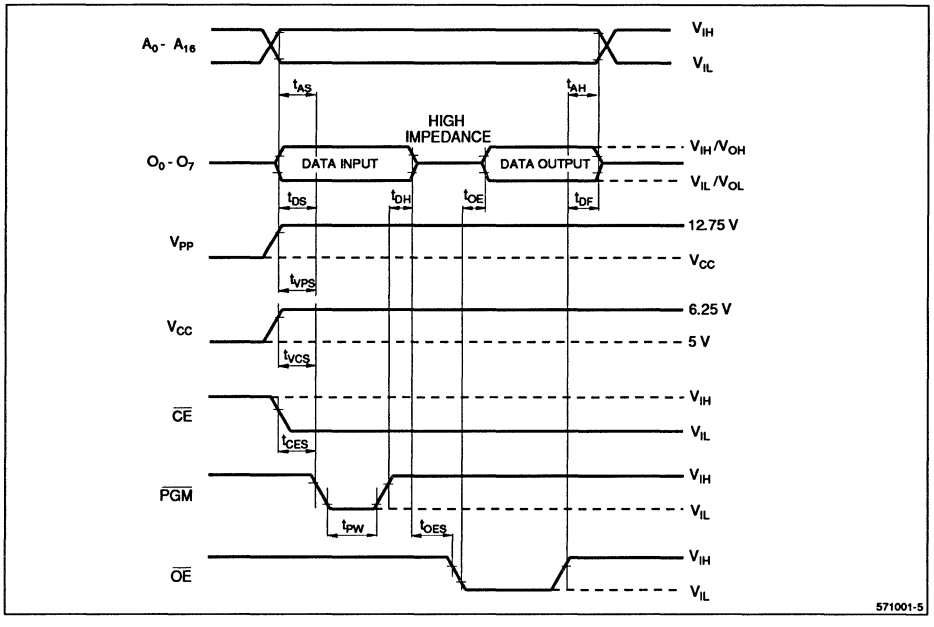


Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see Erasure section), the LH571001 and LH571001J have all 131,072 × 8 bits in the "1", or high state. "0's" are loaded into the LH571001 and LH571001J through the procedure of programming.

The programming mode is entered when +12.75 V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH571001J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH571001J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH571001J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH571001J and similar devices will erase with light sources having wave-length shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH571001J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

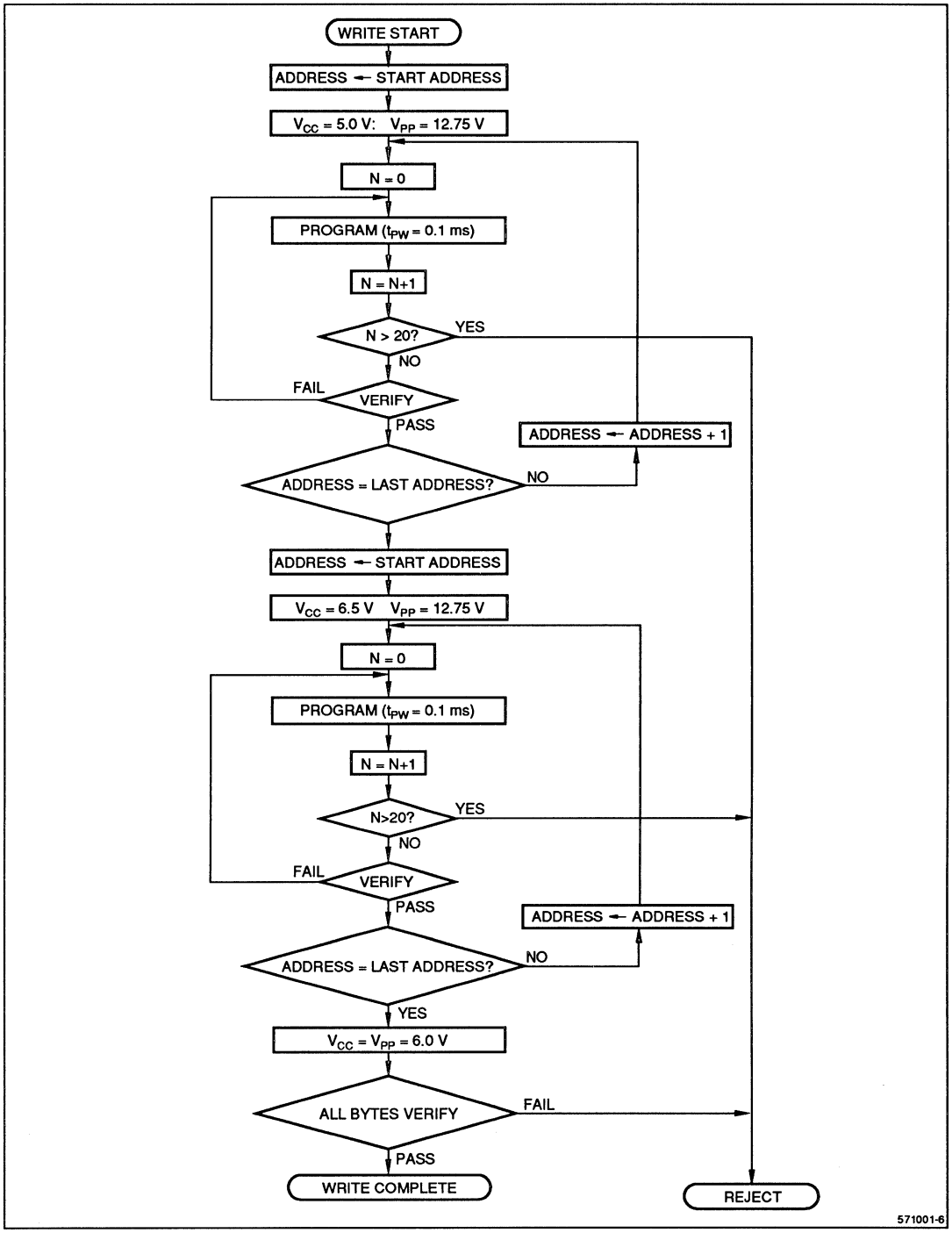
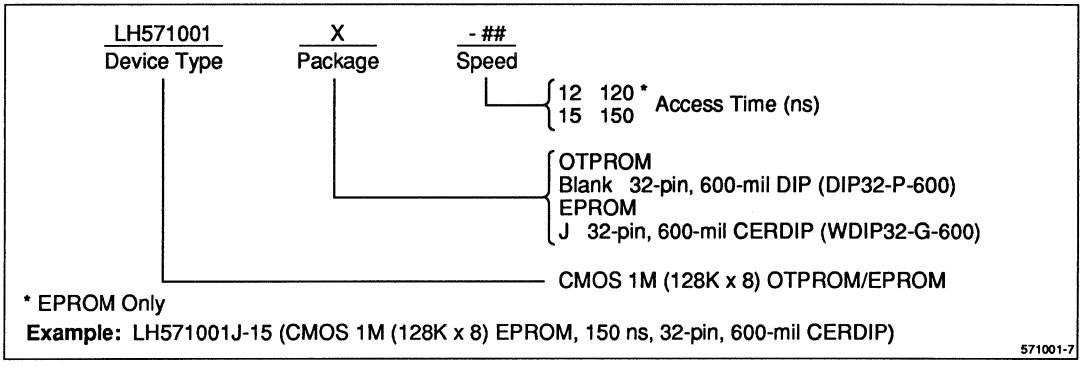


Figure 6. Programming Flowchart

ORDERING INFORMATION



LH2369

NMOS 64K (8K × 8) Mask Programmable ROM

FEATURES

- 8,192 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 330 mW (MAX.)
  Standby: 220 mW (MAX.)
- Programmable $S_1/\overline{S}_1$/DC and $S_2/\overline{S}_2$/DC
  (Selectable CE or OE type)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
- JEDEC standard EPROM pinout

DESCRIPTION

The LH2369 is a mask programmable ROM organized as 8,192 × 8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

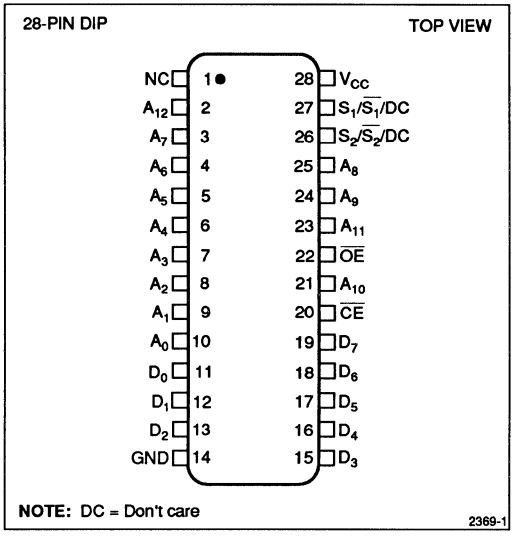


Figure 1. Pin Connections for DIP Package

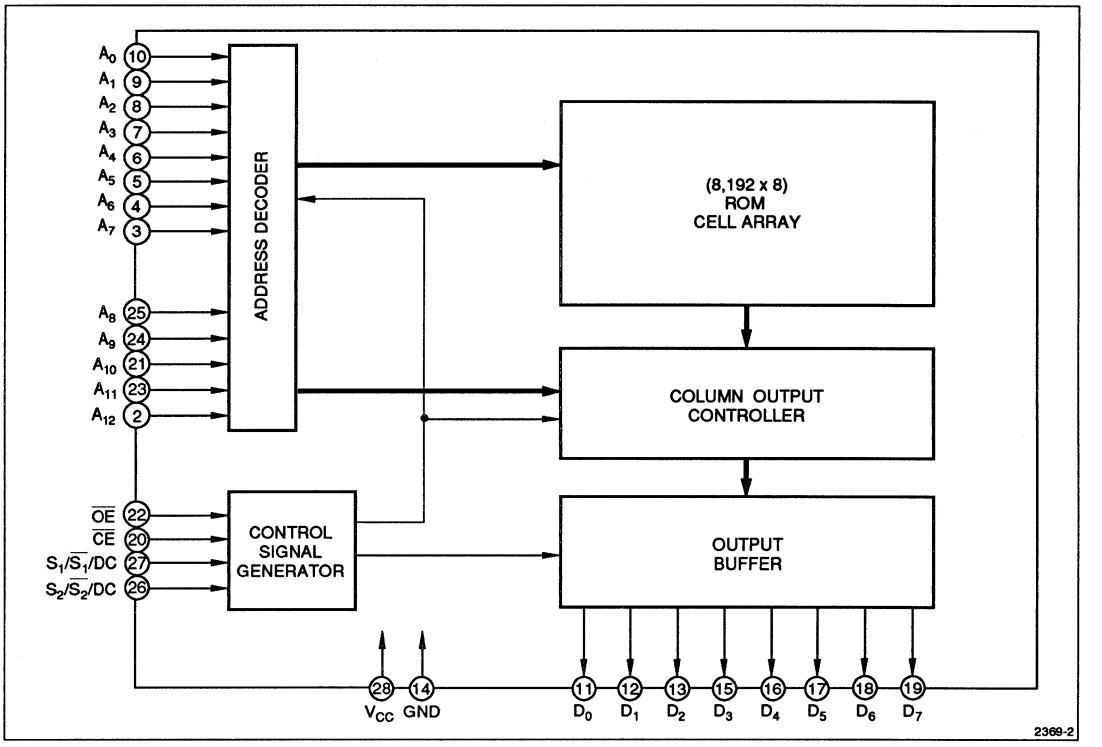


Figure 2. LH2369 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{12}	Address input	
D_0 - D_7	Data output	
$S_1/\overline{S_1}$/DC $S_2/\overline{S_2}$/DC	Function select/Don't care	1, 2
$\overline{OE}$	Output enable input	

SIGNAL	PIN NAME	NOTE
$\overline{CE}$	Chip enable input	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. Pin 26 and pin 27 are used to select either CE or OE by mask program.
   The active level of these pins are also mask programmable. Selecting DC allows the chip to be active for both high and low levels applied to these pins. However, it is recommended to apply either a "High" or "Low" to the DC pin.
2.

	CE TYPE	OE TYPE
$S_1/\overline{S_1}$/DC	$CE_1/\overline{CE_1}$/DC	$OE_1/\overline{OE_1}$/DC
$S_2/\overline{S_2}$/DC	$CE_2/\overline{CE_2}$/DC	$OE_2/\overline{OE_2}$/DC

TRUTH TABLE

(1) TYPE 1 (CE TYPE OF S_1 AND S_2)

$\overline{CE}$	$CE_1/\overline{CE_1}$	$CE_2/\overline{CE_2}$	$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z	Standby (I_{SB})	1
X	L/H	X	X	Non selected	High-Z	Standby (I_{SB})	
X	X	L/H	X	Non selected	High-Z	Standby (I_{SB})	
L	H/L	H/L	H	Non selected	High-Z	Operating (I_{CC})	
L	H/L	H/L	L	Selected	D_{OUT}	Operating (I_{CC})	

(2) TYPE 2 (OE TYPE OF S_1 AND S_2)

$\overline{CE}$	$OE_1/\overline{OE_1}$	$OE_2/\overline{OE_2}$	$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z	Standby (I_{SB})	1
L	L/H	X	X	Non selected	High-Z	Operating (I_{CC})	
L	X	L/H	X	Non selected	High-Z	Operating (I_{CC})	
L	X	X	H	Non selected	High-Z	Operating (I_{CC})	
L	H/L	H/L	L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Output voltage	V_{OUT}	-0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -200 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC}	t_{RC} = 200 ns, outputs open		30	60	mA	2
Standby current	I_{SB}			20	40	mA	3

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{S_1}/\overline{S_2} = V_{IH}$ or $S_1/S_2 = V_{IL}$
2. $V_{IN} = V_{IH}/V_{IL}$, $\overline{CE} = V_{IL}$, $CE_1/\overline{CE_1} = V_{IH}/V_{IL}$, $CE_2/\overline{CE_2} = V_{IH}/V_{IL}$ (CE type)
3. $\overline{CE} = V_{IH}$, $CE_1/\overline{CE_1} = V_{IL}/V_{IH}$ or $CE_2/\overline{CE_2} = V_{IL}/V_{IH}$ (CE type)

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
$\overline{CE}$ output delay time	t_{ACE}			200	ns	
$\overline{OE}$ output delay time	t_{OE}			100	ns	
Chip enable to output in High-Z	t_{CHZ}			60	ns	1
Output enable to output in High-Z	t_{OHZ}			60	ns	
Output hold time	t_{OH}	0			ns	

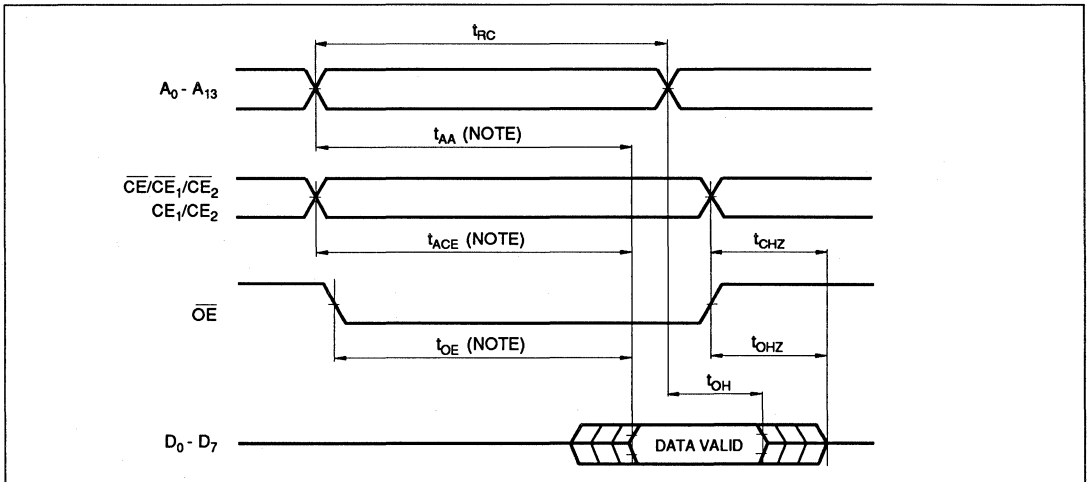
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.0 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V			12	pF



NOTE: Data becomes valid after t_{AA}, t_{ACE} and t_{OE} from address input, chip enable input and output enable input respectively have been met.

2369-3

Figure 3. Type 1 (CE Type of S_1 and S_2)

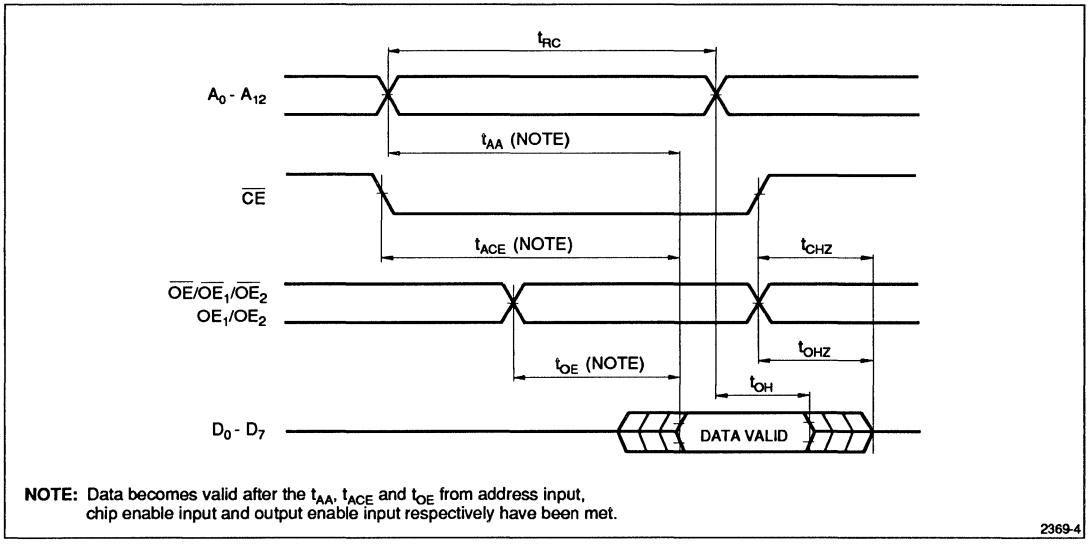
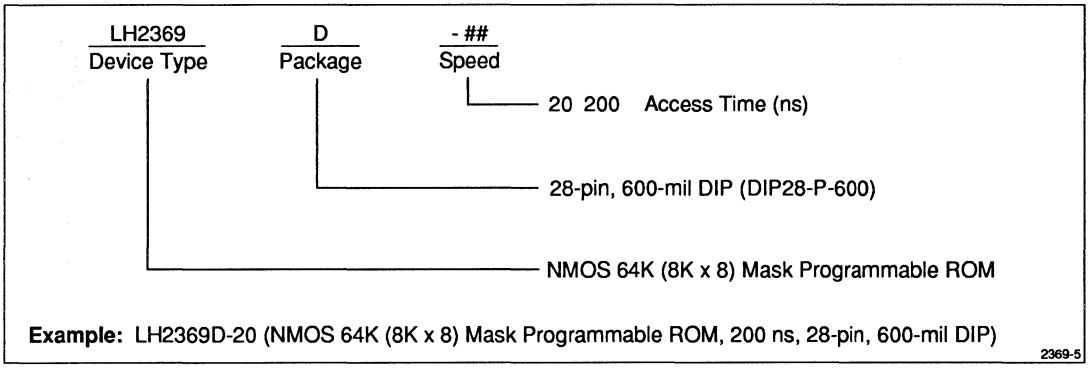


Figure 4. Type 2
(OE Type of S_1 and S_2)

ORDERING INFORMATION



LH23126

NMOS 128K (16K × 8) Mask Programmable ROM

FEATURES

- 16,384 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 440 mW (MAX.)
- Mask-programmable chip enable
  $CE_0/\overline{CE}_0$/NC, $CE_1/\overline{CE}_1$/NC
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
- JEDEC standard EPROM pinout

DESCRIPTION

The LH23126 is a mask programmable ROM organized as 16,384 × 8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

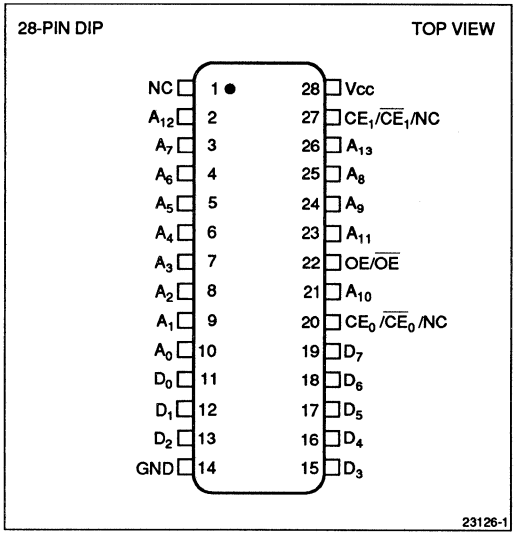


Figure 1. Pin Connections for DIP Package

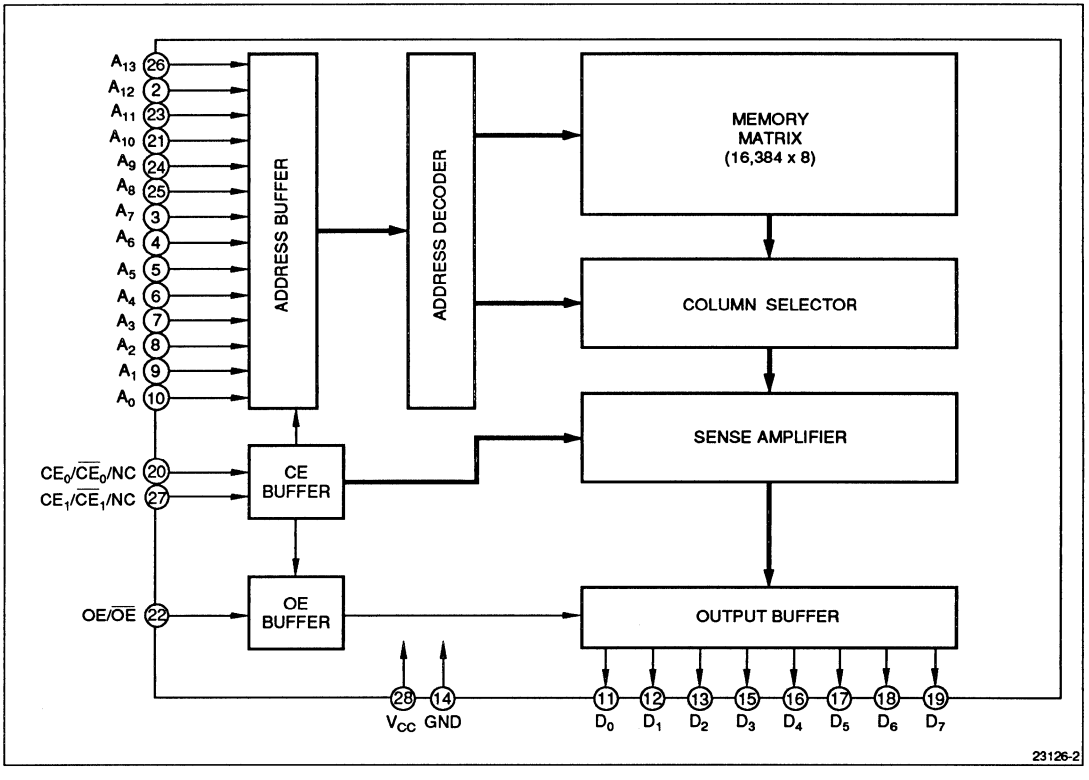


Figure 2. LH23126 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{13}	Address input	
D_0 - D_7	Data output	
$CE_0/\overline{CE_0}$/NC	Chip enable input/non-connection	1
$CE_1/\overline{CE_1}$/NC	Chip enable input/non-connection	1

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. The active level and non-connection of $CE_0/\overline{CE_0}$/NC, $CE_1/\overline{CE_1}$/NC, OE/$\overline{OE}$ are mask programmable.

TRUTH TABLE

$CE_0/\overline{CE_0}$	$CE_1/\overline{CE_1}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
L/H	X	X	Non selected	High-Z	Standby (I_{SB})	1
X	L/H	X				
H/L	H/L	L/H			Operating (I_{CC})	
H/L	H/L	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Output voltage	V_{OUT}	-0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage		V_{IL}		-0.3		0.8	V	
Input "High" voltage		V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage		V_{OL}	I_{OL} = 3.2 mA			0.4	V	
Output "High" voltage		V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current		$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current		$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Current consumption	Operating	I_{CC}	t_{RC} = t_{RC} (MIN.)			80	mA	2
	Standby	I_{SB}				40	mA	3

NOTES:
1. $\overline{CE_0}/\overline{CE_1}/\overline{OE}$ = V_{IH} or $CE_0/CE_1/OE$ = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $CE_0/\overline{CE_0}$ = V_{IH}/V_{IL}, $CE_1/\overline{CE_1}$ = V_{IH}/V_{IL}, outputs open.
3. $CE_0/\overline{CE_0}$ = V_{IL}/V_{IH} or $CE_1/\overline{CE_1}$ = V_{IL}/V_{IH}

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable time	t_{ACE}			200	ns	
Output enable time	t_{OE}			100	ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	
Output hold time	t_{OH}	10			ns	

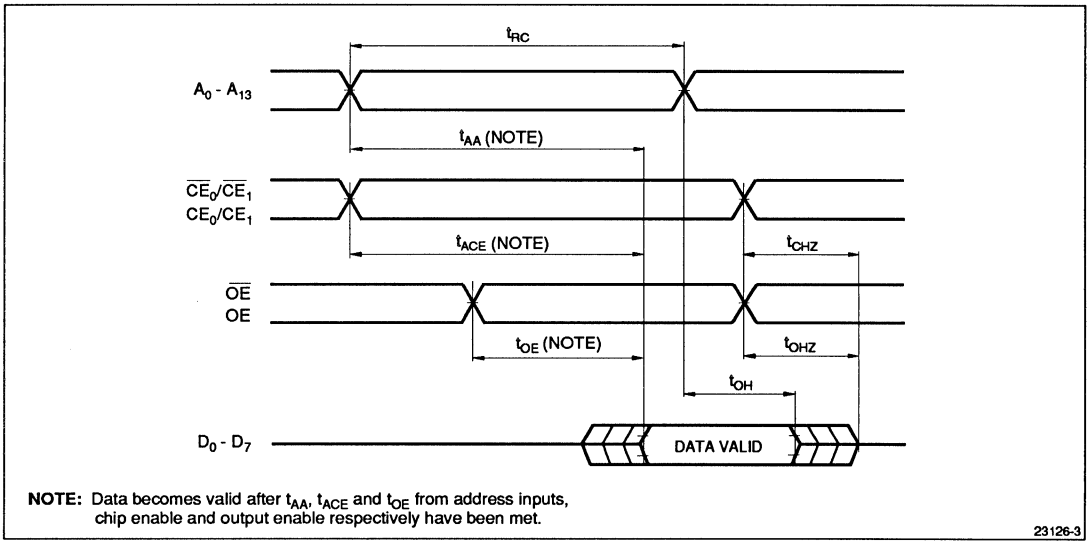
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.0 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			8	pF
Output capacitance	C_{OUT}			10	pF

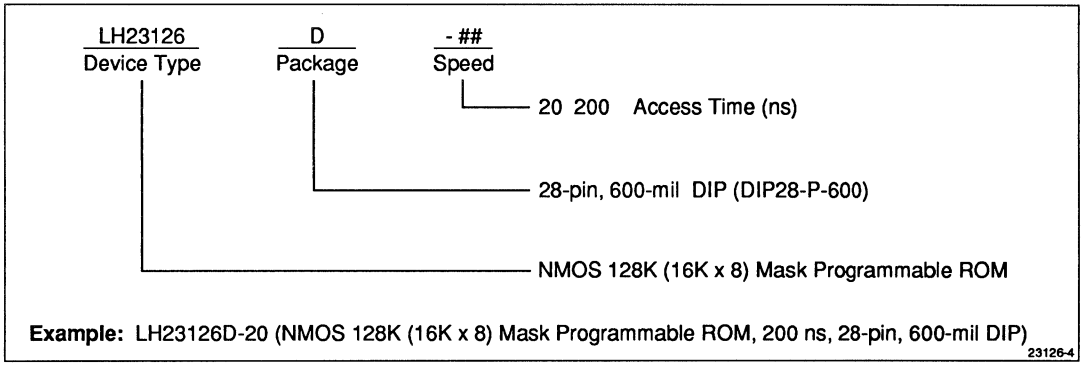


NOTE: Data becomes valid after t_{AA}, t_{ACE} and t_{OE} from address inputs, chip enable and output enable respectively have been met.

23126-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH23126D-20 (NMOS 128K (16K x 8) Mask Programmable ROM, 200 ns, 28-pin, 600-mil DIP)

23126-4

LH23255

NMOS 256K (32K × 8) Mask Programmable ROM

FEATURES

- 32,768 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 440 mW (MAX.)
  Standby: 248 mW (MAX.)
- Programmable CE/$\overline{CE}$ and OE/$\overline{OE}$
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
- JEDEC standard EPROM pinout

DESCRIPTION

The LH23255 is a mask programmable ROM organized as 32,768 × 8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

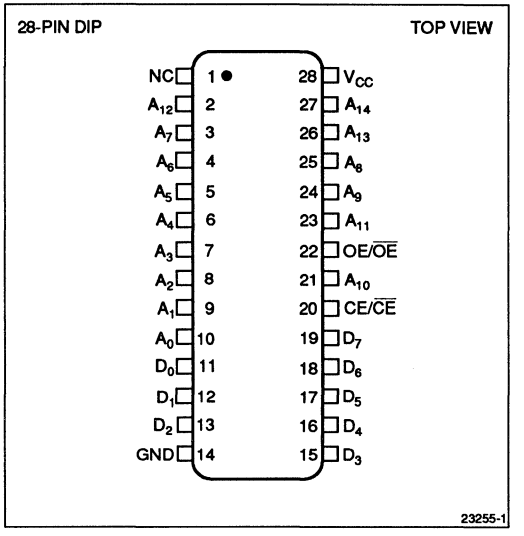


Figure 1. Pin Connections for DIP Package

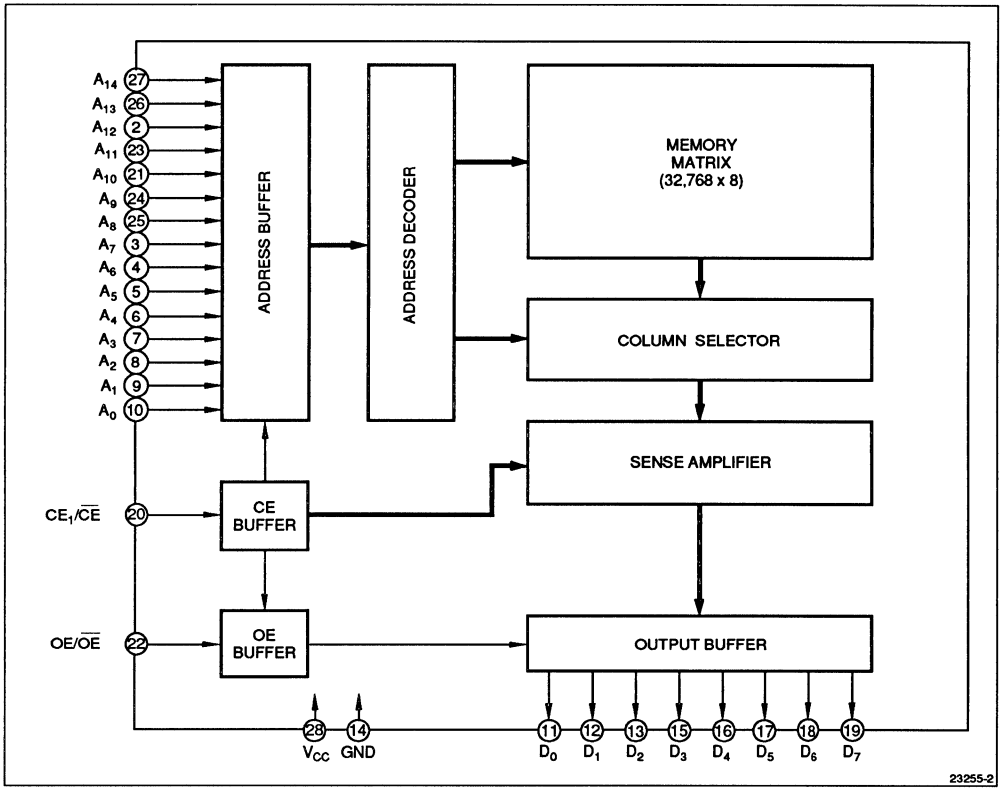


Figure 2. LH23255 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
D_0 - D_7	Data output	
CE/$\overline{CE}$	Chip enable input	1
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	Non connection	

NOTE:
1. The active level of CE/$\overline{CE}$ and OE/$\overline{OE}$ are mask programmable.

TRUTH TABLE

CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
L/H	X	Non selected	High-Z	Standby (I_{SB})	1
H/L	L/H			Operating (I_{CC})	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	
Output voltage	V_{OUT}	-0.3 to +7.0	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage		V_{IL}		-0.3		0.8	V	
Input "High" voltage		V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage		V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage		V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current		$\|I_{LI}\|$	V_{IN} = 0 to V_{CC}			10	µA	
Output leakage current		$\|I_{LO}\|$	V_{OUT} = 0 to V_{CC}			10	µA	1
Current consumption	Operating	I_{CC}	t_{RC} = t_{RC} (MIN.)			80	mA	2
	Standby	I_{SB}	CE = V_{IL}, $\overline{CE}$ = V_{IH}			45	mA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or CE/OE = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, CE = V_{IH}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Access time	t_{AA}			200	ns	
Chip enable time	t_{ACE}			200	ns	
Output enable time	t_{OE}			80	ns	
CE to output in High-Z	t_{CHZ}			80	ns	1
OE to output in High-Z	t_{OHZ}			80	ns	
Output hold time	t_{OH}	10			ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			8	pF
Output capacitance	C_{OUT}			10	pF

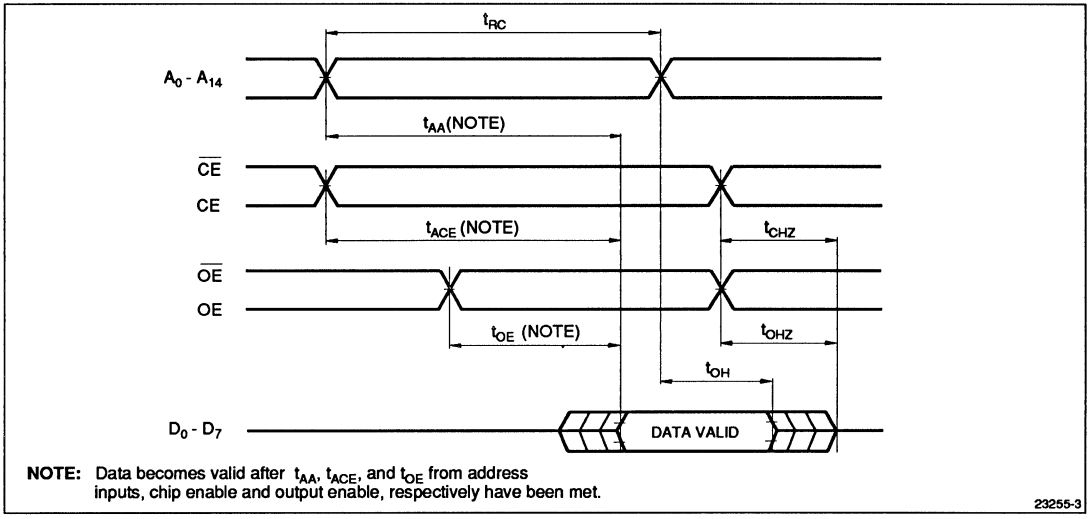
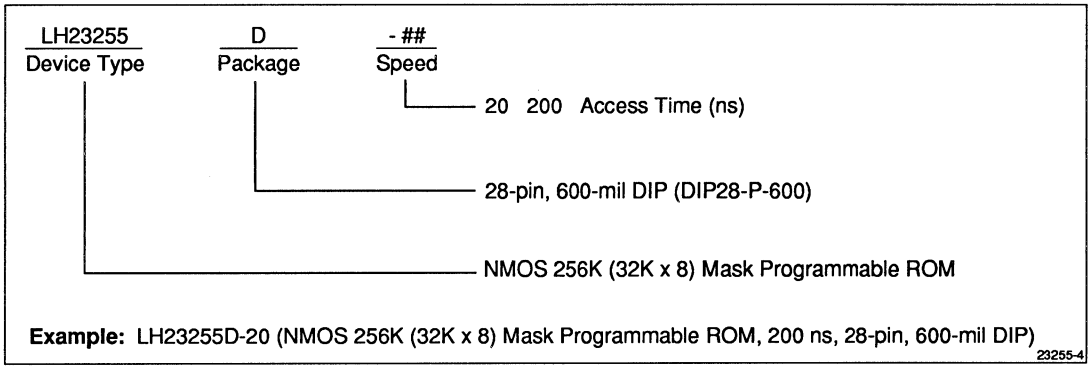


Figure 3. Timing Diagram

ORDERING INFORMATION



LH23512

NMOS 512K (64K × 8) Mask Programmable ROM

FEATURES

- 65,536 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 550 mW (MAX.)
  Standby: 110 mW (MAX.)
- Programmable CE/$\overline{CE}$ and OE/$\overline{OE}$
- Fully static operation (No clock required)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
- JEDEC standard EPROM pinout

DESCRIPTION

The LH23512 is a mask programmable ROM organized as 65,536×8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

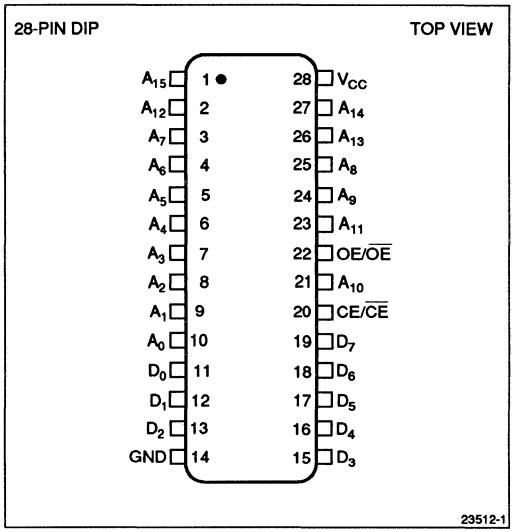


Figure 1. Pin Connections for DIP Package

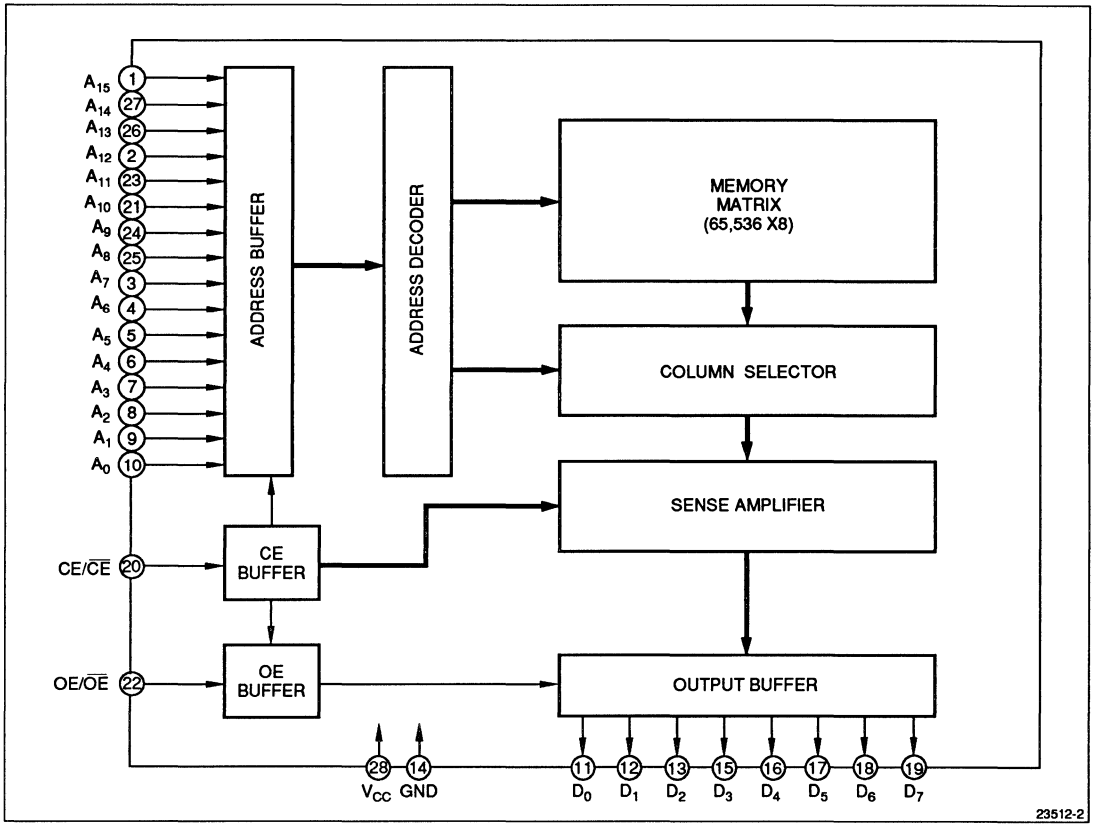


Figure 2. LH23512 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{15}	Address input	
D_0 - D_7	Data output	
CE/$\overline{CE}$	Chip enable input	1

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. The active level of CE/$\overline{CE}$ and OE/$\overline{OE}$ are mask programmable.

TRUTH TABLE

CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
L/H	X	Non selected	High-Z	Standby (I_{SB})	1
H/L	L/H	Non selected	High-Z	Operating (I_{CC})	
H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Output voltage	V_{OUT}	-0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to + 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage		V_{IL}		-0.3		0.8	V	
Input "High" voltage		V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage		V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage		V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current		$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}			10	µA	
Output leakage current		$\lvert I_{LO} \rvert$	V_{OUT} = 0 to V_{CC}			10	µA	1
Current consumption	Operating	I_{CC}	t_{RC} = 200 ns			100	mA	2
	Standby	I_{SB}	CE ≤ V_{IL}, $\overline{CE}$ ≥ V_{IH}			20	mA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or CE/OE = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, CE = V_{IH}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable time	t_{ACE}			200	ns	
Output enable time	t_{OE}			80	ns	
Output floating time	t_{CHZ}			80	ns	1
	t_{OHZ}			80	ns	
Output hold time	t_{OH}	10			ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			8	pF
Output capacitance	C_{OUT}			10	pF

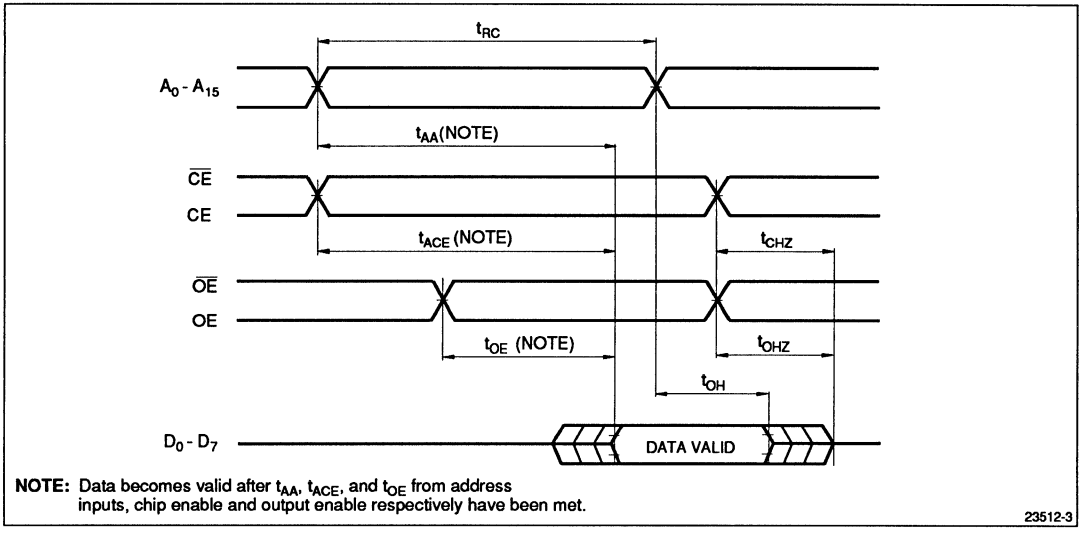
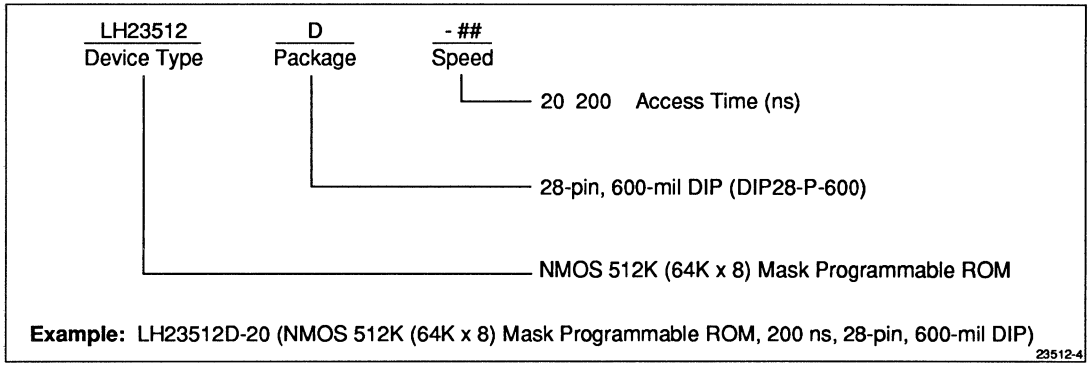


Figure 3. Timing Diagram

ORDERING INFORMATION



LH231000B NMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 550 mW (MAX.)
- Programmable OE/$\overline{OE}$
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  28-pin, 600-mil DIP
- Mask ROM specific pinout

DESCRIPTION

The LH231000B is a mask programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

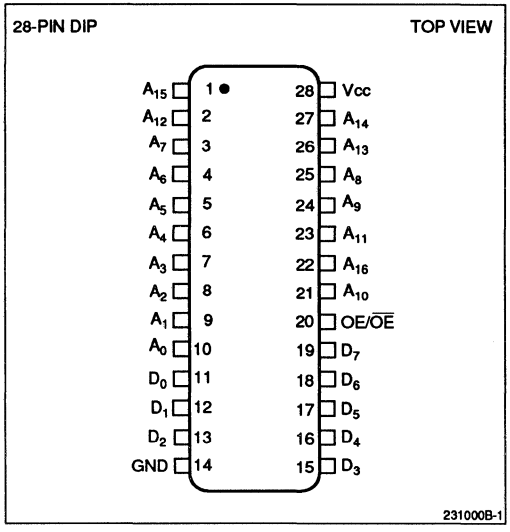


Figure 1. Pin Connections for DIP Package

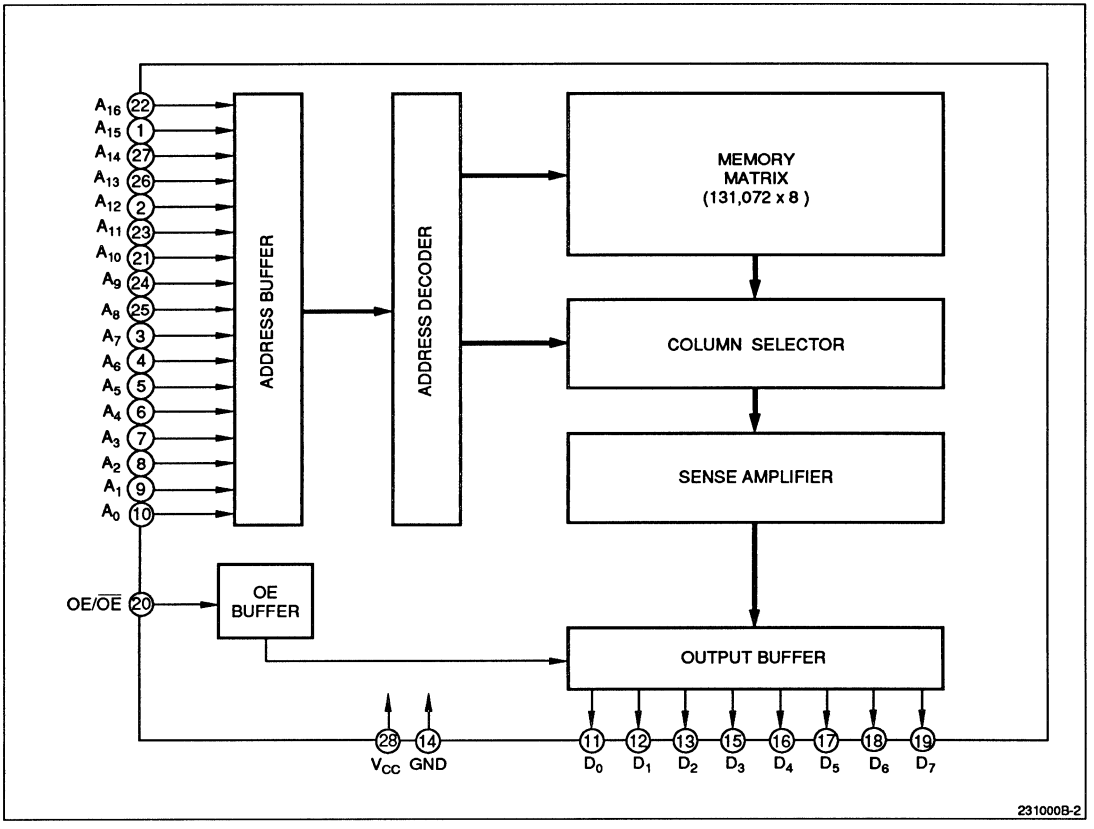


Figure 2. LH231000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$/OE/$\overline{OE}$	Chip enable or Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. The $\overline{CE}$/OE/$\overline{OE}$ function is mask programmable.

TRUTH TABLE

OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
L/H	Non selected	High-Z	Operating (I_{CC})
H/L	Selected	D_{OUT}	Operating (I_{CC})

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	
Output voltage	V_{OUT}	-0.3 to +7.0	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage		V_{IL}		-0.3		0.8	V	
Input "High" voltage		V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage		V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage		V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current		$\|I_{LI}\|$	V_{IN} = 0 to V_{CC}			10	µA	
Output leakage current		$\|I_{LO}\|$	V_{OUT} = 0 to V_{CC}			10	µA	1
Current consumption	Operating	I_{CC}	t_{RC} = t_{RC} (MIN.)			100	mA	2

NOTES:
1. $\overline{OE}$ = V_{IH} or OE = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Access time	t_{AA}			200	ns	
Output enable time	t_{OE}			80	ns	
Output floating time	t_{OHZ}			80	ns	1
Ouput hold time	t_{OH}	10			ns	

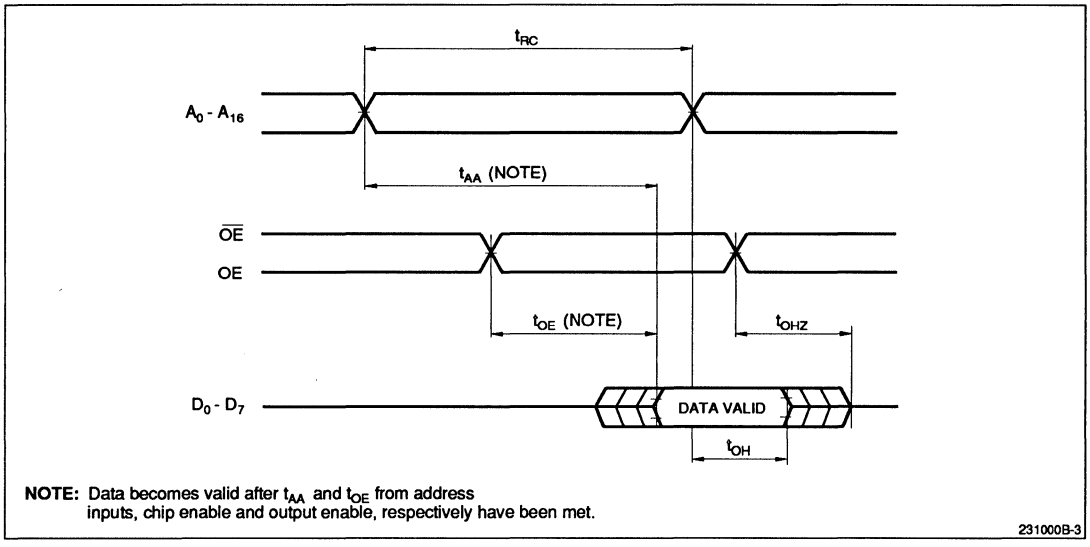
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			8	pF
Output capacitance	C_{OUT}			12	pF

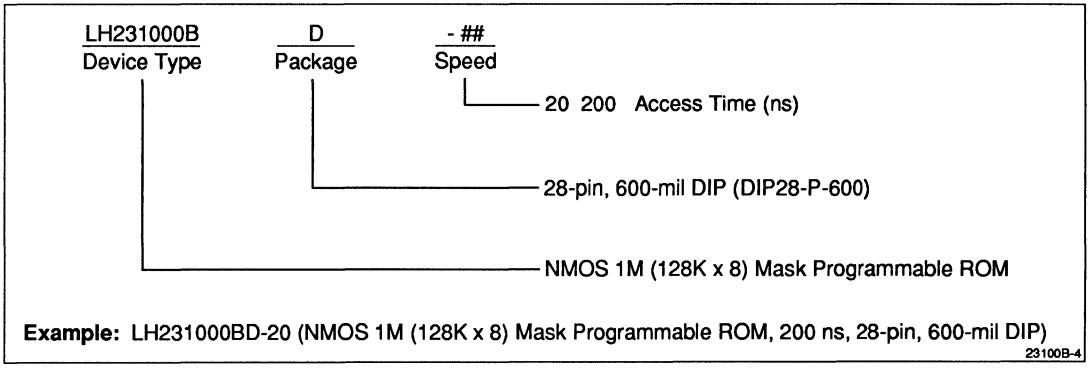


NOTE: Data becomes valid after t_{AA} and t_{OE} from address inputs, chip enable and output enable, respectively have been met.

231000B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH231000BD-20 (NMOS 1M (128K x 8) Mask Programmable ROM, 200 ns, 28-pin, 600-mil DIP)

23100B-4

LH231100B NMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 550 mW (MAX.)
- Mask-programmable $OE_1/\overline{OE}_1$/DC and $OE_2/\overline{OE}_2$/DC
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  32-pin, 600-mil DIP
  (32-pin compatible to 28-pin 1M mask ROM specific pinout)

DESCRIPTION

The LH231100B is a mask programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate NMOS process technology.

PIN CONNECTIONS

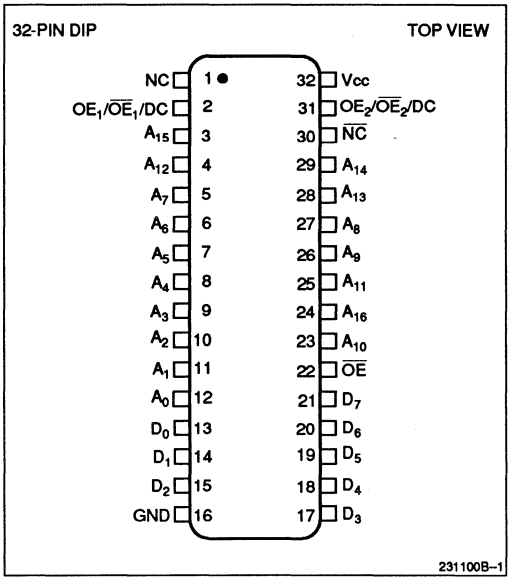


Figure 1. Pin Connections for DIP Package

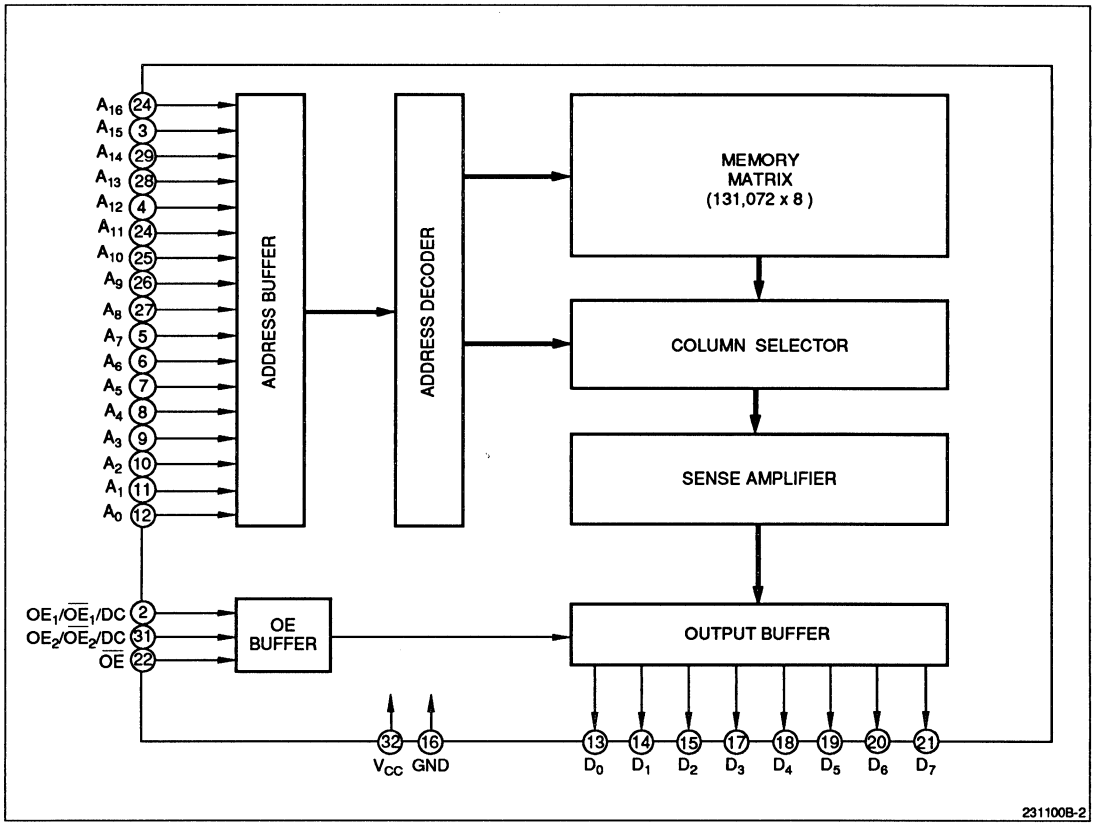


Figure 2. LH231100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
$OE_1/\overline{OE}_1/DC$ $OE_2/\overline{OE}_2/DC$	Output enable input or Don't Care connection	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active level of output enable is mask programmable. When DC is selected, it is fixed to an active level. (However, it is recommended to apply either "High" or "Low" to the DC pin).

TRUTH TABLE

$\overline{OE}$	$OE_1/\overline{OE}_1$	$OE_2/\overline{OE}_2$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Operating (I_{CC})	1
X	L/H	X				
X	X	L/H				
L	H/L	H/L	Selected	D_{OUT}		

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	
Output voltage	V_{OUT}	-0.3 to +7.0	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC}	t_{RC} = 200 ns			100	mA	2

NOTES:
1. $\overline{OE}/\overline{OE_1}/\overline{OE_2}$ = V_{IH} or OE_1/OE_2 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Output enable access time	t_{OE}			80	ns	
Output hold time	t_{OH}	10			ns	
OE to output in High-Z	t_{OHZ}			80	ns	1

NOTE:
1. This is the time required for the output to become high impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			8	pF
Output capacitance	C_{OUT}			12	pF

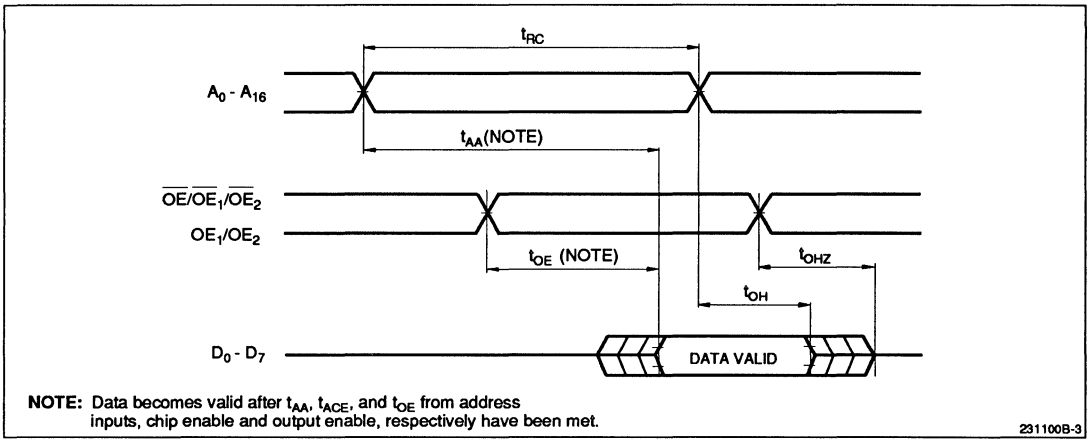
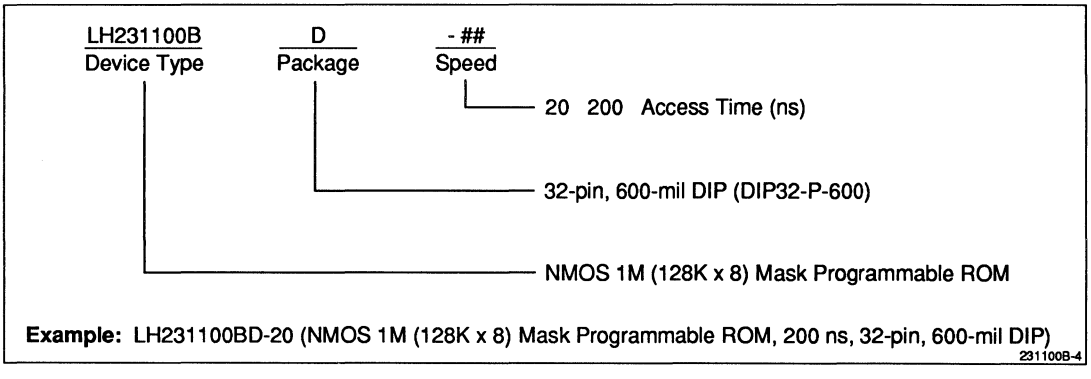


Figure 3. Timing Diagram

ORDERING INFORMATION



LH53259

CMOS 256K (32K × 8) Mask Programmable ROM

FEATURES

- 32,768 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 110 mW (MAX.)
  Standby: 82.5 μW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53259 is a mask programmable ROM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

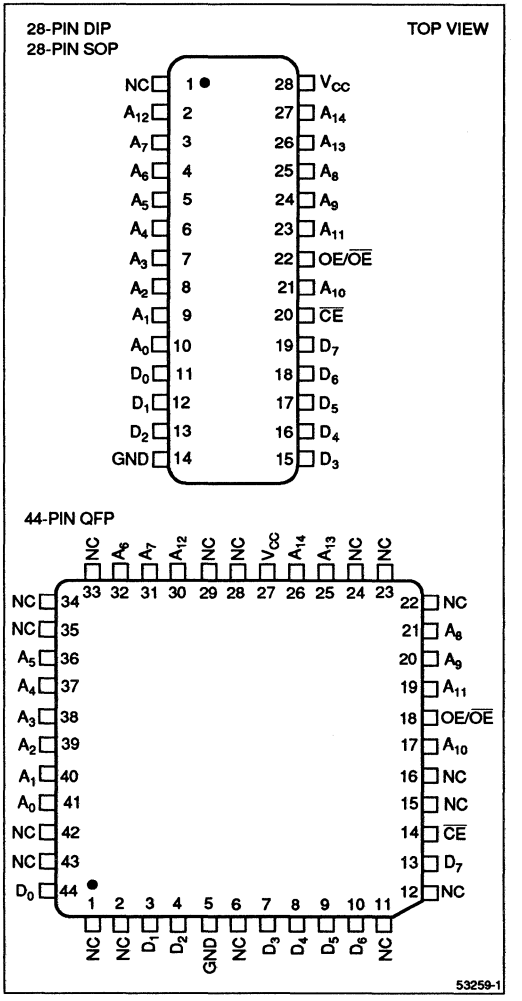


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

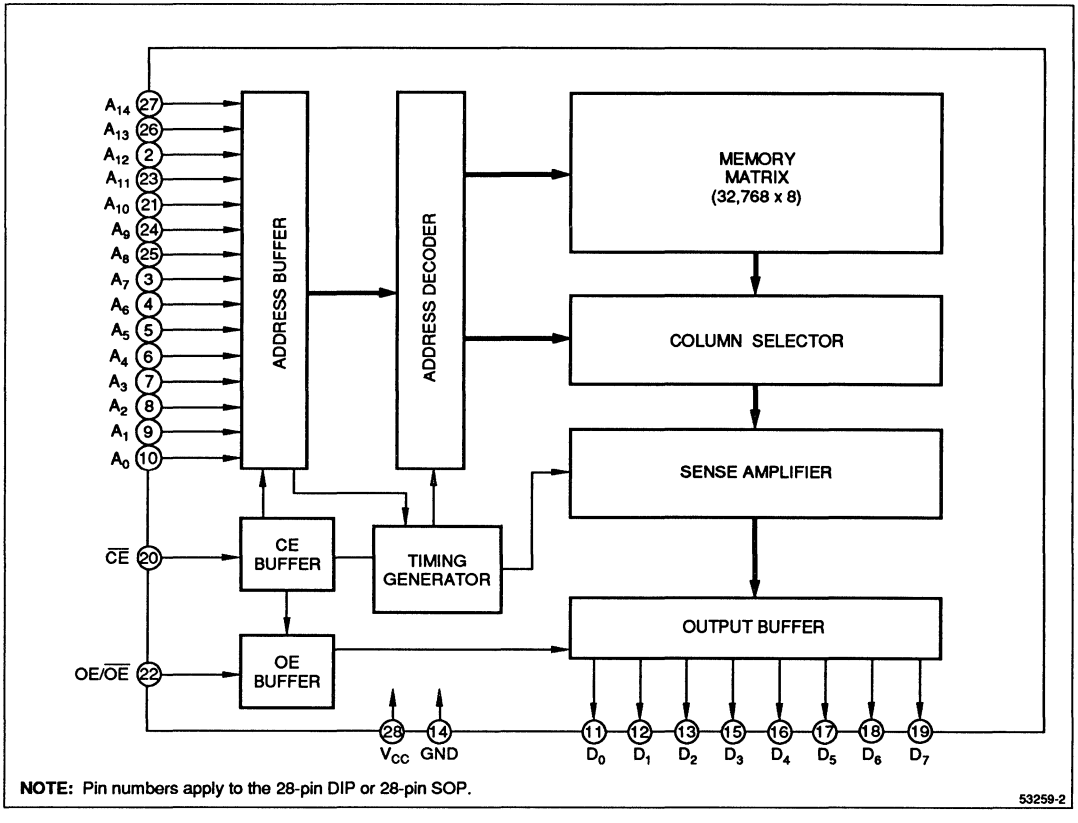


Figure 2. LH53259 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	Non connection	

NOTE:
1. The active level of OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby	1
L	L/H			Operating	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			20	mA	2
	I_{CC2}	t_{RC} = 1 µs			15		
	I_{CC3}	t_{RC} = 150 ns			15	mA	3
	I_{CC4}	t_{RC} = 1 µs			10		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			15	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or OE = VIL
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:
1. This is the time required for the output to become high impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

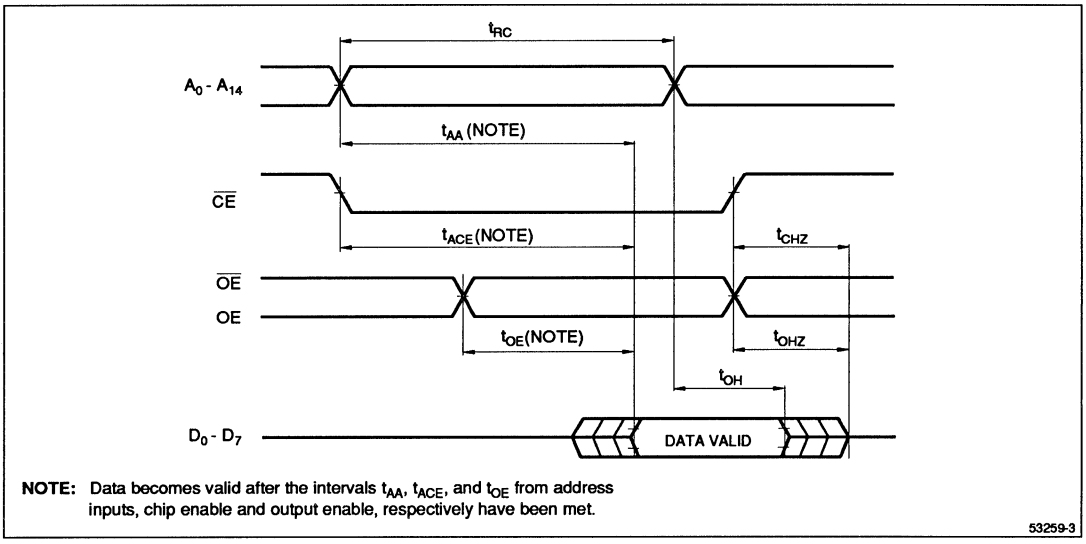


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

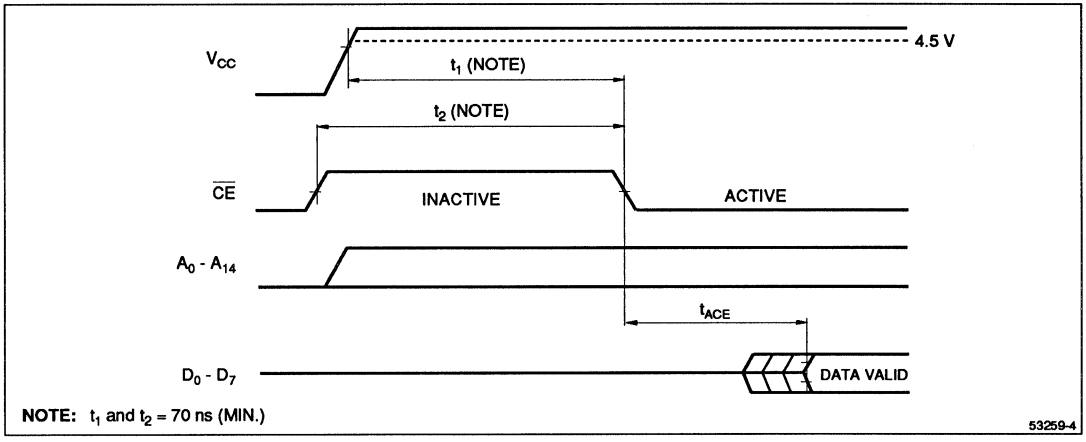


Figure 4. Power On With $\overline{CE}$ Inactive

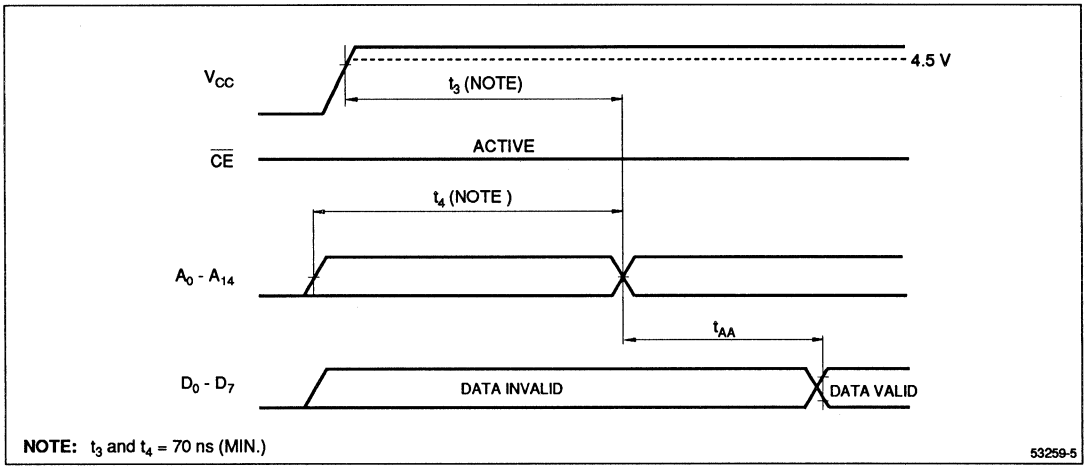
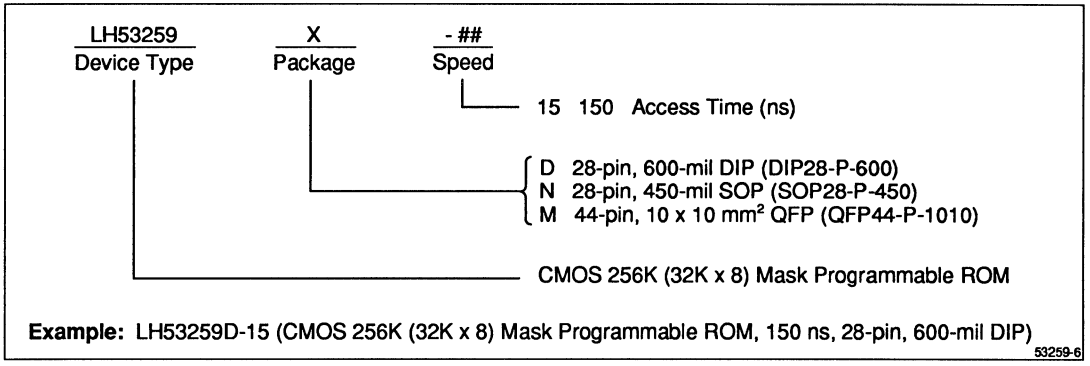


Figure 5. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



Example: LH53259D-15 (CMOS 256K (32K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)

53259-6

LH53515

CMOS 512K (64K × 8) Mask Programmable ROM

FEATURES

- 65,536 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 195 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

PIN CONNECTIONS

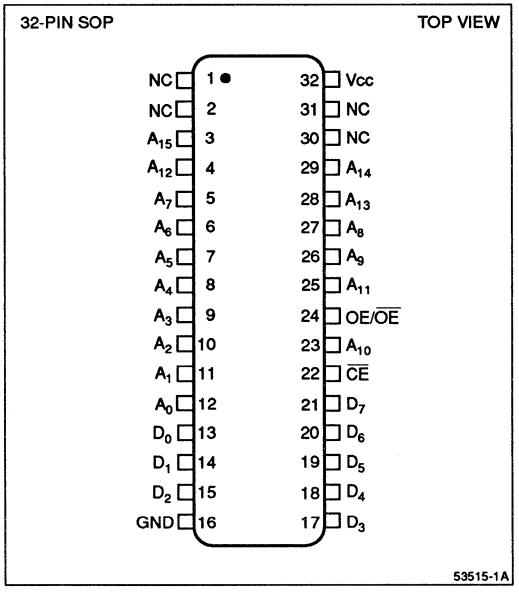


Figure 1. Pin Connections for SOP Package

DESCRIPTION

The LH53515 is a mask programmable ROM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

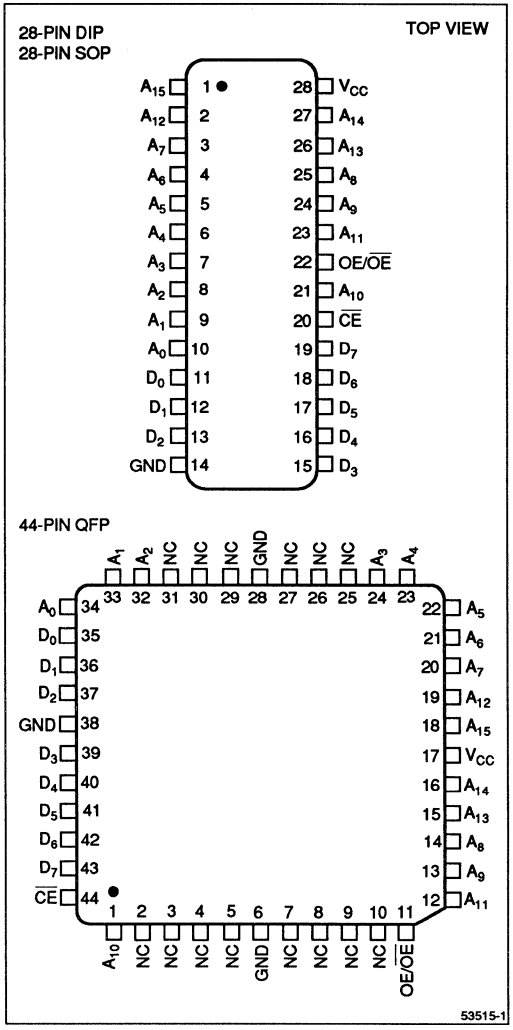


Figure 2. Pin Connections for DIP, SOP, and QFP Packages

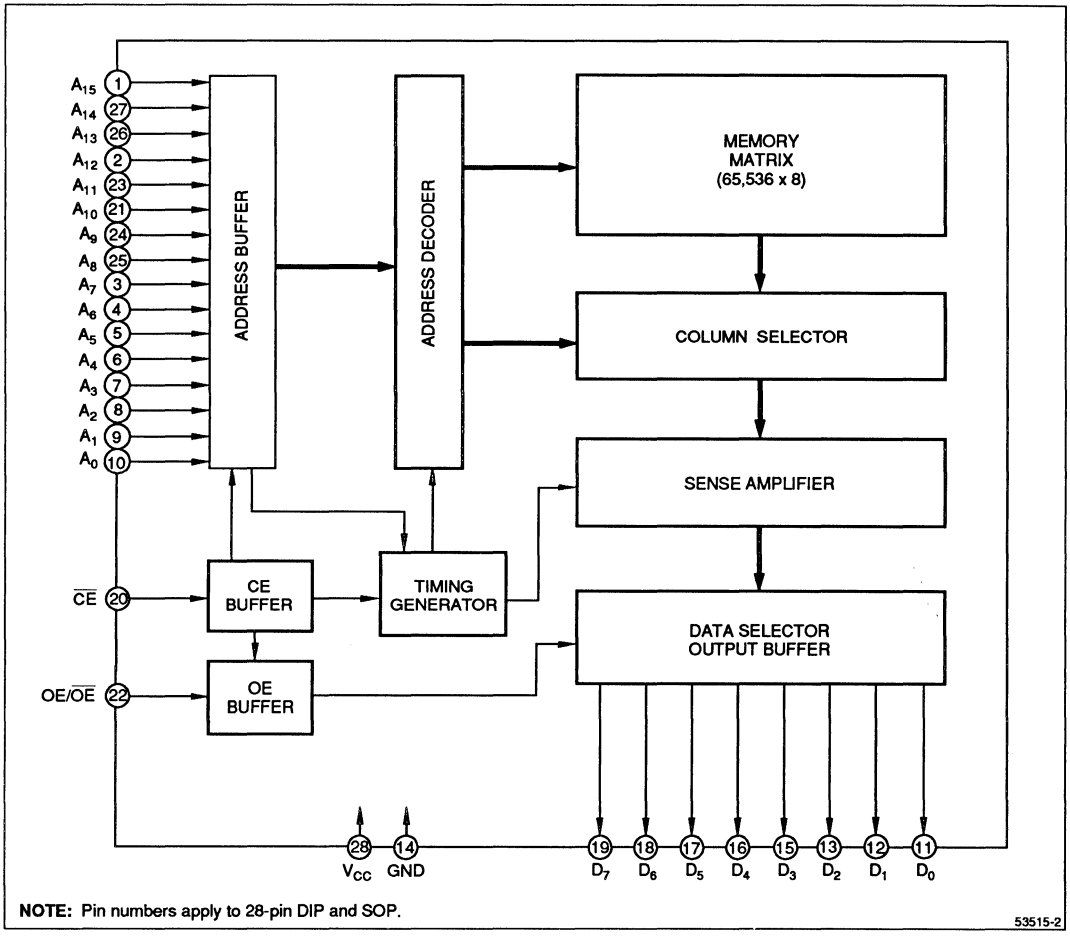


Figure 3. LH53515 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{15}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	CURRENT CONSUMPTION	NOTE
H	X	Non selected	High-Z	Standby(I_{SB})	1
L	L/H			Operating(I_{CC})	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL} or $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}				150	ns	
Output enable time	t_{OE}		10		80	ns	
Output hold time	t_{OH}		5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}				70	ns	1
OE to output in High-Z	t_{OHZ}				70	ns	1

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

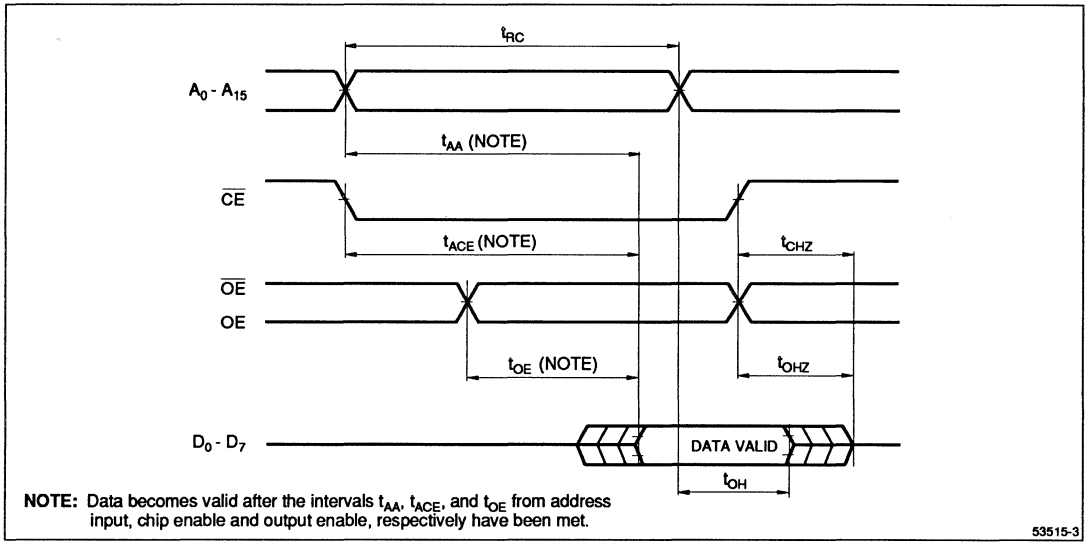


Figure 4. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses A_2 - A_{15} if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

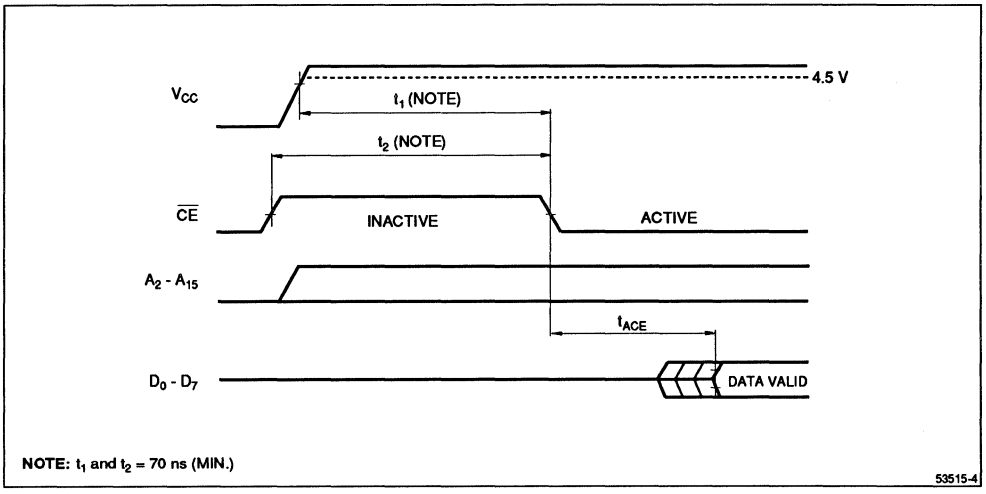


Figure 5. Power On With $\overline{CE}$ Inactive

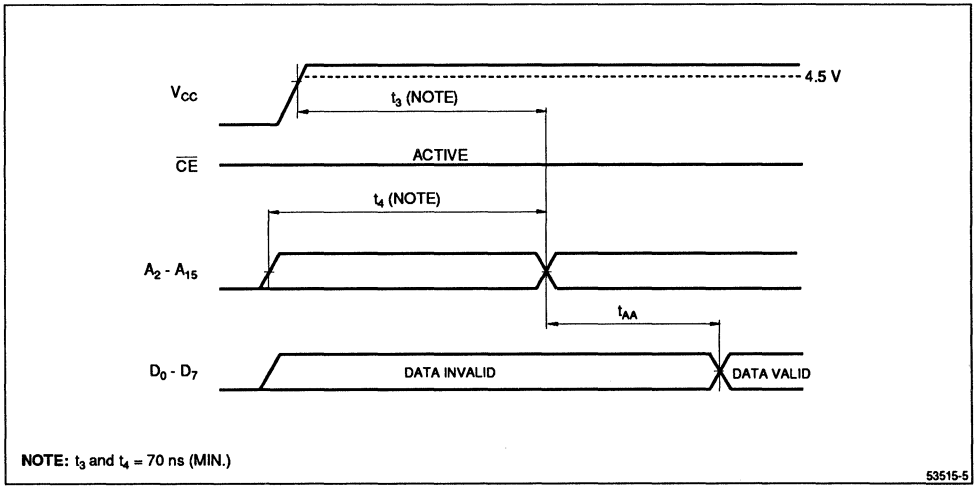
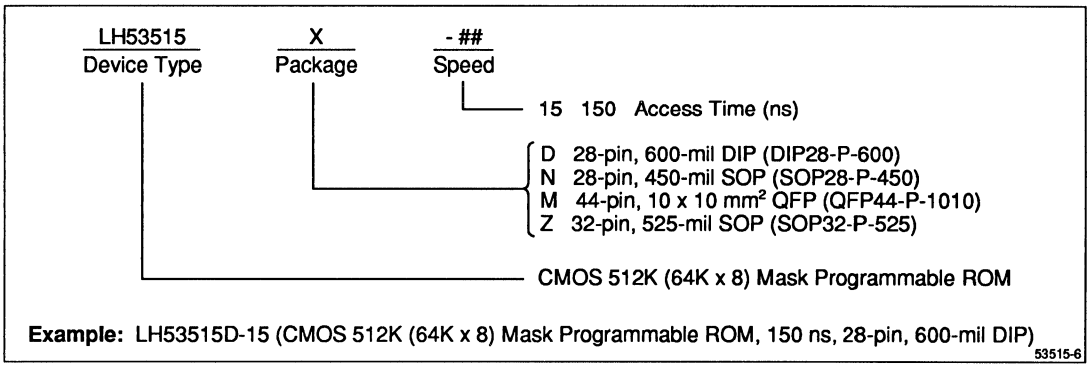


Figure 6. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



Example: LH53515D-15 (CMOS 512K (64K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)

53515-6

LH53H1000

PRELIMINARY

CMOS 1M (64K × 16) Mask Programmable ROM

FEATURES

- 65,536 × 16 bit organization
- Access time: 55 ns (MAX.)
- Power consumption:
  Operating: 660 mW (MAX.)
  Standby: 440 mW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53H1000 is a high speed mask programmable ROM organized as 65,536 × 16 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

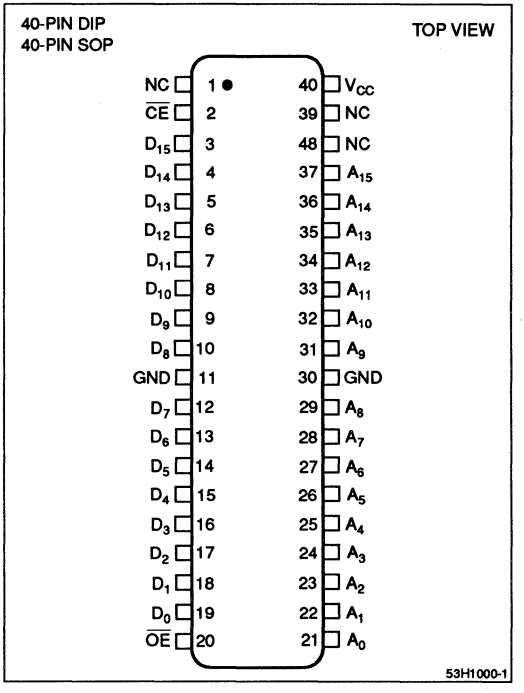


Figure 1. Pin Connections for DIP and SOP Packages

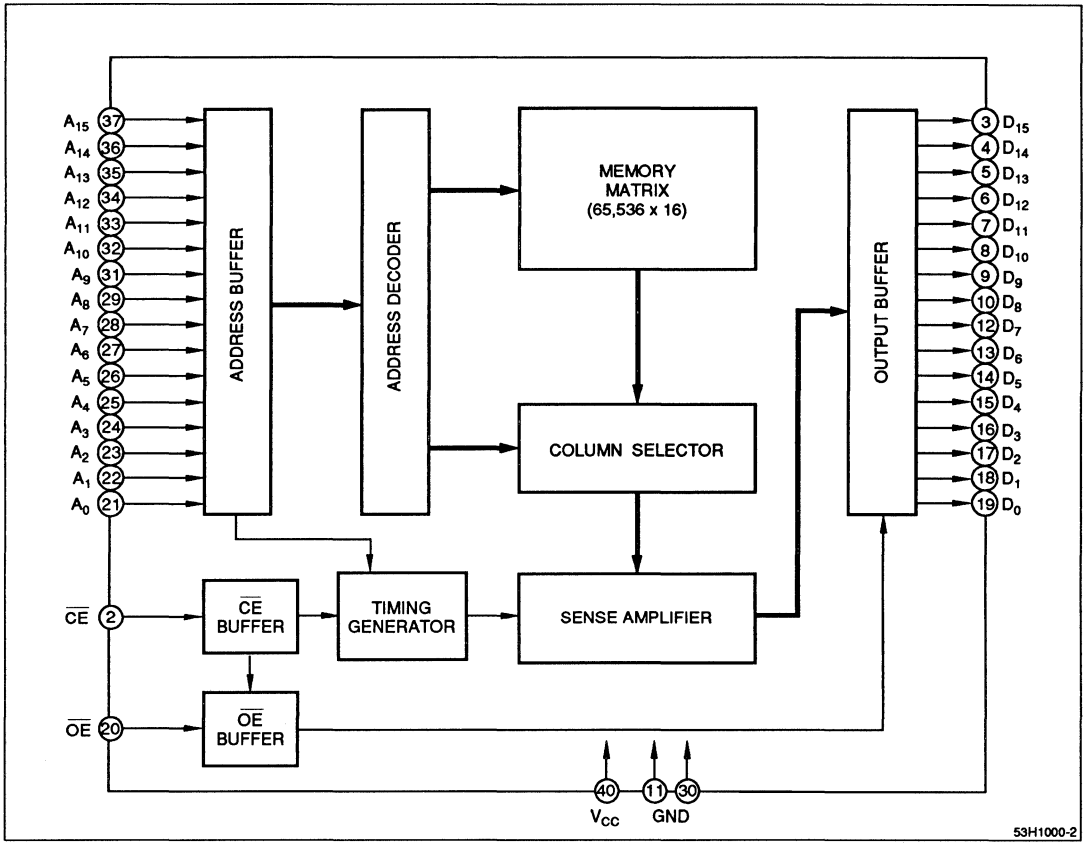


Figure 2. LH53H1000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{15}	Address input
D_0 - D_{15}	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	D_0 - D_{15}	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I_{SB})	1
L	H	Non selected	High-Z	Operating (I_{CC})	
L	L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 3.2 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 55 ns			120	mA	2
	I_{CC2}	t_{RC} = 55 ns			110		3
Standby current	I_{SB}	$\overline{CE}$ = V_{IH}			2	mA	

NOTES:
1. $\overline{CE}$ or $\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	55			ns	
Address access time	t_{AA}			55	ns	
Chip enable time	t_{ACE}			55	ns	
Output enable delay time	t_{OE}			25	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			25	ns	1
OE to output in High-Z	t_{OHZ}			25	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3.0 V
Input rise/fall time	5 ns
Input reference level	1.5 V
Output load condition	1TTL + 30 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

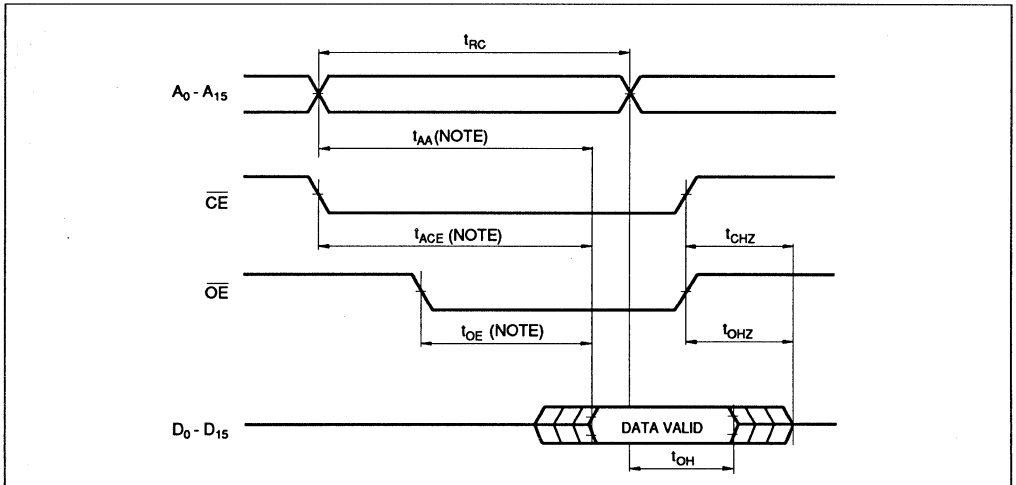
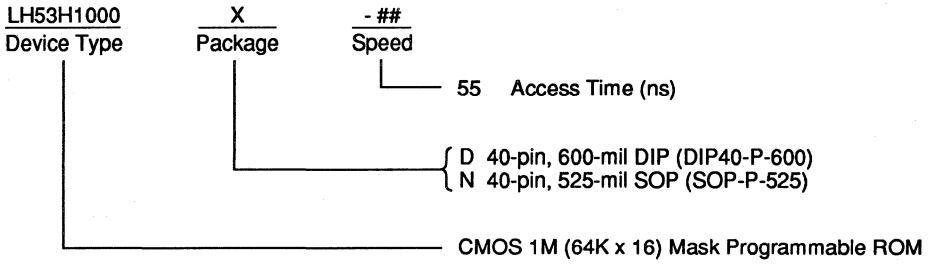


Figure 3. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the Vcc pin and GND.

ORDERING INFORMATION



Example: LH53H1000D-55 (CMOS 1M (64K x 16) Mask Programmable ROM, 55 ns, 40-pin, 600-mil DIP)

53H1000-4

LH53H1100

PRELIMINARY

CMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 35 ns (MAX.)
- Power consumption:
  Operating: 660 mW (MAX.)
  Standby: 440 mW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53H1100 is a high speed mask programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

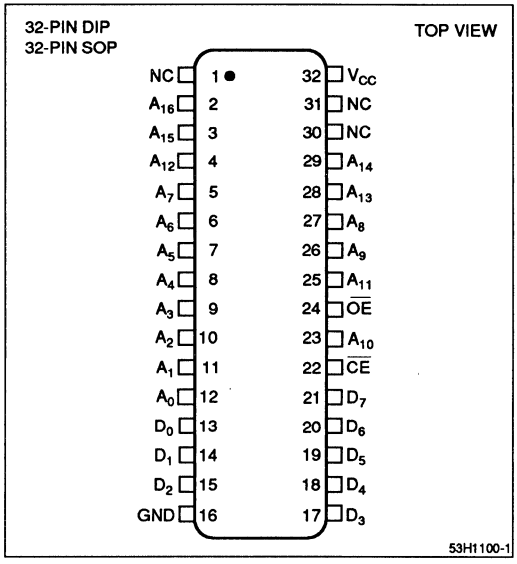


Figure 1. Pin Connections for DIP and SOP Packages

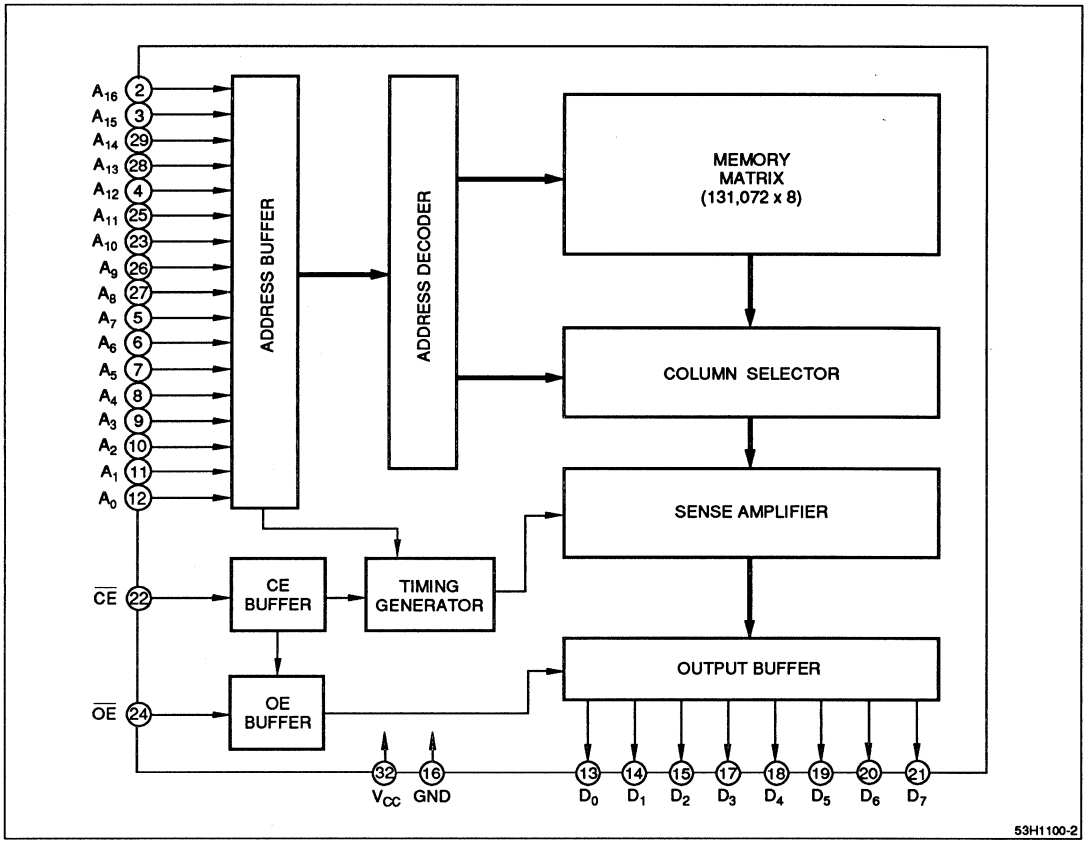


Figure 2. LH53H1100 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
D_0 - D_7	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I_{SB})	1
L	H	Non selected	High-Z	Operating (I_{CC})	
L	L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 3.2 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 35 ns			120	mA	2
	I_{CC2}	t_{RC} = 35 ns			110		3
Standby current	I_{SB}	$\overline{CE}$ = V_{IH}			80	mA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	35			ns	
Address access time	t_{AA}			35	ns	
Chip enable time	t_{ACE}			35	ns	
Output enable time	t_{OE}			15	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			15	ns	1
OE to output in High-Z	t_{OHZ}			15	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3.0 V
Input rise/fall time	5 ns
Input reference level	1.5 V
Output load condition	1TTL + 30 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

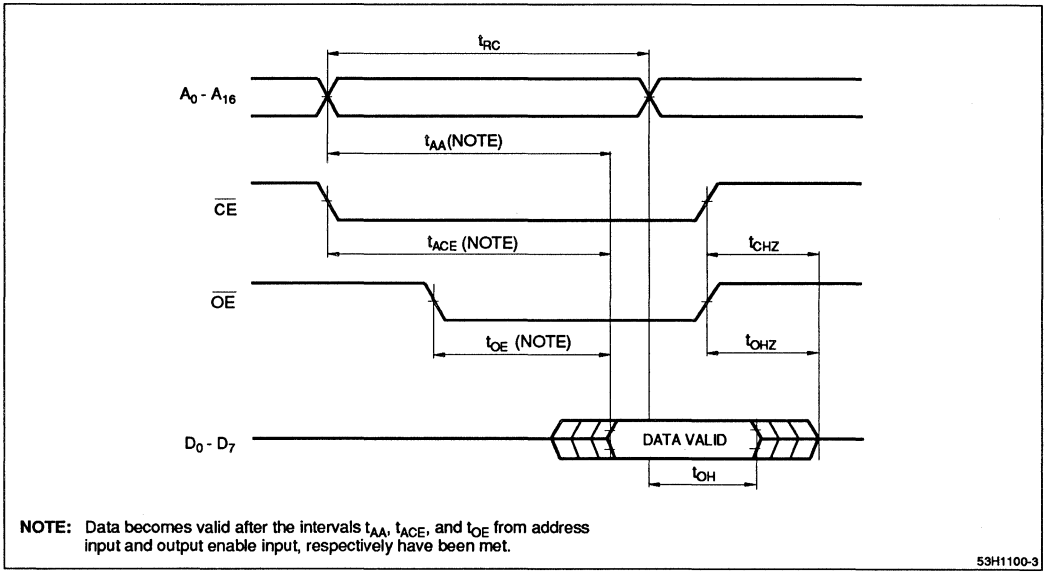
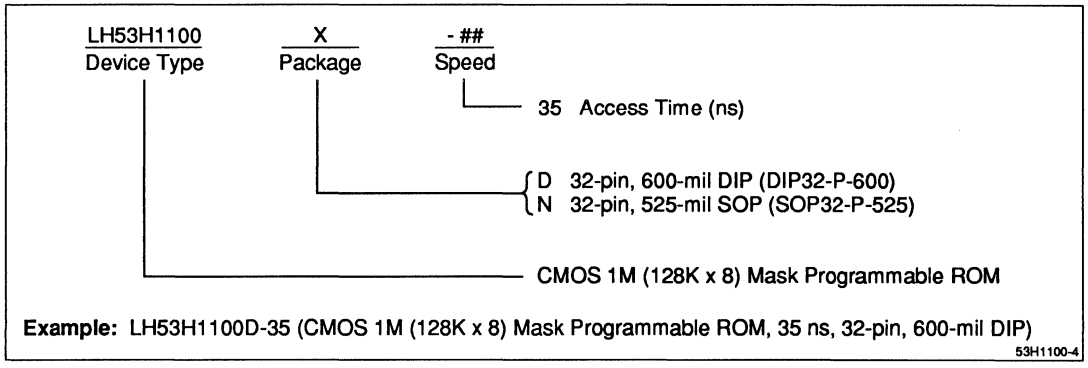


Figure 3. Timing Diagram

CAUTION

To stablize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



Example: LH53H1100D-35 (CMOS 1M (128K x 8) Mask Programmable ROM, 35 ns, 32-pin, 600-mil DIP)

53H1100-4

LH530800A CMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 193 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH530800A is a mask programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

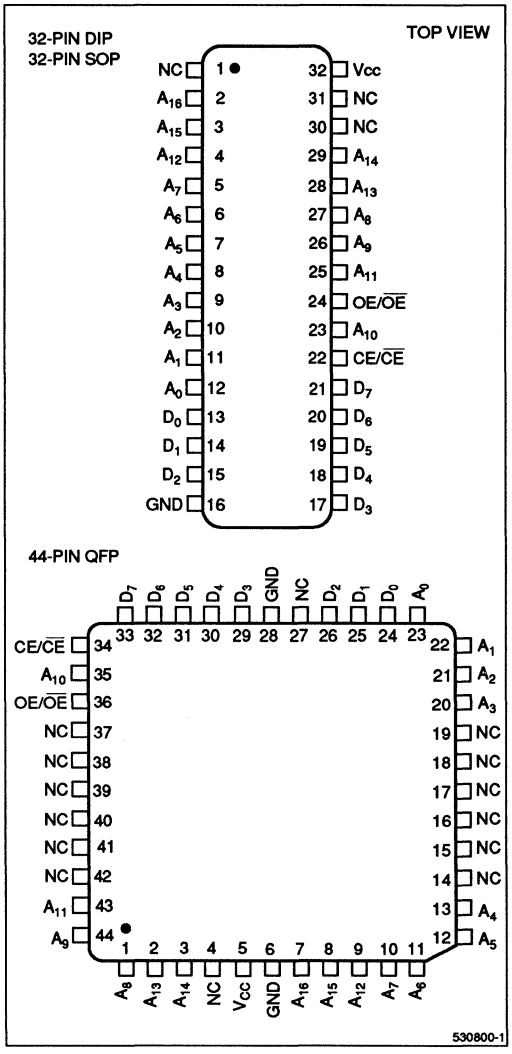


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

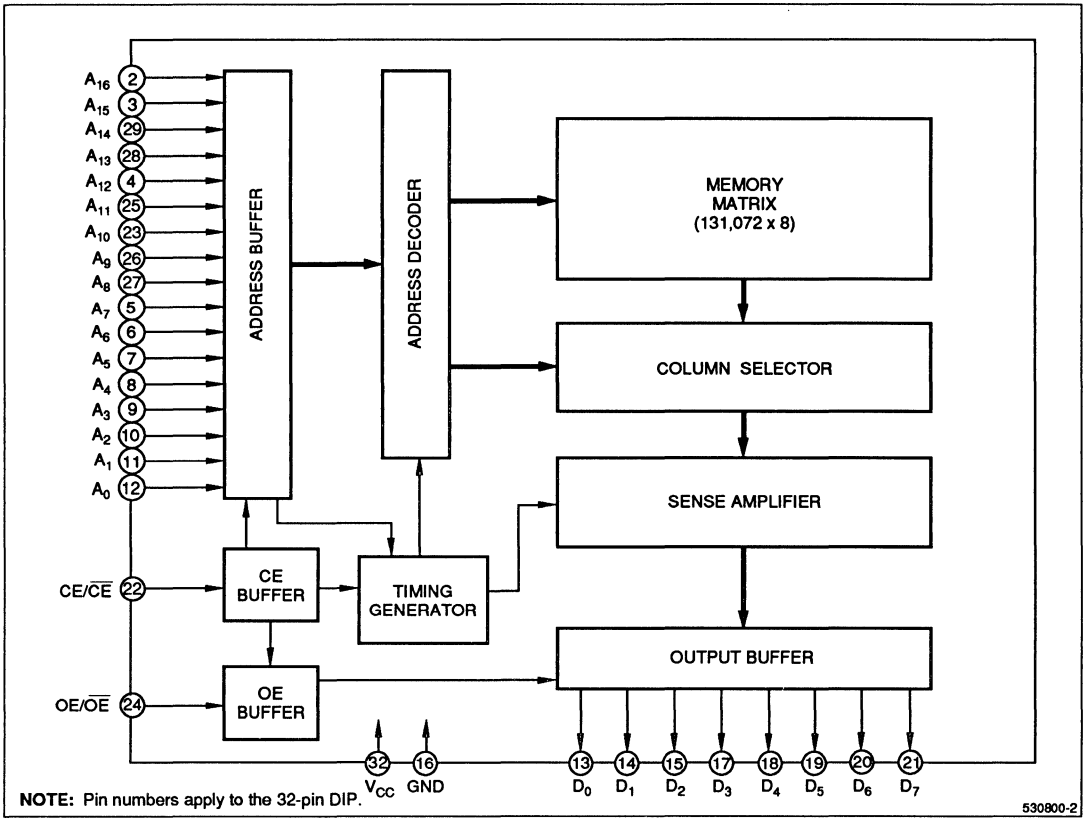


Figure 2. LH530800A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data Output	
CE/$\overline{CE}$	Chip enable input	1

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active levels of CE/$\overline{CE}$ and OE/$\overline{OE}$ are mask programmable.

TRUTH TABLE

CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
L/H	X	Non selected	High-Z	Standby (I_{SB})	1
H/L	L/H	Non selected	High-Z	Operating (I_{CC})	
H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$CE = V_{IL}$, $\overline{CE} = V_{IH}$			2	mA	
	I_{SB2}	$\overline{CE} = V_{CC}$ - 0.2 V, CE = 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE} = V_{IH}$ or $CE/OE = V_{IL}$
2. $V_{IN} = V_{IH}/V_{IL}$, $\overline{CE} = V_{IL}$, $CE = V_{IH}$, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, $CE = V_{CC}$ - 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

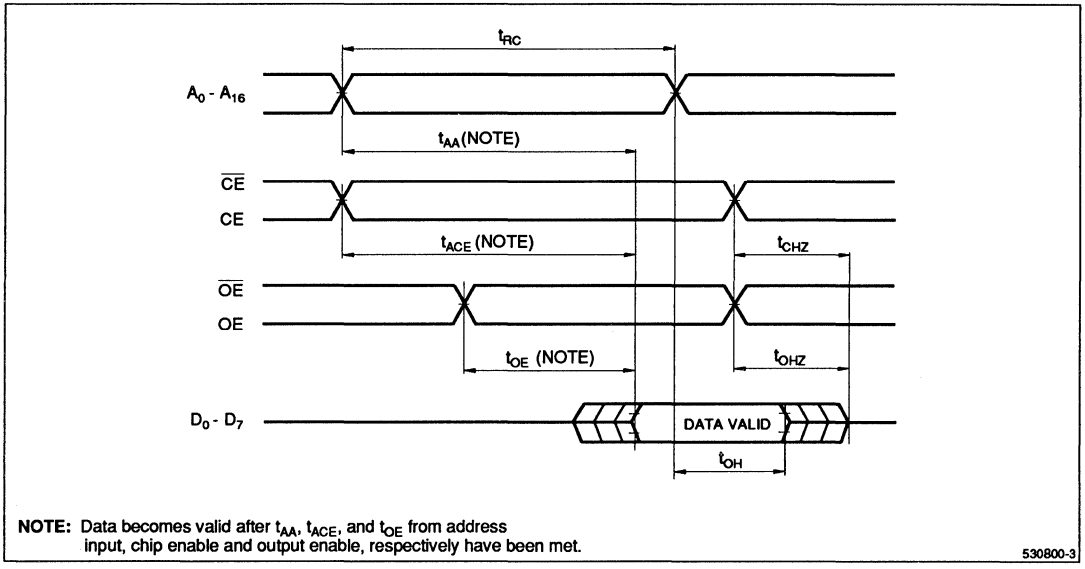


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

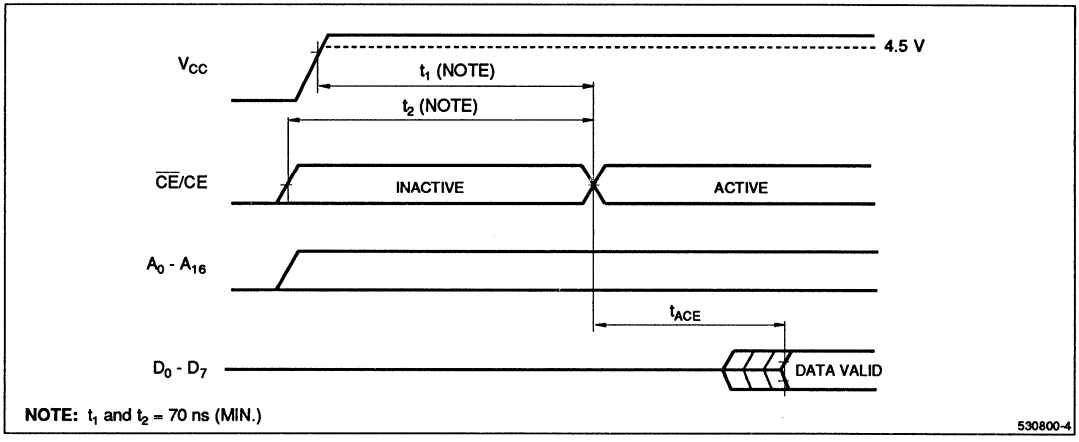


Figure 4. Power On With $\overline{CE}$ Inactive

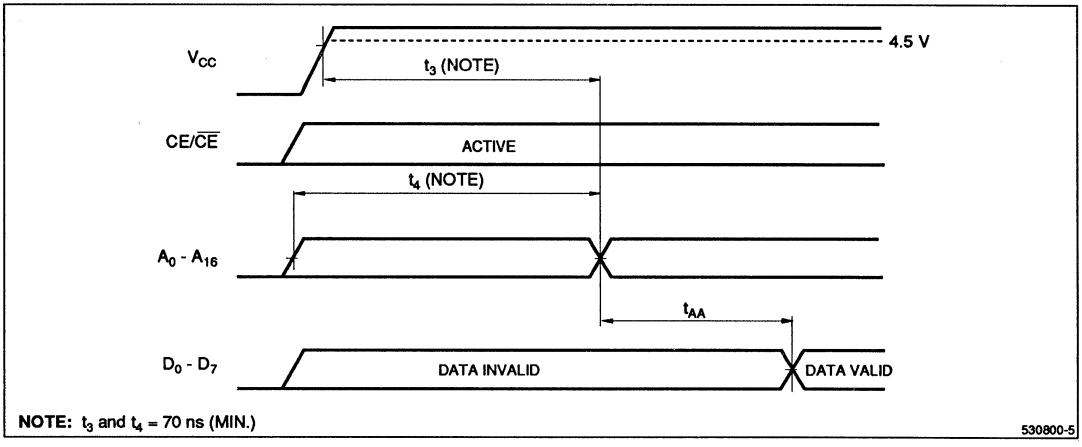
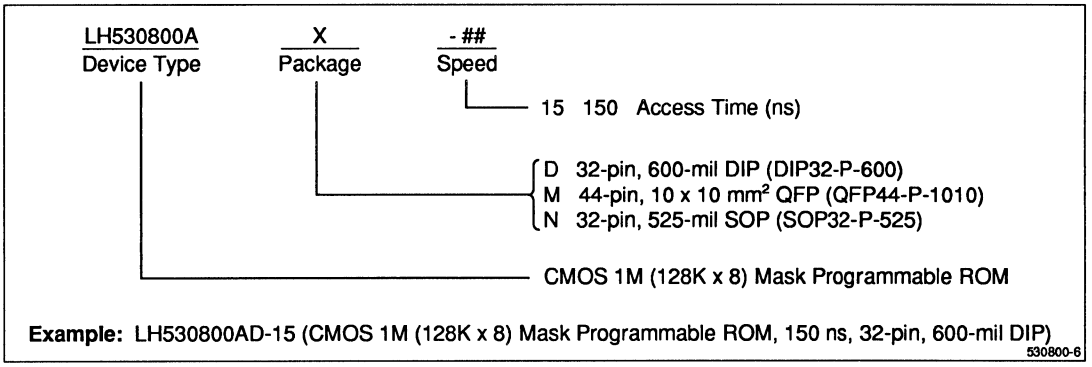


Figure 5. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



Example: LH530800AD-15 (CMOS 1M (128K x 8) Mask Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

530800-6

LH530900A CMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 193 mW (MAX.)
- Programmable $OE_1/\overline{OE}_1$/DC and $OE_2/\overline{OE}_2$/DC
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- 32-pin, 600-mil DIP
  (32-pin compatible to 28-pin 1M mask ROM-specific pinout)

DESCRIPTION

The LH530900A is a mask programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

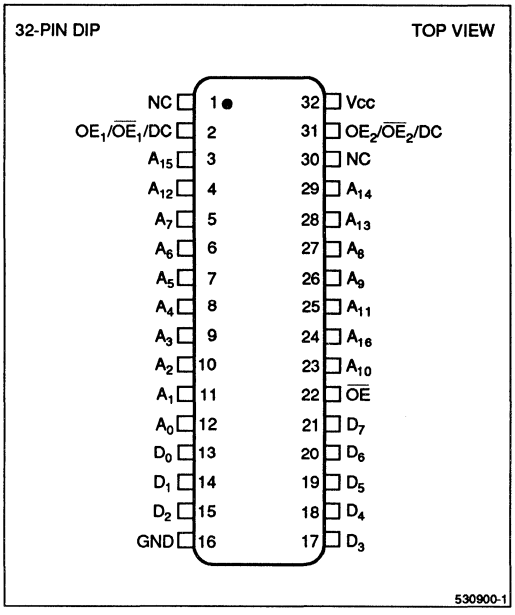


Figure 1. Pin Connections for DIP Package

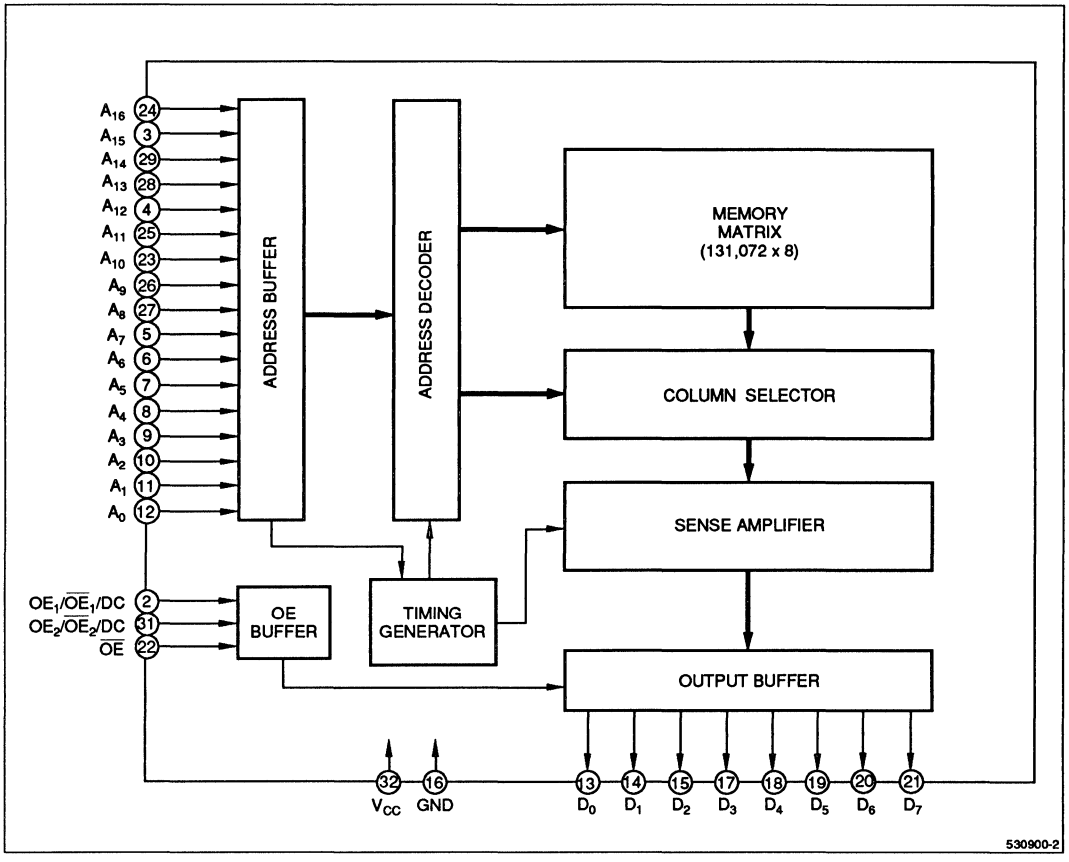


Figure 2. LH530900A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
$\overline{OE}$	Output Enable input	
$OE_1/\overline{OE_1}$/DC	Output Enable input/Don't Care	1

SIGNAL	PIN NAME	NOTE
$OE_2/\overline{OE_2}$/DC	Output Enable input/Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active level of output enable is mask programmable.
   Selecting DC allows the outputs to be active for both high and low levels applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{OE}$	$OE_1/\overline{OE_1}$	$OE_2/\overline{OE_2}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Operating (I_{CC})	1
X	L/H	X	Non selected	High-Z	Operating (I_{CC})	
X	X	L/H	Non selected	High-Z	Operating (I_{CC})	
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		

NOTES:
1. $\overline{OE}/\overline{OE_1}/\overline{OE_2}$ = V_{IH} or OE_1/OE_2 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
OE to output in High-Z	t_{OHZ}			70	ns	1

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

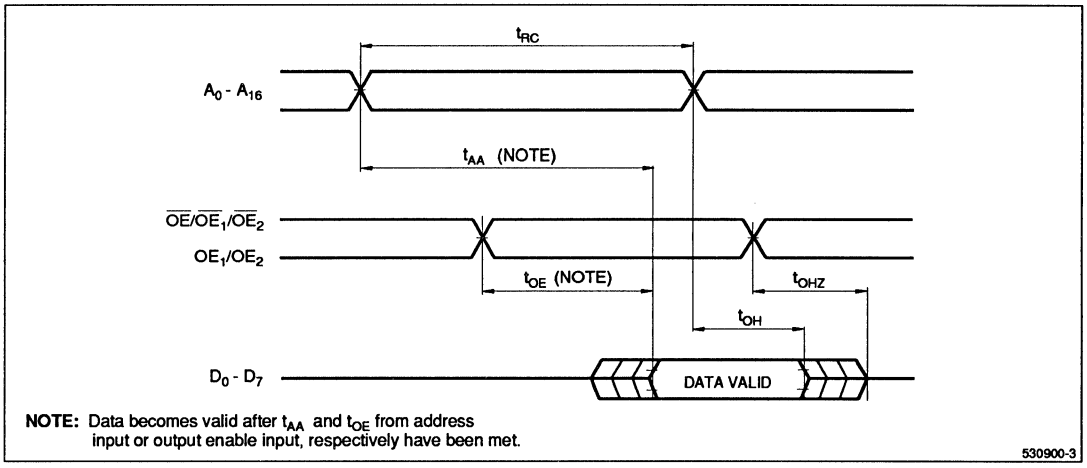


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, change one or more addresses after power up.

The valid data will be output at t_{AA} following a transition from the above operation.

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

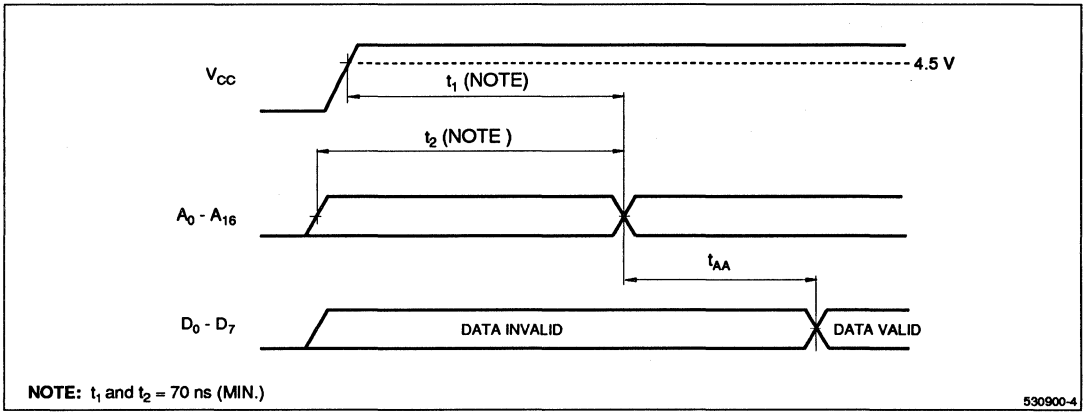
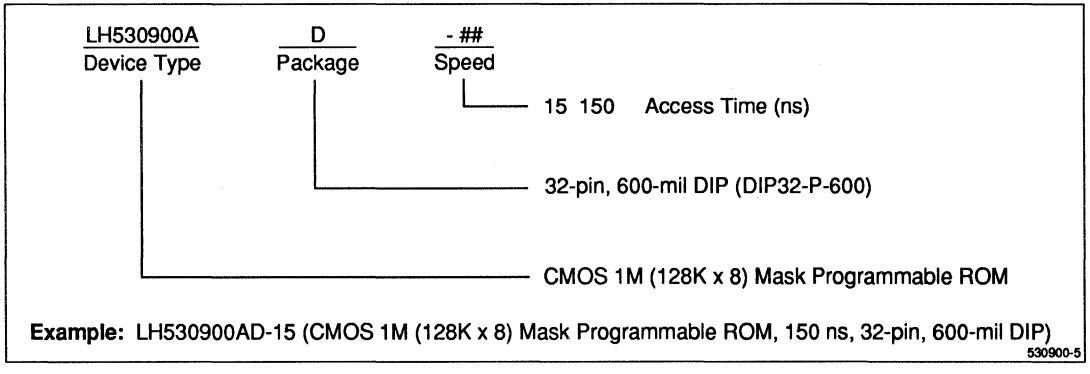


Figure 4. Power On Initialization

ORDERING INFORMATION



LH531000B CMOS 1M (128K × 8) Mask Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 192.5 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable CE/$\overline{CE}$ or OE/$\overline{OE}$
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 14 × 14 mm^2 QFP
- Mask ROM specific pinout

DESCRIPTION

The LH531000B is a mask programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

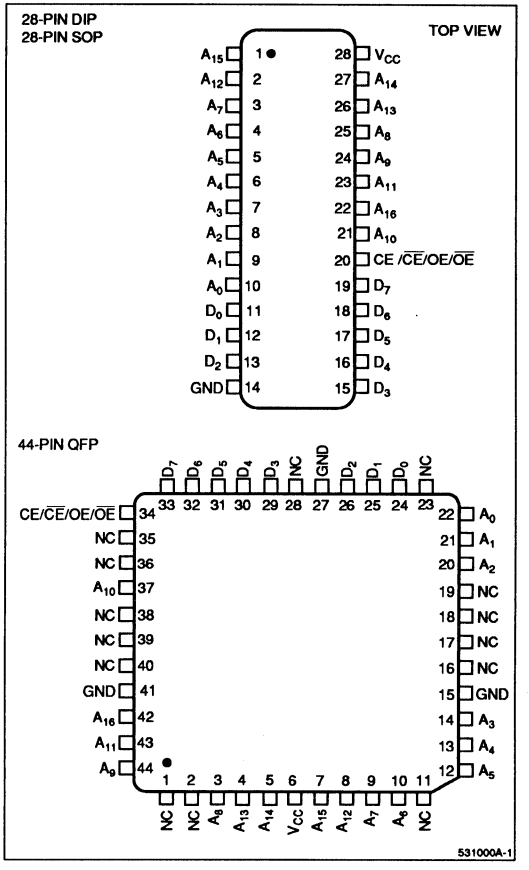


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

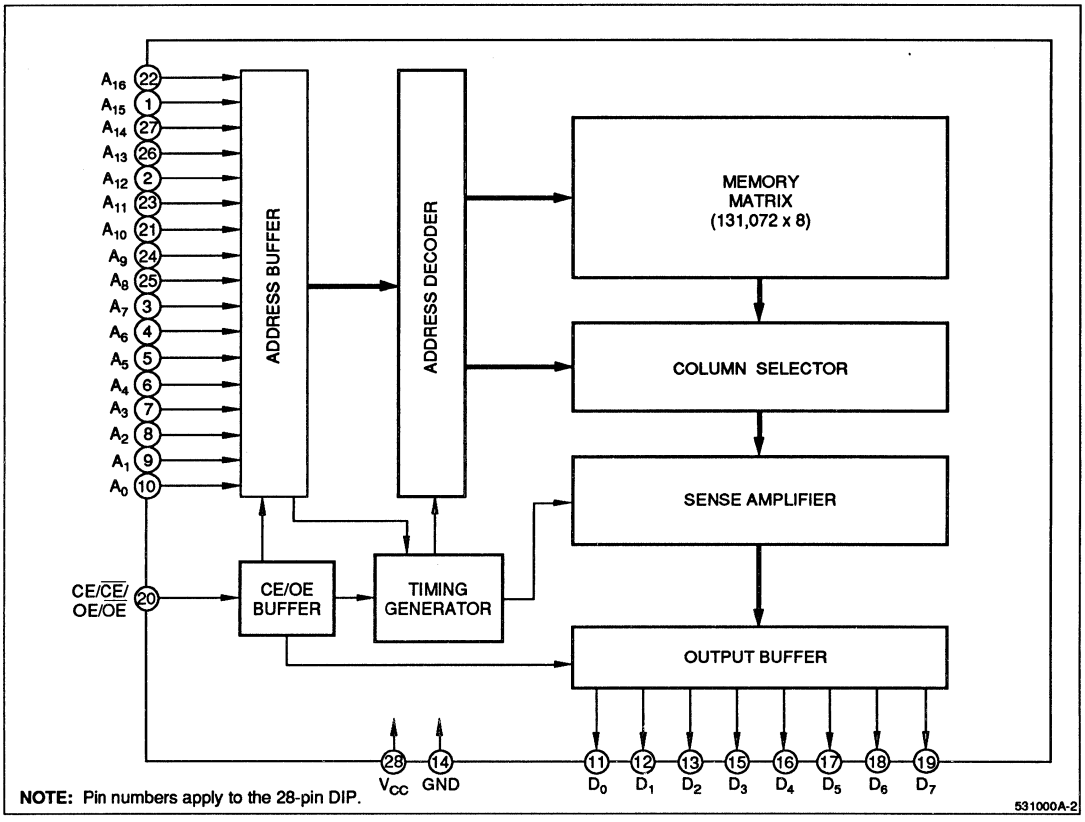


Figure 2. LH531000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
CE/$\overline{CE}$/OE/$\overline{OE}$	Chip Enable input or Output Enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of CE/$\overline{CE}$ or OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

PIN 20 (DIP/SOP) or PIN 34 (QFP)	CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
CE type	H/L	—	Selected	D_{OUT}	Operating (I_{CC})
	L/H	—	Non selected	High-Z	Standby (I_{SB})
OE type	—	H/L	Selected	D_{OUT}	Operating (I_{CC})
	—	L/H	Non selected	High-Z	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}, CE = V_{IL}			2	mA	4
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V, CE = 0.2 V			100	µA	

NOTES:
1. CE/$\overline{OE}$ = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, CE = V_{IH}, $\overline{CE}$ = V_{IL} (CE type), outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V. CE = V_{CC} - 0.2 V, $\overline{CE}$ = 0.2 V (CE type), outputs open
4. CE type only

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}	CE type			150	ns	
Output enable time	t_{OE}	OE type	10		80	ns	
Output hold time	t_{OH}		5			ns	
CE to output in High-Z	t_{CHZ}	CE type			70	ns	1
OE to output in High-Z	t_{OHZ}	OE type			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

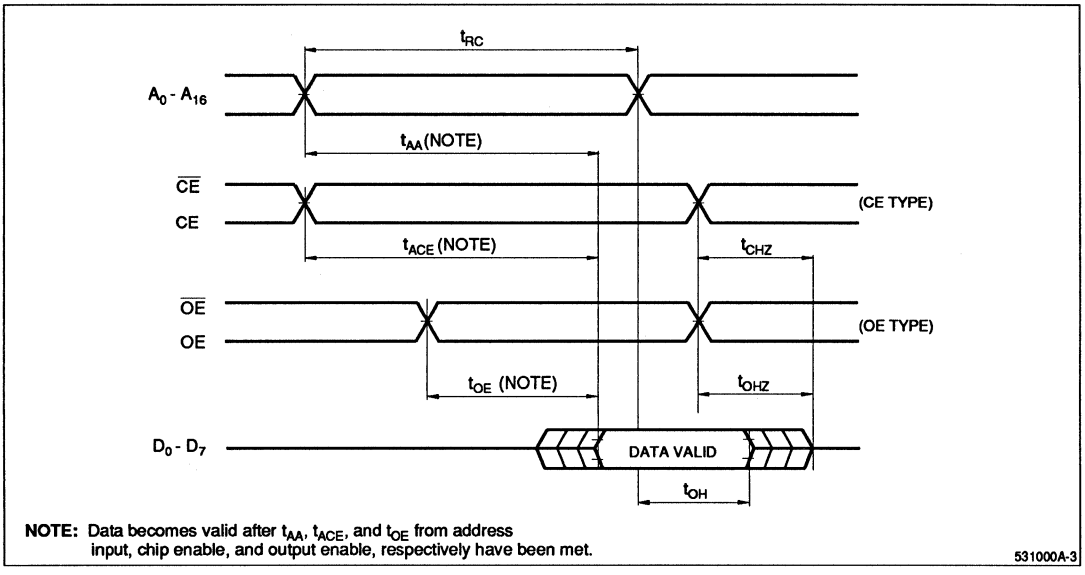


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

$\overline{CE}$ or CE Type

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

$\overline{OE}$ or OE Type

1. Change one or more addresses at power up.

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

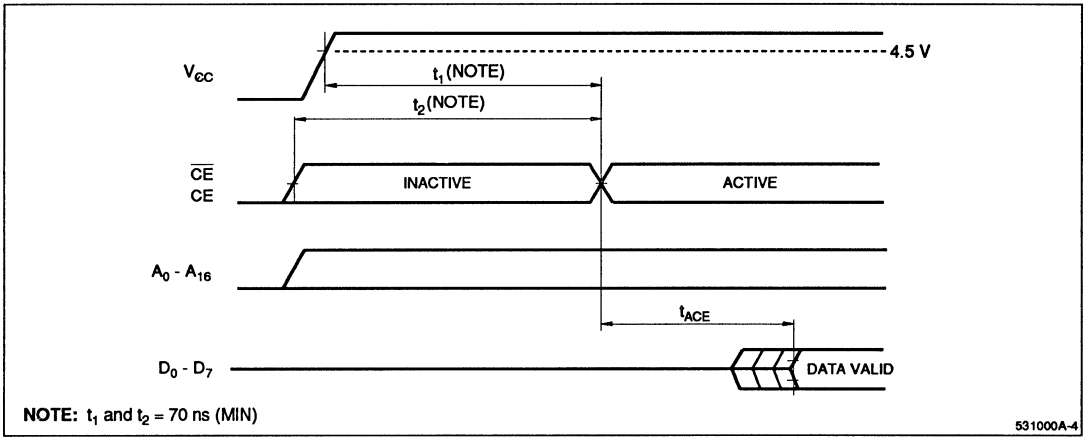


Figure 4. Power On With CE/$\overline{CE}$ Inactive ($\overline{CE}$ or CE Type in Operation)

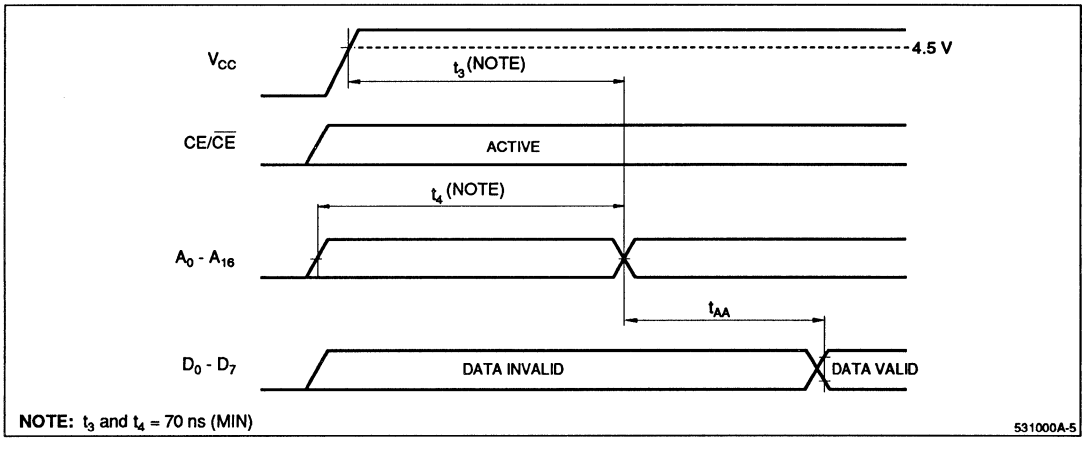


Figure 5. Power On With CE/$\overline{CE}$ Active ($\overline{CE}$ or CE Type in Operation)

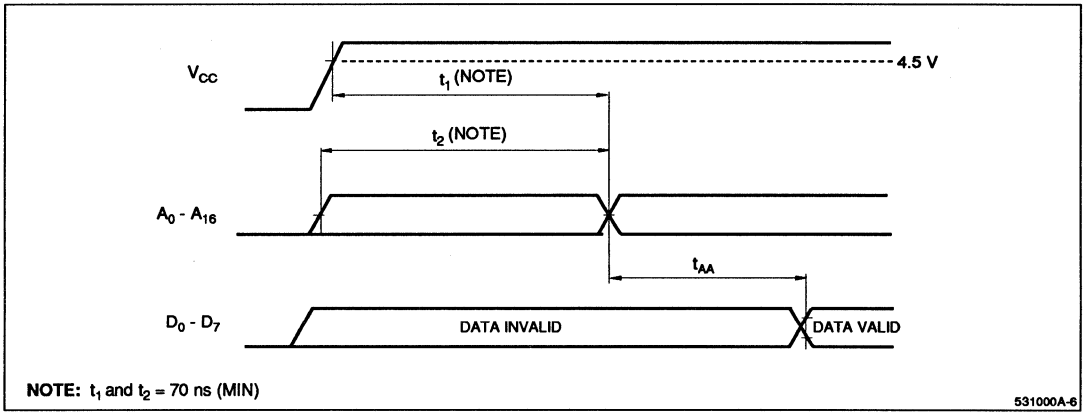
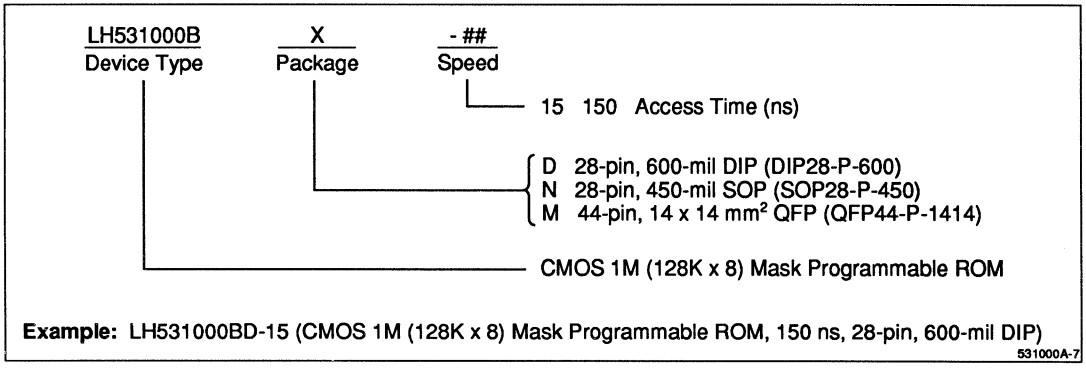


Figure 6. Power On Initialization ($\overline{OE}$ or OE Type In Operation)

ORDERING INFORMATION



LH532000B

CMOS 2M (256K × 8 / 128K × 16) Mask Programmable ROM

FEATURES

- Selectable memory organization:
  262,144 × 8 bit (byte mode)
  131,072 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 120/150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable OE/$\overline{\text{OE}}$ and $\text{OE}_1/\overline{\text{OE}_1}$/DC
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  44-pin, 10 × 10 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH532000B is a 2M bit mask programmable ROM with two programmable memory organizations, byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

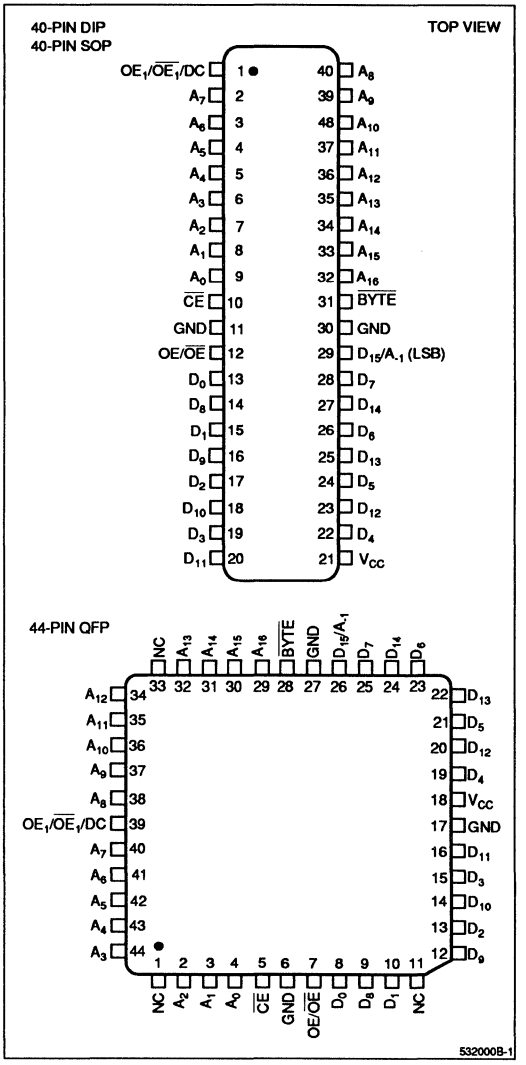


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

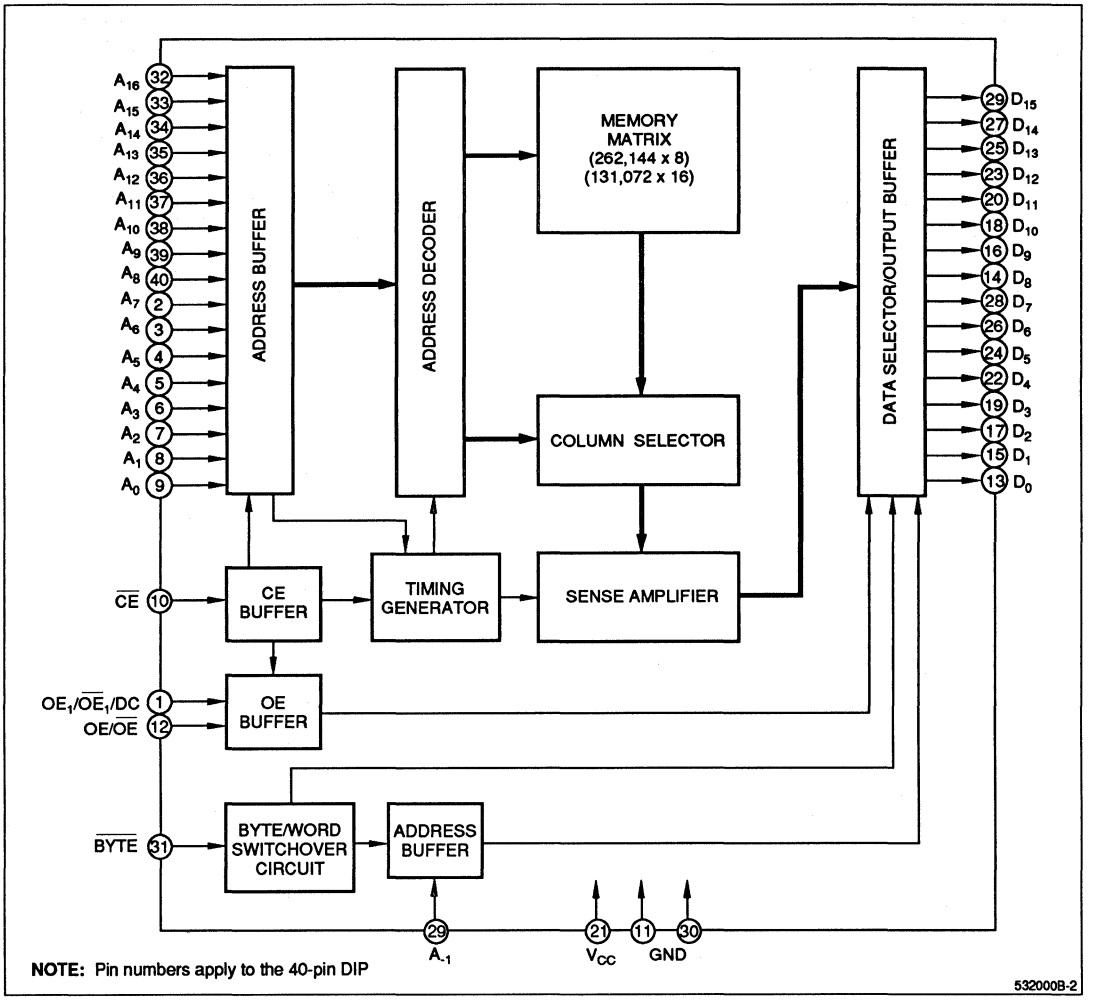


Figure 2. LH532000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{16}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	2

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output enable input or Don't care	2
$\overline{BYTE}$	$\overline{BYTE}$/WORD switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. The active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC are mask programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	X	Non selected	High-Z		Operating (I_{CC})
L	X	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = t_{RC} (MIN.)			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = t_{RC} (MIN.)			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE/OE_1= V_{IL}, $\overline{CE}$/$\overline{OE}$/$\overline{OE_1}$= V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		55	10	70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		55		70	ns	1
OE to output in High-Z	t_{OHZ}		55		70	ns	

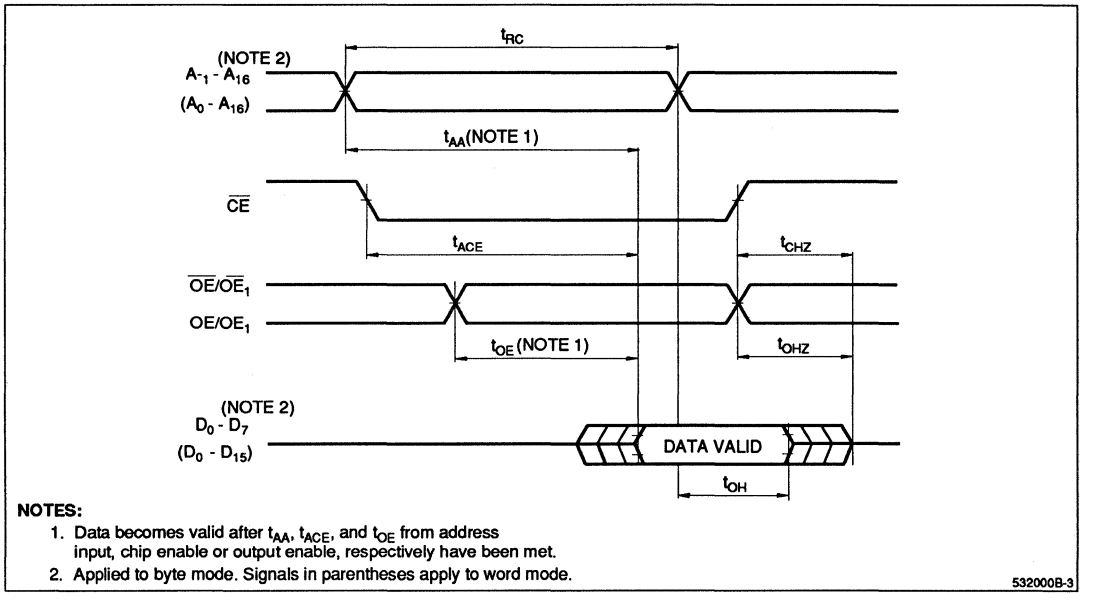
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

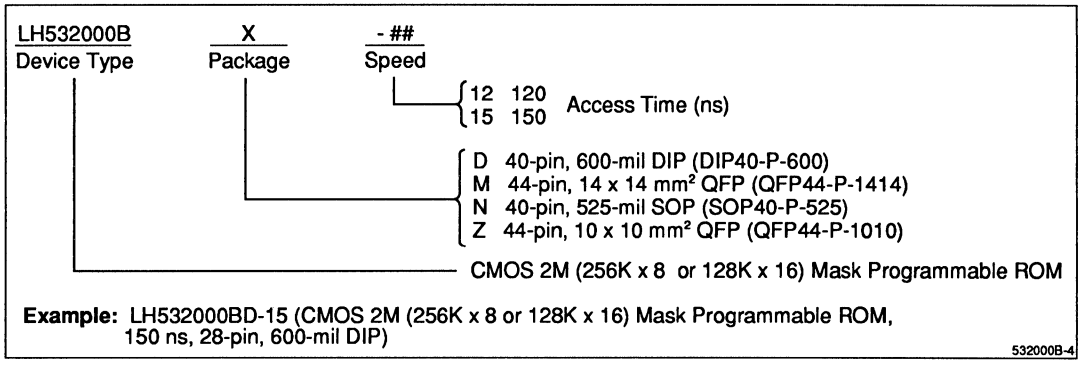


NOTES:
1. Data becomes valid after t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.
2. Applied to byte mode. Signals in parentheses apply to word mode.

532000B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



LH532100B CMOS 2M (256K × 8) Mask Programmable ROM

FEATURES

- 262,144 × 8 bit organization
- Access time: 120/150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- Mask-programmable OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH532100B is a mask programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

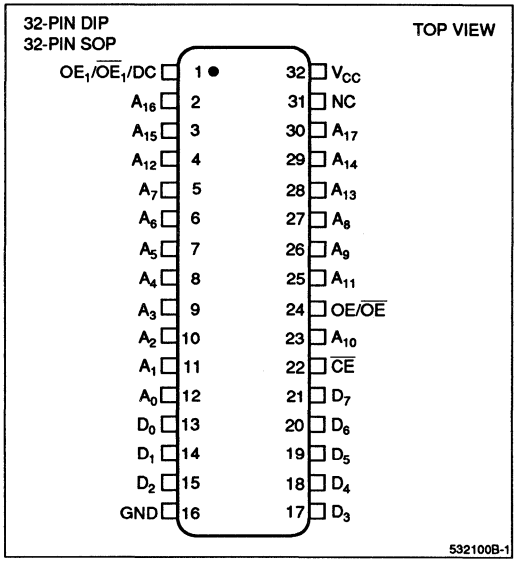


Figure 1. Pin Connections for DIP and SOP Packages

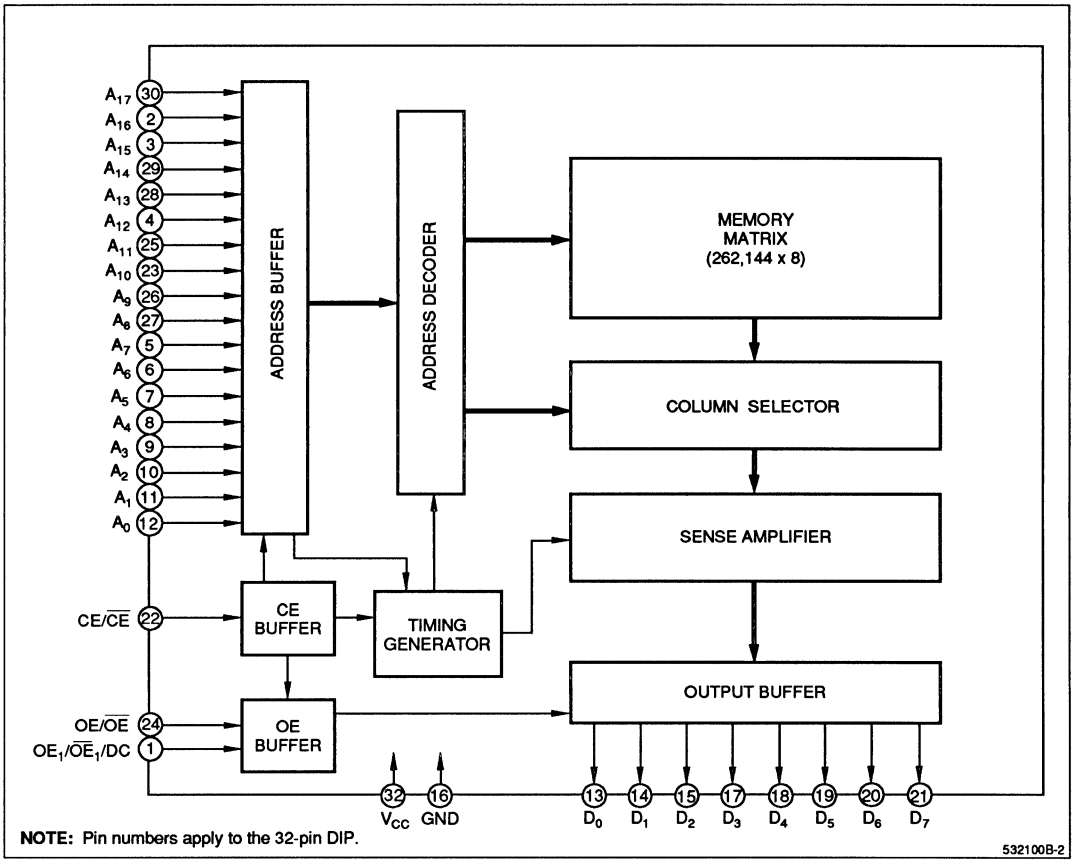


Figure 2. LH532100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{17}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care connection	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC are mask programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:

X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	CE = V_{IL}, $\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	CE = 0.2 V, $\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		50	10	70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		50		70	ns	1
OE to output in High-Z	t_{OHZ}		50		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

CAUTION

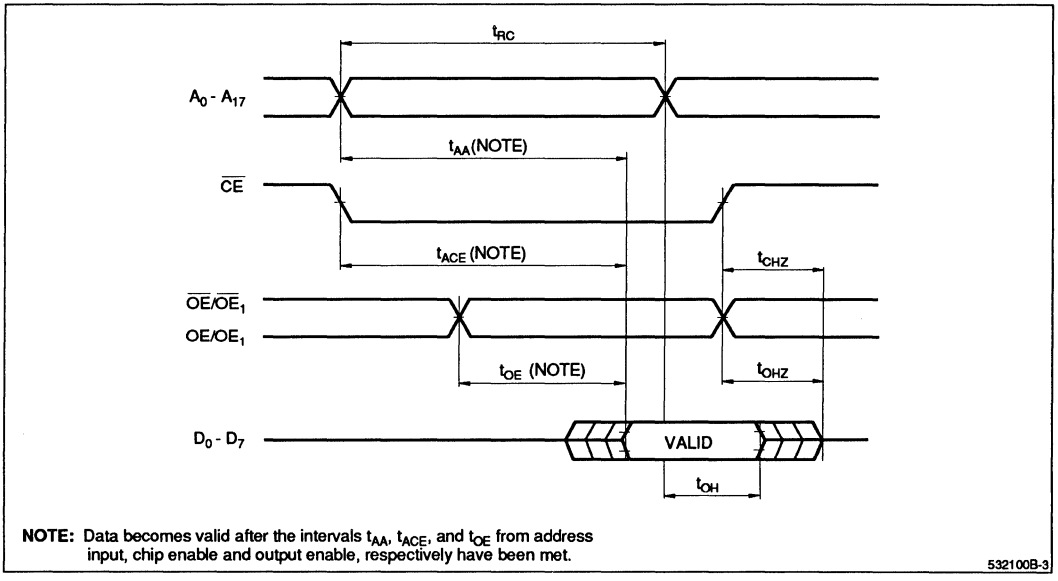
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

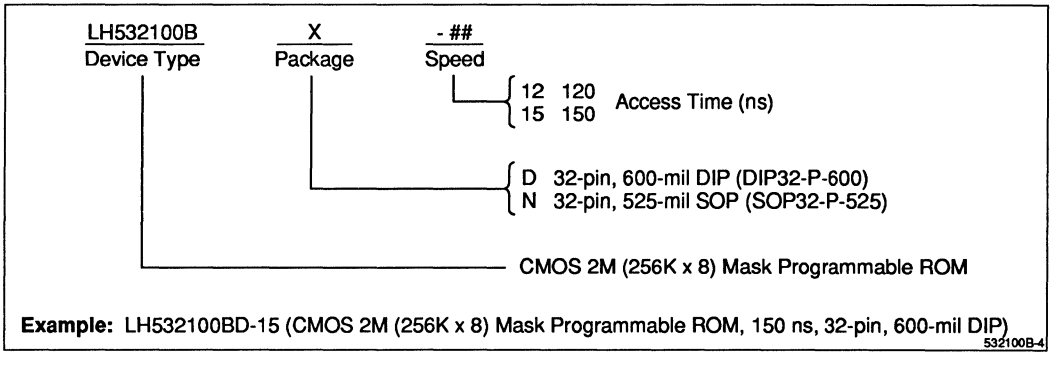


NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable and output enable, respectively have been met.

532100B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH532100BD-15 (CMOS 2M (256K x 8) Mask Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

532100B-4

LH532200B CMOS 2M (256K × 8) Mask Programmable ROM

FEATURES

- 262,144 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
- Static operation (No clock required)
- Mask-programmable $OE_1/\overline{OE}_1/DC$ and $OE_2/\overline{OE}_2/DC$
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- 32-pin, 600-mil DIP
  Compatible to 28-pin 1M-bit mask ROM specific pinout

DESCRIPTION

The LH532200B is a mask programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

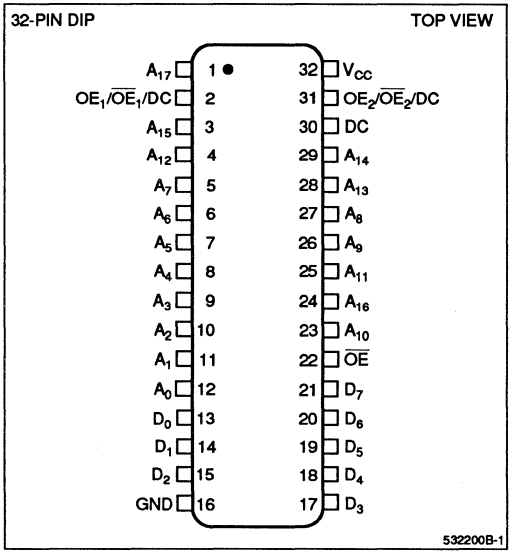


Figure 1. Pin Connections for DIP Package

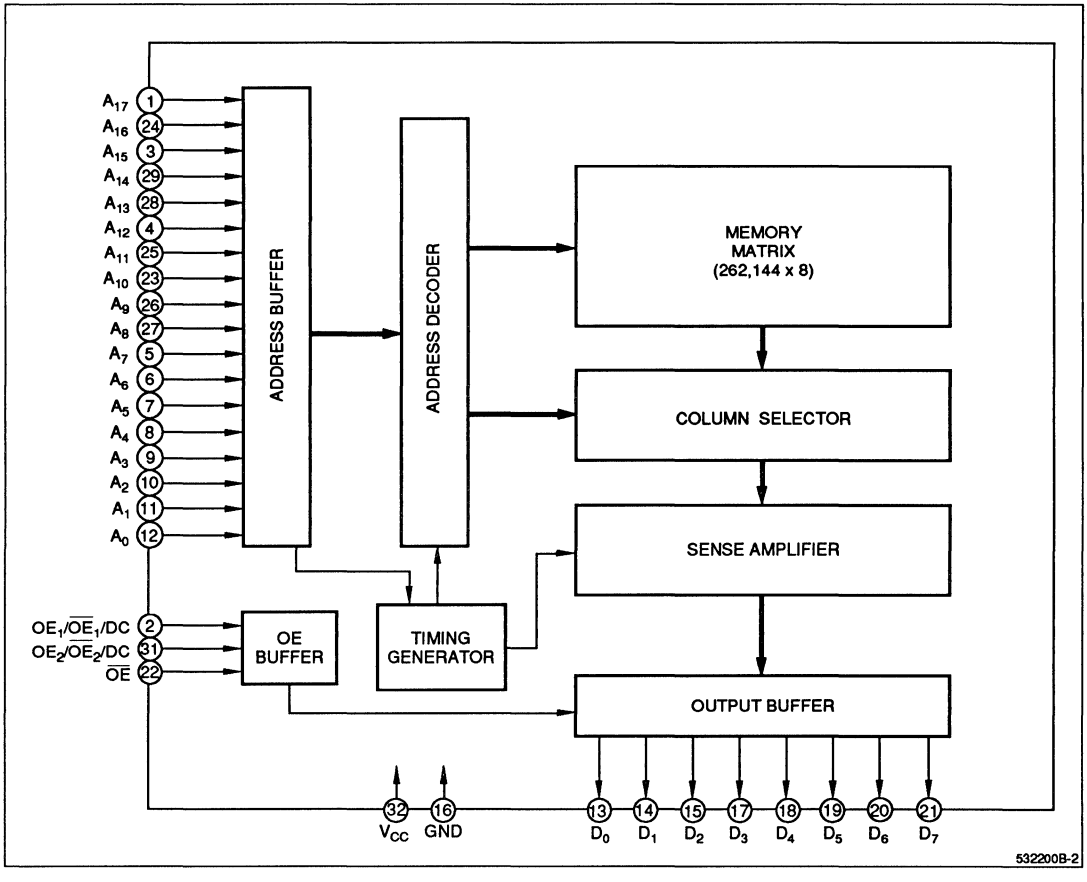


Figure 2. LH532200B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{17}	Address input	
D_0 - D_7	Data output	
$\overline{OE}$	Output Enable input	
$OE_1/\overline{OE}_1/DC$	Output Enable input/ Don't Care	1
$OE_2/\overline{OE}_2/DC$	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of $OE_1/\overline{OE}_1/DC$ and $OE_2/\overline{OE}_2/DC$ are mask programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{OE}$	$OE_1/\overline{OE_1}$	$OE_2/\overline{OE2}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Operating (I_{CC})
X	L/H	X	Non selected	High-Z	Operating (I_{CC})
X	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.0	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		

NOTES:
1. $\overline{OE}/\overline{OE_1}/\overline{OE_2}$ = V_{IH} or OE_1/OE_2 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Output enable delay time	t_{OE}	10		70	ns	
Output hold time	t_{OH}	10			ns	
OE to output in High-Z	t_{OHZ}			70	ns	1

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

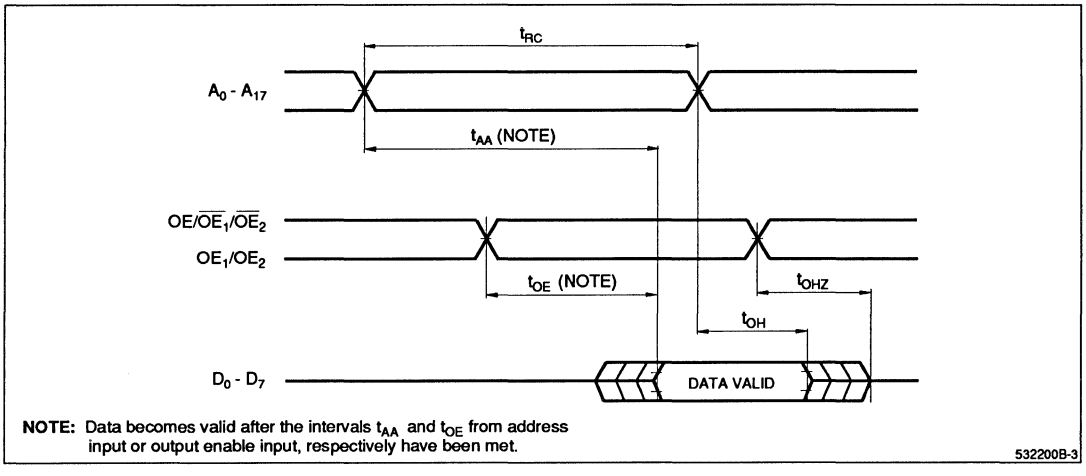
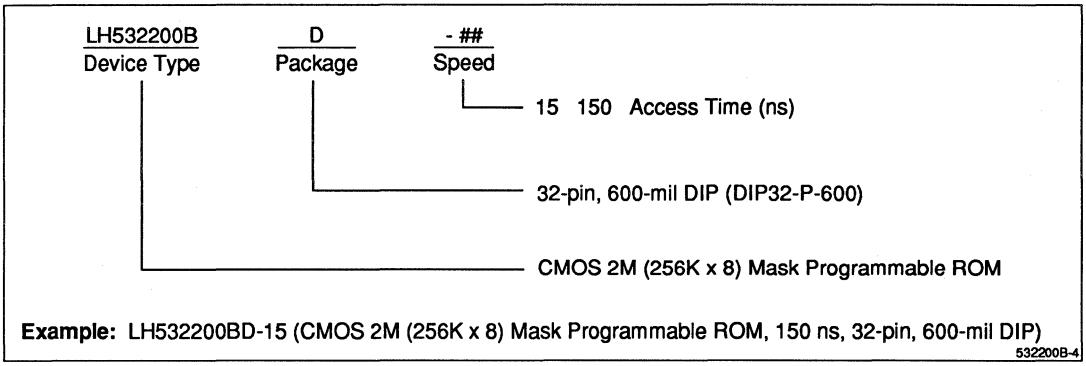


Figure 3. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



Example: LH532200BD-15 (CMOS 2M (256K x 8) Mask Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

532200B-4

LH534000B

CMOS 4M (512K × 8 / 256K × 16)
Mask Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  44-pin, 10 × 10 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534000B is a 4M bit mask programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

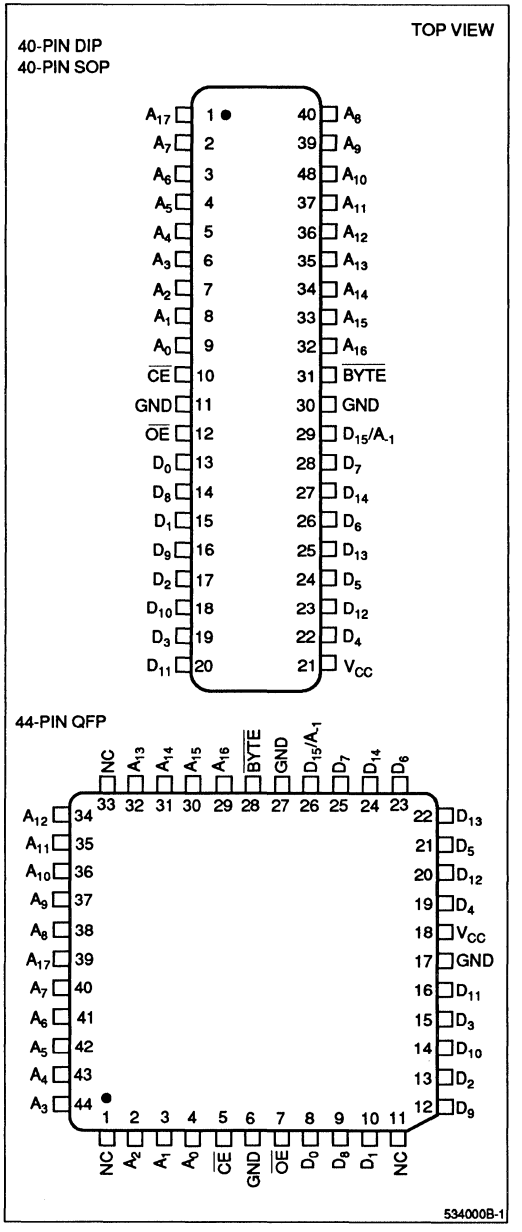


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

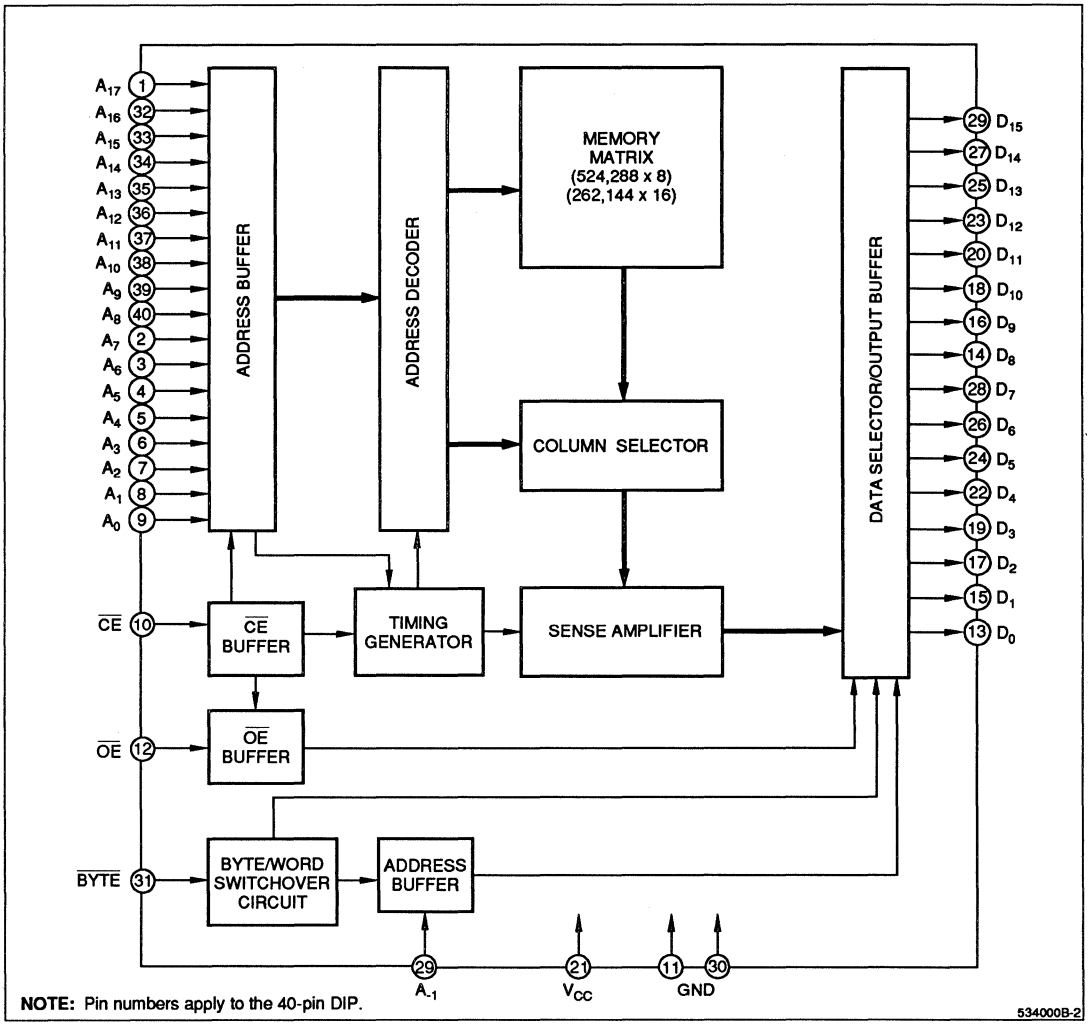


Figure 2. LH534000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Chip enable input	
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTES:
1. X = H or L
2. The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either HIGH or LOW.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable access time	t_{ACE}			200	ns	
Output enable delay time	t_{OE}			80	ns	
Output hold time	t_{OH}	10			ns	
CE to output in High-Z	t_{CHZ}			80	ns	1
OE to output in High-Z	t_{OHZ}			80	ns	

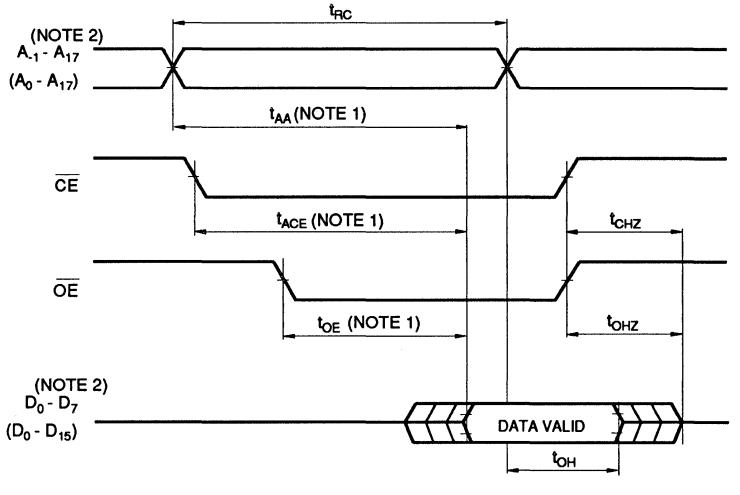
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

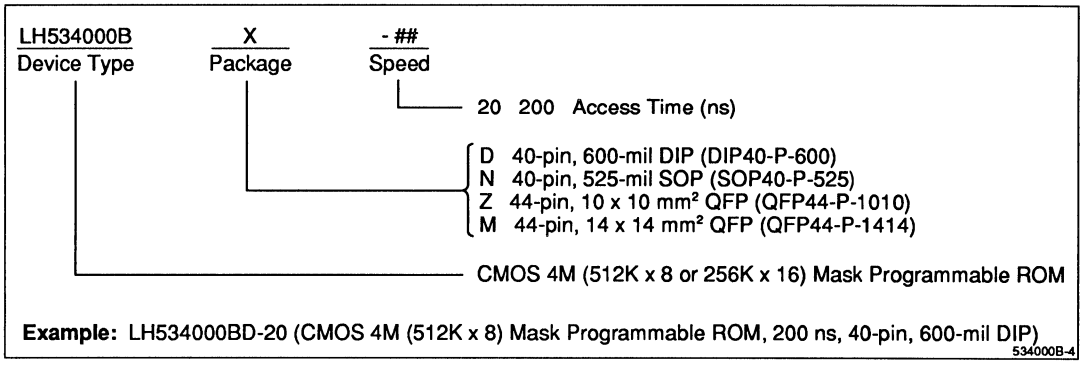


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

534000B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534000BD-20 (CMOS 4M (512K x 8) Mask Programmable ROM, 200 ns, 40-pin, 600-mil DIP)

LH534100B CMOS 4M (512K × 8) Mask Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Mask programmable OE/$\overline{OE}$ and $OE_1/\overline{OE}_1$/DC
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH534100B is a 4M-bit mask programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

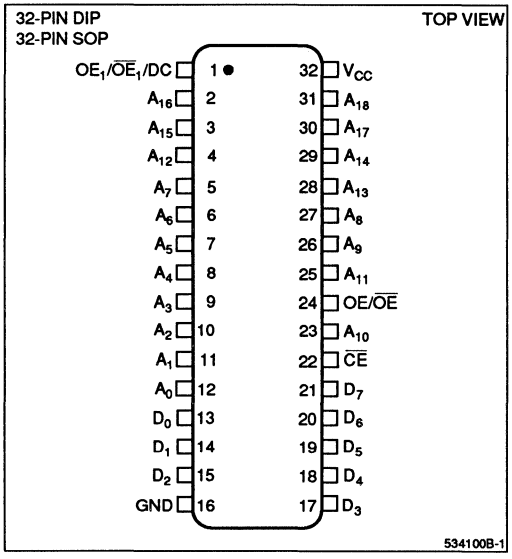


Figure 1. Pin Connections for DIP and SOP Packages

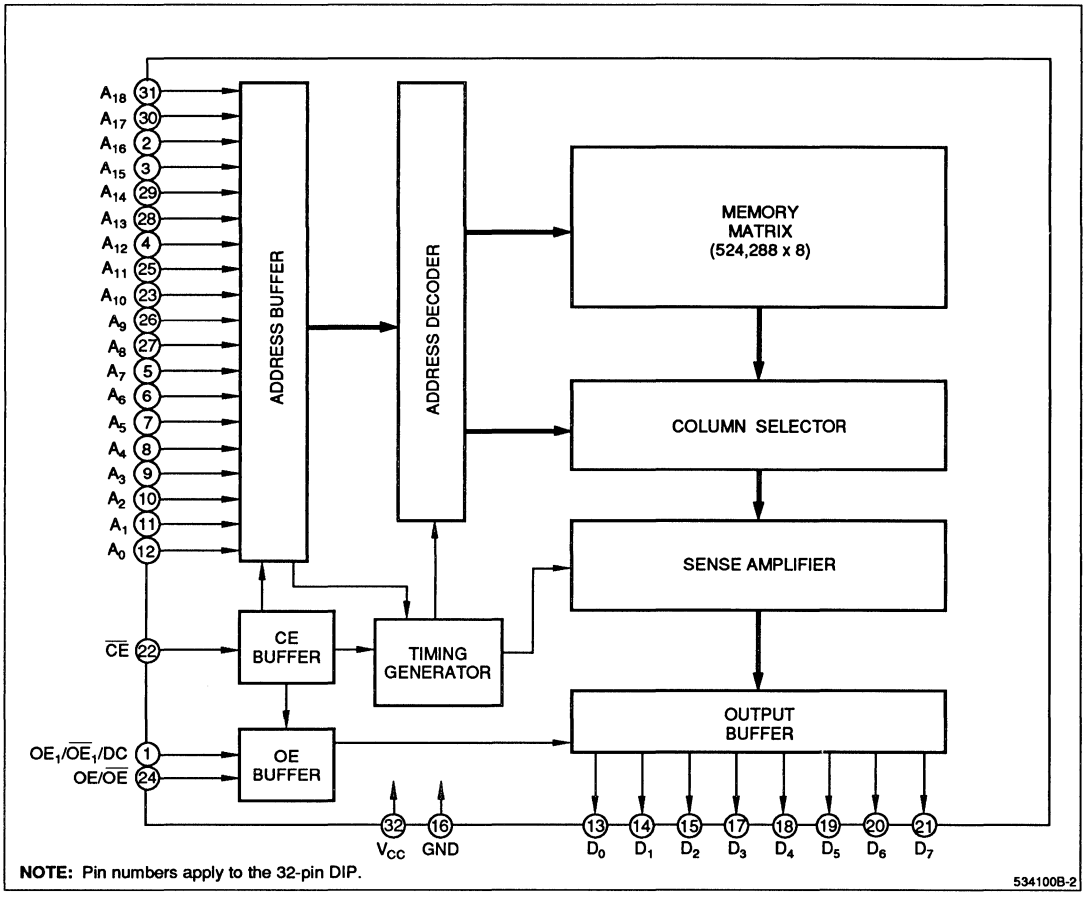


Figure 2. LH534100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of $OE_1/\overline{OE_1}$/DC and OE/$\overline{OE}$ are mask programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/OE/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	10		ns	
CE to output in High-Z	t_{CHZ}		80	ns	1
OE to output in High-Z	t_{OHZ}		80	ns	

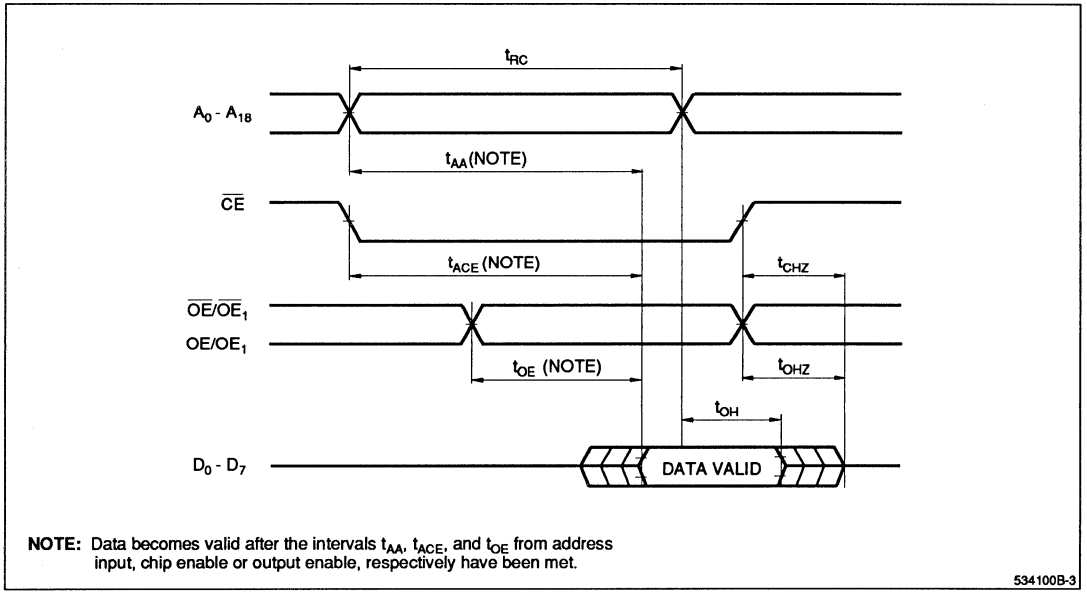
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

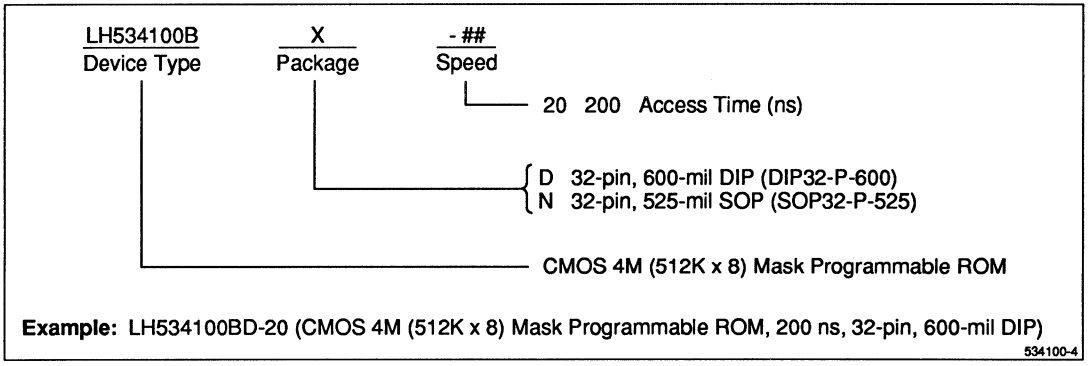


NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.

534100B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534100BD-20 (CMOS 4M (512K x 8) Mask Programmable ROM, 200 ns, 32-pin, 600-mil DIP)

534100-4

LH534200B CMOS 4M (512K × 8) Mask Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
- Mask-programmable $OE_1/\overline{OE}_1/DC$
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  Compatible with 28-pin 1M mask ROM-specific pinout

DESCRIPTION

The LH534200B is a mask programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

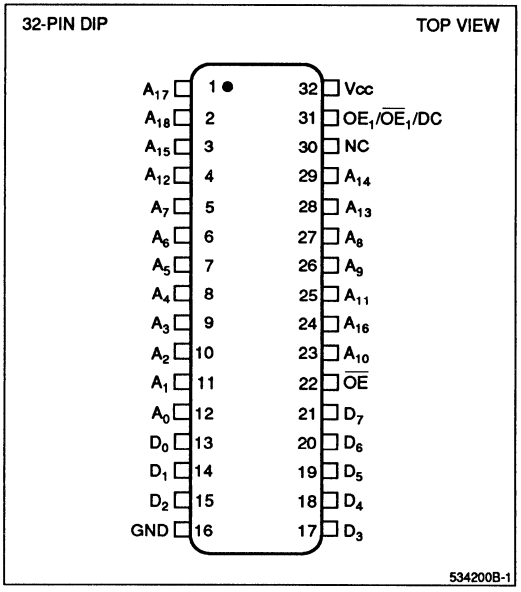


Figure 1. Pin Connections for DIP Package

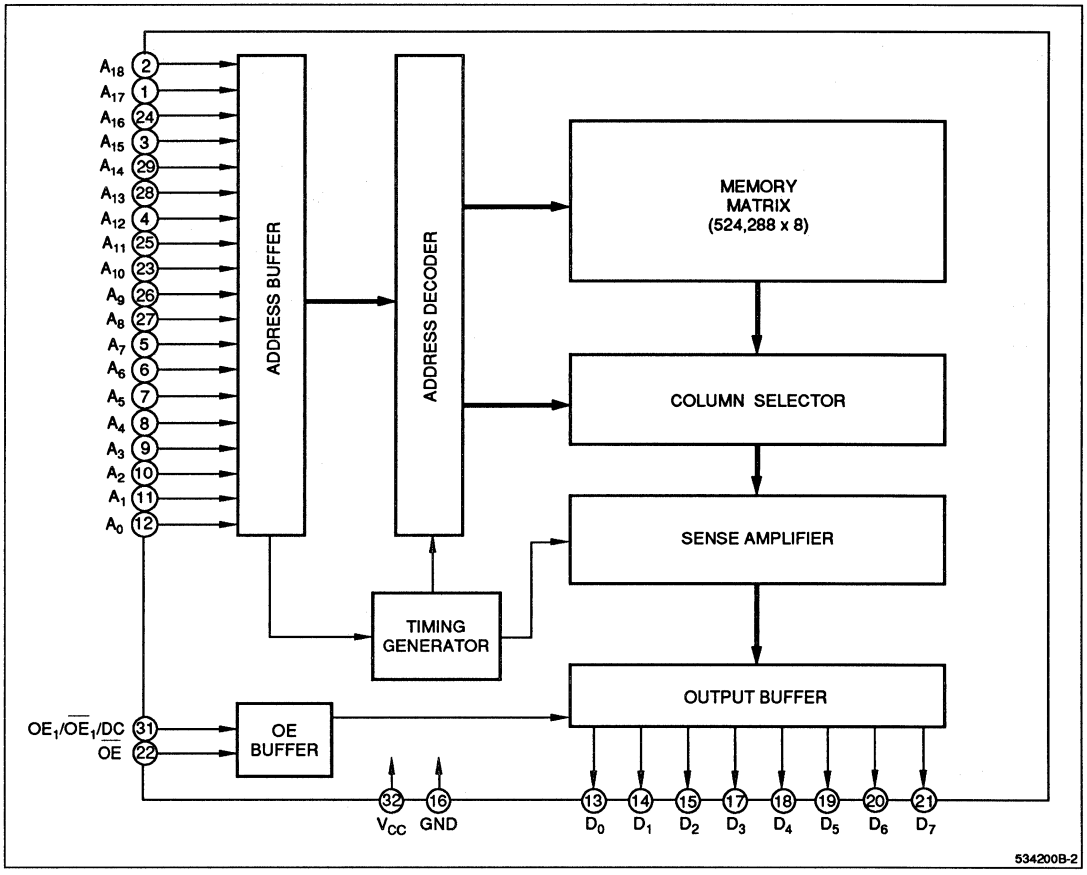


Figure 2. LH534200B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE}_1/DC$	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. The active level of $OE_1/\overline{OE}_1/DC$ is mask programmable.
   Selecting DC allows the outputs to be active for both high and low levels that are applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

TRUTH TABLE

$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	Non selected	High-Z	Operating (I_{CC})
X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		

NOTES:
1. $\overline{OE}/\overline{OE_1}$ = V_{IH} or OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	10		ns	
OE to output in High-Z	t_{OHZ}		80	ns	1

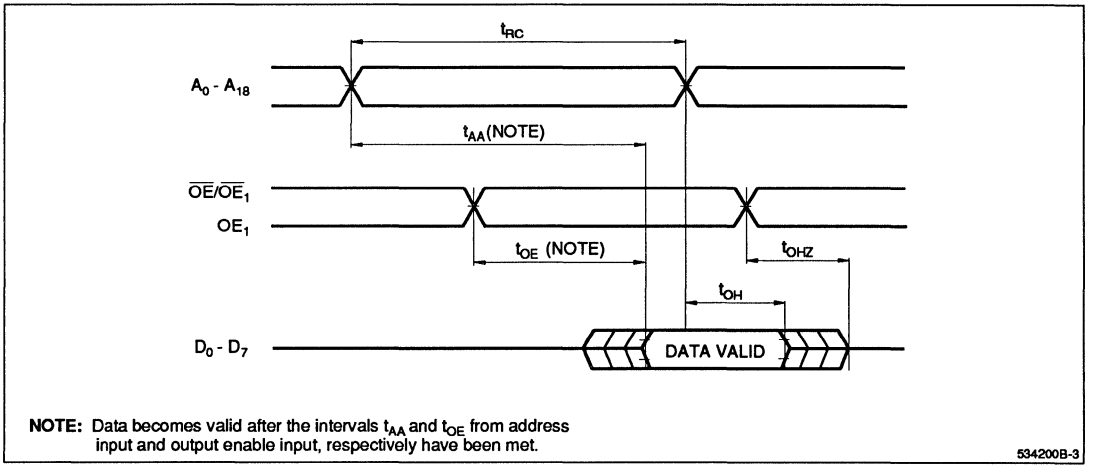
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

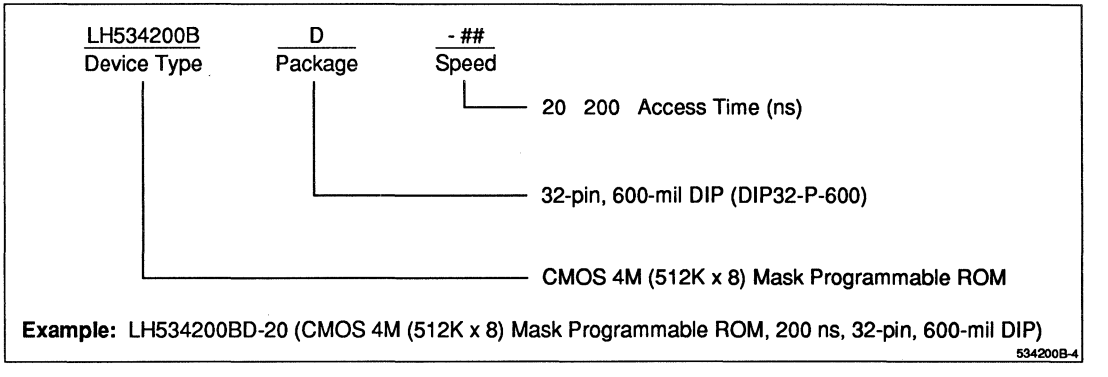


NOTE: Data becomes valid after the intervals t_{AA} and t_{OE} from address input and output enable input, respectively have been met.

534200B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534200BD-20 (CMOS 4M (512K x 8) Mask Programmable ROM, 200 ns, 32-pin, 600-mil DIP)

534200B-4

LH534300A CMOS 4M (512K × 8) Mask Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Mask programmable OE/$\overline{OE}$ and $OE_1/\overline{OE}_1$/DC
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH534300A is a 4M-bit mask programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

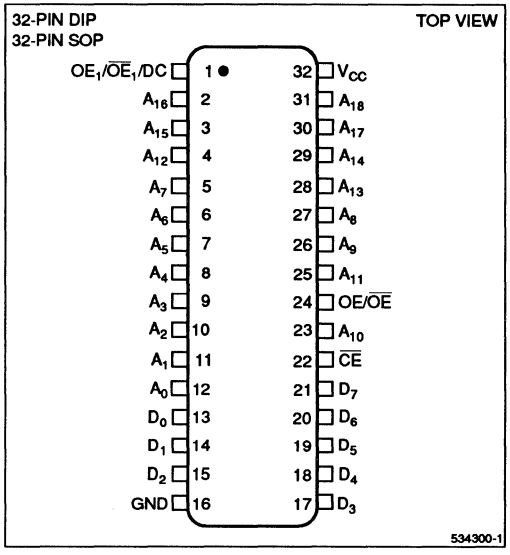


Figure 1. Pin Connections for DIP and SOP Packages

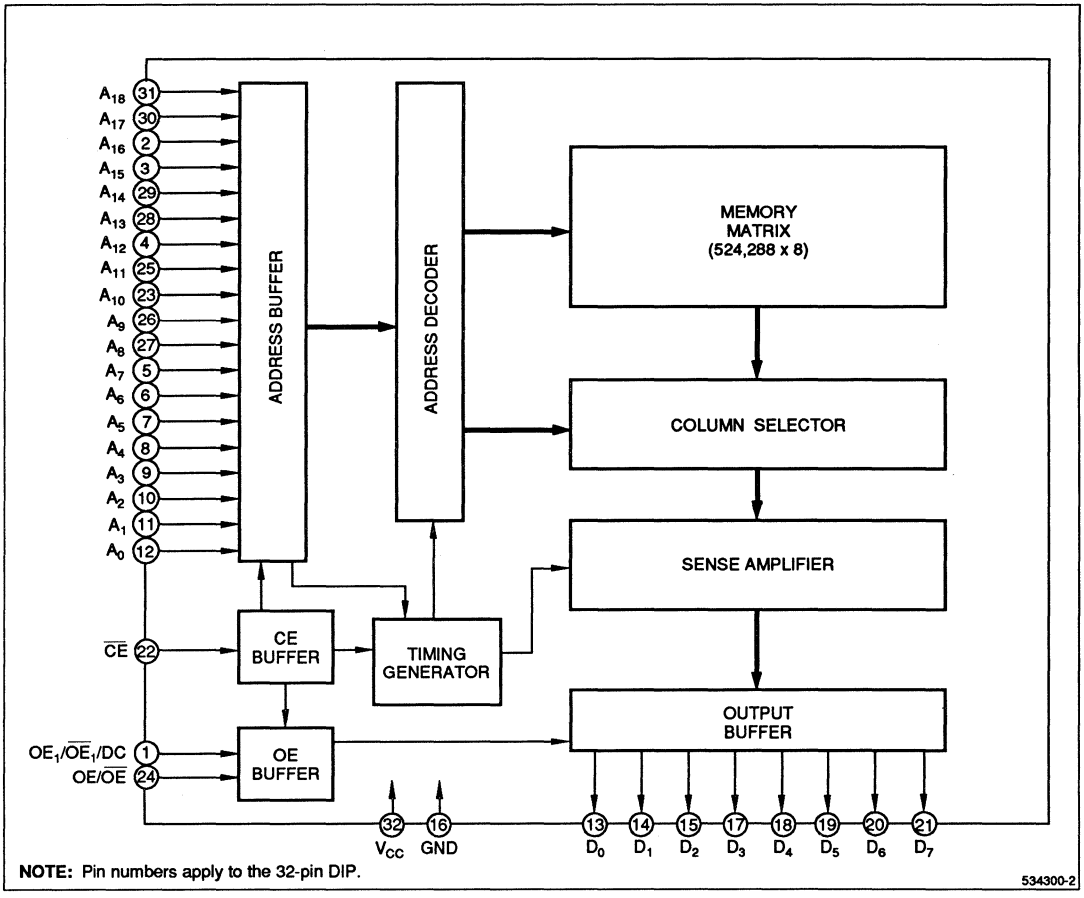


Figure 2. LH534300A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE}_1$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of $OE_1/\overline{OE}_1$/DC and OE/$\overline{OE}$ are mask programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

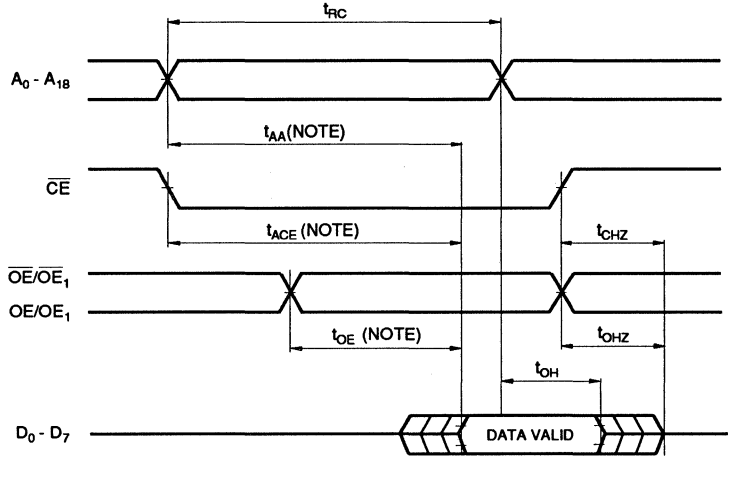
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

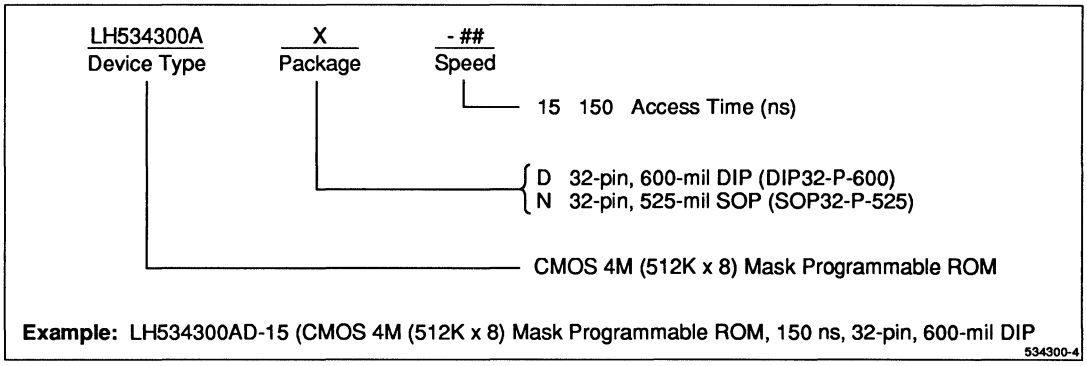


NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.

534300-3

Figure 3. Timing Diagram

ORDERING INFORMATION



LH534400A CMOS 4M (512K × 8) Mask Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
- Programmable $OE_1/\overline{OE}_1$/DC and OE/$\overline{OE}$
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  Compatible with 28-pin 1M mask ROM-specific pinout

DESCRIPTION

The LH534400A is a mask programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

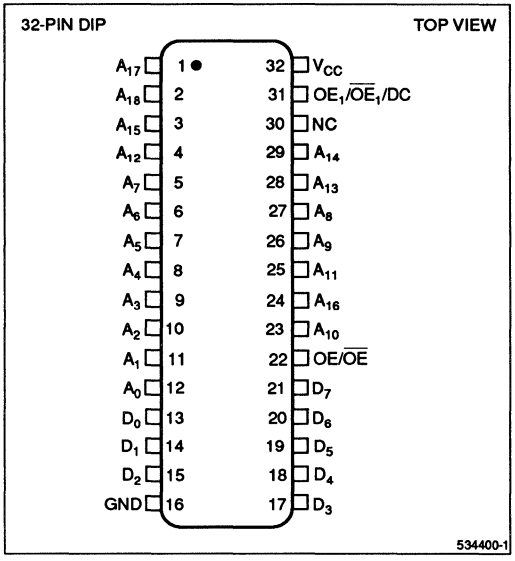


Figure 1. Pin Connections for DIP Package

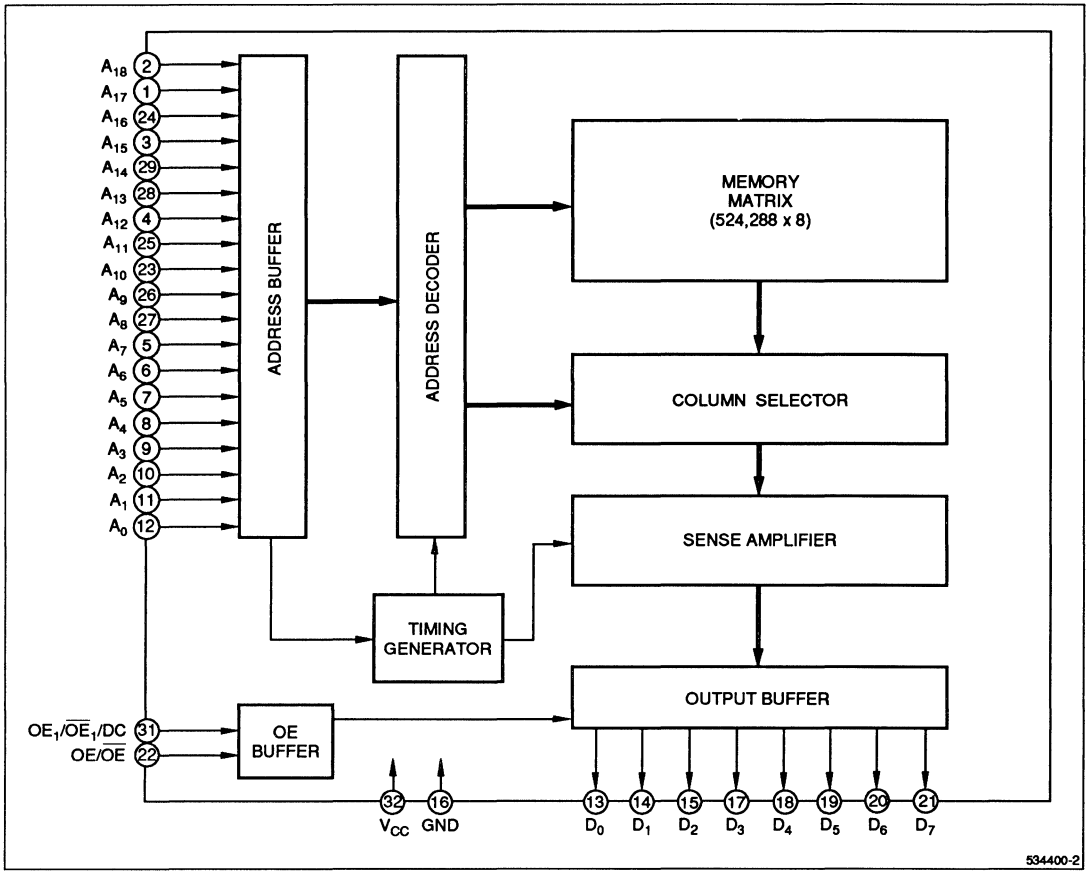


Figure 2. LH534400A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$OE/\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE}_1/DC$	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. The active levels of $OE_1/\overline{OE}_1/DC$ and $OE/\overline{OE}$ are mask programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$OE/\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
L/H	X	Non selected	High-Z	Operating (I_{CC})
X	L/H	Non selected	High-Z	Operating (I_{CC})
H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		

NOTES:
1. $\overline{OE}/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
OE to output in High-Z	t_{OHZ}		70	ns	1

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

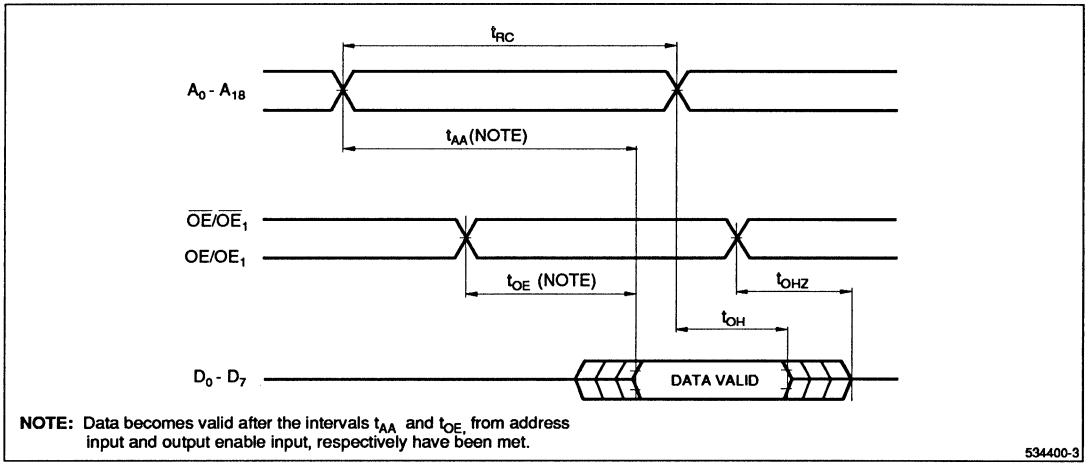


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up, it is necessary to change one or more addresses once the supply is stable. Valid data will be output at t_{AA} following the address transition.

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

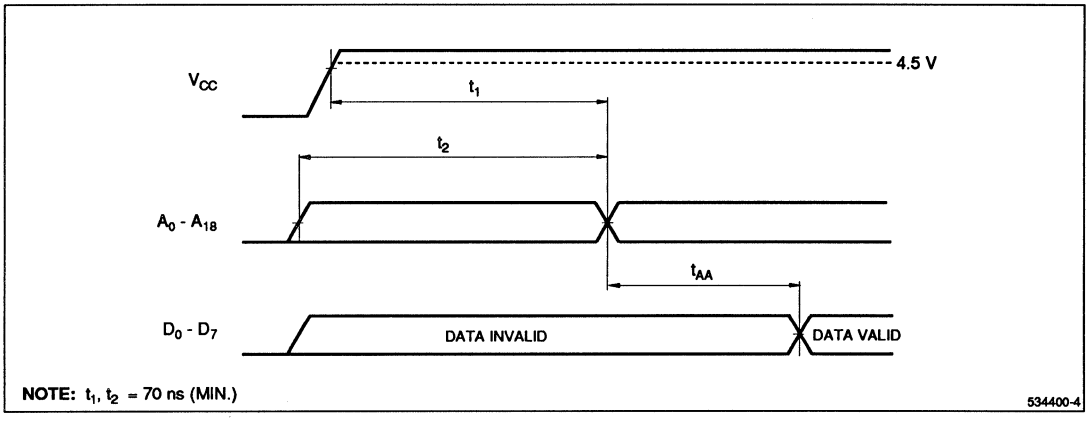
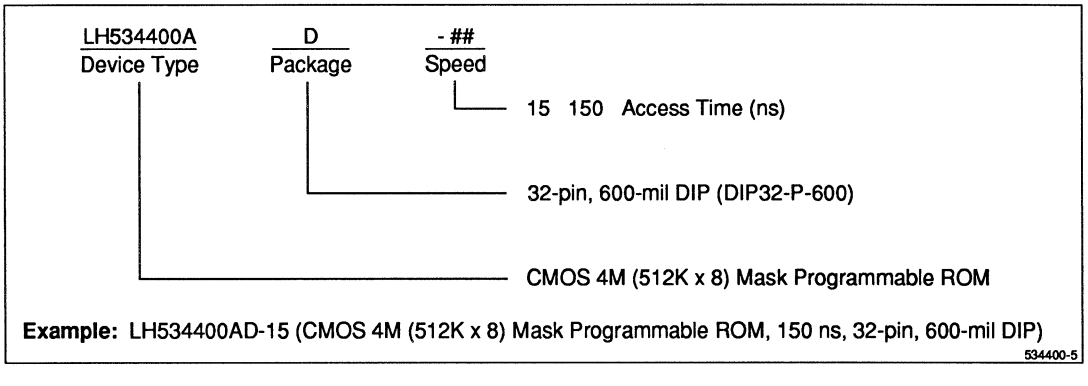


Figure 4. Power Up Initialization

ORDERING INFORMATION



LH534500A

CMOS 4M (512K × 8 / 256K × 16)
Mask Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- Automatic power down mode
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534500A is a 4M bit mask programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

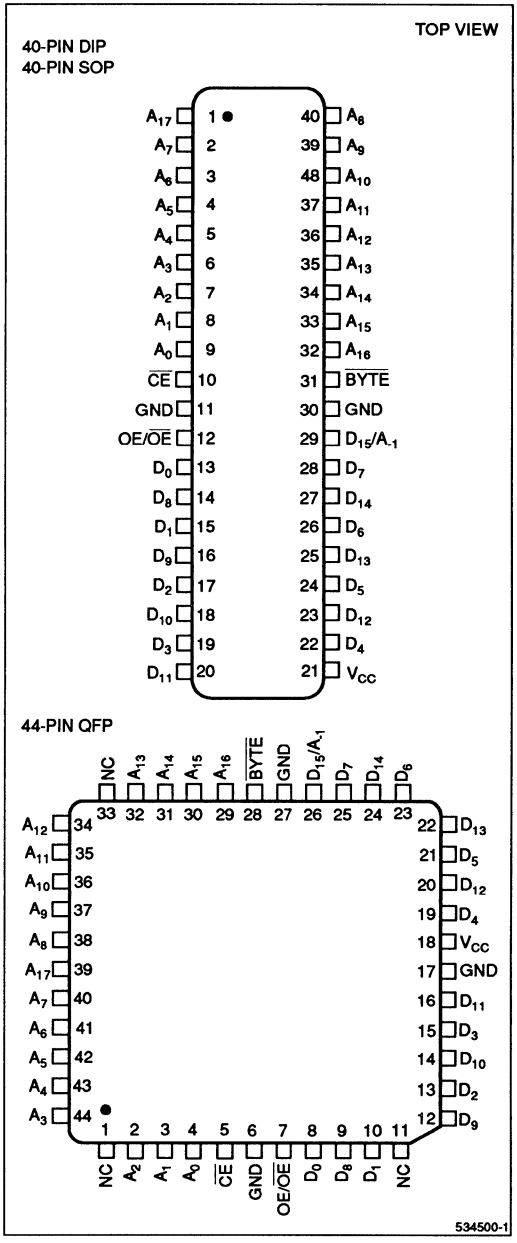


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

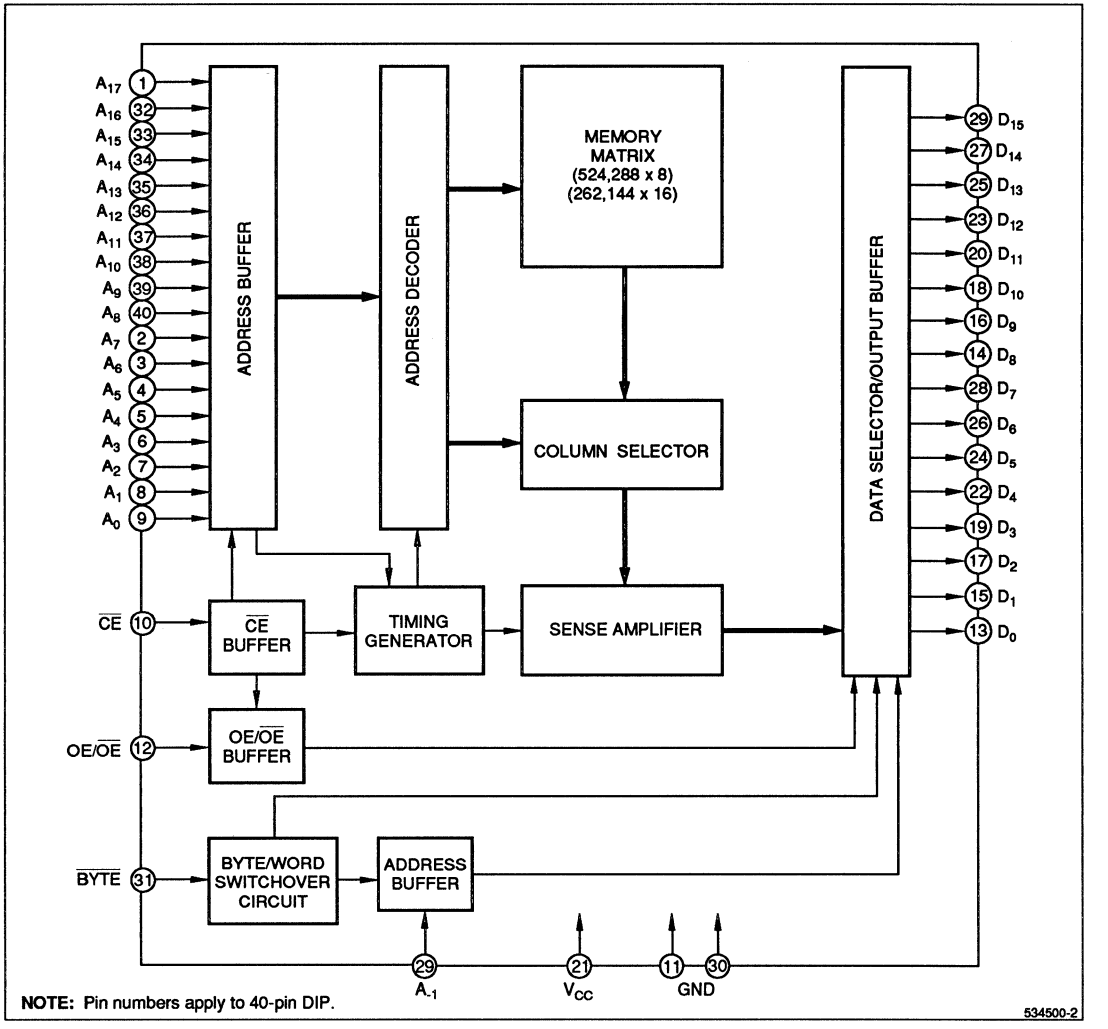


Figure 2. LH534500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Chip Enable input	2
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
X = High or Low
The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			5	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

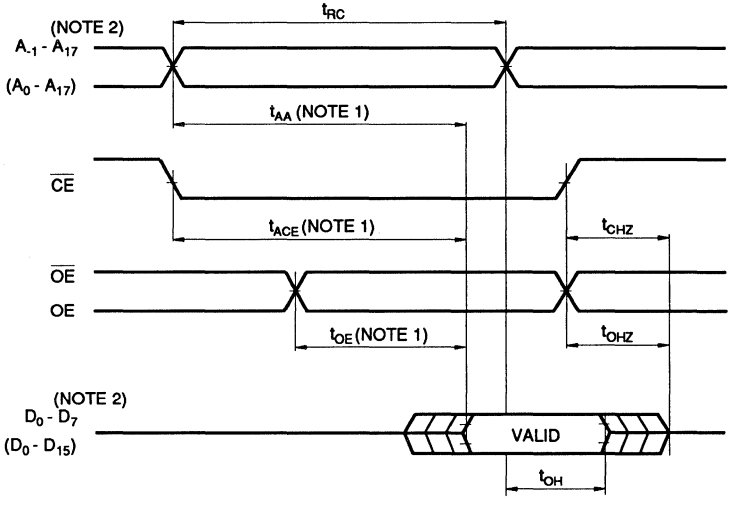
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

534500-3

Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

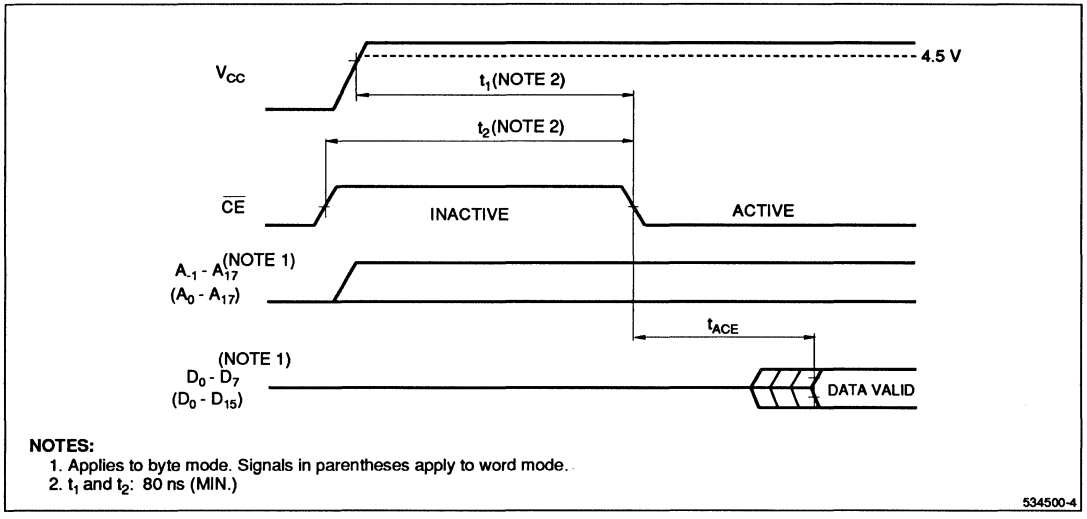
To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

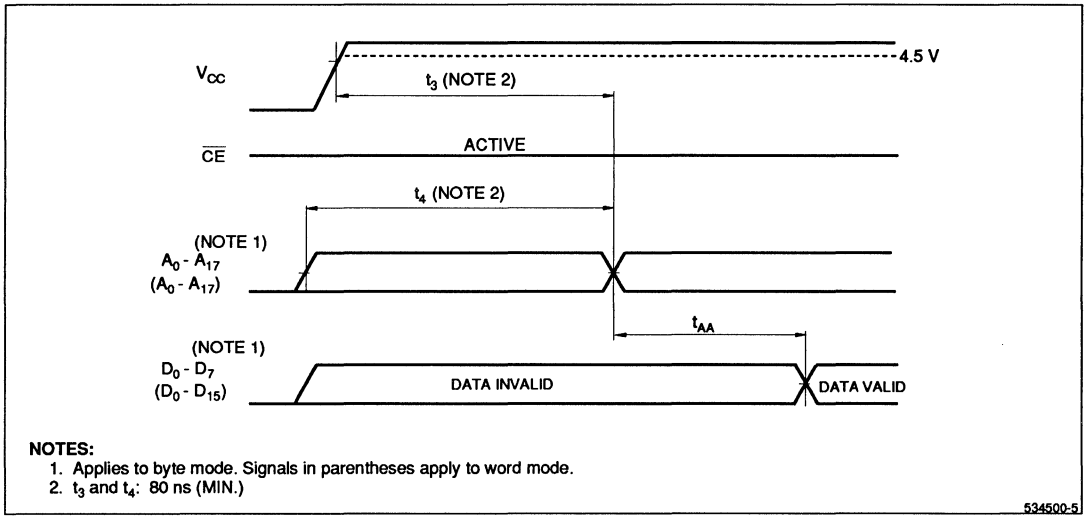
To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.



NOTES:
1. Applies to byte mode. Signals in parentheses apply to word mode.
2. t_1 and t_2: 80 ns (MIN.)

534500-4

Figure 4. Timing Diagram (Power On With $\overline{CE}$ Inactive)

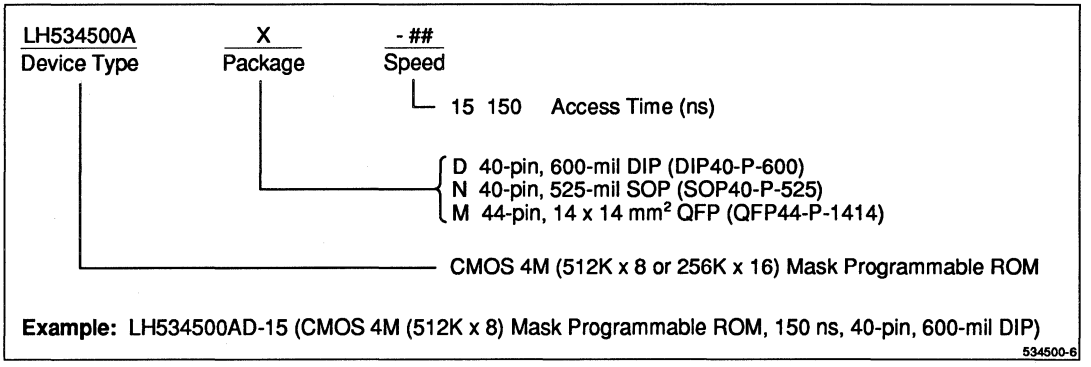


NOTES:
1. Applies to byte mode. Signals in parentheses apply to word mode.
2. t_3 and t_4: 80 ns (MIN.)

534500-5

Figure 5. Timing Diagram (Power On With $\overline{CE}$ Active)

ORDERING INFORMATION



LH534600

CMOS 4M (512K × 8 / 256K × 16) Mask Programmable ROM

FEATURES

- 524,288 × 8 bit organization
  (Byte mode)
  262,144 × 16 bit organization
  (Word mode)
- $\overline{BYTE}$ input pin selects bit configuration
- Access time: 100 ns (MAX.)
- Low power consumption:
  Operating: 550 mW (MAX.)
  Standby: 1.65 mW (MAX.)
- Static operation (Internal sync. system)
- Automatic power down mode
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534600 is a 4M bit mask programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

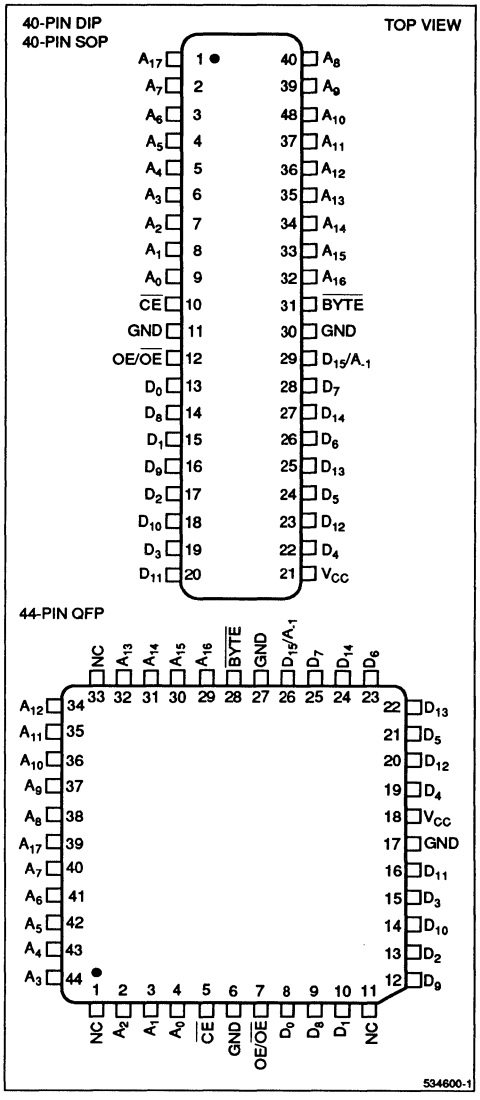


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

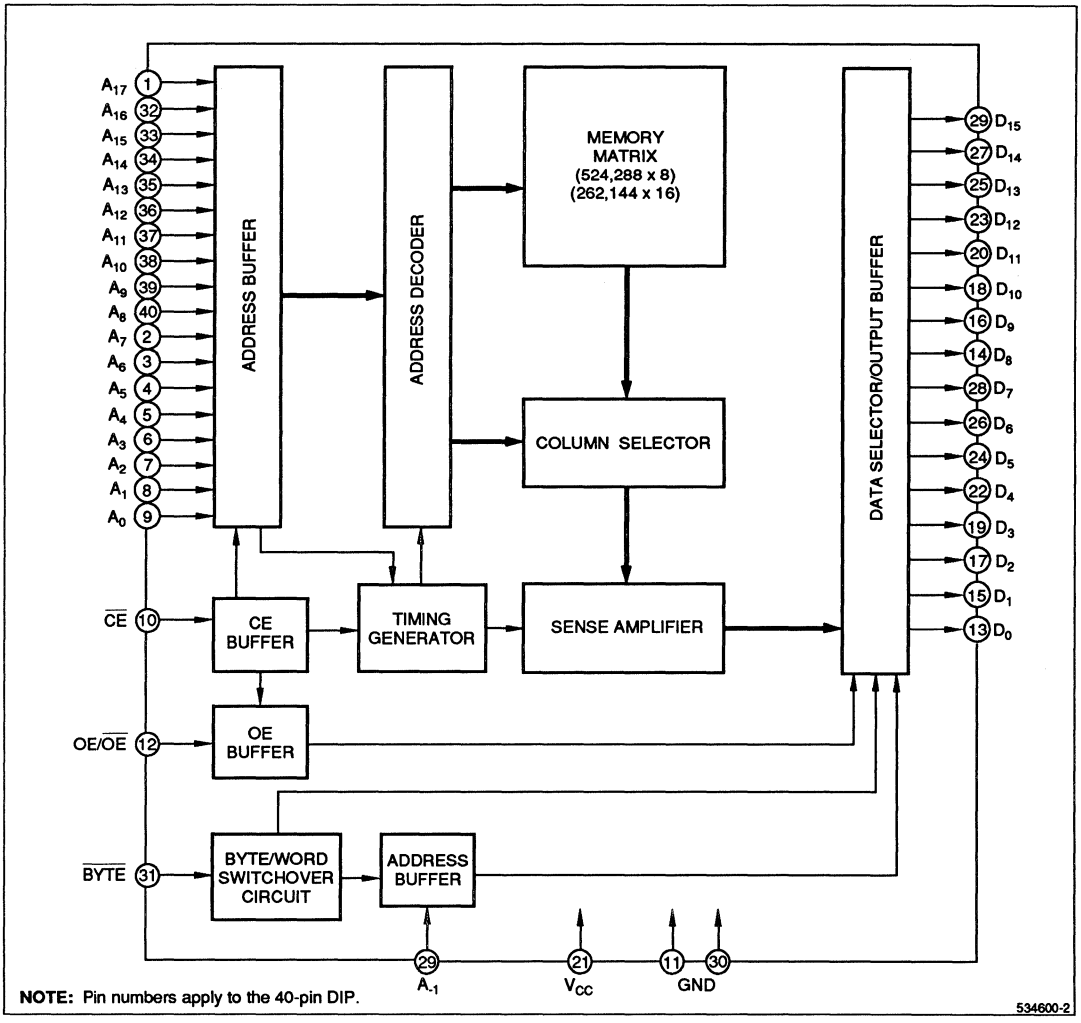


Figure 2. LH534600 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input ($\overline{BYTE}$ MODE)	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output Enable input	2
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})	
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})	

NOTE:
1. The input state of $\overline{BYTE}$ pin must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low.
   X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns			100	mA	2
	I_{CC2}	t_{RC} = 1 µs			70		
	I_{CC3}	t_{RC} = 100 ns			100	mA	3
	I_{CC4}	t_{RC} = 1 µs			70		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			300	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH534600			UNIT	NOTE
		MIN.	TYP.	MAX.		
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			40	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			40	ns	1
OE to ouput in High-Z	t_{OHZ}			40	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

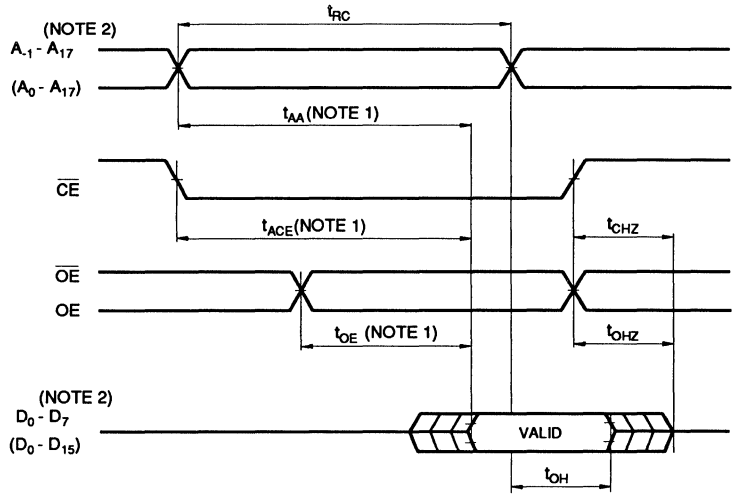
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

CAUTION

To stabillize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

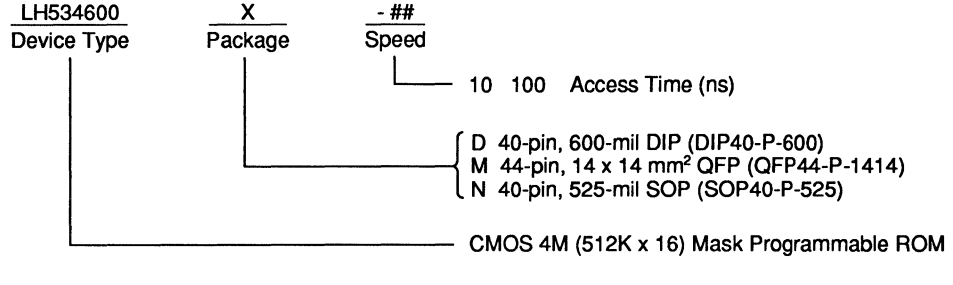


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input and output enable input, respectively have been met.
2. Apply to byte mode. Signals in parentheses apply to word mode.

534600-3

Figure 3. Timing Diagram

ORDERING INFORMATION



Example: LH534600D-10 (CMOS 4M Mask Programmable ROM, 100 ns, 40-pin, 600-mil DIP)

534600-4

LH538000

CMOS 8M (1M × 8 / 512K × 16) Mask Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH538000 is a mask programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

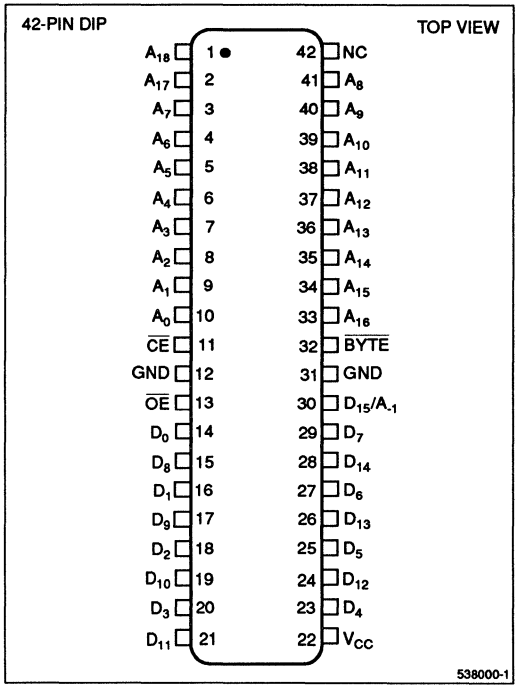


Figure 1. Pin Connections for DIP Package

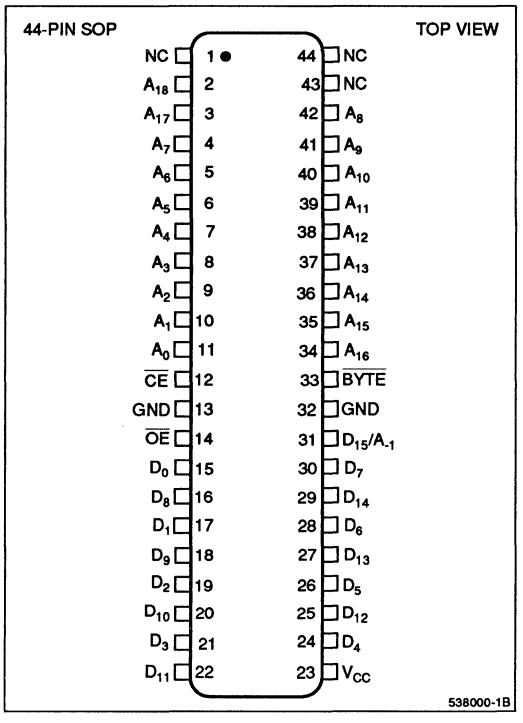


Figure 3. Pin Connections for SOP Package

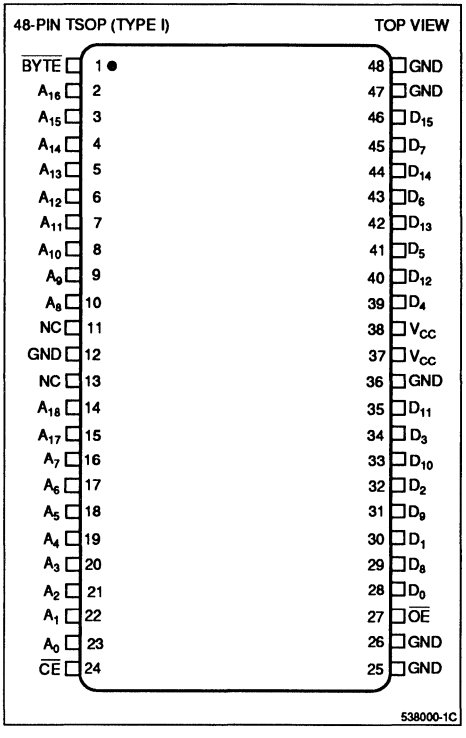


Figure 4. Pin Connections for TSOP Package

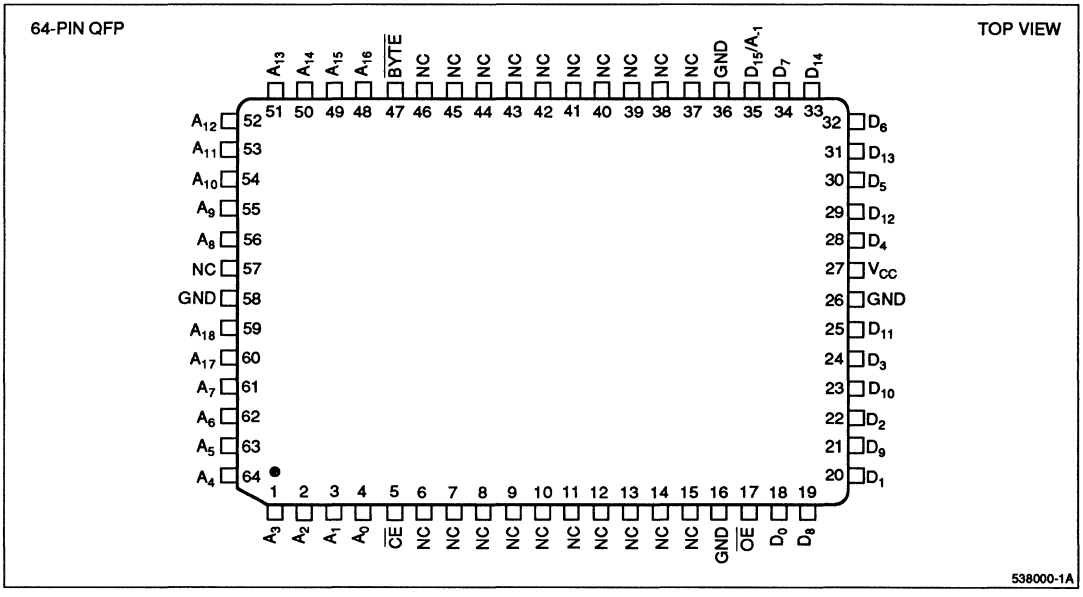


Figure 2. Pin Connections for QFP Package

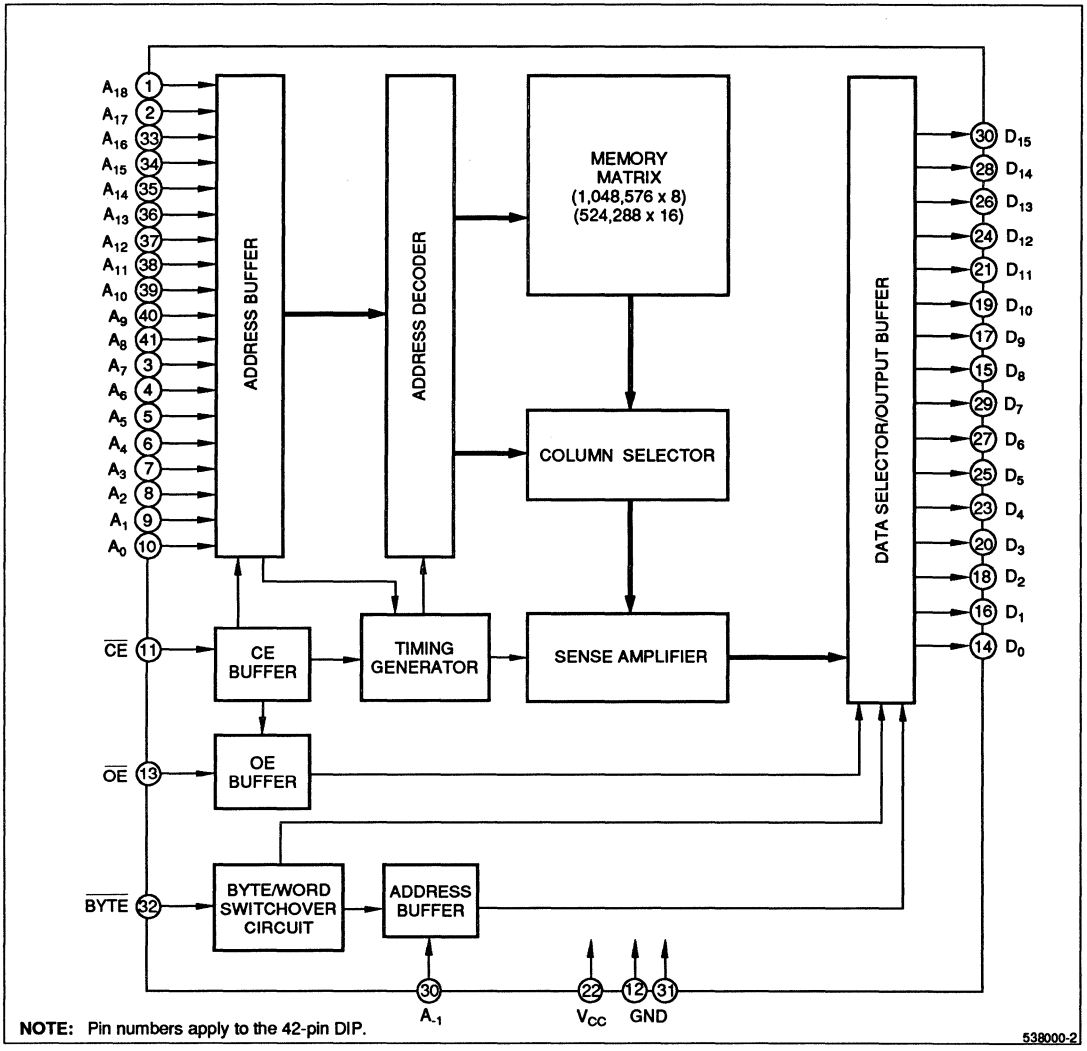


Figure 5. LH538000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte Mode)	1
A_0 - A_{18}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	
L	L	L	L	Byte	D_0 - D_7	High-Z	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}$ /$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

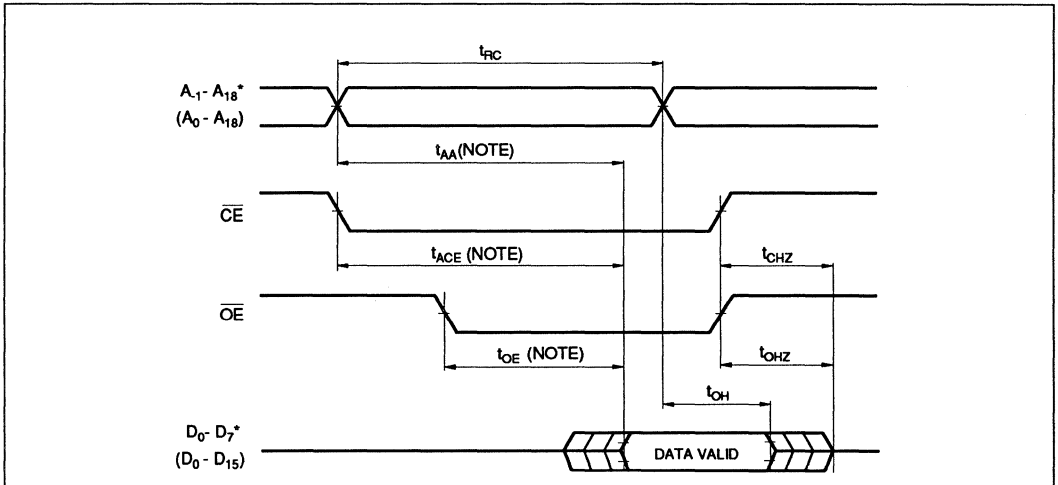
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable and output enable, respectively have been met.
2. (*) Applied to byte mode. Signals in parentheses apply to word mode.

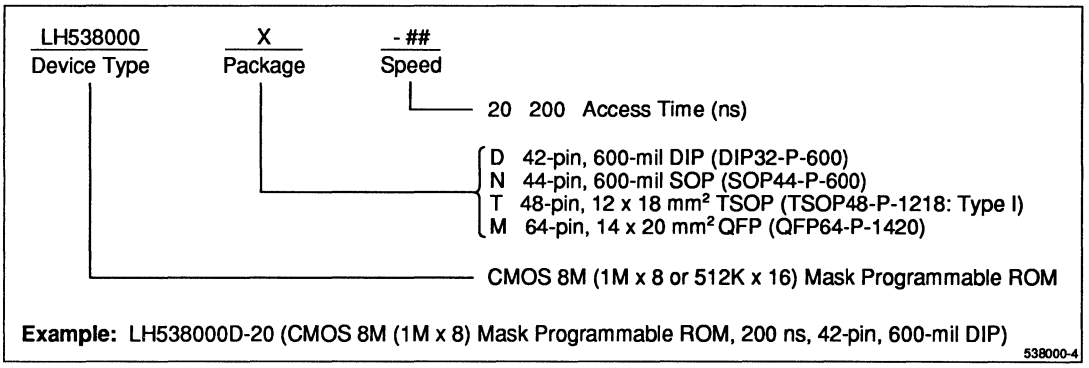
538000-3

Figure 6. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



Example: LH538000D-20 (CMOS 8M (1M x 8) Mask Programmable ROM, 200 ns, 42-pin, 600-mil DIP)

538000-4

LH538100

CMOS 8M (1M × 8) Mask Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 500 μW (MAX.)
- Programmable output enable
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH538100 is a mask programmable ROM organized as 1,048,576 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

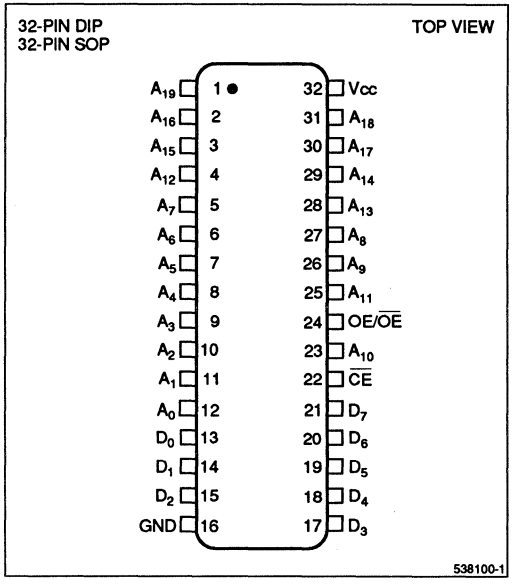


Figure 1. Pin Connections for DIP and SOP Packages

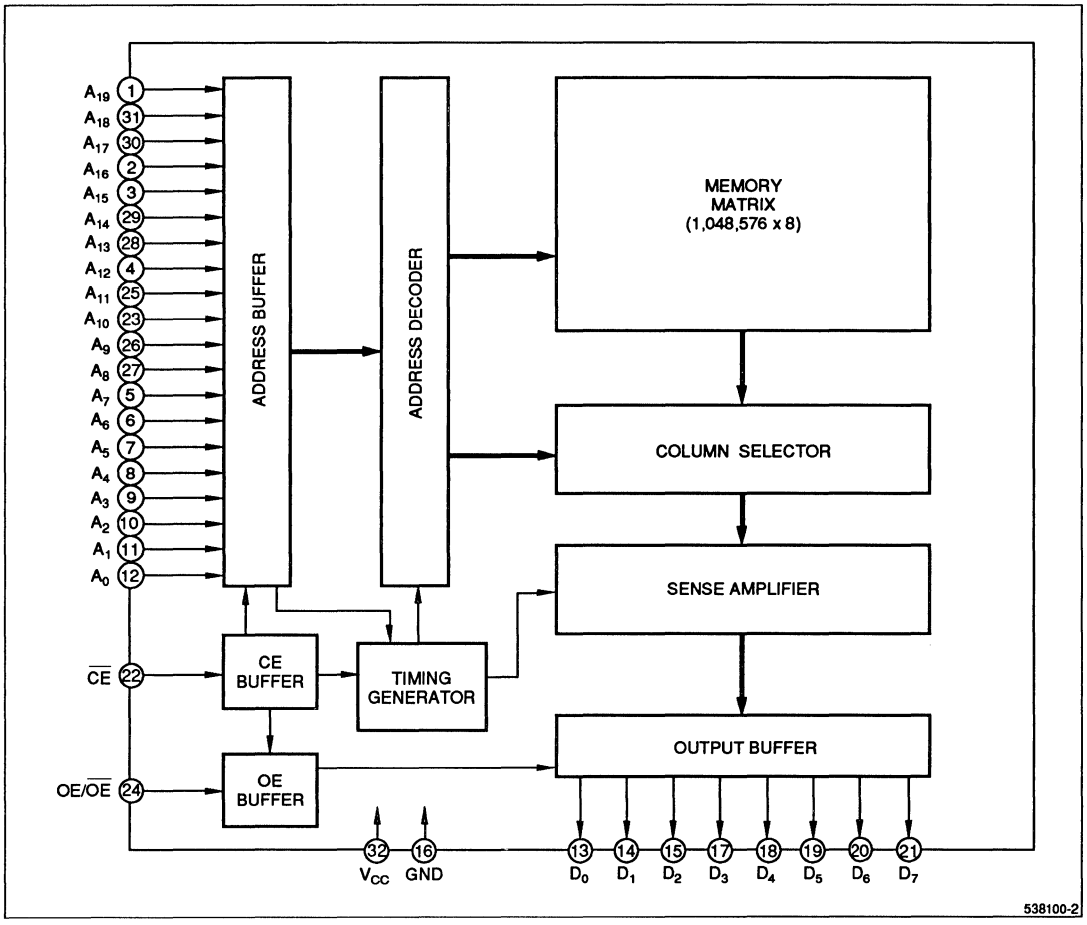


Figure 2. LH538100 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{19}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output Enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. The active level of OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	Non selected	High-Z	Standby (I_{SB})
L	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			40		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}$ = V_{IH} or OE/$\overline{OE}$ = V_{IL}/V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable time	t_{ACE}			200	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

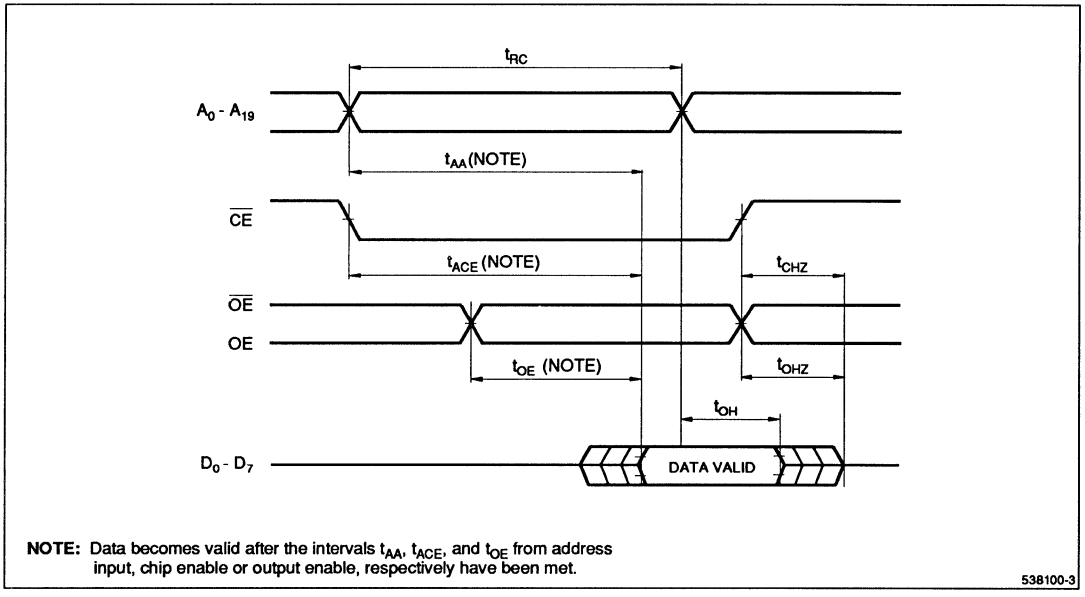
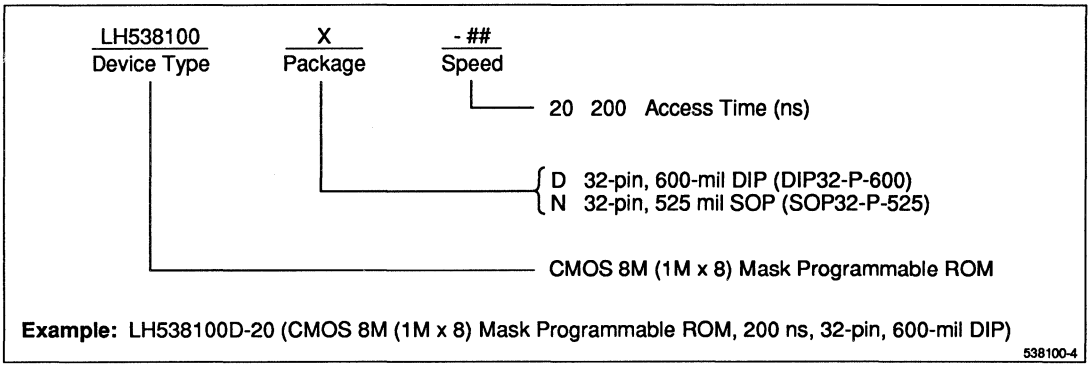


Figure 3. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



Example: LH538100D-20 (CMOS 8M (1M x 8) Mask Programmable ROM, 200 ns, 32-pin, 600-mil DIP)

538100-4

LH538200

CMOS 8M (1M × 8) Mask Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
- Programmable $OE_1/\overline{OE}_1/DC$
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package:
  32-pin, 600-mil DIP
  Compatible with 28-pin 1M-bit mask programmable ROM-specific pinout

DESCRIPTION

The LH538200 is a mask programmable ROM organized as 1,048,576 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

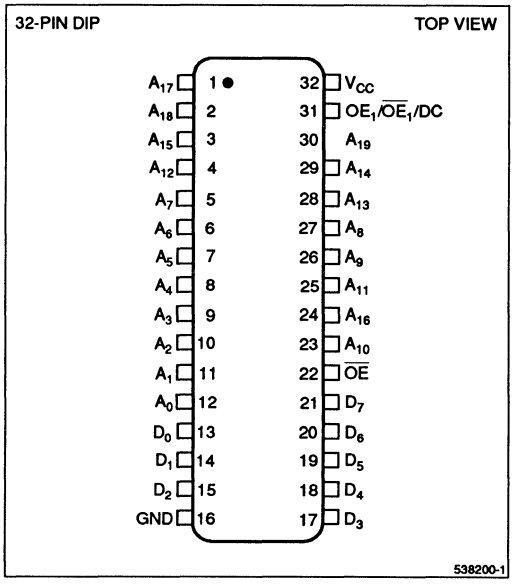


Figure 1. Pin Connections for DIP Package

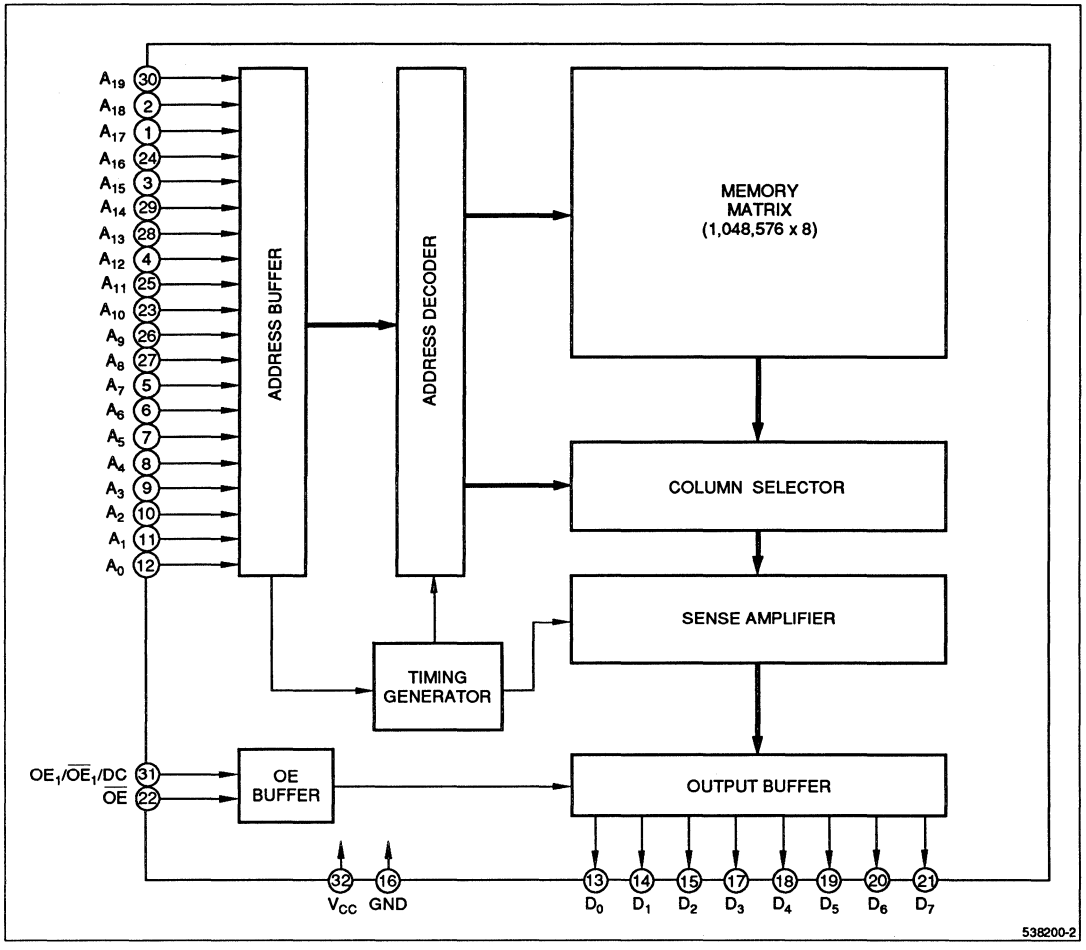


Figure 2. LH538200 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{19}	Address input	
D_0 - D_7	Data output	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. The active level of $OE_1/\overline{OE_1}$/DC is mask programmable.
   Selecting DC allows the outputs to be active for both high and low levels that are applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{OE}$	$OE_1/\overline{OE_1}/DC$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	Non selected	High-Z	Operating (I_{CC})
X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			40		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			35		

NOTES:
1. $\overline{OE}/\overline{OE_1}$ = V_{IH} or OE_1= V_{IL}.
2. V_{IN} = V_{IH}/V_{IL}, outputs open.
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, outputs open.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Output enable delay time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
OE to output in High-Z	t_{OHZ}			70	ns	1

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

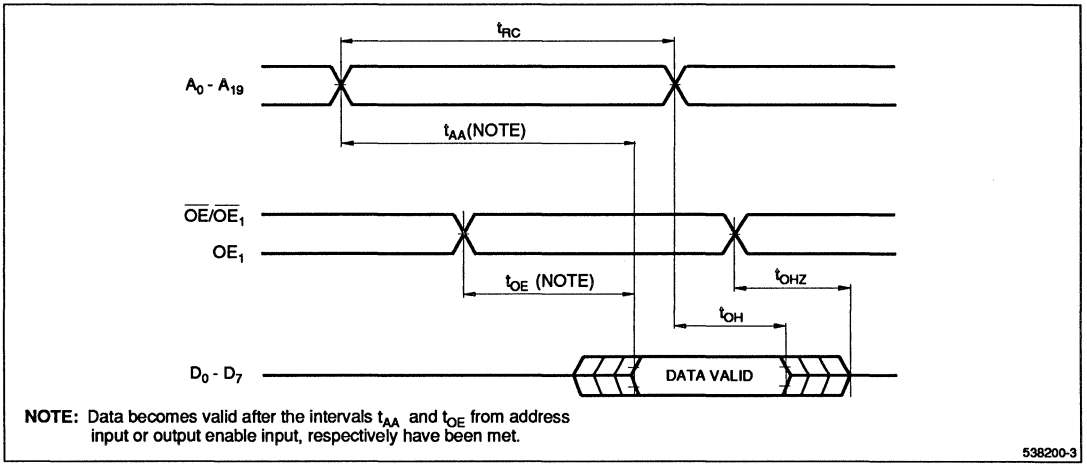
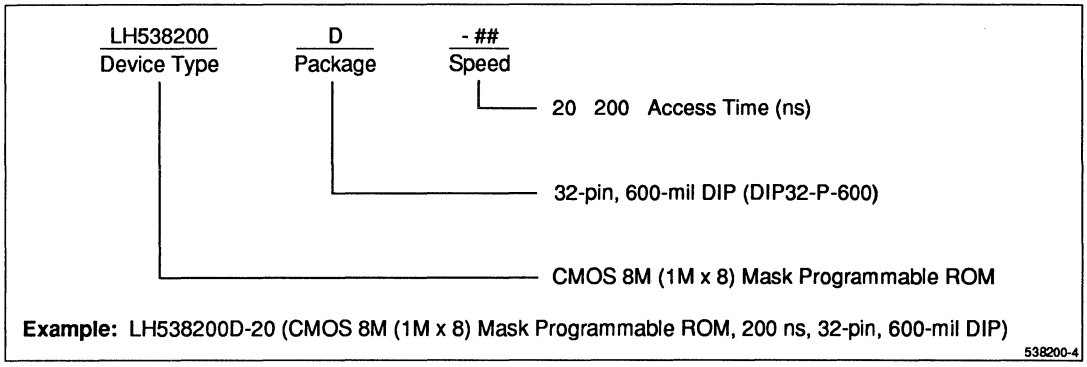


Figure 3. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



LH538500A

CMOS 8M (1M × 8 / 512K × 16)
Mask Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  64-pin, 14 × 20 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP I
- X16 word-wide pinout

DESCRIPTION

The LH538500A is a mask programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

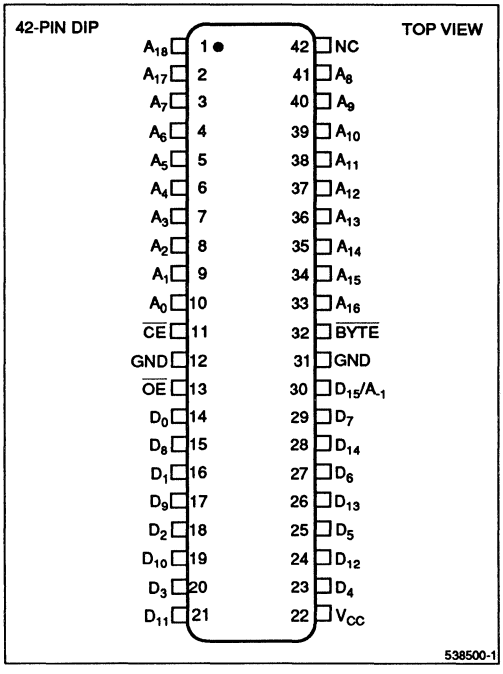


Figure 1. Pin Connections for DIP Package

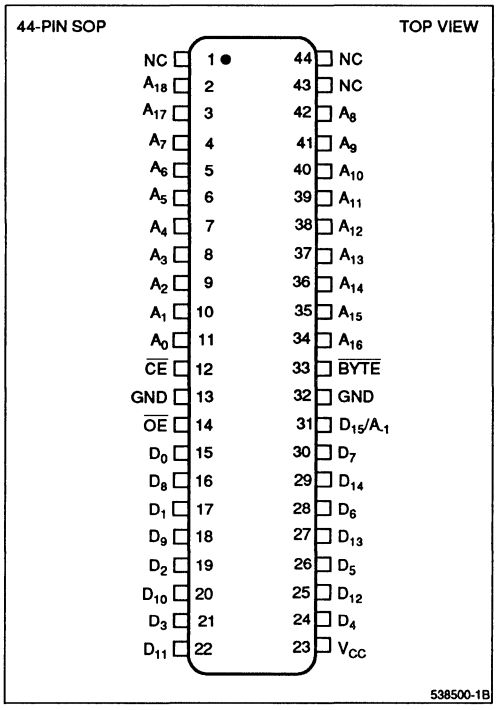


Figure 2. Pin Connections for SOP Package

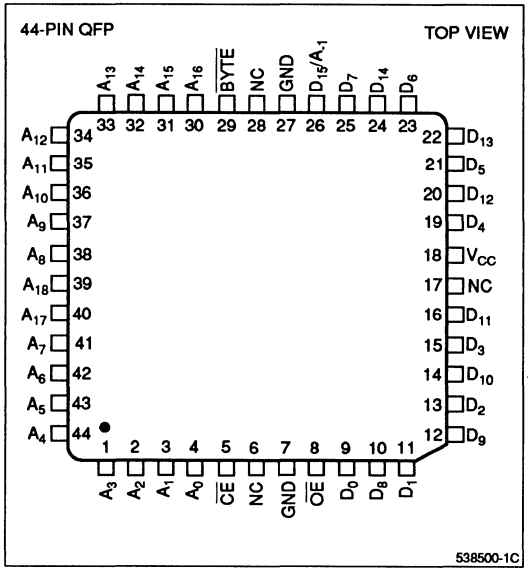


Figure 3. Pin Connections for 44-Pin QFP

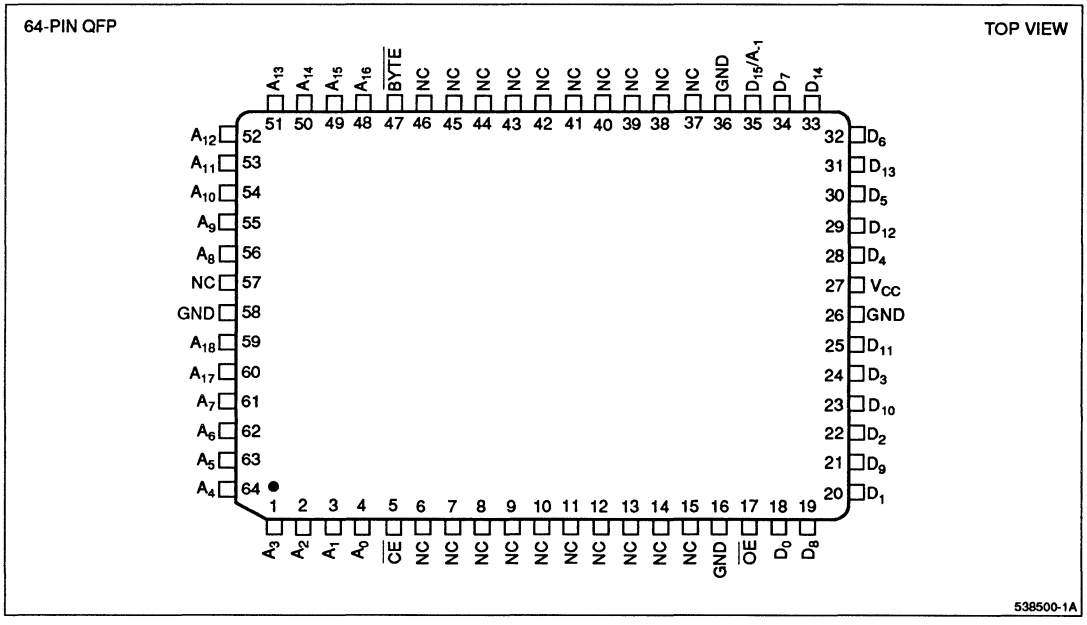


Figure 4. Pin Connections for 64-Pin QFP Package

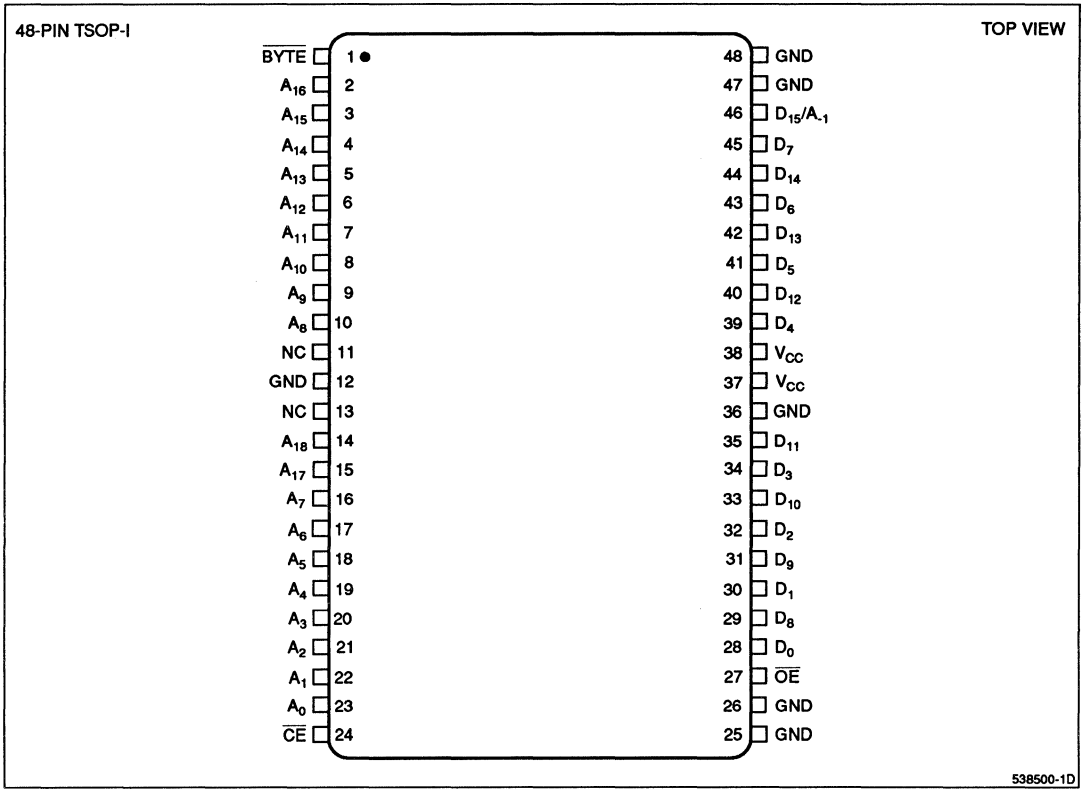


Figure 5. Pin Connections for TSOP Package

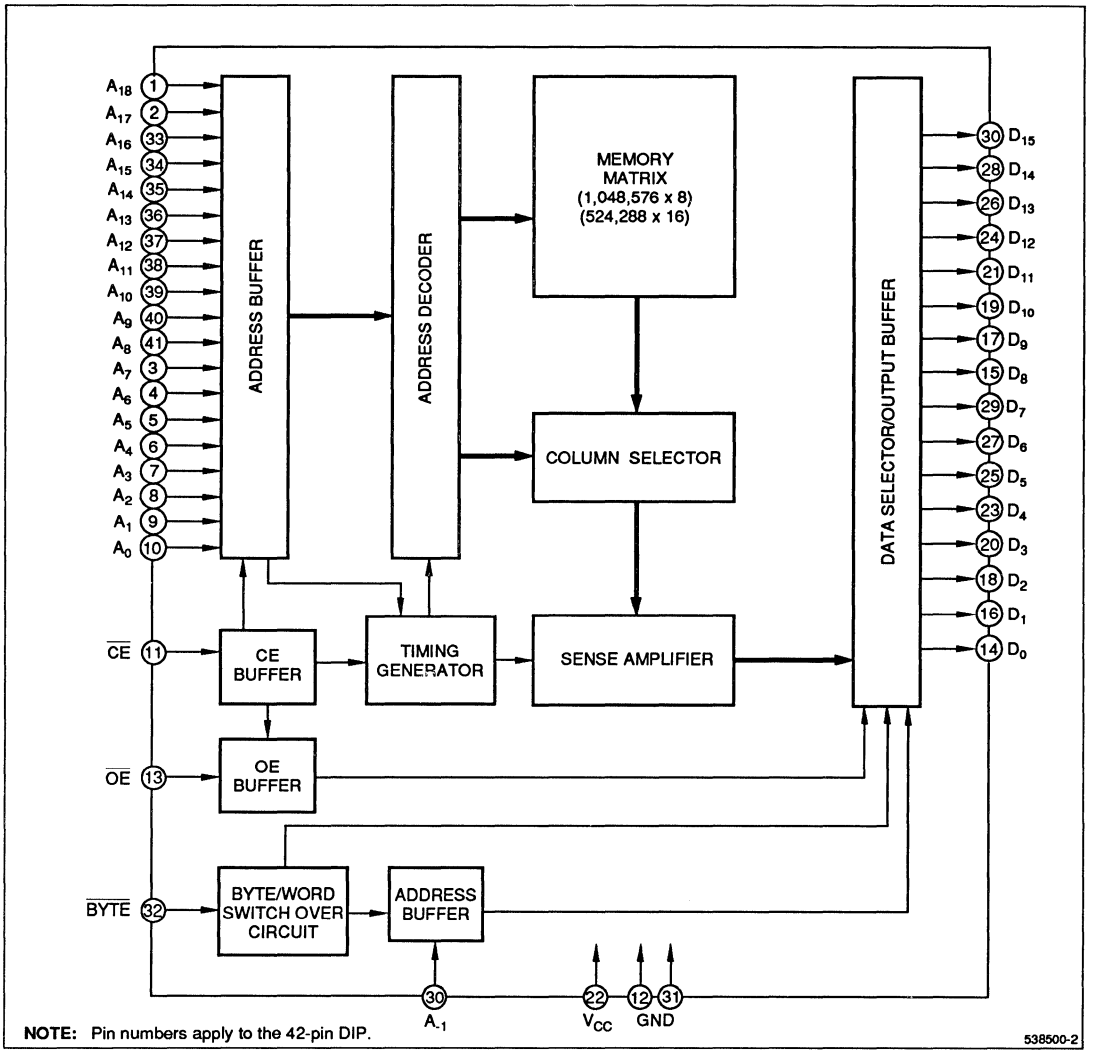


Figure 6. LH538500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte mode)	1
A_0 - A_{18}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ *	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})	
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L
   * $\overline{BYTE}$ input state must be set to H or L and must not be changed during operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

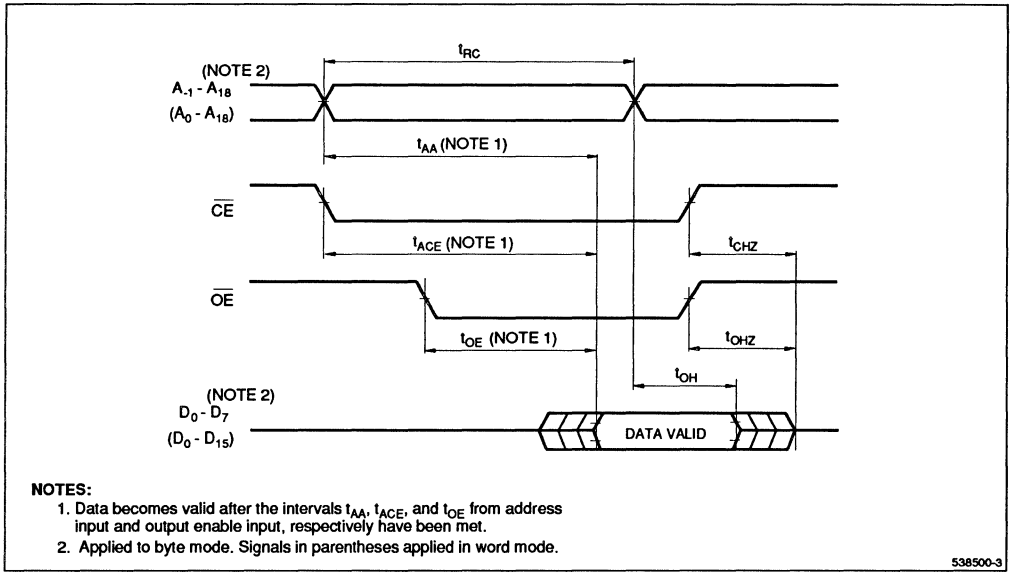
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input and output enable input, respectively have been met.
2. Applied to byte mode. Signals in parentheses applied in word mode.

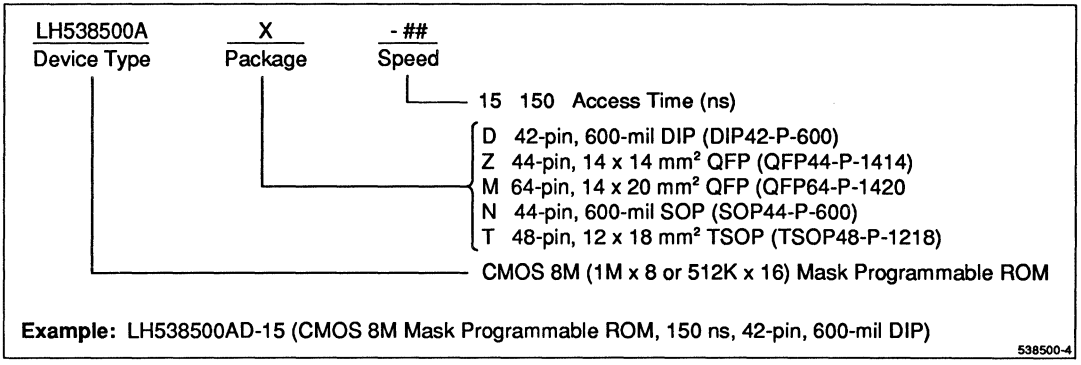
538500-3

Figure 7. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the Vcc pin and GND.

ORDERING INFORMATION



Example: LH538500AD-15 (CMOS 8M Mask Programmable ROM, 150 ns, 42-pin, 600-mil DIP)

538500-4

LH5316000

CMOS 16M (2M × 8 / 1M × 16)
Mask Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode)
  1,048,576 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  64-pin, 750-mil SDIP
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH5316000 is a mask programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by an input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

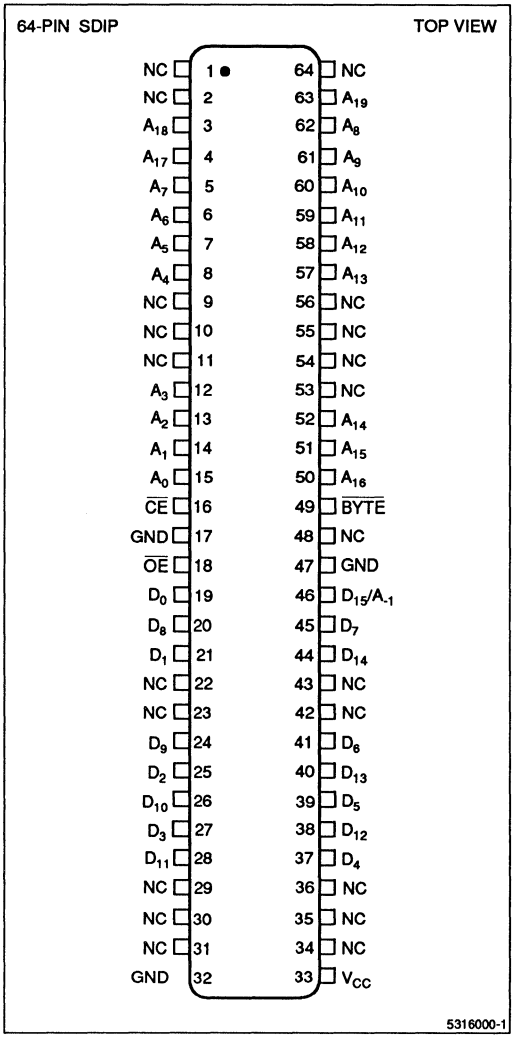


Figure 1. Pin Connections for SDIP Package

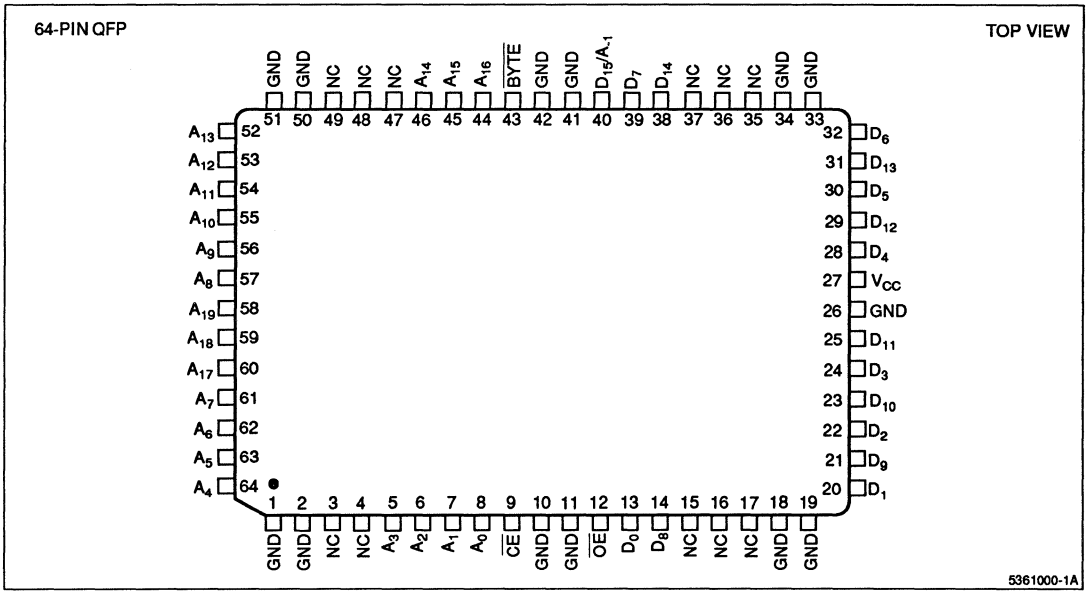


Figure 2. Pin Connections for QFP Package

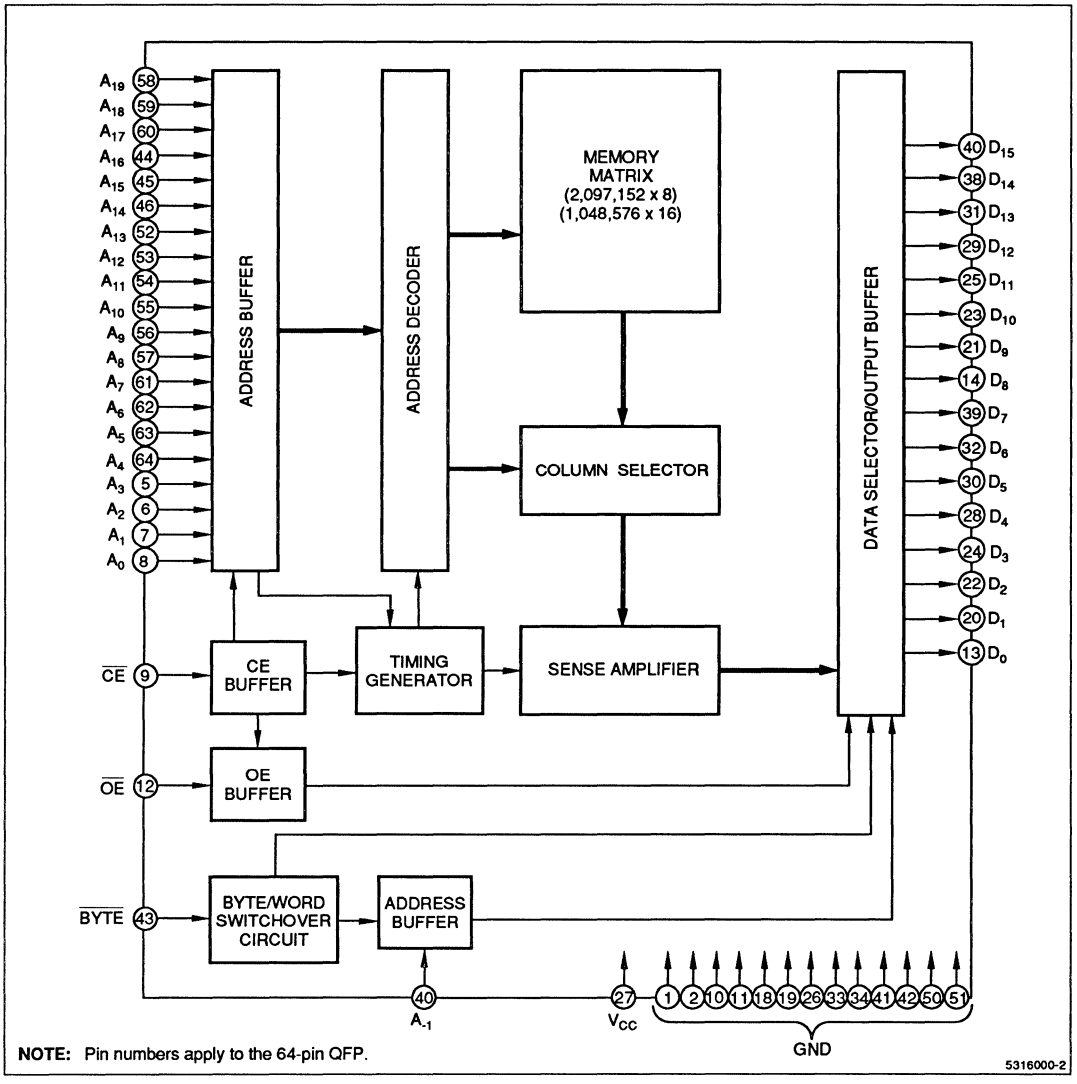


Figure 3. LH5316000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte Mode)	1
A_0 - A_{19}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}$ /$\overline{OE}$ = V_{IH}.
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open.
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

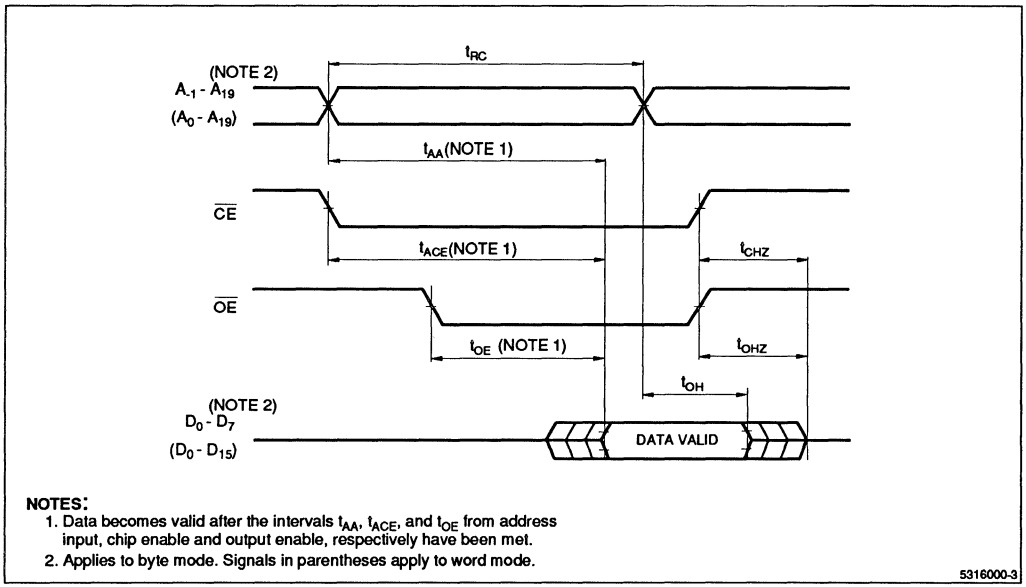
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

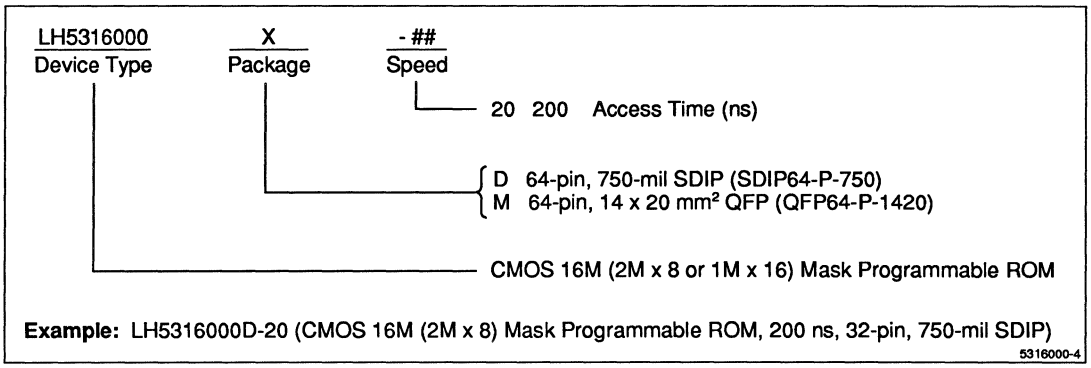
5316000-3

Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



Example: LH5316000D-20 (CMOS 16M (2M x 8) Mask Programmable ROM, 200 ns, 32-pin, 750-mil SDIP)

5316000-4

PRELIMINARY

LH5332000

CMOS 32M (4M × 8 / 2M × 16)
Mask Programmable ROM

FEATURES

- 4,194,304 × 8 bit organization
  (Byte mode)
  2,097,152 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  44-pin, 600-mil SOP
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH5332000 is a mask programmable ROM organized as 4,194,304 × 8 bits (Byte mode) or 2,097,152 × 16 bits (Word mode) that can be selected by input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

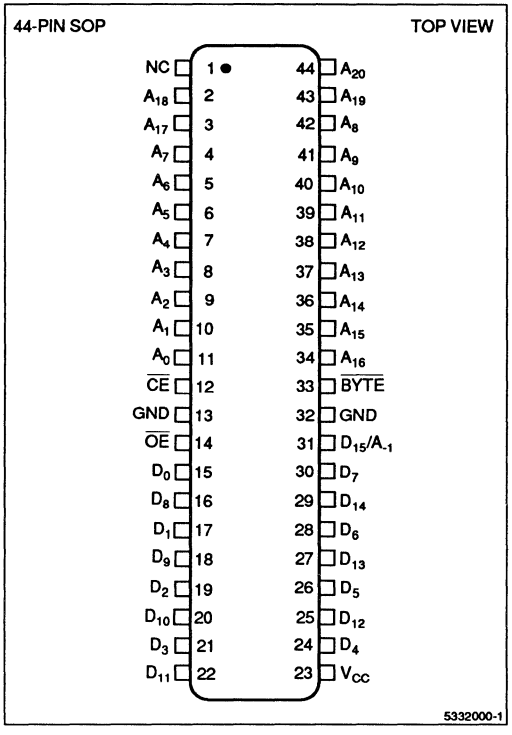


Figure 1. Pin Connections for SOP Package

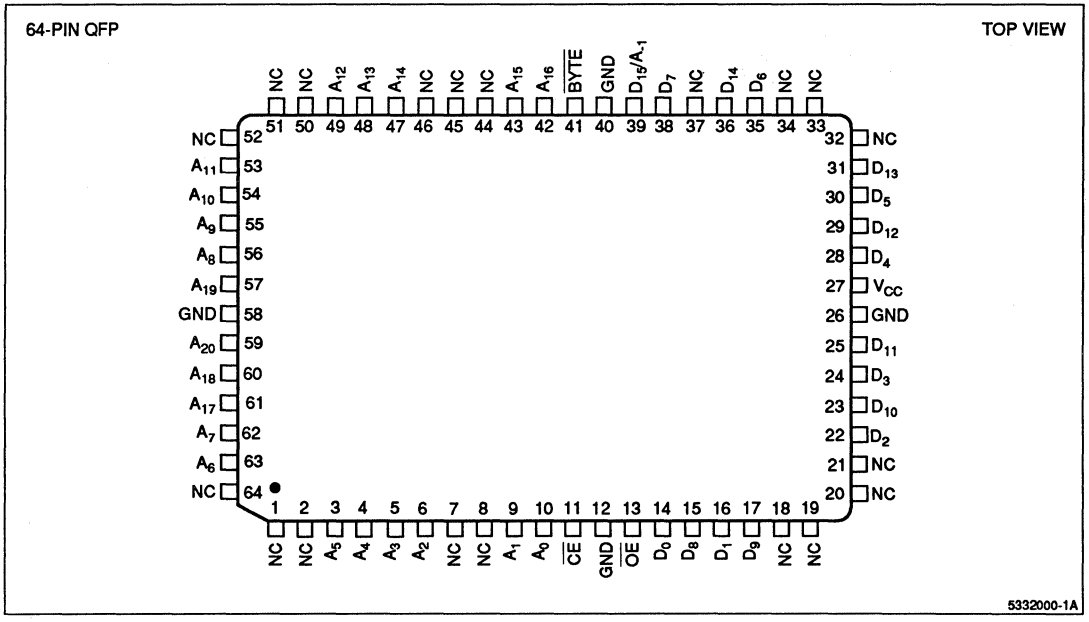


Figure 2. Pin Connections for QFP Package

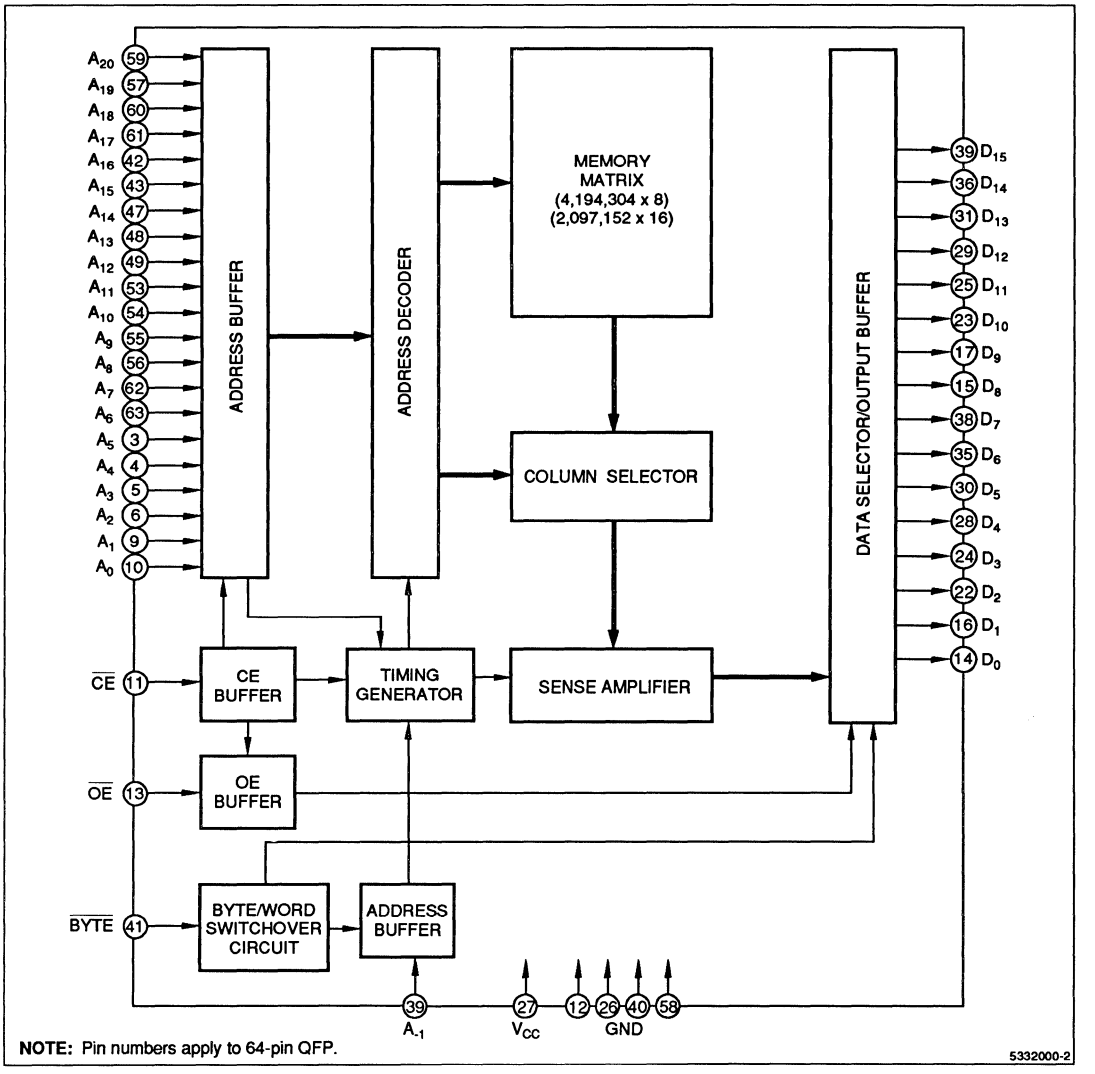


Figure 3. LH5332000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte mode)	1
A_0 - A_{20}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ *	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}		
L	L	L	L	Byte	D_0 - D_7	High-Z		
L	L	L	H	Byte	D_8 - D_{15}	High-Z		

NOTE:
1. X = H or L
   * $\overline{BYTE}$ input state must be set to H or L which must not be changed during operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

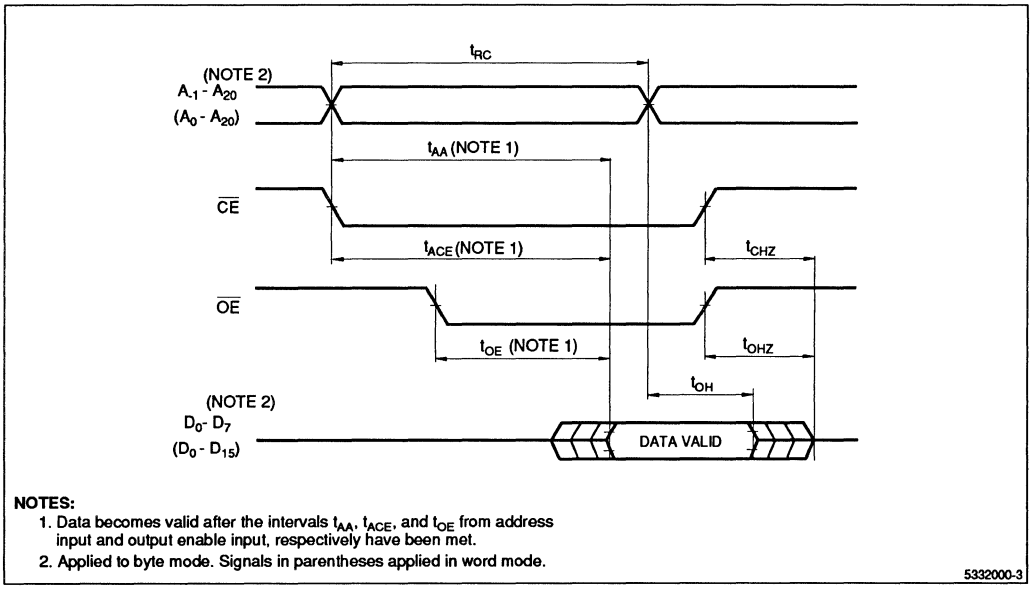
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input and output enable input, respectively have been met.
2. Applied to byte mode. Signals in parentheses applied in word mode.

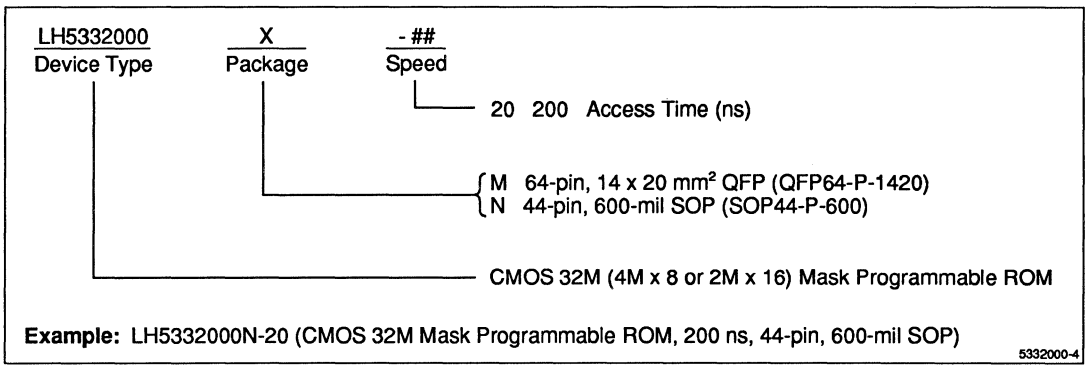
5332000-3

Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



Example: LH5332000N-20 (CMOS 32M Mask Programmable ROM, 200 ns, 44-pin, 600-mil SOP)

5332000-4

LH5481
LH5491

Cascadeable 64 × 8 FIFO
Cascadeable 64 × 9 FIFO

FEATURES

- Fastest 64 × 8/9 Cascadeable FIFO 35/25/15 MHz
- Expandable in Word Width & FIFO Depth
- Almost-Full/Almost-Empty & Half-Full Flags
- Fully Independent Asynchronous Inputs & Outputs
- LH5481 Output Enable forces Data Outputs to High-Impedance State
- Pin Compatible & Cascadeable with LH5485/5495 256 × 8/9 FIFOs
- Industry Standard Pinout
- 28-Pin, 300-mil DIP & 28-Pin PLCC Packaging

FUNCTIONAL DESCRIPTION

The LH5481 and LH5491 are high-performance, asynchronous First-In, First-Out (FIFO) memories organized 64 words deep by 8 or 9-bits wide. The 8-bit LH5481 has an Output Enable ($\overline{OE}$) function, which can be used to force the eight data outputs (DO) to a high-impedance state. The LH5491 has nine data outputs.

These FIFOs accept 8 or 9-bit data at the Data Inputs (DI). A Shift In (SI) signal writes the DI data into the FIFO. A Shift Out (SO) signal shifts stored data to the Data Outputs (DO). The Output Ready (OR) signal indicates when valid data is present on the DO outputs.

If the FIFO is full and unable to accept more DI data Input Ready (IR) will not return high and SI pulses will be ignored. If the FIFO is empty and unable to shift data to the DO outputs, OR will not return high and SO pulses will be ignored. The Almost-Full/Almost-Empty (AFE) flag is asserted (HIGH) when the FIFO is almost-full (56 words or more) or almost- empty (8 words or less). The Half-Full (HF) flag is asserted (HIGH) when the FIFO contains 32 words or more.

Reading and writing operations may be asynchronous, allowing these FIFOs to be used as buffers between digital machines of different operating frequencies. The high speed makes these FIFOs ideal for high performance communication and controller applications.

PIN CONNECTIONS

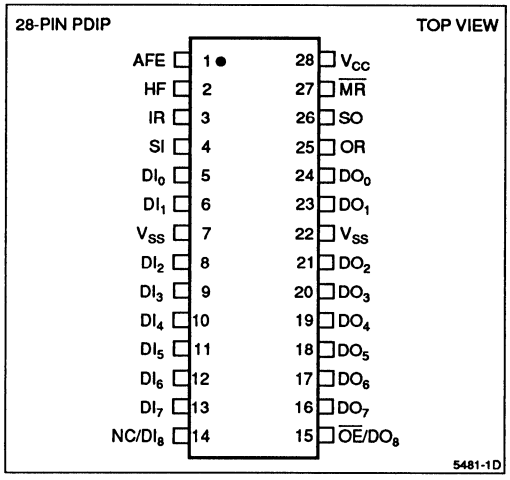


Figure 1. Pin Connections for DIP Package

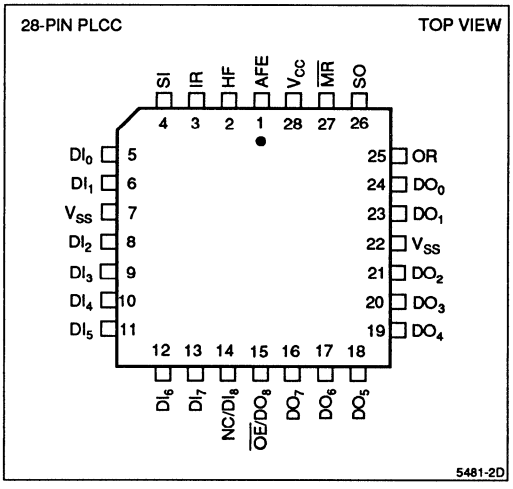


Figure 2. Pin Connections for PLCC Package

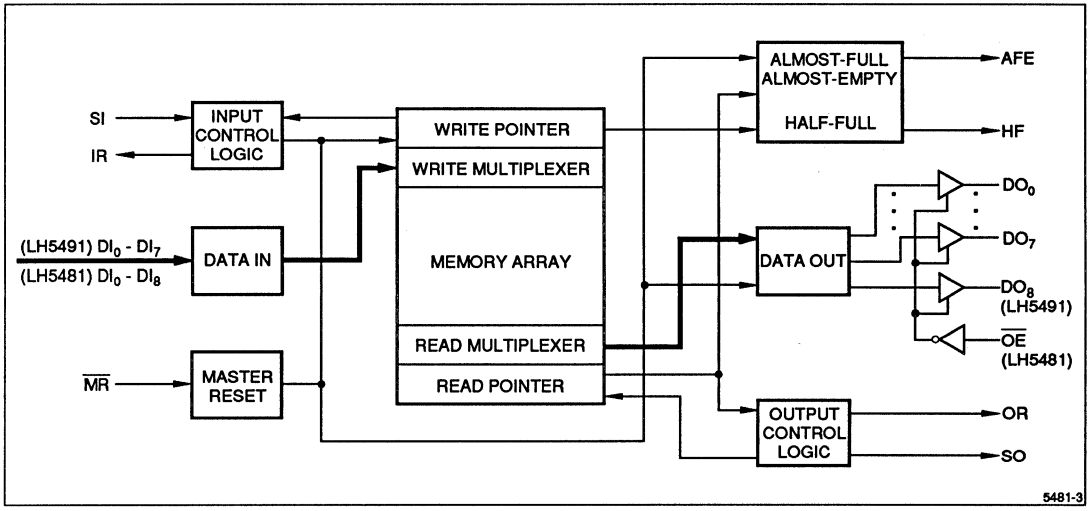


Figure 3. LH5481/91 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$DI_0 - DI_8$	Data Inputs
$DO_0 - DO_8$	Data Outputs
SI	Shift In
SO	Shift Out
IR	Input Ready
OR	Output Ready

PIN	DESCRIPTION
HF	Half-Full Flag
AFE	Almost-Full / Almost-Empty
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable (LH5481 only)
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	RATING
Vcc Range	−0.5 V to 7 V
Input Voltage Range	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 40 mA
Storage Temperature	−65°C to 150°C
DC Voltage Applied To Outputs In High-Z state	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
Static Discharge Voltage [4]	> 2000 V
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. All voltages are measured with respect to Vss.
2. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
4. Sample tested only.

OPERATING RANGE [1]

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_A	Temperature, Ambient	0.0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
Vss	Ground	0.0	0.0	V
V_{IL}	Input Low Voltage (Logic "0") [2]	−0.5	0.8	V
V_{IH}	Input High Voltage (Logic "1")	2.0	Vcc + 0.5	V

NOTES:

1. All voltages are measured with respect to Vss.
2. FIFO inputs are able to withstand a −1.5 V undershoot for less than 10 ns per cycle.

DC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range Unless Otherwise Noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current (High-Z)	V_{CC} = 5.5 V, V_{OUT} = 0 V to V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA		0.4	V
I_{CCQ}	Power Supply Quiescent Current	V_{CC} = 5.5 V, I_{OUT} = 0 mA $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$		25	mA
I_{CC}	Power Supply Current [2]	fsi = 35MHz, fso = 35MHz		45	mA

NOTES:

1. All voltages are measured with respect to Vss.
2. Icc is dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS [1]

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times (10% / 90%)	Figure 4a
Input Timing Reference Levels	1.5 V
Output Timing Reference Levels	1.5 V
Output Load for AC Timing Tests	Figure 4b

NOTE:
1. All voltages are measured with respect to Vss.

CAPACITANCE [1,2]

PARAMETER	DESCRIPTION	TEST CONDITIONS	RATING
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 4.5 V	5 pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1MHz, Vcc = 4.5 V	7 pF

NOTES:
1. All voltages are measured with respect to Vss.
2. Sample tested only.

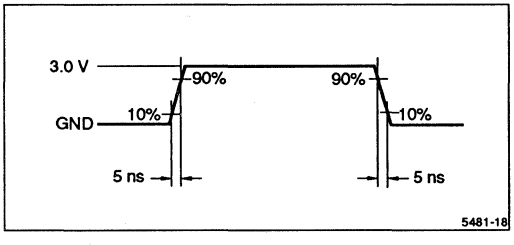


Figure 4a. Input Rise and Fall Times

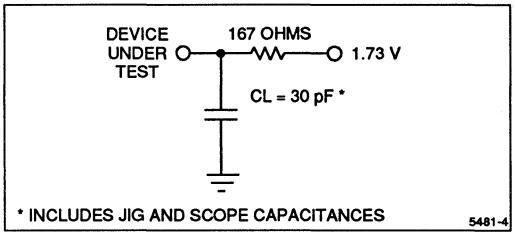


Figure 4b. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	15MHz		25MHz		35MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f_O	Operating Frequency [2]		15		25		35	MHz
t_{PHSI}	SI HIGH Time [3,8]	15		11		9		ns
t_{PLSI}	SI LOW Time [3,8]	20		15		13		ns
t_{SSI}	Data Setup to SI [4]	–1		–1		–1		ns
t_{HSI}	Data Hold from SI [4]	14		12		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW		20		18		16	ns
t_{DHIR}	Delay, SI LOW to IR HIGH		24		20		18	ns
t_{PHSO}	SO HIGH Time [3]	15		11		9		ns
t_{PLSO}	SO LOW Time [3]	20		15		13		ns
t_{DLOR}	Delay, SO HIGH to OR LOW		20		18		16	ns
t_{DHOR}	Delay, SO LOW to OR HIGH		24		20		18	ns
t_{SOR}	Data Setup to OR HIGH	–1		–1		–1		ns
t_{HSO}	Data Hold from SO LOW	0		0		0		ns
t_{FT}	Fallthrough Time		36		34		30	ns
t_{BT}	Bubblethrough Time		28		26		25	ns
t_{SIR}	Data Setup to IR [5]	5		5		5		ns
t_{HIR}	Data Hold from IR [5]	5		5		5		ns
t_{PIR}	Input Ready Pulse HIGH [8]	7		7		7		ns
t_{POR}	Output Ready Pulse HIGH [8]	7		7		7		ns
t_{DLZOE}	OE LOW to LOW Z (LH5481) [6,9]		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (LH5481) [6,9]		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH		40		40		36	ns
t_{DLHF}	SO LOW to HF LOW		40		40		36	ns
t_{DLAFE}	SO or SI LOW to AFE LOW		40		40		36	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH		40		40		36	ns
t_{PMR}	$\overline{MR}$ Pulse Width	35		35		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		25		22	ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW [7]		25		25		20	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH [7]		25		25		20	ns
t_{LXMR}	$\overline{MR}$ LOW to Output LOW [7]		25		25		20	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH		30		30		30	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW		30		30		30	ns

NOTES:

1. All time measurements performed at " AC Test Conditions".
2. $f_O = f_{SI} = f_{SO}$.
3. $t_{PHSI} + t_{PLSI} = t_{PHSO} + t_{PLSO} = 1/f_O$.
4. t_{SSI} and t_{HSI} apply when memory is not full.
5. t_{SIR} and t_{HIR} apply when memory is full and SI is HIGH.
6. High-Z transitions are referenced to the steady-state V_{OH} – 500 mV and V_{OL} + 500 mV levels on the output.
7. After reset goes LOW, all Data outputs will be at LOW level, IR goes HIGH and OR goes LOW.
8. Common dash number devices are guaranteed by design to function properly in a cascaded configuration.
9. Sample tested only.

OPERATIONAL DESCRIPTION

Unlike earlier versions of FIFOs, the LH5481 and LH5491 use dual-port Random-Access-Memory, write and read pointers, and special control logic. The write pointer is incremented by the falling edge of the Shift In (SI) signal, while the read pointer is incremented by the falling edge of the Shift Out (SO) signal. The Input Ready (IR) signal enables data writing to the FIFO. Output Ready (OR) indicates valid read information is available on the Data Output (DO) pins.

Resetting The FIFO

The FIFO Must Be Reset, upon Power-Up, using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, indicated by the Output Ready (OR) being LOW and Input Ready (IR) being HIGH. All Data Output (DO) pins will be LOW in this state. The AFE flag will be HIGH and the HF flag will be LOW.

If Shift In (SI) is HIGH, when the Master Reset ($\overline{MR}$) signal is ended, then the data on the Data Input (DI) pins will be written into the FIFO and Input Ready (IR) will return LOW until Shift In (SI) is brought LOW.

If Shift In (SI) is LOW when the Master Reset ($\overline{MR}$) is ended, then Input Ready (IR) will go HIGH, but the data on the Data Input (DI) pins will not enter the FIFO until Shift In (SI) goes HIGH.

Shifting Data In

Data Input (DI) is shifted into the FIFO on the rising edge of Shift In (SI). This loads input data into the FIFO and causes Input Ready (IR) to go LOW. When a falling edge of Shift In (SI) occurs,the write pointer increments to the next word position and Input Ready (IR) goes HIGH, indicating that the FIFO is ready to accept new data. When the FIFO is full, Input Ready (IR) remains LOW after the negative edge of Shift In (SI) signal; Shift Out (SO) action is required to unload a word of data and bring Input Ready (IR) HIGH – see Bubblethrough description.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of Shift Out (SO). The read pointer increments to the next word location and FIFO data, if present, will appear on the Data Output (DO) pins and the Output Ready (OR) signal will go HIGH. If FIFO data is not present, Output Ready (OR) will stay LOW, indicating the FIFO is empty; in this case, the last valid data read from the FIFO will remain on the Data Output (DO) pins. When the FIFO is not empty, Output Ready (OR) will go LOW after the rising edge of Shift Out (SO). The previous data remains on the Data Output (DO) pins until a falling edge of Shift Out (SO).

Fallthrough Condition

When the FIFO is empty, a data word entering through the Shift In (SI) action will follow one of two sequences.

If Shift Out (SO) is LOW, the data will propagate to the Data Output (DO) pins and Output Ready (OR) will go HIGH and stay HIGH until the next rising edge of Shift Out (SO).

If Shift Out (SO) is held HIGH while data is shifted into an empty FIFO (as occurs in depth cascading of FIFOs), data will propagate to the Data Output (DO) pins and Output Ready (OR) will pulse HIGH for a minimum time duration specified by t_{POR} and then go back LOW again. The stored word will remain on the Data Output (DO) pins. If more words are written into the FIFO, they will line up behind the first word and not appear on the Data Output (DO) pins until Shift Out (SO) has returned LOW.

Bubblethrough Condition

When the FIFO is full, Shift Out (SO) action will initiate one of the following two sequences:

If Shift In (SI) is LOW, Input Ready (IR) will go HIGH and stay HIGH until the next rising edge of Shift In (SI).

If Shift In (SI) is held HIGH while data is shifted out of a full FIFO (as occurs in depth cascading of FIFOs), Input Ready (IR) will pulse HIGH for a minimum time duration specified by t_{PIR} and then go back LOW again. Special Data Input (DI) setup and hold times (t_{SIR} and t_{HIR}, respectively) are defined for this condition.

TIMING DIAGRAMS

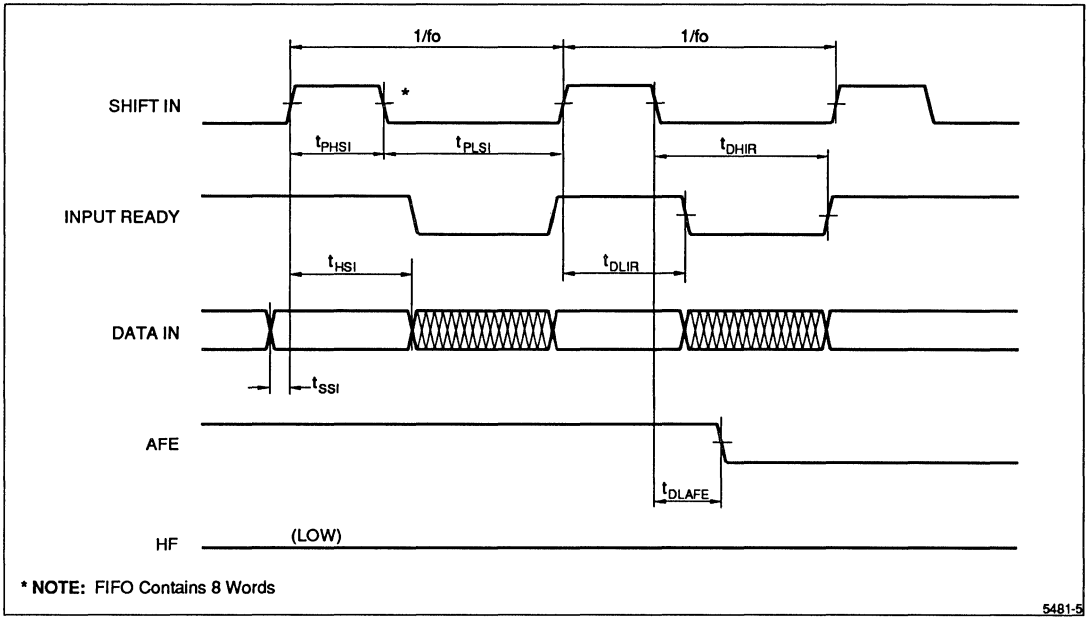


Figure 5. Data In Timing

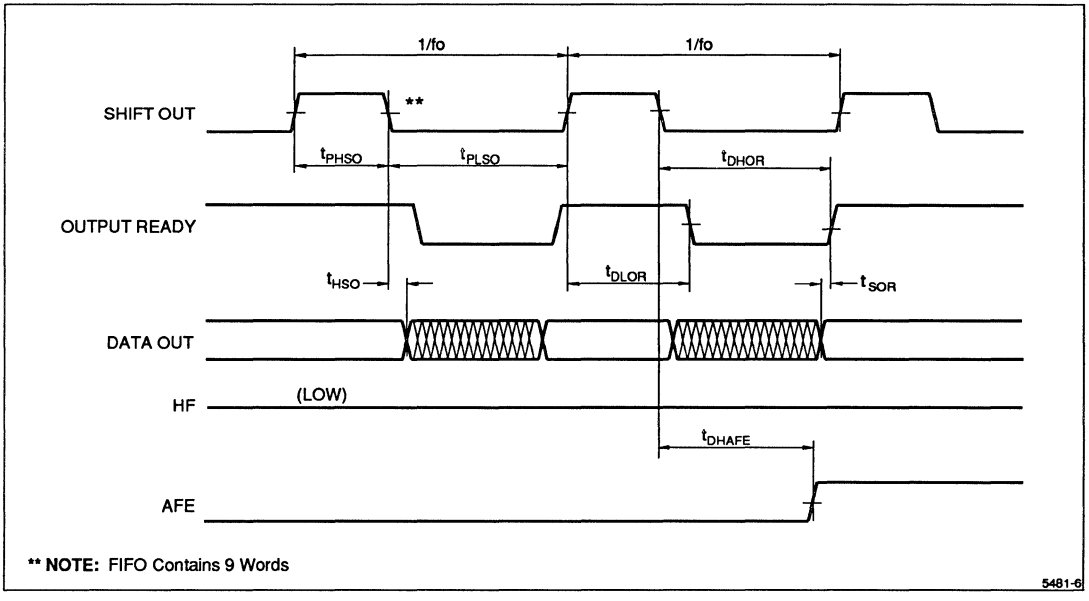


Figure 6. Data Out Timing

TIMING DIAGRAMS (cont'd)

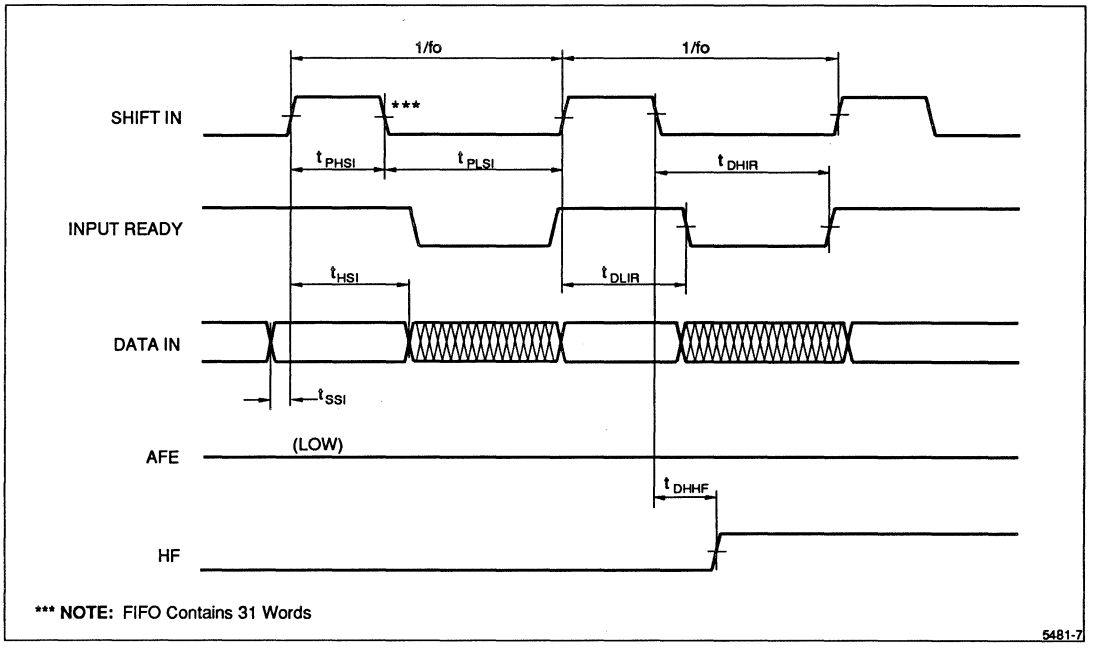


Figure 7. Data In Timing

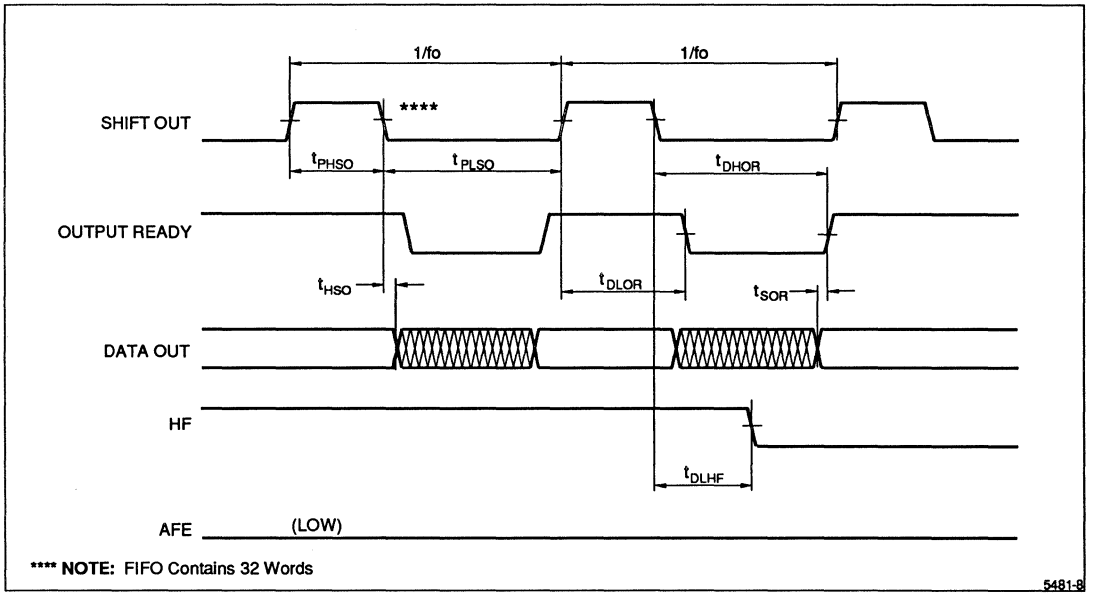


Figure 8. Data Out Timing

TIMING DIAGRAMS (cont'd)

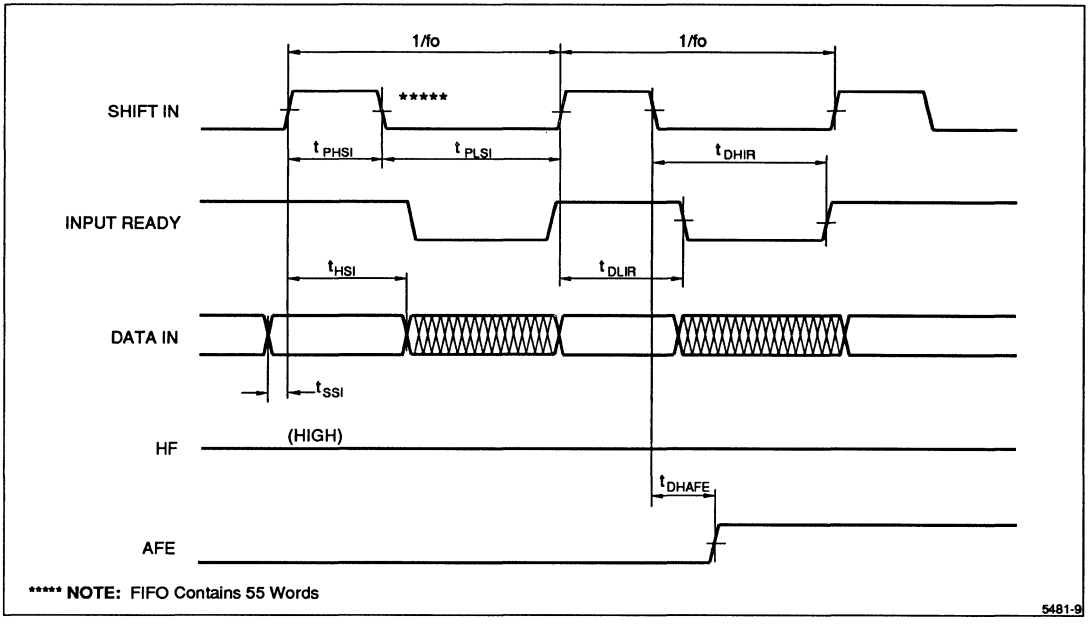


Figure 9. Data In Timing

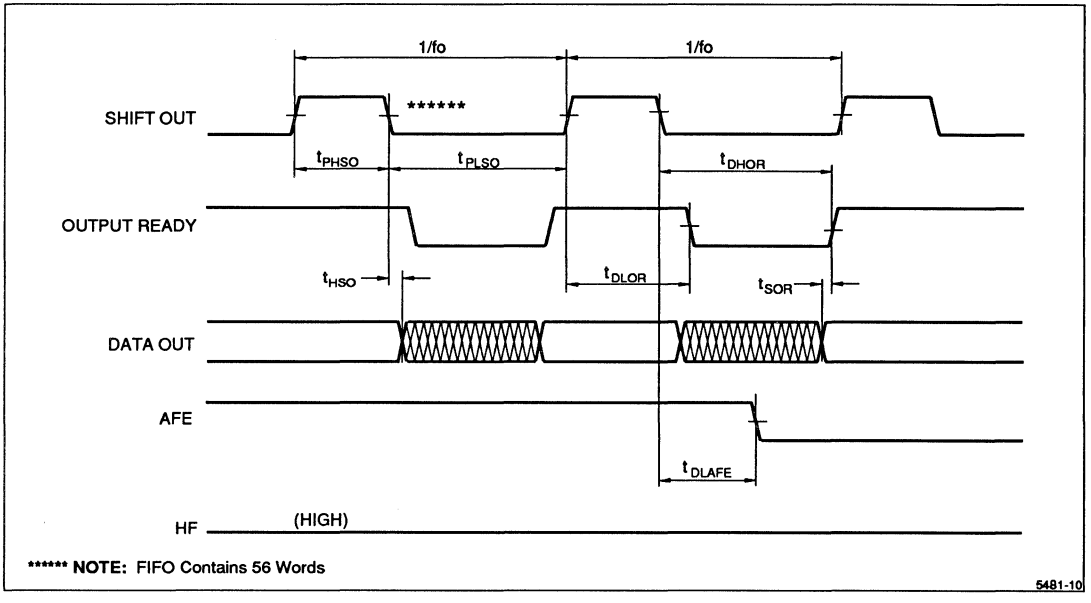


Figure 10. Data Out Timing

TIMING DIAGRAMS (cont'd)

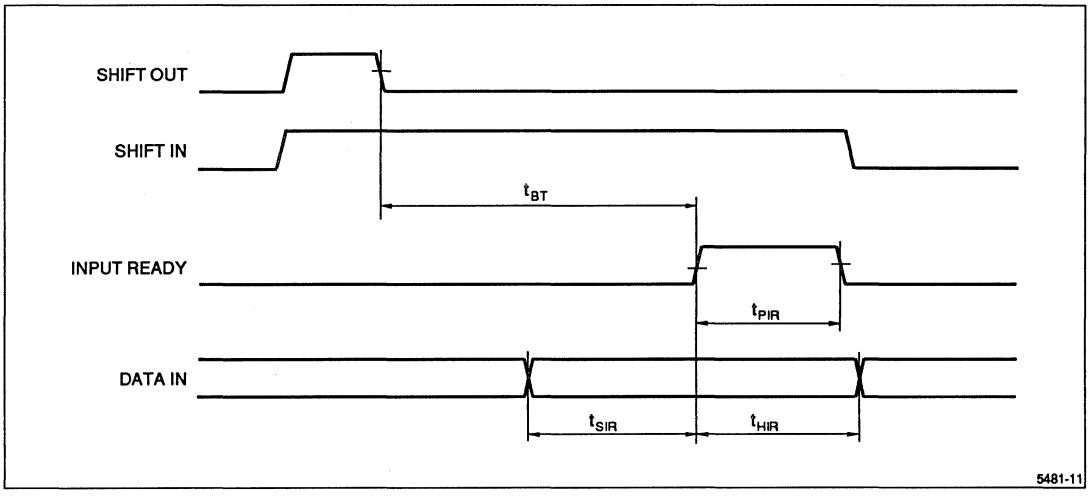


Figure 11. Bubblethrough Timing (Reading a Full FIFO)

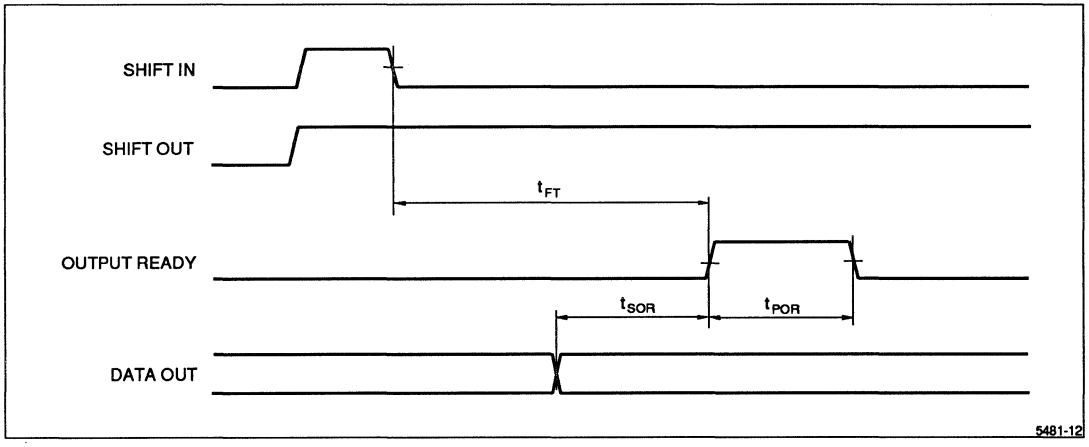


Figure 12. Fallthrough Timing (Writing an Empty FIFO)

TIMING DIAGRAMS (cont'd)

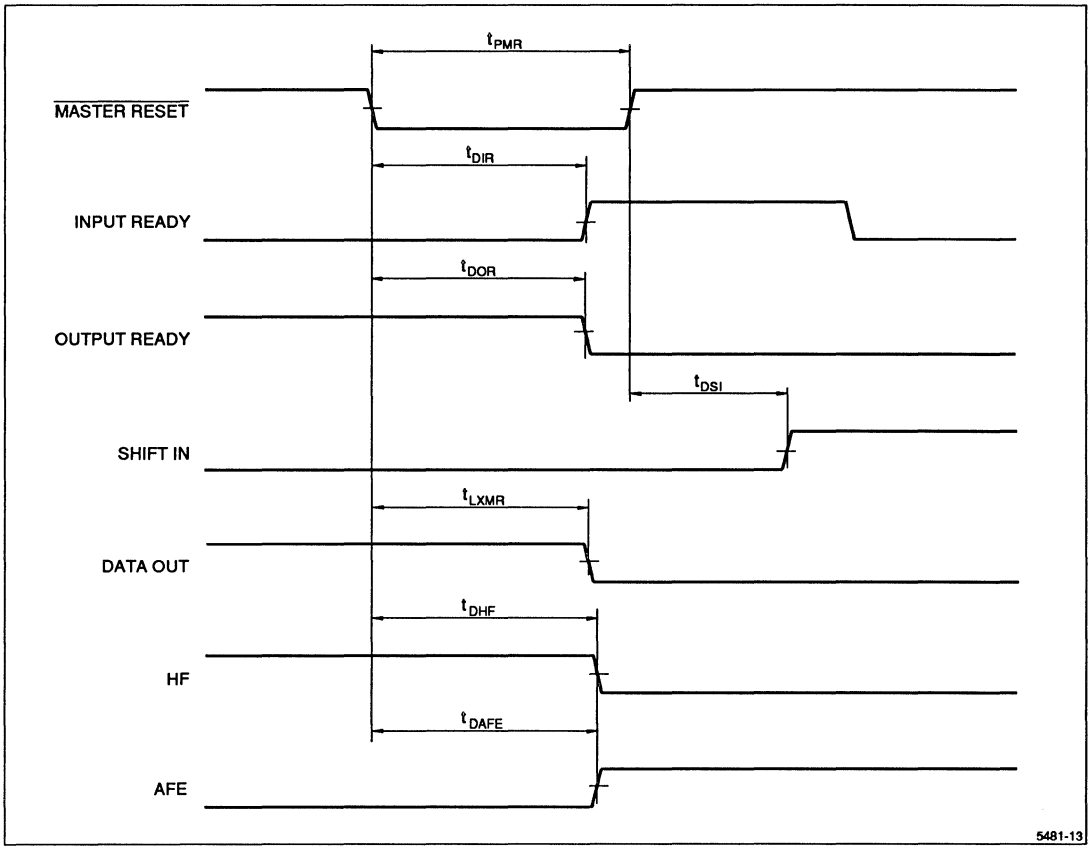


Figure 13. Master Reset Timing

TIMING DIAGRAMS (cont'd)

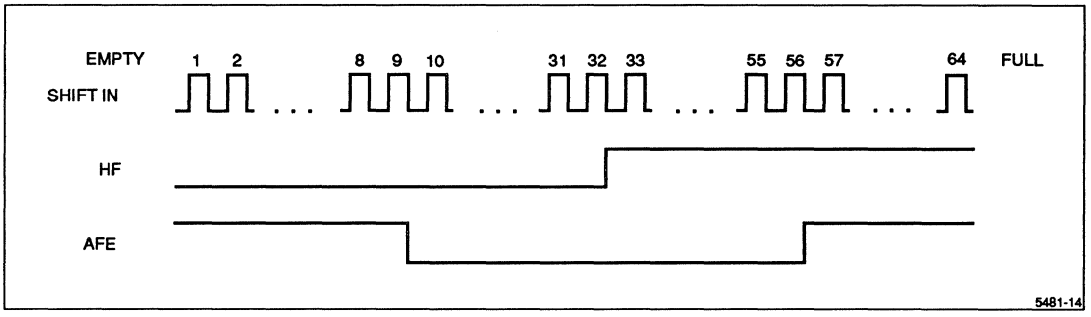


Figure 14. Shifting Words In

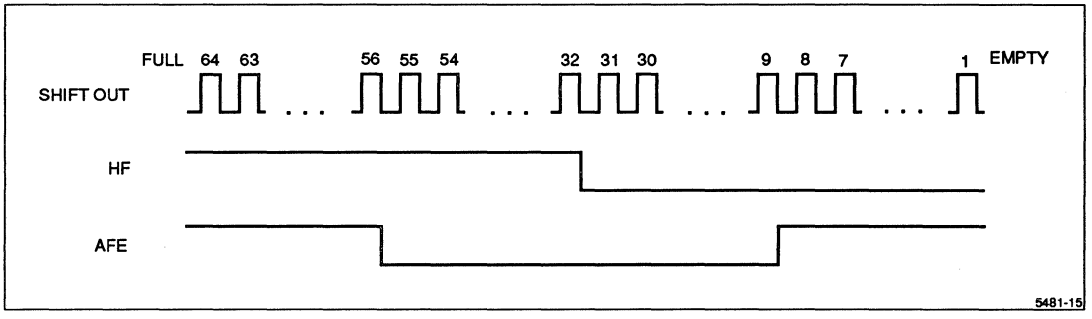


Figure 15. Shifting Words Out

FIFO EXPANSION

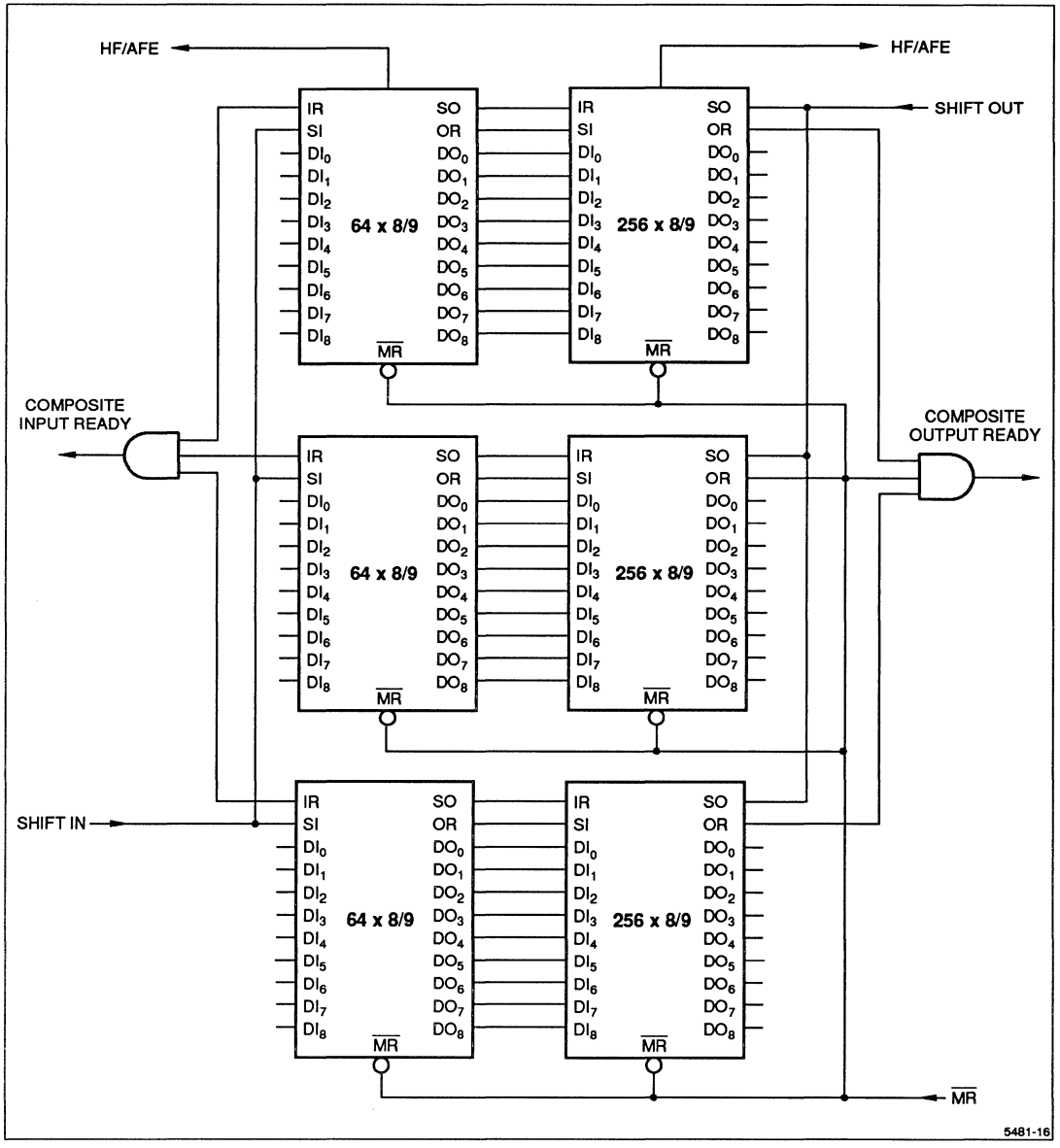


Figure 16. 320 × 24/27 Configuration Using 64 × 8/9 (LH5481/91) & 256 × 8/9 (LH5485/95) FIFOs

FIFO EXPANSION (cont'd)

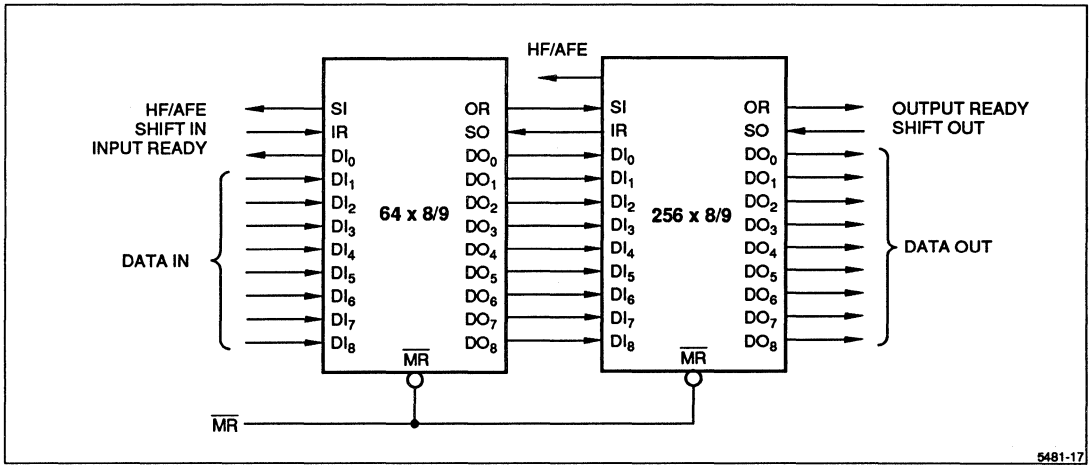


Figure 17. 128 × 8/9 Configuration

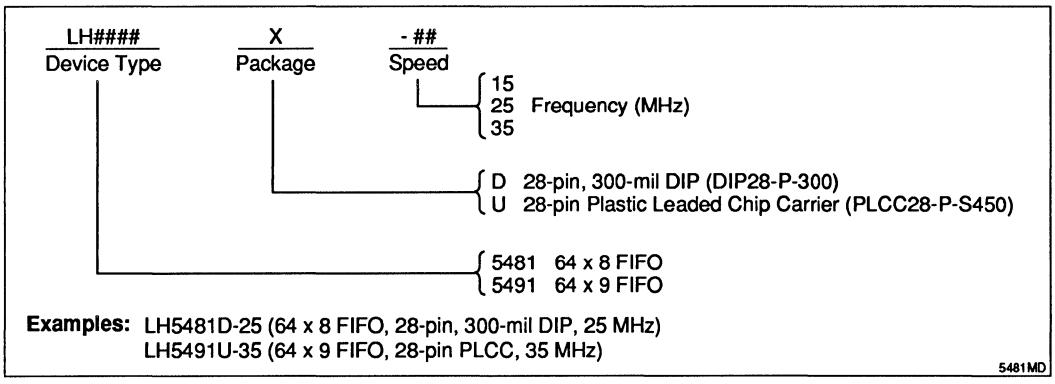
FIFOs are expandable in depth and width. However, in forming wider words, external logic is required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs. The example circuit (Figure 16) uses simple AND gates as the external IR and OR generators. More complex logic may be required if fallthrough and bubblethrough pulses are needed by the external system.

FIFOs can be easily cascaded to any desired depth as illustrated in Figure 17. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

NOTES:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. All SHARP FIFOs will cascade with other SHARP FIFOs of the same architecture (i.e., 64 × 8/9 with 64 × 8/9 or 64 × 8/9 with 256 × 8/9). However, they may not cascade with FIFOs from other manufacturers.

ORDERING INFORMATION



LH5485
LH5495

Cascadeable 256 × 8 FIFO
Cascadeable 256 × 9 FIFO

FEATURES

- Fastest 256 × 8/9 Cascadeable FIFO 35/25/15 MHz
- Expandable in Word Width & FIFO Depth
- Almost-Full / Empty & Half-Full Flags
- Fully Independent Asynchronous Inputs & Outputs
- LH5485 Output Enable forces Data Outputs to High-Impedance State
- Pin Compatible & Cascadeable with LH5481/5491 64 × 8/9 FIFOs
- Industry Standard Pinout
- 28-Pin, 300-mil DIP & 28-Pin PLCC Packaging

FUNCTIONAL DESCRIPTION

The LH5485 and LH5495 are high performance, asynchronous First-In-First-Out (FIFO) memories organized 256 words deep by 8 or 9 bits wide. The 8-bit LH5485 has an Output Enable ($\overline{OE}$) function, which can be used to force the 8 data outputs (DO) to a high-impedance state. The LH5495 has 9 data outputs.

These FIFOs accept 8 or 9-bit data at the DI data inputs. A Shift In (SI) signal writes the DI data into the FIFO. A Shift Out (SO) signal shifts stored data to the DO outputs. The Output Ready (OR) signal indicates when valid data is present on the DO outputs.

If the FIFO is full and unable to accept more DI data IR will not return high and SI pulses will be ignored. If the FIFO is empty and unable to shift data to the DO outputs, OR will not return high and SO pulses will be ignored. The Almost-Full and Almost-Empty (AFE) flag is asserted (HIGH) when the FIFO is almost-full (248 words or more) or almost-empty (8 words or less). The Half-Full (HF) flag is asserted (HIGH) when the FIFO contains 128 words or more.

Reading and writing operations may be asynchronous, allowing these FIFOs to be used as buffers between digital machines of widely different operating frequencies. The high speed makes these FIFOs ideal for high performance communication and controller applications.

PIN CONNECTIONS

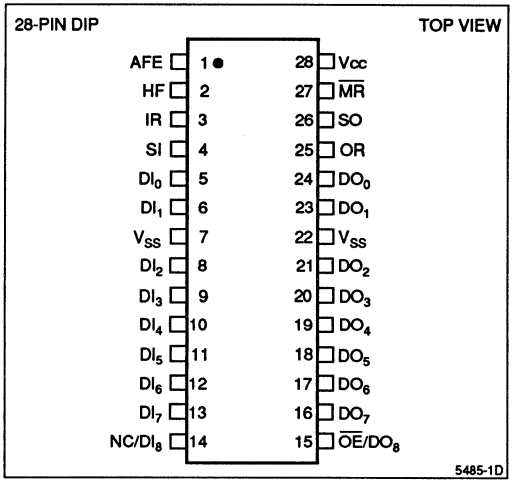


Figure 1. Pin Connections for DIP Package

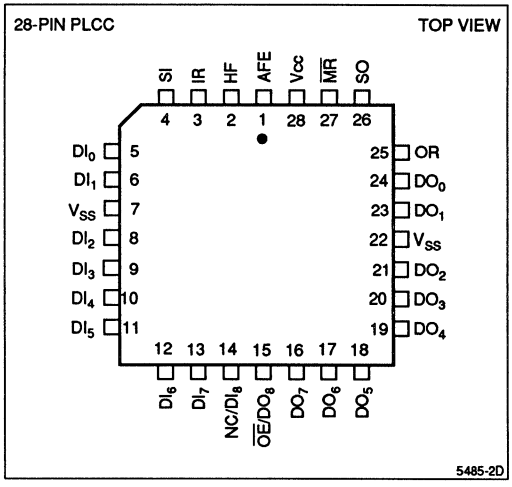


Figure 2. Pin Connections for PLCC Package

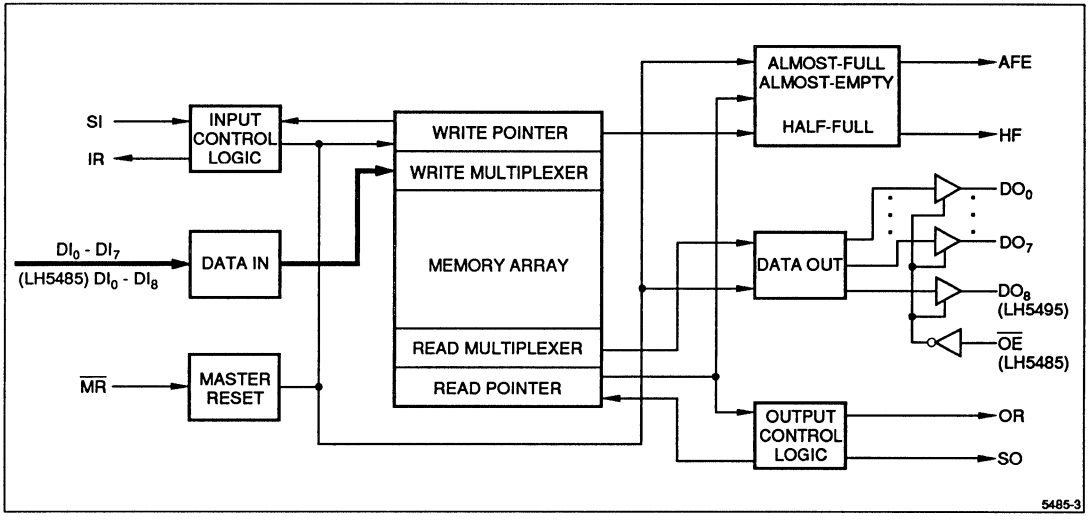


Figure 3. LH5485/95 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$DI_0 - DI_8$	Data Inputs
$DO_0 - DO_8$	Data Outputs
SI	Shift In
SO	Shift Out
IR	Input Ready
OR	Output Ready

PIN	DESCRIPTION
HF	Half-Full Flag
AFE	Almost-Full / Almost-Empty
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable (LH5485 only)
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	RATING
Vcc Range	−0.5 V to 7 V
Input Voltage Range	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 40 mA
Storage Temperature	−65°C to 150°C
DC Voltage Applied To Outputs In High-Z state	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
Static Discharge Voltage [4]	> 2000 V
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. All voltages are measured with respect to Vss.
2. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
4. Sample tested only.

OPERATING RANGE [1]

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_A	Temperature, Ambient	0.0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
Vss	Ground	0.0	0.0	V
V_{IL}	Input Low Voltage (Logic "0") [2]	−0.5	0.8	V
V_{IH}	Input High Voltage (Logic "1")	2.0	Vcc + 0.5	V

NOTES:

1. All voltages are measured with respect to Vss.
2. FIFO inputs are able to withstand a −1.5 V undershoot for less than 10 ns per cycle.

DC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range, Unless Otherwise Noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current (High-Z)	V_{CC} = 5.5 V, V_{OUT} = 0 V to V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA		0.4	V
I_{CCQ}	Power Supply Quienscent Current	V_{CC} = 5.5 V, I_{OUT} = 0 mA $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$		25	mA
I_{CC}	Power Supply Current [2]	fsi = 35 MHz, fso = 35 MHz		70	mA

NOTES:

1. All voltages are measured with respect to Vss.
2. Icc is dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS [1]

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times (10% / 90%)	Figure 4a
Input Timing Reference Levels	1.5 V
Output Timing Reference Levels	1.5 V
Output Load for AC Timing Tests	Figure 4b

NOTE:
1. All voltages are measured with respect to Vss.

CAPACITANCE [1,2]

PARAMETER	DESCRIPTION	TEST CONDITIONS	RATING
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, Vcc = 4.5 V	5 pF
C_{OUT}	Output Capacitance	TA = 25°C, f = 1MHz, Vcc = 4.5 V	7 pF

NOTES:
1. All voltages are measured with respect to Vss.
2. Sample tested only.

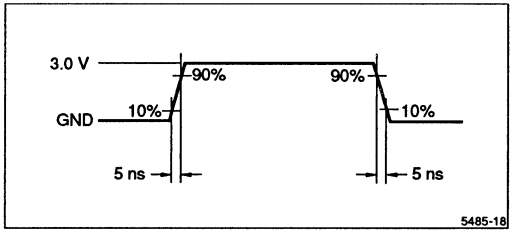


Figure 4a. Input Rise and Fall Times

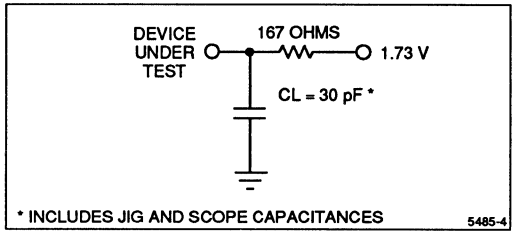


Figure 4b. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	15MHz		25MHz		35MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_O	Operating Frequency [2]		15		25		35	MHz
t_{PHSI}	SI HIGH Time [3,8]	15		11		9		ns
t_{PLSI}	SI LOW Time [3,8]	20		15		13		ns
t_{SSI}	Data Setup to SI [4]	–1		–1		–1		ns
t_{HSI}	Data Hold from SI [4]	14		12		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW		20		18		16	ns
t_{DHIR}	Delay, SI LOW to IR HIGH		24		20		18	ns
t_{PHSO}	SO HIGH Time [3]	15		11		9		ns
t_{PLSO}	SO LOW Time [3]	20		15		13		ns
t_{DLOR}	Delay, SO HIGH to OR LOW		20		18		16	ns
t_{DHOR}	Delay, SO LOW to OR HIGH		24		20		18	ns
t_{SOR}	Data Setup to OR HIGH	–1		–1		–1		ns
t_{HSO}	Data Hold from SO LOW	0		0		0		ns
t_{FT}	Fallthrough Time		40		34		30	ns
t_{BT}	Bubblethrough Time		28		26		25	ns
t_{SIR}	Data Setup to IR [5]	5		5		5		ns
t_{HIR}	Data Hold from IR [5]	5		5		5		ns
t_{PIR}	Input Ready Pulse HIGH [8]	7		7		7		ns
t_{POR}	Output Ready Pulse HIGH [8]	7		7		7		ns
t_{DLZOE}	OE LOW to LOW Z (LH5485) [6,9]		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (LH5485) [6,9]		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH		45		45		40	ns
t_{DLHF}	SO LOW to HF LOW		45		45		40	ns
t_{DLAFE}	SO or SI LOW to AFE LOW		45		45		40	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH		45		45		40	ns
t_{PMR}	$\overline{MR}$ Pulse Width	35		35		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		25		22	ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW [7]		25		25		20	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH [7]		25		25		20	ns
t_{LXMR}	$\overline{MR}$ LOW to Output LOW [7]		25		25		20	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH		30		30		30	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW		30		30		30	ns

NOTES:

1. All time measurements performed at "AC Test Conditions".
2. $f_O = f_{SI} = f_{SO}$.
3. $t_{PHSI} + t_{PLSI} = t_{PHSO} + t_{PLSO} = 1/f_O$.
4. t_{SSI} and t_{HSI} apply when memory is not full.
5. t_{SIR} and t_{HIR} apply when memory is full and SI is HIGH.
6. High-Z transitions are referenced to the steady-state V_{OH} – 500 mV and V_{OL} + 500 mV levels on the output.
7. After reset goes LOW, all Data outputs will be at LOW level, IR goes HIGH and OR goes LOW.
8. Common dash number devices are quaranteed by design to function properly in a cascaded configuration.
9. Sample tested only.

OPERATIONAL DESCRIPTION

Unlike earlier versions of FIFOs, the LH5485 and LH5495 use dual-port Random-Access-Memory, write and read pointers, and special control logic. The write pointer is incremented by the falling edge of the Shift In (SI) signal, while the read pointer is incremented by the falling edge of the Shift Out (SO) signal. The Input Ready (IR) signal enables data writing to the FIFO, while Output Ready (OR) indicates valid read information is available on the Data Output (DO) pins.

Resetting the FIFO

The FIFO must be reset, upon Power-Up, using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, indicated by the Output Ready (OR) being LOW and Input Ready (IR) being HIGH. All Data Output (DO) pins will be LOW in this state. The AFE flag will be HIGH and the HF flag will be LOW.

If Shift In (SI) is HIGH, when the Master Reset ($\overline{MR}$) signal is ended, then the data on the Data Input (DI) pins will be written into the FIFO and Input Ready (IR) will return LOW until Shift In (SI) is brought LOW.

If Shift In (SI) is LOW when the Master Reset ($\overline{MR}$) is ended, then Input Ready (IR) will go HIGH, but the data on the Data Input (DI) pins will not enter the FIFO until Shift In (SI) goes HIGH.

Shifting Data In

Data Input (DI) is shifted into the FIFO on the rising edge of Shift In (SI). This loads input data into the FIFO and causes Input Ready (IR) to go LOW. When a falling edge of Shift In (SI) occurs, the write pointer increments to the next word position and Input Ready (IR) goes HIGH, indicating that the FIFO is ready to accept new data. When the FIFO is full, Input Ready (IR) remains LOW after the negative edge of Shift In (SI) signal; Shift Out (SO) action is required to unload a word of data and bring Input Ready (IR) HIGH – see Bubblethrough description.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of Shift Out (SO). The read pointer increments to the next word location and FIFO data, if present, will appear on the Data Output (DO) pins and the Output Ready (OR) signal will go HIGH. If FIFO data is not present, Output Ready (OR) will stay LOW, indicating the FIFO is empty; in this case, the last valid data read from the FIFO will remain on the Data Output (DO) pins. When the FIFO is not empty, Output Ready (OR) will go LOW after the rising edge of Shift Out (SO). The previous data remains on the Data Output (DO) pins until a falling edge of Shift Out (SO).

Fallthrough Condition

When the FIFO is empty, a data word entering through the Shift In (SI) action will follow one of two sequences.

If Shift Out (SO) is LOW, the data will propagate to the Data Output (DO) pins and Output Ready (OR) will go HIGH and stay HIGH until the next rising edge of Shift Out (SO).

If Shift Out (SO) is held HIGH while data is shifted into an empty FIFO (as occurs in depth cascading of FIFOs), data will propagate to the Data Output (DO) pins and Output Ready (OR) will pulse HIGH for a minimum time duration specified by t_{POR} and then go back LOW again. The stored word will remain on the Data Output (DO) pins. If more words are written into the FIFO, they will line up behind the first word and not appear on the Data Output (DO) pins until Shift Out (SO) has returned LOW.

Bubblethrough Condition

When the FIFO is full, Shift Out (SO) action will initiate one of the following two sequences.

If Shift In (SI) is LOW, Input Ready (IR) will go HIGH and stay HIGH until the next rising edge of Shift In (SI).

If Shift In (SI) is held HIGH while data is shifted out of a full FIFO (as occurs in depth cascading of FIFOs), Input Ready (IR) will pulse HIGH for a minimum time duration specified by t_{PIR} and then go back LOW again. Special Data Input (DI) setup and hold times (t_{SIR} and t_{HIR}, respectively) are defined for this condition.

TIMING DIAGRAMS

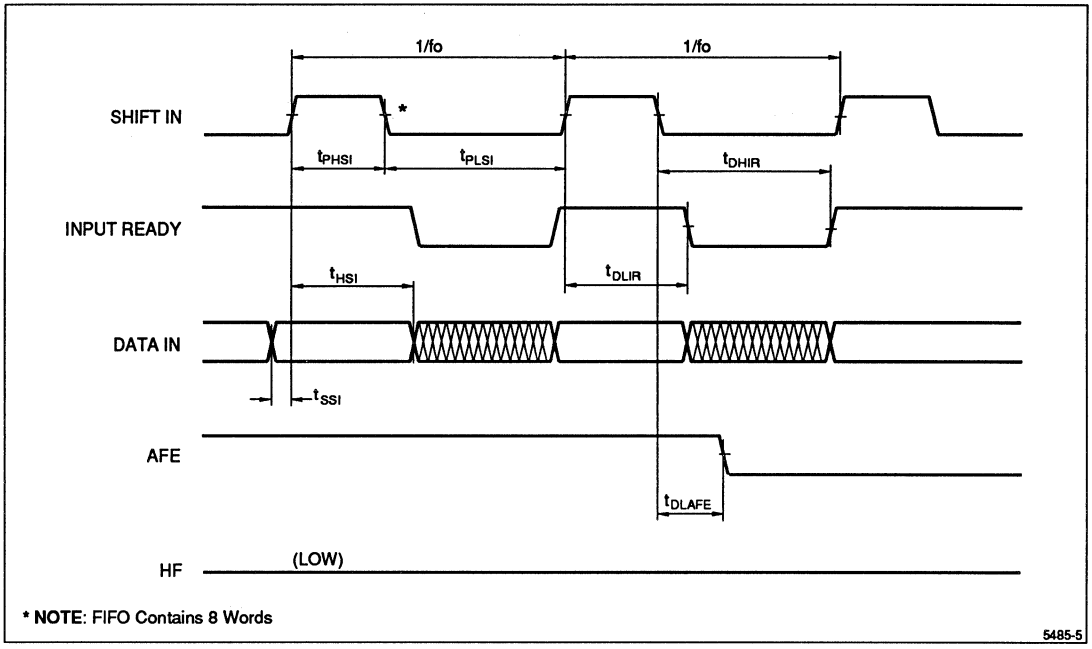


Figure 5. Data In Timing

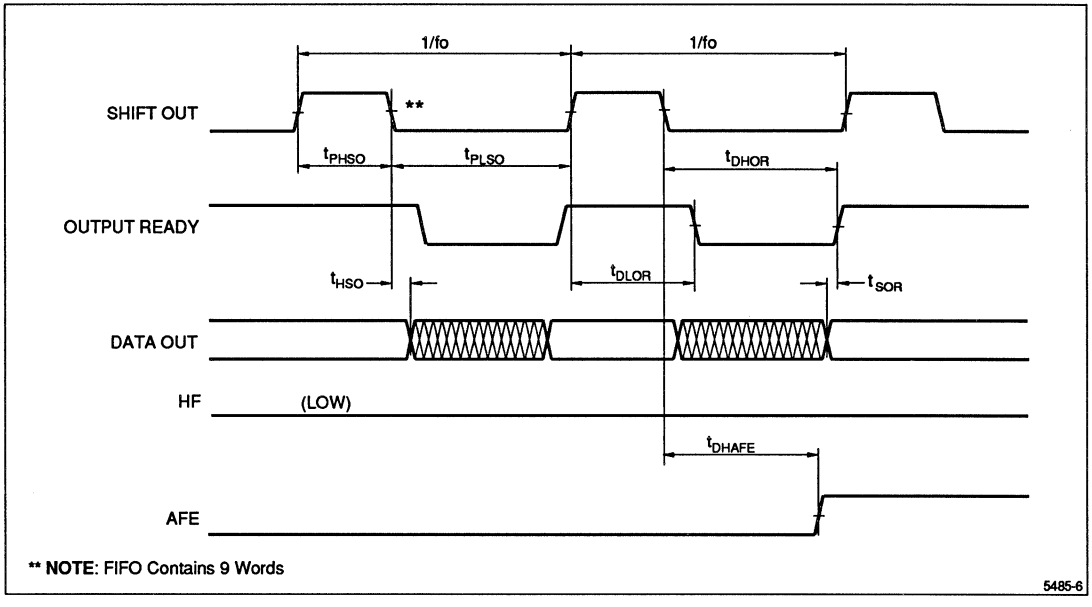


Figure 6. Data Out Timing

TIMING DIAGRAMS (cont'd)

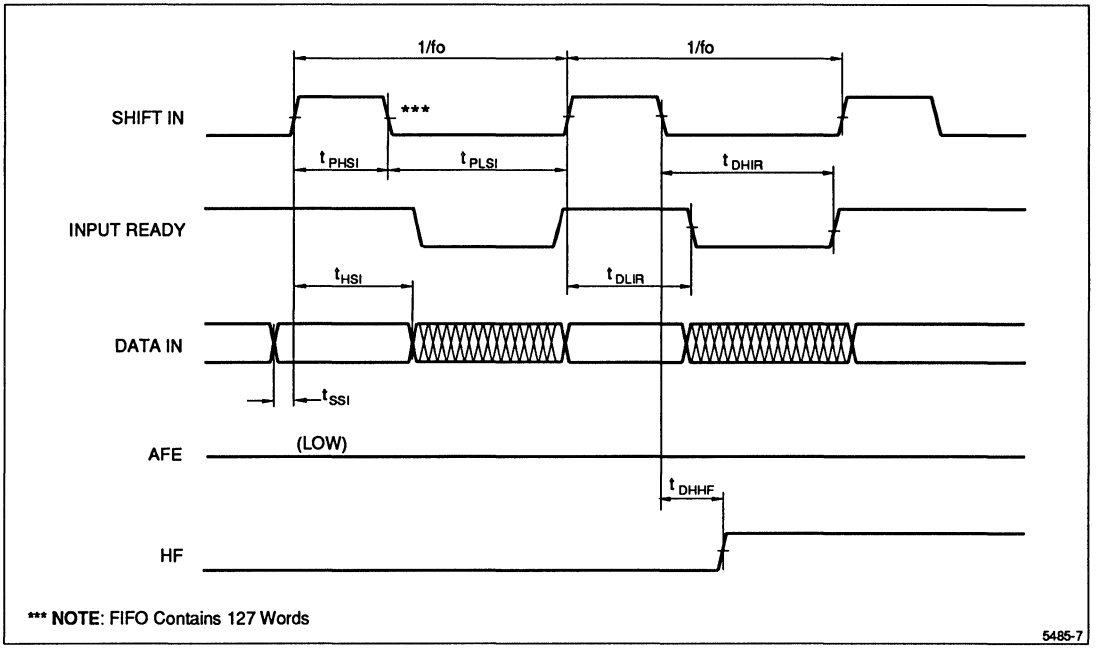


Figure 7. Data In Timing

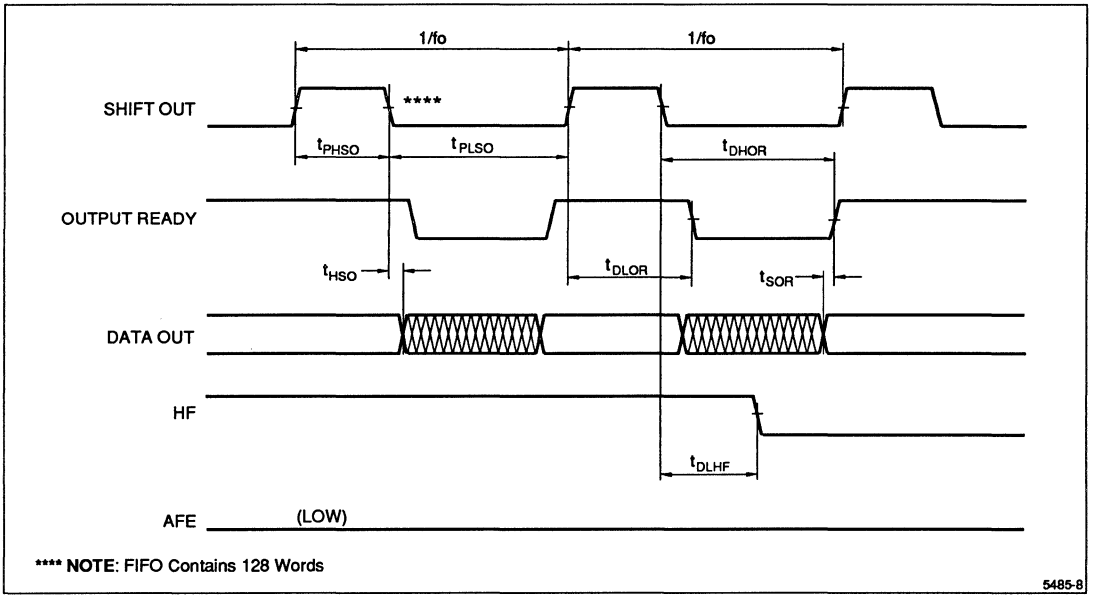


Figure 8. Data Out Timing

TIMING DIAGRAMS (cont'd)

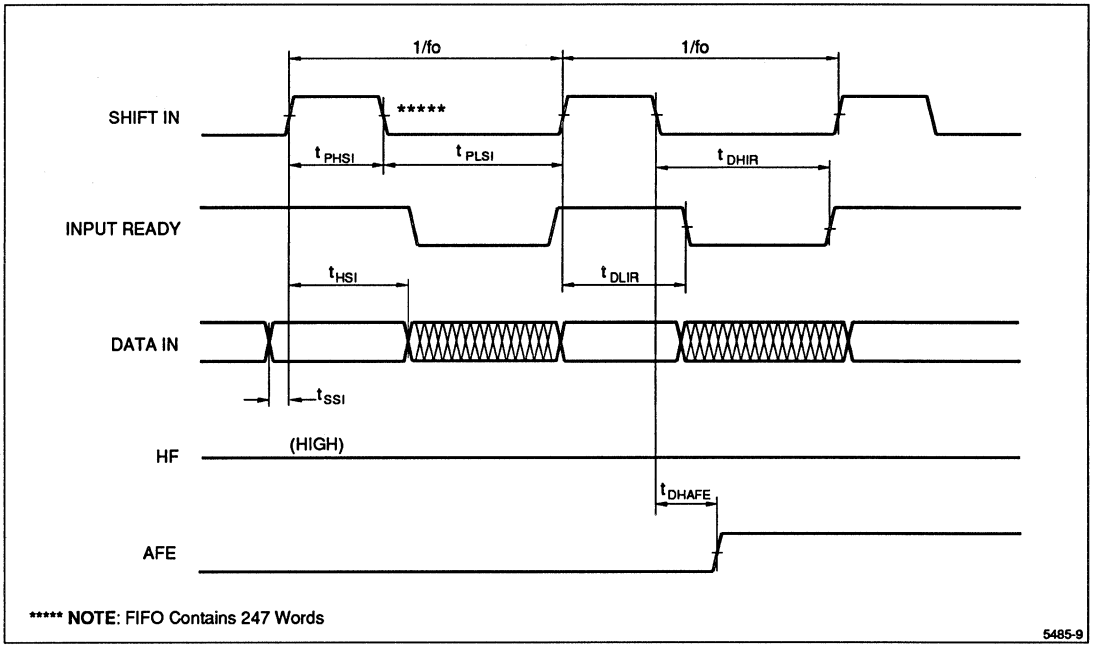


Figure 9. Data In Timing

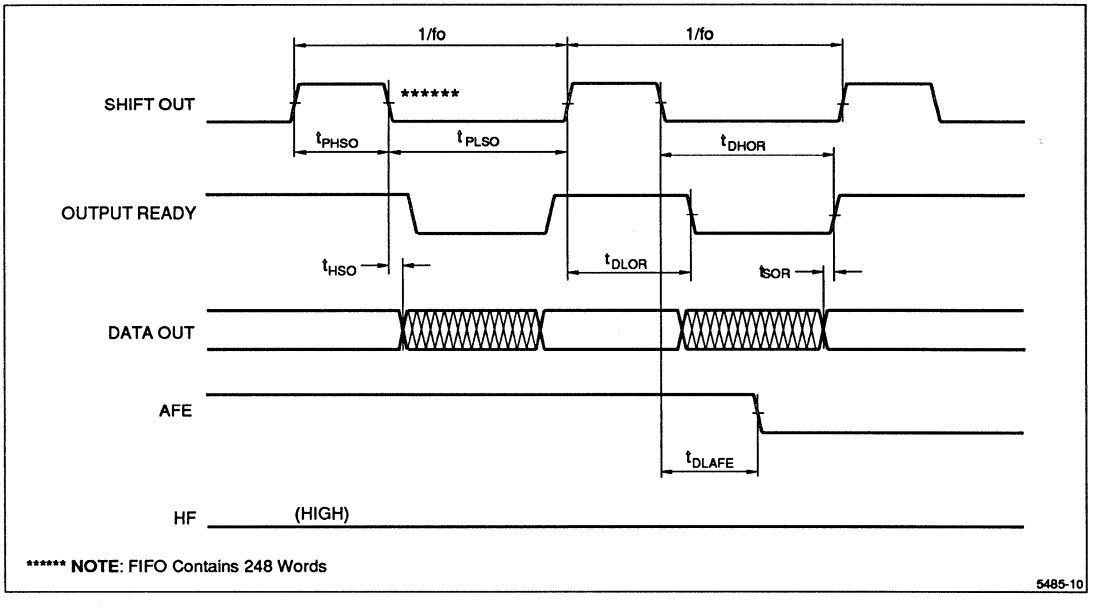


Figure 10. Data Out Timing

TIMING DIAGRAMS (cont'd)

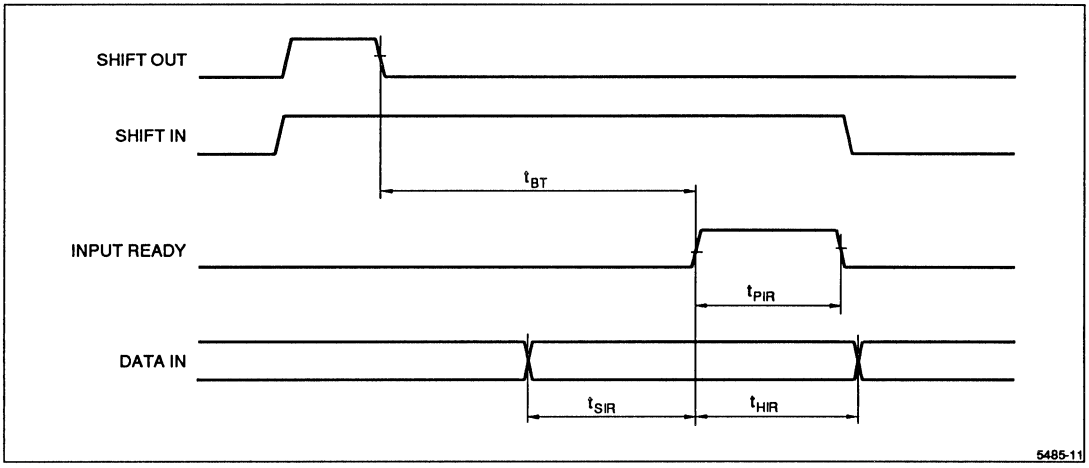


Figure 11. Bubblethrough Timing (Reading a Full FIFO)

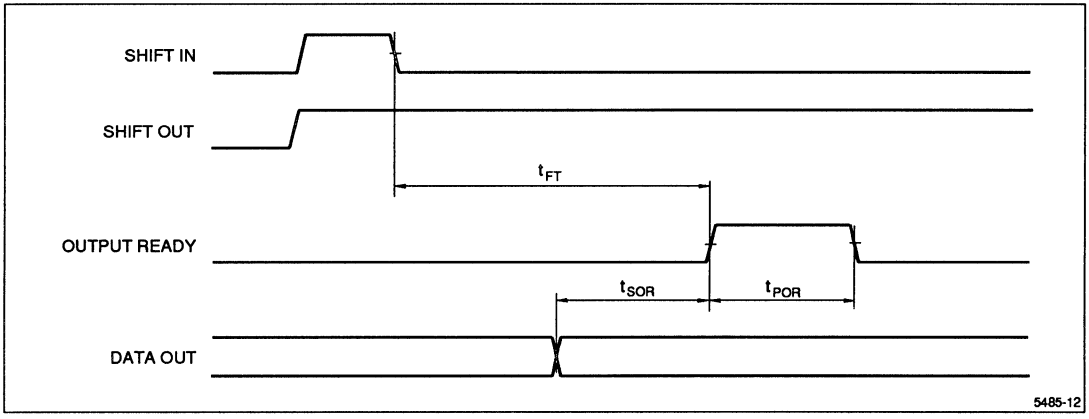


Figure 12. Fallthrough Timing (Writing an Empty FIFO)

TIMING DIAGRAMS (cont'd)

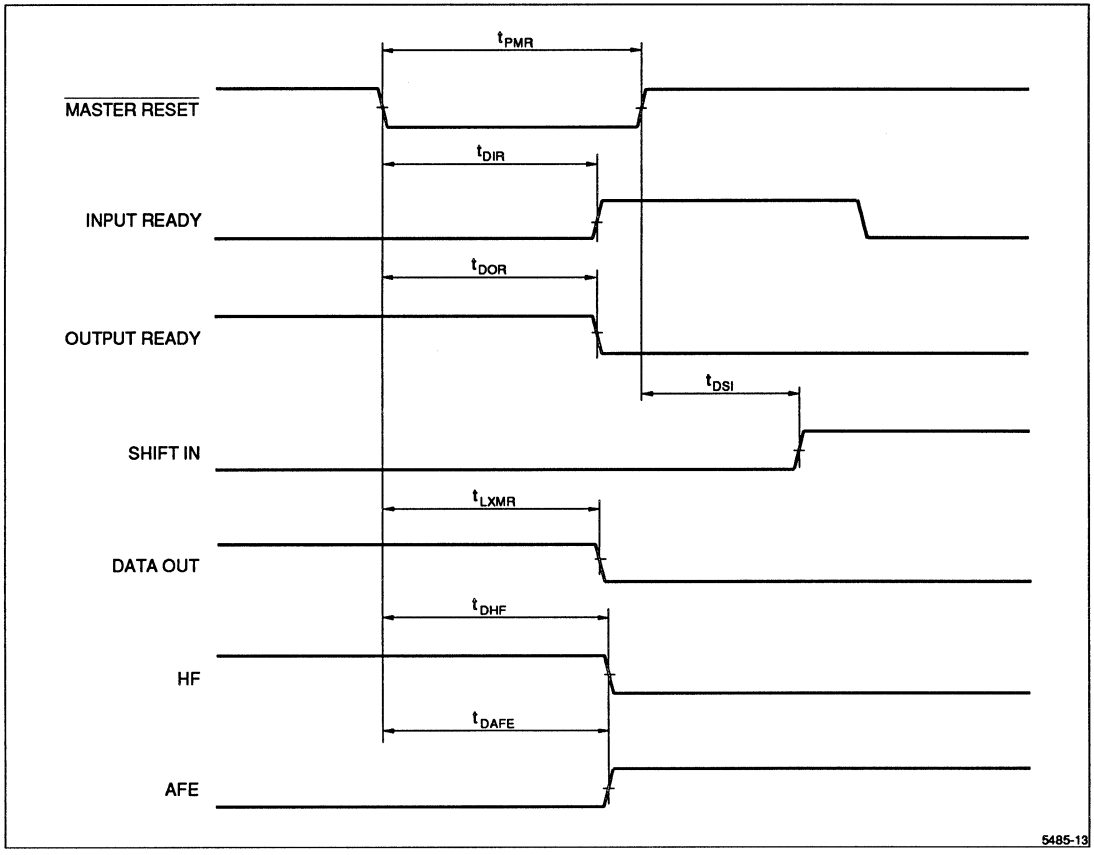


Figure 13. Master Reset Timing

TIMING DIAGRAMS (cont'd)

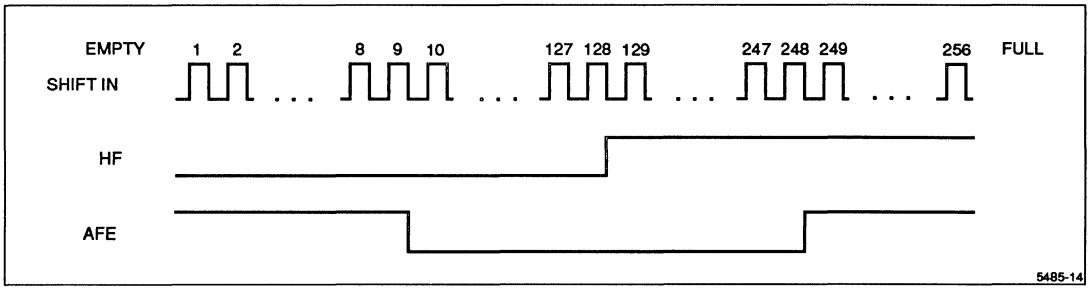


Figure 14. Shifting Words In

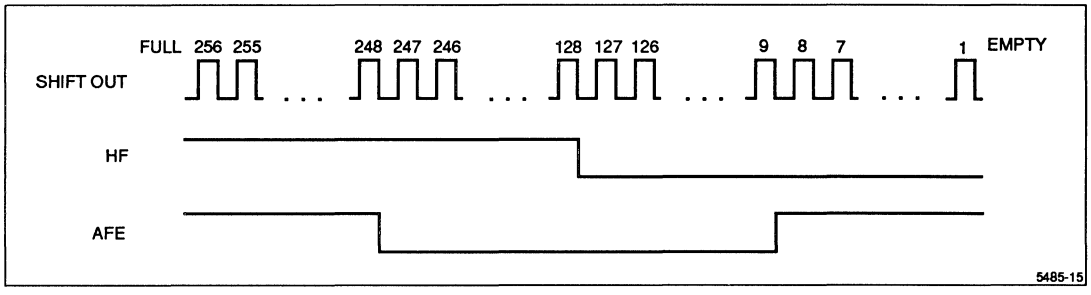


Figure 15. Shifting Words Out

FIFO EXPANSION

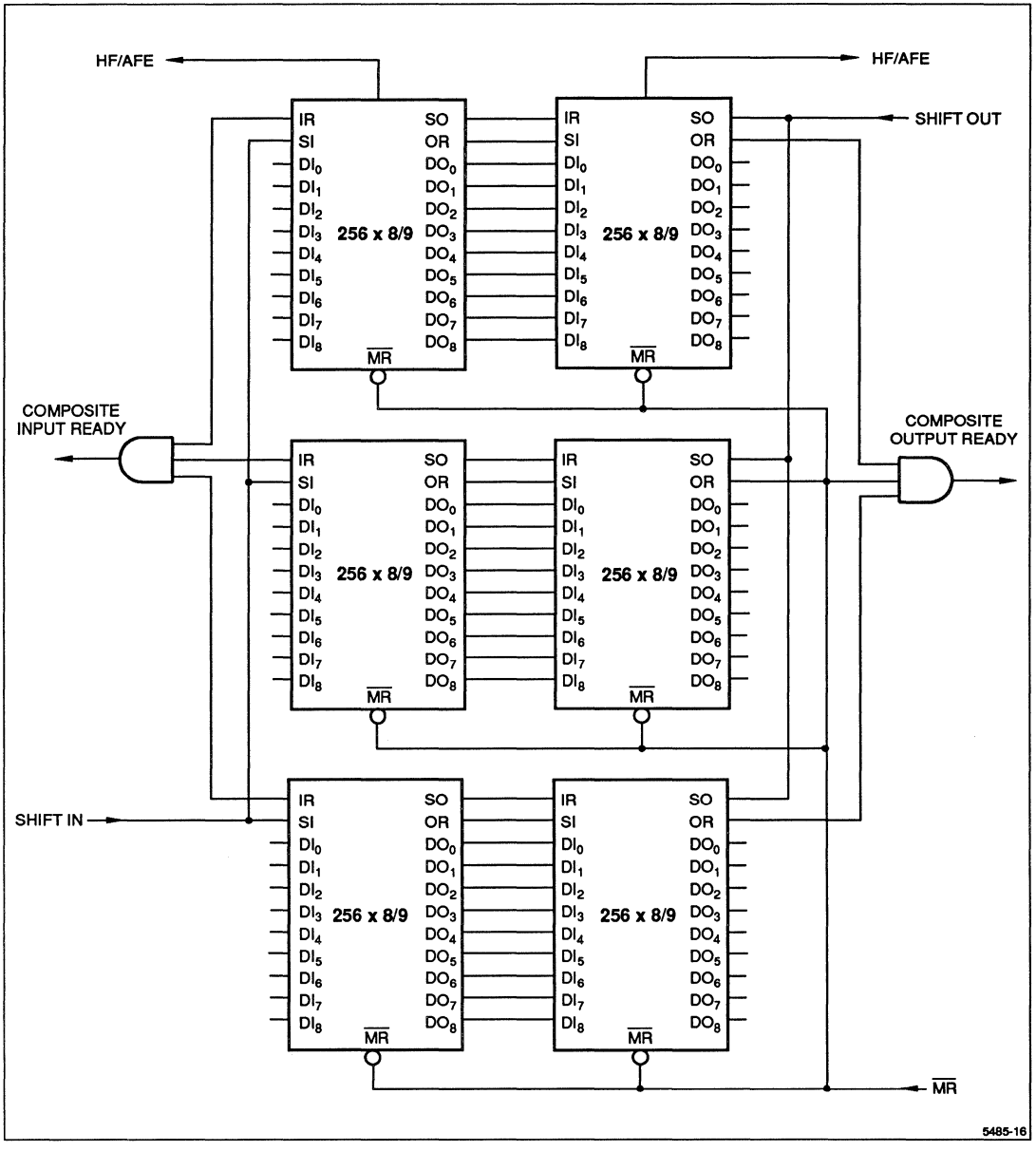


Figure 16. 512 × 24/27 Configuration Using 256 × 8/9 (LH5485/95) FIFOs.

FIFO EXPANSION (cont'd)

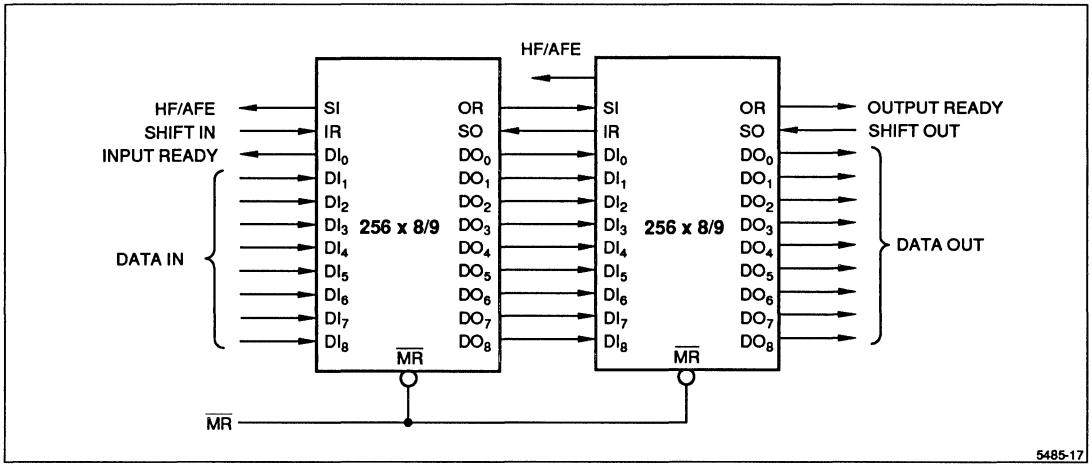


Figure 17. 512 × 8/9 Configuration

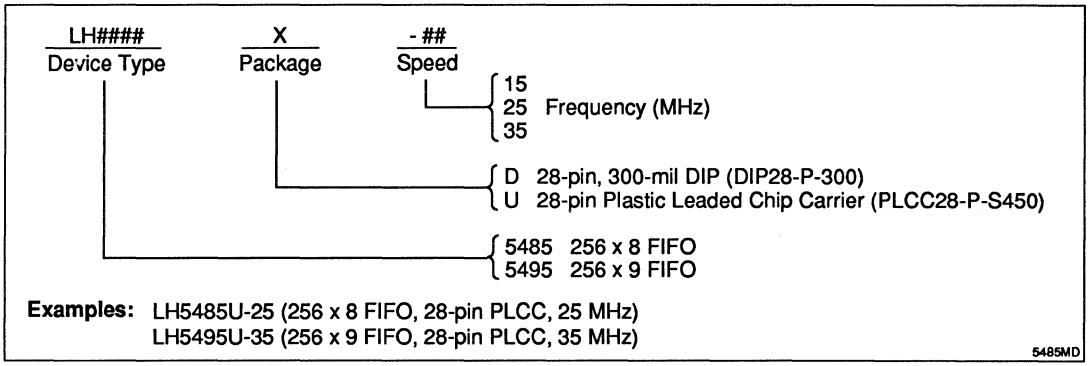
FIFOs are expandable in depth and width. However, in forming wider words, external logic is required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs. The example circuit in Figure 16 uses simple AND gates as the external IR and OR generators. More complex logic may be required if fallthrough and bubblethrough pulses are needed by the external system.

FIFOs can easily cascaded to any desired depth as illustrated in Figure 17. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

NOTES:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. All SHARP FIFOs will cascade with other SHARP FIFOs of the same architecture (i.e., 64 × 8/9 with 64 × 8/9 or 64 × 8/9 with 256 × 8/9). However, they may not cascade with FIFOs from other manufacturers.

ORDERING INFORMATION



LH5496

CMOS 512 × 9 FIFO

FEATURES

- Fast Access Times:
  15/20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable-in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil PDIP,
  28-Pin, 600-mil PDIP or
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7201

FUNCTIONAL DESCRIPTION

The LH5496 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic provides for unlimited expansion in both word size and depth.

Read and write operations automatically access sequential locations in memory in that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

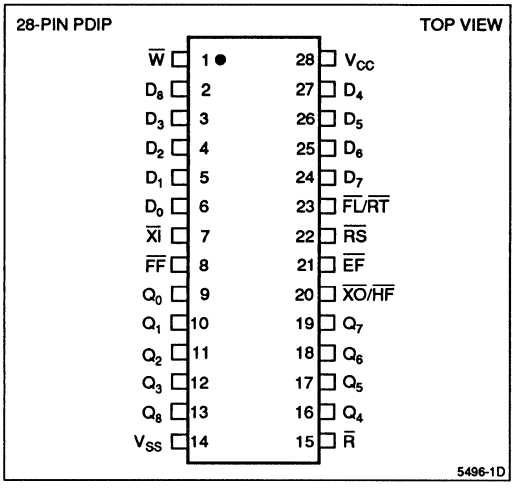


Figure 1. Pin Connections for PDIP Package

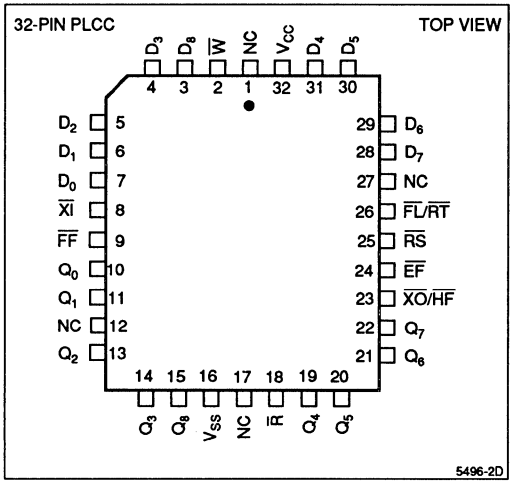


Figure 2. Pin Connections for PLCC Package

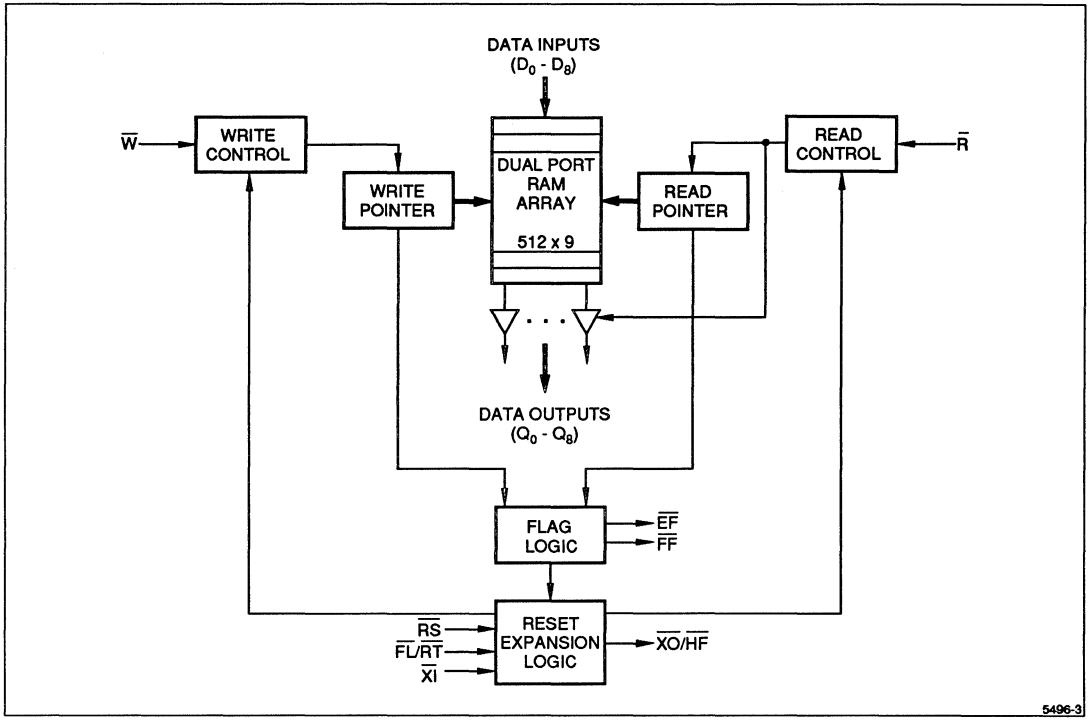


Figure 3. LH5496 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Control
$\overline{R}$	Read Control
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL}/\overline{RT}$	First Load, Retransmit
$\overline{RS}$	Reset
Vcc	Positive Power Supply
Vss	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied To Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a device stress rating for transient conditions only. Functional operation at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
V_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2 V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

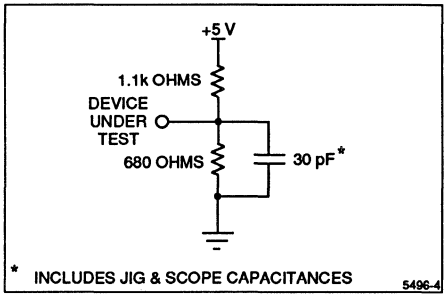


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read Low [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write High [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read High [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read High to $\overline{RS}$ High	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write High to $\overline{RS}$ High	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
FLAG TIMING																
t_{EFL}	Reset to Empty Flag Low	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset to Half & Full Flag High	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read Low to Empty Flag Low	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read High to Half-Full Flag High	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out Low	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out High	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The Device is reset whenever the RESET pin ($\overline{RS}$) is taken to a low state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in SINGLE mode or DEPTH EXPANSION mode. A reset pulse is required when the device is first powered up. The READ ($\overline{R}$) and WRITE ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a high state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the WRITE ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the FULL flag pin is HIGH). Writes may occur independently of any ongoing read opertations.

At the falling edge of the first write after the memory is half filled, the HALF flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The HALF flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The FULL flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The FULL flag will inhibit further writes until cleared by a valid read. The FULL flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the READ ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes high, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The EMPTY flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the READ ($\overline{R}$) pin is brought low while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the EMPTY flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains low, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the WRITE ($\overline{W}$) pin is brought low while the FIFO is full, and held low in anticipation of a read cycle. At the end of the read cycle, the FULL flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held low. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ low. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 512 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

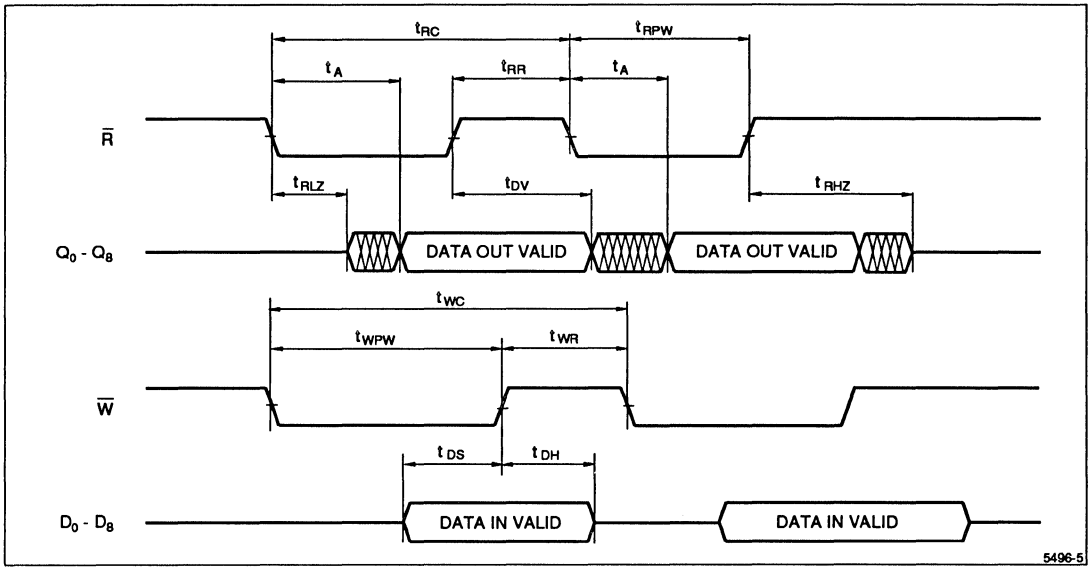


Figure 5. Asynchronous Write and Read Operation

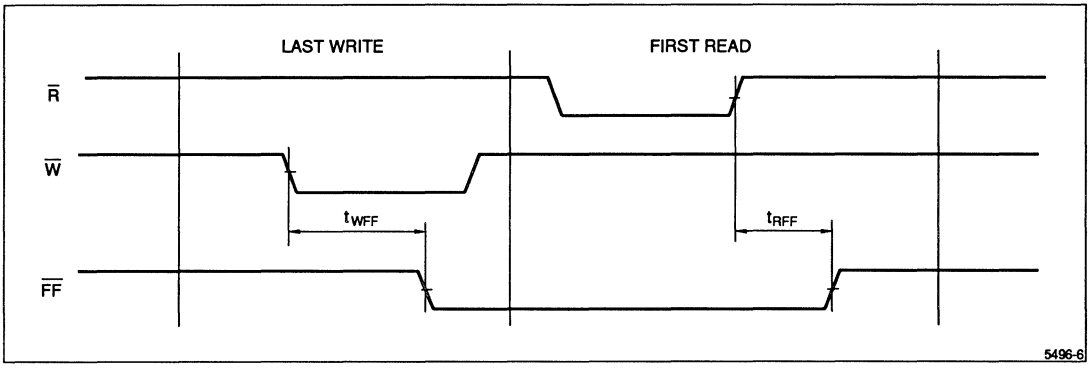


Figure 6. Full Flag from Last Write to First Read

TIMING DIAGRAMS (cont'd)

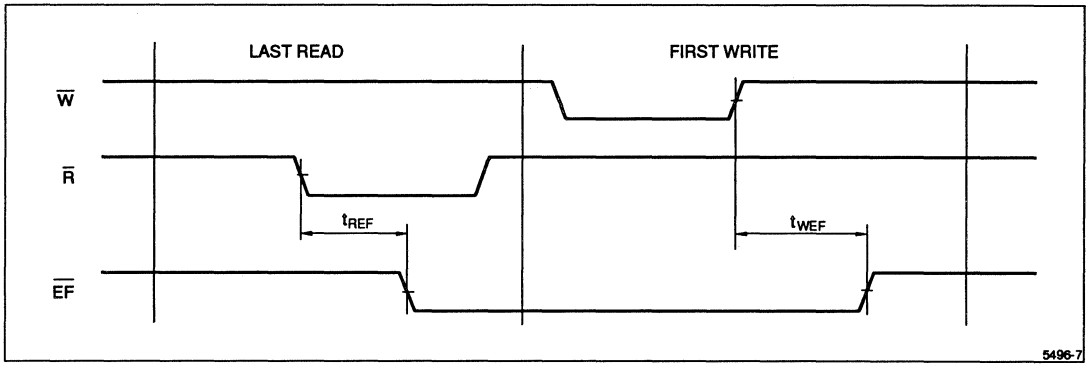


Figure 7. Empty Flag from Last Read to First Write

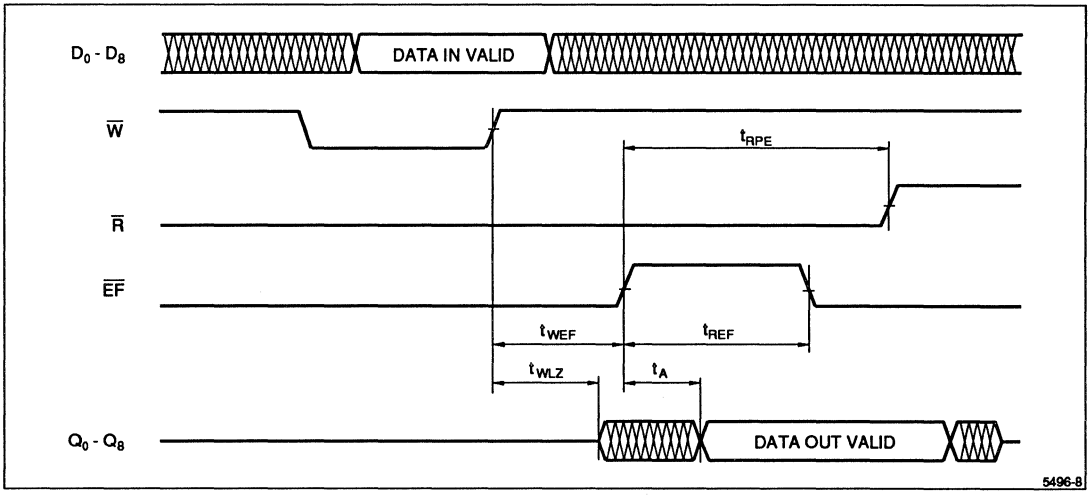


Figure 8. Read Data Flow-Through

TIMING DIAGRAMS (cont'd)

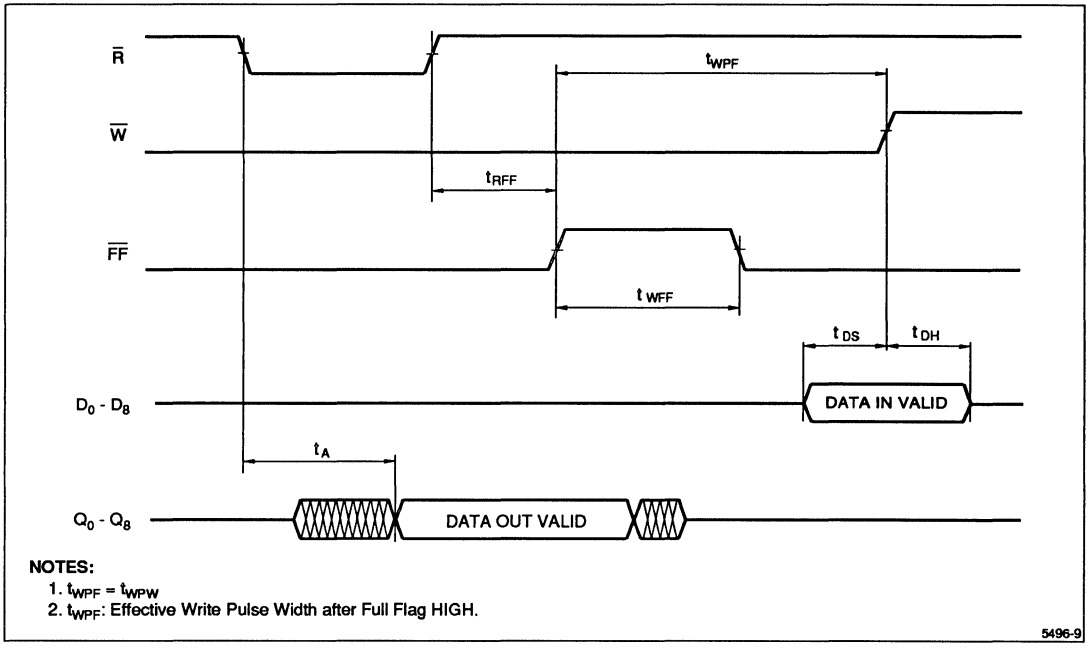


Figure 9. Write Data Flow-Through

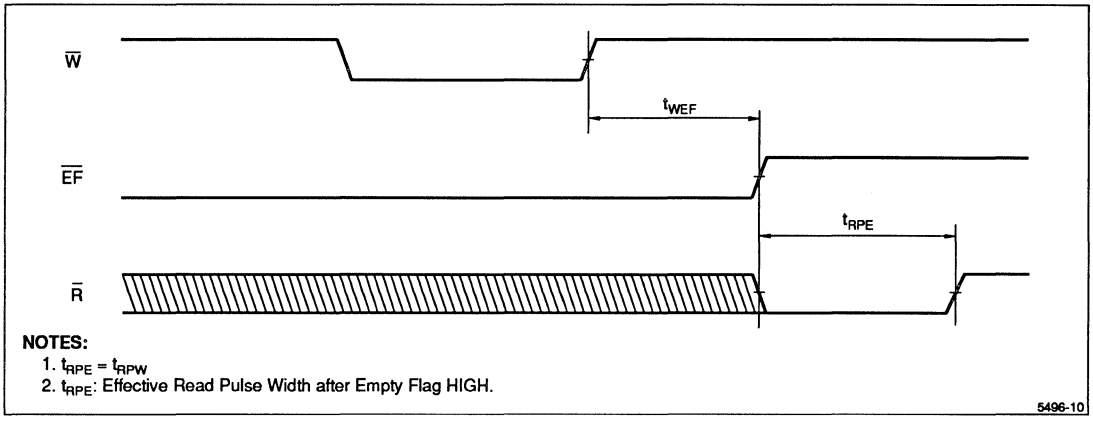


Figure 10. Empty Flag Timing

TIMING DIAGRAMS (cont'd)

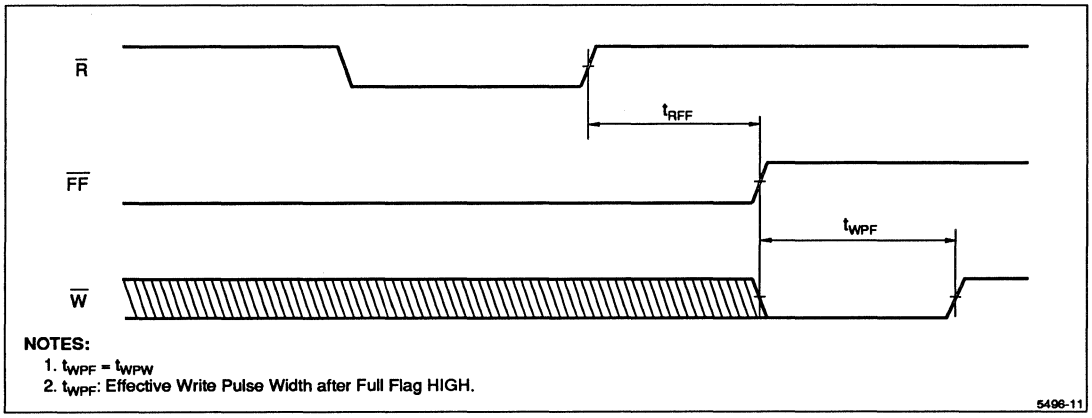


Figure 11. Full Flag Timing

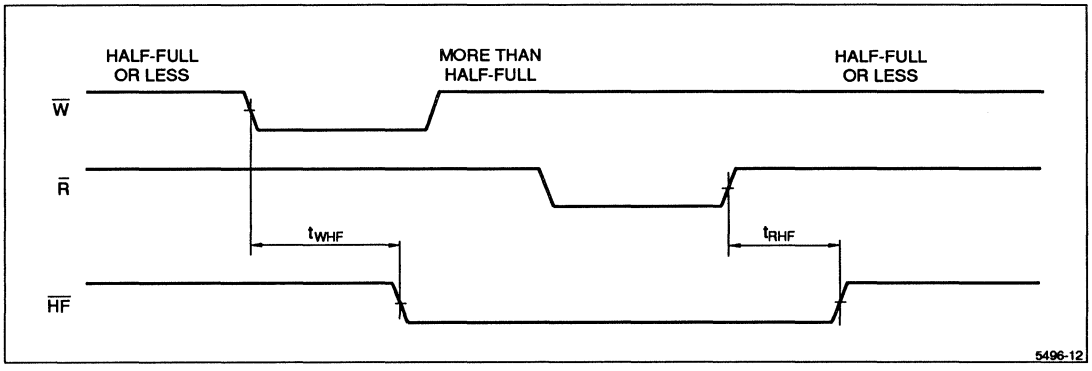


Figure 12. Half-Full Flag Timing

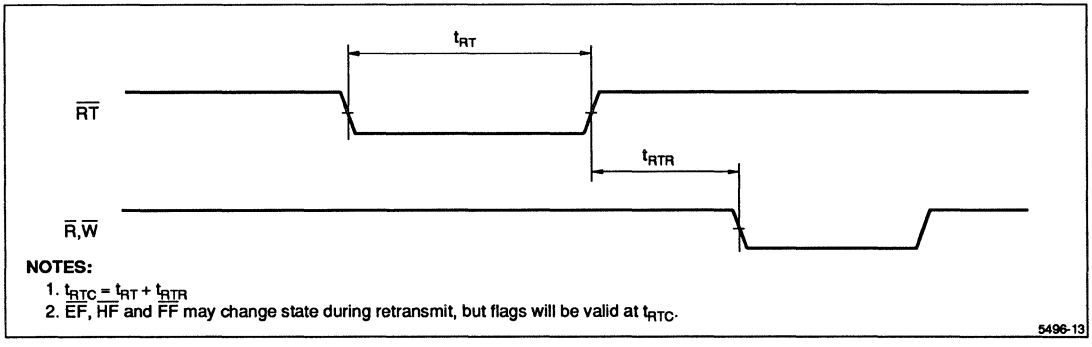


Figure 13. Retransmit Timing

TIMING DIAGRAMS (cont'd)

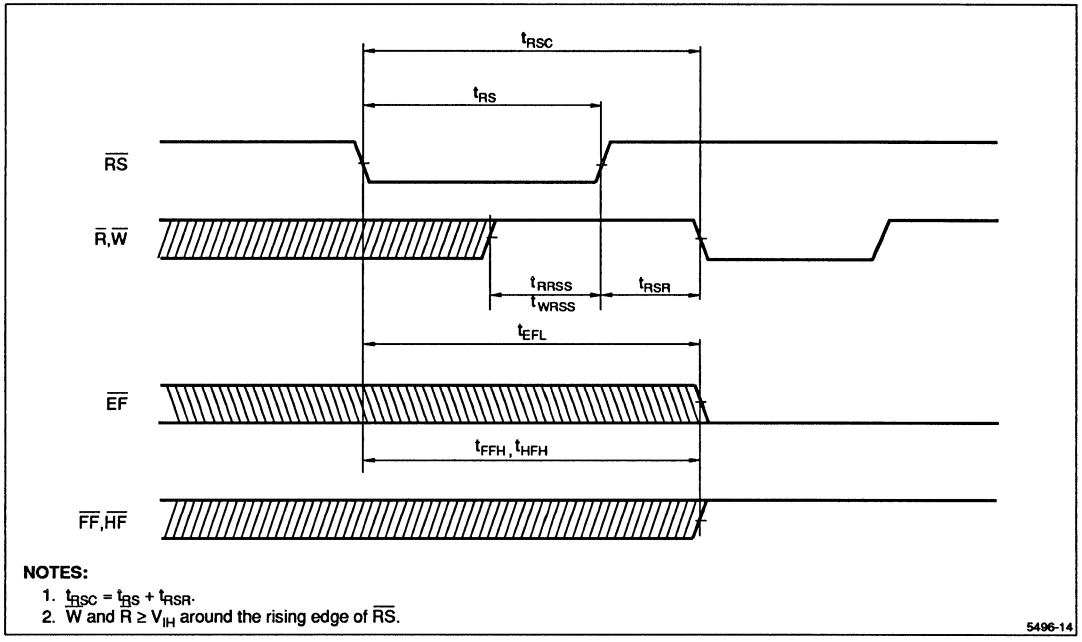


Figure 14. Reset Timing

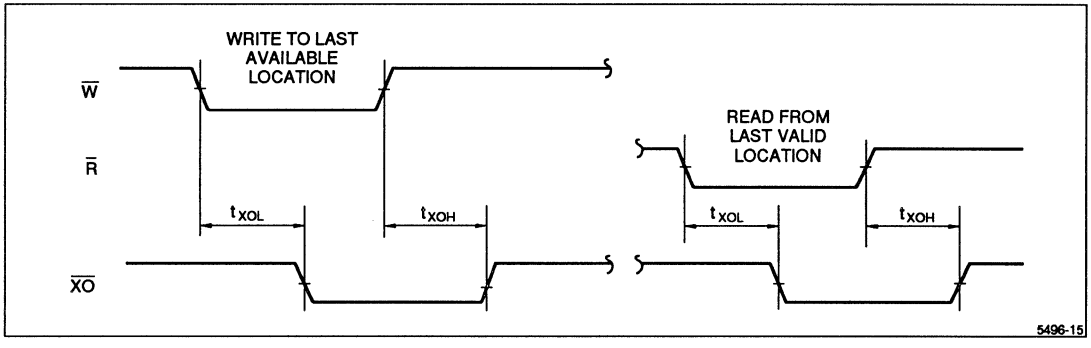


Figure 15. Expansion Out Timing

TIMING DIAGRAMS (cont'd)

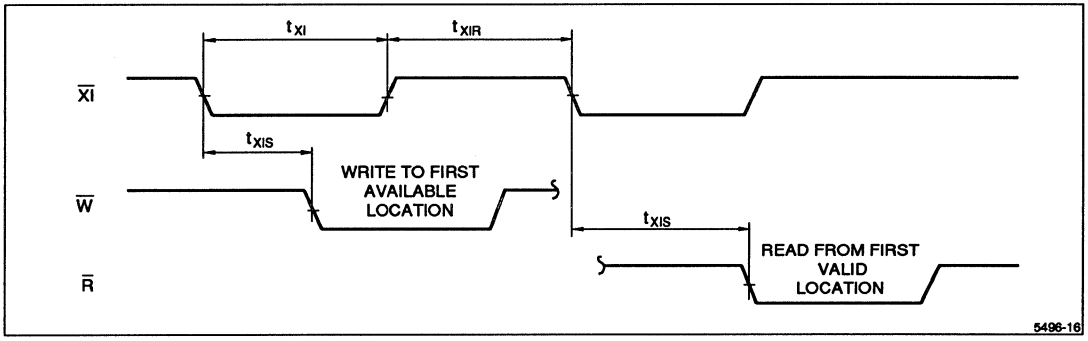


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in SINGLE mode by tying the EXPANSION IN pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word width expansion is implemented by placing multiple devices in parallel. Each device should be configured for SINGLE mode. In this arrangement, the behavior of the status flags will be identical for all devices, so these flags may be derived from any one device.

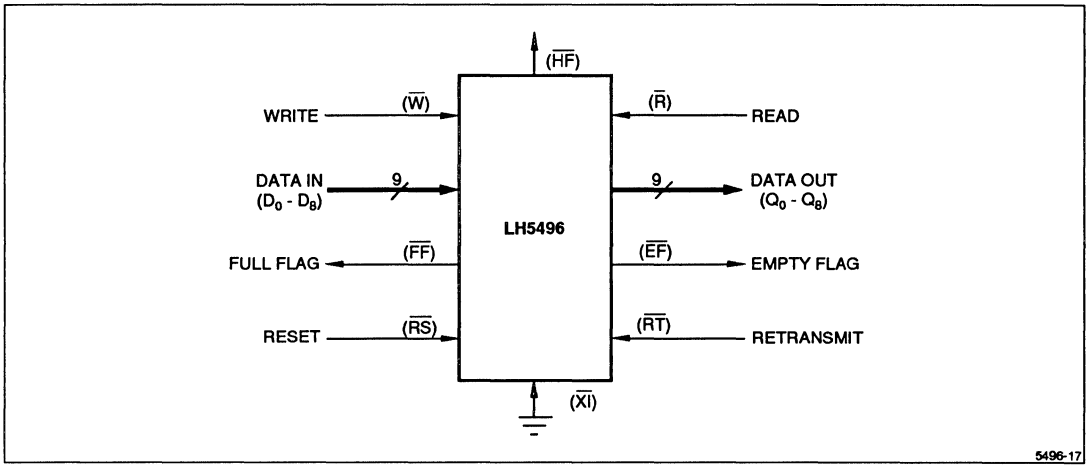


Figure 17. Single FIFO (512 × 9)

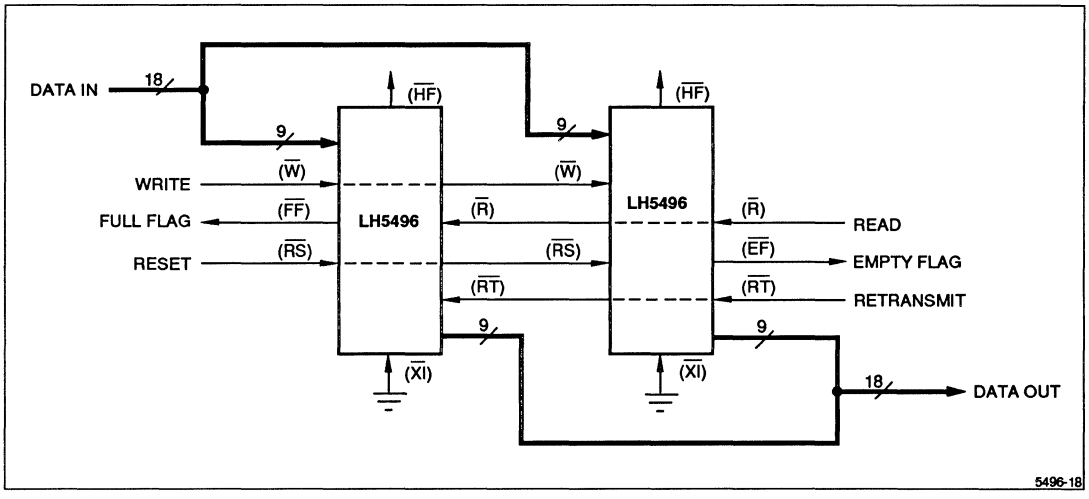


Figure 18. FIFO Width Expansion (512 × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in EXPANSION mode. In this arrangement, the FIFOs are connected in a circular fashion with the EXPANSION OUT pin ($\overline{XO}$) of each device tied to the EXPANSION IN pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the FIRST LOAD pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In EXPANSION mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The HALF flag and RETRANSMIT functions are not available in DEPTH EXPANSION mode.

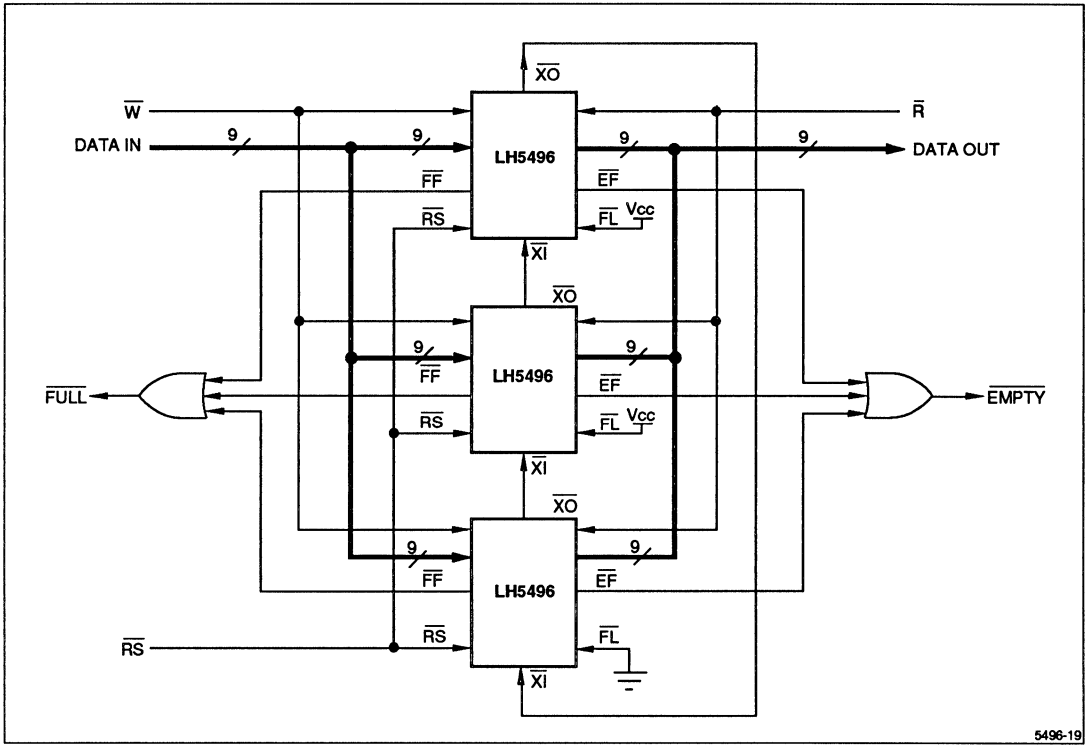


Figure 19. FIFO Depth Expansion (1536 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5496 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

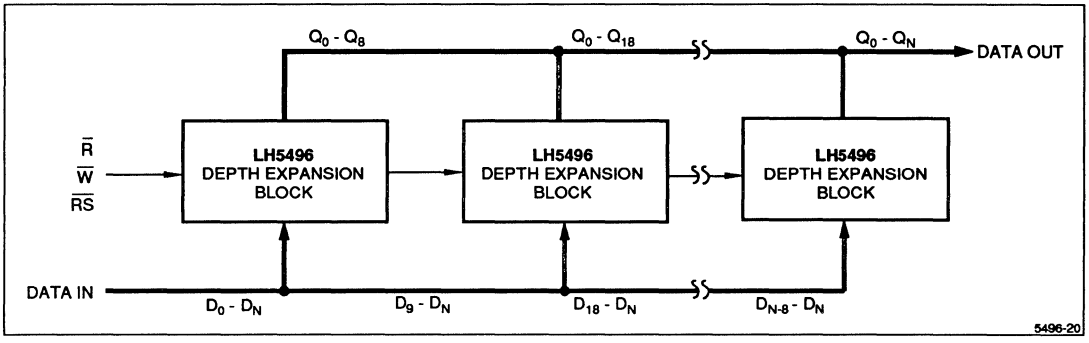


Figure 20. Compound FIFO Expansion

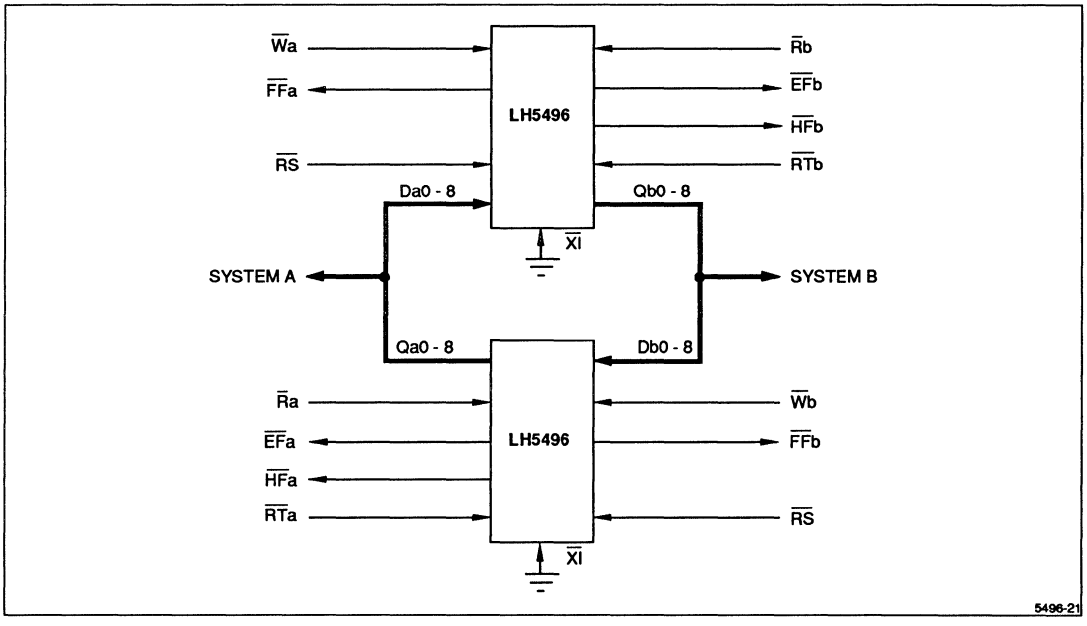
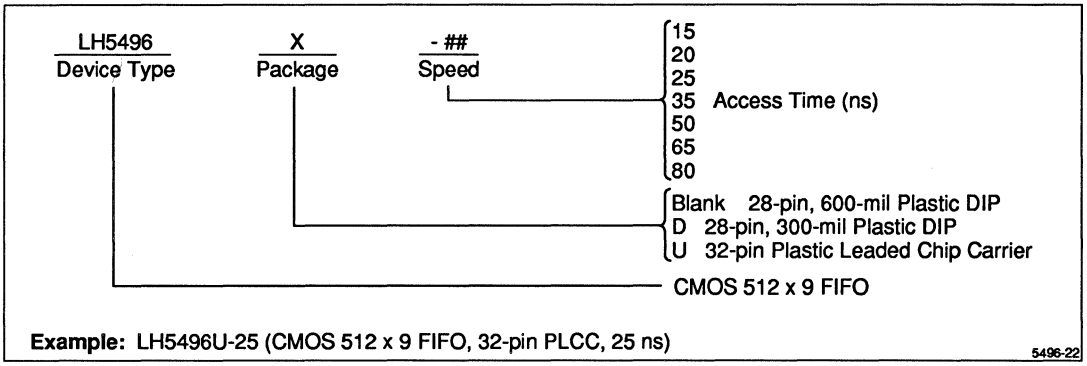


Figure 21. Bidirectional FIFO Buffer

ORDERING INFORMATION



Example: LH5496U-25 (CMOS 512 x 9 FIFO, 32-pin PLCC, 25 ns)

5496-22

LH5497

CMOS 1K × 9 FIFO

FEATURES

- Fast Access Times:
  15/20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP,
  28-Pin, 600-mil DIP or
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7202

FUNCTIONAL DESCRIPTION

The LH5497 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

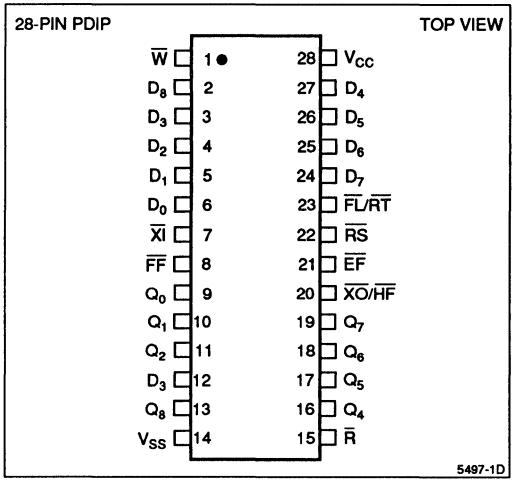


Figure 1. Pin Connections for DIP Package

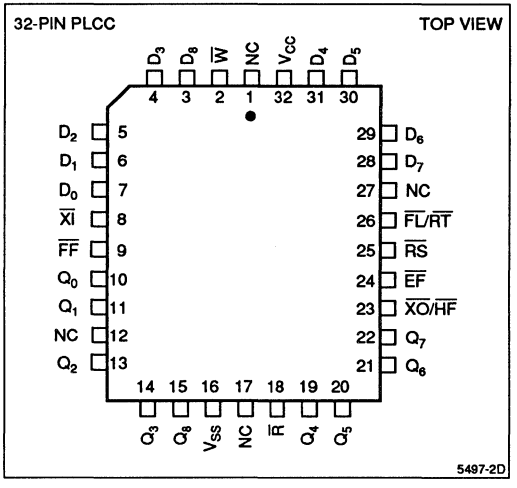


Figure 2. Pin Connections for PLCC Package

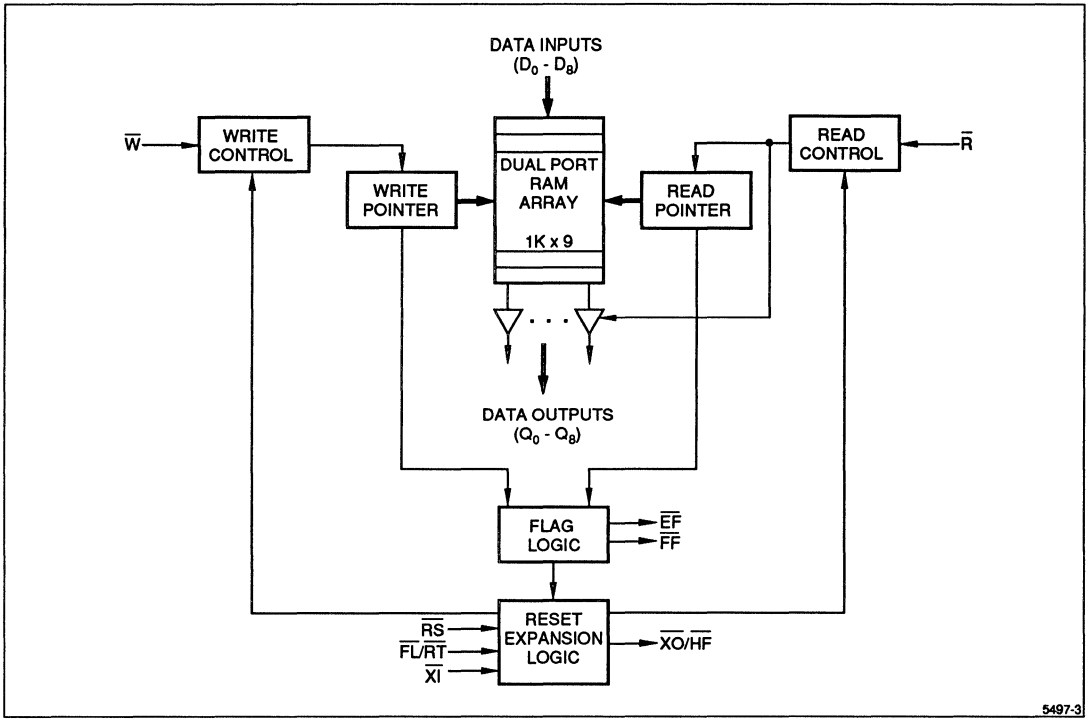


Figure 3. LH5497 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Control
$\overline{R}$	Read Control
$\overline{EF}$	Empty Flag

PIN	DESCRIPTION
$\overline{FF}$	Full Flag
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL}/\overline{RT}$	First Load, Retransmit
$\overline{RS}$	Reset

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs in High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage[1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4	—	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA	—	0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40MHz	—	100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}	—	15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V	—	5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

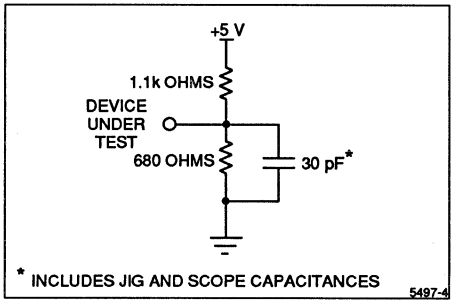


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read Low [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write High [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read High [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset to Empty Flag Low	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset to Half & Full Flag High	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read Low to Empty Flag Low	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read High to Half-Full Flag High	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out Low	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out High	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The Device is reset whenever the RESET pin ($\overline{RS}$) is taken to a low state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in SINGLE mode or DEPTH EXPANSION mode. A reset pulse is required when the device is first powered up. The READ ($\overline{R}$) and WRITE ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a high state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the WRITE ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the FULL flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the HALF flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The HALF flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The FULL flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The FULL flag will inhibit further writes until cleared by a valid read. The FULL flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the READ ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The EMPTY flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the READ ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the EMPTY flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains low, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the WRITE ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the FULL flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ low. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 1024 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

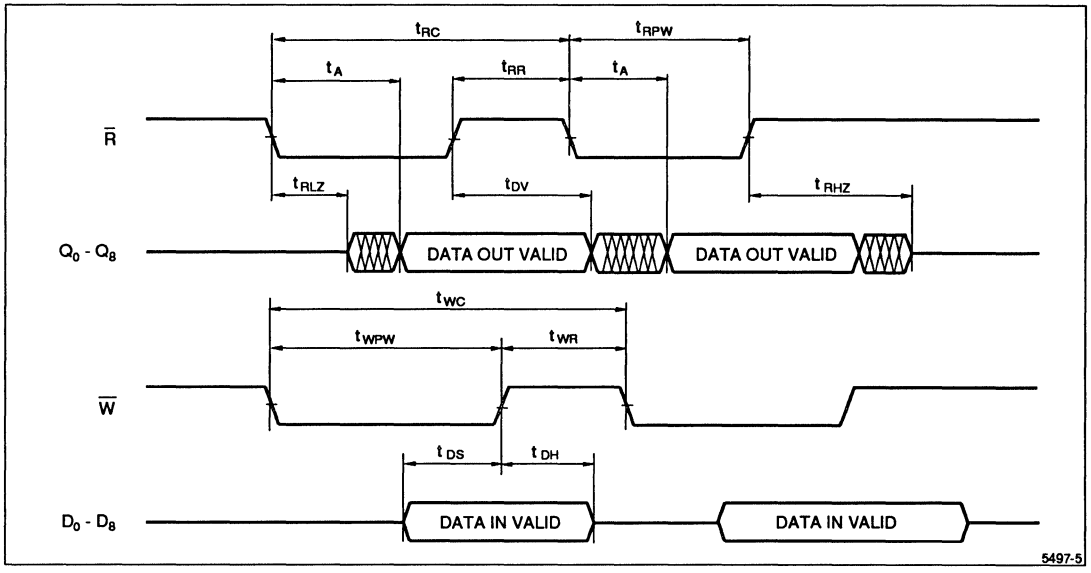


Figure 5. Asynchronous Write and Read Operation

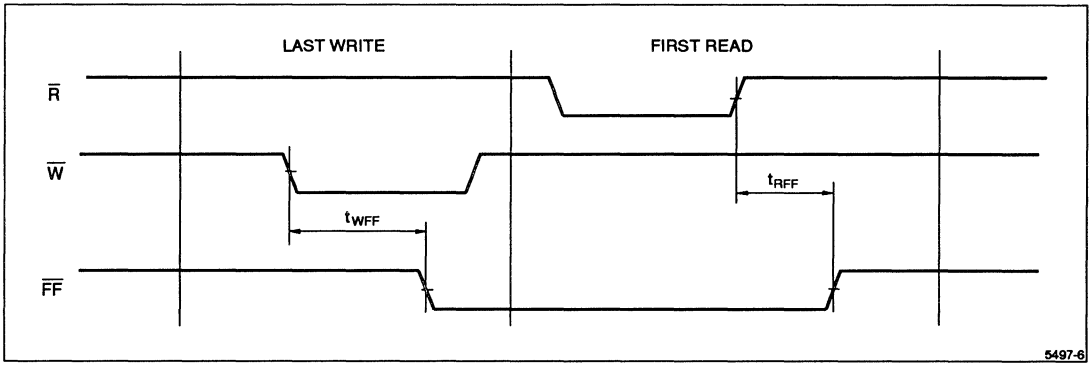


Figure 6. Full Flag from Last Write to First Read

TIMING DIAGRAMS (cont'd)

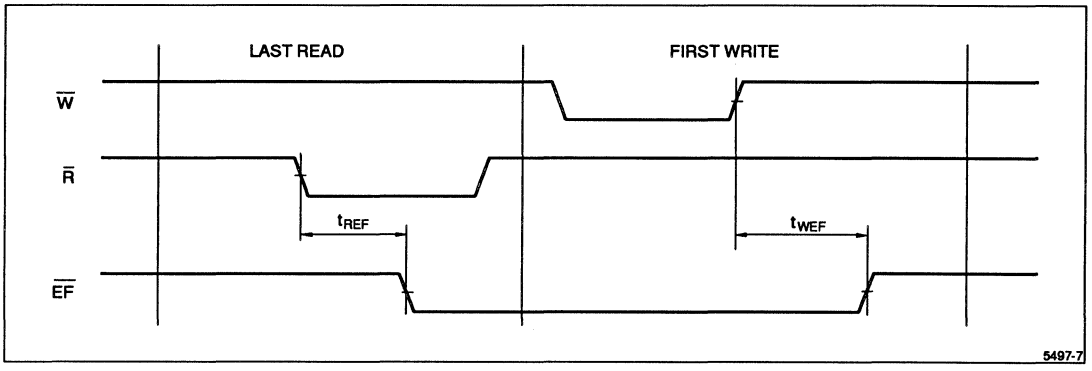


Figure 7. Empty Flag from Last Read to First Write

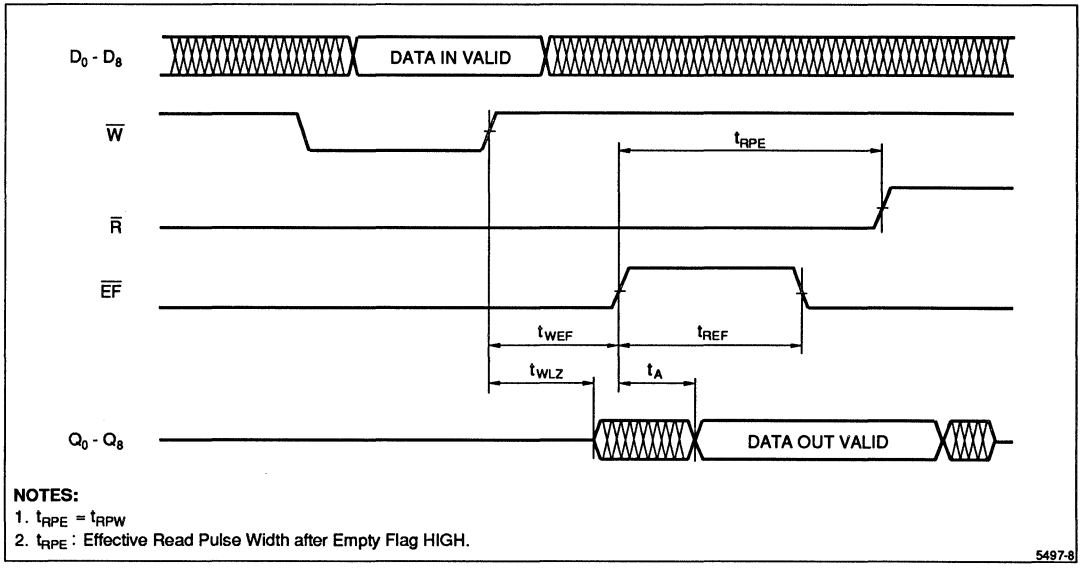


Figure 8. Read Data Flow-Through

TIMING DIAGRAMS (cont'd)

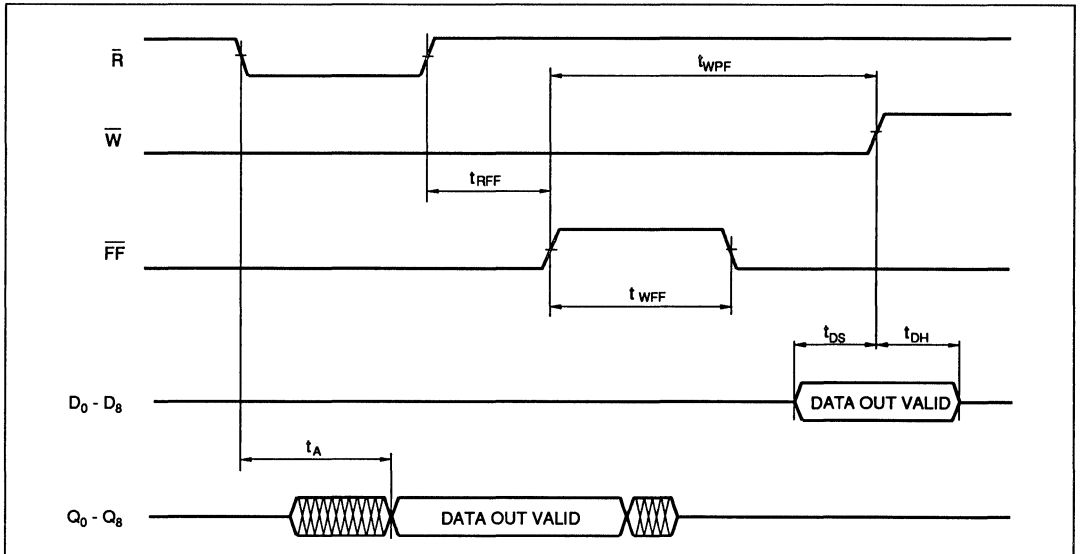


Figure 9. Write Data Flow-Through

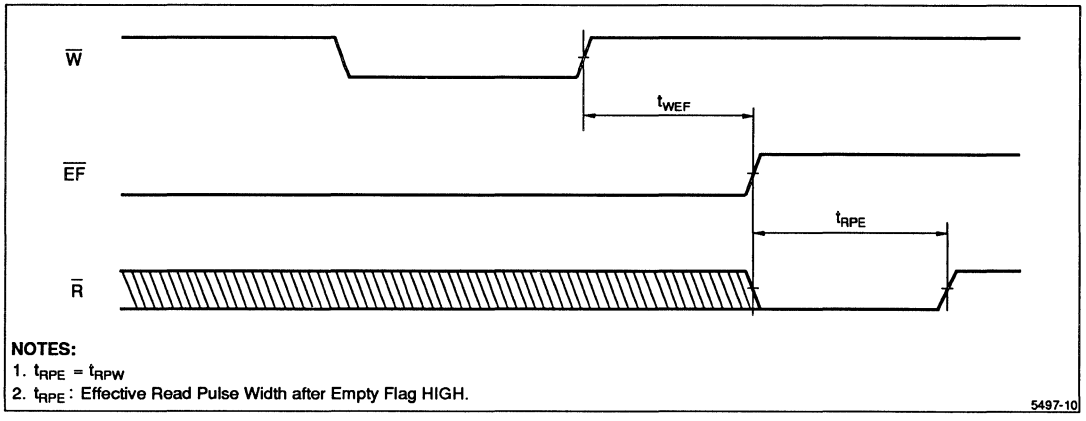


Figure 10. Empty Flag Timing

TIMING DIAGRAMS (cont'd)

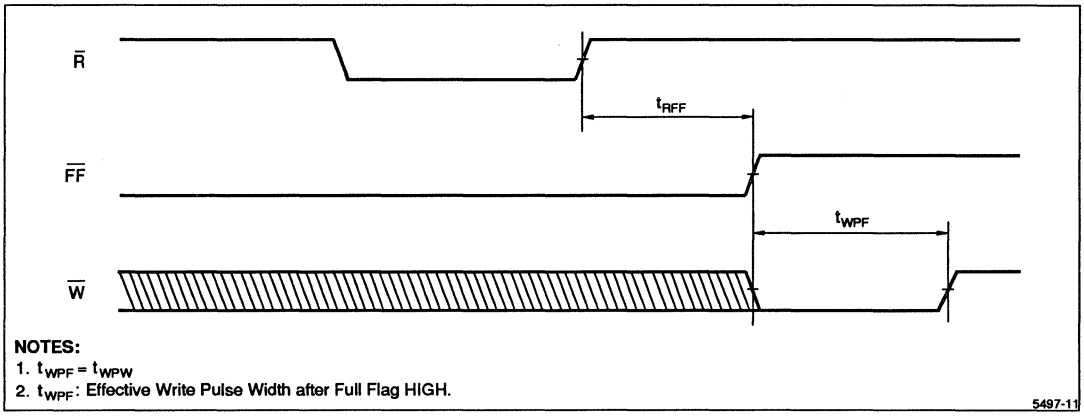


Figure 11. Full Flag Timing

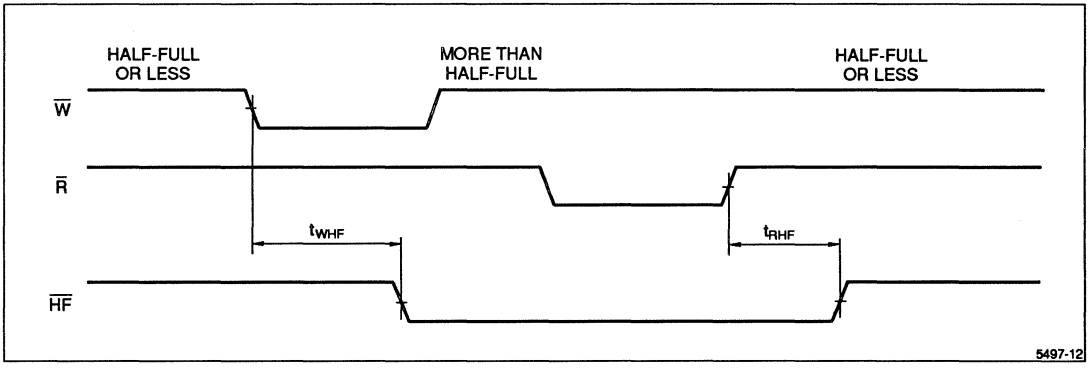


Figure 12. Half-Full Flag Timing

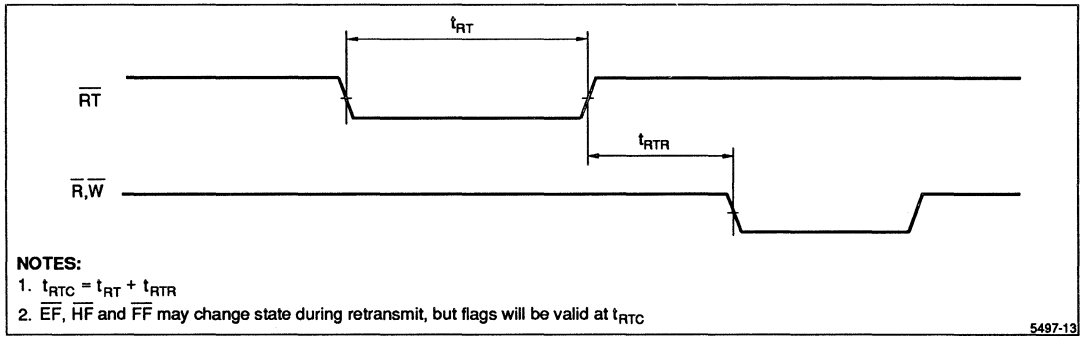


Figure 13. Retransmit Timing

TIMING DIAGRAMS (cont'd)

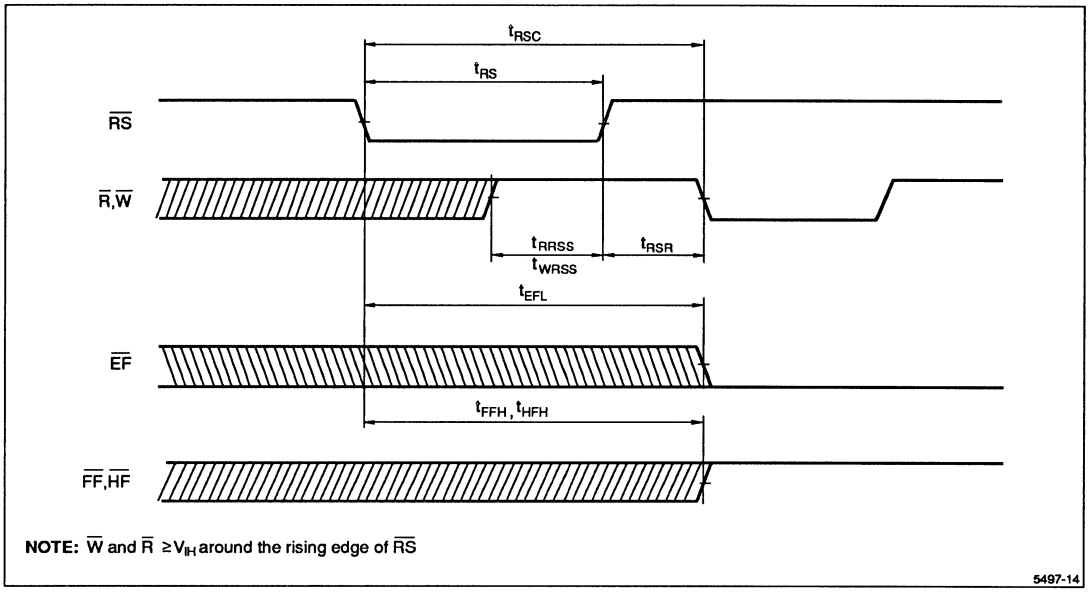


Figure 14. Reset Timing

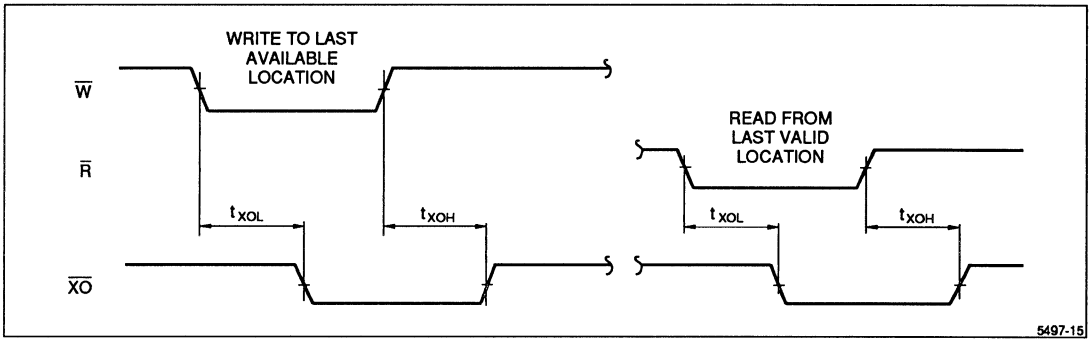


Figure 15. Expansion Out Timing

TIMING DIAGRAMS (cont'd)

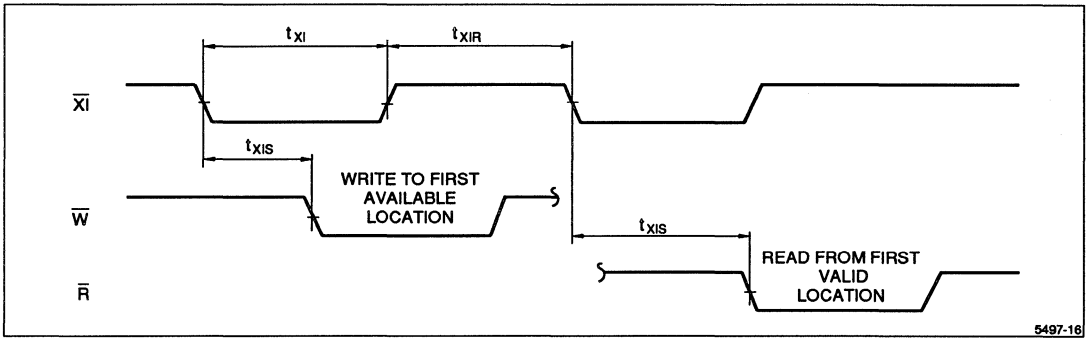


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in SINGLE mode by tying the EXPANSION IN pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word width expansion is implemented by placing multiple devices in parallel. Each device should be configured for SINGLE mode. In this arrangement, the behavior of the status flags will be identical for all devices, so these flags may be derived from any one device.

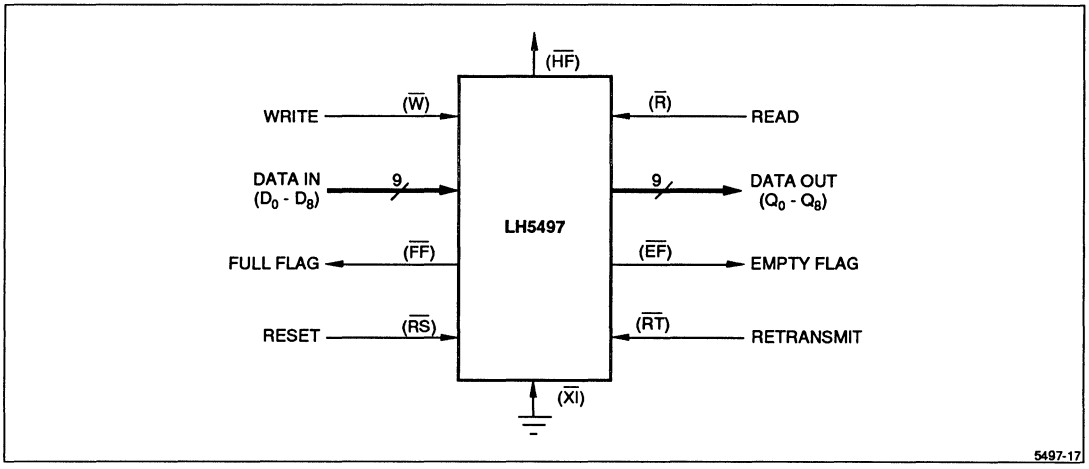


Figure 17. Single FIFO (1K × 9)

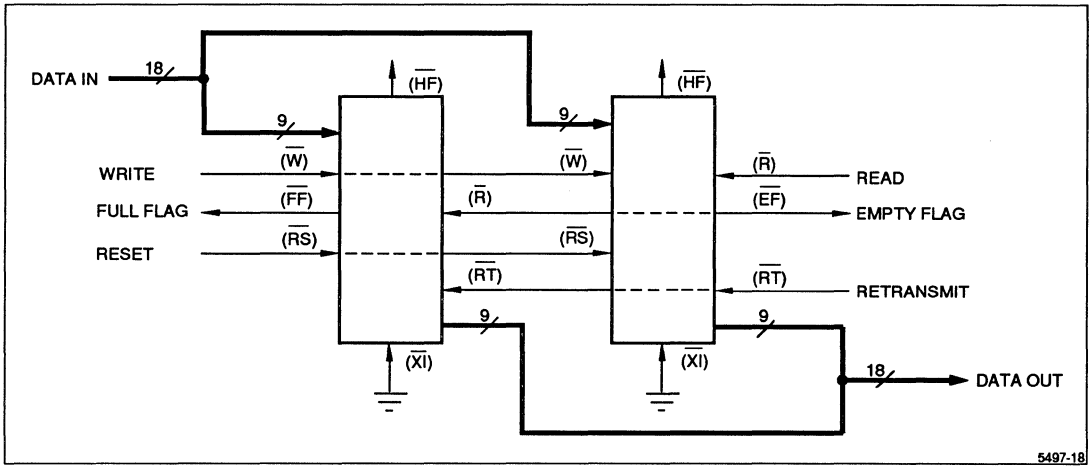


Figure 18. FIFO Width Expansion (1K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in EXPANSION mode. In this arrangement, the FIFOs are connected in a circular fashion with the EXPANSION OUT pin ($\overline{XO}$) of each device tied to the EXPANSION IN pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the FIRST LOAD pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In EXPANSION mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The HALF flag and RETRANSMIT functions are not available in DEPTH EXPANSION mode.

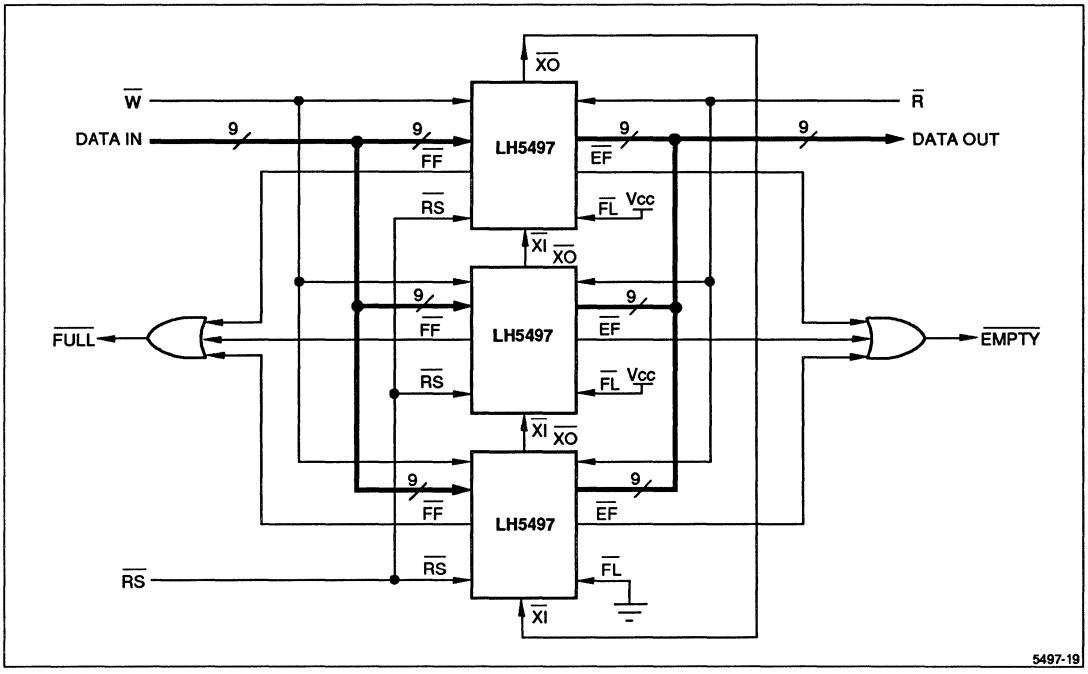


Figure 19. FIFO Depth Expansion (3072 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5497 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

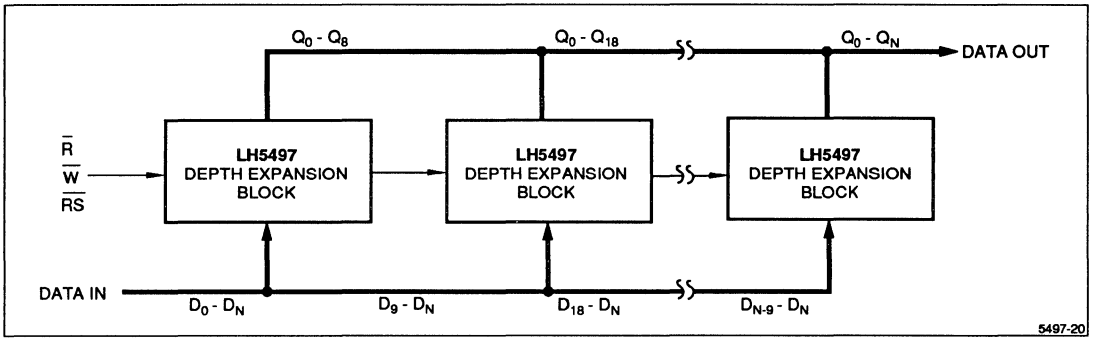


Figure 20. Compound FIFO

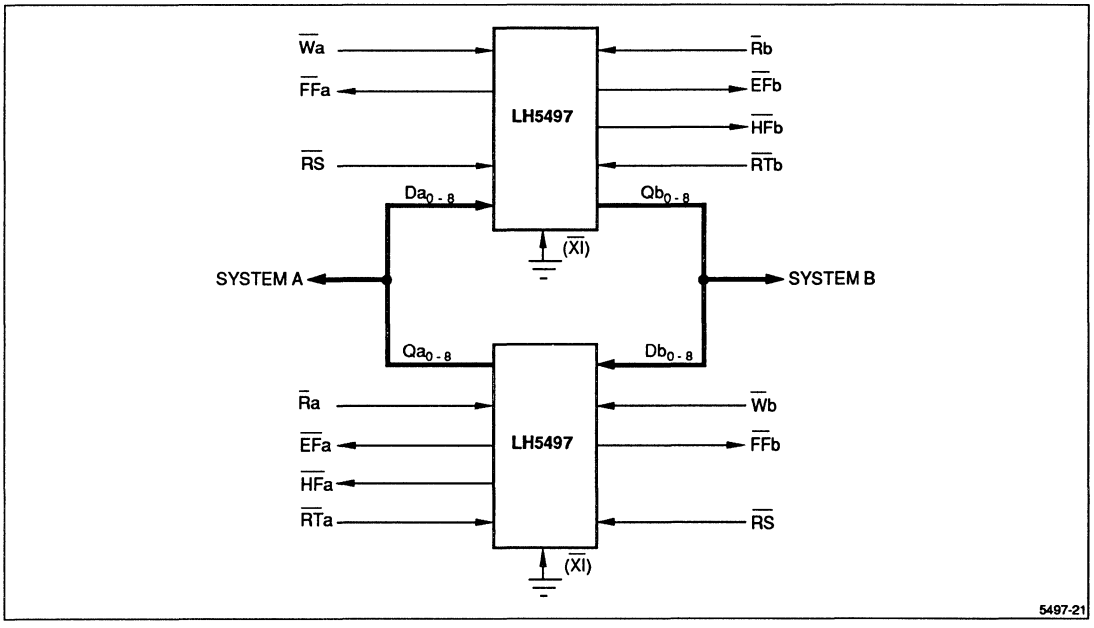
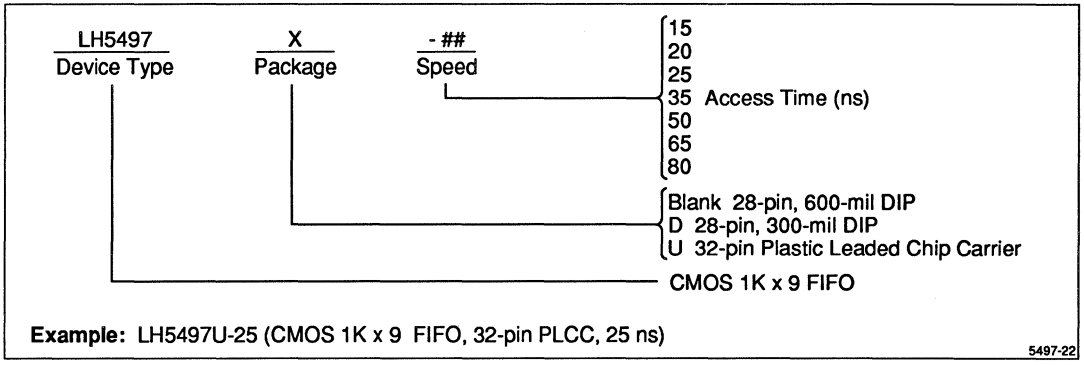


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5498

CMOS 2K × 9 FIFO

FEATURES

- Fast Access Times: 15/20/25/35/50/ 65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP,
  28-Pin, 600-mil DIP or
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7203

FUNCTIONAL DESCRIPTION

The LH5498 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

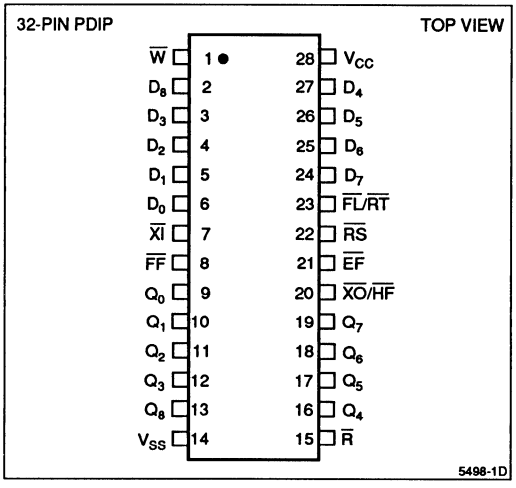


Figure 1. Pin Connections for DIP Package

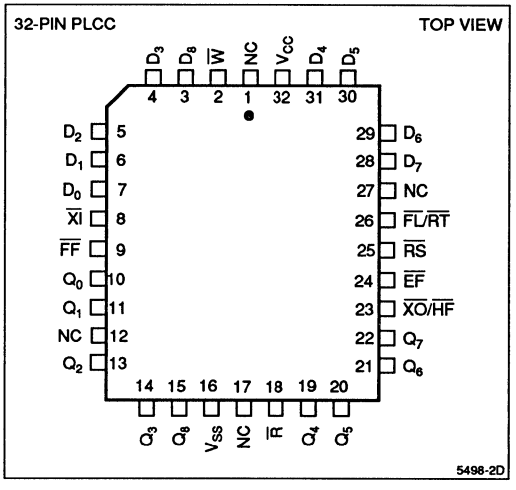


Figure 2. Pin Connections for PLCC Package

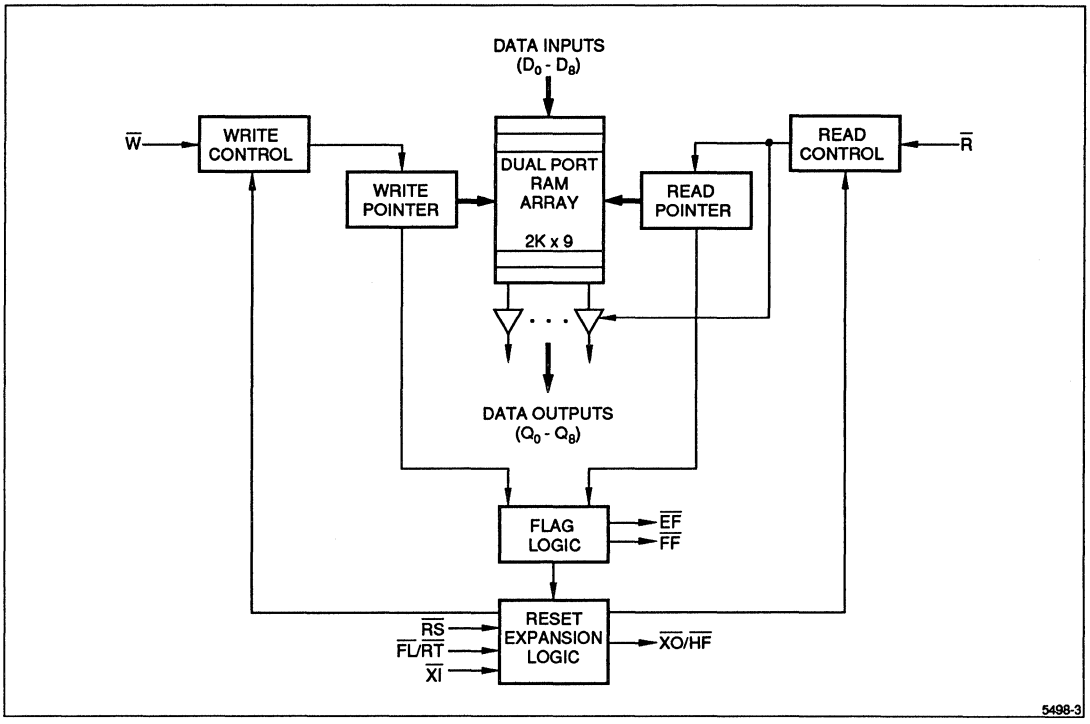


Figure 3. LH5498 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Control
$\overline{R}$	Read Control
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL}/\overline{RT}$	First Load, Retransmit
$\overline{RS}$	Reset
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any conditions other than those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage[1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

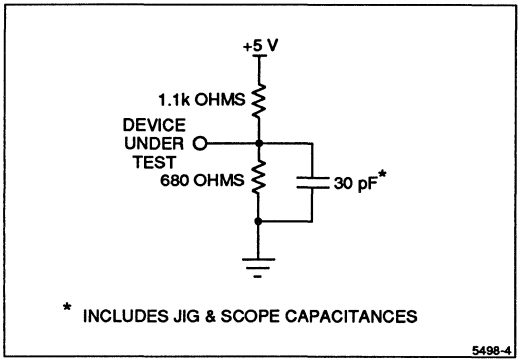


Figure 4. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read Low [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write High [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read High [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read High to $\overline{RS}$ High	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write High to $\overline{RS}$ High	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset to Empty Flag Low	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset to Half & Full Flag High	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read Low to Empty Flag Low	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read High to Half-Full Flag High	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out Low	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out High	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion In Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The Device is reset whenever the RESET pin ($\overline{RS}$) is taken to a low state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in SINGLE mode or DEPTH EXPANSION mode. A reset pulse is required when the device is first powered up. The READ ($\overline{R}$) and WRITE ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a high state t_{RRSS} and t_{WRSS} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the WRITE ($\overline{W}$) pin. Data setup and hold times must be observed on the data-in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the FULL flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the HALF flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one-half the total capacity of the FIFO. The HALF flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The FULL flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The FULL flag will inhibit further writes until cleared by a valid read. The FULL flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the READ ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The EMPTY flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the READ ($\overline{R}$) pin is brought low while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the EMPTY flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains low, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the WRITE ($\overline{W}$) pin is brought low while the FIFO is full, and held low in anticipation of a read cycle. At the end of the read cycle, the FULL flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be re-accessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 2048 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

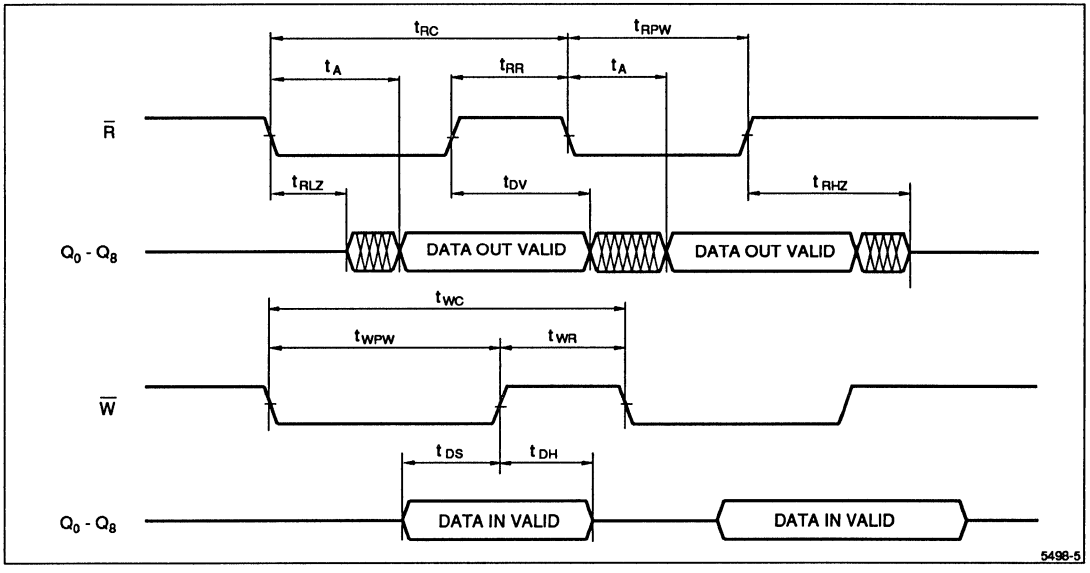


Figure 5. Asynchronous Write and Read Operation

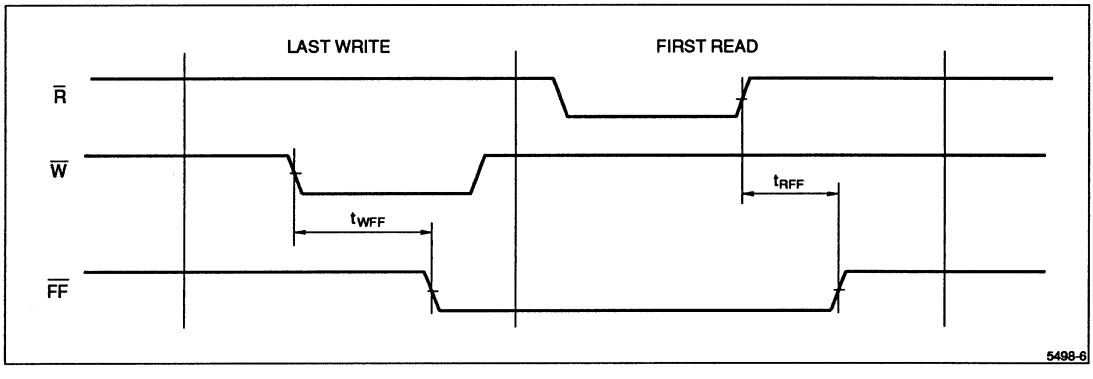


Figure 6. Full Flag from Last Write to First Read

TIMING DIAGRAMS (cont'd)

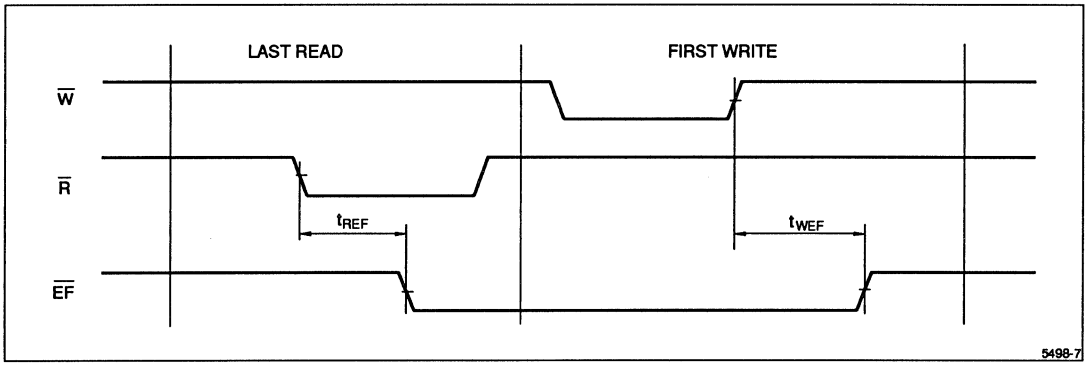


Figure 7. Empty Flag from Last Read to First Write

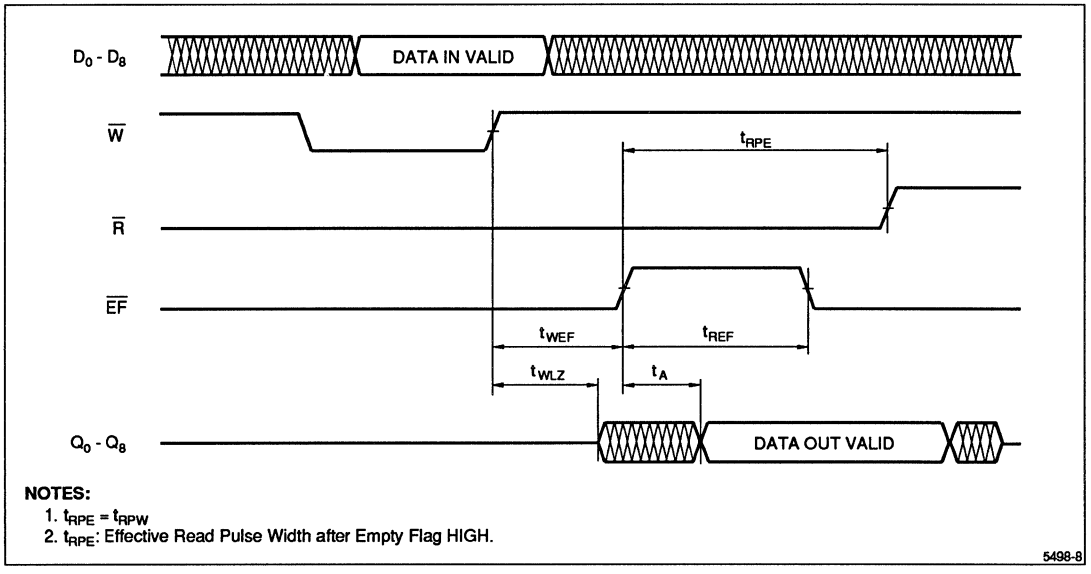


Figure 8. Read Data Flow-Through

TIMING DIAGRAMS (cont'd)

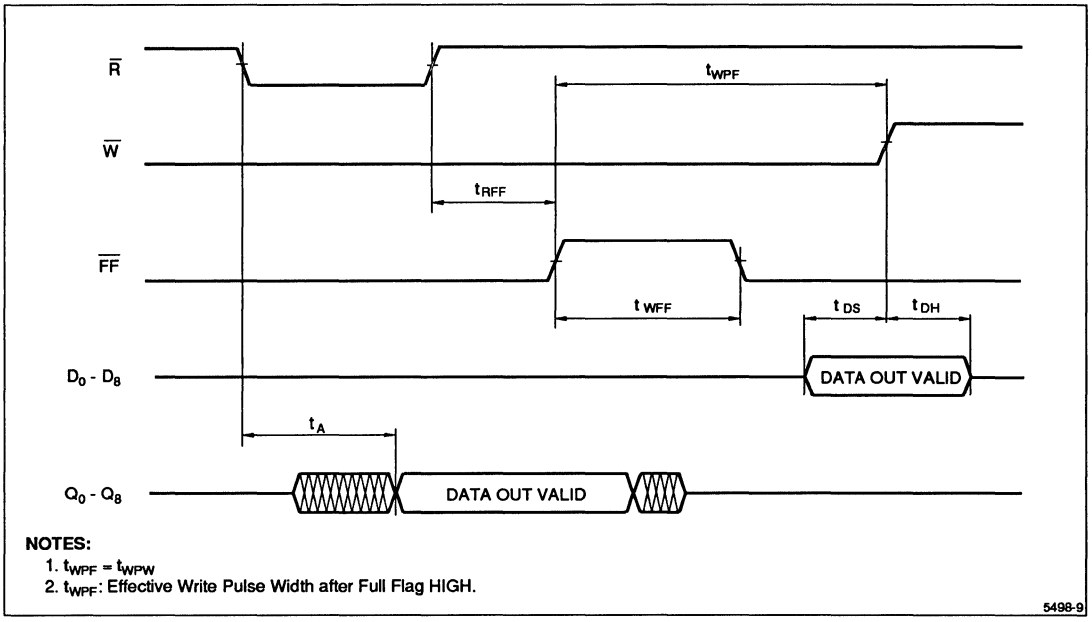


Figure 9. Write Data Flow-Through

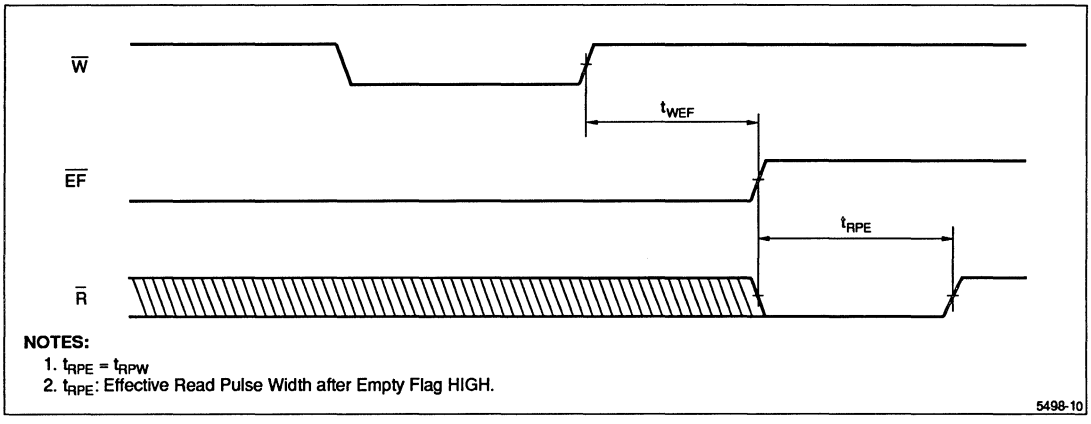


Figure 10. Empty Flag Timing

TIMING DIAGRAMS (cont'd)

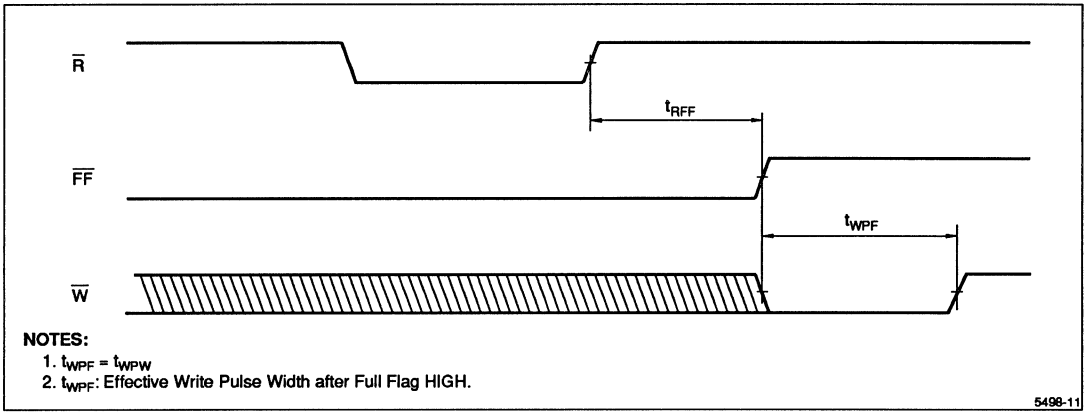


Figure 11. Full Flag Timing

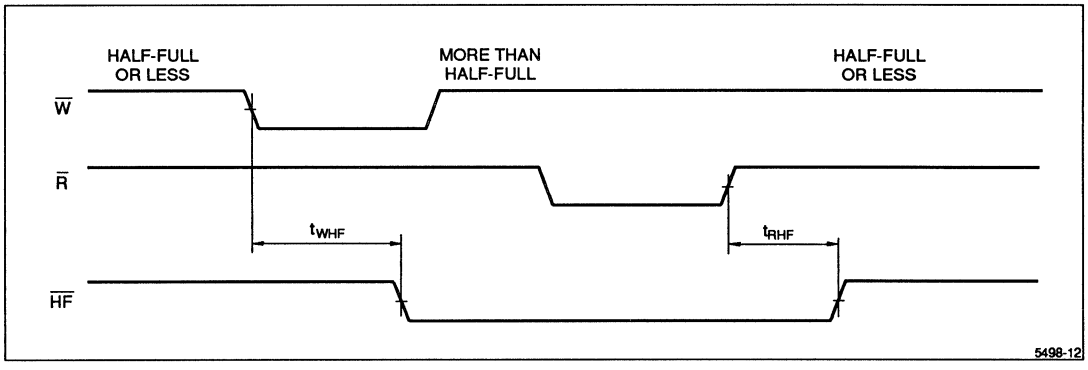


Figure 12. Half-Full Flag Timing

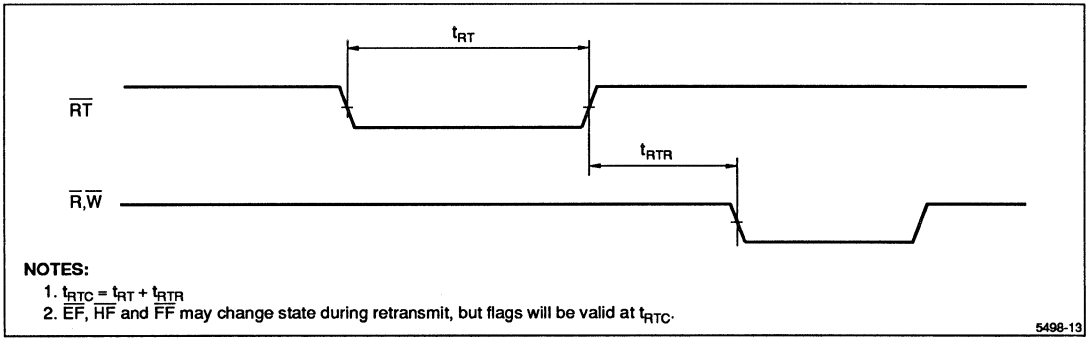


Figure 13. Retransmit Timing

TIMING DIAGRAMS (cont'd)

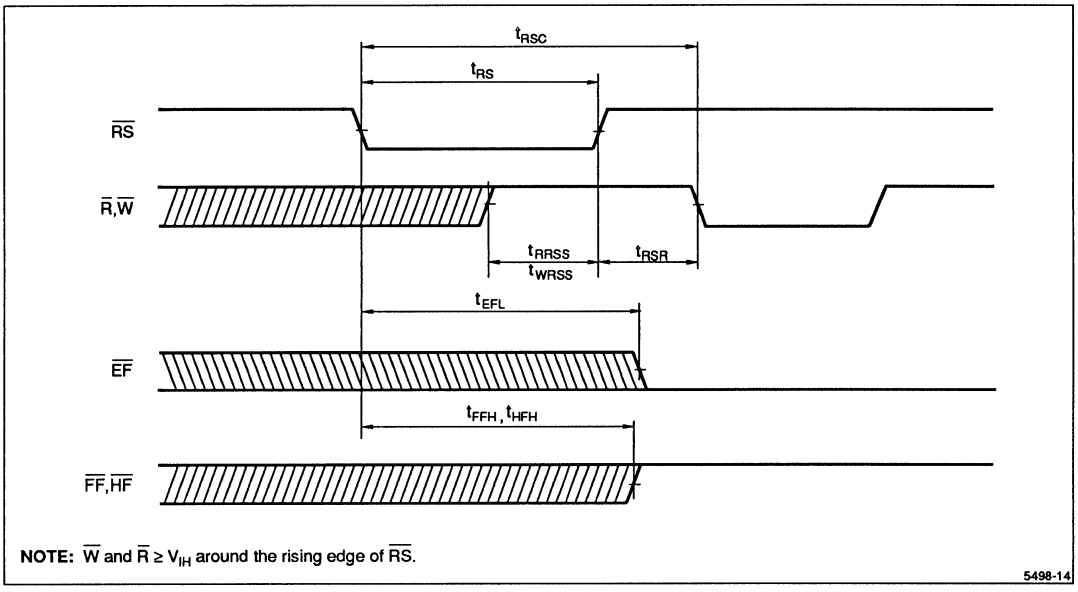


Figure 14. Reset Timing

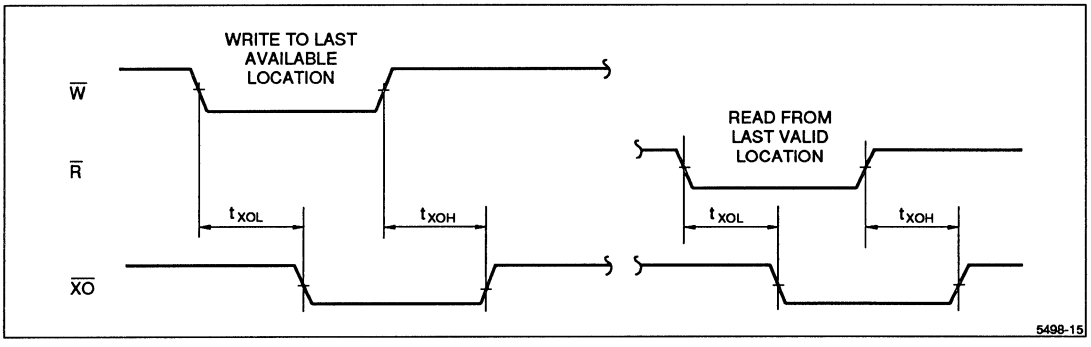


Figure 15. Expansion Out Timing

TIMING DIAGRAMS (cont'd)

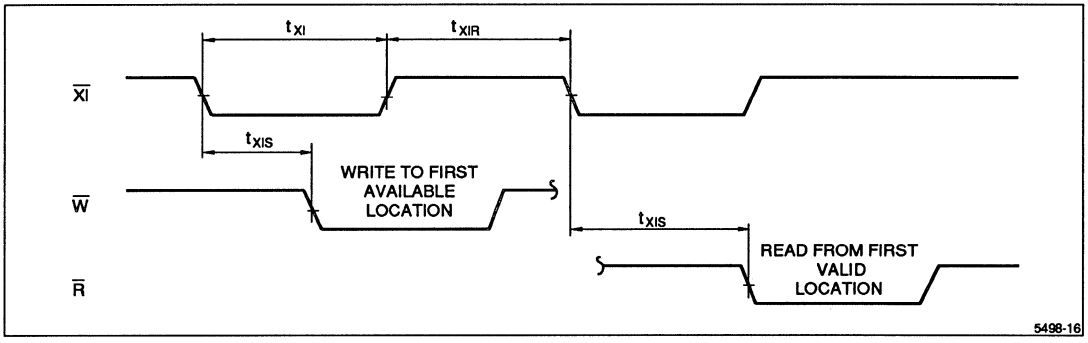


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in SINGLE mode by tying the EXPANSION IN pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word width expansion is implemented by placing multiple devices in parallel. Each device should be configured for SINGLE mode. In this arrangement, the behavior of the status flags will be identical for all devices, so these flags may be derived from any one device.

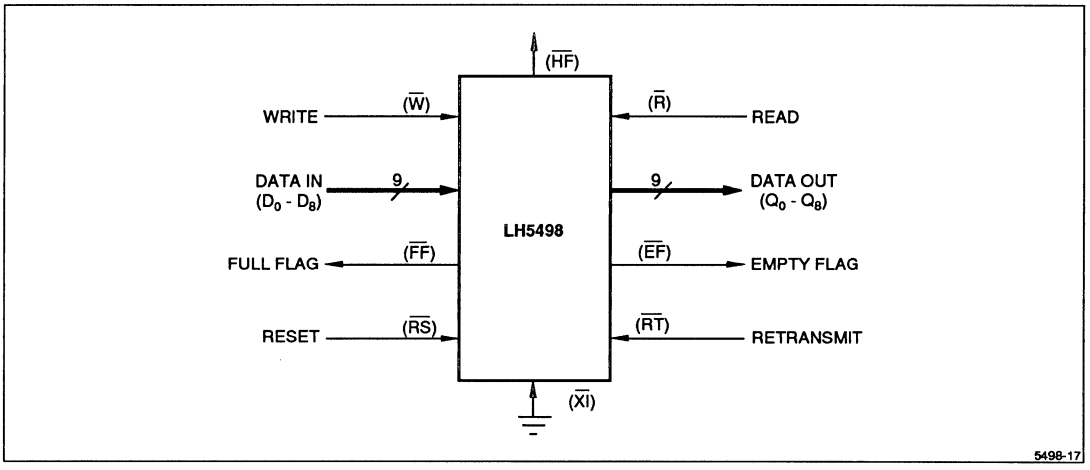


Figure 17. Single FIFO (2K × 9)

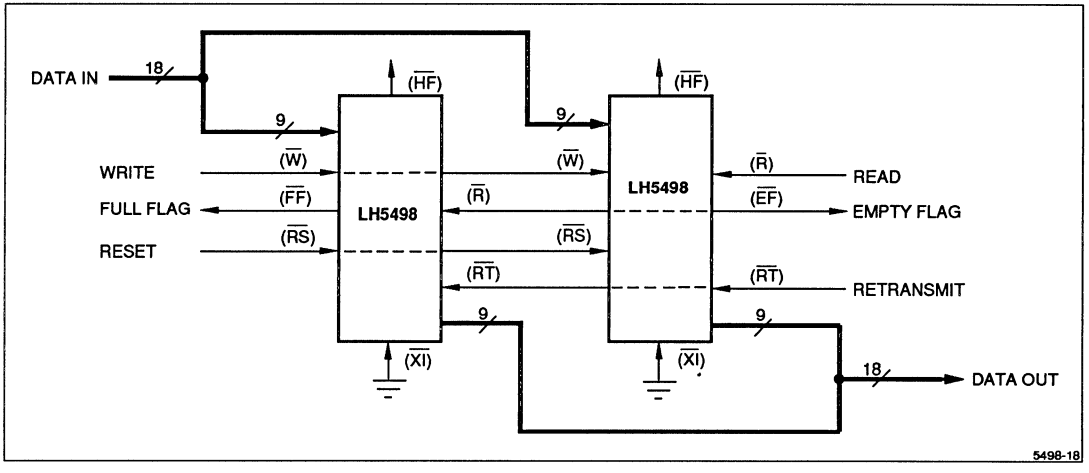


Figure 18. FIFO Width Expansion (2K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in EXPANSION mode. In this arrangement, the FIFOs are connected in a circular fashion with the EXPANSION OUT pin ($\overline{XO}$) of each device tied to the EXPANSION IN pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the FIRST LOAD pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In EXPANSION mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The HALF flag and RETRANSMIT functions are not available in DEPTH EXPANSION mode.

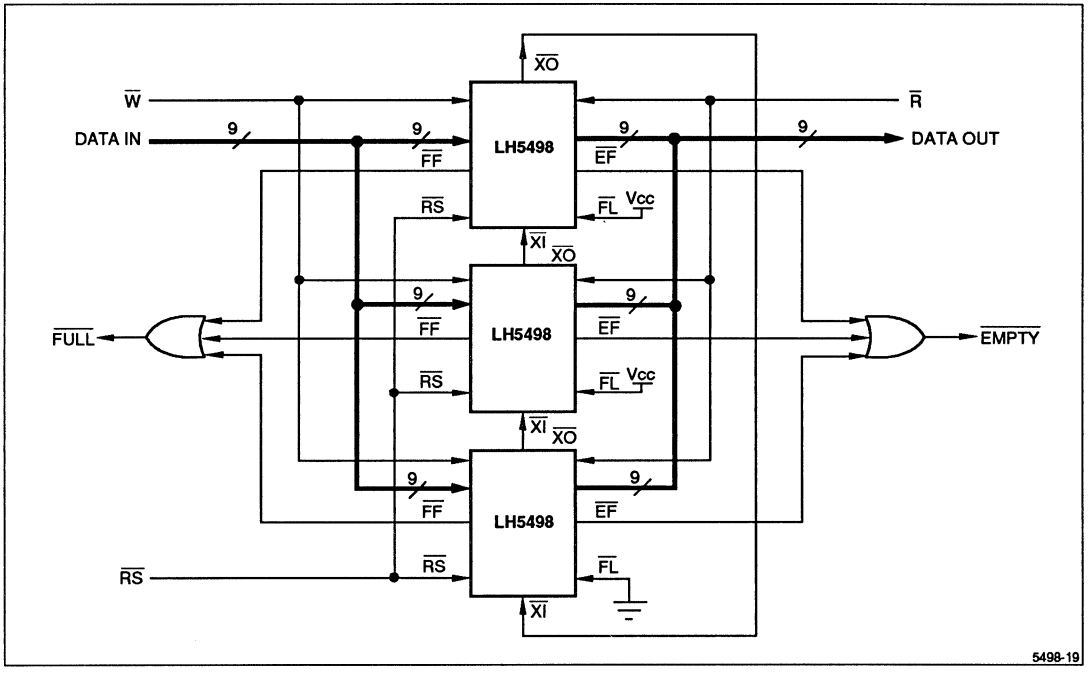


Figure 19. FIFO Depth Expansion (6144 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5498 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

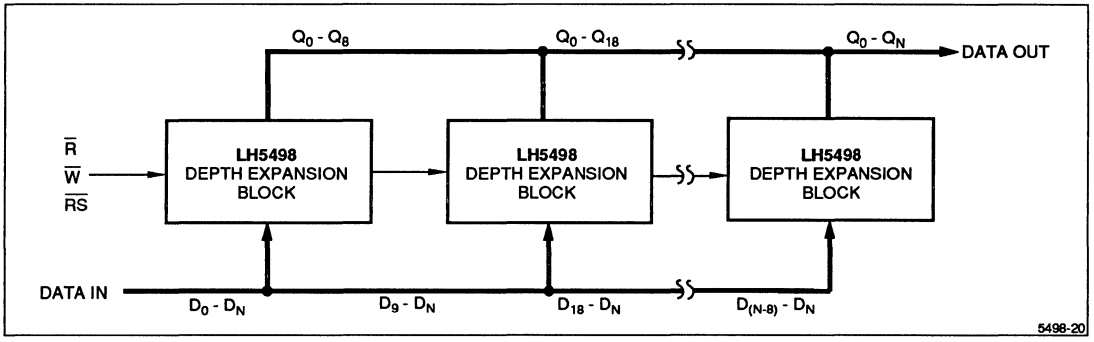


Figure 20. Compound FIFO

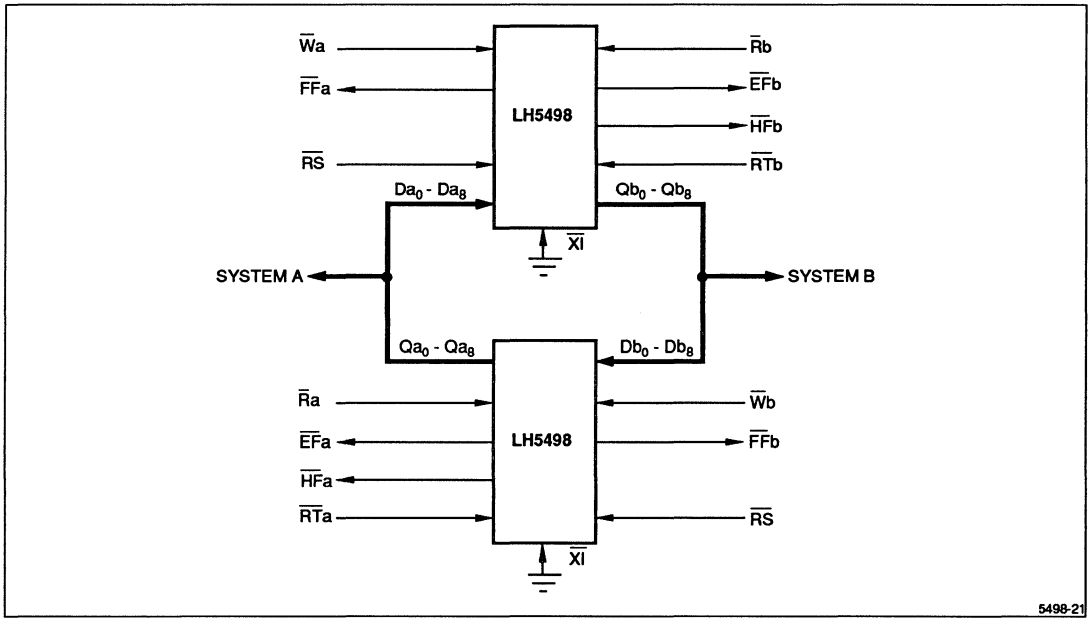
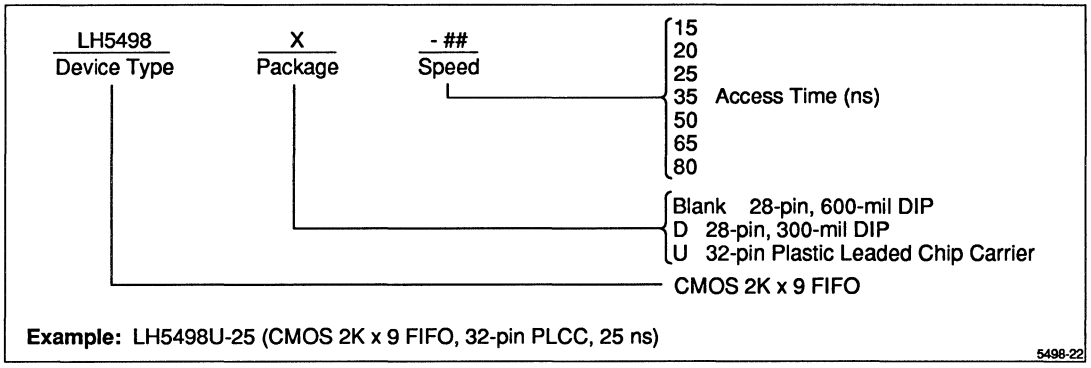


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5499

CMOS 4K × 9 FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 600-mil PDIP &
  32-Pin, PLCC
- Pin and Functionally Compatible with IDT7204

FUNCTIONAL DESCRIPTION

The LH5499 is a dual port memory with internal addressing to implement First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. Internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion in and Expansion out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

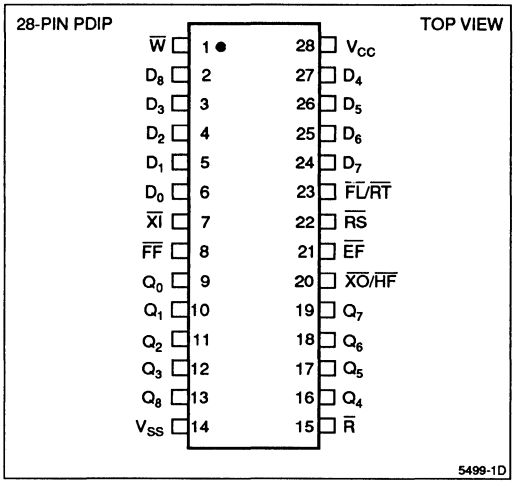


Figure 1. Pin Connections for PDIP Package

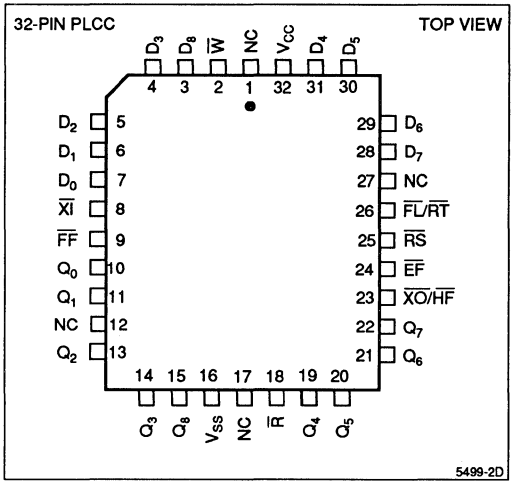


Figure 2. Pin Connections for PLCC Package

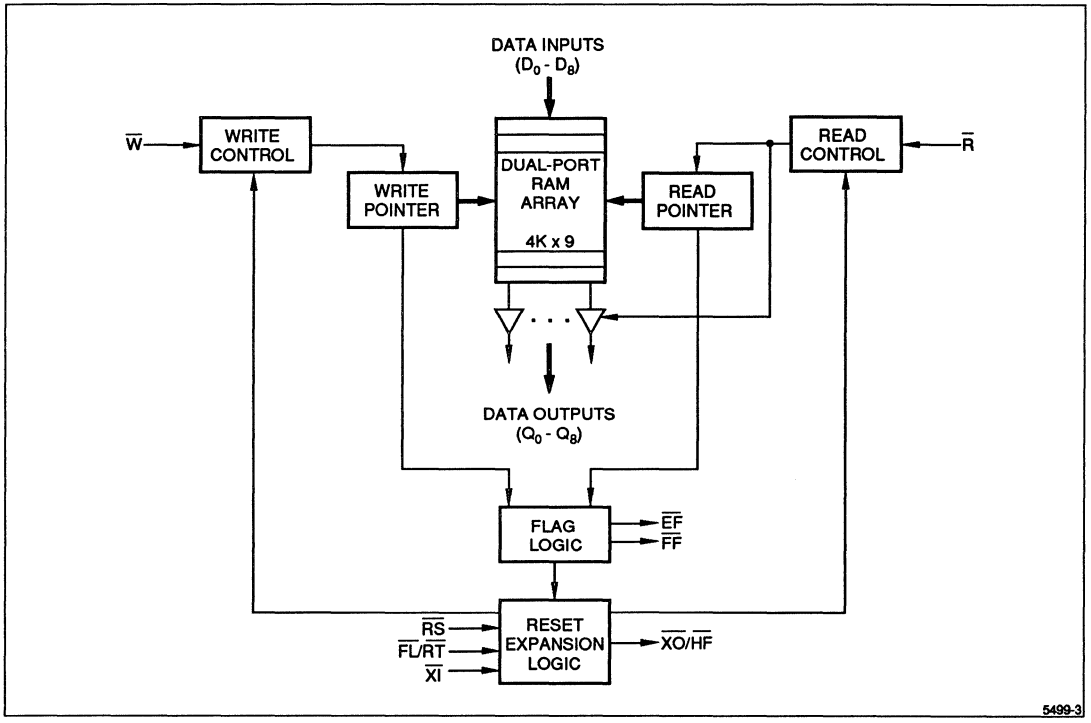


Figure 3. LH5499 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Control
$\overline{R}$	Read Control
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL}/\overline{RT}$	First Load, Retransmit
$\overline{RS}$	Reset
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in thc "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 33 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		8	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

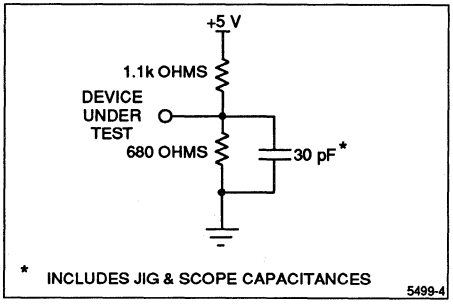


Figure 4. Output Load Caption

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING														
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read Low [3]	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write High [3,4]	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read High [3]	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING														
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING														
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
RETRANSMIT TIMING														
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING														
t_{EFL}	Reset to Empty Flag Low	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset to Half & Full Flag High	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read Low to Empty Flag Low	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read High to Half-Full Flag High	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING														
t_{XOL}	Expansion Out Low	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out High	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The Device is reset whenever the RESET pin ($\overline{RS}$) is taken to a low state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in SINGLE mode or DEPTH EXPANSION mode. A reset pulse is required when the device is first powered up. The READ ($\overline{R}$) and WRITE ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a high state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the WRITE ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the FULL flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the HALF flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The HALF flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The FULL flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The FULL flag will inhibit further writes until cleared by a valid read. The FULL flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the READ ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes high, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The EMPTY flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the READ ($\overline{R}$) pin is brought low while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the EMPTY flag will be momentarily de-asserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains low, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the WRITE ($\overline{W}$) pin is brought low while the FIFO is full, and held low in anticipation of a read cycle. At the end of the read cycle, the FULL flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held low. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ low. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 4096 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

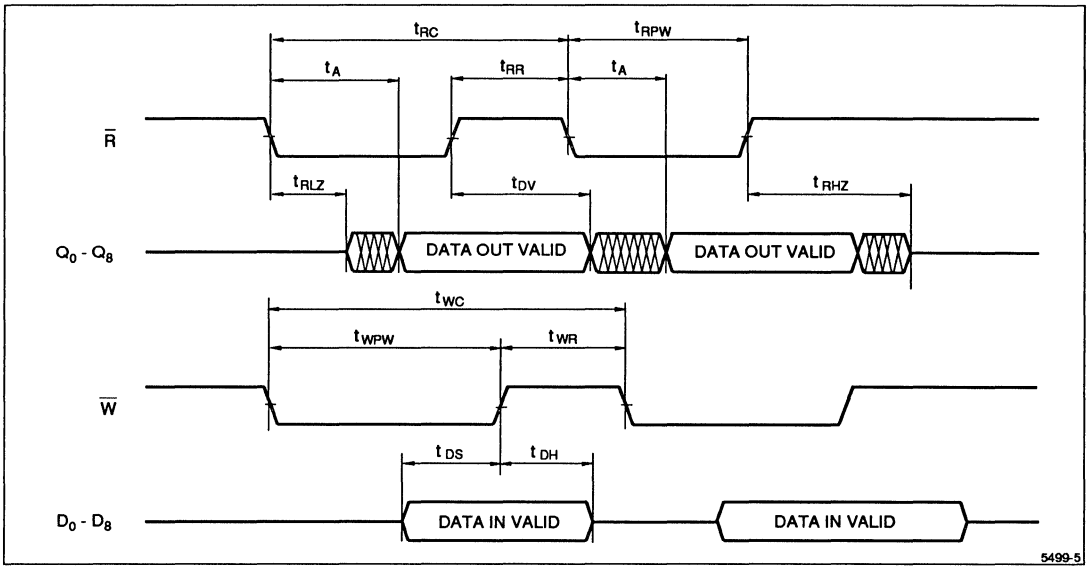


Figure 5. Asynchronous Write and Read Operation

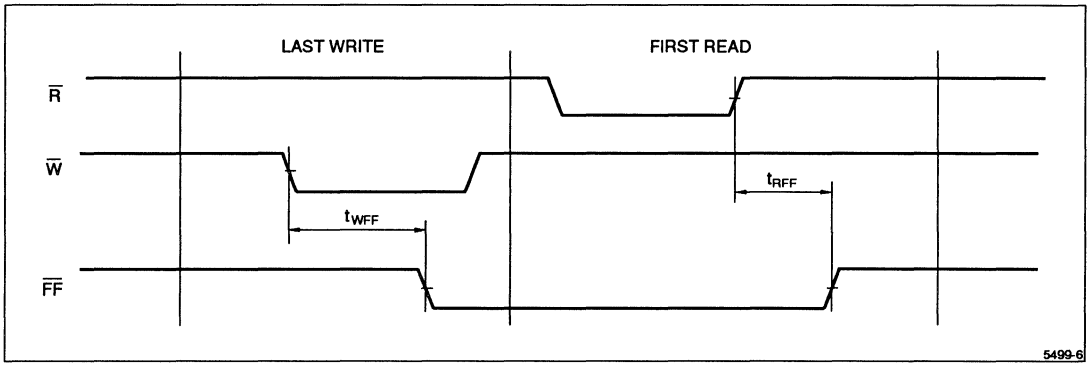


Figure 6. Full Flag from Last Write to First Read

TIMING DIAGRAMS (cont'd)

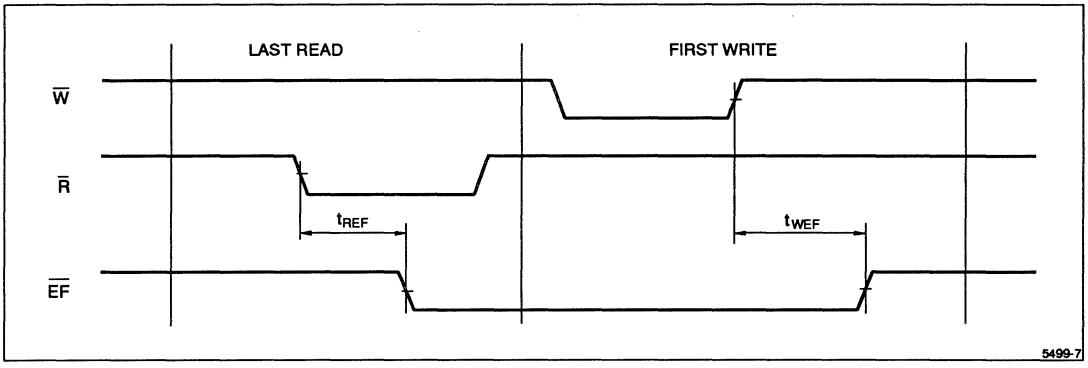


Figure 7. Empty Flag from Last Read to First Write

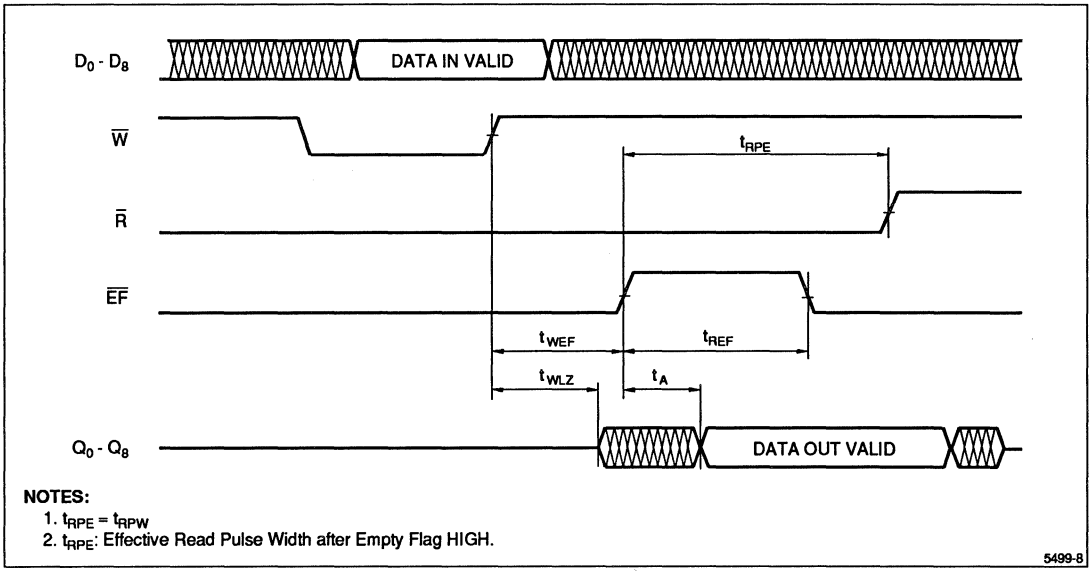
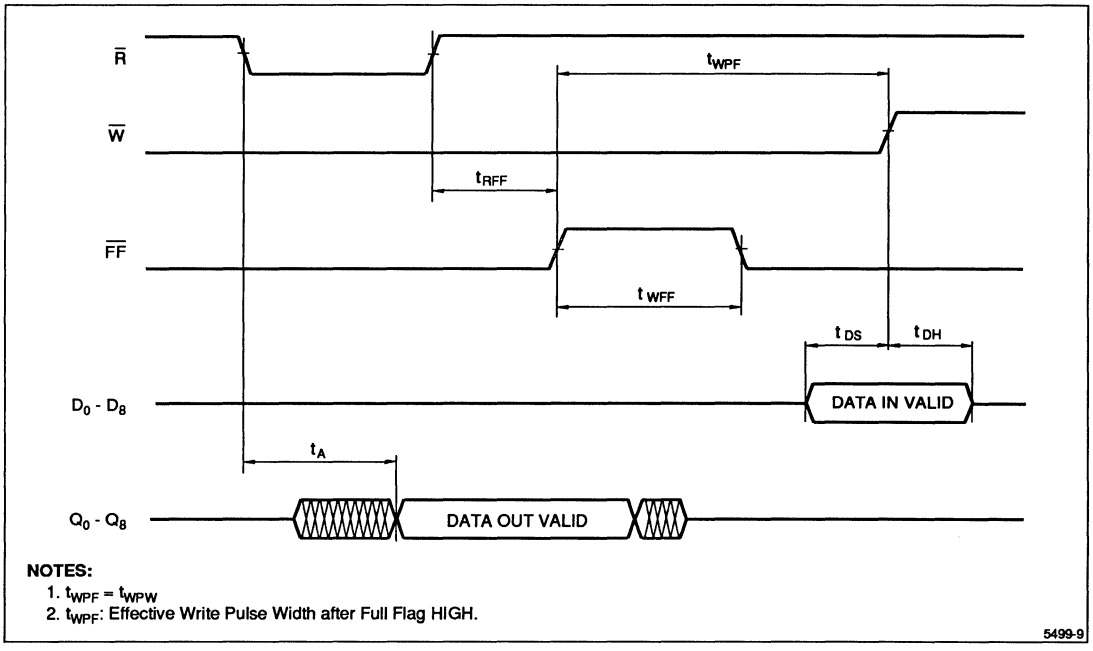


Figure 8. Read Data Flow-Through

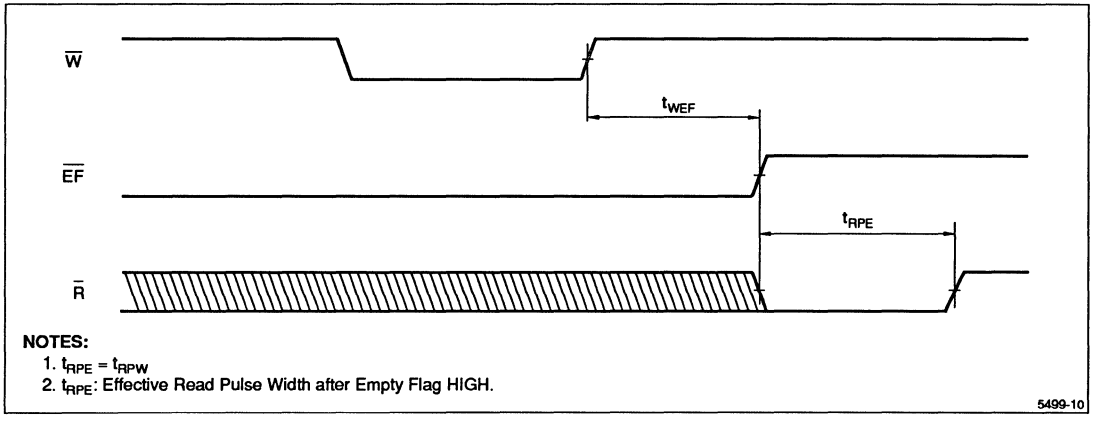
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

5499-9

Figure 9. Write Data Flow-Through

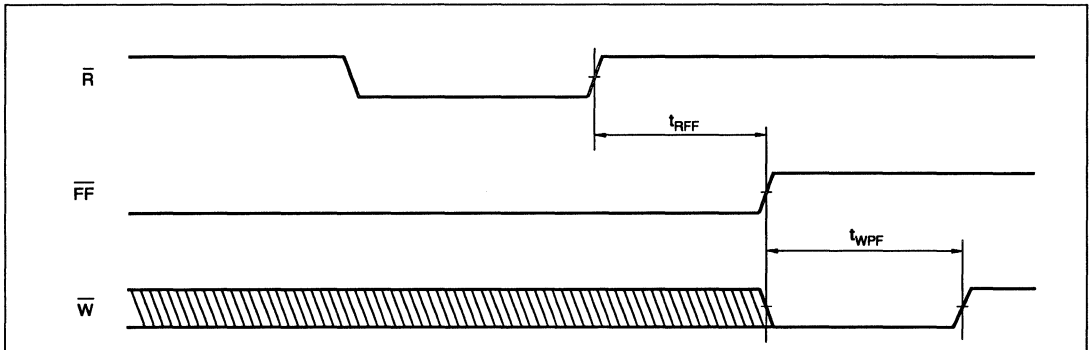


NOTES:
1. $t_{RPE} = t_{RPW}$
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

5499-10

Figure 10. Empty Flag Timing

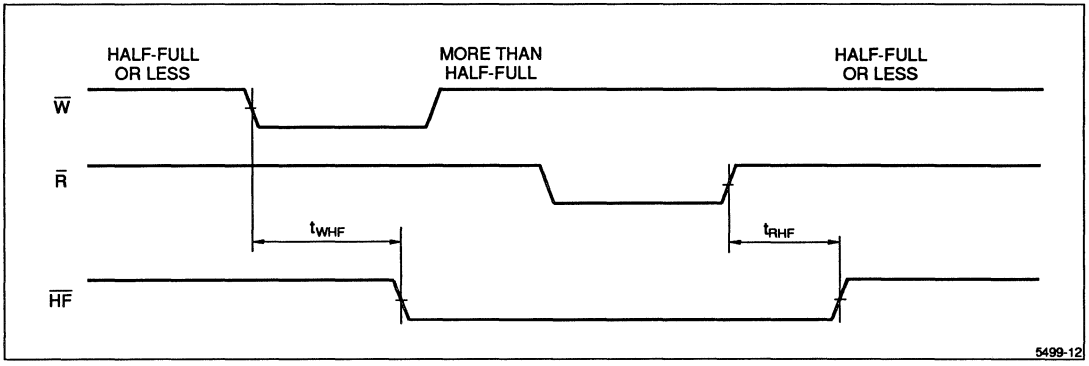
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

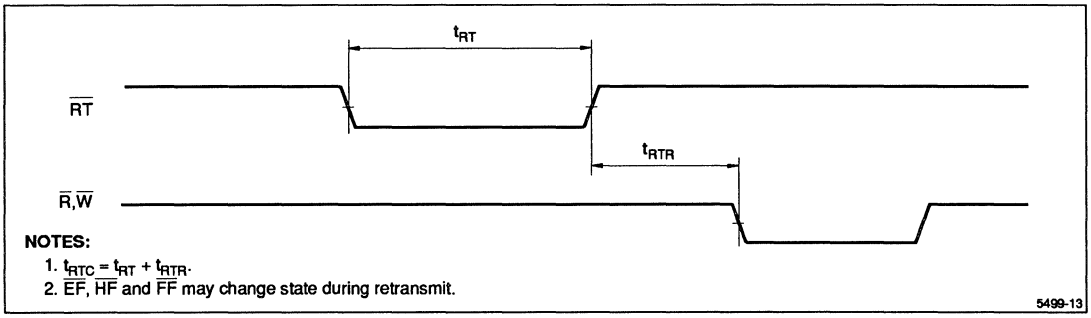
5499-11

Figure 11. Full Flag Timing



5499-12

Figure 12. Half-Full Flag Timing



NOTES:
1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit.

5499-13

Figure 13. Retransmit Timing

TIMING DIAGRAMS (cont'd)

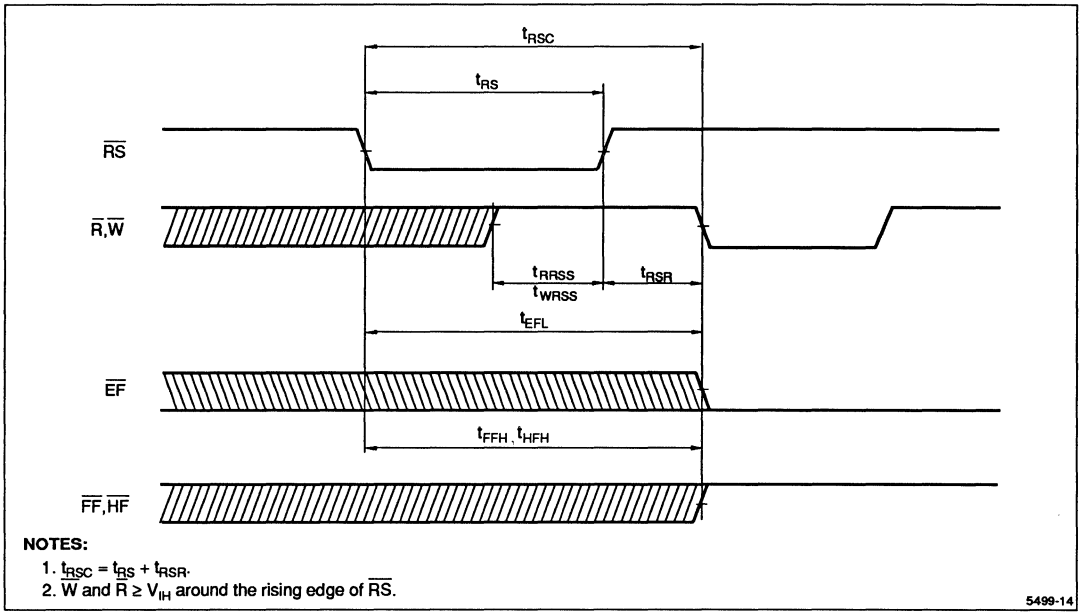


Figure 14. Reset Timing

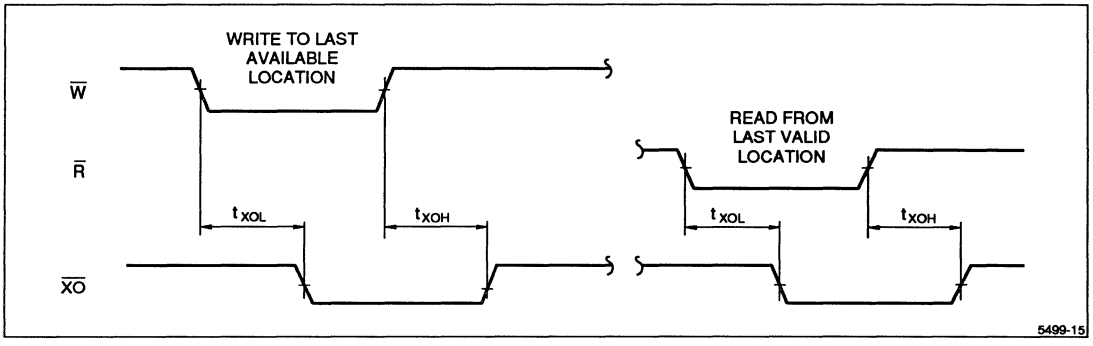


Figure 15. Expansion Out Timing

TIMING DIAGRAMS (cont'd)

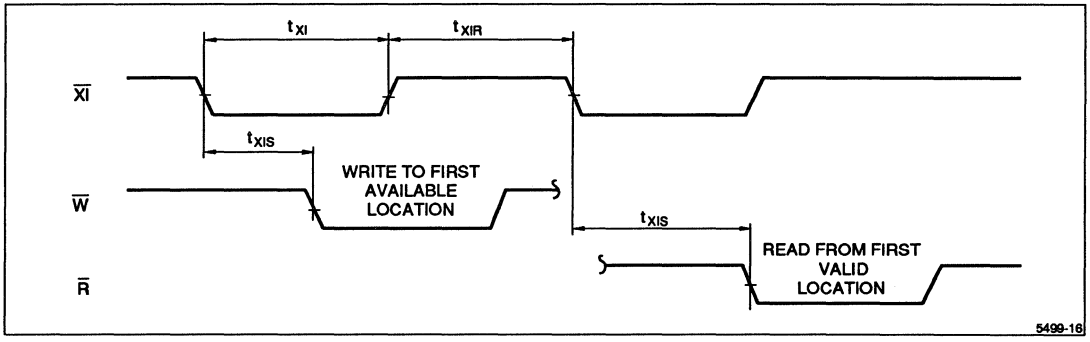


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in SINGLE mode by tying the EXPANSION IN pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word width expansion is implemented by placing multiple devices in parallel. Each device should be configured for SINGLE mode. In this arrangement, the behavior of the status flags will be identical for all devices, so these flags may be derived from any one device.

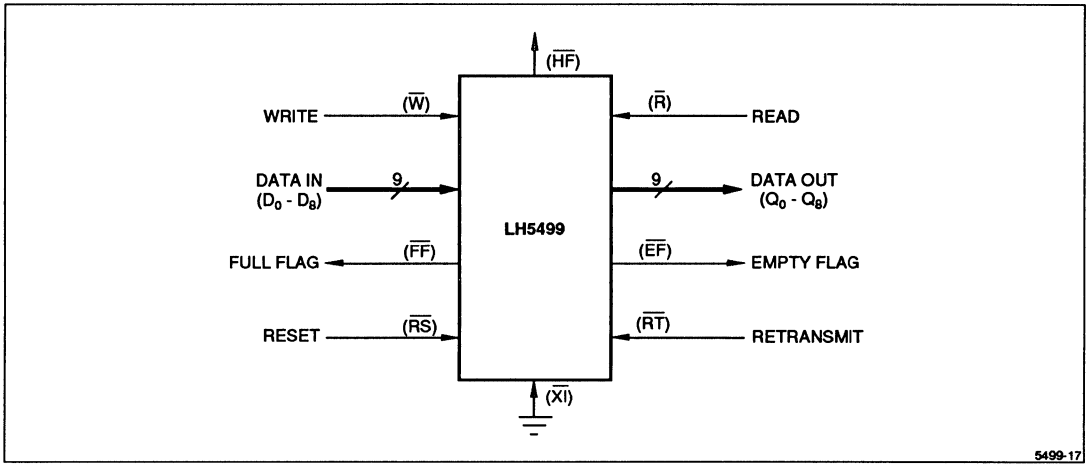


Figure 17. Single FIFO (4K × 9)

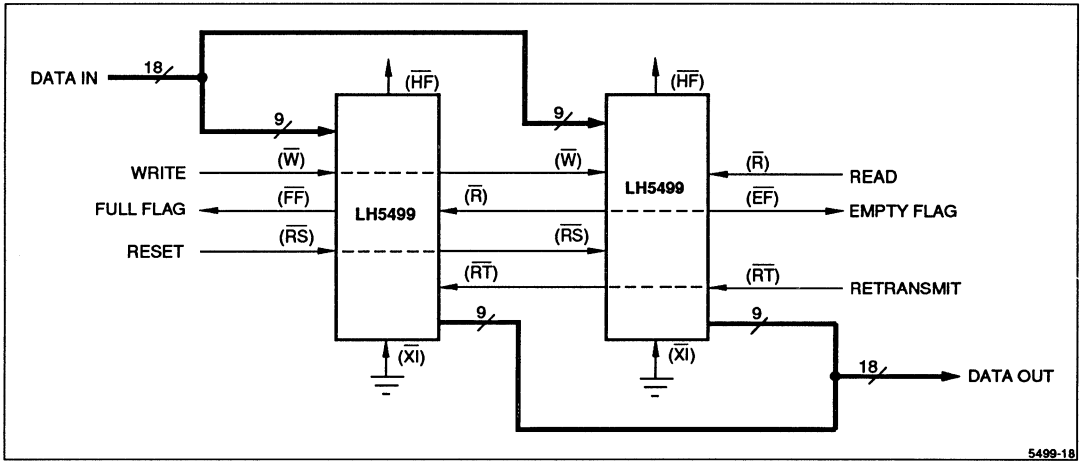


Figure 18. FIFO Width Expansion (4K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in EXPANSION mode. In this arrangement, the FIFOs are connected in a circular fashion with the EXPANSION OUT pin ($\overline{XO}$) of each device tied to the EXPANSION IN pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the FIRST LOAD pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In EXPANSION mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The HALF flag and RETRANSMIT functions are not available in DEPTH EXPANSION mode.

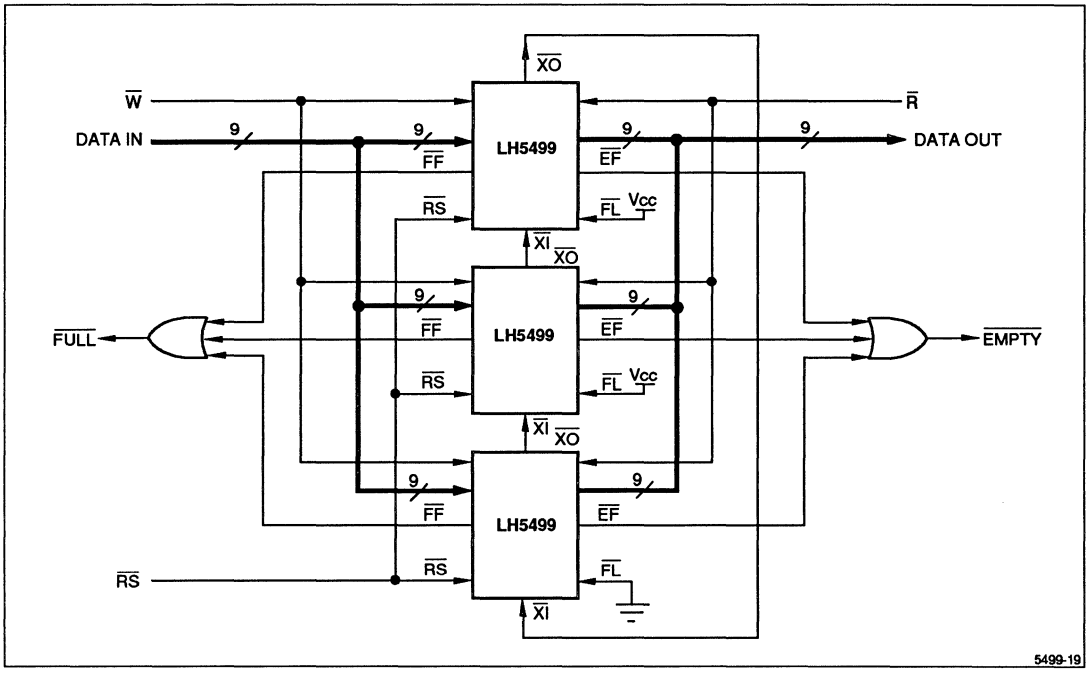


Figure 19. FIFO Depth Expansion (12288 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5499 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

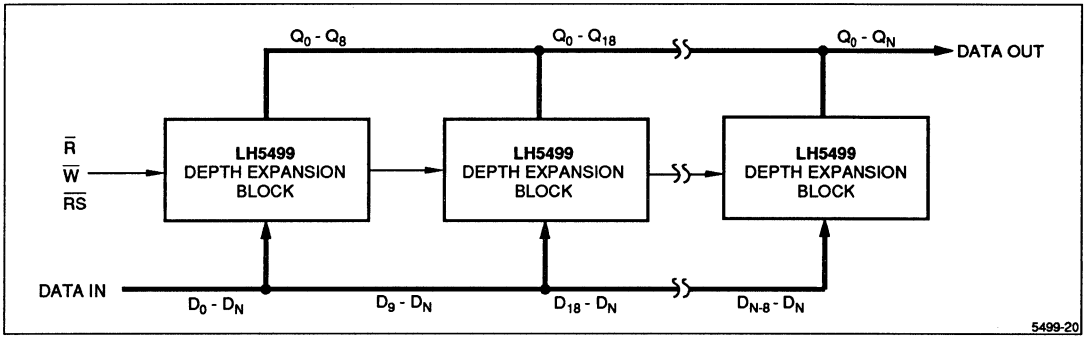


Figure 20. Compound FIFO

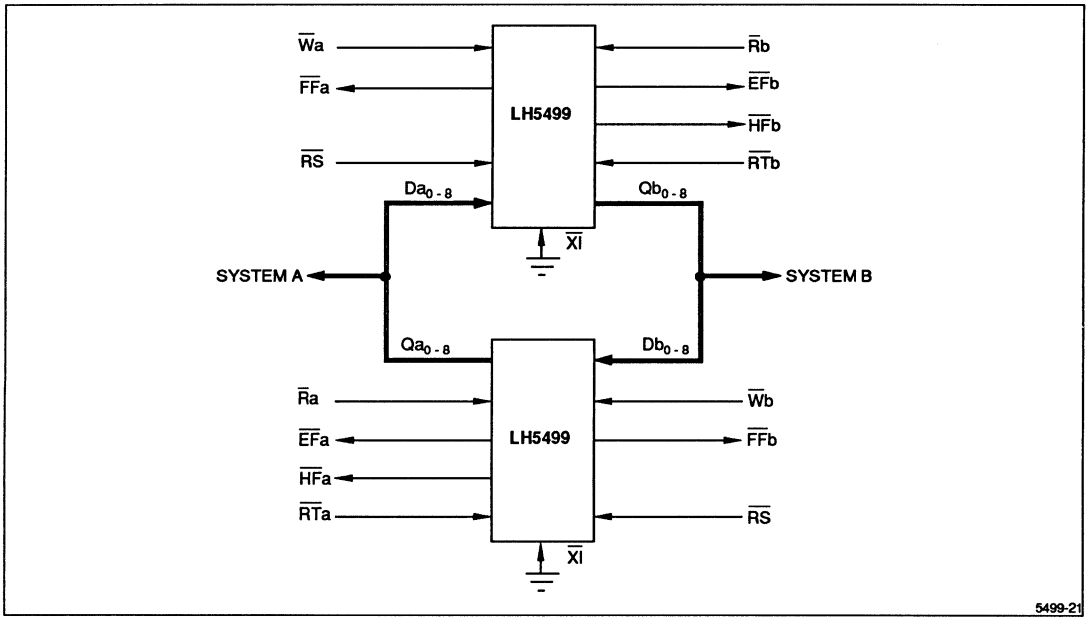
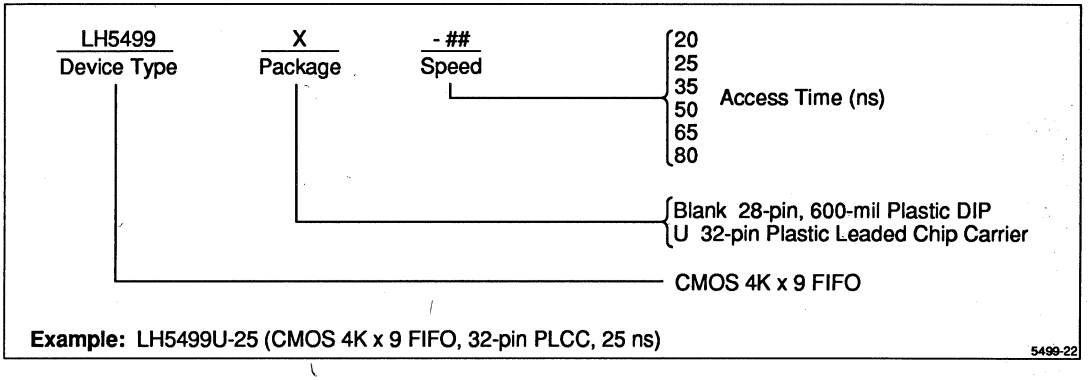


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5492

4K × 9 Clocked FIFO

FEATURES

- Fast Cycle Times: 25/35/50 ns
  Frequency: 40/28.5/20 MHz
- Parallel Data In; Parallel Data Out
- Two Read Enable Inputs and Two Write Enable Inputs, Sampled on Rising Edge of the Appropriate Clock
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM Technology, 4096 × 9
- Independently-Synchronized Operation of Input Port and Output Port
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Three-State Outputs with Output Enable
- May be Used for Bidirectional Bus Interfaces
- May be Used to Interface between Buses of Different Word Widths
- Reset/Reread Capability
- TTL and CMOS Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5492 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port RAM technology, capable of containing up to 4096 9-bit words. A single LH5492 FIFO can input and output 9-bit bytes; it has one 9-bit parallel input (write) port, and one 9-bit parallel output (read) port. Multiple write enables and read enables support paralleling LH5492s for greater-word-width operation, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5492 combination remains capable of performing all of the operations which a standalone LH5492 can perform. Thus, if two LH5492s are paralleled, the combination can input and output 18-bit halfwords. This paralleling scheme extends to an *arbitrary* number of paralleled LH5492s, although some external logic is required for more than two.

The LH5492 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either absolutely full or else absolutely empty.

Two edge-sampled enable control inputs, WEN_1 and WEN_2, are provided for the input port; and two more such control inputs, REN_1 and REN_2, are provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5492 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN_1 or to WEN_2, and the Empty flag likewise may be tied directly to REN_1 or REN_2, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 10.)

PIN CONNECTIONS

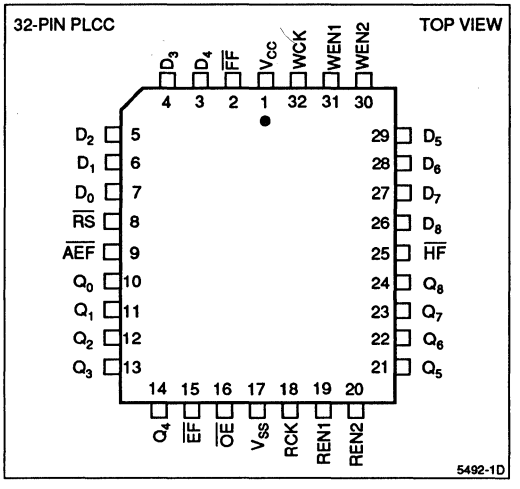


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

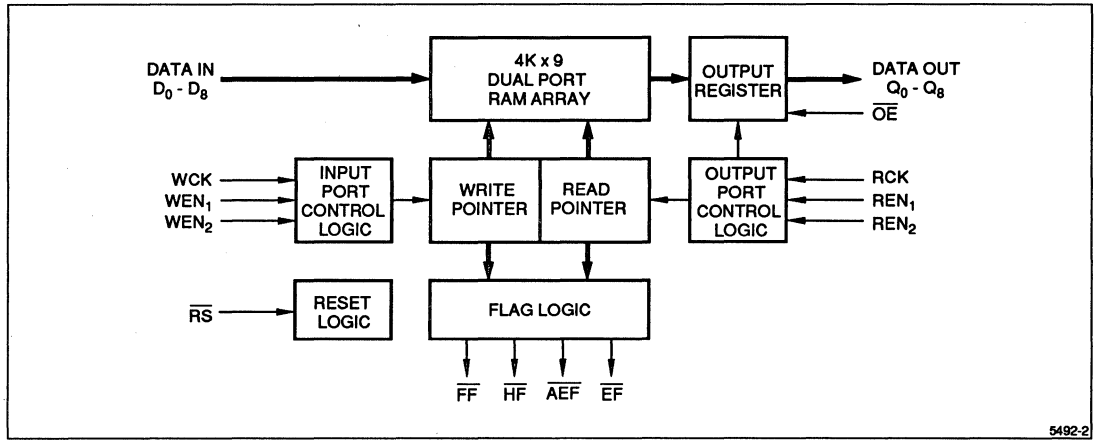


Figure 2. LH5492 Block Diagram

SIGNAL/PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for write operations.
RCK	Read Clock. A free-running clock input for read operations.
$D_0 - D_8$	Data Inputs. $D_0 - D_8$ are sampled on the rising edge of WCK, whenever both WEN_1 and WEN_2 are being asserted.
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever both REN_1 and REN_2 are being asserted.
WEN_1	Write Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
WEN_2	Write Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
REN_1	Read Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
REN_2	Read Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.
$\overline{OE}$	Output Enable. An assertive-LOW signal which places the data outputs $Q_0 - Q_8$ in a low- impedance state.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1. 5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

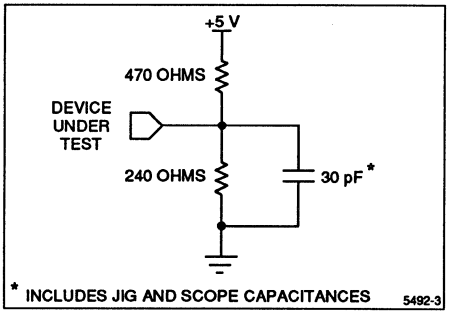


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_O (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-35		-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	28.5	–	20	MHz
t_{WC}	Write Clock Cycle Time	25	–	35	–	50	–	ns
t_{WH}	Write Clock High Time	10	–	14	–	20	–	ns
t_{WL}	Write Clock Low Time	10	–	14	–	20	–	ns
t_{RC}	Read Clock Cycle Time	25	–	35	–	50	–	ns
t_{RH}	Read Clock High Time	10	–	14	–	20	–	ns
t_{RL}	Read Clock Low Time	10	–	14	–	20	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	15	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	2	–	ns
t_{ES}	Enable Setup Time to Rising Clock	10	–	10	–	15	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	2	–	ns
t_A	Data Output Access Time	–	20	–	25	–	35	ns
t_{OH}	Output Hold Time (from rising RCK)	5	–	5	–	5	–	ns
t_{OL}	$\overline{OE}$ to Data Outputs Low-Z [2]	1	–	1	–	1	–	ns
t_{OZ}	$\overline{OE}$ to Data Outputs High-Z [2]	–	10	–	12	–	15	ns
t_{OE}	Output Enable to Data Valid	–	10	–	12	–	15	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	25	–	35	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	25	–	35	ns
t_{HF}	Clock to Half Flag Valid	–	35	–	40	–	45	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	40	–	45	ns
t_{RS}	Reset Pulse Width	25	–	35	–	50	–	ns
t_{RSS}	Reset Setup Time	10	–	15	–	25	–	ns
t_{RF}	Reset Low to Flag Valid	–	30	–	35	–	40	ns
t_{RQ}	Reset to Data Outputs Low	–	20	–	25	–	30	ns
t_{FRL}	First Read Latency	18	–	20	–	20	–	ns
t_{FWL}	First Write Latency	18	–	20	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN_1 and WEN_2 are both being asserted, or else a rising edge of RCK occurs while REN_1 and REN_2 are both being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Write and/or read operations need not be deactivated during a reset operation, but failure to do so requires observance of the Reset Setup Time (t_{RSS}) to assure that the first write and/or first read following reset will occur predictably.

If no read operations have been performed following a reset operation, then the previous data word being held in the output register consists of all zeroes. This data word will be seen on the output bus ($Q_0 - Q_8$) whenever the output enable ($\overline{OE}$) is being held LOW.

Write

A write operation consists of storing parallel data from the data inputs to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both of the edge-sampled Write Enable inputs (WEN_1 and WEN_2) are held HIGH for the prescribed setup times and hold times. Setup times and hold times must also be observed for the Data In pins (D_0–D_8).

When a full condition is reached, write operations should be ceased in order to prevent overwriting unread data. The state of the four status flags has no direct effect on write operations; that is, the execution of write operations is gated only by WEN_1 and WEN_2, and the internal logic of the LH5492 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 10 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location becomes freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The next write operation should begin no earlier than a First Write Latency time (t_{FWL}) after the first read operation from a full FIFO, in order to assure that a correct data word is written into the FIFO memory.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK), whenever both of the edge-sampled Read Enable inputs (REN_1 and REN_2) are held HIGH for the prescribed setup times and hold times. Read data becomes valid on the Data Out pins ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK, provided that the Output Enable ($\overline{OE}$) is being held LOW. $\overline{OE}$ is an assertive-LOW asynchronous input. When $\overline{OE}$ is taken LOW, the $Q_0 - Q_8$ outputs are driven (i.e., are in a low-Z state) within a minimum time t_{OL}. When $\overline{OE}$ is taken HIGH, the $Q_0 - Q_8$ outputs are in a high-Z state within a maximum time t_{OZ}.

When an empty condition is reached, read operations should be ceased until a valid write operation(s) has loaded additional data into the FIFO. The state of the four status flags has no direct effect on read operations; that is, the execution of read operations is gated only by REN_1 and REN_2, and the internal logic of the LH5492 itself has no interlock to prevent underrunning valid data after the internal read pointer 'wraps around' and catches up to the write pointer – and passes it, if reading is continued. Figure 10 illustrates how such an interlock may be implemented by means of external connections.

Following the first write to an empty FIFO, the Empty Flag ($\overline{EF}$) is deasserted ($\overline{EF}$ = HIGH). The next read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write operation into an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

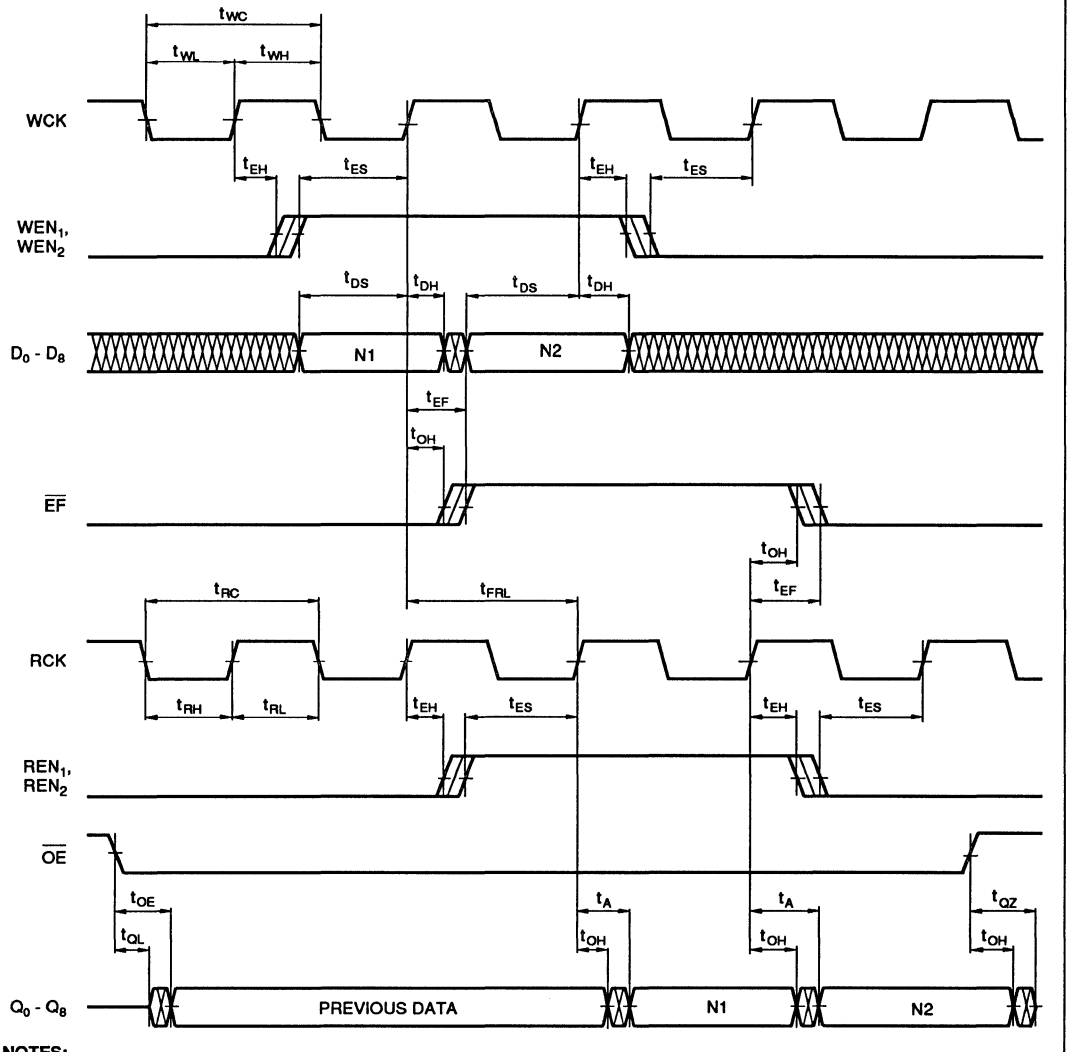
Status Flags are included for Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1. Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

The FIFO can be made to reread previously read data through a reset operation, which initializes the internal read-address and write-address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 data words which previously had been written into and/or read from the FIFO still then remain in the FIFO memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data words are being written to the FIFO following the reset operation.

TIMING DIAGRAMS



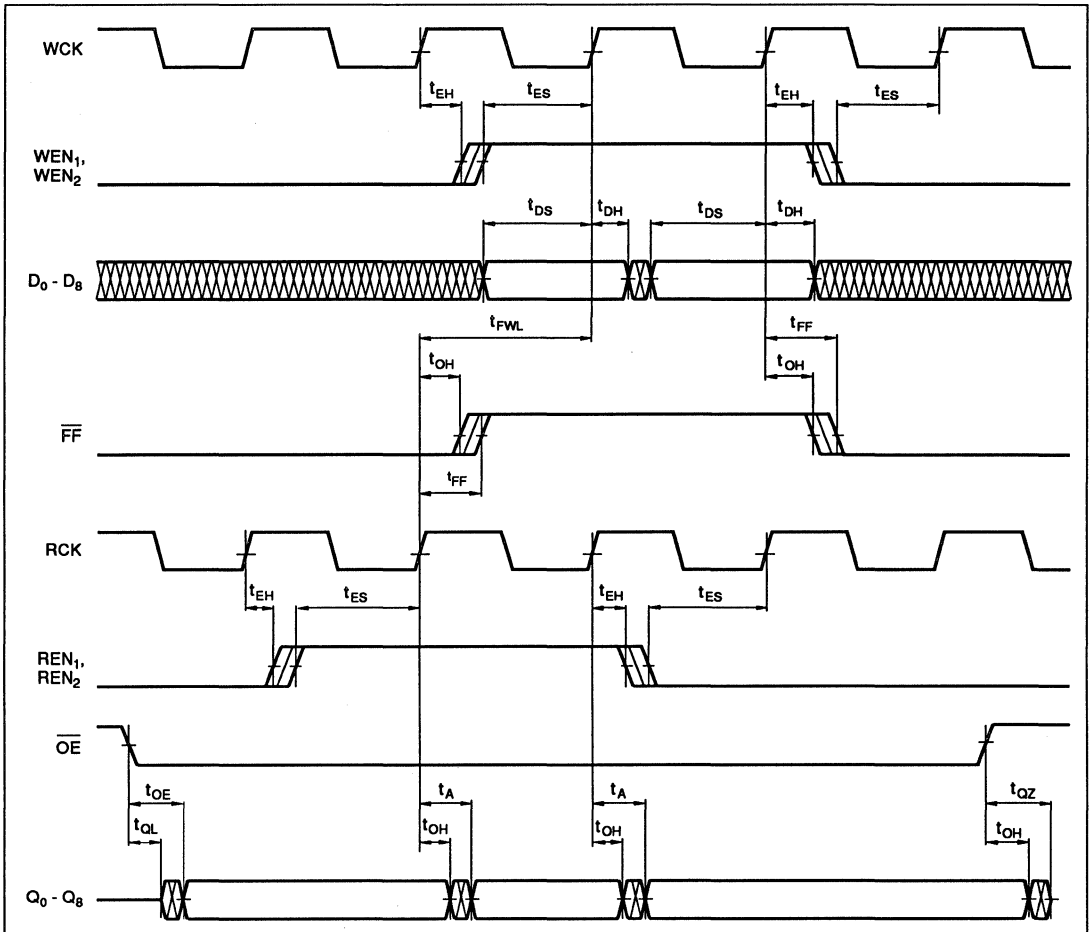
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ asserted (LOW) does not prevent further read operations, unless it is tied either to REN_1 or to REN_2.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to assure valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.
5. Immediately following a reset operation, the 'previous data' will be all bits LOW.

5492-4

Figure 4. Write and Read Operation in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



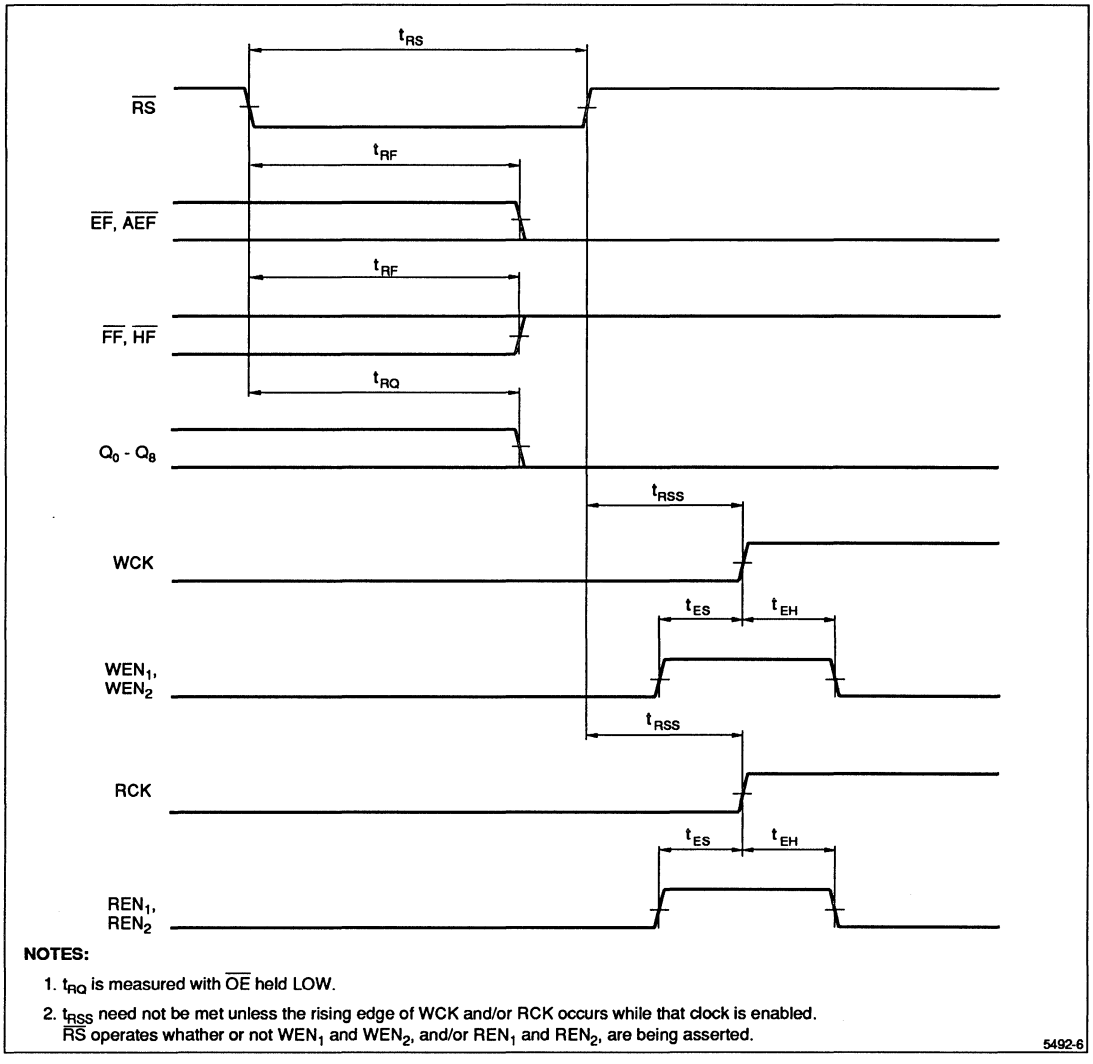
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ asserted (LOW) does not prevent further write operations, unless it is tied either to WEN_1 or to WEN_2.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5492-5

Figure 5. Read and Write Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. t_{RQ} is measured with $\overline{OE}$ held LOW.
2. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN_1 and WEN_2, and/or REN_1 and REN_2, are being asserted.

5492-6

Figure 6. Reset Timing

TIMING DIAGRAMS (cont'd)

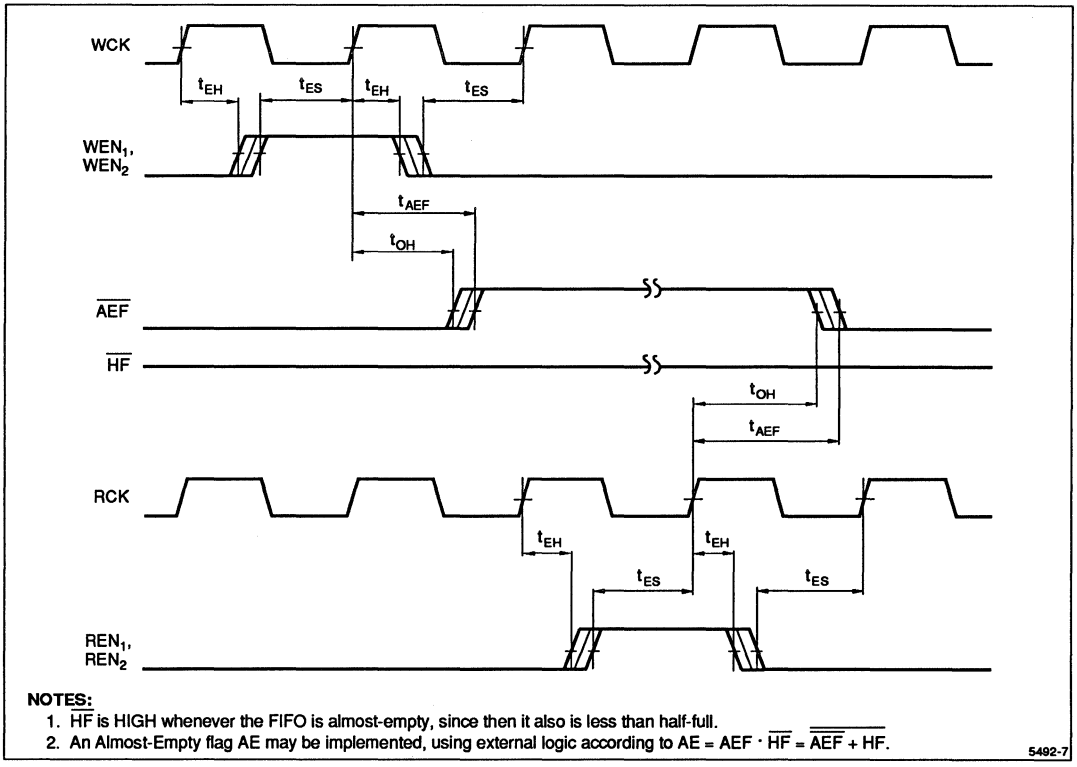


Figure 7. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	AEF	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2047
1	1	0	1	8	2047	2048	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

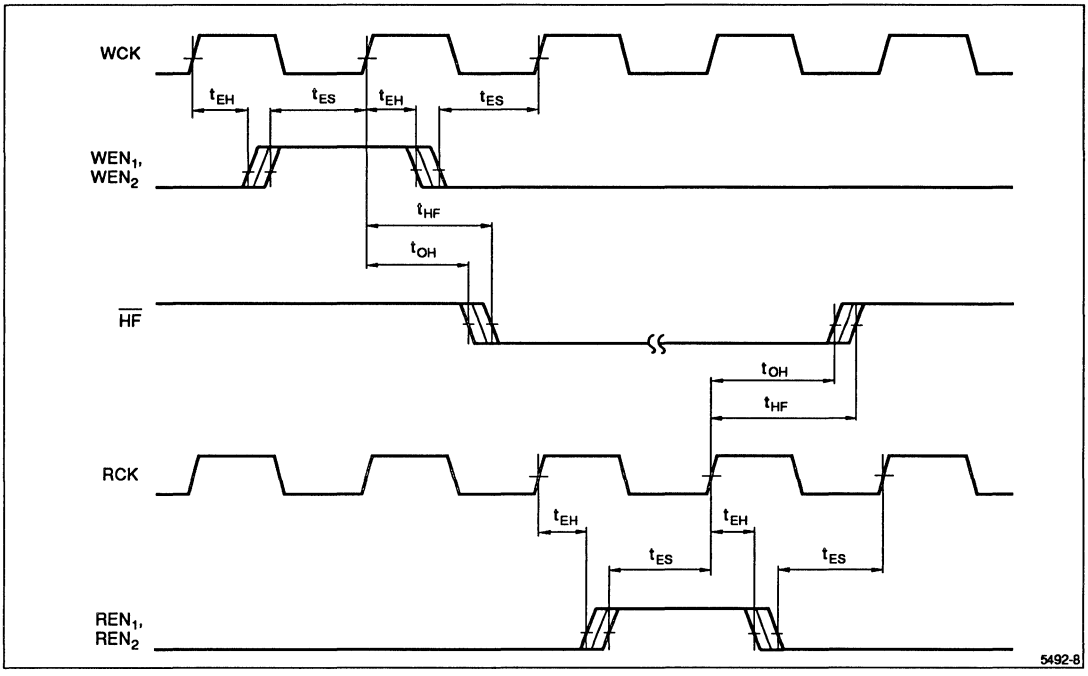
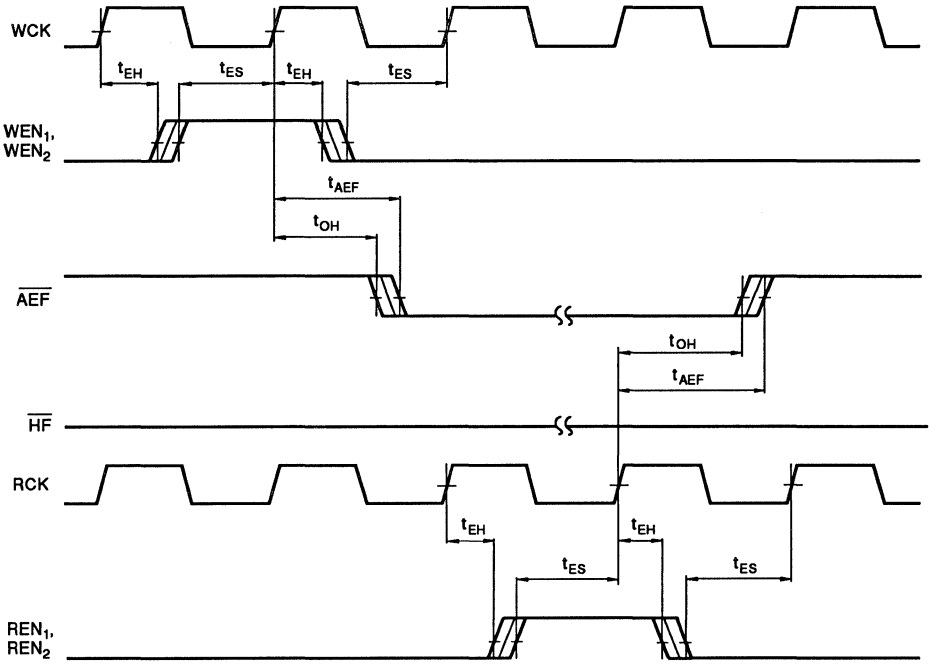


Figure 8. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to $AF = AEF \cdot HF = \overline{\overline{AEF} + \overline{HF}}$.

5492-9

Figure 9. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Read and Write Operations

Read and Write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. In this case, the Write Enable (WEN_1 and WEN_2) and Read Enable (REN_1 and REN_2) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the WEN_1, WEN_2, REN_1, and REN_2 inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to either WEN_1 or WEN_2, to prevent 'overrun' write operations when the full condition is reached, while the other Write Enable input remains available for system control. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to either REN_1 or REN_2, to prevent 'underrun' read operations when the empty condition is reached, while the other Read Enable input remains available for system control.

Asynchronous Read and Write Operations

Write operations and read operations also may be performed completely asynchronously, relative to each other, when the WCK input and the RCK input are derived from the clock signals of *different* systems. Under these conditions, the status-flag transitions occur relative to two unpredictably-related clock edges; and so, these flags should not be used to directly drive Write Enable or Read Enable inputs, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user, in order to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underruning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

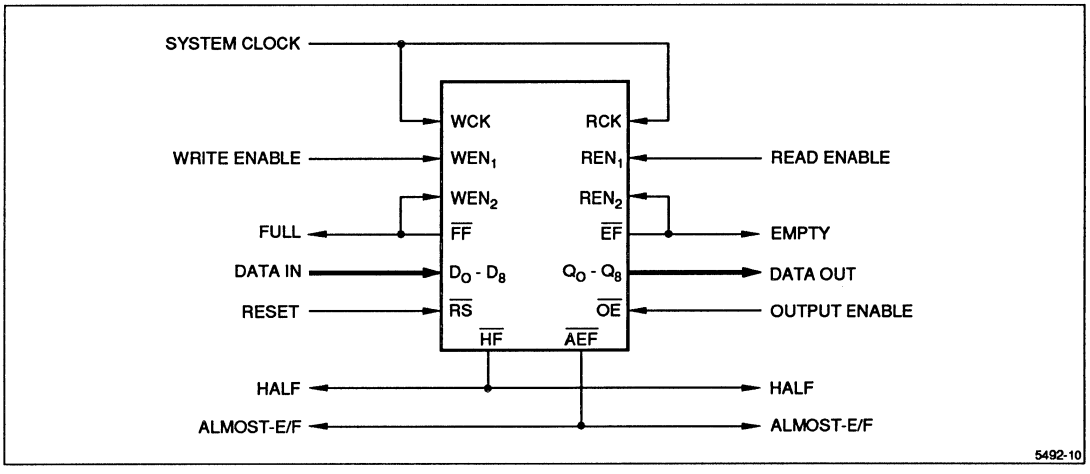


Figure 10. Synchronous Operation

OPERATIONAL MODES (cont'd)

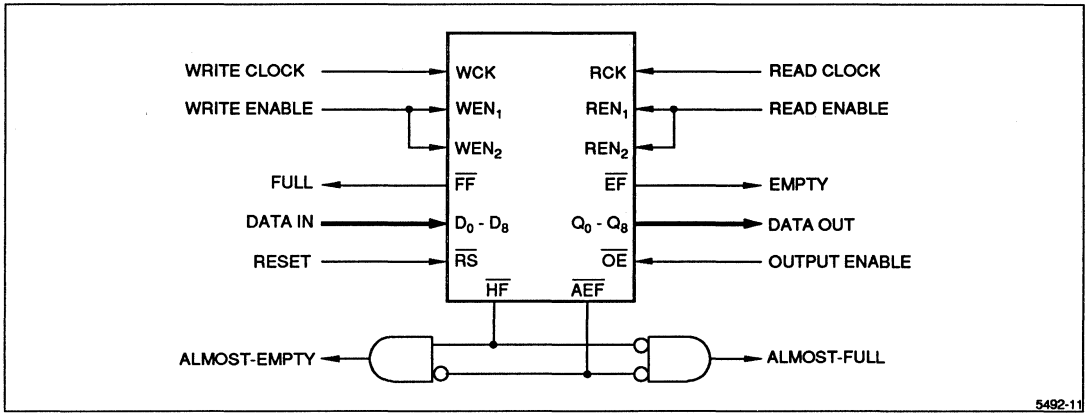


Figure 11. Asynchronous Operation

OPERATIONAL MODES (cont'd)

Depth Expansion

Increased FIFO depth may be realized by using multiple LH5492 devices. The availability of two enable control inputs for each port assists in this expansion. For either the input port or the output port, one enable input may be used for system control, while the other is driven by decode logic to direct the flow of data. Typically, this decode logic alternates accesses sequentially from one device to the next. Status flags are then derived from the last device in the sequence. The simplest form of this decode logic consists of a single toggle flipflop, which alternates access between two devices for every enabled clock cycle as shown in Figure 13.

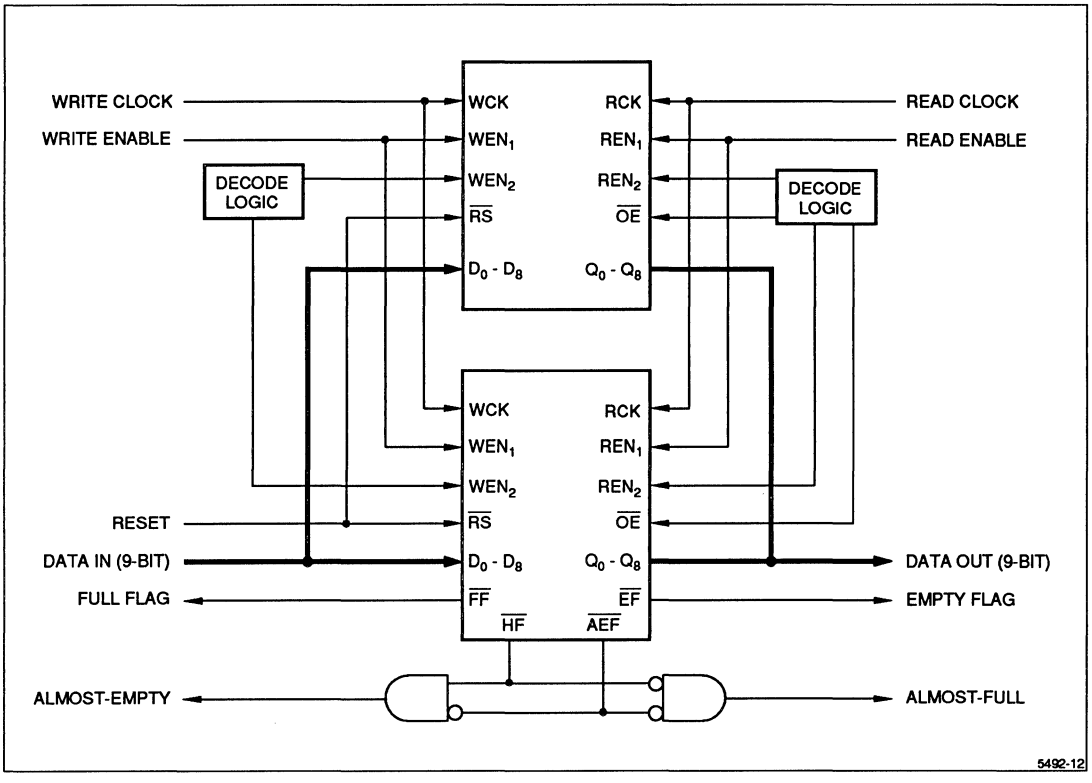


Figure 12. FIFO Depth Expansion (8192 × 9)

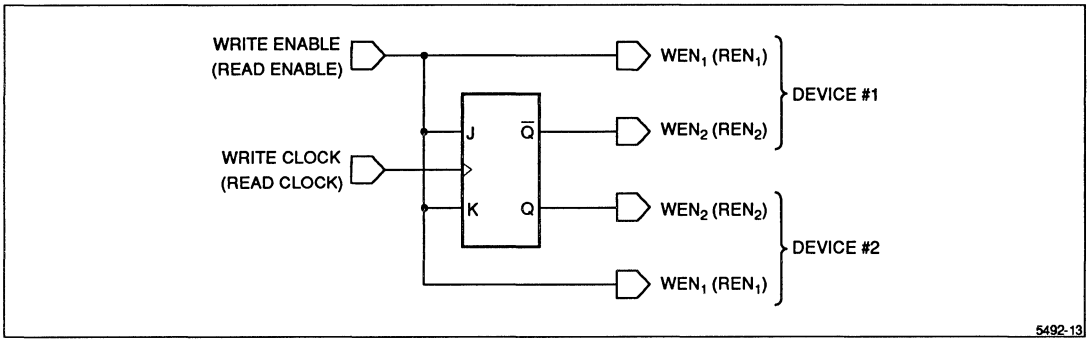


Figure 13. Simple Decode Logic

OPERATIONAL MODES (cont'd)

Interface Between Different Bus Widths

Applications which require interface between system buses of different word widths also may be implemented with multiple LH5492 devices. Essentially, one port may be configured for greater FIFO depth, while the other port is configured for greater word width. Referring to Figures 14 and 15, the wide-word port accesses data simultaneously from multiple devices, while the narrow-word port uses decode logic to direct the flow of data between two or more devices.

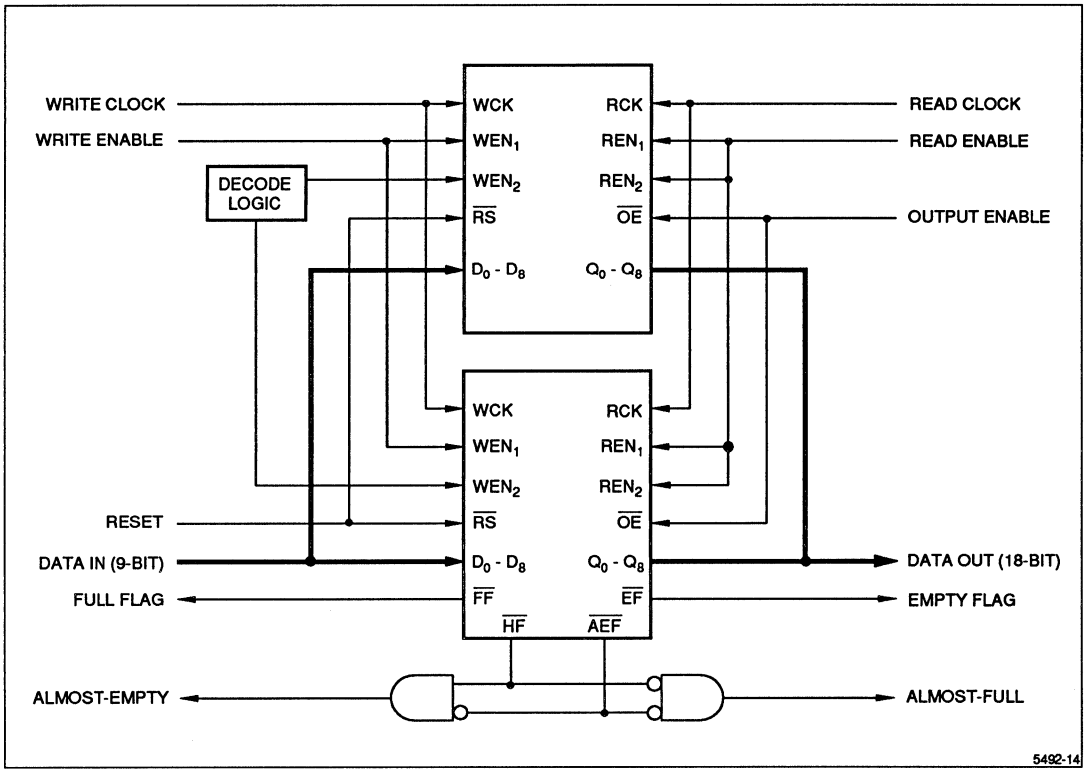


Figure 14. 8K × 9-Bit to 4K × 18-Bit Bus

OPERATIONAL MODES (cont'd)

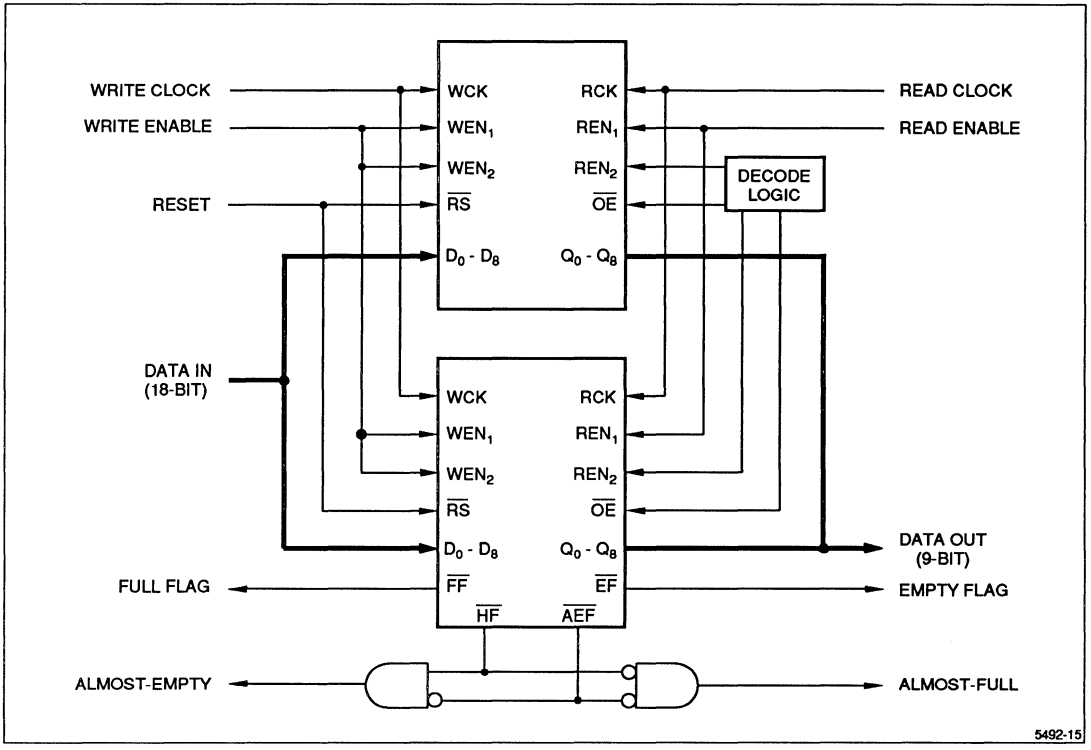


Figure 15. 4K × 18-Bit to 8K × 9-Bit Bus

OPERATIONAL MODES (cont'd)

Bidirectional Operation

Applications which require bidirectional data buffering between two systems may be realized by operating LH5492 devices in parallel, but in opposite directions. The Data In pins of one device may be tied to the corresponding Data Out pins of another device operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate clock, enable, and flag signals are routed to each system. The extra enable control signals may be used to extend FIFO depth, or to interface bidirectional buses of different word widths.

Width Expansion

Any of the previously described applications can be extended in word width by operating groups of these device configurations in parallel. The enable setup and hold times should be satisfied for *all* devices, in order to ensure that all width-expanded devices respond *identically* to the same sequence of events.

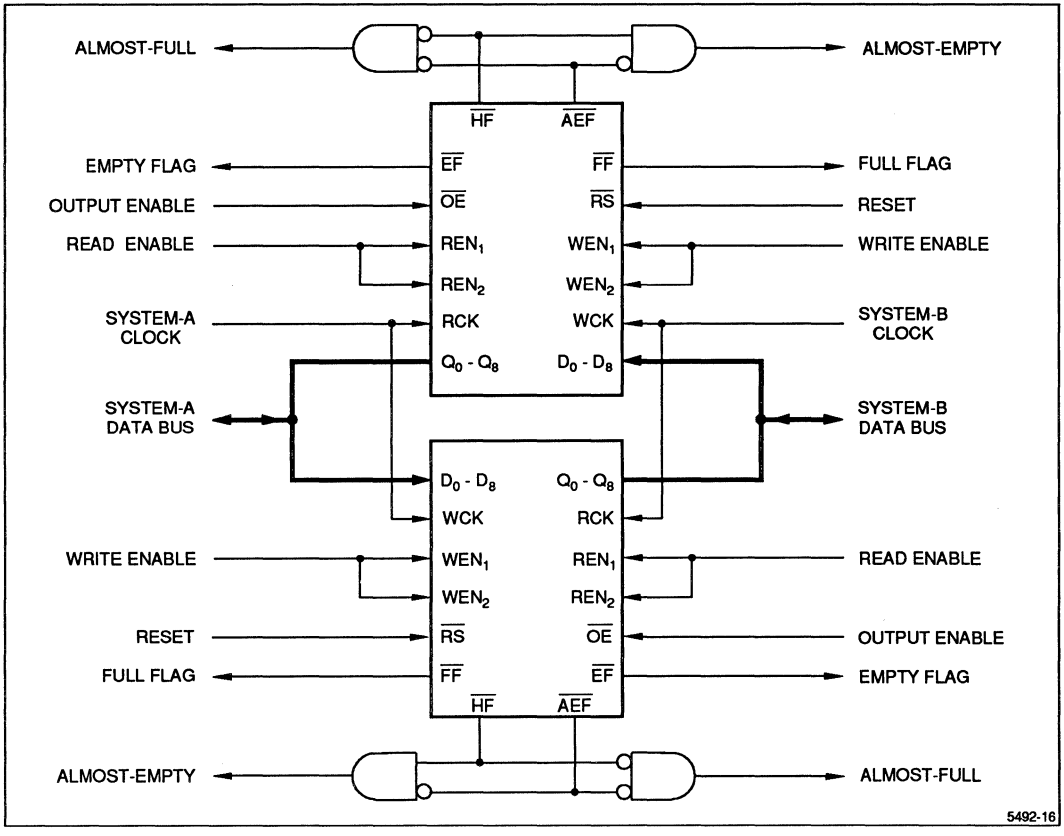
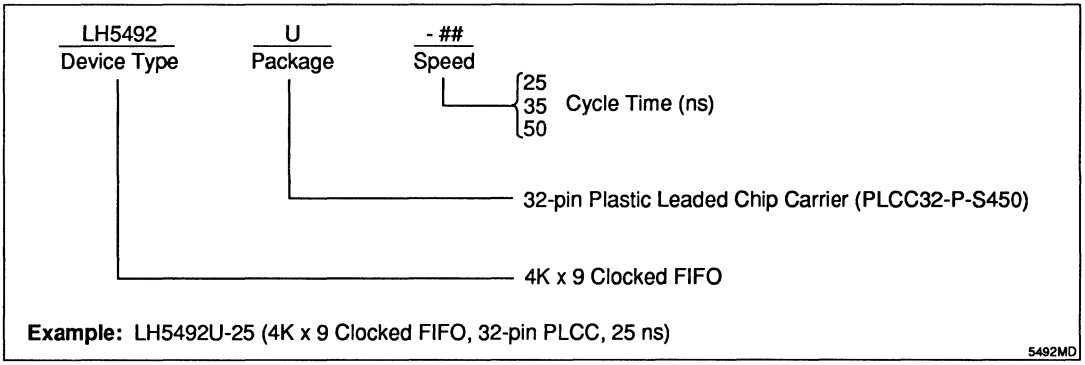


Figure 16. Bidirectional Operation

ORDERING INFORMATION



LH5493

4K × 9 Parallel-to-Serial FIFO

FEATURES

- Fast Cycle Times: 25/35/50 ns
  Frequency: 40/28.5/20 MHz
- Parallel Data In; Serial Data and/or Parallel Data Out
- Serial Input and Serial Shift Capability in Output Register, for Long-Word-Length Parallel-to-Serial Operations
- Read Enable Input and Two Write Enable Inputs, Sampled on Rising Edge of the Appropriate Clock
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM Technology, 4096 × 9
- Fully Asynchronous Read and Write Operations
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Reset/Reread Capability
- TTL/CMOS-Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5493 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 4096 9-bit words. One LH5493 FIFO can input 9-bit bytes; and it can either output 9-bit bytes in parallel, or else output a serial bitstream. Thus, a single LH5493 is capable of 9-bit-to-1-bit PISO (Parallel-In, Serial-Out) operation.

An LH5493 has one 9-bit parallel input (write) port, and one 9-bit parallel output (read) port. And there is one 1-bit serial input, which supports paralleling LH5493s for longer-word-width PISO operation. This serial input also allows additional control bits to be inserted at will into the serial output bitstream. There is no serial output port as such; *any* individual bit position in the parallel output register may be chosen as the serial-output data path, according to the desired time phase of the output bitstream.

The LH5493 architecture supports a very convenient method of *paralleling* multiple FIFOs for PISO operation, without any additional logic being needed, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5493 combination remains capable of performing all of the operations which a standalone LH5493 can perform. Thus, if two LH5493s are paralleled, the combination can input 18-bit halfwords; and it can either output 18-bit halfwords, or else output a serial bitstream for 18-bit-to-1-bit PISO operation. This paralleling scheme extends without change to an *arbitrary* number of LH5493s.

The LH5493 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either absolutely full or else absolutely empty.

Two edge-sampled enable control inputs, WEN_1 and WEN_2, are provided for the input port; and one such control input, REN, is provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5493 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

PIN CONNECTIONS

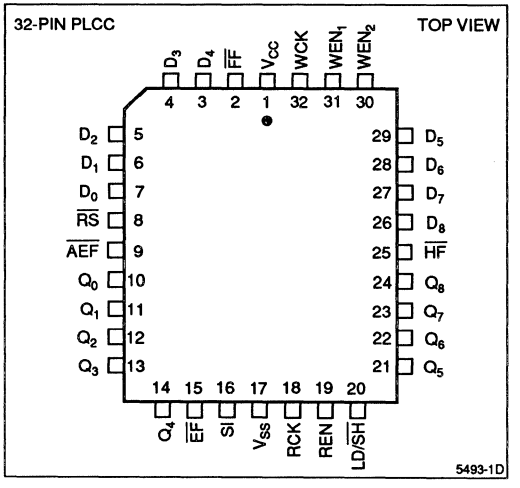


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN_1 or to WEN_2, and the Empty flag likewise may be tied directly to REN, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 11.)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

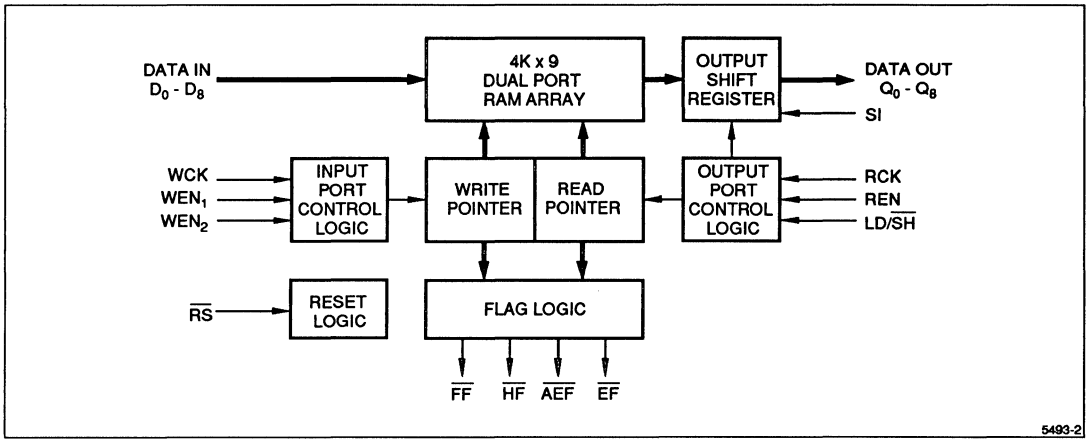


Figure 2. LH5493 Block Diagram

SIGNAL PIN |DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for write operations.
RCK	Read Clock. A free-running clock input for read operations.
SI	Serial Input. A serial data input to allow paralleled PIS0 operation of multiple devices.
$D_0 - D_8$	Data Inputs. $D_0 - D_8$ are sampled on the rising edge of WCK, whenever both WEN_1 and WEN_2 are being asserted..
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever REN is being asserted.
WEN_1	Write Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
WEN_2	Write Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
REN	Read Enable. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO.
LD/$\overline{SH}$	Read Load/Shift. An input signal which is sampled on the rising edge of RCK to control the loading or shifting of data in the output register.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at fc = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

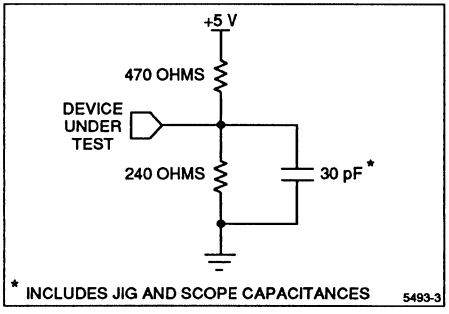


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_O (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-35		-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	28.5	–	20	MHz
t_{WC}	Write Clock Cycle Time	25	–	35	–	50	–	ns
t_{WH}	Write Clock HIGH Time	10	–	14	–	20	–	ns
t_{WL}	Write Clock LOW Time	10	–	14	–	20	–	ns
t_{RC}	Read Clock Cycle Time	25	–	35	–	50	–	ns
t_{RH}	Read Clock HIGH Time	10	–	14	–	20	–	ns
t_{RL}	Read Clock LOW Time	10	–	14	–	20	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	15	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	2	–	ns
t_{ES}	Enable Setup Time to Rising Clock	10	–	10	–	15	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	2	–	ns
t_A	Data Output Access Time	–	20	–	25	–	35	ns
t_{OH}	Output Hold Time	5	–	5	–	5	–	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	25	–	35	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	25	–	35	ns
t_{HF}	Clock to Half-Full Flag Valid	–	35	–	40	–	45	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	40	–	45	ns
t_{RS}	Reset Pulse Width	25	–	35	–	50	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	15	–	25	–	ns
t_{RF}	Reset Low to Flag Valid	–	30	–	35	–	40	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	25	–	30	ns
t_{FRL}	First Read Latency [4]	18	–	20	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	20	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN_1 and WEN_2 both are being asserted, or else a rising edge of RCK occurs while REN is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Read, shift, and/or write operations need not be deactivated during a reset operation. However, failure to do so requires observance of the Reset Setup Time (t_{RSS}), to assure that the first write and/or first read following a reset operation will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' being held in the output register and seen on the output bus ($Q_0 - Q_8$) consists of all zeroes.

Write

A write operation consists of storing parallel data from the data inputs to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both of the edge-sampled Write Enable inputs (WEN_1 and WEN_2) are held HIGH for the prescribed setup times and hold times. Setup times and hold times must also be observed for the Data In inputs ($D_0 - D_8$).

When a full condition is reached, write operations should be ceased in order to prevent overwriting unread data. The state of the status flags has no direct effect on write operations; that is, the execution of write operations is gated only by WEN_1 and WEN_2, and the internal logic of the LH5493 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location is freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, in order to ensure that correct read data is retrieved.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK), whenever both the edge-sampled Read Enable input (REN) and the Load/Shift input (LD/$\overline{SH}$) are held HIGH for the prescribed setup times and hold times. Read data becomes valid at the Data Out outputs ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK. A shift of data in the output register is performed whenever REN is held HIGH and LD/$\overline{SH}$ is held LOW on the rising edge of RCK. Data is shifted in the MSB-to-LSB direction, with data on the Serial Input (SI) replacing the contents of bit position Q_8.

When an empty condition is reached, read operations should be ceased in order to prevent underruning the actual meaningful data. The state of the four status flags has no direct effect on read or shift operations; that is, the execution of read or shift operations is gated only by REN and LD/$\overline{SH}$, and the internal logic of the LH5493 itself has no interlock to prevent underrunning valid data after the internal read pointer catches up to the write pointer – and passes it, if reading is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

When an empty condition is reached, shift operations may continue; but read operations should be ceased until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the Empty Flag will be deasserted ($\overline{EF}$ = HIGH). The first read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write to an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

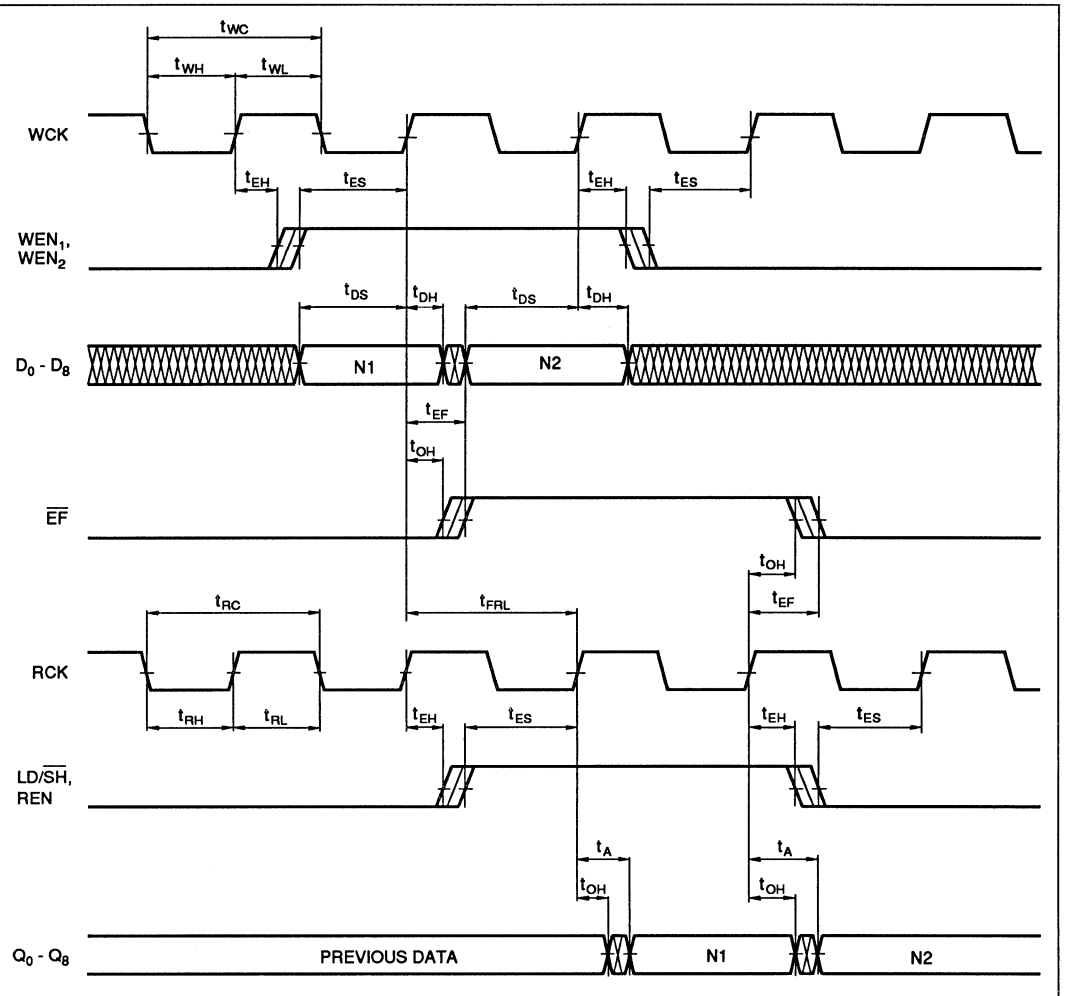
The following four status flags are included: Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated on the appropriate boundary conditions as illustrated in Figure 8. Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

The FIFO may be made to reread previously-read data by means of a reset operation, which initializes the internal read and write address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 words of old data, which previously had been written into and/or read from the FIFO, still remains in the memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data words are being written to the FIFO following the reset operation.

TIMING DIAGRAMS



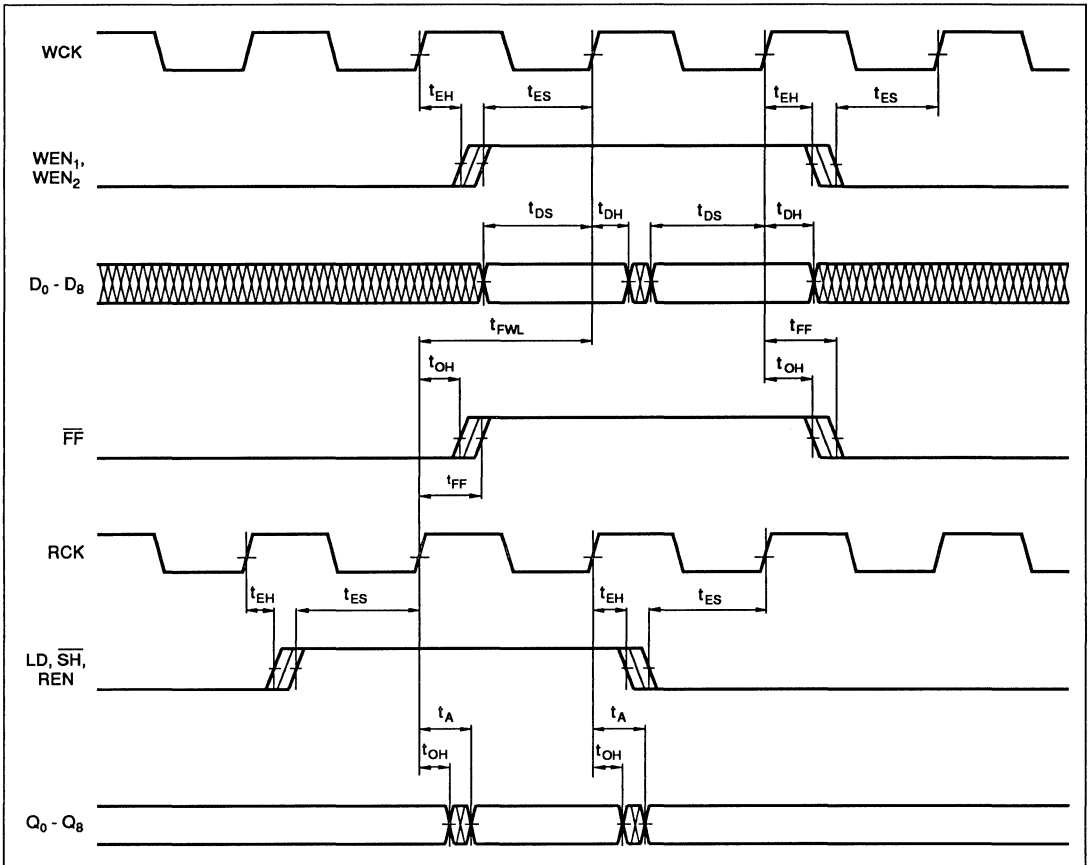
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN and LD/$\overline{SH}$ must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ being asserted (LOW) does not prevent further read operations, unless it is tied to REN.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, in order to ensure that valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.

5493-4

Figure 4. Write and Read Operation in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN and LD/$\overline{SH}$ must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ being asserted (LOW) does not prevent further write operations, unless it is tied either to WEN_1 or to WEN_2.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5493-5

Figure 5. Write and Read Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)

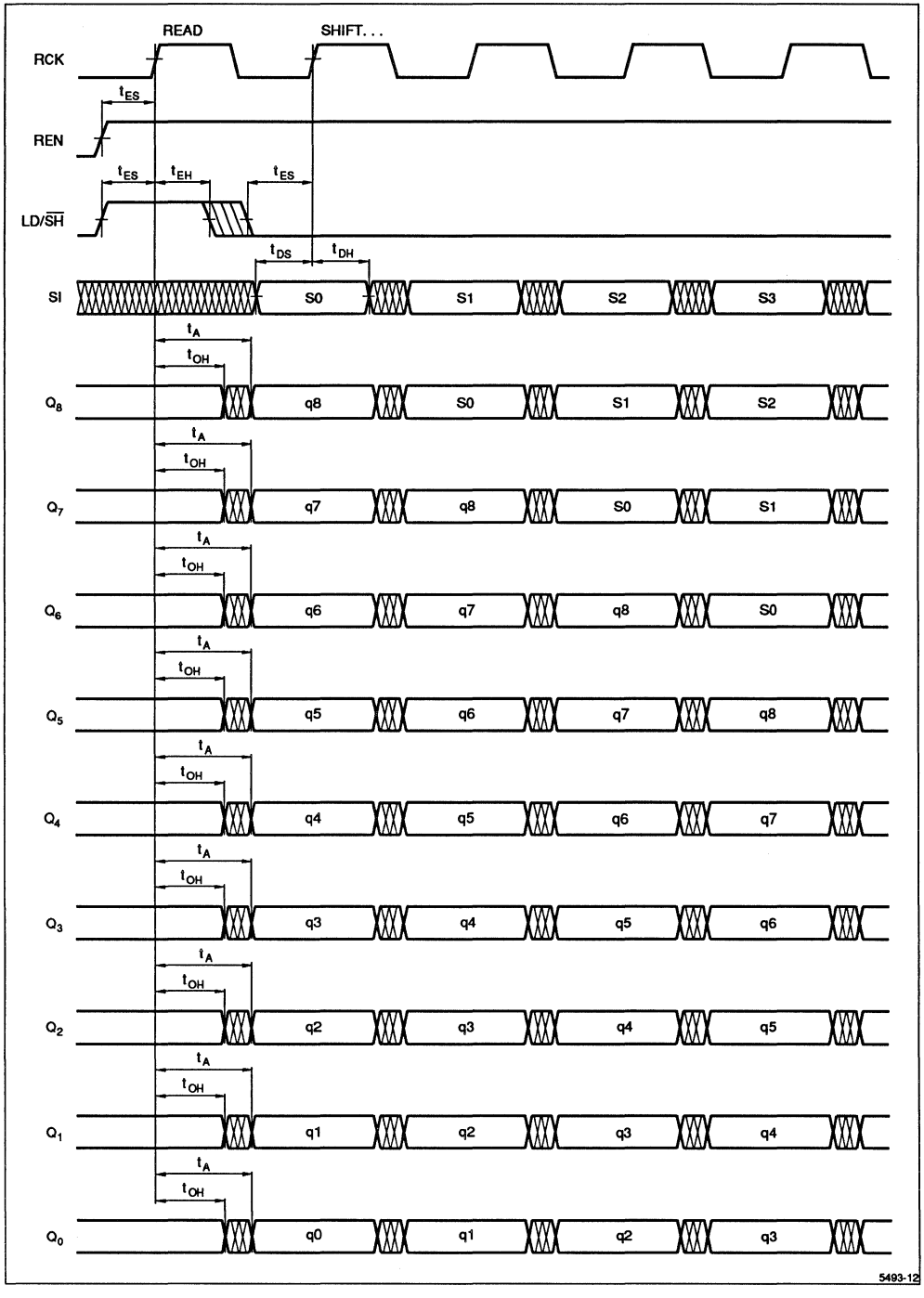
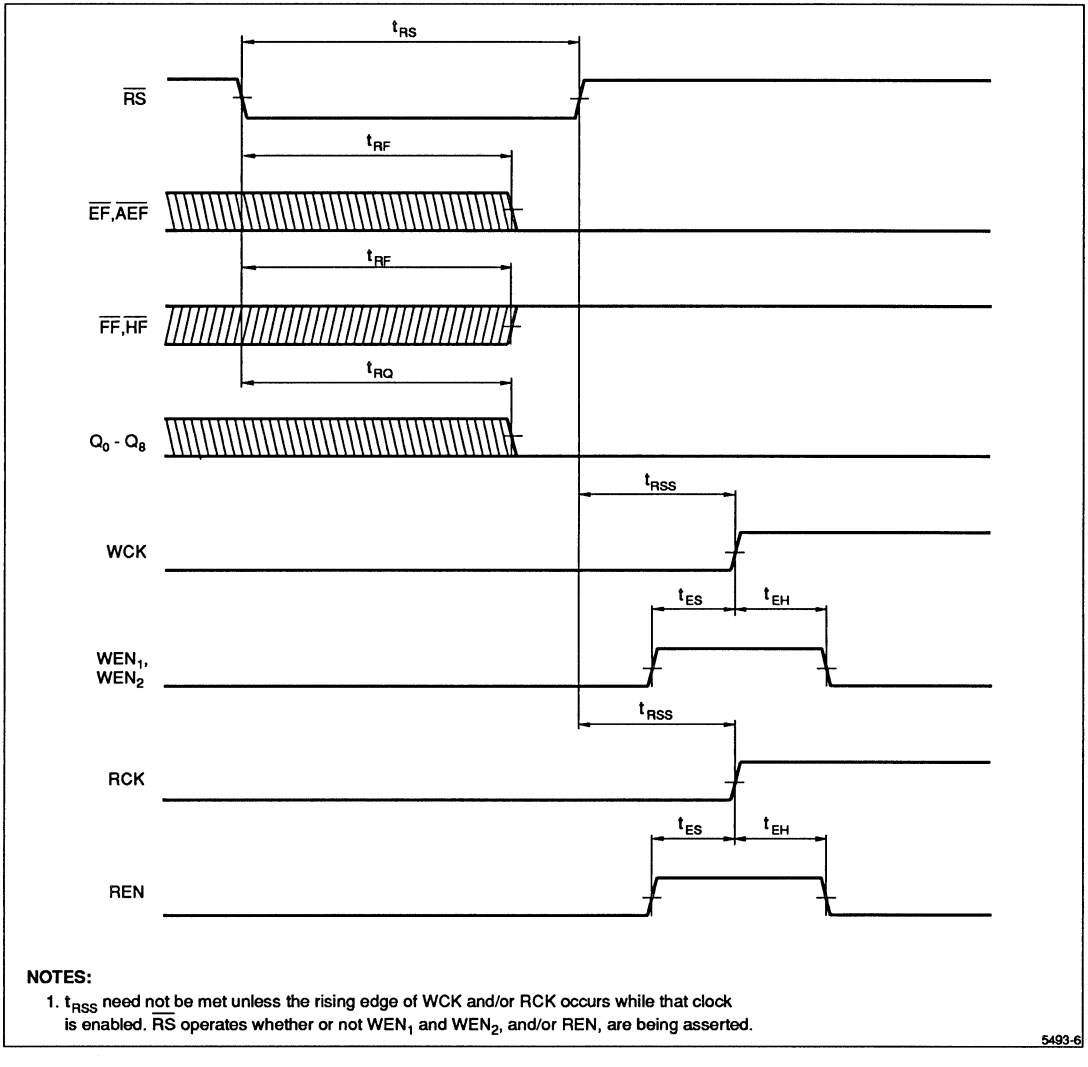


Figure 6. Serial Shift/Read Timing

TIMING DIAGRAMS (cont'd)



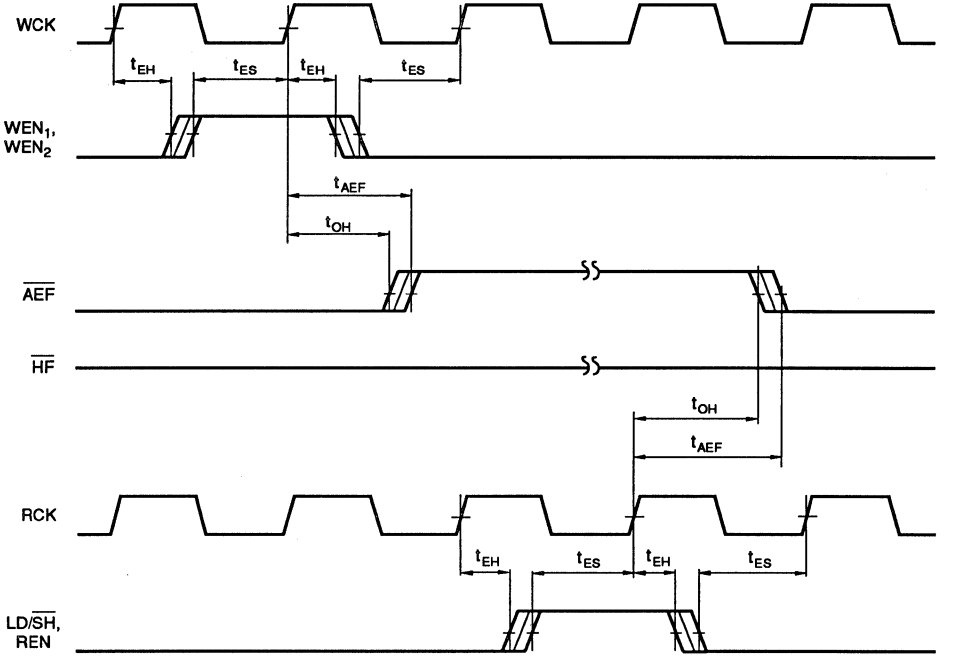
NOTES:

1. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN_1 and WEN_2, and/or REN, are being asserted.

5493-6

Figure 7. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to $AE = AEF \cdot \overline{HF} = \overline{\overline{AEF} + HF}$.

5493-7

Figure 8. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2048
1	1	0	1	8	2047	2049	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

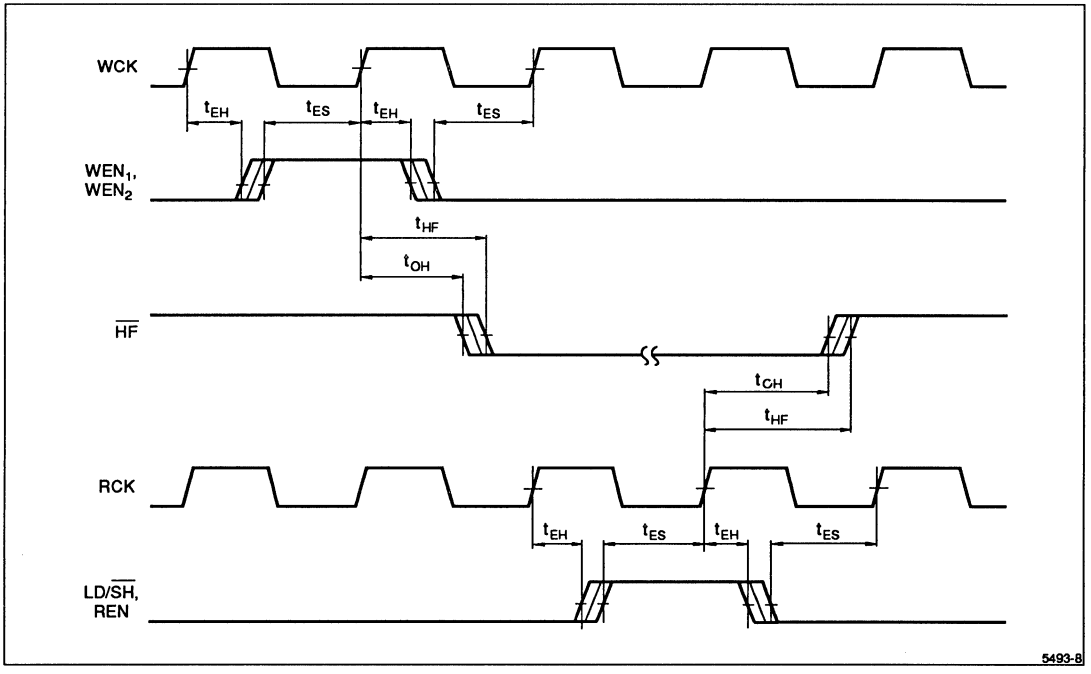
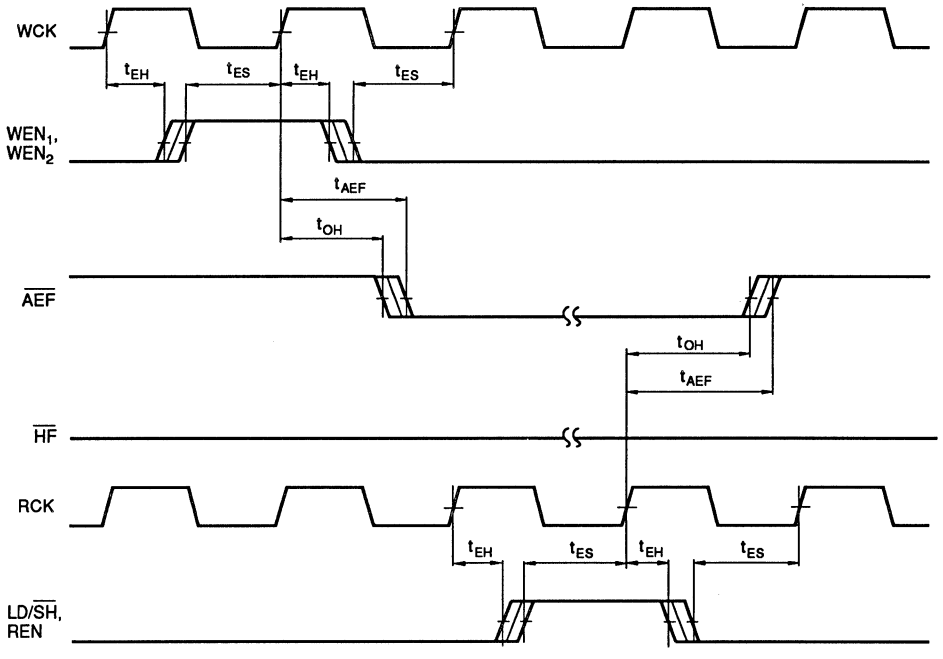


Figure 9. Half-Full Flag Timing

TIMING DIAGRAMS



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to AF = AEF · HF = $\overline{\overline{AEF} + \overline{HF}}$.

5493-9

Figure 10. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Write and Read Operations

Read and write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. In this case, the Write Enable (WEN_1 and WEN_2), Read Enable (REN), and Load/Shift ($LD/\overline{SH}$) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the WEN_1, WEN_2, and REN inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to WEN_1 or WEN_2, to prevent 'overrun' write operations after the full condition is reached, while the other Write Enable input remains available for system control. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to REN, to prevent 'underrun' read operations after the empty condition is reached.

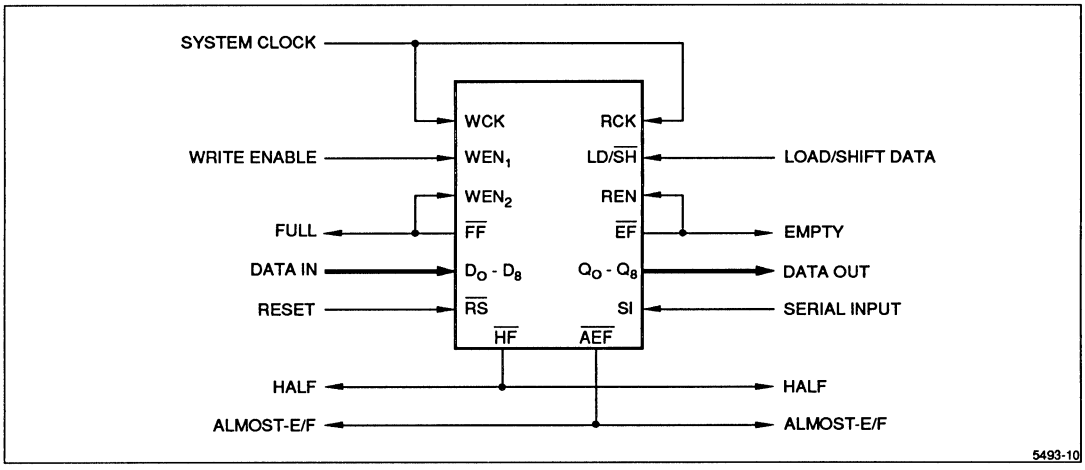


Figure 11. Synchronous Operation

OPERATIONAL MODES (cont'd)

Asynchronous Write and Read Operations

Write operations and read operations may be performed completely asynchronously with respect to each other, when the WCK input and the RCK input are derived from the clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to directly drive Write Enable or Read Enable inputs, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underrunning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

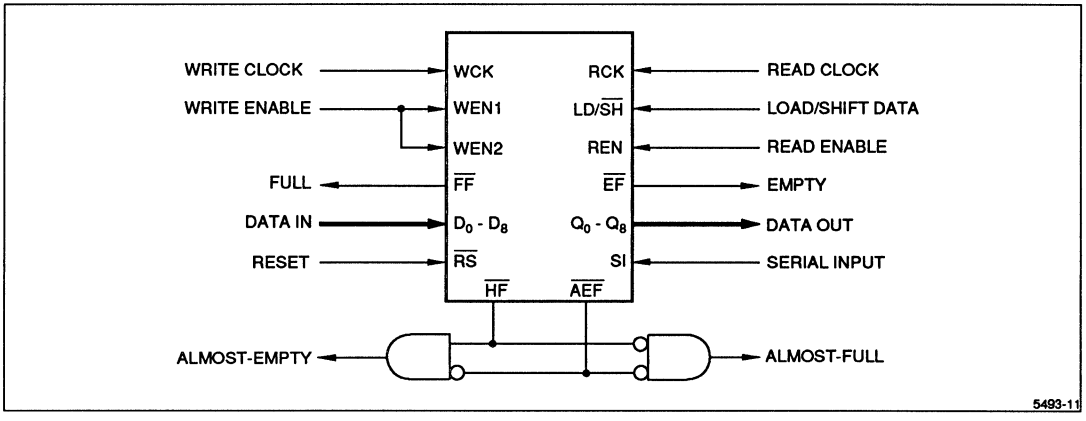


Figure 12. Asychronous Operation

OPERATIONAL MODES (cont'd)

Paralleled Operation

In paralleled operation, two or more LH5493 FIFOs are chained together into a wider 'effective FIFO.' The Serial Input (SI) of the first device in the chain serves as the 'effective-FIFO' serial input. This 'effective-FIFO' serial input may be used to insert additional control bits into the serial data stream, or may be tied to a permanent logic LOW or HIGH signal if unused. The SI input of each subsequent device is connected to one of the Data Out outputs ($Q_8 - Q_0$) of the preceding device in the chain. The final 'effective-FIFO' serial output bitstream is taken from one of the Data Out outputs of the last device in the chain. By choosing different Data Out pins, an additional one to nine bits of width can be added per device.

In 'paralleled' operation, the write enable inputs WEN_1 and WEN_2, and the read enable input REN, may be made common for all devices. Since there are multiple write enable inputs, one of them on each FIFO device may be crosscoupled to the Full Flag on another FIFO device, or to the logic AND of several such Full Flags, in order to prevent any individual FIFO device from getting out of synchronization with the overall 'effective FIFO.' The approach is analogous to the method shown in Figure 11 for preventing an LH5493 from overrunning its internal FIFO boundaries. Implementing the equivalent measures during reading always requires some external logic, since each LH5493 has just one read enable input.

Word widths do not have to be a multiple of nine. For instance, making the following changes to the circuit of Figure 13 adapts it to handle 16-bit parallel data in. The D_0 input and the Q_0 output need not be used for either LH5493. The Q_1 output of the LH5493 on the left is connected to the SI input of the LH5493 on the right; and the Q_1 output of the LH5493 on the right becomes the main 'Serial Data Out' output.

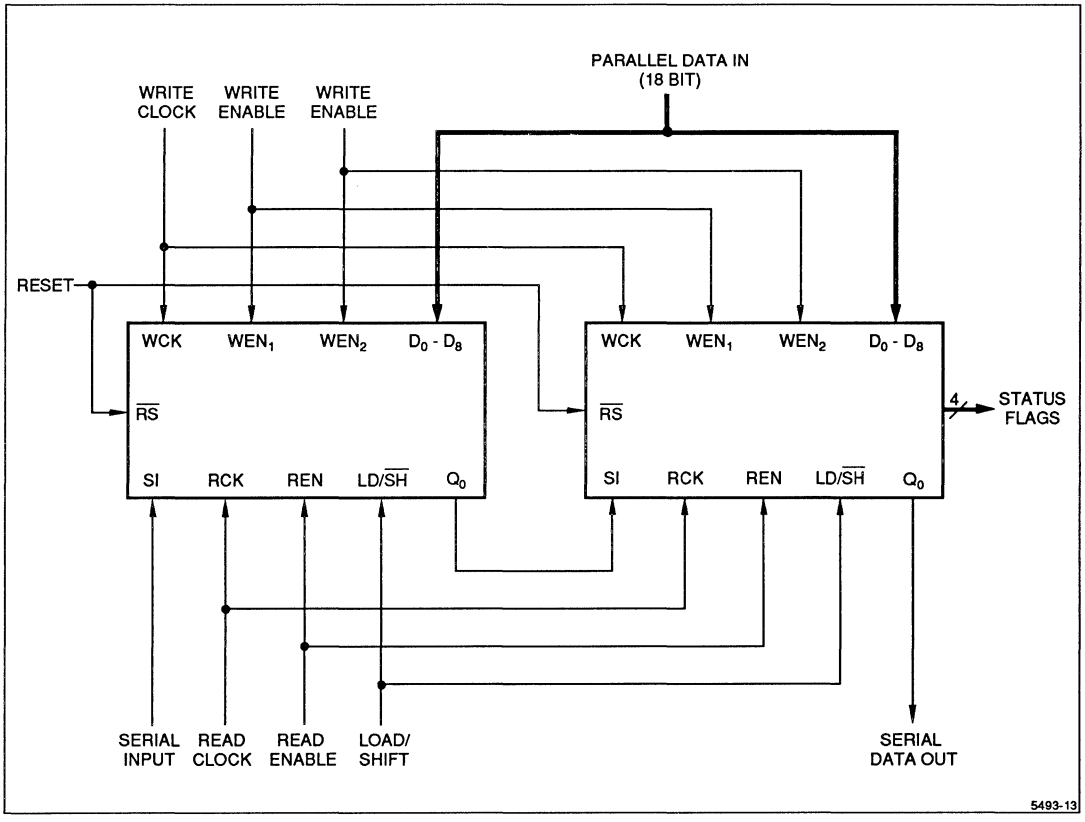
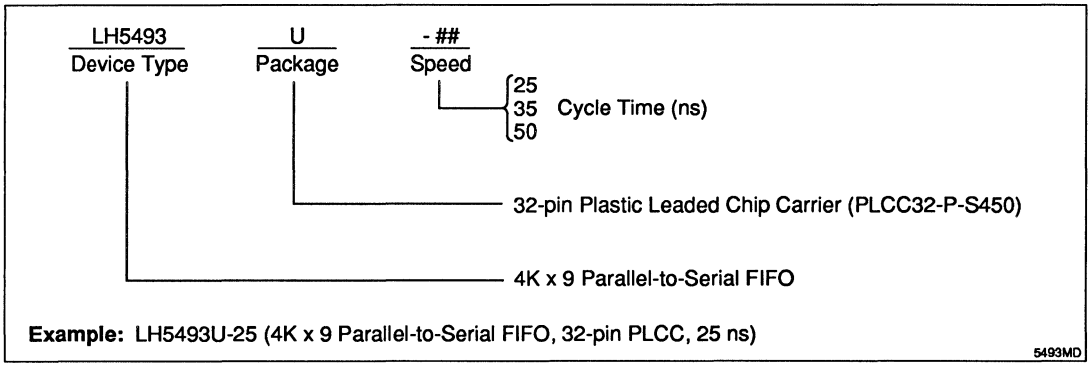


Figure 13. Paralleled Serial Operation (4096 × 18 Bit)

ORDERING INFORMATION



LH5494

4K × 9 Serial-to-Parallel FIFO

FEATURES

- Fast Cycle Times: 25/35/50 ns
  Frequency: 40/28.5/20 MHz
- Serial Data In; Parallel Data Out
- Serial Output for Cascading Input Register
- Two Read Enable Inputs and One Write Enable Input, Sampled on Rising Edge of the Appropriate Clock
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port RAM Technology, 4096 × 9
- Fully Asynchronous Read and Write Operations
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Three-State Outputs with Output Enable
- Reset/Reread Capability
- TTL and CMOS Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5494 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 4096 9-bit words. One LH5494 FIFO can input a serial bitstream, and output 9-bit bytes in parallel. Thus, a single LH5494 is capable of 9-bit-to-1-bit SIPO (Serial-In, Parallel-Out) operation.

An LH5494 has one 1-bit serial input, and one 9-bit parallel output (read) port. And there is one 1-bit serial output, which supports paralleling LH5494s for longer-word-width SIPO operation. This serial output also allows additional control bits to be inserted at will into the serial output bitstream.

The LH5494 architecture supports a very convenient method of *paralleling* multiple FIFOs for SIPO operation, without any additional logic being needed, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5494 combination remains capable of performing all of the operations which a standalone LH5494 can perform. Thus, if two LH5494s are paralleled, the combination can input a serial bitstream and output 18-bit halfwords for 1-bit-to-18-bit SIPO operation. This paralleling scheme extends without change to an *arbitrary* number of LH5494s.

The LH5494 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either absolutely full or else absolutely empty.

One edge-sampled enable control input, WEN, is provided for the input port; and two such control inputs, $\overline{REN_1}$ and $\overline{REN_2}$, are provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5494 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN, and the Empty flag likewise

PIN CONNECTIONS

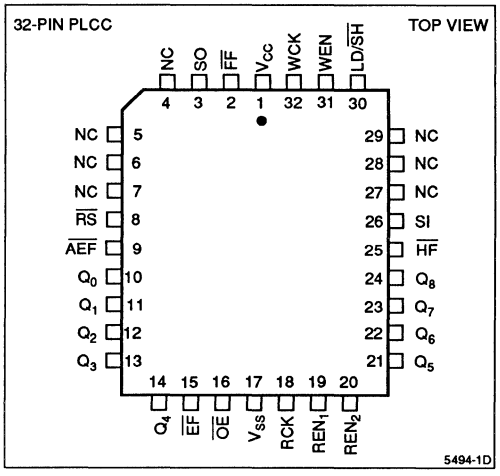


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

may be tied directly to REN_1 or to REN_2, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 11.)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

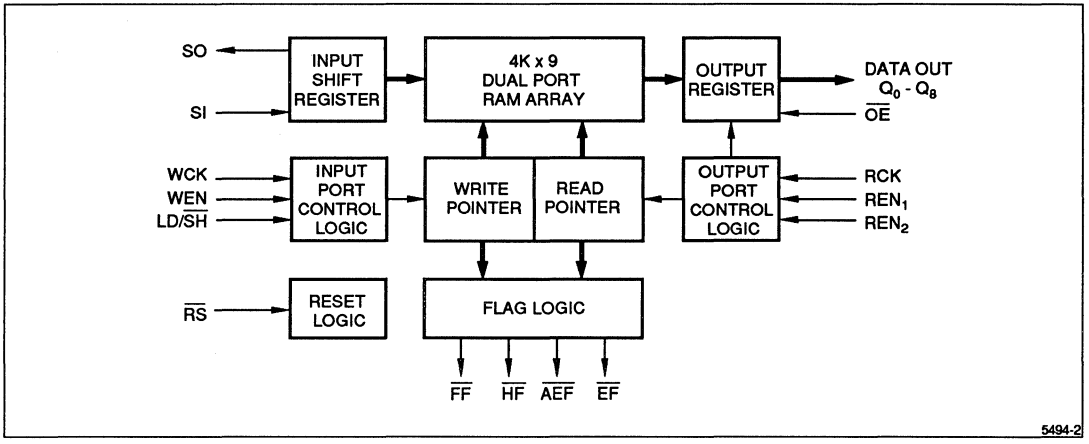


Figure 2. LH5494 Block Diagram

SIGNAL PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for Write operations.
RCK	Read Clock. A free-running clock input for Read operations.
SI	Serial Input. SI is sampled on the rising edge of WCK, whenever WEN is being asserted.
SO	Serial Output. A serial data output signal, to allow paralleled SIPO operation of multiple devices.
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever REN_1 and REN_2 are both being asserted.
WEN	Write Enable. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO.
LD/$\overline{SH}$	Load/Shift. An input signal which is sampled on the rising edge of WCK to control the load of parallel data from Input Shift Register into the FIFO.
REN_1	Read Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
REN_2	Read Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.
$\overline{OE}$	Output Enable. An assertive-LOW signal which places the data outputs $Q_0 - Q_8$ in a low-impedance state.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IH} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

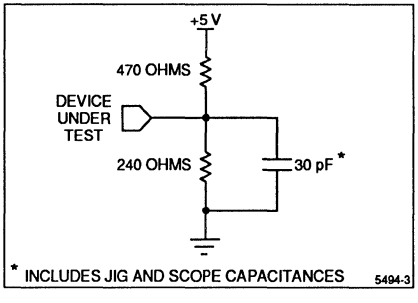


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance	7 pF
C_O (Output Capacitance)	7 pF

NOTES:
1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	–25		–35		–50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	28.5	–	20	MHz
t_{WC}	Write Clock Cycle Time	25	–	35	–	50	–	ns
t_{WH}	Write Clock High Time	10	–	14	–	20	–	ns
t_{WL}	Write Clock Low Time	10	–	14	–	20	–	ns
t_{RC}	Read Clock Cycle Time	25	–	35	–	50	–	ns
t_{RH}	Read Clock High Time	10	–	14	–	20	–	ns
t_{RL}	Read Clock Low Time	10	–	14	–	20	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	15	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	2	–	ns
t_{ES}	Enable Setup TIme to Rising Clock	10	–	10	–	15	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	2	–	ns
t_A	Data Output Access Time	–	20	–	25	–	35	ns
t_{SA}	Serial Output Access Time	–	20	–	25	–	35	ns
t_{OH}	Output Hold Time	5	–	5	–	5	–	ns
t_{QL}	$\overline{OE}$ to Data Outputs Low-Z [2]	1	–	1	–	1	–	ns
t_{QZ}	$\overline{OE}$ to Data Outputs High-Z [2]	–	10	–	12	–	15	ns
t_{OE}	Output Enable to Data Valid	–	10	–	12	–	15	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	25	–	35	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	25	–	35	ns
t_{HF}	Clock to Half Flag Valid	–	35	–	40	–	45	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	40	–	45	ns
t_{RS}	Reset Pulse Width	25	–	35	–	50	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	15	–	25	–	ns
t_{RF}	Reset Low to Flag Valid	–	30	–	35	–	40	ns
t_{RQ}	Reset to Data Outputs Low	–	20	–	25	–	30	ns
t_{FRL}	First Read Latency [4]	18	–	20	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	20	–	20	–	ns

NOTES:
1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN is being asserted, or else a rising edge of RCK occurs while REN_1 and REN_2 are both being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The Device is reset whenever the asynchronous RESET input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Read, shift, and/or write operations need not be deactivated during a reset operation, but failure to do so requires observance of the Reset Setup Time (t_{RSS}), to assure that the first write and/or first read following a reset operation will occur predictably.

If no read operations have been performed following a reset operation, then the previous data word being held in the output register consists of all zeroes. This data word will be seen on the output bus ($Q_0 - Q_8$) whenever the output enable ($\overline{OE}$) is held LOW. Likewise, data in the input shift register will be initialized to all zeroes after a reset operation.

Write

A shift operation is initiated on the rising edge of WCK, whenever WEN is HIGH and LD/$\overline{SH}$ is LOW. Data bits are shifted from MSB to LSB, with the data bit on the Serial Input (SI) replacing the contents of bit position D_7 in the input shift register, and the Serial Output (SO) copying the contents of bit position D_0.

A write operation consists of a parallel loading of data from the input shift register (bits $D_7 - D_0$), and the SI pin (bit D_8) to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both the edge-sampled Write Enable input (WEN) and the Load/Shift input (LD/$\overline{SH}$) are held HIGH.

When a full condition is reached, shift operations may continue, but write operations should be ceased in order to prevent overwriting unread data. The state of the status flags has no direct effect on shift or write operations, that is, the execution of write operations is gated only by WEN, and the internal logic of the LH5494 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location is freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency time (t_{FWL}) after the first read operation from a full FIFO, in order to assure that a correct data word is written into the FIFO memory.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK) whenever both of the edge-sampled Read Enable inputs (REN_1 and REN_2) are held HIGH for the prescribed setup and hold times. Read data becomes valid on the Data Out pins ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK, provided that the Output Enable ($\overline{OE}$) is being held LOW. $\overline{OE}$ is an assertive-LOW asynchronous input. When $\overline{OE}$ is taken LOW, the $Q_0 - Q_8$ outputs are driven (i.e., are in a low-Z state) within a minimum time t_{OL}. When $\overline{OE}$ is taken HIGH, the $Q_0 - Q_8$ outputs are in a high-Z state within a maximum time t_{OZ}. The state of the four status flags has no direct effect on read operations; that is, the execution of read or shift operations is gated only by REN_1 and REN_2 and LD/$\overline{SH}$, and the internal logic of the LH5494 itself has no interlock to prevent underrunning valid data after the internal read pointer catches up to the write pointer – and passes it, if reading is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

When an empty condition is reached, read operations should be ceased until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the Empty Flag ($\overline{EF}$) is deasserted ($\overline{EF}$ = HIGH). The next read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write operation into an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

Status Flags are included for Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1. Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

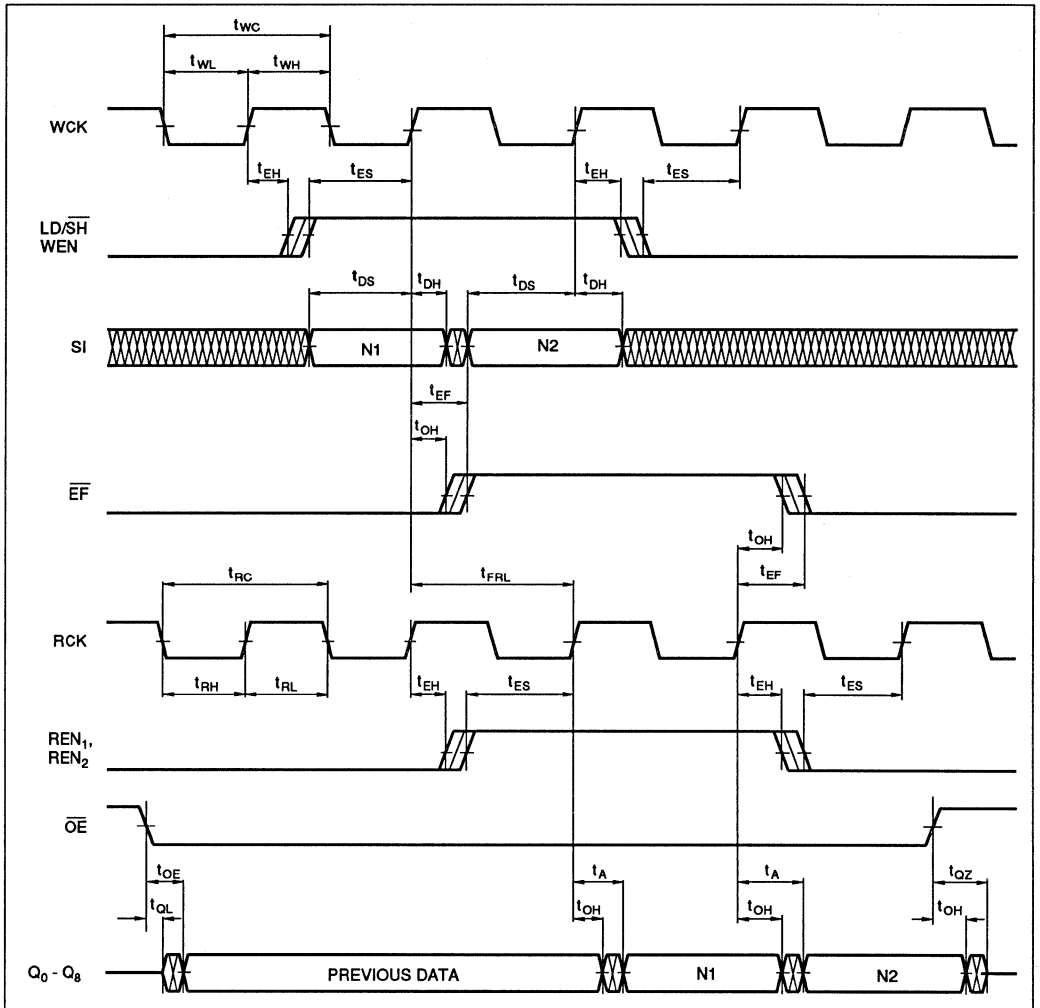
Reset, Reread

The FIFO can be made to reread previously read data through a reset operation, which initializes the internal read and write address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 words of old data, which previously had been written into and/or read from the FIFO, still then remains

OPERATIONAL DESCRIPTION (cont'd)

in the memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data are being written to the FIFO following the Reset.

TIMING DIAGRAMS

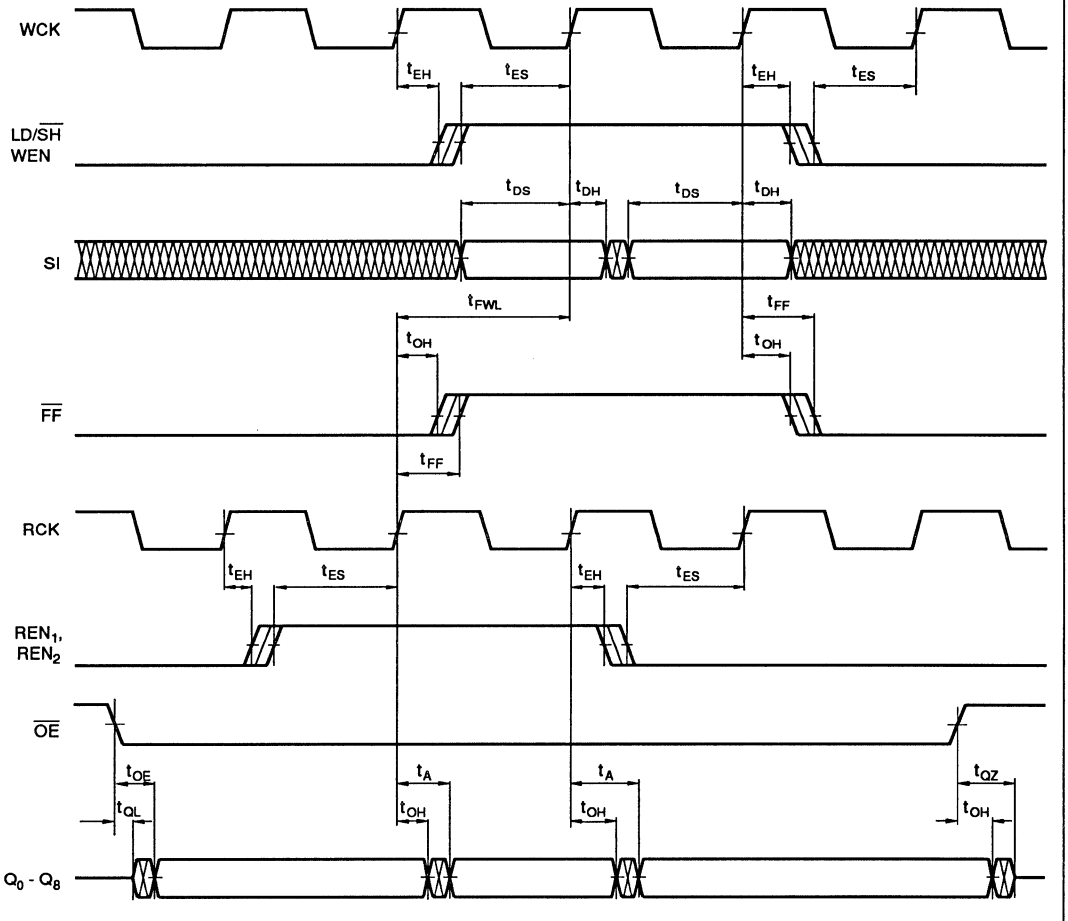


NOTES:

1. Both WEN and LD/$\overline{SH}$ must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ asserted (LOW) does not prevent further read operations, unless it is tied either to REN_1 or to REN_2.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, in order to ensure that valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.
5. Immediately following a reset operation, the 'previous data' will be all bits LOW.

Figure 4. Write and Read Operations in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. Both WEN and LD/$\overline{SH}$ must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ asserted (LOW) does not prevent further write operations, unless it is tied to WEN.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5494-5

Figure 5. Read and Write Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)

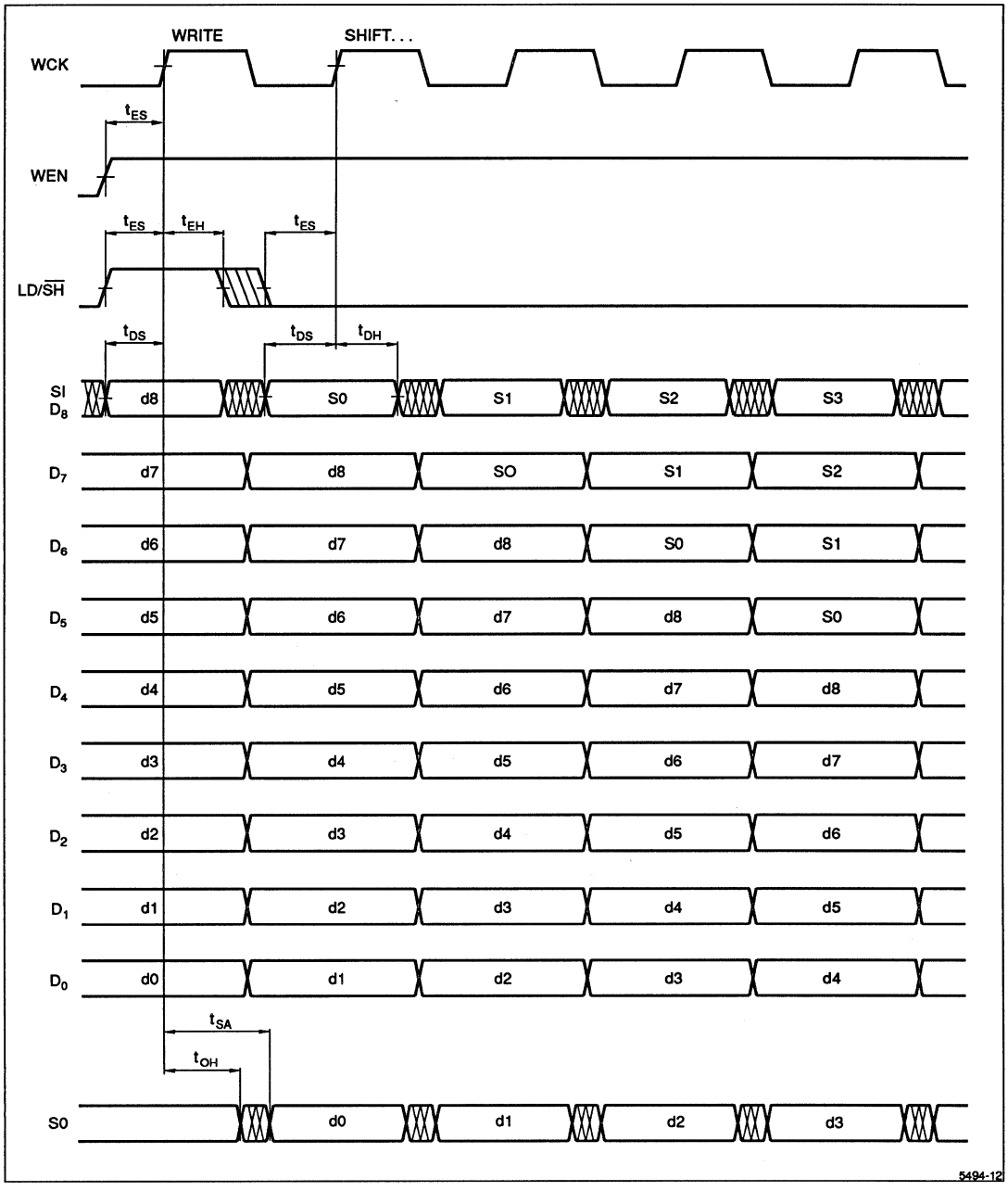
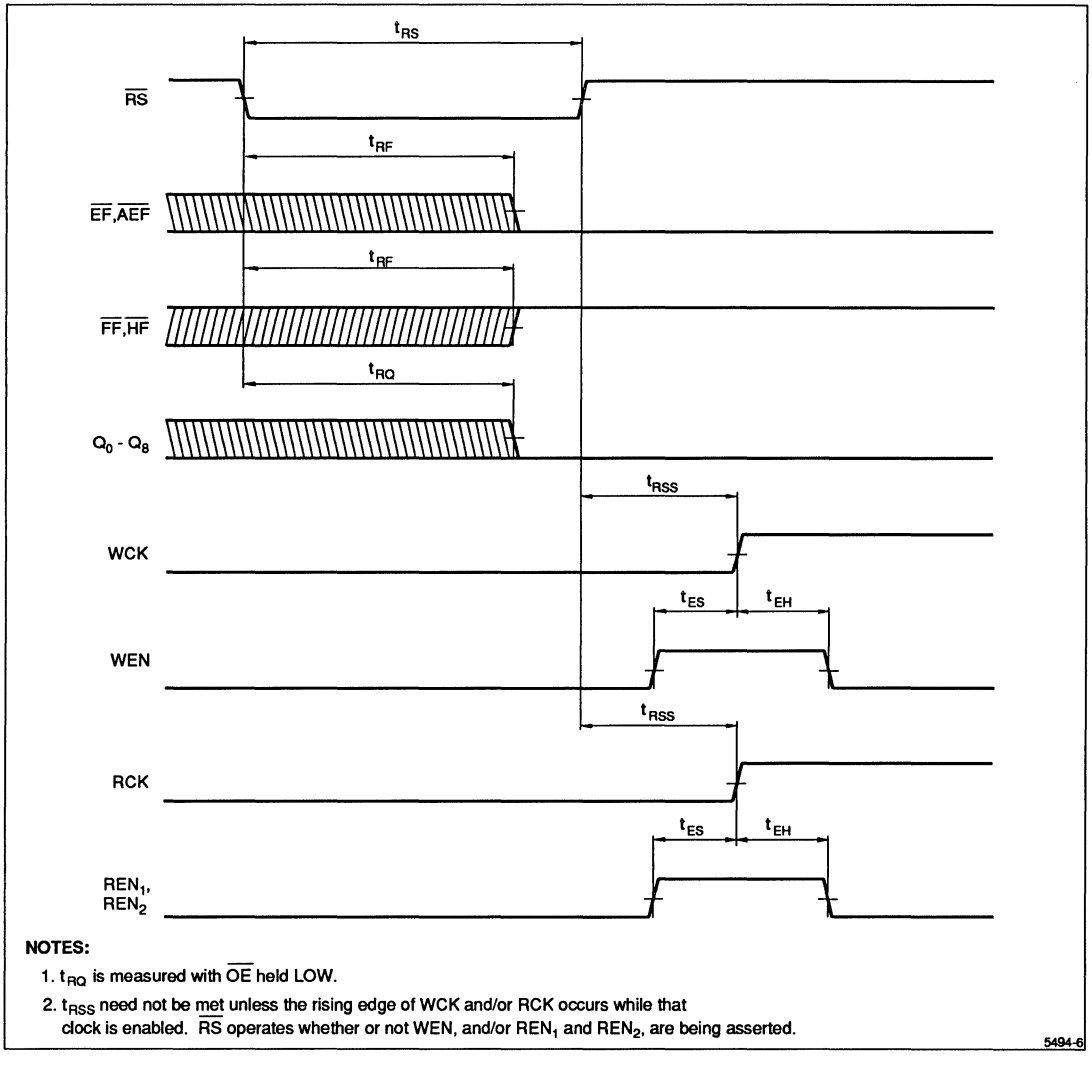


Figure 6. Serial Shift, Write Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. t_{RQ} is measured with $\overline{OE}$ held LOW.
2. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN, and/or REN_1 and REN_2, are being asserted.

5494-6

Figure 7. Reset Timing

TIMING DIAGRAMS (cont'd)

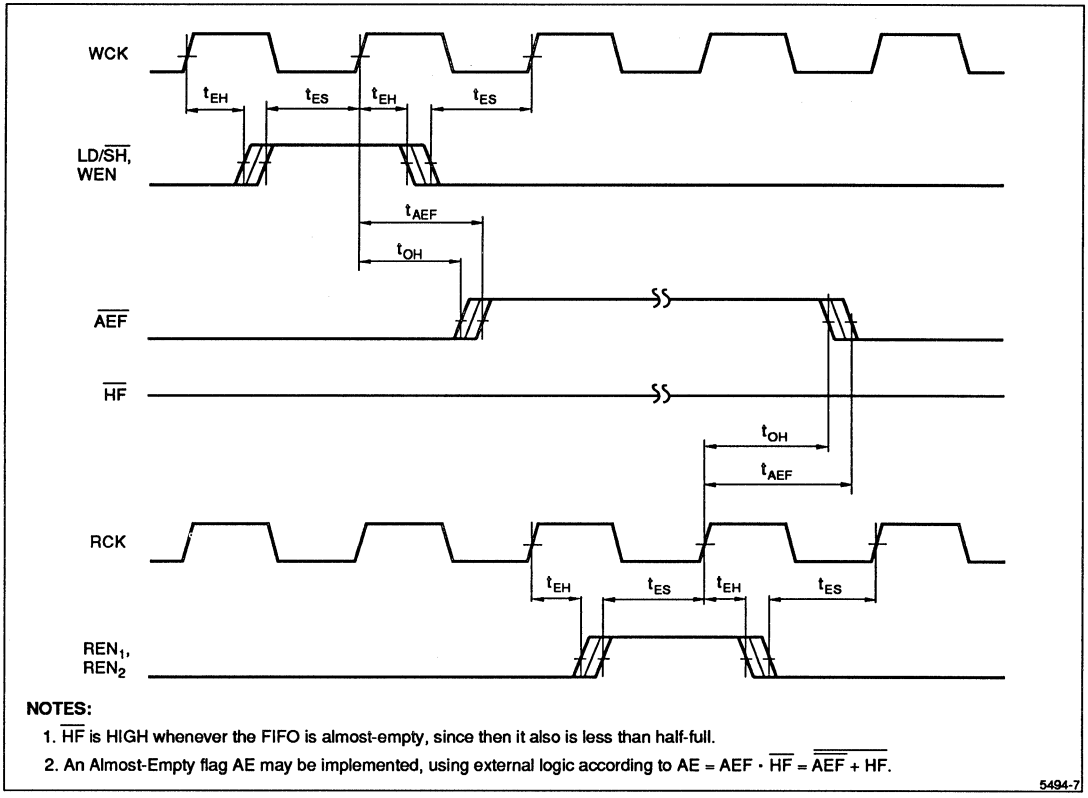


Figure 8. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2048
1	1	0	1	8	2047	2049	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

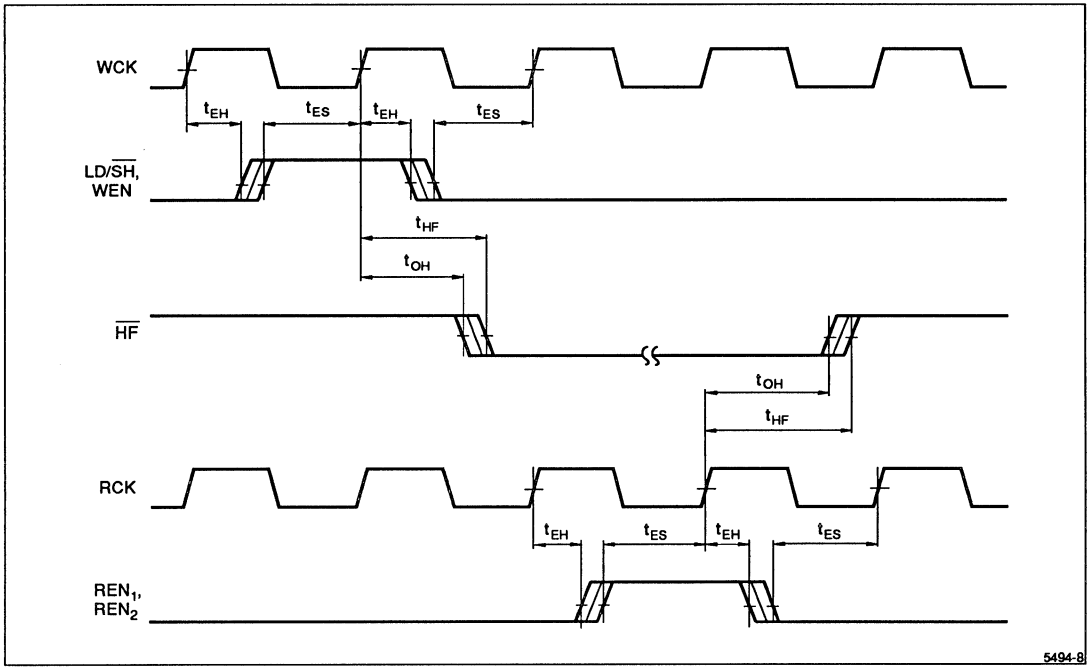
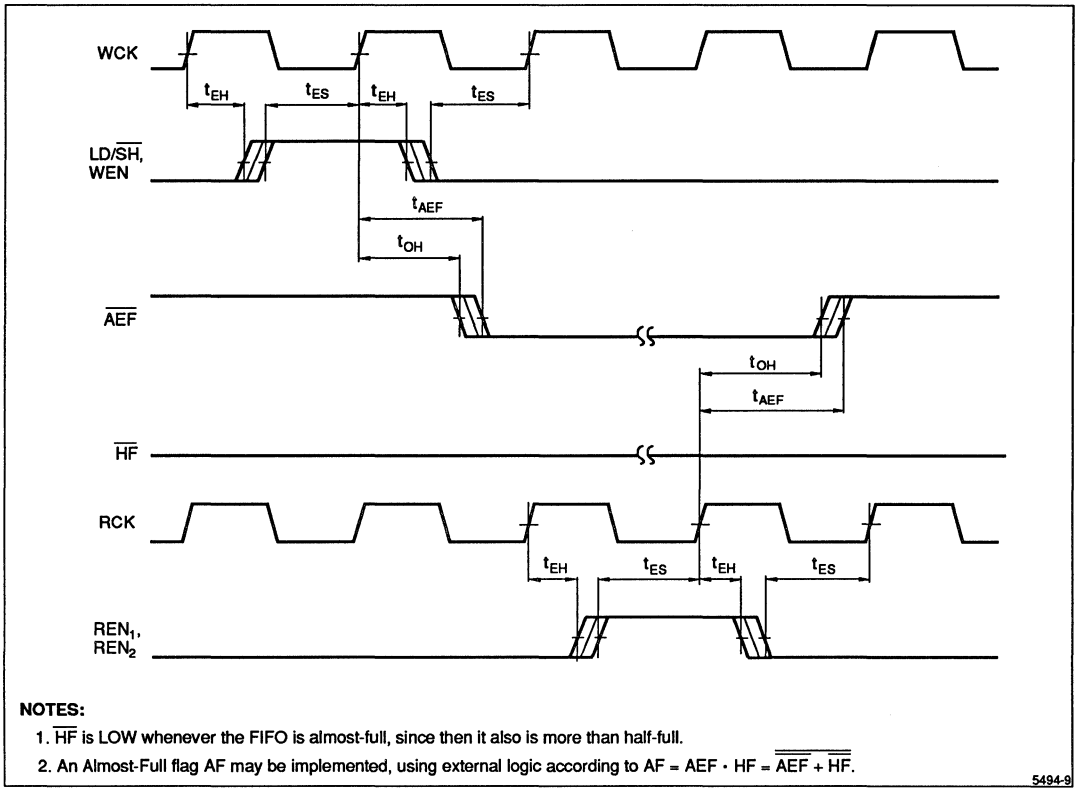


Figure 9. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to AF = AEF • HF = $\overline{\overline{AEF} + \overline{HF}}$.

5494-9

Figure 10. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Read and Write Operations

Read and write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. As such, the Read Enable (REN_1 and REN_2), Write Enable (WEN), and Load/Shift (LD/$\overline{SH}$) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the REN_1, REN_2, and WEN inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to WEN, in order to prevent 'overrun' write operations when the full condition is reached. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to REN_1 or REN_2, in order to prevent 'underrun' read operations when the empty condition is reached, while the other Read Enable input remains available for system control.

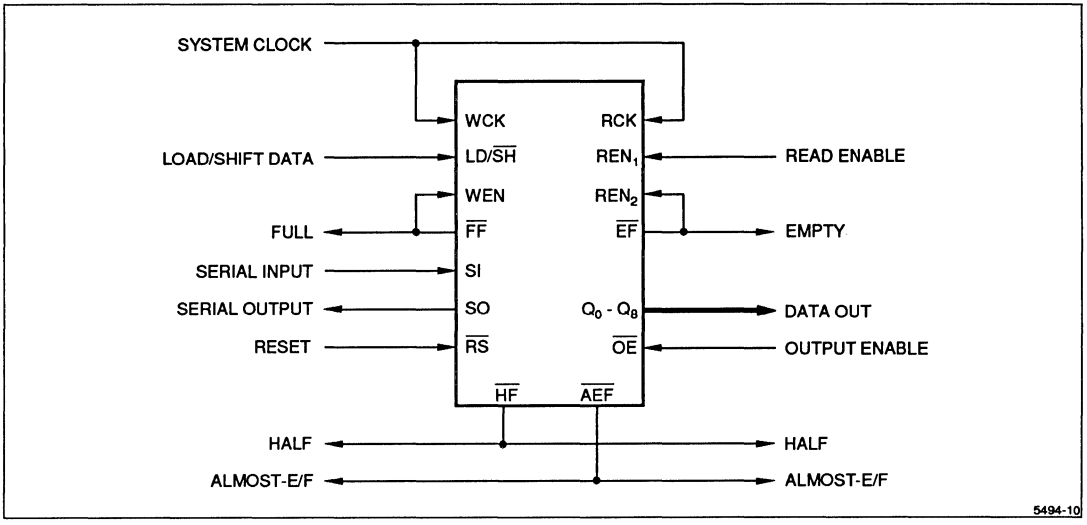


Figure 11. Synchronous Operation

OPERATIONAL MODES (cont'd)

Asynchronous Read and Write Operations

Write operations and read operations may be performed completely asynchronously relative to each other, when the RCK input and the WCK input are derived from clock signals of *different* systems. Under these conditions, the transition of status flags is performed relative to two unpredictably-related clock edges; and so, these flags should not be used to directly drive Read Enable or Write Enable inputs, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user, in order to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and Half-Full flag should be used to provide some advance warning, to avoid overrunning or underrunning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

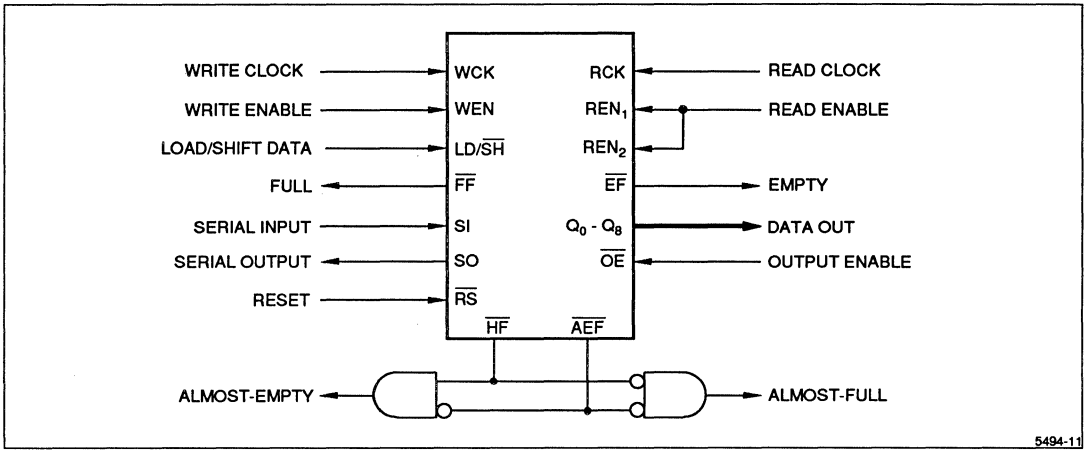


Figure 12. Asychronous Operation

OPERATIONAL MODES (cont'd)

Cascaded Operation

Cascaded operation allows LH5494 input shift registers to be extended in wordwidth, by interconnecting multiple LH5494 devices in a serial chain. The Serial Input (SI) of the first device in the chain serves as the 'effective-FIFO' serial input. The SI pin of any subsequent device is connected to the Serial Out (SO) pin of the preceding device in the chain. The final 'effective FIFO' serial output data (if needed) is taken from the SO pin of the last device in the chain.

In cascaded operation, the output port may be configured either for an increase in FIFO depth, or for an increase in FIFO wordwidth. When the output port is expanded in width, the Read Enable inputs (REN_1 and REN_2) and Output Enable ($\overline{OE}$) are common for all devices.

When the output port is expanded in depth, the common Data Out pins of multiple devices may be tied together. One Read Enable may then be used for system control, while the other Read Enable and $\overline{OE}$ are driven by decode logic to direct the flow of data. This decode logic should alternate read accesses from one device to the next in a sequential manner.

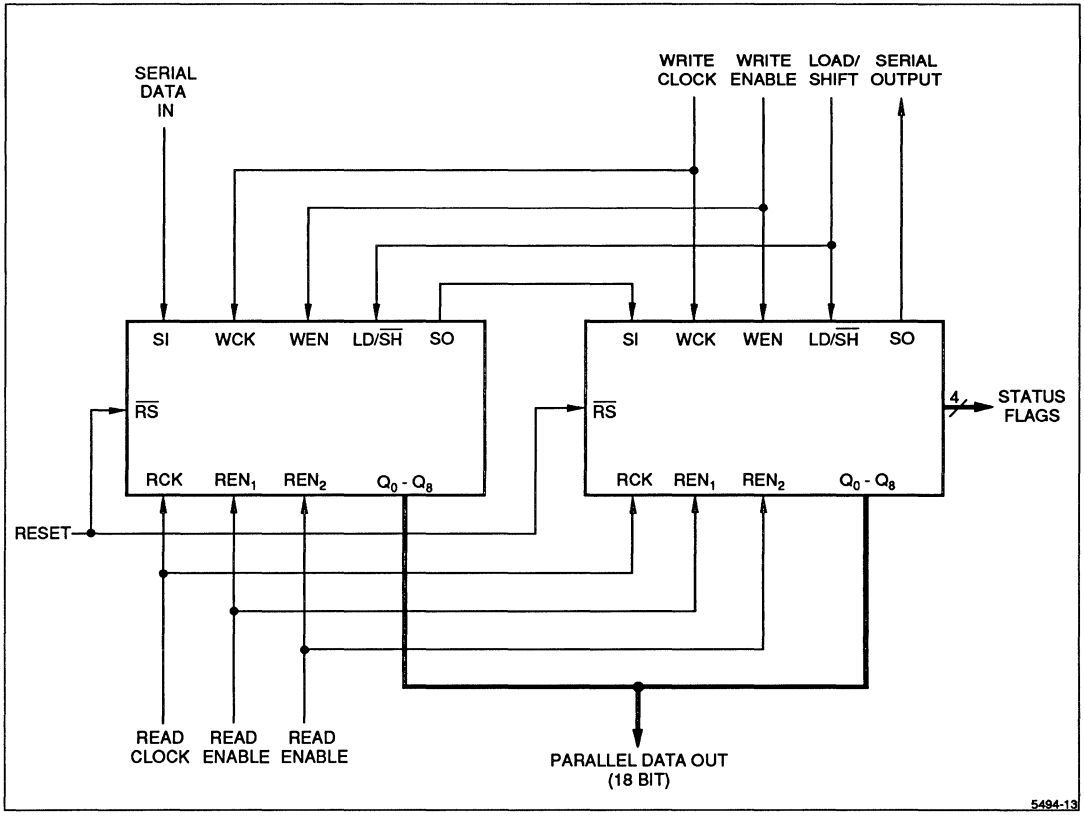
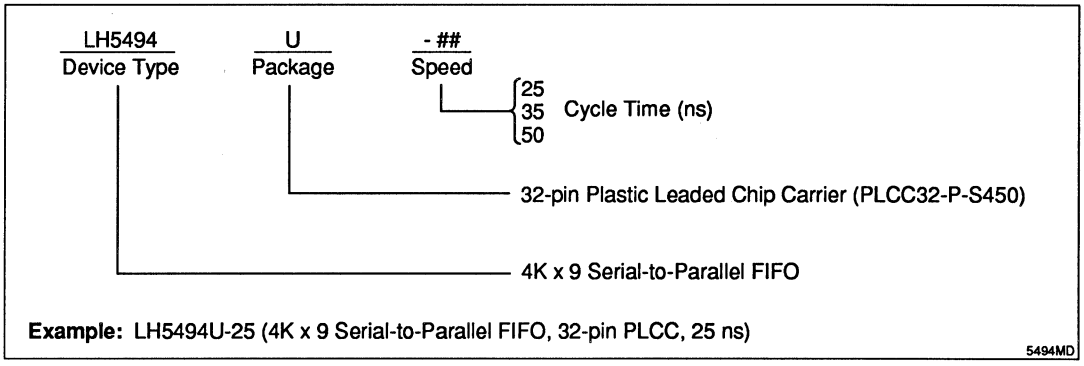


Figure 13. Cascaded Serial Operation (4096 × 18 Bit)

ORDERING INFORMATION



Example: LH5494U-25 (4K x 9 Serial-to-Parallel FIFO, 32-pin PLCC, 25 ns)

5494MD

LH5420

256 × 36 × 2 Bidirectional FIFO

FEATURES

- Fast Cycle Times: 25/30/35 ns
- Two 256 × 36-bit FIFO Buffers
- Full 36-bit Word Width
- Selectable 36/18/9-bit Word Width on Port B
- Fully Asynchronous Port-to-Port Communications
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- R/$\overline{W}$, Enable, Request, and Address Control Inputs Sampled on the Rising Clock Edge
- Synchronous Request/Acknowledge 'Handshake' Capability; Use is Optional
- Device Comes Up Into Known Default State at Reset; Programming is Allowed, but is not Required
- Asynchronous Output Enables
- 5 Status Flags per Port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Almost-Full Flag and Almost-Empty Flag are Programmable
- Mailbox Registers with Synchronized Flags
- Data Bypass Function
- Data Retransmit Function
- Automatic Byte Parity Checking
- TTL/CMOS-Compatible I/O
- Space-Saving PQFP * and PGA Packages
- Mosel MS76542-SSFC and National Semiconductor NMF256X36X2 are Pin-Compatible and Functionally Equivalent

* This is a final data sheet; except, that all references to the PQFP package still have preliminary status.

FUNCTIONAL DESCRIPTION

The LH5420 contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bidirectional data buffering. FIFO #1 and FIFO #2 each are organized as 256 words by 36 bits. The LH5420 is ideal either for wide unidirectional applications or for bidirectional data applications; component count and board area are reduced.

The LH5420 has two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated on a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the LH5420 is a fully-static part.

Conceptually, the port clocks CK_A and CK_B are free-running, periodic 'clock' waveforms, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that these 'clock' waveforms *must* be periodic. An 'asynchronous' mode of operation is possible, in one or both directions, independently, if the appropriate enable and request inputs are continuously asserted, and aperiodic 'clock' pulses of suitable duration are generated by external logic.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/ acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for *each* FIFO. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 256 or fewer words may be retransmitted any desired number of times.

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a New-Mail-Alert Flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

FUNCTIONAL DESCRIPTION (cont'd)

Data bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36, 18, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths.

A Byte Parity Check Flag at each port monitors data integrity. These flags are initialized for odd data parity at reset, but may be reprogrammed for even parity.

PIN CONNECTIONS

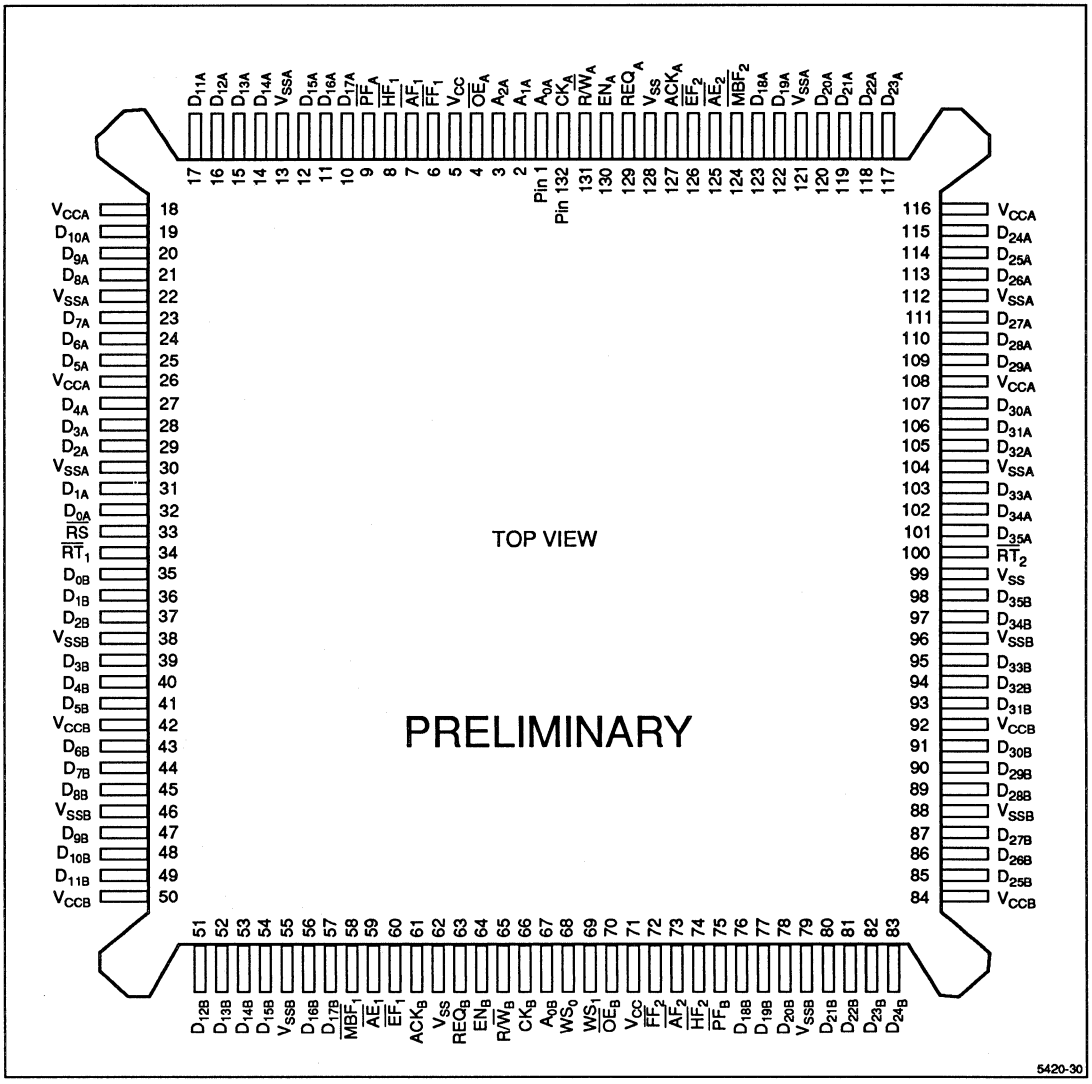
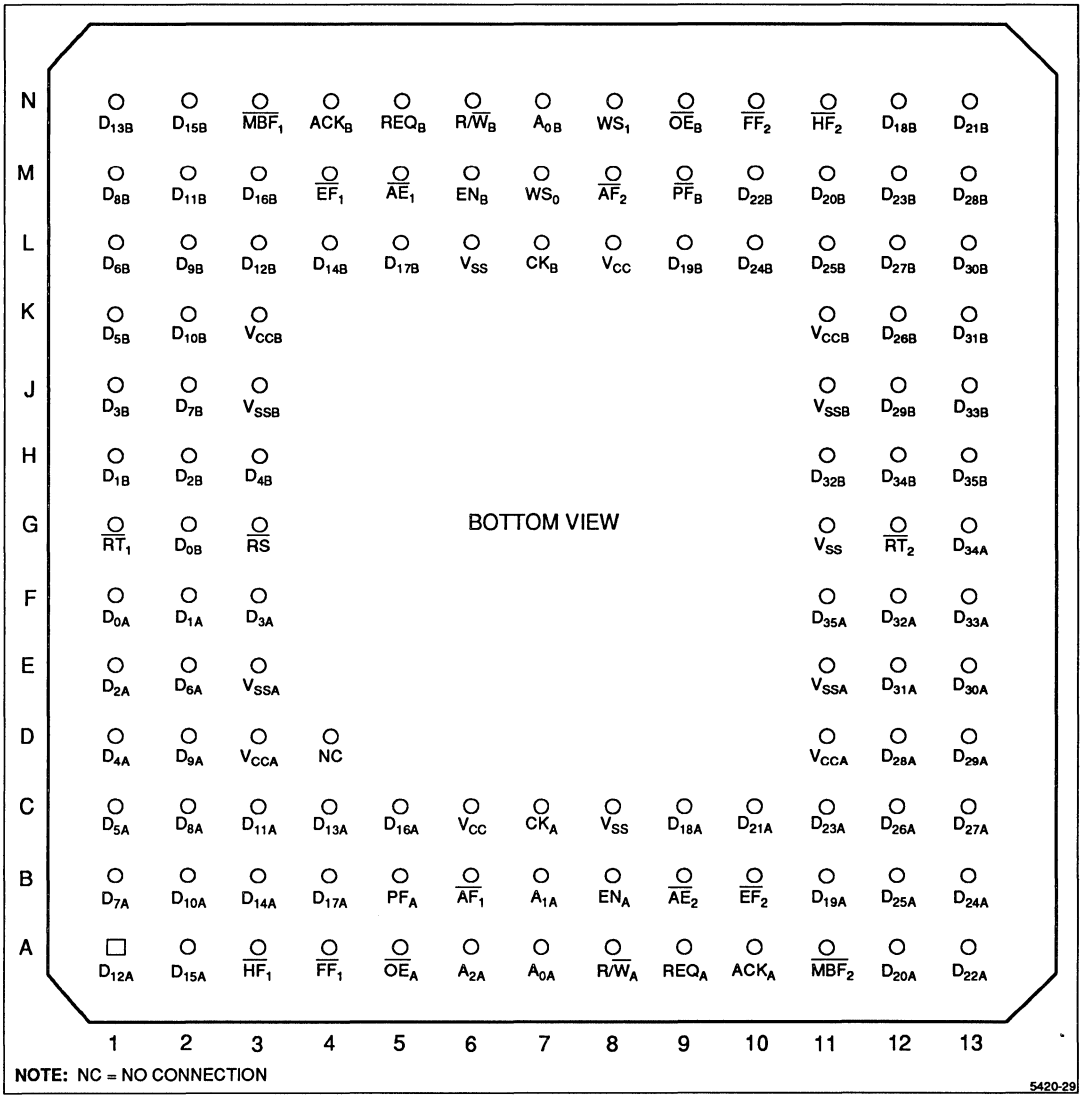


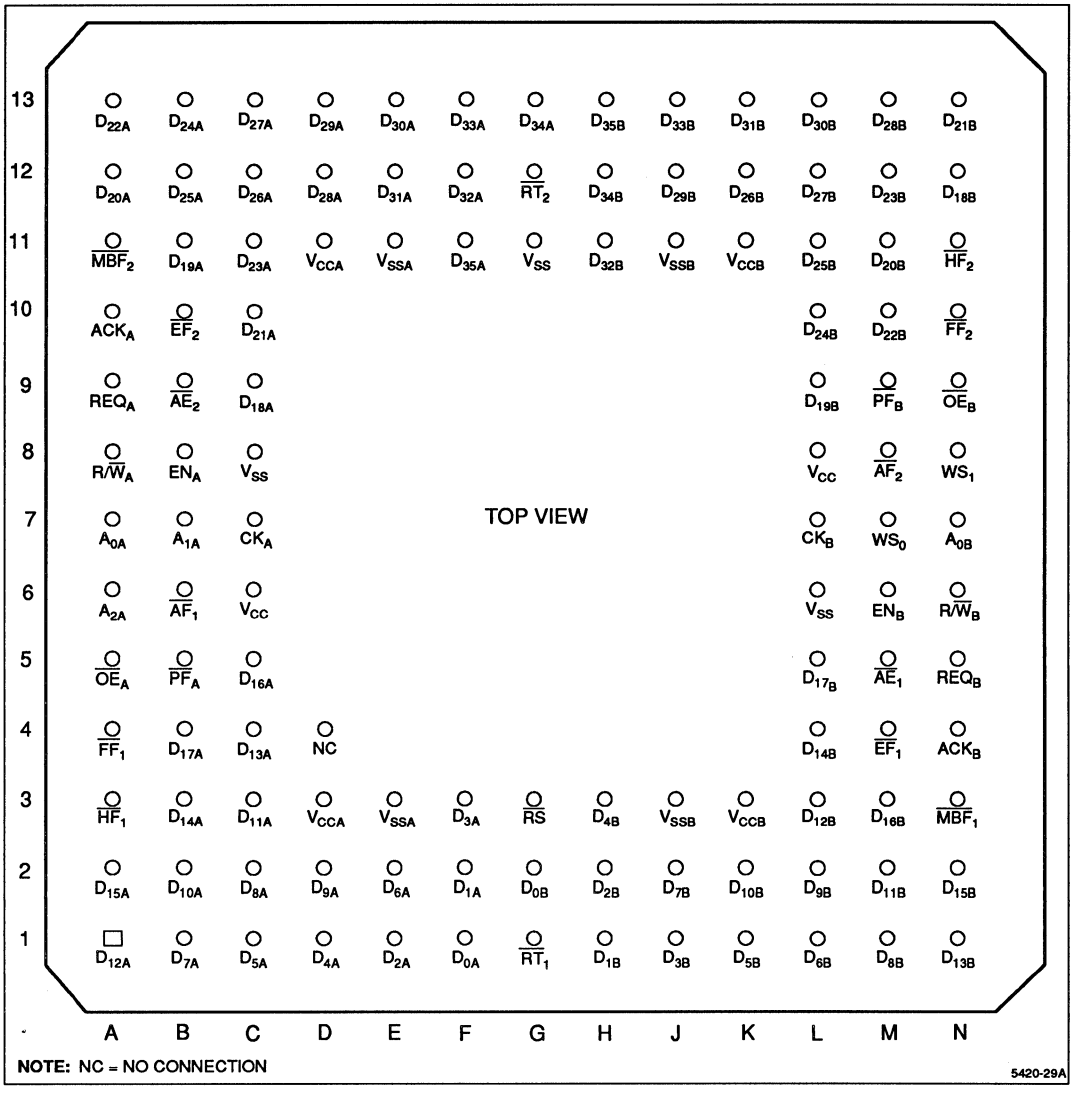
Figure 1. Pin Connections for 132-Pin Quad Flat Package (TOP VIEW)



NOTE: NC = NO CONNECTION

5420-29

Figure 2. Pin Connections for 120-Pin PGA Package (BOTTOM VIEW)



NOTE: NC = NO CONNECTION

5420-29A

Figure 3. Pin Connections for 120-Pin PGA Package (TOP VIEW)

PIN LIST

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
A_{0A}	1	A7
A_{1A}	2	B7
A_{2A}	3	A6
$\overline{OE}_A$	4	A5
$\overline{FF}_1$	6	A4
$\overline{AF}_1$	7	B6
$\overline{HF}_1$	8	A3
$\overline{PF}_A$	9	B5
D_{17A}	10	B4
D_{16A}	11	C5
D_{15A}	12	A2
D_{14A}	14	B3
D_{13A}	15	C4
D_{12A}	16	A1
D_{11A}	17	C3
D_{10A}	19	B2
D_{9A}	20	D2
D_{8A}	21	C2
D_{7A}	23	B1
D_{6A}	24	E2
D_{5A}	25	C1
D_{4A}	27	D1
D_{3A}	28	F3
D_{2A}	29	E1
D_{1A}	31	F2
D_{0A}	32	F1
$\overline{RS}$	33	G3
$\overline{RT}_1$	34	G1
D_{0B}	35	G2
D_{1B}	36	H1
D_{2B}	37	H2
D_{3B}	39	J1
D_{4B}	40	H3
D_{5B}	41	K1
D_{6B}	43	L1
D_{7B}	44	J2
D_{8B}	45	M1
D_{9B}	47	L2
D_{10B}	48	K2
D_{11B}	49	M2
D_{12B}	51	L3
D_{13B}	52	N1
D_{14B}	53	L4
D_{15B}	54	N2

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{16B}	56	M3
D_{17B}	57	L5
$\overline{MBF}_1$	58	N3
$\overline{AE}_1$	59	M5
$\overline{EF}_1$	60	M4
ACK_B	61	N4
REQ_B	63	N5
EN_B	64	M6
$R/\overline{W}_B$	65	N6
CK_B	66	L7
A_{0B}	67	N7
WS_0	68	M7
WS_1	69	N8
$\overline{OE}_B$	70	N9
$\overline{FF}_2$	72	N10
$\overline{AF}_2$	73	M8
$\overline{HF}_2$	74	N11
$\overline{PF}_B$	75	M9
D_{18B}	76	N12
D_{19B}	77	L9
D_{20B}	78	M11
D_{21B}	80	N13
D_{22B}	81	M10
D_{23B}	82	M12
D_{24B}	83	L10
D_{25B}	85	L11
D_{26B}	86	K12
D_{27B}	87	L12
D_{28B}	89	M13
D_{29B}	90	J12
D_{30B}	91	L13
D_{31B}	93	K13
D_{32B}	94	H11
D_{33B}	95	J13
D_{34B}	97	H12
D_{35B}	98	H13
$\overline{RT}_2$	100	G12
D_{35A}	101	F11
D_{34A}	102	G13
D_{33A}	103	F13
D_{32A}	105	F12
D_{31A}	106	E12
D_{30A}	107	E13
D_{29A}	109	D13

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{28A}	110	D12
D_{27A}	111	C13
D_{26A}	113	C12
D_{25A}	114	B12
D_{24A}	115	B13
D_{23A}	117	C11
D_{22A}	118	A13
D_{21A}	119	C10
D_{20A}	120	A12
D_{19A}	122	B11
D_{18A}	123	C9
$\overline{MBF}_2$	124	A11
$\overline{AE}_2$	125	B9
$\overline{EF}_2$	126	B10
ACK_A	127	A10
REQ_A	129	A9
EN_A	130	B8
$R/\overline{W}_A$	131	A8
CK_A	132	C7
V_{CC}	5	C6
V_{SSA}	13	E3
V_{CCA}	18	D3
V_{SSA}	22	E3
V_{CCA}	26	D3
V_{SSA}	30	E3
V_{SSB}	38	J3
V_{CCB}	42	K3
V_{SSB}	46	J3
V_{CCB}	50	K3
V_{SSB}	55	J3
V_{SS}	62	L6
V_{CC}	71	L8
V_{SSB}	79	J11
V_{CCB}	84	K11
V_{SSB}	88	J11
V_{CCB}	92	K11
V_{SSB}	96	J11
V_{SS}	99	G11
V_{SSA}	104	E11
V_{CCA}	108	D11
V_{SSA}	112	E11
V_{CCA}	116	D11
V_{SSA}	121	E11
V_{SS}	128	C8

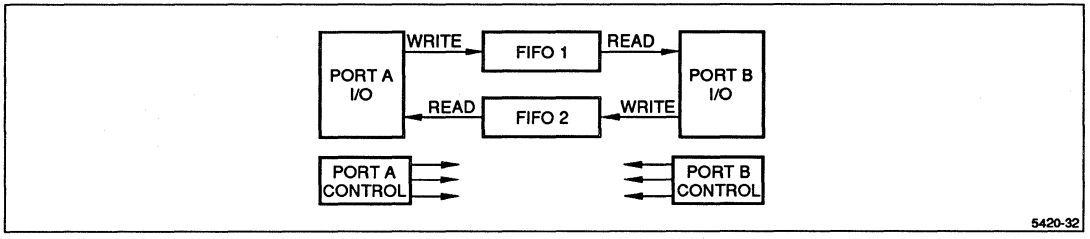


Figure 4a. Simplified LH5420 Block Diagram

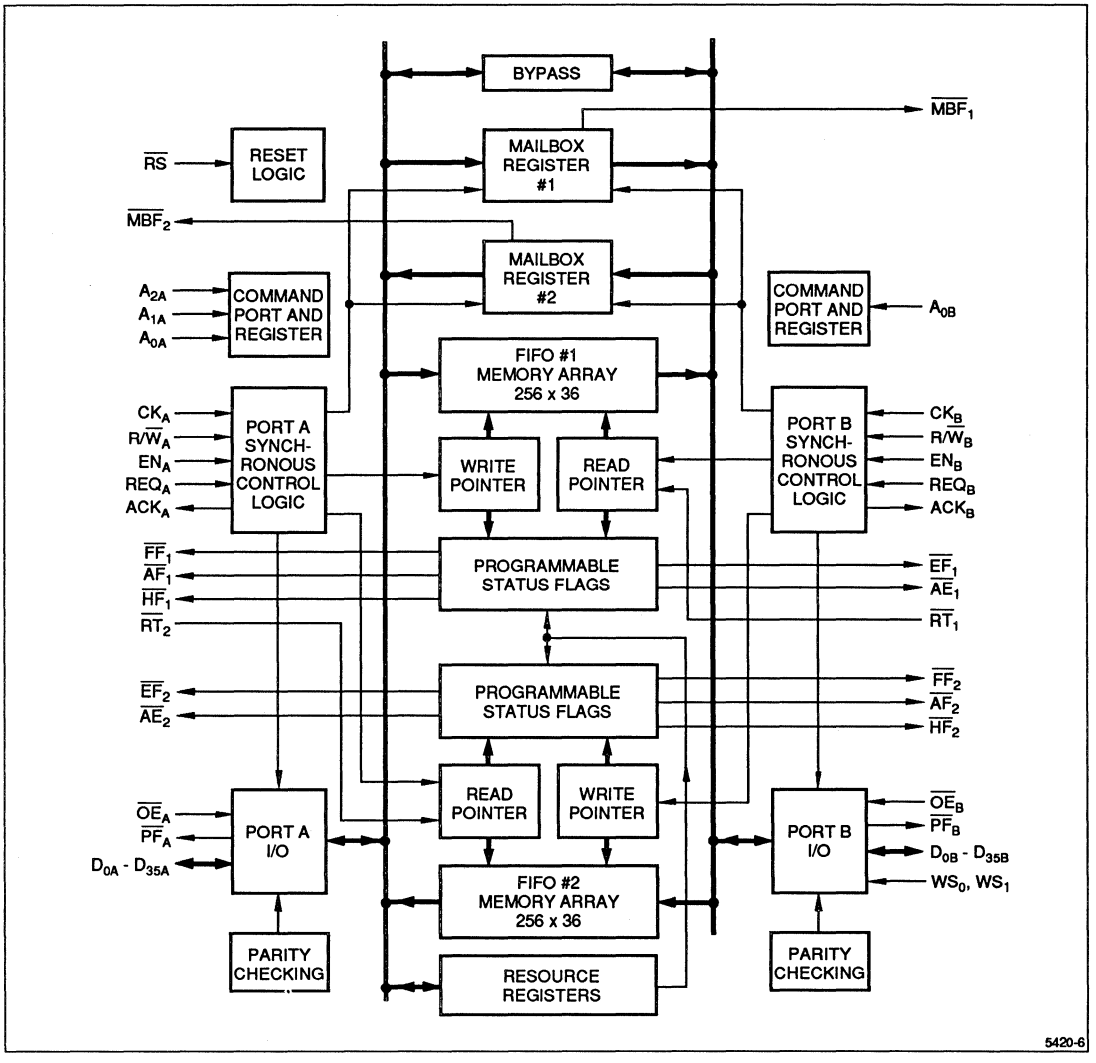


Figure 4b. Detailed LH5420 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
		GENERAL
V_{CC}, V_{SS}	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CK_A	I	Port A Free-Running Clock
$R/\overline{W}_A$	I	Port A Edge-Sampled Read/Write Control
EN_A	I	Port A Edge-Sampled Enable
A_{0A}, A_{1A}, A_{2A}	I	Port A Edge-Sampled Address Pins
$D_{0A} - D_{35A}$	I/O/Z	Port A Bidirectional Data Bus
$\overline{OE}_A$	I	Port A Level-Sensitive Output Enable
$\overline{FF}_1$	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}_1$	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_1$	O	FIFO #1 Half-Full Flag
$\overline{AE}_2$	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_2$	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}_A$	O	Port A Mailbox New-Mail-Alert Flag for Mailbox #2
$\overline{PF}_A$	O	Port A Parity Flag
REQ_A	I	Port A Request/Enable
ACK_A	O	Port A Acknowledge
$\overline{RT}_2$	I	FIFO #2 Retransmit
		PORT B
CK_B	I	Port B Free-Running Clock
$R/\overline{W}_B$	I	Port B Edge-Sampled Read/Write Control
EN_B	I	Port B Edge-Sampled Enable
A_{0B}	I	Port B Edge-Sampled Address Pin
$D_{0B} - D_{35B}$	I/O/Z	Port B Bidirectional Data Bus
$\overline{OE}_B$	I	Port B Level-Sensitive Output Enable
$\overline{FF}_2$	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}_2$	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_2$	O	FIFO #2 Half-Full Flag
$\overline{AE}_1$	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_1$	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}_B$	O	Port B Mailbox New-Mail-Alert Flag for Mailbox #1
$\overline{PF}_B$	O	Port B Parity Flag
WS_0, WS_1	I	Port B Word-Width Select
REQ_B	I	Port B Request/Enable
ACK_B	O	Port B Acknowledge
$\overline{RT}_1$	I	FIFO #1 Retransmit

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	−10	10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at fc = max		280	mA
I_{CC2}	Average Standby Supply Current [1]	All Inputs = V_{IHMIN} (Clock idle)			mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC} − 0.2 V (Clock idle)			mA

4. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 5

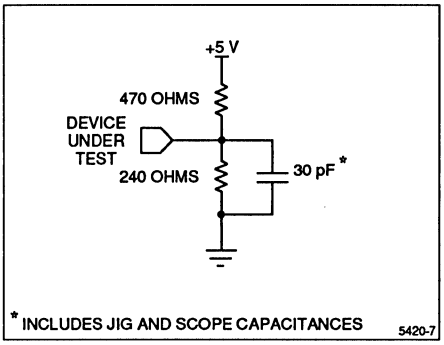


Figure 5. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_O (Output Capacitance)	8 pF

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DECRIPTION	-25		-30		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{CC}	Clock Cycle Frequency	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	25	—	30	—	35	—	ns
t_{CH}	Clock High Time	10	—	12	—	15	—	ns
t_{CL}	Clock Low Time	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	11	—	13	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time [6]	11	—	13	—	15	—	ns
t_{EH}	Enable Hold Time [6]	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	13	—	15	—	18	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time [6]	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time [6]	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time [6]	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time [6]	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	15	—	20	—	25	ns
t_{ACK}	Acknowledge Access Time	—	17	—	20	—	25	ns
t_{OH}	Output Hold Time	5	—	5	—	5	—	ns
t_{ZX}	Output Enable Time, $\overline{OE}$ LOW to $D_0 - D_{35}$ Low-Z [3]	5	—	5	—	5	—	ns
t_{XZ}	Output Disable Time, $\overline{OE}$ HIGH to $D_0 - D_{35}$ High-Z [3]	—	15	—	20	—	25	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	20	—	25	—	30	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	20	—	25	—	30	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full)	—	20	—	25	—	30	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty)	—	20	—	25	—	30	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full)	—	20	—	25	—	30	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	15	—	20	—	25	ns
t_{PF}	Data to Parity Flag Valid	—	17	—	20	—	25	ns
t_{RS}	Reset/Retransmit Pulse Width [7]	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time [3]	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time [3]	10	—	15	—	20	—	ns
t_{RF}	Reset Low to Flag Valid	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency [4]	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency [5]	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	20	—	25	—	30	ns

NOTES:

1. Timing measurements performed at 'AC Test Condition' levels.
2. Values are guaranteed by design; not currently production tested.
3. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CK_A occurs while EN_A is being asserted, or else a rising edge of CK_B occurs while EN_B is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful writing of data.
6. t_{AS}, t_{AH} address setup times and hold times need only be satisfied at clock edges which occur while the corresponding enables are being asserted.
7. First number used only when CK_A or CK_B is enabled; $t_{RS} = t_{RSS} + t_{CH} + t_{RSH}$.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken to a LOW state. A reset is required after power-up, before the first write operation may occur. The LH5420 is fully ready for operation after reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFO's first physical memory locations. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE}_1/\overline{AE}_2$ flag gets asserted within eight locations of an empty condition, and the $\overline{AF}_1/\overline{AF}_2$ flag likewise gets asserted within eight locations of a full condition, for FIFO #1/FIFO #2 respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and does not permit write or read operations during reset. The direction of the bypass data transmission is determined by th $R/\overline{W}_A$ control input, which does not get overridden by the $\overline{RS}$ input. The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device at reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A_{0A}, A_{1A}, and A_{2A}, which select between FIFO access, mailbox-register access, and flag-offset-value-programming operating mode. Port B has a single address input, A_{0B}, to select between FIFO access or mailbox-register access. The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Select-input definitions are summarized in Table 1.

FIFO Write

Port A writes to FIFO #1, and Port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held LOW; the FIFO address is selected; and the prescribed setup and hold times are observed for all of these signals. Setup and hold times must also be observed on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$).

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data is retrieved.

FIFO Read

Port A reads from FIFO #2, and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; and the FIFO address is selected; and the prescribed setup and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive-LOW, asynchronous output enables. Their effect is only to enable or disable the output drivers of the respective Port. Disabling the outputs does *not* disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs are again enabled, unless subsequently overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be deasserted (HIGH). The first read operation should begin no earlier than a First Read Latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Table 1. Resource Register Addresses

A_{2A}	A_{1A}	A_{0A}	RESOURCE
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ Flag Offset Registers
H	L	L	Parity Mode Bit
L	H	H	$\overline{AE}_1$ Flag Offset Register
L	H	L	$\overline{AF}_1$ Flag Offset Register
L	L	H	$\overline{AE}_2$ Flag Offset Register
L	L	L	$\overline{AF}_2$ Flag Offset Register
A_{0B}			RESOURCE
PORT B			
H			FIFO
L			Mailbox

OPERATIONAL DESCRIPTION (cont'd)

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for full ($\overline{FF}_1$ and $\overline{FF}_2$), half-full ($\overline{HF}_1$ and $\overline{HF}_2$), and empty ($\overline{EF}_1$ and $\overline{EF}_2$). $\overline{FF}_1$, $\overline{HF}_1$, and $\overline{EF}_1$ indicate the status of FIFO #1; and $\overline{FF}_2$, $\overline{HF}_2$, and $\overline{EF}_2$ indicate the status of FIFO #2.

A full flag is asserted following the rising clock edge for a write operation that fills the FIFO. A full flag is deasserted following the falling clock edge for a read operation to a full FIFO. A half-full flag is updated following the rising clock edge of a read or write operation to a FIFO. An empty flag is asserted following the rising clock edge for a read operation that empties the FIFO. An empty flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided, two for almost-full ($\overline{AF}_1$ and $\overline{AF}_2$) and two for almost-empty ($\overline{AE}_1$ and $\overline{AE}_2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset, but can be reprogrammed over the entire FIFO depth.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word; or, each programmable flag offset can be set individually, through one of four 8-bit status words. Table 3 illustrates the data format for flag-programming words.

Mailbox Operation

Two mailbox registers are provided for passing control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (EN_A or EN_B) HIGH. That is, writing to Mailbox Register #1, or reading from Mailbox Register #2, is synchronized to CK_A; and writing to Mailbox Register #2, or reading from Mailbox Register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register access. Each mailbox register has its own New-Mail-Alert Flag, which is synchronized to the reading port's clock. These New-Mail-Alert Flags are status indicators only, and cannot inhibit mailbox-register read or write operations.

Request Acknowledge Handshake

An optional, synchronous, request-acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronously-operated ports. The Request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read or FIFO write operation is being requested. The Acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the Enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does *not* prove that a FIFO write access or read access actually did occur. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a synchronized predictor of the full flag for write operations, or as a synchronized predictor of the empty flag for read operations. Outside the 'almost-full' region and the 'almost-empty' region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the 'almost-full' region or the 'almost-empty' region, $ACK_{A/B}$ occurs only on every *third* cycle, to prevent an overrun of the FIFO's actual full or empty boundaries and to ensure that the t_{FWL} (first write latency) and t_{FRL} (first read latency) specifications are satisfied before $ACK_{A/B}$ is received. The 'almost-full region' is defined as 'that region, where the almost-full flag is being asserted,' and the 'almost-empty region' as 'that region, where the almost-empty flag is being asserted.' Thus, the extent of these 'almost' regions depends on how the system has programmed the offset values for the Almost-Full Flags and the Almost-Empty Flags. If the system has *not* programmed them, these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is *not* asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port *must* be asserted for the corresponding FIFO to operate.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical location, so that data may be reread. The write pointer is not affected. The status flags are updated; and a block of up to 256 data words, which previously had been written and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO location and the FIFO location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT}_1$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT}_2$ pin LOW. Read and write operations to a FIFO should

OPERATIONAL DESCRIPTION (cont'd)

be stopped while the corresponding Retransmit signal is being asserted.

Parity Check

The Parity Check Flags, $\overline{PF}_A$ and $\overline{PF}_B$, reflect the parity status of the data present on the corresponding port's data bus. The four bytes of a 36-bit word are grouped as $D_0 - D_8$, $D_9 - D_{17}$, $D_{18} - D_{25}$, and $D_{26} - D_{35}$; the parity of each 9-bit byte is individually checked, and the four single bit parity indications are logically ORed to produce the Parity-Flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even or odd parity during operation.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS_1 and WS_0 control inputs. WS_1 is tied HIGH for 36-bit access. WS_1 and WS_0 are both tied LOW for single-byte access. For double-byte access, WS_1 is tied LOW and WS_0 is tied HIGH.

In the single-byte or double-byte access mode, FIFO write operations on Port B pack the data to form 36-bit words when viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Note that the word-width programming feature is *only* supported for FIFO accesses. Mailbox and Data Bypass operations do *not* support word-width matching between Port A and Port B. Table 2, Figure 3 and Figure 4 summarize word-width selection for Port B.

Table 2. Port B Word-Width Selection

WS_1	WS_0	PORT B DATA WIDTH
H	H	36-Bit
H	L	36-Bit
L	H	18-Bit
L	L	9-Bit

Table 3. Flag Programming Words

36-BIT MODE (A_{2A}, A_{1A}, A_{0A}) = 1, 0, 1							
	D_{34A} . . . D_{27A}		D_{25A} . . . D_{18A}		D_{16A} . . . D_{9A}		D_{7A} . . . D_{0A}
X	$\overline{AF}_2$ Offset [1]	X	$\overline{AE}_2$ Offset [1]	X	$\overline{AF}_1$ Offset [1]	X	$\overline{AE}_1$ Offset [1]
8-BIT $\overline{AE}_1$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 1, 1							
							D_{7A} . . . D_{0A}
X...						X	$\overline{AE}_1$ Offset [1]
8-BIT $\overline{AF}_1$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 1, 0							
							D_{7A} . . . D_{0A}
X...						X	$\overline{AF}_1$ Offset [1]
8-BIT $\overline{AE}_2$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 0, 1							
							D_{7A} . . . D_{0A}
X...						X	$\overline{AE}_2$ Offset [1]
8-BIT $\overline{AF}_2$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 0, 0							
							D_{7A} . . . D_{0A}
X...						X	$\overline{AF}_2$ Offset [1]
PARITY MODE (A_2, A_1, A_0) = 1, 0, 0 (WRITE ONLY)							
							D_{0A}
X...						X	Parity Mode [2]

NOTES:

1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 4. Flag Definition Table

FLAG	VALID READ CYCLES REMAINING				VALID WRITE CYCLES REMAINING			
	FLAG = LOW		FLAG = HIGH		FLAG = LOW		FLAG = HIGH	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256-offset	256	0	255-offset	0	offset	offset + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	offset	offset + 1	256	256-offset	256	0	255-offset
$\overline{EF}$	0	0	1	256	256	256	0	255

PORT B WORD-WIDTH SELECTION

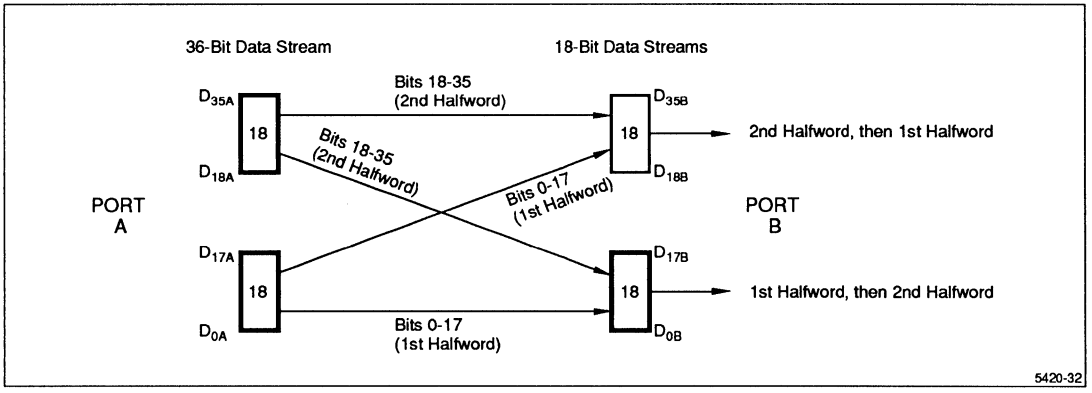


Figure 6a. 36-to-18 Funneling Through FIFO #1

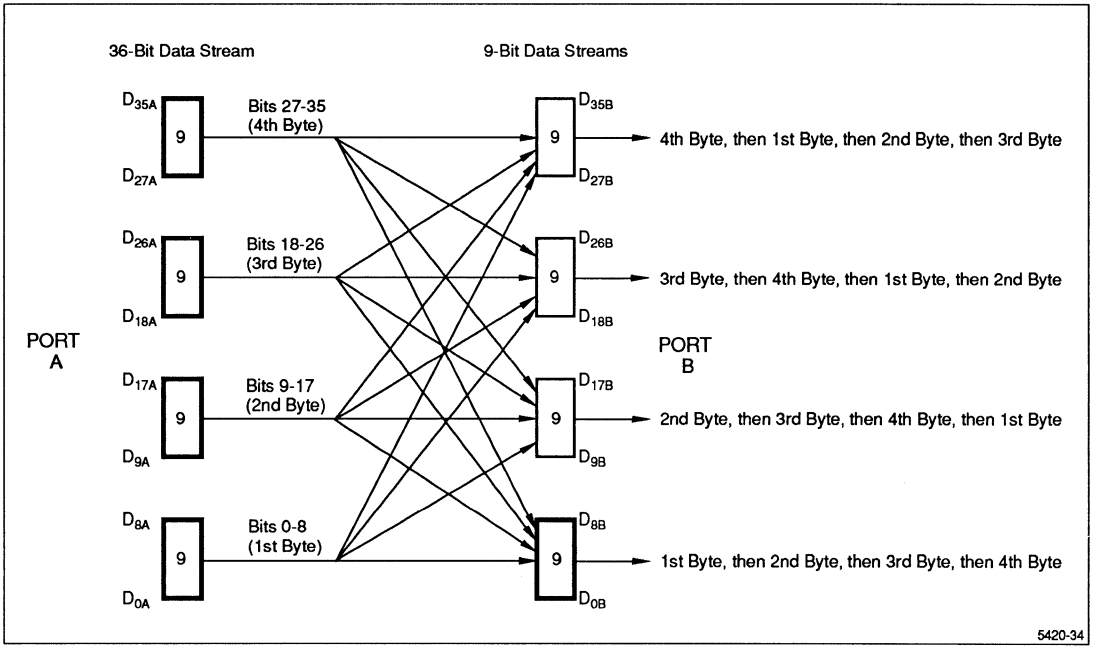


Figure 6b. 36-to-9 Funneling Through FIFO #1

NOTES:

1. The heavy black borders on register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 6a) or bytes (Figure 6b) are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to read D_{0B} – D_{35B}. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

PORT B WORD-WIDTH SELECTION

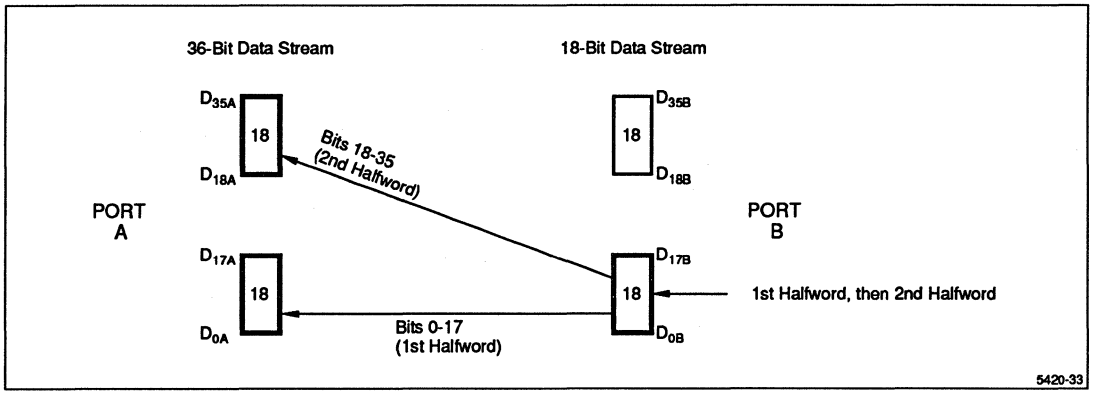


Figure 7a. 18-to-36 Defunneling Through FIFO #2

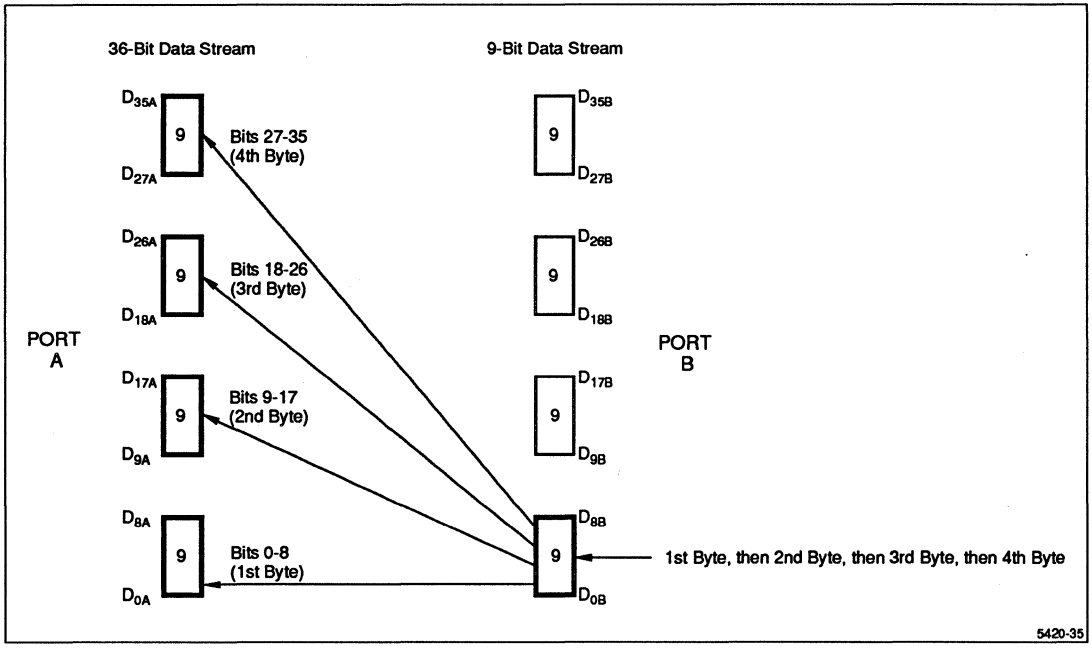
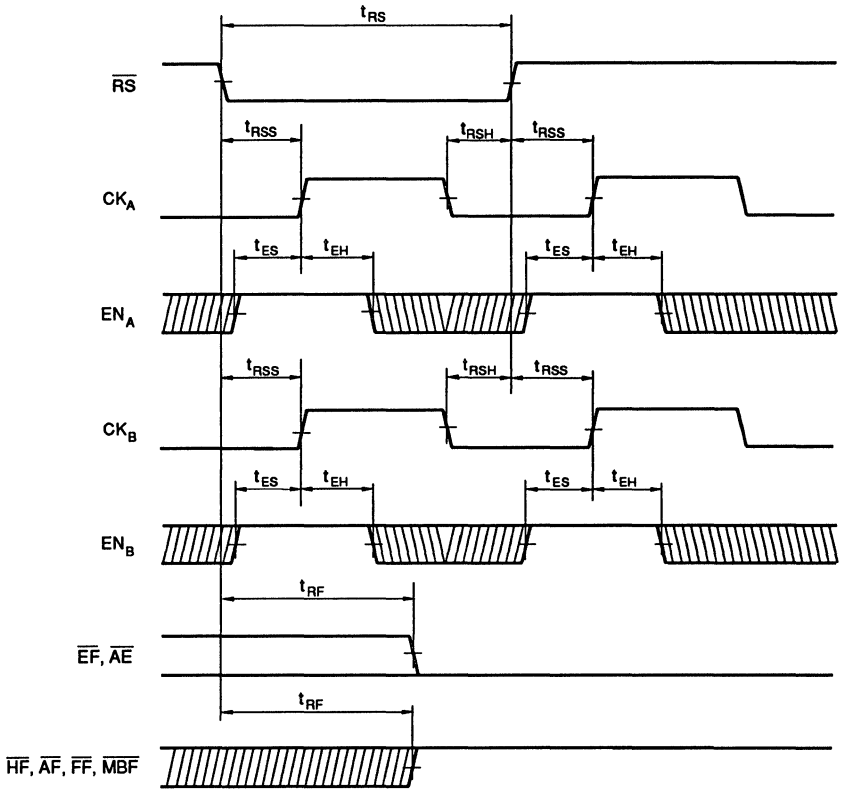


Figure 7b. 9-to-36 Defunneling Through FIFO #2

NOTES:

1. The heavy black borders on register segments indicate the only data paths used. The other byte segments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords (Figure 7a) or bytes (Figure 7b) are transferred in parallel form from Port B to Port A.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to send data. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

TIMING DIAGRAMS



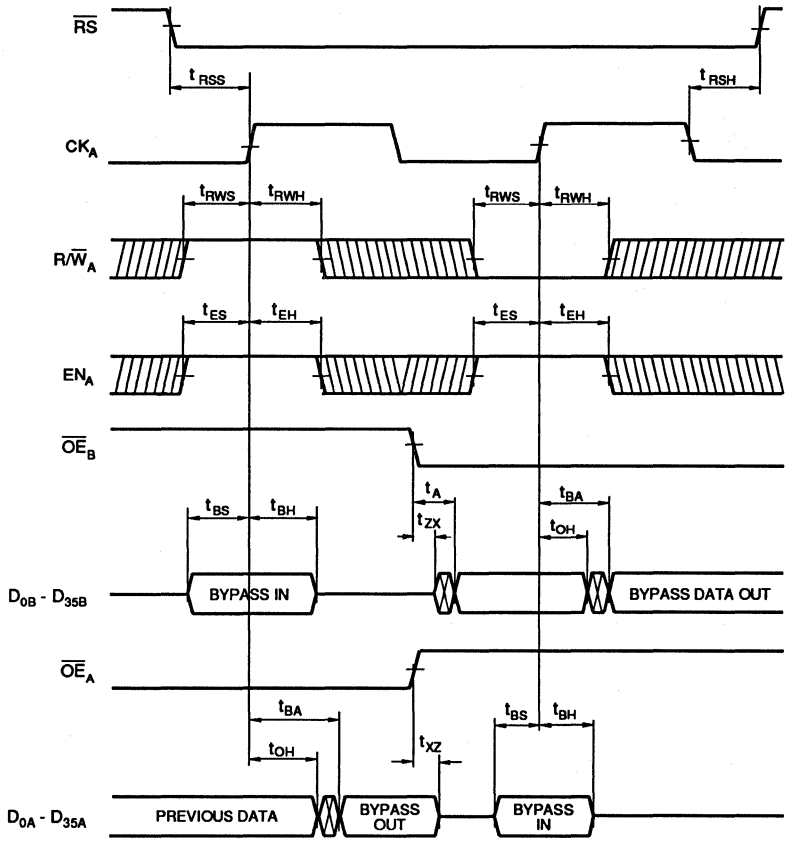
NOTES:

1. RS overrides all other input signals, and operates asynchronously. RS operates whether or not EN_A and/or EN_B are asserted.
2. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity check is initialized to odd byte parity at reset.
4. The AE and AF flag offsets are initialized to eight locations from the boundary at reset.

5420-26

Figure 8. Reset Timing

TIMING DIAGRAMS (cont'd)



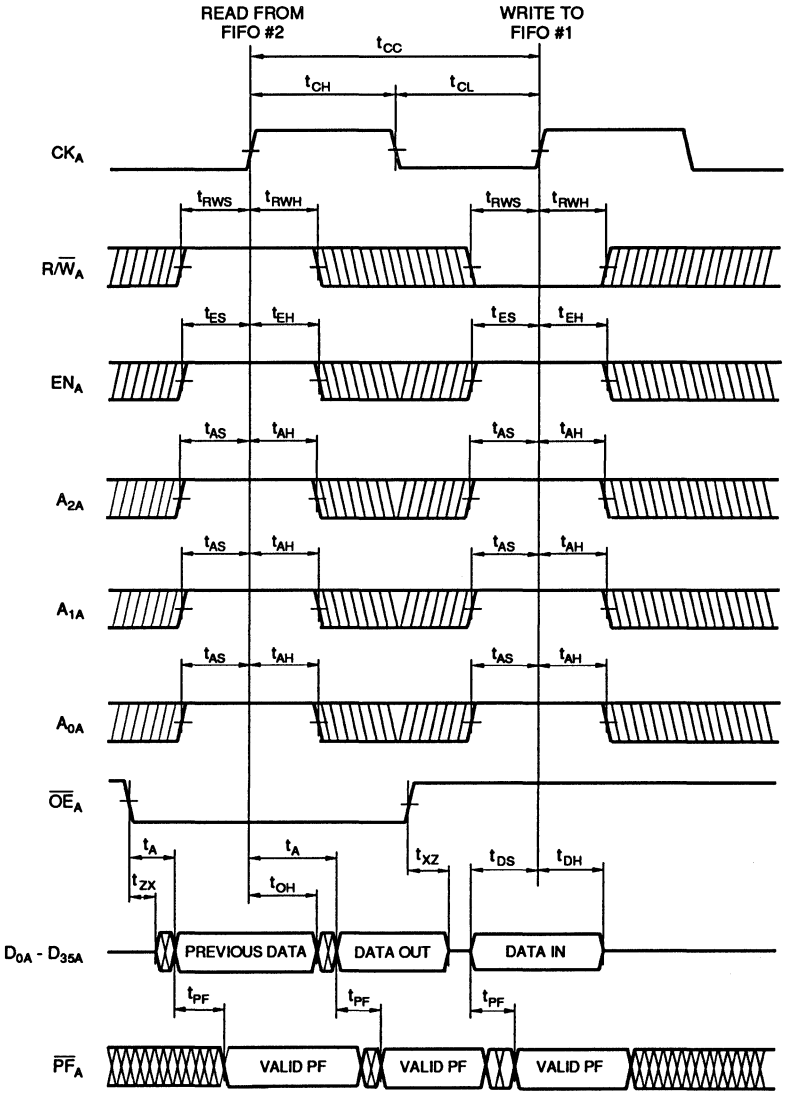
NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, and EN_A control the transmission of data between ports at reset.

5420-27

Figure 9. Data Bypass Timing

TIMING DIAGRAMS (cont'd)



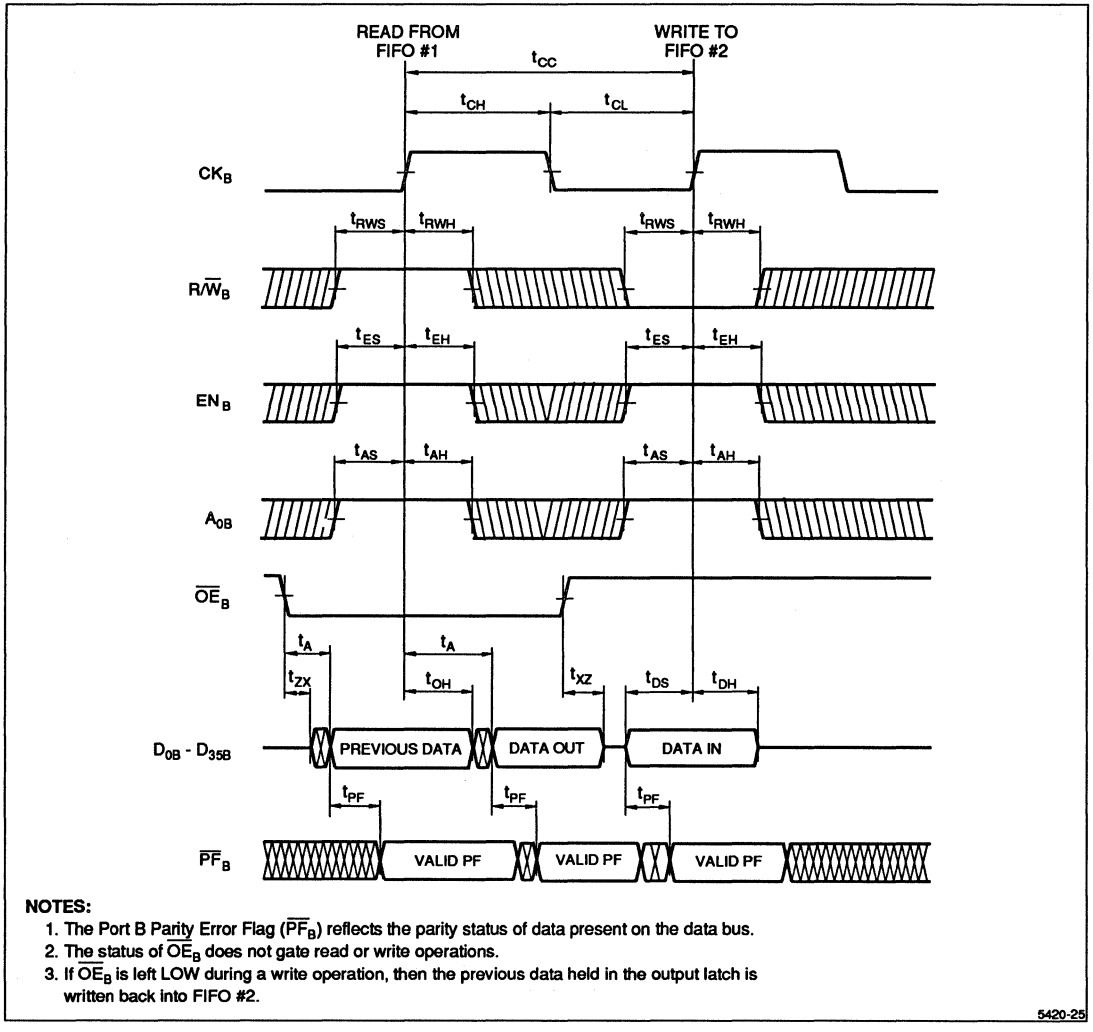
NOTES:

1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

5420-24

Figure 10. Port A FIFO Read/Write

TIMING DIAGRAMS (cont'd)



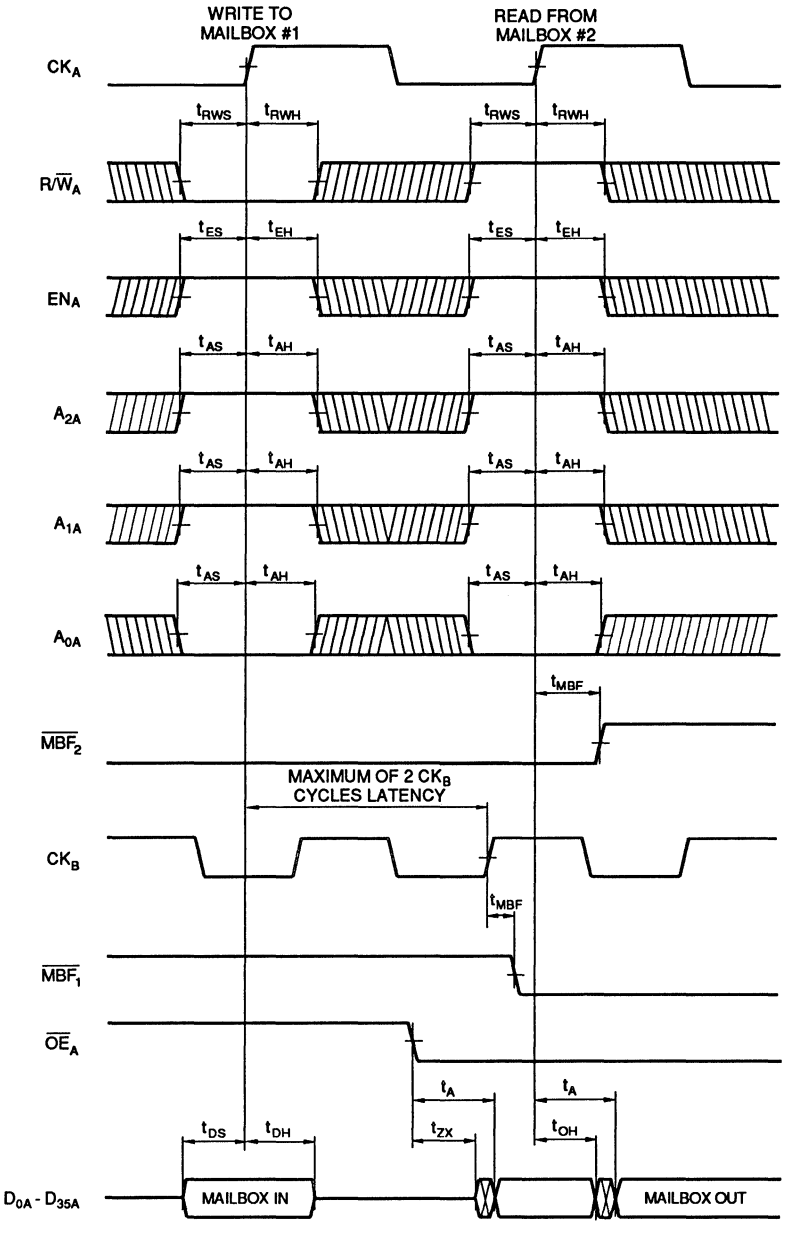
NOTES:

1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

5420-25

Figure 11. Port B FIFO Read/Write

TIMING DIAGRAMS (cont'd)



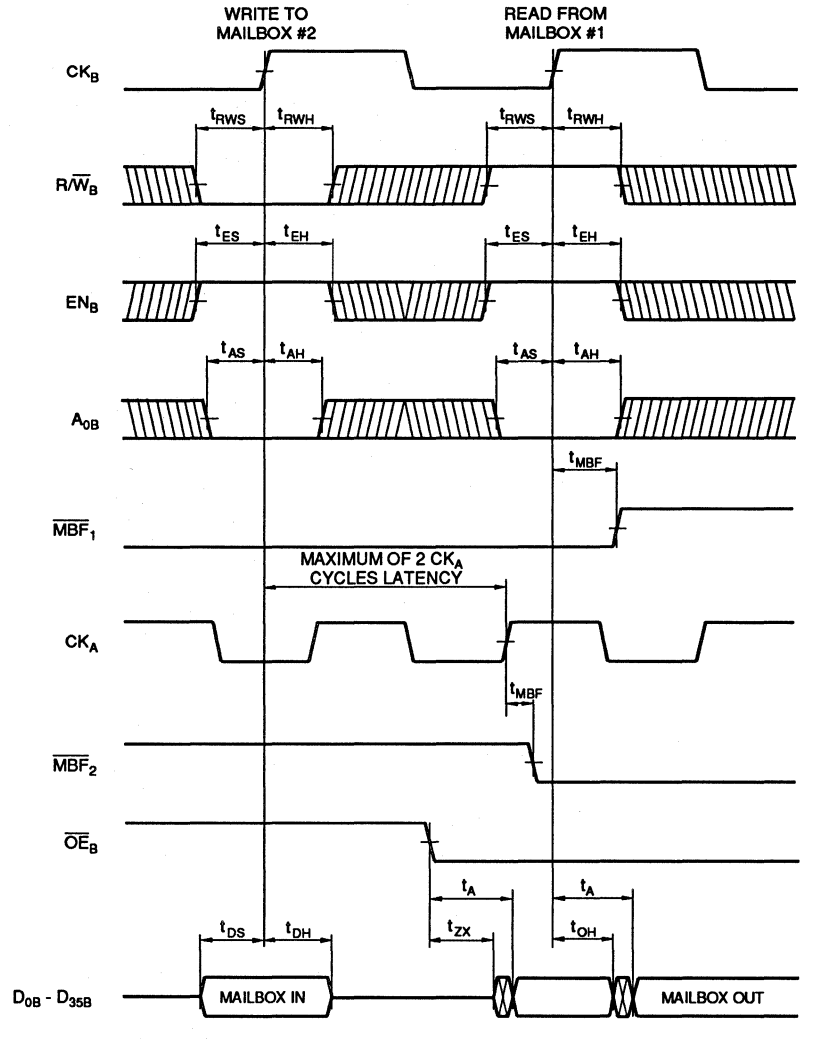
NOTES:

1. Both edges of $\overline{MBF_2}$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF_1}$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of 2 CK_B clock cycles of synchronization latency before $\overline{MBF_1}$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

5420-22

Figure 12. Port A Mailbox Access

TIMING DIAGRAMS (cont'd)



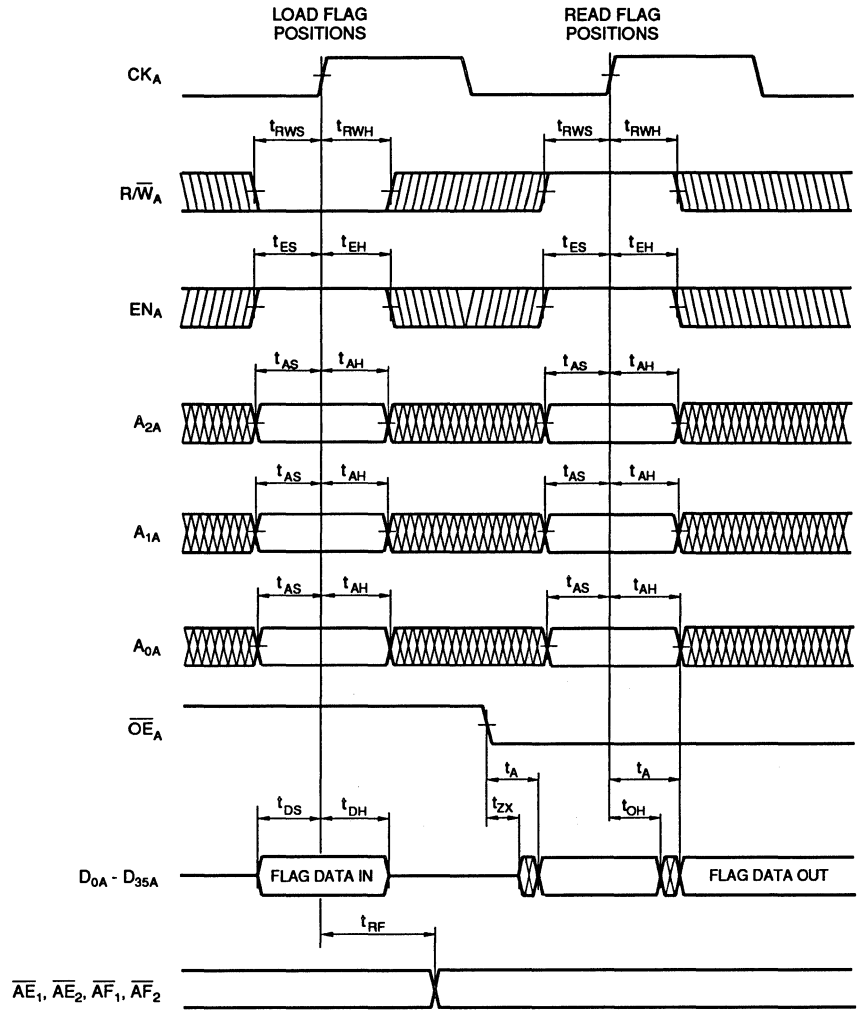
NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of 2 CK_A clock cycles of synchronization latency before $\overline{MBF}_2$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

5420-23

Figure 13. Port B Mailbox Access

TIMING DIAGRAMS (cont'd)



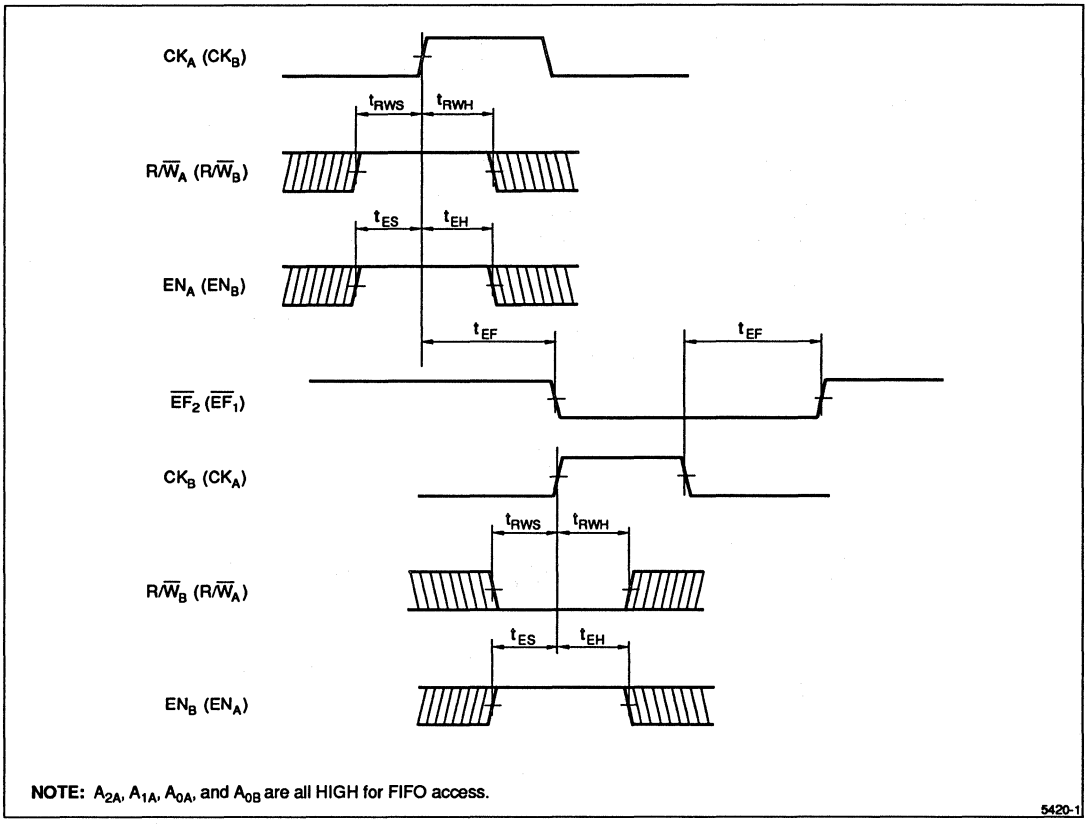
NOTES:

1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}.

5420-18

Figure 14. Flag Programming

TIMING DIAGRAMS (cont'd)



NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all HIGH for FIFO access.

5420-1

Figure 15. Empty Flag Timing

TIMING DIAGRAMS (cont'd)

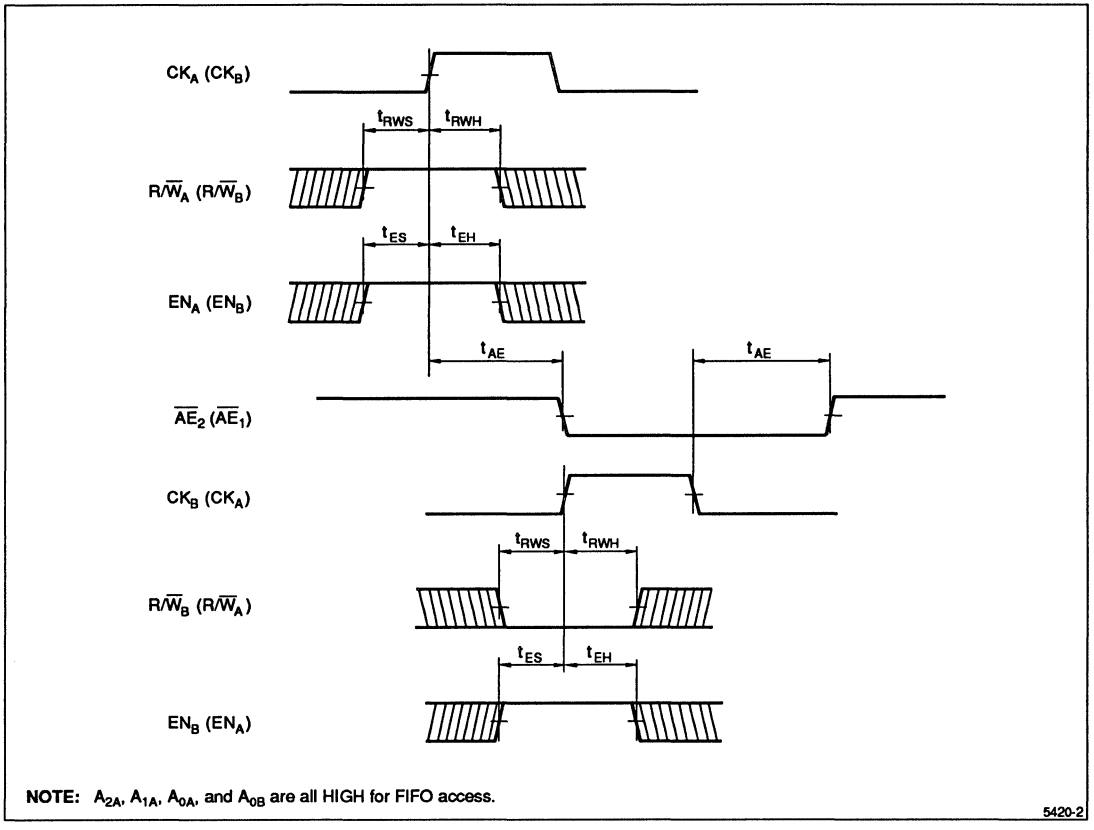


Figure 16. Almost-Empty Flag Timing

TIMING DIAGRAMS (cont'd)

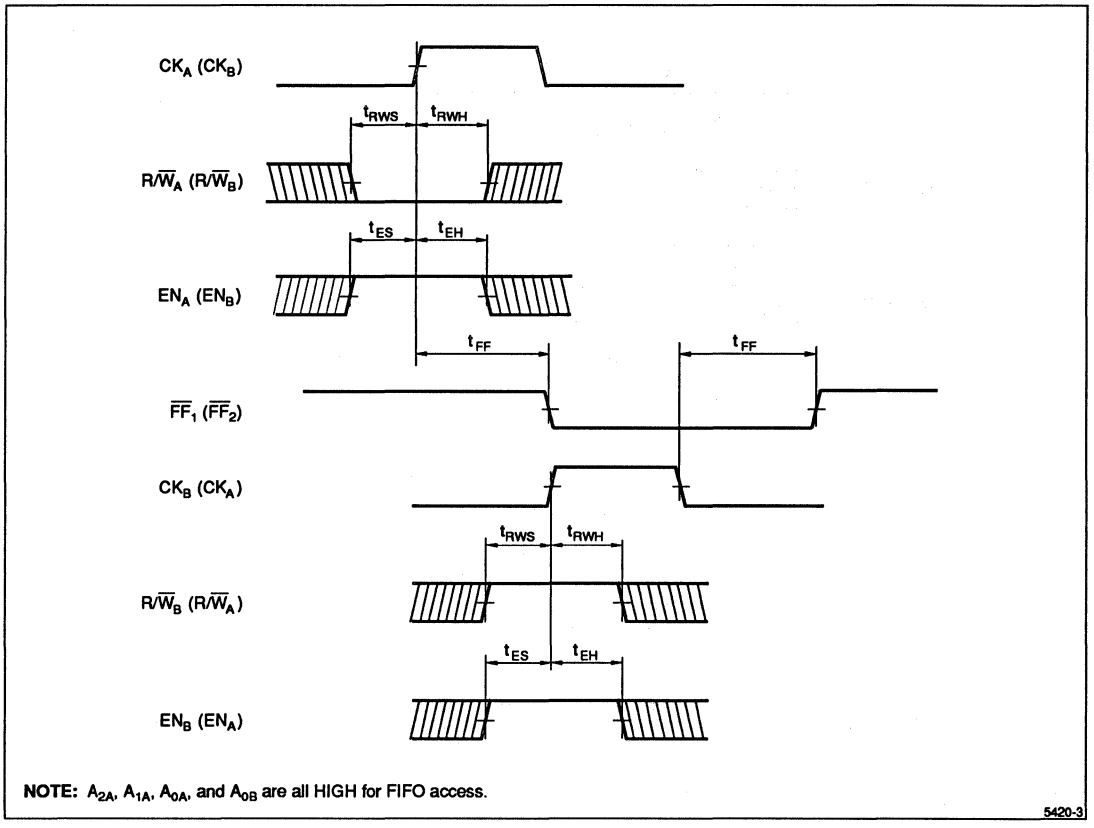


Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

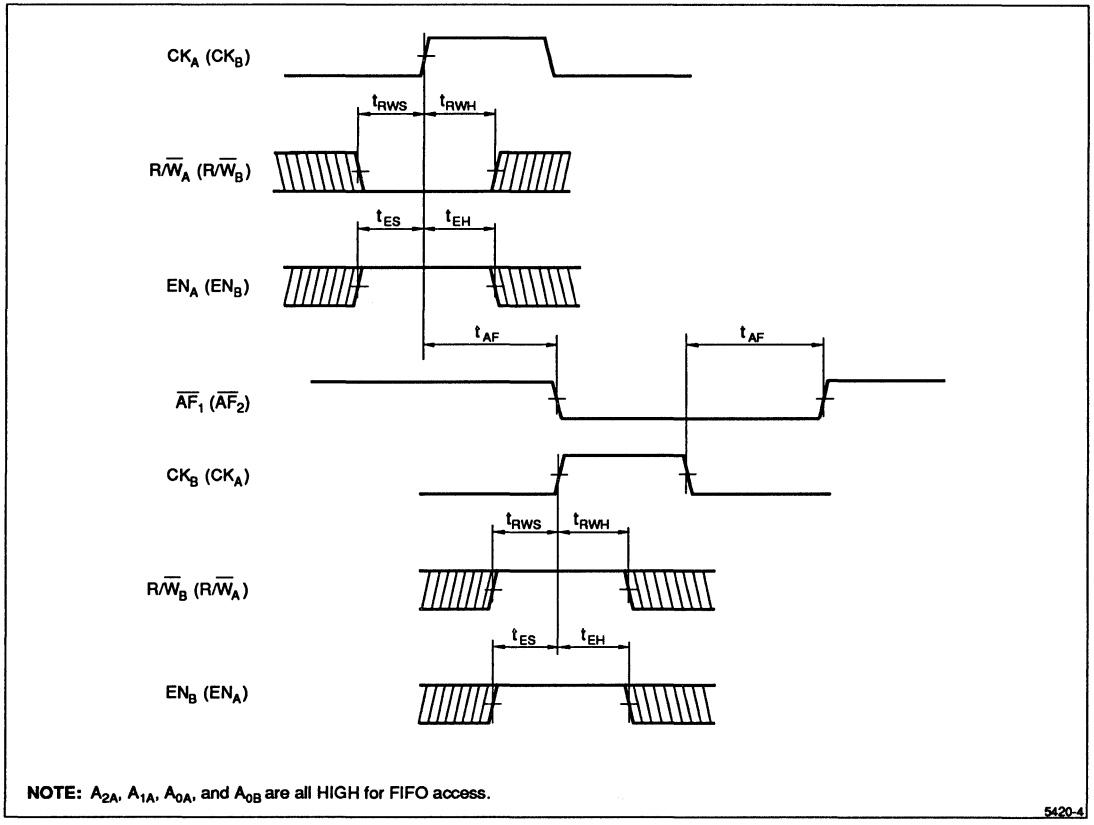


Figure 18. Almost-Full Flag Timing

TIMING DIAGRAMS (cont'd)

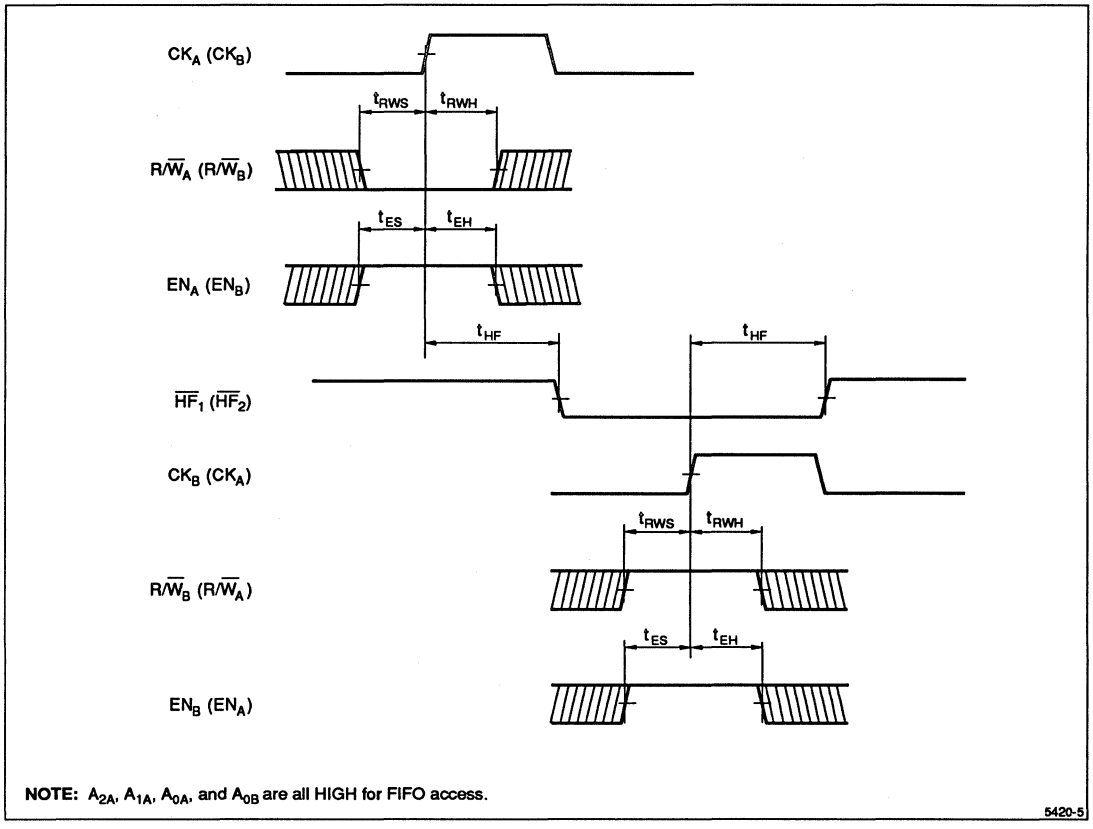
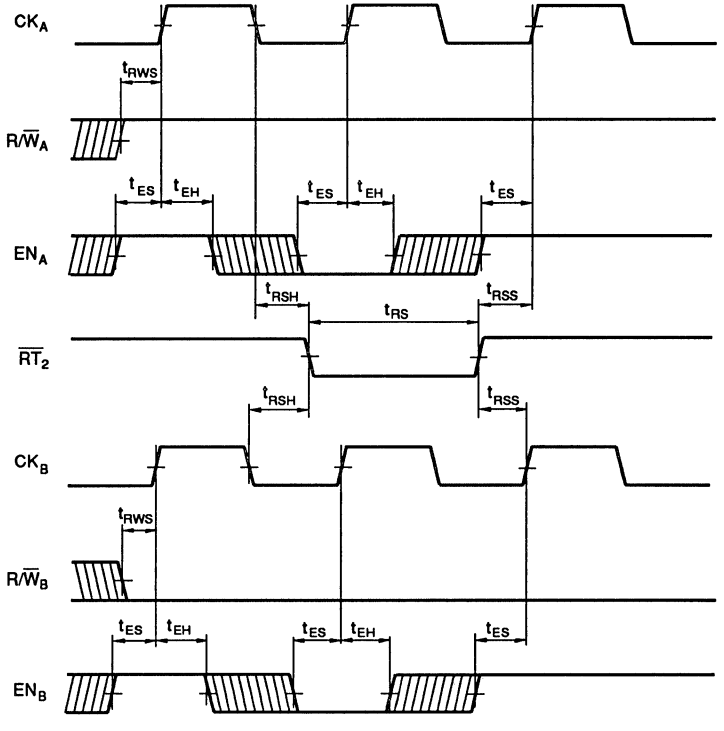


Figure 19. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)



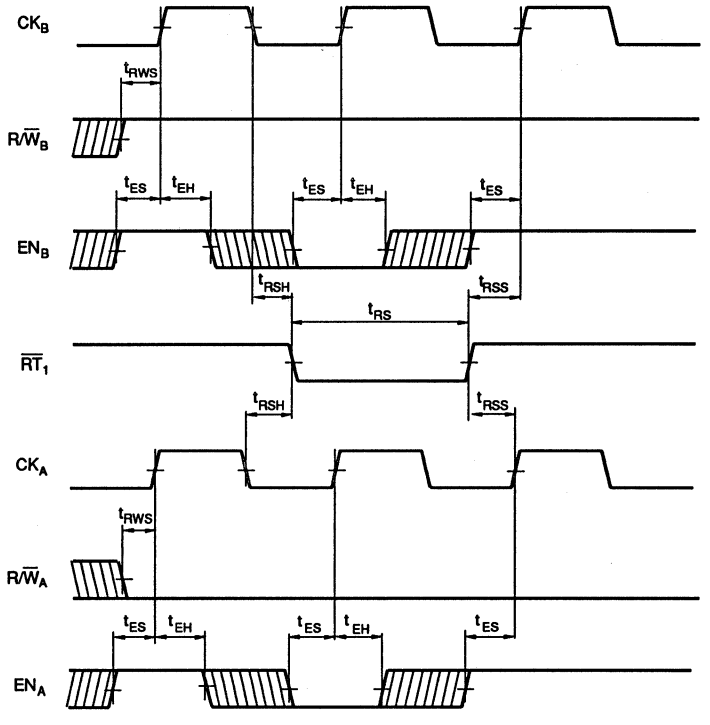
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.

5420-20

Figure 20. FIFO #2 Retransmit

TIMING DIAGRAMS (cont'd)



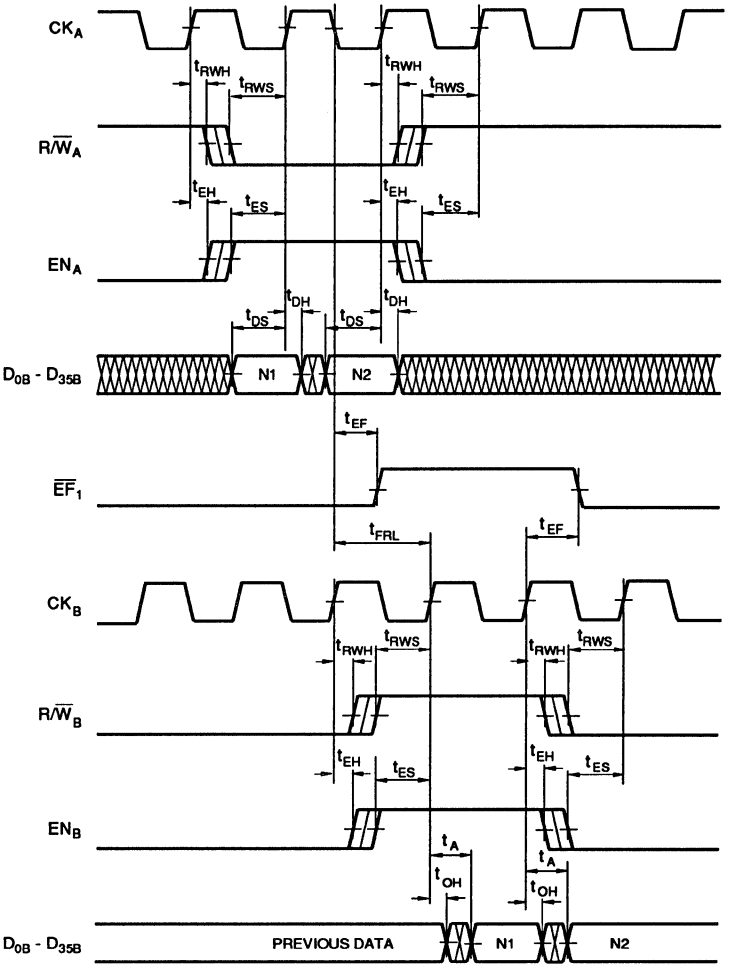
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.

5420-21

Figure 21. FIFO #1 Retransmit

TIMING DIAGRAMS (cont'd)



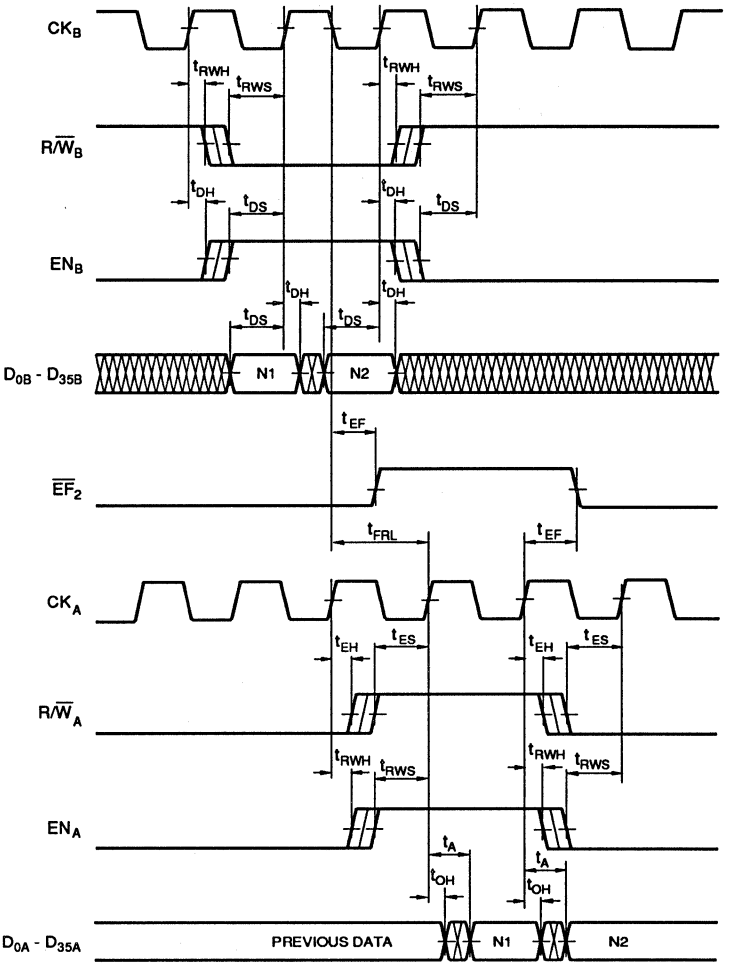
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

5420-16

Figure 22. FIFO #1 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



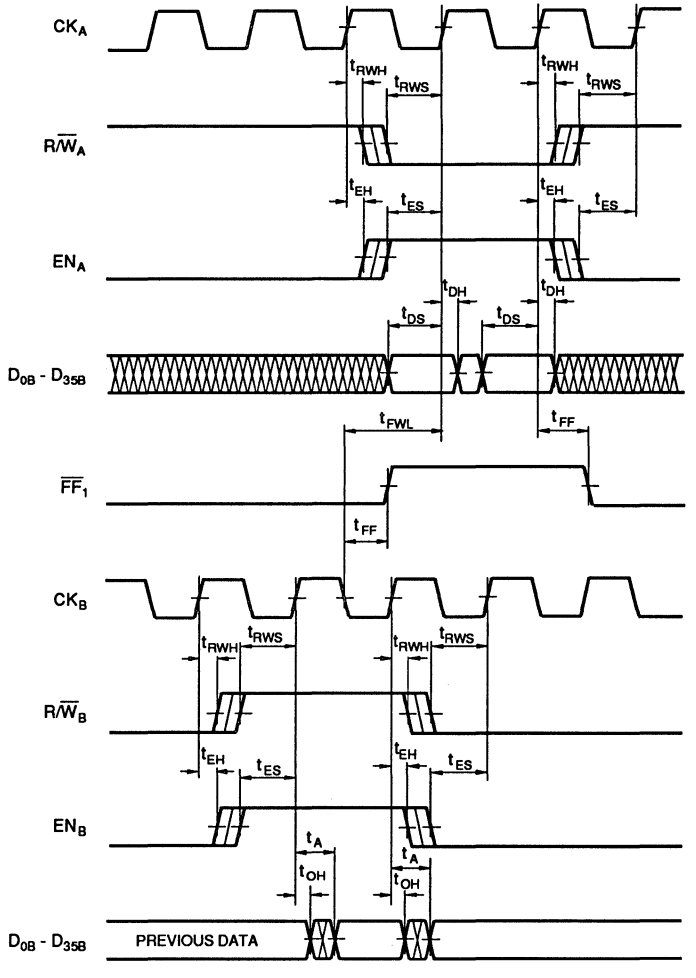
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

5420-17

Figure 23. FIFO #2 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



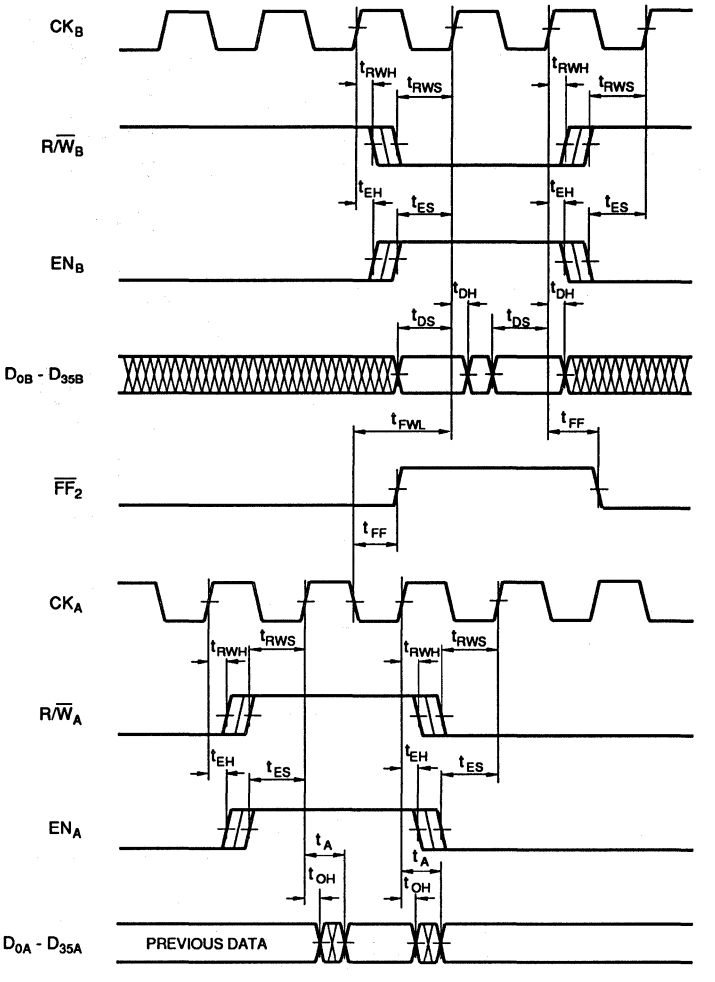
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5420-14

Figure 24. FIFO #1 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



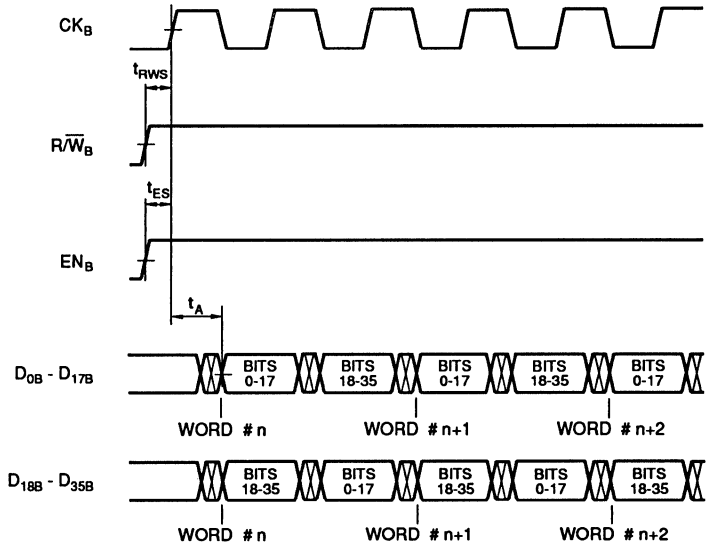
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held LOW.
3. $\overline{OE}_B$ is held HIGH.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5420-15

Figure 25. FIFO #2 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



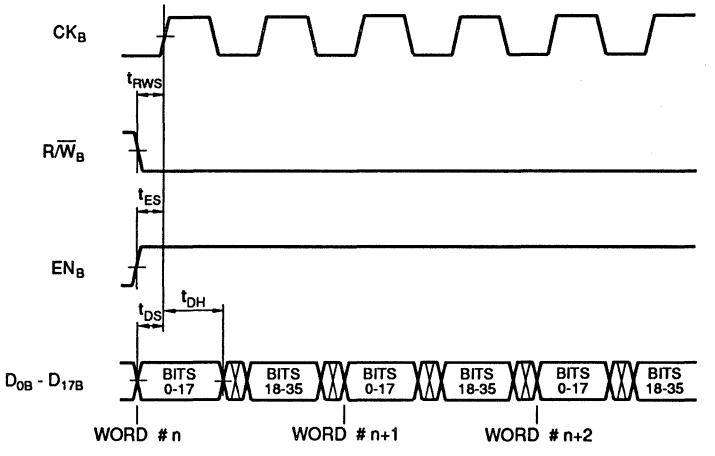
NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

5420-13

Figure 26. Port B Double-Byte FIFO #1 Read Access for 36-to-18 Funneling

TIMING DIAGRAMS (cont'd)

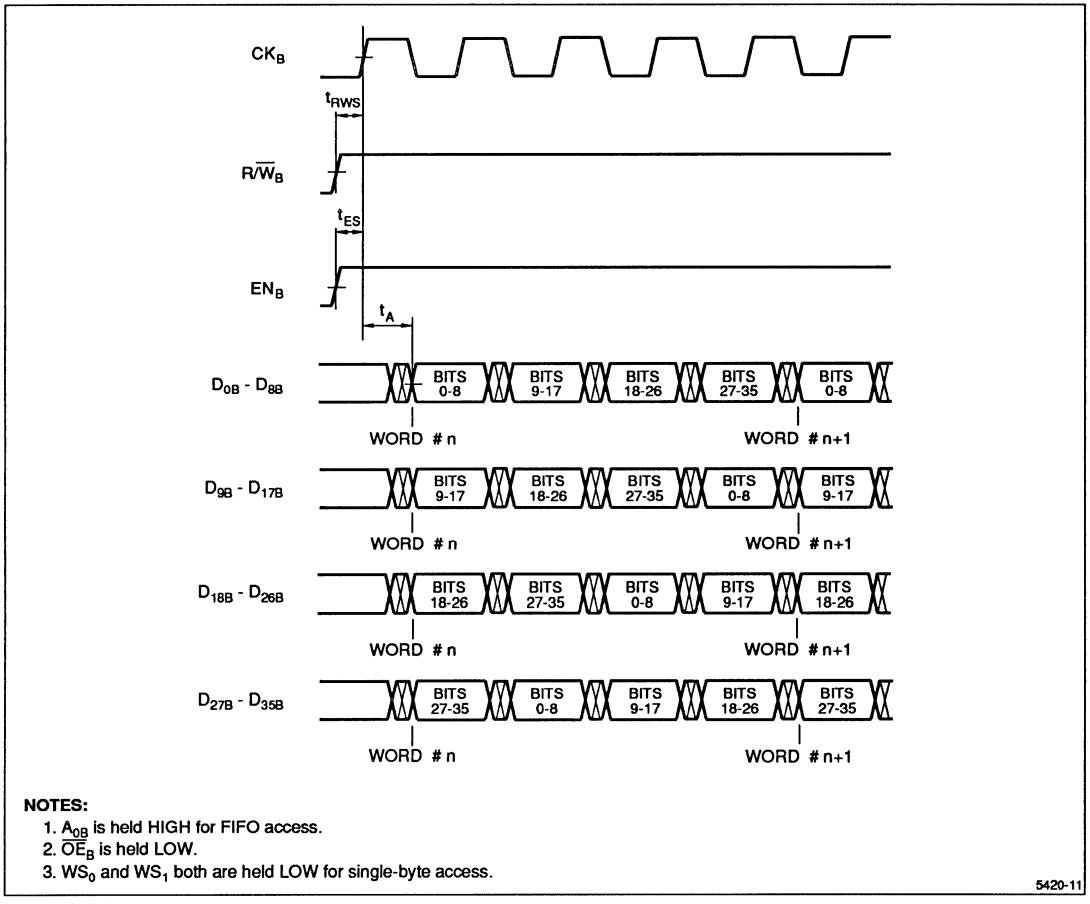


NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

5420-12

Figure 27. Port B Double-Byte FIFO #2 Write Access for 18-to-36 Defunneling

TIMING DIAGRAMS (cont'd)



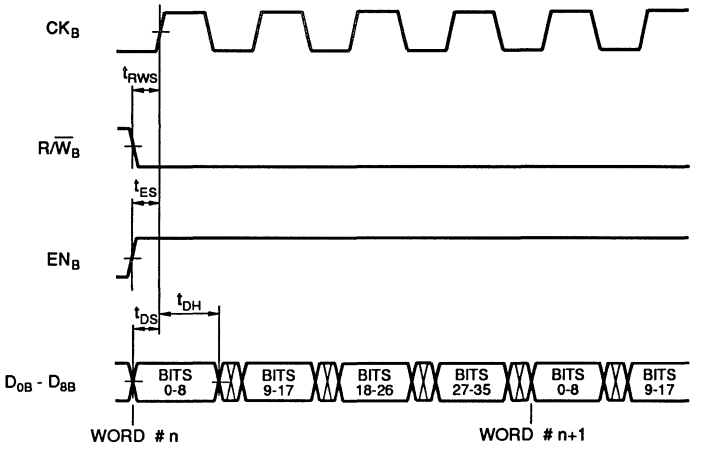
NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 and WS_1 both are held LOW for single-byte access.

5420-11

Figure 28. Port B Single-Byte FIFO #1 Read Access for 36-to-9 Funneling

TIMING DIAGRAMS (cont'd)

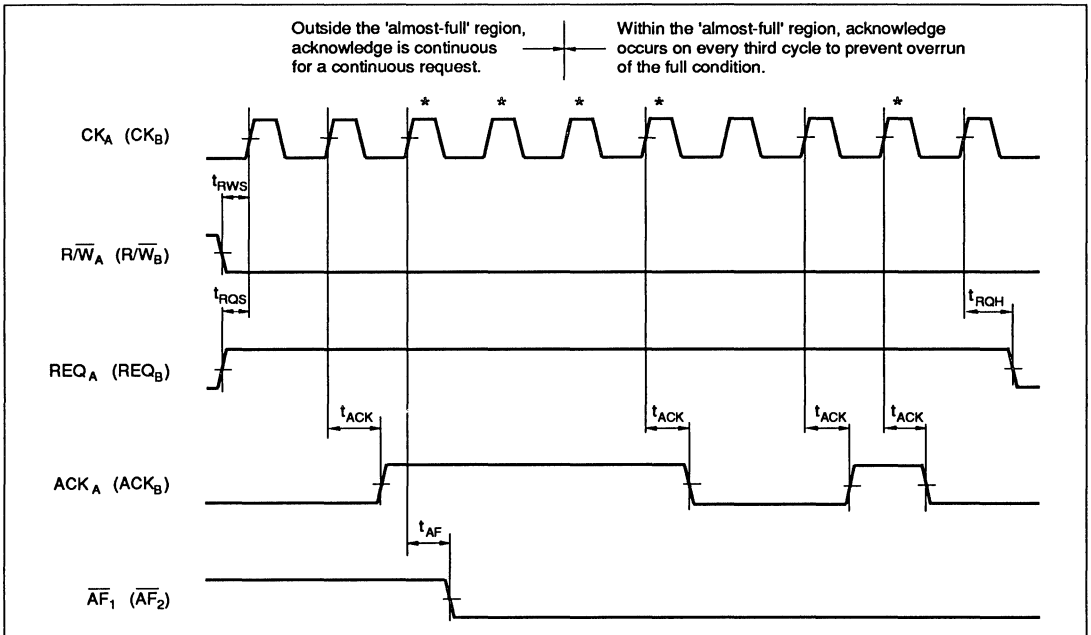


NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held HIGH.
3. WS_0 and WS_1 both are held LOW for single-byte access.

5420-10

Figure 29. Port B Single-Byte FIFO #2 Write Access for 9-to-36 Defunneling

TIMING DIAGRAMS (cont'd)



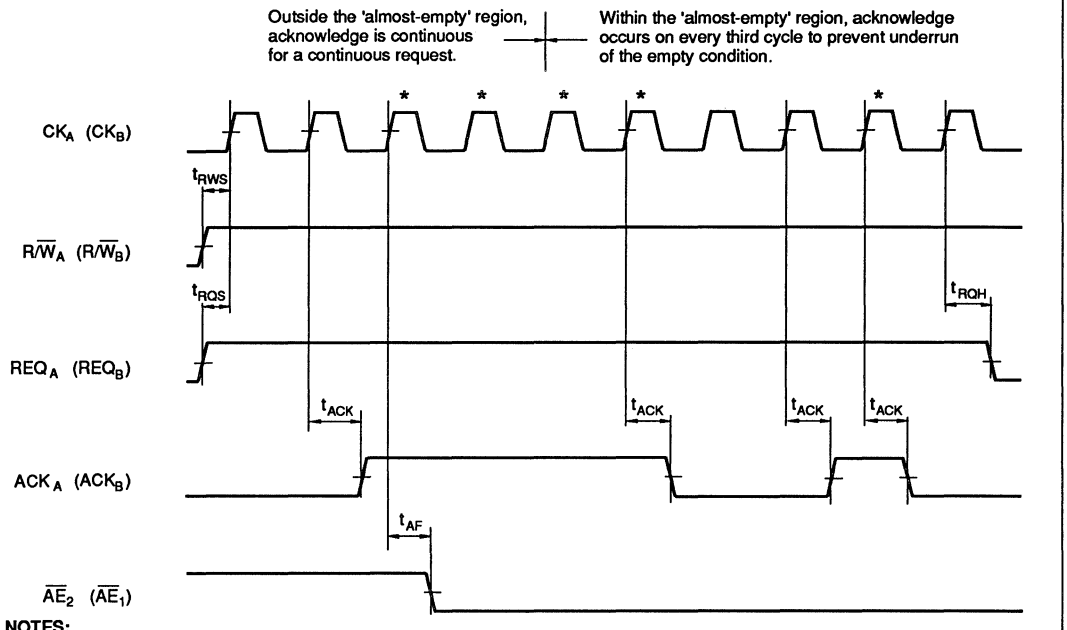
NOTES:

1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

5420-8

Figure 30. Write Request/Acknowledge Handshake

TIMING DIAGRAMS (cont'd)



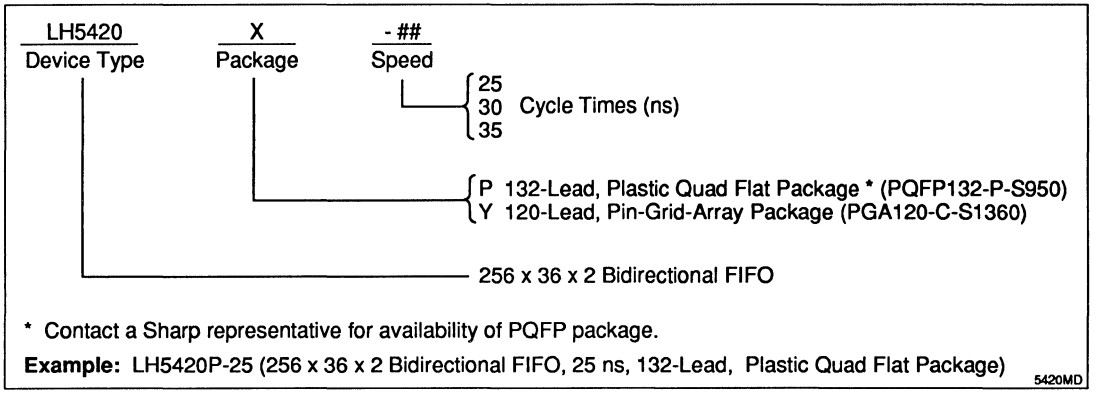
NOTES:

1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

5420-9

Figure 31. Read Request/Acknowledge Handshake

ORDERING INFORMATION



* Contact a Sharp representative for availability of PQFP package.

Example: LH5420P-25 (256 x 36 x 2 Bidirectional FIFO, 25 ns, 132-Lead, Plastic Quad Flat Package)

5420MD

LH540201/02/03

CMOS 512/1024/2048 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 12/15/20/25/35 ns
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM technology
- Independently-Synchronized Operation of Input Port and Output Port
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Retransmission Capability
- TTL-Compatible I/O
- 28-Pin PDIP and 32-Pin PLCC Packages
- Pin and Functionally Compatible with Sharp LH5496/97/98 and with Am/IDT/MS7201/02/03
- Control Signals Assertive-LOW for Noise Immunity

FUNCTIONAL DESCRIPTION

The LH540201/02/03 are FIFO (First-In, First-Out) memory devices, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 512, 1024, and 2048 9-bit words respectively. They follow the industry-standard architecture and package pinouts for 9-bit asynchronous FIFOs. Each 9-bit FIFO word may consist of a standard 8-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to overfill an already-full FIFO, or by attempting to read additional words from an already-empty FIFO. However, the Half-Full Flag is not available when a FIFO is operating in a depth-expanded configuration.

Data words emerge from the FIFO's output port in precisely the same order that they entered at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external

PIN CONNECTIONS

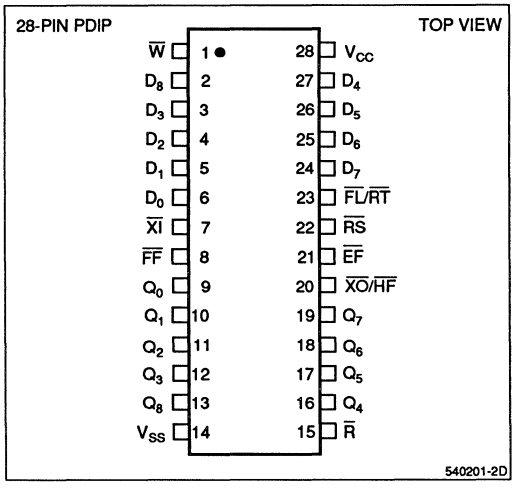


Figure 1. 28-Pin PDIP (Top View)

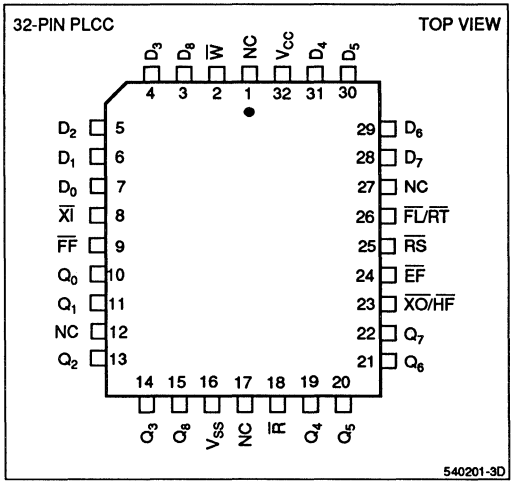


Figure 2. 32-Pin PLCC (Top View)

FUNCTIONAL DESCRIPTION (cont'd)

addressing information is required for the operation of the device. Also, drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of standard 9-bit asynchronous FIFOs; the only change is in the number of words implied by states of the Full and Half-Full status flags.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer value address may be read out *repeatedly*, an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available when a FIFO is operating in a depth-expanded configuration.

A cascading (depth-expansion) scheme may be implemented by use of the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO/HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual FIFO devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one FIFO device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL/RT}$) control input; the remaining FIFO devices are designated as 'slaves,' by tying their $\overline{FL/RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full flag and the retransmission capability are not available for either 'master' or 'slave' FIFO devices operating in cascaded mode.

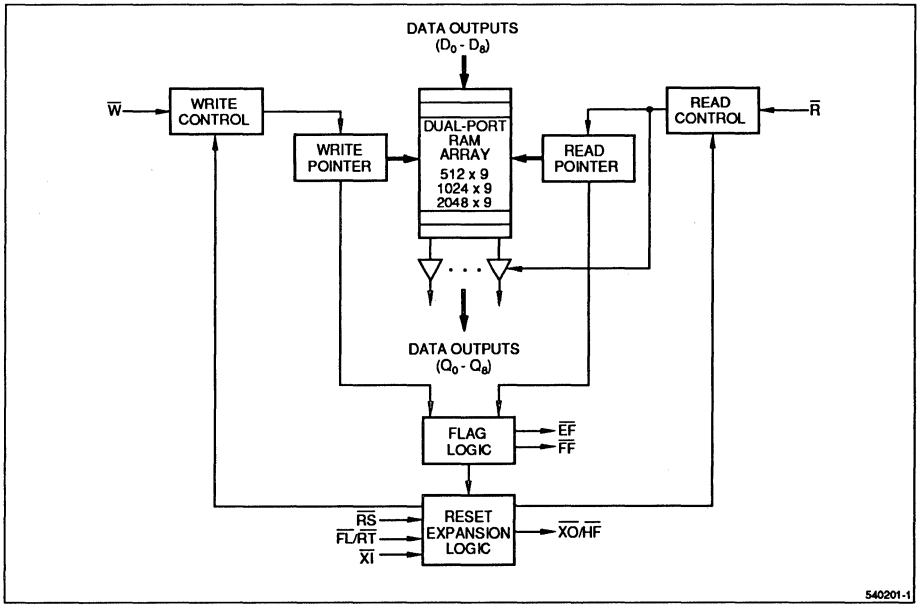


Figure 3. LH540201/02/03 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Request Input
$\overline{R}$	Read Request Input
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO/HF}$	Expansion Out/Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL/RT}$	First Load/Retransmit
$\overline{RS}$	Reset
V_{CC}	Positive Power Supply
V_{SS}	Ground

LH540204

PRODUCT PREVIEW

CMOS 4096 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35 ns
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM technology
- Independently-Synchronized Operation of Input Port and Output Port
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Retransmission Capability
- TTL-Compatible I/O
- 28-Pin PDIP and 32-Pin PLCC Packages
- Pin and Functionally Compatible with Sharp LH5499 and with Am/IDT/MS7204
- Control Signals Assertive-LOW for Noise Immunity

FUNCTIONAL DESCRIPTION

The LH540204 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 4096 9-bit words. It follows the industry-standard architecture and package pinouts for 9-bit asynchronous FIFOs. Each 9-bit FIFO word may consist of a standard 8-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to overfill an already-full FIFO, or by attempting to read additional words from an already-empty FIFO. However, the Half-Full Flag is not available when a FIFO is operating in a depth-expanded configuration.

Data words emerge from the FIFO's output port in precisely the same order that they entered at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the

PIN CONNECTIONS

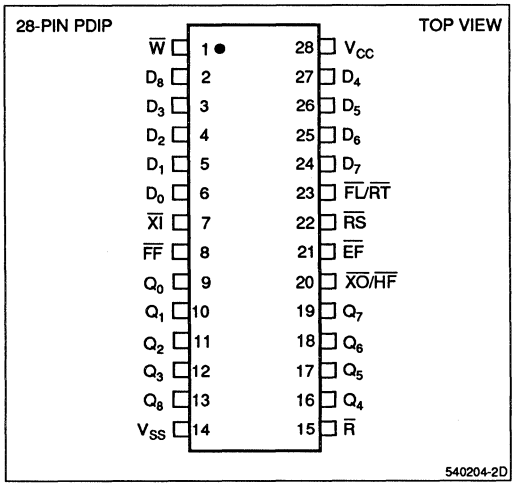


Figure 1. 28-Pin PDIP (Top View)

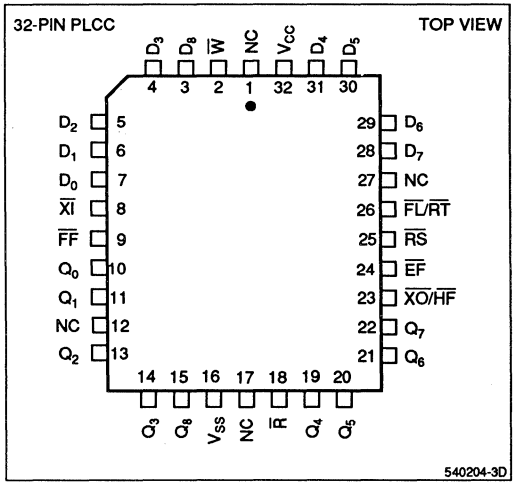


Figure 2. 32-Pin PLCC (Top View)

FUNCTIONAL DESCRIPTION (cont'd)

device. Also, drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of standard 9-bit asynchronous FIFOs; the only change is in the number of words implied by states of the Full and Half-Full status flags.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer value address may be read out *repeatedly*, an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available when a FIFO is operating in a depth-expanded configuration.

A cascading (depth-expansion) scheme may be implemented by use of the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual FIFO devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one FIFO device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining FIFO devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full flag and the retransmission capability are not available for either 'master' or 'slave' FIFO devices operating in cascaded mode.

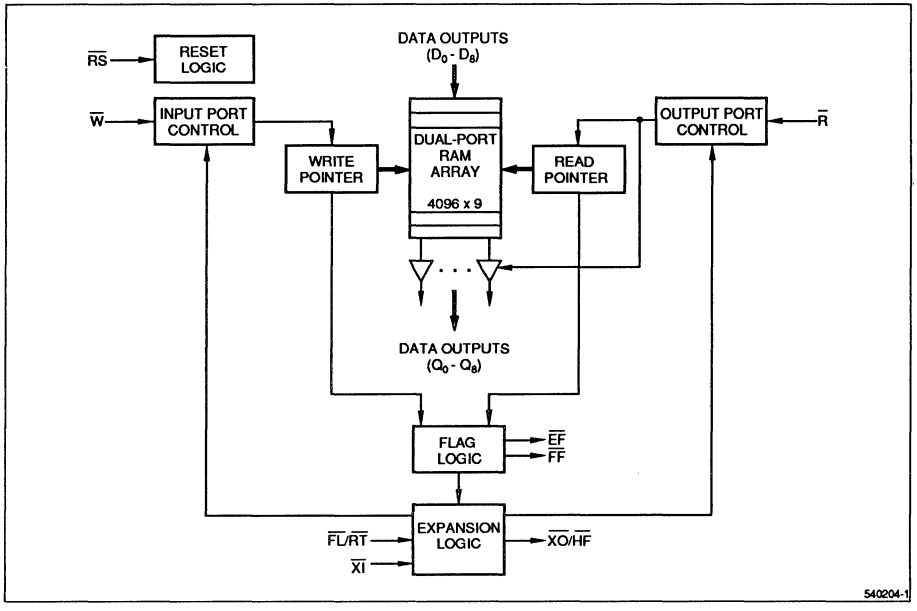


Figure 3. LH540204 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Request Input
$\overline{R}$	Read Request Input
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO}/\overline{HF}$	Expansion Out/Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL}/\overline{RT}$	First Load/Retransmit
$\overline{RS}$	Reset
V_{CC}	Positive Power Supply
V_{SS}	Ground

LH540205

PRODUCT PREVIEW

CMOS 8192 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35 ns
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM technology
- Independently-Synchronized Operation of Input Port and Output Port
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Retransmission Capability
- TTL-Compatible I/O
- 28-Pin PDIP and 32-Pin PLCC Packages
- Pin and Functionally Compatible with Am/IDT7205
- Control Signals Assertive-LOW for Noise Immunity

FUNCTIONAL DESCRIPTION

The LH540205 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 8192 9-bit words. It follows the industry-standard architecture and package pinouts for 9-bit asynchronous FIFOs. Each 9-bit FIFO word may consist of a standard 8-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to overfill an already-full FIFO, or by attempting to read additional words from an already-empty FIFO. However, the Half-Full Flag is not available when a FIFO is operating in a depth-expanded configuration.

Data words emerge from the FIFO's output port in precisely the same order that they entered at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the

PIN CONNECTIONS

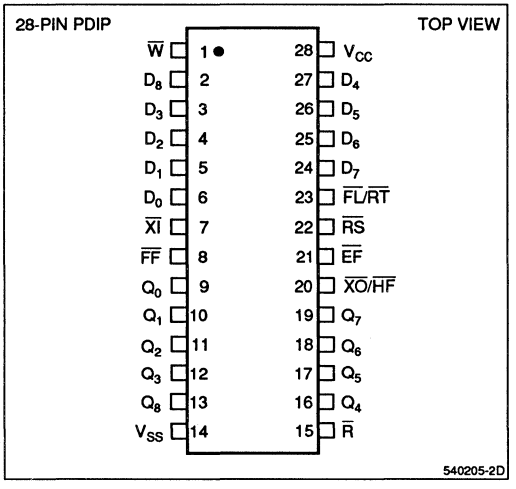


Figure 1. 28-Pin PDIP (Top View)

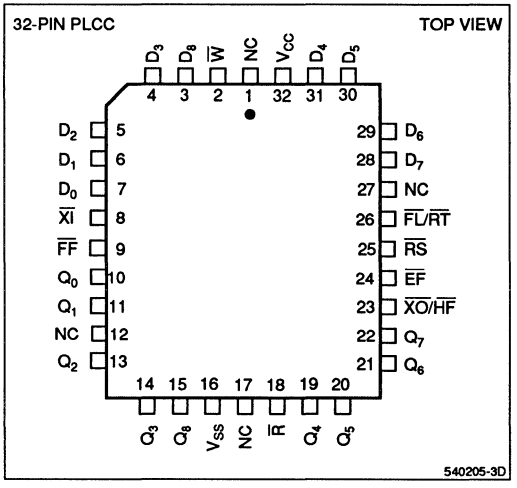


Figure 2. 32-Pin PLCC (Top View)

FUNCTIONAL DESCRIPTION (cont'd)

device. Also, drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of standard 9-bit asynchronous FIFOs; the only change is in the number of words implied by states of the Full and Half-Full status flags.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer value address may be read out *repeatedly*, an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available when a FIFO is operating in a depth-expanded configuration.

A cascading (depth-expansion) scheme may be implemented by use of the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO/HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual FIFO devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one FIFO device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL/RT}$) control input; the remaining FIFO devices are designated as 'slaves,' by tying their $\overline{FL/RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full flag and the retransmission capability are not available for either 'master' or 'slave' FIFO devices operating in cascaded mode.

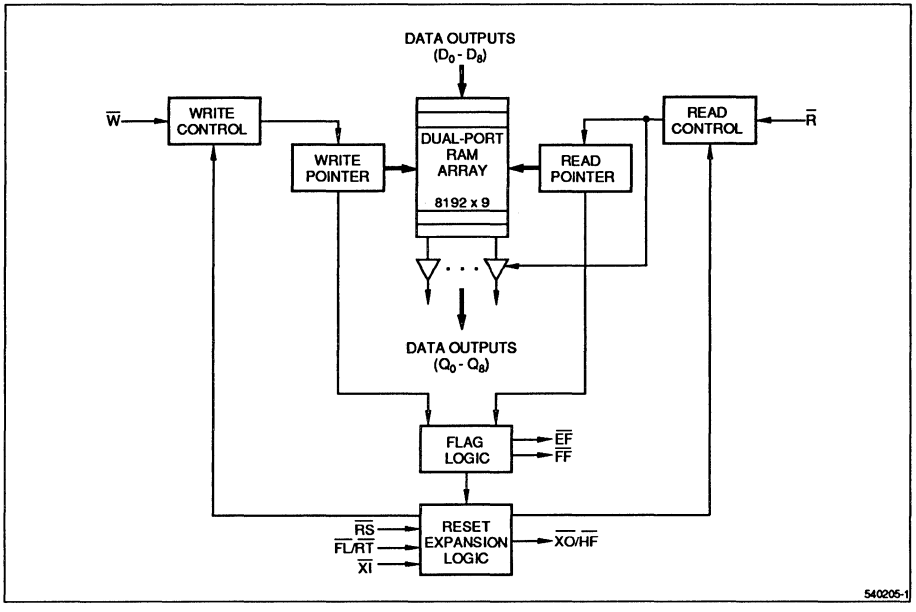


Figure 3. LH540205 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Request Input
$\overline{R}$	Read Request Input
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO/HF}$	Expansion Out/Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL/RT}$	First Load/Retransmit
$\overline{RS}$	Reset
V_{CC}	Positive Power Supply
V_{SS}	Ground

LH540206

PRODUCT PREVIEW

CMOS 16384 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35 ns
- Fast Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM technology
- Independently-Synchronized Operation of Input Port and Output Port
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Retransmission Capability
- TTL-Compatible I/O
- 28-Pin PDIP and 32-Pin PLCC Packages
- Pin and Functionally Compatible with IDT7206
- Control Signals Assertive-LOW for Noise Immunity

FUNCTIONAL DESCRIPTION

The LH540206 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 16384 9-bit words. It follows the industry-standard architecture and package pinouts for 9-bit asynchronous FIFOs. Each 9-bit FIFO word may consist of a standard 8-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to overfill an already-full FIFO, or by attempting to read additional words from an already-empty FIFO. However, the Half-Full Flag is not available when a FIFO is operating in a depth-expanded configuration.

Data words emerge from the FIFO's output port in precisely the same order that they entered at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the

PIN CONNECTIONS

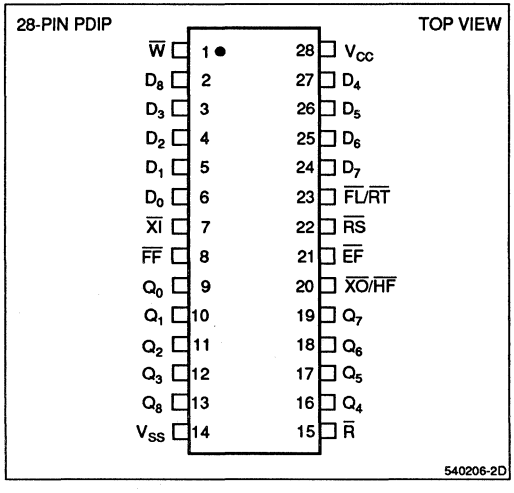


Figure 1. 28-Pin PDIP (Top View)

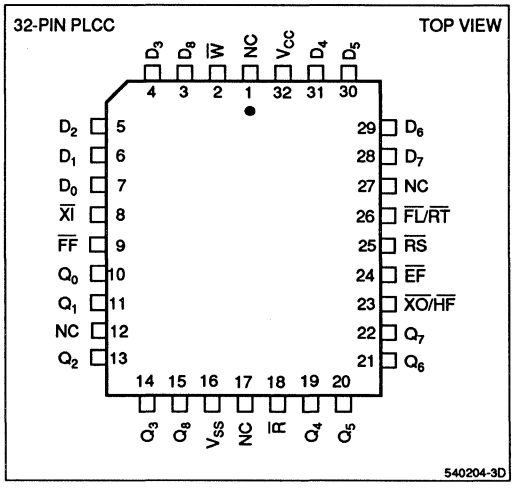


Figure 2. 32-Pin PLCC (Top View)

FUNCTIONAL DESCRIPTION (cont'd)

device. Also, drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of standard 9-bit asynchronous FIFOs; the only change is in the number of words implied by states of the Full and Half-Full status flags.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer value address may be read out *repeatedly*, an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available when a FIFO is operating in a depth-expanded configuration.

A cascading (depth-expansion) scheme may be implemented by use of the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual FIFO devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one FIFO device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining FIFO devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full flag and the retransmission capability are not available for either 'master' or 'slave' FIFO devices operating in cascaded mode.

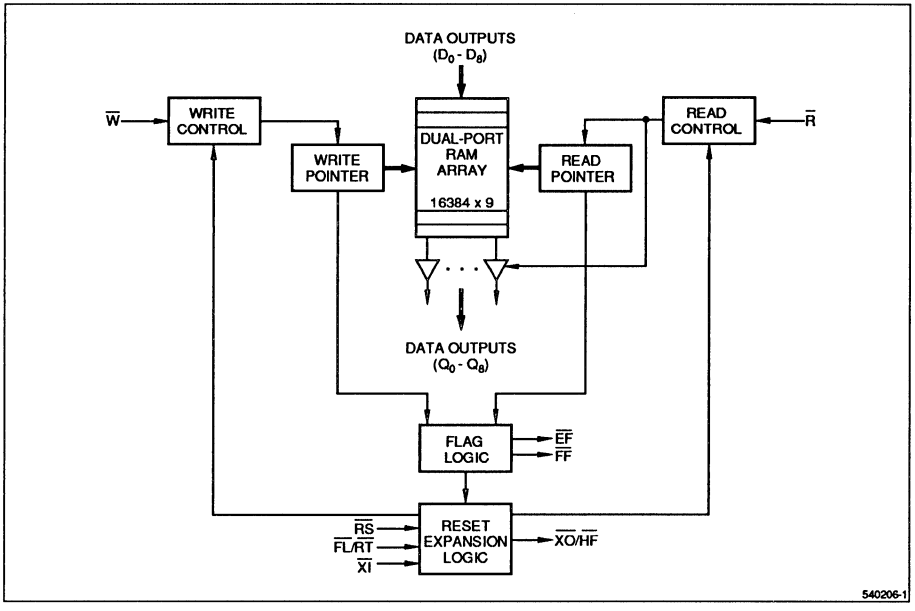


Figure 3. LH540206 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs
$\overline{W}$	Write Request Input
$\overline{R}$	Read Request Input
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag

PIN	DESCRIPTION
$\overline{XO}/\overline{HF}$	Expansion Out/Half-Full Flag
$\overline{XI}$	Expansion In
$\overline{FL}/\overline{RT}$	First Load/Retransmit
$\overline{RS}$	Reset
V_{CC}	Positive Power Supply
V_{SS}	Ground

LH540215/25

ADVANCE INFORMATION

512 × 18 / 1024 × 18 Synchronous FIFO

FEATURES

- Fast Cycle Times: 15/20/25/35 ns
- Pin-Compatible Drop-In Replacements for IDT72215A/25A FIFOs; Default Operating Mode is Functionally IDT-Compatible
- Device Comes Up into Known Default State at Reset; Programming is Allowed, but is not Required
- Fast Fall-Through Time Internal Memory Array Architecture Based on CMOS Dual-Port SRAM Technology, 512 × 18 or 1024 × 18
- 'Synchronous' Enable-Plus-Clock Control at Both Input Port and Output Port
- Independently-Synchronized Operation of Input Port and Output Port
- Control Inputs Sampled on Rising Clock Edge
- All Control Signals Assertive-LOW for Noise Immunity
- May be Cascaded for Increased Depth or Paralleled for Increased Width
- 16-mA-I_{OL} Three-State Outputs
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- Almost-Full, Half-Full, and Almost-Empty Flags may be Made Completely Synchronous, in Optional Enhanced Operating Mode
- Duplicate Enables for Interlocked Paralleled FIFO Operation, for 36-Bit Data Width, when Appropriately Connected, in Optional Enhanced Operating Mode
- Disabling Three-State Outputs Suppresses Reading, in Optional Enhanced Operating Mode
- Data Retransmit Function
- TTL/CMOS-Compatible I/O
- Space-Saving 68-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH540215/25 are FIFO (First-In, First-Out) memory devices, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 512 or 1024 18-bit words respectively. They can replace two or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Their architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flag offsets are programmable over the entire FIFO depth; but, during a reset operation, each of these is initialized to a default offset of about 1/8 of the depth of one single FIFO, from the respective FIFO boundary. If this default offset is satisfactory, no further programming is required.

After a reset operation, these FIFOs operate in the Default Operating Mode. In this mode, each part is pin-compatible and functionally-compatible with the IDT72215A/25A part of similar depth and speed grade. However, the system may program the Command Register to activate *any or all* of the features available in the optional Enhanced Operating Mode, including selectable-clock-edge flag synchronization, and read inhibition when the data outputs are disabled. Interlocked-operation paralleling is also available, by appropriate interconnection of the FIFO's expansion inputs. Also, assertion of the $\overline{\text{EMODE}}$ control input leaves Command Register bits 06-11 set, which causes the FIFO to operate in the Enhanced Operating Mode.

The Retransmit control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address pointer address may be read out *repeatedly*, an arbitrary number of times.

FUNCTIONAL DESCRIPTION (cont'd)

The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available when a FIFO is operating in IDT-compatible depth-cascaded mode.

Programming the programmable-flag offsets, the number of FIFOs to be cascaded in depth, the timing synchronization of the various status flags, and the optional read-suppression functionality of $\overline{OE}$ may be individually controlled by asserting the signal $\overline{LD}$, without any reset operation. When $\overline{LD}$ is asserted, while writing is enabled by asserting $\overline{WEN}$, some or all of the input bus word $D_0 - D_{17}$ is used at the next rising edge of WCLK to program one or more of the resource registers on successive write clocks. Likewise, the values programmed into these resource registers may be read out for verification by asserting $\overline{REN}$, with the outputs $Q_0 - Q_{17}$ enabled. Reading out these resource registers should not be initiated while they are being written into.

Coordinated operation of two 18-bit FIFOs as one 36-bit FIFO may be ensured by 'interlocked' crosscoupling of status-flag outputs from each port to expansion inputs of the other one; that is, $\overline{EF}$ to $\overline{WXI}/WEN_2$, and $\overline{FF}$ to $\overline{RXI}/REN_2$, in *both* directions between two paralleled FIFOs. This 'interlocked' operation takes effect automatically, if two paralleled FIFOs are crossconnected in this manner. (See Table 2.) IDT-compatible depth cascading is no longer available when operating in this mode; however, pipelined depth cascading remains possible.

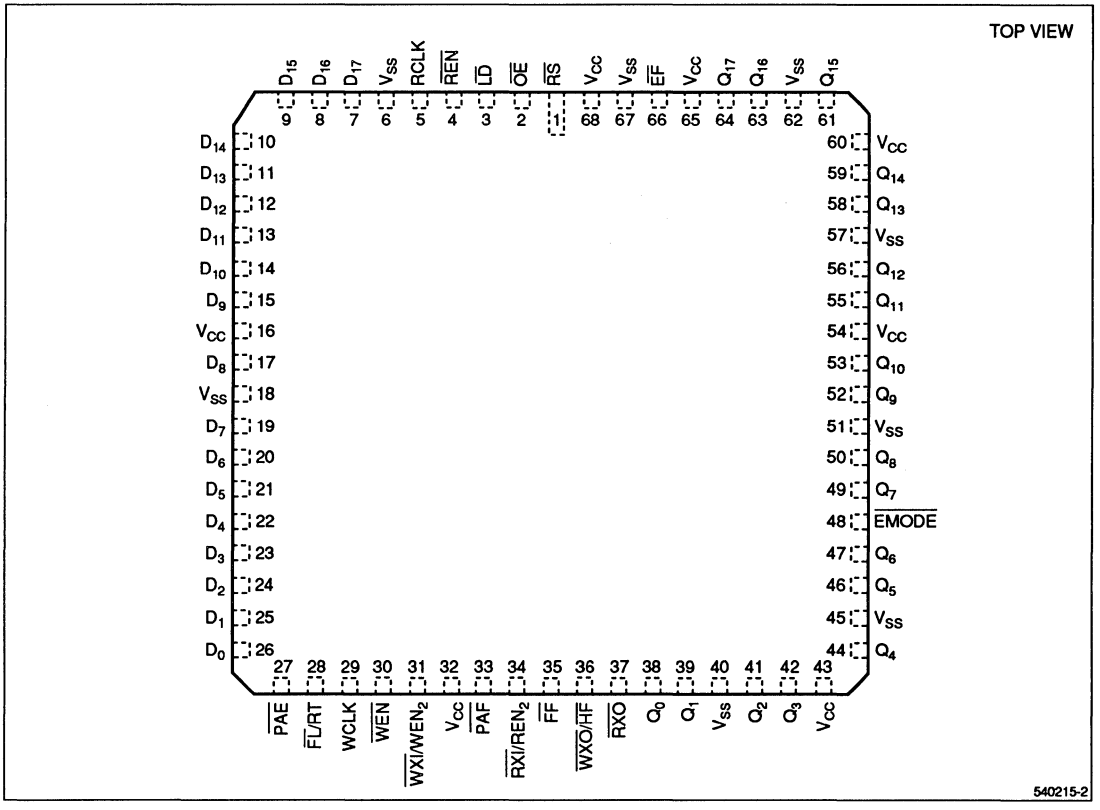


Figure 1. Pin Connections for PLCC Package

PIN DESCRIPTIONS

PIN	NAME	PIN TYPE*	DESCRIPTION
$D_0 - D_{17}$	Data Inputs	I	Data inputs from an 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is taken LOW, the FIFO's internal read and write pointers are set to address the first physical location of the RAM array; $\overline{FF}$ and $\overline{PAF}$ go HIGH; and $\overline{PAE}$ and $\overline{EF}$ go LOW. The offset registers and the Command Register are set to their default values. A reset is required before an initial write after power-up.
$\overline{EMODE}$	Enhanced Operating Mode	I	When $\overline{EMODE}$ is held LOW, Command Register bits 06-10 are forced HIGH rather than LOW, thus enabling all Enhanced Operating Mode features. (See Table 5.) If this behavior is always desired, $\overline{EMODE}$ may be grounded. Alternatively, $\overline{EMODE}$ may be tied to V_{CC}, so that the FIFO is functionally IDT-compatible.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ (Write Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a resource register rather than the internal FIFO memory is written into.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO internal memory continues to hold the previous data. (See Table 3.) Data will not be written into the FIFO if $\overline{FF}$ is LOW. In the optional Enhanced Operating Mode, WEN_2 may be combined with $\overline{WEN}$ to produce an effective internal write-enable signal.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK whenever $\overline{REN}$ (Read Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a resource register rather than the internal FIFO memory is read from.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the FIFO's output register continues to hold the previous data word, whether or not $Q_0 - Q_{17}$ (the data outputs) are enabled. (See Table 3.) In the optional Enhanced Operating Mode, REN_2 may be combined with $\overline{REN}$ to produce an effective internal read-enable signal.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in high-Z (high-impedance) state. In the optional Enhanced Operating Mode, $\overline{OE}$ not only continues to control the outputs in this same manner, but also may be configured to function as an additional input to the combined effective read-enable signal, along with $\overline{REN}$ and perhaps also with REN_2. (See Table 5.)
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, the data word on $D_0 - D_{17}$ (the data inputs) is written to the offset and command registers on the LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ is LOW. (See Table 3.) Also, when $\overline{LD}$ is LOW, a word is read to $Q_0 - Q_{17}$ (the data outputs) from the offset and/or command registers on the LOW-to-HIGH transition of RCLK, whenever $\overline{REN}$ is LOW. (See again Table 3.) When $\overline{LD}$ is HIGH, normal FIFO write and read operations are enabled.

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE *	DESCRIPTION
$\overline{FL}/RT$	First Load/ Retransmit	I	In the standalone or paralleled configuration, $\overline{FL}$ may be grounded. However, in the standalone or paralleled configuration, if $\overline{FL}$ is taken HIGH, it functions instead as RT (Retransmit), and resets the FIFO's internal read pointer to the first physical location of the RAM array. In the cascaded configuration, $\overline{FL}$ has an entirely different function; it is grounded for the first FIFO device (the 'master' device or 'first-load' device), and is set to HIGH for all other FIFO devices in the daisy chain.
$\overline{WXI}/WEN_2$	Write Expansion Input/ Write Enable 2	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the two other control inputs $\overline{RXI}/REN_2$ and $\overline{FL}/RT$. (See Tables 2 and 6.) In the standalone or paralleled configuration, $\overline{WXI}/WEN_2$ is grounded. In the cascaded configuration, $\overline{WXI}/WEN_2$ is connected to $\overline{WXO}$ (Write Expansion Output) of the previous device, and functions as $\overline{WXI}$. In the optional Enhanced Operating Mode, $\overline{WXI}/WEN_2$ functions as a second write-enable signal, WEN_2, which is combined with $\overline{WEN}$ to produce an effective internal write-enable signal.
$\overline{RXI}/REN_2$	Read Expansion Input/ Read Enable 2	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the two other control inputs $\overline{WXI}/WEN_2$ and $\overline{FL}/RT$. (See Tables 2 and 6.) In the standalone or paralleled configuration, $\overline{RXI}/REN_2$ is grounded. In the cascaded configuration, $\overline{RXI}/REN_2$ is connected to $\overline{RXO}$ (Read Expansion Output) of the previous device, and functions as $\overline{RXI}$. In the optional Enhanced Operating Mode, $\overline{RXI}/REN_2$ functions as a second read-enable signal, REN_2, which is combined with $\overline{REN}$ – and perhaps also with $\overline{OE}$, if Command-Register bit 10 is set – to produce an effective internal read-enable signal.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full; further advancement of its internal write-address pointer, and further data writes into its inputs, are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is 'almost full,' based on the almost-full offset programmed into the FIFO. The default value of this offset at reset is about 1/8 of the FIFO capacity, measured from 'full.' (See Table 4.) In Default Mode, $\overline{PAF}$ is asynchronous; in the optional Enhanced Operating Mode, $\overline{PAF}$ is synchronized to WCLK. (See Table 5.)
$\overline{WXO}/\overline{HF}$	Write Expansion Output/ Half-Full Flag	O	This signal is dual-purpose; its functionality is determined during a reset operation according to the states of the two control inputs $\overline{WXI}/WEN_2$ and $\overline{RXI}/REN_2$. (See Tables 2 and 6.) In the standalone or paralleled configuration, whenever $\overline{HF}$ is LOW the device is more than half full. In Default Mode, $\overline{HF}$ is asynchronous; in the optional Enhanced Operating Mode, $\overline{HF}$ may be synchronized either to WCLK or to RCLK. (See Table 5.) In the cascaded configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device whenever the last location in the FIFO is written.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is 'almost empty,' based on the almost-empty offset programmed into the FIFO. The default value of this offset at reset is about 1/8 of the FIFO capacity, measured from 'empty.' (See Table 4.) In Default Mode, $\overline{PAE}$ is asynchronous; in the optional Enhanced Operating Mode, $\overline{PAE}$ is synchronized to RCLK. (See Table 5.)

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE *	DESCRIPTION
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty; further advancement of its internal read-address pointer, and further changes in the data word present at its outputs, are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{RXO}$	Read Expansion Output	O	In the IDT-compatible cascaded configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next FIFO whenever the last location in the FIFO is read.
$Q_0 - Q_{17}$	Data Outputs	O/Z	Data outputs to drive an 18-bit bus.
V_{CC}	Power	V	Seven +5 V power-supply pins.
V_{SS}	Ground	V	Eight 0 V ground pins.

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

Table 1. Depth-Code Programming

DEPTH CODE d	TOTAL DEPTH	
	WITH LH540215s	WITH LH540225s
0	512	1024
1	512	1024
2	1024	2048
3	1536	3072
...	...	...
d	512d	1024d
...	...	...
31	15872	31744
32	16384	32768

Table 2. Grouping-Mode Determination During a Reset Operation

$\overline{EMODE}$	$\overline{WXI}/WEN_2$	$\overline{RXI}/REN_2$	$\overline{FL}/RT$	MODE	$\overline{WXO}/\overline{HF}$ USAGE	$\overline{WXI}/WEN_2$ USAGE	$\overline{RXI}/REN_2$ USAGE	$\overline{FL}/RT$ USAGE
H	H	H	H	Cascaded Slave [1]	$\overline{WXO}$	$\overline{WXI}$	RXI	$\overline{FL}$
H	H	H	L	Cascaded Master [1]	$\overline{WXO}$	$\overline{WXI}$	RXI	$\overline{FL}$
H	H	L	X	(Reserved)	($\overline{HF}$)	($\overline{WXI}$)	($\overline{RXI}$)	(RT)
H	L	H	X	(Reserved)	($\overline{WXO}$)	($\overline{WXI}$)	($\overline{RXI}$)	($\overline{FL}$)
H	L	L	H	Retransmit [2]	$\overline{HF}$	(none)	(none)	RT
H	L	L	L	Standalone	$\overline{HF}$	(none)	(none)	RT
L	X	X	X	Interlocked Paralleled	$\overline{HF}$	WEN_2	REN_2	RT

NOTES:

1. The terms 'master' and 'slave' refer to IDT-compatible cascading. In pipelined cascading, there is no such distinction.
2. Momentary only; basically standalone grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

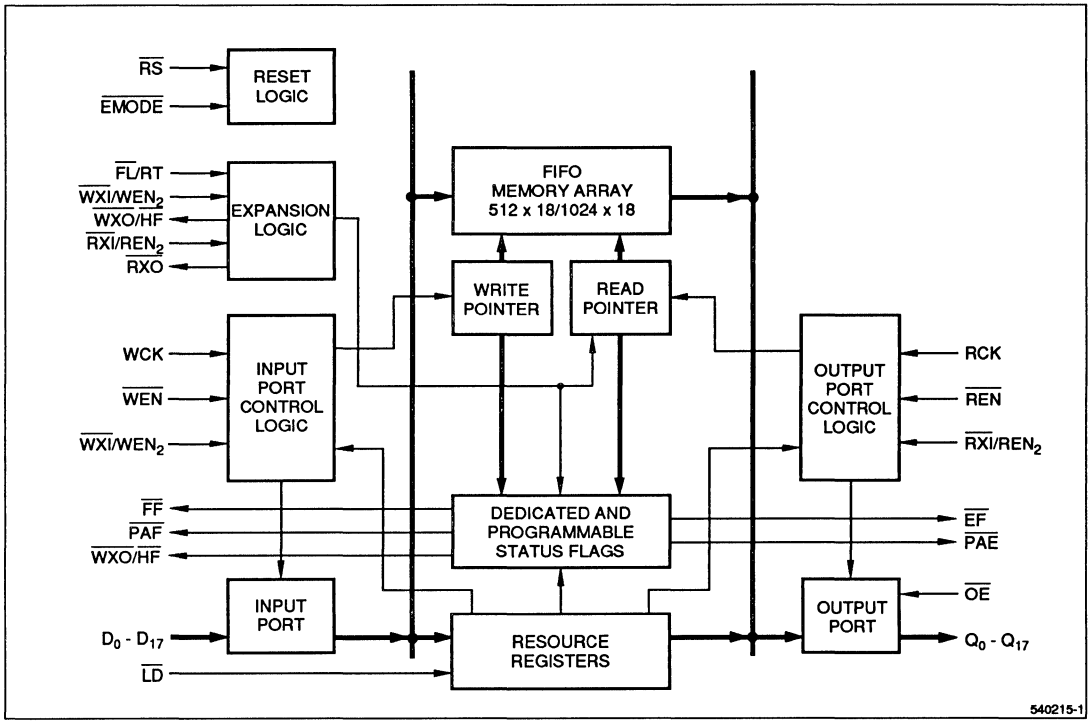


Figure 2. LH540215/25 Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential	−0.5 V to V_{CC} + 0.5 V
DC Output Current [1]	±75 mA
Temperature Range with Power Applied [2]	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 W (PLCC)

NOTES:
1. Only one output may be shorted at a time, for a period not exceeding 30 seconds.
2. Measured with clocks idle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−1	1	µA
I_{LO}	I/O Leakage	OE ≥ V_{IH}, 0 V ≤ V_{OUT} ≤ V_{CC}	−2	2	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −8.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16.0 mA		0.4	V
I_{CC}	Average Operating Supply Current	Measured at fc = max		250	mA
I_{CC2}	Average Standby Supply Current	All inputs = V_{IHMIN} (clock idle)		60	mA
I_{CC3}	Power-Down Supply Current	All inputs = V_{CC} − 0.2 V (clock idle)		1	mA

AC TEST CONDITIONS

PARAMETER		RATING
Input Pulse Levels		V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)		3 ns
Output Reference Levels		1.5 V
Input Timing Reference Levels		1.5 V
Output Load, Timing Tests	R_1 (Top Resistor)	1.1k Ohms
	R_2 (Bottom Resistor)	680 Ohms
	C_L (Load Capacitance)	30 pF

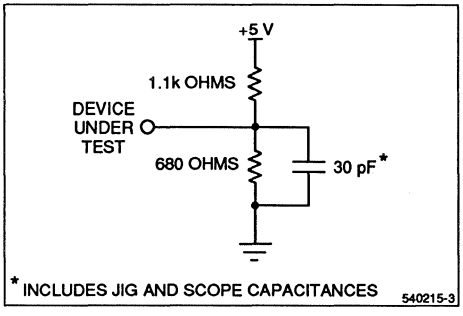


Figure 3. Output Load Circuit

CAPACITANCE

PARAMETER	RATING
C_{IN} (Input Capacitance) V_{IN} = 0 V	7 pF
C_O (Output Capacitance) V_{OUT} = 0 V	7 pF

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	-15		-20		-25		-50	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
f_S	Clock Cycle Frequency		67		50		40		20
t_A	Data Access Time	2	11	2	14	3	15	3	25
t_{CLK}	Clock Cycle Time	15		20		25		50	
t_{CLKH}	Clock HIGH Time	6		8		10		20	
t_{CLKL}	Clock LOW Time	7		9		10		20	
t_{DS}	Data Setup Time	4		5		6		10	
t_{DH}	Data Hold Time	1		1		1		2	
t_{ENS}	Enable Setup Time	4		5		6		10	
t_{ENH}	Enable Hold Time	1		1		1		2	
t_{RS}	Reset Pulse Width [1]	15		20		25		50	
t_{RSS}	Reset Setup Time [2]	9		12		15		30	
t_{RSF}	Reset to Flag and Output Time		15		20		25		50
t_{OLZ}	Output Enable to Output in Low-Z [2]	0		0		0		0	
t_{OE}	Output Enable to Output Valid		7		9		12		20
t_{OHZ}	Output Enable to Output in High-Z [2]	1	7	1	9	1	12	1	20
t_{WFF}	Write Clock to Full Flag		11		14		16		30
t_{REF}	Read Clock to Empty Flag		11		12		15		30
t_{PAF}	Clock to Programmable Almost-Full Flag (Default Mode)		15		20		22		35
t_{PAE}	Clock to Programmable Almost-Empty Flag (Default Mode)		15		20		22		35
t_{HF}	Clock to Half-Full Flag (Default Mode)		15		20		22		35
t_{PAFS}	Clock to Programmable Almost-Full Flag (Enhanced Mode)		11		12		15		30
t_{PAES}	Clock to Programmable Almost-Empty Flag (Enhanced Mode)		11		12		15		30
t_{HFS}	Clock to Half-Full Flag (Enhanced Mode)		11		12		15		30
t_{XO}	Clock to Expansion-Out		9		12		15		30
t_{XI}	Expansion-In Pulse Width	6		8		10		20	
t_{XIS}	Expansion-In Setup Time	6		8		10		20	
t_{SKEW1}	Skew Time Between Read Clock and Write Clock for Full Flag	11		14		16		20	
t_{SKEW2}	Skew Time Between Read Clock and Write Clock for Empty Flag	11		14		16		20	

NOTES:

1. Pulse widths less than the stated minimum values may cause incorrect operation.
2. Values are guaranteed by design; not currently tested.

Table 3. Selection of Read and Write Operations

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	WCLK	RCLK	ACTION
L	X	X	–	–	No operation.
L	L	H	∧	–	Write to a resource register. [1]
L	H	H	∧	–	Increment resource-register write counter, but do not write. [2]
L	H	L	–	∧	Read from a resource register. [1]
L	H	H	–	∧	Increment resource-register read counter, but do not read. [2]
L	X	X	∧	∧	Illegal combination, which will cause errors.
H	L	X	∧	X	Normal FIFO write operation.
H	X	L	X	∧	Normal FIFO read operation.
H	L	X	–	X	No write operation.
H	H	X	X	X	No write operation.
H	X	L	X	–	No read operation.
H	X	H	X	X	No read operation.
H	L	L	–	–	No operation.
H	H	H	X	X	No operation.

KEY:

H = Logic 'HIGH'; L = Logic 'LOW'; X = 'Don't-care' (logic 'HIGH,' logic 'LOW,' or any transition);
∧ = A 'LOW'-to-'HIGH' transition; – = Any condition EXCEPT a 'LOW'-to-'HIGH' transition.

NOTES:

1. The selection of a resource register to be written or read is controlled by two simple state machines. One state machine controls the selection for writing; the other state machine controls the selection for reading. These two state machines operate independently of each other. Both state machines are reset to point to Word 0 by a reset operation.
2. The order of the three resource registers, as selected by either state machine, is always:
   Word 0: Almost-Empty Offset Register
   Word 1: Almost-Full Offset Register
   Word 2: Command Register
   Word 0: Almost-Empty Offset Register
   ...
   (repeats indefinitely)
   ...

Table 4. Status Flags

NUMBER OF DATA WORDS PRESENT WITHIN FIFO [1, 2]		$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
512 × 18 FIFO	1024 × 18 FIFO					
0	0	H	H	H	L	L
1 to n	1 to n	H	H	H	L	H
(n + 1) to 256	(n + 1) to 512	H	H	H	H	H
257 to (512 – (m + 1))	513 to (1024 – (m + 1))	H	H	L	H	H
(512 – m) to 511	(1024 – m) to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

NOTES:

1. n = Programmable-Almost-Empty Offset. (Default values: 512 × 18, n = 63; 1024 × 18, n = 127.)
2. m = Programmable-Almost-Full Offset. (Default values: 512 × 18, m = 63; 1024 × 18, m = 127.)

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES

Data Inputs

DATA IN ($D_0 - D_{17}$)

Data, programmable-flag-offset values, and Command-Register codes are input to the FIFO as 18-bit words on $D_0 - D_{17}$. Unused bit positions in offset and Command-Register words should be zero-filled.

Control Inputs

RESET ($\overline{RS}$)

The FIFO is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken to a LOW state. A reset operation is required after power-up, before the first write operation may occur. The state of the FIFO is fully defined after a reset operation. If the default values which are entered into the Programmable-Flag-Offset-Value Registers and the Command Register by a reset operation are acceptable, then no device programming is required. A reset operation initializes the FIFO's internal read-address and write-address pointers to the FIFO's first physical memory location. The five status flags, $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$, are updated to indicate that the FIFO is completely empty; thus, the first three of these are reset to HIGH, and the last two are reset to LOW. The flag-offset values for $\overline{PAF}$ and $\overline{PAE}$ each are initialized to about 1/8 of the depth of a single FIFO; 63 for a 512-word FIFO, and 127 for a 1024-word FIFO. The Command Register is initialized to configure the FIFO to operate in the 100% IDT72215A/25A-compatible Default Operating Mode. The Depth Code is initialized to LLLLLH (01_{10}).

ENHANCED OPERATING MODE ($\overline{EMODE}$)

Whenever $\overline{EMODE}$ is being asserted, Command Register bits 06-11 remain HIGH rather than LOW after the completion of the reset operation. Thus, $\overline{EMODE}$ has the effect of activating optional Enhanced Operating Mode features, without the need to configure the Command Register by the normal programming method. The behavior of these optional features is described in Table 5. For permanent Enhanced Operating Mode operation, $\overline{EMODE}$ must be grounded.

WRITE CLOCK (WCLK)

A rising edge (LOW-to-HIGH transition) of WCLK initiates a FIFO write cycle if $\overline{LD}$ is HIGH, or a resource-register write cycle if $\overline{LD}$ is LOW. The 18 data inputs, and all input-side synchronous control inputs, must meet setup and hold times with respect to the rising edge of WCLK. The input-side status flags are meaningful after specified time intervals, following a rising edge of WCLK.

Conceptually, WCLK receives a free-running, periodic 'clock' waveform, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the WCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{WEN}$ is continuously asserted (that is, is continuously held LOW), and WCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that WCLK must have any particular relation to the read clock RCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

WRITE ENABLE ($\overline{WEN}$)

Whenever $\overline{WEN}$ is being asserted (is LOW) and $\overline{LD}$ is HIGH, and the FIFO is not full, an 18-bit data word is loaded into the input register for the memory array at every WCLK rising edge (LOW-to-HIGH transition). Data words are stored into the two-port memory array sequentially, regardless of any ongoing read operation. Whenever $\overline{WEN}$ is not being asserted (is HIGH), the input register retains whatever data word it contained previously, and no new data word gets loaded into the memory array.

To prevent overrunning the internal FIFO boundaries, further write operations are inhibited whenever the Full Flag ($\overline{FF}$) is being asserted (is LOW). If a valid read operation then occurs, upon the completion of that read cycle $\overline{FF}$ again goes HIGH after a time t_{WFF}, and another write operation is allowed to begin whenever WCLK makes another LOW-to-HIGH transition. Effectively, $\overline{WEN}$ is overridden by $\overline{FF}$; thus, $\overline{WEN}$ has no effect when the FIFO is full.

In the optional Enhanced Operating Mode, if $\overline{EMODE}$ is being asserted (is LOW), $\overline{WXI}/WEN_2$ functions as WEN_2, an additional duplicate (albeit assertive-HIGH) write-enable input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs. To control writing, WEN_2 is combined with $\overline{WEN}$; the logic-AND function of $\overline{WEN}$ and WEN_2 then behaves like $\overline{WEN}$ in the foregoing description.

READ CLOCK (RCLK)

A rising edge (LOW-to-HIGH transition) of RCLK initiates a FIFO read cycle if $\overline{LD}$ is HIGH, or a resource-register read cycle if $\overline{LD}$ is LOW. All output-side synchronous control inputs must meet setup and hold times with respect to the rising edge of RCLK. The 18 data outputs, and the output-side status flags, are meaningful after specified time intervals, following a rising edge of RCLK.

Conceptually, RCLK receives a free-running, periodic 'clock' waveform, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the RCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{REN}$ is continuously asserted (that is, is continuously held LOW), and RCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

requirement that RCLK must have any particular relation to the write clock WCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

READ ENABLE ($\overline{REN}$)

Whenever $\overline{REN}$ is being asserted (is LOW), and the FIFO is not full, an 18-bit data word is loaded into the output register from the memory array at every RCLK rising edge (LOW-to-HIGH transition). Data words are read from the two-port memory array sequentially, regardless of any ongoing write operation. Whenever $\overline{REN}$ is not being asserted (is HIGH), the output register retains whatever data word it contained previously, and no new data word gets loaded into it from the memory array.

To prevent underrunning the internal FIFO boundaries, further read operations are inhibited whenever the Empty Flag ($\overline{EF}$) is being asserted (is LOW). If a valid write operation then occurs, upon the completion of that write cycle $\overline{EF}$ again goes HIGH after a time t_{REF}, and another read operation is allowed to begin whenever RCLK makes another LOW-to-HIGH transition. Effectively, $\overline{REN}$ is overridden by $\overline{EF}$; thus, $\overline{REN}$ has no effect when the FIFO is empty.

In the optional Enhanced Operating Mode, one or two additional read enable inputs may be combined with $\overline{REN}$ to control reading; the logic-AND function of these two or three inputs then behaves like $\overline{REN}$ in the foregoing description. If $\overline{EMODE}$ is being asserted (is LOW), $\overline{RXI}/REN_2$ functions as REN_2, an additional duplicate (albeit assertive-HIGH) $\overline{REN}$ input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs.

Also, if Command Register bit 10 has been set, $\overline{OE}$ takes on the extra role of serving as yet another duplicate $\overline{REN}$ input, in addition to its usual function of controlling the FIFO's data outputs, in order to inhibit further read operations whenever the FIFO's data outputs are disabled.

OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is an assertive-LOW, asynchronous, output enable. In the Default Operating Mode, $\overline{OE}$ has only the effect of enabling or disabling the data outputs $Q_0 - Q_{17}$. That is, disabling $Q_0 - Q_{17}$ does not inhibit a read operation, for data being transmitted to the output register; the data will remain available later, when the outputs are again enabled, unless subsequently overwritten. When $Q_0 - Q_{17}$ are enabled, each of these 18 data outputs is in a normal HIGH or LOW state, according to the bit pattern of the data word in the output register. When $Q_0 - Q_{17}$ are disabled, each of these outputs is in the high-Z (high-impedance) state.

In the optional Enhanced Operating Mode, if Command Register bit 10 has been set, $\overline{OE}$ behaves as an additional read enable, as well as enabling and disabling the data outputs $Q_0 - Q_{17}$. Under these circumstances, incrementing the read-address pointer is inhibited whenever $Q_0 - Q_{17}$ are in the high-Z state. Thus, 'reading' successive words which fail to reach the outputs is prevented, as a safeguard against data loss.

LOAD ($\overline{LD}$)

The Sharp LH540215/25 FIFOs contain three 18-bit resource registers. The contents of these three registers may be loaded with data from the data inputs $D_0 - D_{17}$, or read out on the data outputs $Q_0 - Q_{17}$. The first two registers are the Programmable-Flag-Offset-Value Registers, for the Programmable Almost-Empty Flag ($\overline{PAE}$) and the Programmable Almost-Full Flag ($\overline{PAF}$) respectively. The third register is the Command Register, which includes the 6-bit IDT72215A/25A 'Depth Code' field, along with several configuration-control bits for Sharp's optional Enhanced-Operating-Mode features.

None of these three registers makes use of all of its available 18 bits. Figure 4 shows which bit positions of each register are operational. The two Programmable-Flag-Offset-Value Registers each contain the offset value in bits 0-15; bits 16-17 are unused. The Command Register configuration is shown in Table 5. For the Command Register, the default value for any operational bit which has not been programmed is zero (LOW); except, that the default value of the Depth Code is LLLLLH (01_{10}), in conformity with IDT's usage. The default values for both offsets are about 1/8 of the total number of words in the FIFO: 63 for a 512 × 18 FIFO, and 127 for a 1024 × 18 FIFO.

Whenever $\overline{LD}$ and $\overline{WEN}$ are simultaneously being asserted (are both LOW) the 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Empty-Flag-Offset-Value Register at the first rising edge (LOW-to-HIGH transition) of the write clock (WCLK). (See Table 3.) If $\overline{LD}$ and $\overline{WEN}$ continue to be simultaneously asserted, another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Full-Flag-Offset-Value Register at the second rising edge of WCLK, and still another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Command Register at the third rising edge of WCLK. At the fourth rising edge of WCLK, writing again occurs to the Programmable-Empty-Flag-Offset-Value Register; and the writing sequence gets repeated on subsequent WCLK rising edges.

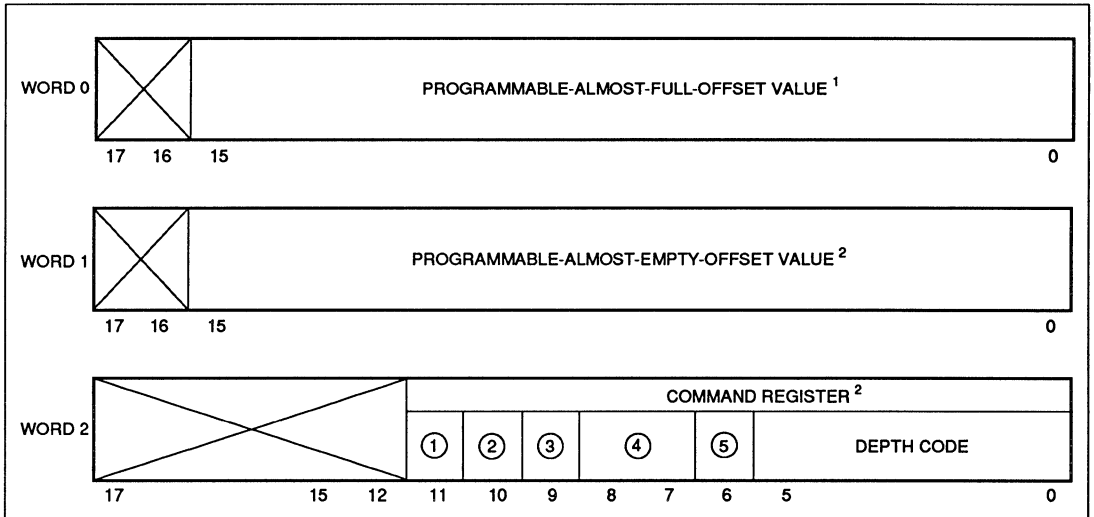
DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

The lower 9 bits of these data words are made use of by the 512-word LH540215, and the lower 10 bits by the 1024-word LH540225. 10 bits are used for the Command Register, by both the LH540215 and the LH540225. There is no restriction on the values which may occur in these data fields; however, unused bit positions should be encoded LOW in order to maintain forward compatibility.

Writing contents to these three resource registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{WEN}$ is not being asserted (is HIGH), the FIFO's internal resource-register-write-address pointer advances without any writing actually taking place. Thus, for instance, one or two resource registers may be written, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).

Likewise, whenever $\overline{LD}$ and $\overline{REN}$ are simultaneously being asserted (are both LOW) the 18-bit data word from the Programmable-Empty-Flag-Offset-Value Register is read to the data outputs $Q_0 - Q_{17}$ at the first rising edge (LOW-to-HIGH transition) of the read clock (RCLK). (See Table 3.) If $\overline{LD}$ and $\overline{REN}$ continue to be simultaneously asserted, another 18-bit data word from the Programmable-Full-Flag-Offset-Value Register is read to the data outputs $Q_0 - Q_{17}$ at the second rising edge of RCLK, and still another 18-bit data word from the Command Register is read to the data outputs $Q_0 - Q_{17}$ at the third rising edge of RCLK. At the fourth rising edge of RCLK, reading again occurs from the Programmable-Empty-Flag-Offset-Value Register; and the reading sequence gets repeated on subsequent RCLK rising edges.

Reading contents from these three resource registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{REN}$ is not being asserted (is HIGH), the FIFO's internal resource-register-read-address pointer advances without any reading actually taking place. Thus, for instance, one or two resource registers may be read, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).



(1) Reserved. Enables a special test mode, for manufacturers use only; disables normal operating mode.
(2) Enables suppressing reading whenever data outputs are disabled.
(3) Makes $\overline{PAF}$ synchronous.
(4) Makes $\overline{HF}$ synchronous.
(5) Makes $\overline{PAE}$ synchronous.

NOTES:
1. Default offset values are 63_{10} (LH540215) or 127_{10} (LH540225).
   See 'Command-Register Format' table for the default state of the command register.
2. The assertion of EMODE forces Command Register bits 06-11 HIGH.

540215-4

Figure 4. Resource Registers

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

To ensure correct operation, rising edges of WCLK and RCLK should not both be occuring at the same time while $\overline{LD}$ is being asserted.

FIRST LOAD/RETRANSMIT ($\overline{FL}$/RT)

$\overline{FL}$/RT is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2. There are four possible grouping modes: standalone, interlocked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 2 and 6 show the signal encodings which select each grouping mode.

In standalone or paralleled operation, the $\overline{FL}$/RT pin should be grounded for strict IDT72215A/25A-compatible operation. However, if it is taken HIGH, the FIFO's internal read-address pointer is reset to address the FIFO'S first physical memory location, without any other reset actions being taken; in particular, the FIFO's internal write-address pointer is unaffected. Subsequent read operations may then again read out the same block of data, delimited by the FIFO's first physical memory location and the current value of the write pointer, as was read out previously. There is no limit on the number of times that a block of data may be retransmitted. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' and address the FIFO's first physical memory location a second time during the retransmission process, and that the retransmit facility is unavailable during IDT-compatible cascaded operation.

In IDT-compatible cascaded operation, $\overline{FL}$/RT is grounded to distinguish the 'master' or 'first-load' FIFO from the other 'slave' FIFOs in the cascade, which must all have their $\overline{FL}$/RT inputs HIGH during a reset operation. (See again Tables 2 and 6.) The cascade will not operate correctly either without any 'master' FIFO, or with more than one 'master' FIFO.

WRITE EXPANSION INPUT/WRITE ENABLE 2 ($\overline{WXI}$/WEN_2)

$\overline{WXI}$/WEN_2 is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{FL}$/RT and $\overline{RXI}$. There are four possible grouping modes: standalone, interlocked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 2 and 6 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2 both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. In interlocked paralleled operation, $\overline{WXI}$/WEN_2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN_2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.

In cascaded operation, $\overline{WXI}$/WEN_2 is connected to the $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/$\overline{HF}$) output of the previous FIFO in the cascade. $\overline{RXI}$/REN_2 is likewise connected to the $\overline{RXO}$ (Read Expansion Output) output of that previous FIFO. A reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2 inputs thus connected come up in one of the two cascaded grouping modes, according to whether their $\overline{FL}$/RT inputs are grounded or tied HIGH. (See again Tables 2 and 6.)

READ EXPANSION INPUT/READ ENABLE 2 ($\overline{RXI}$/REN_2)

$\overline{RXI}$/REN_2 is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{FL}$/RT and $\overline{WXI}$. There are four possible grouping modes: standalone, interlocked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 2 and 6 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2 both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. In interlocked paralleled operation, $\overline{WXI}$/WEN_2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN_2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.

In cascaded operation, $\overline{RXI}$/REN_2 is connected to the $\overline{RXO}$ (Read Expansion Output) of the previous FIFO in the cascade. $\overline{WXI}$/WEN_2 is likewise connected to the $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/HF) output of that previous FIFO. A reset operation forces $\overline{RXO}$ and $\overline{WXO}$/$\overline{HF}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{RXI}$/REN_2 and $\overline{WXI}$/WEN_2 inputs thus connected come up in one of the two IDT-compatible cascaded grouping modes, according to whether their $\overline{FL}$/RT inputs are grounded or tied HIGH. (See again Tables 2 and 6.)

Data Outputs

DATA OUT ($Q_0 - Q_{17}$)

Data, programmable-flag-offset values, and Command-Register codes are output from the FIFO as 18-bit words on $Q_0 - Q_{17}$. Unused bit positions in offset and Command-Register words are zero-filled.

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Table 5. Command-Register Format

COMMAND REGISTER BITS	CODE	VALUE AFTER RESET	FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
00-05	XXXXXX	LLLLLH	–	Depth code, from 00_{10} to 32_{10}.	Same functionality as in IDT72215A/25A.
06	L	L/H [2]	$\overline{PAE}$	Set by ↑RCLK, reset by ↑WCLK.	Asynchronous flag clocking.
	H			Set and reset by ↑RCLK.	Synchronous flag clocking.
07-08	LL	LL/HH [2]	$\overline{HF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	LH			Set and reset by ↑RCLK.	Synchronous flag clocking at output port.
	HL			Set and reset by ↑WCLK.	Synchronous flag clocking at input port.
	HH				
09	L	L/H [2]	$\overline{PAF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	H			Set and reset by ↑WCLK.	Synchronous flag clocking.
10	L	L/H [2]	–	$\overline{OE}$ has no effect on a read operation.	Allows the read-address pointer to advance even when $Q_0 - Q_{17}$ are not driving the output bus.
	H			$\overline{OE}$ inhibits a read operation whenever the data outputs $Q_0 - Q_{17}$ are in the high-Z state.	Inhibits the read-address pointer from advancing when $Q_0 - Q_{17}$ are not driving the output bus; thus, guards against data loss.
11	L	L	–	Normal operating mode.	For all in-system applications.
	H			Special test mode.	Reserved for testing purposes.

NOTES:

1. When Command Register bits 06-11 are LOW, the FIFO behaves in a manner functionally equivalent to the IDT72215A/25A FIFO of similar depth and speed grade.
2. If $\overline{EMODE}$ is not asserted (is HIGH), Command Register bits 06-10 remain LOW. However, if $\overline{EMODE}$ is asserted (is LOW), Command Register bits 06-10 are forced HIGH, and remain HIGH until changed. Command Register bits 00-05 and 11 are unaffected by $\overline{EMODE}$.

Table 6. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	INTERLOCKED PARALLELED	MASTER	SLAVE
I	$\overline{WXI}$/WEN_2	Grounded	From $\overline{FF}$ (other FIFO)	From $\overline{WXO}$ (n-1st FIFO)	From $\overline{WXO}$ (n-1st FIFO)
O	$\overline{WXO}$/$\overline{HF}$	Becomes $\overline{HF}$	Becomes $\overline{HF}$	To $\overline{WXI}$ (n+1st FIFO)	To $\overline{WXI}$ (n+1st FIFO)
I	$\overline{RXI}$/REN_2	Grounded	From $\overline{EF}$ (other FIFO)	From $\overline{RXO}$ (n-1st FIFO)	From $\overline{RXO}$ (n-1st FIFO)
O	$\overline{RXO}$	Unused	Unused	To $\overline{RXI}$ (n+1st FIFO)	To $\overline{RXI}$ (n+1st FIFO)
I	$\overline{FL}$/RT	Becomes RT	Becomes RT	Grounded (Logic LOW)	Logic HIGH

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Control/Status Outputs

FULL FLAG ($\overline{FF}$)

$\overline{FF}$ goes LOW whenever the FIFO is completely full; that is, whenever the FIFO's internal write pointer has completely caught up with its internal read pointer, so that if another word were to be written it would have to overwrite the unread word now in position for reading out by the next requested read operation. Under these conditions, the FIFO is filled to its nominal capacity, which is 512 18-bit words for the LH540215 or 1024 18-bit words for the LH540225 respectively. Write operations are inhibited whenever $\overline{FF}$ is LOW, regardless of the assertion or deassertion of Write Enable ($\overline{WEN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), $\overline{FF}$ initially is HIGH. But, whenever no read operations have been performed since the completion of the reset operation, $\overline{FF}$ goes LOW after 512 write operations for the LH540215, or after 1024 write operations for the LH540225. (See Table 4.)

$\overline{FF}$ gets updated after a LOW-to-HIGH transition of the Write Clock (WCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

$\overline{PAF}$ goes LOW whenever the FIFO is 'almost' full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than the value of the Programmable-Almost-Full-Flag Offset 'm.' The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of 'm' after the completion of a reset operation is about 1/8 of this total nominal number of words: 63 for the LH540215 or 127 for the LH540225 respectively. However, 'm' may be set to any value which does not exceed this total nominal number of words, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no read operations have been performed since the completion of the reset operation, $\overline{PAF}$ goes LOW after (512-m) write operations for the LH540215, or after (1024-m) write operations for the LH540225. (See Table 4.)

If m is still at its default value, $\overline{PAF}$ is LOW whenever the FIFO is from 7/8 full to completely full.

In the IDT-compatible Default Operating Mode, $\overline{PAF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{PAF}$ behaves as an 'asynchronous flag.'

In the optional Enhanced Operating Mode, on the other hand, $\overline{PAF}$ gets updated only after a LOW-to-HIGH transition of the Write Clock WCLK, and thus behaves as a 'synchronous flag.' (See Table 5.) This behavior may be selected by setting Command Register bit 09.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

$\overline{WXO}/\overline{HF}$ is a dual-purpose signal. In 'standalone' operation, it behaves as a Half-Full Flag ($\overline{HF}$), in accordance with Table 4. In IDT-compatible 'cascaded' operation, it behaves as a Write Expansion Output ($\overline{WXO}$) signal to coordinate writing operations with the next FIFO in the cascade. Under these same conditions, also, the dual-purpose $\overline{WXI}/WEN_2$ and $\overline{RXI}/REN_2$ inputs behave as Write Expansion Input ($\overline{WXI}$) and Read Expansion Input ($\overline{RXI}$) signals respectively.

When two or more LH540215 or LH540225 FIFOs are 'cascaded' to operate as a larger 'effective FIFO,' in a 'daisy-chain' ring configuration, the Write Expansion Input ($\overline{WXI}$) of each FIFO is connected to $\overline{WXO}$ of the previous FIFO in the ring, with $\overline{WXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{WXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{WXO}$-to-$\overline{WXI}$ connections, for Read Expansion Input ($\overline{RXI}$) and Read Expansion Output ($\overline{RXO}$).

When the last physical location has been written in a FIFO operating in cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{WXO}$ output; otherwise, $\overline{WXO}$ remains constantly HIGH whenever the FIFO is operating in cascaded mode. This LOW-going $\overline{WXO}$ pulse serves as a 'token' in the 'token-passing' FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{WXI}$ input. When this next FIFO receives the token, it is activated for writing.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{WXO}$ has no necessary function for FIFOs operating in the 'standalone' mode. Consequently, in that mode, the same output pin is used for $\overline{HF}$; it follows that $\overline{HF}$ is not available as an output from any FIFO which is operating in the IDT-compatible cascaded mode. A FIFO is initialized into 'cascaded master' mode, into 'cascaded slave' mode, into interlocked paralleled mode, or into standalone mode according to the

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

state of its $\overline{WXI}/WEN_2$, $\overline{RXI}/REN_2$, and $\overline{FL}/RT$ control inputs during a reset operation, and of Command Register bit 11. (See Table 2, Table 5, and Table 6.)

In standalone or interlocked paralleled operation, $\overline{HF}$ goes LOW whenever the FIFO is more than half full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than half of the total nominal number of 18-bit words in the FIFO's physical memory, which is 256 for the LH540215 or 512 for the LH540225 respectively. (See Table 4.) The subtraction is performed using modular arithmetic, modulo this total nominal number of words, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and it is operating in standalone or interlocked paralleled mode, and no read operations have been performed since the completion of the reset operation, $\overline{HF}$ goes LOW after 257 write operations for the LH540215, or after 513 write operations for the LH540225. (See again Table 4.)

In the IDT-compatible Default Operating Mode, $\overline{HF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{HF}$ behaves as an 'asynchronous flag.'

In the optional Enhanced Operating Mode, on the other hand, $\overline{HF}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, or else after a LOW-to-HIGH transition of the Write Clock WCLK, according to the setting of bits 07 and 08 of the Command Register. (See Table 5.) Thus, in this mode $\overline{HF}$ behaves as a 'synchronous flag,' and may be synchronized *either* to the input side or to the output side of the FIFO.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

$\overline{PAE}$ goes LOW whenever the FIFO is 'almost empty'; that is, whenever subtracting the value of the FIFO's internal write pointer from the value of its internal read pointer yields a difference which is less than n + 1, where 'n' is the value of the Programmable-Almost-Empty-Flag Offset. The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of n after the completion of a reset operation is about 1/8 of this total nominal number of words, 63 for the LH540215 or 127 for the LH540225 respectively. However, n may be set to any value which does not exceed this total nominal number of words, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{PAE}$ is LOW. (See Table 4.)

If n is still at its default value, $\overline{PAE}$ is LOW whenever the FIFO is from 1/8 full to completely empty.

In the IDT-compatible Default Operating Mode, $\overline{PAE}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Read Clock RCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Write Clock WCLK. Thus, in this operating mode, $\overline{PAE}$ behaves as an 'asynchronous flag.'

In the optional Enhanced Operating Mode, on the other hand, $\overline{PAE}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, and thus behaves as a 'synchronous flag.' (See Table 5.) This behavior may be selected by setting Command Register bit 06.

EMPTY FLAG ($\overline{EF}$)

$\overline{EF}$ goes LOW whenever the FIFO is completely empty; that is, whenever the FIFO's internal read pointer has completely caught up with its internal write pointer, so that if another word were to be read out it would have to come from the physical memory location now in position to be written into by the next requested write operation. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the assertion or deassertion of $\overline{REN}$.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{EF}$ is LOW. (See Table 4.)

$\overline{EF}$ gets updated after a LOW-to-HIGH transition of the Read Clock RCLK.

READ EXPANSION OUT ($\overline{RXO}$)

When two or more LH540215 or LH540225 FIFOs are operating in IDT-compatible 'cascaded' mode as a larger 'effective FIFO,' the dual-purpose $\overline{RXI}/REN_2$ and $\overline{WXI}/WEN_2$ inputs behave as Read Expansion Input ($\overline{RXI}$) and Write Expansion Input ($\overline{WXI}$) signals respectively. The cascade of FIFO devices has a 'daisy-chain' ring configuration; the Read Expansion Input ($\overline{RXI}$) of each FIFO is connected to $\overline{RXO}$ of the previous FIFO in the ring, with $\overline{RXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{RXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{RXO}$-to-$\overline{RXI}$ connections, for Write Expansion Input ($\overline{WXI}$) and Write Expansion Output ($\overline{WXO}$).

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

When the last physical location has been read in a FIFO operating in cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{RXO}$ output; otherwise, $\overline{RXO}$ remains constantly HIGH. This LOW-going $\overline{RXO}$ pulse serves as a 'token' in the token-passing FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{RXI}$ input. When this next FIFO receives the token, it is activated for reading.

After a FIFO emits an $\overline{RXO}$ pulse, its data outputs go into high-Z state, regardless of the assertion or deassertion of its Output Enable ($\overline{OE}$) control input, until it again receives the token.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{RXO}$ has no necessary function for a FIFO which is operating in 'standalone' mode. Consequently, in that mode, $\overline{RXO}$ is never asserted, and remains constantly HIGH. A FIFO is initialized into 'standalone' mode, into 'cascaded master' mode, or into 'cascaded slave' mode according to the state of its $\overline{WXI}/WEN_2$, $\overline{RXI}/REN_2$, and $\overline{FL}/RT$ control inputs during a reset operation. It also may be forced into interlocked paralleled mode by $\overline{EMODE}$. (See Table 2, Table 5, and Table 6.)

LH543620

PRODUCT PREVIEW

1024 × 36 Synchronous FIFO

FEATURES

- Fast Cycle Times: 15/20/25/30 ns
- Selectable 36/18/9-Bit Word Width on *Both* Input Port and Output Port
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- Independently-Synchronized Operation of Input Port and Output Port
- Pinout Similar to LH5420 256 × 36 × 2 Bidirectional FIFO
- Control Inputs Sampled on Rising Clock Edge (Except $\overline{RS}$ and $\overline{AOE}$)
- Most Control Signals Assertive-LOW for Noise Immunity
- High-Drive Three-State Outputs
- Device Comes Up Into Known Default State at Reset; Programming is Allowed, but is not Required
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- All Five Status Flags are Completely Synchronous
- Duplicate Enables for Interlocked Paralleled FIFO Operation, for 72-Bit Data Width
- Both Edge-Sampled ($\overline{OE}$) and Asynchronous ($\overline{AOE}$) Output Enables
- Automatic Byte Parity Checking; Optional Byte Parity Generation
- TTL/CMOS-Compatible I/O
- IEEE1149.1-Compliant (JTAG) Boundary-Scan Test Logic
- Space-Saving PQFP and PGA Packages

FUNCTIONAL DESCRIPTION

The LH543620 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 1024 36-bit words. It can replace four or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Its architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth; but they are each initialized to a default offset of eight locations from the respective boundaries during a reset operation. If this default offset is satisfactory, no further programming is required.

Both the input port and the output port may be set, *independently*, to operate at three data-word widths: 36 bits, 18 bits, and 9 bits. This setting may be changed during system operation; however, the word-width-control signals must meet the usual setup-time and hold-time conditions for control inputs.

9-bit bytes passing through the FIFO are assumed to be making use of a parity bit, and parity is automatically passively checked. A flag indicates the results of this parity checking; if parity checking is not desired, the value of this flag may be ignored. When the FIFO is reset, the parity-checking logic is initialized to use odd data parity; but the FIFO may be programmed to use either even parity or odd parity during subsequent operations. Also, the FIFO may be programmed to actively generate, and *record*, a parity bit into the most-significant bit of each 9-bit byte of data passing through the internal memory array, overwriting the previous contents of those bits.

Coordinated operation of two paralleled LH543620 FIFOs, as one 1K × 72 FIFO, may be ensured by 'interlocked' crosscoupling of the $\overline{FF}$ and $\overline{EF}$ outputs from each FIFO to the assertive-HIGH enable inputs of the other one; $\overline{FF}$ to ENI_2, and $\overline{EF}$ to ENO_2, in *both* directions between two paralleled FIFOs.

Two separate input control signals are provided for enabling/disabling the 3-state outputs: $\overline{OE}$, which is synchronized to CKO, and is held in a flipflop within the LH543620 during use; and $\overline{AOE}$, which is entirely asynchronous. In any given application, whichever one of these signals is *not* in use normally must be *grounded*; *both* must be asserted to enable the 3-state outputs.

LH64270

CMOS 1M (270K × 4) Field Memory

FEATURES

- 276,480 × 4 bit configuration
  (270 lines × 1,024 bits)
- Applicable to 4 f_{SC} sampling field size
  (263 lines × 910 bits) for NTSC signal
- Selectable field size:
  Line count: 262, 262.5, 263, or 270
  Line length: 910 or 1,024
- $\overline{RCLR}$ and $\overline{WCLR}$ pins allow the memory to be used as a delay line of desired bit length (1 to 276,480 bits)
- Access time: 50 ns (MAX.)
- Cycle time: 60 ns (MIN.)
- Power supply: 5 V ± 10%
- Power consumption:
  Operating: 550 mW (MAX.)
  Standby: 110 mW (MAX.)
- TTL compatible I/O
  (Three state for DO_0 - DO_3)
- Package:
  28-pin, 400-mil SDIP

DESCRIPTION

The LH64270 is a field memory LSI organized as 276,480 words × 4 bits of dynamic RAM.

It performs consecutive read and write operation of NTSC signals at a 4 f_{SC} sampling rate to obtain one field of delayed data (as a result).

It is designed for use in personal computers as well as in IDTV systems.

PIN CONNECTIONS

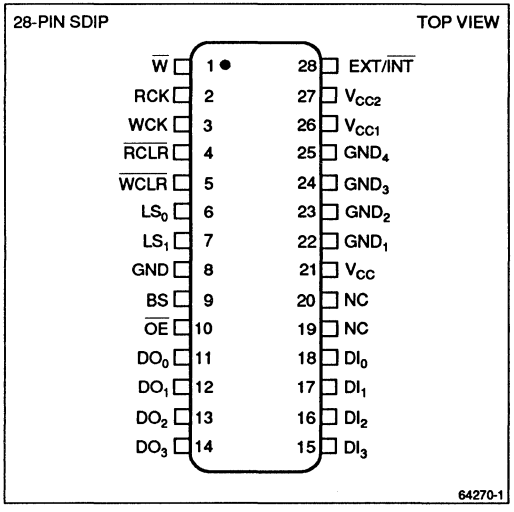


Figure 1. Pin Connections for SDIP Package

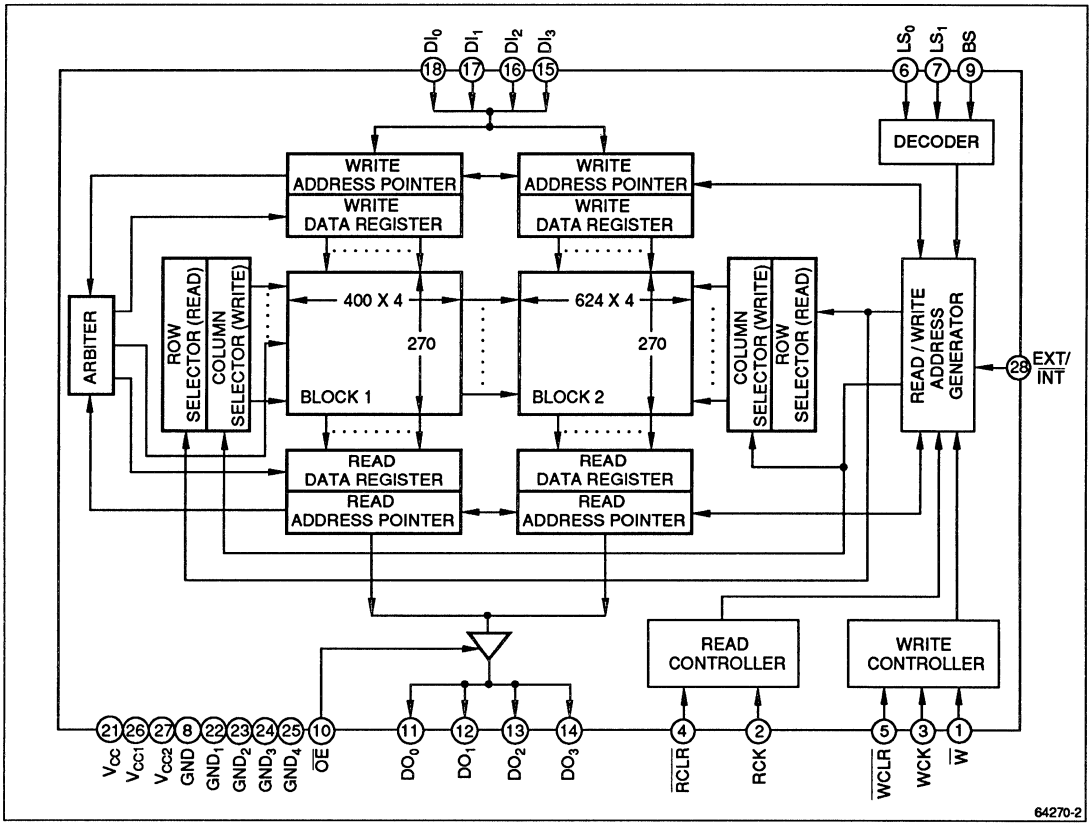


Figure 2. LH64270 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
WCK,RCK	Write/read clock input	
$\overline{W}$	Write control input	
$\overline{OE}$	Output enable input	
EXT/$\overline{INT}$	External/internal sync. select input	
$\overline{WCLR}$, $\overline{RCLR}$	Write/read address clear input	
DI_0 - DI_3	Write data input	

SIGNAL	PIN NAME	NOTE
DO_0 - DO_3	Read data output	
LS_0, LS_1	Line count select input	
BS	Bit count select input	
V_{CC}, V_{CC1}, V_{CC2}	+5 V power supply	1
GND, GND_1-GND_4	Ground	2
NC	Non connection	

NOTES:
1. Pins 21, 26 and 27 are not interconnected. These pins should all be connected to +5 V power.
2. Pins 8, 22, 23, 24 and 25 are not interconnected. These pins should all be connected to 0 V.

PIN FUNCTION

SIGNAL	PIN NAME	I/O	FUNCTION
DI_0 - DI_3	Data input	I	Write data input
DO_0 - DO_3	Data output	O	Read data output (Three state)
$\overline{WCLR}$	Write address pointer clear	I	Set the address of the next write cycle, after setting the $\overline{WCLR}$ signal at "LOW", to the beginning-of-field address (Address 0). The $\overline{WCLR}$ signal is detected only for one write cycle period after its falling edge.
$\overline{RCLR}$	Read address pointer clear	I	Set the address of the next read cycle, after setting the $\overline{RCLR}$ signal at "LOW", to the beginning-of-field address (Address 0). The $\overline{RCLR}$ signal is detected only for one read cycle period after its falling edge.
$\overline{W}$	Write control	I	The $\overline{W}$ signal controls data write operation. It also enables write operation of one field ($\overline{W}$ = "Low") or disables write operation of one field ($\overline{W}$ = "High") by synchronizing with the $\overline{WCLR}$ signal.
$\overline{OE}$	Output enable	I	The $\overline{OE}$ signal controls data read from data output pins. Its "Low" level enables data read on the data output pins, and its "High" level prohibits data read with setting the data output pins to high-impedance. Regardless of the $\overline{OE}$ signal's input level, the read address pointer continues to step up in response to the read clock (RCK).
WCK	Write clock	I	The WCK clock is a system clock input for data write. Write data is sampled by a rising edge of the WCK clock and transferred to an internal write data register. The write address pointer is stepped up by one address in each write clock cycle.
RCK	Read clock	I	The RCK clock is a system clock input for data read. Read data is output after the access time from the rising edge of the clock. The read address pointer is stepped up by one address in each read clock cycle. The RCK clock is required to be identical to the WCK clock.
LS_0, LS_1	Line selection	I	LS_0 and LS_1 signals determine the line number of one field. According to the combination of these signal input levels, one field can be 262 lines, 262.5 lines, 263 lines, or 270 lines. The line number can be determined for each field. [(LS_0, LS_1) ; (L, L) = 262 lines, (H, L) = 262.5 lines, (L, H) = 263 lines, (H, H) = 270 lines]
BS	Bit selection	I	The BS signal sets the line bit length to either 910 bits (BS = "Low") or 1024 bits (BS = "High"), which is selectable for each field.
EXT/$\overline{INT}$	Ext./Int. sync. selection	I	$\overline{INT}$ sync. mode: Setting this pin "LOW" invokes internal sync. mode. In this mode, the write address and read address are always coincident. Following a data write or a data read of the last bit of the last line of a field, the first clock input (WCK, RCK) starts a new access from the first bit of the first line of the next field. (Data input and output for one field is consecutively performed). The clear signals ($\overline{WCLR}$, $\overline{RCLR}$) must be kept at "HIGH" level in this mode. EXT sync. mode: Setting this pin "HIGH" invokes external sync. mode. In this mode, the write address and the read address can be independently controlled. The write address and the read address can be reset by the $\overline{WCLR}$ signal and the $\overline{RCLR}$ signal, respectively.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Pin voltage	V_T	-1.0 to +7.0	V
Supply voltage	V_{CC}	-1.0 to +7.0	V
Output current	I_O	50	mA
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input "High" voltage	V_{IH}	2.4		5.5	V
Input "Low" voltage	V_{IL}	-1.0		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Supply current	I_{CC1}	t_{WCS}, t_{RCS} = 60 ns		100	mA
Standby current	I_{CC2}	$\overline{W}$, $\overline{RCLR}$, $\overline{WCLR}$, $\overline{OE}$ = V_{IH} BS, RCK, WCK, LS_0, LS_1 = V_{IL} DI_0 - DI_3, EXT/$\overline{INT}$ = Don't care DO_0 - DO_3 = Open		20	mA
Input leakage current	I_I	0 V ≤ V_{IN} ≤ 5.5 V 0 V on all inputs except the pin under test	-10	10	µA
Output leakage current	I_O	0 V ≤ V_{OUT} ≤ 5.5 V DO_0 - DO_3 = High-impedance	-10	10	µA
Output "High" voltage	V_{OH}	I_{OUT} = -2 mA	2.4	—	V
Output "Low" voltage	V_{OL}	I_{OUT} = 4.0 mA	—	0.4	V

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
RCK cycle time	t_{RCS}	60	160	ns
WCK cycle time	t_{WCS}	60	160	ns
RCK "High" pulse width	t_{RCW}	20		ns
WCK "High" pulse width	t_{WCW}	20		ns
RCK "Low" pulse width	t_{RCP}	20		ns
WCK "Low" pulse width	t_{WCP}	20		ns
Input data setup to WCK	t_{IDS}	5		ns
Input data hold to WCK	t_{IDH}	5		ns
Access time from RCK	t_{RAC}		50	ns
Output data hold to RCK	t_{ROH}	5		ns
$\overline{OE}$ access time	t_{OEA}		30	ns
Output data hold time from $\overline{OE}$	t_{OEH}	0		ns
Output disable time from $\overline{OE}$	t_{OEZ}		40	ns
$\overline{W}$ setup time from WCK	t_{WWS}	5		ns
$\overline{W}$ hold time from WCK	t_{WWH}	0		ns
BS setup time from RCK, WCK	t_{BSS}	0		ns
BS hold time from RCK, WCK	t_{BSH}	15		ns
LS_0 - LS_1 setup time from RCK, WCK	t_{LSS}	0		ns
LS_0 - LS_1 hold time from RCK, WCK	t_{LSH}	15		ns
$\overline{RCLR}$, $\overline{WCLR}$ pulse width	t_{CLP}	30		ns
$\overline{RCLR}$, $\overline{WCLR}$ setup time from RCK, WCK	t_{CLS}	5		ns
$\overline{RCLR}$, $\overline{WCLR}$ hold time from RCK, WCK	t_{CLH}	5		ns
Input transition time (rise/fall)	t_T	3	35	ns

NOTE: At least 500 µs of pause time after power-on should be given, and then clocks (WCK and RCK) must be input more than 8,192 times to initialize dynamic circuits.

AC TEST CONDITIONS

PARAMETER	RATING
Input pulse level	0 to 3 V
Input rise/fall time	5 ns
Input timing reference level	1.5 V
Output timing reference level	0.8 V, 2 V

CAPACITANCE

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_I	All input pins		10	pF
Output capacitance	C_O	All output pins		10	pF

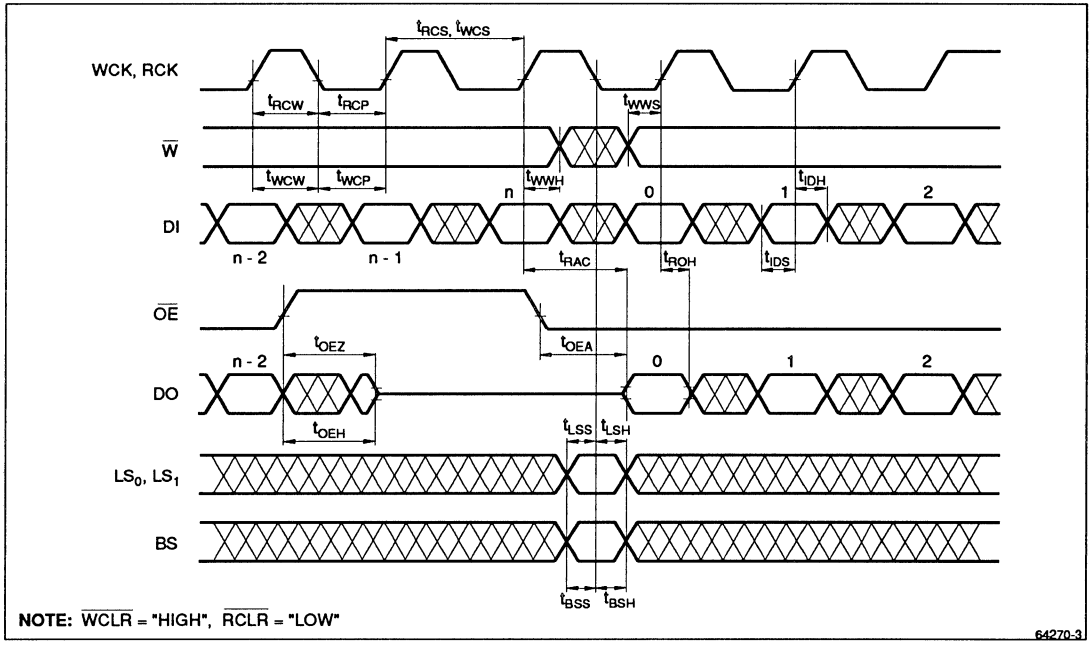


Figure 3. Internal Sync. Mode (EXT/$\overline{INT}$ - Low)

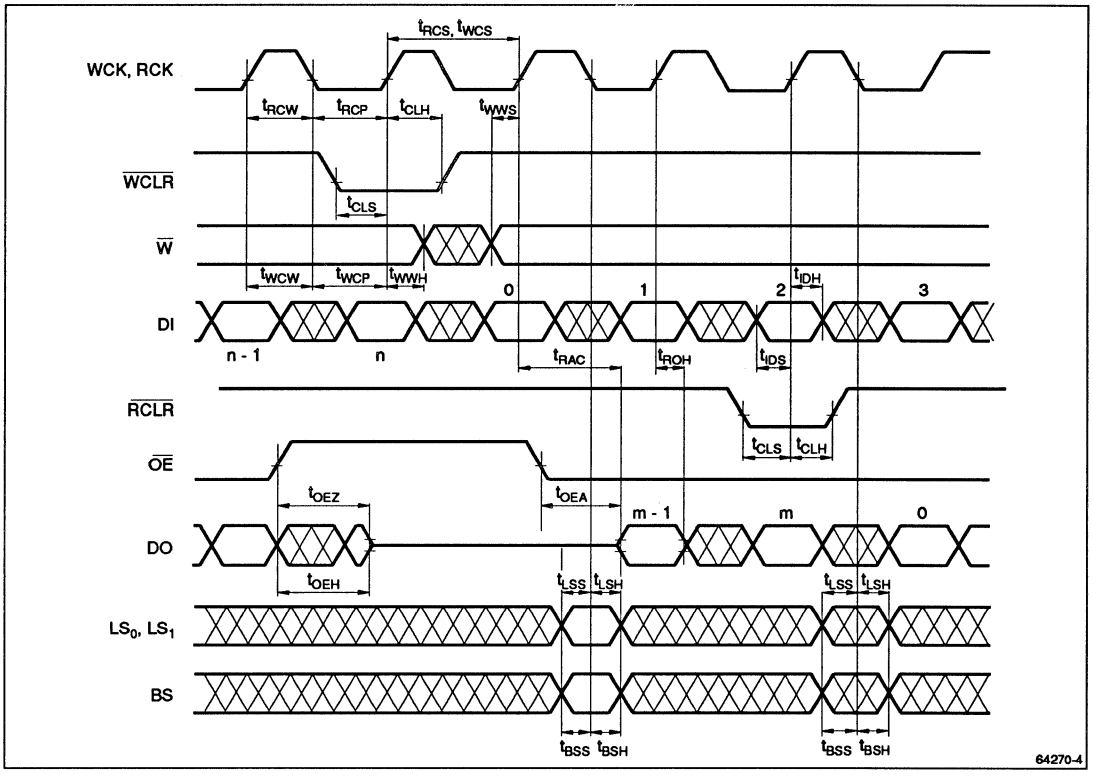
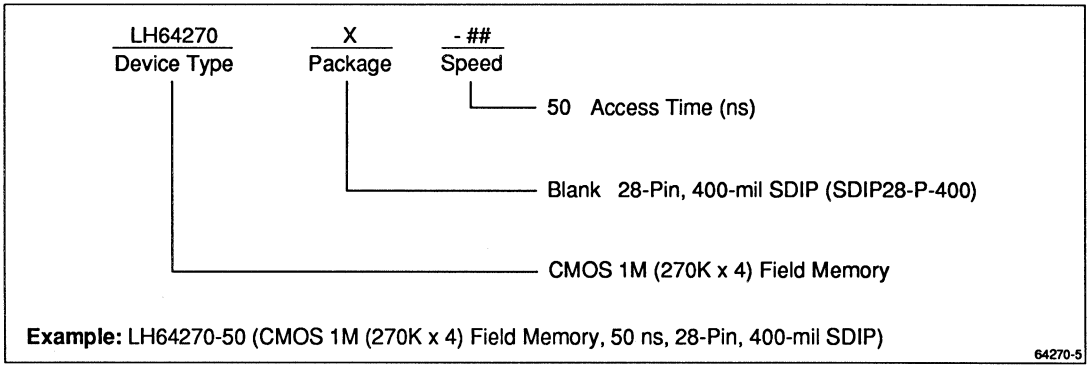


Figure 4. External Sync. Mode (EXT/$\overline{INT}$ - High)

ORDERING INFORMATION



LH66180

CMOS 1M (180K × 6) Field Memory for VCR

FEATURES

- Dynamic "FIFO" memory organized as 263 rows × 720 columns × 6 bits (compatible with NTSC composite signal processing)
- First FIFO operation:
  Serial access time: 65 ns (MAX.)
  Serial cycle time: 88 ns (MIN.)
- Power consumption:
  Operating: 413 mW (MAX.)
  Standby: 83 mW (MIN.)
- 6-bit parallel I/O pin
- Uninterrupted, simultaneous read/write capability
- Built-in top address data register for memory address reset data
- Built-in resettable sequential address generator
- Self-refresh function
- Memory address reset capability for one field
- Single +5 V power supply
- TTL compatible I/O
- CMOS double-metal process
- Package:
  22-pin, 400-mil DIP

DESCRIPTION

The LH66180 is a 189,360 × 6 bit dynamic FIFO memory which provides fast image data processing at a 6 bit rate. Since it is compatible with 3 f_{SC} sampling and one field of 6-bit quantized data, the LH66180 is applicable to a field memory for use in VCRs and video disc recorders.

The LH66180's memory block is divided into two sections so that fast image data of large capacity can be efficiently processed. Those two sections of memory block are alternately accessed to read and write data simultaneously and continuously.

PIN CONNECTIONS

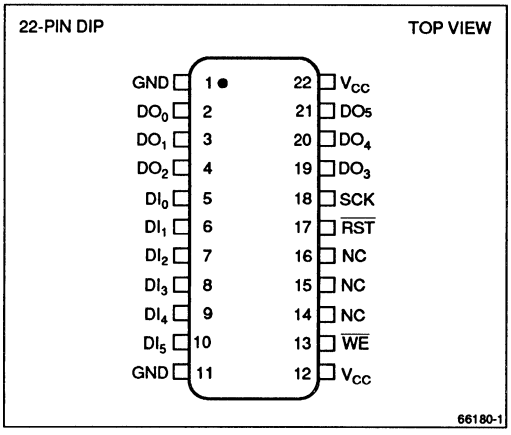


Figure 1. Pin Connections for DIP Package

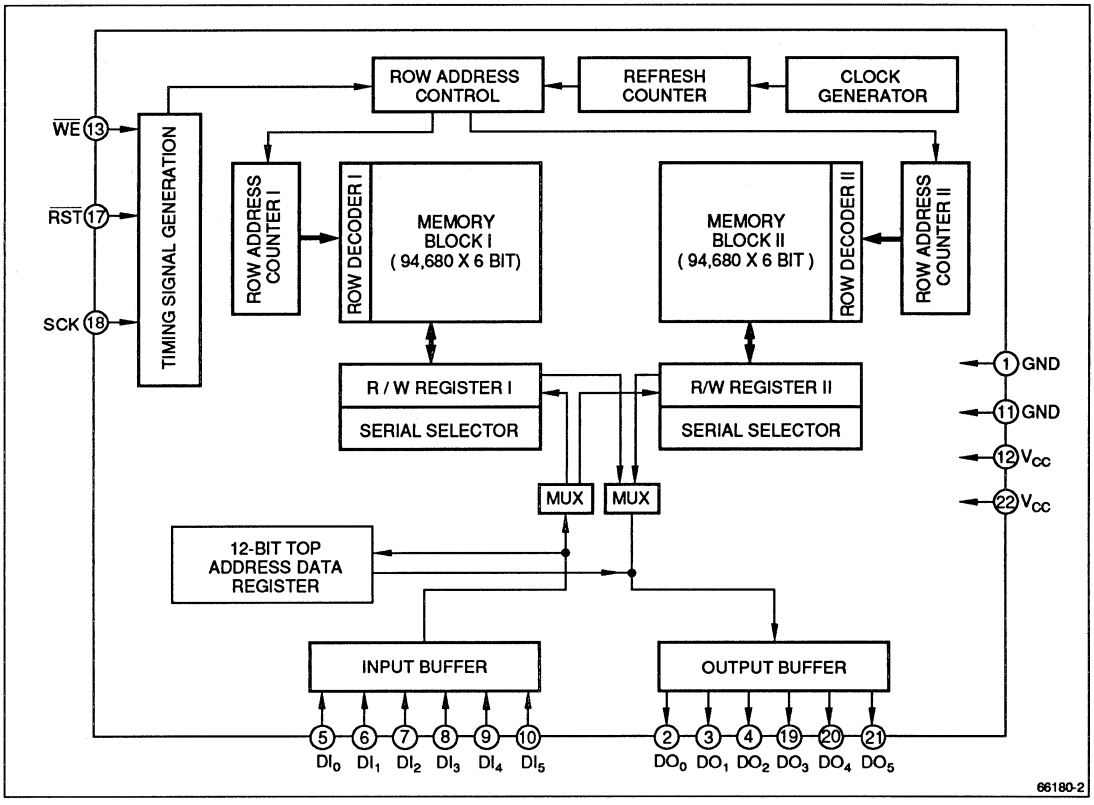


Figure 2. LH66180 Block Diagram

PIN DESCRIPTION

SIGNAL	I/O	PIN NAME
DI_0 - DI_5	I	Serial input for 6-bit data to be received from A/D converter.
DO_0 - DO_5	O	Serial output for 6-bit data to be transferred to D/A converter.
SCK	I	Serial clock input. Applying a HIGH level signal to the SCK pin places the device in self-refresh mode.
$\overline{RST}$	I	Reset input for an accessed memory address. The memory address is reset in response to the fall of the $\overline{RST}$ signal, and restarts memory cycling from the top address of memory.
$\overline{WE}$	I	Write control input for one field of serial input data. Applying a LOW level signal to $\overline{WE}$ pin allows read/write operation. A HIGH level signal allows read operation
V_{CC}	I	+5 V power supply *
GND	I	0 V power supply *

NOTE: The device has multiple V_{CC} and GND for reduced noise. All V_{CC} and GND pins must be connected.

READ OPERATION

The Field Memory consists of a DRAM cell array which is divided into two blocks, and a top address register which is accessed immediately after a reset. Data is output from DO_0-DO_5 synchronously with SCK. The first 12 bits of data are accessed from the top address register in response to the fall of the $\overline{RST}$ signal. During this period, data in all the memory cells linked to row address No. 1 of the first memory block are transferred to the first R register. This data is subsequently output in succession from the first R register by the SCK clock. Before all the data is output from the first R register, the second memory block becomes active, and data in all the memory cells linked to row address No. 1 of the second memory block are transferred to the second R register. These are output by the SCK clock following the last data of the first R register. In this manner, the memory blocks are alternately accessed, so that data can be continuously output from the alternate R registers by the SCK clock. Whenever the memory address is reset with the $\overline{RST}$ signal, data is re-read starting with the top address register. Thus, uninterrupted reading of data is made possible.

WRITE OPERATION

Data is input through DI_0-DI_5 whenever $\overline{WE}$ = "Low". The first 12 bits are input to the top address register in response to the fall of the $\overline{RST}$ signal. Thereafter, data is input to the first W register, synchronously with the SCK clock. Once the first W register becomes filled with input data, subsequent input data is directed to the second W register. Meanwhile, the contents of the first W register are transferred into row address No. 1 of the first memory block. Once the second W register becomes filled, its contents are transferred into row address No. 1 of the second memory block, while the first W register receives new input data. In this manner, the data is alternately input to the W registers, then transferred to the memory cells one row at a time. This operation is alternately repeated until the memory address is reset by the $\overline{RST}$ signal, causing data to be input to the top address register while the row address is reset. Thus, uninterrupted writing of data is made possible.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE: 1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		6.5	V
	V_{IL}	-1.0		0.8	V

NOTE: Referenced to GND.

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input voltage	V_{IH}		2.4	6.5	V
	V_{IL}		-1.0	0.8	V
Output voltage	V_{OH}	I_{OUT} = -2 mA	2.4		V
	V_{OL}	I_{OUT} = 4.2 mA		0.4	V
Operating current	I_{CC}	During normal operation t_{SCC} = MIN., outputs open		75	mA
Standby current	I_{SB}	SCK = V_{IH} (MIN.)		20	mA
	I_{SB1}	SCK = V_{CC} - 0.2 V		15	mA
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V, outputs open 0 V on all other pins	-10	10	µA

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Serial clock "H" pulse width	t_{SCH}	30	40		ns
Serial clock "L" pulse width	t_{SCL}	30	40		ns
Serial clock cycle time	t_{SCC}	88	93	140	ns
$\overline{RST}$ setup time	t_{RSS}	5			ns
$\overline{RST}$ hold time	t_{RSH}	15			ns
Access time from SCK	t_{SCA}			65	ns
Hold time for SCK	t_{SDH}	10			
$\overline{WE}$ setup time	t_{WCS}	5			ns
$\overline{WE}$ hold time	t_{WCH}	0			ns
Setup time for data input	t_{DS}	5			ns
Hold time for data input	t_{DH}	25			ns
Self-refresh start time	t_{REFST}	100			µs

CAUTION:

At power on, for proper operation, at least 500 µs of pause time followed by 1,440 initialization cycles should be given.

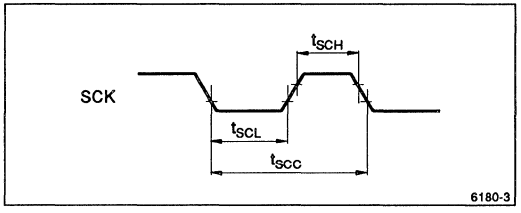


Figure 3. Serial Clock Timing

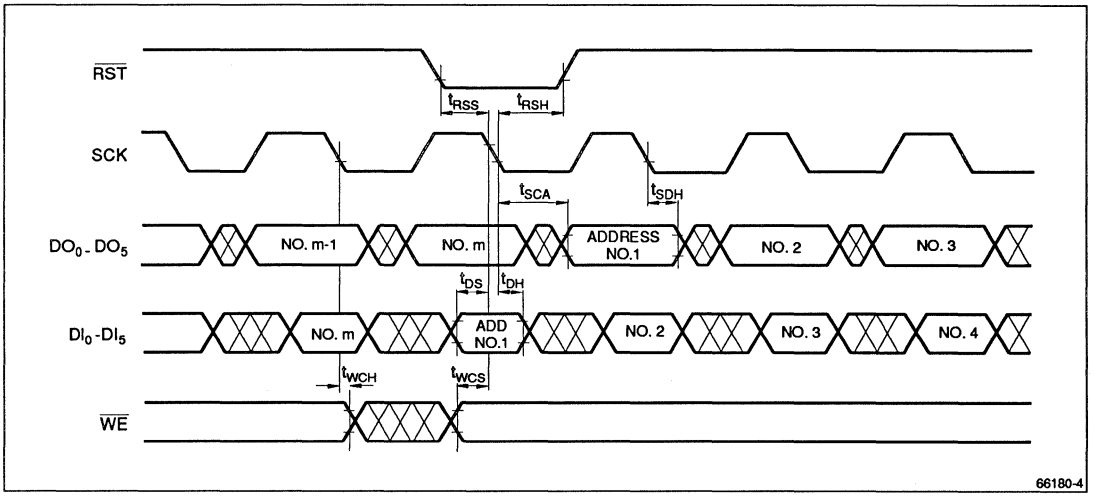
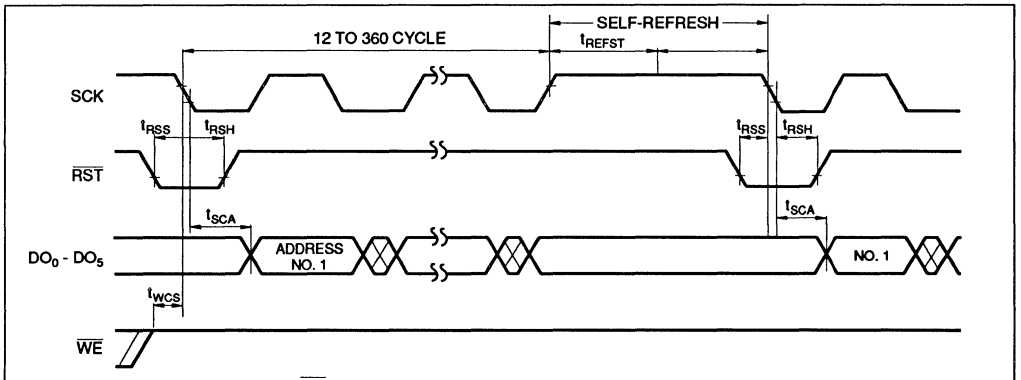


Figure 4. Field Synchronous Mode (Read/Write Cycle)



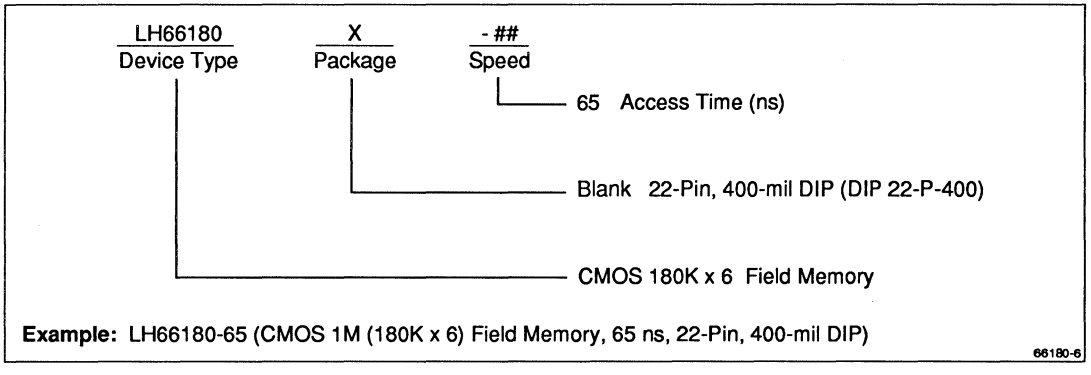
NOTE: Appling a HIGH level signal to $\overline{WE}$ places the device in read-out mode, and still pictures can be obtained.

To enter self-refresh mode, it is necessary to return to the top of a memory address with an $\overline{RST}$ input, while the $\overline{WE}$ signal is kept HIGH in order to inhibit write operation. Then, at least 12 initialization cycles up to 360 cycles should be given. When the SCK goes HIGH for more than 100 µs, the device is placed in self-refresh mode. To resume access after self-refresh, it is necessary to return to the top of a memory address with an $\overline{RST}$ input. Read out the one field after self-refresh by applying a HIGH level signal to $\overline{WE}$.

66180-5

Figure 5. Self-refresh Mode (Note 2)

ORDERING INFORMATION



Example: LH66180-65 (CMOS 1M (180K x 6) Field Memory, 65 ns, 22-Pin, 400-mil DIP)

66180-6

DATABUS FUNNELING MADE EASY

INTRODUCTION

The Sharp LH5420 256 × 36 × 2 CMOS Bidirectional FIFO is an innovative device which turns the difficult task of funneling and defunneling different-size databusses into an easy one-component solution. Funneling refers to a situation where data from a larger databus (eg. 32-bits wide, 36-bits with parity) must be segmented (usually in increments of 8-bits, 9-bits with parity) and transferred to a smaller databus (eg. 8-bits wide, 9-bits with parity). The funneling options available on the LH5420 are "36-bits to 9-bits" and "36-bits to 18-bits". Defunneling refers to just the opposite of funneling. To defunnel, data from a smaller databus (eg. 8-bits wide, 9-bits with parity) is combined together sequentially with other data from that databus, and transferred in parallel to a larger databus (eg. 32-bit wide, 36-bit with parity). The defunneling options available are "9-bits to 36-bits" and "18-bits to 36-bits". For wide word applications on both ports, "36-bit to 36-bit" buffering is also available.

A very important feature of the LH5420 is the ability to operate bidirectionally. The term Bidirectional refers to the LH5420s ability to funnel and defunnel between different sized databusses, allowing data to travel in both directions. Bidirectional operation is also available when the full width of both ports are used (eg. 36-bit to 36-bit buffering).

The advantages of the LH5420 bidirectional FIFO to the system designer are: elimination of several conventional FIFOs and glue logic; significant reduction of board space; elimination of the complexities of handling bus contention; and improved system performance. But, most importantly, it makes databus funneling easy.

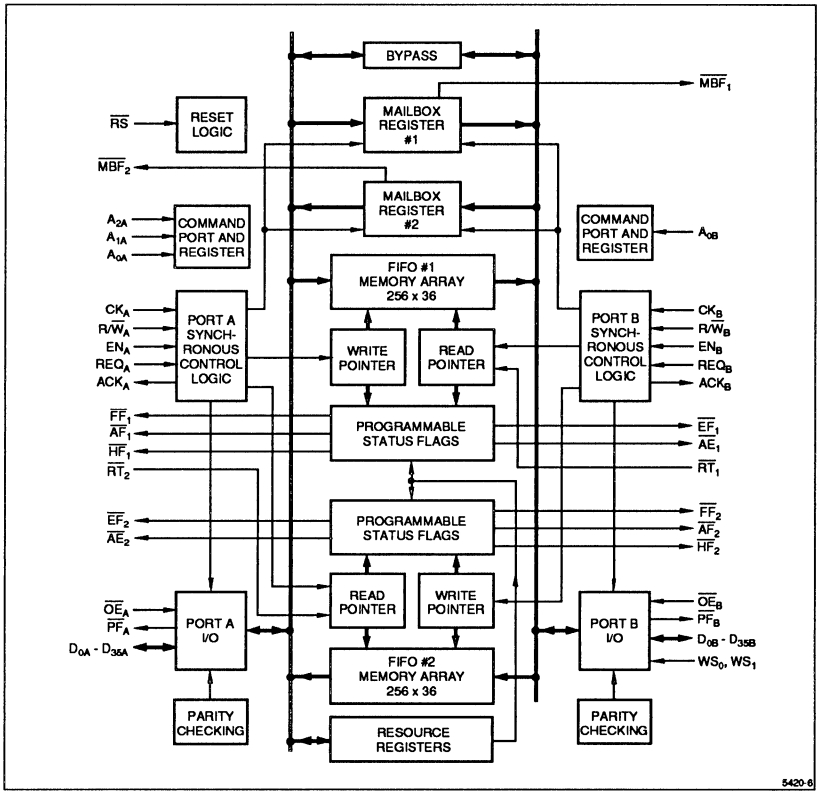


Figure 1. LH5420 Block Diagram

CONVENTIONAL DATABUS FUNNELING SOLUTIONS CAN BE AWKWARD

The rapid transfer of information between a databus of one size to a databus of a different size (funneling or defunneling) seems like a simple enough operation, when viewed on paper in block diagram form; but the block diagram must be transformed into a high-speed circuit design. Conventional solutions require many components, and considerable board area. Further, the timing required for reading, writing, and flag detection for multiple parts in parallel, places a heavy burden on reliable high speed operation.

CONVENTIONAL FUNNELING CIRCUIT DESIGN

Figure 2 shows a bus-funneling circuit designed using conventional components. Figure 2a is an example of the timing required to use the circuit in Figure 2. Figure 3 shows the circuit which must accompany Figure 2 if the circuit were expected to operate bidirectionally (funnel and defunnel). Figure 3a is an example of the timing required to use the circuit in Figure 3. An obvious disadvantage of this conventional funneling circuit is the number of components required. One "Programmable Logic Device" (PLD) and four standard 256 × 9 FIFOs are required for one-way funneling. If bidirectional operation (funneling and defunneling) is important, two PLD's and eight 256 × 9 FIFOs are required. The combination of all these components results in very restrictive data setup (t_{DS}) and hold (t_{DH}) timings during a Write cycle, and restrictive access timings (t_A) due to the risk of databus contention during a Read cycle. In many cases, high speed operation would be out of the question. Tight controls on signal noise and signal skew might also be required to keep the four FIFOs synchronized. After all this, the circuit designer would do just about anything for a single-chip solution. Setup and Hold times for a single asynchronous 256 × 9 FIFO are typically 10 ns and 0 ns respectively for access times of 20 ns. Because this defunneling circuit is a combination of separate components (see Figure 3), setup and hold times would have to be increased significantly to ensure correct synchronization due to signal propagation delays of the control signals and data. In a conventional defunneling circuit, there could be as many as four 9-bit words waiting to be written sequentially into four different FIFOs. Each of the four 9-bit words requires its own setup (t_{DS}) and hold (t_{DH}) time (see Figure 3a). These restrictions will limit the maximum defunneling frequency of this circuit.

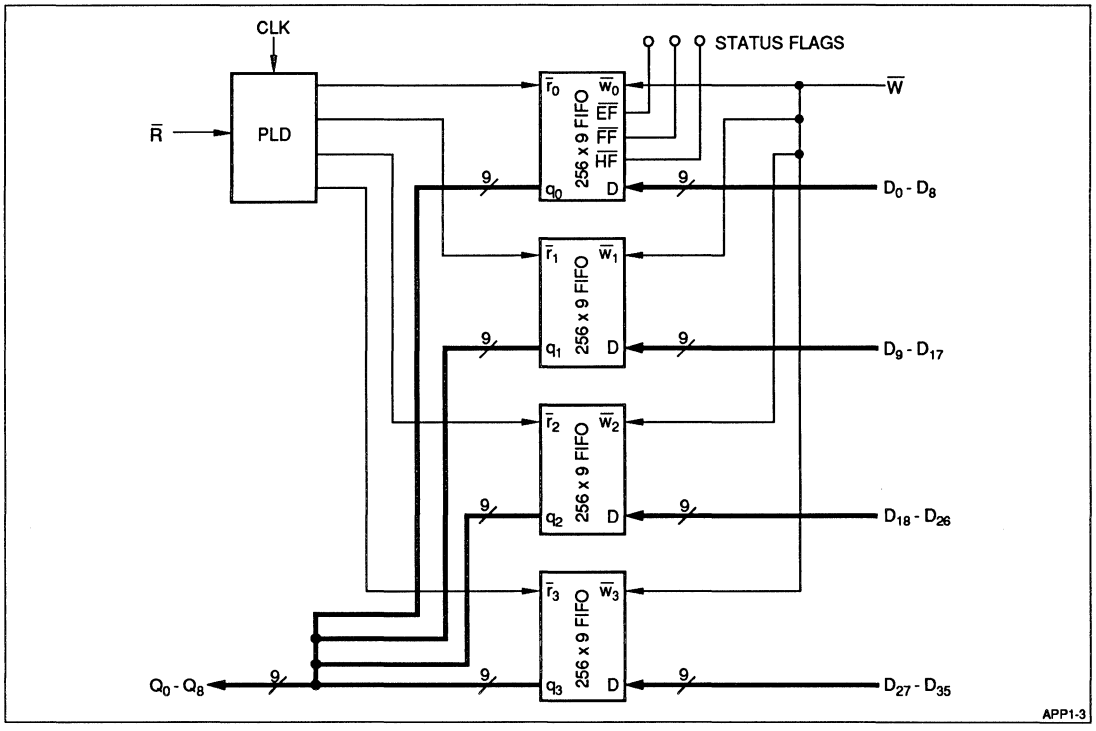


Figure 2. 36-Bit to 9-Bit Conventional Funneling FIFO Circuit

Databus contention is a common problem experienced when combining two or more output pins from different devices in parallel, on the same databus (see Figure 2). If during a Read cycle, at least two of the output pins happen to be momentarily on at the same time, the two output drivers potentially could fight against each other driving the data bus to opposite logic states (one driver pulling the bus to 0V, while the other driver is simultaneously pulling the bus to 5 V). Databus contention degrades system performance and increases the system operating current.

Another significant disadvantage with using the conventional component solution is handling the flags. Each 256 × 9 FIFO has 3 types of flags which can be used in the application to indicate the current FIFO status (Empty , Full, or Half Full). Most designers use a flag from only one of the four FIFOs. This flag-handling technique has a significant disadvantage. When a flag from only one of the four 9-bit wide FIFOs is used to represent the entire 36-bit word, there is no way to insure that the other three FIFO flags are synchronized (empty, full, or half full at the same time) with the first. There is the possibility that one, two, or all three of the other FIFOs may have become unsynchronized (due to signal noise, excessive signal skew, etc.) and are now contributing incorrect data to the 36-bit word.

SHARP's Single Chip Solution to the Complexities of Funneling

The LH5420 CMOS Bidirectional FIFO was designed specifically to simplify the handling of wide-word (up to 36-bits) data buffering. The notable features of this device relating to data bus funneling are:

- Selectable 36/18/9-bit Word Width on Port B
- Two 256 × 36-bit FIFO Buffers for Bidirectional Operation
- Synchronous operation on both Ports A and B
- Fully Asynchronous Communications between Port A and Port B
- Only One Set of Flags for the Entire 36-bit Wide Word
- Capable of 40-MHz operation

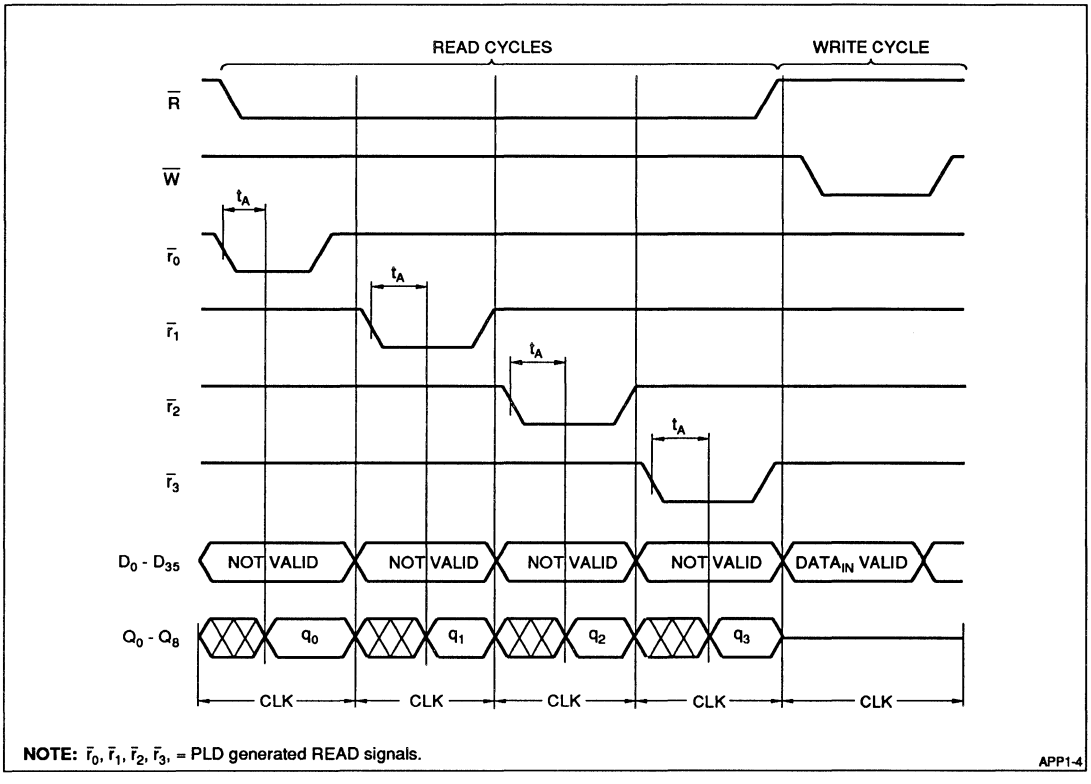


Figure 2a. 36-Bit to 9-Bit Conventional Funneling Write and Read Timing Diagram

The LH5420 provides an easy one chip solution to the problems associated with funneling one size databus to a different size databus (see Figure 3). The LH5420 also provides a simple method of buffering wide word databusses up to 36 bits wide on each port. There are two ports on the LH5420, Port A and Port B. A Port is defined as an interface between the outside databus and the internal FIFO memory. Each port can be used as an input or an output depending on which direction the data will travel. The LH5420 allows Port B to be selectable in word widths from 36, 18 or 9 bits wide, while Port A is fixed at 36-bits wide.

Two separate 256 × 36-bit FIFO buffers work side-by-side to move data in opposite directions. This is what enables the LH5420 to operate bidirectionally. As an example, a 36-bit databus and a 9-bit databus can send and receive data back and forth, giving unrestricted communication privileges between an 8-bit microcontroller and a 32-bit microprocessor. Clock-frequency differences between the two busses are not an issue. Even though the individual ports are synchronous in nature, each port is controlled from separate system clocks (CKA and CKB). Each port operates independently from the other, so that port-to-port communication occurs asynchronously.

The LH5420 has five different types of flags available: Full Flag (FF), Empty Flag (EF), Half Full Flag (HF), Almost Full Flag (AF), and Almost Empty Flag (AE). The Almost Empty and Almost Full Flags are programmable. One set of these flags are available for each 256 × 36 FIFO buffer, to cover the status of data going in either direction. The low skew inherent in a single monolithic solution eliminates the risk that desynchronization will occur within the 36-bit wide word in the FIFO. Further protection is afforded because the flags cover the full 36-bit word width and not just the 9 bits that were used in the conventional funneling design mentioned above. The problems of designing a system around restrictive read and write timing constraints are no longer an issue, because the complexities of funneling timing synchronization are handled automatically within the LH5420 bidirectional FIFO.

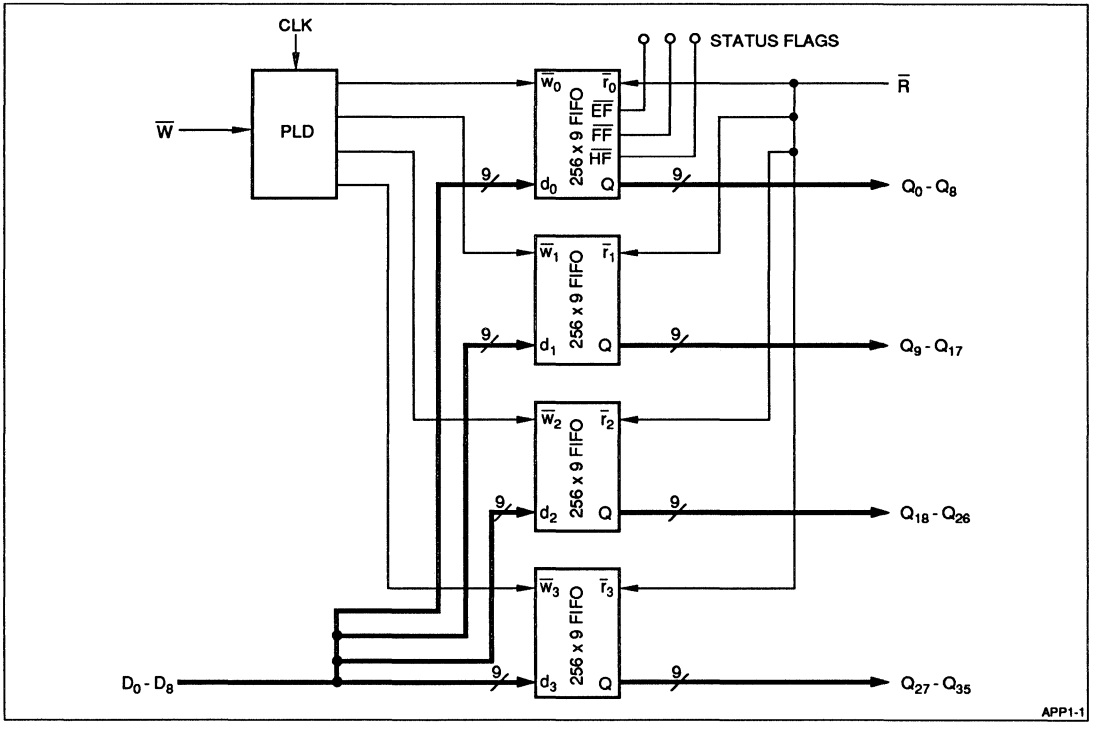


Figure 3. 9-Bit to 36-Bit Conventional Funneling FIFO Circuit

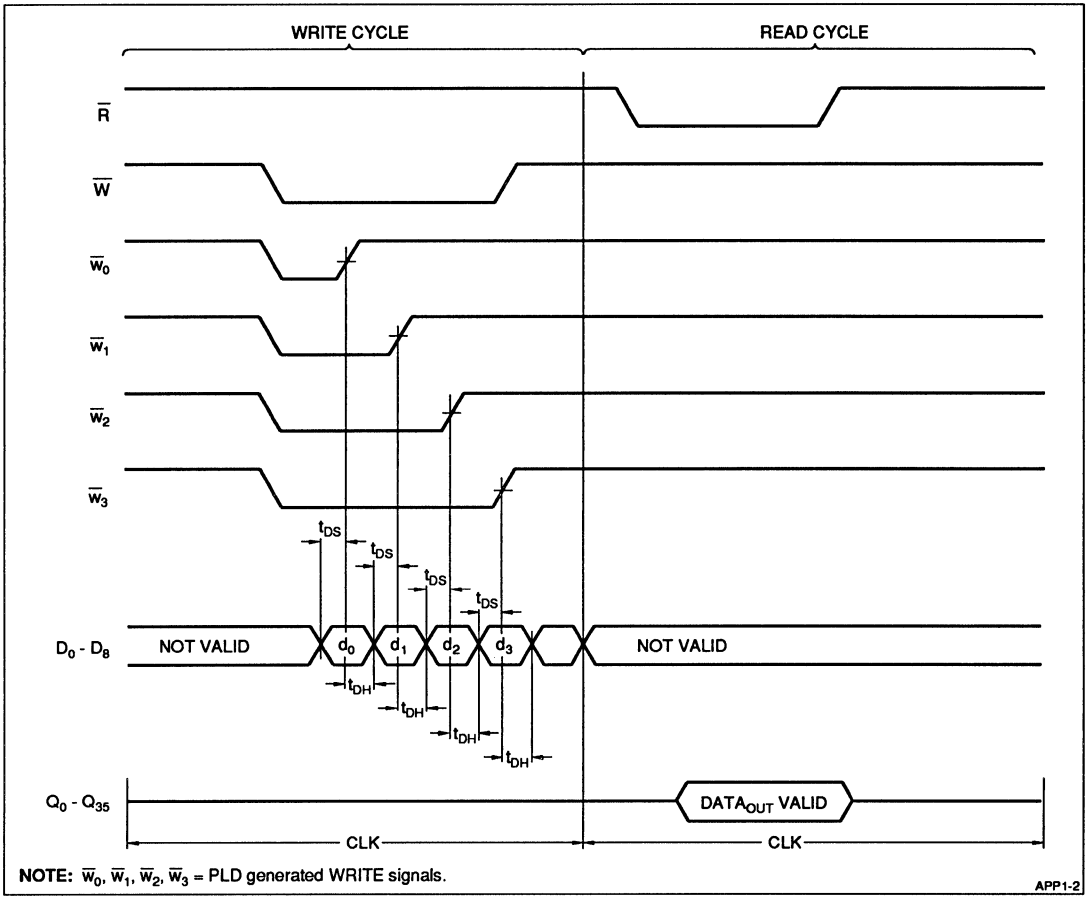


Figure 3a. 9-Bit to 36-Bit Conventional Defunneling Read and Write Timing Diagram

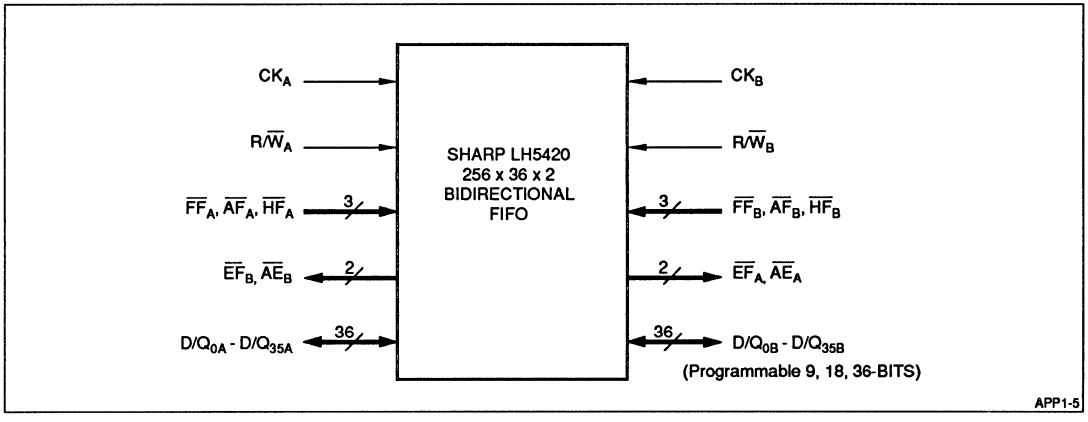


Figure 4. LH5420, the Single Chip Solution for Databus Funneling

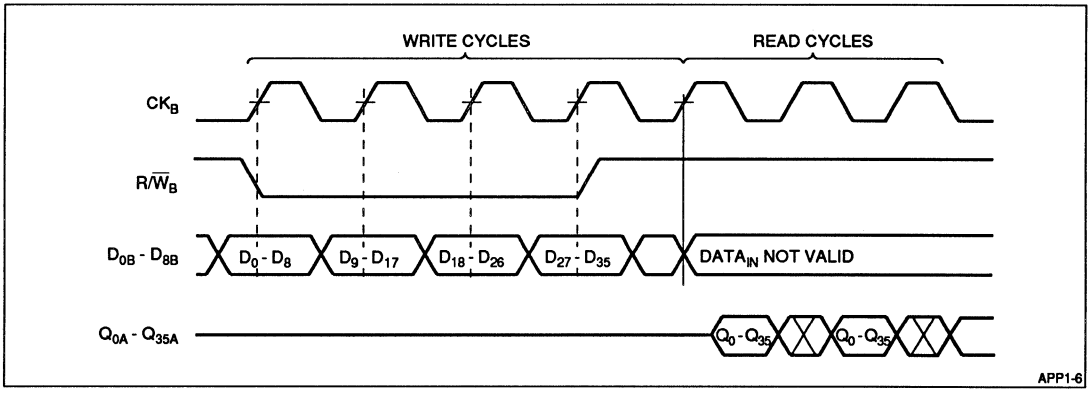


Figure 4a. LH5420 9-Bit to 36-Bit Funneling Write and Read Timing Diagram

SUMMARY

The SHARP LH5420 bidirectional FIFO provides many benefits to a system designer working on applications which use wide word databusses (36 bits wide), or applications which require funneling and defunneling between databusses of different widths (eg. 8-bit to 32-bit, 18-bit to 36-bit, etc.). In comparison with conventional databus funneling methods, the LH5420 simplifies your circuit design, allows faster operating speeds, uses less board space, reduces component count, and provides bidirectional funneling with no additional circuitry. But best of all, it is easy to use.

A ONE-CHIP TWO-WAY STREET FOR MICROPROCESSOR COMMUNICATIONS: THE SHARP LH5420 36-BIT BIDIRECTIONAL FIFO *

Chuck Hastings
Marketing/Applications Manager, FIFO and Specialty Memories

Sharp Microelectronics Technology, Inc.
5700 N. W. Pacific Rim Boulevard
Camas, WA 98607
206/834-8615

INTRODUCTION

New integrated circuits often evolve as single-chip embodiments of groups of lower-complexity parts. When the same multiple-device configuration starts turning up in many new designs, a semiconductor manufacturer may get inspired to develop a one-chip-does-all replacement just by listening to its customers. Bidirectional FIFOs, wide enough to hold an entire word of data, are one such frequently-occurring combination. Perhaps one out of every five system applications for FIFOs fits this description. Usually, the role of a bidirectional FIFO is to provide convenient two-way communication between two processors or microprocessors.

In the past, an effective bidirectional FIFO for communication back and forth between two 32-bit-processors has needed to consist of at least *eight* industry-standard byte-wide unidirectional FIFO devices, arranged into two 'back-to-back' ranks of four paralleled FIFOs each. When parity checking is implemented, the data path between processors becomes 36-bit. Sometimes only one of the two processors is 32-bit, and the other one is 16-bit or 8-bit. In this event, even more devices must be added, to implement multiplexing, demultiplexing, and control functions at the narrower end of the bidirectional data path.

The LH5420 256 × 36 × 2 bidirectional FIFO, now available from Sharp, is a 'one-chip-does-all' solution to such system requirements for two-way interprocessor communication. One LH5420 can provide either a convenient fully-parallel two-way connection from one 36-bit bus to another such bus, or it can provide a two-way 'funneling/defunneling' connection from a 36-bit bus to an 18-bit bus, or to a 9-bit bus. Thus, the LH5420 supports all of the usual microprocessor word widths, and accommodates the extra bit per byte for parity or marker-bit usage. It operates at up to 40 MHz, and is available either in a 120-pin PGA package or in a 132-pin PQFP package.

LH5420 ARCHITECTURE AND OPERATION

The LH5420 includes several enhancements, aimed at making a system designer's life easier. The LH5420 itself can check the parity of all bytes passing through it in either direction. And it features programmable almost-full and almost-empty flags, retransmission capability in either direction, 'mailbox' capability in either direction, a limited form of transceiver-mode oper-ation, and a synchronous request/acknowledge capability which is useful in burst-mode communications.

Conceptually, an LH5420 is organized as two 36-bit-wide bidirectional ports, Port A and Port B. Two full-width 256-word FIFOs, FIFO # 1 and FIFO # 2, are connected between the two ports, one transmitting in each direction. (See Figure 1.) There are also two full-width one-word mailboxes between the two ports, one likewise transmitting in each direction. And there is a full-width bidirectional data bypass path, which functions during a reset operation. Two asyn-

* See copyright information on page 11.

chronous control inputs set the data width of Port B at 36 bits, at 18 bits, or at 9 bits.

Each port has its own clock input. In typical applications, a port's clock input is connected to a periodic free-running clock signal, which may or may not be derived from the same frequency source as the other port's clock input. Each port also has three control inputs which are sampled at the rising edge (LOW-to-HIGH transition) of its clock: read/write, enable, and request. Each port also has an 'Acknowledge'

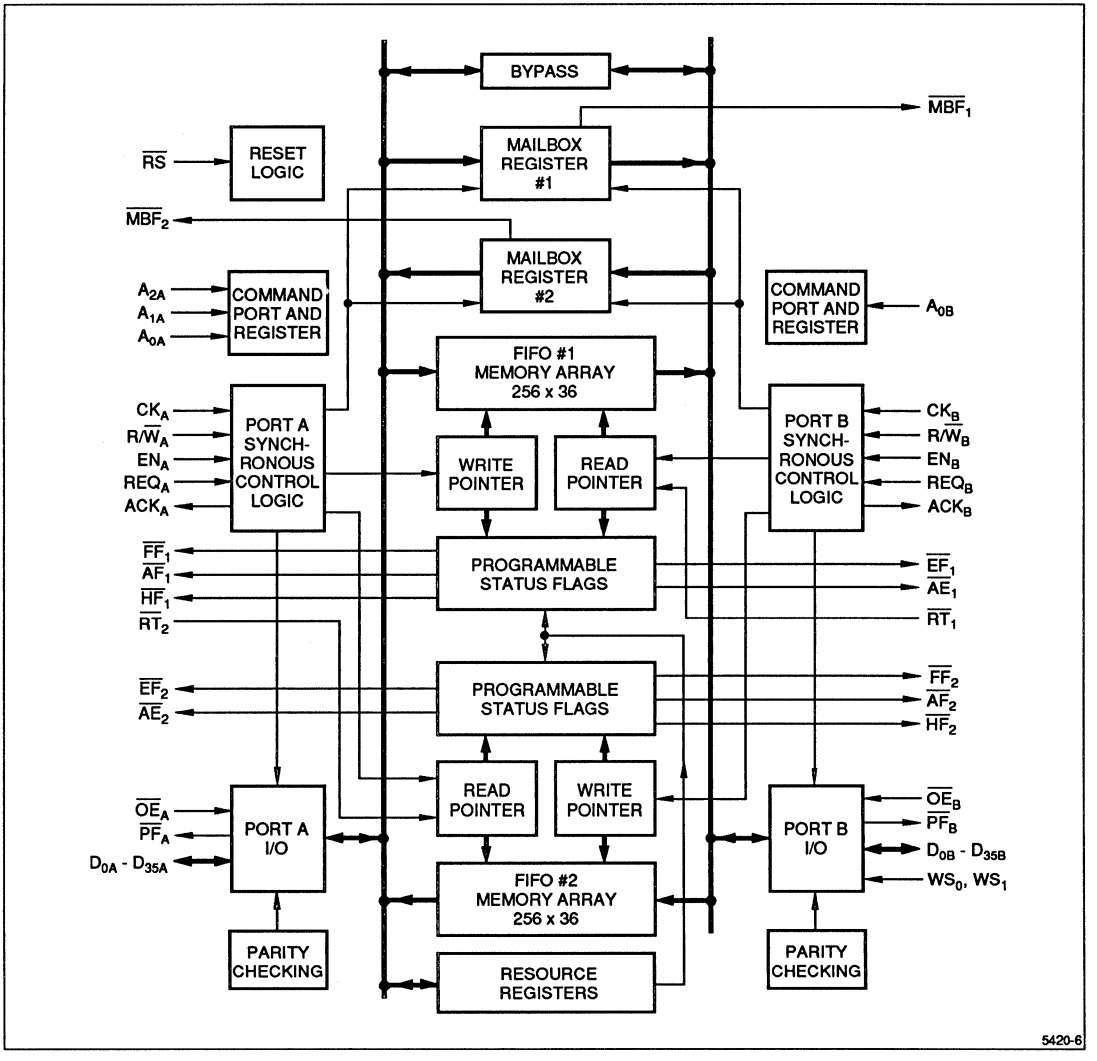


Figure 1. LH5420 Block Diagram

output which is synchronized to its clock, a parity flag output, and asynchronous control inputs for initiating data re-transmission and for enabling/disabling its data outputs.

FIFO # 1 and FIFO # 2 each have five status flags to indicate relative fullness: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Full, Half-Full, and Empty flags are hard-wired to signal exactly what their names indicate. But there are programmable 'offsets' controlling the operation of the Almost-Full and Almost-Empty flags, to numerically define the boundaries of the 'Almost-Full' region and the 'Almost-Empty' region. These offset values are both initialized to eight during a reset operation; but either one may be changed under system control, independently of the other one, to any value from zero to 255.

While a data transfer is actually taking place, the port's Acknowledge output repeats the same information as either the Almost-Full flag or the Almost-Empty flag, depending on the current direction of data transfer – Almost-Full when writing, and Almost-Empty when reading.

The five relative-fullness status flags may change state either in response to a write event clocked at one port, or else in response to a read event clocked at the other port. The port's Acknowledge output signal, however, is totally synchronous with the clock input signal at that port; except, that it gets deasserted immediately if at any time the Request input signal is deasserted.

Both the Request control input and the Enable control input of a port must be asserted, in order for that port to carry out a read operation or a write operation. The Read/Write control input determines which type of operation gets performed.

The action of the Request and Enable signals within the LH5420 are generally similar; but their detailed timing is different. The Enable signal is presumed to be originating as a synchronous signal referenced to the same clock signal used by the port. On the other hand, the Request signal may arise asynchronously, elsewhere in the system; the LH5420 contains resynchronizing circuits, which reference the Request signal to the port clock internally within the LH5420.

Either port may place a full 36-bit word in the other port's mailbox register. Doing so sets a mailbox flag, which is synchronized to the receiving port's clock. This flag is reset whenever the receiving port has read the word in the mailbox register. Both ports have the ability to select either their outgoing FIFO or their outgoing mailbox for writing, or either their incoming FIFO or their incoming mailbox for reading.

Although Port A and Port B both have the capability to send and receive 36-bit data words, each port has one major function unique to it. Port A is the master port for purposes of resource-allocation and control functions, such as changing the value of the offsets for the Almost-Full and Almost-Empty flags, or changing the byte parity scheme from odd parity to even parity. Port B, on the other hand, is the port which is capable of setting its effective data width at 36 bits, 18 bits, or 9 bits.

Two asynchronous inputs control the data width of Port B. Changing this data width does not require any reset operation. However, sufficient time must be allowed for the LH5420's internal byte-shifting and demultiplexing circuits to settle; waiting for two full Port B clock cycles is recommended.

'SYNCHRONOUS' FIFOs AND 'ASYNCHRONOUS' FIFOs

The antonyms 'synchronous' and 'asynchronous' each have taken on two very different meanings in FIFO applications literature. The first meaning has to do with the timing of the FIFO's data and control inputs, and of its data and status outputs. The second meaning has to do with the capability of the FIFO to adjust itself to different and unrelated timing requirements at each of its two ends.

According to the first meaning of these terms, a 'synchronous' FIFO operates with a free-running clock input, but performs operations such

as writing or reading only when these operations are 'enabled.' Data inputs, and control inputs such as enable signals and mode-control signals, must all meet setup time and hold time requirements with respect to the free-running clock. Data outputs and status outputs are presumed valid after some specified delay time has elapsed, following a transition of the free-running clock.

FIFOs which are 'asynchronous,' according to this meaning of 'asynchronous,' do not use any such free-running clock. Some older-architecture 'asynchronous' FIFOs even use edge-sensitive, rather than level-sensitive, control inputs. 'Synchronous' FIFOs sometimes may be made to behave as 'asynchronous' FIFOs, if desired, by connecting their 'enable' inputs to be permanently asserted, and using their free-running clock inputs as asynchronous edge-sensitive 'demand' control input signals.

According to the second meaning of the terms 'synchronous' and 'asynchronous,' however, a 'synchronous' FIFO would be a FIFO having both its input port and its output port always synchronized to the same 'clock' signal; in other words, a glorified shift register. An 'asynchronous' FIFO, on the other hand, can operate with its input port synchronized to one timing signal, and its output port synchronized to a second timing signal having no necessary relation to the first one; and neither timing signal needs to be regular or periodic.

The LH5420 has a free-running-clock-plus-enable control structure; and so its two internal FIFOs are 'synchronous' FIFOs in the first sense of this term, except that the behavior of the five relative-fullness flags is not entirely 'synchronous.' However, they are completely 'asynchronous' FIFOs in the second sense; there is no necessary synchronization relation between the Port A clock and the Port B clock, nor is either of these clocks required to be strictly periodic. This type of behavior is usually considered to be useful, system-friendly, and what FIFOs are all about.

DESIGNING WITH THE LH5420

In some applications, data bursts get pushed through a FIFO at or close to the FIFO's maximum word rate; but the system must take some immediate action if the FIFO ever becomes completely full or completely empty. The LH5420's Request/Acknowledge feature supports such a mode of operation. The Acknowledge output signal meets the setup time and hold time requirements for the Enable input, and may simply be tied back to it, in order to prevent complete filling or complete emptying of the active FIFO. This mode of operation slightly decreases the maximum data rate.

In essence, the Acknowledge signal is a synchronous 'proxy' or 'predictor' for whichever 'Almost' flag is pertinent to the current data-transfer operation. Because synchronous predictive logic is used to determine the state of this signal, it is actually faster than the corresponding flag.

Assume now that a port's Request input is being continuously asserted, say for writing into the outbound FIFO for that port. As long as the FIFO does not get into the 'Almost-Full' region, that is, the number of vacant FIFO physical words never falls below the 'Almost-Full' offset value, then the Acknowledge output is continuously asserted by the LH5420 control logic, and a word gets written into the FIFO as a result of every write-clock pulse. However, if the FIFO does become 'Almost Full,' then the Acknowledge output gets asserted only on every *third* write-clock pulse, rather than continuously. Thus, if the Acknowledge output has been tied back to the Enable input, the wide-open data rate then gets slowed down immediately, so that the writing of each word can be handled on a full-handshake basis. This operational technique allows achieving the maximum data rate much of the time, and yet protects the system against data loss caused by overrunning the FIFO boundaries.

When the system is operating an LH5420 in block-transfer mode, where a full block gets loaded at one port and then gets unloaded at the other port, the Acknowledge signals may be used to locate the end of a block, in lieu of having to implement an external block-length counter. As a simple example, say that the system block length is 193 words. The sending port loads in one complete block, and 55 words from the next block, in burst mode. At this point, its Acknowledge signal gets deasserted, indicating that the FIFO is 'Almost Full.' The Acknowledge signal does behave exactly in this manner, provided that the corresponding 'Almost-Full' flag offset still remains at its default value of eight. The receiving port then unloads the block. If its 'Almost-Empty' offset value has been set to 55, its Acknowledge signal will get deasserted exactly at the end of the block. Since this indication occurs within a clock period, it is fast enough to be accurate without any uncertainty.

The LH5420's parity-checking facilities treat all nine bits alike, of each byte passing through one of the two FIFOs; the 'parity bit' may be in any position within a byte. A ten-input parity gate scans each group of nine bits in the output register of each port; the tenth input of each parity gate is from the even/odd-parity control flipflop, which may be programmed from Port A. This flipflop is set for odd parity when the LH5420 is reset; but it may be reprogrammed to even, or back to odd, at any time subsequently. If any of the four parity gates at a port ever detects an odd number of 'ones' in a byte, *including* the control flipflop in the 'ones' count, then the port's parity flag is asserted as long as the word containing the erroneous byte remains in the output register.

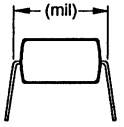
SUMMARY

The LH5420 36-bit bidirectional synchronous FIFO, available now from Sharp, is a system-oriented 'one-chip-does-all' part, intended to simplify back-and- forth communications between two microprocessors, microcontrollers, or similar devices.

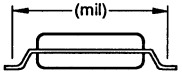
The LH5420 offers several sophisticated features: on-the-fly parity checking, word-width matching of a 36-bit bus to an 18-bit bus or to a 9-bit bus, two-way mailbox communications, and synchronous Acknowledge signals which can be used to give a quick and accurate end-of-block indication or an advance warning of FIFO fullness or emptiness.

In most bidirectional-FIFO applications, one LH5420 replaces many lower-level and discrete parts, and simplifies system design. It offers high performance for burst operations; it can transfer a 36-bit word in each direction every 25 nanoseconds.

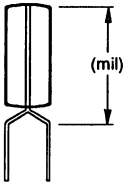
NOMINAL DIMENSIONS



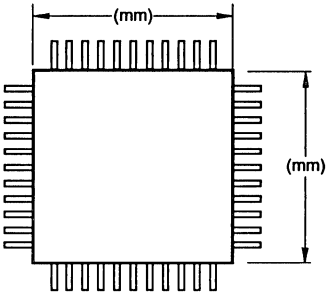
DIP



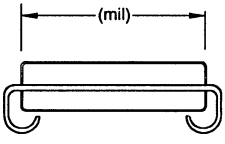
SOP



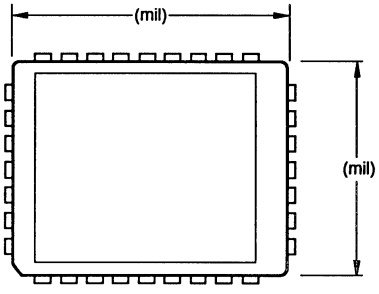
ZIP



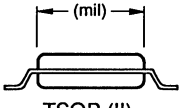
QFP



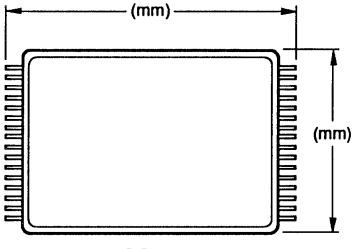
SOJ



PLCC



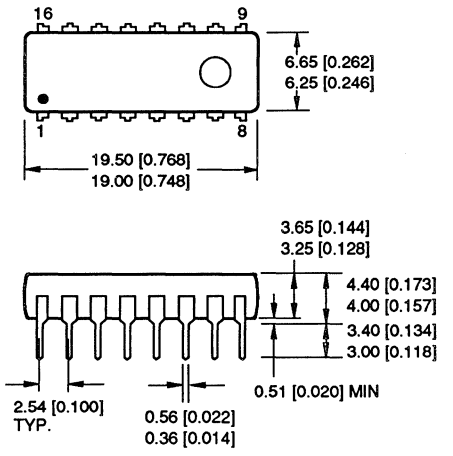
TSOP (II)

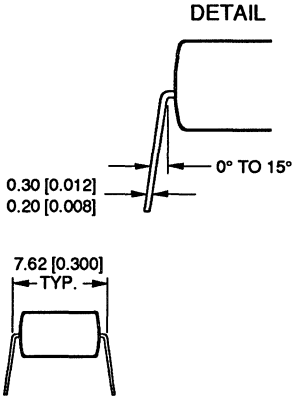


TSOP (I)

ND-1

16DIP (DIP16-P-300)

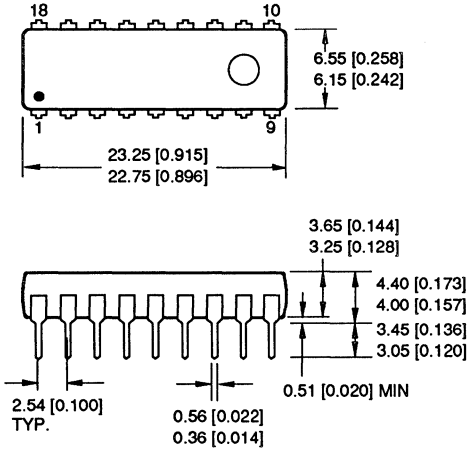


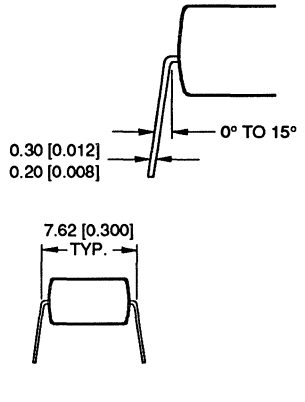


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

16DIP

18DIP (DIP18-P-300)

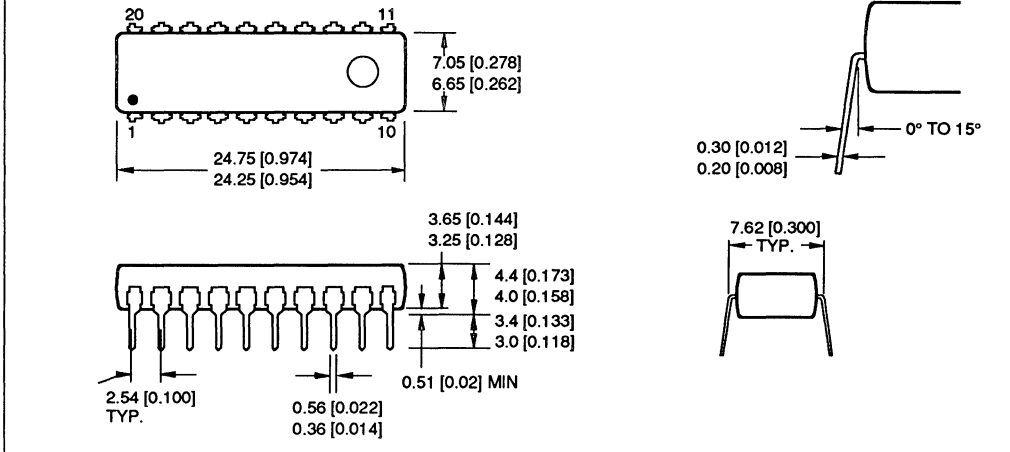




DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

18DIP

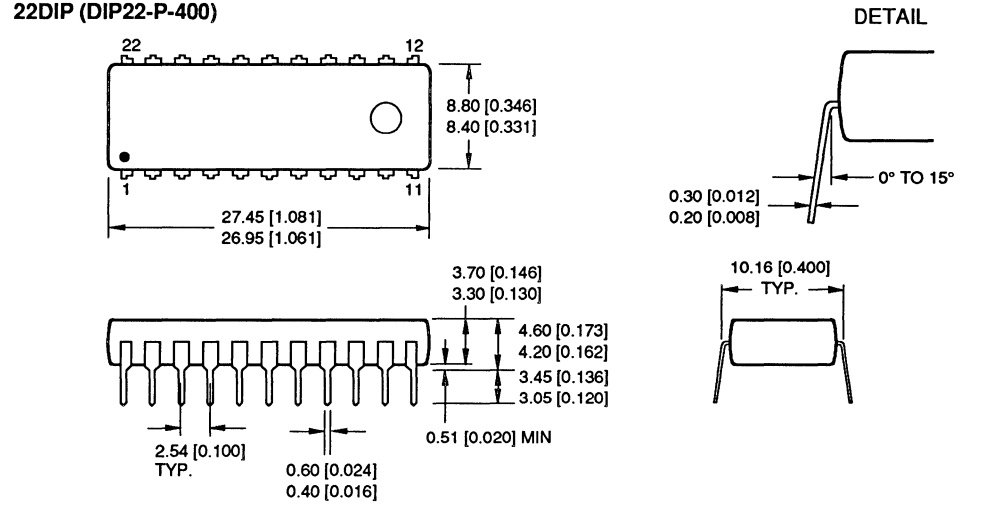
20DIP (DIP-20-P-300A)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

20DIP-2

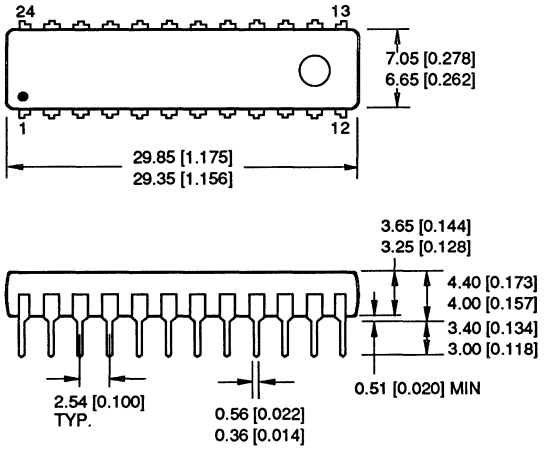
22DIP (DIP22-P-400)



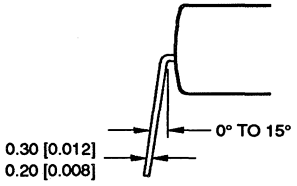
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

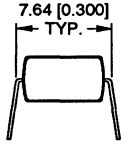
22DIP-2

24DIP (DIP24-P-300)



DETAIL

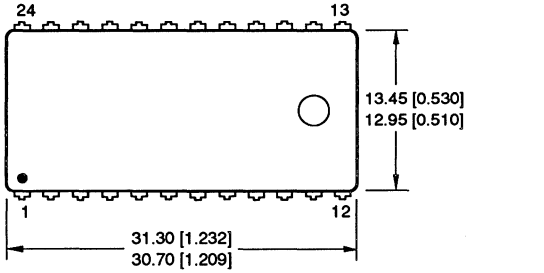




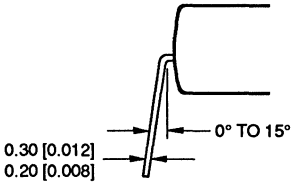
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

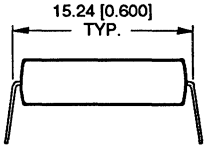
24DIP-1

24DIP (DIP24-P-600)



DETAIL

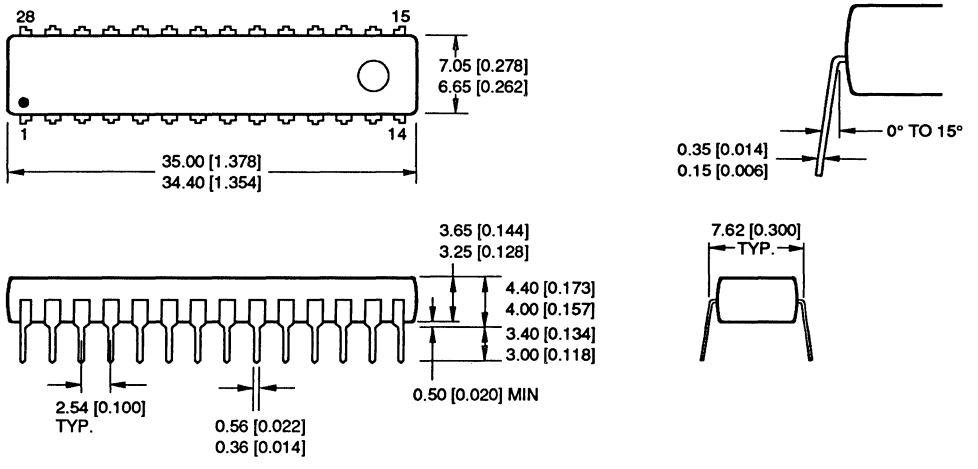




DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24DIP-2

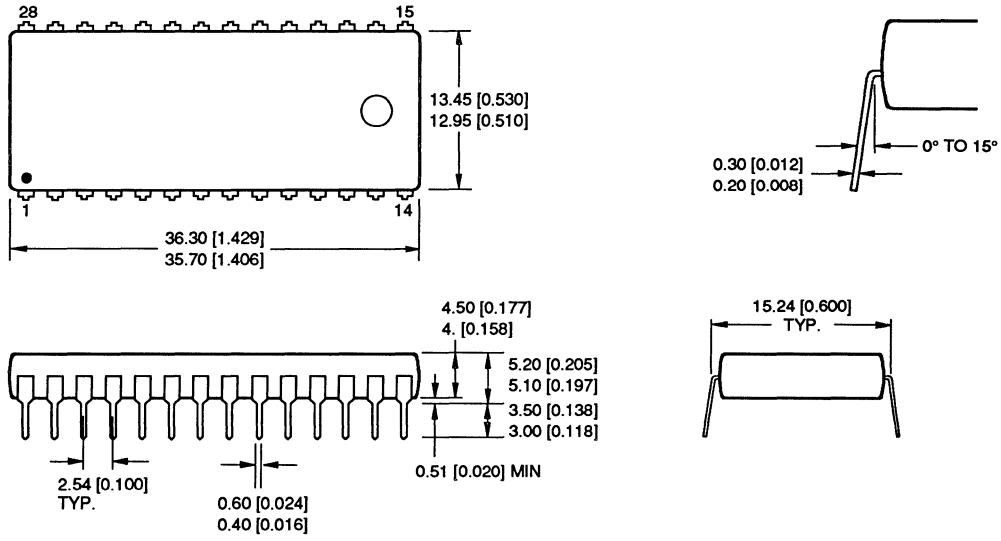
28DIP (DIP28-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-1

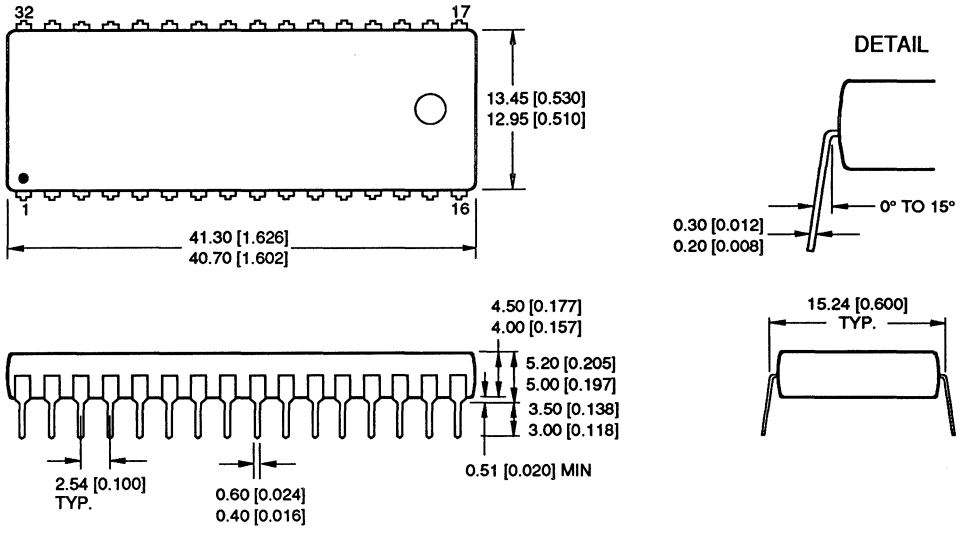
28DIP (DIP28-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

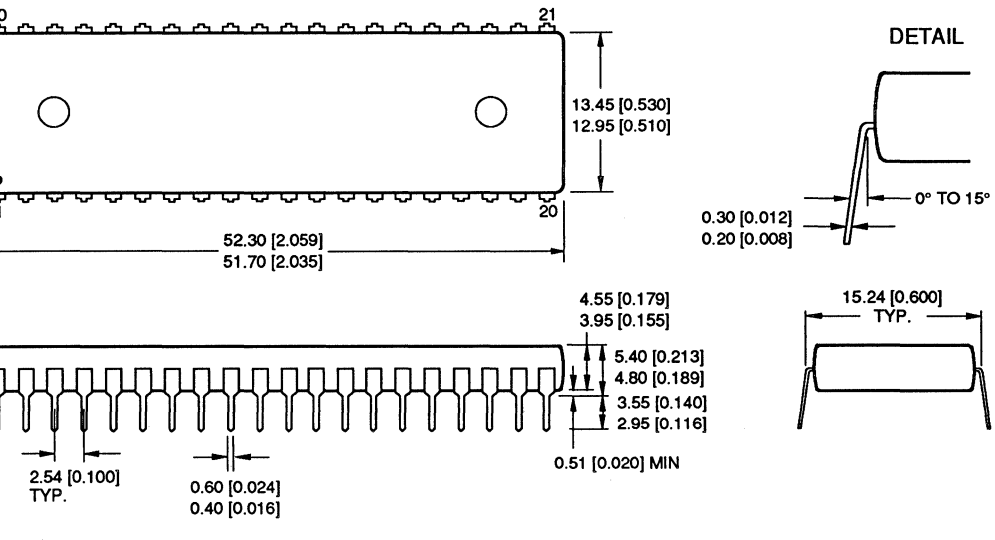
32DIP (DIP32-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32DIP

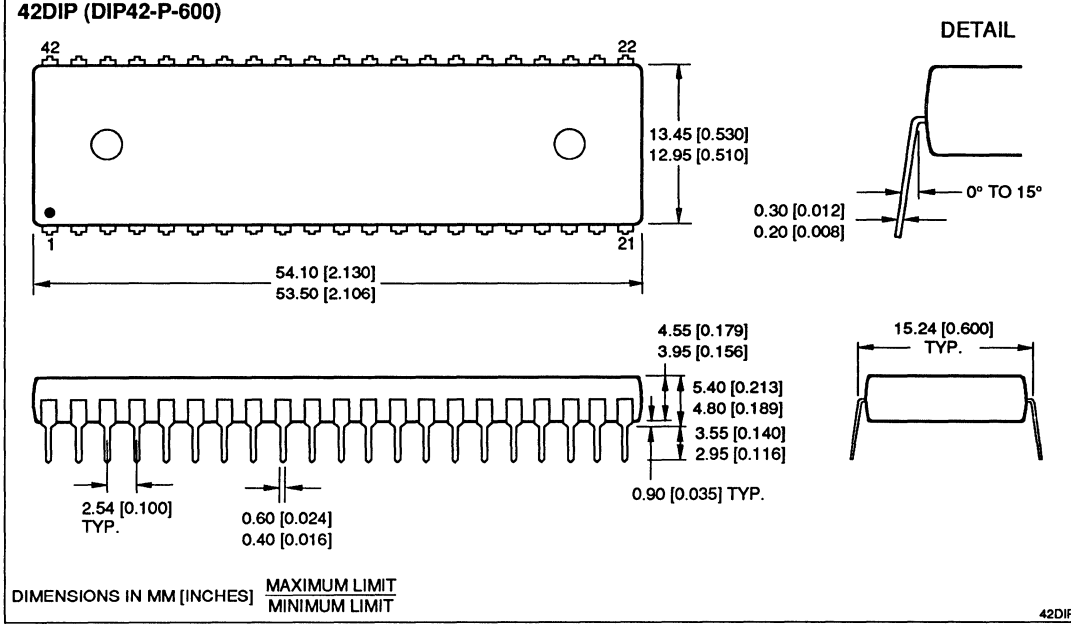
40DIP (DIP40-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40DIP

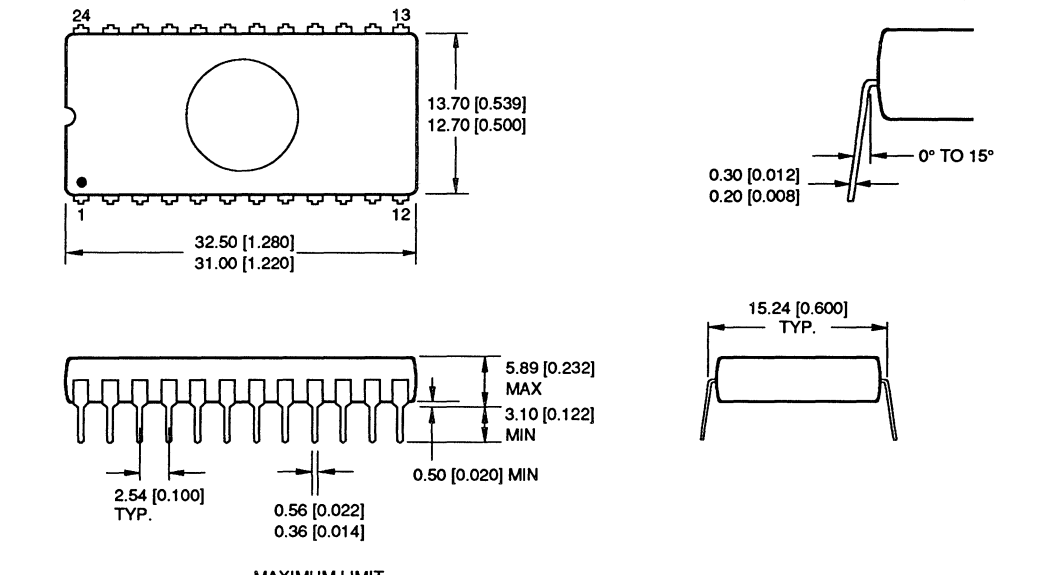
42DIP (DIP42-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

42DIP

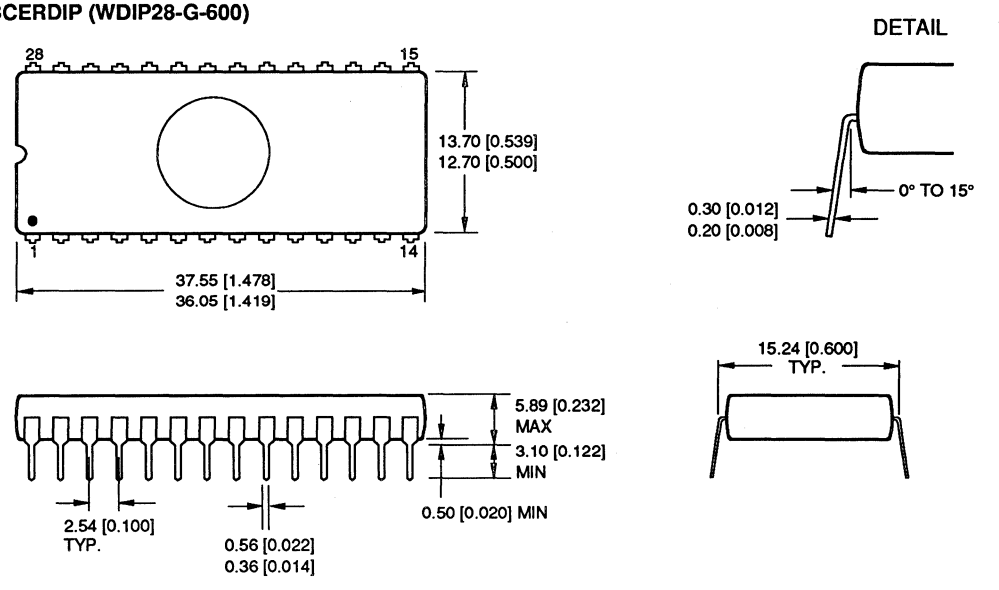
24CERDIP (WDIP24-G-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24CDIP

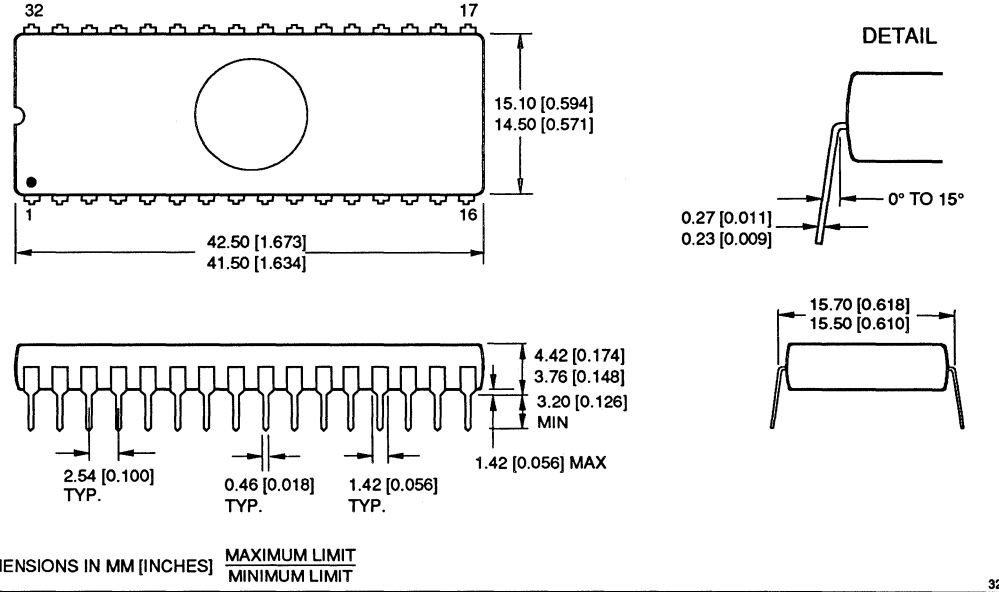
28CERDIP (WDIP28-G-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28CDIP

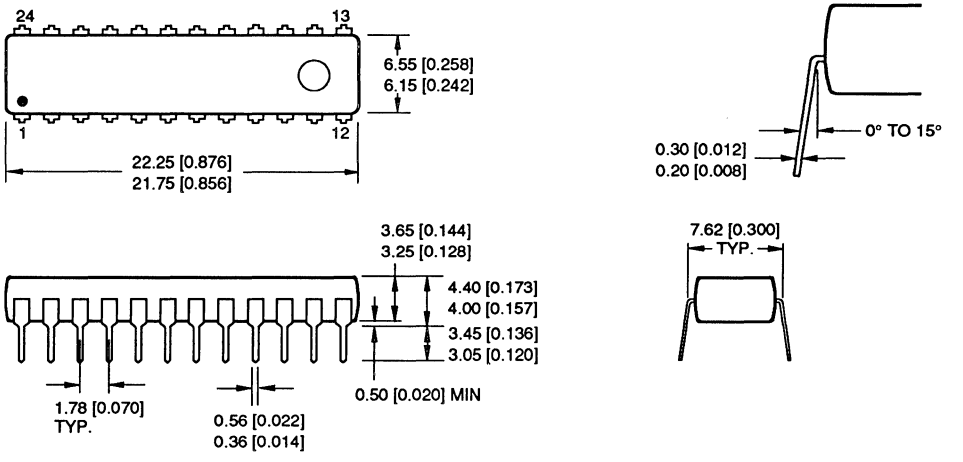
32CERDIP (WDIP32-G-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32CDIP

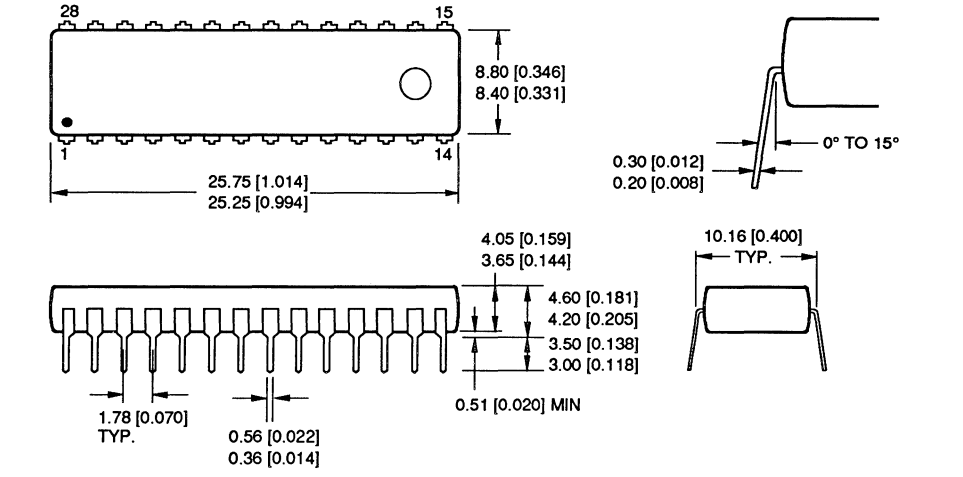
24SDIP (SDIP24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SDIP

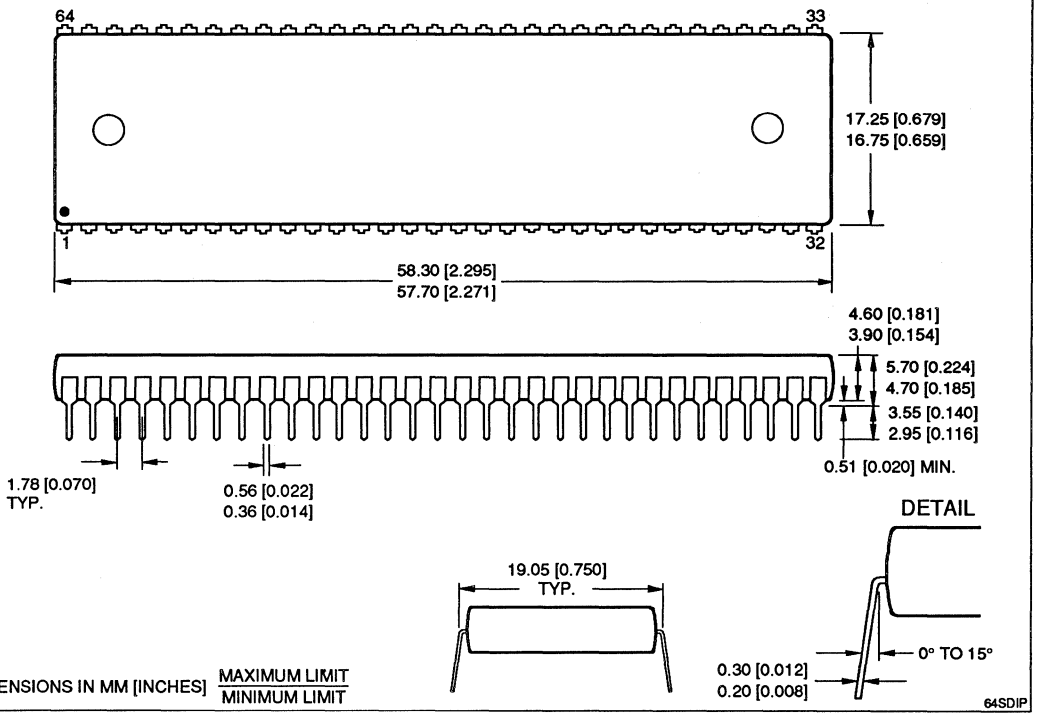
28SDIP (SDIP28-P-400)



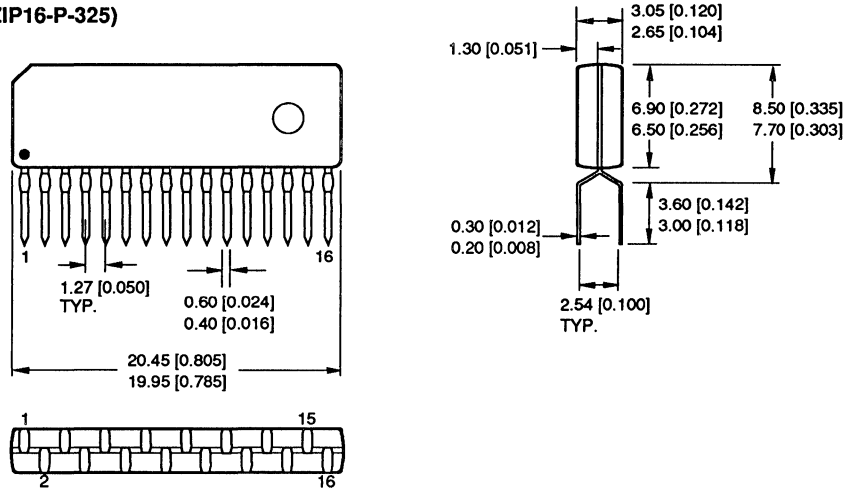
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SDIP

64SDIP (SDIP64-P-750)



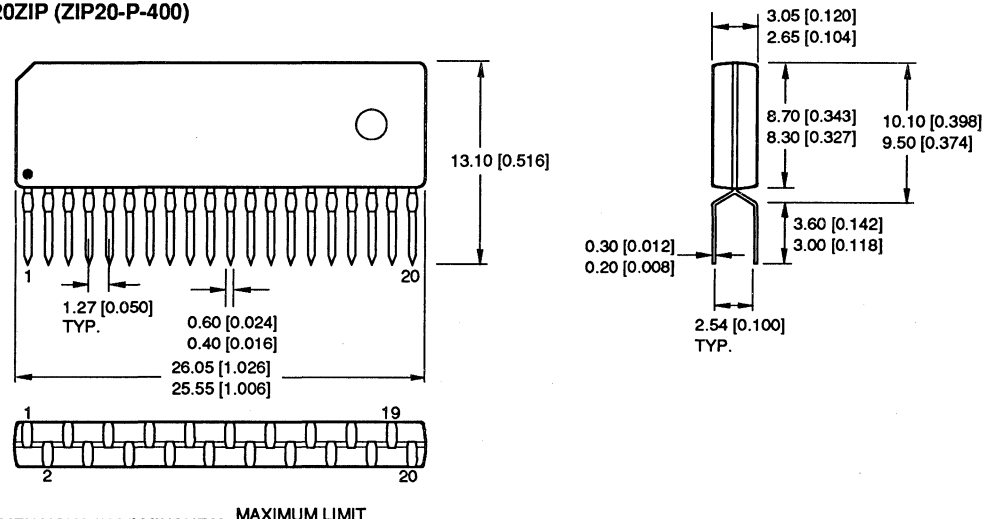
16ZIP (ZIP16-P-325)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

16ZIP

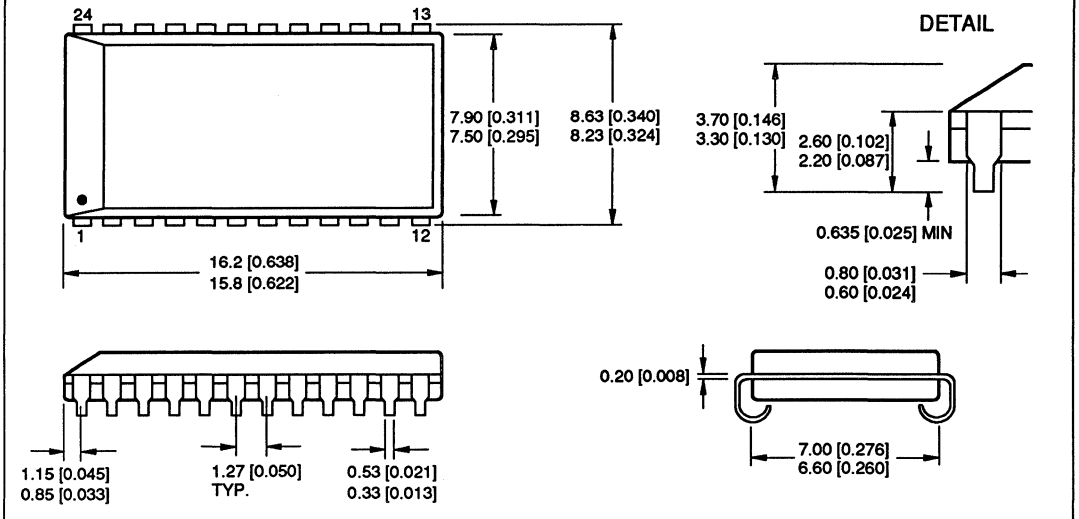
20ZIP (ZIP20-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

20ZIP

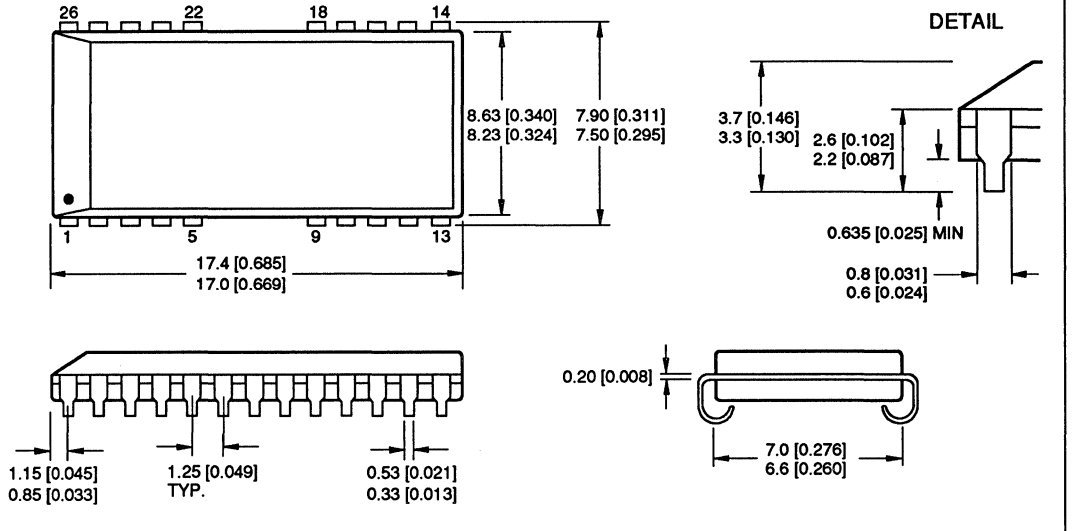
24SOJ (SOJ24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOJ

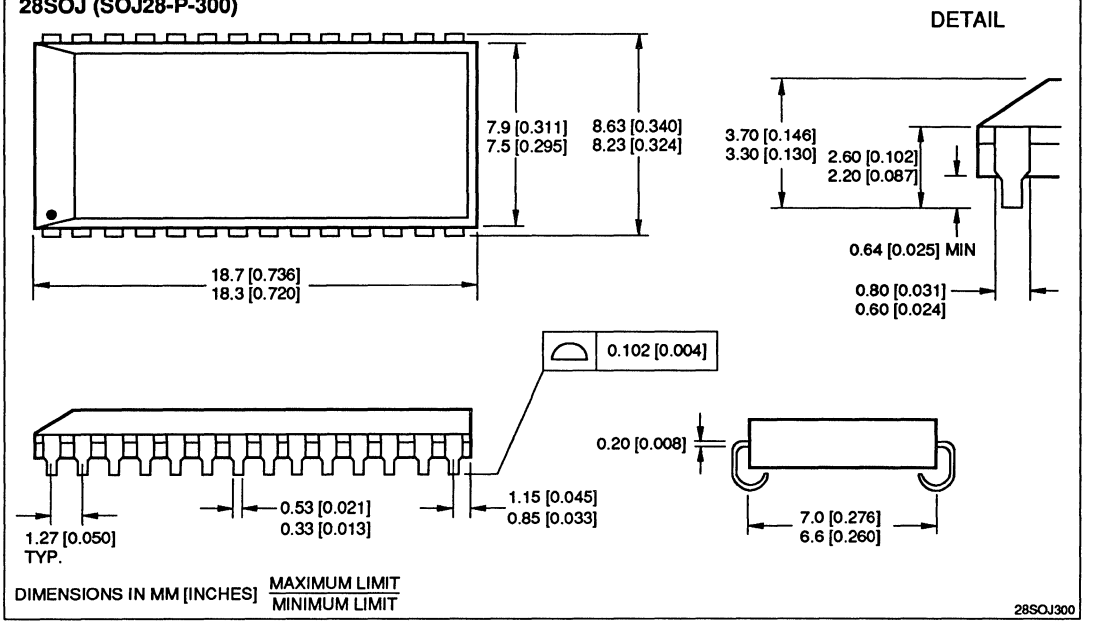
26SOJ (SOJ26-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

26SOJ

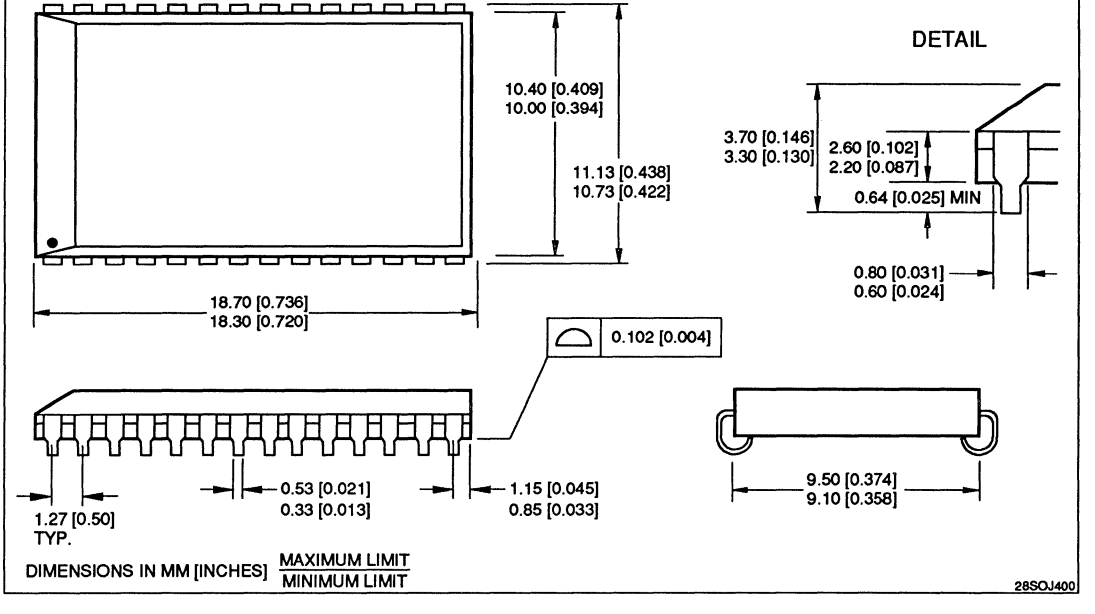
28SOJ (SOJ28-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOJ300

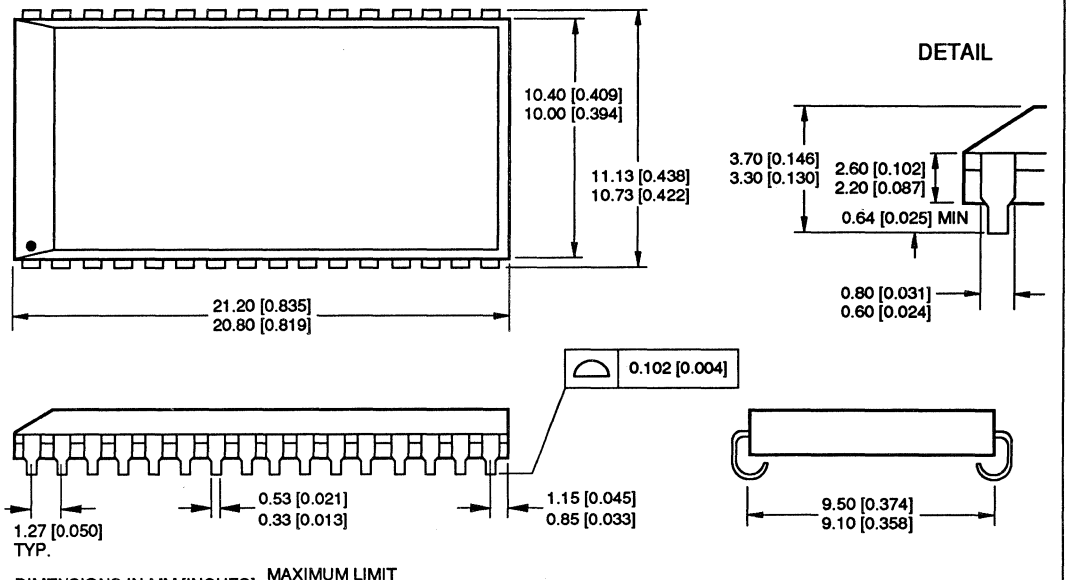
28SOJ (SOJ28-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOJ400

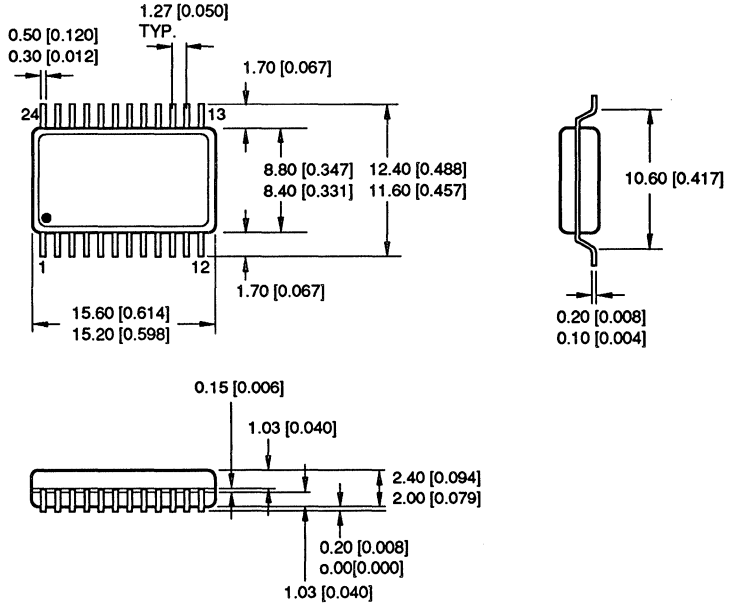
32SOJ (SOJ32-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32SOJ400

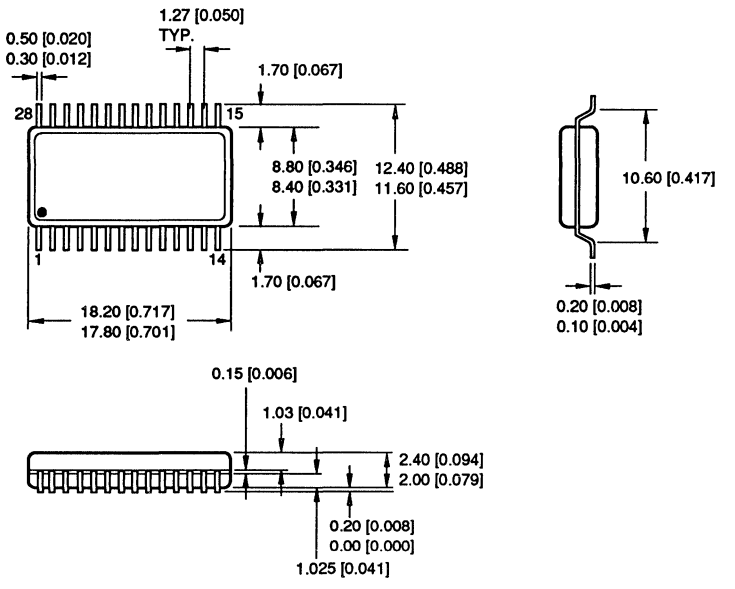
24SOP (SOP24-P-450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOP

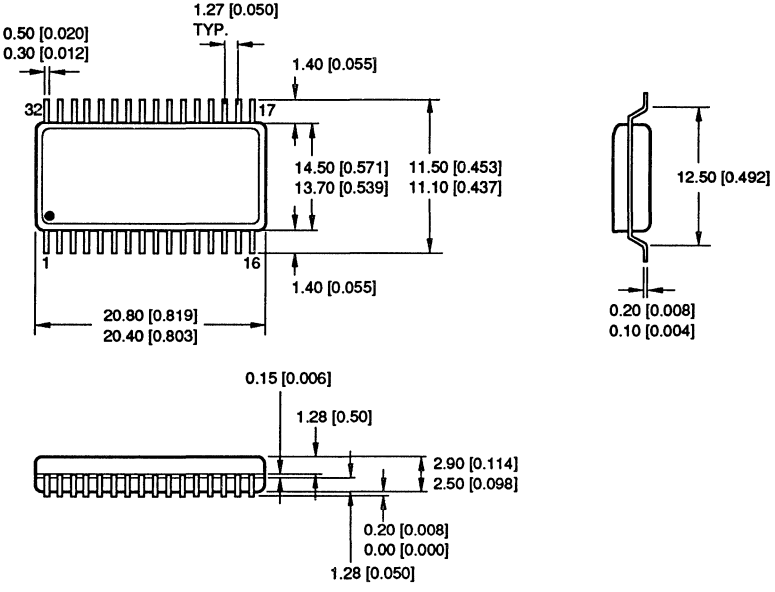
28SOP (SOP28-P-450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

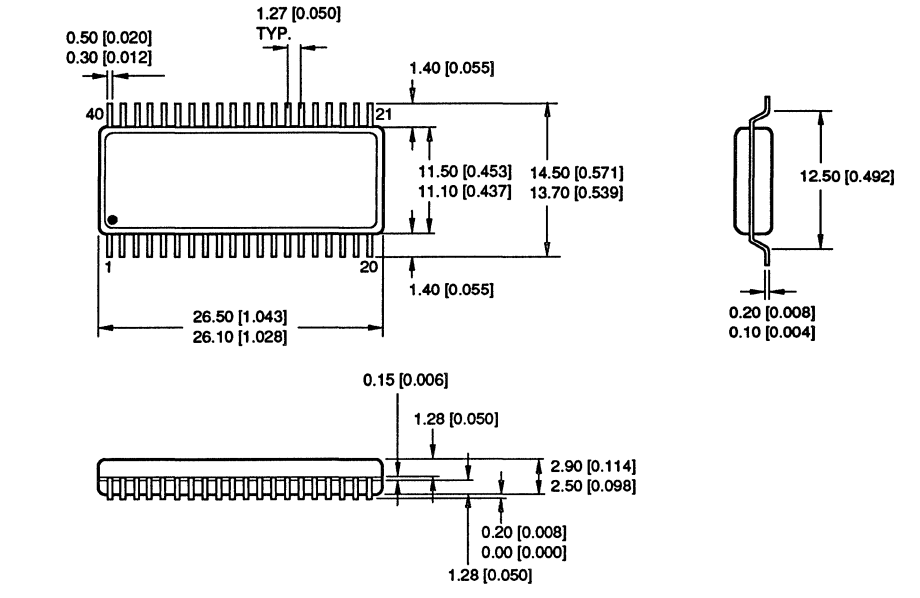
32SOP (SOP32-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32SOP

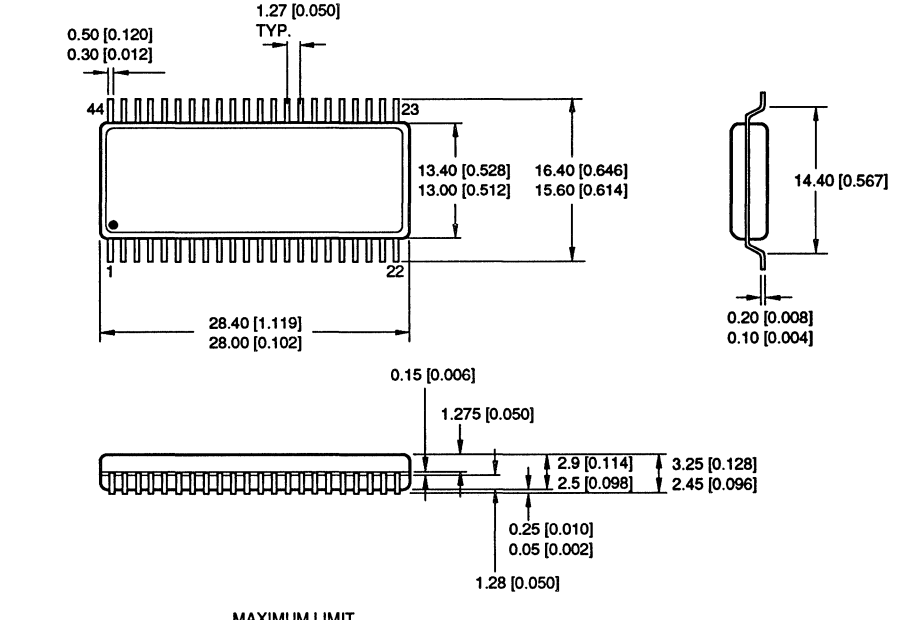
40SOP (SOP40-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40SOP

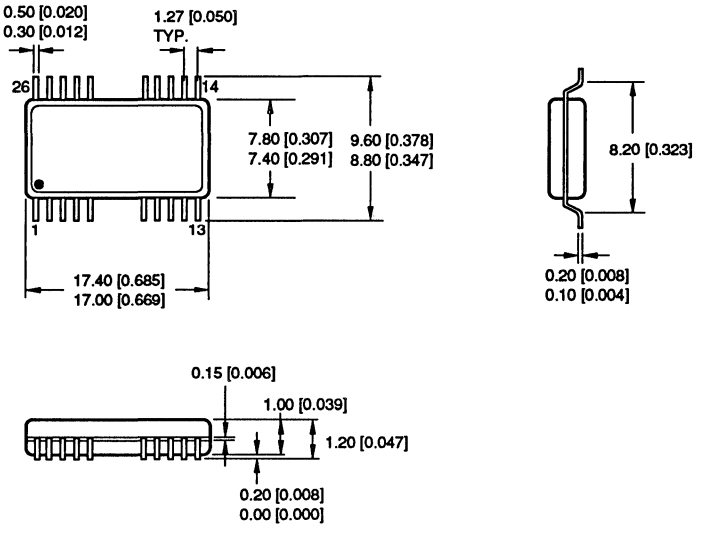
44SOP (SOP44-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44SOP

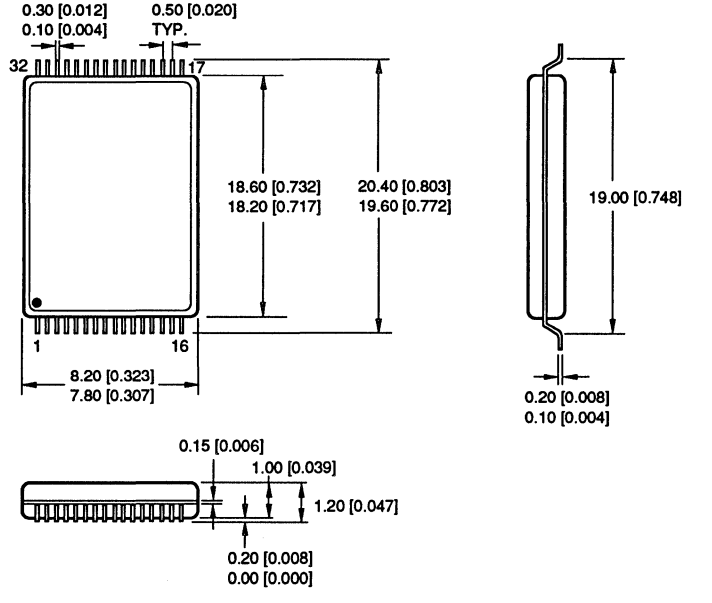
26TSOP (TSOP26-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

26TSOP

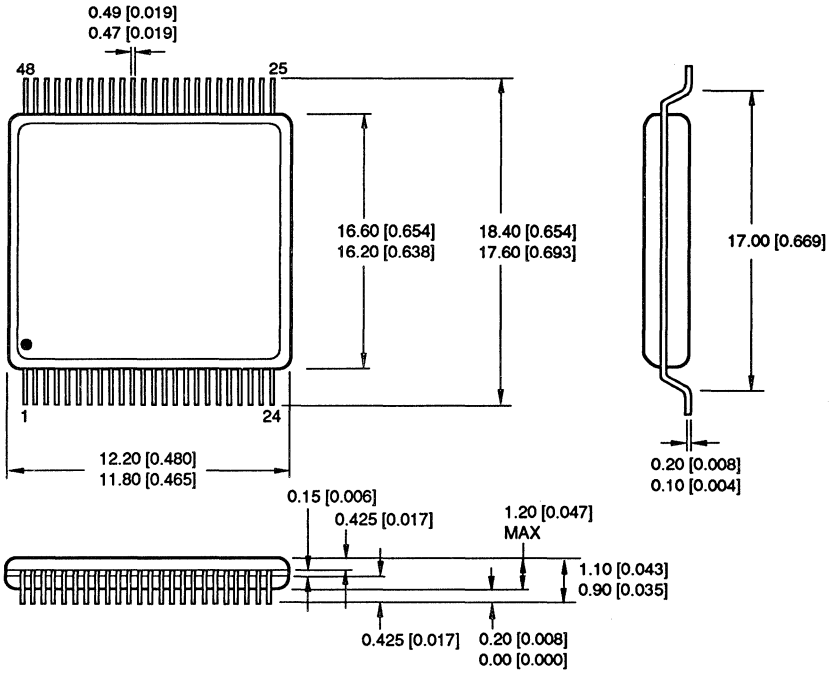
32TSOP (TSOP32-P-0820)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32TSOP

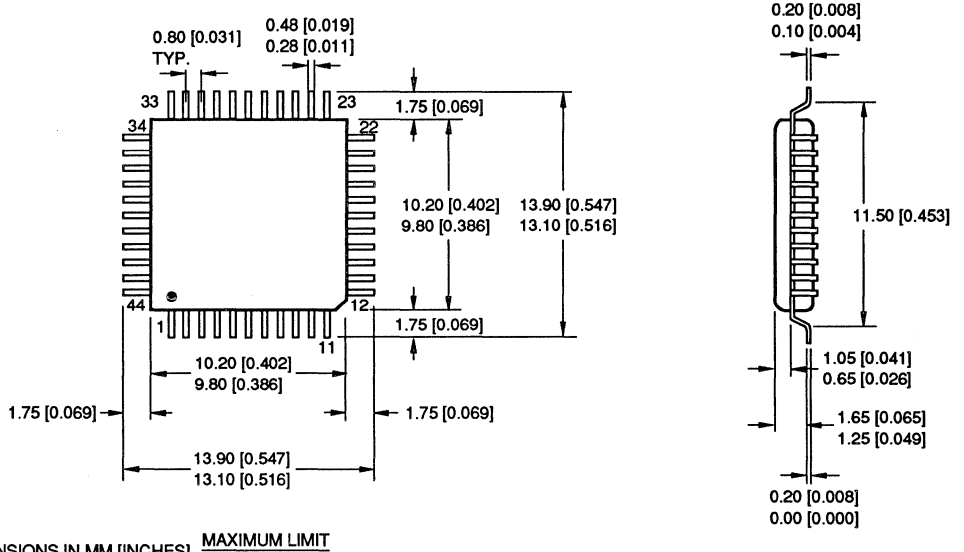
48TSOP (TSOP48-P-1218)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

48TSOP

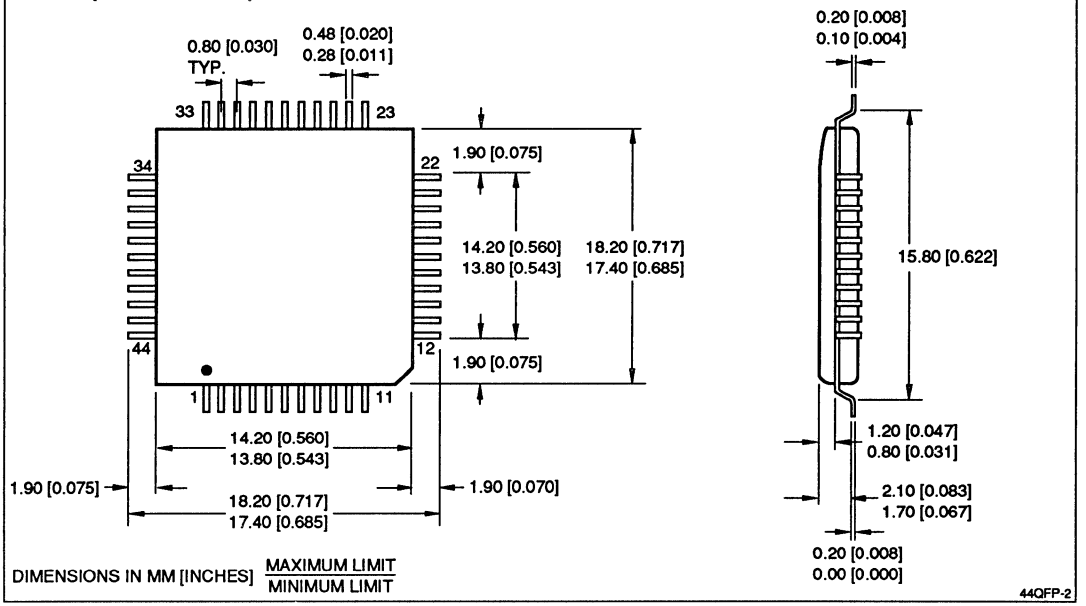
44QFP (QFP-44-P-1010)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44QFP-1

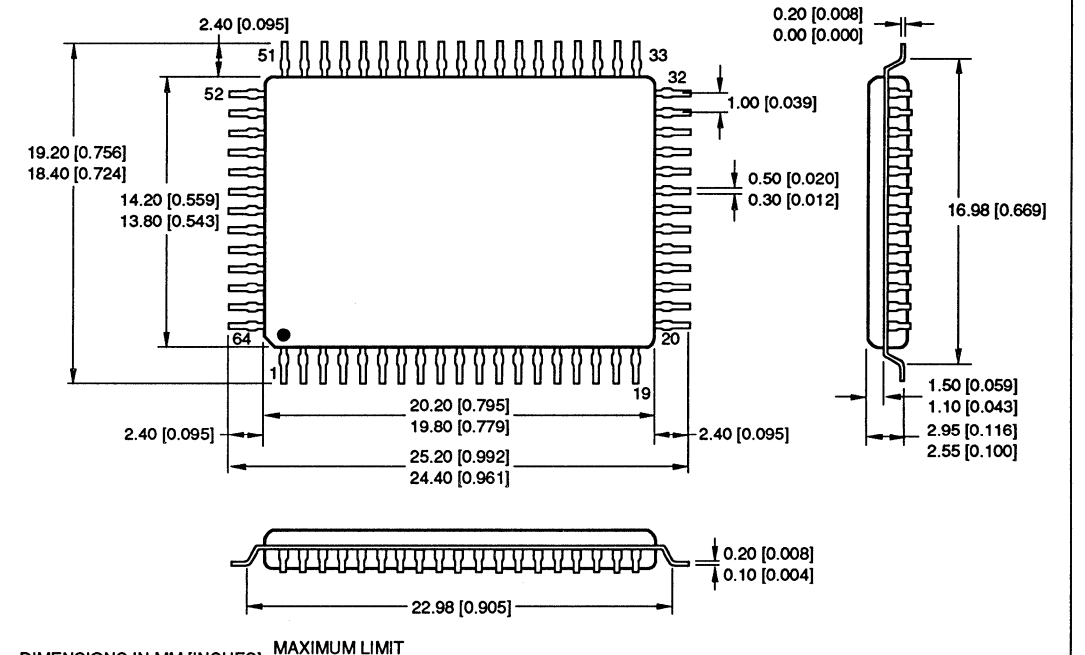
44QFP (QFP-44-P-1414)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44QFP-2

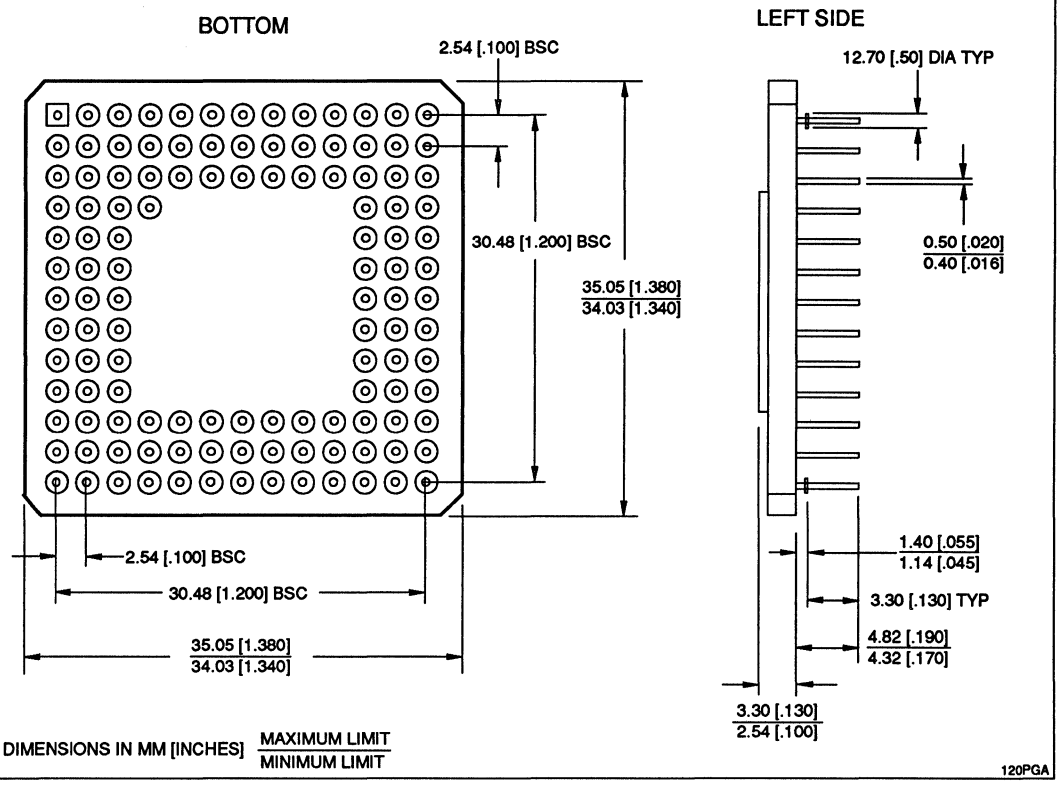
64QFP (QFP64-P-1420)



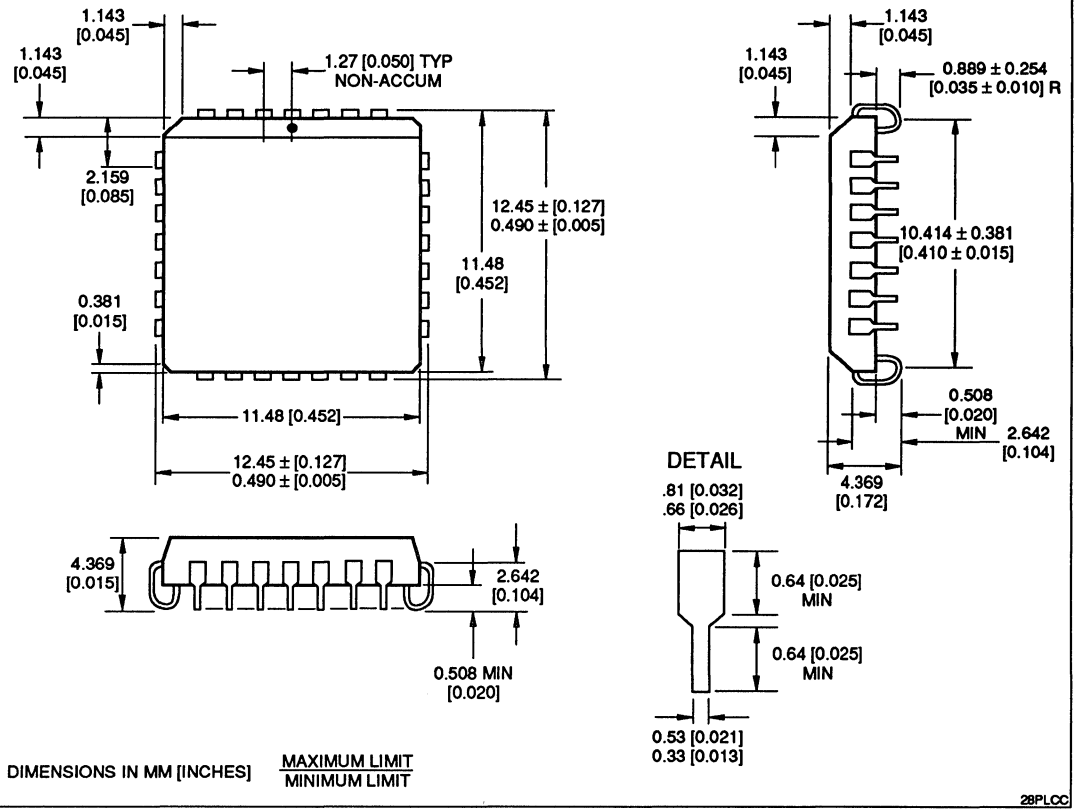
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

64QFP

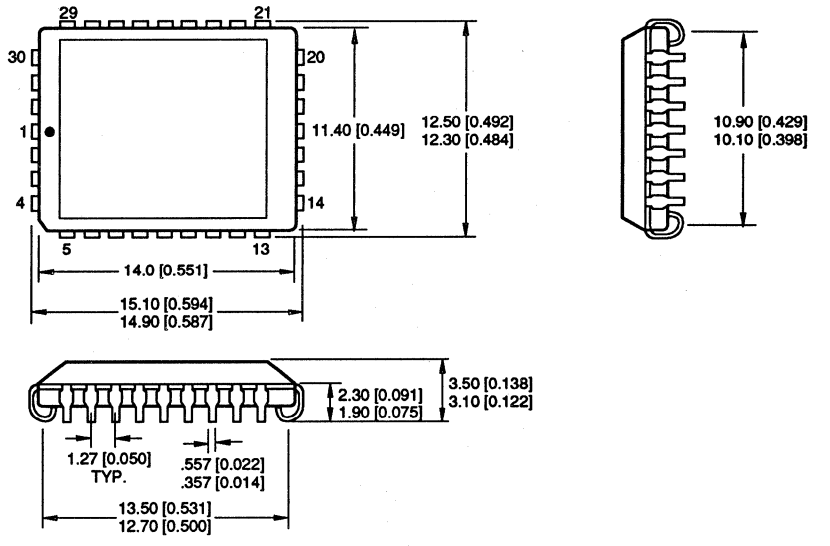
120PGA (PGA120-C-S1360)



28PLCC (PLCC28-P-S450)



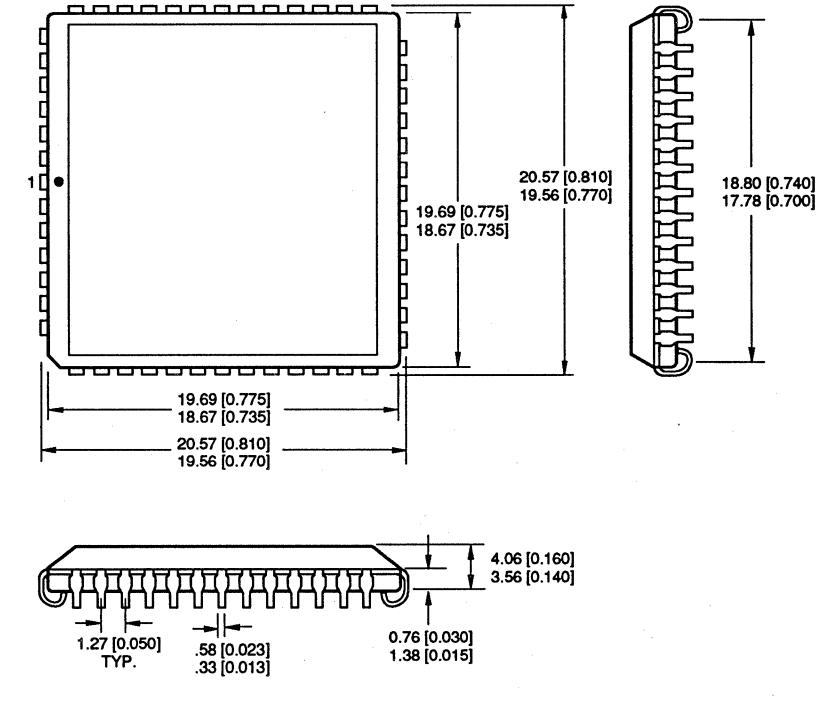
32PLCC (PLCC32-P-R450)



DIMENSIONS IN MM (INCHES) $\frac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

32PLCC

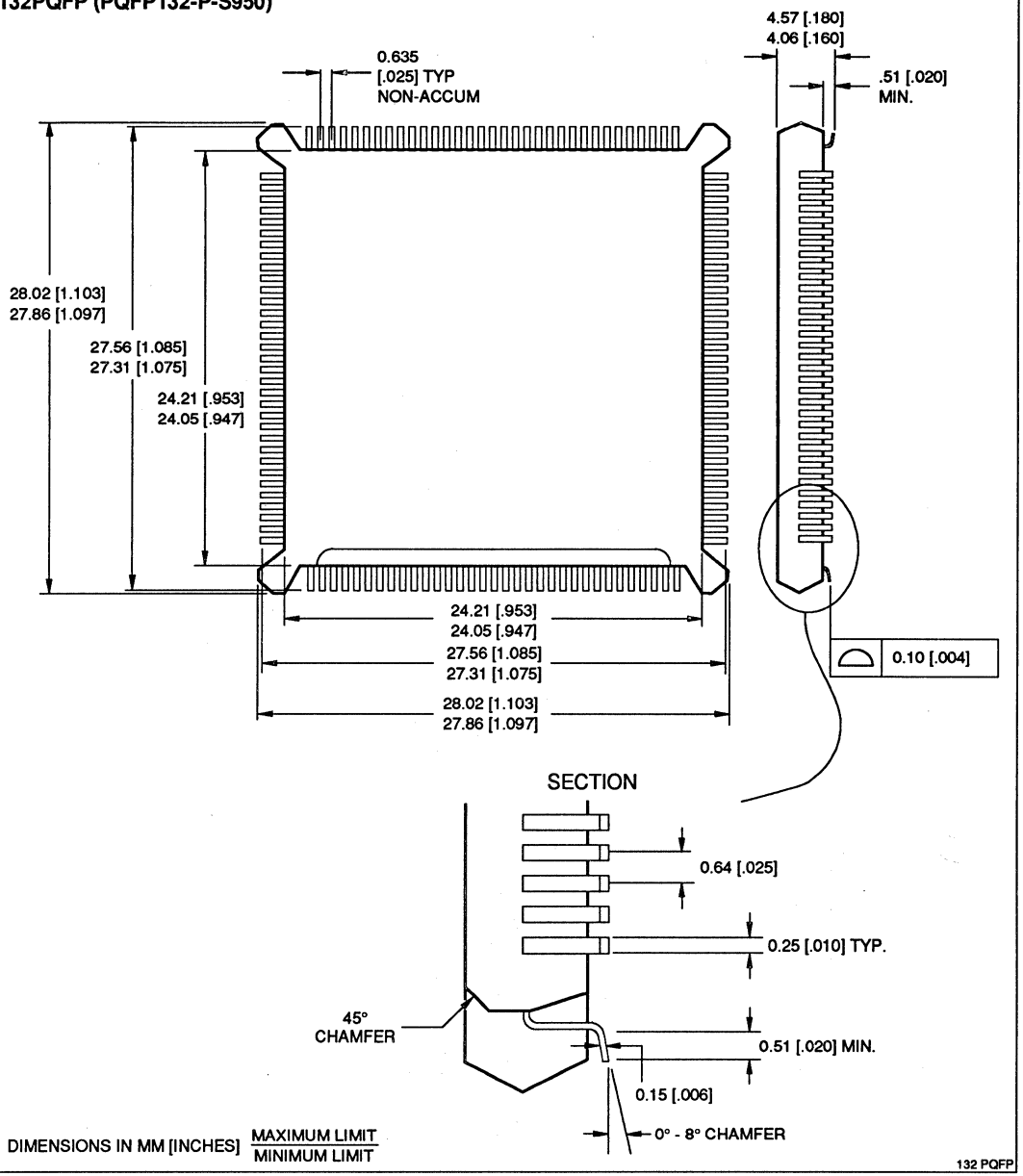
52PLCC (PLCC52-P-750)



DIMENSIONS IN MM (INCHES) $\frac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

52PLCC

132PQFP (PQFP132-P-S950)



SHARP

JAPAN

SHARP Corporation
IC Sales Department
International Sales & Marketing Group
IC/Electronic Components
2613-1 Ichinomoto-Cho
Tenri-City Nara 632, Japan
Phone: (07436) 5-1321
Telex: LABOMETA-B J63428
Facsimile: (07436) 5-1532

EUROPE

SHARP Electronics (Europe) GmbH
Microelectronics Division
Sonninstraße 3, 2000
Hamburg 1, F.R. Germany
Phone: (40) 23-775-216
Telex: 2161867 (HEEG D)
Facsimile: (40) 23-775-232

SINGAPORE

SHARP-ROXY Sales (Singapore) PTE. Ltd.
100G Pasir Panjang Road, Singapore 0511
Phone: 4731911
Telex: 55504 (SRSSIN RS)
Facsimile: 4794105

NORTH AMERICA

SHARP Electronics Corporation
Microelectronics Group
5700 Northwest Pacific Rim Blvd., M/S 20
Camas, Washington 98607, U.S.A.
Phone: (206) 834-2500
Telex: 49608472 (SHARPCAM)
Facsimile: (206) 834-8903

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division
Room 1701-1710, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: 8229311/8229348
Telex: 74258 SRHL HX
Facsimile: 5297561/8660779

KOREA

SHARP Electronics Industrial Corporation
4F, Dae San Bldg. 14-27 Yeoyido-dong.
Young Deung Po-ku, Seoul, Korea
Phone: 782-8637 ~ 40
Telex: SHARPEI K26754
Facsimile: (02) 782-5070

Reference No. WT255C