signetics

# DIGITAL
# 54/7400 TTL
# SUPPLEMENT

# TABLE OF CONTENTS

**The following is a parts list of Signetics Digital Product lines, now available, as described in the Utilogic II and MSI Handbooks.**

## UTILOGIC II/SP600 FAMILY LINE

**NOR Gates**

| | |
|---|---|
| 314A | Single 7-Input NOR Gate |
| 317A | Dual 4-Input Expandable NOR Gate |
| 370A | Triple 3-Input NOR Gate |
| 380A | Quad 2-Input NOR Gate |
| 381A | Quad 2-Input NOR Gate (Open-Collector) |

**OR Gates**

| | |
|---|---|
| 333A | Dual 3-Input Expandable OR Gate |
| 334A | Dual 4-Input Expandable OR Gate |
| 374A | Triple 3-Input OR Gate |
| 375A | Triple 2-Input Expandable OR Gate |
| 384A | Quad 2-Input OR Gate |

**AND Gates**

| | |
|---|---|
| 302A | Quad 2-Input AND Gate |
| 304A | Dual 4-Input AND Gate (Expandable) |
| 305A | Single 6-Input AND Gate |
| 306A | Single 6-Input AND Gate |
| 306A | Dual 3-Input AND Gate |

**NAND Gates**

| | |
|---|---|
| 337A | Dual 4-Input Expandable NAND Gate |
| 337A | Triple 3-Input NAND Gate |
| 387A | Quad 2-Input NAND Gate |
| 391A | Hex Inverter (Open Collector) |

**Gate Expanders**

| | |
|---|---|
| 300A | Dual 3-Input Expander for OR and NOR Gates |
| 301A | Quad 2-Input Diode Expander for NAND Gates |

**Buffer Drivers**

| | |
|---|---|
| 352A | Dual 3-Input Expandable NAND Buffer Driver (Open Collector) |
| 356A | Dual 4-Input Expandable NAND Buffer Driver |
| 357A | Quad 2-Input NAND Power Driver |
| 358A | Quad 2-Input NAND Power Driver (Open Collector) |

**Binaries**

| | |
|---|---|
| 321A | Dual J-K Binary |
| 322A | Dual J-K Binary |
| 328A | Dual D Binary |

**Pulse Shapers**

| | |
|---|---|
| 362A | Monostable Multivibrator |
| 363A | Dual Zero Crossing Detector |

**Shift Register**

| | |
|---|---|
| 3271B | 4-Bit Shift Register |

**Counters**

| | |
|---|---|
| 3280A | BCD Decade Counter |
| 3281A | 4-Bit Binary Counter |

**NAND Gates**

| | |
|---|---|
| 616A | Dual 4-Input Expandable NAND Gate |
| 670A | Triple 3-Input NAND Gate |
| 680A | Quad 2-Input NAND Gate |

**Buffer Driver**

| | |
|---|---|
| 659A | Dual 4-Input Buffer/Driver |

**J-K Binary**

| | |
|---|---|
| 620A | Single J-K Binary |

**RS/T Binary**

| | |
|---|---|
| 629A | Single RS/T Binary |

**Inverter**

| | |
|---|---|
| 690A | Hex Inverter |

**Expander**

| | |
|---|---|
| 631A | Gate Expander |

## MSI DIGITAL LINE

| | |
|---|---|
| 8200 | Dual 5-Bit Buffer Register – D Inputs |
| 8201 | Dual 5-Bit Buffer Register – D Inputs |
| 8202 | 10-Bit Buffer Register – D Inputs |
| 8203 | 10-Bit Buffer Register – D Inputs |
| 8220 | High Speed Content Addressable Memory Element (CAM) |
| 8224 | 256 Bit ROM, ASCII to EBCDIC Code Converter, Alphabet Only |
| 8225 | Signetics 64-Bit Bipolar Scratch Pad Memory |
| 8230 | 8-Input Digital Multiplexer |
| 8231 | 8-Input Digital Multiplexer |
| 8232 | 8-Input Digital Multiplexer |
| 8233 | 2-Input 4-Bit Digital Multiplexers |
| 8234 | 2-Input 4-Bit Digital Multiplexers |
| 8235 | 2-Input 4-Bit Digital Multiplexers |
| 8241 | Quad Exclusive-OR Element |
| 8242 | 4-Bit Digital Comparator (Quad Exclusive-NOR) |
| 8243 | 8-Bit Position Scaler |
| 8250 | Binary-to-Octal Decoder |
| 8251 | BCD-to-Decimal Decoder |
| 8260 | Arithmetic Logic Element |
| 8261 | Fast Carry Extender |
| 8262 | 9-Bit Parity Generator and Checker |
| 8263 | 3-Input, 4-Bit Digital Multiplexer |
| 8264 | 3-Input, 4-Bit Digital Multiplexer |
| 8266 | 2-Input, 4-Bit Digital Multiplexer |
| 8267 | 2-Input, 4-Bit Digital Multiplexer |
| 8268 | Gated Full Adder |
| 8270 | 4-Bit Shift Registers |
| 8271 | 4-Bit Shift Registers |
| 8275 | Quad Bistable Latch |
| 8276 | 8-Bit Shift Register |
| 8277 | Dual 8-Bit Shift Register |
| 8280 | BCD Decade Counter/Storage Element |
| 8281 | 4-Bit Binary Counter/Storage Element 8281 |
| 8284 | Binary Hexadecimal Synchronous Up/Down Counter |
| 8285 | BCD Decade Synchronous Up/Down Counter |
| 8288 | Divide-by-Twelve Counter/Storage Element |
| 8290 | Presettable High Speed Decade Counter |
| 8291 | Presettable High Speed Binary Counter |
| 8292 | Presettable Low Power Decade Counter |
| 8293 | Presettable Low Power Binary Counter |
| 8T01 | Nixie* Decoder/Driver |
| 8T04 | Seven Segment Decoder/Lamp Driver |
| 8T05 | Seven Segment Decoder/Transistor Driver |
| 8T06 | Seven Segment Decoder/Display Driver |
| 8T13 | Dual Line Driver |
| 8T14 | Triple Line Receiver |
| 8T15 | Dual Communications EIA/MIL Line Driver |
| 8T16 | Dual Communications EIA/MIL Line Receiver |

**To Be Announced 2nd Quarter**

| | |
|---|---|
| 8269 | 4-Bit Comparator |
| 8273 | 10-Bit Serial-In-Parallel-Out Shift Register |
| 8T09 | Quad Bus High-Speed Buffer Gate |
| 8T22 | Retriggerable One-Shot (Replacement for 9601) |

*A trademark of Burroughs Corporation

**The following is a parts list of Signetics 54/74 Products now available, as described in the 54/74 Handbook.**

### 54/74XX / 54/74HXX FAMILY LINES

| | |
|---|---|
| 54/7400 | Quadruple 2-Input Positive NAND Gate |
| 54/7401 | Quadruple 2-Input Positive NAND Gate (With open collector output) |
| 54/7402 | Quadruple 2-Input Positive NOR Gate |
| 54/7403 | Quadruple 2-Input Positive NAND Gate (With open collector output) |
| 54/7404 | Hex Inverter |
| 54/7405 | Hex Inverter (With open collector output) |
| 54/7408 | Quadruple 2-Input Positive AND Gates |
| 54/7410 | Triple 3-Input Positive NAND Gate |
| 54/7411 | Triple 3-Input Positive AND Gate |
| 54/7420 | Dual 4-Input Positive NAND Gate |
| 54/7421 | Dual 4-Input AND Gate |
| 54/7430 | 8-Input Positive NAND Gate |
| 54/7440 | Dual 4-Input Positive NAND Buffer |
| N7441 | BCD-to-Decimal Decoder/Driver |
| 54/7450 | Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate |
| 54/7451 | Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate |
| 54/7453 | 4-Wide 2-Input AND-OR-Invert Gate |
| 54/7454 | 4-Wide 2-Input AND-OR-Invert Gate |
| S5460 | Dual 4-Input Expander |
| N7460 | Dual 4-Input Expander |
| 54/7470 | J-K Flip-Flop |
| 54/7472 | J-K Master-Slave Flip-Flop |
| 54/7473 | Dual J-K Master-Slave Flip-Flop |
| 54/7474 | Dual D-Type Edge-Triggered Flip-Flop |
| 54/7475 | Quadruple Bistable Latch |
| 54/7476 | Dual J-K Master-Slave Flip-Flop with Preset and Clear |
| 54/7477 | Quadruple Bistable Latch |
| 54/7480 | Gated Full Adder |
| 54/7490 | Decade Counter |
| 54/7491 | 8-Bit Shift Register |
| 54/7492 | Divide-by-Twelve Counter(Divide-by-Two & Divide-by-Six) |
| 54/7493 | 4-Bit Binary Counter |
| 54/74107 | Dual J-K Master Slave Flip-Flop |
| 54/74H00 | Quadruple 2-Input Positive NAND Gate |
| 54/74H01 | Quadruple 2-Input Positive NAND Gate (With open collector output) |
| 54/74H04 | Hex Inverter |
| 54/74H05 | Hex Inverter (With open collector output) |
| 54/74H08 | Quadruple 2-Input Positive AND Gate |
| 54/74H10 | Triple 3-Input Positive NAND Gate |
| 54/74H11 | Triple 3-Input Positive AND Gate |
| 54/74H20 | Dual 4-Input Positive NAND Gate |
| 54/74H21 | Dual 4-Input Positive AND Gate |
| 54/74H22 | Dual 4-Input Positive NAND Gate (With open collector output) |
| 54/74H30 | 8-Input Positive NAND Gate |
| 54/74H40 | Dual 4-Input Positive NAND Buffers |
| 54/74H50 | Dual 2-Wide 2-Input AND-OR-Invert Gates |
| 54/74H51 | Dual 2-Wide 2-Input AND-OR-Invert Gates |
| 54/74H52 | 4-Wide 2-2-2-3-Input AND-OR-Gate |
| 54/74H53 | Expandable 2-2-2-3-Input AND-OR-Invert Gate |
| 54/74H54 | Expandable 2-2-2-3-Input AND-OR-Invert Gate |
| 54/74H55 | Expandable 4-Input AND-OR-Invert Gate |
| 54H60 | Dual 4-Input Expander (For use with S54H50, S54H53, S54H55 circuits) |
| 74H60 | Dual 4-Input Expander (For use with N74H50, N74H53, N74H55 circuits) |
| 54/74H61 | Triple 3-Input Expanders (For use with S54H52, N74H52 circuits) |
| S54H62 | 3-2-2-3-Input AND-OR Expander (For use with S54H50, S54H53, S54H55 circuits) |
| N74H62 | 3-2-2-3-Input AND-OR Expander (For use with N74H50, N74H53, N74H55 circuits) |
| 54/74H72 | J-K Master Slave Flip-Flops |
| 54/74H73 | Dual J-K-Master-Slave Flip-Flops |
| 54/74H74 | Dual D-Type Edge-Triggered Flip-Flops |
| 54/74H76 | Dual J-K Master-Slave Flip-Flops |

**To Be Announced**

| | |
|---|---|
| 74181 | 4-Bit Arithmetic Unit W/Full Look-Ahead |
| 74182 | Look-Ahead Carry Generator |
| 74157 | Quad 2-to-1 Line |
| 74166 | Parallel-In, Serial-Out, Synchronous Load Shift Register |
| 74198 | 8-Bit Shift Register Parallel-Access, Shift Right-Left |
| 74199 | 8-Bit Shift Register Parallel-Access J-K Inputs W/Mode Control |
| 74195 | 4-Bit Shift Register Parallel-Access J-K Inputs Mode Control |
| 74123 | Dual-Retriggerable Monostable Multivibrator W/Clear |
| 74153 | Data Selector/Multiplexer Dual 4-to-1 Line |
| 74H71 | J-K Master Slave Flip-Flop |

## GENERAL DESCRIPTION

**Series 54/74 Logic Family**

The 54/74XX logic family is medium speed TTL, and high speed TTL integrated circuits. The family includes a multiple number of functions in a variety of packages. The 54XX devices are characterized for the full military temperature range of -55°C to +125°C. The 74XX devices are characterized for the limited temperature range of 0° to +70° C.

## DESIGN CONSIDERATIONS

**Logic Definition**

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL "0"

HIGH VOLTAGE = LOGICAL "1"

**Unused Inputs**

For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4V but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package load, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to a supply voltage. Preferably, this voltage should be between 2.4V and 5.5V.

b. Connect unused inputs to a used input if maximum fanout of the driving output will not be exceeded. Each input presents a full load in the logical "1" state to the driving output.

**Input-Current Requirements**

Input-current requirements reflect worst-case $V_{cc}$ and temperature condition. Currents into the input terminals are specified as positive values.

**54/74 Logic**

Each input of the multiple-emitter input transistor that utilizes a 4 KΩ resistor requires no more than --1.6 mA flow out of the input at a logical "0" voltage level; therefore, one load (N = 1) for 54/74 logic is -1.6 mA maximum. Each input requires current into the input at a logical "1" voltage level. This current is 40μA maximum for each emitter input.

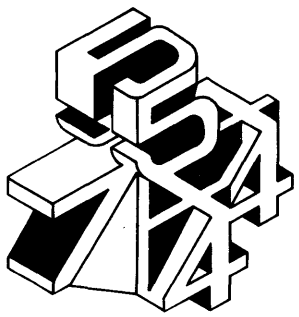
**Fanout Capability**

Fanout reflects the ability of an output to sink current from a number of loads (N) at a logical "0" voltage level and to supply current at a logical "1" voltage level. Each standard 54/74 output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate (54/7440) is capable of sinking current or supplying current to 30 loads (N = 30).

## ELECTRICAL CHARACTERISTICS

These are guaranteed over the applicable operating free-air temperature range, unless otherwise noted, as shown in Section 2 of the handbook.

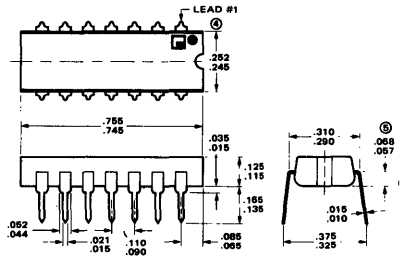
## GENERAL INFORMATION
## 54/74 LOGIC FAMILIES



# Section One

## PACKAGE TYPES

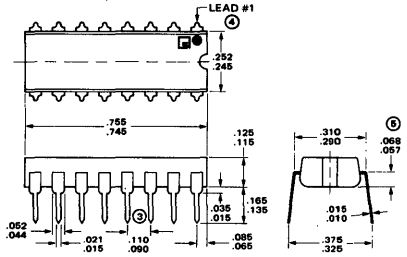
### A PACKAGE (TO-116)




NOTES:

1. Lead Material: Alloy 42 or equivalent
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash
7. Thermal resistance: $\theta J_A$ = .16°C/mW, $\theta J_C$ = .08°C/mW

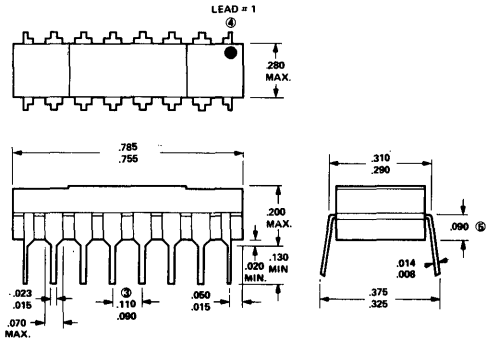
### B PACKAGE




NOTES:

1. Lead Material: Alloy 42 or equivalent
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash
7. Thermal resistance: $\theta J_A$ = .16°C/mW, $\theta J$ = .08°C/mW

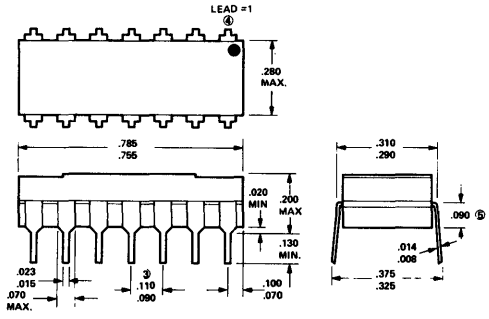
### E PACKAGE




NOTES:

1. Lead Material: Kovar or equivalent, tin plated
2. Body Material: Ceramic with glass seal
3. Tolerances non-cumulative
4. Signetics symbol denotes lead no. 1
5. Lead spacing shall be measured within this zone

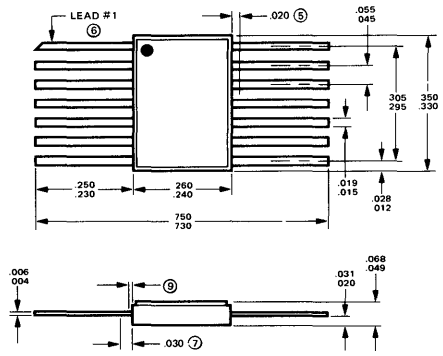
### F PACKAGE




NOTES:

1. Lead Material: Kovar or equivalent, tin plated
2. Body Material: Ceramic with glass seal
3. Tolerances non-cumulative
4. Signetics symbol denotes lead no. 1
5. Lead spacing shall be measured within this zone

## J PACKAGE (TO-88)




NOTES:

(1.) Recommended minimum offset before lead bend

2. Lead Material: Kovar or equivalent, gold plated
3. Body Material: Glass
4. Lid Material: Kovar, oxidized, glass seal

(5.) Tolerances non-cumulative

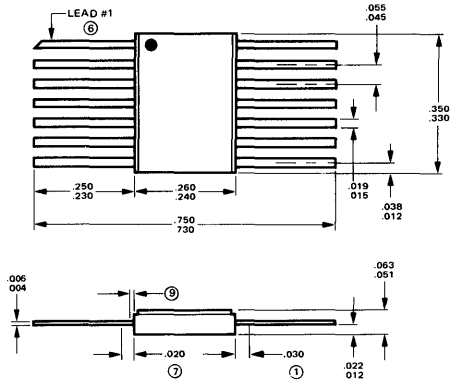
(6.) Signetics symbol or angle cut denotes Lead No. 1

(7.) Lead spacing shall be measured within this zone

8. Thermal Resistance: $\theta J_A$ = .300 °C/mW, $\theta J_C$ = .140°C/mW

(9.) Maximum glass climb: .010

## Q PACKAGE (TO-88)




NOTES:

1. Lead Material: Kovar or equivalent, gold plated
2. Body Material: Ceramic with glass seal at leads
3. Lid Material: Ceramic, glass seal

(4.) Tolerances non-cumulative

(5.) Lead spacing shall be measured within this zone

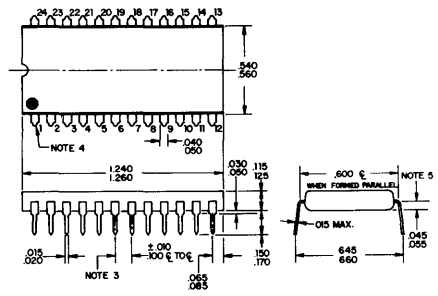
(6.) Signetics symbol or angle cut denotes Lead no. 1

(7.) Recommended minimum offset before lead bend

8. Thermal Resistance: $\theta J_A$ = .150°C/mW, $\theta J_C$ = .050 °C/mW

(9.) Maximum glass climb .010

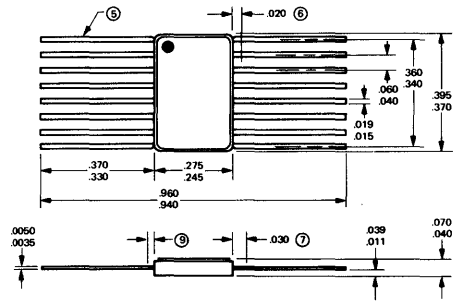
## N PACKAGE




NOTES:

1. Lead Material: Kovar, solder coated
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash

## R PACKAGE




NOTES:

1. Lead Material: Kovar or equivalent, gold plated
2. Body Material: Top ring and Base – Kovar or equivalent, gold plated, glass body
3. Lid Material: Kovar or equivalent, gold plated, alloy seal

(4.) Tolerances non-cumulative

(5.) Signetics symbol denotes Lead no. 1

(6.) Lead spacing shall be measured within this zone

(7.) Recommended minimum offset before lead bend

8. Thermal Resistance: $\theta J_A$ = .155 °C/mW, $\theta J_C$ = .070 °C/mW

(9.) Maximum glass climb: .010

**ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE–AIR TEMPERATURE RANGE (unless otherwise noted)**

| | | |
|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1) | | 7V |
| Input Voltage $V_{in}$ (See Note 1) | | 5.5V |
| Operating Free-Air Temperature Range: | Series 54 | –55°C to +125°C |
| | Series 74 | 0°C to +70°C |
| Storage Temperature Range | | –65°C to +150°C |

NOTE: 1. Voltage values are with respect to network ground terminal.

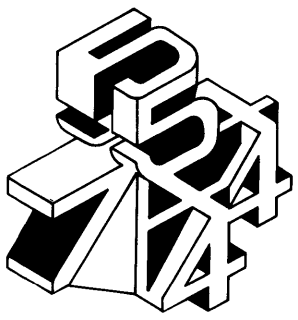
## ORDERING INSTRUCTIONS

| S54 | 40 | J |
|---|---|---|
| **TEMPERATURE RANGE*** | **PART IDENTIFICATION** | **PACKAGE*** |
| S54 = –55 °C to +125°C (Military Range)<br>N74 = 0°C to +70°C (Industrial Range) | Must contain two to four characters.<br>Examples:<br>00<br>H20<br>107 | "A" = 14-pin dual in-line silicone package (TO-116)<br>"B" = 16-pin dual in-line silicone package<br>"E" = 16 lead ceramic dual in-line<br>"F" = 14 lead ceramic dual in-line<br>"J" = 14-pin ceramic flat pak (TO-88)<br>"N" = 24 lead dual in-line<br>"Q" = 14-pin ceramic flat pak (TO-88)<br>"R" = 16 lead flat pak |

*Availability of a circuit device in a particular package and temperature range is indicated on the appropriate device. Electrical Characteristics Data Sheet is shown in Section 2 of this handbook.

Manufacturer reserves the right to make design and process changes and improvements.

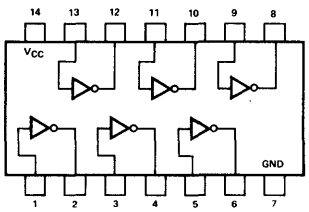
54/74XX
ELECTRICAL
CHARACTERISTICS



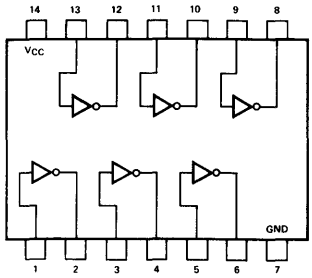
# Section Two

**N7406A,Q**
**S5406A,Q,F**
**N7416A,Q**
**S5416A,Q,F**

# Hex Inverter Buffer/Driver with Open Collector High Voltage Outputs




A,F PACKAGE

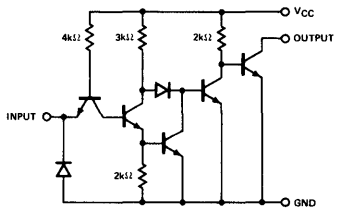



Q PACKAGE

## DESCRIPTION

The 54/7406 and 54/7416 Hex Inverter Buffer/Drivers feature standard TTL inputs with inverted high voltage, high current, open collector outputs for interface with MOS, lamps or relays. The 54/7406 minimum output breakdown is 30 volts and the 54/7416 minimum output breakdown is 15 volts.

## SCHEMATIC (each inverter)




Note: Component values shown are nominal

## RECOMMENDED OPERATING CONDITIONS.

| | | S5406, S5416 | | | N7406, N7416 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Output voltage, $V_{OH}$ | S5406, N7406 | | | 30 | | | 30 | V |
| | S5416, N7416 | | | 15 | | | 15 | |
| Low-level output current, $I_{OL}$ | | | | 30 | | | 40 | mA |
| Operating free-air temperature range, $T_A$ | | -55 | 25 | 125 | 0 | 25 | 70 | °C |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

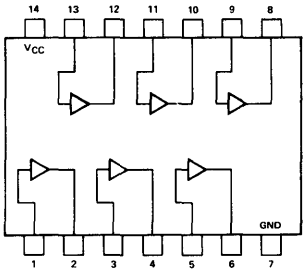
| PARAMETER | | | TEST CONDITIONS * | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = MIN, $V_I$ = 0.8V, $V_{OH}$ = MAX | | | 250 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_I$ = 2V, $I_{OL}$ = MAX | | | 0.7 | V |
| | | | $V_{CC}$ = MIN, $V_I$ = 2V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current (each input) | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current (each input) | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{CCH}$ | Supply current, high-level output | | $V_{CC}$ = MAX, $V_I$ = 0 | | 30 | 42 | mA |
| $I_{CCL}$ | Supply current, low-level output | | $V_{CC}$ = MAX, $V_I$ = 5V | | 27 | 38 | mA |

## SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25 °C

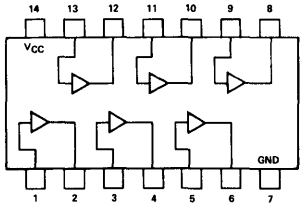
| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | | $C_L$ = 15pF, $R_L$ = 110Ω | | 10 | 15 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | $C_L$ 15pF, $R_L$ = 110Ω | | 14 | 23 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25 °C.




Q PACKAGE




A,F PACKAGE

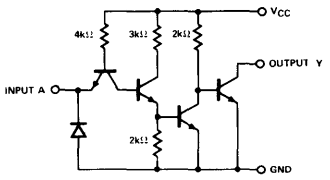
**Hex Buffer/Driver with Open Collector High Voltage Outputs**

**N7407A,Q S5407A,Q,F N7417A,Q S5417A,Q,F**

## DESCRIPTION

The 54/7407 and 54/7417 Hex Buffer/Driver features standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays. The 54/7407 minimum output is 30 volts and the 54/7417 minimum output is 15 volts.

## SCHEMATIC (each buffer/driver)




Note: Component values shown are nominal

## RECOMMENDED OPERATING CONDITIONS.

| | | S5407, S5417 | | | N7407, N7417 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Output voltage, $V_{OH}$ | S5407, N7407 | | | 30 | | | 30 | V |
| | S5417, N7417 | | | 15 | | | 15 | |
| Low-level output current, $I_{OL}$ | | | | 30 | | | 40 | mA |
| Operating free-air temperature range, $T_A$ | | -55 | 25 | 125 | 0 | 25 | 70 | °C |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = MIN, $V_I$ = 2V, $V_{OH}$ = MAX | | | 250 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_I$ = 0.8V, $I_{OL}$ = MAX | | | 0.7 | V |
| | | | $V_{CC}$ = MIN, $V_I$ = 0.8V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current (each input) | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current (each input) | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{CCH}$ | Supply current, high-level output | | $V_{CC}$ = MAX, $V_I$ = 5V | | 29 | 41 | mA |
| $I_{CCL}$ | Supply current, low-level output | | $V_{CC}$ = MAX, $V_I$ = 0 | | 21 | 30 | mA |

## SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C

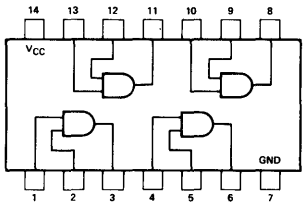
| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | | $C_L$ = 15pF, $R_L$ = 110Ω | | 6 | 10 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | $C_L$ = 15pF, $R_L$ = 110Ω | | 20 | 30 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

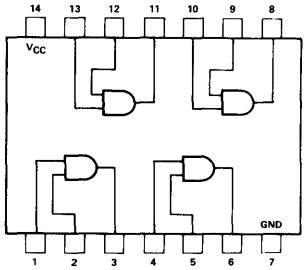
**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**N7409A,Q**
**S5409A,Q,F**

# Quad 2–Input AND Gate with Open Collector Outputs




A,F PACKAGE

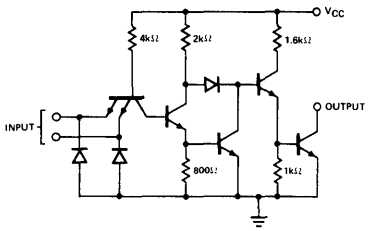



Q PACKAGE

## DESCRIPTION

The 54/7409 Quad 2-Input AND Gate with open collector outputs provides the capability of expanding AND logic functions.

## SCHEMATIC (each gate)




Note: Component values shown are nominal

## RECOMMENDED OPERATING CONDITIONS.

| | S5409 | | | N7409 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Normalized fan-out from each output, N | | | 10 | | | 10 | |
| Operating free-air temperature range, $T_A$ | -55 | 25 | 125 | 0 | 25 | 70 | °C |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

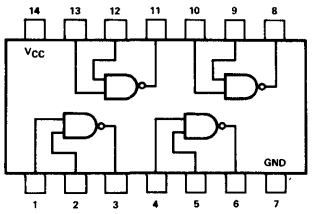
| PARAMETER | | | TEST CONDITIONS * | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{OH}$ = 5.5V | | | 250 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current (each input) | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current (each input) | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{CCH}$ | Supply current, high-level output | | $V_{CC}$ = MAX, $V_I$ = 5V | | 10 | 15 | mA |
| $I_{CCL}$ | Supply current, low-level output | | $V_{CC}$ = MAX, $V_I$ = 0 | | 18 | 26 | mA |

## SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | | $C_L$ = 15pF, | | 21 | 32 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | $R_L$ = 400Ω | | 16 | 24 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values at $V_{CC}$ = 5V, $T_A$ = 25°C.




A,F PACKAGE

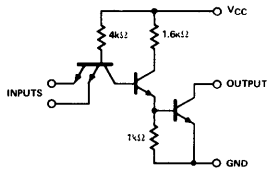
# Quad 2–Input High Voltage NAND Gate

**N7426A**
**S5426A,F**

## DESCRIPTION

The 54/7426 Quad 2-Input NAND Gate features standard TTL inputs with high voltage (15 volts) open collector outputs for interface with MOS, lamps or relays.

## SCHEMATIC (each gate)




Note: Component values shown are nominal

## RECOMMENDED OPERATING CONDITIONS.

| | S5426 | | | N7426 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Output voltage, $V_{OH}$ | | | 15 | | | 15 | V |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature range, $T_A$ | -55 | 25 | 125 | 0 | 25 | 70 | °C |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8V, $I_{OH}$ = 1mA | 15 | | | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8V, $V_{OH}$ = 12V | | | 50 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current (each input) | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current (each input) | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{CCH}$ | Supply current, high-level output | $V_{CC}$ = MAX, $V_I$ = 0 | | 4 | 8 | mA |
| $I_{CCL}$ | Supply current, low-level output | $V_{CC}$ = MAX, $V_I$ = 5V | | 12 | 22 | mA |

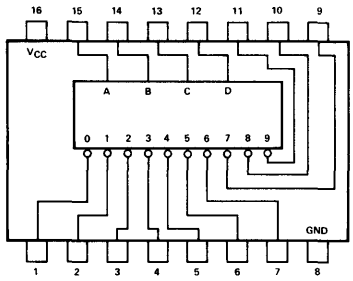
## SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15pF, $R_L$ = 1kΩ | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $C_L$ = 15pF, $R_L$ = 1kΩ | | 11 | 17 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**N7442B,R**
**S5442B,R,E** **BCD—to—Decimal Decoder**

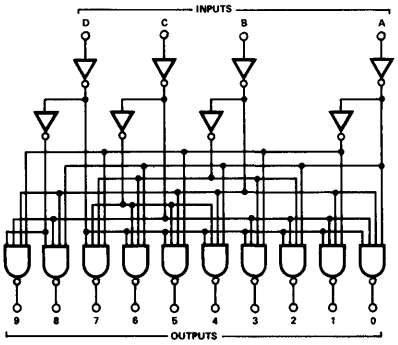



**B,E,R PACKAGE**

**DESCRIPTION**

The 54/7442 BCD-to-Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7442 decodes a four bit BCD number to one of ten outputs.

**LOGIC DIAGRAM**




**TRUTH TABLE**

| S5442/N7442 BCD INPUT | | | | ALL TYPES DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**RECOMMENDED OPERATING CONDITIONS.**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ | S5442, Circuits | 4.5 | 5 | 5.5 | V |
| | N7442, Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from each Output (N) | | | | 10 | |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input terminal | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -400μA | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | $V_{CC}$ = MAX, S5442 | -20 | | -55 | mA |
| | | $V_{CC}$ = MAX, N7442 | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, S5442 | | 28 | 41 | mA |
| | | $V_{CC}$ = MAX, N7442 | | 28 | 56 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

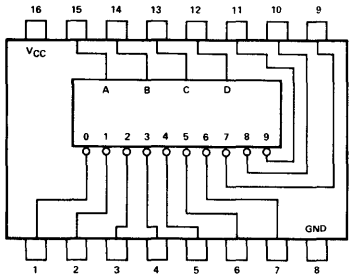
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd0}$ | Propagation delay time to logical 0 level through two logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | 22 | 30 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level through three logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | | 23 | 35 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level through two logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | 17 | 25 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level through | $C_L$ = 15pF, $R_L$ = 400Ω | | 26 | 35 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N7443B,R**
**S5443B,R,E** **Excess 3—to—Decimal Decoder**

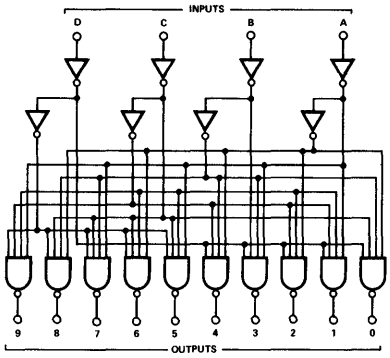



**B,E,R PACKAGE**

**DESCRIPTION**

The 54/7443 Excess 3 Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion application. The 54/7443 decodes excess 3 code numbers to one of ten outputs.

**LOGIC DIAGRAM**




**TRUTH TABLE**

| S5443/N7443 EXCESS INPUT | | | | ALL TYPES DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**RECOMMENDED OPERATING CONDITIONS.**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ | S5443, Circuits | 4.5 | 5 | 5.5 | V |
| | N7443, Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from each Output (N) | | | | 10 | |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input terminal | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -400μA | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | $V_{CC}$ = MAX, S5443 | -20 | | -55 | mA |
| | | $V_{CC}$ = MAX, N7443 | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, S5443 | | 28 | 41 | mA |
| | | $V_{CC}$ = MAX, N7443 | | 28 | 56 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

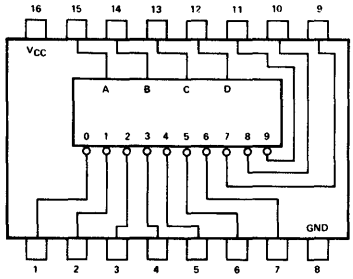
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd0}$ | Propagation delay time to logical 0 level through two logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | 22 | 30 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level through three logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | | 23 | 35 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level through two logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | 17 | 25 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level through | $C_L$ = 15pF, $R_L$ = 400Ω | | 26 | 35 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N7444B,R,E**
**S5444B,R Excess 3–Gray–to–Decimal Decoder**

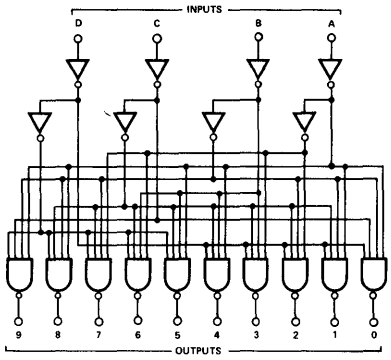



**B,E,R PACKAGE**

**DESCRIPTION**

The 54/7444 Excess-3-Gray Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7444 decodes excess three gray code to one of ten outputs.

**LOGIC DIAGRAM**




**TRUTH TABLE**

| S5444/N7444 EXCESS 3 GRAY INPUT | | | | ALL TYPES DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**RECOMMENDED OPERATING CONDITIONS.**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ | S5444, Circuits | 4.5 | 5 | 5.5 | V |
| | N7444, Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from each Output (N) | | | | 10 | |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input terminal | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -400μA | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | $V_{CC}$ = MAX, S5444 | -20 | | -55 | mA |
| | | $V_{CC}$ = MAX, N7444 | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, S5444 | | 28 | 41 | mA |
| | | $V_{CC}$ = MAX, N7444 | | 28 | 56 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

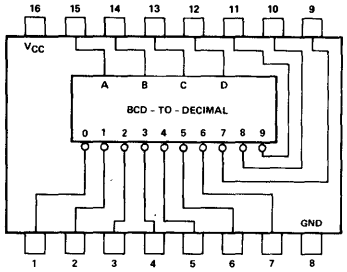
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd0}$ | Propagation delay time to logical 0 level through two logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | 22 | 30 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level through three logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | | 23 | 35 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level through two logic levels | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | 17 | 25 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level through | $C_L$ = 15pF, $R_L$ = 400Ω | | 26 | 35 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N7445B,R**
**S5445R,E** **BCD—to—Decimal Decoder/Driver**
**N74145B,R** **with Open Collector**
**S54145R,E** **High Voltage Outputs**

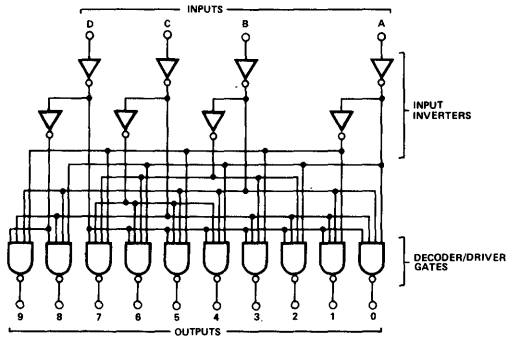



**B,E,R PACKAGE**

**DESCRIPTION**

The 54/7445 and 54/74145 BCD-to-Decimal Decoder/Driver is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The 54/7445 minimum output breakdown is 30 volts and the 54/74145 minimum output breakdown is 15 volts.

**LOGIC DIAGRAM**




**TRUTH TABLE**

| INPUTS | | | | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTE: 1. These voltage values are with respect to network ground terminal.

**RECOMMENDED OPERATING CONDITIONS.**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S5445, S54145 Circuits | 4.5 | 5 | 5.5 | V |
| | N7445, N74145 Circuits | 4.75 | 5 | 5.25 | V |
| Voltage on any Output | S5445, N7445 Circuits | | | 30 | V |
| | S54145, N74145 Circuits | | | 15 | V |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{in}$ (1) | Input voltage required to ensure logical 1 at any input terminal | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in}$ (0) | Input voltage required to ensure logical 0 at any input terminal | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{on}$ | On-state output voltage | $V_{CC}$ = MIN, $I_{sink}$ = 80mA | | 0.5 | 0.9 | V |
| | | $V_{CC}$ = MIN, $I_{sink}$ = 20mA | | | 0.4 | V |
| $V_{off}$ | Off-state output voltage (S5445 or N7445) | $V_{CC}$ = MAX, $I_{off}$ = 250μA | 30 | | | V |
| $V_{off}$ | Off-state output voltage (S54145 or N74145) | $V_{CC}$ = MAX, $I_{off}$ = 250μA | 15 | | | V |
| $I_{in}$ (1) | Logical 1 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in}$ (0) | Logical 0 level input current (each input) | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX S5445, S54145 | | 43 | 62 | mA |
| | | $V_{CC}$ = MAX N7445, N74145 | | 43 | 70 | mA |

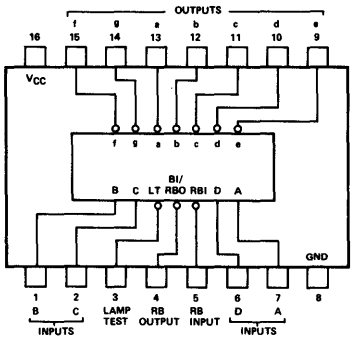
**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C,**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd1}$ | Propagation delay time logical 1 level | $C_L$ = 15pF, $R_L$ = 100Ω | | | 60 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level | $C_L$ = 15pF, $R_L$ = 100Ω | | | 60 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**N7446B** **BCD–to–Seven Segment**
**N7447B** **Decoder/Driver**




**B PACKAGE**

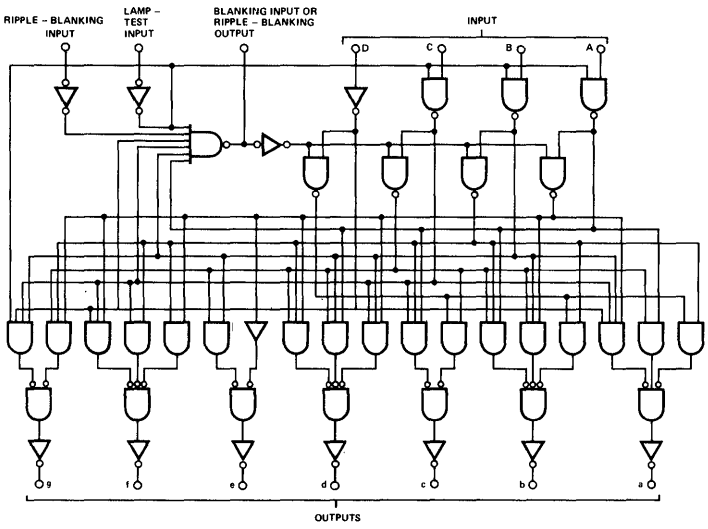
## DESCRIPTION

The 7446 and 7447 BCD-to-Seven Segment Decoder/Driver are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

The 7446 and 7447 provide bare collector output transistors for directly driving lamps. The output transistor breakdown of the 7446 is 30 volts and the 7447 is 15 volts.

## LOGIC DIAGRAM



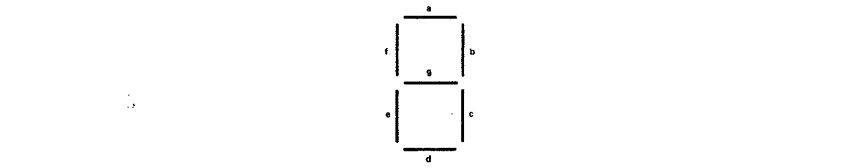

## TRUTH TABLE

| | INPUTS | | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DECIMAL OR FUNCTION | LT | RBI | D | C | B | A | BI/RBO | a | b | c | d | e | f | g | NOTE |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| BI | X | X | X | X | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3 |
| LT | 0 | X | X | X | X | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 |

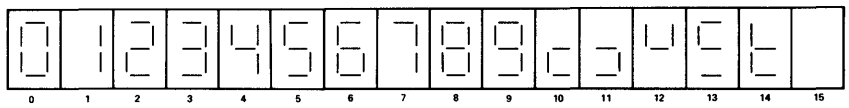
NOTES:

1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs to to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

## SEGMENT IDENTIFICATION




SEGMENT IDENTIFICATION




NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

## RECOMMENDED OPERATING CONDITIONS.

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (see Note 1): | | | | |
| N7446, N7447 Circuits | 4.75 | 5 | 5.25 | V |
| Continuous Voltage at Outputs a through g: | | | | |
| N7446 Circuits | | | 30 | V |
| N7447 Circuits | | | 15 | V |
| Normalized Fan-Out From Outputs a through g to Series 54/74 loads: | | | | |
| N7446, N7447 Circuits | | | 12 | |
| Normalized Fan-Out From BI/RBO Node to Series 54/74 loads: | | | | |
| N7446, N7447 Circuits | | | 5 | |
| Output Sink Current, $I_{sink}$: | | | | |
| N7446, N7447 Outputs a through g | | | 20 | mA |
| N7446, N7447, BI/RBO Node | | | 8 | mA |

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input | | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in(0)}$ | Input voltage reguired to ensure logical 0 at any input | | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{on}$ | On-state output voltage at outputs a through g | | $V_{CC}$ = MIN, $I_{sink}$ = 20mA | | 0.27 | 0.4 | V |
| $V_{out}$ (0) | Logical 0 output voltage at BI/RBO node | | $V_{CC}$ = MIN, $I_{sink}$ = 8mA | | 0.3 | 0.4 | V |
| $V_{off}$ | Off-state output voltage at outputs a through g (S5446 and N7446 only) | | $V_{CC}$ = MAX, $I_{off}$ = 250μA | 30 | | | V |

**ELECTRICAL CHARACTERISTICS (Cont'd)**

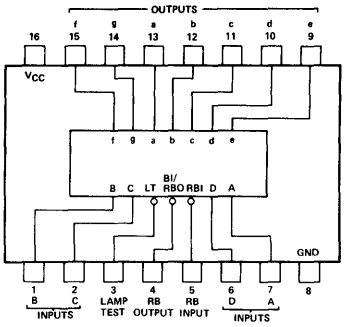
| PARAMETER | | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{off}$ | Off-state output voltage at outputs a through g (S5447 and N7447 only) | | $V_{CC}$ = MAX, $I_{off}$ = 250μA | 15 | | | V |
| $V_{out}$ (1) | Logical 1 output voltage at BI/RBO node | | $V_{CC}$ = MIN, $I_{load}$ = -200μA | 2.4 | 3.7 | | V |
| $I_{in(0)}$ | Logical 0 level input current at any input except BI/RBO node | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at BI/RBO node | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -4.2 | mA |
| $I_{in(1)}$ | Logical 1 level input current at any input except BI/RBO node | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V<br>$V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 40<br>1 | μA<br>mA |
| $I_{OS}$ | Short-circuit output current at BI/RBO node | | $V_{CC}$ = MAX | | | -4 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX N7446, N7447 | | 53 | 90 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25 °C,**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | Propagation delay time to logical 1 level from A input to any output | | $C_L$ = 15pF, $R_L$ = 280Ω | | | 100 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from A input to any output | | $C_L$ = 15pF, $R_L$ = 280Ω | | | 100 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level from RBI input to any output | | $C_L$ = 15pF, $R_L$ = 280Ω | | | 100 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from RBI input to any output | | $C_L$ = 15pF, $R_L$ = 280Ω | | | 100 | ns |

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.




**B PACKAGE**

**BCD–to–Seven Segment Decoder/Driver** **N7448B**

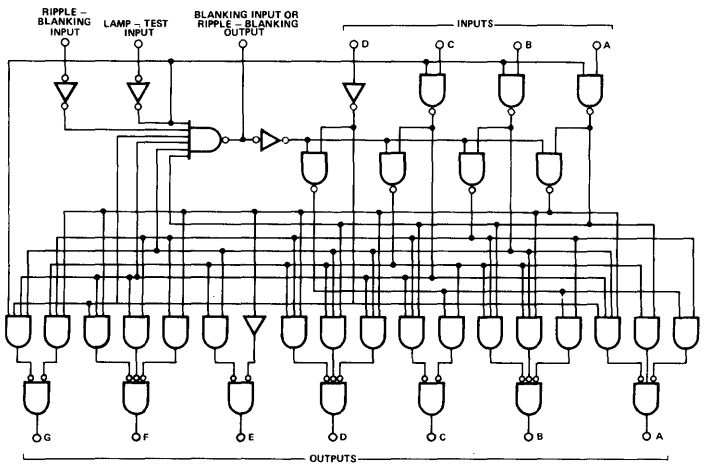
## DESCRIPTION

The 7448 BCD-to-Seven Segment Decoder/Driver is a TTL monolithic device consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

The 7448 has resistor pull up on the outputs to provide source current to drive interface elements.

## LOGIC DIAGRAM



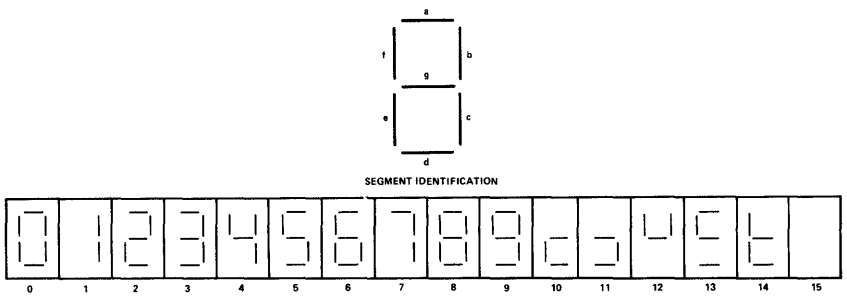

## TRUTH TABLE

| | INPUTS | | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DECIMAL OR FUNCTION | LT | RBI | D | C | B | A | BI/RBO | a | b | c | d | e | f | g | NOTE |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | X | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 1 | X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 3 | 1 | X | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 4 | 1 | X | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 5 | 1 | X | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | |
| 6 | 1 | X | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | |
| 7 | 1 | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 8 | 1 | X | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 9 | 1 | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | |
| 10 | 1 | X | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | |
| 11 | 1 | X | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | |
| 12 | 1 | X | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | |
| 13 | 1 | X | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| 14 | 1 | X | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 15 | 1 | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| BI | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| RBI | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 |
| LT | 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4 |

NOTES:

1. BI/RBO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 output. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0, and A = B = C = D = logical 0, all segment outputs go to a logical 0 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 1.

**SEGMENT IDENTIFICATION**




SEGMENT IDENTIFICATION

NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

**RECOMMENDED OPERATING CONDITIONS.**

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | | | | |
| N7448 Circuit | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out From Outputs a through g to Series 54/74 Loads: | | | | |
| N7448 Circuits | | | 4 | |
| Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads: | | | | |
| N7448 Circuits | | | 5 | |
| Output Sink Current, $I_{sink}$: | | | | |
| N7448 Outputs a through g | | | 6.4 | mA |
| N7448 BI/RBO Node | | | 8 | mA |

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input | | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input | | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out}$ (0) | Logical 0 output voltage at any output | | $V_{CC}$ = MIN, $I_{sink}$ = MAX | | 0.27 | 0.4 | V |
| $V_{out}$ (1) | Logical 1 level output voltage at outputs a through g | | $V_{CC}$ = MIN, $I_{load}$ = -400μA | 2.4 | 4.2 | | V |
| $V_{out}$ (1) | Logical 1 level output at BI/BRO node | | $V_{CC}$ = MIN, $I_{load}$ = -200μA | 2.4 | 3.7 | | V |

**ELECTRICAL CHARACTERISTICS (Cont'd)**

| PARAMETER | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{load}$ | Load current available at outputs a through g | $V_{CC}$ = MIN, $V_{out}$ = 0.85V | -1.3 | -2 | | mA |
| $I_{in(0)}$ | Logical 0 level input current of any input except BI/RBO node. | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at BI/RBO node | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -4.2 | mA |
| $I_{in(1)}$ | Logical 1 level input current at any input except BI/RBO node | $V_{CC}$ = MAX, $V_{in}$ = 2.4V<br>$V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 40<br>1 | μA<br>mA |
| $I_{OS}$ | Short-circuit output current at any output | $V_{CC}$ = MAX | | | - 4 | mA |
| $I_{CC}$ | Supply current | S5448<br>N7448 | | 53<br>53 | 76<br>90 | mA<br>mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C,**

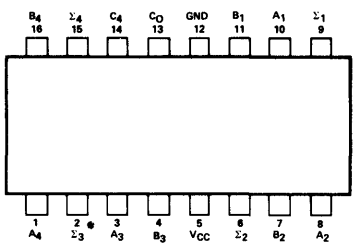
| PARAMETER | | TEST CONDITIONS * | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd1}$ | Propagation delay time to logical 1 level from A input to any output | $C_L$ = 15pF | | | 100 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from A input to any output | $C_L$ = 15pF | | | 100 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level from RBI input to any output | $C_L$ = 15pF | | | 100 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from RBI Input to any output | $C_L$ = 15pF | | | 100 | ns |

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

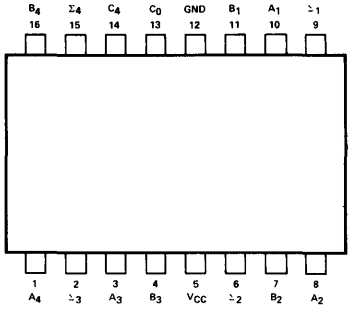
** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**N7483B,R**
**S5483R,E**

# 4–Bit Binary Full Adder (look Ahead Carry)




B,E PACKAGE




R PACKAGE

## DESCRIPTION

The 54/7483 is a 4-Bit Binary Full Adder for adding two four bit binary numbers. A Carry Look Ahead circuit is included to provide minimum carry propagation delays.

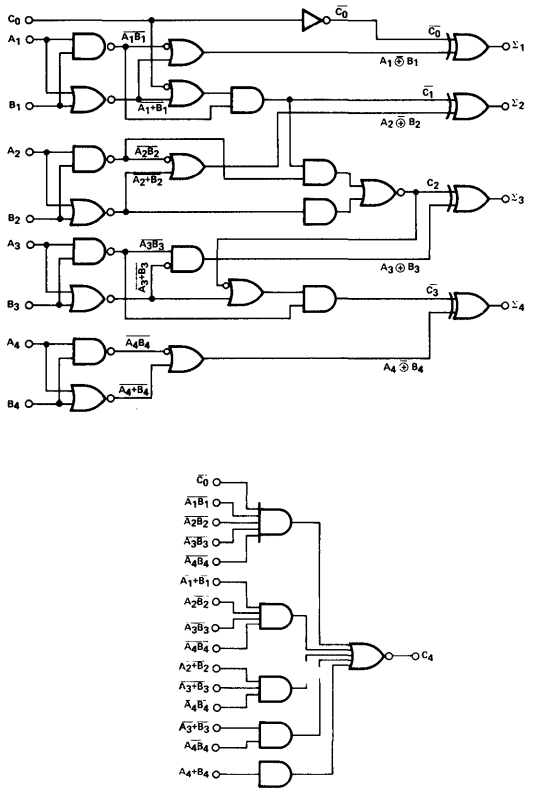
Propagation delays of carry-in to carry-out is typically 12nsec.

## TRUTH TABLE

| INPUT | | | | | | OUTPUT | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | WHEN $C_0 = 0$ | | | WHEN $C_0 = 1$ | | |
| | | | | WHEN $C_2 = 0$ | | | WHEN $C_2 = 1$ | | |
| $A_1$ / $A_3$ | $B_1$ / $B_3$ | $A_2$ / $A_4$ | $B_2$ / $B_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ | $\Sigma_1$ / $\Sigma_3$ | $\Sigma_2$ / $\Sigma_4$ | $C_2$ / $C_4$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

NOTE:
Input conditions at $A_1$, $A_2$, $B_1$, $B_2$, and $C_0$ are used to determine outputs $\Sigma_1$ and $\Sigma_2$, and the value of the internal carry $C_2$. The values at $C_2$, $A_3$, $B_3$, $A_4$, and $B_4$, are then used to determine outputs $\Sigma_3$, $\Sigma_4$, and $C_4$.

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$: (See Note 1) | S5483 Circuits | 4.5 | 5 | 5.5 | V |
| | N7483 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out From Outputs: | | | | | |
| $C_4$ | | | | 5 | |
| $\Sigma_1$, $\Sigma_2$, $\Sigma_3$ or $\Sigma_4$ | | | | 10 | |

NOTE: 1. These voltage values are with respect to network ground terminal.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

† Not more than one output should be shorted at a time.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS * | | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | $V_{CC}$ = MIN | | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 1 at any input terminal | $V_{CC}$ = MIN | | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN | | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN | | | | 0.4 | V |
| $I_{in(0)}$ | Logical 0 level input current at $A_1$, $A_3$. $B_1$, $B_3$, or $C_0$ | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -3.2 | mA |
| $I_{in(0)}$ | Logical 0 level input current at $A_2$, $A_4$, $B_2$, or $B_4$ | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{in(1)}$ | Logical 1 level input current $A_1$, $A_3$, $B_1$, $B_3$, or $C_0$ | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 80 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(1)}$ | Logical 1 level input current $A_2$, $A_4$, $B_2$, or $B_4$ | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 40 | μA |
| | | $V_{CC}$ @ MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{OS}$ | Short-circuit output current at $\Sigma_1$, $\Sigma_2$, $\Sigma_3$, or $\Sigma_4$ † | $V_{CC}$ = MAX | S5483 | -20 | | -55 | mA |
| | | | N7483 | -18 | | -55 | mA |
| $I_{OS}$ | Short-circuit output current at $C_4$ † | $V_{CC}$ = MAX | S5483 | -20 | | -70 | mA |
| | | | N7483 | -18 | | -70 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = MAX, | | | 58 | 79 | mA |

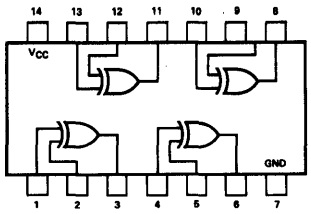
**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, unless otherwise noted N = 10**

| PARAMETER ‡ | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd1}$ | From $C_0$ to 1 | $C_L$ = 50pF, $R_L$ = 400Ω | | 23 | 34 | ns |
| $t_{pd0}$ | From $C_0$ to 1 | $C_L$ = 50pF, $R_L$ = 400Ω | | 20 | 34 | ns |
| $t_{pd1}$ | From $C_0$ to 2 | $C_L$ = 50pF, $R_L$ = 400Ω | | 24 | 35 | ns |
| $t_{pd0}$ | From $C_0$ to 2 | $C_L$ = 50pF, $R_L$ = 400Ω | | 22 | 35 | ns |
| $t_{pd1}$ | From $C_0$ to 3 | $C_L$ = 50pF, $R_L$ = 400Ω | | 30 | 50 | ns |
| $t_{pd0}$ | From $C_0$ to 3 | $C_L$ = 50pF, $R_L$ = 400Ω | | 24 | 40 | ns |
| $t_{pd1}$ | From $C_0$ to 4 | $C_L$ = 50pF, $R_L$ = 400Ω | | 30 | 50 | ns |
| $t_{pd0}$ | From $C_0$ to 4 | $C_L$ = 50pF, $R_L$ = 400Ω | | 28 | 50 | ns |
| $t_{pd1}$ | From $C_0$ to $C_4$ | $C_L$ = 50pF, $R_L$ = 780Ω | | 12 | 20 | ns |
| $t_{pd0}$ | From $C_0$ to $C_4$ | $C_L$ = 50pF, $R_L$ = 780Ω | | 12 | 20 | ns |
| $t_{pd1}$ | From $A_2$ or $B_2$ to 2 | $C_L$ = 50pF, $R_L$ = 400Ω | | | 40 | ns |
| $t_{pd0}$ | From $A_2$ or $B_2$ to 2 | $C_L$ = 50pF, $R_L$ = 400Ω | | | 35 | ns |
| $t_{pd1}$ | From $A_4$ of $B_4$ to 4 | $C_L$ = 50pF, $R_L$ = 400Ω | | | 40 | ns |
| $t_{pd0}$ | From $A_4$ of $B_4$ to 4 | $C_L$ = 50pF, $R_L$ = 400Ω | | | 35 | ns |

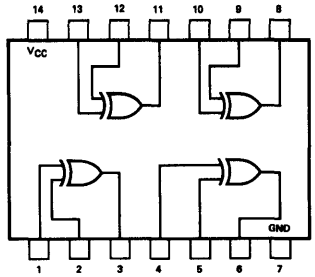
‡$T_{pd1}$ is propagation delay time to logical 1 level. $t_{pd0}$ is propagation delay time to logical 0 level.

NOTE: Electrical Characteristics Notes see Page 26.

**N7486A,J**
**S5486A,J,F** **Quad 2–Input Exclusive OR Gate**




A,F PACKAGE




J PACKAGE

**DESCRIPTION**

The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function $A\overline{B} + \overline{A}B$ at the output.

**TRUTH TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**RECOMMENDED OPERATING CONDITIONS.**

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S5486 Circuits | 4.5 | 5 | 5.5 | V |
| | N7486 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-out from each output, N: | Logical 0 | | | 10 | |
| | Logical 1 | | | 20 | |

NOTE: 1. These voltage values are with respect to network ground terminal.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS * | | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{in}$ (1) | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | | 2 | | | V |
| $V_{in}$ (0) | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | | 0.8 | V |
| $V_{out}$ (1) | Logical 1 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -800μA | | 2.4 | | | V |
| $V_{out}$ (0) | Logical 0 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ 0.8V, $I_{sink}$ = 16mA | | | | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{OS}$ | Short circuit output current† | | $V_{CC}$ = MAX, $V_{in(1)}$ = 4.5V, $V_{in(0)}$ = 0 | S5486 | -20 | | -55 | mA |
| | | | | N7486 | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, $V_{in}$ = 4.5V | S5486 | | 30 | 43 | mA |
| | | | | N7486 | | 30 | 50 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

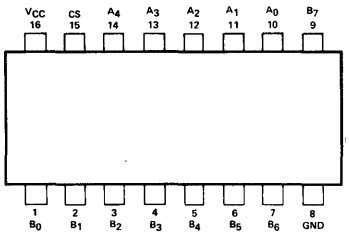
| PARAMETER | | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd0}$ | Propagation delay time to logical 0 level (other input low) | | $C_L$ = 15pF, $R_L$ = 400Ω | | 11 | 17 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level (other input low) | | $C_L$ = 15pF, $R_L$ = 400Ω | | 15 | 23 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level (other input high) | | $C_L$ = 15pF, $R_L$ = 400Ω | | 13 | 22 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level (other input high) | | $C_L$ = 15pF, $R_L$ = 400Ω | | 18 | 30 | ns |

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

† Not more than one output should be shorted at a time.

## N7488B,R 256–Bit Read–Only Memory




B,R PACKAGE

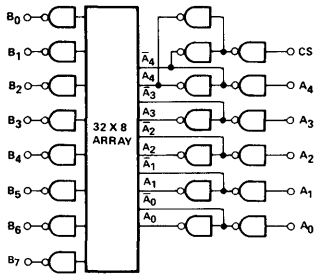
### DESCRIPTION

The 7488 is a TTL 256-Bit Read Only Memory organized as 32 word with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Select input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Select input is taken high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-OR operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

Customer may specify patterns for the 256-Bit Read Only Memory by completing the truth table/order blank.

### LOGIC DIAGRAM




### ELECTRICAL CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | | | | | | |

## 256-BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

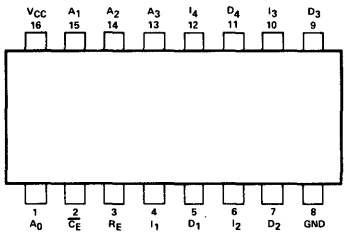
P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

| | INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WORD | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | ENABLE | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | | | | | | | | |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | | | | | | | | |
| 3 | 0 | 0 | 0 | 1 | 1 | 0 | | | | | | | | |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | | | | | | | | |
| 5 | 0 | 0 | 1 | 0 | 1 | 0 | | | | | | | | |
| 6 | 0 | 0 | 1 | 1 | 0 | 0 | | | | | | | | |
| 7 | 0 | 0 | 1 | 1 | 1 | 0 | | | | | | | | |
| 8 | 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | |
| 9 | 0 | 1 | 0 | 0 | 1 | 0 | | | | | | | | |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | | | | | | | | |
| 11 | 0 | 1 | 0 | 1 | 1 | 0 | | | | | | | | |
| 12 | 0 | 1 | 1 | 0 | 0 | 0 | | | | | | | | |
| 13 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | | | | |
| 14 | 0 | 1 | 1 | 1 | 0 | 0 | | | | | | | | |
| 15 | 0 | 1 | 1 | 1 | 1 | 0 | | | | | | | | |
| 16 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |
| 17 | 1 | 0 | 0 | 0 | 1 | 0 | | | | | | | | |
| 18 | 1 | 0 | 0 | 1 | 0 | 0 | | | | | | | | |
| 19 | 1 | 0 | 0 | 1 | 1 | 0 | | | | | | | | |
| 20 | 1 | 0 | 1 | 0 | 0 | 0 | | | | | | | | |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | | | | | | | | |
| 22 | 1 | 0 | 1 | 1 | 0 | 0 | | | | | | | | |
| 23 | 1 | 0 | 1 | 1 | 1 | 0 | | | | | | | | |
| 24 | 1 | 1 | 0 | 0 | 0 | 0 | | | | | | | | |
| 25 | 1 | 1 | 0 | 0 | 1 | 0 | | | | | | | | |
| 26 | 1 | 1 | 0 | 1 | 0 | 0 | | | | | | | | |
| 27 | 1 | 1 | 0 | 1 | 1 | 0 | | | | | | | | |
| 28 | 1 | 1 | 1 | 0 | 0 | 0 | | | | | | | | |
| 29 | 1 | 1 | 1 | 0 | 1 | 0 | | | | | | | | |
| 30 | 1 | 1 | 1 | 1 | 0 | 0 | | | | | | | | |
| 31 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | | | | |
| ALL | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## N7489B 64—Bit Read/Write Memory (RAM)



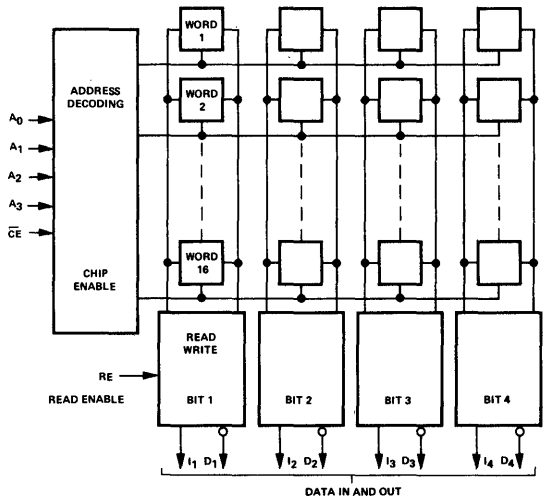

B PACKAGE

**DESCRIPTION**

The 7489 is a TTL 64-Bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 7489 is ideally suited for application in scratch pads and high speed buffer memories.

Words are selected through a 4-input binary decoder when the chip select input ($C_E$) is at logic "0". Data is written into the memory when Read Enable ($R_E$) is at logic "0" and read from the memory when $R_E$ is at logic "1".

**LOGIC DIAGRAM**

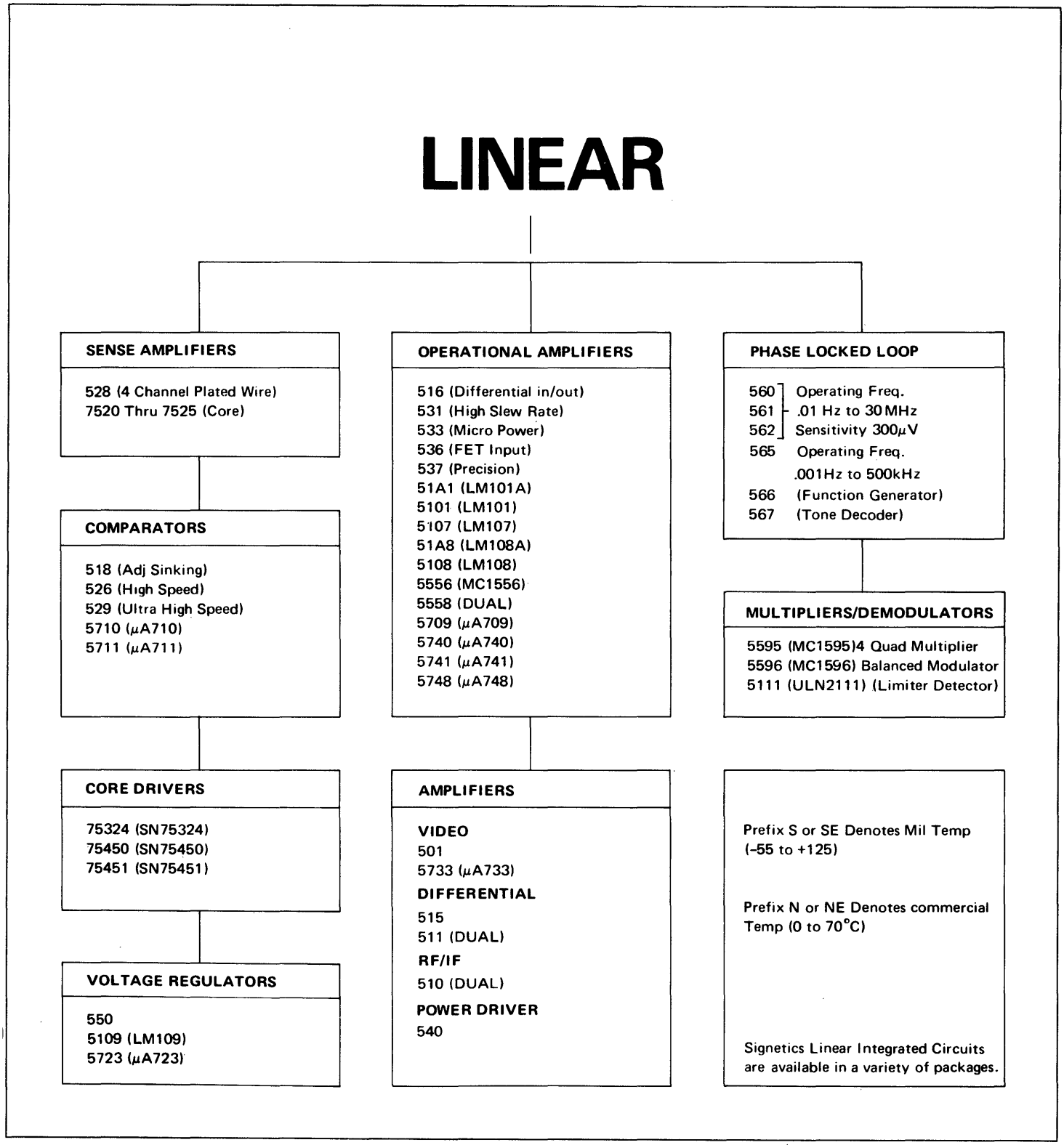



**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | | | | | | |

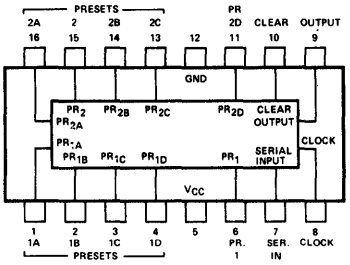
Refer to 8225 Data Sheet

# Signetics Linear Product Line

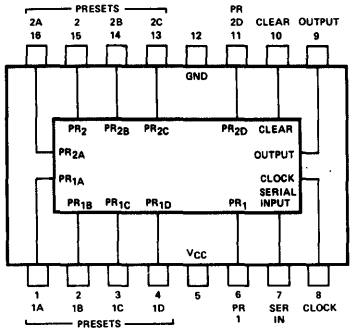


**N7494B,R**
**S5494R,E**

# 4–Bit Shift Register (Parallel–in, Serial–Out)




B,E PACKAGE



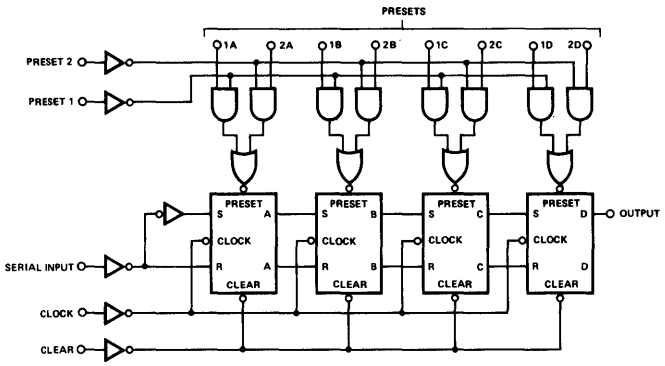

R PACKAGE

## DESCRIPTION

The 54/7494 4-Bit Shift Register is a TTL monolithic array configured to perform parallel-in to serial-out or serial-to-serial transfers of data.

Two sets of parallel preset inputs are provided to allow selection of data from two sources.

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1) | S5494 Circuits | 4.5 | 5 | 5.5 | V |
| | N7494 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out From Each Output | | | | 10 | |
| Width of Clock Pulse, $t_p$(clock) | | 35 | | | ns |
| Width of Clear Pulse, $t_p$(clear) | | 30 | | | ns |
| Width of Preset Pulse, $t_p$(preset) | | 30 | | | ns |
| Serial Input Setup Time: $t_{setup}$ (1) | | 35 | | | ns |
| Serial Input Setup Time: $t_{setup}$(0) | | 25 | | | ns |
| Serial Input Hold Time, $t_{hold}$ | | 0 | | | |

NOTE: 1. These voltage values are with respect to network ground terminal.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS * | | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | | $V_{CC}$ = MIN, $I_{load}$ = -400μA | | 2.4 | 3.5 | | V |
| $V_{out(0)}$ | Logical 0 output voltage | | $V_{CC}$ = MIN, $I_{sink}$ = 16mA | | | 0.22 | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current at any input except preset 1 and preset 2 | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(1)}$ | Logical 1 level input current at preset 1 and preset 2 | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 160 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current at any input except preset 1 and preset 2 | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at preset 1 and preset 2 | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -6.4 | mA |
| $I_{OS}$ | Short-circuit input current† | | $V_{CC}$ = MAX, $V_{out}$ = 0 | S5494 | -20 | | -57 | mA |
| | | | | N7494 | -18 | | -57 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | S5494 | | 35 | 50 | mA |
| | | | | N7494 | | 35 | 58 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | | | MHz |
| $t_{pd1}$ | Propagation delay time to logical 1 level from clock to output to output | | $C_L$ = 15pF, $R_L$ = 400Ω | | 25 | 40 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from clock to output | | $C_L$ = 15pF, $R_L$ = 400Ω | | 25 | 40 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level from preset to output | | $C_L$ = 15pF, $R_L$ = 400Ω | | | 35 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from clear to output | | $C_L$ = 15pF, $R_L$ = 400Ω | | | 40 | ns |

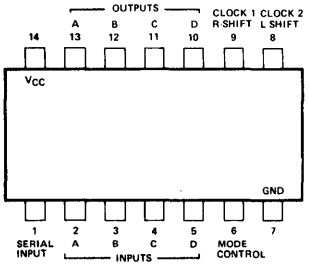
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

† Not more than one output should be shorted at a time.

**N7495A**
**S5495A,F**

# 4–Bit Right–Shift Left–Shift Register

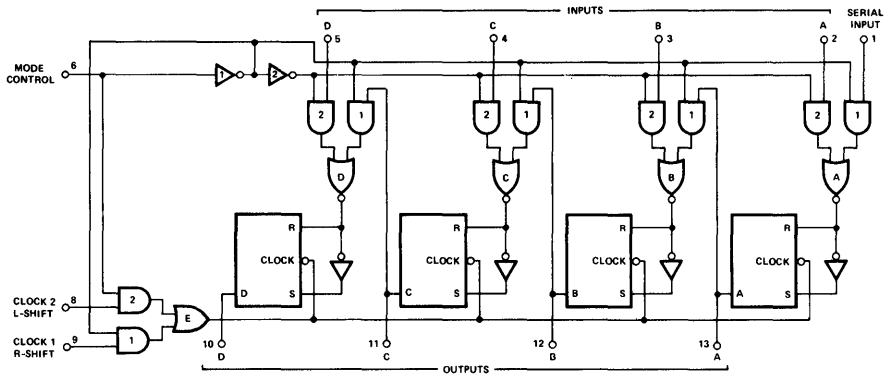



**A,F PACKAGE**

## DESCRIPTION

The 54/7495 is a Universal 4-Bit Shift Register designed with standard TTL techniques. The register consists of logic configured to perform right, left shift or parallel-in, parallel-out operations depending on the logical input level at the mode control.

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S5495 Circuits | 4.5 | 5 | 5.5 | V |
| | N7495 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out From Each Output | | | | 10 | |
| Width of Clock Pulse $t_p$(clock) | S5495 Circuits | 20 | 10 | | ns |
| | N7495 Circuits | 15 | 10 | | ns |
| Setup Time Required at Serial, A, B,.C, or D Inputs $t_{setup}$ | | 20 | 10 | | ns |
| Hold Time Required at Serial, A, B, C, or D Inputs $t_{hold}$ | | 0 | 10 | | ns |
| Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 1 input) | | 20 | | | ns |
| Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 2 input) | | 20 | | | ns |
| Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 2 input) | | 10 | | | ns |
| Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 1 input) | | 10 | | | ns |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. input voltages must be zero or positive with respect to network ground terminal.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS * | | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | | $V_{CC}$ = MIN, $I_{load}$ = -400μA | | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | | $V_{CC}$ = MIN, $I_{sink}$ = 16mA | | | | 0.4 | V |
| $I_{in(0)}$ | Logical 0 level input current at any input except mode control | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at mode control | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -3.2 | mA |
| $I_{in(1)}$ | Logical 1 level input current at any input except mode control | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(1)}$ | Logical 1 level input current at mode control | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 80 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{OS}$ | Short-circuit output current† | | $V_{CC}$ = MAX | | -18 | | -57 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | S5495 | | 50 | 72 | mA |
| | | | | N7495 | | 50 | 82 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

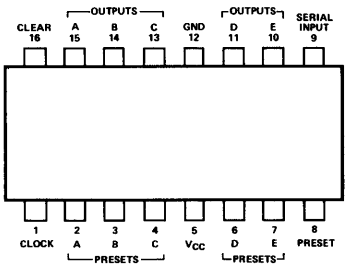
| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum shift frequency | | $C_L$ = 15pF, $R_L$ = 400Ω | 20 | 31 | | MHz |
| $t_{pd1}$ | Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs | | $C_L$ = 15pF, $R_L$ = 400Ω | | 26 | 35 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs | | $C_L$ = 15pF, $R_L$ = 400Ω | | 24 | 35 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

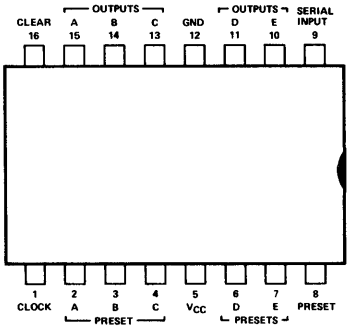
**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N7496B,R**
**S5496R,E** **5–Bit Shift Register**




**B,E PACKAGE**

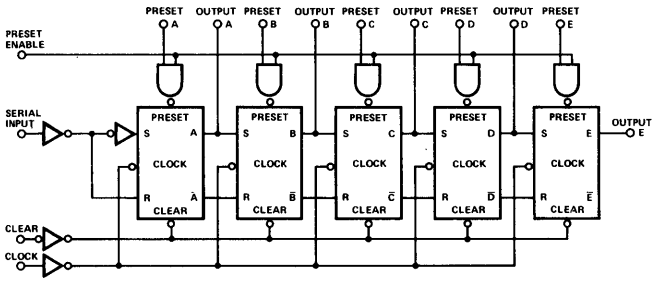



**R PACKAGE**

**DESCRIPTION**

The 54/7496 5-Bit Shift Register is designed with standard TTL techniques. The 5-Bit register is configured to perform parallel-to-serial or serial-to-parallel transfers of data. Each flip-flop has a preset input which is controlled by the preset enable. The preset is independent of the state of the clock input.

**LOGIC DIAGRAM**




**RECOMMENDED OPERATING CONDITIONS.**

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S5496 Circuits | 4.5 | 5 | 5.5 | V |
| | N7496 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from Output | | | | 10 | |
| Width of Clock Pulse, $t_{p(clock)}$ | | 35 | | | ns |
| Width of Clear Pulse, $t_{p(clear)}$ | | 30 | | | ns |
| Serial Input Setup Time, $t_{setup}$ | | 30 | | | ns |
| Serial Input Hold Time, $t_{hold}$ | | 0 | | | ns |

NOTE: 1: This voltage value is with respect to network ground terminal.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | 0.8 | V |

**ELECTRICAL CHARACTERISTICS (Cont'd)**

| PARAMETER | | TEST CONDITIONS * | | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN, $I_{load}$ = -400μA | | 2.4 | 3.5 | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN, $I_{sink}$ = 16mA | | | 0.22 | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current at any input except preset (pin ⑧) | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(1)}$ | Logical 1 level input current at preset (pin ⑧) | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 200 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current at any input except preset (pin ⑧) | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at preset (pin ⑧) | $V_{CC}$ = Max, $V_{in}$ = 0.4V | | | | -8 | mA |
| $I_{OS}$ | Short-circuit output current† | $V_{CC}$ = MAX, $V_{out}$ = 0 | S5496 | -20 | | -57 | mA |
| | | | N7496 | -18 | | -57 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX | S5496 | | 48 | 68 | mA |
| | | | N7496 | | 48 | 79 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

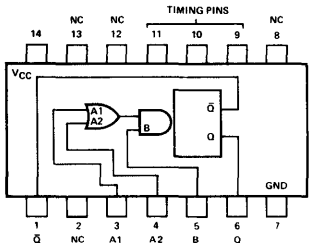
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum clock frequency | $C_L$ = 15pF, $R_L$ = 400Ω | 10 | | | MHz |
| $t_{pd1}$ | Propagation delay time to logical 1 level from clock to output | $C_L$ = 15pF, $R_L$ = 400Ω | | 25 | 40 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from clock to output | $C_L$ = 15pF, $R_L$ = 400Ω | | 25 | 40 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level from preset to output | $C_L$ = 15pF, $R_L$ = 400Ω | | | 35 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from preset to output | $C_L$ = 15pF, $R_L$ = 400Ω | | 28 | 40 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from clear to output | $C_L$ = 15pF, $R_L$ = 400Ω | | | 55 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

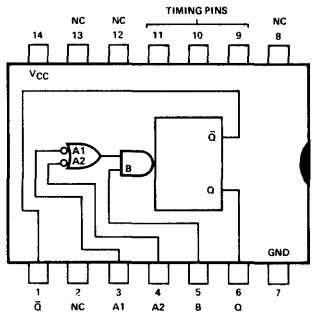
**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N74121A,Q**
**S54121A,Q,F** **Monostable Multivibrator**




A, F PACKAGE




Q PACKAGE

## DESCRIPTION

The 54/74121 Monostable Multivibrator is a monolithic TTL device providing triggering from either positive or negative going inputs. Both the true and complement output pulses are provided.

Pulse duration is determined by addition of an external timing capacitor between pins 10 and 11.

## TRUTH TABLE

| $t_n$ INPUT | | | $t_{n+1}$ INPUT | | | OUTPUT |
|---|---|---|---|---|---|---|
| A1 | A2 | B | A1 | A2 | B | |
| 1 | 1 | 0 | 1 | 1 | 1 | Inhibit |
| 0 | X | 1 | 0 | X | 0 | Inhibit |
| X | 0 | 1 | X | 0 | 0 | Inhibit |
| 0 | X | 0 | 0 | X | 1 | One Shot |
| X | 0 | 0 | X | 0 | 1 | One Shot |
| 1 | 1 | 1 | X | 0 | 1 | One Shot |
| 1 | 1 | 1 | 0 | X | 1 | One Shot |
| X | 0 | 0 | X | 1 | 0 | Inhibit |
| 0 | X | 0 | 1 | X | 0 | Inhibit |
| X | 0 | 1 | 1 | 1 | 1 | Inhibit |
| 0 | X | 1 | 1 | 1 | 1 | Inhibit |
| 1 | 1 | 0 | X | 0 | 0 | Inhibit |
| 1 | 1 | 0 | 0 | X | 0 | Inhibit |

$1 = V_{in(1)} \geq 2V$
$0 = V_{in(0)} \leq 0.8V$

NOTES:
1. $t_n$ = time before input transition.
2. $t_{n+1}$ = time after input transition.
3. X indicates that either a logical 0 or 1, may be present

## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$: | S54121 Circuits | 4.5 | 5 | 5.5 | V |
| | N74121 Circuits | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out From Each Output, N | | | | 10 | |
| Input Pulse Rise/Fall Time: | Schmitt Input (B) | | | 1 | V/s |
| | Logic Inputs (A1, A2) | | | 1 | V/μs |
| Input Pulse Width | | 50 | | | ns |
| External Timing Resistance Between Pins (11) and (14) (Pin (9) open) | | 1.4 | | | kΩ |
| External Timing Resistance: | S54121 | | | 30 | kΩ |
| | N74121 | | | 40 | kΩ |
| Timing Capacitance | | 0 | | 1000 | μF |
| Output Pulse Width | | | | 40 | s |
| Duty Cycle: | $R_T$ = 2 kΩ | | | 67% | |
| | $R_T$ = 30 kΩ (S54121) or | | | 90% | |
| | $R_T$ = 40 kΩ (N74121) | | | | |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS * | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going threshold voltage at A input | | $V_{CC}$ = MIN | | 1.4 | 2 | V |
| $V_{T-}$ | Negative-going threshold voltage at A input | | $V_{CC}$ = MIN | 0.8 | 1.4 | | V |
| $V_{T+}$ | Positive-going threshold voltage at B input | | $V_{CC}$ = MIN | | 1.55 | 2 | V |

**ELECTRICAL CHARACTERISTICS (Cont'd)**

| PARAMETER | | TEST CONDITIONS * | | MIN | TYP ** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{T-}$ | Negative-going threshold voltage at B input | $V_{CC}$ = MIN | | 0.8 | 1.35 | | V |
| $V_{out(0)}$ | Logical 0 output voltage | $V_{CC}$ = MIN, $I_{sink}$ = 16mA | | | 0.22 | 0.4 | V |
| $V_{out(1)}$ | Logical 1 output voltage | $V_{CC}$ = MIN, $I_{load}$ = -400μA | | 2.4 | 3.3 | | V |
| $I_{in(0)}$ | Logical 0 level input current at $A_1$ or $A_2$ | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1 | -1.6 | mA |
| $I_{in(0)}$ | Logical 0 level input current at B | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -2 | -3.2 | mA |
| $I_{in(1)}$ | Logical 1 level input current at $A_1$ of $A_2$ | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 2 | 40 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 0.05 | 1 | mA |
| $I_{in(1)}$ | Logical 1 level input current at B | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 4 | 80 | μA |
| | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 0.05 | 1 | mA |
| $I_{OS}$ | Short circuit output current at Q or $\overline{Q}$† | $V_{CC}$ = MAX | S54121 | -20 | -25 | -55 | mA |
| | | | N74121 | -18 | -25 | -55 | mA |
| $I_{CC}$ | Power supply current in quiescent (unfired) state | $V_{CC}$ = MAX | | | 13 | 25 | mA |
| $I_{CC}$ | Power supply current in fired state | $V_{CC}$ = MAX | | | 23 | 40 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C,**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | Propagation delay time to logical 1 level from B input to Q output | $C_L$ = 15pF, | $C_T$ = 80pF | 15 | 35 | 55 | ns |
| $t_{pd1}$ | Propagation delay time to logical 1 level from A1/A2 inputs to Q output | $C_L$ = 15pF, | $C_T$ = 80pF | 25 | 45 | 70 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from B input to $\overline{Q}$ output | $C_L$ = 15pF, | $C_T$ = 80pF | 20 | 40 | 65 | ns |
| $t_{pd0}$ | Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output | $C_L$ = 15pF, | $C_T$ = 80pF | 30 | 50 | 80 | ns |
| $t_{p(out)}$ | Pulse width obtained using internal timing resistor | $C_L$ = 15pF, $R_T$ = Open, | $C_T$ = 80pF Pin ⑨ to $V_{CC}$ | 70 | 110 | 150 | ns |
| $t_{p(out)}$ | Pulse width obtained with zero timing capacitance | $C_L$ = 15pF, $R_T$ = Open, | $C_T$ = 0. Pin ⑨ to $V_{CC}$ | 20 | 30 | 50 | ns |
| $t_{p(out)}$ | Pulse width obtained using external timing resistor | $C_L$ = 15pF, $R_T$ = 10kΩ, | $C_T$ = 100pF, Pin ⑨ Open | 600 | 700 | 800 | ns |
| $t_{p(out)}$ | Pulse width obtained using external timing resistor | $C_L$ = 15pF, $R_T$ = 10kΩ | $C_T$ = 1μF, Pin ⑨ Open | 6 | 7 | 8 | ms |
| $t_{hold}$ | Minimum duration of trigger pulse | $C_L$ = 15pF, $R_T$ = Open, | $C_T$ = 80pF, Pin ⑨ to $V_{CC}$ | | 30 | 50 | ns |

NOTE: Electrical Characteristics Notes See Page 42

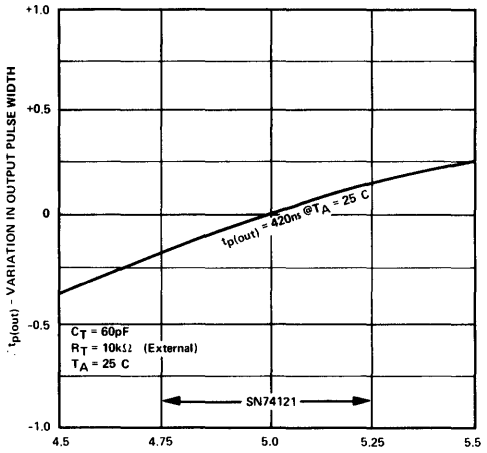
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

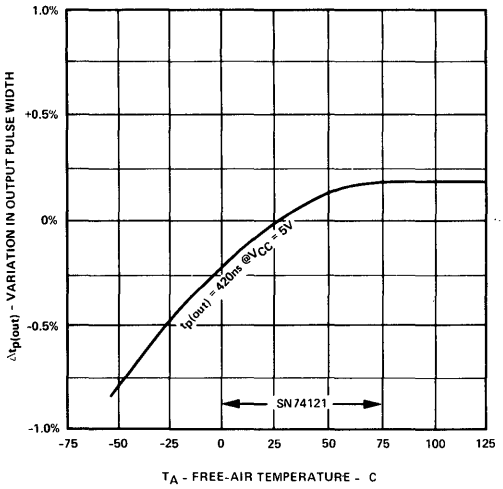
†Not more than one output should be shorted at a time.

## TYPICAL CHARACTERISTICS

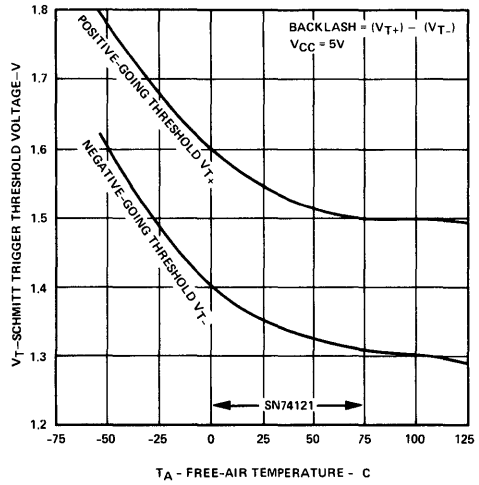
### VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



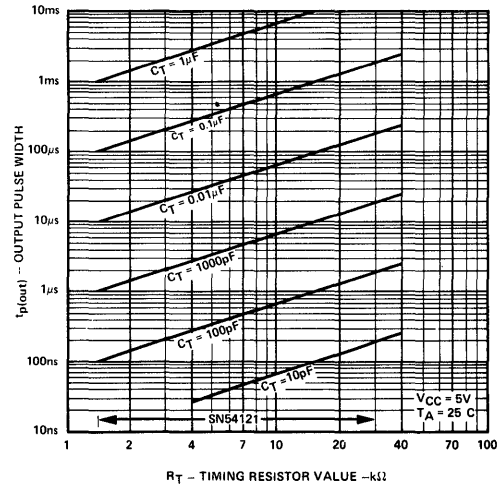

### VARIATION IN OUTPUT PULSE WIDTH VERSUS FREE-AIR TEMPERATURE




### SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS FREE-AIR TEMPERATURE




### OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE



# Signetics MOS Roundup

## DYNAMIC SHIFT REGISTERS

**2502**
**Quad 256-Bit DSR**
10MHz Data Rate
$C_{CL}$ = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

**2503**
**Dual 512-Bit DSR**
10MHz Data Rate
$C_{CL}$ = 140pF max.
Power Supplies +5, -5V
40μmW/bit/MHz
Multiplexed Data

**2504**
**Single 1024-Bit DSR**
10MHz Data Rate
$C_{CL}$ = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

**2505**
**512-Bit DSR**
5MHz Clock Rate
$C_{CL}$ = 80pF
Power Supplies +5, -5V
100μW/bit/MHz
Recirculate +CS Logic

**2506**
**Dual 100-Bit DSR**
3MHz Clock Rate
$C_{CL}$ = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Bare Drain Output

**2507**
**Dual 100-Bit DSR**
3MHz Clock Rate
$C_{CL}$ = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Resistor Pull-down (7.5k)

**2512**
**1024-Bit DSR**
5MHz Clock Rate
$C_{CL}$ = 140pF
Power Supplies +5, -5V
150μW/bit/MHz
Recirculate Logic

**2515**
**Dual 512-Bit DSR**
5MHz Clock Rate
$C_{CL}$ = 140pF
Power Supplies +5, -5V
100μW/bit/MHz
Recirculate +CS logic

**2517**
**Dual 100-Bit DSR**
3MHz Clock Rate
$C_{CL}$ = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Resistor Pull-down (20k)

## STATIC SHIFT REGISTERS

**2509**
**Dual 50-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Data & Clock TTL Comp.
Tri-State Outputs
Recirculate Logic

**2510**
**Dual 100-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Data & Clock TTL Comp.
Tri-State Outputs
Recirculate Logic

**2511**
**Dual 200-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Data & Clock TTL Comp.
Tri-State Outputs
Recirculate Logic

**2518 (COMING SOON)**
**Hex 32-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Recirculate Logic

**2519 (COMING SOON)**
**Hex 40-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Recirculate Logic

**2521 (COMING SOON)**
**Dual 128-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Data and Clock TTL Comp.
Tri-State Outputs
Recirculate Logic

**2522 (COMING SOON)**
**Dual 132-Bit SSR**
3MHz Clock Rate
Power Supplies +5, -12V
Data and Clock TTL Comp.
Tri-State outputs
Recirculate Logic

## STATIC SHIFT REGISTERS

**2000 SERIES**
$C_L$=5pF
−14, −28V Power Supplies

**S2001**
**Dual 16-Bit SSR**
0-1 MHz

**S2002**
**Dual 25-Bit SSR**
0-1 MHz

**S2003**
**Dual 32-Bit SSR**
0-1 MHz

**S2004**
**Dual 50-Bit SSR**
0-1 MHz

**S2005**
**Dual 100-Bit SSR**
0-1 MHz

**N2010**
**Dual 100-Bit SSR**
0-3 MHz

## RANDOM ACCESS MEMORIES

**2501**
**256 X 1 SRAM**
Decoded
AT 800ns
300mW
Power Supplies +5, -7, -10V
Silicone 16-pin DIP

**2508**
**1024 X 1 DRAM**
Decoded
AT 330ns
CT 500ns
3 Chip Selects
2.7mA Out
4 Clocks
Power Supplies +5, -12V
TTL Comp. Inputs

**2500 SERIES**
**SILICON GATE MOS**

## READ-ONLY MEMORIES

**2513**
**64 X 7 X 5/64 X 8 X 5**
Static Character Gen.
600ns Access Time
ASCII Font Standard
Power Supplies +5, -5, -12V
350mW

**2514**
**512 X 5 SROM**
600ns Access Time
Power Supplies +5, -5, -12V
350mW

**2516**
**64 X 6 X 8 Character Generator**
384 X 8 Static ROM
550ns Access Time
Tri-State outputs
ASCII Font Standard
Power Supplies +5, -5, -12V

## STATIC READ-ONLY MEMORIES

**2400 SERIES**
550ns Access Time
250mW
+12, −12V Power Supplies
Bare Drain or MOS
Pull-Down Resistor

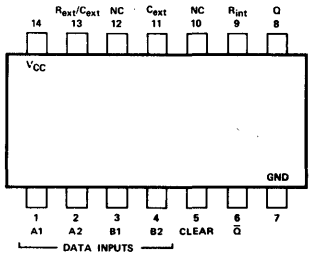
**2410**
**256 X 4**
16-Pin DIP

**2420**
**256 X 4, 128 X 8**
Single or 3-line Chip Enable
24-Pin DIP

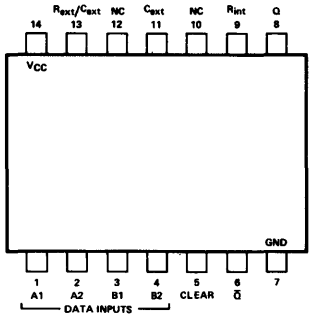
**2430**
**256 X 8**
Single or 3-line Chip Enable
24-Pin DIP

**METAL GATE MOS**

**N74122A,Q** **Retriggerable Monostable**
**S54122A,Q,F** **Multivibrator with Clear**




A,F PACKAGE



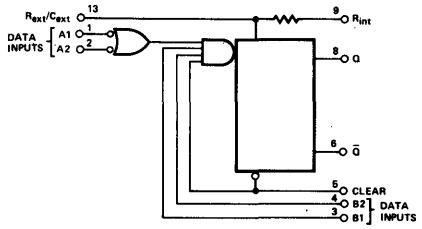

Q PACKAGE

## DESCRIPTION

The 54/74122 Retriggerable Monostable Miltivibrator with clear is a monolithic TTL device providing triggering from either a positive or negative going pulse. Both the true and complement output pulses are provided. A direct clear input is provided and will override the output pulse.

Pulse duration is determined by addition of an external capacitor between pins 11 and 13.

## LOGIC DIAGRAM




## TRUTH TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| A1 | A2 | B1 | B2 | Q | Q̄ |
| H | H | X | X | L | H |
| X | X | L | X | L | H |
| X | X | X | L | L | H |
| L | X | H | H | L | H |
| L | X | ↑ | H | ⎍ | ⎎ |
| L | X | H | ↑ | ⎍ | ⎎ |
| X | L | H | H | L | H |
| X | L | ↑ | H | ⎍ | ⎎ |
| X | L | H | ↑ | ⎍ | ⎎ |
| H | ↓ | H | H | ⎍ | ⎎ |
| ↓ | ↓ | H | H | ⎍ | ⎎ |
| ↓ | H | H | H | ⎍ | ⎎ |

NOTE: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions.).

## RECOMMENDED OPERATING CONDITIONS.

| | | S54122 | | | N74122 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Normalized fan-out from each output, N | High logic level | | | 20 | | | 20 | |
| | Low logic level | | | 10 | | | 10 | |
| Input data setup time, $t_{setup}$ (see Note 3 and Figure 2) | | 40† | | | 40† | | | ns |
| Input data hold time, $t_{hold}$ (see Note 4 and Figure 2) | | 40† | | | 40† | | | ns |
| Width of clear pulse, $t_{w(clear)}$ | | 40† | | | 40† | | | ns |
| External timing resistance | | 5 | | 25 | 5 | | 50 | kΩ |
| External capacitance | | No restriction | | | No restriction | | | |
| Wiring capacitance at $R_{ext}/C_{ext}$ terminal | | | | 50 | | | 50 | pF |
| Operating free-air temperature, $T_A$ | | -55 | 25 | 125 | 0 | 25 | 70 | °C |

NOTES:
1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the S54122/N74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.
5. Ground $C_{ext}$ to measure $V_{OH}$ at $\overline{Q}$, $V_{OL}$ at Q, or $I_{OS}$ at Q. $C_{ext}$ is open to measure $V_{OH}$ at $\overline{Q}$, $V_{OL}$ at Q, or $I_{OS}$ at $\overline{Q}$.
6. Quiescent $I_{CC}$ is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, $C_{ext}$ = 0.02μF, and $R_{ext}$ = 25kΩ, $R_{int}$ of S54122/N74122 is open.
7. $I_{CC}$ is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, $C_{ext}$ = 0.02μF, and $R_{ext}$ = 25kΩ. $R_{int}$ of S54122/N74122 is open.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS* | | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_I$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = -12mA | | | | -1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $I_{OH}$ = -800μA, See Note 5 | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $I_{OL}$ = 16mA, See Note 5 | | | 0.22 | 0.4 | V |
| $i_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, $V_I$ = 2.4V | data inputs | | | 40 | μA |
| | | | | clear inputs | | | 80 | μA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = MAX, $V_I$ = 0.4V | data inputs | | | -1.6 | mA |
| | | | | clear inputs | | | -3.2 | mA |
| $I_{OS}$ | Short-circuit output current† | | $V_{CC}$ = MAX, | | -10 | | -40 | mA |
| $I_{CC}$ | Supply current (quiescent or triggered) | | $V_{CC}$ = MAX, S54122,N74122 | | | 23 | 28 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output, from either A input | | | | 22 | 33 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output, from either B input | | | | 19 | 28 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q output, from either A input | | $C_{ext}$ = 0, $R_{ext}$ = 5kΩ, $C_L$ = 15pF, $R_L$ = 400Ω | | 30 | 40 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q output from either B input | | | | 27 | 36 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q output, from clear input | | | | 18 | 27 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output, from clear input | | | | 30 | 40 | ns |
| $t_w$ (min) | Minimum width of Q output pulse | | | | 45 | 65 | ns |
| $t_w$ | Width of Q output pulse | | $C_{ext}$ = 1000pF, $R_{ext}$ = 10kΩ, $C_L$ = 15pF, $R_L$ = 400Ω | 3.08 | 3.42 | 3.76 | μs |

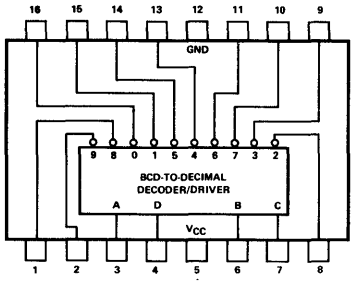
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

## N74141B

## BCD–to–Decoder/Driver with Blanking



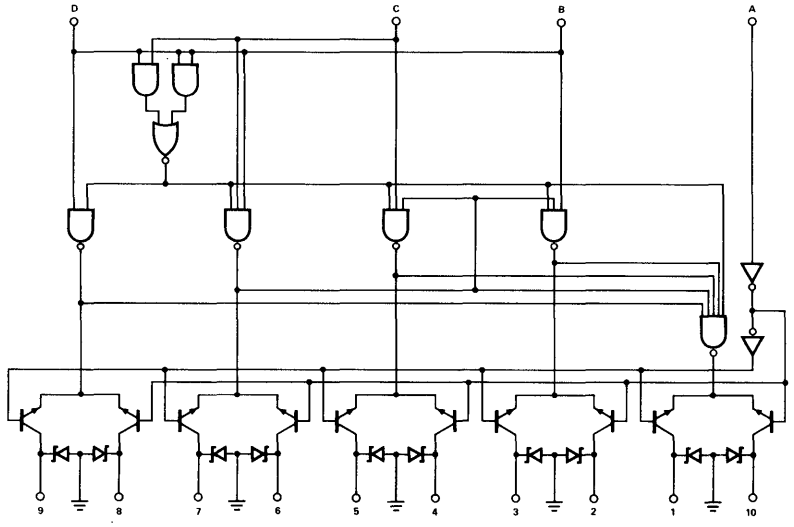

**B PACKAGE**

### DESCRIPTION

The 74141 BCD-to-Decimal Decoder/Driver is a one-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes.

Blanking (outputs turned off) is provided for binary codes 10 through 15.

### LOGIC DIAGRAM




### TRUTH TABLE

| INPUT | | | | OUTPUT |
|---|---|---|---|---|
| D | C | B | A | ON* |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |
| H | L | L | L | 8 |
| H | L | L | H | 9 |
| H | L | H | L | NONE |
| H | L | H | H | NONE |
| H | H | L | L | NONE |
| H | H | L | H | NONE |
| H | H | H | L | NONE |
| H | H | H | H | NONE |

H = high level, L = low level

*All other outputs are off

### RECOMMENDED OPERATING CONDITIONS.

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage $V_{CC}$ (see Note 1) | 4.75 | 5 | 5.25 | V |
| Output voltage (see Notes 1 and 2) | | | 65 | V |
| Operating free-air temperature range | 0 | 25 | 70 | °C |

NOTES:

1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

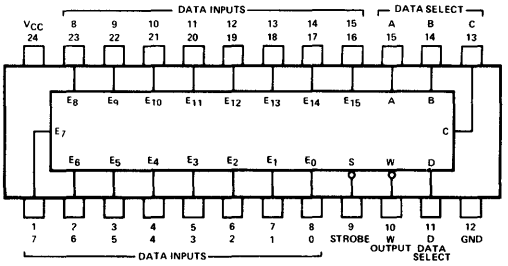
| PARAMETER | | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{O(on)}$ | On-state output voltage | | $V_{CC}$ = MIN, $I_O$ = 7mA | | | 2.5 | V |
| $V_O$ (off) | Off-state output voltage for input counts 0 thru 9 | | $V_{CC}$ = MAX, $I_O$ = 0.5mA | 65 | | | V |
| $I_{O(off)}$ | Off-state reverse current | | $V_{CC}$ = MAX, $V_O$ = 55V | | | 50 | μA |
| $I_O$ (off) | Off-state reverse current for input counts 10 thru 15 | | $V_{CC}$ = MAX, $V_O$ = 30V | | | 5 | μA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current into A | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{IL}$ | Low-level input current into B, C, or D | | | | | -3.2 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | | 11 | 16 | mA |

**NOTE: SEE THE 8T02 FOR IMPROVED PERFORMANCE IN THE SAME PIN CONFIGURATION.**

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
**This typical value is at $V_{CC}$ = 5V, $T_A$ = 25°C.

**N74150N,P**
**S54150N,P,Y**

# 16—Line to 1—Line Data Selector/Multiplexer

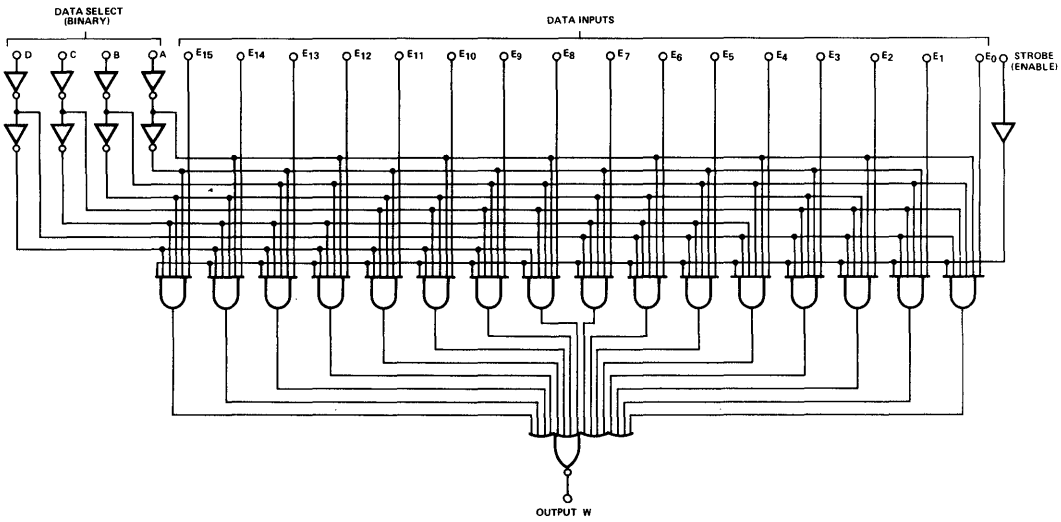



**N,Y PACKAGE**

## DESCRIPTION

The 54/74150 is a one-of-sixteen data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line;

## LOGIC DIAGRAM




## TRUTH TABLE

| INPUTS | | | | | | | | | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | STROBE | $E_0$ | $E_1$ | $E_2$ | $E_3$ | $E_4$ | $E_5$ | $E_6$ | $E_7$ | $E_8$ | $E_9$ | $E_{10}$ | $E_{11}$ | $E_{12}$ | $E_{13}$ | $E_{14}$ | $E_{15}$ | W |
| X | X | X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 0 | 0 | 1 | 0 | X | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 0 | 0 | 1 | 0 | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 0 | 1 | 0 | 0 | X | X | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 0 | 1 | 0 | 0 | X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | 0 | X | X | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 1 | 0 | 0 | 0 | X | X | X | X | 1 | X | X | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 1 | 0 | 1 | 0 | X | X | X | X | X | 0 | X | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 1 | 0 | 1 | 0 | X | X | X | X | X | 1 | X | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | 0 | X | X | X | X | X | X | X | X | X | 1 |
| 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | 1 | X | X | X | X | X | X | X | X | X | 0 |
| 0 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | X | X | X | X | X | X | X | X | 1 |
| 0 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | 1 | X | X | X | X | X | X | X | X | 0 |
| 1 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | 0 | X | X | X | X | X | X | X | 1 |
| 1 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | 1 | X | X | X | X | X | X | X | 0 |
| 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | 0 | X | X | X | X | X | X | 1 |
| 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | 1 | X | X | X | X | X | X | 0 |
| 1 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | 0 | X | X | X | X | X | 1 |
| 1 | 0 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | 1 | X | X | X | X | X | 0 |
| 1 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | 0 | X | X | X | X | 1 |
| 1 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | 1 | X | X | X | X | 0 |
| 1 | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | 0 | X | X | X | 1 |
| 1 | 1 | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | 1 | X | X | X | 0 |
| 1 | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | X | X | 1 |
| 1 | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | X | X | 0 |
| 1 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | X | 1 |
| 1 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | X | 0 |
| 1 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | 0 |

When used to indicate an input condition , X = LOGICAL 1 or LOGICAL 0

## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ | S54150 Circuit | 4.5 | 5 | 5.5 | V |
| | N74150 Circuit | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from Each Output (N): | Logical 0 | | | 10 | |
| | Logical 1 | | | 20 | |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{in}$ (1) | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in}$ (0) | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out}$ (1) | Logical 1 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -800μA | 2.4 | | | V |
| $V_{out}$ (0) | Logical 0 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | 0.4 | V |
| $I_{in}$ (1) | Logical 1 level input (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short circuit output current† | | $V_{CC}$ = MAX, $V_{out}$ = 0 | -20 | | -55 | mA |
| | | | | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, $V_{in}$ = 4.5V | | 40 | 68 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd0}$ | A,B,orC(4 levels) | Y | | | 20 | 30 | ns |
| $t_{pd1}$ | A,B,orC(4 levels) | Y | | | 35 | 52 | ns |
| $t_{pd0}$ | A,B,C,orD(3 levels) | W | | | 22 | 33 | ns |
| $t_{pd1}$ | A,B,C,orD(3 levels) | W | | | 23 | 35 | ns |
| $t_{pd0}$ | STROBE | Y | | | 19 | 30 | ns |
| $t_{pd1}$ | STROBE | Y | $C_L$ = 15pF, $R_L$ = 400Ω | | 35 | 52 | ns |
| $t_{pd0}$ | STROBE | W | | | 21 | 30 | ns |
| $t_{pd1}$ | STROBE | W | | | 15.5 | 24 | ns |
| $t_{pd0}$ | $D_0$ thru $D_7$ | Y | | | 16 | 24 | ns |
| $t_{pd1}$ | $D_0$ thru $D_7$ | Y | | | 19 | 29 | ns |
| $t_{pd0}$ | $E_0$ thru $E_{15}$ | W | | | 8.5 | 14 | ns |
| $t_{pd1}$ | $E_0$ thru $E_{15}$ | W | | | 13 | 20 | ns |

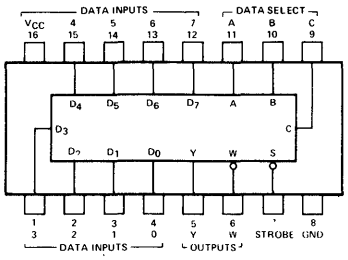
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

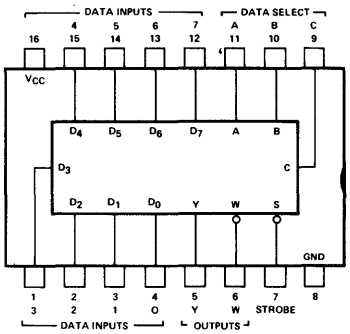
†Not more than one output should be shorted at a time.

**N74151B,R**
**S54151B,R,E**

**8—Line to 1—Line Data Selector/Multiplexer**




**B,E PACKAGE**

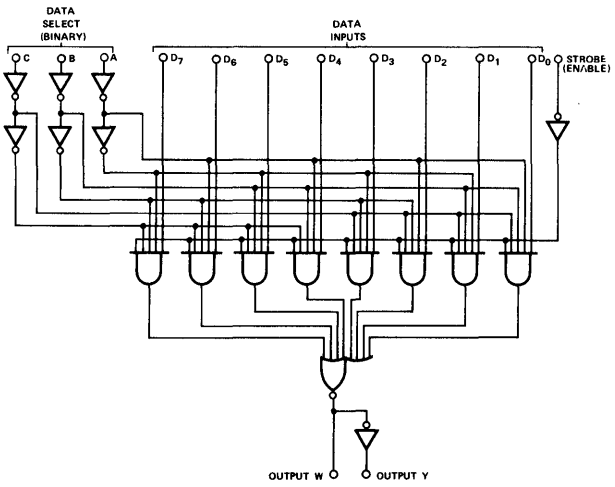



**R PACKAGE**

## DESCRIPTION

The 54/74151 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line. Both true and complement outputs are available.

## LOGIC DIAGRAM




## TRUTH TABLE

| INPUTS | | | | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | B | A | STROBE | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | Y(1) | W |
| X | X | X | 1 | X | X | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | 1 | 0 |
| 0 | 0 | 1 | 0 | X | 0 | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 1 | 0 | X | 1 | X | X | X | X | X | X | 1 | 0 |
| 0 | 1 | 0 | 0 | X | X | 0 | X | X | X | X | X | 0 | 1 |
| 0 | 1 | 0 | 0 | X | X | 1 | X | X | X | X | X | 1 | 0 |
| 0 | 1 | 1 | 0 | X | X | X | 0 | X | X | X | X | 0 | 1 |
| 0 | 1 | 1 | 0 | X | X | X | 1 | X | X | X | X | 1 | 0 |
| 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | X | X | 0 | 1 |
| 1 | 0 | 0 | 0 | X | X | X | X | 1 | X | X | X | 1 | 0 |
| 1 | 0 | 1 | 0 | X | X | X | X | X | 0 | X | X | 0 | 1 |
| 1 | 0 | 1 | 0 | X | X | X | X | X | 1 | X | X | 1 | 0 |
| 1 | 1 | 0 | 0 | X | X | X | X | X | X | 0 | X | 0 | 1 |
| 1 | 1 | 0 | 0 | X | X | X | X | X | X | 1 | X | 1 | 0 |
| 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | 1 | 1 | 0 |

NOTES:
1. S54151/N74151 only.
2. When used to indicate an input, X = irrelevant.

## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S54151 Circuit | 4.5 | 5 | 5.5 | V |
| | N74151 Circuit | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from Each Output (N): | Logical 0 | | | 10 | |
| | Logical 1 | | | 20 | |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{in}$ (1) | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in}$ (0) | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out}$ (1) | Logical 1 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -800μA | 2.4 | | | V |
| $V_{out}$ (0) | Logical 0 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | 0.4 | V |
| $I_{in}$ (1) | Logical 1 level input current (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short circuit output current† | | $V_{CC}$ = MAX, $V_{out}$ = 0 | -20 | | -55 | mA |
| | | | | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, $V_{in}$ = 4.5V | | 29 | 48 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd0}$ | A,B,orC(4 levels) | Y | | | 20 | 30 | ns |
| $t_{pd1}$ | A,B,orC(4 levels) | Y | | | 35 | 52 | ns |
| $t_{pd0}$ | A,B,C,orD(3 levels) | W | | | 22 | 33 | ns |
| $t_{pd1}$ | A,B,C,orD(3 levels) | W | | | 23 | 35 | ns |
| $t_{pd0}$ | STROBE | Y | | | 19 | 30 | ns |
| $t_{pd1}$ | STROBE | Y | $C_L$ = 15pF, $R_L$ = 400Ω | | 35 | 52 | ns |
| $t_{pd0}$ | STROBE | W | | | 21 | 30 | ns |
| $t_{pd1}$ | STROBE | W | | | 15.5 | 24 | ns |
| $t_{pd0}$ | $D_0$ thru $D_7$ | Y | | | 16 | 24 | ns |
| $t_{pd1}$ | $D_0$ thru $D_7$ | Y | | | 19 | 29 | ns |
| $t_{pd0}$ | $E_0$ thru $E_{15}$ | W | | | 8.5 | 14 | ns |
| $t_{pd1}$ | $E_0$ thru $E_{15}$ | W | | | 13 | 20 | ns |

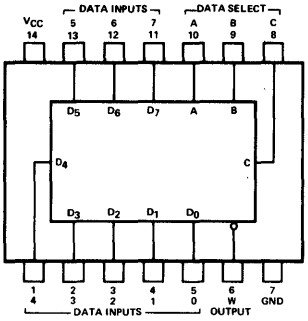
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

† Not more than one output should be shorted at a time.

N74152Q
S54152Q

# 8–Line to 1–Line Data Selector/Multiplexer

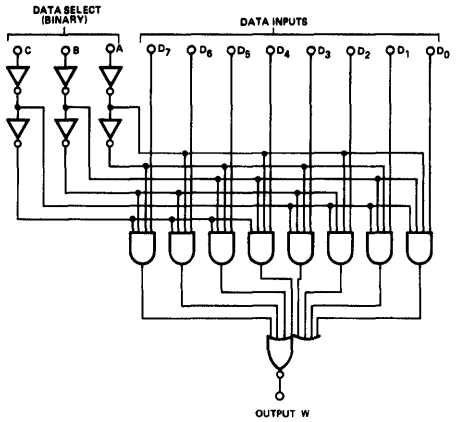



**Q PACKAGE**

## DESCRIPTION

The 54/74152 is a one-of-eight data selector which performs parallel to serial data conversion. The 54/74152 is identical to the 54/74151 with the exclusion of the true output and strobe. It is available in the 14-pin flatpak only.

## LOGIC DIAGRAM




## TRUTH TABLE

| INPUTS | | | | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C | B | A | STROBE | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | Y(1) | W |
| X | X | X | 1 | X | X | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | 1 | 0 |
| 0 | 0 | 1 | 0 | X | 0 | X | X | X | X | X | X | 0 | 1 |
| 0 | 0 | 1 | 0 | X | 1 | X | X | X | X | X | X | 1 | 0 |
| 0 | 1 | 0 | 0 | X | X | 0 | X | X | X | X | X | 0 | 1 |
| 0 | 1 | 0 | 0 | X | X | 1 | X | X | X | X | X | 1 | 0 |
| 0 | 1 | 1 | 0 | X | X | X | 0 | X | X | X | X | 0 | 1 |
| 0 | 1 | 1 | 0 | X | X | X | 1 | X | X | X | X | 1 | 0 |
| 1 | 0 | 0 | 0 | X | X | X | X | 0 | X | X | X | 0 | 1 |
| 1 | 0 | 0 | 0 | X | X | X | X | 1 | X | X | X | 1 | 0 |
| 1 | 0 | 1 | 0 | X | X | X | X | X | 0 | X | X | 0 | 1 |
| 1 | 0 | 1 | 0 | X | X | X | X | X | 1 | X | X | 1 | 0 |
| 1 | 1 | 0 | 0 | X | X | X | X | X | X | 0 | X | 0 | 1 |
| 1 | 1 | 0 | 0 | X | X | X | X | X | X | 1 | X | 1 | 0 |
| 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | 1 | 1 | 0 |

When used to indicate an input, X = Irrelevant.

## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S54152 Circuit | 4.5 | 5 | 5.5 | V |
| | N74152 Circuit | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from Each Output (N): | Logical 0 | | | 10 | |
| | Logical 1 | | | 20 | |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{in}$ (1) | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | 2 | | | V |
| $V_{in}$ (0) | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{out}$ (1) | Logical 1 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -800μA | 2.4 | | | V |
| $V_{out}$ (0) | Logical 0 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | 0.4 | V |
| $I_{in}$ (1) | Logical 1 level input (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current (each input) | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short circuit output current† | | $V_{CC}$ = MAX, $V_{out}$ = 0 | -20<br>-18 | | -55<br>-55 | mA<br>mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, $V_{in}$ = 4.5V | | 26 | 43 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd0}$ | A,B,orC(4 levels) | Y | | | 20 | 30 | ns |
| $t_{pd1}$ | A,B,orC(4 levels) | Y | | | 35 | 52 | ns |
| $t_{pd0}$ | A,B,C,orD(3 levels) | W | | | 22 | 33 | ns |
| $t_{pd1}$ | A,B,C,orD(3 levels) | W | | | 23 | 35 | ns |
| $t_{pd0}$ | STROBE | Y | | | 19 | 30 | ns |
| $t_{pd1}$ | STROBE | Y | $C_L$ = 15pF, $R_L$ = 400Ω | | 35 | 52 | ns |
| $t_{pd0}$ | STROBE | W | | | 21 | 30 | ns |
| $t_{pd1}$ | STROBE | W | | | 15.5 | 24 | ns |
| $t_{pd0}$ | $D_0$ thru $D_7$ | Y | | | 16 | 24 | ns |
| $t_{pd1}$ | $D_0$ thru $D_7$ | Y | | | 19 | 29 | ns |
| $t_{pd0}$ | $E_0$ thru $E_{15}$ | W | | | 8.5 | 14 | ns |
| $t_{pd1}$ | $E_0$ thru $E_{15}$ | W | | | 13 | 20 | ns |

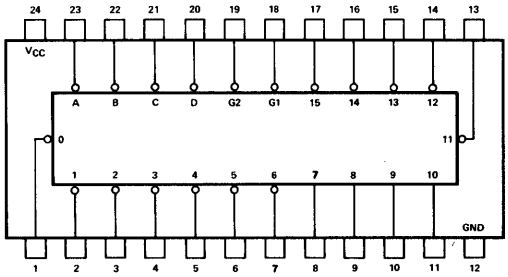
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N74154N,P**
**S54154N,P,Y**

# 4—Line to 16 Line Decoder/Demultiplexer

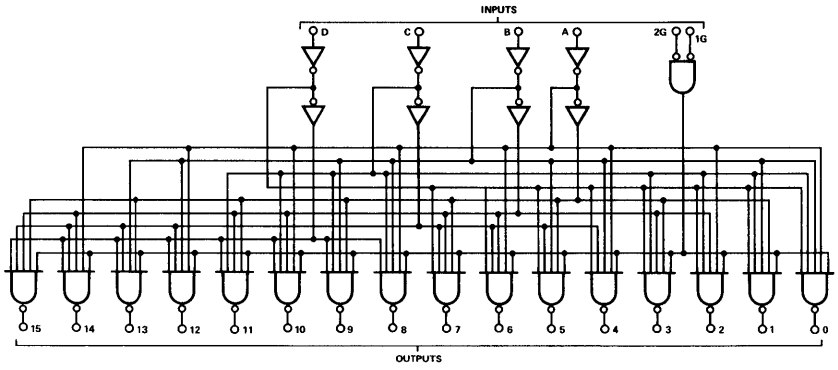



**N,Y,P PACKAGE**

## DESCRIPTION

The 54/74154 decodes 4 binary-coded inputs to one of 16 mutually exclusive outputs when each of the two strobe inputs are low. The demultiplexing function is achieved by using the 4 input lines for output addressing and data from one strobe input while the other strobe input is held low.

## LOGIC DIAGRAM




## TRUTH TABLE

| INPUTS | | | | | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | G2 | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 1 | 12 | 13 | 14 | 15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = high, L = low, X = irrelevant

## RECOMMENDED OPERATING CONDITIONS.

| | | S54154 | | | N74154 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Normalized fan-out from each output, N | Low logic level | | | 10 | | | 10 | |
| | High logic level | | | 20 | | | 20 | |
| Operating free-air temperature range | | -55 | 25 | 125 | 0 | 25 | 70 | °C |

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS* | | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = -800μA | | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 16mA | | | | 0.4 | V |
| $I_{IH}$ | High-level input current (each input) | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IL}$ | Low-level input current (each input) | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | $V_{CC}$ = MAX | S54154 | -20 | | -55 | mA |
| | | | N74154 | -18 | | -57 | |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX | S54154 | | 34 | 49 | mA |
| | | | N74154 | | 34 | 56 | |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

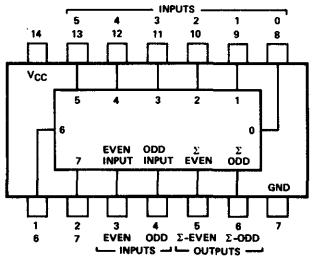
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic | $C_L$ = 15pF, $R_L$ = 400 | | 24 | 36 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic | | | 22 | 33 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output, from either strobe input | | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output, from either strobe input | | | 18 | 27 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

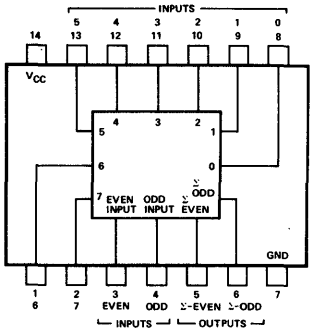
**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N74180A,Q** **8–Bit Odd/Even Parity**
**S54180A,Q,F** **Generator/Checker**




**A,F PACKAGE**

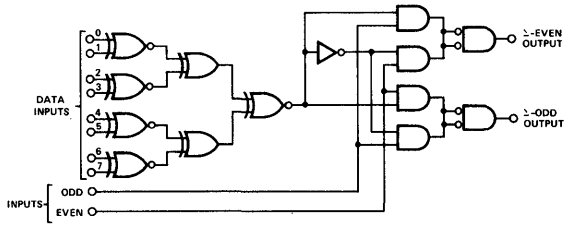



**Q PACKAGE**

## DESCRIPTION

The 54/74180 8-Bit Odd/Even Parity Generator/Checker is a TTL monolithic array featuring gating logic arranged to generate or check odd or even parity.

## LOGIC DIAGRAM




## TRUTH TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| Σ OF 1's AT 0 THRU 7 | EVEN | ODD | Σ EVEN | Σ ODD |
| EVEN | 1 | 0 | 1 | 0 |
| ODD | 1 | 0 | 0 | 1 |
| EVEN | 0 | 1 | 0 | 1 |
| ODD | 0 | 1 | 1 | 0 |
| X | 1 | 1 | 0 | 0 |
| X | 0 | 0 | 1 | 1 |

X = irrelevant

## RECOMMENDED OPERATING CONDITIONS.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ (See Note 1): | S54180 | 4.5 | 5 | 5.5 | V |
| | N74180 | 4.75 | 5 | 5.25 | V |
| Normalized Fan-Out from Each Output (N): | Logical 0 | | | 10 | V |
| | Logical 1 | | | 20 | V |

NOTE: 1. These voltage values are with respect to network ground terminal.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS* | | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{in(1)}$ | Input voltage required to ensure logical 1 at any input terminal | | $V_{CC}$ = MIN | | 2 | | | V |
| $V_{in(0)}$ | Input voltage required to ensure logical 0 at any input terminal | | $V_{CC}$ = MIN | | | | 0.8 | V |
| $V_{out(1)}$ | Logical 1 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, $I_{load}$ = -800μA | | 2.4 | | | V |
| $V_{out(0)}$ | Logical 0 output voltage | | $V_{CC}$ = MIN, $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V, $I_{sink}$ = 16mA | | | | 0.4 | V |
| $I_{in(1)}$ | Logical 1 level input current at each data input | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current at each data input | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -1.6 | mA |
| $I_{in(1)}$ | Logical 1 level input current at even or odd input | | $V_{CC}$ = MAX, $V_{in}$ = 2.4V | | | | 80 | μA |
| | | | $V_{CC}$ = MAX, $V_{in}$ = 5.5V | | | | 1 | mA |
| $I_{in(0)}$ | Logical 0 level input current at even or odd input | | $V_{CC}$ = MAX, $V_{in}$ = 0.4V | | | | -3.2 | mA |
| $I_{OS}$ | Short-circuit output current† | | $V_{CC}$ = MAX | S54180 | -20 | | -55 | mA |
| | | | | N74180 | -18 | | -55 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | S54180 | | 34 | 49 | mA |
| | | | | N74180 | | 34 | 56 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10**

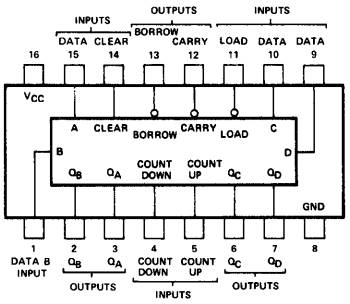
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{pd1}$ | Data | Σ Even | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 40 | 60 | ns |
| $t_{pd0}$ | Data | Σ Even | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 25 | 38 | ns |
| $t_{pd1}$ | Data | Σ Odd | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 32 | 48 | ns |
| $t_{pd0}$ | Data | Σ Odd | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 45 | 68 | ns |
| $t_{pd1}$ | Data | Σ Even | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 32 | 48 | ns |
| $t_{pd0}$ | Data | Σ Even | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 45 | 68 | ns |
| $t_{pd1}$ | Data | Σ Odd | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 40 | 60 | ns |
| $t_{pd0}$ | Data | Σ Odd | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 25 | 38 | ns |
| $t_{pd1}$ | Even or Odd | Σ Even or Σ Odd | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 13 | 20 | ns |
| $t_{pd0}$ | Even or Odd | Σ Even or Σ Odd | | $C_L$ = 15pF, | $R_L$ = 400Ω | | 7 | 10 | ns |

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

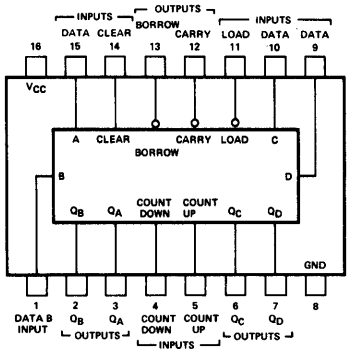
**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

**N74192B,R** **Synchronous Decade Up/Down**
**S54192B,R,E** **Counter with Preset Inputs**




**R PACKAGE**

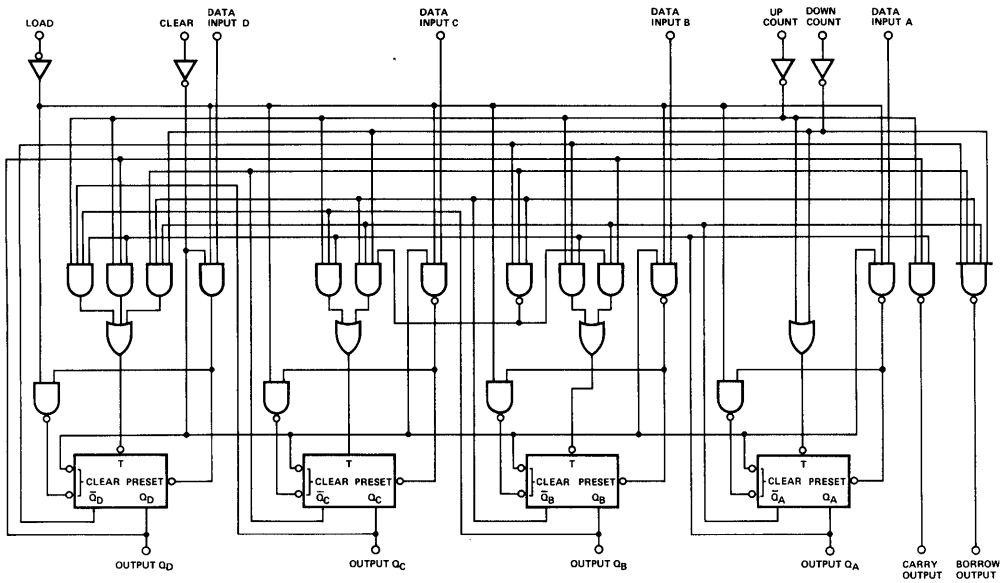



**B,E PACKAGE**

## DESCRIPTION

The 54/74192 Synchronous Decode Up/Down Counter with preset inputs is a TTL monolithic array containing gates and binaries interconnected to provide a bi-directional divide-by-ten sequence as a function of the clock inputs.
The counter is capable of being preset to any number of addressing the data inputs while the load input is low.

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS.

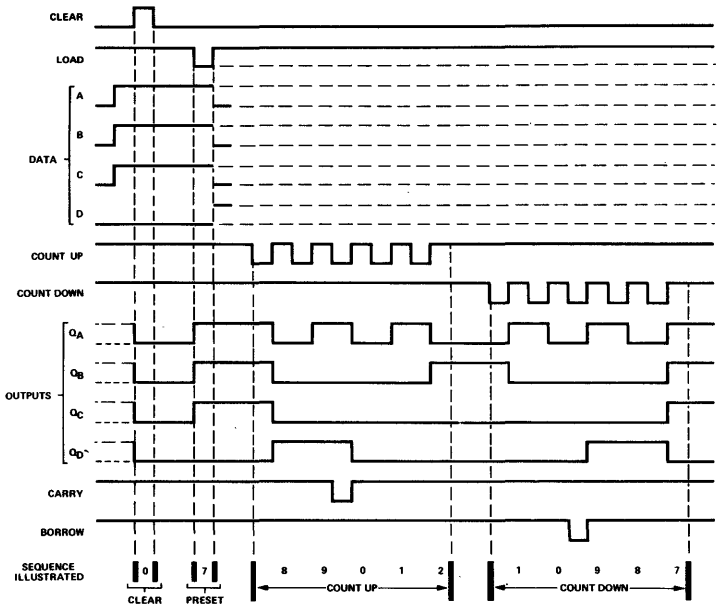
| | S54192 | | | N74192 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Normalized fan-out from each output, N | | | 10 | | | 10 | |
| Input count frequency, $f_{count}$ | 0 | | 25* | 0 | | 25* | MHz |
| Width of any input pulse, $t_w$ | 20* | | | 20* | | | ns |
| Data setup time, $t_{setup}$ (see Note 2) | 20* | | | 20* | | | ns |
| Data hold time, $t_{hold}$ (see Note 3) | 0 | | | 0 | | | ns |
| Operating free-air temperature range, $T_A$ | -55 | 25 | 125 | 0 | 25 | 70 | °C |

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at $V_{CC}$ = 5V, $T_A$ = 25°C.

**DECADE COUNTER (typical clear, load, and count sequences)**

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.




NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **S54192** | | | | | | | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = -400μA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | | $V_{CC}$ = MAX | -20 | | -65 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | | 65 | 89 | mA |

**ELECTRICAL CHARACTERISTICS (Cont'd)**

| PARAMETER | | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
|---|---|---|---|---|---|---|
| **N74192** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = -400μA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | $V_{CC}$ = MAX | -18 | | -65 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX | | 65 | 102 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10 (See Note)**

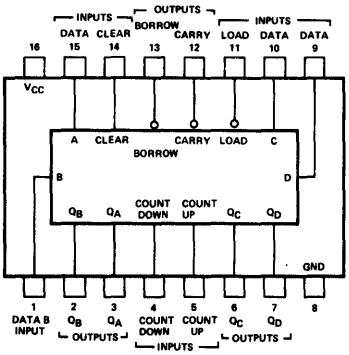
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum input count frequency | $C_L$ = 15pF, $R_L$ = 400Ω | 25 | 32 | | MHz |
| $t_{setup}$ | Minimum input setup time | | | 14 | 20 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level carry output from count-up input | | | 17 | 26 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level carry output from count-up input | | | 16 | 24 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level borrow output from count-down input | | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation delay time, high-to low-level borrow output from count-down input | | | 16 | 24 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output from either count input | | | 25 | 38 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q output from either count input | | | 31 | 47 | ns |

NOTE: Above Switching Table Applies to (S54192 & N74192)

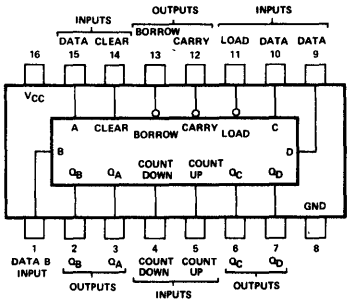
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

† Not more than one output should be shorted at a time.




R PACKAGE




B,E PACKAGE

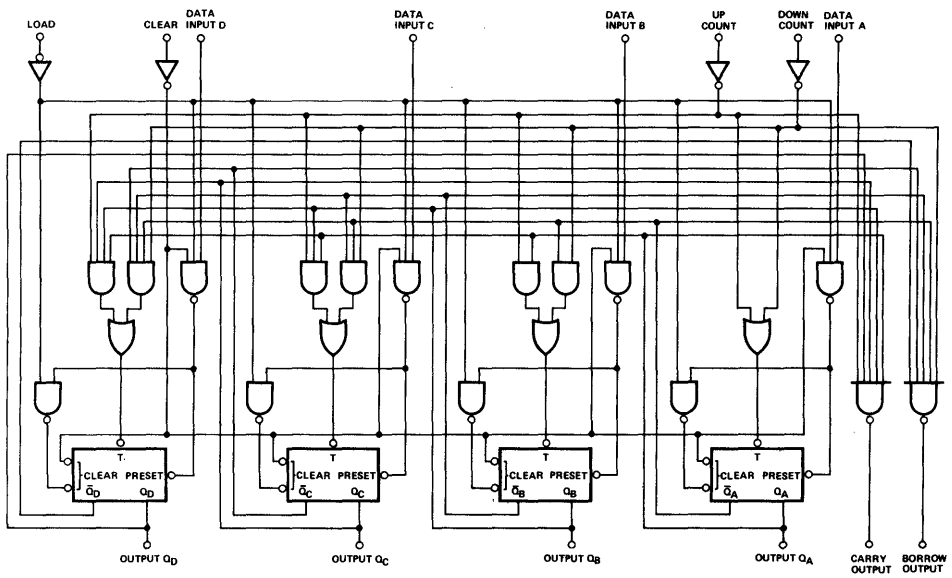
**Synchronous 4–Bit Binary Up/Down Counter with Preset Inputs**

**N74193B,R**
**S54193B,R,E**

## DESCRIPTION

The 54/74193 Synchronous 4-Bit Binary Up/Down Counter with preset inputs is a TTL monolithic array containing gates and binaries interconnected to provide a bi-directional divide-by-sixteen sequence as a function of the clock inputs.
The counter is capable of being preset to any number by addressing the data inputs while the load input is low.

## LOGIC DIAGRAM




## RECOMMENDED OPERATING CONDITIONS.

| | S54193 | | | N74193 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Normalized fan-out from each output, N | | | 10 | | | 10 | |
| Input count frequency, $f_{count}$ | 0 | | 25* | 0 | | 25* | MHz |
| Width of any input pulse, $t_w$ | 20* | | | 20* | | | ns |
| Data setup time, $t_{setup}$ (see Note 2) | 20* | | | 20* | | | ns |
| Data hold time, $t_{hold}$ (see Note 3) | 0 | | | 0 | | | ns |
| Operating free-air temperature range, $T_A$ | -55 | 25 | 125 | 0 | 25 | 70 | °C |

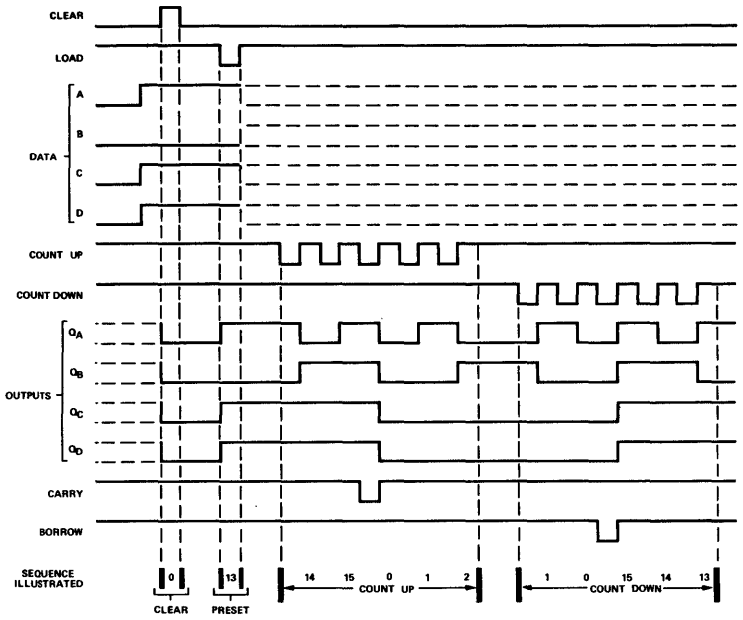
NOTES:

1. Voltage values are with respect to network ground terminal.
2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at $V_{CC}$ = 5V, $T_A$ = 25°C.

**BINARY COUNTER (typical clear, load, and count sequences)**

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.




NOTES:
A. Clear overides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

**ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **S54193** | | | | | | | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = -400μA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | | $V_{CC}$ = MAX | -20 | | -65 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | | 65 | 89 | mA |

**ELECTRICAL CHARACTERISTICS (Cont'd)**

| PARAMETER | | | TEST CONDITIONS* | MIN** | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **N74193** | | | | | | | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = 0.8V, $I_{OH}$ = -400μA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2V $V_{IL}$ = 0.8V, $I_{OL}$ = 16mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = MAX, $V_I$ = 2.4V | | | 40 | μA |
| | | | $V_{CC}$ = MAX, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = MAX, $V_I$ = 0.4V | | | -1.6 | mA |
| $I_{OS}$ | Short-circuit output current† | | $V_{CC}$ = MAX | -18 | | -65 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX | | 65 | 102 | mA |

**SWITCHING CHARACTERISTICS, $V_{CC}$ = 5V, $T_A$ = 25°C, N = 10 (See Note)**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum input count frequency | | $C_L$ = 15pF, $R_L$ = 400Ω | 25 | 32 | | MHz |
| $t_{setup}$ | Minimum input setup time | | | | 14 | 20 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level carry output from count-up input | | | | 17 | 26 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level carry output from count-up input | | | | 16 | 24 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level borrow output from count-down input | | | | 16 | 24 | ns |
| $t_{PHL}$ | Propagation delay time, high-to low-level borrow output from count-down input | | | | 16 | 24 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level Q output from either count input | | | | 25 | 38 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level Q output from either count input | | | | 31 | 47 | ns |

NOTE: Above Switching Table Applies to (S54193 & N74193)

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.

†Not more than one output should be shorted at a time.

# See Signetics for Line Driving and Receiving Capability

**Low Impedance Transmission Lines:**

**8T13** - Dual Line Driver for driving 50Ω to 500Ω cable

**8T14** - Triple Line Receiver with high input impedance (> 20k) plus hysteresis

**Communications Equipment**

**8T15** - Dual Line Driver (±25 Volt output protection)

**8T16** - Dual Line Receiver with hysteresis control

**Inter-Board Interfacing:**

**SP357** - Quad 2-Input NAND Driver (100mA)

**SP358** - Quad 2-Input NAND Driver with Bare Collector (100mA)

**SP380** - Quad 2-Input NOR/High Input Impedance

**SP381** - Quad 2-Input NOR/High Input Impedance

**SP391** - Hex Inverter/High Input Impedance

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