SIGNETICS DIGITAL 54/7400 DATA BOOK

SIGNETICS DIGITAL 54/74 TTL SERIES

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54/74 FAMILY LINES (Cont'd)

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8200 MSI FAMILY LINES

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8200 MSI FAMILY LINES (Cont'd)

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8T04	Seven-Segment Decoder/Driver (Active low -40mA current sink)
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8242	4-Bit Comparator
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8224	256 Bit ROM
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8228	4096 Bit ROM
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8T01	Nixie* Decoder/Driver (68V, 5mA)
8T04	Seven-Segment Decoder/Driver (Active low -40mA current sink)
8T05	Seven-Segment Decoder/Driver (Active high -2.5mA current source)
8T06	Seven-Segment Decoder/Driver (Active high - bare collector)
8T09	Quad Bus Driver
8T10	Quad D-Type Bus Flip-Flop
8T13	Dual Line Driver
8T14	Triple Line Receiver
8T15	Dual Communications Line Driver
8T16	Dual Communications Line Receiver
8T18	Dual 2-Input NAND Interface Gate
8T23	Dual Line Driver (IBM Compatible)
8T24	Triple Line Receiver (IBM Compatible)
8T80	Quad 2-Input NAND Interface Gate
8T90	Hex Inverter Interface Element

74S TO BE ANNOUNCED

74S10 Triple 3 NAND Gate
74S11 Triple 3 NAND Gate
74S15 Triple 3 NAND Gate with open collector
74S64 4-2-3-2 AND-OR-Invert Gate
74S65 4-2-3-2 AND-OR-Invert Gate with open collector
74S74 Dual D Flip-Flop

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General Information
54/74 Logic Families

GENERAL DESCRIPTION

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7V
Input Voltage, V_{in} (See Note 1	5.5V
Interemitter Voltage (See Note 2)	5.5V
Resistor Node Voltage, 54121, 74121 (See Note 1)	-5.5V to 7V
Operating Free-Air Temperature Range:	
Series 54 Circuits	-55°C to 125°C
Series 74 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

Series 54/74 Logic Family
The 54/74XX logic family is medium speed TTL, and high speed TTL integrated circuits. The family includes a multiple number of functions in a variety of packages. The 54XX devices are characterized for the full military temperature range of -55°C to +125°C. The 74XX devices are characterized for the limited temperature range of 0°C to +70°C.

INPUT CLAMPING DIODES
Although not shown on all schematic diagrams, all of these SSI circuits incorporate input diodes. Each clamping diode is capable of limiting negative excursions at the input to a maximum of 1.5 volts below ground, even if -12mA of current is drawn.

DESIGN CONSIDERATIONS

Logic Definition

Series 54/74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:
LOW VOLTAGE = LOGICAL "0"
HIGH VOLTAGE = LOGICAL "1"

Unused Inputs
For optimum switching times and minimum noise susceptibility unused inputs should be maintained at a positive voltage greater than 2.4V but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package load, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to a supply voltage. Preferably, this voltage should be between 2.4V and 5.5V.
b. Connect unused inputs to a used input if maximum fanout of the driving output will not be exceeded. Each input presents a full load in the logical "1" state to the driving output.

Input-Current Requirements
Input-current requirements reflect worst-case V_{CC} and temperature condition. Currents into the input terminals are specified as positive values.

54/74 Logic
Each input of the multiple-emitter input transistor that utilizes a 4 KΩ resistor requires no more than -1.6 mA flow out of the input at a logical "0" voltage level; therefore, one load (N = 1) for 54/74 logic is -1.6 mA maximum. Each input requires current into the input at a logical "1" voltage level. This current is 40μA maximum for each emitter input.

Fanout Capability
Fanout reflects the ability of an output to sink current from a number of loads (N) at a logical "0" voltage level and to supply current at a logical "1" voltage level. Each standard 54/74 output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate (54/7440) is capable of sinking current or supplying current to 30 loads (N = 30).

ELECTRICAL CHARACTERISTICS
These are guaranteed over the applicable operating free-air temperature range, unless otherwise noted, as shown in Section 2 of the handbook.

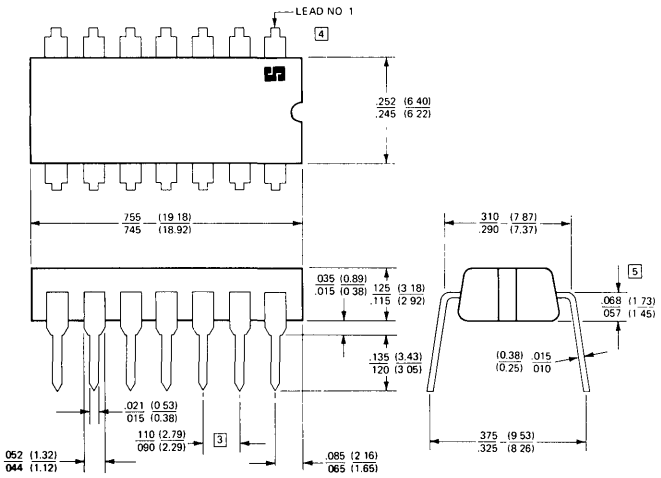
NOTE
Any product available in an A or B package can also be supplied in the F cer-dip package.

SECTION 1

PHYSICAL DIMENSIONS

A PACKAGE (TO-116)

14 Pin dual in-line, molded

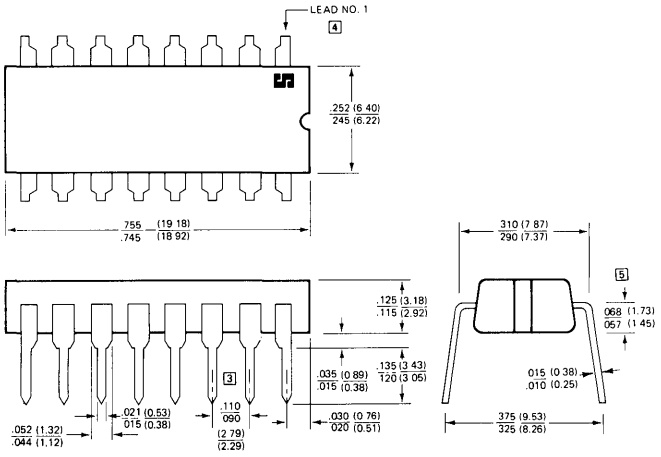


NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

B PACKAGE

16 Pin dual in-line, molded



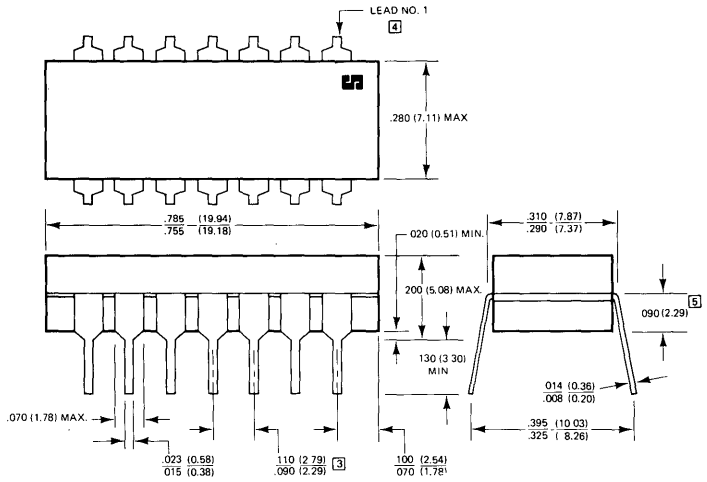
NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: Θ Ja = .16 C/mW, Θ Jc = .08 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

PHYSICAL DIMENSIONS (Cont'd)

F PACKAGE

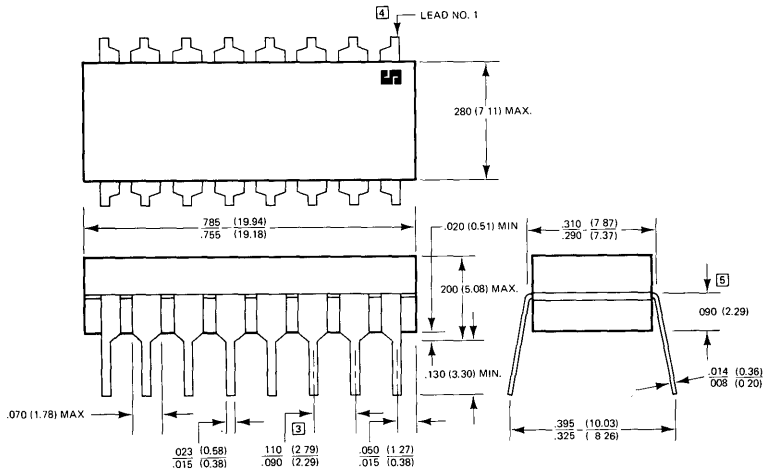
14 Lead dual in-line



NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Ja = .065°C/mW, Θ Jc = .020°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

F PACKAGE

16 Lead dual in-line

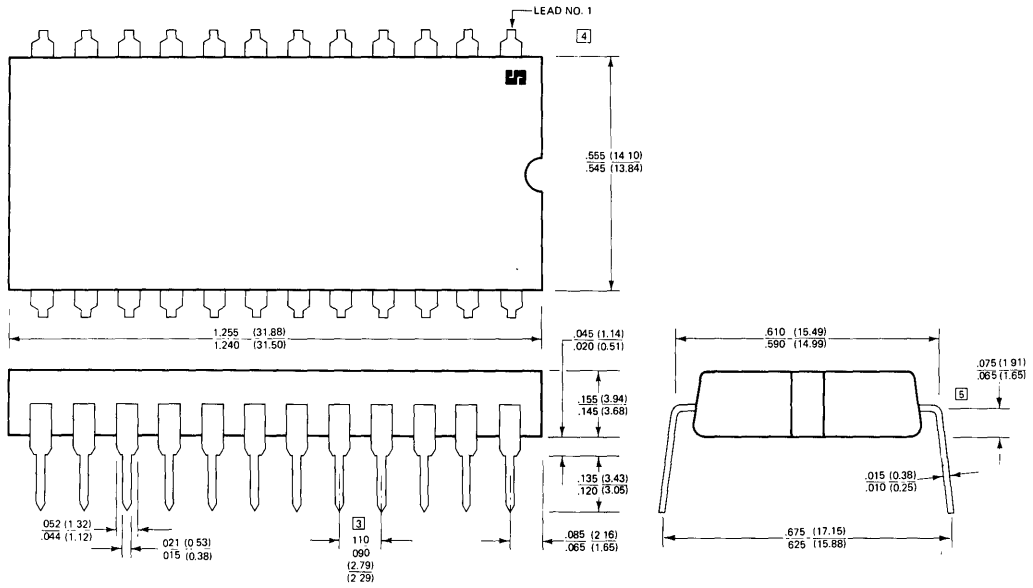


NOTES:
1. LEAD MATERIAL: KOVAR OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL.
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. THERMAL RESISTANCE: Θ Ja = .090°C/mW, Θ Jc = .023°C/mW.
7. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

PHYSICAL DIMENSIONS (Cont'd)

N PACKAGE

24 Pin dual in-line, molded

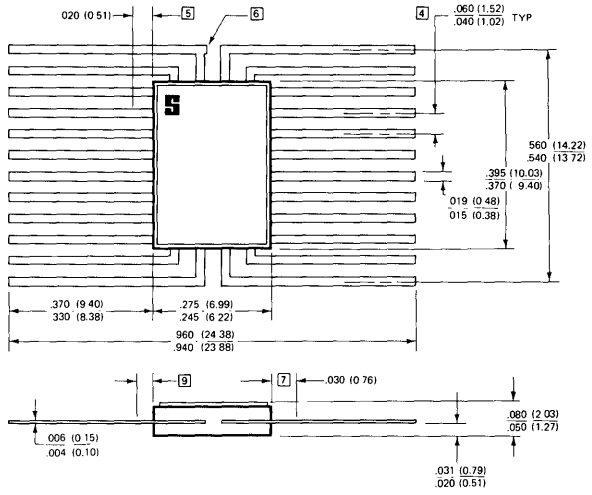


NOTES:

1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT.
2. BODY MATERIAL: SILICONE MOLDED
3. TOLERANCES NON CUMULATIVE.
4. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. BODY DIMENSIONS DO NOT INCLUDE MOLDING FLASH.
7. THERMAL RESISTANCE: ⊖ Ja = .12°C/mW, ⊖ Jc = .05 C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

Q PACKAGE

24 Pin flat ceramic

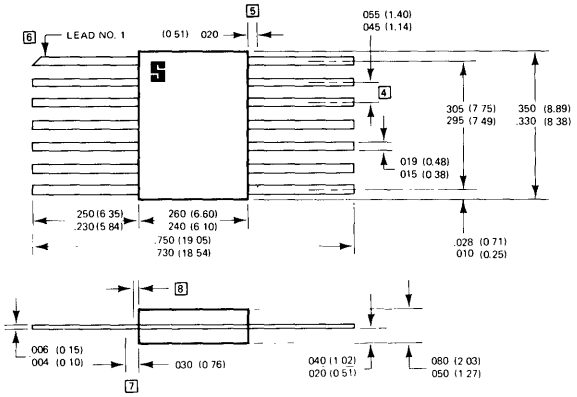


NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. THERMAL RESISTANCE: ⊖ Ja = .150°C/mW, ⊖ Jc = .050°C/mW.
9. MAXIMUM GLASS CLIMB, LID SKEW, OR FRIT SQUEEZE OUT IS .010.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE

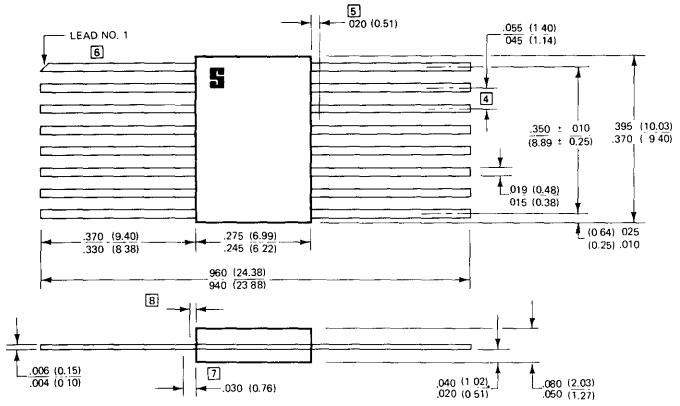
14 Pin flat cerpac



NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. MAXIMUM GLASS CLIMB .010.
9. THERMAL RESISTANCE: Θ Ja = .200°C/mW, Θ Jc = .085°C/mW.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

W PACKAGE

16 Pin flat cerpac

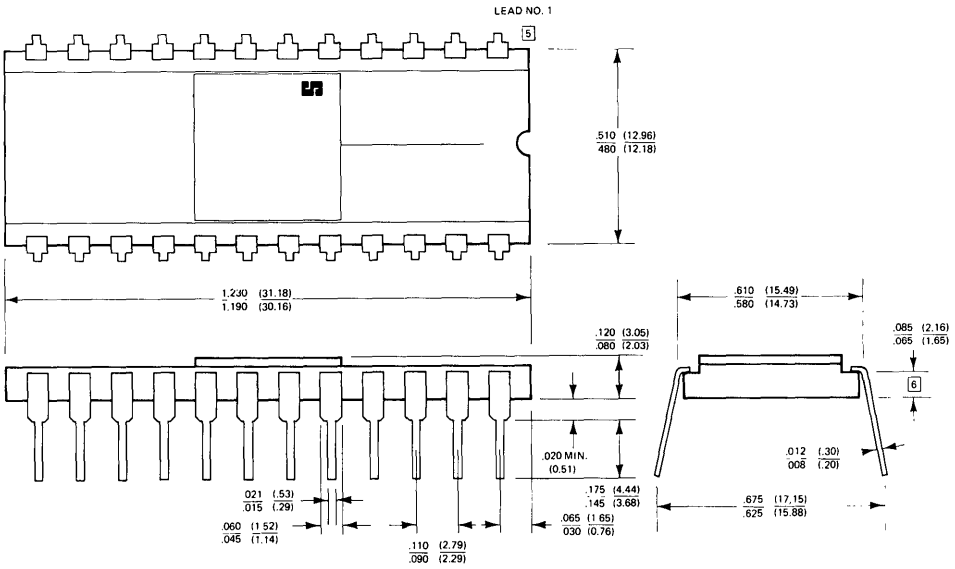


NOTES:
1. LEAD MATERIAL: ALLOY 42 OR EQUIVALENT, TIN PLATED.
2. BODY MATERIAL: CERAMIC WITH GLASS SEAL AT LEADS.
3. LID MATERIAL: CERAMIC, GLASS SEAL.
4. TOLERANCES NON CUMULATIVE.
5. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
6. SIGNETICS SYMBOL OR ANGLE CUT DENOTES LEAD NO. 1.
7. RECOMMENDED MINIMUM OFFSET BEFORE LEAD BEND.
8. MAXIMUM GLASS CLIMB .010.
9. THERMAL RESISTANCE: Θ Ja = .200 C/mW, Θ Jc = .085 C/mW.
10. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

PHYSICAL DIMENSIONS (Cont'd)

F PACKAGE

24 Pin dual in-line, ceramic

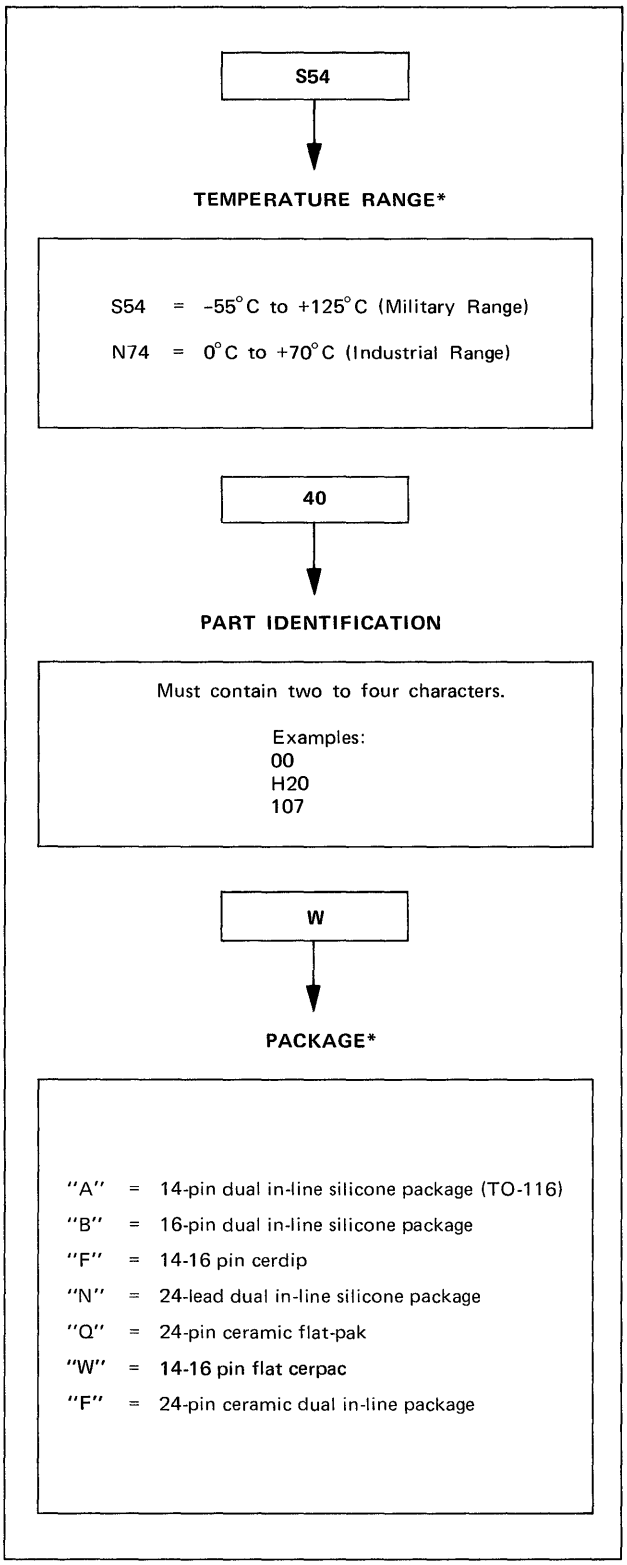


NOTES:

1. LEAD MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED.
2. BODY MATERIAL: CERAMIC WITH KOVAR OR EQUIVALENT.
3. LID MATERIAL: KOVAR OR EQUIVALENT, GOLD PLATED, ALLOY SEAL.
4. TOLERANCES NON CUMULATIVE.
5. SIGNETICS SYMBOL DENOTES LEAD NO. 1.
6. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
7. THERMAL RESISTANCE: Θ Ja = .050°C/mW, Θ Jc = .010°C/mW.
8. ALL DIMENSIONS SHOWN IN PARENTHESES ARE METRIC EQUIVALENTS. (MILLIMETERS)

54XX/74XX
Electrical Characteristics

ORDERING INSTRUCTIONS



*Availability of a circuit device in a particular package and temperature range is indicated on the appropriate device. Electrical Characteristics Data Sheet is shown in Section 2 of this handbook.

Manufacturer reserves the right to make design and process changes and improvements.

SECTION 2

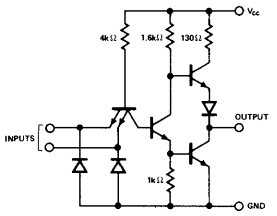
QUADRUPLE 2-INPUT POSITIVE NAND GATE

S5400 N7400

S5400–A,F,W • N7400–A,F

DIGITAL 54/74 TTL SERIES

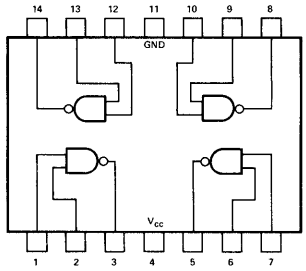
SCHEMATIC (each gate)



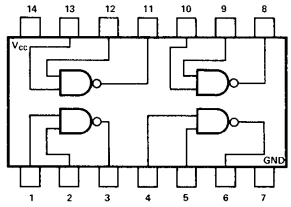
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5400 Circuits		4.5	5	5.5	V
N7400 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5400 Circuits	-55	25	125	°C
	N7400 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5400	-20		-55	mA
				N7400	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		11	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

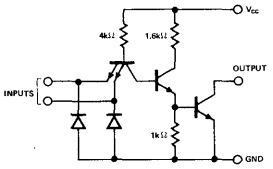
QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S5401 N7401

S5401–A,F,W • N7401–A,F

DIGITAL 54/74 TTL SERIES

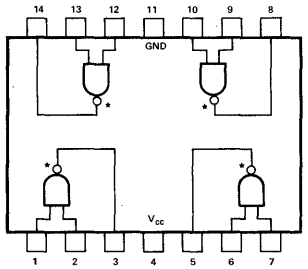
SCHEMATIC (each gate)



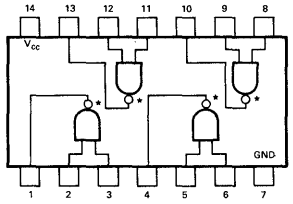
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



★ No pull-up provided

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5401 Circuits	4.5	5	5.5	V
	N7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5401 Circuits	-55	25	125	°C
	N7401 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	$V_{in(0)}$ = 0.8V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX	V_{in} = 0		4	8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 4 kΩ		35	45	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

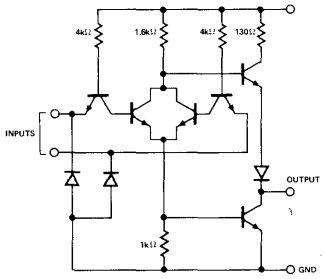
QUADRUPLE 2-INPUT POSITIVE NOR GATE

S5402
N7402

S5402–A,F,W • N7402–A,F

DIGITAL 54/74 TTL SERIES

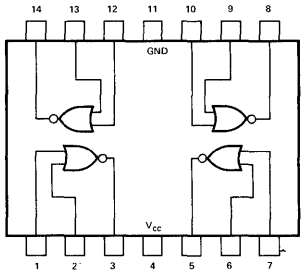
SCHEMATIC (each gate)



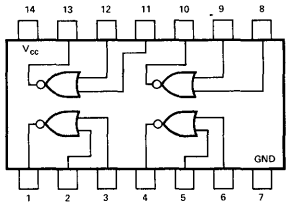
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5402 Circuits	4.5	5	5.5	V
	N7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5402 Circuits	-55	25	125	°C
	N7402 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output Current†	V_{CC} = MAX		S5402 N7402	-20 -18		-55 -55	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		8	16	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

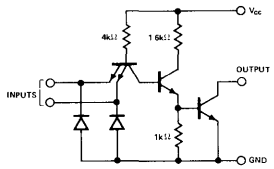
QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S5403 N7403

S5403–A,F • N7403–A,F

DIGITAL 54/74 TTL SERIES

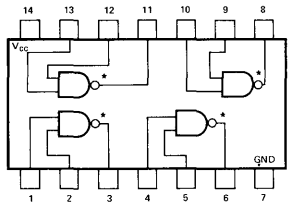
SCHEMATIC (each gate)



NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

A,F PACKAGE



★ No pull-up provided

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5403 Circuits		4.5	5	5.5	V
N7403 Circuits		4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5403 Circuits	-55	25	125	°C
	N7403 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN,	V_{in} = 0.8V			0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 2V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			40	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	8	mA

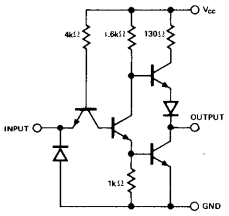
SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C,

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 4 kΩ		35	45	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

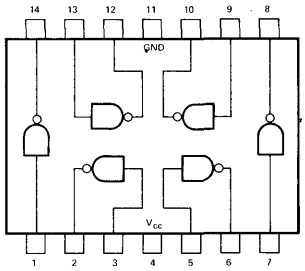
SCHEMATIC (each inverter)



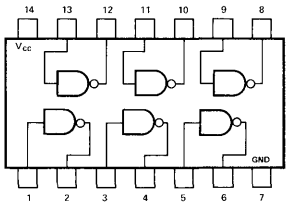
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5404 Circuits	4.5	5	5.5	V
N7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A: S5404 Circuits	-55	25	125	°C
N7404 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5404	-20		-55	mA
				N7404	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		6	12	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

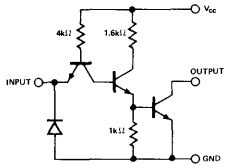
HEX INVERTER WITH OPEN COLLECTOR OUTPUT

S5405 N7405

S5405–A,F,W • N7405–A,F

DIGITAL 54/74 TTL SERIES

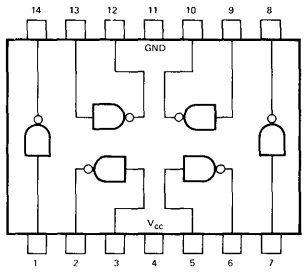
SCHEMATIC (each inverter)



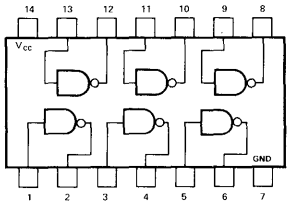
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5405 Circuits	4.5	5	5.5	V
	N7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5405 Circuits	-55	25	125	°C
	N7405 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			40 1	μA mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = 5V, T_A = 25°C	V_{in} = 5V,		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = 5V, T_A = 25°C	V_{in} = 0,		6	12	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 4 kΩ		40	55	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C

HEX INVERTER BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5406
S5416
N7406
N7416

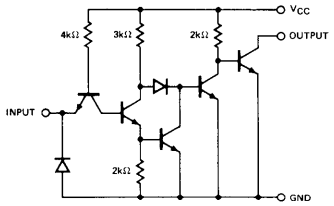
S5406–A,F,W • S5416–A,F,W • N7406–A,F • N7416–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7406 and 54/7416 Hex Inverter Buffer/Drivers features standard TTL inputs with inverted high voltage, high current, open collector outputs for interface with MOS, lamps or relays. The 54/7406 minimum output breakdown is 30 volts and the 54/7416 minimum output breakdown is 15 volts.

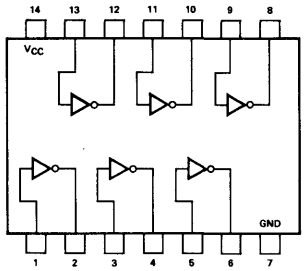
SCHEMATIC (each inverter)



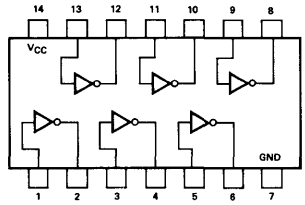
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A, F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5406, S5416			N7406, N7416			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, V_{OH}: S5406, N7406			30			30	V
S5416, N7416			15			15	V
Low-level output current, I_{OL}			30			40	mA
Operating Free-air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_I = 0.8V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2V, I_{OL} = MAX			0.7	V
		V_{CC} = MIN, V_I = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_I = 5V		27	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 110 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF, R_L = 110 Ω		14	23	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

HEX BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5407
S5417
N7407
N7417

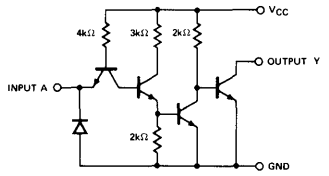
S5407–A,F,W • S5417–A,F,W • N7407–A,F • N7417–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7407 and 54/7417 Hex Buffer/Driver features standard TTL inputs with non-inverted high voltage, high current open collector outputs for interface with MOS, lamps or relays. The 54/7407 minimum output is 30 volts and the 54/7417 minimum output is 15 volts.

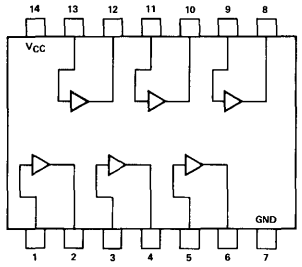
SCHEMATIC (each buffer/driver)



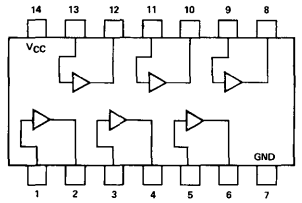
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5407, S5417			N7407, N7417			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, V_{OH}: S5407, N7407			30			30	
S5417, N7417			15			15	V
Low-Level Output Current, I_{OL}			30			40	mA
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_1 = 2V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_1 = 0.8V, I_{OL} = MAX			0.7	V
		V_{CC} = MIN, V_1 = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_1 = 2.4V			40	μA
		V_{CC} = MAX, V_1 = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_1 = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_1 = 5V		29	41	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_1 = 0		21	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 110Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF, R_L = 110Ω		20	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

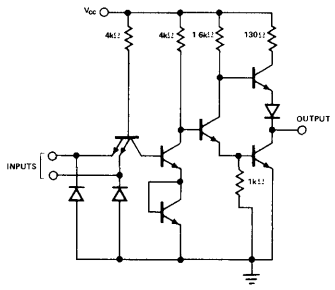
QUADRUPLE 2-INPUT POSITIVE AND GATES

S5408 N7408

S5408–A,F,W • N7408–A,F

DIGITAL 54/74 TTL SERIES

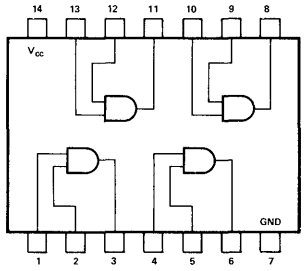
SCHEMATIC (each gate)



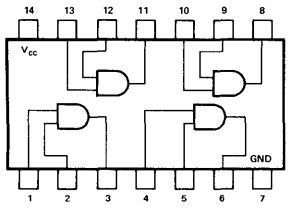
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5408 Circuits	4.5	5	5.5	V
	N7408 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5408 Circuits	-55	25	125	°C
	N7408 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800μA	V_{in} = 2.0V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 0.8V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5408	-20		-55	mA
				N7408	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 5V		10	15	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		18	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		12	19	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		17.5	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C
† Not more than one output should be shorted at a time.

QUAD 2-INPUT AND GATE WITH OPEN COLLECTOR OUTPUTS

S5409 N7409

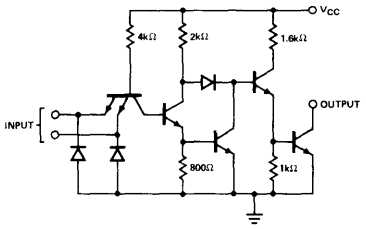
S5409–A,F,W • N7409–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7409 Quad 2-Input AND Gate with open collector outputs provides the capability of expanding AND logic functions.

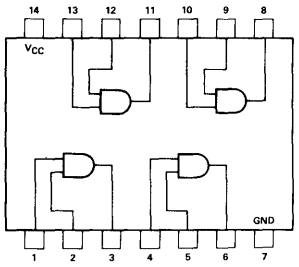
SCHEMATIC (each gate)



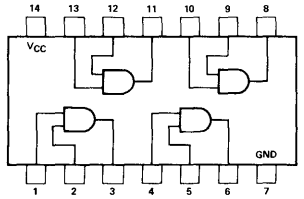
NOTE: Component values shown are nominal

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5409			N7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2V, V_{OH} = 5.5V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_I = 5V		10	15	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_I = 0		18	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N =10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 400 Ω		16	24	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at V_{CC} = 5V, T_A = 25°C.

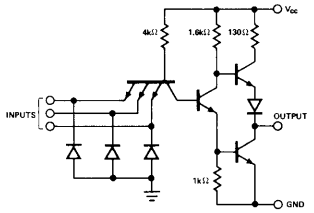
TRIPLE 3-INPUT POSITIVE NAND GATE

S5410
N7410

S5410—A,F,W • N7410—A,F

DIGITAL 54/74 TTL SERIES

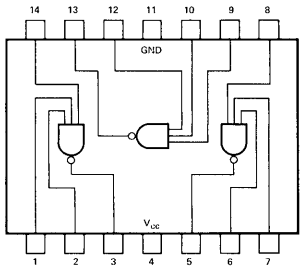
SCHEMATIC (each gate)



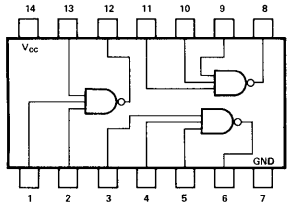
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5410 Circuits		4.5	5	5.5	V
N7410 Circuits		4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5410 Circuits	-55	25	125	°C
	N7410 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = 5.5V		S5410	-20		-55	mA
				N7410	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		3	6	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		7	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		11	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC}= 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

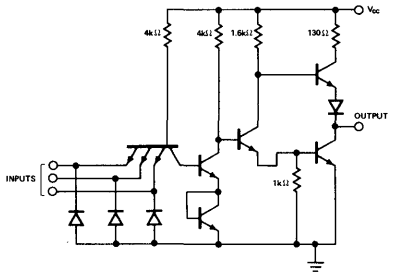
TRIPLE 3-INPUT POSITIVE AND GATE

S5411
N7411

S5411–A,F,W • N7411–A,F

DIGITAL 54/74 TTL SERIES

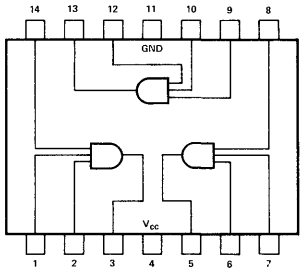
SCHEMATIC DIAGRAM



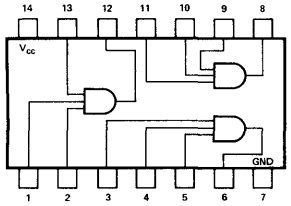
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5411 Circuits		4.5	5	5.5	V
N7411 Circuits		4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5411 Circuits	-55	25	125	°C
	N7411 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800μA	V_{in} = 2.0V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 0.8V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX	V_{in} = 2.4V				40	μA
		V_{CC} = MAX	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5411	-20		-55	mA
				N7411	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 5V		7.5	12	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		13.5	20	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		12	19	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		17.5	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C
† Not more than one output should be shorted at a time.

DUAL NAND SCHMITT TRIGGER

S5413
N7413

S5413–A,F,W • N7413–A,F

DIGITAL 54/74 TTL SERIES

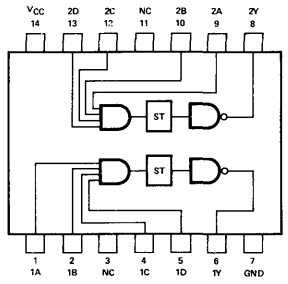
DESCRIPTION

The 5413 and 7413 dual Schmitt triggers consist of two identical Schmitt-trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a four-input NAND gate, but because of the Schmitt action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, or backlash, which is the difference between the two threshold levels, is typically 800mV.

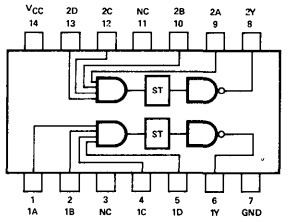
An important design feature is the built-in temperature compensation which ensures very high stability of the threshold levels and the hysteresis over a very wide temperature range. Typically, the hysteresis changes by 3% over the temperature range of −55°C to 125°C and the upper threshold changes by 1% over the same range. The 5413/7413 can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. It can not be triggered from straight dc levels.

These circuits are fully compatible with most other TTL, DTL, or MSI circuits. The 5413 is characterized for operation over the full military temperature range of −55°C to 125°C; the 7413 is characterized for operation from 0°C to 70°C.

W PACKAGE



A, F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	5413			7413			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Fan-Out From Each Output, N — High Logic Level			20			20	
Fan-Out From Each Output, N — Low Logic Level			10			10	
Operating Free-Air Temperature Range, T_A	-55	0	125	0	25	70	°C
Maximum Input Rise and Fall Times	No Restriction			No Restriction			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_{CC} = 5V		1.5	1.7	2	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5V		0.6	0.9	1.1	
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5V		0.4	0.8		V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -800μA	V_I = 0.6V,	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_I = 2V,		0.22	0.4	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5V,	$V_I = V_{T+}$		-0.65		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5V,	$V_I = V_{T-}$		-0.85		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V		-1	-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,		-18		-55	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	V_I = 0		14	23	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	V_I = 4.5V		20	32	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 400Ω		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 400Ω		15	22	ns

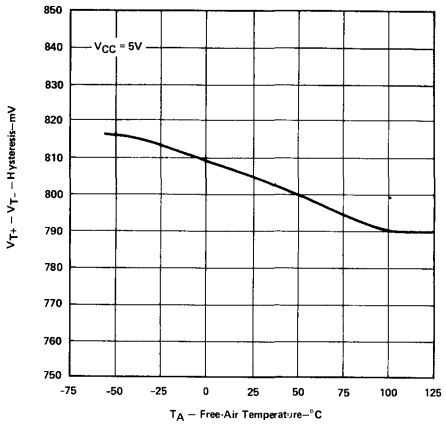
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

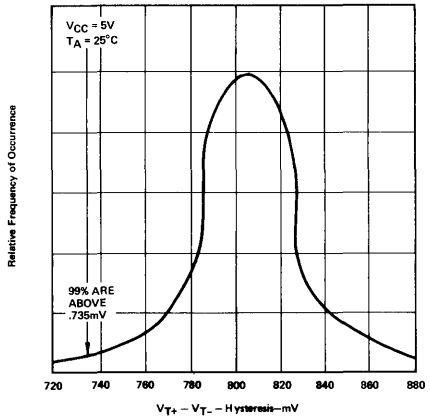
† Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

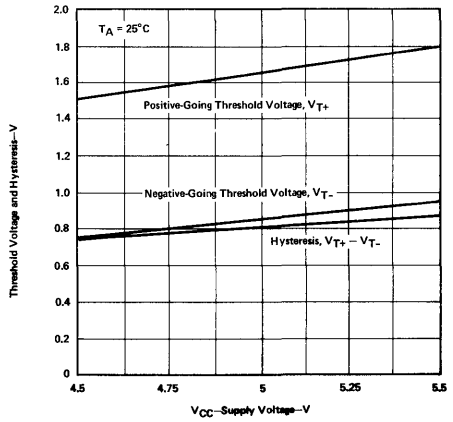
HYSTERESIS VS FREE-AIR TEMPERATURE



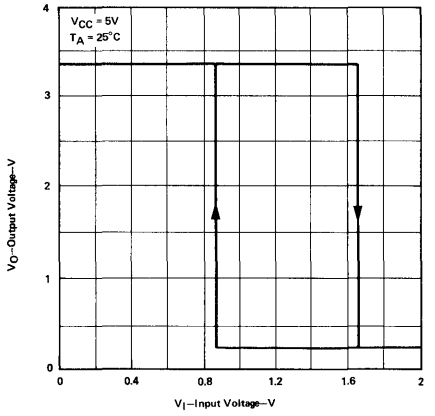
DISTRIBUTION OF UNITS FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS VS SUPPLY VOLTAGE



OUTPUT VOLTAGE VS INPUT VOLTAGE



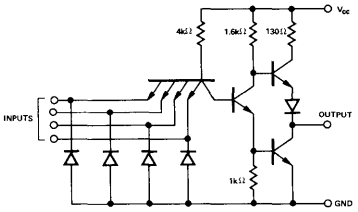
DUAL 4-INPUT POSITIVE NAND GATE

S5420
N7420

S5420—A,F,W • N7420—A,F

DIGITAL 54/74 TTL SERIES

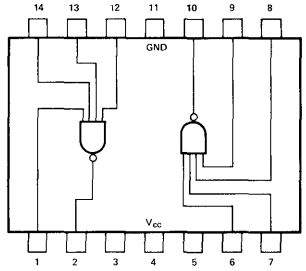
SCHEMATIC (each gate)



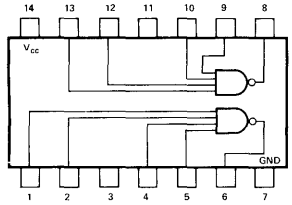
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5420 Circuits		4.5	5	5.5	V
N7420 Circuits		4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5420 Circuits	-55	25	125	°C
	N7420 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		S5420	-20		-55	mA
				N7420	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		2	4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		12	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

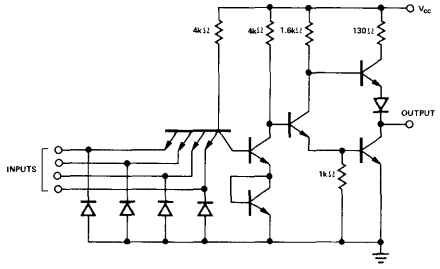
DUAL 4-INPUT POSITIVE AND GATE

S5421
N7421

S5421–A,F,W • N7421–A,F

DIGITAL 54/74 TTL SERIES

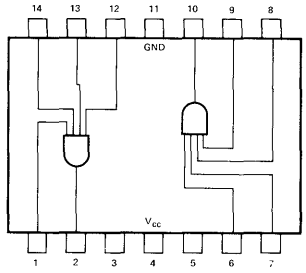
SCHEMATIC DIAGRAM



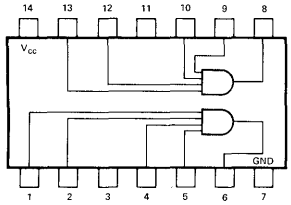
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5421 Circuits	4.5	5	5.5	V
	N7421 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5421 Circuits	-55	25	125	°C
	N7421 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -800μA	V_{in} = 2.0V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 0.8V			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output	V_{CC} = MAX,		S5421	-20		-55	mA
				N7421	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 5V		5	8	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		9	13	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		12	19	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		17.5	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC}= 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

QUAD 2-INPUT HIGH VOLTAGE NAND GATE

S5426
N7426

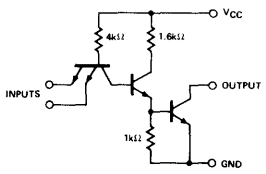
S5426–A,F • N7426–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7426 Quad 2-Input NAND Gate features standard TTL inputs with high voltage (15 volts) open collector outputs for interface with MOS, lamps or relays.

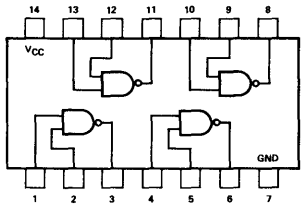
SCHEMATIC (each gate)



Note: Component values shown are nominal.

PIN CONFIGURATION

A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S5426			N7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
Output Voltage, V_{OH}			15			15	V
Low-Level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = 1mA	15			V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8V, V_{OH} = 12V			50	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_1 = 2.4V			40	μA
		V_{CC} = MAX, V_1 = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_1 = 0.4V			-1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, V_1 = 0		4	8	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, V_1 = 5V		12	22	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 1kΩ		16	24	ns
t_{PHL}	Propagation delay time high-to-low-level output	C_L = 15pF,	R_L = 1kΩ		11	17	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

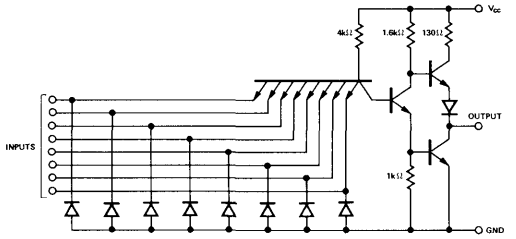
8-INPUT POSITIVE NAND GATE

S5430
N7430

S5430–A,F,W • N7430A,F

DIGITAL 54/74 TTL SERIES

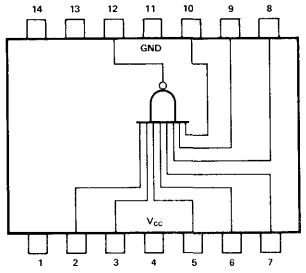
SCHEMATIC DIAGRAM



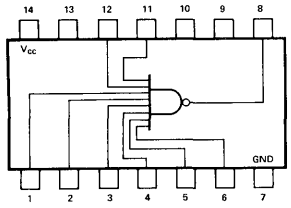
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5430 Circuits	4.5	5	5.5	V
N7430 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A: S5430 Circuits	-55	25	125	°C
N7430 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,		S5430	-20		-55	mA
				N7430	-18		-55	

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		3	6	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		1	2	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC}= 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

S5437–A,F,W • S5438–A,F,W • N7437–A,F,W • N7438–A,F

DIGITAL 54/74 TTL SERIES

S5437
S5438
N7437
N7438

DESCRIPTION

The S5437/N7437 is a NAND Gate (output low only when all inputs are high) the same as N7400 except that it will drive 3 times as many loads. The S5438/N7438 is also a NAND Gate but is open-collector similar to N7403. Each one is the same pinout.

The S5437/N7437 and S5438/N7438 contain four 2-input NAND gates in a package with a guaranteed fan-out of 30-Series 54/74 loads in both the logical "1" (1.2mA), and logical "0" (48mA) states. The S5438/N7438 has an open collector output for "WIRE–AND" applications but still retains the high sink current capability of the S5437/N7437.

ABSOLUTE MAXIMUM RATINGS (over operating temperature range unless otherwise noted)

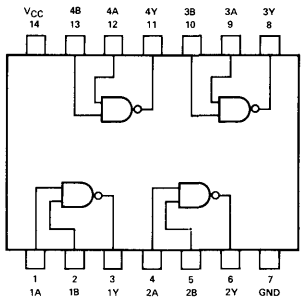
Supply Voltage V_{CC} (See Note 1)	7V
Input Voltage (See Note 1)	5.5V
Intermitter Voltage (See Note 2)	5.5V
Output Voltage (See Notes 1 and 3):	
S5438, N7438 Circuits	5.5V
Operating Free-Air Temperature Range:	
S5437, S5438 Circuits	-55°C to 125°C
N7437, N7438 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:

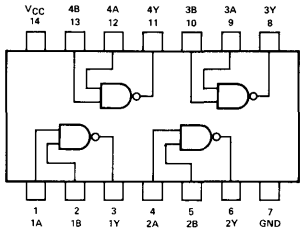
1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

PIN CONFIGURATIONS

W PACKAGE

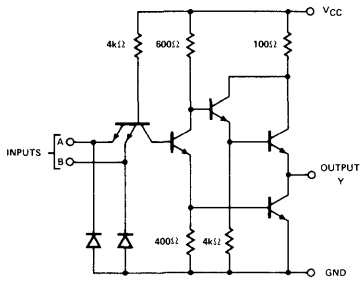


A,F PACKAGE

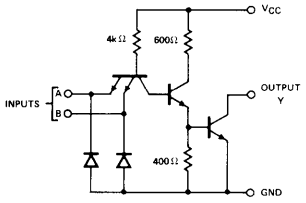


SCHEMATICS (each buffer)

S5437, N7437 (Totem-Pole Output)



S5438, N7438 (Open-Collector Output)



RECOMMENDED OPERATING CONDITIONS

	S5437, S5438			N7437, N7438			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			30			30	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = 1.2mA	V_{IH} = 2V,	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 48mA	V_{IL} = 0.8V,		0.22	0.4	V
I_I	Input current at max. input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX.	V_I = 2.4V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-20 -18		-55 -55	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		15	22	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		23	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 45pF,	R_L = 133Ω		13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output				8	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

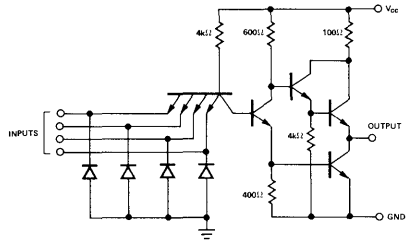
DUAL 4-INPUT POSITIVE NAND BUFFER

S5440
N7440

S5440–A,F,W • N7440–A,F

DIGITAL 54/74 TTL SERIES

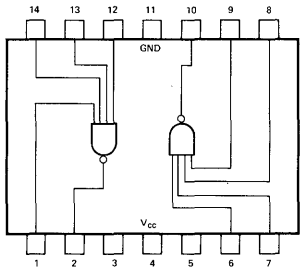
SCHEMATIC (each gate)



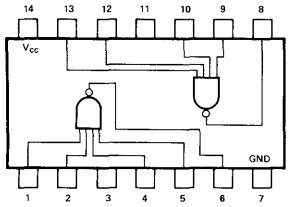
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5440 Circuits		4.5	5	5.5	V
N7440 Circuits		4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5440 Circuits	-55	25	125	°C
	N7440 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -1.2mA	V_{in} = 0.8V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 48mA	V_{in} = 2V,			0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		S5440	-20		-70	mA
				N7440	-18		-70	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V		17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4	6.8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 133Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 133Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC}= 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DESCRIPTION

The N7441B Nixie* Decoder/Driver is a one-out-of-ten decoder which has been designed to provide the necessary high voltage characteristics required for driving gas-filled cold-cathode indicator tubes.

It may also be utilized in driving relays or other high voltage interface circuitry. The element is designed using TTL techniques and is therefore completely compatible with DTL and TTL elements.

The specially designed output drivers provide the necessary stable output state. There are no input codes where all outputs are "off" or where more than one output can be turned "on".

RECOMMENDED OPERATING CONDITIONS

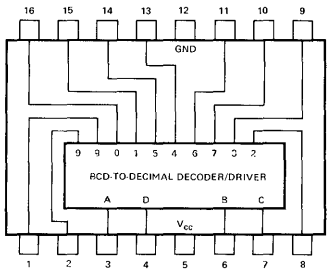
Supply Voltage V_{CC} (See Note 1)	4.75 to 5.25V
Maximum Voltage on any Output	70V

NOTE:

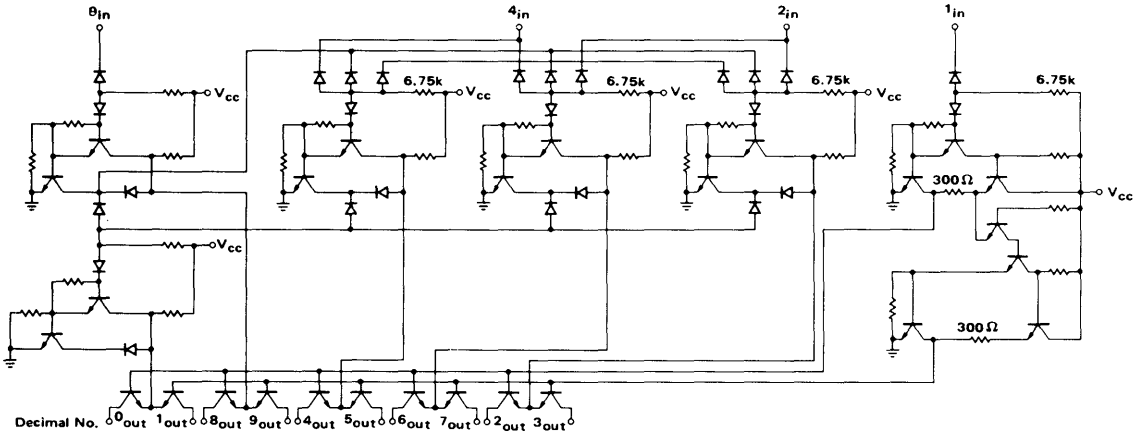
1. These voltage values are with respect to network ground terminal.

PIN CONFIGURATION

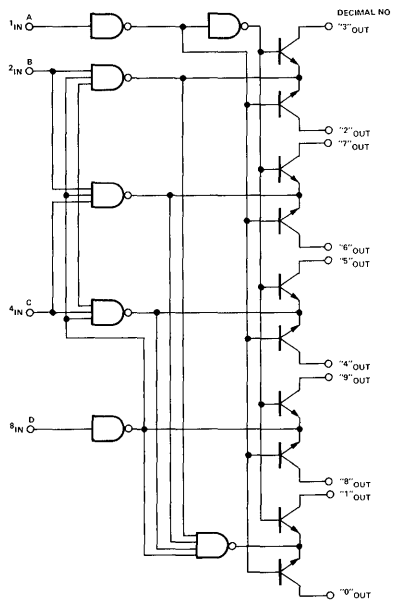
B PACKAGE



SCHEMATIC DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

† All other inputs are off.

ELECTRICAL CHARACTERISTICS, T_A = 0° C to 70° C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP*	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	V_{CC} = 4.75V		2			V
$V_{in(0)}$	Logical 0 input voltage	V_{CC} = 4.75V				0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.75V,	I_{on} = 7mA			2.5	V
I_{off}	Off-state reverse current	V_{CC} = 5.25V,	V_{out} = 55V			50	μA
		V_{CC} = 5.25V,	V_{out} = 70V			2	mA
$I_{in(1)}$	Logical 1 level input current at B, C, or D	V_{CC} = 5.25V,	V_{in} = 2.4V			40	μA
		V_{CC} = 5.25V,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at A	V_{CC} = 5.25V,	V_{in} = 2.4V			80	μA
		V_{CC} = 5.25V,	V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at B, C, or D	V_{CC} = 5.25V,	V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A	V_{CC} = 5.25V,	V_{in} = 0.4V			-3.2	mA
I_{CC}	Supply current	V_{CC} = 5.25V			21	42	mA

* All typical values are at V_{CC} = 5V, T_A = 25°C.

*Trademark Burroughs Corporation.

BCD-TO-DECIMAL DECODER

S5442
N7442

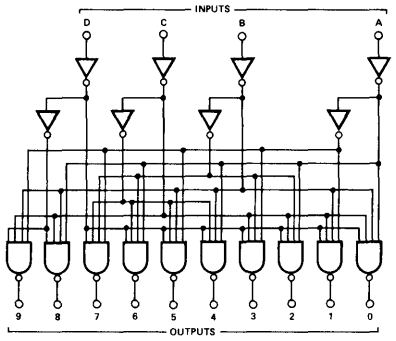
S5442–B,F,W • N7442–B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

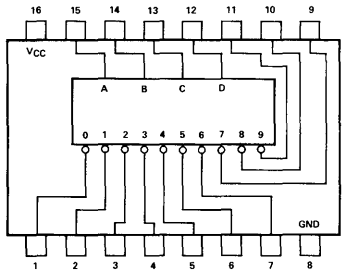
The 54/7442 BCD-to-Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7442 decodes a four bit BCD number to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5442/N7442 BCD INPUT

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5442 Circuits	4.5	5	5.5	V
N7442 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5442	-20		-55	mA
			N7442	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5442		28	41	mA
			N7442		18	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

EXCESS 3-TO-DECIMAL DECODER

S5443
N7443

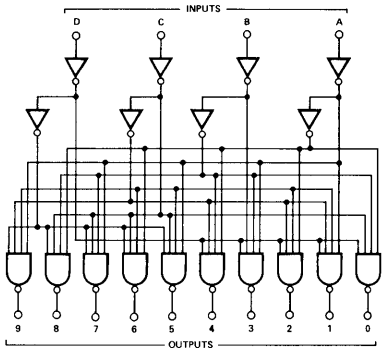
S5443–B,F,W • N7443–B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

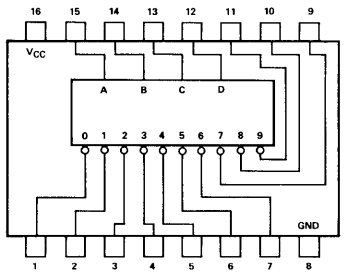
The 54/7443 Excess 3 Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion application. The 54/7443 decodes excess 3 code numbers to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5443/N7443 EXCESS INPUT

D	C	B	A
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0

ALL TYPES DECIMAL OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5443 Circuits	4.5	5	5.5	V
N7443 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5443	-20		-55	mA
			N7443	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5443		28	41	mA
			N7443		28	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

** All typical values are at V_{CC}= 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

EXCESS 3-GRAY-TO-DECIMAL DECODER

S5444
N7444

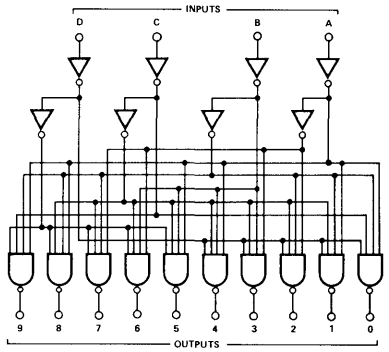
S5444–B,W • N7444–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

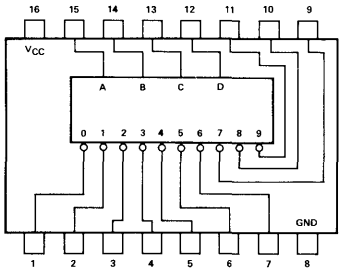
The 54/7444 Excess-3-Gray Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion applications. The 54/7444 decodes excess three gray code to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5444/N7444
EXCESS 3 GRAY
INPUT

D	C	B	A
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
0	0	0	0
0	0	0	1
0	0	1	1

ALL TYPES
DECIMAL
OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5444 Circuits	4.5	5	5.5	V
N7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$		V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S5444	-20		-55	mA
			N7444	-18		-55	mA
I_{CC}	Supply Current	V_{CC} = MAX,	S5444		28	41	mA
			N7444		28	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15pF,	R_L = 400Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15pF,	R_L = 400Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15pF,	R_L = 400Ω		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

BCD-TO-DECIMAL DECODER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

S5445 S54145 N7445 N74145

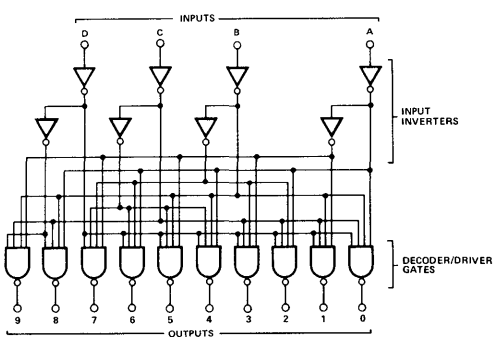
S5445–F,W • S54145–F,W • N7445–B • N74145–B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7445 and 54/74145 BCD-to-Decimal Decoder/Driver is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The 54/7445 minimum output breakdown is 30 volts and the 54/74145 minimum output breakdown is 15 volts.

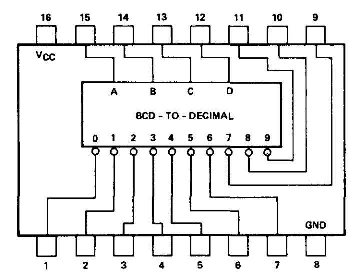
LOGIC DIAGRAM



NOTE: 1. These voltage values are with respect to network ground terminal.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S5445, S54145 Circuits	4.5	5	5.5	V
	N7445, N74145 Circuits	4.75	5	5.25	V
Voltage on any Output	S5445, N7445 Circuits			30	V
	S54145, N74145 Circuits			15	V

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
V_{on}	On-state output voltage	V_{CC} = MIN, I_{sink} = 80mA			0.5	0.9	V
		V_{CC} = MIN, I_{sink} = 20mA				0.4	V
V_{off}	Off-state output voltage (S5445 or N7445)	V_{CC} = MAX, I_{off} = 250 μA		30			V
V_{off}	Off-state output voltage (S54145 or N74145)	V_{CC} = MAX, I_{off} = 250 μA		15			V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{CC}	Supply current	V_{CC} = MAX	S5445, S54145		43	62	mA
			N7445, N74145		43	70	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time logical 1 level	C_L = 15pF, R_L = 100 Ω			60	ns
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF, R_L = 100 Ω			60	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

BCD-TO-SEVEN SEGMENT DECODER/DRIVER

N7446
N7447

N7446-B • N7447-B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

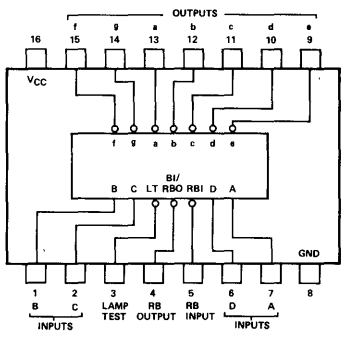
The 7446 and 7447 BCD-to-Seven Segment Decoder/Driver are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

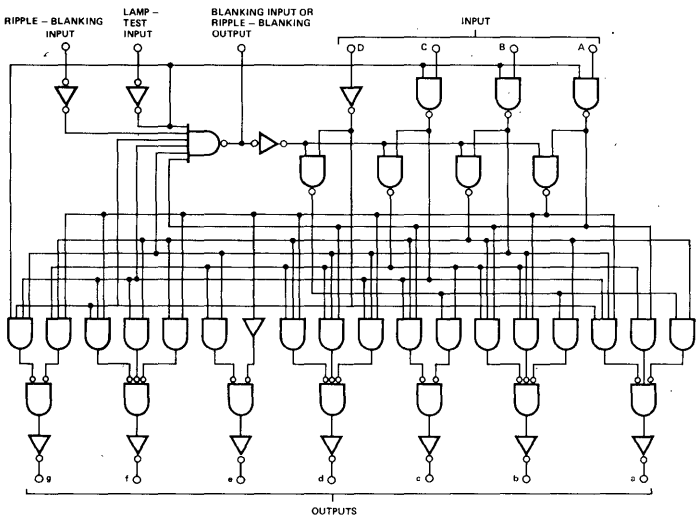
The 7446 and 7447 provide bare collector output transistors for directly driving lamps. The output transistor breakdown of the 7446 is 30 volts and the 7447 is 15 volts.

PIN CONFIGURATION

B PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

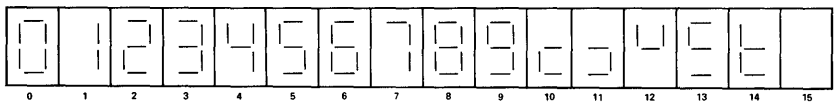
	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	x	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	x	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	x	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	x	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	x	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	x	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	x	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	x	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	x	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	x	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	x	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	x	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	x	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	x	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	x	1	1	1	1	1	1	1	1	1	1	1	1	
BI	x	x	x	x	x	x	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	x	x	x	x	x	1	0	0	0	0	0	0	0	4

NOTES:

1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 0.

SEGMENT IDENTIFICATION

SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): N7446, N7447 Circuits	4.75	5	5.25	V
Continuous Voltage at Outputs a through g: N7446 Circuits			30	V
N7447 Circuits			15	V
Normalized Fan-Out From Outputs a through g to Series 54/74 loads:				
N7446, N7447 Circuits			12	
Normalized Fan-Out From BI/RBO Node to Series 54/74 loads:				
N7446, N7447 Circuits			5	
Output Sink Current, I_{sink}: N7446, N7447 Outputs a through g			20	mA
N7446, N7447, BI/RBO Node			8	mA

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any point	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	V_{CC} = MIN			0.8	V
V_{on}	On-state output voltage at outputs a through g	V_{CC} = MIN, I_{sink} = 40mA		0.27	0.4	V
$V_{out(0)}$	Logical 0 output voltage at BI/RBO node	V_{CC} = MIN, I_{sink} = 8mA		0.3	0.4	V
V_{off}	Off-state output voltage at outputs a through g (S5446 and N7446 only)	V_{CC} = MAX, I_{off} = 250 A	30			V
V_{off}	Off-state output voltage at outputs a through g (S5447 and N7447 only)	V_{CC} = MAX, I_{off} = 250 A	15			V
$V_{out(1)}$	Logical 1 output voltage at BI/RBO node	V_{CC} = MIN, I_{load} = 200 A	2.4	3.7		V
$I_{in(0)}$	Logical 0 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current at BI/RBO node	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	V_{CC} = MAX N7446, N7447		53	90	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	C_L = 15pF, R_L = 280 Ω			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	C_L = 15pF, R_L = 280 Ω			100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

BCD-TO-SEVEN SEGMENT DECODER/DRIVER

N7448

N7448-B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

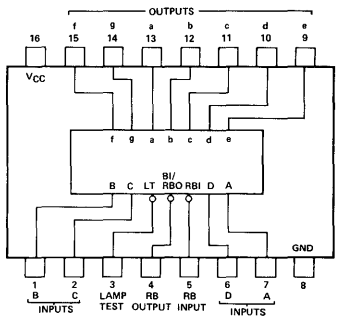
The 7448 BCD-to-Seven Segment Decoder/Driver is a TTL monolithic device consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs.

Incorporated in this device is a blanking circuit allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments.

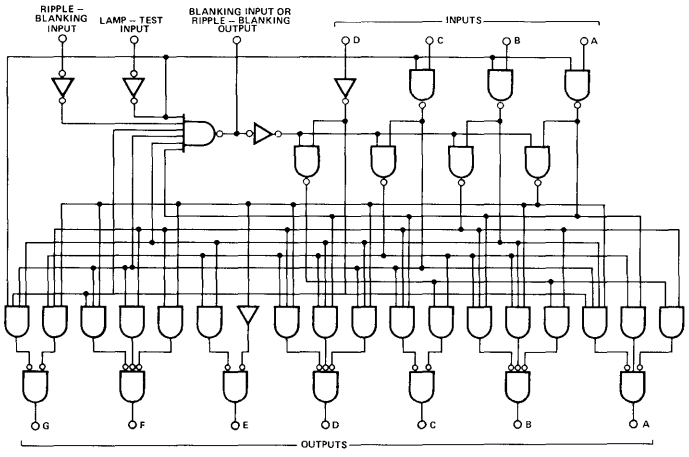
The 7448 has resistor pull up on the outputs to provide source current to drive interface elements.

PIN CONFIGURATIONS

B PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

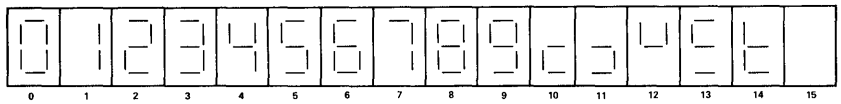
	INPUTS							OUTPUTS							
FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	x	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	x	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	x	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	x	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	x	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	x	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	x	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	x	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	x	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	x	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	x	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	x	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	x	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	x	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	x	1	1	1	1	1	0	0	0	0	0	0	0	
BI	x	x	x	x	x	x	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	x	x	x	x	x	1	1	1	1	1	1	1	1	4

NOTES:

1. BI/BRO is wire-OR logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input must be open or held at a logical 1 when output functions 0 through 15 are desired and ripple-blanking input (RBI) must be open or at a logical 1 during the decimal 0 input. X = input may be high or low.
2. When a logical 0 is applied to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition.
3. When ripple-blanking input (RBI) is at a logical 0 and A = B = C = D = logical 0, all segment outputs go to a logical 1 and the ripple-blanking output goes to a logical 0 (response condition).
4. When blanking input/ripple-blanking output is open or held at a logical 1, and a logical 0 is applied to lamp-test input, all segment outputs go to a logical 1.

SEGMENT IDENTIFICATION

SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): N7448 Circuit	4.75	5	5.25	V
Normalized Fan-Out From Outputs a through g to Series 54/74 loads: N7448 Circuits			4	
Normalized Fan-Out From BI/RBO Node to Series 54/74 Loads: N7448 Circuits			5	
Output Sink Current, I_{sink}: N7448 Outputs a through g			6.4	mA
N7448 BI/RBO Node			8	mA

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.
3. This rating applies when the output is off.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input	V_{CC} = MIN			0.8	V
$V_{out(0)}$	Logical 0 output voltage at any output	V_{CC}= MIN, I_{sink} = MAX		0.27	0.4	V
$V_{out(1)}$	Logical 1 level output voltage at outputs a through g	V_{CC} = MIN, I_{load} = -400 μA	2.4	4.2		V
$V_{out(1)}$	Logical 1 level output at BI/RBO node	V_{CC} = MIN, I_{load} = 200 μA	2.4	3.7		V
I_{load}	Load current available at outputs a through g	V_{CC} = MIN, V_{out} = 0.85V	-1.3	-2		mA
$I_{in(0)}$	Logical 0 level input current of any input except BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at BI/RBO node	V_{CC} = MAX, V_{in} = 0.4V			-4.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except BI/RBO node	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current at any output	V_{CC} = MAX			-4	mA
I_{CC}	Supply current	S5448		53	76	mA
		N7448		53	90	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C,

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from A input to any output	C_L = 15pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from A input to any output	C_L = 15pF			100	ns
t_{pd1}	Propagation delay time to logical 1 level from RBI input to any output	C_L = 15pF			100	ns
t_{pd0}	Propagation delay time to logical 0 level from RBI input to any output	C_L = 15pF			100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

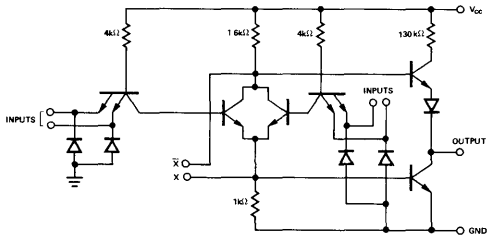
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

S5450
S5451
N7450
N7451

S5450A,F,W • S5451–A,F,W • N7450–A,F • N7451–A,F

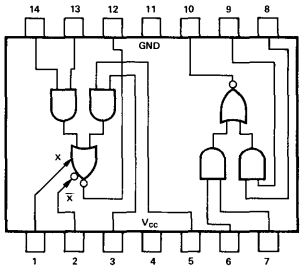
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

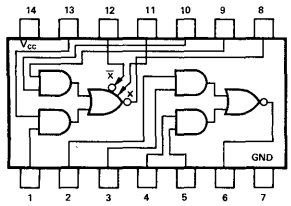


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and $\overline{X}$ pins of the S5451 and N7451.
5. A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5450, S5451 Circuits	4.5	5	5.5	V
	N7450, N7451 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5450, S5451 Circuits	-55	25	125	°C
	N7450, N7451 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		S5450, S5451	-20		-55	mA
				N7450, N7451	-18		-55	
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V			7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0			4	8	mA

ELECTRICAL CHARACTERISTICS (S5450 circuits) using expander inputs, V_{CC} = 4.5V, T_A = -55° C

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA, R_1 = 0	I_1 = 0.41mA,			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -0.15mA	I_1 = 0.15mA,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink}= 16mA, R_1 = 138Ω	I_1 = 0.3mA,		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (N7450 circuits) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

PARAMETER		TEST CONDITIONS		MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA, R_1 = 0	I_1 = 0.62mA,			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -270μA	I_1 = 270μA,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA, R_1 = 130Ω	I_1 = 0.43mA,		0.22	0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
** All typical values are at V_{CC}= 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

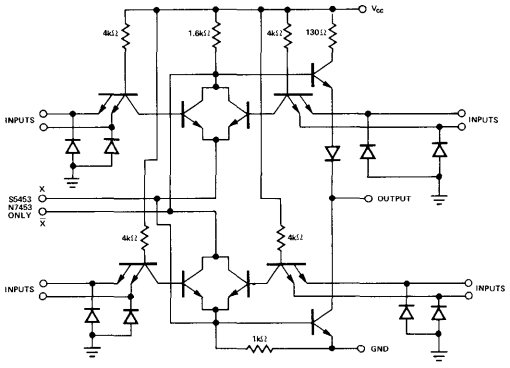
4-WIDE 2-INPUT AND-OR-INVERT GATE

S5453
S5454
N7453
N7454

S5453–A,F,W • S5454–A,F,W •N7453–A,F • N7454–A,F

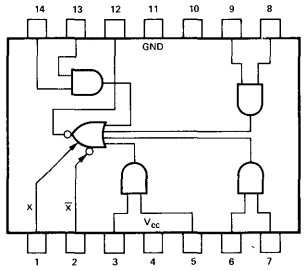
DIGITAL 54/74 TTL SERIES

SCHEMATIC DIAGRAM

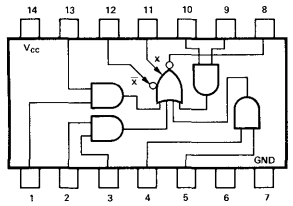


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Make no external connection to X and X pins of the S5454 and N7454.
5. A total of four expander gates can be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5453, S5454 Circuits	4.5	5	5.5	V
N7453, N7454 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output, N			10	
Operating Free-Air Temperature Range, T_A: S5453, S5454 Circuits	-55	25	125	°C
N7453, N7454 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA	V_{in} = 0.8V,	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA	V_{in} = 2V,		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = 5.5V		S5453, S5454	-20		-55	mA
				N7453, N7454	-18		-55	
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 5V			5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0			4	8	mA

ELECTRICAL CHARACTERISTICS (S5453 circuits) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA				2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA,	I_1 = 0.41mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -0.15mA	I_1 = 0.15mA,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA,	I_1 = 0.3mA,	R_1 = 138Ω		0.22	0.4	V

ELECTRICAL CHARACTERISTICS (N7453 circuits) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

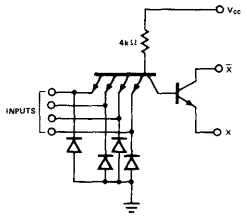
PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
I_X	Expander current	V_1 = 0.4V,	I_{sink} = 16mA				3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	I_{sink} = 16mA,	I_1 = 0.62mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -400μA, I_2 = -270μA	I_1 = 270μA,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 16mA,	I_1 = 0.43mA,	R_1 = 130Ω		0.22	0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS*		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15pF,	R_L = 400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15pF,	R_L = 400Ω		13	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and $\overline{X}$ are open.
** All typical values are at V_{cc} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

SCHEMATIC (each expander)

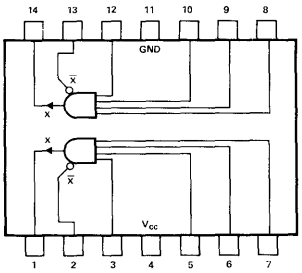


NOTES:

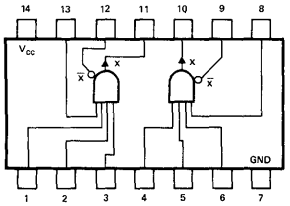
1. Connect to X input of S5450 or S5453 circuit.
2. Connect to $\overline{X}$ input of S5450 or S5453 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S5450 or one S5453 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = –55°C to 125°C)

	PARAMETER	TEST CONDITIONS			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.5V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, R = 1.1 kΩ,	V_{in} = 2V, T_A = –55°C	V_1 = 1V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 1.2 kΩ,	V_{in} = 0.8V, T_A = –55°C	V_1 = 4.5V,			150	μA
I_{on}	On-state output current	V_{CC} = 4.5V, T_A = –55°C	V_{in} = 2V,	V_1 = 1V,	–0.3			mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 0.4V				–1.6	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

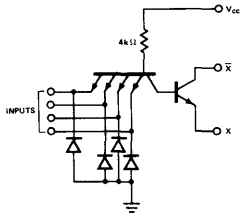
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 2.4V				40	μA
		V_{CC} = 5.5V,	V_{in} = 5.5V				1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V,	V_{in} = 5V,	V_1 = 0.85V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.5V,	V_{in} = 0,	V_1 = 0.85V		2	4	mA

SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through S5450 or S5453 circuit)	C_L = 15pF,	R_L = 400Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through S5450 or S5453 circuit)	C_L = 15pF,	R_L = 400Ω		15	30	ns

** All typical values are at V_{CC} = 5V, T_A = 25°C.

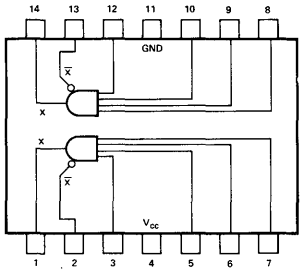
SCHEMATIC (each expander)



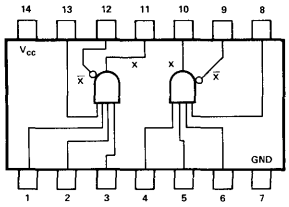
NOTES:
1. Connect to X input of N7450 or N7453 circuit.
2. Connect to $\overline{X}$ input of N7450 or N7453 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.75 to 5.25V
Maximum number of expanders that may be fanned-in to one N7450 or one N7453 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.75V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.75V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.75V, R = 1.1 kΩ,	V_{in} = 2V, T_A = 0°C	V_1 = 1V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.75V, R = 1.2 kΩ,	V_{in} = 0.8V, T_A = 0°C	V_1 = 4.5V,			270	μA
I_{on}	On-state output current	V_{CC} = 4.75V,	V_{in} = 2V,	V_1 = 1V	–0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 0.4V				–1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 2.4V				40	μA
		V_{CC} = 5.25V,	V_{in} = 5.5V				1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.25V, V_{in} = 5V, V_1 = 0.85V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.25V, V_{in} = 0 V_1 = 0.85V		2	4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through N7450 or N7453)	C_L = 15pF, R_L = 400Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through N7450 or N7453)	C_L = 15pF, R_L = 400Ω		15	30	ns

** All typical values are at V_{CC} = 5V, T_A = 25°C.

DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

TRUTH TABLE

LOGIC

J_n	K_n	Q_{n+1}	PRESET	CLEAR	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\overline{Q}_n$	1	1	Q

$J = J_1 J_2 J^*$ $K = K_1 K_2 K^*$

n is time prior to clock

n+1 is time following clock

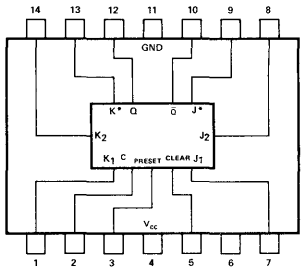
† Both outputs in 0 state

POSITIVE LOGIC

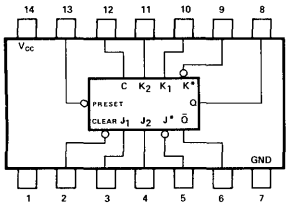
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

PIN CONFIGURATIONS

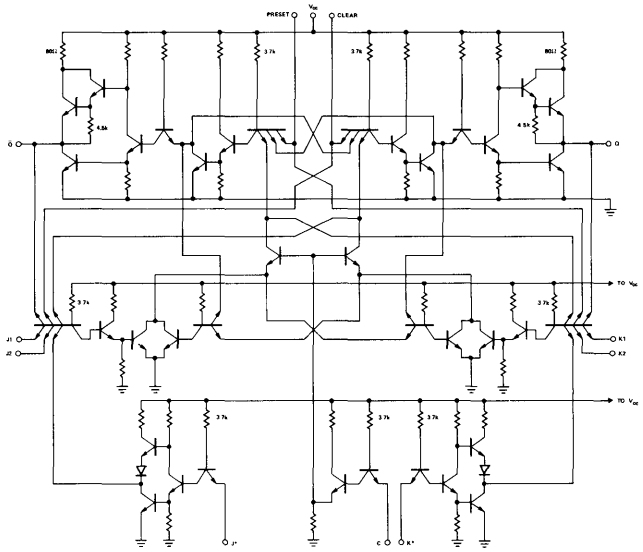
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



NOTE: Component values are typical.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5470 Circuits	4.5	5	5.5	V
	N7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5470 Circuits	−55	25	125	°C
	N7470 Circuits	0	25	70	°C
Normalized Fanout from each Output, N				10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$		5		150	ns
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J★, K1, K2, K★, or clock	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J★, K1, K2, K★, or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5470 N7470	−20 −18		−75 −75	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			13	26	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	35		MHz
t_{setup}	Minimum Input Setup time	C_L = 15pF,	R_L = 400Ω		10	20	ns
t_{hold}	Minimum input hold time	C_L = 15pF,	R_L = 400Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	18	50	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

J-K MASTER-SLAVE FLIP-FLOP

S5472
N7472

S5472–A,F,W • N7472–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

TRUTH TABLE

LOGIC

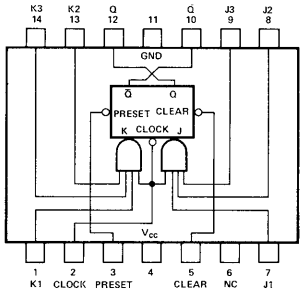
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:

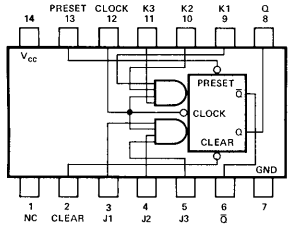
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. **NC = No Internal Connection.**

PIN CONFIGURATIONS

W PACKAGE

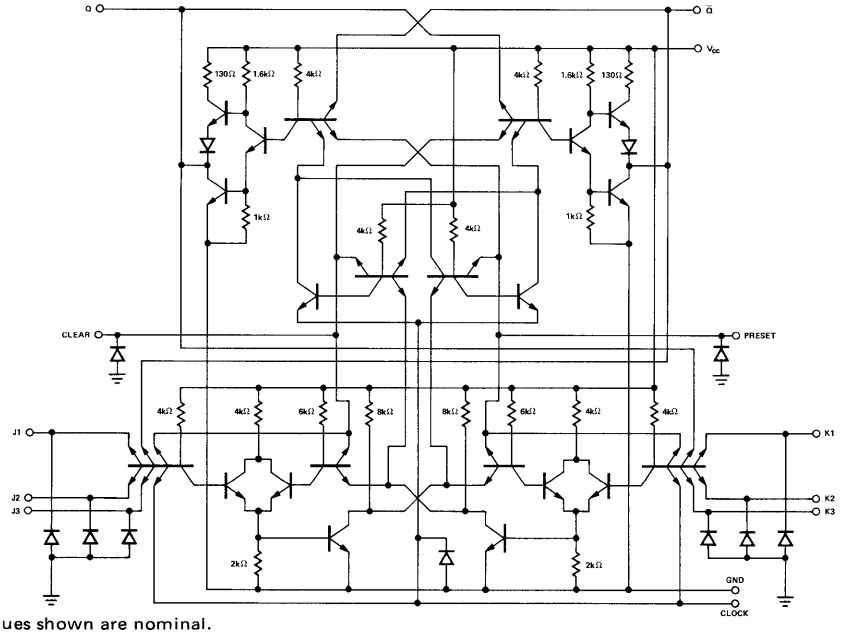


A,F PACKAGE



CLOCK WAVEFORM

SCHEMATIC DIAGRAM



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5472 Circuits		4.5	5	5.5	V
N7472 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5472 Circuits	-55	25	125	°C
	N7472 Circuits	0	25	70	°C
Normalized Fan-Out From each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		**2.4**	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			**0.22**	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5472	-20		-57	mA
				N7472	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			10	20	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC}= 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DUAL J-K MASTER-SLAVE FLIP-FLOP

S5473 N7473

S5473–A,F,W • N7473–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5473/N7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

TRUTH TABLE

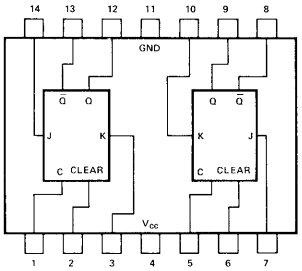
LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

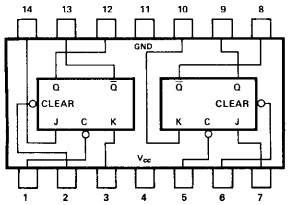
NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

PIN CONFIGURATIONS

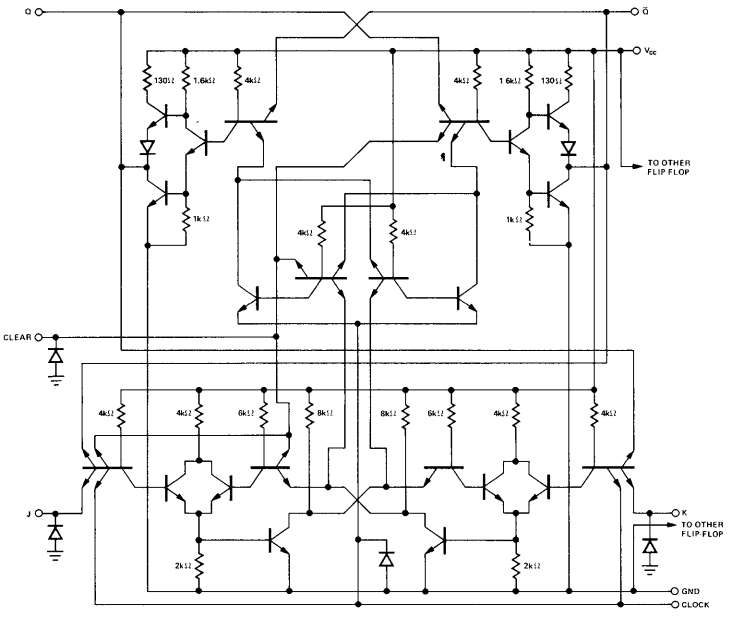
W PACKAGE



A,F PACKAGE



SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5473 Circuits		4.5	5	5.5	V
N7473 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5473 Circuits	-55	25	125	°C
	N7473 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(Clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN,					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5473 N7473	-20 -18		-57 -57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

S5474 N7474

S5474–A,F,W • N7474–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5474/N7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

TRUTH TABLE

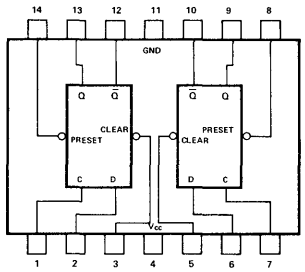
D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

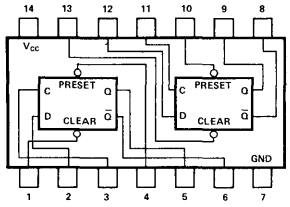
† Both outputs in 1 state
n is time prior to clock
n+1 is time following clock

PIN CONFIGURATIONS

W PACKAGE

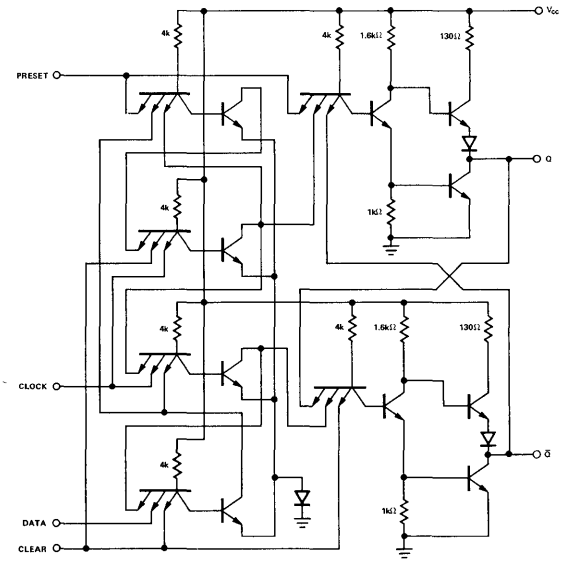


A,F PACKAGE



POSITIVE LOGIC — Low input to preset sets Q to logical 1 Low input to clear sets Q to logical 0; Preset and clear are independent of clock

SCHEMATIC DIAGRAM



NOTE: 1/2 of unit shown. Component values are typical.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5474 Circuits		4.5	5	5.5	V
N7474 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5474 Circuits	-55	25	125	°C
	N7474 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required t . ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				120 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5474 N7474	-20 -18		-57 -57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			17	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	25		MHz
t_{setup}	Minimum input setup time	C_L = 15pF,	R_L = 400Ω		15	20	ns
t_{hold}	Minimum input hold time	C_L = 15pF,	R_L = 400Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	20	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{cc} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

QUADRUPLE BISTABLE LATCH

S5475
N7475

S5475-B • N7475-B

DIGITAL 54/74 TTL SERIES

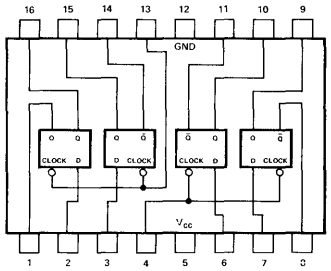
DESCRIPTION

The S5475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

PIN CONFIGURATIONS

B PACKAGE



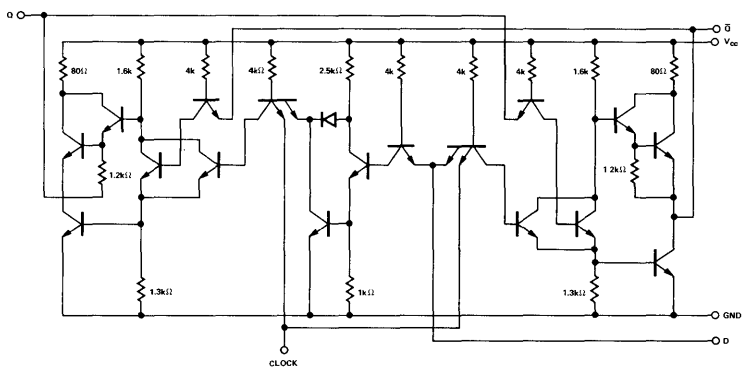
TRUTH TABLE

LOGIC

(Each Latch)		
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse
3. These voltages are with respect to network ground terminal.

SCHEMATIC (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S5475 Circuits	4.5	5	5.5	V
	N7475 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Outputs				10	
Operating Free-Air Temperature Range, T_A:	S5475 Circuits	-55	25	125	°C
	N7475 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,				-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX	V_{in} = 2.4V			160	μA
		V_{CC} = MAX	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	S5475	-20		-75	mA
		V_{out} = 0	N7475	-18		-75	mA
I_{CC}	Supply current	V_{CC} = MAX,	S5475		32	46	mA
			N7475		32	53	mA

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		24	40	ns
$t_{pd0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns
$t_{pd1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

DUAL J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR

S5476 N7476

S5476—B,F,W • N7476—B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5476B/N7476B J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

TRUTH TABLE

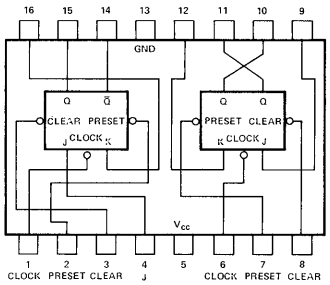
LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

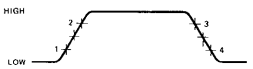
NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

PIN CONFIGURATIONS

B,F,W PACKAGE



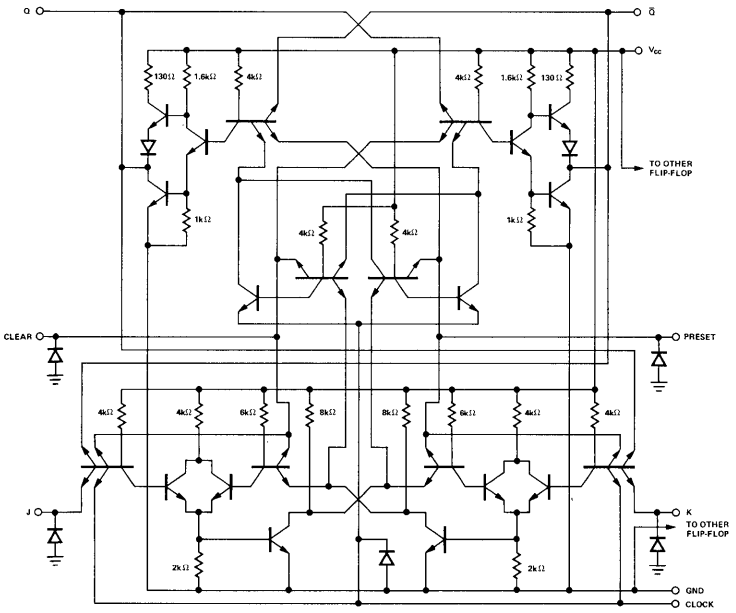
CLOCK WAVEFORM



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent from clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5476 Circuits	4.5	5	5.5	V
	N7476 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5476 Circuits	-55	25	125	°C
	N7476 Circuits	0	25	70	°C
Normalized Fanout from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Preset Pulse, $t_{p(preset)}$		25			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset, or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear, preset, or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S5476 N7476	-20 -18		-57 -57	mA
I_{CC}	Supply current (each flip-flop)	V_{CC} = MAX,	V_{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

QUADRUPLE BISTABLE LATCH

S5477
N7477

S5477W • N7477W

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5477Q/N7477Q is a monolithic, quadruple, bistable latch with Q outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

TRUTH TABLE

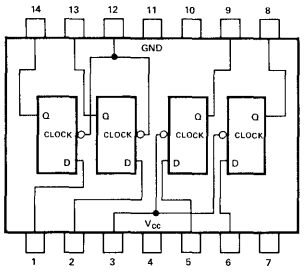
LOGIC

(Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

PIN CONFIGURATIONS

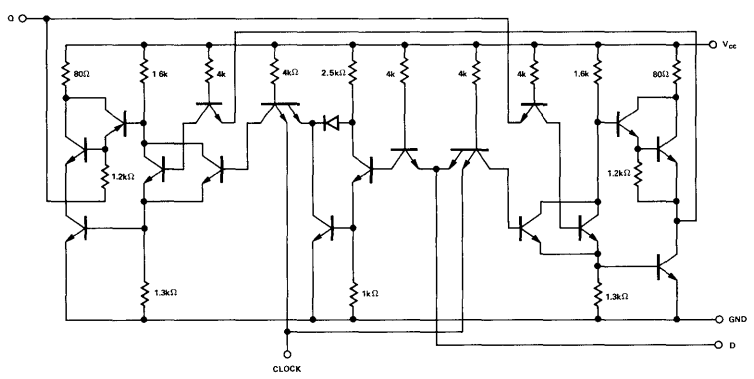
W PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S5477 Circuits	4.5	5	5.5	V
	N7477 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5477 Circuits	-55	25	125	°C
	N7477 Circuits	0	25	70	°C

SCHEMATIC (each latch)



ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,					−6.4	mA
$I_{in(1)}$	**Logical 1 level input** current at D	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX, V_{in} = 2.4V, V_{CC} = MAX,	 V_{in} = 5.5V				160 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, V_{out} = 0		S5477 N7477	−20 −18		−75 −75	mA mA
I_{CC}	Supply current	V_{CC} = MAX,		S5477 N7477		32 32	46 53	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	**Propagation** delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

GATED FULL ADDER

S5480
N7480

S5480–A,F,W • N7480–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5480/N7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

TRUTH TABLE (See Notes 1,2, and 3)

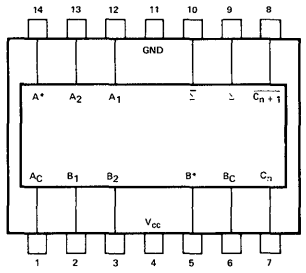
LOGIC

C_n	B	A	$C_{\overline{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

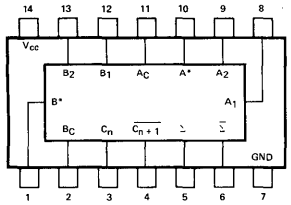
NOTES:
1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$, $B^* = \overline{B_1 \cdot B_2}$.
2. When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively, must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A* or B* respectively, must be open or used to perform Dot-OR logic.
4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

PIN CONFIGURATIONS

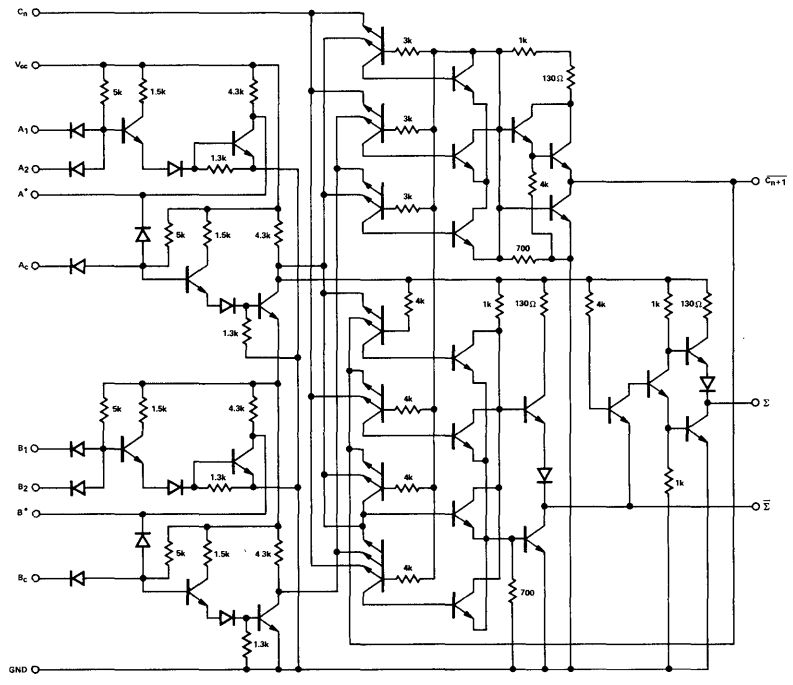
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5480 Circuits	4.5	5	5.25	V
	N7480 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Outputs:	$\overline{C_n+1}$, N			5	
	Σ or $\overline{\Sigma}$, N			10	
	A* or B*, N			3	
Operating Free-Air Temperature Range, T_A:	S5480 Circuits	-55	25	125	°C
	N7480 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN			2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN				0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A* or B*	V_{CC} = MAX,	V_{in} = 0.4V				-2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	V_{CC} = MAX,	V_{in} = 0.4V				-8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	V_{CC} = MAX, V_{CC} = MAX	V_{in} = 2.4V V_{in} = 5.5V				15 1	µA mA
$I_{in(1)}$	Logical 1 level input current at C_n	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				200 1	µA mA
I_{OS}	Short circuit output current at Σ or $\overline{\Sigma}$†	V_{CC} = MAX,		S5480 N7480	-20 -18		-57 -57	mA mA
I_{OS}	Short circuit output current at $\overline{C_{n+1}}$†	V_{CC} = MAX,		S5480 N7480	-20 -18		-70 -70	mA mA
I_{CC}	Supply current	V_{CC} = MAX,		S5480 N7480		21 21	31 35	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	C_L = 15pF,	R_L = 780Ω		13	17	ns
t_{pd0}			C_L = 15pF,	R_L = 780Ω		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	C_L = 15pF,	R_L = 780Ω		18	25	ns
t_{pd0}			C_L = 15pF,	R_L = 780Ω		38	55	ns
t_{pd1}	A_C	Σ	C_L = 15pF,	R_L = 400Ω		52	70	ns
t_{pd0}			C_L = 15pF,	R_L = 400Ω		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	C_L = 15pF,	R_L = 400Ω		38	55	ns
t_{pd0}			C_L = 15pF,	R_L = 400Ω		56	75	ns
t_{pd1}	A_1	A*	C_L = 15pF			48	65	ns
t_{pd0}			C_L = 15pF			17	25	ns
t_{pd1}	B_1	B*	C_L = 15pF			48	65	ns
t_{pd0}			C_L = 15pF			17	25	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC}= 5V, T_A = 25°C

† Not more than one output should be shorted at a time.

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

4-BIT BINARY FULL ADDER (LOOK AHEAD CARRY)

S5483 N7483

S5483–B,F,W • N7483–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7483 is a 4-Bit Binary Full Adder for adding two four bit binary numbers. A Carry Look Ahead circuit is included to provide minimum carry propagation delays.

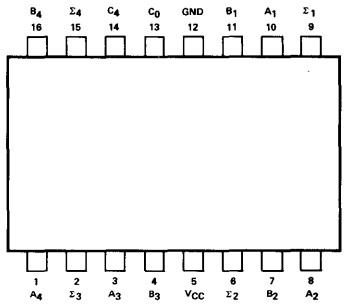
Propagation delays of carry-in to carry-out is typically 12 nsec.

TRUTH TABLE

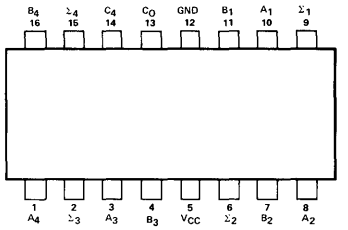
INPUT				OUTPUT					
				WHEN $C_0 = 0$ / WHEN $C_2 = 0$			WHEN $C_0 = 1$ / WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

PIN CONFIGURATIONS

W PACKAGE

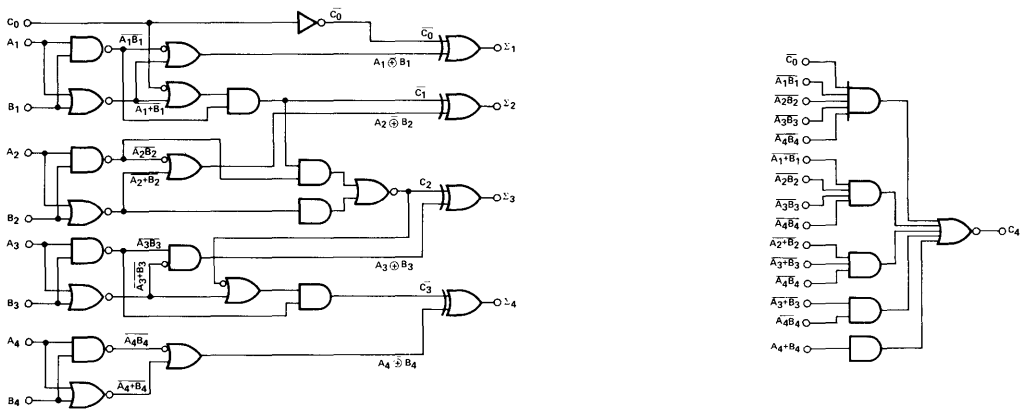


B,F PACKAGE



NOTES:
Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	S5483 Circuits	4.5	5	5.5	V
	N7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:	C_4			5	
	Σ_1, Σ_2, Σ_3 or Σ_4			10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN				0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current A_1, A_3, B_1, B_3, or C_0	V_{CC} = MAX, V_{in} = 2.4V				80	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current A_2, A_4, B_2, or B_4	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} @ MAX, V_{in} = 5.5V				1	mA
I_{OS}	Short-circuit output current at Σ_1, Σ_2, Σ_3, or Σ_4 †	V_{CC} = MAX	S5483	-20		-55	mA
			N7483	-18		-55	mA
I_{OS}	Short-circuit output current at C_4 †	V_{CC} = MAX	S5483	-20		-70	mA
			N7483	-18		-70	mA
I_{CC}	Supply current	V_{CC} = MAX,			58	79	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, unless otherwise noted N = 10

PARAMETER ‡		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	From C_0 to 1	C_L = 50pF,	R_L = 400Ω		23	34	ns
t_{pd0}	From C_0 to 1	C_L = 50pF,	R_L = 400Ω		20	34	ns
t_{pd1}	From C_0 to 2	C_L = 50pF,	R_L = 400Ω		24	35	ns
t_{pd0}	From C_0 to 2	C_L = 50pF,	R_L = 400 Ω		22	35	ns
t_{pd1}	From C_0 to 3	C_L = 50pF,	R_L = 400Ω		30	50	ns
t_{pd0}	From C_0 to 3	C_L = 50pF,	R_L = 400Ω		24	40	ns
t_{pd1}	From C_0 to 4	C_L = 50pF,	R_L = 400Ω		30	50	ns
t_{pd0}	From C_0 to 4	C_L = 50pF,	R_L = 400Ω		28	50	ns
t_{pd1}	From C_0 to C_4	C_L = 50pF,	R_L = 780Ω		12	20	ns
t_{pd0}	From C_0 to C_4	C_L = 50pF,	R_L = 780Ω		12	20	ns
t_{pd1}	From A_2 or B_2 to 2	C_L = 50pF,	R_L = 400Ω			40	ns
t_{pd0}	From A_2 or B_2 to 2	C_L = 50pF,	R_L = 400Ω			35	ns
t_{pd1}	From A_4 of B_4 to 4	C_L = 50pF,	R_L = 400Ω			40	ns
t_{pd0}	From A_4 of B_4 to 4	C_L = 50pF,	R_L = 400Ω			35	ns

† T_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

NOTE 1: These voltage values are with respect to network ground terminal.

QUAD 2-INPUT EXCLUSIVE OR GATE

S5486
N7486

S5486–A,F,W • N7486–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

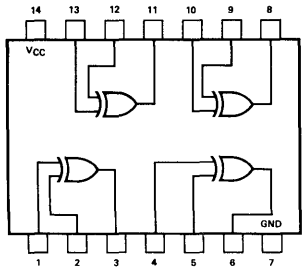
The 54/7486 Quad 2-Input Exclusive OR Gate is a TTL element providing the function $\overline{A}B + A\overline{B}$ at the output.

TRUTH TABLE

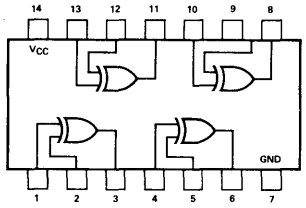
INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S5486 Circuits	4.5	5	5.5	V
	N7486 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each output, N:	Logical 0			10	
	Logical 1			20	

NOTE: 1. These voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, $V_{in(1)}$ = 4.5V, $V_{in(0)}$ = 0	S5486	-20		-55	mA
			N7486	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V	S5486		30	43	mA
			N7486		30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (other input low)	C_L = 15pF, R_L = 400		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	C_L = 15pF, R_L = 400		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (Other input high)	C_L = 15pF, R_L = 400		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	C_L = 15pF, R_L = 400		18	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

\+ Not more than one output should be shorted at a time.

256-BIT READ-ONLY MEMORY | N7488

N7448–B,W

DIGITAL 54/74 TTL SERIES

DESCRIPTION

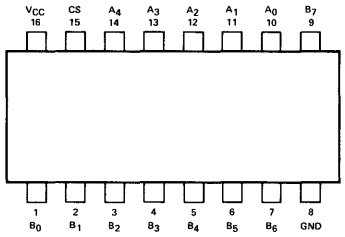
The 7488 is a TTL 256-Bit Read Only Memory organized as 32 word with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Select input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Select input is taken high.

This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-OR operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

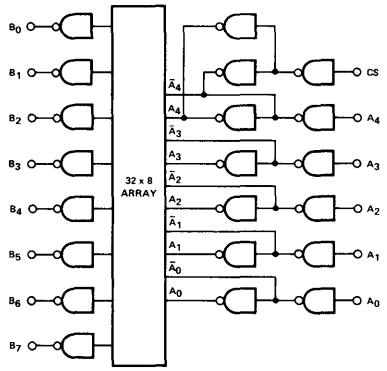
Customer may specify patterns for the 256-Bit Read Only Memory by completing the truth table/order blank.

PIN CONFIGURATIONS

B,W PACKAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
See 8223 or 8224 Data Sheet for Pin-for-Pin Replacement					

256-BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

	INPUTS						OUTPUTS							
WORD	A_4	A_3	A_2	A_1	A_0	ENABLE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1

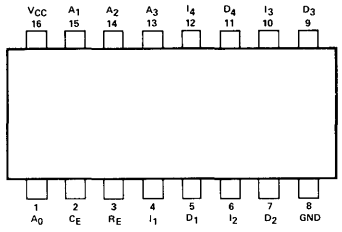
DESCRIPTION

The 7489 is a TTL 64-Bit Read-Write Random Access Memory organized as 16-words of 4 bits each. The 7489 is ideally suited for application in scratch pads and high speed buffer memories.

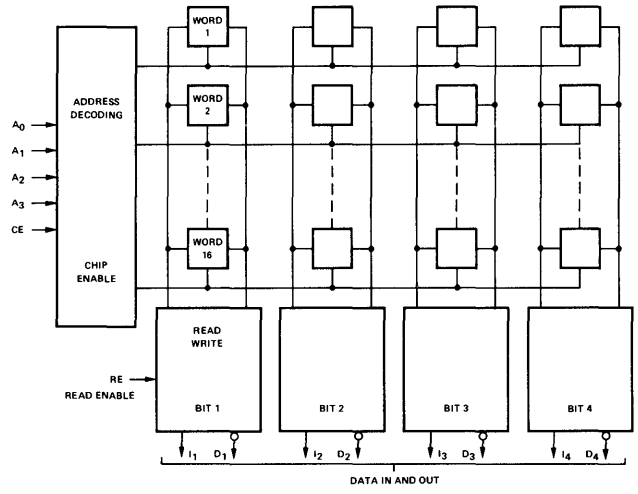
Words are selected through a 4-input binary decoder when the chip select input (CE) is at logic "0". Data is written into the memory when Read Enable (RE) is at logic "0" and read from the memory when RE is at logic "1".

PIN CONFIGURATION

B PACKAGE



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

See 8225 Data Sheet for Pin-for-Pin Replacement

DECADE COUNTER | S5490 N7490

S5490–A,F,W • N7490–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

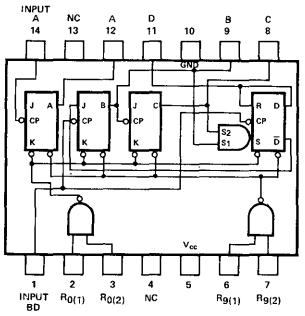
The S5490/N7490 is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical "0" or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional "0" reset, inputs are provided to reset a BCD 9 count for nine's complement decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

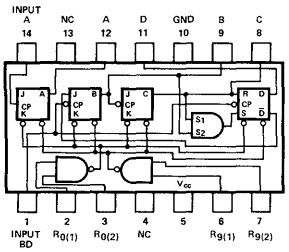
The 5490/7490 is completely compatible with Series 54 and Series 74 logic familes. Average power dissipation is 160mW.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



LOGIC TRUTH TABLES

BCD COUNT SEQUENCE (See Note 1)

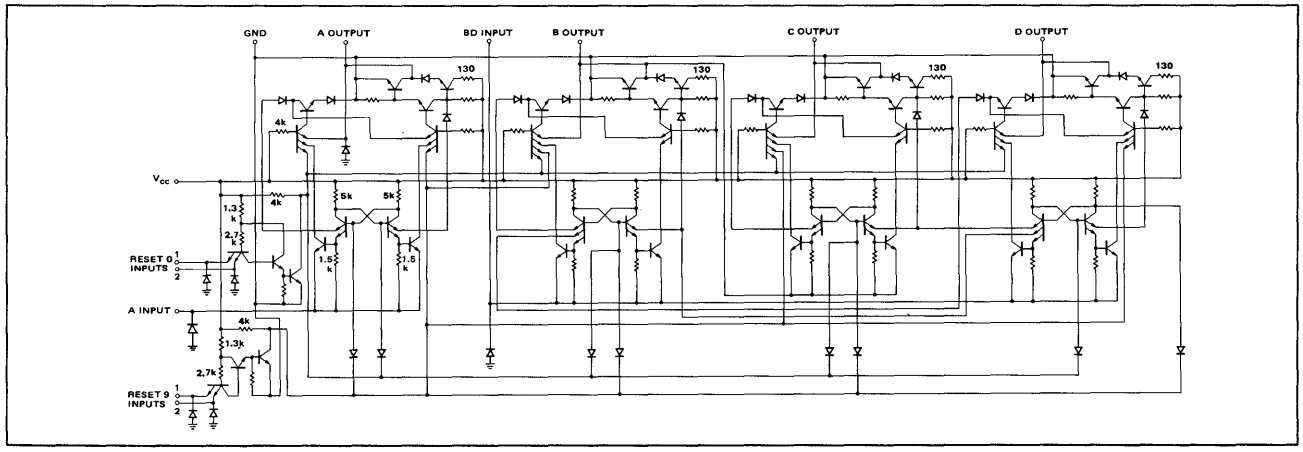
COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(2)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NOTES:
1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5490 Circuits	4.5	5	5.5	V
	N7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns
Operating Free-Air Temperature Range, T_A:	S5490 Circuits	-55	25	125	°C
	N7490 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				80 1	μA mA
$I_{in(1)}$	Logical 1 level input current at input BD	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V				160 1	μA mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	V_{CC} = MAX,	V_{in} = 0.4V				-6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0V	S5490 N7490	-20 -18		-57 -57	mA mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5490 N7490		32 32	46 53	mA mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	C_L = 15pF,	R_L = 400Ω		60	100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

8-BIT SHIFT REGISTER

S5491
N7491

S5491–A,F,W • N7491–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5491/N7491 is a monolithic serial-in, serial-out 8-bit shift register utilizing high-speed transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes the S5491/N7491 to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the S5470/N7470 flip-flop and the S5474/N7474 dual D-type flip-flop.

TRUTH TABLE

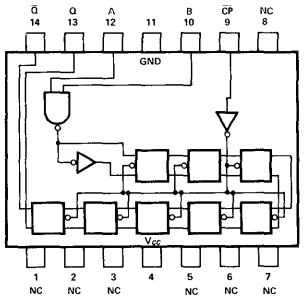
LOGIC

t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

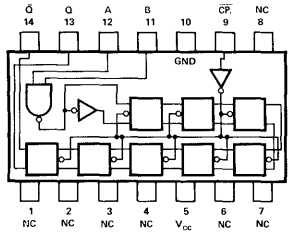
NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+8} = bit time after 8 clock pulse.

PIN CONFIGURATIONS

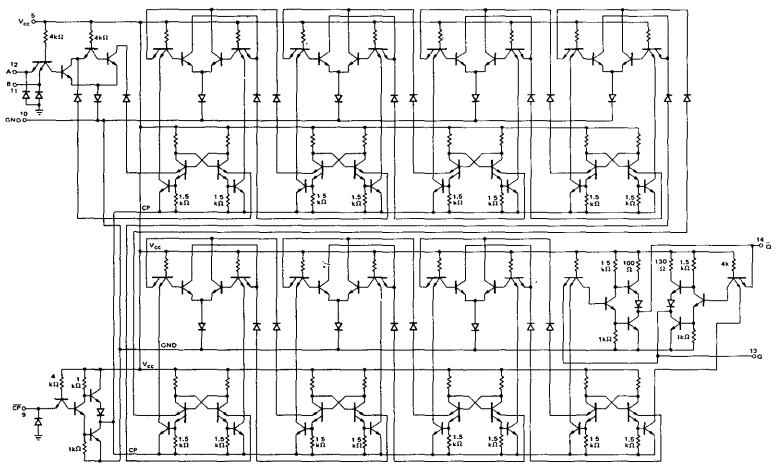
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S5491 Circuits	4.5	5	5.5	V
	N7491 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5491 Circuits	-55	25	125	°C
	N7491 Circuits	0	25	70	°C
Width of Clock Pulse, $t_{p(clock)}$		25			ns
Input Setup Time, t_{setup}		25			ns
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	S5491	-20		-57	mA
				N7491	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5491		35	50	mA
				N7491		35	58	mA

SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		27	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC}= 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

S5492 N7492

S5492–A,F,W • N7492–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5492/N7492 is a high-speed monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flops outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

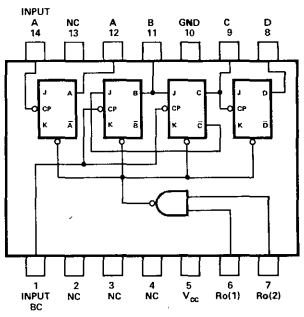
1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous division of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table.

2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency division of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

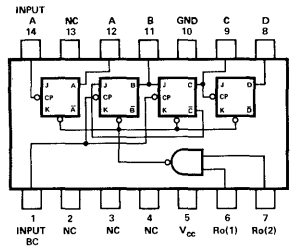
The S5492/N7492 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 155mW.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



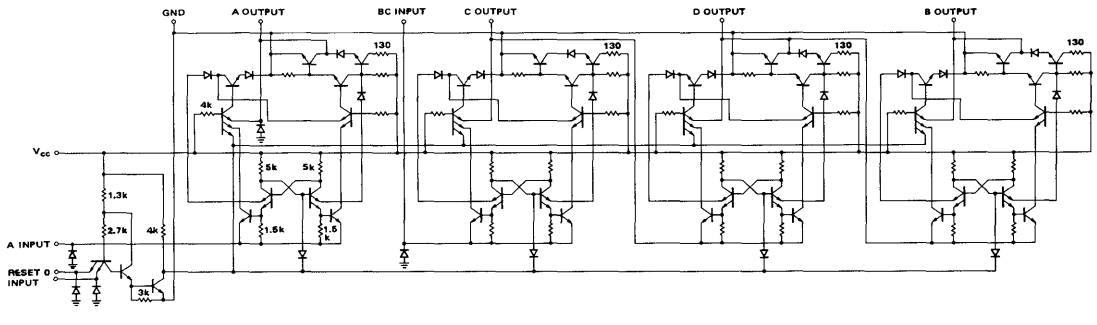
TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1

COUNT	OUTPUT			
	D	C	B	A
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5492 Circuits		4.5	5	5.5	V
N7492 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5492 Circuits	-55	25	125	°C
	N7492 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BC	V_{CC} = MAX,	V_{in} = 2.4V				160	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current input A	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	V_{CC} = MAX,	V_{in} = 0.4V				-6.4	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	S5492	-20		-57	mA
				N7492	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5492		31	44	mA
				N7492		31	51	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		60	100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

4-BIT BINARY COUNTER

S5493
N7493

S5493–A,F,W • N7493–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5493/N7493 is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

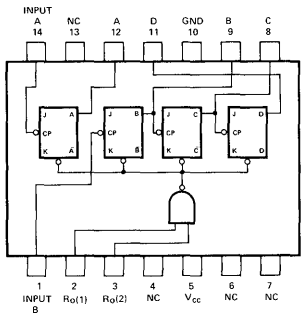
1. When used as a 4-bit ripple-through counter output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

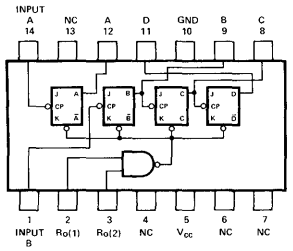
The S5493/N7493 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 32mW per flip-flop (128mW total).

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



TRUTH TABLE (See Notes 1 and 2)

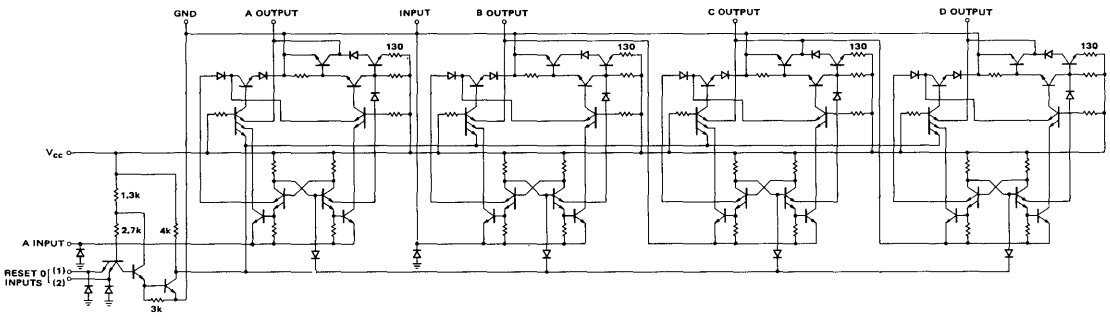
LOGIC

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

COUNT	OUTPUT			
	D	C	B	A
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES:
1. Output A connected to input B.
2. To reset all outputs to logical 0, both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5493 Circuits		4.5	5	5.5	V
N7493 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S5493 Circuits	-55	25	125	°C
	N7493 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Input Count Pulse, $t_{p(in)}$		50			ns
Width of Reset Pulse, $t_{p(reset)}$		50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{out} = 0	S5493	-20		-57	mA
				N7493	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5493		32	46	mA
				N7493		32	53	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	C_L = 15pF,	R_L = 400Ω		75	135	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

4-BIT SHIFT REGISTER (PARALLEL-IN, SERIAL-OUT)

S5494 N7494

S5494–B,F,W • N7494–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

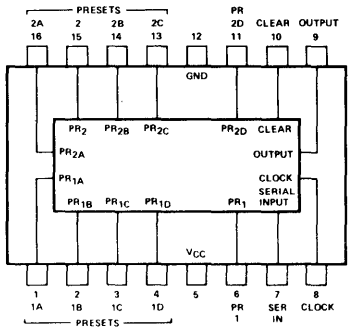
The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The output of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

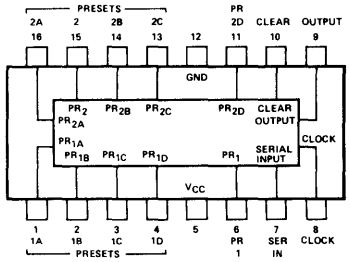
This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

PIN CONFIGURATIONS

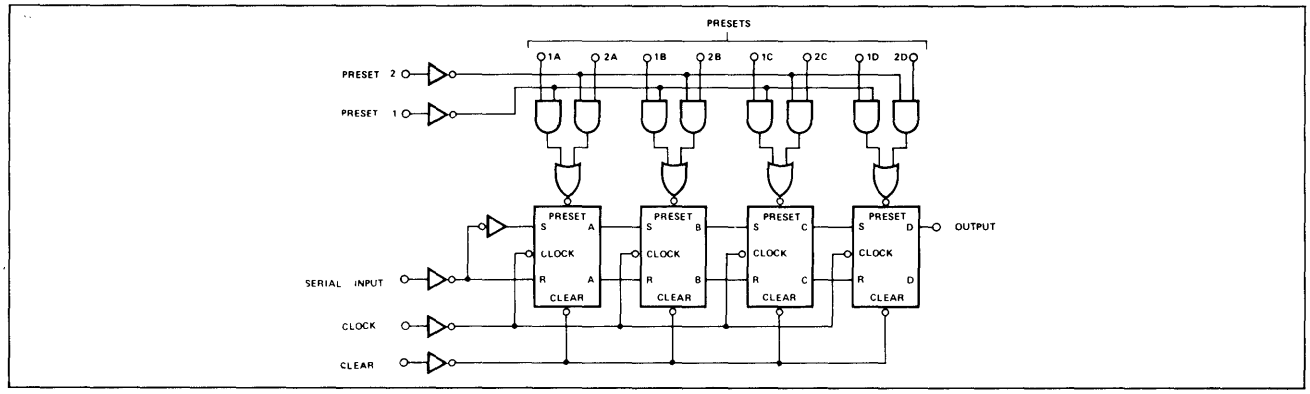
W PACKAGE



B,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): S5494 Circuits	4.5	5	5.5	V
N7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time: $t_{setup(1)}$	35			ns
$t_{setup(0)}$	25			ns
Serial Input Hold Time, t_{hold}	0			

NOTE: 1. The voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4V				160	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4V				-6.4	mA
I_{OS}	Short-circuit input current†	V_{CC} = MAX, V_{out} = 0	S5494	-20		-57	mA
			N7494	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX	S5494		35	50	mA
			N7494		35	58	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15pF,	R_L = 400Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400Ω			40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTER

S5495 N7495

S5495–A,F • N7495–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/7495 is a monolithic universal 4-Bit Shift Register designed with standard TTL techniques. The circuit layout consists of 4 R-S master-slave flip-flops, 4 AND-OR-INVERT gates, and 6 inverters configured to form a versatile register which will perform right-shift, left-shift, or parallel-in, parallel-out operations depending on the logical input level to the mode control.

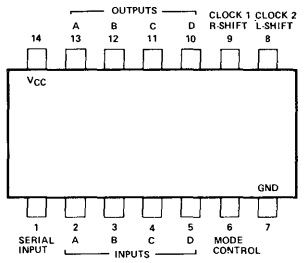
Right-shift operations are performed when a logical 0 level is applied to the mode control. Serial data is entered at the serial input D_S and shifted one position right on each clock 1 pulse. In this mode, clock 2 and parallel inputs D_A thru D_D are inhibited.

Parallel-in, parallel-out operations are performed when a logical 1 level is applied to the mode control. Parallel data is entered at parallel inputs D_A thru D_D and is transferred to the data outputs A_0 thru D_0 on each clock 2 pulse. In this mode, shift-left operations may be implemented by externally tying the output of each flip-flop to the parallel input of the previous flip-flop (D_0 to D_C and etc.), with serial data entry at input D_D.

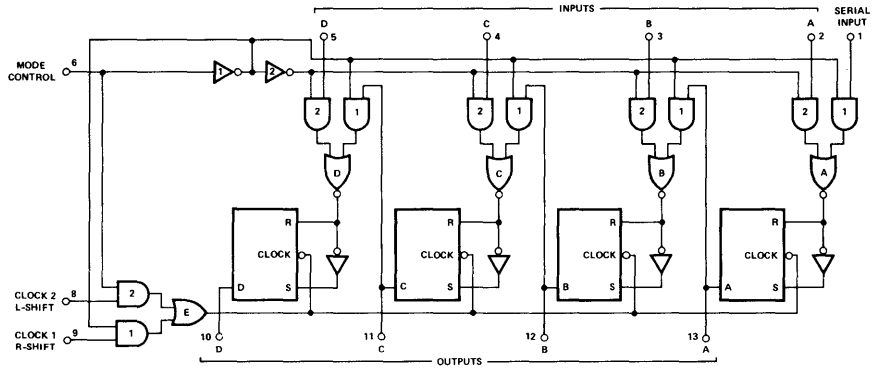
Information must be present at the R-S inputs prior to clocking and transfer of data occurs on the falling edge of the clock pulse.

PIN CONFIGURATIONS

A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S5495 Circuits	4.5	5	5.5	V
	N7495 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output				10	
Width of Clock Pulse $t_{p(clock)}$	S5495 Circuits	20	10		ns
	N7495 Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup}		10	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold}		0	10		ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 1 inputs)		15			ns
Logical 1 level Setup Time Required at Mode Control (With Respect to Clock 2 input)		15			ns
Logical 0 Level Setup Time Required at Mode Control (With Respect to Clock 2 input)		5			ns
Logical 1 Level Setup Time Required at Mode Control (With Respect to Clock 1 input)		5			ns

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	V_{CC} = MAX, V_{in} = 2.4V				80	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX	N7495	39	50	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	C_L = 15pF,	R_L = 400Ω	25	36		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	C_L = 15pF,	R_L = 400Ω		18	27	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	C_L = 15pF,	R_L = 400Ω		21	32	ns

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

5-BIT SHIFT REGISTER

S5496
N7496

S5496-B,F,W • N7496-B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

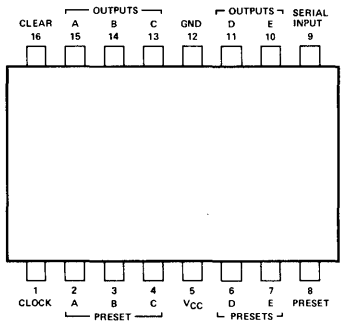
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

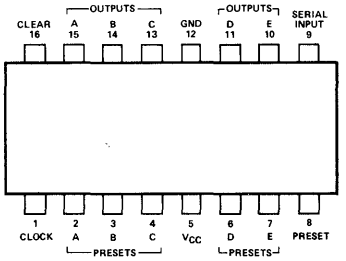
Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

PIN CONFIGURATIONS

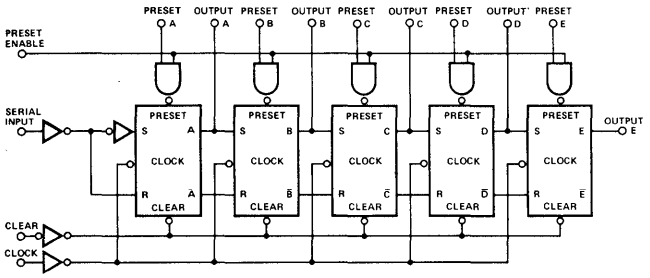
W PACKAGE



B,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S5496 Circuits	4.5	5	5.5	V
	N7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output				10	
Width of Clock Pulse, $t_{p(clock)}$		35			ns
Width of Clear Pulse, $t_{p(clear)}$		30			ns
Width of Preset Pulse, $t_{p(preset)}$		30			ns
Serial Input Setup Time, t_{setup}		30			ns
Serial Input Hold Time, t_{hold}		0			ns

NOTE: 1. This voltage value is with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset (pin (8))	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset (pin (8))	V_{CC} = MAX, V_{in} = 2.4V				200	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset (pin (8))	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset (pin (8))	V_{CC} = MAX, V_{in} = 0.4V				-8	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX, V_{out} = 0	S5496	-20		-57	mA
			N7496	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX	S5496		48	68	mA
			N7496		48	79	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15pF,	R_L = 400Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 15pF,	R_L = 400Ω		28	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400			55	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

4-BIT BISTABLE LATCH

S54100
N74100

S54100–N,Q,F • N74100–F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The S54100/N74100 features two independent quadruple latches in a single 24-pin dual in-line package. These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of -55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

ABSOLUTE MAXIMUM RATINGS (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3)	7V
Input Voltage, V_{in} (See Notes 3 and 4)	5.5V
Operating Free-Air Temperature Range:	
S54100 Circuits	-55°C to 125°C
N74100 Circuits	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES:
3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

TRUTH TABLE

LOGIC

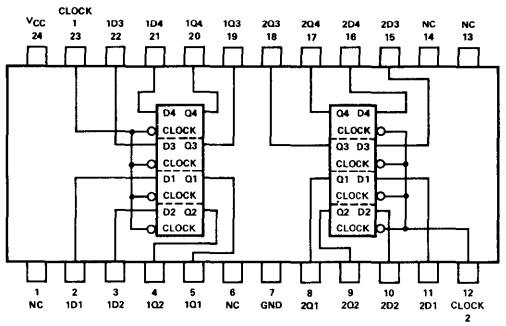
(Each Latch)	
t_n D	t_{n+1} Q
1	1
0	0

NOTES:
1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

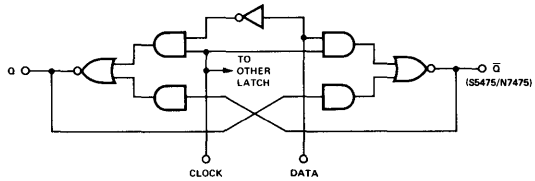
NC – No internal connection.

PIN CONFIGURATIONS

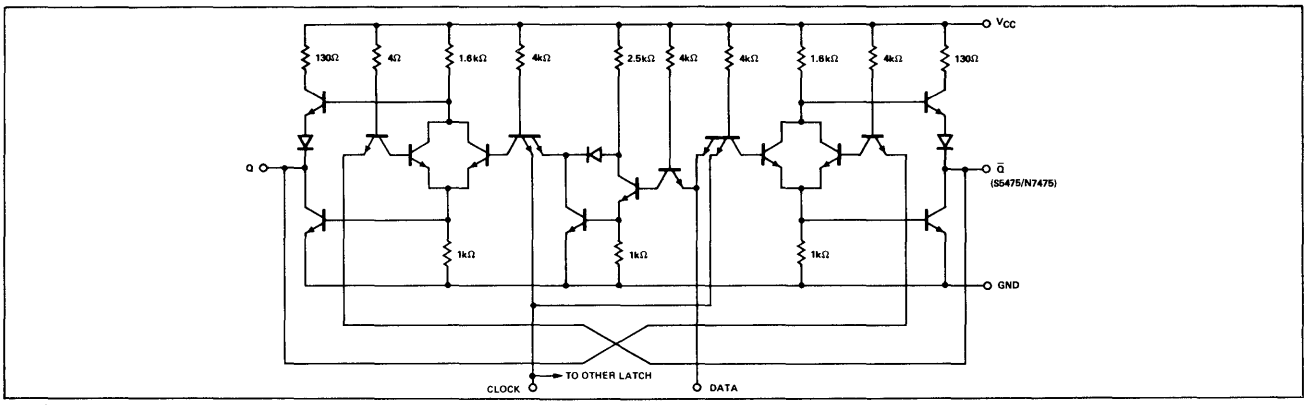
N,Q,F PACKAGE



LOGIC DIAGRAM (each latch)



SCHEMATIC DIAGRAM (each latch)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3):	S54100	4.5	5	5.5	V
	N74100	4.75	5	5.25	V
Normalized Fan-Out from Output				10	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	V_{CC} = MAX,	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	S54100, N74100			-12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC} = MAX,	V_{in} = 2.4V			80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,				160	μA
		V_{in} = 2.4V,	S54100, N74100			320	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	S54100	-20		-57	mA
		V_{out} = 0	N74100	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	S54100		64	92	mA
			N74100		64	106	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	C_L = 15pF,	R_L = 400Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	C_L = 15pF,	R_L = 400Ω	0	6¶		ns
$t_{pd1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	C_L = 15pF,	R_L = 400Ω		14	25	ns
$t_{pd1(D-\overline{Q})}$	Propagation delay time to logical 1 level from D input to $\overline{Q}$ output (S5475, N7475)	C_L = 15pF,	R_L = 400Ω		24	40	ns
$t_{pd1(C-Q)}$	Progagation delay time to logical 1 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	C_L = 15pF,	R_L = 400Ω		7	15	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

DUAL J-K-MASTER-SLAVE FLIP-FLOP

S54107
N74107

S54107–A,F • N74107–A,F

DIGITAL 54/74 TTL SERIES

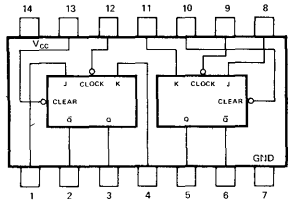
DESCRIPTION

The S54107A/N74107A J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:
See S5473/N7473 waveform.

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

PIN CONFIGURATIONS

A,F PACKAGE



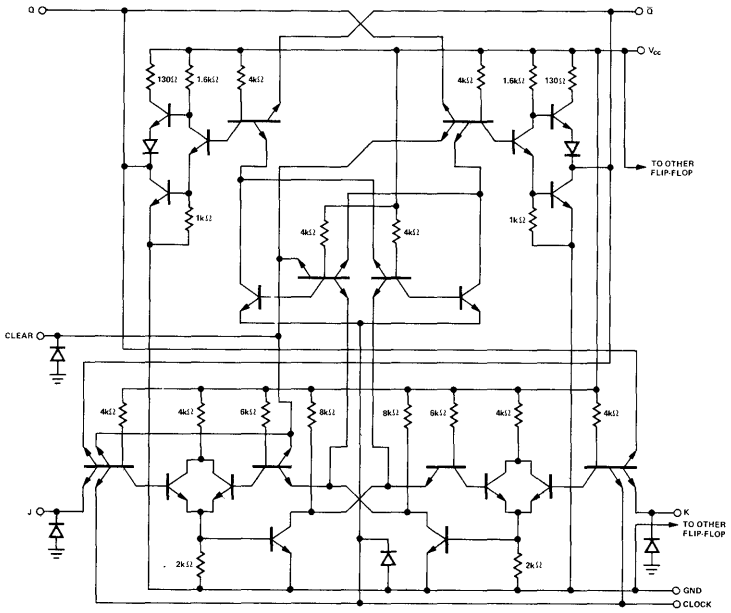
TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54107 Circuits	4.5	5	5.5	V
	N74107 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54107 Circuits	-55	25	125	°C
	N74107 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		20			ns
Width of Clear Pulse, $t_{p(clear)}$		25			ns
Input Setup Time, t_{setup}		$\geqslant t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX,	V_{in} = 0.4V				-1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 0.4V				-3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	V_{CC} = MAX,	V_{in} = 2.4V				80	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 0	S54107	-20		-57	mA
				N74107	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{clock}	Maximum clock frequency	C_L = 15pF,	R_L = 400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 15pF,	R_L = 400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15pF,	R_L = 400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

MONOSTABLE MULTIVIBRATOR | N74121

N74121–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

This monolithic TTL monostable multivibrator features d-c triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 nanoseconds to 40 seconds by choosing appropriate timing components. With no external timing components (i.e., pin (9) connected to pin (14), pins (10), (11) open) an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

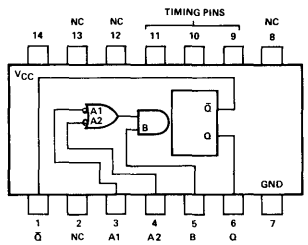
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10μF) and more than one decade of timing resistance (2kΩ to 40kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 milliwatts at 5 volts (50% duty cycle) and a quiescent dissipation of typically 65 milliwatts.

Duty cycles as high as 90% are achieved when using R_T - 40kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

PIN CONFIGURATIONS

A,F PACKAGE



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

1 = $V_{in(1)} \geq 2V$ 0 = $V_{in(0)} \leq 0.8V$

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
3. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of 30ns is obtained typically.
4. To use the internal timing resistor (2kΩ nominal), connect pin (9) to pin (14).
5. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
6. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.
7. t_n = time before input transition.
8. t_{n+1} = time after input transition.
9. x indicates that either a logical 0 or 1, may be present.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:				V
N74121 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Input Pulse Rise/Fall Time: Schmitt Input (B)			1	V/s
Logic Inputs (A1, A2)			1	V/μs
Input Pulse Width	50			ns
External Timing Resistance Between Pins (11) and (14) (Pin (9) open)	1.4			kΩ
External Timing Resistance: S54121			30	kΩ
N74121			40	kΩ
Timing Capacitance	0		1000	μF
Output Pulse Width			40	s
Duty Cycle: R_T = 2kΩ			67%	
R_T = 30kΩ (S54121) or			90%	
R_T = 40kΩ (N74121)				

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN				1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN			0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN				1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN			0.8	1.35		V
V_{out} (0)	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
V_{out} (1)	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -400μA		2.4	3.3		V
I_{in} (0)	Logical 0 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 0.4V			-1	-1.6	mA
I_{in} (0)	Logical 0 level input current at B	V_{CC} = MAX,	V_{in} = 0.4V			-2	-3.2	mA
I_{in} (1)	Logical 1 level input current at A_1 of A_2	V_{CC} = MAX,	V_{in} = 2.4V			2	40	μA
		V_{CC} = MAX,	V_{in} = 2.4V			0.05	1	mA
I_{in} (1)	Logical 1 level input current at B	V_{CC} = MAX,	V_{in} = 2.4V			4	80	μA
		V_{CC} = MAX,	V_{in} = 5.5V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\bar{Q}$†	V_{CC} = MAX		S54121	-20	-25	-55	mA
				N74121	-18	-25	-55	mA
I_{CC}	Power supply current in quiescent (unfired) state	V_{CC} = MAX				13	25	mA
I_{CC}	Power supply current in fired state	V_{CC} = MAX				23	40	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	C_L = 15pF,	C_T = 80pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output	C_L = 15pF,	C_T = 80pF	25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	C_L = 15pF,	C_T = 80pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output	C_L = 15pF,	C_T = 80pF	30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	C_L = 15pF, R_T = Open,	C_T = 80pF Pin (9) to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	C_L = 15pF, R_T = Open,	C_T = 0. Pin (9) to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 100pF, Pin (9) Open	600	700	800	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	C_L = 15pF, R_T = 10kΩ	C_T = 1μF, Pin (9) Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	C_L = 15pF, R_T = Open,	C_T = 80pF, Pin (9) to V_{CC}		30	50	ns

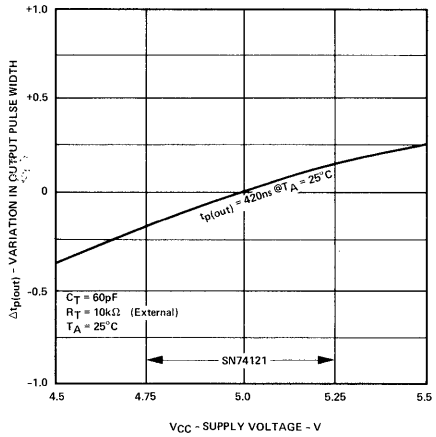
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

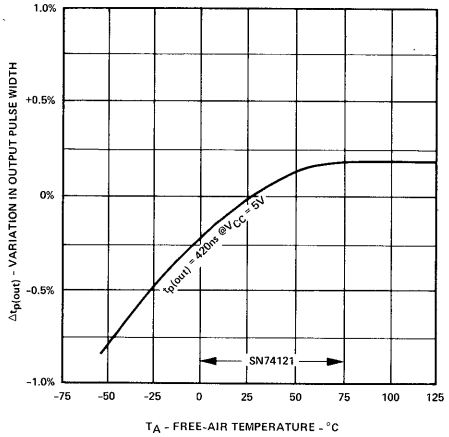
† Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

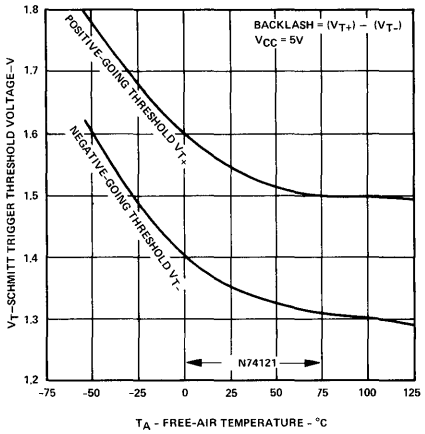


VARIATION IN OUTPUT PULSE WIDTH VERSUS FREE-AIR TEMPERATURE

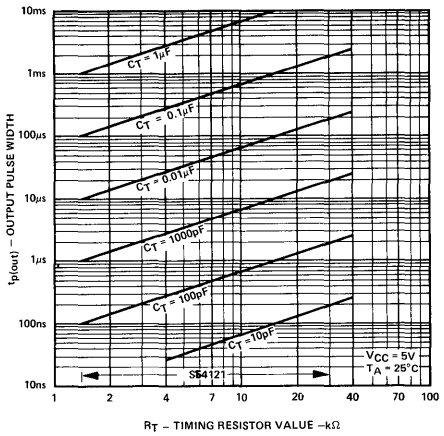


TYPICAL CHARACTERISTICS (Cont'd)

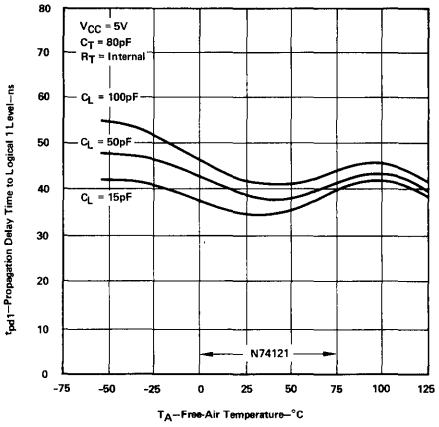
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS FREE-AIR TEMPERATURE



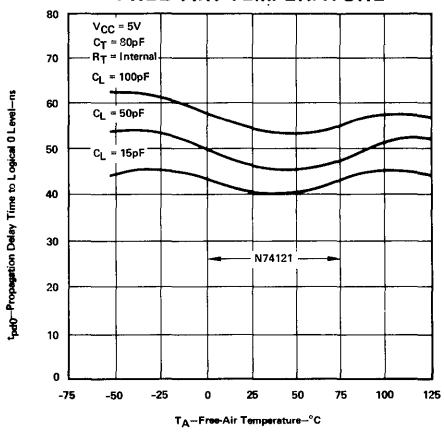
OUTPUT PULSE WIDTH VERSUS TIMING RESISTOR VALUE



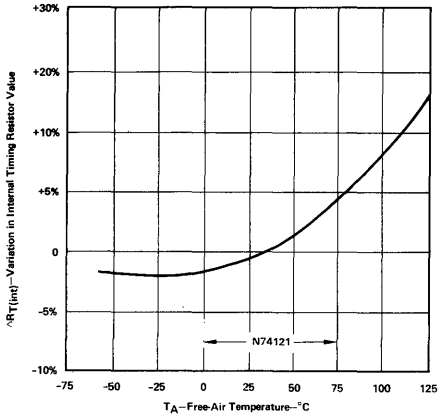
PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL (B INPUT TO Q OUTPUT) VERSUS FREE-AIR TEMPERATURE



VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS FREE-AIR TEMPERATURE



RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

N74122 S54123 N74123

N74122–A,F • S54123–B,F,W • N74123–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. N74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with N74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000pF$, the output pulse width (t_w) is defined as:

$$t_w = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

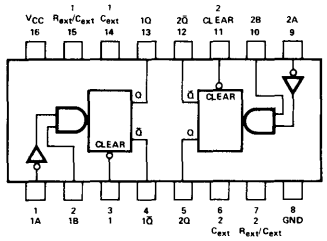
R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leqslant 1000pF$, see Figure B.

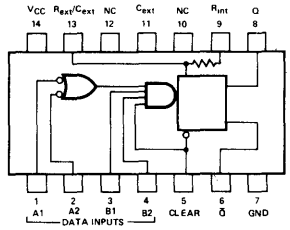
These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The N74122 and N74123 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

54/74123 B,F,W PACKAGE



74122 A,F PACKAGE



†Pin assignments for these circuits are the same for all packages.

TRUTH TABLE (See Note A)

N74122

INPUTS				OUTPUTS	
A_1	A_2	B_1	B_2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎌
L	X	H	↑	⎍	⎌
X	L	H	H	L	H
X	L	↑	H	⎍	⎌
X	L	H	↑	⎍	⎌
H	↓	H	H	⎍	⎌
↓	↓	H	H	⎍	⎌
	H	H	H	⎍	⎌

S54123,N74123

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎌
↓	H	⎍	⎌

NOTES:

A. H = high level (steady-state), L = low level (steady-state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎌ = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = No internal connection.

C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.

D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

RECOMMENDED OPERATING CONDITIONS

		S54123, N74122, N74123			UNIT
		MIN	NOM	MAX	
Supply Voltage V_{CC}		4.75	5	5.25	V
Normalized Fan-Out from each Output, N	High Logic Level			20	
	Low-Logic Level			10	
Input data setup time, t_{setup} (See Note 3)		40†			ns
Input data hold time, t_{hold} (See Note 4)		40†			ns
Width of Clear Pulse, $t_{w(clear)}$		40†			ns
External Timing Resistance		5		50	kΩ
External Capacitance		No Restriction			
Wiring Capacitance at R_{ext}/C_{ext} Terminal				50	pF
Operating Free-Air Temperature, T_A		0	25	70	°C

†These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

NOTES:
1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the N74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.
5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open. C_{ext} = 0.02μF, and R_{ext} = 25kΩ. R_{int} of S54122/N74122 is open.
7. I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open. C_{ext} = 0.02μF, and R_{ext} = 25kΩ. R_{int} of S54122/N74122 is open.

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

	PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = -12mA			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = -800μA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 16mA,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
		clear input					-3.2	
I_{OS}	Short-circuit output current†		V_{CC} = MAX,	See Note 5	-10		-40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7	N74122		23	28	mA
				N74123		46	66	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input				22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input	C_{ext} = 0, C_L = 15pF,	R_{ext} = 5kΩ, R_L = 400Ω,		30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				30	40	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000pF, C_L = 15pF,	R_{ext} = 10kΩ R_L = 400Ω	3.08	3.42	3.76	μs

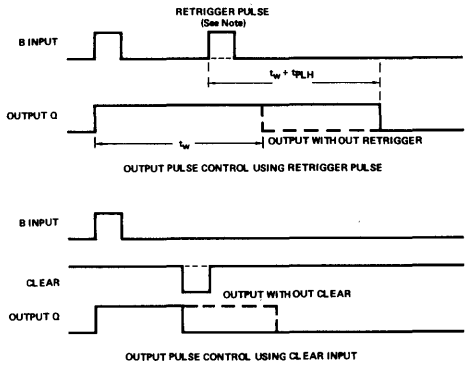
* For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

DESCRIPTION

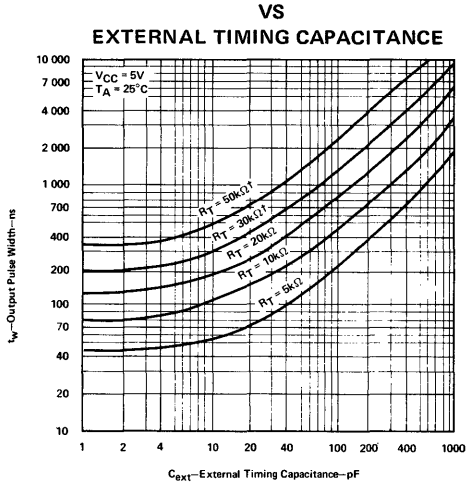
These monolithic TTL retriggerable monostable multivibrators feature dc triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

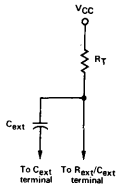
Figure A illustrates triggering the one-shot with the high-level-active (B) inputs.

TYPICAL INPUT/OUTPUT PULSES (Figure A)



TYPICAL CHARACTERISTICS (Figure B)





NOTE:
When using electrolytic capacitor, insure that minimum rating is 20 volts so that 5% reverse voltage rating is 1.0 volt or greater.

BCD-TO-DECODER/DRIVER WITH BLANKING

N74141

N74141-B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

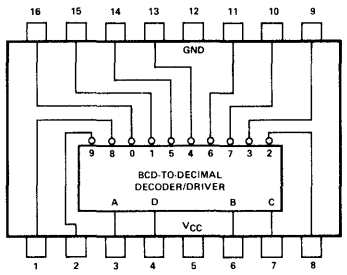
The N74141 is a BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the N74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The then high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

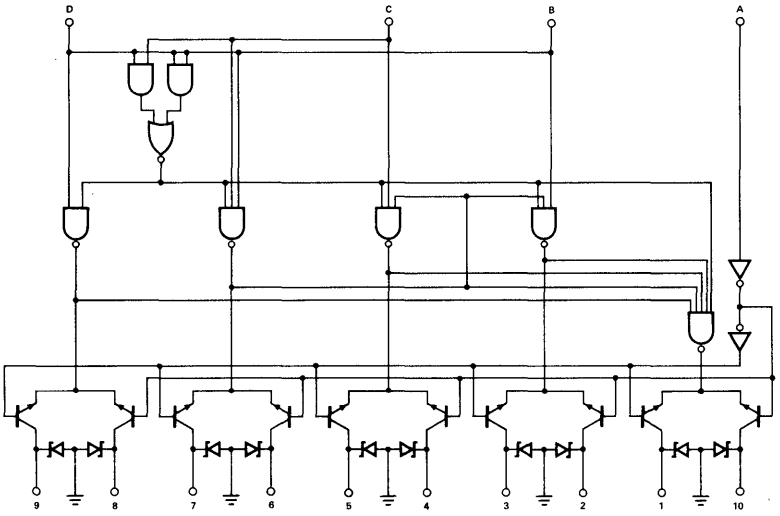
Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The N74141 is characterized for operation over the temperature range of 0°C to 70°C.

PIN CONFIGURATIONS

B PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level

*All other outputs are off

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1)	4.75	5	5.25	V
Output Voltage (See Notes 1 and 2)			65	V
Operating Free-Air Temperature Range	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, I_O = 7mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	V_{CC} = MAX, I_O = 0.5mA	65			V
$I_{O(off)}$	Off-state reverse current	V_{CC} = MAX, V_O = 55V			50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15	V_{CC} = MAX, V_O = 30V			5	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current into A					
I_{IL}	Low-level input current into	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
	B, C, or D				-3.2	mA
I_{CC}	Supply current	V_{CC} = MAX		11	16	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

** This typical value is at V_{CC} = 5V, T_A = 25°C.

NOTE: SEE THE 8T02 FOR IMPROVED PERFORMANCE IN THE SAME PIN CONFIGURATION.

16-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

S54150 N74150

S54150–N,Q,F • N74150–N,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54/74150 is a one-of-sixteen data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line.

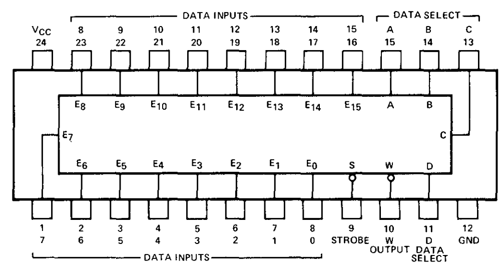
The S54150/N74150 is provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

This data selector/multiplexer is fully compatible for use with other TTL or DTL circuit. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

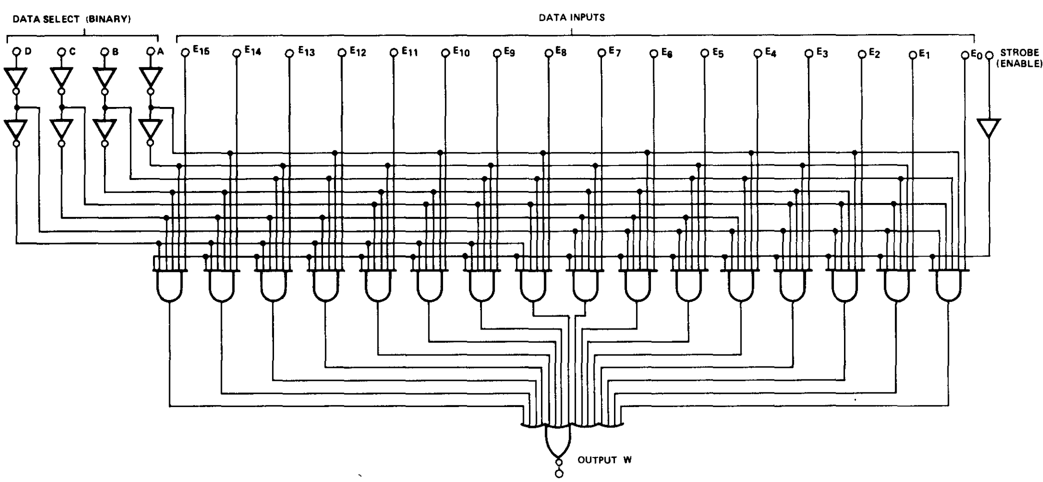
S54150/N74150 – 200 milliwatts.

PIN CONFIGURATIONS

N,Q,F PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUTS																					OUTPUT
D	C	B	A	STROBE	e_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54150 Circuits	4.5	5	5.5	V
N74150 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Logical 0			10	
Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	-20		-55	mA
		V_{OUT} = 0	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V		40	68	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	C_L = 15pF, R_L = 400Ω		20	30	ns
t_{pd1}	A,B,orC(4levels)	Y			35	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D_0 thru D_7	Y			16	24	ns
t_{pd1}	D_0 thru D_7	Y			19	29	ns
t_{pd0}	E_0 thru E_{15}	W			8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

S54151
N74151

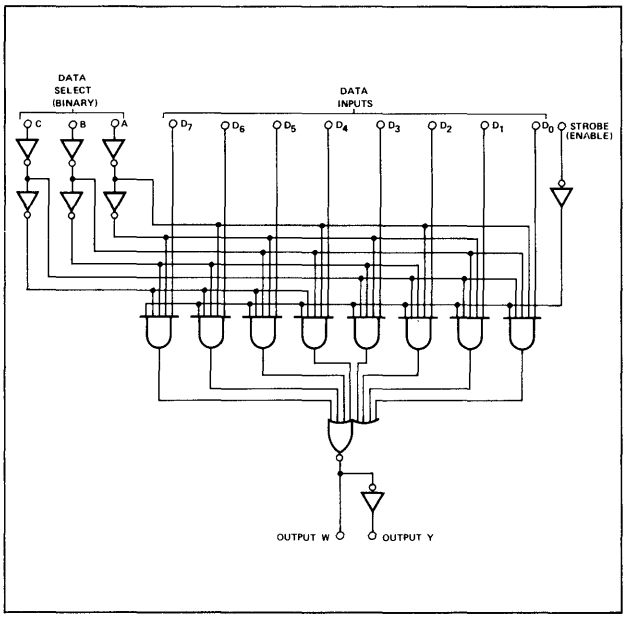
S54151—B,F,W • N74151—B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

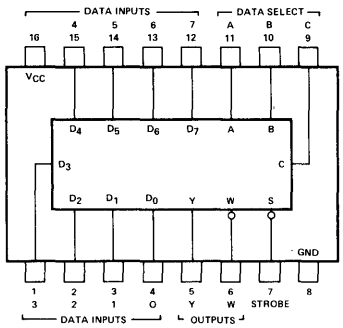
The 54/74151 is a one-of-eight data selector which performs parallel-to-serial data conversion. The unit incorporates an enable circuit for chip select. This allows multiplexing from N-lines to one-line. Both true and complement outputs are available.

LOGIC DIAGRAM

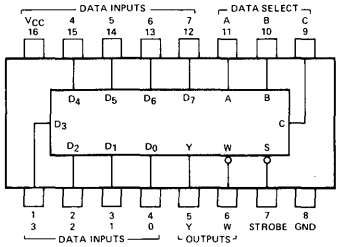


PIN CONFIGURATIONS

W PACKAGE



B,F PACKAGE



TRUTH TABLE

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = irrelevant.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54151 Circuits	4.5	5	5.5	V
N74151 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Logical 0			10	
Logical 1			20	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, V_{out} = 0	-20		-55	mA
			-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V		29	48	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	C_L = 15pF, R_L = 400Ω		20	30	ns
t_{pd1}	A,B,orC(4 levels)	Y			35	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D_0 thru D_7	Y			16	24	ns
t_{pd1}	D_0 thru D_7	Y			19	29	ns
t_{pd0}	E_0 thru E_{15}	W			8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

S54152

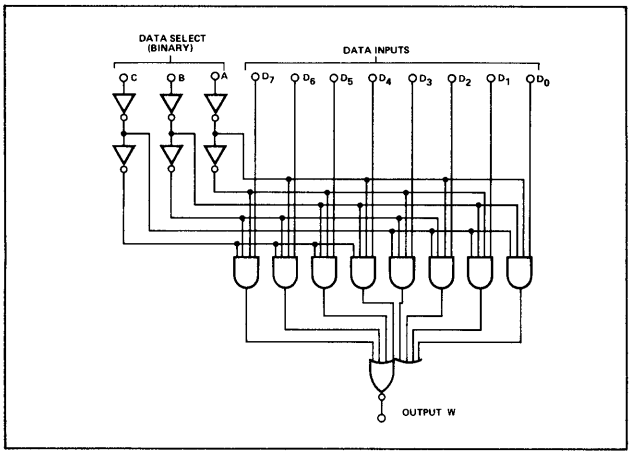
S54152–W

DIGITAL 54/74 TTL SERIES

DESCRIPTION

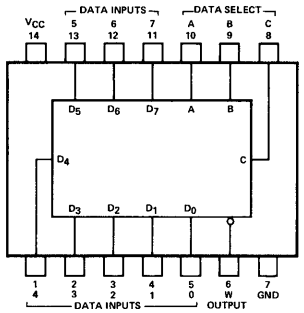
The S54152 is a one-of-eight data selector which performs parallel to serial data conversion. The S54152 is identical to the S54152 with the exclusion of the true output and strobe. It is available in the 14-pin flatpak only.

LOGIC DIAGRAM



PIN CONFIGURATIONS

W PACKAGE



TRUTH TABLE

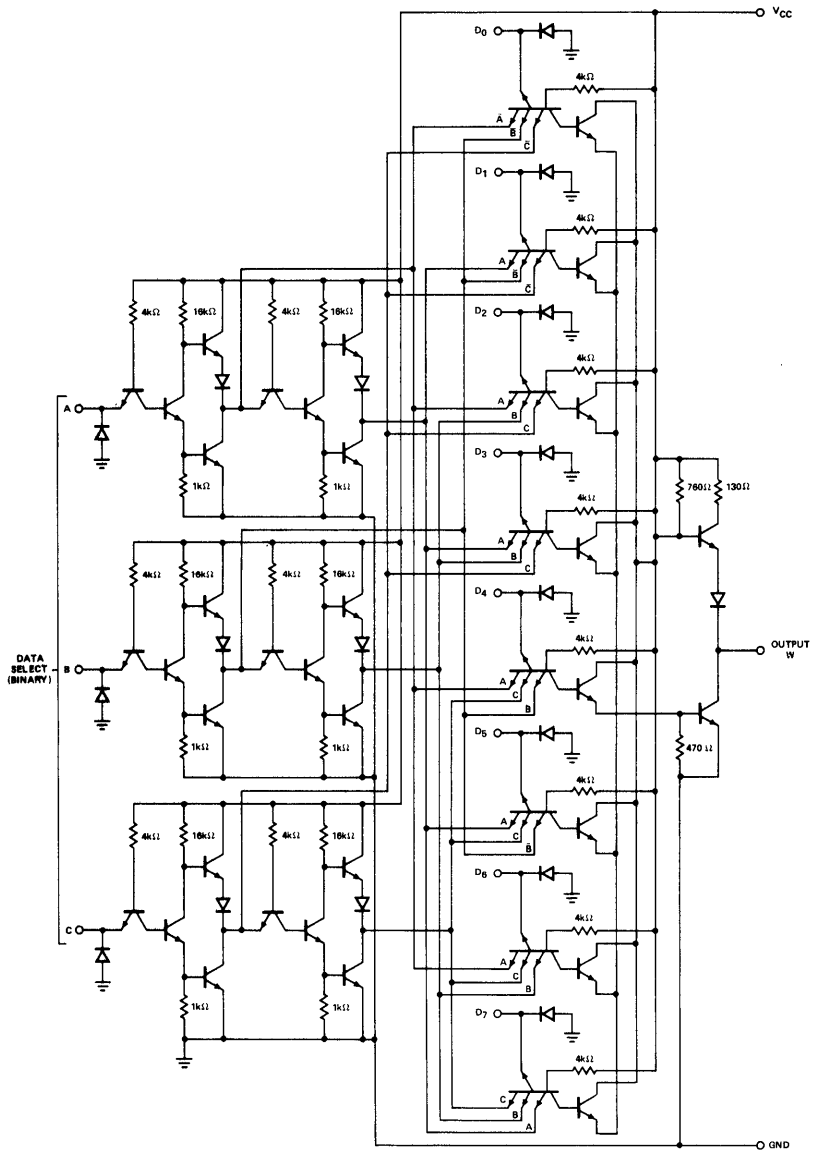
INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input, X = Irrelevant.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54152 Circuits	4.5	5	5.5	V
Normalized Fan-Out from each Output, N: Logical 0			10	
Logical 1			20	

SCHEMATIC DIAGRAM



Component values shown are nominal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input (each input)	V_{CC} = MAX, V_{in} = 2.4V			40	μA
		V_{CC} = MAX, V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX, V_{in} = 0.4V			-1.6	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX, V_{out} = 0	-20		-55	mA
			-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX, V_{in} = 4.5V		26	43	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A,B,orC(4 levels)	Y	C_L = 15pF, R_L = 400Ω		20	30	ns
t_{pd1}	A,B,orC(4 levels)	Y			35	52	ns
t_{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t_{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t_{pd0}	STROBE	Y			19	30	ns
t_{pd1}	STROBE	Y			35	52	ns
t_{pd0}	STROBE	W			21	30	ns
t_{pd1}	STROBE	W			15.5	24	ns
t_{pd0}	D_0 thru D_7	Y			16	24	ns
t_{pd1}	D_0 thru D_7	Y			19	29	ns
t_{pd0}	E_0 thru E_{15}	W			8.5	14	ns
t_{pd1}	E_0 thru E_{15}	W			13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DUAL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER

S54153
N74153

S54153—B,F,W • N74153—B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

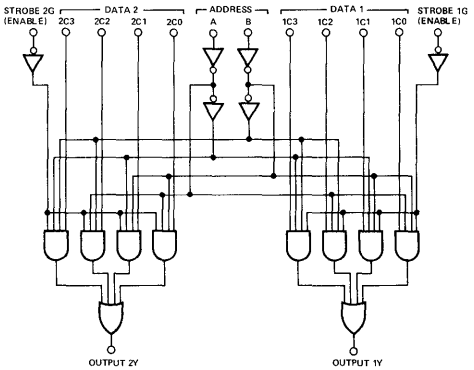
Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The S54153 is characterized for operation over the full military temperature range of -55°C to 125° C; the N74153 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

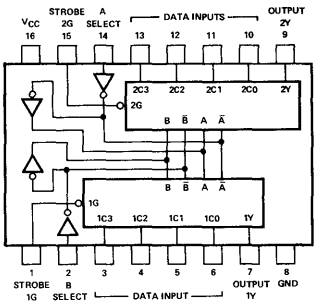
Address inputs A and B are common to both sections. H = high level, L = low level, X = irrelevant.

LOGIC DIAGRAM

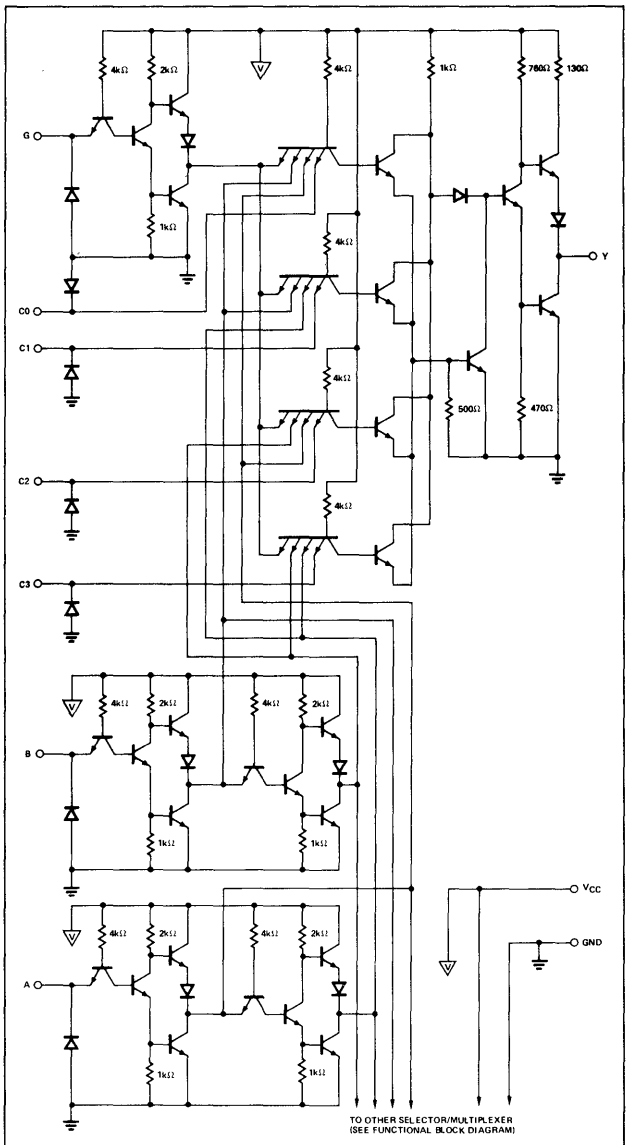


PIN CONFIGURATIONS

B,F,W PACKAGE



SCHEMATIC DIAGRAM



$-V_{CC}$ bus

NOTE:
Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	S54153			N74153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
High Logic Level			20			20	
Low Logic Level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA		0.2	0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX,	S54153	-20		-55	mA
			N74153	-18		-57	
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	S54153		36	52	mA
			N74153		36	60	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y			12	18	ns
t_{PHL}	Data	Y			15	23	ns
t_{PLH}	Address	Y			22	34	ns
t_{PHL}	Address	Y	C_L = 30pF, R_L = 400Ω		22	34	ns
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}	Strobe	Y			15	23	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

4-LINE TO 16 LINE DECODER/DEMULTIPLEXER

S54154
N74154

S54154–N,Q,F • N74154–N

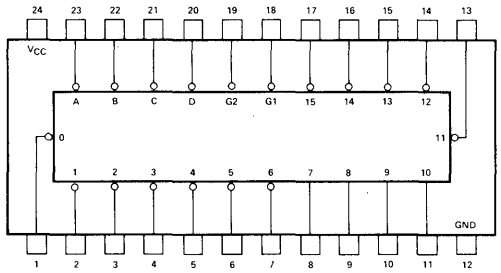
DIGITAL 54/74 TTL SERIES

DESCRIPTION

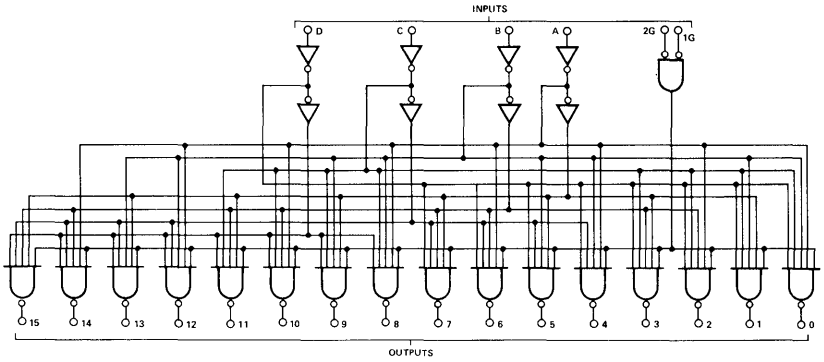
The 54/74154 decodes 4 binary-coded inputs to one of 16 mutually exclusive outputs when each of the two strobe inputs are low. The demultiplexing function is achieved by using the 4 input lines for output addressing and data from one strobe input while the other strobe input is held low.

PIN CONFIGURATIONS

N,Q,F PACKAGE



LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High, L = Low, X = Irrelevant

RECOMMENDED OPERATING CONDITIONS

	S54154			N74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: Low logic level			10			10	
High logic level			20			20	
Operating Free-Air Temperature Range	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.4V				40	A
		V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	S54154	-20		-55	mA
			N74154	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX	S54154		34	49	mA
			N74154		34	56	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15pF, R_L = 400Ω		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

S54155
S54156
N74155
N74156

S54155–B,F,W • S54156–B,F,W • N74155–B • N74156–B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired.

Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3- to 8-line decoder or 1- to 8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

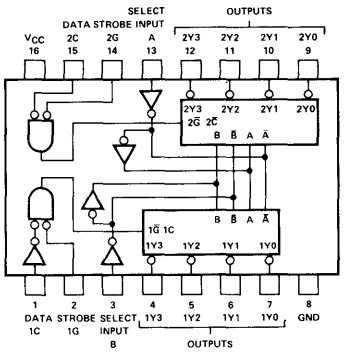
The S54155/N74155 circuits, with totem pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The S54156/N74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the S54155/N74155.

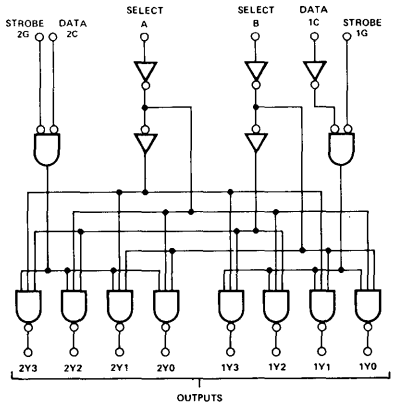
The S54155 and S54156 are characterized for operation over the full military temperature range of −55°C to 125°C the N74155 and N74156 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



TRUTH TABLES

TRUTH TABLES (H = High Level, L = Low Level, X = Irrelevant)

2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

RECOMMENDED OPERATING CONDITIONS

	S54155			N74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

	S54156			N74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			S54155,N74155 MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -800μA	V_{IH} = 2V,		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_{IL} = 0.8V,				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V				40	μA
		V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		S54155	-20		-55	mA
				N74155	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX		S54155		25	35	mA
				N74155		25	40	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			S54156,N74156 MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_I = 2V,				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_{IL} = 0.8V,				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V				40	μA
		V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{CC}	Supply current	V_{CC} = MAX		S54156		25	35	mA
				N74156		25	40	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	S54155 N74155 MIN	TYP	MAX	S54156 N74156 MIN	TYP	MAX	UNIT
t_{PLH}	A,B,2C, 1G,or2G	Y	2			13	20		15	23	ns
t_{PHL}	A,B,2C, 1G,or2G	Y	2	C_L = 15pF,		18	27		20	30	ns
t_{PLH}	A or B	Y	3	R_L = 400Ω		21	32		23	34	ns
t_{PHL}	A or B	Y	3			21	32		23	34	ns
t_{PLH}	1C	Y	3			16	24		18	27	ns
t_{PHL}	1C	Y	3			20	30		22	33	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

TYPICAL APPLICATION DATA

The S54155, N74155, S54156, or N74156 may be used as a dual 2-line to 4-line decoder or a 1-line to 4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

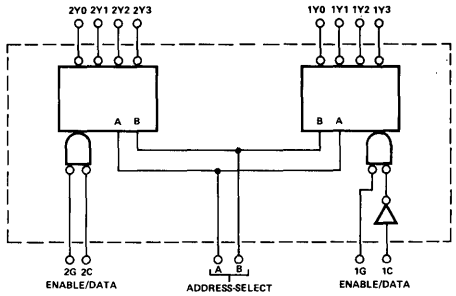
Any of these circuits may also be used as a 3-line to 8-line decoder or a 1-line to 8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.

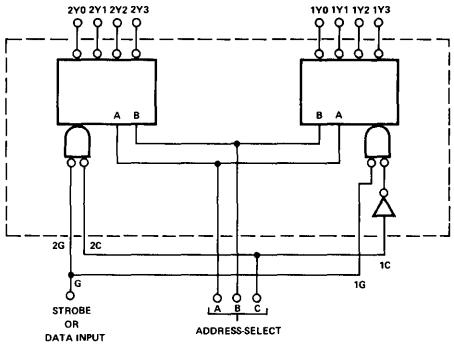
DUAL 2-LINE TO 4-LINE DECODER/1-TO 4-LINE DEMULTIPLEXER

S54155, N74155, S54156, N74156



3-LINE TO 8-LINE DECODER/1-TO 8-LINE DEMULTIPLEXER

S54155, N74155, S54156, N74156



QUADRUPLE 2-INPUT DATA SELECTOR/MULTIPLEXER

S54157
S54158
N74157
N74158

S54157—B,F,W • N74157—B,F • S54158—B,F,W • N74158—B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54157/N74157 and S54158/N74158 are identical with the exception of the S54158/N74158 being inverted. These devices are logical implementations of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The devices provide the ability, in one package, to select four bits of either data or control from two sources. By proper manipulation of the inputs, it can generate four functions of two variables with one variable common. Thus any number of random topic elements used to generate unusual truth tables can be replaced. All outputs are low when disabled (enable high). Both inputs and outputs are buffered.

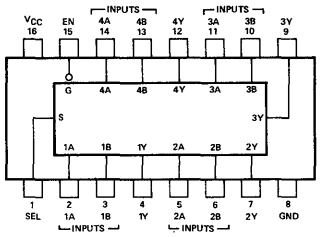
TRUTH TABLE

INPUTS				OUTPUT Y
ENABLE	SELECT	A	B	S54/N74157
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Irrelevant

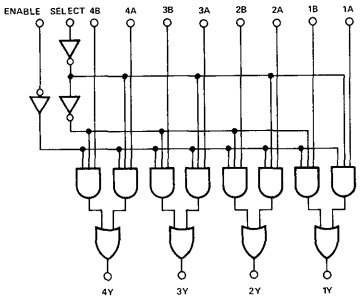
PIN CONFIGURATION

B,F,W PACKAGE

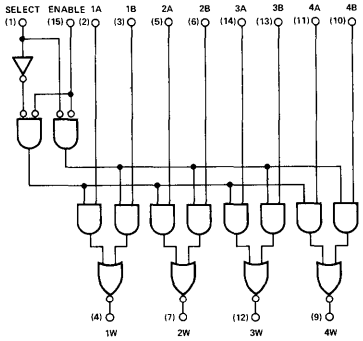


LOGIC DIAGRAMS

N74157



S54/N74158



RECOMMENDED OPERATING CONDITIONS

	S54157/58			N74157/58			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
High Logic Level			20			20	
Low Logic Level			10			10	
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54157/58			N74157/58			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-55	-18		-55	mA
I_{CC}	Supply current	V_{CC} = MAX			30	48		30	48	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Data	Output			9	14	ns
t_{PLH}	Data	Output	C_L = 15pF, R_L = 400		9	14	ns
t_{PHL}	Enable	Any Output			14	21	ns
t_{PLH}	Enable	Any Output			13	20	ns
t_{PHL}	Select	Any Output			18	27	ns
t_{PLH}	Select	Any Output			15	23	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

SYNCHRONOUS 4-BIT COUNTER

S54160 N74160
S54161 N74161
S54162 N74162
S54163 N74163

S54160–B,F,W • S54161–B,F,W • S54162–B,F,W • S54163–B,F,W
N74160–B,F • N74161–B,F • N74162–B,F • N74163–B,F

DIGITAL 54/74 TTL SERIES

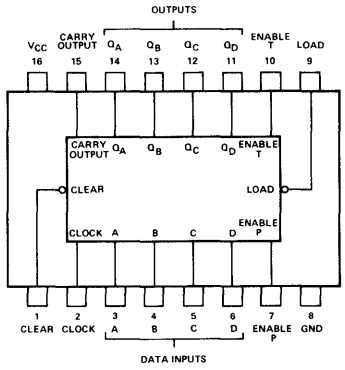
DESCRIPTION

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The S54160, S54162, N74160, and N74162 are decade counters and the S54161, S54163, N74161, and N74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs and power dissipation is typically 325 milliwatts.

PIN CONFIGURATION

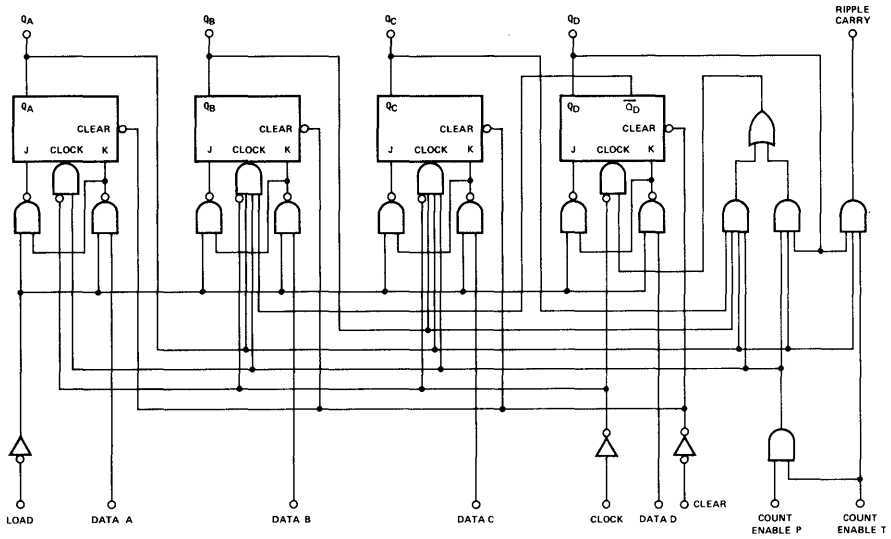
B,F,W PACKAGE



LOGIC DIAGRAM

S54160/N74160 SYNCHRONOUS DECADE COUNTERS

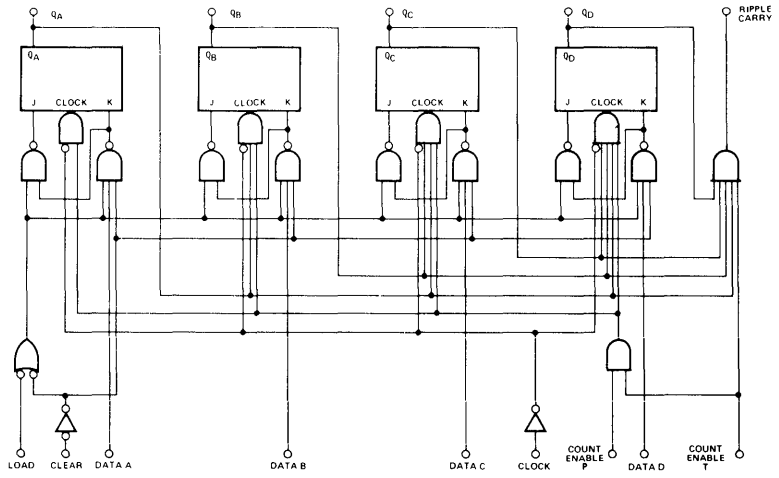
(S54162/N74162 synchronous decade counters are similar; however the clear is synchronous as shown for the S54163/N74163 binary counters).



LOGIC DIAGRAM (Cont'd)

S54163/N74163 SYNCHRONOUS BINARY COUNTERS

S54161/N74161 synchronous binary counters are similar; however the clear is asynchronous as shown for the S54160/N74160 decade counters).



RECOMMENDED OPERATING CONDITIONS

	S54160, S54161 S54162, S54163			N74160, N74161 N74162, N74163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock Pulse, $t_{w(clock)}$	25			25			ns
Width of Clear Pulse, $t_{w(clear)}$	20			20			ns
Setup Time, t_{setup}: Data Inputs, A,B,C,D	15			15			
Enable P	20			20			
Load	15			15			ns
Clear	20			20			
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise specified)

PARAMETER		TEST CONDITIONS*		S54160,S54161 S54162,S54163			N74160,N74161 N74162,N74163			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MAX,				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current: Clock or enable T	V_{CC} = MAX,	V_I = 2.4V			80			80	μA
	Other inputs					40			40	
I_{IL}	Low-level input current: Clock or enable T	V_{CC} = MAX,	V_I = 0.4V			-3.2			-3.2	mA
	Other inputs					-1.6			-1.6	
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CCL}	Supply current, all outputs high	V_{CC} = MAX,	See Note 3		59	85		59	94	mA
	Supply current, all outputs low	V_{CC} = MAX,	See Note 4		63	91		63	101	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T			8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			20	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

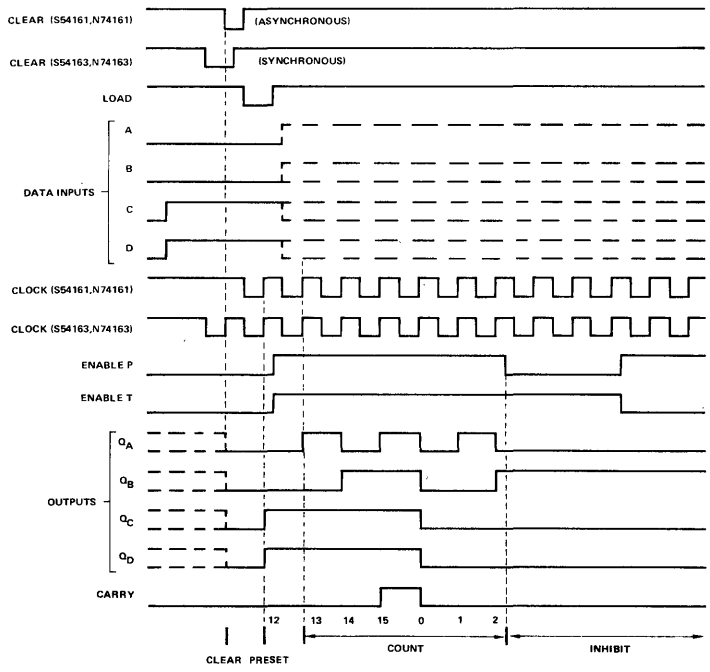
NOTES:

3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

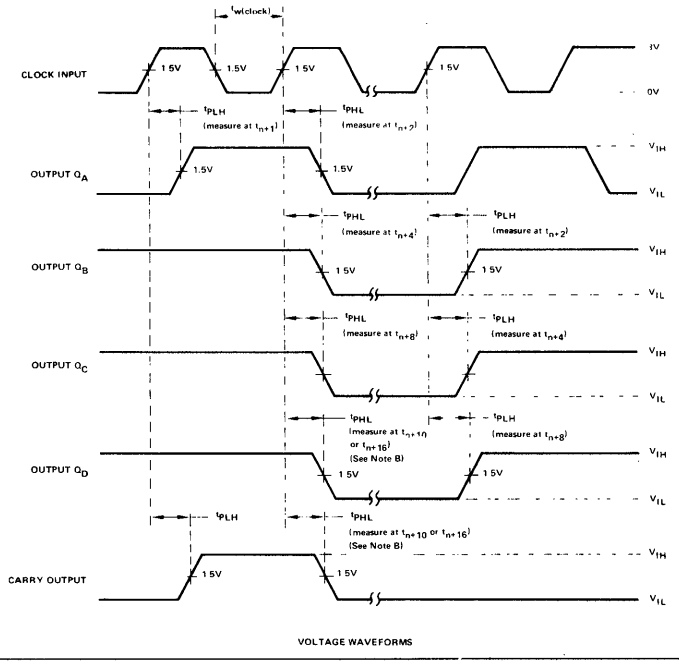
TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



PARAMETER MEASUREMENT INFORMATION

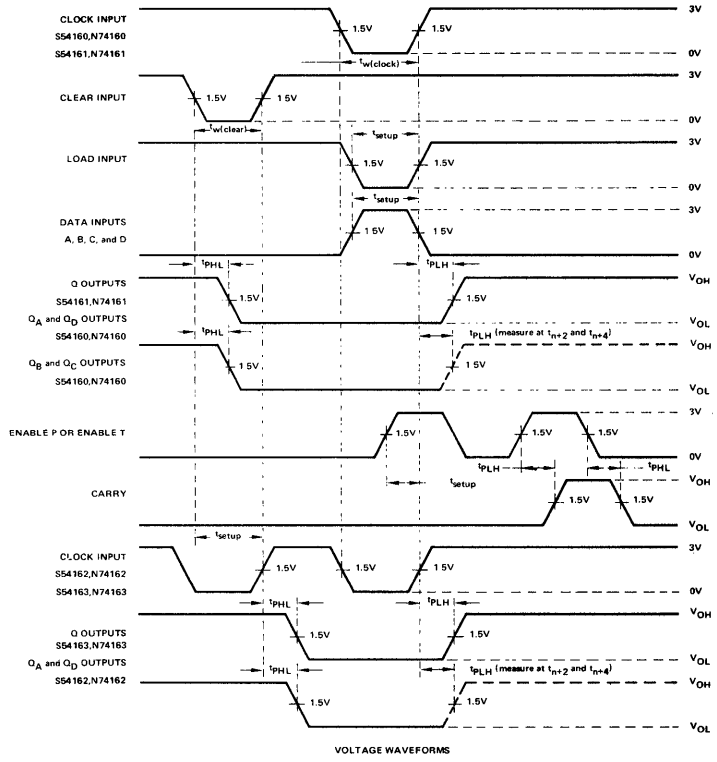


VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10ns$; $t_f \leq 10ns$. PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the S54160, S54162, N74160, and N74162, and at t_{n+16} for the S54161, S54163, N74161, and N74163, where t_n is the bit time when all outputs are low.



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10ns$; $t_f \leq 10ns$; PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%; $Z_{out} \approx 50\Omega$.

B. Enable P and enable T setup times are measured at $t_n = 0$.

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

S54164
N74164

S54164—A,F,W • N74164—A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The S54164 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74164 is characterized for operation from 0°C to 70°C.

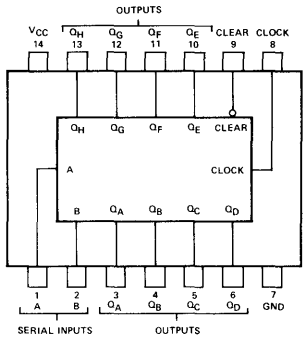
TRUTH TABLE

SERIAL INPUTS A AND B

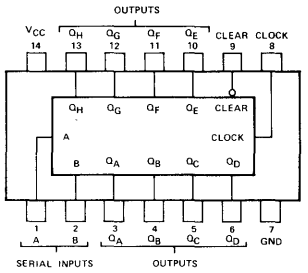
INPUTS AT_{t_n}		OUTPUT AT_{t_n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

PIN CONFIGURATIONS

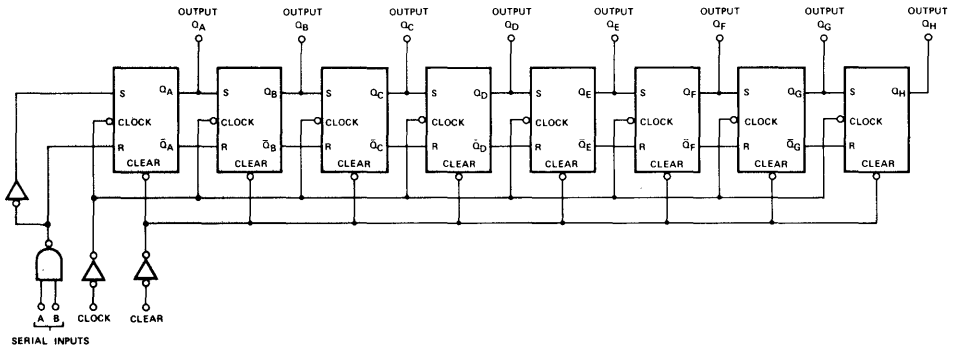
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54164			N74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			10			10	
Low logic level			5			5	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock or Clear Input Pulse, t_w	20			20			ns
Data Setup Time, t_{setup}	15			15			ns
Data Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		S54164			N74164			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 8mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		-10		-27.5	-9		-27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note	$V_{I(clock)}$ = 0.4V		30			30		mA
			$V_{I(clock)}$ = 2.4V		37	54		37	54	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 5

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	C_L = 15pF		24	36	ns
		C_L = 50pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input	C_L = 15pF	8	17	27	ns
		C_L = 50pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input	C_L = 15pF	10	21	32	ns
		C_L = 50pF	10	25	37	

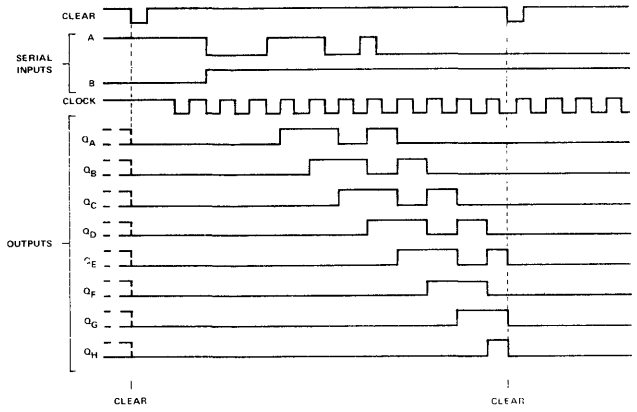
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

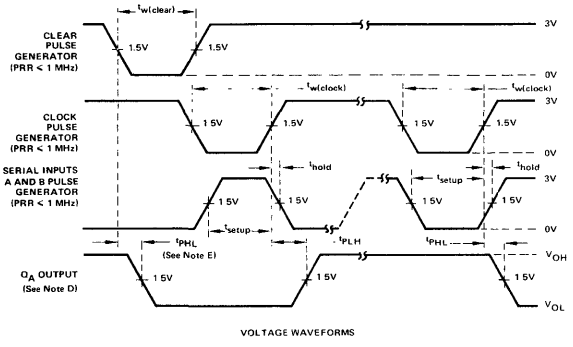
† Not more than two outputs should be shorted at a time.

NOTE : I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V, applied to clear.

TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES



PARAMETER MEASUREMENT INFORMATION



NOTES:
A. The pulse generators have the following characteristics: $t_r \leq 10$ns, $t_f \leq 10$ns, duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

PARALLEL-LOAD 8-BIT SHIFT REGISTER

S54165
N74165

S54165–B,F,W • N74165–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

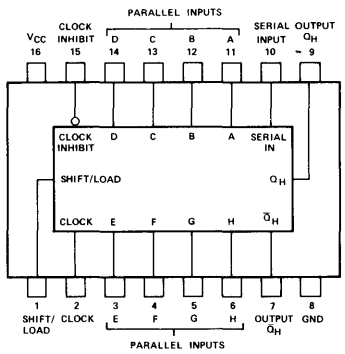
The S54165 and N74165 are 8-bit serial shift registers that shift data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

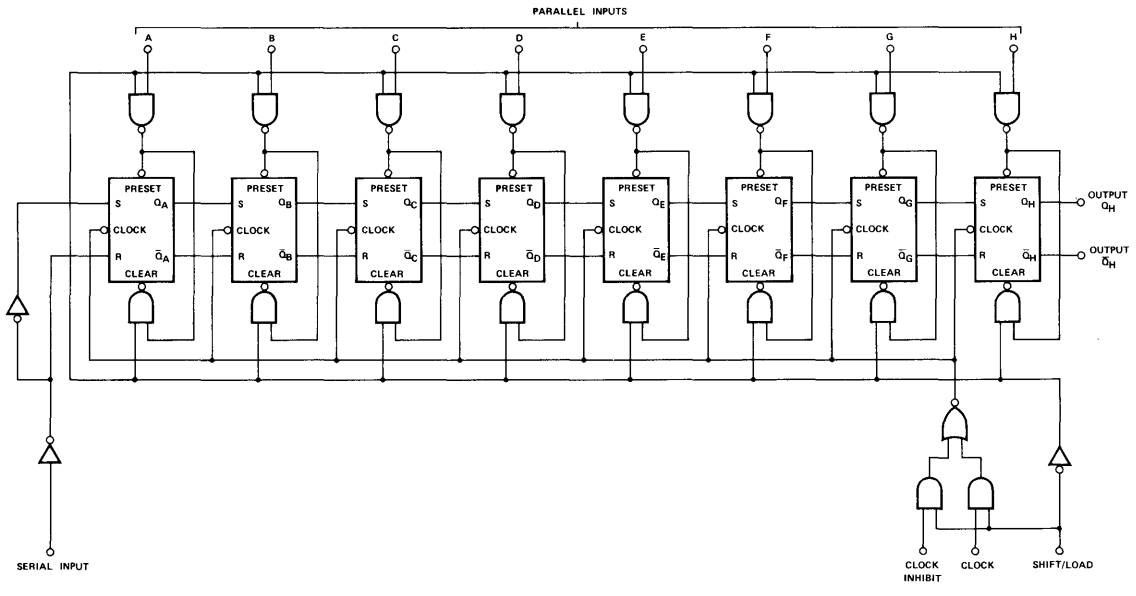
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The S54165 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74165 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54165			N74165			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		20	0		20	MHz
Width of Clock Input Pulse, $t_{w(clock)}$	25			25			ns
Width of Load Input Pulse, $t_{w(load)}$	15			15			ns
Clock-Enable Setup Time, t_{setup}	30			30			ns
Parallel Input Setup Time, t_{setup}	10			10			ns
Serial Input Setup Time, t_{setup}	20			20			ns
Shift Setup Time, t_{setup}	45			45			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS *	S54165			N74165			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = -12 mA			- 1.5			-1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	Load Input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			-3.2			-3.2	mA
		Other inputs				-1.6			-1.6	
I_{OS}	Short-circuit output current †		V_{CC} = MAX	-20		-55	-18		-55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note		42	63		42	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				20	26		MHz
t_{PLH}					21	31	
t_{PHL}	Load	Any			27	40	ns
t_{PLH}	Clock	Any	C_L = 15 pF, R_L = 400 Ω,		16	27	ns
t_{PHL}					21	34	
t_{PLH}					11	20	
t_{PHL}	H	Q_H			24	36	ns
t_{PLH}					18	27	
t_{PHL}	H	$\bar{Q}_H$			18	27	ns

NOTE : With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5 V, T_A = 25°C.

† Not more than one output should be shorted at a time.

f_{max} ≡ Maximum input count frequency

t_{PLH} ≡ Propagation delay time, low-to-high-level output

t_{PHL} ≡ Propagation delay time, high-to-low-level output

8-BIT SHIFT REGISTER

S54166
N74166

S54166–B,F,W • N74166–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

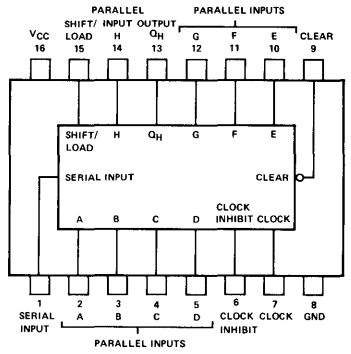
These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C. Series 74 devices are characterized for operation from 0°C to 70°C.

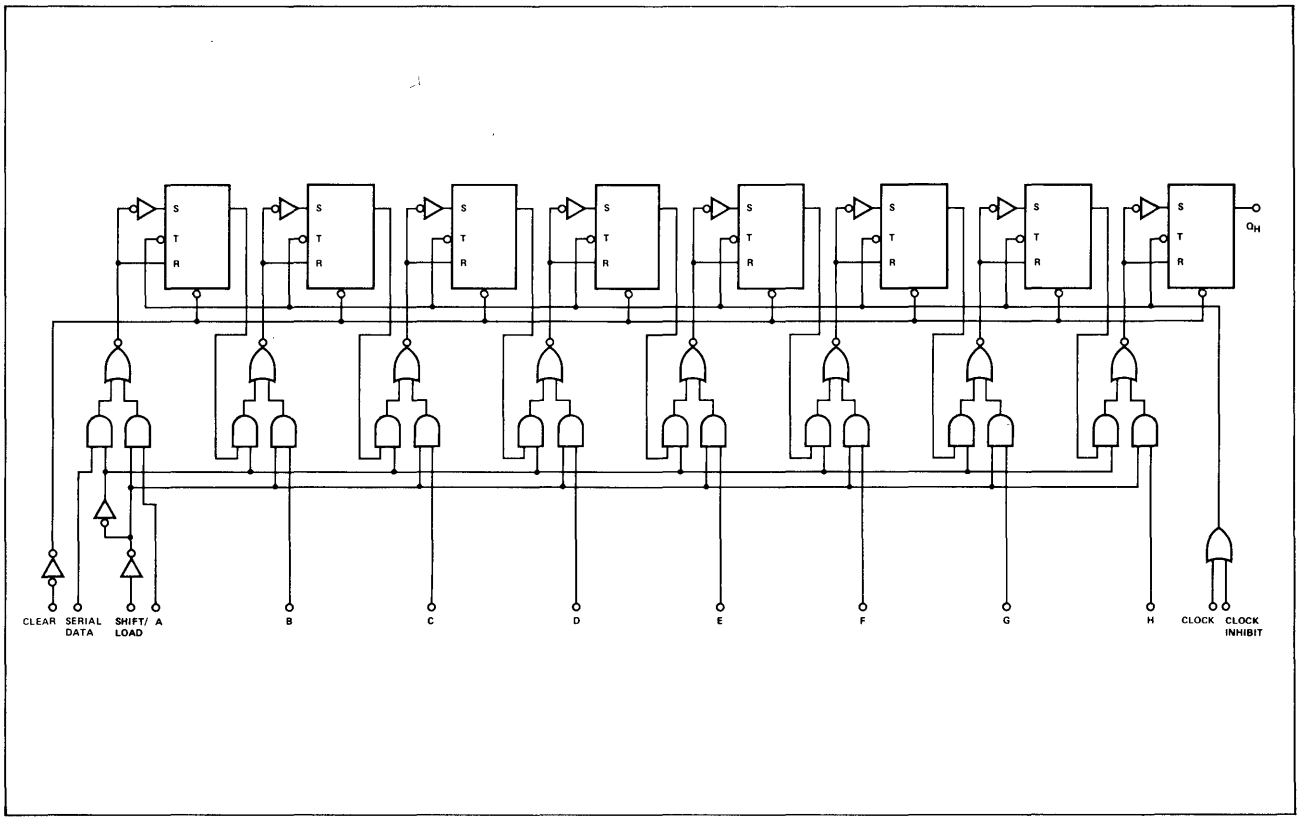
These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54166			N74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	S54166			N74166			UNIT
			MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX, Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54166, N74166	Serial Input	Clock	All other inputs

4×4 REGISTER FILE

S54170
N74170

S54170–B,F,W • N74170–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54170 and 74170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates on a monolithic chip. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W is high, the data inputs are inhibited and their states can cause no change in the information stored in the internal latches. When the read enable output, G_R, is high, the data outputs are inhibited and remain high.

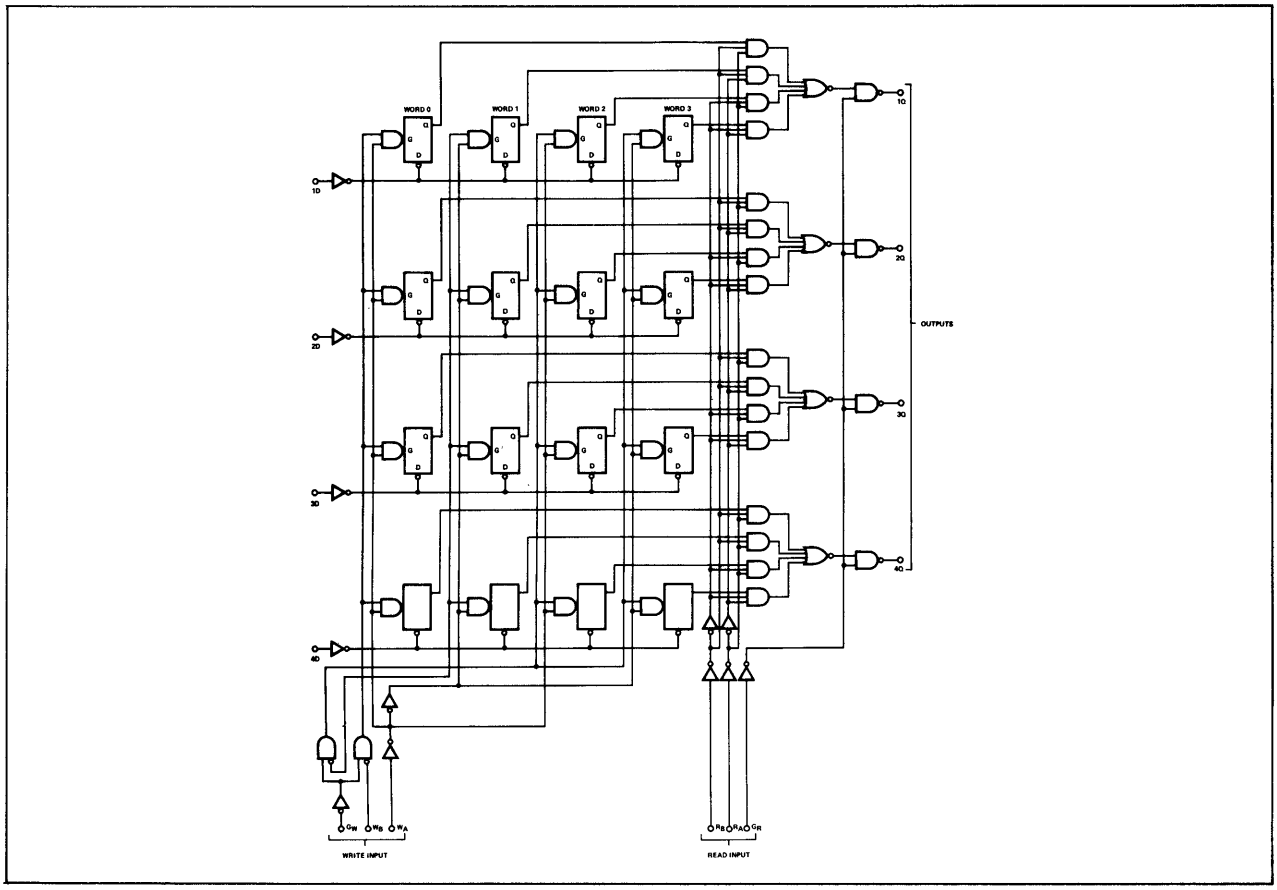
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a non-destructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Power dissipation is typically 500 mW total or 5 mW per gate. The 54170 is characterized for operation over the full military temperature range of -55°C to 125°C; the 74170 is characterized for operation from 0°C to 70°C.

LOGIC DIAGRAM



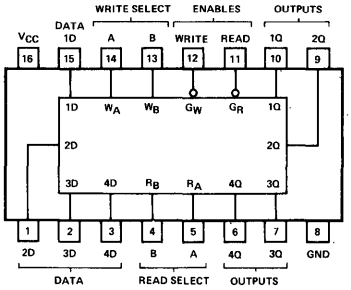
ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range:
54170 Circuits . . . . . -55°C to 125°C
74170 N Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . -65°C to 150°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

PIN CONFIGURATION

B,F,W, PACKAGE



RECOMMENDED OPERATING CONDITIONS

		54170			74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (See Note 3)	data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	write select with respect to write enable, $t_{setup(W)}$	15			15			ns
	read select with respect to read enable, $t_{setup(R)}$	5			5			ns
Hold times, high- or low-level data (See Note 4)	data input with respect to write enable, $t_{hold(D)}$	0			0			ns
	write select with respect to write enable, $t_{hold(W)}$	5			5			ns
	read select with respect to read enable, $t_{hold(R)}$	5			5			ns
Latch time for new data, t_{latch} (See Note 5)		25			25			ns
Operating free-air temperature range, T_A		-55	25	125	0	25	70	°C

NOTES:
3. Setup time is the interval immediately preceding the negative-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its continued recognition.
5. Latch time is the time required for the internal output of the latch to assume the state of new data. See Figure 1. This is important only when attempting to read from a location immediately after that location has received new data.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12 mA			-1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_O = 5.5 V			30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			-1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, see Note 6	54170		125 ‡	140	mA
			74170		125 ‡	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Typical power dissipation shown is an average for 50% duty cycle at V_{CC} = 5 V, T_A = 25°C.

NOTE 6:

Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		10	15	ns
t_{PHLq}	Propagation delay time, high-to-low-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		20	30	ns

LOGIC

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q = D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q = D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q = D
X	X	H	Q_n	Q_n	Q_n	Q_n

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	1Q	2Q	3Q	4Q
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES:

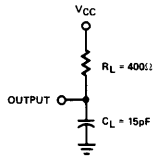
A. H = high level, L = low level, X = irrelevant

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_n = No change.

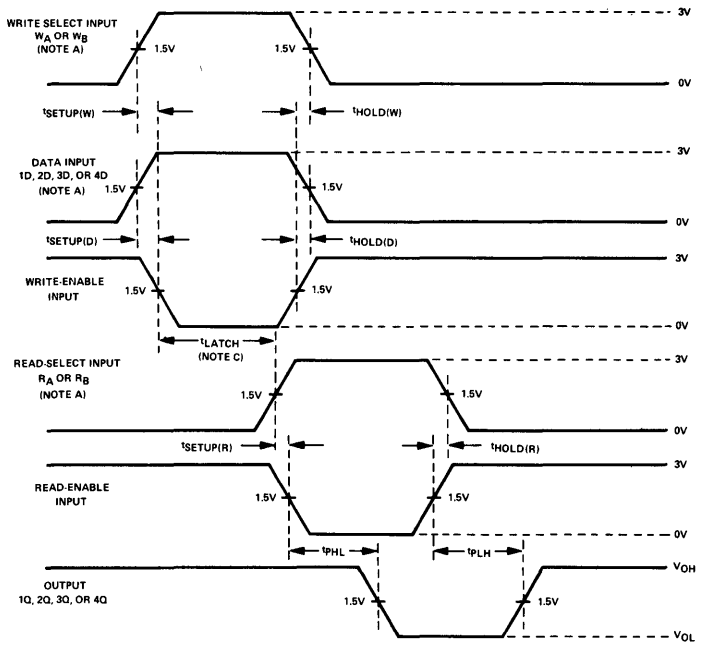
D. W0B1 = The first bit of word 0, etc.

SWITCHING CHARACTERISTICS



LOAD FOR OUTPUT UNDER TEST

VOLTAGE WAVEFORMS



NOTES:

A. Hign-level inputs are illustrated; however, low-level setup and hold times are the same.

B. Waveforms are supplied by generators with the following characteristics: PRR ⩽ 1MHz, $Z_{OUT} \approx 50\Omega$, duty cycle ⩽ 50%, $t_r \leqslant 10$ns, $t_f = 10$ns.

C. This applies only when reading from a location immediately after that location has received new data.

QUADRUPLE D-TYPE EDGE-TRIGGERED FLIP-FLOPS

S54175
N74175

S54175–B,F,W • N74175–B,F

DIGITAL 54/74 TTL SERIES

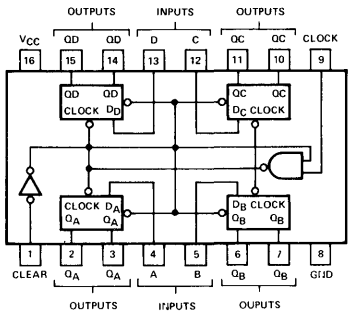
DESCRIPTION

These monolithic, positive-edge-triggered flip-flops utilize TTL circuits to implement the D-type flip-flop logic. Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 low logic-level loads and 20 high-logic-level loads is available from each of the outputs. This simplifies system design by allowing unused inputs to be tied to driven inputs. Maximum clock frequency is typically 25 megahertz, with a typical power dissipation of 38 milliwatts per flip-flop.

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

INPUT	OUTPUT
t_n	$t_n + 1$
D	Q
H	H
L	L

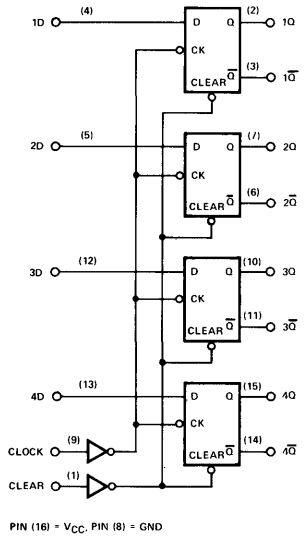
t_n = Bit time before clock pulse transition.
$t_n + 1$ = Bit time after clock pulse transition.

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply voltage V_{CC} (See Note 1)	7 V
Input voltage (See Note 1)	5.5 V
Operating free-air temperature range:	
54175 Circuits	-55°C to 125°C
74175 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1:
Voltage values are with respect to network ground terminal.

LOGIC DIAGRAM



PIN (16) = V_{CC}, PIN (8) = GND

RECOMMENDED OPERATING CONDITIONS

	54175			74175			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N — High Logic Level			20			20	
Low Logic Level			10			10	
Input clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_W	20			20			ns
Data setup time, t_{setup}	20			20			ns
Hold time t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55	25	125	0	25	70	°C
Clear release setup, $t_{release}$	25			25			ns

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		54175 MIN	54175 TYP	54175 MAX	74175 MIN	74175 TYP	74175 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12 mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, J_{OH} =-800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2V, J_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX								
		Note 1	54175							
			74175		30	45		30	45	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output Q from clear	C_L = 15 pF R_L = 400		23	35	ns
t_{PLH}	Propagation delay time low-to-high-level output Q from clear (54175, 74175)			16	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns

8-BIT ODD/EVEN PARITY GENERATOR/CHECKER

S54180
N74180

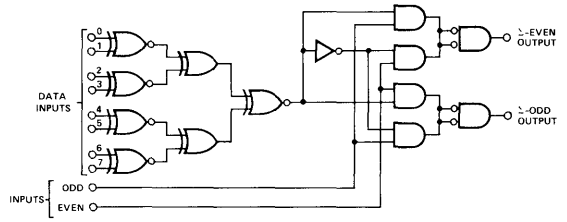
S54180–A,F,W • N74180–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

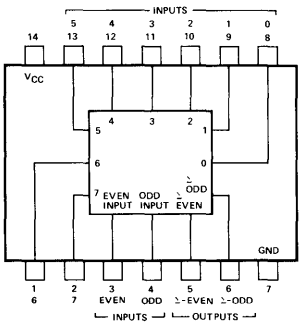
The 54/74180 8-Bit Odd/Even Parity Generator/Checker is a TTL monolithic array featuring gating logic arranged to generate or check odd or even parity.

LOGIC DIAGRAM

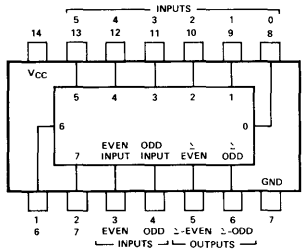


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	S54180	4.5	5	5.5	V
	N74180	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	Logical 0			10	V
	Logical 1			20	V

NOTE: 1. These voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V, $V_{in(0)}$ = 0.8V, I_{load} = -800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V, I_{sink} = 16mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	V_{CC} = MAX, V_{in} = 2.4V				40	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	V_{CC} = MAX, V_{in} = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	V_{CC} = MAX, V_{in} = 2.4V				80	μA
		V_{CC} = MAX, V_{in} = 5.5V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	V_{CC} = MAX, V_{in} = 0.4V				-3.2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	S54180	-20		-55	mA
			N74180	-18		-55	mA
I_{CC}	Supply current	V_{CC}= MAX	S54180		34	49	mA
			N74180		34	56	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		25	38	ns
t_{pd1}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Even	C_L = 15pF,	R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Odd	C_L = 15pF,	R_L = 400 Ω		25	38	ns
t_{pd1}	Even or Odd	Σ Even or Σ Odd	C_L = 15pF,	R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd	C_L = 15pF,	R_L = 400 Ω		7	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

HIGH-SPEED ARITHMETIC LOGIC

S54181
N74181

S54181—N,F,Q • N74181—N,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The 54181 and 74181 are high-speed arithmetic logic units (ALU)/ function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the 54181/74181 for fast, simultaneous carry generation with a group carry propagate (P) and carry generate (G) for the 4 bits in the package. When used in conjunction with the 54182 or 74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the 54181/74181 is 24 nanoseconds for 4 bits. When expanding to 16-bit addition with the 54182/74182, only 13 nanoseconds, further delay is added so that the total addition time is 35 nanoseconds, or 2.2 nanoseconds per bit. One 54182/74182 is needed for every 16 bits (four 54181/74181 circuits).

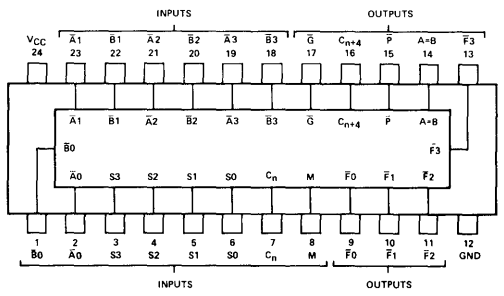
These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR and OR functions.

The 54181/74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

The 54181 is characterized for operation over the full military temperature range of -55°C to 125°C; the 74181 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

N,F,Q PACKAGE



TRUTH TABLES

TABLE OF ARITHMETIC OPERATIONS

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOW LEVELS ACTIVE	HIGH LEVELS ACTIVE
L	L	L	L	F = A minus 1	F = A
L	L	L	H	F = AB minus 1	F = A+B
L	L	H	L	F = A$\overline{B}$ minus 1	F = A+$\overline{B}$
L	L	H	H	F = minus 1 (2's complement)	F = minus 1 (2's complement)
L	H	L	L	F = A plus (A+$\overline{B}$)	F = A plus A$\overline{B}$
L	H	L	H	F = AB plus (A+$\overline{B}$)	F = (A+B) plus A$\overline{B}$
L	H	H	L	F=A minus B minus 1	F=A minus B minus 1
L	H	H	H	F = A+$\overline{B}$	F = A$\overline{B}$ minus 1
H	L	L	L	F = A plus (A+B)	F = A plus AB
H	L	L	H	F = A plus B	F = A plus B
H	L	H	L	F=A$\overline{B}$ plus (A+B)	F=(A+$\overline{B}$) plus AB
H	L	H	H	F = A+B	F = AB minus 1
H	H	L	L	F = A plus A†	F = A plus A†
H	H	L	H	F = AB plus A	F=(A+B) plus A
H	H	H	L	F = A$\overline{B}$ plus A	F=(A+$\overline{B}$) plus A
H	H	H	H	F = A	F = A minus 1

TABLE OF LOGIC FUNCTIONS

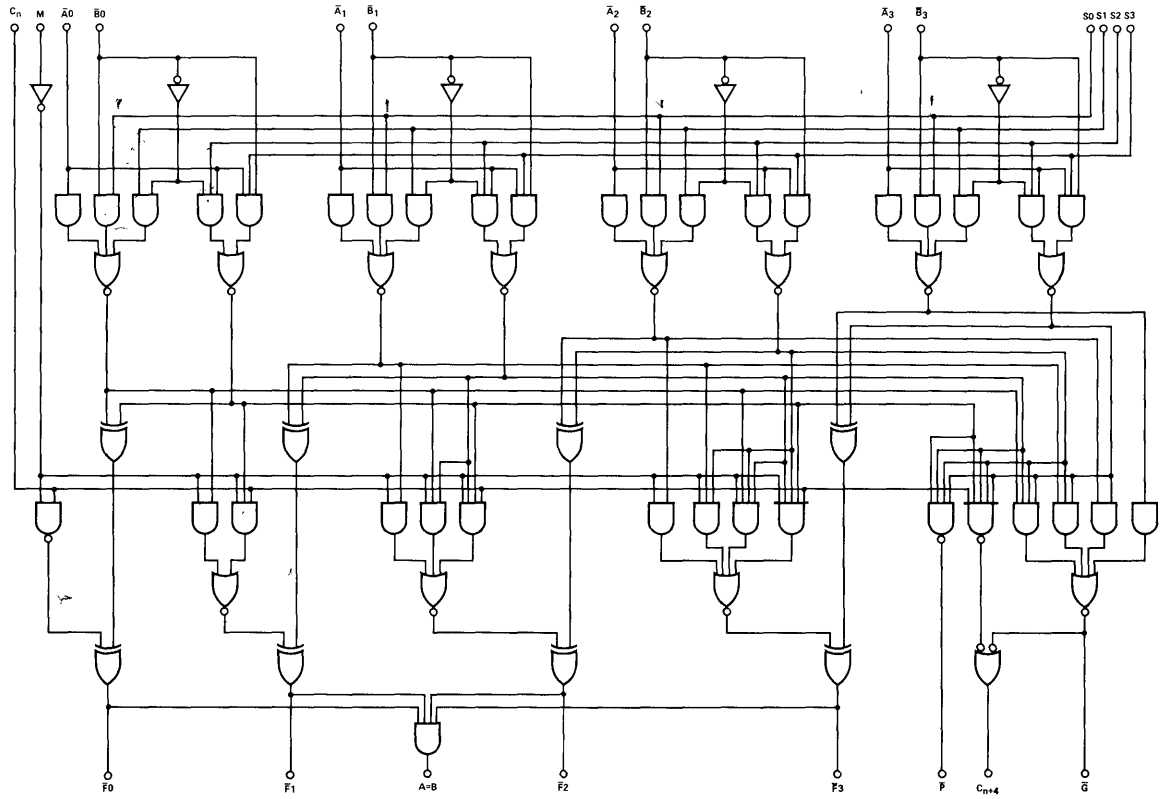
FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	NEGATIVE LOGIC	POSITIVE LOGIC
L	L	L	L	F = $\overline{A}$	F = $\overline{A}$
L	L	L	H	F = $\overline{AB}$	F = $\overline{A+B}$
L	L	H	L	F = $\overline{A}$+B	F = $\overline{A}$B
L	L	H	H	F=Logical 1	F=Logical 0
L	H	L	L	F = $\overline{A+B}$	F = $\overline{AB}$
L	H	L	H	F = $\overline{B}$	F = $\overline{B}$
L	H	H	L	F=$\overline{A + B}$	F=A + B
L	H	H	H	F = A+$\overline{B}$	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$B	F = $\overline{A}$+B
H	L	L	H	F=A + B	F=$\overline{A + B}$
H	L	H	L	F = B	F = B
H	L	H	H	F = A+B	F = AB
H	H	L	L	F= Logical 0	F=Logical 1
H	H	L	H	F = AB	F = A+$\overline{B}$
H	H	H	L	F = AB	F = A+B
H	H	H	H	F = A	F = A

Notes (See Page 158)

NOTES:
With mode control (M) and C_n low
†Each bit is shifted to the next more significant position.

With mode control (M) high: C_n irrelevant
For positive logic: logical 1 = high voltage
logical 0 = low voltage
For negative logic: logical 1 = low voltage
logical 0 = high voltage

LOGIC DIAGRAM



RECOMMENDED OPERATING CHARACTERISTICS

	S54181			N74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (mode input)						40	μA
I_{IH}	High-level input current (any $\overline{A}$ or $\overline{B}$ input)	V_{CC} = MAX,	V_I = 2.4V				120	μA
I_{IH}	High-level input current (any S input)						160	μA
I_{IH}	High-level input current (carry input)						200	μA
I_{IH}	High-level input current (any input)	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (mode input)						-1.6	mA
I_{IL}	Low-level input current (any $\overline{A}$ or $\overline{B}$ input)	V_{CC} = MAX,	V_I = 0.4V				-4.8	mA
I_{IL}	Low-level input current (any S input)						-6.4	mA
I_{IL}	Low-level input current (carry input)						-8	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		S54181	-20		-55	mA
				N74181	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX		S54181		88	127	mA
				N74181		88	140	
I_{CC}	Supply current	V_{CC} = MAX		S54181		94	135	mA
				N74181		94	150	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (C_L = 15pF, R_L = 400Ω)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			12	18	ns
t_{PHL}					13	19	
t_{PLH}	C_n	Any $\overline{F}$	M = 0V		13	19	ns
t_{PHL}			(SUM or $\overline{DIFF}$ mode)		12	18	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0V, S0 = S3 = 4.5V,		13	19	ns
t_{PHL}			S1 = S2 = 0V ($\overline{SUM}$ mode)		13	19	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0V, S0 = S3 = 0V,		17	25	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0V, S0 = S3 = 4.5V,		13	19	ns
t_{PHL}			S1 = S2 = 0V ($\overline{SUM}$ mode)		17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0V, S0 = S3 = 0V,		17	25	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0V, S0 = S3 = 4.5V,		28	42	ns
t_{PHL}			S1 = S2 = 0V ($\overline{SUM}$ mode)		21	32	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 0V, S0 = S3 = 0V,		32	48	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		23	34	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	Any $\overline{F}$	M = 4.5V (logic model)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{A} = \overline{B}$	M = 0V, S0 = S3 = 0V,		35	50	ns
t_{PHL}			S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		32	48	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

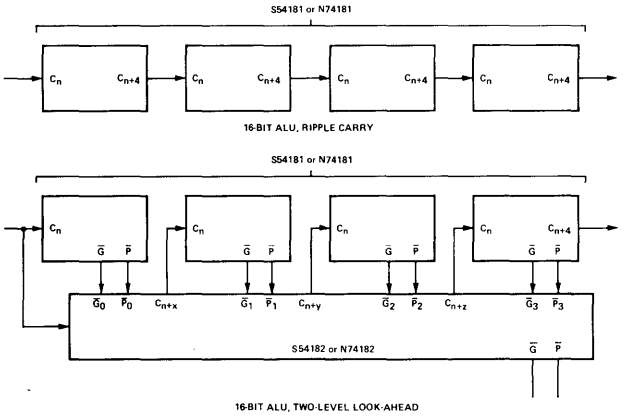
¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

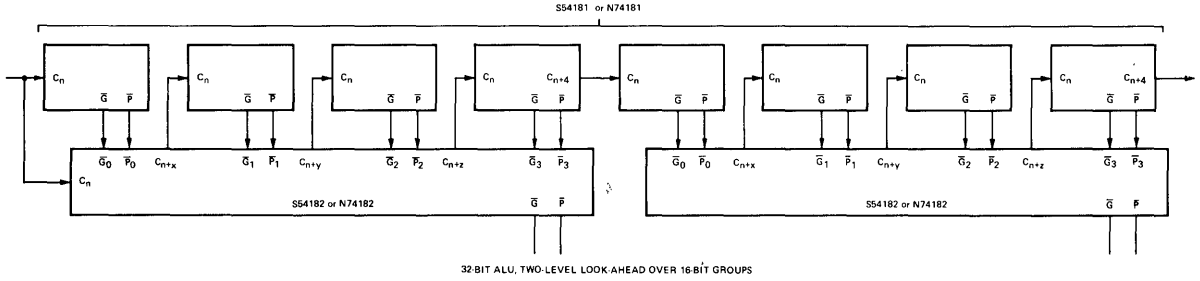
TYPICAL APPLICATION DATA

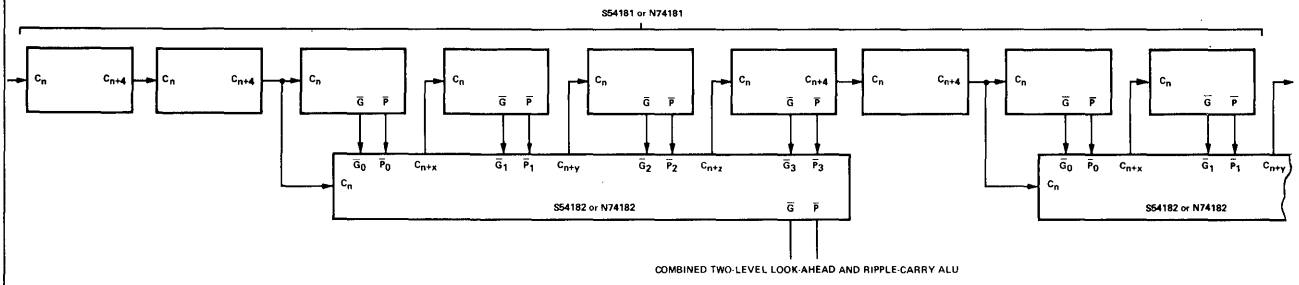
Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

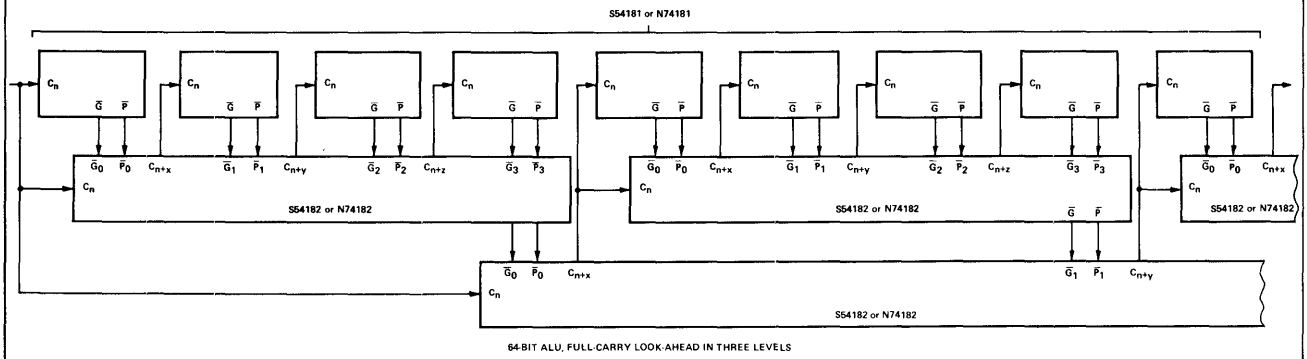
TYPICAL ADDITION TIMES

NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT	
			S54181/ N74181	S54182 N74182
4	24	6.0	1	
8	36	4.5	2	
12	48	4.0	3	
12	36	3.0	3	1
16	60	3.8	4	
16	36	2.2	4	1
32	120	3.8	8	
32	96	3.0	8	1
32	72	2.2	8	2
32	60	1.9	8	3
48	165	3.4	12	
48	148	3.1	12	1
48	132	2.7	12	2
48	108	2.2	12	3
48	60	1.25	12	4
64	220	3.5	16	
64	192	3.0	16	2
64	172	2.7	16	3
64	144	2.2	16	4
64	60	0.94	16	5









LOOK-AHEAD CARRY GENERATOR

S54182
N74182

S54182–B,F,W • N74182–B, F

DIGITAL 54/74 TTL SERIES

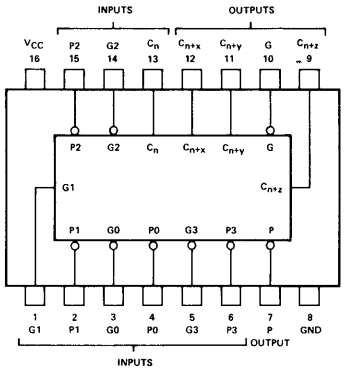
DESCRIPTION

The S54182, N74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanoseconds delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

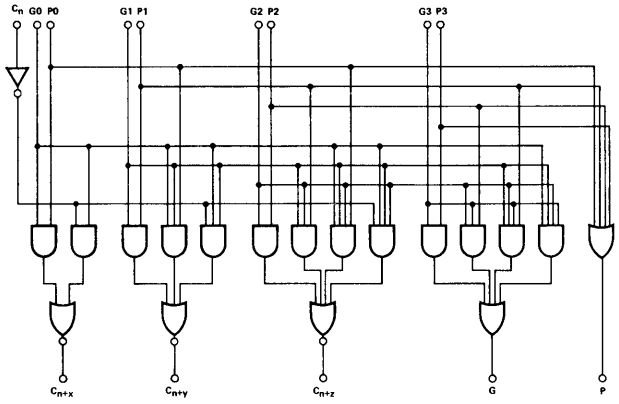
The S54182 or N74182, when used in conjunction with the S54181 or N74181 arithmetic logic unit (ALU), provides full high-speed carry look-ahead capability for up to n-bit words. Each S54182/N74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. Applications data for the S54181/N74181 illustrates cascading of S54182/N74182 circuits to perform multi-level look-ahead.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54182			N74182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_{IH}	High-level input current (C_n input)						80	μA
I_{IH}	High-level input current (P3 input)						120	μA
I_{IH}	High-level input current (P2 input)						160	μA
I_{IH}	High-level input current (P0, P1, or G3 input)	V_{CC} = MAX,	V_I = 2.4V				200	μA
I_{IH}	High-level input current (G0 or G2 input)						360	μA
I_{IH}	High-level input current (G1 input)						400	μA
I_{IH}	High-level input current (any input)	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (C_n input)						-3.2	mA
I_{IL}	Low-level input current (P3 input)						-4.8	mA
I_{IL}	Low-level input current (P2 input)						-6.4	mA
I_{IL}	Low-level input current (P0, P1, or G3 input)	V_{CC} = MAX,	V_I = 0.4V				-8	mA
I_{IL}	Low-level input current (G0 or G2 input)						-14.4	mA
I_{IL}	Low-level input current (G1 input)						-16	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX			-40		-100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX		S54182		27		mA
				N74182		27		
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX		S54182		45	65	mA
				N74182		45	72	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 400Ω		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

SYNCHRONOUS DECADE UP/DOWN COUNTER WITH PRESET INPUTS

S54192
N74192

S54192–B,F,W • N74192–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

This is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. The S54192 and N74192 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

These counters are fully programmable; that is, the outputs may be present to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

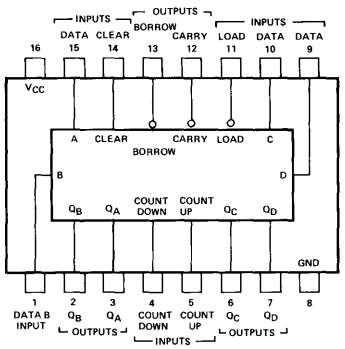
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

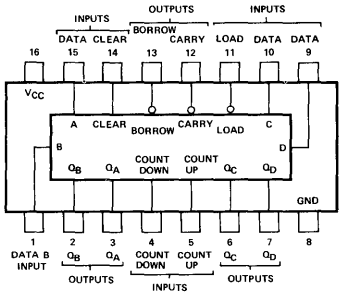
Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25MHz minimum.

PIN CONFIGURATIONS

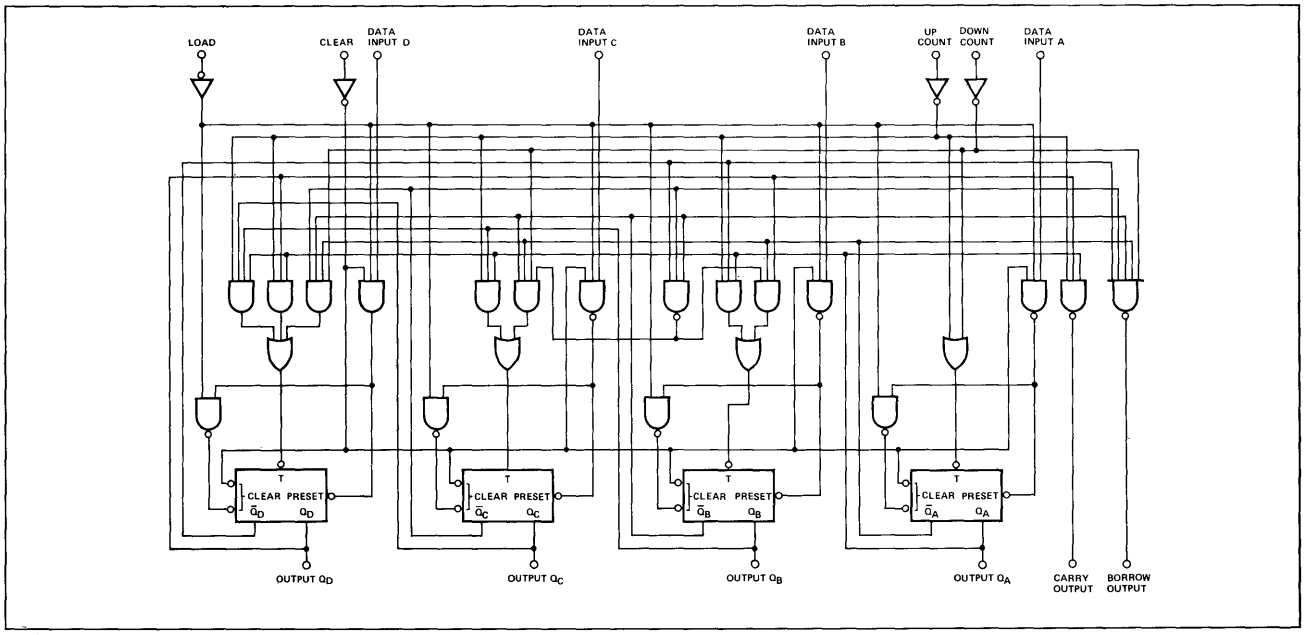
B,F PACKAGE



W PACKAGE

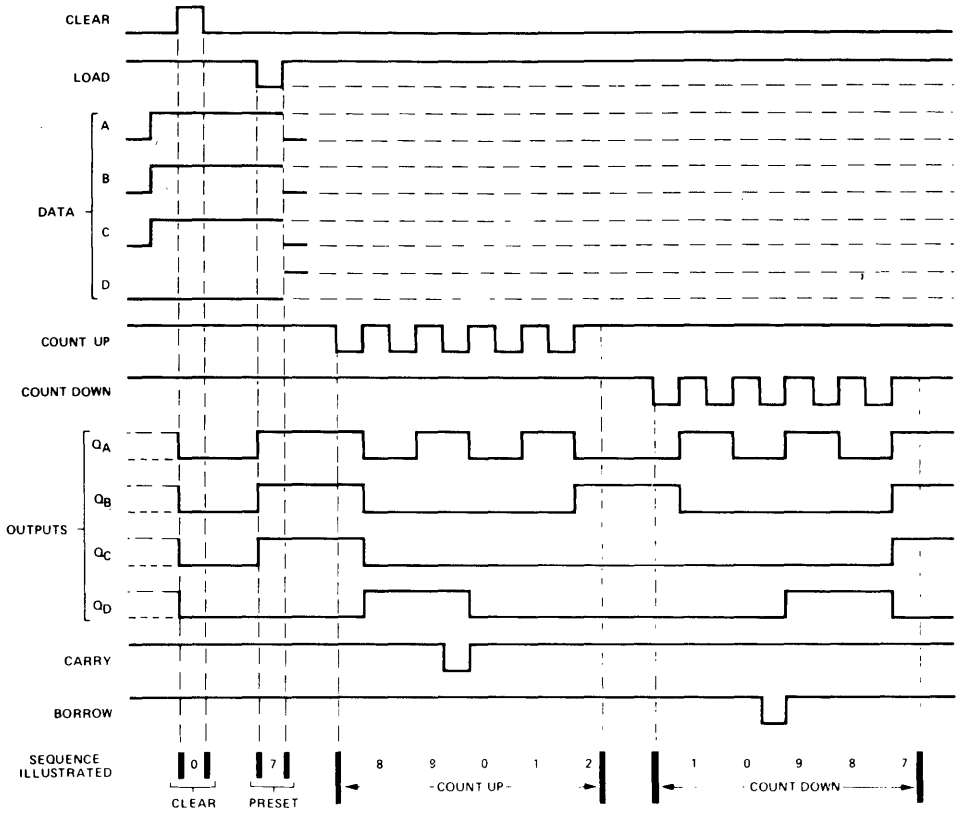


LOGIC DIAGRAM



DECADE COUNTER (typical clear, load, and count sequences)

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

RECOMMENDED OPERATING CONDITIONS

	S54192			N74192			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Input Count Frequency, f_{count}	0		25*	0		25*	MHz
Width of Any Input Pulse, t_w	20*			20*			ns
Data Setup Time, t_{setup} (See Note 2)	20*			20*			ns
Data Hold Time, t_{hold} (See Note 3)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
S54192						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	-20		-65	mA
I_{CC}	Supply current	V_{CC} = MAX		65	89	mA
N74192						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V			40	μA
		V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX	-18		-65	mA
I_{CC}	Supply current	V_{CC} = MAX		65	102	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (See Note)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency		25	32		MHz
t_{setup}	Minimum input setup time			14	20	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from count-up input			17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from count-up input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level borrow output from count-down input	C_L = 15pF, R_L = 400Ω		16	24	ns
t_{PHL}	Propagation delay time, high-to low-level borrow output from count-down input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from either count input			25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either count input			31	47	ns
t_{PLH} LOAD				27		
t_{PLH} LOAD				29	40	
t_{PHL} CLEAR				22	25	

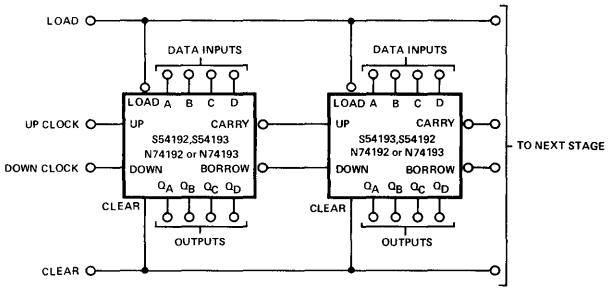
NOTE: Above Switching Table Applies to (S54192 & N74192)

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

CASCADING



Circuitry is provided internally for cascading these counters. The mode of cascading shown is ripple borrow/carry. No external components are required.

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER WITH PRESET INPUTS

S54193
N74193

S54193–B,F,W • N74193–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54193 and N74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The oututs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

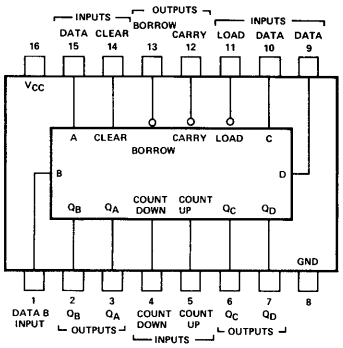
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

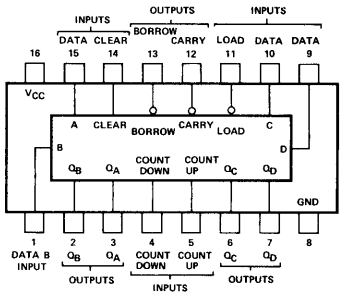
Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

PIN CONFIGURATIONS

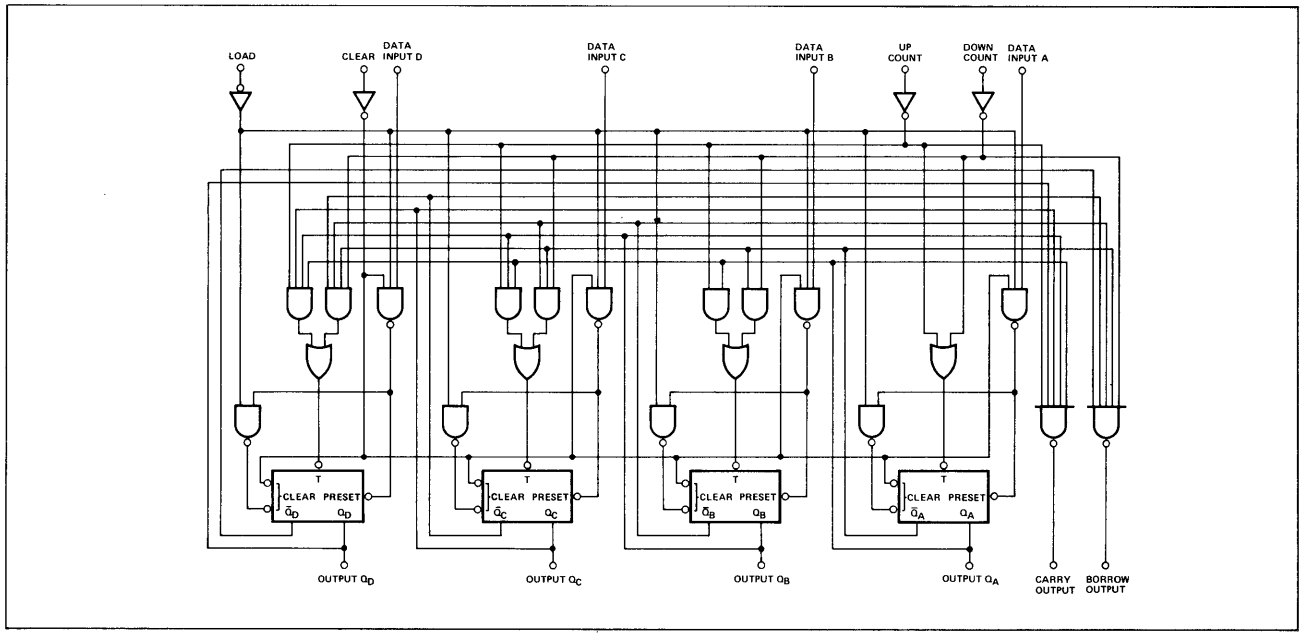
W PACKAGE



B,F PACKAGE

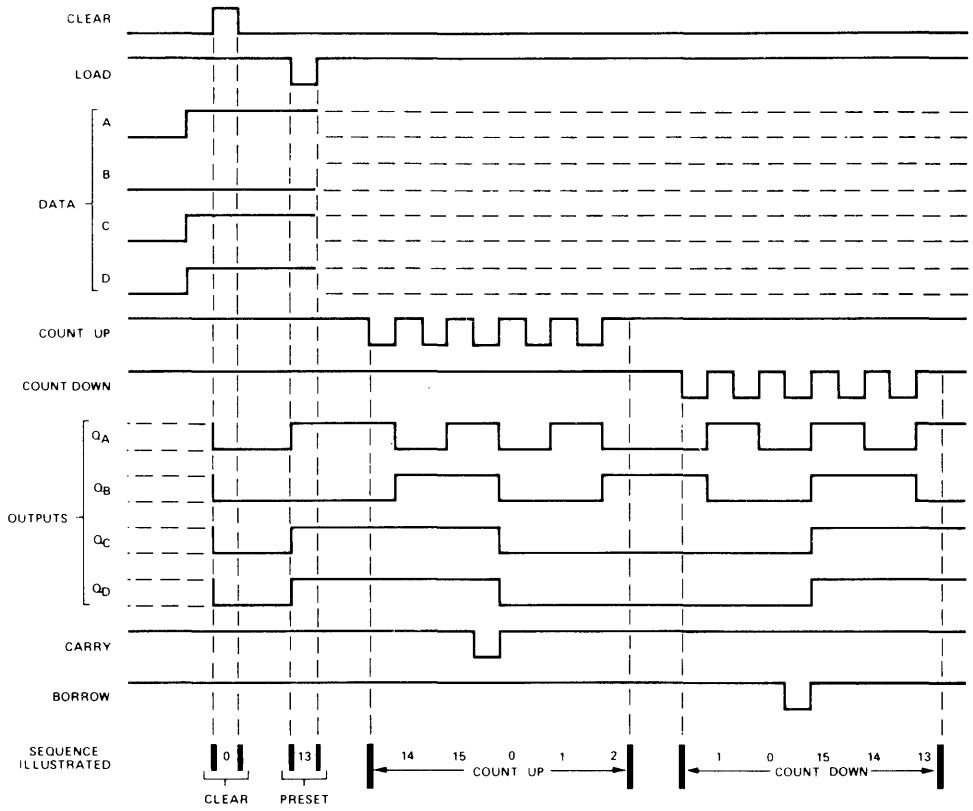


LOGIC DIAGRAM



BINARY COUNTER (typical clear, load, and count sequences)

Illustrated below is the following sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

RECOMMENDED OPERATING CONDITIONS

	S54193			N74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10			10	
Input Count Frequency, f_{count}	0		25*	0		25*	MHz
Width of Any Input Pulse, t_w	20*			20*			ns
Data Setup Time, t_{setup} (See Note 2)	20*			20*			ns
Data Hold Time, t_{hold} (See Note 3)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:
1. Voltage values are with respect to network ground terminal.
2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

*These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
S54193							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-65	mA
I_{CC}	Supply current	V_{CC} = MAX			65	89	mA
N74193							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V I_{OL} = 16mA			0.4	V
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40	μA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-18		-65	mA
I_{CC}	Supply current	V_{CC} = MAX			65	102	mA

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10 (See Note)

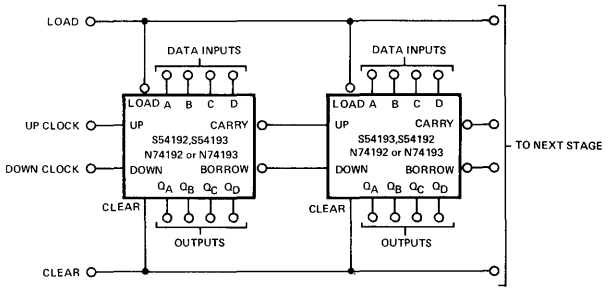
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	32		MHz
t_{setup}	Minimum input setup time			14	20	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from count-up input			17	26	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from count-up input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level borrow output from count-down input			16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level borrow output from count-down input			16	24	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from either count input			25	38	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either count input			31	47	ns
t_{PLH} LOAD				27	40	
t_{PLH} LOAD				29	40	
t_{PHL} CLEAR				22	25	

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

CASCADING



Circuitry is provided internally for cascading these counters. The mode of cascading shown is ripple borrow/carry. No external components are required.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

S54194
N74194

S54194–B,F,W • N74194–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

	MODE CONTROL S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Hold)	L	L

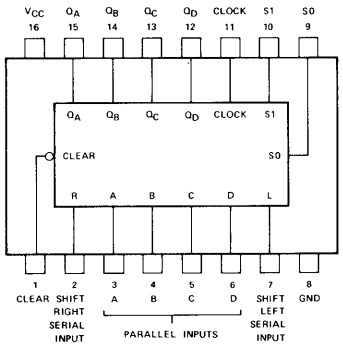
In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

These 4-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195mW.

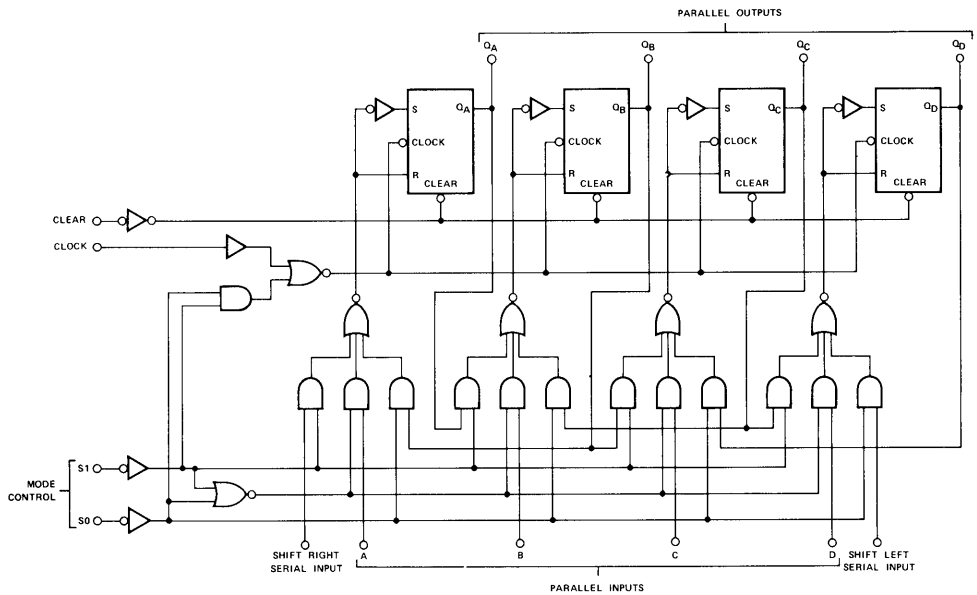
The S54194 is characterized for operation over the full military temperature range of -55°C to 125°C; the N74194 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54194			N74194			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Setup Time, t_{setup}: Mode control	30			30			ns
Serial and parallel data	20			20			ns
Clear inactive-state	25			25			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		S54194	-20		-57	mA
				N74194	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			39	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF,	R_L = 400Ω	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

4-BIT PARALLEL-ACCESS SHIFT REGISTER

S54195 N74195

S54195–B,F,W • N74195–B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

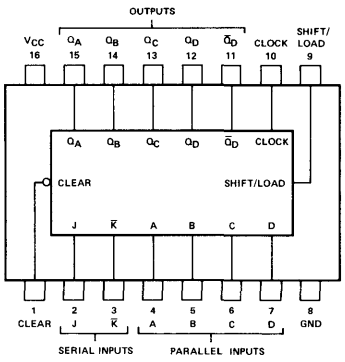
Parallel loading is accomplished by applying the 4 bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode are entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The S54195 is characterized for operation over the full military temperature range of -55° C to 125° C; the N74195 is characterized for operation from 0° C to 70° C.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	K	Q_A	Q_B	Q_C	Q_D	$\bar{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	L	$\bar{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$

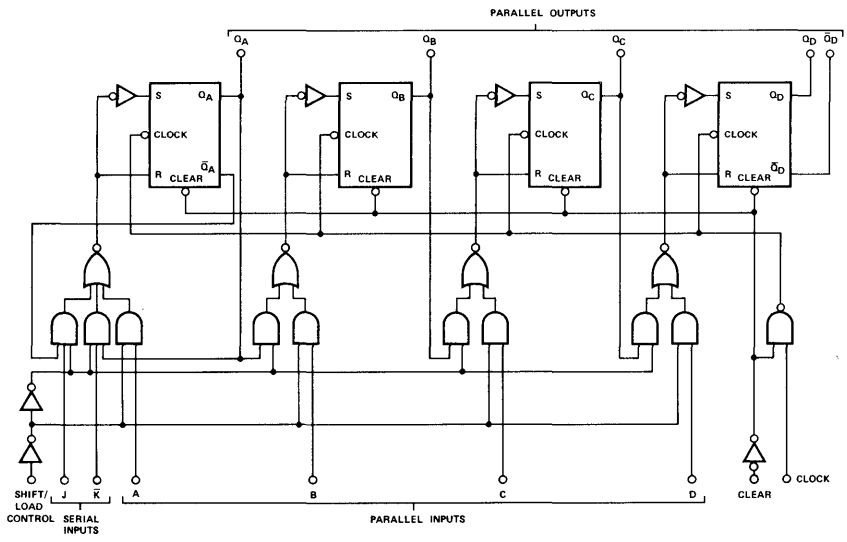
H = High Level, L = Low Level

NOTES A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

C. Q_{An} = state of Q_A at t_n

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54195			N74195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		30	0		30	MHz
Width of Clock Input Pulse, $t_{w(clock)}$	16			16			ns
Width of Clear Input Pulse, $t_{w(clear)}$	12			12			ns
Setup Time, t_{setup}: Shift/load	25			25			
Serial and parallel data	15			15			ns
Clear inactive-state	25			25			
Shift/Load Release Time, $t_{release}$			10			10	ns
Serial and Parallel Data Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -800μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		S54195	-20		-57	mA
				N74195	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note			39	63	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15pF,	R_L = 400Ω	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

NOTE With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.

8-BIT SHIFT REGISTERS

S54198
N74198

S54198—N,F,Q • N74198—F,N

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of -55°C to 125°C. Series 74 devices are characterized for operation from 0°C to 70°C.

The bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

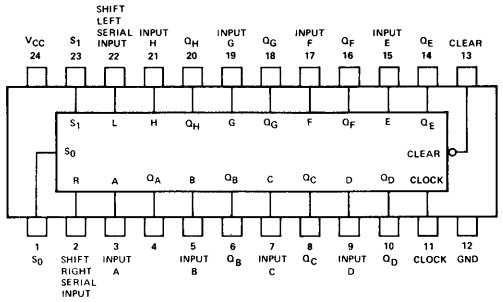
Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

Average power dissipation per gate is typically 4.15 mW.

PIN CONFIGURATIONS

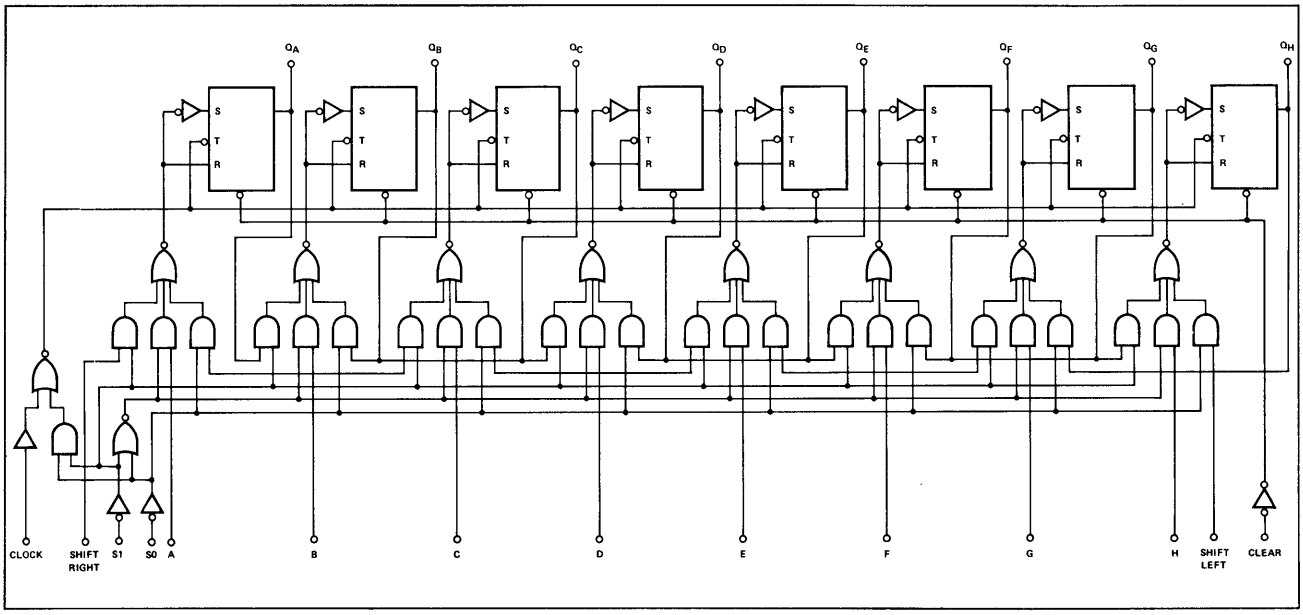
N,F,Q PACKAGE



TRUTH TABLE

OPERATION OF MODE CONTROL		
INPUTS		MODE
S_1	S_0	
L	L	INHIBIT CLOCK
H	L	SHIFT LEFT
L	H	SHIFT RIGHT
H	H	PARALLEL LOAD

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54198			N74198			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54198			N74198			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH}=-800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54198, N74198	Serial input, S_0, S_1	Clock	Clear, Inputs A thru H

8-BIT SHIFT REGISTERS

S54199
N74199

S54199–N,F,Q • N74199–N,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

These synchronous 8-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

Parallel loading is accomplished by applying the 8 bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

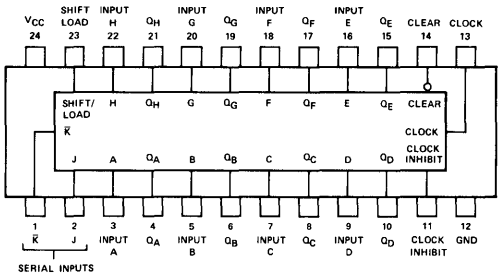
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-K inputs. See the J-K inputs truth table for states required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

PIN CONFIGURATIONS

N,F,Q PACKAGES



†Pin assignments for these circuits are the same for packages.

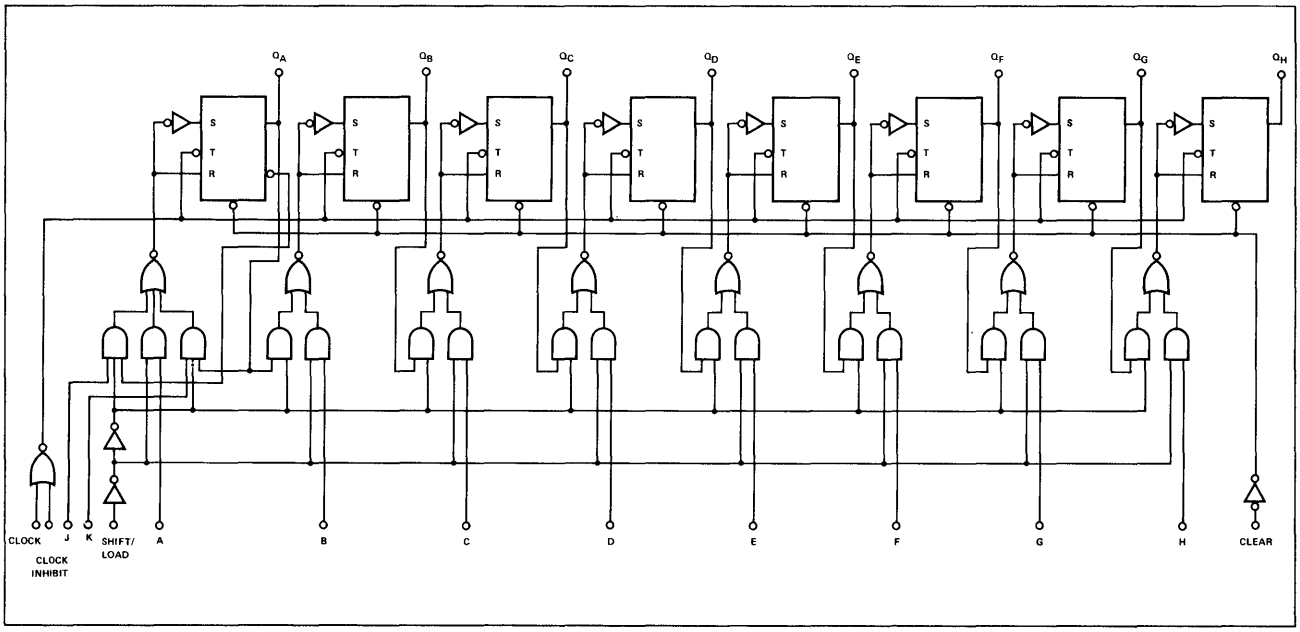
TRUTH TABLE

INPUTS at t_n		OUTPUT t_{n+1}
J	K	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

H - high level, L = low level

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54199			N74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out From each output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		S54199			N74199			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH}=-800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		-20		-57	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX,	Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54199, N74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

54H/74H
High Speed Series SSI

SECTION 3

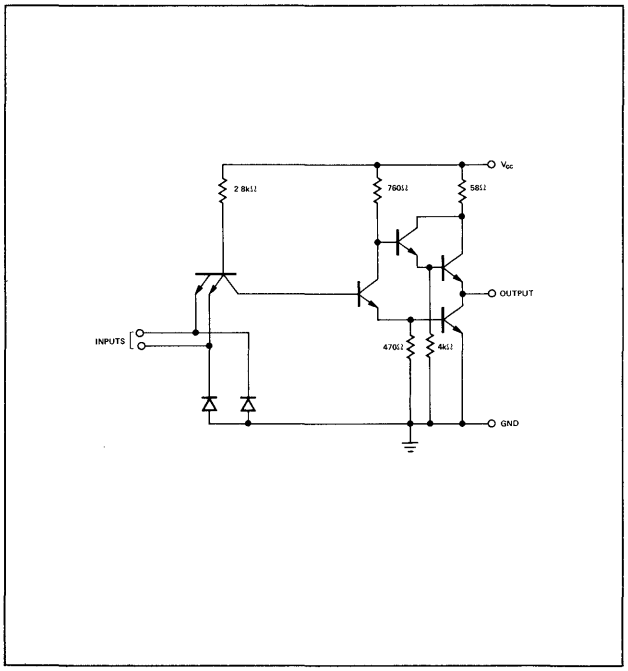
QUADRUPLE 2-INPUT POSITIVE NAND GATE

S54H00
N74H00

S54H00–A,F,W • N74H00–A,F

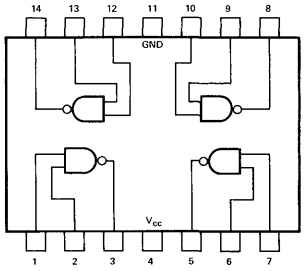
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

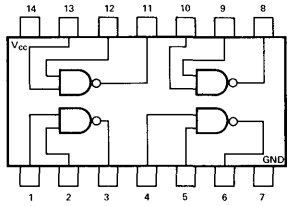


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H00 Circuits		4.5	5	5.5	V
N74H00 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H00 Circuits	-55	25	125	°C
	N74H00 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		–40		–100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		10	16.8	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		6.2	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		5.9	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

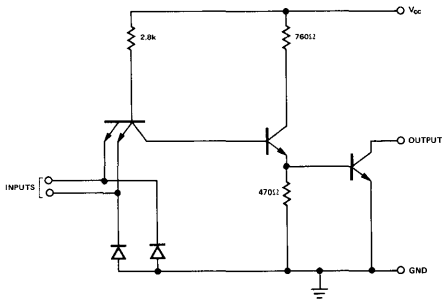
QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S54H01
N74H01

S54H01–A,F,W • N74H01–A,F

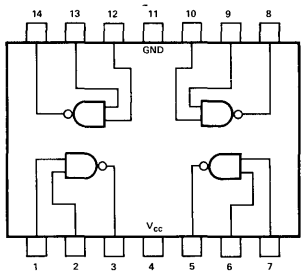
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

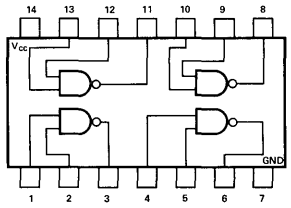


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H01 Circuits		4.5	5	5.5	V
N74H01 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H01 Circuits	-55	25	125	°C
	N74H01 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		26	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX	V_{in} = 0		6.8	10.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

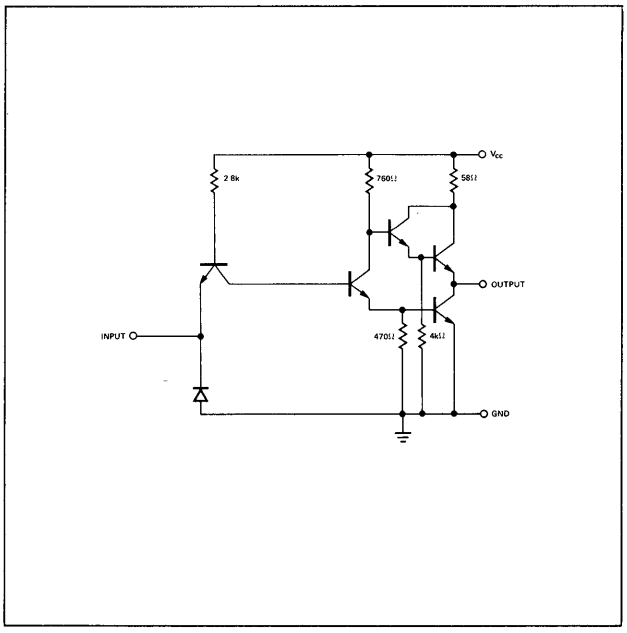
PARAMETER		TEST CONDITIONS†	MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		7.5	12.0	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		10.0	15.0	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

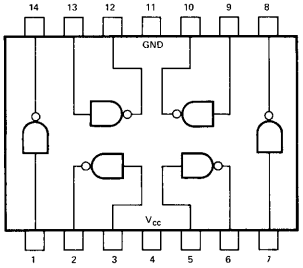
† Load resistor R_L is connected from V_{CC} to the output, and load capacitor C_L is connected from the output to ground.

SCHEMATIC (each inverter)

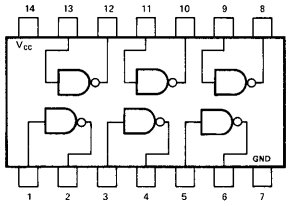


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H04 Circuits	4.5	5	5.5	V
	N74H04 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H04 Circuits	-55	25	125	°C
	N74H04 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V,		40.0	58.0	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0,		16.0	26.0	mA

SWITCHING CHARACTERISTICS, V_{cc} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		6.5	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		9.0	13.0	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{cc} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.

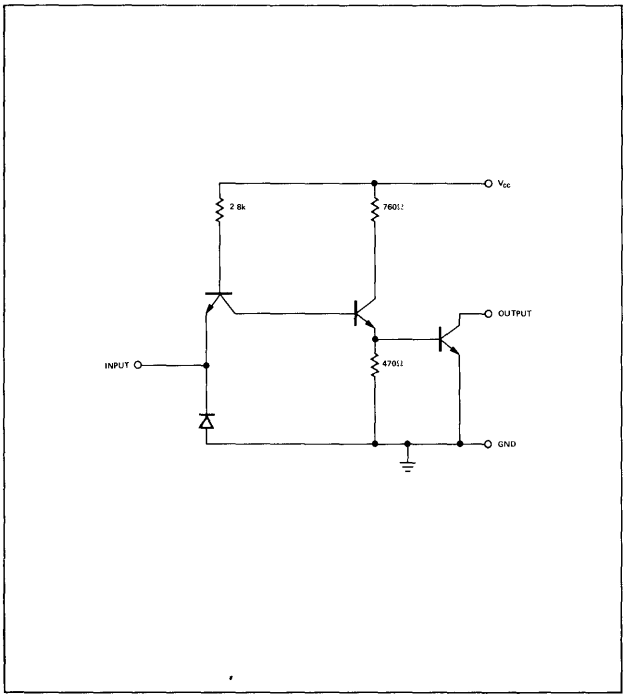
HEX INVERTER WITH OPEN COLLECTOR OUTPUT

S54H05 N74H05

S54H05–A,F,W • N74H05–A,F

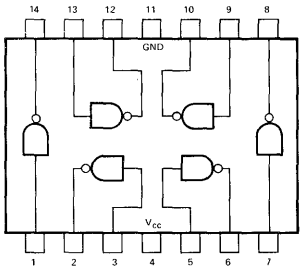
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each inverter)

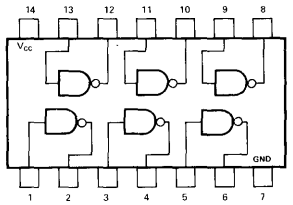


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGES



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H05 Circuits		4.5	5	5.5	V
N74H05 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H05 Circuits	-55	25	125	°C
	N74H05 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		40.0	58.0	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		16.0	26.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		10	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		13	18	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Load resistor R_L is connected from V_{CC} to the output, and load capacitor C_L is connected from the output to ground.

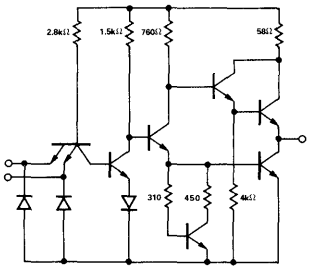
QUADRUPLE 2-INPUT POSITIVE AND GATE

S54H08
N74H08

S54H08–A,F,W • N74H08–A,F

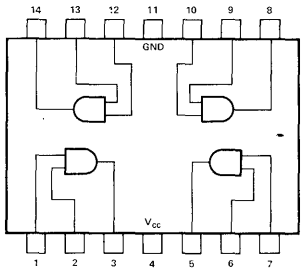
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

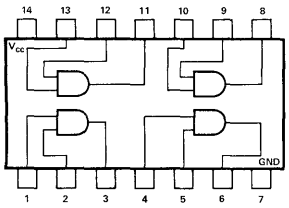


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:				
S54H08 Circuits	4.5	5	5.5	V
N74H08 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A:				
S54H08 Circuits	-55	25	125	°C
N74H08 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.4V$	2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4V$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = 500μA	V_{in} = 0.8V	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		40	64	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		24	40	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CI}	Input negative clamp voltage	V_{CC} = 5V, I_{in} = -12.0mA, T_A = 25°C			-1.5	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		7.6	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at: V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

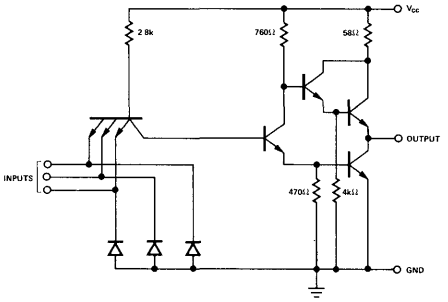
TRIPLE 3-INPUT POSITIVE NAND GATE

S54H10–A,F,W • N74H10–A,F

DIGITAL 54/74 TTL SERIES

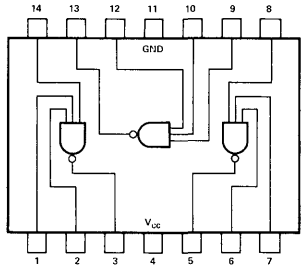
S54H10
N74H10

SCHEMATIC (each gate)

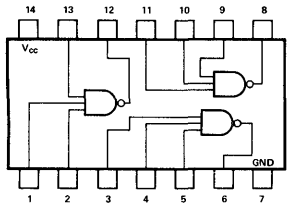


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H10 Circuits	4.5	5	5.5	V
	N74H10 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H10 Circuits	-55	25	125	°C
	N74H10 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			– 2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		–40		–100	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX, V_{in} = 4.5V		19.5	30	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX, V_{in} = 0		7.5	12.6	mA

SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		6.3	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		5.9	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

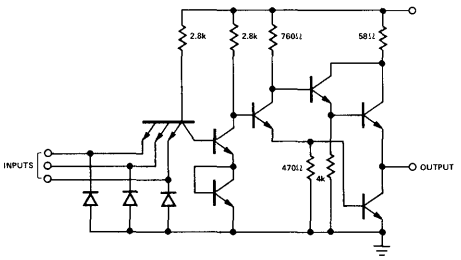
TRIPLE 3-INPUT POSITIVE AND GATE

S54H11
N74H11

S54H11–A,F,W • N74H11–A,F

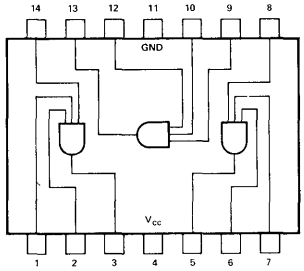
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

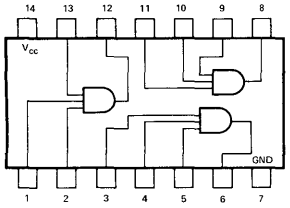


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H11 Circuits		4.5	5	5.5	V
N74H11 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H11 Circuits	-55	25	125	°C
	N74H11 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 0 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –500μA	$V_{in(1)}$ = 2V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	$V_{in(0)}$ = 0.8V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 4.5V	–40		–100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		30	48	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		18	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		8.8	12	ns
t_{pd1}	Propagation delay time	C_L = 25pF, R_L = 280Ω		7.6	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

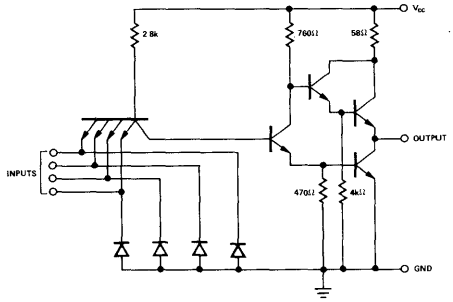
DUAL 4-INPUT POSITIVE NAND GATE

S54H20
N74H20

S54H20–A,F,W • N74H20–A,F

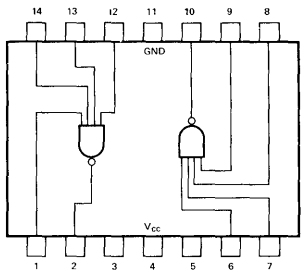
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

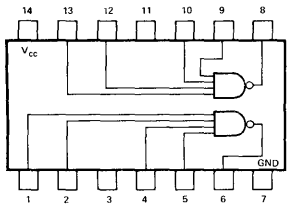


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H20 Circuits	4.5	5	5.5	V
	N74H20 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H20 Circuits	-55	25	125	°C
	N74H20 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		5	8.4	mA

SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		7	10	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		6	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

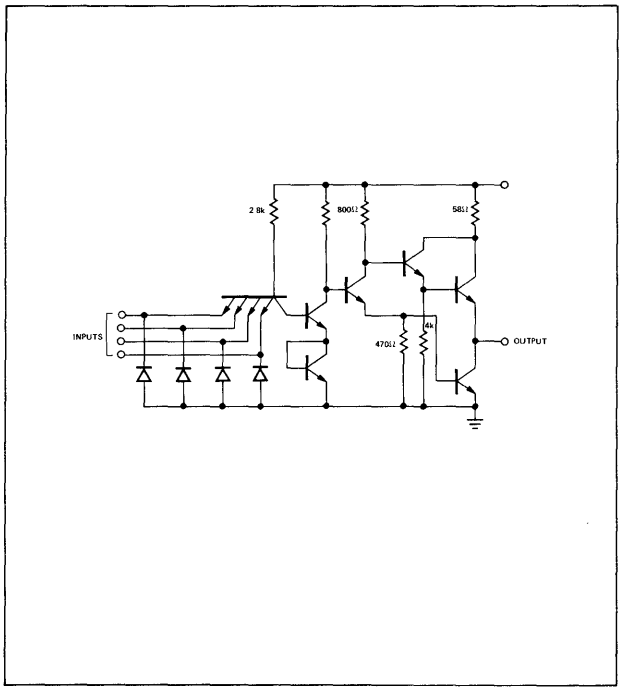
DUAL 4-INPUT POSITIVE AND GATE

S54H21
N74H21

S54H21–A,F,W • N74H21–A,F

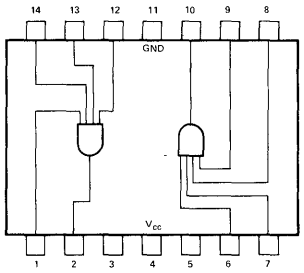
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

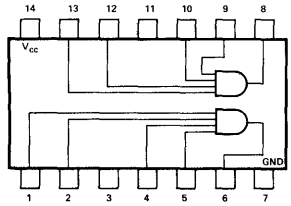


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H21 Circuits		4.5	5	5.5	V
N74H21 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H21 Circuits	-55	25	125	°C
	N74H21 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 0 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –500μA	$V_{in(1)}$ = 2V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	$V_{in(0)}$ = 0.8V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,	V_{in} = 4.5V	-40		–100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		20	32	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		12	20	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		8.8	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		7.6	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

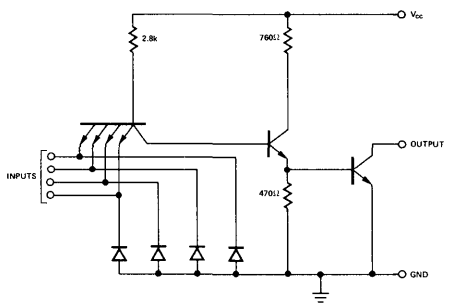
DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

S54H22
N74H22

S54H22–A,F,W • N74H22–A,F

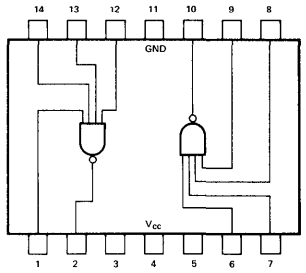
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

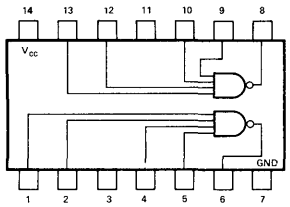


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H22 Circuits	4.5	5	5.5	V
N74H22 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range: S54H22 Circuits	-55	25	125	°C
N74H22 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical $0_{(on)}$ level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical $1_{(off)}$ level at output	V_{CC} = MIN,				0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, $V_{out(1)}$ = 5.5V	V_{in} = 0.8V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		13	20	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		3.4	5.0	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS†	MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		7.5	12.0	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		10.0	15.0	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time and duration of short circuit test should not exceed 1 second.

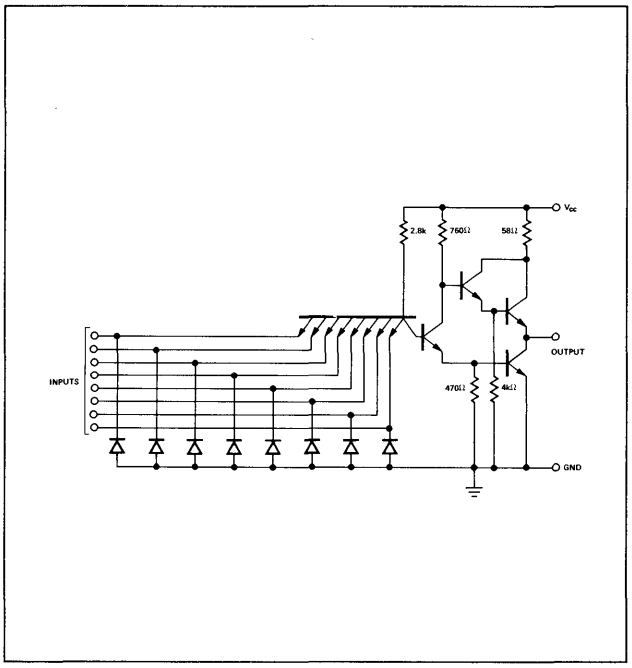
8-INPUT POSITIVE NAND GATE

S54H30
N74H30

S54H30–A,F,W • N74H30A,F,W

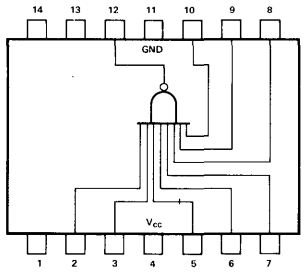
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

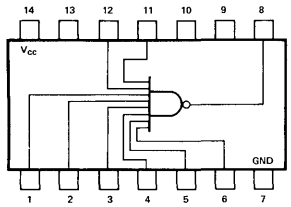


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H30 Circuits	4.5	5	5.5	V
	N74H30 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H30 Circuits	–55	25	125	°C
	N74H30 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required of any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = –500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX		–40		–100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		6.5	10	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		2.5	4.2	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP**	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 280Ω		8.9	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 280Ω		6.8	10	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values at: V_{CC} = 5V, T_A = 25°C.

† Duration of short circuit test should not exceed 1 second.

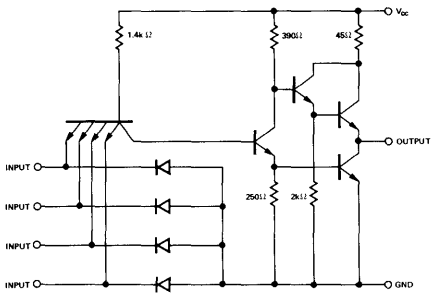
DUAL 4-INPUT POSITIVE NAND BUFFER

S54H40
N74H40

S54H40–A,F,W • N74H40–A,F

DIGITAL 54/74 TTL SERIES

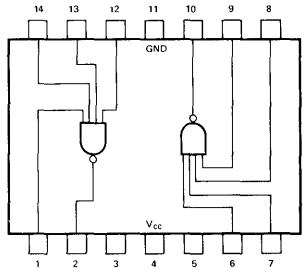
SCHEMATIC (each gate)



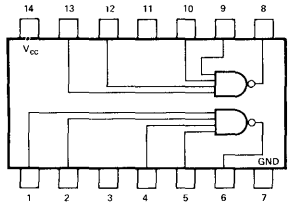
NOTES:
1. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H40 Circuits	4.5	5	5.5	V
	N74H40 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				30	
Operating Free-Air Temperature Range, T_A:	S54H40 Circuits	-55	25	125	°C
	N74H40 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -1.5mA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 60mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-4	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			100 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX		-40		-125	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		25	40	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		10.4	16	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF, R_L = 93Ω		6.5	12	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF, R_L = 93Ω		8.5	12	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

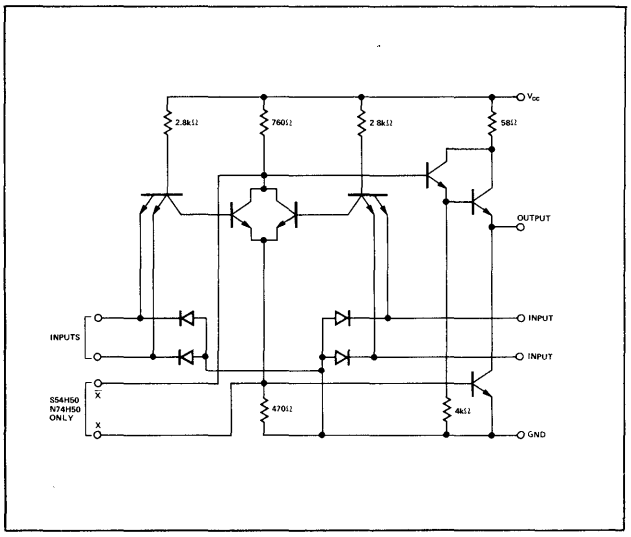
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

S54H50 S54H51 N74H50 N74H51

S54H50–A,F,W • S54H51–A,F,W • N74H50–A,F • N74H51–A,F

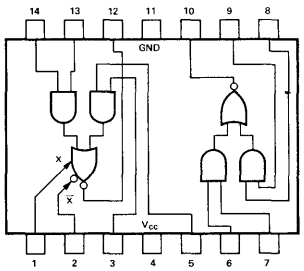
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)

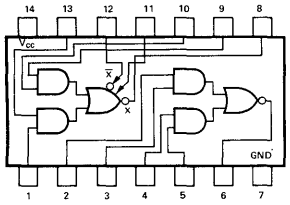


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:
1. Component values are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the S54H50 and N74H50 circuits only. Make no external connection to X and $\overline{X}$ pins of the S54H51 and N74H51.
5. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H50, S54H51 Circuits	4.5	5	5.5	V
N74H50, N74H51 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	
Operating Free-Air Temperature Range, T_A: S54H50, S54H51 Circuits	-55	25	125	°C
N74H50, N74H51 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{OS}	Short circuit output current**	V_{CC} = MAX			-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V			15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0			8.2	12.8	mA

ELECTRICAL CHARACTERISTICS (S54H50 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 700μA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -320μA	I_1 = 320μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 470μA,	R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H50 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = 0°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 1.1mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -570μA	I_1 = 570μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 600μA,	R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		6.8	11	ns

SWITCHING CHARACTERISTICS, (S54H50/N74H50 circuits only), V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15 pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		11		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

4-WIDE 2-2-2-3-INPUT AND-OR GATE

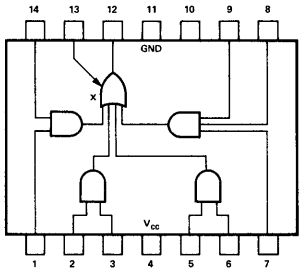
S54H52
N74H52

S54H52–A,F,W • N74H52–A,F

DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS

W PACKAGE



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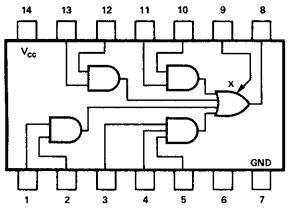
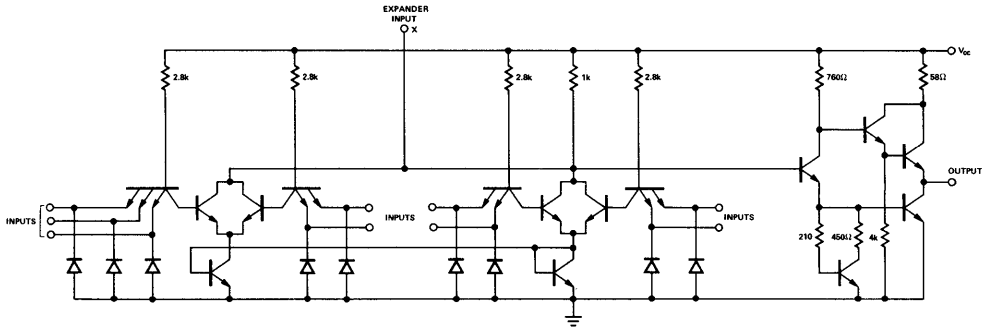


SCHEMATIC DIAGRAM



NOTE:

1. A total of six expander gates may be connected to the expander input.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H52 Circuits		4.5	5	5.5	V
N74H52 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H52 Circuits	-55	25	125	°C
	N74H52 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*	MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 1 at output	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 0 at output	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, V_{in} = 2V, I_{load} = –500μA	2.4			V

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 0.8V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 4.5V	-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 0		15.2	24	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		20	31	mA

ELECTRICAL CHARACTERISTICS (S54H52 circuits only) using expander input, V_{CC} = 4.5V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	V_X = 1V, T_A = -55°C	I_{load} = -500μA,	-2.7		-4.5	mA
$V_{out(1)}$	Logical 1 output voltage	V_X = 1V, T_A = -55°C	I_{load} = -500μA,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{inX} = -300μA, T_A = 125°C	I_{sink} = 20mA,			0.4	V

ELECTRICAL CHARACTERISTICS (N74H52 circuits only) using expander input, V_{CC} = 4.75V

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{inX}	Expander-node input current	V_X = 1V,	I_{load} = -500μA,	T_A = 0°C	-2.9		-5.35	mA
$V_{out(1)}$	Logical 1 output voltage	V_X = 1V,	I_{load} = -500μA,	T_A = 0°C	2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{inX} = -300μA,	I_{sink} = 20mA,	T_A = 70°C			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pin is open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		9.2	15	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		10.6	15	ns

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		9.8		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		14.8		ns

* For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions for the applicable device type. Expander pin is open.

** Duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

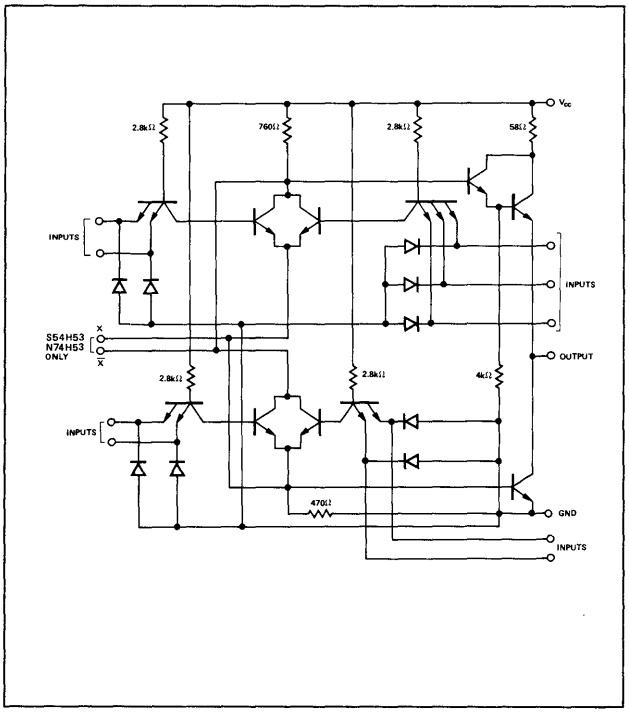
EXPANDABLE 2-2-2-3-INPUT AND-OR-INVERT GATE

S54H53–A,F,W • S54H54–A,F,W • N74H53–A,F • N74H54–A,F

DIGITAL 54/74 TTL SERIES

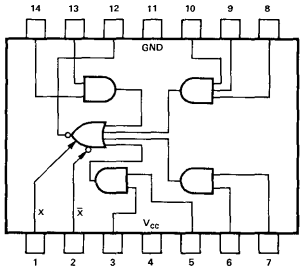
S54H53
S54H54
N74H53
N74H54

SCHEMATIC DIAGRAM

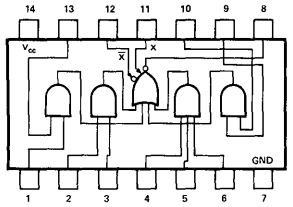


PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



NOTES:

1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used leave X and $\overline{X}$ pins open.
4. Expander inputs X and $\overline{X}$ are functional on the S54H53 and N74H53 circuits only. Make no external connection to X and $\overline{X}$ pins of the S54H54 and N74H54.
5. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H53, S54H54 Circuits	4.5	5	5.5	V
	N74H53, N74H54 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H53, S54H54 Circuits	-55	25	125	°C
	N74H53, N74H54 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	V_{CC} = MIN,		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current **	V_{CC} = MAX		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		9.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		7.1	11	mA

ELECTRICAL CHARACTERISTICS (S54H53 circuits only) using expander inputs, V_{CC}= 4.5V, T_A = -55°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 700μA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -320μA	I_1 = 320μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA	I_1 = 470μA,	R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H53 circuits only) using expander inputs, V_{CC}= 4.75V, T_A = 0°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					-6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 1.1mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = -500μA, I_2 = -570μA	I_1 = 570μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 600μA,	R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.2	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		7	11	ns

SWITCHING CHARACTERISTICS, (S54H53/N74H53 circuits only) V_{CC}= 5V, T_A = 25°C, N = 10, C_X = 15 pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.4		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		11.4		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

** Duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC}= 5V, T_A = 25°C.

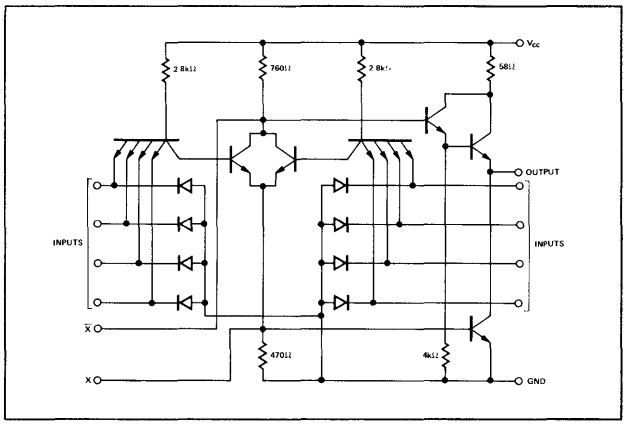
EXPANDABLE 4-INPUT AND-OR-INVERT GATES

S54H55 N74H55

S54H55–A,F,W • N74H55–A,F

DIGITAL 54/74 TTL SERIES

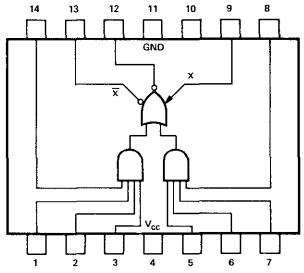
SCHEMATIC DIAGRAM



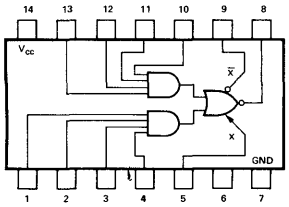
NOTES:
1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding.
3. If expander is not used, leave X and X pins open.
4. A total of four S54H60/N74H60 expander gates or one S54H62/N74H62 expander gate may be connected to the expander inputs.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H55 Circuits		4.5	5	5.5	V
N74H55 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S54H55 Circuits	-55	25	125	°C
	N74H55 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -500μA	V_{in} = 0.8V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 20mA	V_{in} = 2V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,		-40		-100	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX,	V_{in} = 4.5V		7.5	12	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX,	V_{in} = 0		4.5	6.4	mA

ELECTRICAL CHARACTERISTICS (S54H55 circuits only) using expander inputs, V_{CC} = 4.5V, T_A = −55°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					−5.85	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 700μA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = −500μA, I_2 = −320μA	I_1 = 320μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 470μA,	R_1 = 68Ω			0.4	V

ELECTRICAL CHARACTERISTICS (N74H55 circuits only) using expander inputs, V_{CC} = 4.75V, T_A = 0°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{in\overline{X}}$	Expander-node input current	$V_{\overline{X}}$ = 1.4V					−6.3	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor Q	I_{sink} = 20mA,	I_1 = 1.1mA,	R_1 = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	I_{load} = −500μA I_2 = −570μA	I_1 = 570μA,		2.4			V
$V_{out(0)}$	Logical 0 output voltage	I_{sink} = 20mA,	I_1 = 600μA,	R_1 = 63Ω			0.4	V

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, expander pins are open

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		6.5	11	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		7	11	ns

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10, C_X = 15pF

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 25pF,	R_L = 280Ω		7.7		ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 25pF,	R_L = 280Ω		11.4		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander pins are open.

** Duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

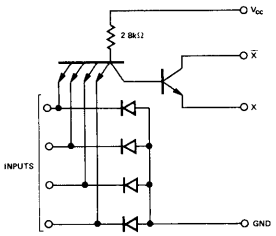
DUAL 4-INPUT EXPANDER (FOR USE WITH S54H50, S54H53, S54H55 CIRCUITS)

S54H60

S54H60–A,F,W

DIGITAL 54/74 TTL SERIES

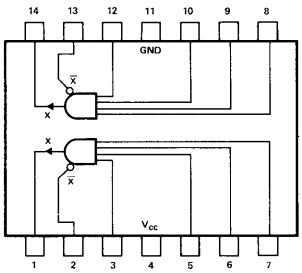
SCHEMATIC (each expander)



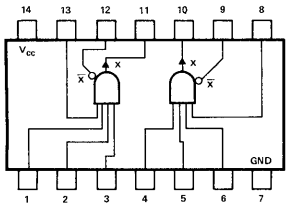
NOTES:
1. Connect to X input of S54H50, S54H53, or S54H55 circuit.
2. Connect to $\overline{X}$ input of S54H50, S54H53, or S54H55 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S54H50, S54H53, or S54H55 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.5V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, I_{on} = 5.85mA,	V_{in} = 2V, T_A = –55°	V_1 = 1V,			0.4	V
		V_{CC} = 5.5V I_{on} = 7.85mA,	V_{in} = 2V, T_A = 125°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 575Ω,	V_{in} = 0.8V, T_A = –55°C	V_1 = 4.5V,			320	μA
I_{on}	On-state output current	V_{CC}= 4.5V, T_A = –55°C	V_{in} = 2V,	V_1 = 1V,	–470			μA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V	V_{in} = 0.4V				–2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 2.4V				50	μA
		V_{CC} = 5.5V,	V_{in} = 5.5V				1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 4.5V,			1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC}= 5.5V, V_1 = 0.85V	V_{in} = 0,			3	4.5	mA

† All typical values are at V_{CC} = 5V, T_A = 25°C.

OUTPUT CAPACITANCE V_{CC} and GND terminals open, T_A = 25°C.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_X	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

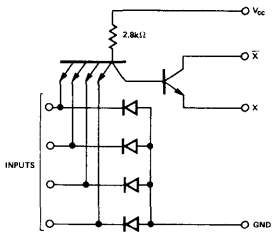
DUAL 4-INPUT EXPANDER (FOR USE WITH N74H50, N74H53, N74H55 CIRCUITS)

N74H60

N74H60–A,F

DIGITAL 54/74 TTL SERIES

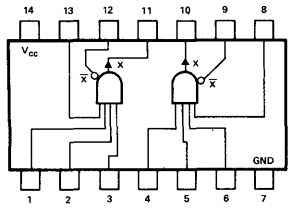
SCHEMATIC (each expander)



NOTES:
1. Connect to X input of N74H50, N74H53, or N74H55 circuit.
2. Connect to $\overline{X}$ input of N74H50, N74H53, or N74H55 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.75V to 5.25V
Maximum number of expanders that may be fanned-in to one N74H50, N74H53, or N74H55 circuit	4

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.75V			2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = 4.75V					0.8	V
V_{OS}	On-state output voltage	V_{CC} = 4.75V, I_{on} = 6.3mA,	V_{in} = 2V, T_A = 0°C	V_1 = 1V,			0.4	V
		V_{CC} = 5.25V, I_{on} = 7.4mA,	V_{in} = 2V, T_A = 70°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.75V, R = 575Ω	V_{in} = 0.8V, T_A = 0°C	V_1 = 4.5V,			570	μA
I_{on}	On-state output current	V_{CC} = 4.75V, T_A = 0°C	V_{in} = 2V,	V_1 = 1V,	-600			μA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 0.4V				-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.25V,	V_{in} = 2.4V				50	μA
		V_{CC} = 5.25V,	V_{in} = 5.5V				1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.25V, V_1 = 0.85V	V_{in} = 4.5V,			1.9	3.5	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.25V, V_1 = 0.85V	V_{in} = 0,			3	4.5	mA

OUTPUT CAPACITANCE V_{CC} and GND terminals open, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

† All typical values are at $V_{CC} = 5V$, $T_A = 25°C$

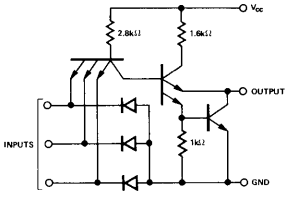
TRIPLE 3-INPUT EXPANDER (FOR USE WITH S54H52, N74H52 CIRCUITS)

S54H61
N74H61

S54H61—A,F,W • N74H61—A,F

DIGITAL 54/74 TTL SERIES

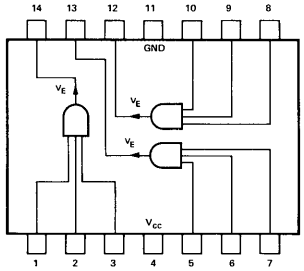
SCHEMATIC (each expander)



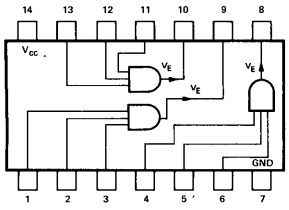
NOTES:
1. Component values shown are nominal.
2. A total of six expander gates may be connected to the S54H52/N74H52 expander input.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H61 Circuits	4.5	5	5.5	V
	N74H61 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H61 Circuits	-55	25	125	°C
	N74H61 Circuits	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output is in the off state	V_{CC} = MIN				0.8	V
I_{off}	Off-state reverse current	V_{CC} = MIN, V_{off} = 2.2V,	$V_{in(0)}$ = 0.8V, T_A = MAX			50	μA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = MAX,	V_{in} = 4.5V		7.2	12	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = MAX,	V_{in} = 0		3	5	mA

ELECTRICAL CHARACTERISTICS S54H61 circuits only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.5V	2			V
V_{on}	On-state output voltage	V_{CC} = 4.5V, $V_{in(1)}$ = 2V, I_{on} = 4.5mA, T_A = −55°C			1	V

ELECTRICAL CHARACTERISTICS N74H61 circuits only

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output is in the on state	V_{CC} = 4.75V	2			V
V_{on}	On-state output voltage	V_{CC} = 4.75V, $V_{in(1)}$ = 2V, I_{on} = 5.35mA, T_A = 0°C			1	V

OUTPUT CAPACITANCE, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

† All typical values are at V_{CC} = 5V, T_A = 25°C

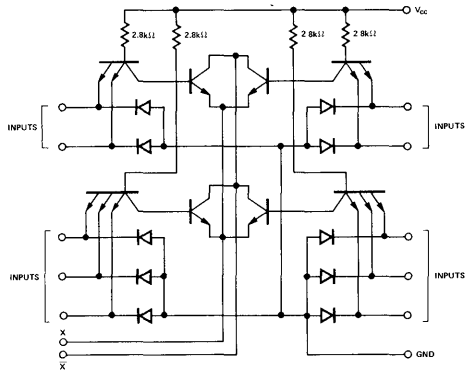
3-2-2-3-INPUT AND-OR EXPANDER (FOR USE WITH S54H50, S54H53, S54H55 CIRCUITS)

S54H62

S54H62–A,F,W

DIGITAL 54/74 TTL SERIES

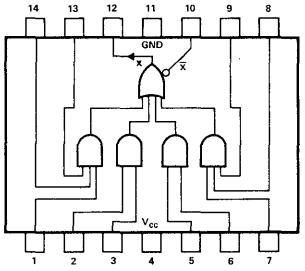
SCHEMATIC (each gate)



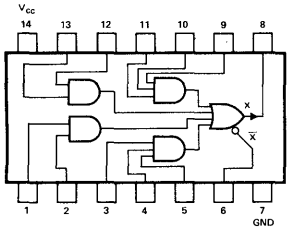
NOTES:
1. Connect to X input of S54H50, S54H53, or S54H55 circuit
2. Connect to $\overline{X}$ input of S54H50, S54H53, or S54H55 circuit
3. Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.5V to 5.5V
Maximum number of expanders that may be fanned-in to one S54H50, S54H53, or S54H55 circuit	1

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = -55°C to 125°C)

	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	V_{CC} = 4.5V			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	V_{CC} = 4.5V,					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.5V, I_{on} = 5.85mA,	V_{in} = 2V, T_A = -55°C	V_1 = 1V,			0.4	V
		V_{CC} = 5.5V, I_{on} = 7.85mA,	V_{in} = 2V, T_A = 125°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.5V, R = 575Ω,	V_{in} = 0.8V, T_A = -55°C	V_1 = 4.5V,			320	μA
I_{on}	On-state output current	V_{CC} = 4.5V, T_A = -55°C	V_{in} = 2V,	V_1 = 1V,	-470			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.5V,	V_{in} = 2.4V			50	μA
		V_{CC} = 5.5V,	V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 4.5V,		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.5V, V_1 = 0.85V	V_{in} = 0,		6	9	mA

OUTPUT CAPACITANCE, V_{CC} and GND terminals open, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capaitance of output transistor Q_1	f = 1 MHz		1.3		pF

†All typical values are at V_{CC} = 5V, T_A = 25°C.

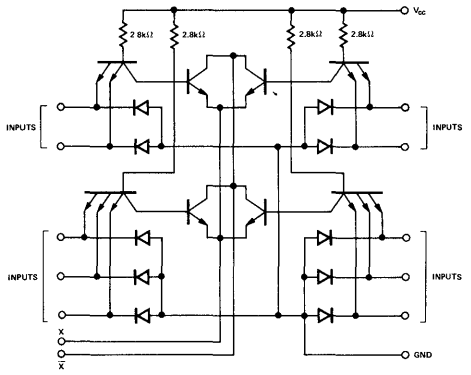
3-2-2-3-INPUT AND-OR EXPANDER (FOR USE WITH N74H50, N74H53, N74H55 CIRCUITS)

N74H62

N74H62–A,F

DIGITAL 54/74 TTL SERIES

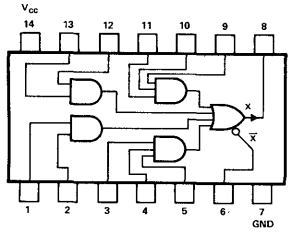
SCHEMATIC (each gate)



NOTES:
1. Connect to X input of N74H50, N74H53, or N74H55 circuit.
2. Connect to $\overline{X}$ input of N74H50, N74H53, or N74H55 circuit.
3. Component values shown are nominal.

PIN CONFIGURATIONS

A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	4.75V to 5.25V
Maximum number of expanders that may be fanned-in to one N74H50, N74H53, or N74H55 circuit	1

ELECTRICAL CHARACTERISTICS (unless otherwise noted T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of one AND section to ensure output is in the on state	V_{CC} = 4.75V			2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure output is in the off state	V_{CC} = 4.75V					0.8	V
V_{on}	On-state output voltage	V_{CC} = 4.75V, I_{on} = 6.3mA,	V_{in} = 2V, T_A = 0°C	V_1 = 1V,			0.4	V
		V_{CC} = 5.25V, I_{on} = 7.4mA,	V_{in} = 2V, T_A = 70°C	V_1 = 0.6V,			0.4	V
I_{off}	Off-state output current	V_{CC} = 4.75V, R = 575Ω,	V_{in} = 0.8V T_A = 0°C	V_1 = 4.5V,			570	μA
I_{on}	On-state output current	V_{CC} = 4.75V, T_A = 0°C	V_{in} = 2V,	V_1 = 1V,	–600			μA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = 5.25V, V_{in} = 0.4V			-2	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = 5.25V, V_{in} = 2.4V			50	μA
		V_{CC} = 5.25V, V_{in} = 5.5V			1	mA
$I_{CC(on)}$	On-state supply current	V_{CC} = 5.25V, V_{in} = 4.5V, V_1 = 0.85V		3.8	7	mA
$I_{CC(off)}$	Off-state supply current	V_{CC} = 5.25V, V_{in} = 0, V_1 = 0.85V		6	9	mA

OUTPUT CAPACITANCE V_{cc} **and GND terminals open,** T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Cx	Effective capacitance of output transistor Q_1	f = 1 MHz		1.3		pF

†All typical values are at V_{CC} = 5V, T_A = 25°C.

J-K MASTER-SLAVE FLIP-FLOP

S54H71
N74H71

S54H71–A,F,W • N74H71–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND-OR gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

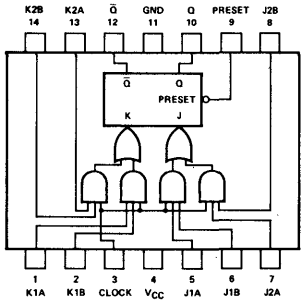
TRUTH TABLE

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

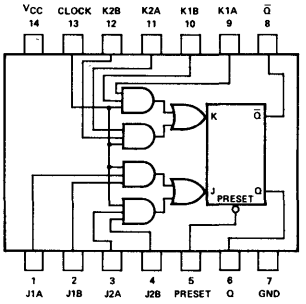
NOTES:
1. J = (J1A • J1B) + (J2A • J2B)
2. K = (K1A • K1B) + (K2A • K2B)
3. t_n = Bit time before clock pulse.
4. t_n+1 = Bit time after clock pulse.

PIN CONFIGURATIONS

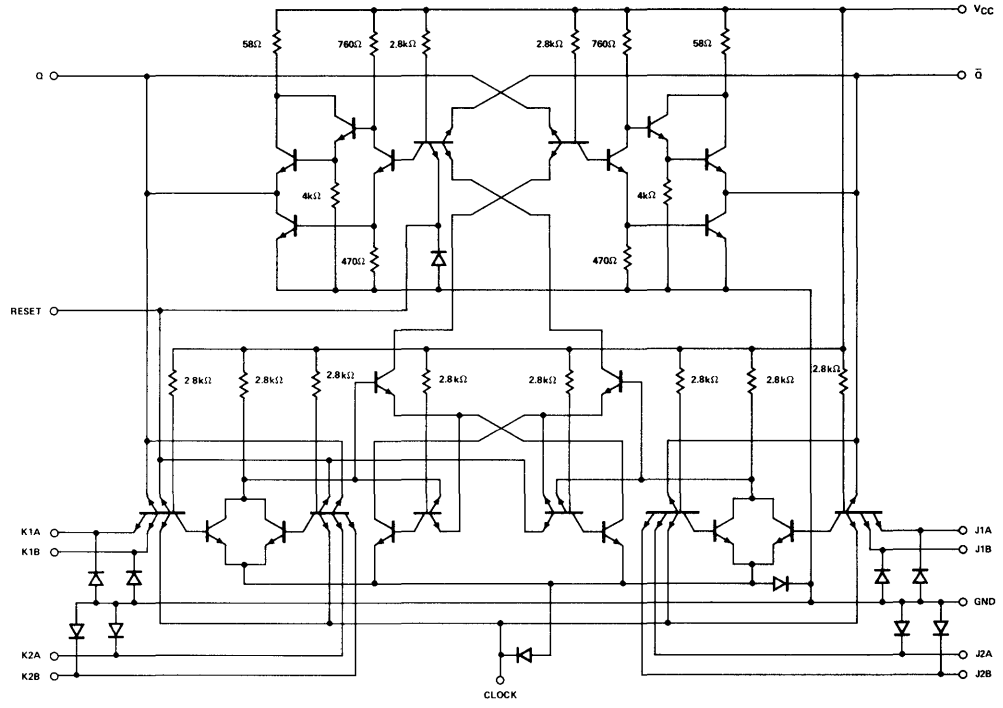
W PACKAGE



A,F PACKAGE



SCHEMATIC



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H71 Circuits	4.5	5	5.5	V
	N74H71 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H71 Circuits	-55	25	125	°C
	N74H71 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Input Setup Time, t_{setup} (See Above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(0)}$	Logical 0 level input current at preset	V_{CC} = MAX,	V_{in} = 0.4V			-6	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V			-4	mA
$I_{in(1)}$	Logical 1 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, or K2B	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4V			150	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current **	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			19	30	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25 pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 25 pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 25 pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25 pF,	R_L = 280Ω	6	14	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25 pF,	R_L = 280Ω	10	22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

J-K MASTER-SLAVE FLIP-FLOP

S54H72
N74H72

S54H72–A,F,W • N74H72–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state

TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES:

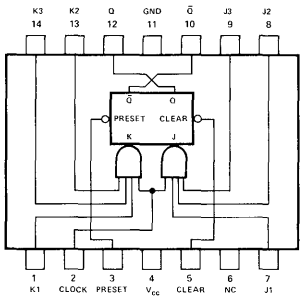
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = bit time before clock pulse
4. t_{n+1} = bit time after clock pulse.

POSITIVE LOGIC

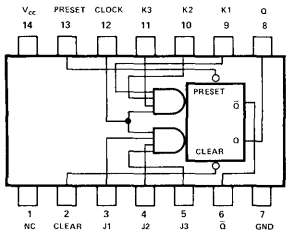
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

PIN CONFIGURATIONS

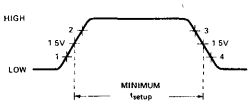
W PACKAGE



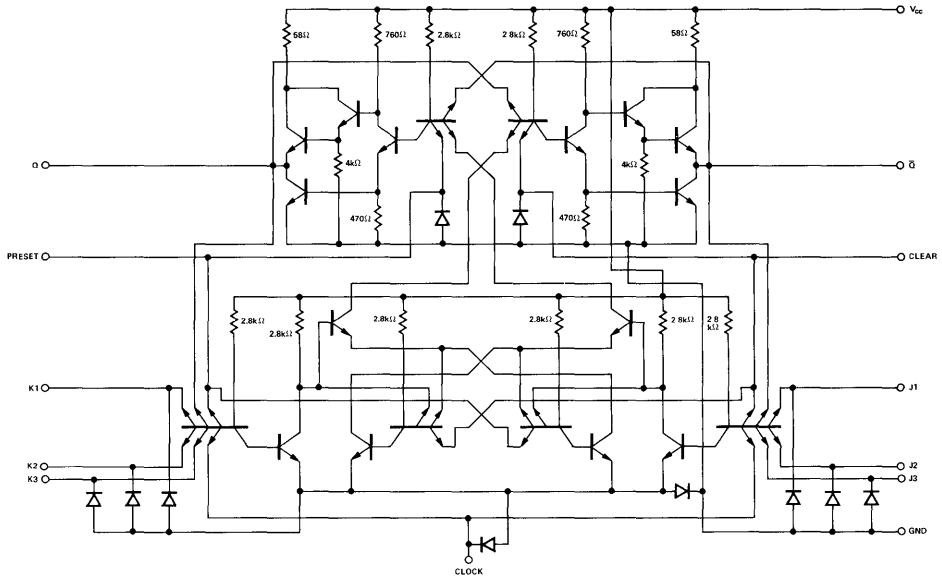
A,F PACKAGE



CLOCK WAVEFORM



SCHEMATIC DIAGRAM



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H72 Circuits		4.5	5	5.5	V
N74H72 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H72 Circuits	-55	25	125	°C
	N74H72 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN,				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = –500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	V_{CC} = MAX,	V_{in} = 0.4V			–2	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 0.4V			–4	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			100 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,			16	25	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DUAL J-K-MASTER-SLAVE FLIP-FLOP

S54H73
N74H73

S54H73–A,F,W • N74H73–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:

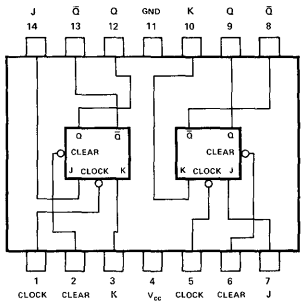
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

POSITIVE LOGIC

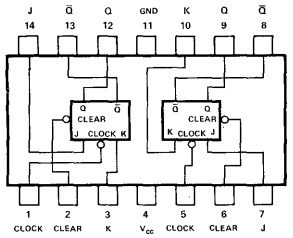
Low input to clear sets Q to logical 0
Clear is independent of clock

PIN CONFIGURATIONS

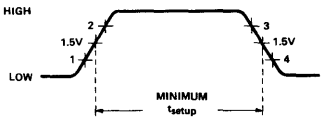
W PACKAGE



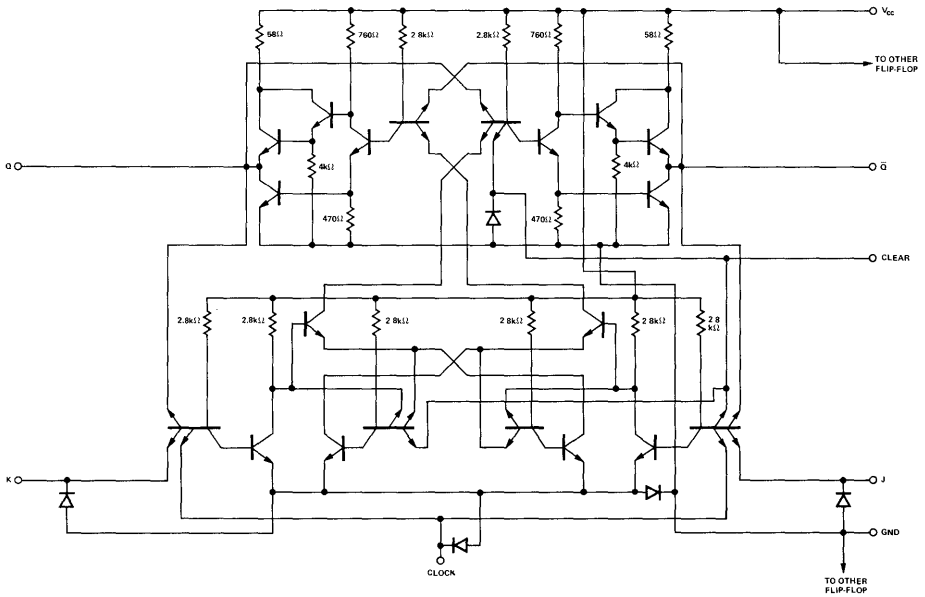
A,F PACKAGE



CLOCK WAVEFORM



SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H73 Circuits		4.5	5	5.5	V
N74H73 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H73 Circuits	-55	25	125	°C
	N74H73 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See above)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS**		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(0)}$	Logical 0 level input current at clear	V_{CC} = MAX,	V_{in} = 0.4V			-4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			32	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C

DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

S54H74–A,F,W • N74H74–A,F

DIGITAL 54/74 TTL SERIES

S54H74
N74H74

DESCRIPTION

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify systems design. A full fan-out to 10 normalized Series 54H/74H loads is available from each of the outputs in the low-level condition. In the high-level state, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 35 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

TRUTH TABLE

LOGIC

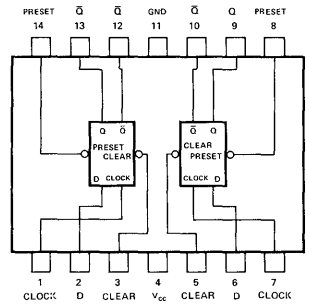
(Each Flip-Flop)		
t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
L	L	H
H	H	L

H = High Level, L = Low Level

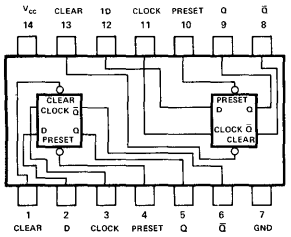
NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

PIN CONFIGURATIONS

W PACKAGE



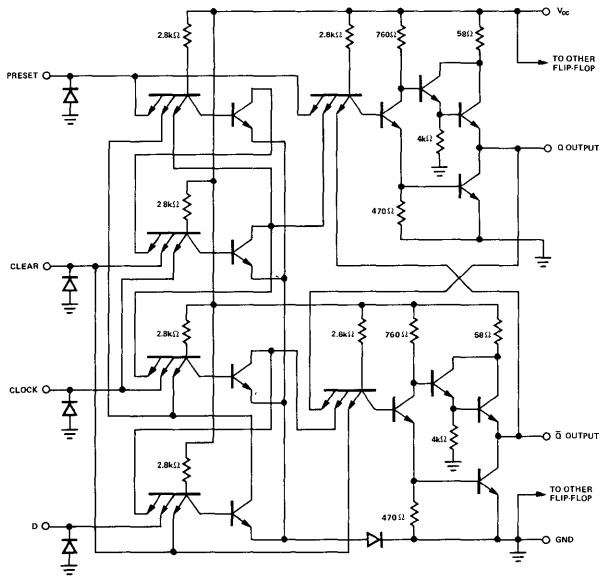
F PACKAGE



ASYNCHRONOUS INPUTS

Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

	S54H74			N74H74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N							
Low Logic Level			10			10	
High Logic Level			20			20	
Clock Frequency, f_{clock}	0		35†	0		35	MHz
Width of Clock Pulse, $t_{w(clock)}$	15†			15†			ns
Width of Preset Pulse, $t_{w(preset)}$	25†			25†			ns
Width of Clear Pulse, $t_{w(clear)}$	25†			25†			ns
Input Setup Time, t_{setup} (See Note 3):							
High-level data	10†			10†			ns
Low-level data	15†			15†			ns
Input Hold Time, t_{hold} (See Note 4)	0			0			ns
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

NOTES:
3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

† These conditions are recommended for use at V_{CC} = 5V, T_A = 25°C.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = -1mA	2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20mA		0.22	0.4	V
I_{IH}	High-level input current into D	V_{CC} = MAX,	V_I = 2.4V			50	µA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current into preset or clock	V_{CC} = MAX,	V_I = 2.4V			100	µA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current into clear	V_{CC} = MAX,	V_I = 2.4V			150	µA
		V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IL}	Low-level input current into preset or D	V_{CC} = MAX,	V_I = 0.4V			-2	mA
I_{IL}	Low-level input current into clear or clock	V_{CC} = MAX,	V_I = 0.4V			-4	mA
I_{OS}	Short circuit output current†	V_{CC} = MAX,		-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	S54H74		30	42	mA
			N74H74		30	50	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency			35	43		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs					20	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs	C_L = 25pF,	R_L = 280Ω			30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			4	8.5	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input			7	13	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

DUAL J-K MASTER-SLAVE FLIP-FLOP

S54H76
N74H76

S54H76-B • N74H76-B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

LOGIC

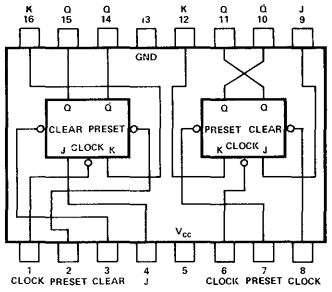
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:

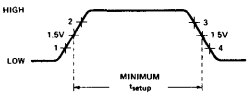
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

PIN CONFIGURATIONS

B PACKAGE



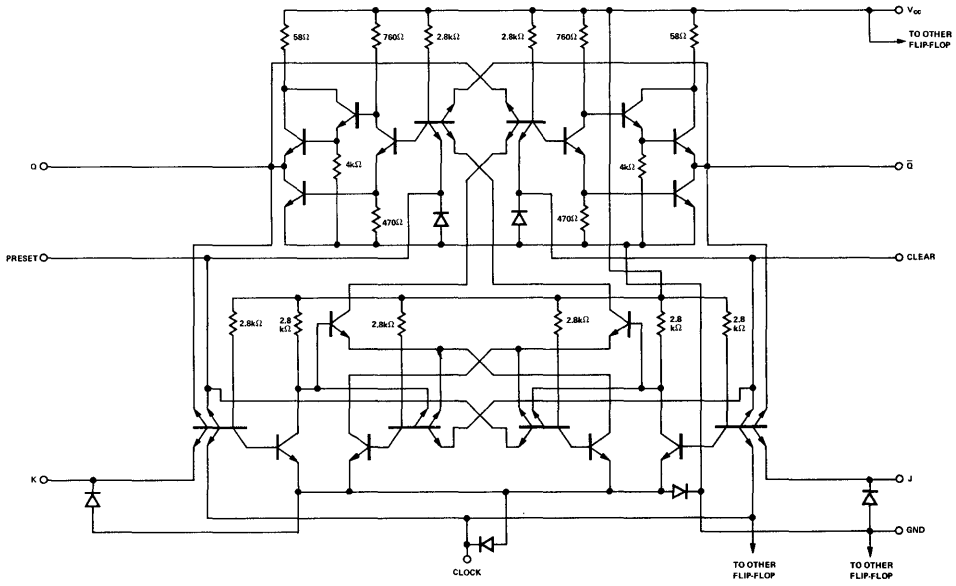
CLOCK WAVEFORM



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent of clock

SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H76 Circuits		4.5	5	5.5	V
N74H76 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H76 Circuits	-55	25	125	°C
	N74H76 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		12			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		$\geqslant t_{p(clock)}$			
Input Setup Time, t_{setup} (See above)					
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clock	V_{CC} = MAX,	V_{in} = 0.4V			-2	mA
$I_{in(0)}$	Logical 0 level input current at clear or preset	V_{CC} = MAX,	V_{in} = 0.4V			-4	mA
$I_{in(1)}$	Logical 1 level input current at J,K, or clock	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			50 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear or preset	V_{CC} = MAX, V_{CC} = MAX,	V_{in} = 2.4V V_{in} = 5.5V			100 1	μA mA
I_{OS}	Short circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V		32	50	mA

SWITCHING CHARACTERISTICS, V_{CC}= 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_L = 25pF,	R_L = 280Ω	25	30		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		6	13	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_L = 25pF,	R_L = 280Ω		12	24	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω		16	21	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

** Not more than one output should be shorted at a time.

J-K EDGE-TRIGGERED FLIP-FLOP

S54H101
N74H101

S54H101–A,F,W • N74H101–A,F

DESCRIPTION

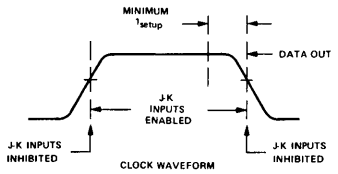
These monolithic J-K flip-flops are negative-edge-triggered. The AND-OR gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable-will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

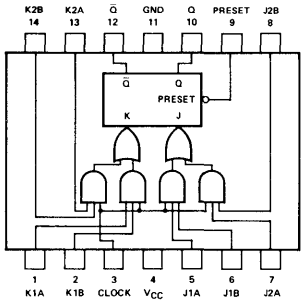
NOTES:
1. J=(J1A•J1B)+(J2A•J2B)
2. K=(K1A•K1B)+(K2A•K2B)
3. t_n=Bit time before clock pulse
4. t_{n+1}=Bit time after clock pulse

CLOCK WAVEFORM

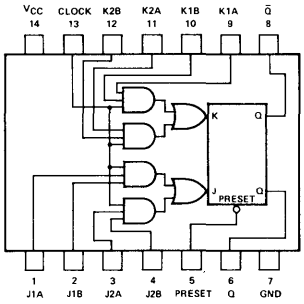


PIN CONFIGURATIONS

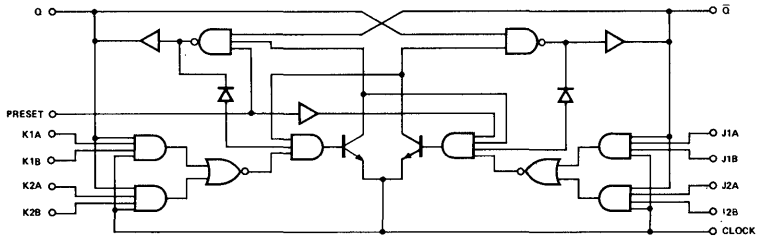
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H101 Circuits	4.5	5	5.5	V
	N74H101 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H101 Circuits	-55	25	125	°C
	N74H101 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Input Setup Time, t_{setup} (See Above):	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1A, J1B, J2A, J2B, K1A, K1B, K2A, K2B, or preset	V_{CC} = MAX,	V_{in} = 0.4 V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4 V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4 V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			20	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25 pF,	R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 25 pF,	R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock low)	C_L = 25 pF,	R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output (clock high)	C_L = 25 pF,	R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

J-K EDGE-TRIGGERED FLIP-FLOPS WITH AND INPUTS

S54H102
N74H102

S54H102–A,F,W • N74H102–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic J-K flip-flops are negative edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable-will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

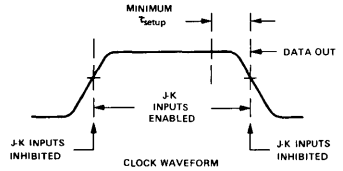
TRUTH TABLE

LOGIC

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

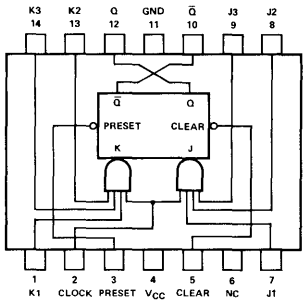
NOTES:
1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC—No Internal Connection.

CLOCK WAVEFORM

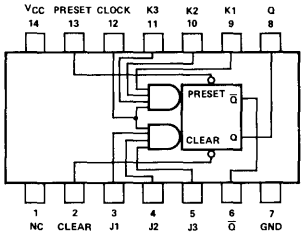


PIN CONFIGURATIONS

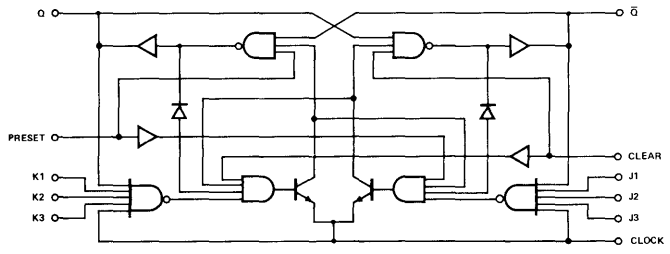
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H102 Circuits	4.5	5	5.5	V
	N74H102 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H102 Circuits	-55	25	125	°C
	N74H102 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		15			ns
Width of Clear Pulse, $t_{p(clear)}$		15			ns
Input Setup Time, t_{setup} (See Above):	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, K3, preset, or clear	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current clock	V_{CC} = MAX,	V_{in} = 0.4V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current**	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			20	38	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H103
N74H103

S54H103–A,F,W • N74H103–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable-will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative edge of the clock pulse.

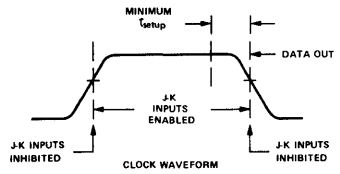
TRUTH TABLE

t_n J	t_n K	t_{n+1} Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES:

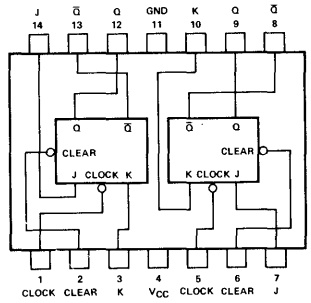
1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse

CLOCK WAVEFORM

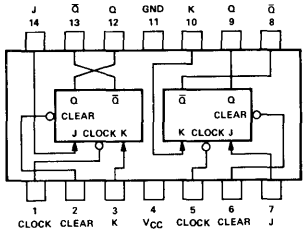


PIN CONFIGURATIONS

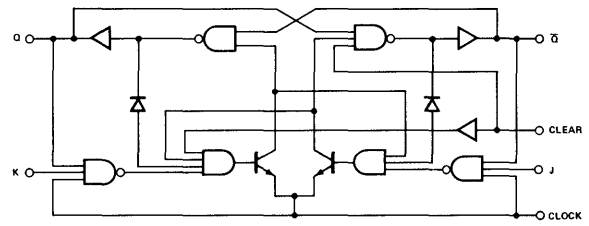
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H103 Circuits		4.5	5	5.5	V
N74H103 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H103 Circuits	-55	25	125	°C
	N74H103 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}: Logical 1		10			ns
Logical 0		13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, or clear	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current **	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output. (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed one second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H106
N74H106

S54H106–B,F,W • N54H106–B,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual monolithic J-K flip-flops are negative edge-triggered. They feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

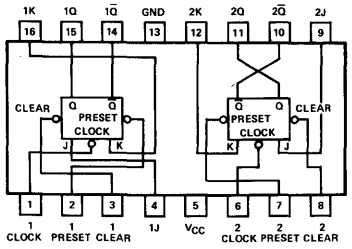
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

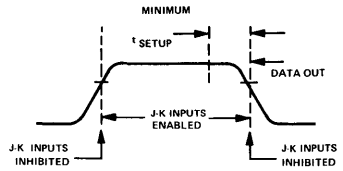
NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

PIN CONFIGURATION

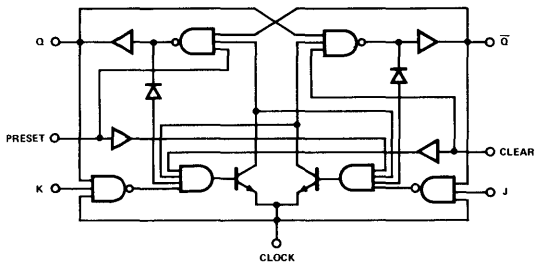
B,F,W PACKAGE



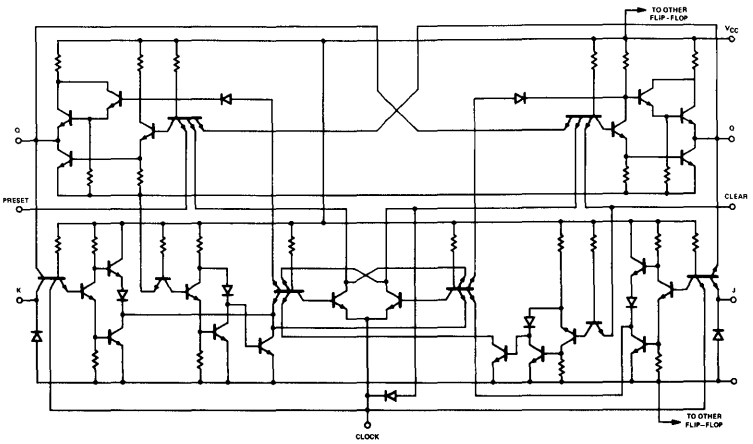
CLOCK WAVEFORM



BLOCK DIAGRAM (each flip-flop)



SCHEMATIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S54H106 Circuits		4.5	5	5.5	V
N74H106 Circuits		4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H106 Circuits	-55	25	125	°C
	N74H106 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		16			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup} (See Above):	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP§	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = 500 μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20 mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J, K, preset, or clear	V_{CC} = MAX,	V_{in} = 0.4 V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4 V		-3	-4.8	mA
$I_{in(1)}$	Logical 1 level input current at	V_{CC} = MAX,	V_{in} = 2.4 V			50	μA
	J or K	V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at	V_{CC} = MAX,	V_{in} = 2.4 V			100	μA
	present or clear	V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at	V_{CC} = MAX,	V_{in} = 2.4 V	0		-1	mA
	clock	V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current‡	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§All typical values are at V_{CC} = 5 V, T_A = 25°C.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25 pF,	R_L = 280 Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	C_L = 25 pF,	R_L = 280 Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	C_L = 25 pF,	R_L = 280 Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	C_L = 25 pF,	R_L = 280 Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25 pF,	R_L = 280 Ω	8	16	20	ns

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54H108
N74H108

S54H108–A,F,W • N74H108–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These dual monolithic J-K flip-flops are negative-edge-triggered. They feature individual J, K, and asynchronous preset inputs to each flip-flop as well as common clock and asynchronous clear inputs. When the clock goes high, the inputs are enabled and data is accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable performs according to the truth table as long as minimum set-up times are observed. Data input is transferred to the outputs on the negative edge of the clock pulse.

TRUTH TABLE

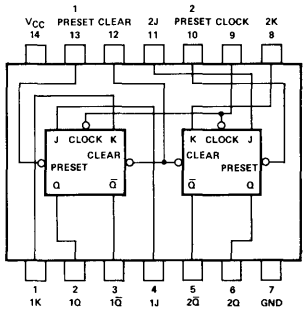
LOGIC

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

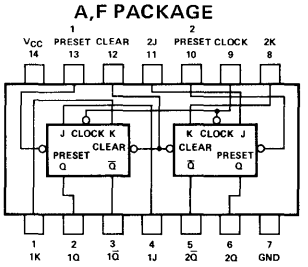
NOTES:
1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	S54H108 Circuits	4.5	5	5.5	V
	N74H108 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:	S54H108 Circuits	-55	25	125	°C
	N74H108 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$		10			ns
Width of Preset Pulse, $t_{p(preset)}$		15			ns
Width of Clear Pulse, $t_{p(clear)}$		16			ns
Input Setup Time, t_{setup}:	Logical 1	10			ns
	Logical 0	13			ns
Input Hold Time, t_{hold}		0			ns
Clock Pulse Transition Time, t_0				150	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP†	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = -500μA	2.4	3.2		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 20mA		0.25	0.4	V
$I_{in(0)}$	Logical 0 level input current at J,K, or preset	V_{CC} = MAX,	V_{in} = 0.4V		-1	-2	mA
$I_{in(0)}$	Logical 0 level input current at clock	V_{CC} = MAX,	V_{in} = 0.4V		-6	-9.6	mA
$I_{in(0)}$	Logical 0 level input current at clear	V_{CC} = MAX,	V_{in} = 0.4V		-2	-4	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX,	V_{in} = 2.4V			50	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	V_{CC} = MAX,	V_{in} = 2.4V	0		-1	mA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA

ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current at preset	V_{CC} = MAX,	V_{in} = 2.4V			100	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX,	V_{in} = 2.4V			200	μA
		V_{CC} = MAX,	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current **	V_{CC} = MAX,	V_{in} = 0	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX			40	76	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum input clock frequency	C_L = 25pF,	R_L = 280Ω	40	50		MHz
t_{pd1}	Propagation delay time to logical 1 level from preset or clear to output	C_L = 25pF,	R_L = 280Ω		8	12	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock low)	C_L = 25pF,	R_L = 280Ω		23	35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset or clear to output (clock high)	C_L = 25pF,	R_L = 280Ω		15	20	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 25pF,	R_L = 280Ω	5	10	15	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 25pF,	R_L = 280Ω	8	16	20	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

† All typical values are at V_{CC} = 5V, T_A = 25°C.

Schottky TTL
54S/74S SSI Devices

SECTION 4

SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC FOR HIGH-SPEED, HIGH-PERFORMANCE DIGITAL SYSTEMS

DESCRIPTION

Series 54S/74S Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.

Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54S/74S circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54L/74L TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the four speed-power ranges offered (Series 54/74, 54H/74H, 54L/74L, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54S circuits and over the temperature range of 0°C to 70°C for Series 74S circuits.

FEATURES

VERY-HIGH-SPEED, LOW-POWER OPERATION

- 3-ns typical gate propagation delay time
- 19-mW-per-gate power dissipation at 50% duty cycle—speed-power product = 57pJ
- 125-MHz typical J-K flip-flop maximum input clock frequency (d-c coupled)

EASE OF SYSTEM DESIGN

- fully compatible with Series 54/74, 54H/74H, and 54L/74L TTL (including MSI/LSI), and most DTL
- Schottky-diode-clamped inputs simplify system design
- terminated, controlled-impedance lines not normally required
- low output impedance: provides low AC noise susceptability drives highly capacitive loads

IMPROVED CIRCUIT PERFORMANCE

- switching times virtually insensitive to power supply and/or temperature variations
- power dissipation remains relatively low at operating frequencies up to 100 MHz
- high-fan-out: 20 54S/74S loads at the high logic level 10 54S/74S loads at the low logic level
- high DC noise margin—typically 1 volt

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range unless otherwise noted)

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Intermitter Voltage	5.5V
Output Voltage	7V
Operating Free-Air Temperature Range:	
Series 54S Circuits	−55°C to 125°C
Series 74S Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES:

1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

UNUSED INPUTS OF POSITIVE-AND/NAND GATES

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not to exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7V and 3.5V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

INPUT-CURRENT REQUIREMENTS

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 2mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 50μA maximum for each emitter. Currents into the input terminals are specified as positive values.

FAN-OUT CAPABILITY

Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54H, 74H, 54S, or 74S loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard output is capable of sinking current from 10 Series 54H, 74H, 54S, or 74S loads (N_L = 10).

RECOMMENDED OPERATING CONDITIONS

	SERIES 54S CIRCUITS			SERIES 74S CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

S54S/N74SXX
Electrical Characteristics

SECTION 5

OPEN COLLECTOR POSITIVE-NAND GATE

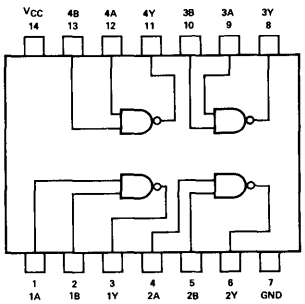
S54S00
S54S03
N74S00
N74S03

S54S00/503–A,F • N74S00/503–A,F

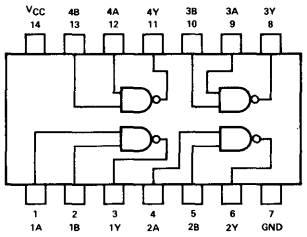
DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS

W PACKAGE

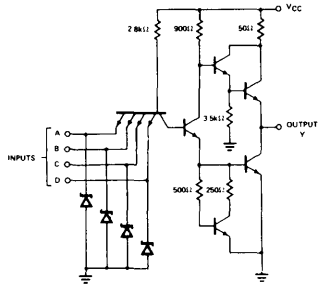


A,F PACKAGE



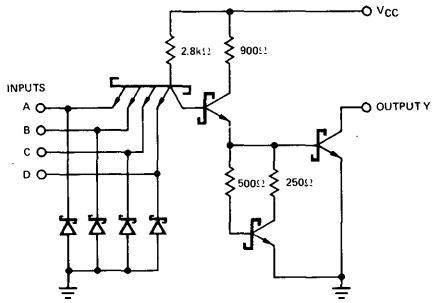
SCHEMATIC (each gate)

S54/N74S00



NOTE:
Component values shown are nominal.

S54/N74S03



RECOMMENDED OPERATING CONDITIONS

	S54S00			N74S00			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *			MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
		I_{OH} = -1mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			-40		-100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	2	3	4.5	ns
		C_L = 50pF,	R_L = 280Ω		4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω	2	3	5	ns
		C_L = 50pF,	R_L = 280Ω		5		

S54/N74S03

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_{IL} = 0.8V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	2	5	7.5	ns
		C_L = 50pF,	R_L = 280Ω		7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω	2	4.5	7	ns
		C_L = 50pF,	R_L = 280Ω		7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, t_1 = t_0 = 2.5ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\Omega$.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

OPEN COLLECTOR POSITIVE-HEX INVERTER

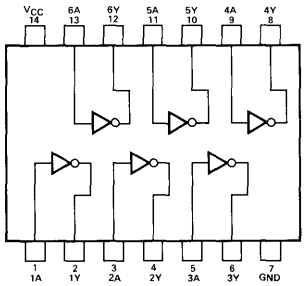
S54S04
S54S05
N74S04
N74S05

S54S04—A,F,W • S54S05—A,F,W • N74S04—A,F,W • N74S05—A,F

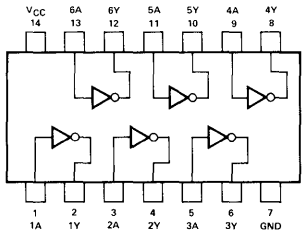
DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS

W PACKAGE

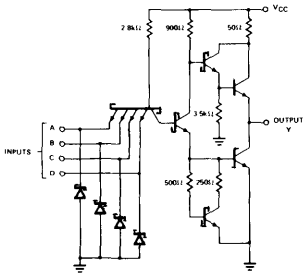


A,F PACKAGE

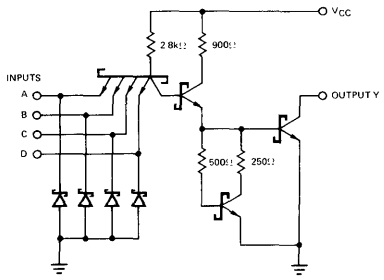


SCHEMATIC (each gate)

S54/N74S04



S54/N74S05



NOTE: Component values shown are nominal.

RECOMMENDED OPERATING CONDITIONS

		S54S04			N74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:	High logic level			20			20	
	Low logic level			10			10	
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
		I_{OH} = -1mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			-40		-100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	4.5	ns
		C_L = 50 pF,	R_L = 280 Ω		4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	5	ns
		C_L = 50 pF,	R_L = 280 Ω		5		

S54/N74S05

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_{IL} = 0.8V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	2	5	7.5	ns
		C_L = 50pF,	R_L = 280Ω		7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω	2	4.5	7	ns
		C_L = 50pF,	R_L = 280Ω		7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

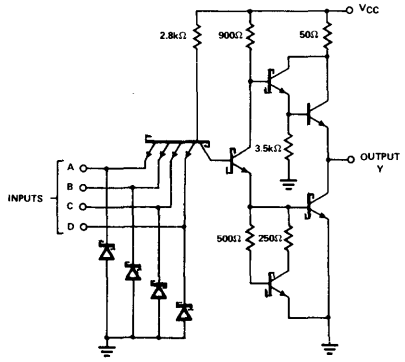
NOTES:

A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, t_1 = t_0 = 2.5ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\Omega$.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

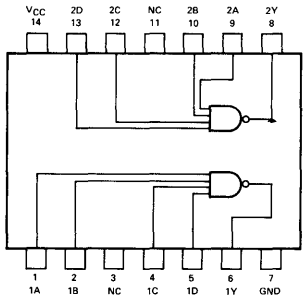
SCHEMATIC (each gate)



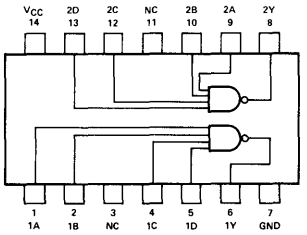
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S54S20			N74S20			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
		I_{OH} = -1mA		Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2V,					
		I_{OL} = 20mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX			-40		-100	mA
ICCH	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			2.5	4	mA
ICCL	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	2	3	4.5	ns
		C_L = 50pF,	R_L = 280Ω		4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω	2	3	5	ns
		C_L = 50pF,	R_L = 280Ω		5		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, $t_1 = t_0$ = 2.5ns, PRR = 1MHz, duty cycle = 50%, and $Z_{out} \approx 50\Omega$.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

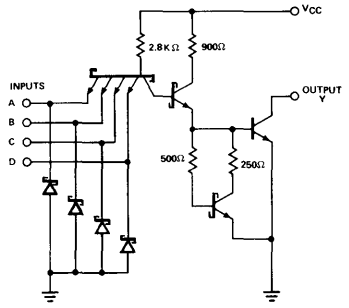
POSITIVE-NAND GATE WITH OPEN-COLLECTOR OUTPUTS

S54S22
N74S22

S54S22–A,F,W • N74S22–A,F

DIGITAL 54/74 TTL SERIES

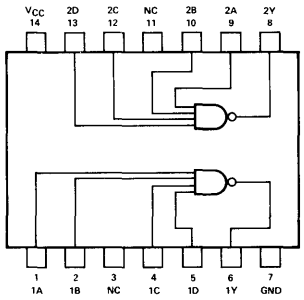
SCHEMATIC (each gate)



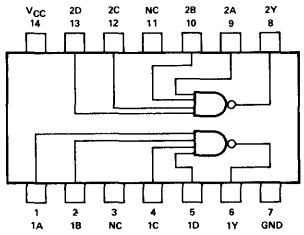
NOTE: Component values shown are nominal.

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



RECOMMENDED OPERATING CONDITIONS

	S54S22			N74S22			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from any Output, N			10			10	
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_{IL} = 0.8V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20mA	V_{IH} = 2V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V			-2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V		5	9	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15pF,	R_L = 280Ω	2	5	7.5	ns
		C_L = 50pF,	R_L = 280Ω		7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15pF,	R_L = 280Ω	2	4.5	7	ns
		C_L = 50pF,	R_L = 280Ω		7		

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

NOTES:

A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, $t_1 = t_0$ = 2.5ns, PRR = 1MHz, duty cycle = 50%, and $Z_{out} \approx 50\Omega$.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

DUAL J-K EDGE-TRIGGERED FLIP-FLOP

S54S112
N74S112

S54S112–B,F,W • N74S112–B

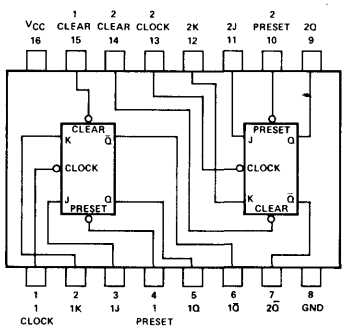
DIGITAL 54/74 TTL SERIES

DESCRIPTION

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup and hold times are observed. Input data are transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

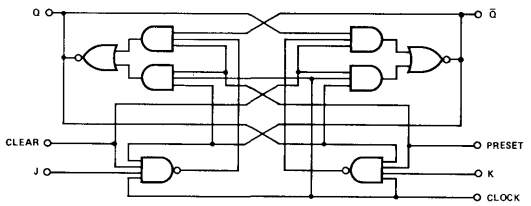
A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

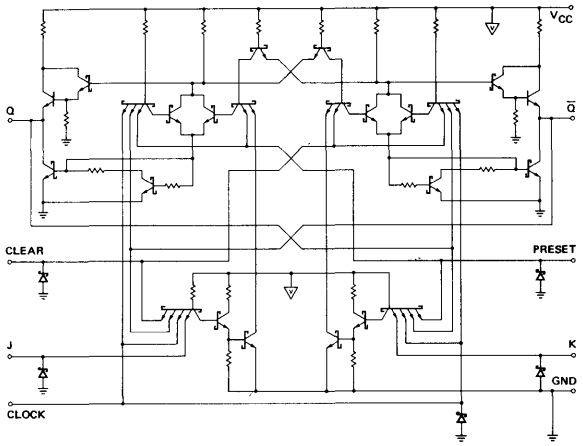
POSITIVE LOGIC

positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Clear and preset are independent of clock.

LOGIC DIAGRAM (each flip-flop)



SCHEMATIC (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

	S54S112			N74S112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N : High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		80	0		80	MHz
Width of Clock Pulse, $t_{w(clock)}$	6			6			ns
Width of Preset Pulse, $t_{w(preset)}$	8			8			ns
Width of Clear Pulse, $t_{w(clear)}$	8			8			ns
Input Setup Time, t_{setup} (See Note 1)	3			3			ns
Input Hold Time, t_{hold} (See Note 2)	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS *			MIN	TYP **	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -1mA	S54S112	2.5	3.4		V
				N74S112	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V		J or K input			50	μA
				Clock, preset, or clear			100	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V		J or K input			-1.6	mA
				Clock			-4	
				Preset or clear			-7	
I_{OS}	Short-circuit output current†	V_{CC} = MAX,			-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3			30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset	C_L = 15pF, R_L = 280Ω	2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES:

1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.
3. I_{CC} is measured with outputs open, clock grounded, and J-K preset and clear at 4.5V.

DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

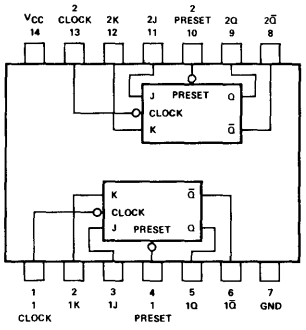
S54S113
S54S114
N74S113
N74S114

S54S113–A,F,W • S54S114–A,F,W • N74S113–A,F• N74S114–A,F

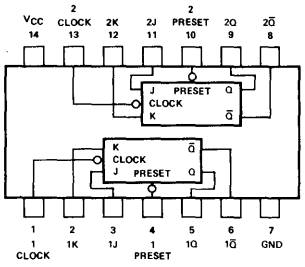
DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS

Q PACKAGE



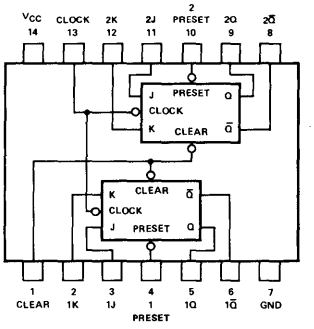
A,F PACKAGE



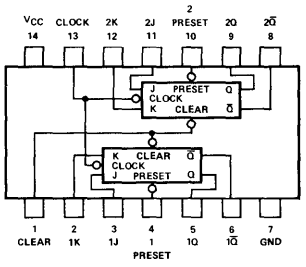
S54S113, N74S113

PIN CONFIGURATIONS

W PACKAGE



A,F PACKAGE



S54S114, N74S114

DESCRIPTION

The S54S113 and N74S113 offer individual J, K, preset, and clock inputs. The S54S114 and N74S114 offer common clock and common clear inputs and individual J, K, and preset inputs.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data are transferred to the outputs on the negative-going edge of the clock pulse.

TRUTH TABLE

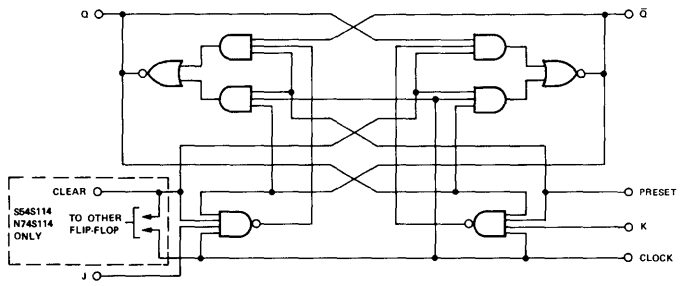
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:

A. t_n = bit time before clock pulse

B. t_{n+1} = bit time after clock pulse

LOGIC DIAGRAM (each flip-flop)



RECOMMENDED OPERATING CONDITIONS

	S54S113, S54S114			N74S113, N74S114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, f_{clock}	0		80	0		80	MHz
Width of Clock Pulse, $t_{w(clock)}$	6			6			ns
Width of Preset Pulse, $t_{w(preset)}$	8			8			ns
Width of Clear Pulse, $t_{w(clear)}$: S54S114, N74S114	8			8			ns
Input Setup Time, t_{setup}	3			3			ns
Input Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54S113 N74S113			S54S114 N74S114			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA			-1.2			-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = -1mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OL} = 20mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	J or K input			50			50	μA
			Clock			100			200	
			Preset			100			100	
			Clear						200	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	J or K input			-1.6			-1.6	mA
			Clock			-4			-8	
			Preset			-7			-7	
			Clear						-14	
I_{OS}	Short circuit output current†	V_{CC} = MAX		-40		-100	-40		-100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 1		30	50		30	50	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15pF, R_L = 280Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset		2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 64 through 69 of the Series 54H/74H section for test circuits.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5V.

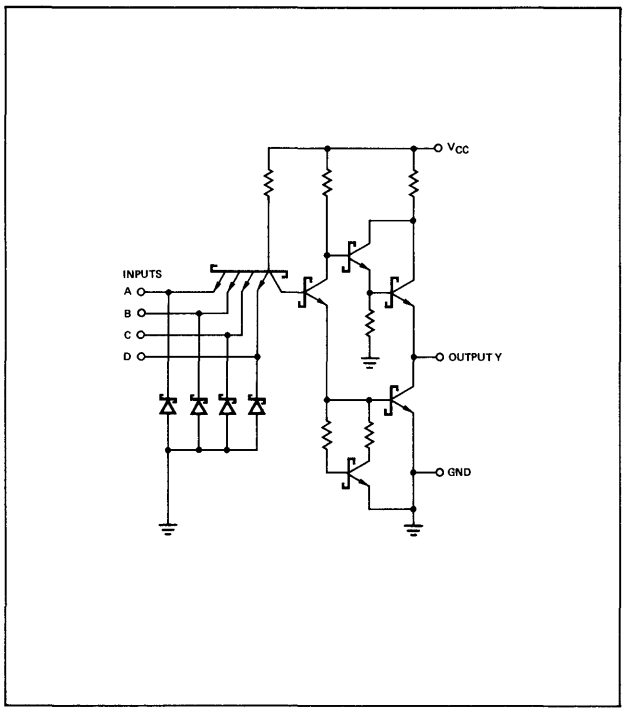
DUAL 4-INPUT POSITIVE-NAND BUFFERS/LINE DRIVERS

S54S40 S54S140 N74S40 N74S140

S54S40–A,F,W • S54S140–A,F,W • N74S40–A,F • N74S140–A,F

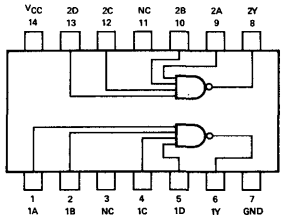
DIGITAL 54/74 TTL SERIES

SCHEMATIC (each gate)



PIN CONFIGURATIONS

A,F PACKAGE



NC — No internal connection

RECOMMENDED MAXIMUM FAN-OUT FROM EACH OUTPUT

Loads at a high logic level	60
Load at a low logic level	30

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -18mA				-1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -3mA	V_{IL} = 0.8V,	Series 54S	2.5	3.4		V
				Series 74S	2.7	3.4		
		V_{CC} = MIN, R_O = 50Ω To GND	V_I = 0.5V,	S54S140 N74S140	2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 60mA	V_{IH} = 2V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7V				100	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5V				-4	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX			-50		-225	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0V			5	9	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5V			12.5	22	mA

NOTES:

A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3V, $V_{in(0)}$ = 0V, $t_1 = t_0$ = 2.5ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\Omega$.

B. Inputs not under test are at 2.7V.

C. C_L includes probe and jig capacitance.

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50pF,	R_L = 93Ω	2	4	6.5	ns
		C_L = 150pF,	R_L = 93Ω		6		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 50pF,	R_L = 93Ω	2	4	6.5	ns
		C_L = 150pF,	R_L = 93Ω		6		ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed 100 milliseconds.

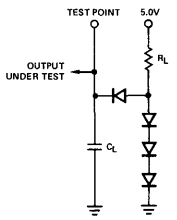
54/74 And 54/74H Typical A.C. Loads And Waveforms

SECTION 6

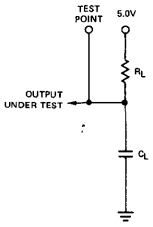
54/74 AND 54/74H TYPICAL A.C. LOADS AND WAVEFORMS

TYPICAL A.C. LOADS

STANDARD OUTPUT STRUCTURE

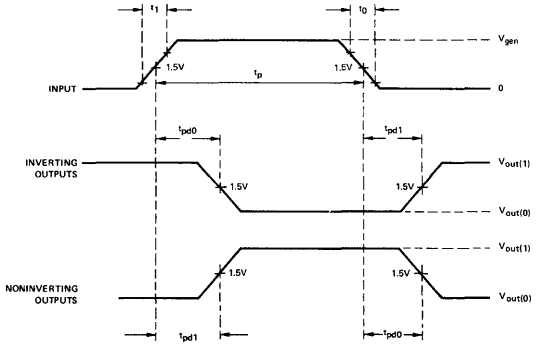


OPEN COLLECTOR STRUCTURE



NOTES:
R_L and C_L are specified for each part on the data sheet.
C_L includes probe and jig capacitance.
Diodes are 1N3064.

TYPICAL A.C. WAVEFORM



NOTES:
$t_1 \equiv t_r$ (typically $\leqslant$ 10ns)
$t_0 \equiv t_f$ (typically $\leqslant$ 10ns)
$t_{pd1} \equiv t_{PLH}$ (See Data Sheet)
$t_{pd0} \equiv t_{PHL}$ (See Data Sheet)
$t_p \equiv t_w \equiv P_w$ (Determined by device under test)
V_{GEN} Typically 3.0V
Point "a" is typically 0.7V or 10% of V_{GEN}
Point "b" is typically 2.7V or 90% of V_{GEN}

Signetics Sure 883 Program

SECTION 7

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical tests. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables IIIA, IIIB, and IIIC provide a complete process qualification and verification program in accordance with the conditions of MIL-STD-883, Group A, B and C tests. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period. A summary of these test results is available on request at the time of order placement.

* Systematic Uniformity and Reliability Evaluation

All of the applicable Electrical Parameters of Table IIIA are performed at pretest on the Table IIIC samples. This provides the MIL-STD-883 electrical parameter and design verification Group A tests. These tests are performed on representative circuit types from every die process family type in manufacturing during this period.

Table IIIB consists of the package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these package and assembly qualification tests.

Table IIIC consists of the die process oriented qualification electrical stress or operational tests at high temperature per MIL-STD-883, Groups B and C. Representative devices from each die process family are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

An additional screening series is available at extra cost. Details are given in Table V, MIL-STD-883, method 5004, high reliability screening.

Table I — 100% Production Screen Tests

TEST	CONDITIONS
Preseal Visual	High Power — Low Power
Thermal Shock	Liquid to Liquid, 5 Cycles, 60 Seconds at 0°C, 60 Seconds at 100°C, transfer time 5 Seconds. (See Note 1.)
Centrifuge	Y_1 Axis; 30,000 g minimum, 1 minute. (See Note 1.)
Hermeticity	Gross leak test (Bubble Test). (See Note 1.)
Production Electrical Tests	

Table II — Signetics Acceptance Tests (See Notes 2 and 3)

SIGNETICS SUBGROUP	TEST	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
A-2	DC Parameters	$T_A = +25°C$	1.0%	II
A-3	DC Parameters	$T_A = +25°C$	1.0%	II
A-4	DC Parameters	$T_A = +125° C$	1.0%	II
A-5	DC Parameters	$T_A = -55°C$	1.0%	II
A-6	AC Parameters	$T_A = +25°C$	1.0%	II

TABLE IIIA. MIL-STD-883 GROUP A ELECTRICAL TESTS

MIL-STD-883 GROUP A SUBGROUP	SIGNETICS SUBGROUP	TEST DESCRIPTION
A1	A-2, A-3	Static tests at 25°C
A2	A-4	Static tests at maximum rated operating temperature.
A3	A-5	Static tests at minimum rated operating temperature.
A4	A-6	Dynamic tests at 25°C,
A5	C 2, when applicable	Dynamic tests at maximum rated operating temperature.
A6	C 2, when applicable	Dynamic tests at minimum rated operating temperature.
A7	*	Functional tests at 25°C.
A8	A-4, A-5	Functional tests at maximum and minimum rated operating temperatures.
A9	A-6	Switching tests at 25°C.
A10	C-2, when applicable	Switching tests at maximum rated operating temperature.
A11	C-2, when applicable	Switching tests at minimum rated operating temperature.

TABLE IIIB. MIL-STD-883 GROUPS B AND C ENVIRONMENTAL TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
B_1	Physical Dimensions	2008	Test Condition A	15
B_2	Marking Permanency Visual and Mechanical Bond Strength	2008 2008 2011	Test Condition B, Para. 3,2,1 Test Condition B Test Condition D	4 devices/no failure 1 device/no failure 15
B_3	Solderability	2003	Solder Temperature 260°C ±10°C	15
B_4	Lead Fatigue Hermeticity a. Fine b. Gross	2004 1014	Test Condition B_2 See Note 4 Test Condition A or B Test Condition C	15
C_1	Pre-Test Electrical Parameters Thermal Shock Temperature Cycle Moisture Resistance End Point Electrical Parameters FAILURE CRITERIA	 1011 1010 1004	Signetics Subgroup A-3 15 Cycles. Test Condition C, +150°C to -65°C 10 Cycles. Test Condition C, 150°C to -65°C Omit initial conditioning. Signetics Subgroup A-3 Refer to Table IV.	15
C_2	Pre-Test Electrical Parameters Mechanical Shock Vibration Variable Frequency Constant Acceleration End Point Electrical Parameters FAILURE CRITERIA	 2002 2007 2001	Signetics Subgroup A-3 Test Condition B Test Condition A Test Condition E Signetics Subgroup A-3 Refer to Table IV.	15
C_3	Salt Atmosphere	1009	Test Condition A. Omit initial conditioning.	15
C_4	Pre-Test Electrical Parameters High Temperature Storage End Point Electrical Parameters FAILURE CRITERIA	 1008	Signetics Subgroup A-3 T_A = +150°C, t = 1000 hours Signetics Subgroup A-3 Refer to Table IV.	λ = 15

TABLE IIIC. MIL-STD-883 GROUPS B AND C HIGH TEMPERATURE OPERATING LIFE TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
	Pre-Test and Design Verification Electrical Parameters		Table IIIA as applicable, data sheet groups A & C.	
C_6	High Temperature Steady State Reverse Bias End Point Electrical Parameters FAILURE CRITERIA	1015	Test Condition A. T_A = 150°C t = 72 hours. Signetics Subgroup A-3 Refer to Table IV	λ = 10
B_5 & C_5	High Temperature Operating Life End Point Electrical Parameters FAILURE CRITERIA	1005	Test Condition D or E as applicable. T_A = +125°C or +85°C, per Part Data Sheet. t = 1000 hours. Signetics Subgroup A-3 Refer to Table IV.	λ = 10

*Signetics performs a truth table test.

Table IV – Signetics Failure Criteria

TEST	"1" Input Current	"1" Output Voltage	"0" Input Current	"0" Output Voltage	Expansion Node Current
LIMITS	Data Sheet Limits and: 10X Initial Value for DTL 5X Initial Value for TTL	Data Sheet Limits and: ±20% Initial Value	Data Sheet Limits ±20% Initial Value	Data Sheet Limits and: ±0.1V	Data Sheet Limits and: ±20% Initial Value

Optional High Reliability Screening

To maximize reliability in critical application, the Optional High Reliability Screening of Table V provides for three levels of 100% screening per MIL-STD-883, Method 5004 at extra cost. This series eliminates the necessity for special specification, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal Group A acceptance test. Circuits subjected to this Preconditioning Series are clearly distinguishable from standard products in the following ways:

1. Individual serial number on each circuit (Class A only).
2. The first letters of a part number are either RA, RB, or RC.

   RA = Class A
   RB = Class B
   RC = Class C
   i.e., RA8880J = 100% screening of Table V, Class A.
3. Individual device variables parametric test data is supplied with each shipment (Class A only).

Consult your local representative for price information. Device types should be specified with the appropriate letter prefixes.

Notes:

1. Not applicable to solid molded packaged devices.
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
3. Detailed tests, conditions, and limits applicable to each subgroup are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table. See Table IIIA for the corresponding Group A tests of MIL-STD-883.
4. The Hermeticity tests are not employed for solid molded packages.
5. Class B and Class C may be subjected to thermal shock as an alternate.
6. The test sequence of fine and gross leak may be reversed when fluorocarbons are utilized for gross leak.
7. The individual MIL-STD-883 Test Methods are, in many cases designed to "stand alone" as a sole screen or sole Group B environmental sampling test. But since 5004 specifies a screening series or flow, some of the measurements, etc., specified in an individual Test Method are not intended to be applicable in the screening series.

TABLE V – MIL-STD-883 METHOD 5004, HIGH RELIABILITY SCREENING

TEST	MIL-STD-883 METHOD	CLASS A	CLASS B	CLASS C	CLARIFICATIONS (See Note 7)
Internal Visual (preseal)	2010.1	Cond. A	Cond. B	Cond. B	Test Condition A, Paragraph 3.1.1.7, a, delete the words "and parameter".
Stabilization Bake	1008 (24 hours)	Cond. C	Cond. C	Cond. C	Condition C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements at this point.
Thermal Shock	1011	Cond C	Not required. NOTE 5	Not required. NOTE 5	Cond. C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection at this point.
Temperature Cycling	1010	Cond. C	Cond. C NOTE 5	Cond. C NOTE 5	(150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection, no hermeticity tests at this point.
Mechanical Shock	2002, Y1 plane only	Cond. B	Not Required	Not Required	No electrical measurements at this point.
Centrifuge	2001	Cond. E Y2 then Y1 plane	Cond. E Y1 plane	Cond. E Y1 plane	
Hermeticity A. Fine Leak B. Gross Leak	1014, Note 6 (Hermetic devices only)	 Cond. A or B Cond. C	 Cond. A or B Cond. C	 Cond. A or B Cond. C	
Critical Electrical Parameters	Signetics Subgroup A-3	Read and Record	Not Required	Not Required	
Burn-In Test	1015, T_A = +125°C	240 hours Cond. D or E (as applicable)	168 hours Cond. D or E (as applicable)	Not Required	
Critical Electrical Parameters	Signetics Subgroup A-3	Read and Record	Not Required	Not Required	
Signetics FAILURE CRITERIA		Table IV	Not Required	Not Required	
Reverse Bias Burn In	1015, T_A = +150°C t = 72 hours	Cond. A or C	Not Required	Not Required	Required only when specified in the applicable procurement document. Signetics standard burn-in (above) includes reverse bias of unused junctions.
Final Electrical Test	Perform go no go measurements of Signetics Subgroup A Parameters	Signetics Subgroups A 2, A 4, A-5, A 6, Functional tests, truth table when applicable	Signetics Subgroups A 2, A 3, A 6, Functional tests, truth table when applicable	Signetics Subgroups A 2, A 3 Functional tests, truth table when applicable	
Radiographic Inspection	2012	Yes	Not Required	Not Required	
External Visual	2009	Yes	Yes	Yes	

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