

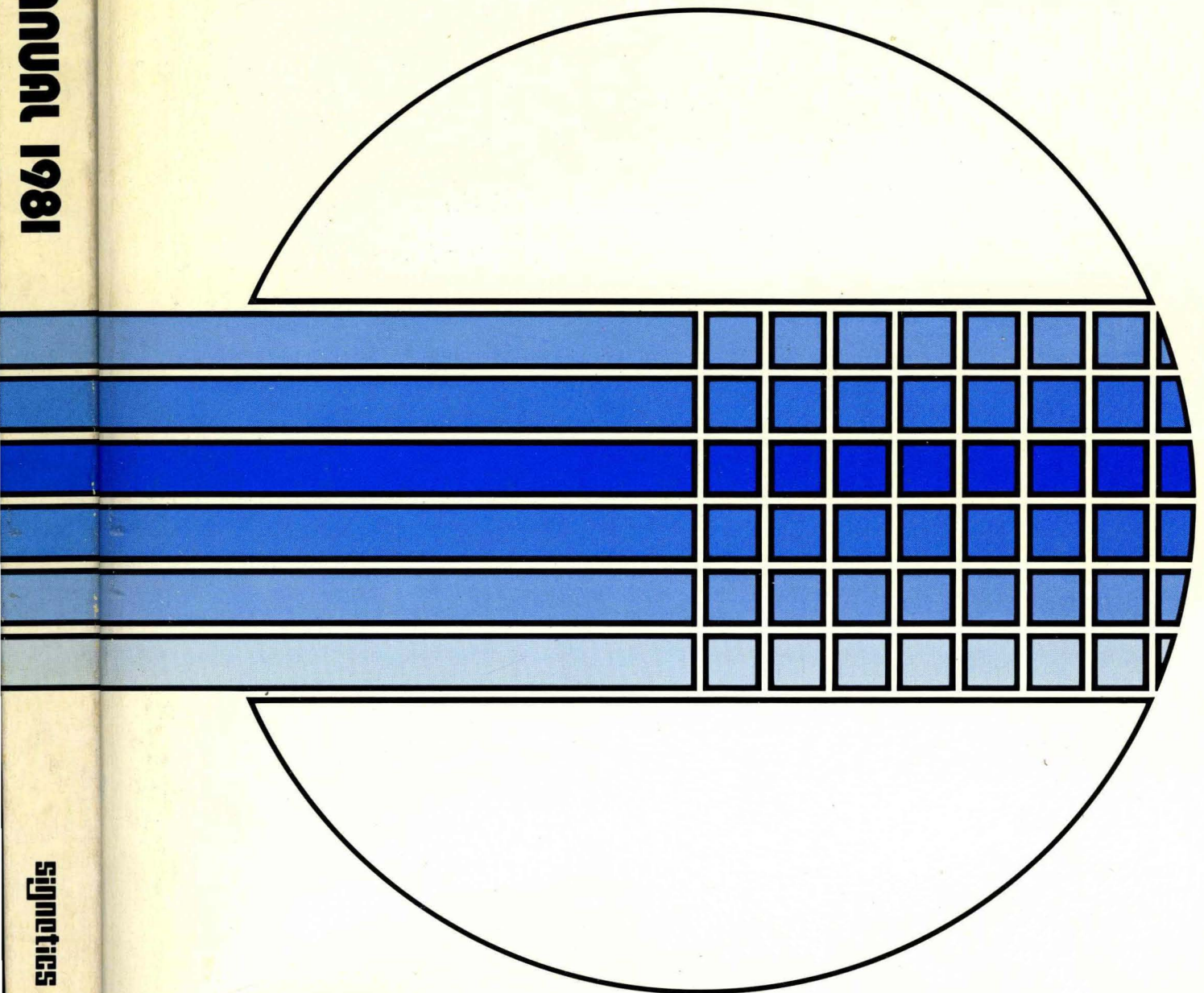
ANALOG DATA MANUAL 1981

**ANALOG
DATA
MANUAL
1981**

signetics

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*This data sheet may be obtained by writing Publication Services at Signetics, 811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-2111.

INTRODUCTION

As one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures, and sells over 1600 different types of integrated circuits. Signetics produces integrated circuits utilizing both bipolar and metal-oxide semiconductor (MOS) manufacturing processes for Memory, Microprocessor, Digital, and Analog applications.

The Analog division, one of eight divisions, is a major broad line supplier of Analog circuits consisting of Signetics' original designs, industry standard devices, and custom circuits for EDP, Automotive, Military, Communications, Industrial, and Consumer markets. The family of 555 Timers, the NE5534 High Performance Operational Amplifier, the NE5018 and NE5020 microprocessor compatible DAC's and the NE5560 Switched Mode Power Supply Regulator are a few examples of Signetics' original products. The breadth of the Analog product line offers the designer, the component engineer, and the purchasing agent a broad Analog circuit product line backed by Signetics' industry image as a quality manufacturer to whom the servicing of the customers' needs is paramount.

The 1981 Analog Data Manual is intended to serve as a single reference for Analog circuits by presenting information necessary to select Signetics' Analog products properly. The data manual is updated and rewritten to reflect data on new products issued in the past 2 years, as well as new package configurations such as the new microminiature packages which have recently been released for volume production. Designated the SO package (SO = Small Outline), this new package offers advantages to the hybrid as well as the P.C. board assembler in the purchasing of fully DC- and AC-tested circuits for substrate assembly. Complete details on this new package are available in the Packaging section at the end of this manual.

Additions and errata will be generated at periodic intervals as appropriate.

Your inputs to improve this or any of our publications would be greatly appreciated.

Lou Johnson
Marketing Manager, Analog Division

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
 \$1000 per order
 \$50 per line item per order

Military Product:
 \$250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

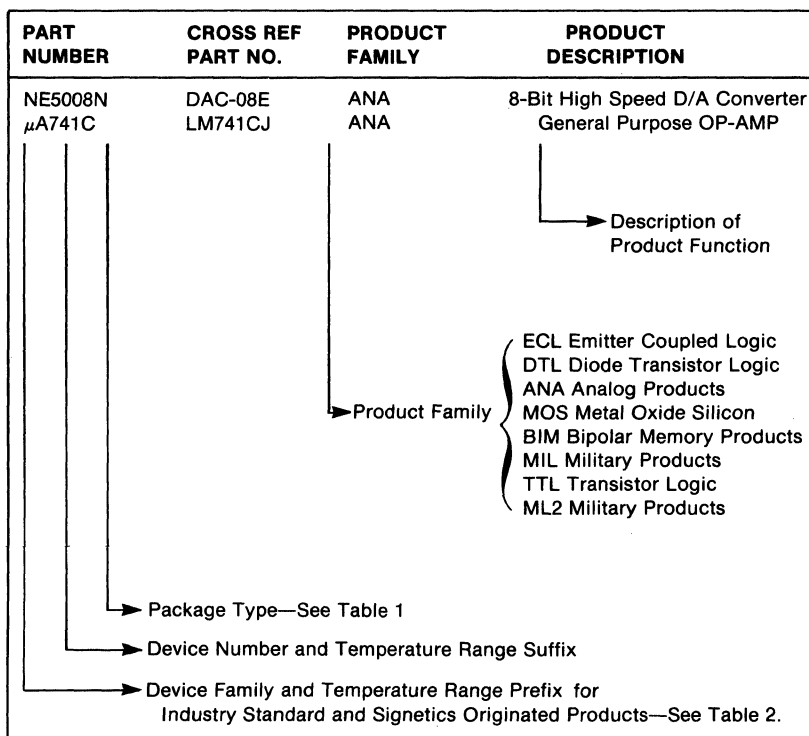


Table 1 PART NUMBER DESCRIPTION

SUFFIX		PACKAGE DESCRIPTION ²
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package
DB	HB	3-lead TO-39
DC	EC	4-lead TO-46
DE	EE	4-lead TO-72
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
SK	SK	Microprocessor kit
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 2 PACKAGE DESCRIPTIONS

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-40° to +85°C
SU	-25° to +85°C

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DS	Linear Industry Standard
JB	Mil Rel—Jan ² Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
SD	Linear DMOS
μ A	Linear Industry Standard
ULN	Linear Industry Standard

Table 4 FAMILY PREFIX

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time. The Signetics SUPR II Program has been designed to upgrade the basic product quality through the use of more rigorous screening criteria at the critical process steps. These additional screens constitute the Level A portion of the Program. A burn-in option is available for those users requiring enhanced reliability performance, and this option is designated as Level B.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. The SUPR II Program focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SURE II/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is available upon request as is the ten-year reliability summary, Signetics Product Reliability Report, R-363.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the cus-

tomers. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

SIGNETICS SUPR II LEVEL A

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAM's, ROM's, PROM's), and MOS Memories (RAM's, ROM's, Shift Registers). All package options are also available.

The SUPR II flow is detailed in Figure 5, including the test methods and Quality acceptance levels (Table 2 provides the electrical/mechanical finished product AQL's). Highlights of the flow are visual in-

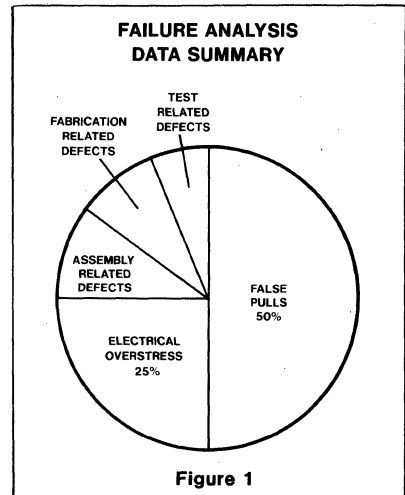


Figure 1

spectations, thermal shock preconditioning, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 2. Here we are comparing the various levels of inspection (AQL's) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing. Using the standard commercial AQL in functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically only 12% rework is required.

SIGNETICS SUPR II LEVEL B

Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system

FAILURE MECHANISMS	CAUSES	SUPR II CONTROL
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Bake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity Hot-Rail Testing
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing

Table 1

AQL LEVELS ON FUNCTIONALITY VERSUS BOARD REWORK RATES

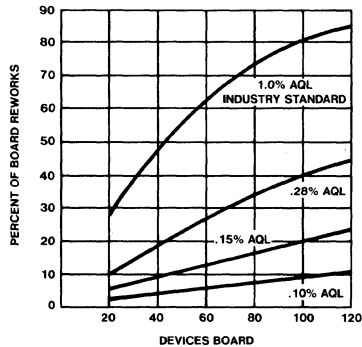


Figure 2

manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been pre-conditioned to eliminate the early failures. Each customer must choose the most cost-effective

RELATIVE FAILURE RATE VERSUS TIME

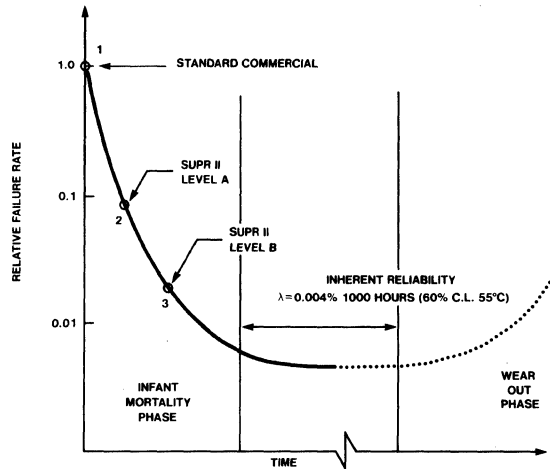


Figure 3

method for his particular business. A considerable number of the reliability defects which cause early failures are elimi-

nated by the manufacturing control and pre-conditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 3.

		ANALOG	
		Plastic	Ceramic Metal Can
HOT OPENS	100°C	.015%	-
FUNCTIONALITY (NOTE 1)	25°C	0.10	0.10
	HIGH	0.15	0.15
D.C. PARAMETRIC TEMPERATURE	25°C	0.15	0.15
	OVER	0.40	0.40
A.C. PARAMETRIC	25°C	0.65	0.65
MECHANICAL	MAJOR	0.25	0.25
	MINOR	1.0	1.0
SEAL TEST (CERAMIC METAL CAN ONLY)	FINE LEAK 1 x 10 ⁻⁷ cc/s	N/A	1.0
	GROSS LEAK 1 x 10 ⁻⁵ cc/s	N/A	0.65

NOTE

1. To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses attention on tightened AQL's on functionality. For analog devices, D.C. parameters, such as input current and offset voltages, tend to be more critical to system operation than for logic devices. A 0.25% AQL is therefore offered on analog D.C. parameters, with the realization that careful attention must be paid to establishing correlation at the customer's incoming inspection.

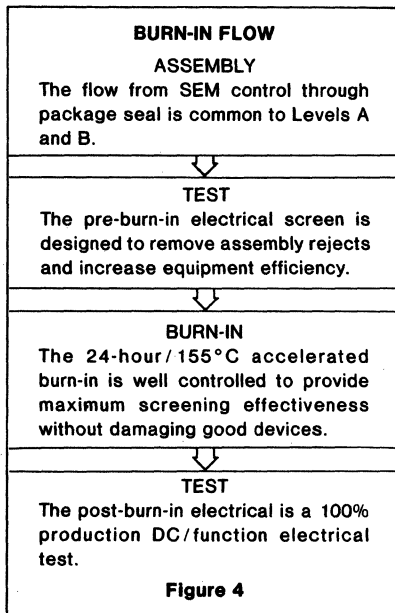
Table 2 SUPRA II AQL GUARANTEE

Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.



Marking Format

Product processed to the SUPR II manufacturing flow can be identified by an SA for Level A, and an SB for the Level B burn-in option.

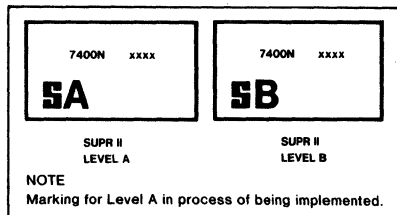
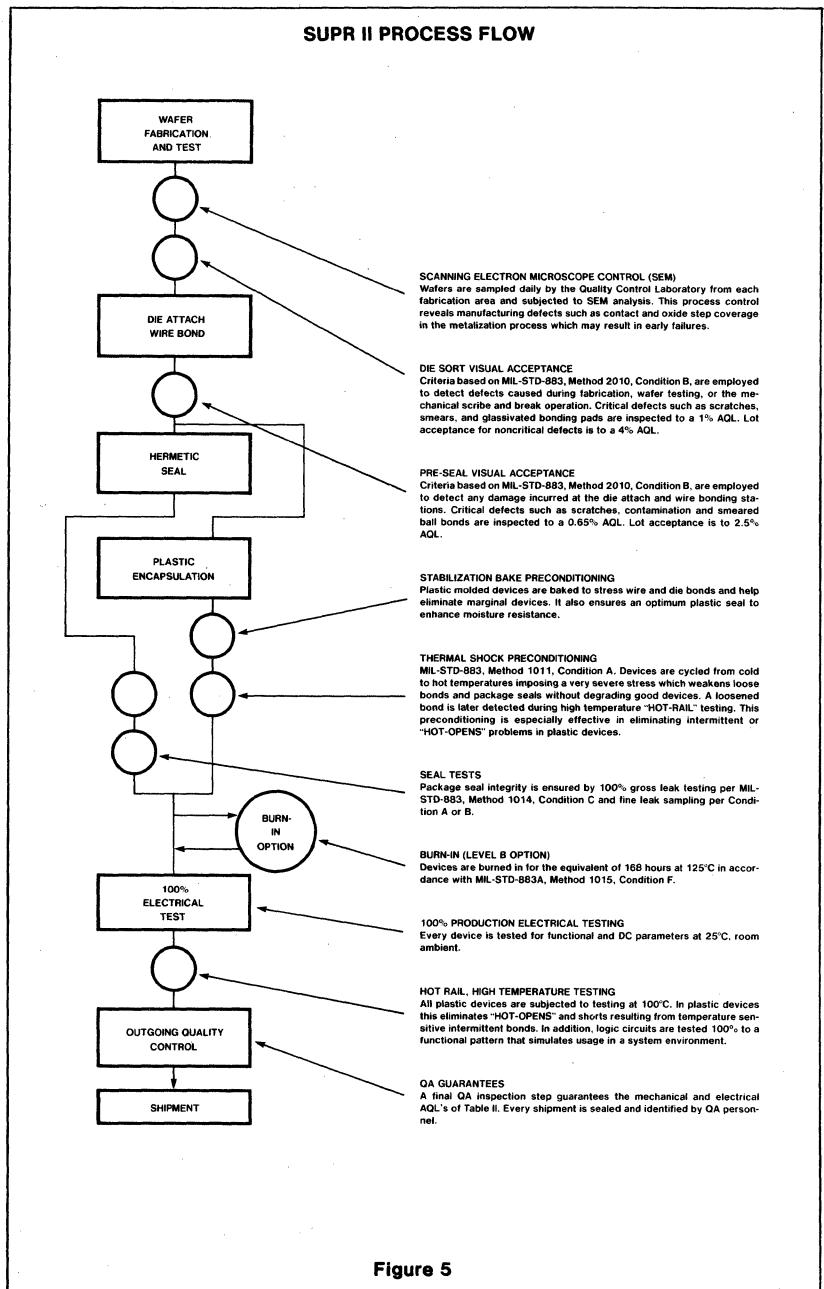


Figure 5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic, and MOS) may follow slightly different procedures dictated by the specific device characteristics.



**SURE II/883B
RELIABILITY PROGRAM**

Definition

Signetics is recognized as a manufacturer of reliable integrated circuits. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The

1978 SURE II/883B Reliability Program contains minor changes to the 1975 SURE II/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-SD-883B, Method 5005.4 and MIL-M-3851OD). The SURE II/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

For more detailed information regarding the SURE II program, refer to Section 11 of the 1979 Signetics Analog Applications Manual.

ANALOG CROSS REFERENCE

Manufacturer	SIGNETICS	AMD	FAIRCHILD	INTEL	MOTOROLA	NATIONAL	T.I.
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TEMPERATURE RANGE CROSS REFERENCE

Commercial	NE	C	C	—	14, 34, 86	3, 86, 88	72, 74, 75
Military	SE	M	M	M	15, 35, 96	1, 96, 78	52, 54, 55

PACKAGE CROSS REFERENCE

Hermetic DIP	F-FE	D	D	C, D	L	D	J
Molded DIP	N	P	P	P	P ₂	N	N
Mini-molded DIP	N	T	T	—	P ₁	N	P
Metal can	H	H	H	—	G, R	H	L

PART NUMBER CROSS REFERENCES

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
AD741CN	μA741CN	CA555F	SE555F	DS8880J	DS8880F
AD559JD	MC1408-8F	CA555T	SE555H	DS8880N	DS8880N
AD559K	MC1408-8F	CA723CE	μA723CN	LM111D	LM111F
AD559KD	MC1408-8F	CA723CT	μA723CH	LM111H	LM111H
AD559S	MC1508-8F	CA723E	μA723N	LM111J	LM111F
AD559SD	MC1508-8F	CA723T	μA723H	LM111L	LM111H
AM555DC	NE555F	CA741CE	μA741CN	LM119D	LM119F
AM555DM	SE555F	CA741CF	μA741CFE	LM119H	LM119H
AM555HC	NE555H	CA741F	μA741FE	LM119J	LM119F
AM555HM	SE555H	CA747CF	μA747CF	LM124D	LM124F
AM555TC	NE555N	CA747CT	μA747CH	LM124J	LM124F
AM723DC	μA723CF	CA747F	μA747F	LM139D	LM139F
AM723DM	μA723F	CA747T	μA747H	LM139J	LM139F
AM723HC	μA723CH	CA748CE	μA748CN	LM158H	LM158H
AM723HM	μA723H	CA748CF	μA748CF	LM158JG	LM158FE
AM741DC	μA741CFE	CA748F	μA748F	LM158L	LM158H
AM741DM	μA741FE	CA1458E	MC1458N	LM161D	SE529F
AM747DC	μA747CF	CA1458F	MC1458FE	LM161H	SE529H
AM747DM	μA747F	CA1458T	MC1458H	LM161J	SE529F
AM747HC	μA747CH	CA1558T	MC1558H	LM193L	LM193H
AM747HM	μA747H	CA3081E	CA3081N	1LM211D	LM211F
AM748DC	μA748CF	CA3082E	CA3082N	LM211H	LM211H
AM748DM	μA748F	CA3183E	CA3183N	LM211J	LM211F
AMLM111H	LM111H	DM7820AJ	DS7820AF	LM219D	LM219F
AMLM211D	LM211F	DM7820J	DS7820F	LM219H	LM219H
AMLM211H	LM211H	DM7830J	DS7830F	LM219J	LM219F
AMLM311D	LM311F	DM7880J	DS7880F	LM224D	LM224F
AMLM311H	LM311H	DM8820AJ	DS8820AF	LM224J	LM224F
CA111F	LM111F	DM8820AN	DS8820AN	LM224N	LM224N
CA111T	LM111H	DM8820J	DS8820F	LM239D	LM239F
CA124F	LM124F	DM8820N	DS8820N	LM239J	LM239F
CA139AF	LM139AF	DM8830J	DS8830F	LM239N	LM239N
CA139F	LM139F	DM8830N	DS8830N	LM258H	LM238H
CA211F	LM211F	DM8880J	DS8880F	LM258JG	LM258FE
CA211T	LM211H	DM8880N	DS8880N	LM258L	LM258H
CA224F	LM224F	DS1488J	MC1488F	LM258P	LM258N
CA239AF	LM239F	DS1489AJ	MC1489AF	LM293L	LM293H
CA239F	LM239F	DS1489J	MC1489F	LM293P	LM293N
CA301AF	LM301AFE	DS7820AJ	DS7820AF	LM301AJG	LM301AFE
CA311F	LM311F	DS7820J	DS7820F	LM311D	LM311F
CA311T	LM311H	DS7830J	DS7830F	LM311H	LM311H
CA324E	LM324N	DS7880J	DS7880F	LM311J	LM311F
CA324F	LM324F	DS8820J	DS8820F	LM311J-14	LM311F
CA339E	LM339N	DS8820AJ	DS8820AF	LM311JG	LM311FE
CA339F	LM339F	DS8820AN	DS8820AN	LM311L	LM311H
CA555CE	NE555N	DS8820N	DS8820N	LM311N	LM311N
CA555CF	NE555F	DS8830J	DS8830F	LM311P	LM311N
CA555CT	NE555H	DS8830N	DS8830N	LM319D	LM319F

PART NUMBER CROSS REFERENCES (Cont'd)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
LM319H	LM319H	LM748J	μA748F	MC1723G	μA723H
LM319J	LM319F	LM1458H	MC1458H	MC1723L	μA723F
LM319N	LM319N	LM1458J	MC1458FE	MC1733CG	μA733CH
LM324J	LM324F	LM1458N	MC1458N	MC1733CL	μA733CF
LM324N	LM324N	LM1496H	MC1496H	MC1733CP	μA733CN
LM339J	LM339F	LM1496J	MC1496F	MC1733G	μA733H
LM339N	LM339N	LM1496N	MC1496N	MC1733L	μA733F
LM358H	LM358H	LM1558H	MC1558H	MC1741CP1	μA741CN
LM358JG	LM358FE	LM1558J	MC1558FE	MC1741CU	μA741CFE
LM358L	LM358H	LM1596H	MC1596H	MC1741SCG	NE535H
LM358N	LM358N	LM1596J	MC1596F	MC1741SCP1	NE535N
LM358P	LM358N	LM2901J	LM2901F	MC1741SCU	NE535FE
LM361D	NE529F	LM2901N	LM2901N	MC1741SG	SE535H
LM361H	NE529H	LM2902J	LM2902F	MC1741SU	SE535FE
LM361J	NE529F	LM2902N	LM2902N	MC1741U	SE535FE
LM361N	NE529N	LM2903L	LM2903H	MC1747CG	μA747CH
LM381N	LM381N	LM2903N	LM2903N	MC1747CL	μA747CF
LM382N	LM382N	LM2903P	LM2903N	MC1747CP2	μA747CN
LM387N	LM387N	MC1408L6	MC1408-6F	MC1747G	μA747H
LM393H	LM393H	MC1408L7	MC1408-7F	MC1747L	μA747F
LM393L	LM393H	MC1408L8	MC1408-8F	MC1748CP1	μA748CN
LM393N	LM393N	MC1408P6	MC1408-6N	MC1748G	μA748H
LM393P	LM393N	MC1408P7	MC1408-7N	MC3302L	MC3302F
LM555CH	NE555H	MC1408P8	MC1408-8N	MC3302P	MC3302N
LM555CN	NE555N	MC1411P	ULN2001N	MC3456L	NE556F
LM555H	SE555H	MC1416P	ULN2004N	MC3456P	NE556N
LM556CD	NE556F	MC1455G	NE555H	MC3556L	SE556F
LM556CJ	NE556F	MC1455P1	NE555N	MC75107L	75S107F
LM556CN	NE556N	MC1455U	NE555FE	MC75107P	75S107N
LM556D	SE556F	MC1458CP1	MC1456N	MC75108L	75S108F
LM556J	SE556F	MC1458CU	MC1456FE	MC75108P	75S108N
LM565CH	NE565H	MC1456P1	MC1456N	MLM111G	LM111H
LM565CN	NE565N	MC1456U	MC1456FE	MLM111L	LM111F
LM565H	SE565H	MC1458CG	MC1458H	MLM111U	LM111FE
LM566CH	NE566H	MC1458CL	MC1458F	MLM124L	LM124F
LM566CN	NE566N	MC1458CP1	MC1458N	MLM139AL	LM139AF
LM566H	SE566H	MC1458CU	MC1458FE	MLM139L	LM139F
LM567H	SE567H	MC1458G	MC1458H	MLM158G	LM158H
LM567CN	NE567N	MC1458JG	MC1458FE	MLM158U	LM158FE
LM567H	SE567H	MC1458P	MC1458N	MLM211G	LM211H
LM723CD	μA723CF	MC1458P1	MC1458N	MLM211L	LM211F
LM723CH	μA723CH	MC1458SG	NE5535H	MLM211U	LM211FE
LM723CJ	μA723CF	MC1458SL	NE5535F	MLM224L	LM224F
LM723CN	μA723CN	MC1458SP1	NE5535N	MLM224P	LM224N
LM723D	μA723F	MC1458U	MC1458FE	MLM239AL	LM239AF
LM723H	μA723H	MC1488L	MC1488F	MLM239AP	LM239AN
LM723J	μA723F	MC1489AL	MC1489AF	MLM239L	LM239F
LM723N	μA723N	MC1489L	MC1489F	MLM239P	LM239N
LM733CD	μA733CF	MC1496G	MC1496H	MLM258G	LM258H
LM733CH	μA733CH	MC1496L	MC1496F	MLM258P1	LM258N
LM733CJ	μA733CF	MC1496P	MC1496N	MLM258U	LM258FE
LM733CN	μA733CN	MC1508L8	MC1508-8F	MLM301AP1	LM301AN
LM733D	μA733F	MC1555G	SE555H	MLM301AU	LM301AFE
LM733H	μA733H	MC1555U	SE555FE	MLM311G	LM311H
LM733T	μA733F	MC1556U	MC1556FE	MLM311L	LM311F
LM741CJ	μA741CFE	MC1558G	MC1558H	MLM311P1	LM311N
LM741CN	μA741CN	MC1558JG	MC1558FE	MLM311U	LM311FE
LM747CD	μA747CF	MC1558SG	SE5535H	MLM324L	LM324F
LM747CH	μA747CH	MC1558SL	SE5535F	MLM324P	LM324N
LM747CJ	μA747CF	MC1558U	MC1558FE	MLM339AL	LM339AF
LM747D	μA747F	MC1596G	MC1596H	MLM339AP	LM339AN
LM747H	μA747H	MC1596L	MC1596F	MLM339L	LM339F
LM747J	μA747F	MC1723CF	μA723CH	MLM339P	LM339N
LM748CJ	μA748CF	MC1723CL	μA723CF	MLM358G	LM358H
LM748CN	μA748CN	MC1723CP	μA723CN	MLM358P1	LM358N

PART NUMBER CROSS REFERENCES (Cont'd)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
MLM358U	LM358FE	μA0802DM-1	MC1508-8F	SN72747J	μA747CF
MLM565CP	NE565N	μA0802PC-1	MC1408-8N	SN72747L	μA747CH
MLM2901P	LM2901N	μA0802PC-2	MC1408-7N	SN72747N	μA747CN
MLM2902P	LM2902N	μA0802PC-3	MC1408-6N	SN72748J	μA748CF
μA111HM	LM111H	μA1458HC	MC1458H	SN72748P	μA748CN
μA124DM	LM124F	μA1458TC	MC1458N	SN72771N	MC1458N
μA224DM	LM224F	μA1558HM	MC1558H	SN75107AT	75S107F
μA301ANC	LM301AN	μA2901PC	LM2901N	SN75107AN	75S107N
μA311HC	LM311H	μA2902PC	LM2902N	SN75108AT	75S108F
μA311TC	LM311N	NE555JG	NE555FE	SN75108AN	75S108N
μA324DC	LM324F	NE555L	NE555H	SN75182J	DS8820F
μA324PC	LM324N	NE555P	NE555N	SN75182N	DS8820N
μA339ADC	LM339AF	NE5592G	NE592H	SN75183J	DS8830F
μA339DC	LM339F	NE592L	NE592F	SN75183N	DS8830N
μA339PC	LM339N	RC723D	μA723CF	SN75188J	MC1488F
μA555HC	NE555H	RC723T	μA723CH	SN75188N	MC1488N
μA555HM	SE555H	RC733D	μA733CF	SN75189AT	MC1489AF
μA555TC	NE555N	RC733T	μA733CH	SN75189AN	MC1489AN
μA556DC	NE556F	RC741DN	μA741CN	SN75189J	MC1489F
μA556DM	SE556F	RC747D	μA747CF	SN75189N	MC1489N
μA556PC	NE556N	RC747T	μA747CH	SN75207J	75S207F
μA723CJ	μA723CF	RC1458DN	MC1458N	SN75207N	75S207N
μA723CL	μA723CH	RC1458T	MC1458H	SN75208J	75S208F
μA723CN	μA723CN	RC1488DC	MC1488F	SN75208N	75S208N
μA723DC	μA723CF	RC1489ADC	MC1489AF	TBB0747	μA747CH
μA723DM	μA723F	RC1489DC	MC1489F	TBB0748B	μA748CN
μA723HC	μA723CH	SE555JG	SE555FE	TBB1458	MC1458H
μA723HM	μA723H	SE555L	SE555H	TBB1458B	MC1458N
μA723MJ	μA723F	SE592G	SE592H	TBC0747	μA747H
μA723ML	μA723H	SE592L	SE592F	TBC1458	MC1558H
μA723PC	μA723CN	SFC2111M	LM111H	TDB0555	NE555H
μA733CJ	μA733CF	SFC2211	LM211H	TDB0555B	NE555N
μA733CL	μA733CH	SFC2301ADC	LM301AN	TDB0556A	NE556N
μA733CN	μA733CN	SFC2311	LM311H	TDB0723	μA723CH
μA733DC	μA733CF	SFC2741DC	μA741CN	TDB0723A	μA723CN
μA733DM	μA733F	SFC2741EC	μA741CN	TDC0555	SE555H
μA733HC	μA733CH	SFC2741EM	μA741N	TDC0723	μA723H
μA733HM	μA733H	SFC2748DC	μA748CN	ULN2001A	ULN2001N
μA733MJ	μA733F	SN52555L	SE555H	ULN2003A	ULN2003N
μA733ML	μA733H	SN52558L	MC1558H	ULN2004A	ULN2004N
μA740HC	μA740CH	SN52723J	μA723F	556CJ	NE556CN
μA741CJG	μA741CFE	SN52723L	μA723H	723BE	μA723H
μA741CP	μA741CN	SN52733J	μA733F	723CE	μA723CH
μA741MJG	μA741FE	SN52733L	μA733H	723CT	μA723CN
μA741TC	μA741CN	SN52747J	μA747F	723CL	μA723CF
μA747CJ	μA747CF	SN52747L	μA747H	733BE	μA733H
μA747CL	μA747CH	SN52748J	μA748F	733CE	μA733CH
μA747CN	μA747CN	SN55182J	DS7820F	733CJ	μA733CN
μA747DC	μA747CF	SN55182N	DS7820N	747BE	μA747H
μA747DM	μA747F	SN55183J	DS7830F	747BL	μA747F
μA747HC	μA747CH	SN55183N	DS7830N	747CE	μA747CH
μA747HM	μA747H	SN72301AP	LM301AN	747CJ	μA747CN
μA747MJ	μA747F	SN72311J	LM311F	747CL	μA747CF
μA747ML	μA747H	SN72311L	LM311H	748BL	μA748F
μA747PC	μA747CN	SN72311P	LM311N	748CL	μA748CF
μA748CJ	μA748CF	SN72555L	NE555H	1458CE	MC1458H
μA748CP	μA748CN	SN72555P	NE555N	1458CP	MC1458N
μA748DC	μA748CF	SN72558L	MC1458H	1458E	MC1458H
μA748DM	μA748F	SN72558P	MC1458N	1458P	MC1458N
μA748MJ	μA748F	SN72723L	μA723CH	1558E	MC1558H
μA748TC	μA748CN	SN72723N	μA723CN	2740CE	μA740CH
μA796HC	MC1496H	SN72733J	μA733CF	9665DC	ULN2001F
μA0802DC-1	MC1408-8F	SN72733L	μA733CH	0665PC	ULN2001N
μA0802DC-2	MC1408-7F	SN72733N	μA733CN	UA3089N	CA3089N
μA0802DC-3	MC1408-6F	SN72741P	μA741CN	UA3089	CA3089N

PART NUMBER CROSS REFERENCES (Cont'd)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
UA760HM	NE527H	UA758PC	UA758N	SN7512N	NA733N
UA760DC	NE527N	UA798HM	LM158H	SN76689N	CA3089N
UA798TC	NE532N	UA739PC	LM387N	ULN2210A	UA758N
UA740HM	NE536N	UA739PC	LM382N	ULN2244	μA758N
UA556PC	NE556N	UA796PC	MC1496N	UA740HC	μA740CH
UA0801	DAC-08N	UA760HC	NE529N		
UA0801A	DAC-08AN	SN7512L	NA733CH		

SECTION I **OPERATIONAL AMPLIFIERS**

Section 1—OPERATIONAL AMPLIFIERS

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NE/SE5533/5533A	Single and Dual Low Noise Operational Amplifier	104
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NE/SE5539	Ultra High Frequency Operational Amplifier	109
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μ A741/741C/SA741C	General Purpose Operational Amplifier	119
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OPERATIONAL AMPLIFIERS DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Bandwidth

The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, $\mu\text{V}/\mu\text{s}$ or other convenient units.

Hold-Mode Feed Through

The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/ μs).

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Threshold

Level shall be defined as that level which causes the switch control to change state.

Average Input Offset Current T⁰ coeff.

The change in input offset current divided by the change to ambient temperature producing it.

Average Input Offset Voltage T⁰ coeff.

The change in input offset voltage divided by the change in ambient temperature producing it.

Common Mode Input Resistance

The resistance looking into both inputs, with inputs tied together.

Common Mode Rejection Ratio (CMRR)

The ratio of the change of input offset voltage to the input common mode voltage change producing it.

Full Power Bandwidth

The maximum frequency at which the full sinewave output might be obtained.

Input Bias Current

The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

OPERATIONAL AMPLIFIERS DEFINITIONS (Cont'd)

Input Capacitance

The capacitance looking into either input terminal with the other grounded.

Input Current

The current into an input terminal.

Input Noise Voltage

The square root of the mean square narrow-band noise voltage referred to the input.

Input Offset Current

The difference in the currents into the two input terminals with the output at zero volts.

Input Offset Voltage

That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

Input Resistance

The resistance looking into either input terminal with the other grounded.

Input Voltage Range

The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

Large-Signal Voltage Gain

The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

Output Resistance

The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions

at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

Output Short-Circuit Current

The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Output Voltage Swing

The peak output swing, referred to zero, that can be obtained.

Power Consumption

The dc power required to operate the amplifier with the output at zero and with the output at zero and with no load current.

Power Supply Rejection Ratio

The ratio of the change in input offset voltage to the change in supply voltages producing it.

Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate

The maximum rate of change of output voltage under large signal condition.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Temperature Stability of Voltage Gain

The maximum variation of the voltage gain over the specified temperature range.

NOTE

Refer to Section 3 of the 1979 Analog Applications Manual for an in depth explanation of Operational Amplifiers and their applications

Device #	Complexity	Temp. Range	Max. Input Voltage		Max. Input Current		Min. A VOL V/mV	Typ. BW $A_V=1$ MHz	Typ. Slew Rate V/ μ s	Diff. Inp. Volt. V	Typical Common Mode Rej. Volt		Typ. PSRR dB	Supply Volt. Typ.		Outp. Curr. mA	Max Supply Curr. mA	Min. Outp. Volt. Swing V	Int. Compensation	Input Noise Volt. N/Hz	Packages
			Offset mV	Drift μ V/ $^{\circ}$ C	Offset nA	Bias nA					Ratio dB	Range V		Min. V	Max. V						
NE536	Sing.	Ind.	30●	30●	5pA■	0.1▲	25	1.0	6.0	± 30	80	± 11	80	± 6	± 20	5.0	8.0▲	± 12	yes		H
SU536	Sing.	Ext.	30	20●	5pA■	3.0	50	1.0	6.0	± 30	80	± 11	86	± 6	± 18	5.0	5.5▲	± 12	yes		H
NE530	Sing.	Ind.	6.0	6●	80	200	25	3.0	35	± 30	90	± 13	70	± 15	± 18	25▲	3.0	± 12	yes		H,N,FE
SE530	Sing.	Ind.	3.0	15	20	100	25	3.0	35	± 30	90	± 13	70	± 15	± 18	25▲	3.0	± 12	yes		H,N,FE
SE538	Sing.	Mil.	3.0	15	20	100	25	6.0	60	± 30	90	± 13	70	± 15	± 22	25▲	3.6	± 12	yes		H,N,FE
NE538	Sing.	Ind.	6.0	6●	80	200	25	6.0	60	± 30	90	± 13	70	± 15	± 18	25▲	2.2●	± 12	yes		H,N,FE
NE5534/A	Sing.	Ext.	4.0▲		300▲	1500▲	30▲	10.0	13	± 5	100	± 13	100	± 3	± 22	38■	6.5▲	± 12	yes	4.5	H,N,FE
SE5534/A	Sing.	Mil.	3.0		500	1500	25	10.0	13	± 5	100	± 13	100	± 3	± 22	38■	9.0	± 12	yes	4.5	H,N,FE
μ A740C	Sing.	Ind.	30●		0.06●	10.0	500●	1.0	6.0	± 30	80	± 12	80	± 5	± 22	5.0	8.0▲	± 12	yes		H
μ A741	Sing.	Mil.	6.0		500	1500	25	1.0	0.5	± 30	90	± 13	100	± 3	± 22	5.0	2.5	± 12	yes		N,FE
μ A741C	Sing.	Ind.	7.5		300	800	15	1.0	0.5	± 30	90	± 13	100	± 3	± 18	5.0	2.8▲	± 12	yes		N,FE
μ A748	Sing.	Mil.	6.0		500	1500	25	1.0	0.5	± 30	90	± 13	90	± 3	± 22	5.0	2.8	± 12	no		N,F
μ A748C	Sing.	Ind.	7.5		300	800	25	1.0	0.5	± 30	90	± 13	90	± 3	± 18	5.0	2.8	± 12	no		N,F
LM158	Dual	Mil.	7.0	7●	100	300	25	1.0		32	70	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		H
LM258	Dual	Ext.	9.0	7●	150	500	15	1.0		32	65	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		H,N,FE
LM358	Dual	Ind.	9.0	7●	150	500	15	1.0		32	65	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		H,N,FE
MC1458	Dual	Ind.	7.5		300	800	15	1.0	0.8	± 30	90	± 13	90	± 3	± 18	5.0	5.6▲	± 12	yes		H,N,FE
MC1558	Dual	Mil.	6.0		500	1500	25	1.0	0.5	± 30	90	± 13	90	± 3	± 22	5.0	5.0▲	± 12	yes		H,N,FE
SA1458	Dual	Ext.	7.5		500	1500	15	1.0	0.8	± 30	90	± 13	90	± 3	± 18	5.0	5.0▲	± 12	yes		N
NE532	Dual	Ind.	7.5	7●	150	500	15	1.0		32	70	$V_S-1.5$	100	3	30	40	1.2	V_S-2	yes		H,N,FE
SA532	Dual	Ext.	7.5	7.5●	150	500	15	1.0		32	70	$V_S-1.5$	100	3	30	40	1.2	V_S-2	yes		N
SE532	Dual	Mil.	7.0	7●	100	300	25	1.0		32	70	$V_S-1.5$	100	3	30	40	1.2	V_S-2	yes		H,FE
μ A747	Dual	Mil.	6.0		500	1500	25	1.0	.05	± 30	90	± 13	90	± 3	± 22	5.0	3.3	± 12	yes		F,H,N
μ A747C	Dual	Ind.	7.5		300	800	15	1.0	0.5	± 30	90	± 13	90	± 3	± 18	5.0	3.3	± 12	yes		F,H,N
SE5535	Dual	Mil.	3.0	15	20	100	25	1.0	15	± 30	90	± 13	70	± 3	± 22	5.0	3.3	± 12	yes		H,N
NE5535	Dual	Ind.	6.0	6●	80	200	25	1.0	15	± 30	90	± 13	70	± 3	± 18	5.0	2.0●	± 12	yes		H,N
LM124	Quad	Mil.	7.0	7●	100	300	25	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		F
LM224	Quad	Ext.	9.0	7●	150	500	15	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		F,N
LM324	Quad	Ind.	9.0	7●	150	500	15	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		F,N
SA534	Quad	Ext.	9.0	7●	150	500	15	1.0		32	85	$V_S-1.5$	100	3	30	40	2.0	V_S-2	yes		N,F
LM2902	Quad	Ext.	15.0	7●	200	1000	15	1.0		26	85	$V_S-1.5$	100	3	26	40	2.0	V_S-2	yes		N
SE5538	Dual	Mil.	3.0	15	20	100	25	6.0	60	± 30	90	± 13	70	± 15	± 22	25▲	3.6	± 12	yes		H,N
NE5538	Dual	Ind.	6.0	6●	80	200	25	6.0	60	± 30	90	± 13	70	± 15	± 18	25▲	2.2●	± 12	yes		H,N
SE5530	Dual	Mil.	3.0	15	20	100	25	3.0	35	± 30	90■		70	± 3	± 22		3.6	± 13	yes		H,N
NE5530	Dual	Ind.	6.0	6●	80	200	25	3.0	35	± 30	90■		70	± 3	± 18		2.2	± 13	yes		H,N
NE5532/A	Dual	Ind.	5.0		200	1000	10	10	9	± 5	100		80	± 5	± 22		16	± 15	yes	6	H,FE,N
NE5533/A	Dual	Ind.	5.0		400	2000	15	10	13	± 5	100		80	± 5	± 22		8	± 15	yes	4.5	N,F

NOTES

- Military -55°C - $+125^{\circ}\text{C}$
 Extended -25°C - $+85^{\circ}\text{C}$
 Industrial 0°C - $+70^{\circ}\text{C}$
- Specifications guaranteed over full temperature range unless otherwise indicated by following marks:
 ● Typical over full temperature range ▲ Guaranteed at 25°C ■ Typical at 25°C

SIGNETICS REPLACEMENT STANDARDS

MC1458 DUAL OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	.8	Slew Rate	10 to 60	NE/SE { 5530 5538	Yes		
			V/μ sec	NE { 5532 5532A 5533 5533A	Yes		
	14	Full power out	30 to 300	NE/SE { 5530 5538	Yes		
			kHz	NE { 5532 5532A 5533 5533A	Yes		
	45	Noise	4, 5	NE { 5532 5532A 5533 5533A	Yes		
			nv/√Hz		Yes		
	6	Offset voltage	4	NE { 5532 5532A 5533 5533A	Yes		
			mv		Yes		
	500	Bias current	60 to 150	NE/SE { 5530 5538	Yes		
			na		Yes		
	1	Gain bandwidth	1.5 ↓ 15	NE/SE { 5530 5538	Yes		
			MHz	NE { 5533 5533A 5532 5532A	Yes		
	2,000	Maximum loading	600	NE { 5533 5533A 5532 5532A	Yes		
			OHM		Yes		

SIGNETICS REPLACEMENT STANDARDS

μa741 SINGLE OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS	
					SURE II	SUPR II		
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	0.5	Slew rate	10 to 600	NE/SE { 530 538 5534 5534A	Yes		*Not pin for pin replacement.	
			V/μ sec		NE 5539*	Yes		Yes
	10	Full power out	300 to 350,000	NE/SE { 530 538 5534 5534A	Yes			*Not pin for pin replacement.
			kHz		NE 5539*	Yes		
	45	Noise	4, 5	NE/SE { 5534 5534A	Yes	Yes		
			nv/√Hz		NE/SE { 5534 5534A	Yes		
	5	Offset voltage	4	NE/SE { 5534 5534A	Yes	Yes		
			mv		NE/SE { 5534 5534A	Yes		
	500	Bias current	60 to 150	NE/SE { 530 538	Yes			
			na		NE/SE { 530 538	Yes		
	1	Gain bandwidth	1.5 ↓ 1200	NE/SE { 530 538 5534 5534A	Yes			*Not pin for pin replacement.
			MHz		NE 5539*	Yes		
2,000	Maximum loading	600	NE/SE { 5534 5534A	Yes	Yes			
		OHM		NE/SE { 5534 5534A	Yes		Yes	

DESCRIPTION

The LF355 and LF356 operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

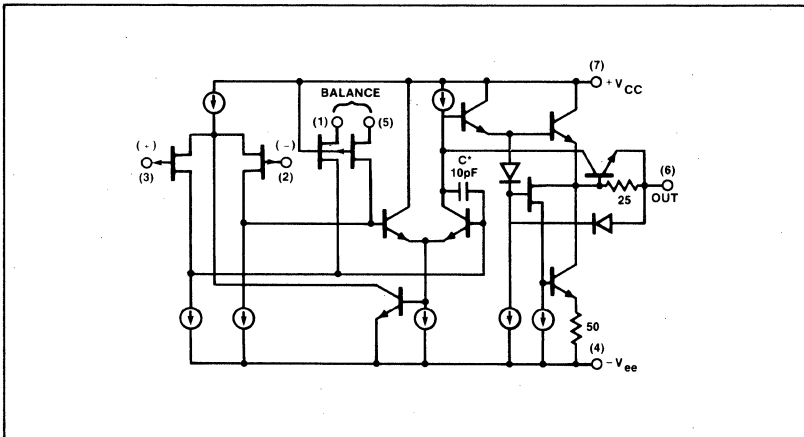
COMMON FEATURES (TYPICAL)

- Low input bias current 50pA
- Low input offset current 10pA
- High input impedance $10^{12}\Omega$
- Low input offset voltage 3mV
- Low V_{OS} temperature drift $5\mu V/^{\circ}C$
- Low input noise current $0.01pA/\sqrt{Hz}$

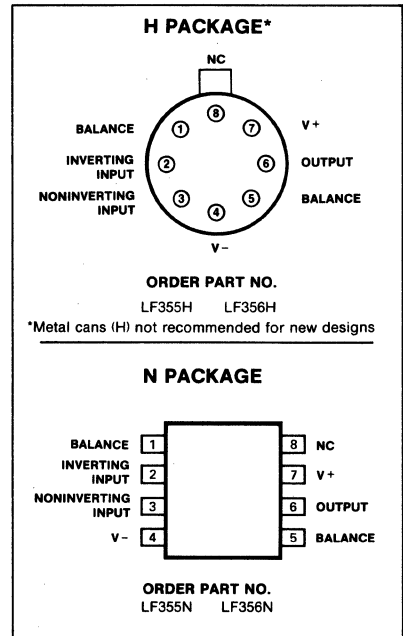
APPLICATIONS

- Precision high speed integrators
- Fast A/D, D/A converters
- High impedance buffers
- Wideband, low noise, low drift amplifier

EQUIVALENT SCHEMATIC



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation	500	mW
Operating temperature range	0 to +70	$^{\circ}C$
T_j (Max)	100	$^{\circ}C$
Input voltage range ¹	± 20	V
Output short circuit duration	Continuous	
Storage temperature range	-65 to +150	$^{\circ}C$
Lead temperature (soldering 10 sec.)	300	$^{\circ}C$

NOTE

1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

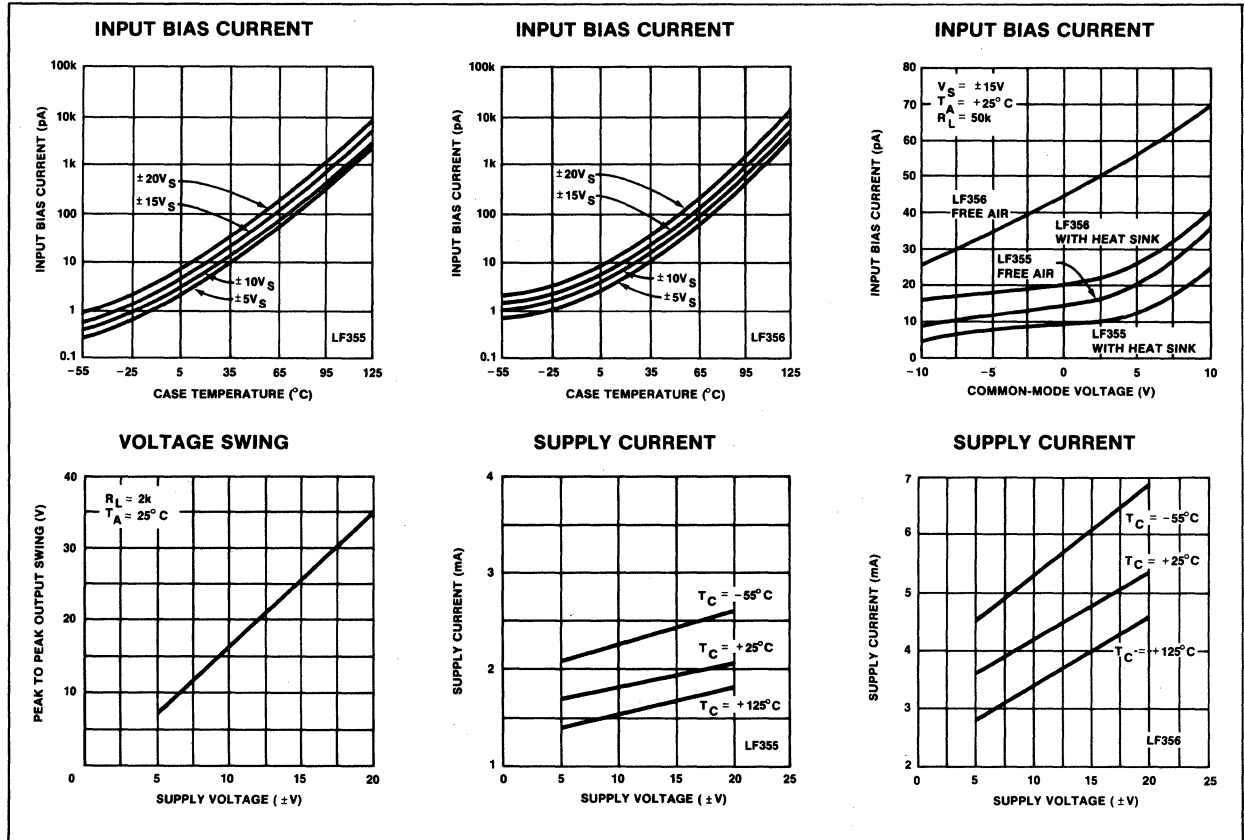
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_s = \pm 15\text{V}$ unless otherwise specified.¹

PARAMETER	TEST CONDITIONS	LF355			LF356			UNIT
		Min	Typ	Max	Min	Typ	Max	
SR Slew rate	$A_v = 1$		5			12		$\text{V}/\mu\text{s}$
GBW Gain bandwidth product			2.5			5		MHz
t_s Settling time ¹ to 0.01%			4			1.5		μs
e_n Equiv. input noise volt.	$R_s = 100\Omega$ $f = 100\text{Hz}$ $f = 1000\text{Hz}$		25 20			15 12		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
i_n Equiv. input noise current	$f = 100\text{Hz}$ $f = 1000\text{Hz}$		0.01 0.01			0.01 0.01		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$
C_{in} Input capacitance			3			3		pF

NOTE

1. Settling time is defined here, for a unity gain inverter connection using $2\text{k}\Omega$ resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

TYPICAL DC PERFORMANCE CHARACTERISTICS



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LF355/356			UNIT
		Min	Typ	Max	
V_{os} Input offset voltage	$R_s = 50\Omega$		3	10 13	mV mV
$\Delta V_{os}/\Delta T$ Avg. TC of input offset voltage	$R_s = 50\Omega$		5		$\mu\text{V}/^\circ\text{C}$
$\Delta\text{TC}/\Delta V_{os}$ Change in average TC ² with V_{os} adjust	$R_s = 50\Omega$		0.5		$\mu\text{V}/^\circ\text{C}$ per mV
I_{os} Input offset current ^{1,3}	$T_J = 25^\circ\text{C}$ $T_J \leq T_{high}$		3	50 2	pA nA
I_B Input bias current ^{1,3}	$T_J = 25^\circ\text{C}$ $T_J \leq T_{high}$		30	200 8	pA nA
R_{IN} Input resistance	$T_J = 25^\circ\text{C}$ $V_s = \pm 15\text{V}$ $V_o = \pm 10\text{V}, R_L = 2\text{k}\Omega$ Over temp.	25	10 ¹²		Ω
A_{VOL} Large signal voltage gain		15	200		V/mV
V_o Output voltage swing	$V_s = \pm 15\text{V}, R_L = 10\text{k}\Omega$ $V_s = \pm 15\text{V}, R_L = 2\text{k}\Omega$	± 12 ± 10	± 13 ± 12		V V
V_{CM} Input common mode Voltage range	$V_s = \pm 15\text{V}$	± 10	+15.1 -12		V V V
CMRR Common-mode rejection ratio		80	100		dB
PSRR Supply volt. rej. ratio ⁴		80	100		dB

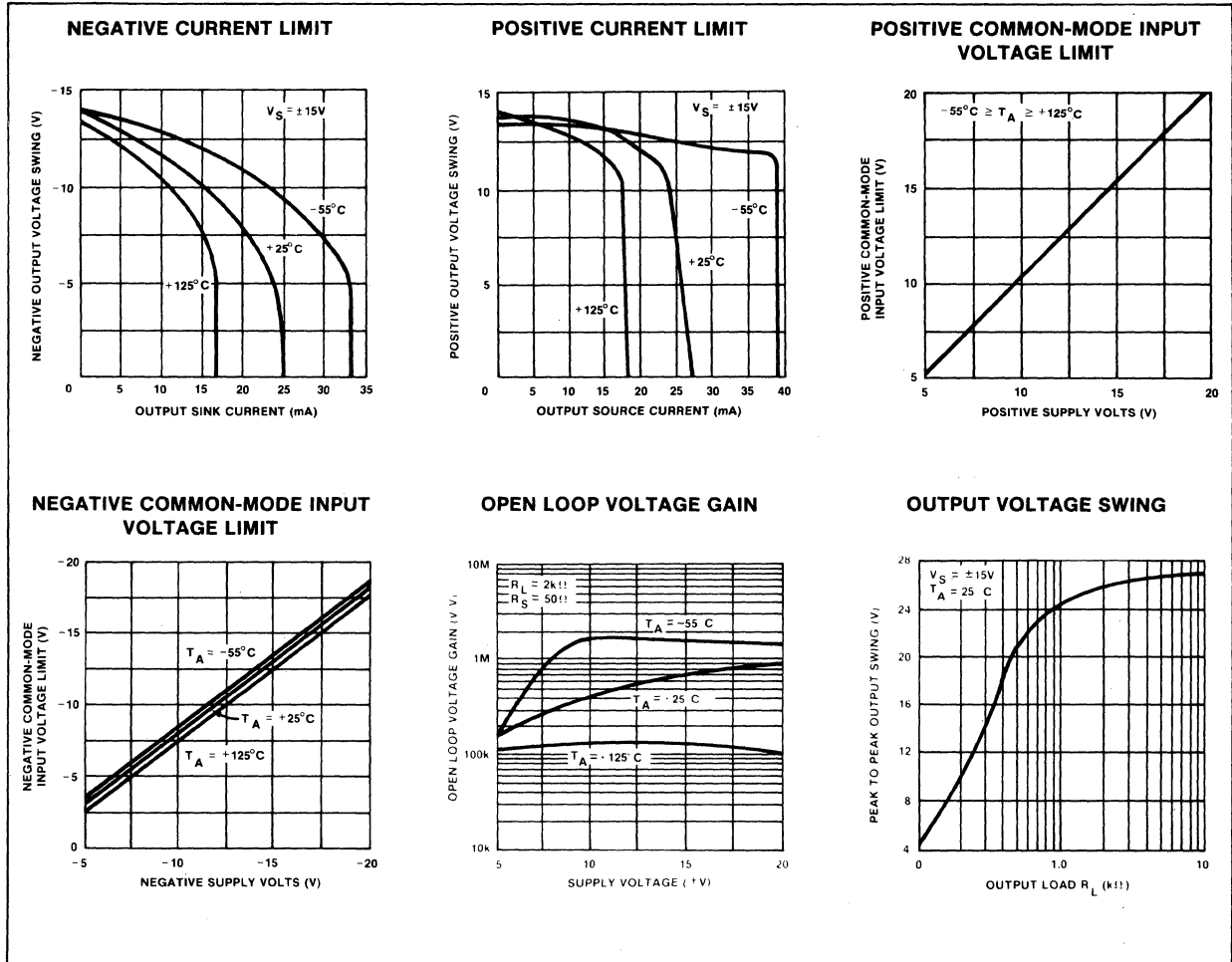
DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_s = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	LF355			LF356			UNIT
	Min	Typ	Max	Min	Typ	Max	
Supply current		2	4		5	10	mA

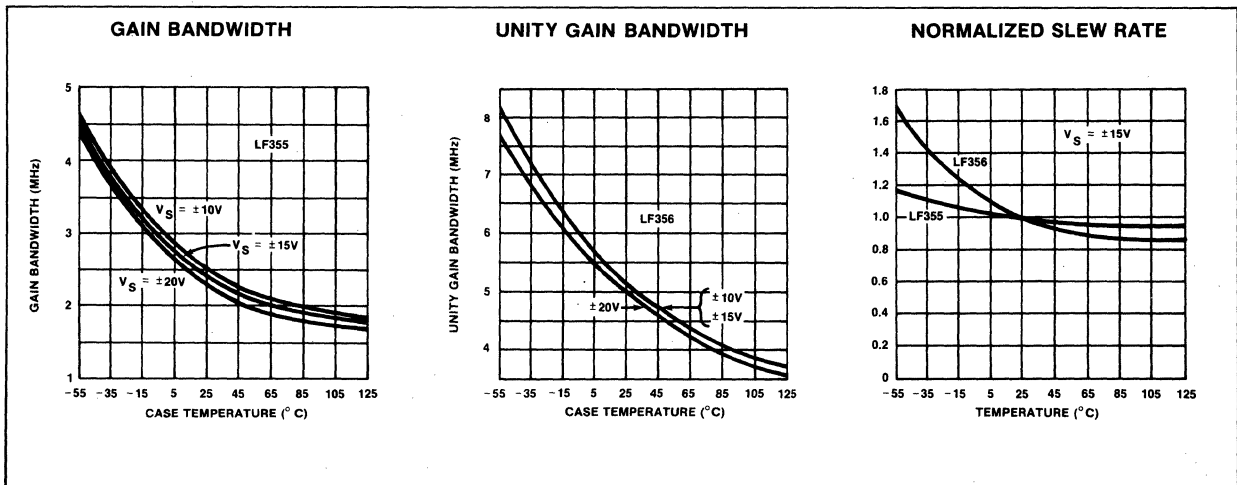
NOTES

- These specifications apply for $V_s = \pm 15\text{V}$ and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$. V_{os} , I_B and I_{os} are measured at $V_{CM} = 0$.
- The Temperature Coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
- The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d . $T_J = T_A + \theta_{JA} P_d$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)

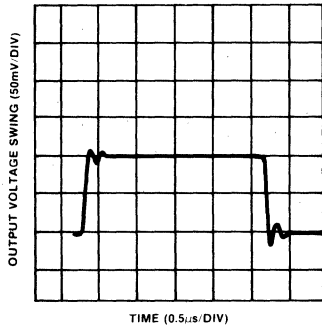


TYPICAL AC PERFORMANCE CHARACTERISTICS

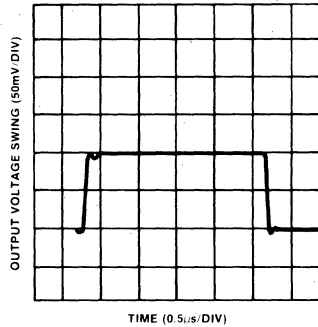


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

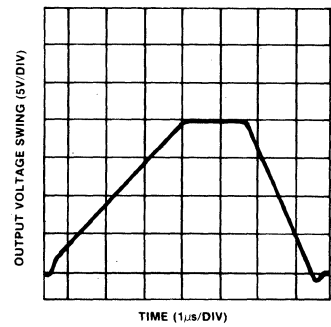
LF355 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



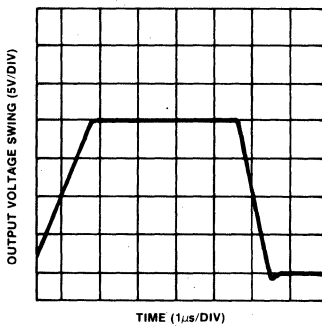
LF356 SMALL SIGNAL PULSE RESPONSE, $A_V = +1$



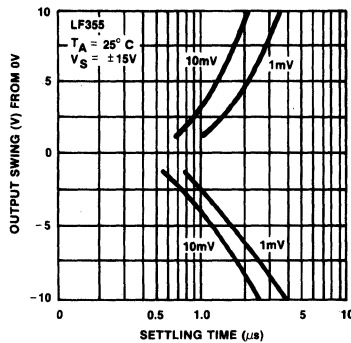
LF355 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



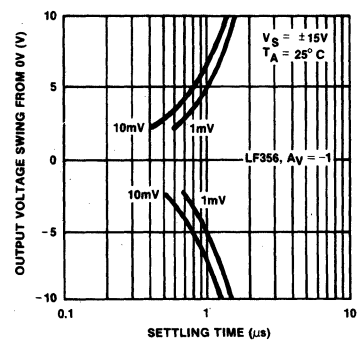
LF356 LARGE SIGNAL PULSE RESPONSE, $A_V = +1$



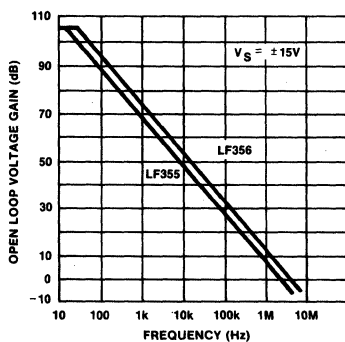
INVERTER SETTLING TIME



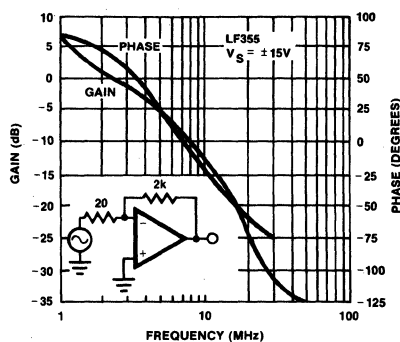
INVERTER SETTLING TIME



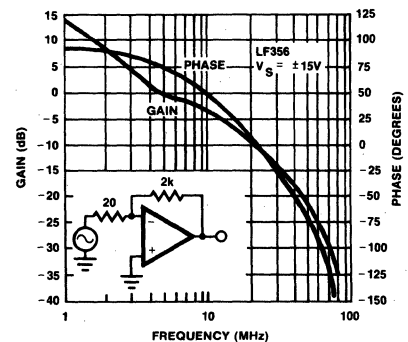
OPEN LOOP FREQUENCY RESPONSE



BODE PLOT

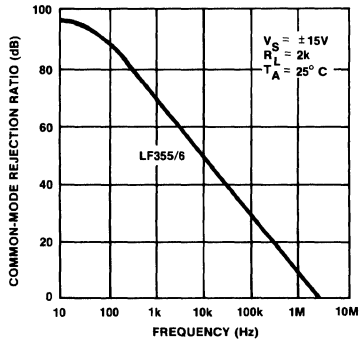


BODE PLOT

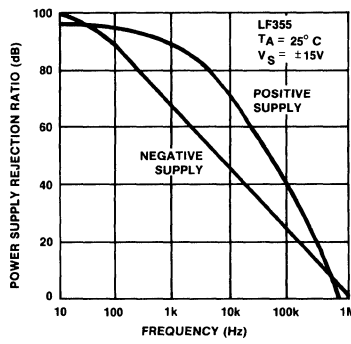


TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

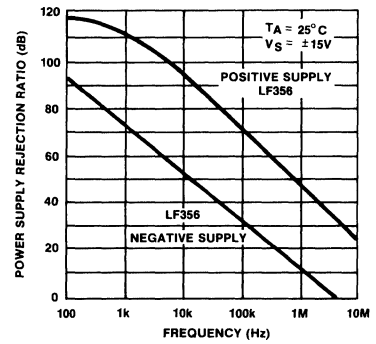
COMMON-MODE REJECTION RATIO



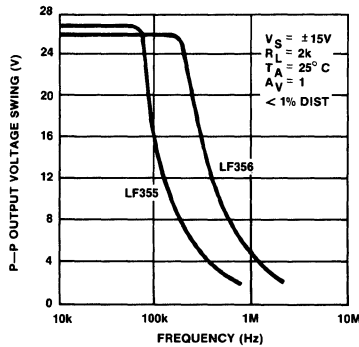
POWER SUPPLY REJECTION RATIO



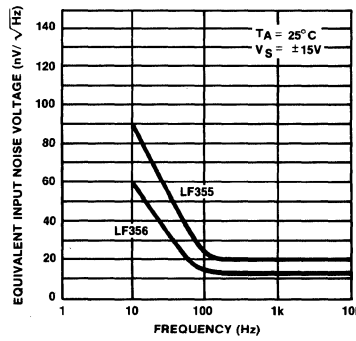
POWER SUPPLY REJECTION RATIO



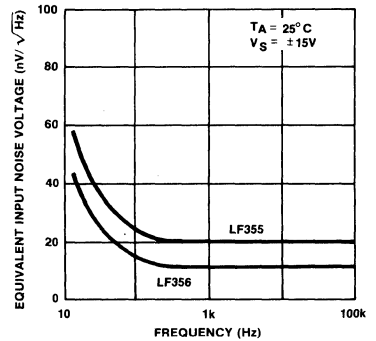
UNDISTORTED OUTPUT VOLTAGE SWING



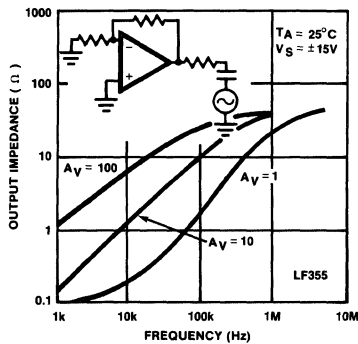
EQUIVALENT INPUT NOISE VOLTAGE



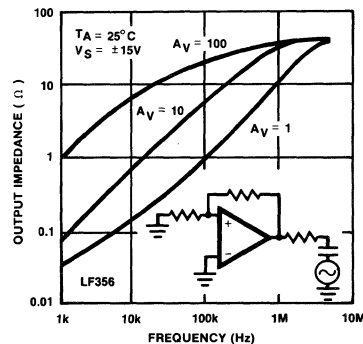
EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



OUTPUT IMPEDANCE

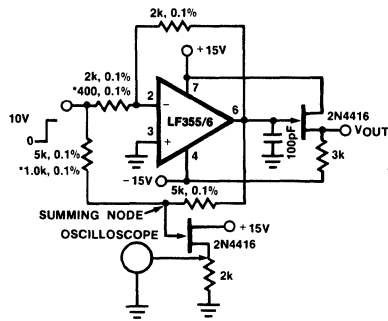


OUTPUT IMPEDANCE



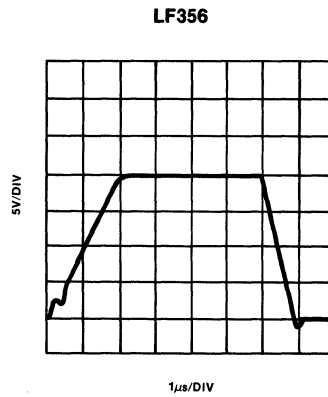
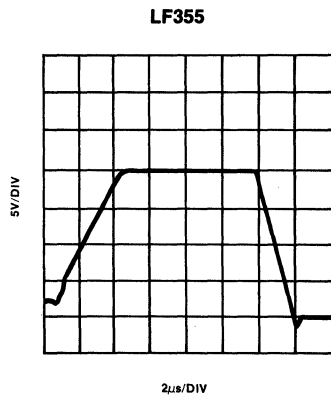
TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

SETTLING TIME TEST CIRCUIT



- Settling time is tested with the LF355/6 connected as unity gain inverter,
- FET used to isolate the probe capacitance
- Output = 10V step

LARGE SIGNAL INVERTER OUTPUT, V_{OUT} (FROM SETTLING TIME CIRCUIT)



APPLICATIONS

The LF355 and LF356 are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit. Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs ex-

ceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore

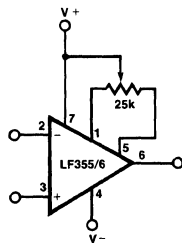
essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

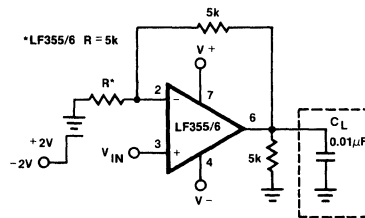
TYPICAL CIRCUIT CONNECTIONS

V_{OS} ADJUSTMENT



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100ppm/°C or less the additional drift with adjust is ≈ 0.5μV/°C/mV of adjustment
- Typical overall drift: 5μV/°C ± (0.5μV/°C/mV of adj.)

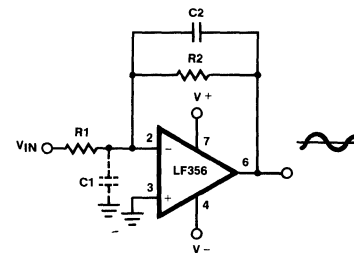
DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. C_L max ≤ 0.01μF.
Overshoot ≤ 20%
Setting time (ts) ≥ 5μs

TYPICAL APPLICATIONS

WIDE BW LOW NOISE, LOW DRIFT AMPLIFIER



- Power BW: $f_{MAX} = \frac{S_r}{2\pi/p} \approx 240kHz$
- Parasitic input capacitance C₁ ≈ (3pF for LF355 and LF356, plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C₂ such that: R₂C₂ ≈ R₁C₁.

TYPICAL APPLICATIONS (Cont'd)

HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER

- $V_{OUT} = \frac{R_3}{R} \left[\frac{2R_2}{R_1} + 1 \right] \Delta V$, $V_- + 2V \leq V_{IN} \text{ Common-Mode} \leq V_+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120dB.

HIGH Q NOTCH FILTER

- $2R_1 = R = 10M\Omega$
- $2C = C_1 = 300pF$
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120Hz$, notch = 55dB, $Q > 180$
- Use LF355 for Δ Low I_B
- Δ Low supply current

HIGH ACCURACY SAMPLE AND HOLD

- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, Cc: additional compensation
- Use LF356 for Δ Fast settling time
- Δ Low V_{OS}

FAST LOGARITHMIC CONVERTER

$$|V_{OUT}| = \left[1 + \frac{R_2}{R} \right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF} R_i} \right] = \log V_i \frac{1}{R_i I_R}$$

$R_2 = 15.71$, $R_1 = 1k$, $0.3\%/^{\circ}C$ (for temperature compensation)

- Dynamic range: $100\mu A \leq I_i \leq 1mA$ (5 decades, $|V_O| = 1V/\text{decades}$)
- Transient response: $3\mu s$ for Δ , = decades
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF356 to minimize quiescent error
- Rr: Tel Labs type Q81 + $0.3\%/^{\circ}C$.

DESCRIPTION

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

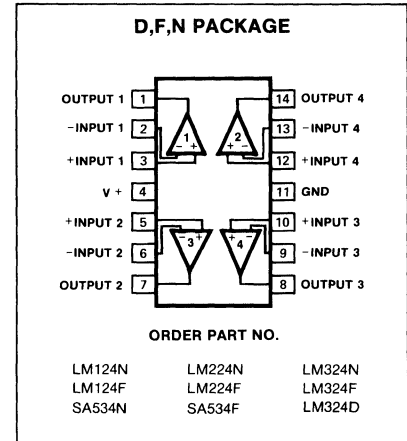
The unity gain cross frequency is temperature compensated.

The input bias current is also temperature compensated.

FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain—(100dB)
- Wide bandwidth (unity gain)—1MHz (temperature compensated)
- Wide power supply range
Single supply—(3Vdc to 30Vdc) or dual supplies—(±1.5Vdc to ±15Vdc)
- Very low supply current drain—essentially independent of supply voltage (1mW/op amp at +5Vdc)
- Low input biasing current—(45nAdc temperature compensated)
- Low input offset voltage—(2mVdc) and offset current—(5nAdc)
- Differential input voltage range equal to the power supply voltage
- Large output voltage—(0Vdc to V+—1.5Vdc swing)
- LM124 Mil std 883A,B,C available

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V+	Supply voltage	32 or ±16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation ¹		
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier ²	Continuous	
	V+ < 15Vdc and T _A = 25°C		
	Input current (V _{IN} < -0.3V) ³	50	mA
	Operating temperature range		
	LM324	0 to +70	°C
	LM224	-25 to +85	°C
	SA534	-40 to +85	°C
	LM124	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM 124/224 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

DC ELECTRICAL CHARACTERISTICS $V+ = 5V, T_A = 25^\circ C$ unless otherwise specified.

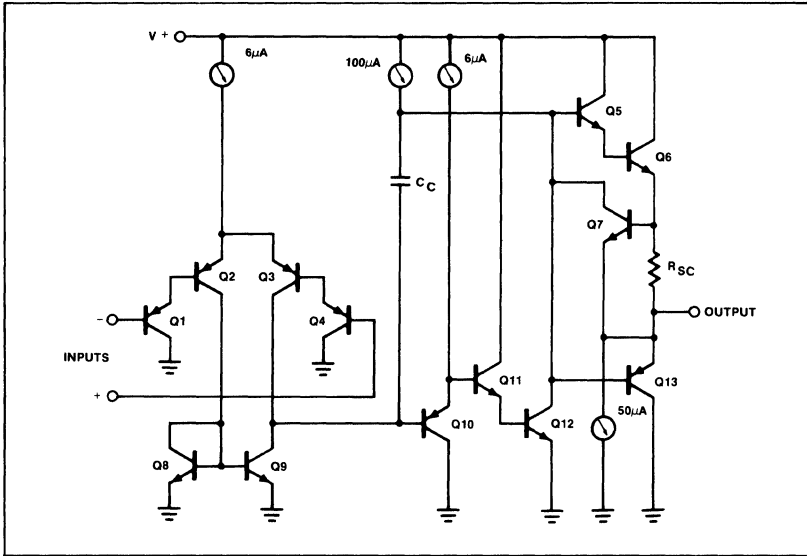
PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage ¹	R _S = 0Ω R _S = 0Ω, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V _{OS} Drift	R _S = 0Ω		7			7		μV/°C
I _{BIAS} Input current ²	I _{IN} (+) or I _{IN} (-) I _{IN} (+) or I _{IN} (-), over temp.		45 40	150 300		45 40	250 500	nA nA
I _{OS} Offset current	I _{IN} (+) - I _{IN} (-) I _{IN} (+) - I _{IN} (-), over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I _{OS} Drift			10			10		pA/°C
V _{CM} Common mode voltage range ³	V+ = 30V V+ = 30V, over temp.	0 0		V+ - 1.5 V+ - 2	0 0		V+ - 1.5 V+ - 2	V V
C _{MRR} Common mode rejection ratio		70	85		65	70		dB
V _{OUT} Output voltage swing	R _L = 2kΩ, V+ = +30V, over temp.	26			26			V
V _{OH}	R _L ≤ 10kΩ, over temp.	27	28		27	28		V
V _{OL}	R _L ≤ 10kΩ, V+ = 5V, over temp.		5	20		5	20	mV
I _{CC} Supply current	R _L = ∞, V _{CC} = 30V, over temp. R _L = ∞, on all op amps, over temp.		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA
A _{VOL} Large signal voltage gain	V+ = +15V (for large V _O swing), R _L ≥ 2kΩ V+ = +15V (for large V _O swing), R _L ≥ 2kΩ, over temp.	50 25	100		25 15	100		V/mV V/mV
Amplifier-to-amplifier coupling ⁵	f = 1kHz to 20kHz, input referred		-120			-120		dB
PSRR	R _S ≤ 0Ω	65	100		65	100		dB
Output current Source	V _{IN+} = +1Vdc, V _{IN-} = 0Vdc, V+ = 15Vdc V _{IN+} = +1Vdc, V _{IN+} = 0Vdc, V+ = 15Vdc, over temp.	20 10	40 20		20 10	40 20		mA mA
Sink	V _{IN-} = +1Vdc, V _{IN+} = 0Vdc, V+ = 15Vdc V _{IN-} = +1Vdc, V _{IN+} = 0Vdc, V+ = 15Vdc, over temp. V _{IN+} = 0Vdc, V _{IN-} = +1Vdc, V _O = 200mV	10 5 12	20 8 50		10 5 12	20 8 50		mA mA μA
I _{SC} Short circuit current ⁴			40	60		40	60	mA
Differential input voltage ⁶				V+			V+	V

NOTES

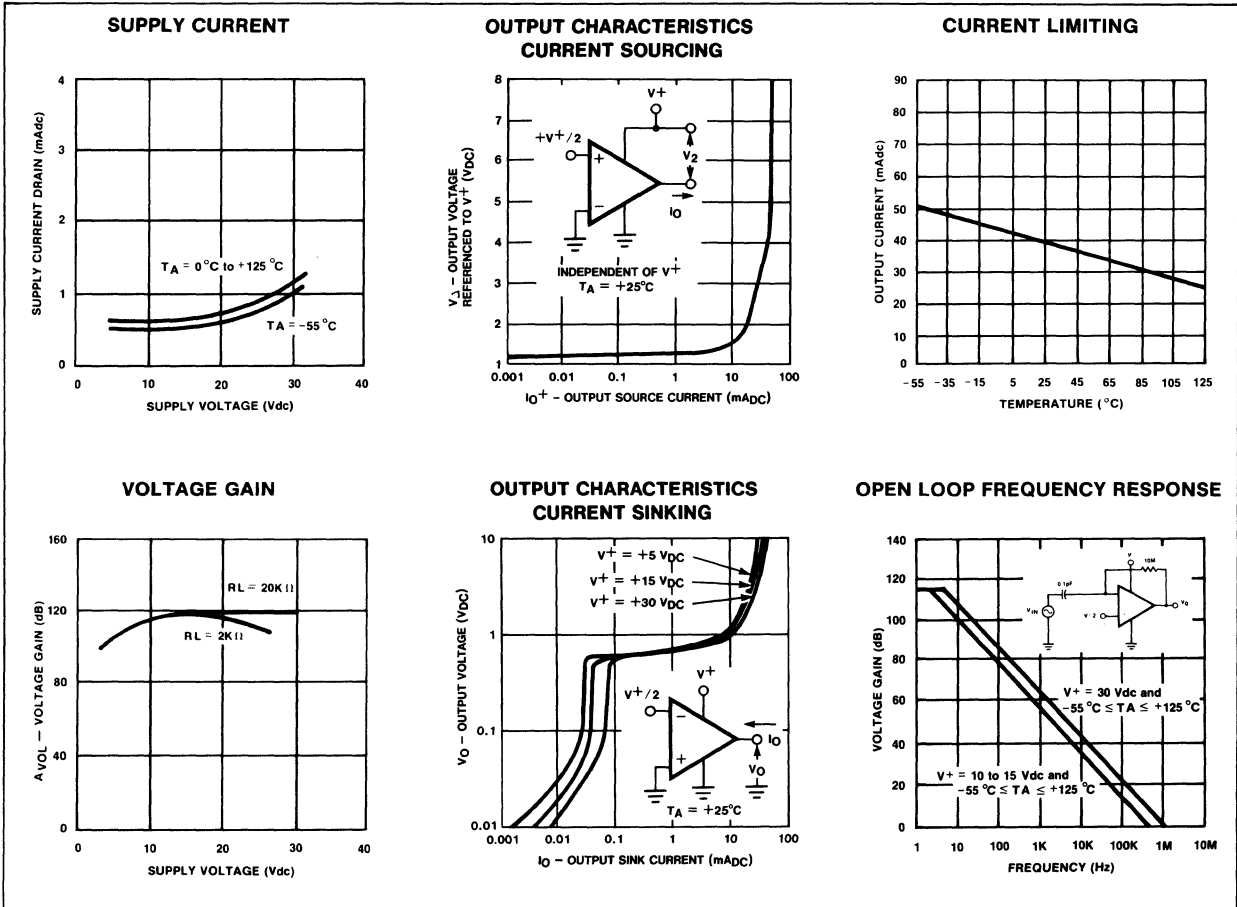
1. V_O = 1.4Vdc, R_S = 0Ω with V+ from 5V to 30V and over full input common mode range (0Vdc to V+ - 1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ - 1.5, but either or both inputs can go to +32V without damage.
4. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the

5. magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
 6. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
5. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ - 1.5V, but either or both inputs can go to +32Vdc without damage.

EQUIVALENT SCHEMATIC

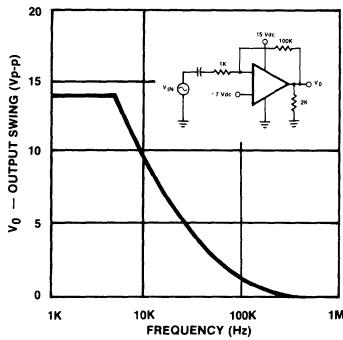


TYPICAL PERFORMANCE CHARACTERISTICS

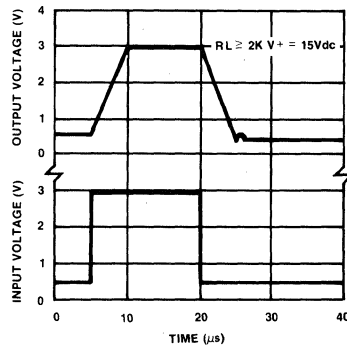


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

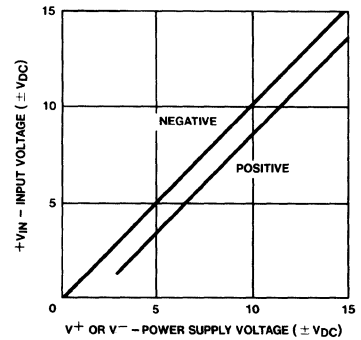
**LARGE SIGNAL
FREQUENCY RESPONSE**



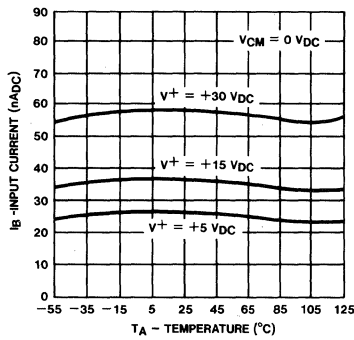
**VOLTAGE FOLLOWER
PULSE RESPONSE**



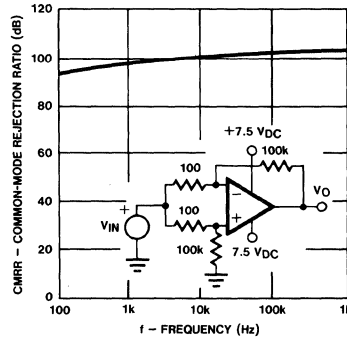
INPUT VOLTAGE RANGE



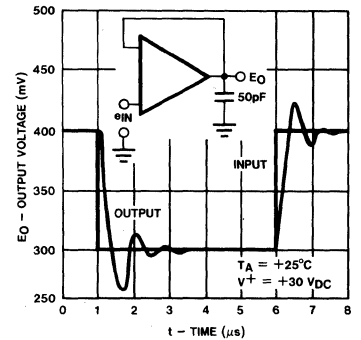
INPUT CURRENT



**COMMON MODE REJECTION
RATIO**



**VOLTAGE FOLLOWER PULSE
RESPONSE (SMALL SIGNAL)**



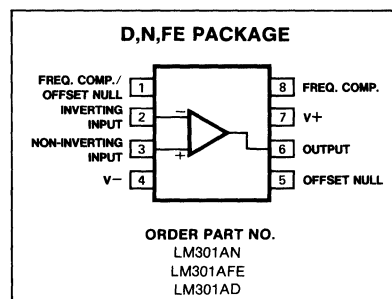
DESCRIPTION

The LM301A is a high performance operational amplifier featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- Short circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch up
- LM101, LM101A, LH2101, LH2101A
Mil std 883A,B,C available
- LM101A, LH2101A Mil std 38510 (JAN) available

PIN CONFIGURATIONS



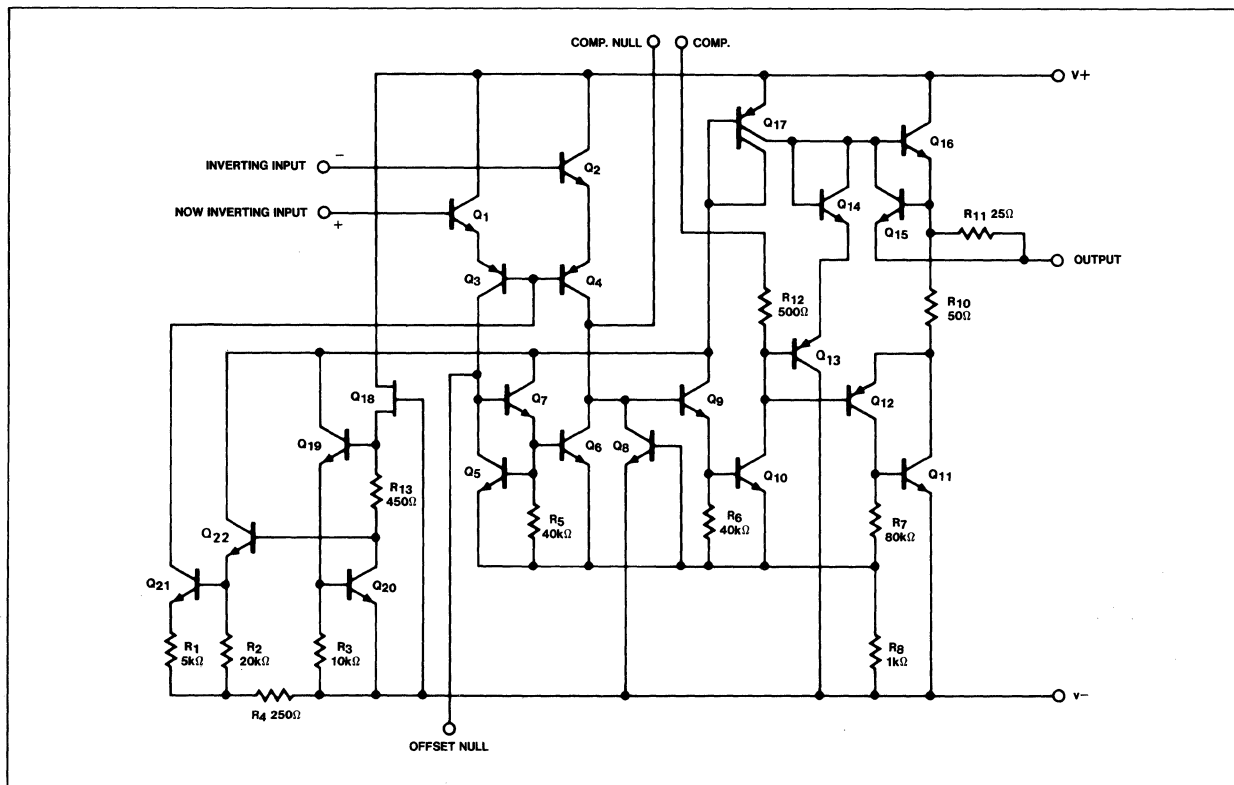
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage LM301A	± 18	V
Power dissipation	500	mW
Differential input voltage	± 30	V
Input voltage ¹	± 15	V
Output short circuit duration	Indefinite	
Operating temperature range LM301A	0 to +70	$^{\circ}\text{C}$
Storage temperature range	-65 to +150	$^{\circ}\text{C}$
Lead temperature (soldering 60sec)	300	$^{\circ}\text{C}$

NOTES

1. For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



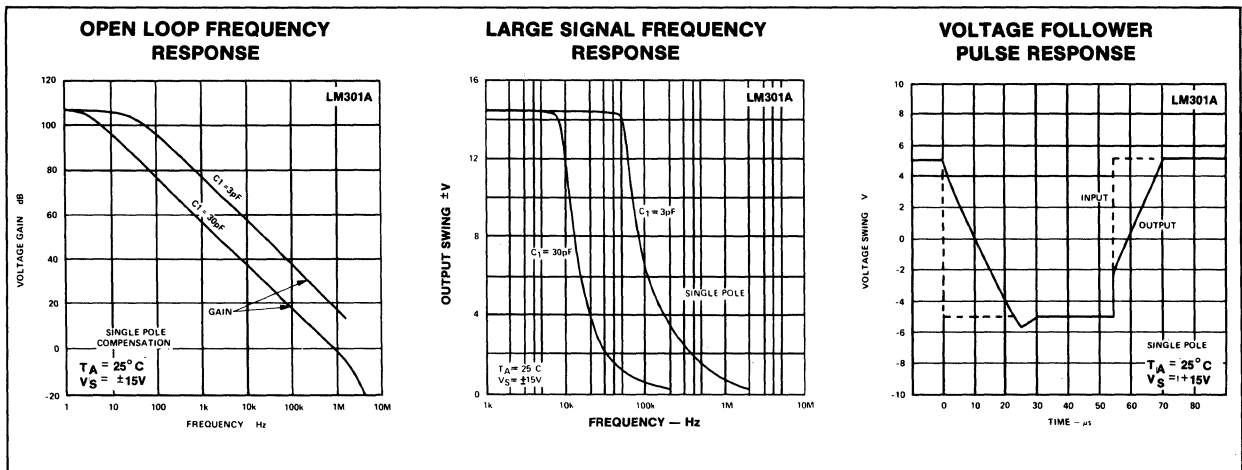
DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A < 70^{\circ}\text{C}$, $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ and $C_1 = 30\text{pF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{OS} Input Offset Voltage	T _A = 25°C, R _S < 50kΩ		2.0	7.5	mV
I _{OS} Input Offset Current	T _A = 25°C		3	50	nA
I _{BIAS} Input Bias Current	T _A = 25°C		70	250	nA
I _{OS} Input Resistance	T _A = 25°C	0.5	2		MΩ
I _{CC} Supply Current	T _A = 25°C, V _S = ±15V		1.8	3.0	mA
AV _{OL} Large Signal Voltage Gain	T _A = 25°C, V _S = ±15V V _{OUT} = ±10V; R _L > 2kΩ	25	160		V/mV
V _{OS} Input Offset Voltage	R _S < 50kΩ			10	mV
V _{OS} Average Temperature Coefficient of Input Drift Offset Voltage			6.0	30	μV/°C
I _{OS} Input Offset Current				70	nA
I _{OS} Average Temperature Coefficient of Input Offset Current	25°C < T _A < 70°C 0°C < T _A < 25°C		0.01 0.02	0.3 0.6	nA/°C nA/°C
I _{BIAS} Input Bias Current				300	nA
AV _{OL} Large Signal Voltage Gain	V _S = ±15V, V _{OUT} = ±10V R _L > 2kΩ	15			V/mV
V _{OUT} Output Voltage Swing	V _S = ±15V, R _L = 10kΩ R _L = 2kΩ	±12 ±10	±14 ±13		V V
V _{IN} Input Voltage Range	V _S = ±15V	±12			V
C _{MRR} Common Mode Rejection Ratio	R _S < 50kΩ	70	90		dB
P _{SRR} Supply Voltage Rejection Ratio	R _S < 50kΩ	70	96		dB

*NOTE

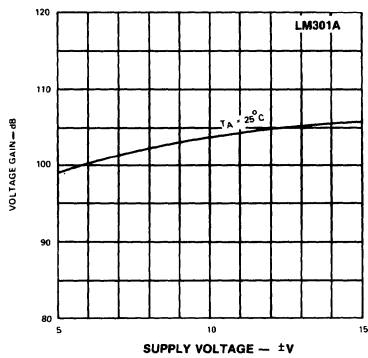
Unless otherwise specified, all specifications for LM301A are $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$.

TYPICAL PERFORMANCE CHARACTERISTICS

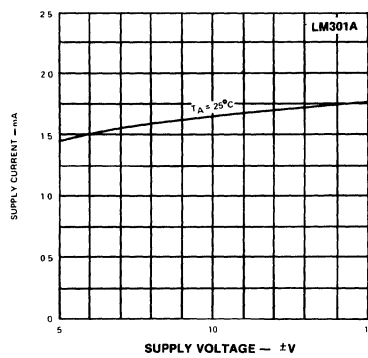


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

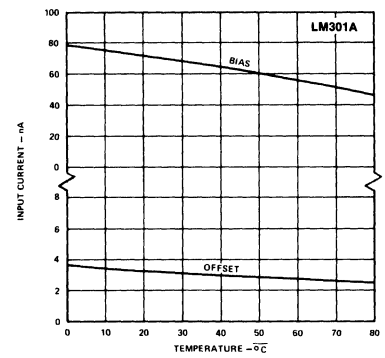
VOLTAGE GAIN



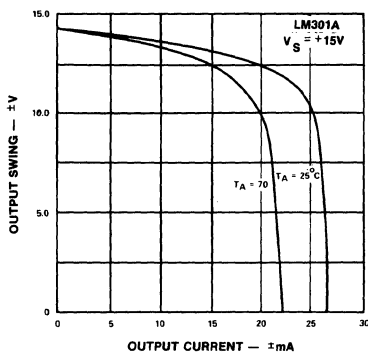
SUPPLY CURRENT



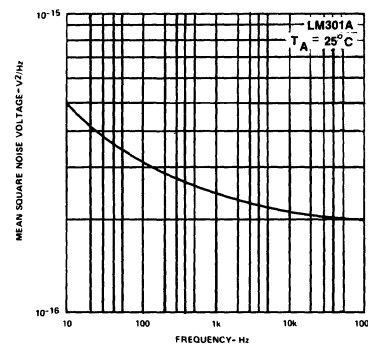
INPUT CURRENT



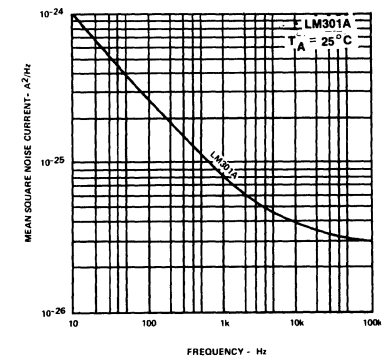
CURRENT LIMITING



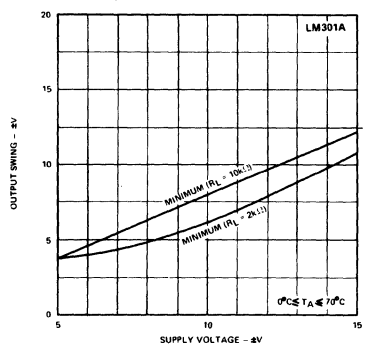
INPUT NOISE VOLTAGE



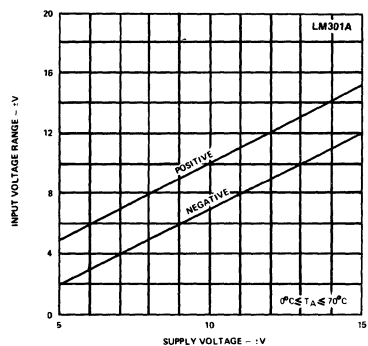
INPUT NOISE CURRENT



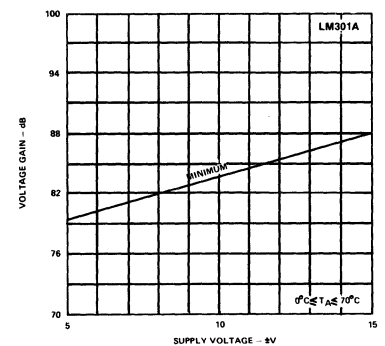
OUTPUT SWING



INPUT VOLTAGE RANGE

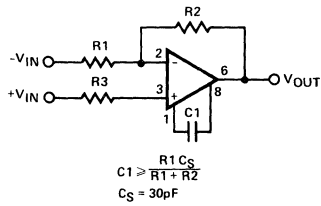


VOLTAGE GAIN

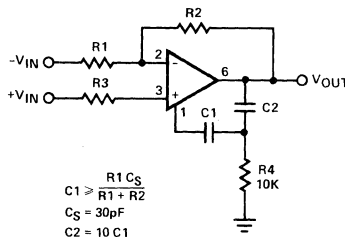


COMPENSATION CIRCUITS

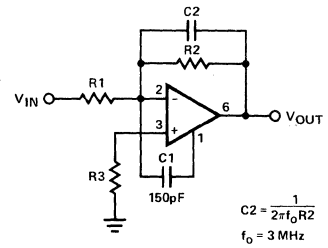
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION

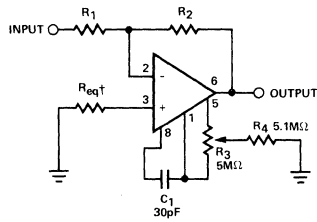


FEED FORWARD COMPENSATION



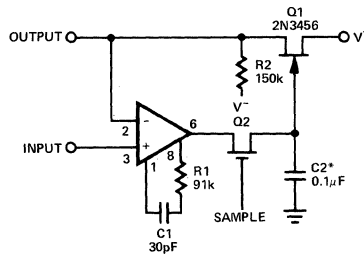
TYPICAL APPLICATIONS

INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

LOW DRIFT SAMPLE AND HOLD



*Polycarbonate Dielectric Capacitor

DESCRIPTION

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are specifically designed to complement the dynamic range of the amplifiers.

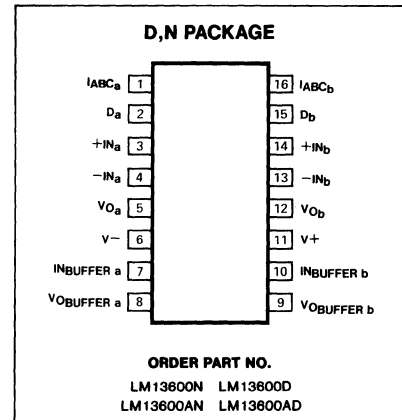
FEATURES

- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal to noise ratio
- Wide supply range $\pm 2V$ to $\pm 22V$.
- See Signetics NE5517 for typical circuit applications information

APPLICATIONS

- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

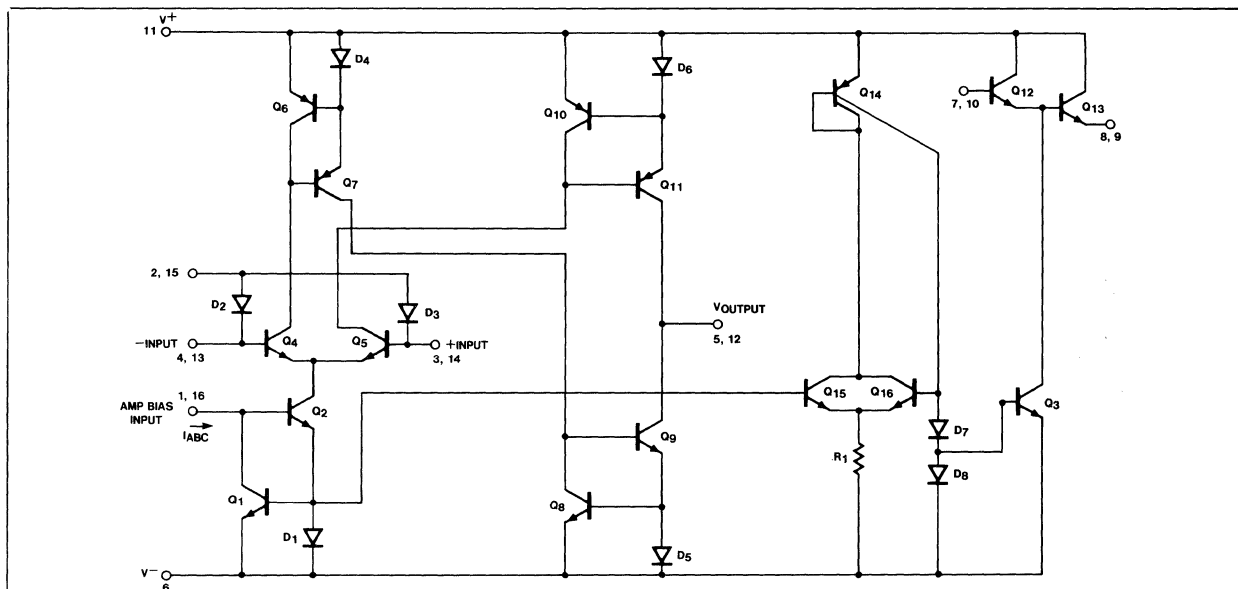
PIN DESCRIPTION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage ¹		
LM13600	36 V _{DC} or ± 18	V
LM13600A	44 V _{DC} or ± 22	V
Power dissipation ² T _A = 25°C		
LM13600N, LM13600AN	570	mW
Differential input voltage	± 5	V
Diode bias current (I _D)	2	mA
Amplifier bias current (I _{ABC})	2	mA
Output short circuit duration	Indefinite	
Buffer output current ³	20	mA
Operating temperature range		
LM13600N, LM13600AN	0°C to +70	°C
DC input voltage	+V _S to -V _S	
Storage temperature range	-65°C to +150	°C
Lead temperature (Soldering, 10 Seconds)	300	°C

BLOCK DIAGRAM



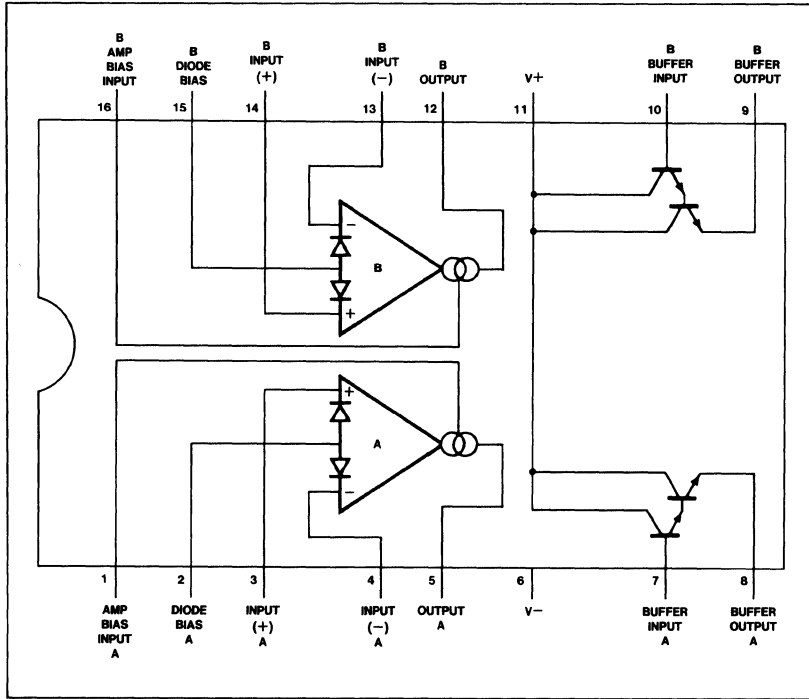
ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LM13600			LM13600A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V _{OS})	Over specified temperature range I _{ABC} 5μA		0.4	5		0.4	2	mV
			0.3	5		0.3	5	mV
			0.3	5		0.3	2	mV
V _{OS} including diodes	Diode Bias Current (I _D) = 500 μA		0.5	5		0.5	2	mV
Input offset change	5 μA ≤ I _{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
Input bias current	Over specified temperature range		0.4	5		0.4	5	μA
			1	8		1	7	μA
Forward Transconductance (gm)	Over specified temperature range	6700	9600	13000	7700	9600	12000	μmho
		5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I _{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I _{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over specified temp range	300			300			μA
Peak output voltage positive	RL = ∞, 5 μA ≤ I _{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
	RL = ∞, 5 μA ≤ I _{ABC} ≤ 500 μA	-12	-14.4		-12	-14.4		V
Supply current	I _{ABC} = 500 μA, Both channels		2.6			2.6		mA
V _{OS} sensitivity positive	ΔV _{OS} /ΔV+		20	150		20	150	μV/V
			20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input ⁵ 20 Hz < f < 20 KHz		100			100		dB
Diff. input current	I _{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage current	I _{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V

NOTES

- For selections to a supply voltage above ±22V, contact factory.
- For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
- Buffer output current should be limited so as to not exceed package dissipation.
- These specifications apply for V_S = ±15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for V_S = ±15V, I_{ABC} = 500 μA, R_{OUT} = 5Ω connected from the buffer output to -V_S and the input of the buffer is connected to the transconductance amplifier output.

CONNECTION DIAGRAM



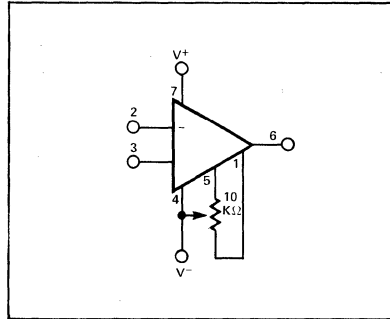
DESCRIPTION

The MC1456/1556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The MC1456/1556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

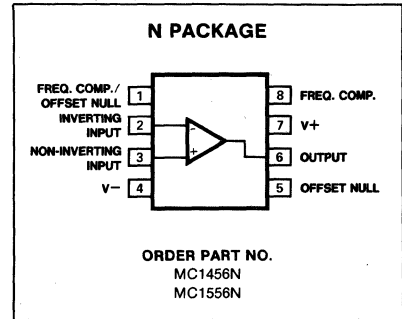
FEATURES

- Low input bias current—15nA maximum
- Low input offset current—2.0nA maximum
- Low input offset voltage—4.0mV maximum
- High slew rate—2.5V/ μ s typical
- Large power bandwidth—40kHz typical
- Low power consumption—45mW maximum
- Offset voltage null capability
- Output short circuit protection
- Input over-voltage protection
- Mil std 883A,B,C, available

OFFSET ADJUST CIRCUIT



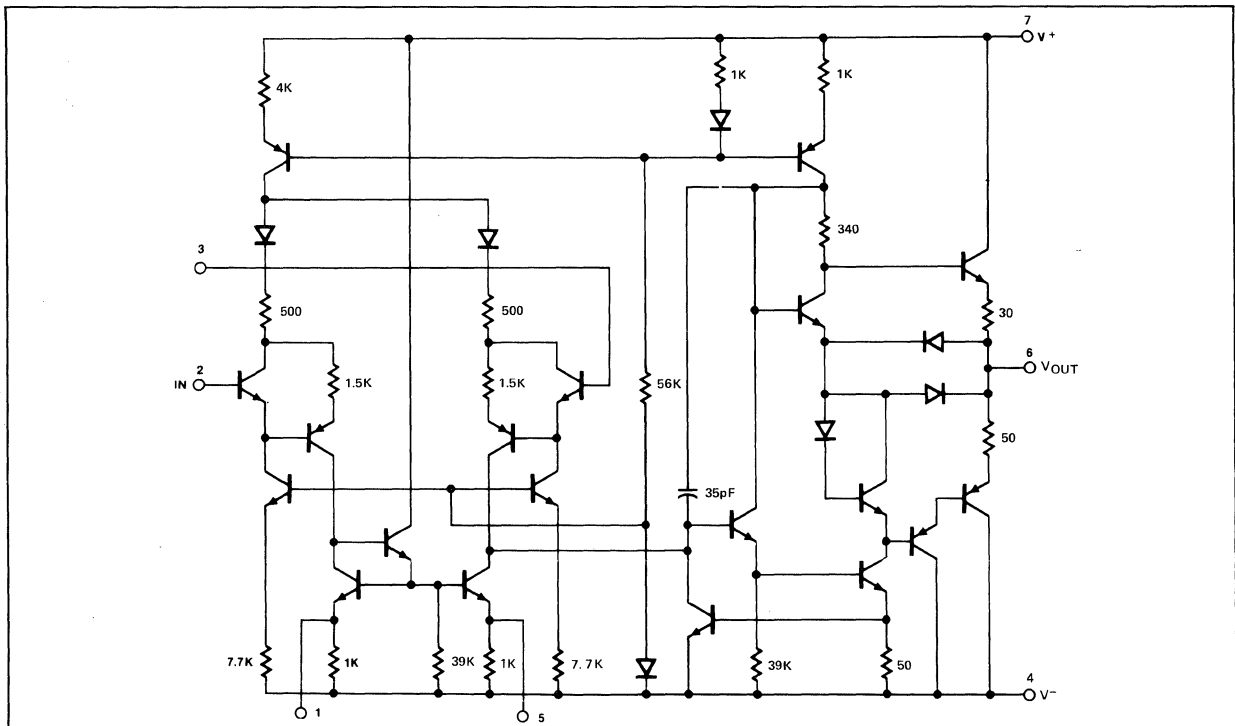
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage MC1556	± 22	V
MC1456	± 18	V
Differential input voltage	$\pm V_{CC}$	V
Common mode input voltage	$\pm V_{CC}$	V
Load current	20	mA
Output short circuit duration	Continuous	
Power dissipation	680	mW
Derate above $T_A = 25^\circ\text{C}$	4.6	mW/ $^\circ\text{C}$
Operating temperature range MC1556	-55 to +125	$^\circ\text{C}$
MC1456	0 to +70	$^\circ\text{C}$
Storage temperature range	-65 to +150	$^\circ\text{C}$

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified

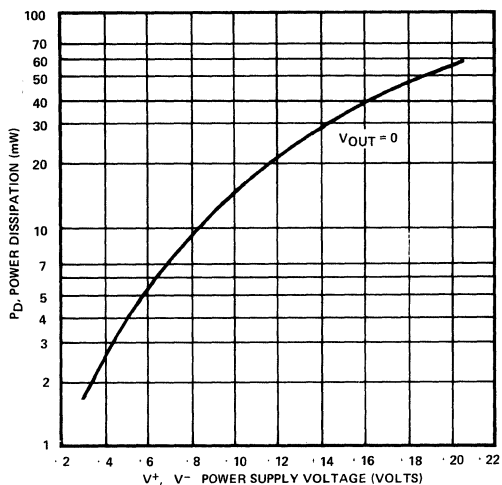
PARAMETER	TEST CONDITIONS	MC1556			MC1456			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	Over temperature		2.0	4.0 6.0		5.0	10.0 14.0	mVdc mVdc
I_{OS} Offset current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		1.0	2.0 3.0 5.0		5.0	10.0 14	nA nA nA
I_{BIAS} Input current	Over temperature		8.0	15 30		15.0	30.0 40	nA nA
V_{CM} Common mode voltage range	$R_S \leq 10\text{k}\Omega$, $T_A = 25^\circ\text{C}$, $f = 100\text{Hz}$	± 12	± 13		± 11	± 12		V
CMRR Common mode rejection ratio		80	110		70	110		dB
Z_{IN} Common mode input impedance		$f = 20\text{Hz}$		250			250	
V_{OUT} Output voltage swing	$R_L = 2\text{k}\Omega$	± 12	± 13		± 11	± 12		V
I_{CC} Supply current			1.0	1.5		1.3	3.0	mA
P_D DC quiescent power dissipation ($V_O = 0$)			30	45		40	90	mW
$PSRR$ Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		50	100		75	200	$\mu\text{V}/\text{V}$
Large signal voltage gain	$R_L \leq 2\text{k}\Omega$, $V_{OUT} = \pm 10\text{V}$, $T_A = 25^\circ\text{C}$ Over temperature	100 40	200		70 40	100		V/mV V/mV

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

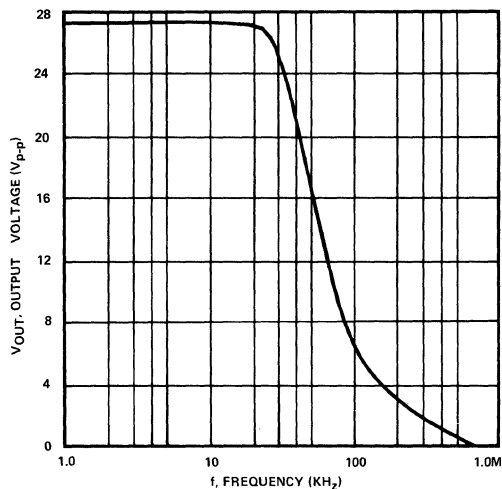
PARAMETER	TEST CONDITIONS	MC1556			MC1456			UNIT
		Min	Typ	Max	Min	Typ	Max	
c_p Differential input impedance	Open loop $f = 20\text{Hz}$ $A_V = 100$, $R_S = 10\text{k}\Omega$, $f = 1.0\text{kHz}$, $BW = 1.0\text{kHz}$		6.0			6.0		pF
r_p Parallel input capacitance			5			3		M Ω
e_n Parallel input resistance				45			45	$\text{nV}/\sqrt{\text{Hz}}$
BW_p Power bandwidth	$A_V = 1$, $R_L = 2\text{k}\Omega$, $\text{THD} \leq 5\%$ $V_{OUT} = \pm 10\text{V}$		40			40		kHz
Phase margin (open loop, unity gain)			70			70		degrees
Gain margin			18			18		dB
S_R Slew rate (unity gain)			2.5			2.5		V/ μsec
Z_{OUT} Output impedance	$f = 20\text{Hz}$		1.0	2.0		1.0	2.5	k Ω
BW Unity gain crossover frequency (open loop)			1.0			1.0		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

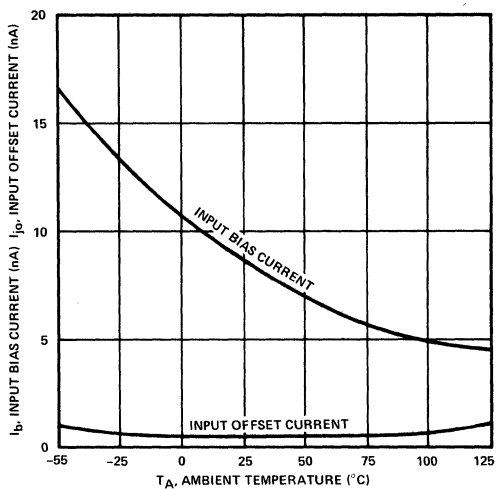
POWER DISSIPATION vs
POWER SUPPLY VOLTAGE



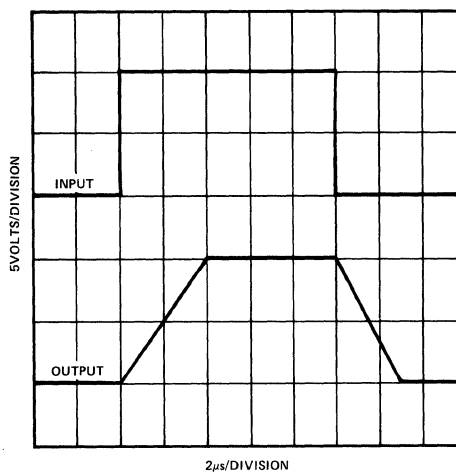
POWER
BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT vs
TEMPERATURE FOR MC1556



VOLTAGE FOLLOWER
PULSE RESPONSE



MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

DESCRIPTION

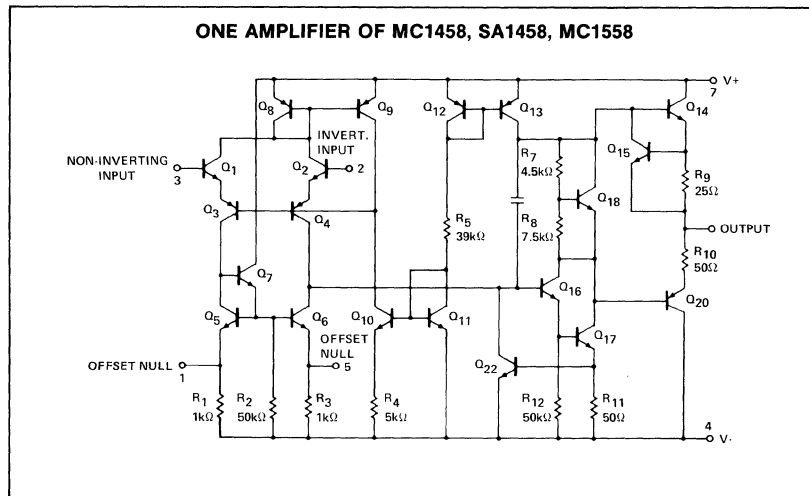
The MC1458 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The MC1458 is short-circuit protected and allows for nulling of offset voltage.

The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range
- No latch-up
- 1558/1458 are 2 "op amps" in space of one 741 package
- MC1558 Mil std 883A,B,C available

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
MC1458	±18	V
SA1458	±18	V
MC1558	±22	V
Internal power dissipation		
N package	500	mW
H package ¹	800	mW
F,FE package	1000	mW
Differential input voltage	±30	V
Input voltage ²	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
MC1458	0 to +70	°C
SA1458	-40 to +85	°C
MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 240°C/W, 150°C/W, 110°C/W for N, H, F and FE packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONFIGURATIONS

F PACKAGE

ORDER PART NO.

MC1458F
MC1558F

H PACKAGE*

ORDER PART NO.

MC1458H
MC1558H

*Metal cans (H) not recommended for new designs

D,N,FE PACKAGE

ORDER PART NO.

MC1458N MC1458FE
MC1558N MC1558FE
SA1458N MC1458D

MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1558			UNIT
		Min	Typ	Max	
V_{OS} Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$, over temp.		1.0	5.0 6.0	mV mV
I_{OS} Offset current	Over temp.		20	200 500	nA nA
I_{BIAS} Input bias current	Over temp.		80	500 1500	nA nA
V_{OUT} Output voltage swing	$R_L = 10\text{k}\Omega$, over temp. $R_L = 2\text{k}\Omega$, over temp.	± 12 ± 10	± 14 ± 13		V V
A_{VOL} Large signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	50 25	100		V/mV V/mV
Offset voltage adjustment range			± 30		mV
$PSRR$ Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		30	150	$\mu\text{V/V}$
$CMRR$ Common mode rejection ratio		70	90		dB
I_{CC} Supply current			2.3	5.0	mA
V_{IN} Input voltage range		± 12	± 13		V
P_d Power consumption			70	150	mW
R_{OUT} Channel separation			120		dB
I_{SC} Output resistance			75		Ω
I_{SC} Output short-circuit current			25		mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

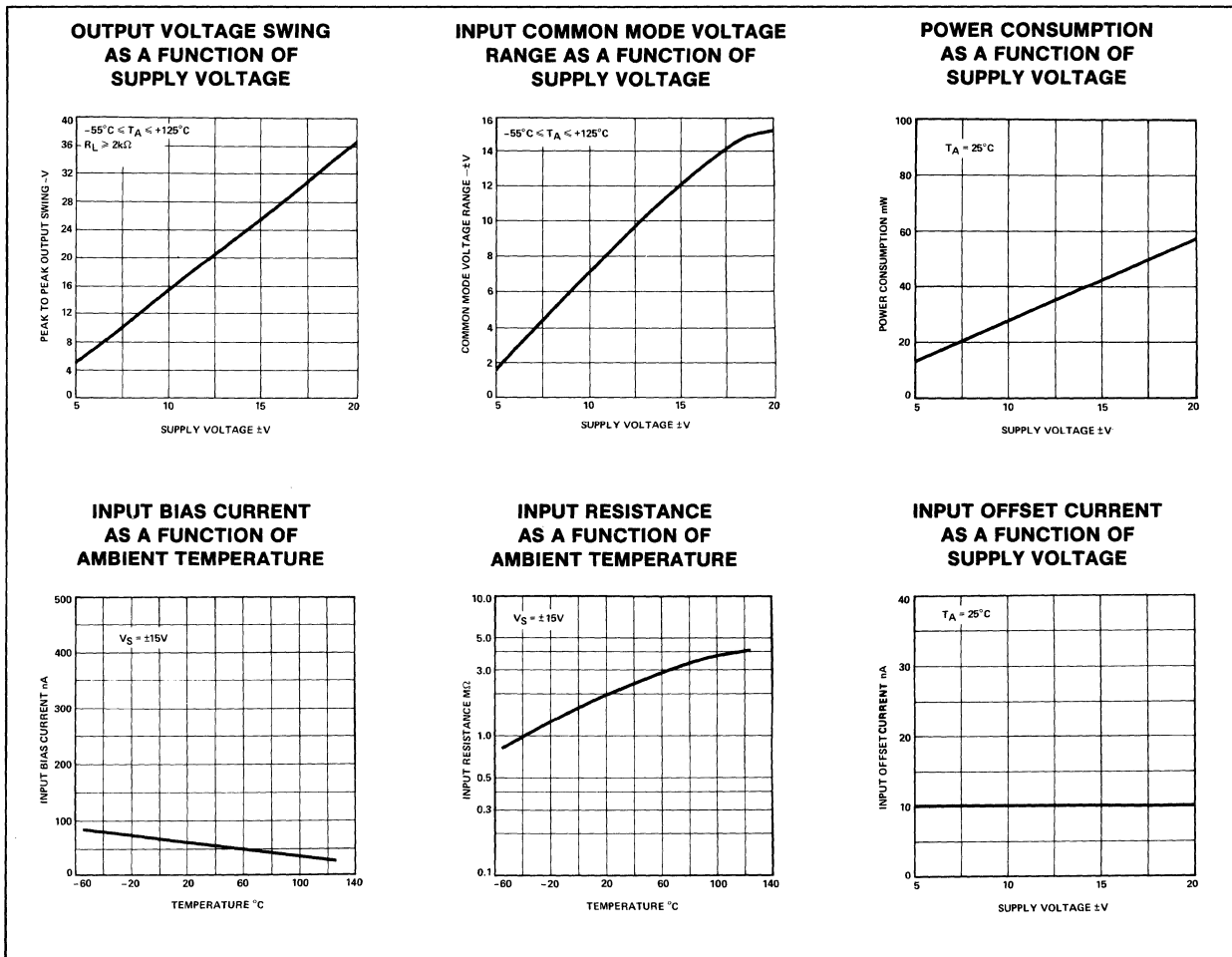
PARAMETER	TEST CONDITIONS	MC1458			SA1458			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$, over temp.		2.0	6.0 7.5		2.0	6.0 7.5	mV mV
I_{OS} Offset current	Over temp.		20	200 300		20	200 500	nA nA
I_{BIAS} Input bias current	Over temp.		80	500 800		80	500 1500	nA nA
V_{OUT} Output voltage swing	$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$, over temp.	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V
A_{VOL} Large signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	25 15	200		20 15	200		V/mV V/mV
Offset voltage adjustment range			± 30			± 30		mV
$PSRR$ Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		30	150		30	150	$\mu\text{V/V}$
$CMRR$ Common mode rejection ratio		70	90		70	90		dB
I_{CC} Supply current			2.3	5.6		2.3	5.6	mA
V_{IN} Input voltage range		± 12	± 13		± 12	± 13		V
R_{IN} Input resistance								$\text{M}\Omega$
P_d Power consumption			70	170		70	170	mW
R_{OUT} Channel separation			120			120		dB
I_{SC} Output short-circuit current			25			25		mA

MC1458/1558-N,H,FE,F
SA1458-N
MC1458-D

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

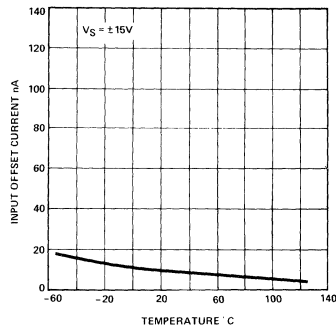
PARAMETER	TEST CONDITIONS	MC1458 SA1458, MC1558			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, $f = 20\text{Hz}$	0.3			$M\Omega$
Common mode input impedance	$f = 20\text{Hz}$		200		$M\Omega$
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0k\text{Hz}$ $f = 1.0k\text{Hz}$		45		$nV/\sqrt{\text{Hz}}$
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $\text{THD} \leq 5\%$ $V_{OUT} = 20\text{Vp-p}$		14		kHz
Phase margin			65		degrees
Gain margin			11		dB
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{IN} = 20\text{mV}$, $R_L = 2k\Omega$, $C_L \leq 100\text{pf}$		0.3		μs
Rise time			5.0		%
Overshoot			0.8		$\text{V}/\mu\text{s}$
Slew rate	$C \leq 100\text{pf}$, $R_L \geq 2k$, $V_{IN} = \pm 10\text{V}$				

TYPICAL PERFORMANCE CHARACTERISTICS

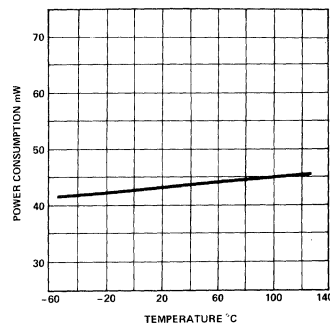


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

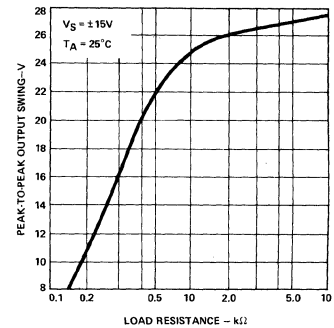
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



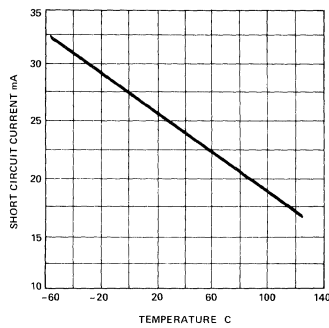
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



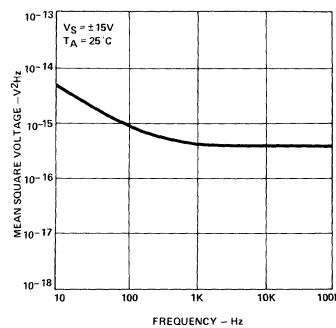
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



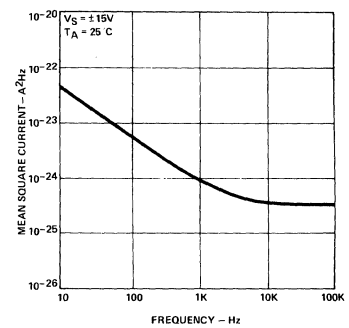
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



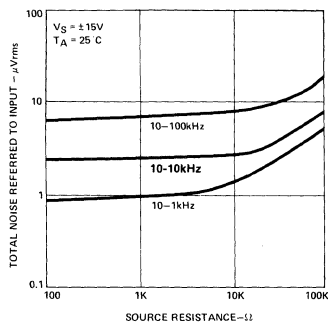
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



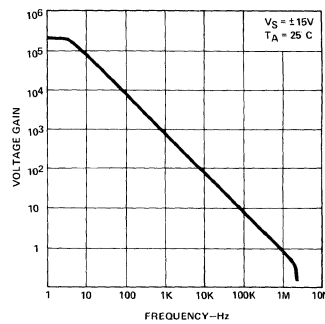
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



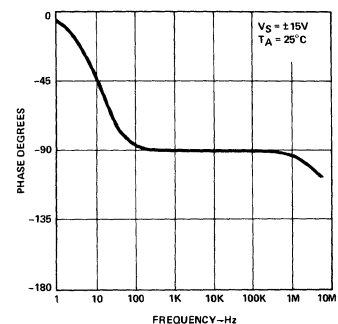
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

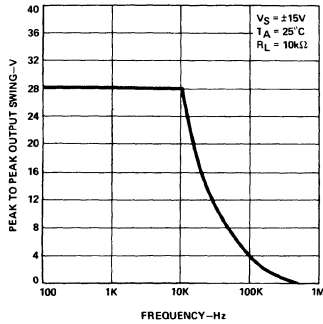


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

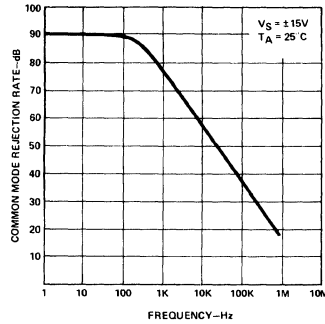


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

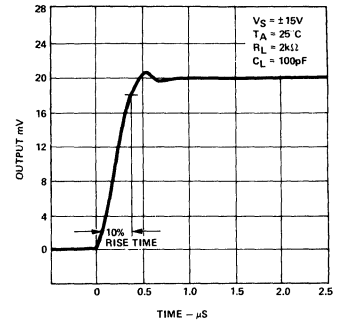
OUTPUT VOLTAGE SWING
AS A FUNCTION OF
FREQUENCY



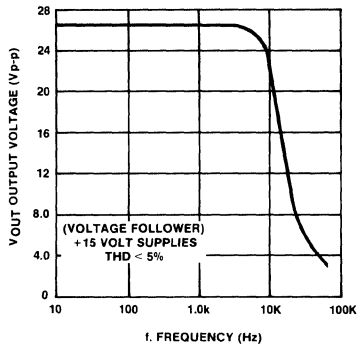
COMMON MODE REJECTION
RATIO AS A FUNCTION OF
FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH
(Large Signal Swing vs Frequency)



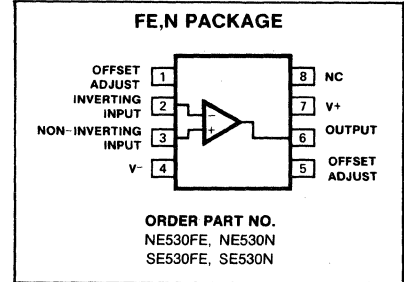
DESCRIPTION

The 530/5530 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated, the SE530/5530 guarantee slew rates of 25V/ μ s with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741, 747, 1458, 4558 and LF356 types.

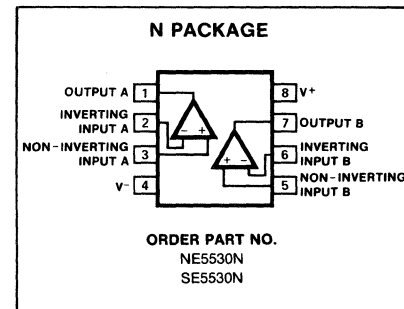
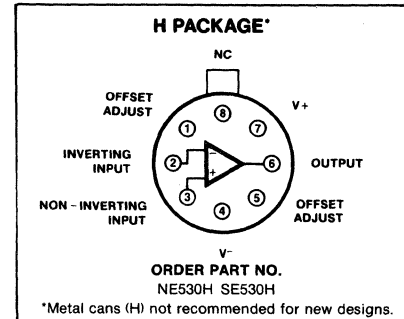
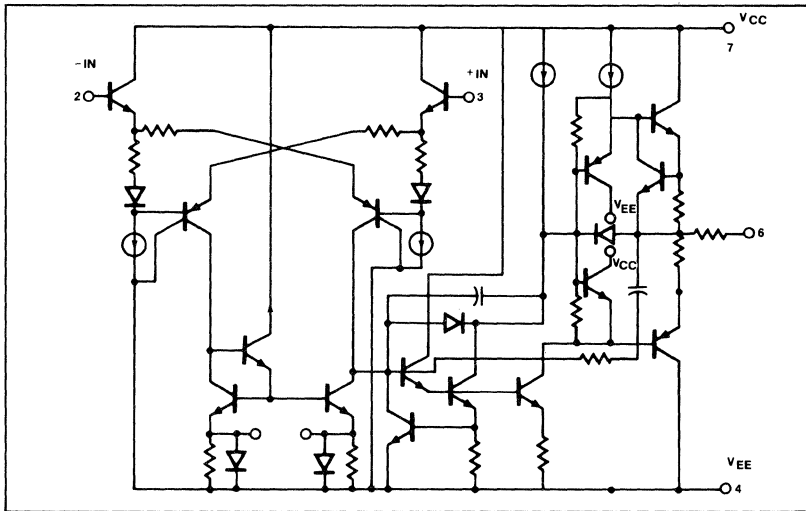
FEATURES

- Gain bandwidth product—3MHz
- 35V/ μ s slew rate (Gain = -1)
- Internal frequency compensation
- Low input offset voltage 2mV max
- Low input bias current-60nA max
- Short circuit protection
- Offset null capability
- Large common mode and differential voltage ranges

PIN CONFIGURATIONS

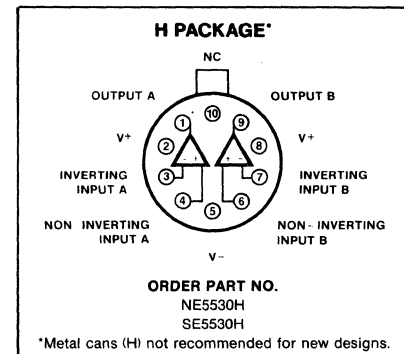


EQUIVALENT SCHEMATIC EACH AMPLIFIER



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE530/5530	± 22	V
NE530/5530	± 18	V
Internal power dissipation		
N Package	500	mW
H Package	800	mW
FE Package	1000	mW
Differential input voltage	± 30	V
Input voltage	± 15	V
Operating temperature range		
SE530/5530	-55 to +125	$^{\circ}$ C
NE530/5530	0 to +70	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature range	300	$^{\circ}$ C
(Solder, 60sec)		
Output short circuit	Indefinite	



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise specified.¹

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_s \leq 10\text{k}\Omega$ Over temperature		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
Temperature coefficient of input offset voltage			3	15		6		$\mu\text{V}/^\circ\text{C}$
Input offset current	Over temperature		5	20 40		15	40 80	nA nA
Input bias current	Over temperature		45	80 200		65	150 200	nA nA
Input resistance		3	10		1	6		$\text{M}\Omega$
Input voltage range		± 12	± 13		± 12	± 13		V
Large signal voltage gain	$R_L \geq 2\text{k}\Omega$, $V_0 = \pm 10\text{V}$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Output voltage swing	$R_L \geq 10\text{k}\Omega$ $R_L \geq 2\text{k}\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V V
Output short circuit current			25			25		mA
Output resistance			100			100		Ω
Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
Common mode rejection ratio	$R_s \leq 10\text{k}\Omega$ Over temperature	70	90		70	90		dB
Power supply rejection ratio	$R_s \leq 10\text{k}\Omega$ Over temperature		30	150		30	150	$\mu\text{V}/\text{V}$

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise specified.

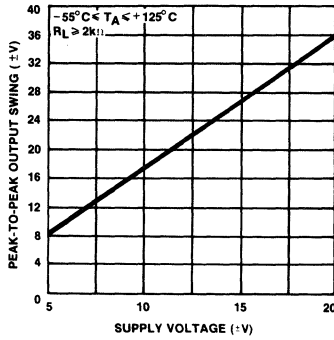
PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response Small signal rise time Small signal overshoot Settling time	TO 0.1% (10V step)		.06 13 0.9			.06 13 0.9		μs % μs
Slew rate Unity gain inverting Unity gain non-inverting	$\pm 15\text{V}$ supply, $V_0 = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	25 18	35 25		20 12	35 25		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
Power bandwidth	5% THD, $V_0 = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Channel separation			120			120		dB

NOTE

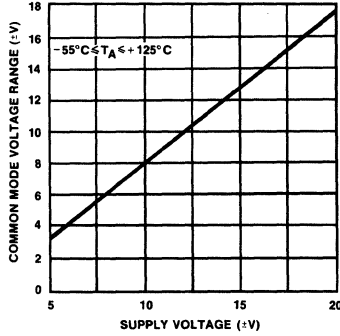
1. Operating temperature range for the SE530/5530 is -55°C to $+125^\circ\text{C}$.
Operating temperature range for the NE530/5530 is 0°C to $+70^\circ\text{C}$.

TYPICAL PERFORMANCE CHARACTERISTICS

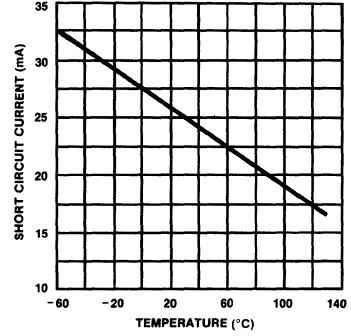
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



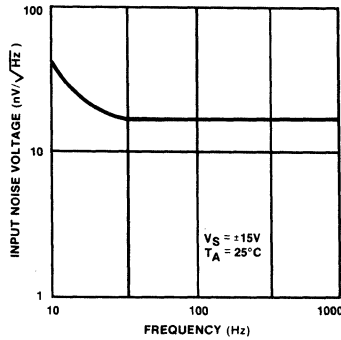
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



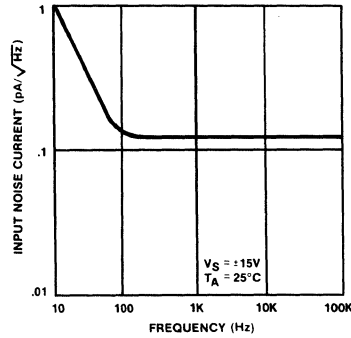
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



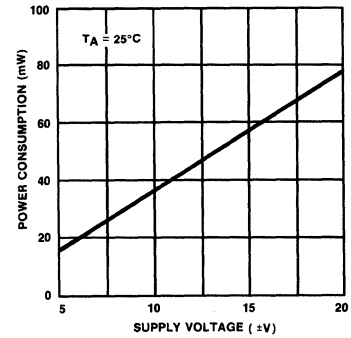
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



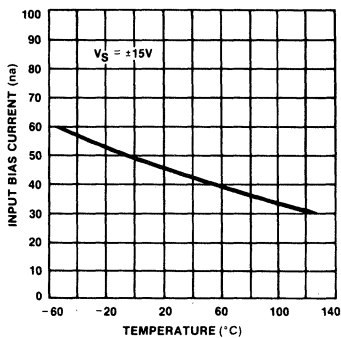
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



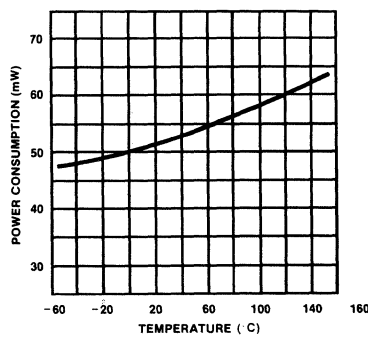
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (EACH AMPLIFIER)



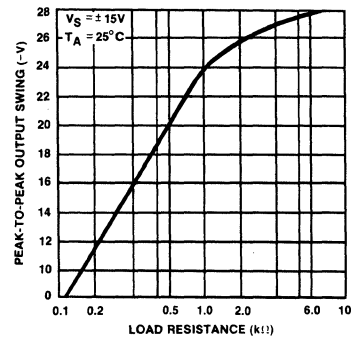
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (EACH AMPLIFIER)

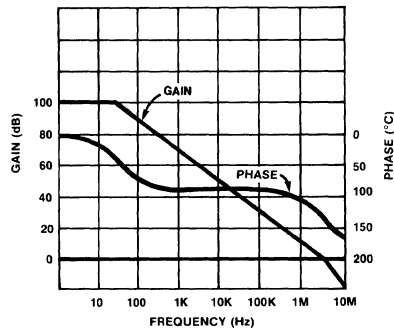


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

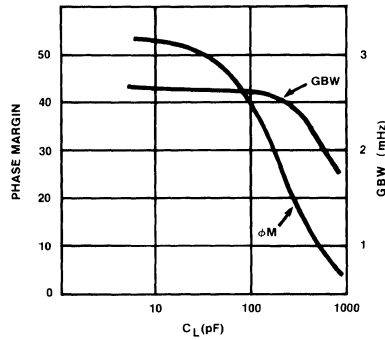


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

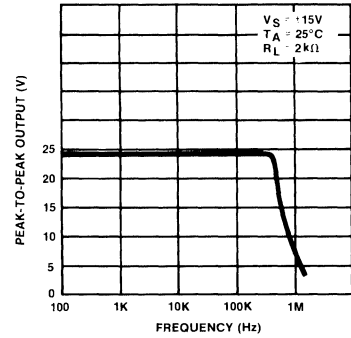
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



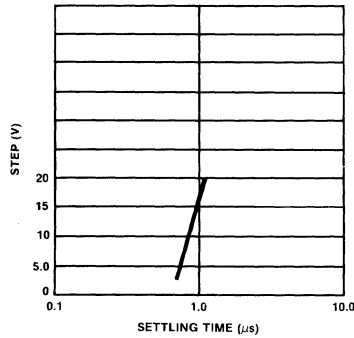
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



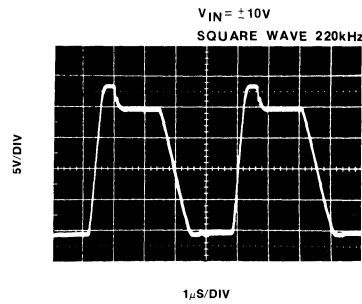
POWER BANDWIDTH



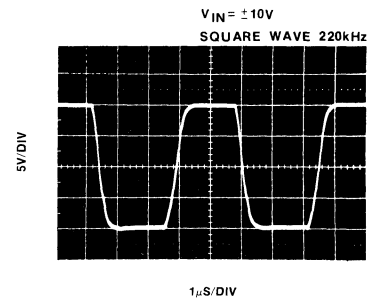
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

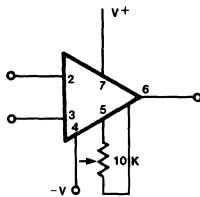


SLEW RATE (-1 AMPLIFIER)

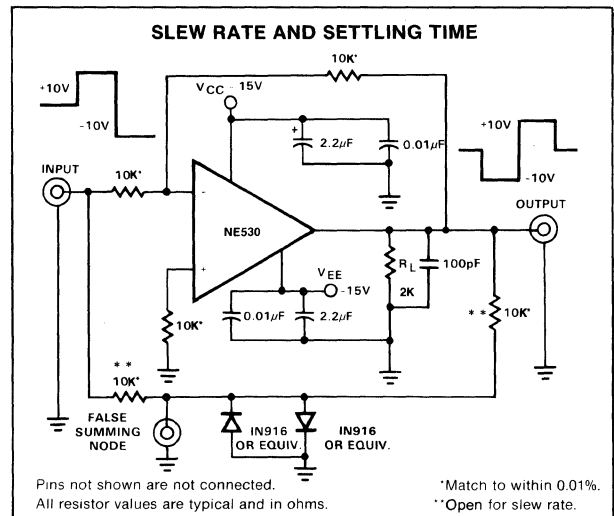
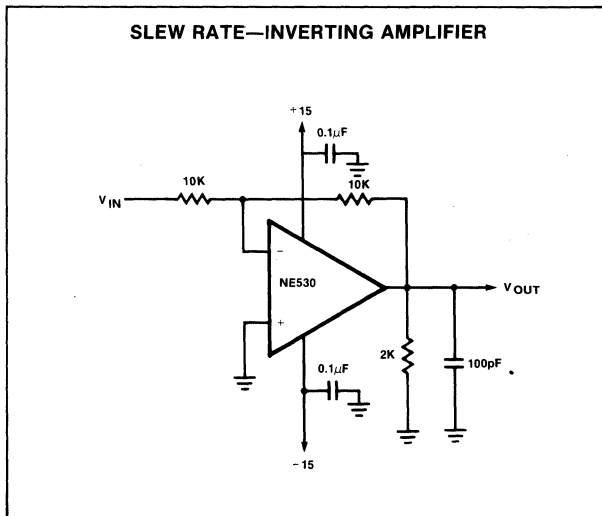
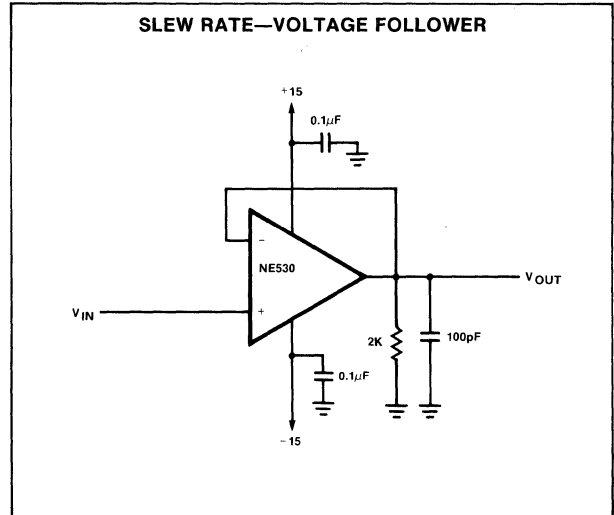
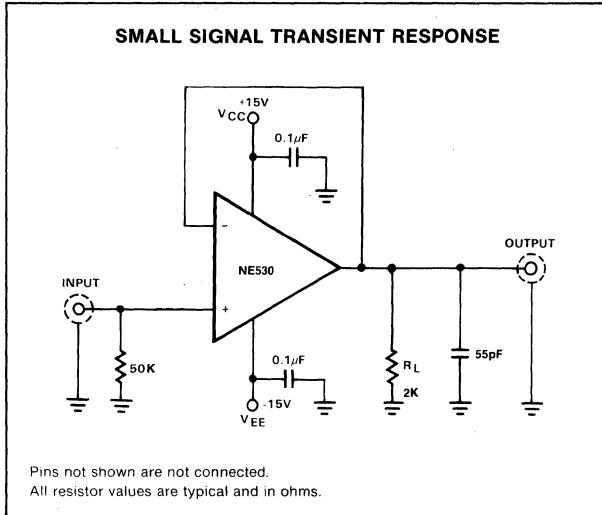


TYPICAL CIRCUIT CONNECTION

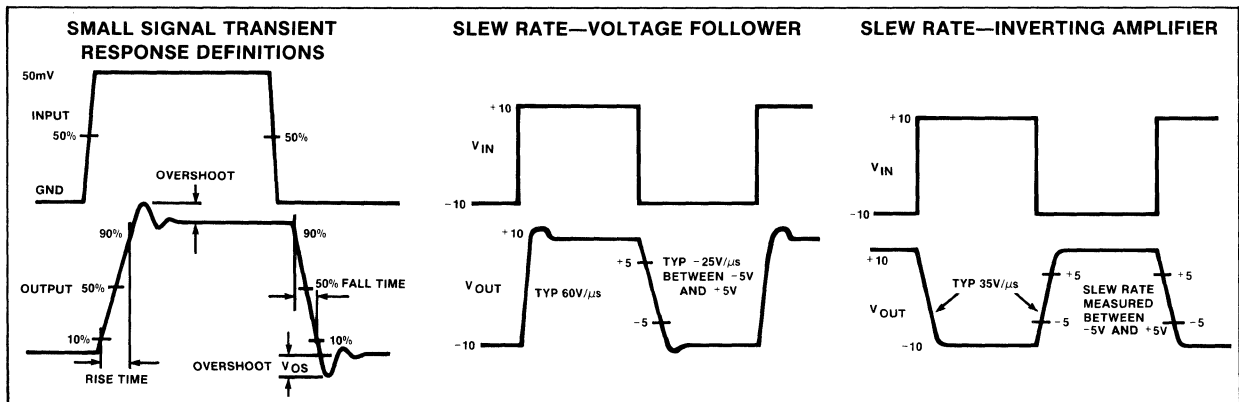
OFFSET ADJUST CIRCUIT



TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



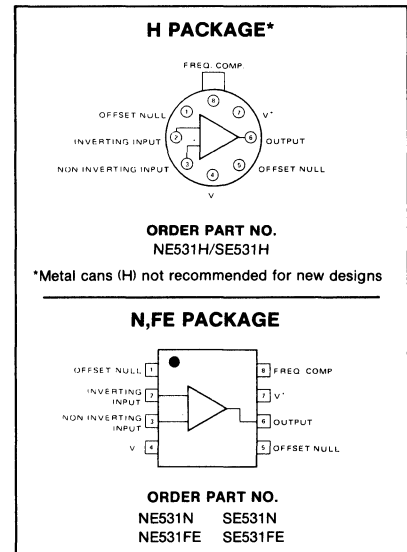
DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier outperforms conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

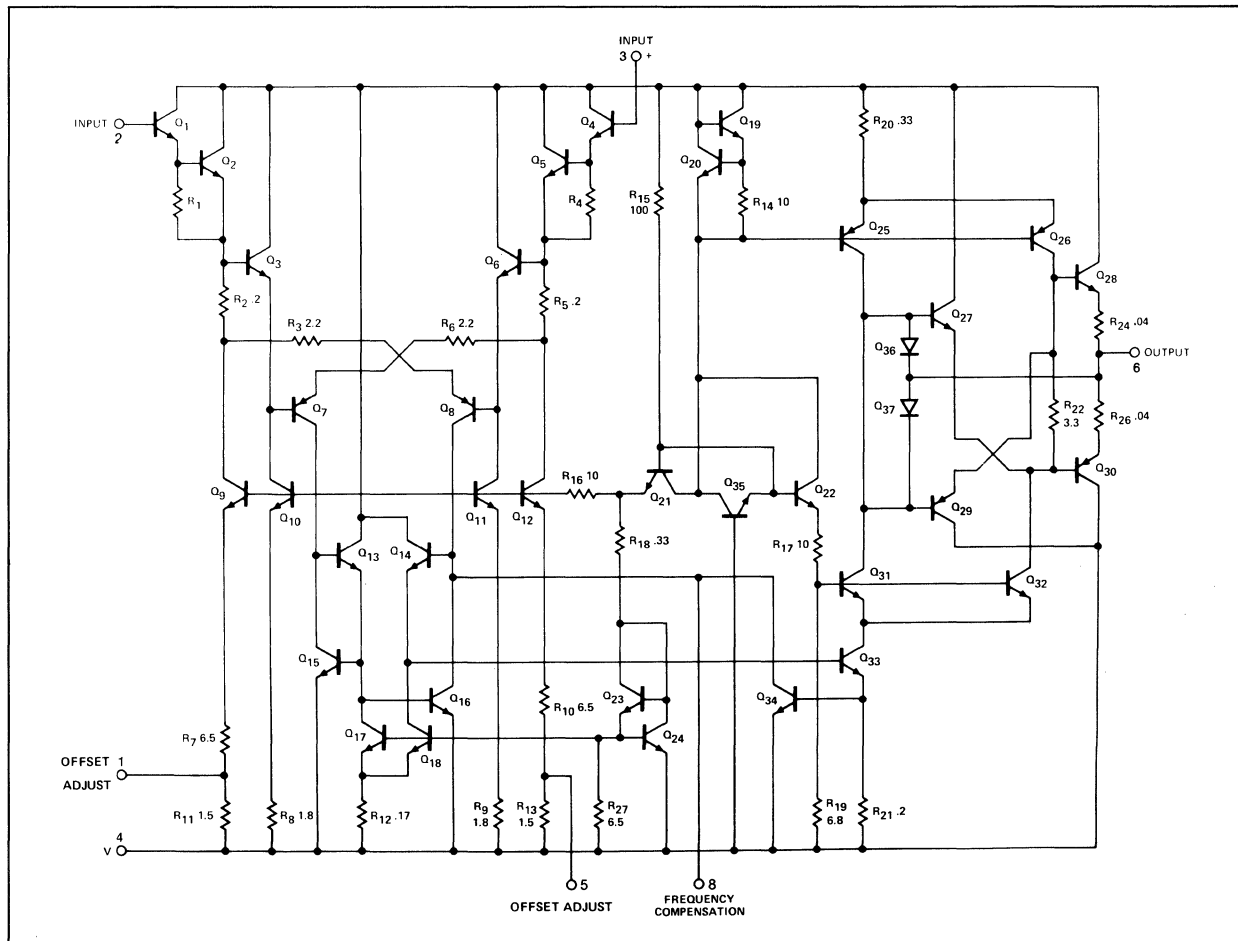
FEATURES

- 35V/ μ sec slew rate at unity gain
- Pin for pin replacement for μ A709, μ A748 or LM101
- Compensated with a single capacitor
- Same low drift offset null circuitry as μ A741
- Small signal bandwidth 1MHz
- Large signal bandwidth 500KHz
- True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation ¹	300	mW
Differential input voltage	±15	V
Common mode input voltage ²	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration ³	indefinite	

NOTES

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE531 ¹			NE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25^\circ C$ $R_S \leq 10k\Omega$, over temp		2.0	5.0 6.0		2.0	6.0 7.5	mV mV
I_{OS} Offset current	$T_A = 25^\circ C$ $T_A = HIGH$ $T_A = LOW$		30	200 200 500		50	200 200 300	nA nA nA
I_{BIAS} Input current	$T_A = 25^\circ C$ $T_A = HIGH$ $T_A = LOW$		300	500 500 1500		400	1500 1500 2000	nA nA nA
V_{CM} Common mode voltage range	$T_A = 25^\circ C$	±10			±10			V
CMRR Common mode rejection ratio	$T_A = 25^\circ C$, $R_S \leq 10k\Omega$ Over temp $R_S \leq 10k\Omega$	70	90		70	100		dB dB
R_{IN} Input resistance	$T_A = 25^\circ C$		20			20		MΩ
V_{OUT} Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC} Supply current	$T_A = 25^\circ C$ T_{MAX} $T_A = 25^\circ C$			7.0 7.0 210			10 10 300	mA mA mW
P_{SRR} Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25^\circ C$ $R_S \leq 10k\Omega$, over temp		10	150		10	150	μV/V μV/V
R_{OUT} Output resistance	$T_A = 25^\circ C$		75			75		Ω
A_{VOL} Large signal voltage gain	$T_A = 25^\circ C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$ $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	50 25	100		20 15	60		V/mV V/mV

NOTE

1. Temperature range:
SE531 -55°C ≤ T_A ≤ 125°C
NE531 0°C ≤ T_A ≤ 70°C

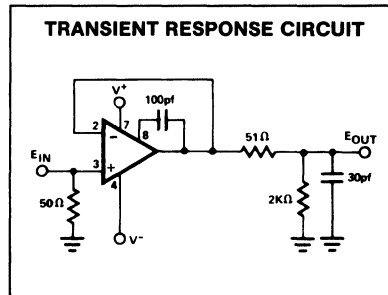
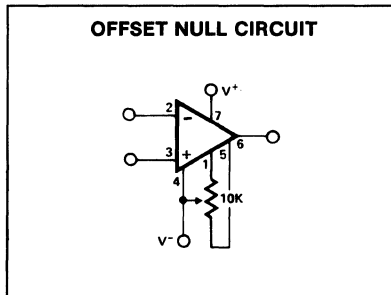
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1% (.01%))	$A_v = +1$, $V_{IN} = \pm 10\text{V}$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot	$A_v = +1$, $V_{IN} = \pm 10\text{V}$		2			2		%
Small signal overshoot	$A_v = +1$, $V_{IN} = 400\text{mV}$		5			5		%
Small signal risetime	$A_v = +1$, $V_{IN} = 400\text{mV}$		300			300		ns
Slew rate	$A_v = 100$		35			35		$\text{V}/\mu\text{s}$
	$A_v = 10$		35			35		$\text{V}/\mu\text{s}$
	$A_v = 1$ (noninverting)		30		20	30		$\text{V}/\mu\text{s}$
	$A_v = 1$ (inverting)		35		25	35		$\text{V}/\mu\text{s}$

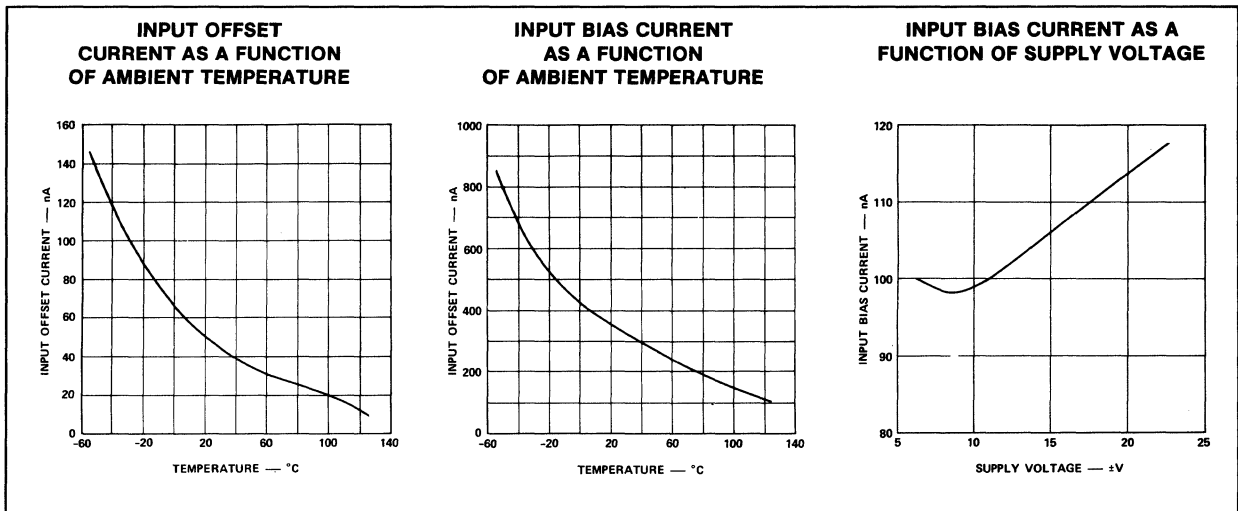
NOTE

1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

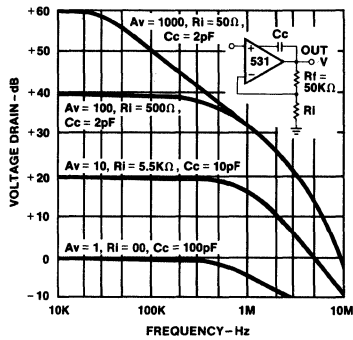


TYPICAL PERFORMANCE CHARACTERISTICS $(V_S = \pm 15\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.)

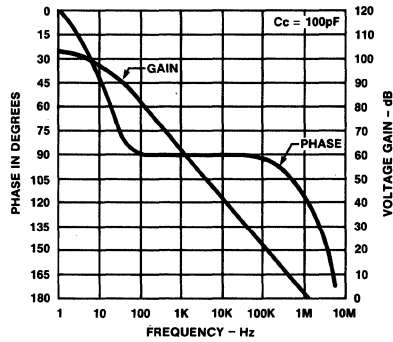


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

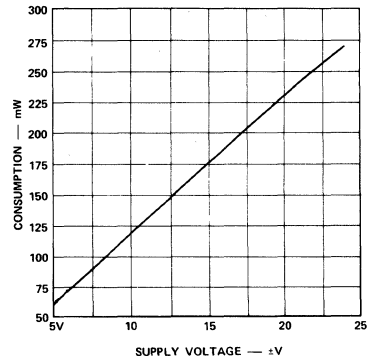
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



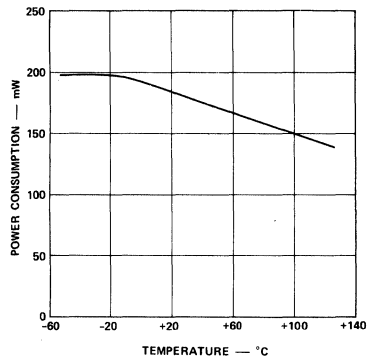
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



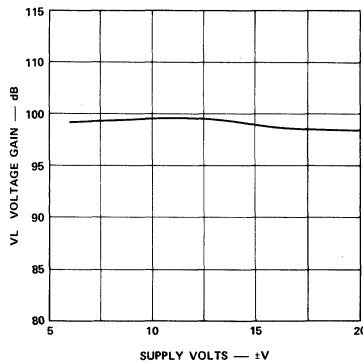
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



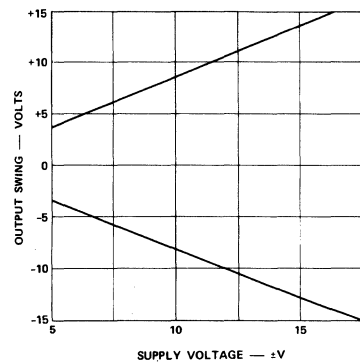
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



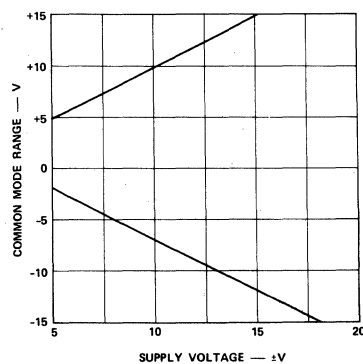
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



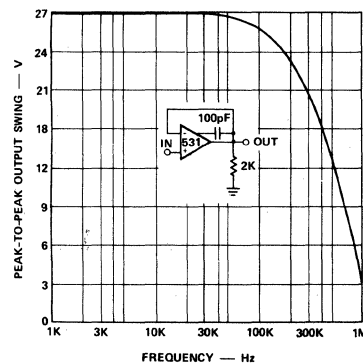
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



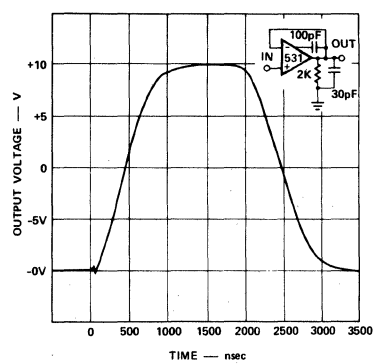
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



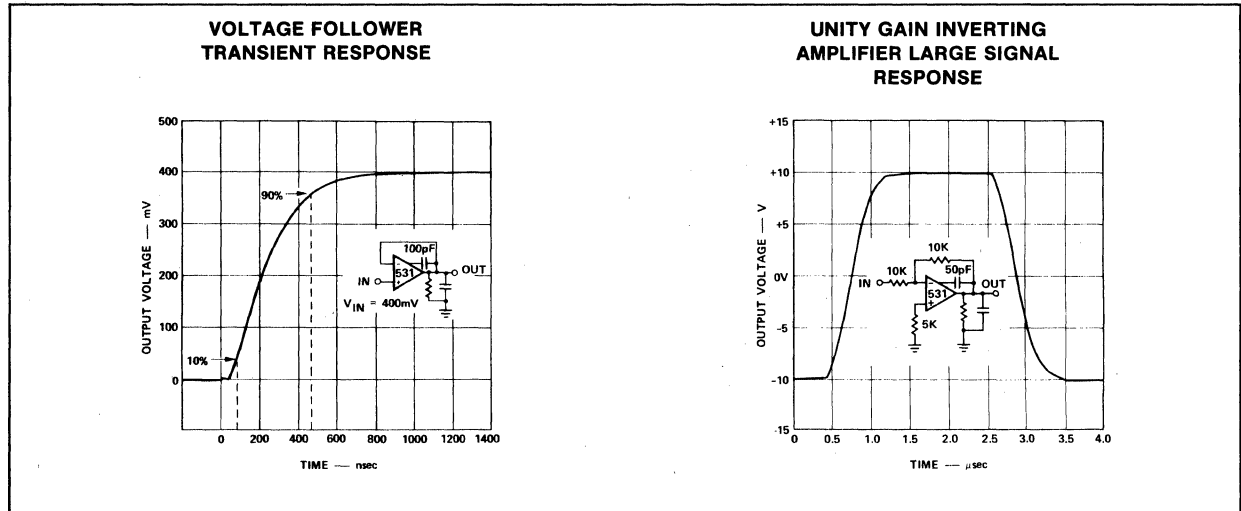
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



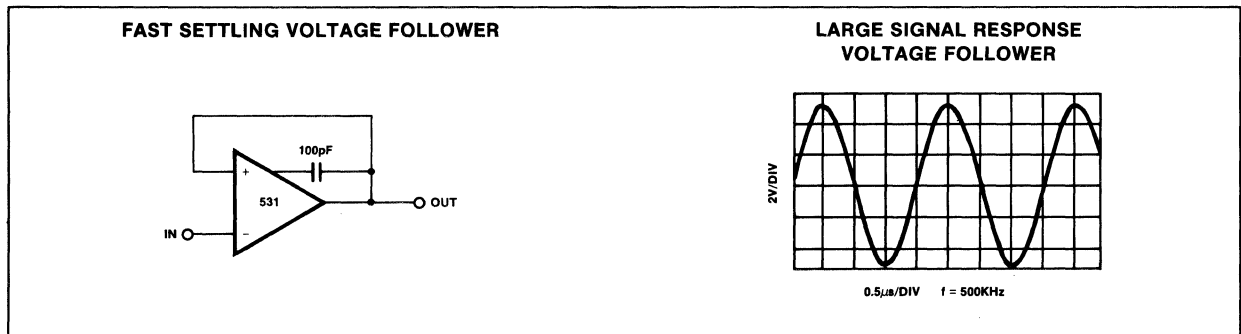
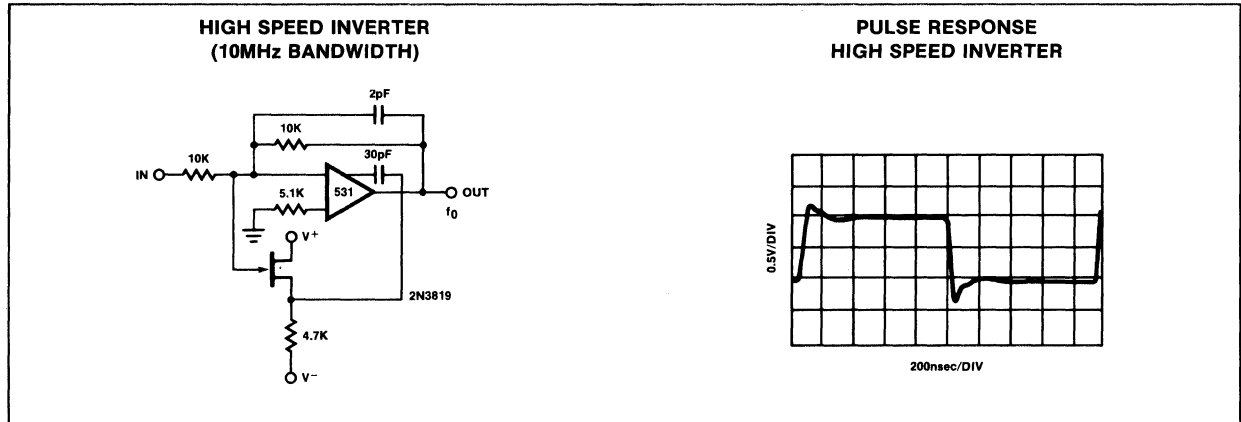
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

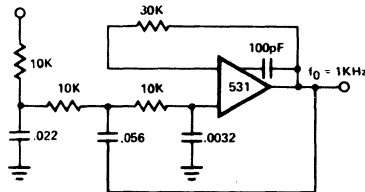


TYPICAL APPLICATIONS

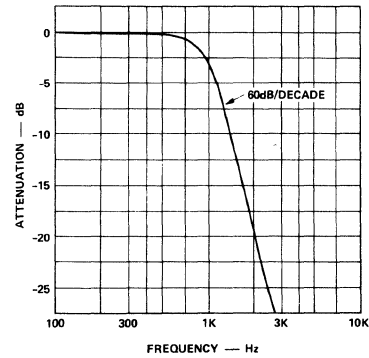


TYPICAL APPLICATIONS (Cont'd)

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



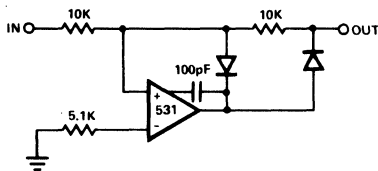
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



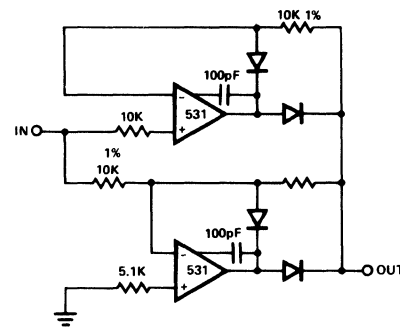
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

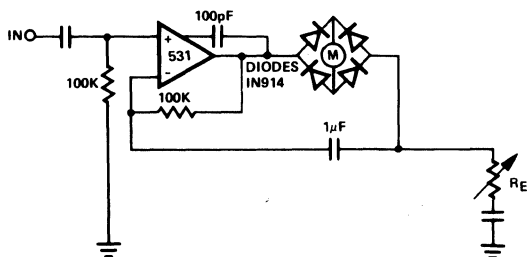
(a) HALF WAVE



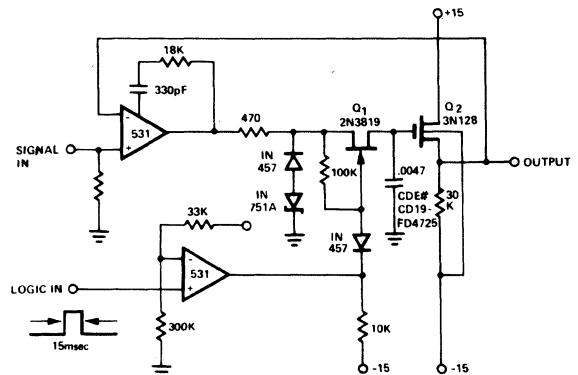
(b) FULL WAVE



AC MILLIVOLTMETER



SAMPLE AND HOLD



DUAL OPERATIONAL AMPLIFIER SINGLE OR DUAL POWER SUPPLY OPERATION

NE/SE/SA532
LM158/258/358

NE/SE532-N,H,FE/SA532-N
LM158/258/358-N,H,FE

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

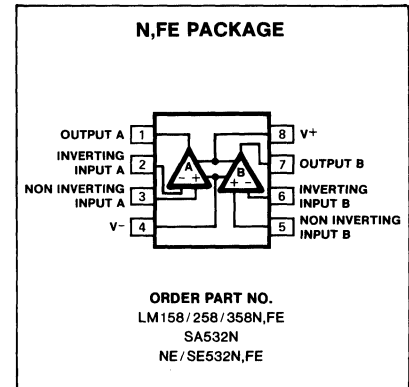
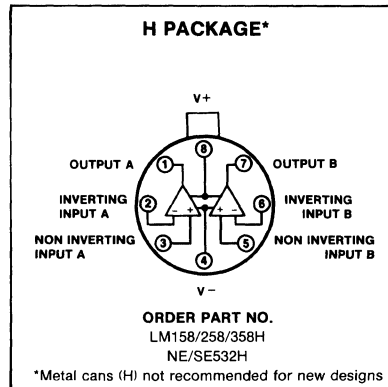
FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain—(100dB)
- Wide bandwidth (unity gain)—1MHz (temperature compensated)
- Wide power supply range
 - single supply—(3Vdc to 30Vdc)
 - or dual supplies—(± 1.5 Vdc to ± 15 Vdc)
- Very low supply current drain (400 μ A)—essentially independent of supply voltage (1mW/op amp at +5Vdc)
- Low input biasing current—(45nA dc temperature compensated)
- Low input offset voltage—(2mVdc) and offset current—(5nA dc)
- Differential input voltage range equal to the power supply voltage
- Large output voltage—(0Vdc to $V+$ —1.5Vdc swing)
- SE532 MII std 883A,B,C available

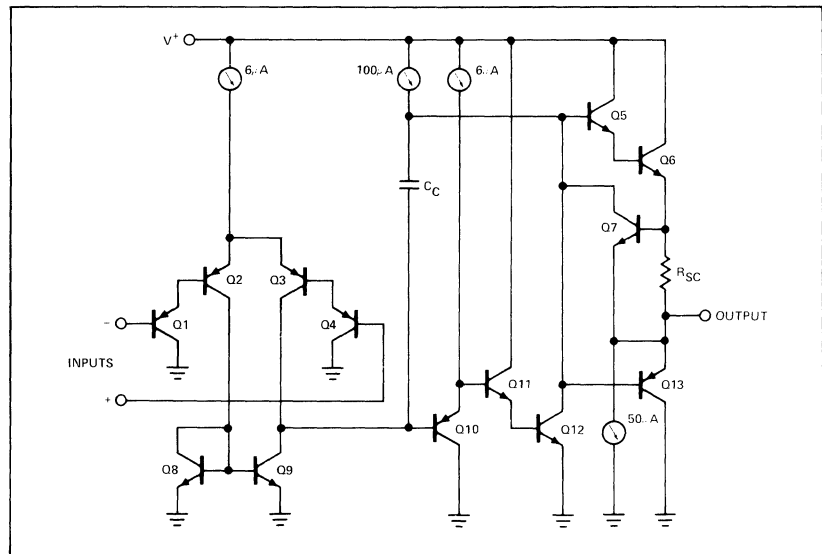
UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, $V+$	32 or ± 16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation ¹		
FE package	900	mW
H package	680	mW
N package	500	mW
Output short-circuit to GND ⁵ $V+ < 15$ Vdc and $T_A = 25^\circ\text{C}$	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	$^\circ\text{C}$
LM258	-25 to +85	$^\circ\text{C}$
SA532N	-40 to +85	$^\circ\text{C}$
SE532/LM158	-55 to +125	$^\circ\text{C}$
Storage temperature range	-65 to +150	$^\circ\text{C}$
Lead temperature (soldering, 10sec)	300	$^\circ\text{C}$

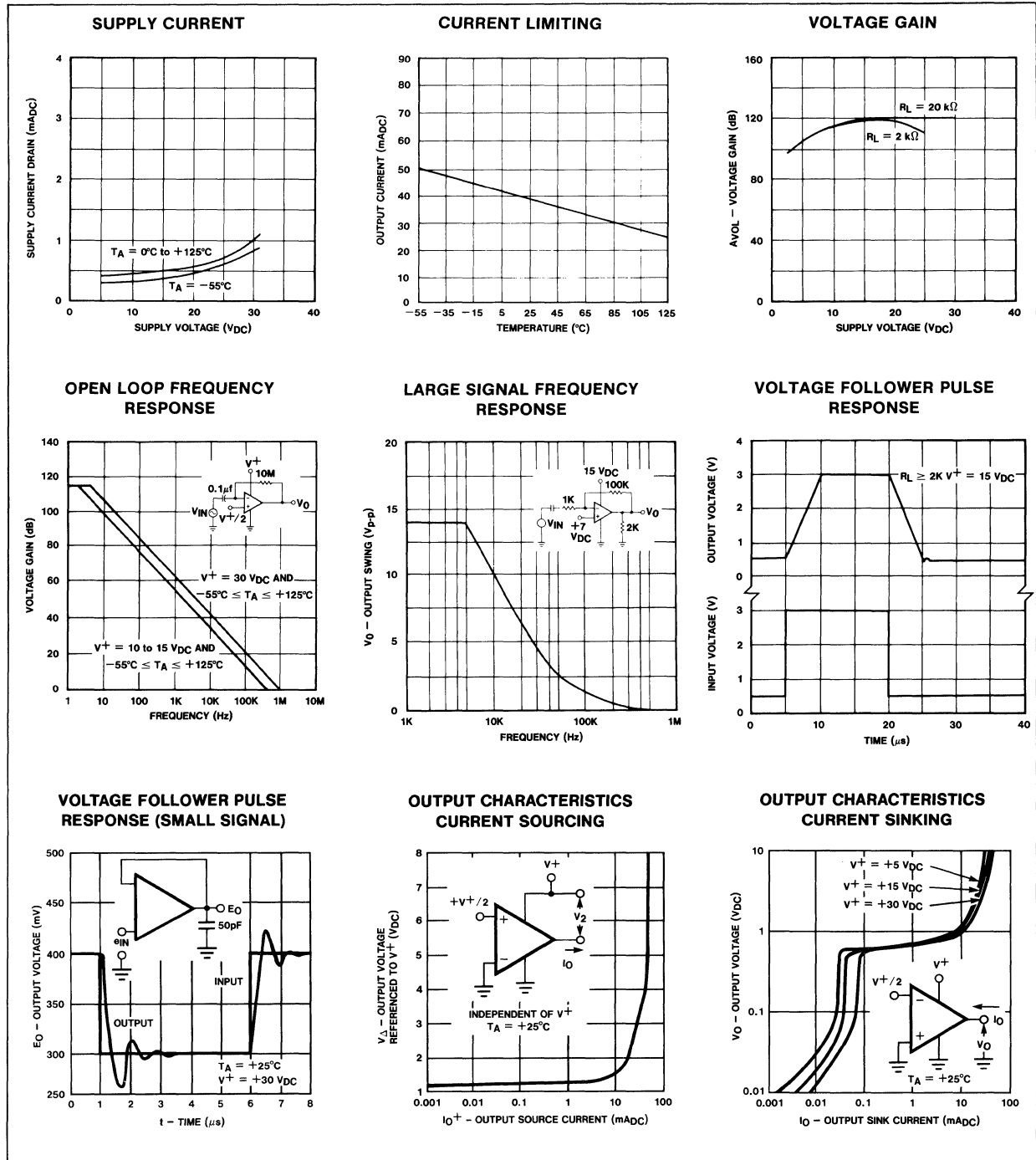
DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_+ = +5\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage ¹	$R_S \leq 0\Omega$ $R_S \leq 0\Omega$, over temp.		± 2	± 5 ± 7		± 2	± 7 ± 9	mV mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		$\mu\text{V}/^\circ\text{C}$
I_{OS} Offset current	$I_{IN(+)} - I_{IN(-)}$ Over temp.		± 3	± 30 ± 100		± 5	± 50 ± 150	nA nA
I_{OS} Drift			10			10		$\text{pA}/^\circ\text{C}$
I_{BIAS} Input current ²	$I_{IN(+)}$ or $I_{IN(-)}$ Over temp., $I_{IN(+)}$ or $I_{IN(-)}$		45 40	150 300		45 40	250 500	nA nA
V_{CM} Common mode voltage range ³	$V_+ = 30\text{V}$ Over temp., $V_+ = 30\text{V}$	0 0		$V_+ - 1.5$ $V_+ - 2.0$	0 0		$V_+ - 1.5$ $V_+ - 2.0$	V V
C_{MRR} Common mode rejection ratio		70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2\text{k}\Omega$, $V_+ = 30\text{V}$, over temp	26			26			V
V_{OUT} Output voltage swing (V_{OL})	$R_L \geq 10\text{k}\Omega$, $V_+ = 30\text{V}$, over temp $R_L \leq 10\text{k}\Omega$, over temp.	27	28 5	20	27	28 5	20	V mV
I_{CC} Supply current	$R_L = \infty$, $V_+ = 30\text{V}$ $R_L = \infty$ on all amplifiers, over temp		1.0 0.5	2.0 1.2		1.0 0.5	2.0 1.2	mA mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_{OUT} \pm 10\text{V}$, $V_+ = 15\text{V}$ (for large V_O swing) Over temp.	50 25	100		25 15	100		V/mV V/mV
$PSRR$ Supply voltage rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling ⁴	$f = 1\text{kHz}$ to 20kHz (input referred)		-120			-120		dB
Output current Source	$V_{IN+} = +1\text{Vdc}$, $V_{IN-} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$	20	40		20	40		mA
Sink	$V_{IN+} = +1\text{Vdc}$, $V_{IN-} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$, over temp.	10	20		10	20		mA
	$V_{IN-} = +1\text{Vdc}$, $V_{IN+} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$	10	20		10	20		mA
	$V_{IN-} = +1\text{Vdc}$, $V_{IN+} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$, over temp.	5	8		5	8		mA
	$V_{IN+} = 0\text{V}$, $V_{IN-} = +1\text{Vdc}$, $V_O = 200\text{mV}$	12	50		12	50		μA
I_{SC} Short circuit current ⁵			40	60		40	60	mA
Differential input voltage ⁶				V_+			V_+	V

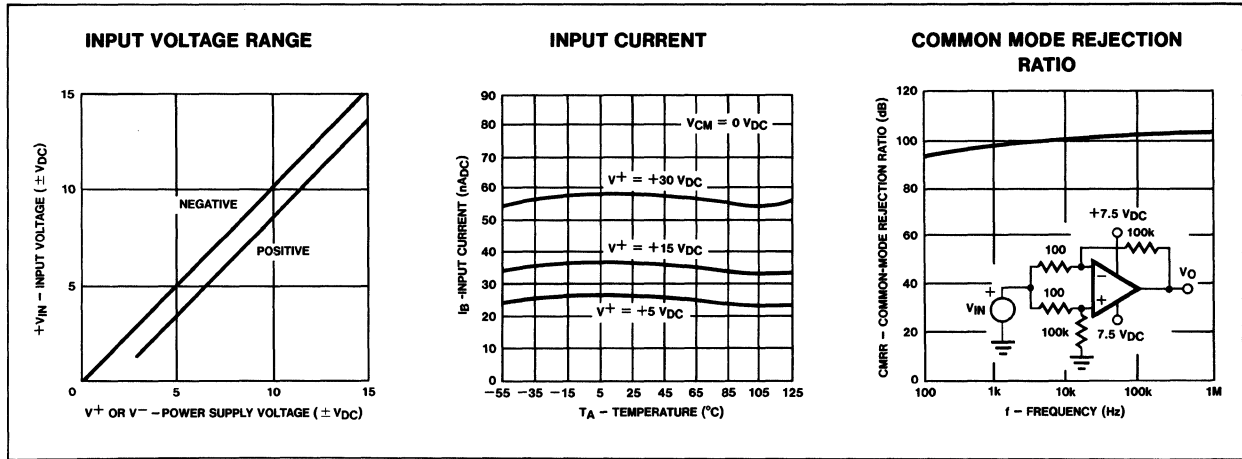
NOTES

- $V_O \approx 1.4\text{V}$, $R_S = 0\Omega$ with V_+ from 5V to 30V ; and over the full input common-mode range (0V to $V_+ - 1.5\text{V}$).
- The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V . The upper end of the common-mode voltage range is $V_+ - 1.5\text{V}$, but either or both inputs can go to $+32\text{V}$ without damage.
- Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_+ . At values of supply voltage in excess of $+15\text{Vdc}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V . The upper end of the common-mode voltage range is $V_+ - 1.5\text{V}$, but either or both inputs can go to $+32\text{Vdc}$ without damage.
- For operating at high temperatures, all devices must be derated based on a $+125^\circ\text{C}$ maximum junction temperature and a thermal resistance of $175^\circ\text{C}/\text{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



DESCRIPTION

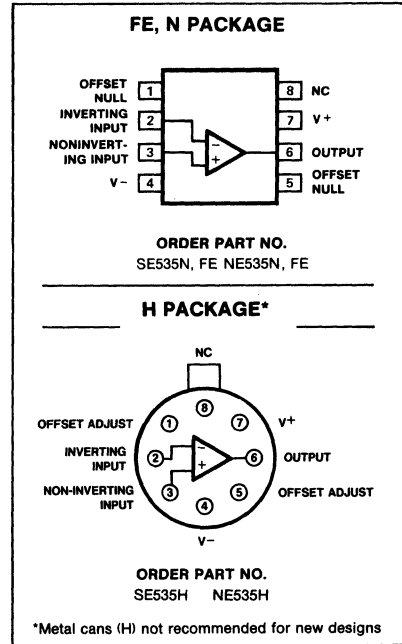
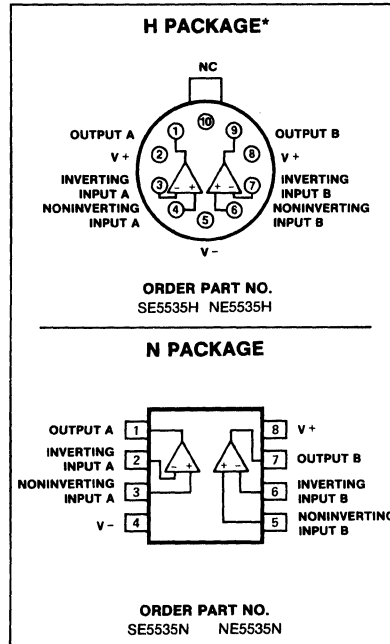
The 535 and 5535 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. The 535 is a single device while the 5535 is a dual configuration. Internally compensated for unity gain, the SE535 and SE5535 feature a guaranteed unity gain slew rate of $10V/\mu s$ with 2mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 741, 747 and 1558.

FEATURES

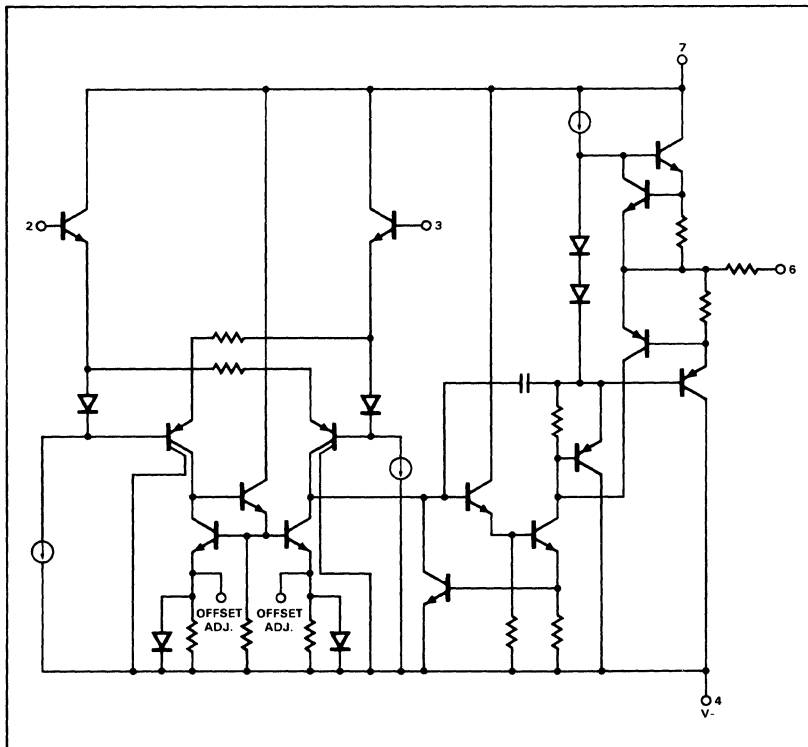
- $15V/\mu s$ unity gain slew rate
- Internal frequency compensation
- Low input offset voltage—2mV
- Low input bias current 80nA max
- Short circuit protected
- Offset null capability
- Large common mode and differential voltage ranges

	535	5535
• Pin out	741	747,1558
• Configuration	Single	Dual

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC (One Amplifier)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SE535/ SE5535	NE535/ NE5535	UNIT
Supply voltage	±22	±18	V
Internal power dissipation ¹			
N Package	500	500	mW
H Package	800	800	mW
F Package	1000	1000	mW
Differential input voltage	±30	±30	V
Input voltage ²	±15	±15	V
Operating temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (solder, 60sec)	300	300	°C
Output short circuit ³	Indefinite	Indefinite	

NOTES

- Rating applies for thermal resistances junction to ambient of 240°C/W and 150°C/W for N and H packages, respectively. Maximum chip temperature is 150°C.
- For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V unless otherwise specified.*

PARAMETER	TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Input offset voltage	R _S ≤ 10kΩ R _S ≤ 10kΩ, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV _{OS} Input offset voltage drift	R _S = 0Ω, over temp.		4.0			6.0		μV/°C
I _{OS} Input offset current	Over temp.		5	20 40		15	40 80	nA VnA
I _B Input current	Over temp.		45	80 200		65	150 200	nA nA
V _{CM} Common mode voltage range		±12	±13		±12	±13		V
CMRR Common mode rejection ratio	R _S ≤ 10kΩ, over temp.	70	90		70	90		dB
PSRR Power supply rejection	R _S ≤ 10kΩ, over temp.		30	150		30	150	μV/V
R _{IN} Input resistance		3	10		1	6		MΩ
A _{VOL} Large signal voltage gain	R _L ≥ 2kΩ, V _{OUT} = ±10V R _L ≥ 2kΩ, V _{OUT} = ±10V, over temp.	50	500		50	500		V/mV V/mV
V _{OUT} Output voltage	R _L ≥ 2kΩ, over temp. R _L ≥ 10kΩ, over temp.	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I _{CC} Supply current	Per amplifier Per amplifier, over temp.		1.8 2	2.8 3.3		1.8 2	2.8 3.3	mA mA
P _D Power dissipation	Per amplifier Per amplifier, over temp.		54 60	84 99		54 60	84 99	mW mW
I _{SC} Output short circuit current			25			25		mA
R _{OUT} Output resistance			100			100		Ω

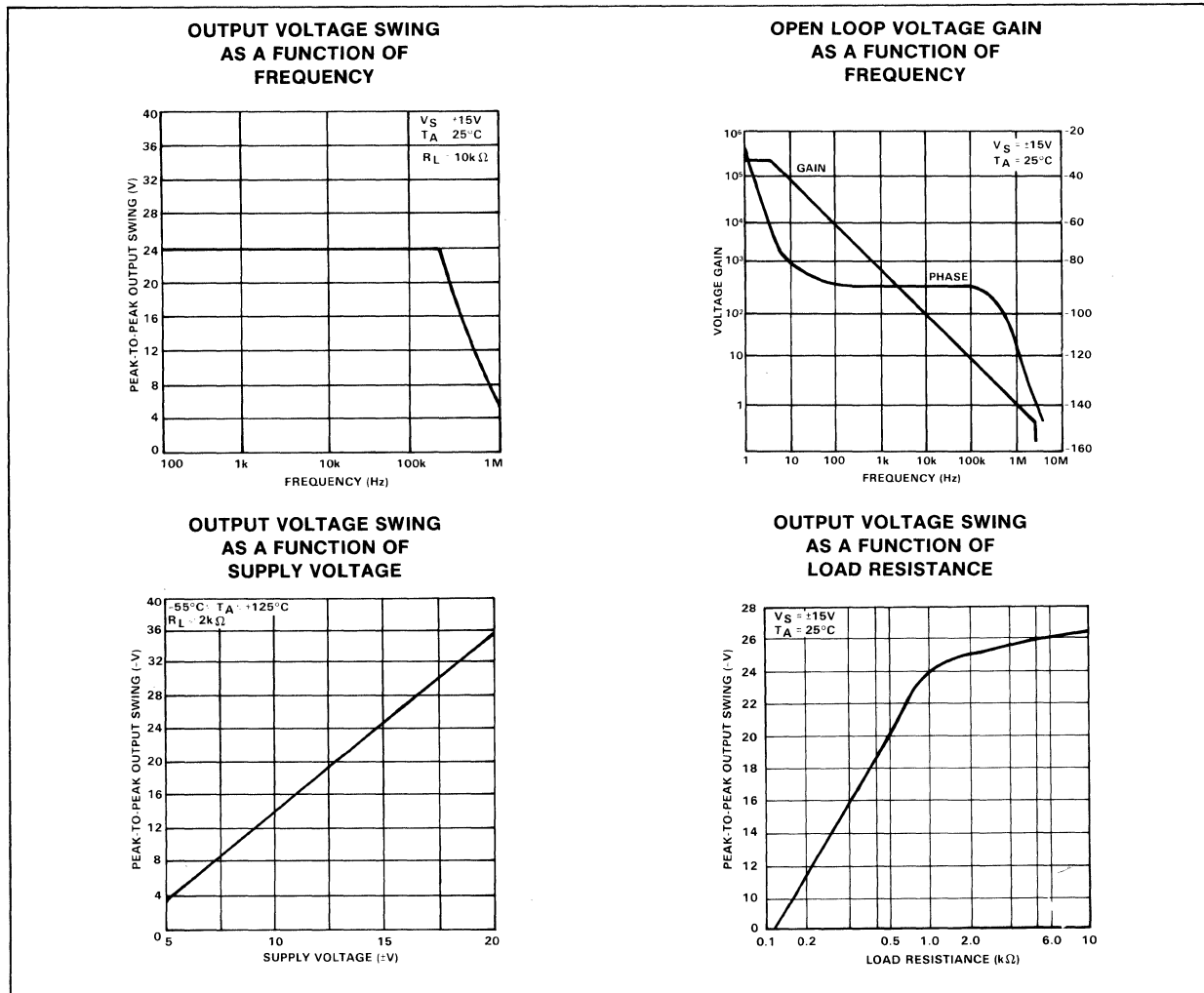
*NOTE

Temperature range
SE types -55°C ≤ T_A ≤ 125°C
NE types 0°C ≤ T_A ≤ 70°C

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

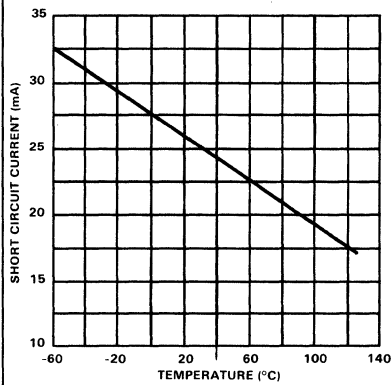
PARAMETER	TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain/bandwidth product			1			1		MHz
Transient response			0.25			0.25		μs
Small signal rise time			6			6		%
Small signal overshoot			3			3		μs
Settling time			15			15		$\text{V}/\mu\text{s}$
Slew rate	$T_0 = 0.1\%$ $T_A = 25^\circ\text{C}, R_L \geq 10\text{k}\Omega$, unity gain, non-inverting	10			10			

TYPICAL PERFORMANCE CHARACTERISTICS

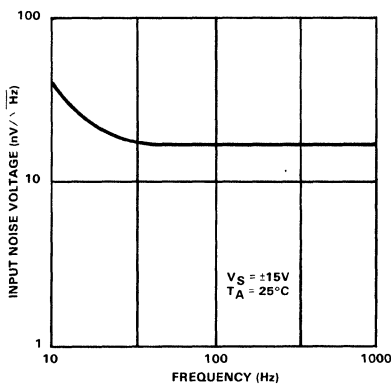


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

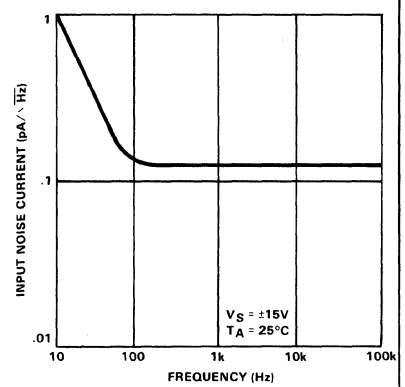
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



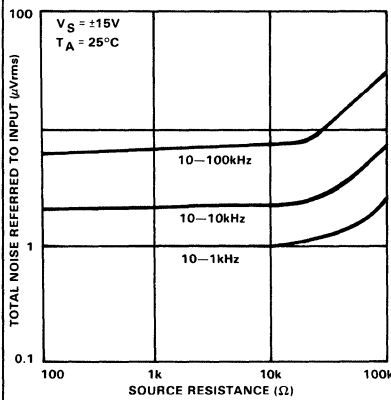
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



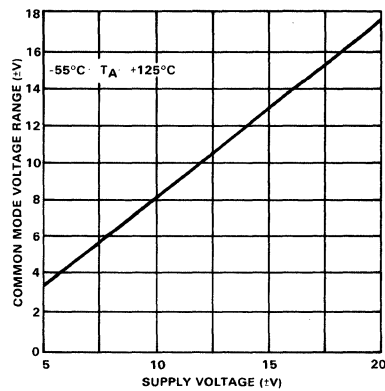
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



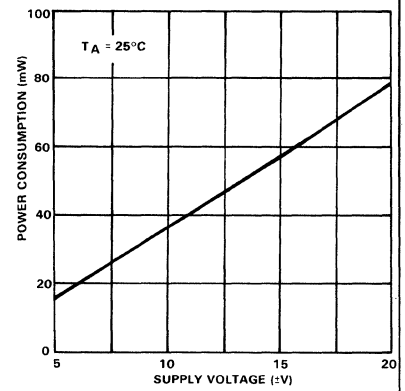
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



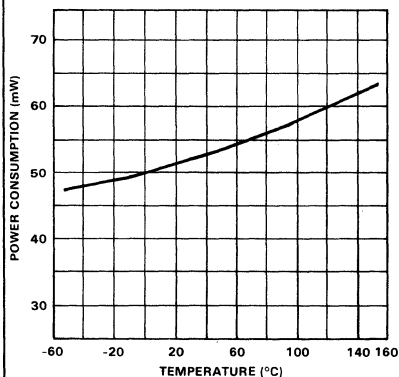
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



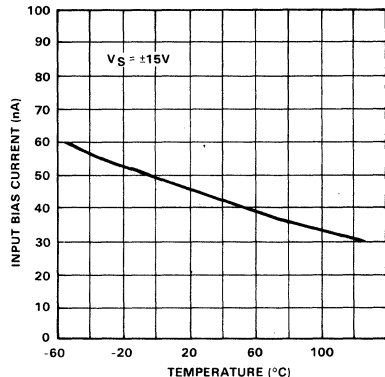
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



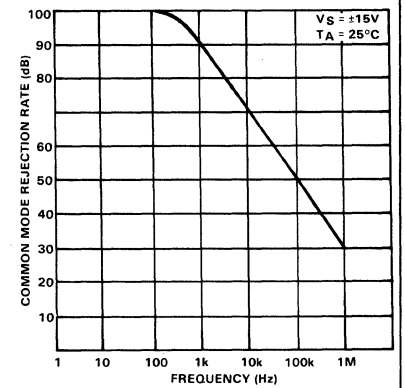
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



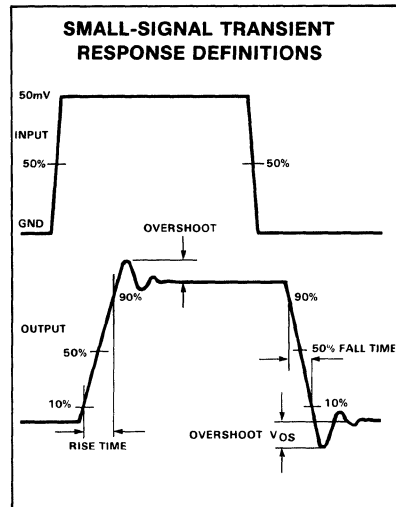
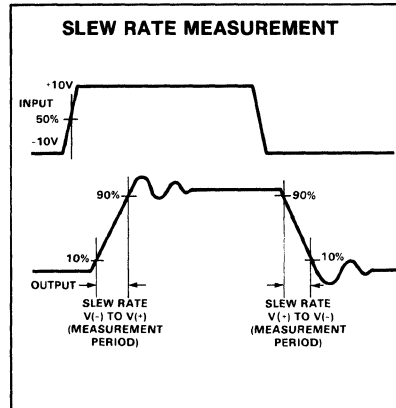
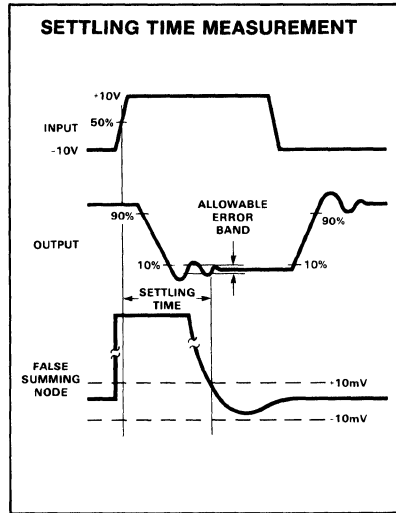
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



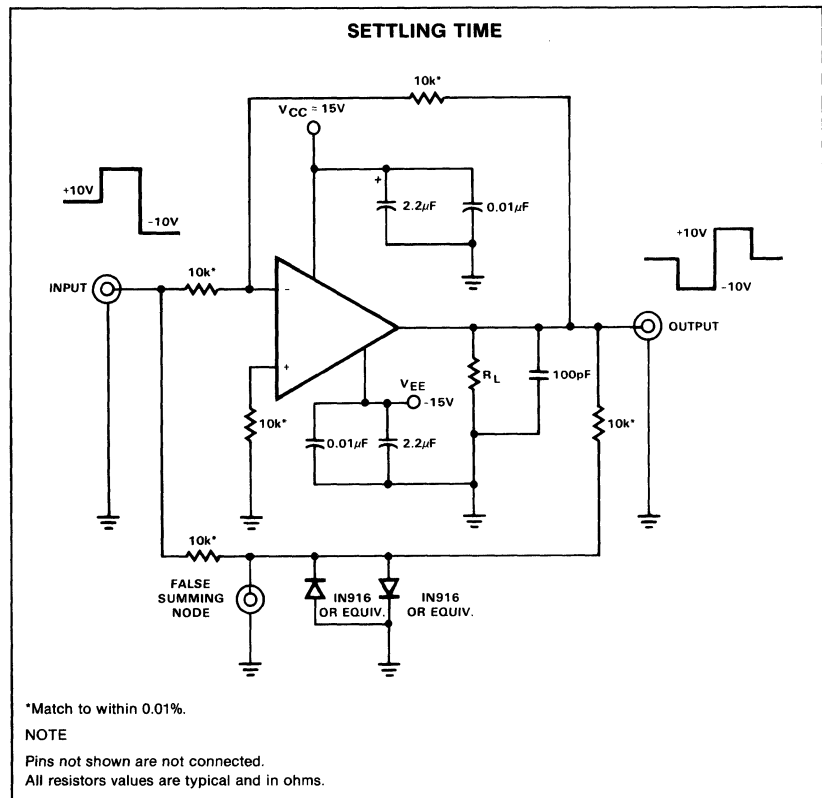
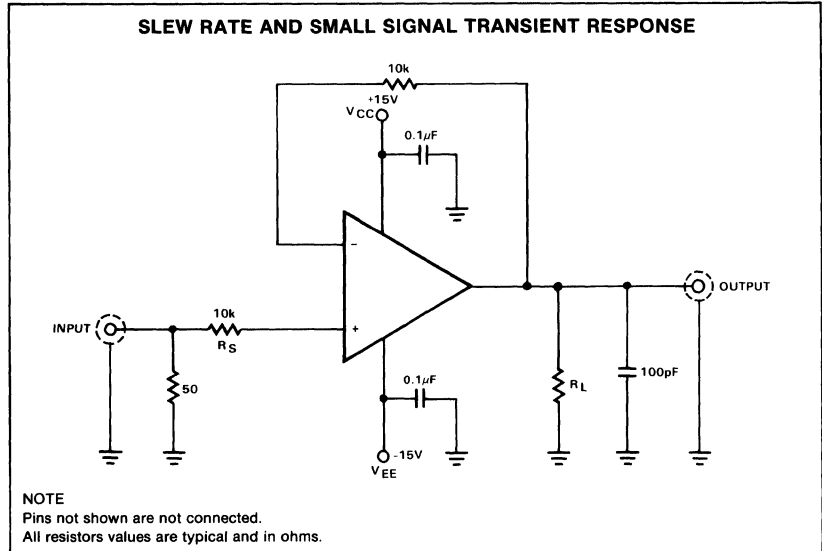
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



VOLTAGE WAVEFORMS



TEST CIRCUITS



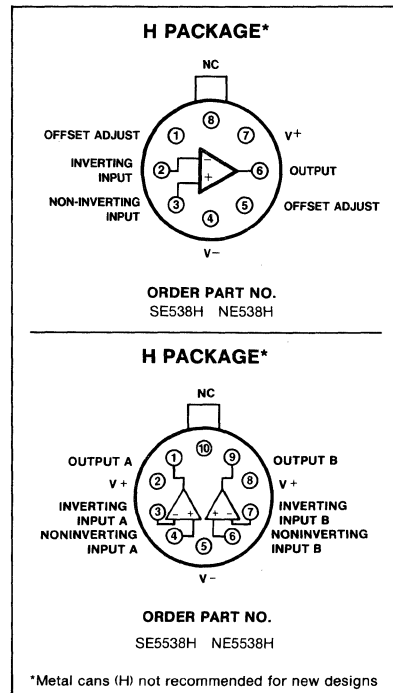
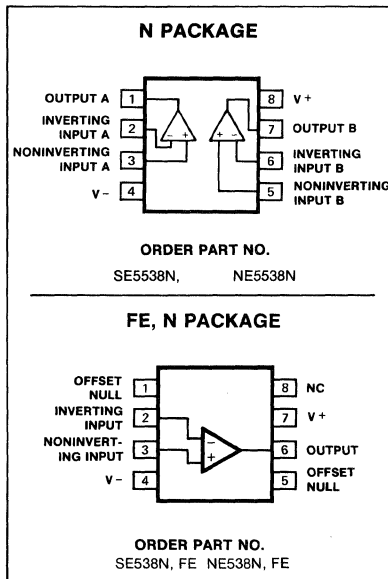
DESCRIPTION

The NE/SE538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/5538 offers guaranteed minimum slew rates of 40V/μs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- 2mV input offset voltage
- 80nA max input offset current
- Short circuit protected
- Offset null capability
- Large common mode and differential voltage ranges
- 60V/μs slew rate (gain of +5, -4 min)
- 6MHz gain bandwidth product (gain +5, -4 minimum)
- Internal frequency compensation (gain of +5, -4 minimum)
- Pin out: 538 same as 741 (single)
5538 same as 747, 1458 (dual)

PIN CONFIGURATIONS



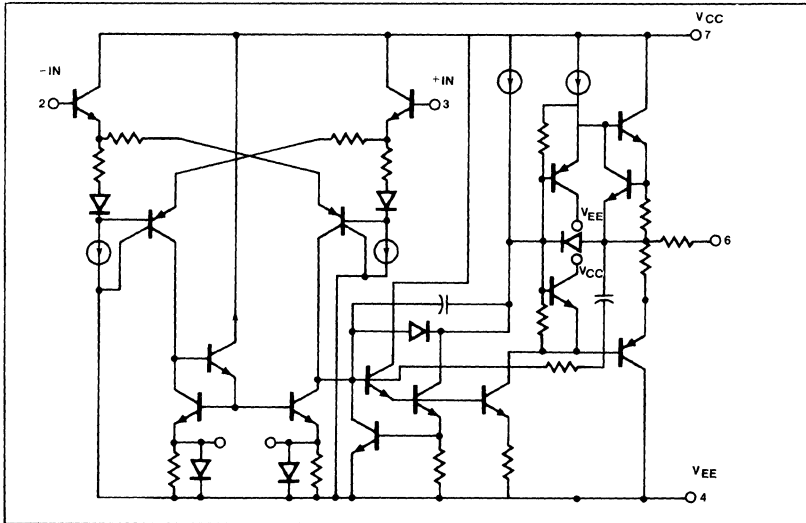
ABSOLUTE MAXIMUM RATINGS^{1,2,3}

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	±22	V
SE military grade	±18	V
NE commercial grade	±15	V
P _D Internal power dissipation	1000	mW
FE package		
P _D Internal power dissipation ¹	500	mW
N package		
P _D Internal power dissipation ¹	800	mW
H package		
Differential input voltage	±30	V
Input voltage ²	±15	V
Operating temperature range		
SE military grade	-55 to +125	°C
NE commercial grade	0 to 70	°C
Output short circuit ³	indefinite	
Storage temperature range	-65 to +150	°C
Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and H packages. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage	$R_S \leq 10\text{k}\Omega$ $R_S \leq 10\text{k}\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS} Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		$\mu\text{V}/^\circ\text{C}$
I_{OS} Input offset current	Over temp.		5	20 40		15	40 80	nA nA
I_B Input current	Over temp.		45	80 200		65	150 200	nA nA
V_{CM} Input common mode voltage range		± 12	± 13		± 12	± 13		V
$CMRR$ Common mode rejection ratio	$R_S \leq 10\text{k}\Omega$, over temp.	70	90		70	90		dB
$PSRR$ Power supply rejection	$R_S \leq 10\text{k}\Omega$, over temp.		30	150		30	150	$\mu\text{V}/\text{V}$
R_{IN} Input resistance		3	10		1	6		$\text{M}\Omega$
A_{VOL} Large signal voltage gain	$R_L \geq 2\text{k}\Omega$, $V_{OUT} = \pm 10\text{V}$ Over temp., $R_L \geq 2\text{k}\Omega$, $V_{OUT} = \pm 10\text{V}$	50 25	200		50 25	200		V/mV V/mV
V_{OUT} Output voltage	Over temp., $R_L \geq 2\text{k}\Omega$ Over temp., $R_L \geq 10\text{k}\Omega$	± 10 ± 12	± 13 ± 14		± 10 ± 12	± 13 ± 14		V V
I_{CC} Supply current	Per amplifier Over temp., per amplifier		2 2.2	3 3.6		2 2.2	3	mA mA
P_D Power dissipation	Per amplifier Over temp., per amplifier		60 66	90 108		60 66	90	mW mW
I_{SC} Output short circuit current			25			25		mA
R_{OUT} Output resistance			100			100		Ω

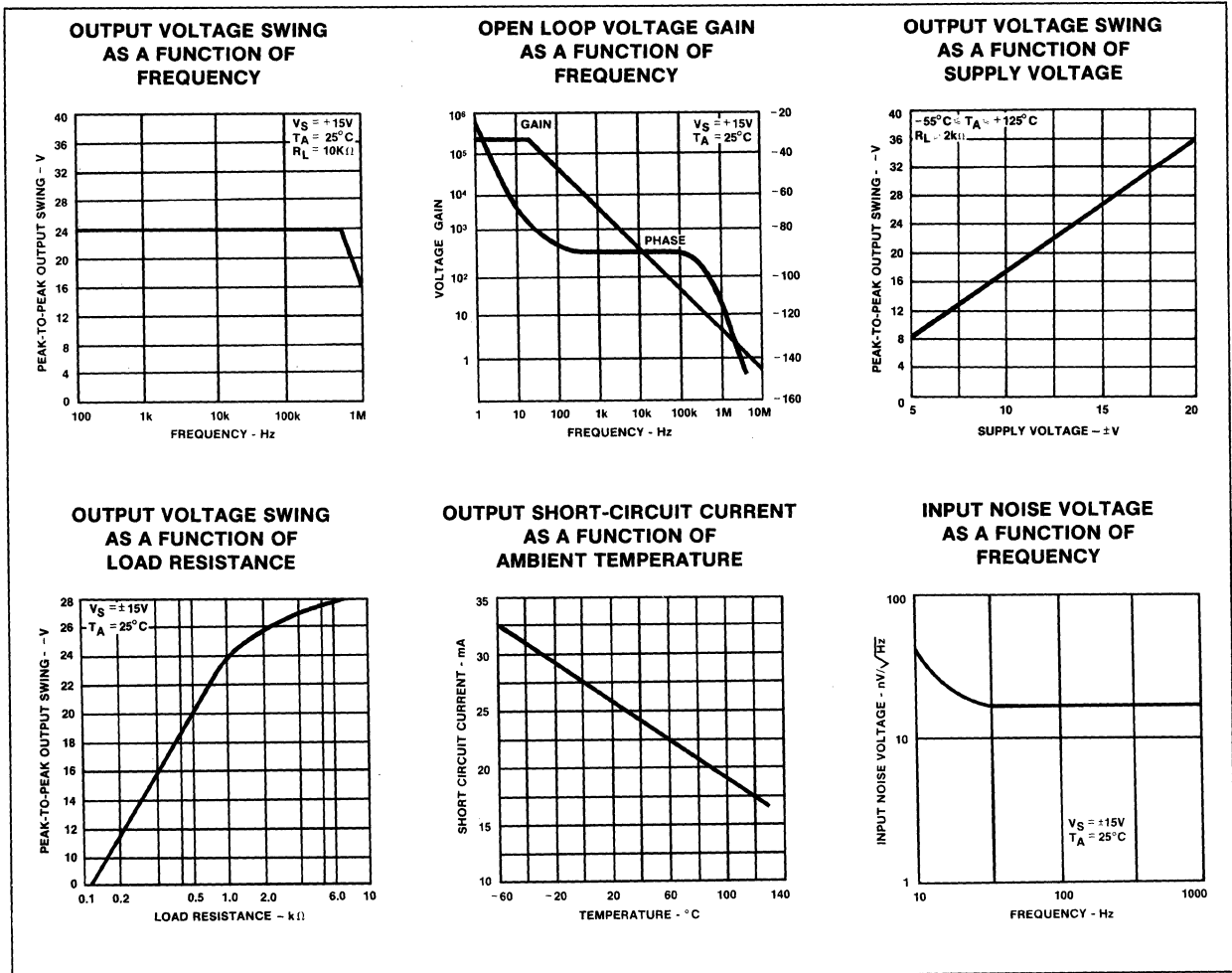
NOTE

Temperature Range
SE Types $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$
NE Types $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

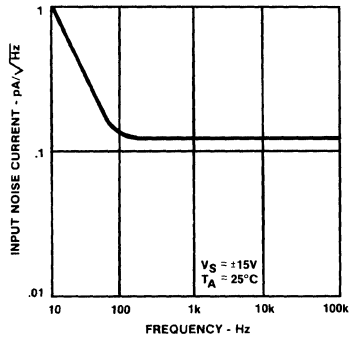
PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			0.25 6			0.25 6		μs %
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2\text{k}\Omega$	40	60			60		$\text{V}/\mu\text{s}$

TYPICAL PERFORMANCE CHARACTERISTICS

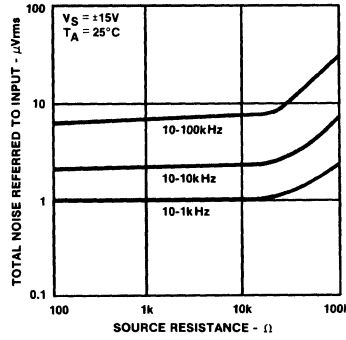


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

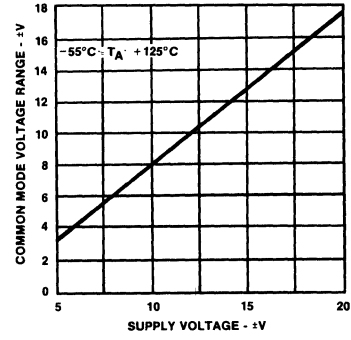
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



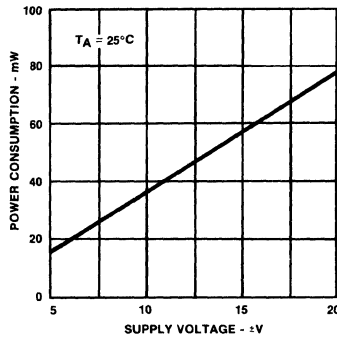
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



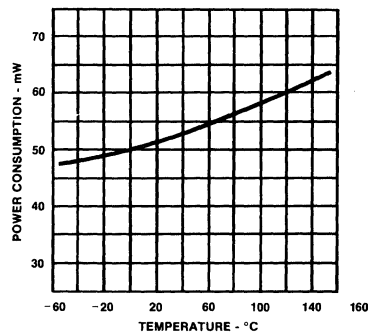
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



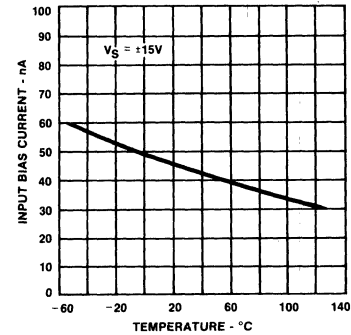
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



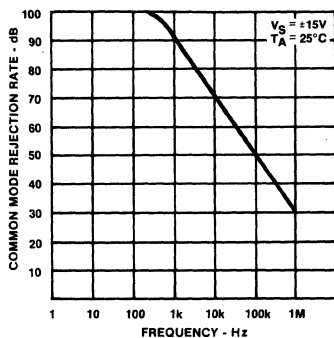
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



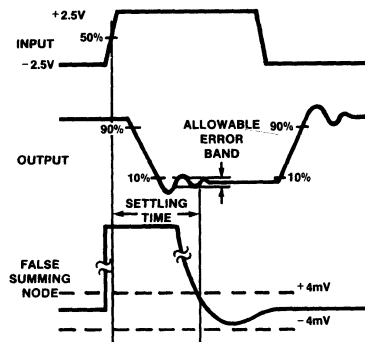
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



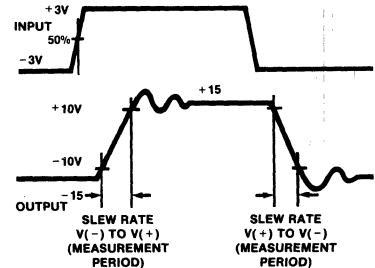
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



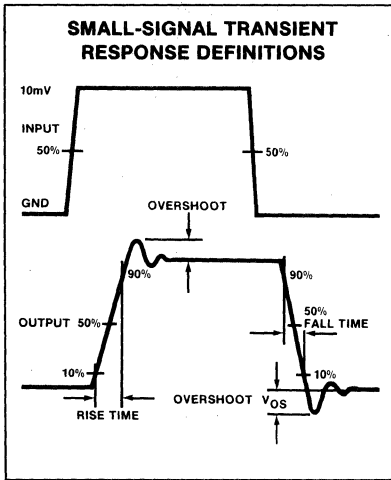
SETTLING TIME MEASUREMENT WAVEFORMS



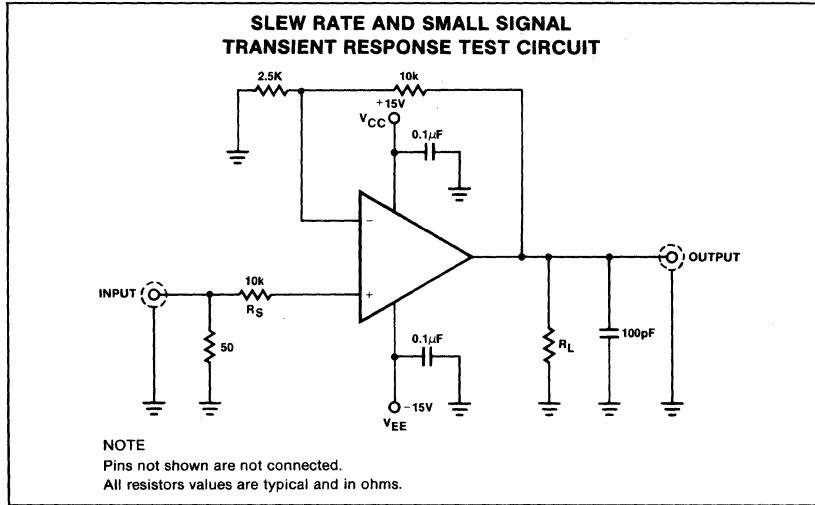
SLEW RATE MEASUREMENT VCC = ±20V



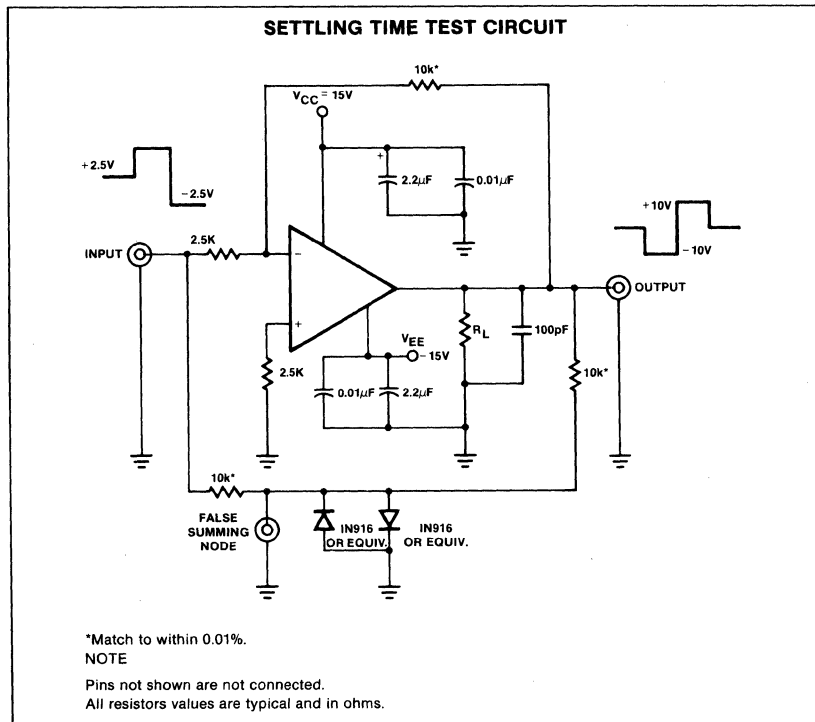
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TEST LOAD CIRCUITS



TEST LOAD CIRCUITS (Cont'd)



DESCRIPTION

The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

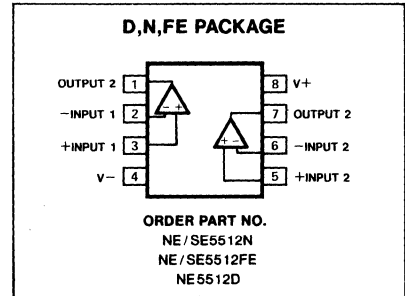
APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation applications

FEATURES

- Low input bias $< \pm 3nA$
- Low input offset current $< \pm 3nA$
- Low input offset voltage $< 1mV$
- Low V_{OS} temperature drift $4\mu V/^{\circ}C$
- Low input bias temperature drift $30pA/^{\circ}C$
- Low input voltage noise $25nV/\sqrt{Hz}$
- Low supply current $1.5mA/amp$
- High slew rate $1.0V/\mu s$
- High CMRR 100dB
- High input impedance $100M\Omega$
- High PSRR 110dB
- High differential input voltage limit
- No cross-over distortion
- Indefinite output short circuit protection
- Internally compensated for unity gain

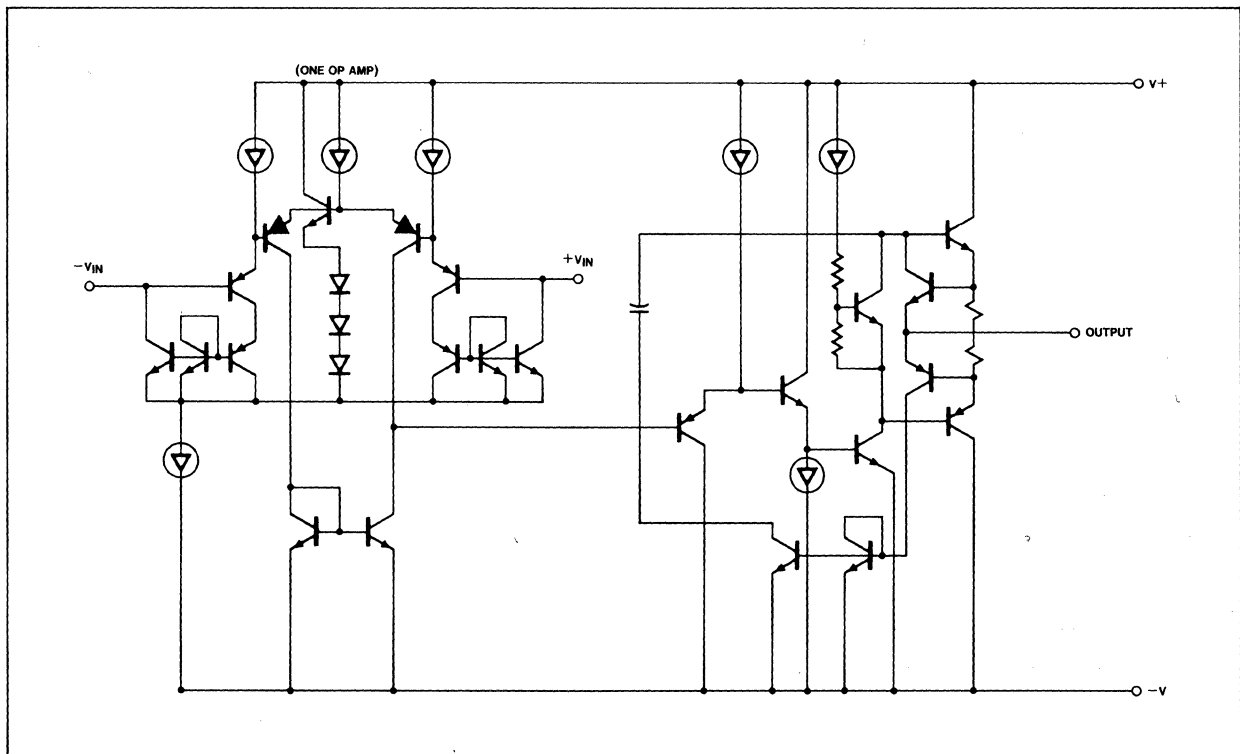
PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC} Supply Voltage	± 16	V
V_D Power dissipation	500	mW
T_A Operating temperature range	0 to 70	$^{\circ}C$
	-55 to +125	$^{\circ}C$
T_{STG} Storage temperature range	-65 to +150	$^{\circ}C$
T_{SOLD} Lead temperature soldering	300	$^{\circ}C$

EQUIVALENT SCHEMATIC



ELECTRICAL PERFORMANCE CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = $-55^{\circ}C$ to $+125^{\circ}C$ (SE), $0^{\circ}C$ to $+70^{\circ}C$ (NE)

PARAMETER	TEST CONDITIONS	SE5512			NE5512			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS}	Input offset voltage $R_S = 100\Omega$ $T_A = +25^{\circ}C$ $T_A = F.R.$		0.7 1	1.5 2.5		1 1.5	3 4	mV
I _{OS}	Input offset current $R_S = 100k\Omega$ $T_A = +25^{\circ}C$ $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
I _B	Input bias current $R_S = 100k\Omega$ $T_A = +25^{\circ}C$ $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
R _{IN}	Input resistance Differential $T_A = 25^{\circ}C$		100			100		M Ω
V _{CM}	Input common mode range $T_A = 25^{\circ}C$ $T_A = F.R.$	± 13.5 ± 13	± 13.7 ± 13.2		± 13.5 ± 13	± 13.7 ± 13.2		V
CMRR	Input common-mode rejection ratio $V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ (RM) $T_A = 25^{\circ}C$ $V_{IN} = \pm 13V$ (F.R.) $T_A = F.R.$	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain $R_L = 2k\Omega$ $T_A = 25^{\circ}C$ $V_O = \pm 10V$ $T_A = F.R.$	50 25	200		50 25	200		V/mV
S.R.	Slew rate $T_A = 25^{\circ}C$	0.6	1			1		V/ μ s
GBW	Small-signal unity gain bandwidth $T_A = 25^{\circ}C$		1			1		MHz
θ_M	Phase margin $T_A = 25^{\circ}C$		45			45		Degree
V _{OUT}	Output voltage swing $R_L = 2k\Omega$ $T_A = 25^{\circ}C$ $T_A = F.R.$	± 13 ± 12.5	± 13.5 ± 13		± 13 ± 12.5	± 13.5 ± 13		V
V _{OUT}	Output voltage swing $R_L = 600\Omega^*$ $T_A = 25^{\circ}C$ $T_A = F.R.$	± 10 ± 8	± 11.5 ± 9		± 10 ± 8	± 11.5 ± 9		V
I _{CC}	Power supply current $R_L = \text{Open}$ $T_A = 25^{\circ}C$ $T_A = F.R.$		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
PSRR	Power supply rejection ratio $T_A = 25^{\circ}C$ $T_A = F.R.$	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling $f = 1kHz$ to $20kHz$ $T_A = 25^{\circ}C$		-120			-120		dB
HD	Total harmonic distortion $f = 10kHz$ $T_A = 25^{\circ}C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V _{INN}	Input noise voltage $f = 1kHz$ $T_A = 25^{\circ}C$		30			30		nV/ \sqrt{Hz}
I _{INN}	Input noise current $f = 1kHz$ $T_A = 25^{\circ}C$.2			.2		pA/ \sqrt{Hz}

NOTE

* For operation at elevated temperature, N package must be derated based on a thermal resistance of 120°/W junction to ambient. Thermal resistance of the FE package is 125°/W.

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a possible solution to these general requirements (Figure 1).

For $V_S = 10$ volts, the common mode voltage is approximately +5 volts, well within the common mode limits of the NE5512.

The sensitivity of the input stage is approximately

$$\frac{RF \cdot V_S}{2R}$$

to a change in transducer resistance ΔR . This gives a gain factor of ≈ 50 for $V_S = 10V$ and $R = 25k\Omega$. The second stage gain is $\times 100$ giving a total gain of ≈ 5000 .

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common mode noise rejection is particularly important making matched differential impedance critical. The NE5512 typically provides 100dB of common mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	$\frac{\Delta R}{R}$	$\frac{\Delta E_{out}}{E_{in}}$
leg 1	10Ω	-2.6V
	5Ω	-1.3V
leg 2	10Ω	+2.4
	5Ω	+1.2

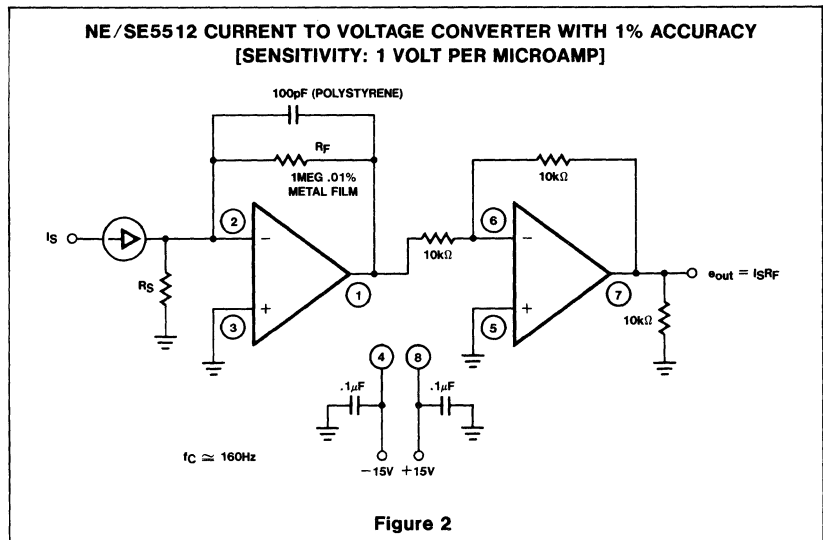
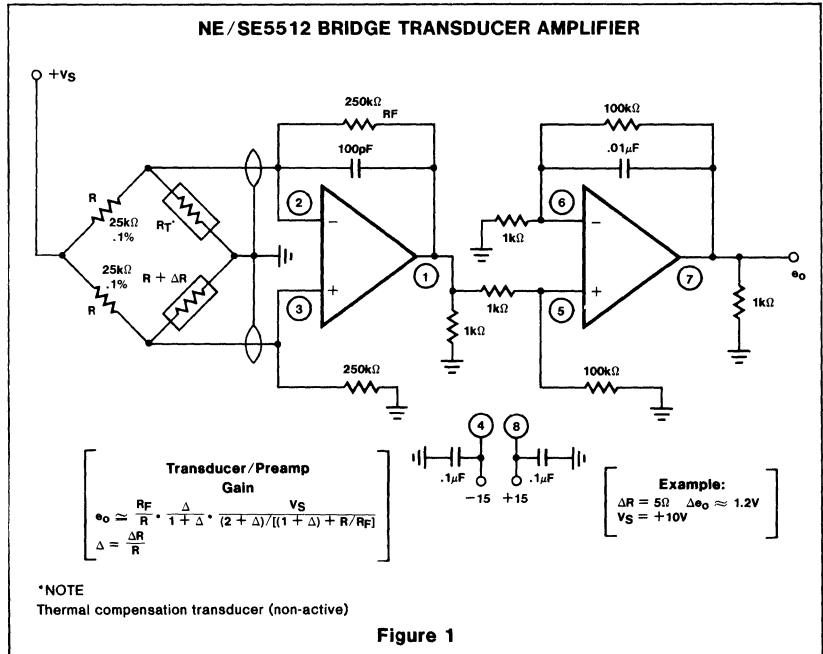
Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT TO VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current to voltage converter as shown below (Figure 2).

The lower limit of measuring accuracy is determined by I_B (inverting) which is typically 6nA. In order to attain a measurement accu-



racy of 1% the following inequality must hold,

$$I_B \leq (.01) I_{Smin}$$

Where I_B = input bias current, I_{Smin} = minimum measured current. For $I_B = 6nA$ and $I_{Smin} = 1\mu A$,

$$6nA \leq (.01) 1\mu A = 10nA$$

and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≈ 1 for $R_S \gg R_F$.

The measured results for this circuit appear below ($V_{CC} = \pm 15$ volts).

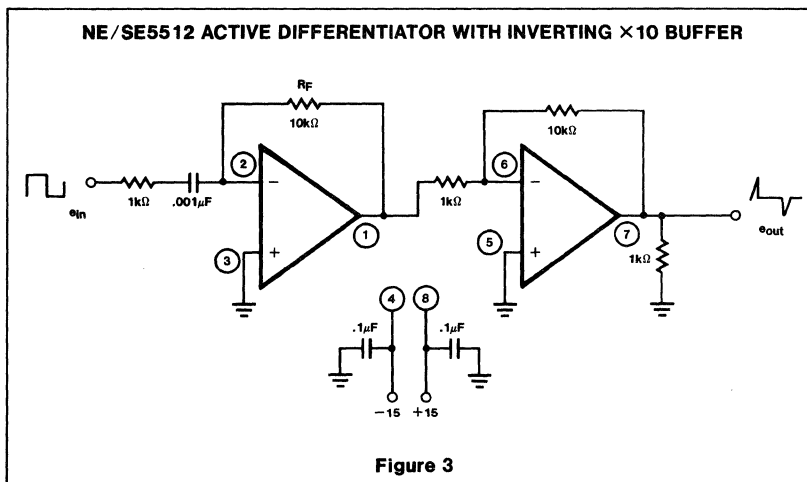
INPUT CURRENT	OUTPUT VOLTAGE
$1\mu A$	1.008 Volts
$5\mu A$	5.00 Volts
$10.00\mu A$	10.00 Volts

NE5512 OPERATIONAL DIFFERENTIATOR

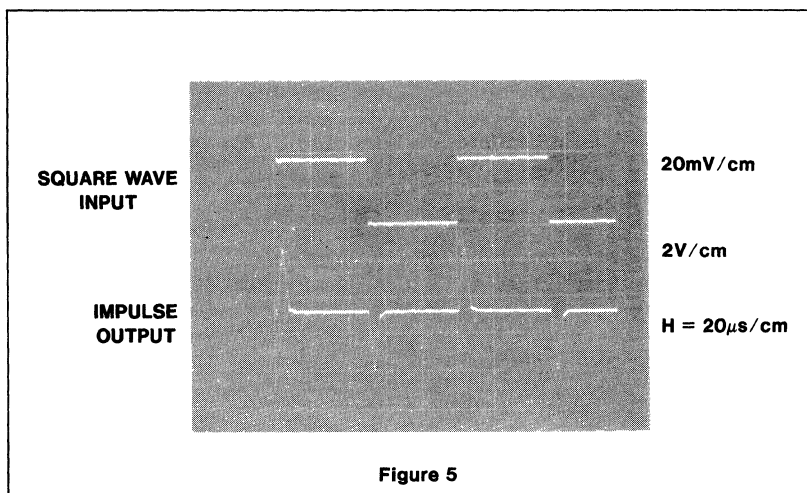
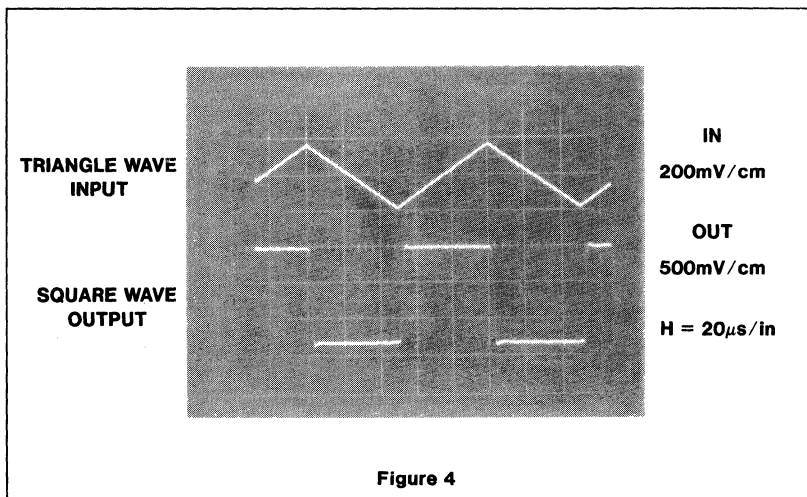
By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the wave forms in figures 4, 5 and 6. One of the primary problems with such circuits is the tendency toward instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency requiring low input noise in the amplifier.

The relative stability is shown by the output signal wave forms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC , must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.



DIFFERENTIATOR WAVEFORMS



THE OPERATIONAL INTEGRATOR

The operational compliment of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration the time constant must fulfill the following requirement:

$$RC \approx 15T$$

Where T is the period of the input wave form. For the ideal integrator

$$e_{out} = \frac{1}{RC} \int e_{in} dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The wave forms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of $\approx 89^\circ$ for sine wave input over the active frequency range. For a square wave the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

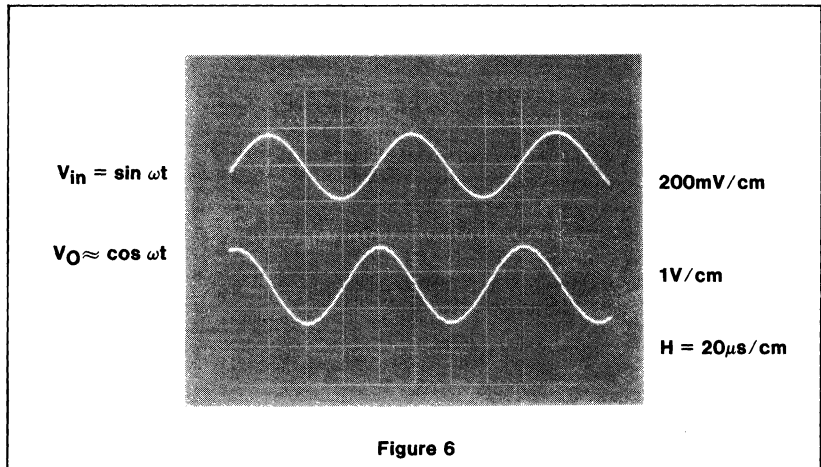


Figure 6

NE/SE5512 ACTIVE INTEGRATOR WITH INVERTING BUFFER

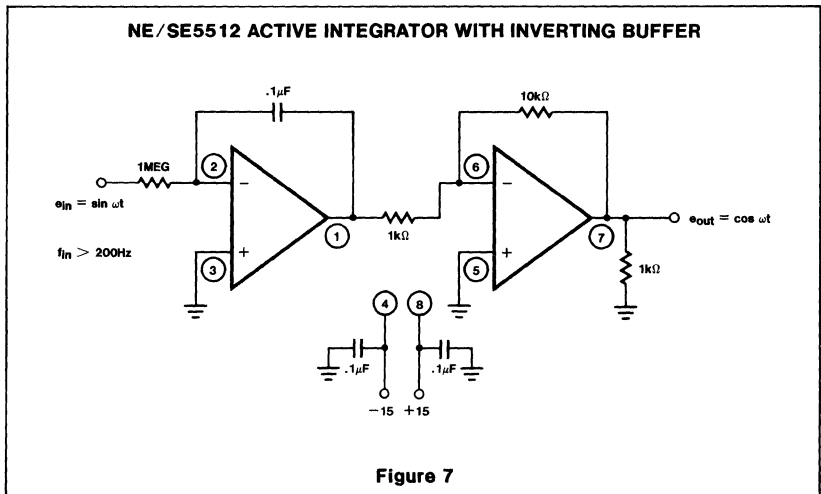


Figure 7

INTEGRATOR WAVEFORMS

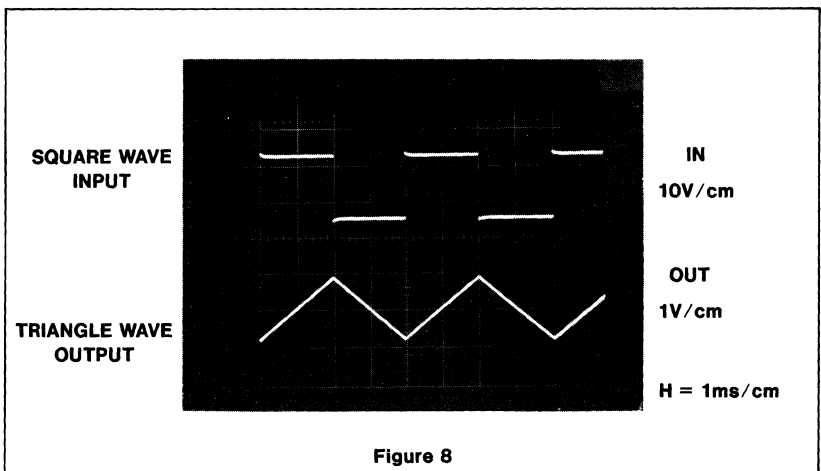
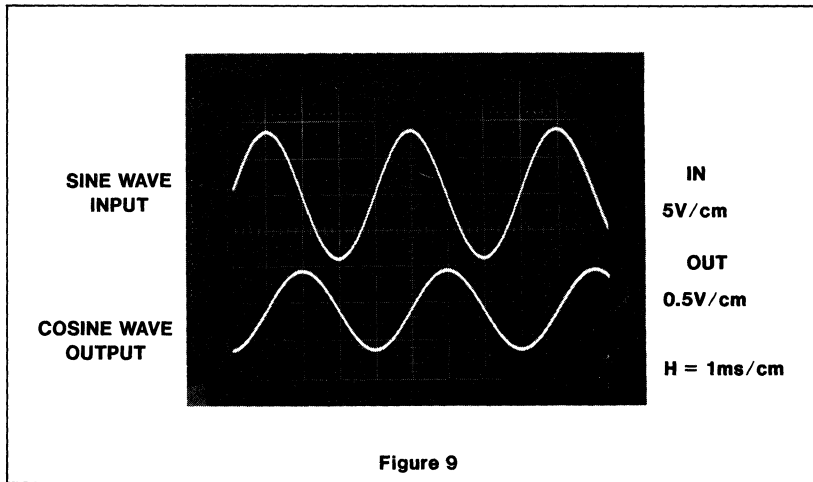


Figure 8

INTEGRATOR WAVEFORMS



DESCRIPTION

The NE/SE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μ A741 with improved slew and drive capability.

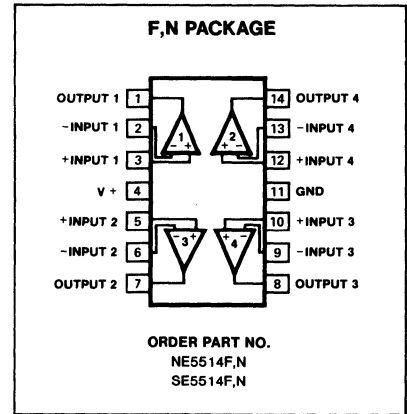
FEATURES

- Low input bias current: $< \pm 3nA$
- Low input offset current: $< \pm 3nA$
- Low input offset voltage: $< 1mV$
- Low supply current: 1.5mA/Amp
- 1 V/ μ sec slew rate
- High input impedance: 100M Ω
- High common mode impedance: 10G Ω
- Internal compensation for unity gain

APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Instrumentation amplifier

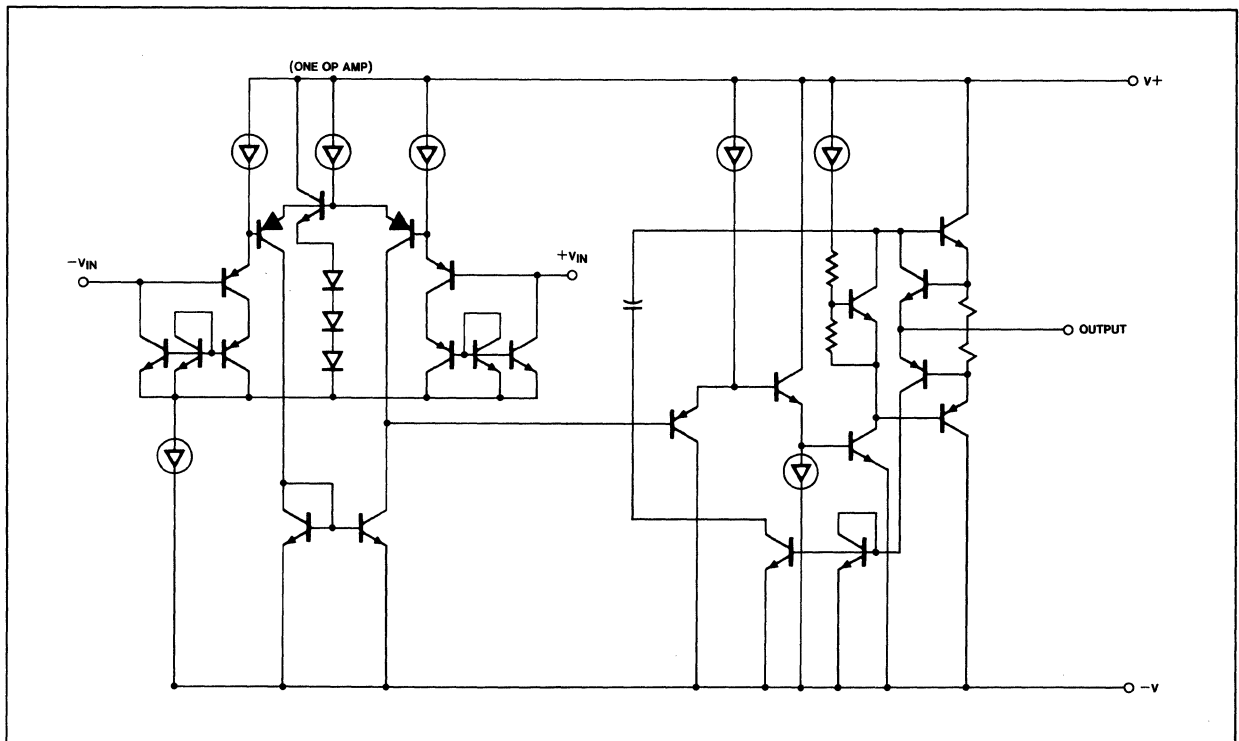
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	± 16 V
V _{DIFF}	Differential input voltage	32 V
V _{IN}	Input voltage	0 to 32 V
	Output short to ground	Continuous
T _S	Storage temperature range	-65 to +150 °C
T _{SOLD}	Lead soldering temperature	300 °C
T _A	Operating temperature range	
	NE5514	0 to 70 °C
	SE5514	-55 to +125 °C

EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = $-55^{\circ}C$ to $+125^{\circ}C$ (SE) $0^{\circ}C$ to $70^{\circ}C$ (NE)

PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS}	Input offset voltage $R_S = 100\Omega$, $T_A = +25^{\circ}C$, $T_A = F.R.$		0.7 1	2 3		1 1.5	5 6	mV
I _{OS}	Input offset current $R_S = 100k\Omega$, $T_A = +25^{\circ}C$, $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
I _B	Input bias current $R_S = 100k\Omega$, $T_A = +25^{\circ}C$, $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
R _{IN}	Input resistance differential $T_A = 25^{\circ}C$		100			100		M Ω
V _{CM}	Input common mode range $T_A = 25^{\circ}C$, $T_A = F.R.$	± 13.5 ± 13.5	± 13.7 ± 13.2		± 13.5 ± 13	± 13.7 ± 13.2		V
CMRR	Input common-mode rejection ratio $V_{CC} = \pm 15V$, $V_{IN} = \pm 13.5V$ (RM), $T_A = 25^{\circ}C$, $V_{IN} = \pm 13V$ (F.R.), $T_A = F.R.$	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain $R_L = 2k\Omega$, $T_A = 25^{\circ}C$ $V_C = \pm 10V$, $T_A = F.R.$	50 25	200		50 25			V/mV
S.R.	Slew rate $T_A = 25^{\circ}C$	0.6	1		0.6	1		V/ μ s
GBW	Small-signal unity gain bandwidth $T_A = 25^{\circ}C$		1			1		MHz
θ_M	Phase margin $T_A = 25^{\circ}C$		45			45		Degr
V _{OUT}	Output voltage swing $R_L = 2k\Omega$, $T_A = 25^{\circ}C$ $T_A = F.R.$	± 13 ± 12.5	± 13.5 ± 13		± 13 ± 12.5	± 13.5 ± 13		V
V _{OUT}	Output voltage swing $R_L = 600\Omega^*$, $T_A = 25^{\circ}C$ $T_A = F.R.$	± 10 ± 8	± 11.5 ± 9		± 10 ± 8	± 11.5 ± 9		V
I _{CC}	Power supply current $R_L = \text{Open}$, $T_A = 25^{\circ}C$ $T_A = F.R.$		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio $T_A = 25^{\circ}C$, $T_A = F.R.$	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling $f = 1kHz$ to $20kHz$, $T_A = 25^{\circ}C$		-120			-120		dB
HD	Total harmonic distortion $f = 10kHz$, $T_A = 25^{\circ}C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V _{INN}	Input-noise voltage $f = 1kHz$, $T_A = 25^{\circ}C$		30			30		nV/ \sqrt{Hz}

NOTE

*For operation at elevated temperature, N package must be derated based on a thermal resistance of $95^{\circ}C/W$ junction to ambient.

FOUR QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photo-conductive mode (reverse biased) very small currents in the micro ampere range must be sensed in the photo active operating region. Dark currents in the nano amperes are common. Generally, for this reason, J-FET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6na) to allow its use under these circuit constraints as shown in a possible design used to sense four quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation. (See figure 1).

The wide input common mode voltage range of the device allows a +10 volt supply to be used to drive the signal bridge giving high sensitivity and improved signal to noise. Obviously, input balancing is critical to achieving common mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. D.C. offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow band active pre-filters to attain selectivity and gain, the effective

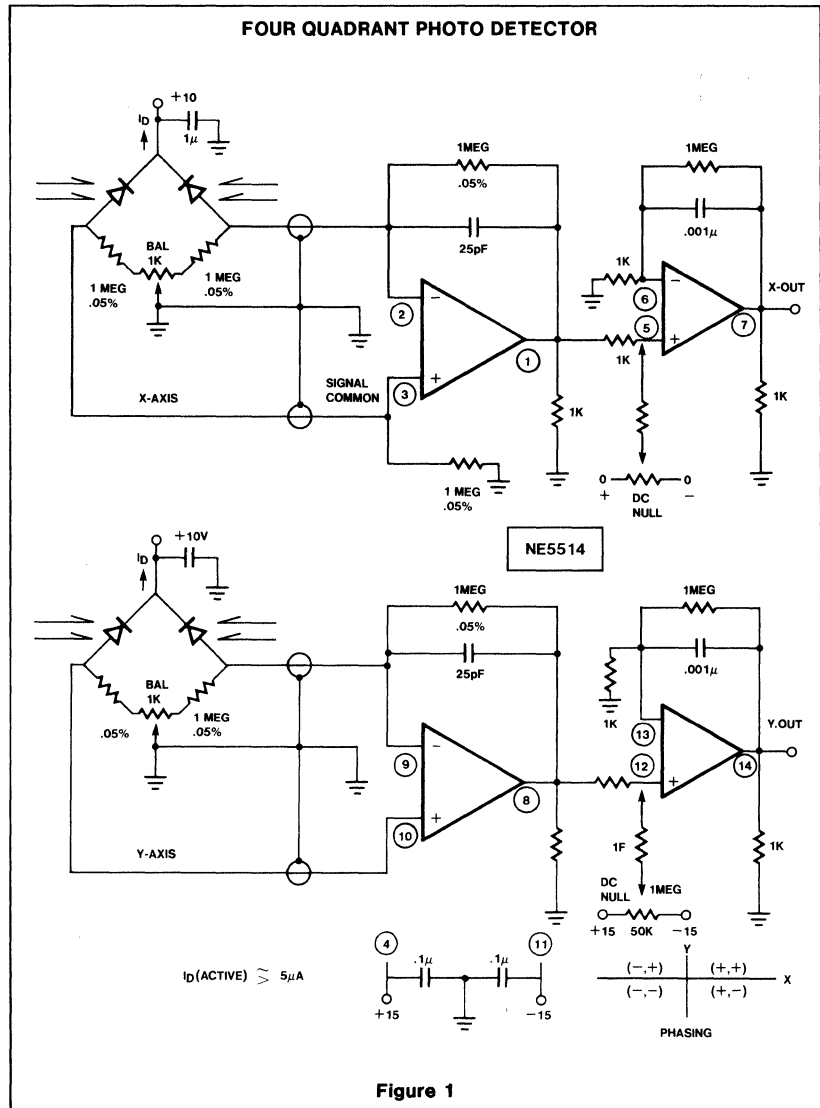


Figure 1

signal to noise ratio is greatly improved. The NE/SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition its very high input impedance drastically reduces loading on the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from this filter configuration were as follows:

Wide band signal to noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	OdBM (.775v _{rms})

Note that the amplifiers are operated from a single +12 volt supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

4-STATION 0-50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current-voltage relationship of a forward biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

$$\text{and } I_E \propto I_S \exp(V_{BE}/V_T); V_T = \frac{kt}{q}$$

therefore, $V_{BE} \propto V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E \gg I_S$). I_S is typically .05 pA, therefore, setting I_E to 1 or 2 μ A gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "0" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100 millivolts per °C output.

Only the transistor need be placed in the temperature controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

**NE/SE5514
MFB BANDPASS FILTER
FOR
MULTI-CHANNEL TONE DECODER**

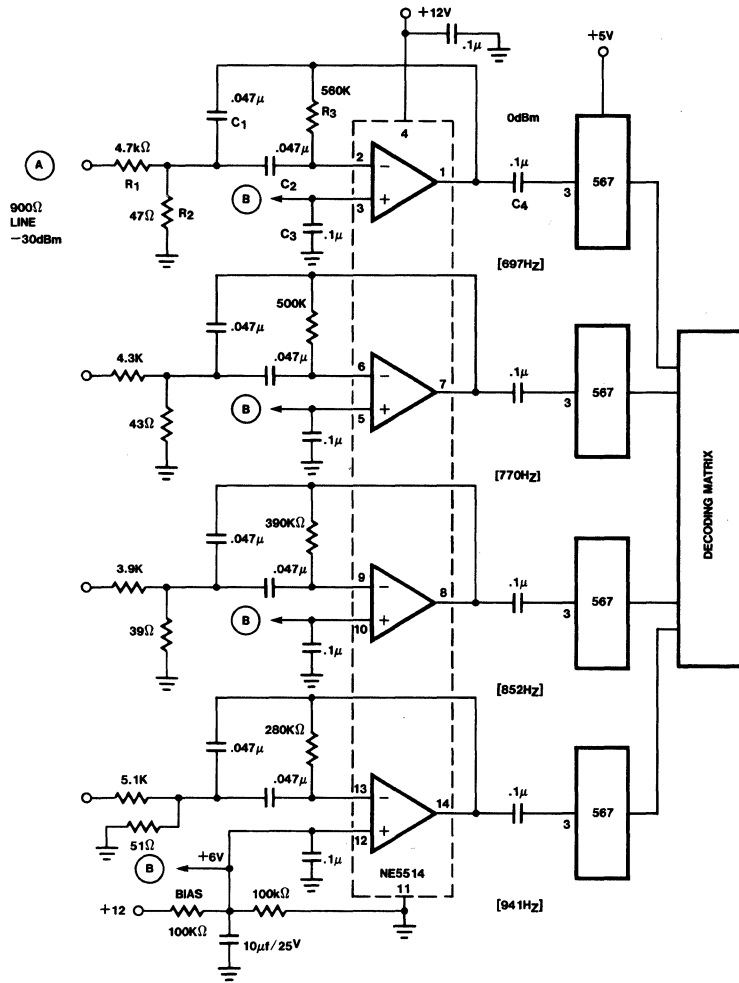


Figure 2

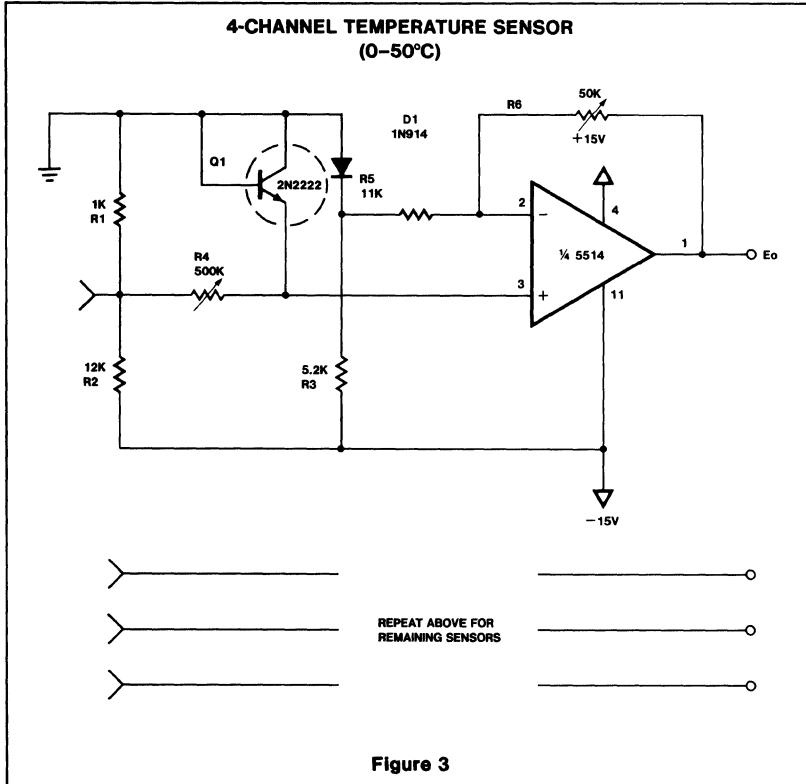


Figure 3

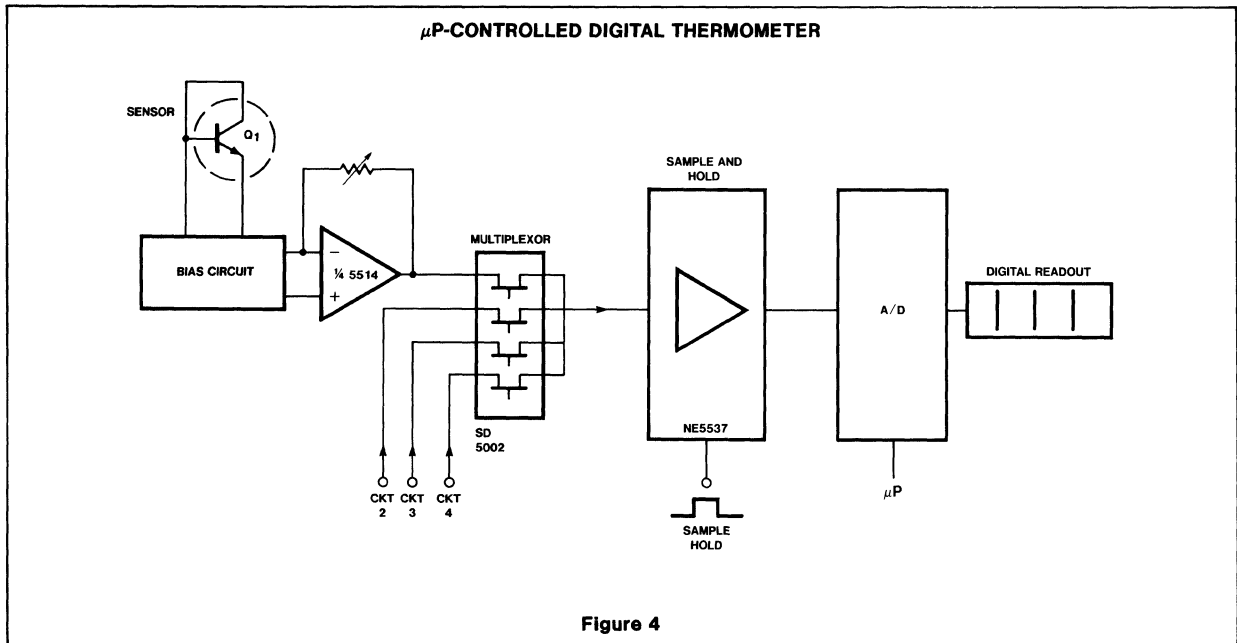


Figure 4

DESCRIPTION

The NE5517 contains two current controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Constant impedance buffers are provided which effectively eliminate changes in output offset voltage as the amplifier bias current is varied. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal to noise improvement referenced to .5 percent THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

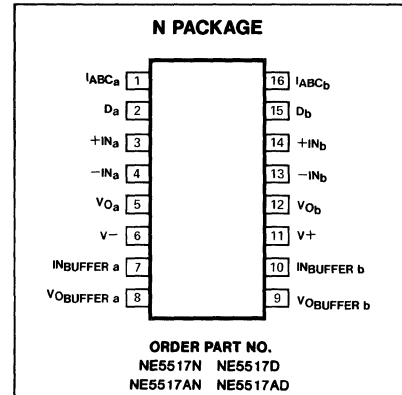
FEATURES

- Constant impedance buffers
- ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change
- Pin compatible with LM13600
- Excellent matching between amplifiers
- Linearizing diodes
- High output signal-to-noise ratio

APPLICATIONS

- Multiplexers
- Timers
- Electronic music synthesizers
- Dolby* HX Systems
- Current-controlled amplifiers, filters
- Current-controlled oscillators, impedances

PIN CONFIGURATION

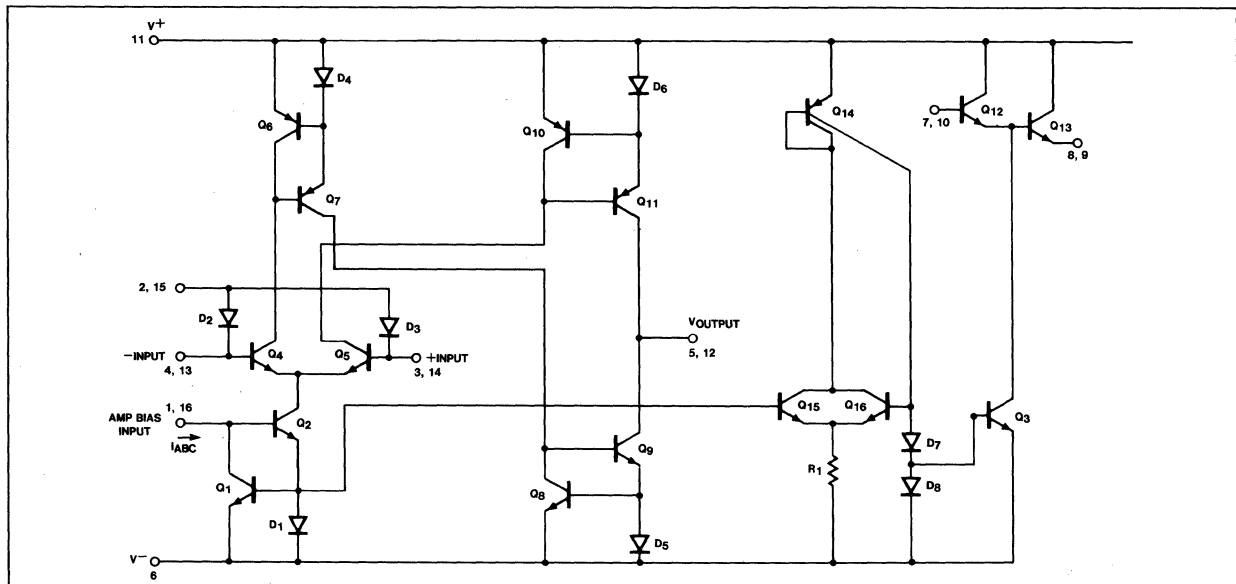


NOTE
*Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage ¹		
NE5517	36 V _{DC} or ± 18	V
NE5517A	44 V _{DC} or ± 22	V
Power Dissipation ² T _A = 25°C		
NE5517N, NE5517AN	570	mW
Differential Input Voltage	± 5	V
Diode Bias Current (I _D)	2	mA
Amplifier Bias Current (I _{ABC})	2	mA
Output Short Circuit Duration	Indefinite	
Buffer Output Current ³	20	mA
Operating Temperature Range		
NE5517N, NE5517AN	0°C to +70	°C
DC Input Voltage	+V _S to -V _S	
Storage Temperature Range	-65°C to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C

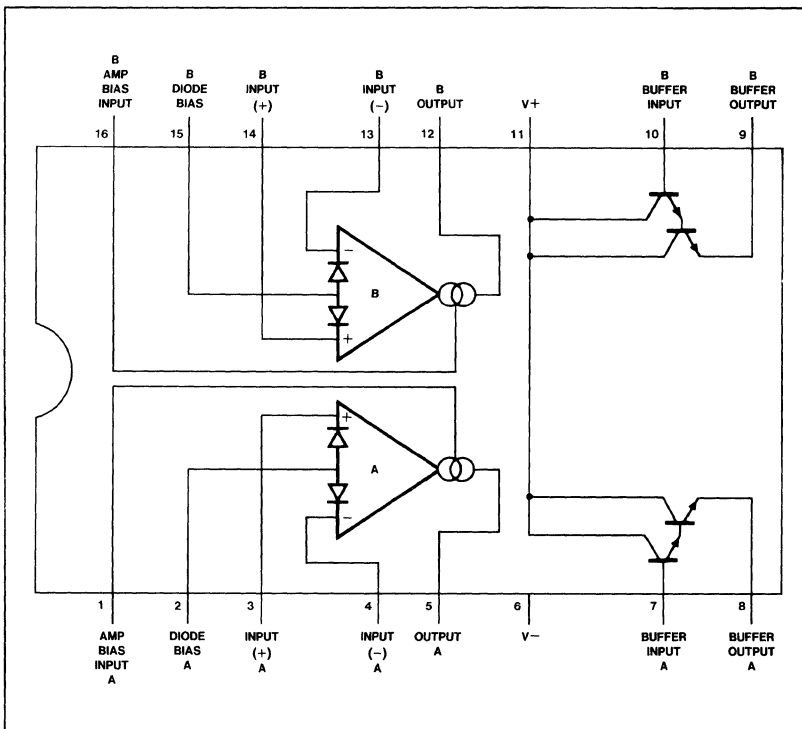
CIRCUIT SCHEMATIC



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{Oa}	Output A
6	$V-$	negative supply
7	$IN_{Buffer(a)}$	Buffer input A
8	$V_{oBuffer(a)}$	Buffer output A
9	$V_{oBuffer(b)}$	Buffer output B
10	$IN_{Buffer(b)}$	Buffer input B
11	$V+$	Positive supply
12	V_{Ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

CONNECTION DIAGRAM



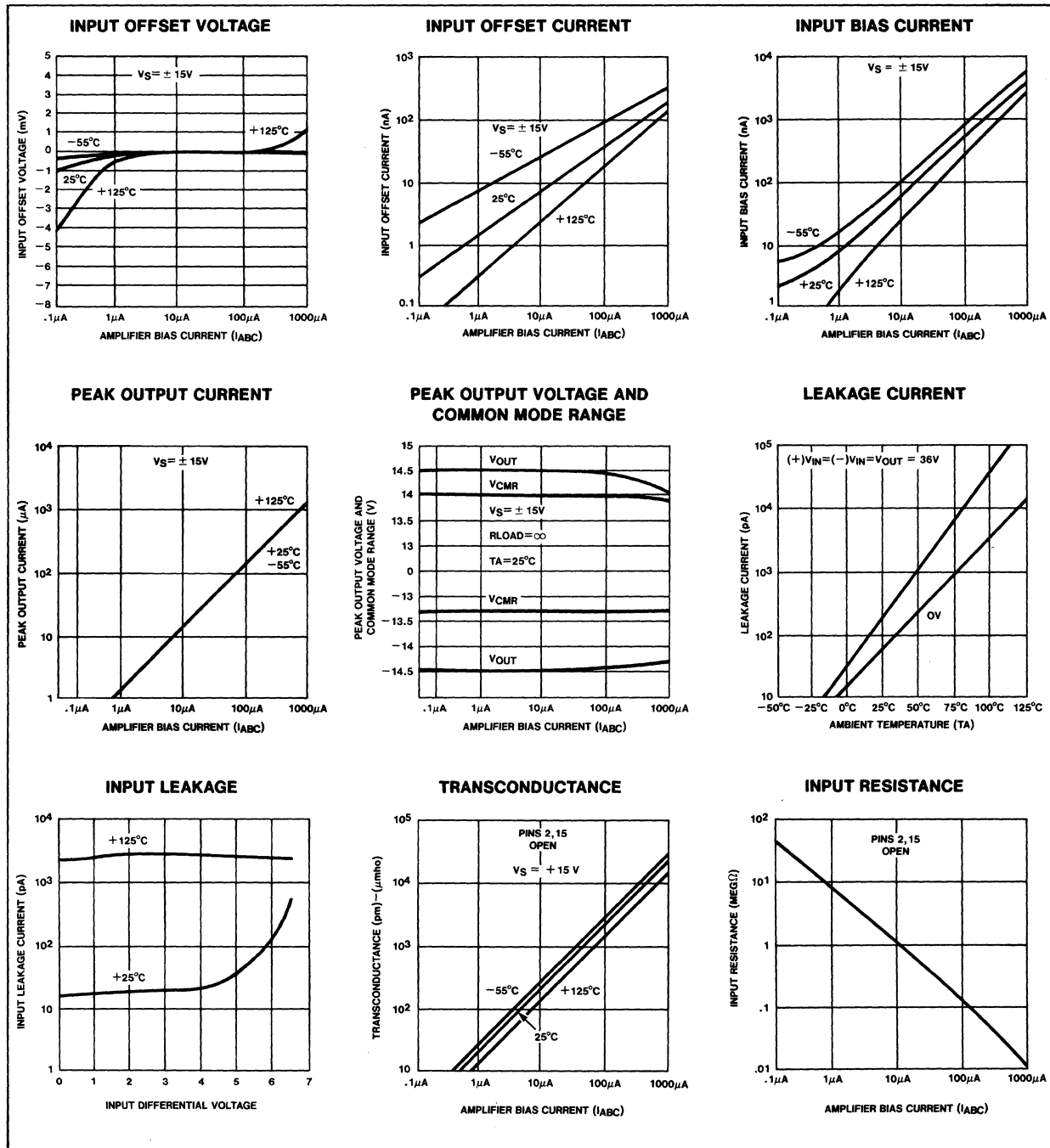
ELECTRICAL CHARACTERISTICS⁴

PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V _{OS})	Over temperature range I _{ABC} 5μA		0.4	5		0.4	2	mV
			0.3	5		0.3	5	mV
							2	mV
V _{OS} including diodes	Diode bias current (I _D) = 500μA		0.5	5		0.5	2	mV
Input offset change	5μA ≤ I _{ABC} ≤ 500μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
Input bias current	Over temperature range		0.4	5		0.4	5	μA
			1	8		1	7	μA
Forward Transconductance (gm)	Over temperature range	6700	9600	13000	7700	9600	12000	μmho
		5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I _{ABC} = 5μA RL = 0, I _{ABC} = 500μA RL = 0,	350	5	650	3	5	7	μA
		300	500		350	500	650	μA
					300			
Peak output voltage	RL = ∞, 5μA ≤ I _{ABC} ≤ 500μA RL = ∞, 5μA ≤ I _{ABC} ≤ 500μA	+12	+14.2		+12	+14.2		V
		-12	-14.4		-12	-14.4		V
Supply current	I _{ABC} = 500μA, both channels		2.6			2.6		mA
V _{OS} sensitivity	Δ V _{OS} /Δ V+ Δ V _{OS} /Δ V-		20	150		20	150	μV/V
			20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to input ⁵ 20Hz < f < 20kHz		100			100		dB
Diff. input current	I _{ABC} = 0, input = ± 4V		0.02	100		0.02	10	nA
Leakage current	I _{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V
Δ V _{BE} of buffer	6 Refer to Buffer V _{BE} test circuit		0.5	5		0.5	5	mV

NOTES

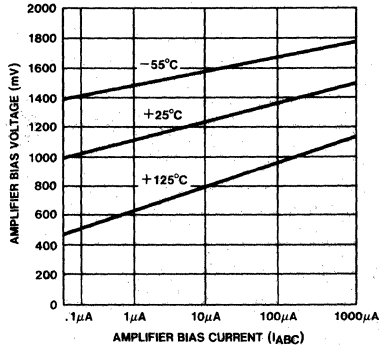
- For selections to a supply voltage above ±22V, contact factory.
- For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
- Buffer output current should be limited so as to not exceed package dissipation.
- These specifications apply for V_S = ± 15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for V_S = ± 15V, I_{ABC} = 500μA, R_{OUT} = 5kΩ connected from the buffer output to -V_S and the input of the buffer is connected to the transconductance amplifier output.
- V_S = ± 15, R_{OUT} = 5Ω connected from Buffer output to -V_S and 5μA ≤ I_{ABC} ≤ 500μA.

TYPICAL PERFORMANCE CHARACTERISTICS

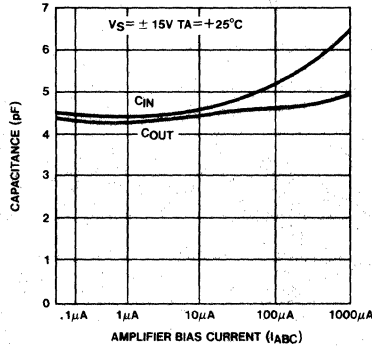


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

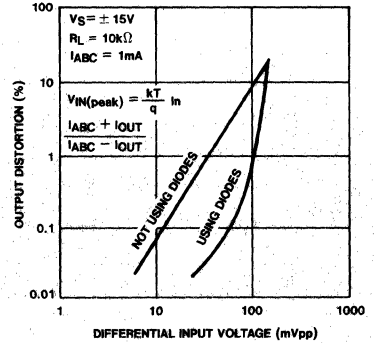
AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT



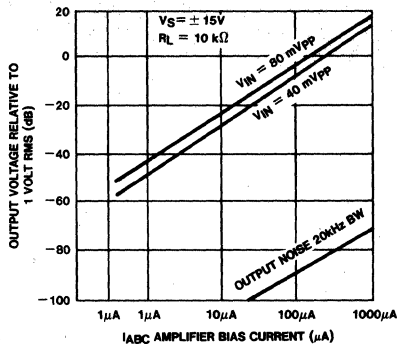
INPUT AND OUTPUT CAPACITANCE



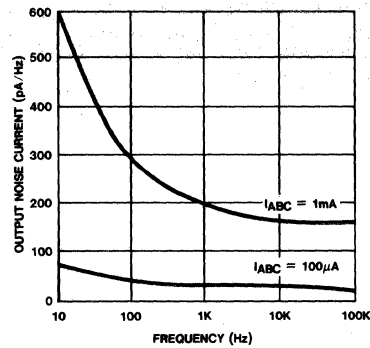
DISTORTION vs DIFFERENTIAL INPUT VOLTAGE



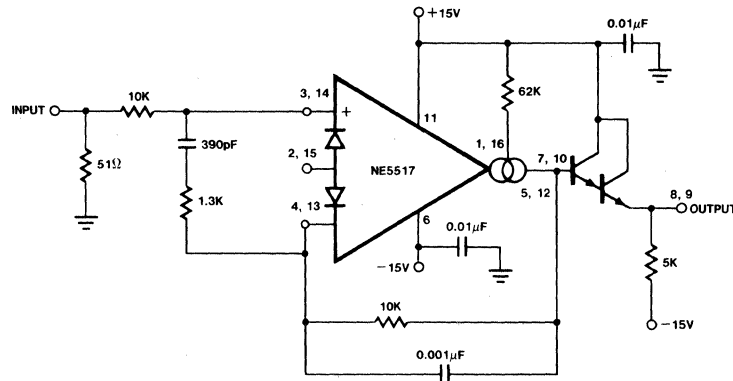
VOLTAGE vs AMPLIFIER BIAS CURRENT



OUTPUT NOISE vs FREQUENCY

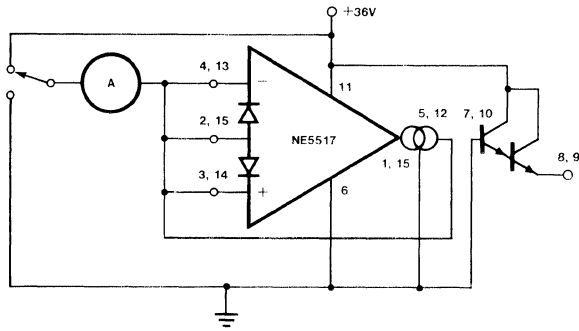


UNITY GAIN FOLLOWER

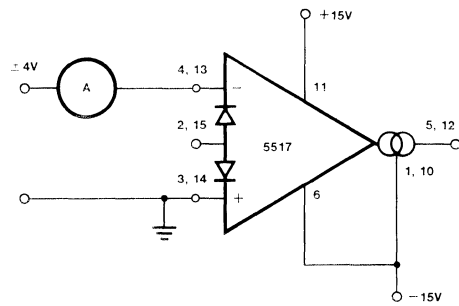


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

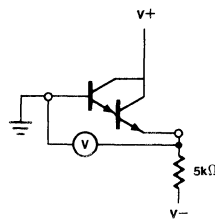
LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT



BUFFER V_{BE} TEST CIRCUIT



DESCRIPTION

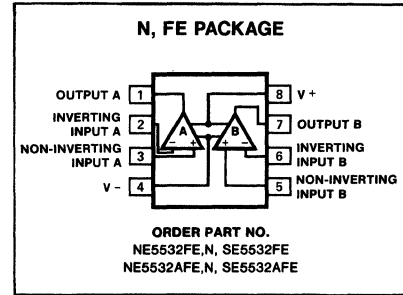
The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

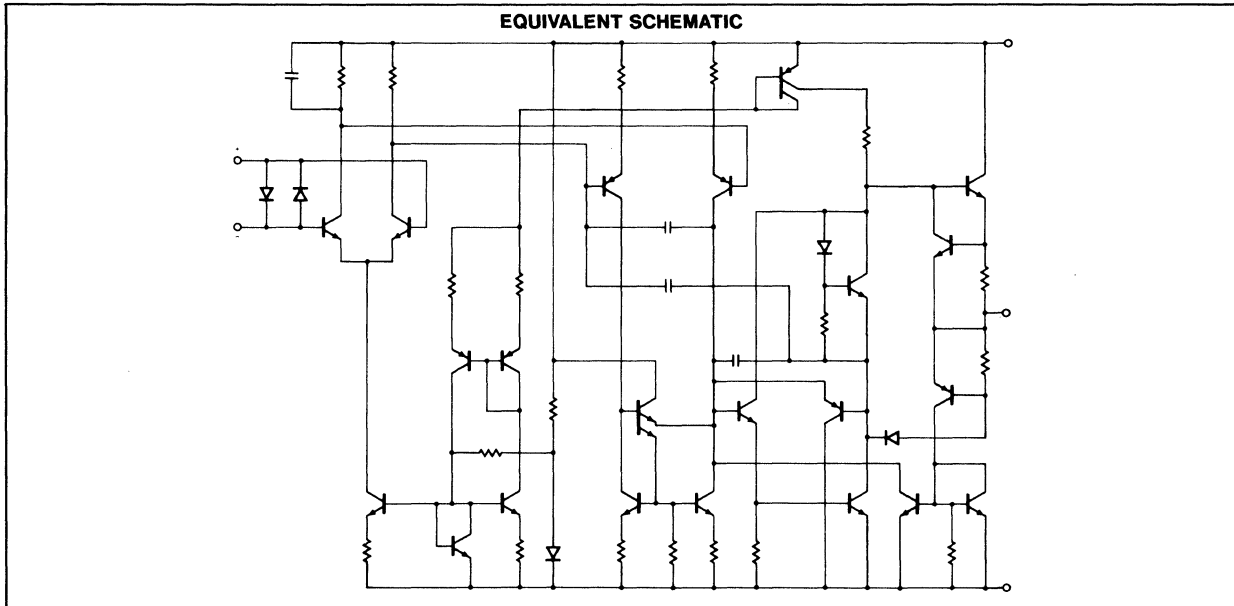
FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, 10V (rms)
- Input noise voltage: $5nV/\sqrt{Hz}$
- DC voltage gain: 50000
- AC voltage gain: 2200 at 10kHz
- Power bandwidth: 140kHz
- Slew-rate: $9V/\mu s$
- Large supply voltage range: ± 3 to $\pm 20V$

PIN CONFIGURATION



EACH AMPLIFIER



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _S Supply voltage	± 22	V
V _{IN} Input voltage	$\pm V$ supply	V
V _{DIFF} Differential input voltage ¹	$\pm .5$	V
T _A Operating temperature range	0 to 70	°C
T _{STG} Storage temperature	-65 to +150	°C
T _J Junction temperature	150	°C
P _D Power dissipation		
5532FE	1000	mW
Lead temperature (soldering, 10 sec)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to $\pm 10mA$.
2. Thermal resistance of the FE package is 125°C/W.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	Over temperature		.5	2 3		.5	4 5	mV mV
I_{OS} Offset current	Over temperature			100 200		10	150 200	nA nA
I_B Input current	Over temperature		200	400 700		200	800 1000	nA nA
I_{CC} Supply current	Over temperature			13		8	16	mA mA
V_{CM} Common mode input range		± 12	± 13		± 12	± 13		V
CMRR Common mode rejection ratio		80	100		70	100		dB
PSRR Power supply rejection ratio			10	50		10	100	$\mu\text{V/V}$
A_{VOL} Large signal voltage gain	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	50			25	100		V/mV
	Over temperature	25			15			V/mV
	$R_L \geq 600\Omega$, $V_O = \pm 10\text{V}$	40			15	50		V/mV
	Over temperature	20			10			V/mV
V_{OUT} Output swing	$R_L \geq 600\Omega$				± 12	± 13		V
	$R_L \geq 600\Omega$, $V_S = \pm 18\text{V}$				± 15	± 16		V
	$R_L \geq 2\text{k}\Omega$	± 12	± 13					V
R_{IN} Input resistance		30	300		30	300		k Ω
I_{SC} Output short circuit current			38			38		mA

NOTES

- For NE5532, NE5532A, $T_{Min} = 0^\circ\text{C}$, $T_{Max} = 70^\circ\text{C}$.
- For SE5532/5532A, $T_{Min} = -55^\circ\text{C}$, $T_{Max} = +125^\circ\text{C}$.

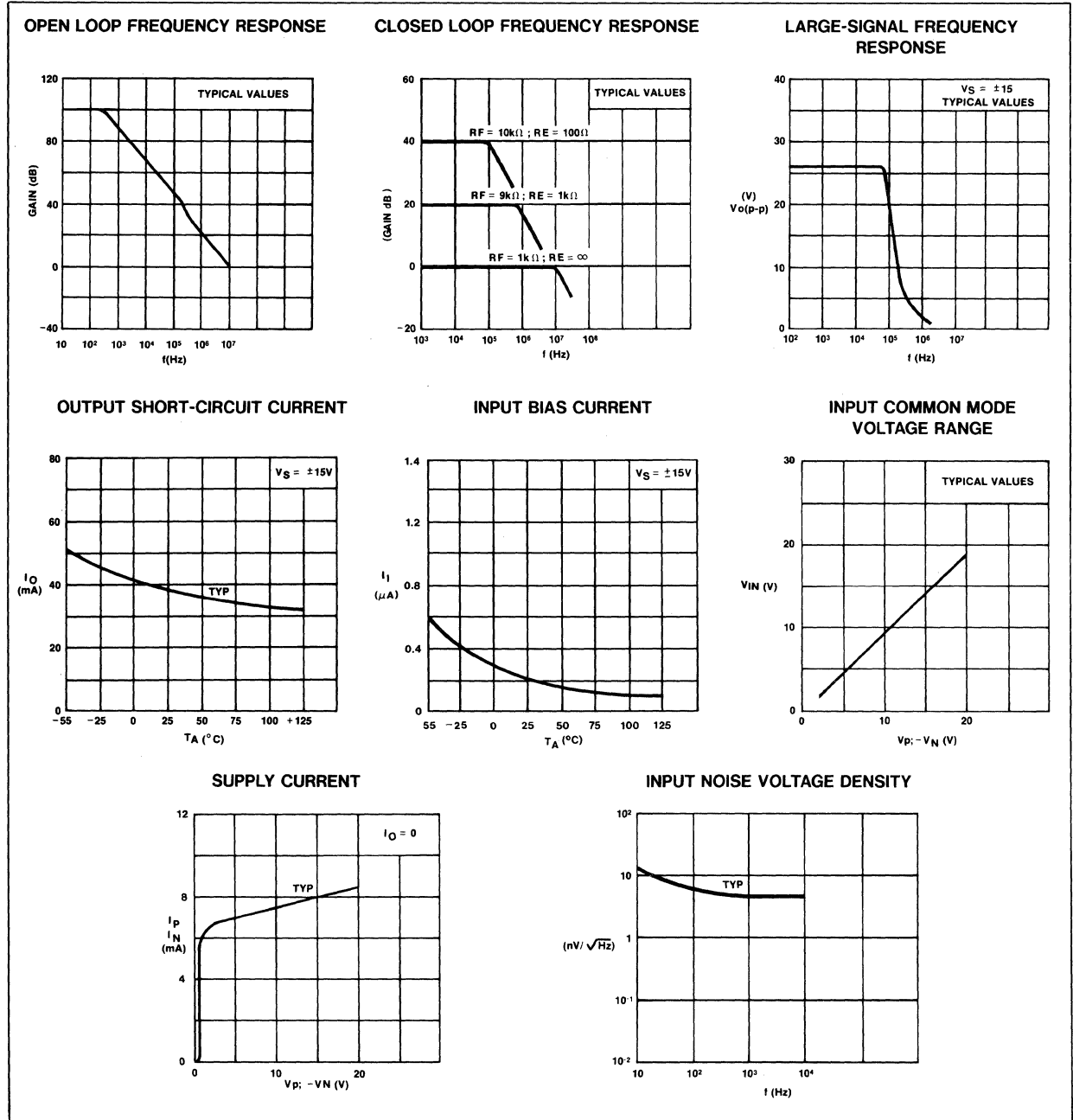
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE/SE5532/5532A			UNIT
		Min	Typ	Max	
R_{OUT} Output resistance	$A_V = 30\text{dB}$ Closed loop $f = 10\text{kHz}$, $R_L = 600\Omega$		0.3		Ω
Overshoot	Voltage follower $V_{IN} = 100\text{mV p-p}$ $C_L = 100\text{pF}$ $R_L = 600\Omega$		10		%
Gain	$f = 10\text{kHz}$		2.2		V/mV
Gain bandwidth product	$C_L = 100\text{pF}$ $R_L = 600\Omega$		10		MHz
Slew rate			9		V/ μs
Power bandwidth	$V_{OUT} = \pm 10\text{V}$		140		kHz
	$V_{OUT} = \pm 14\text{V}$, $R_L = 600\Omega$, $V_{CC} = \pm 18\text{V}$		100		kHz

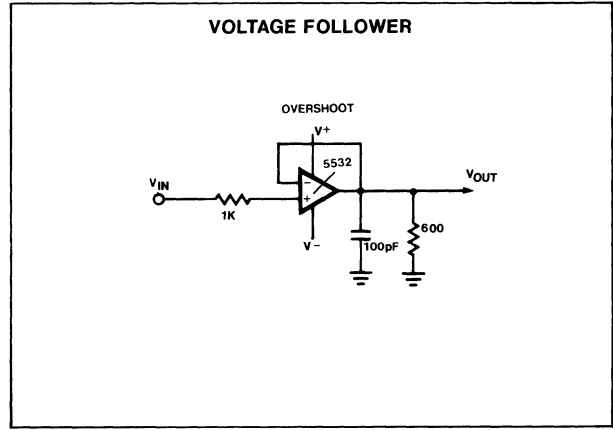
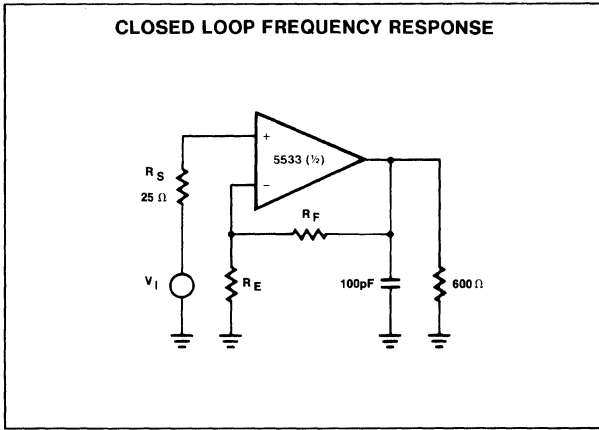
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30\text{Hz}$		8			8	12	$\text{nV}/\sqrt{\text{Hz}}$
	$f_o = 1\text{kHz}$		5			5	6	$\text{nV}/\sqrt{\text{Hz}}$
Input noise current	$f_o = 30\text{Hz}$		2.7			2.7		$\text{pA}/\sqrt{\text{Hz}}$
	$f_o = 1\text{kHz}$		0.7			0.7		$\text{pA}/\sqrt{\text{Hz}}$
Channel separation	$f = 1\text{kHz}$, $R_S = 5\text{k}\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS



TEST CIRCUITS



APPLICATIONS

The Signetics 5532 High Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

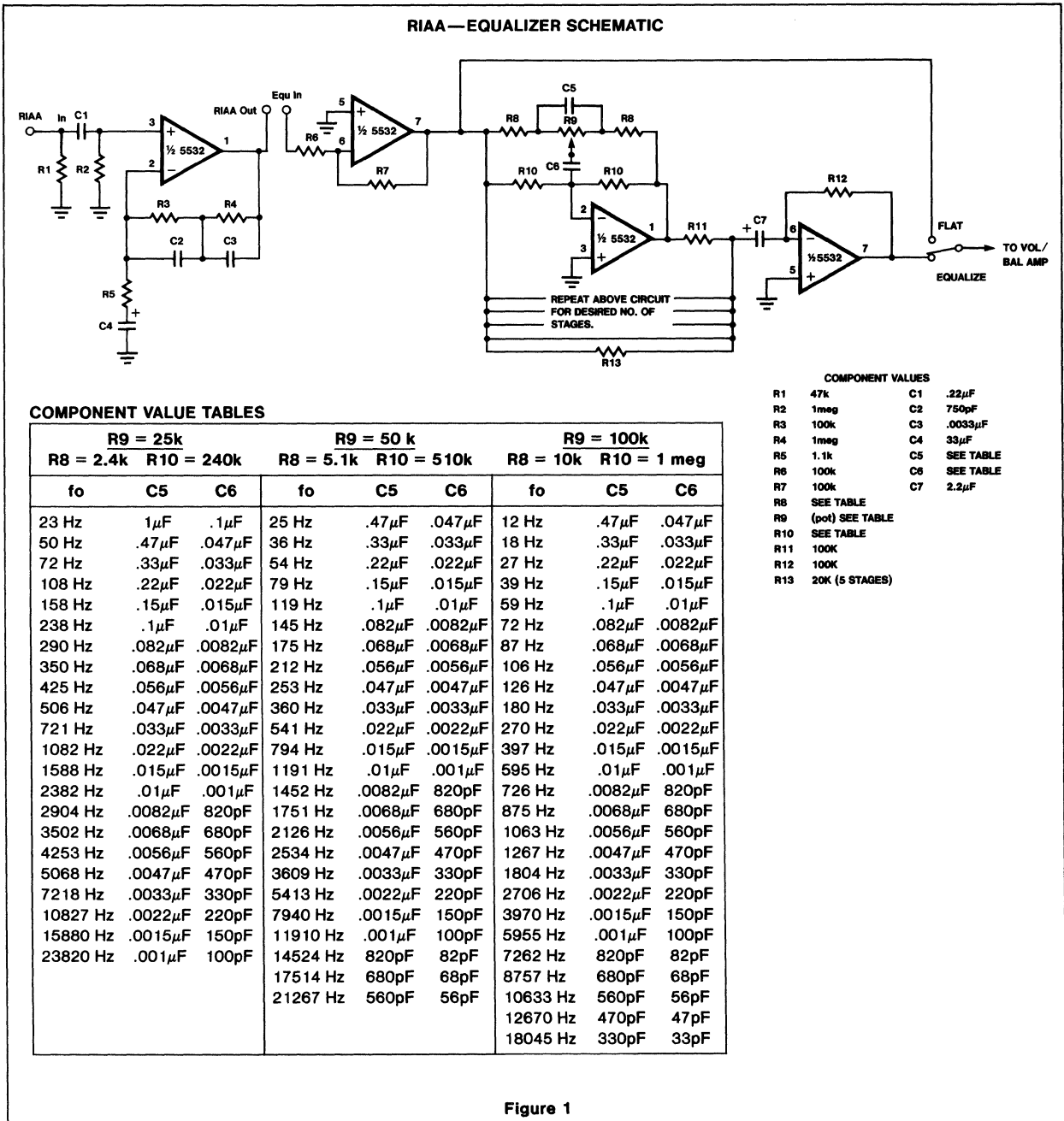
The circuit included in this application note has been assembled on a P.C. board, and tested with actual audio input devices

(Tuner and Turntable). It consists of an RIAA pre-amp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA pre-amp section is a standard compensation configuration with low frequency boost provided by the Magnetic car-

tridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an



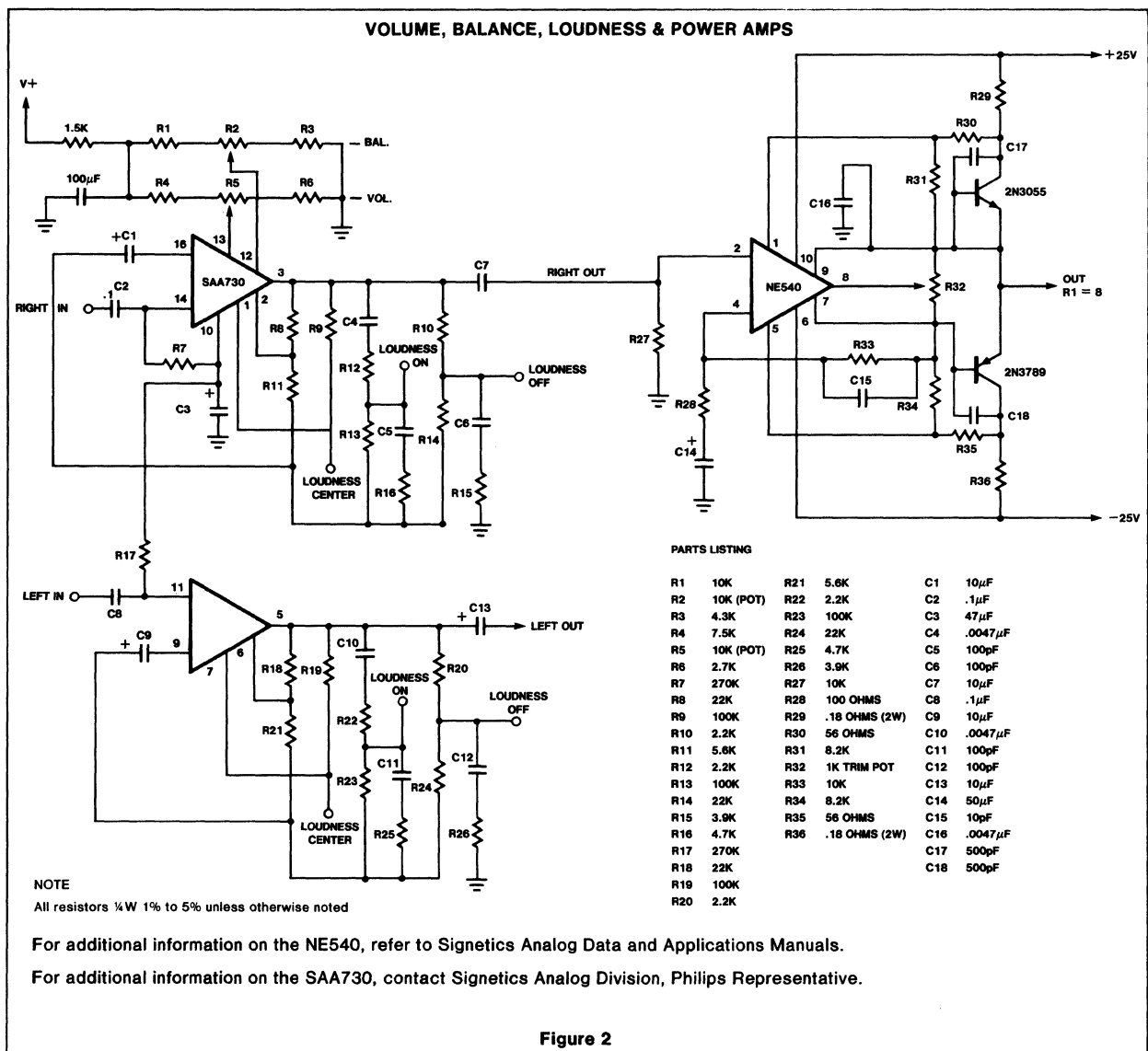
output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the pre amplifiers and the equalizer section. Because the 5532 is internally compensated, no external compensation is required. The 5-band active filter section is actually 5 individual active filters with the same feedback design for all 5. The main difference in all five stages is the values of C5 and C6 which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5

equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

The final stage is the summing amplifier/buffer stage, to sum the individual filters (Figure 2). Note the original signal is subtracted from the sum by a factor dependant on the number of filter stages. This subtraction is necessary to maintain a unity gain configuration at the output with all pots set to the flat position. If R13 were omitted the output with 1 volt at each stage would equal 5 volts (in this case) instead of the desired 1 volt. Full boost and cut using the table val-

ues is about $\pm 15\text{dB}$. Although 5 bands were chosen for this application, the user may have as many bands as are required. Please note that the subtracting resistor R13, must be adjusted to meet the unity requirement using $R13 = \frac{100K}{\# \text{ of stages}}$ i.e. 5 stages = 20k.

The remainder of the circuit employs the Philips TCA 730H volume, balance, and loudness-control circuit and the Signetics NE540 power driver circuit, which as shown will net about 35 watts per channel RMS. The NE540 can be found in the Signetics Analog Data Manual, and Applications Manual. Information on the TCA730A may be obtained from Signetics Analog Division.



PARTS LISTING

R1	10K	R21	5.6K	C1	10 μ F
R2	10K (POT)	R22	2.2K	C2	.1 μ F
R3	4.3K	R23	100K	C3	47 μ F
R4	7.5K	R24	22K	C4	.0047 μ F
R5	10K (POT)	R25	4.7K	C5	100pF
R6	2.7K	R26	3.9K	C6	100pF
R7	270K	R27	10K	C7	10 μ F
R8	22K	R28	100 OHMS	C8	.1 μ F
R9	100K	R29	.18 OHMS (2W)	C9	10 μ F
R10	2.2K	R30	56 OHMS	C10	.0047 μ F
R11	5.6K	R31	8.2K	C11	100pF
R12	2.2K	R32	1K TRIM POT	C12	100pF
R13	100K	R33	10K	C13	10 μ F
R14	22K	R34	8.2K	C14	50 μ F
R15	3.9K	R35	56 OHMS	C15	10pF
R16	4.7K	R36	.18 OHMS (2W)	C16	.0047 μ F
R17	270K			C17	500pF
R18	22K			C18	500pF
R19	100K				
R20	2.2K				

DESCRIPTION

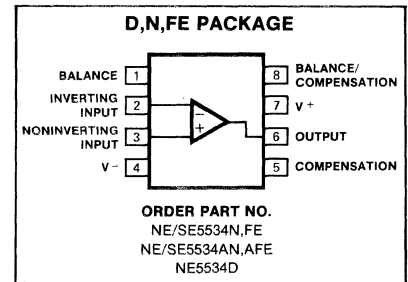
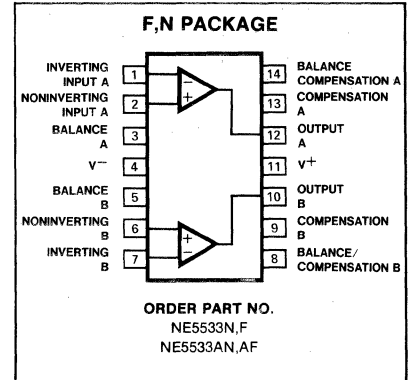
The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

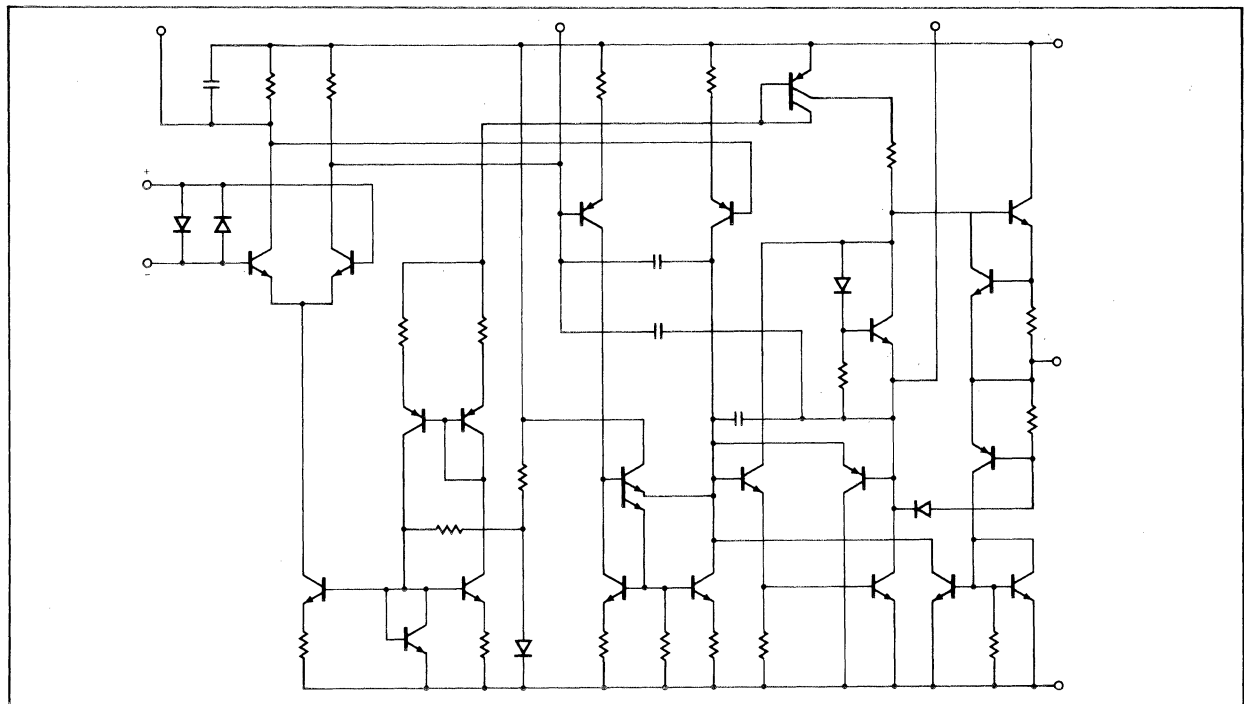
FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_s = \pm 18V$**
- **Input noise voltage: $4nV/\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: $13V/\mu s$**
- **Large supply voltage range: ± 3 to $\pm 20V$**

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _S	Supply voltage	±22	V
V _{IN}	Input voltage	±V supply	V
V _{DIFF}	Differential input voltage ¹	±.5	V
T _A	Operating temperature range		
	SE 5534 / 5534A	-55 to +125	°C
	NE5533 / 5533A / 5534 / 5534A	0 to +70	°C
T _{STG}	Storage temperature	-65 to +150	°C
T _J	Junction temperature	150	°C
P _D	Power dissipation at 25°C ²		
	5533N, 5534N, 5534FE	800	mW
	5533F	1000	mW
	Output short circuit duration ³	indefinite	
	Lead temperature (soldering 10 sec)	300	°C

NOTES

- Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
- For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistances:
 - 8-pin ceramic (FE) 140°C/W
 - 14-pin ceramic (F) 110°C/W
 - 8-pin plastic (N) 162°C/W
 - 14-pin plastic (IN) 150°C/W
- Output may be shorted to ground at V_S = ±15V, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage	Over temperature		.5	2 3		.5	4 5	mV mV
I _{OS} Offset current	Over temperature		10	200 500		20	300 400	nA nA
I _B Input current	Over temperature		400	800 1500		500	1500 2000	nA nA
I _{CC} Supply current Per op amp	Over temperature		4	6.5 9		4	8	mA mA
V _{CM} Common mode input range		±12	±13		±12	±13		V
CMRR Common mode rejection ratio		80	100		70	100		dB
PSRR Power supply rejection ratio			10	50		10	100	μV/V
A _{VOL} Large signal voltage gain	R _L ≥ 600Ω, V _O = ±10V Over temperature	50 25	100		25 15	100		V/mV V/mV
V _{OUT} Output swing	R _L ≥ 600Ω R _L ≥ 600Ω V _S = ±18V	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V
R _{IN} Input resistance		50	100		30	100		kΩ
I _{SC} Output short circuit current			38			38		mA

NOTES

- For NE5533/5533A/5534/5534A, T_{MIN} = 0°C, T_{MAX} = 70°C
- For SE5534/5534A, T_{MIN} = -55°C, T_{MAX} = +125°C

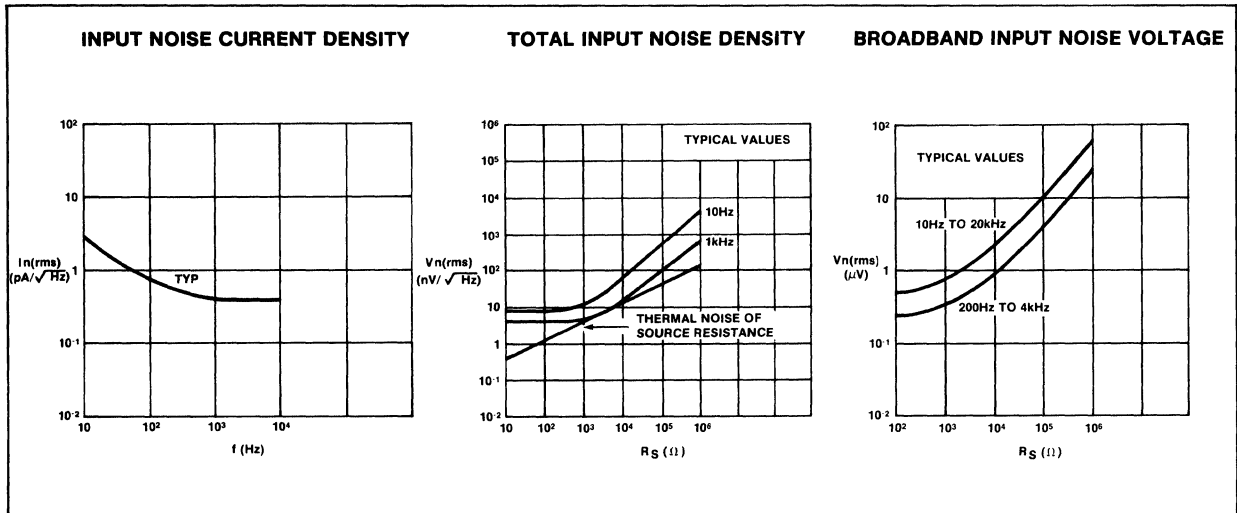
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{OUT} Output resistance	$A_V = 30\text{dB}$ closed loop $f = 10\text{kHz}$, $R_L = 600\Omega$, $C_C = 22\text{pF}$		0.3			0.3		Ω
Transient response	Voltage follower, $V_{IN} = 50\text{mV}$ $R_L = 600\Omega$, $C_C = 22\text{pF}$, $C_L = 100\text{pF}$							
T_R Rise time Overshoot			20 20			20 20		ns %
Transient response	$V_{IN} = 50\text{mV}$, $R_L = 600\Omega$ $C_C = 47\text{pF}$, $C_L = 500\text{pF}$							
T_R Rise time Overshoot			50 35			50 35		ns %
AC Gain	$f = 10\text{kHz}$, $C_C = 0$ $f = 10\text{kHz}$, $C_C = 22\text{pF}$		6 2.2			6 2.2		V/mV V/mV
Gain bandwidth product	$C_C = 22\text{pF}$, $C_L = 100\text{pF}$		10			10		mHz
Slew rate	$C_C = 0$ $C_C = 22\text{pF}$		13 6			13 6		V/ μS V/ μS
Power bandwidth	$V_{OUT} = \pm 10\text{V}$, $C_C = 0$ $V_{OUT} = \pm 10\text{V}$, $C_C = 22\text{pF}$ $V_{OUT} = \pm 14\text{V}$, $R_L = 600\Omega$ $C_C = 22\text{pF}$, $V_{CC} = \pm 18\text{V}$		200 95 70			200 95 70		kHz kHz kHz

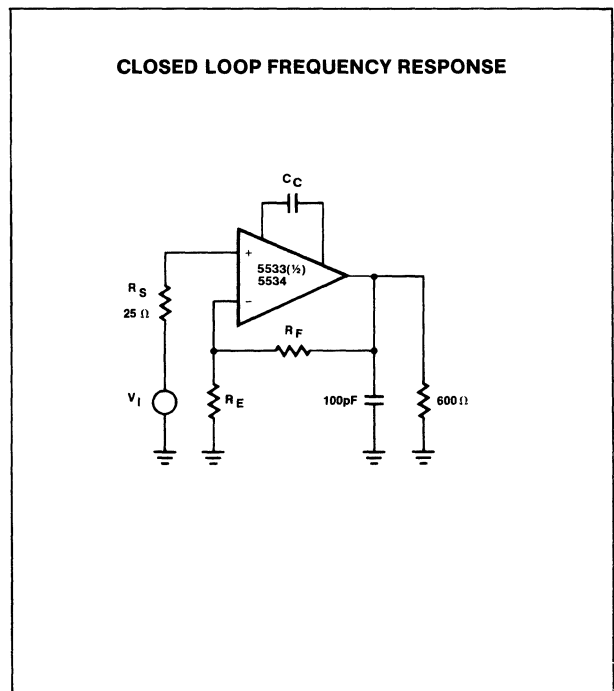
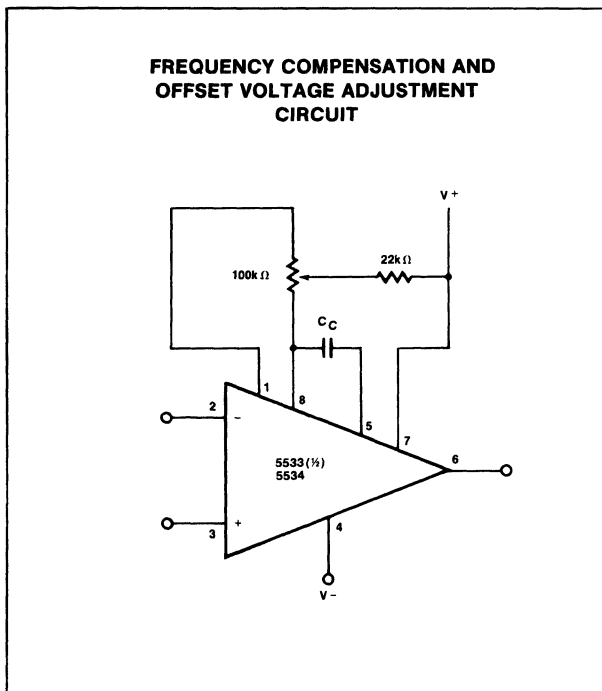
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		7 4			5.5 3.5	7 4.5	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Input noise current	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		2.5 0.6			1.5 0.4		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
Broadband noise figure	$f = 10\text{Hz} - 20\text{kHz}$, $R_S = 5\text{k}\Omega$					0.9		dB
Channel separation	$f = 1\text{kHz}$, $R_S = 5\text{k}\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

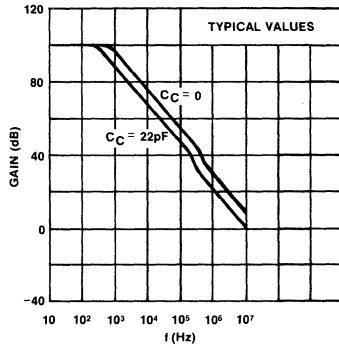


TEST LOAD CIRCUITS

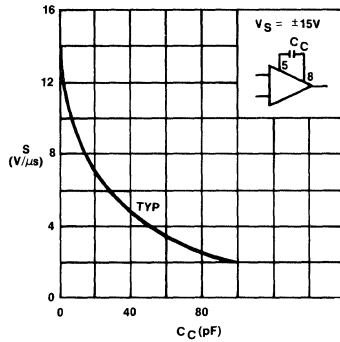


TYPICAL PERFORMANCE CHARACTERISTICS

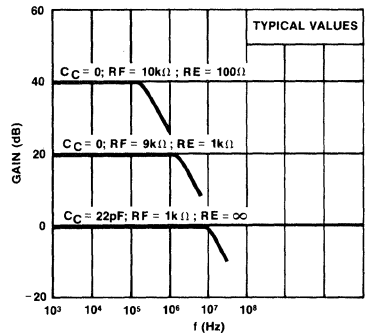
OPEN LOOP FREQUENCY RESPONSE



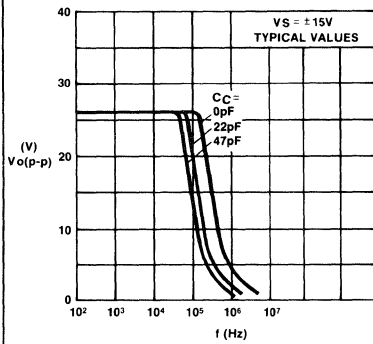
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



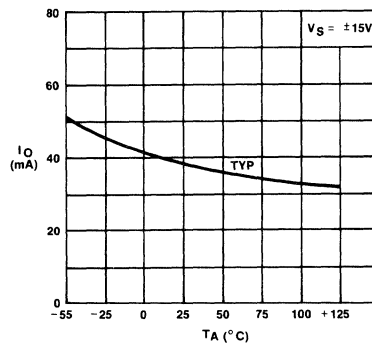
CLOSED LOOP FREQUENCY RESPONSE



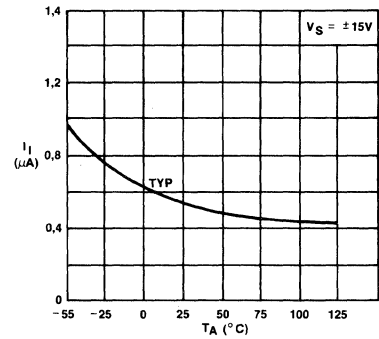
LARGE-SIGNAL FREQUENCY RESPONSE



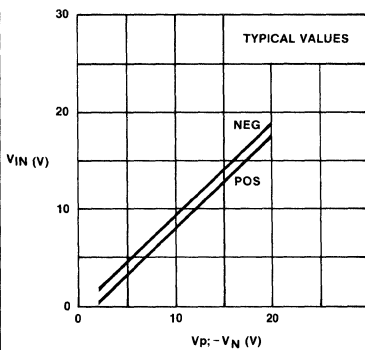
OUTPUT SHORT-CIRCUIT CURRENT



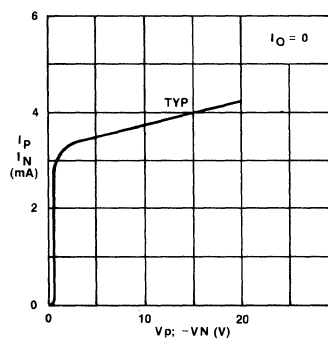
INPUT BIAS CURRENT



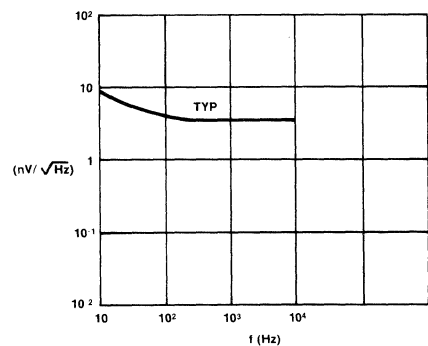
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP AMP



INPUT NOISE VOLTAGE DENSITY



DESCRIPTION

The Signetics NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

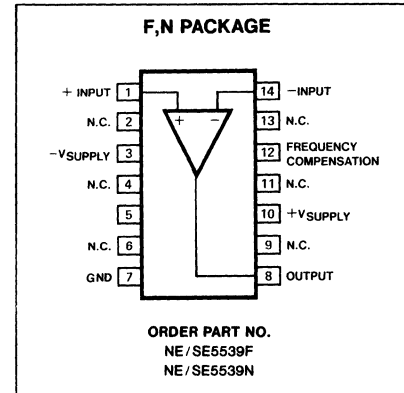
FEATURES

- Gain bandwidth product: 1.2GHz
- Slew rate: 600V/ μ sec
- Full power response: 48MHz
- AVOL: 50dB

APPLICATIONS

- Fast pulse amplifiers
- RF oscillators
- Fast sample and hold
- High gain video amplifiers (BW > 20MHz)

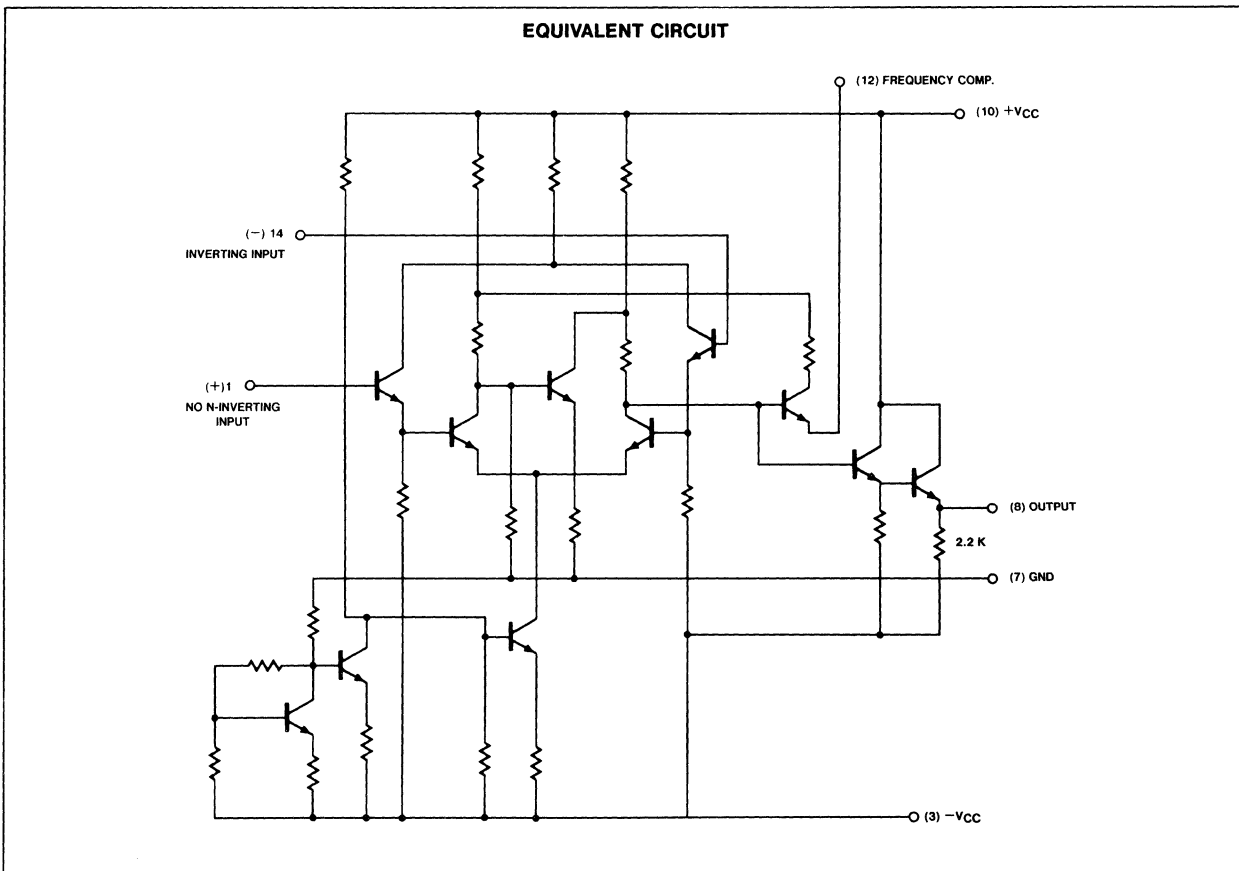
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	± 12	V
P _D	550	mW
T _{STG}	-65 to +150	°C
T _J	150	°C
T _A		
NE	0 to 70	°C
SE	-55 to +125	°C
Lead temperature	300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V, T_A = 25^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT	
		Min	Typ	Max	Min	Typ	Max		
V _{OS} Input offset voltage	V _O = 0V, R _S = 100Ω	Over temp		2	5			mV	
		T _A = 25°C		2	3		2.5		5
I _{OS} Input offset current		Over temp		.1	3			μA	
		T _A = 25°C		.1	1				2
I _B Input bias current		Over temp		6	25			μA	
		T _A = 25°C		5	13		5		20
CMRR Common mode rejection ratio	F = 1 kHz, R _S = 100Ω, V _{CM} = 1.7V	70	80		70	85		dB	
R _{IN} Input impedance			100			100		kΩ	
R _{OUT} Output impedance			10			10		Ω	
V _{OUT} Output voltage swing	R _L = 150Ω to GND and 470Ω to -V _{CC}	+Swing				+2.3	+2.7	V	
		-Swing				-1.7	-2.2		
V _{OUT} Output voltage swing	R _L = 2Ω to GND	Over temp	+Swing	+2.3	+3.0			V	
			-Swing	-1.5	-2.1				
		T _A = 25°C	+Swing	+2.5	+3.1			V	
			-Swing	-2.0	-2.7				
I _{CC+} Positive supply current	V _O = 0, R _I = ∞	Over temp		14	18			mA	
		T _A = 25°C		14	17		14		18
I _{CC-} Negative supply current	V _O = 0, R _I = ∞	Over temp		11	15			mA	
		T _A = 25°C		11	14		11		15
PSRR Power supply rejection ratio	ΔV _{CC} = ±1V	Over temp		300	1000			μV/V	
		T _A = 25°C					200		1000
AVOL Large signal voltage gain	V _O = +2.3V, -1.7V R _L = 150Ω to GND, 470Ω to -V _{CC}					47	52	57	dB
AVOL Large signal voltage gain	V _O = +2.3V, -1.7V R _L = 2K to GND	Over temp							dB
		T _A = 25°C					47	52	
AVOL Large signal voltage gain	V _O = +2.5V, -2.0V R _L = 2Ω to GND	Over temp	46		60				dB
		T _A = 25°C	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V, R_L = 150\Omega$ to GND & 390Ω to -V_{CC} unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	A _{CL} = 7 V _O = 0.1 V _{p-p}					1200		MHz
Small signal bandwidth	A _{CL} = 2 R _L = 150Ω					110		MHz
Settling time	A _{CL} = 2 R _L = 150Ω					15		nSec
Slew rate	A _{CL} = 2 R _L = 150Ω		330			600		V/μSec
Propagation delay	A _{CL} = 2 R _L = 150Ω		10			7		nSec
Full power response	A _{CL} = 2 R _L = 150Ω		20			48		MHz
Full power response	A _V = 7, R _L = 150Ω					20		MHz
Wide band noise (RMS)	B _W = 5MHz, R _S = 50Ω					5		μV

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT	
		Min	Typ	Max	Min	Typ	Max		
V_{OS} Input offset voltage	Over temp		2	5				mV	
	$T_A = 25^\circ C$		2	3					
I_{OS} Input offset current	Over temp		.1	3				μA	
	$T_A = 25^\circ C$.1	1					
I_B Input bias current	Over temp		5	20				μA	
	$T_A = 25^\circ C$		4	10					
CMRR Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$	70	85					dB	
I_{CC+} Positive supply current	Over temp		11	14				mA	
	$T_A = 25^\circ C$		11	13					
I_{CC-} Negative supply current	Over temp		8	11				mA	
	$T_A = 25^\circ C$		8	10					
PSRR Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		300	1000				$\mu V/V$	
V_{OUT} Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+Swing	+1.4	+2.0				V
			-Swing	-1.1	-1.7				
	$T_A = 25^\circ C$	+Swing	+1.5	+2.0				V	
		-Swing	-1.4	-1.8					

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$		700					MHz
Small signal bandwidth	$A_{CL} = 2$		120					MHz
Settling time	$A_{CL} = 2$		23					nSec
Slew rate	$A_{CL} = 2$		330					$V/\mu Sec$
Propagation delay	$A_{CL} = 2$		4.5					nSec
Full power response	$A_{CL} = 2$		20					MHz

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wide band operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown (figure 1) along with the Vectorscope photograph showing the amplifier response to a standard NTSC color signal. (Note that the input reference vectors are displayed simultaneously with the output.) The polar representation indicates amplifier differential

phase error overall to be less than 2° . Gain also remains linear or constant with the varying input amplitudes.

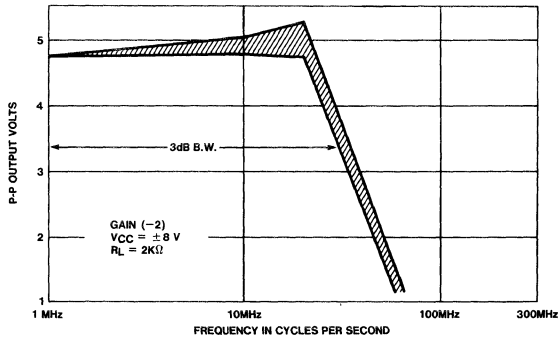
The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of 10 (20dB).

A second series of test waveforms show the amplifier's response to a 3.58MHz burst signal (figures 2 and 3).

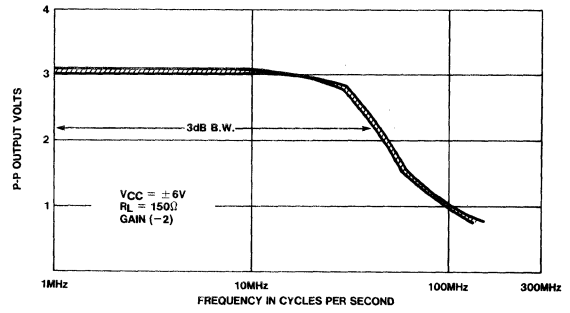
Finally, the amplifier response is shown as a function of time for the NTSC signal with no perceptible droop or overshoot in response to step functions (see figure 4). Note that no external compensation was required since the gain was greater than 7 (17dB).

V_{CC} is ± 8 volts for all cases shown.

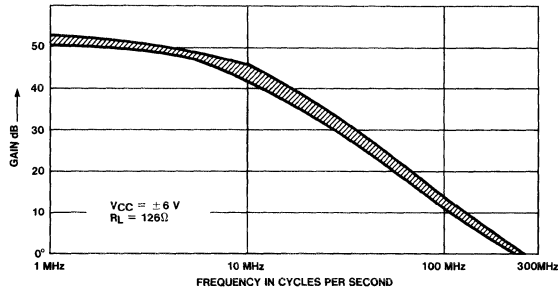
POWER BANDWIDTH (SE)



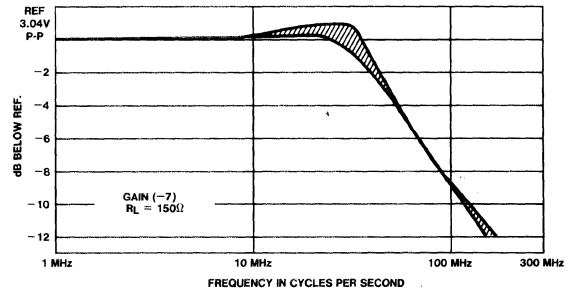
POWER BANDWIDTH (NE)



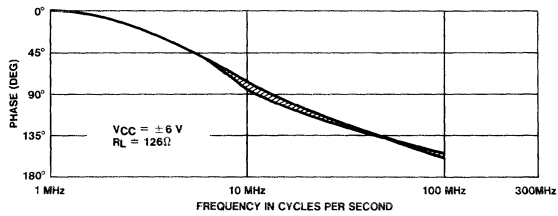
SE5539 OPEN LOOP GAIN vs FREQUENCY



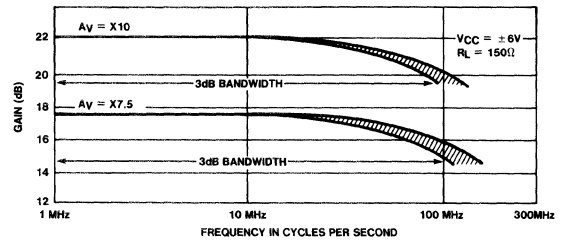
POWER BANDWIDTH




SE5539 OPEN LOOP PHASE vs FREQUENCY



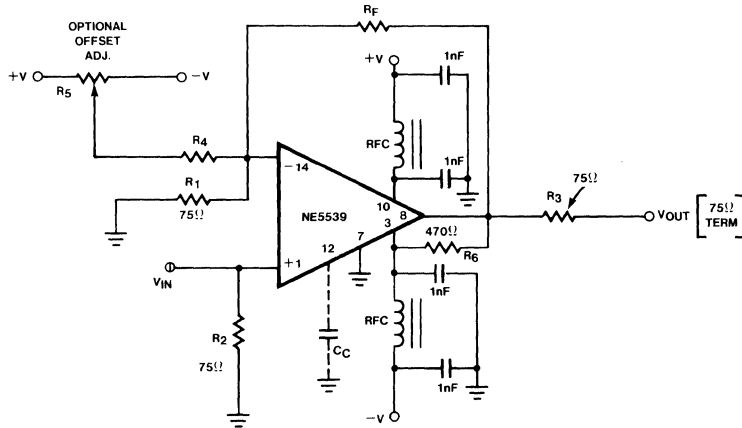
GAIN BANDWIDTH PRODUCT vs FREQUENCY



NOTE

 Indicates typical distribution $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$

28dB NON-INVERTING AMP
SAMPLE P.C. LAYOUT

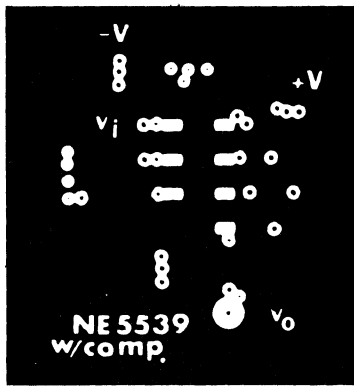


R₁ = 75Ω 5% CARBON
R₂ = 75Ω 5% CARBON
R₃ = 75Ω 5% CARBON
R₄ = 36K 5% CARBON

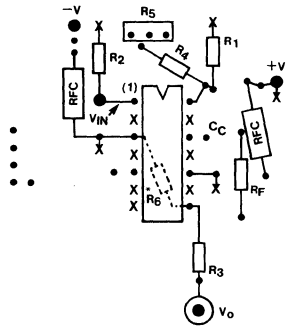
R₅ = 20K TRIMPOT (CERMET)
R_f = 1.5K (28dB GAIN)
R₆ = 470Ω 5% CARBON

RFC 3T # 26 BUSSWIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

TOP PLANE COPPER*
(Component Side)

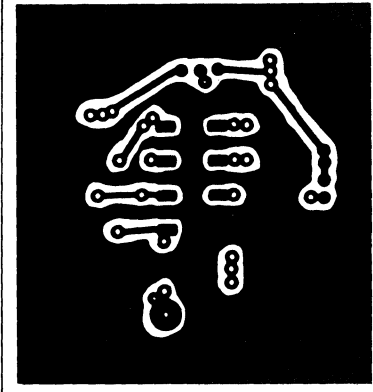


COMPONENT SIDE
(Component Layout)



NOTE
(X) indicates ground connection to top plane.
* R₆ is on bottom side.

BOTTOM PLANE
COPPER*



NOTE
Bond edges of top and bottom ground plane copper.

Figure 10

SMALL SIGNAL RESPONSE

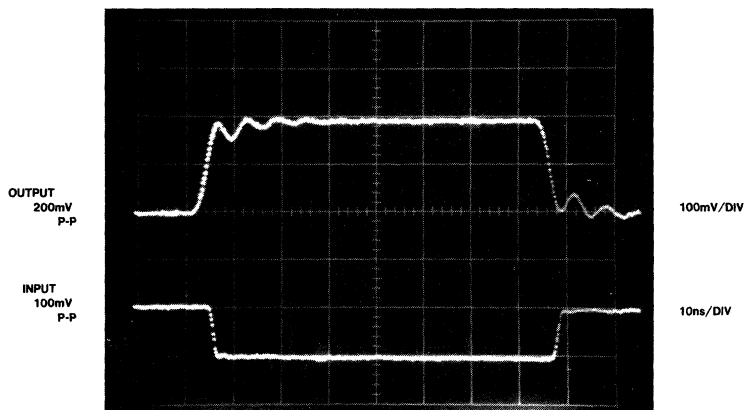


Figure 8

LARGE SIGNAL RESPONSE

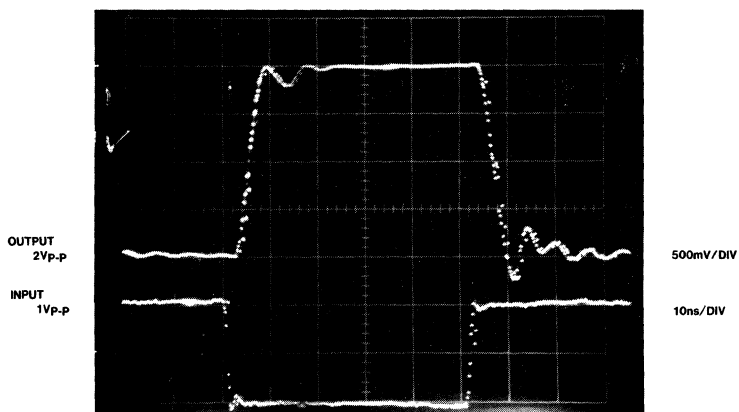


Figure 9

The primary reasoning behind this procedure is to force the closed loop circuit to appear as a gain of X7 above the critical frequency where phase changes rapidly (approx. 70MHz; refer to figure 7a). The lag network raises the phase at the upper operating frequencies, greatly improving the phase margin.

The calculations below show the application of these principles to the circuit in figure 7b.

The circuit shown has an inverting gain of 2, therefore solving for R₂:

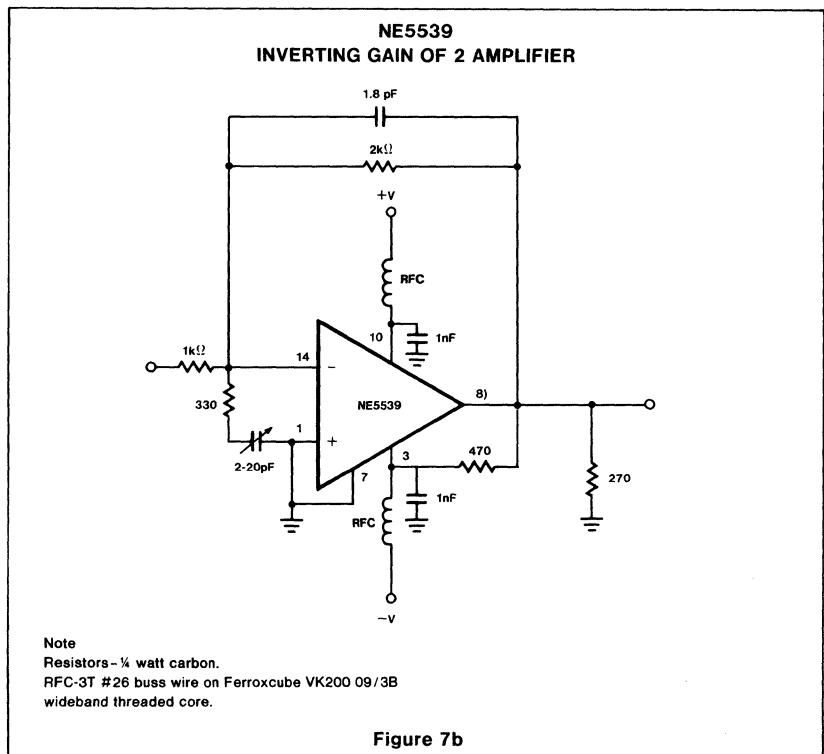
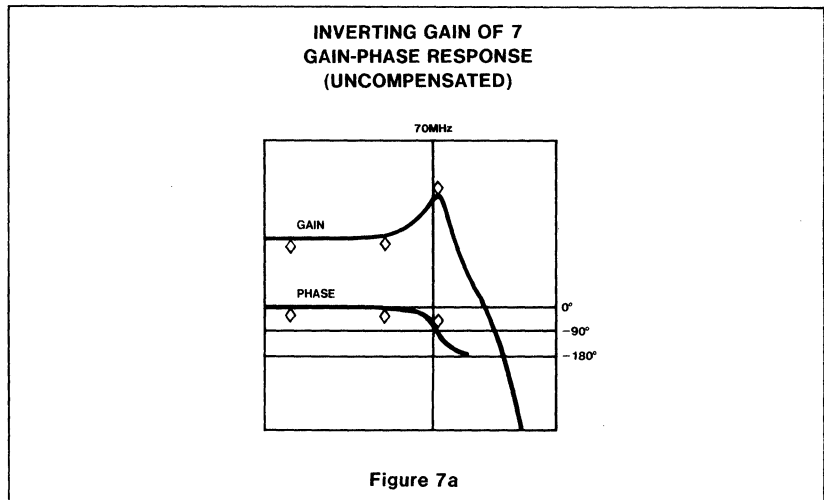
$$R_2 \leq \frac{R_f}{7 - |A_{CL}|} \leq \frac{2K}{7 - 2} = 400$$

Let R₂ = 330Ω

Assuming a gain bandwidth product of 350 MHz, C_G may now be calculated as follows:

$$\therefore C_G \approx \frac{5}{\pi \cdot 330 \cdot 350 \cdot 10^6} \approx 14\text{pF}$$

In the circuit shown, a lead compensation capacitor of ≈ 1.6pF was used with a value of R₂ of 330Ω and C_G was a 2 – 20pF trimmer cap (JFD piston-type). Rise and fall times of 2.8 to 3ns were measured in the small signal mode with quite adequate range in the lag compensation trimmer to optimize overshoot and reduce ringing (see pulse response—figures 9 and 10).



CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. A double-sided printed circuit board will result in more favorable system operation (see figure 10).

The effect of the distributed and input capacitance added by the inverting node of the amplifier must be considered when calculating actual system closed loop performance. The RC product of the input resistor (R_{IN}) in parallel with C_{DIST} and feedback resistor (R_F) create a pole at pin 14 (figure 5). This frequency must fall beyond the unity gain frequency of the system in order to maintain stability and system performance.

CLOSED LOOP GAIN LESS THAN 7

The NE5539 is stable for all closed loop gains greater than seven (7). When operating at gains less than seven (7), the device can become unstable. The circuit in figure 7 is an example of a unity gain inverting amplifier. The compensation components are added to obtain stable operation.

Capacitor C_L improves the phase margin (of the operational amplifier) by compensating for the lag introduced by the distributed capacitor (C_D).

It can be shown that the optimal conditions for amplifier stability occur when $R_1 C_D = R_F C_L$; however, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed loop amplifier will be reduced.

The actual value for C_L , based on a distributed capacitance of 3.5pFd, would be $\approx 2pF$.

Determination of Compensation Capacitance:

$$C_{lead} = \frac{C_{dist}}{ACL}$$

The above equation defines the relationship between the distributed capacitance, closed loop gain (ACL), and the compensation capacitor (C_L). For closed loop stability and gains less than 5, C_{lead} becomes a practical consideration. When bandwidth is of primary concern, the simple lead compensation will usually be adequate. However, if transient response is also a factor in the design, then a lag compensation network (C_G, R_2) may be necessary.

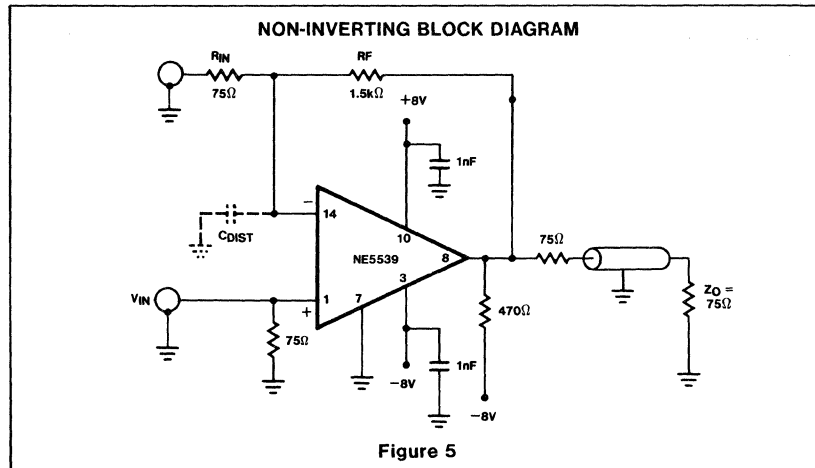


Figure 5

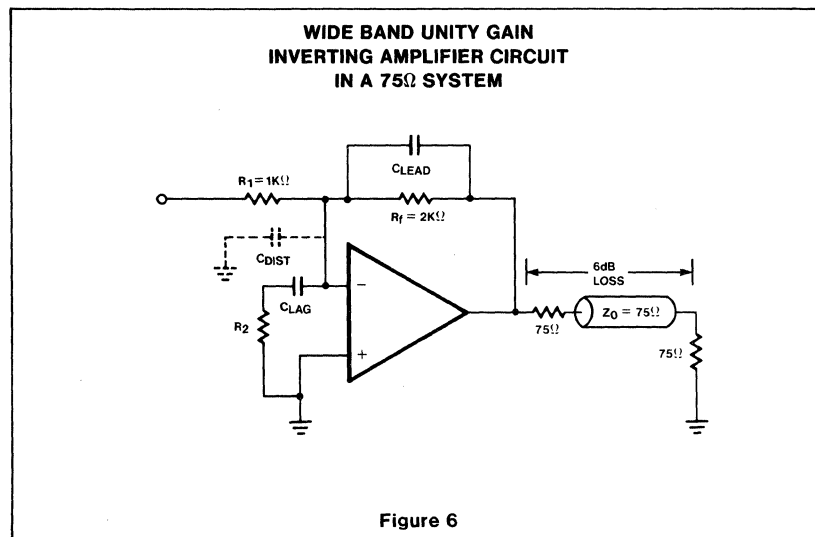


Figure 6

For practical applications, the following equations can be used to determine the proper lag compensation components:

$$\frac{R_f}{R_1 \parallel R_2} \geq 7 \quad \text{(Equation 1)}$$

$$\therefore R_2 \leq \frac{R_f}{7 - ACL} \quad \text{(Equation 2)}$$

(Using Equation 1 to insure a closed loop gain of X7 above the network break frequency allows you to solve for R_2 , the lag network resistor.)

C_{lag} may be approximated by the following equations. First set the lag network break frequency in relation to the amplifier total gain product (open loop).

$$\text{Set } \omega_{lag} \approx \frac{2\pi \cdot GBW}{10} \text{ rad/sec}$$

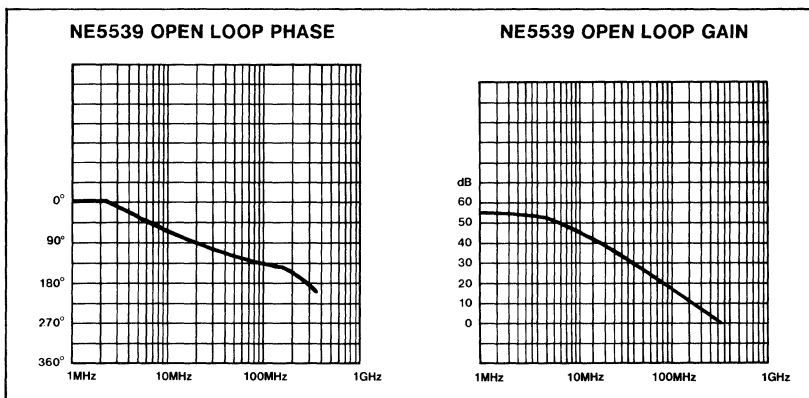
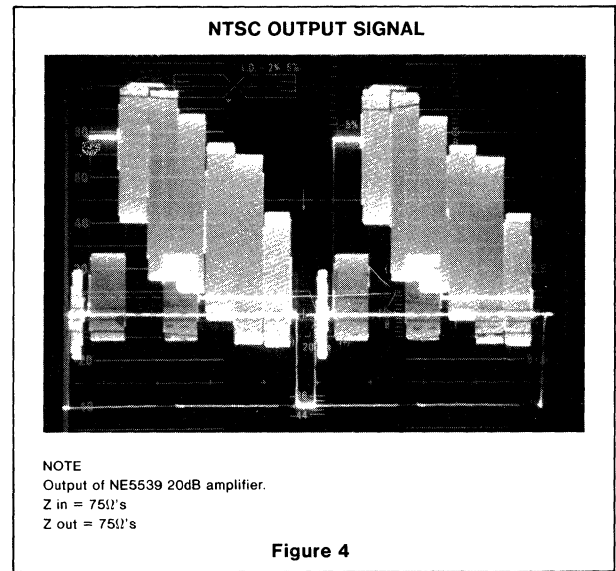
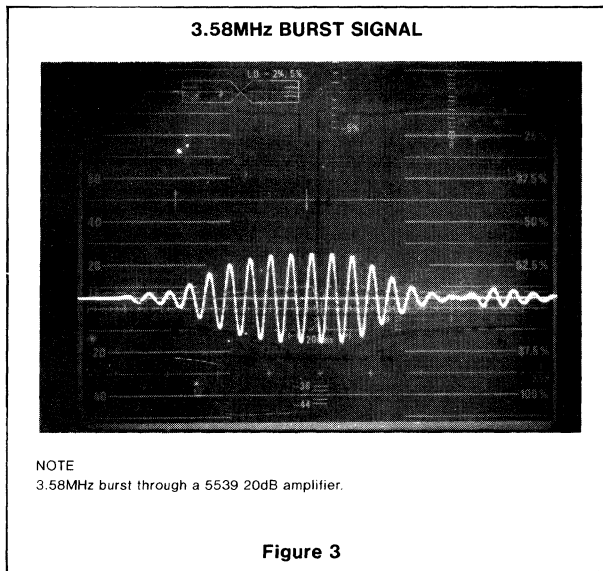
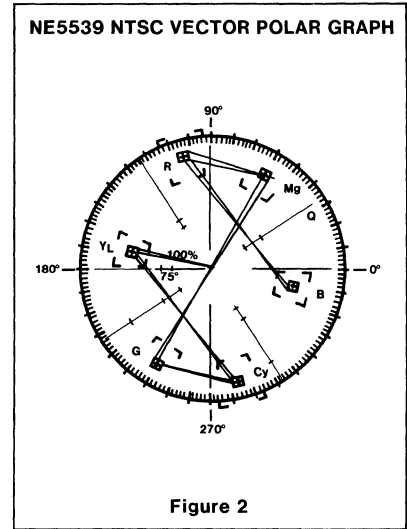
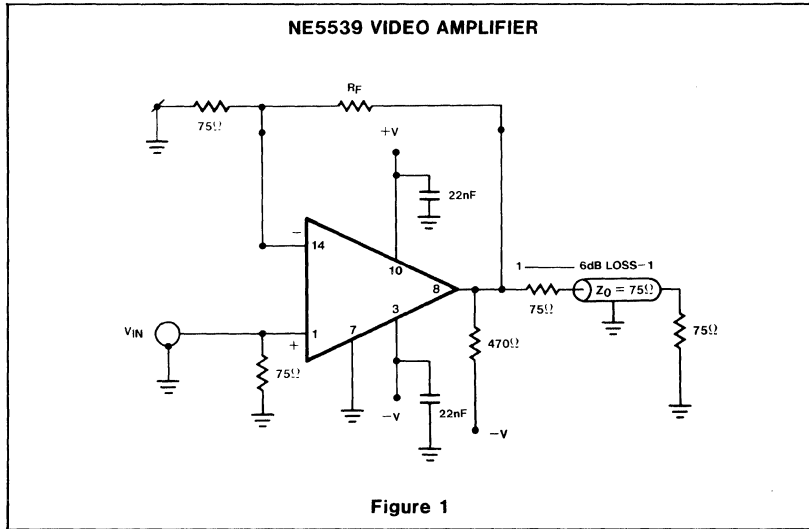
$$\approx \frac{\pi \cdot GBW}{5} \text{ rad/sec.}$$

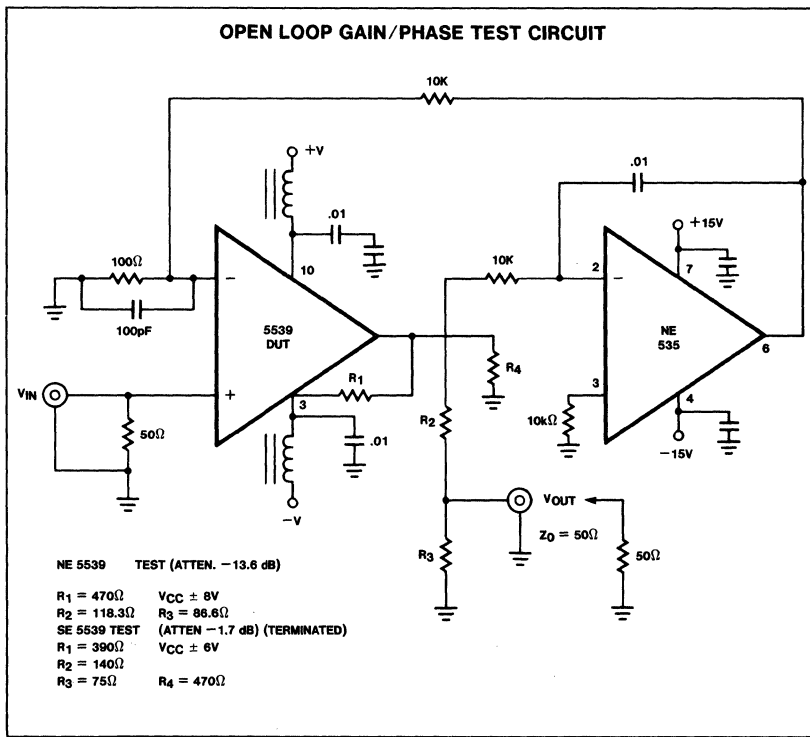
$$\text{then } \omega_{lag} = \frac{1}{R_2 C_{lag}}$$

and C_{lag} may now be determined.

$$\therefore C_{lag} \approx \frac{5}{\pi \cdot R_2 \cdot GBW}$$

$$< \text{Assume } GBW = 350\text{MHz} > \quad \text{(Equation 3)}$$





μ A741/741C-N,FE
SA741C-N
 μ A741C-D

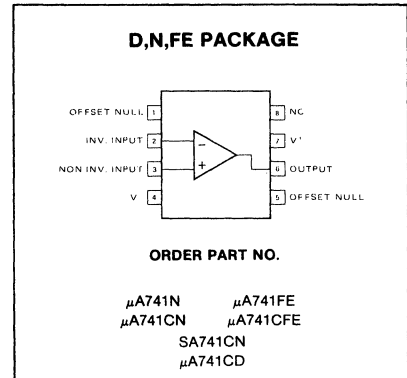
DESCRIPTION

The μ A741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μ A741 is short-circuit protected and allows for nulling of offset voltage.

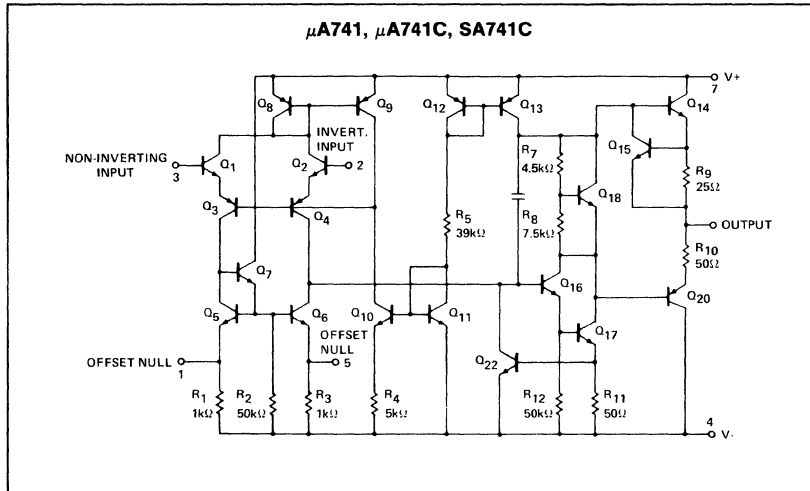
FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μ A741C	± 18	V
μ A741	± 22	V
Internal power dissipation		
N package	500	mW
FE package	1000	mW
Differential input voltage	± 30	V
Input voltage ¹	± 15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μ A741C	0 to +70	$^{\circ}$ C
SA741C	-40 to +85	$^{\circ}$ C
μ A741	-55 to +125	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature (soldering 60sec)	300	$^{\circ}$ C

NOTE

1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V _{OS}	Offset voltage	R _S = 10kΩ R _S = 10kΩ, over temp.		1.0 1.0	5.0 6.0		2.0 6.0 7.5	mV mV	
I _{OS}	Offset current	Over temp. T _A = +125°C T _A = -55°C		20 7.0 20	200 200 500		20 300 300	nA nA nA nA	
I _{BIAS}	Input bias current	Over temp. T _A = +125°C T _A = -55°C		80 30 300	500 500 1500		80 500 800	nA nA nA nA	
V _{OUT}	Output voltage swing	R _L = 10kΩ R _L = 2kΩ, over temp.	±12 ±10	±14 ±13		±12 ±10	±14 ±13	V V	
AVOL	Large signal voltage gain	R _L = 2kΩ, V _O = ±10V R _L = 2kΩ, V _O = ±10V, over temp.	50 25	200		20 15	200	V/mV V/mV	
	Offset voltage adjustment range			±30			±30	mV	
PSRR	Supply voltage rejection ratio	R _S ≤ 10kΩ R _S ≤ 10kΩ, over temp.		10	150		10 150	μV/V μV/V	
CMRR	Common mode rejection ratio	Over temp.	70	90				dB dB	
I _{CC}	Supply current	T _A = +125°C T _A = -55°C		1.4 1.5 2.0	2.8 2.5 3.3		1.4 2.8	mA mA mA	
V _{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13	V	
R _{IN}	Input resistance		0.3	2.0		0.3	2.0	MΩ	
P _d	Power consumption	T _A = +125°C T _A = -55°C		50 45 45	85 75 100		50 85	mW mW mW	
R _{OUT}	Output resistance			75			75	Ω	
I _{SC}	Output short-circuit current			25			25	mA	

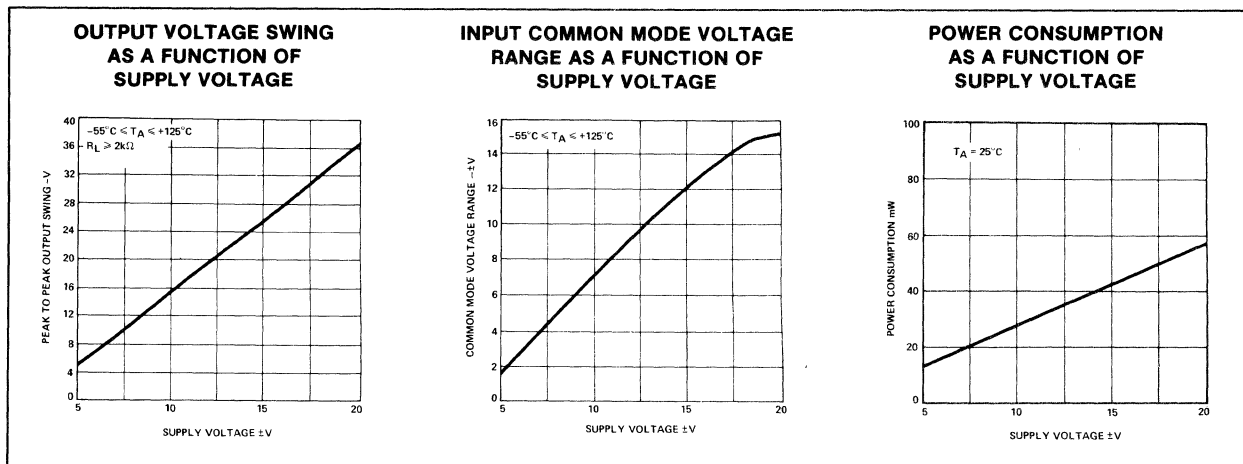
DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	SA741C			UNIT
		Min	Typ	Max	
V _{OS} Offset voltage	R _S = 10k Ω R _S = 10k Ω , over temp.		2.0	6.0	mV
				7.5	mV
I _{OS} Offset current	Over temp.		20	200	nA
				500	nA
I _{BIAS} Input bias current	Over temp.		80	500	nA
				1500	nA
V _{OUT} Output voltage swing	R _L = 10k Ω R _L = 2k Ω , over temp.	± 12	± 14		V
		± 10	± 13		V
A _{VOL} Large signal voltage gain	R _L = 2k Ω , V _O = $\pm 10\text{V}$ R _L = 2k Ω , V _O = $\pm 10\text{V}$, over temp.	20	200		V/mV
		15			V/mV
Offset voltage adjustment range			± 30		mV
PSRR Supply voltage rejection ratio	R _S \leq 10k Ω		10	150	$\mu\text{V/V}$
CMRR Common mode rejection ratio					dB
I _{CC} Supply current			1.4	2.8	mA
V _{IN} Input voltage range	(μ A741, over temp.)	± 12	± 13		V
R _{IN} Input resistance		0.3	2.0		M Ω
P _d Power consumption			50	85	mW
R _{OUT} Output resistance			75		Ω
I _{SC} Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

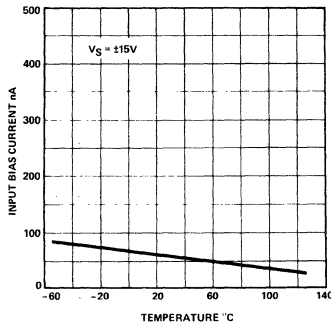
PARAMETER	TEST CONDITIONS	μ A741, μ A741C			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				M Ω
Parallel input capacitance	Open loop, f = 20Hz		1.4		pF
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	V _{IN} = 20mV, R _L = 2k Ω , C _L \leq 100pf				
Rise time			0.3		μs
Overshoot			5.0		%
Slew rate	C \leq 100pf, R _L \geq 2k, V _{IN} = $\pm 10\text{V}$		0.5		V/ μs

TYPICAL PERFORMANCE CHARACTERISTICS

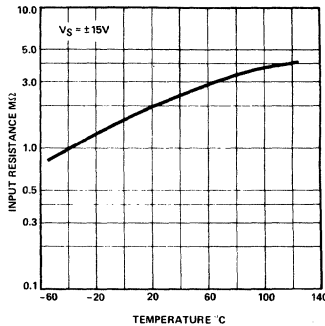


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

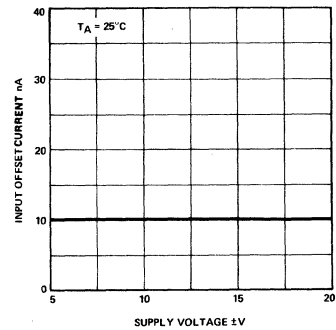
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



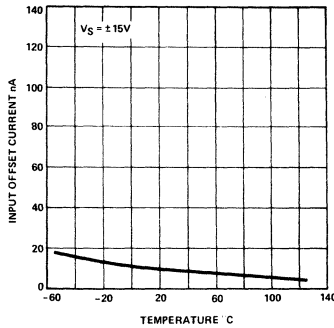
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



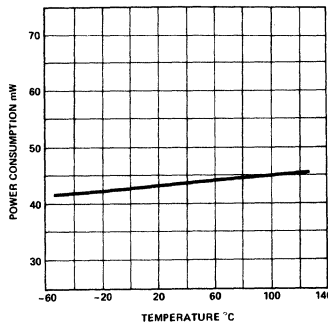
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



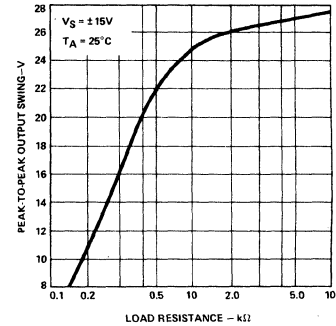
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



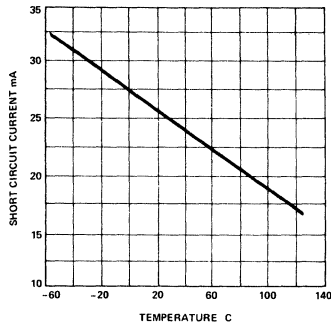
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



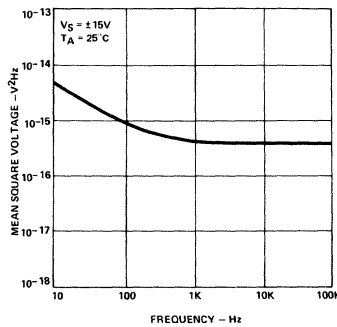
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



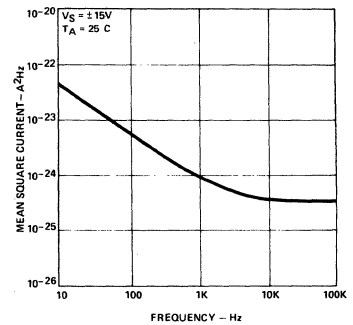
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

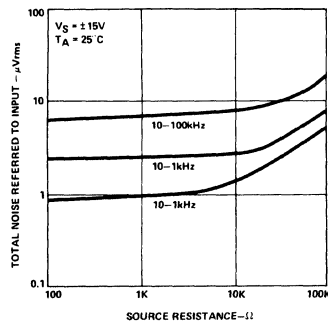


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

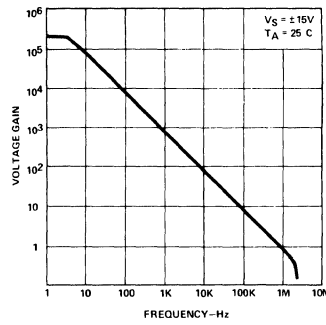


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

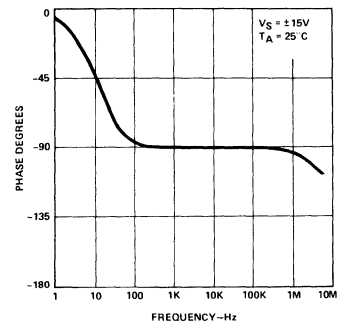
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



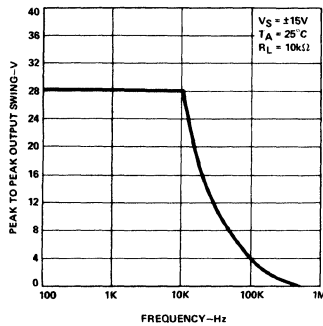
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



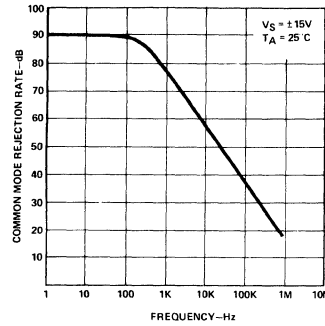
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



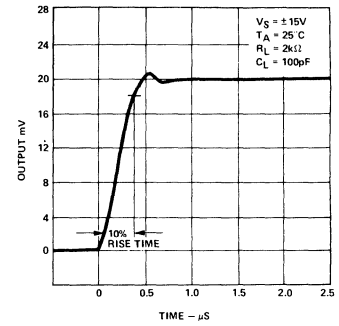
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



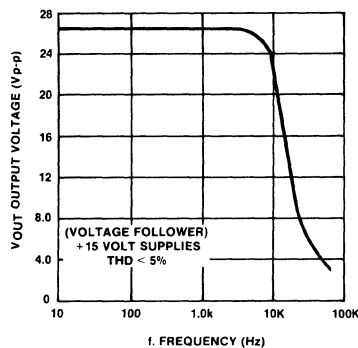
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



μ A747/747C-F,H,N
SA747C-N
 μ A747C-D

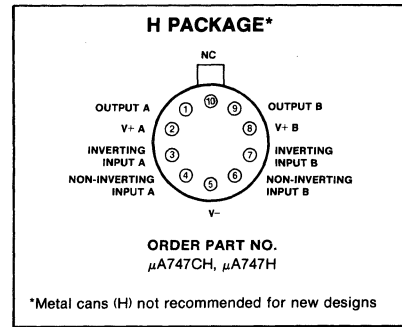
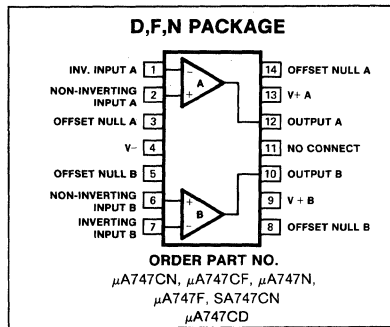
DESCRIPTION

The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μ A741 data sheet.

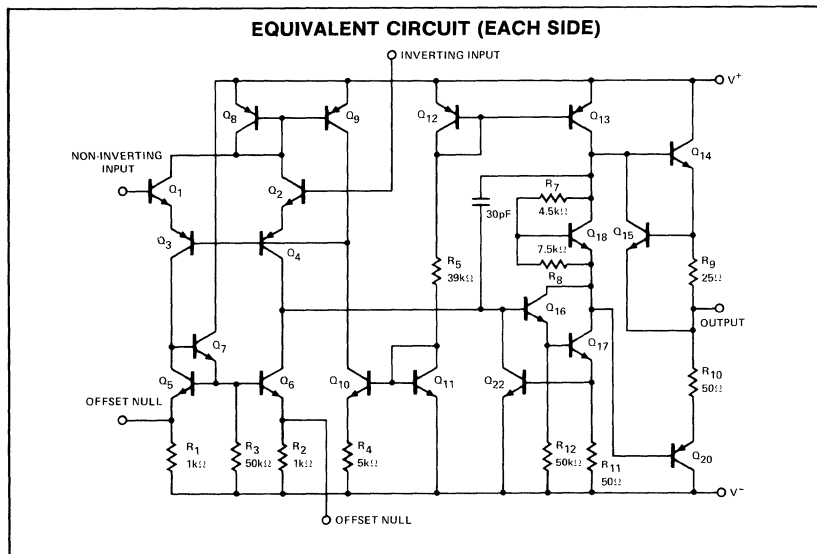
FEATURES

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		V
μ A747	±22	V
μ A747C	±18	V
SA747C	±18	V
Internal power dissipation		mW
H Package	500	mW
N,F Packages	670	mW
Differential input voltage	±30	V
Input voltage	±15	V
Voltage between offset null and V-	±0.5	V
Storage temperature range	-65 to +155	°C
Operating temperature range		°C
μ A747	-55 to +125	°C
μ A747C	0 to +70	°C
SA747C	-40 to +85	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short-circuit duration	indefinite	

μA747/747C-F,H,N
SA747C-N
μA747C-D

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SA747C			UNIT
		Min	Typ	Max	
V _{OS} Offset voltage	$R_S \leq 10\text{k}\Omega$		2.0	6.0	mV
	$R_S \leq 10\text{k}\Omega$, over temp		3.0	7.5	mV
I _{OS} Offset current	Over temp		20	200	nA
				500	nA
I _{BIAS} Input current	Over temp			500	nA
				1500	nA
V _{OUT} Output voltage swing	$R_L \geq 2\text{k}\Omega$, over temp	±10	±13		V
	$R_L \geq 10\text{k}\Omega$, over temp	±12	±14		V
I _{CC} Supply current	Over temp		1.7	2.8	mA
			2.0	3.3	mA
Power consumption	Over temp		50	85	mW
			60	100	mW
Input capacitance			1.4		pF
Offset voltage adjustment range			±15		V
Output resistance			75		Ω
Channel separation			120		dB
P _{SRR} Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$, over temp		30	150	μV/V
A _{VOL} Large signal voltage gain (DC)	$R_L \geq 2\text{k}\Omega$ V _{OUT} = ±10V	25,000			V/V
C _{MRR}	$R_S \leq 10\text{k}\Omega$, V _{CM} ±12V over temp	70			dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA747/μA747C/SA747C			UNIT
		Min	Typ	Max	
Transient response Risetime Overshoot	V _{IN} = 20mV, R ₁ = 2kΩ, C ₁ < 100pf Unity gain CL ≤ 100pf Unity gain CL ≤ 100pf		0.3		μs
			5.0		%
			0.5		V/μs
Slew rate	R _L > 2kΩ		0.5		V/μs

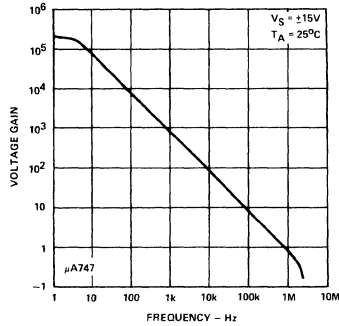
μA747/747C-F,H,N
SA747C-N
μA747C-D

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

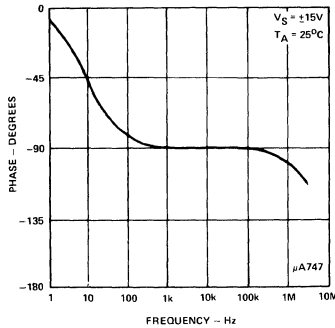
PARAMETER	TEST CONDITIONS	μA747			μA747C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage	R _S ≤ 10kΩ R _S ≤ 10kΩ, over temp		2.0	5.0		2.0	6.0	mV
			3.0	6.0		3.0	7.5	mV
I _{OS} Offset current	T _A = +125°C T _A = -55°C Over temp		20	200		20	200	nA
			7.0	200				nA
			85	500		7.0	300	nA
I _{BIAS} Input current	T _A = 125°C T _A = -55°C Over temp		80	500		80	500	nA
			30	500				nA
			300	1500				nA
						30	800	
V _{OUT} Output voltage swing	R _L ≥ 2kΩ, over temp R _L ≥ 10kΩ, over temp	±10	±13		±10	±13		V
		±12	±14		±12	±14		V
I _{CC} Supply current each side	T _A = 125°C T _A = -55°C Over temp		1.7	2.8		1.7	2.8	mA
			1.5	2.5				mA
			2.0	3.3		2.0	3.3	mA
Power consumption	T _A = 125°C T _A = -55°C Over temp		50	85		50	85	mW
			45	75				mW
			60	100				mW
						60	100	
Input capacitance		1.4			1.4		pF	
Offset voltage adjustment range		±15			±15		V	
Output resistance		75			75		Ω	
Channel separation		120			120		dB	
P _{SRR} Supply voltage rejection ratio	R _S ≤ 10kΩ, over temp		30	150		30	150	μV/V
A _{VOL} Large signal voltage gain (DC)	R _L ≥ 2kΩ V _{OUT} = ±10V Over temp	50,000			25,000			V/V
		25,000			15,000			V/V
CMRR	R _S ≤ 10KΩ, V _{CM} ±12V over temp	70			70			dB

TYPICAL PERFORMANCE CHARACTERISTICS

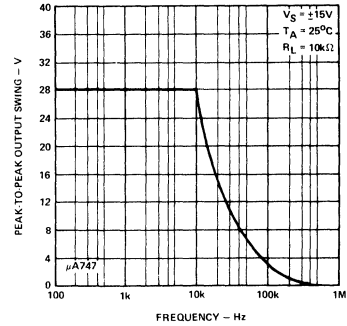
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



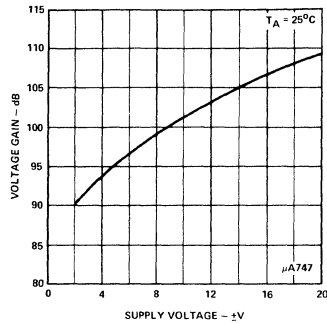
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



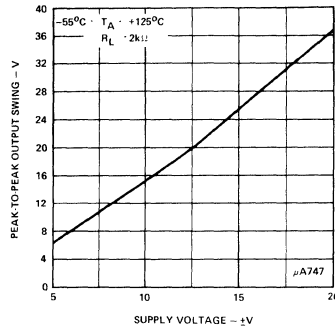
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



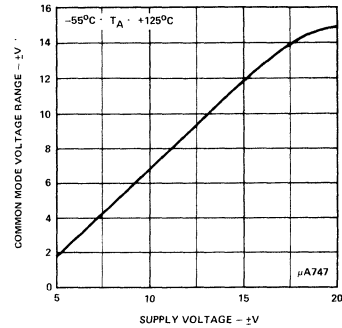
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



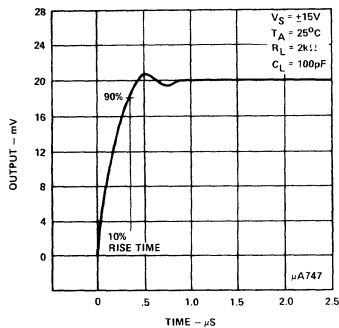
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



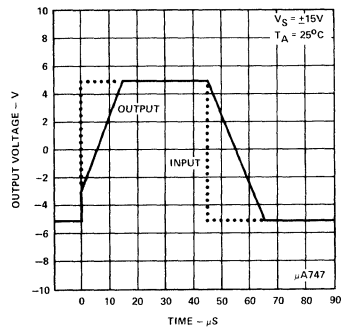
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



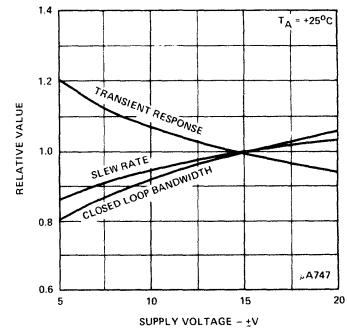
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

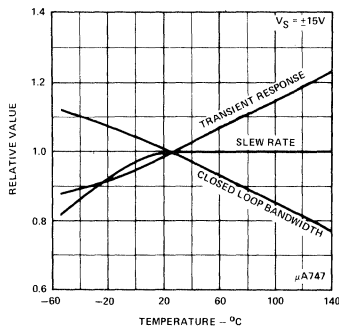


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

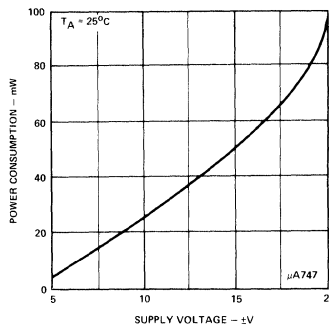


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

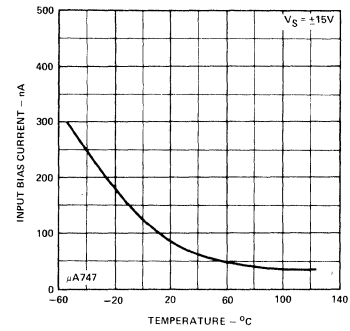
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



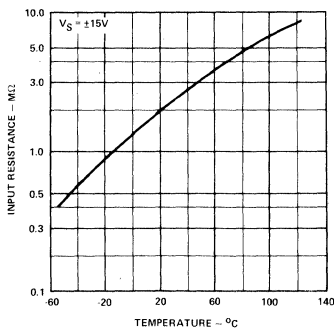
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



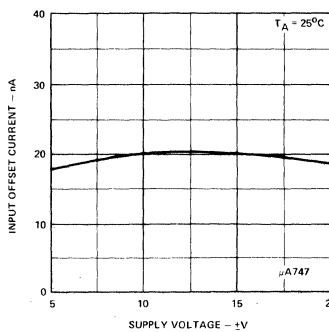
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



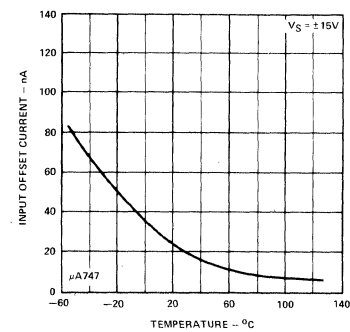
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



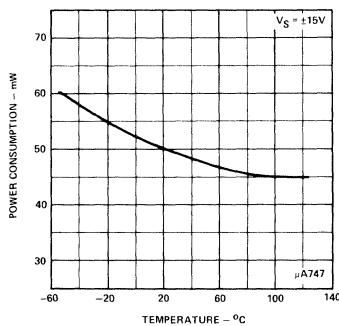
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



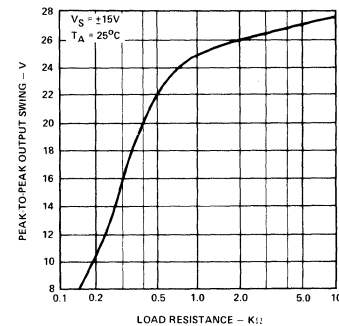
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



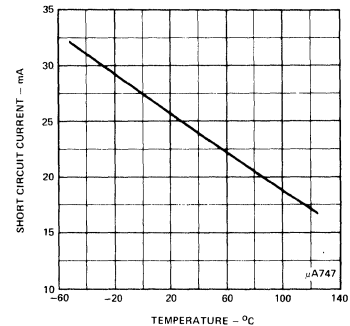
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

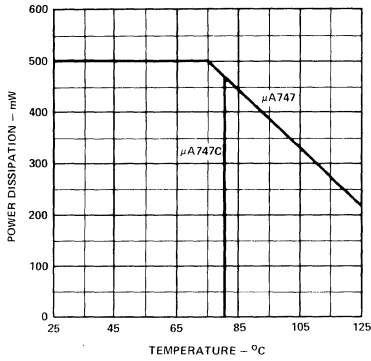


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

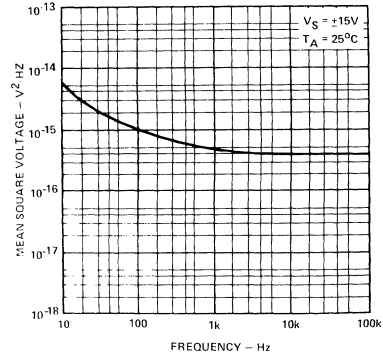


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

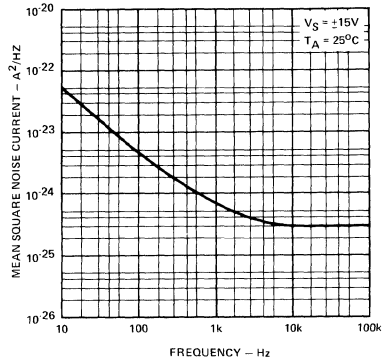
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



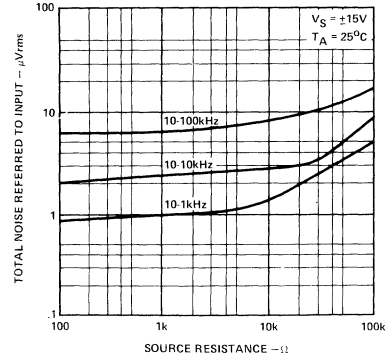
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

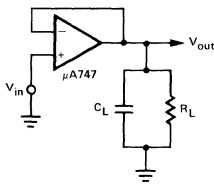


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

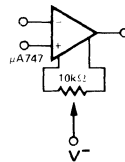


TEST CIRCUITS

TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



DESCRIPTION

The 748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

- Short circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

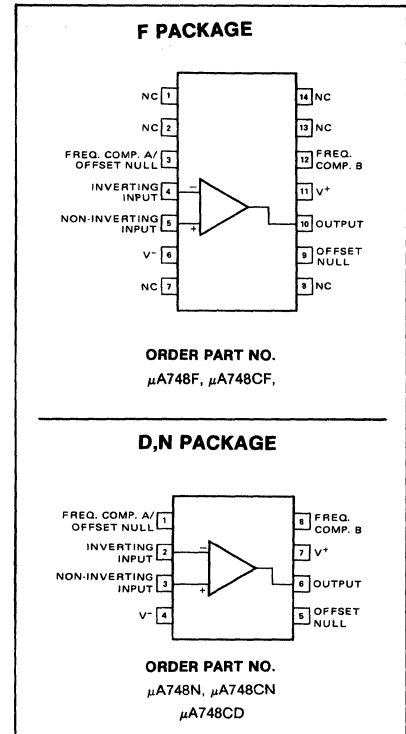
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μ A748	± 22	V
μ A748C	± 18	V
Internal power dissipation ¹	500	mW
Differential output voltage	± 30	V
Input voltage ²	± 15	V
Storage temperature range	-65 to +150	$^{\circ}$ C
Operating temperature range		
μ A748	-55 to +125	$^{\circ}$ C
μ A748C	0 to +70	$^{\circ}$ C
Lead temperature	300	$^{\circ}$ C
Output short circuit duration ³	indefinite	

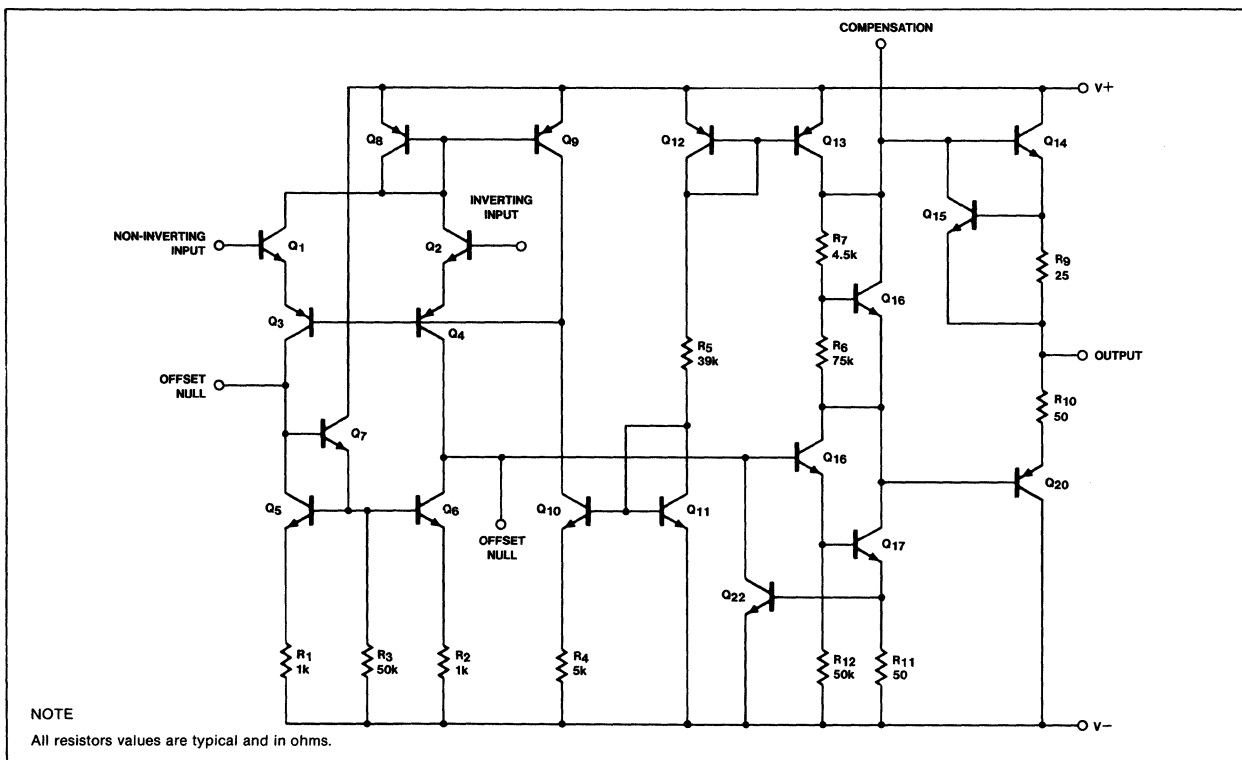
NOTES

1. Rating applies for case temperatures to +70 $^{\circ}$ C.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70 $^{\circ}$ C ambient temperature.

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA748			μA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage	R _S ≤ 10kΩ, T _A = 25°C Over temperature		1.0	5.0 6.0		2.0	6.0 7.5	mV mV
I _{OS} Offset current	25° ≤ T _A ≤ T _{max} T _{min} ≤ T _A ≤ 25°C		20 7.0 85	200 200 500		20 9.0 35	200 300 300	nA nA nA
I _{BIAS} Input current	25° ≤ T _A ≤ T _{max} T _{min} ≤ T _A ≤ 25°C		80 30 300	500 500 1500		80 40 130	500 800 800	nA nA nA
V _{CM} Common mode voltage range	Over temperature	±12	±13		±12	±13		V

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

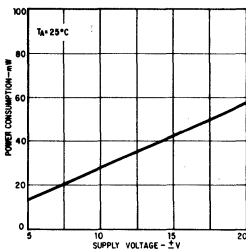
PARAMETER	TEST CONDITIONS	μA748			μA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
C _{MRR} Common mode rejection ratio	R _S ≤ ±10kΩ, over temperature	70	90		70	90		dB
R _{IN} Input resistance		0.3	2.0		.30	2.0		MΩ
V _{OUT} Output voltage swing	R _L ≥ 2kΩ, over temperature R _L ≥ 10kΩ, over temperature	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I _{CC} Supply current	25° ≤ T _A ≤ T _{max} T _{min} ≤ T _A ≤ 25°C		1.7 1.5 2.0	2.83 2.50 3.33		1.7 1.6 1.8	2.83 3.33 3.33	mA mA mA
P _d Power consumption	T _A = 25°C 25° ≤ T _A ≤ T _{max} T _{min} ≤ T _A ≤ 25°C		50 45 60	85 75 100		50 48 54	85 100 100	mW mW mW
P _{SRR} Supply voltage rejection ratio	R _S ≤ 10kΩ, over temperature		30	150		30	150	μV/V
Output resistance	T _A = 25°C		75			75		Ω
A _{VOL} Large signal voltage gain	R _L ≥ 2kΩ V _{OUT} ±10V ±15V Over temperature	50	200		50	200		V/mV V/mV
Input capacitance			1.4			1.4		pF
Offset voltage adjustment range			±15			±15		mV

AC ELECTRICAL CHARACTERISTICS

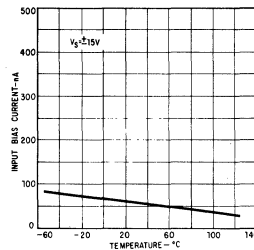
PARAMETER	TEST CONDITIONS	μA748			μA748C/SA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response (unity gain)	V _{IN} = 20mV, R _L = 2kΩ C _L ≤ 100pF C ₁ = 30pF							
Rise time			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew rate	R _L ≥ 2kΩ C ₁ = 30pF		0.5			0.5		V/μs

TYPICAL CHARACTERISTIC CURVES

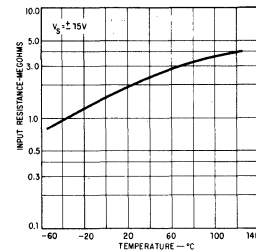
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



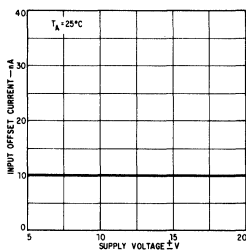
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



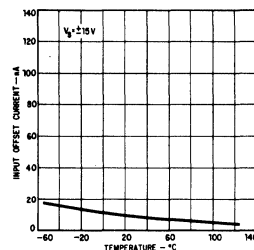
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



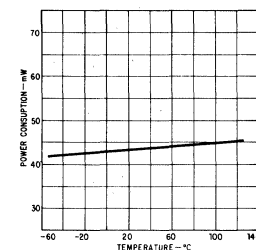
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



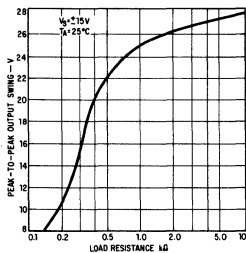
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



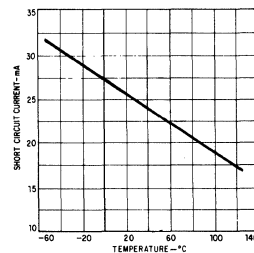
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



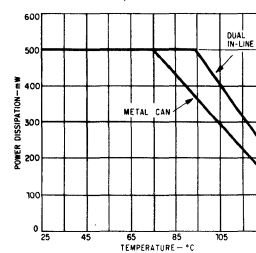
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



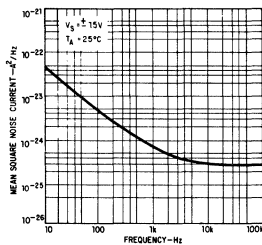
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



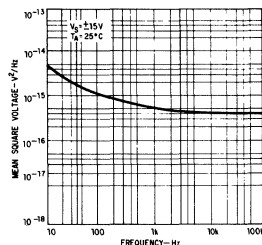
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



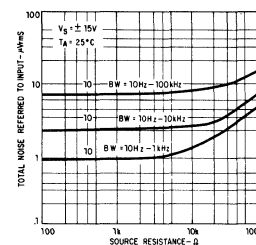
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

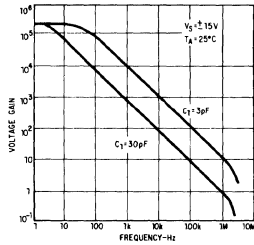


BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE

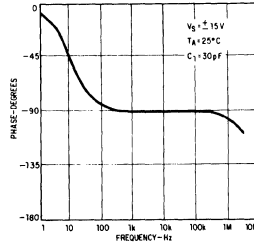


TYPICAL CHARACTERISTIC CURVES (Cont'd)

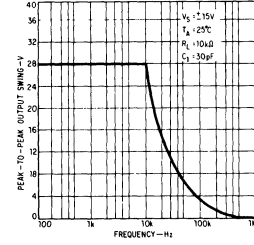
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



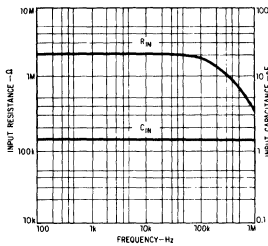
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



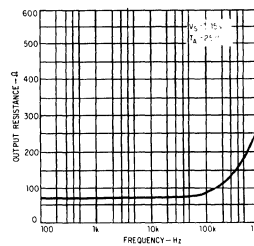
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



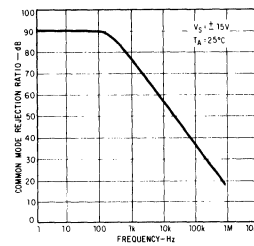
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



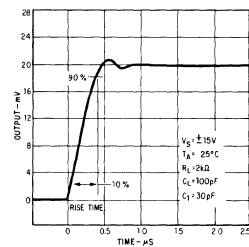
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



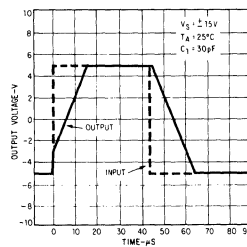
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



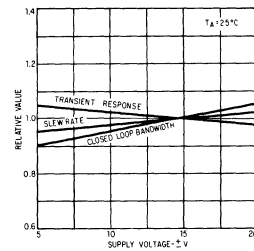
TRANSIENT RESPONSE



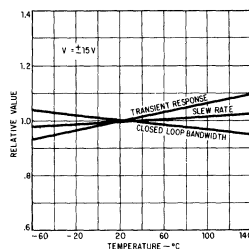
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



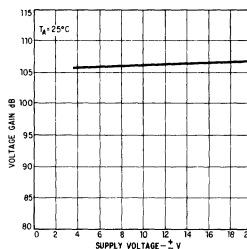
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



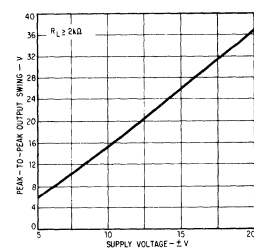
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



SECTION 2

VIDEO AMPLIFIERS

Section 2 — VIDEO AMPLIFIERS

NE/SE592	Video Amplifier	137
μ A733/733C	Differential Video Amplifier	143

NE592-D,F,H,N
SE592-F,H

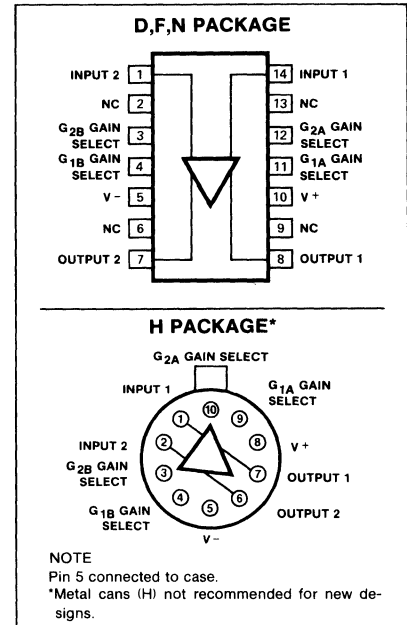
DESCRIPTION

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The 592 is a pin-for-pin replacement for the μ A733.

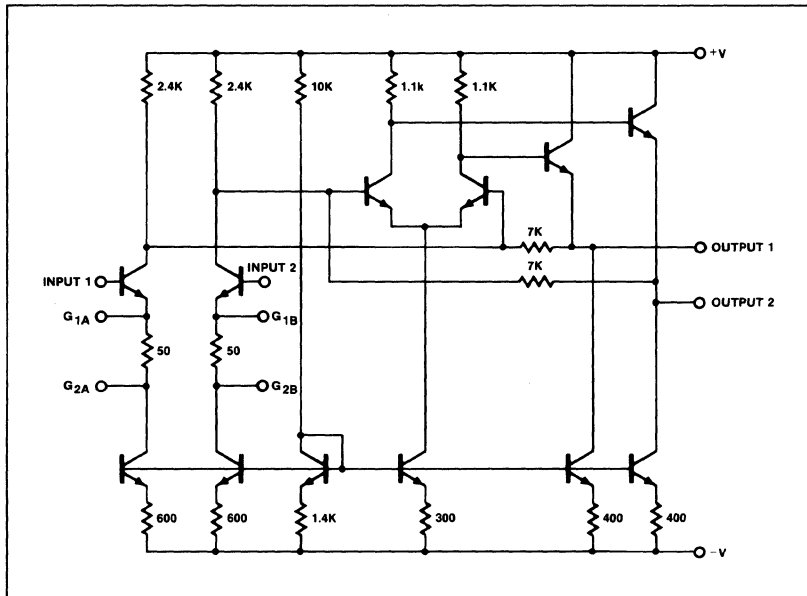
FEATURES

- 120MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	± 8	V
Differential input voltage	± 5	V
Common mode		
Input voltage	± 6	V
Output current	10	mA
Operating temperature range		
SE592K	-55 to +125	$^\circ\text{C}$
NE592K	0 to +70	$^\circ\text{C}$
Storage temperature range	-65 to +150	$^\circ\text{C}$
Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $V_{CM} = 0$ unless otherwise specified
Recommend operating supply voltages $V_S = \pm 6.0\text{V}$

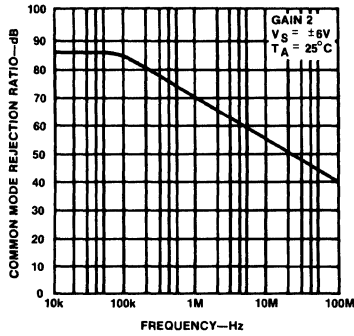
PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain Gain 11 Gain 22	$R_L = 2\text{k}\Omega$, $V_{OUT} = 3\text{V p-p}$	250 80	400 100	600 120	300 90	400 100	500 110	V/V V/V
Bandwidth Gain 11 Gain 22 Rise time Gain 11 Gain 22	$V_{OUT} = 1\text{V p-p}$		40 90 10.5 4.5			40 90 10.5 4.5		MHz MHz ns ns
Propagation delay Gain 11 Gain 22	$V_{OUT} = 1\text{V p-p}$		7.5 6.0			7.5 6.0		ns ns
Input resistance Gain 11 Gain 22 Input capacitance ² Input offset current Input bias current Input noise voltage Input voltage range	Gain 2 BW 1kHz to 10MHz	10	4.0 30 2.0 0.4 9.0 12		20	4.0 30 2.0 0.4 9.0 12		k Ω k Ω pF μA μA μVrms V
Common mode rejection ratio Gain 2 Gain 2 Supply voltage rejection ratio Gain 2	$V_{CM} \pm 1\text{V}$, $F < 100\text{kHz}$ $V_{CM} \pm 1\text{V}$, $F = 5\text{MHz}$ $\Delta V_S = \pm 0.5\text{V}$	60	86 60		60	86 60		dB dB dB
Output offset voltage Gain 2 ² Output common mode voltage Output voltage swing differential Output resistance Power supply current	$R_L = \infty$ $R_L = \infty$ $R_L = 2\text{K}$ $R_L = \infty$		0.35 2.4 3.0 20 18	0.75 3.4 4.0 20 24		0.35 2.9 4.0 20 18		V V V Ω mA

NOTES

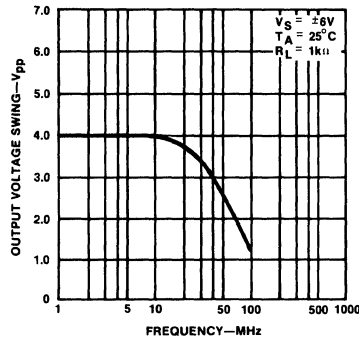
- Gain select pins G_{1A} and G_{1B} connected together.
- Gain select pins G_{2A} and G_{2B} connected together.
- All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

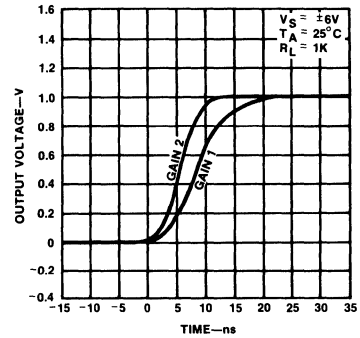
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



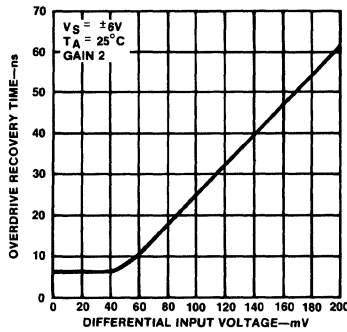
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



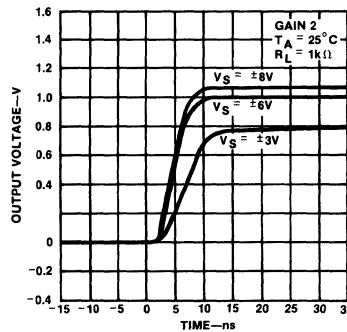
PULSE RESPONSE



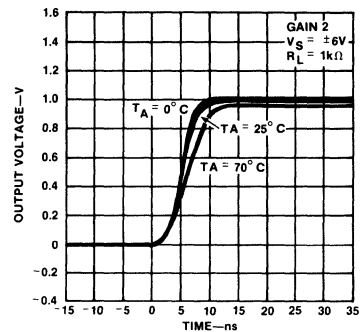
DIFFERENTIAL OVERDRIVE RECOVERY TIME



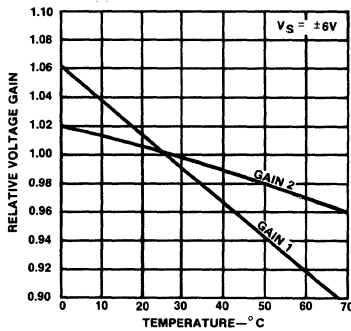
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



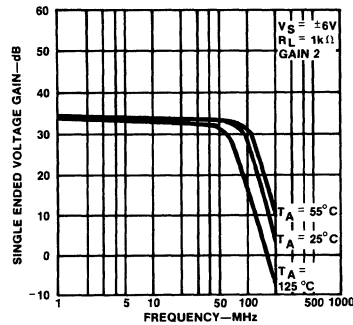
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



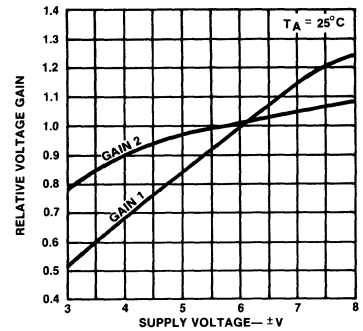
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

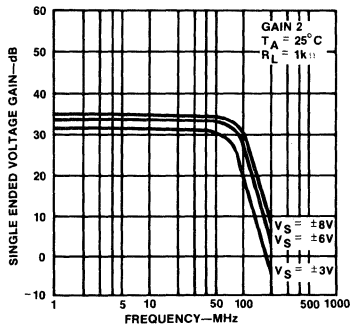


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

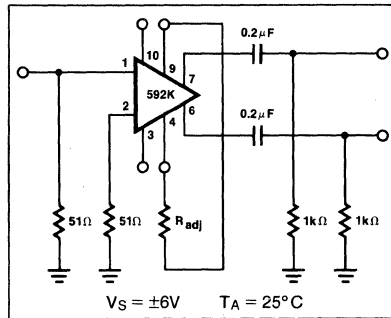


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

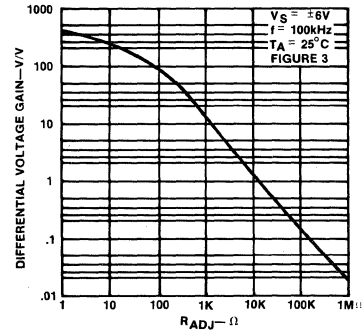
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



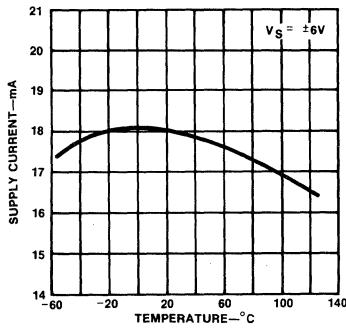
VOLTAGE GAIN ADJUST CIRCUIT



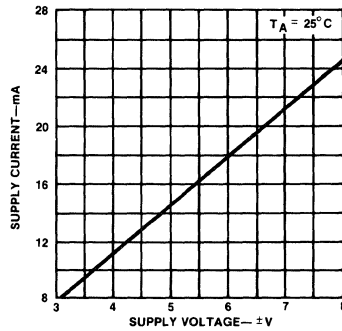
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



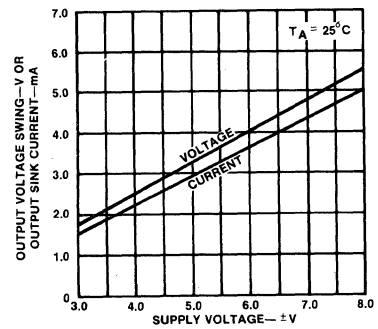
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



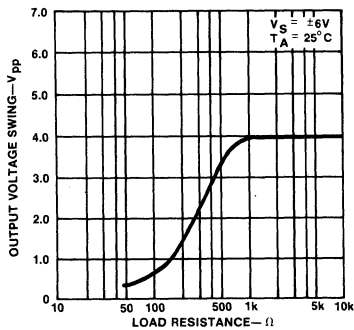
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



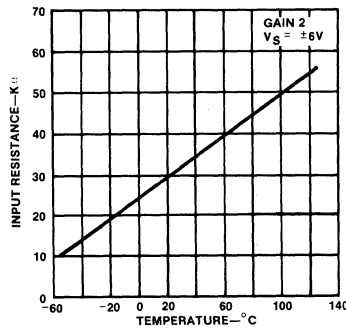
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



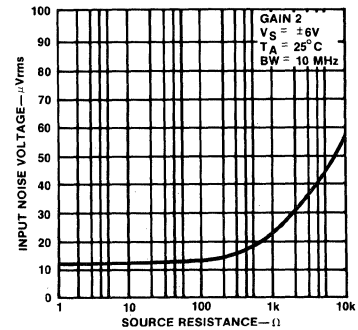
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

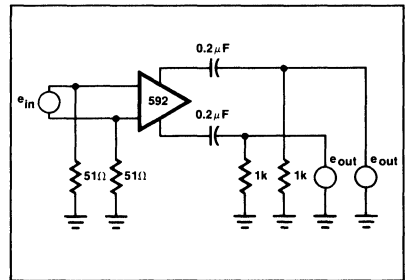
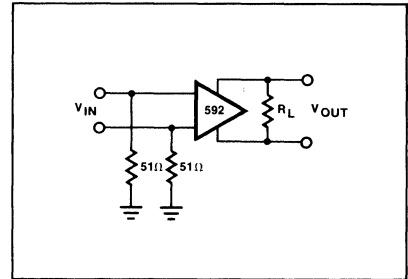
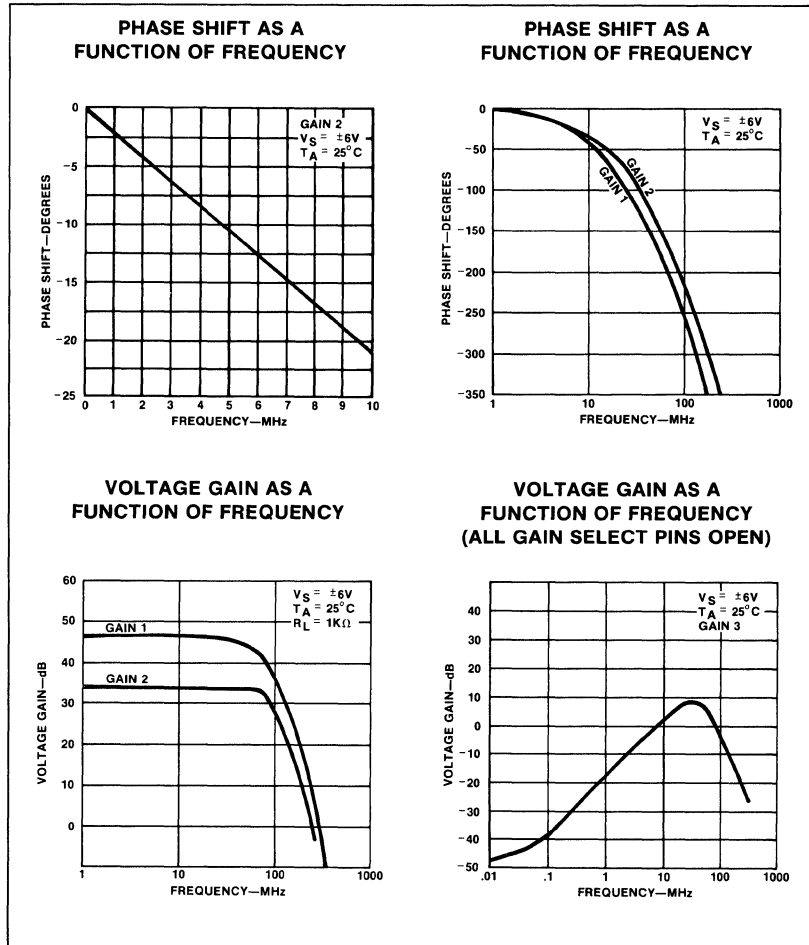


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



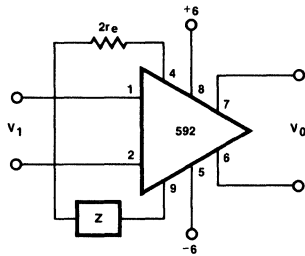
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

TEST CIRCUITS $T_A = 25^\circ\text{C}$ unless otherwise specified



TYPICAL APPLICATIONS

FILTER NETWORKS



$$\frac{V_0(s)}{V_1(s)} \approx \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\approx \frac{1.4 \times 10^4}{Z(s) + 32}$$

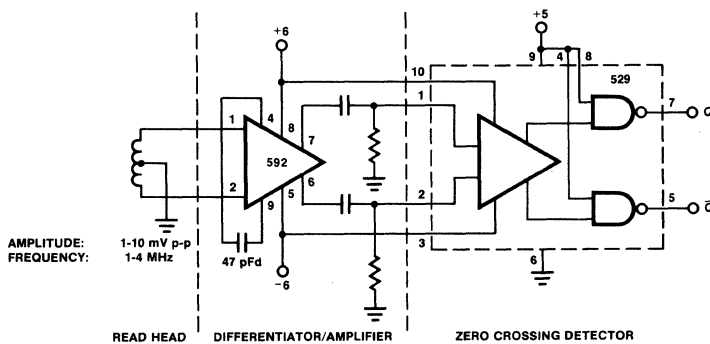
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$V_0(s)$ TRANSFER $V_1(s)$ FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L} \right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC} \right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/L s + 1/LC} \right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC} \right]$

NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω .

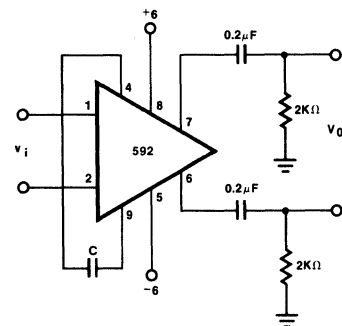
DISC/TAPE PHASE MODULATED READBACK SYSTEMS



AMPLITUDE: 1-10 mV p-p
FREQUENCY: 1-4 MHz

READ HEAD DIFFERENTIATOR/AMPLIFIER ZERO CROSSING DETECTOR

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $F_1 \ll 1/2 \pi (32) C$
 $V_0 \approx 1.4 \times 10^4 C \frac{dV_1}{dt}$

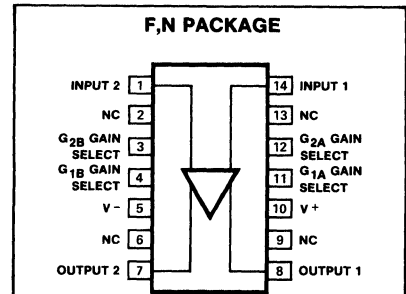
DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

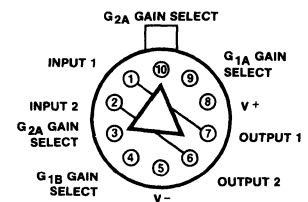
FEATURES

- 120MHz bandwidth
- 250kΩ input resistance
- Selectable gains of 10,100 and 400
- No frequency compensation required
- Mil std 883A,B,C available

PIN CONFIGURATION



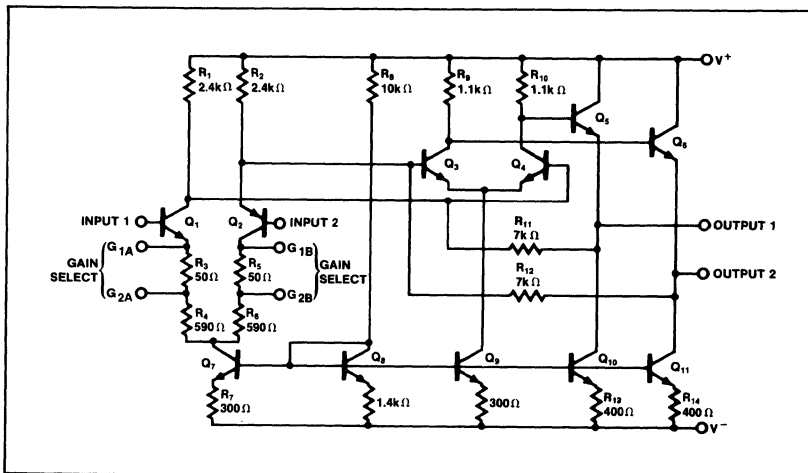
H PACKAGE *



NOTE

Pin 5 connected to case.
*Metal cans (H) not recommended for new designs

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Differential input Voltage	±5	V
Common mode input Voltage	±6	V
V _{CC}	±8	V
Output current	10	mA
Junction temperature	+150	°C
Storage temperature range	-65 to +150	°C
Operation temperature range		
μA733C	0 to +75	°C
μA733	-55 to +125	°C
P _D Power dissipation		
K package	500	mW
N, F package	670	mW

DC ELECTRICAL CHARACTERISTICS $T_A = +25^\circ\text{C}$, $V_S = \pm V$, $V_{CM} = 0$ unless otherwise specified.
Recommended operating supply voltages $V_S = \pm 6.0V$.

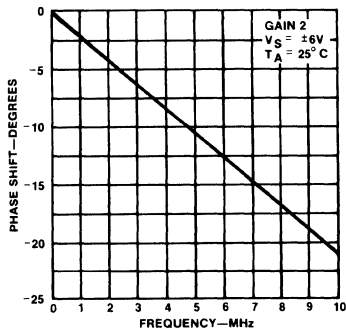
PARAMETER	TEST CONDITIONS	μA733C			μA733			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain Gain 1 ¹ Gain 2 ² Gain 3 ³	$R_I = 2k\Omega$, $V_{OUT} = 3V_{p-p}$	250 80 8.0	400 100 10	600 120 12	300 90 9.0	400 100 10	500 110 11	V/V V/V V/V
Bandwidth Gain 1 ¹ Gain 2 ² Gain 3 ³ Rise time Gain 1 ¹ Gain 2 ² Gain 3 ³	$V_{OUT} = 1V_{p-p}$		40 90 120 10.5 4.5 2.5			40 90 120 10.5 4.5 2.5		MHz MHz MHz ns ns ns
Propagation delay Gain 1 ¹ Gain 2 ² Gain 3 ³	$V_{OUT} = 1V_{p-p}$		7.5 6.0 3.6	10		7.5 6.0 3.6	10	ns ns ns
Input resistance Gain 1 ¹ Gain 2 ² Gain 3 ³ Input capacitance ² Input offset current Input bias current Input noise voltage Input voltage range	Gain 2 BW = 1kHz to 10MHz	10	4.0 30 250 2.0 0.4 9.0 12	5.0 30	20	4.0 30 250 2.0 0.4 9.0 12	3.0 20	kΩ kΩ kΩ pF μA μA μVrms V
Common mode Rejection ratio Gain 2 Gain 2 Supply voltage Rejection ratio Gain 2	$V_{CM} = \pm V, f \leq 100\text{kHz}$ $V_{CM} = \pm 1V, F = 5\text{MHz}$ $\Delta V_S = \pm 0.5V$	60	86 60		60	86 60		dB dB dB
Output offset voltage Gain 1 ¹ Gain 2 and 3 ^{2,3} Output common mode voltage Output voltage swing, differential Output sink current Output resistance Power supply current	$R_L = \infty$ $R_L = \infty$ $R_L = 2k$ $R_L \pm \infty$		0.6 0.35 2.9 3.0 2.5 20 18	1.5 1.5 3.4		0.6 0.35 2.9 3.0 3.6 20 18	1.5 1.0 3.4	V V V mA Ω mA

NOTES

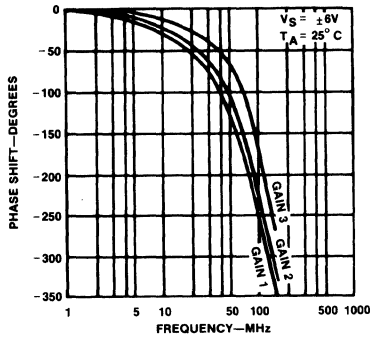
- Gain select pins G_{1A} and G_{1B} connected together.
- Gain select pins G_{2A} and G_{2B} connected together.
- All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

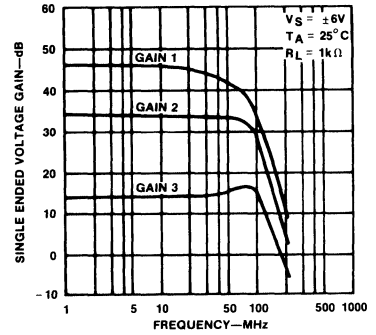
PHASE SHIFT AS A FUNCTION OF FREQUENCY



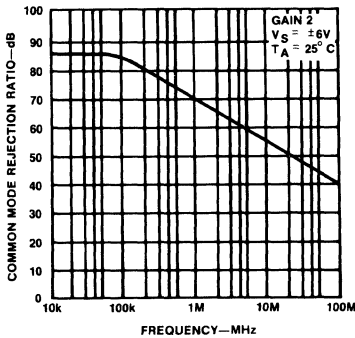
PHASE SHIFT AS A FUNCTION OF FREQUENCY



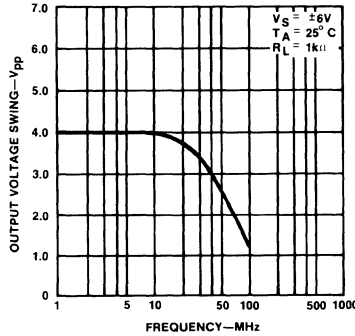
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



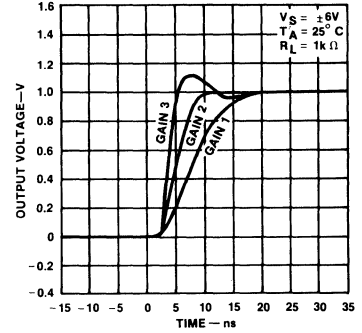
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



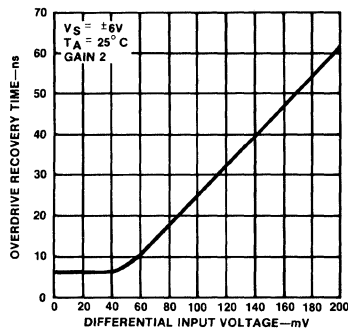
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



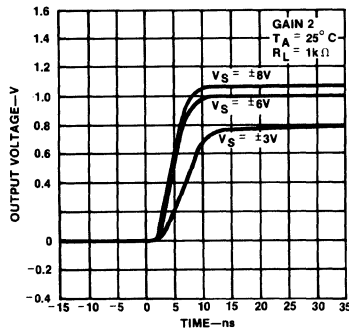
PULSE RESPONSE



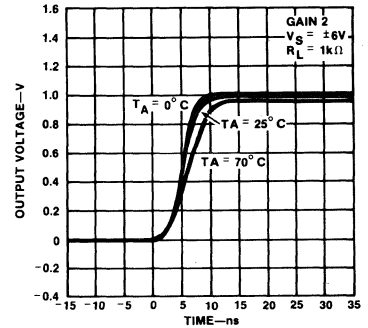
DIFFERENTIAL OVERDRIVE RECOVERY TIME



PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE

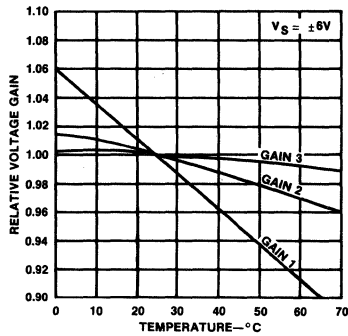


PULSE RESPONSE AS A FUNCTION OF TEMPERATURE

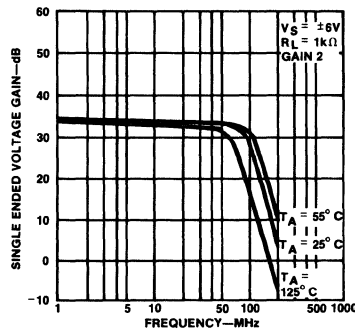


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

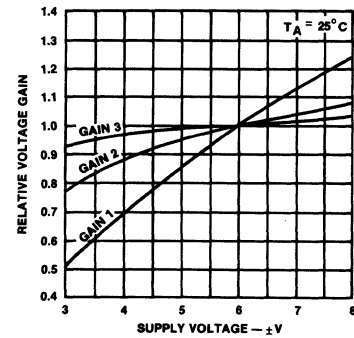
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



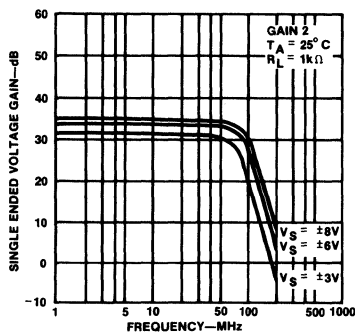
GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



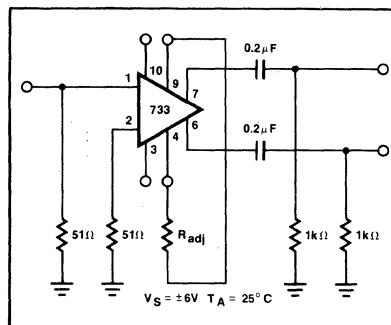
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

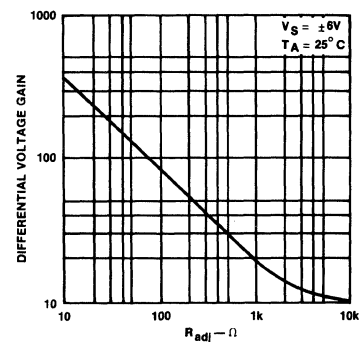


VOLTAGE GAIN ADJUST CIRCUIT

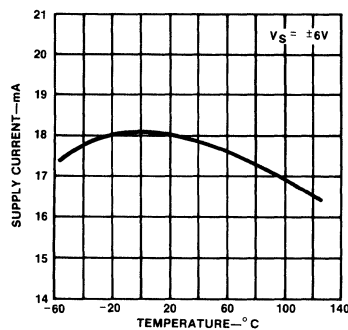


(Pin numbers apply to K Package)

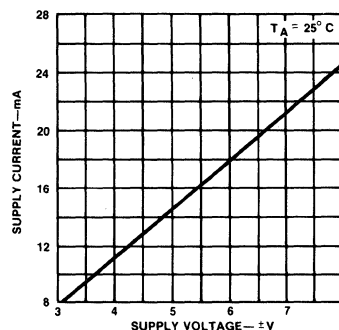
VOLTAGE GAIN AS A FUNCTION OF R_{adj} (FIGURE 3)



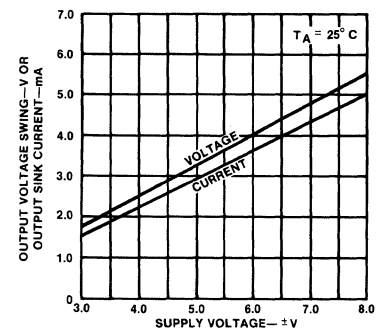
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

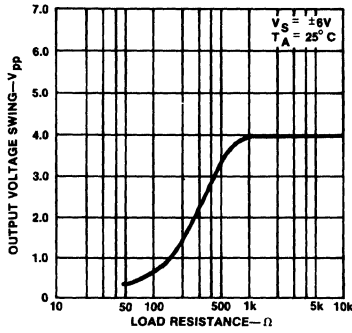


OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE

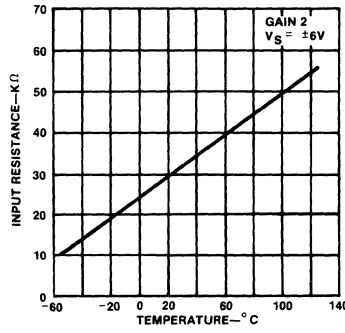


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

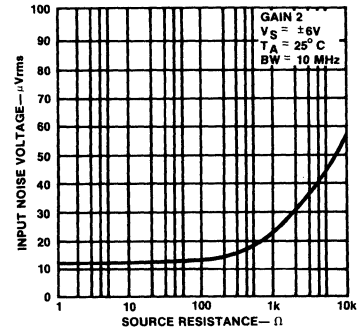
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



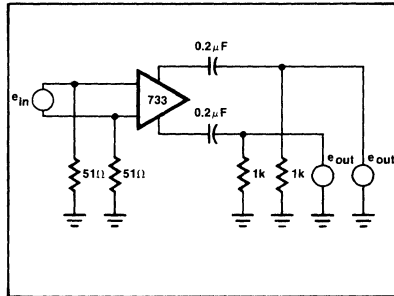
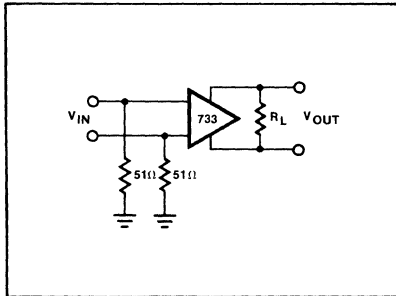
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



TEST CIRCUITS $T_A = 25^\circ\text{C}$ unless otherwise specified.



SECTION 3 POWER CONTROLLERS

Section 3—POWER CONTROLLERS

NE/SE5553/5554	Dual Polarity Regulator	153
NE/SE5560	Switched-Mode Power Supply Control Circuit	157
SG1524/2524/3524	Regulating Pulse Width Modulator	161
μA723/723C/SA723C	Precision Voltage Regulator	169

VOLTAGE REGULATOR DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 V_{ACRMS} to 125 V_{ACRMS}). Measured in mv/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mv/V.

Thermal Regulation

Referred to as changes due to ambient variations or thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mv/°C.

Transient Response

The ability of a regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds (ms).

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in Volts.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius (C).

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50 watt input and a 40 watt output, its efficiency is 80 percent).

EMI/RFI

("Electromagnetic Interference/Radio Frequency Interference") regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers).

NOTE

Refer to Section 4 of Analog Applications Manual for an in-depth explanation of Voltage Regulators

SIGNETICS REPLACEMENT STANDARDS

DUAL TRACKING VOLTAGE REGULATOR

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS	
					SURE II	SUPR II		
NATIONAL MOTOROLA RAYTHEON		Line Regulator	1	SE/NE 555X	Yes		I _{OUT} 400mA	
			%					
LM125, -6, -7	0.1 %	Line Regulator	0.25					
			%					
Raytheon 4194	±.05 to ± 40	V _{OUT}	± 5 to ± 20	SE/NE 5553/4	Yes			
			Volts					
Motorola 1568	100 mA	I _{OUT}	± 400	SE/NE 5553/4				
			mA					
		Package Power Dissipation	8	SE { NE { 5553/4	Series in SIL-9 package			
			Watts					



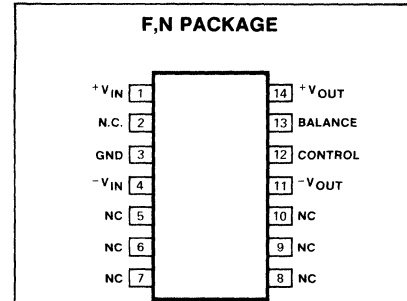
DESCRIPTION

The NE/SE5553,4 are dual polarity tracking regulators designed to produce balanced or unbalanced output voltages from 5 to 20 volts with up to 300 mA output current. Similar in specifications to the 78MX and 79MX fixed regulators, the 5553/4 series can be continuously adjusted, balanced or unbalanced. The fixed voltage on the 5553 is $\pm 12V$, and on the 5554 is $\pm 15V$. Employing current limiting and thermal shutdown protection, these dual polarity regulators are ideal for local on-card regulation.

FEATURES

- Output current to 300mA
- Internally current limited
- Thermal overload protected
- Input voltage to $\pm 32V$
- Output balance 1% typ.
- External balance control
- Continuously adjustable from 5 to 20 volts, balanced or unbalanced
- No external components required
- Short circuit current 400mA
- Maximum power capability can be achieved with proper heat sinking

PIN CONFIGURATIONS



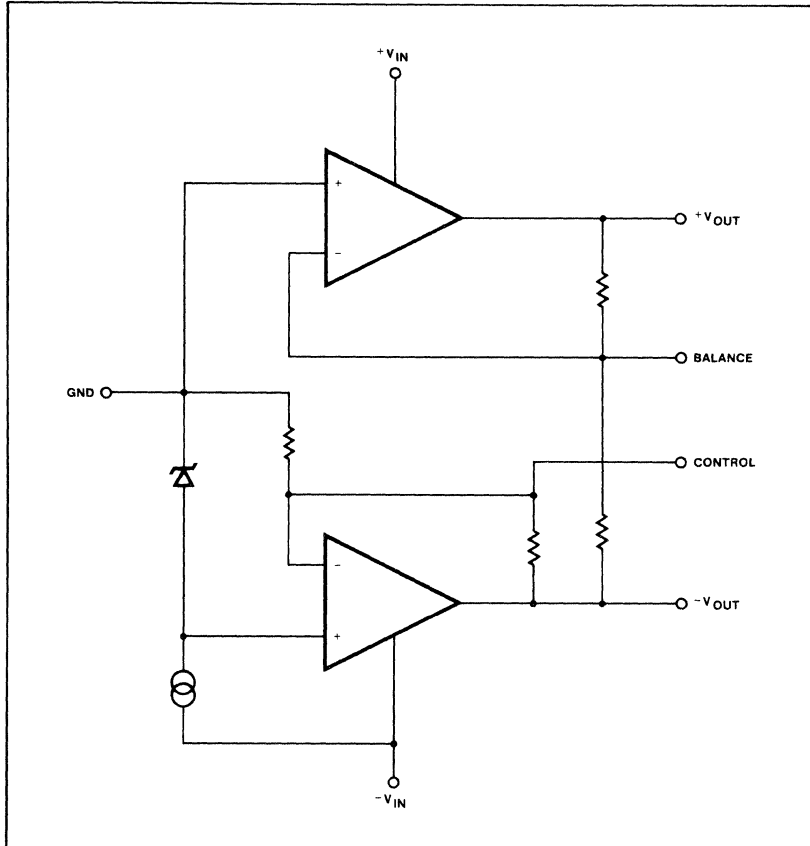
ORDER PART NO.

VOLTAGE	PART NO.
$\pm 12V$	NE/SE5553F,N
$\pm 15V$	NE/SE5554F,N

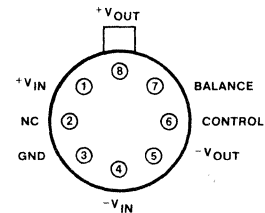
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{IN} Input voltage	± 32	V
T_{SG} Storage temperature	-65 to +150	$^{\circ}C$
T_J Operating junction temperature	0 to +125	$^{\circ}C$
	NE5553/5554	$^{\circ}C$
SE5553/5554	-55 to +150	$^{\circ}C$
Lead temperature 10 sec.	300	$^{\circ}C$

BLOCK DIAGRAM



H PACKAGE*

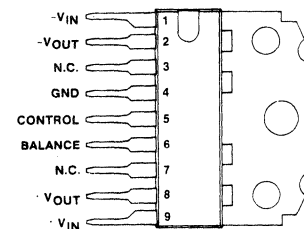


ORDER PART NO.

VOLTAGE	PART NO.
$\pm 12V$	NE/SE5553H
$\pm 15V$	NE/SE5554H

*Metal cans (H) not recommended for new designs

U PACKAGE



ORDER PART NO.

VOLTAGE	PART NO.
$\pm 12V$	NE/SE5553U
$\pm 15V$	NE/SE5554U

THERMAL RESISTANCE

H Package: $\theta_{JC} = 20^{\circ}C/W$ $\theta_{JA} = 150^{\circ}C/W$
 N Package: $\theta_{JC} = 33^{\circ}C/W$ $\theta_{JA} = 95^{\circ}C/W$
 U Package: $\theta_{JC} = 30^{\circ}C/W$ $\theta_{JA} = 62^{\circ}C/W$
 F Package: $\theta_{JC} = 30^{\circ}C/W$ $\theta_{JA} = 110^{\circ}C/W$

DC ELECTRICAL CHARACTERISTICS $V_{IN} = \pm 20V$, $I_L = 100mA$, $T_J = 25^\circ C$,
 $C_{IN} = C_{OUT} = 0.1\mu F$ unless otherwise specified.²

PARAMETER	TEST CONDITIONS	SE5553			NE5553			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT+} V_{OUT-}	Positive output voltage Negative output voltage	+11.5 -12.5	+12 -12	+12.5 -11.5	+11.5 -12.5	+12 -12	+12.5 -11.5	V
ΔV_{OUT}	Line regulation	$\pm 20 \leq V_{IN} \leq \pm 30V$		100	150	100	300	mV
ΔV_{OUT}	Load regulation	$1mA \leq I_{Load} \leq 50mA$ $1mA \leq I_{Load} \leq 200mA$		10 30	25 100	10 30	50 200	mV mV
V_{OUT+} V_{OUT-}	Positive output voltage Negative output voltage	$1mA \leq I_L \leq 100mA$ $\pm 20V \leq V_{IN} \leq \pm 30V$ over temp. ¹		+11.4 -12.6	+12 -12	+12.6 -11.4	+12 -12	V V
I_{Q+} I_{Q-}	Positive quiescent current Negative quiescent current	$I_{Load} = 0$ $I_{Load} = 0$		1.70 5.60	3.5 8.5	1.70 5.60	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	100Hz to 10kHz		2.5 .2 55		2.5 .2 55		V V μV_{rms}
I_{Peak}	Peak output current Temperature stability of output voltage			400 1		400 1		mA mV/ $^\circ C$

DC ELECTRICAL CHARACTERISTICS $V_{IN} = \pm 20V$, $I_L = 100mA$, $T_J = 25^\circ C$,
 $C_{IN} = C_{OUT} = 0.1\mu F$ unless otherwise specified.²

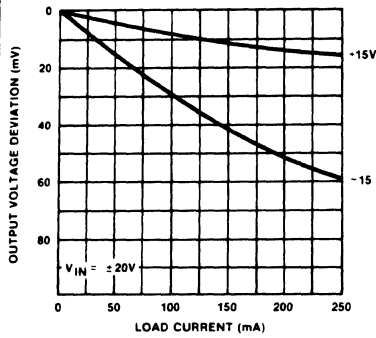
PARAMETER	TEST CONDITIONS	SE5554			NE5554			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OUT+} V_{OUT-}	Positive output voltage Negative output voltage	+14.4 -15.6	+15 -15	+15.6 -14.4	+14.4 -15.6	+15 -15	+15.6 -14.4	V
ΔV_{OUT}	Line regulation	$\pm 20 \leq V_{IN} \leq \pm 30V$		100	150	100	300	mV
ΔV_{OUT}	Load regulation	$1mA \leq I_{Load} \leq 50mA$ $1mA \leq I_{Load} \leq 200mA$		10 30	25 100	10 30	50 200	mV mV
V_{OUT+} V_{OUT-}	Positive output voltage Negative output voltage	$1mA \leq I_L \leq 100mA$ $\pm 20V \leq V_{IN} \leq \pm 30V$ over temp. ¹		+14.25 -15.75	+15 -15	+15.75 -14.25	+15 -15	V V
I_{Q+} I_{Q-}	Positive quiescent current Negative quiescent current	$I_{Load} = 0$ $I_{Load} = 0$		1.70 5.60	3.5 8.5	1.70 5.60	3.5 8.5	mA mA
V_{BAL}	Input/output differential voltage Output voltage balance Output noise voltage	100Hz to 10kHz		2.5 .2 55		2.5 .2 55		V V μV_{rms}
I_{Peak}	Peak output current Temperature stability of output voltage			400 1		400 1		mA mV/ $^\circ C$

NOTES

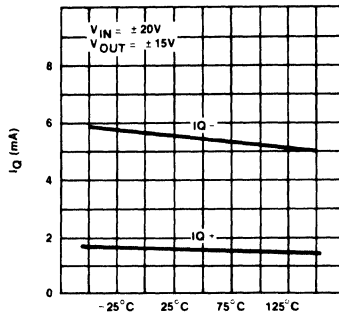
- Junction temperature range
 SE prefix $-55^\circ C < T_J < 150^\circ C$
 NE prefix $0^\circ C < T_J < 125^\circ C$
- C_{IN} needed only when remote from filter capacitors
 C_{OUT} needed only if dynamic regulation is to be improved.

TYPICAL PERFORMANCE CHARACTERISTICS

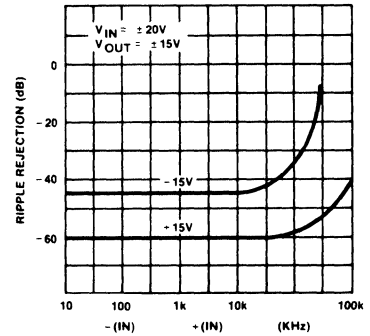
LOAD REGULATION



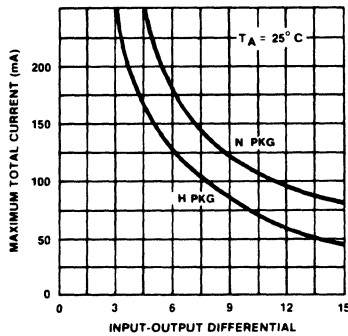
I_Q +, I_Q -



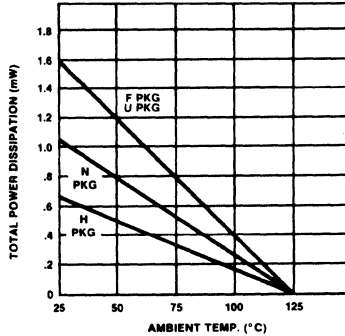
RIPPLE REJECTION



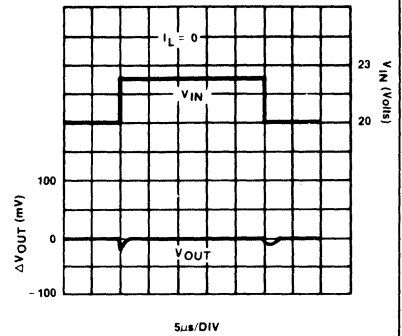
MAXIMUM CURRENT CAPABILITY



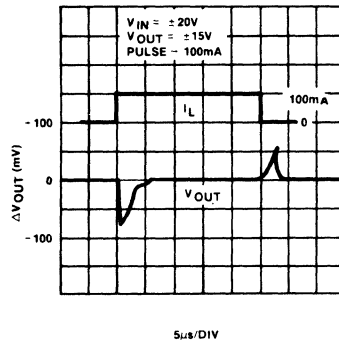
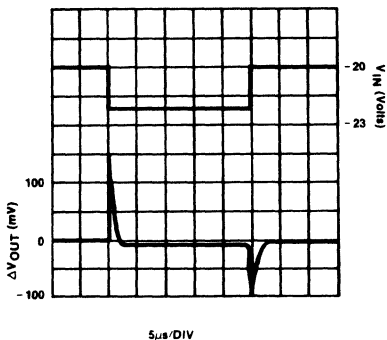
MAXIMUM FREE AIR POWER DISSIPATION



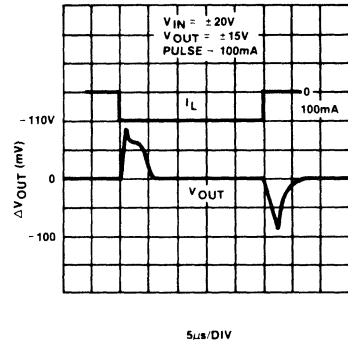
LINE TRANSIENT RESPONSE, POSITIVE



LINE TRANSIENT RESPONSE, NEGATIVE LOAD TRANSIENT RESPONSE, POSITIVE

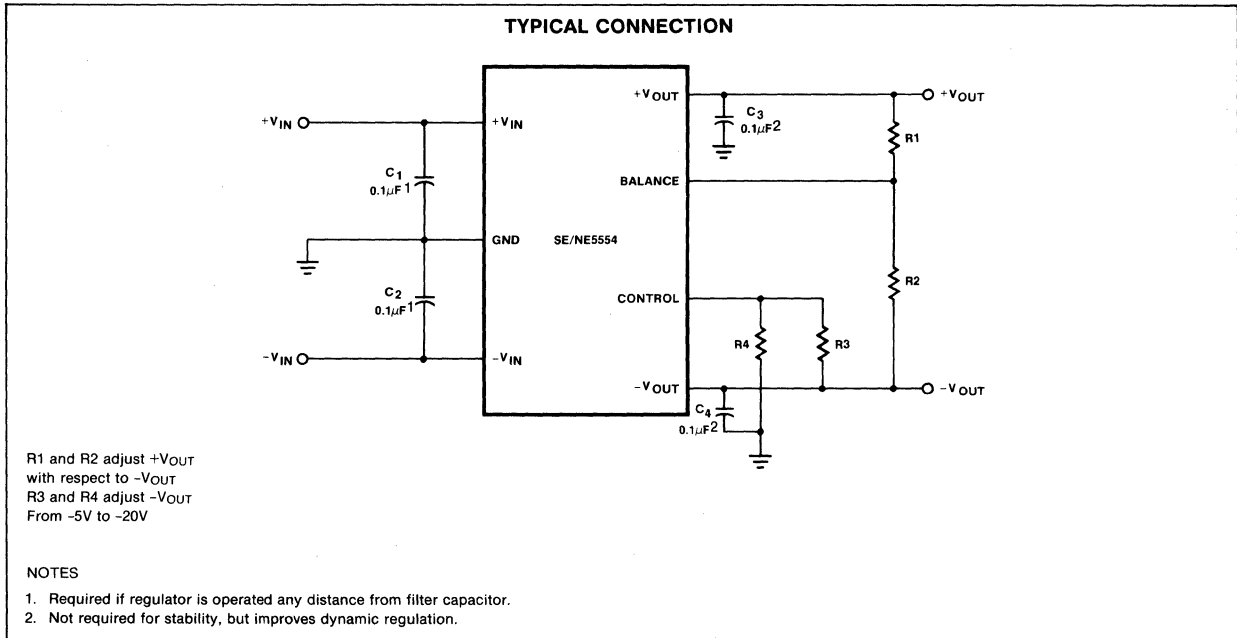


LOAD TRANSIENT RESPONSE, NEGATIVE

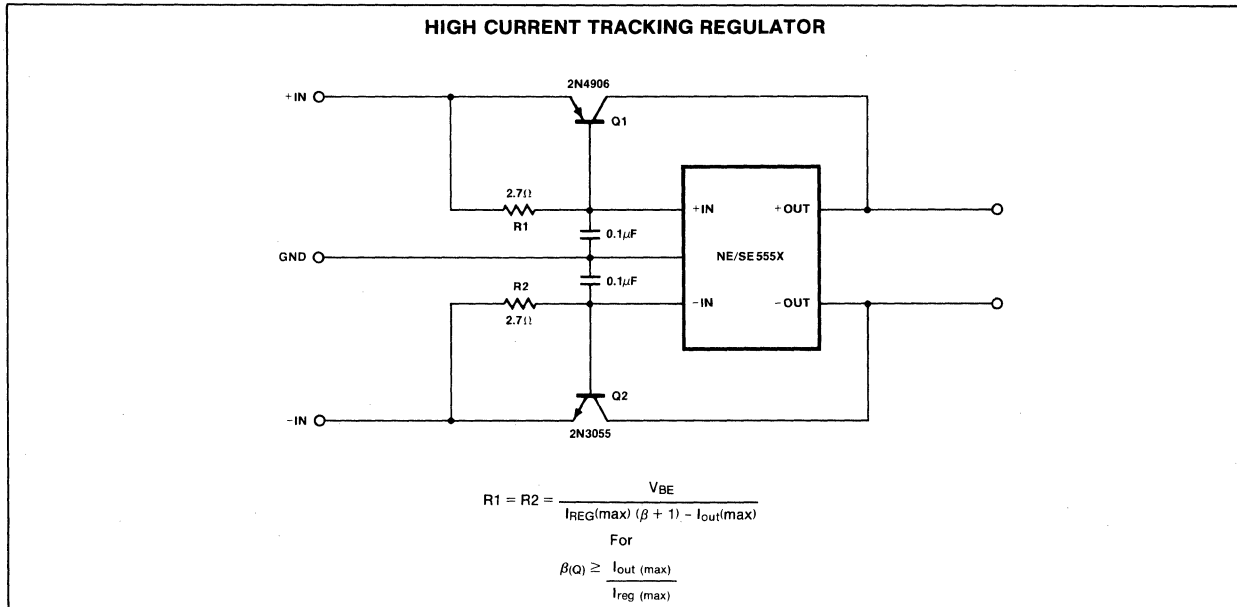


4. Device capability in free air.

BLOCK DIAGRAM



TYPICAL APPLICATIONS



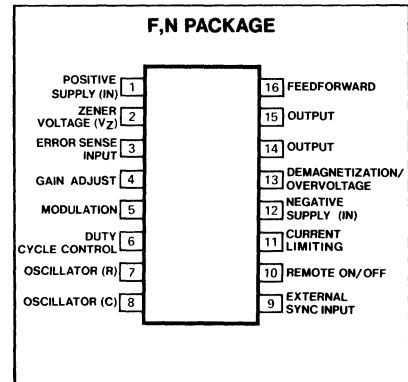
DESCRIPTION

The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- Stabilized power supply
- Temperature compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle adjustment
- Feed forward control
- External synchronization

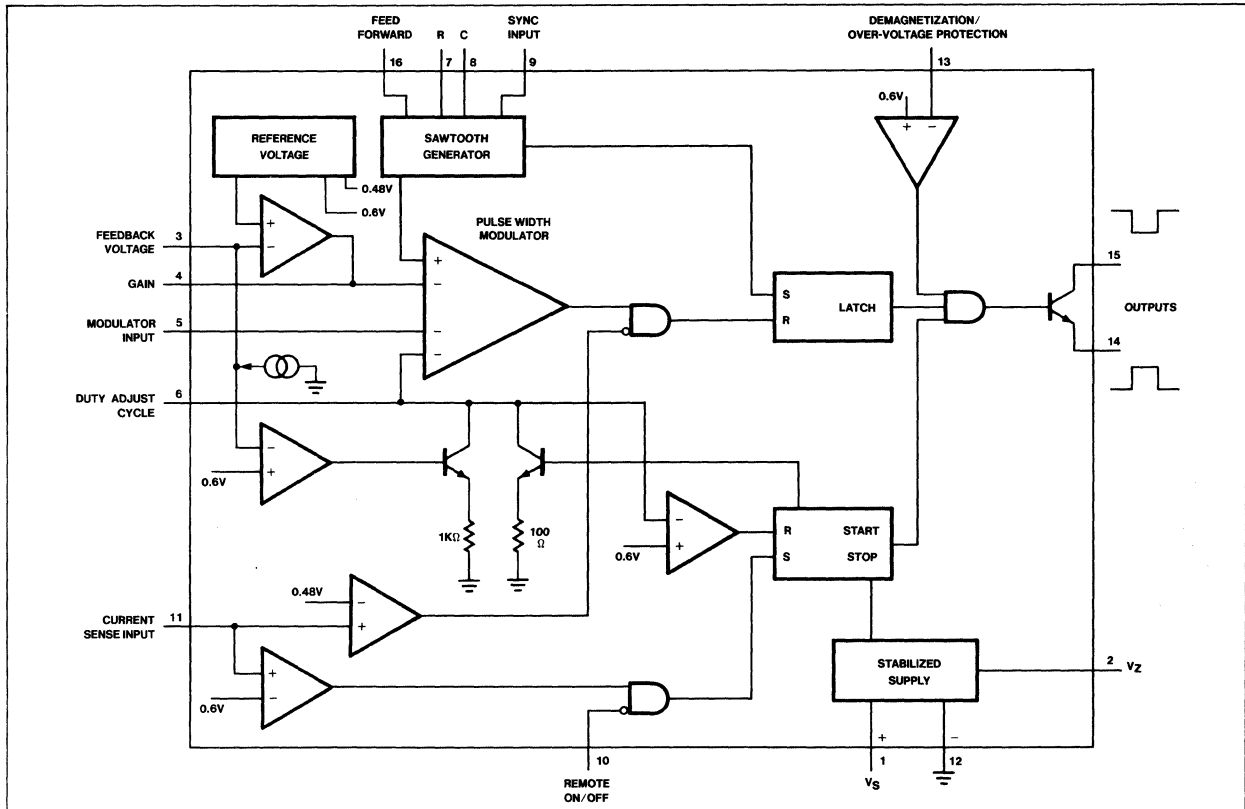
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage (Voltage sourced)	+18	V
Supply current (Current sourced)	30	mA
Output current	40	mA
Operating temperature range (ambient)		
SE5560	-55 to +125	°C
NE5560	0 to +70	°C
Storage temperature range	-65 to +150	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTIONS Internal reference voltage (V_{ref}) Internal Zener reference (V_Z) Temperature coefficient of V_{ref} Temperature coefficient of V_Z	25°C $I_L = 7\text{mA}$	3.69 7.8	3.76 8.4 ± 150	3.84 9.0 ± 100	3.57 7.8	3.76 8.4 ± 100 ± 150	3.96 9.0	V V ppm/ $^\circ\text{C}$ ppm/ $^\circ\text{C}$
OSCILLATOR SECTION Frequency range Initial accuracy Duty cycle range ¹	$R = 5\text{K}$ $f_o = 20\text{kHz}$	50 0	5	100K 98	50 0	5 98	100K 98	Hz % %
MODULATOR Modulator input current	Voltage at Pin 5 = 1V		0.2	20		0.2	20	μA
HOUSEKEEPING FUNCTION Pin 6 Duty cycle limit control Pin 6 Input current Pin 1 Low supply voltage protection thresholds Pin 3 Feedback loop protection trip on threshold Pin 3 Pull up current Pin 13 Demagnetization/over voltage protection trip on threshold Pin 13 Input current Pin 16 Feed forward duty cycle ² control Feed forward input current	(For 50% Maximum duty cycle) 15kHz to 50kHz 25°C Voltage at Pin 16 = 2V _Z 25°C	38 8.5 400 470	40 .2 9.1 500 -15 600 0.6 0.4 0.2	42 20 10.5 720 -35 720 10 5	37 8.5 400 470	40 0.2 9.1 500 -15 600 0.6 0.4 0.2	43 20 10.5 720 -35 720 10 5	% of V_Z μA V mV μA mV μA original duty cycle μA
EXTERNAL SYNCHRONIZATION Pin 9 off on Sink current	Voltage at Pin 9 = 0V 25°C	0 2		0.8 V_Z -100	0 2		0.8 V_Z -125	V V μA
REMOTE Pin 10 off on Sink current	25°C	0 2		0.8 V_Z -100	0 2		0.8 V_Z -125	V V μA
CURRENT LIMITING Pin 11: I_{IN} Single pulse inhibit delay Trip Levels: Shut down/slow start Current limit	Voltage at Pin 11 = 250mV, 25°C Inhibit delay time for 20% overdrive at 40mA I_{OUT}		-2 0.7	-10 0.8		-2 0.7	-10 0.8	μA μs V V
		.500 .400	.600 .48	.700 .56	.500 .400	.600 .480	.700 .560	

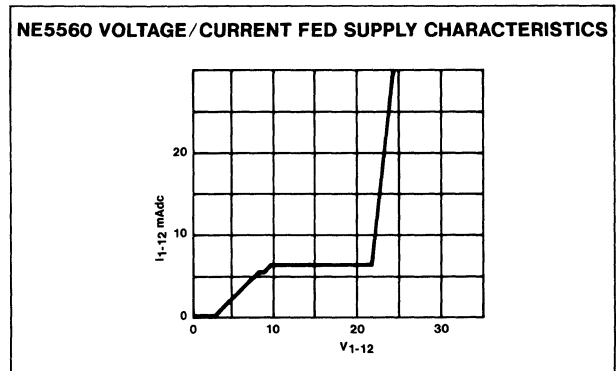
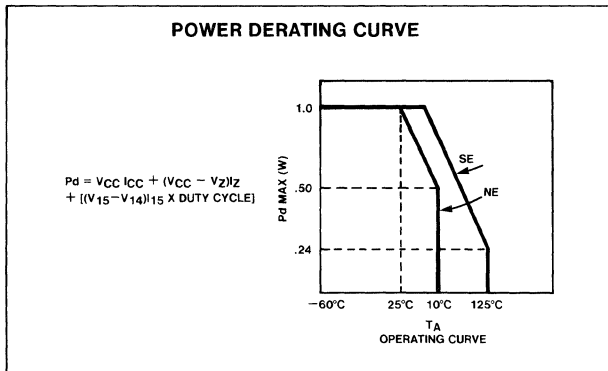
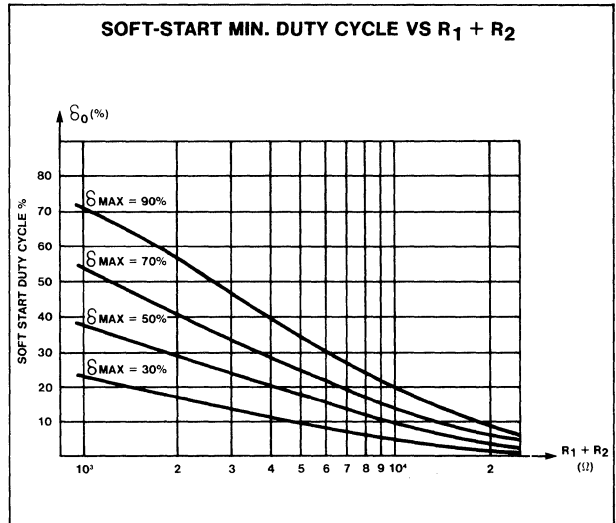
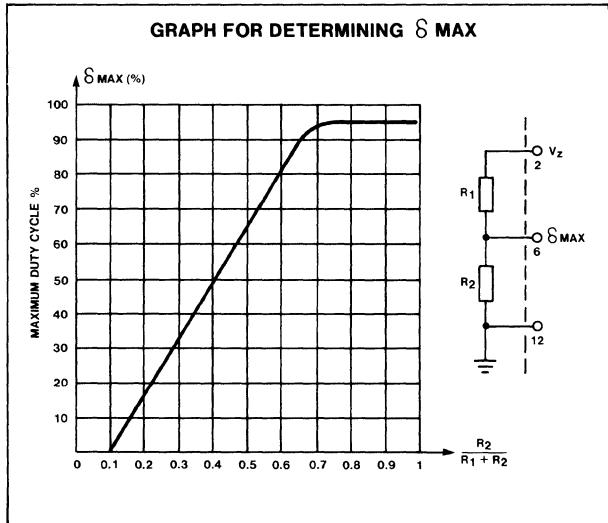
NOTES
 1. See graph
 2. See graph

DC ELECTRICAL CHARACTERISTICS (Con't) $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$ unless otherwise specified

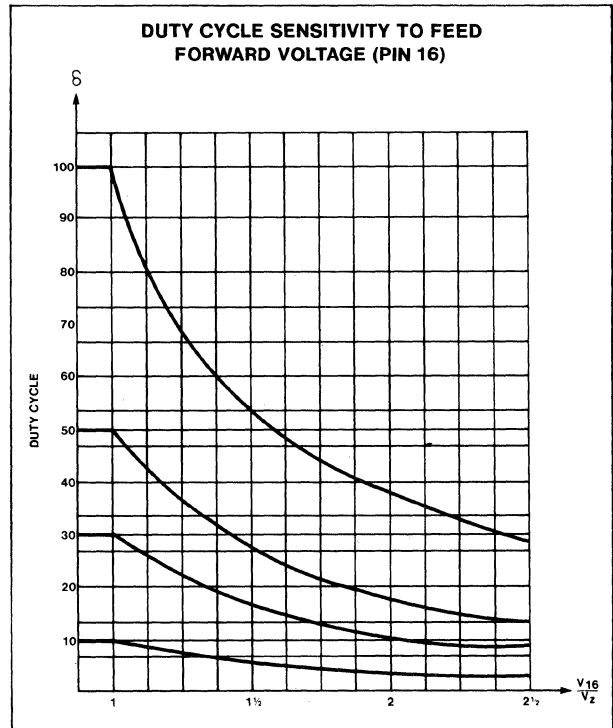
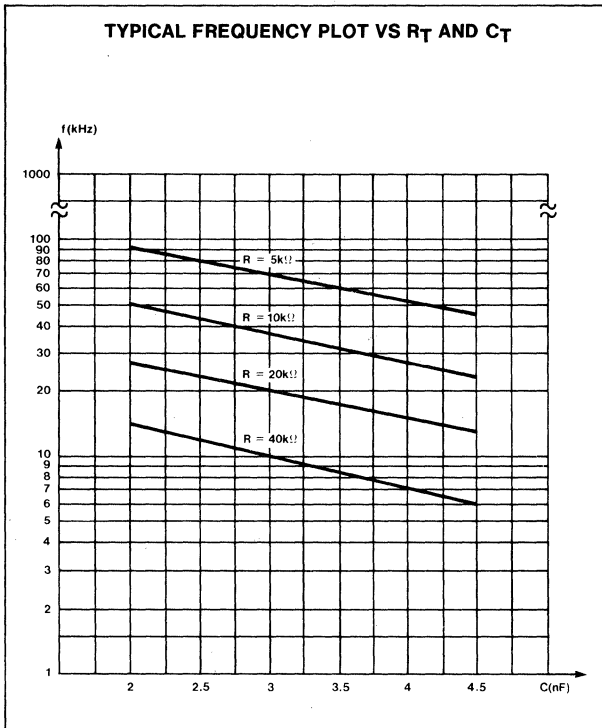
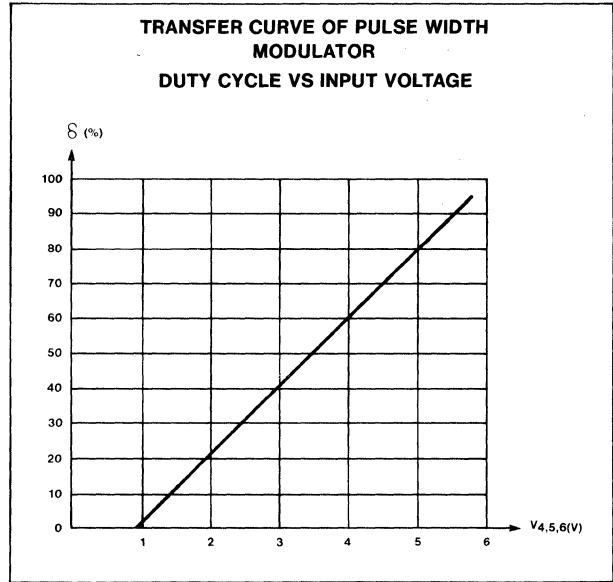
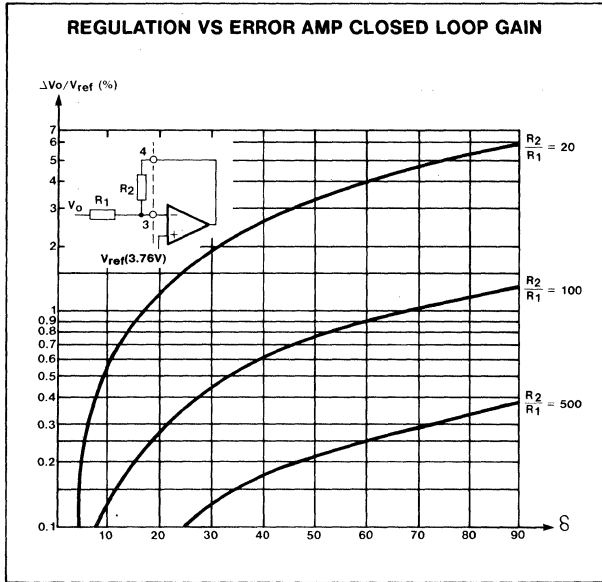
PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER Open loop gain Feedback resistor Small signal bandwidth Output voltage swing (positive) Output voltage swing (negative)			60			60		dB
		10K			10K			Ω
			3			3		MHz
			6.2			6.2		V
					0.7		0.6	V
OUTPUT STAGE Output Current (Pin 15) Max emitter voltage (Pin 14) $V_{CE(SAT)} I_C = 40\text{mA}$		40			40			mA
		5	6		5	6		V
				0.5			0.5	V
SUPPLY VOLTAGE/CURRENT I_{CC} V_{CC} V_{CC}	$I_Z=0$, Voltage fed, $V_{CC}=12\text{V}$, 25°C $I_{CC} = 10\text{ mA}$, Current fed $I_{CC} = 30\text{ mA}$, Current fed			10			10	mA
			20		23		24	V
			20		30		30	V

- NOTES
1. See graph
2. See graph

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



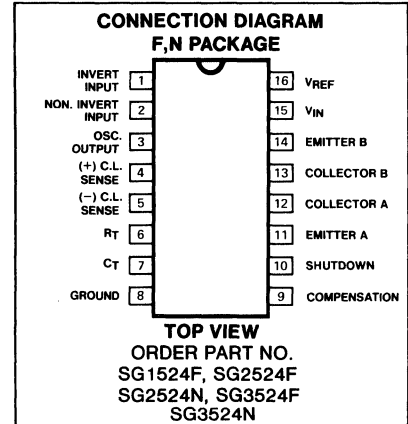
DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of -55°C to +125°C, while the SG2524 and SG3524 are designed for commercial applications of 0°C to +70°C.

FEATURES

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current is less than 10mA
- Operation beyond 100kHz

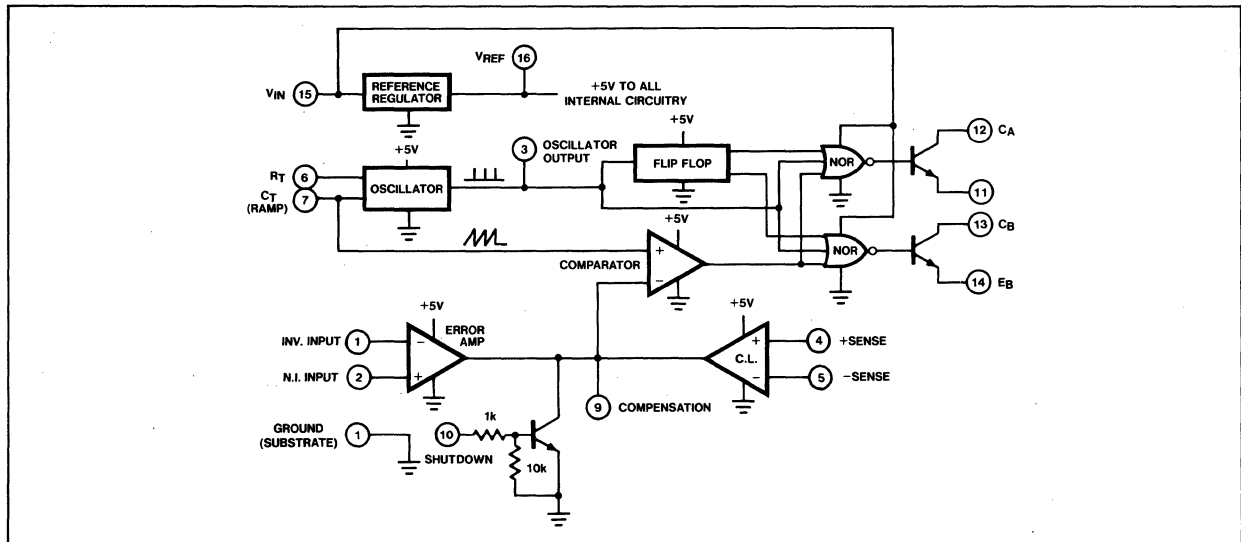
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range		
SG1524	-55 to +125	°C
SG2524/SG3524	0 to +70	°C
Storage temperature range	-65 to +150	°C

BLOCK DIAGRAM

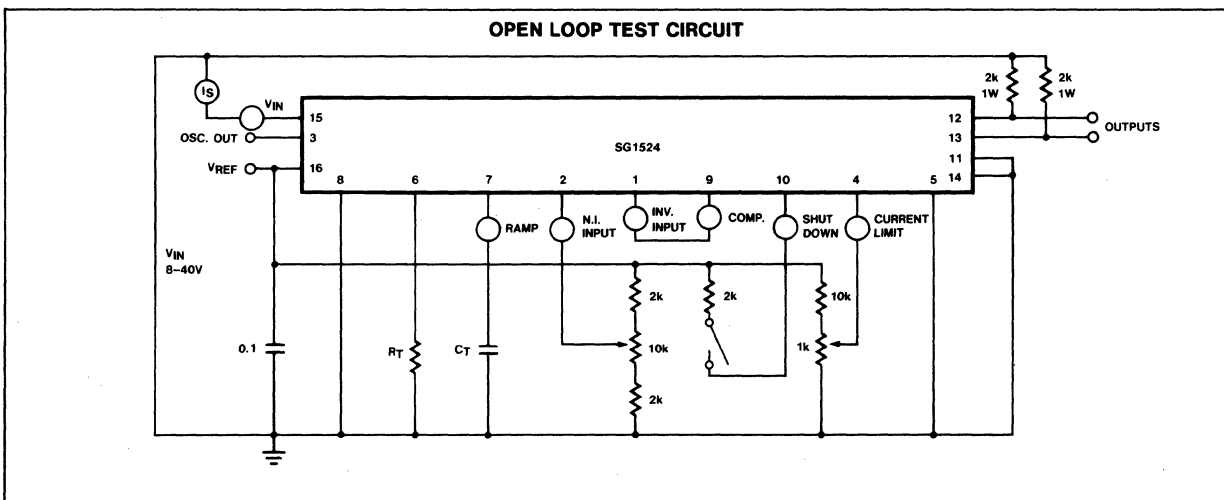


DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the SG1524 and 0°C to $+70^\circ\text{C}$ for the SG2524 and SG3524, $V_{IN} = 20\text{V}$, and $f = 20\text{kHz}$)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8$ to 40V		10	20		10	30	mV
Load regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Ripple rejection	$f = 120\text{Hz}$, $T_A = 25^\circ\text{C}$		66			66		dB
Short circuit current limit	$V_{REF} = 0$, $T_A = 25^\circ\text{C}$		100			100		mA
Temperature stability	Over operating temperature range		0.3	1		0.3	1	%
Long term stability	$T_A = 25^\circ\text{C}$		20			20		mV/kHr
OSCILLATOR SECTION								
Maximum frequency	$C_T = .001$ mfd, $R_T = 2\text{k}\Omega$		300			300		kHz
Initial accuracy	R_T and C_T constant		5			5		%
Voltage stability	$V_{IN} = 8$ to 40V , $T_A = 25^\circ\text{C}$			1			1	%
Temperature stability	Over operating temperature range						2	%
Output amplitude	Pin 3, $T_A = 25^\circ\text{C}$		3.5			3.5		Vp
Output pulse width	$C_T = .01$ mfd, $T_A = 25^\circ\text{C}$		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	$V_{CM} = 2.5\text{V}$		0.5	5		2	10	mV
Input bias current	$V_{CM} = 2.5\text{V}$		2	10		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	$T_A = 25^\circ\text{C}$	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	$T_A = 25^\circ\text{C}$		70			70		dB
Small signal bandwidth	$A_V = 0\text{dB}$, $T_A = 25^\circ\text{C}$		3			3		MHz
Output voltage	$T_A = 25^\circ\text{C}$	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty cycle	% each output "ON"	0		45	0		45	%
Input threshold	Zero duty cycle		1			1		V
Input threshold	Maximum duty cycle		3.5			3.5		V
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25^\circ\text{C}$	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV/ $^\circ\text{C}$
Common mode voltage		-1		+1	-1		+1	V
OUTPUT SECTION (each output)								
Collector-emitter voltage (breakdown)		40			40			V
Collector-leakage current	$V_{CE} = 40\text{V}$		0.1	50		0.1	50	μA
Saturation voltage	$I_C = 50\text{mA}$		1	2		1	2	V
Emitter output voltage	$V_{IN} = 20\text{V}$	17	18		17	18		V

DC ELECTRICAL CHARACTERISTICS (Cont'd) (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the SG1524 and 0°C to $+70^\circ\text{C}$ for the SG2524 and SG3524, $V_{IN} = 20\text{V}$, and $f = 20\text{kHz}$)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
Rise time	$R_C = 2\text{K ohm}$, $T_A = 25^\circ\text{C}$		0.2			0.2		μs
Fall time	$R_C = 2\text{K ohm}$, $T_A = 25^\circ\text{C}$		0.1			0.1		μs
TOTAL STANDBY CURRENT (excluding oscillator charging current, error and current limit dividers, and with outputs open)	$V_{IN} = 40\text{V}$		8	10		8	10	mA



APPLICATIONS

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The

charging current is equal to $3.6\text{V} \div R_T$ and should be kept within the range of approximately $30\mu\text{A}$ to 2mA , i.e., $1.8\text{K} < R_T < 100\text{K}$.

The range of values for C_T also has limits as the discharge time of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance ($\approx 100\text{pF}$) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when $R_T = \text{ohms}$ and $C_T = \text{microfarads}$. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG1524 to an external clock, a pulse of $\approx +3$ volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG1524's must be synchronized together, one must be designated as master with its $R_T C_T$ set for the correct peri-

TYPICAL APPLICATION

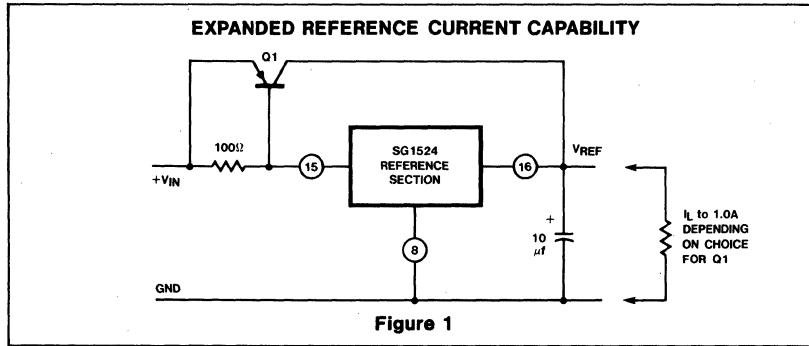


Figure 1

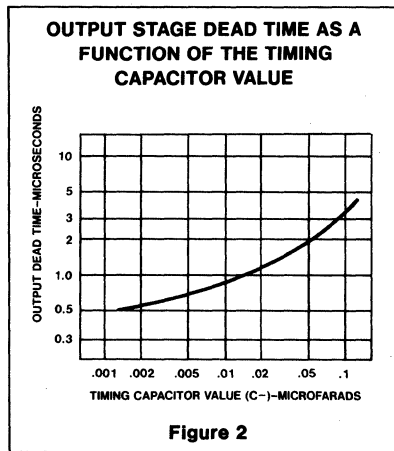


Figure 2

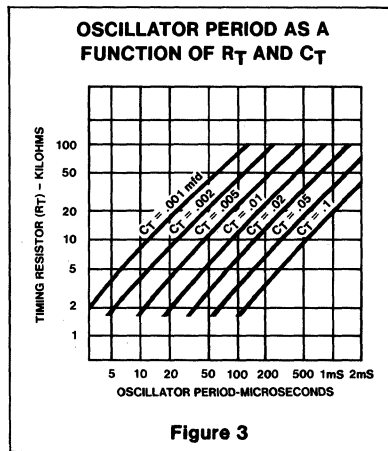


Figure 3

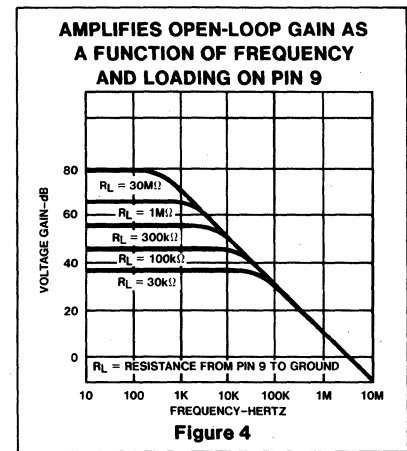


Figure 4

od. The slaves should each have an $R_T C_T$ set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L \approx 5M\Omega$). The gain is

$$A_V = gmR_L = \frac{8 I_C R_L}{2KT}$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1 ,

$$\begin{aligned} \text{Threshold} &= V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2) \\ &= I_1 R_2 \approx 200mV \end{aligned}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by $R_1 C_1$ and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer

saturation occur. (Refer to Figure 14). Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

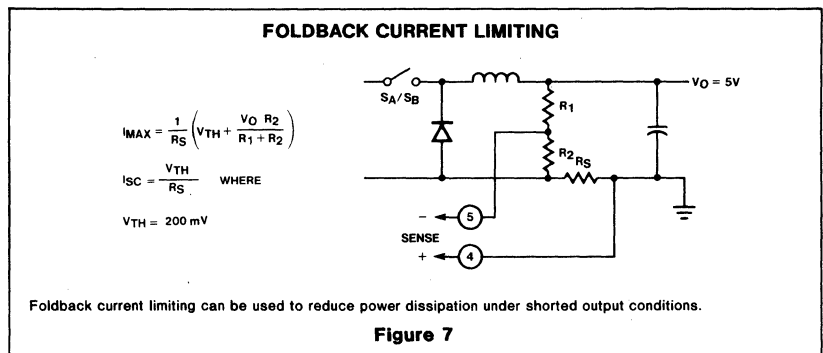
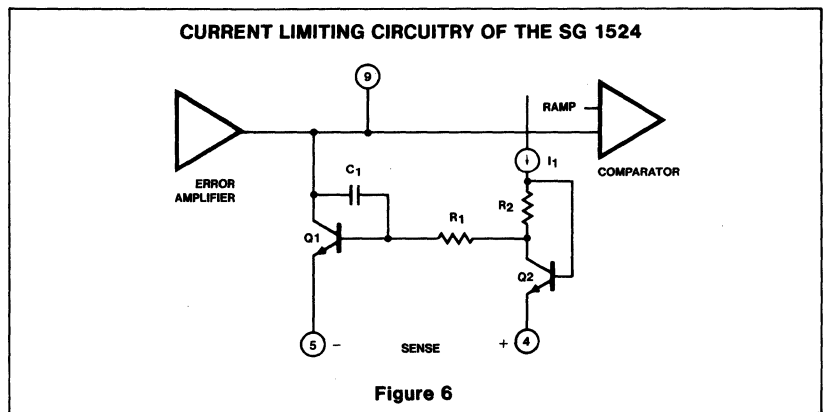
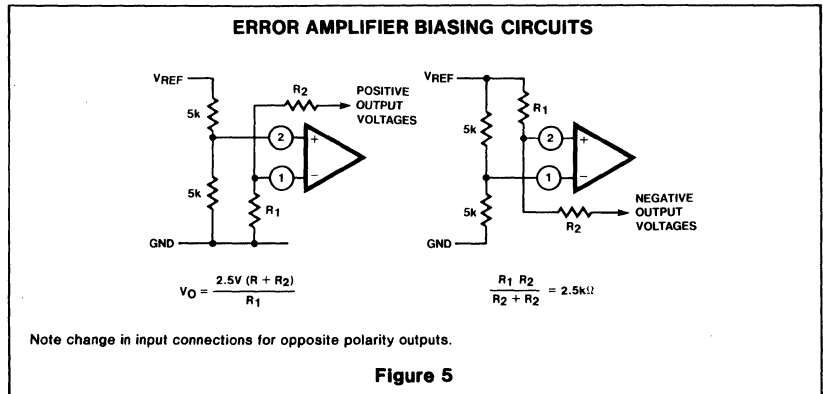
Output Circuits

The outputs of the SG1524 are two identical NPN transistors with both collectors and emitters uncommitted. This circuitry is very similar to that used in the SG111 comparator in that each output transistor has antisaturation circuitry for fast response, and current limiting set for a maximum output current of approximately 100mA. The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors.

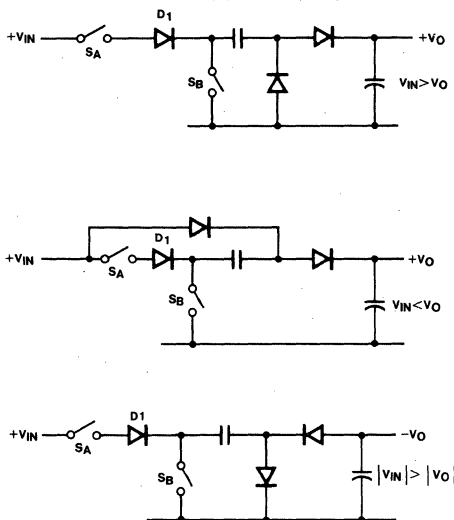
In considering the application of the SG1524 to voltage regulator circuitry, there are a multitude of output configurations possible. In general, however, they fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

Examples of each category are shown in Figures 8, 9 and 10. In each case, the switches indicated can be either the output transistors in the SG1524 or added external transistors according to the load current requirements.



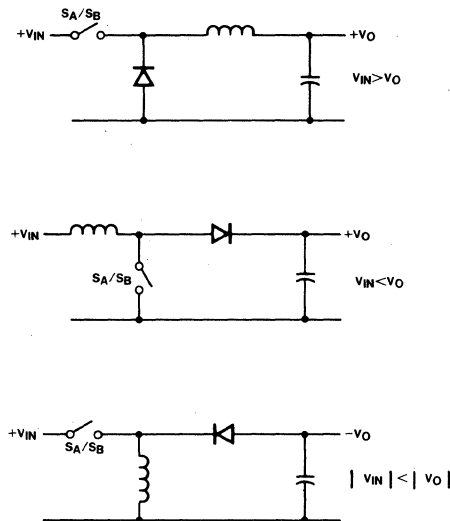
CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES



Note: Diode D1 is necessary to prevent reverse emitter-base breakdown to transistor switch SA.

Figure 8

SINGLE-ENDED INDUCTOR CIRCUITS



Single-ended inductor circuits where the two outputs of the SG1524 are connected in parallel.

Figure 9

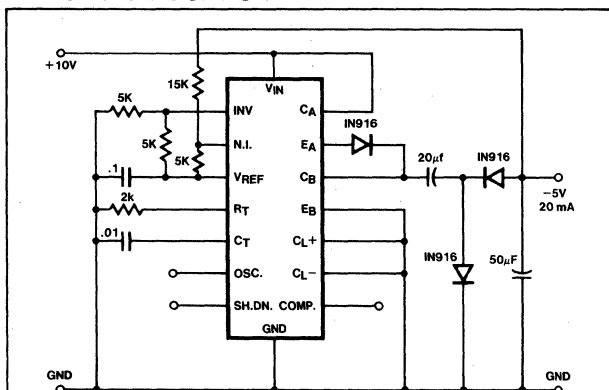
TRANSFORMER-COUPLED OUTPUTS



Transformer-coupled outputs need not relate to the input in either amplitude or polarity.

Figure 10

TYPICAL APPLICATION



The capacitor-diode output circuit is used here as a polarity converter to generate a -5 volt supply from +15 volts. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Figure 11

TYPICAL APPLICATION

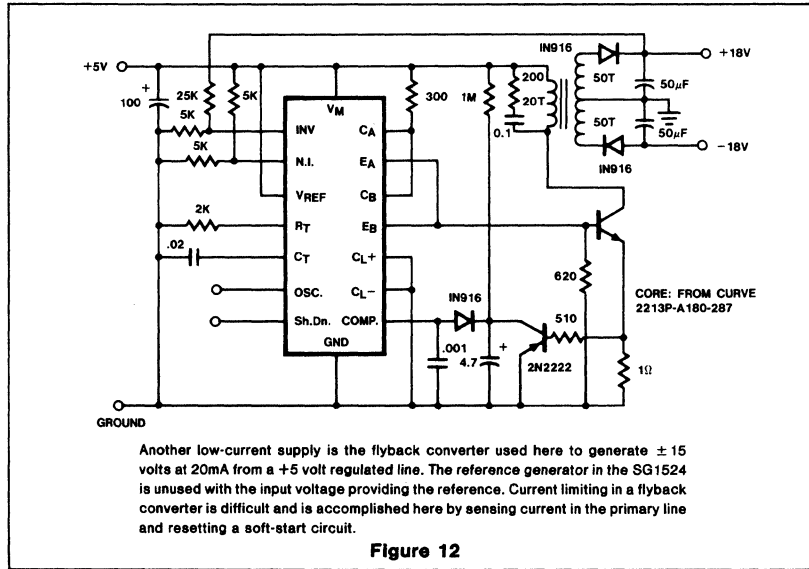


Figure 12

TYPICAL APPLICATION

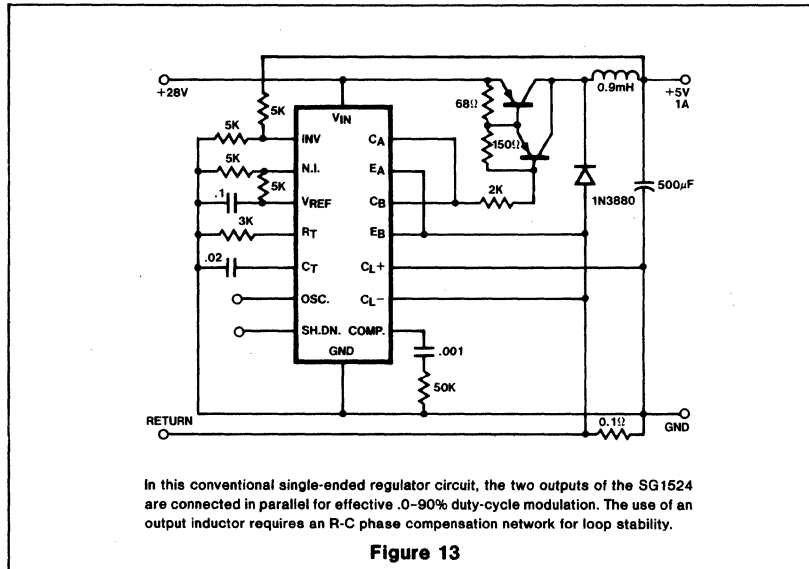
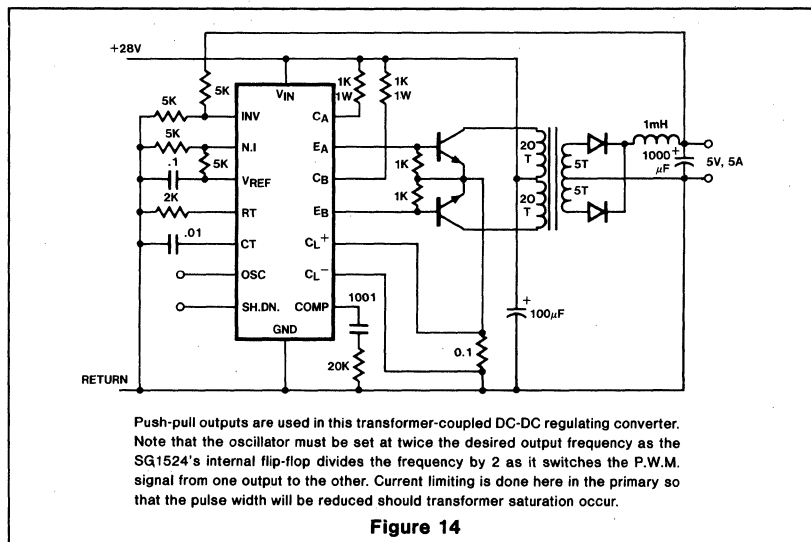


Figure 13

TYPICAL APPLICATION



μ A723/723C-F,H,N
SA723C-N
 μ A723C-D

DESCRIPTION

The μ A723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

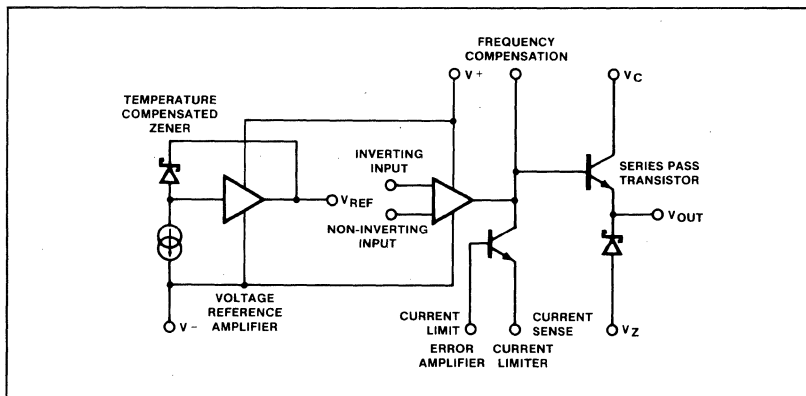
FEATURES

- Positive or negative supply operation
- Series, shunt, switching or floating operation
- .01% line and load regulation
- Output voltage adjustable from 2 to 37 volts
- Output current to 150mA without external pass transistor
- μ A723 MIL STD 88 3A, B, C available

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Pulse voltage from V+ to V- (50 ms)	50	V
Continuous voltage from V+ to V-	40	V
Input-output voltage differential	40	V
Maximum output current	150	mA
Current from VREF	15	mA
Current from Vz	25	mA
Internal power dissipation ¹	800	mW
Operating temperature range		°C
μ A723	-55 to +125	
μ A723C	0 to 70	
SA723C	-40 to +85	
Storage temperature range	-65 to +150	°C
Lead temperature	300	°C

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

D,F,N PACKAGE

ORDER PART NO.
 μ A723F,N
 μ A723CF,CN
SA723CN
 μ A723CD

H PACKAGE*

ORDER PART NO.
 μ A723H
 μ A723CH

*Metal cans (H) not recommended for new designs



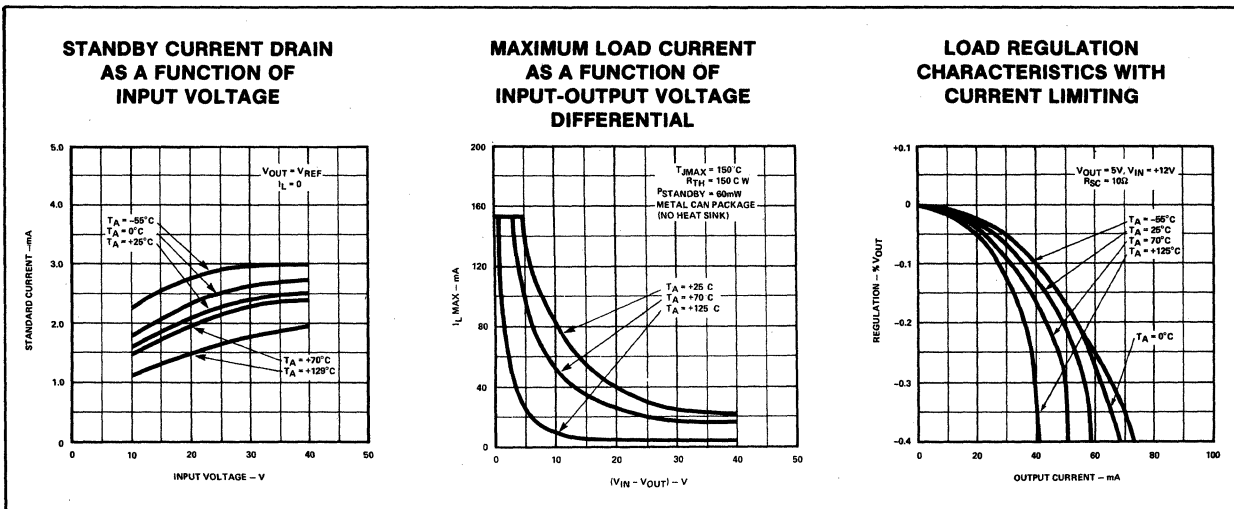
DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.¹

PARAMETER	TEST CONDITIONS	μA723			μA723C/SA723C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation ²	$V_{IN} = 12\text{V to } V_{IN} = 15\text{V}$ $V_{IN} = 12\text{V to } V_{IN} = 40\text{V}$		0.01 0.02	0.1 0.2		0.01 0.1	0.1 0.5	% V_{OUT} % V_{OUT}
Load regulation ²	$I_L = 1\text{mA to } I_L = 50\text{mA}$ $f = 50\text{Hz to } 10\text{kHz, } C_{REF} = 0$ $f = 50\text{Hz to } 10\text{kHz, } C_{REF} = 5\mu\text{F}$		0.03 74 86	0.15		0.03 74 86	0.2	% V_{OUT} dB dB
Short circuit current limit	$R_{SC} = 10\Omega, V_{OUT} = 0$		65			65		mA
Reference voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output noise voltage	$BW = 100\text{Hz to } 10\text{kHz, } C_{REF} = 0$ $BW = 100\text{Hz to } 10\text{kHz, } C_{REF} = 5\mu\text{F}$		20 2.5			20 2.5		μVrms μVrms
Long term stability			0.1			0.1	0.1	%/1000hrs.
Standby current drain	$I_L = 0, V_{IN} = 30\text{V}$		2.3	3.5		2.3	4.0	mA
Input voltage range		9.5		40	9.5		40	V
Output voltage range		2.0		37	2.0		37	V
Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges								
Line regulation				0.3			0.3	% V_{OUT}
Load regulation				0.6			0.6	% V_{OUT}
Average temperature coefficient of output voltage	$V_{IN} = 12\text{V to } V_{IN} = 15\text{V}$ $I_L = 1\text{mA to } I_L = 50\text{mA}$		0.002	0.015		0.003	0.015	%/ $^\circ\text{C}$

NOTES

- $V_{IN} = V^+ = V_C = 12\text{V}, V^- = 0\text{V}, V_{OUT} = 5\text{V}, I_L = 1\text{mA}, R_{SC} = 0, C_1 = 100\mu\text{F}, C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10\text{k}\Omega$ when connected as shown in Figure 3.
- The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

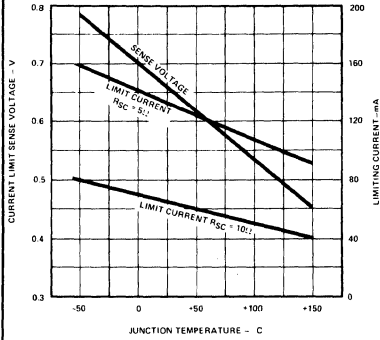
TYPICAL PERFORMANCE CHARACTERISTICS



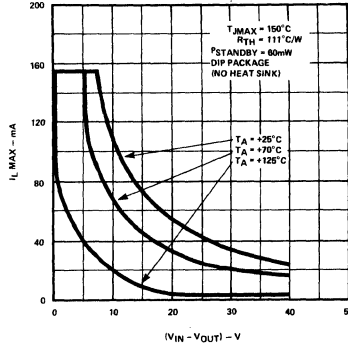
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



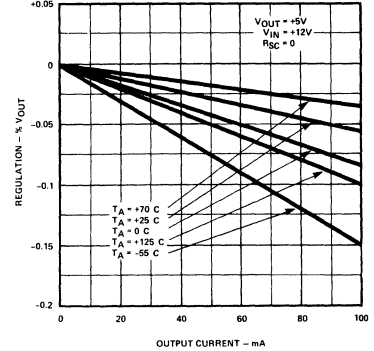
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



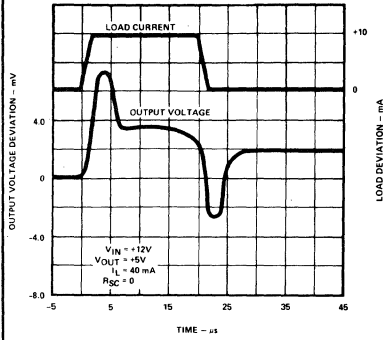
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



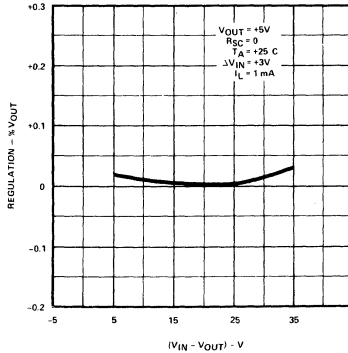
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



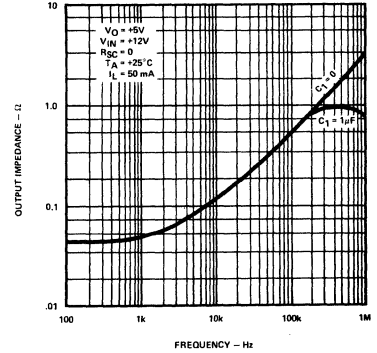
LOAD TRANSIENT RESPONSE



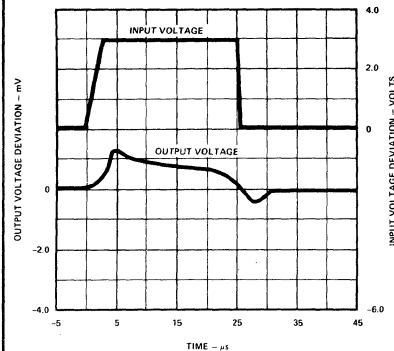
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



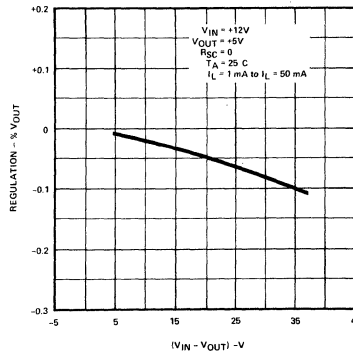
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



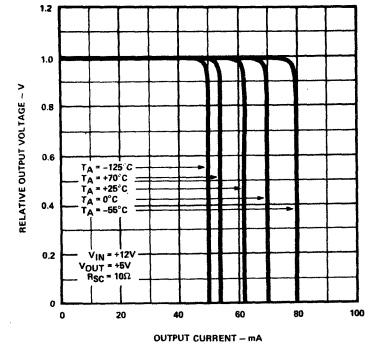
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

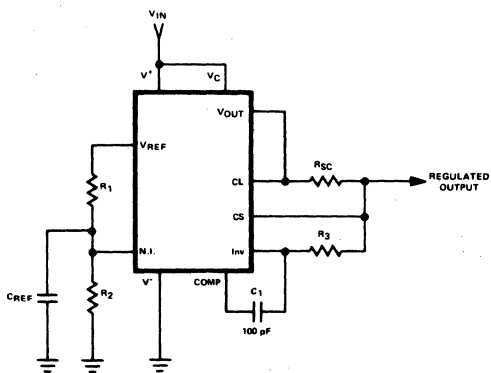


CURRENT LIMITING CHARACTERISTICS



TYPICAL APPLICATIONS

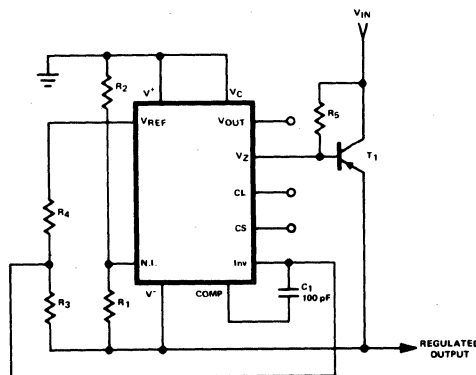
LOW VOLTAGE REGULATOR
(V_{OUT} = 2 TO 7 VOLTS)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

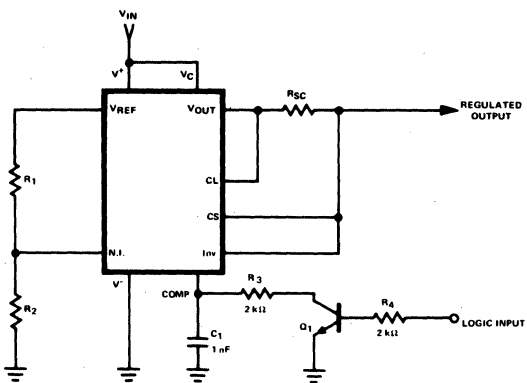
$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

NEGATIVE VOLTAGE REGULATOR



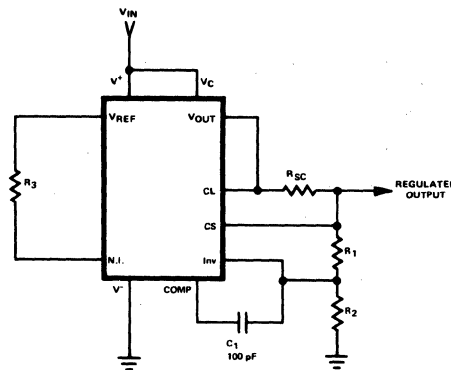
$$V_{out} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1} \right]; R_3 = R_4$$

REMOTE SHUTDOWN REGULATOR
WITH CURRENT LIMITING
(V_{OUT} = 2 TO 7 VOLTS)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

HIGH VOLTAGE REGULATOR
(V_{OUT} = 7 TO 37 VOLTS)



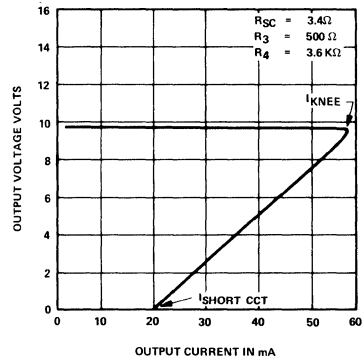
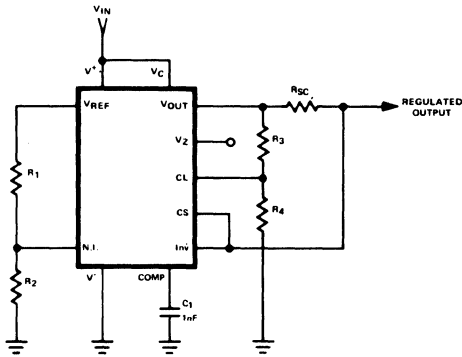
$$V_{out} = \left[V_{REF} \times \frac{R_1 + 2}{R_2} \right]$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

R₃ may be eliminated for minimum component count

TYPICAL APPLICATIONS (Cont'd)

FOLDBACK CURRENT LIMITING REGULATOR
(V_{OUT} = 2 TO 7 VOLTS)



$$I_{KNEE} = \left[\frac{V_{out} R_3}{R_{sc} R_4} + \frac{V_{SENSE} (R_3 + R_4)}{R_{sc} R_4} \right]$$

$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2} \right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4} \right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT} I_{SC}}{V_{SENSE} (I_{KNEE} - I_{SHORTCKT})} - 1$$

$$R_{sc} = \frac{V_{SENSE}}{I_{sc}} \left[1 + \frac{R_3}{R_4} \right]$$



SECTION 4 TIMERS

Section 4—TIMERS

NE/SE555/SE555C	Timer	177
NE/SA/SE556	Dual Timer	180
NE/SA/SE556-1/SE556-1C	Dual Timer	183
NE/SA/SE558	Quad Timer	186

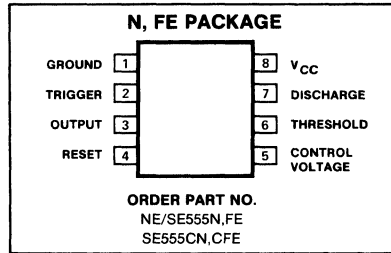
DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

- Turn off time less than 2μs
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle

PIN CONFIGURATIONS



- TTL compatible
- Temperature stability of 0.005% per °C

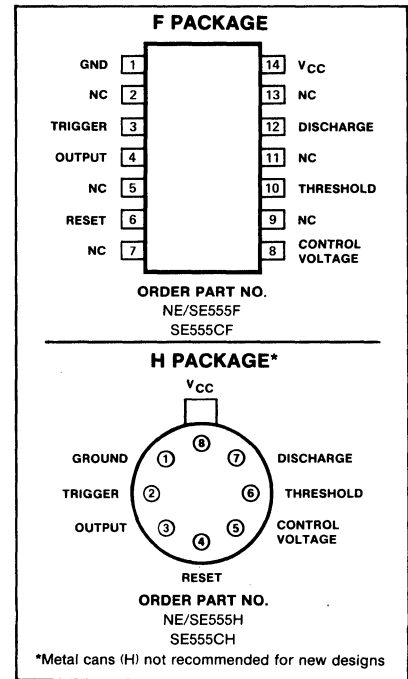
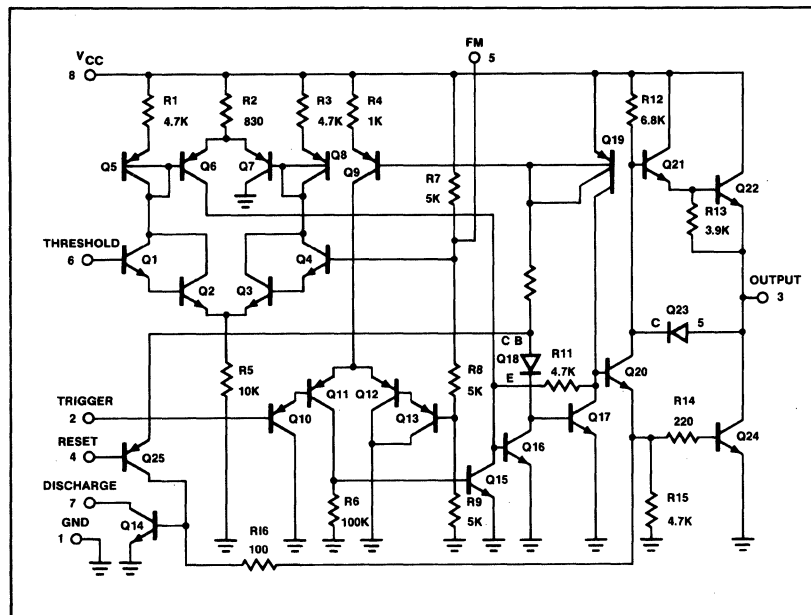
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

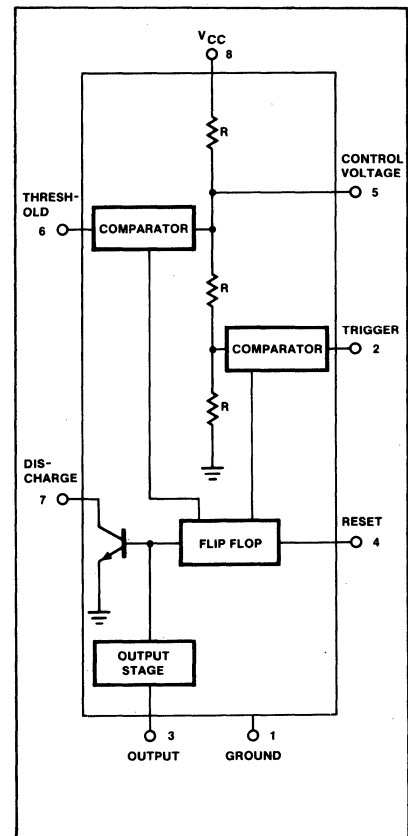
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	°C
SE555, SE555C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

EQUIVALENT SCHEMATIC



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15$ unless otherwise specified.

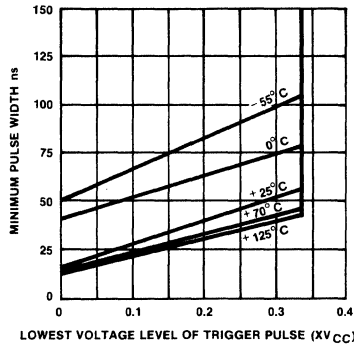
PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V } R_L = \infty$ $V_{CC} = 15\text{V } R_L = \infty$		3 10	5 12		3 10	6 15	 mA mA
Timing error (monostable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A = 2\text{K}\Omega$ to $100\text{K}\Omega$ $C = 0.1\mu\text{F}$		0.5 30 0.05	2.0 100 0.2		1.0 50 0.1	3.0 3.0 0.5	 % ppm/ $^\circ\text{C}$ %/V
Timing error (astable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$		1.5 90 0.15			2.25 150 0.3		 % ppm/ $^\circ\text{C}$ %/V
Control voltage level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	 V V
Threshold voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	 V V
Threshold current ³			0.1	0.25		0.1	0.25	μA
Trigger voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	 V V
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
Reset voltage ⁴		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	$V_{RESET} = 0\text{V}$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 2.0 2.5	0.15 0.5 2.2 2.5		0.1 0.4 2.0 2.5	0.25 0.75 2.5 2.5	 V V V V V V V
Output voltage (high)	$V_{CC} = 15\text{V}$ $I_{SOURCE} = 200\text{mA}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SOURCE} = 100\text{mA}$	13.0 3.0	12.5 13.3 3.3		12.75 2.75	12.5 13.3 3.3		 V V V
Turn off time ⁵	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

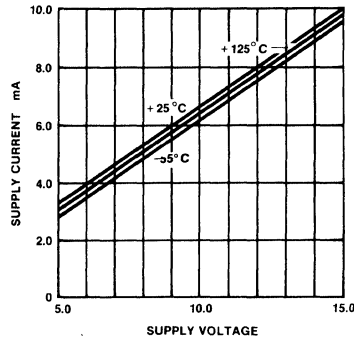
- Supply current when output high typically 1mA less.
- Tested at $V_{CC} = 5\text{V}$ and $V_{CC} = 15\text{V}$.
- This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total $R = 10$ megohm, and for 5V operation, the max total $R = 3.4$ megohm.
- Specified with trigger input high.
- Time measured from a positive going input pulse from 0 to $0.8 \times V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

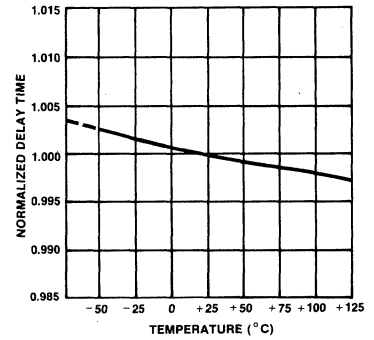
MINIMUM PULSE WIDTH
REQUIRED FOR TRIGGERING



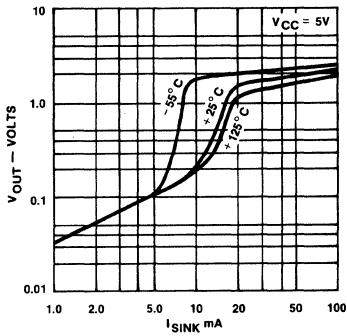
SUPPLY CURRENT
vs SUPPLY VOLTAGE



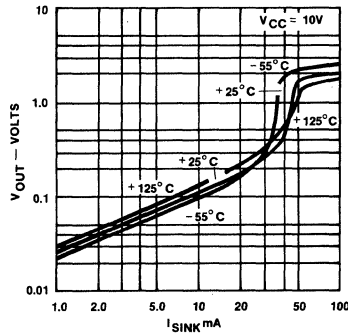
DELAY TIME
vs TEMPERATURE



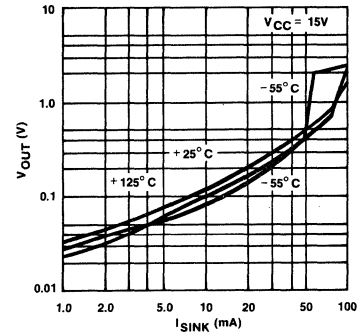
LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT



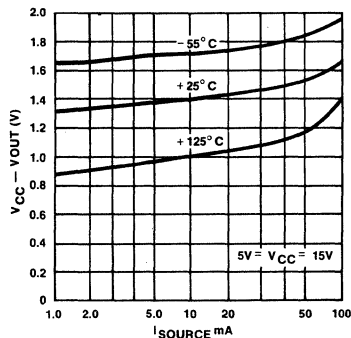
LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT



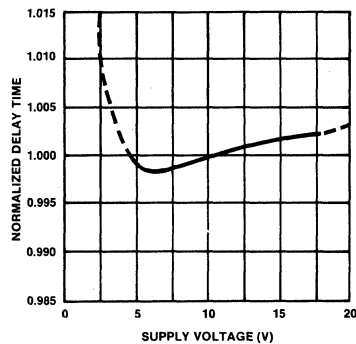
LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT



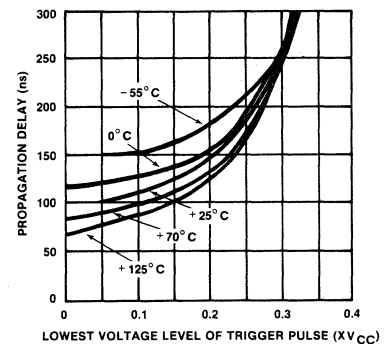
HIGH OUTPUT VOLTAGE DROP
vs OUTPUT SOURCE CURRENT



DELAY TIME vs
SUPPLY VOLTAGE



PROPAGATION DELAY
vs VOLTAGE LEVEL
OF TRIGGER PULSE



DESCRIPTION

The 556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

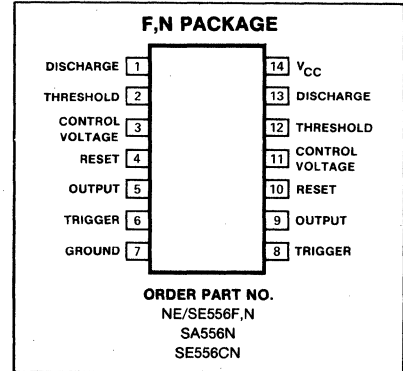
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

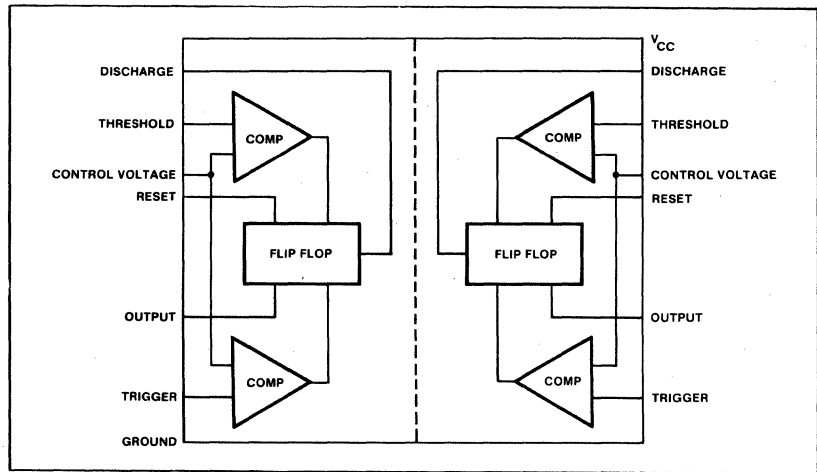
FEATURES

- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).

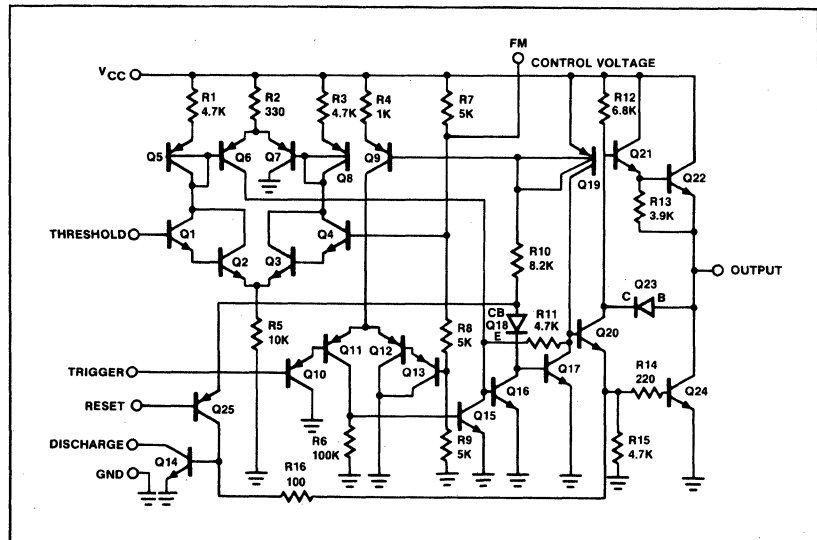
PIN CONFIGURATION



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)





ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556, SE556C	+16	V
SE556	+18	V
Power dissipation	600	mW
Operating temperature range		
NE556	0 to +70	°C
SA556	-40 to +85	°C
SE556, SE556C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature	+300	°C
(Soldering, 60 sec)		

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

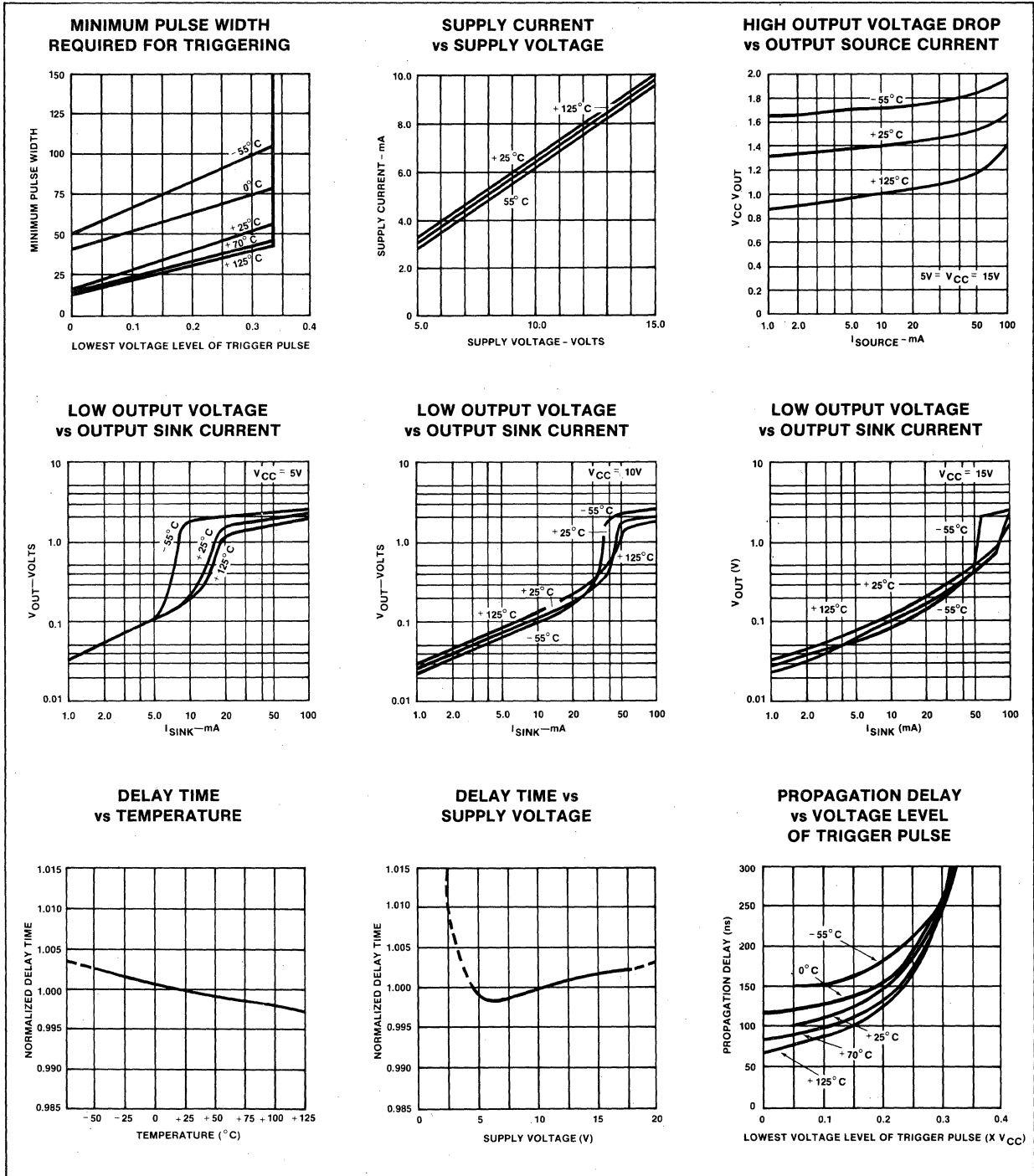
PARAMETER	TEST CONDITIONS	SE556			NE/SA556/SE556C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V}$ $R_L = \infty$ $V_{CC} = 15\text{V}$ $R_L = \infty$		6 20	10 24		6 20	12 30	mA mA
Timing error (monostable)	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$							
Initial accuracy ²			0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$							
Initial accuracy ²			1.5			2.25		%
Drift with temperature			90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
Threshold voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
Threshold current ³			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
Reset voltage ⁵		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0\text{V}$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 2.0 2.5	0.15 0.5 2.25		0.1 0.4 2.0 2.5	0.25 0.75 3.2	V V V V
Output voltage (high)	$V_{CC} = 15\text{V}$ $I_{SOURCE} = 200\text{mA}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SOURCE} = 100\text{mA}$	13.0 3.0	12.5 13.3 3.3		12.75 2.75	12.5 13.3 3.3		V V V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics ⁴								
Initial accuracy ²			0.5	1.0		1.0	2.0	%
Drift with temperature			10			10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES See following page

NOTES

- Supply current when output is high is typically 1.0mA less.
- Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
- This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total $R = 10$ meg-ohms, and for 5V operation, the max. total $R = 3.4$ meg-ohms.
- Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
- Specified with trigger input high.

TYPICAL PERFORMANCE CHARACTERISTICS



DESCRIPTION

The 556-1 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556-1 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

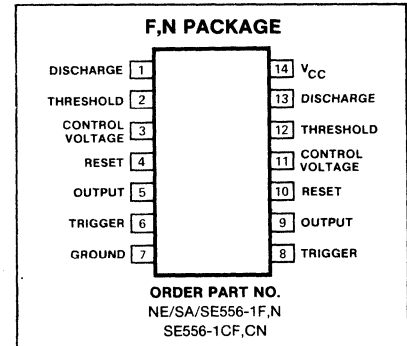
FEATURES

- Turn off time less than $2\mu S$
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

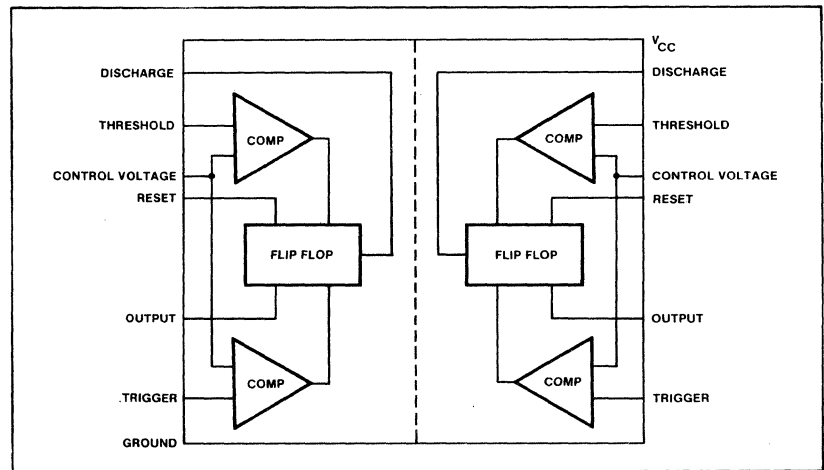
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

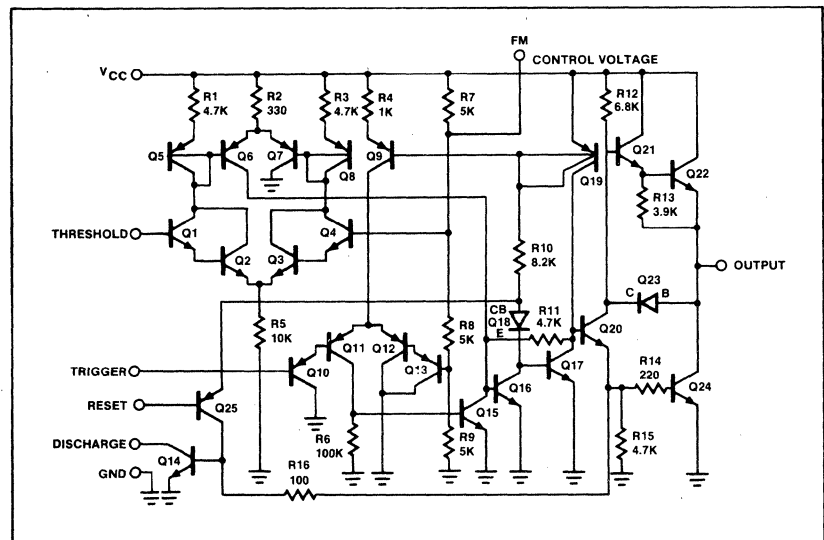
PIN CONFIGURATION



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage NE/SA556-1, SE556-1C SE556-1	+16 +18	V V
Power dissipation	1.20	W
Operating temperature range NE/SA556-1 SA556-1 SE556-1, SE556-1C	0 to +70 -40 to +85 -55 to +125	°C °C °C
Storage temperature range Lead temperature (soldering, 60 sec)	-65 to +150 +300	°C °C

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

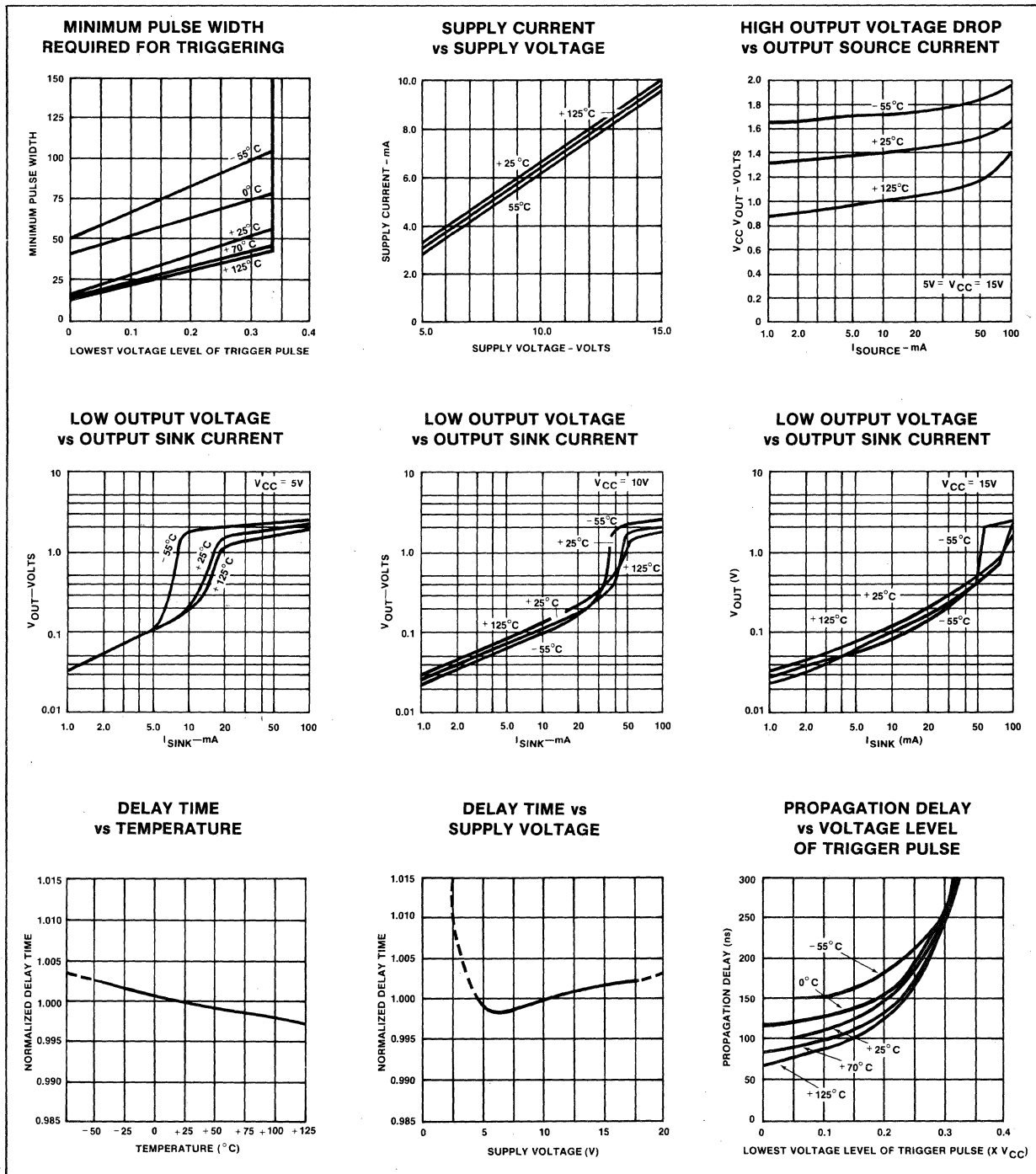
PARAMETER	TEST CONDITIONS	SE556-1			NE556-1/SE556-1C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V}$ $R_L = \infty$ $V_{CC} = 15\text{V}$ $R_L = \infty$		6 20	10 24		6 20	12 30	mA mA
Timing error (monostable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$		0.5 30 0.05	1.5 100 0.2		0.75 50 0.1	3.0 ppm/°C %/V	% ppm/°C %/V
Timing error (astable) Initial accuracy ² Drift with temperature Drift with supply voltage Control voltage level	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$		1.5 90 0.15 9.6 2.9			2.25 150 0.3 10.0 3.33	11.0 4.0	% ppm/°C %/V V V
Threshold voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0 250	8.8 2.4	10.0 3.33 30	11.2 4.2 250	V V nA
Trigger voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67 0.5	5.6 2.2 2.0	V V μA
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5		
Reset voltage ⁵ Reset current Reset current	$V_{RESET} = 0\text{V}$	0.4	0.7 0.1 0.4	1.0 0.4 1.0	0.4	0.7 0.1 0.4	1.0 0.6 1.5	V mA mA
Output voltage (low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 0.8 2.5	0.15 0.5 1.2		0.1 0.4 2.0 2.5	0.25 0.75 2.5	V V V V V V V
Output voltage (high)	$V_{CC} = 15\text{V}$ $I_{SOURCE} = 200\text{mA}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SOURCE} = 100\text{mA}$	13.0	12.5 13.3		12.75	12.5 13.3		V V V
Turn off time ⁶ Rise time of output Fall time of output	$V_{RESET} = V_{CC}$		0.5 100 100	2.0 200 200		0.5 100 100	300 300	μs ns ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics ⁴ Initial accuracy ² Drift with temperature Drift with supply voltage			0.5 ±10 0.1	1.0		1.0 ±10 0.2	2.0 0.5	% ppm/°C %/V

NOTES
See following page

NOTES

1. Supply current when output is high is typically 1.0mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total $R = 10$ megohms, and for 5V operation, the max. total $R = 3.4$ megohms.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high.
6. Time measured from a positive going input pulse from 0 to $0.8V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL CHARACTERISTICS



DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

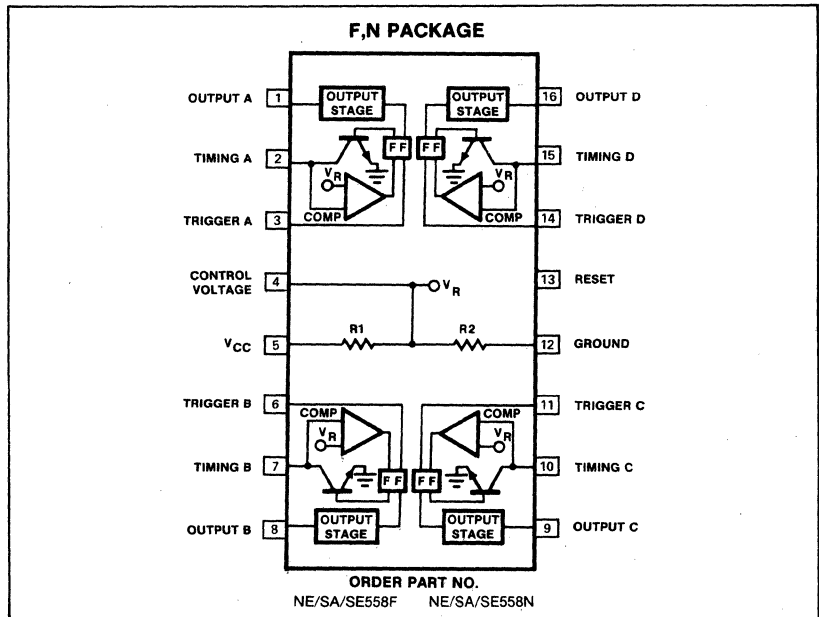
FEATURES

- 100mA output current per section
- Edge triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5V to 18V
- Timer intervals from microseconds to hours
- Time period equals RC
- Military qualifications pending

APPLICATIONS

- Sequential timing
- Time delay generation
- Precision timing
- Industrial controls
- Quad one-shot

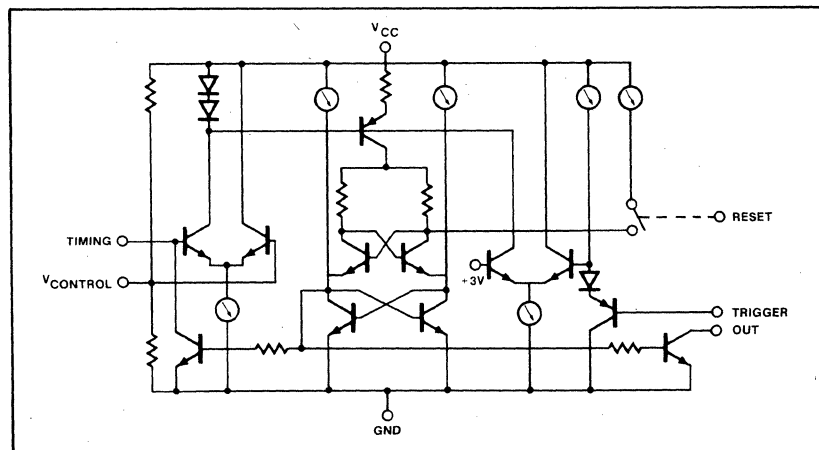
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+16	V
NE/SA558	+18	V
SE558	1.25	W
Power dissipation	0 to +70	°C
Operating temperature range	-40 to +85	°C
NE558	-55 to +125	°C
SA558	-65 to +150	°C
SE558	+300	°C
Storage temperature range		
Lead temperature (soldering, 60sec)		

558 EQUIVALENT CIRCUIT





ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current	$V_{CC} = \text{Reset} = 15\text{V}$		21	32		27	36	mA
Timing accuracy (T = RC)	$R = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 1\mu\text{F}$							
Initial accuracy			1.0	3		2		%
Drift with temperature			150			150		ppm/ $^\circ\text{C}$
Drift with supply voltage			0.1			0.1		%/V
Trigger voltage ¹	$V_{CC} = 15\text{V}$	0.8	1.5	2.4	0.8	1.5	2.4	V
Trigger current	Trigger = 0V		5	30		5	100	μA
Reset voltage ²		0.8	1.5	2.4	0.8	1.5	2.4	V
Reset current	Reset		50	300		50		μA
Threshold voltage			0.63			0.63		$\times V_{CC}$
Threshold leakage			15			15		nA
Output voltage ³	$I_L = 10\text{mA}$ $I_L = 100\text{mA}$		0.1	0.2		0.1	0.4	V
Output leakage			0.7	1.5		1.0	2.0	V
Propagation delay			10			10		nA
Risetime of output			1.0			1.0		μs
Falltime of output	$I_L = 100\text{mA}$ $I_L = 100\text{mA}$		100			100		ns
			100			100		ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.

SECTION 5 COMPARATORS

Section 5—COMPARATORS

LM111/211/311	Voltage Comparator	191
LM119/219/319	Dual Voltage Comparator	194
LM139/239/339	Quad Voltage Comparator	199
LM193/A/293/A/393/A	Low Power Dual Voltage Comparator	204
LM2901	Quad Voltage Comparator	199
LM2903	Low Power Dual Voltage Comparator	204
MC3302	Quad Voltage Comparator	199
NE/SE521	High Speed Dual Differential Comparator/Sense Amp	207
NE/SE522	High Speed Dual Differential Comparator/Sense Amp	211
NE/SE527	Voltage Comparator	215
NE/SE529	Voltage Comparator	219

COMPARATORS SELECTION GUIDE

DEVICE	COM- PLEXITY	TEMP. RANGE*	MAX. INP. OFFSET VOLT. (mV)	MAX. INP. CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE		OUTPUT STRUCTURE	VOLTAGE GAIN (TYP.) V/mV	TTL FANOUT	MAX. DIFF. INP. VOLTAGE V	PACKAGES
				Bias (μ A)	Offset (μ A)				VOL max (V)	VOH min (V)					
LM111 ¹	Single	M	4.00	0.15	0.02	± 15	200	± 14	0.4		O.C.	200	5	± 30	F,T
LM211	Single	E	4.00	0.15	0.02	to	200	± 14	0.4		O.C.	200	5	± 30	F,N,T
LM311	Single	I	10.0	0.30	0.07	+5 and GND	200	± 14	0.4		O.C.	200	5	± 30	F,N,T
NE527 ²	Single	I	10.0	4.00	1.00	± 5 to ± 15	16	± 6	0.5	2.7	TTL		5	± 5	F,K,N
SE527	Single	M	6.00	4.00	1.00	and GND	16	± 6	0.5	2.5	TTL		5	± 5	F,K
NE529 ²	Single	I	10.0	50.0	15.0	± 5 to ± 15	12	± 6	0.5	2.7	TTL		5	± 5	F,K,N
SE529	Single	M	6.00	36.0	9.00	and GND	12	± 6	0.5	2.5	TTL		5	± 5	F,K
LM119 ³	Dual	M	7.00	1.00	0.10	± 15	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM219	Dual	E	7.00	1.00	0.10	to	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM319	Dual	I	10.0	1.20	0.30	± 5 and GND	80	± 13	0.6		O.C.	40	2	± 5	F,K,N
LM193 ³	Dual	M	9.00	0.30	0.10	± 1 to ± 18	1300	0 to VS -2	0.7		O.C.	200	2	36	T
LM293	Dual	E	9.00	0.40	0.15	or	1300	0 to VS -2	0.7		O.C.	200	2	36	N,T
LM393	Dual	I	9.00	0.40	0.15	+2 to +36 GND	1300	0 to VS -2	0.7		O.C.	200	2	36	N,T
LM2903	Dual	E	15.0	0.50	0.20		1300	0 to VS -2	0.7		O.C.	100	2	36	N,T
NE521 ⁴	Dual	I	10.0	40.0	12.0	+5, -5, GND	7	± 3	0.5	2.7	TTL		12	± 6	F,N
NE522	Dual	I	10.0	40.0	12.0	+5, -5, GND	9	± 3	0.5		O.C.		12	± 6	F,N
LM139 ³	Quad	M	9.00	0.30	0.10		1300	0 to VS -2	0.7		O.C.	200	2	36	F,N
LM239	Quad	E	9.00	0.40	0.15	± 1 to ± 18 or	1300	0 to VS -2	0.7		O.C.	200	2	36	F,N
LM339	Quad	I	9.00	0.40	0.15	+2 to +36	1300	0 to VS -2	0.7		O.C.	200	2	36	F,N
LM2901	Quad	E	15.0	0.50	0.20		1300	0 to VS -2	0.7		O.C.	100	2	36	N
MC3302 ³	Quad	E	40.0	1.00	0.20	+2 to +28 GND	2000	0 to VS -2	0.4		O.C.	30	2	28	N

*Temperature Range

E = Extended

I = Industrial

M = Military

NOTES

1. With strobe; will work from single supply
2. Complementary output gates with individual strobes
3. Will operate from single or dual supplies
4. Ultra high speed

DESCRIPTION

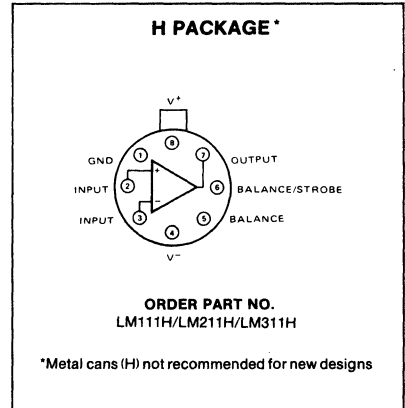
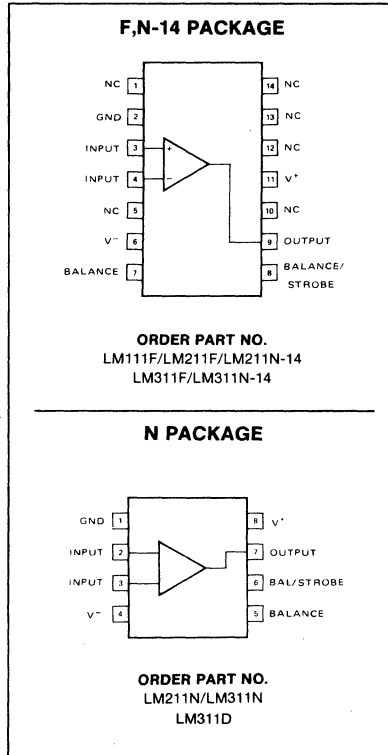
The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μ A710. They are designed to operate over a wider range of supply voltages; from standard $\pm 15V$ op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μ A710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μ A710 series.

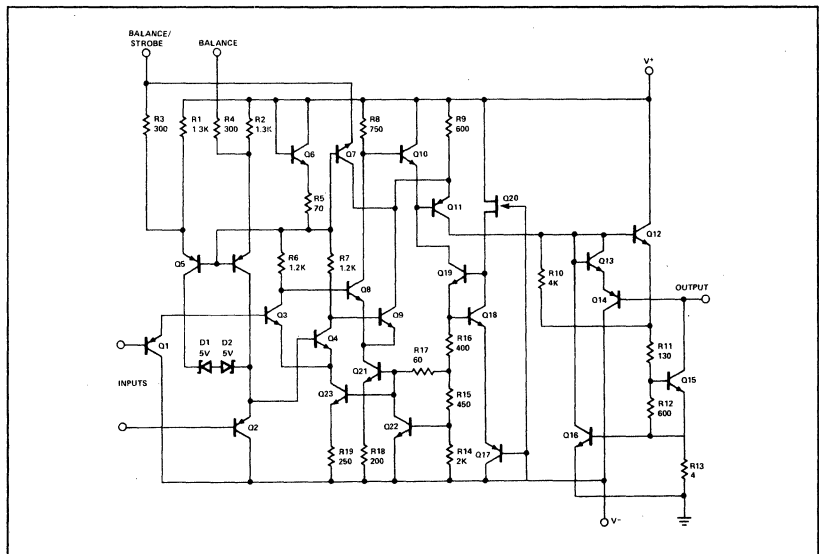
FEATURES

- Operates from single 5V supply
- Maximum input bias current: 150nA (LM311 - 250nA)
- Maximum offset current: 20nA (LM311 - 50nA)
- Differential input voltage range: $\pm 30V$
- Power consumption: 135mW at $\pm 15V$
- High sensitivity—200V/mV
- Military qualification pending

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage:		
LM111/LM211	50	V
LM311	40	V
Ground to negative supply voltage	30	V
Differential input voltage	±30	V
Input voltage ¹	±15	V
Power dissipation ²	500	mW
Output short circuit duration	10	sec
Operating temperature range		
LM111	-55 to +125	°C
LM211	-25 to +85	°C
LM311	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS 1,2,3

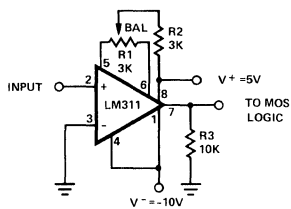
PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ⁴	$T_A = 25^\circ\text{C}, R_S \leq 50\text{k}\Omega$		0.7	3.0		2.0	7.5	mV
Input offset current ⁴	$T_A = 25^\circ\text{C}$		4.0	10		6.0	50	nA
Input bias current	$T_A = 25^\circ\text{C}$		60	100		100	250	nA
Voltage gain	$T_A = 25^\circ\text{C}$		200			200		V/mV
Response time ⁵	$T_A = 25^\circ\text{C}$		200			200		ns
Saturation voltage	$V_{IN} \leq -5\text{mV}, I_{OUT} = 50\text{mA}$ $T_A = 25^\circ\text{C}$		0.75	1.5		0.75	1.5	V
Strobe on current	$T_A = 25^\circ\text{C}$		3.0			3.0		mA
Output leakage current	$V_{IN} \geq 5\text{mV}, V_{OUT} = 35\text{V}$ $T_A = 25^\circ\text{C}, I_{STROBE} = 3\text{mA}$		0.2	10		0.2	50	nA
Input offset voltage ⁴	$R_S \leq 50\text{k}\Omega$			4.0			10	mV
Input offset current ⁴				20			70	nA
Input bias current				150			300	nA
Input voltage range			±14			±14		V
Saturation voltage	$V_+ \geq 4.5\text{V}, V_- = 0$ $V_{IN} \leq -6\text{mV}, I_{SINK} \leq 8\text{mA}$		0.23	0.4		0.23	0.4	V
Output leakage current	$V_{IN} \geq 5\text{mV}, V_{OUT} = 35\text{V}$		0.1	0.5				µA
Positive supply current	$T_A = 25^\circ\text{C}$		5.1	6.0		5.1	7.5	mA
Negative supply current	$T_A = 25^\circ\text{C}$		4.1	5.0		4.1	5.0	mA

NOTES

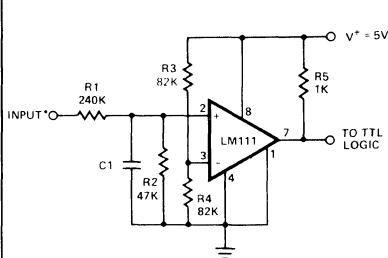
1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, in the N package, a thermal resistance of 162°C/W, and °C/W for the Ceramic package. The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient. The thermal resistance of the Cerdip package is 110°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15\text{V}$ and $0^\circ\text{C} < T_A < 70^\circ\text{C}$ unless otherwise specified. With the LM211, however, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ and for the LM111 is limited to $-55^\circ\text{C} < T_A < 125^\circ\text{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

TYPICAL APPLICATIONS

ZERO CROSSING DETECTOR
DRIVING MOS LOGIC



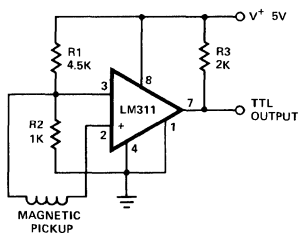
TTL INTERFACE WITH HIGH
LEVEL LOGIC



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

DETECTOR FOR MAGNETIC
TRANSDUCER



5

DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μ A710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

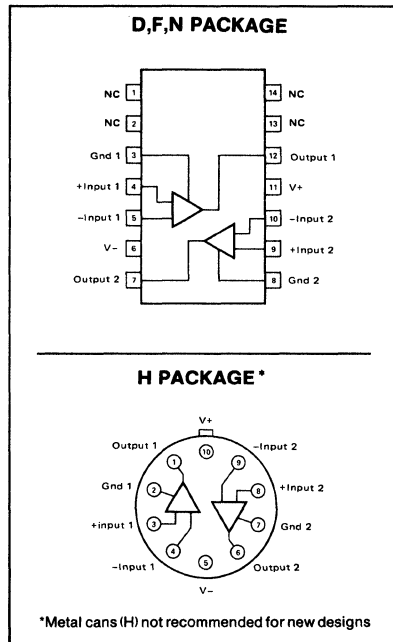
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to $\pm 15V$. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μ A711.

The LM119 is specified from $-55^{\circ}C$ to $+125^{\circ}C$, the LM219 is specified from $-25^{\circ}C$ to $+85^{\circ}C$, and the LM319 is specified from $0^{\circ}C$ to $+70^{\circ}C$.

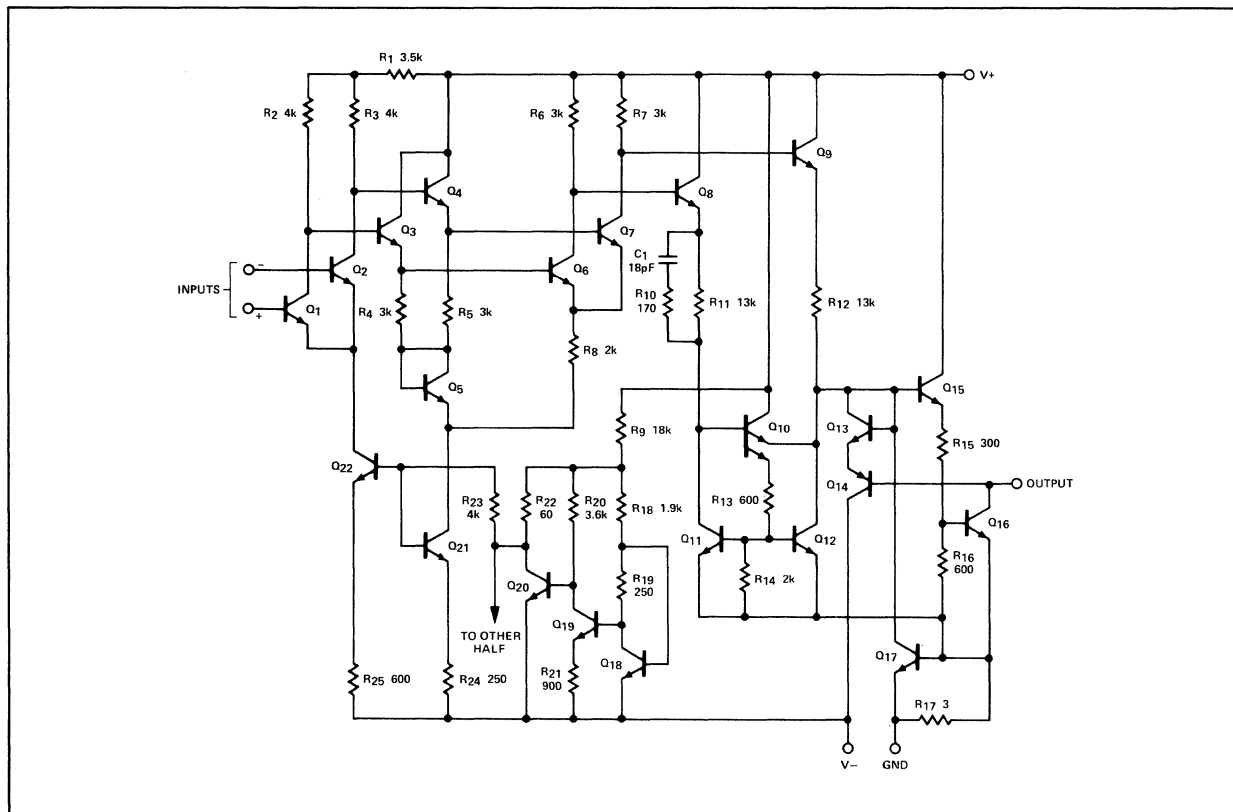
FEATURES

- Two independent comparators
- Operates from a single 5V supply
- Typically 80ns response time at $\pm 15V$
- Minimum fan-out of 3 (each side)
- Maximum input current of $1\mu A$ over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate
- Mil std 883 A, B, C available

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage	36	V
Ground to negative supply voltage	25	V
Ground to positive supply voltage	18	V
Differential input voltage	±5	V
Input voltage ¹	±15	V
Power dissipation ²	500	mW
Output short circuit duration	10	s
Operating temperature range		
LM119	-55 to +125	°C
LM219	-25 to +85	°C
LM319	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NOTES

- For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
- The absolute maximum junction temperature is 150°C. Device dissipation must be derated as follows:
N/K package—150°C/watt above 75°C
F package —110°C/watt above 95°C



DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, for $\left. \begin{matrix} \text{LM119, } -55^\circ\text{C} \leq T_A \leq 125^\circ\text{C} \\ \text{LM219, } -25^\circ\text{C} \leq T_A \leq 85^\circ\text{C} \\ \text{LM319, } 0^\circ\text{C} \leq T_A \leq 70^\circ\text{C} \end{matrix} \right\}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM119/219			LM319			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Input offset voltage ^{1,2}	R _S ≤ 5KΩ, T _A = 25°C Over temp.		0.7	4.0		2.0	8.0	mV
				7			10	mV
I _{OS} Input offset current ^{1,2}	T _A = 25°C Over temp.		30	75		80	200	nA
				100			300	nA
I _B Input bias current ¹	T _A = 25°C Over temp.		150	500		250	1000	nA
				1000			1200	nA
A _V Voltage gain	T _A = 25°C	10	40		8	40		V/mV
V _{OL} Saturation voltage	V _{IN} = 5mV, I _{OUT} = 25mA, T _A = 25°C		0.75	1.5		0.75	1.5	V
	V _{IN} = 10mV, I _{OUT} = 25mA, T _A = 25°C V ⁺ ≥ 4.5V, V ⁻ = 0							V
	V _{IN} = 6mV, I _{OUT} = 3.2mA T _A ≥ 0°C		0.23	0.4				V
	T _A ≤ 0°C V _{IN} = 10mV, I _{OUT} = 3.2mA			0.6		0.3	0.4	V
I _{OH} Output leakage current	V ⁻ = 0V, V _{IN} = 5mV V _{OUT} = 35V, T _A = 25°C Over temp.		0.2	2				μA
	V ⁻ = 0V, V _{IN} = 10mV V _{OUT} = 35V, T _A = 25°C		1	10				μA
V _{IN} Input voltage range	V _S = ±15V		±13			±13		V
	V ⁺ = 5V, V ⁻ = 0V	1		3	1		3	V
V _{ID} Differential input voltage				±5			±5	V
I ⁺ Positive supply current	V ⁺ = 5V, V ⁻ = 0V, T _A = 25°C		4.3			4.3		mA
I ⁺ Positive supply current	V _S = ±15V, T _A = 25°C		8.0	11.5		8.0	12.5	mA
I ⁻ Negative supply current	V _S = ±15V, T _A = 25°C		3.0	4.5		3.0	5.0	mA

NOTES

- V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of V_S = ±15V down to a single 5V supply.
- The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

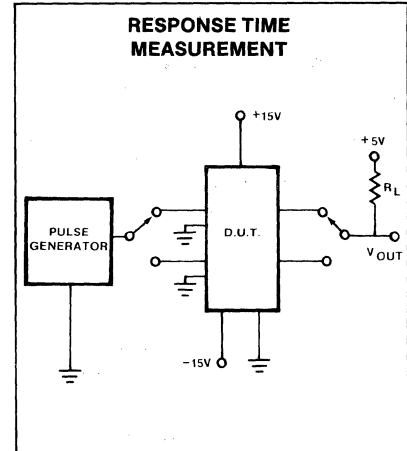
AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Response time*	$V_S = \pm 15V, T_A = 25^\circ C$ $R_L = 500\Omega$ (see test figure)		80		ns

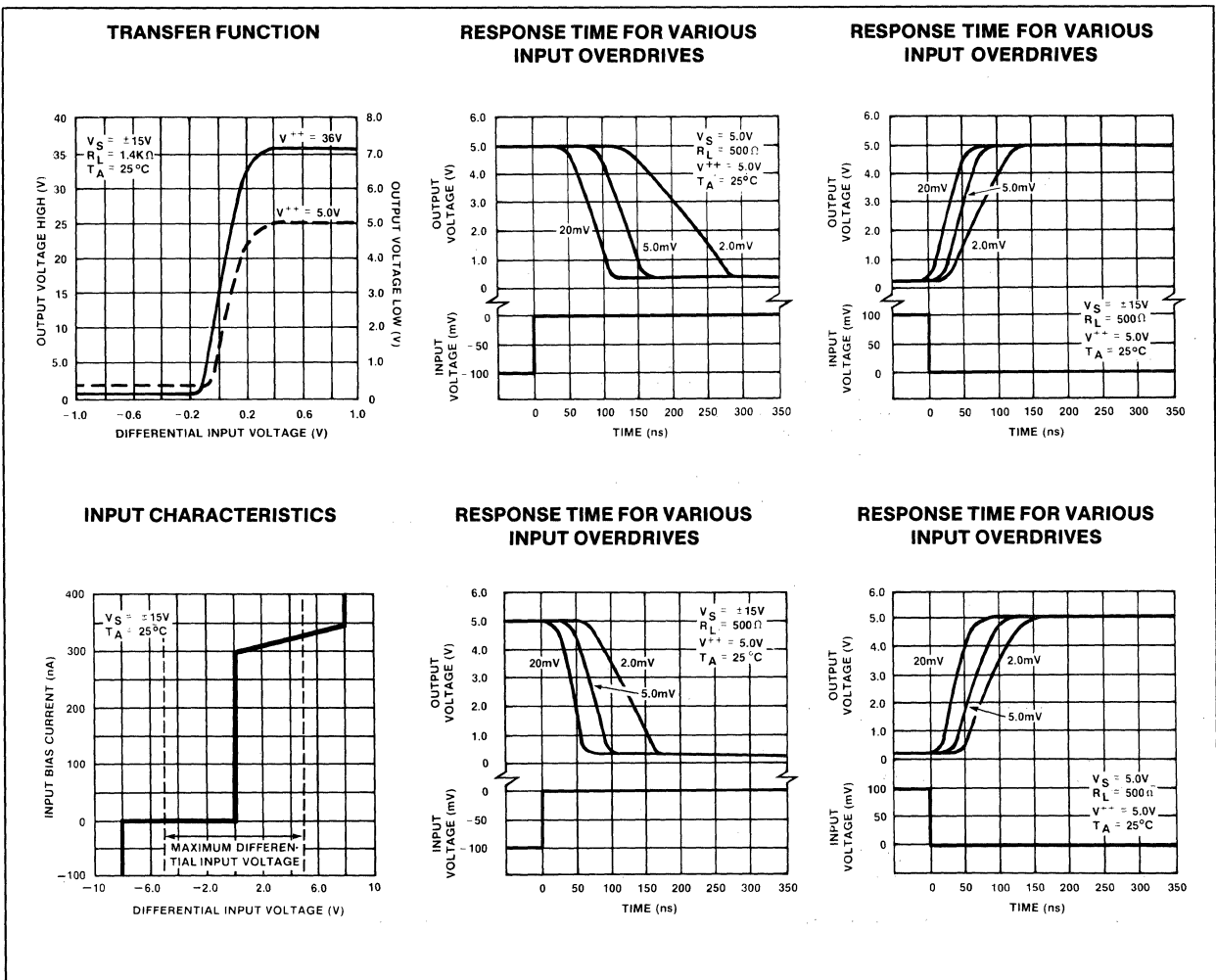
*NOTE

The response time specified is for a 100mV step with 5mV overdrive.

TEST CIRCUIT

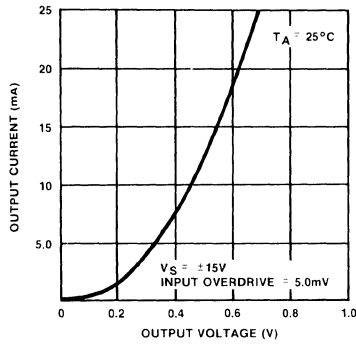


TYPICAL PERFORMANCE CHARACTERISTICS

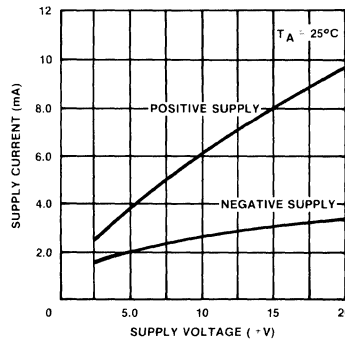


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

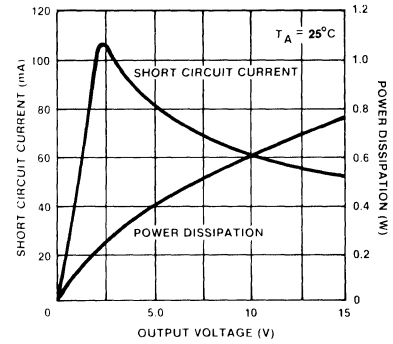
OUTPUT SATURATION VOLTAGE



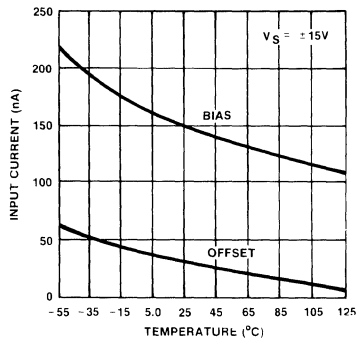
SUPPLY CURRENT



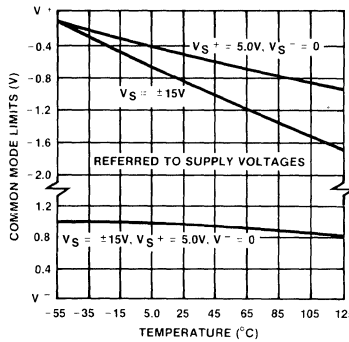
OUTPUT LIMITING CHARACTERISTICS



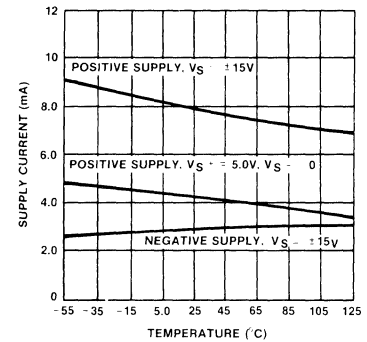
INPUT CURRENTS (LM119/219)



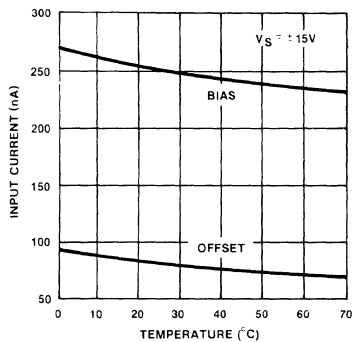
COMMON MODE LIMITS (LM119/219)



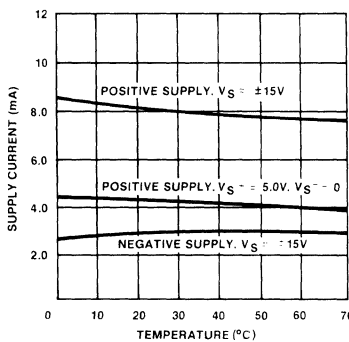
SUPPLY CURRENT (LM119/219)



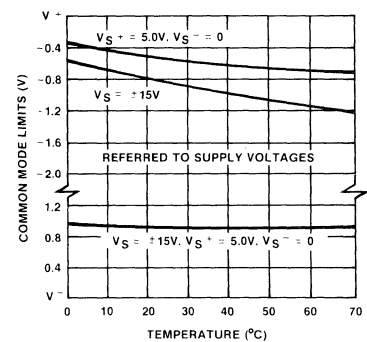
INPUT CURRENTS (LM319)



SUPPLY CURRENTS (LM319)



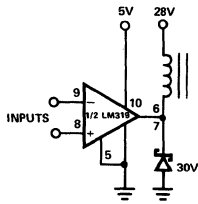
COMMON MODE LIMITS (LM319)



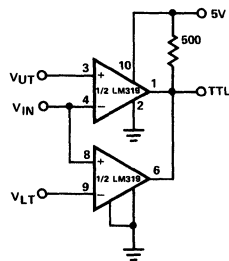
5

TYPICAL APPLICATIONS

RELAY DRIVER

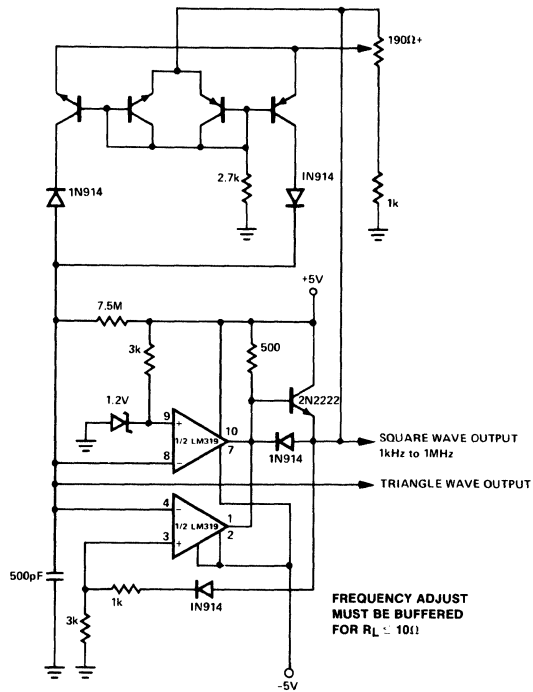


WINDOW DETECTOR



$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$
 $V_{OUT} = 0$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

WIDE RANGE VARIABLE
OSCILLATOR



DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

- Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies $\pm 1.0Vdc$ to $\pm 18Vdc$
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0Vdc)
- Low input biasing current 25nA
- Low input offset current $\pm 5nA$ and offset voltage $\pm 2mV$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage.
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.

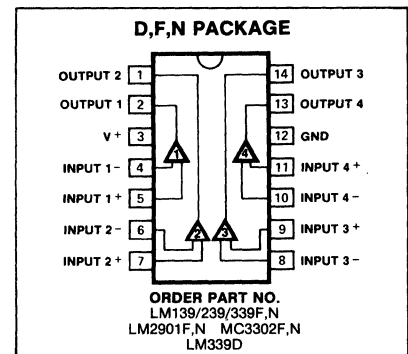
APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

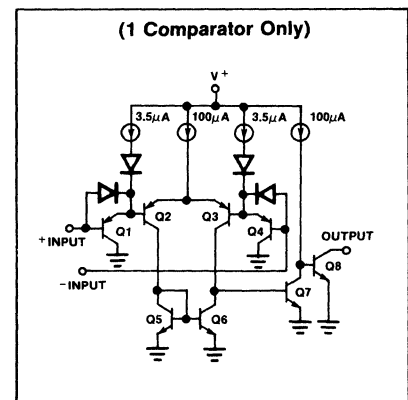
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} supply voltage	36 or ± 18	
Differential input voltage	36	
Input voltage	-0.3 to +36	
Power dissipation ¹		
Molded DIP	570	mW
CERDIP	900	mW
Output short circuit to ground ²	Continuous	
Input current (V _{IN} < -0.3Vdc) ³	50	mA
Operating temperature range		
LM139	-55 to +125	°C
LM239	-25 to +85	°C
LM339	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

PIN CONFIGURATION



EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_+ = 5V_{dc}$, LM139: $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ unless otherwise specified
LM239: $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ unless otherwise specified
LM339: $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ⁵	$T_A = 25^{\circ}C$ Over temp.		± 2.0	± 5.0 9.0		± 2.0	± 5.0 9.0	mV
V_{CM} Input common mode voltage range ⁶	$T_A = 25^{\circ}C$ Over temp.	0		$V_+ - 1.5$ $V_+ - 2.0$	0		$V_+ - 1.5$ $V_+ - 2.0$	V
V_{IDR} Differential input voltage ⁴	Keep all $V_{INs} \geq 0V_{dc}$ (or V -if used)			V_+			V_+	V
I_B Input bias current ⁷	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^{\circ}C$ Over temp.		25	100 300		25	250 400	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^{\circ}C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{dc}$, $T_A = 25^{\circ}C$	6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1V_{dc}$, $V_{IN(-)} = 0$ $V_O = 5V_{dc}$, $T_A = 25^{\circ}C$ $V_O = 30V_{dc}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC} Supply current	$R_L = \infty$ on all comparators, $T_A = 25^{\circ}C$		0.8	2.0		0.8	2.0	mA
A_V Voltage gain	$R_L \geq 15k\Omega$, $V_+ = 15V_{dc}$ $T_A = 25^{\circ}C$	50	200		50	200		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25^{\circ}C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR} Large signal response time	$V_{IN} = TTL$ logic swing, $V_{REF} = 1.4V_{dc}$, $V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^{\circ}C$		300			300		ns
T_R Response time ⁸	$V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^{\circ}C$		1.3			1.3		μs

DC ELECTRICAL CHARACTERISTICS $V+ = 15V_{dc}$, MC3302
LM2901/MC3302: $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ unless otherwise specified

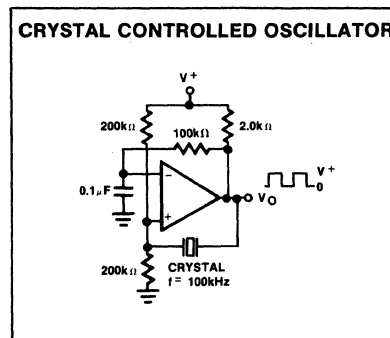
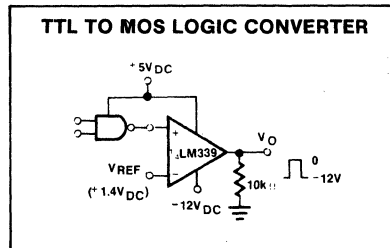
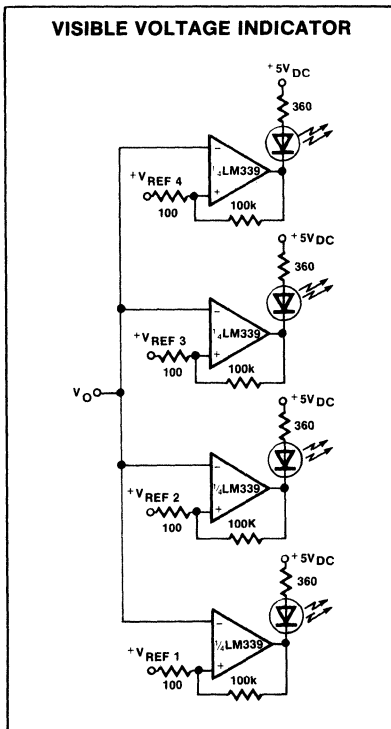
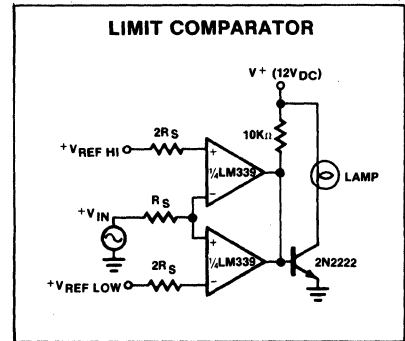
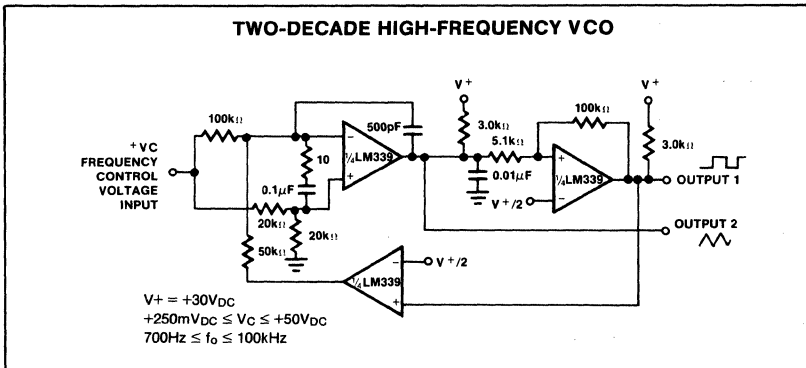
PARAMETER	TEST CONDITIONS	LM2901			MC3302			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Input offset voltage ⁵	T _A = 25°C Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV
V _{CM} Input common mode voltage range ⁶	T _A = 25°C Over temp.	0 0		V+ - 1.5 V+ - 2.0			V+ - 1.5 V+ - 2.0	V
V _{IDR} Differential input voltage ⁴	Keep all V _{IN} 's ≥ 0Vdc (or V- if need)			V+			V+	V
I _B Input bias current ⁷	I _{IN(+)} or I _{IN(-)} with output in linear range T _A = 25°C Over temp.		25 200	250 500		25	500 1000	nA
I _{OS} Input offset current	I _{IN(+)} - I _{IN(-)} T _A = 25°C Over temp.		±5 ±50	±50 ±200		±5		nA nA
I _{OL} Output sink current	V _{IN(-)} ≥ 1Vdc, V _{IN(+)} = 0, V _O ≤ 1.5Vdc, T _A = 25°C V _O = 800mV, Over temp.	6.0	16		2.0			mA
I _{OH} Output leakage current	V _{IN(+)} ≥ 1Vdc, V _{IN(-)} = 0 V _O = 5Vdc, T _A = 25°C V _O = 30V Over temp. V _O = 28V T _A = 25°C		0.1	1.0		0.1	1.0	nA μA
I _{CC} Supply current	R _L = ∞ on comparators, V+ = 5Vdc, T _A = 25°C V+ = 30V, T _A = 25°C V+ = 5 to 28 Vdc, T _A = 25°C		0.8 1.0	2.0 2.5		0.8	2.0	mA
A _V Voltage gain	R _L ≥ 15kΩ, V+ = 15Vdc T _A = 25°C	25	100		2	100		V/mV
V _{OL} Saturation voltage	V _{IN(-)} ≥ 1Vdc, V _{IN(+)} = 0, I _{SINK} ≤ 4mA T _A = 25°C Over temp. I _{SINK} = 2mA, V+ = 5V to 28V, T _A = 25°C		400	400 700		150	400	mV
T _{LSR} Large signal response time	V _{IN} = TTL logic swing, V _{REF} = 1.4Vdc, V _{RL} = 5Vdc, R _L = 5.1kΩ, T _A = 25°C		300			300		ns
T _R Response time ⁸	V _{RL} = 5Vdc, R _L = 5.1kΩ, T _A = 25°C		1.3			1.3		μs



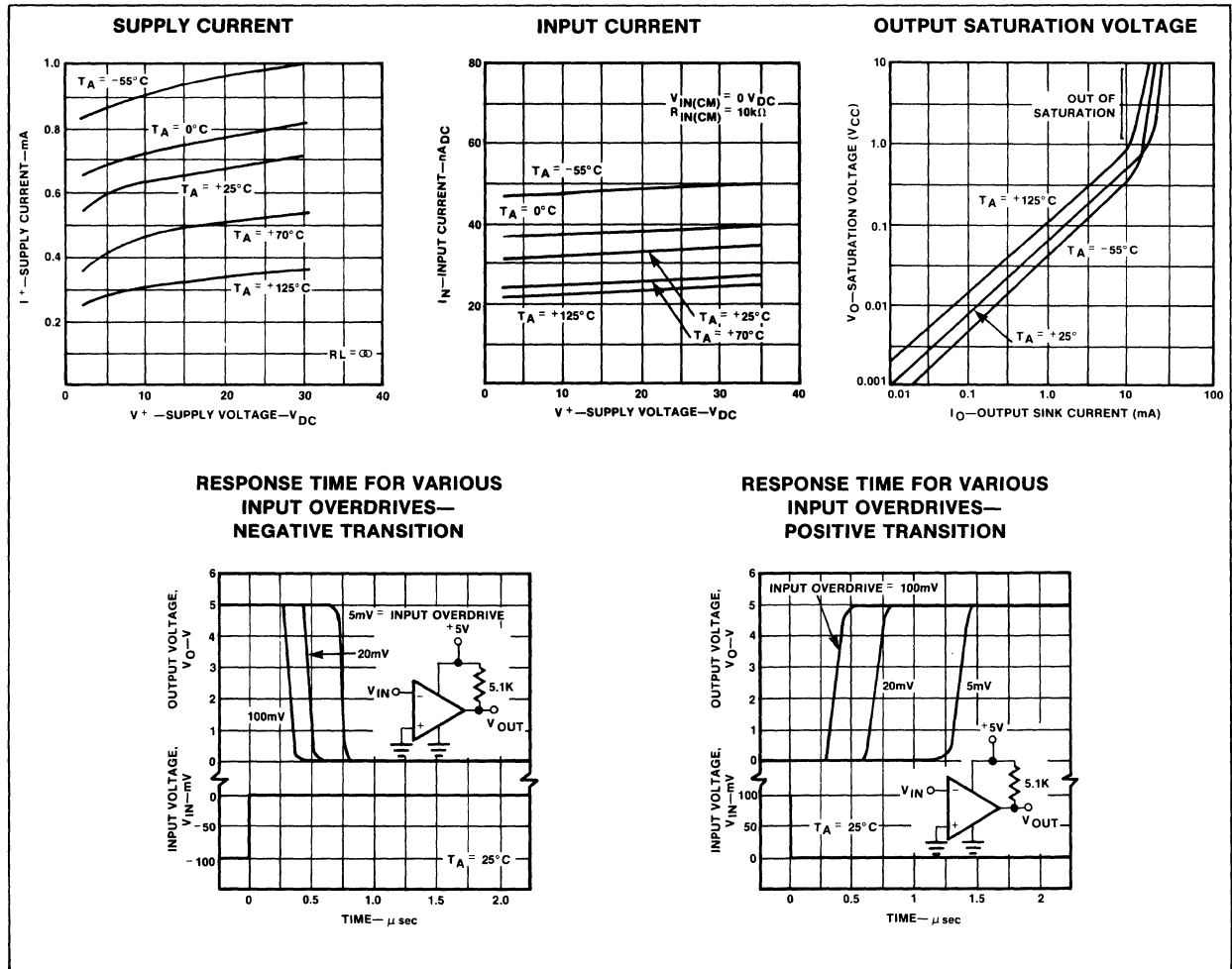
NOTES

- For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V_+ .
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V_+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{dc}$.
- Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{dc}$ (or $0.3V_{dc}$ below the magnitude of the negative power supply, if used).
- At output switch point, $V_O \approx 1.4V_{dc}$, $R_S = 0\Omega$ with V_+ from $5V_{dc}$ to $30V_{dc}$; and over the full input common-mode range ($0V_{dc}$ to $V_+ - 1.5V_{dc}$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $30V_{dc}$ without damage.
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.

TYPICAL APPLICATIONS



TYPICAL PERFORMANCE CHARACTERISTICS



5

LM193/293/393/193A/293A/393A/2903-N,FE,H

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

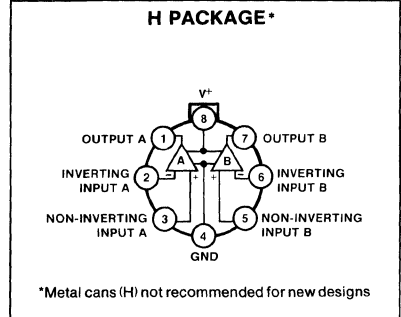
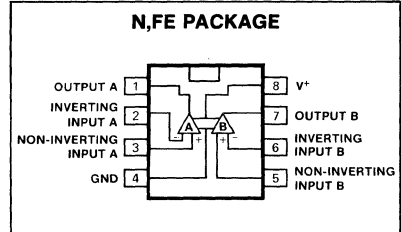
FEATURES

- Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies $\pm 1.0Vdc$ to $\pm 18Vdc$
- Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/-comparator at 5.0Vdc)
- Low input biasing current 25nA
- Low input offset current $\pm 5nA$ and offset voltage $\pm 2mV$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage.
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

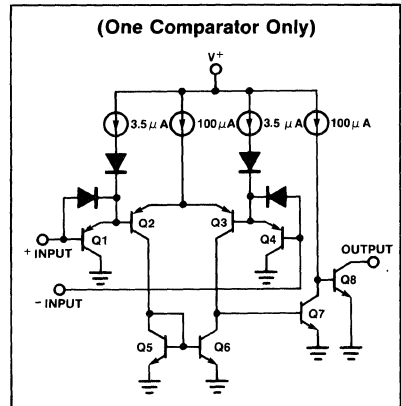
PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Vcc supply voltage	36 or ± 18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation ¹		
Molded DIP	570	mW
Metal can	900	mW
Output short circuit to ground ²	Continuous	
Input current ($V_{IN} < -0.3Vdc$) ³	50	mA
Operating temperature range		
LM193/193A	-55 to +125	°C
LM293/293A	-25 to +85	°C
LM393/393A	0 to +70	°C
LM2903	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT



LM193/293/393/193A/293A/393A/2903-N,FE,H

DC ELECTRICAL CHARACTERISTICS $V_+ = 5V_{dc}$, LM193/193A: $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise specified.
 LM293/293A: $-25^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.
 LM393/393A: $0^\circ C \leq T_A \leq +70^\circ C$ unless otherwise specified.
 LM2903: $-40^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.⁷

PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ⁵	$T_A = 25^\circ C$ Over temp.		± 1.0	± 2.0 ± 4.0		± 1.0	± 2.0 ± 4.0		± 2.0 ± 9	± 7.0 ± 15	mV
V_{CM} Input common mode voltage range ^{6,10}	$T_A = 25^\circ C$ Over temp.	0 0		$V+ - 1.5$ $V+ - 2.0$	0 0		$V+ - 1.5$ $V+ - 2.0$	0 0		$V+ - 1.5$ $V+ - 2.0$	V
V_{IDR} Differential input voltage ⁴	Keep all $V_{INs} \geq 0V_{dc}$ (or $V-$ -if need)			$V+$			$V+$			$V+$	V
I_B Input bias current ⁸	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^\circ C$ Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^\circ C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150		± 5 ± 50	± 50 ± 200	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $V_0 \leq 1.5V_{dc}$, $T_A = 25^\circ C$	6.0	16		6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1V_{dc}$, $V_{IN(-)} = 0$ $V_0 = 30V_{dc}$ Over temp. $V_0 = 5V_{dc}$, $T_A = 25^\circ C$		0.1	1.0		0.1	1.0		0.1	1.0	μA na
I_{CC} Supply current	$R_L = \infty$ on both comparators. $T_A = 25^\circ C$ $V_+ = 30V$, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V Voltage gain	$R_L \geq 15k\Omega$, $V_+ = 15V_{dc}$, $T_A = 25^\circ C$	50	200		50	200		25	100		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25^\circ C$ Over temp.		250	400 700		250	400 700		400	400 700	mV
T_{LSR} Large signal response time	$V_{IN} = TTL$ logic swing, $V_{REF} = 1.4V_{dc}$, $V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		300			300			300		ns
T_R Response time ⁹	$V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		1.3			1.3			1.3		μs



DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_+ = 5V_{dc}$, LM193/193A: $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise specified.
LM293/293A: $-25^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.
LM393/393A: $0^\circ C \leq T_A \leq +70^\circ C$ unless otherwise specified.
LM2903: $-40^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.⁷

LM193/293/393/193A/293A/393A/2903-N,FE,H

PARAMETER	TEST CONDITIONS	LM193			LM293/393			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ⁵	$T_A = 25^\circ C$ Over temp.		± 2.0	± 5.0 ± 9.0		± 2.0	± 5.0 ± 9.0	mV
V_{CM} Input common mode voltage range ^{6,10}	$T_A = 25^\circ C$ Over temp.	0 0		$V_{\pm 1.5}$ $V_{\pm 2.0}$	0 0		$V_{\pm 1.5}$ $V_{\pm 2.0}$	V
V_{IDR} Differential input voltage ⁴	Keep all V_{IN} 's $\geq 0V_{dc}$ (or V-if need)			V+			V+	V
I_B Input bias current ⁸	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^\circ C$ Over temp.		25	100 300		25	250 400	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^\circ C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{dc}$, $T_A = 25^\circ C$	6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1V_{dc}$, $V_{IN(-)} = 0$ $V_O = 5V_{dc}$, $T_A = 25^\circ C$ $V_O = 30V_{dc}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC} Supply current	$R_L = \infty$ on both comparators $T_A = 25^\circ C$ $V_+ = 30V$, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V Voltage gain	$R_L \geq 15K\Omega$, $V_+ = 15V_{dc}$	50	200		50	200		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25^\circ C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR} Large signal response time	$V_{IN} = TTL$ logic swing, $V_{REF} = 1.4V_{dc}$, $V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		300			300		ns
T_R Response time ⁹	$V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		1.3			1.3		μs

NOTES

- For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a $125^\circ C$ maximum junction temperature and a thermal resistance of $175^\circ C/W$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a $150^\circ C$ maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V_+ .
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V_+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{dc}$.
- Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{dc}$ (V_{dc} below the magnitude of the negative power supply, if used).
- At output switch point, $V_O = 1.4V_{dc}$, $R_S = 0\Omega$ with V_+ from $5V_{dc}$ to $30V_{dc}$; and over the full input common-mode range ($0V_{dc}$ to $V_+ - 1.5V_{dc}$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $30V_{dc}$ without damage.
- With the LM293/293A, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$ and the LM393/393A, all temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$. The LM2903 is limited to $-40^\circ C \leq T_A \leq +85^\circ C$.
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The response time specified is for a 100mV input step with a 5mV overdrive.
- For input signals that exceed V_{CC} , only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

NE521-F,N
SE521-F

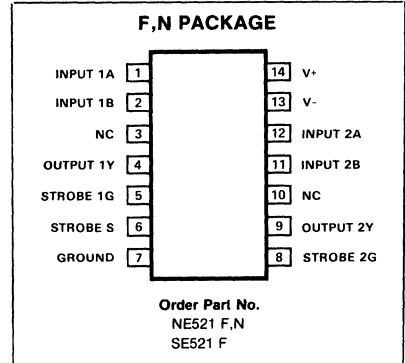
FEATURES

- 12ns maximum guaranteed propagation delay
- 20µA maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

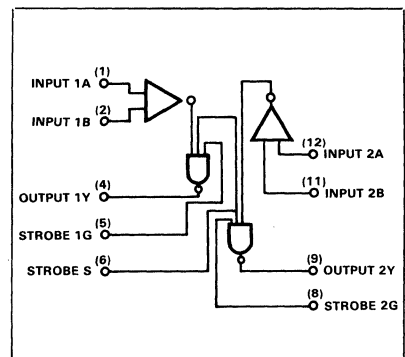
PIN CONFIGURATION



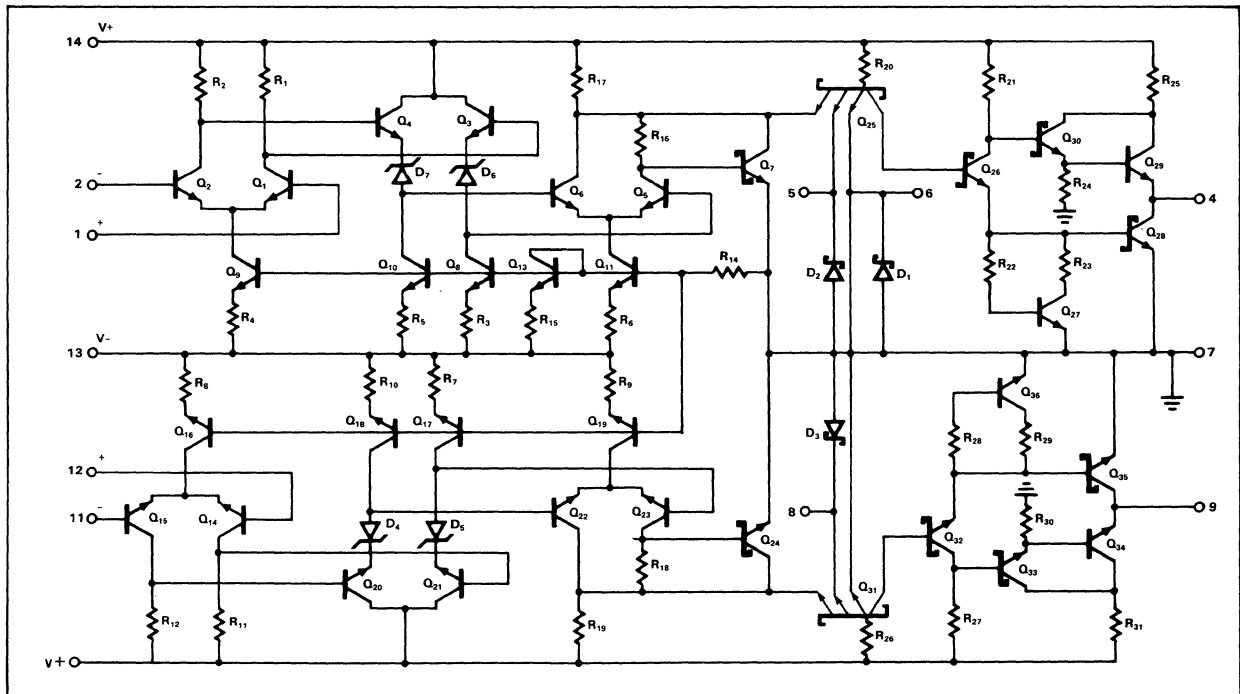
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		V
V+	+7	
V-	-7	
V _{IDR}	±6	V
V _{IN}		V
Common mode	±5	
Strobe/gate	+5.25	
P _D	600	mW
T _A		°C
NE	0 to 70	
SE	-55 to +125	
T _{stg}		°C
Storage temperature range	-65 to +150	
Lead temperature	+300	
(solder, 60 sec)		

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V_+ = +5V$, $V_- = -5V$, $T_A = -55$ to $+125^\circ\text{C}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE LIMITS			UNITS	
		Min	Typ	Max		
V_{OS}	Input offset voltage At 25°C Over temperature range		6	7.5 15	mV	
I_{BIAS}	Input bias current At 25°C Over temperature range		7.5	20 40	μA	
I_{OS}	Input offset current At 25°C Over temperature range		1.0	5 12	μA	
V_{CM}	Common mode voltage range	± 3			V	
V_{IL}	Low level input voltage At 25°C Over temperature			0.8 0.7	V	
V_{IH}	High level input voltage	2.0			V	
I_{IH}	Input current High	$V_+ = +5.5V$, $V_- = -5.5V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S		50 100	μA μA	
I_{IL}	Low	$V_{IL} = 0.5V$ 1G or 2G strobe Common strobe S		-2.0 -4.0	mA mA	
V_{OH} V_{OL}	Output voltage High Low	$V_I(S) = 2.0V$ $V_+ = +4.5V$, $V_- = -4.5V$, $I_{LOAD} = -1mA$ $V_+ = +4.5V$, $V_- = -4.5V$, $I_{LOAD} = 10mA$ $T_A = 25^\circ\text{C}$, $I_{LOAD} = 20mA$	2.5	3.4	0.5 0.5	V
V_+ V_-	Supply voltage Positive Negative		4.5 -4.5	5.0 -5.0	5.5 -5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	$V_+ = 5.5V$, $V_- = -5.5V$, $T_A = 25^\circ\text{C}$		27 -15	50 -28	mA
I_{SC}	Short circuit output current		-35		-115	μA



DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_+ = +5V, V_- = -5V, T_A = 0$ to $70^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	NE LIMITS			UNITS
		Min	Typ	Max	
V_{OS} Input offset voltage At $25^\circ C$ Over temperature range	$V_+ = +4.75V, V_- = -4.75V$		6	7.5 10	mV
I_{BIAS} Input bias current At $25^\circ C$ Over temperature range	$V_+ = +5.25V, V_- = -5.25V$		7.5	20 40	μA
I_{OS} Input offset current At $25^\circ C$ Over temperature range	$V_+ = +5.25V, V_- = -5.25V$		1.0	5 12	μA
V_{CM} Common mode voltage range	$V_+ = +4.75V, V_- = -4.75V$	± 3			V
I_{IH} Input current High	$V_+ = +5.25V, V_- = -5.25V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL} Low	$V_{IL} = 0.5V$ 1G or 2G strobe Common strobe S			-2.0 -4.0	mA mA
V_{OH} V_{OL} Output voltage High Low	$V_{I(S)} = 2.0V$ $V_+ = +4.75V, V_- = -4.75V, I_{LOAD} = -1mA$ $V_+ = +5.25V, V_- = -5.25V, I_{LOAD} = 20mA$	2.7	3.4	0.5	V
V_+ V_- Supply voltage Positive Negative		4.75 -4.75	5.0 -5.0	5.25 -5.25	V
I_{CC+} I_{CC-} Supply current Positive Negative	$V_+ = 5.25V, V_- = -5.25V, T_A = 25^\circ C$		27 -15	50 -28	mA
I_{SC} Short circuit output current		-40		-100	μA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, R_L = 280 \Omega, C_L = 15pF, V_+ = +5V, V_- = -5V$

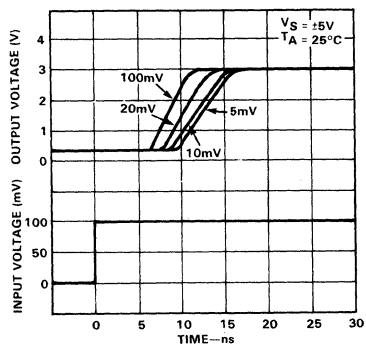
PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
			Min	Typ	Max	
Large Signal Switching Speed Propagation delay						ns
$t_{PLH(D)}$ Low to high ¹	Amp	Output		8	12	
$t_{PHL(D)}$ High to low ¹	Amp	Output		6	9	
$t_{PLH(S)}$ Low to high ²	Strobe	Output		4.5	10	
$t_{PHL(S)}$ High to low ²	Strobe	Output		3.0	6	
Maximum operating frequency			40	55		MHz

NOTES

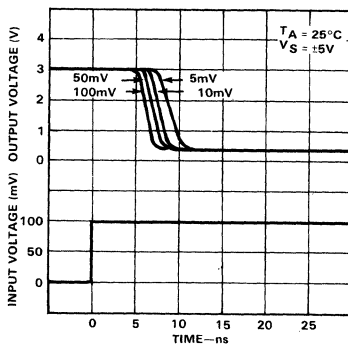
- Response time measured from 0V point of $\pm 100mV$ p-p 10MHz square wave to the 1.5V point of the output
- Response time measured from 1.5V point of input to 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

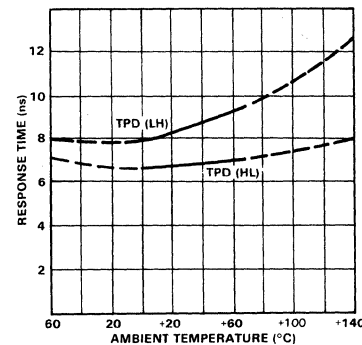
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



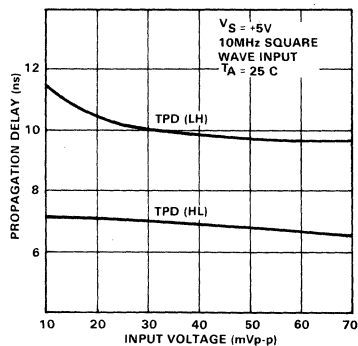
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



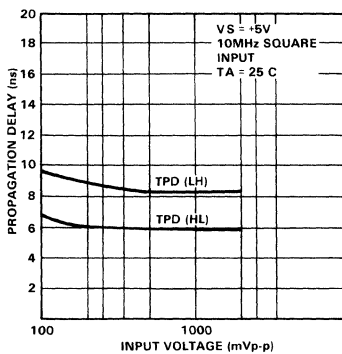
RESPONSE TIME vs TEMPERATURE



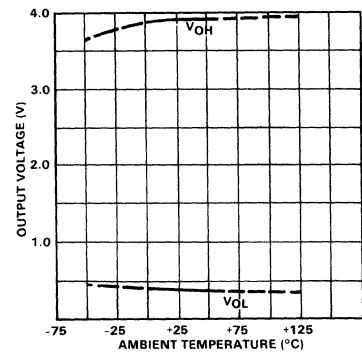
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



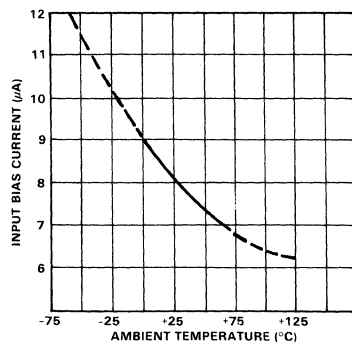
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



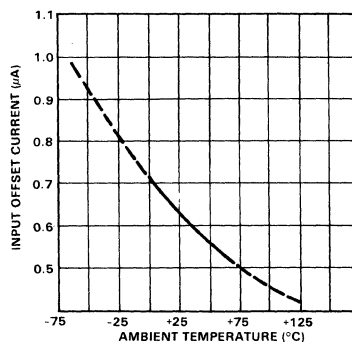
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



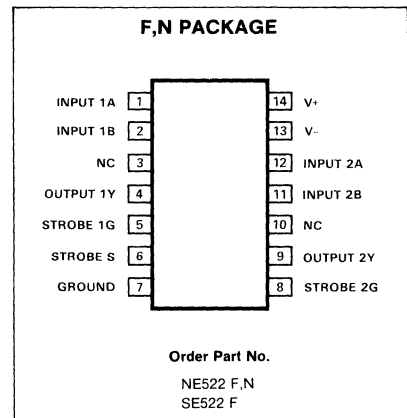
FEATURES

- 15ns maximum guaranteed propagation delay
- 20 μ A maximum input bias current
- TTL compatible strobes and outputs
- Open collector output for wire-OR'd applications
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

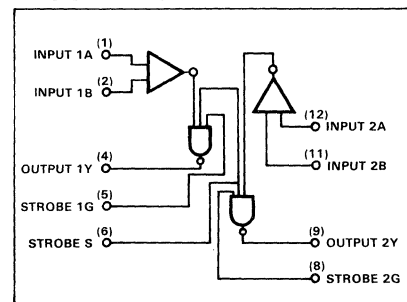
PIN CONFIGURATION



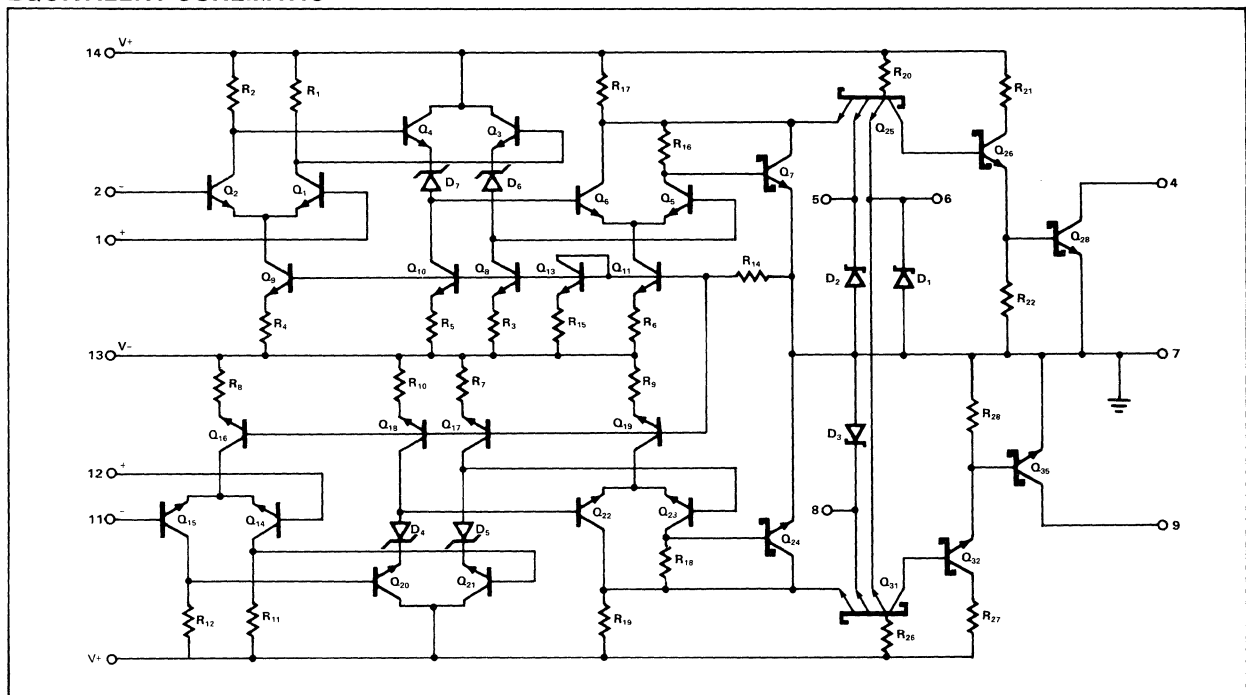
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V+	Supply voltage	V
	Positive	+7
V-	Negative	-7
VIDR	Differential input voltage	± 6
V _{IN}	Input voltage	V
	Common mode	± 5
	Strobe/gate	± 5.25
P _D	Power dissipation	600
T _A	Operating temperature range NE	0 to 70
	SE	-55 to +125
T _{stg}	Storage temperature range	-65 to +150
	Lead temperature (solder, 60 sec)	+300

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $\pm 5V \pm 10\%$, $T_A = -55$ to 125°C unless otherwise specified

PARAMETER	TEST CONDITIONS	SE LIMITS			UNIT	
		Min	Typ	Max		
V_{OS}	Input offset voltage At 25°C Over temperature range		6	7.5 15.	mV	
I_{BIAS}	Input bias current At 25°C Over temperature range		7.5	20. 40.	μA	
I_{OS}	Input offset current At 25°C Over temperature range		1.0	5. 12.	μA	
V_{CM}	Common mode voltage range	± 3			V	
V_{IL}	Low level input Voltage at 25°C over temperature			.08 .07	V	
V_{IH}	High level temperature	2.0			V	
I_{IH}	Input current High	$V_+ = +5.5V, V_- = -5.5V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S		50 100	μA μA	
I_{IL}	Low	$V_{IL} = 0.5V$ 1G 2G strobe Common strobe S		-2 -4	mA mA	
V_{OL}	Output voltage Low	$V_+ = +4.5V, V_- = -4.5V$ $I_{OL} = 20\text{mA}, T_A = 25^\circ\text{C}$ $I_{OL} = 10\text{mA}$.5 .5	V	
I_{OH}	Output current High	$V_{CC+} = +4.5, V_{CC-} = -4.5V, V_{OH} = 5.5V$		250	μA	
V_+ V_-	Supply voltage Positive Negative		4.5 -4.5	5.0 -5.0	5.5 -5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	$V_+ = 5.5V, V_- = -5.5V$		27 -15	50 -28	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\pm 5V \pm 5\%$, $T_A = 0$ to $70^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	NE LIMITS			UNIT	
		Min	Typ	Max		
V_{OS}	Input offset voltage At $25^\circ C$ Over temperature range		6	7.5 10	mV	
I_{BIAS}	Input bias current At $25^\circ C$ Over temperature range		7.5	20 40	μA	
I_{OS}	Input offset current At $25^\circ C$ Over temperature range		1.0	5 12	μA	
V_{CM}	Common mode voltage range		± 3		V	
I_{IH}	Input current High	$V_+ = +5.25V, V_- = -5.25V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S		50 100	μA μA	
I_{IL}	Low	$V_{IL} = 0.5V$ 1G 2G strobe Common strobe S		-2.0 -4.0	mA mA	
V_{OL}	Output voltage Low	$V_+ = +5.25V, V_- = -5.25V, V_I(S) = 2.0V$ $I_{LOAD} = 20mA$		0.5	V	
I_{OH}	Output current High	$V_{CC+} = +4.75,$ $V_{CC-} = -4.75V, V_{OH} = 5.25V$		250	μA	
V_+ V_-	Supply voltage Positive Negative		4.75 -4.75	5.0 -5.0	5.25 -5.25	V
I_{CC+} I_{CC-}	Supply current Positive Negative	$V_+ = 5.25V, V_- = -5.25V, T_A = 25^\circ C$		27 -15	50 -28	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, R_L = 280\Omega, C_L = 15pF$

PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
			Min	Typ	Max	
Input resistance				4		k Ω
Input capacitance				3		pF
Large Signal Switching Speed						
Propagation delay						ns
$t_{PLH(D)}$	Low to high ¹	Amp		10	15	
$t_{PHL(D)}$	High to low ¹	Amp		8	12	
$t_{PLH(S)}$	Low to high ²	Strobe		6	13	
$t_{PHL(S)}$	High to low ²	Strobe		5	9	
Maximum operating frequency			25	35		MHz

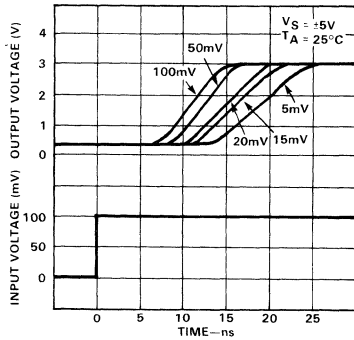
NOTES

- Response time measured from 0V point of $\pm 100mV$ p-p 10MHz square wave to the 1.5V point of the output
- Response time measured from 1.5V point of input to 1.5V point of the output

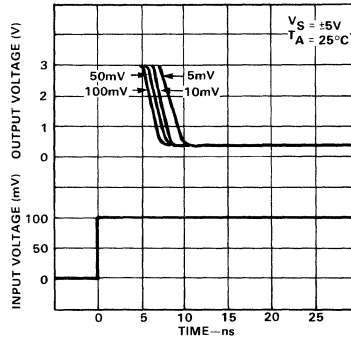


TYPICAL PERFORMANCE CHARACTERISTICS

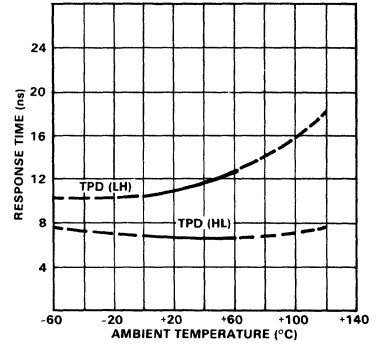
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



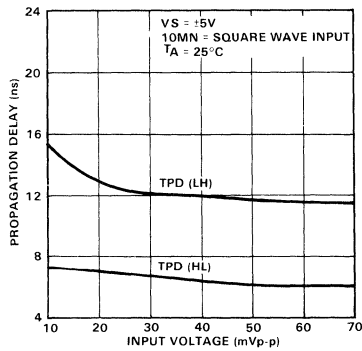
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



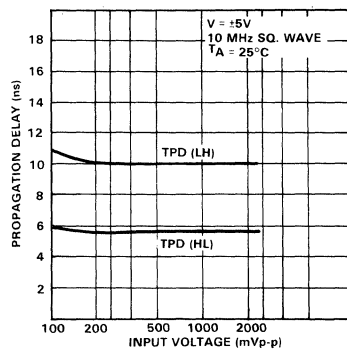
RESPONSE TIME vs TEMPERATURE



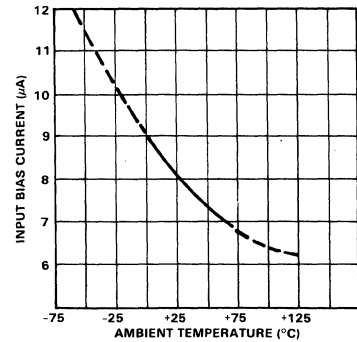
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



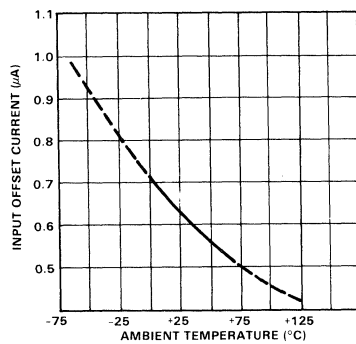
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T2L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

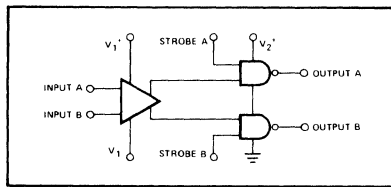
FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range
- Mil std 883A,B,C available

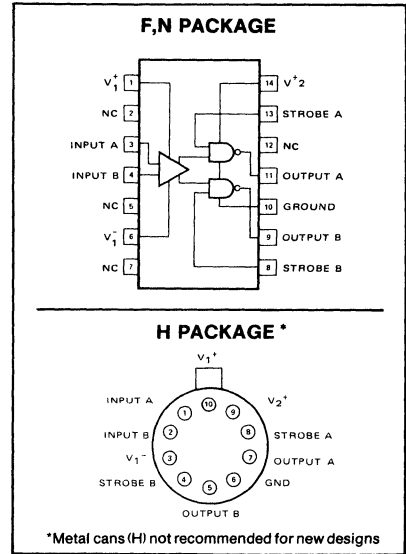
APPLICATIONS

- A/D conversion
- ECL to TTL interface
- TTL to ECL interface
- Memory sensing
- Optical data coupling

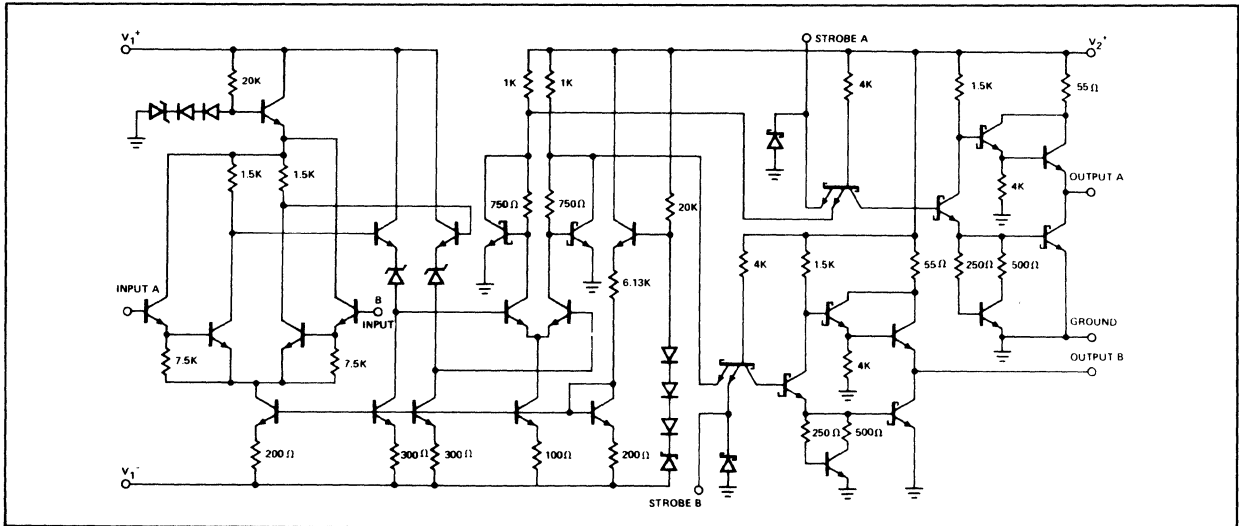
BLOCK DIAGRAM



PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_{1+} = 10V, V_{1-} = -10V, V_{2+} = +5.0V$

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C				2			2	μA
Over temperature range				4			4	μA
Input offset current @ 25°C	$V_{IN} = 0V$			0.5			0.75	μA
Over temperature range				1			1	μA
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_{2+} = 4.75V, I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_{2+} = 4.75V, I_{SINK} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current	$V_{2+} = 5.25V, V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C	$V_{2+} = 5.25V, V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_{2+} = 5.25V, V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_{2+} = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_{2+} = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_{2+} = 5.25V, V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V1+		5		10	5		10	V
V1-		-6		-10	-6		-10	V
V2+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_{1+} = 10V, V_{1-} = -10V$							
	$V_{2+} = 5.25V$							
I1+	Over temp.			5			5	mA
I1-	Over temp.			10			10	mA
I2+	Over temp.			20			20	mA

*NOTE

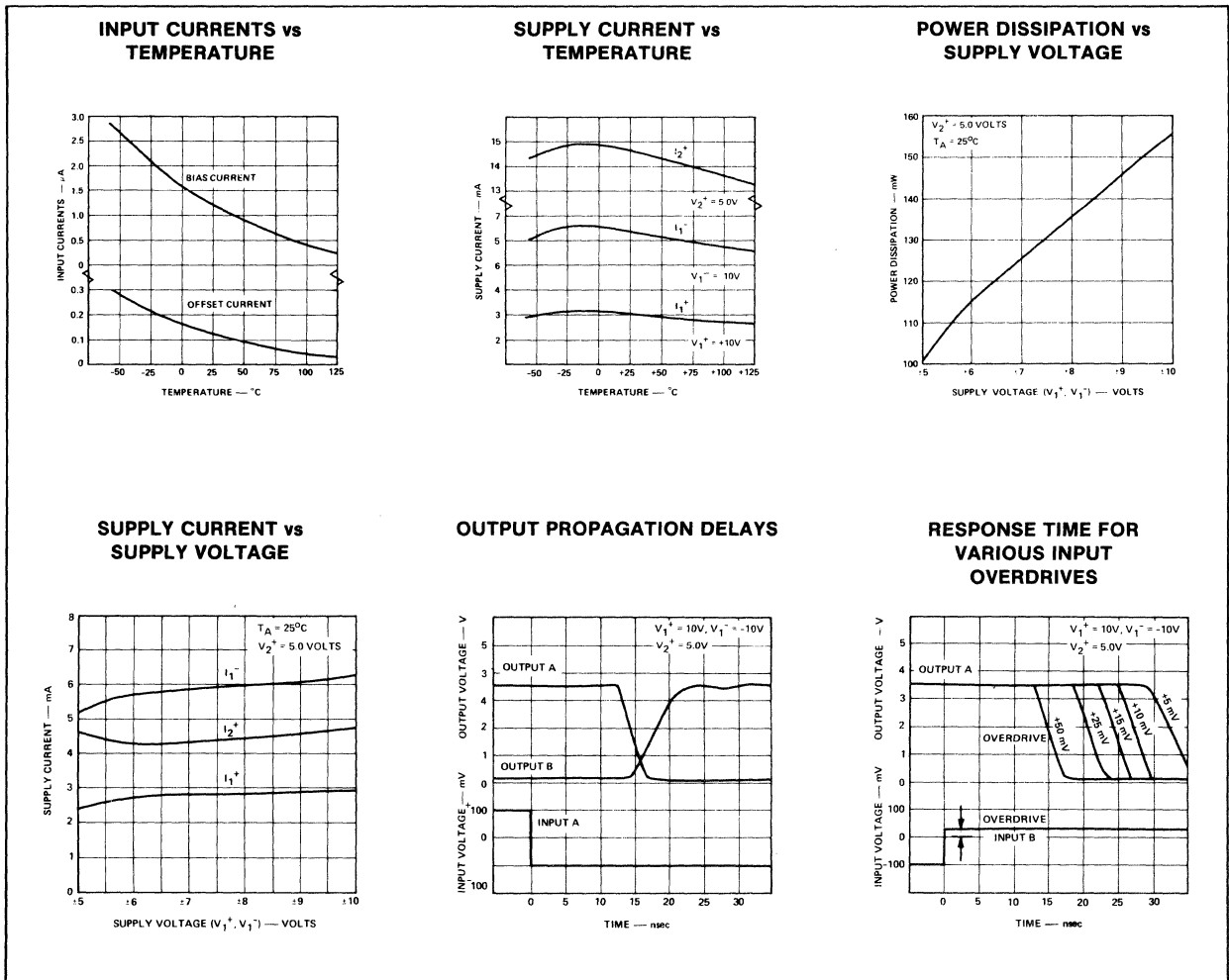
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time t_{PLH} t_{PHL}	$V_{IN} = \pm 100\text{mV}$ step		16	26	ns
			14	24	ns
Delay between output A and B			2	5	ns
Strobe delay time t_{on} Turn-on time t_{off} Turn-off time			6		ns
			6		ns



TYPICAL PERFORMANCE CHARACTERISTICS

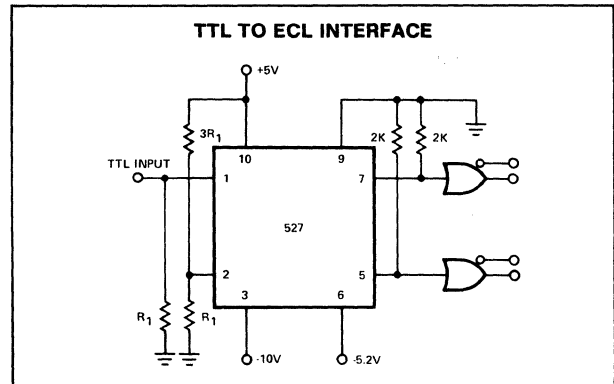
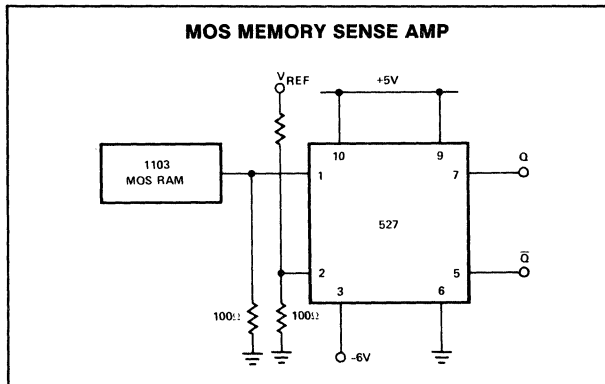
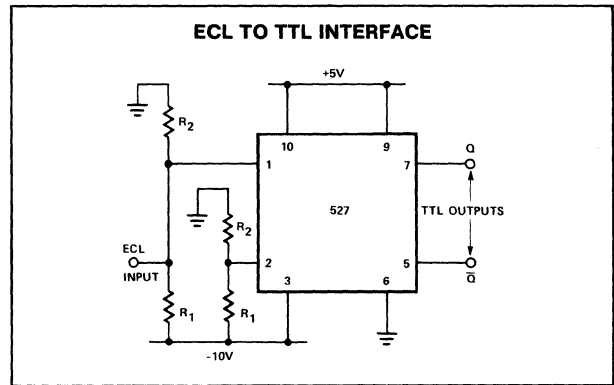
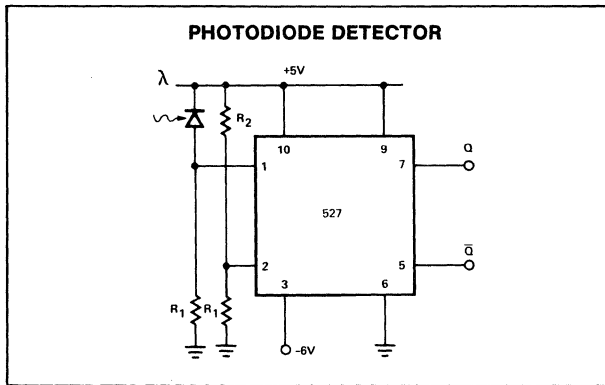


APPLICATIONS

One of the main features of the device is that supply voltages (V_{1+} , V_{1-}) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_{1-}) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_{1+} and V_{1-}) up to a maximum of ± 6 volts as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS



DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

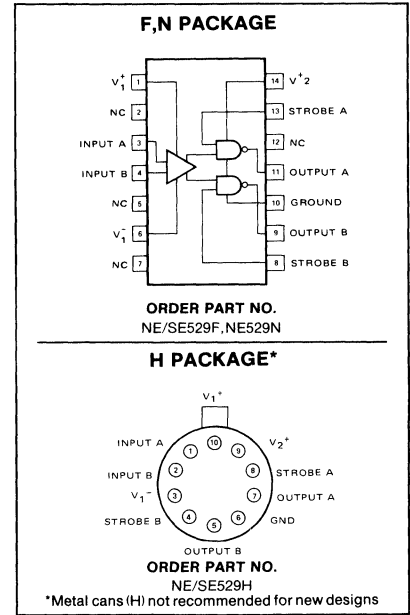
FEATURES

- 10ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range

APPLICATIONS

- A/D conversion
- ECL to TTL interface
- TTL to ECL interface
- Memory sensing
- Optical data coupling
- Mil std 883A,B,C available

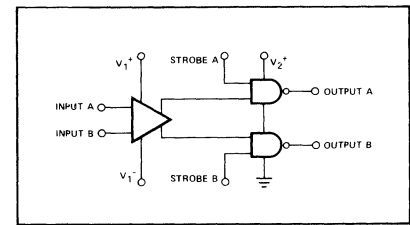
PIN CONFIGURATION



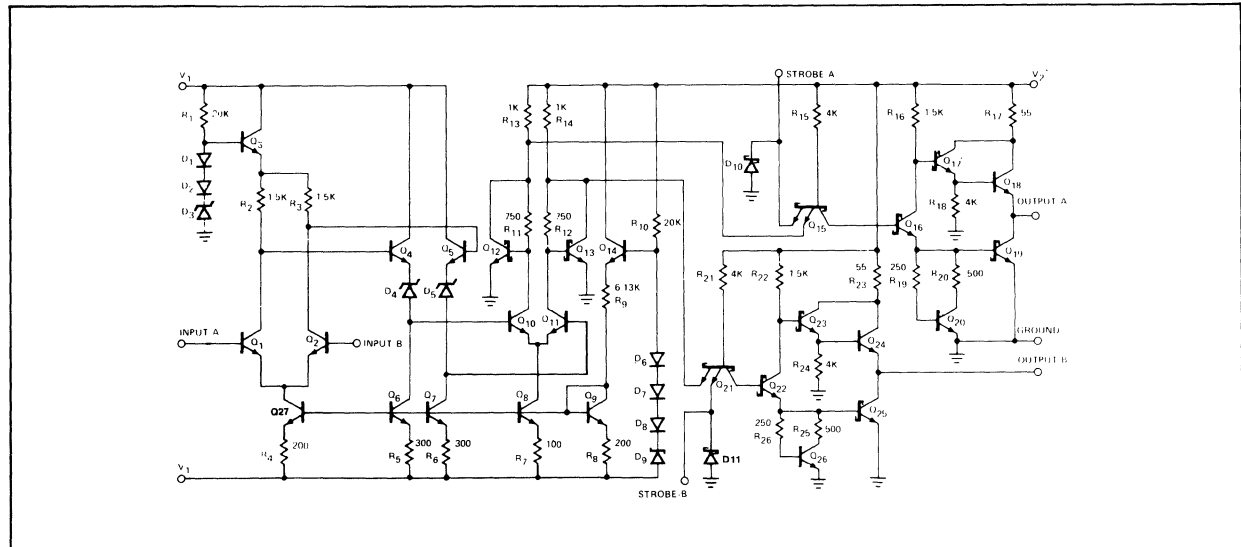
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V_{1+} = +10V, V_{2+} = +5.0V, V_{1-} = -10V$

PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT	
		Min	Typ	Max	Min	Typ	Max		
INPUT CHARACTERISTICS Input offset voltage @25°C Over temperature range				4 6			6 10	mV mV	
			5	12 36		5	20 50	μA μA	
Input bias current @25°C Over temperature range	$V_{IN} = 0V$		2	3 9		2	5 15	μA μA	
GATE CHARACTERISTICS Output voltage "1" state "0" state	$V_{2+} = 4.75V, I_{source} = -1mA$ $V_{2+} = 4.75V, I_{sink} = 10mA$	2.5	3.3		2.7	3.3		V V	
				0.5			0.5		
Strobe inputs "0" input current "1" input current @25°C Over temperature range "0" input voltage "1" input voltage	$V_{2+} = 5.25V, V_{strobe} = 0.5V$ $V_{2+} = 5.25V, V_{strobe} = 2.7V$ $V_{2+} = 5.25V, V_{strobe} = 2.7V$ $V_{2+} = 4.75V$ $V_{2+} = 4.75V$			-2 50 200 0.8			-2 100 200 0.8	mA μA μA V V	
		2.0			2.0				
Short circuit Output current	$V_{2+} = 5.25V, V_{OUT} = 0V$	-18		-70	-18		-70	mA	
POWER SUPPLY REQUIREMENTS Supply voltage V_{1+} V_{1-} V_{2+}		5		10	5		10	V V V	
		-6		-10	-6		-10		
		4.5	5	5.5	4.75	5	5.25		
Supply current I_{1+} I_{1-} I_{2+}	$V_{1+} = 10V, V_{1-} = -10V$ $V_{2+} = 5.25V$ Over temp. Over temp. Over temp.			5 10 20			5 10 20	mA mA mA	

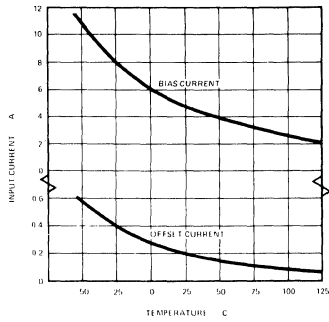
Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$

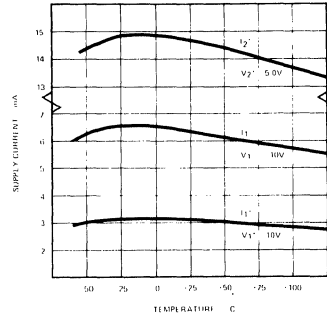
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response Propagation delay time t_{PLH} t_{PHL}	$V_{IN} = \pm 100mV$ step		12	22	ns
			10	20	ns
			2	5	ns
Delay between output A and B					ns
Strobe delay time t_{ON} turn-on time t_{OFF} turn-off time			6 6		ns ns

TYPICAL PERFORMANCE CHARACTERISTICS

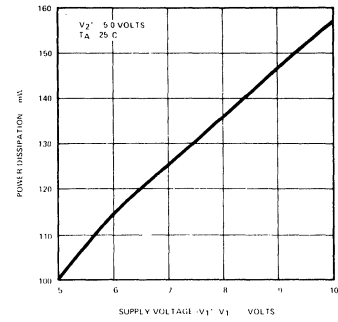
INPUT CURRENTS vs TEMPERATURE



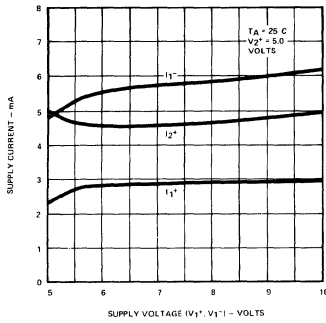
SUPPLY CURRENT vs TEMPERATURE



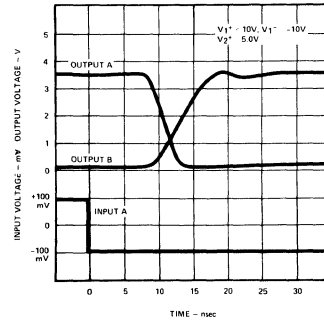
POWER DISSIPATION vs SUPPLY VOLTAGE



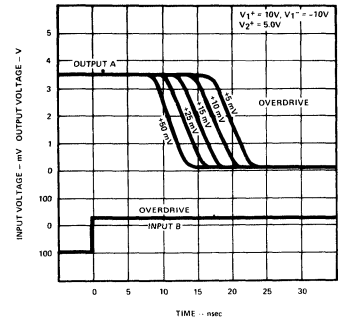
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



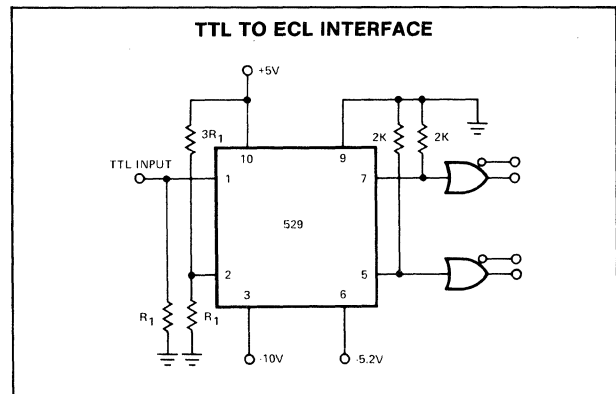
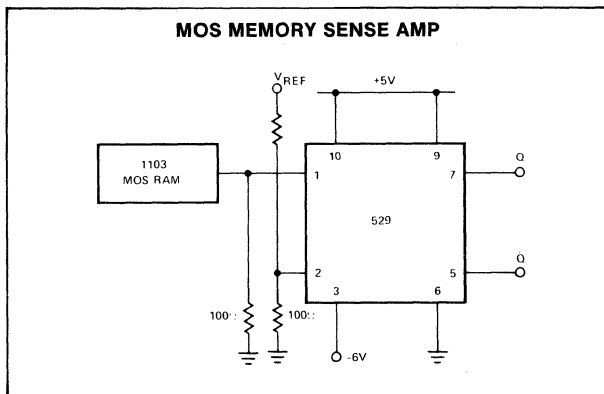
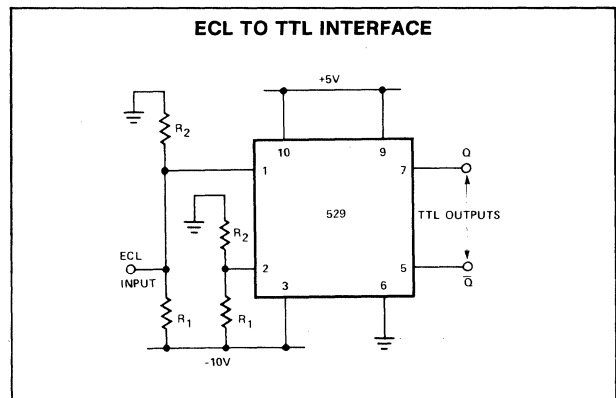
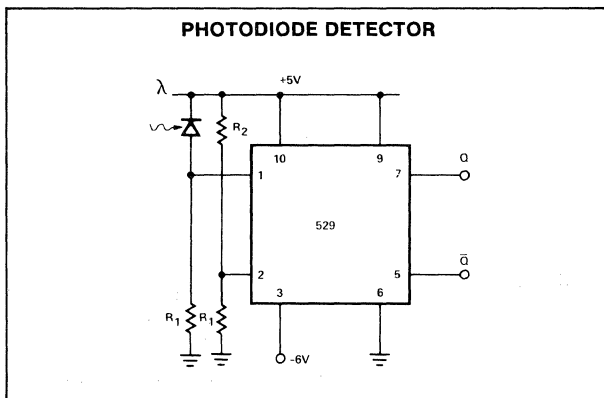
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APPLICATIONS

One of the main features of the device is that supply voltages (V_{1+} , V_{1-}) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_{1-}) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_{1+} and V_{1-}) up to a maximum of ± 6 volts as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS



SECTION 6

MICROPROCESSOR

INTERFACE

Section 6—MICROPROCESSOR INTERFACE

NE590/591 Addressable Peripheral Drivers225

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a \overline{CE} input line which also serves the function of further address decoding. A common clear input, \overline{CLR} , turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S . This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

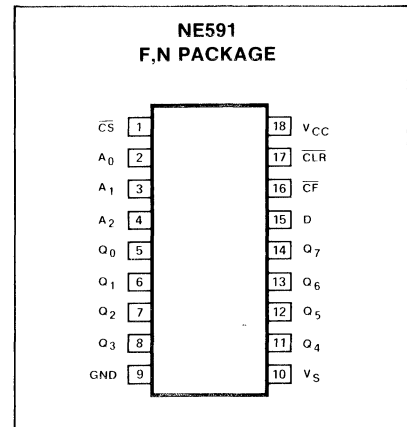
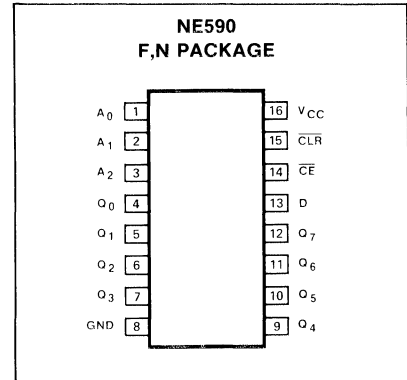
FEATURES

- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 9334

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATIONS



PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A ₀ -A ₂	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q ₀ -Q ₇	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	\overline{CE}	The chip enable. When this input is low, the output latches will accept data. When \overline{CE} goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	\overline{CLR}	The clear input. When \overline{CLR} goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, \overline{CLR} low will override any other condition.
—	1	\overline{CS}	The chip select input provides for an additional level of address decoding.
—	10	V _S	The V _S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V _{CC} or another supply.



TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
CLR	CE	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q _{N-1} →							Memory	
H	L	L	L	L	L	H	Q _{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q _{N-1} →							
H	L	L	H	L	L	Q _{N-1}	H	Q _{N-1} →						
H	L	H	H	L	L	Q _{N-1}	L	Q _{N-1} →						
H	L	L	H	H	H	Q _{N-1}	→ H							
H	L	H	H	H	H	Q _{N-1}	→ L							

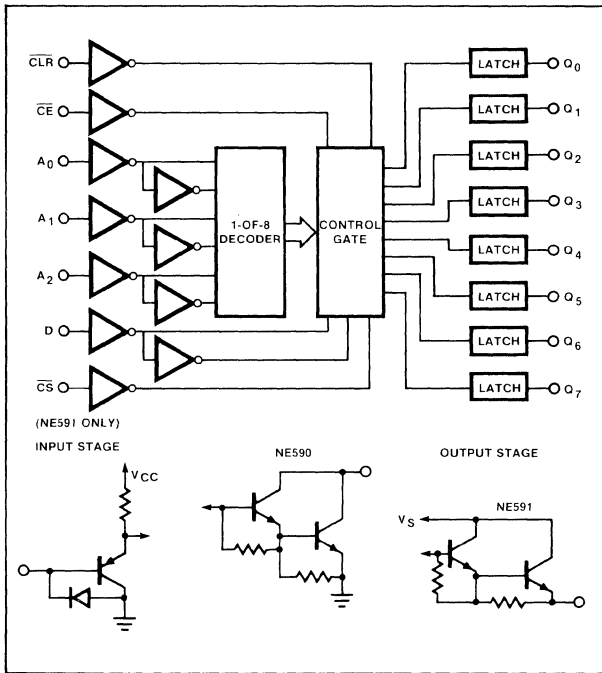
X = Don't care condition
 Q_{N-1} = Previous output state
 L = Low voltage level/"ON" output state
 H = High voltage level/"OFF" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
CLR	CE	CS	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q _{N-1} →							Memory	
H	H	L	X	X	X	X	Q _{N-1} →								
H	L	H	X	X	X	X	Q _{N-1} →								
H	L	L	L	L	L	L	L	Q _{N-1} →							Addressable Latch
H	L	L	H	L	L	L	H	Q _{N-1} →							
H	L	L	L	H	L	L	Q _{N-1}	L	Q _{N-1} →						
H	L	L	H	H	L	L	Q _{N-1}	H	Q _{N-1} →						
H	L	L	L	H	H	H	Q _{N-1} →						L		
H	L	L	H	H	H	H	Q _{N-1} →						H		

X = Don't care
 Q_{N-1} = Previous output state
 L = Low voltage level/"OFF" output state
 H = High voltage level/"ON" output state

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	-0.5 to +7	V
V_{IN} Input voltage	-0.5 to +15	V
V_{OUT} Output voltage		V
	NE590	0 to +7
	NE591	0 to V_{CC}
V_S Source bus voltage		V
	NE591 only	-0.5 to +7
$V_S - V_{CC}$ Source/supply differential voltage		V
	NE591 only	-5 to +2
I_{OUT} Output current		mA
	Each output	300
	All outputs	1000
P_D Power dissipation ¹		W
	Temperature range	1
T_A Ambient		$^\circ\text{C}$
T_J Junction	0 to +70	
T_{STG} Storage	150	
T_{sold} Lead soldering temperature (10sec max)	-65 to +150	$^\circ\text{C}$
	300	

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75$ to 5.25V , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ unless otherwise specified.^{2,3}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IH} Input voltage High		2.0			V
V_{IL} Input voltage Low				0.8	V
V_{OL} Output voltage Low (NE590 only)	$I_{OL} = 250\text{mA}$, $T_A = 25^\circ\text{C}$		1.0	1.3	V
V_{OH} Output voltage High (NE591 only)	Over temperature $I_{OH} = -250\text{mA}$, $V_{CC} = V_S = 5\text{V}$	2.9		1.5	V
I_{IH} Input current High	$V_{in} = V_{CC}$		0.1	10	μA
I_{IL} Input current Low	$V_{in} = 0\text{V}$		-25	-60	μA
I_{CCL} Supply current ⁴ All outputs low	$V_S = V_{CC} = 5\text{V}$				mA
	NE590		33	50	
	NE591		15	50	
I_{CCH} Supply current ⁴ All outputs high	$V_S = V_{CC} = 5\text{V}$				mA
	NE590		15	50	
	NE591		30	50	

NOTES

- Derate power dissipation as indicated above threshold ambient temperature:
 NE590N at $95^\circ\text{C}/\text{W}$ above 55°C
 NE590F at $100^\circ\text{C}/\text{W}$ above 50°C
 NE591N at $90^\circ\text{C}/\text{W}$ above 60°C
 NE591F at $93^\circ\text{C}/\text{W}$ above 57°C
- All typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
- For the NE591, $V_S = V_{CC}$ in all tests.
- Supply current for the NE591 is measured with no output load.

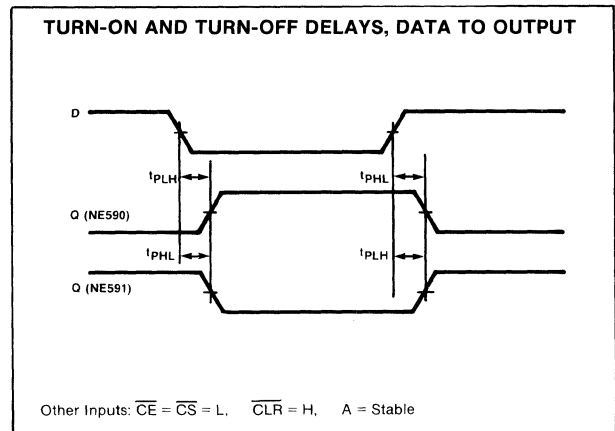
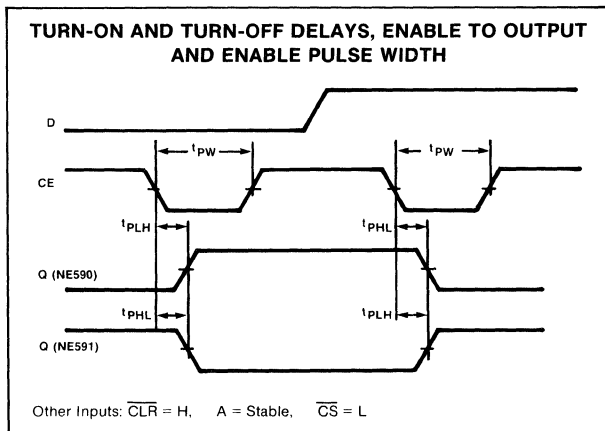
SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TO	FROM	NE590			NE591			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation delay time Low to high ⁵ High to low ⁵	Output	\overline{CE}	100 130			70 80		ns
t_{PLH} t_{PHL}	Low to high ⁶ High to low ⁶	Output	Data	80 100			60 70		
t_{PLH} t_{PHL}	Low to high ⁷ High to low ⁷	Output	Address	125 115			70 70		
t_{PLH} t_{PHL}	Low to high ⁸ High to low ⁸	Output	\overline{CLR}	80			60		
t_{PLH} t_{PHL}	Low to high ⁵ High to low ⁵	Output	\overline{CS}				70 80		
SWITCHING SET-UP REQUIREMENTS									
$t_{s(H)}^9$ $t_{s(L)}^9$	Chip enable Chip enable	High data Low data		120 120			50 70		ns ns
$t_{s(A)}^{10}$	Chip enable	Address		-60			-10		ns
$t_{h(H)}^9$ $t_{h(L)}^9$	Chip enable Chip enable	High data Low data		-60 -60			-60 -20		ns ns
$t_{s(CS)}^9$	Chip enable	Low chip select					70		ns
$t_{pw(E)}$	Chip enable pulse width ⁵			150			80		ns

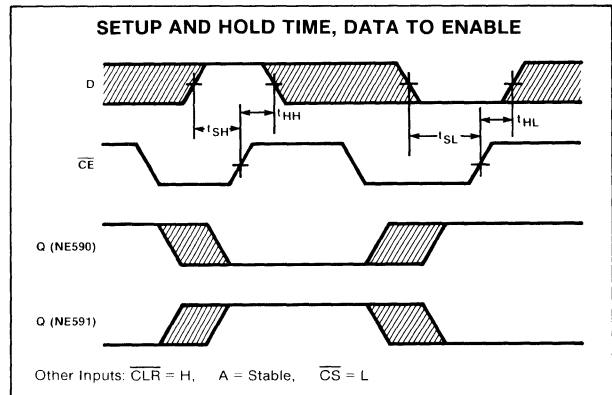
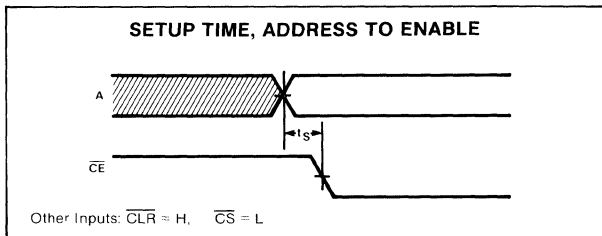
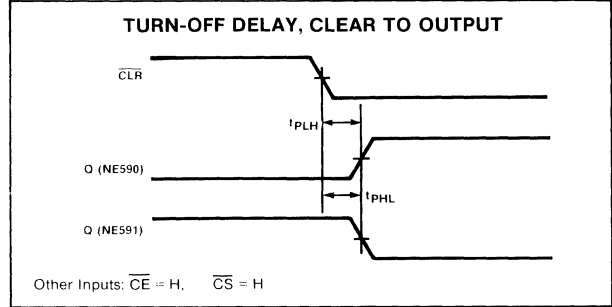
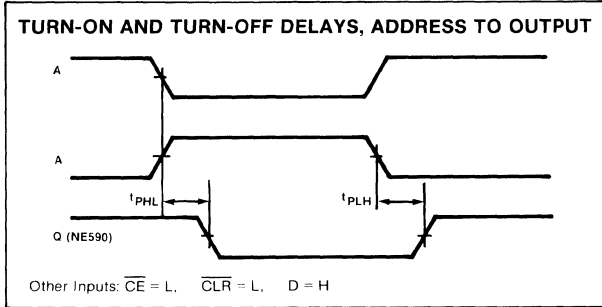
NOTES

5. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8. See Turn-Off Delay, Clear to Output timing diagram.
9. See Setup and Hold Time, Data to Enable timing diagram.
10. See Setup Time, Address to Enable timing diagram.

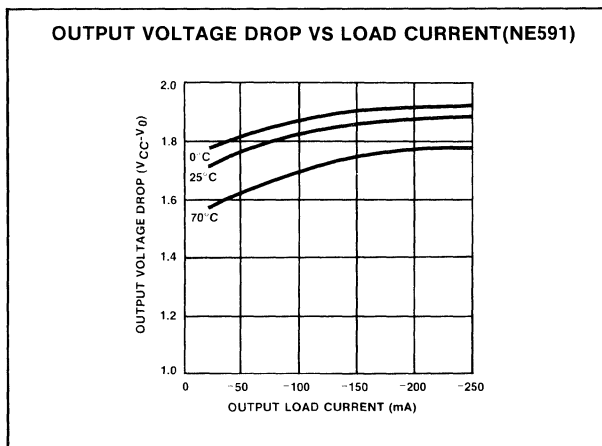
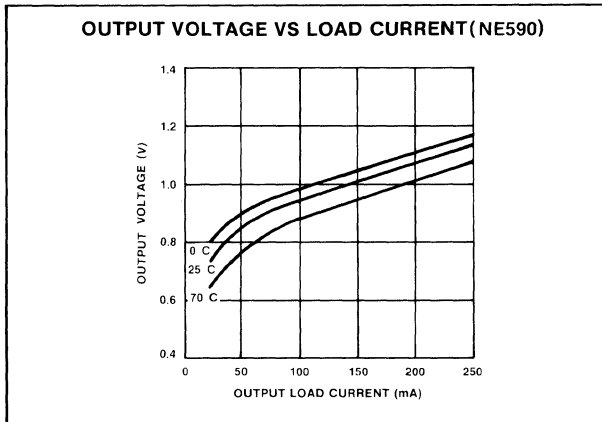
TIMING DIAGRAMS



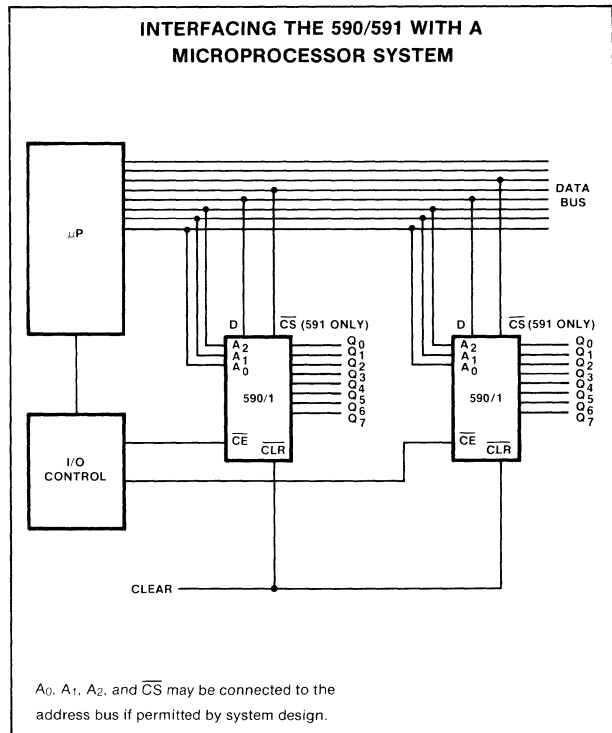
TIMING DIAGRAMS (Cont'd)



TYPICAL PERFORMANCE CHARACTERISTICS

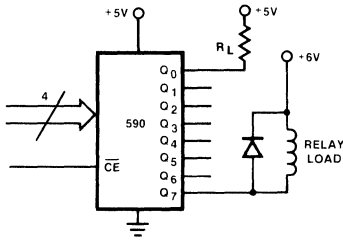


TYPICAL APPLICATIONS

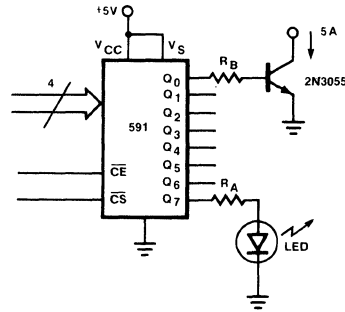


TYPICAL APPLICATIONS (Cont'd)

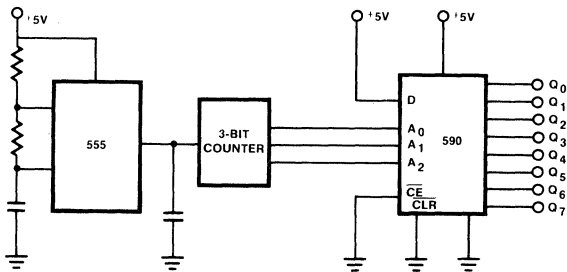
NE590 DRIVING SIMPLE LOADS



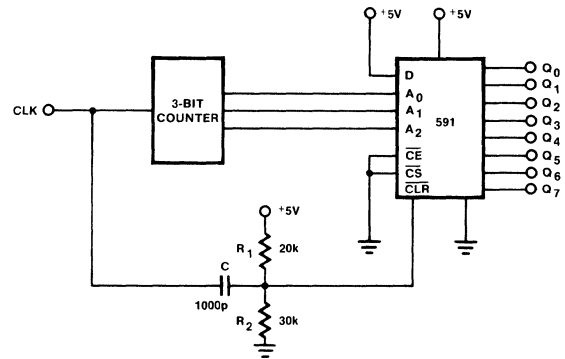
NE591 DRIVING SIMPLE LOADS



NE590 OPERATING IN DEMULTIPLEX MODE

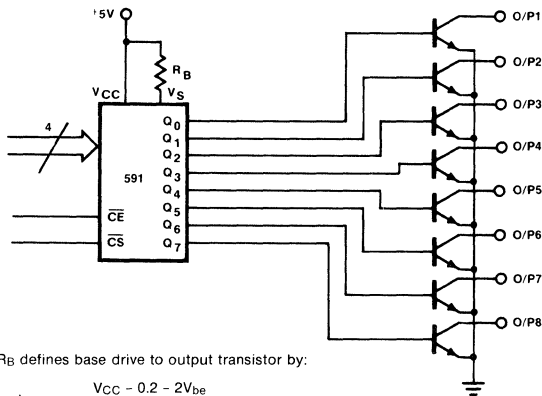


NE591 OPERATING IN DEMULTIPLEX MODE



For display applications, interdigit blanking is provided by time constant $\tau = C(R_1/R_2) \approx 10\mu s$ with values shown.

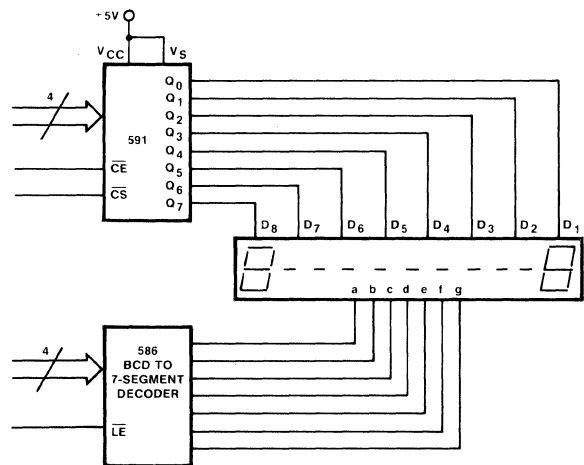
NE591 DRIVING HIGH CURRENT (5A) TRANSISTORS



R_B defines base drive to output transistor by:

$$I_b = \frac{V_{CC} - 0.2 - 2V_{be}}{R_B}$$
 provided that only one output is ON at any time.

NE591 AS THE DIGIT DRIVER IN A LED DISPLAY SYSTEM



SECTION 7

TRANSISTOR ARRAYS

Section 7—TRANSISTOR ARRAYS

CA3081/3082	Seven Transistor Array	233
ULN2001/2003/2004	High Voltage/High Current Darlington Transistor Arrays	236

DESCRIPTION

The CA3081 and CA3082 are monolithic integrated circuits, each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads of up to 100mA. At the same time, the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small-signal applications. In the CA3081, the transistors are connected in a common emitter configuration, while in the CA3082, the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays, as well as for general purpose applications. The CA3081 and CA3082 are available in both 16-lead dual-in-line plastic and cerdip packages.

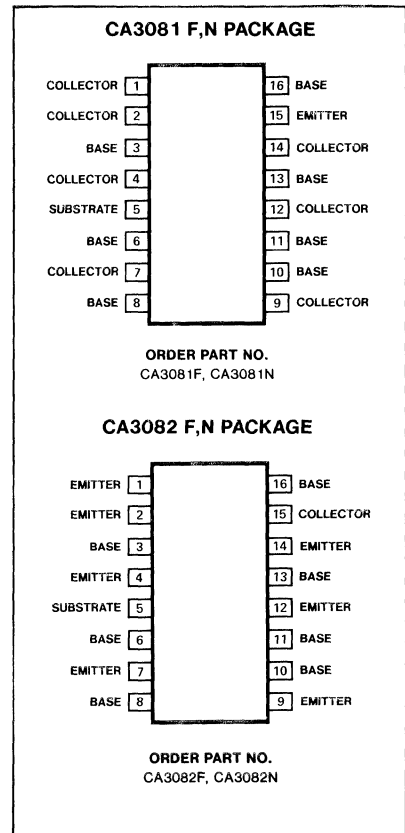
FEATURES

- Seven transistors permit a wide range of applications in either a common emitter (CA3081) or common-collector (CA3082) configuration.
- High I_C : 100mA maximum
- Low $V_{CE\ sat}$ (at 50mA): 0.4V typical

APPLICATIONS

- Drivers for:
Incandescent display devices
LED
Relay control
Thyristor firing

PIN CONFIGURATIONS



PIN DESIGNATION (CA3081)

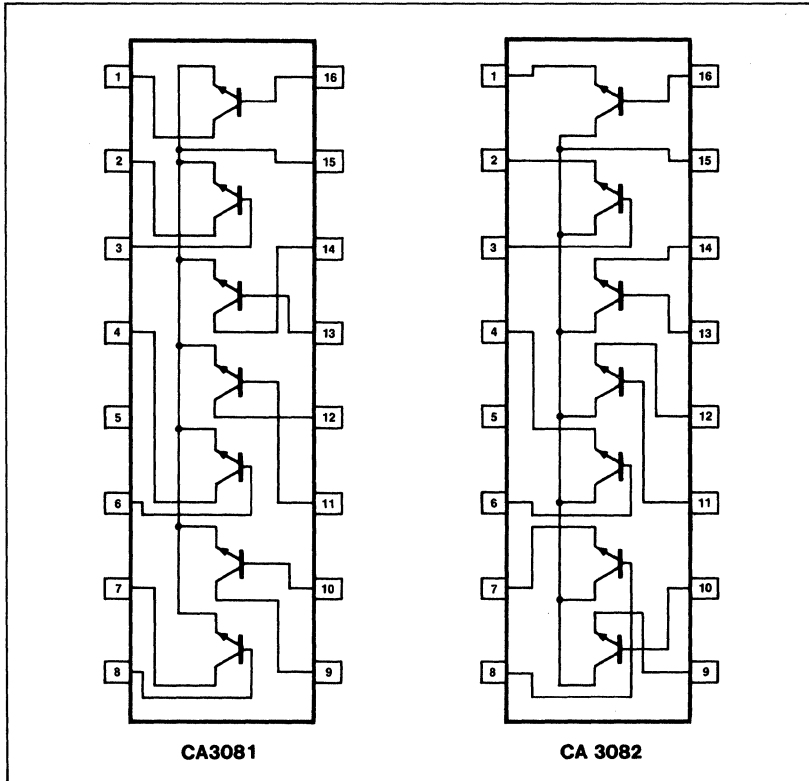
PIN NO.	SYMBOL	NAME AND FUNCTION
1	C1	Collector, Transistor 1
2	C2	Collector, Transistor 2
3	B2	Base, Transistor 2
4	C5	Collector, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	C7	Collector, Transistor 7
8	B7	Base, Transistor 7
9	C6	Collector, Transistor 6
10	B6	Base, Transistor 6
11	B4	Base, Transistor 4
12	C4	Collector, Transistor 4
13	B3	Base, Transistor 3
14	C3	Collector, Transistor 3
15	E	Common emitter
16	B1	Base, Transistor 1

PIN DESIGNATION (CA3082)

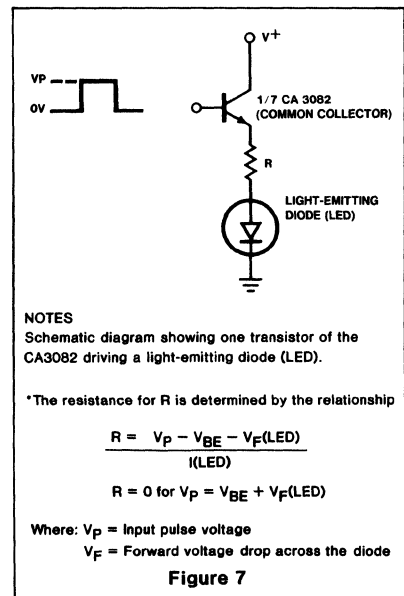
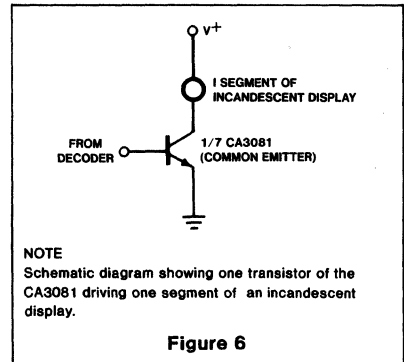
PIN	SYMBOL	NAME AND FUNCTION
1	E1	Emitter, Transistor 1
2	E2	Emitter, Transistor 2
3	B2	Base, Transistor 2
4	E5	Emitter, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	E6	Emitter, Transistor 6
8	B6	Base, Transistor 6
9	E7	Emitter, Transistor 7
10	B7	Base, Transistor 7
11	B4	Base, Transistor 4
12	E4	Emitter, Transistor 4
13	B3	Base, Transistor 3
14	E3	Emitter, Transistor 3
15	C	Common collector
16	B1	Base, Transistor 1



BLOCK DIAGRAM



TYPICAL READ-OUT DRIVER APPLICATIONS



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$

PARAMETER	RATING	UNIT	
P	Power dissipation: Any one transistor	500 750	mW mW
PTOT	Total package Above 55°C	Derate Linearly 6.67	mW/°C
TA	Ambient temperature range: Operating	-55 to +125	°C
Tstg	Storage	-65 to +150	°C
	Lead temperature (10 seconds)	265	°C
VCEO	Collector to emitter voltage ¹	16	V
VCBO	Collector to base voltage ¹	20	V
VCIO	Collector to substrate voltage ^{1,2}	20	V
VEBO	Emitter to base voltage ¹	5	V
IC	Collector current ¹	100	mA
IB	Base current ¹	20	mA

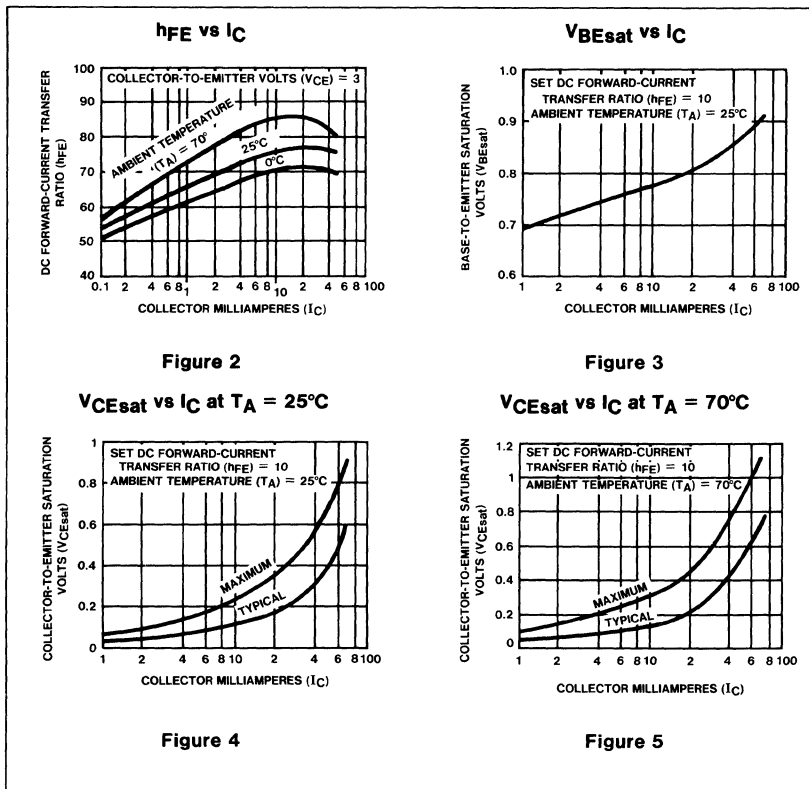
NOTES

1. Ratings apply for each transistor in the device.
2. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC ELECTRICAL CHARACTERISTICS FOR EACH TRANSISTOR $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ	Max		
V_{CBO} (BR)	Collector to base breakdown voltage	20	60		V	
V_{CIO} (BR)	Collector to substrate breakdown voltage					
V_{CEO} (BR)	Collector to emitter breakdown voltage	20	60		V	
V_{EBO} (BR)	Emitter to base breakdown voltage	16	24		V	
		5	6.9		V	
h_{FE}	DC forward current Transfer Ratio	$V_{CE} = 0.5\text{V}, I_C = 30\text{mA}$	30	68		
		$V_{CE} = 0.8\text{V}, I_C = 50\text{mA}$	40	70		
$V_{BE\text{ sat}}$	Base to emitter saturation voltage	$I_C = 30\text{mA}, I_B = 1\text{mA}$		0.87	1.0	V
$V_{CE\text{ sat}}$	Collector to emitter saturation voltage	CA3081 / CA3082				
		CA3081		0.27	0.5	V
		CA3082		0.4	0.7	V
		CA3082		0.4	0.8	V
I_{CEO}	Collector cutoff current	$V_{CE} = 10\text{V}, I_B = 0$			10	μA
I_{CBO}	Collector cutoff current	$V_{CB} = 10\text{V}, I_E = 0$			1	μA

TYPICAL PERFORMANCE CHARACTERISTICS



DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2001 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN-2003.

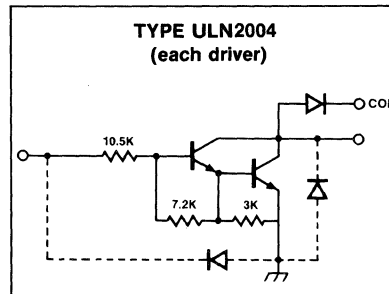
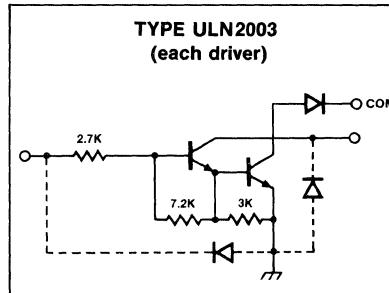
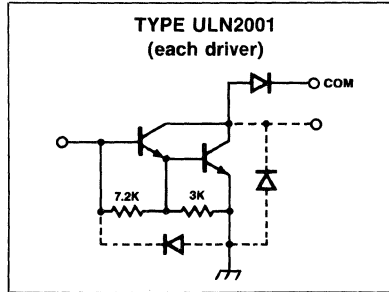
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

FEATURES

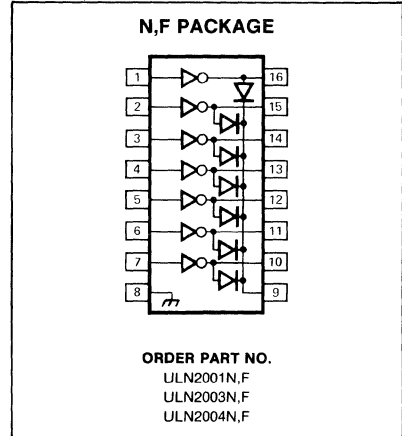
- Peak inrush current 600mA
- Protected internally against inductive loads
- Open collector topology
- Compatible with most logic technologies

ABSOLUTE MAXIMUM RATINGS

EQUIVALENT SCHEMATICS



PIN CONFIGURATION



at 25°C Free-Air temperature for any one Darlington pair unless otherwise specified.

PARAMETER	RATING	UNIT
V _{CE} Output voltage	50	V
V _{IN} Input voltage	30	V
V _{EBO} Emitter base voltage	6	V
I _C Continuous collector current	500	mA
I _B Continuous base current	25	mA
P _D Power dissipation	1.3	W
Derating factor above 25°C	95	°C/W
T _A Ambient temperature range (operating)	0 to +85	°C
T _S Storage temperature range	-65 to +150	°C

*NOTE
Under normal operating conditions, these units will sustain 350mA per output with V_{CE(SAT)} = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.1,2,3

PARAMETER	TEST CONDITIONS	Test Fig.	LIMITS			UNIT
			Min	Typ	Max	
I _{CEX} Output leakage current Type ULN-2004	V _{CE} = 50V, T _A = 70°C V _{CE} = 50V, T _A = 70°C, V _{IN} = 1V	1A	—	—	100	μA
		1B	—	—	500	μA
V _{CE(SAT)} Collector-emitter Saturation voltage	I _C = 350mA, I _B = 500μA I _C = 200mA, I _B = 350μA I _C = 100mA, I _B = 250μA	2	—	1.25	1.6	V
		2	—	1.1	1.3	V
		2	—	0.9	1.1	V
I _{IN(ON)} Input current Type ULN-2003 Type ULN-2004	V _{IN} = 3.85V V _{IN} = 5V V _{IN} = 12V	3	—	0.93	1.35	mA
		3	—	0.35	0.5	mA
		3	—	1.0	1.45	mA
I _{IN(OFF)} Input current	I _C = 500μA, T _A = 70°C	4	50	65	—	μA
V _{IN(ON)} Input voltage Type ULN-2003 Type ULN-2004	V _{CE} = 2V, I _C = 200mA V _{CE} = 2V, I _C = 250mA V _{CE} = 2V, I _C = 300mA	5	—	—	2.4	V
		5	—	—	2.7	V
		5	—	—	3.0	V
	V _{CE} = 2V, I _C = 125mA V _{CE} = 2V, I _C = 200mA V _{CE} = 2V, I _C = 275mA V _{CE} = 2V, I _C = 350mA	5	—	—	5.0	V
		5	—	—	6.0	V
		5	—	—	7.0	V
5	—	—	8.0	V		
h _{FE} D-C forward current transfer ratio Type ULN-2001	V _{CE} = 2V, I _C = 350mA	2	1000	—	—	—
C _{IN} Input capacitance		—	—	15	30	pF
I _R Clamp diode leakage current	V _R = 50V	6	—	—	50	μA
V _F Clamp diode forward voltage	I _F = 350mA	7	—	1.7	2	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The I_{IN(OFF)} current limit guarantees against partial turn-on of the output.
3. The V_{IN(ON)} voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.1,2,3

PARAMETER	TEST CONDITIONS	Test Fig.	LIMITS			UNIT
			Min	Typ	Max	
t _{PLH} Turn-on delay	0.5 E _{IN} to 0.5 E _{OUT}	—	—	1.0	5	μs
t _{PHL} Turn-off delay	0.5 E _{IN} to 0.5 E _{OUT}	—	—	1.0	5	μs

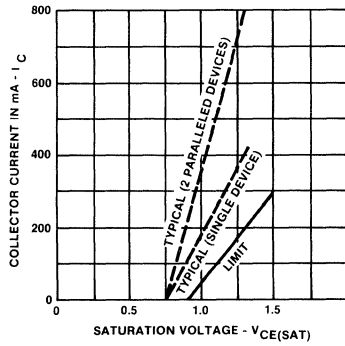
NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The I_{IN(OFF)} current limit guarantees against partial turn-on of the output.
3. The V_{IN(ON)} voltage limit guarantees a minimum output sink current per the specified test conditions.

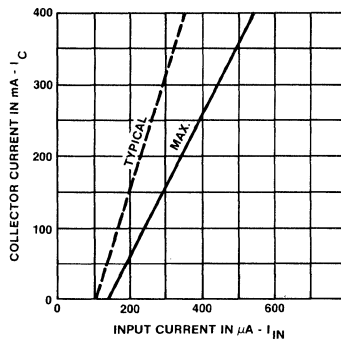


TYPICAL PERFORMANCE CHARACTERISTICS

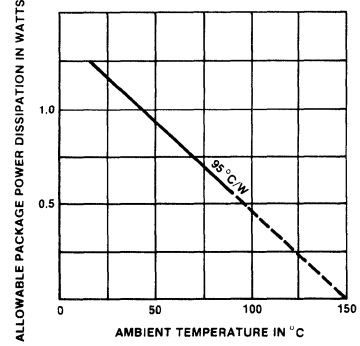
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



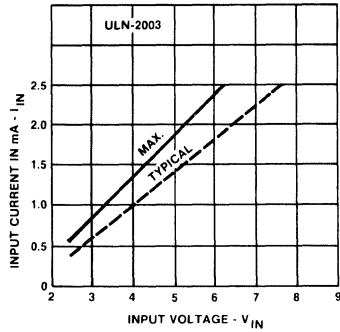
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



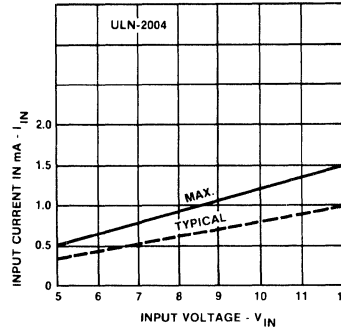
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



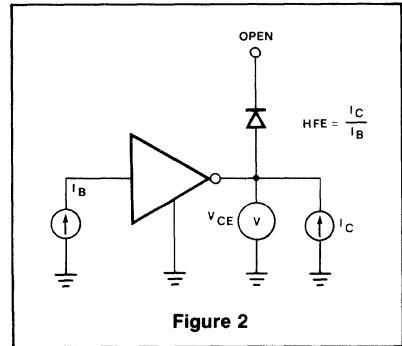
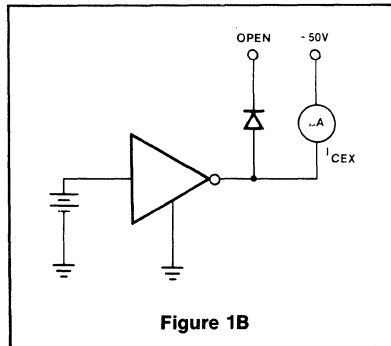
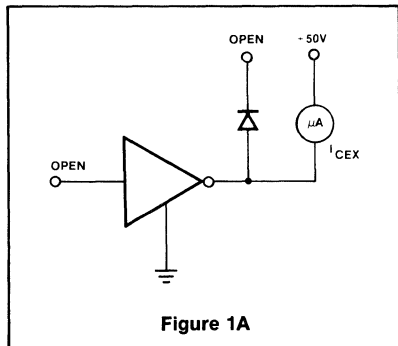
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004



TEST FIGURES



TEST FIGURES (Cont'd)

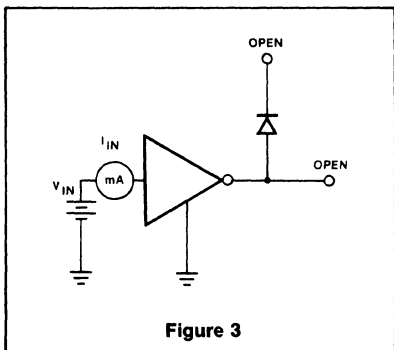


Figure 3

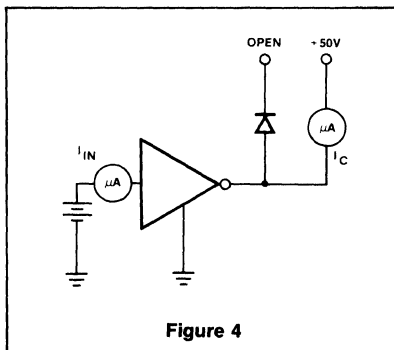


Figure 4

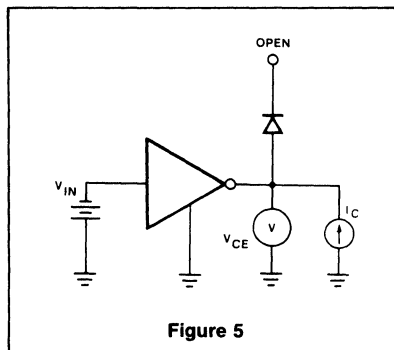


Figure 5

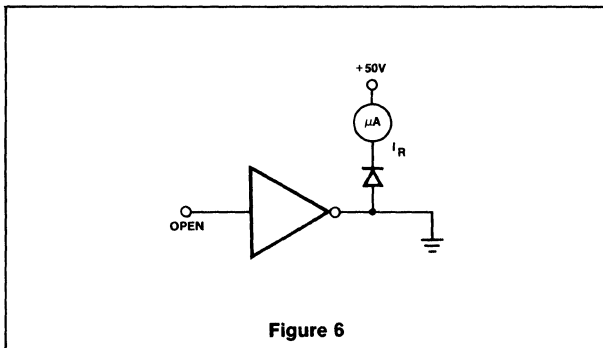


Figure 6

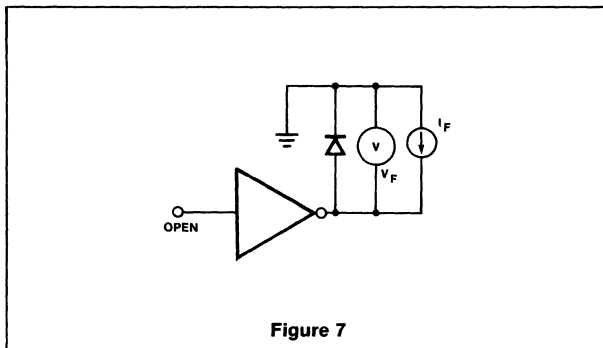
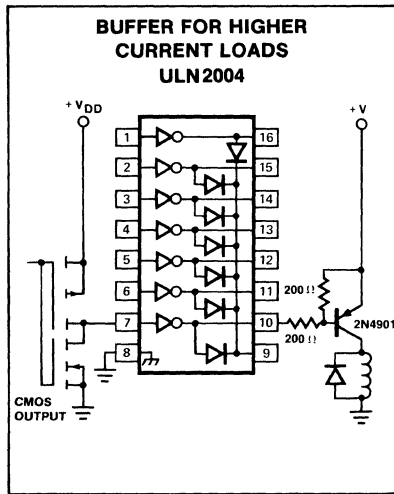
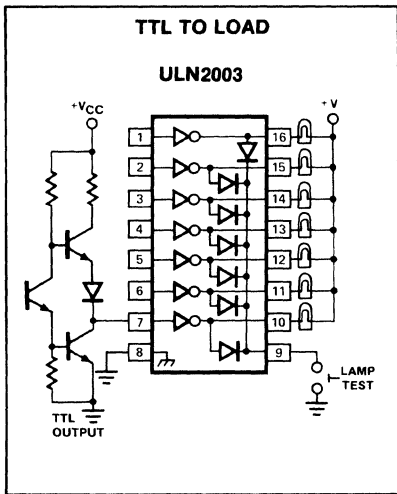


Figure 7

7

TYPICAL APPLICATIONS



SECTION 8 INTERFACE

Section 8—INTERFACE

DS7820/8820	Dual Line Receiver	243
DS7820A/8820A	Dual Line Receiver	245
DS7830/8830	Dual Differential Line Driver	249
MC1488	Quad Line Driver	251
MC1489/1489A	Quad Line Receivers	254
75S107	High Speed Dual Line Receiver	256
75S108	High Speed Dual Line Receiver	259
75S207	High Speed Dual Sense Amplifier for MOS Memories	263
75S208	High Speed Dual Sense Amplifier for MOS Memories	266

DESCRIPTION

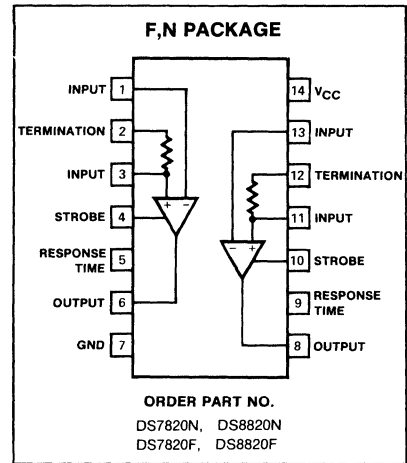
The DS7820, specified from -55°C to 125°C, and the DS8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

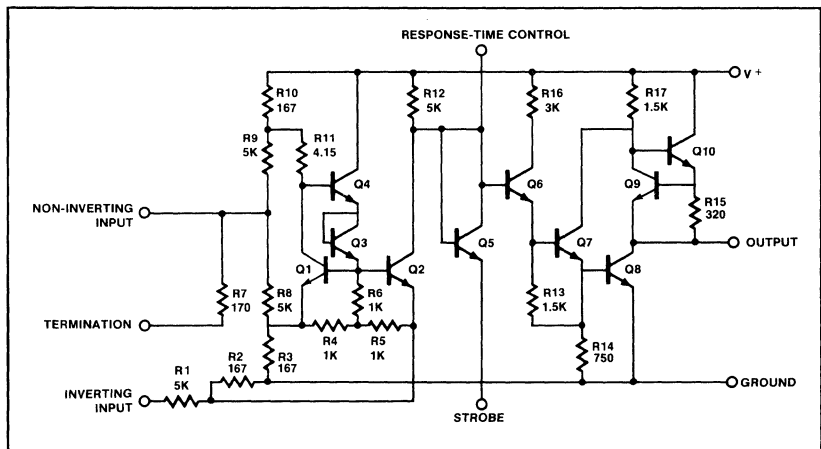
FEATURES

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Independent channel strobing
- High input resistance
- Fanout of two with DTL or TTL
- Output can be wire OR'ed
- DS7820 Mil std 883A,B,C available

PIN CONFIGURATION



CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	25	mA
Power dissipation	600	mW
Operating temperature range		
DS7820	-55 to +125	°C
DS8820	0 to 70	°C
Lead temperature (soldering, 10sec)	300	°C

NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.



DC ELECTRICAL CHARACTERISTICS

Specifications apply for $4.5V \leq V_{CC} \leq 5.5$,
 $-15V \leq V_{CM} \leq 15V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ for the DS7820
 or $0^\circ C \leq T_A \leq +70^\circ C$ for the DS8820 unless otherwise specified.
 Typical values given are for $V_{CC} = 5.0V$, $T_A = 25^\circ C$ and $V_{CM} = 0V$
 unless stated differently.^{1,2,3}

PARAMETER	TEST CONDITIONS	DS7820			DS8820			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{TH}	Input threshold	-0.5	0	0.5	-0.5	0	0.5	V
V _{TH}	Input threshold	-1.0	0	1.0	-1.0	0	1.0	V
V _{OH}	High output level	2.5		5.5	2.5		5.5	V
V _{OL}	Low output level	0		0.4	0		0.4	V
R _{IN -}	Inverting input resistance	3.6	5.0		3.6	5.0		kΩ
R _{IN +}	Noninverting input resistance	1.8	2.5		1.8	2.5		kΩ
R _T	Line termination resistance	120	170	250	120	170	250	Ω
I _{ST}	Strobe current		1.0	1.4		1.0	1.4	mA
I _{ST}	Strobe current			-5			-5	μA
I _{CC}	Supply current ³		3.2	6.0		3.2	6.0	mA
I _{CC}	Supply current ³		5.8	10.2		5.8	10.2	mA
I _{CC}	Supply current ³		8.3	15.0		8.3	15.0	mA
I _{IN +}	Noninverting input current		3.0	7.0		5.0	7.0	mA
I _{IN +}	Noninverting input current	-1.6	-1.0		-1.6	-1.0		mA
I _{IN +}	Noninverting input current	-9.8	-7.0		-9.8	-7.0		mA
I _{IN -}	Inverting input current		3.0	4.2		3.0	4.2	mA
I _{IN -}	Inverting input current		0	-0.5		0	-0.5	mA
I _{IN -}	Inverting input current	-4.2	-3.0		-4.2	-3.0		mA

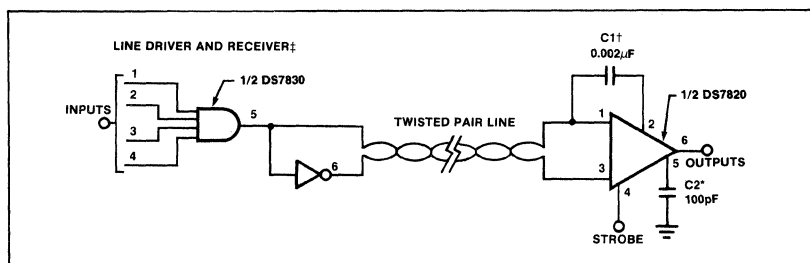
NOTES

- All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
- Only one output at a time should be shorted.
- The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	DS7820			DS8820			UNIT
		Min	Typ	Max	Min	Typ	Max	
T _R	Response time C _{delay} = 0		40			40		ns
T _R	Response time C _{delay} = 100pF		150			150		ns

DS7820-DS8820 TYPICAL APPLICATION



†Exact value depends on line length
 ‡V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830
 *Optional to control response time

DESCRIPTION

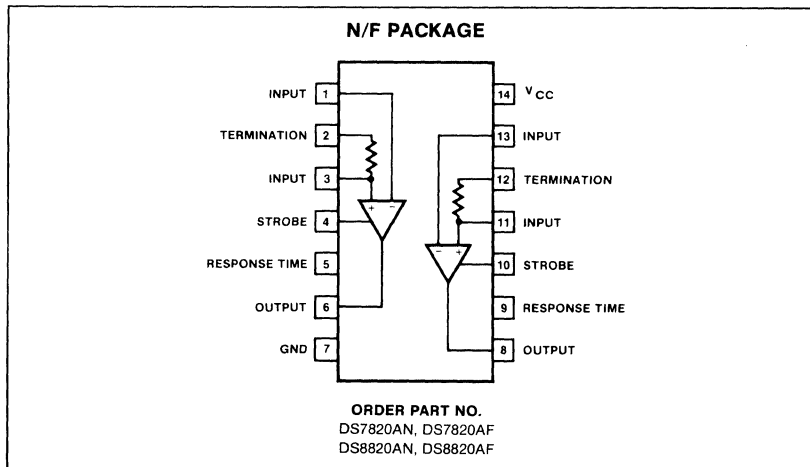
The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (-55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

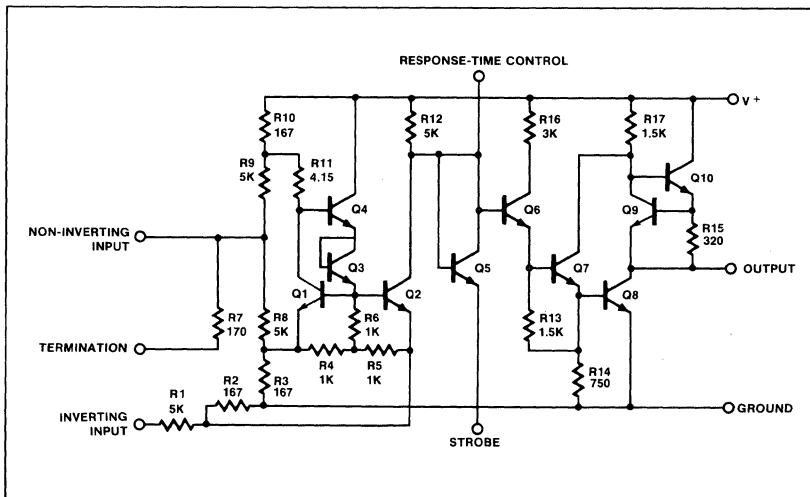
FEATURES

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	50	mA
Power dissipation	600	mW
Operating temperature range		
DS7820A	-55 to +125	°C
DS8820A	0 to +70	°C
Lead temperature (soldering, 60sec)	300	°C

*NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.1,2,3,4

PARAMETER	TEST CONDITIONS	DS7820A/DS8820A			UNIT
		Min	Typ	Max	
V _{TH} Differential threshold voltage	I _{OUT} = -400μA		0.06	0.5	V
	V _{OUT} ≥ 2.5V		0.06	1.0	V
	I _{OUT} = +16mA		-0.08	-0.5	V
	V _{OUT} ≤ 0.4V		-0.08	-1.0	V
R _{I-} Inverting input resistance	-15V ≤ V _{CM} ≤ +15V	3.6	5		kΩ
R _{I+} Non-inverting input resistance	-15V ≤ V _{CM} ≤ +15V	1.8	2.5		kΩ
R _T Line termination resistance		120	170	250	Ω
I _{I-} Inverting input current	V _{CM} = 15V		3.0	4.2	mA
	V _{CM} = 0V		0	-0.5	mA
	V _{CM} = -15V		-3.0	-4.2	mA
I _{I+} Non-inverting input current	V _{CM} = 15V		5.0	7.0	mA
	V _{CM} = 0V		-1.0	-1.6	mA
	V _{CM} = -15V		-7.0	-9.8	mA
I _{CC} Power supply current	V _{DIFF} = -1V, I _{OUT} = Logical "0", V _{DIFF} = -0.5V,		3.9	6.0	mA
	V _{CM} = 15V		9.2	14.0	mA
	V _{CM} = -15V, V _{CM} = 0V		6.5	10.2	mA
V _{OH} Logical "1" output voltage	I _{OUT} = -400μA, V _{DIFF} = 1V	2.5	4.0	5.5	V
V _{OL} Logical "0" output voltage	I _{OUT} = +16mA, V _{DIFF} = -1V	0	0.22	0.4	V
V _{SH} Logical "1" strobe input voltage	I _{OUT} = +16mA, V _{OUT} ≤ 0.4V, V _{DIFF} = -3V	2.1			V
V _{SL} Logical "0" strobe input voltage	I _{OUT} = -400μA, V _{OUT} ≥ 2.5V, V _{DIFF} = -3V			0.9	V
I _{SH} Logical "1" strobe input current	V _{STROBE} = 5.5V, V _{DIFF} = 3V		0.01	5.0	μA
I _{SL} Logical "0" strobe input current	V _{STROBE} = 0.4V, V _{DIFF} = -3V		-1.0	-1.4	mA
I _{SC} Output short circuit current	I _{OUT} = 0V, V _{CC} = 5.5V, V _{STROBE} = 0V	-2.8	-4.5	-6.7	mA

NOTES

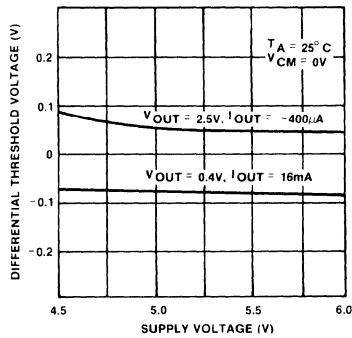
1. These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, -15V ≤ V_{CM} ≤ 15V and -55°C ≤ T_A ≤ +125°C for the DS7820A or 0°C ≤ T_A ≤ +70°C for the DS8820A unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
3. Only one output at a time should be shorted.
4. The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, V_{CC} = 5V unless otherwise specified.

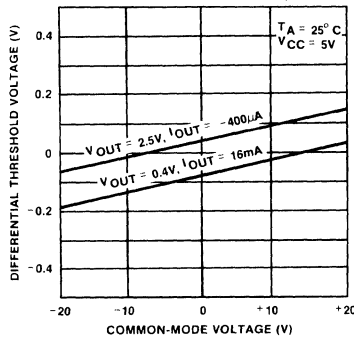
PARAMETER	TEST CONDITIONS	DS7820A/DS8820A			UNIT
		Min	Typ	Max	
t _{PD0} Propagation delay, differential input to "0" output			30	45	ns
t _{PD1} Propagation delay, differential input to "1" output			27	40	ns
t _{PD0} Propagation delay, strobe input to "0" output			16	25	ns
t _{PD1} Propagation delay, strobe input to "1" output			18	30	ns

TYPICAL PERFORMANCE CHARACTERISTICS

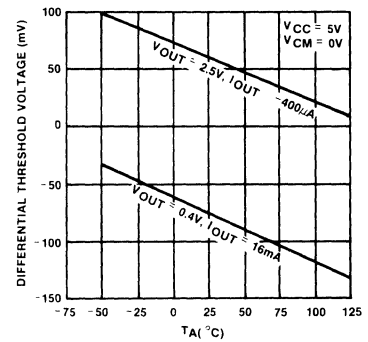
SUPPLY VOLTAGE SENSITIVITY



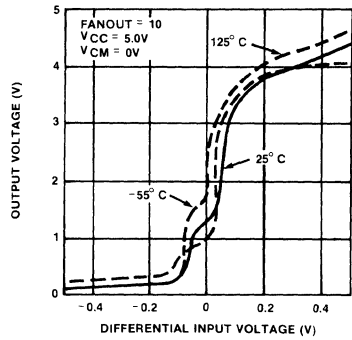
COMMON-MODE VOLTAGE SENSITIVITY



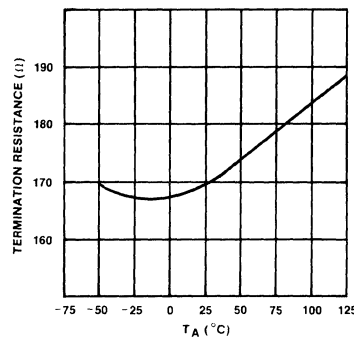
TEMPERATURE SENSITIVITY



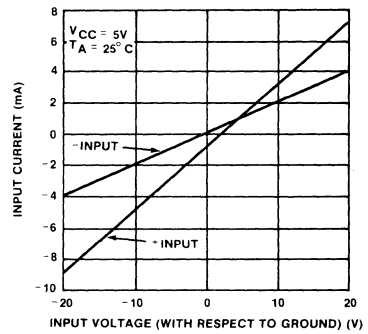
TRANSFER FUNCTION



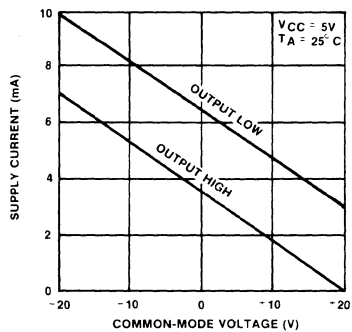
TERMINATION RESISTANCE



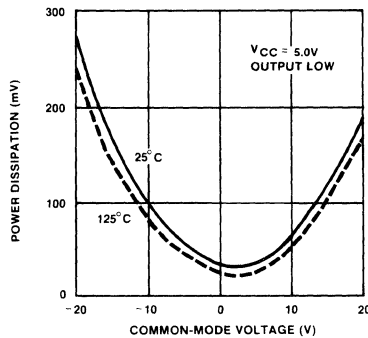
INPUT CHARACTERISTICS



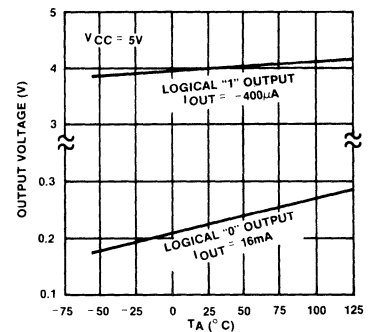
POWER SUPPLY CURRENT



INTERNAL POWER DISSIPATION

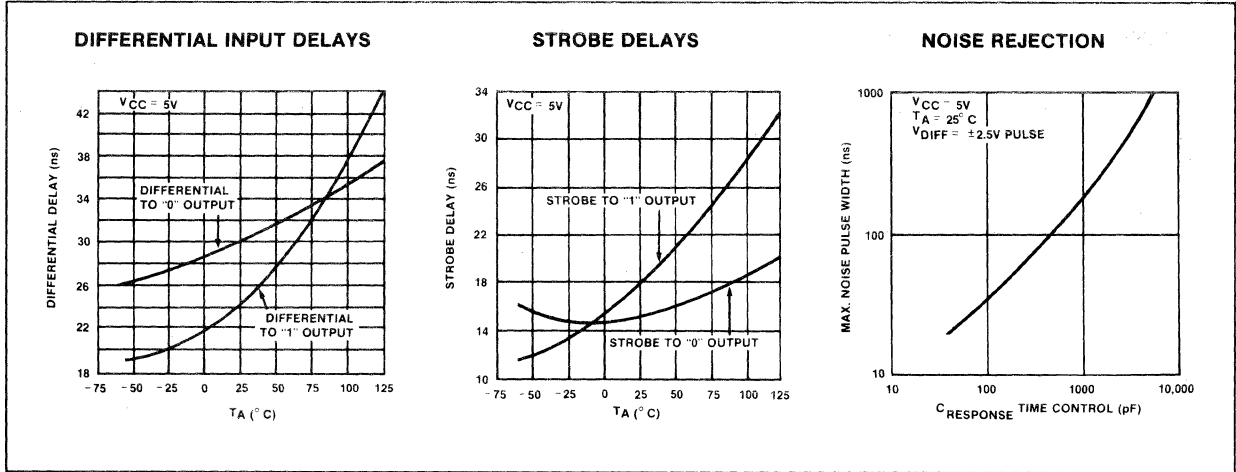


OUTPUT VOLTAGE LEVELS

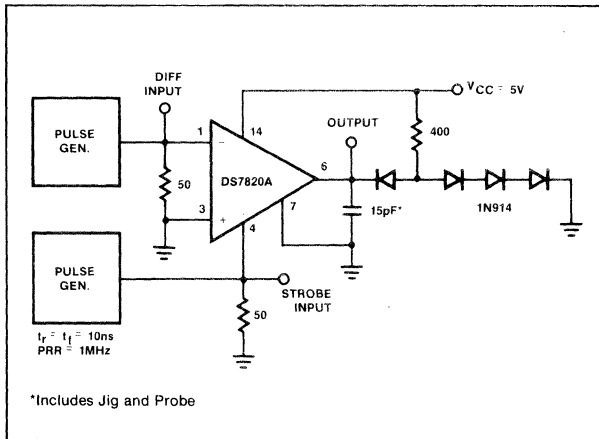


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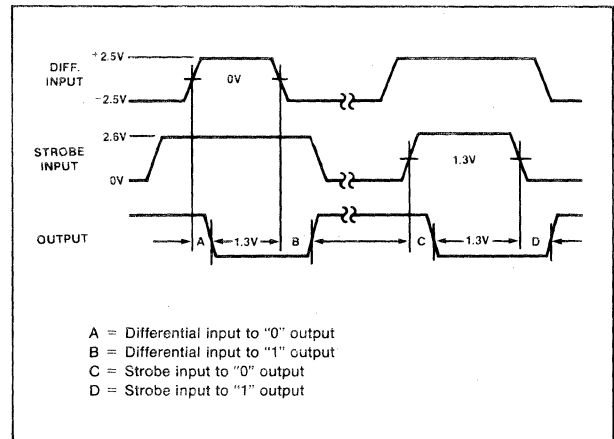
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



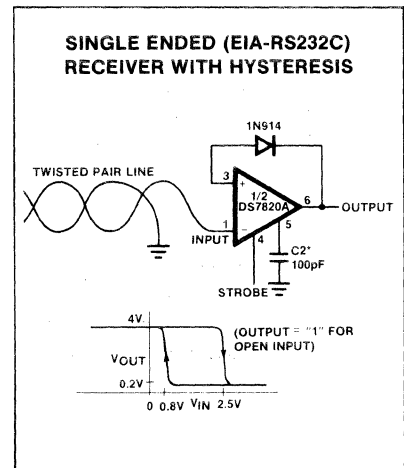
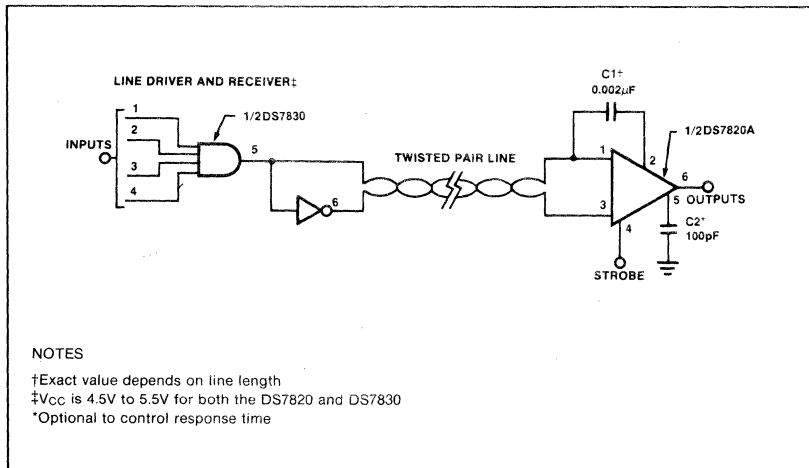
AC TEST CIRCUIT



VOLTAGE WAVEFORM



TYPICAL APPLICATIONS



DESCRIPTION

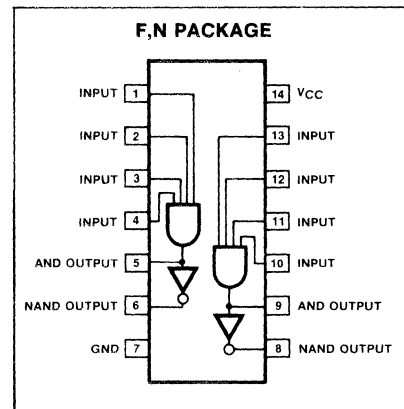
The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

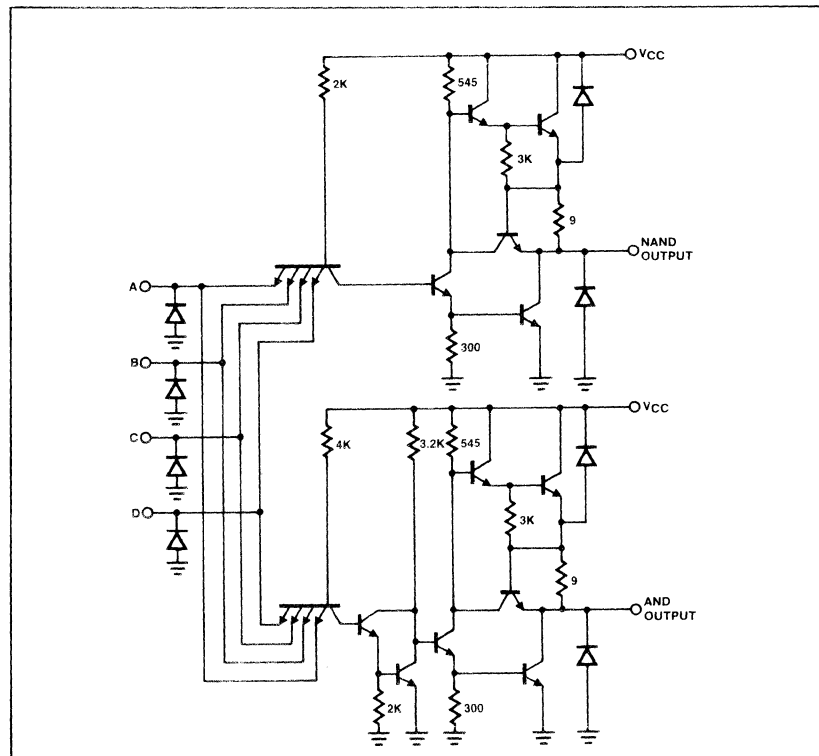
FEATURES

- Single 5 volt power supply
- High speed
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- Short circuit protection
- DS7830 Mil std 883A,B,C available

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{cc}	7.0	V
Input voltage	5.5	V
Operating temperature range		
DS7830	-55 to +125	°C
DS8830	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C



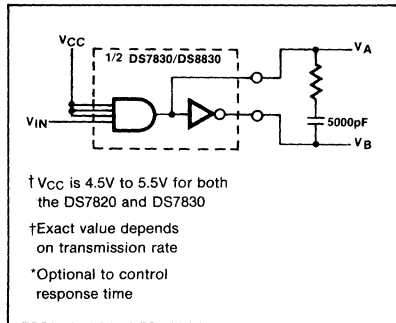
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$ unless otherwise specified.1,2

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Logical "1" input voltage		2.0			V
Logical "0" input voltage				0.8	V
Logical "1" output voltage	$V_{IN} = 0.8\text{V}$ $I_{OUT} = -0.8\text{mA}$	2.4			V
Logical "1" output voltage	$V_{IN} = 0.8\text{V}$ $I_{OUT} = -40\text{mA}$	1.8	2.9		V
Logical "0" output voltage	$V_{IN} = 2.0\text{V}$ $I_{OUT} = +32\text{mA}$		0.2	0.4	V
Logical "0" output voltage	$V_{IN} = 2.0\text{V}$ $I_{OUT} = +40\text{mA}$		0.22	0.5	V
Logical "1" input current	$V_{IN} = +2.4\text{V}$			120	μA
Logical "1" input current	$V_{IN} = 5.5\text{V}$			2	mA
Logical "0" input current	$V_{IN} = 0.4\text{V}$			4.8	mA
Output short circuit current ²	$V_{CC} = 5.0\text{V}$	-40	-100	-120	mA
Supply current	$V_{CC} = 5.0\text{V}$ $V_{IN} = 5.0\text{V}$ (Each driver)		11	18	mA
Propagation delay AND gate	t_{pd1}	$T_A = 25^\circ\text{C}$	8	12	ns
	t_{pd0}	$V_{CC} = 5.0\text{V}$	11	18	ns
Propagation delay NAND gate	t_{pd1}	$C_L = 15\text{pF}$	8	12	ns
	t_{pd0}	See Figure 1	5	8	ns
Differential delay t_1	Load, 100 Ω and 5000pF		12	16	ns
Differential delay t_2	See Figure 2		12	16	ns

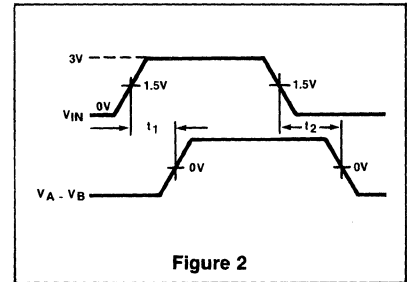
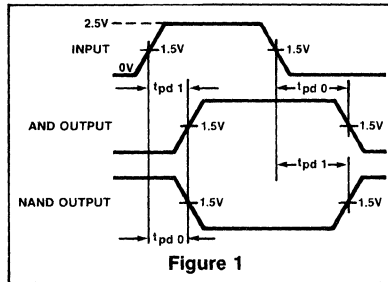
NOTES

- Specifications apply for DS7830 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, DS8830 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$ unless otherwise specified.
- Applies for $T_A = +125^\circ\text{C}$, only one output at a time to be shorted.

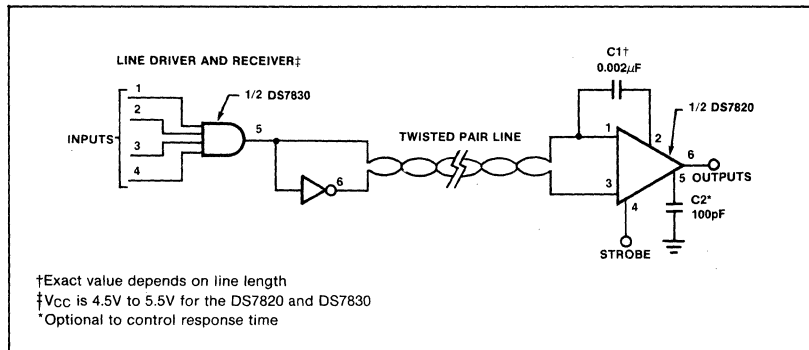
AC TEST CIRCUIT



SWITCHING TIME WAVEFORMS



TYPICAL APPLICATION



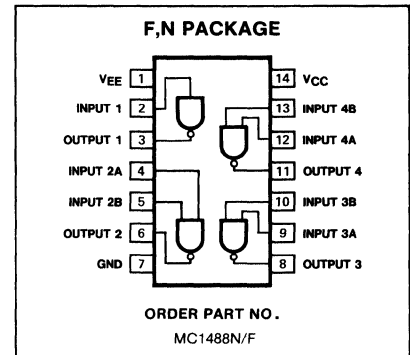
DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

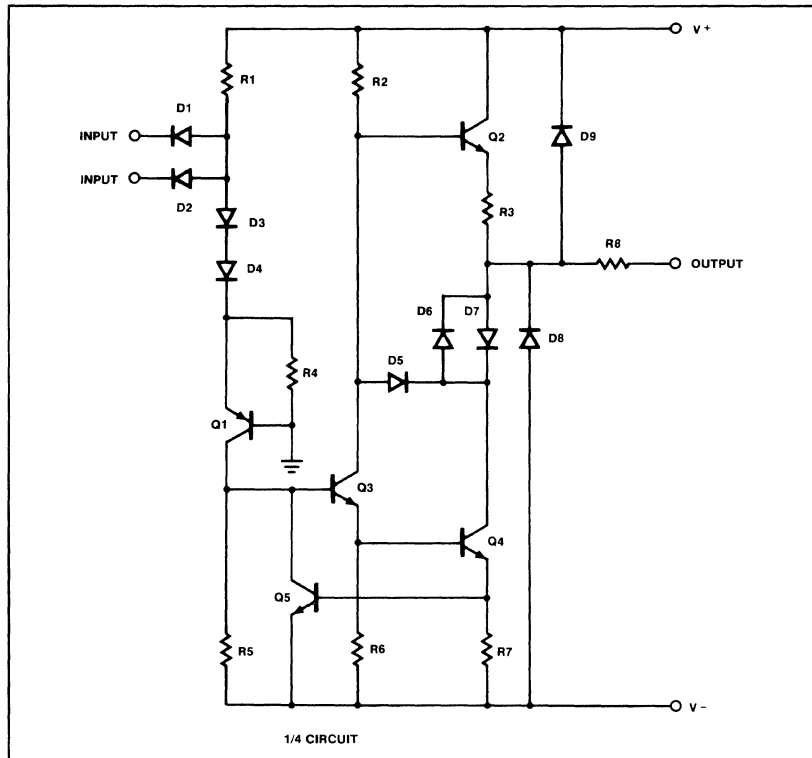
FEATURES

- Current limited output: $\pm 10\text{mA}$ Typ
- Power-off source impedance: 300Ω Min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

PIN CONFIGURATION



CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V _{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	± 15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C



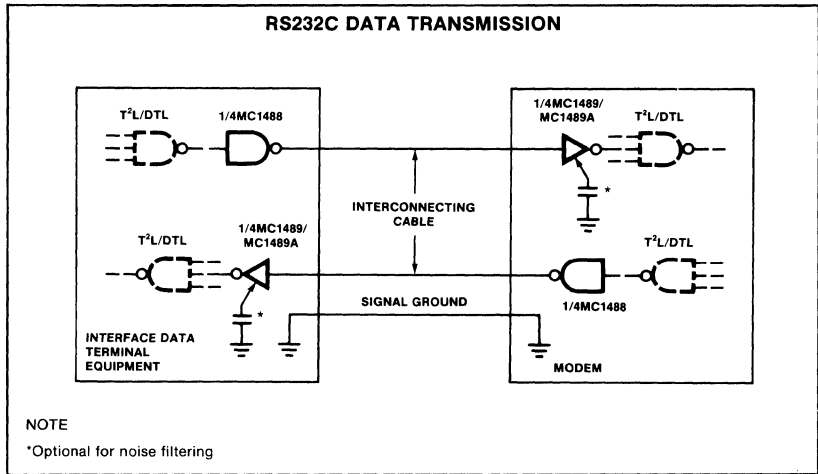
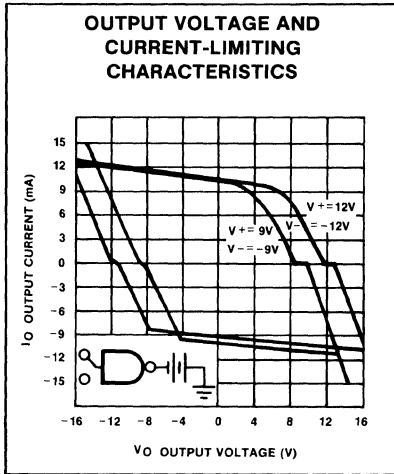
DC ELECTRICAL CHARACTERISTICS $V_+ = +9.0V \pm 1\%$, $V_- = -9.0V \pm 1\%$, $T_A = 0^\circ C$ to $+75^\circ C$
 unless otherwise specified.
 All typicals are for $V_+ = 9.0V$, $V_- = -9.0V$, and $T_A = 25^\circ C$.*

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ	Max		
Logic "0" input current	$V_{IN} = 0V$		-1.0	-1.6	mA	
Logic "1" input current	$V_{IN} = +5.0V$.005	10.0	μA	
High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V_+ = 9.0V$ $V_- = -9.0V$	6.0	7.0	V	
		$V_+ = 13.2V$ $V_- = -13.2V$	9.0	10.5	V	
Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V_+ = 9.0V$ $V_- = -9.0V$	-6.0	-6.8	V	
		$V_+ = 13.2V$ $V_- = -13.2V$	-9.0	-10.5	V	
High level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		-6.0	-10.0	mA	
Low level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		6.0	10.0	mA	
Output resistance	$V_+ = V_- = 0V$ $V_{OUT} = \pm 2V$		300		Ω	
Positive supply current (output open)	$V_{IN} = 1.9V$	$V_+ = 9.0V, V_- = -9.0V$		15.0	20.0	mA
		$V_+ = 12V, V_- = -12V$		19.0	25.0	mA
		$V_+ = 15V, V_- = -15V$		25.0	34.0	mA
	$V_{IN} = 0.8V$	$V_+ = 9.0V, V_- = -9.0V$		4.5	6.0	mA
		$V_+ = 12V, V_- = -12V$		5.5	7.0	mA
		$V_+ = 15V, V_- = -15V$		8.0	12.0	mA
Negative supply current (output open)	$V_{IN} = 1.9V$	$V_+ = 9.0V, V_- = -9.0V$		-13.0	-17.0	mA
		$V_+ = 12V, V_- = -12V$		-18.0	-23.0	mA
		$V_+ = 15V, V_- = -15V$		-25.0	-34.0	mA
	$V_{IN} = 0.8V$	$V_+ = 9.0V, V_- = -9.0V$		-1	-15	μA
		$V_+ = 12V, V_- = -12V$		-1	-15	μA
		$V_+ = 15V, V_- = -15V$		-.01	-2.5	mA
Power dissipation	$V_+ = 9.0V, V_- = -9.0V$ $V_+ = 12V, V_- = -12V$		252	333	mW	
Propagation delay to "1" (t_{pd1})	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		444	576	mW	
Propagation delay to "0" (t_{pd0})	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		275	560	ns	
Rise time (t_r)	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		70	175	ns	
Fall time (t_f)	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		75	100	ns	
			40	75	ns	

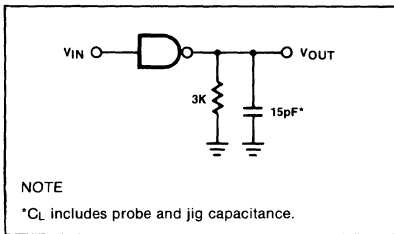
NOTE

*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

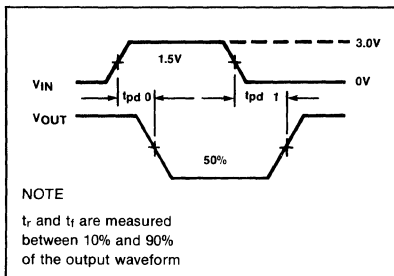
TYPICAL PERFORMANCE CHARACTERISTICS



AC LOAD CIRCUIT



SWITCHING WAVEFORMS



APPLICATIONS

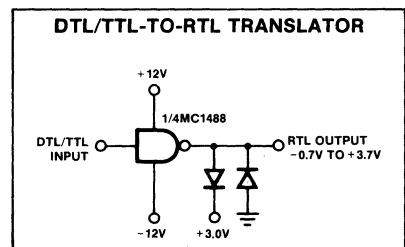
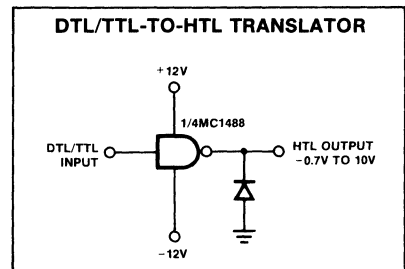
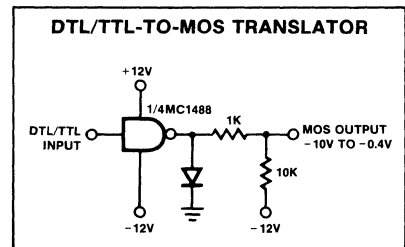
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{sc} (\Delta T / \Delta V)$$

where C is the required capacitor, I_{sc} is the short circuit current value, and ΔV/ΔT is the slew rate.

RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS



8

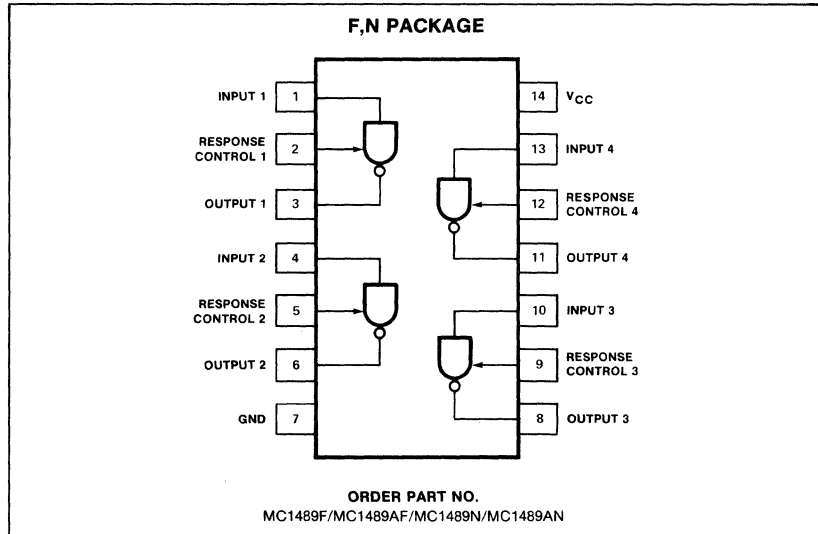
DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

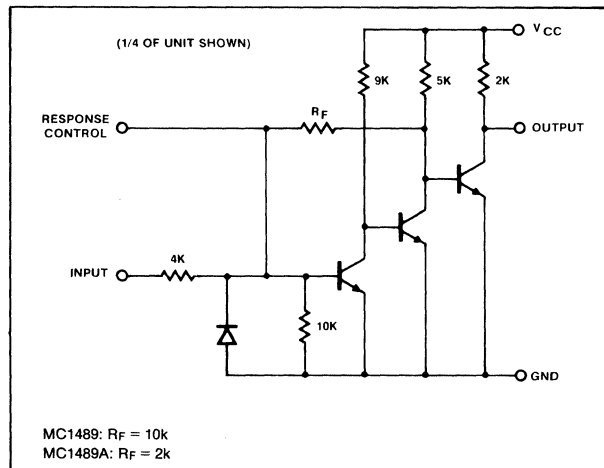
FEATURES

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand $\pm 30V$

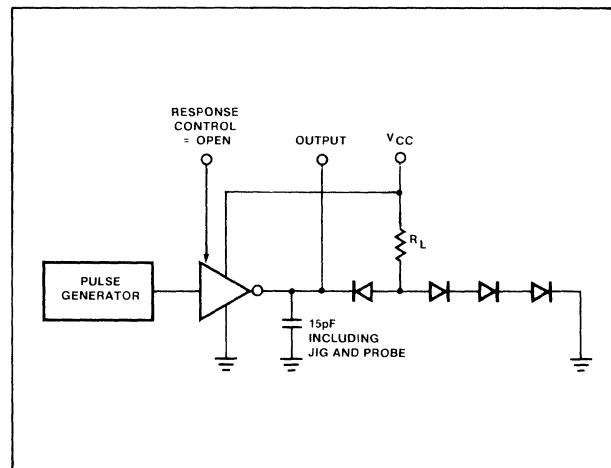
PIN CONFIGURATION



EQUIVALENT SCHEMATIC



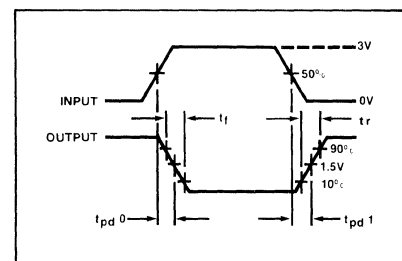
AC TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	± 30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$

VOLTAGE WAVEFORMS



DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $0^\circ C \leq T_A \leq +75^\circ C$ unless otherwise specified.1,2

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	$T_A = 25^\circ C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10mA$	1.0		1.5	1.75		2.25	V
Input low threshold voltage	$T_A = 25^\circ C$, $V_{OUT} \leq 2.5V$, $I_{OUT} = -0.5mA$	0.75		1.25	0.75		1.25	V
Input current	$V_{IN} = +25V$	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	$V_{IN} = -25V$	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
Input current	$V_{IN} = +3V$ $V_{IN} = -3V$	+0.43 -0.43	+0.53 -0.53		+0.43 -0.43	+0.53 -0.53		mA
Output high voltage	$V_{IN} = 0.75V$, $I_{OUT} = -0.5mA$	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	Input = Open, $I_{OUT} = -0.5mA$ $V_{IN} = 3.0V$, $I_{OUT} = 10mA$	2.6	3.8 0.33	5.0 0.45	2.6	3.8 0.33	5.0 0.45	V
Output short circuit current	$V_{IN} = 0.75V$		3.0			3.0		mA
Supply current	$V_{IN} = 5.0V$		20	26		20	26	mA
Power dissipation	$V_{IN} = 5.0V$		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

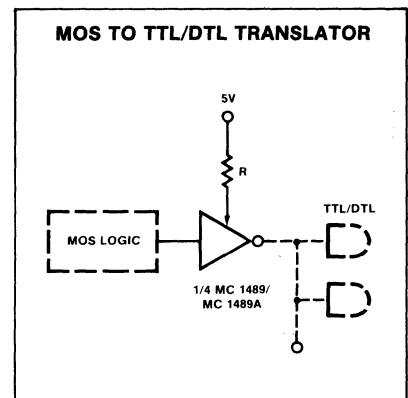
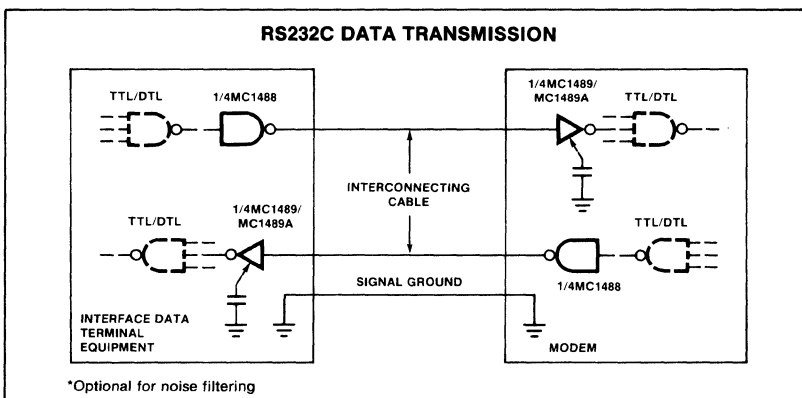
AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $T_A = 25^\circ C$ unless otherwise specified.1,2

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	$R_L = 3.9k\Omega$ (AC test circuit)		25	85		25	85	ns
	Input to output "low" Propagation delay (t_{pd0})		20	50		20	50	
Output rise time	$R_L = 3.9k\Omega$ (AC test circuit)		110	175		110	175	ns
Output fall time	$R_L = 390\Omega$ (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

TYPICAL APPLICATIONS



DESCRIPTION

The 75S107 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75107A. It features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S107 maintains $\pm 3V$ common mode voltage range, 7.5mV input offset voltage and 5 μA offset current. It also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

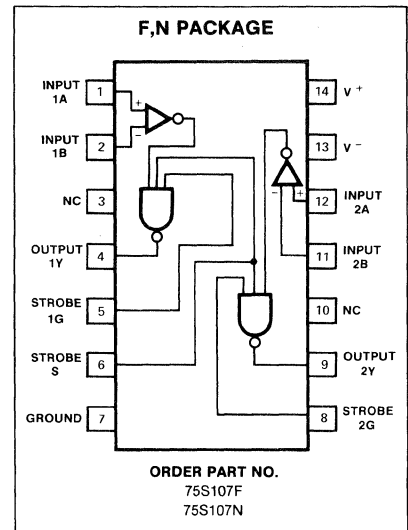
FEATURES

- Functionally equivalent and pin compatible to SN75107A
- 17ns maximum guaranteed propagation delay
- 20 μA maximum input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A/D conversion
- High speed line receiver

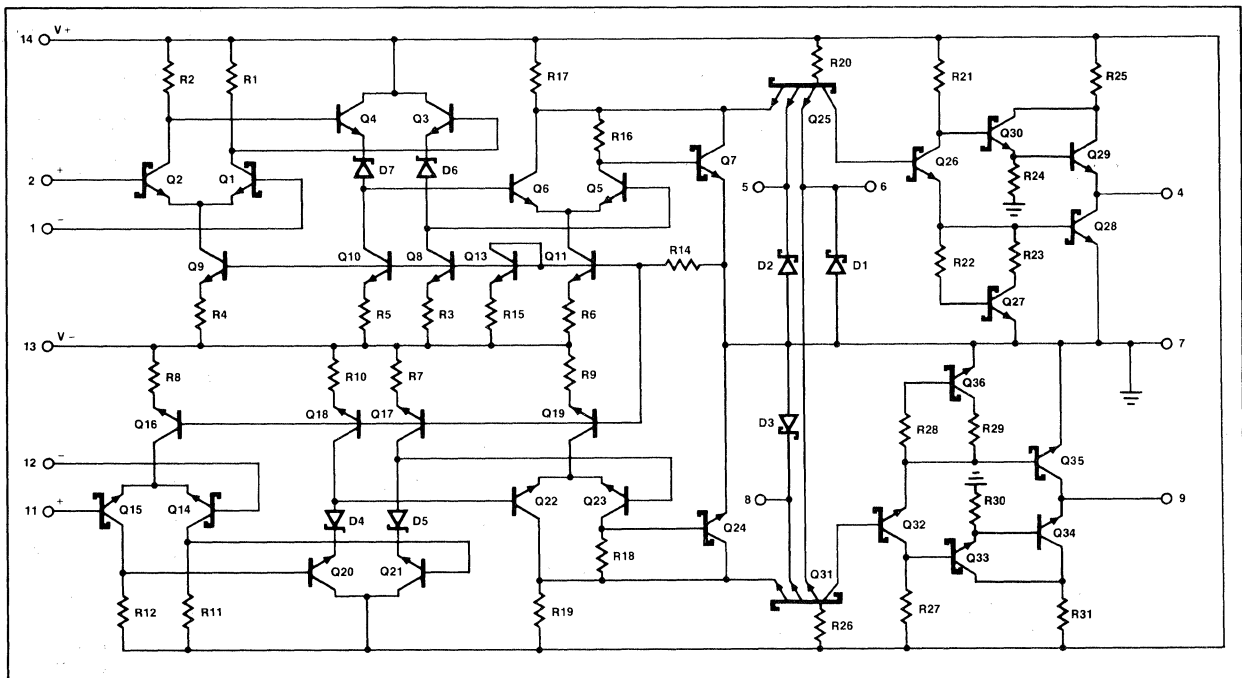
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	± 6	V
Common mode input voltage	± 5	V
Strobe/gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to +70	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$
Lead temperature (soldering 60sec)	+300	$^{\circ}C$

EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS $T_A = 0$ to $+70^\circ\text{C}$, $V_+ = +5.00$, $V_- = -5.00$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	75S107			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT					
Input offset voltage	$V_+ = 4.75$, $V_- = -4.75$			25	mV
Input bias current @ 25°C over temp. range	$V_+ = 5.25$, $V_- = -5.25$ $V_+ = 5.25$, $V_- = -5.25$		7.5	20 40	μA μA
Input offset current @ 25°C over temp. range	$V_+ = 5.25$, $V_- = -5.25$ $V_+ = 5.25$, $V_- = -5.25$		1.0	5 12	μA μA
Input common mode voltage range	$V_+ = 4.75$, $V_- = -4.75$	± 3			V
Input resistance			4		k Ω
Input capacitance			3	6	pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS					
I_{IH} High level input current into 1G or 2G strobe	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			50 1	μA mA
I_{IH} High level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			100 2	μA mA
I_{IL} Low level input current into 1G or 2G	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-2.0	mA
I_{IL} Low level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-4.0	mA
V_{OH} High level output voltage	$V_+ = 4.75\text{V}$, $V_{I(S)} = 2.0\text{V}$ $V_- = -4.75\text{V}$ $I_{LOAD} = -1\text{mA}$	2.7	3.4		V
V_{OL} Low level output voltage	$V_+ = 4.75$ $V_- = -4.75$ $I_{LOAD} = 20\text{mA}$ $V_{I(S)} = 2.0\text{V}$			0.5	V
POWER SUPPLY REQUIREMENTS					
Supply voltage					
V_+		4.75	5.00	5.25	V
V_-		-4.75	-5.00	-5.25	V
I_{CC+} Supply current	$V_+ = 5.25\text{V}$ $V_- = -5.25\text{V}$ $T_A = 25^\circ\text{C}$		20	30	mA
I_{CC-}			-11	-15	mA
I_{OS} Short circuit output current	$V_+ = +5.25$ $V_- = -5.25$	-40		-100	mA
LARGE SIGNAL SWITCHING SPEED					
T_{pLH} (D) Low to high propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		12	17	ns
T_{pHL} (D) High to low propagation delay from amps inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		9	13	ns
T_{pLH} (S) Low to high propagation delay from strobes input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		4.5	6	ns
T_{pHL} (S) High to low propagation delay strobe input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		3.0	4.5	ns
Maximum operating frequency	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$	40	55		MHz

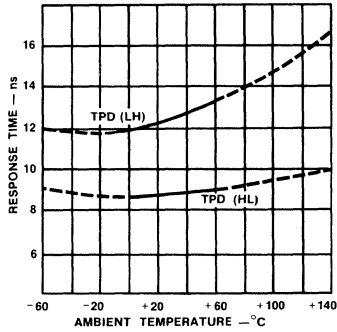
NOTES

- Response time measured from 0V point of $\pm 100\text{mV}$ -p 10MHz square wave to the 1.5 point of the output.
- Response time measured from 1.5V point to input to 1.5V point of output.
- Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

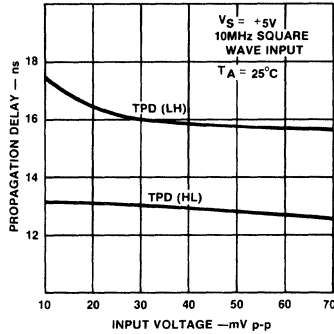


TYPICAL PERFORMANCE CHARACTERISTICS

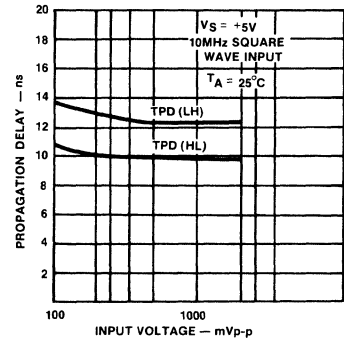
RESPONSE TIME vs TEMPERATURE



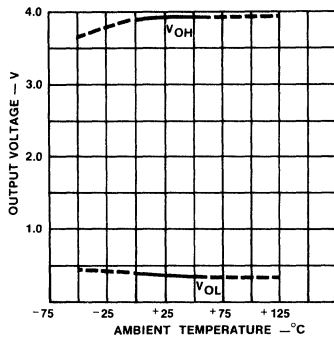
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



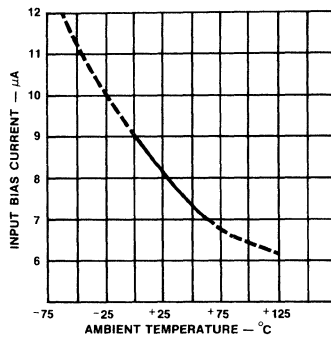
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



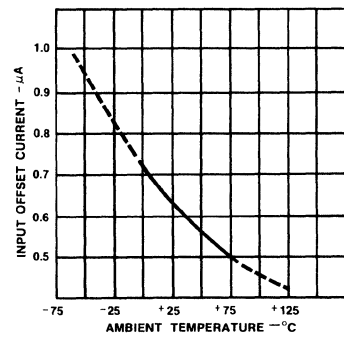
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



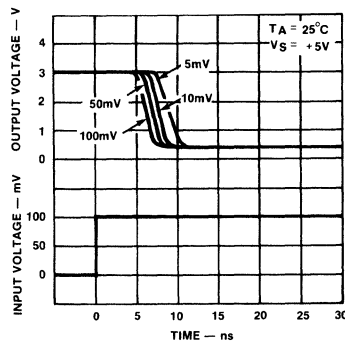
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



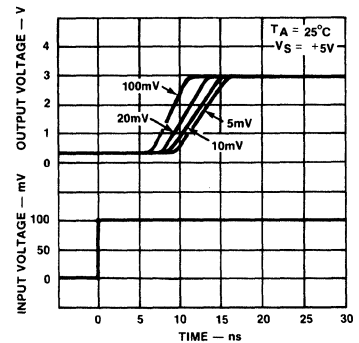
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The 75S108 is a high speed dual line receiver that is functionally equivalent and pin compatible to the SN75108N. It features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S108 maintains $\pm 3V$ common mode voltage range, 7.5mV input offset voltage and 5 μA offset current. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

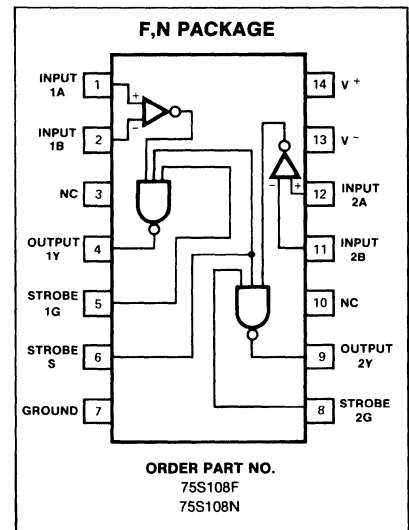
FEATURES

- Functionally equivalent and pin compatible to SN75108A
- 17ns maximum guaranteed propagation delay
- 20 μA maximum input bias current
- TTL compatible strobes and outputs
- Open collector outputs
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- High speed line receiver
- MOS memory sense amp
- A/D conversion

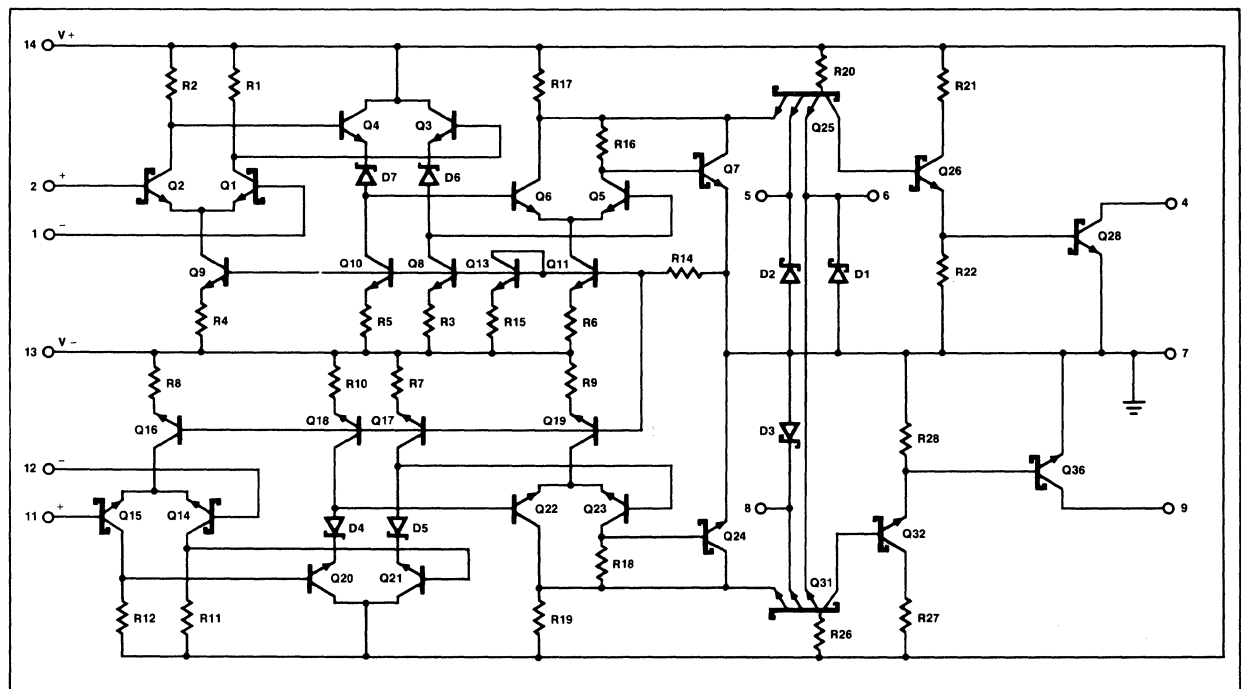
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	± 6	V
Common mode input voltage	± 5	V
Strobe gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to 70	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$
Lead temperature (soldering 60 sec)	+300	$^{\circ}C$

EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS $T_A = 0$ to 70°C , $V_+ = +5.00$, $V_- = -5.00$ unless otherwise specified.

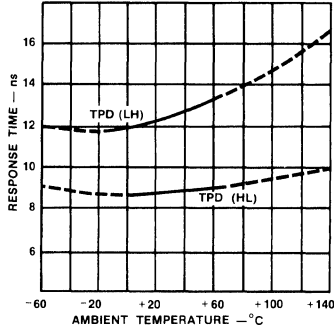
PARAMETER	TEST CONDITIONS	75S108			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT Input offset voltage	$V_+ = 4.75$, $V_- = -4.75$			25	mV
Input bias current @ 25°C over temp range	$V_+ = 5.25$, $V_- = -5.25$ $V_+ = 5.25$, $V_- = -5.25$		7.5	20 40	μA μA
Input offset current @ 25°C over temp range	$V_+ = 5.25$, $V_- = -5.25$ $V_+ = 5.25$, $V_- = -5.25$		1.0	5 12	μA μA
Input common mode voltage range	$V_+ = 4.75$, $V_- = -4.75$	± 3		± 3	V
Input resistance			4		k Ω
Input capacitance			3	6	pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS					
I_{IH} High level input current into 1G or 2G strobe	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			50 1	μA mA
I_{IH} High level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			100 2	μA mA
I_{IL} Low level input current into 1G or 2G	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-2.0	mA
I_{IL} Low level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-4.0	mA
V_{OL} Low level output voltage	$V_+ = 4.75$, $V_1(S) = 2.0\text{V}$ $V_- = -4.75$ $I_{LOAD} = 20\text{mA}$			0.5	V
I_{OH} High level output current	$V_{CC+} = 5.25\text{V}$ $V_{CC-} = -5.25\text{V}$ $V_{OH} = 5.25\text{V}$			250	μA
POWER SUPPLY REQUIREMENTS					
Supply voltage					
V_+		4.75	5.00	5.25	V
V_-		-4.75	-5.00	-5.25	V
Supply current	$V_+ = 5.25\text{V}$ $V_- = -5.25\text{V}$ $T_A = 25^\circ\text{C}$				
I_{CC+}			20	30	mA
I_{CC-}			-11	-15	mA
LARGE SIGNAL SWITCHING SPEED					
$T_{pLH}(D)$ Low to high propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		12	17	ns
$T_{pHL}(D)$ High to low propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		9	13	ns
$T_{pLH}(S)$ Low to high propagation delay from strobes input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		6	10	ns
$T_{pHL}(S)$ High to low propagation delay strobe input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		5	8	ns
Maximum operating frequency	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$	25	35		MHz

NOTES:

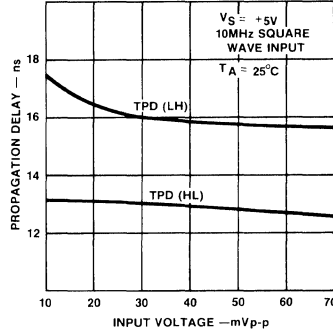
- Response time measured from 0V point of ± 100 mVp-p 10MHz square wave to the 1.5 point of the output.
- Response time measured from 1.5V point of input to 1.5V point of output.
- Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

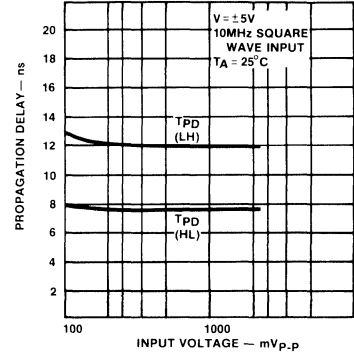
RESPONSE TIME vs TEMPERATURE



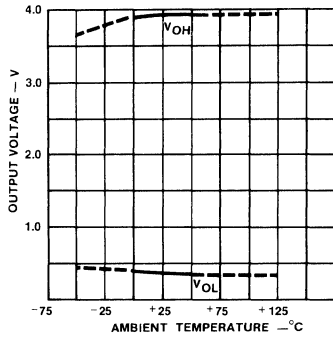
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



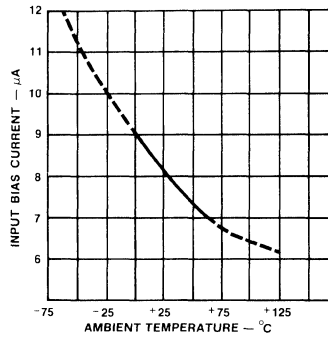
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



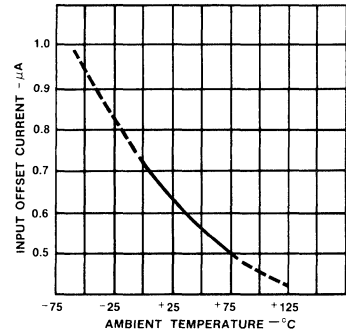
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



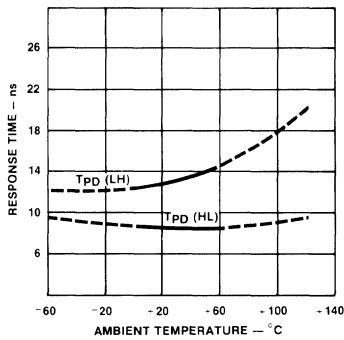
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



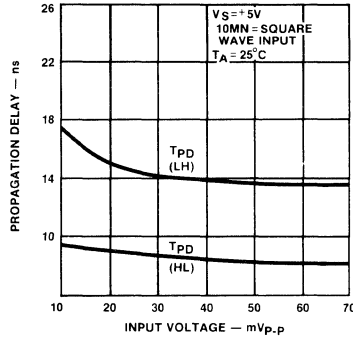
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



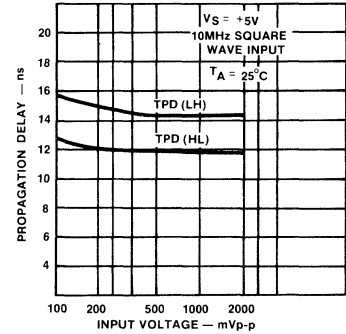
RESPONSE TIME vs TEMPERATURE



PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

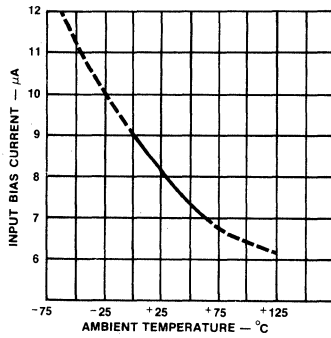


PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES

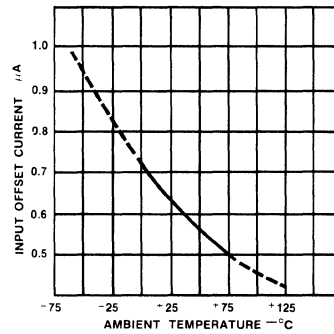


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

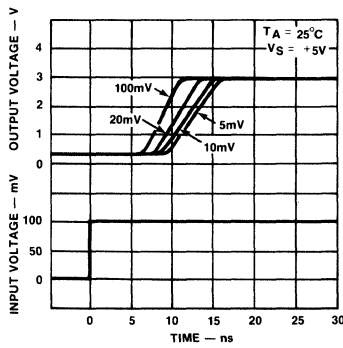
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



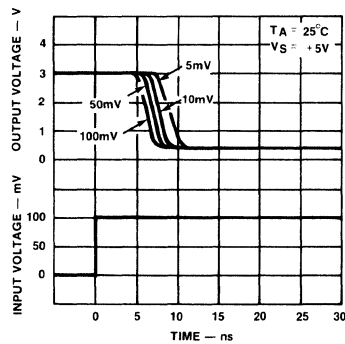
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The 75S207 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75207. The improved input sensitivity of $\pm 10\text{mV}$ makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles. The 75S207 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology.

The 75S207 also features STTL compatible output levels with a minimum sink/source capability of 10 Schottky gate loads.

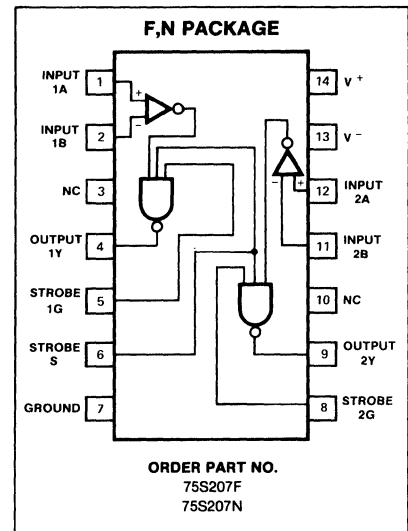
FEATURES

- Functionally equivalent and pin compatible to SN75207
- 17ns maximum guaranteed propagation delay
- 20 μA maximum input bias current
- STTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memories sense amp
- A/D conversion
- High speed line receiver

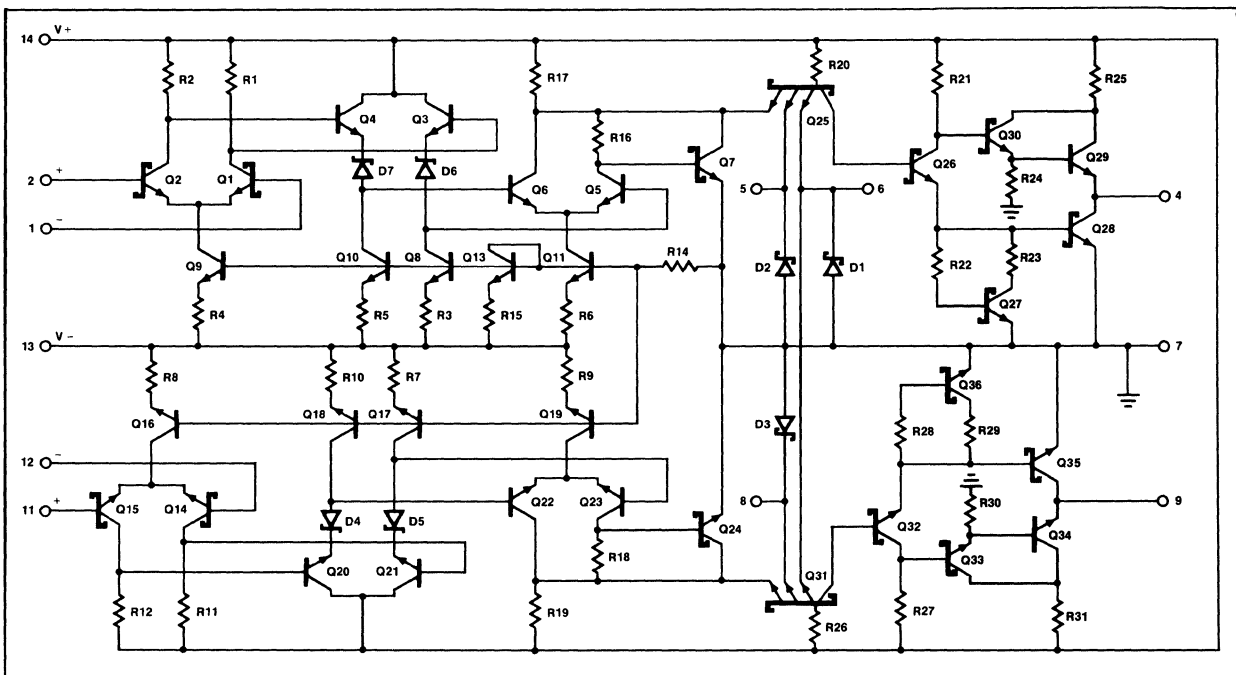
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	± 6	V
Common mode input voltage	± 5	V
Strobe/gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to 70	$^{\circ}\text{C}$
Storage temperature range	-65 to +150	$^{\circ}\text{C}$
Lead temperature (soldering 60sec)	+300	$^{\circ}\text{C}$

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V_+ = +5.00$, $V_- = -5.00$, $T_A = 0$ to 70°C unless otherwise specified.

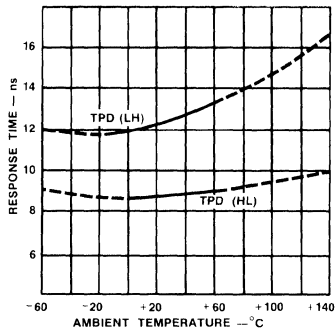
PARAMETER	TEST CONDITIONS	75S207			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT					
Input offset voltage	$V_+ = 4.75$, $V_- = -4.75$			10	mV
Input bias current @ 25°C over temp. range	$V_+ = 5.25$, $V_- = -5.25$		7.5	20	μA
	$V_+ = 5.25$, $V_- = -5.25$			40	μA
Input offset current @ 25°C over temp. range	$V_+ = 5.25$, $V_- = -5.25$		1.0	5	μA
	$V_+ = 5.25$, $V_- = -5.25$			12	μA
Input common mode voltage range	$V_+ = 4.75$, $V_- = -4.75$	± 3			V
Input resistance			4		$\text{k}\Omega$
Input capacitance			3	6	pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT					
I_{IH} High level input current into 1G or 2G strobe	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			50 1	μA mA
I_{IH} High level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			100 2	μA mA
I_{IL} Low level input current into 1G or 2G	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-2.0	mA
I_{IL} Low level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-4.0	mA
V_{OH} High level output voltage	$V_+ = 4.75$, $V_{I(S)} = 2.0\text{V}$ $V_- = -4.75$ $I_{LOAD} = -1\text{mA}$	2.7	3.4		V
V_{OL} Low level output voltage	$V_+ = 4.75$, $V_- = -4.75$ $I_{LOAD} = 20\text{mA}$ $V_{I(S)} = 2.0\text{V}$			0.5	V
POWER SUPPLY REQUIREMENTS					
Supply voltage					
V_+		4.75	5.00	5.25	V
V_-		-4.75	-5.00	-5.25	V
I_{CC+} I_{CC-} Supply current	$V_+ = 5.25\text{V}$ $V_- = -5.25\text{V}$ $T_A = 25^\circ\text{C}$		20	30	mA
			-11	-15	mA
I_{OS} Short circuit output current	$V_+ = 5.25$ $V_- = -5.25$	-40		-100	mA
LARGE SIGNAL SWITCHING SPEED					
$T_{pLH(D)}$ Low to high propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		12	17	ns
$T_{pHL(D)}$ High to low propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		9	13	ns
$T_{pLH(S)}$ Low to high propagation delay from strobes input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		4.5	6	ns
$T_{pHL(S)}$ High to low propagation delay strobe input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		3.0	4.5	ns
Maximum operating frequency	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$	40	55		MHz

NOTES

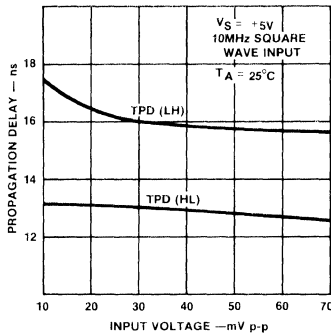
- Response time measured from 0V point of $\pm 100\text{mV}$ P-P 10MHz square wave to the 1.5 point of the output.
- Response time measured from 1.5V point of input to 1.5V point of the output.
- Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

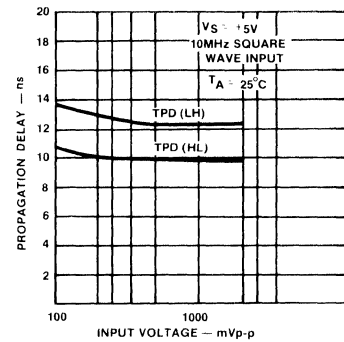
RESPONSE TIME vs TEMPERATURE



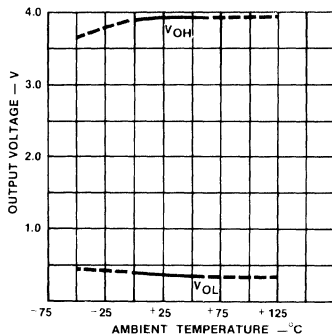
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



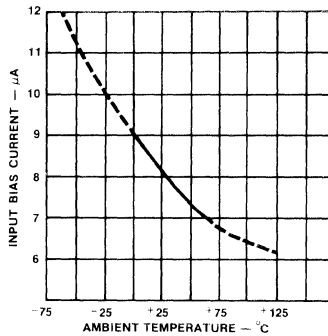
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



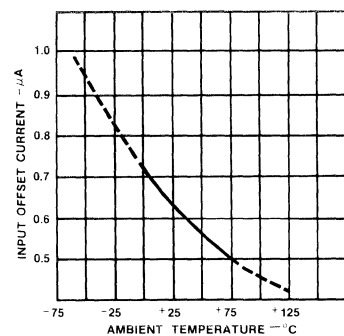
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



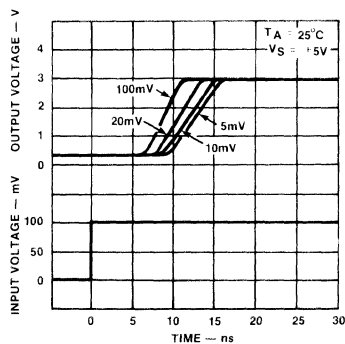
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



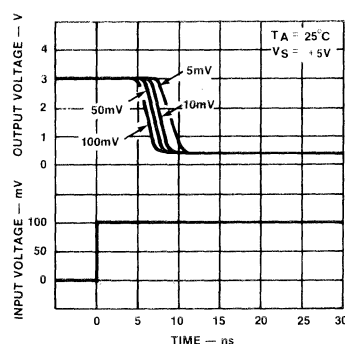
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The 75S208 is a high speed dual sense amplifier that is functionally equivalent and pin compatible to the SN75208. The improved input sensitivity of $\pm 10\text{mV}$ makes it suitable as a MOS memory sense amplifier which can result in faster memory cycles.

The 75S208 features less than 17ns propagation delay without sacrificing input performance characteristics. This is accomplished through the utilization of Schottky technology. It also features STTL compatible output levels with an open collector configuration for wired-AND logic applications.

FEATURES

- Functionally equivalent and pin compatible to 75208
- 17ns maximum guaranteed propagation delay
- 20 μA maximum input bias current
- STTL compatible strobes and outputs
- Open collector outputs
- Large common mode input voltage range
- Operates from standard supply voltages

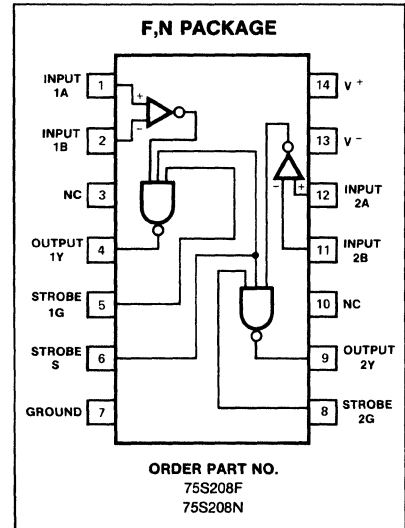
APPLICATIONS

- MOS memories sense amp
- A/D conversion
- High speed line receiver

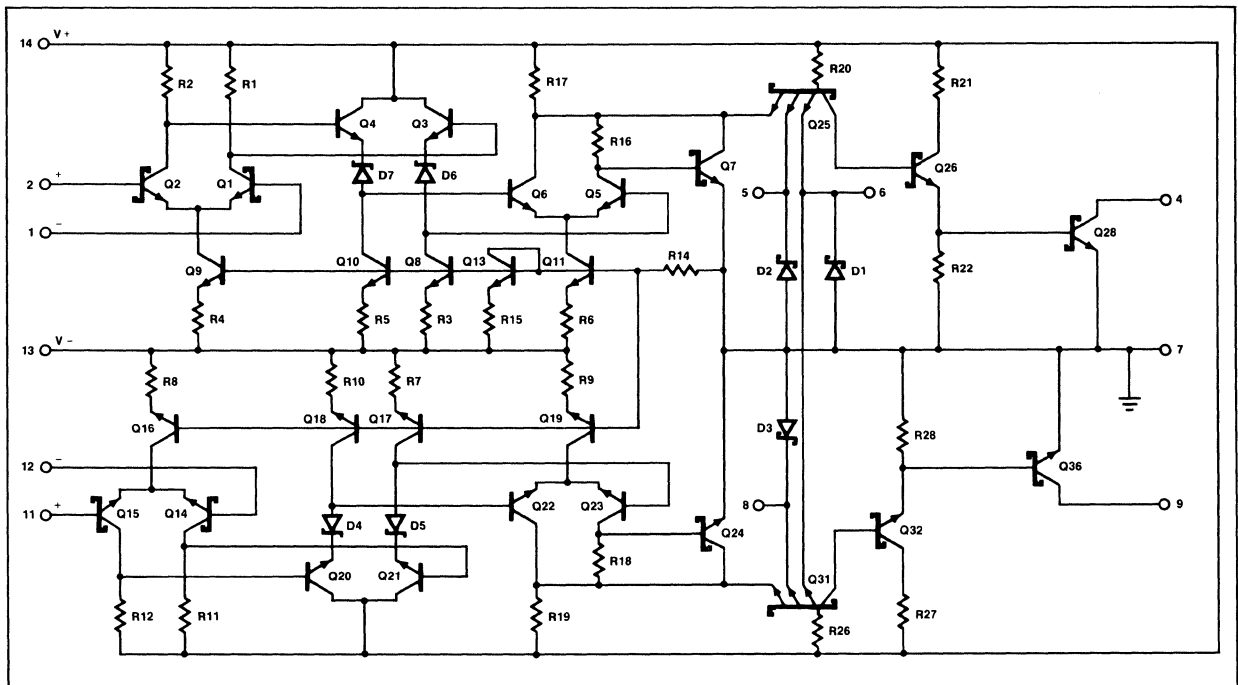
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V+)	+7	V
Negative supply voltage (V-)	-7	V
Differential input voltage	± 6	V
Common mode input voltage	± 5	V
Strobe/gate input voltage	+5.25	V
Power dissipation	600	mW
Operating temperature range	0 to + 70	$^{\circ}\text{C}$
Storage temperature range	-65 to +150	$^{\circ}\text{C}$
Lead temperature (soldering 60sec)	+300	$^{\circ}\text{C}$

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V_+ = +5.00$, $V_- = -5.00$, $T_A = 0$ to 70°C unless otherwise specified.

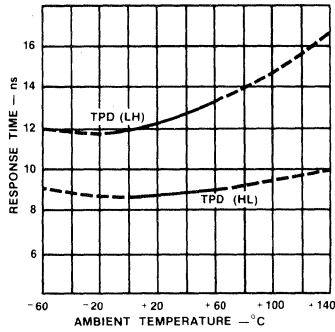
PARAMETER	TEST CONDITIONS	75S208			UNIT
		Min	Typ	Max	
AMPLIFIER INPUT Input offset voltage	$V_+ = 4.75$, $V_- = -4.75$			10	mV
Input bias current @ 25°C over temp. range	$V_+ = 5.25$, $V_- = -5.25$ $V_+ = 5.25$, $V_- = -5.25$		7.5	20 40	μA μA
Input offset current @ 25°C over temp. range	$V_+ = 5.25$, $V_- = -5.25$ $V_+ = 5.25$, $V_- = -5.25$		1.0	5 12	μA μA
Input common mode voltage range	$V_+ = 4.75$, $V_- = -4.75$	± 3			V
Input resistance			4		k Ω
Input capacitance			3	6	pF
Voltage gain			5		V/mV
SCHOTTKY GATE/OUTPUT CHARACTERISTICS					
I_{IH} High level input current into 1G or 2G strobe	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			50 1	μA mA
I_{IH} High level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IH} = 2.7\text{V}$ $V_{IH} = 5.25\text{V}$			100 2	μA mA
I_{IL} Low level input current into 1G or 2G	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-2.0	mA
I_{IL} Low level input current into common strobe S	$V_+ = 5.25$, $V_- = -5.25$ $V_{IL} = 0.5\text{V}$			-4.0	mA
V_{OL} Low level output voltage	$V_+ = 4.75$, $V_{(S)} = 2.0\text{V}$ $V_- = -4.75$ $I_{LOAD} = 20\text{mA}$			0.5	V
I_{OH} High level output current	$V_{CC+} = 5.25\text{V}$ $V_{CC-} = -5.25\text{V}$ $V_{OH} = 5.25\text{V}$			250	μA
POWER SUPPLY REQUIREMENTS					
Supply voltage					
V_+		4.75	5.00	5.25	V
V_-		-4.75	-5.00	-5.25	V
I_{CC+} Supply current	$V_+ = 5.25\text{V}$		20	30	mA
I_{CC-}	$V_- = -5.25\text{V}$ $T_A = 25^\circ\text{C}$		-11	-15	mA
LARGE SIGNAL SWITCHING SPEED					
$T_{pLH(D)}$ Low to high propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		12	17	ns
$T_{pHL(D)}$ High to low propagation delay from amp inputs to output ¹	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		9	13	ns
$T_{pLH(S)}$ Low to high propagation delay from strobes input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		6	10	ns
$T_{pHL(S)}$ High to low propagation delay strobe input to output ²	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$		5	8	ns
Maximum operating frequency	$R_L = 280\Omega$ $C_L = 15\text{pF}$ $T_A = 25^\circ\text{C}$	25	35		MHz

NOTES

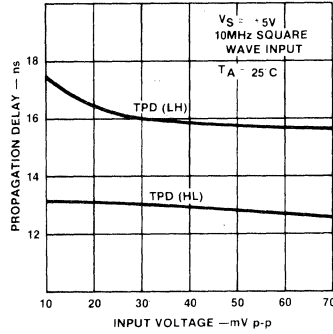
- Response time measured from 0V point of $\pm 100\text{MHz}$ square wave to the 1.5V point of the output.
- Response time measured from 1.5V point of input to 1.5V point of the output.
- Response time measured from the start of a 100mV input step with 5mV overdrive to the 1.5V point of the output.

TYPICAL PERFORMANCE CHARACTERISTICS

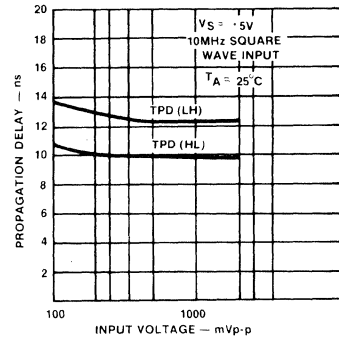
RESPONSE TIME vs TEMPERATURE



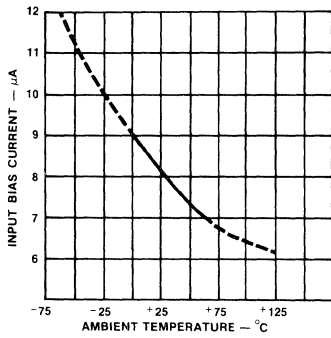
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



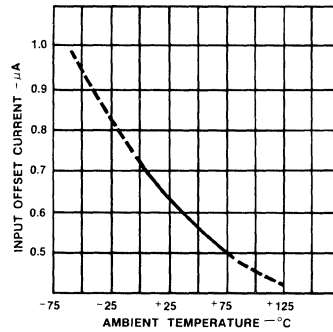
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



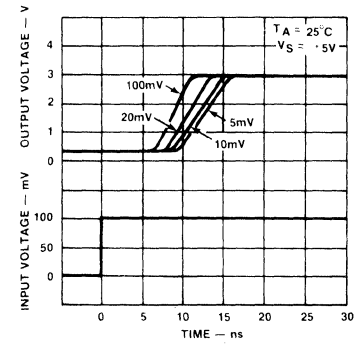
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



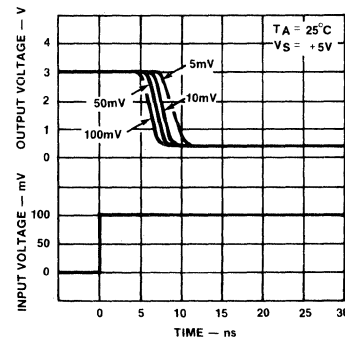
INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



SECTION 9 DISPLAY DRIVERS

Section 9—DISPLAY DRIVERS

NE582	Hex Universal Driver	273
NE587	LED Decoder/Driver	275
NE589	LED Decoder/Driver	284
NE/SA594	Vacuum Fluorescent Display Driver	293

DISPLAY DRIVER DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (- V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

LED

Light Emitting Diode

\overline{XX}

Negate Bar-when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.

i.e. \overline{LE} - would require a logic high level to cause a latch enable.

$\overline{\overline{LE}}$ - would require a logic low level to cause a latch enable.

I_{SEG}

Segment Current. The amount of current supplied to each segment in a display. Current ratios are generally compared to segment 'b'.

BCD

Binary Coded Decimal

\overline{BI}/RBO

Blanking Input or Ripple Blanking Output.

\overline{RBI}

Ripple Blanking Input. The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

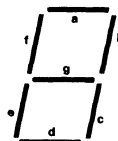
t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

Segment Identification



t_h

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s

Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_w

Pulse Width. The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

Typical Value

The typical value of a particular parameter determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-

DISPLAY DRIVER DEFINITIONS (Cont'd)

max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

V_F

Forward voltage drop of a device at a specified current level.

I_B

Input Bias Current Current into an analog circuit input, specified at a particular voltage level.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

CE

Chip Enable.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL} .

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

I_{CC}(-I_{CC})

Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}

Input High Current. The Current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OL}

Output Low Current. The current flowing into an output when a which is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is short circuit to the ground.

I_{CEX}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

DESCRIPTION

The NE582 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400mA with a typical saturation voltage of 0.5V. Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.

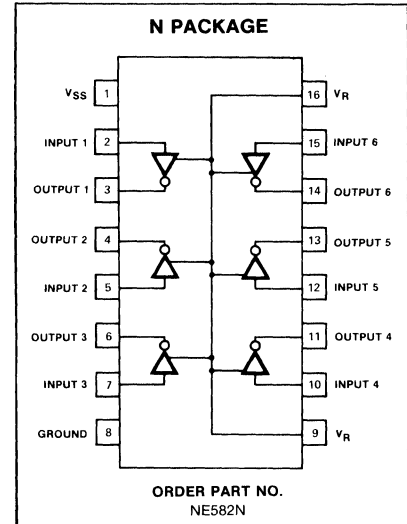
The NE582 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

The NE582 is supplied in a 16-pin high dissipation dual-in-line plastic package.

FEATURES

- Low saturation voltage (typically 0.5V) for minimum power dissipation
- High output sink current capability—400mA
- Low input current loading for MOS compatibility
- Low standby power consumption
- Suitable for 3 volt battery operation
- Inputs/outputs are compatible with 75494

PIN CONFIGURATION



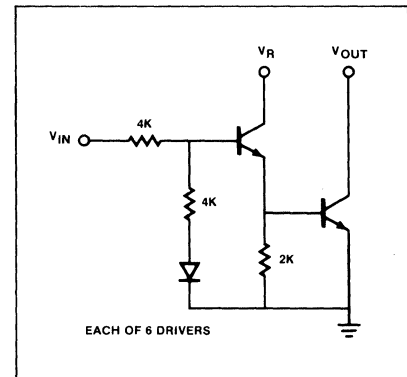
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage range ¹	-12 to V _{SS}	V
Output voltage ²	10	V
Output to input voltage differential	10	V
Voltage at V _{SS} (pin 1)	10	V
Output current—each output	400	mA
Output current—all outputs	800	mA
Continuous total power dissipation at or below 25°C ³	800	mW
Current in V _R (pin 9 or 16)	25	mA
Operating free-air temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature 1/16 inch from case for 10sec	260	°C

NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

EQUIVALENT SCHEMATIC



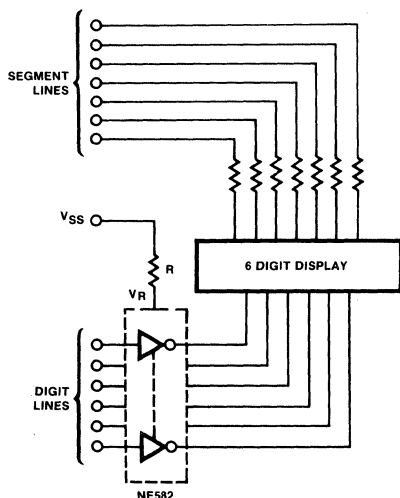
ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V _{OL} Low level output voltage	V _{IN} I _R I _{OL} V mA mA 6.5 12 250 6.5 20 400 R _{IN} = 1K (Series input resistance)		.320	.450	V
			.500	.750	V
I _{OH} High level output current	V _{OH} = 10V, I _{IN} = 40μA V _{OH} = 10V, V _{IN} = 0.5V			400	μA
				400	μA
I _{IN} Input current at maximum Input voltage	V _{IN} = 10V, I _{OL} = 20mA, I _R = 2mA		2.2	3.3	mA
V _R I _{SS} Current into pin 1	V _{IN} = 6.5V, I _R = 6mA, I _{OL} = 80mA V _{SS} = 10V		.9	1.5	V
				100	μA

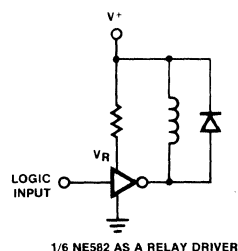
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
T_{PLH}	Switching characteristics Propagation delay, low to high level input $R_R = 680\Omega$ $R_L = 39\Omega$ $C_L = 15\text{pF}$		300		ns
T_{PHL}	Propagation delay, high to low level input $V_{IH} = 7.5\text{V}$ $V_{IL} = 0\text{V}$ $t_r = t_f \leq 10\text{ns}$ $t_w = 1\mu\text{s}$ $\text{PRR} = 100\text{kHz}$		30		ns

TYPICAL APPLICATION FOR DIGIT DRIVING OF AN LED DISPLAY

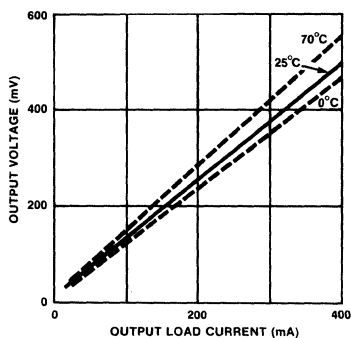


1/6 NE582 AS A RELAY DRIVER

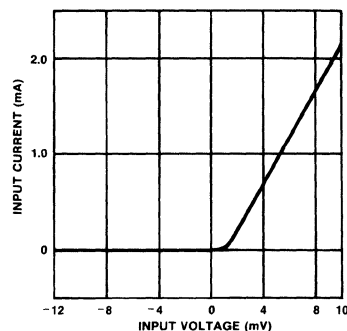


PRELIMINARY SPECIFICATION

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT,
 $I_R = 25\text{mA}$
 $V_{IN} = 6.5\text{VOLTS}$



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE,
 $I_R = 25\text{mA}$, $V_{SS} = 10\text{V}$, $T_A = 25^\circ\text{C}$



DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and \overline{LE} (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading and/or trailing edge zeros

APPLICATIONS

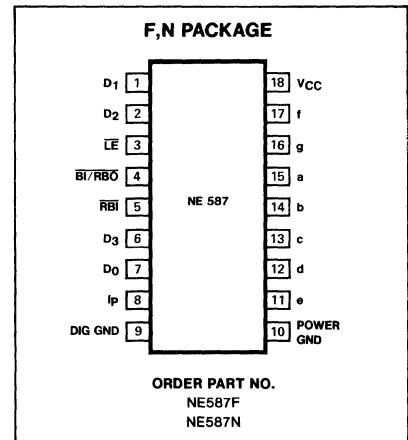
- Digital panel meters
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified

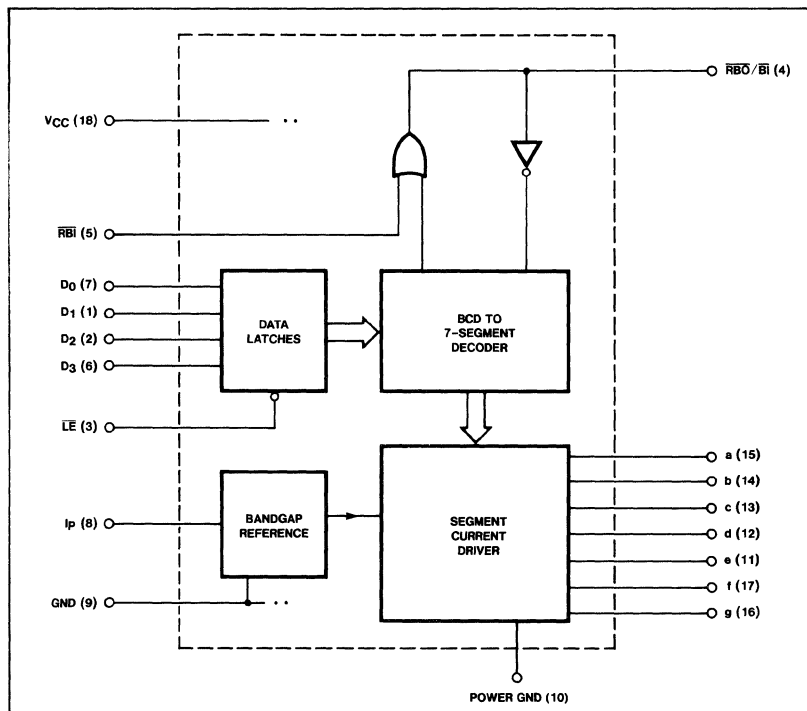
PARAMETER	RATING	UNIT
V_{CC} Supply voltage	-0.5 to +7	V
V_{IN} Input voltage ($D_0 - D_3, \overline{LE}, \overline{RBI}$)	-0.5 to +15	V
V_{OUT} Output voltage (a-g, RBO)	-0.5 to +7	V
P_D Power dissipation (25°C) ¹	1000	mW
T_A Ambient temperature range	0 to 70	$^\circ\text{C}$
T_J Junction temperature	150	$^\circ\text{C}$
T_{STG} Storage temperature range	-65 to +150	$^\circ\text{C}$
T_{SOLD} Soldering temperature (10 sec. max)	300	$^\circ\text{C}$

NOTE
 Derate power dissipation as indicated
 N package - 95°C/watt above 55°C
 F package - 100°C/watt above 50°C

PIN CONFIGURATIONS



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 4.75$ to $5.25V$, $0^{\circ}C < T_A < 70^{\circ}C$.Typical values are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $R_P = 1k\Omega$ ($\pm 1\%$) unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE587			UNIT	
		Min	Typ	Max		
V_{CC}	Operating supply voltage	4.75	5.00	5.25	V	
V_{IH}	Input high voltage	2.0 2.0		15 5.5	V	
V_{IL}	Input low voltage			0.8	V	
V_{IC}	Input clamp voltage			-1.5	V	
I_{IH}	Input high current		0.1 10		μA μA	
I_{IL}	Input low current	$V_{IN} = 0.4V$, Inputs $D_0 - D_3$ \overline{LE} , $\overline{RB1}$		-5 -200	μA	
		Input \overline{BI} $V_{CC} = 5.25V$ $\overline{RB1} = H$, $V_{IN} = 0.4V$		-0.7	mA	
V_{OL}	Output low voltage		.2		V	
V_{OH}	Output high voltage		4.5		V	
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" $V_{OUT} = 2.0V$	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment $V_{OUT} = 2.0V$	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" $V_{OUT} = 5.0V$		20	250	μA
I_{CCO}	Supply current	$V_{CC} = 5.25V$ All outputs "ON" $V_{OUT} > 1V$		33		mA
I_{CCI}	Supply current	$V_{CC} = 5.25V$ All outputs blanked		50		mA

NOTE

NE587 PROGRAMMING

The NE587 output current can be programmed, provided a program resistor, R_P , be connected between I_P (pin 8) and Ground (pin 9). The voltage at I_P (pin 8) is constant ($\approx 1.3V$). Thus, a current through R_P is $I_P \approx \frac{1.3V}{R_P}$, as shown in Figure 5. $\frac{I_P}{I_O}$ is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25^\circ C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

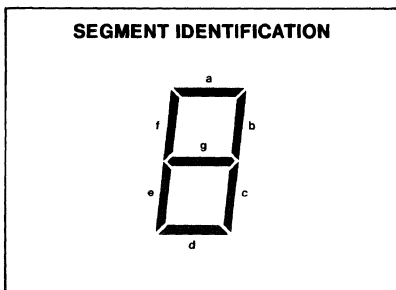
PARAMETER	TEST CONDITIONS	NE587			UNIT
		Min	Typ	Max	
$t_{D_{av}}$ Propagation delay Figure 2	From data to output		85		ns
$t_{D_{av}}$ Propagation delay Figure 3	From \overline{LE} to output		85		ns
t_W Latch enable pulse width Figure 4		85			ns
t_S Latch enable setup time Figure 4	From data to \overline{LE}	75			ns
t_H Latch enable hold time Figure 4	From \overline{LE} to data	0			ns

NOTE
 $t_{D_{av}} = \frac{1}{2} (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY	
	\overline{LE}	RBI	D ₃	D ₂	D ₁	D ₀	a	b	c	d	e	f	g	RBO		
—	H	*	X	X	X	X	STABLE								**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK	
0	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	H	6
7	L	X	L	H	H	H	L	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	H	E
12	L	X	H	H	L	L	L	L	L	H	L	L	L	H	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	H	blank
BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L	blank	

NOTES
 H = HIGH voltage level, output is "OFF"
 L = LOW voltage level, output is "ON"
 X = Don't care
 * The RBI will blank the display only if a binary zero is stored in the latches.
 ** $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.



NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_p , connected between r_p (pin 8) and Gnd (pin 9). The voltage at r_p (pin 8) is constant ($\approx 1.40V$). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_p , is 20 in the 15mA to 50mA range. Note that I_p must be derived from a resistor (R_p), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

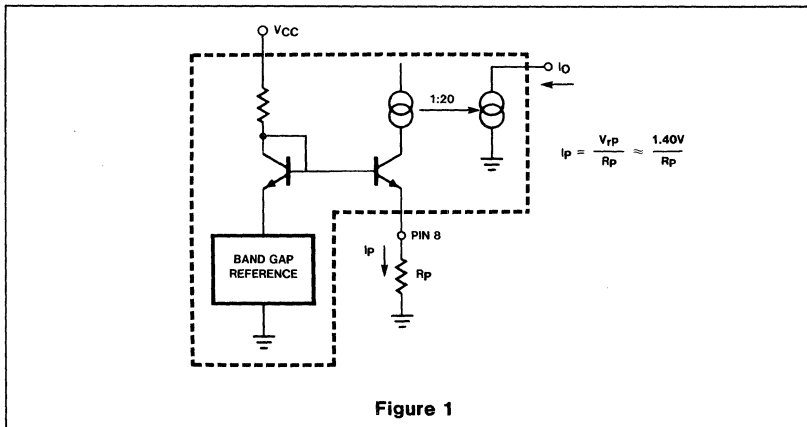


Figure 1

TIMING DIAGRAMS

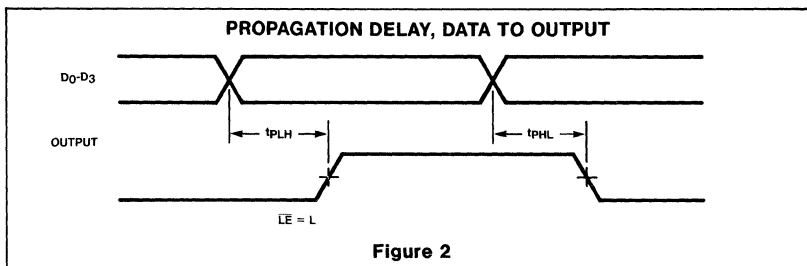


Figure 2

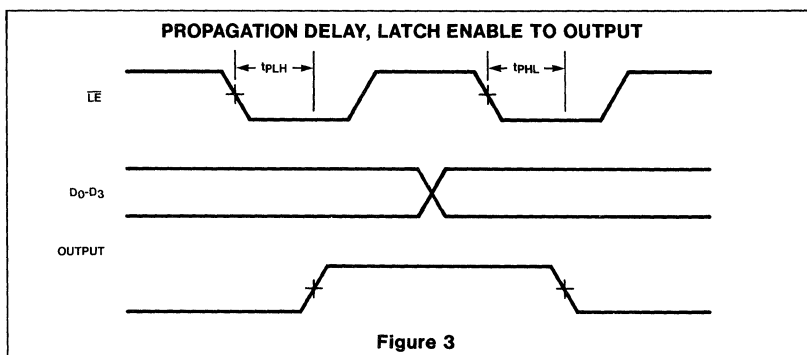


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

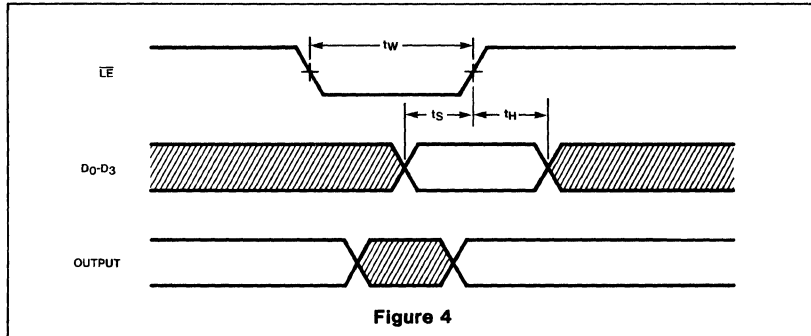
Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S . In many cases, these will be the same voltage. Necessary parameters are:

V_{CC} ,	Supply voltage to driver
V_S ,	Supply voltage to display
I_{CC} ,	Quiescent supply current of driver
I_{SEG} ,	LED segment current
V_F ,	LED segment forward voltage at I_{seg}
K_{DC} ,	% Duty cycle

V_F , the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)



These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC} \text{ mW}$$

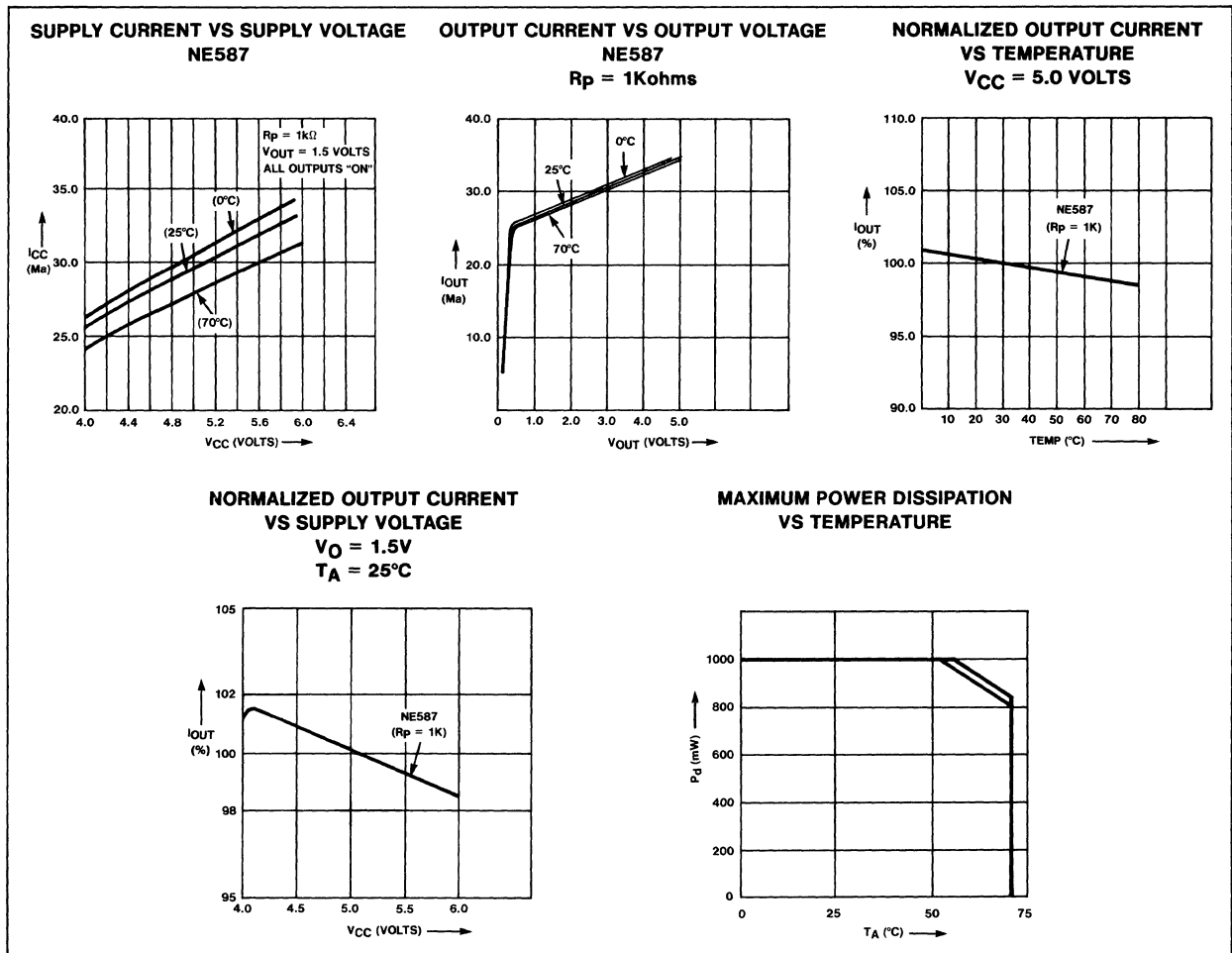
Assuming $V_S = V_{CC} = 5.25V$

$V_F = 2.0V$

$K_{DC} = 100\%$

$$P_d \text{ max} = 5.25 \times 50 + 3.25 \times 7 \times 30 \text{ mW} = 945 \text{ mW}$$

TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES (Cont'd)

OUTPUT CURRENT VS PROGRAM RESISTOR

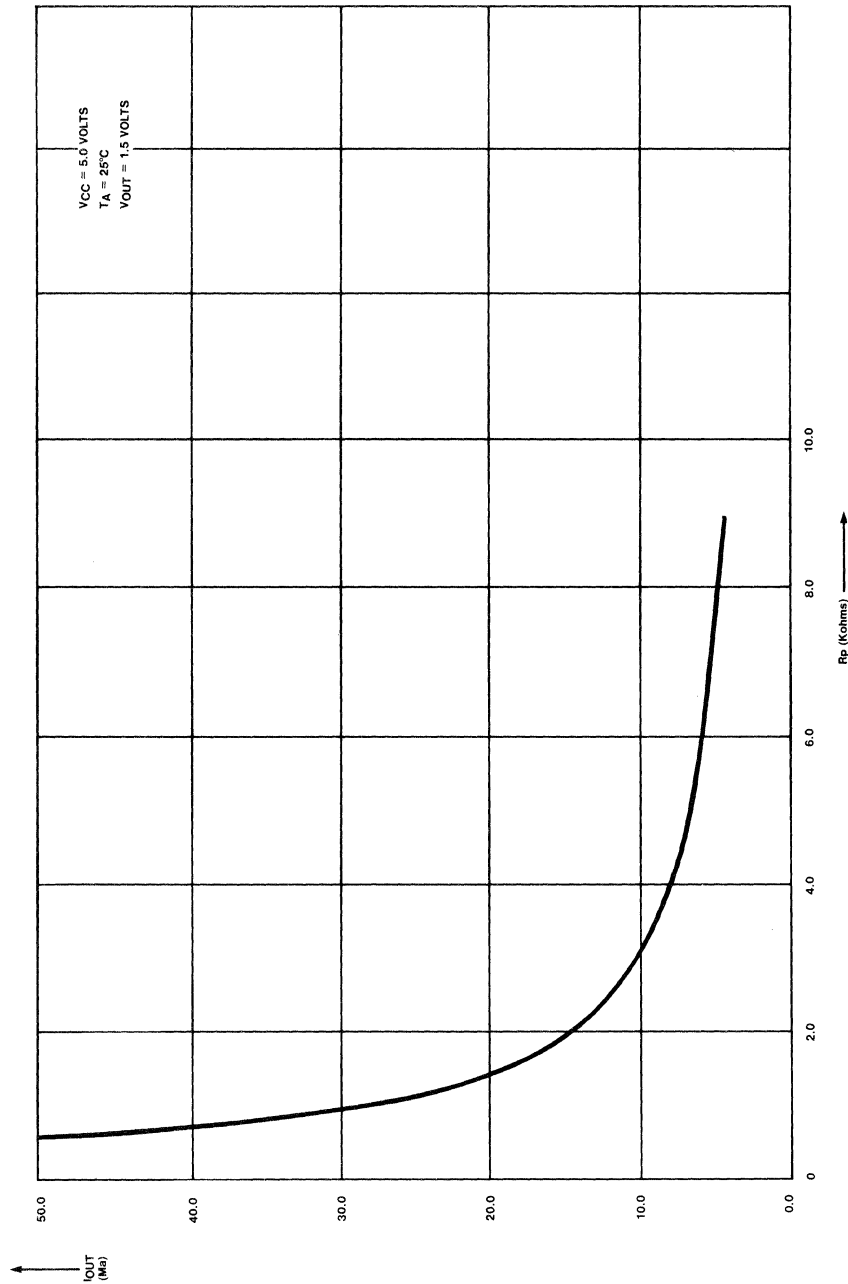
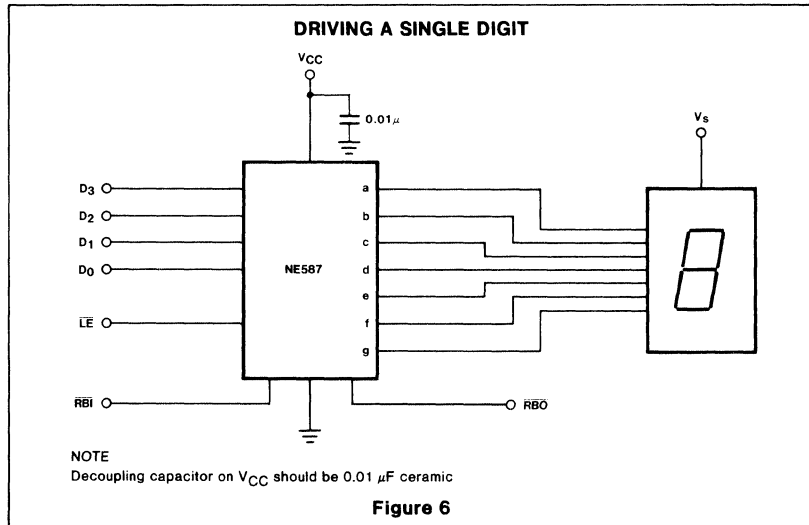


Figure 5

TYPICAL APPLICATIONS



However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d \text{ av}} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} \\ = 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d \text{ max}}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resis-

tor from V_{CC} to V_S . The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{\text{seg}}} \approx 10\Omega \text{ (}\frac{1}{2}\text{ W rating)}$$

assuming worst case I_{seg} of 30 mA

$$\text{Hence now } P_{d \text{ max}} = V_{CC} \times I_{CC} + (V_S - V_V - \\ R_X \times 7 \times I_{\text{seg}}) \times 7 \times I_{\text{seg}} \\ \times K_{DC} \\ = 5.25 \times 50 + 1.25 \times 7 \times 30 \\ \text{mW} \\ = 525 \text{ mW}$$

$$\text{and } P_{d \text{ av}} = 5.0 \times 30 + 1.25 \times 5 \times 25 \\ = 306 \text{ mW}$$

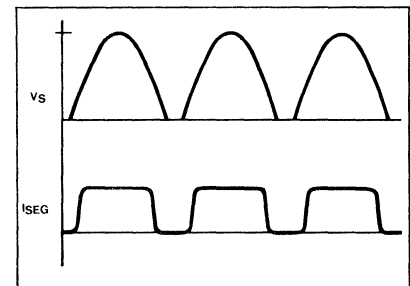
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_D, V_D \approx 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:

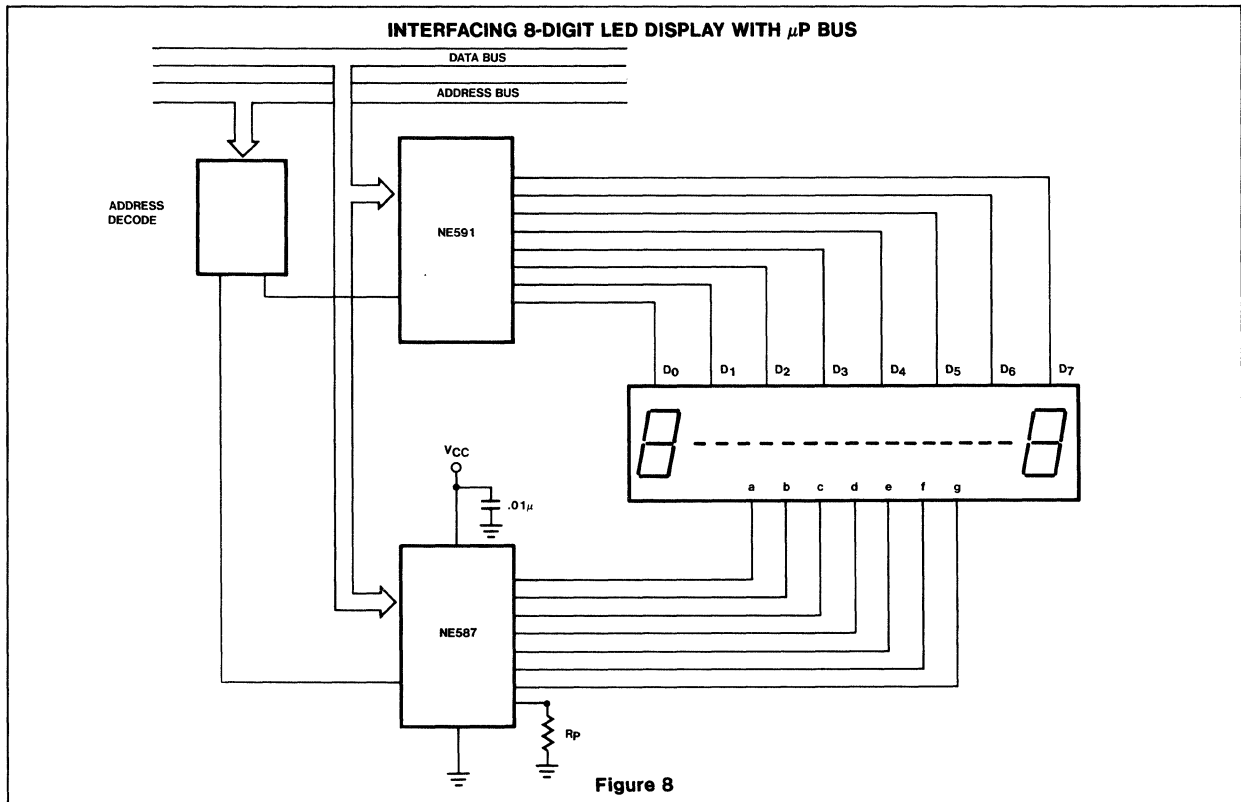
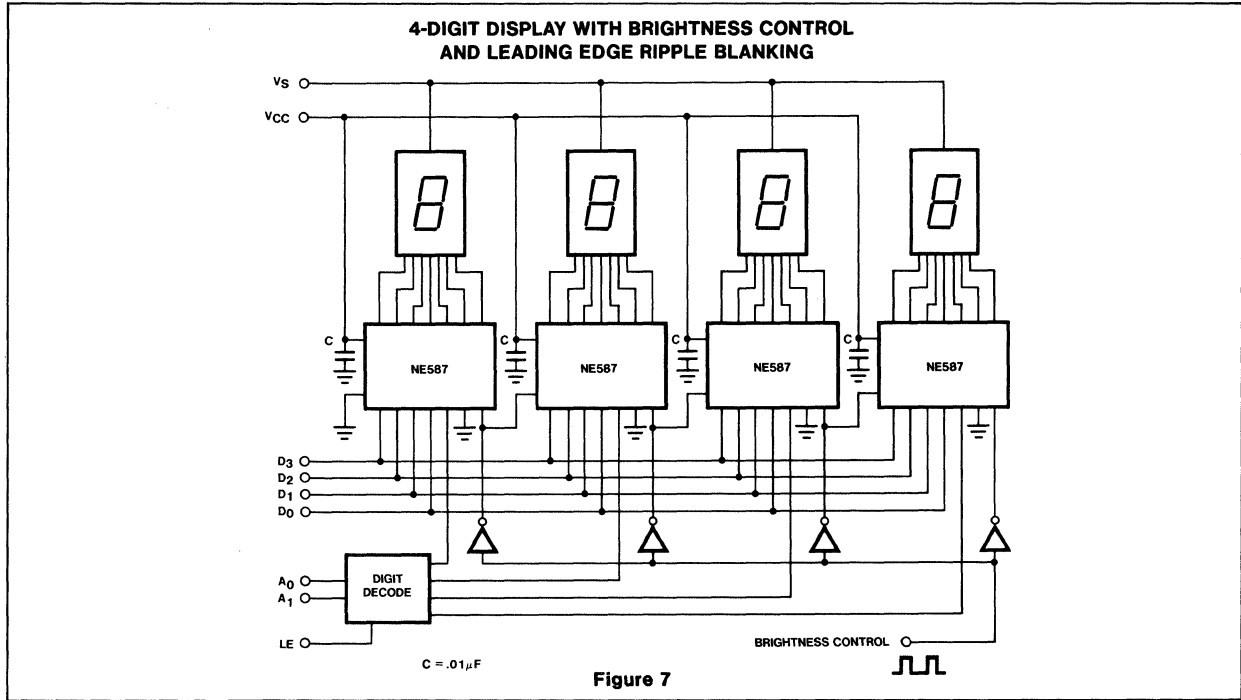


The duty cycle for this system depends upon V_S , V_F and the output characteristics of the display driver.

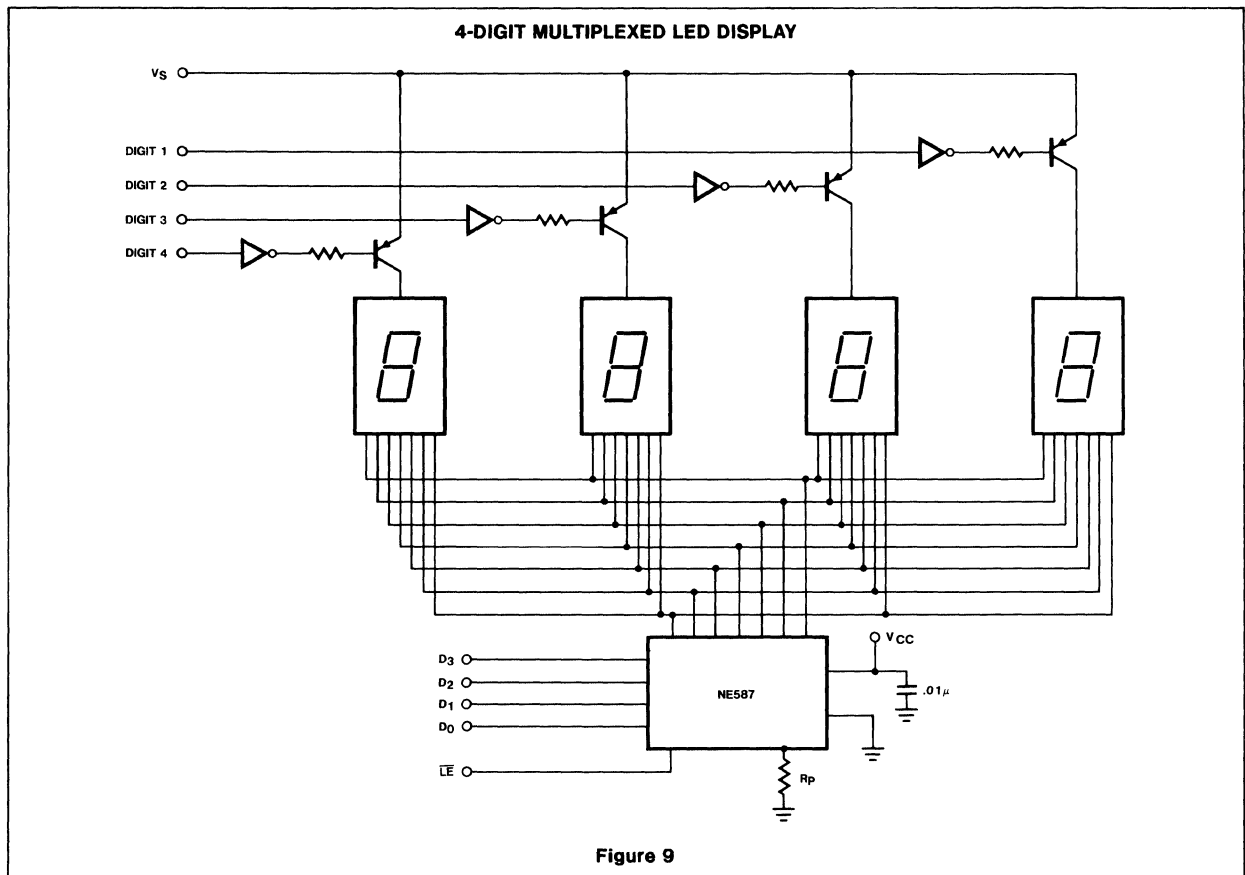
$$\text{With } \\ V_S = 4.9V \text{ pk.} \\ V_F = 2.0V$$

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)



TYPICAL APPLICATIONS (Cont'd)



DESCRIPTION

The NE589 is a latch / decoder / driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and \overline{LE} (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading and/or trailing edge zeros

APPLICATIONS

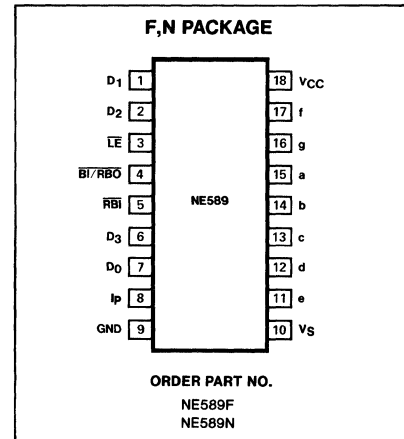
- Digital panel meters
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified

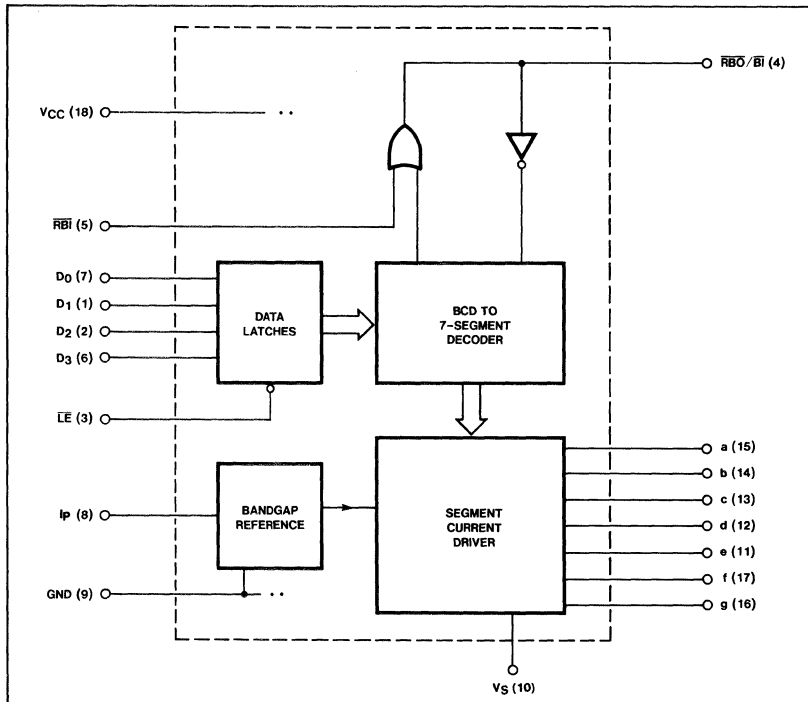
PARAMETER	RATING	UNIT
V_{CC}, V_S Supply voltage	-0.5 to +7	V
V_{IN} Input voltage ($D_0 - D_3, \overline{LE}, \overline{RBI}$)	-0.5 to +15	V
V_{OUT} Output voltage (a-g, RBO)	-0.5 to +7	V
P_D Power dissipation (25°C) ¹	1000	mW
T_A Ambient temperature range	0 to 70	$^\circ\text{C}$
T_J Junction temperature	150	$^\circ\text{C}$
T_{STG} Storage temperature range	-65 to +150	$^\circ\text{C}$
T_{SOLD} Soldering temperature (10 sec. max)	300	$^\circ\text{C}$

NOTE
Derate power dissipation as indicated
N package - $95^\circ\text{C}/\text{watt}$ above 55°C
F package - $100^\circ\text{C}/\text{watt}$ above 50°C

PIN CONFIGURATION



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 4.75$ to $5.25V$, $0^{\circ}C < T_A < 70^{\circ}C$.Typical values are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $R_p = 6k\Omega$ ($\pm 1\%$) unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE589			UNIT
		Min	Typ	Max	
V_{CC}	Operating supply voltage	4.75	5.00	5.25	V
V_{IH}	Input high voltage	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage			0.8	V
V_{IC}	Input clamp voltage			-1.5	V
I_{IH}	Input high current		0.1		μA
I_{IH}	Input high current		10		μA
I_{IL}	Input low current		-5 -200		μA
I_{IL}	Input low current		-0.7		mA
V_{OL}	Output low voltage				V
V_{OH}	Output high voltage		4.5		V
I_{OUT}	Output segment "ON" current	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current		20	250	μA
I_{CCO}	Supply current		25		mA
I_{CCI}	Supply current		30		mA

NOTE:

NE587 PROGRAMMING

The NE587 output current can be programmed, provided a program resistor, R_p , be connected between I_p (pin 8) and Ground (pin 9). The voltage at I_p (pin 8) is constant ($\approx 1.3V$). Thus, a current through R_p is $I_p \approx \frac{1.3V}{R_p}$, as shown in Figure 10. $\frac{I_o}{I_p}$ is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25^\circ C$ $R_L = 130\Omega$ $C_L = 30pF$ including probe capacity.

PARAMETER	TEST CONDITIONS	NE589			UNIT
		Min	Typ	Max	
$t_{D_{av}}$ Propagation delay Figure 2	From data to output		85		ns
$t_{D_{av}}$ Propagation delay Figure 3	From \overline{LE} to output		85		ns
t_W Latch enable pulse width Figure 4		85			ns
t_S Latch enable setup time Figure 4	From data to \overline{LE}	75			ns
t_H Latch enable hold time Figure 4	From \overline{LE} to data	0			ns

NOTE:

$$t_{D_{AV}} = \frac{1}{2} (t_{HL} + t_{LH})$$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	\overline{LE}	\overline{RBI}	D ₃	D ₂	D ₁	D ₀	a	b	c	d	e	f	g	\overline{RBO}	
—	H	*	X	X	X	X	STABLE								STABLE BLANK
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	L	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	L	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	L	H	H	L	H	c
13	L	X	H	H	L	H	L	L	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	blank

NOTES

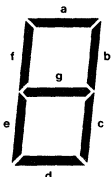
H = HIGH voltage level, output is "ON"

L = LOW voltage level, output is "OFF"

X = Don't care

* The \overline{RBI} will blank the display only if a binary zero is stored in the latches.** $\overline{RBO}/\overline{BI}$ used as an input overrides all other input conditions.

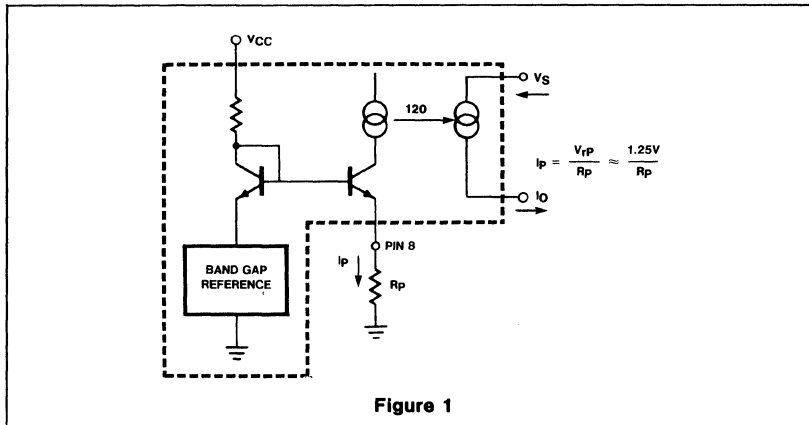
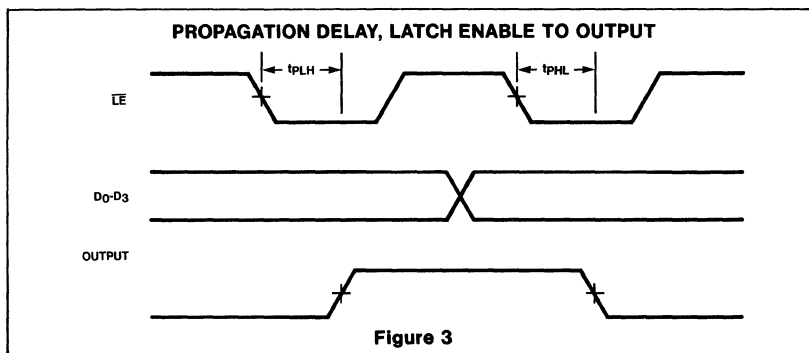
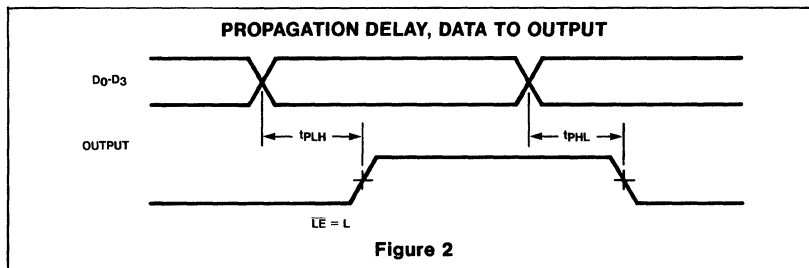
SEGMENT IDENTIFICATION



NE589 PROGRAMMING

NE589 output current can be programmed by using a programming resistor, R_p , connected between r_p (pin 8) and Gnd (pin 9). The voltage at r_p (pin 8) is constant ($\approx 1.25V$). A partial schematic of the voltage reference used in the NE589 is shown in figure 1.

Output current to program current ratio, I_O/I_p , is 20 in the 15mA to 50mA range. Note that I_p must be derived from a resistor (R_p), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

**TIMING DIAGRAMS****POWER DISSIPATION CONSIDERATIONS**

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

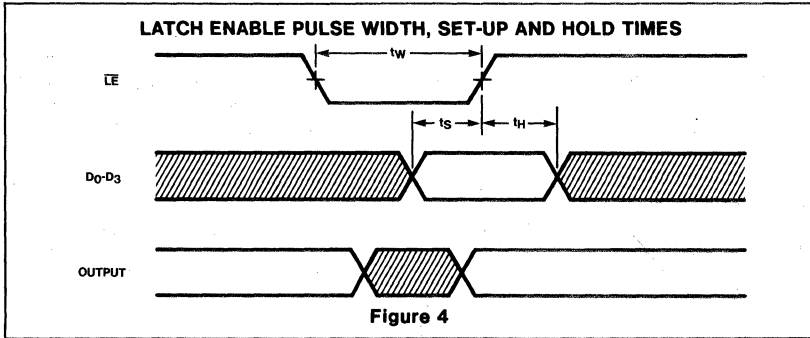
Power dissipation may be calculated as follows. Referring to figure 12, the two system power supplies are V_{CC} and V_S . In many cases, these will be the same voltage. Necessary parameters are:

V_{CC} ,	Supply voltage to driver
V_S ,	Supply voltage to display
I_{CC} ,	Quiescent supply current of driver
I_{SEG} ,	LED segment current
V_F ,	LED segment forward voltage at I_{seg}
KDC ,	% Duty cycle

V_F , the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)



These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC} \text{ mW}$$

Assuming $V_S = V_{CC} = 5.25V$

$V_F = 2.0V$

$K_{DC} = 100\%$

$$P_{d \text{ max}} = 5.25 \times 50 + 3.25 \times 7 \times 30 \text{ mW} = 945 \text{ mW}$$

TYPICAL PERFORMANCE CURVES

OUTPUT CURRENT VS OUTPUT VOLTAGE

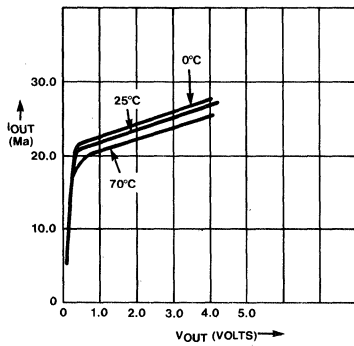


Figure 5

OUTPUT CURRENT VS OUTPUT VOLTAGE

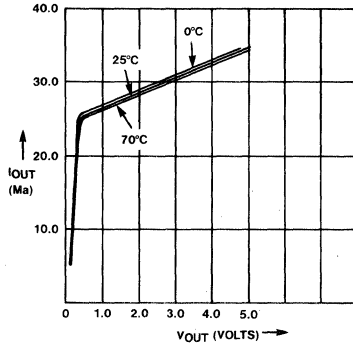


Figure 6

NORMALIZED OUTPUT CURRENT VS TEMPERATURE
 $V_{CC} = 5.0 \text{ VOLTS}$

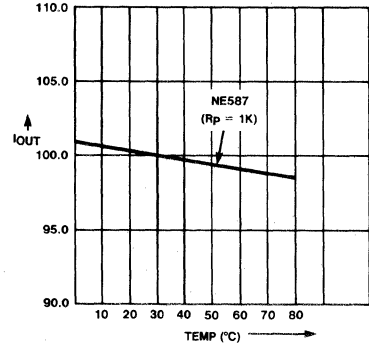


Figure 7

NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE V_{CC}
 $V_O = 1.5V$
 $T_A = 25^\circ C$

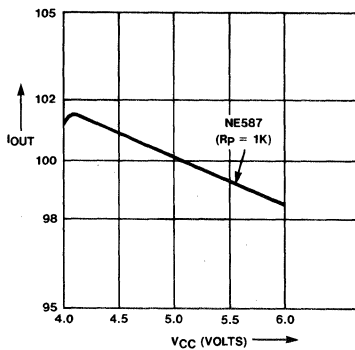


Figure 8

MAXIMUM POWER DISSIPATION VS TEMPERATURE

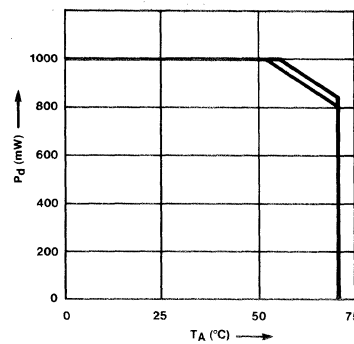


Figure 9

TYPICAL PERFORMANCE CURVES (Cont'd)

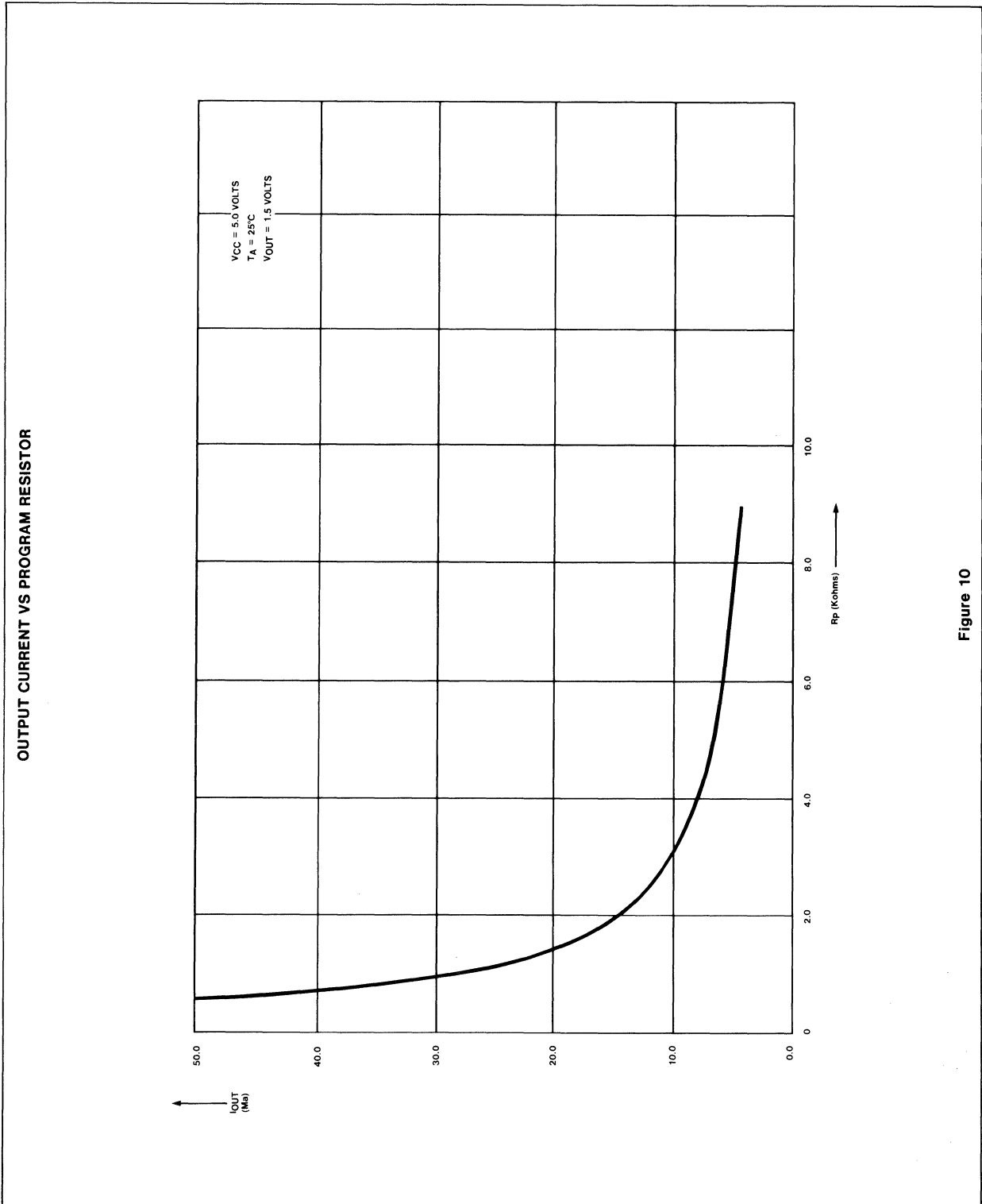


Figure 10



TYPICAL PERFORMANCE CURVES (Cont'd)

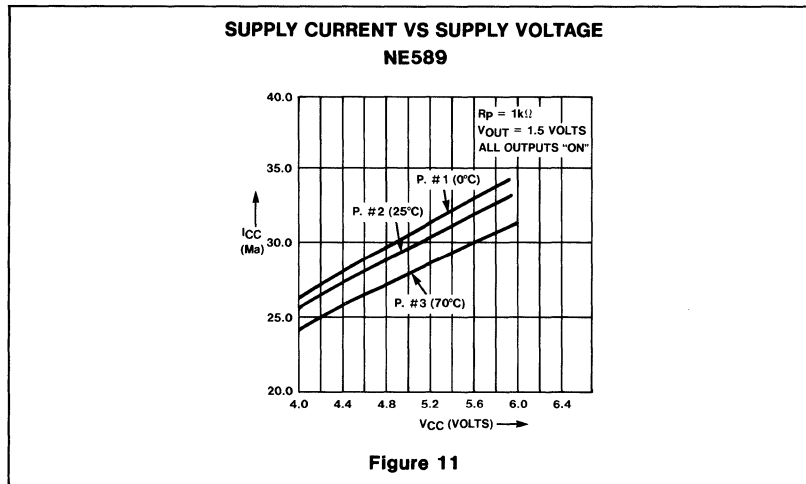
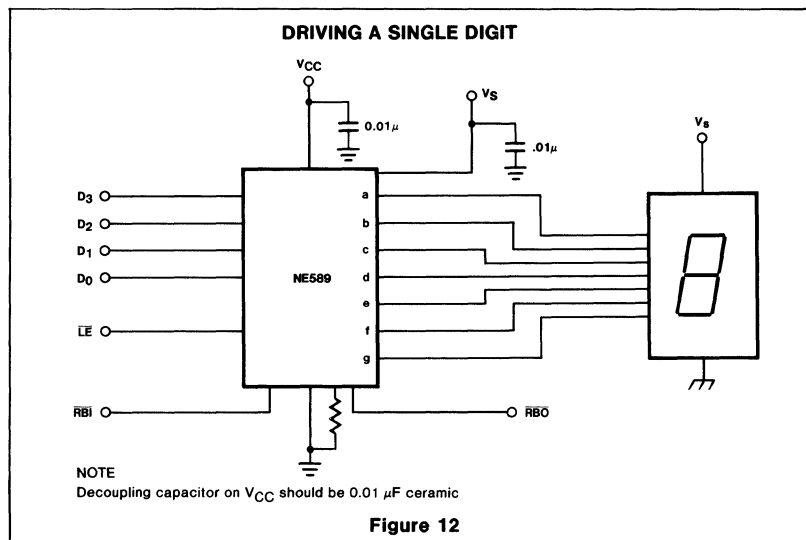


Figure 11

TYPICAL APPLICATIONS



NOTE
Decoupling capacitor on V_{CC} should be 0.01 μF ceramic

Figure 12

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\text{ av}} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} = 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation ($P_{d\text{ max}}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S . The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{\text{seg}}} \approx 10\Omega \text{ (}\frac{1}{2}\text{ W rating)}$$

assuming worst case I_{seg} of 30 mA

$$\begin{aligned} \text{Hence now } P_{d\text{ max}} &= V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{\text{seg}}) \times 7 \times X \times I_{\text{seg}} \\ &= 5.25 \times 50 + 1.25 \times 7 \times 30 \\ &= 525 \text{ mW} \end{aligned}$$

$$\text{and } P_{d\text{ av}} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306 \text{ mW}$$

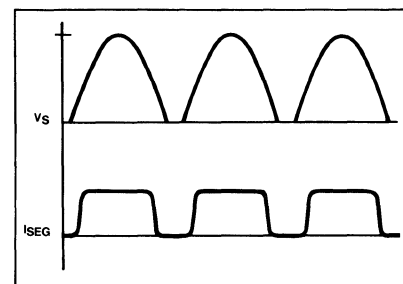
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_D, V_D \approx 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 15. For example a darlington PNP or NPN emitter follower may be preferable. Figure 14 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:

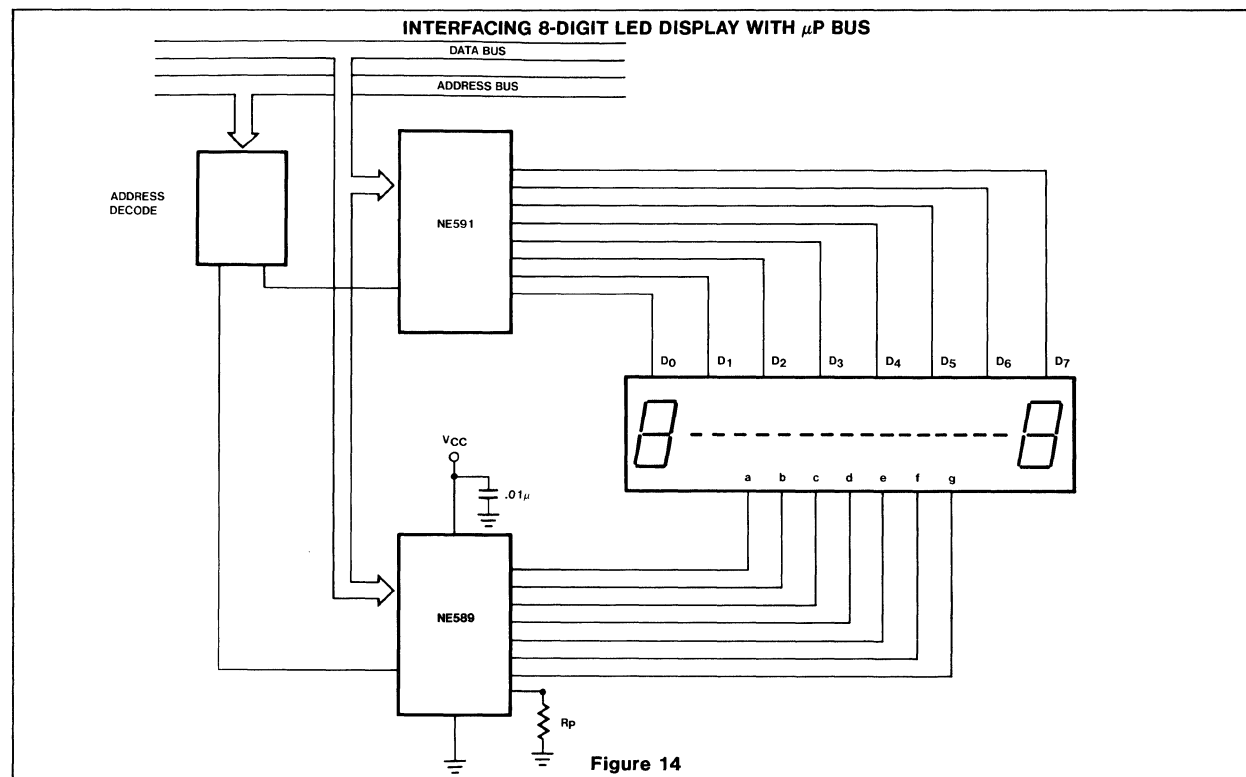
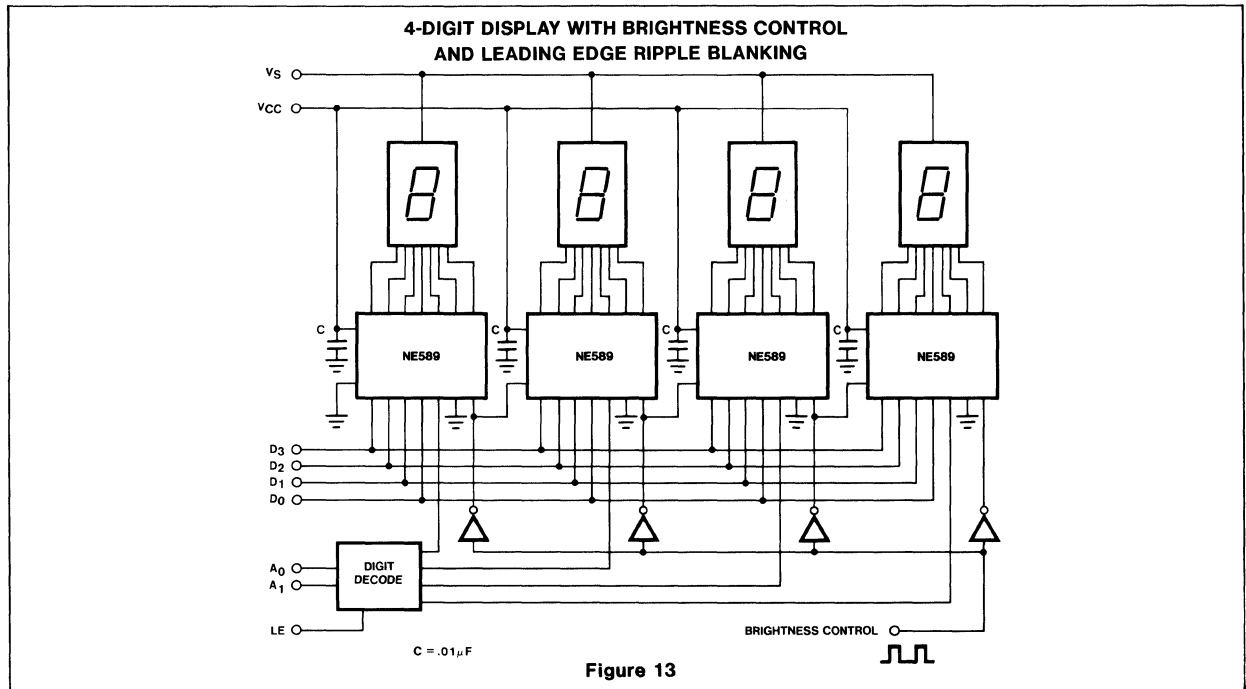


The duty cycle for this system depends upon V_S , V_F and the output characteristics of the display driver.

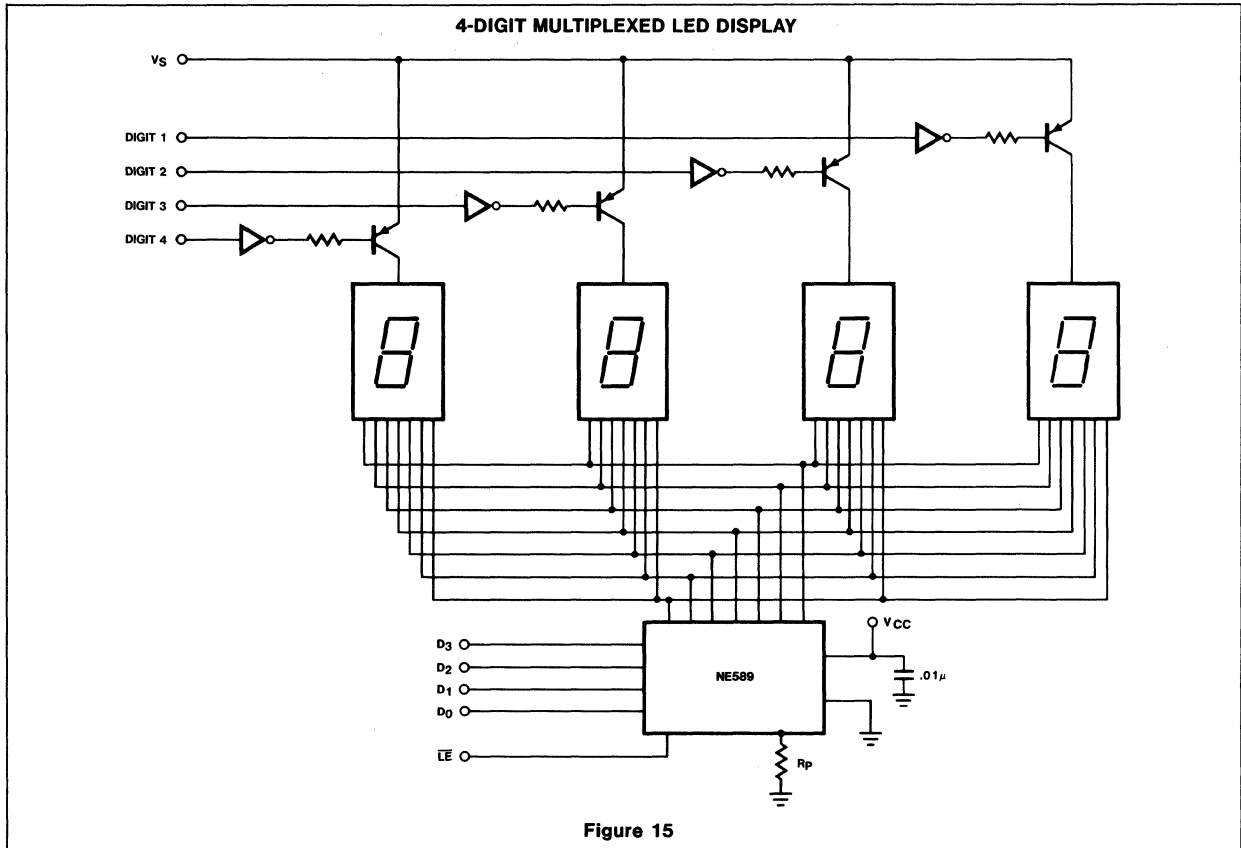
With
 $V_S = 4.9V \text{ pk.}$
 $V_F = 2.0V$

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)



TYPICAL APPLICATIONS (Cont'd)



DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

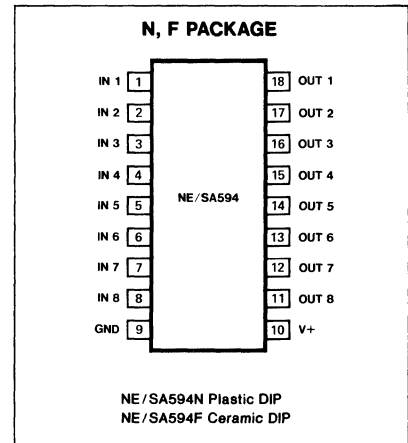
The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

- Digit and/or segment drivers
- Active output pull-down circuitry
- High output breakdown voltage
- Low supply voltage
- Input compatible with all logic outputs

PIN CONFIGURATION



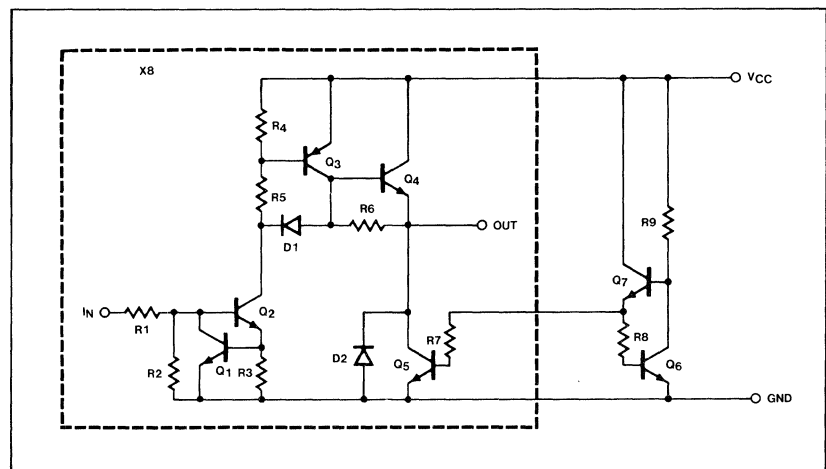
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER	RATING	UNIT	
VCC	Supply voltage	45	V
VOUT	Output voltage	VCC	
VIN	Input voltage	-0.3, +20	V
IOUT	Output current		
	Each output	50	mA
Pd	All outputs	200	mA
	Power dissipation* (at 25°C)	800	mW
TA	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
TSTG	Storage temperature range	-65 to +150	°C
TJ	Maximum junction temperature	150	°C
TSOLD	Lead soldering temperature (10 seconds)	300	°C

NOTE

*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $V_{CC} = +4.75$ to $+40V$, T_A (NE) = 0 to $70^\circ C$, T_A (SA) = -40 to $+85^\circ C$ unless otherwise stated.

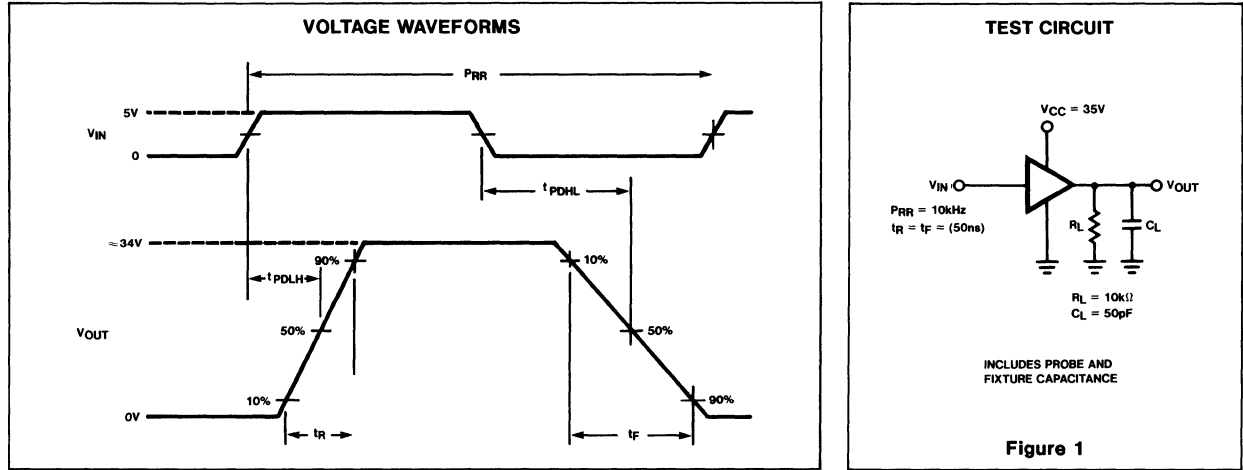
SA594	PARAMETER	TEST CONDITIONS	NE/SA594			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range		4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	$V_{CC} = 40V$ $V_{IN} = 3.5V$		3	6	mA
I_{CCL}	Supply current (all outputs low)	$V_{CC} = 40V$ $V_{IN} = 0.4V$		0.4	1	mA
V_{IN}	Input voltage range		0		15	V
V_{IH}	Input voltage to ensure logic '1'		2.6			V
V_{IL}	Input voltage to ensure logic '0'				0.8	V
I_{IH}	Input current to ensure logic '1'		100		10	μA
I_{IL}	Input current to ensure logic '0'			60	130	μA
I_{IN}	Input current	$V_{IN} = 2.6V$ $V_{IN} = 5.0V$ $V_{IN} = 15.0V$		180	330	μA
V_{OH}	Output high voltage	$V_{IN} = 3.5V$ $T_A = 25^\circ C$	$V_{CC}-1.5$	$V_{CC}-1.1$		V
		$I_{OUT} = -25mA$ Over Temp.	$V_{CC}-2$	$V_{CC}-1.3$		V
		V_{OUT} with respect to V_{CC}				
V_{OH}	Output high, <i>no load</i> voltage	$V_{IN} = 3.5V$ $I_{OUT} = 0$, $T_A = 25^\circ C$ V_{OUT} with respect to V_{CC}	$V_{CC}-1$	$V_{CC}-0.8$		V
V_{OFF}	Output 'OFF' voltage level	$V_{IN} = 0.8V$ $I_{OUT} = 0$		10	200	mV
I_{OH}	Available output current	$V_{CC} = 35V$ $V_{IN} = 3.5V$ $V_{OUT} = 30V$ $T_A = 25^\circ C$	-35			mA
I_{OUT}	Output pulldown current	$V_{CC} = V_{OUT} = 35V$ Inputs open	100	200	400	μA
I_{CEX}	Output leakage current	$T_A = 25^\circ C$ $V_{IN} = 0.4V$ $V_{CC} = 40V$, $V_{OUT} = 0V$		-1		μA

AC ELECTRICAL CHARACTERISTICS¹ $V_{CC} = 35V$, $T_A = 25^\circ C$

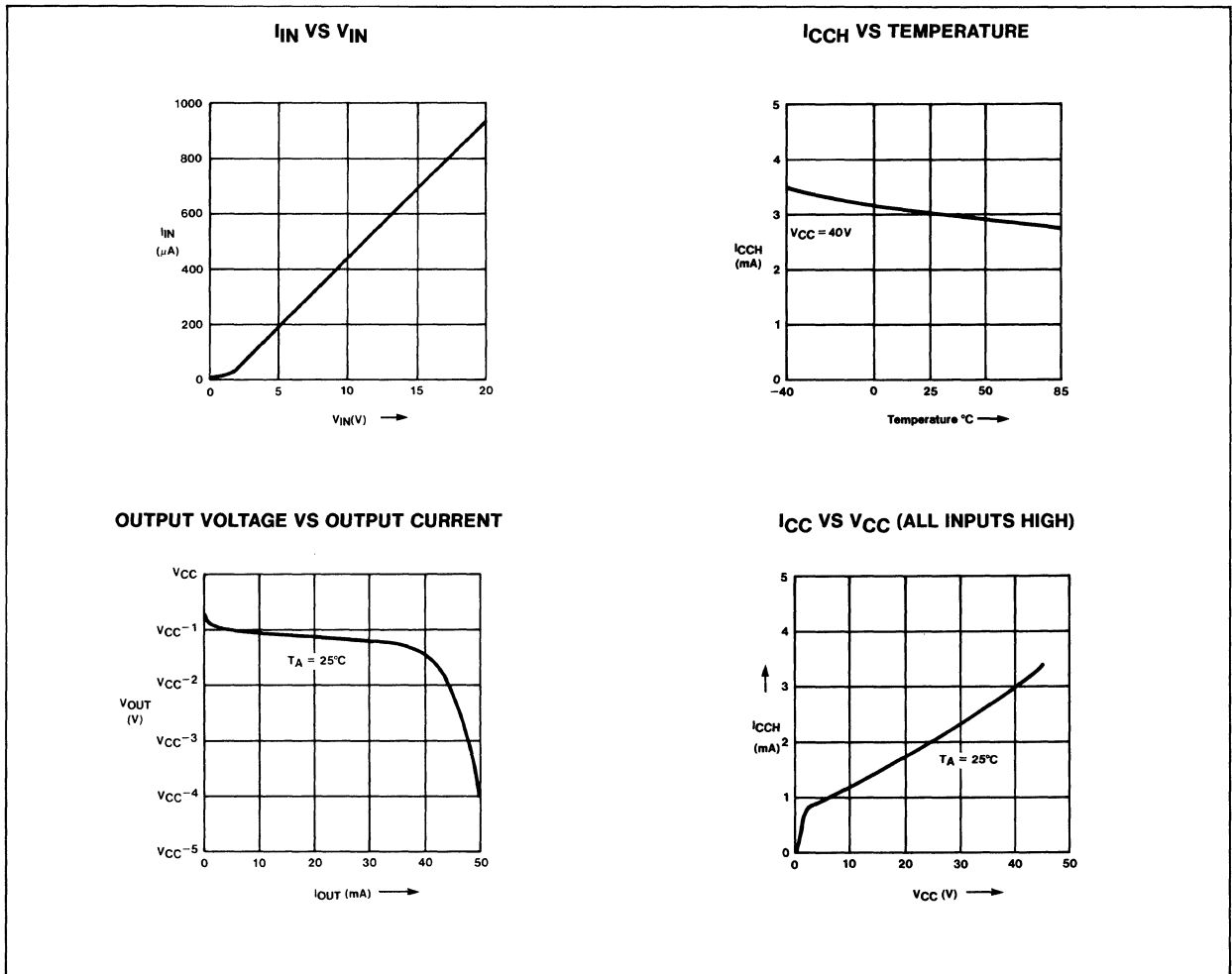
PARAMETER	TEST CONDITIONS	NE/SA594			UNIT
		Min	Typ	Max	
t_{pDLH}	Propagation delay - low to high output transition.		1	5	μS
t_{pDHL}	Propagation delay - high to low output transition.		3	10	μS
t_R	Output rise time		0.5	3	μS
t_F	Output fall time		1.5	5	μS

NOTE
1. See figure 1

SWITCHING TIMES OF DRIVERS



TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATION
DIGITAL CLOCK WITH ALARM

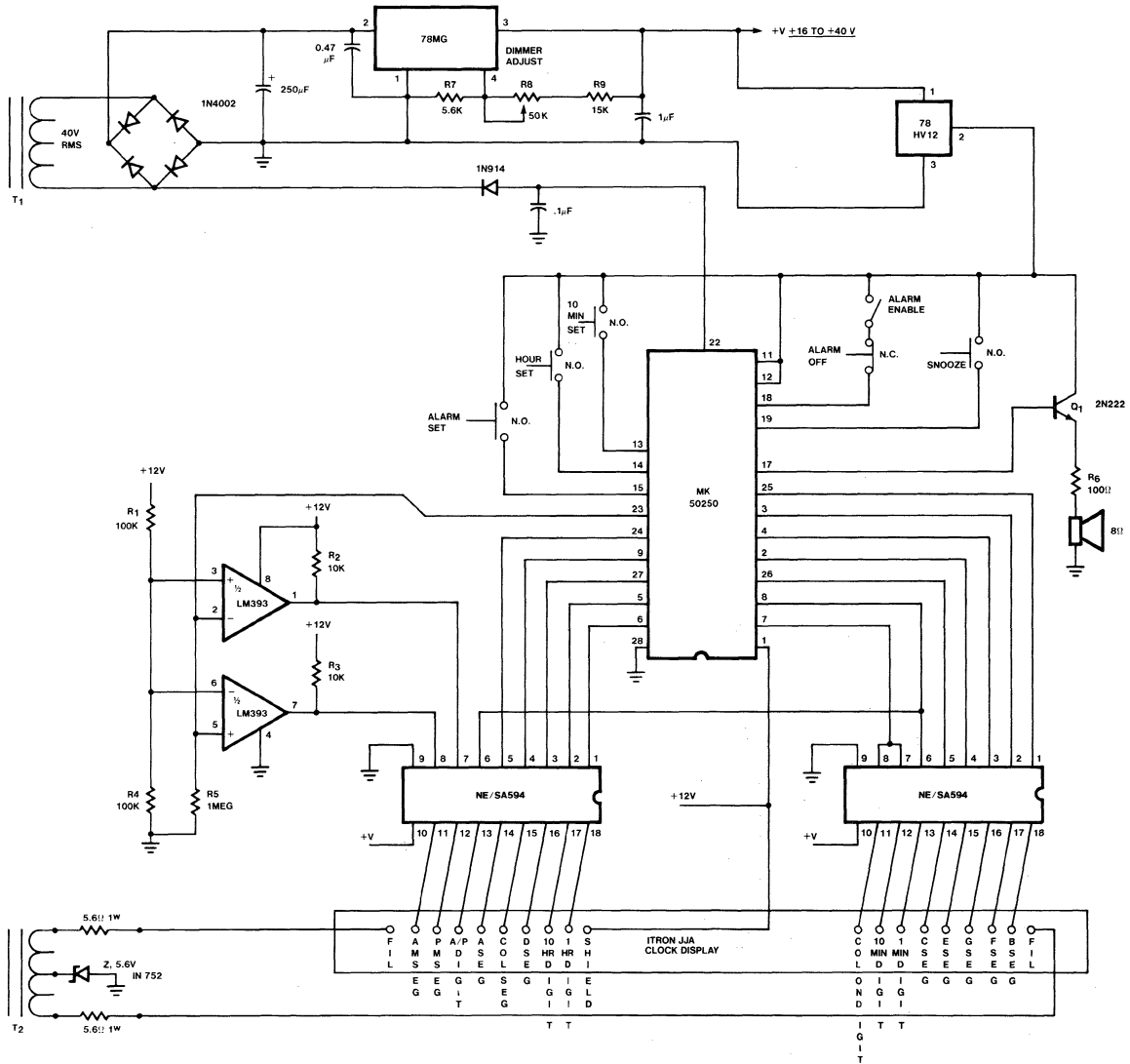


Figure 2

VACUUM FLUORESCENT DISPLAY DRIVER

NE/SA594

NE/SA594-N.F

SECTION 10 DATA ACQUISITION

Section 10—DATA ACQUISITION

DAC-08 SERIES	8-Bit High Speed Multiplying D/A Converter	313
LF398	Monolithic Sample and Hold Circuits	303
MC1508-8/1408-8/1408-7	8-Bit Multiplying D/A Converter	307
NE5007/5008/SE5008	8-Bit High Speed Multiplying D/A Converter	313
NE/SE5009	8-Bit High Speed Multiplying D/A Converter	318
NE/SE5018	8-Bit Microprocessor-Compatible D/A Converter	325
NE/SE5019	8-Bit Microprocessor-Compatible D/A Converter	330
NE/SE5118	8-Bit Microprocessor-Compatible D/A Converter-Current Output	335
NE/SE5119	8-Bit Microprocessor-Compatible D/A Converter-Current Output	339
NE5020	10-Bit Microprocessor-Compatible D/A Converter	343
NE/SE5537	Sample and Hold Amplifier	351

A/D-D/A CONVERTERS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Accuracy

The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale; 1 LSB for any bit combination.

Monotonicity

For a 1 LSB increase of input code, the output either increases or remains the same.

Differential Linearity

The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB and with a tempo of essentially zero.

Absolute Accuracy

Error of a D/A converter output is the difference between the analog output expected and the actual output with a given code applied. Error of an A/D converter is the difference between the theoretical analog output required to produce a given output code and the actual input required to produce a given output code and the actual input required to produce that same code. The actual input is a range and the measured value is the midpoint of the measured band and the theoretical midpoint.

Resolution

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2ⁿ when n is

the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Quantizing Error

In an A/D converter, there is an infinite number of possible input voltages, but only 2ⁿ output codes (n = number of bits). Therefore, there will be an error as great as 1/2LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

No Missing Codes

This is a property of an A/D converter that is related to, but is more stringent than monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

Most Significant Bit (MSB)

The highest-order bit or the bit with the greatest weight.

Least Significant Bit (LSB)

The lowest-order bit or the bit with the least weight.

Gain Error

The error in the input-to-output ratio, usually expressed in percent.

Offset Error

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a D/A output or an A/D input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

Settling Time

The time delay between a change of input signal value and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to arrive at, and remain within, a certain error band around the final value and is often given for several different magnitudes of input step change.

Conversion Time

Time required for a complete measurement by an A/D converter. Conversion times are a function of the number of bits (resolution) and the clock frequency.

Switching Time

The time it takes for a multiplexer to change from one channel to the next with the new output signal being within a certain percentage of its final value. It is expressed for a maximum voltage transition.

Throughput Rate

An A/D converter or a data acquisition system has a finite number of points that it can convert in any given time. Throughput rate is an expression of that quantity. It is dependent on the time it takes to make a conversion and the time required to set up to make the next conversion. In a data acquisition system this time includes the composite delay due to switching and settling times of the mux, settling time of the amplifier and acquisition time of the sample-and-hold.

Full Scale Tempco

The change in DAC full scale current with change in temperature expressed in ppm/°C.

Differential Non-Linearity Tempco

The non-linearity specification over a specified range of temperatures. This specification generally appears as the range of tem-



A/D-D/A CONVERTERS DEFINITIONS (Cont'd)

peratures that the device is monotonic (DAC) or has no missing codes (ADC).

Leakage Current

Multiplexer input current that does not flow through to the output but is shunted internally. It is also current that flows from OFF channels into the ON channel. In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

Power Supply Sensitivity

The change in DAC output current with changes in power supply voltage.

Output Voltage Compliance

The range of allowable voltage levels the output pins can assume without a major effect on circuit performance.

Compliance Voltage Range

For a current source the maximum range of terminal voltage for which the current source will maintain its specified values.

NOTE

Refer to Section 5 (Interface Circuits) of the 1979 Analog Applications Manual for an in-depth explanation of Converters and their applications

SIGNETICS D/A CONVERTER SELECTION GUIDE

PRODUCT	# BITS	ACC. %	OUTPUT			INT. REF.	INT. LATCH	PACKAGE		TEMPERATURE RANGE		RELIABILITY	
			V	I	T			N	F	ComL	MII	SURE II	SUPR II
MC1408-6	8	.78		X				X	X	X		X	
MC1408-7	8	.39		X				X	X	X		X	X
MC1408-8	8	.19		X				X	X	X		X	X
MC1508-8	8	.19		X					X		X	X	X
NE5007	8	.39		X	X			X	X	X		X	X
NE5008	8	.19		X	X			X	X	X		X	X
NE5009	8	.1		X	X			X	X	X		X	X
SE5008	8	.19		X	X				X		X	X	X
SE5009	8	.1		X	X				X		X	X	X
NE5018	8	.19	X			X	X	X	X	X		X	X
NE5019	8	.1	X			X	X	X	X	X		X	X
SE5018	8	.19	X			X	X		X		X	X	X
SE5019	8	.1	X			X	X		X		X	X	X
NE5118	8	.19		X		X	X	X	X	X		X	
NE5119	8	.1		X		X	X	X	X	X		X	
SE5118	8	.19		X		X	X		X		X	X	
SE5119	8	.1		X		X	X		X		X	X	
NE5020	10	.1	X			X	X	X	X	X		X	

SIGNETICS REPLACEMENT STANDARDS

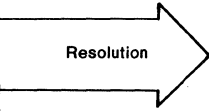
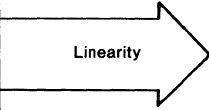
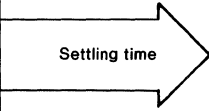
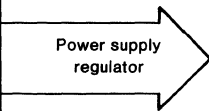
SE/NE 5018 DAC

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD	8	Resolution (Bits)	8	NE5018 SE5018 NE5019 SE5019	Yes Yes Yes Yes	Yes Yes Yes Yes	*Not pin for pin replacement. Do not have total capability of the NE5018 μ P compatible series.
Analog Devices			Bits				
Datel	.19	Linearity	0.1				
Fairchild			%				
Harris			2- 300 μ sec	Settling Time $\frac{1}{2}$ LSB	2		
Precision					μ sec		
National	10-50	Gain TC	20				
			PPM / °C				
	0-4	Current (Output)		NE / SE 5118 NE / SE 5119	Yes Yes	Yes Yes	
			mA				
	-10 to +18	Voltage (Output)	0-10 ± 5	NE5018 SE5019	Yes Yes	Yes Yes	
			Volts				



SIGNETICS REPLACEMENT STANDARDS

DAC-08/08A

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD Analog Devices Datel Motorola National	8	Resolution 	8	NE/SE5008 NE/SE5009	Yes	Yes	
					Yes	Yes	
	.19	Linearity 	19	NE/SE5008 NE/SE5009	Yes	Yes	
			%FS		Yes	Yes	
	85-300	Settling time 	135	NE/SE5008 NE/SE5009	Yes	Yes	
			nsec		Yes	Yes	
	48-500	Power supply regulator 	48	NE/SE5008 NE/SE5009	Yes	Yes	
			mW		Yes	Yes	

DESCRIPTION

The Signetics LF398 is a monolithic sample and hold circuit which utilizes high-voltage lon-Inplant JFET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.004% typical and acquisition time is as low as 6 μ s to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF398 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of 10¹⁰ Ω allows high source impedances to be used without degrading accuracy.

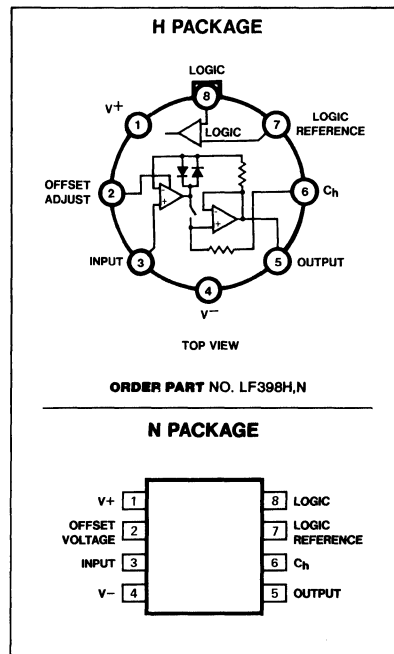
P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1 μ F hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs on the LF398 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF398 will operate from \pm 5V to \pm 18V supplies. It is available in an 8-lead TO-5 package or an 8-pin plastic DIP.

FEATURES

- Operates from \pm 5V to \pm 18V supplies
- Less than 10 μ s acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at C_h = 0.01 μ F
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- The LF398 is ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup.

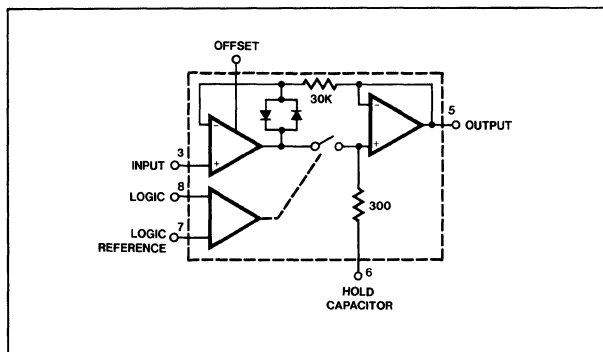
PIN CONFIGURATION



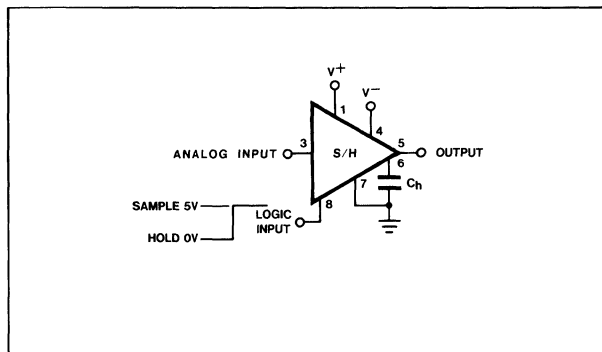
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	\pm 18	V
Power dissipation (package limitation) ¹	500	mW
Operating ambient temperature range LF398	0 to +70	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage ²	+7, -30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	$^{\circ}$ C

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25^\circ C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

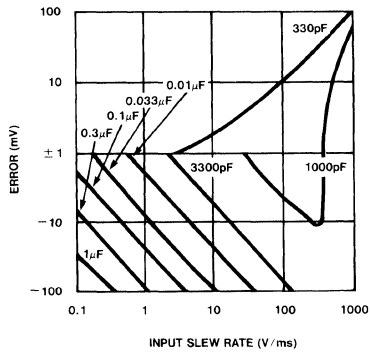
PARAMETER	TEST CONDITIONS	LF398			UNIT
		Min	Typ	Max	
Input offset voltage ⁶	$T_j = 25^\circ C$ Full temperature range		2	7	mV
				10	mV
Input bias current ⁶	$T_j = 25^\circ C$ Full temperature range		10	50	nA
				100	nA
Input impedance	$T_j = 25^\circ C$		10^{10}		Ω
Gain error	$T_j = 25^\circ C$, $R_L = 10K$ Full temperature range		0.004	0.01	%
				0.02	%
Feedthrough attenuation ratio at 1kHz	$T_j = 25^\circ C$, $C_h = 0.01\mu F$	80	90		dB
Output impedance	$T_j = 25^\circ C$, "HOLD" mode Full temperature range		0.5	4	Ω
				6	Ω
"HOLD" step ⁴ Supply current ⁶	$T_j = 25^\circ C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$ $T_j \geq 25^\circ C$		1.0	2.5	mV
			4.5	6.5	mA
Logic and logic reference input current	$T_j = 25^\circ C$		2	10	μA
Leakage current into hold capacitor ⁶	$T_j = 25^\circ C^5$ Hold mode		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4		μs
			20		μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_j = 25^\circ C$	0.8	1.4	2.4	V

NOTES

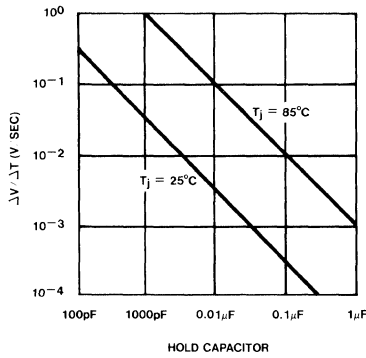
1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θ_{JA}) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25^\circ C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k$. Logic reference voltage = 0V and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01 μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ± 5 to $\pm 18V$.

TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

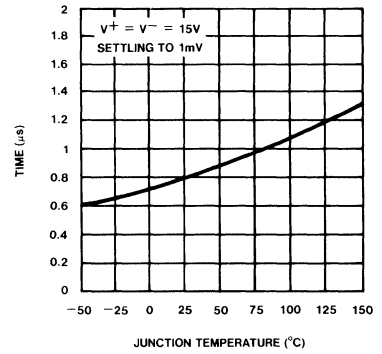
DYNAMIC SAMPLING ERROR



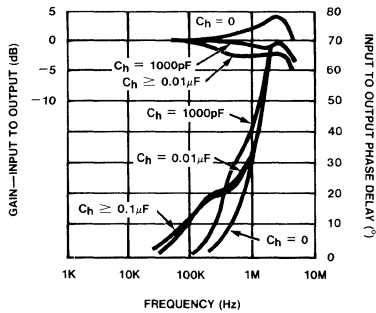
OUTPUT DROOP RATE



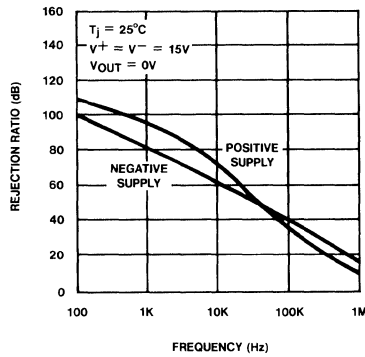
"HOLD" SETTLING TIME



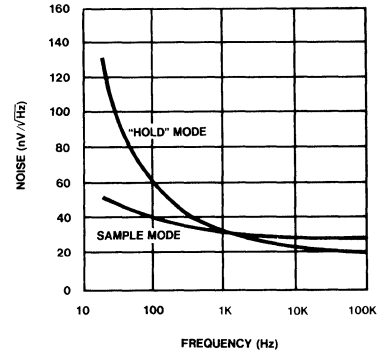
PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)



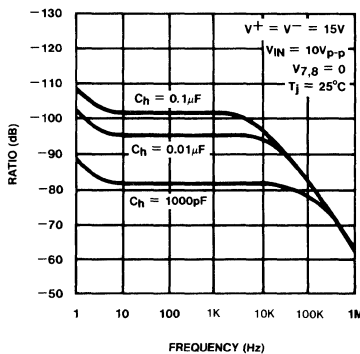
POWER SUPPLY REJECTION



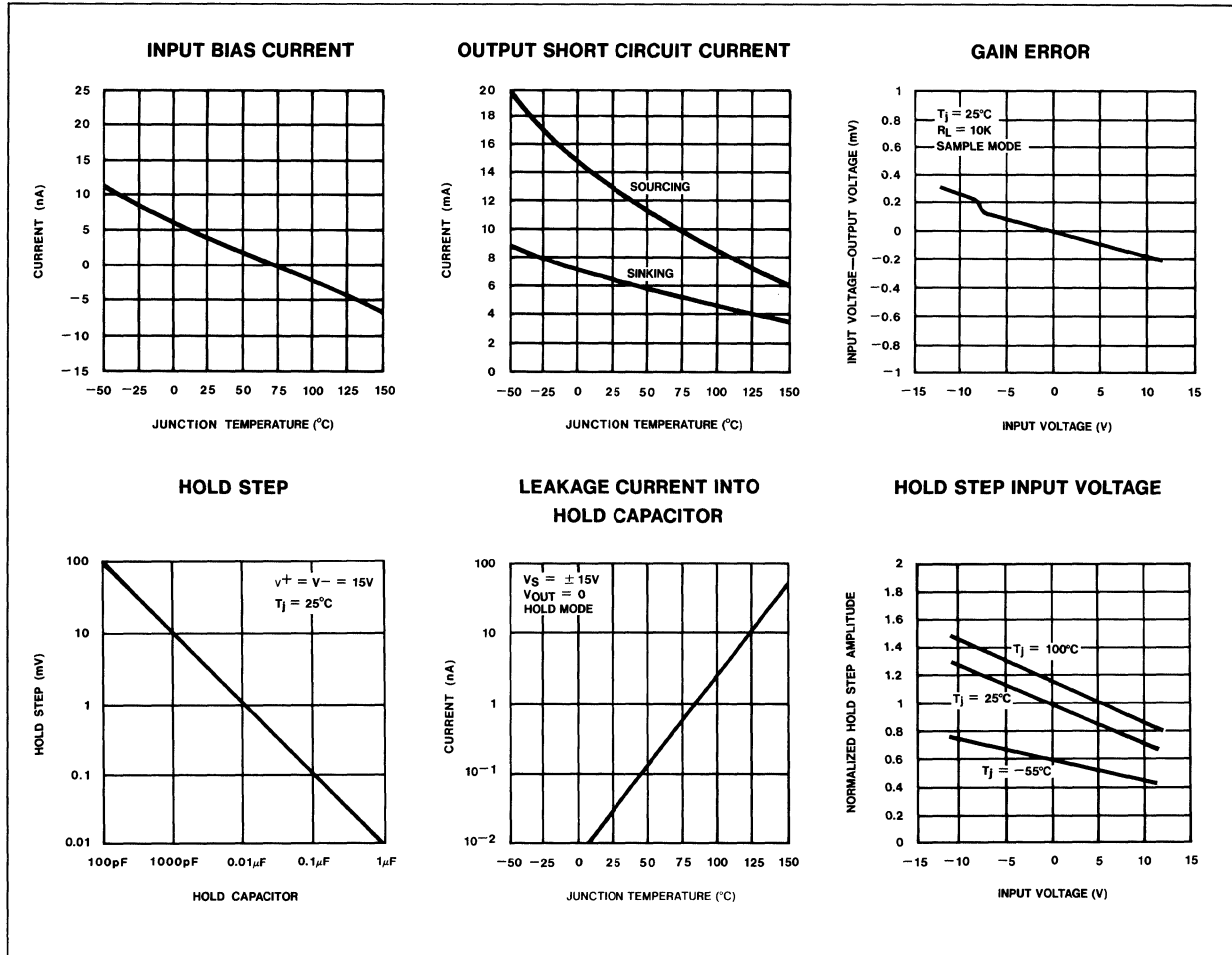
OUTPUT NOISE



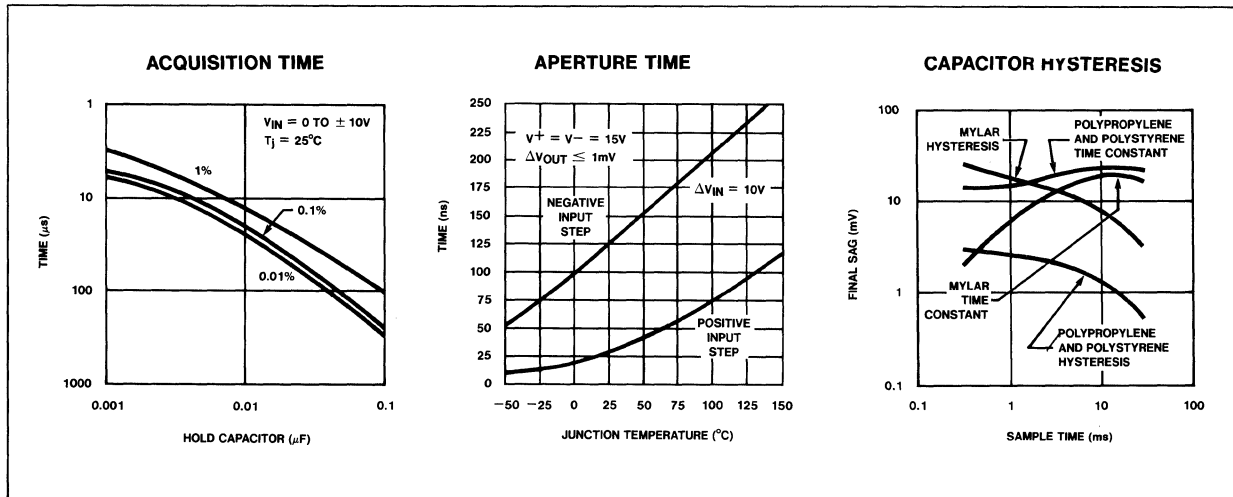
FEEDTHROUGH REJECTION RATIO (HOLD MODE)



TYPICAL DC PERFORMANCE CHARACTERISTICS



TYPICAL AC PERFORMANCE CHARACTERISTICS



DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

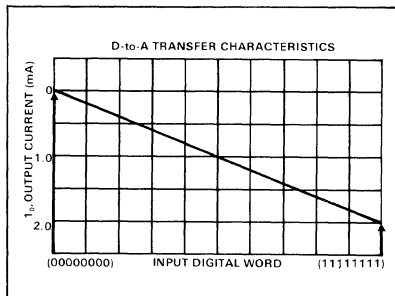
FEATURES

- **Fast settling time—300ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High speed multiplying rate 4.0mA/μs (input slew)**
- **Output voltage swing +5V to -5.0V**
- **Standard supply voltages + 5.0V and -5.0V to -15V**
- **Military qualifications pending**

APPLICATIONS

- Tracking A-to-D converters
- 2½-digit panel meters and DVM's
- Waveform synthesis
- Sample and hold
- Peak detector
- Programmable gain and attenuation
- CRT character generation
- Audio digitizing and decoding
- Programmable power supplies
- Analog-digital multiplication
- Digital-digital multiplication
- Analog-digital division
- Digital addition and subtraction
- Speech compression and expansion
- Stepping motor drive

TYPICAL PERFORMANCE CHARACTERISTICS



CIRCUIT DESCRIPTION

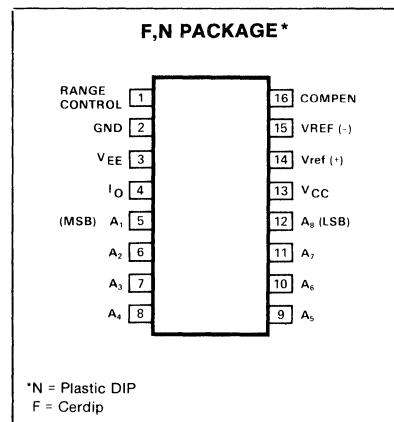
The MC1508/MC1408 consists of a reference current amplifier, and R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

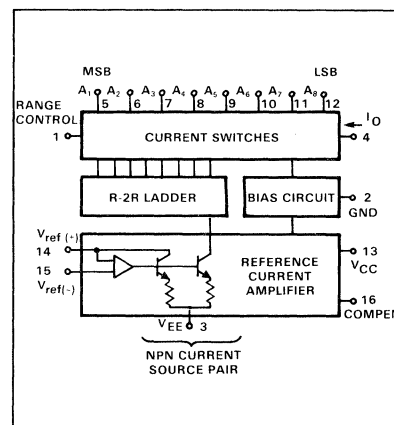
The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise specified

PARAMETER	RATING	UNIT
V _{CC}	Power supply voltage	
V _{EE}	Positive	+5.5
V _{5-V12}	Negative	-16.5
V _O	Digital input voltage	+5.5, 0
I ₁₄	Applied output voltage	+0.5, -5.2
V _{14,V15}	Reference current	5.0
	Reference amplifier inputs	V _{CC} , V _{EE}
P _D	Power dissipation (package limitation)	
	Ceramic package	1000
	Plastic package	800
T _A	Operating temperature range	
	MC1508	-55 to +125
	MC1408	0 to +75
T _{stg}	Storage temperature range	-65 to +70

MC1508-8/MC1408-8/MC1408-7 -F,N

Pin 3 must be 3V more negative than the potential to which R₁₅ is returned.

DC ELECTRICAL CHARACTERISTICS¹ V_{CC} = +5.0Vdc, V_{EE} = -15Vdc, $\frac{V_{ref}}{R_{14}} = 2.0mA$
 unless otherwise specified.

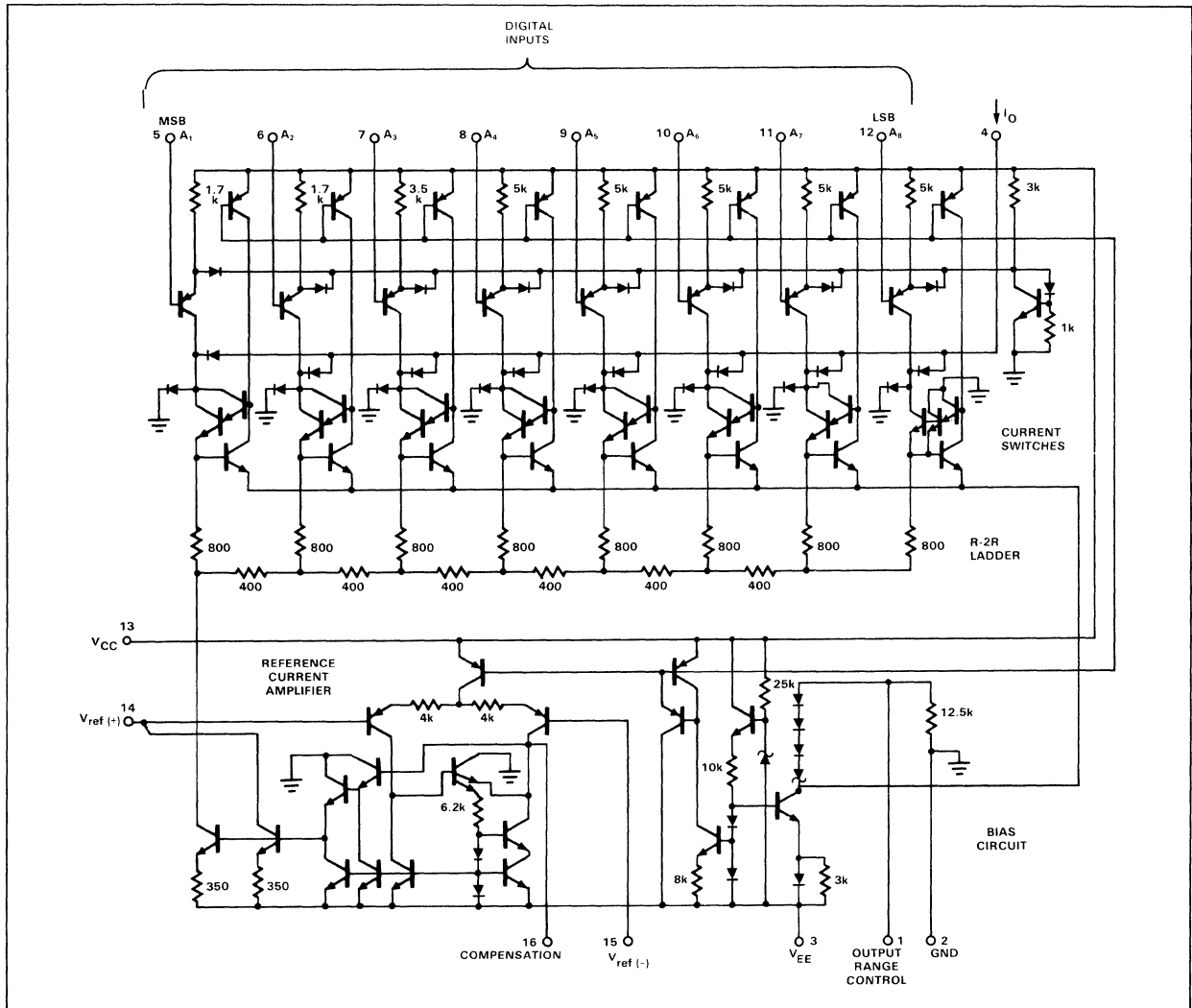
MC1508: T_A = -55°C to 125°C. MC1408: T_A = 0°C to 70°C

PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
E _r	Relative accuracy	Error relative to full scale I _o , Figure 3			±0.19			±0.19			%		
t _s	Setting time ¹	To within 1/2 LSB, includes t _{PLH} , T _A = +25°C, Figure 4			300			300			ns		
t _{PLH}	Propagation delay time Low-to-high	T _A = +25°C, Figure 4			30			30			ns		
t _{PHL}	High-to-low	30			100			30			100		
T _{ClO}	Output full scale current drift	-20			-20			-20			PPM/°C		
V _{IH}	Digital input logic level (MSB) High	Figure 5			2.0			2.0			Vdc		
V _{IL}	Low	2.0			0.8			2.0			0.8		
I _{IH}	Digital input current (MSB) High	Figure 5			0			0			mA		
I _{IL}	Low	V _{IH} = 5.0V V _{IL} = 0.8V			-0.4			-0.4			-0.8		
I _{I5}	Reference input bias current	Pin 15, Figure 5			-1.0			-1.0			-3.0	µA	
I _{OR}	Output current range	Figure 5			0			0			mA		
I _O	Output current	V _{EE} = -5.0V V _{EE} = -7.0V to -15V			2.0			2.0			2.1		
I _{O(min)}	Off-state	Figure 5 V _{ref} = 2.000V, R ₁₄ = 1000Ω All bits low			1.9			1.9			1.99	2.1	µA
V _O	Output voltage compliance	E _r ≤ 0.19% at T _A = +25°C, Figure 5 V _{EE} = -5V V _{EE} below -10V			-0.6, +0.5 -5.0, +0.5			-0.6, +0.5 -5.0, +0.5			-0.6, +0.5 -5.0, +0.5	Vdc	
S _R I _{ref}	Reference current slew rate	Figure 6			4.0			4.0			4.0	mA/µs	
PSRR ₍₋₎	Output current power supply sensitivity	I _{ref} = 1mA			0.5			0.5			2.7	µA/V	
I _{CC}	Power supply current Positive	All bits low, Figure 5			+13.5			+13.5			+22	mA	
I _{EE}	Negative	+13.5			+22			+13.5			+22		
V _{CCR}	Power supply voltage range Positive	T _A = +25°C, Figure 5			+4.5			+4.5			+5.0	Vdc	
V _{EE}	Negative	+4.5			+5.0			+4.5			+5.0		
P _D	Power dissipation	All bits low, Figure 5			105			105			170	mW	
		V _{EE} = -5.0Vdc V _{EE} = -15Vdc			190			190			305		
		All bits high, Figure 5			90			90			160		
		V _{EE} = -5.0Vdc V _{EE} = -15Vdc			160			160			160		

NOTES

1. All bits switched

EQUIVALENT CIRCUIT SCHEMATIC



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current (I_{14}) must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full current I_{14} . For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with

only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0k Ω , minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown in Figure 2. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be

handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the 2 resistors with 0.1 μ F to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and



the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.6 to $+0.5$ V at -24°C , due to the current switching methods employed in the MC1508/MC1408. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is 1 diode voltage below ground when pin 1 is grounded, so a negative voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508/MC1408 may be extended to -5.0 V by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 V. Using a full scale current of 1.992 mA and load resistor of 2.5 k Ω between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 Ω do not significantly affect performance, but 2.5 k Ω load increases worst case settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on settling time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -7.0 V, due to the increased voltage drop across the 350 Ω resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508/MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in

the absolute accuracy of output current. However, the MC1508/MC1408 has a very low full scale current drift with temperature.

The MC1508/ \pm MC1408 series is guaranteed accurate to within $\pm 1/2$ LSB at $+25^{\circ}\text{C}$ at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of 1 LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1508/MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1508/MC1408 circuits' full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total error $\pm 1/2$ of 1 part in 65,536, or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.19\%$ specification provided by the MC1508/MC1408.

Multiplying Accuracy

The MC1508/MC1408 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under worst case conditions, these 8 amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within 8-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508/MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

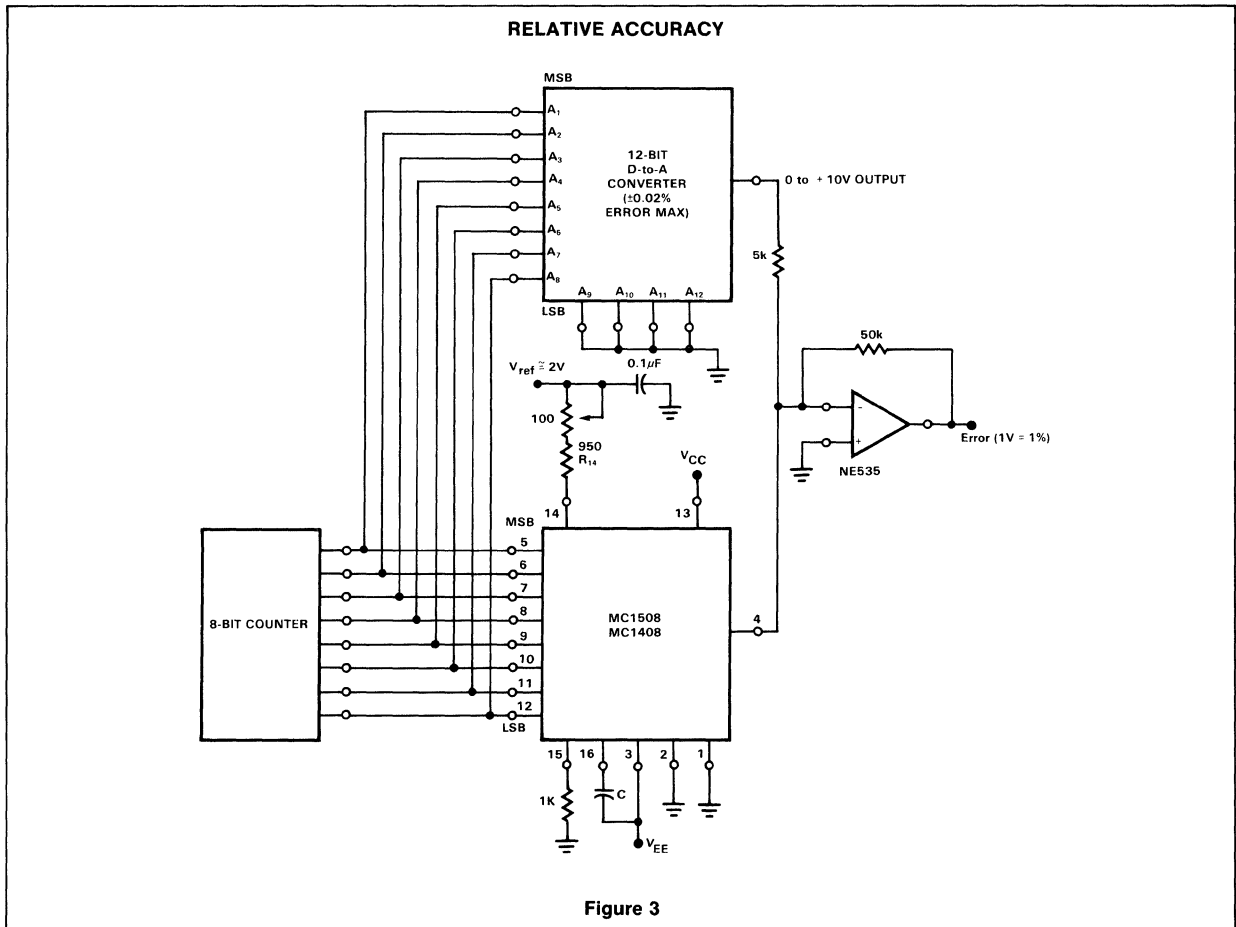
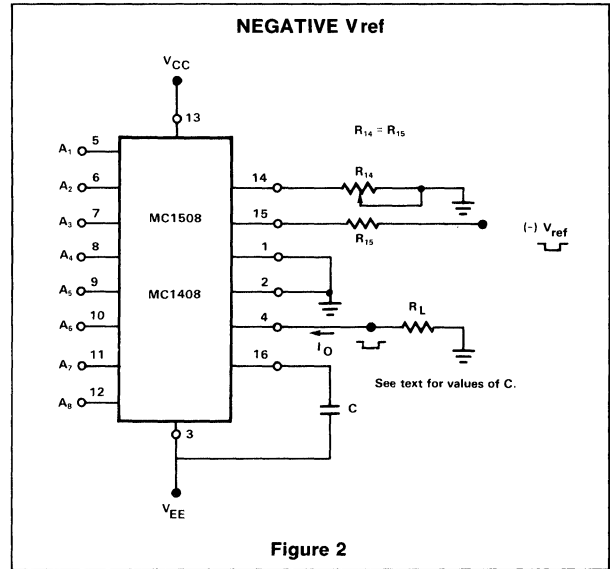
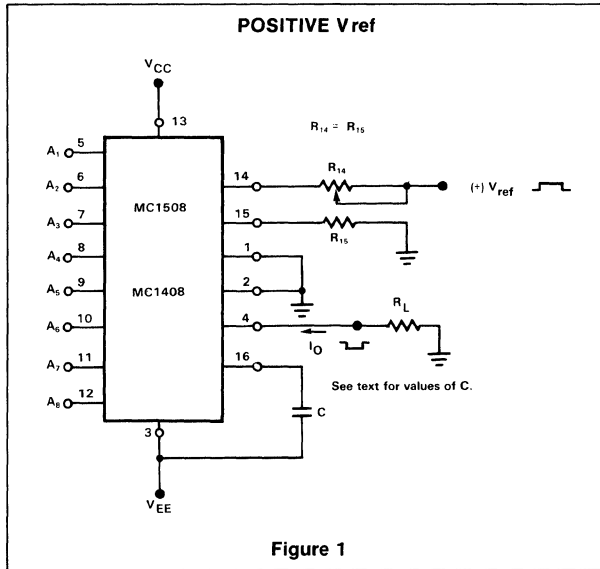
The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within $\pm 1/2$ LSB for 8-bit accuracy and 200 ns to $1/2$ LSB for 7-bit accuracy. The turnoff is typically under 100 ns. These times apply when $R_L \leq 500$ Ω and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit, which turns on and settles in 250 ns and turns off in 80 ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst case switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns on in 200 ns and off in 80 ns, while bit A6 turns on in 150 ns and off in 80 ns.

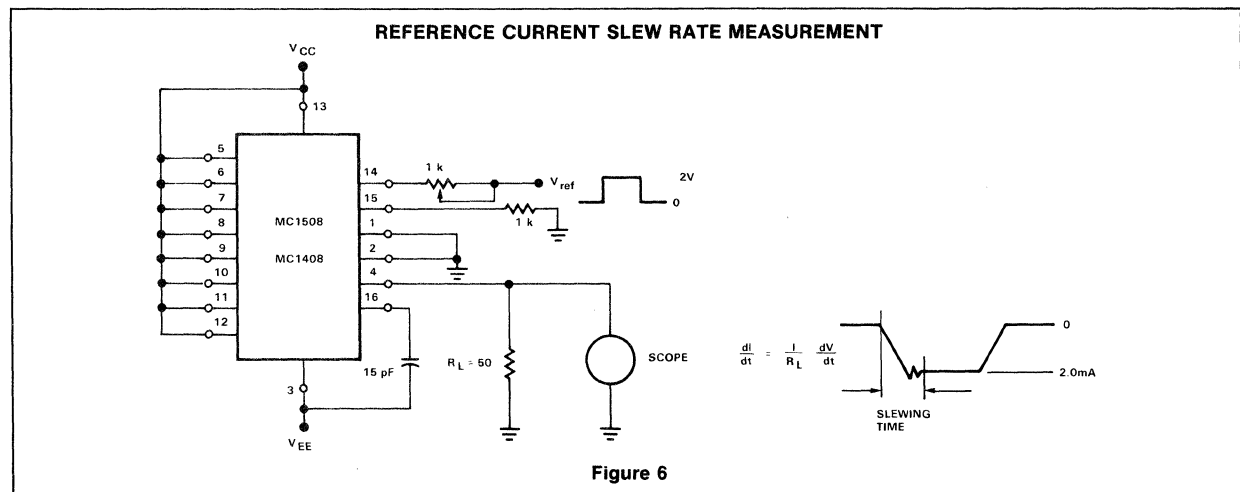
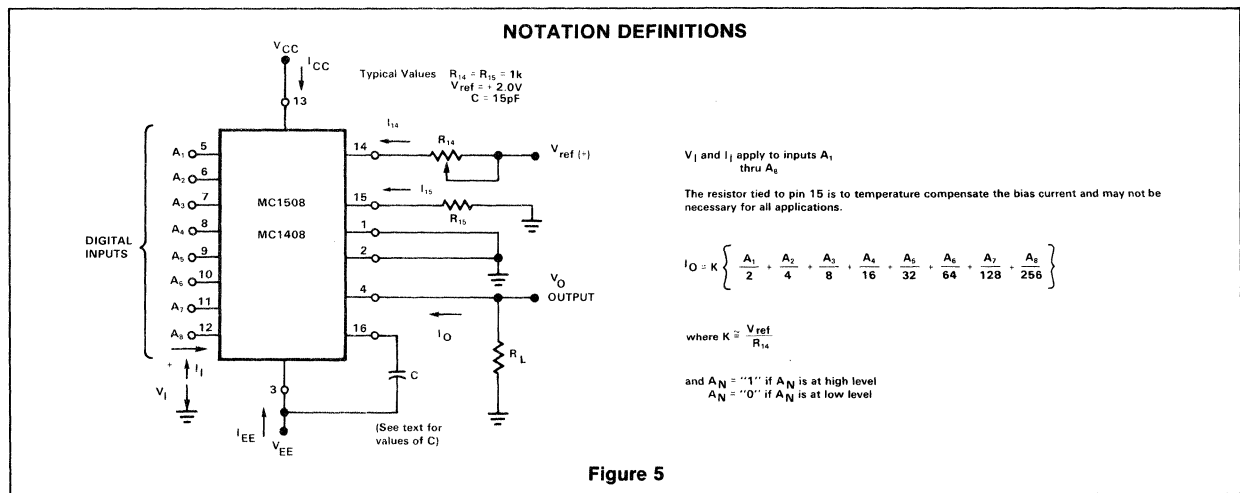
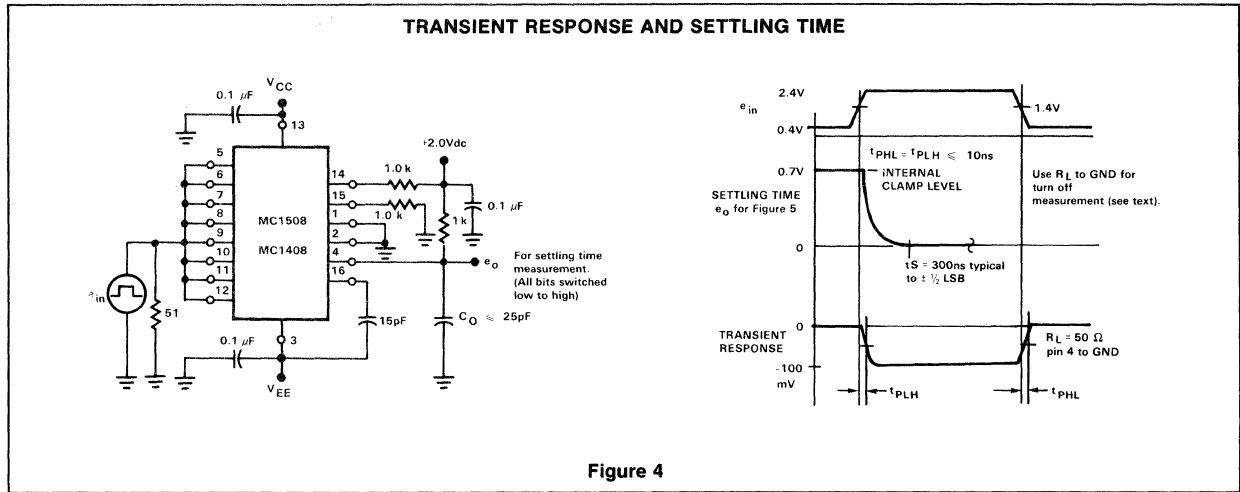
The test circuit of Figure 4 requires a smaller voltage swing for the current switches due to internal voltage clamping in MC1508/MC1408. A 1.0 k Ω load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output R_C time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TEST CIRCUITS



TEST CIRCUITS (Cont'd)



DESCRIPTION

The 5007/5008 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All 5007/5008 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the $\pm 4.5V$ to $\pm 18V$ power supply range, with 33mW power consumption attainable at $\pm 5V$ supplies.

The compact size and low power consumption make the 5007/5008 attractive for portable and military/aerospace applications.

FEATURES

- Fast settling output current—85ns
- Full scale current prematched to ± 1 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Relative accuracy to 0.1% maximum over temperature range
- High output compliance— $-10V$ to $+18V$
- True and complemented outputs
- Wide range multiplying capability
- Low FS current drift— $\pm 10\text{ppm}/^\circ\text{C}$
- Wide power supply range— $\pm 4.5V$ to $\pm 18V$
- Low power consumption—33mW at $\pm 5V$
- SE5008 military qualifications pending

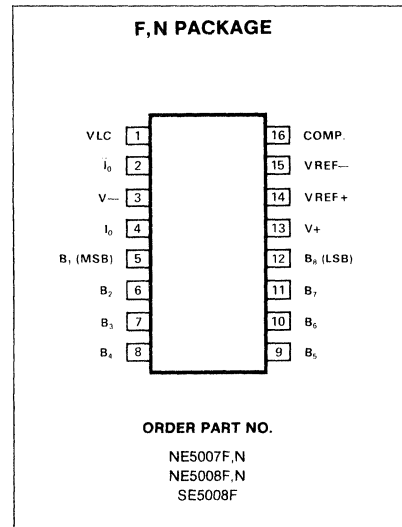
APPLICATIONS

- 8-bit, $1\mu\text{s}$ A-to-D converters
- Servo-motor and pen drivers
- Waveform generators
- Audio encoders and attenuators
- Analog meter drivers
- Programmable power supplies
- CRT display drivers
- High speed modems
- Other applications where low cost, high speed and complete input/output versatility are required

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	-55 to 125°C
0.39% FS	NE5007N NE5007F	-
0.19% FS	NE5008N NE5008F	SE5008F

PIN CONFIGURATION



CROSS REFERENCE

The 5007/5008 series are pin and functionally compatible with the DAC-08 series of devices.

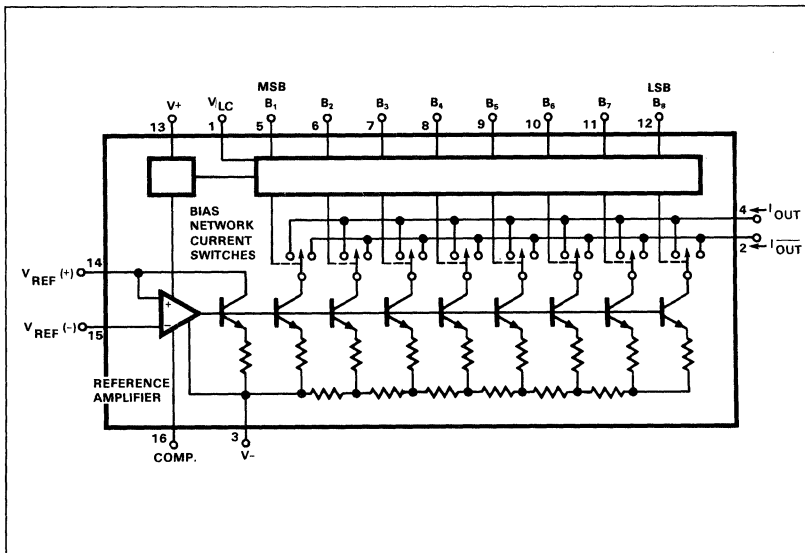
PMI	SIGNETICS
DAC-08A	SE5009
DAC-08	SE5008
DAC-08H	NE5009
DAC-08E	NE5008
DAC-08C	NE5007

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

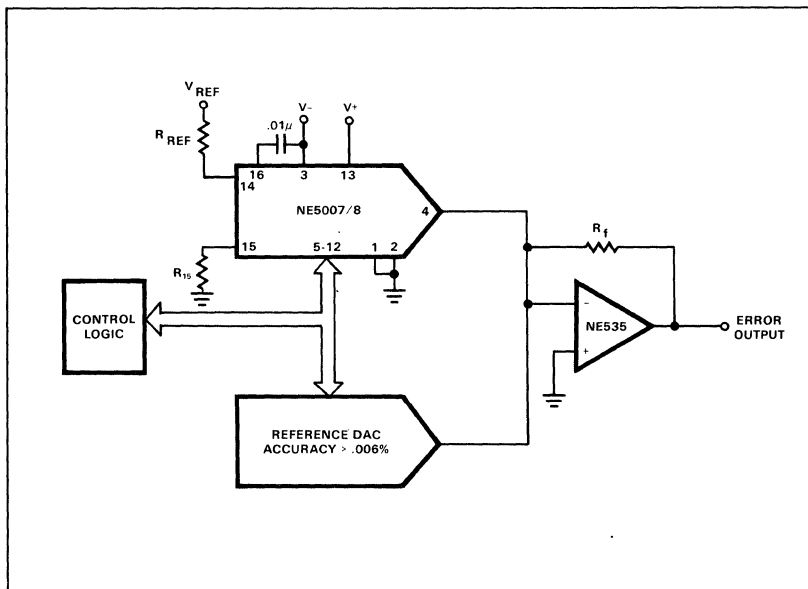
PARAMETER	RATING	UNIT
T_A	Operating temperature range SE5008 NE5007/8	$^\circ\text{C}$
t_{stg}	Storage temperature	$^\circ\text{C}$
P_D	Power dissipation	mW
	Lead soldering temperature (60sec)	$^\circ\text{C}$
	$V+$ to $V-$ supply	V
V_{LC}	Logic inputs Logic threshold control Analog current outputs	$V-$ to $V-$ plus 36V $V-$ to $V+$ See output current or output voltage performance curve
V_{14}, V_{15}	Reference inputs	$V-$ to $V+$
V_{14} to V_{15}	Reference input differential voltage	± 18
I_{14}	Reference input current	mA



BLOCK DIAGRAM



TEST CIRCUIT



Pin 3 must be 3V more negative than the potential to which R₁₅ is returned.

ELECTRICAL CHARACTERISTICS V_S = ±15V, I_{REF} = 2.0mA, Output characteristics refer to both I_{OUT} and I_{OUT} unless otherwise noted. NE5008: T_A = 0°C to 70°C. SE5008: T_A = -55°C to 125°C.

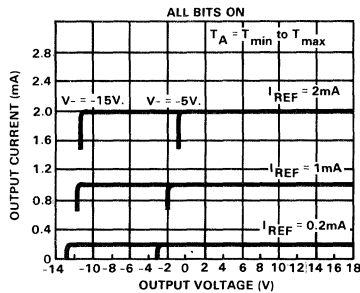
PARAMETER		TEST CONDITIONS	NE5007			NE5008			SE5008			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity*		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19			±0.19	%FS
t _s	Settling time	To ±½ LSB, all bits switched on or off, T _A =25°C		85	135		85	135		85	135	ns
t _{PLH} t _{PHL}	Propagation delay	T _A =25°C, each bit. All bits switched										ns
	Low-to-high High-to-low			35	60		35	60		35	60	
TC _{FS}	Full scale tempco			±10			±10			±10		ppm/°C
V _{OC}	Output voltage compliance	Full scale current change <½ LSB	-10		+18	-10		+18	-10		+18	V
I _{FS4}	Full scale current	V _{REF} =10.000V, R ₁₄ , R ₁₅ =5.000kΩ, T _A =25°C	1.94	1.99	2.04	1.94	1.99	2.04	1.94	1.99	2.04	mA
I _{FSS}	Full scale symmetry	I _{FS4} -I _{FS2}		±2.0	±16		±1.0	±8.0		±1.0	±8.0	µA
I _{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	2.0	µA
I _{FSR}	Output current	V ₋ =-5.0V V ₋ =-7.0V to -18V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
			0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
V _{IL} V _{IH}	Logic input levels	V _{LC} =0V			0.8			0.8			0.8	V
			2.0			2.0			2.0			
I _{IL} I _{IH}	Logic input current	V _{LC} =0V V _{IN} =-10V to +0.8V V _{IN} =2.0V to 18V		-2.0	-10		-2.0	-10		-2.0	-10	µA
				0.002	10		0.002	10		0.002	10	
V _{IS}	Logic input swing	V ₋ =-15V	-10		+18	-10		+18	-10		+18	V
V _{THR}	Logic threshold range	V _S =±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I ₁₅	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	µA
dl/dt	Reference input slew rate	Figures 1, 3	4.0	8.0		4.0	8.0		4.0	8.0		mA/µs
PSSI _{FS+} PSSI _{FS-}	Power supply sensitivity	I _{REF} =1mA V ₊ =+4.5 to 5.5V, V ₋ =-15V; V ₊ =+13.5 to 16.5V, V ₋ =-15V V ₋ =-4.5 to -5.5V, V ₊ =+15V; V ₋ =-13.5 to -16.5, V ₊ =+15V		0.0003	0.01		0.0003	0.01		0.0003	0.01	%FS/%V _S
				0.002	0.01		0.002	0.01		0.002	0.01	
I ₊ I ₋	Powersupply current	V _S =±5V, I _{REF} =1.0mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
				-4.3	-5.8		-4.3	-5.8		-4.3	-5.8	
				2.4	3.8		2.4	3.8		2.4	3.8	
I ₊ I ₋	Positive Negative	V _S =+5V, -15V, I _{REF} =2.0mA		-6.4	-7.8		-6.4	-7.8		-6.4	-7.8	
				2.5	3.8		2.5	3.8		2.5	3.8	
				-6.5	-7.8		-6.5	-7.8		-6.5	-7.8	
I ₊ I ₋	Positive Negative	V _S =±15V, I _{REF} =2.0mA		2.5	3.8		2.5	3.8		2.5	3.8	
				-6.5	-7.8		-6.5	-7.8		-6.5	-7.8	
				2.5	3.8		2.5	3.8		2.5	3.8	
P _D	Power dissipation	±5V, I _{REF} =1.0mA +5V, -15V, I _{REF} =2.0mA ±15V, I _{REF} =2.0mA		33	48		33	48		33	48	mW
				108	136		108	136		108	136	
				135	174		135	174		135	174	

NOTE *NE5007 must have a minimum reference current of .8µA.

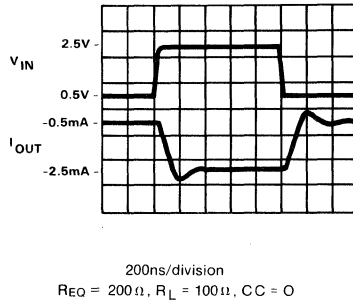


TYPICAL PERFORMANCE CHARACTERISTICS

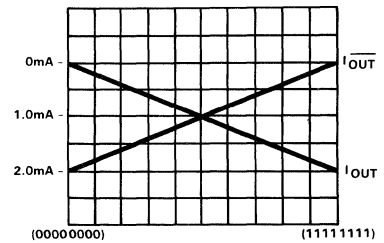
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



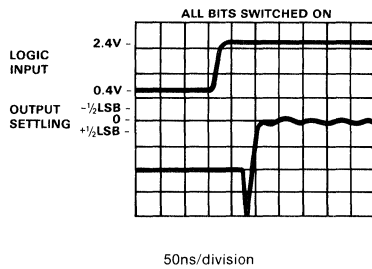
FAST PULSED REFERENCE OPERATION



TRUE AND COMPLEMENTARY OUTPUT OPERATION

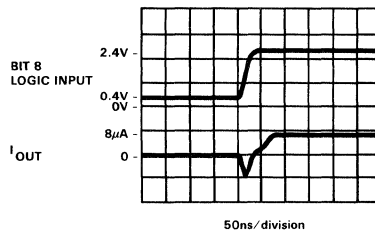


FULL SCALE SETTLING TIME

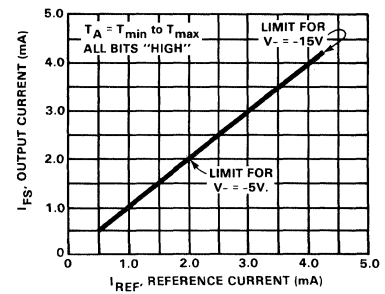


$I_{FS} = 2mA, R_L = 1k\Omega, \frac{1}{2}LSB = 4\mu A$

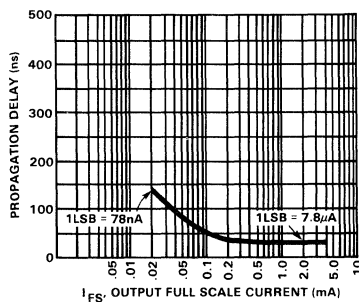
LSB SWITCHING



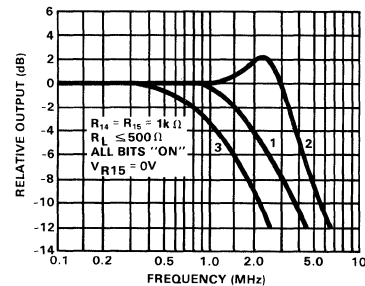
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



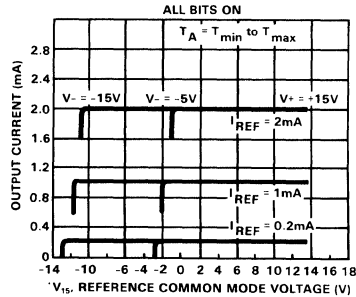
REFERENCE INPUT FREQUENCY RESPONSE



Curve 1: $CC = 15pF, V_{IN} = 2.0V$ p-p centered at +1.0V.
Curve 2: $CC = 15pF, V_{IN} = 50mV$ p-p centered at +200mV.
Curve 3: $CC = 0pF, V_{IN} = 100mV$ p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14} .

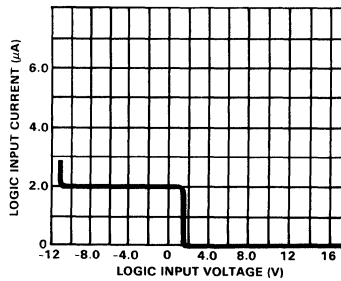
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

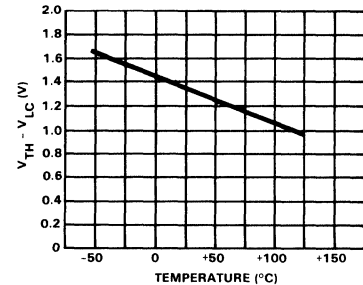


Positive common mode range is always $(V+) - 1.5V$

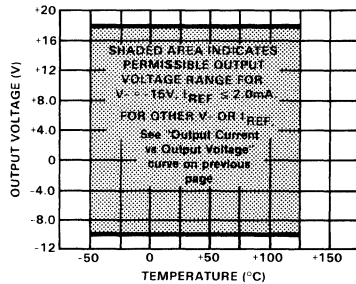
LOGIC INPUT CURRENT vs INPUT VOLTAGE



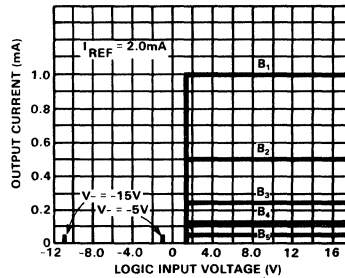
$V_{TH} - V_{LC}$ vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



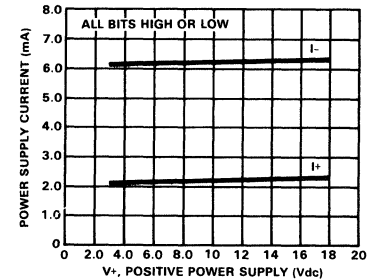
BIT TRANSFER CHARACTERISTICS



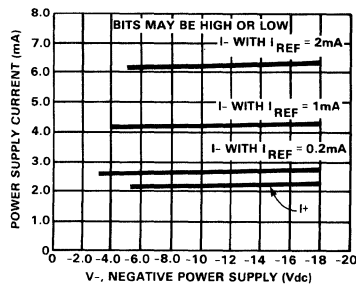
NOTE

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than $1/2$ LSB error, at less than $\pm 100mV$ from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range ($V_{LC} = 0.0V$).

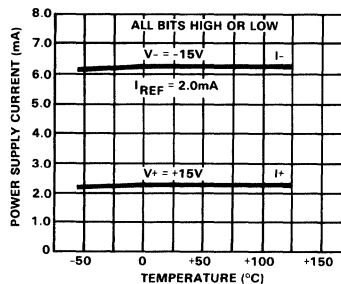
POWER SUPPLY CURRENT vs $V+$



POWER SUPPLY CURRENT vs $V-$

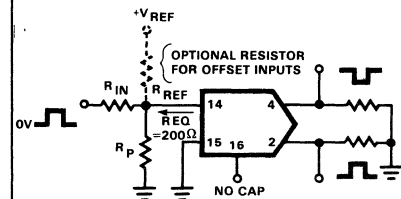


POWER SUPPLY CURRENT vs TEMPERATURE



TYPICAL APPLICATION

PULSED REFERENCE OPERATION



TYPICAL VALUES

$R_{IN} = 5K$
 $+V_{IN} = 10V$

DESCRIPTION

The 5009 monolithic 8-bit digital-to-analog converter is an electrical selection of the 5007/8 series of 8-bit D/A converters. Relative accuracy is specified to $\pm 1/4$ LSB maximum over the operating temperature range. Differential nonlinearity and settling times are also specified to maximum limits.

The device is specifically designed for precision applications in process control and military systems. The SE5009 is specified as equal or superior to the PMI DAC-08A in all respects. Additional relevant testing and application material is shown in the data sheet and application notes for the NE5007/8.

CROSS REFERENCE

The 5009 series are pin and functionally compatible with the DAC-08 series of devices.

PMI	SIGNETICS
DAC-08A	SE-5009
DAC-08	SE-5008
DAC-08H	NE-5009
DAC-08E	NE-5008
DAC-08C	NE-5007

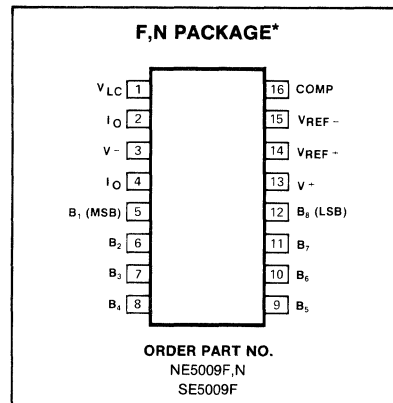
FEATURES

- **Fast settling output current**—60ns typical, 135ns maximum
- **Relative accuracy**— $\pm 0.1\%$ maximum
- **Differential nonlinearity**— $\pm 0.19\%$ maximum
- **Low full-scale current drift**, ± 10 ppm/ $^{\circ}$ C typical
- **SE5009 military qualifications pending**

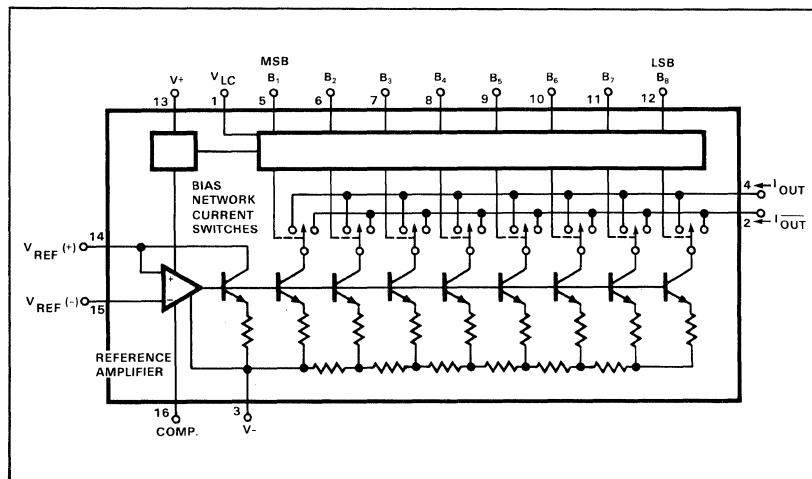
APPLICATIONS

- **Fast 8-bit A/D converter**
- **Variable gain amplifiers**
- **Waveform generators**
- **3 digit BCD D/A converter (0.1%)**
- **Programmable power supplies**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $T_A = 25^{\circ}$ C unless otherwise specified.

PARAMETER	RATING	UNIT
Total supply voltage ($V+ - V-$)	36	V
Logic input voltage	$V- + 36$	V
V_{LC} Voltage at pin 1	$V- \text{ to } V+$	V
Reference input voltage	$V- \text{ to } V+$	V
Reference input differential voltage	± 18	V
Reference input current	5.0	mA
Operating temperature range		$^{\circ}$ C
SE5009	-55 to +125	$^{\circ}$ C
NE5009	0 to +70	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead soldering temperature (10sec)	300	$^{\circ}$ C
Power dissipation*	500	mW

NOTE
*Derate F package at 10mW/ $^{\circ}$ C above 100 $^{\circ}$ C.

DC ELECTRICAL CHARACTERISTICS Pin 3 must be 3V more negative than the potential to which R₁₅ is returned.

These specs apply for V_S = ± 15V, I_{REF} = 2mA,
 T_A for NE5009 0° to 70°C, T_A for SE5009 -55° to +125°C.
 Output characteristic for both I_{OUT} and I_{OUT}.

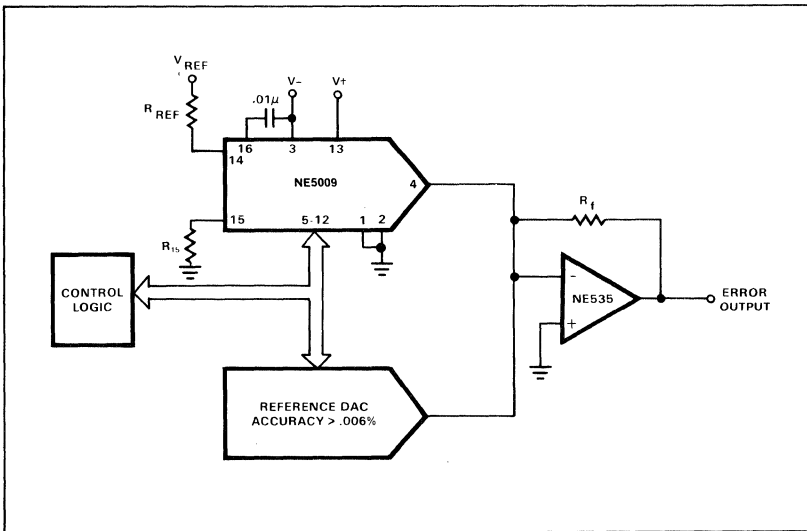
PARAMETER	TEST CONDITIONS	NE5009			SE5009			UNIT	
		Min	Typ	Max	Min	Typ	Max		
Resolution		8	8	8	8	8	8	bits	
Monotonicity		8	8	8	8	8	8	bits	
Relative accuracy	Over temperature range		±0.1	±0.1		±0.1	±0.1	% FS	
Differential nonlinearity				±0.19			±0.19	% FS	
TC _{IFS}	Full scale tempco		±10	±50		±10	±50	ppm/°C	
V _{OC}	Output voltage compliance	Full scale current change < 1/2 LSB	-10		+18	-10	+18	V	
I _{FS4}	Full scale current	V _{REF} = 10.000V, R ₁₄ -R ₁₅ = 5.00CK T _A = 25°C	1.984	1.992	2.000	1.984	1.992	2.000	mA
I _{FSS}	Full scale symmetry	I _{FS4} - I _{FS2}		±0.5	±4.0		±0.5	±4.0	μA
I _{ZS}	Zero scale current			0.1	1.0		0.1	1.0	μA
I _{FSR}	Output current range	V ₋ = -5.0V V ₋ = -7.0V to -18V	0	2.0	2.1	0	2.0	2.1	mA
			0	2.0	4.2	0	2.0	4.2	mA
V _{IL}	Logic input levels	V _{LC} = 0V			0.8			0.8	V
V _{IH}	Logic "1"	V _{LC} = 0V	2.0			2.0			V
I _{IL}	Logic input current	V _{LC} = 0V		-2.0	-10		-2.0	-10	μA
I _{IH}	Logic "1"	V _{IN} = -10V to +0.8V V _{IN} = 2.0V to 18V		0.002	10		0.002	10	μA
V _{IS}	Logic input swing	V ₋ = -15V	-10		+18	-10		+18	V
V _{THR}	Logic threshold range	V _S = ±15V	-10		+13.5	-10		+13.5	V
I ₁₅	Reference bias current			-1.0	-3.0		-1.0	-3.0	μA
PSSIFS+	Power supply sensitivity	I _{REF} = 1mA, V ₋ = -15V: V ₊ = 4.5 to 5.5V V ₊ = 13.5 to 16.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
PSSIFS-		I _{REF} = 1mA, V ₊ = +15V: V ₋ = -4.5 to -5.5V V ₋ = -13.5 to -16.5V		0.0003	0.01		0.0003	0.01	%FS/%VS
I ₊	Power supply current	V _S = ±15V, I _{REF} = 1.0mA		2.3	3.8		2.3	3.8	mA
I ₋				-4.3	-5.8		-4.3	-5.8	mA
I ₊	Power supply current	V _S = +5V, -15V; I _{REF} = 2.0mA		2.4	3.8		2.4	3.8	mA
I ₋				-6.4	-7.8		-6.4	-7.8	mA
I ₊	Power supply current	V _S = ±15V, I _{REF} = 2.0mA		2.5	3.8		2.5	3.8	mA
I ₋				-6.5	-7.8		-6.5	-7.8	mA
P _D	Power dissipation	±5V, I _{REF} = 1.0mA +5V, -15V, I _{REF} = 2.0mA ±15V, I _{REF} = 2.0mA		33	48		33	48	mW
				108	136		108	136	mW
				135	174		135	174	mW



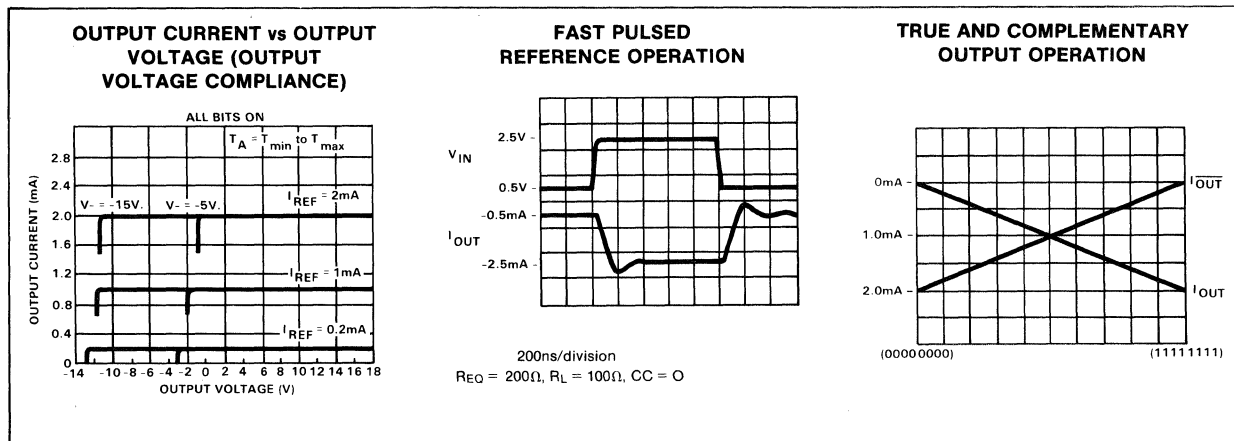
AC ELECTRICAL CHARACTERISTICS These specs apply for $V_S = \pm 15V$, $I_{REF} = 2mA$, Output characteristic for both I_{OUT} and I_{OUT} .

PARAMETER	TEST CONDITIONS	SE/NE5009			UNIT
		Min	Typ	Max	
t_s Settling time	To $\pm 1/2$ LSB all bits switched ON or OFF, $T_A = 25^\circ C$		60	135	ns
	Major carry transition		20		ns
t_{PLH}, t_{PHL} Propagation delay	$T_A = 25^\circ C$		35	60	ns
		Each bit	35	60	ns
di/dt Reference input slew rate		4.0	8.0		$mA = \mu S$

TEST CIRCUIT

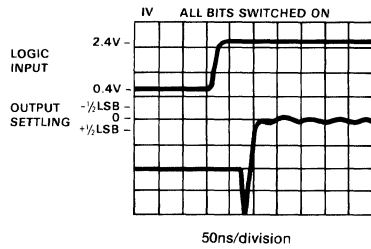


TYPICAL PERFORMANCE CHARACTERISTICS



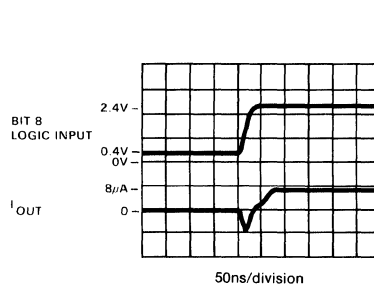
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

FULL SCALE SETTLING TIME

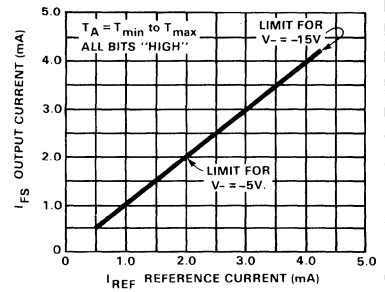


See Figure 13 for settling time fixture

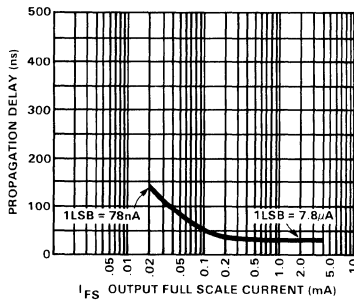
LSB SWITCHING



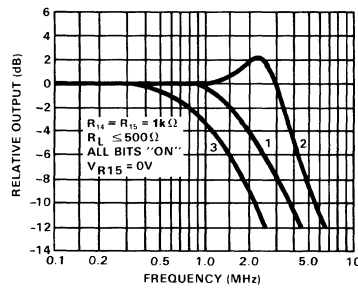
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS

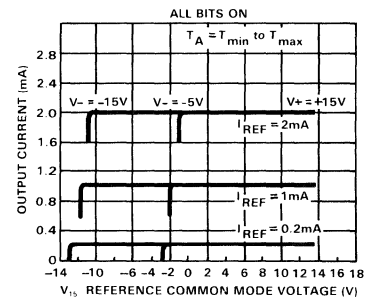


REFERENCE INPUT FREQUENCY RESPONSE



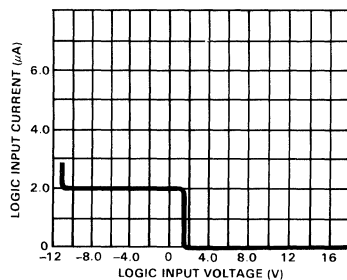
Curve 1: CC = 15pF, V_{IN} = 2.0V p-p centered at +1.0V.
 Curve 2: CC = 15pF, V_{IN} = 50mV p-p centered at +200mV.
 Curve 3: CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R₁₄.

REFERENCE AMP COMMON MODE RANGE

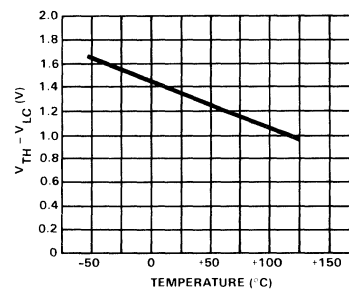


Positive common mode range is always (V₊) - 1.5V

LOGIC INPUT CURRENT vs INPUT VOLTAGE

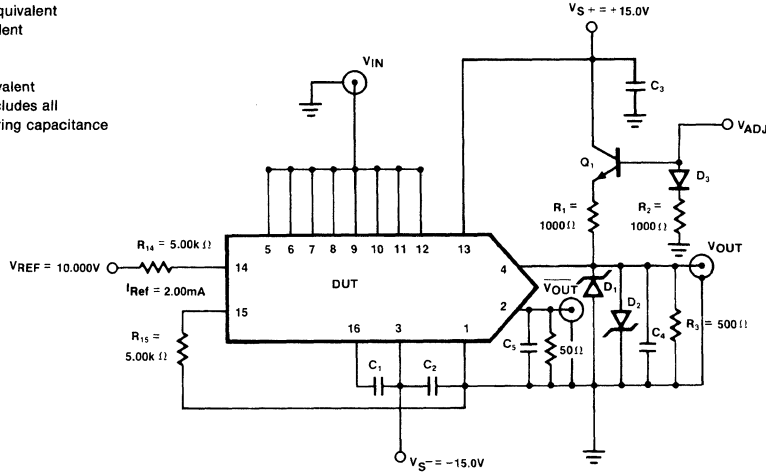


V_{TH}-V_{LC} vs TEMPERATURE

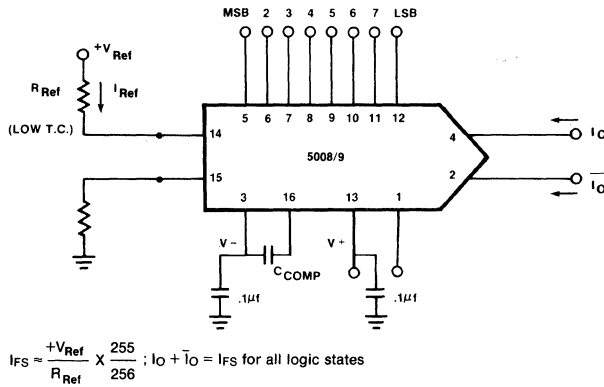


SETTLING TIME AND PROPAGATION DELAY

- D₁, D₂ = IN6263 or equivalent
- D₃ = IN914 or equivalent
- C₁ = 0.01 μf
- C₂, C₃ = 0.1 μf
- Q₁ = 2N3904 or equivalent
- C₄, C₅ = 15pf and includes all probe and fixturing capacitance

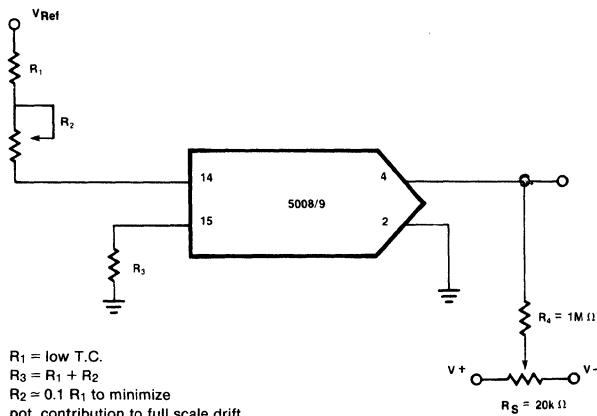


BASIC 5008/5009 CONFIGURATION

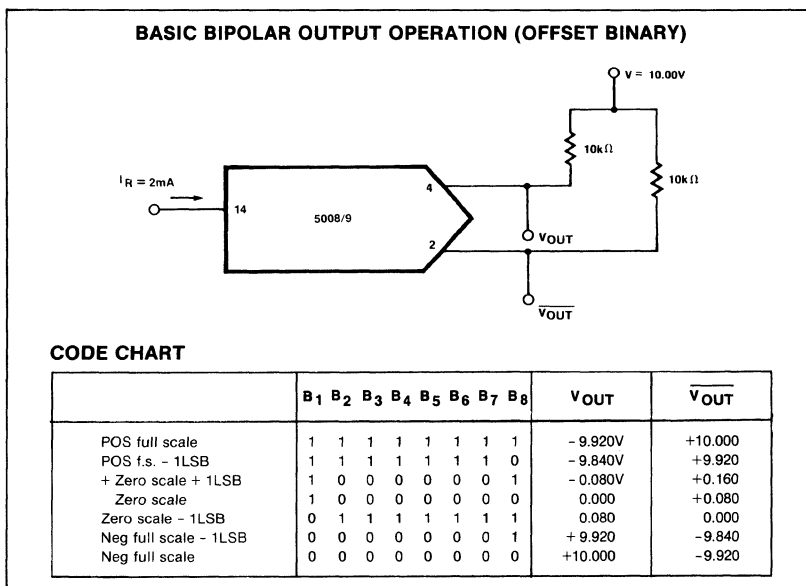
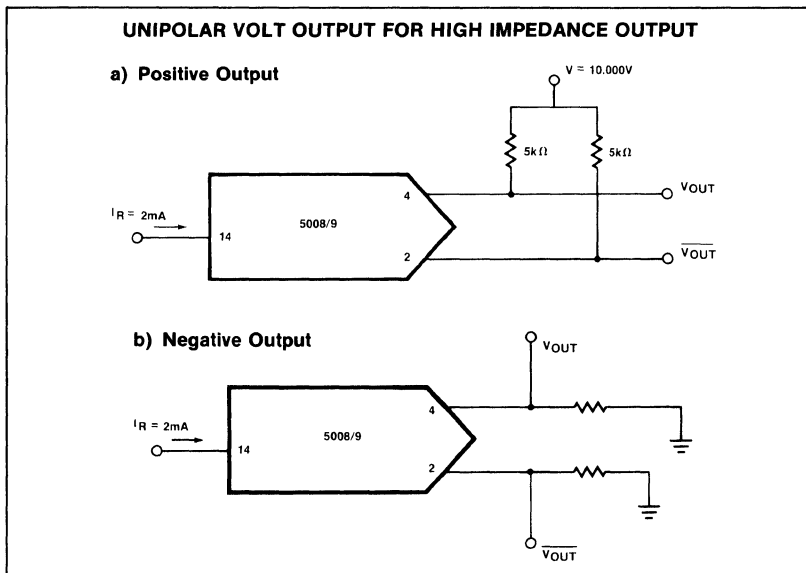
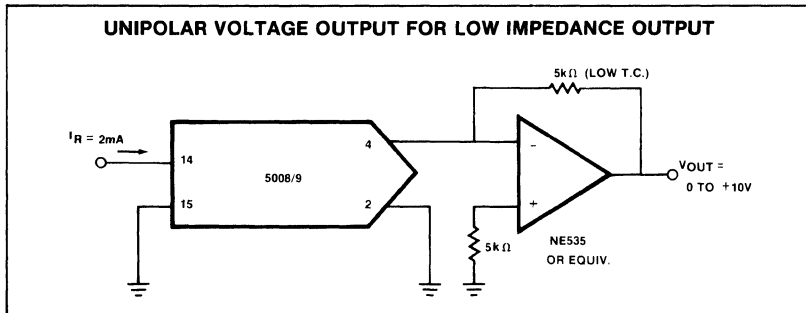


$$I_{FS} \approx \frac{+V_{Ref}}{R_{Ref}} \times \frac{255}{256}; I_O + \bar{I}_O = I_{FS} \text{ for all logic states}$$

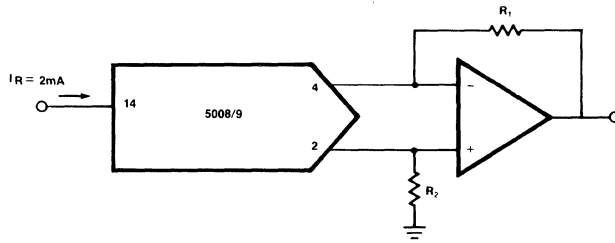
RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.



- R₁ = low T.C.
- R₃ = R₁ + R₂
- R₂ = 0.1 R₁ to minimize pot. contribution to full scale drift



SYMMETRICAL OFFSET BINARY (BIPOLAR)



$V_{OUT} = 0 \text{ to } \pm V^*$

$\pm V^*$ Range:
 $\pm 5V$ for $R_1 = R_2 = 2.5K$
 $\pm 10V$ for $R_1 = R_2 = 5.0K$

3 DIGIT BCD CONVERTER

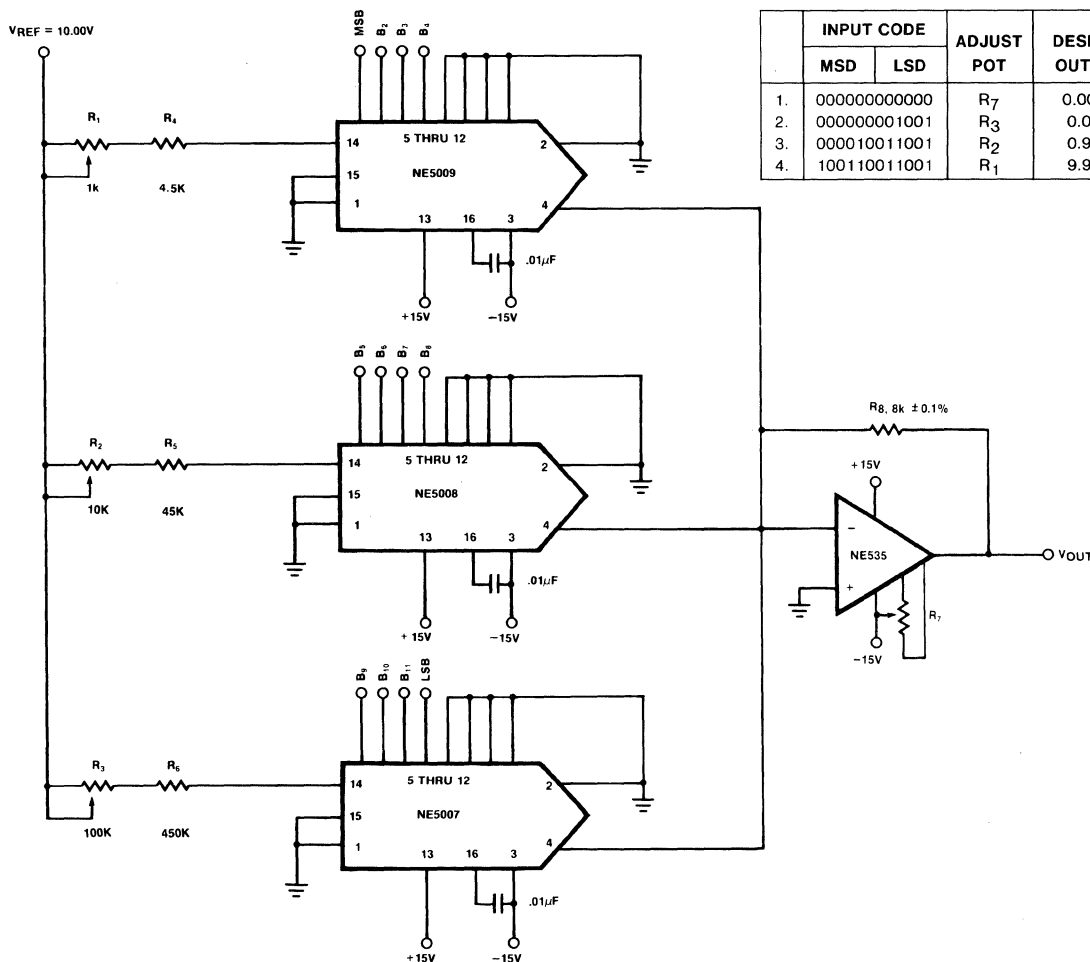
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve $\pm 0.1\%$ accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the zero scale at 0.00V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH $\pm 0.1\%$ ACCURACY



	INPUT CODE		ADJUST POT	DESIRED OUTPUT
	MSD	LSD		
1.	000000000000		R_7	0.000V
2.	000000001001		R_3	0.09V
3.	000010011001		R_2	0.99V
4.	100110011001		R_1	9.99V

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the LE input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

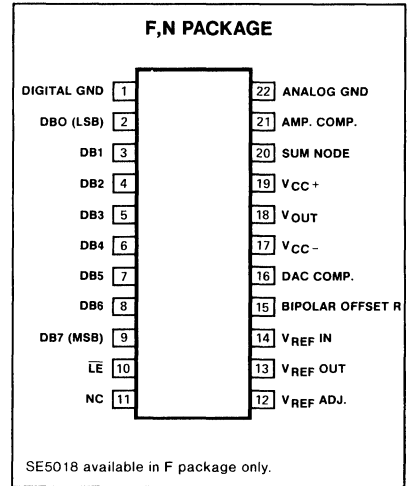
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1/2$ LSB (.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 2650,8080 and many other μ P's

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATION



BLOCK DIAGRAM

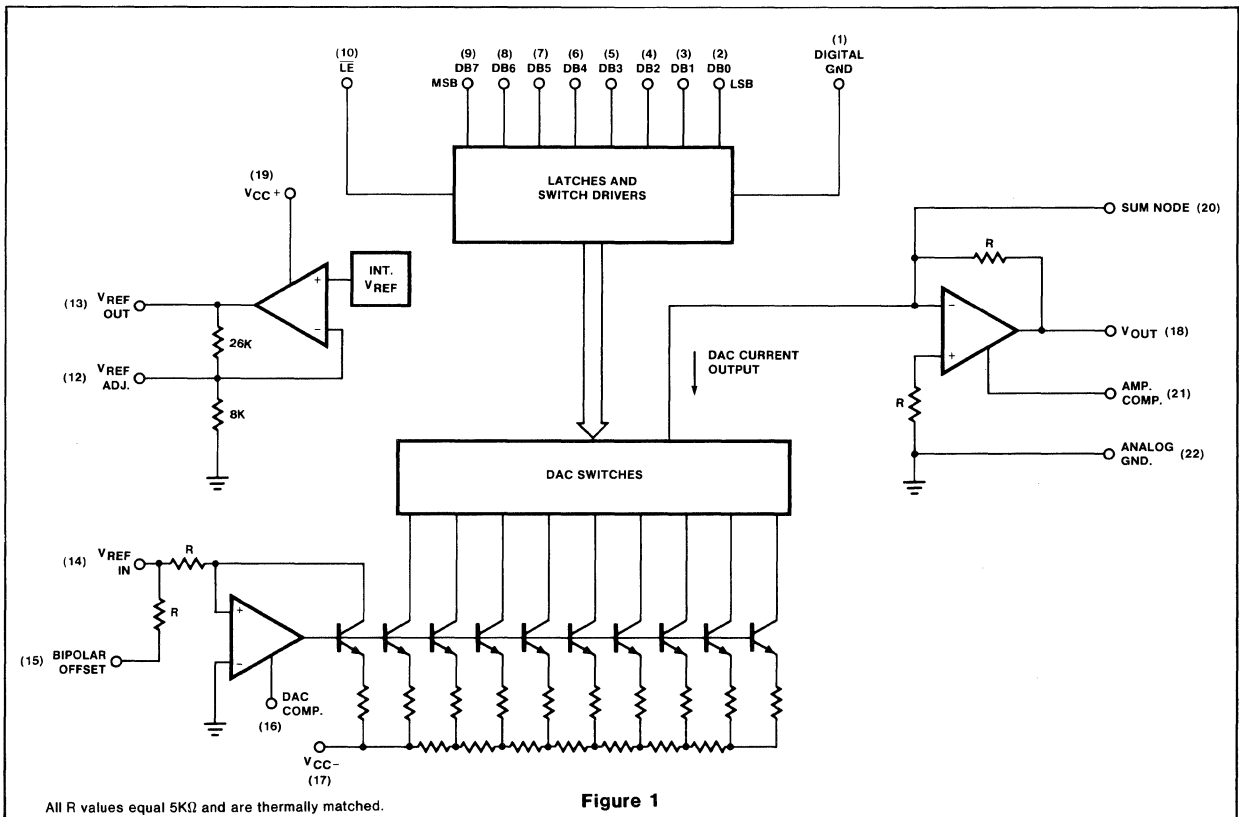


Figure 1



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at V _{REF} input	12	V
V _{REFADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{OUTSC}	Short-circuit current to ground or either supply at V _{OUT}	Continuous	
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

V_{CC+} = +15V, V_{CC-} = -15V, SE5018. -55°C ≤ T_A ≤ 125°C,NE5018. 0°C ≤ T_A ≤ 70°C unless otherwise specified!

Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5018			NE5018			UNIT	
		Min	Typ	Max	Min	Typ	Max		
Resolution		8	8	8	8	8	8	Bits	
Monotonicity		8	8	8	8	8	8	Bits	
Relative accuracy				±0.19			±0.19	%FS	
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V	
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V	
V _{IN(1)}	Logic "1" input voltage	2.0			2.0			V	
V _{IN(0)}	Logic "0" input voltage			0.8			0.8	V	
I _{IN(1)}	Logic "1" input current	Pin 1 = 0V, 2V < V _{IN} < 18V	0.1	10		0.1	10	μA	
I _{IN(0)}	Logic "0" input current	Pin 1 = 0V, -5V < V _{IN} < 0.8V		-2.0		-2.0	-10	μA	
V _{FS}	Full scale output voltage	Unipolar operation	9.50	9.961	10.50	9.50	9.961	10.50	V
V _{FS}	Full scale output voltage	Bipolar operation		+4.961			+4.961		V
V _{ZS}	Zero scale voltage	V _{REF IN} = 5.000V, T _A = 25°C		-5.000			-5.000		mV
				5			5		mV
I _{OS}	Output short circuit current	T _A = 25°C V _{OUT} = 0V		15	40		15	40	mA
PSR ⁺ (out)	Output power supply rejection (+)	V ₋ = -15V, 13.5V ≤ V ₊ ≤ 16.5V, external V _{REF IN} = 5.000V		.001	.01		.001	.01	%FS / %VS
PSR ⁻ (out)	Output power supply rejection (-)	V ₊ = 15V, -13.5V ≤ V ₋ ≤ -16.5V, external V _{REF IN} = 5.000V		.001	.01		.001	.01	%FS / %VS
TC _{FS}	Full scale temperature coefficient	V _{REF IN} = 5.000V		20			20		ppm/°C
TC _{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5018. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, NE5018. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.¹
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE/5018			NE5018			UNIT			
		Min	Typ	Max	Min	Typ	Max				
I_{REF} I_{REFSC}	Reference output current Reference short circuit current	Note 8 $T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$				15	3 30		3 30	mA mA	
$PSR^+(REF)$ $PSR^-(REF)$	Reference power supply rejection (+) Reference power supply rejection (-)	$V^- = -15V, 13.5V \leq V^+ \leq 16.5V$, $I_{REF} = 1.0mA$ $V^+ = 15V, -13.5V \leq V^- \leq 16.5V$,				.003	.01		.003 .01	.01 .01	%VR/ %VS %VR/ %VS
V_{REF} T_{CREF}	Reference voltage Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$			4.5	5.0	5.5	4.5	5.0	5.5	V ppm/ $^{\circ}C$
Z_{IN}	DAC $V_{REF IN}$ input impedance	$I_{REF} = 1.0mA$			4.0	5.0	6.0	4.0	5.0	6.0	K Ω
I_{CC+} I_{CC-}	Positive supply current Negative supply current	$V_{CC+} = 15V$ $V_{CC-} = -15V$				7 -10	14 -15		7 -10	14 -15	mA mA
P_D	Power dissipation	$I_{REF} = 1.0mA, V_{CC} = \pm 15V$				255	435		255	435	mW

NOTE

1. Refer to Figure 2.

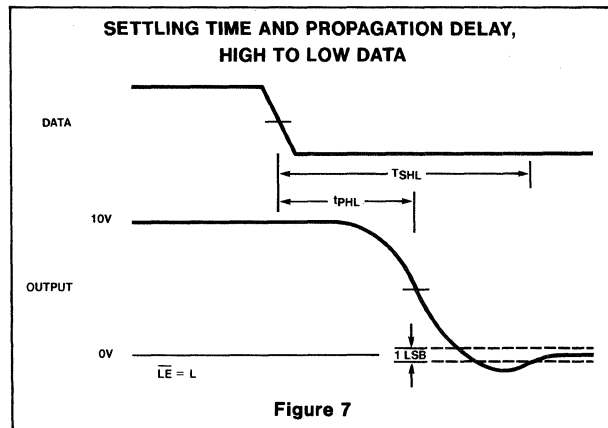
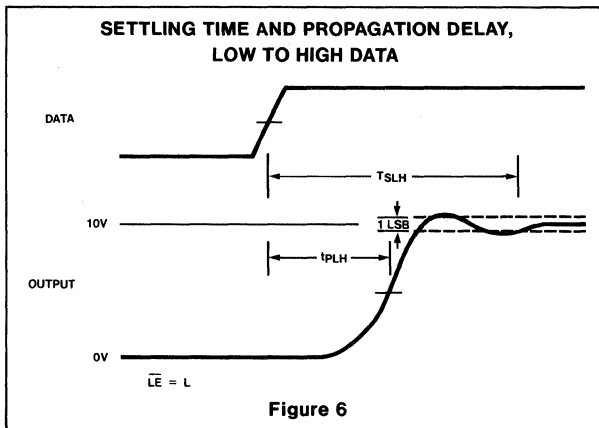
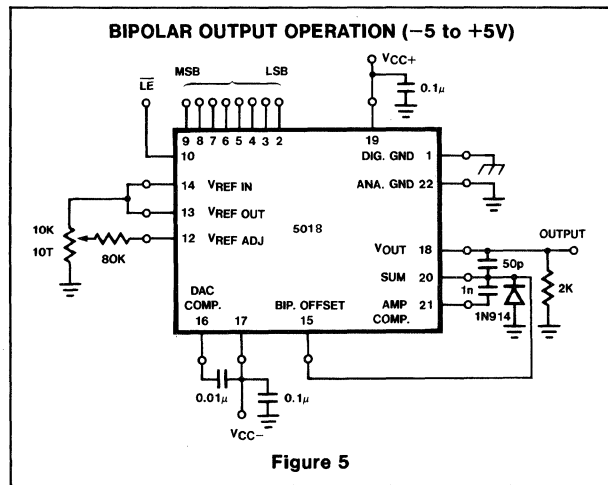
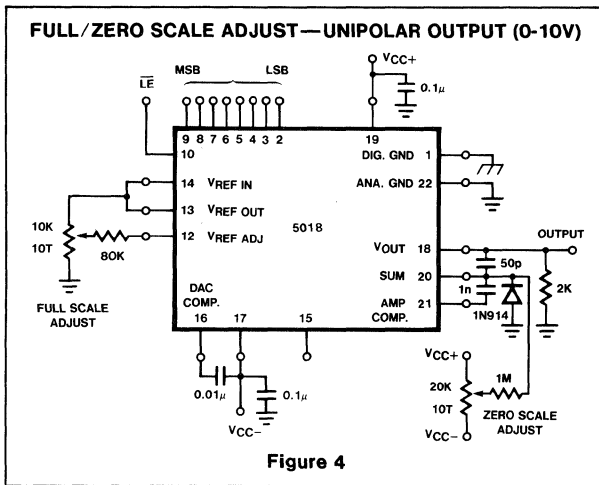
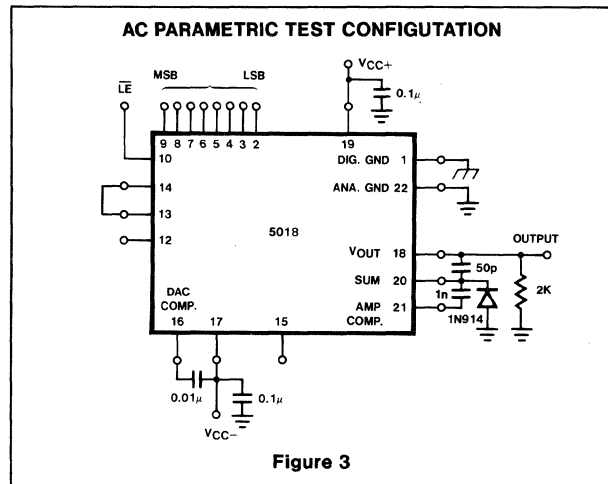
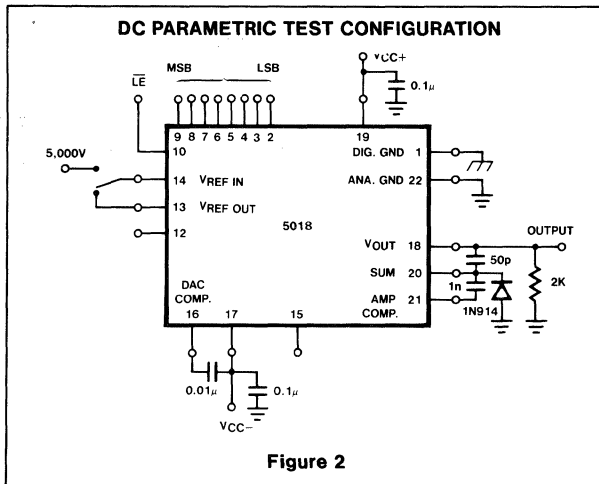
AC ELECTRICAL CHARACTERISTICS² $V_{CC} = \pm 15V, T_A = 25^{\circ}C$

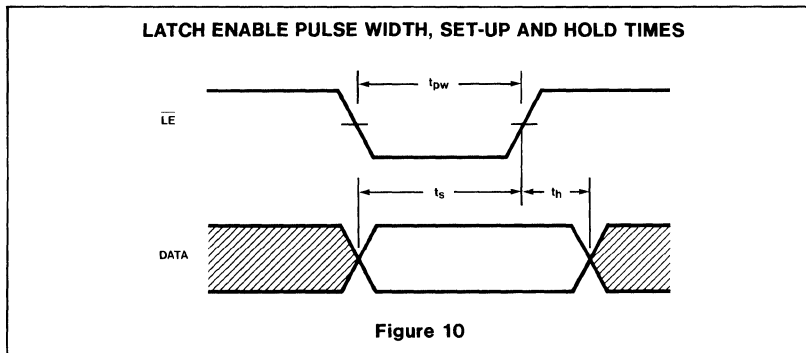
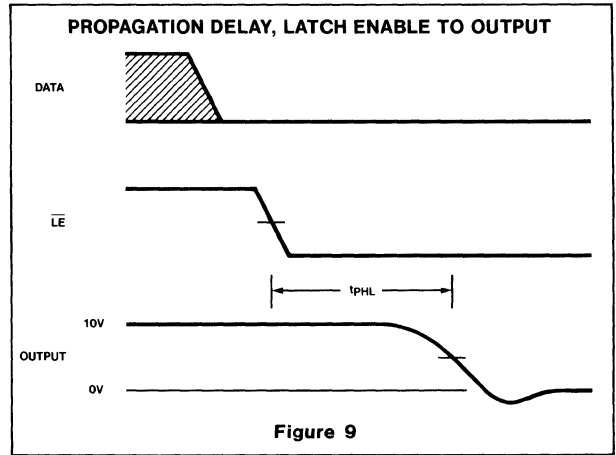
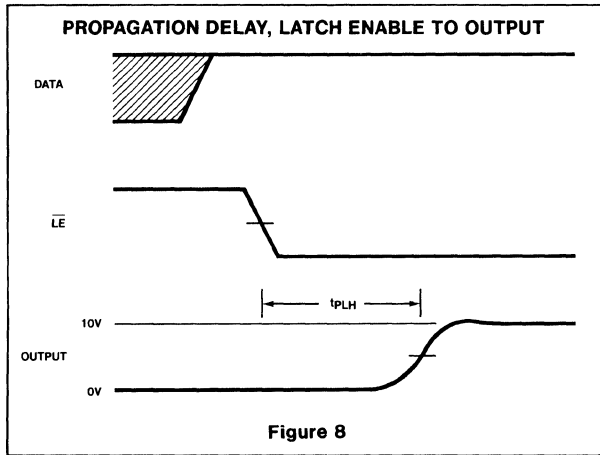
PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
				Min	Typ	Max	
T_{SLH} T_{SHL}	$\pm \frac{1}{2}$ LSB $\pm \frac{1}{2}$ LSB	Input Input	All bits low to high ³ All bits high to low ⁴		1.8		μs μs
t_{plh} t_{phl} t_{plsb} t_{plh} t_{phl}	Output Output Output Output Output	Input Input Input \overline{LE} \overline{LE}	All bits switched low to high ³ All bits switched high to low ⁴ 1 LSB change ^{3,4} low to high transition ⁵ high to low transition ⁶			300 150 150 300 150	ns ns ns ns ns
t_s t_h t_{pw}	Set-up time Hold time Latch enable pulse width	\overline{LE} Input \overline{LE}		2, 7 2, 7 2, 7	100 50 150		ns ns ns

NOTES

- Refer to Figure 3.
- See Figure 6.
- See Figure 7.
- See Figure 7.
- See Figure 8.
- See Figure 9.
- See Figure 10.
- For reference currents $> 3mA$, use of an external buffer is required.







DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the LE input is in the low state. When LE goes high, the input data present at the moment of transition is latched and retained until LE again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

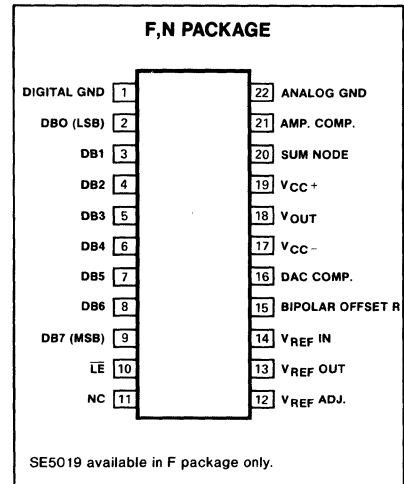
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1/4$ LSB (.1%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 2650,8080 and many other μ P's

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATION



BLOCK DIAGRAM

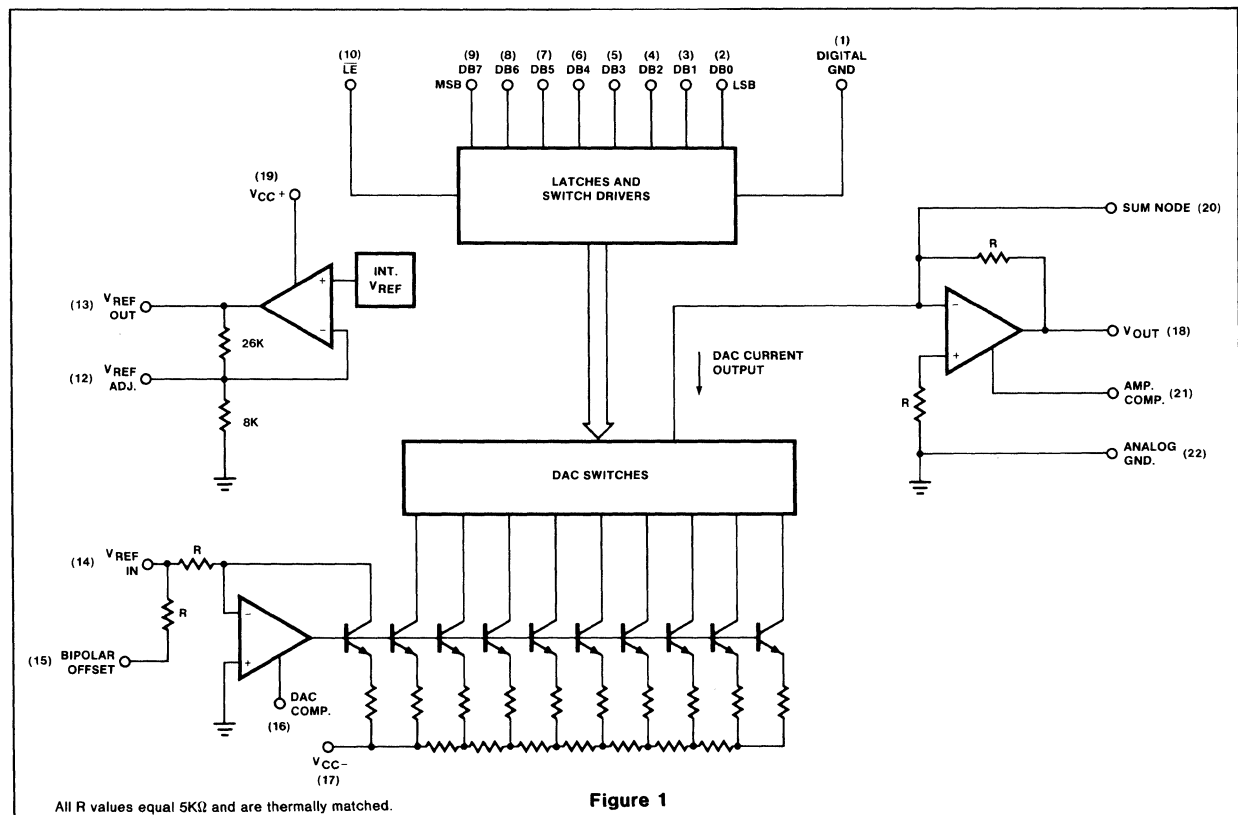


Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at V _{REF} input	12	V
V _{REFADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{OUTSC}	Short-circuit current to ground or either supply at V _{OUT}	Continuous	
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5019	-55 to +125	°C
	NE5019	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C
 For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS V_{CC+} = +15V, V_{CC-} = -15V, SE5019. -55°C ≤ T_A ≤ 125°C, NE5019. 0°C ≤ T_A ≤ 70°C unless otherwise specified.¹
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT		
		Min	Typ	Max	Min	Typ	Max			
Resolution		8	8	8	8	8	8	Bits		
Monotonicity		8	8	8	8	8	8	Bits		
Relative accuracy				±0.1			±0.1	%FS		
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V		
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V		
V _{IN(1)}	Logic "1" input voltage	Pin 1 = 0V			2.0			V		
V _{IN(0)}	Logic "0" input voltage	Pin 1 = 0V				0.8		V		
I _{IN(1)}	Logic "1" input current	Pin 1 = 0V, 2V < V _{IN} < 18V			0.1	10		μA		
I _{IN(0)}	Logic "0" input current	Pin 1 = 0V, -5V < V _{IN} < 0.8V			-2.0	-10		μA		
V _{FS}	Full scale output voltage	Unipolar operation		9.50	9.961	10.50	9.50	9.961	10.50	V
		V _{REF IN} = 5.000V, T _A = 25°C								
V _{FS}	Full scale output voltage	Bipolar operation			+4.961			+4.961		V
		V _{REF IN} = 5.000V, T _A = 25°C			-5.000			-5.000		
V _{ZS}	Zero scale voltage				5			5		mV
I _{OS}	Output short circuit current	T _A = 25°C V _{OUT} = 0V			15	40		15	40	mA
PSR ⁺ (out)	Output power supply rejection (+)	V ₋ = -15V, 13.5V ≤ V ₊ ≤ 16.5V, external V _{REF IN} = 5.000V			.001	.01		.001	.01	%FS / %VS
PSR ⁻ (out)	Output power supply rejection (-)	V ₊ = 15V, -13.5V ≤ V ₋ ≤ -16.5V, external V _{REF IN} = 5.000V			.001	.01		.001	.01	%FS / %VS
TC _{FS}	Full scale temperature coefficient	V _{REF IN} = 5.000V			20			20		ppm/°C
TC _{ZS}	Zero scale temperature coefficient				5			5		ppm/°C

NOTE

1. Refer to Figure 2.



DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5019. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5019. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.¹
Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT			
		Min	Typ	Max	Min	Typ	Max				
I_{REF} I_{REFSC}	Reference output current Reference short circuit current	Note 8 $T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$				15	30		15	30	mA mA
PSR+REF	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$.003		.01		.003	.01	%VR/ %VS
PSR-REF	Reference power supply rejection (-)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,			.003		.01		.003	.01	%VR/ %VS
V_{REF} T_{CREF}	Reference voltage Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$			4.5	5.0	5.5	4.5	5.0	5.5	V ppm/°C
Z_{IN}	DAC V_{REFIN} input impedance	$I_{REF} = 1.0mA$			4.0	5.0	6.0	4.0	5.0	6.0	K Ω
I_{CC+} I_{CC-}	Positive supply current Negative supply current	$V_{CC+} = 15V$ $V_{CC-} = -15V$				7	14		7	14	mA mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$			255		435		255	435	mW

NOTE

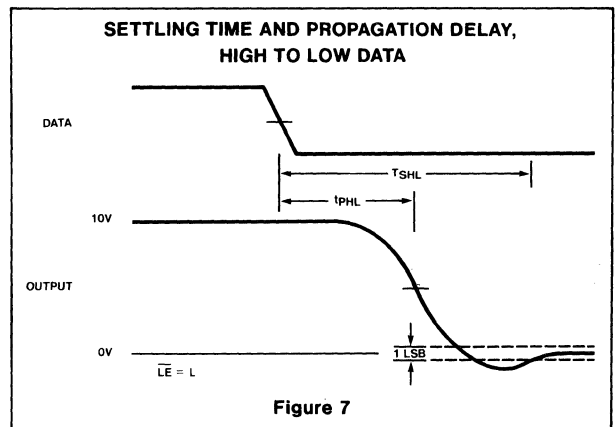
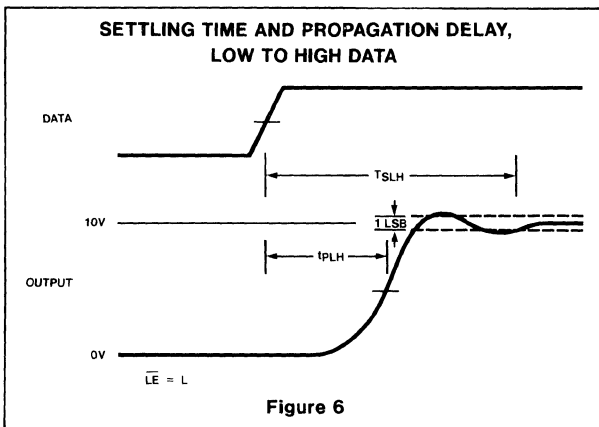
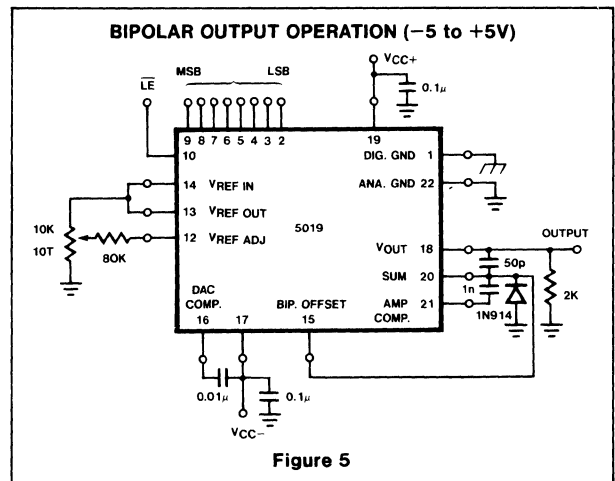
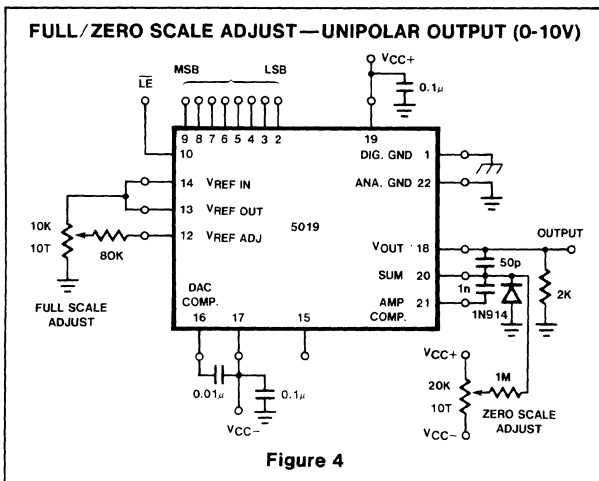
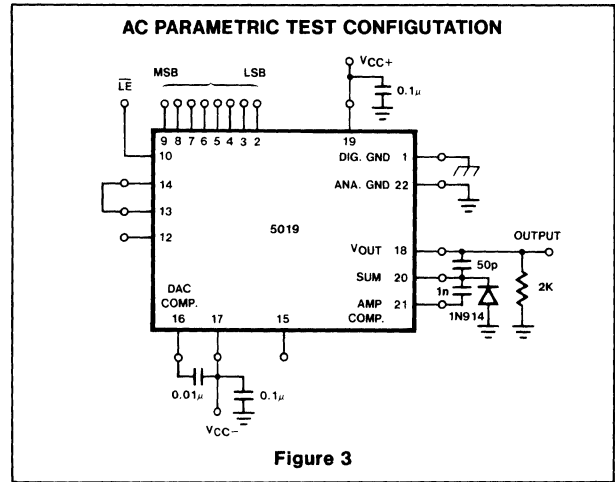
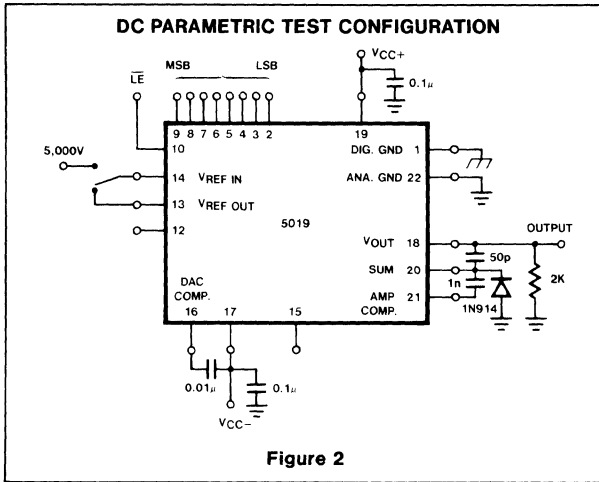
1. Refer to Figure 2.

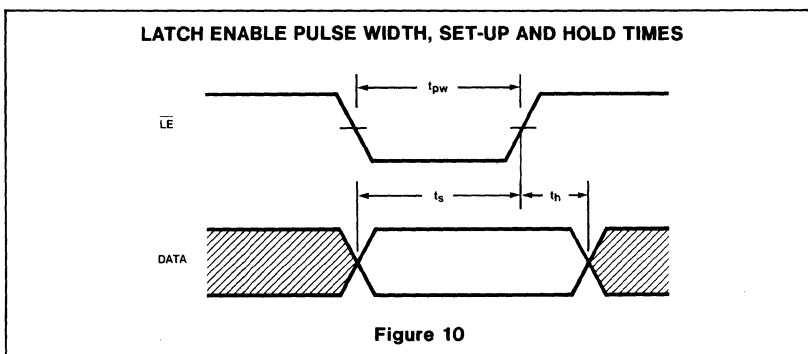
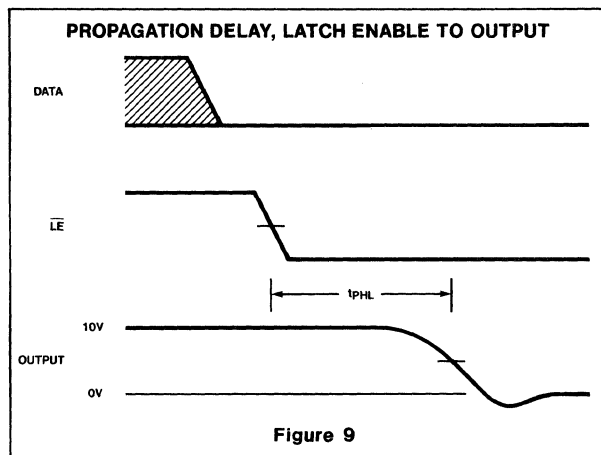
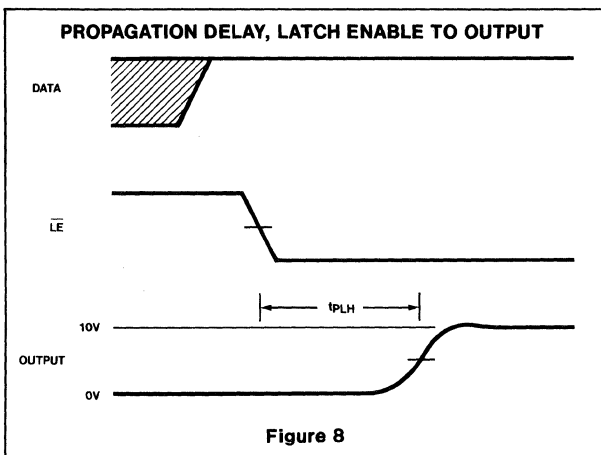
AC ELECTRICAL CHARACTERISTICS² $V_{CC} = \pm 15V$, $T_A = 25^{\circ}C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT	
				Min	Typ	Max		
T_{SLH} T_{SHL}	Settling time Settling time	$\pm \frac{1}{2}$ LSB $\pm \frac{1}{2}$ LSB	Input Input	All bits low to high ³ All bits high to low ⁴		1.8 2.3		μs μs
t_{plh} t_{phi} t_{plsb} t_{plh} t_{phi}	Propagation delay Propagation delay Propagation delay Propagation delay Propagation delay	Output Output Output Output Output	Input Input Input \overline{LE} \overline{LE}	All bits switched low to high ³ All bits switched high to low ⁴ 1 LSB change ^{3,4} low to high transition ⁵ high to low transition ⁶		300 150 150 300 150		ns ns ns ns ns
t_s t_h t_{pw}	Set-up time Hold time Latch enable pulse width	\overline{LE} Input	Input \overline{LE}	2, 7 2, 7 2, 7	100 50 150			ns ns ns

NOTES

- Refer to Figure 3.
- See Figure 6.
- See Figure 6.
- See Figure 7.
- See Figure 8.
- See Figure 9.
- See Figure 10.
- For reference currents > 3mA, use of an external buffer is required.





DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

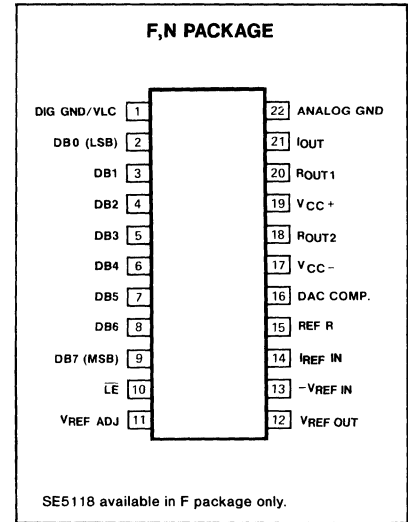
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current—200ns
- Accurate to $\pm 1/2$ LSB (.19%)
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 2650, 8080 and many other μ P's

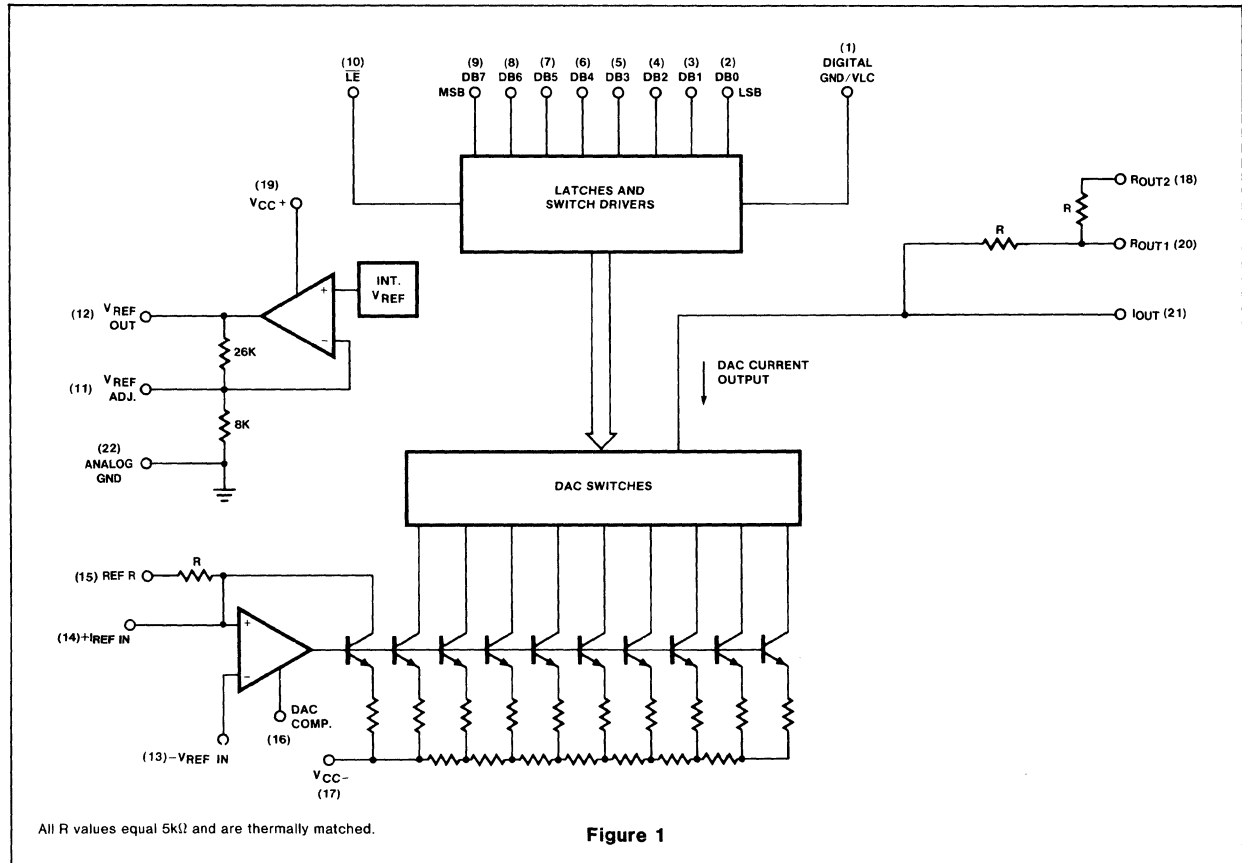
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at R _{REF} input	12	V
V _{REFADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{REFIN}	Reference input current (Pin 14)	3	mA
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5118	-55 to +125	°C
	NE5118	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS V_{CC+} = +15V, V_{CC-} = -15V, SE5118. -55°C ≤ T_A ≤ 125°C, NE5118. 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT		
		Min	Typ	Max	Min	Typ	Max			
Resolution		8	8	8	8	8	8	Bits		
Monotonicity		8	8	8	8	8	8	Bits		
Relative accuracy				±0.19			±0.19	%FS		
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V		
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V		
V _{IN(1)}	Logic "1" input voltage	Pin 1 = 0V			2.0			V		
V _{IN(0)}	Logic "0" input voltage	Pin 1 = 0V				0.8		V		
I _{IN(1)}	Logic "1" input current	Pin 1 = 0V, 2V < V _{IN} < 18V		0.1	10		0.1	10	μA	
I _{IN(0)}	Logic "0" input current	Pin 1 = 0V, -5V < V _{IN} < 0.8V		-2.0	-10		-2.0	-10	μA	
I _{FS}	Full scale output current	Unipolar operation V _{REF IN} = 5.000V, T _A = 25°C		1.90	1.992	2.10	1.90	1.992	2.10	mA
I _{ZS}	Zero scale current				1			1		μA
V _{REF}	Reference voltage	I _{REF} = 1mA T _A = 25°C		4.5	5.0	5.5	4.5	5.0	5.5	V
PSR ⁺ (out)	Output power supply rejection (+)	V ₋ = -15V, 13.5V ≤ V ₊ ≤ 16.5V, external V _{REF IN} = 5.000V			.001	.01		.001	.01	%FS/ %VS
PSR ⁻ (out)	Output power supply rejection (-)	V ₊ = 15V, -13.5V ≤ V ₋ ≤ -16.5V, external V _{REF IN} = 5.000V			.001	.01		.001	.01	%FS/ %VS
TC _{FS}	Full scale temperature coefficient	V _{REF IN} = 5.000V ¹			20			20		ppm/°C
TC _{ZS}	Zero scale temperature coefficient	I _{REF IN} = 1.00mA ²			5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic.
2. This is for current output mode.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5118. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5118. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.
Typical values are specified at $25^{\circ}C$

PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT	
		Min	Typ	Max	Min	Typ	Max		
I_{REF}	Reference output current	Note 1							
I_{REFSC}	Reference short circuit current	$T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$						mA	
PSR+(REF)	Reference power supply rejection (+)	$V- = -15V, 13.5V \leq V+ \leq 16.5V,$ $I_{REF} = 1.0mA$.003	.01		.003	.01	%VR/ %VS	
PSR-(REF)	Reference power supply rejection (-)	$V+ = 15V, -13.5V \leq V- \leq 16.5V,$ $I_{REF} = 1.0mA$.003	.01		.003	.01	%VR/ %VS	
TCREF	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$	60			60		ppm/ $^{\circ}C$	
ZIN	DAC RREFIN input impedance		4.0	5.0	6.0	4.0	5.0	6.0	k Ω
I_{CC+}	Positive supply current	$V_{CC+} = 15V$		7	14		7	14	mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$		-10	-15		-10	-15	mA
PD	Power dissipation	$I_{REF} = 1.0mA, V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V, T_A = 25^{\circ}C$

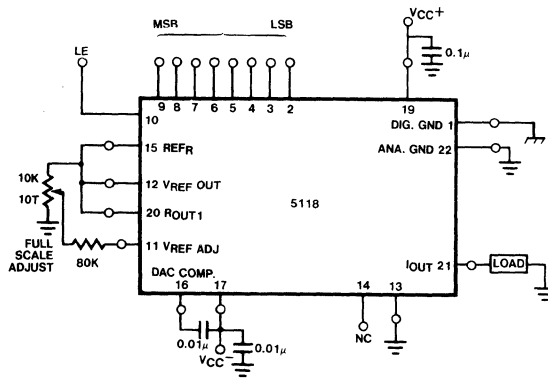
PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5118			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits Low-to-high			ns
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits High-to-low			ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high			ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low			ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change			ns
t_{PLH}	Propagation delay	Output	\overline{LE}	Low-to-high transition			ns
t_{PHL}	Propagation delay	Output	\overline{LE}	High-to-low transition			ns
t_s	Set-up time	\overline{LE}	Input	100			ns
t_h	Hold time	Input	\overline{LE}	50			ns
t_{pw}	Latch enable pulse width			150			ns

NOTES

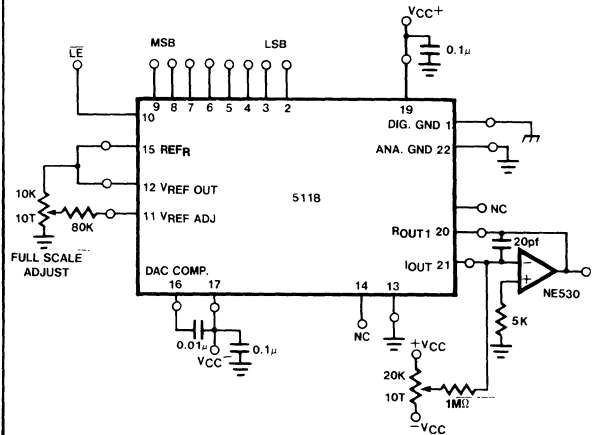
1. For reference currents $> 3mA$, use of an external buffer is required.



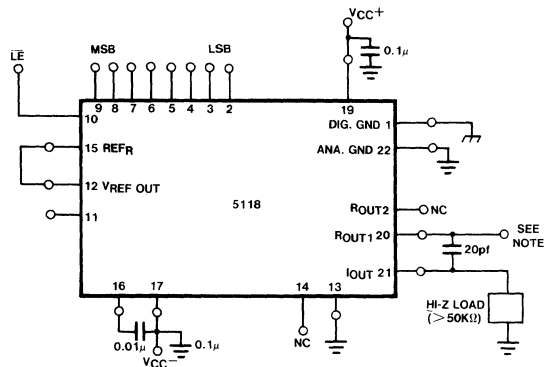
BIPOLAR OUTPUT OPERATION (-1mA TO +1mA)



UNIPOLAR VOLTAGE OUTPUT (0 → +10V)



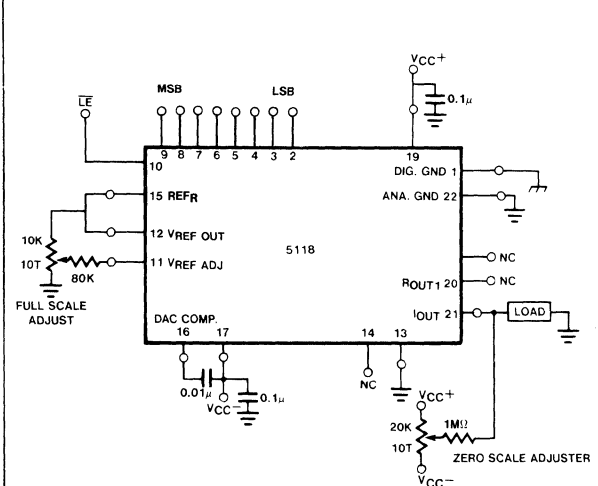
FAST VOLTAGE OUTPUT



NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	-10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 → -2mA)



DESCRIPTION

The NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

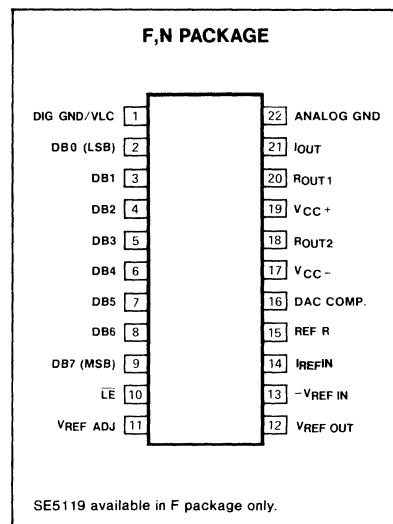
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current—200ns
- Accurate to $\pm 1/4$ LSB (.1%)
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 2650, 8080 and many other μ P's

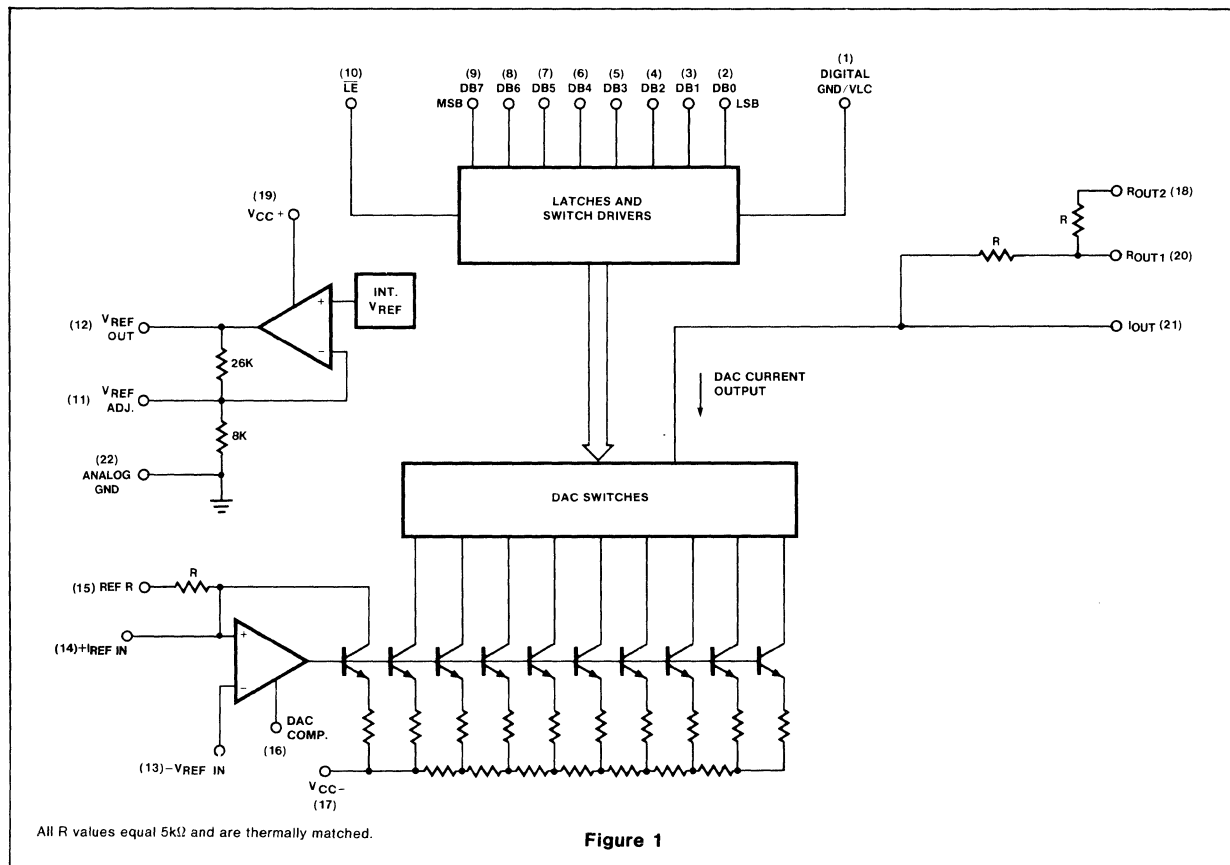
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V_{CC+}	Positive supply voltage	18	V
V_{CC-}	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REFIN}	Voltage at R_{REF} input	12	V
V_{REFADJ}	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REFIN}	Reference input current (Pin 14)	3	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5119	-55 to +125	°C
	NE5119	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5119. $-55^\circ C \leq T_A \leq 125^\circ C$, NE5119. $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT	
		Min	Typ	Max	Min	Typ	Max		
Resolution		8	8	8	8	8	8	Bits	
Monotonicity		8	8	8	8	8	8	Bits	
Relative accuracy				± 0.1			± 0.1	%FS	
V_{CC+}	Positive supply voltage	11.4	15		11.4	15		V	
V_{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V	
$V_{IN(1)}$	Logic "1" input voltage	2.0			2.0			V	
$V_{IN(0)}$	Logic "0" input voltage			0.8			0.8	V	
$I_{IN(1)}$	Logic "1" input current		0.1	10		0.1	10	μA	
$I_{IN(0)}$	Logic "0" input current		-2.0	-10		-2.0	-10	μA	
I_{FS}	Full scale output current	1.90	1.992	2.10	1.90	1.992	2.10	mA	
I_{ZS}	Zero scale current		1			1		μA	
V_{REF}	Reference voltage	4.5	5.0	5.5	4.5	5.0	5.5	V	
$PSR^+(out)$	Output power supply rejection (+)	$V_- = -15V$, $13.5V \leq V_+ \leq 16.5V$, external $V_{REF IN} = 5.000V$.001	.01		.001	.01	%FS/ %VS
$PSR^-(out)$	Output power supply rejection (-)	$V_+ = 15V$, $-13.5V \leq V_- \leq -16.5V$, external $V_{REF IN} = 5.000V$.001	.01		.001	.01	%FS/ %VS
TC_{FS}	Full scale temperature coefficient	$V_{REF IN} = 5.000V^1$			20		20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	$I_{REF IN} = 1.00mA^2$			5		5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic
2. This is for current output mode

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5119. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5119. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.
Typical values are specified at $25^{\circ}C$

PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT	
		Min	Typ	Max	Min	Typ	Max		
I_{REF}	Reference output current	Note 1							mA
I_{REFSC}	Reference short circuit current	$T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$							mA
PSR+(REF)	Reference power supply rejection (+)	$V- = -15V, 13.5V \leq V+ \leq 16.5V,$ $I_{REF} = 1.0mA$							%VR/ %VS
PSR-(REF)	Reference power supply rejection (-)	$V+ = 15V, -13.5V \leq V- \leq 16.5V,$ $I_{REF} = 1.0mA$							%VR/ %VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$							ppm/ $^{\circ}C$
Z_{IN}	DAC R_{REFIN} input impedance	4.0	5.0	6.0	4.0	5.0	6.0	k Ω	
I_{CC+}	Positive supply current	$V_{CC+} = 15V$							mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$							mA
PD	Power dissipation	$I_{REF} = 1.0mA, V_{CC} = \pm 15V$							mW

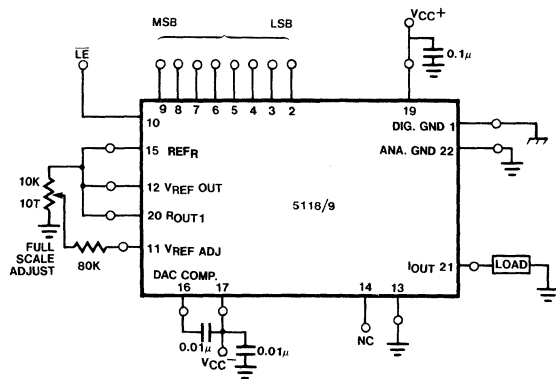
AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V, T_A = 25^{\circ}C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5119			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits Low-to-high			ns
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits High-to-low			ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high			ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low			ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change			ns
t_{PLH}	Propagation delay	Output	\overline{LE}	Low-to-high transition			ns
t_{PHL}	Propagation delay	Output	\overline{LE}	High-to-low transition			ns
t_s	Set-up time	\overline{LE}	Input	100			ns
t_h	Hold time	Input	\overline{LE}	50			ns
t_{pw}	Latch enable pulse width			150			ns

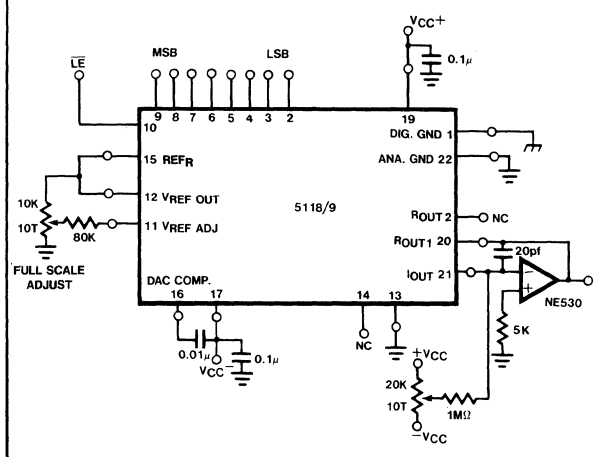
NOTES

1. For reference currents $> 3mA$, use of an external buffer is required.

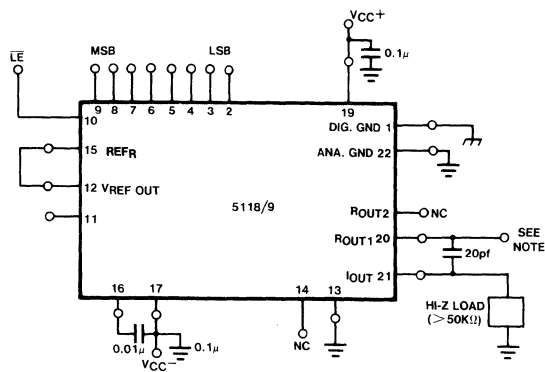
BIPOLAR OUTPUT OPERATION (-1mA TO +1mA)



UNIPOLAR VOLTAGE OUTPUT (0 → +10V)



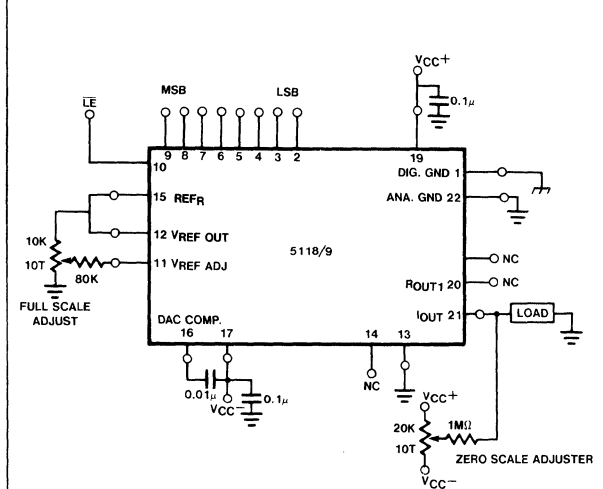
FAST VOLTAGE OUTPUT



NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	-10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 → -2mA)



DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and $\pm 0.1\%$ accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

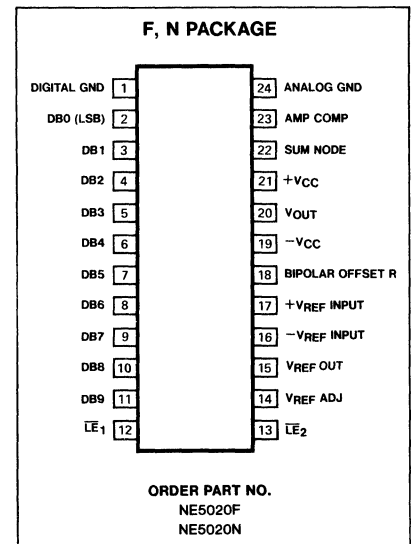
FEATURES

- 10-bit resolution
- Guaranteed monotonicity over operating range
- $\pm 0.1\%$ relative accuracy
- Unipolar (0V to +10V) and Bipolar ($\pm 5V$) output range
- Logic bus compatible
- 5 μ sec settling time

APPLICATIONS

- Precision 10-bit D/A converters
- 10-bit Analog to Digital converters
- Programmable power supplies
- Test equipment
- Measurement instruments

PIN CONFIGURATION



BLOCK DIAGRAM

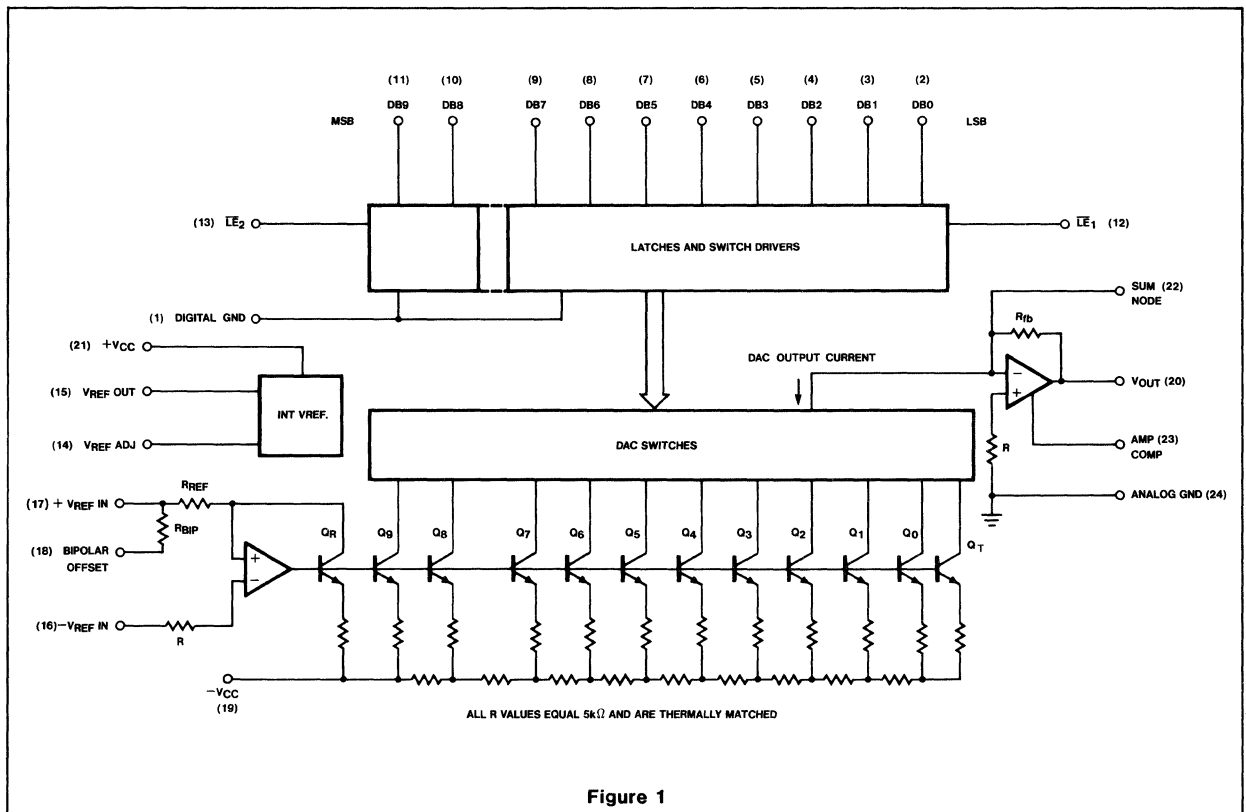


Figure 1



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REF IN}	Voltage at +V _{REF} input	12	V
V _{REF ADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{OUTSC}	Short-circuit current to ground or either supply at V _{OUT}	Continuous	
P _D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T _A	Operating temperature range		
	NE5020	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C
 For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS V_{CC+} = +15V, V_{CC-} = -15V, 0°C ≤ T_A ≤ 70°C unless otherwise specified.¹
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	NE5020			UNIT
		Min	Typ	Max	
Resolution				10	Bits
Monotonicity				10	Bits
Relative accuracy				±0.1	%FS
V _{CC+}	Positive supply voltage	11.4	15	16.5	V
V _{CC-}	Negative supply voltage	-11.4	-15	-16.5	V
V _{IN(1)}	Logic "1" input voltage	Pin 1 = 0V			V
V _{IN(0)}	Logic "0" input voltage	Pin 1 = 0V		0.8	V
I _{IN(1)}	Logic "1" input current	Pin 1 = 0V, 2V < V _{IN} < 18V		0.1	μA
I _{IN(0)}	Logic "0" input current	Pin 1 = 0V, -5V < V _{IN} < 0.8V		-2.0	μA
V _{FS}	Full scale output voltage	Unipolar operation V _{REF IN} = 5.000V, T _A = 25°C		9.9902	V
V _{FS}	Full scale output voltage	Bipolar operation V _{REF IN} = 5.000V, T _A = 25°C		4.9902	V
V _{ZS}	Zero scale voltage	Unipolar operation		5	mV
I _{OS}	Output short circuit current	T _A = 25°C V _{OUT} = 0V		±15	mA
PSR ₊ (out)	Output power supply rejection (+)	V ₋ = -15V, 13.5V ≤ V ₊ ≤ 16.5V, external V _{REF IN} = 5.000V		.001	%FS/ %VS
PSR ₋ (out)	Output power supply rejection (-)	V ₊ = 15V, -13.5V ≤ V ₋ ≤ -16.5V, external V _{REF IN} = 5.000V		.001	%FS/ %VS
TC _{FS}	Full scale temperature coefficient	V _{REF IN} = 5.000V		20	ppmFS /°C
TC _{ZS}	Zero scale temperature coefficient			5	ppmFS /°C

NOTE

1. Refer to Figure 2.

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V, V_{CC-} = -15V, 0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.¹
Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	NE5020			UNIT	
		Min	Typ	Max		
I_{REF}^2	Reference output current			3	mA	
$I_{REF SC}$	Reference short circuit current		15	30	mA	
PSR+REF	Reference power supply rejection (+)	$V_{-} = -15V, 13.5V \leq V_{+} \leq 16.5V, I_{REF} = 1.0mA$.003	.01	%VR / %VS
PSR-REF	Reference power supply rejection (-)	$V_{+} = 15V, -13.5V \leq V_{-} \leq 16.5V, I_{REF} = 1.0mA, T_A = 25^{\circ}C$.003	.01	%VR / %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA, T_A = 25^{\circ}C$		4.5	5.0	V
T_{CREF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$			60	ppm/°C
Z_{IN}	DAC V_{REFIN} input impedance	$I_{REF} = 1.0mA$		4.0	5.0	k Ω
I_{CC+}	Positive supply current	$V_{CC+} = 15V$			7	mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$			-10	mA
P_D	Power dissipation	$I_{REF} = 1.0mA, V_{CC} = \pm 15V$			255	mW

NOTE

1. Refer to Figure 2.
2. For $I_{REF OUT}$ greater than 3mA, an external buffer is required.

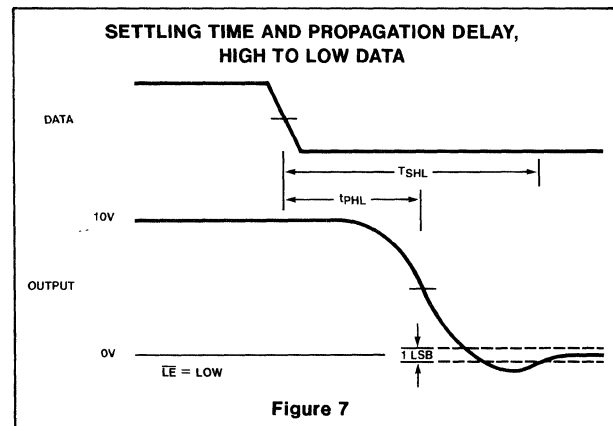
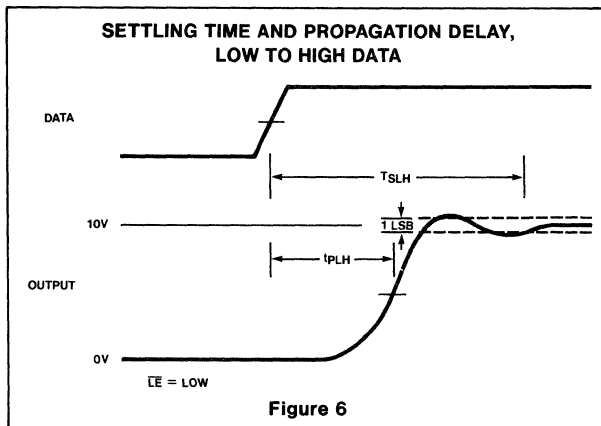
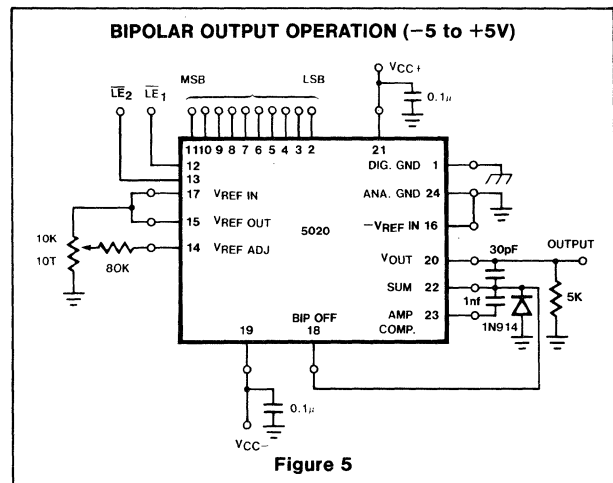
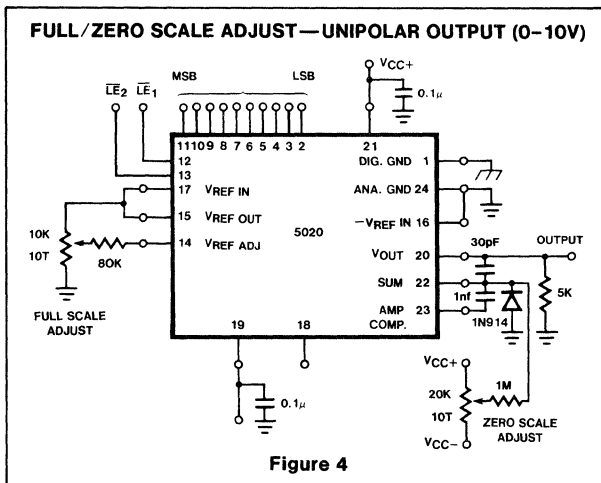
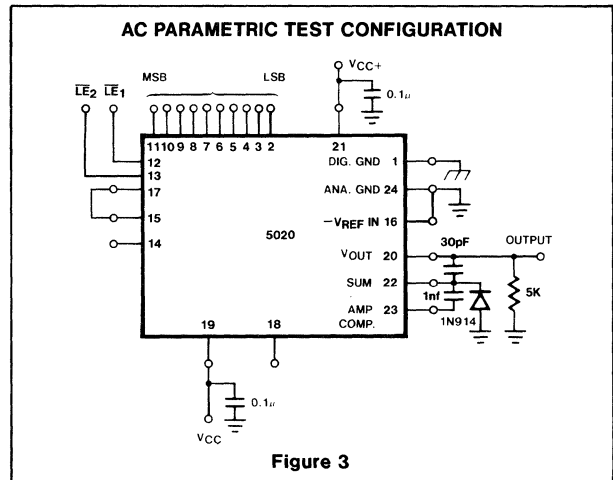
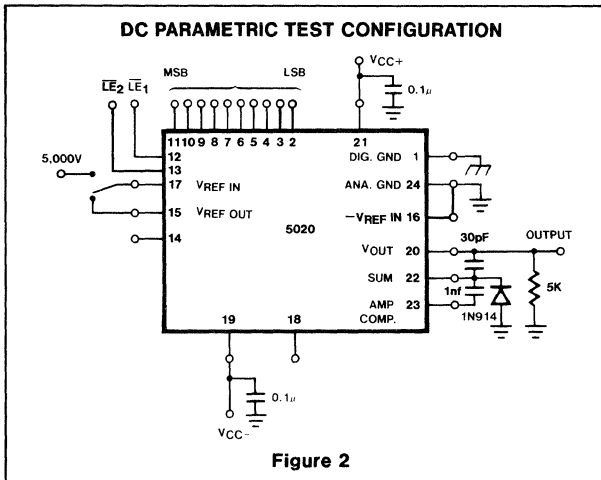
AC ELECTRICAL CHARACTERISTICS³ $V_{CC} = \pm 15V, T_A = 25^{\circ}C$

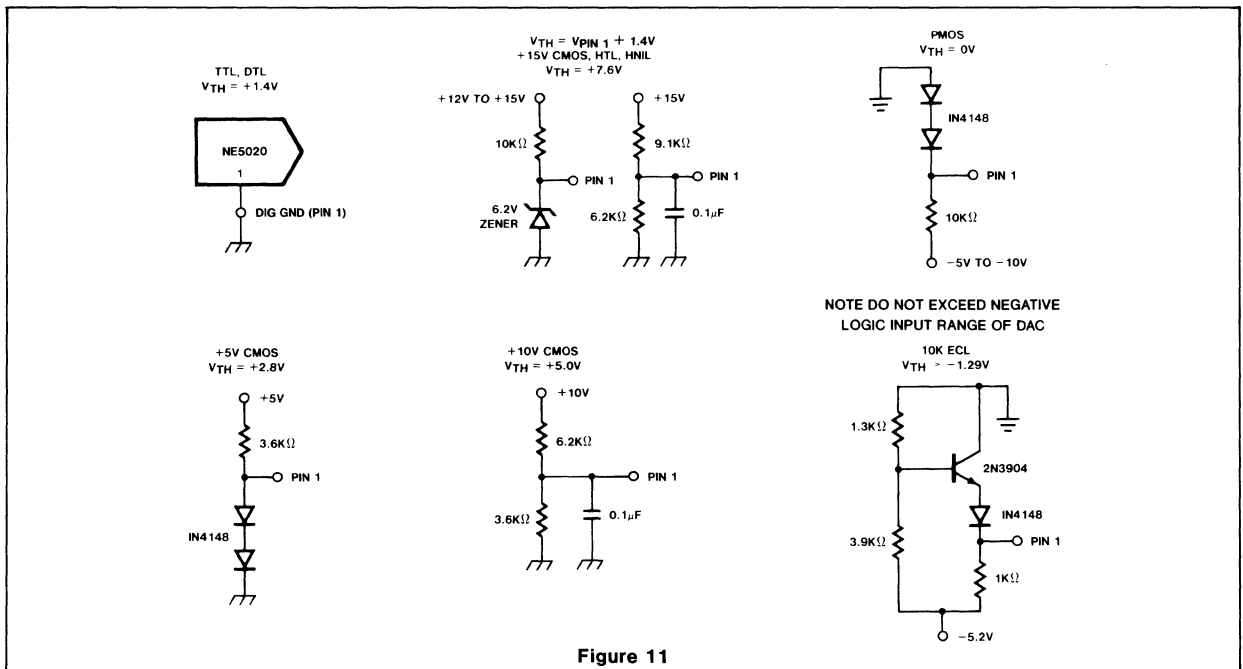
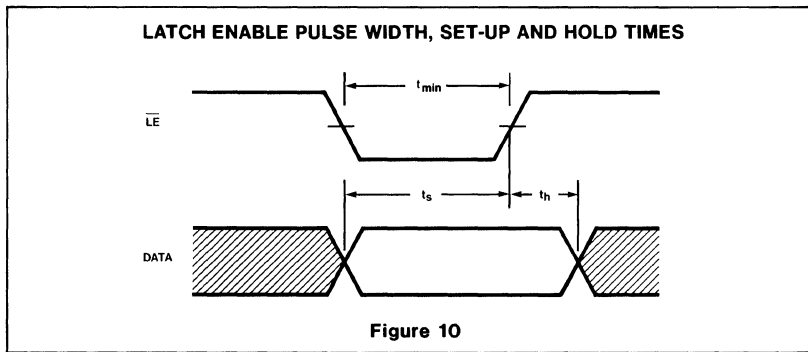
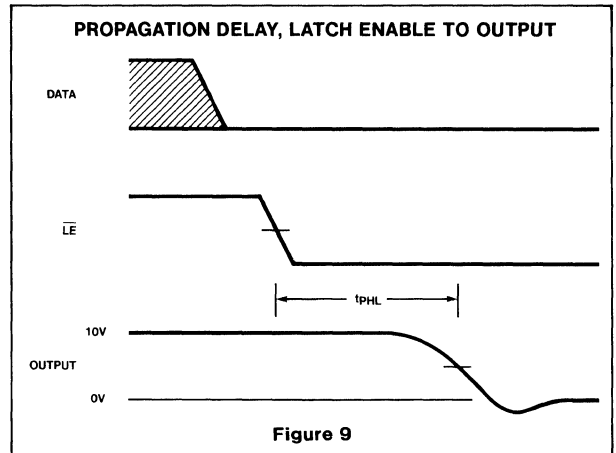
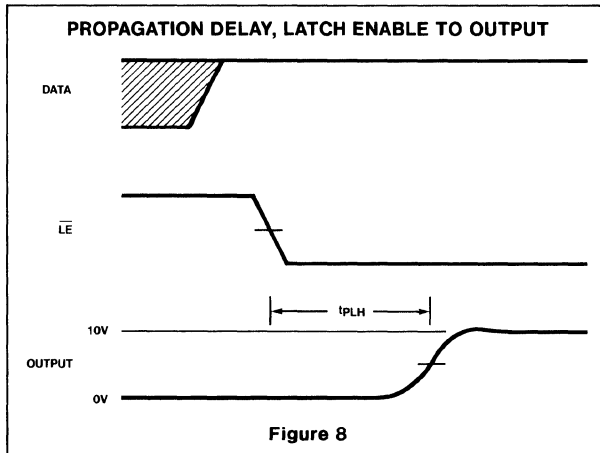
PARAMETER	TO	FROM	TEST CONDITIONS	NE5020			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits low to high ⁴			μ s
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits high to low ⁵			μ s
t_{plh}	Propagation delay	Output	Input	All bits switched low to high ⁴			ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low ⁵			ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change ^{4,5}			ns
t_{plh}	Propagation delay	Output	\overline{LE}	low to high transition ⁶			ns
t_{phl}	Propagation delay	Output	\overline{LE}	high to low transition ⁷			ns
t_s	Set-up time	\overline{LE}	Input	3, 8	100		ns
t_h	Hold time	Input	\overline{LE}	3, 8	50		ns
t_{pw}	Latch enable pulse width			3, 8	150		ns

NOTES

3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.







CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports (\overline{LE}_1 and \overline{LE}_2) and ten data input latches. \overline{LE}_2 controls the two most significant bits of data (DB₉ and DB₈) while \overline{LE}_1 controls the eight lesser significant bits (DB₇ through DB₀). Both the latch enable ports (\overline{LE}) and the data inputs are static and threshold sensitive. When the latch enable ports (\overline{LE}) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the \overline{LE} with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which \overline{LE} goes high) 'memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (.8V max) or $0.1\mu A$ for high (2.0V min)) when the \overline{LE} is high. Any changes on the data bus with \overline{LE} high will have no effect on the DAC output.

The digital logic inputs (\overline{LE} and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after \overline{LE} is changed to a high state.

The independent \overline{LE} (\overline{LE}_1 and \overline{LE}_2) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when \overline{LE}_2 is activated low and returned high according to the NE5020 timing requirements. Then \overline{LE}_1 is activated low and the remaining eight LSB's of data are transferred into the DAC. With

\overline{LE}_1 returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via \overline{LE} pre-load) the external latch with the two MSB values, \overline{LE}_2 is activated low and the eight LSB's and the

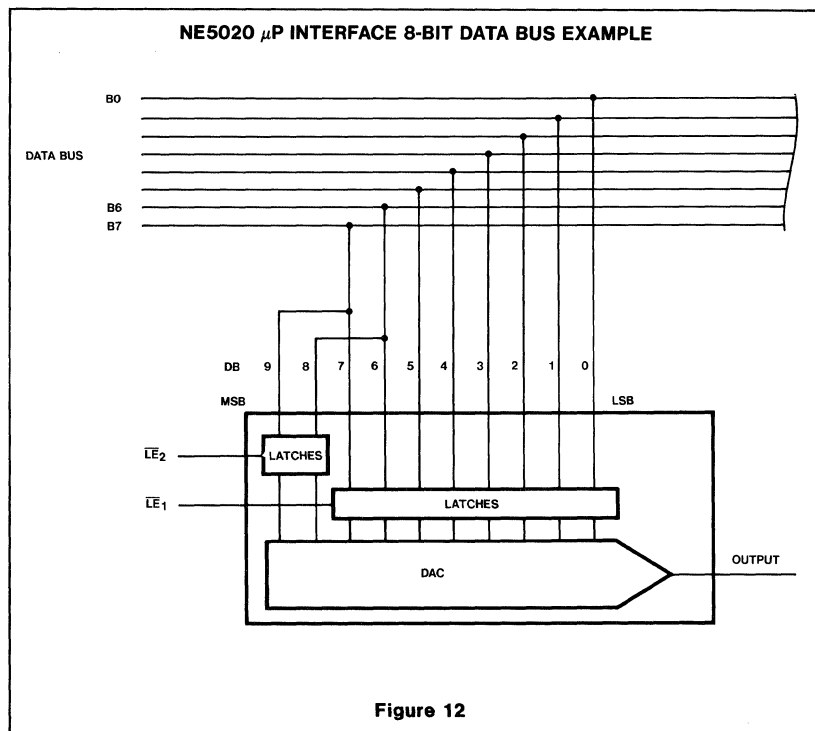


Figure 12

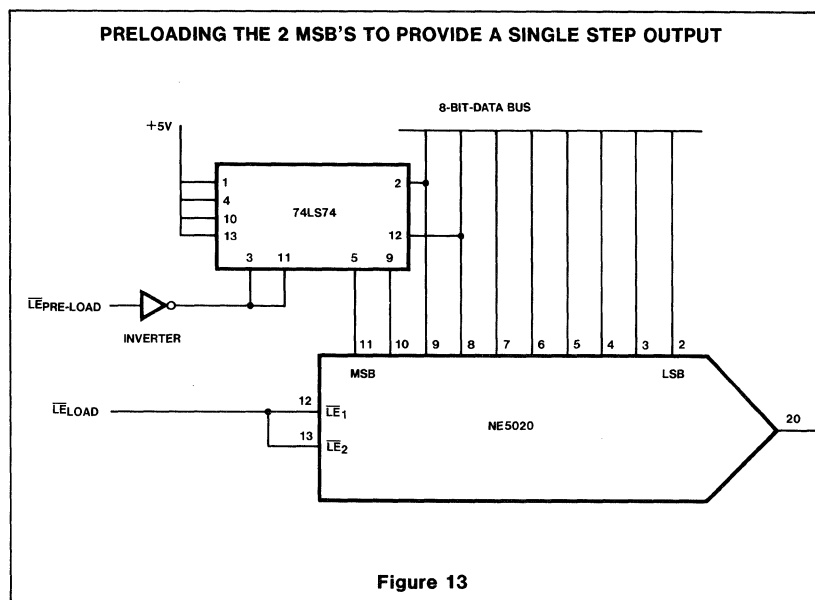


Figure 13

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a VREFADJ (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only VREF adjustment but also full scale output adjust. Notice that the VREFADJ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the VREFADJ pin and observing good layout practices.

The VREF out node can drive loads greater than the DAC VREF input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through QR with a 5 volt VREF. This current sets the input bias to the ladder network. Data bit 9 (DB9)(Q9), when turned on, will mirror this current and will contribute 1mA to the output. DB8 (Q8) will contribute 1/2 of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}} \left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024} \right)$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/ μ sec and source impedances at the VREF INPUT greater than 5k Ω should be avoided to maintain stability.

The -VREF INPUT pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode +VREF INPUT is grounded and the negative reference is tied directly to the -VREF INPUT. The -VREF INPUT contains a 5k Ω resistor that matches a like resistor in the +VREF INPUT to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at 15V/ μ sec and settle to within $\pm 1/2$ LSB in 5 μ sec. These times are typical when driving the rated loads of $R_L \geq 5k$ and $C_L \leq 50pF$ with recommended values of $C_{FF} = 1nF$ and $C_{FB} = 30pF$. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip RFB resistor. RFB is matched to RREF and RBIP to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition IOUT will limit at $\pm 15mA$ typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, RBIP, to offset the output voltage by 5 volts to obtain -5V to +5V output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to $(V_{REF IN} - V_{sum node}) \div RBIP$, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), $(2mA - 1mA)5k = 5V$ will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and $V_{OUT} = -(5k)(1mA) = -5V$. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim $V_{OUT} = 0.00$ with the MSB high or $V_{OUT} = -5.0V$ with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R2 that counteracts the error current. Adjusting potentiometer R1 until VOUT equals 0.000 volts in the unipolar mode or -5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R3 is adjusted until VOUT equals 9.99023V. In many applications where the absolute accu-

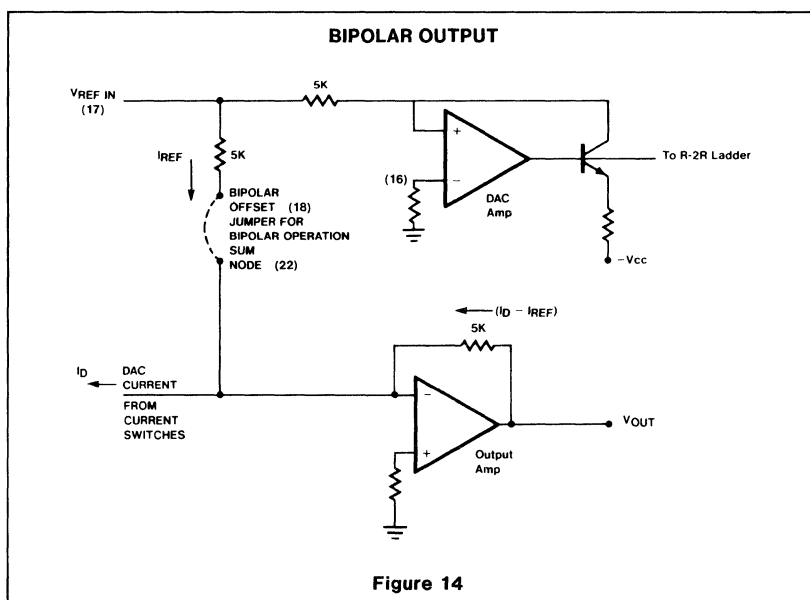


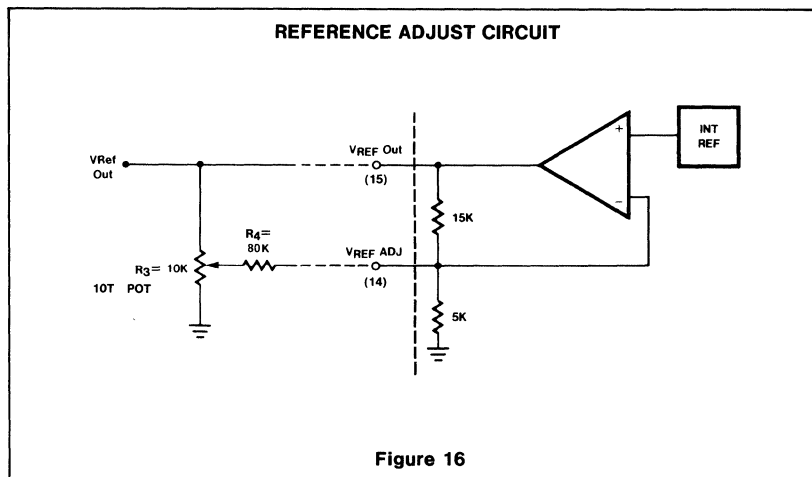
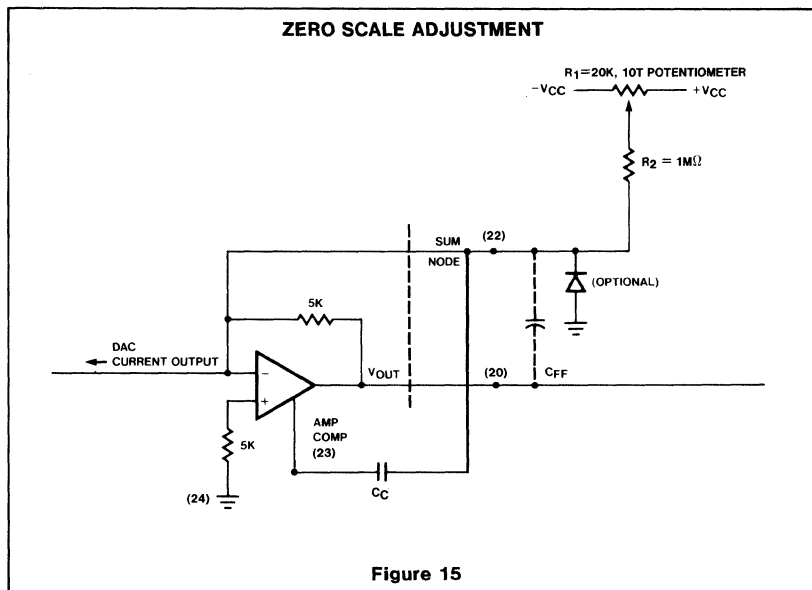
Figure 14



racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF} , R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity,

they match and track in value closely over wide ambient temperature variations. Typical matching is less than $\pm 0.3\%$ which implies that typical full scale (or gain) error is less than $\pm 0.3\%$ of ideal full scale value.



DESCRIPTION

The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the Sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2KΩ load. The logic input is compati-

ble with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the Sample mode occurring when the logic input is high. It is available in 8-lead TO-5 and 8-pin plastic DIP packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_J25°C
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at C_h = 0.01μF
- Low input offset: 1mV (typical)
- 0.002% gain accuracy with R_L = 2kΩ
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation (package limitation) ¹	500	mW
Operating ambient temperature range		
SE5537	-55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	-65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage ²	+7, -30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. The maximum junction temperature of the SE5537 is 150°C and for the NE5537 is 100°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θ_{ja}) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BLOCK DIAGRAM

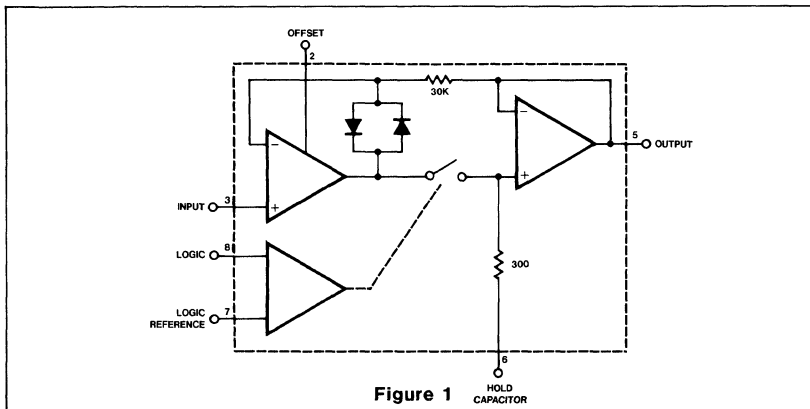
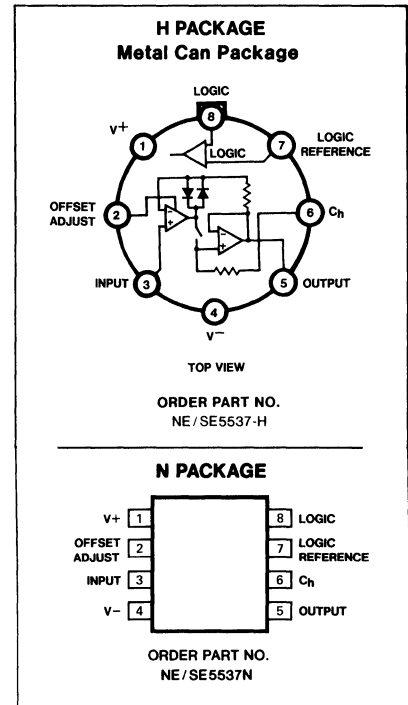


Figure 1

PIN CONFIGURATION



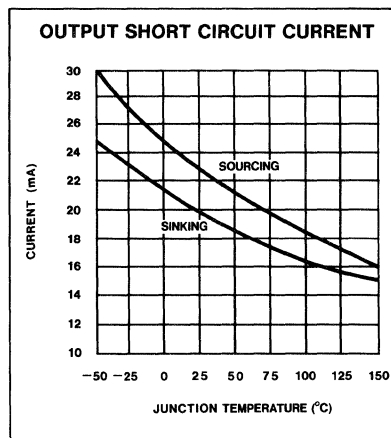
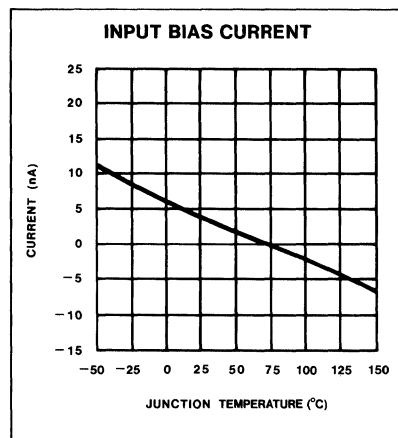
ELECTRICAL CHARACTERISTICS³

PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ⁶	$T_j = 25^\circ\text{C}$ Full temperature range		1	3 5		2	7 10	mV mV
Input bias current ⁶	$T_j = 25^\circ\text{C}$ Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	$T_j = 25^\circ\text{C}$		10^{10}			10^{10}		Ω
Gain error	$T_j = 25^\circ\text{C}$, $-10\text{V} \leq V_{IN} \leq 10\text{V}$, $R_L = 2\text{K}$ $-11.5\text{V} \leq V_{IN} \leq 11.5\text{V}$, $R_L = 10\text{K}$ Full temperature range		0.002	0.007 0.02		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	$T_j = 25^\circ\text{C}$, $C_h = 0.01\mu\text{F}$	86	96		80	90		dB
Output impedance	$T_j = 25^\circ\text{C}$, "HOLD" mode full temperature range		0.5	2 4		0.5	4 6	Ω
"HOLD" Step ⁴	$T_j = 25^\circ\text{C}$, $C_h = 0.01\mu\text{F}$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply current ⁶	$T_j = 25^\circ\text{C}$		4.5	6.5		4.5	7.5	mA
Logic and logic reference input current	$T_j = 25^\circ\text{C}$		2	10		2	10	μA
Leakage current into hold capacitor ⁶	$T_j = 25^\circ\text{C}$ hold mode ⁵		6	50		6	100	pA
Acquisition time to 0.1%	$V_{OUT} = 10\text{V}$, $C_h = 1000\text{pF}$ $C_h = 0.01\mu\text{f}$		4 20			4 20		μs μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\text{V}$		5			5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential logic threshold	$T_j = 25^\circ\text{C}$	0.8	1.4	2.4	0.8	1.4	2.4	V

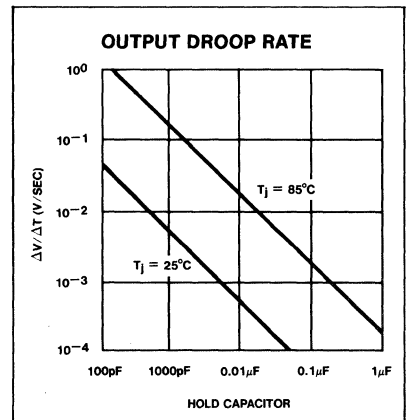
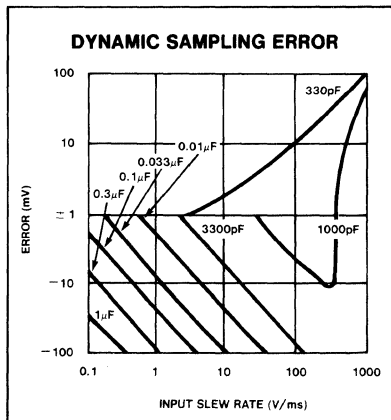
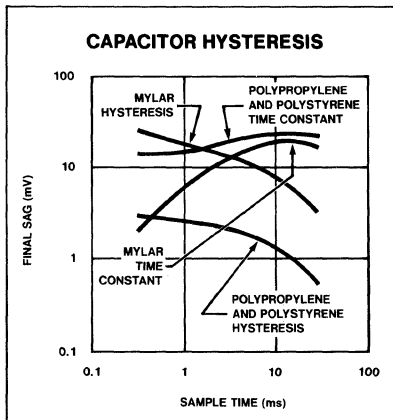
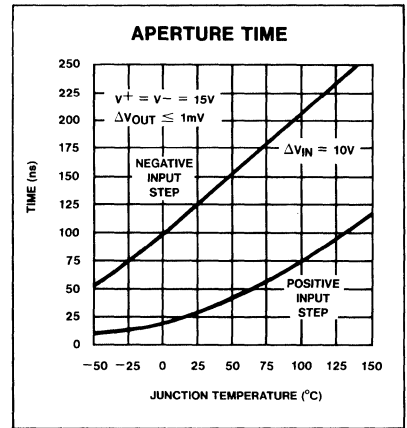
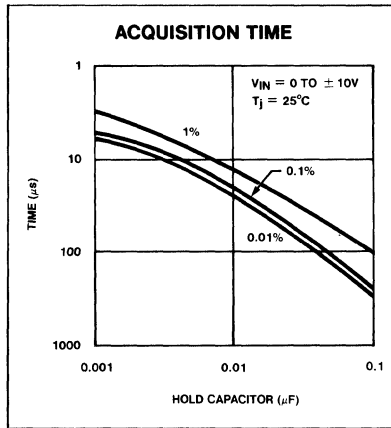
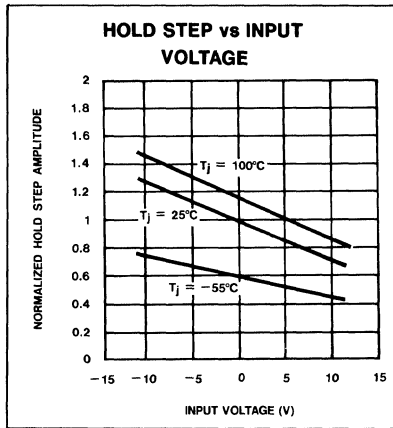
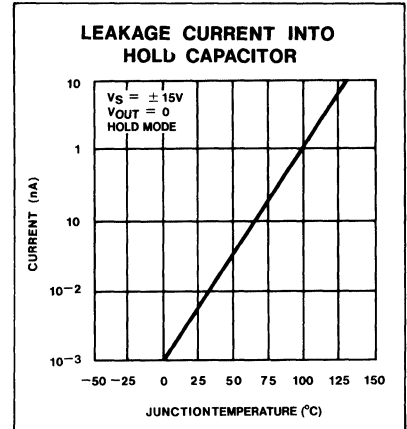
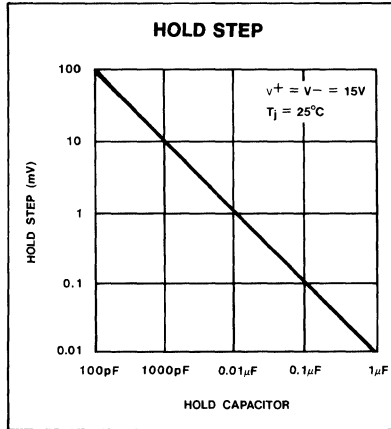
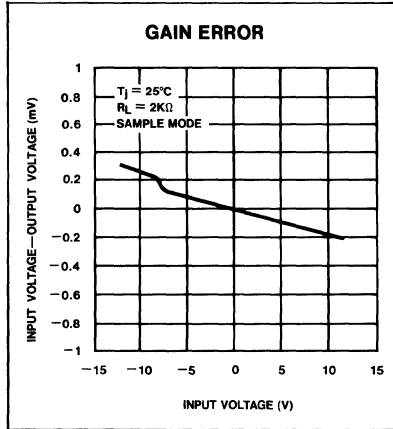
NOTES

- Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15\text{V}$, $T_j = 25^\circ\text{C}$, $-11.5\text{V} \leq V_{IN} \leq 11.5\text{V}$, $C_h = 0.01\mu\text{F}$, and $R_L = 2\text{k}\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
- Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
- Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
- These parameters guaranteed over a supply voltage range of ± 5 to $\pm 18\text{V}$.

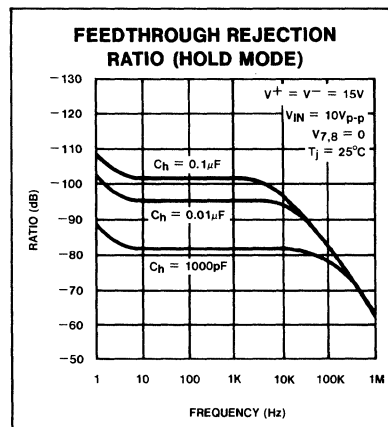
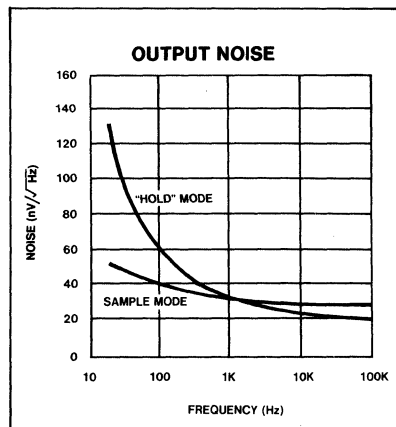
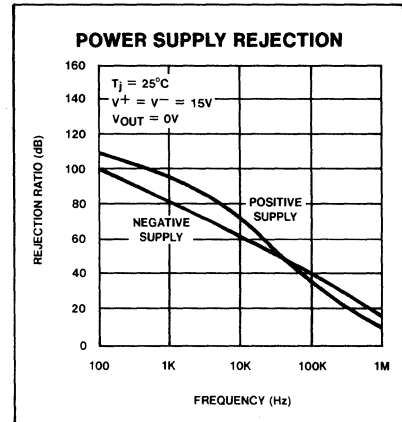
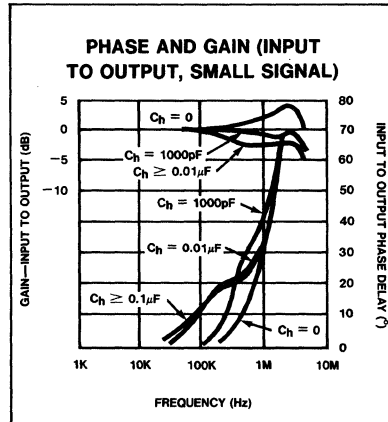
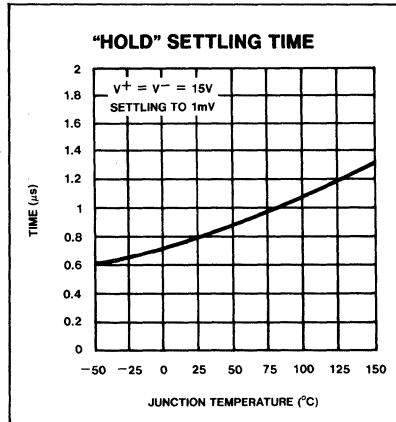
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



APERTURE TIME: The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

BANDWIDTH: The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

EFFECTIVE APERTURE DELAY: The time difference between the hold command and the time at which the input signal is at the held voltage.

FIGURE OF MERIT: The ratio of the available charging current during sample mode to the leakage current during hold mode.

HOLD-MODE DROOP: The output voltage change per unit of time while in hold. Commonly specified in V/s, $\mu\text{V}/\mu\text{s}$ or other convenient units.

HOLD-MODE FEEDTHROUGH: The percentage of an input sinusoidal signal that is measured at the output of a sample-and-hold when it's in hold mode.

HOLD SETTLING TIME: The time required for the output to settle within 1mV of final value after the "hold" logic command.

SAMPLE-TO-HOLD OFFSET ERROR: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

SLEW RATE: The fastest rate at which the sample & hold output can change (specified in V/ μs).

HOLD STEP: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

SAMPLE AND HOLD

INTRODUCTION

For many years designers have used the sample and hold (or track and hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample and hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample and hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog to digital converter products available today the "dc memory" of the sample and hold can be

easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample and hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

ACQUISITION TIME: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

APERTURE DELAY TIME: The time elapsed from the hold command to the opening of the switch.

APERTURE JITTER: Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

DYNAMIC SAMPLING ERROR: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

GAIN ERROR: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

THRESHOLD: Level shall be defined as that level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample and hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference figure 1.

The block diagram of the NE5537 is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to *all* sample and hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. Reference figure 2. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, & CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (pin 8 is 1.4 volts higher than pin 7) and presents a load of 5 microamperes to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This

amplifier, whose input impedance is effectively:

$$R = R_{IN}(A_{OL}) / (1 + 1/A)$$

where

$$R = \text{Effective input impedance}$$

$$R_{IN} = \text{Open loop input impedance}$$

$$A_{OL} = \text{Open loop gain}$$

$$A = \text{AC loop gain}$$

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the NE5537 is less than 10 μ sec, (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2k Ω .

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of figure 3, the sample and hold circuit is used to supply a "variable" reference to the digital to analog converter. As the input reference varies, the output will change in accordance with equation 1, shown in figure 3.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's used are the Signetics SE/NE 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for

instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC Zeroing

DC Zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1k Ω potentiometer which has one end tied to V⁺ and the other end tied through a resistor to ground. The resistor should be selected to give \approx 0.6mA through the 1K Ω potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample and hold circuits. There exist finite phase delays through the sample and hold circuit causing an input-output phase differential for moving signals. In addition, the series protection resistor (300 Ω to pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10kHz. Maximum dV/dt is 0.6V/ μ s. With no analog phase delay and 100ns logic delay, one could expect up to (0.1 μ s) (0.6V/ μ s) = 60mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive going input would give a \pm 60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μ s) (0.6V/ μ s) = -96mV (analog) for a total of -36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this prob-

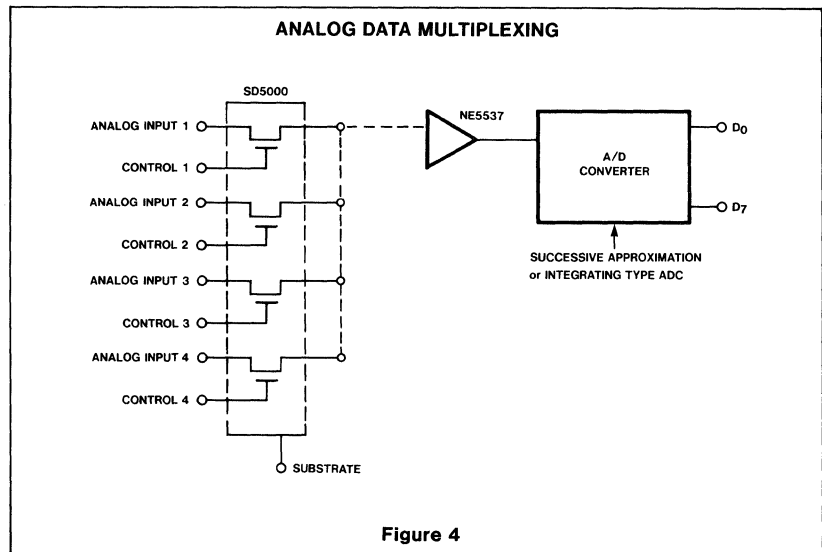
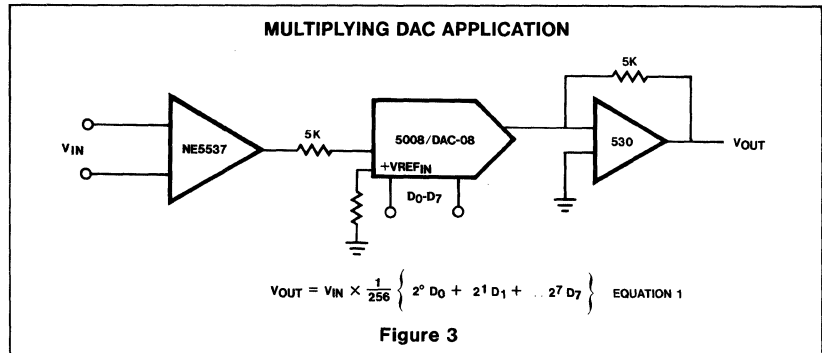
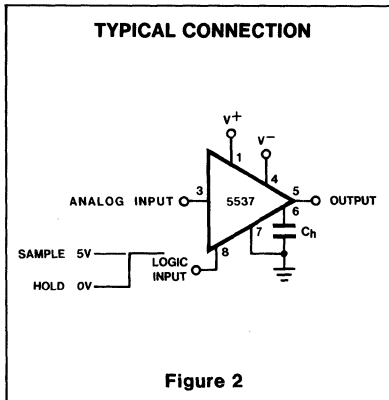
lem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a P.C. card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample and hold systems.
2. Reference should be made to Design Engineering, volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample and hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

TYPICAL APPLICATIONS



SECTION II

RADIO CIRCUITS

Section 11—RADIO CIRCUITS

CA3089	FM-IF System	359
MC1496/1596	Balanced Modulator-Demodulator	364
NE544/644	Servo Amplifier	367
NE5044	Programmable Seven Channel RC Encoder	373
NE5045	Seven Channel RC Decoder	376
NE5046	2-Channel RC Decoder	379
TCA440	AM Receiver Circuit	381
μ A758	FM Stereo Multiplex Decoder, Phase Locked Loop	388

NEW PRODUCTS

CA3189	FM-IF System—Available 1st Quarter 1981
LM1870	FM Decoder with Stereo/Mono Switching—Available 3rd Quarter 1981

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8 to +18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

FEATURES

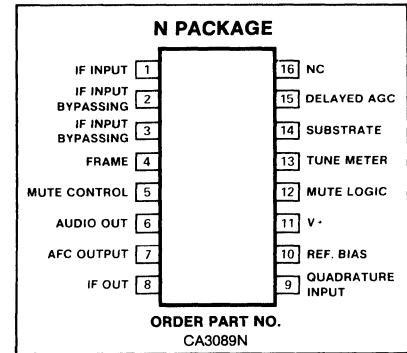
- Exceptional limiting sensitivity: 10µV typ. at -3dB point
- Low distortion: 0.1% typ. (with double-tuned coil)

- Single-coil tuning capability
- High recovered audio: 400mV typ.
- Provides specific signal for control of interchannel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- Provides delayed AGC voltage for RF amplifier
- Provides a specific circuit for flexible AFC
- Internal supply/voltage regulators

APPLICATIONS

- High-fidelity FM receivers
- Automotive FM receivers
- Communications FM receivers

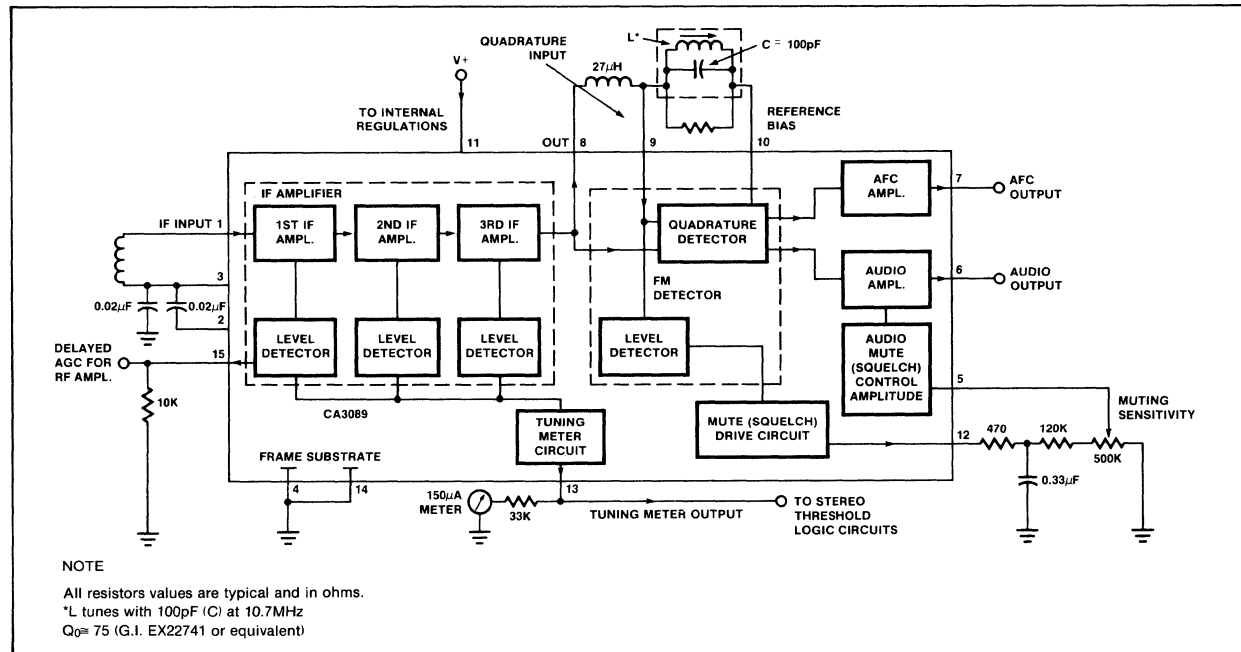
PIN CONFIGURATION



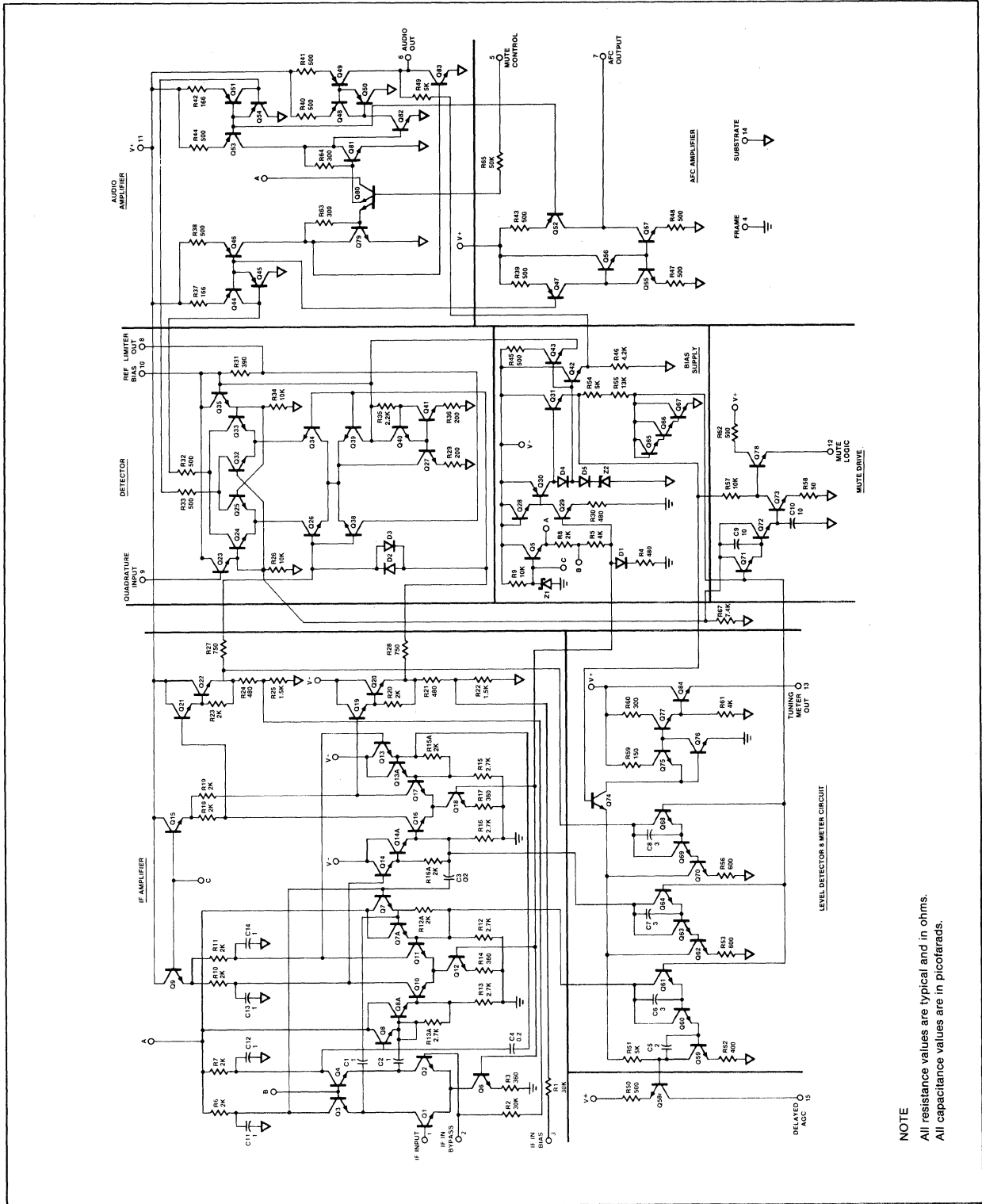
ABSOLUTE MAXIMUM RATINGS

	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC Current (out of terminal 15)	2	mA
Device dissipation:		
Up to T _A = 60°C	600	mW
Above T _A = 60°C	derate linearly	
	6.7	mW/°C
Ambient temperature range:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead temperature (during soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE
All resistance values are typical and in ohms.
All capacitance values are in picofarads.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$ unless otherwise specified.

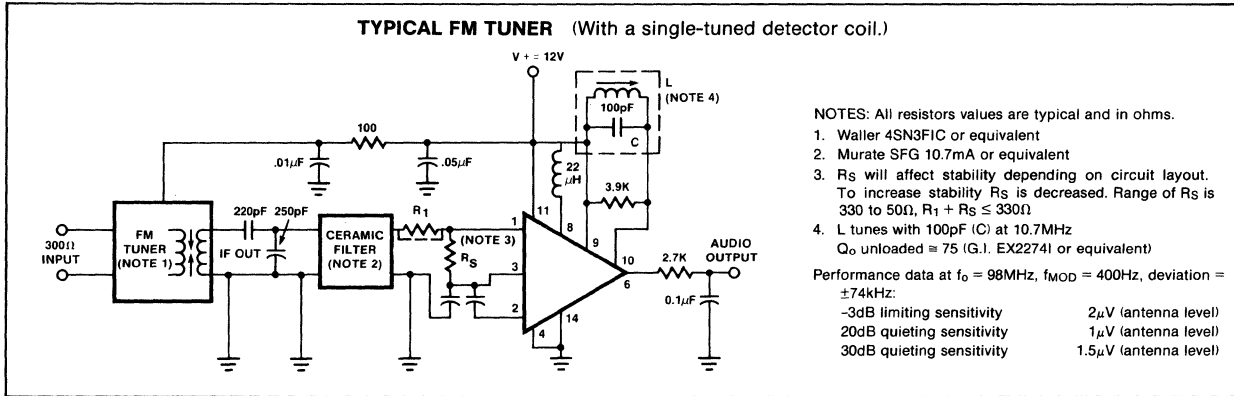
PARAMETER	TEST CONDITIONS	CA3089			UNIT
		Min	Typ	Max	
STATIC (DC) CHARACTERISTICS					
I_{11} Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages: ⁴					
V_1 Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2 Terminal 2 (ac return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3 Terminal 3 (dc bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6 Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.4	V
V_7 Terminal 7 (A.F.C.)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10} Terminal 10 (dc reference)	No signal input, non-muted	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS					
$V_{I(lim)}$ Input limiting voltage (-3dB point) ³			10	30	μV
AMR AM Rejection (terminal 6) ⁴	$V_{IN} = 0.1\text{V}$, $F_0 = 10.7\text{MHz}$, $f_{mod} = 400\text{Hz}$, AM Mod = 30%	45	55		dB
V_O Recovered audio voltage (terminal 6) ³		300	400	500	mV
Total harmonic distortion: ¹					
THD Single tuned (terminal 6) ³			0.5	1.0	%
THD Double tuned (terminal 6) ⁴	$f_{mod} = 400\text{Hz}$, $V_{IN} = 0.1$		0.1		%
S+N/N Signal plus noise to noise ratio (terminal 6) ³	Deviation = $\pm 75\text{kHz}$	60	67		dB
MU_{IN} Mute input (terminal 5)	$V_5 = 2.5\text{V}$		70		dB
MU_{OUT} Mute output (terminal 12)	$V_{IN} = 50\mu\text{V}$ $V_{IN} = 0\text{V}$	4.0		.5	V V
MTR Meteroutput (terminal 13)	$V_{IN} = 0.1\text{V}$	3.5	4.5		V
	$V_{IN} = 500\mu\text{V}$	1.0	1.5		V
	$V_{IN} = 0\text{V}$.7	V
AGC Delayed AGC (terminal 15)	$V_{IN} = 0.1\text{V}$.5	V
	$V_{IN} = 10\mu\text{V}$	4.0	5.0		V
THD Double tuned (terminal 6) ⁴	$f_{mod} = 400\text{Hz}$ $V_{IN} = 0.1$		0.1		%

NOTES

1. THD characteristics and Audio Level are essentially a function of the phase and Q characteristics of the network connected between terminals 8, 9 and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.



TEST CIRCUITS



SYSTEM DESIGN CONSIDERATIONS

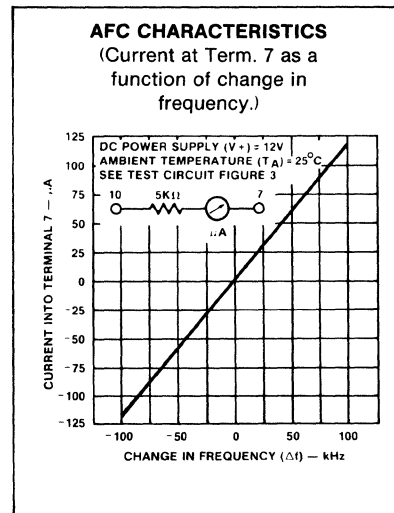
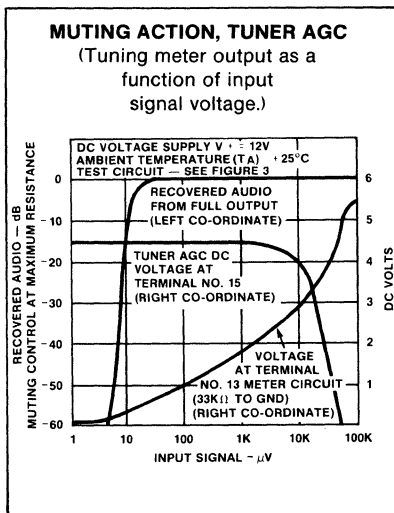
The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input by-pass capacitors should be located close to the input terminals and the values should not be

large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

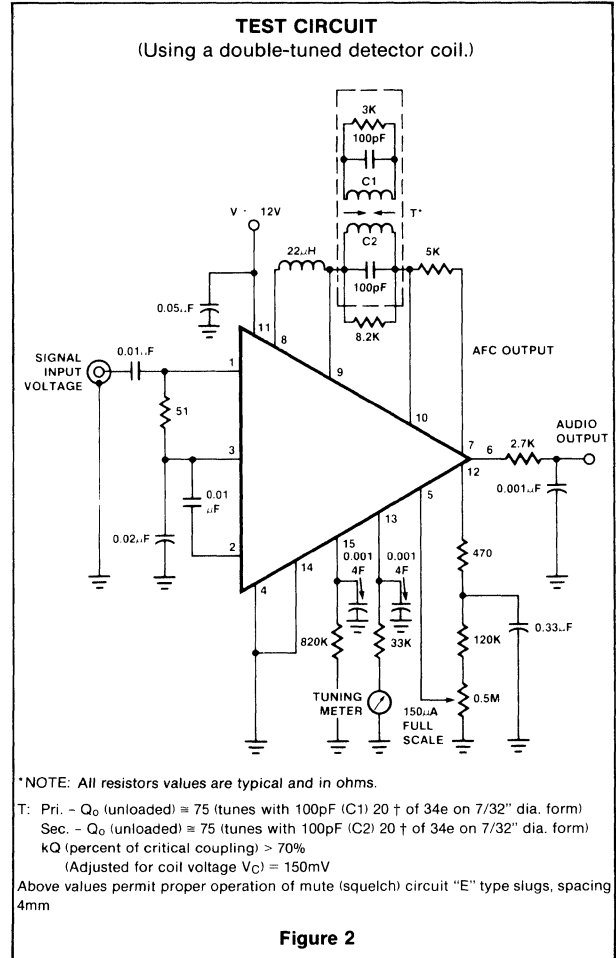
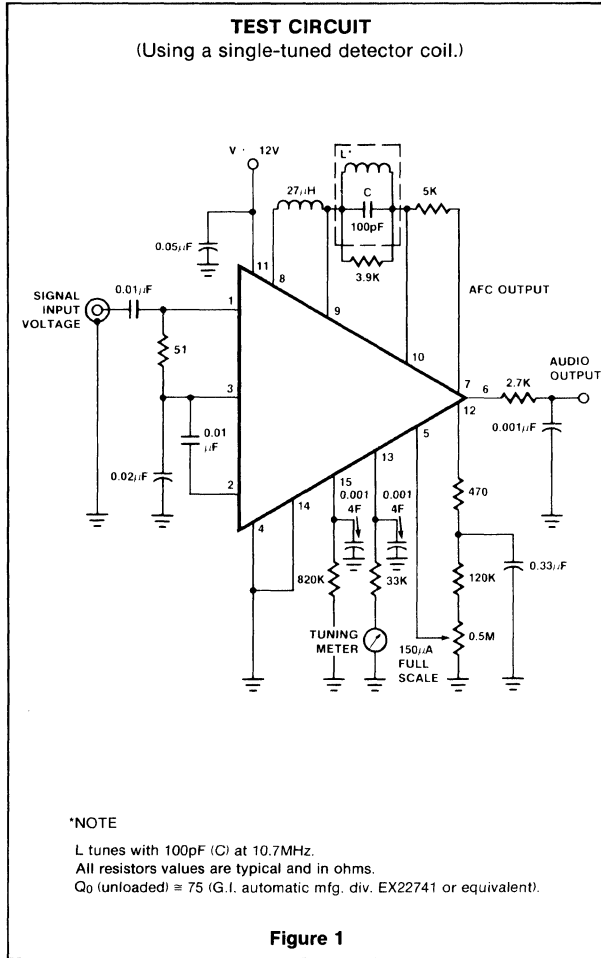
The input impedance of the CA3089 is approximately 10,000 ohms. It is not recommended to match this impedance. The value

of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS



TEST CIRCUITS



DESCRIPTION

The MC1496 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55°C to +125°C. The MC 1496 is intended for applications within the range of 0°C to +70°C.

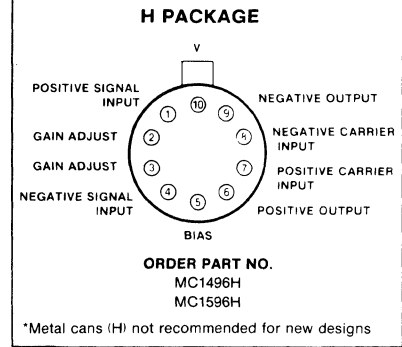
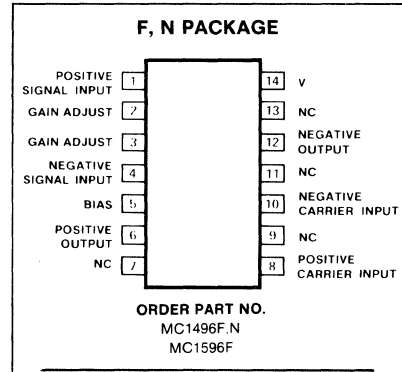
FEATURES

- Excellent carrier suppression
65dB typ @ 0.5MHz
50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection—85dB typ

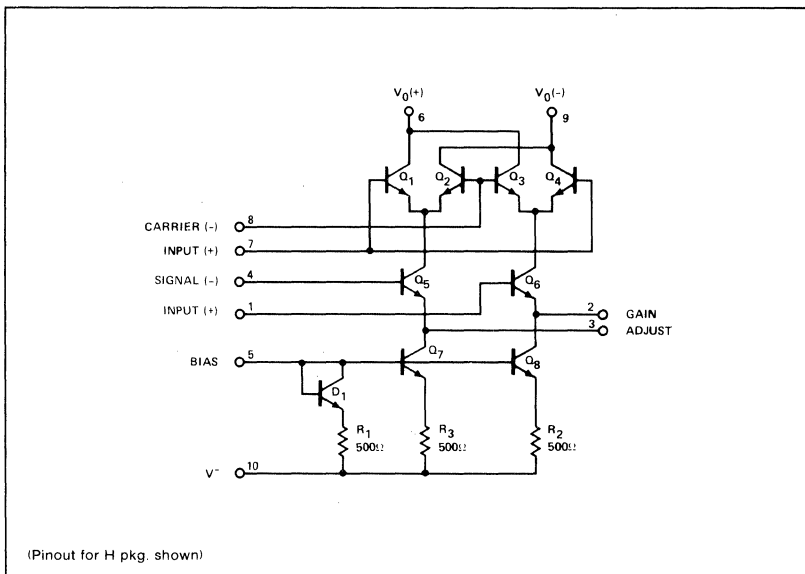
APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage ^{1,2}	30	V
Differential input signal (V ₇ -V ₈)	±5.0	V
Differential input signal (V ₄ -V ₁)	(5 ± 15 R _e)	V
Input signal (V ₂ -V ₁ , V ₃ -V ₄)	5.0	V
Bias current (I ₅)	10	mA
Power dissipation (pkg. limitation)		
N package	900	mW
Operating temperature range		
MC1496	0 to +70	°C
MC1596	-55 to +125	°C
Storage temperature range	-65 to +150	°C

NOTES

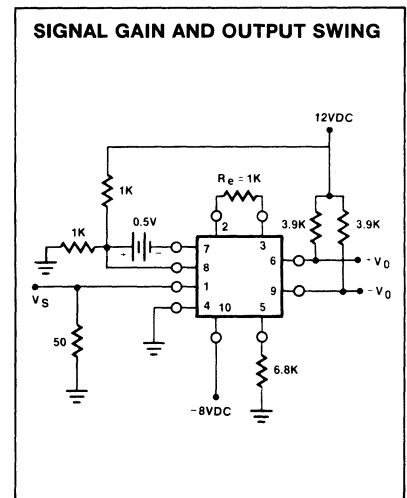
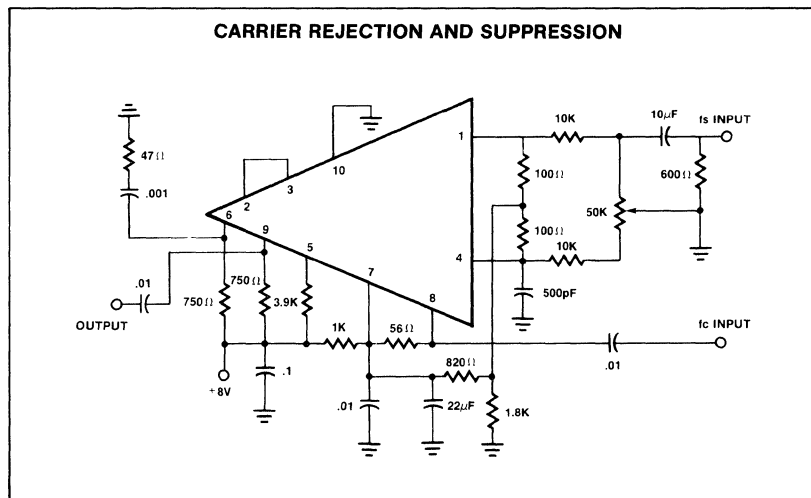
1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to H package pinout only.

MC1496-F,N,H
MC1596-F,H

DC ELECTRICAL CHARACTERISTICS $V^+ = +12\text{Vdc}$, $V^- = -8.0\text{Vdc}$, $I_S = 1.0\text{mA}$, $R_L = 3.9\text{k}\Omega$, $R_e = 1.0\text{k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{ip} C_{ip}	Single-ended input impedance Parallel input resistance Parallel input capacitance		200 2.0			200 2.0		$\text{k}\Omega$ pF
R_{op} C_{op}	Single-ended output impedance Parallel output resistance Parallel output capacitance		40 5.0			40 5.0		$\text{k}\Omega$ pF
I_{bS} I_{bC}	Input bias current $I_{bS} = \frac{I_1 + I_4}{2}$ $I_{bC} = \frac{I_7 + I_8}{2}$		12 12	25 25		12 12	30 30	μA μA
I_{ioS} I_{ioC}	Input offset current $I_{ioS} = I_1 - I_4$ $I_{ioC} = I_7 - I_8$		0.7 0.7	5.0 5.0		0.7 0.7	7.0 7.0	μA μA
$T_{cI_{io}}$ I_{oo}	Average temperature coefficient of input offset current Output offset current $I_6 - I_9$		2.0 14			2.0 15		$\text{nA}/^\circ\text{C}$ μA
$T_{cI_{oo}}$ V_o	Average temperature coefficient of output offset current Common-mode quiescent Output voltage (Pin 6 or Pin 9)		90 8.0			90 8.0		$\text{nA}/^\circ\text{C}$ Vdc
I_{D+} I_{D-}	Power supply current $I_6 + I_9$ I_{10}		2.0 3.0	3.0 4.0		2.0 3.0	4.0 5.0	mA mA
P_D	DC power dissipation		33			33		mW

NOTE
Pin number references pertain to H package pinout only.



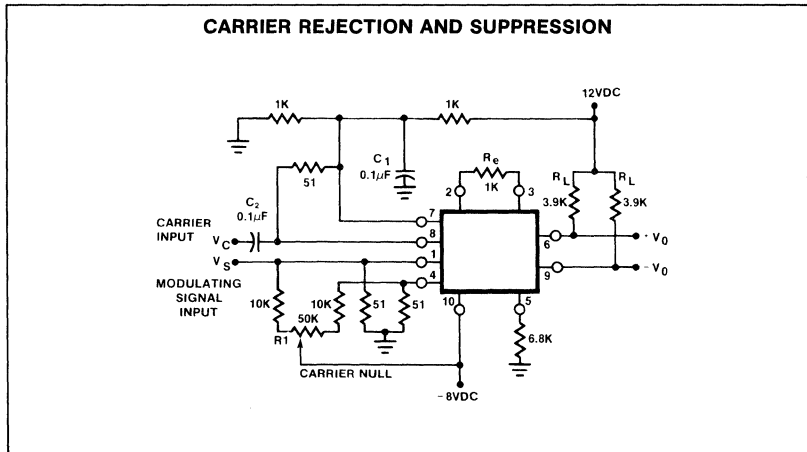
MC1496-F,N,H
MC1596-F,H

AC ELECTRICAL CHARACTERISTICS $V^+ = +12\text{Vdc}$, $V^- = -9.0\text{Vdc}$, $I_S = 1.0\text{mAdc}$, $R_L = 3.9\text{k}\Omega$, $R_e = 1.0\text{k}\Omega$,
 $T_A = +25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CFT} Carrier feedthrough	$V_C = 60\text{mVrms}$ sinewave and offset adjusted to zero $f_C = 1.0\text{kHz}$ $f_C = 10\text{MHz}$ $V_C = 300\text{mVp-p}$ squarewave: Offset adjusted to zero $f_C = 1.0\text{kHz}$ Offset not adjusted $f_C = 1.0\text{kHz}$		40 140			40 140		μVrms
			0.04 20	0.2 100		0.04 20	0.4 200	mVrms
V_{CS} Carrier suppressions	$f_S = 10\text{kHz}$, 300mVrms sinewave $f_C = 500\text{kHz}$, 60mVrms sinewave $f_C = 10\text{MHz}$, 60mVrms sinewave	50	65 50		40	65 50		dB
BW_{3dB} Transadmittance bandwidth (Magnitude) ($R_L = 50\Omega$)	Carrier input port, $V_C = 60\text{mVrms}$ sinewave $f_S = 1.0\text{kHz}$, 300mVrms sinewave Signal input port, $V_S = 300\text{mVrms}$ sinewave $ V_C = 0.5\text{Vdc}$		300			300		MHz
				80			80	MHz
AV_S Signal gain	$V_S = 100\text{mVrms}$; $f = 1.0\text{kHz}$ $ V_C = 0.5\text{Vdc}$	2.5	3.5		2.5	3.5		V/V
CMV Common-mode input swing	Signal port, $f_S = 1.0\text{kHz}$		5.0			5.0		Vp-p
ACM Common-mode gain	Signal port, $f_S = 1.0\text{kHz}$ $ V_C = 0.5\text{Vdc}$		-85			-85		dB
DV_{OUT} Differential output voltage swing capability			8.0			8.0		Vp-p

NOTE

Pin number references pertain to H package pinout only.



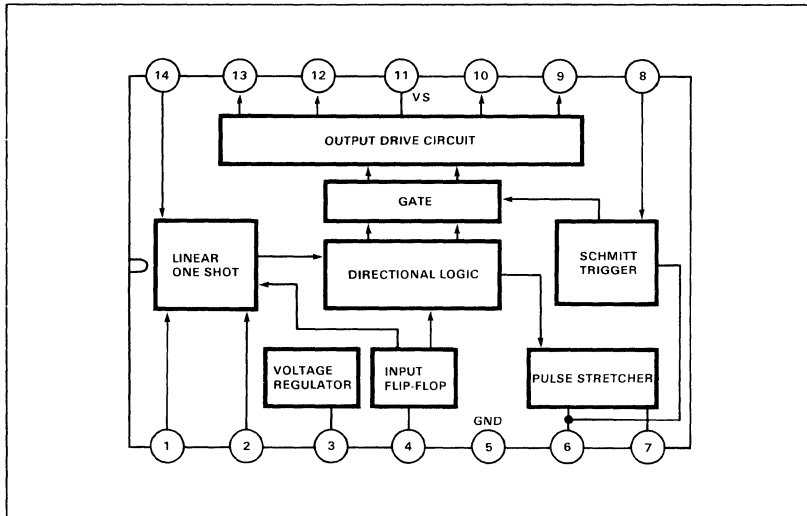
DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

- 500mA load current capability
- Bidirectional bridge output with single power supply
- Low standby power drain
- Adjustable deadband and trigger thresholds
- High linearity, 0.5% maximum error
- Output drive for external PNP transistors (optional)
- Wide supply voltage range

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
V_+ Supply voltage	6.0	V
I_O Output current	500	mA
T_A Operating temperature	-20 to +75	$^\circ\text{C}$
T_{stg} Storage temperature	-65 to +150	$^\circ\text{C}$

PIN CONFIGURATIONS

D,N PACKAGE

ORDER PART NO.
NE544N
NE544D

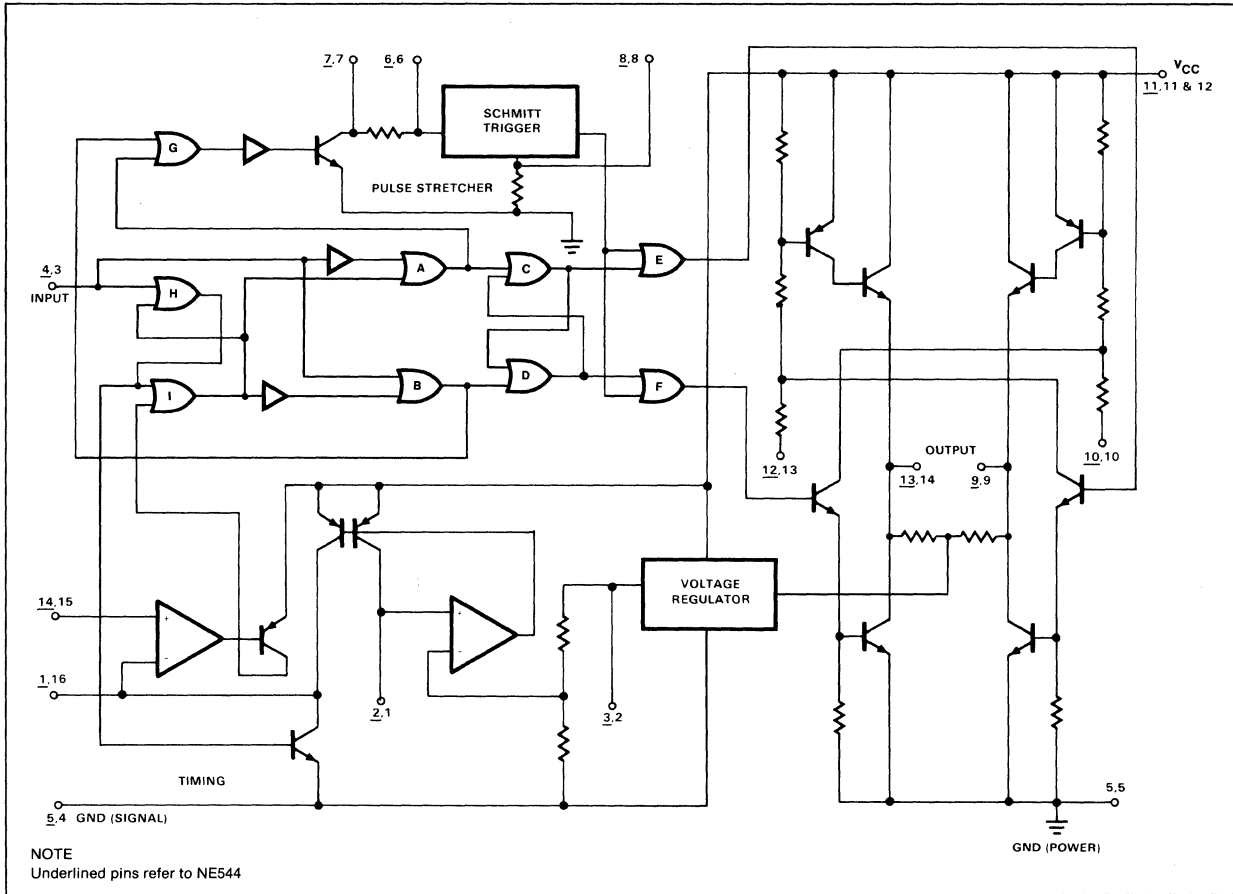
N PACKAGE

Order part no. NE644N

W PACKAGE*

*Pinout same as 644N package
Order part no. NE644W

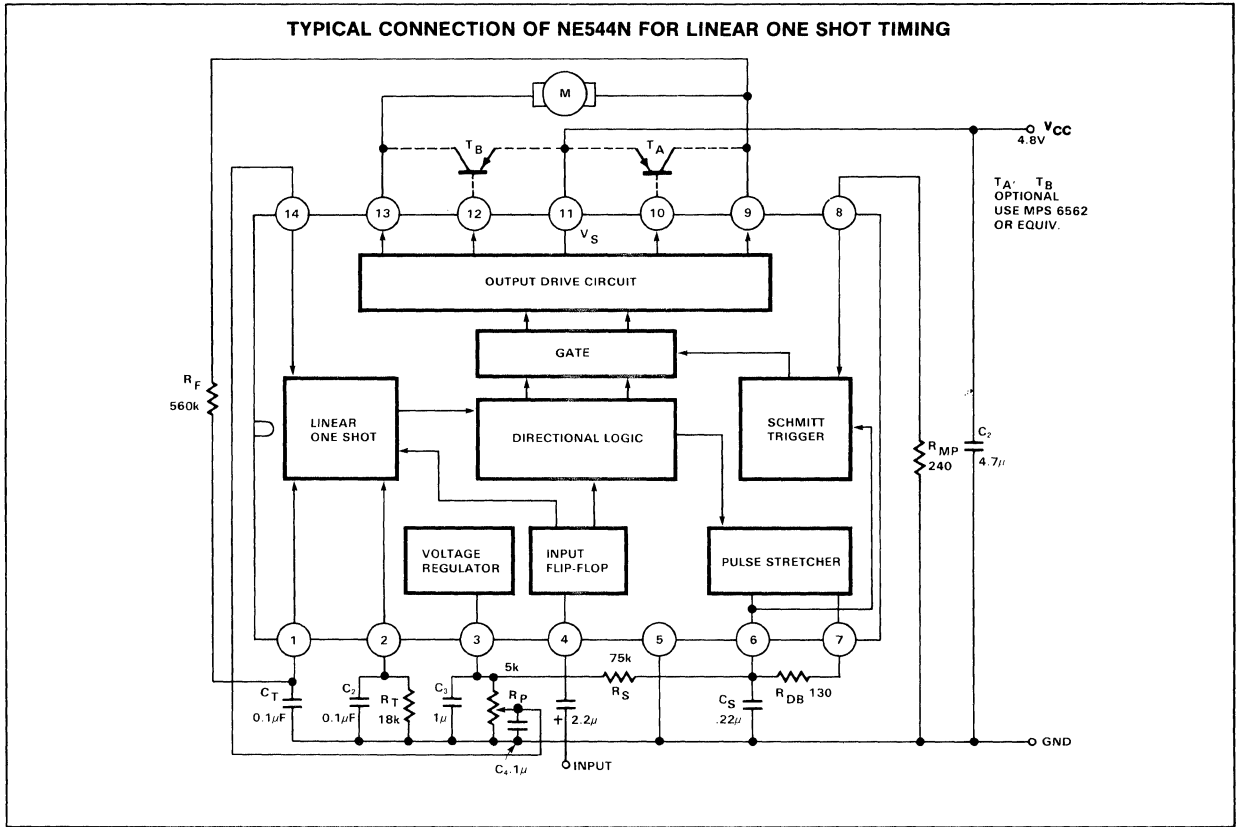
EQUIVALENT CIRCUIT SCHEMATIC

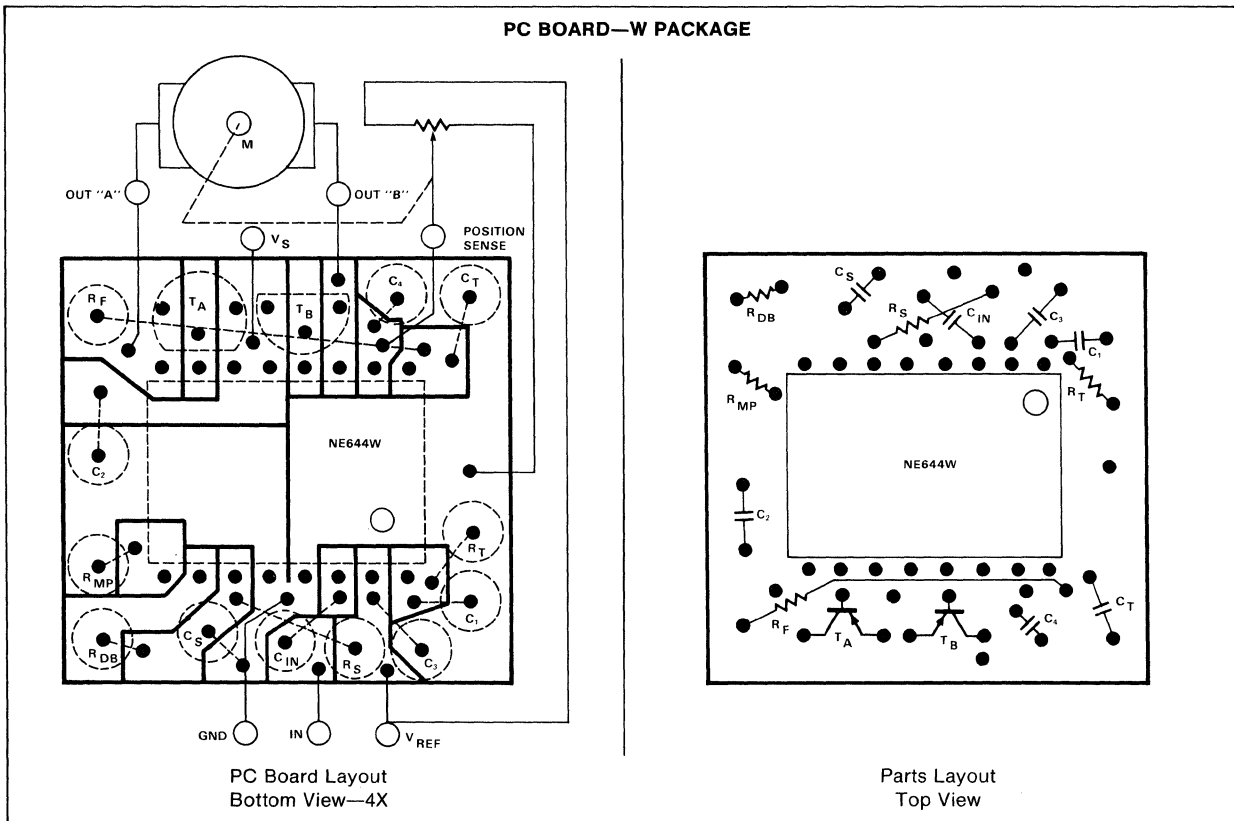
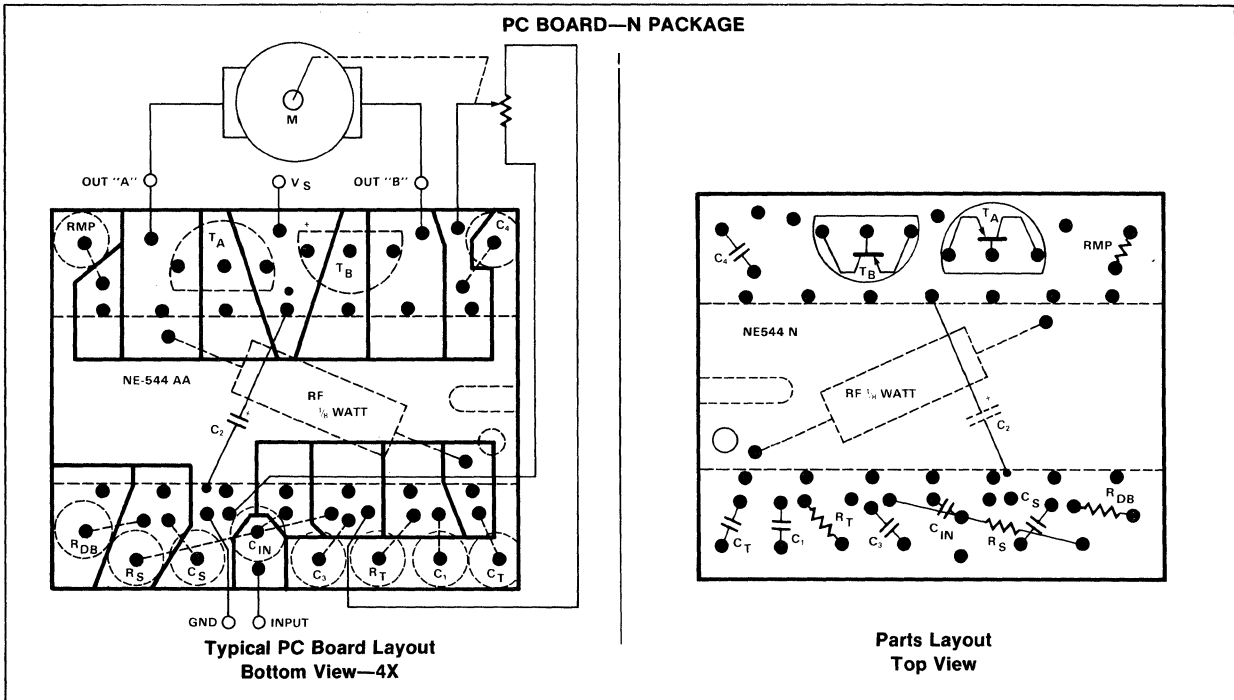


DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = 4.8\text{V}$ unless otherwise specified.

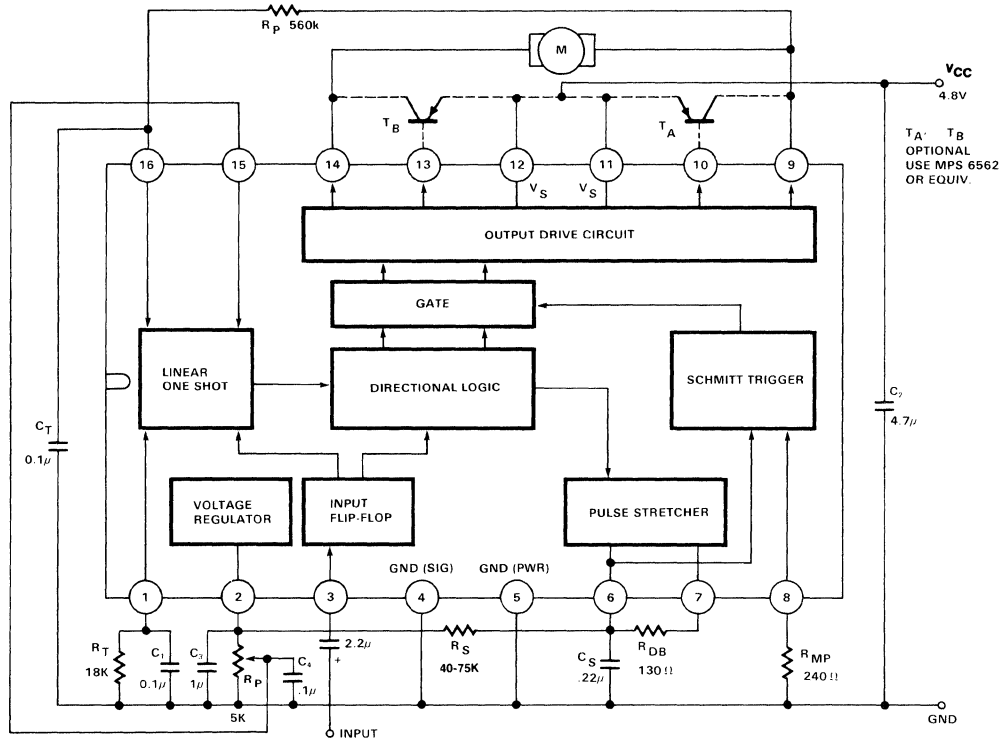
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CC} Supply voltage		3.2	4.8	6	V
I_{CC} Supply current	Pin 11 Quiescent	4.2	5.5	10	mA
V_{TH} Input threshold	Pin 4		1.5		V
			1.4		
Z_{IN} Input resistance	Pin 4		18		k Ω
V_{OL} Output voltage			0.3		V
V_{OH} High	Pin 9 or 13, $I_L = 400\text{mA}$		3.9		
V_{REG} Regulated voltage	Pin 3	2.1	2.5	2.9	V
ΔV_{REG} Regulation	Pin 3 $3.5\text{V} \leq V_{CC} \leq 6\text{V}$		10		mV/V
	Pin 7 $R_{DB} = 0$		1		μs
	One shot temperature coefficient		.01		%/ $^\circ\text{C}$
Standby output voltage	Pin 9 and 13		2.5		V
PNP drive current	Pin 10 and 12		20		mA

TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING



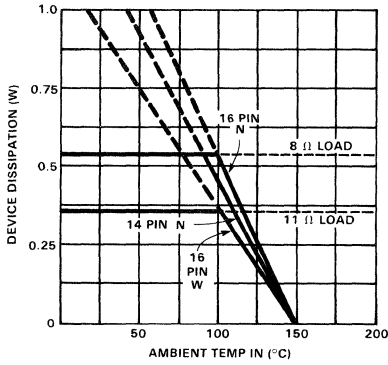


TYPICAL CONNECTION OF NE644W AND NE644N FOR LINEAR ONE SHOT TIMING

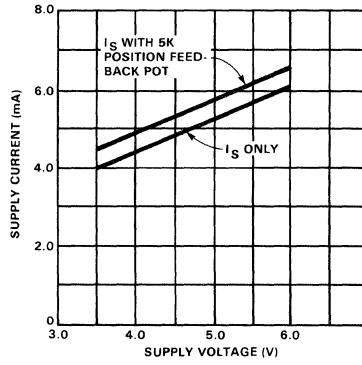


TYPICAL PERFORMANCE CHARACTERISTICS

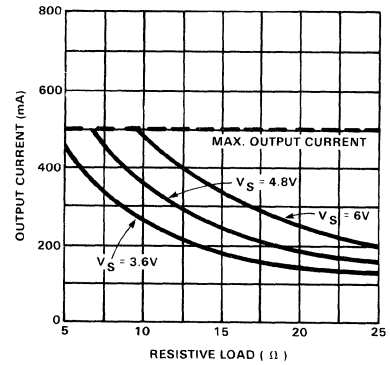
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



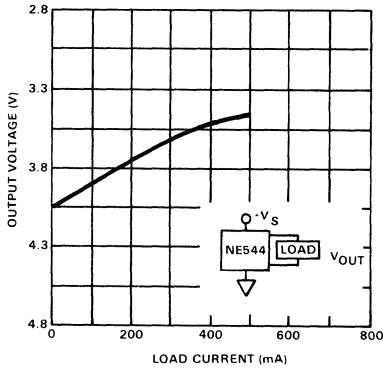
SUPPLY CURRENT vs SUPPLY VOLTAGE



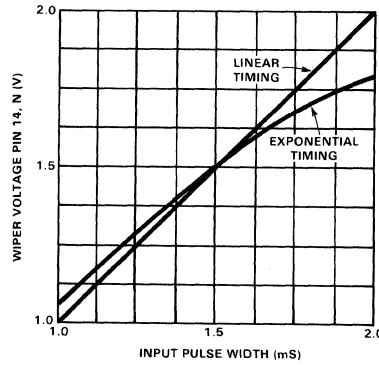
OUTPUT CURRENT vs LOAD RESISTANCE



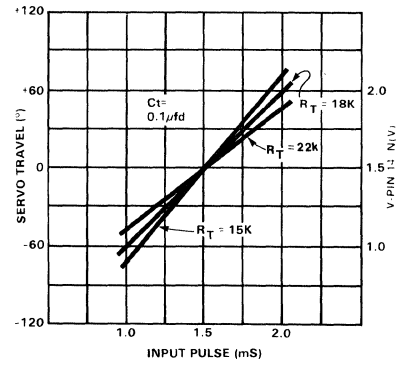
OUTPUT VOLTAGE vs LOAD CURRENT



INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



INPUT PULSE vs SERVO TRAVEL



DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

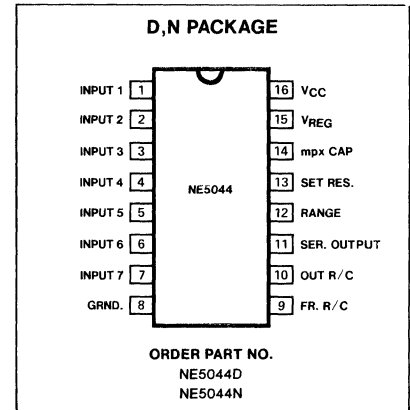
FEATURES

- 3 to 7 channels, externally selectable
- Constant current dual linear ramp for linearity better than .3%
- Internal voltage regulator for low drift
- Wide supply range 4.5 - 16V
- Fixed or variable frame rate set by external R-C
- External control for channel gain or range
- Versatile applications; exponential rates, mixing, dual rate, reversing etc.
- Compatible with all transmission mediums

APPLICATIONS

- Radio controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote Analog/digital data transmission
- Automotive sensor systems

PIN CONFIGURATION

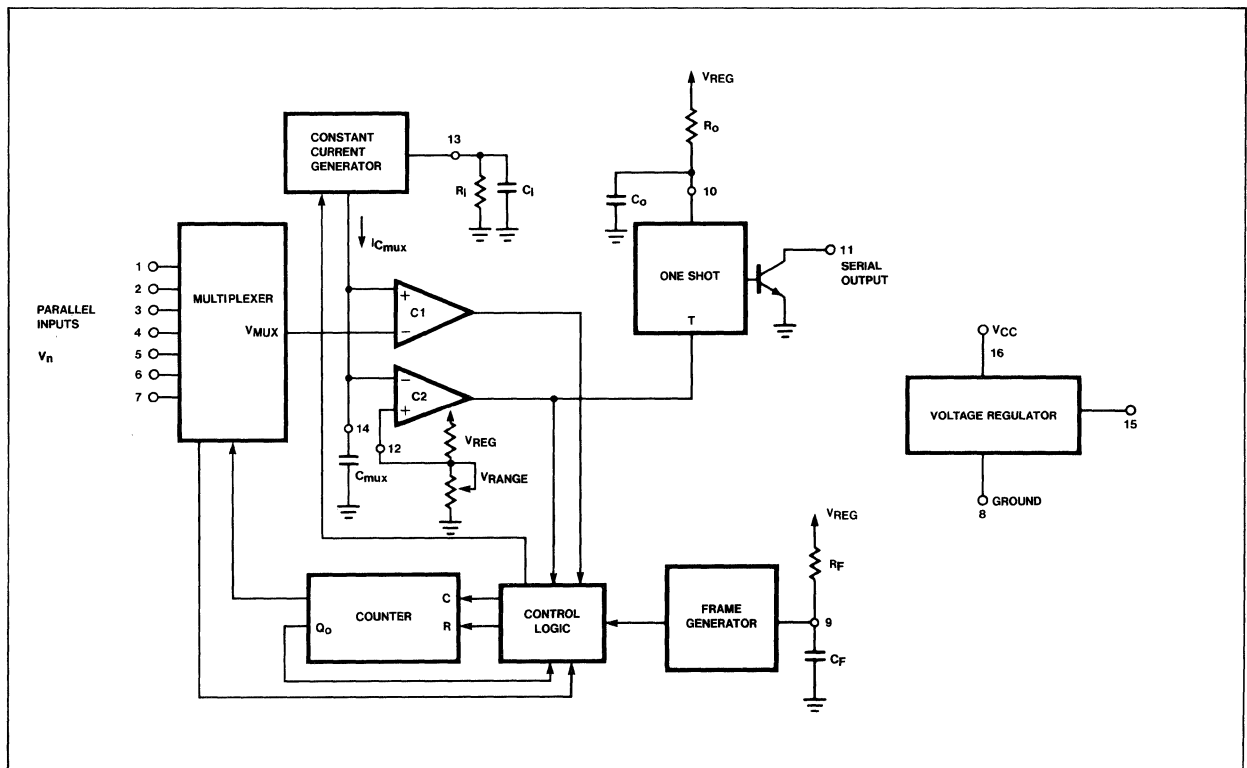


ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
VCC, Supply voltage	17	V
Regulator output current	-25	mA
Serial output peak current	30	mA
Constant current generator	-1	mA
Parallel inputs, range input	0-VREG	V
One shot input, frame generator input	0-VREG	V
Operating temperature	-20 to +75	°C
Storage temperature	-65 to +150	°C

NOTE
1. T_A = 25° unless otherwise stated.

BLOCK DIAGRAM



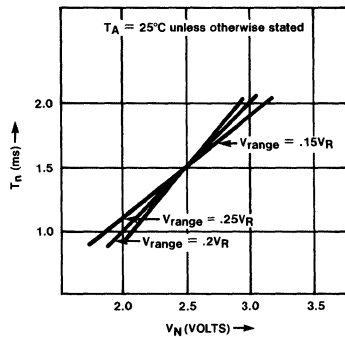
DC ELECTRICAL CHARACTERISTICS Test conditions $T_A = 25^\circ\text{C}$, $V_{CC} = 10\text{V}$ using Test Circuit A unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE 5044			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS ¹ Power supply voltage range Power supply current	Excluding control pots and serial output currents	4.5		16	V
			11	15	mA
V _{REG} VOLTAGE REGULATOR Output voltage Output current Line regulation	$V_R \geq 4.5\text{V}$ $7 \leq V_{CC} \leq 16$	4.5	5.0	5.5	V
				.005	0.2
MULTIPLEXER Input current Input voltage range Crosstalk	$V_n = 2.5\text{v}$ $V_n - V_{\text{Range}} \geq .75\text{V}$		± 30	± 200	nA
			1.5		5
T _n OUTPUT PULSE Position Position linearity error Position tempco Position PSR	$R_I \cdot C_{\text{mux}} = 1.25\text{ms}$ $V_n = .5V_{\text{REG}}; V_{\text{RANGE}} = .2V_{\text{REG}}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $6\text{V} \leq V_{CC} \leq 16\text{V}$	1350	1500	1650	μs
				5	
T ₀ Width Saturation voltage I ₁₁ Leakage current Range input voltage Frame time (Fixed) Inhibit threshold	$R_0 C_0 = 300\mu\text{s}$ $I_0 = 25\text{mA}$ $R_I = 50\text{k}\Omega$ $R_I = 25\text{k}\Omega$ $R_F C_F = 30\text{ms}$	240	285	330	μs
				.6	1
		.75	.05	50	μA
		1.00			V
		17	20	23	ms
				.4	V

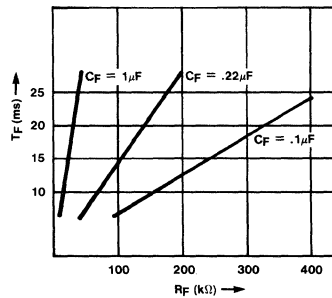
NOTE

- At supply voltages exceeding 12 V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended.

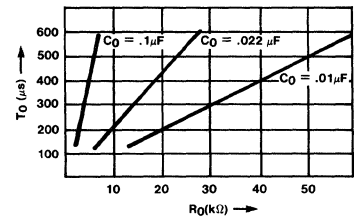
OUTPUT PULSE WIDTH (T_n) vs INPUT VOLTAGE (V_n)



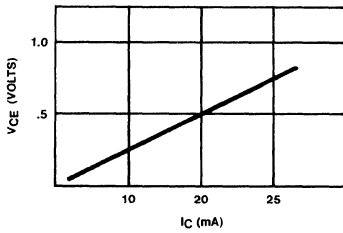
FRAME TIME (T_F) vs R_F



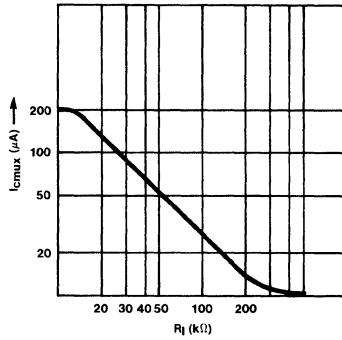
OUTPUT ONESHOT TIME (T₀) vs R₀



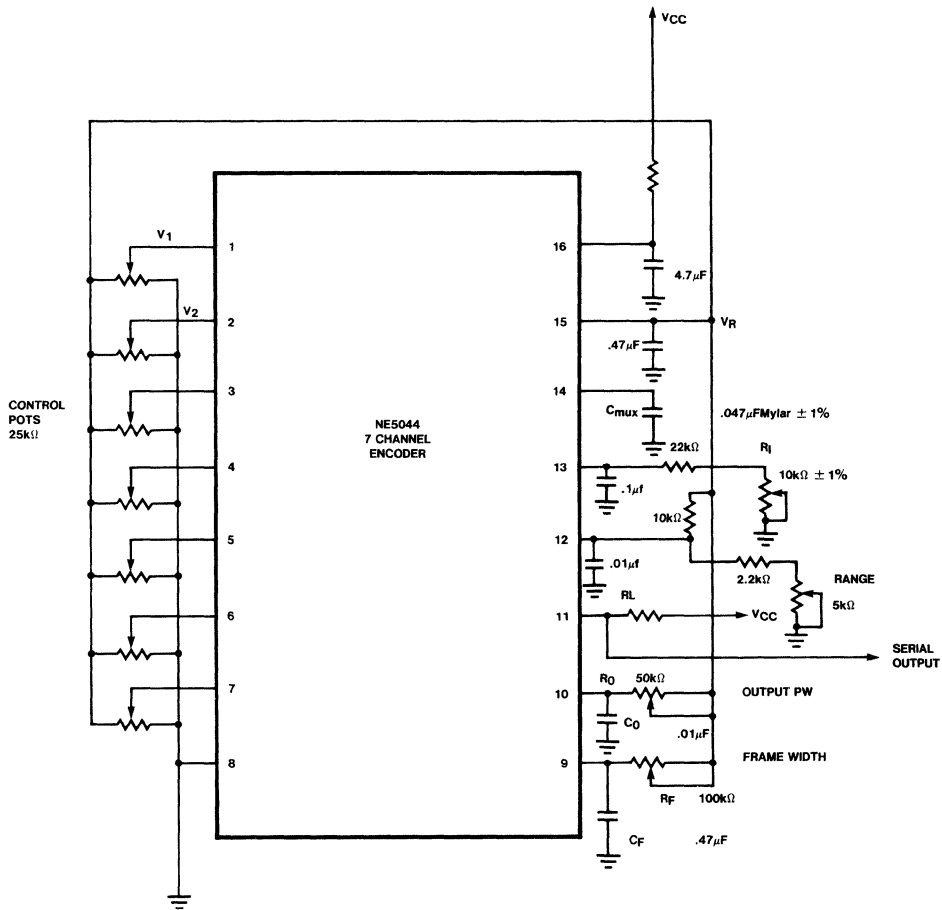
OUTPUT SATURATION VOLTAGE vs OUTPUT CURRENT



CONSTANT CURRENT vs R_I



TEST CIRCUIT A



DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_w = R_s C_s$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

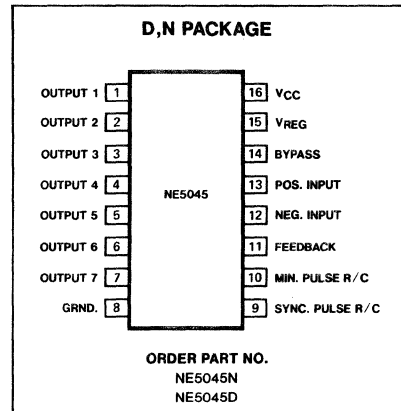
FEATURES

- Decodes up to 7 channels
- High gain input amplifier
- Externally set sync. pause and minimum pulse
- Wide supply voltage range, 3.6V-8V.
- Positive or negative pulse inputs
- Noise and flutter rejection
- Outputs reset to zero without inputs
- Compatible with all transmission mediums

APPLICATIONS

- Radio controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote Analog/digital data transmission
- Automotive sensor systems

PIN CONFIGURATION

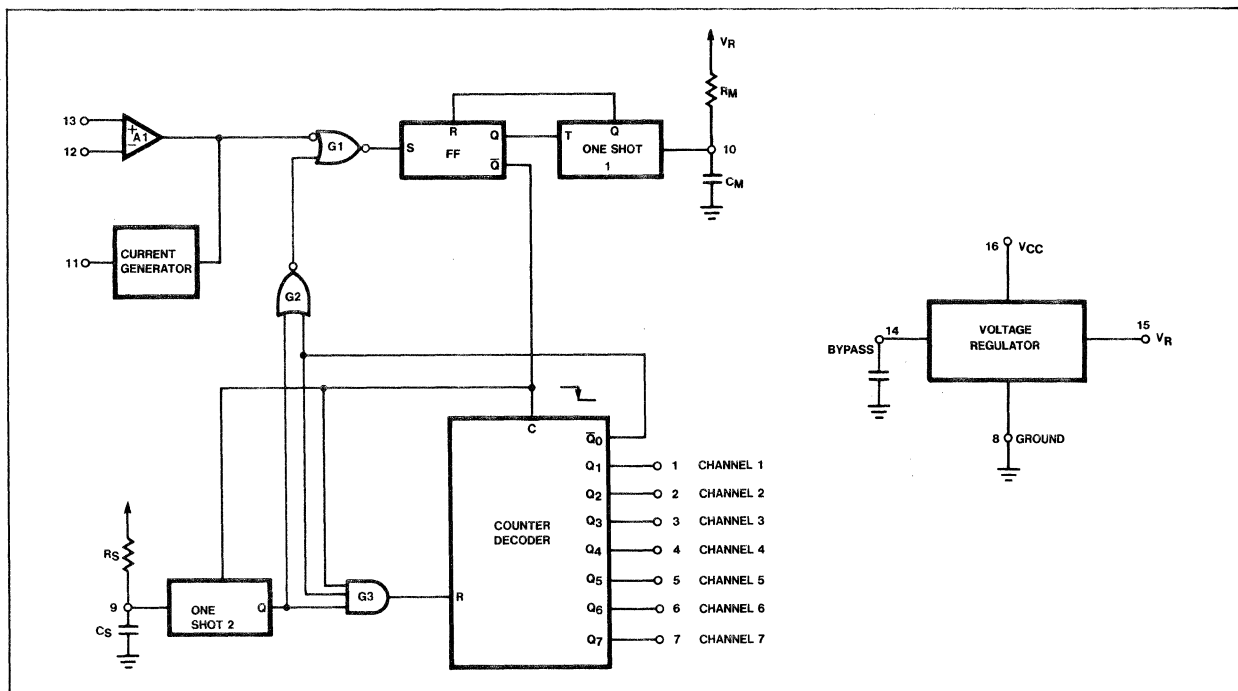


ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
V _{CC} , Supply voltage	10	V
Regulator output current	-25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V _R	V
Input amplifier voltage	0 to V _R	V
Operating temperature	-20 to +75	°C
Storage temperature	-65 to +150	°C

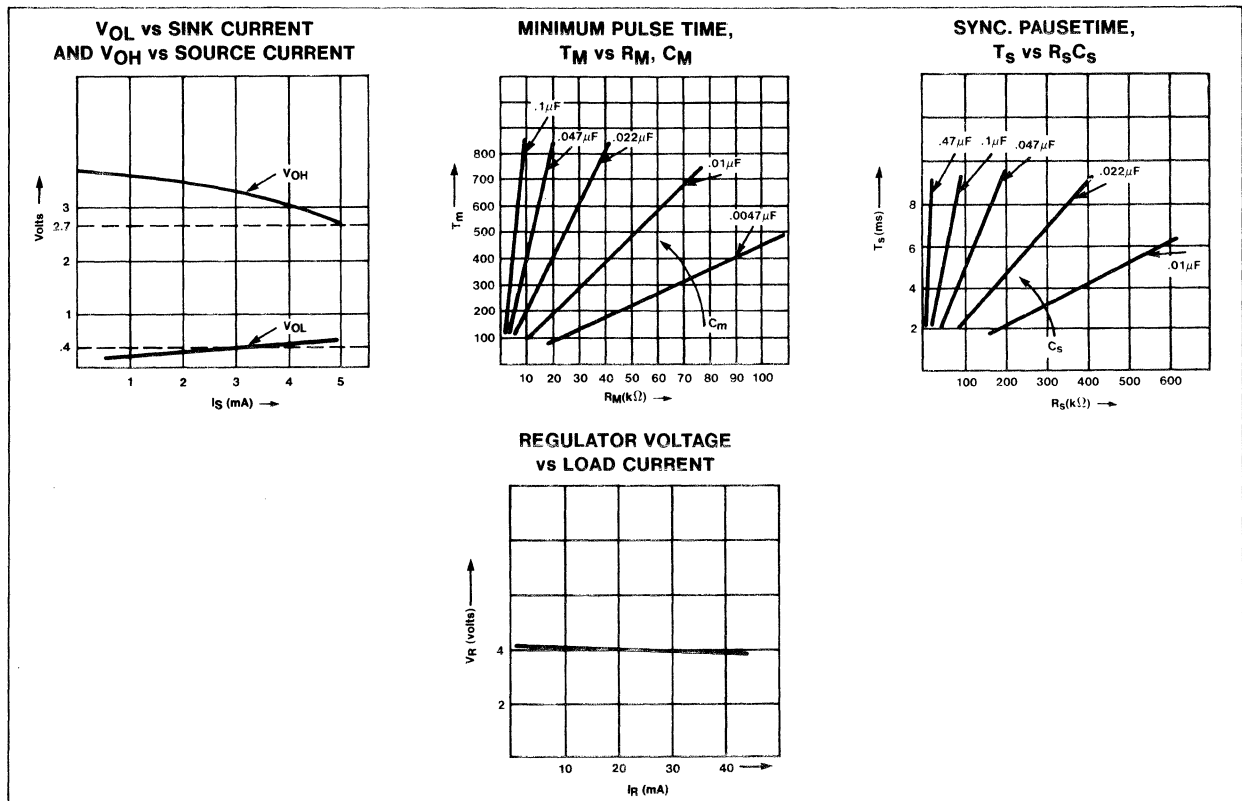
NOTE
1. T_A = 25°C unless otherwise stated

BLOCK DIAGRAM

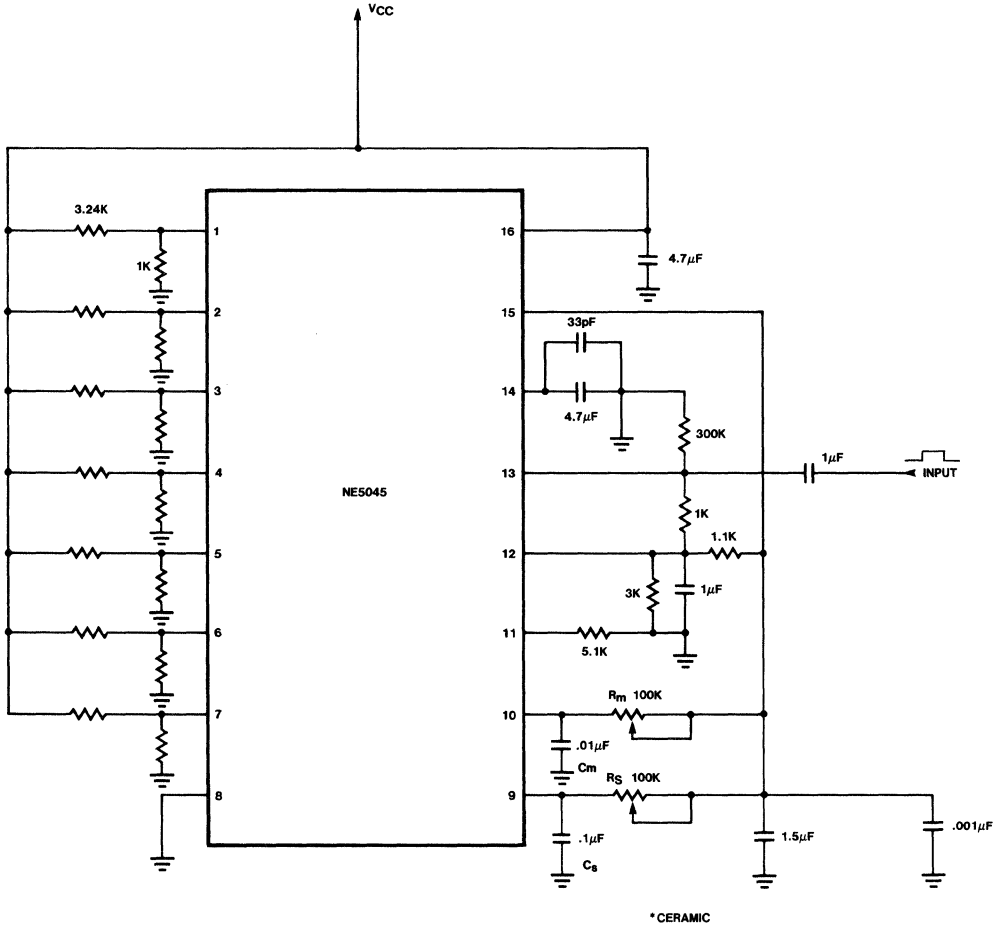


DC ELECTRICAL CHARACTERISTICS Standard conditions: ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$ unless otherwise stated), using Test Circuit # 1

PARAMETER	TEST CONDITIONS	NE5045			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS Power supply voltage range Power supply current	Test circuit # 1 Excluding input bias current	3.6	9.0	8.0 14.0	V mA
V_R VOLTAGE REGULATOR Output voltage Output current Line regulation Voltage drop	$V_R \geq 3.7\text{V}$ $V_{CC} = 6\text{V to } 8\text{V}$ $V_{CC} = 4\text{V}$, $I_R = -10\text{mA}$	3.7	4.1	4.5 -15 .01 .05 1.3	V mA V/V V
T_S T_M INPUT AMPLIFIER Input bias current Input voltage range Open loop gain Feedback current Detection threshold Sync. pause time Minimum pulse time	Test circuit # 1, $\Delta V_{12 \& 13}$ $R_S C_S = 6.0\text{ms}$ $R_M C_M = 500\mu\text{s}$	2.0	10 60	100 4.0	nA V dB μA mV ms μs
OUTPUTS-ALL CHANNELS V _{OL} V _{OH}	$I_{\text{SINK}} = 1\text{mA}$ $I_{\text{SOURCE}} = 2\text{mA}$	2.7	.25	.5	V V



TEST CIRCUIT #1



DESCRIPTION

The NE5046 is a serial input parallel output decoder designed for 2 channel digital proportional pulse width or pulse position modulation systems. The detection threshold is internally set and has hysteresis to prevent false triggering on noise. In a typical application, the serial input from the receiver is processed through an amplifier and pulse shaper, then converted to parallel output with a shift register. An internal sync separator detects the sync pause and clears the shift register. An internal voltage regulator provides power for the decoder and can be used to supply power for a radio receiver.

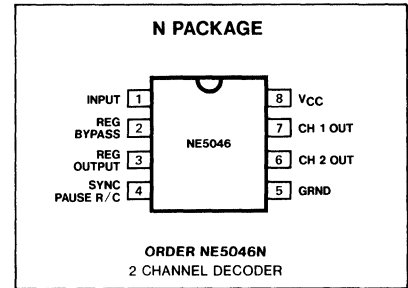
FEATURES

- High gain input amplifier with hysteresis
- Externally adjustable sync separator
- Wide supply voltage range 3.6V-8V
- Noise and flutter rejection
- Outputs reset to zero without input
- Compatible with all transmission mediums

APPLICATIONS

- Radio-controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote-controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote Analog/digital data transmission
- Automotive sensor systems

PIN CONFIGURATION

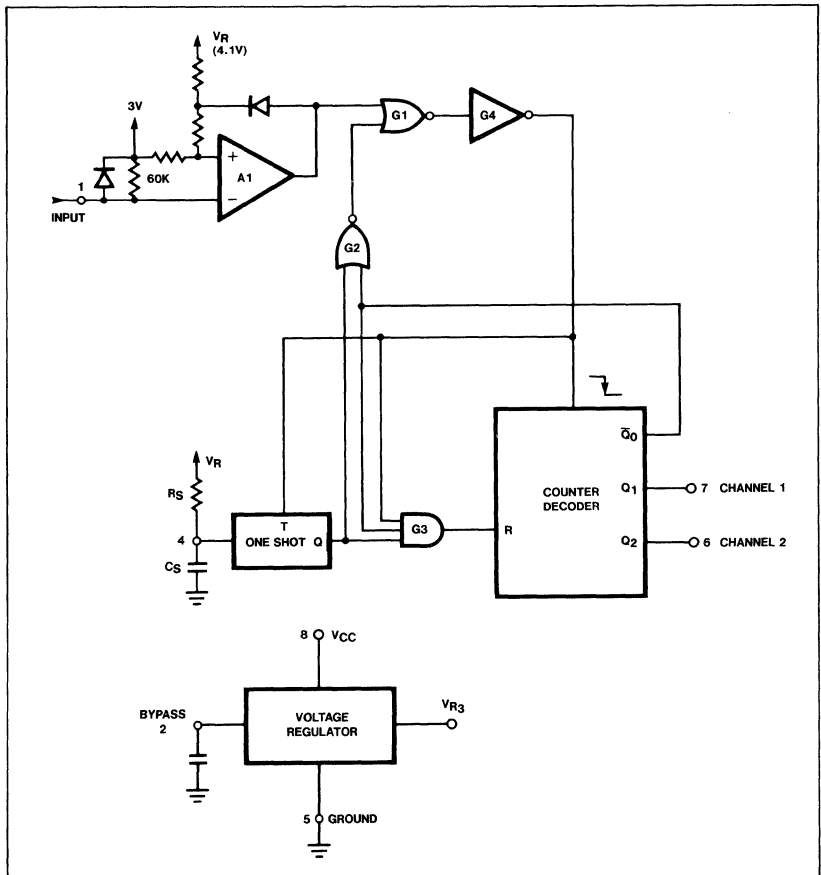


ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
V _{CC} , Supply voltage	10	V
Regulator output current	-25	mA
Decoded output current	±5	mA
Sync pause input	0 to V _R	V
Input amplifier voltage	0 to V _R	V
Input amplifier current	±1	mA
Operating temperature	-20 to +75	°C
Storage temperature	-65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated.

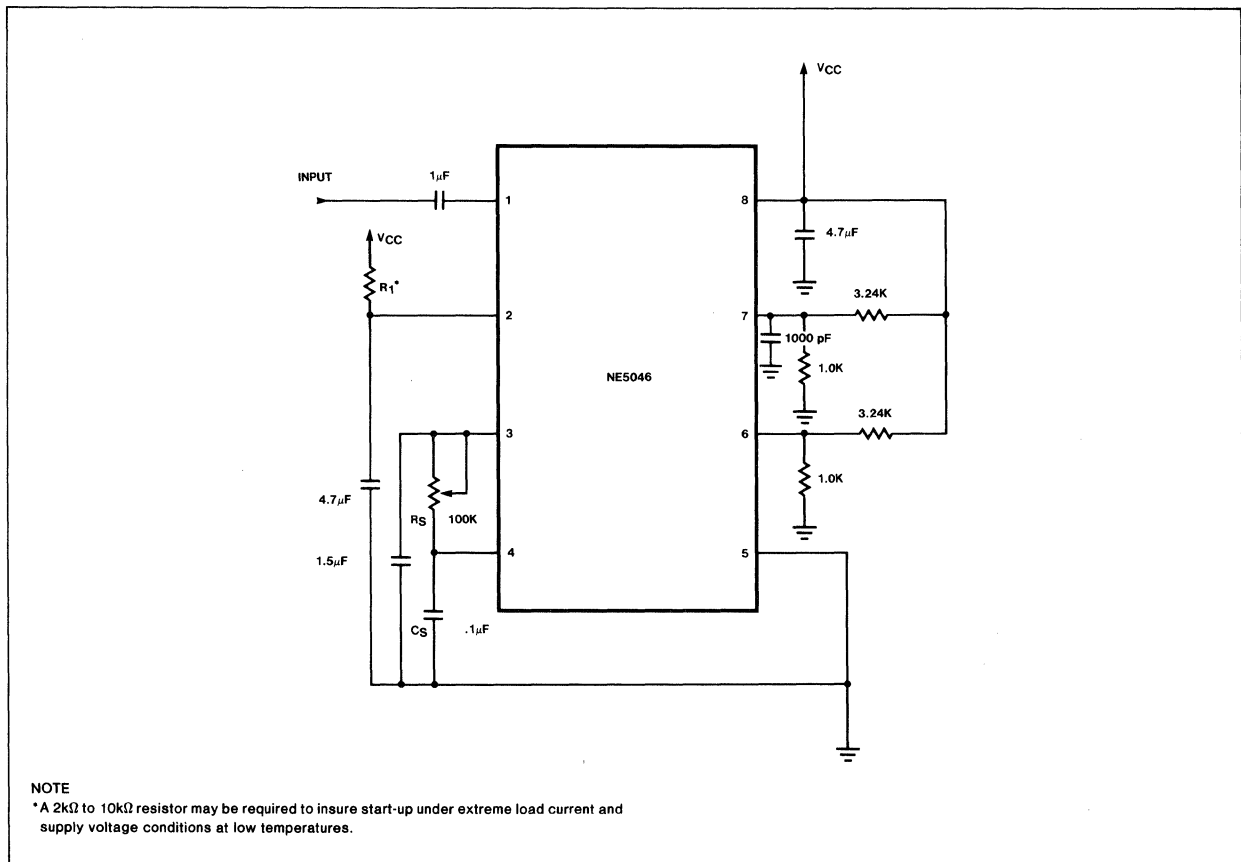
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS Test Conditions: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, Test Circuit 1, unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE5046			UNIT
		Min	Typ	Max	
V_{CC} supply voltage		3.6	5.0	8.0	V
Power supply current			6.0	9.0	mA
Regulator output voltage		3.0	4.1	4.5	V
Regulator output current	$V_R \geq 3.6\text{V}$			-15	mA
Regulator line regulation	$V_{CC} = 6\text{V to } 8\text{V}$.01	.05	V/V
Regulator voltage drop	$V_{CC} = 4\text{V}$, $I_R = -10\text{mA}$			1.0	V
Input threshold voltage		.15			V
Sync. pause time	$R_S C_S = 6\text{ms}$	5.1	6.0	6.9	ms
Output voltage both channels			.25		V
V_{OL}	$I_{SINK} = 1\text{mA}$.5	V
V_{OH}	$I_{SOURCE} = 2\text{mA}$	2.7			V

TEST CIRCUITS



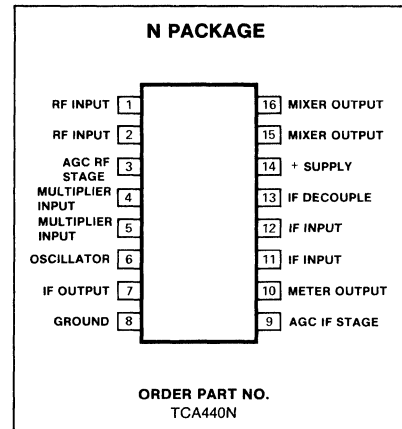
DESCRIPTION

TCA440 is a monolithic IC, especially developed for AM receivers up to 30MHz. It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

FEATURES

- **Balanced circuit**
- **Separately controllable prestage**
- **Multiplicative push-pull mixer with separate oscillator**
- **High signal handling capability even with 4.5V supply voltage**
- **100dB feedback control range in 5 stages**
- **Direct connection for tuning meter**
- **Minimum external components**

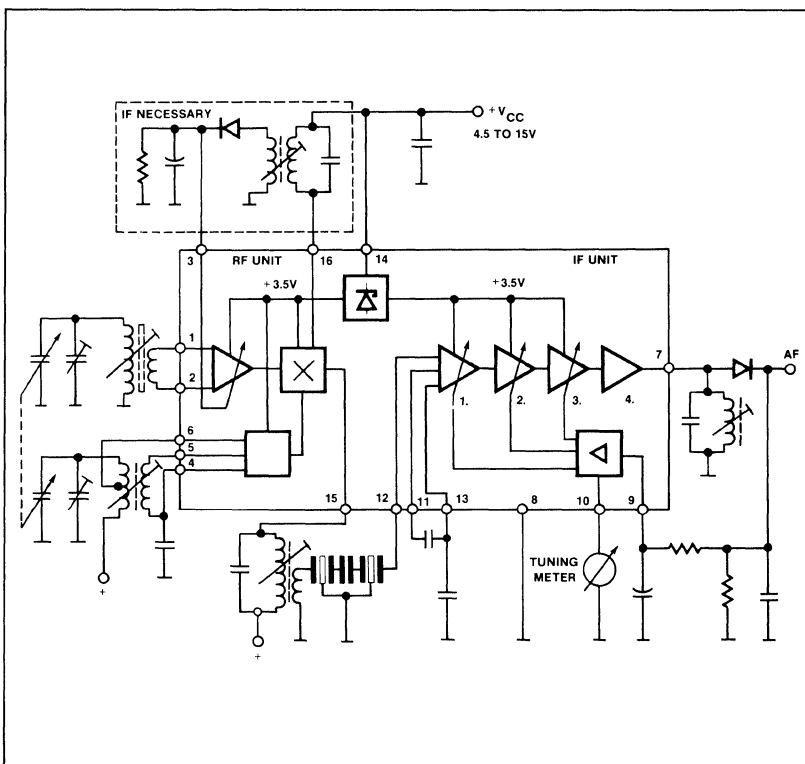
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	15
T _{amb}	Ambient temperature in operation	-15 to +80
T _s	Storage temperature	-30 to +125
V _{CC}	Range of operation	4.5 to 15

BLOCK DIAGRAM



TUNING METER

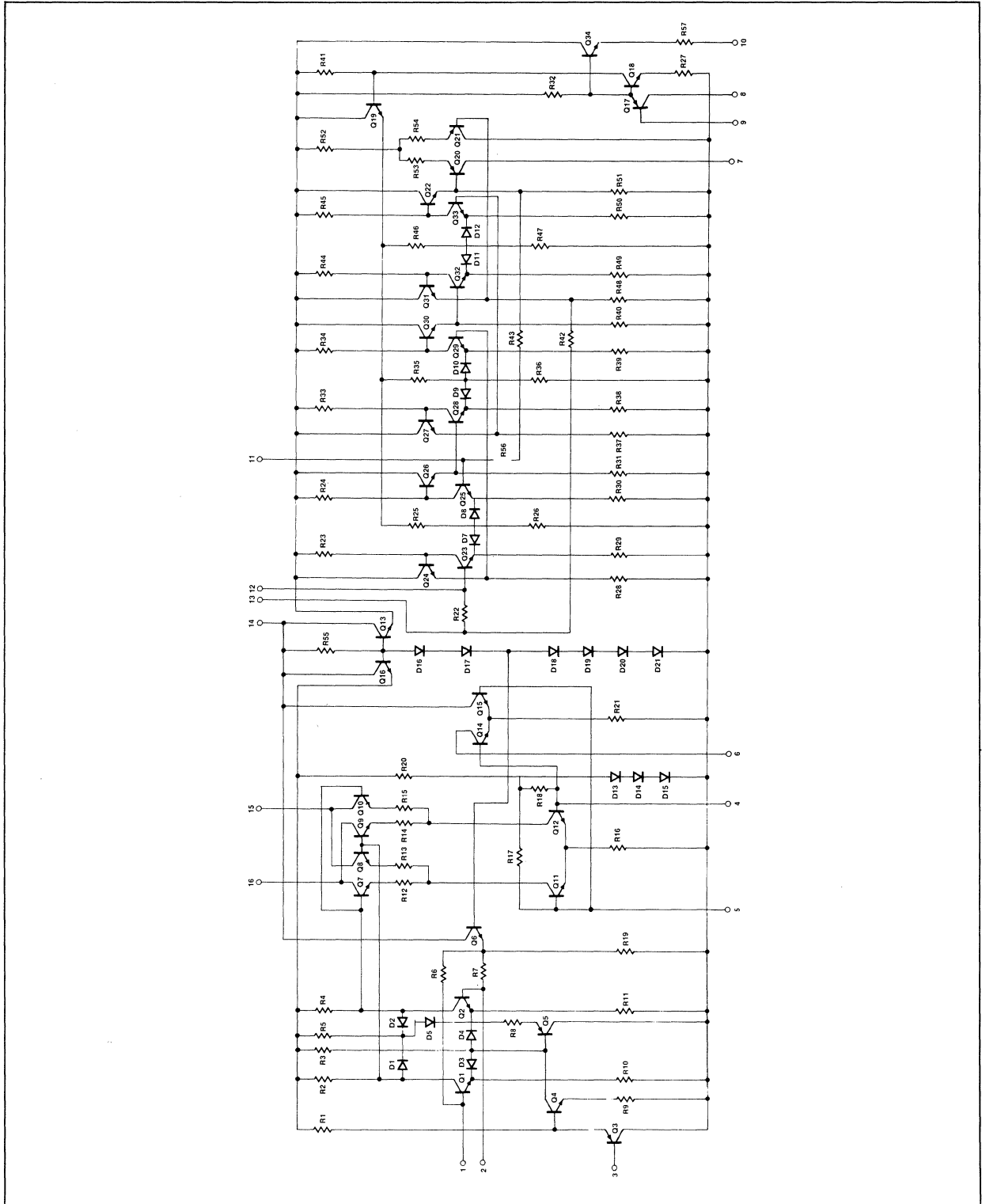
Recommended instruments:
 or 500μA (R₁ = 800Ω)
 300μA (R₁ = 1.5kΩ)

The IC offers at pin 10 a tuning meter voltage of 600 mV_{EMP} max. with a source impedance of approx. 400Ω.

FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of 2.6V_{PP} on the IC input can be handled with very low distortion. The push-pull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100dB. The bridge circuit of the mixer provides good isolation of the oscillator.

EQUIVALENT SCHEMATIC



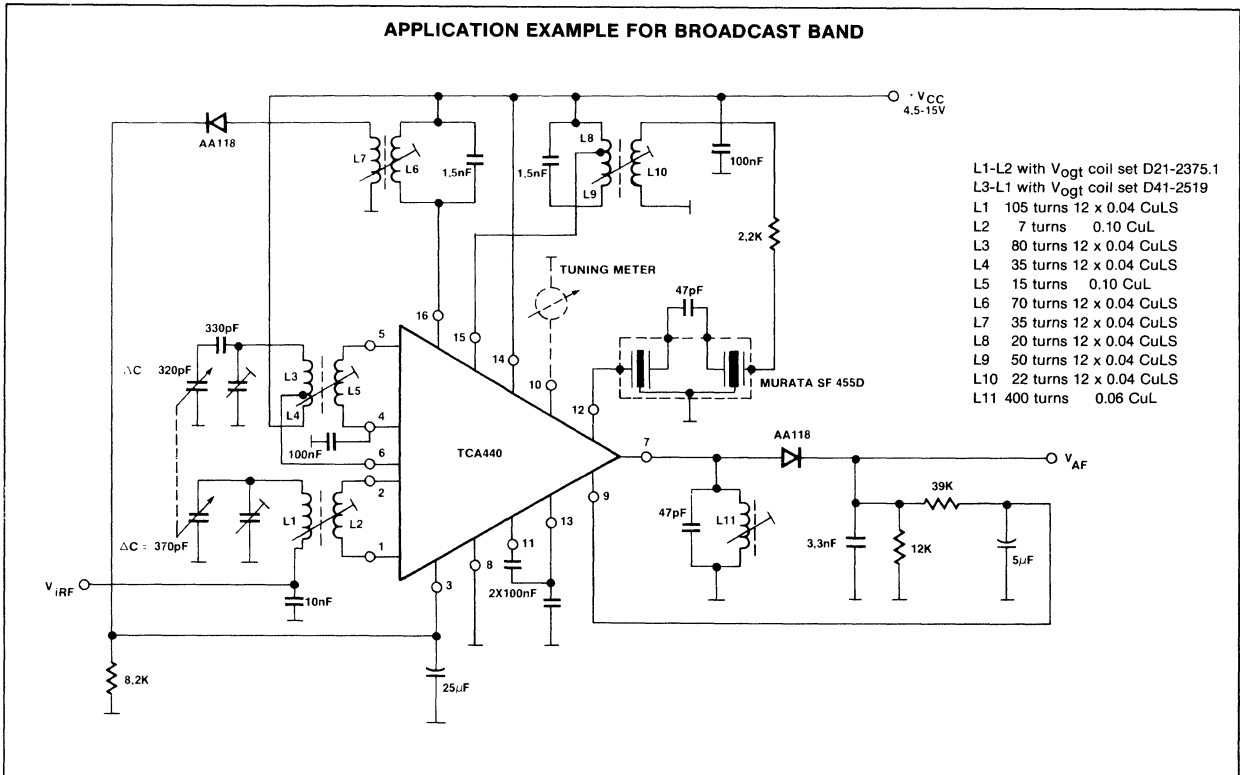
DC ELECTRICAL CHARACTERISTICS $V_{CC} = 9V, T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	TCA 440			UNIT
		Min	Typ	Max	
I_{CC}	Total current consumption at:	$V_{CC} = 4.5V$	7		mA
		$V_{CC} = 9V$	10.5		mA
		$V_{CC} = 15V$	12		mA

AC ELECTRICAL TEST $V_{CC} = 9V, T_A = 25^\circ C, f_c = 1MHz, f_{MOD} = 1kHz$ unless otherwise specified.

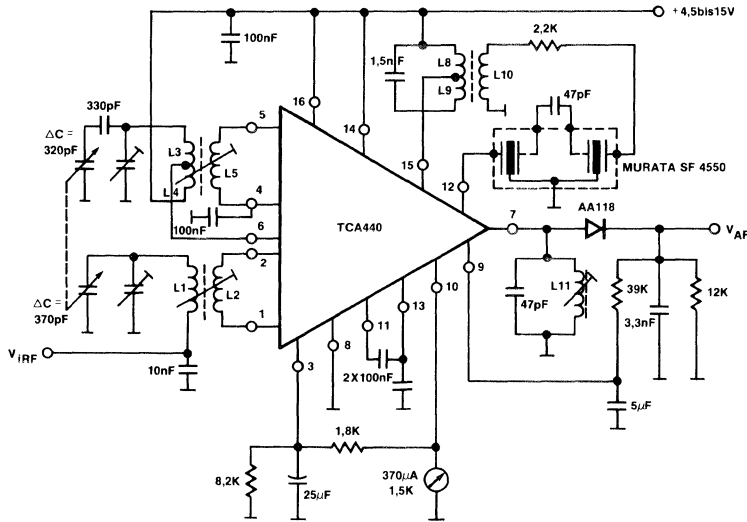
PARAMETER	TEST CONDITIONS	TCA 440			UNIT
		Min	Typ	Max	
V_O	Audio output voltage		100		mV
SEN	Input sensitivity ($f_c = 1MHz, m = 30\%/0\%, R_G = 540\Omega$)		10		μV
	Noise		1.5		mV
M_O	Meter Output		150		μV

TYPICAL APPLICATIONS



TYPICAL APPLICATIONS (Cont'd)

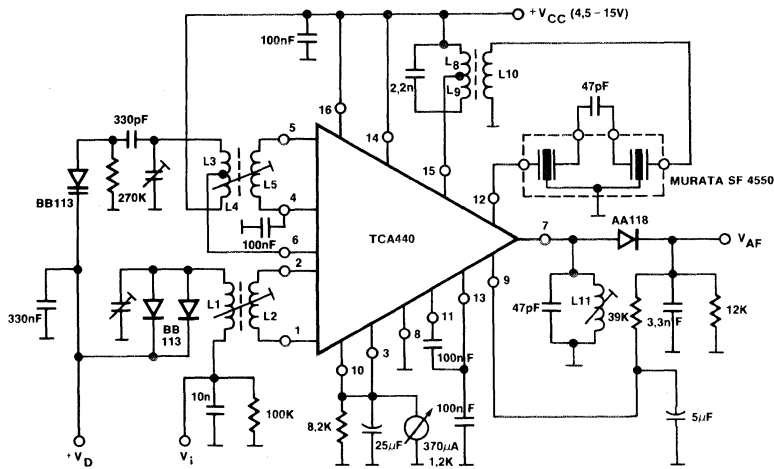
APPLICATION EXAMPLE FOR BROADCAST BAND



Prestage control is derived from IF control

- L1 105 turns 12 x 0.04 CuLS
- L2 7 turns 0.10 CuL
- L3 80 turns 12 x 0.04 CuLS
- L4 35 turns 12 x 0.04 CuLS
- L5 15 turns 0.10 CuL
- L8 20 turns 12 x 0.04 CuLS
- L9 50 turns 12 x 0.04 CuLS
- L10 22 turns 12 x 0.04 CuLS
- L11 400 turns 0.04 CuL
- L1-L2 with Vogt coil set D21-23751
- L3-L11 with Vogt coil set D41-2519

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113



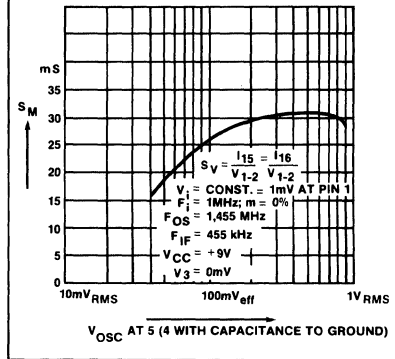
- L1 105 turns 12 x 0.04 CuLS
- L2 7 turns 0.10 CuL
- L3 80 turns 12 x 0.04 CuLS
- L4 35 turns 12 x 0.04 CuLS
- L5 15 turns 0.10 CuL
- L8 20 turns 12 x 0.04 CuLS
- L9 50 turns 12 x 0.04 CuLS
- L10 22 turns 12 x 0.04 CuLS
- L11 400 turns 0.06 CuL

L1-L2 with Vogt coil set D21-23751
L3-L11 with Vogt coil set D41-2519

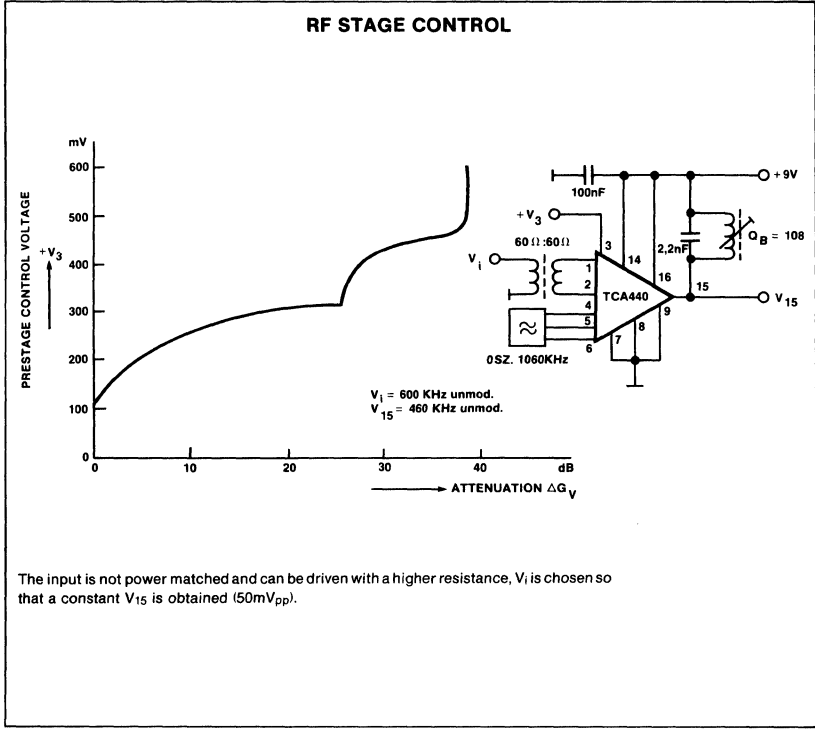
$V_D = 8.5V \rightarrow f_i = 800kHz$
 $V_D = 30V \rightarrow f_i = 1620kHz$

TYPICAL APPLICATIONS (Cont'd)

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE

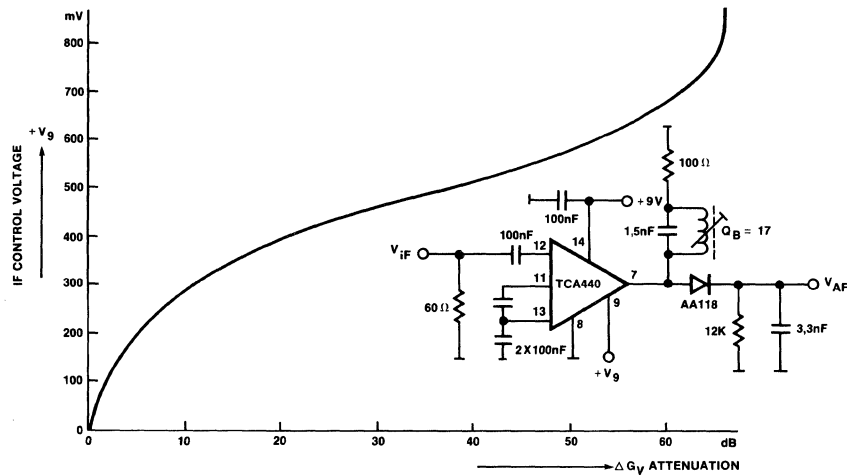


RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, V_1 is chosen so that a constant V_{15} is obtained (50mV_{pp}).

IF CONTROL

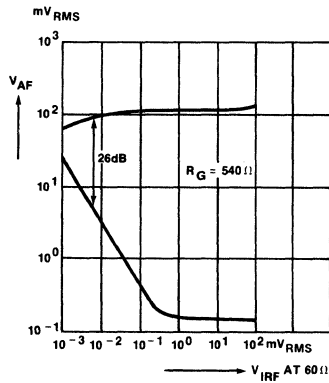


V_{IF} (469kHz; $m = 80\%$; $f_{mod} = 1\text{kHz}$) is chosen so that always a constant V_{AF} is obtained (200mV_{RMS})

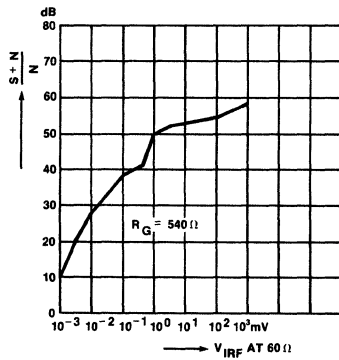


TYPICAL PERFORMANCE CHARACTERISTICS

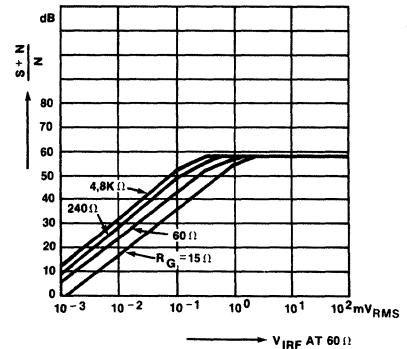
AF OUTPUT VOLTAGE AND NOISE FIGURE vs RF INPUT VOLTAGE (switching position 1)



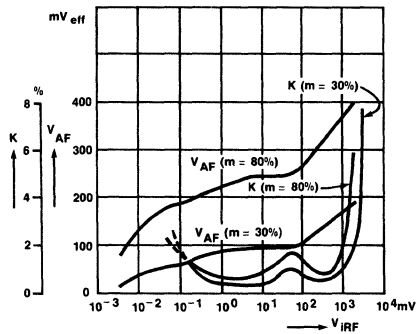
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE (switching position 2)



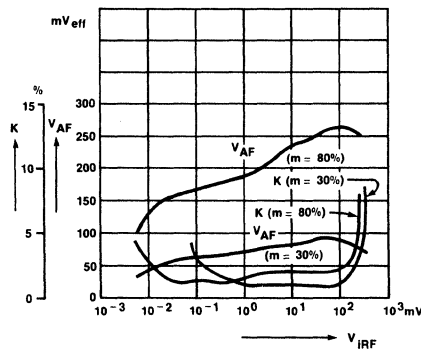
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE (parameter is generator impedance) (switching position 1)



TEST FIGURES FOR APPLICATION EXAMPLE FOR MW HARMONIC DISTORTION AND AF OUTPUT VOLTAGE vs RF INPUT VOLTAGE MEASURED SYMMETRICALLY AT PINS 1 AND 2 $f_i = 1\text{MHz}$, $f_{\text{mod}} = 1\text{kHz}$, $f_{\text{IF}} = 455\text{kHz}$, $V_{\text{CC}} = 9\text{V}$



TEST FIGURES FOR APPLICATION EXAMPLE FOR AM USING BB 113 $f_i = 1\text{MHz}$, $f_{\text{mod}} = 1\text{kHz}$, $f_{\text{IF}} = 455\text{kHz}$, $V_{\text{CC}} = 9\text{V}$, V_{IRF} measured symmetrically at pins 1 and 2

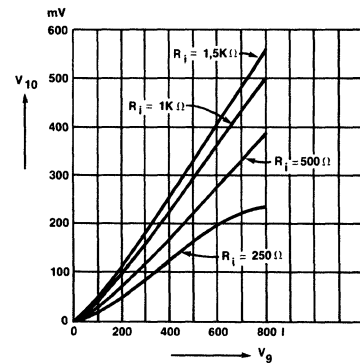


Example for moving coil instruments

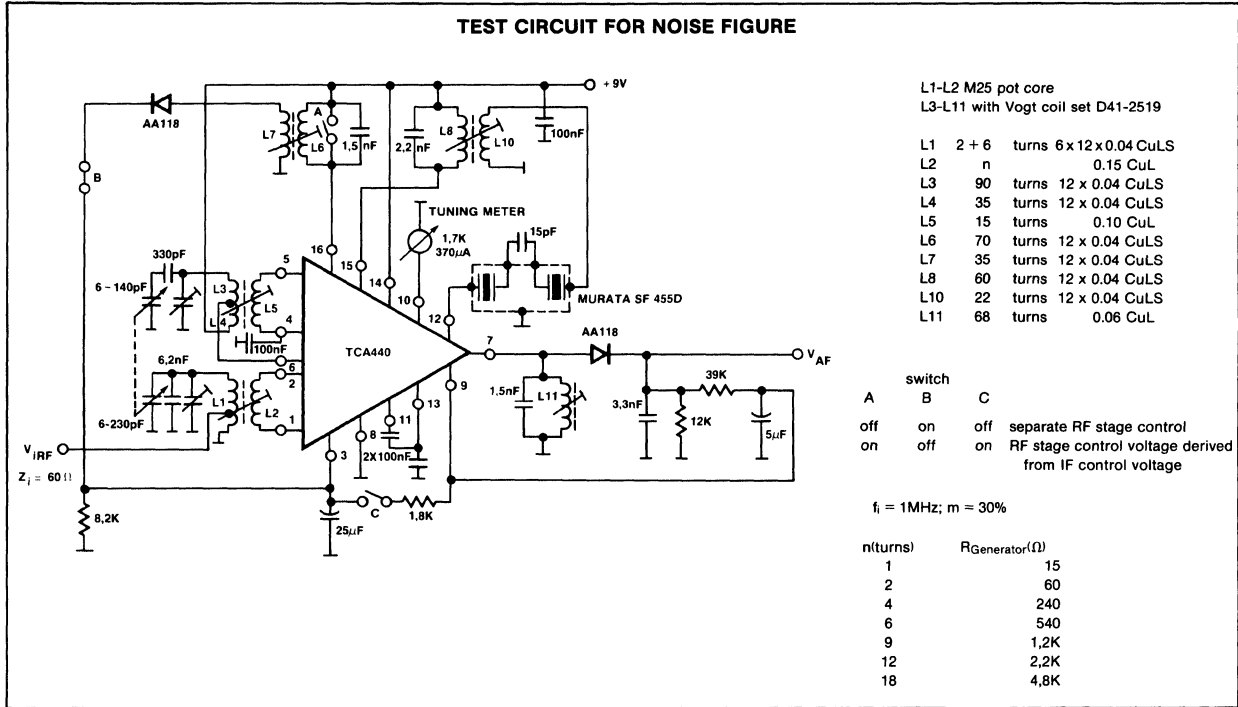
R_i for full-scale deflection

1.5k Ω	100 μA
1.5k Ω	170 μA
2k Ω	200 μA
350 Ω	500 μA

TUNING METER VOLTAGE vs IF CONTROL VOLTAGE (parameter is impedance of tuning meter)



TEST CIRCUITS



DESCRIPTION

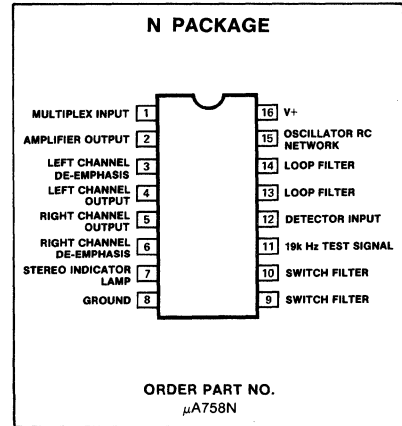
The μA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

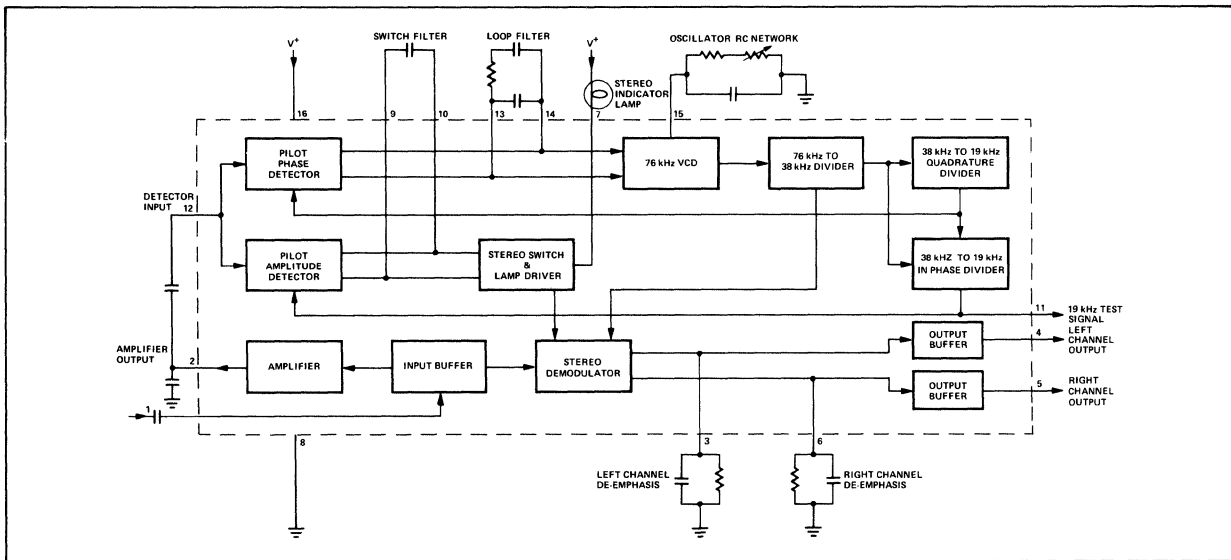
FEATURES

- 45dB channel separation
- Automatic stereo/mono switching
- 70dB SCA rejection
- 10V to 16V supply range
- High impedance input—low impedance output

PIN CONFIGURATION



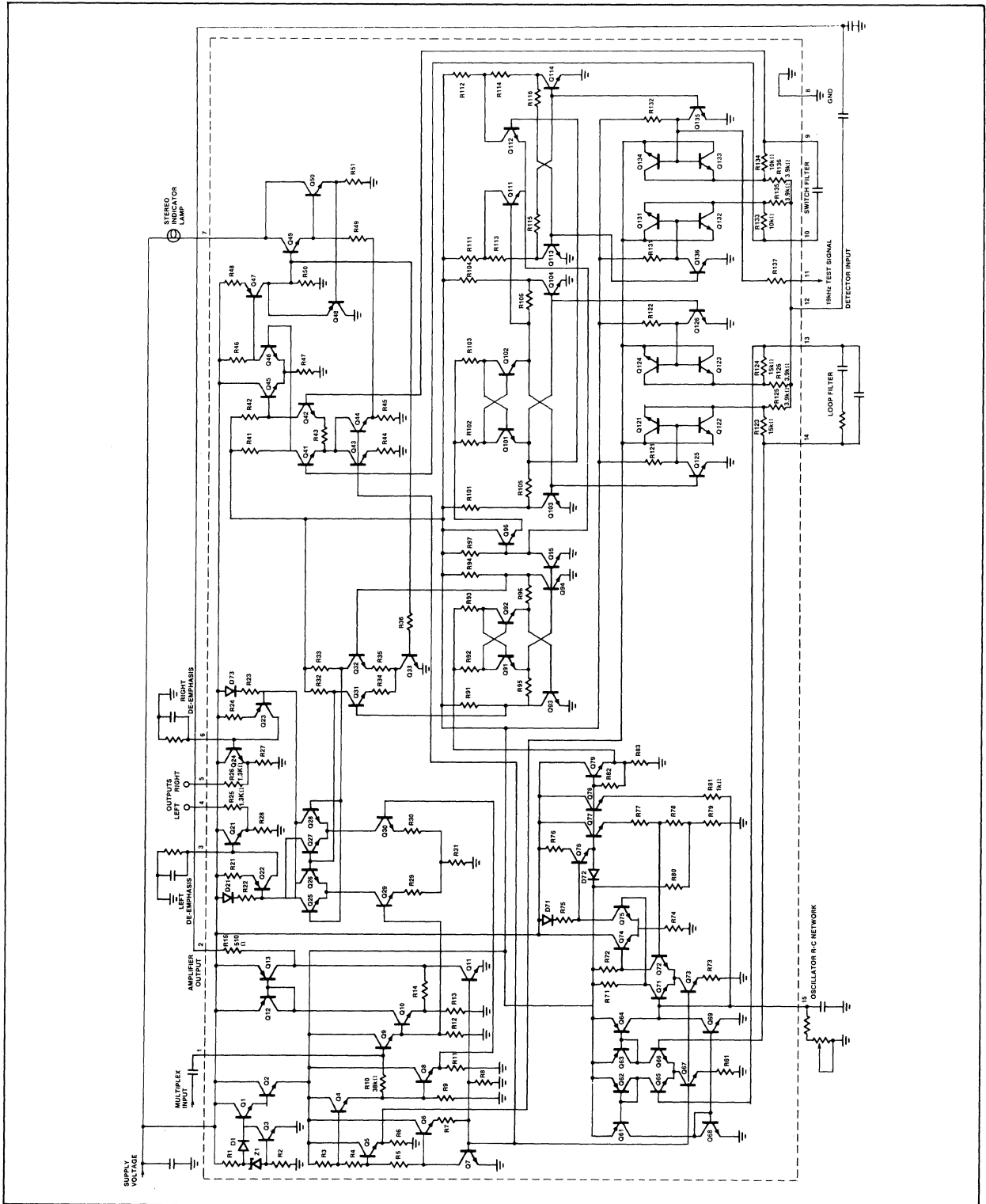
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+18	V
Supply voltage (≤ 15 seconds)	+22	V
Voltage at lamp driver terminal (Lamp OFF)	+22	V
Internal power dissipation	730	mW
Operating temperature range	-40 to +85	°C
Storage temperature range	-55 to +125	°C
Lead temperature (60sec)	300	°C

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_+ = +12\text{V}$, 19kHz pilot level = 30mV_{RMS}, multiplex signal (L = R, pilot OFF) = 300mV_{RMS}, modulation frequency = 400Hz or 1Hz, test circuit 1, unless otherwise specified.

PARAMETER	TEST CONDITIONS	μA758			UNIT
		Min	Typ	Max	
I_{CC} Supply current	Lamp OFF		31	38	mA
I_L Maximum available lamp current		75	150		mA
V_7 Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
r_i Input resistance		20	35		kΩ
r_o Output resistance		0.9	1.3	2.0	kΩ

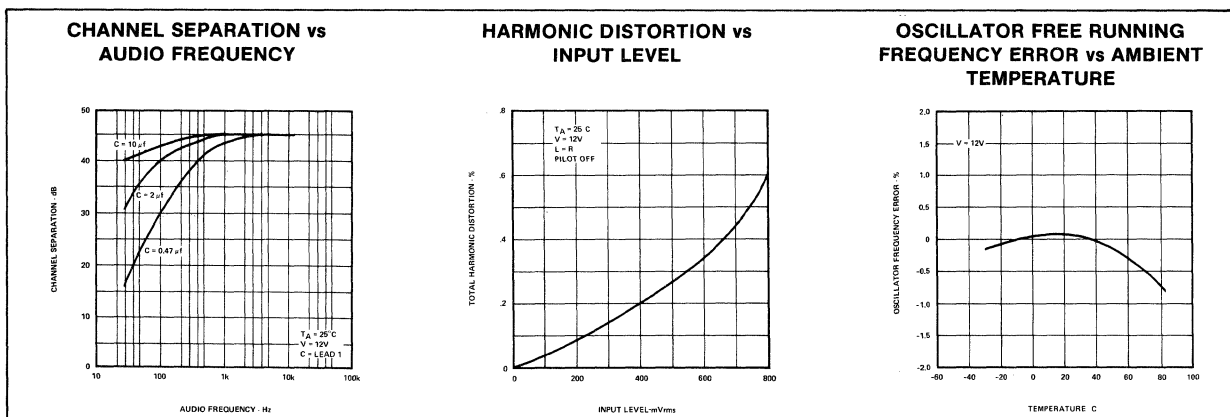
AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	μA758			UNIT
		Min	Typ	Max	
$\Delta(V_4 \& V_5)$ DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
$P_{S,R,R}$ Power supply ripple rejection	200Hz, 200mV _{RMS}	35			dB
SEP Channel separation	100Hz		40		dB
	400Hz	30	45		dB
	10kHz		45		dB
BAL. Channel balance			0.3	1.5	dB
A_v Voltage gain	1kHz	0.5	0.9	1.4	V/V
Pilot input level	Lamp turn-on		18	25	mV _{RMS}
	Lamp turn-off	2.0	7.0		mV _{RMS}
Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
T.H.D. Capture range		2.0	4.0	6.0	%
T.H.D. Total harmonic distortion	Multiplex level = 600mV _{RMS} pilot OFF		0.4	1.0	%
	19kHz rejection	25	35		dB
	38kHz rejection	25	45		dB
	SCA rejection ¹		70		dB
VCO Tuning resistance ²		21.0	23.3	25.5	kΩ
VCO Frequency drift	$0^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		+0.1	±2	%
	$25^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		-0.4	±2	%

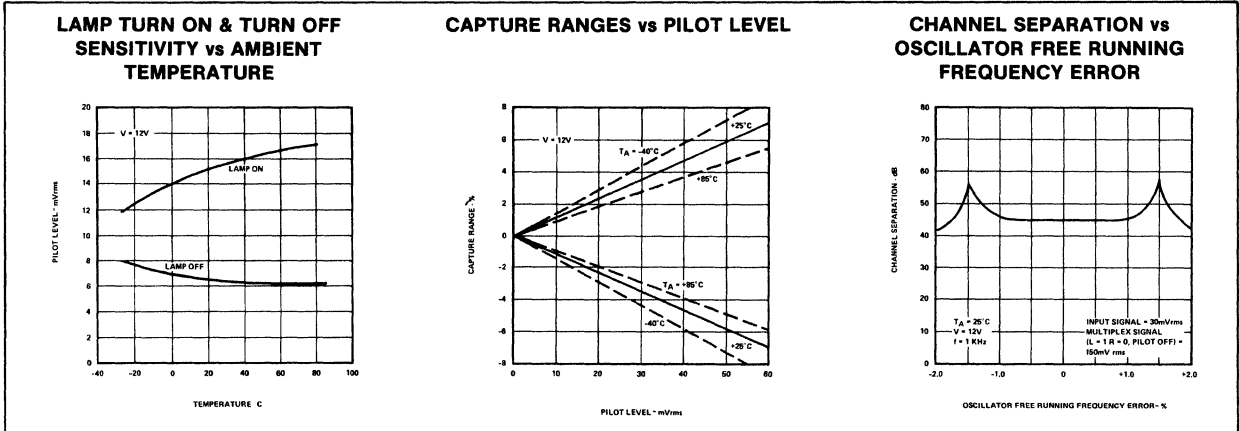
NOTES

1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to 19kHz ± 10hz.

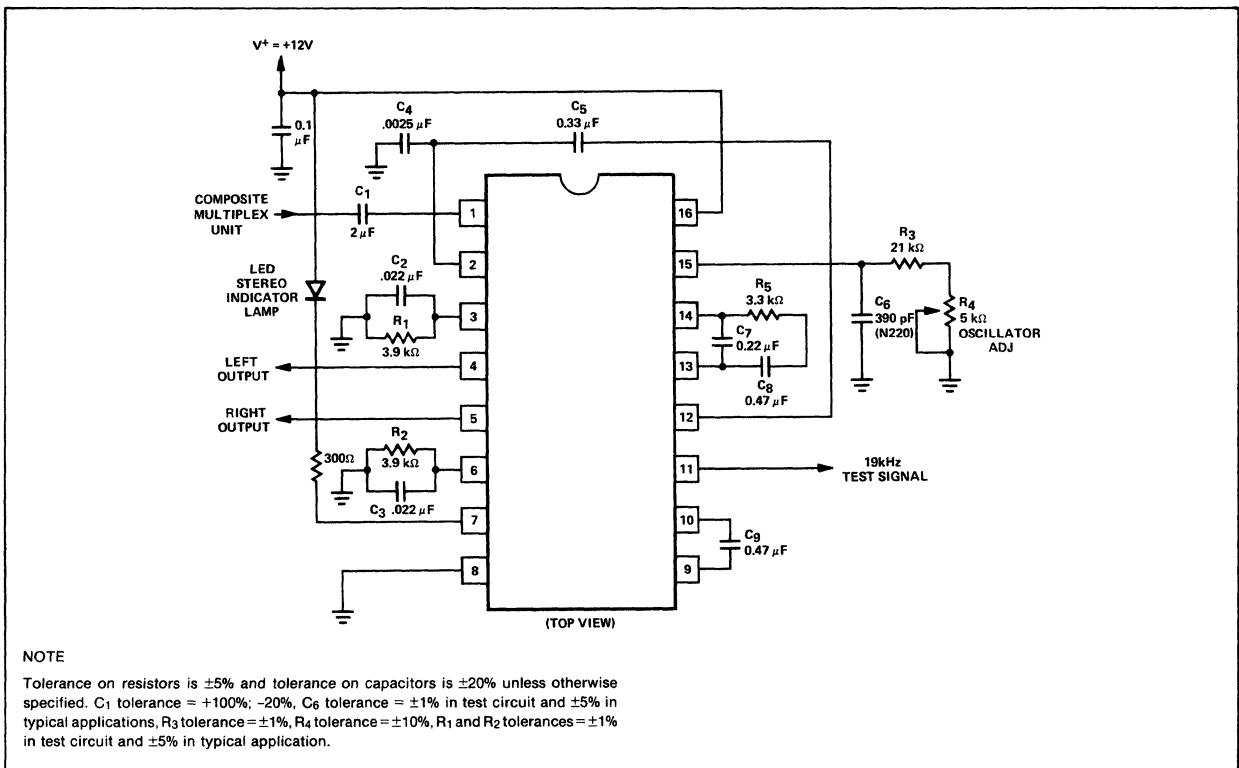
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TEST CIRCUIT AND TYPICAL APPLICATION



SECTION 12

TV CIRCUITS

Section 12—TV CIRCUITS

LM1880	Vertical/Horizontal Processor	395
TBA120S	8-Stage Amplifier with Balanced Demodulator	398
TBA1440G/1441G	TV Video Amplifier with Demodulator	401
ULN2211	2-Watt TV/FM Sound Channel	405

DESCRIPTION

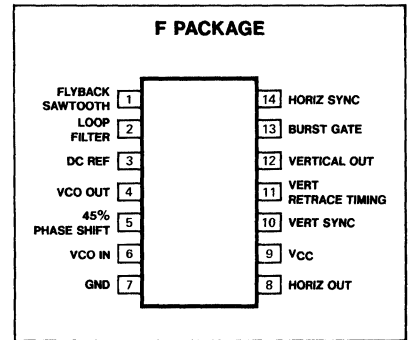
The LM1880 uses compatible Linear/1²L technology to produce the first T.V. horizontal and vertical processing system which completely eliminates the hold controls. The heart of the system is a precision 32 times horizontal frequency VCO which is designed to use a low-cost ceramic resonator as a tuning element.

The VCO signal is divided down in the horizontal section to produce a pre-driver output which is locked to negative sync by means of an on-chip phases detector. The vertical output ramp is injection-locked by vertical sync subject to a sync window derived from the vertical countdown section. A gate pulse centered on the chroma burst is also provided.

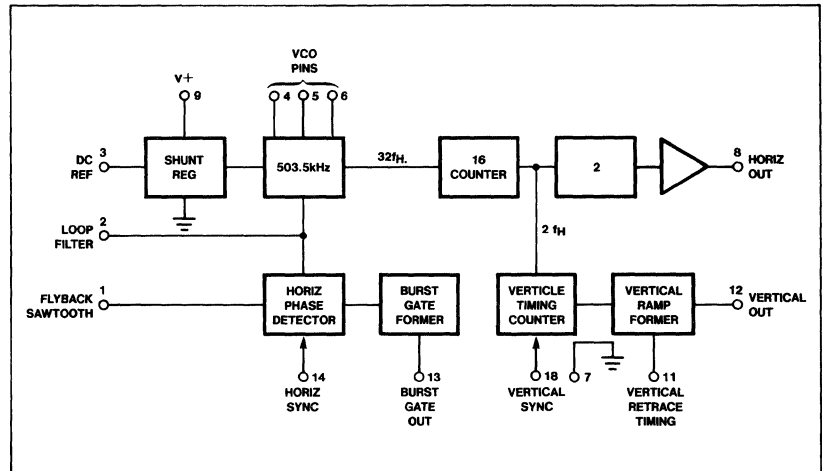
FEATURES

- No frequency set-up required for horizontal or vertical
- Ceramic resonator frequency reference
- Accurate horizontal pre-driver duty cycle
- Vertical sync window referenced to horizontal
- Precise interlaced vertical output
- APC loop parameters completely adjustable
- Vertical retrace time adjustable
- Chroma burst gate output
- Internal voltage regulator

PIN CONFIGURATION

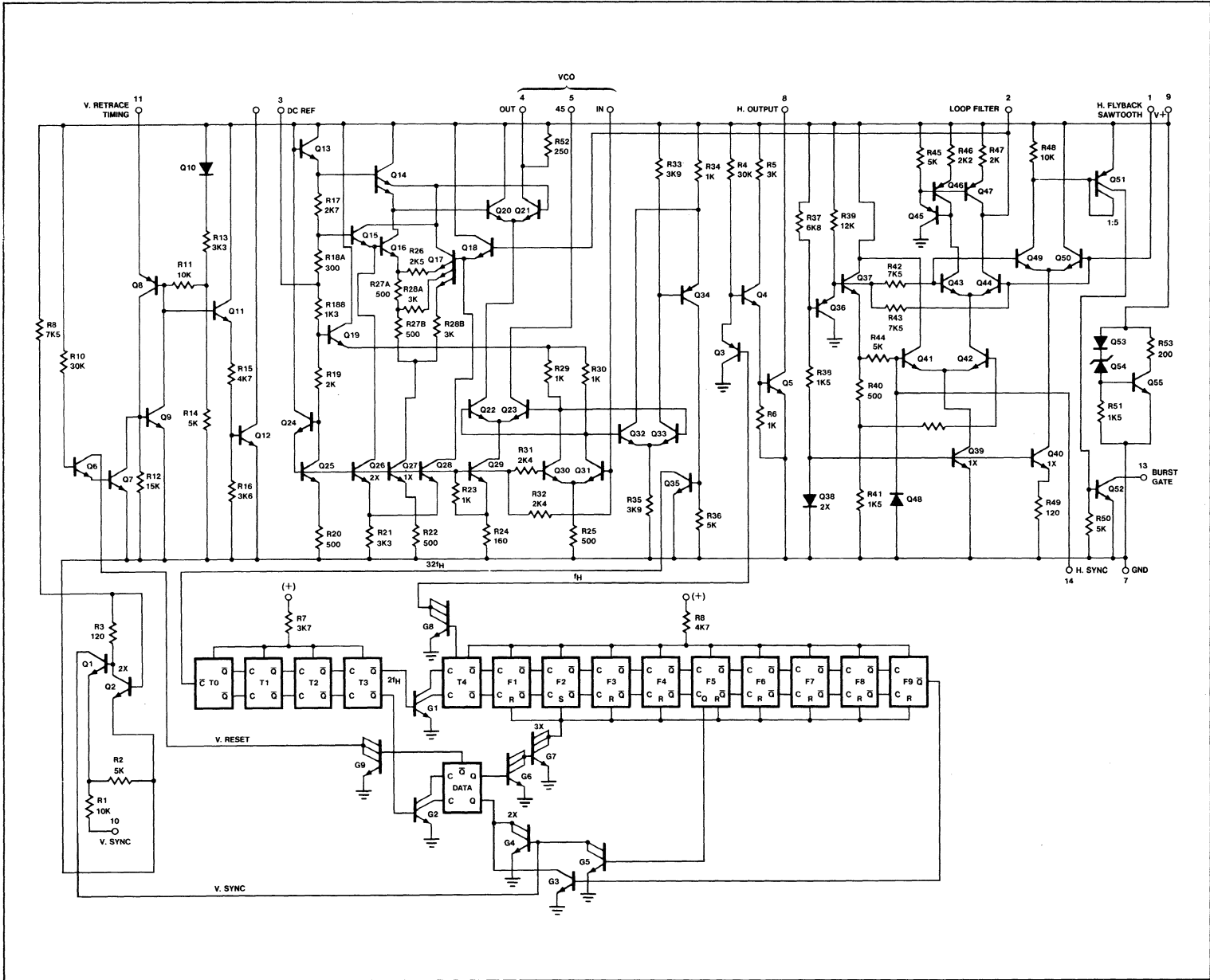


BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Sawtooth input voltage (Pin 1)	5	Vp-p
Package dissipation, T _A = 25°C	0.83	W
Above T _A = 25°C, Derate Based on T _J (MAX) = 150°C and θ _{JA} = 150° C/W		
Storage temperature range	-55°C to 150	°C
Operating temperature range	0°C to +70	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Supply current (Pin 9)	40	mA
Output voltage (Pins 8, 12, 13)	12	V
Output current		
Pin 8	50	mA
Pin 12	15	mA
Pin 13	10	mA
Sync. input voltage (Pins 10, 14)	5	Vp-p



SCHEMATIC DIAGRAM

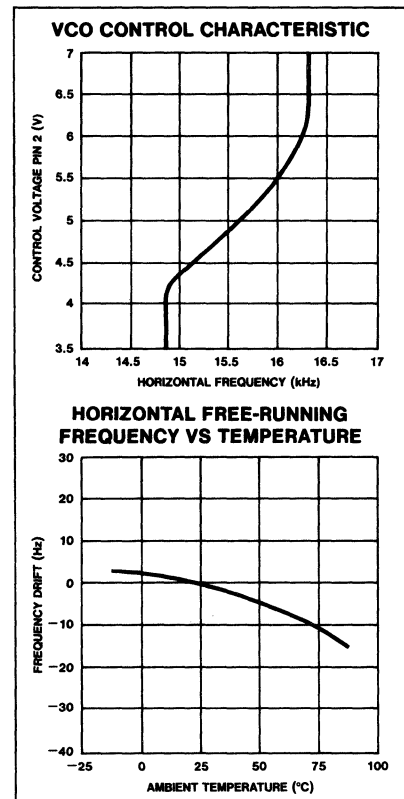
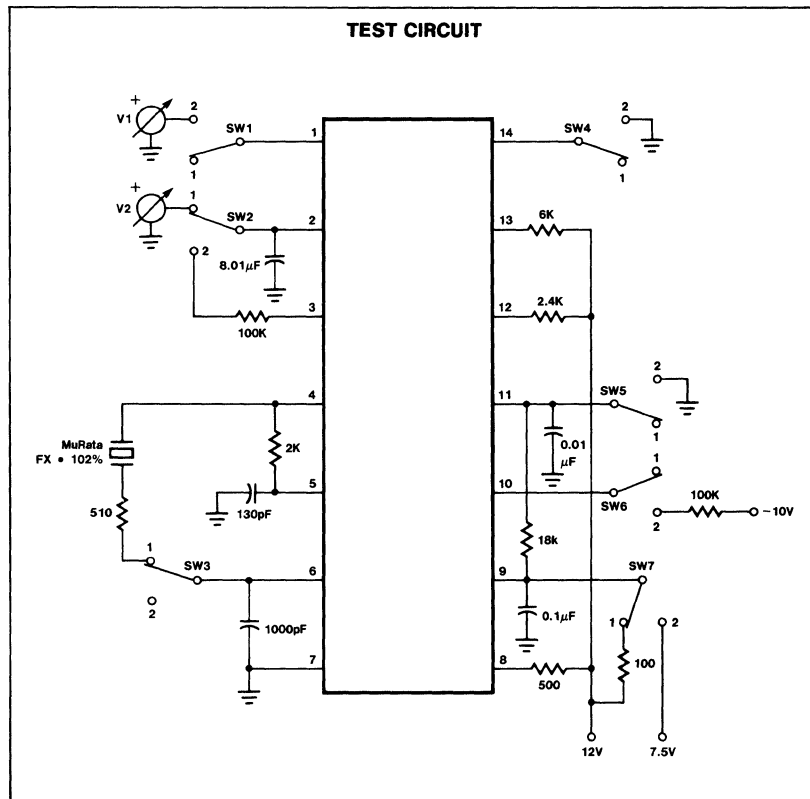
ELECTRICAL CHARACTERISTICS (Test circuit, all SW normally pos. 1, $T_A = 25^\circ\text{C}$)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Regulated voltage (Pin 9)		8.2	8.7	9.2	V
Supply current (Pin 9)	SW 7 Pos. 2	12	18	24	mA
VCO reference voltage (Pin 3)			5.1		V
VCO control current (Pin 2)	$V_2 = 5\text{V}$		0.25	1.0	μA
Horizontal phase detector sink current (Pin 2)	SW 1, SW 4 Pos. 2, $V_1 = 3.9\text{V}$, $V_2 = 5\text{V}$	0.3	0.5		mA
Horizontal phase detector source current (Pin 2)	SW 1, SW 4 Pos. 2, $V_1 = 1.9\text{V}$, $V_2 = 5\text{V}$	0.3	0.5		mA
Horizontal output leakage (Pin 8, OFF Condition)	Change SW 3 to Pos. 2 with Pin 8 High			150	μA
Horizontal output saturation voltage (Pin 8, ON condition)	Change SW 3 to Pos. 2 with Pin 8 Low		0.15	0.4	V
Vertical output saturation voltage (Pin 12)	SW 3, SW 5 Pos. 2		0.25	0.5	V
Burst gate saturation voltage (Pin 13)	SW 1, SW 4 Pos. 2, $V_1 = 1.9\text{V}$		0.15	0.4	V
Horizontal oscillator free-running Frequency (Pin 8) ¹	SW 2 Pos. 2	15,550	15,750	15,950	Hz
Horizontal oscillator maximum frequency (Pin 8)	$V_2 = 7\text{V}$	16,300			Hz
Horizontal oscillator minimum frequency (Pin 8)	$V_2 = 3\text{V}$			15,150	Hz
Vertical minimum lock frequency (Pin 12)	$f_H = 15,734\text{ Hz}$			58.1	Hz
Vertical maximum lock frequency (Pin 12)	SW 6 Pos. 2, $f_H = 15,734\text{ Hz}$	61.7			Hz

NOTE

1. Assumes ceramic resonator $f_R = 503.48\text{kHz}$.

TYPICAL PERFORMANCE CHARACTERISTICS



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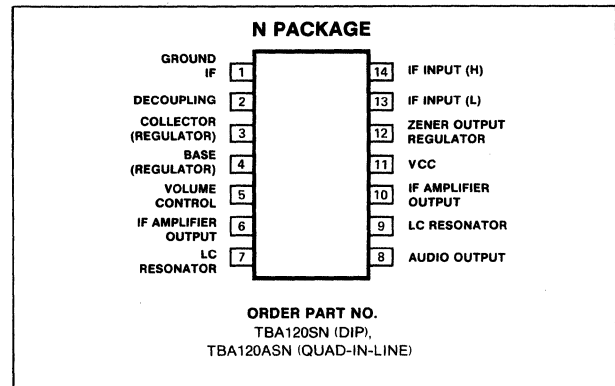
DESCRIPTION

An eight stage amplifier with balanced demodulator for amplifying, limiting and the demodulation of FM signals, specially designed for the sound-IF in TV and RF-IF amplifier in radios. An electronic Volume Control for the audio outputsignal is also provided.

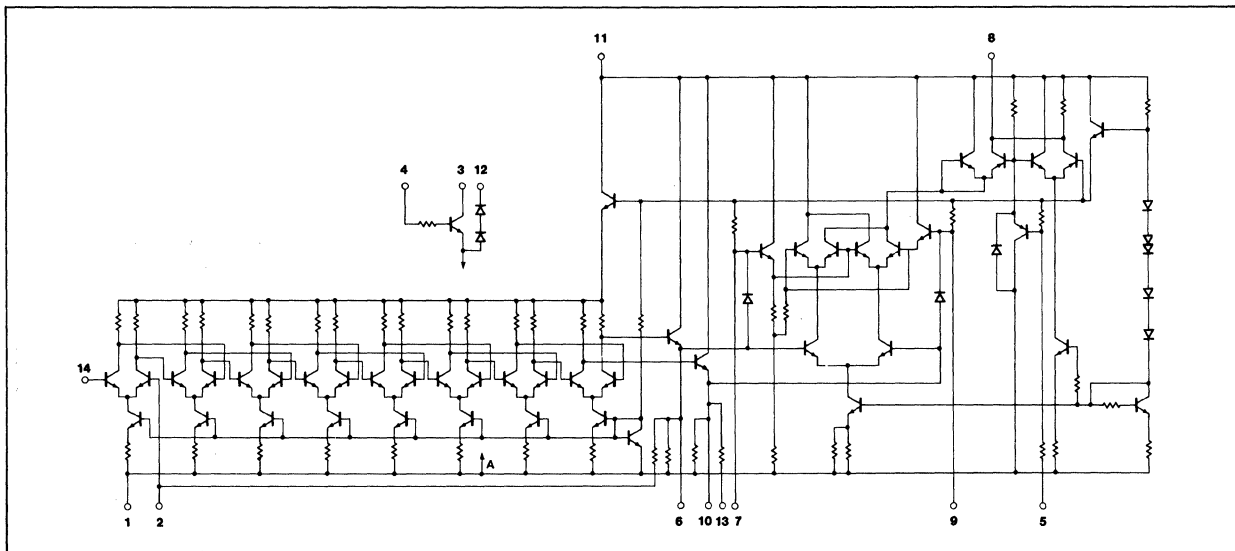
Groups:

TBA120 S is delivered in groups:
An attenuation of -30dB of the audio output signal requires a resistor from pin 5 to ground typ. value 1.8K to 3.4K.

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	18	V
Operating temperature range	-15 to +70	°C
Storage temperature	-40 to +125	°C
Power dissipation	400	mW
max 1 minute	500	mW
Supply current	15	mA
max 1 minute	20	mA
Current 13	1	mA
14	1	mA
Operating supply voltage	6 to 18	V
Frequency range	0 to 12	MHz

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 12V$; $T_{amb} = 25^{\circ}C$)

PARAMETER	TEST CONDITIONS	TBA120S			UNIT
		Min	Typ	Max	
I_{CC} Total current requirement	$R_5 = \infty$ $R_5 = 0$		14	24	mA
			16	26	mA
V_8 dc-portion of the output signal	$V_1 = 0$		8.6		V
V_5 Voltage	-1dB down		2.4		V
	-70dB down		1.3		V

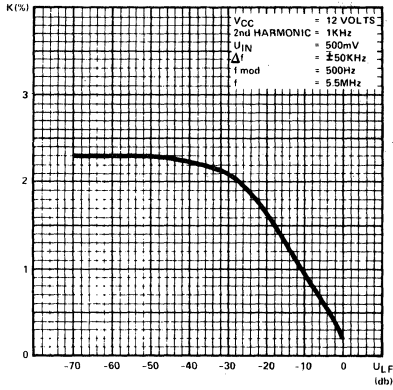
AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$, $V_{CC} = 12V$ unless otherwise specified. $F_C = 4.5$ or $5.5MHz$.

PARAMETER	TEST CONDITIONS	TBA120S			UNIT
		Min	Typ	Max	
A_V IF-voltage gain V_6/V_{14}	$f = 5.5MHz$		68		dB
V_{IF} IF-output voltage at limiting; each output			250		mV
V_O AF-output voltage	$f = 5.5MHz$; $\Delta f = \pm 40kHz$; $V_I = 10mV$; $f_{mod} = 1kHz$; $Q = 45$; $k = 4\%$.50	.9	1.4	V
	$f = 5.5MHz$; $\Delta f = \pm 40kHz$; $V_I = 10mV$; $f_{mod} = 1kHz$; $Q = 20$; $k = 1\%$		500		mV
V_{lim} Input voltage starting limiting	$V_{out} = -3dB$		30	70	μV
Z_I Input impedance	$f = 5.5MHz$		40/4.5		k Ω /pf
R_O Output resistance	Pin 8		2.6		k Ω
VOL Range of volume control			70		dB
AMR AM-rejection	$f = 5.5MHz$ $V_I = 500\mu V$; $f_{mod} = 1kHz$; $MO = 30\%$	40	48		dB
R_5 Potentiometer resistance	-1dB down		3.7	4.7	k Ω
	-70dB down	1.0	1.4		k Ω
CHARACTERISTICS OF THE AUXILIARY CIRCUIT					
V_{12} Z-voltage	$I_{12} = 5mA$	11.2	12	13.2	V
R_Z Z-resistance			30		Ω

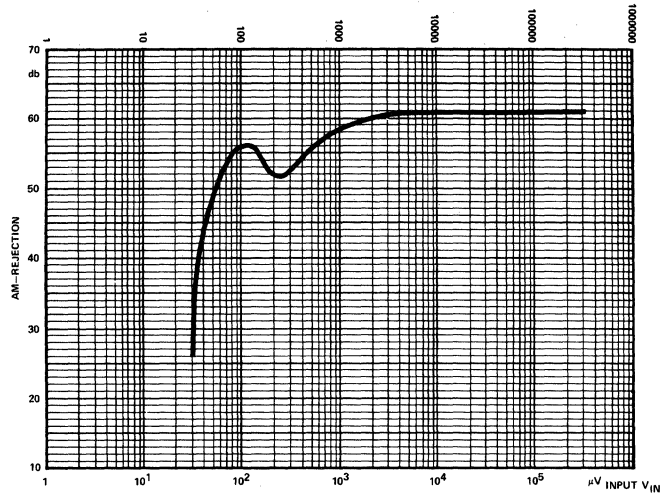


TYPICAL PERFORMANCE CHARACTERISTICS

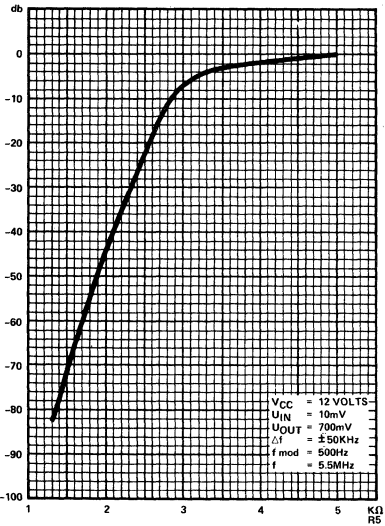
TYPICAL CURVE FROM PRODUCT SELECTION NR3.



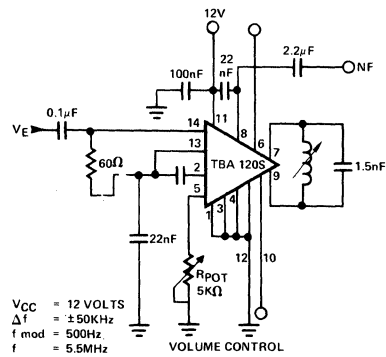
TYPICAL CURVE FROM PRODUCE-REFLECTION NR3.



VOLUME CONTROL SIGNETICS TBA120S



TEST CIRCUIT



DESCRIPTION

The TBA1440G (for pnp tuner pre-stages) and TBA 1441G (for npn tuner pre-stages) have been developed from the TBA440P/N. Their improvements are as follows:

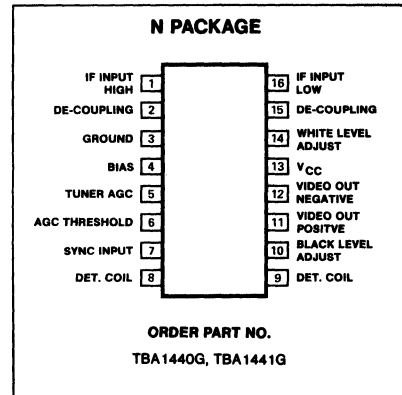
- Reduced residual IF at outputs 11 and 12
- Reduced residual IF at pin 13
- Considerably improved intermodulation distance
- Excellent tuning attitude even with low-ohmic tank circuit at demodulator

The IC's contain a high-amplifying controllable video IF amplifier, a controlled demodulator and two low-resistance video outputs

with positive- and negative-going signals as well as the complete keyed control and delayed tuner control.

- Large control range with low noise and wide dynamic range
- High sensitivity
- Controlled demodulator, so minimum 1.07MHz disturbances
- Internal temperature stabilization
- The white levels of the video signals at the positive and negative video output are independent of the operating voltage
- The white and black levels can be adjusted separately

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V ₁₃ Supply voltage	15*	V
V ₄ Voltages	5	V
V ₅	20	V
V ₁₄	5	V
R ₈₋₉ Ohmic resistance between pins 8 and 9	≤20	Ω
R _{THSA} Thermal resistance (system-air)	100	K/W
T _J Junction temperature	150	°C
T _S Storage temperature	-40 to +125	°C
V ₁₃ Supply voltage range	10.5 to 15	V
T _A Ambient temperature in operation	-25 to +60	°C

NOTE
Briefly 16.5V

DC ELECTRICAL CHARACTERISTICS V₁₃ = 12.4, T_A = 25°C; all data with reference to ground, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TBA1440G/1441			UNIT
		Min	Typ	Max	
I ₁₃ Current consumption	V ₁₃ = 15V	34	47	60	mA
V ₁₁ DC voltage at output 11	V _{IN} = 0		4.5		V
	R ₁₄₋₃ = 68k R ₁₄₋₃ = 0		6.4		V
V ₁₂ DC voltage at output 12	V _{IN} = 0		1.9		V
	R ₁₄₋₃ = 68K R ₁₄₋₃ = 0		3.5		V
V ₆ AGC threshold			2.4		V
V ₄ IF control voltage	For max. gain V _{IN} = 0			.5	V
	For min. gain V _{IO} = 0	2.5			V
V ₇ Sync input			.7	1.2	V
I _{V5} AGC leakage				.5	mA
ΔV ₁₁ ΔV ₁₂	V ₁₃ = 10.5 to 15V		100		mV/V
			50		mV/V

NOTES
1. According to test circuit; V₁ = effective sync pulse level at 60%.
2. Test level a_{cc} = -3dB
a_{cc} = -20dB referring to picture carrier.



AC ELECTRICAL CHARACTERISTICS $V_{13} = 12.4$; $f_c = 45$ MHz; $f_m = 1$ kHz; MOD = 78%

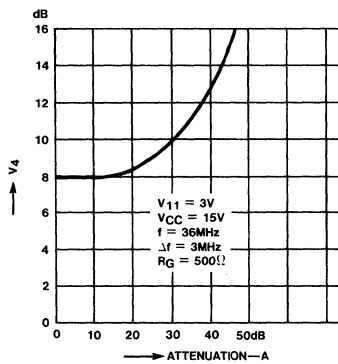
PARAMETER	TEST CONDITIONS	TBA1440G/1441G			UNIT
		Min	Typ	Max	
Black level Pin 11	$V_{IN} = 80$ mv NO. MOD		.7		V
Black level Pin 12			5.8		V
A.G.C. sat. vol. Pin 5	1440G $V_{IN} = 80$ mv 1441G $V_{IN} = 0$		1.3	2.2	V
Audio output P _{11, 12}	$V_{IN} = 80$ mV	3.2	3.8	4.5	V _{PR}
Sensitivity	$V_{OUT} - 3$ DB		240	750	μ V
Intermodulation (3 MHz)			45		DB

NOTES

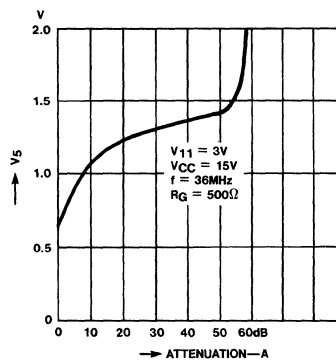
1. According to test circuit; V_1 = effective sync pulse level at 60 Ω .
2. Test level $a_{CC} = -3$ dB
 $a_{CC} = -20$ dB referring to picture carrier.

TYPICAL PERFORMANCE CHARACTERISTICS

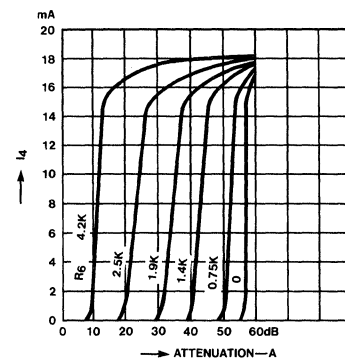
NOISE FIGURE vs ATTENUATION (MEASURED AD VIDEO FREQUENCY)
 $-V_{fb} = 3$ V, $V_{CC} = 15$ V, $f = 36$ MHz,
 $\Delta f = 3$ MHz, $R_G = 500\Omega$



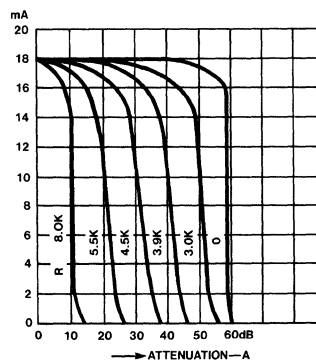
CONTROL VOLTAGE vs ATTENUATION
 $-V_{fb} = 3$ V, $V_{CC} = 15$ V, $f = 36$ MHz,
 $R_G = 500\Omega$



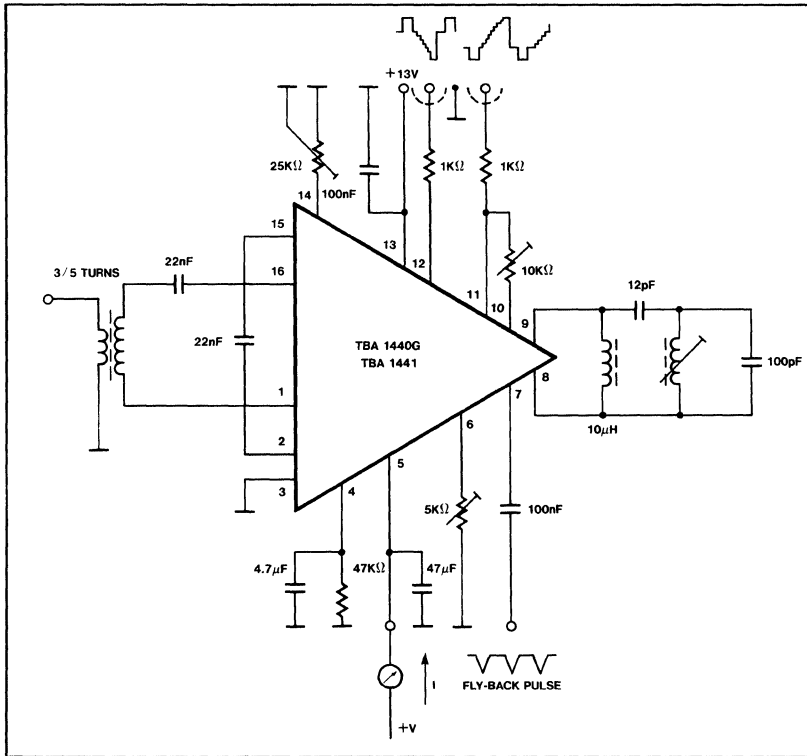
TUNER CONTROL CURRENT vs ATTENUATION
 $R_G =$ PARAMETER
 TBA1440G



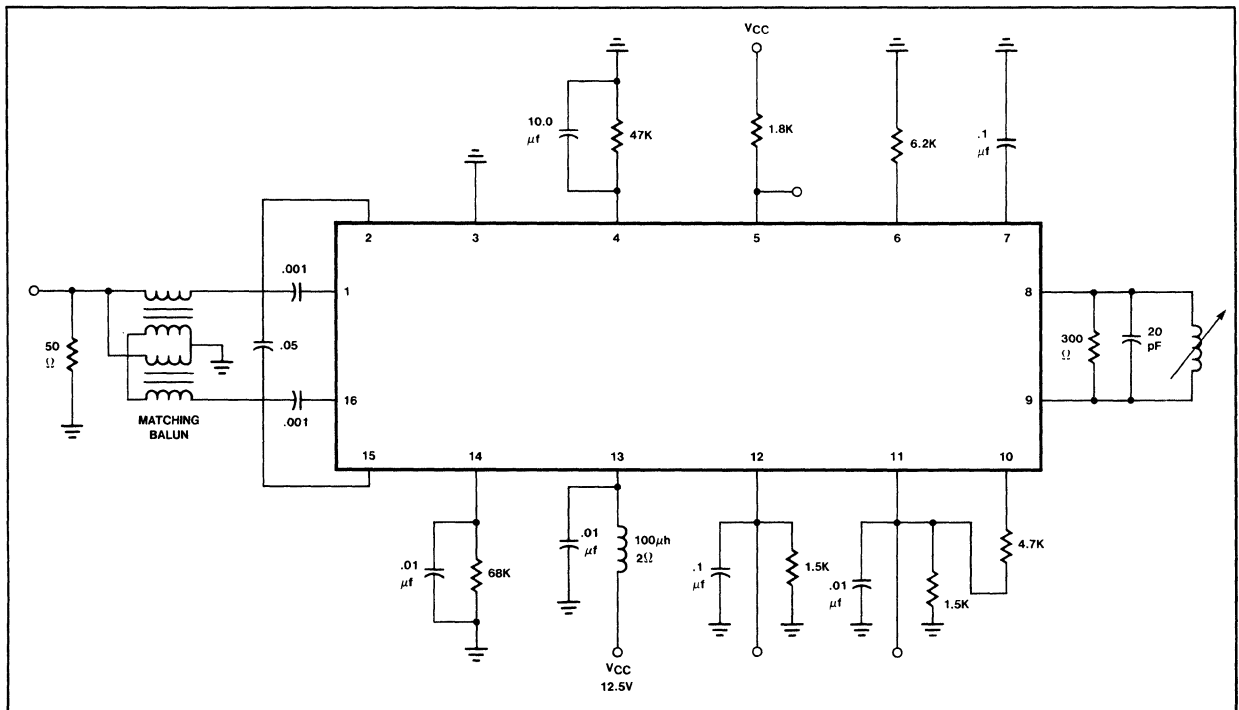
TUNER CONTROL CURRENT vs ATTENUATION
 $R_G =$ PARAMETER
 TBA1441



APPLICATION

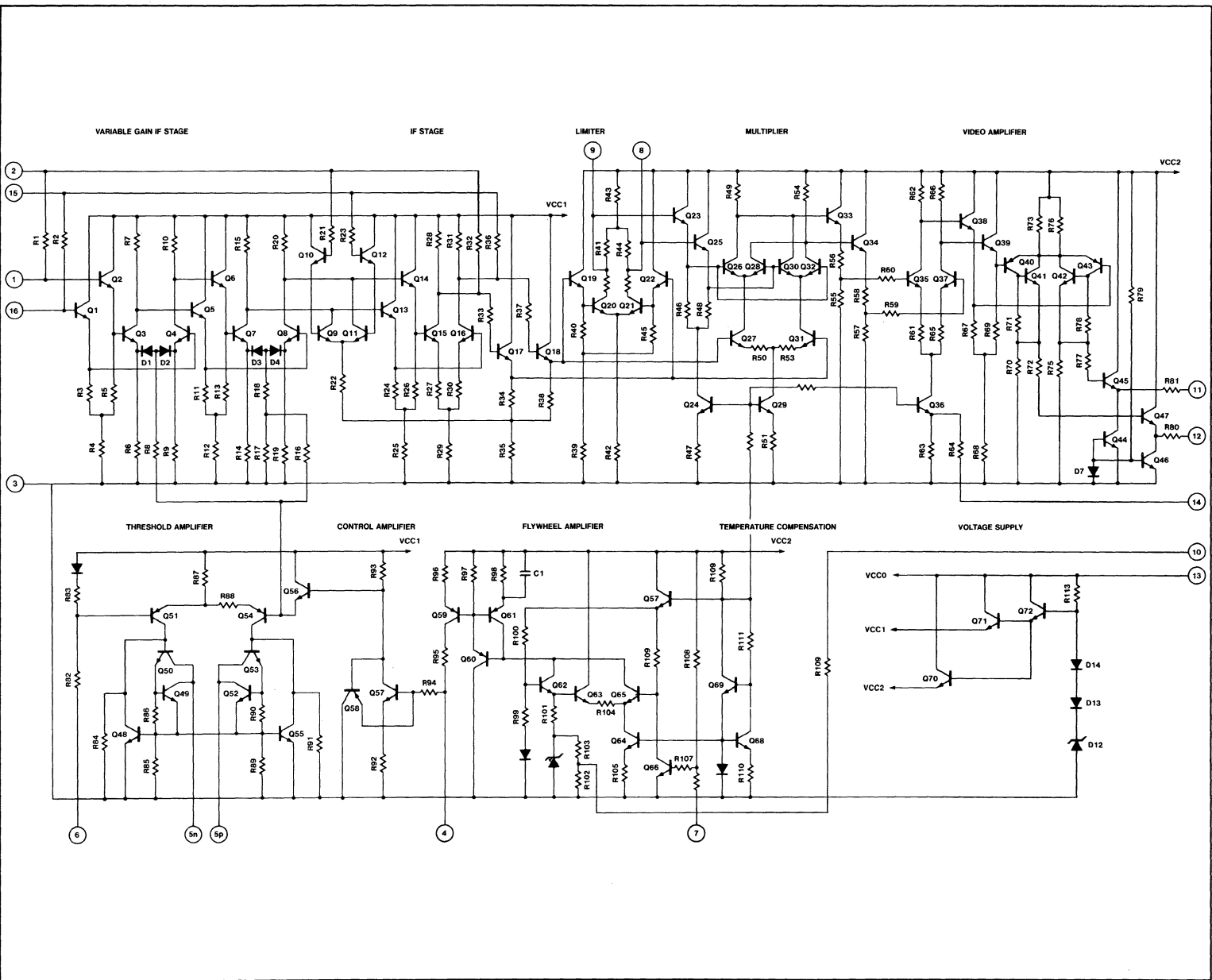


TEST CIRCUIT



12

EQUIVALENT SCHEMATIC



DESCRIPTION

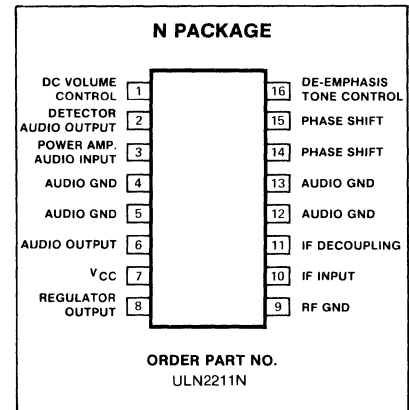
The ULN2211 contains a limiting amplifier, an FM quadrature detector, an electronic gain control stage and a 2-watt audio output stage. It can be used to detect and amplify any FM modulated signal having a 0.1-20MHz carrier frequency.

It is especially recommended as a complete TV sound channel requiring few external components and only one tuning adjustment for the 4.5MHz tank circuit. Provision is made for 6dB/octave de-emphasis and tone control.

FEATURES

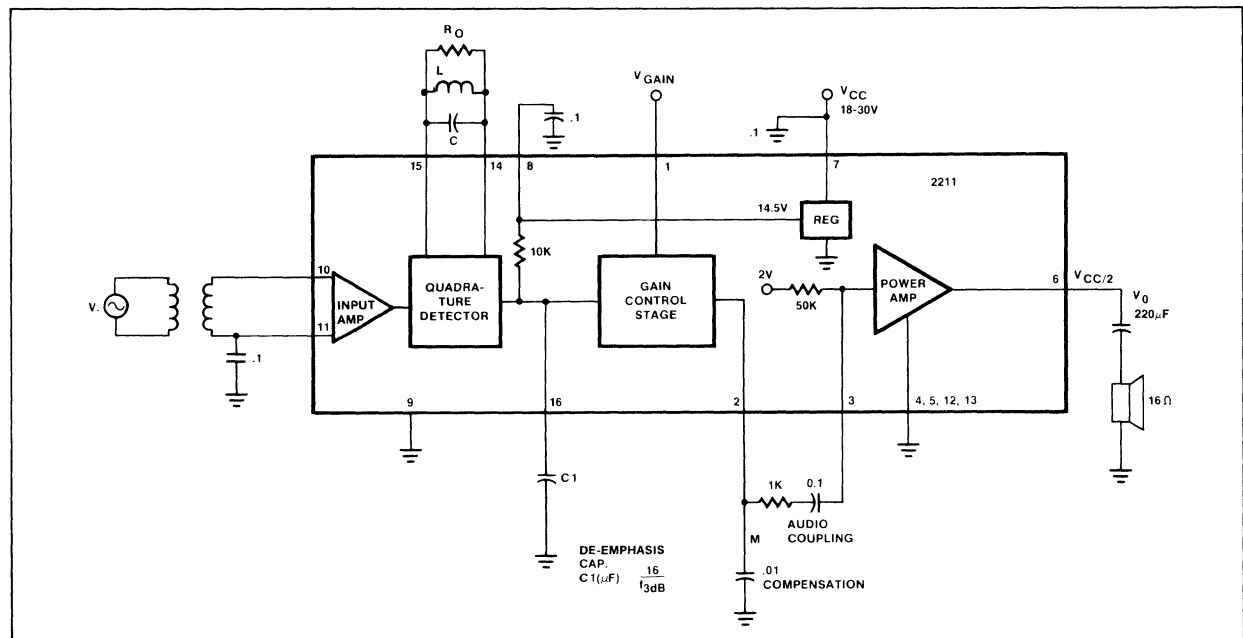
- 2-watt output
- DC volume control attenuation, 70dB typ
- Limiter gain of 70dB
- Limiting threshold typically less than 200 μ V
- Automatic thermal shutdown
- Over-current limiting
- 20dB ripple rejection
- Single supply operation (18-30V)
- No crossover distortion

PIN CONFIGURATION



NOTE: Internal power dissipation in watts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V _{CC}	+30	V
Input voltage (pin 10)	+4.0	V _{rms}
Power consumption (internal)	See Figure 1	
Operating temperature	-25 to +70	°C
Storage temperature	-65 to +150	°C



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +24\text{V}$; $f_o = 4.5\text{MHz}$, $\Delta f = 25\text{kHz}$, $f_m = 400\text{Hz}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	ULN2211			UNIT
		Min	Typ	Max	
V_{TH}	Recovered audio limiting threshold ¹		150	350	μV
AMR	AM rejection ²		55		dB
V_O	Recovered AF voltage (pin 16)	30 500	800		mVrms
THD _D	Detector output distortion		1.0	2.0	%
THD _O	Output distortion		2	10	%
	Playthrough		10	15	mVrms
I_{MAX}	Current limit		800		mA
V_N	Noise		15	25	mVrms
A_V	Power AMP voltage gain ³	25	27	29	dB
V_O/V_{CC}	Output tracking (V_6/V_7)		0.5		V/V
Z_{IN}	Audio amp input impedance	40	50	60	k Ω

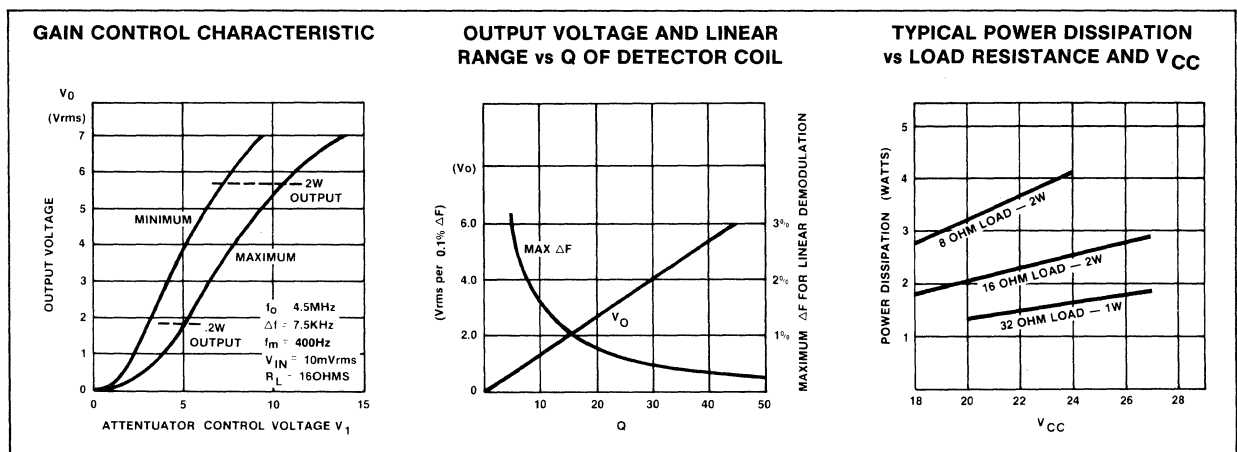
NOTES

- Measured with output at -3dB, reference $V_{IN} = 10\text{mV}$, $\Delta f = 25\text{kHz}$
- $AMR = 20 \log \frac{V_O(\text{FM}, \Delta f = 7.5\text{kHz})}{V_O(\text{AM}, 30\%)}$
- Set $V_O = 1\text{Vrms}$. $A_V = 20 \log \frac{1}{(V_{3\text{rms}})}$

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +24\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	ULN2211			UNIT
		Min	Typ	Max	
I_{CC}	Standby current	25	45	60	mA
V_6	Terminal voltage	10.5	12.5	14.5	V
V_{10}			1.4		V
V_{11}			1.4		V
V_{14}, V_{15}			4.0		V
V_{16}			8.0		V
V_8		14	14.5	16	V
V_2			10		V
V_3			2.6		V

TYPICAL PERFORMANCE CHARACTERISTICS



MAXIMUM ALLOWABLE POWER DISSIPATION

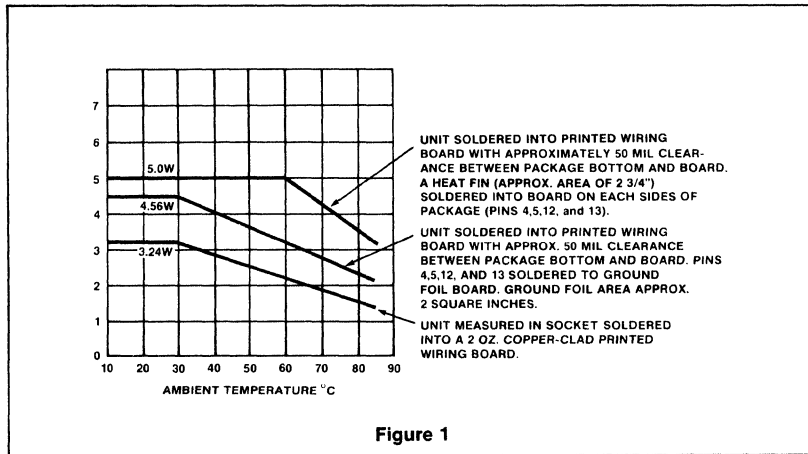


Figure 1

TYPICAL APPLICATION

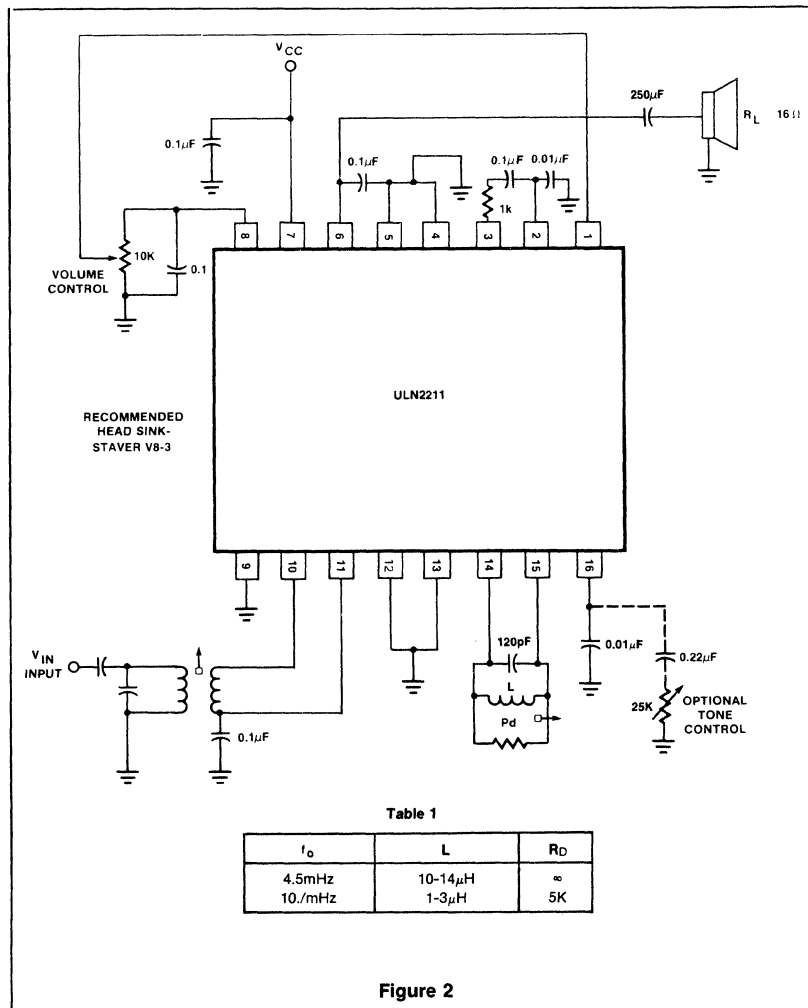


Table 1

f_o	L	R_D
4.5mHz	10-14µH	∞
10./mHz	1-3µH	5K

Figure 2



SECTION 13 AUDIO CIRCUITS

Section 13—AUDIO CIRCUITS

LM387	Dual Low-Noise Preamp	411
NE/SE540	Power Driver	415
NE542	Dual Low Noise Preamp	420
NE545*	Dolby Noise Reduction Processor	
NE570/571/SA571	Compandor	423
NE572	Programmable Analog Compandor	425
NE645B/646B-N	Dolby Noise Reduction Processor	427

NEW PRODUCT

SD5340 4-Input/2-Output Audio Source Selector—Available 2nd Quarter 1981

NOTE

*This data sheet may be obtained by writing Publication Services at Signetics,
811 E. Arques, M/S 027, Sunnyvale, California 94086, or by calling (408) 746-2111.

DESCRIPTION

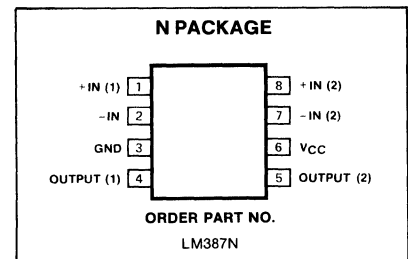
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110dB supply rejection and 60dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing ($V_{CC} - 2V$ p-p), and wide power bandwidth (75kHz, 20V p-p). The LM387 operates from a single supply across the wide range of 9 to 40V.

The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

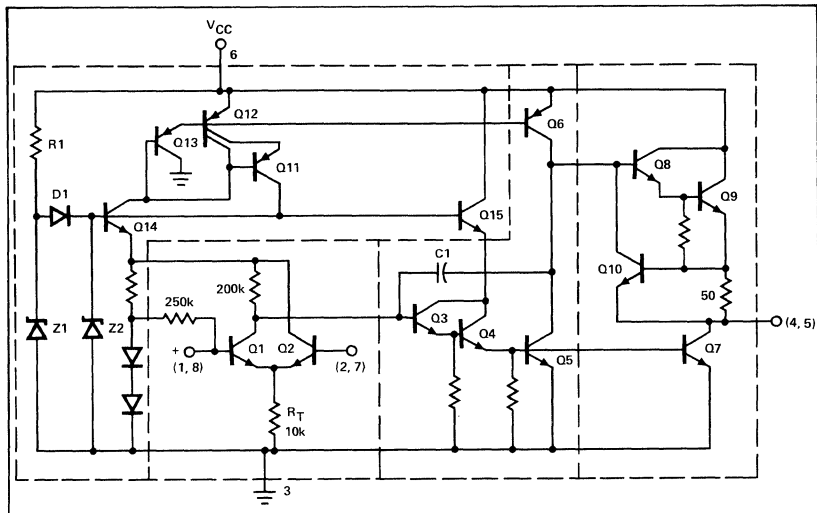
FEATURES

- Low noise— $0.8\mu V$ total input noise
- High gain—104dB open loop
- Single supply operation
- Wide supply range 9 to 40V
- Power supply rejection—110dB
- Large output voltage swing ($V_{CC} - 2V$ p-p)
- Wide bandwidth 15MHz unity gain
- Power bandwidth 75kHz, 20V p-p
- Internally compensated
- Short circuit protected

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 14V$ unless otherwise specified.

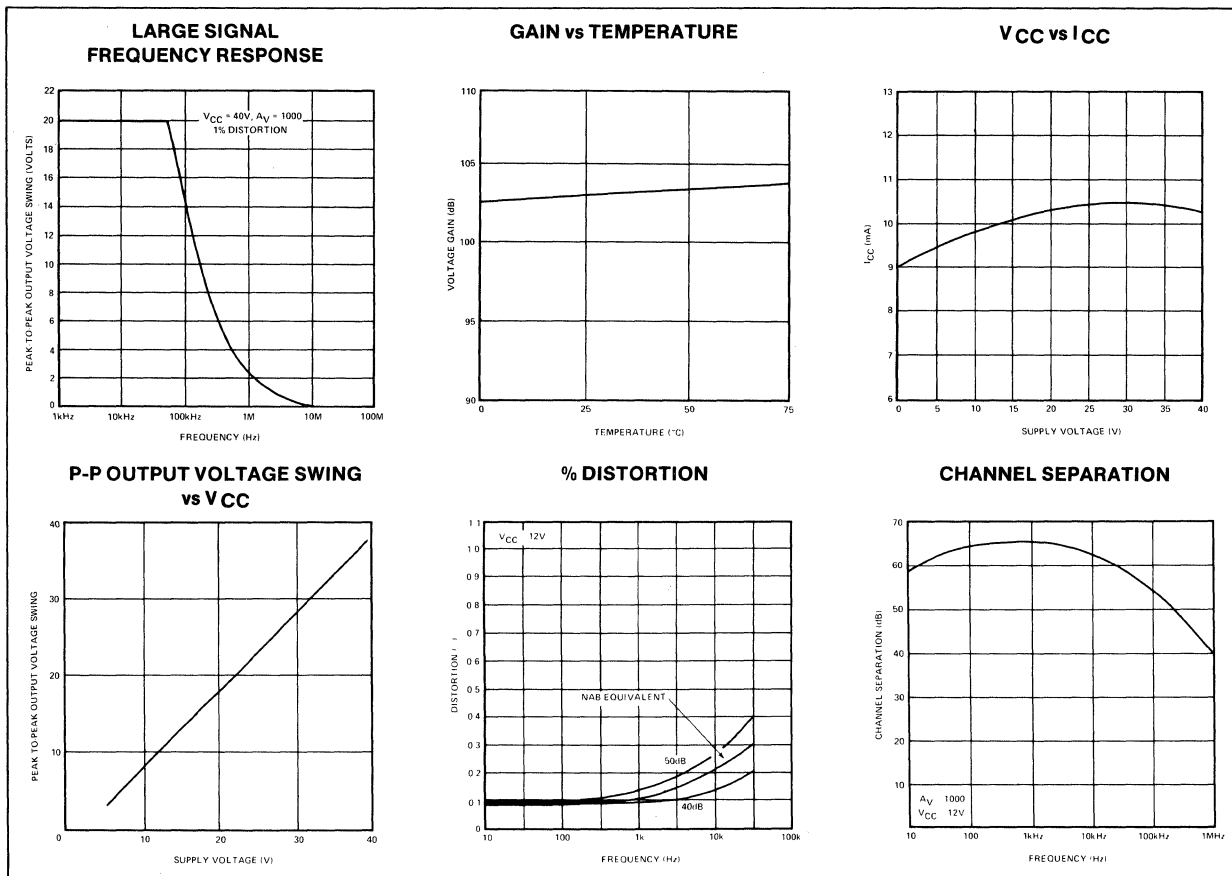
PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input resistance	Positive input		100		k Ω
	Negative input		200		k Ω
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak		$V_{CC}-2$		V



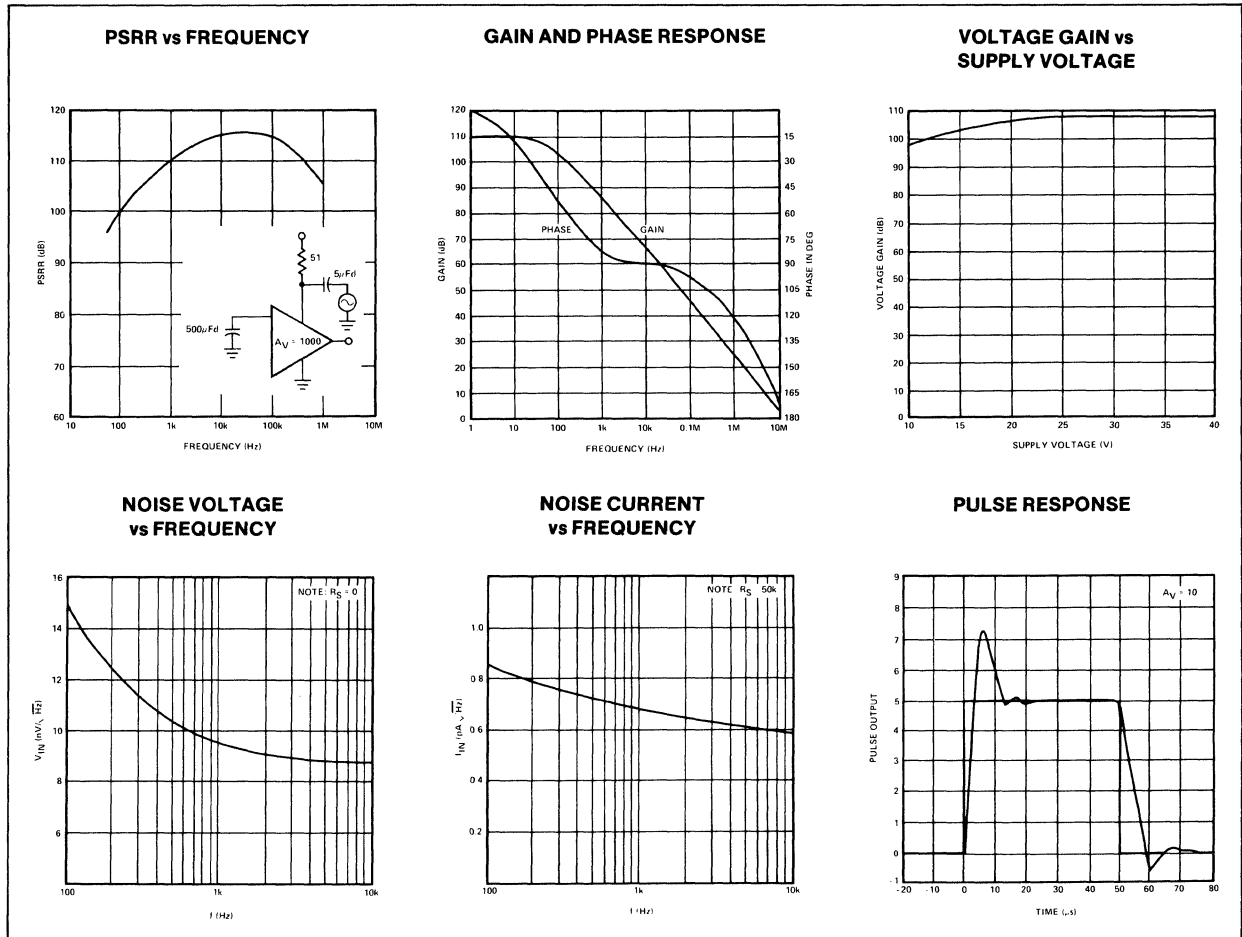
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 14\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Small signal bandwidth	20V p-p ($V_{CC} = 24\text{V}$) Linear operation		15		MHz
Power bandwidth			75		kHz
Maximum input voltage					300
Supply rejection ratio	$f = 1\text{kHz}$		110		dB
Channel separation	$f = 1\text{kHz}$		60		dB
Total harmonic distortion	75dB gain, $f = 1\text{kHz}$		0.1		%
Total equivalent input noise	$R_S = 600\Omega$, 100-10,000Hz		0.8	1.4	μVrms
Noise figure	50k Ω , 100-10,000Hz		1.0		dB
	10k Ω , 100-10,000Hz		1.6		dB
	5k Ω , 100-10,000Hz		2.8		dB

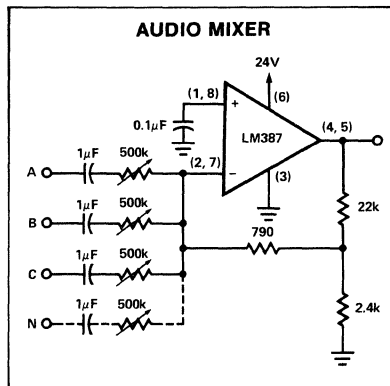
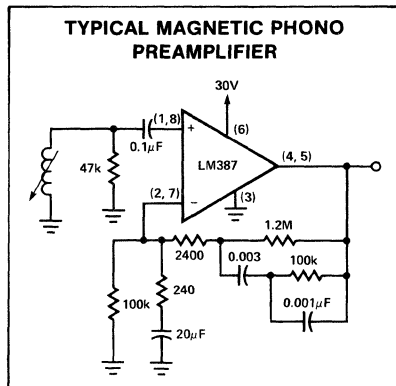
TYPICAL PERFORMANCE CHARACTERISTICS



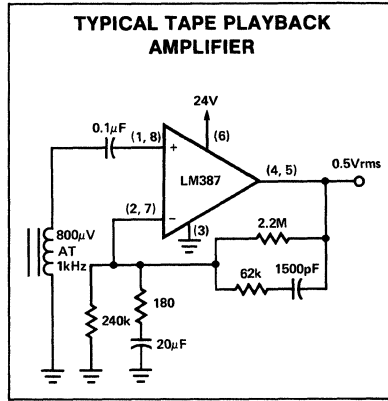
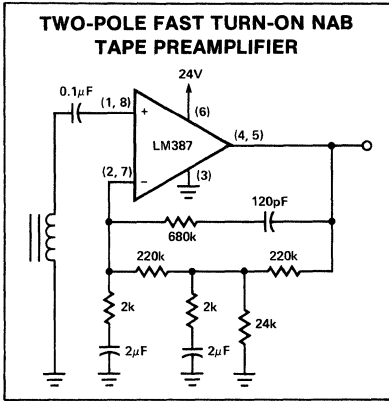
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TYPICAL APPLICATIONS



TYPICAL APPLICATIONS (Cont'd)



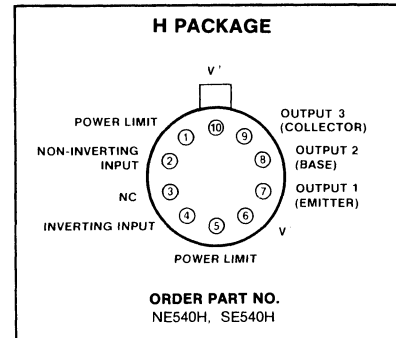
DESCRIPTION

The NE/SE540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

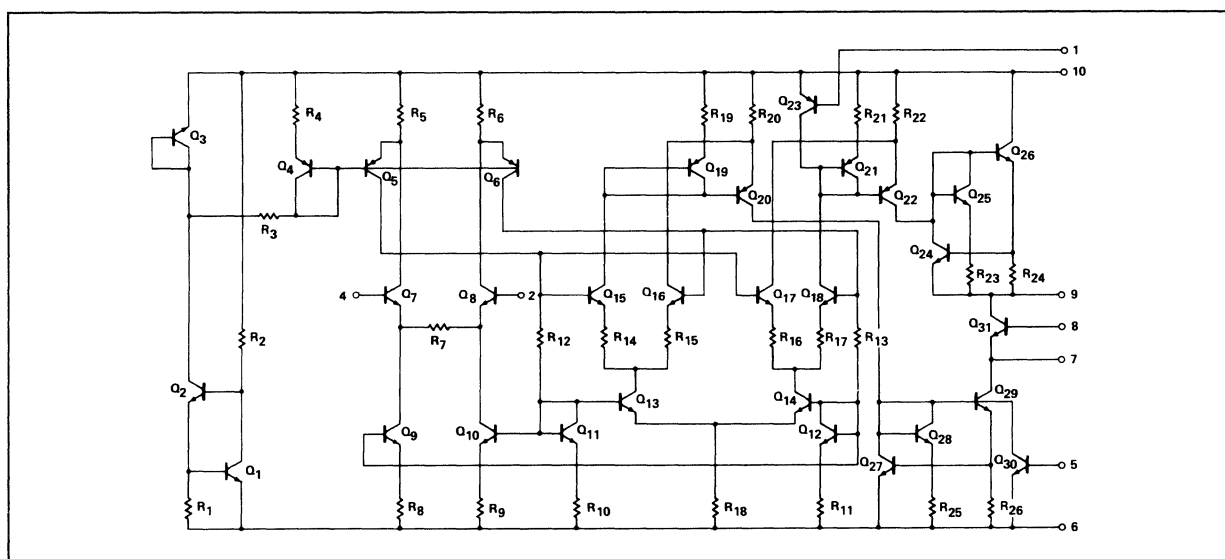
FEATURES

- **Internal current limiting**
- **Low standby current**
- **High output current capability**
- **Wide power bandwidth**
- **Low distortion**

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE540	±27	V
NE540	±22	V
Operating temperature range		
SE540	-55 to +125	°C
NE540	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ and $V_{CC} = \pm 20\text{V}$ unless otherwise specified.

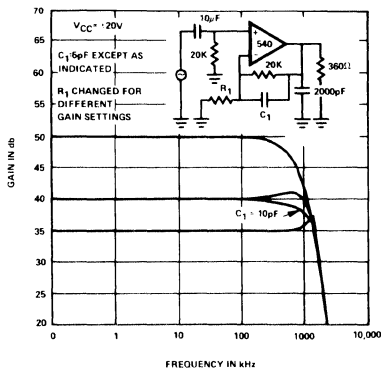
PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Operating supply voltage		± 5		± 25	± 5		± 20	V
Quiescent current			13	20		13	20	mA
Input offset voltage			5	7		7	10	mV
Input offset current			0.3	0.7		0.5	1	μA
Input bias current			1.5	3		2	5	μA
Input impedance			20			20		$\text{k}\Omega$
Current gain		80	100		70	90		dB
Gain variation over temperature range	40dB gain		± 0.1			± 0.1		dB
Power supply rejection ratio	40dB gain	80	90		60	80		dB
Common mode rejection ratio			110			90		dB
Output drive current		± 120	± 150		± 80	± 100		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ and $V_{CC} = \pm 20\text{V}$ unless otherwise specified.

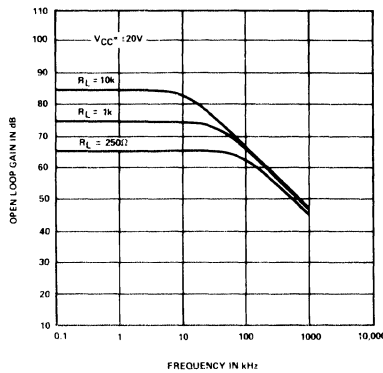
PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Frequency response	40dB gain $\pm 1\text{dB}$		500			100		kHz
Distortion	40dB gain, Output 3dB below clipping $R_L = 600\Omega$ $R_L = 2\text{k}\Omega$		0.25	0.5		0.5	1.0	%
			0.06			0.06		
Equivalent input noise voltage	$R_S = 600\Omega$ 50Hz to 500kHz		10			10		μV
Slew rate	$V_{CC} = \pm 20\text{V}$ $V_{OUT} = \pm 15\text{V}$		200			200		$\text{V}/\mu\text{s}$

TYPICAL PERFORMANCE CHARACTERISTICS

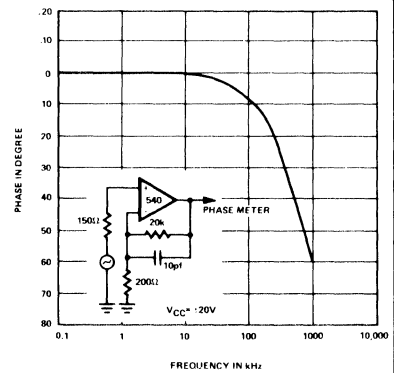
CLOSED LOOP FREQUENCY RESPONSE



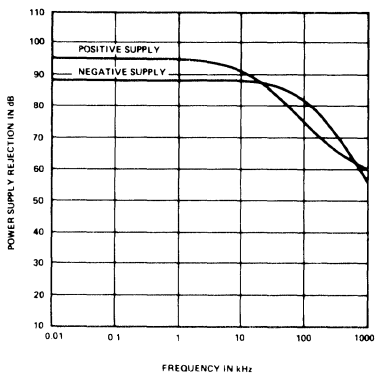
OPEN LOOP GAIN AND FREQUENCY RESPONSE



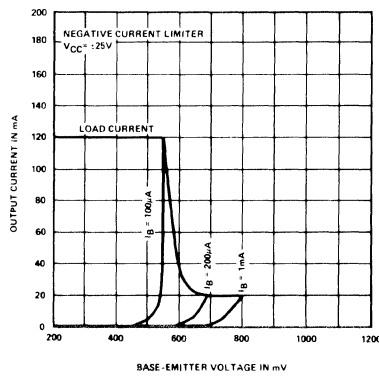
PHASE RESPONSE vs FREQUENCY



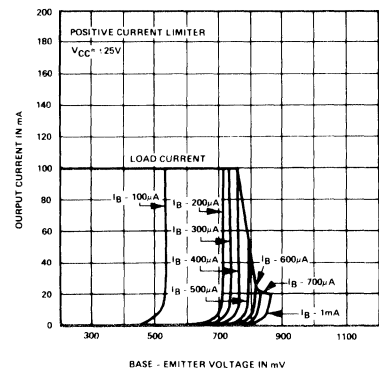
POWER SUPPLY REJECTION vs FREQUENCY



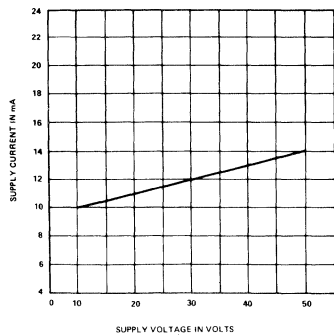
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



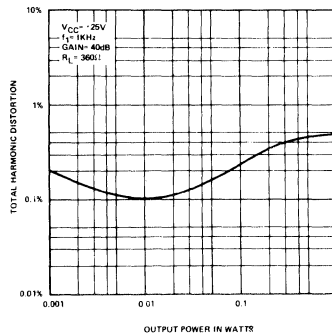
OUTPUT CURRENT vs I_B/V_{BE} OF CURRENT LIMITER



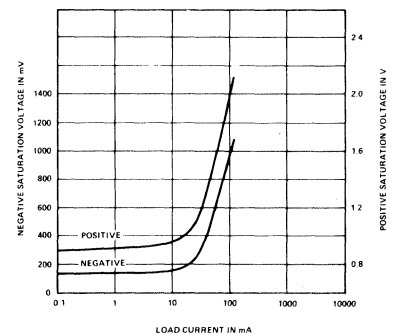
QUIESCENT CURRENT vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs OUTPUT

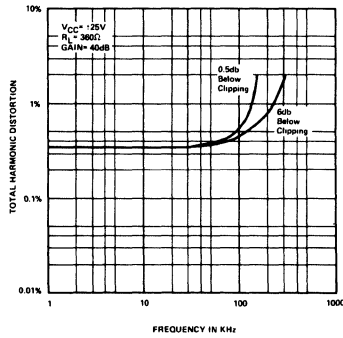


OUTPUT SATURATION VOLTAGE vs LOAD

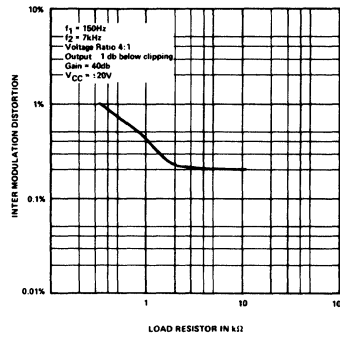


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

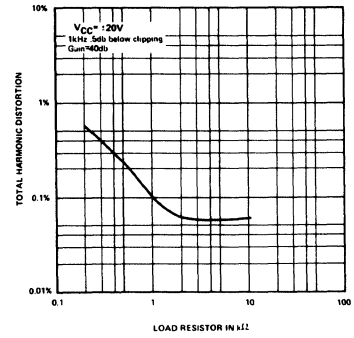
TOTAL HARMONIC DISTORTION vs FREQUENCY



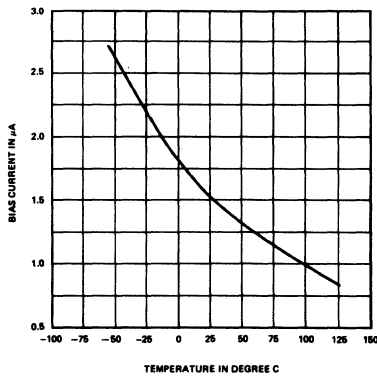
INTERMODULATION DISTORTION vs LOAD



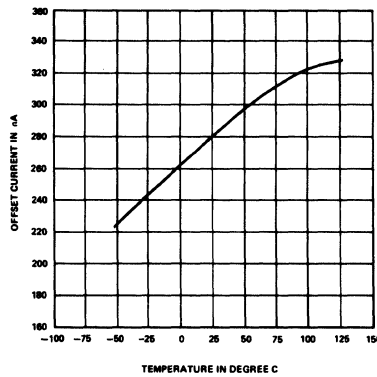
TOTAL HARMONIC DISTORTION vs LOAD



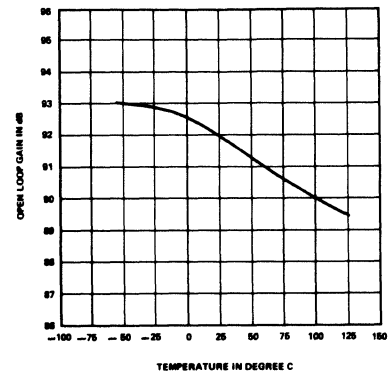
BIAS CURRENT vs TEMPERATURE



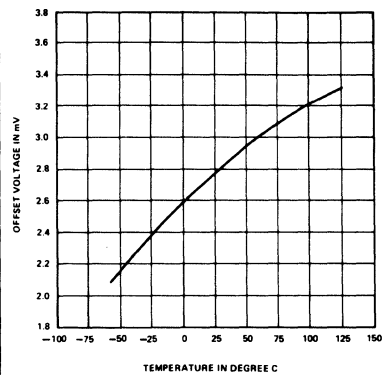
OFFSET CURRENT vs TEMPERATURE



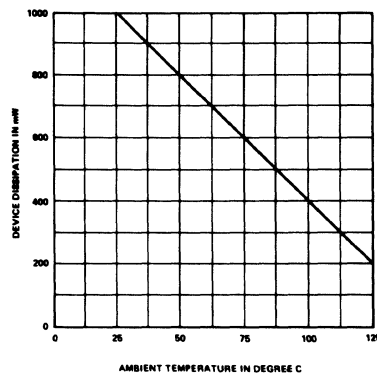
OPEN LOOP GAIN vs TEMPERATURE



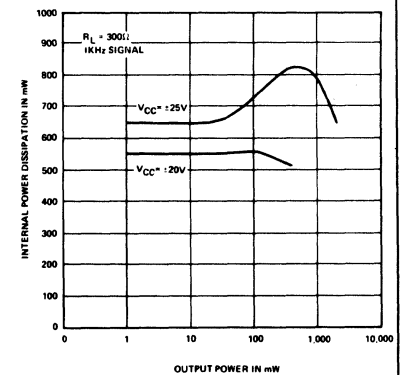
OFFSET VOLTAGE vs TEMPERATURE



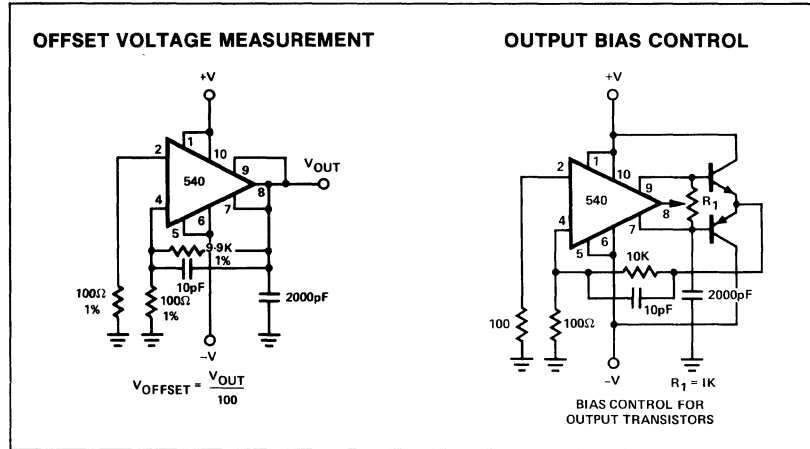
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



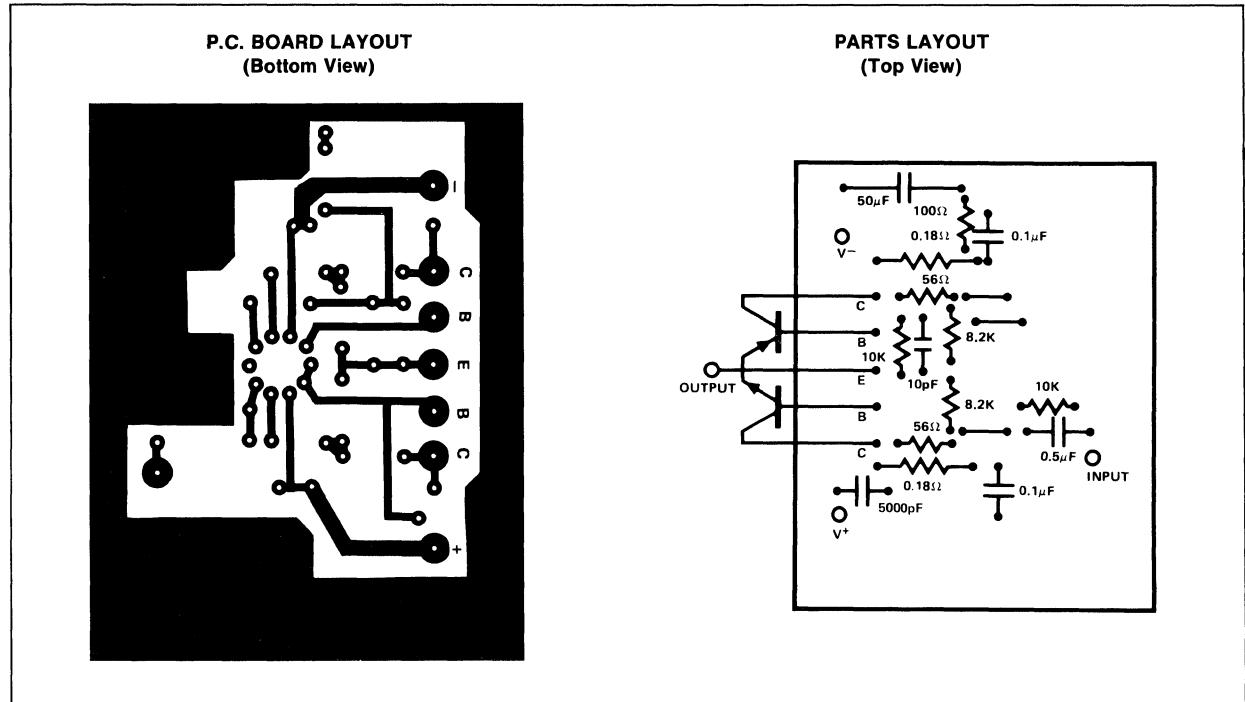
INTERNAL POWER DISSIPATION vs LOAD POWER



TEST CIRCUITS



35 WATT AMPLIFIER



DESCRIPTION

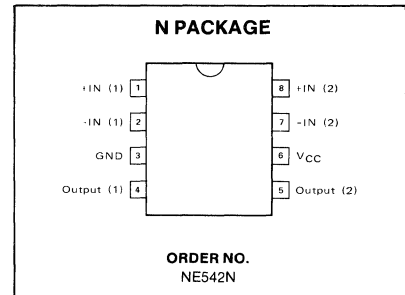
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing ($V_{CC} - 2V_{p-p}$), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

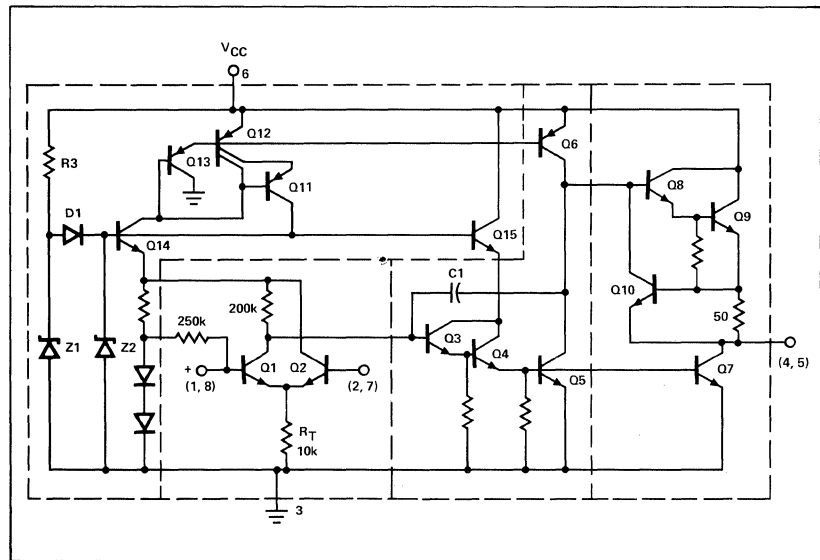
FEATURES

- Low noise— $7\mu V$ total input noise
- High gain—104dB open loop
- Single supply operation
- Wide supply range 9 to 24V
- Power supply rejection 110dB
- Large output voltage swing ($V_{CC} - 2V_{p-p}$)
- Wide bandwidth 15MHz unity gain
- Power bandwidth 100kHz (15V p-p)
- Internally compensated (stable at 10dB)
- Short circuit protected
- High slew rate $5V/\mu s$

PIN CONFIGURATION



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS

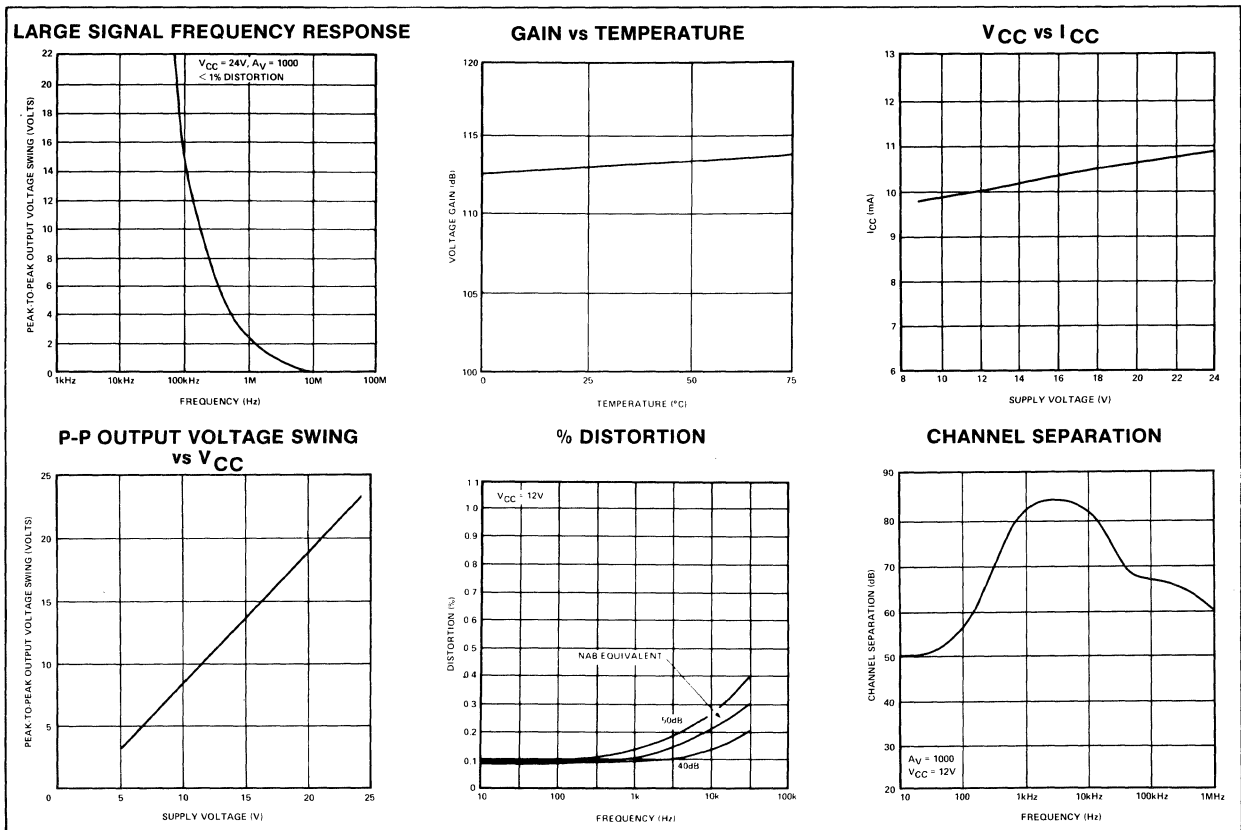
$T_A = 25^\circ C, V_{CC} = 14V$
unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage	$V_{CC} = 9 \text{ to } 18V, R_L = \infty$	9	9	24	V
Supply current				15	mA
Input resistance			100		k Ω
Positive input			200		k Ω
Negative input					
Output resistance	Open loop		150		Ω

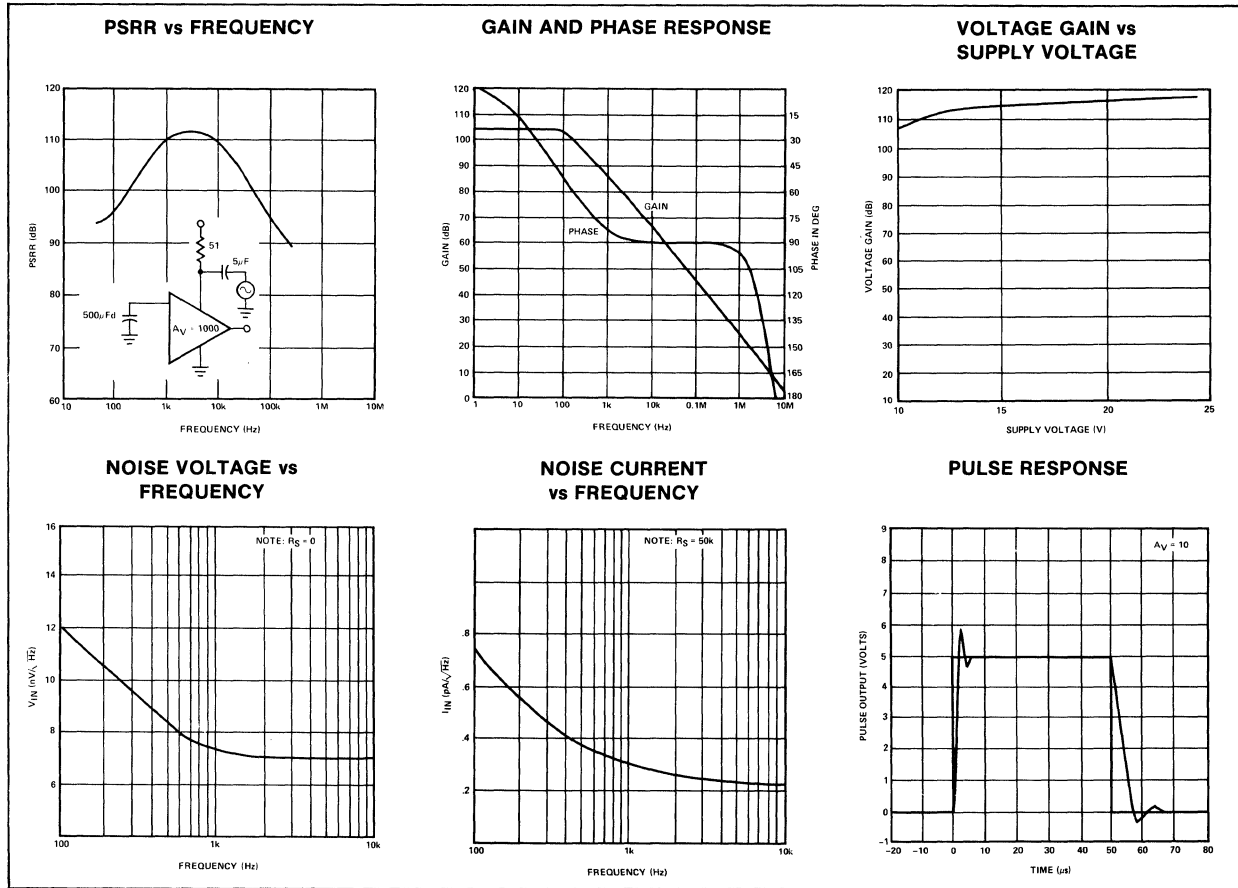
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 14\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			.5		μA
Output current	Source Sink (linear operation)	8 2	14 3		mA mA
Output voltage swing		$V_{CC} - 2.5$	$V_{CC} - 2$		V
Small signal bandwidth			15		MHz
Slew rate			5		$\text{V}/\mu\text{s}$
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	$f = 60, 120\text{Hz}$		100		dB
	$f = 1\text{kHz}$		110		dB
Channel separation	$f = 1\text{kHz}$		70		dB
Total harmonic distortion	75dB gain, $f = 1\text{kHz}$.1		%
Total equivalent input Noise	$R_S = 600\Omega$, 100 - 10,000Hz		.7	1.2	μVrms
Noise figure	$R_S = 50\text{k}\Omega$, 10 - 10,000Hz		1.2		dB
	$R_S = 20\text{k}\Omega$, 10 - 10,000Hz		1.2		dB
	$R_S = 10\text{k}\Omega$, 10 - 10,000Hz		1.5		dB
	$R_S = 5\text{k}\Omega$, 10 - 10,000Hz		2.4		dB

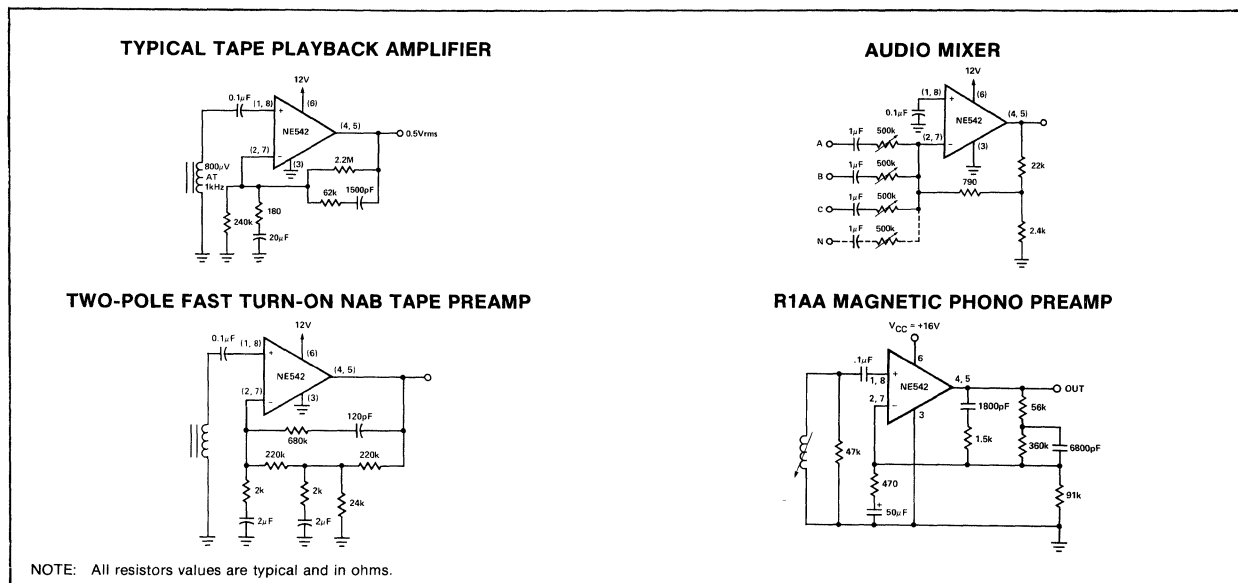
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TYPICAL APPLICATIONS



DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expander. Each channel has a full wave rectifier to detect the average value of the signal; a linearized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

- Complete compressor and expander in 1 IC
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6Vdc
- System levels adjustable with external components
- Distortion may be trimmed out

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF} . The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than $.1\mu A$.

$$G \propto \frac{|V_{IN} - V_{REF}|_{ave}}{R_1}$$

or

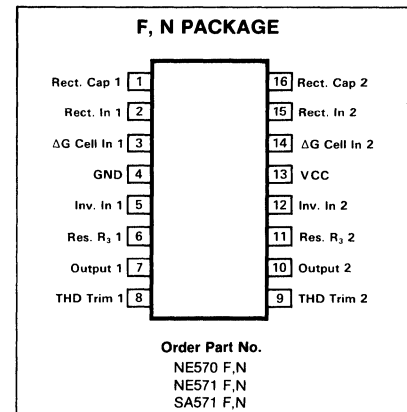
$$G \propto \frac{|V_{IN}|_{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or com-

APPLICATIONS

- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expander—noise gate
- Dynamic noise reduction systems
- Voltage controlled amplifier
- Dynamic filters

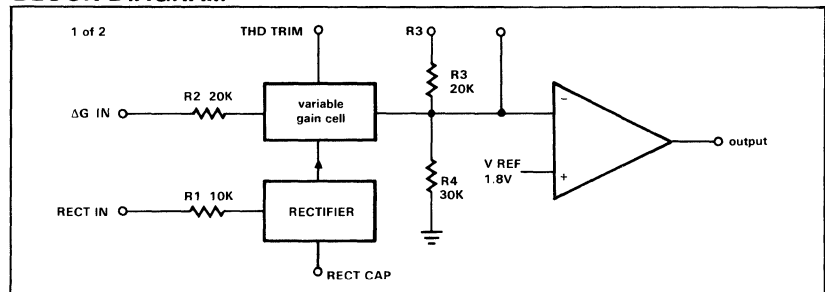
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply	24	Vdc
570	18	
571		
T_A Operating temperature range	0 to 70	$^{\circ}C$
NE	-40 to +85	$^{\circ}C$
SA	400	mW
P_D Power dissipation		

BLOCK DIAGRAM



pressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final}) e^{-t/\tau} + G_{final}; \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF} . The following equation applies for capacitively coupled inputs. The output current, I_{OUT} , is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF} , and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3 , is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

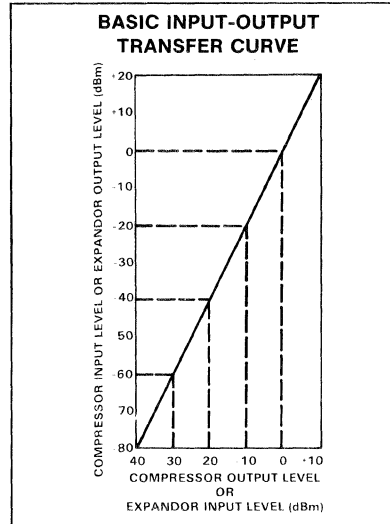


The output stage is capable of $\pm 20\text{mA}$ output current. This allows a $+13\text{dBm}$ (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in $+13\text{dBm}$ with a 600Ω output impedance.

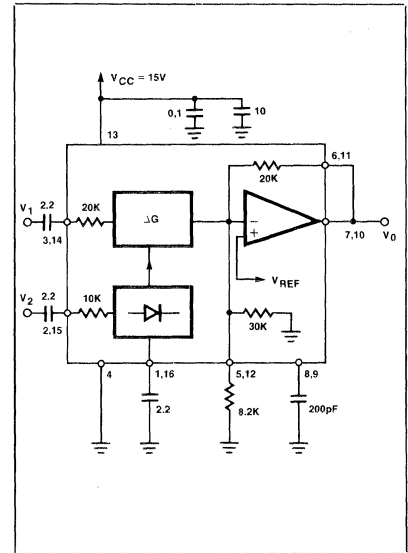
A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempo of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 15\text{V}^1$

PARAMETER	TEST CONDITIONS	NE570			NE/SA571 ⁶			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		± 20						mA
Output slew rate			± 5					V/us
Gain cell distortion ²	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			± 5	± 15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift ³	Untrimmed		± 20	± 50		± 30	± 100	mV
Expander output noise	No signal, 20Hz-20kHz		20					μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dB
Gain change ^{2,4}	$-40^\circ\text{C} < T < 70^\circ\text{C}$		± 1			± 1		dB
	$0^\circ\text{C} < T < 70^\circ\text{C}$		± 1	± 2		± 1	± 4	
Reference drift ⁴	$-40^\circ\text{C} < T < 70^\circ\text{C}$		+2, -25	-10, -40		+2, -25	+20, -50	mV
	$0^\circ\text{C} < T < 70^\circ\text{C}$		± 5	± 10		± 5	± 20	
Resistor drift ⁴	$-40^\circ\text{C} < T < 70^\circ\text{C}$		+8, -0					%
	$0^\circ\text{C} < T < 70^\circ\text{C}$		+1, -0					
Tracking error ⁵ , input	Rectifier input, $V_2 =$							dB
$V_1 = 0\text{dBm}$	+6dBm		± 2					
	-10dBm		+2	-2,+4		+2	-2,+5	
	-20dBm		+2	-3,+6		+2	-4,+7	
	-30dBm		+2	-5,+1		+2	-1,+1.5	
	-40dBm		+2,-4			+2,-4		

NOTES

- Except where indicated, the 571 specifications are identical to the 570
- Measured at 0dBm , 1kHz
- Expander ac input change from no signal to 0dBm
- Relative to value at $T_A = 25^\circ\text{C}$
- Relative to 0dBm
- Electrical characteristics for the SA571 only are specified over -40 to $+85^\circ\text{C}$ temperature range.

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic gain compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous companders.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

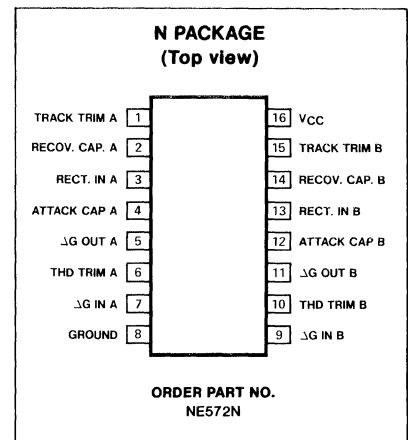
FEATURES

- Independent control of attack and recovery time.
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external Op Amp
- Wide dynamic range—greater than 110dB
- Temperature compensated gain control
- Low distortion gain cell
- Low noise
- Wide supply voltage range—down to 6V.
- System level adjustable with external components.

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expander
- Automatic level control
- High level limiter
- Low level noise gate
- State variable filter

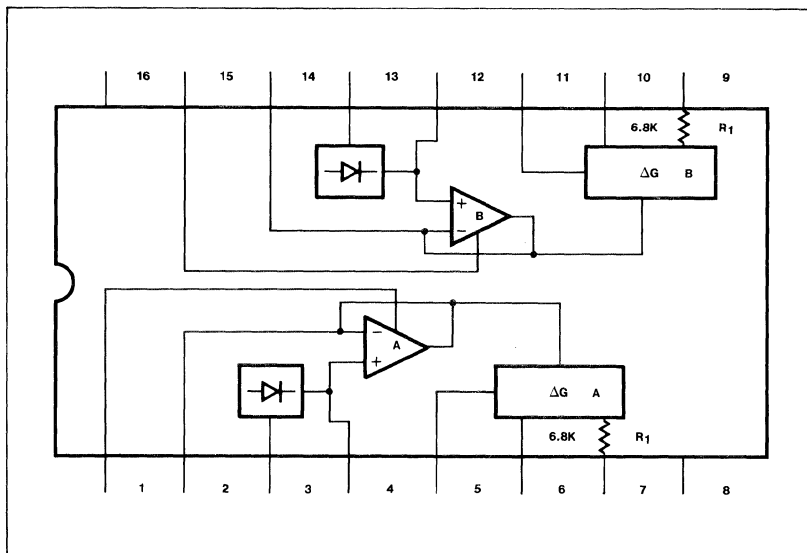
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	22	VDC
T _A Operating temperature range	0 to 70	°C
P _D Power dissipation	500	mW

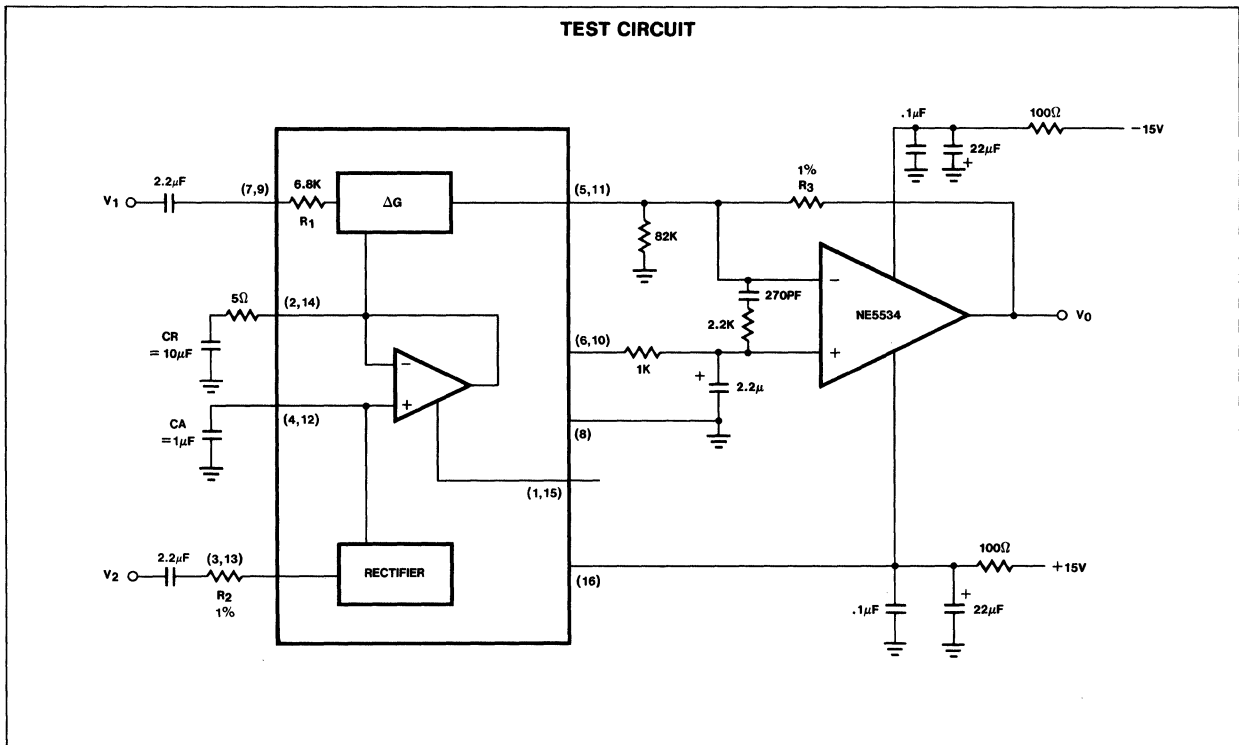
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Standard Test Conditions (unless otherwise noted) $V_{CC} = 15V$ $T_A = 25^\circ C$ Expander mode (see test circuit) Input signals at unity gain level = 100mV RMS at 1KHz, $V_1 = V_2$, $R_2 = 3.3K$ $R_3 = 17.3K$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CC} Supply voltage		6		22	V_{DC}
I_{CC} Supply current	No Signal			6	mA
Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD (untrimmed)	1kHz $C_A = 1.0\mu F$.2	1.0	%
THD (trimmed)	1kHz $C_R = 10\mu F$.05		%
THD (trimmed)	100Hz		.25		%
No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		10	25	μV
DC level shift (untrimmed)	Input change from no signal to 100mV RMS		± 20	± 50	MV
Unity gain level		-1	0	+1	dB
Large signal distortion	$V_1 = V_2 = 400mV$		1.0	3.0	%
Tracking error measured relative to value at unity gain output	Rectifier input $V_2 = +6dB$ $-30dB$		$\pm .2$ $\pm .5$	-1.5 $+ .8$	dB
Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
Power supply rejection ratio	120Hz		60		dB



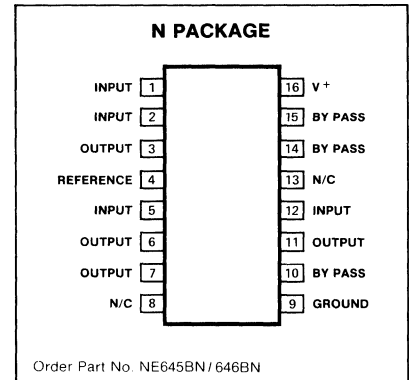
NE645/646B-N

DESCRIPTION

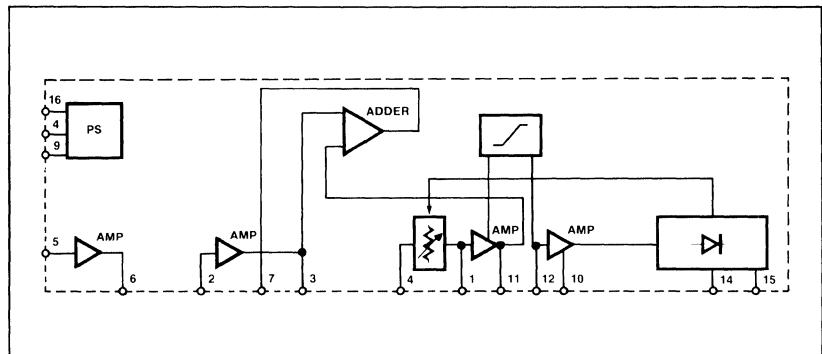
The NE645B/646B is a monolithic audio noise reduction system circuit. This circuit is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is intended for use in a Dolby* B-type noise reduction system and is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco.

NOTE
*T.M. Dolby Laboratories

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		°C
Operating	0 to +70	
Storage	-65 to +150	
Lead temperature (soldering, 60sec)	+300	°C



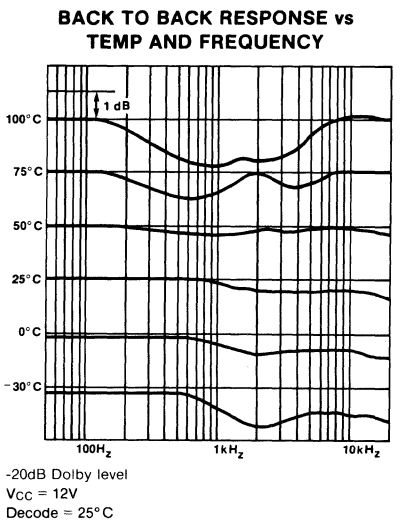
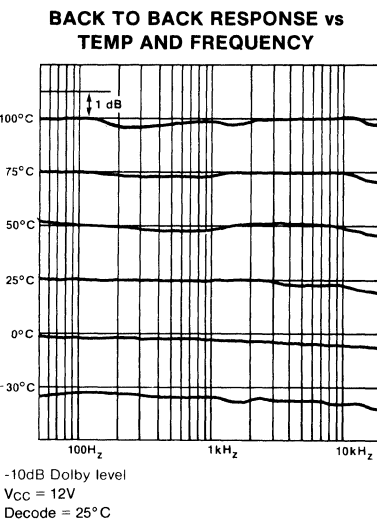
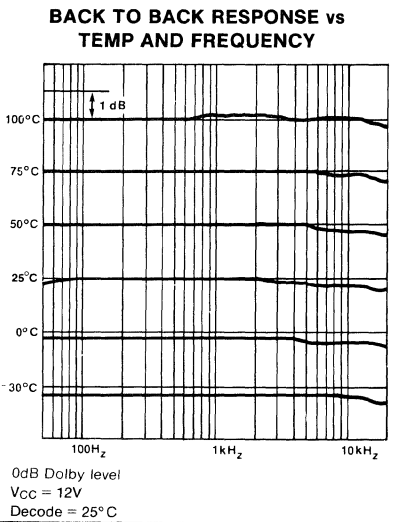
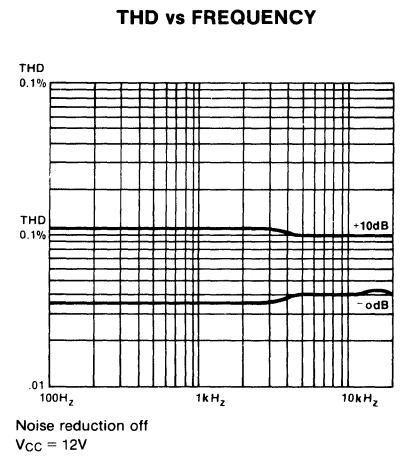
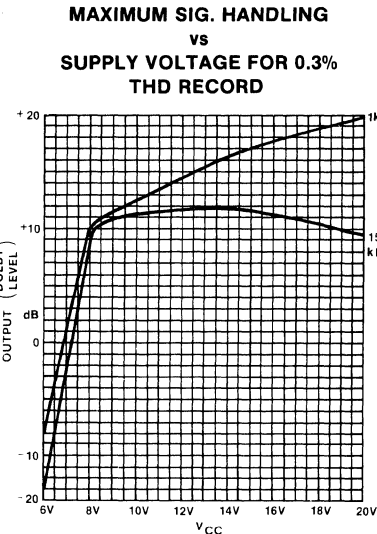
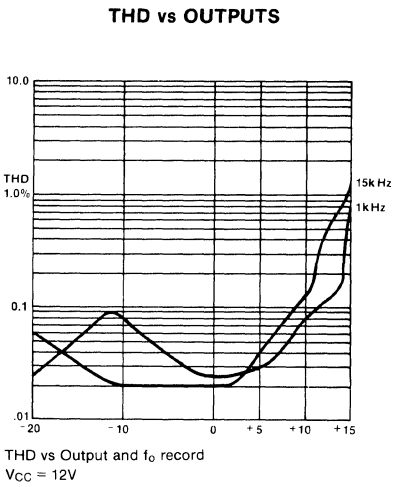
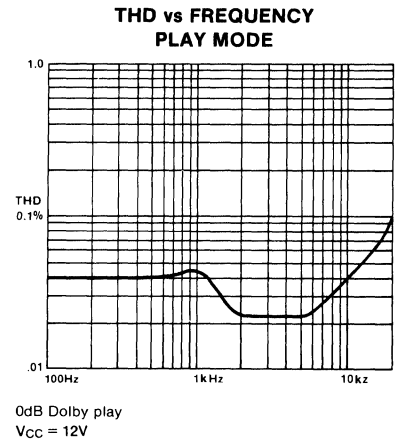
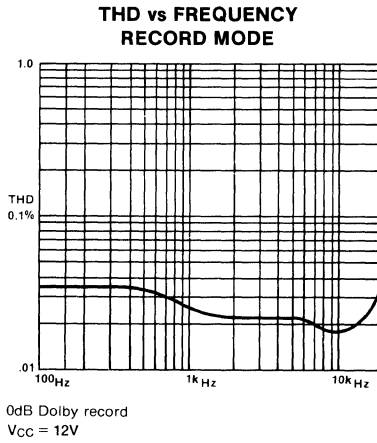
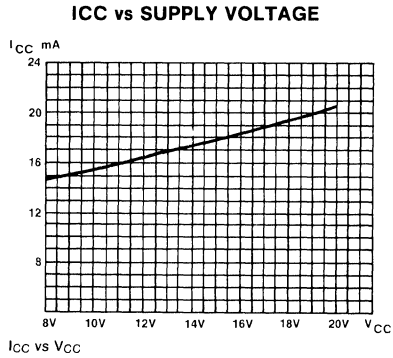
DC ELECTRICAL CHARACTERISTICS $V_{CC} = 12$ volts, $f = 20$ Hz to 20kHz.
 All levels referenced to 580mVrms (0dB) at Pin 3, $T_A = +25^\circ\text{C}$
 unless otherwise noted.

PARAMETER	TEST CONDITIONS	NE645B			NE646B			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range		8		20	8		20	V
Supply current			16	24		16	24	mA
Voltage gain (Pins 5-3)	$f = 1$ kHz (Pins 6 & 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (Pins 3-7)	$f = 1$ kHz, 0dB at pin 3, Noise reduction out	-0.5	0	+0.5	-0.5	0	+0.5	dB
Distortion	$f = 20$ Hz -20kHz 0db		0.05	0.1		0.05	0.2	%
	$f = 20$ Hz -15kHz, +10db		0.15	0.3		0.2	0.5	%
Signal handling	$f = 1$ kHz distortion <0.3%	+10	+14		+10	+12		dB
Signal handling	$f = 1$ kHz distortion < 0.5%							dB
*Signal-to-noise ratio	Record (Pins 6 & 2 connected)	67	72		64	68		dB
	Record (Input on pin 2)	67	72		64	68		dB
	Playback (Pins 6 & 2 connected)	77	82		74	78		dB
	Playback (Input on pin 2)	77	82		74	78		dB
Record mode								
Frequency response (at pin 7)	$f = 1.4$ kHz							
	Input at pin 5 = 0dB	-1	0	+1	-1.5	0	+1.5	dB
	= -20dB	-16.6	-15.6	-14.6	-17.1	-15.6	-14.1	dB
	= -30dB	-23.5	-22.5	-21.5	-24.0	-22.5	-21.0	dB
	$f = 5$ kHz							
	Input at pin 5 = 0dB	-0.7	+0.3	+1.3	-1.2	+0.3	+1.8	dB
	= -20dB	-17.8	-16.8	-15.8	-18.3	-16.8	-15.3	dB
	= -30dB	-22.8	-21.8	-20.8	-23.8	-21.8	-20.3	dB
	= -40dB	-30.2	-29.7	-28.7	-30.2	-29.7	-28.2	dB
	$f = 20$ kHz							
	Input at pin 5 = 0dB	-0.3	+0.7	+1.7	-0.8	+0.7	+2.2	dB
	= -20dB	-18.3	-17.3	-16.3	-18.8	-17.3	-15.8	dB
	= -30dB	-25.2	-24.2	-23.2	-25.7	-24.2	-22.7	dB
Back-to-back frequency Response	Using typical record Mode response	-1	0	+1	-1.5	0	+1.5	dB
Input resistance	Pin 5	35	50	65	35	50	65	k Ω
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	k Ω
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	k Ω
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω

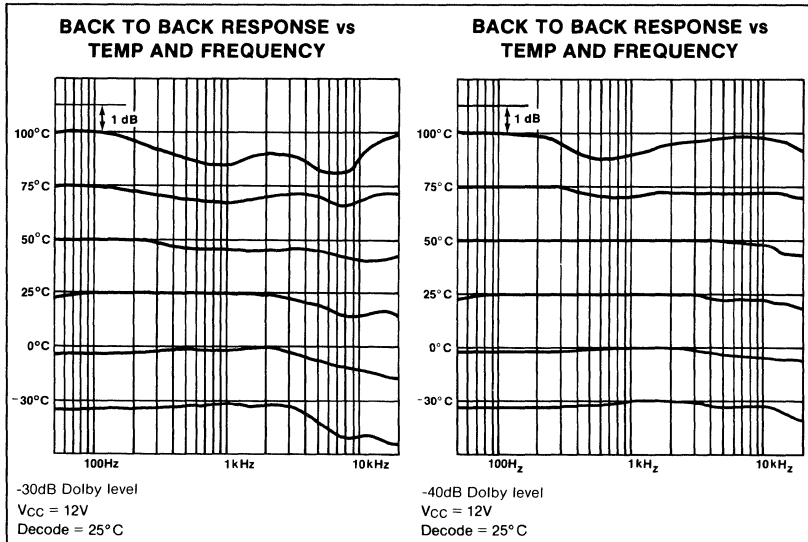
NOTE

* All noise levels are measured CCIR/ARM weighted and 10K source with respect to Dolby level. See Dolby Laboratories bulletin 19.

PERFORMANCE CHARACTERISTICS NE645B



PERFORMANCE CHARACTERISTICS NE645B (cont'd)



DOLBY B-TYPE ENCODER Output for constant level input (single tone frequency response)

Input level (dB) \ Freq. (kHz)	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40	-45
0.1	0	0.1	0	0.1	0	0	0	0	0	0.1
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1	0.2
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.3	0.5	0.6
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1	2.2
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9	3.0
0.6						3.6	3.7	3.8	3.7	3.8
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4	4.6
0.8						4.8	5.0	5.3	5.1	5.2
0.9							5.6	5.8	5.6	5.8
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2	6.3
1.2							6.9	7.1	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7	9.8
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3	10.4
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4	10.6
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4	10.6
14.0	0.5	0.8	1.1	1.8	2.7	4.1	6.1	8.5	10.3	10.6
20.0	0.7	0.7	1.2	1.9	2.7	4.0	5.8	8.0	9.9	10.6

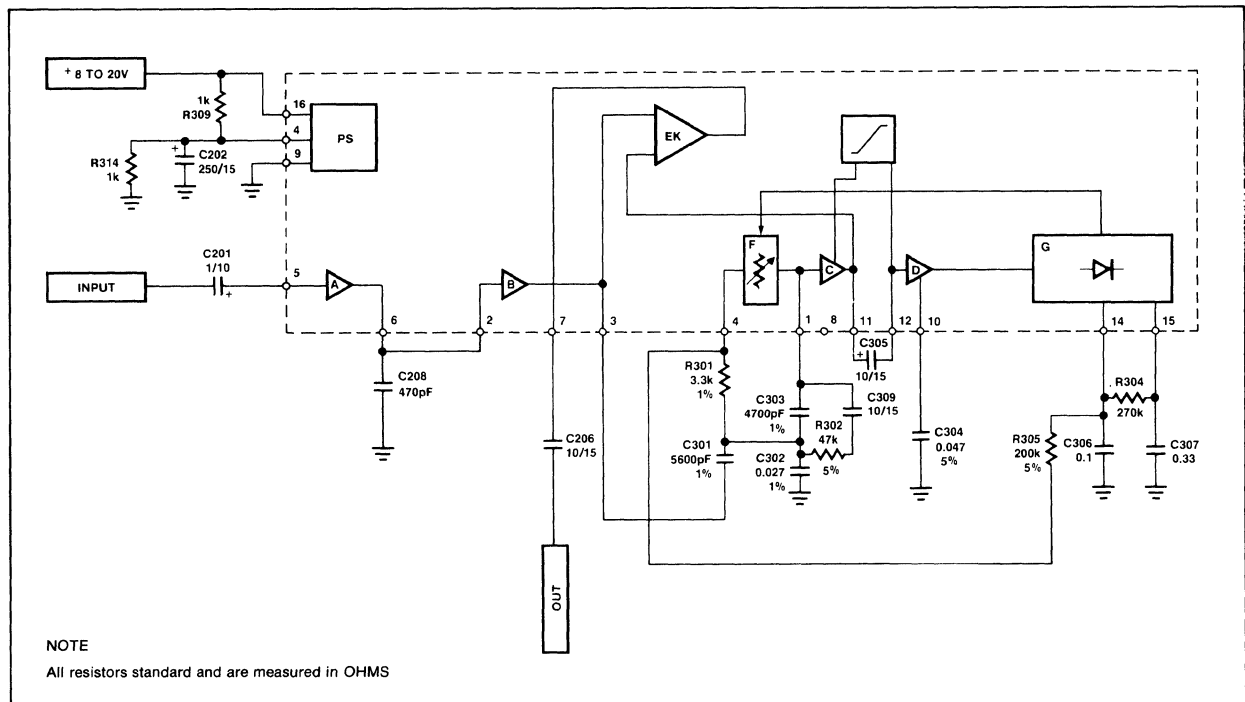
NOTE

The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must maintain in consumer B-Type circuitry. The figures can however be used to plot typical characteristics.

APPLICATION INFORMATION

The NE645B/646B is a direct replacement for the NE545B. For a $\pm 1\text{dB}$ back-to-back frequency response, the external components should be changed as shown in the test circuit. The critical component is R307 which should be shorted out. All other components, R303, R308, and C308 are now connected to empty pins. D301 will only effect the burst performance. C208 is only necessary in the test circuit in order to eliminate high frequency oscillation. In the actual application the 19kHz filter between pin 6 and 2 will perform the same high frequency roll off. All circuit parameters are guaranteed at 12V V_{CC} .

TEST CIRCUIT NE645B/646B

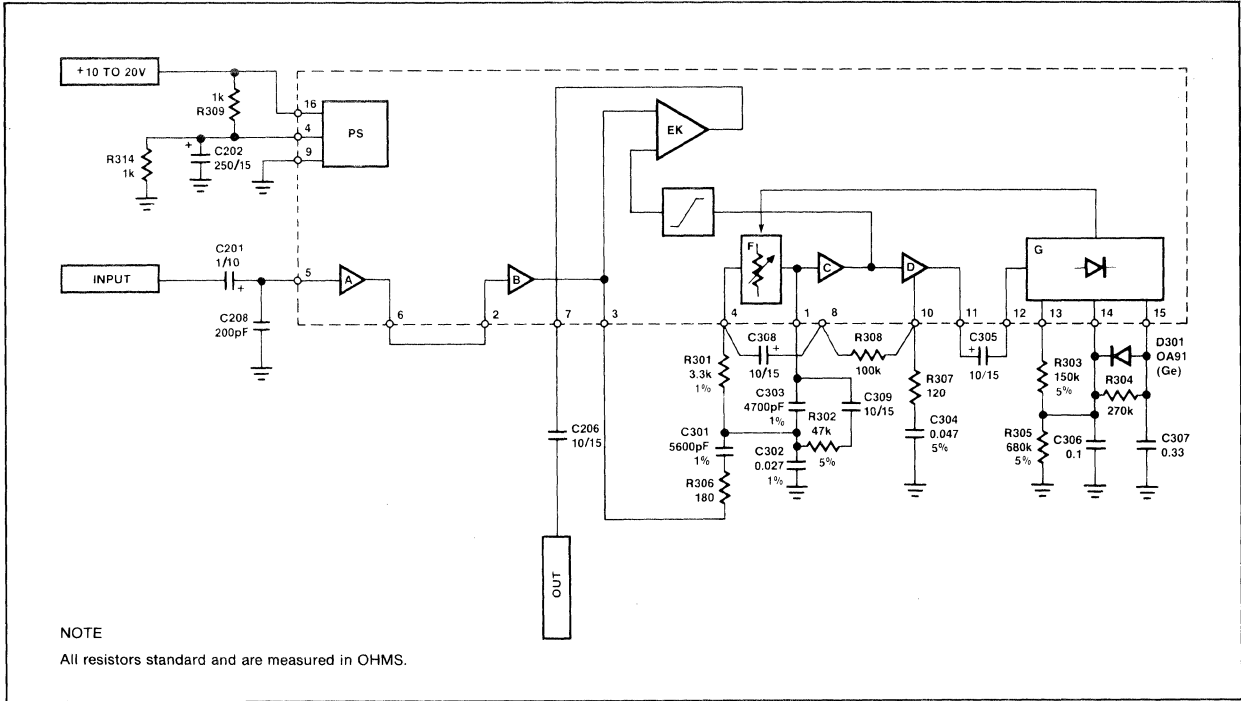


The following components have been eliminated from the NE545B test circuit: (over)
 R303, R306, R307, R308, C308, D301

Component changes:
 C208 is changed from 200pF to 470pF and is moved from pin 5 to pin 6/2
 R305 is changed from 680K to 200K and terminated at pin 4



TEST CIRCUIT NE545B



SECTION 14

PHASE LOCKED LOOPS

Section 14—PHASE LOCKED LOOPS

NE/SE564	Phase Locked Loop	436
NE/SE565	Phase Locked Loop	443
NE/SE566	Function Generator	448
NE/SE567	Tone Decoder/Phase Locked Loop	451

PHASE LOCKED LOOPS DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

FREE-RUNNING FREQUENCY (f_{o'}, ω_{o'}).

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_{o'} and ω_{o'} which are used for the general oscillator frequency. (Many references use f_{o'} and ω_{o'} for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f_{o'} and ω_{o'} are Hz and radians per second respectively.

LOCK RANGE (2f_L, 2ω_L).*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_{o'}. The deviations from f_{o'} are referred to as the *Tracking Range* or *Hold-in Range*. (See figure 1.6). The tracking range is therefore one-half of the lock range.

CAPTURE RANGE (2f_C, 2ω_C).**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The cap-

ture range also is centered at f_{o'} with the equal deviations called the *Lock-in* or *Pull-in Ranges*. The capture range can never exceed the lock range.

LOCK-UP TIME (t_L).**

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

PHASE COMPARATOR CONVERSION GAIN (K_D).

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_D is also a function of signal amplitude. K_D has units of volts per radian (V/rad).

VCO CONVERSION GAIN (K_O).

The conversion constant relating the oscillators frequency shift from f_{o'} to the applied input voltage. K_O has units of radians per second per volt (rad/sec/volt). K_O is a linear function of ω_{o'} and must be obtained using a formula or graph provided or experimentally measured at the desired ω_{o'}.

LOOP GAIN (K_V).

The product of K_D, K_O, and the low-pass filters gain at dc. K_D is evaluated at the appropriate input signal level and K_O at the appropriate ω_{o'}. K_V has units of (sec)⁻¹.

CLOSED LOOP GAIN (CLG).

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_V}{1 + K_V} \quad \text{(Equation 1.4)}$$

NATURAL FREQUENCY (ω_n).

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_{o'} and at which the phase error swing is the greatest.

DAMPING FACTOR (ζ).

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

LOOP NOISE BANDWIDTH (B_L).

A loop property relating ω_n and τ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

* Also called Synchronization Range.

** Also called Acquisition Range.

*** Also called Acquisition Time.

NOTE

Refer to Section 10 of the 1979 Analog Applications Manual for an in-depth explanation of Phase Locked Loops and their applications.

DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

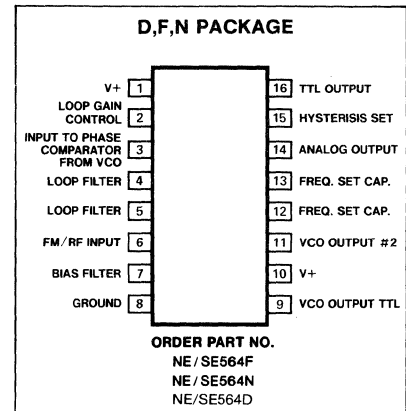
APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators

FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (Externally Controlled)

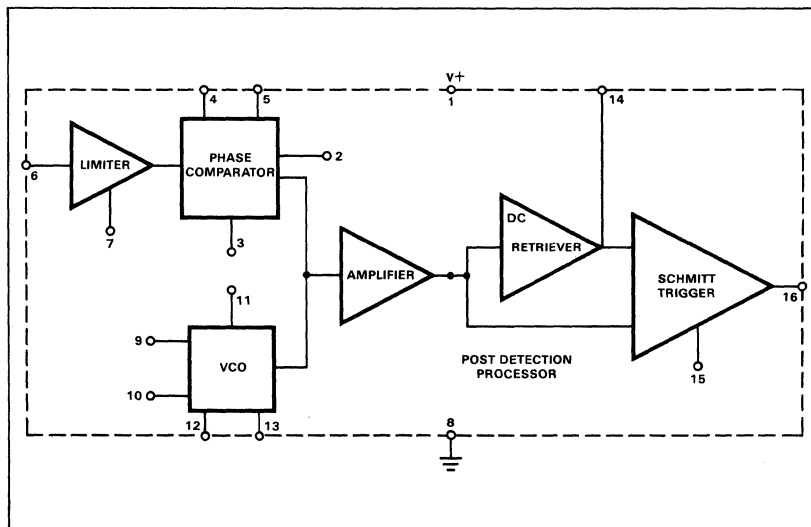
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V+	Supply voltage		V
	Pin 1	14	
P _D	Power dissipation	400	mW
	Pin 10	6	
T _A	Operating temperature	NE	0 to 70 °C
	Operating temperature	SE	-55 to +125 °C
t _{stg}	Storage temperature	-65 to 150	°C

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \quad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
 f_{in} = frequency of the input signal
 f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is

ELECTRICAL CHARACTERISTICS $V+ = 5V, T_A = 25^\circ C, f_o = 5MHz, I_B = -200\mu A$ unless otherwise specified.
Test Circuit: Figure 1

PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency		50	65		45	60		MHz
Lock range	Input $\geq 200mV_{rms}$, $T_A = 25^\circ C$ = $125^\circ C$ = $-55^\circ C$ = $0^\circ C$ = $70^\circ C$	60 30 120	90 50 150		60 100 50	90 120 70		% of f_o
Capture range	Input $\geq 200mV_{rms}$, $R_2 = 27\Omega$ = 100Ω	25 35	35 50		25 35	35 50		% of f_o
VCO frequency drift with temperature	$f_o = 5MHz, T_A = -55^\circ C$ to $125^\circ C$ = $0^\circ C$ to $70^\circ C$ $f_o = 500kHz, T_A = -55^\circ C$ to $125^\circ C$ = $0^\circ C$ to $70^\circ C$		400 250	1000 500		400 400	1250 850	PPM/ $^\circ C$
VCO frequency change with supply voltage Demodulated output voltage	$V+ = 4.5V$ to $5.5V$ Modulation frequency: 1kHz, $f_o = 5MHz$ Input deviation: 10%, $T = 25^\circ C$ 1%, $T = 25^\circ C$ $T = 0^\circ C$ = $-55^\circ C$ = $70^\circ C$ = $125^\circ C$		3 120 10 8 14	6 140 14 12 16		3 120 10 9 13 15	6 140 14 13 15	% of f_o mVrms mVrms mVrms mVrms mVrms
Linearity	Deviation: 1% to 8%		1	3		1	3	%
Signal to noise ratio AM rejection			40 35			40 35		dB dB
Supply current Leakage current Output current	$V+ = 5V$ Pin 9 Pin 9		35 1	50 10 6		35 1 6	50 10 6	mA μA mA
Supply voltage	Pin 1 Pin 10	4.5 4.5		12 5.5	4.5 4.5		12 5.5	V V

accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equi-

valent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25}-Q_{26}$ form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{16R_C C_1} \quad \text{Equation 2}$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
 C_1 = external frequency setting capacitor

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_B with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier

to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier $Q_{42}-Q_{43}$ together with an external capacitor which is connected at the am-



plifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_0 = \frac{g_m}{C_2} \int V_{in} dt \quad \text{Equation 3}$$

- g_m = transconductance of the amplifier
- C_2 = capacitor at the output (pin 14)
- V_{in} = signal voltage at amplifier input

With proper selection of C_2 , the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q49-Q50 with positive feedback being provided by Q47-Q48. The hysteresis is varied by changing the current in Q52 with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_0 = \frac{1}{16R_C C_1} \text{ in Hz} \quad \text{Equation 4}$$

- $R_C = 100\Omega$
- $C_1 = \text{external cap in farads}$

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \quad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function

$$\text{at } \omega = \frac{1}{RC_3}$$

FM DEMODULATOR

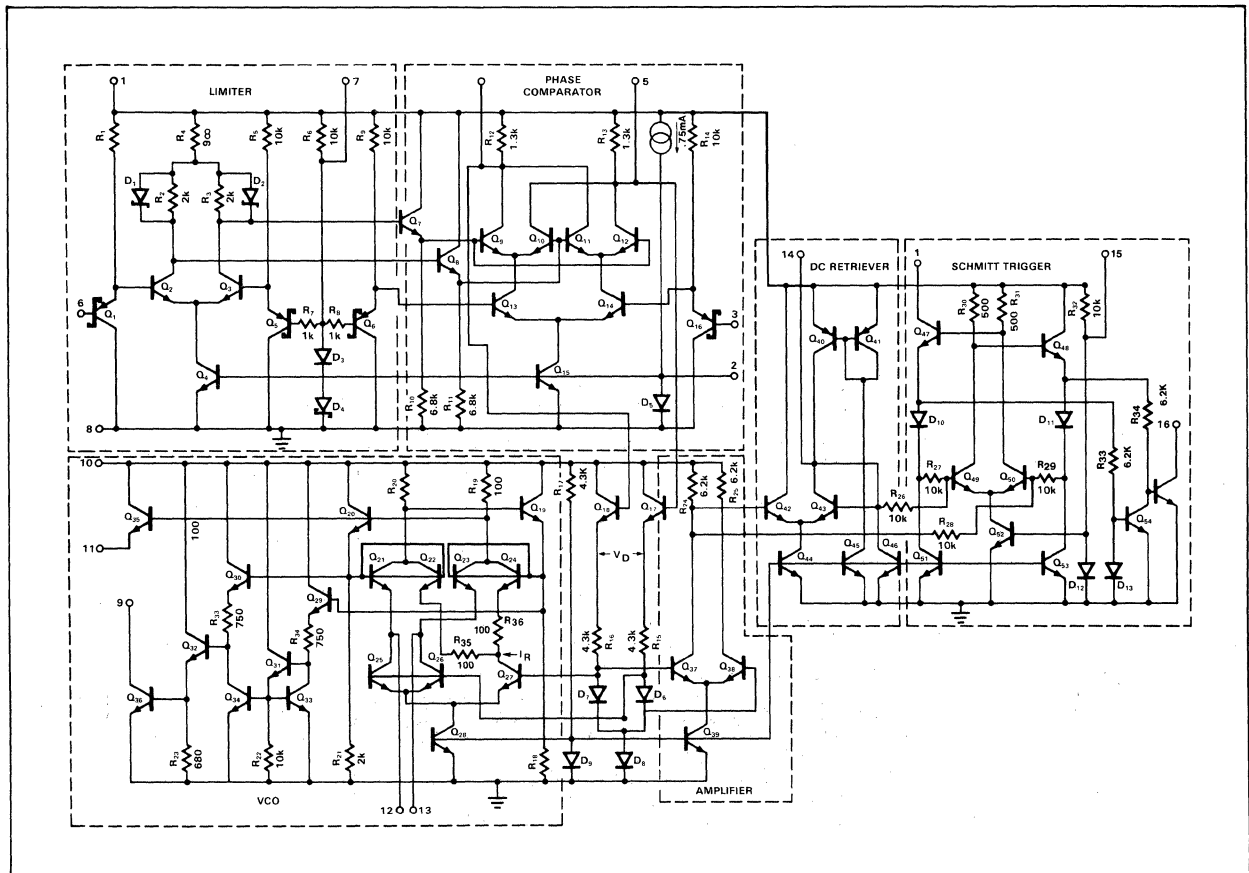
The NE564 can be used as an FM demodulator. The connections for operation

at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

EQUIVALENT SCHEMATIC



FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 6 shows a high-frequency FSK decoder designed for input frequency deviations of $\pm 1.0\text{MHz}$ centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_o' to 10.8MHz.

Figure 9 indicates that the $\pm 1.0\text{MHz}$ frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_o' frequencies.

The hysteresis was adjusted experimentally via the 10k Ω potentiometer and 2k Ω bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

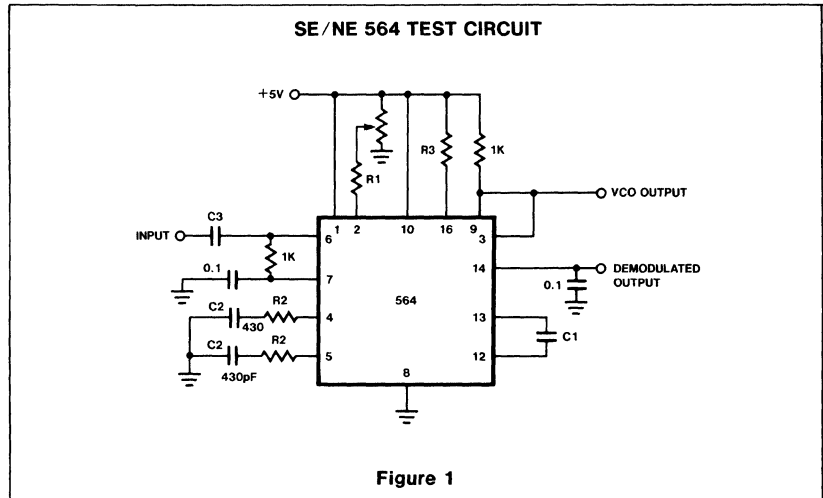


Figure 1

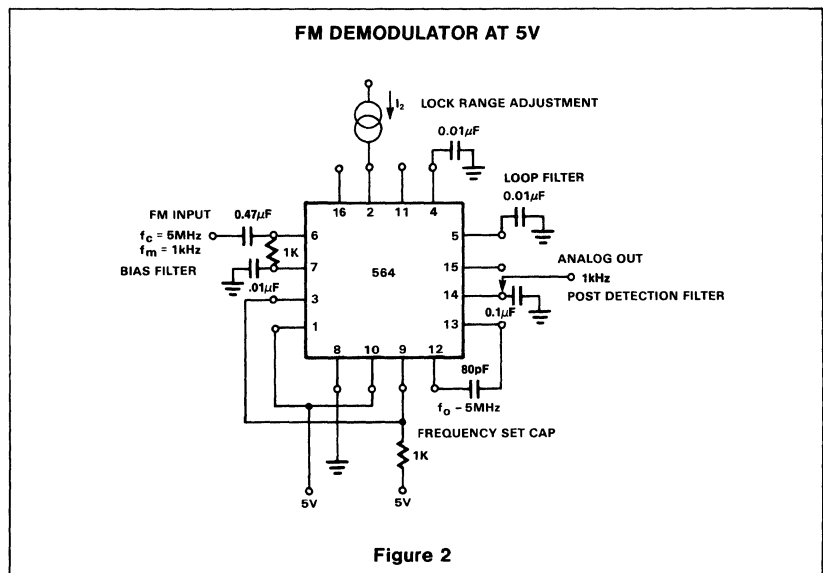
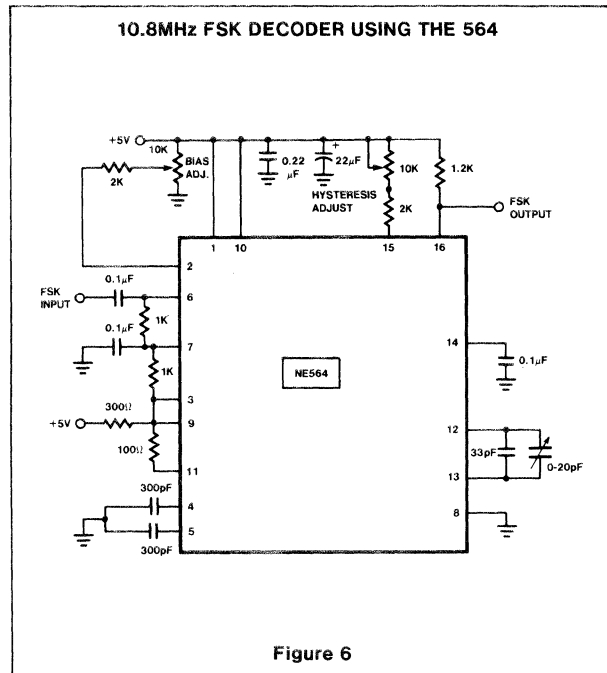
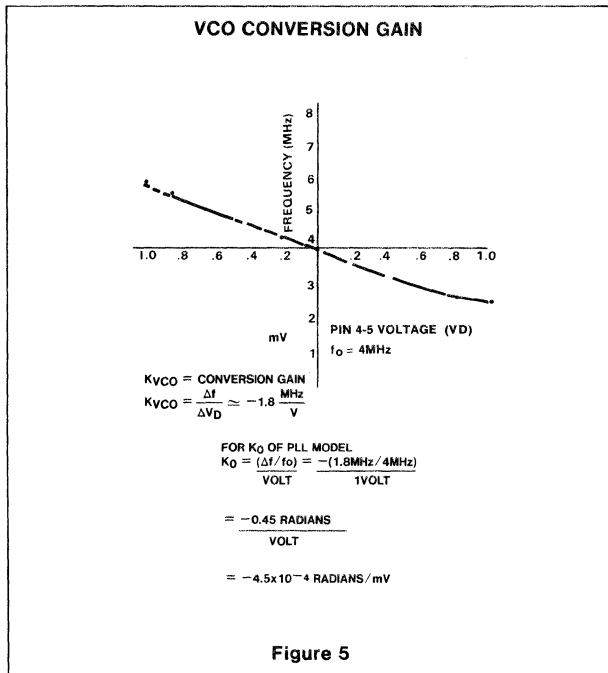
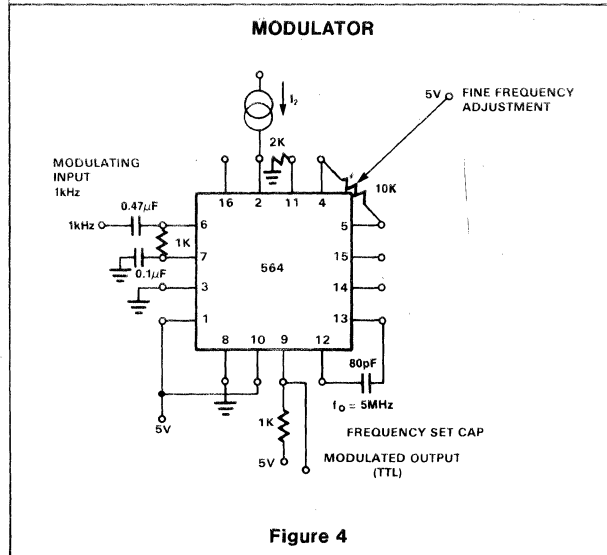
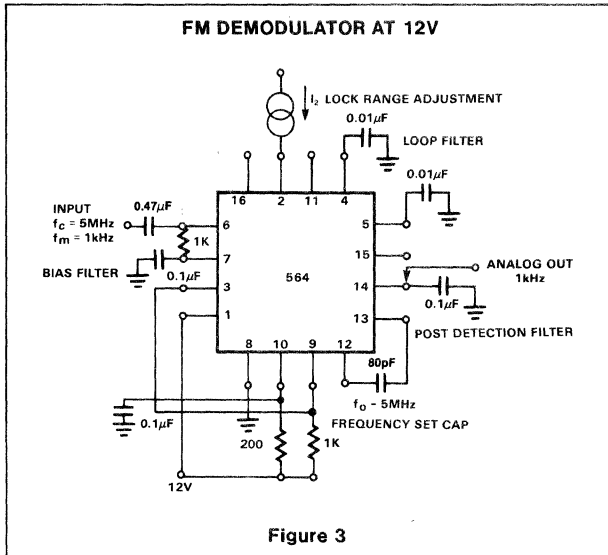
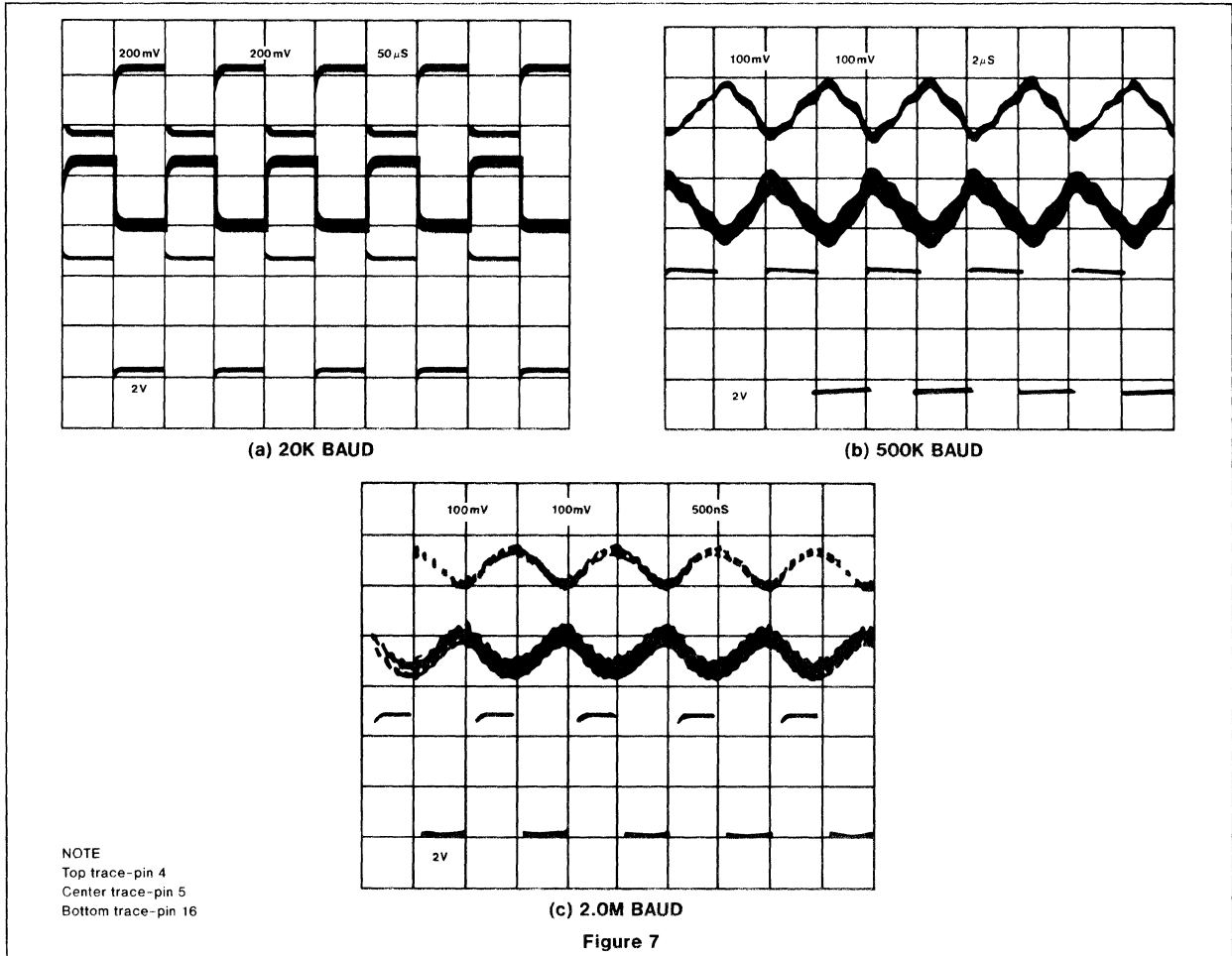


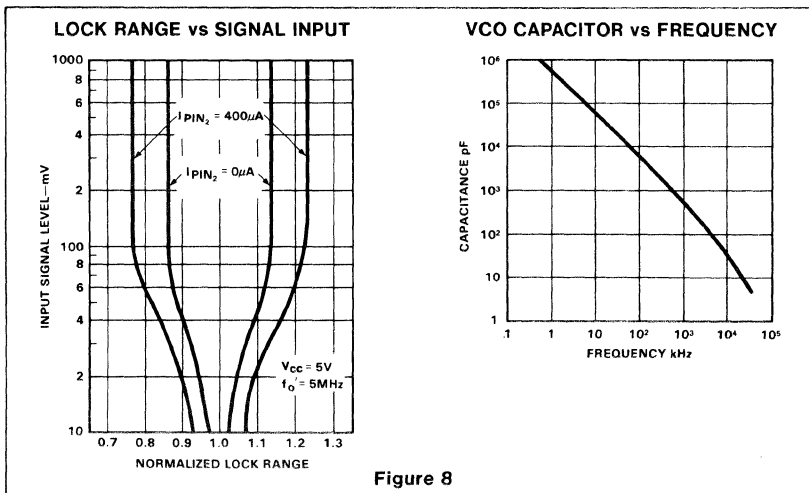
Figure 2



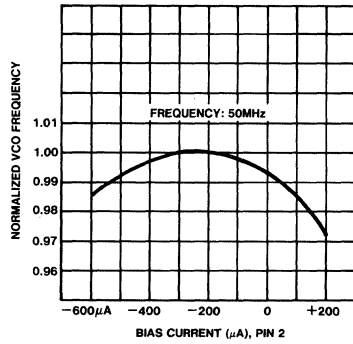
PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



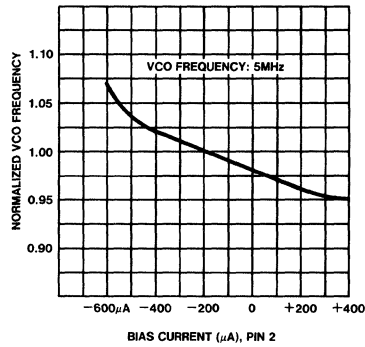
TYPICAL PERFORMANCE CHARACTERISTICS



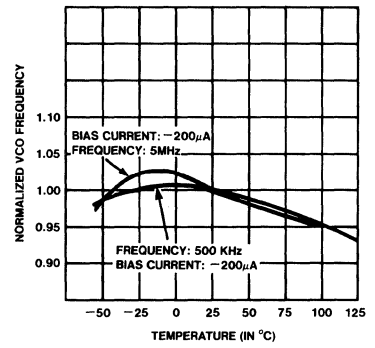
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

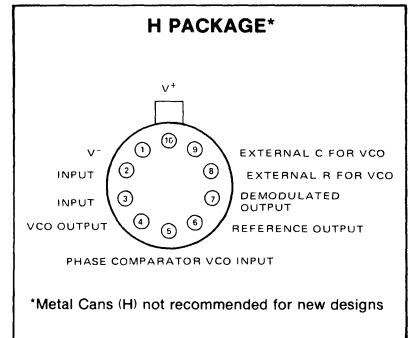
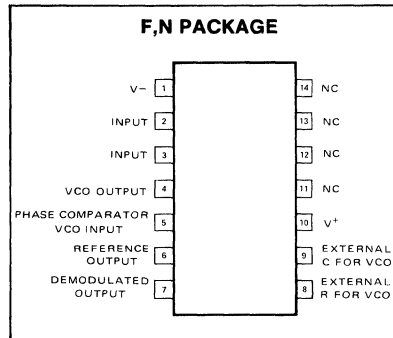
FEATURES

- Highly stable center frequency (200ppm/°C typ.)
- Wide operating voltage range (± 6 to ± 12 volts)
- Highly linear demodulated output (0.2% typ.)
- Center frequency programming by means of a resistor or capacitor, voltage or current
- TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from $< \pm 1\%$ to $> \pm 60\%$
- Frequency adjustable over 10 to 1 range with same capacitor

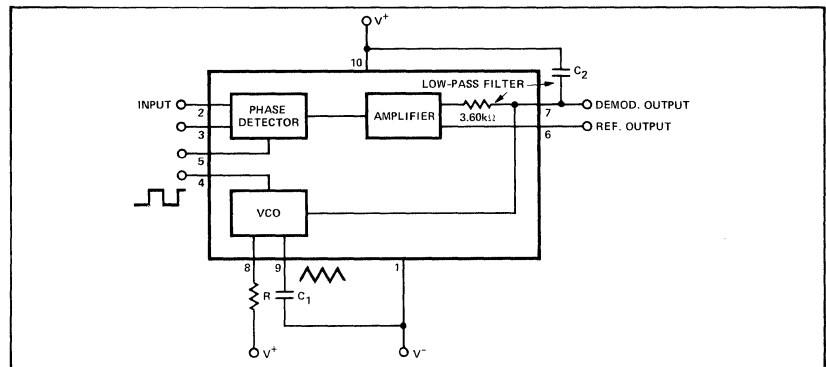
APPLICATIONS

- Frequency shift keying
- Modems
- Telemetry receivers
- Tone decoders
- SCA receivers
- Wideband FM discriminators
- Data synchronizers
- Tracking filters
- Signal restoration
- Frequency multiplication & division

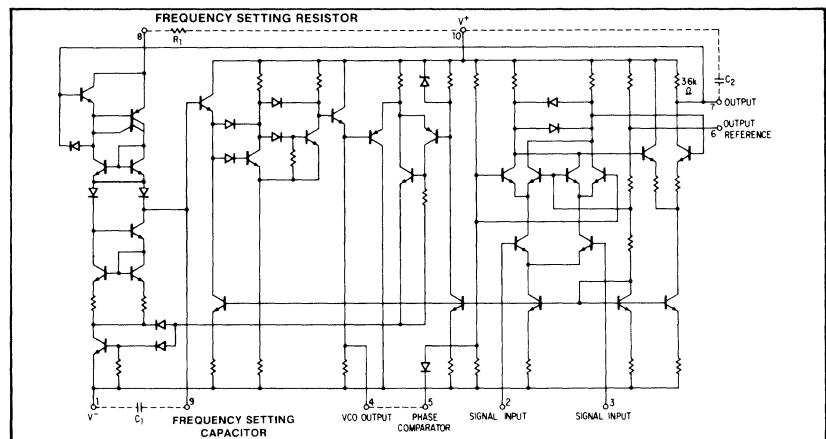
PIN CONFIGURATIONS



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	Vp-p
Storage temperature	-65 to +150	°C
Operating temperature range		
NE565	0 to +70	°C
SE565	-55 to +125	°C
Power dissipation	300	mW



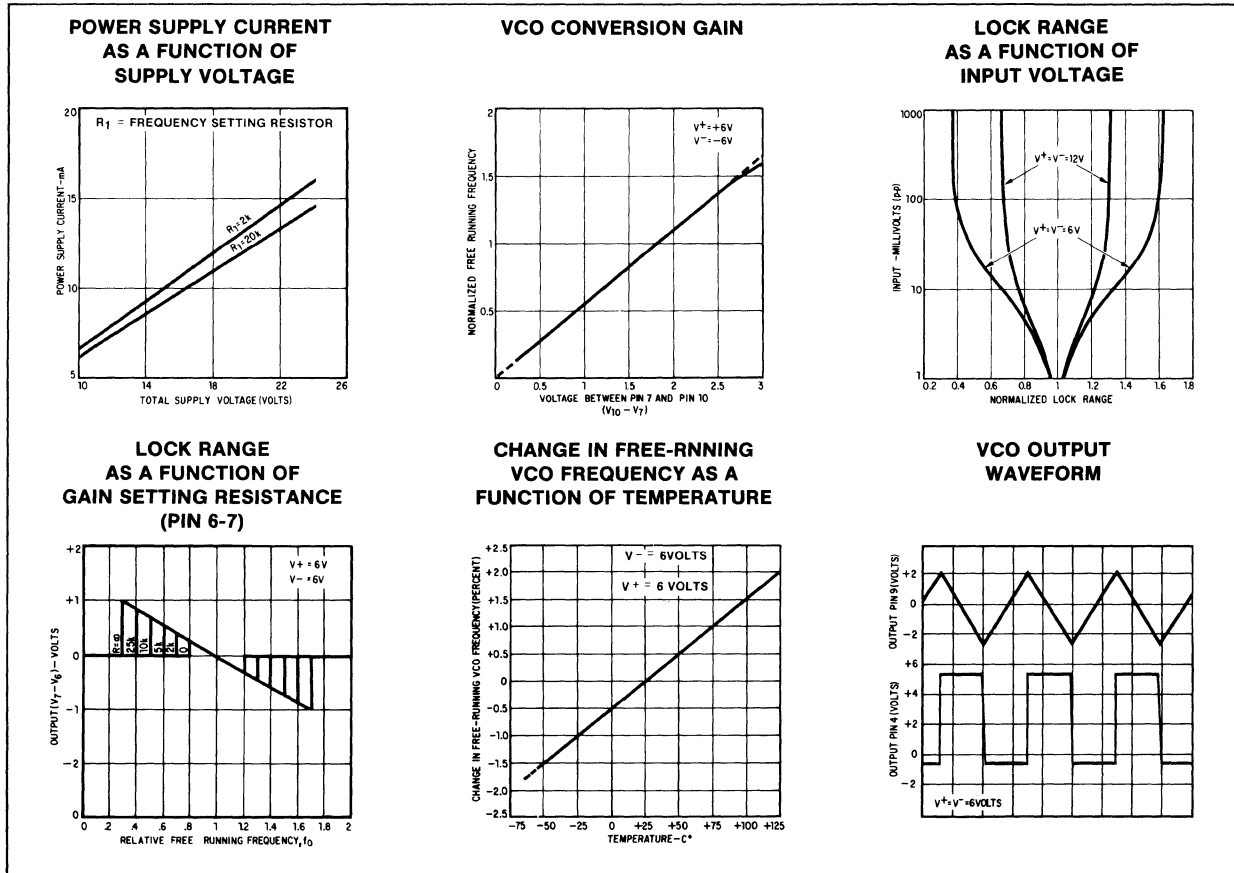
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 6\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS								
Supply voltage		12		± 12	± 6			V
Supply current			8	12.5		8	± 12 12.5	mA
INPUT CHARACTERISTICS								
Input impedance ¹	$f_o = 50\text{kHz}$, $\pm 10\%$ frequency deviation	7	10		5	10		k Ω
Input level required for tracking		10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center frequency	$C_1 = 2.7\text{pF}$ Distribution taken about $f_o = 50\text{kHz}$, $R_1 = 5.0\text{k}\Omega$, $C_1 = 1200\text{pF}$	300	500			500		kHz
Maximum value								
Distribution ²		-10	0	+10	-30	0	+30	%
Drift with temperature	$f_o = 50\text{kHz}$		200			300		ppm/ $^\circ\text{C}$
Drift with supply voltage	$f_o = 50\text{kHz}$, $V_{CC} = \pm 6$ to ± 7 volts		0.1	1.0		0.2	1.5	%/V
Triangle wave								
Output voltage level		1.9	0		1.9	0		V
Amplitude			2.4	3		2.4	3	Vp-p
Linearity			0.2			0.5		%
Square wave								
Logical "1" output voltage	$f_o = 50\text{kHz}$	+4.9	+5.2		+4.9	+5.2		V
Logical "0" output voltage	$f_o = 50\text{kHz}$		-0.2	+0.2		-0.2	+0.2	V
Duty cycle	$f_o = 50\text{kHz}$	45	50	55	40	50	60	%
Rise time			20	100		20		ns
Fall time			50	200		50		ns
Output current (sink)		0.6	1		0.6	1		mA
Output current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output voltage level	Measured at pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum voltage swing ³	$\pm 10\%$ frequency deviation		2			2		Vp-p
Output voltage swing		250	300		200	300		mVp-p
Total harmonic distortion			0.2	0.75		0.4	1.5	%
Output impedance ⁴				3.6		3.6		k Ω
Offset voltage (V6-V7)			30	100		50	200	mV
Offset voltage vs temperature (drift)			50			100		$\mu\text{V}/^\circ\text{C}$
AM rejection		30	40			40		dB

NOTES

- Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
- The external resistance for frequency adjustment (R1) must have a value between 2k Ω and 20k Ω .
- Output voltage swings negative as input frequency increases.
- Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO: $f_0 \approx \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm \frac{8f_0}{V_{CC}}$ in Hz

Capture-range: $f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically $\pm 60\%$) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_0 = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C₁ can be any value, but R₁ should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be

decreased with little change in the free-running frequency. In this manner the lock range can be decreased from $\pm 60\%$ of f_0 to approximately $\pm 20\%$ of f_0 (at $\pm 6V$).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C₂, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

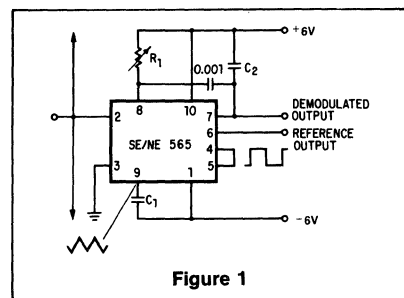


Figure 1



Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with $f_{IN} = 1070\text{Hz}$.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be

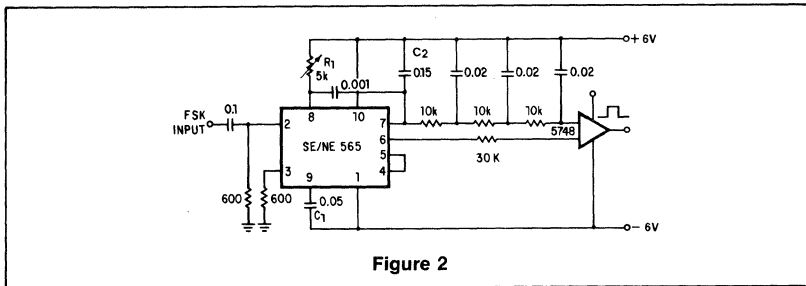


Figure 2

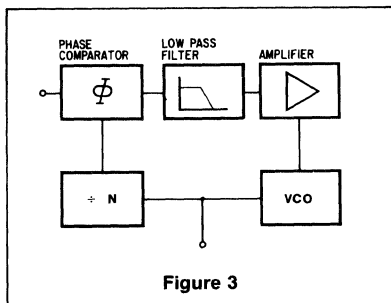


Figure 3

a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so

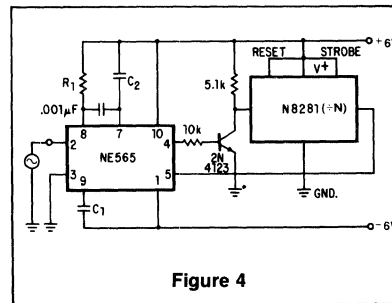


Figure 4

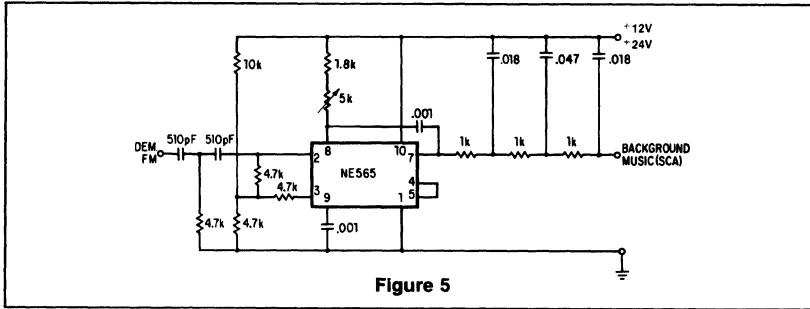
as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.



DESCRIPTION

The NE/SE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

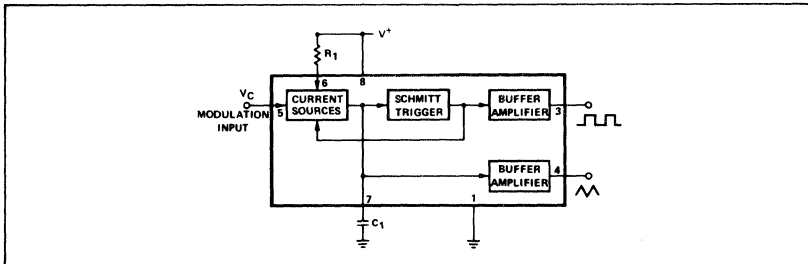
FEATURES

- Wide range of operating voltage (up to 24 volts)
- High linearity of modulation
- Highly stable center frequency (200 ppm/°C typical)
- Highly linear triangle wave output
- Frequency programming by means of a resistor or capacitor, voltage or current
- Frequency adjustable over 10 to 1 range with same capacitor

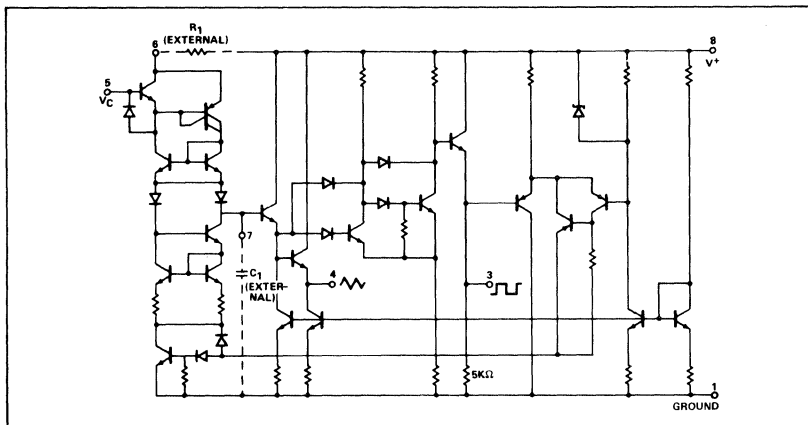
APPLICATIONS

- Tone generators
- Frequency shift keying
- FM modulators
- Clock generators
- Signal generators
- Function generators

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V _{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

PIN CONFIGURATIONS

H PACKAGE*

ORDER PART NO. NE/SE566H

*Metal cans (H) not recommended for new designs

N PACKAGE

ORDER PART NO. NE/SE566N

F PACKAGE

ORDER PART NO. NE/SE566F

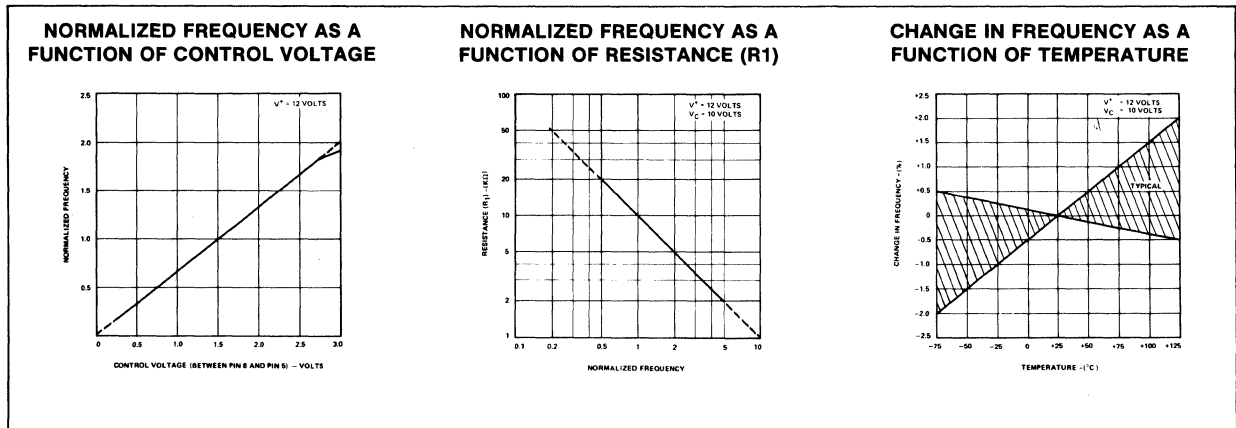
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$; $V_{CC} = 12\text{V}$ unless otherwise specified.

PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	$^\circ\text{C}$
Operating supply voltage			24			24	V
Operating supply current		7	12.5		7	12.5	mA
VCO¹							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/ $^\circ\text{C}$
Frequency drift with supply voltage		1			2		%/V
Control terminal input impedance ²		1			1		M Ω
FM distortion ($\pm 10\%$ deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		V _{pp}
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		V _{pp}
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

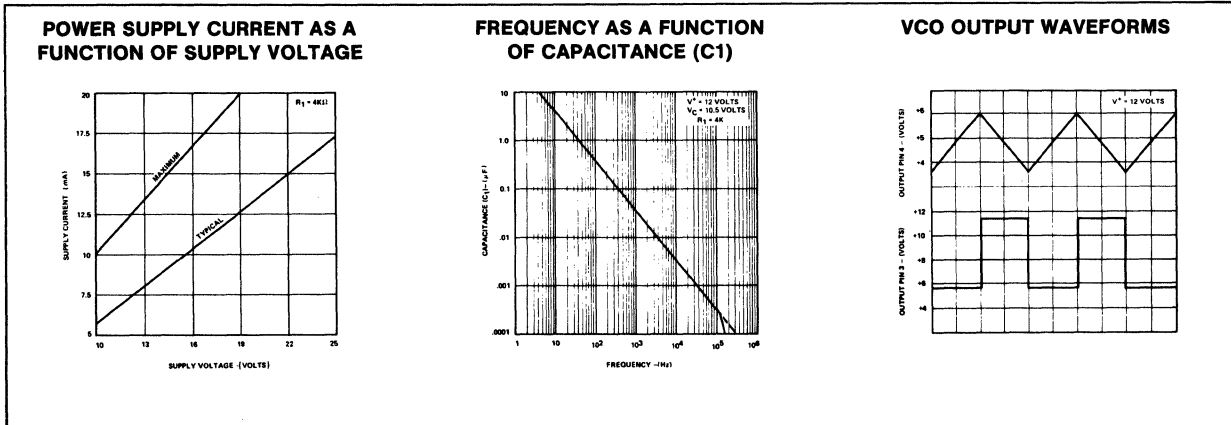
NOTES

- The external resistance for frequency adjustment (R_1) must have a value between 2k Ω and 20k Ω .
- The bias voltage (V_C) applied to the control terminal (pin 5) should be in the range $3/4V^+ \leq V_C \leq V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (Vc) in the range

$$3/4 V^+ \leq V_C \leq V^+$$

where Vcc is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R2 and R3. The modulating signal is then ac coupled with

the capacitor C2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

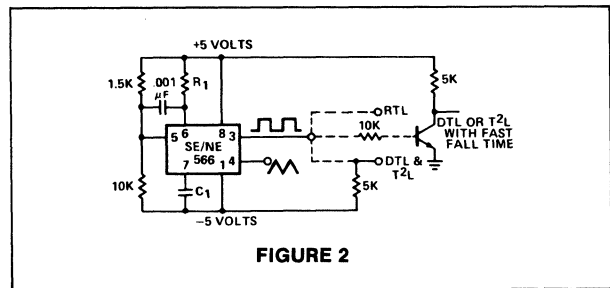
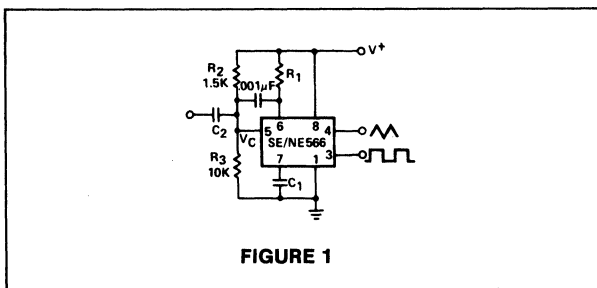
$$f_o \approx \frac{2[(V^+) - (V_C)]}{R_1 C_1 V^+}$$

and R1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically 0.001μf) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard

logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T2L gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T2L circuitry which requires a fast fall time (<50ns) and a large current sinking capability.



DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

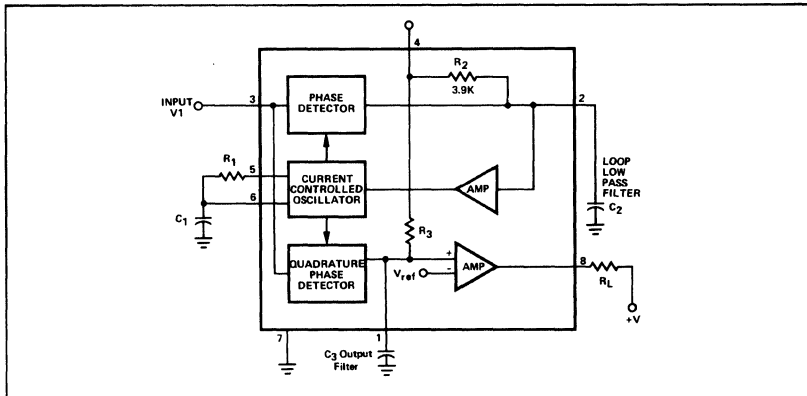
FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14 percent)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20 to 1 range with an external resistor
- Military processing available

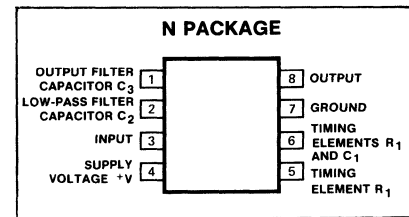
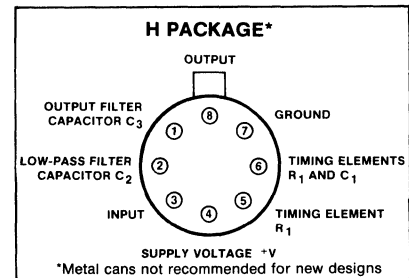
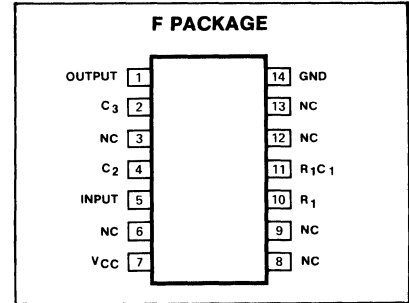
APPLICATIONS

- Touch Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

BLOCK DIAGRAM



PIN CONFIGURATIONS

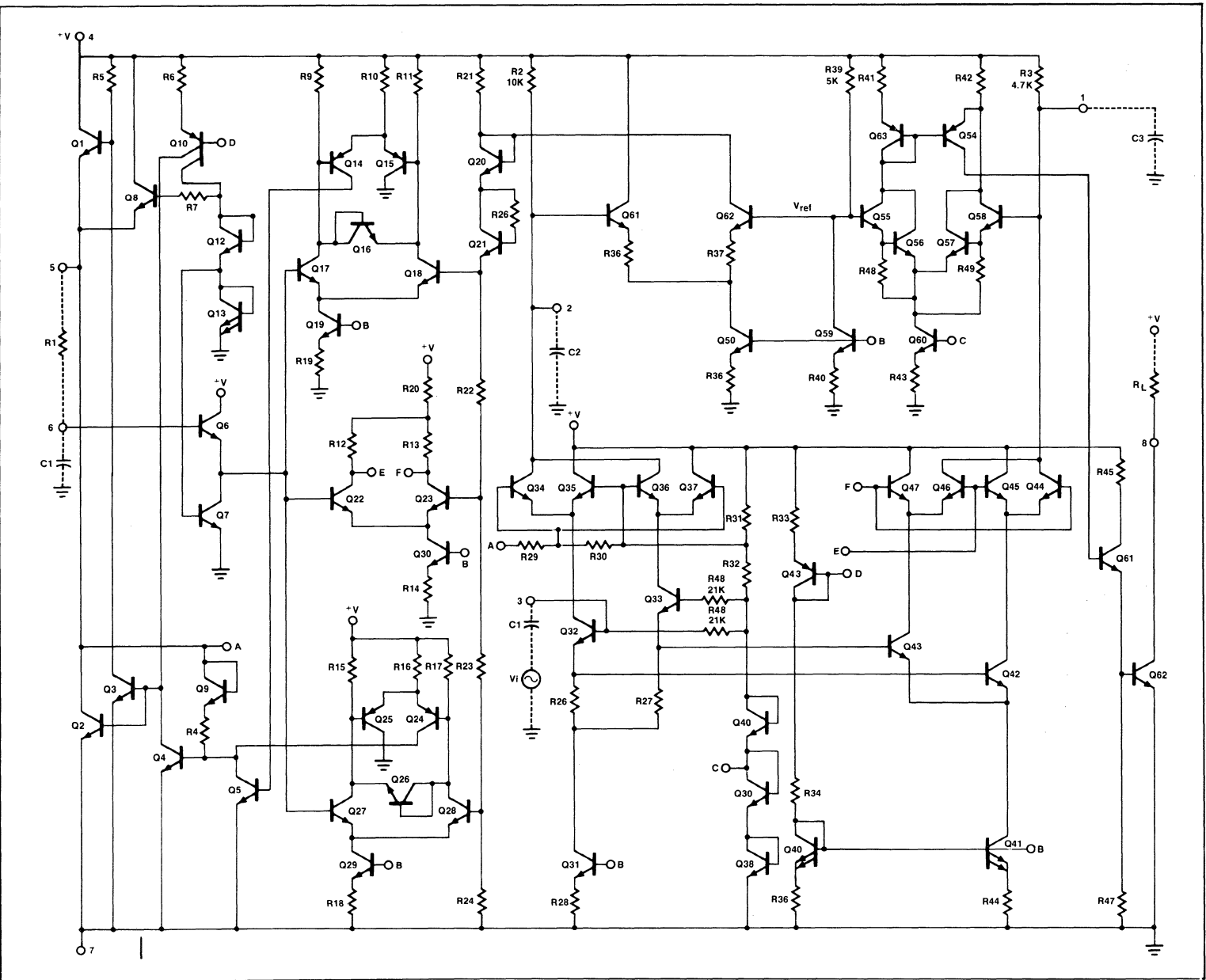


ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + Vs	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

EQUIVALENT SCHEMATIC

NE/SE567-F.N.H



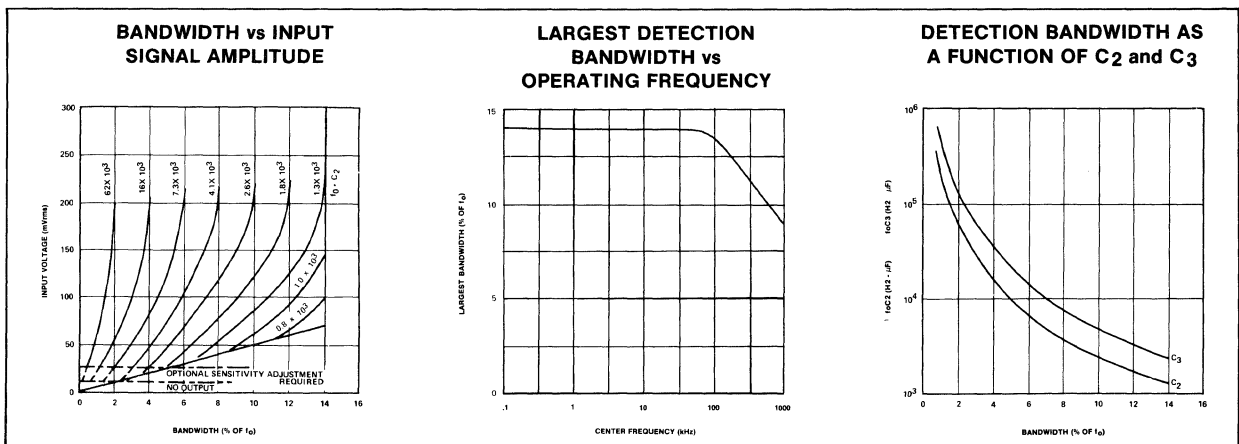
DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; T_A = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY ¹ Highest center frequency (f _o)		100	500		100	500		kHz
Center frequency stability ²	-55 to +125°C		35±140			35±140		ppm/°C
	0 to +70°C		35±60			35±60		ppm/°C
Center frequency shift with supply voltage	f _o = 100kHz		0.5	1		0.7	2	%/V
DETECTION BANDWIDTH Largest detection bandwidth	f _o = 100kHz	12	14	16	10	14	18	% of f _o
Largest detection bandwidth skew	V _i = 300mVrms		2	4		3	6	% of f _o
Largest detection bandwidth— variation with temperature			±0.1			±0.1		%/°C
Largest detection bandwidth— variation with supply voltage	V _i = 300mVrms		±2			±2		%/V
INPUT Input resistance			20			20		kΩ
Smallest detectable input voltage (V _i)	I _L = 100mA, f _i = f _o		20	25		20	25	mVrms
Largest no-output input voltage	I _L = 100mA, f _i = f _o	10	15		10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6			+6		dB
Minimum input signal to wideband noise ratio	B _n = 140kHz		-6			-6		dB
OUTPUT Fastest on-off cycling rate			f _o /20			f _o /20		
"1" output leakage current	I _L = 30mA		0.01	25		0.01	25	μA
"0" output voltage	I _L = 100mA		0.2	0.4		0.2	0.4	V
	R _L = 50Ω		0.6	1.0		0.6	1.0	V
Output fall time ³	R _L = 50Ω		30			30		ns
Output rise time ³			150			150		ns
GENERAL Operating voltage range		4.75		9.0	4.75		9.0	V
Supply current quiescent			6	8		7	10	mA
Supply current—activated	R _L = 20kΩ		11	13		12	15	mA
Quiescent power dissipation			30			35		mW

NOTES

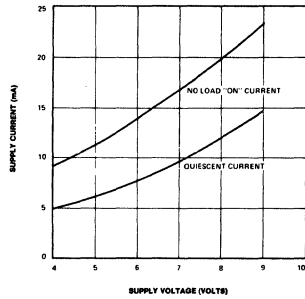
1. Frequency determining resistor R₁ should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL PERFORMANCE CHARACTERISTICS

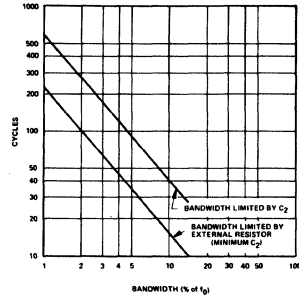


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

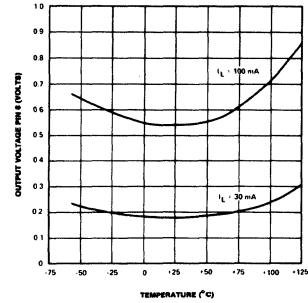
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE



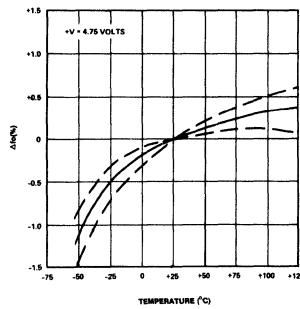
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



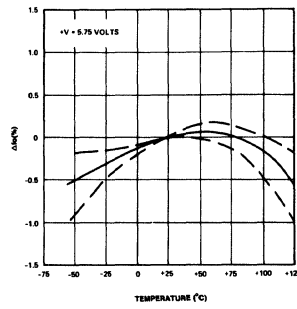
TYPICAL OUTPUT VOLTAGE vs TEMPERATURE



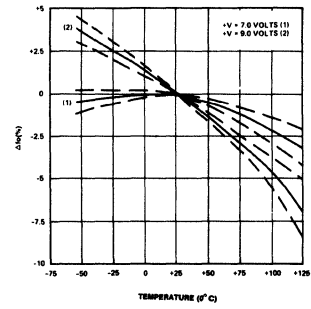
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



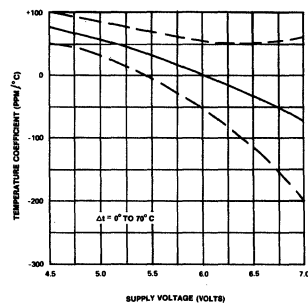
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



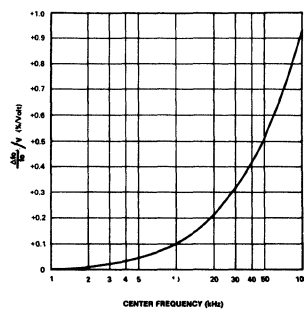
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



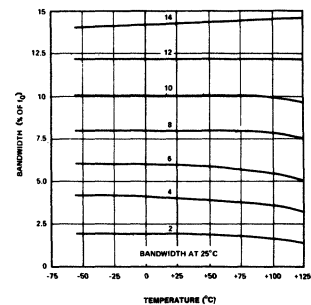
CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)



CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY



TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



DESIGN FORMULAS

$$f_0 \approx \frac{1.1}{R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_1}{f_0 C_2}} \text{ in \% of } f_0, V_1 \leq 200\text{mVrms}$$

Where

V_1 = Input Voltage (Vrms)
 C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_0 , within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

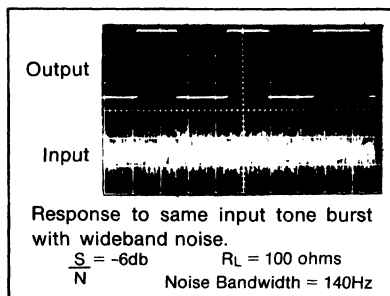
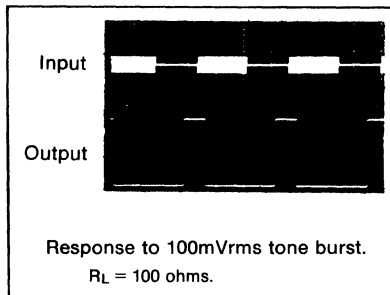
A measure of how well the detection band is centered about the center frequency, f_0 . The skew is defined as $(f_{\text{max}} + f_{\text{min}} - 2f_0)/2f_0$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1 , C_1 , C_2 and C_3 .

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the $R_1 C_1$ product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low pass capacitor, C_2 , by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of $f_0 C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, con-

TYPICAL RESPONSE



stant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the $f_0 C_2$ product (f_0 (Hz), C_2 (μfd)).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave

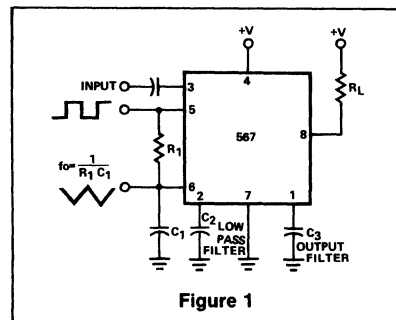


Figure 1

output of magnitude $(+V - 2V_{be}) \approx (+V - 1.4V)$ having a dc average of $+V/2$. A 1k Ω load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of $+V/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.
2. The 567 will lock onto signals near $(2n + 1) f_0$, and will give an output for signals near $(4n + 1) f_0$ where $n = 0, 1, 2$, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01 μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o} \mu F$$

$$C_3 = \frac{260}{f_o} \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is

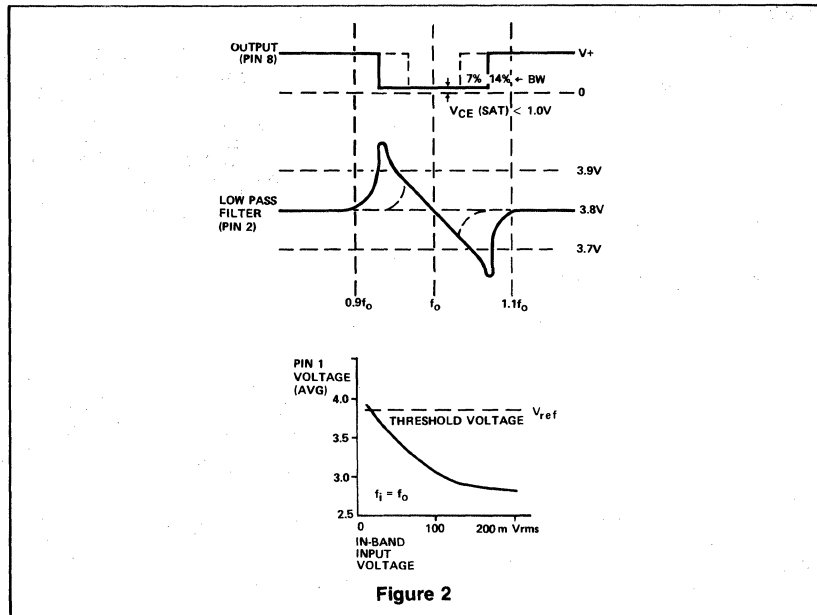


Figure 2

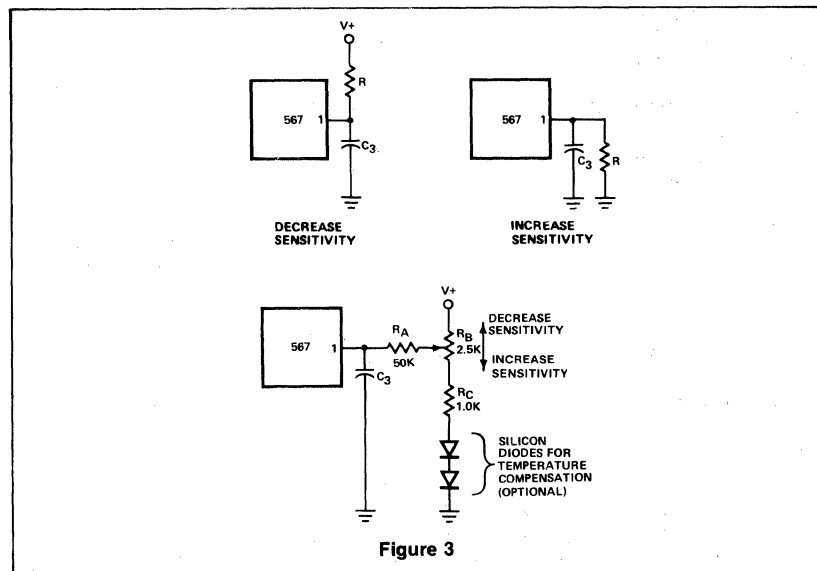


Figure 3

taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same

temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current from terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the

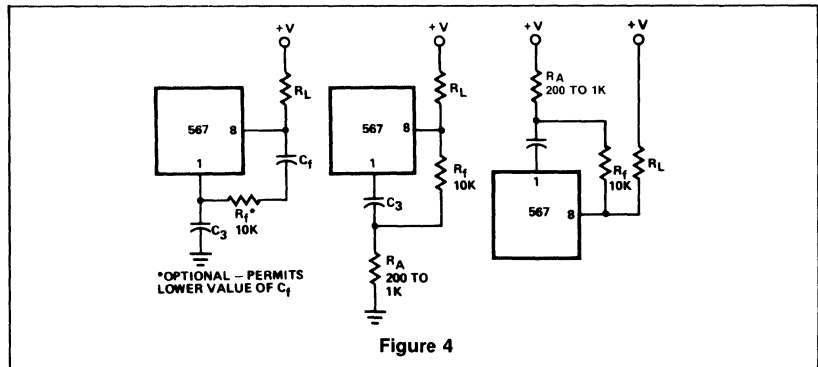


Figure 4

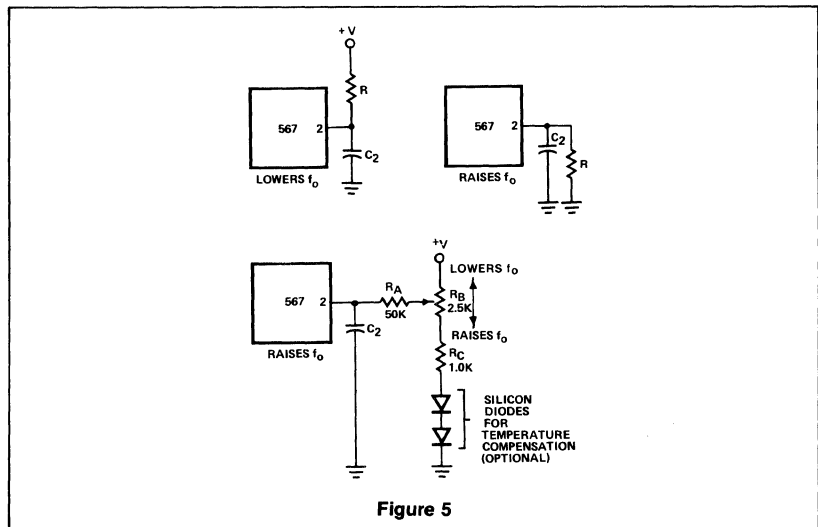


Figure 5

circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger

value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

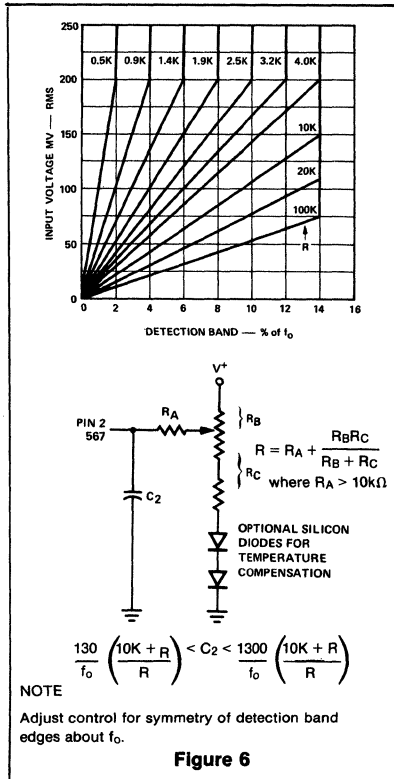
REDUCTION OF C_1 VALUE

(Figure 8)

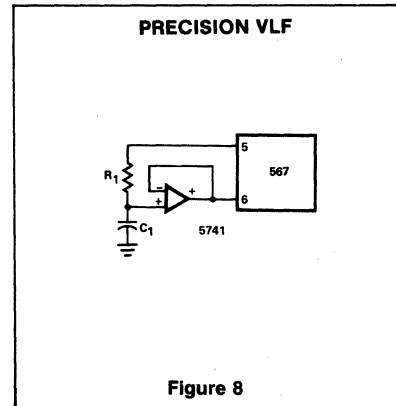
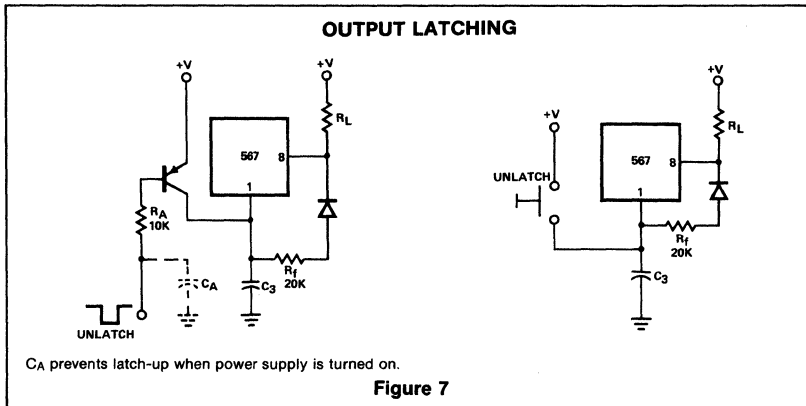
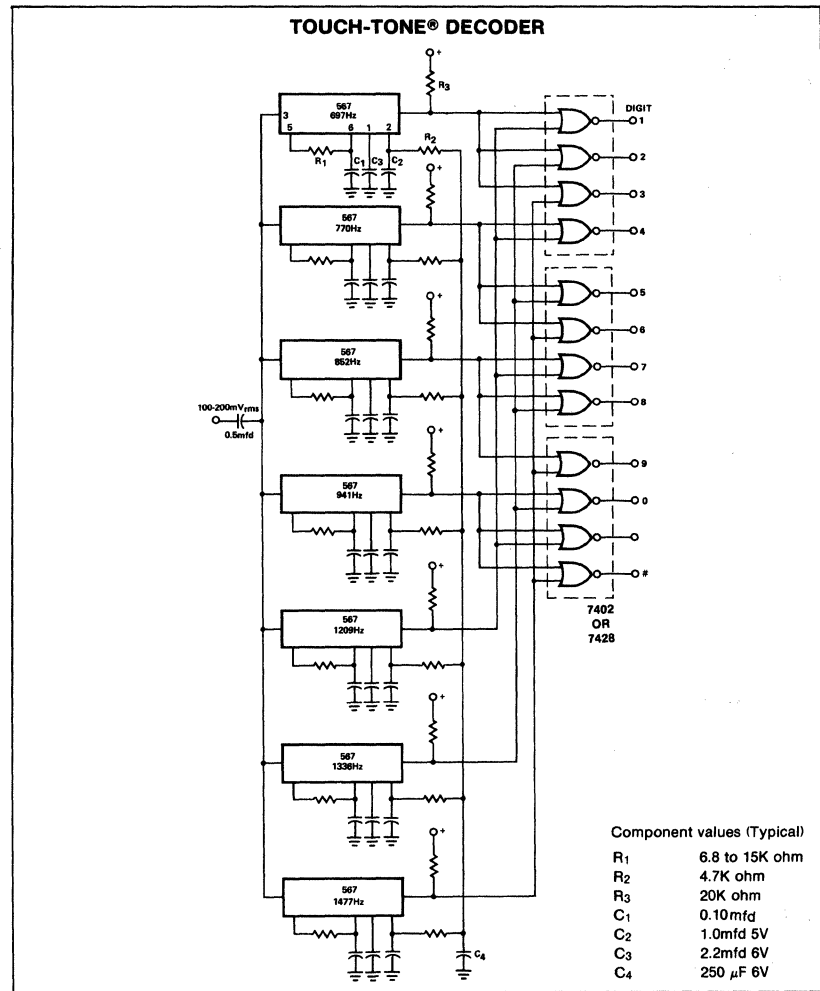
For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

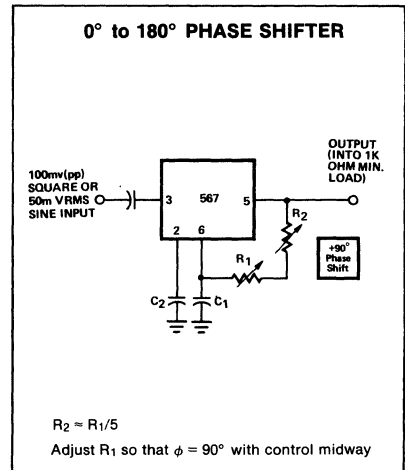
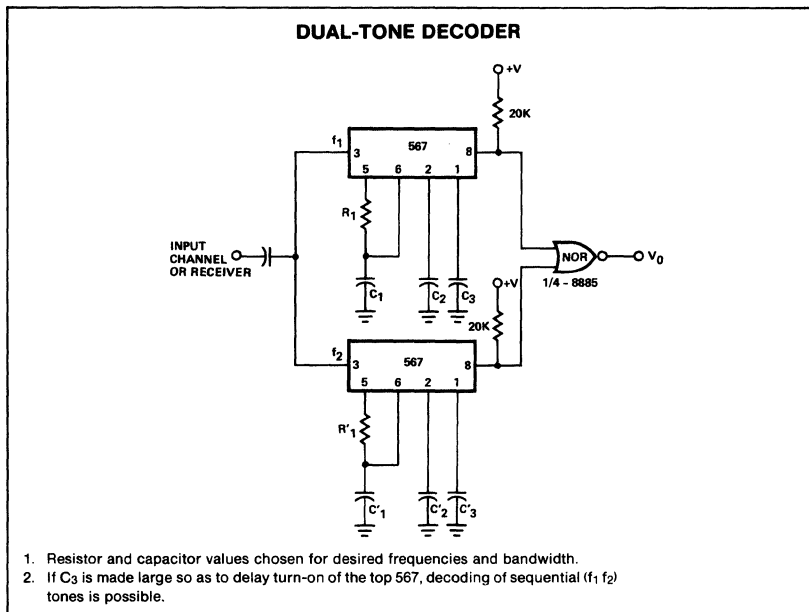
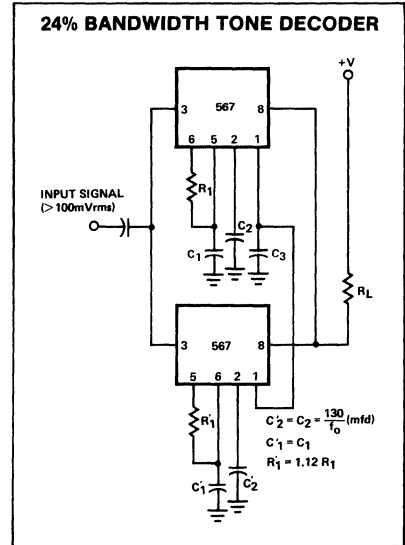
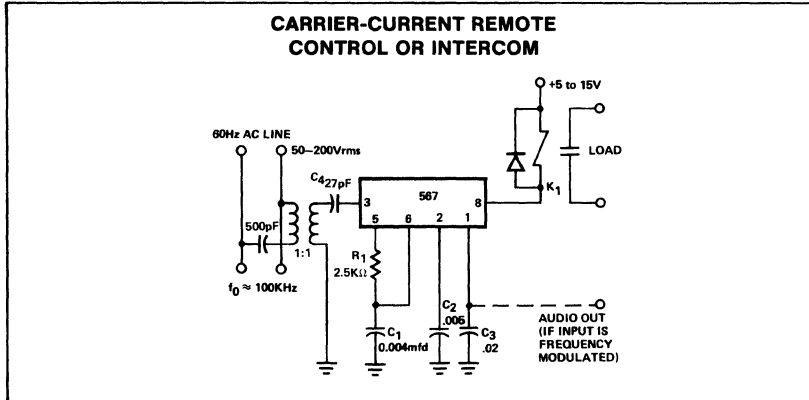
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.



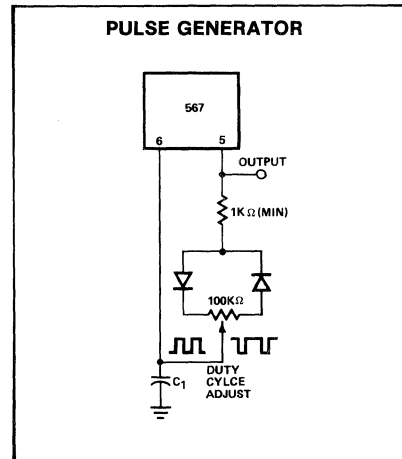
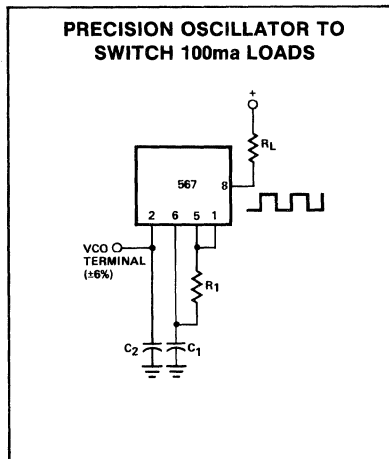
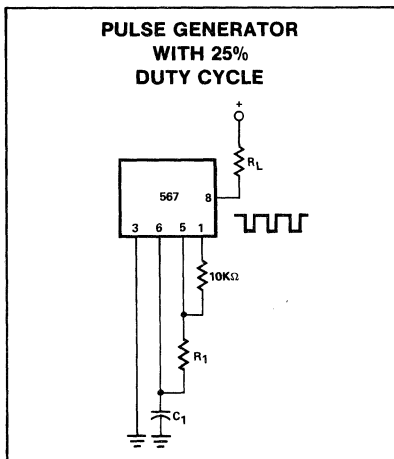
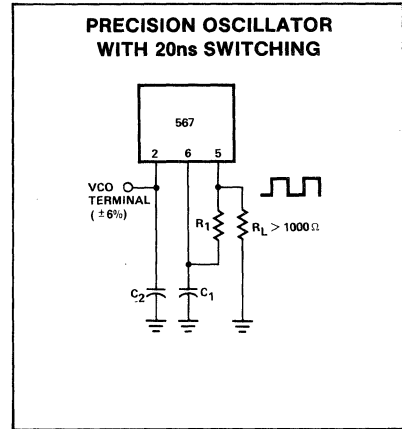
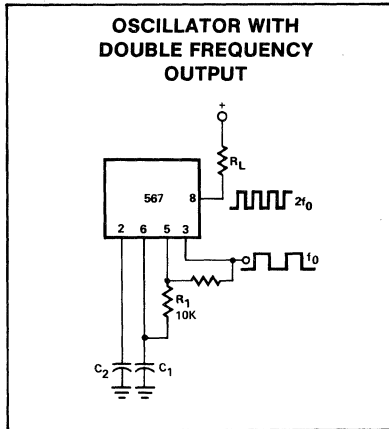
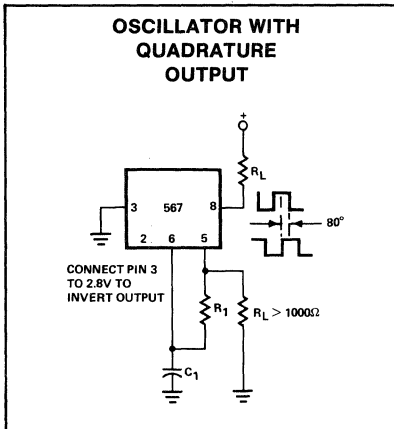
TYPICAL APPLICATIONS



TYPICAL APPLICATIONS (Cont'd)



TYPICAL APPLICATIONS (Cont'd)



NOTE
Application information available on request.

SECTION 15

D-MOS FETS

Section 15—D-MOS

SD210/211/212/213/214/215	D-MOS FET Switch N-Channel Enhancement	463
SD300/303/304	D-MOS FET Dual Gate N-Channel Enhancement	468
SD305/306	D-MOS FET Dual Gate N-Channel Enhancement	475
SD5000/5001/5002	D-MOS FET Quad Analog Switch Arrays and Multiplexers	484

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of -0.3V to +30V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

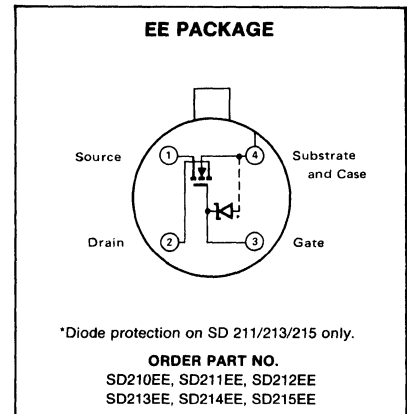
FEATURES

- Low feedback capacitance: 0.30pF
- Low drain node capacitance: 1.3pF
- Low gate node capacitance: 2.4pF
- Low feedthrough and feedback transients
- Ion-implanted for greater reliability
- Excellent isolation from input to output: -120dB
- 35V drain-to-source voltage for SD210/211
- Military qualifications pending

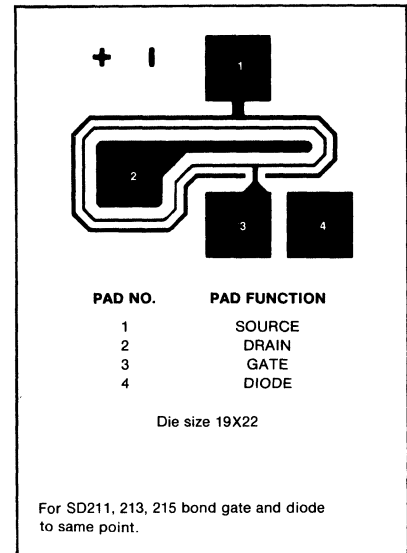
APPLICATIONS

- Switch driver
- Analog switch
- Multiplexers
- Digital switch
- Sample and hold
- Choppers
- A-TO-D converters
- D-TO-A converters

PIN CONFIGURATION (Top View)



CHIP DIAGRAM



ABSOLUTE MAXIMUM RATINGS (all devices)

PARAMETER	RATING	UNIT
Drain current (I _D)	50	mA
Ambient temperature range		
Storage	-65 to +175	°C
Operating	-55 to +125	°C
Transistor dissipation (P _T)		
At 25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
At 25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.*

PARAMETER	SD210	SD211	SD212	SD213	SD214	SD215	UNIT
V _{DS} Drain-to-source	+30	+30	+10	+10	+20	+20	Vdc
V _{SD} Source-to-drain*	+10	+10	+10	+10	+20	+20	Vdc
V _{DB} Drain-to-substrate	+30	+30	+15	+15	+25	+25	Vdc
V _{SB} Source-to-substrate	+15	+15	+15	+15	+25	+25	Vdc
V _{GS} Gate-to-source	±40	-15	±40	-15	±40	-25	Vdc
		+25		+25		+30	
V _{GB} Gate-to-substrate	±40	-0.3	±40	-0.3	±40	-0.3	Vdc
		+25		+25		+30	
V _{GD} Gate-to-drain	±40	-30	±40	-15	±40	-25	Vdc
		+25		+25		+30	

*NOTE
Refer to test conditions specified in Electrical Characteristics Table.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD210			SD211			SD212			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage											
BV _{DS} Drain-to-source	$V_{GS} = V_{BS} = 0V, I_D = 10\mu A$	30	35		30	35					V
BV _{SD} Source-to-drain	$V_{GS} = V_{BS} = -5V, I_S = 10nA$ $V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10	25		10	25		10	25		V
BV _{DB} Drain-to-substrate	$V_{GB} = 0V, \text{source OPEN}$ $I_D = 10nA$	15			15			15			V
BV _{SB} Source-to-substrate	$V_{GB} = 0V, \text{drain OPEN}$ $I_S = 10\mu A$	15			15			15			V
Leakage current											
I _{DS(OFF)} Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$		1	10		1	10		1	10	nA
I _{SD(OFF)} Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$		1	10		1	10		1	10	nA
I _{GBS} Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = \pm 40V$ $V_{GB} = +25V$			0.1			10			0.1	nA μA
V _T Threshold voltage	$V_{DS} = V_{GS} = V_T, I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	V
r _{DS(ON)} Drain-to-source resistance	$I_D = 1.0mA, V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$ $V_{GS} = +25V$		50 30 23 19 17	70 45		50 30 23 19	70 45		50 30 23 19 17	70 45	Ω Ω Ω Ω Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD213			SD214			SD215			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage											
BV _{DS} Drain-to-source	V _{GS} = V _{BS} = -5V, I _S = 10nA	10	25		20	25		20	25		V
BV _{SD} Source-to-drain	V _{GD} = V _{BD} = -5V I _D = 10nA	10			20			20			V
BV _{DB} Drain-to-substrate	V _{GB} = 0V, source OPEN I _D = 10nA	15			25			25			V
BV _{SB} Source-to-substrate	V _{GB} = 0V, drain OPEN I _S = 10μA	15			25			25			V
Leakage current											
I _{DS(OFF)} Drain-to-source	V _{GS} = V _{BS} = -5V V _{DS} = +10V		1	10							nA
I _{SD(OFF)} Source-to-drain	V _{DS} = +20V V _{GD} = V _{BD} = -5V					1	10		1	10	nA
I _{GS} Gate	V _{SD} = +10V V _{SD} = +20V V _{DB} = V _{SB} = 0V V _{GB} = ±40V V _{GB} = +25V V _{GB} = +30V		1	10		1	10		1	10	nA μA μA
V _T Threshold voltage	V _{DS} = V _{GS} = V _T , I _S = 1μA V _{SB} = 0V	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
r _{DS(ON)} Drain-to-source resistance	I _D = 1.0mA, V _{SB} = 0 V _{GS} = +5V V _{GS} = +10V V _{GS} = +15V V _{GS} = +20V V _{GS} = +25V		50 30 23 19	70 45		50 30 23 19 17	70 45		50 30 23 19 17	70 45	Ω Ω Ω Ω Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD210			SD211			SD212			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
g _{fs} Forward transconductance	V _{DS} = 10V, V _{SB} = 0V I _D = 20mA, f = 1kHz	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)	V _{DS} = 10V, f = 1MHz V _{GS} = V _{BS} = -15V										
C _(GS+GD+GB) Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
C _(GD+DB) Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
C _(GS+SB) Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C _{DG} Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

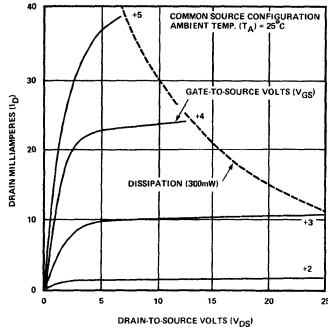
AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD213			SD214			SD215			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
g _{fs} Forward transconductance	V _{DS} = 10V, V _{SB} = 0V I _D = 20mA, f = 1kHz	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)	V _{DS} = 10V, f = 1MHz V _{GS} = V _{BS} = -15V										
C _(GS+GD+GB) Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
C _(GD+DB) Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
C _(GS+SB) Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C _{DG} Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

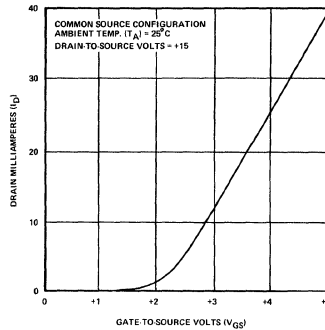


TYPICAL PERFORMANCE CHARACTERISTICS

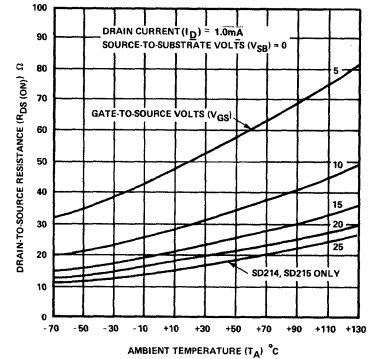
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



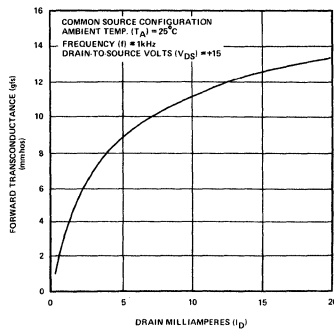
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



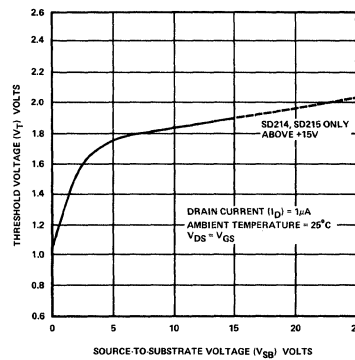
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



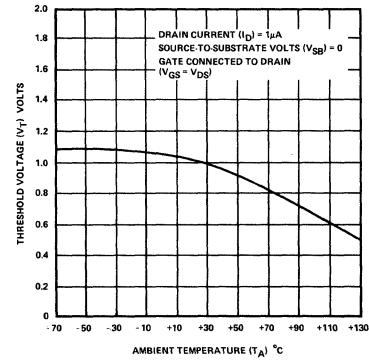
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



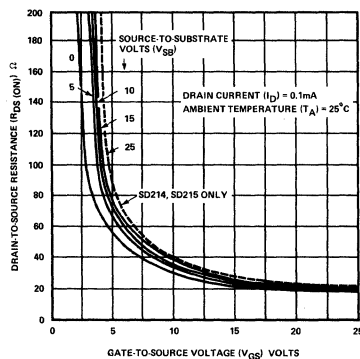
THRESHOLD VOLTAGE vs SOURCE-TO-SUBSTRATE VOLTAGE



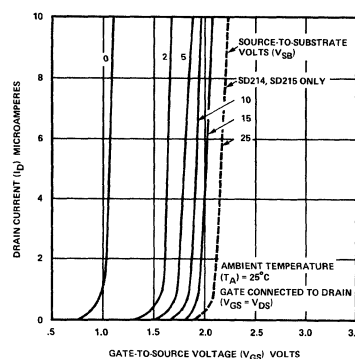
THRESHOLD VOLTAGE vs TEMPERATURE



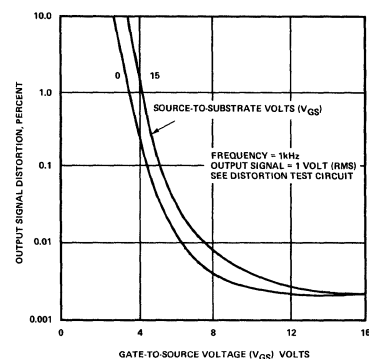
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



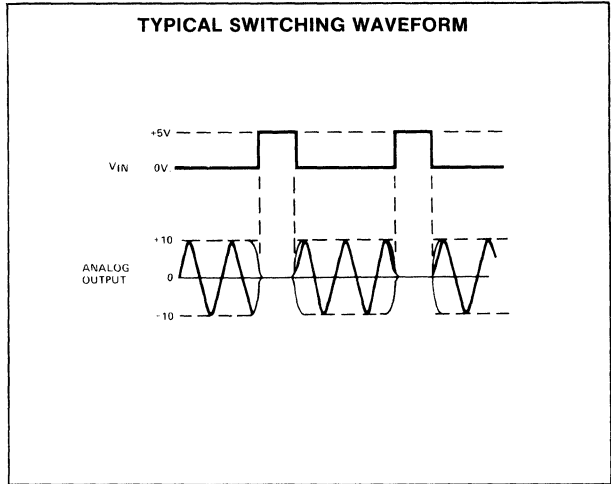
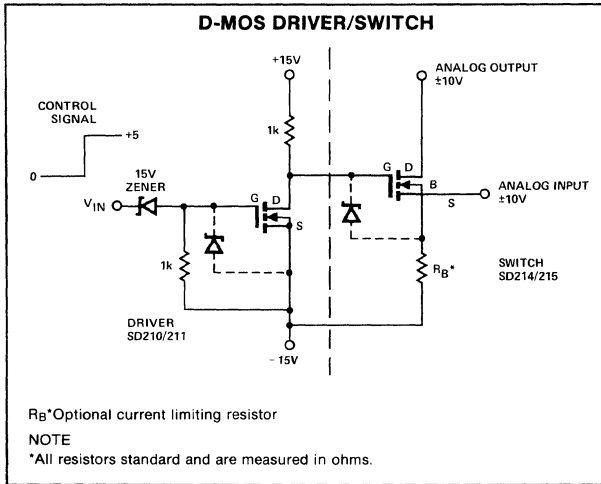
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



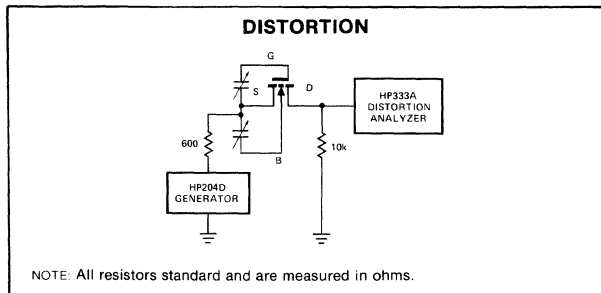
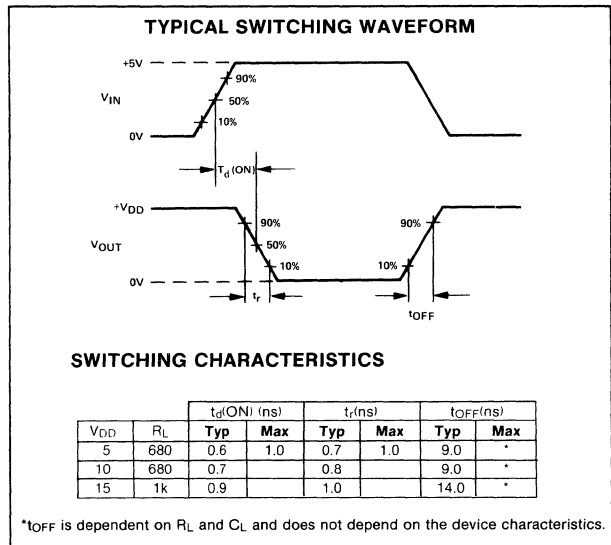
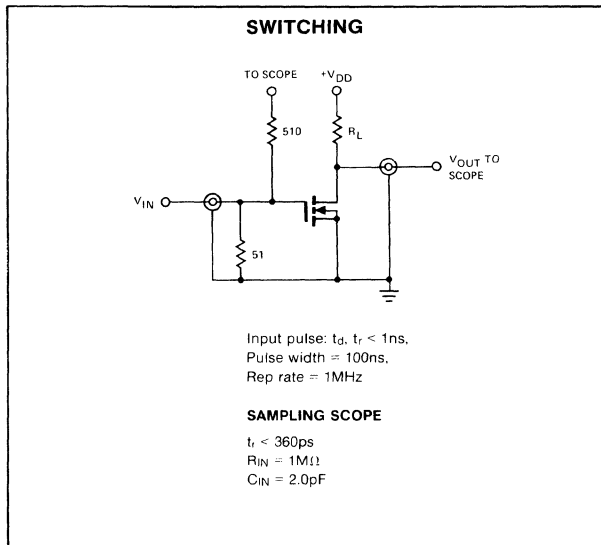
DISTORTION vs GATE-TO-SOURCE VOLTAGE



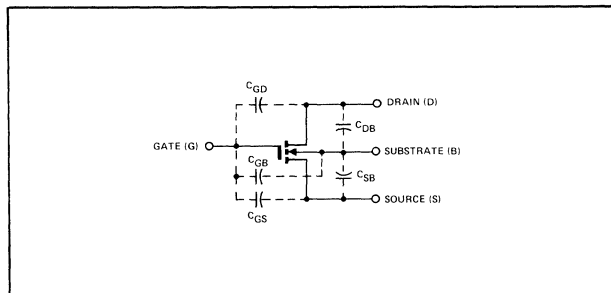
TYPICAL APPLICATION



TEST CIRCUITS



CAPACITANCE MODEL



DESCRIPTION

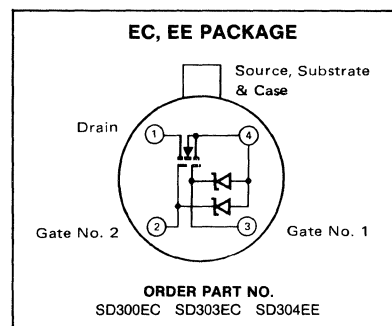
The Signetics D-MOS SD300/303/304 are silicon, dual-insulated-gate, field effect transistor of the N-channel enhancement mode type. It is fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +25.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The device characteristics make it ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (Crss) low. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of these devices. The SD300/303/304 are hermetically sealed in a modified 4-lead TO-72 package.

GENERAL FEATURES

- Lower cross-modulation and wider dynamic range than bipolar or single gate FETs
- Reverse AGC capability
- Linear mixing capability
- Diode protected gates
- High forward transconductance: 10mmhos
- ION-implanted
- Positive bias only

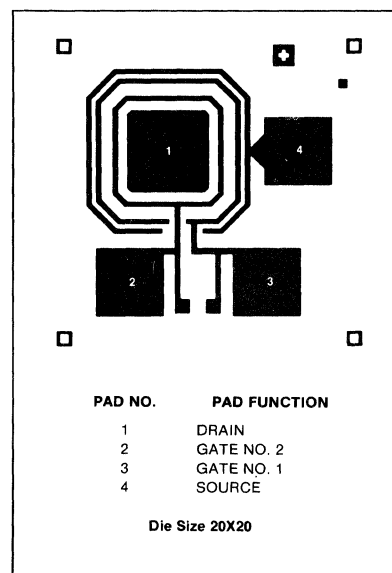
PIN CONFIGURATIONS (Top View)



FEATURES (Typical Values)

PARAMETER	SD300	SD303	SD304	UNIT
High gain through UHF range	13	14		dB at 1GHz
High gain through VHF range			16	dB at 500MHz
Low noise through UHF range	8	5.5		dB at 1GHz
Low noise through VHF range			5	dB at 500MHz
Low input capacitance	2.0	3.0	2.5	pF
Low feedback capacitance	0.02	0.02	0.03	pF
Low output capacitance	1.0	0.6	1.0	pF

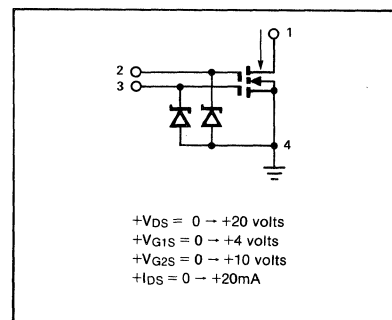
CHIP DIAGRAM



ABSOLUTE MAXIMUM RATINGS TA = 25°C unless otherwise specified.

PARAMETER	RATING	UNIT
VDS Drain-to-source		
SD300/304	+25	V
SD303	+20	V
VG1B DC gate no. 1-to-substrate voltage	-0.3, +10	V
VG2B DC gate no. 2-to-substrate voltage	-0.3, +15	V
ID Drain current	50	mA
TA Ambient temperature range		
Storage	-65 to +175	°C
Operating	-55 to +125	°C
PT Transistor dissipation		
At +25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
At +25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

DUAL GATE CASCODE BIAS SCHEME



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD300			SD303			UNIT
			Min	Typ	Max	Min	Typ	Max	
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V, I_D = 5\mu A$	25	30		20	25		V
I_{G1SS}	Gate 1 Leakage current	$V_{G1S} = +5V, V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS}	Gate 2 Leakage current	$V_{G2S} = +10V, V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
$I_{D(OFF)}$	Drain-to-source Leakage current	$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$		0.001	0.1		0.001	0.1	μA
I_{DSS}	Zero bias Drain current	$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$		0.001	0.1		0.001	0.1	μA
V_{T1}	Gate 1 Threshold voltage	$V_{DS} = V_{G1S} = V_{T1}, V_{G2S} = +10V, I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2 Threshold voltage	$V_{DS} = V_{G2S} = V_{T2}, V_{G1S} = +4V, I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
$r_{DS(ON)}$	Drain-to-source On resistance	$V_{G1S} = +5V, V_{G2S} = +10V, I_D = 1.0mA$		90	130		65	80	Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD304			UNIT
			Min	Typ	Max	
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V, I_D = 5\mu A$	25	30		V
I_{G1SS}	Gate 1 Leakage current	$V_{G1S} = +5V, V_{G2S} = V_{DC} = 0V$		0.001	0.1	μA
I_{G2SS}	Gate 2 Leakage current	$V_{G2S} = +10V, V_{G1S} = V_{DS} = 0V$		0.001	0.1	μA
$I_{D(OFF)}$	Drain-to-source Leakage current	$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$		0.001	0.1	μA
I_{DSS}	Zero bias Drain current	$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$		0.001	0.1	μA
V_{T1}	Gate 1 Threshold voltage	$V_{DS} = V_{G1S} = V_{T1}, V_{G2S} = +10V, I_D = 1\mu A$	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold voltage	$V_{DS} = V_{G2S} = V_{T2}, V_{G1S} = +4V, I_D = 1\mu A$	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-source On resistance	$V_{G1S} = +5V, V_{G2S} = +10V, I_D = 1.0mA$		90	130	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD300			SD303			SD304			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C _{iss} Small signal short circuit Capacitances Input	f = 1MHz, Gate 2 AC grounded V _{DS} = +15V, V _{G1S} = 3.5V, V _{G2S} = +10V, I _D = 18mA		2.0	2.5							pF
		V _{DS} = +15V, V _{G1S} = +2.5V, V _{G2S} = +10V, I _D = 18mA					3.0	3.5			
C _{oss} Output	V _{DS} = +15V, V _{G1S} = 0V V _{G2S} = +10V		1.0	1.2		0.6			1.0	1.2	pF
C _{rss} Reverse transfer	V _{DS} = +15V V _{G1S} = 0V, V _{G2S} = +10V		0.02			0.02			0.03		pF
g _{fs} Forward transconductance	V _{DS} = +15V, V _{G1S} = +3.5V V _{G2S} = +10V, I _D = 18mA, f = 1kHz	8.0	10.0					8.0	10.0		mmhos
		V _{DS} = +15V, V _{G1S} = +2.5V, V _{G2S} = +10V, I _D = 18mA				13.0	15.0				
G _{ps} Power gain	V _{DS} = +15V, V _{G1S} = +3.5V, V _{G2S} = +10V, I _D = 18mA f = 1GHz f = 500MHz f = 200MHz	9.0	13.0*								dB
								13.0	16.0		dB
		22.0	24.0		10.0	14.0*					dB
NF Noise figure	V _{DS} = +15V, V _{G1S} = +3.5V, V _{G2S} = +10V, I _D = 18mA f = 1GHz f = 500MHz f = 200MHz		8.0*	9.0							dB
								5.0	6.0		dB
			3.0	4.0		5.5*	7.0				dB
E _{int} Interfering signal level at gate for 1% cross-modulation distortion. Peak voltage referenced to 300Ω system.	V _{DS} = +15V, V _{G2S} = +10V, I _D = 18mA, Desired signal f = 500MHz, Undersired signal f = 501MHz			200					200		mV
		V _{DS} = +15V, V _{G2S} = +10V, I _D = 18mA, Wanted Signal f = 1GHz, Interfering signal f = 0.995GHz					150				
AGC Range of automatic (V _{G2S}) Gain control	V _{DS} = +15V, V _{G1S} = +3.5V, f = 500MHz		40						40		dB
		V _{DS} = +15V, V _{G1S} = +2.5V, f = 500MHz					40				dB

*NOTE

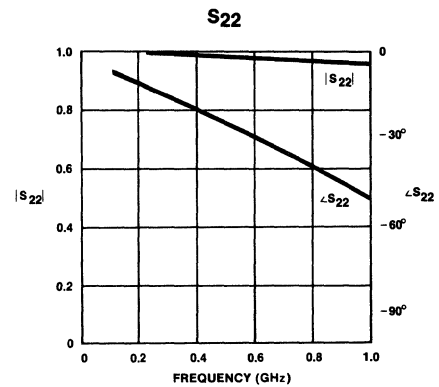
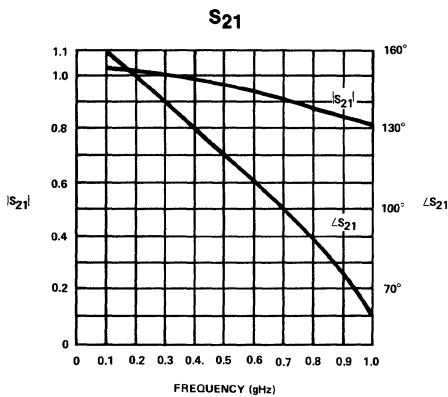
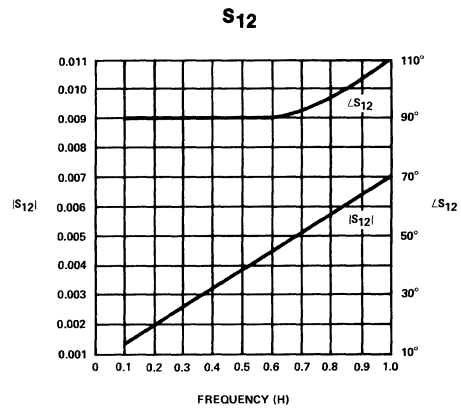
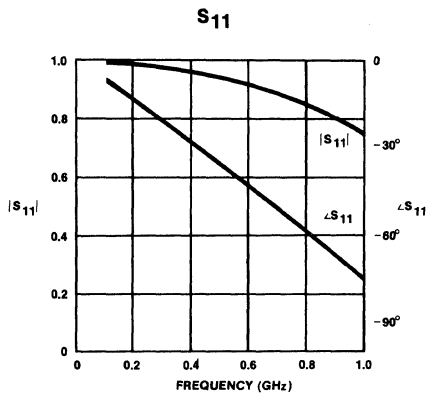
Measured in amplifier test fixture.

SD300 TYPICAL PERFORMANCE CHARACTERISTICS

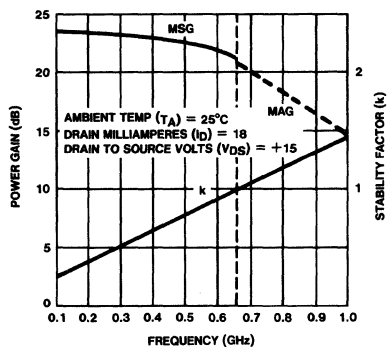
SD300 "S" PARAMETERS

AMBIENT TEMP. (TA) = +25°C
DRAIN MILLIAMPERES (ID) = 18

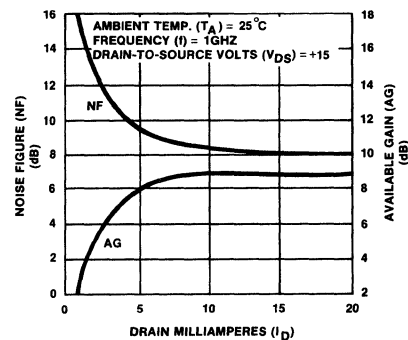
DRAIN-TO-SOURCE VOLTS (VDS) = +15
GATE NO. 1-TO-SOURCE VOLTS (VG1S) ≈ +3.5
GATE NO. 2-TO-SOURCE VOLTS (VG2S) = +10



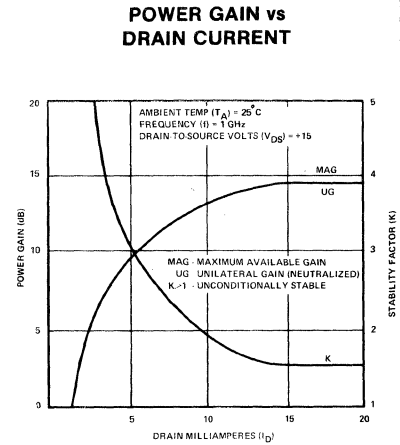
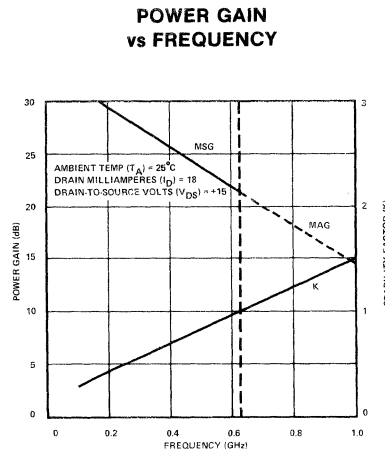
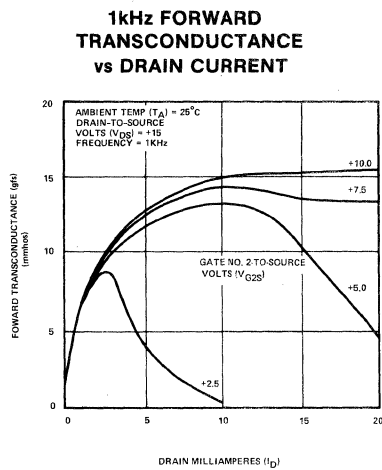
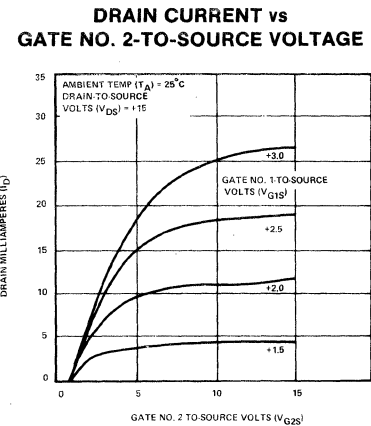
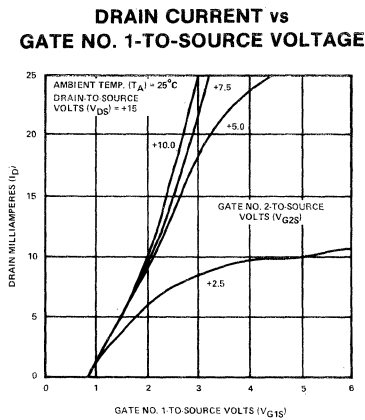
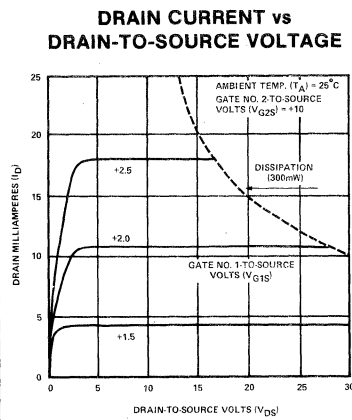
POWER GAIN vs FREQUENCY



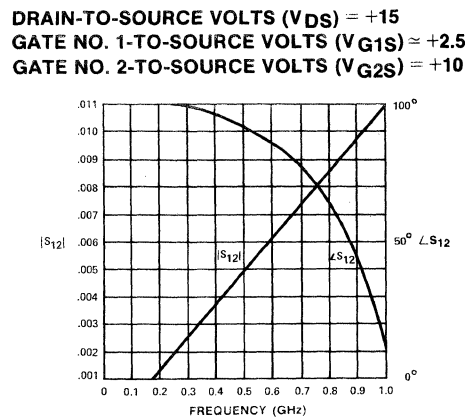
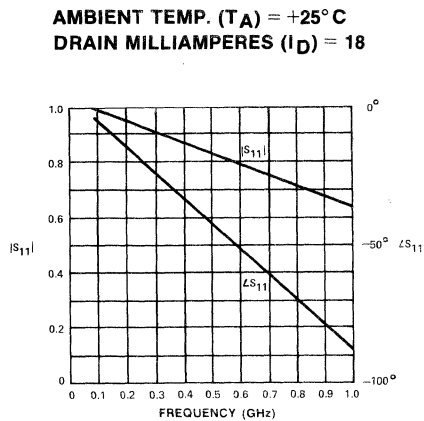
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



SD303 TYPICAL PERFORMANCE CHARACTERISTICS

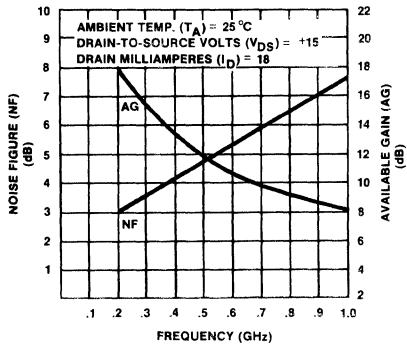


SD303 "S" PARAMETERS

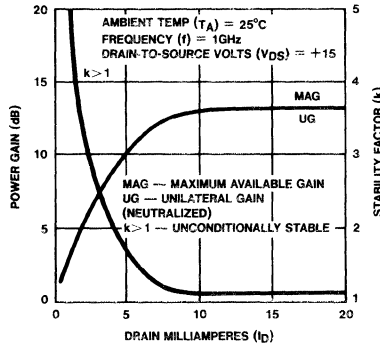


SD300/SE304 TYPICAL PERFORMANCE CHARACTERISTICS(Cont'd)

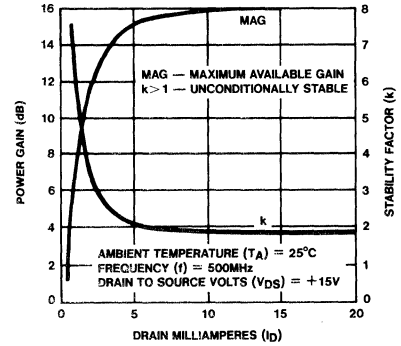
NOISE FIGURE AND AVAILABLE GAIN vs FREQUENCY
SD300



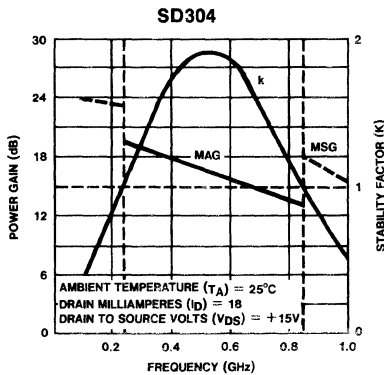
POWER GAIN vs DRAIN CURRENT
SD300



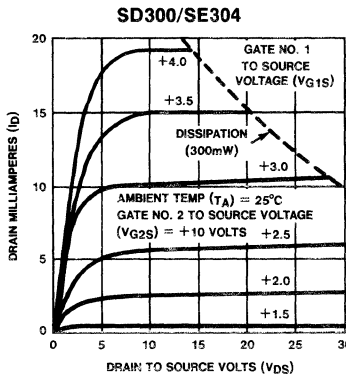
POWER GAIN vs DRAIN CURRENT
SD304



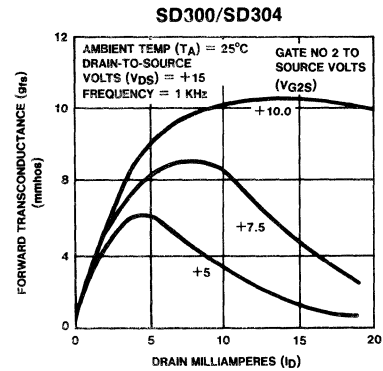
POWER GAIN vs FREQUENCY
SD304



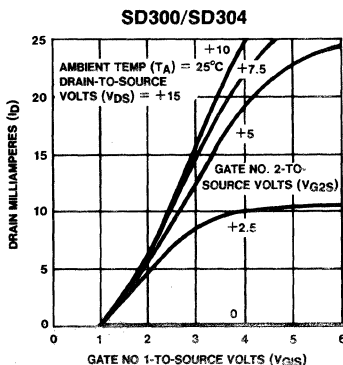
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE
SD300/SE304



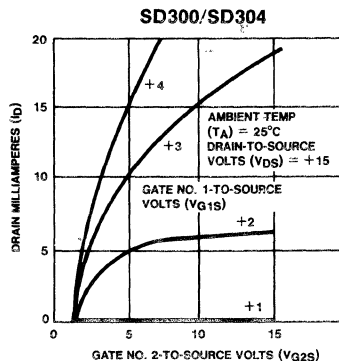
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT
SD300/SD304



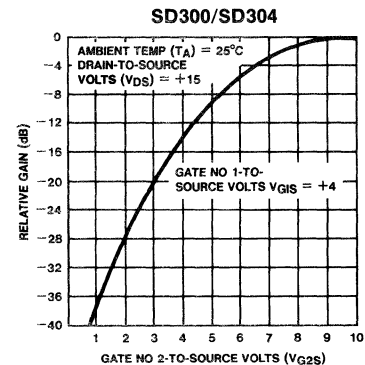
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE
SD300/SD304



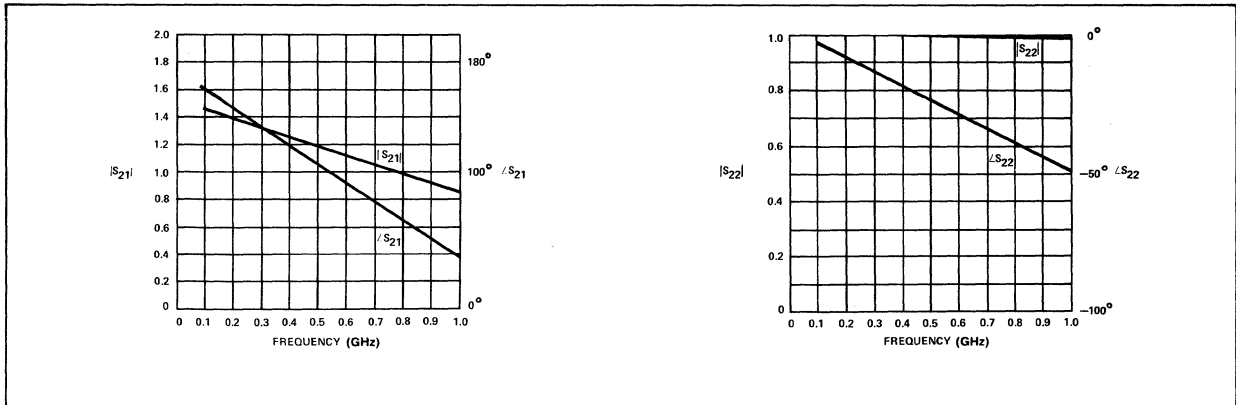
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE
SD300/SD304



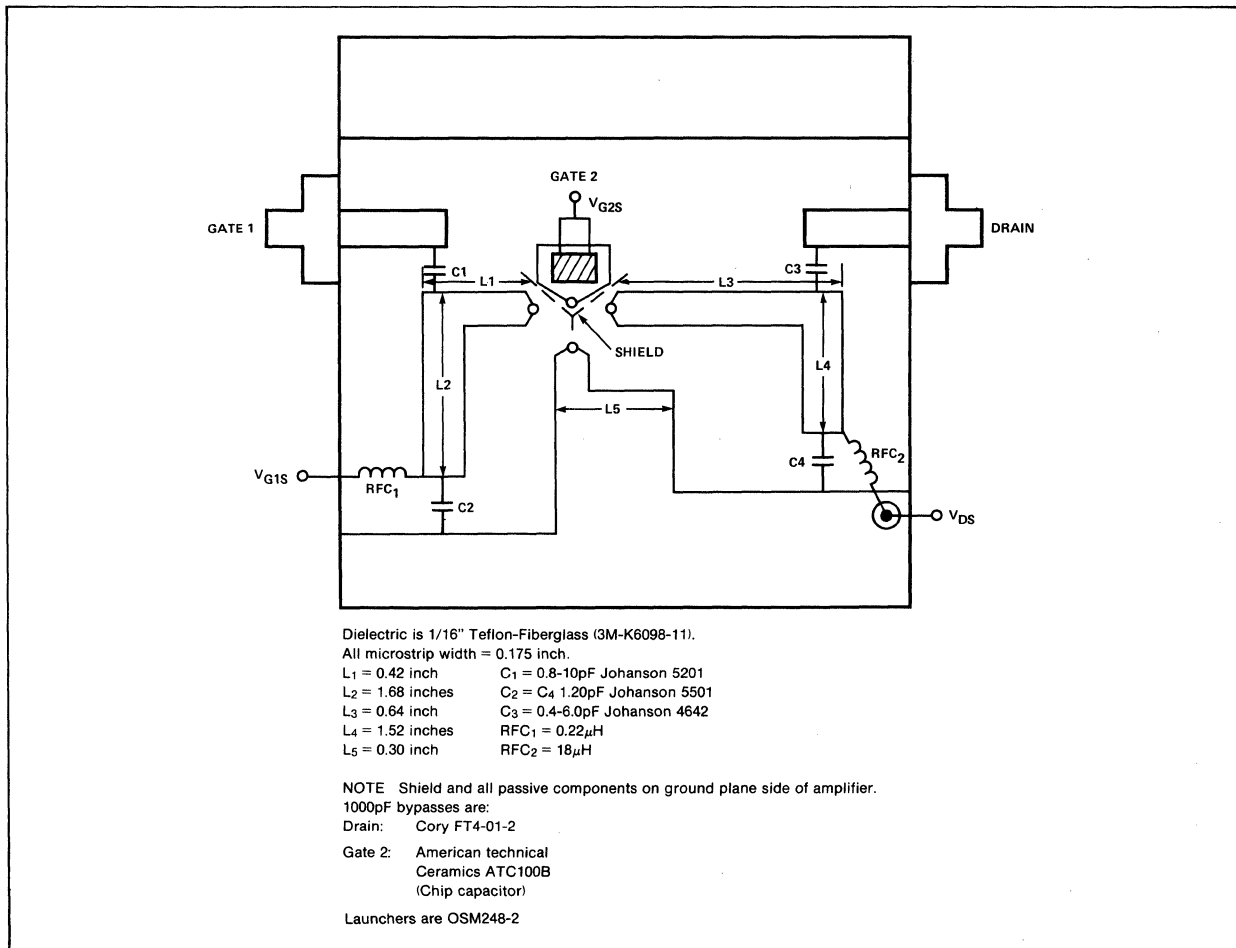
AUTOMATIC GAIN CONTROL RANGE AT 50MHz
SD300/SD304



SD303 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



1GHz TEST FIXTURE (used with SD300, SD303)



DESCRIPTION

The Signetics D-MOS SD305 and 306 are silicon, dual-insulated gate, field-effect transistors of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of -0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The characteristics of the devices make them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (C_{G1D}) typically less than 0.03pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the devices. The SD305 and SD306 are hermetically sealed in a 4-lead TO-72 package.

GENERAL FEATURES

- Positive bias only
- Low gate voltages
- Enhancement mode operation
- Wide AGC range: -50dB at 200MHz
- Zener diode gate protection
- ION implanted for greater reliability

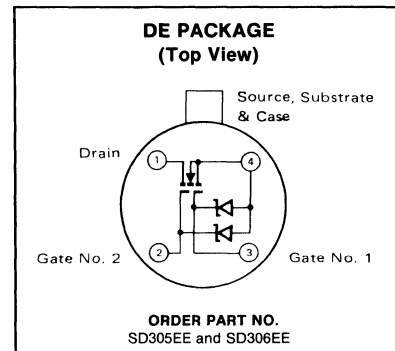
FEATURES—SD305 (VHF TV and FM Mixer)

- High conversion gain: 17dB at 200MHz with $V_{G1S} = V_{G2S}$ for biasing simplicity
- Excellent isolation from Gate No. 1 (RF) to Gate No. 2 (LO): -20dB at 200MHz
- Low input capacitance: 4.0pF
- Low feedback capacitance: 0.03pF
- Excellent cross modulation performance and low noise operation
- High transconductance: 27mmhos

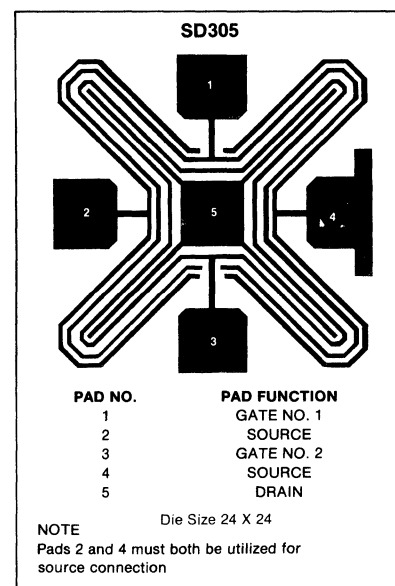
FEATURES—SD306 (VHF TV and FM RF Amplifier)

- High power gain without neutralization: 20dB at 200MHz
- Low noise figure: 1.5dB at 200MHz
- Low input and output capacitance: 3.3pF and 1.0pF constant with AGC
- Low feedback capacitance: 0.03pF
- Superior cross modulation performance
- High transconductance: 15mmhos

PIN CONFIGURATION

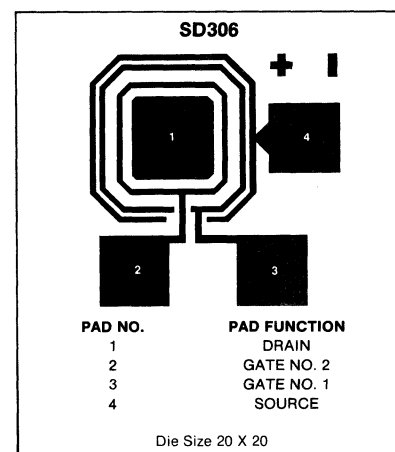


CHIP DIAGRAMS



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
V_{DS} Drain-to-source voltage	+20	V
V_{G1B} Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
V_{G2B} Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
I_D Drain current		
SD305	150	mA
SD306	50	mA
T_A Ambient temperature range		
Storage	-65 to +175	$^\circ\text{C}$
Operating	-55 to +125	$^\circ\text{C}$
P_T Transistor dissipation		
At 25 $^\circ\text{C}$ case temperature (Derate linearly to 125 $^\circ\text{C}$ case temperature at the rate of 8.0mW/ $^\circ\text{C}$)	1.2	W
At 25 $^\circ\text{C}$ free-air temperature (Derate linearly to 125 $^\circ\text{C}$ free-air temperature at the rate of 2.0mW/ $^\circ\text{C}$)	300	mW



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD305			SD306			UNIT
		Min	Typ	Max	Min	Typ	Max	
OFF Characteristics								
BV_{DS} Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		20	25		V
I_D (OFF) Drain-to-source Leakage current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{DSS} Zero bias drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{G1SS} Gate no. 1 leakage current	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS} Gate no. 2 leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
ON Characteristics								
V_{T1} Gate 1 threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2} Gate 2 threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
$r_{DS(ON)}$ Drain-to-source on resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		30	60		65	100	Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD305			SD306			UNIT
		Min	Typ	Max	Min	Typ	Max	
Small signal characteristics								
g_{fs} Forward transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, $f = 1kHz$ $I_D = 50mA$ $I_D = 18mA$	24	27		13	15		mmhos
g_{fs} (CONV) Conversion transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f = 1kHz$, $E_{LO(RMS)} = 750mV$		10					mmhos mmhos
Capacitances	$f = 1MHz$, gate 2 AC grounded							
C_{G1S} Input	$V_{DS} = +15V$, $V_{G2S} = +10V$ $I_D = 50mA$ $I_D = 18mA$		4.0	5.0				pF
C_{DS} Output	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	5.0		3.3	3.6	pF
C_{G1D} Reverse transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03			0.03		pF
Input admittance $Re(Y_{11})$ $Im(Y_{11})$	$f = 200MHz$, $V_{DS} = +15V$	$V_{G1S} = V_{G2S}$, $I_D = 8mA$	1.05 6.66		$V_{G2S} = +10V$, $I_D = 18mA$	1.11 4.76		mmhos mmhos
Output admittance $Re(Y_{22})$ $Im(Y_{22})$	$f = 200MHz$, $V_{DS} = +15V$		0.73 2.09			1.05 1.54		mmhos mmhos
Forward transmittance $Re(Y_{21})$ $Im(Y_{21})$	$f = 200MHz$, $V_{DS} = +15V$		4.69 -3.01			13.23 -5.62		mmhos mmhos
Reverse transmittance $Re(Y_{12})$ $Im(Y_{12})$	$f = 200MHz$, $V_{DS} = +15V$		0.04 -0.03			0.01 -0.04		mmhos mmhos
G_{ps} Power gain ²	$V_{DS} = +15V$, $V_{G2S} = +10V$ $I_D = 18mA$, $f = 200MHz$				17	20		dB

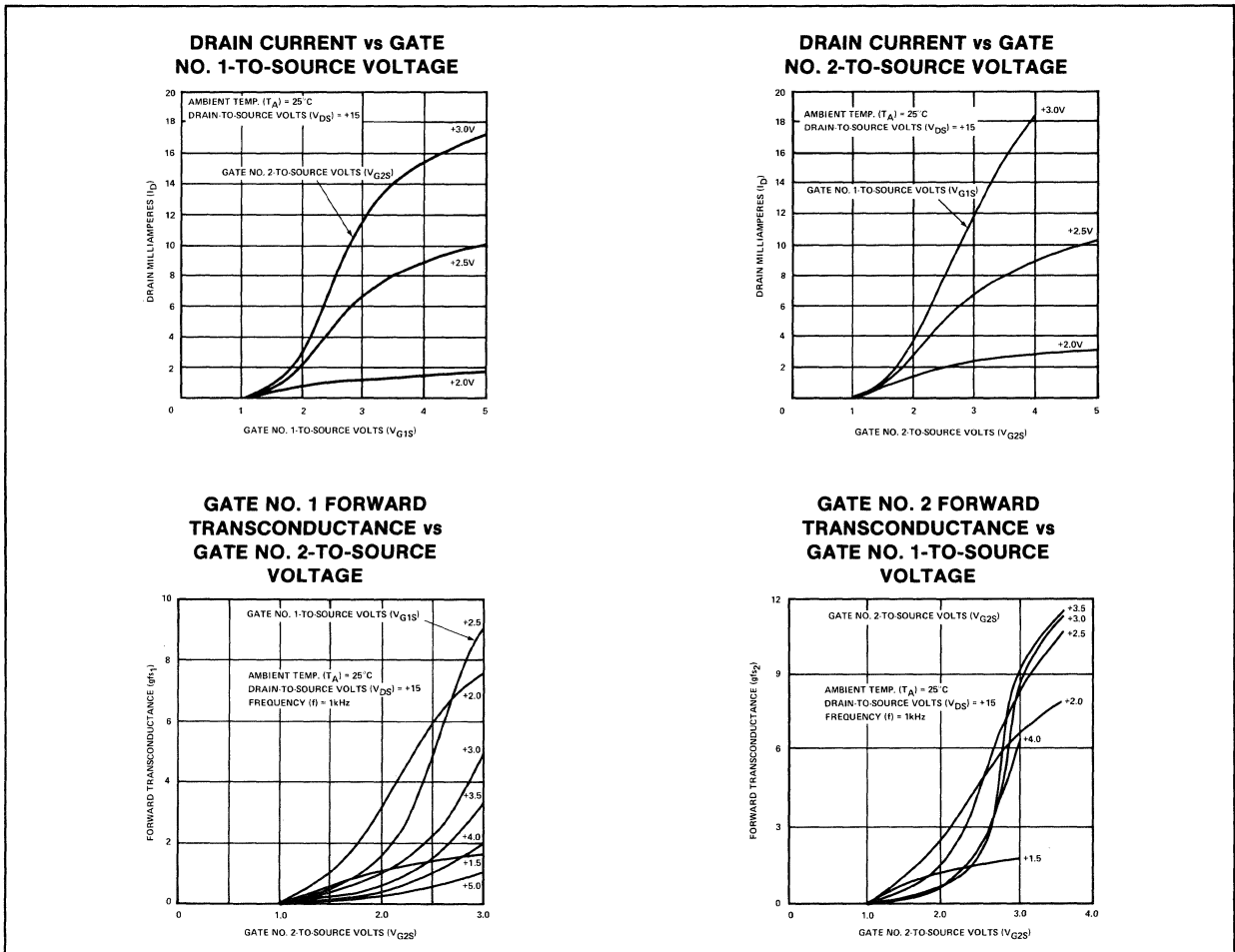
AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD305			SD306			UNIT
		Min	Typ	Max	Min	Typ	Max	
$G_{ps}(\text{CONV})$ Conversion power gain ¹	$V_{DS} = +15\text{V}$, $V_{G1S} = V_{G2S}$, $I_D = 8\text{mA}$, $f_{rf} = 200\text{MHz}$, $f_{LO} = 245\text{MHz}$	14	17					dB
NF Noise figure	$V_{DS} = +15\text{V}$, $V_{G2S} = +10\text{V}$, $I_D = 18\text{mA}$, $f = 200\text{MHz}$					1.5	2.5	dB
$AGC_{V_{G2S}}$ Range of automatic gain control	$V_{DS} = +15\text{V}$, $V_{G1S} \cong +2.5\text{V}$, $V_{G2S} = +10\text{V} \rightarrow 0\text{V}$, $f = 200\text{MHz}$					50		dB
E_{INT} Interfering signal level at gate 1 for 1% cross modulation distortion, peak voltage referenced to 50Ω system ³	$V_{DS} = 15\text{V}$, $V_{G2S} = +8\text{V}$, $I_D = 15\text{mA}$ Wanted signal $f = 200\text{MHz}$ interfering signal $f = 196\text{MHz}$					480		mV

NOTES

1. Measured in mixer test fixture.
2. Measured in amplifier test fixture.
3. Measured as shown in block diagram.

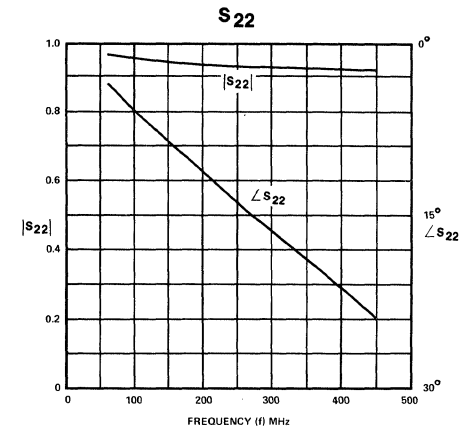
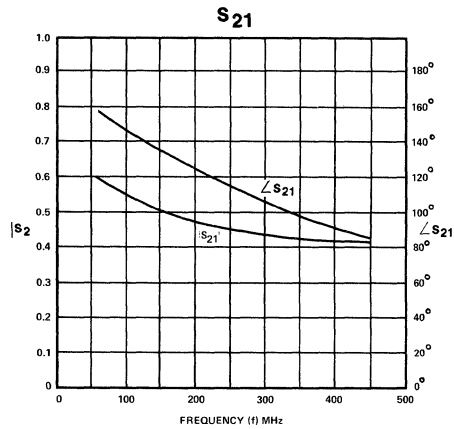
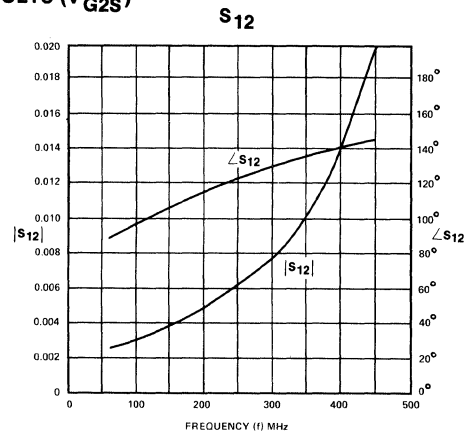
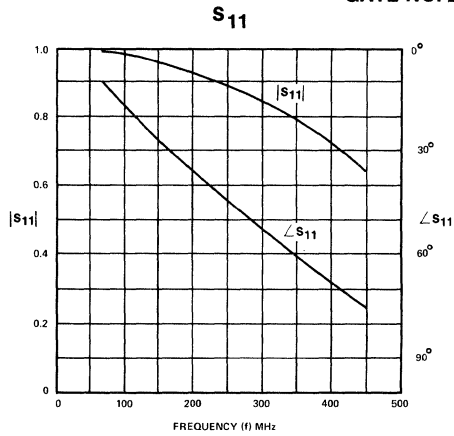
SD305 TYPICAL PERFORMANCE CHARACTERISTICS



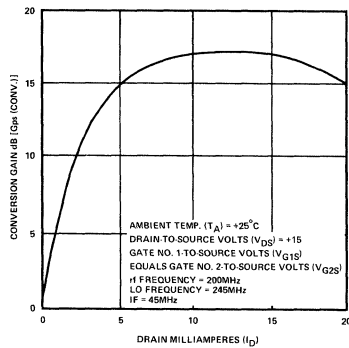
SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

"S" PARAMETERS

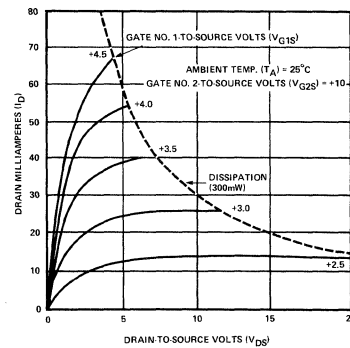
AMBIENT TEMP. (T_A) = +25°C
 DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
 DRAIN MILLIAMPERES (I_D) = 8
 GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) =
 GATE NO. 2-TO-SOURCE VOLTS (V_{G2S})



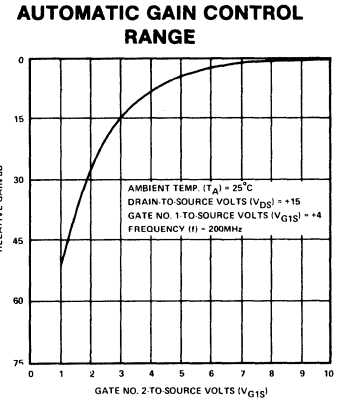
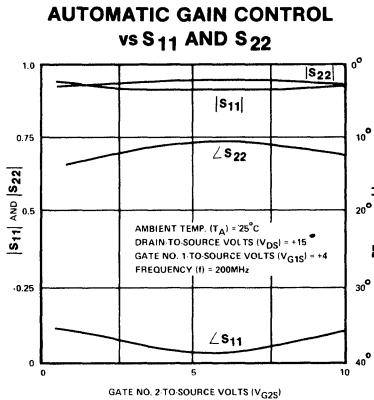
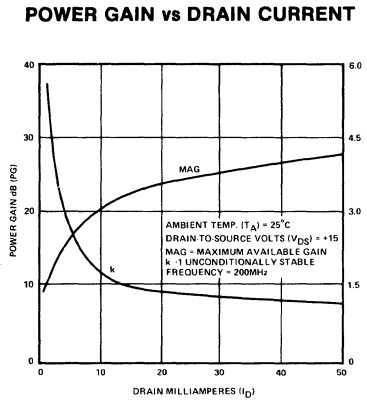
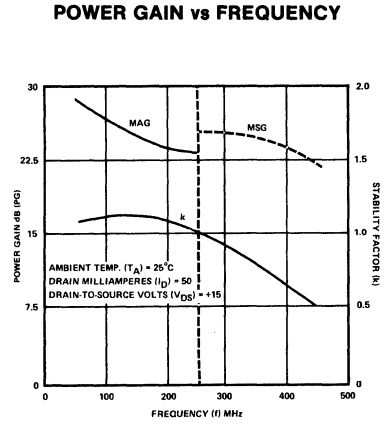
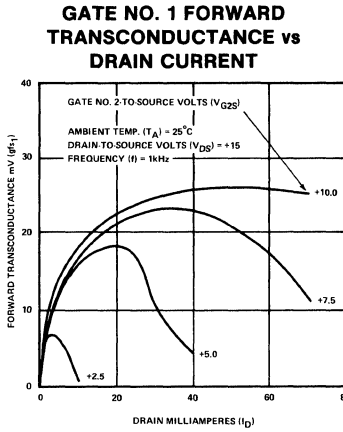
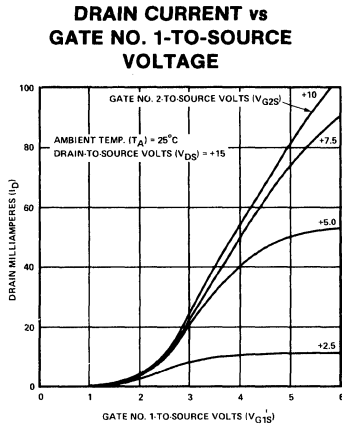
CONVERSION GAIN vs DRAIN CURRENT



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

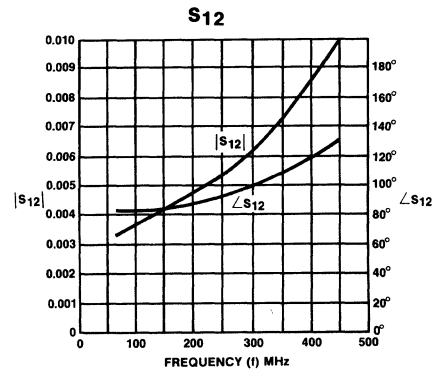
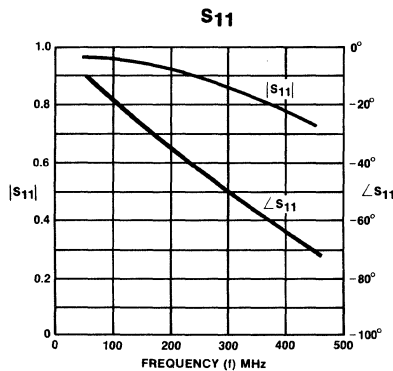


SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

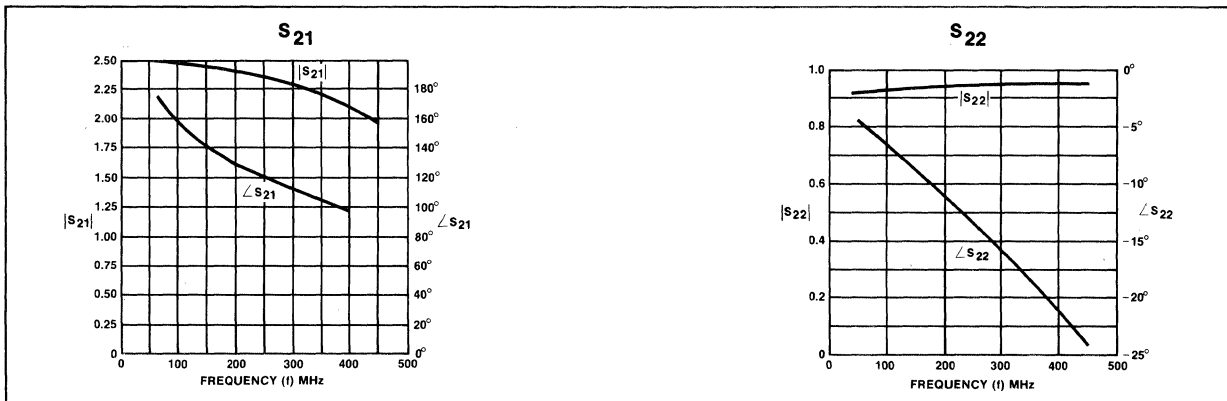


“S” PARAMETERS

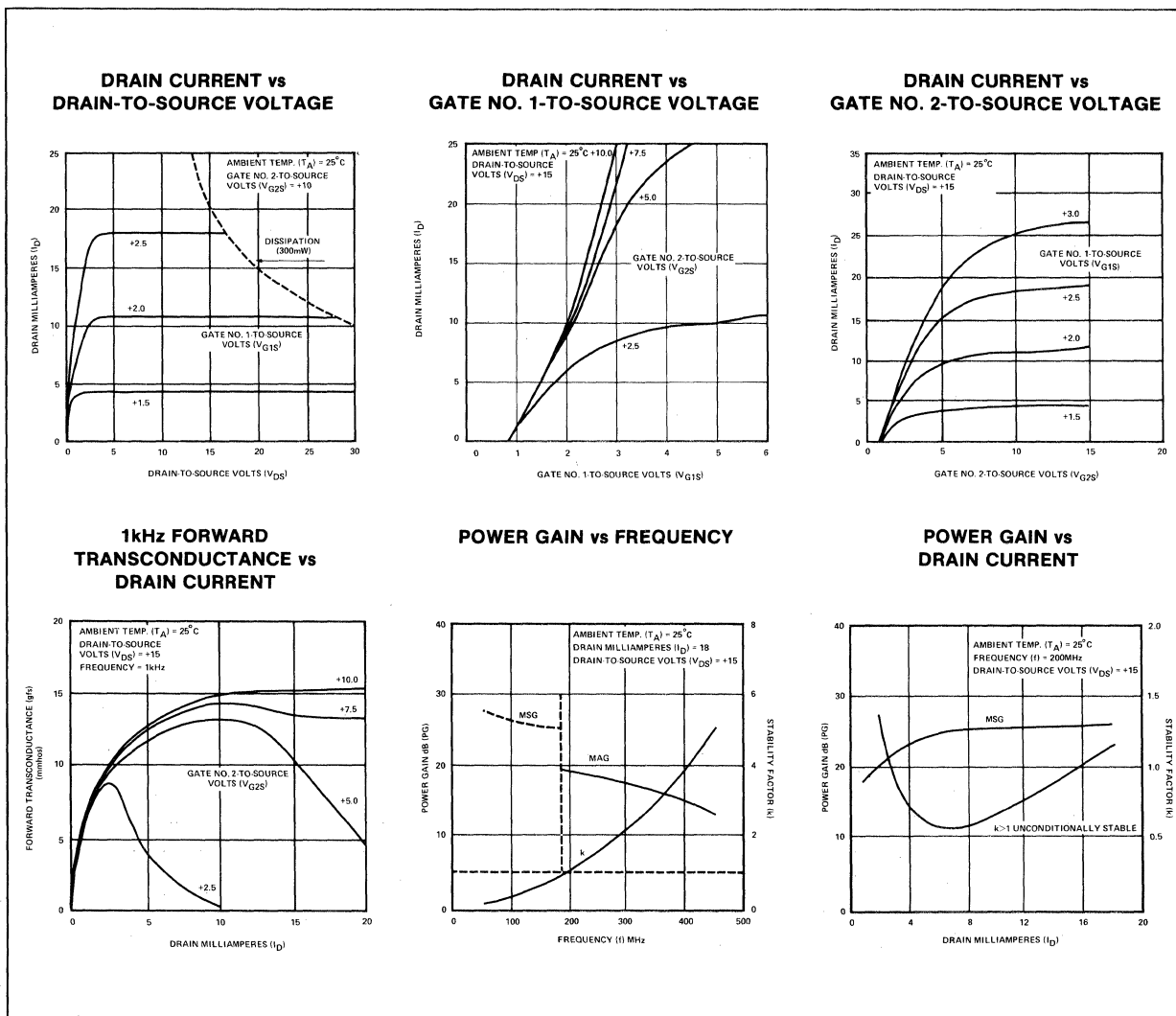
AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
DRAIN MILLIAMPERES (I_D) = 50
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) = +3.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10



SD305 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

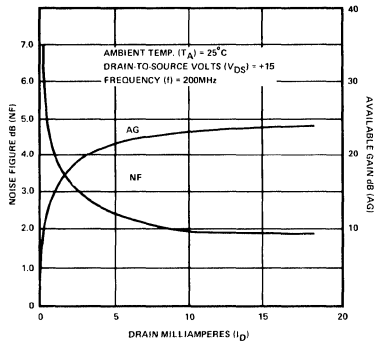


SD306 TYPICAL PERFORMANCE CHARACTERISTICS

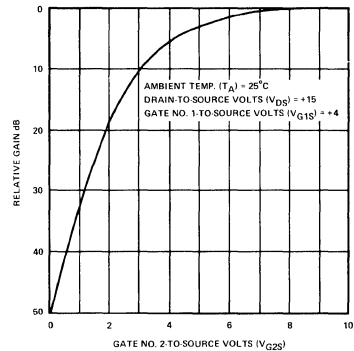


SD306 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

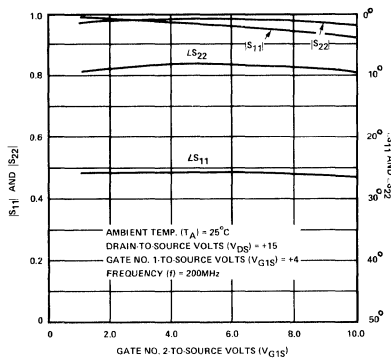
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



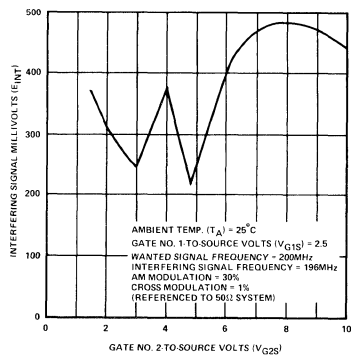
AUTOMATIC GAIN CONTROL RANGE AT 200MHz



S11 AND S22 vs AUTOMATIC GAIN CONTROL



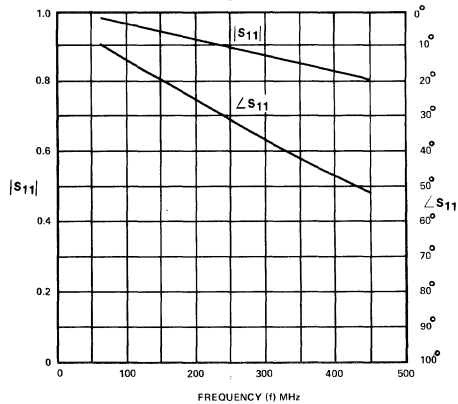
INTERFERING SIGNAL LEVEL vs GATE NO. 2-TO-SOURCE VOLTS



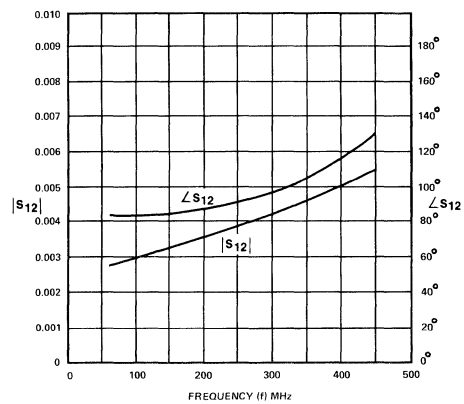
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
 DRAIN-TO-SOURCE VOLTS (V_{DS}) = 15
 DRAIN MILLIAMPERES (I_D) = 8
 GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) = +2.5
 GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

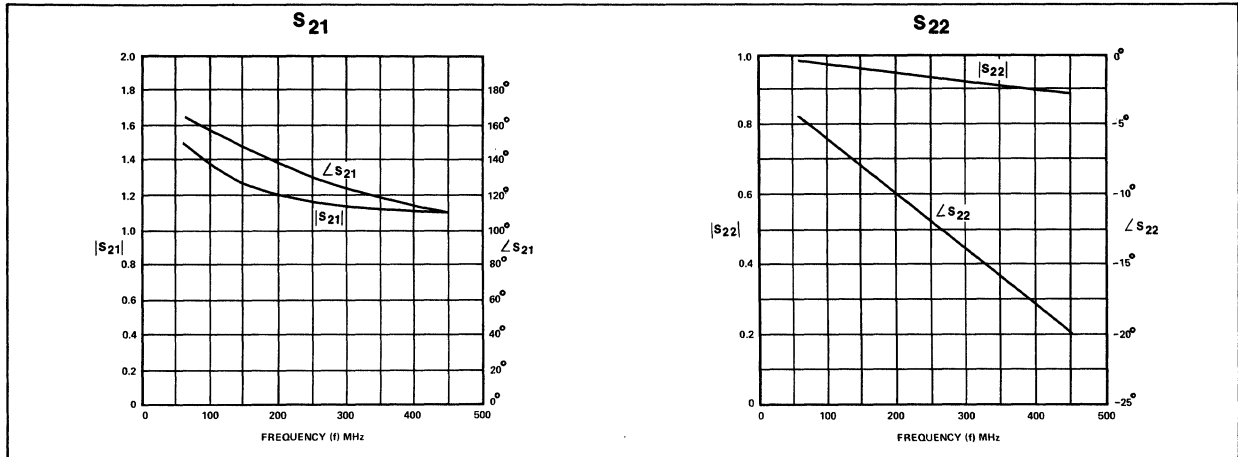
S11



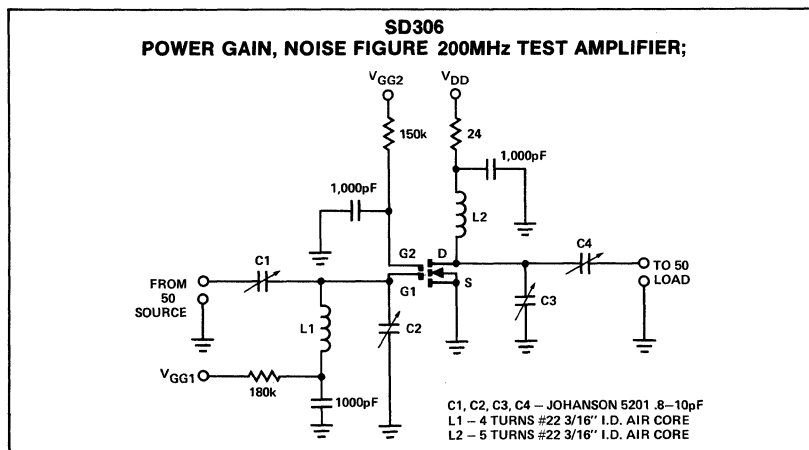
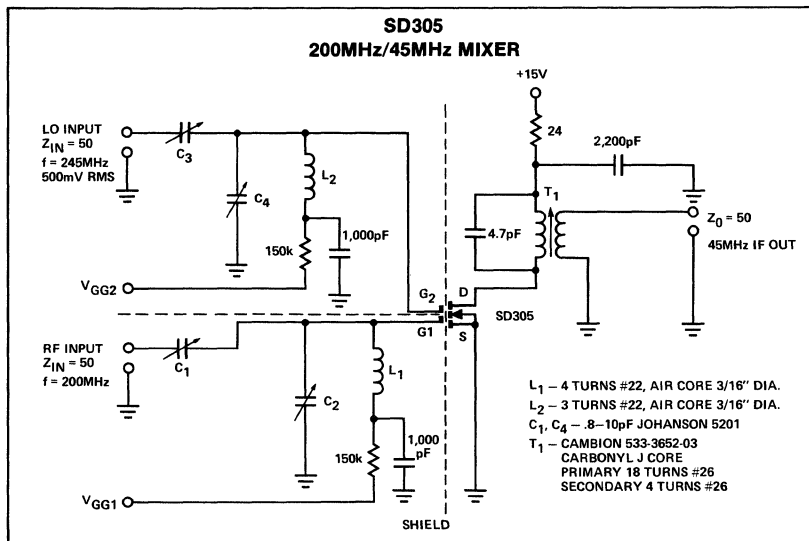
S12



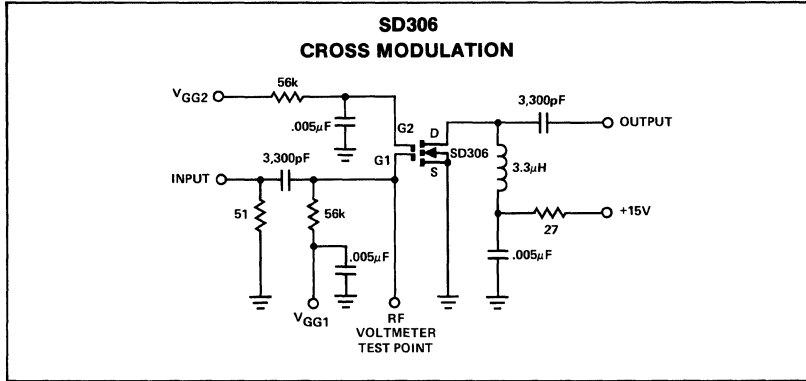
SD306 TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



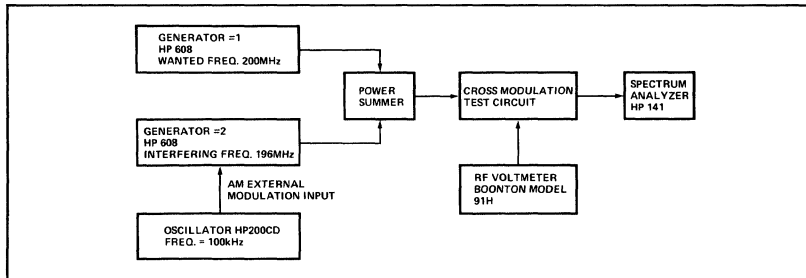
TEST CIRCUITS



TEST CIRCUITS (Cont'd)



BLOCK DIAGRAM OF CROSS MODULATION TEST



SD306

TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately -15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turn off the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

DESCRIPTION

The Signetics D-MOS SD5000 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enhancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response, and wide voltage range are required. The SD5000 quad switch array quad multiplexer can handle high voltage analog signals ($\pm 10V$). The SD5002 is designed for $\pm 7.5V$ analog signals using $\pm 15V$ power supplies. The SD5001 is designed for lower voltage applications.

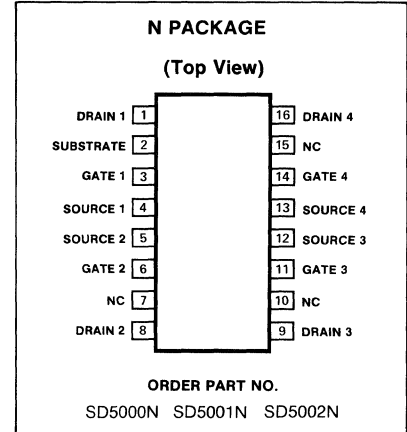
FEATURES

- Low input capacitance: 2.4pF
- Low feedback capacitance: 0.3pF
- Low output capacitance: 1.3pF
- $\pm 10V$ analog signal range
- Low propagation delay time: 600ps
- Low on resistance: 30Ω
- Low feedthrough and feedback transients
- Ion implanted for greater reliability
- High channel-to-channel isolation: 107dB
- Transient protection for gates
- Military qualifications pending

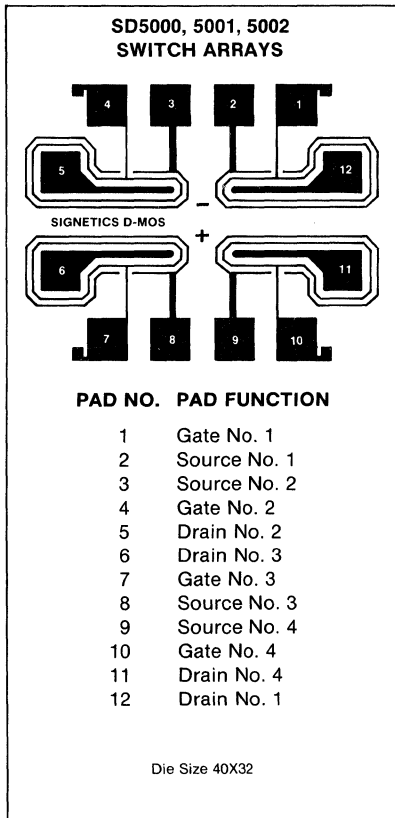
APPLICATIONS

- SD5000 applications
 - Analog switching (up to very high frequencies)
 - Audio routing
 - Choppers
 - Crosspoint switches
 - Sample and hold

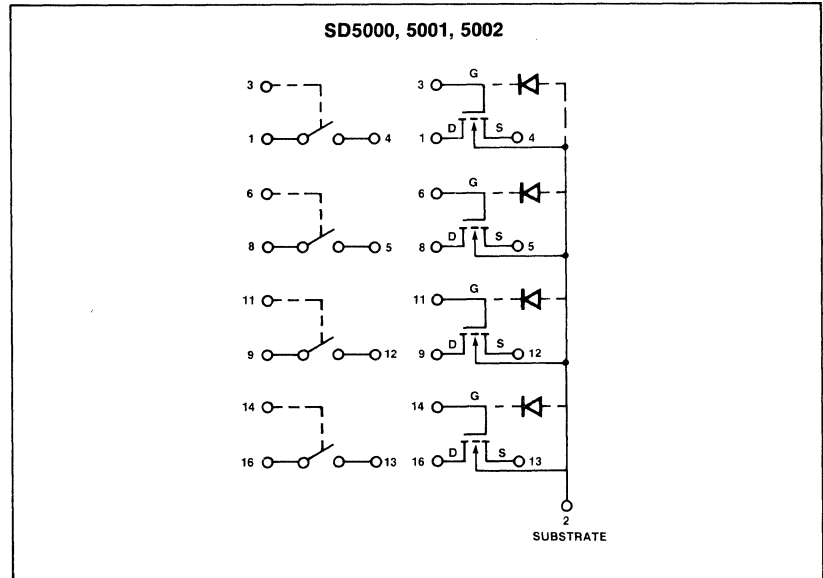
PIN CONFIGURATIONS



CHIP DIAGRAM



FUNCTIONAL AND SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER		SD5000	SD5001	SD5002	UNIT
V_{DS}	Drain-to-source	+20	+10	+15	Vdc
V_{SD}	Source-to-drain ¹	+20	+10	+15	Vdc
V_{DB}	Drain-to-substrate	+25	+15	+22.5	Vdc
V_{SB}	Source-to-substrate	+25	+15	+22.5	Vdc
V_{GS}	Gate-to-source	+30	+25	+30	Vdc
		-25	-15	-22.5	
V_{GB}	Gate-to-substrate	+30	+25	+30	Vdc
		-0.3	-0.3	-0.3	
V_{GD}	Gate-to-drain	+30	+25	+30	Vdc
		-25	-15	-22.5	
I_D	Drain current	50	50	50	mA
Ambient temperature range					
	Storage	-55 to +150			$^\circ\text{C}$
	Operating	0 to +85			$^\circ\text{C}$
Power Dissipation					
	Total package dissipation ²	640			mW
	Individual transistor dissipation	300			mW

NOTES

1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5mW per degree centigrade.

DC ELECTRICAL CHARACTERISTICS $T_A = +25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD5000			SD5001			UNIT		
		Min	Typ	Max	Min	Typ	Max			
BREAKDOWN VOLTAGE										
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V, I_S = 10\text{nA}$		20	25		10	25	V	
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V, I_D = 10\text{nA}$		20			10		V	
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V, \text{source Open}$ $I_D = 10\text{nA}$		25			15		V	
BV_{SB}	Source-to-substrate	$V_{GB} = 0V, \text{drain Open}$ $I_S = 10\mu\text{A}$		25			15		V	
LEAKAGE CURRENT										
$I_{DS(OFF)}$	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +20V$ $V_{DS} = +10V$			1	10		1	10	nA nA
$I_{SD(OFF)}$	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +20V$ $V_{SD} = +10V$			1	10		1	10	nA nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = 30V$ $V_{GB} = 25V$				1			1	μA μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T, I_S = 1\mu\text{A}$ $V_{SB} = 0V$		0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-source-resistance	$I_D = 1.0\text{mA}, V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$			50 30 23 19	70		50 30 23 19	70	Ω Ω Ω Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = +25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD5002			UNIT
		Min	Typ	Max	
BREAKDOWN VOLTAGE					
BV_{DS} Drain-to-source	$V_{GS} = V_{BS} = -5V, I_S = 10nA$	15	25		V
BV_{SD} Source-to-drain	$V_{GS} = V_{BS} = 0V, I_S = 1\mu A$	15			V
BV_{DB} Drain-to-substrate	$V_{GD} = V_{BD} = -5V, I_D = 10nA$				V
BV_{SB} Source-to-substrate	$V_{GB} = 0V, \text{source Open}$ $I_D = 10nA$ $I_D = 1\mu A$	22.5			V
	$V_{GB} = 0V, \text{drain Open}$ $I_S = 10\mu A$	22.5			V
LEAKAGE CURRENT					
$I_{DS(OFF)}$ Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +15V$ $V_{GS} = V_{BS} = 0V, V_{DS} = +10V$		1	10	nA nA
$I_{SD(OFF)}$ Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +15V$		1	10	nA
I_{GBS} Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = 30V$ $V_{GB} = 25V$			1	μA μA
V_T Threshold voltage	$V_{DS} = V_{GS} = V_T, I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	V
$r_{DS(ON)}$ Drain-to-source-resistance	$I_D = 1.0mA, V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$		50 30 23 19	70	Ω Ω Ω Ω

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SD5000			SD5001			UNIT
		Min	Typ	Max	Min	Typ	Max	
g_{fs} Forward transconductance	$V_{DS} = 10V, V_{SB} = 0V$ $I_D = 20mA, f = 1kHz$	10	15		10	15		mmhos
Small signal capacitances								
$C_{(GS+GD+GB)}$ Gate node	$V_{DS} = 10V, f = 1MHz$ $V_{GS} = V_{BS} = -15V$ See capacitance model in Figure 1		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$ Drain node			1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$ Source node			3.5	4.0		3.5	4.0	pF
C_{DG} Reverse transfer			0.3	0.5		0.3	0.5	pF
C_T Cross talk	See test circuits no. 1 and 2, $f = 3kHz$		-107			-107		dB

AC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	SD5002			UNIT
		Min	Typ	Max	
gfs Forward transconductance	$V_{DS} = 10V, V_{SB} = 0V$ $I_D = 20mA, f = 1kHz$	10	15		mmhos
Small signal capacitances					
$C_{(GS+GD+GB)}$ Gate node	$V_{DS} = 10V, f = 1MHz$ $V_{GS} = V_{BS} = -15V$ See capacitance model in Figure 1		2.4	3.5	pF
$C_{(GD+DB)}$ Drain node			1.3	1.5	pF
$C_{(GS+SB)}$ Source node			3.5	4.0	pF
C_{DG} Reverse transfer			0.3	0.5	pF
C_T Cross talk	See test circuits no. 1 and 2, $f = 3kHz$		-107		dB

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ± 10 volts for the SD5000 and ± 7.5 volts for the SD5002. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T , the FET switch starts to turn ON with V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for ± 5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are **isolation, crosstalk between switches, feed-through and feedback transients, insertion loss and speed of operation.** The SD5000 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically 30Ω and OFF resistance is typically $10^{10}\Omega$, which results in an OFF to ON resistance ratio in excess of 10^9 . Isolation from output to input from 3kHz analog signals is typically -107dB.

Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example, for 600Ω source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5000 switches turn ON at sub-nanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

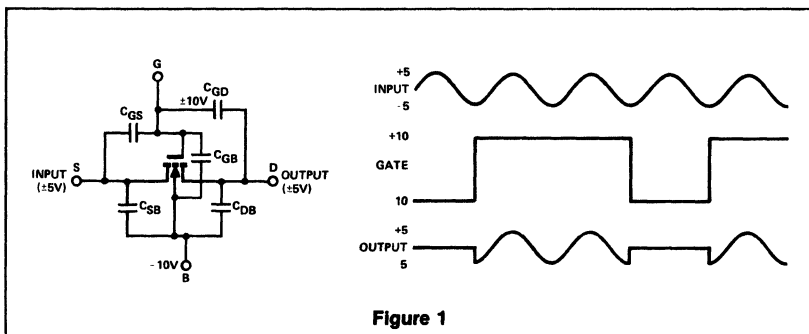
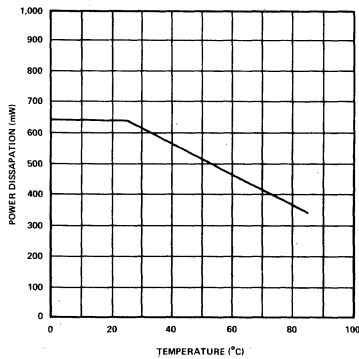


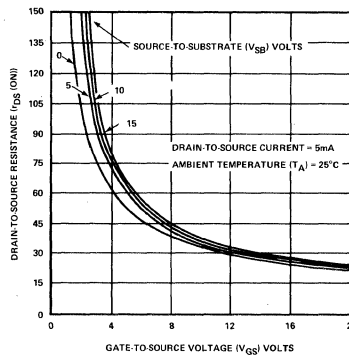
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS

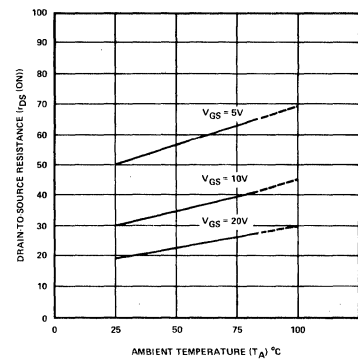
MAXIMUM POWER DISSIPATION vs TEMPERATURE



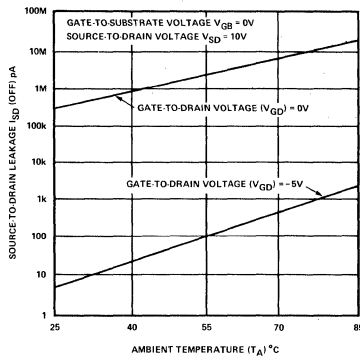
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE AND SOURCE-TO-SUBSTRATE VOLTAGE



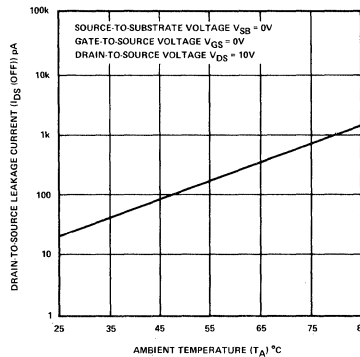
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



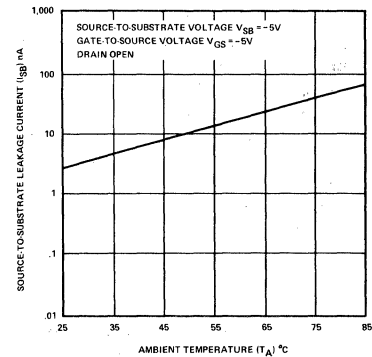
SOURCE-TO-DRAIN LEAKAGE CURRENT vs TEMPERATURE



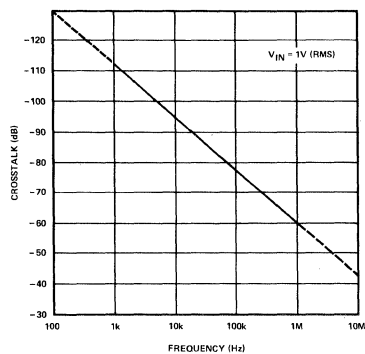
DRAIN-TO-SOURCE LEAKAGE CURRENT vs TEMPERATURE



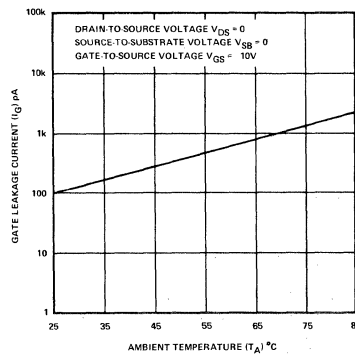
SOURCE-TO-SUBSTRATE LEAKAGE CURRENT vs TEMPERATURE



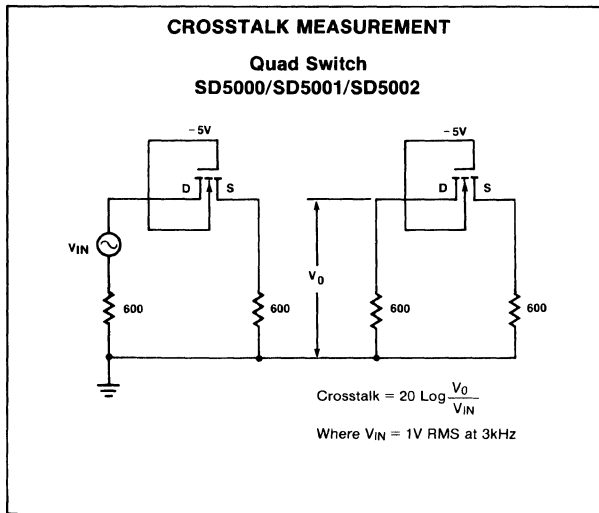
CROSSTALK vs FREQUENCY



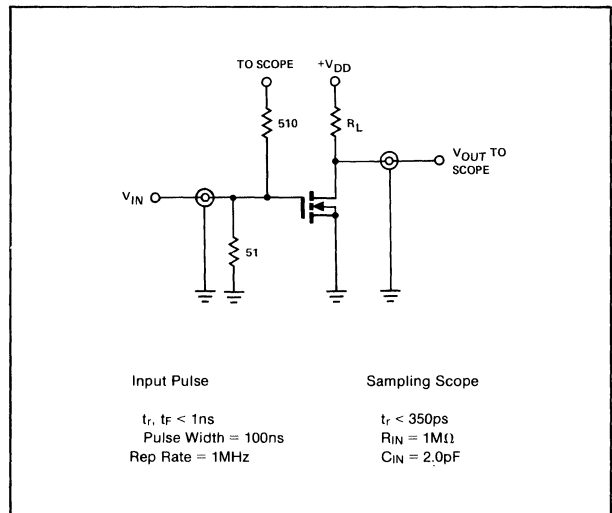
GATE LEAKAGE CURRENT vs TEMPERATURE



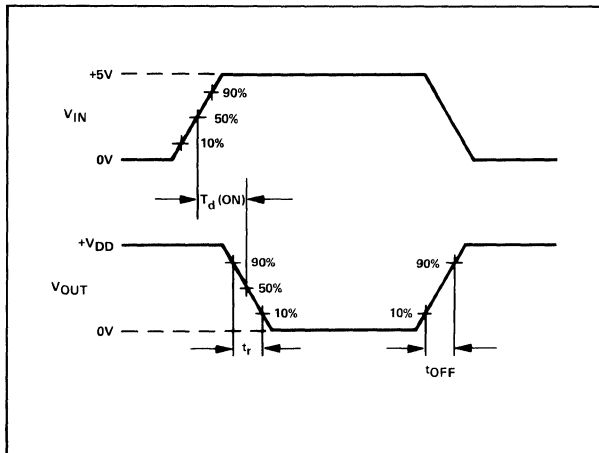
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS

V _{DD}	R _L	t _d (ON) (ns)		t _r (ns)		t _{OFF} (ns)*	
		TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SECTION 16 INDUSTRIAL CONTROLLERS

Section 16—INDUSTRIAL CONTROLLERS

NE5522 Universal Analog Controller 493

DESCRIPTION

The Signetics NE5522 may be used in a wide range of industrial applications where closed loop control of machine speed and acceleration is required. Uses such as conveyor systems, web infeed for plastic film or paper sheet, wire reel take-up and many other process motion control areas, which involve the predetermined ramp up and final speed setting under closed-loop control, can be handled by the Universal Controller.

Inputs to the device are discrete voltage level commands which tell the controller what function is desired such as "Set Memory", "Memory Erase", "Positive Ramp", "Compare to Memory", etc. The closed loop control function is accomplished by an A-C tachometer frequency representative of the speed of the system being fed into the NE5522 where it is compared with an internal reference voltage after being processed by the F/V converter. An error signal is then generated which governs the corrective response of the output. The output function consists of three buffered open collector transistor ports which provide gating and on-off commands to peripheral circuitry. An analog error output is also available for interface with linear control systems.

Basically the NE5522 consists of a frequency to voltage converter, an internal reference oscillator, D to A converter, an I²L logic encoder-decoder and 256 bit F/V D.C. level data storage.

The nominal supply voltage is +8.2V with a range of 7.4 to 9 volts allowed. Current drain is nominally 20mA for an 8.2V supply.

A typical operation sequence might be to bring a motor up to speed using the program accel mode. This would be accomplished by setting pin 3 (Command Input) to $\approx .55V_{CC}$. A ramp function determined by R20-C11 (pins 14, 15) then automatically programs the error system to drive up at a fixed rate. Once the desired speed is reached a voltage of $.75V_{CC}$ is momentarily impressed on the command input and the motor speed will then be controlled to stay at that level previously programmed in memory. Note that a voltage level of $1.1V_{CC}$ must be applied momentarily to the command input (pin 3) upon initial turn-on in order to enable the device.

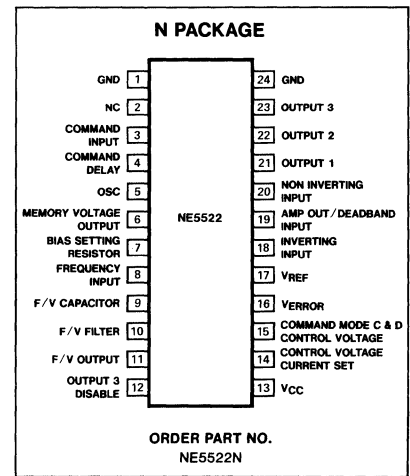
FEATURES

- Adjustable system gain
- Adjustable frequency sensitivity
- Adjustable ramp rate
- Voltage programmable command modes
 1. On
 2. Positive ramp and hold
 3. Compare to set memory
 4. Memory erase
 5. Set memory
 6. Off

APPLICATIONS

- Conveyor Controller
- Web infeed controller
- AC or dc motor speed control
- Actuator control loop
- Engine speed control
- Process control
- Magnetics tape transport control
- Mag/floppy disc controller

PIN CONFIGURATION



TRUTH TABLE

PIN 3 COMMAND INPUT VOLTAGE	MODE	FUNCTION
Greater than $1.1V_{CC}$	ON	ON
$.900V_{CC}$ to V_{CC}	A	Set memory after command C or D.
$.725V_{CC}$ to $.8V_{CC}$	B	Compare to set memory.
$.482V_{CC}$ to $.599V_{CC}$	C	Positive ramp.
$.148V_{CC}$ to $.272V_{CC}$	D	Memory erase.
Less than $.094V_{CC}$	OFF	OFF

TRUTH TABLE

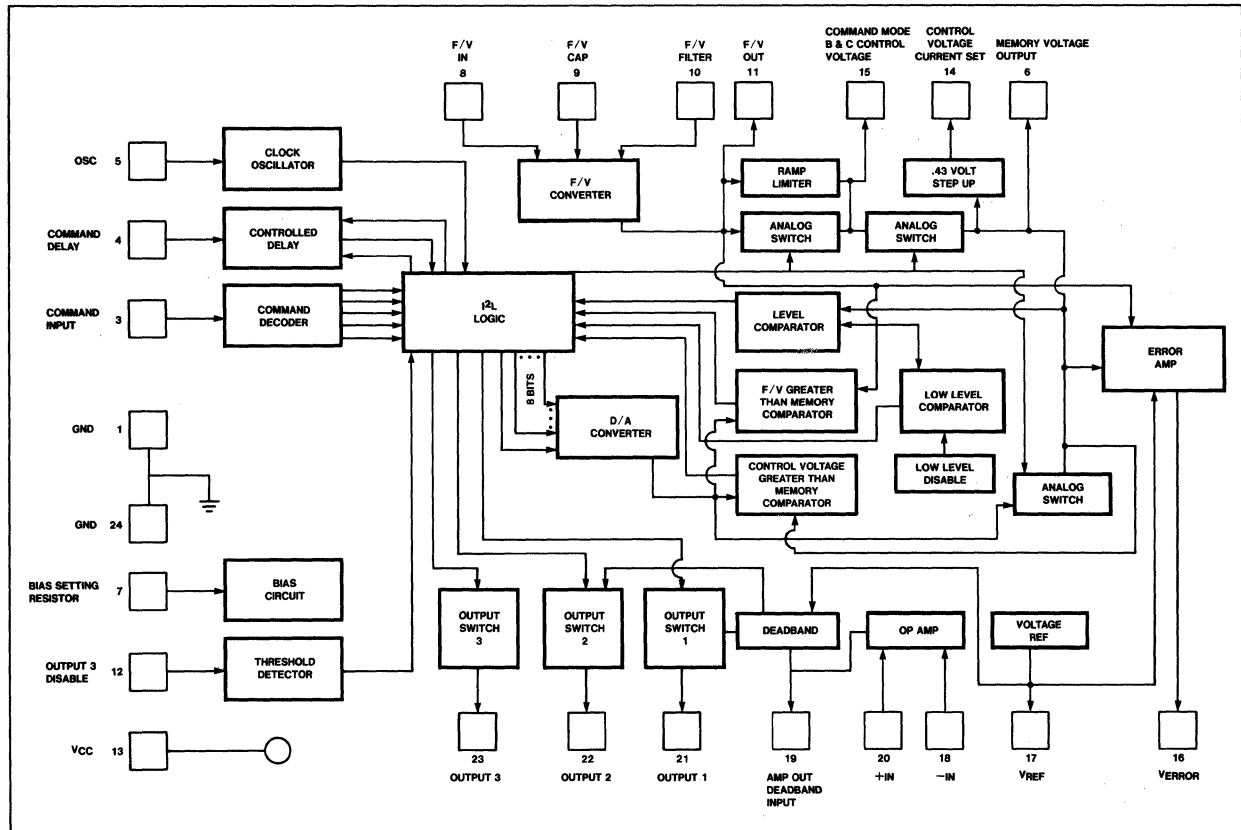
COMMAND MODE INPUT SEQUENCE	OUTPUT 1	OUTPUT 2	OUTPUT 3	V ₆ (MEMORY)
OFF	L	L	H	< 1V
ON/C	H	H	L	< 1V
ON/C/A ($V_S \ll V_M$)	H	H	L	V _F /V
ON/C/A ($V_S \gg V_M$)	L	L	L	V _F /V
ON/C/A/D	L	L	H	< 1V
ON/C/A/D/A ($V_S \ll V_M$)	H	H	L	V _F /V
ON/C/A/D/A ($V_S \gg V_M$)	L	L	L	V _F /V
ON/D/A/disable	L	L	H	V _F /V
ON/C/A/DIS/B ($V_S \ll V_M$)	H	H	L	V _F /V
ON/C/A/DIS/B ($V_S \gg V_M$)	L	L	L	V _F /V

NOTES
 V_S = F/V Output
 V_M = Memory Voltage
 Disable = Pin 12, Output 3
 Command Delay Equations: t_d (All except command B) = $45K(C_4)$, $t_{d(B)}$ = $305K(C_4)$, $C_4 > .05\mu$

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature	0 to +70	°C
Storage temperature	-65 to +150	°C
Supply voltage	9	V

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

(1) **Input Power (V_{CC})**—A regulated power source of 8.2 volts ± 10% must be applied between pin 13 and ground. Pins 1 and 24 are the IC ground pins. Pin 2 should be connected to ground also. Standby current drain is typically 20mA. A resistor of 43kΩ ± 5% must be connected between pin 7 and ground to establish the internal current sources.

(2) **Frequency-to-Voltage Converter**—The F/V input signal for this device is applied to pin 8. It may be in the form of any periodic wave with approximately 50% duty cycle at the zero crossings. Peak amplitudes greater than ± 2 volts should be current limited by a resistor in series with pin 8. Maximum currents should not exceed 1mA. This input is internally amplified and limited at the zero crossings (refer to typical test circuit).

A capacitor, C₆, must be applied from pin 9 to ground. A capacitor, C₇, and resistor, R₁₈, must be applied in parallel between pin 10 and ground. A voltage will then appear on pin 11 with a d-c level, V_S, proportional to

the input frequency, and a sawtooth ripple frequency equal to twice the input frequency, f_s. V_S and the peak-to-peak ripple amplitude, V_r, are given approximately by the following equations:

$$V_S = (4 \text{ volts}) (R_{18}) (C_6) (f_s)$$

$$V_r = (2 \text{ volts}) \left(\frac{C_6}{C_7} \right) \left[1 - (80k\Omega) C_6 f_s \right]$$

The maximum linear value of V_S is typically (V_{CC} - 1.0 volt). The maximum input frequency for linear output is given by:

$$f_s \text{ max} = \frac{1}{(80k\Omega) C_6}$$

assuming symmetrical zero crossings in the input wave. A resistor of no less than 10kΩ from pin 11 to ground is allowable to maintain bias on the NPN emitter follower output stage.

The pin 11 voltage is applied internally to the positive input of the servo error amp.

(3) **Input Command Signal (V_C)**—The analog voltage applied to pin 3, V_C, determines the operating mode. This input signal should be current limited and well filtered to avoid

noise pulses triggering spurious operating conditions.

a) **Turn-on**—When power is first applied the part normally comes up in the Off state. If V_C is raised above V_{CC} so that the input current exceeds 100μa (in the current limited mode), the internal logic circuitry will go into the standby mode and be ready to receive other input commands.

b) **Standby**—To maintain the part in the standby or control mode, V_C should be maintained in the voltage range for mode A as indicated in the table.

c) **Positive Ramp, Set**—The voltage that appears on pin 6, V_m, is the internally generated servo drive voltage. This voltage is internally connected to the negative input of the servo error amp.

When V_C is in mode C as indicated in the table, the voltage V_m will increase at a rate given by (0.43 volts)/R₈C₁, where R₈ is the resistor between pins 14 and 15, and C₁ is the capacitor between pin 15 and ground. The capacitor must have a leakage at 8 volts of much less than 0.43v/R₈ under all

conditions to minimize the variability of this rate. Rates as low as 50mv/sec are practical.

When V_C is restored from mode C to mode A, the value of the pin 11 voltage, V_S , is stored in the internal memory, and this voltage then appears on pin 6 as the servo drive voltage, V_m .

The mechanism by which the value of V_S is stored is as follows. A digital counter whose output is applied to a DAC is turned on. When the DAC output reaches the level of V_S , the counter is stopped, and the DAC output appears on pin 6. The frequency that the counter counts is generated by an internal oscillator connected to a capacitor on pin 5. The oscillator frequency is inversely proportional to capacitor size, and .001 μ f produces about 75 kHz. This frequency determines the time that it takes for the DAC output to reach the V_S level and set. Since the maximum count is 256, a frequency of 75kHz (period = 13.3 μ s) provides a maximum set time of 3.4ms. Frequencies higher than 100kHz are not recommended.

d) Disable, Return to Memory—For normal servo and logic operation the voltage on the Disable input, pin 12, must be less than $V_{CC}/2$. If this voltage is raised above $V_{CC}/2$, the device reverts to the standby mode, except that the internal memory voltage, V_m , remains set at its current level. If the input command voltage, V_C , is then reduced momentarily to mode B, as given in the table, the servo drive voltage, V_m , on pin 6 will start at the current value of V_S and increase at the positive ramp rate described earlier until it reaches the level stored in memory. It will then remain at this value. A Disable-Return sequence when V_S is greater than the memory level will restore V_m to the memory level.

e) Memory Erase, Set—If the value of V_C is reduced to mode D given in the table, the part will revert to the standby mode and memory is erased. If V_C then returns to mode A, the memory and the servo drive voltage, V_m , will be set at the current value of V_S in the same manner as described earlier for the Positive Ramp, Set function.

f) Off—If the value of V_C is reduced to the Off level as given in the table, the device reverts to the inactive state until turned on again as described earlier.

g) Low Level Lockout—The device will revert to the standby condition whenever the value of the F/V output voltage, V_S , drops below the LLL0 voltage, which is approximately 1.5 volts. However, the internal memory voltage is maintained. A Disable-Return sequence after V_S again rises above the

LLLO voltage, will return the voltage V_m to the memory level in the manner described earlier.

h) Command-Delay—When the command voltage, V_C , changes from the standby level as described above, the logic will not see the change for a period of time given in all but one case by the following equation:

$$t_d = \frac{V_{CC} C_3}{(182\mu a)},$$

where C_3 is a capacitor that must be inserted between pin 4 and ground. $C_3 = .68\mu$ f produces a delay of $t_d = 30$ ms with nominal V_{CC} . The exception to this formula is the delay for the Return to Memory function. This delay is given by:

$$t_{dr} = \frac{V_{CC} C_3}{27 \mu a},$$

so that a typical delay with $C_3 = .68\mu$ f is 200ms. These delays are designed to eliminate switch bounce problems, as well as other noise that might appear on the input command signal. In a relatively noise free environment, C_3 may be small, reducing the delay times.

(4) Error Amplifier—This amplifier has a gain of approximately unity. The differential inputs are connected as described above, so that the output, which appears on pin 16, is approximately $V_S - V_m$. The current drawn from pin 16 should be less than $\pm 50\mu$ a. The maximum linear voltage swing is about ± 0.5 volts. The output is referenced to a level roughly equal $V_{CC}/2$, which is typically equal to the reference level on pin 17. Output currents from pin 17 should also be limited to $\pm 50\mu$ a maximum.

(5) Operational Amplifier—The non-inverting input of this amplifier is pin 20, the inverting input is pin 18, and the output is pin 19. The output is internally connected to the input of the deadband circuit. The output impedance at pin 19 is high, typically 600K, so that for loads on pin 19 of 100K or less, this becomes a transconductance amplifier. The amplifier input impedance is greater than one megohm, and the input bias current is typically less than 1 μ a. Low frequency open circuit output gain is typically 150, with a bandwidth of about 10kHz.

(6) Deadband Circuit—The input of this circuit comes from the Op Amp output, as described above. It is a differential amplifier with the second input internally connected to a voltage approximately equal to $V_{CC}/2$. The input on pin 19 can be forced to any desired level between zero and V_{CC} by external circuitry, if desired, without damaging the part. The maximum drive current required to do this is typically $\pm 100\mu$ a.

The circuit deadband is typically ± 0.6 volts relative to $V_{CC}/2$. The circuit outputs appear on pins 21 and 22. These outputs are activated by the logic circuitry when it is in one of the control modes. If the pin 19 voltage is above the upper deadband level in the active mode, both outputs will be high. If the pin 19 voltage is between the two deadband levels, pin 21 will be high, and pin 22 low. If the pin 19 voltage is below the lower deadband voltage, both outputs will be low.

When deactivated by the logic, both outputs are low. The signal output on pin 23 indicates the logic state and is low when the pin 21 and 22 outputs are active. The pin 21, 22, and 23 outputs are essentially open collector outputs for voltages below 5 volts, with a current sinking capability typically better than 20ma.

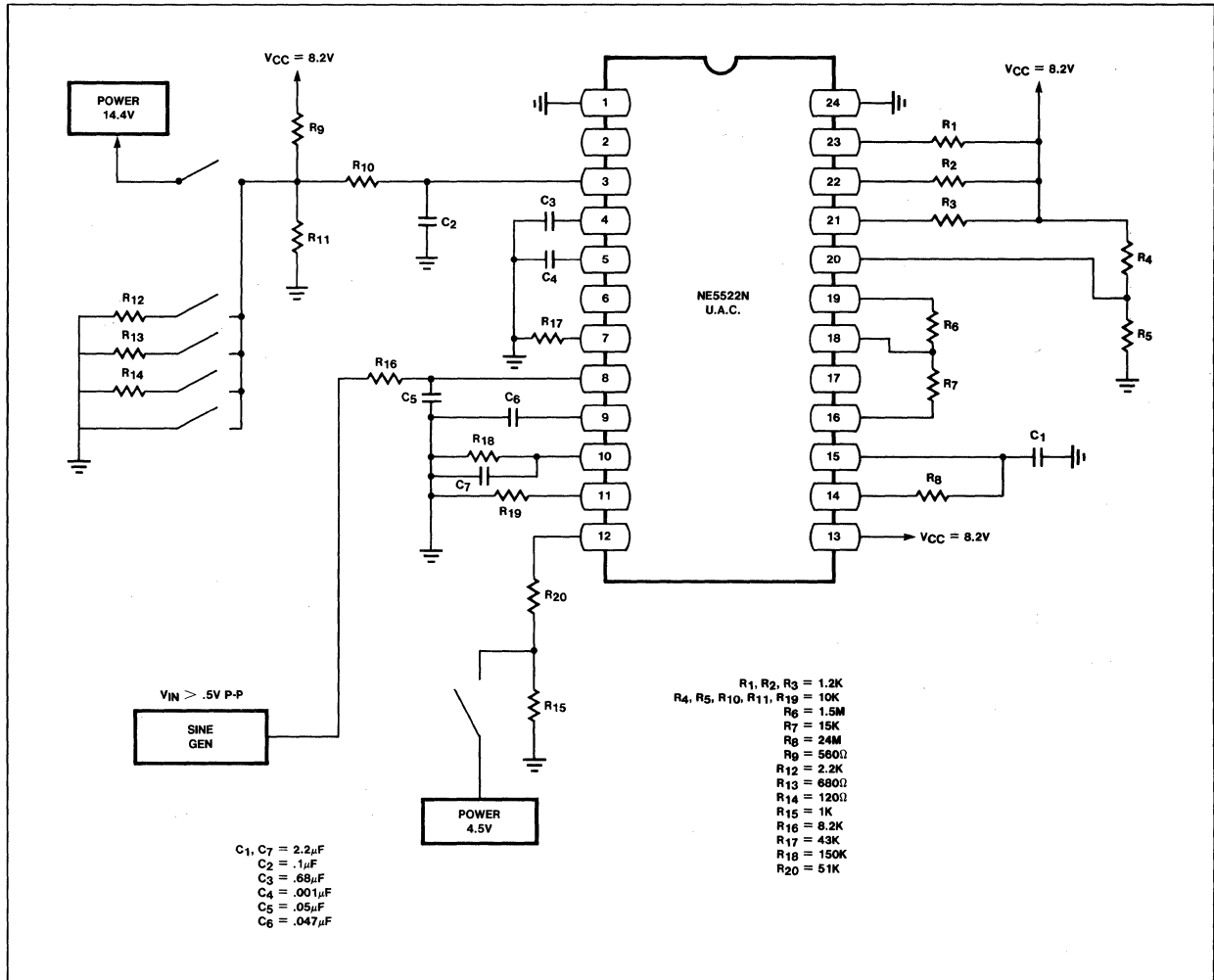
(7) Motor Speed Control—In a typical speed control application an a-c tach signal is fed to the F/V input, pin 8, producing a d-c tach signal on pin 11 (V_S). This is compared to the servo drive voltage, V_m , on pin 6 in the error amplifier. The servo loop gain is established using the op amp with the negative input, pin 18, connected thru a suitable resistor (typically greater than 10k Ω) to the error amp output, pin 16. A feedback resistor between pins 19 and 18 sets the op amp gain. An acceleration feedback signal from the servo is also applied thru a suitable impedance to the negative input, pin 18. The sawtooth ripple from the F/V is amplified by the op amp sufficiently so that it sweeps thru one or both of the deadband circuit thresholds, producing pulse width modulated outputs on pin 21 and 22, the pulse widths increasing as the d-c level at pin 19 increases. The frequency of the pulse width modulation is, of course, the frequency of the ripple, which is twice the input tach frequency.

The pin 21 and 22 outputs are typically applied to some type of "bang-bang" type servo control in such a way that acceleration occurs when both outputs are high and deceleration occurs when both outputs are low.

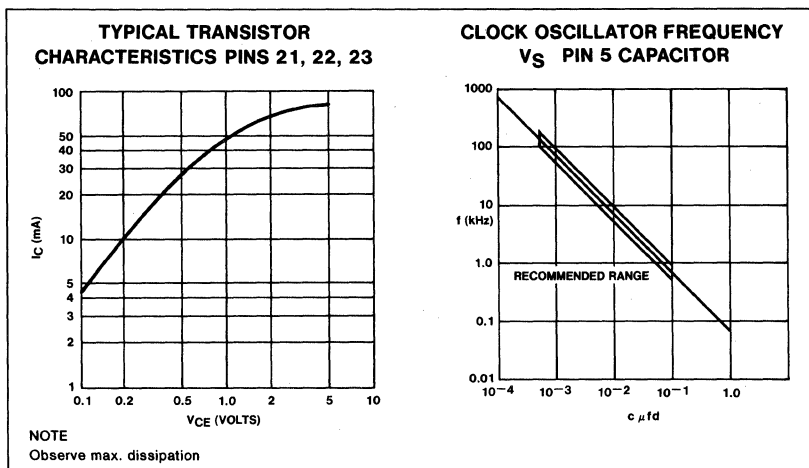
DC MOTOR SPEED CONTROL APPLICATION

This circuit was developed to independently control the speed of two or more model trains running on the same pair of tracks. Each train is equipped with a receiver tuned to a different carrier frequency. The carrier frequency is modulated at the transmitter by a variable audio frequency which carries the speed and direction information. The train which is tuned to the carrier frequency being

TYPICAL TEST CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS



transmitted will receive this signal and provide an enable command to the receiver circuit. The modulating audio frequency signal is demodulated and decoded. Train speed (motor voltage) adjusts to the decoded information. When the carrier frequency is removed the receiver stores the last decoded signal and the train (motor) maintains the set speed until it is again addressed using its carrier frequency and the speed can be adjusted.

THEORY OF OPERATION

(A) Transmitter—The transmitter's carrier frequency was selected to be in the 100 to 500kHz range and the modulating frequency in the 1 to 4kHz range. A simple oscillator/modulator was built using an NE556N dual timer.

The two required frequencies are generated by connecting each timer in the astable

mode. These circuits generated square waves whose frequency is adjusted by changing the variable resistors (figure 2) R_A and R_B respectively. The oscillation frequency is approximately equal to 0.72 divided by the RC product of the charging and discharging path. For the low frequency oscillator: $f_m = .72 / (5K + R_A)(.02\mu)$ and for the high frequency oscillator: $f_c = .72 / (3K + R_B)(500p)$. This gives a carrier frequency which can be adjusted between 110 and 480kHz. Each carrier frequency is adjusted to its receiver frequency which is set by a fixed resistor. This was done to eliminate any adjustments at the receiver. The low frequency is variable between 1 and 3kHz. Modulation of the high frequency by the low is accomplished by connecting the low frequency output to the control voltage input of the high frequency oscillator thru a resistor whose value sets the amount of modulation.

The modulated signal is connected to the train track thru an isolation transformer. A variable resistor R_c is connected in series with the output to adjust the output signal.

(B) Receiver—The receiver is broken down into 5 sections for easier analysis (see figure 1);

- (1) Receiver / Demodulator
- (2) Frequency Converter / Memory
- (3) Decoder
- (4) Motor Driver
- (5) Power Circuits

(1) Receiver / Demodulator (R/D)—An NE567N Phase Locked Loop is used to perform this function. The lock frequency is set by the resistor R whose value is 1.1×10^9 divided by the desired carrier frequency. Two signals from the R/D circuit are used to drive the next circuit block; a logic low level on pin 8 when the tuned carrier frequency is detected and the demodulated low frequency appearing on pin 1.

(2) Frequency Converter / Memory—An NE5522N Universal Analog Controller (UAC) is used for this function. The low frequency signal from the R/D circuit is amplified and applied to the f to V converter of the UAC. A d.c. voltage proportional to the input frequency is generated. The conversion factor is set by the capacitor on pin 9 and the resistor on pin 10; its value is: $V_{dc}/f = 4 R_{10}C_9$. Thus for the circuit values shown, $V_{dc}/f = 1.72mV/Hz$; at 1kHz, 1.72V, at 2kHz 3.44V and 3kHz 5.16V.

When the enable signal is removed (carrier frequency turned off) the converted D.C. voltage is stored and is continuously available on pin 6 of the UAC.

(3) Decoder—An NE324N quad op amp is used to decode the d.c. level from the UAC. One amplifier is connected to give an output which is proportional to the d.c. level. Its output goes to zero at about 3.65V. Another amplifier is connected so that its output is

inversely proportional to the d.c. level below 3.25 volts. A deadband is set so that both amplifier outputs are at zero between 3.25 and 3.65V. A transfer characteristic of these two amplifiers is shown in figure 3.

The remaining two amplifiers are used as comparators, each going high when the amplifier driving it goes positive. Thus when the UAC pin 6 voltage is greater than 3.65V, amplifier (4) and comparator (2) have positive output voltages and when this voltage is less than 3.25V amplifier (3) and comparator (1) have positive output voltages.

(4) Motor Driver—The motor driver consists of four NPN transistors connected in an H bridge configuration. The bases of the upper transistors are driven by the decoder amplifier output voltages which are proportional to the UAC voltage as previously described. The bases of the lower transistors are driven by the decoder comparators and are either on or off depending on the UAC voltage above the deadband, inversely proportional to the UAC voltage below the deadband, and zero in the deadband. A system transfer function is shown in figure 4.

(5) Power Circuits—The power supply for the IC's and the transistor drivers is supplied from a bridge rectifier. The transistor bridge and motor are supplied with rectified unfiltered 60Hz. A filtered, regulated 8 volt d.c. supply is used for the IC's.

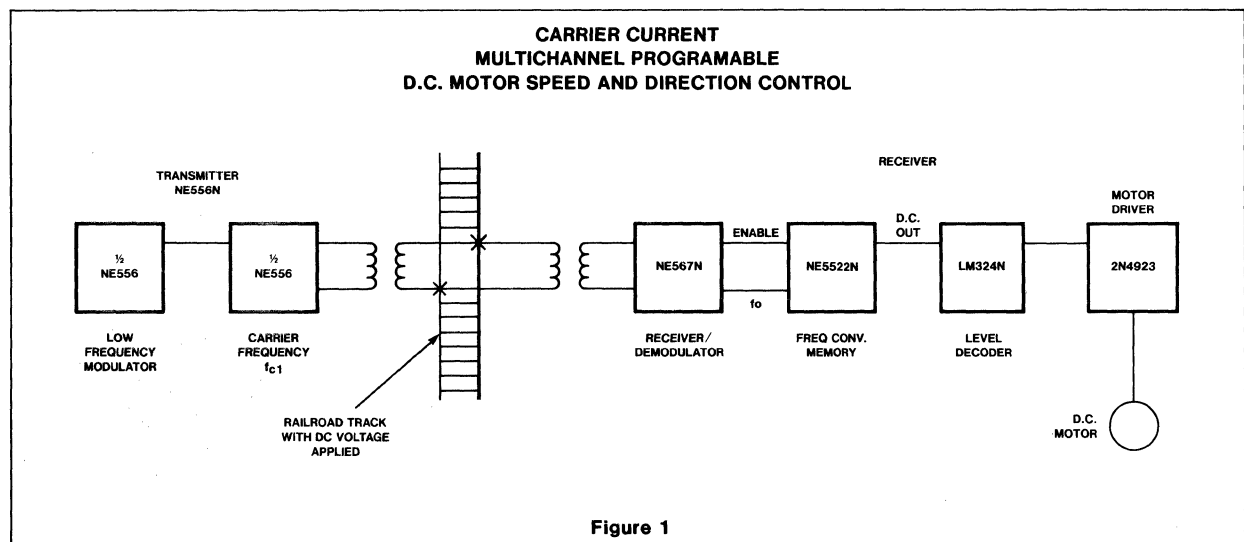
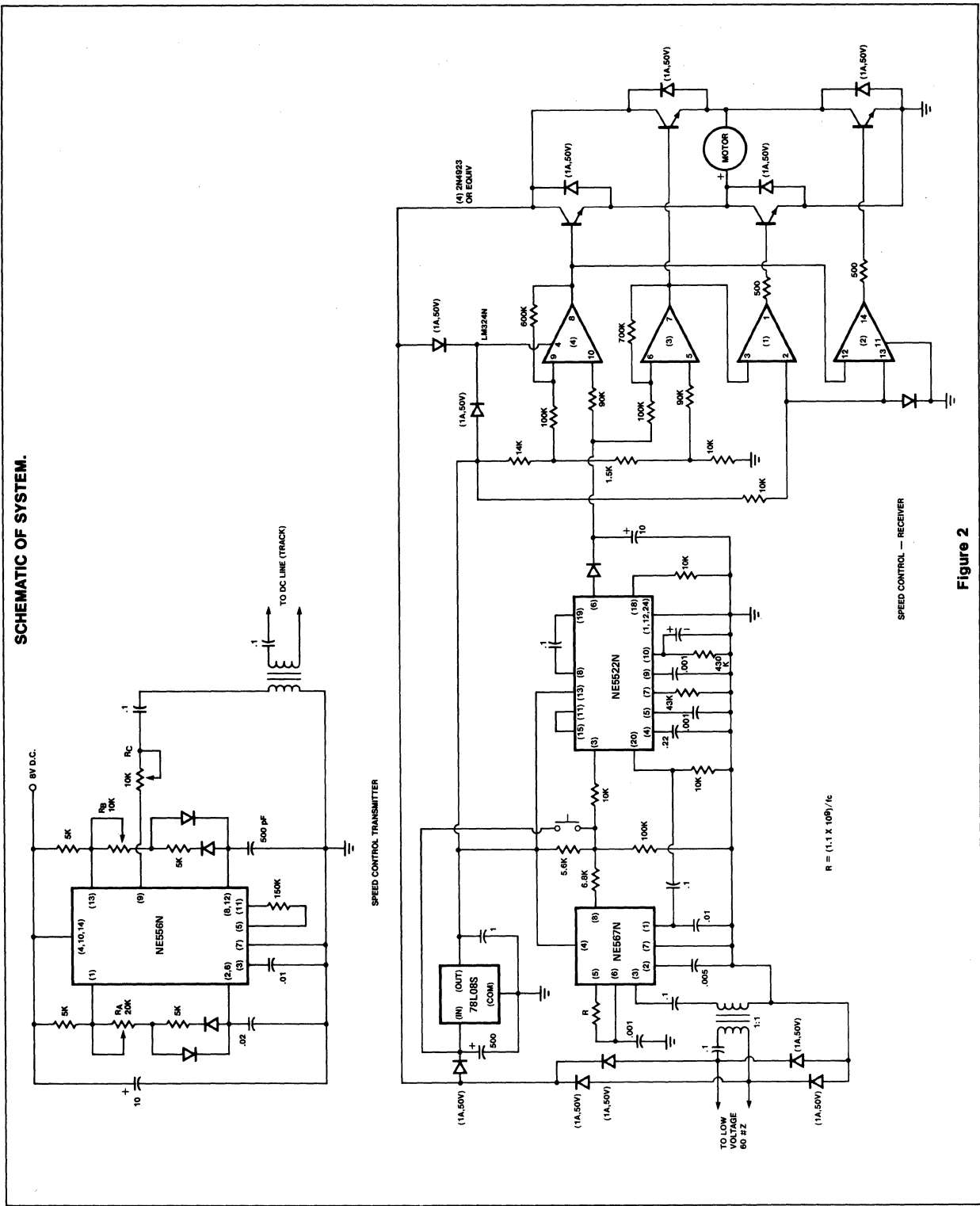
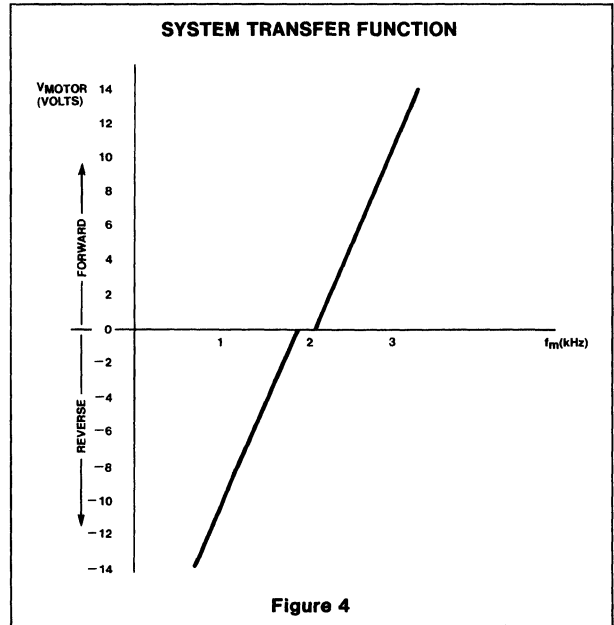
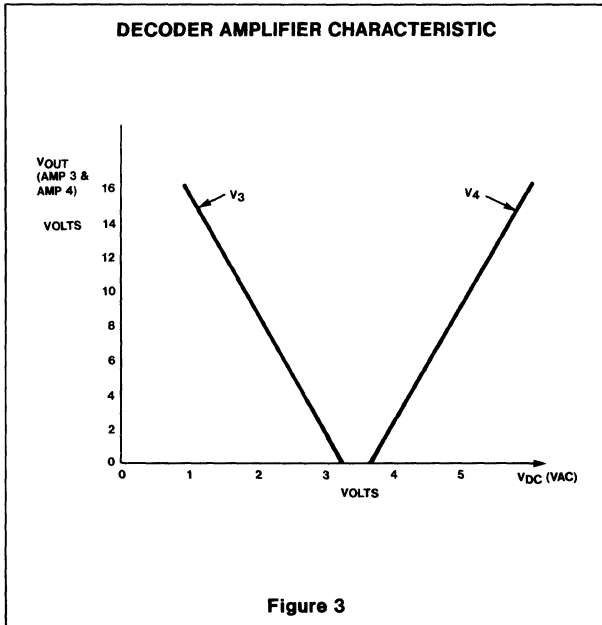


Figure 1

APPLICATION—REMOTE DC MOTOR SPEED CONTROL—MODEL TRAIN

SCHEMATIC OF SYSTEM.





SECTION 17 APPENDICES

MILITARY

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily avail-

able before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond. B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED	QUALIFIES	OPTION 1	OPTION 2
SUB-GROUPS			
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*

Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
1. Pre-Certification						
A. Product Assurance Program Plan						
B. Manufacturer's Certification						
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling*	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	X	X	X	X
*For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)						
9. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10 ⁻⁸ CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ -55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard	10%	10% 3% Funct'I	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510 / XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per pkg. group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per µcircuit type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

LINEAR DEVICES

DEVICE	DESCRIPTION	PACKAGE*	
		DIP	CAN
OPERATIONAL AMPLIFIERS			
LF155	JFET Op Amp		H
LF156	JFET Op Amp		H
LH2101A	Dual Op Amp	F	
LM101/A	Hi Perf Op Amp	F	H
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		H
MC1556	Hi Perf Op Amp	F	H
MC1558	Dual Op Amp	F	H
SE530	Hi Slew Op Amp	F	H
SE532	Dual Op Amp		H
SE5512	Dual Op Amp	FE	H
SE5532	Dual Op Amp	F,FE	H
SE5532A	Dual Op Amp	FE	
SE5534	Lo Noise Op Amp	F,FE	H
SE5534A	Lo Noise Op Amp	FE	H
SE5537	Sample and Hold Amp	FE	H
SE5539	High Freq Op Amp	F	—
μA747	Dual Op Amp	F	H
COMPARATORS			
SE521	Dual Differential Comparator	F	
SE522	Dual Differential Comparator	F	
SE527	Voltage Comparator	F	H
SE529	Voltage Comparator	F	H
LH2111	Dual Voltage Comparator	F	
LM111	Voltage Comparator	F	H
LM139/A	Quad Voltage Comparator	F	
LM193/A	Dual Voltage Comparator		H
DIFFERENTIAL AMPLIFIERS			
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
μA733	Video Amplifier	F	H
PHASE LOCKED LOOPS			
SE567	Tone Decoder PLL	F	H
SE564	Phase Locked Loop	F	H
TIMERS			
SE555	Timer	F,FE	H
SE556-1	Dual Timer	F	
SE558	Quad Timer	F	

DEVICE	DESCRIPTION	PACKAGE*	
		DIP/ CAN	CAN
VOLTAGE REGULATORS			
SE5553	Dual Track Reg	F	H
SE5554	Dual Track Reg	F	H
μA723	Adj Volt Reg	F	H

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
D to A CONVERTERS			
DAC-08	8-Bit Mult DAC	F,Q	H
MC1508-8	8-Bit Mult DAC	F	—
SE5008	8-Bit Mult DAC	F	—
SE5009	8-Bit Mult DAC	F	—
SE5018	8-Bit μP-Comp DAC	F	—
SE5019	8-Bit μP-Comp DAC	F	—
SE5118	8-Bit μP-Comp DAC	F	—
SE5119	8-Bit μP-Comp DAC	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
DUAL LINE RECEIVERS			
DS7820/A	Dual Line Receiver	F	—
DS7830/A	Dual Diff Line Driver	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
MOS FET SWITCH			
SD210	Switch N-Channel Enhance	EE	—
SD211	Switch N-Channel Enhance	EE	—
SD5002	Quad Analog Switch	I	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
SMPS CONTROL CIRCUITS			
SE5560	SMPS Controller	F	—
SG1524	Reg Pulse Width Mod	F	—

JAN M - 38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
SE555	10903BCB	F	QPL 1
SE555	10903BPB	FE	QPL 1
SE555	10901BGC	H	QPL 1
SE556-1	10902BCB	F	QPL 1
LH2101A	10105BEB	F	QPL 1
LM101A	10103BCB	F	QPL 1
LM101A	10103BPB	FE	QPL 1
LM101AH	10103BGC	H	QPL 1
μA741	10101BGC	H	QPL 1
μA747	10101BGC	H	QPL 1
LM124	11005BCB	F	1980
DAC-08	11301BCB	F	1980
DAC-08A	11302BCB	F	1980
SE5537			1980
SG1524			1980

NOTES
F = Cerdip
H = TO-5

LINEAR INDUSTRY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μA111	LM111
μA139	LM139
μA733	μA733
μAF155/156	LF155/156
μA101	LM101
μA101A	LM101A
MC1556	MC1556
μA1558	MC1558
μA747	μA747
MC1555	SE555
μA556	SE556
μA109	LM109
μA79XX	79XX(7)
μA723	μA723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1733	μA733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MC1558	MC1558
MC1747	μA747
MC3556	SE556
MLM109	LM109
MC78XX	78XX(7)
MC79XX	79XX(7)
MC1723	μA723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM733	μA733
LF155/56	LF155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM747	μA747
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM109	LM109
LM723	μA723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM733	μA733
LF155/56/57	LF155/156
LM101	LM101
LM101A	LM101A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM747	μA747
RM555	SE555
LM109	LM109
RM723	μA723

T.I.	SIGNETICS
LM111	LM111
SN52733	μA733
LF155/56	LF155/156
SN52101A	LM101A
SN55182	DM7820
SN55183	DM7830
SN52555	SE555
SE556	SE556
LM109	LM109
μA79XX	μA79XX(7)
SN52723	μA723

PACKAGES

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

- Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
- Lead spacing shall be measured within this zone.
 - Shoulder and lead tip dimensions are to centerline of leads.
- Tolerances non-cumulative
- Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

- Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
- Body material: Plastic (Epoxy)
- Round hole in top corner denotes lead No. 1.
- Body dimensions do not include molding flash.
- SO Packages-microminature packages.
 - Lead material: Alloy-42.
 - Body material: Plastic (Epoxy).

Hermetic Only

- Lead material
 - ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
 - ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
 - ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
- Body Material
 - Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
 - Ceramic with glass seal at leads.
 - BeO ceramic with glass seal at leads.
 - Ceramic with ASTM alloy F-30 or equivalent.

12. Lid Material

- Nickel or tin plated nickel, weld seal.
 - Ceramic, glass seal.
 - ASTM alloy F-15 or equivalent, gold plated, alloy seal.
 - BeO Ceramic with glass seal.
- Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
 - Recommended minimum offset before lead bend.
 - Maximum glass climb .010 inches.
 - Maximum glass climb or lid skew is .010 inches.
 - Typical four places.
 - Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION ¹
Standard Dual-In-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NNE NNF	120/60	Slim Line
28	NQ	116/53	MO-015
40	NW	110/50	MO-015
Power Dual-In-Line			
14	NHA ²	95/33	Butterfly
16	NJA ²	95/33	Butterfly
18	NKA ²	90/26	Butterfly
20	NLA ²	90/26	Butterfly
24	NNA ²	60/23	Heatsink
28	NQA ²	56/21	Heatsink
SO Packages			
8	DE	110	SO-8
14	DH	100	SO-14
16	DJ	100	SO-16

NOTES

- Dual-in-Line packages unless otherwise described.
- Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads.

HERMETIC PACKAGES

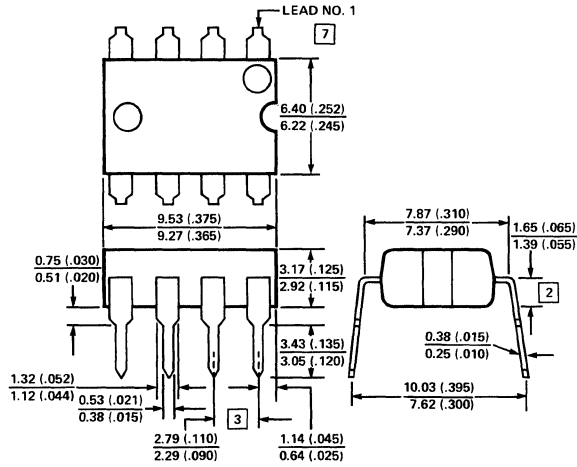
NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION¹
Metal Headers			
3	HBA	100/20	TO-5 Header
4	EC	100/20	TO-46 Header
4	EE	150/25	TO-72 Header
8	HEA/HEB	150/25	TO-5 Header
10	HFB/HFA	150/25	TO-5/TO-100 Header, Short Can
10	HFD/HFC	150/25	TO-5/TO-100 Header, Tall Can
Flat Packs			
10	QF	230/55	Flat Ceramic
10	WF	240/50	Flat Ceramic
14	QHA	185/45	Flat Ceramic Laminate
14	WH	205/50	Flat Ceramic
16	QJA	170/45	Flat Ceramic Laminate
16	RJA	133/30	Flat Ceramic, BeO
16	WJ	200/50	Flat Ceramic
18	RKA	107/22	Flat Ceramic, BeO
24	QNA	155/44	Flat Ceramic Laminate
24	RNA	107/22	Flat Ceramic, BeO
24	WN	155/40	Flat Ceramic
28	RQA	107/22	Flat Ceramic, BeO
40	RWA	95/20	Flat Ceramic, BeO
Cerdip Family			
8	FE	110/30	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	90/25	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA/IKB	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC/INH	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
28	GQ*	90/35	Chip Carrier
40	IWA	55/25	Dip Laminate
44	GX*	75/30	Chip Carrier
48	JY*	55/25	Dual-in-Line Ceramic
50	IZA	42/20	Dip Laminate

*Contact factory for Package drawings.

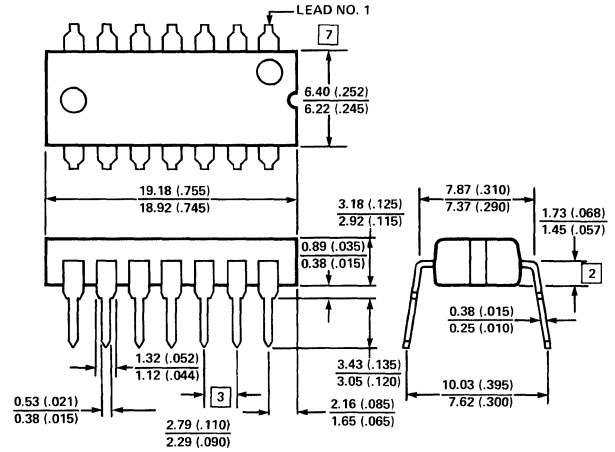
PACKAGES

PLASTIC: Standard and Power Dual-In-Line

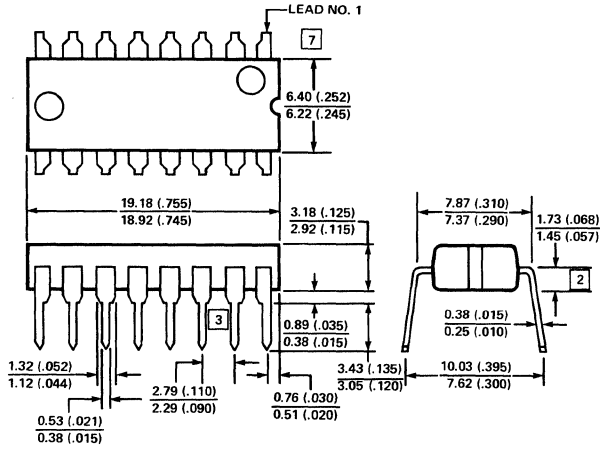
NE Package



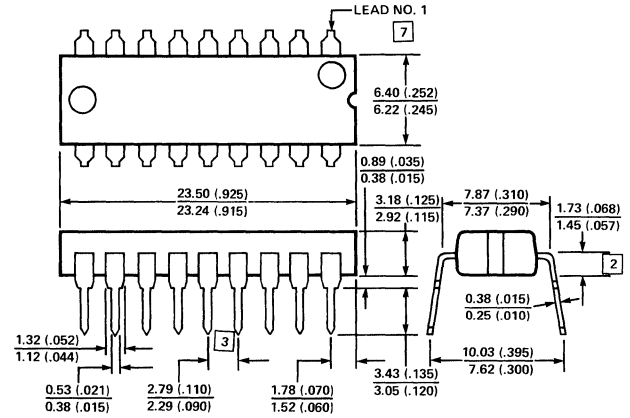
NH Package



NJ Package



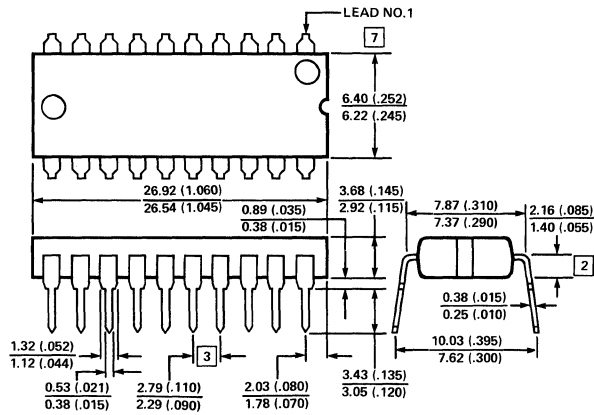
NK Package



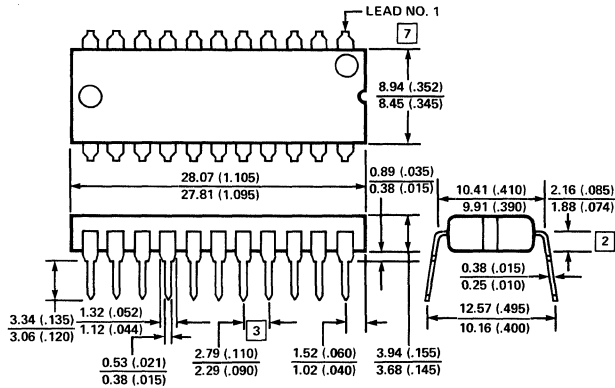
PACKAGES

PLASTIC: Standard and Power Dual-In-Line (cont'd.)

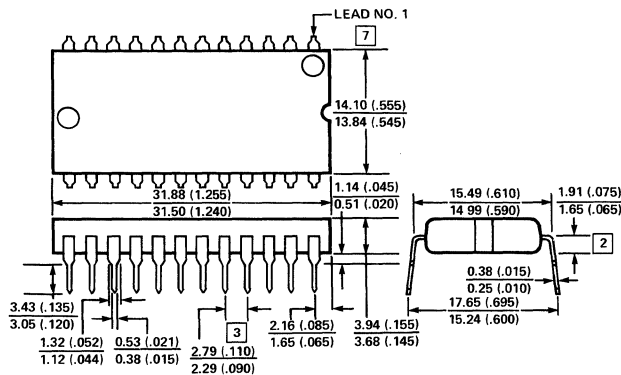
NL Package



NM Package



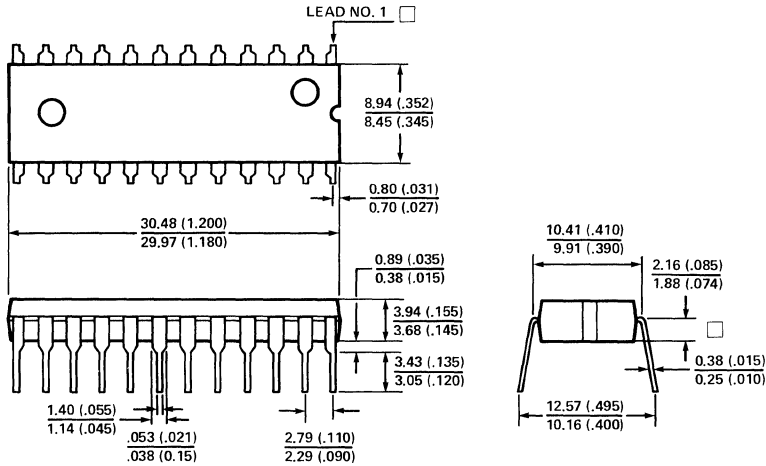
NN Package



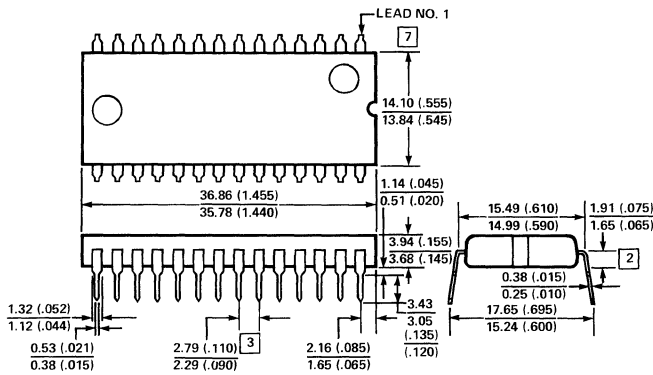
PACKAGES

PLASTIC: Standard and Power Dual-In-Line (cont'd.)

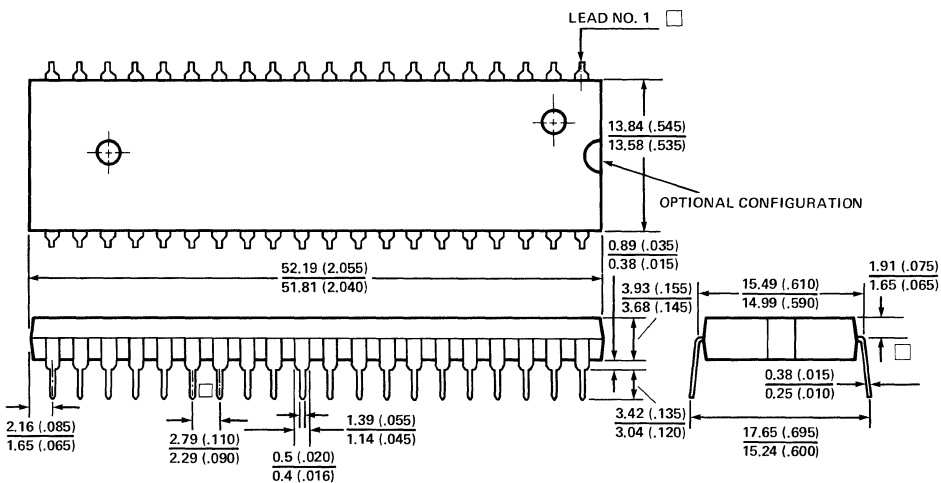
NNE/NNF Package



NQ Package



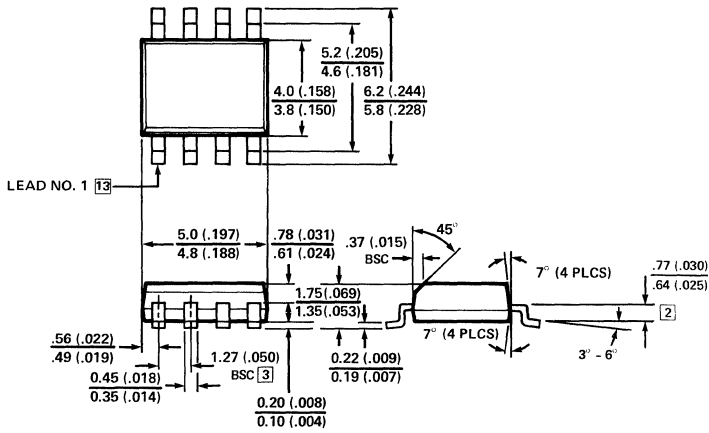
NW Package



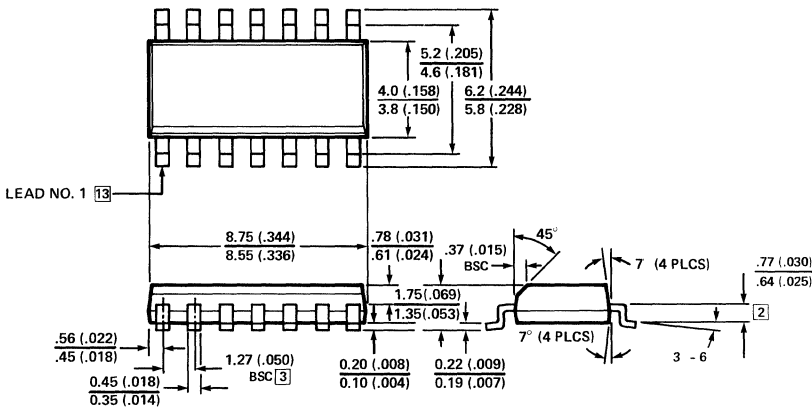
PACKAGES

PLASTIC: SO Packages

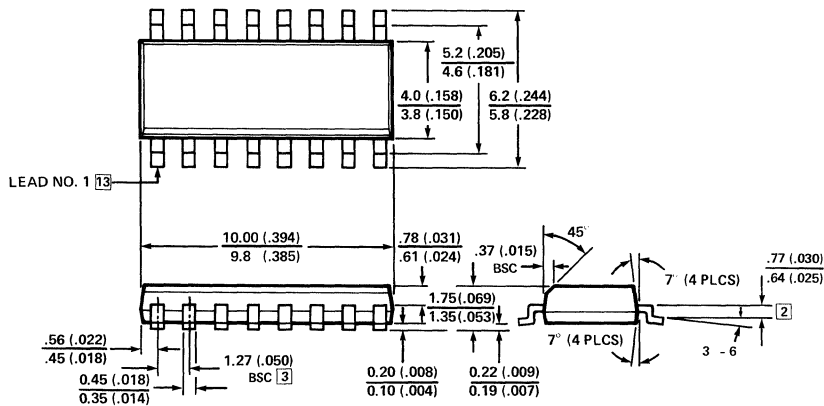
DE Package



DH Package



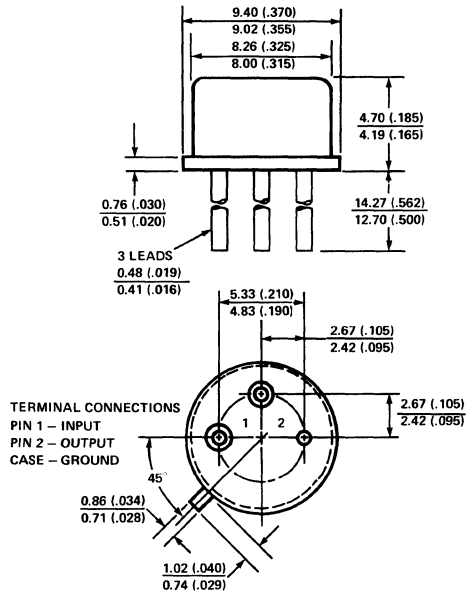
DJ Package



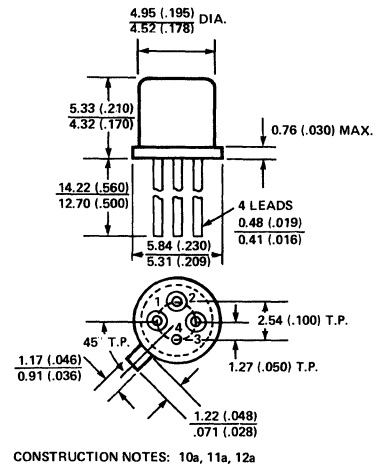
PACKAGES

HERMETIC: Metal Headers

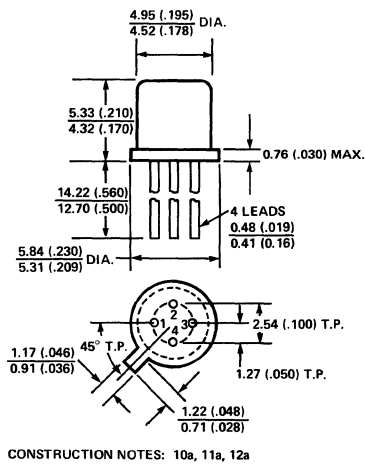
HBA Package



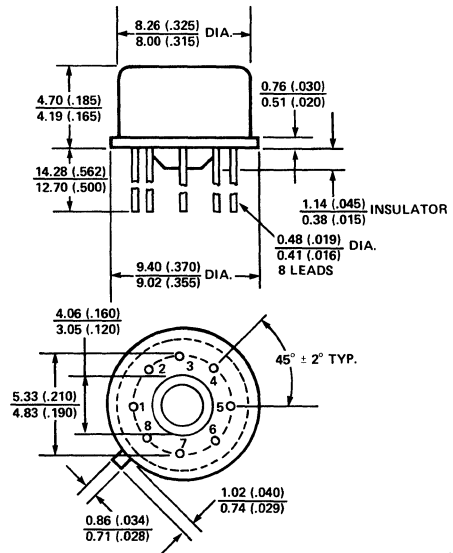
EC Package



EE Package



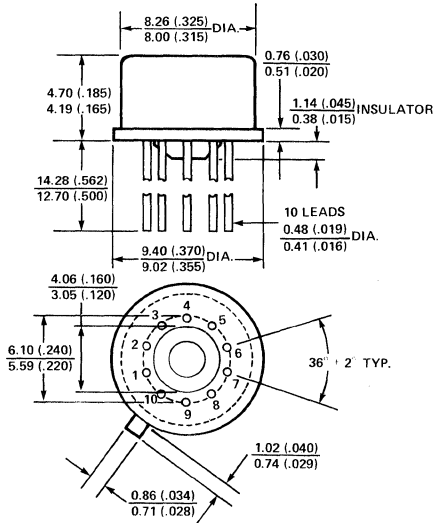
HEA/HEB Package



PACKAGES

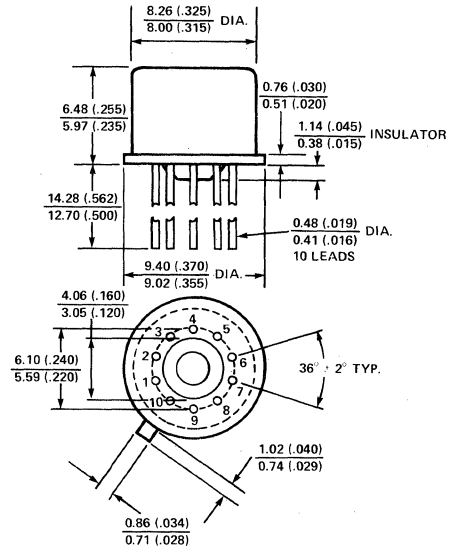
HERMETIC: Metal Headers (cont'd.)

HFB/HFA Package



CONSTRUCTION NOTES: 10a, 11a, 12a

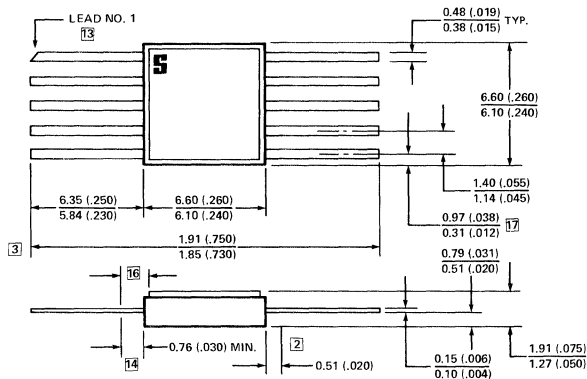
HFD/HFC Package



CONSTRUCTION NOTES: 10a, 11a, 12a

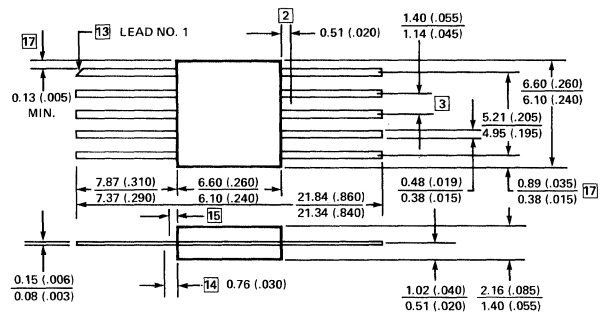
HERMETIC: Flat Packs

QF Package



CONSTRUCTION NOTES: 10c, 11d, 12b

WF Package

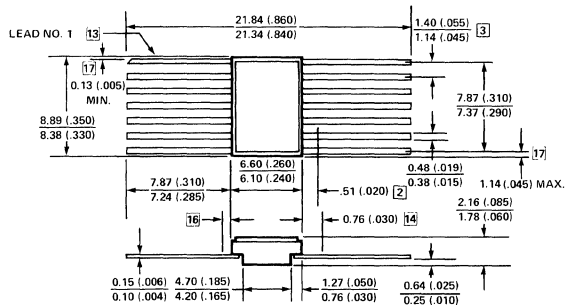


CONSTRUCTION NOTES: 10b, 11b, 12b

PACKAGES

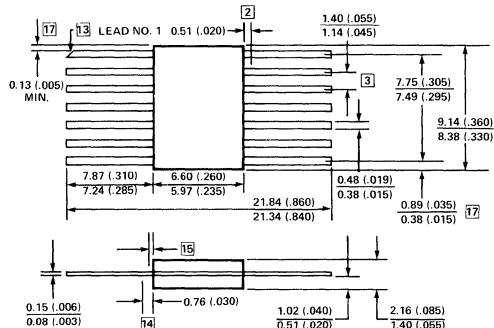
HERMETIC: Flat Packs (cont'd.)

QHA Package



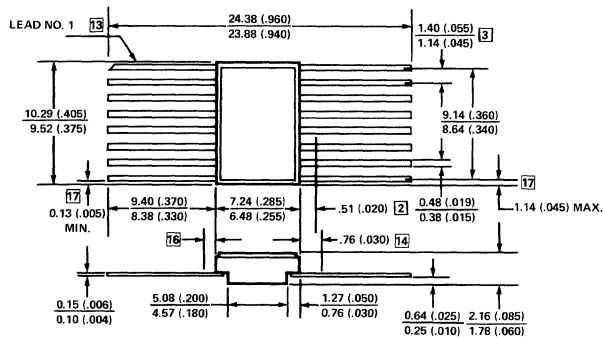
CONSTRUCTION NOTES: 10c, 11d, 12b

WH Package



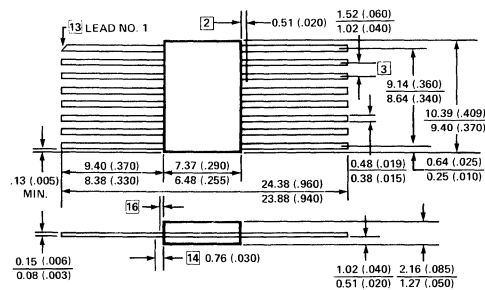
CONSTRUCTION NOTES: 10b, 11b, 12b

QJA Package



CONSTRUCTION NOTES: 10c, 11d, 12b

RJA Package

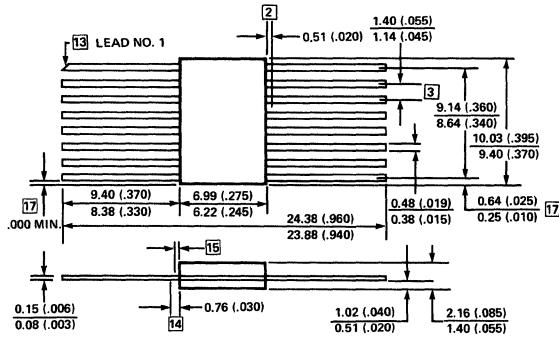


RJA CONSTRUCTION NOTES: 10b, 11c, 12b

PACKAGES

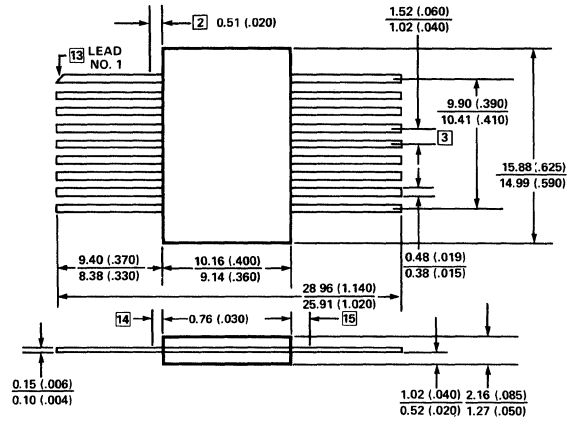
HERMETIC: Flat Packs (cont'd.)

WJ Package



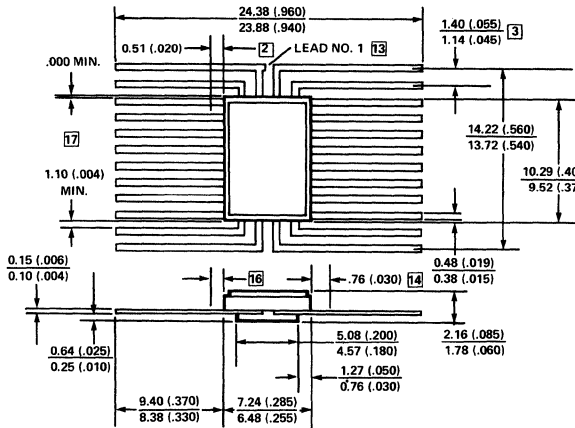
CONSTRUCTION NOTES: 10b, 11b, 12b

RKA Package



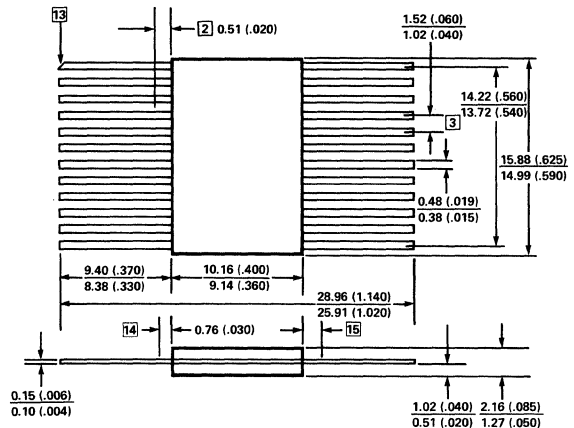
CONSTRUCTION NOTES: 10b, 11c, 12d

QNA Package



CONSTRUCTION NOTES: 10c, 11d, 12b

RNA Package

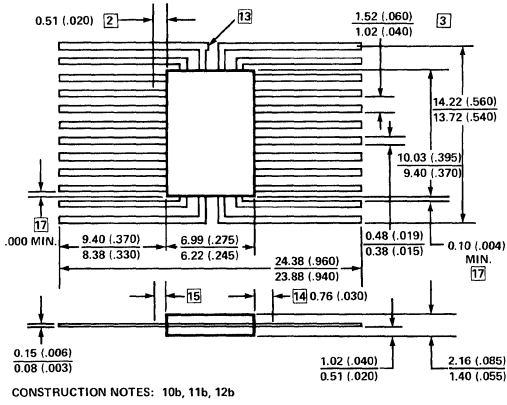


CONSTRUCTION NOTES: 10b, 11c, 12d

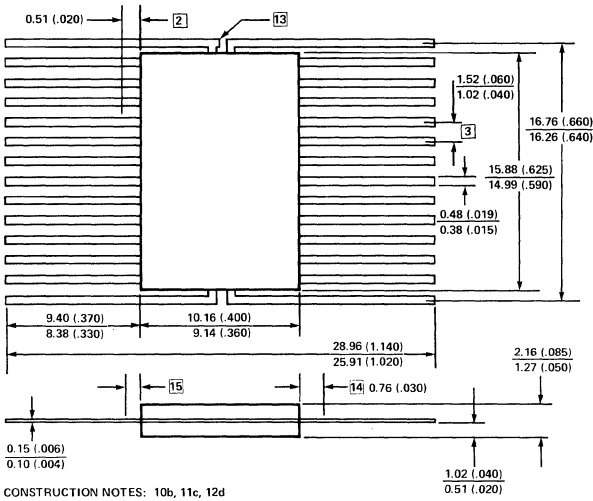
PACKAGES

HERMETIC: Flat Packs (cont'd.)

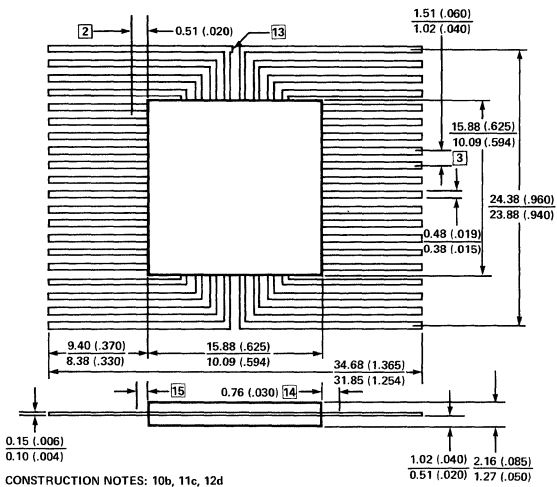
WN Package



RQA Package



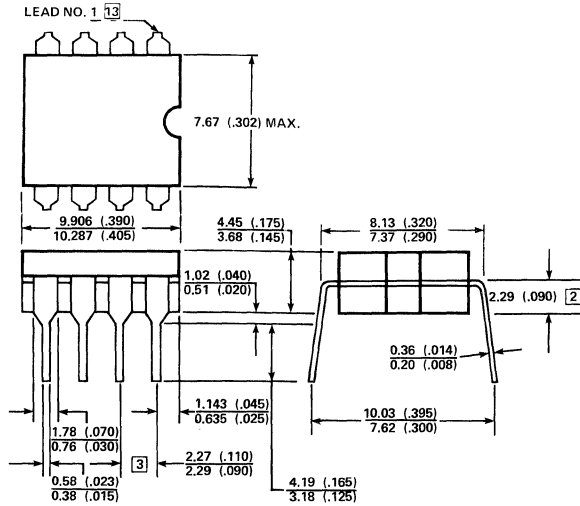
RWA Package



PACKAGES

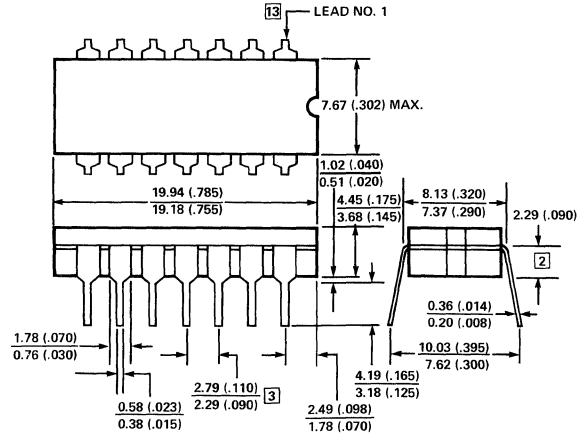
HERMETIC: Cerdip Family

FE Package



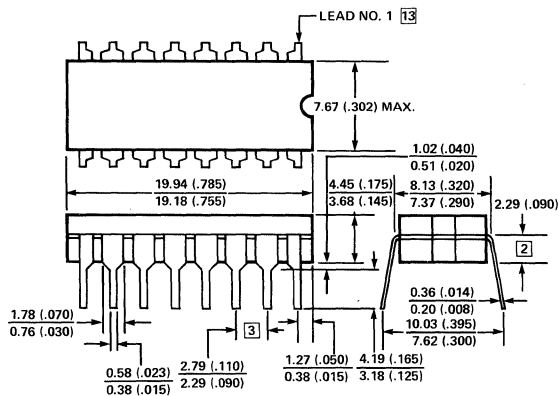
CONSTRUCTION NOTES: 10b, 11b, 12b

FH Package



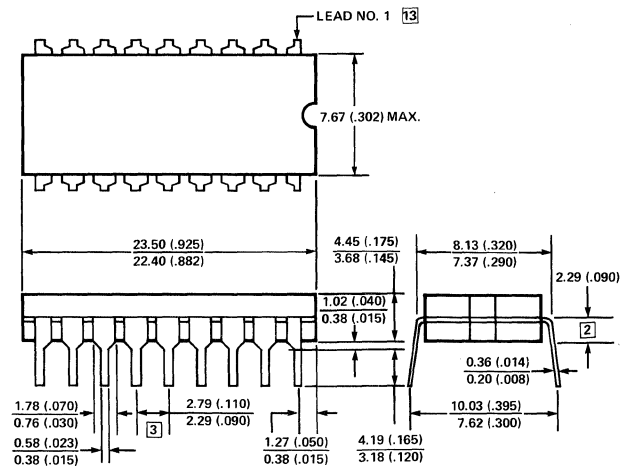
CONSTRUCTION NOTES: 10b, 11b, 12b

FJ Package



CONSTRUCTION NOTES: 10b, 11b, 12b

FK Package

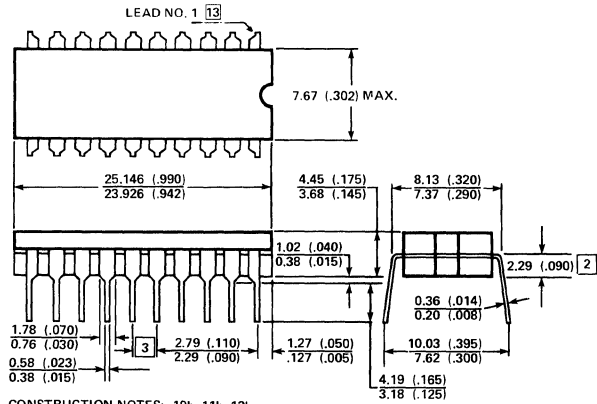


CONSTRUCTION NOTES: 10b, 11b, 12b

PACKAGES

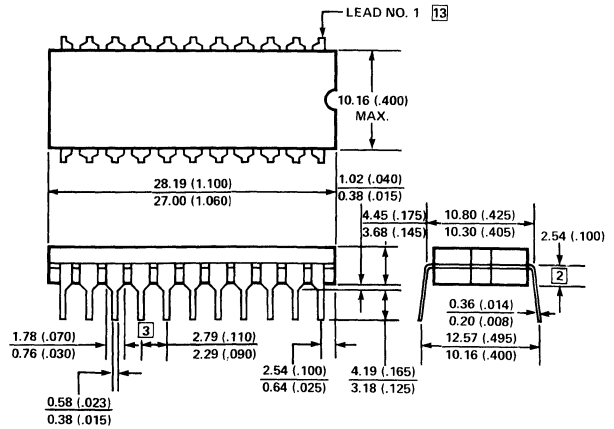
HERMETIC: Cerdip Family (cont'd.)

FL Package



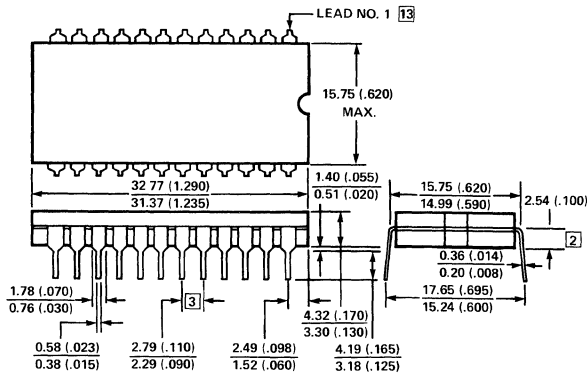
CONSTRUCTION NOTES: 10b, 11b, 12b

FM Package



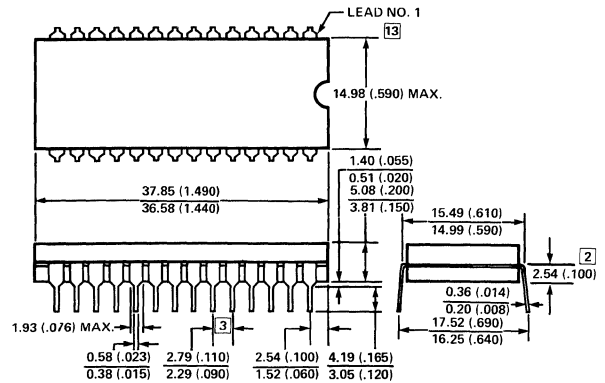
CONSTRUCTION NOTES: 10b, 11b, 12b

FN Package



CONSTRUCTION NOTES: 10b, 11b, 12b

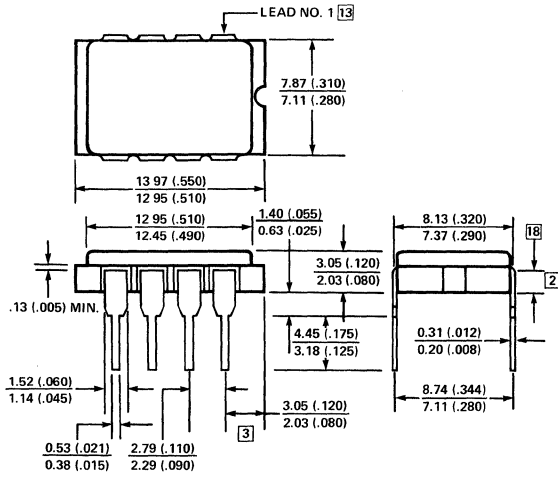
FQ Package



CONSTRUCTION NOTES: 10b, 11b, 12b

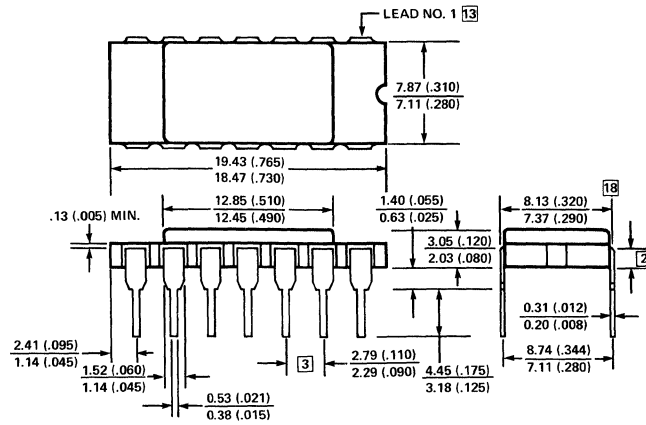
HERMETIC: Laminated Ceramic, Side Braze Lead

IEA Package



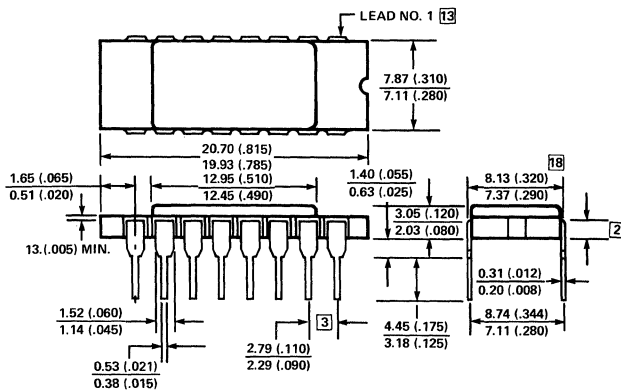
CONSTRUCTION NOTES: 10b, 11d, 12b

IHA Package



CONSTRUCTION NOTES: 10b, 11d, 12b

IJA Package

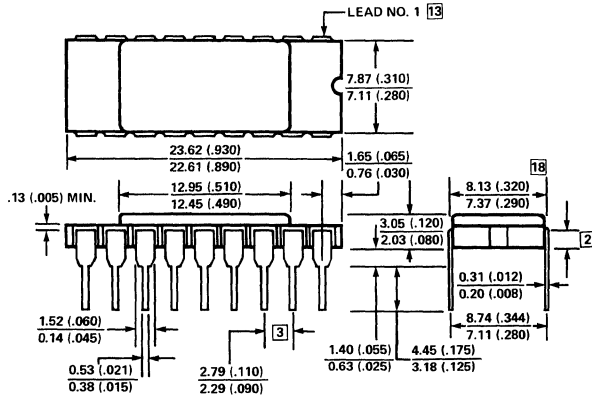


CONSTRUCTION NOTES: 10b, 11d, 12b

PACKAGES

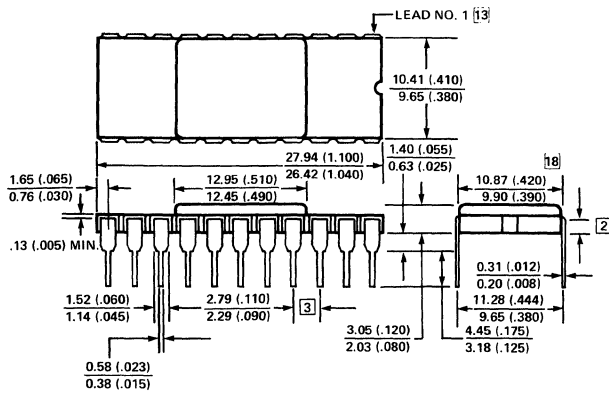
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IKA/IKB Package



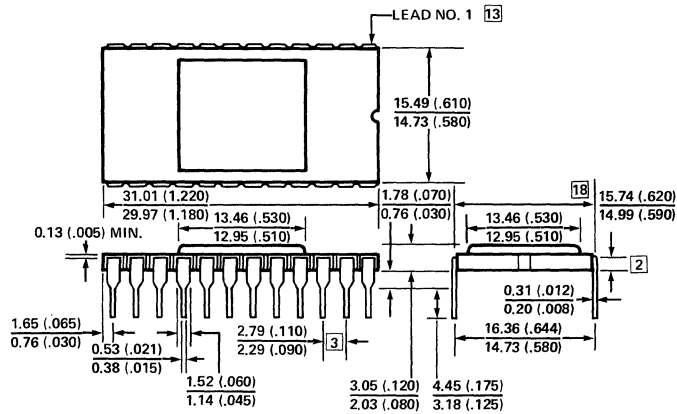
CONSTRUCTION NOTES: 10b, 11d, 12b OR 12c

IMA Package



CONSTRUCTION NOTES: 10b, 11d, 12b

INC/INH Package

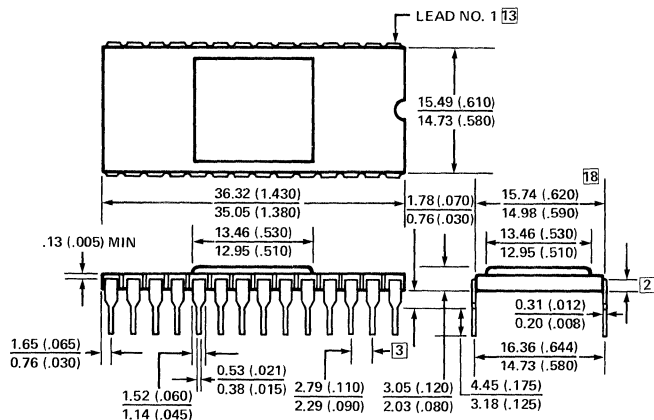


CONSTRUCTION NOTES: 10b, 11b, 12b

PACKAGES

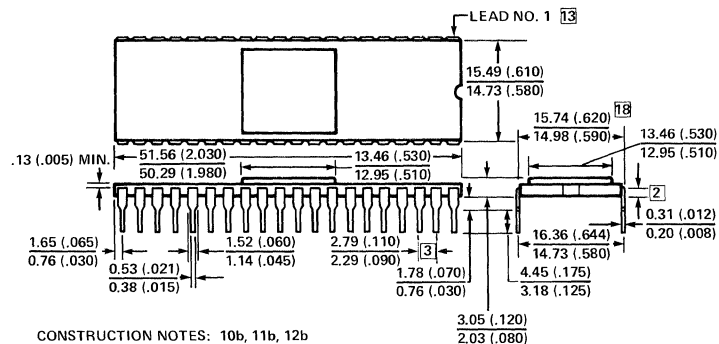
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



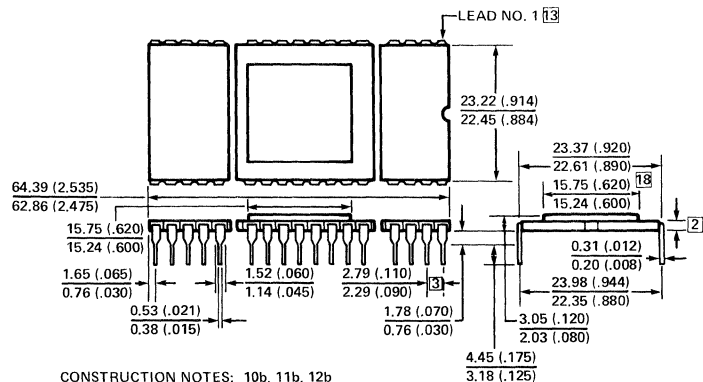
CONSTRUCTION NOTES: 10b, 11b, 12b

IWA Package



CONSTRUCTION NOTES: 10b, 11b, 12b

IZA Package



CONSTRUCTION NOTES: 10b, 11b, 12b

WHAT IS A MINIATURE IC PACKAGE?

In order to overcome the physical size constraint sometimes encountered with standard plastic dual-in-line packages, N.V. Philips of Eindhoven, the Netherlands, with which Signetics is affiliated, developed the SO package (SO = small outline). The true advantage of this miniature package is that it is possible to seal standard integrated circuit die inside of a dual-in-line package with significantly reduced outside dimensions.

This has advantages not only in the assembly of PC boards, but it also allows hybrid manufacturers to purchase fully DC- and AC-tested circuits for assembly onto substrates. Presently, with chip and wire assembly techniques, it is only possible to purchase DC-tested, unpackaged integrated circuits.

A BRIEF HISTORY

Early in the 1960's, hybrid circuit manufacturers began using unpackaged chips. Problems swiftly arose. Handling was difficult, mounting was messy, bonding was a hand operation, and AC- and DC-testing was almost impossible until the circuit was completed.

In 1967, Philips introduced the first miniature packages for discrete components in the form of SOT-23 devices. These brought outstanding improvements in manufacturing yields with significant cost reductions to hybrid circuits.

In 1971, Philips commenced a similar development of a miniature package for integrated circuits for use in the Swiss watch industry.

PRINCIPAL APPLICATIONS

The SO package is not only of interest for the hybrid manufacturer, but also for any equipment manufacturer when size, volume, and weight are critical. Miniaturization on a new scale now becomes possible. In many applications, the small size of the new SO packages opens up new possibilities for equipment manufacturers.

CURRENT USES OF THE NEW SO PACKAGES

- Portable communications equipment (e.g. paging equipment)
- Automobile instrumentation
- Portable instruments
- Television cameras
- Photographic cameras
- Telephone transmission equipment
- Model control

TYPES OF CIRCUITS CURRENTLY AVAILABLE

TYPE	PACKAGE	FUNCTION
LM301AD	SO-8	High performance op amp
LM311D	SO-8	Single general purpose comparator
LM319D	SO-14	Dual voltage comparator
LM324D	SO-14	Quad op amp
LM339D	SO-14	Quad voltage comparator
LM358D	SO-8	Dual op amp
LM13600D/AD	SO-8	Dual operational transconductance amplifier
MC1458D	SO-8	Dual op amp
NE532D	SO-8	Dual op amp
NE544D	SO-14	Servo amplifier
NE555D	SO-8	Timer
NE556D	SO-14	Dual timer
NE564D	SO-16	Phase locked loop
NE592D	SO-14	Video amplifier
NE5512	SO-8	Dual high performance op amp
NE5517D/AD	SO-16	Dual operational transconductance amplifier
NE5534D	SO-8	Low noise op amp
NE5539D	SO-14	Ultra high frequency op amp
NE5044D	SO-16	Seven channel R.C. encoder
NE5045D	SO-16	Seven channel R.C. decoder
μ A723CD	SO-14	Precision voltage regulator
μ A741CD	SO-8	General purpose op amp
μ A747CD	SO-14	Dual general purpose op amp
μ A748CD	SO-8	General purpose op amp

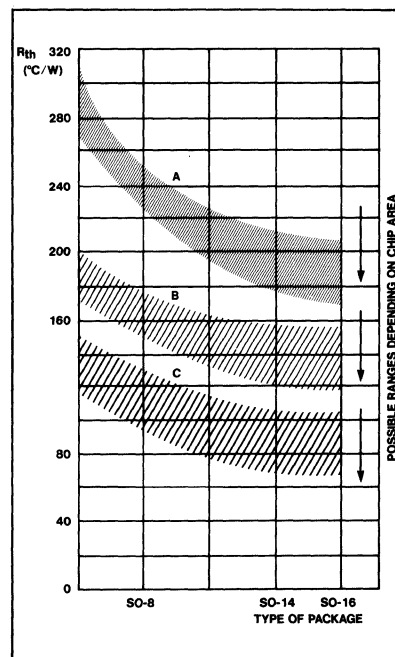
PLANS FOR NEW TYPES

Our analog product range will be extended to include devices in the new SO packaging. We are considering the full line of analog products.

POWER DISSIPATION

Considering their size, the SO packages exhibit excellent properties of power dissipation. When mounted on a ceramic substrate, the heat dissipated can be readily conducted away from the source. The thin size and short connections give a thermal resistance between junction and solder pads or heatsink about the same as for a normal DIP package mounted on a printed circuit board. The thermal resistance of the SO-8 package is about $110^{\circ}\text{C}/\text{W}$, while that of the SO-14 and SO-16 is about $100^{\circ}\text{C}/\text{W}$, or lower. Thermal resistance does, however, depend on chip size. The graph shows typical values of thermal resistance between the junction and heatsink or ambient for SO packages.

Curve A represents the thermal resistance when mounted on ceramic against a heatsink (.984 x .511 x .023 inches); curve B is when mounted on ceramic in free air; curve C is when mounted on a printed circuit board in free air.



RELIABILITY ENGINEERING QUALIFICATION REPORT ON THE "SO" PACKAGE

A Miniature Molded Epoxy Package

K. M. Self & P. J. Naumchik
Signetics Reliability Engineering

ABSTRACT

This report summarizes the Reliability Engineering activities undertaken to evaluate and qualify a miniature molded epoxy package configuration identified as the "SO." The evaluation demonstrated that the stress performance of the "SO" Package is equivalent to the larger standard molded epoxy dual-in-line package in all aspects, and mounted, the package thermal resistance characteristics are exceptional considering the reduced size and mass of the package.

BACKGROUND/ADVANTAGES

The "SO" Package was developed by N.V. Philips in 1967 for applications in hybrid structures and later for watch modules.

The reduced size of this package (refer to Figure 1) offers significant packing density improvements which up to now have been restricted to users of higher cost hermetic flat packages. For hybrid systems with limited size constraints, the "SO" offers an ease-of-use and testability advantage over conventional chip and wire hybrid approaches.

EVALUATION PROGRAM

Our evaluation/qualification program included three Analog products; LM311 voltage comparator, μ A747 dual op amp, and NE532 dual op amp.

These devices encompass three wafer fabrication processes and both 8-Pin and 14-Pin package configurations.

All products were assembled on Alloy 42 lead frames, die attached utilizing conventional gold-silicon eutectic and molded in our standard Morton 410B epoxy Novalac compound. The devices were subjected to a series of accelerated stresses and tested to conventional data sheet parameters. Variables data was taken and drift analysis was performed.

The stress conditions employed were as follows:

- High Temperature Bias Life
 $T_A = 125^\circ\text{C}$ $V_{CC} = \pm 15\text{V}$
- High Temperature Storage Life
 $T_A = 150^\circ\text{C}$
- Temperature/Humidity Bias Life
 $T_A = 85^\circ\text{C}$ RH = 85% $V_{CC} = \pm 15\text{V}$
- Temperature/Humidity/Pressure (Pressure Cooker) $T_A = 121^\circ\text{C}$
 15 PSIG 100% Sat. Steam
- Thermal Shock (Liquid to Liquid)
 -65°C to 150°C

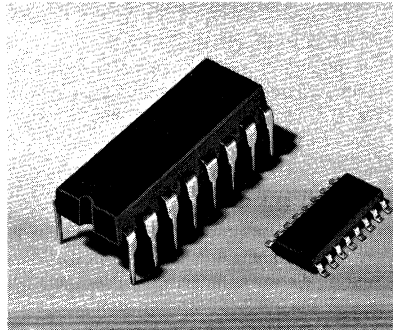


Figure 1

PROGRAM RESULTS

The details of all the stress results are included in Table I. The size of the "SO" Package tends to suggest that the structure may be less rugged than its molded dual-in-line counterpart. The test results demonstrate how misleading a factor size can be. In all stresses the "SO" devices performed as well as standard dual-in-line product. Requirements for qualification were met or exceeded on all three products evaluated.

THERMAL RESISTANCE

Thermal resistance measurements were made with devices mounted on a 2CM x 1CM (13/16" x 3/8") ceramic substrate. The results were as follows:

- 8-Pin "SO" $\theta_{JA} = 110^\circ\text{C/W}$
- 14-Pin "SO" $\theta_{JA} = 100^\circ\text{C/W}$
- 16-Pin "SO" $\theta_{JA} = 100^\circ\text{C/W}$

CONCLUSIONS

The "SO" Package constructed with Alloy-42 lead frame, Au-Si eutectic die attach, and molded in 410B epoxy Novalac provides an integrated circuit with a reliable barrier to hostile external environmental conditions and stresses. It is qualified for use with any Signetics Bipolar Analog or Bipolar Logic device which can tolerate the physical limitations of die attach pad size and can operate reliably within the thermal resistance limitations of the package.

RELIABILITY EVALUATION RESULTS

RELIABILITY ENGINEERING PROJECT ID	SIGNETICS PRODUCT TYPE	STRESS	STRESS CONDITIONS	STRESS DURATION	CUMULATIVE RESULT	ANALYSIS
790707	LM311 (14 Lead "SO")	HTOL	125°C	2,000 Hours	1/49	1 @ 168 Hours: Ball bond to trace short.
		HTSL	150°C	2,000 Hours	0/50	
		Bias/Temperature/Humidity	85°C @ 85% RH V _{CC} = 5.5V	2,000 Hours	2/50	2 @ 2000 Hours: Internal metal corrosion.
		Pressure Pot	121°C 15PSIG	432 Hours	2/51	1 @ 192 Hours: Output leakage = 68nA 1 @ 432 Hours: Output Leakage = 100nA Both internal metal corrosion.
		Thermal Shock	-65°C TO +150°C	1,000 ~	0/45	
790708	μA747 (14 Lead "SO")	HTOL	125°C ± 15V	2,000 Hours	2/50	1 @ 168 Hours: V _{OS} = 10mV. V _{OS} = 7.4mV @ 2K Hours 1 @ 1500 Hours V _{OS} = -80mV, I _B = 8μA Suspect static damage.
		HTSL	150°C	2,000 Hours	0/50	
		Bias/Temperature/Humidity	85°C @ 85% RH V _{CC} = 5.5V	2,000 Hours	1/50	V _{OS} reject @ 500 Hours (-80mV) suspect static damage
		Pressure Pot	121°C 15PSIG	312 Hours	3/50	Three V _{OS} rejects @ 312 Hours (~ 8mV)
		Thermal Shock	-65°C TO +150°C	1,000 ~	1/48	V _{OS} reject @ 700 ~ (-170 mV, I _{B-} = 14μA) Suspect static damage
795003	NE532 (8 Lead "SO")	HTOL	150°C	2,000 Hours	0/45	To 500 Hours, 0/18 from 500 to 2000 Hours (due to capacity limitations).
		HTSL	150°C	2,000 Hours	0/46	
		Bias/Temperature/Humidity	85°C @ 85% RH	2,000 Hours	2/49	1 @ 1500, 1 @ 2000—Both output sink current failures due to corrosion.
		Pressure Pot	121°C 15PSIG	456 Hours	1/43	Output sink current @ 288 hours.
		Thermal Shock	-65°C TO +150°C	1,000 ~	1/45	V _{OS} reject @ 200 ~ (15mV)

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Note

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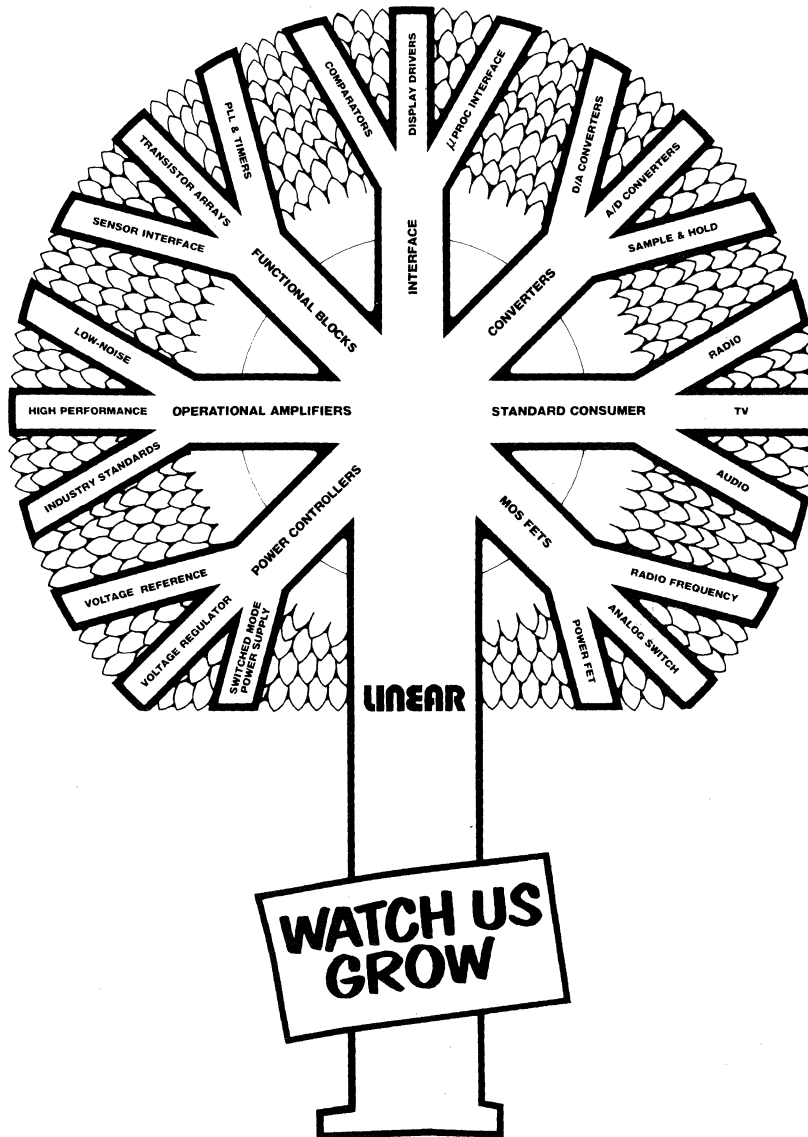
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