SiS 85C460 (ISA 386/486 Single Chip)

FEATURES

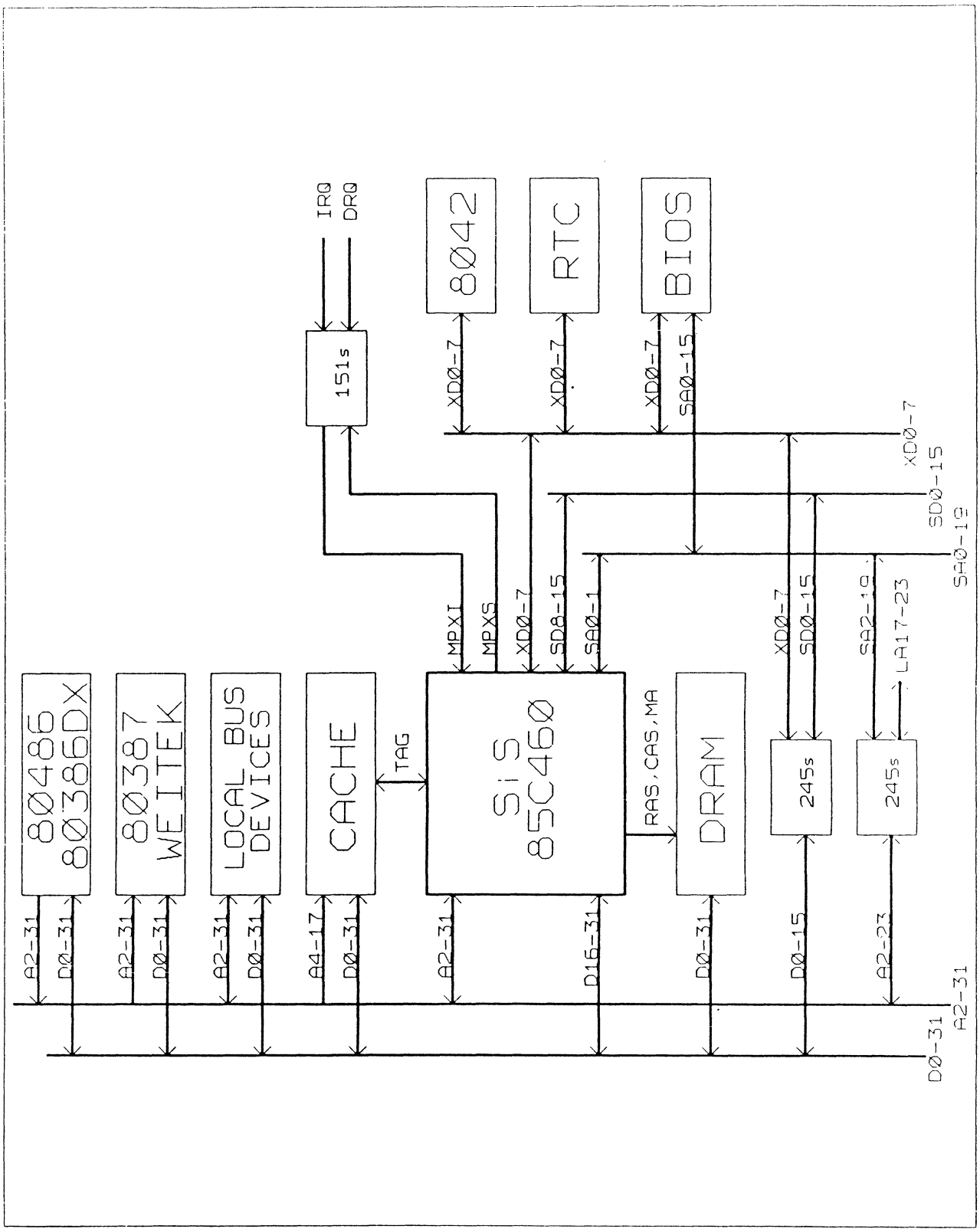
- **Fully IBM PC/AT Compatible 80386DX and 80486DX2/DX/SX Single Chip Controller**
- **Direct Mapped Cache Controller**
  - Write-Back or Write-Through Schemes
  - Bank Interleave/Non-Interleave Cache Access
  - 0/1 Wait State Cache Write Hit
  - Flexible Cache Size: 32/64/128/ 256KB and above
  - Flexible Burst Read Timing Option for 80486 DX/SX Operation: 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2
- **Fast Page Burst Mode DRAM Controller**
  - 4 Banks up to 64MB of DRAM
  - 256K/512K/1M/2M/4MxN DRAM Support
  - Programmable DRAM Speed
- **Two Programmable Non-Cacheable Regions (64KB~4MB)**
- **CAS-before-RAS Transparent DRAM Refresh**
- **BIOS/Video ROM Cacheable**
- **Shadow RAM in Increments of 32KB**
  - Option to Disable Cache in Shadow RAM Area
- **256K Memory Relocation**
- **8042 Emulation of Fast A20GATE and CPU Reset**
- **Hardware/Software De-Turbo Switch**
- **Support 16~40MHz 386DX CPU and 16~50MHz 486 CPU Operation**
- **AT Bus State Machine and AT Bus Controller**
- **Synchronous/Asynchronous AT Bus Clock**
- **Programmable AT Bus Speed**
  - 1/2, 1/3 , 1/4 , 1/5 , 1/6, 1/8, 1/10 of Input Clock or 7.159MHz
- **Programmable Wait State Generation**
  - 1 or 2 Wait States for 16-Bit Transfer
  - 4 or 5 Wait States for 8-Bit Transfer
- **Programmable I/O Recovery Time**
- **32-Bit Data Buffer Between CPU and AT System**
- **Data Conversion and Swapping Logic for 32-/16-/8-Bit Transfer During CPU and DMA Cycles**
- **Data Latch for AT Read Cycle**
- **Parity Generation and Detection Logic**
- **Port B Register and NMI Logic**
- **Integrated Peripheral Controllers**
  - Two 8259A Interrupt Controllers
  - Two 8237 DMA Controllers
  - An 8254 Counter/Timer
  - A 74LS612 Mapper
- **387/487SX and Weitek 3167/4167 Coprocessors Interface**
- **208-Pin PQFP**
- **0.8um Low Power CMOS Technology**

The SiS85C460 is a high performance, 100% PC/AT compatible single chip controller, designed for cache/non-cache 386DX or 486 PC systems running up to 40MHz or 50MHz respectively. The high integration of powerful cache controller, DRAM controller, CPU interface, bus controller, data buffers and peripheral controllers provide an easy and very economical solution for compact board manufacturing.

The SiS85C460 contains a built-in cache controller which provides direct mapped write-through/ write-back schemes. The programmable AT-bus clock supports compatible AT-bus timing for different PC system. Besides, the local bus interface and the integration of DMA Controller, Interrupt Controller and Timer/Counter are designed to give a high performance, compact, and cost-effective product for a 386DX or 486DX/SX PC/AT system.

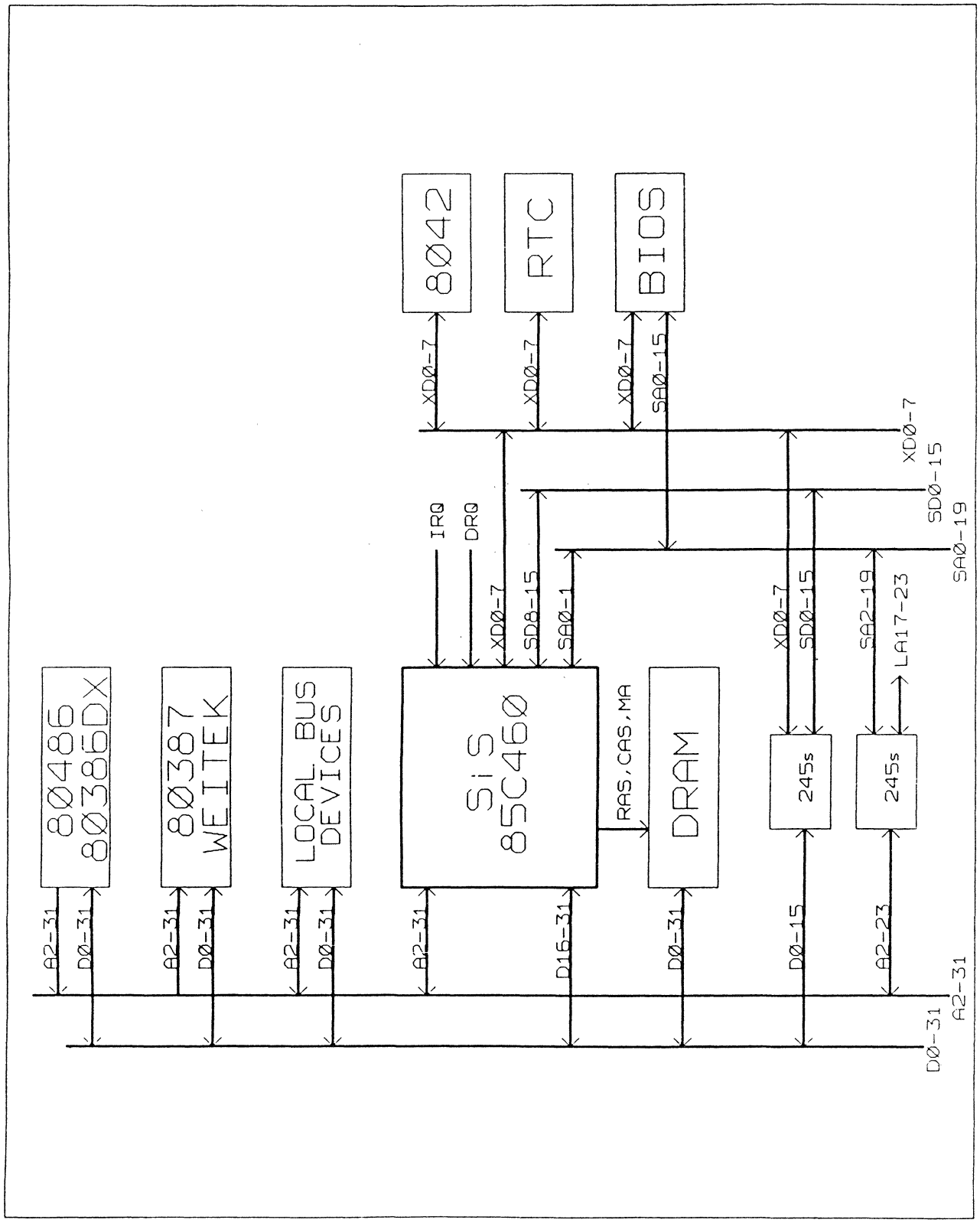
FUNCTIONAL BLOCK DIAGRAM

With CACHE application



FUNCTIONAL BLOCK DIAGRAM (continued)

Without CACHE application



FUNCTIONAL DESCRIPTION

Cache Controller

Direct Mapped Cache

Cache is a good means to de-couple fast processor from slow main memory and get the best performance of the processor. Direct mapped cache is the most straightforward, flexible, easy-to-implement, and cost-effective cache structure. A 2/4-way set associative cache has better performance than the direct mapped cache, but the delta is negligible when the cache size is large enough (e.g. 64KB). The SiS85C460 provides a fast 8-bit tag comparator and all the control logic for a cache of the 80486 processor. To implement a cache, user just needs to add SRAMs for the tag and data memories. The maximum cache size in the configuration register is 256KB but larger (512KB, 1MB, etc.) size is still applicable.

Write-Back vs. Write-Through

When the contents of the cache data are modified (i.e. written) by the processor, the same changes should be made in the main memory as well. Failing to do so will raise an inconsistency problem when the stale data in the main memory are accessed. There are two general approaches to update the main memory. The first is the write-through method and the second is the write-back (also called "copy-back") method.

In a write-through cache system, data are written to the main memory immediately while or after they are written into the cache. So the main memory always contains valid data. All the memory writes will only be as fast as the DRAM write and do not take the speed advantage of the cache.

In a write-back cache system, there is an "alter" bit per data LINE (data line means the data block referenced to a specific tag). When a write hit happens on the cache, the corresponding alter bit will be set. The written data are transferred to the main memory when they are to be over-written by a cache line fill. In this case, the cache controller checks the corresponding alter bit. If the alter bit is set, the cache data will then be written to the main memory before the cache line fill starts.

A write-back cache can offer higher performance than a write-through cache if writes to the main memory are much slower than writes to the cache. The write-back cache is also favored when a memory location is written several times in the cache before written into the main memory. The performance advantage of the write-back cache over write-through cache is software dependent.

The SiS85C460 can be configured to provide a write-back or write-through cache scheme. Besides tag and data RAM, a write-back cache needs an SRAM for the alter bits. So a write-back cache may have better performance, but costs more, than a write-through cache does. It is up to the indivisual user to judge if the extra cost of the write-back cache is justified.

80486 Burst Cache Line Fill

The internal cache of the 80486 has a 16-byte line size. When a read miss happens in the internal cache, the 80486 initiates off-chip memory read cycles to update current cache line. The 80486 will read 16 continuous bytes (4 doublewords). To increase the bus throughput, the 80486 provides a burst mode transfer, four doublewords can be read sequentially in 5 processor clocks (2-1-1-1) at the fastest.

The external cache provided by the SiS85C460 also has a 16-byte line size. It supports the 80486 burst read cycles to get the fastest cache line fill. When both the 80486 internal and external caches encounter a read miss, they are updated with the data read from DRAM simultaneously.

Cache Update Policy

For CPU cycles, the content of the cache memory is renewed when either the cache read miss or write hit occurs. Tag and data RAMs are both updated in the cache read miss cycles. In the cache write hit cycles, the SiS85C460 updates only the data RAM. In the cache write miss cycles, the CPU writes data into the main memory (DRAM), while the cache memory remains unchanged. The alter bits in the write-back cache are reset in the cache update (read miss) cycles and set in the write hit cycles.

When the cache is disabled, all the CPU reads to the cacheable memory are treated as cache read miss, so both tag and data RAMs are updated. This feature is used to initialize the cache memory before enabling it.

In DMA/master cycles, the cache data RAM is written when a write hit occurs, to assure the cache coherency. Cache memory is not accessed in DMA/master write miss or read cycles for the write-through cache. For the write-back cache, DMA/master read hit cycles are conducted to the cache, not to the DRAM.

Cache Size Options

Cache Size	Tag RAM	Data RAM	Alter RAM	Cacheable Size
32KB	2Kx8	8Kx8 x4	2Kx1	8MB
64KB	4Kx8	8Kx8 x8	4Kx1	16MB
128KB	8Kx8	32Kx8 x4	8Kx1	32MB
256KB	16Kx8	32Kx8 x8	16Kx1	64MB
512KB	32Kx8	128Kx8 x4	32Kx1	64MB

The cacheable DRAM size is determined by the cache size because the tag address field is always 8-bit wide. The on-board DRAM beyond the cacheable size is not cacheable. It is still cacheable for the 80486 internal cache, however.

Cache Speed Options for 386 Mode

The SiS85C360 provides two cache read speed options : 2T or 3T, and two options of cache write cycle : 2T or 3T. The 2T cache write is applicable only when the cache read is also set to 2T.

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache data RAM for various speeds of the 80386 CPU.

Read Cycle-Write Cycle	25MHz CPU	33MHz CPU	40MHz CPU
2T-2T	-35	-20	-12
2T-3T	-40	-25	-20
3T-3T	-65	-45	-35

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache tag and alter RAM for various speeds of the 80386 CPU.

Read Cycle-Write Cycle	25MHz CPU	33MHz CPU	40MHz CPU
2T-2T	-25	-20	-12
2T-3T	-35	-25	-15
3T-3T	-45	-35	-25

Cache Speed Options for 486 Mode

The external cache can be configurated to non-interleave or two-bank interleave. Two-bank interleaved cache can use slower cache data RAM but needs more data RAM chips.

The SiS85C460 provides four cache read speed options : 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2, and two options of cache write cycle : 2T or 3T. The cache read speed x-y-y-y is selected via the bit 7 of configuration register 50 (x) and the bit 0 of configuration register 51 (y). The 2T cache write is applicable only when the first cache read of a burst is also set to 2T (2-1-1-1 or 2-2-2-2).

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache data RAM for various speeds of the 80486 CPU.

Cache Configuration	25MHz CPU	33MHz CPU	40MHz CPU	50MHz CPU
2-1-2 Interleave (*1)	-35 (*2)	-20	-12	----
2-1-2 Non-interleave	-25	-15	----	----
2-1-3 Interleave	-40	-25	-20	----
2-1-3 Non-interleave	-25	-15	----	----
3-1-3 Interleave	-45	-25	-20	-12
3-1-3 Non-interleave	-25	-15	----	----
2-2-2 Non-interleave	-35	-20	-12	----
2-2-3 Non-interleave	-40	-25	-20	----
3-2-3 Non-interleave	-65	-45	-35	-25
3-2-3 Interleave	-80	-55	-45	-30

Note: *1. x-y-z means x-y-y-y burst read and zT write cycle.
***2. -m means the access speed of SRAM in ns.**

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache tag and alter RAM for various speeds of the 80486 CPU.

Cache Configuration	25MHz CPU	33MHz CPU	40MHz CPU	50MHz CPU
2-X-2	-25	-20	-12	----
2-X-3	-35	-25	-15	----
3-X-3	-45	-35	-25	-20

Note: X presents either 1T or 2T cycles.

Non-Cacheable Regions

In some applications, users desire a block of memory not to be cached. The SiS85C460 provides two programmable non-cacheable regions to serve this function.

Only the on-board DRAM directly controlled by the SiS85C460 is cacheable. The memory residing on the AT add-ons is non-cacheable. When a memory space is mapped by both the on-board DRAM and AT add-on memory, CPU access will be conducted to the on-board DRAM. If users desire the AT add-on memory to be accessed instead of the on-board DRAM at the overlapped memory space, the two non-cacheable regions can be used to disable the on-board DRAM in the programmed space.

The size and starting address of two non-cacheable regions are programmable in configuration register 54, 55, 56 and 57. The validity of the starting address bits depends on the size of related non-cacheable region.

Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
1M	V	V	V	V	X	X	X	X
2M	V	V	V	X	X	X	X	X
4M	V	V	X	X	X	X	X	X

V = Valid
X = Don't Care

Cache Initialization

The external cache supported by the SiS85C460 does NOT provide the validation flag (bit) for the data lines. All the cache data are assumed valid once the cache is enabled. So the whole cache must be filled by valid data before the cache enable bit is turned on. The cache initialization can be done via sequential reads to a block of on-board DRAM which is equal to or larger than the cache in size.

DRAM Controller

DRAM Speed Options

The SiS85C460 provides 4 read and 2 write speed options in the configuration register. A table of page hit cycle time of all the possible speed configurations is listed as follows:

	Read	486 Burst Read	Write
Fastest	3	3-2-2-2	2
Faster	4	4-3-3-3	2/3
Slower	5	5-4-4-4	2/3
Slowest	6	6-5-5-5	4

Note: The unit of the above table is in T cycles.

There will be plenty of timing margin if the user adopt, Fastest for 25MHz 80386/80486, Faster for 33MHz, Slower for 40MHz, and Slowest only for 50MHz 80486.

DRAM Access Timing

	Fastest	Faster	Slower	Slowest	
Trcd	1.5T	2T	2T	3T	RAS-to-CAS delay
Tcas	1.5T	2T	3T	3T	Read CAS pulse width
Trp	3T	3T	4T	4T	RAS precharge
Tcp	0.5T	1T	1T	2T	CAS precharge

DRAM Size Configuration

The SiS85C460 supports 32 different DRAM configurations in 4 banks. Besides the traditional 256K/1M/4M xN DRAMs, the new 512K xN and future 2M xN DRAMs are also supported.

Refresh

In the original PC/AT design, the CPU is held off (i.e. can not do anything) during the DRAM refresh cycles. It happens once per 15us and takes at least 0.5us each time. In SiS85C460, refresh can be selected to hold CPU or not by setting the bit 5 of the configuration register 58.

Recently the speed of DRAM is becoming faster so the time needed per refresh cycle is getting shorter. The refresh cycle time for the 100ns DRAM is 200ns minimum, for example. In a system with cache, most of the CPU accesses are referred to the cache so that the DRAM usage (percent of time the DRAM is accessed by the CPU) is significantly reduced.

In the SiS85C460, the main memory refresh is independent to the AT-bus refresh so the cycle time is shorter (need not follow the standard AT-bus timing). When the main memory is refreshed, the CPU is NOT held off so it may execute the program stored in the cache at the same time. If the CPU accesses the main memory while it is being refreshed, this access will be pending (i.e. the CPU must wait) until the refresh is finished.

The following table lists the refresh-related RAS timings of the on-board DRAM:

	Fastest	Faster	Slower	Slowest
RAS pre-charge	3T	3T	4T	5T
RAS active	3T	4T	4T	5T

If hidden refresh is selected on AT bus, the AT bus refresh cycles are issued once per 15us when there is no access from the CPU, the DMA controller, or the bus master on the AT bus. The CPU will not feel the existing of the AT bus refresh unless it issues an AT cycle or cache miss cycle coincidentaly. The controller arbitrates among the CPU AT cycle, DMA/master request, and bus refresh so that they can be executed one after another when more than one of them intend to use the AT bus at the same time.

The SiS85C460 has a slow refresh feature to cut the refresh frequency down to 1/4. It should be selected only when the system is equipped with slow-refresh DRAM.

The refresh scheme of local DRAM is the CAS-before-RAS refresh. The CASs go active at least one T before RASs in local refresh. To reduce the power noise caused by refresh, the RASs of odd banks go active one T after that of even banks. It is called "staggered refresh".

Shadow RAM

Memory space 0A0000-0FFFFFh is reserved for the video RAM, I/O and system BIOS ROM. Access to this area should not be conducted to the main memory in standard PC/AT. Since the speed of the DRAM is significantly faster than that of the ROM, if contents of the BIOS ROM are copied to the unused DRAM (0A0000- 0FFFFFh), the DRAM can work as fast BIOS ROM and raise the overall system performance. This is called the "Shadow RAM".

The SiS85C460 provides shadow to 0C0000-0EFFFFh in 32KB granularity and shadow to 0F0000-0FFFFFh. The shadow RAM is default non-cacheable. The shadow RAM in C0000-C7FFFh, and F0000-FFFFFh can be programmed to be cacheable.

256KB Relocation

The SiS85C460 provides the 256KB DRAM relocation from 0A0000-0BFFFFh and 0D0000-0EFFFFh to the top of configurated DRAM size.

This function works for the DRAM sizes of 1MB, 2MB, 4MB, 6MB and 8MB when the shadowing of segments D and E is disabled.

ROM Support

The SiS85C460 provides a chip select signal for the system BIOS ROM. The memory space assigned to the ROM is the highest 64/128KB of the real (1MB) and the protected (4GB) address modes of the 80486/80386DX CPUs.

The system BIOS ROM can be shadowed by the DRAM to improve performance. When the shadow RAM is turned on, the access to system BIOS with address below 100000h will be channeled to the DRAM.

Fast A20GATE And CPU Reset

In the original PC/AT design, the A20GATE and CPU Reset (RC) are controlled by the 8042 keyboard controller to switch the CPU between the real and protected address modes. The operation of 8042 is quite slow so if the address mode switching happens frequently, the program execution speed will be affected.

The SiS85C460 provides a 8042 emulation to generate the A20GATE and CPU reset in hardware. This feature is software transparent.

Local Bus Support

The SiS85C460 uses LBD* (stands for Local Bus Device) and LRDY* (stands for Local Bus Device Ready) pins to implement "Local Bus Device Architecture" such as Weitek 3167/4167. The interface protocol is very straightforward.

When a local bus device decodes the bus definition/address from CPU and finds the cycle belonging to it at the start of a CPU bus cycle, it should assert LBD* to inform the SiS85C460 that it's a local bus device cycle. The SiS85C460 will operate a local bus cycle, until either LRDY* is asserted from the local bus device to SiS85C460 to generate CPURDY*, or the local bus device asserts CPURDY* (wire-OR with the CPURDY* of SiS85C460) itself to terminate current cycle. In the former case, the SiS85C460 will synchronize LRDY* with CCLKIN then asserts CPURDY*. In the later case, the SiS85C460 detects the asserted CPURDY* to finish the current cycle.

When there is more than one local bus devices, their LBD* and LRDY* signals should be ANDed together before connecting to the SiS85C460.

The SiS85C460 samples the LBD* input at the end of T2 when DRAM speed is set to "FASTEST" or "FASTER", and at the end of T3 when DRAM speed is "SLOWER" or "SLOWEST". The LBD* pin should be asserted before the sampling point, when the current cycle is a local bus cycle.

The implementation to support full VESA VL-Bus specification will be provided in the future version of silicon.

Turbo Switch

Some old applications may get into trouble if the system speed is too fast. The SiS85C460 offer a de-turbo function that can be controlled through a hardware switch or software programming. When the de-turbo function is turned on, system performs 1/3 or 2/3 speed selected by the bit 4 of configuration register 58.

Clock Generation

The SiS85C460 provides a flexible software controlled selection of the clock used for the AT bus state machine. Bus clock is determined by the configuration register and can be selected as 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/10 of the input clock or 7.159 MHz.

The clock switches speed automatically, with clean transition, whenever the configuration is changed.

AT Bus State Machine

In order to obtain the maximum performance of the system board, it is desired to run the system board at the maximum CPU frequency. This frequency may be too fast for the slow AT bus. In order to overcome this problem, the SiS85C460 operates the state machine at a slower frequency than the CPU frequency.

The SiS85C460 starts a bus cycle when an BS16* is active and an BALE signal has been inserted in the AT-TS state. It then enters the command cycle AT-TC and provides the timing signals for AT bus cycle and terminates by asserting READY* signal. To determine the bus size, MEMCS16* signal is sampled at the falling edge of BALE during memory cycle. IOCS16* is sampled at every rising edge of SYSCLK after the command is active in an I/O cycle.

The command cycle is terminated only when IORDY* is active and all programmed wait states have been executed. The period of command cycle is selected by the configuration register. For 16-bit transfer, the default is 1 wait state, but can be selected as 2 wait states. For 8-bit transfer, the default is 5 wait states, but can be selected as 4 wait states. No command delay is inserted for 16-bit memory cycle, otherwise 1/2 SYSCLK command delay is always inserted.

IORDY* is sampled at the start of every AT-TC state. The command cycle will not be terminated until IORDY* is sampled HIGH and all programmed wait states have been executed. If ZWS* is detected LOW at the middle of the AT-TC state, the current AT cycle will be terminated immediately.

During read cycle, the data read from device may be lost after the command is finished. The SiS85C460 will latch the data immediately after the read command is inactive and will hold the data until the AT cycle is ended. The "Read Latch" function is active for all AT bus read cycle, except during DMA, Master, or local RAM read cycle.

The shortest command recovery time is two SYSCLK in this chip, this could be too short for some I/O devices. In this case, a configuration register option is provided. If selected, the I/O command recovery time will be at least 2 SYSCLK for 16-bit transfer and 4 SYSCLK for 8-bit transfer.

Data Conversion Logic

If MEMCS16* and IOCS16* signals are sampled HIGH, the current cycle will be an 8-bit transfer cycle. The AT state machine performs data conversion if the CPU executes a 16-bit read or write during an 8-bit transfer. The SiS85C460 separates a 16-bit read or write operation into two 8-bit transfers and activates SA0 signal in the second cycle. Meanwhile, the SiS85C460 will execute all the data swapping process between the 32-bit, 16-bit and 8-bit data bus.

Besides data conversion cycle, the data will also be swapped if it is necessary during AT cycle. In DMA and Master cycles, the data swapping is also needed. The system checks the command, address, and related control signals and then arranges required swapping.

Since the BE0*-BE3* can not be used to select the devices on AT bus directly, BE0*-BE3* will be inputed in AT cycle to generate the SA1, SA0, and BHE* signals needed. In DMA cycle, BE0*-BE3* is generated from the SA1 and SA0 to access the local memory. The SiS85C460 checks these four byte enable signals in AT cycle and determines whether it is a 16-bit read or write and whether data conversion cycle should be performed.

Port B Register and NMI Logic

The SiS85C460 provides access to Port B as defined for IBM PC/AT, as shown below:

Bit	Contents
0	GATE2 - Timer 2 Gate
1	SPKEN - Speaker Data
2	PCKEN - Parity Check Enable
3	IOCHCKEN - I/O Channel Check Enable
4	REFRESH - Refresh Detect
5	OUT2 - Timer 2 Out
6	IOCHCK - I/O Channel Check
7	PCK - Parity Check

The NMI logic in the SiS85C460 will enable and latch the I/O and parity errors to generate a non-maskable interrupt to the CPU, if NMI has been enabled. NMI is enabled when data bit 7 of port 70h is set to 0, and NMI is disabled if it is equal to 1.

Bus Buffer Control Logic

During AT-bus read cycle, the data from device will be latched immediately after the read command is inactive and will be hold till the end of AT cycle.

The SiS85C460 provides 16-bit to 8-bit or 8-bit to 16-bit data bus conversion in AT cycle, and 32-, 16- and 8-bit data bus conversion in DMA cycle.

Parity Generation and Detection

During DRAM write cycles, the SiS85C460 generates even parity for each of the four bytes. The parity bits PD0-PD3 are written to the parity memory in the system DRAM. During the system DRAM read cycles, the SiS85C460 checks for even parity for each byte read. If odd parity is detected, the SiS85C460 flags a parity error. The SiS85C460 detects the error and generates the NMI when enabled. The parity error can be cleared by programming parity check disable, which is defined by bit-2 of the port B register.

Peripheral Controllers

The SiS85C460 contains Peripheral Controllers which include two 8237 DMA Controllers, a 74LS612 Mapper, two 8259 Interrupt Controllers, and an 8254 Counter/Timer.

DMA Controllers

Two DMA controllers are connected in such a way as to provide the user with four DMA channels (DMA1) for 8-bit transfers and three DMA channels (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMA PAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Interrupt Controllers

Sixteen interrupt channels are provided in the SiS85C460. These channels are allocated to two cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, two are connected internally to various devices, allowing 14 user definable interrupt channels. The two internally connected channels are as follows:
Channel 0 - Counter/Timer Counter 0 Interrupt
Channel 2 - Cascade to Slave Interrupt Controller (INTC2)

Counter/Timer

A Counter/Timer (CTC) subsystem contains three independent counters. The clock input for each counter is connected to a clock of 1.19MHz, which is derived by dividing the 14.318MHz crystal input by 12. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task-switching. Counter 1 may be programmed to generate pulses or square waves for used by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

Clock and Wait State Control

The Clock and Wait State Control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023h.

Writing and reading this register is accomplished by first writing a 01h to locaton 022h to select the Configuration Register, and then performing either a read or write to location 023h.

Peripheral Controllers Address Map

DMA Controller Address Map

DMA1	DMA2	XIOR#	XIOW#	FliP Flop	Register Function
000h	0C0h	0	1	0	Read channel 0 current address low byte
		0	1	1	Read channel 0 current address high byte
		1	0	0	Write channel 0 base and current address low byte
		1	0	1	Write channel 0 base and current address high byte
001h	0C2h	0	1	0	Read channel 0 current word count low byte
		0	1	1	Read channel 0 current word count high byte
		1	0	0	Write channel 0 base and current word count low byte
		1	0	1	Write channel 0 base and current word count high byte
002h	0C4h	0	1	0	Read channel 1 current address low byte
		0	1	1	Read channel 1 current address high byte
		1	0	0	Write channel 1 base and current address low byte
		1	0	1	Write channel 1 base and current address high byte
003h	0C6h	0	1	0	Read channel 1 current word count low byte
		0	1	1	Read channel 1 current word count high byte
		1	0	0	Write channel 1 base and current word count low byte
		1	0	1	Write channel 1 base and current word count high byte
004h	0C8h	0	1	0	Read channel 2 current address low byte
		0	1	1	Read channel 2 current address high byte
		1	0	0	Write channel 2 base and current address low byte
		1	0	1	Write channel 2 base and current address high byte
005h	0CAh	0	1	0	Read channel 2 current word count low byte
		0	1	1	Read channel 2 current word count high byte
		1	0	0	Write channel 2 base and current word count low byte
		1	0	1	Write channel 2 base and current word count high byte
006h	0CCh	0	1	0	Read channel 3 current address low byte
		0	1	1	Read channel 3 current address high byte
		1	0	0	Write channel 3 base and current address low byte
		1	0	1	Write channel 3 base and current address high byte
007h	0CEh	0	1	0	Read channel 3 current word count low byte
		0	1	1	Read channel 3 current word count high byte
		1	0	0	Write channel 3 base and current word count low byte
		1	0	1	Write channel 3 base and current word count high byte

An internal flip-flop is used to supplement the addressing of the Count and Address registers. This bit selects between high and low bytes of these registers and toggles each time a read or write occurs to any of these registers.

DMA Controller Address Map (continued)

DMA1	DMA2	XIOR#	XIOW#	Flip Flop	Register Function
008h	0D0h	0	1	X	Read status register
		1	0	X	Write command register
009h	0D2h	0	1	X	Read DMA request register
		1	0	X	Write DMA request register
00Ah	0D4h	0	1	X	Read mode register
		1	0	Z	Write single bit DMA request mask register
00Bh	0D6h	0	1	X	Read mode register
		1	0	X	Write mode register
00Ch	0D8h	0	1	X	Set byte pointer flip-flop
		1	0	X	Clear byte pointer flip-flop
00Dh	0DAh	0	1	X	Read temporary register Master clear
00Eh	0DCh	0	1	X	Clear mode register counter
		1	0	X	Clear all DMA request mask register bits
00Fh	0DEh	0	1	X	Read all DMA request mask register bits
		1	0	X	Write all DMA request mask register bits

DMA Address Extension Register Map

Address	Register Function
080h	Unused
081h	8-bit DMA Channel 2 (DACK2)
082h	8-bit DMA Channel 3 (DACK3)
083h	8-bit DMA Channel 1 (DACK1)
084h	Unused
085h	Unused
086h	Unused
087h	8-bit DMA Channel 0 (DACK0)
088h	Unused
089h	16-bit DMA Channel 2 (DACK6)
08Ah	16-bit DMA Channel 3 (DACK7)
08Bh	16-bit DMA Channel 1 (DACK5)
08Ch	Unused
08Dh	Unused
08Eh	Unused
08Fh	Refresh cycle

Interrupt Controller Address Map

Register	Type	I/O Port	b7	b6	b5	b4	b3	b2	b1	b0
ICW1	WRO	20h (A0h)	X	X	X	SI	LTM	X	SM	X
ICW2	WRO	21h (A1h)	V7	V6	V5	V4	V3	X	X	X
ICW3	WRO	21h	S7	S6	S5	S4	S3	S2	S1	S0
ICW3	WRO	A1h	0	0	0	0	0	ID2	ID1	ID0
ICW4	WRO	21h (A1h)	X	X	X	EMI	X	X	AEOI	X
OCW1	RD/WR	21h (A1h)	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	WRO	20h (A0h)	R	SL	EOI	SI	2/3	L2	L1	L0
OCW3	WRO	20h (A0h)	0	ESSM	SMM	SI	2/3	PM	RR	RIS
IR	RDO	20h (A0h)	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IS	RDO	20h (A0h)	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0

Note:

WRO = Write only register
RDO = Read only register
RD/WR = Read/Write register
X = Don't care

Counter/Timer Address Map

Address	Function
040h	Counter 0 read/write
041h	Coutner 1 read/write
042h	Counter 2 read/write
043h	Control register write only

Configuration Registers

There are eleven configuration registers inside the SiS85C460. An indexing scheme is used to access all the registers. Port 22h is the index register and port 23h is the data register. The configuration registers are accessed by first writing the index to port 22h and immediately followed by a read or a write to port 23h. The index is reset after data access. Every data access to port 23h must be preceded by an index write to port 22h, even if the same register is being accessed. All the reserved bits should be set to zero for future compatibility purpose. The contents of the registers are listed as follows.

Configuration Registers

Register 50 (index50) Default = 00

bit 7, 6 **DRAM Speed** (See DRAM Speed Options on page 10)
00: Slowest
01: Slower
10: Faster
11: Fastest
Bit 7 also defines the cache read cycle time: 0/1 : 3T/2T

bit 5 **DRAM Write CAS Pulse Width**
0: 2T
1: 1T

bit 4~0 **DRAM Size Configuration**

	Bank-0	Bank-1	Bank-2	Bank-3	Total
00000	1M				1MB
00001	1M	1M			2MB
00010	1M	1M	2M		4MB
00011	1M	1M	4M		6MB
00100	1M	1M	2M	4M	8MB
00101	1M	1M	4M	4M	10MB
00110	1M	1M	16M		18MB
00111	2M				2MB
01000	2M	2M			4MB
01001	2M	4M			6MB
01010	2M	2M	4M		8MB
01011	2M	2M	4M	4M	12MB
01100	2M	16M			18MB
01101	2M	2M	16M		20MB
01110	2M	2M	4M	16M	24MB
01111	2M	2M	16M	16M	36MB
10000	4M				4MB
10001	4M	4M			8MB
10010	4M	4M	4M		12MB
10011	4M	4M	4M	4M	16MB
10100	4M	16M			20MB
10101	4M	4M	16M		24MB
10110	4M	16M	16M		36MB
10111	4M	4M	16M	16M	40MB
11000	8M				8MB
11001	8M	8M			16MB
11010	8M	8M	8M		24MB
11011	8M	8M	8M	8M	32MB
11100	16M				16MB
11101	16M	16M			32MB
11110	16M	16M	16M		48MB
11111	16M	16M	16M	16M	64MB

Note: 1MB = 256K x 36bits
2MB = 512K x 36bits
4MB = 1M x 36bits
8MB = 2M x 36bits
16MB = 4M x 36bits

Register 51 (index 51) Default = 00

bit 7 **Cache Enable**
0: Disable
1: Enable

bit 6 **Write Back Enable**
0: Disable (Write Through)
1: Enable (Write Back)

bit 5, 4 **Cache Size**
00: 32KB
01: 64KB
10: 128KB
11: 256KB and above

bit 3 **Cache Interleave Enable**
0: Disable
1: Enable

bit 2 **Cache On/Off**
0: Off
1: On

bit 1 **Cache Write Cycle**
0: 3T
1: 2T

bit 0 **Cache Burst Read Cycle (486 only)**
0: 1T
1: 2T
(Reserved and should be written with 1 in the 386 system)

Register 52 (index 52) Default = 00

bit 7 **Shadow RAM Read Enable**
0: Disable
1: Enable

bit 6 **Shadow RAM Write Protection Enable**
0: Disable
1: Enable

bit 5 **E8000h - EFFFFh Shadow RAM Enable**

bit 4 **E0000h - E7FFFh Shadow RAM Enable**

bit 3 **D8000h - DFFFFh Shadow RAM Enable**

bit 2 **D0000h - D7FFFh Shadow RAM Enable**

bit 1 **C8000h - CFFFFh Shadow RAM Enable**

bit 0 **C0000h - C7FFFh Shadow RAM Enable**

Register 53 (index 53) Default = 00

bit 7 **System BIOS ROM Size**
0: 64K
1: 128K

bit 6 **Combine System BIOS with C0000h~C7FFFh region for ROM area**
0: Disable
1: Enable

bit 5 **F0000h ~ FFFFFh Shadow RAM Cacheable**
0: Non-Cacheable
1: Cacheable

bit 4 **C0000h ~ C7FFFh Shadow RAM Cacheable**
0: Non-Cacheable
1: Cacheable

bit 3, 2 **DMA Cycle Up to 64MB Program A25 and A24**
bit 3: A25
bit 2: A24

bit 1 **Data Parity Check Enable**
0: Disable
1: Enable

bit 0 **De-turbo Switch Enable**
0: De-turbo Switch Enable
1: Always turbo, ignore the Status of Turbo Switch

Register 54 (index 54) Default = 00

bit 7 **Allocation of Non-cacheable Area #1**
0: Local DRAM
1: AT Bus, local DRAM disabled

bit 6~4 **Size of Non-Cacheable Area #1 (within 16MB)**
000: 0KB (disabled)
001: 64KB
010: 128KB
011: 256KB
100: 512KB
101: 1MB
110: 2MB
111: 4MB

bit 3 **Allocation of Non-Cacheable Area #2**
0: Local DRAM
1: AT Bus, local DRAM disabled

bit 2~0 **Size of Non-Cacheable Area #2 (within 64MB)**

000: 0KB (disabled)
001: 64KB
010: 128KB
011: 256KB
100: 512KB
101: 1MB
110: 2MB
111: 4MB

Register 55 (index 55) Default = 00

bit 7~0 **A23~A16 of Non-Cacheable Area #1 (within 16MB)**

Register 56 (index 56) Default = 00

bit 7~0 **A23~A16 of Non-Cacheable Area #2 (with 64MB)**

Register 57 (index 57) Default = 00

bit 7, 6 **A25 and A24 of Non-Cacheable Area #2**

bit 5 **Gate A20 Emulation Enable**
0: Disable
1: Enable

bit 4 **Fast Reset Emulation Enable**
0: Disable
1: Enable

bit 3 **Fast Reset Latency Control**
0: 2us
1: 6us

bit 2 **Slow Refresh Enable (1:4)**
0: Normal Refresh
1: Slow Refresh

bit 1 **De-turbo ON/OFF**
0: Turbo
1: De-Turbo

bit 0 **Cache Sizing Enable**
0: Normal operation
1: Always Cache hit

Register 58 (index 58) Default = 00

bit 7 **Slow CPU (below 25MHz) Enable**
0: Disable
1: Enable

bit 6 **DRAM Write Cycle**
0: 1 wait state
1: 0 wait state

bit 5 **Resvered and should be written with 1**

bit 4 **De-turbo Hold Time**

0: Hold 4us
1: Hold 8us (Every 12us)

bit 3 **Reserved and should be written with 0**

bit 2 **Combine System BIOS with C8000h~CFFFFh region for ROM area**

0: Disable
1: Enable

bit 1, 0 **Reserved and should be written with 0**

Register 60 (index 60) Default = 00

bit 7~5 **Bus Clock Frequency Selection**

000: BUSCLK = 7.159 MHZ
001: BUSCLK = 1/10 CLKIN
010: BUSCLK = 1/8 CLKIN
011: BUSCLK = 1/6 CLKIN
100: BUSCLK = 1/5 CLKIN
101: BUSCLK = 1/4 CLKIN
110: BUSCLK = 1/3 CLKIN
111: BUSCLK = 1/2 CLKIN

bit 4~0 **Reserved and should be written with 0**

Register 61 (index 61) Default = 01

bit 7, 6 **16-Bit I/O Cycle Command Recovery Time Selection**

00: 8 BUSCLK
01: 5 BUSCLK
10: 3 BUSCLK
11: 2 BUSCLK

bit 5, 4 **8-Bit I/O Cycle Command Recovery Time Selection**

00: 16 BUSCLK
01: 11 BUSCLK
10: 7 BUSCLK
11: 4 BUSCLK

bit 3 **Reserved and should be written with 1**

bit 2 **16-bit Memory, I/O Wait State Selection**

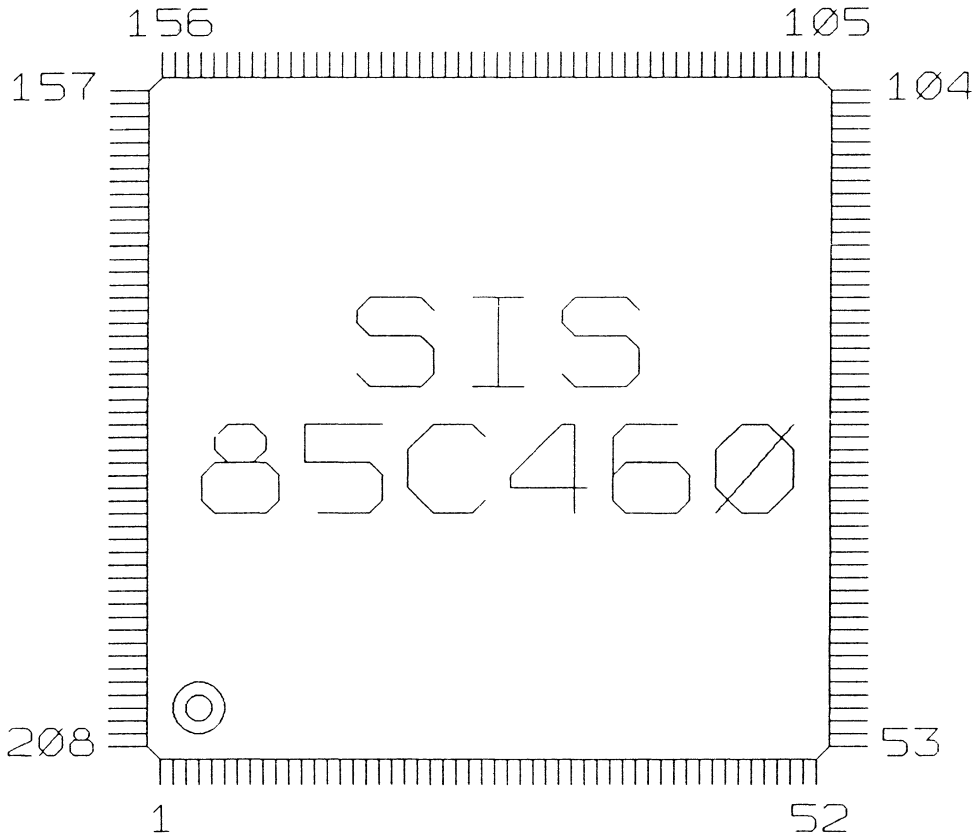
0: 2 wait states
1: 1 wait states

bit 1 **8-bit Memory, I/O Wait State Selection**

0: 5 wait states
1: 4 wait states

bit 0 **Reserved and should be written with 1**

PIN ASSIGNMENT



PIN ASSIGNMENT

1	CLKIN	53	SD11	105	IGNNE*[PREQ386]	157	CAS1*
2	14MHZ	54	GND	106	BLAST*[PREQ387]	158	CAS0*
3	IOR*	55	SD12	107	BRDY*[NC]	159	MA10
4	IOW*	56	SD13	108	BE3*	160	MA9
5	GND	57	SD14	109	BE2*	161	MA8
6	HDEN*	58	SD15	110	BE1*	162	MA7
7	LDEN*	59	GND	111	BE0*	163	MA6
8	BDIR	60	GND	112	NMI	164	GND
9	SDIR	61	VCC	113	INTR	165	VCC
10	VCC	62	PD1	114	VCC	166	MA5
11	ASRTC	63	A31	115	A20M*[CPUA20]	167	MA4
12	DSRTC*	64	A26	116	PCD[BZ387*]	168	MA3
13	DWRTC*	65	A25	117	SPK	169	MA2
14	CLKOUT	66	A24	118	PWRGD	170	MA1
15	GND	67	A23	119	GND	171	MA0
16	ZWS*	68	A22	120	LOCK*	172	BALE
17	XD0	69	A21	121	LBD*	173	AEN
18	XD1	70	A20	122	LRDY*	174	GND
19	XD2	71	A19	123	TA7/IRQ15	175	IORDY*
20	XD3	72	A18	124	TA6/IRQ14	176	EADS*[BZ386*]
21	XD4	73	A17	125	TA5/IRQ12	177	MPXS2/IRQ11
22	XD5	74	A16	126	TA4/IRQ7	178	MPXS1/IRQ10
23	XD6	75	GND	127	TA3/IRQ3	179	MPXS0/IRQ9
24	XD7	76	A15	128	TA2/DRQ7	180	MPXI2/IRQ8
25	PD0	77	A14	129	TA1/DRQ6	181	MPXI1/IRQ6
26	PD2	78	A13	130	TA0/DRQ5	182	MPXI0/IRQ5
27	D16	79	A12	131	TAWE*/WIRQ	183	MEMCS16*
28	D17	80	A11	132	ALT/DTURBO	184	IOCS16*
29	D18	81	A10	133	ALTWE*/RC*	185	MASTER*
30	D19	82	A9	134	MWE*	186	GND
31	D20	83	A8	135	GND	187	DACK7*
32	D21	84	A7	136	KWEX*	188	DACK6*
33	D22	85	A6	137	KWEY*	189	DACK5*
34	D23	86	A5	138	RAS3*	190	DACK3*
35	GND	87	A4	139	RAS2*	191	DACK2*
36	HOLD	88	KEN*[ERR386*]	140	RAS1*	192	DACK1*
37	BS16*	89	GND	141	RAS0*	193	DACK0*
38	GND	90	KBROMCS*	142	GND	194	GND
39	D24	91	A3	143	KREX*	195	TC
40	D25	92	A2	144	KREY*	196	BHE*
41	D26	93	RSTCPU	145	MRE*/IOCHK*	197	REF*
42	D27	94	CCLKIN	146	GND	198	SYSCLK
43	VCC	95	ADS*	147	VCC	199	RSTDRV
44	D28	96	GND	148	KCE3*/DRQ3	200	GND
45	D29	97	VCC	149	KCE2*/DRQ2	201	VCC
46	D30	98	CPURDY*	150	KCE1*/DRQ1	202	MEMR*
47	D31	99	GND	151	KCE0*/DRQ0	203	MEMW*
48	PD3	100	W/R*	152	KA3X/KA3/IRQ4	204	SMEMR*
49	GND	101	D/C*	153	KA3Y/KA2/IRQ1	205	SMEMW*
50	SD8	102	M/IO*	154	GND	206	GND
51	SD9	103	HLDA	155	CAS3*	207	SA1
52	SD10	104	FERR*[ERR387*]	156	CAS2*	208	SA0

Note: [xxx] for 386 mode
/xxx for non-cache mode

Pin Definition

Pin No.	Symbol	Type	Name and Function
95	ADS*	I	The *address status* input from CPU is an active low signal that indicates a valid bus cycle definition and address are available on the cycle definition lines and address bus.
102	M/IO*	I	*Memory I/O* Definition is an input for indicating an I/O cycle when low, and a memory cycle when high.
100	W/R*	I	*Write/Read* Definition is an input for indicating a read cycle when low, and a write cycle when high.
101	D/C*	I	*Data/control* Definition is an input for indicating a control cycle when low, and a data cycle when high.
98	CPURDY*	O	*CPU Ready* output indicates that the current bus cycle is complete and the CPU will terminate the current cycle.
36	HOLD	O	The bus *hold* request is used to request the control of the CPU bus. HLDA will be asserted by the CPU after completing the current bus cycle.
103	HLDA	I	*Hold acknowledge* comes from the CPU in response to a HOLD request. It is active high and remains driven during bus hold. HLDA indicates that the CPU has given the bus to another bus master.
112	NMI	O	*Non-maskable interrupt* is an active high signal to the CPU and is generated to invoke a non-maskable interrupt.
113	INTR	O	*Interrupt* goes high whenever a valid interrupt request is asserted. It interrupts the CPU, and is usually connected to the CPU's interrupt pin.
37	BS16*	O	*Bus Size 16* is an active low output. When actived, SiS85C460 initiates a memory, I/O, or interrupt acknowledge cycle (as qualified by the signals M/IO#, D/C#, and W/R#).

Pin Definiton (continued) **for 486 Mode**

Pin No.	Symbol	Type	Name and Function
115	A20M*	O	*A20 Mask* is the fast A20GATE output to the CPU. It remains high during power up of the CPU reset period, and will force A20 to go low when active.
88	KEN*	O	The 80486 CPU *cache enable* pin is used when the current cycle is cacheable to the internal cache of the 80486 CPU. It is an active low signal asserted by the SiS85C460 during cacheable cycle.
176	EADS*	O	*External address strobe* indicates that a valid external address has been driven onto the 80486 CPU address pins. This address will be used for the CPU to perform an intenal cache invalidation cycle.
104	FERR*	I	*Floating point error* from the 80486 CPU. It is driven active when a floating point error occurs.
105	IGNNE*	O	*Ignore numeric error* informs the 80486 CPU to ignore a numeric error.
106	BLAST*	I	The *burst last* signal indicates that the next time BRDY* is returned the burst bus cycle is complete.
107	BRDY*	I	*Burst ready* indicates that data presented is valid and is used for the 80486 CPU to sample the data during burst cycles.
116	PCD	I	*Page cache disable* pin reflects the state of the page attribute bits of the 80486 CPU.

Pin Definition (continued) **for 386 Mode**

Pin No.	Symbol	Type	Name and Function
115	CPUA20	I	*CPU Address A20* input.
88	ERR386*	O	*Error of 386 CPU* is an actived low output caused by ERR387. It is only active during CPU reset, and is inactive once reset is discontinued. Connect to 80386 ERROR input.
176	BZ386*	O	*Busy of 386 CPU* is an active low output caused by BZ387 input, and should be connected to 80386 BUSY input.
104	ERR387*	I	*Error of 387* is an active low input for indicating an error in the 387 cycle, and determining the presence of the 387 during CPU reset.
105	PREQ386	O	*Request of 386 CPU* is an active high output caused by PREQ387, and should be connected to 80386 PEREQ input.
106	PREQ387	I	*Request of 387* is an active high input from 80387 request output.
116	BZ387*	I	*Busy of 387* is an active low input from 80387 busy output.
107	NC		

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
120	LOCK*	I	The bus *lock* pin indicates that the current bus cycle is locked. The CPU will not allow other system bus masters access to the system bus while it is asserted.
121	LBD*	I	*Local bus device* cycle input for indicating a local bus device cycle. It can be connected to the MCS* output of Weitek 3167/4167.
122	LRDY*	I	*Local bus device ready* is an active low input, indicating that current local bus cycle is finished. It can be connected to the RDYOUT output of Weitek 3167/4167.
111-108	BE0-3*	I	*Byte enable* determine the bytes to be accessed during CPU or DMA cycles. During CPU cycles, they are decoded to generate SA1, SA0, and BHE*. During DMA or Master cycles, the reverse action occurs.
92,91, 87-76, 74-6 64	A2,A3, A4-A15, A16-A26 A31	I/O	CPU *address lines*. They will drive output during CPU hold.
208	SA0	I/O	*AT bus address 0* outputs address 0 for AT bus during AT and DMA cycle, and input address 0 for Master cycle. It outputs LOW, during 16-bit DMA cycle.
207	SA1	I/O	*AT bus address 1* outputs address 1 in AT and DMA cycle, and inputs address 1 in Master cycle.
196	BHE*	I/O	*Byte high enable* signal indicates that the high byte has valid data on the 16-bit data bus. This signal is always an output except in Master mode.
202	MEMR*	I/O	*AT-bus memory read* command signal is an output pin during AT/DMA/refresh/cycle and is an input in MASTER cycles. It is used to retrieve the data from memory.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
203	MEMW*	I/O	*AT-bus memory write* command signal is an output pin during AT/DMA cycle and is an input in MASTER cycles. This active low signal writes data into the selected memory.
204	SMEMR*	O	*AT-bus memory read,* it instructs the memory devices to drive data onto the data bus. It is active only when the memory to be accessed is within the lowest 1MB.
205	SMEMW*	O	*AT-bus memory write,* it instructs the memory devices to store the data present on the data bus. It is active only when the memory to be accessed is within the lowest 1MB.
3	IOR*	I/O	*AT-bus I/O read* command signal is an output pin during AT or DMA cycle and is an input in other cycles. When low, it strobes an I/O device for placing data on the data bus.
4	IOW*	I/O	*AT-bus I/O write* command signal is an output pin during AT or DMA cycle and is an input in other cycles. When low, it strobes data on the data bus into a selected I/O device.
172	BALE	O	*Bus address latch enable* is used on the system board to latch valid address and memory decodes from the CPU.
183	MEMCS16*	I	*16-bit memory chip select* indicates a 16-bit memory transfer when low, and 8-bit memory transfer when high.
184	IOCS16*	I	*16-bit I/O chip select* indicates that the current AT bus cycle is a 16-bit I/O transfer when low, and an 8-bit I/O transfer when high.
16	ZWS*	I	*Zero wait state* is an active low signal. The system ignores the state of IORDY* and immediately terminates AT bus current cycle without additional wait state when it is low.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
175	IORDY	I	*I/O channel ready* is normally high and can be pulled low by the devices on the AT slot bus to lengthen memory or I/O cycles by adding wait states.
185	MASTER*	I	*Master** is an active low signal from AT bus. When active, it indicates that another bus master has already taken over the control of the whole system, the address and control outputs are all in a high-impedence state.
173	AEN	O	*Address Enable* is used to degate the CPU and other device from the I/O channel to allow DMA transfers to take place.
1	CLKIN	I	*Oscillator clock input.*
14	CLKOUT	O	*Clock ouptut* for CPU clock.
94	CCLKIN	I	*Clock input* provides single chip controller an internal clock.
198	SYSCLK	O	*Bus clock* is the system clock for the AT bus. The frequency of the AT bus clock is software programmable, see configuration register 60 for detail.
2	14MHZ	I	*14MHz* is an input of 14.318 MHz, generated by an external oscillator. It is used to be the base clock for the timer, and DMA controller.
118	PWRGD	I	*Power good* is a power on reset input and SiS85C460 accepts valid inputs when this pin is high.
93	RSTCPU	O	*Reset CPU* is an active high output to reset the CPU.
199	RSTDRV	O	*Reset driver* is an active high output for a system reset.
6	HDEN*	O	*High Byte data enable* signal enables the high byte buffer of the SD bus.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Funciton
7	LDEN*	O	*Low Byte data enable* signal enables the buffer of the XD bus.
8	BDIR	O	*Data Buffer Direction* controls the direction flow of the buffer between the high byte SD and D15~D8 and the direction flow of the buffer between the XD and D7~D0. HIGH sets the data path from D15~D8 (D7~D0) to SD (XD) bus, LOW sets the data path from SD (XD) bus to D15~D8 (D7~D0).
9	SDIR	O	*SD low byte Data Direction* controls the direction flow of the low byte buffer between SD and XD. HIGH sets the data path from XD to SD, LOW sets the data path from SD to XD.
179 178 177	MPXS0/IRQ9 MPXS1/IRQ10 MPXS2/IRQ11	O	*Multiplexer I/O* selection pins. In non-cache scheme, they work as "Interrupt Request" (input) pins.
182 181 180	MPXI0/IRQ5 MPXI1/IRQ6 MPXI2/IRQ8	I	*Multiplexer I/O* input pins. In non-cached scheme, they work as "Interrupt Request" pins.
193~190 189~187	DACK0~3 DACK5~7	O	*DMA acknowledge* notifies the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. Reset initializes them to active low. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, these signals must be programmed to active low.
195	TC	O	*Terminal count* gives information concerning the completion of DMA services. A pulse is generated by the DMA controller when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers TC will be output when the TC for channel 1 occurs. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the Status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
117	SPK	O	*Speaker* is the output for the speaker.
11	ASRTC	O	*Address strobe of real time clock* device to latch the address from XD bus when CPU accesses the RTC.
12	DSRTC*	O	*Data read strobe of real time clock* device to drive data onto the XD bus when CPU accesses the RTC.
13	DWRTC*	O	*Data write of real time clock* device to store the data presented on the XD bus when CPU accesses the RTC. This pin must be connected to the R/W of RTC.
90	KBROMCS*	O	*Keyboard controller 8042 or system ROM chip selection.*
197	REF*	I/O	*Refresh* to initiate a refresh cycle. This signal is an input in master mode, and an output in other cycle.
138~141	RAS3~0*	O	*DRAM row address strobe.*
155~158	CAS3~0*	O	*DRAM column address strobe.*
159~163 166~171	MA10~6 MA5~0	O	*DRAM row/column address lines.*
134	MWE*	O	*Memory write enable* is an active low output signal for DRAM write enable.
145	MRE*/IOCHK*	O	*Memory read enable* is an active low output signal for DRAM read enable. In non-cache scheme, it is used as "I/O channel check".
123,124 125 126 127	TA7,6/IRQ15,14 TA5/IRQ12 TA4/IRQ7 TA3/IRQ3	I/O	*Tag RAM data bus lines.* *Interrupt requests* is executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge-triggered mode) or just a high level on an IRQ input (level-triggered mode). In non-cache scheme, they are defined as "Interrupt Request".

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
128~130	TA2~0/DRQ7~5	I/O	Tag RAM data bus lines. In non-cache scheme, they are defined as "DMA Request".
131	TAWE*/WIRQ	O	*Tag RAM* write enable is an active low signal. In non-cache scheme, it is defined as "Weitek 3167/4167 interrupt request".
136	KWEX*	O	*Cache write enable* for even bank.
137	KWEY*	O	*Cache write enable* for odd bank.
143	KREX*	O	*Cache read enable* for even bank.
144	KREY*	O	*Cache read enable* for odd bank.
148~151	KCE3~0*/ DRQ3~DRQ0	O	*Cache enable* pins are active low signal, indicating that the corresponding byte is accessed. In non-cache scheme, they are defined as "DMA Request".
132	ALT/DTURBO	I/O	*Alter* bit of cache indicating that data line has been written into. In non-cache scheme, it is used as an DE-TURBO pin.
133	ALTWE*/RC*	O	*Alter bit write enable* is the write strobe to the alter RAM. This signal is active low when cache read miss or cache write hit occurs, and is used to update the ALT bit. In non-cache scheme, Reset input from Keyboard controller will cause the CPU to be reset when this signal is low.
153	KA3Y/KA2/IRQ1	O	*KA3Y-Cache address 3* for odd bank when Cache interleave mode is used. *KA2-Cache address 2* when Cache non-interleave mode is used. *IRQ1-Interrupt requests* IRQ1 when non-Cache mode is used.
152	KA3X/KA3/IRQ4	O	*KA3X-Cache address 3* for even bank when Cache interleave mode is used. *KA3-Cache address 3* when Cache non-interleave mode is used. *IRQ4-Interrupt requests* IRQ4 when non-Cache mode is used.

Pin Definition (continued)

Pin No.	Symbol	Type	Name and Function
25,62, 26,48	PD0~3	I/O	*DRAM parity bits* generate parity bits in memory write cycle and accept parity bits in memory read cycle.
17~24	XD0~7	I/O	*Peripheral data bus* lines.
50~53 55~58	SD8~11 SD12~15	I/O	*Data bus* for the I/O devices.
27~34 39~42 44~47	D16~23 D24~27 D28~31	I/O	*Data bus* for the microprocessor, Memory, and I/O devices.
10,43, 61,97, 114,147, 165,201	VCC		*+5V DC Power*
5,15,35, 38,49,54, 59,60,75, 89,96,99, 119,135, 142,146, 154,164, 174,186, 194,200, 206	GND		*Ground*

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	°C
Storage temperature	-40	125	°C
Input voltage	-0.3	5.5	V
Output voltage	-0.5	5.5	V

Note:

Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_A = 0 - 70 °C, V_{DD} = 5 V ± 5 % , GND = 0 V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage	2.0	VDD+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL} = 4.0 mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH} = - 1.0 mA
I_{IL}	Input leakage current	-	±10	uA	$0 < V_{IN} < V_{DD}$
I_{OZ}	Tristate leakage current	-	±20	uA	$0.45 < V_{OUT} < V_{DD}$

AC Characteristics

T_A = 0 - 70 °C, V_{DD} = 5V ± 5%, V_{SS} = 0 V, C_L = 85/50* pF

Symbol	Parameter	Min	Typ	Max	Unit
T1	KCE* active delay*	3	7	12	ns
T2	KCE* inactive delay*	3	7	12	ns
T3	Tag address input setup time	8			ns
T4	BRDY* active delay*	3	8	14	ns
T5	BRDY* inactive delay*	3	6	10	ns
T6	BLAST* setup time	4			
T7	KEN* valid delay*	3	8	14	ns
T8	Cache Interleave KRE* active delay	3	7	11	ns
T9	Cache Interleave KRE* inactive delay	3	6	10	ns
T10	KA3X valid delay	3	9	14	ns
T11	KA3Y/KA2 valid delay	3	9	15	ns
T12	Cache Non-interleave KRE* active delay	3	9	15	ns
T13	Cache Non-interleave KRE* inactive delay	3	8	14	ns
T14	ADS* setup time	2			ns
T15	KWE* active delay	3	7	12	ns
T16	KWE* inactive delay	3	7	11	ns
T17	RDY* active delay	4	12	19	ns
T18	RDY* inactive delay	4	11	18	ns
T19	Tag address output valid delay	5	14	24	ns
T20	Tag address output floating delay	5	13	22	ns
T21	TAWE* active delay	4	12	20	ns
T22	TAWE* inactive delay	4	12	20	ns
T23	ALTWE* active delay*	4	11	17	ns
T24	ALTWE* inactive delay*	3	10	16	ns
T25	MRE* active delay	6	16	25	ns
T26	MRE* inactive delay	4	14	24	ns
T27	RAS* active delay	4	10	18	ns
T28	CAS* active delay	4	10	18	ns
T29	CAS* inactive delay	3	9	16	ns
T30	Column address valid delay	4	12	20	ns
T31	MWE* active delay	4	12	20	ns
T32	MWE* inactive delay	3	9	14	ns
T33	LBDY* setup time	4			ns
T34	LBCS* setup time	4			ns
T35	LBCS* hold Time	5			ns

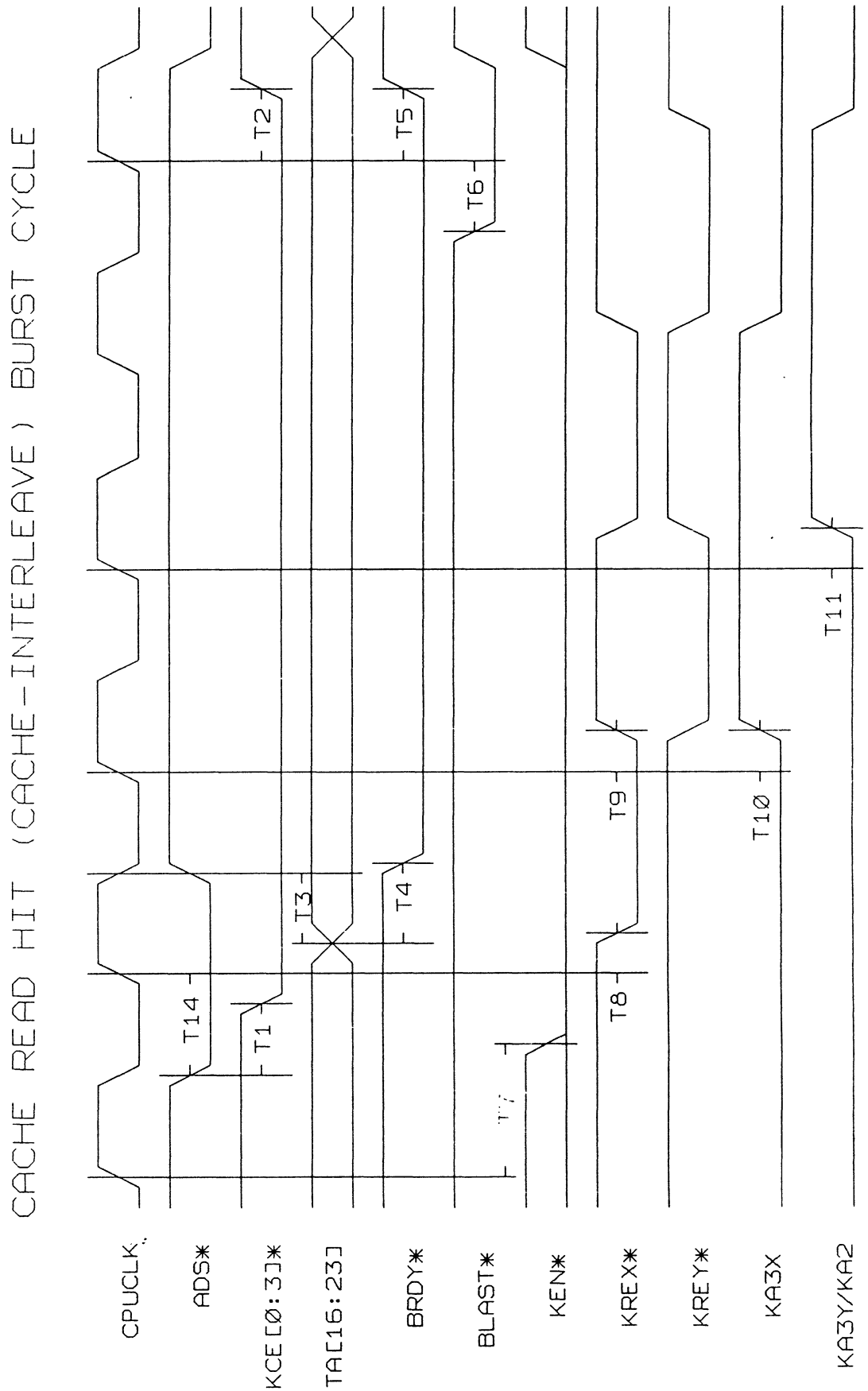
AC Characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
T36	RDY* from local bus setup time	4			ns
T37	RDY* from local bus hold time	5			ns
T38	RAS* inactive delay	4	9	16	ns
T39	Row Address valid delay	4	12	20	ns
T40	Fast cache write RDY* active delay	4	11	19	ns
T41	ALE active delay from SYSCLK falling	5	11	22	ns
T42	ALE inactive delay from SYSCLK	9	21	39	ns
T43	MEMCS16* set up time to SYSCLK	0			
T44	MEMCS16* hold time to SYSCLK	7			ns
T45	IOCS16* set up time to SYSCLK	4			ns
T46	IOCS16* hold time to SYSCLK	3			ns
T47	Command active delay from SYSCLK	8	16	29	ns
T48	Command inactive delay from SYSCLK	7	15	27	ns
T49	ZWS* set up time to SYSCLK	4			ns
T50	ZWS* hold time from SYSCLK	5			ns
T51	HDEN* active delay from BS16*	2	4	7	ns
T52	HDEN* inactive delay from BS16*	8	15	30	ns
T53	SDIR, BDIR active delay from BS16*	5	12	22	ns
T54	SDIR, BDIR inactive delay from BS16*	3	7	13	ns
T55	Data conversion SA0 delay from SYSCLK	6	14	26	ns
T56	Data conversion SA0 delay from SYSCLK	10	23	43	ns
T57	Address bus valid delay from REF*	5	12	22	ns
T58	Address bus float delay from REF*	7	23	44	ns
T59	Address set up time to IOR*, IOW* active	16			ns
T60	Address hold time from IOR*, IOW* inactive	0			ns
T61	SDIR,BDIR delay from command active	8	18	33	ns
T62	SDIR,BDIR delay from command inactive	20	45	84	ns
T63	SDEN*,HDEN* delay from command active	8	19	36	ns
T64	SDEN*,HDEN* delay from command inactive	20	19	36	ns
T65	Data active delay form BS16*	3	7	12	ns
T66	Data valid delay from SYSCLK	19	21	39	ns
T67	Data float delay from BS16*	3	7	12	ns
T68	D15-0 data set up time to command inactive	15			ns
T69	D15-0 data hold time to command inactive	8			ns
T70	D7-0 data valid delay from SYSCLK	10	18	30	ns
T71	D15-8 data valid delay from SYSCLK	7	16	26	ns
T72	D23-16 data valid dealy from SYSCLK	8	20	39	ns
T73	D31-24 data valid delay from SYSCLK	16	38	48	ns
T74	D15-0 data valid delay from D31-16 valid	9	15	27	ns
T75	D7-0 data valid delay from D31-24 valid	15	35	65	ns
T76	D7-0 data valid delay from D23-16 valid	6	14	26	ns
T77	D7-0 data valid delay from D15-8 valid	9	13	39	ns
T78	Data active delay from command active	16	29	54	ns
T79	Data float dealy from command inactive	10	15	28	ns

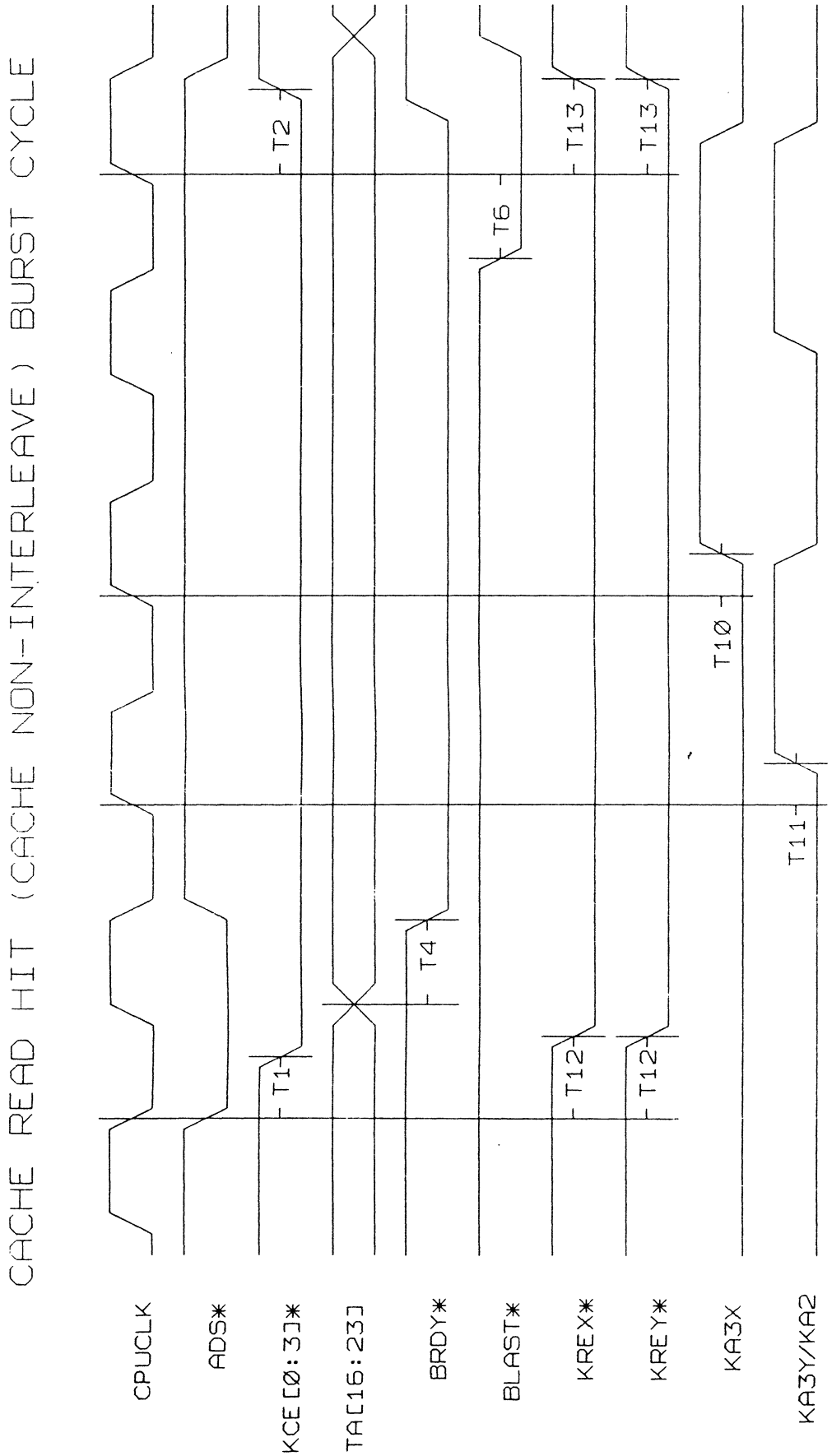
AC Characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
T80	DMA clock delay form bus clock			8	ns
T81	Low byte address valid delay			50	ns
T82	Low byte address invalid delay			45	ns
T83	Page address valid delay			60	ns
T84	Page address invalid delay			47	ns
T85	DACKn* active delay			41	ns
T86	DACKn* inactive delay			34	ns
T87	IOR* or MEMR* active delay			30	ns
T88	IOR* or MEMR* inactive delay			36	ns
T89	IOR* or MEMR* hold time	0			ns
T90	IOW* or MEMW* active delay			32	ns
T91	IOW* or MEMW* inactive delay			31	ns
T92	TC active delay			30	ns
T93	TC inactive delay			42	ns
T94	RSTDRV active delay	4	9	16	ns
T95	RSTDRV inactive delay	6	15	26	ns
T96	RSTCPU active delay*	2	6	11	ns
T97	RSTCPU inactive delay*	3	7	12	ns
T98	RSTCPU duration	25			CCLKIN

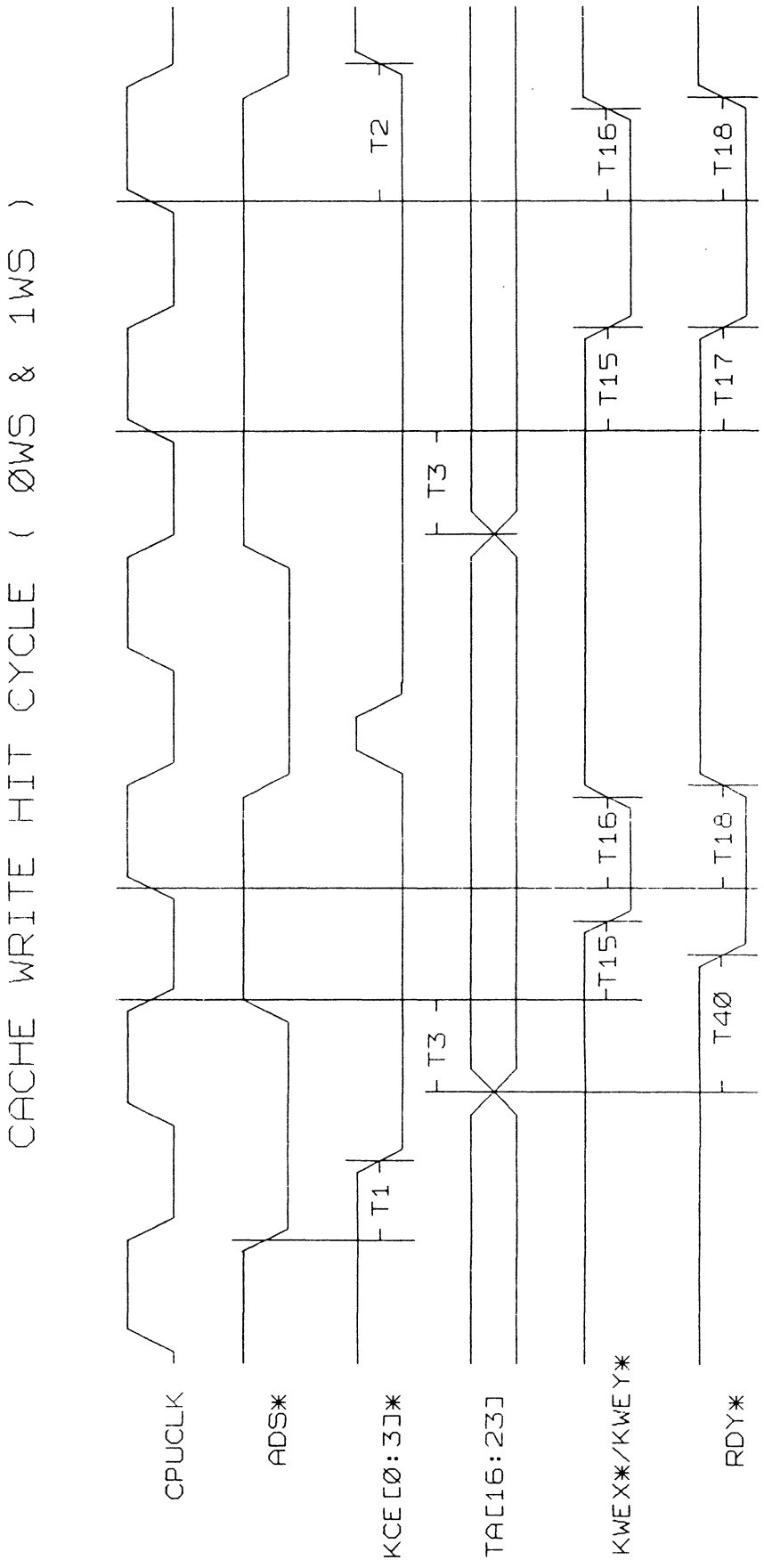
Timing Diagram for 486 Mode



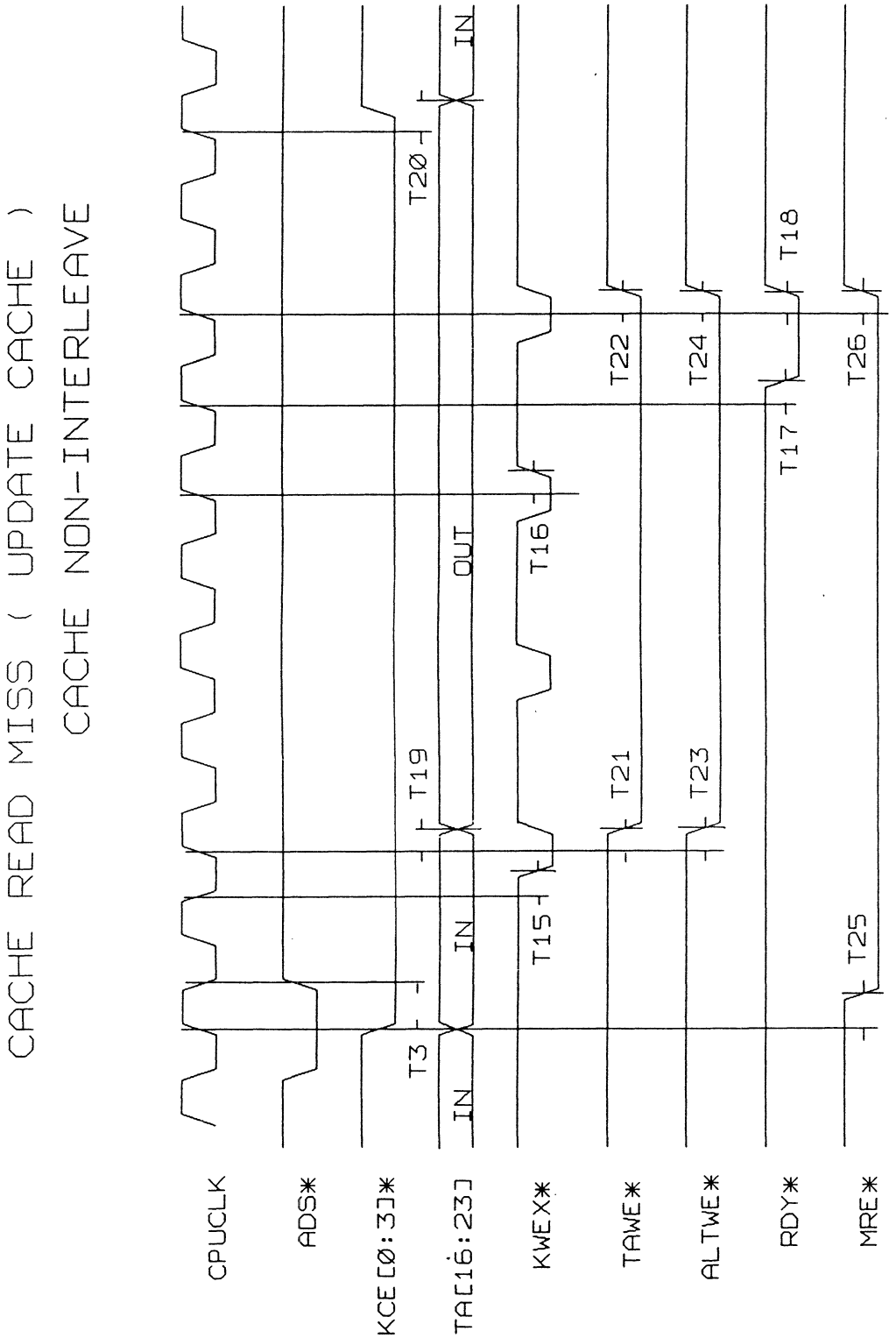
Timing Diagram for 486 Mode



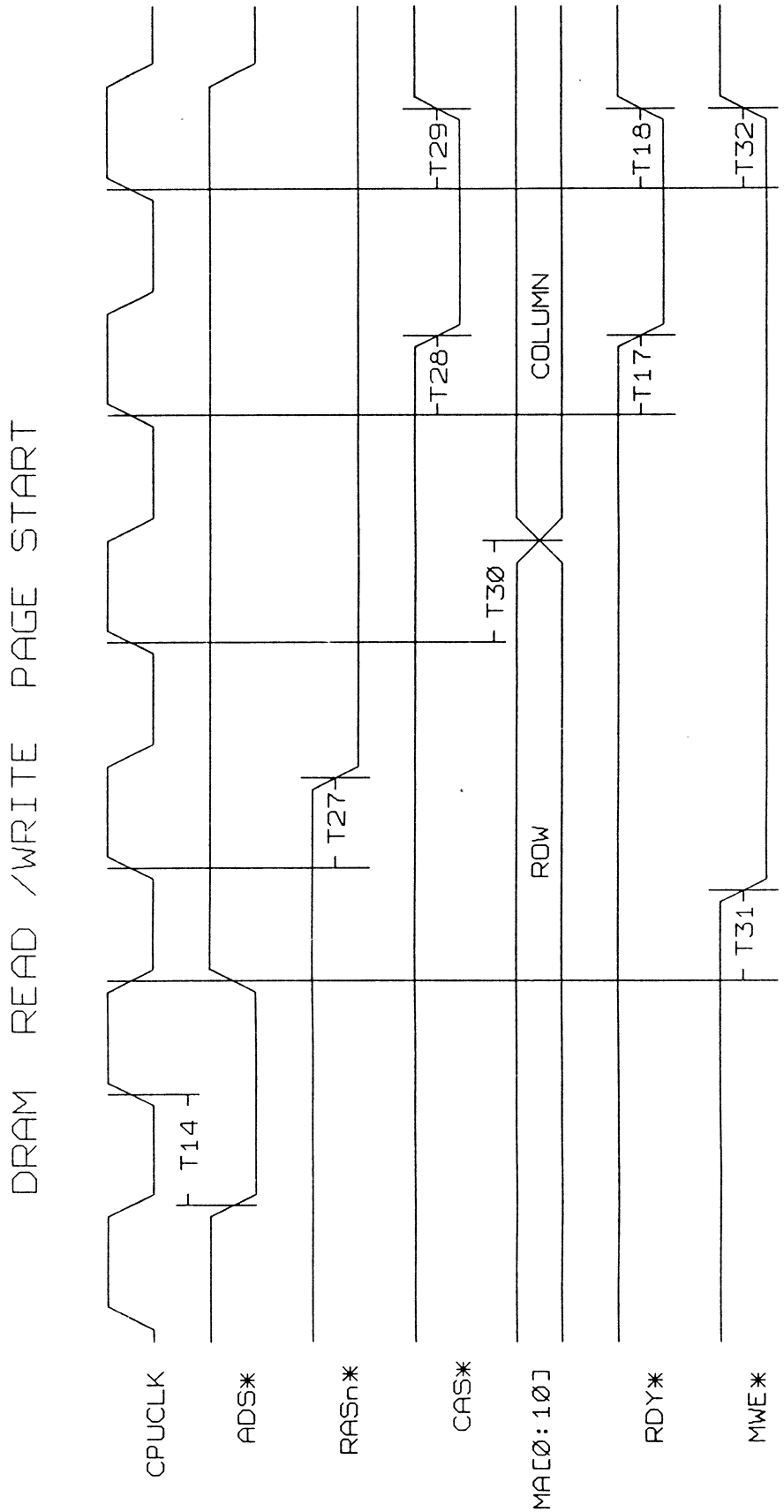
Timing Diagram for 486 Mode



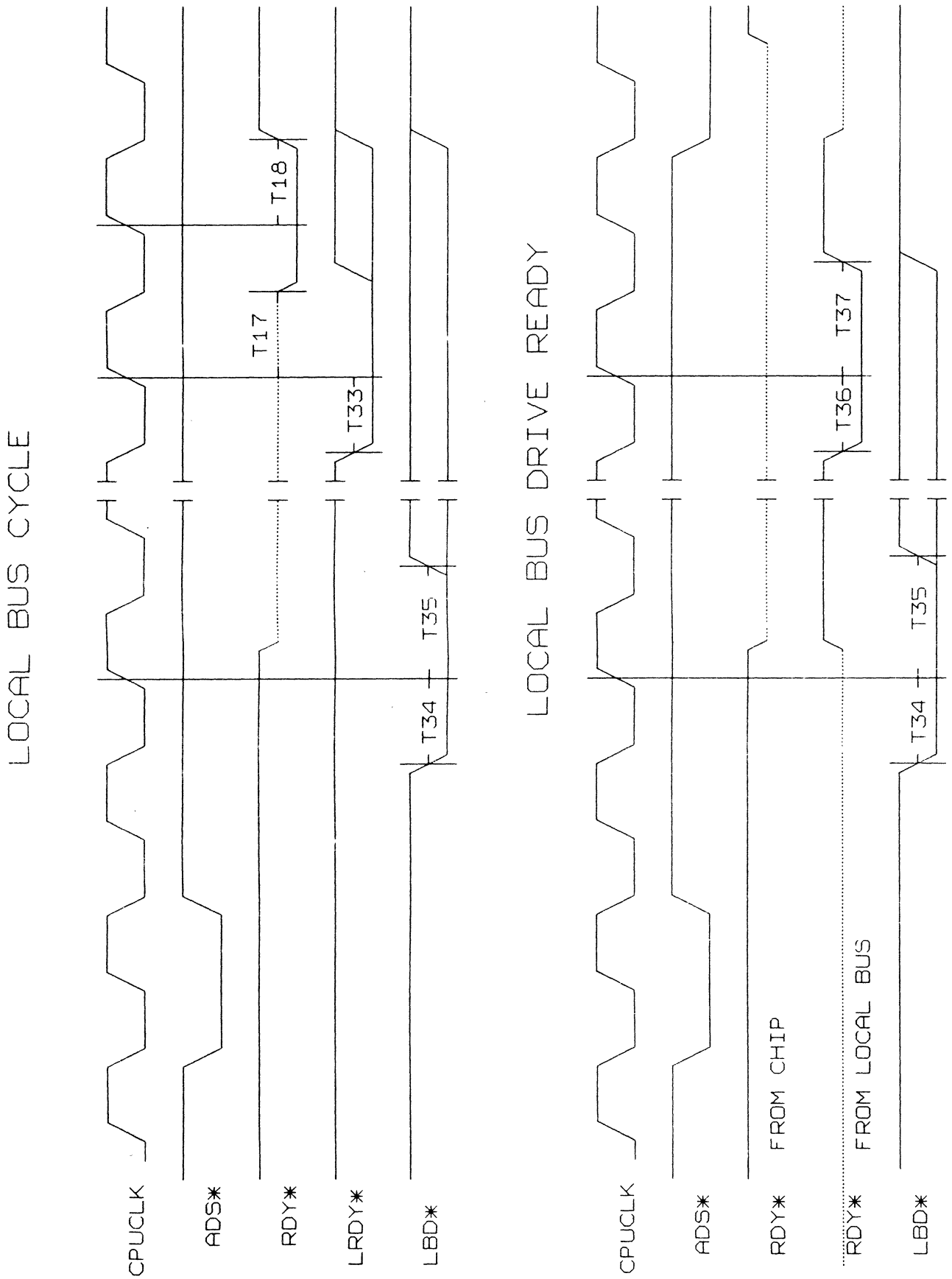
Timing Diagram for 486 Mode



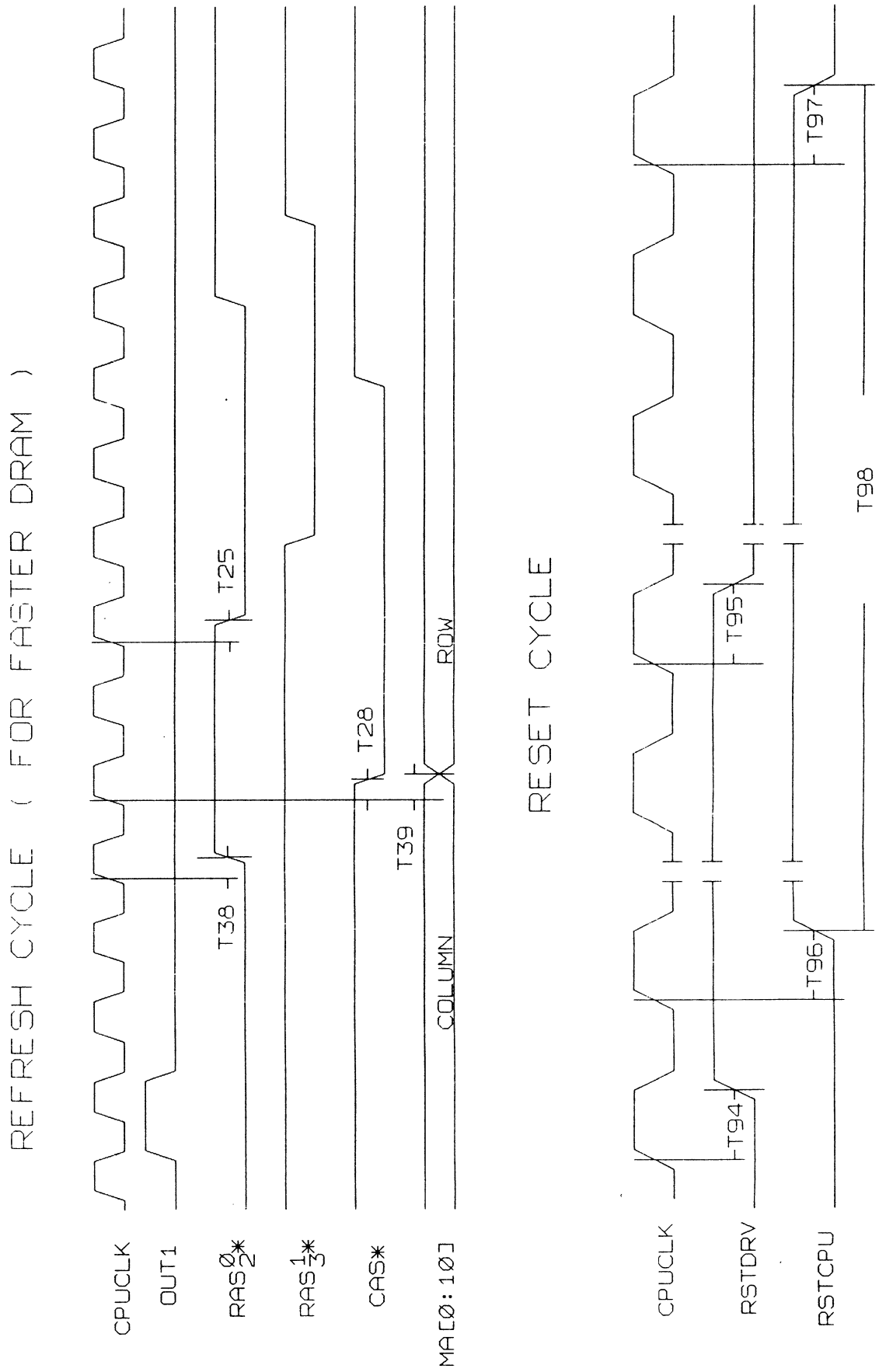
Timing Diagram for 486 Mode



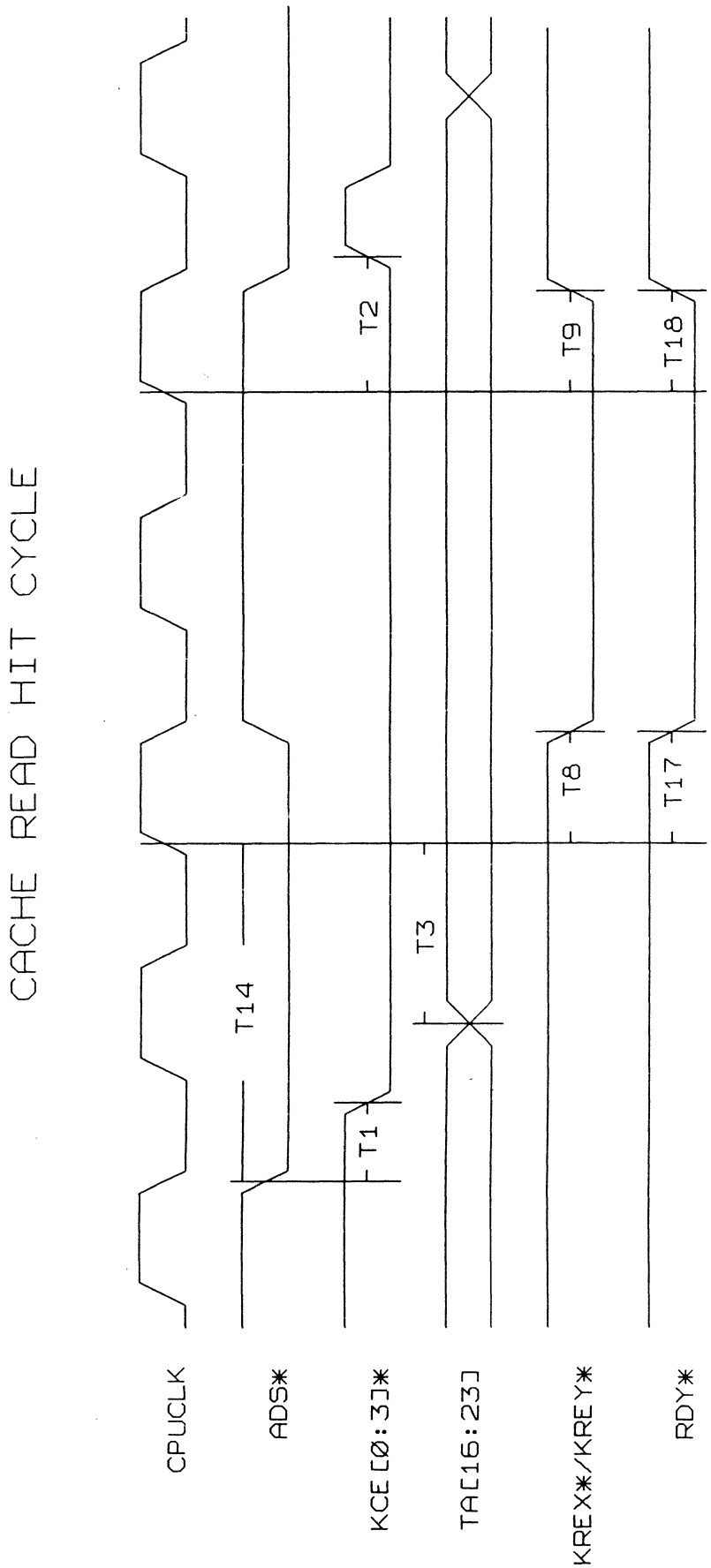
Timing Diagram for 486 Mode



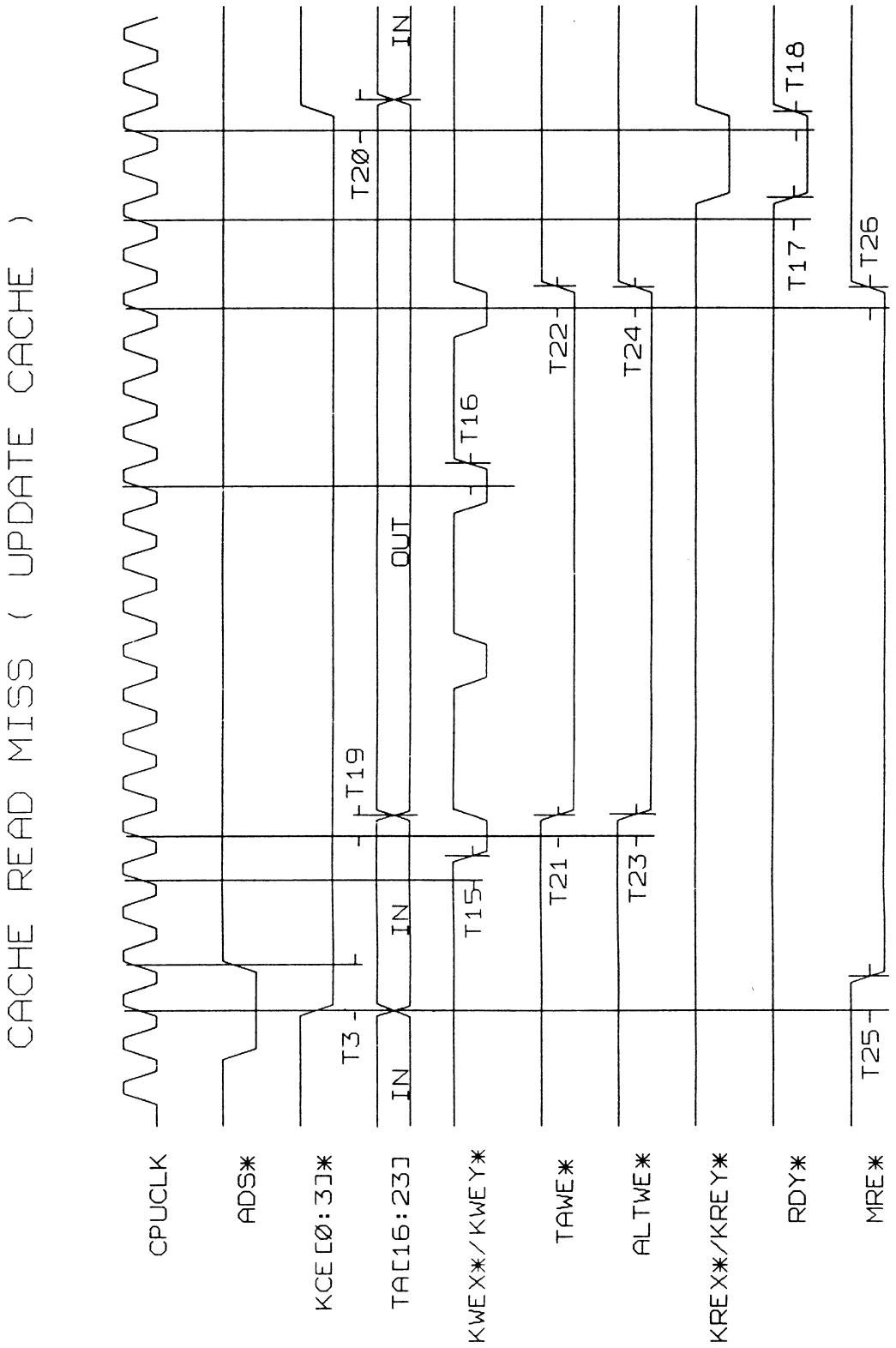
Timing Diagram for 486 Mode



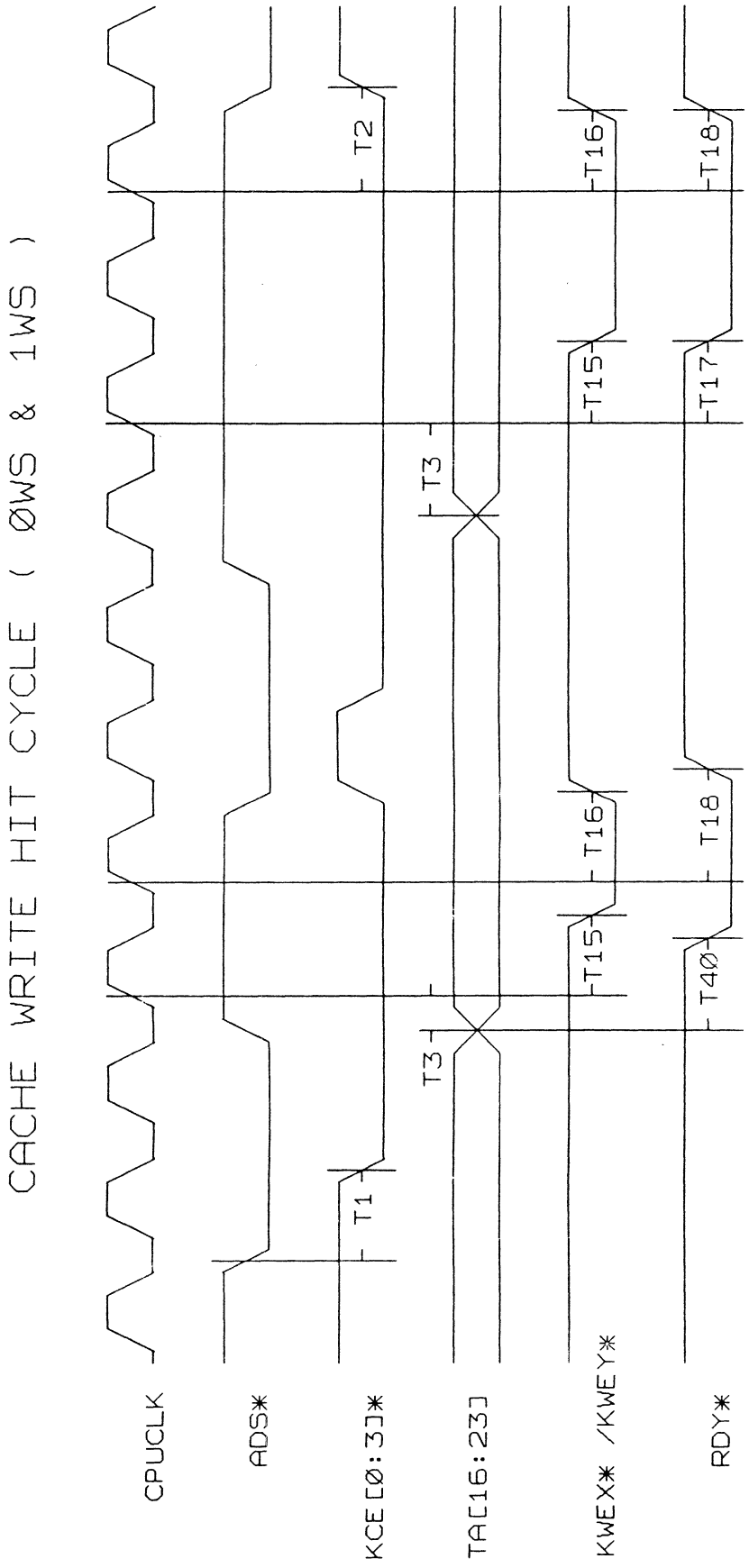
Timing Diagram for 386 Mode



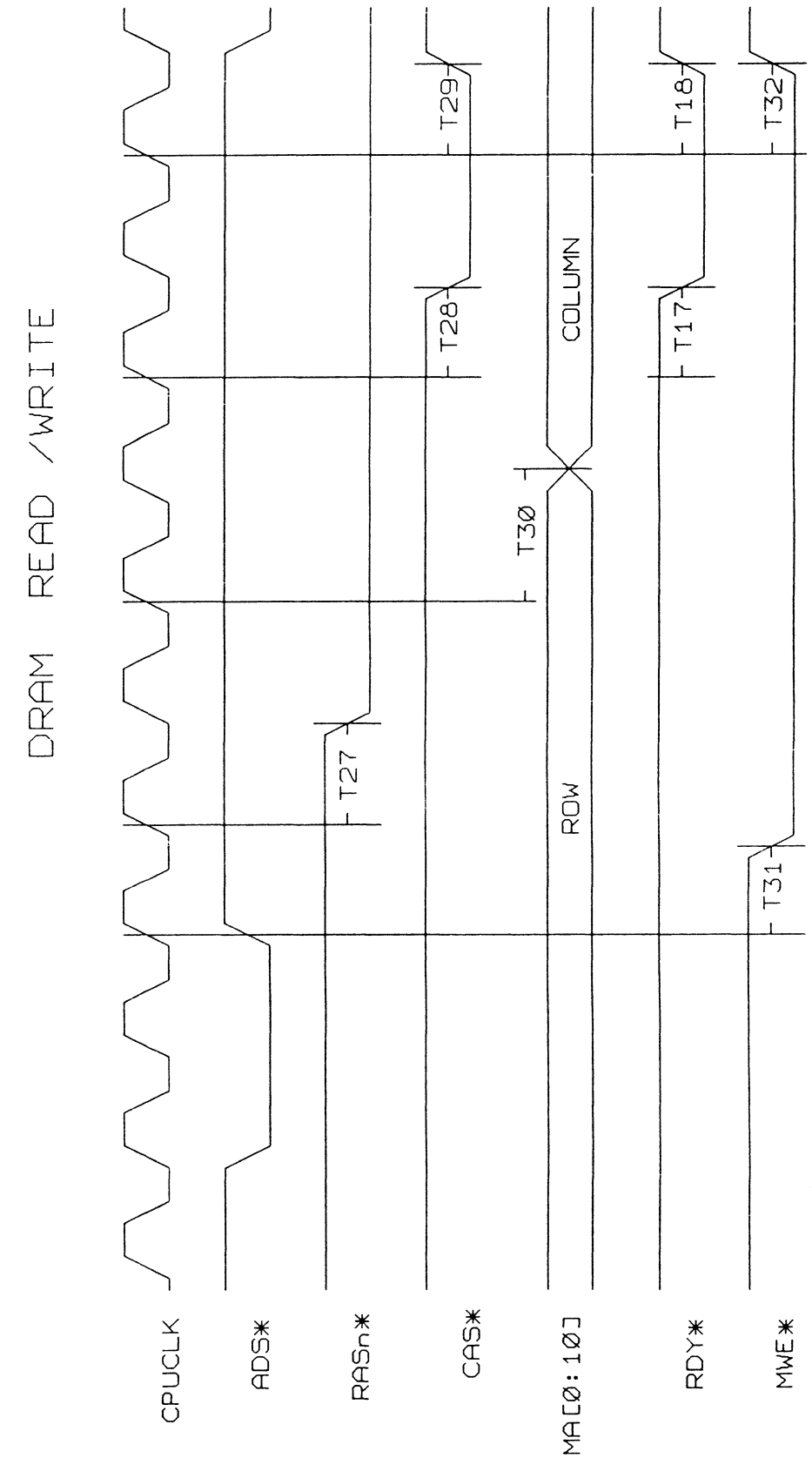
Timing Diagram for 386 Mode



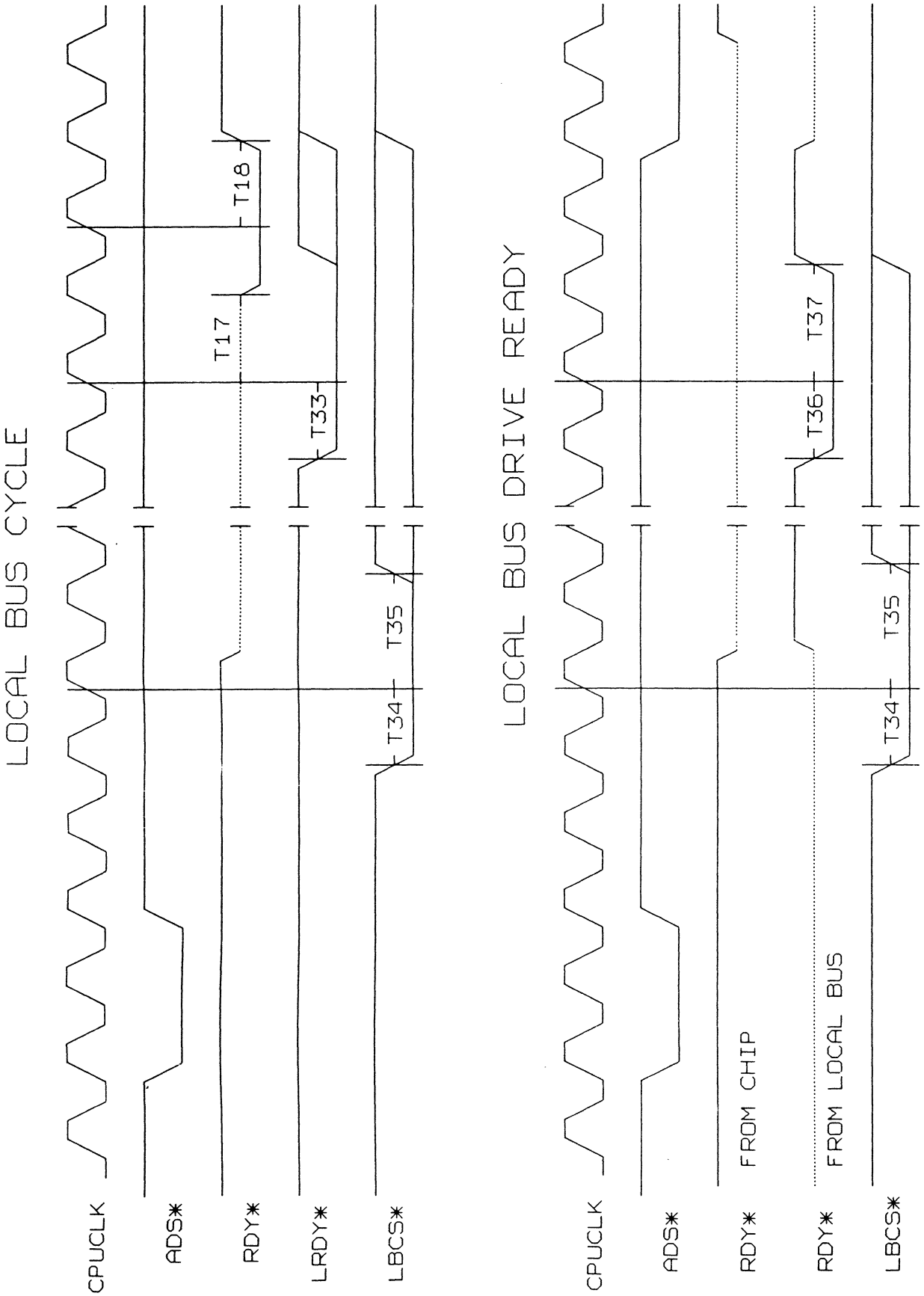
Timing Diagram for 386 Mode

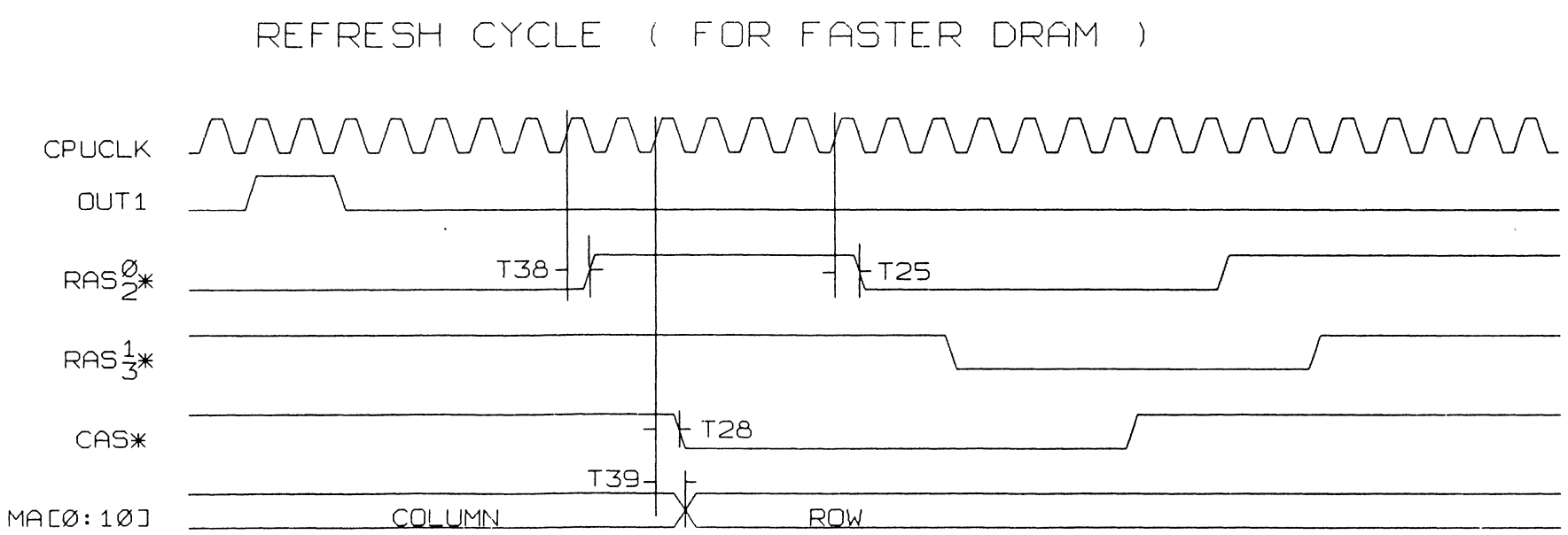


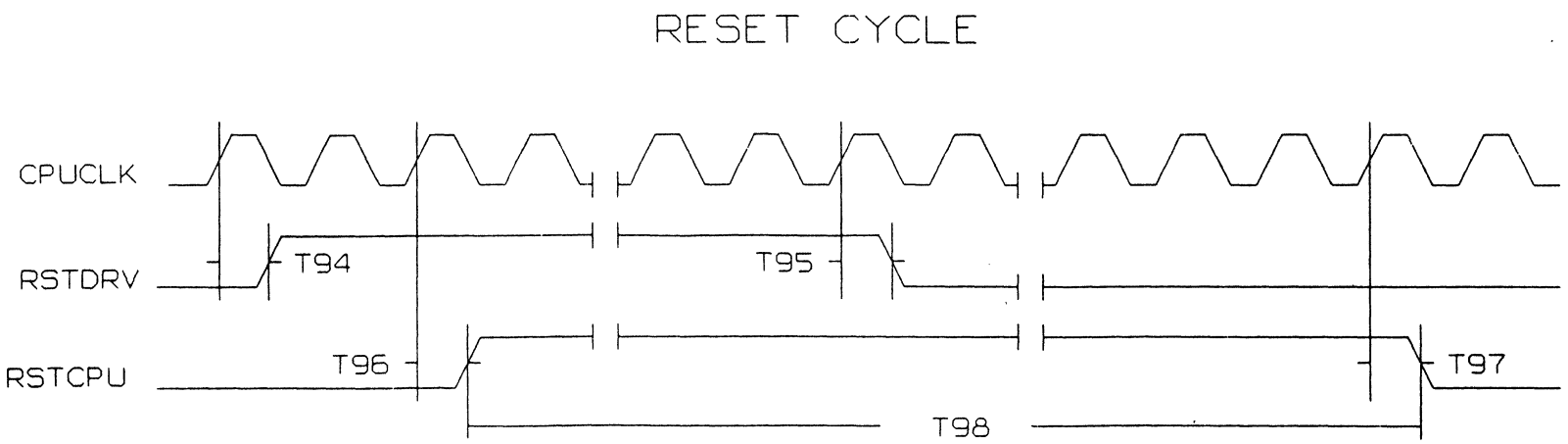
Timing Diagram for 386 Mode



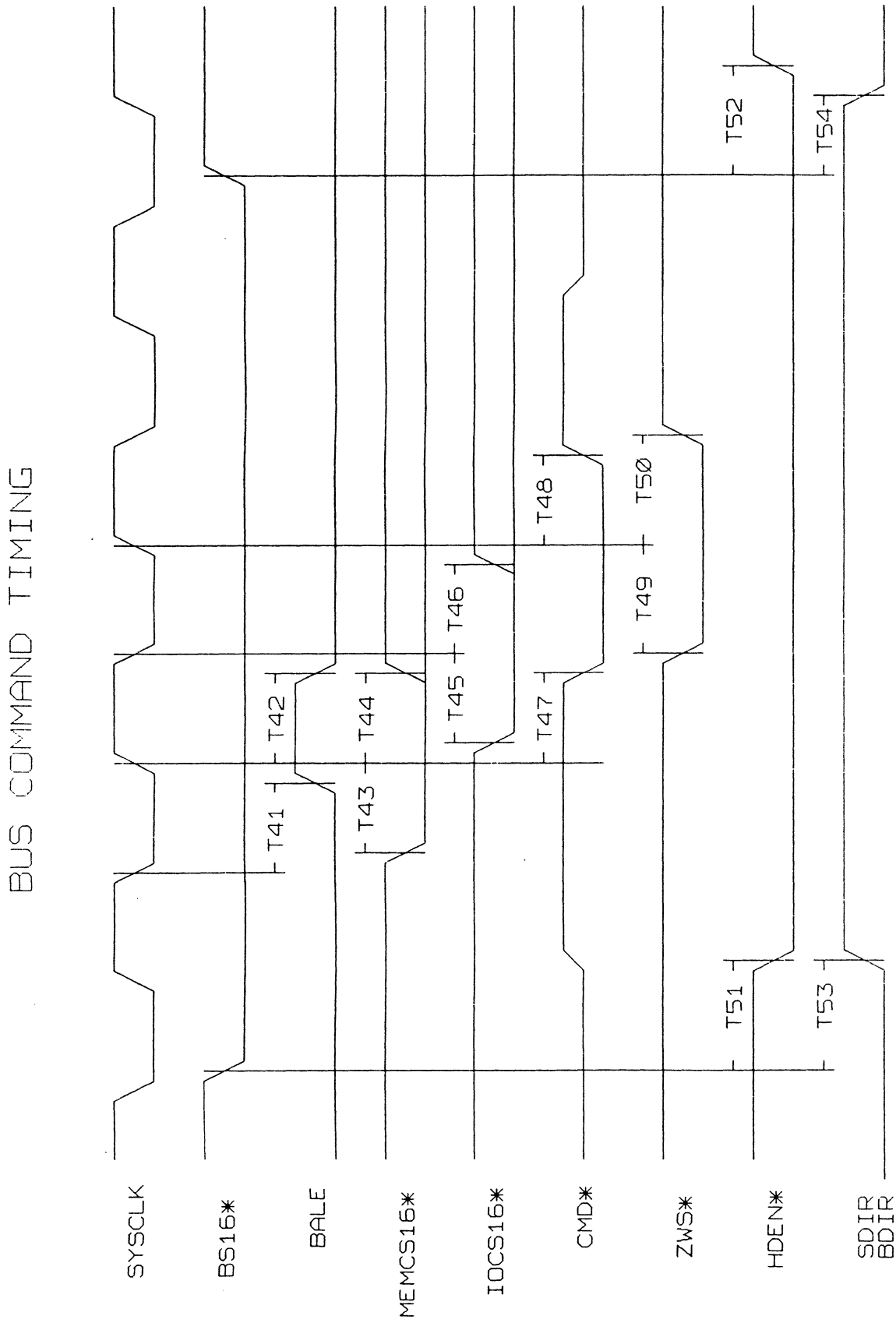
Timing Diagram for 386 Mode



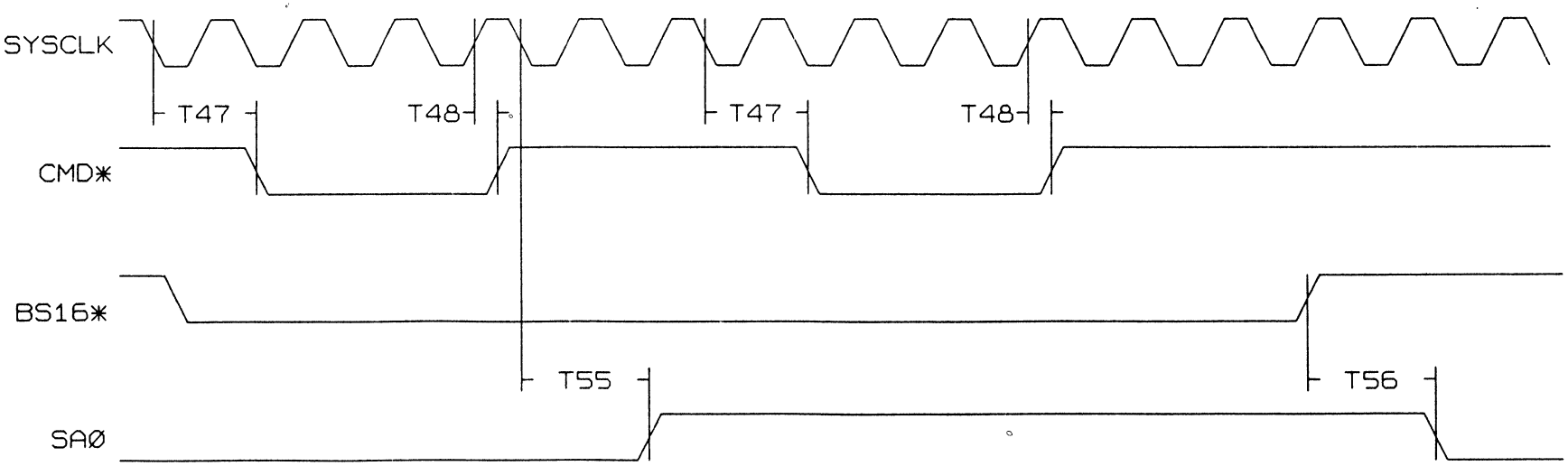

REFRESH CYCLE (FOR FASTER DRAM)
CPUCLK
OUT1
RAS Ø/2*
RAS 1/3*
CAS*
MA[Ø:1Ø]
T38
T25
T28
T39
COLUMN
ROW


RESET CYCLE
CPUCLK
RSTDRV
RSTCPU
T94
T95
T96
T97
T98

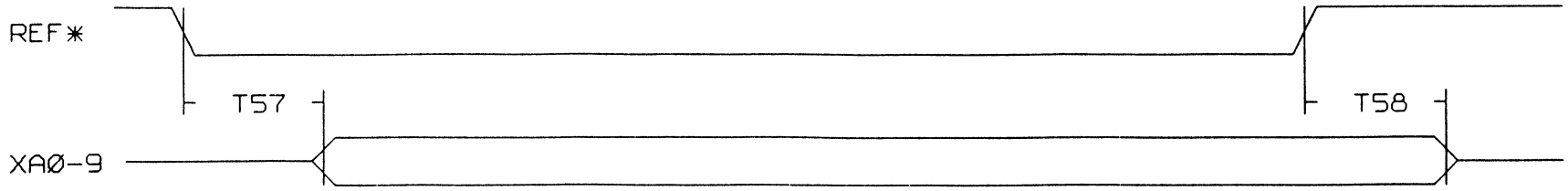
Timing Diagram



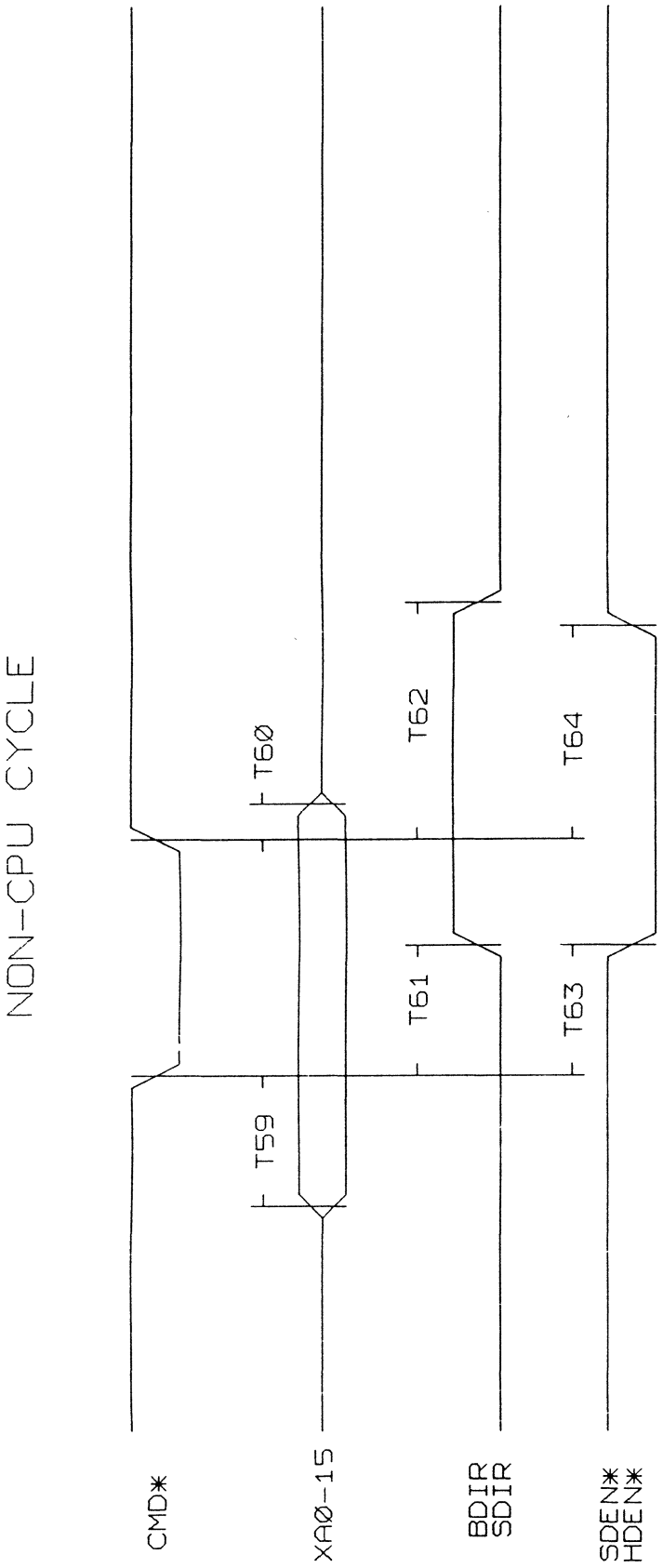
DATA CONVERSION CYCLE



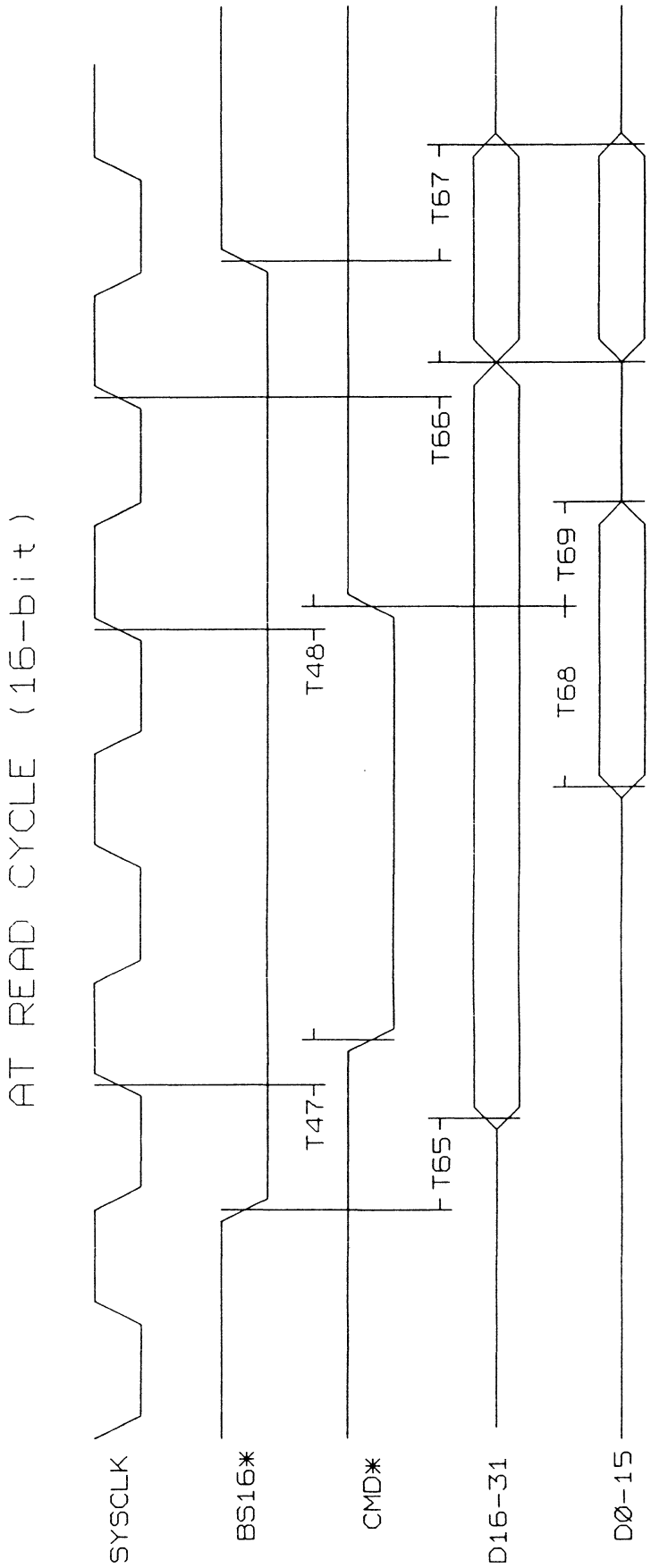
REFRESH CYCLE



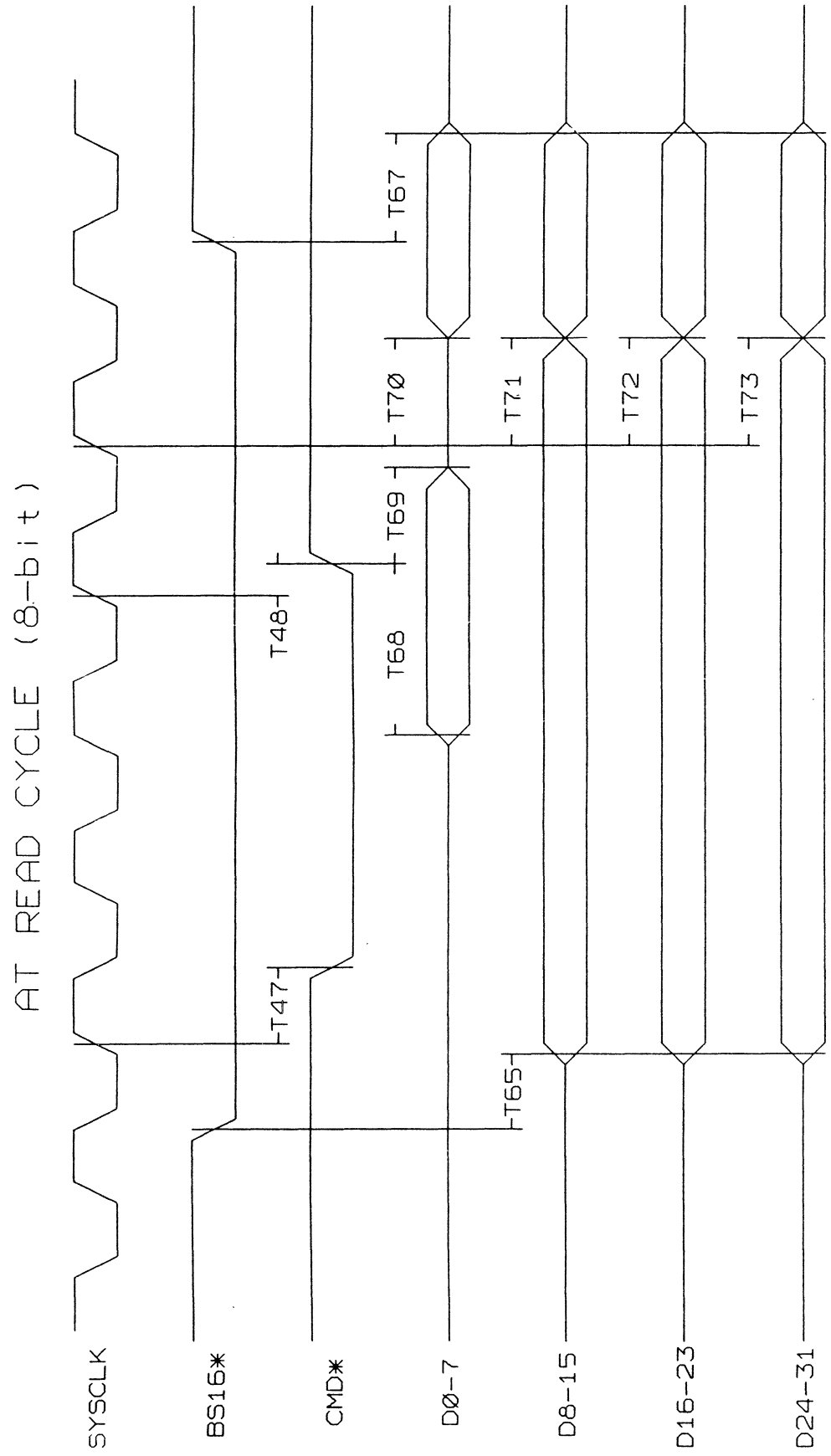
Timing Diagram



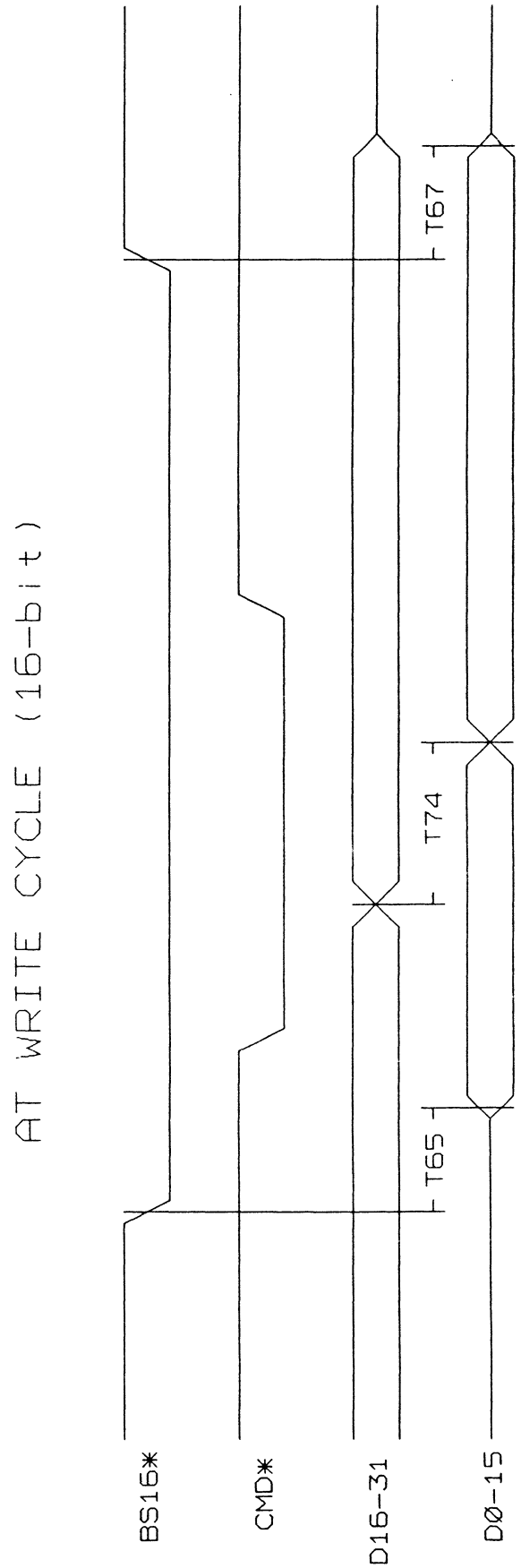
Timing Diagram



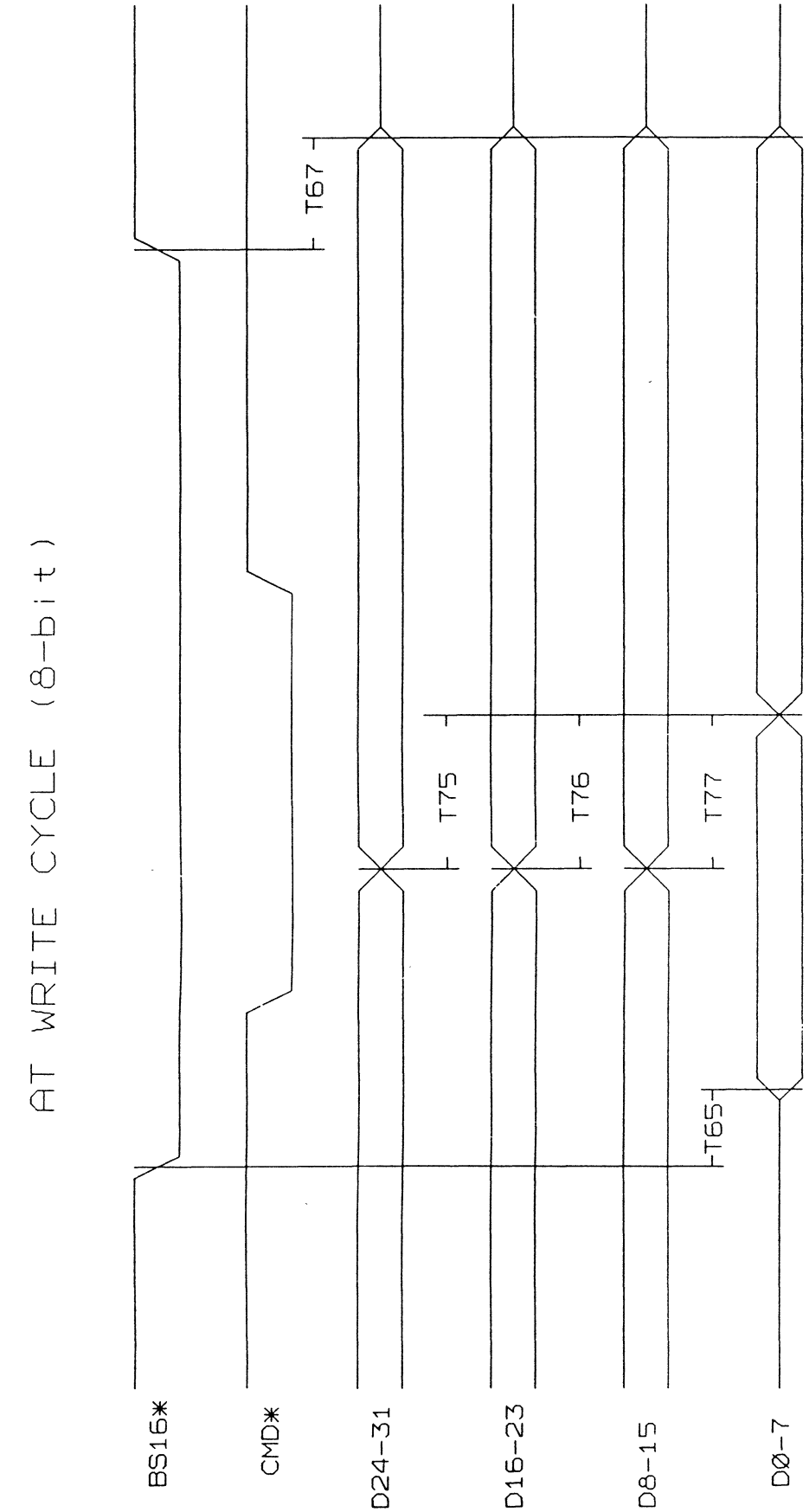
Timing Diagram



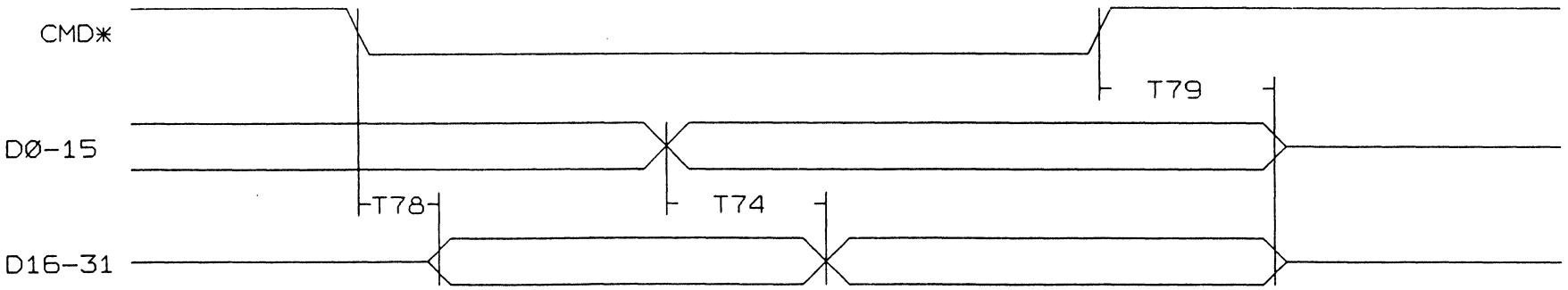
Timing Diagram



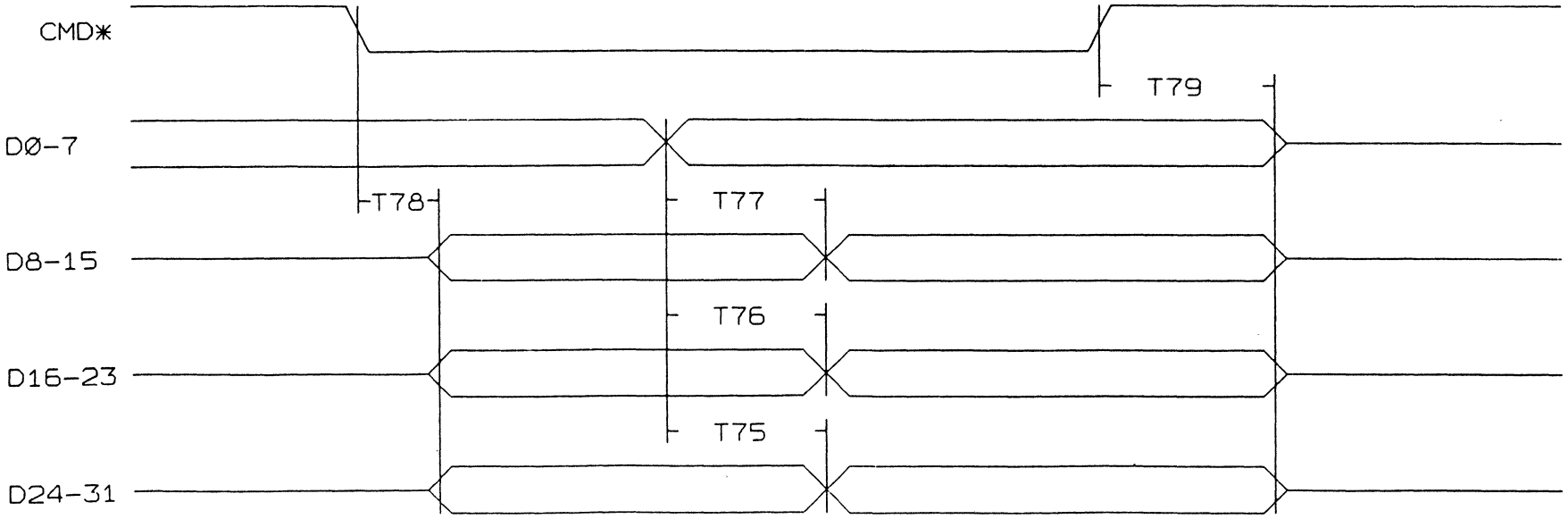
Timing Diagram



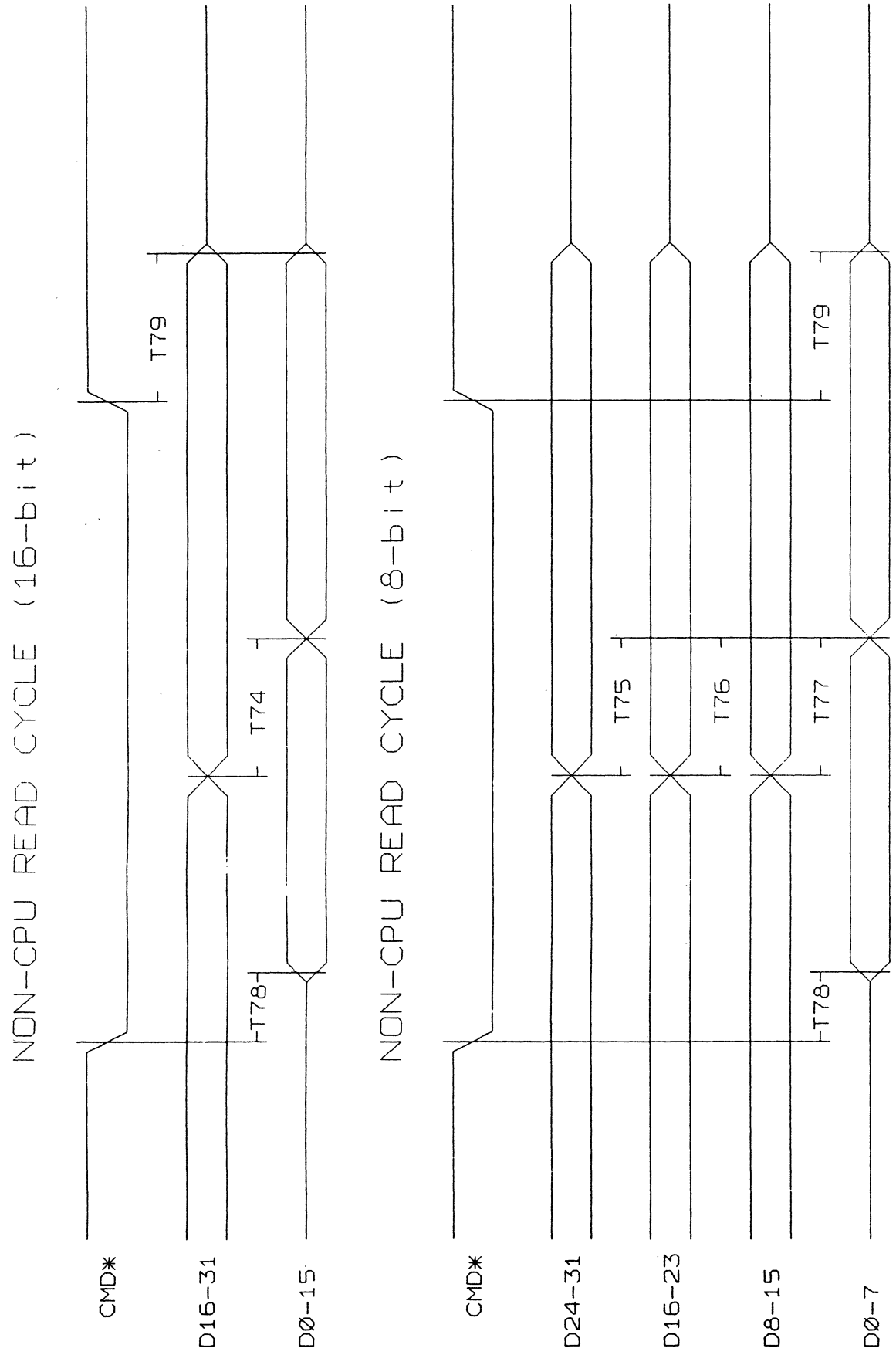
NON-CPU WRITE CYCLE (16-bit)



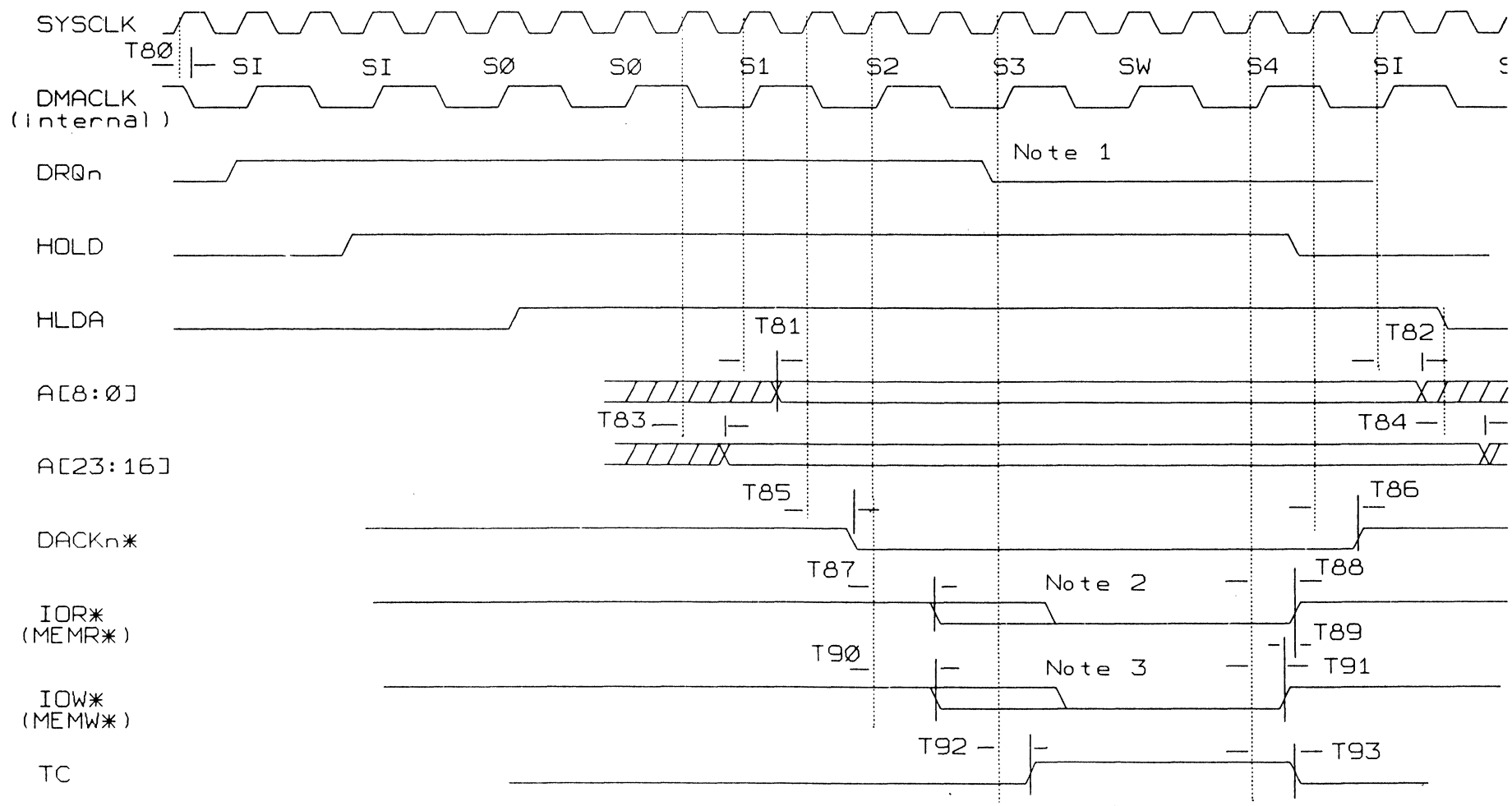
NON-CPU WRITE CYCLE (8-bit)



Timing Diagram



DMA TIMING



Note 1 : DREQ should be held active until DACK is asserted .
Note 2 : The first high to low transition is for normal read .
The second transition is for delay MEMRD# .
Note 3 : The first high to low transition is for extended write .
The second transition is for normal write .

MECHANICAL DIMENSION (FOR SiS85C460)

QFP208-P (208-Pin Plastic Flat Package) Unit: mm