SONY

Semiconductor IC

Data Book 1987
A/D,D/A Converters & D.S.P.

SONY
A/D,D/A Converters & D.S.P.
1987

SONY®

Semiconductor Integrated Circuit Data Book 1987

Semiconductor Integrated Circuit Data Book
1987

SONY®

PREFACE

This is the 1987 version of the Sony semiconductor IC databook. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The Sony semiconductor IC databook has been edited to include only accurate and reliable data. However, because of technical improvements and other modifications the contents are subject to change without notice.

The circuit examples used in this book are for illustration of typical applications only; we are not responsible for any problems that may occur in the circuitry and patents of any third party if these examples are put in practice.

Package abbreviations

DIP : Dual Inline Package
MFP : Mini Flat Package (=Flat DIP)
QIP : Quad Inline Package (=Flat QUIP)
PGA : Pin Grid Array
SRK : Shrink Dual Inline Package
SIP : Single Inline Package

Contents

1. List of Model Names

2. Index by Usage

1) A/D, D/A Converters — Audio —

Type	Function	Page
CX20017	Dual 16bit 44kHz Multiplexed D/A Converter	23
CX20018	Dual 16bit 44kHz Multiplexed A/D Converter	37
CX20133	16bit D/A Converter	56
CX20152	Dual 16bit 88kHz Multiplexed D/A	69
CX23010 CX23060	Dual 10bit 50kHz Multiplexed A/D + D/A	87

2) A/D, D/A Converters — Video —

Type	Function	Page
CX20051A	10bit 30MHz D/A Converter	105
CX20052A	8bit 20MHz Sub-ranging A/D Conveter	116
CX20116/U CXA1066K/UK	8bit 100MHz Flash A/D Converter	125
CX20201A-1/-2/-3 CX20202A-1/-2/-3	10/ 9/ 8bit 160MHz D/A Converter	132
CX20206	8bit 35MHz RGB 3-channel D/A Converter	144
CX20220A-1/-2	10/ 9bit 20MHz Sub-ranging A/D Converter	160
CXA1008P/1009P	High-speed Sample and Hold Amplifier	174
CXA1016P/K/UK CXA1056P/K/UK	8bit 30/50MHz Flash A/D Converter	186
CXA1096P	8bit 20MHz Flash A/D Converter (P)	196
CXA1106P	8bit 35MHz High-speed D/A Converter (P)	203
BX-1300	8bit 20MHz A/D Converter Module	208

(P) : Preliminary

3) Digital Signal Processors

Type	Function	Page
CX-7997	10 × 10bit 15MHz Multiplier/Adder	219
CX23024 CX23067	8bit S-P-S Converter	230
CX23034	Digital Filter for CD	238
CX23038	Programmable Shift Register	249
CX23043	10bit Synchronous Binary Counter	257
CXD1018G	Degital Signal Processing Multipler	266
CXK1201P	Double Scan Converter (P)	283
CXK1202S	Digital Delay Line	295

(P) : Preliminary

4) Evaluation Printed Circuit Boards

Type	Function	Page
CX20017 PCB	CX20017 Evaluation Board	307
CX20018 PCB	CX20018 Evaluation Board	311
CX20052A PCB-3A/3B	8bit 20/15MHz A/D Converter Evaluation Board	322
CX20116/U CXA1066K/UK } PCB	8bit 100MHz A/D Evaluation Board	328
CX23060 PCB	CX23060 Evaluation Board	336
CXA1016P/K/UK CXA1056P/K/UK } PCB	8bit 50MHz/30MHz A/D Evaluation Board	343
FCX20220A-1/-2	10bit/9bit 20MHz Sub-ranging A/D Converter Evaluation Board	352

5) Application Notes

Type	Function	Page
CX20052A	8bit 20MHz Sub-ranging A/D Converter	363
CX20116/U CXA1066K/UK CXA1056P/K/UK CXA1016P/K/UK	8bit High-speed A/D Converter	370

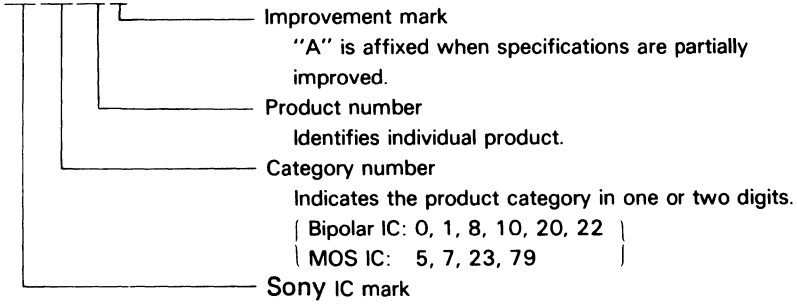
3. IC Nomenclature

1. Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

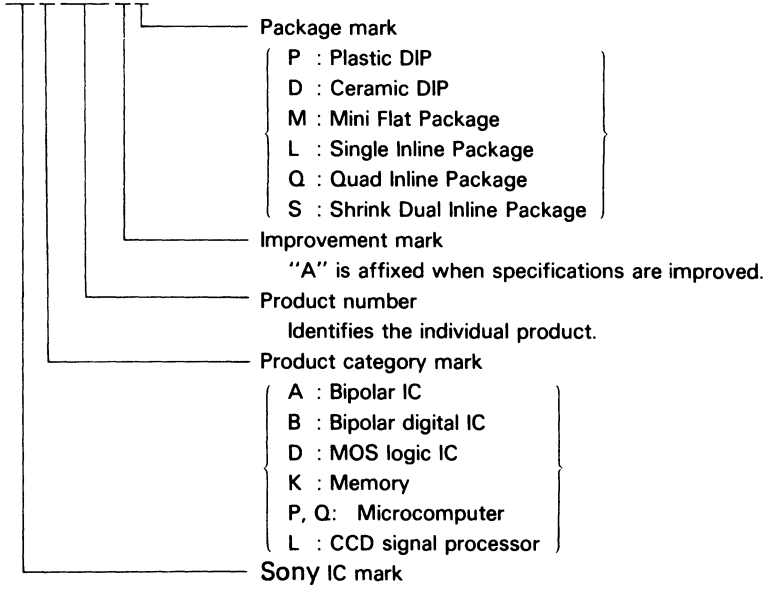
a) Conventional nomenclature system

[Example] CX20011A



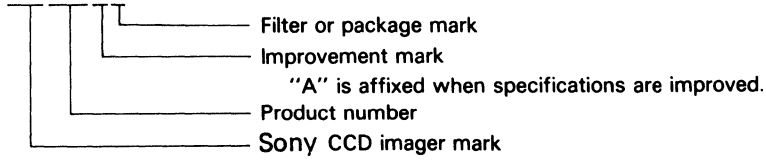
b) New nomenclature

[Example] CXA1001AP



2. Nomenclature for CCD image product name

[Example] ICX016AK



4. Precautions for IC Application

A) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even in a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably short.

Maximum rating must never be reached for two items at the same time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply terminal and ground terminal.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit; the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with the amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

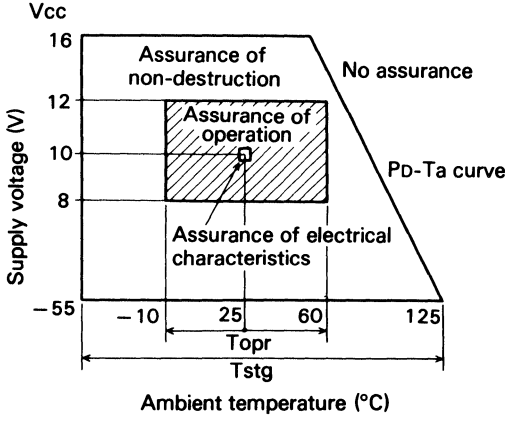
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



B) Protection against electrostatic breakdown

There have been problems of electrostatic destruction of electronic devices since the 2nd World War. Their history is closely related to the advancement in the semiconductor devices; that is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

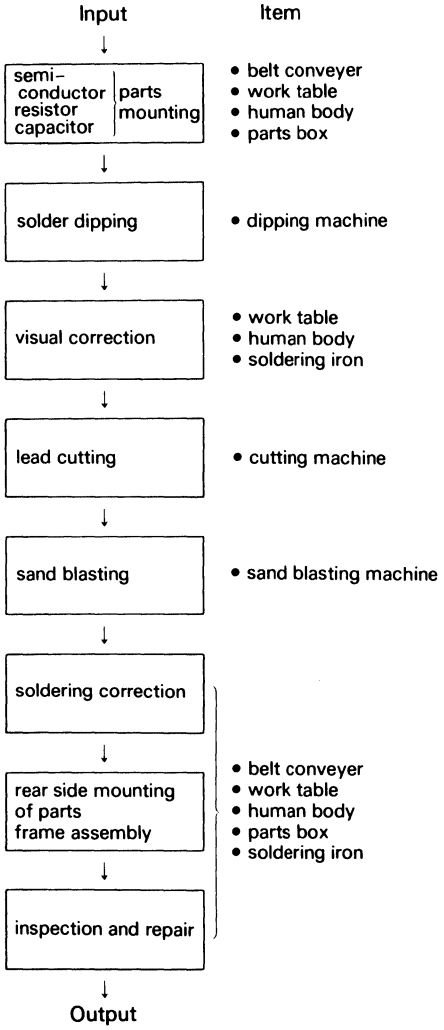
Today, the problem of electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing electrostatic destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for preventing electrostatic destruction

Explained below are procedures that must be taken in fabrication for preventing the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

① Equalize potentials of terminals when transporting or storing.

② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③ Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room about 50%.

Operator

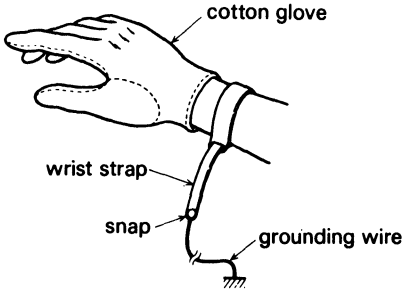
1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If wrist strap cannot be used, then the operator should touch the grounding point with his hand, before handling any semiconductor device.

example of grounding band

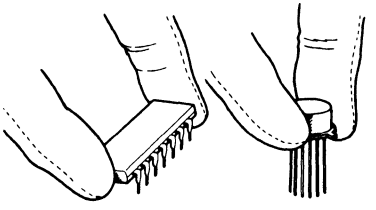


When using a copper wire for grounding, connect a 1M resistance in series near the hand for safety.

3) Handling of semiconductor device

Do not touch the lead. Touch the body of semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

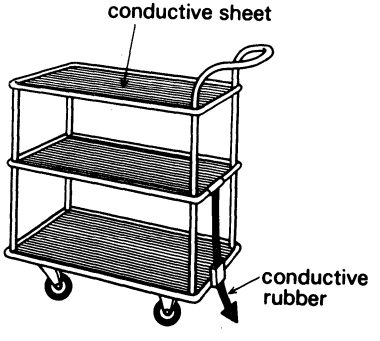
1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

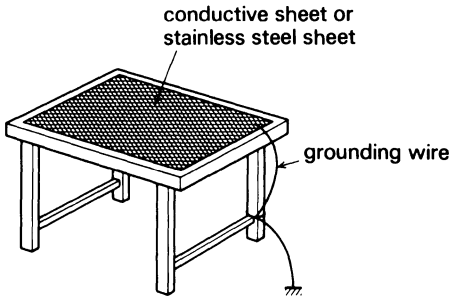
grounding of carrier



2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

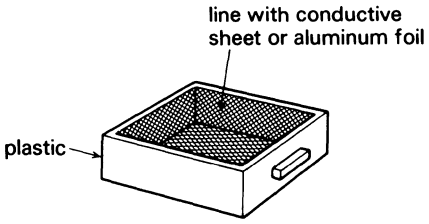
grounding of work table



3) Semiconductor device case

Use the metal case, or the antistatic plastic case (lined with conductive sheet or aluminum foil).

plastic case for semiconductor devices



4) Insertion of semiconductor device

Insert the semiconductor device in mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or a wood or metal carrier.

5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

6) Other points of caution

Take note of the kind of the brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

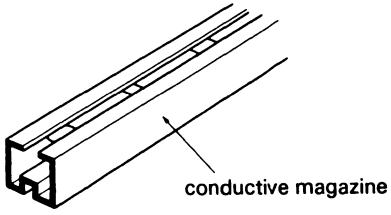
Transporting, storing and packaging methods

1) Magazine

Use the metal, or antistatic-treated plastic IC magazines.

The plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.

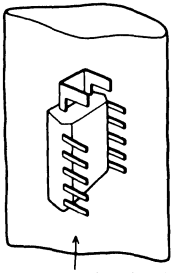
magazine



2) Bag

Use a conductive bag for keeping ICs. If use of a vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.

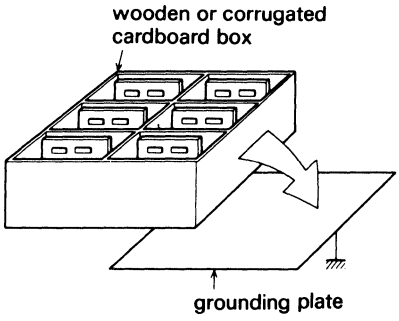
bag



3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



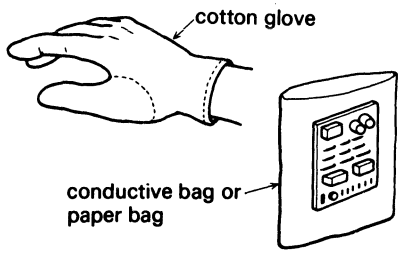
4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron whose insulation resistance after five minutes from energizing is greater than 10 MΩ (DC 500V).

2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

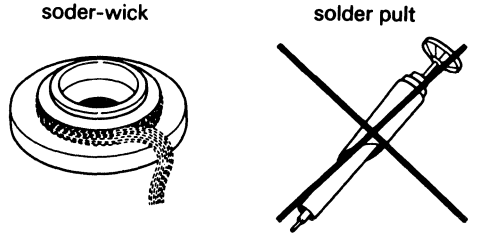
4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Soder-wick or equivalent.

solder remover



6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

C) Mounting method

Soldering and solderability

(1) Solderability guaranteed by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

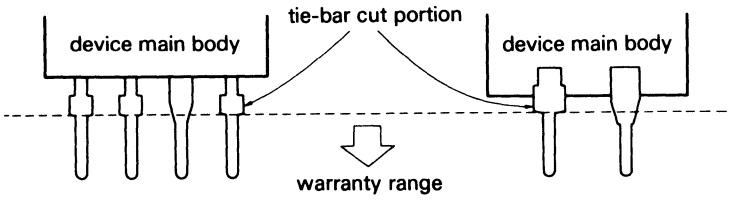
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which has been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{-0}$ seconds in a solder bath of 350°C ±10°C, for a distance of up to 1 to 1.5 mm from the main body.

The temperature of 260°C ±5°C assumes the soldering with solder flow system, and the temperature 350°C ±10°C assumes soldering by soldering iron.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited for 10 seconds at 260°C ±5°C. The distance between the device main body and solder bath is assumed as 1.6 mm.

5. Quality Assurance and Reliability

Sony's Policy of Quality Assurance

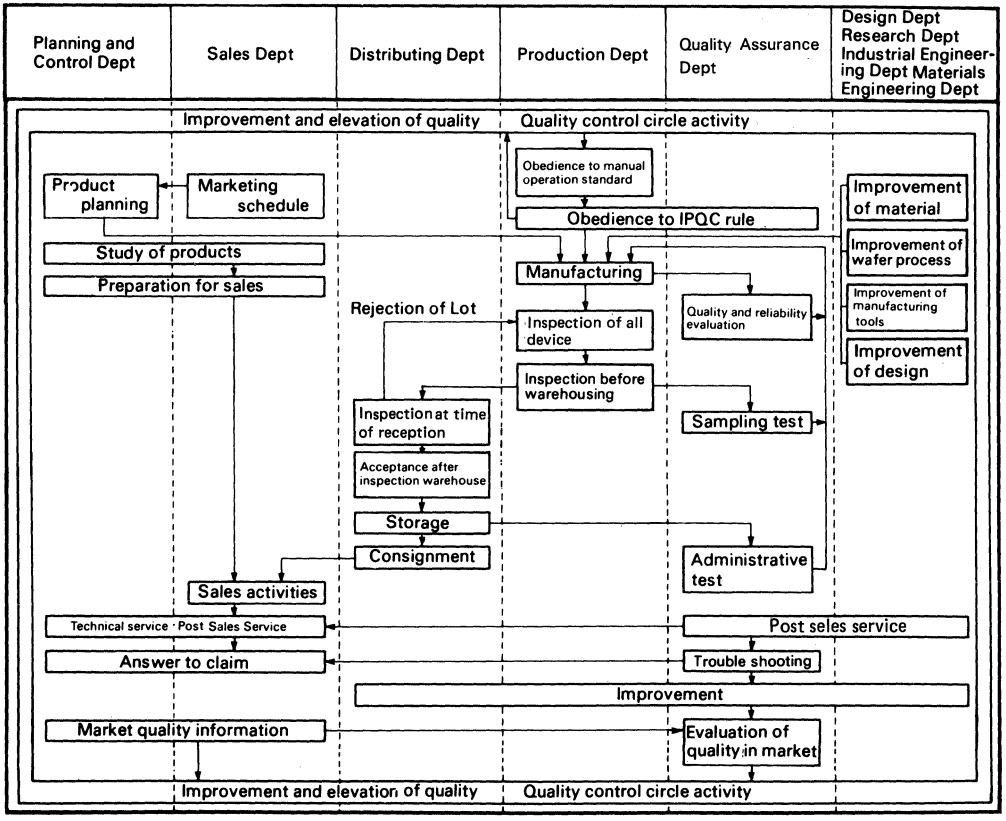
The Sony semiconductor embodies two fundamental ideas: "highest quality" and "lowest cost". There are the two key points for realizing these ideas.

One is the "quality" of men fabricating the semiconductor devices. The reliability of these people is reflected in the Sony products. Accordingly, Sony is making a continuous effort to raise the "quality" of people capable of manufacturing and fabricating Sony semiconductor devices.

The other point is a source management system combined with the concept of thorough quality design. With this system, higher quality products can be steadily manufactured through automation of device design, process design, and the fabrication process.

Sony is making constant efforts to supply the most economical and most useful products of very high quality for users.

Quality assurance system of semiconductor products



Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "total-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodical reliability test

Item		Test Hour	LTPD (%)
Electrical characteristic test		In order to know the quality level, some types are selected and tested again.	
LIFE TEST	High temperature operation	Up to 1000 hr	10%
	High temperature storage	Up to 1000 hr	10%
	Low temperature storage	Up to 1000 hr	10%
	High temperature and high humidity storage	Up to 1000 hr	10%
	High humidity bias test	Up to 1000 hr	10%
	High temperature and high humidity with bias	Up to 500 hr	10%
	Pressure cooker	Up to 200 hr	10%
ENVIRONMENT TEST	Soldering heat resistance heat cycle	10 s	15%
	Heat cycle	10 cycle	15%
MECHANICAL TEST	Solderability	Japan Industrial Standard (JIS)	15%
	Lead strength		15%
OTHER TESTS	if necessary test, are selected accordingly to JIS C7021, C7022, EIAJ SD121, IC121.		

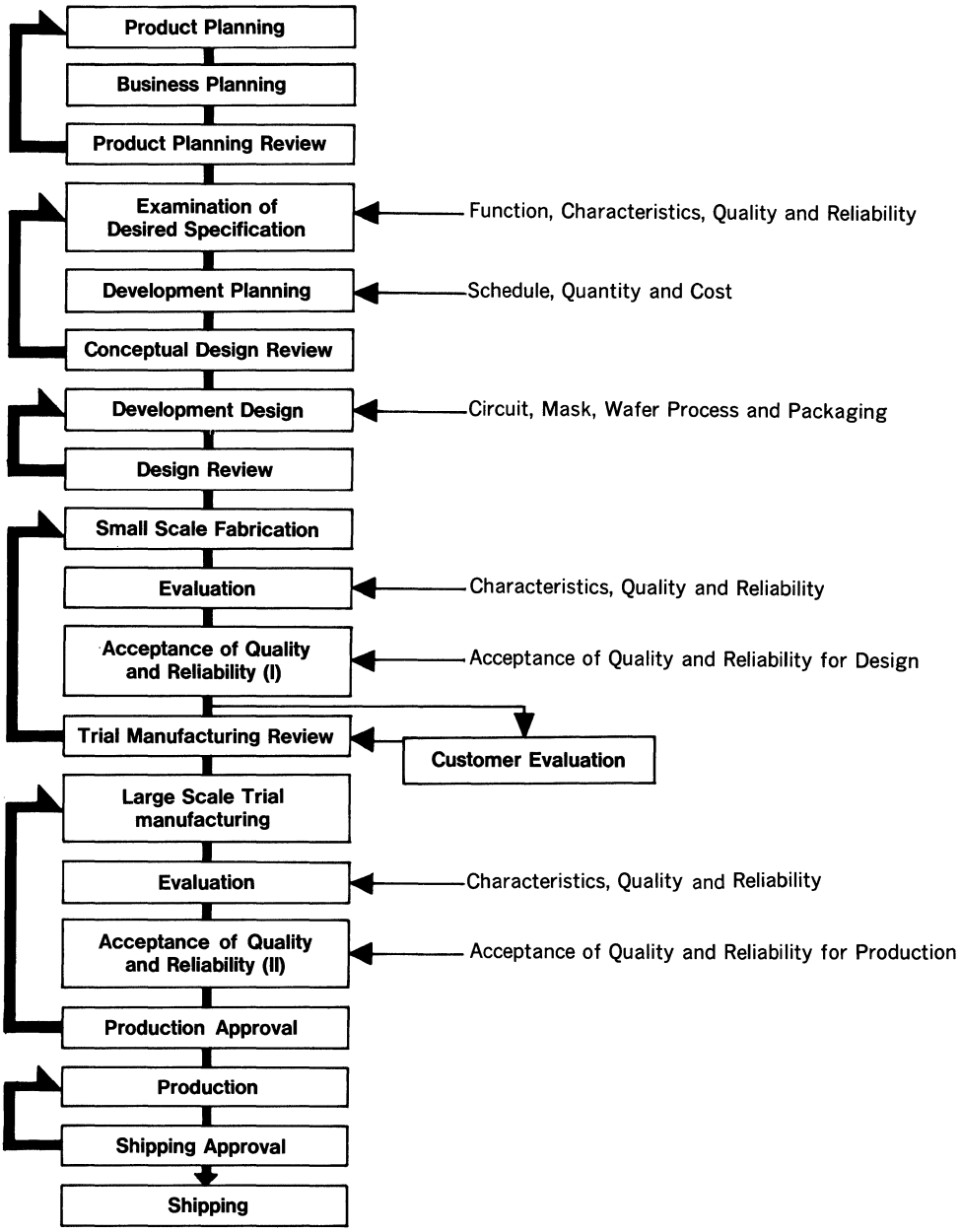
• These tests are selected by sampling standard.

These tests and Inspection data are useful not only to estimate quality in the market place but also as data to improve design and wafer processes.

Reliability test standard for acceptance of products

Type of Test	Condition	Supply voltage	Testing time	LTPD(%)
High temperature operation	Ta=125°C, 150°C	TYP	1000 hr	5%
High temperature with bias	Ta=125°C, 150°C	TYP	1000 hr	5%
High temperature storage	Ta=150°C		1000 hr	5%
Low temperature storage	Ta=−65°C		1000 hr	5%
High temperature and humidity storage	Ta=85°C, 85%RH		1000 hr	5%
High temperature and High humidity with bias	Ta=85°C, 85%RH	TYP (1 hr on/3 hr off)	500hr	5%
Pressure cooker	Ta=121°C, 100%RH, 30 pounds per square inch		1000 hr	5%
Temperature cycle	Ta=−65°C to +150°C		100 C	10%
Heat shock	Ta=0°C to +100°C		5 C	10%
Soldering heat resistance	Tsolder = 260°C		10 S	105
Solderability	Tsolder =230°C (Rosin type flux)		5 S	10%
Mechanical shock	X, Y, Z 1500G 0.5 ms half sine wave		3 times for each direction	10%
Vibration	X, Y, Z 20G 10 to 2000 to 10 Hz (4 min) sine wave vibration		16 minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000 G centrifugal acceleration		1 minute for each direction	10%
Fall by gravity	Falling from the height of 75cm to maple plate by gravity		3 times	10%
Lead strength (Bend) (Pull)	Based on JIS			10%
Electrostatics strength	Device must be designed again, when electrostatic strength is below standard supplying surge voltage To each pin under the conditions of C=200PF and Rs=0Ω.			

From development to production



A/D,D/A Converters Audio

1) A/D, D/A Converters — Audio —

Type	Function	Page
CX20017	Dual 16bit 44kHz Multiplexed D/A Converter	23
CX20018	Dual 16bit 44kHz Multiplexed A/D Converter	37
CX20133	16bit D/A Converter	56
CX20152	Dual 16bit 88kHz Multiplexed D/A	69
CX23010 CX23060	Dual 10bit 50kHz Multiplexed A/D + D/A	87

Dual 16 bit 44 kHz Multiplexed D/A Converter

Description

The CX20017 is a 16 bit D/A converter IC for PCM audio using an integration system. Analog signals can be regenerated from 16 bit digital signals by adding an integrator, an analog switch, and a low-pass filter outside the IC.

Features

- 16 bit D/A converter.
- Clock buffer.
- TTL-ECL interface circuit.
- Discharge drive circuit.
- Analog switch drive circuit.

Functions

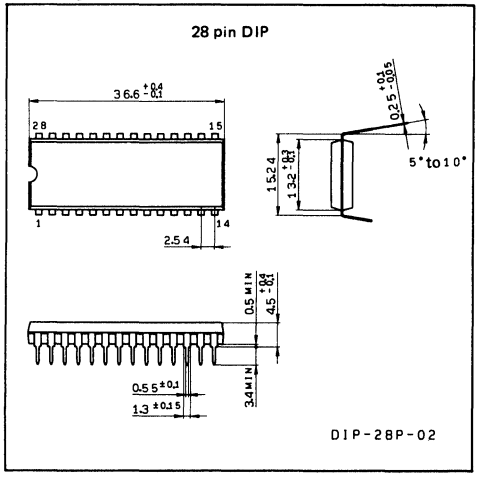
- Two channels for integral current output and discharge signal output.
- Level shift circuit for direct interface with TTLs and MOS LSIs.
- Analog switch drive circuits, etc.

Structure

Silicon Monolithic IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	Topr	−10 to +75	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation	P_D	2.1	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V
	V_{EE}	−5 ± 0.25	V

Block Diagram

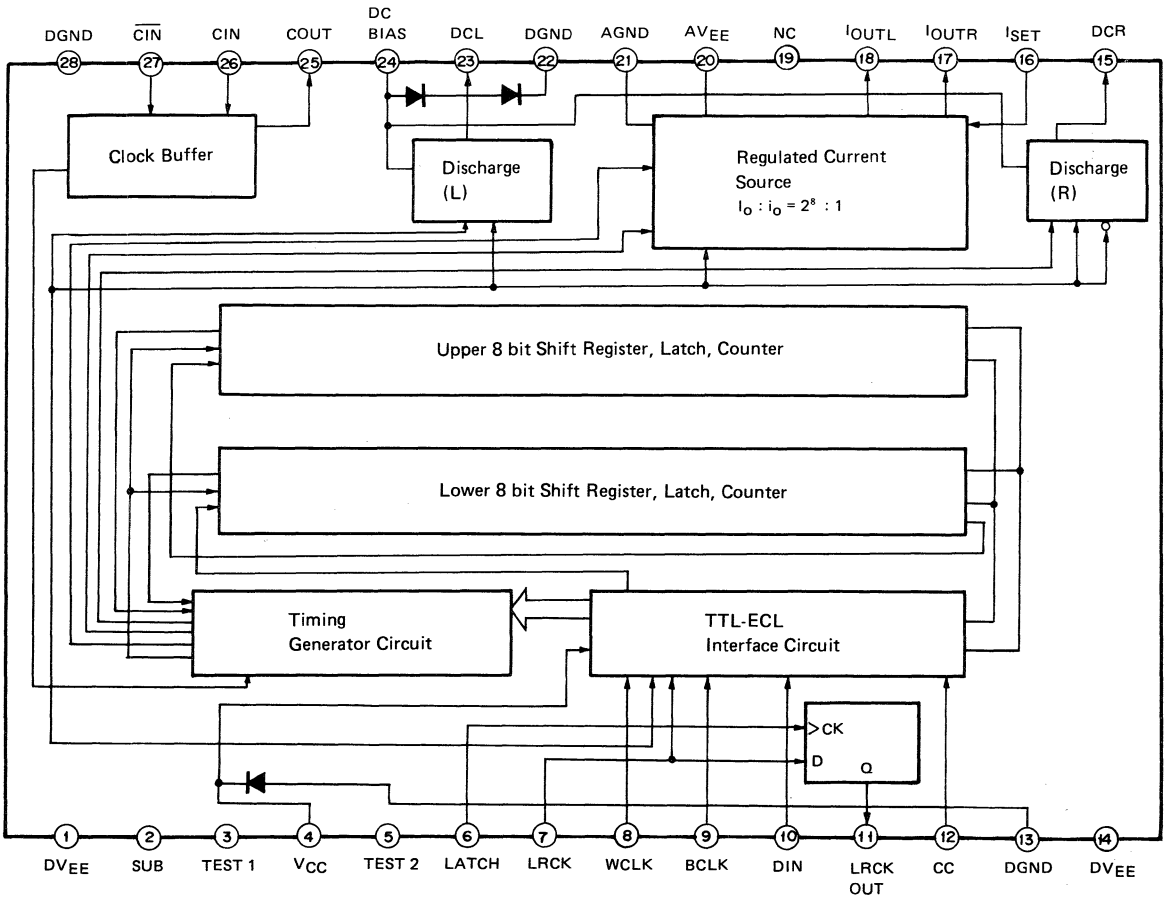


Fig. 1

TEST 1 and TEST 2 are to be used open.

Pin Description

No.	Symbol	Description
1	DV_{EE}	Digital system power supply pin Apply −5V
2	SUB	Board of IC. It is used always being connected to pin 1
3	TEST 1	Test pin. It is used normally in the open state.
4	V_{CC}	Digital system power supply pin Apply +5V
5	TEST 2	Test pin. It is used normally in the open state.
6	LATCH	Clock pin of D type latch
7	LRCK	LRCK input pin
8	WCLK	WCLK input pin
9	BCLK	BCLK input pin
10	DIN	DIN (Data input pin)
11	LRCK OUT	LRCK output pin
12	CC	CC input pin
13	DGND	Digital system GND pin
14	DV_{EE}	Digital system power supply pin Apply −5V
15	DCR	Right channel discharge drive signal output pin
16	I_{SET}	Integral current setting pin
17	I_{OUTR}	Right channel current output pin
18	I_{OUTL}	Left channel current output pin
19	NC	No connection
20	AV_{EE}	Analog system power supply pin
21	AGND	Analog system GND pin
22	DGND	Digital system GND pin
23	DCL	Left channel discharge drive signal output pin
24	DCBIAS	Discharge circuit bias pin
25	COUT	Clock oscillator output pin
26	CIN	Clock oscillator positive input pin
27	$\overline{CIN}$	Clock oscillator negative input pin
28	DGND	Digital system GND pin

Electrical Characteristics

(Ta = 25°C, V_{EE} = −5.0V, V_{CC} = 5.0V)

Item	Symbol	Pin and test condition	Min.	Typ.	Max.	Unit	Note
Circuit Current	I_{EE}	1, 2, 14, 20	−112	−85		mA	1
Circuit Current	I_{CC}	4		9.5	12.5	mA	1
Input Threshold Voltage 1	V_{TH1}	6, 7, 8, 9, 10, 12		−2.9		V	2
Input Threshold Voltage 2	V_{TH2}	6, 7, 8, 9, 10, 12		2.1		V	3
High Level Input Voltage 1	V_{IH1}	6, 7, 8, 9, 10, 12	−2.2			V	2
High Level Input Voltage 2	V_{IH2}	6, 7, 8, 9, 10, 12	2.8			V	3
Low Level Input Voltage 1	V_{IL1}	6, 7, 8, 9, 10, 12			−4.2	V	2
Low Level Input Voltage 2	V_{IL2}	6, 7, 8, 9, 10, 12			0.8	V	3
High Level Input Current 1	I_{IH1}	6, 7, 8, 9, 10, 12 V_{IH} = −0.5V			500	μA	2
High Level Input Current 2	I_{IH2}	6, 7, 8, 9, 10, 12 V_{IH} = 4.5V			500	μA	3
Low Level Input Current 1	I_{IL1}	6, 7, 8, 9, 10, 12 V_{IL} = −0.5V			−15	μA	2
Low Level Input Current 2	I_{IL2}	6, 7, 8, 9, 10, 12 V_{IL} = 0V			500	μA	3
High Level Output Voltage	V_{LRCKH}	11 I_{OH} = −100μA after making Pin7 to be 4.5V. Supply a 0V-5V-0V clock to pin 6	2.7			V	
Low Level Output Voltage	V_{LRCKL}	11 I_{OL} = 100μA after setting Pin 7 0V. Supply a 0V-5V-0V to pin 6.			−2.7	V	
Clock Input Bias Voltage	V_{CIN}	26, 27		−1.3		V	
Clock High Level Output Voltage	V_{CCR}	25		−0.8		V	
Clock Low Level Output Voltage	V_{COL}	25		−1.6		V	
Current Output Pin Leak	I_{OLEAK}	17, 18 Pins17 and 18 voltage 0V. When current output is off.			1.5	μA	

Item	Symbol	Pin and test condition	Min.	Typ.	Max.	Unit	Note
I_{OUT} Output Current	I_{OUT}	17, 18 Pins17 and 18 voltage 0V. Pin 16 I_{SET} = 500 μA, ($I_{OUT} = I_o + i_o$)		2.008		mA	
Current Ratio *2	I_o/i_o	17, 18 Pin16 I_{SET} = 250 μA	255.0	256.0	257.5	—	4
Discharge Circuit Current Consumption	I_{DC}	24 Set Pin24 0V	1.35	1.9	2.5	mA	
Discharge Circuit High Level Output Voltage	V_{DCH}	15, 23 Pin24 voltage = 1.4V. Load current = −100 μA	0.27	0.45	0.77	V	
Discharge Circuit Low Level Output Voltage	V_{DCL}	15, 23 Pin24 voltage = 1.4V. Load current = −100 μA		−4.2	−3.5	V	
Maximum I_{SET} Current	$I_{SET\ MAX}$	16 Range in which current ratio of $I_{OUTL\ (R)}$ meets $255 < I_o/i_o < 257$			520	μA	
Distortion Factor	THD	During 0 dB (full scale) playback for both right and left		0.003	0.005	%	5
		During −20 dB playback for both right and left		0.02	0.025	%	5
Operating Clock Frequency	f_{CLK}	Self-excitation/separate excitation			40	MHz	

Note) 1. Pins13, 17, 18, 21, 22, 24 and 28 are for grounding, pin16 is connected through 5.1 kΩ to ground. Other pins are open.
2. When Pin 4 (V_{CC}) is opened.
3. When Pin 4 (V_{CC}) is made to be 5.0V.
4. Measurement circuit See Fig. 2
Conversion frequency 44.1 kHz.
Input data 16 bit data generated by ROM SG., Full scale data (0 dB) and data of a level −20 dB below it are used.
Distortion meter HP339A (all filters are turned on) or its equivalent that has an 80 kHz LPF, 30 kHz LPF and 400 Hz HPF.

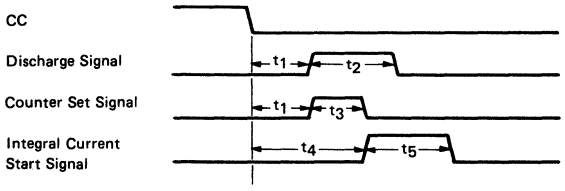
*1 Recommended operating voltage

*2 In the current ratio measurement circuit (Fig. 3):
$-3.9\ (mV) < 1\ (k\Omega) \times I_o\ (\mu A) - 256\ (k\Omega) \times io\ (\mu A) < 5.9\ (mV)$

Description of CX20017 Conversion Process

(1) Data Call In (BCLK, DIN, WCLK, LRCK.) See Fig. 5.
Data is 16 bit serial signals and is of a 2's complement type (2's complement). Data is synchronized with a rising edge of the bit clock (BCLK) from MSB and is sent to the IC sequentially. (Data variations occur with the fall of BCLK.)
Changing the word clock (WCLK) from a high to a low level during the 17th fall of the BCLK, 16 bit data is transferred from the shift register to the latch. Data from the other channel is sent in to the system at the 17th BCLK when CX20017 is used in the stereo mode.
When allocating data in the stereo mode, Rch data is called in while the level of LRCK is low, calling in Lch data while the level of LRCK is high. I_{OUTL} and DCL operate only when the level of LRCK is low, and I_{OUTR} and DCR, operate only when the level of LRCK is high.

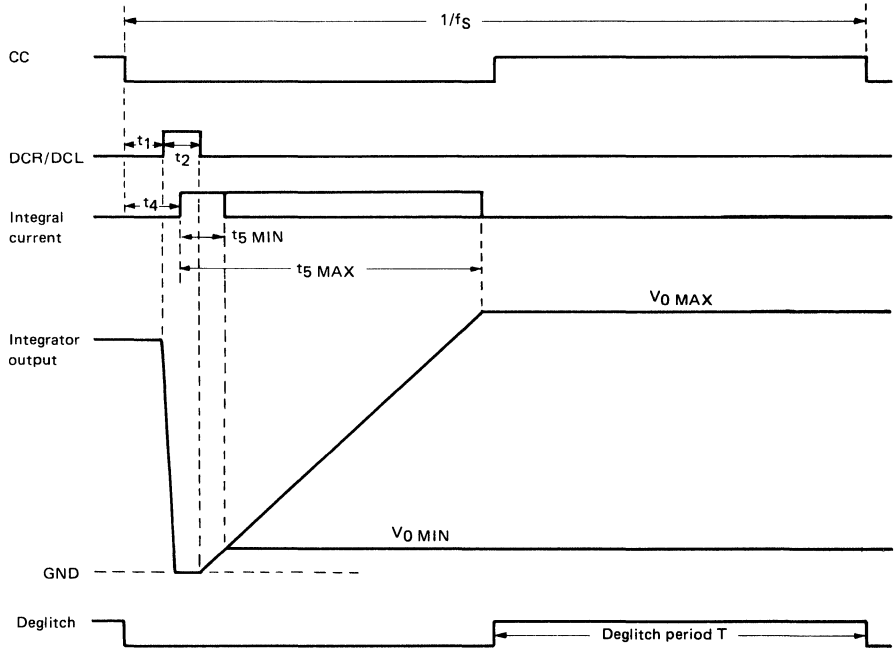
(2) Conversion Process (CC, LRCK, CIN, I_{OUTL}, I_{OUTR}, DCL, and DCR)
All the timing circuits inside are reset, by inputting more than three clocks from the clock input (CIN) after setting the level of the conversion command (CC) to high.
After resetting, the level of CC is set to low, and a clock is supplied into CIN, to start the functioning of the internal timing circuit. It produces three signals: a discharge, a counter set, and an integral current start signals. Depending on periods of clocks and the number of clocks the timings of these three signals are determined as follows:



$t_1 = 34 \times \tau o$
$t_2 = 67 \times \tau o$
$t_3 = 31 \times \tau o$
$t_4 = 65 \times \tau o$
t_5 min $= 47 \times \tau o$ (When input data is 01 . . . 1)
t_5 max $= 302 \times \tau o$ (When input data is 10 . . . 0)

The counter set signal sets data entered in the latch to the counter, and is not output outside. The discharge signal is output from DCL and DCR and is controlled by LRCK. The signal is output from DCL when the level of LRCK is low, and from DCR when the level is high.
The upper current I_o and lower current i_o flow on the instruction of the integral current start signal. The counter starts counting the value preset simultaneously with the turning off the discharge signal. The counter counts eleven offsets and then sends a signal to stop the integral current. The value of t_5 is changed by the input data value preset in the counter and is changed over the range 0 to 255. For this reason, a maximum ($t_4 + t_5$ max) is needed for the conversion time, i.e., the time period between the level of CC becoming low and the completion of integration.
As is the case with the discharge signal, the integral current outputs I_{OUTL} when the level of LRCK is low, outputting I_{OUTR} when the level is high.

Regarding the relationship between sampling frequency fs and clock.



By denoting the clock frequency f_{CLK} cycle as τ_o, the maximum value V_{OMAX} and minimum value V_{OMIN} of the integral voltage output can be given as the following equations.

$$V_{OMAX}=\frac{I_o}{C}*\tau_o*267+\frac{i_o}{C}*\tau_o*266\ (t_4+t_{5\ MAX})$$

$$V_{OMIN}=\frac{I_o}{C}*\tau_o*12+\frac{i_o}{C}*\tau_o*11\ (t_4+t_{5\ MIN})$$

This integral voltage is held to the capacitor C of the integrator when the current switch is turned off. This voltage is utilized as the D/A conversion output in the deglitch period T. This T is determined by the settling time of the deglitch circuit.
If setting of the conversion time and deglitch period are equal, the relationship between the conversion synchronization f_s and the clock frequency f_{CLK} can be given as follows:

$$f_s=\frac{f_{CLK}}{2\times(t_4+t_{5MAX})}=\frac{f_{CLK}}{734}$$

Assuming that f_s=44.1 kHz, f_{CLK} becomes 32.4 MHz.
However, when it is used in practice, it is sufficient to consider that $f_s=f_{CLK}/\{(t_4+t_{5\ MAX}+1.0\mu s)+T\}$, since approximately 0.5 to 1.0 μs will become necessary to the settling of the integrator after the current of t_5 is being switched off.
Where, i_o is the integrated current which is corresponding to 1 LSB, and I_o is that of corresponding to 2^8LSB.

(3) Setting Integral Current (I_{SET}, I_{OUTL}, I_{OUTR})

The integral current is determined by the value of a regulated current flowing from I_{SET} pin. Its relationship can be expressed as follows:

$$I_{OUTL}\ (R) = I_o + i_o$$
$$= (4 + \frac{1}{64})\ I_{SET}$$

Assuming that D_0; MSB, D_{15}; LSB, the integrator output voltage V_o can be given as the following equations.

$$V_o = \frac{I_o}{C}(\overline{D}_0 * 2^7 + \overline{D}_1 * 2^6 + \ldots + \overline{D}_7 * 2^0 + 12)\ \tau_o$$
$$+ \frac{i_o}{C}(\overline{D}_8 * 2^7 + \overline{D}_9 * 2^6 + \ldots + \overline{D}_{15} * 2^0 + 11)\ \tau_o$$

Assuming that I_{SET}=500 μA, τ_o=1/35(MHz)=28.6(ns), and C=2000 pF, the output voltage of the integrator becomes maximum when the input data is "10 to 0", and that value V_{OMAX} becomes as follows:

$$I_o = 4 * I_{SET}$$
$$\text{As } i_o = \frac{1}{64} * I_{SET}$$

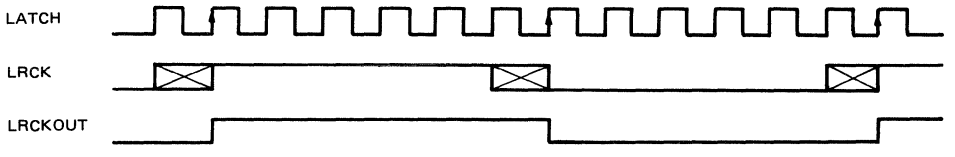
$$V_{OMAX} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} * 267 * 28.6 \times 10^9$$
$$+ \frac{500 * 10^{-6}/64}{2000 \times 10^{-12}} * 266 * 28.6 \times 10^9$$
$$= 7.67(V)$$

(4) Function of LRCK OUT (LATCH, LRCK, LRCK OUT)

The LRCK OUT output drives the analog switch IC (MC 14053B or its equivalent) to cut the output converted by CX20017 and the integrator as a PAM wave.

Jitter in a PAM wave causes conversion errors, and a D-type flip flop is contained to absorb this jitter. The LATCH input is used as a clock to drive the flip flop. The D-type flip flop changes the output condition in synchronization with the rise of the clock.

This LRCK OUT functions only when +5V is applied to V_{CC}. The output voltage level is −3 to +3V and can efficiently drive the CMOS analog switch.



LATCH, LRCK, and LRCKOUT Timing

(5) Clock Input/Output Pin (COUT, CIN $\overline{\text{CIN}}$)

The clock buffer has a configuration similar to that of an ECL logic circuit, and its input pin is biased by an internal bias circuit. (≈ -1.3V) output amplitude level is 0.8V.

(6) Bias Pin (DV_{EE}, SUB, DGND, V_{CC}, AV_{EE}, AGND, and DC BIAS)

SUB is the IC substrate and can be used by making its potential common to DV_{EE}. The standard values of DV_{EE} and AV_{EE} are -5.0V.

The CX20017 can be operated regardless of whether the digital input pin is in the ranges 0 to -5V, or 0 to $+5$V. When operating with an input voltage between 0 and $+5$V, raise the level of the V_{CC} pin to $+5$V. As mentioned before, LRCKOUT is output in this case.

Open the V_{CC} pin when using an input voltage between 0 and -5V. The DC BIAS is the bias circuit for the output circuit of the discharge signal. A current of approximately 2.5 mA is required for the standard value. Supply a current higher than (2.5 mA + α) from a $+5$V and higher power source.

The potential of this pin is biased to $2V_f$.

The value of α is determined as follows. In order to maintain this pin voltage of $2V_f$ (≈ 1.4V), approximately 0.5 mA is required. In addition, the maximum current flowing to load resistance R_L which is connected to DCR (pin 15) and DCL (pin 23) can be obtained by the following:

$$\frac{1}{R_L} \times (V_{DCH} + |DV_{EE}|) \times 2$$

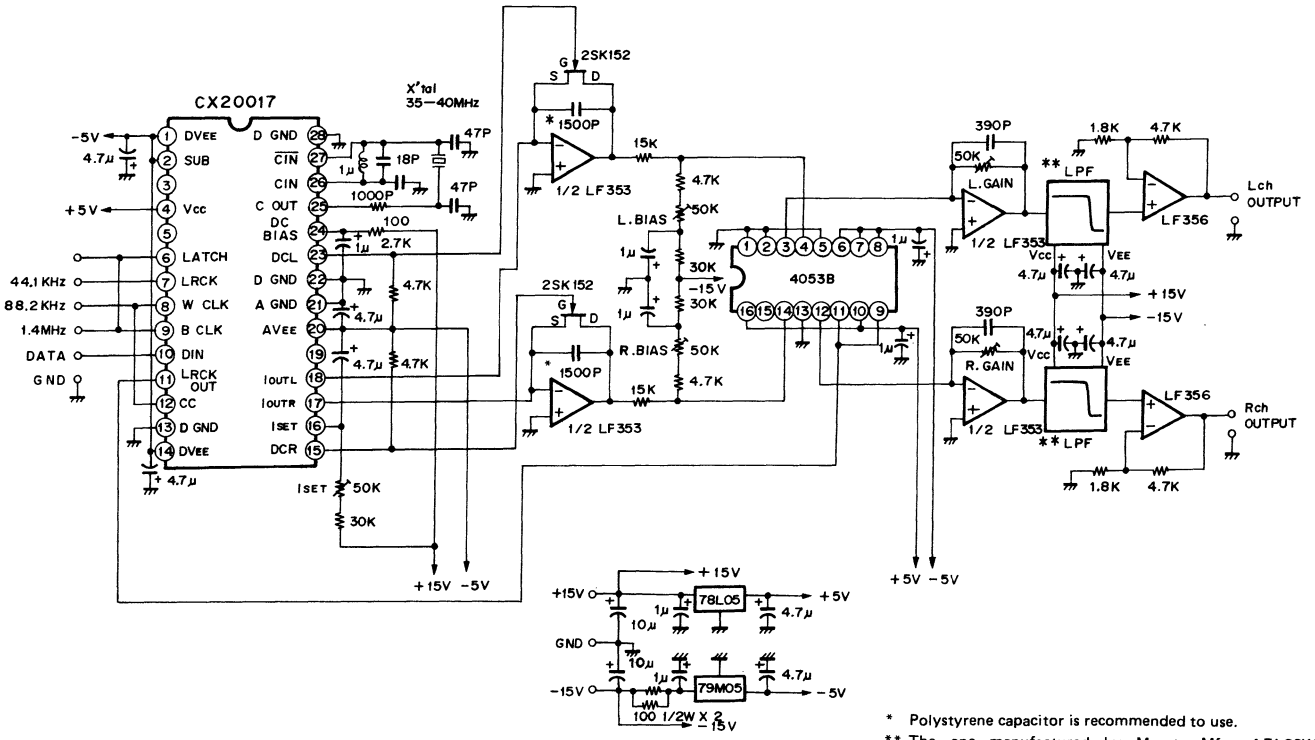
when $R_L = 4.7$ kΩ, $V_{DCH} = 0.4$V and $DV_{EE} = -5$V,

$\alpha = 0.5 + 1.32 = 1.82$ (mA)

and the total becomes 4.32 mA.

As the recommended value, it is 5 mA at $R_L = 4.7$ kΩ.

Peripheral Circuit



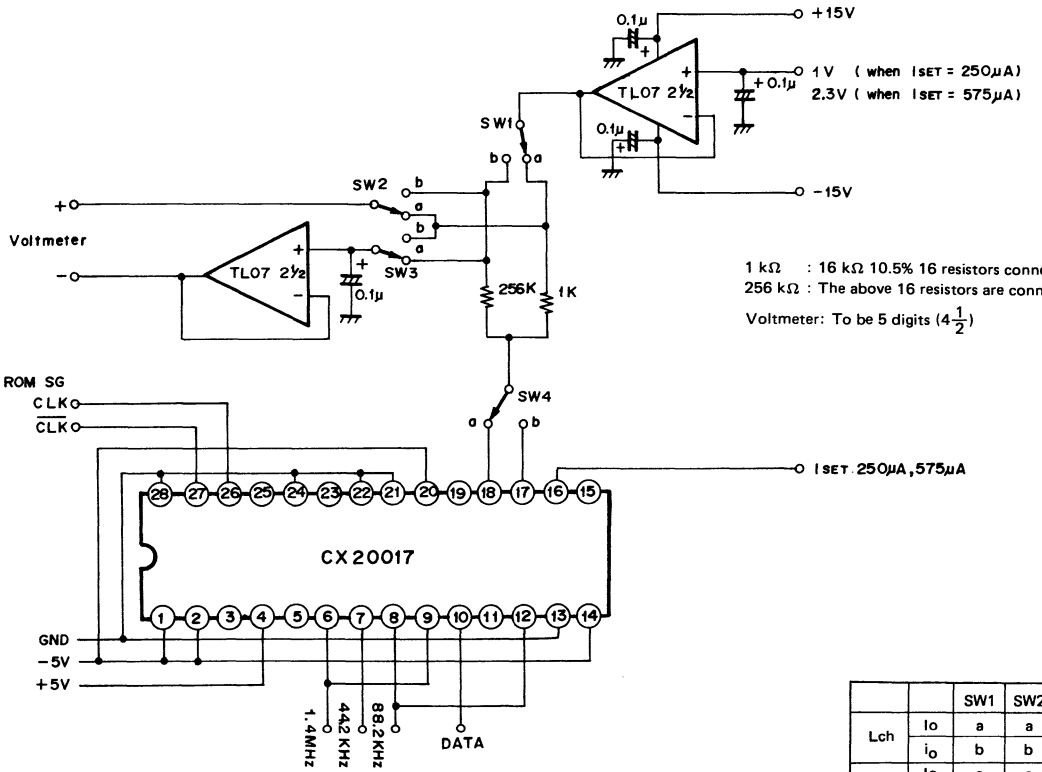
* Polystyrene capacitor is recommended to use.

** The one manufactured by Murata Mfg., AFL89WB 20000C3

The evaluation boards applying the above circuit are prepared.

Fig. 2

Current Ratio Measureing Circuit



		SW1	SW2	SW3	SW4
Lch	Io	a	a	a	a
	i_o	b	b	b	b
Rch	Io	a	a	a	a
	i_o	b	b	b	b

Fig. 3

SONY

A circuit example by which deglitcher is carried out with sample/hold type

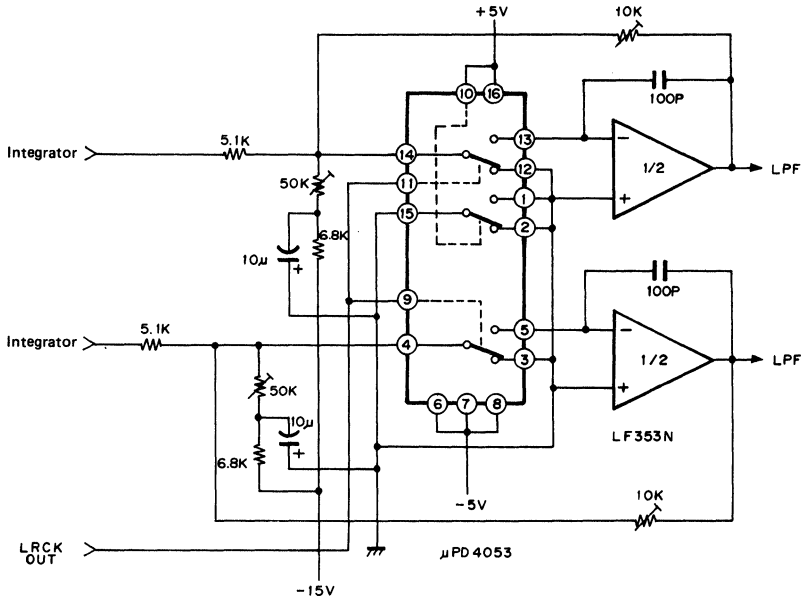


Fig. 4

Timing Chart During Stereo Mode

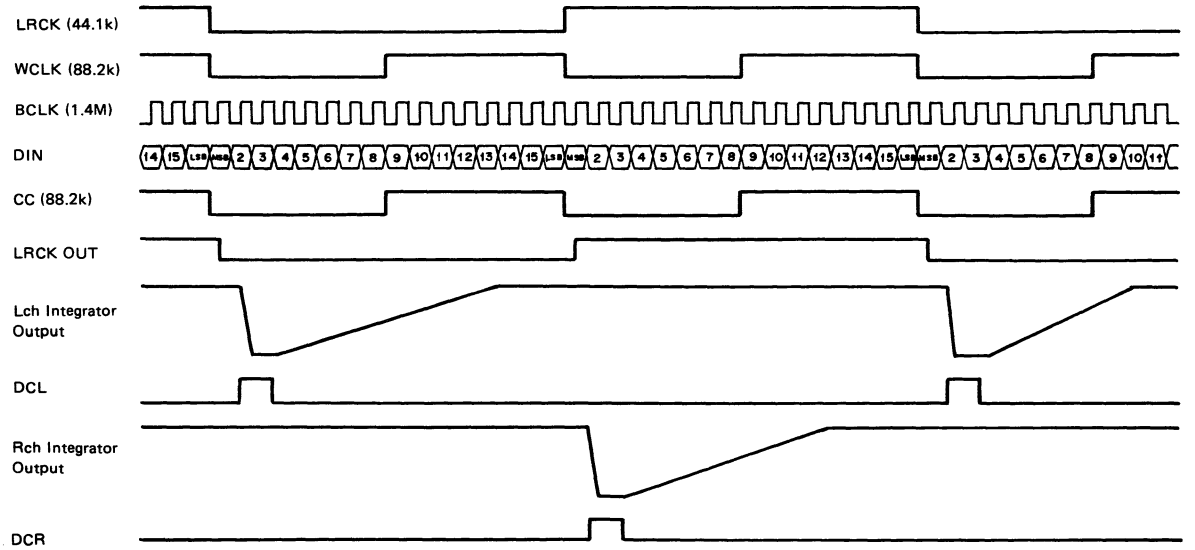
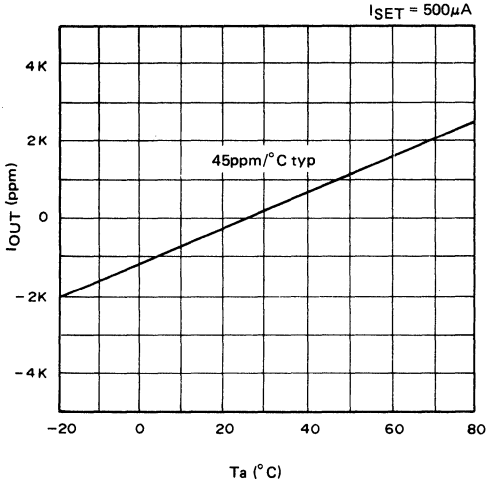
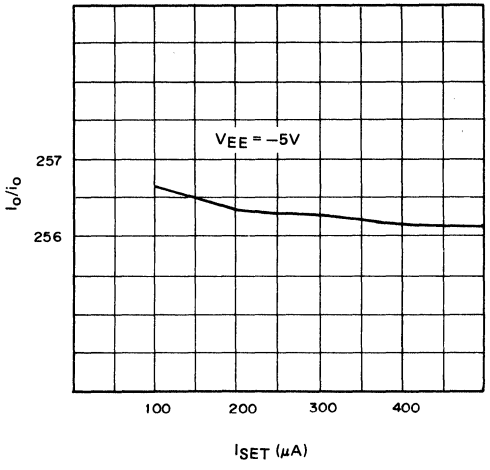


Fig. 5

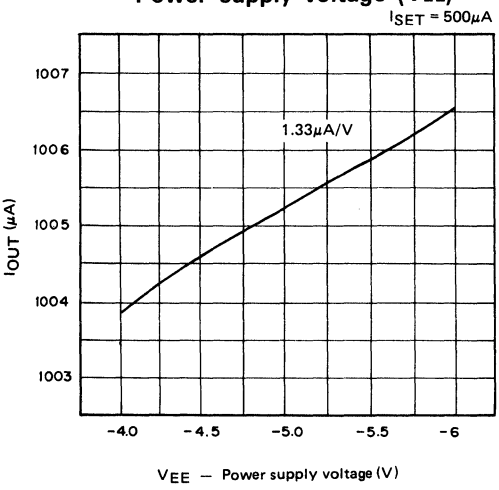
IOUT temperature characteristics (Io+io)



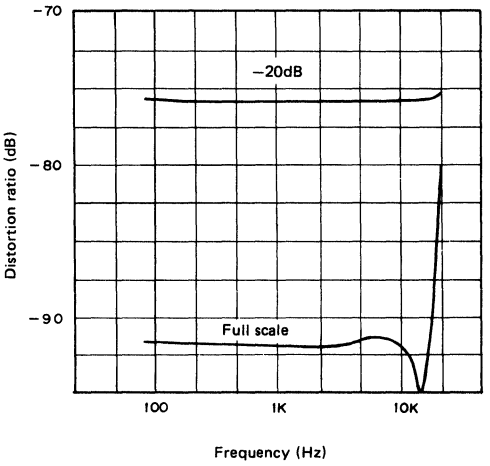
Io/io vs. ISET



Output current vs. Power supply voltage (VEE)



Distortion ratio (dB)



Dual 16 bit 44 kHz Multiplexed A/D Converter

Description

The CX20018 is a monolithic bipolar IC designed for PCM (Pulse Code Modulation) audio. This IC consists of 16 bit counters, shift registers, clock buffer, clocked synchronous comparator, stabilized current source and TTL compatible interface circuits, etc.

Features

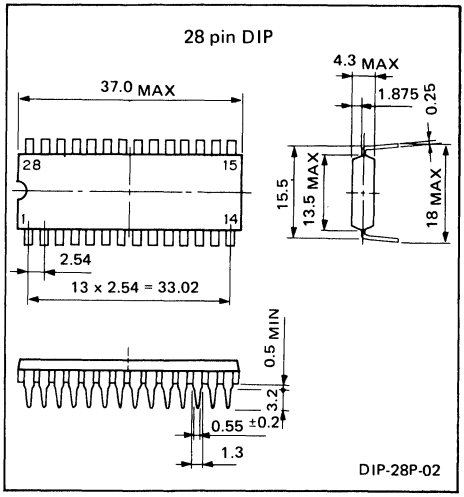
- Line monotonicity
- Low noise
- TTL compatible input/output
- Stereo or monaural modes can be selected by external control

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



Absolute Maximum Ratings

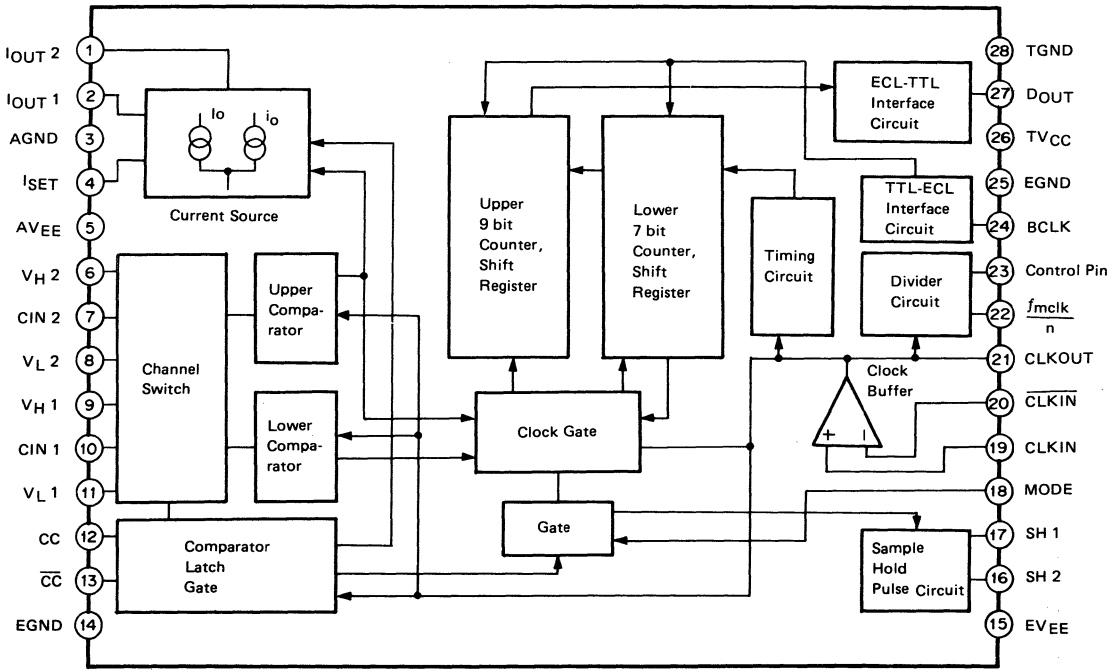
• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	Topr	−20 to +75	°C
• Strange temperature	Tstg	−50 to +150	°C
• Allowable power dissipation	P_D	1.7	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.25 to −4.75	V

*Note: Refer to page 311 (CX20018PCB) as the application note.

Block Diagram



Electrical Characteristics

(Ta=25°C, V_{EE}=−5V, V_{CC}=5V)

Item	Symbol	Pin No. and Test Conditions	Min.	Typ.	Max.	Unit	Note
Supply Voltage Range *1	V_{EE}		−4.75	−5.00	−5.25	V	1
Supply Voltage Range *1	V_{CC}		4.75	5.00	5.25	V	1
Circuit Current	I_{EE}		70.0	102.0	130.0	mA	1
Circuit Current	I_{CC}		4.0	10.0	15.0	mA	1
Current Output Pin Leak	I_{OLEAK}	1, 2 (Pins 1, 2 Voltage=0V when current output is off)			1.0	μA	2
Iout Output Current	I_{out}	1, 2 (Pins 1, 2 Voltage=0V. Iset=410 μA)		1.64		mA	2
Current Ratio *2	I_o/i_o	1, 2 (I_{set}=410 μA)	127.0	128.0	129.0		2
Maximum ISET Current	I_{SET} Max.	4 $127.0 \leqq \frac{I_o}{i_o} \leqq 129.0$			750	μA	2
Sample Hold Pulse High Level Output Voltage	V_{SH1H} V_{SH2H}	16, 17	−0.05	0	0.1	V	
Sample Hold Pulse Low Level Output Voltage	V_{SH1L} V_{SH2L}	16, 17	−4.40	−4.25	−3.50	V	
Clock Input Bias Voltage	V_{CLKIN} $\overline{V_{CLKIN}}$	19, 20	−1.90	−1.72	−1.50	V	
Clock Output Low Level Output Current	$I_{CLKOUTL}$	21		3.0	4.0	mA	
CC, $\widetilde{CC}$ Input Bias Voltage	V_{CCIN} $\overline{V_{CCIN}}$	12, 13	−2.20	−1.92	−1.60	V	
Data Output High Level Output Voltage	V_{DOUTH}	27 I_{OH}=0.1 mA	3.2			V	
Data Output Low Level Output Voltage	V_{DOUTL}	27 I_{OL}=−0.4 mA			0.4	V	
Bit Clock High Level Input Voltage	V_{BCLKH}	24	2.0			V	
Bit Clock Low Level Input Voltage	V_{BCLKL}	24			0.5	V	
Bit Clock High Level Input Current	I_{BCLKH}	24		4		μA	
Bit Clock Low Level Input Current	I_{BCLKL}	24	0.2	1		μA	
Distortion *3 Factor	THD	During 0 dB (full scale) playback for both channel		0.005	0.006	%	3
		During −20 dB playback for both channel			0.05	%	3

Item	Symbol	Pin No. and Test Conditions	Min.	Typ.	Max.	Unit
Maximum Operating Clock Frequency	f_{MCLK}	Self-excitation or separate excitation			100	MHz
Dividing Ratio Control Voltage	V_{CTL} (∞)	23	2.0		5.0	V
	V_{CTL} (2)	23	0.2		0.8	V
	V_{CTL} (4)	23	−0.8		−0.2	V
	V_{CTL} (8)	23	−5.0		−2.0	V
Mode Control Voltage	V_{MODE} (1)	18 Stereo, S/H ON	2.0		5.0	V
	V_{MODE} (2)	18 Stereo, S/H OFF	0.2		0.8	V
	V_{MODE} (3)	18 Monaural, S/H OFF	−0.8		−0.2	V
	V_{MODE} (4)	18 Monaural, S/H ON	−5.0		−2.0	V

Note) 1 Pins 1, 2, 3, 6, 7, 8, 9, 10, 11, 14, 21, 25 and 28 are for grounding, pins 18, 22, 23, are connected V_{CC}. Pin 4 draws 410 μA of current by external current source.

2 Reference to the current ratio test circuit.

3 Conversion Frequency 44.1 kHz

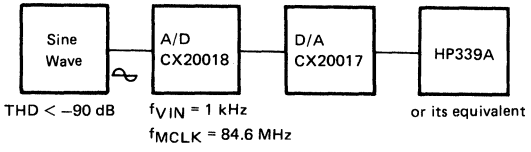
Distortion Meter HP339A (all Filters are turned on) or its equivalent that has an 80 kHz, LPF, 30 kHz LPF and 400 Hz HPF.

*1 Recommended operating voltage

*2 In the current ratio test circuit (See Fig. 1)

$$\left|15 \times 8\ (k\Omega) \times i_O\ (\mu A) - \frac{15}{16}\ (k\Omega) \times I_O\ (\mu A)\right| \quad < 12.0\ mV$$

*3 Measurement Method (See Note 3)



Current Ratio Test Circuit

Electrical Characteristics Test Circuit

Current Ratio Test Circuit

15 kΩ/16: 16 resistors are connected in parallel.
15 kΩ x 8: 8 resistors are connected in series. (resistor tolerance ± 0.5%)
Io: Pin 7 and 10 voltages are set at 0.5V.
i_O: Pin 7 and 10 voltages are set at −1.0V.

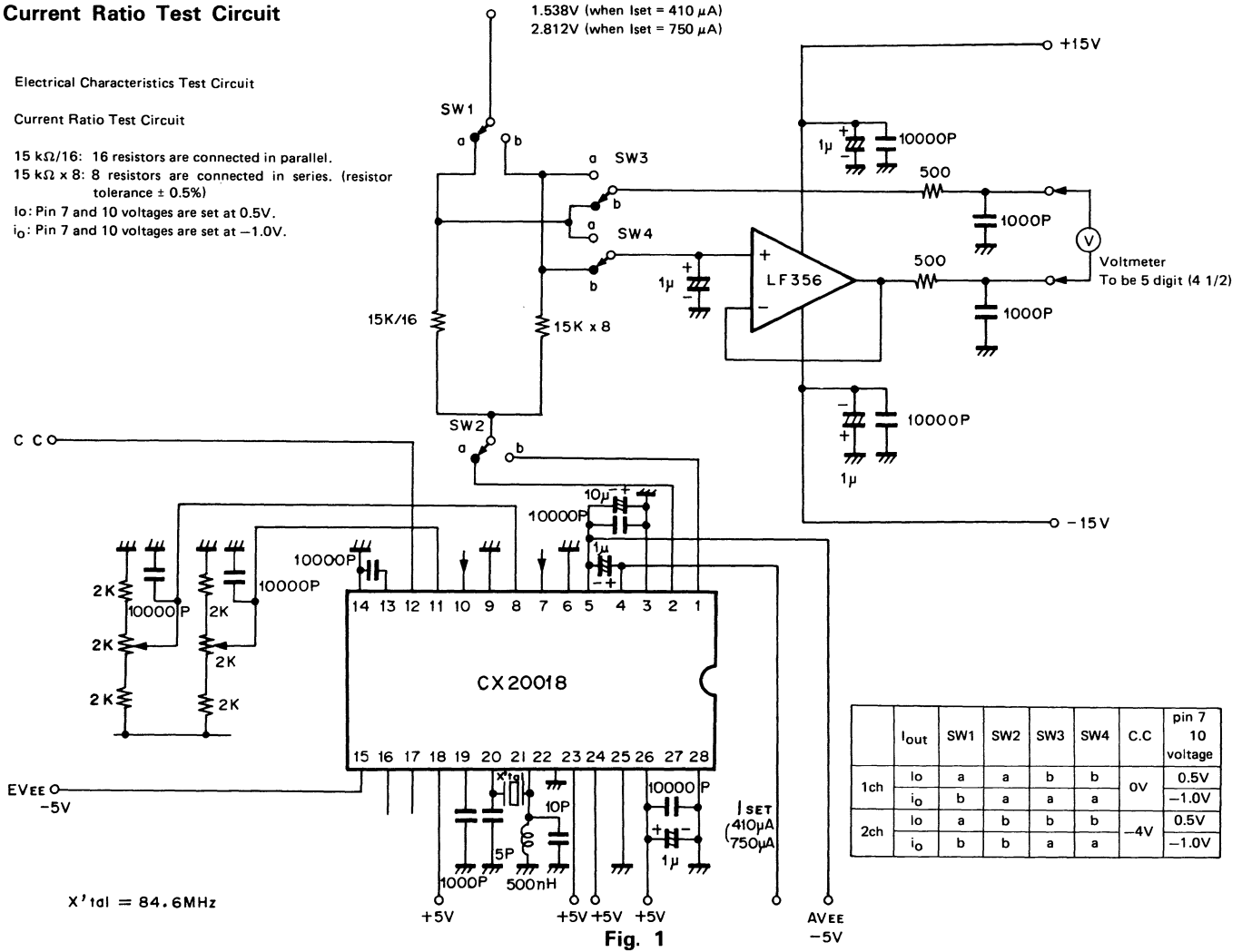


Fig. 1

	I_{out}	SW1	SW2	SW3	SW4	C.C	pin 7 10 voltage
1ch	Io	a	a	b	b	0V	0.5V
	i_O	b	a	a	a		−1.0V
2ch	Io	a	b	b	b	−4V	0.5V
	i_O	b	b	a	a		−1.0V

SONY®

Description of CX20018 Conversion Process

Conversion process

The timing circuit controls a conversion cycle and send "Data Transfer Pulse" to the 16 bit shift register for transmitting the last converted data. It is reset by both the edge of CC (Conversion Command), and the master clock pulse is fed to the timing circuit.

"Data Transfer Pulse" and "Mask Pulse" become "H" level as soon as the timing circuit starts to count clocks. "Data Transfer Pulse" becomes "L" when the timing circuit counts 11 clocks, and then the last data is transferred. Simultaneously, "Current Switch Pulse" becomes "H", and integral current starts to flow. "Counter Preset Pulse" becomes "H" when the timing circuit counts 16 clocks. And then, upper and lower level counters are reset. Counter Preset Pulse holds "H" level during the period of 8 clocks.

When the timing circuit counts 31 clocks, Mask Pulse becomes "L" and A/D conversion starts.

The coarse current "I_o" discharges the sampled charge of integrator until the output voltage of integrator crosses the reference voltage (VrefH). During this period the upper level counter counts the number of clock. After crossing the VrefH the fine current discharges the remaining charge of integrator. The lower level counter counts the number of clock unitl the output voltage of integrator crosses the lower level references voltage (VrefL). (See Figs. 2, 3, 4)

Data output

Data are 16 bit serial signals and 2's complement. The serial data are synchronous with a rising edge of Bit clock (BCLK), and only MSB data is synchronized with a edge of "Data Transfer Pulse". (See Fig. 3)

Monaural operation mode

In monaural mode the external integrator is tracking the input signal during CC is "H" state. At the moment when CC goes "L" state, the CX20018 starts conversion. The data is transferred to the output from MSB sequentially.

After 16 bit data are transferred, "Data Out" comes to the "H" level and keeps "H" level until next conversion. (See Fig. 4)

Timing Chart

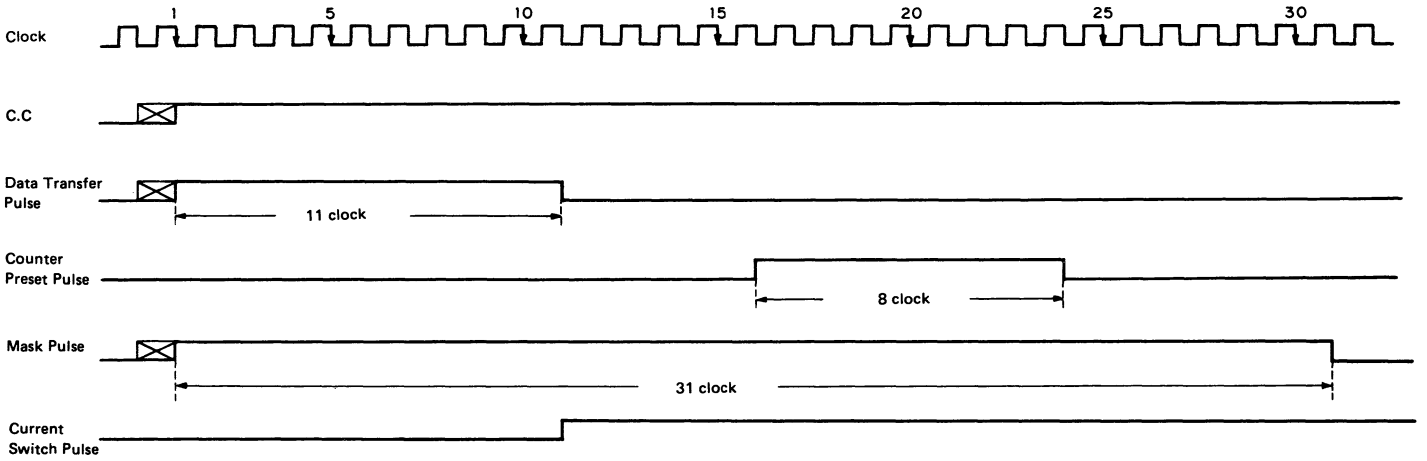


Fig. 2

Stereo Mode

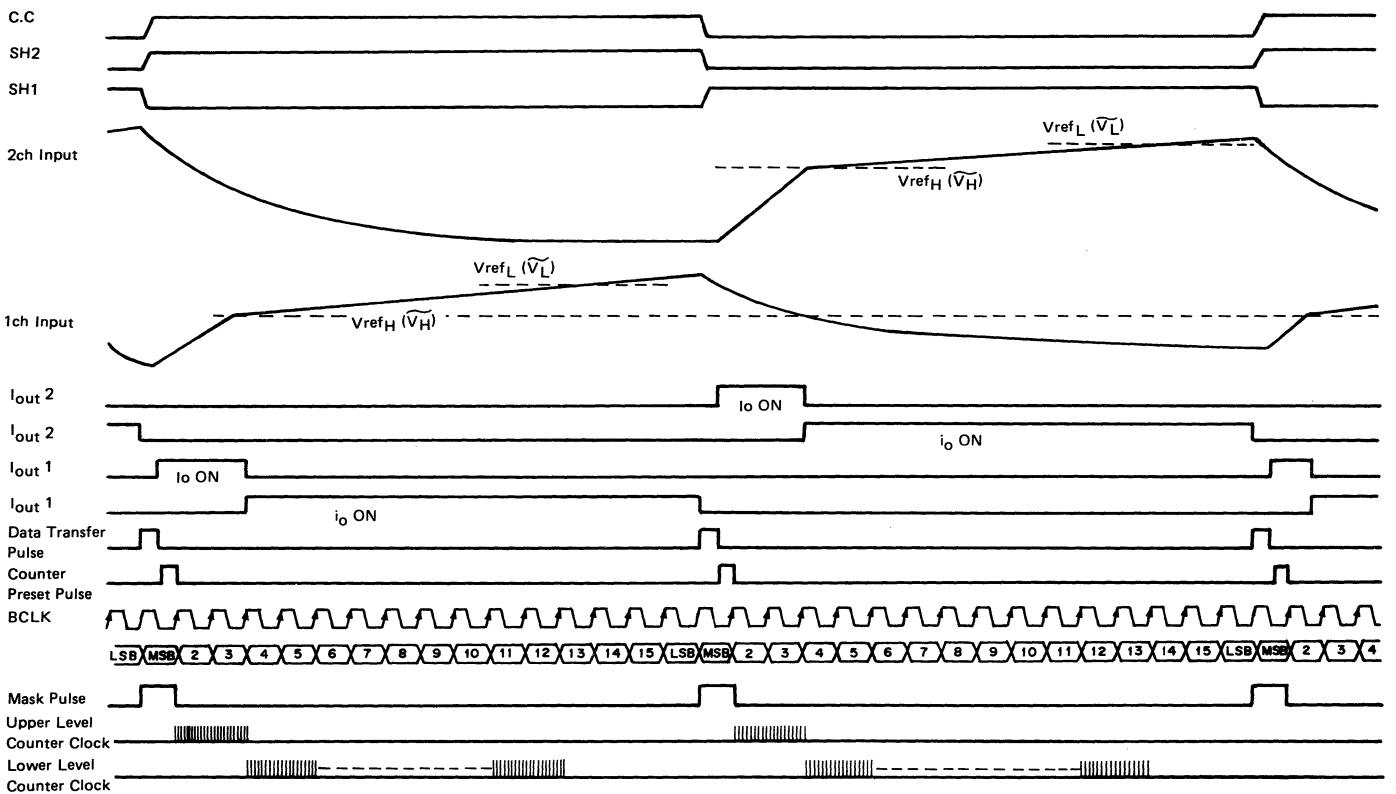


Fig. 3

Monaural Mode

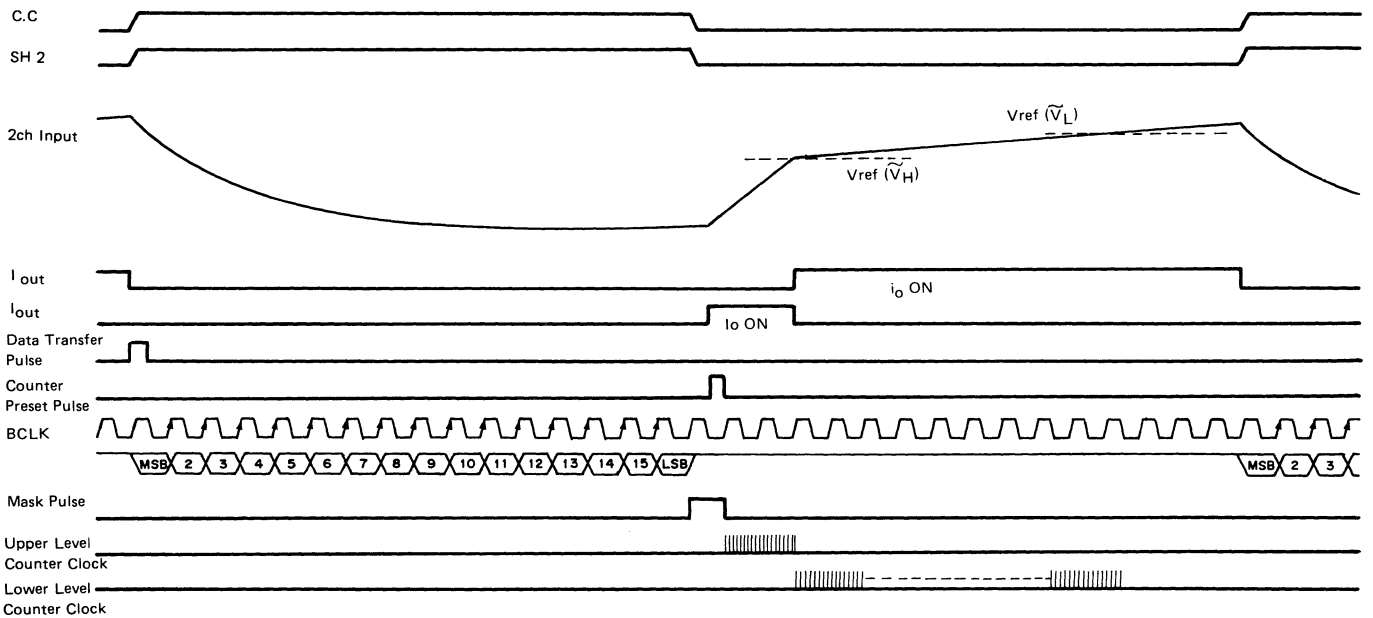


Fig. 4

Interface Circuit, Divider Circuit, Sample Hold Circuit

(1) Integral current output

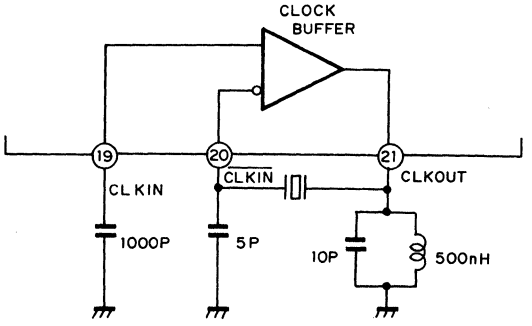
Recommended value; $I_{set} = 410\ \mu A$

$$\left(\begin{array}{l} I_o = 4\ I_{set} = 1.64\ mA \\ i_o = \frac{1}{32}\ I_{set} = 12.8\ \mu A \end{array}\right) \quad \text{at } C = 1000\ pF \quad f_{MCLK} = 84.6\ MHz \text{ full scale } 10V$$

$I_{set} = 750\mu A$

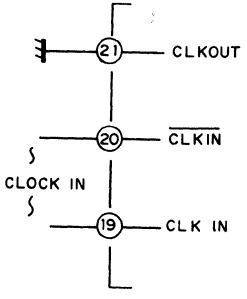
(2) Clock Buffer

(a) Internal clock (Excited circuit with crystal)

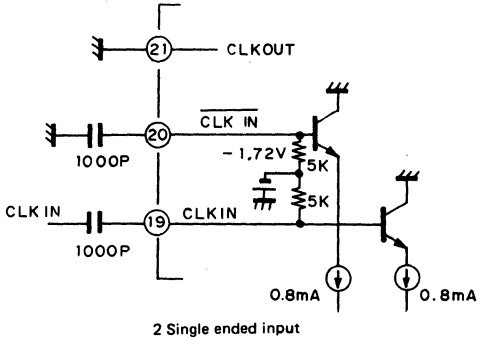


(X'tal 84.6 MHz)

(b) External clock



1 Balanced input



2 Single ended input

Select guide of master clock frequency

- Maximum operation clock frequency 100 MHz
- The minimum number of clock for a conversion is calculated as follows.

$(2^9 - 2) + 2 \times (2^7 - 1) + (2^5 - 1) = 795$ clocks

Upper level Counter — Lower level counter — Timing circuit

In case of conversion frequency of 44.06 kHz,

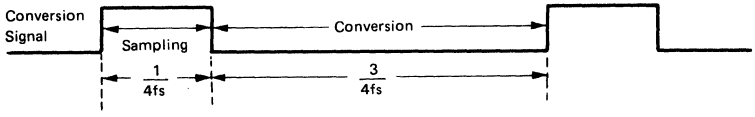
$2f_s \times 795 = 70.1$ MHz f_s: Sampling frequency

$f_{MCLK} \geqq 71$ MHz (Conversion time is assigned 1/2 of period.)

- Conversion time is assigned 3/4 of a period in monaural mode.

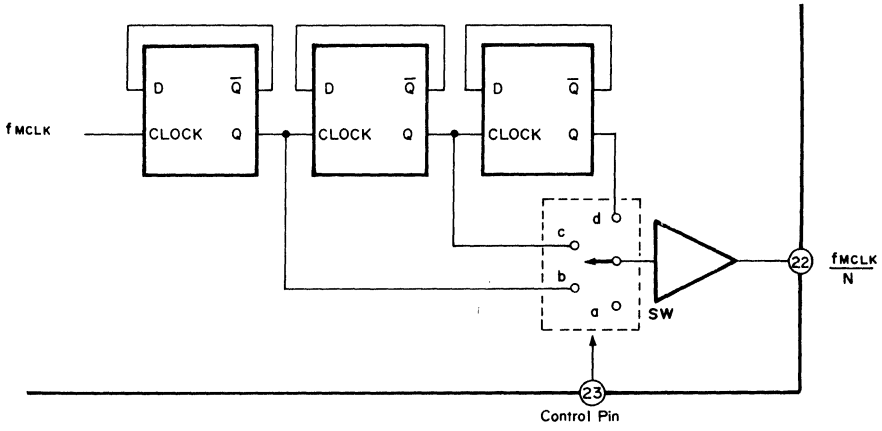
$f_{MCLK} \geqq 48$ MHz

Note; See as follows

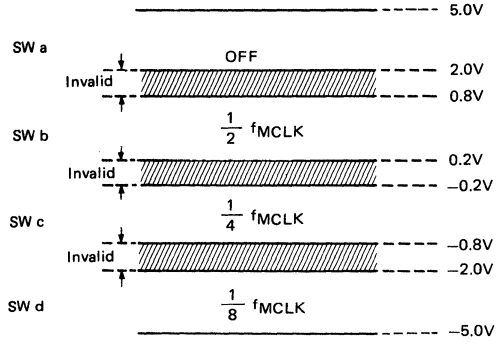


(3) f_{MCLK}/N Output

The output of f_{MCLK}/N is prepared for synchronous operation with digital circuit. Divided Value "N" is determined by external control, and N is 2, 4, 8 or ∞.



Basic Divider Block

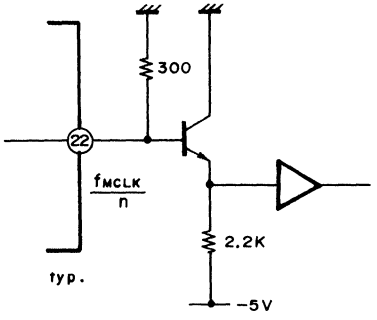


Threshould value of Control Pin

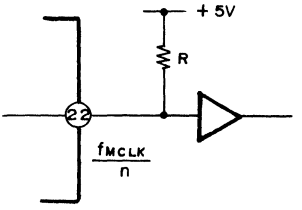
N	V_{CTL} Range
∞	$5.0V \geqq V_{CTL} \geqq 2.0V$
2	$0.8V \geqq V_{CTL} \geqq 0.2V$
4	$-0.2V \geqq V_{CTL} \geqq -0.8V$
8	$-2.0V \geqq V_{CTL} \geqq -5.0V$

(4) Recommended Interface Circuit

(a) ECL 10k (N=2)

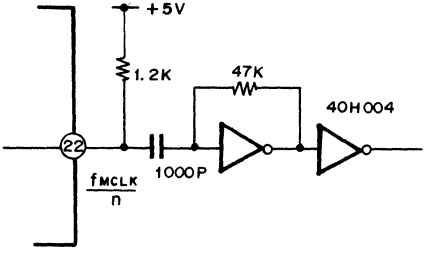


(b) TTLs (N=4 or 8)



R = 9.1K
R = 3.6K (LS)
R = 3K (ALS)

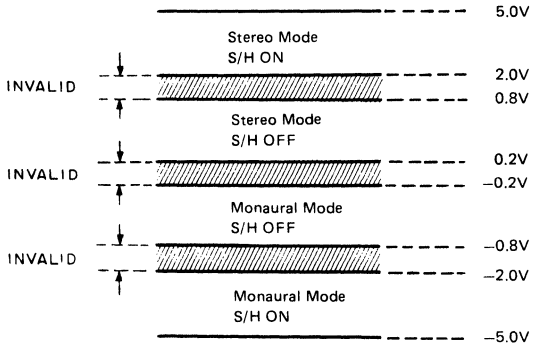
(c) High Speed CMOS (N=8)



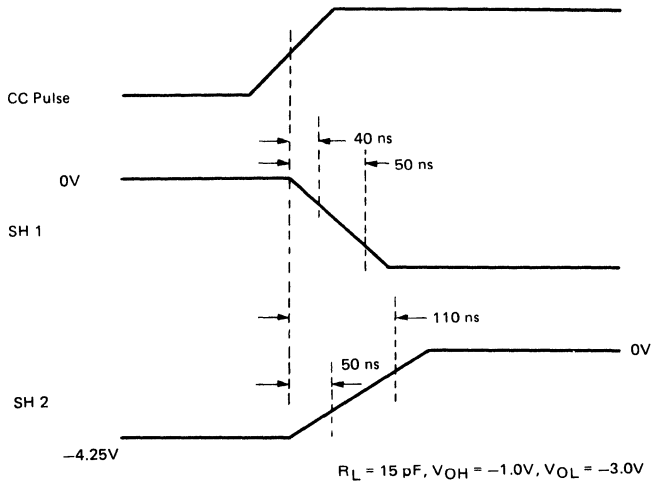
(5) Stereo mode, Monaural mode

Stereo or Monaural modes can be selected by mode pin. And "ON" or "OFF" state of Sample Hold Pulse is selected similary.

This is illustrated in the following way.

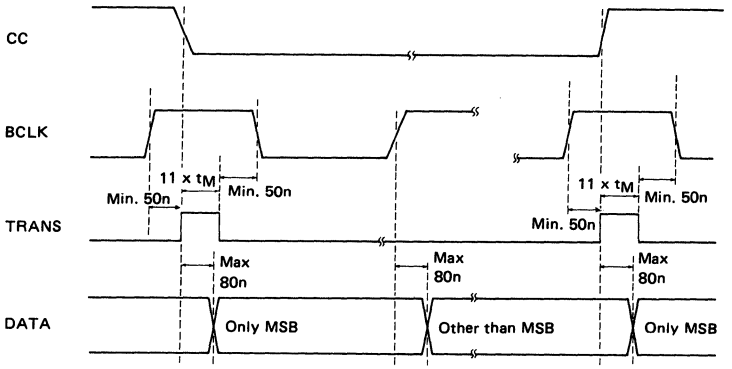


S/H Pulse



Propagation Delay Times from CC input to SH1, SH2 output

(6) Data Out



(Only MSB is delayed against the CC pulse. Others are delayed against the bit clock.)
t_M: One cycle of master clock

The counter data which have been converted are transmitted to the shift register with the TRANS pulse. However, due to the circuit structure of the shift register, it cannot be transmitted unless the BCLK and TRANS are simultaneously at high.

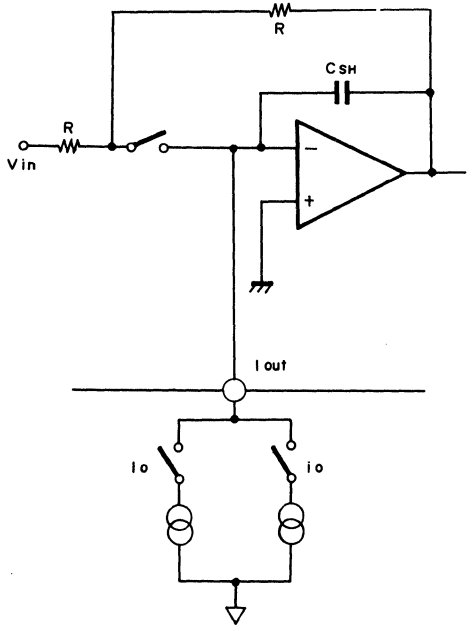
Propagation Delay Time from CC or BCLK Data Out

(7) Relationship of V_{in} max, CSH, I_{set}, I_o and i_o

(1) Vin is defined as the input voltage of integrator.

(2) I_o, i_o are defined as the coarse and fine integral current respectively.

(3) In case of a full scale input voltage.



$$V_{in}\ max = \frac{I_o\ \tau_o}{CSH}(2^9 - 1) + \frac{i_o\ \tau_o}{CSH}(2^7 - 1)$$

Using $I_o = 4I_{set}$, $i_o = \frac{1}{32} I_{set}$

$$V_{in}\ max = \frac{1}{32} \cdot \frac{I_{set}\ \tau_o}{CSH}(2^{16} - 1)$$

Assuming, $V_{in}\ max = 10$ Vp-p, $\tau_o = \frac{1}{f} = \frac{1}{84.6\ MHz}$

$CSH = 1500$ PF

$\therefore I_{set} = 620\ \mu A$

$\therefore 1LSB = \frac{i_o\ \tau_o}{CSH} = 152uV$

Note) In case of non-inverting operation, Vin Max. is limited to 5 Vp-p.

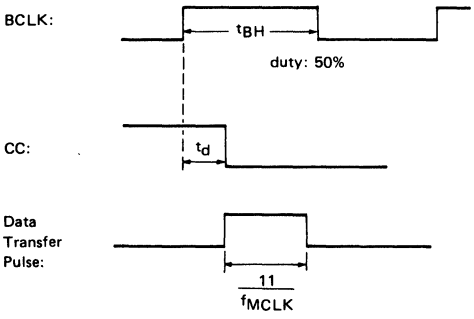
(8) The maximum frequency of BCLK.
The maximum frequency of BCLK is derived as follows:

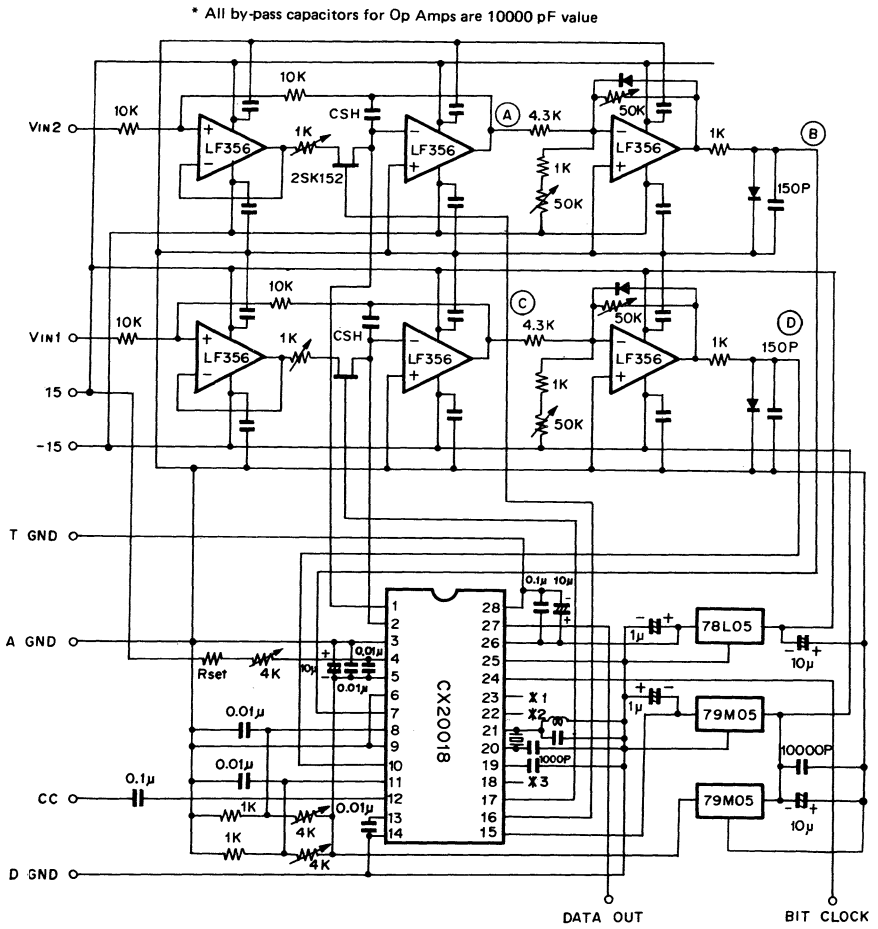
$$f_{BCLK} = \frac{1}{2t_{BH}}$$

$$t_{BH} \geqq td + \frac{11}{f_{MCLK}} + 50^{ns}$$

$$0^{ns} \leqq td \leqq 100^{ns}$$

Therefore,
$f_{BCLK} \leqq 1.7$ MHz on condition that the duty of BCLK is 50%.
$f_{BCLK} \leqq 1.7 \times \frac{X}{50}$ MHz on condition that the duty is X%.

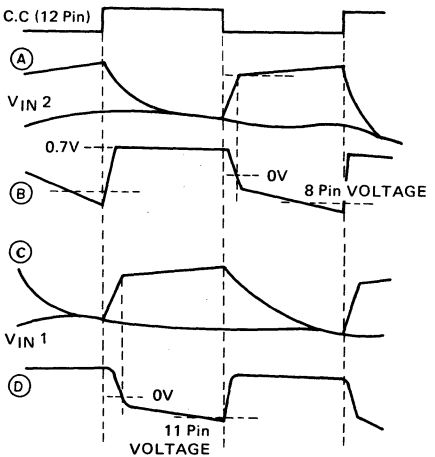




Typical Application

16 Bit AD Convertor Peripheral Circuit (Stereo Mode)

Wave Form



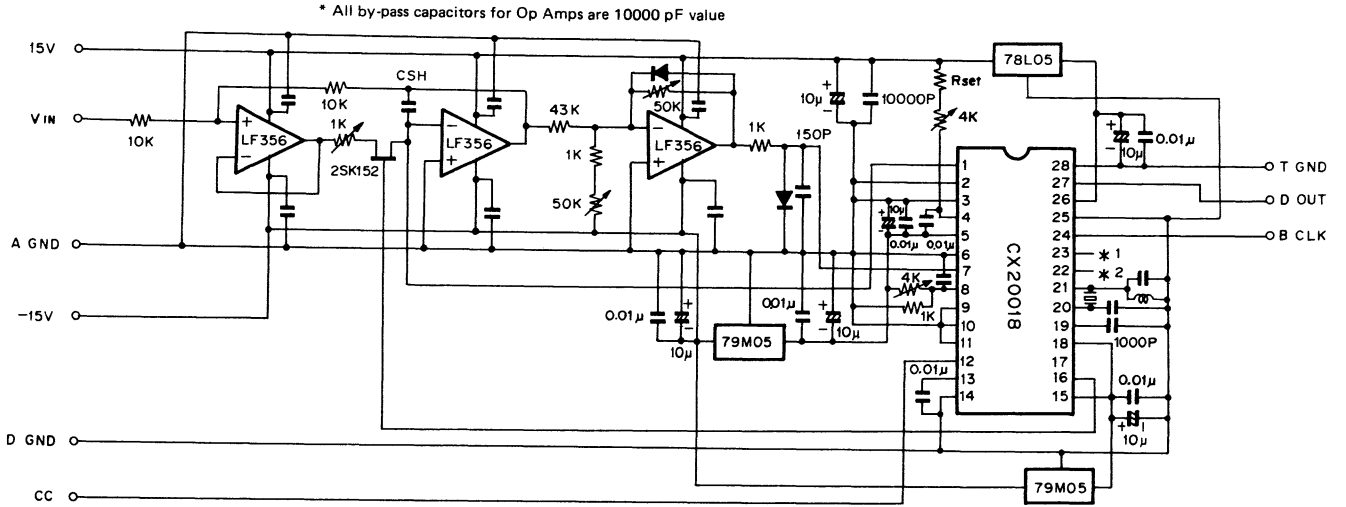
* 1, 2, 3: See to Page 13 and 14.

* Rset, CSH: See to Page 16.
(Rset = 42 kΩ when Iset = 410 μA, Rset = 22 kΩ when Iset = 750 μA.)

Fig. 5 16 bit A/D Converter Peripheral Circuit (Stereo Mode)

Typical Application — Monaural Mode

16 Bit AD Convertor Peripheral Circuit (Monaural Mode)



* 1, 2: See to Page 13 and 14.

* Rset, CSH: See to Page 16 (Rset = 42 kΩ when Iset = 410 μA, Rset = 22 kΩ when Iset = 750 μA).

Fig. 6 16 bit A/D Converter Peripheral Circuit (Monaural Mode)

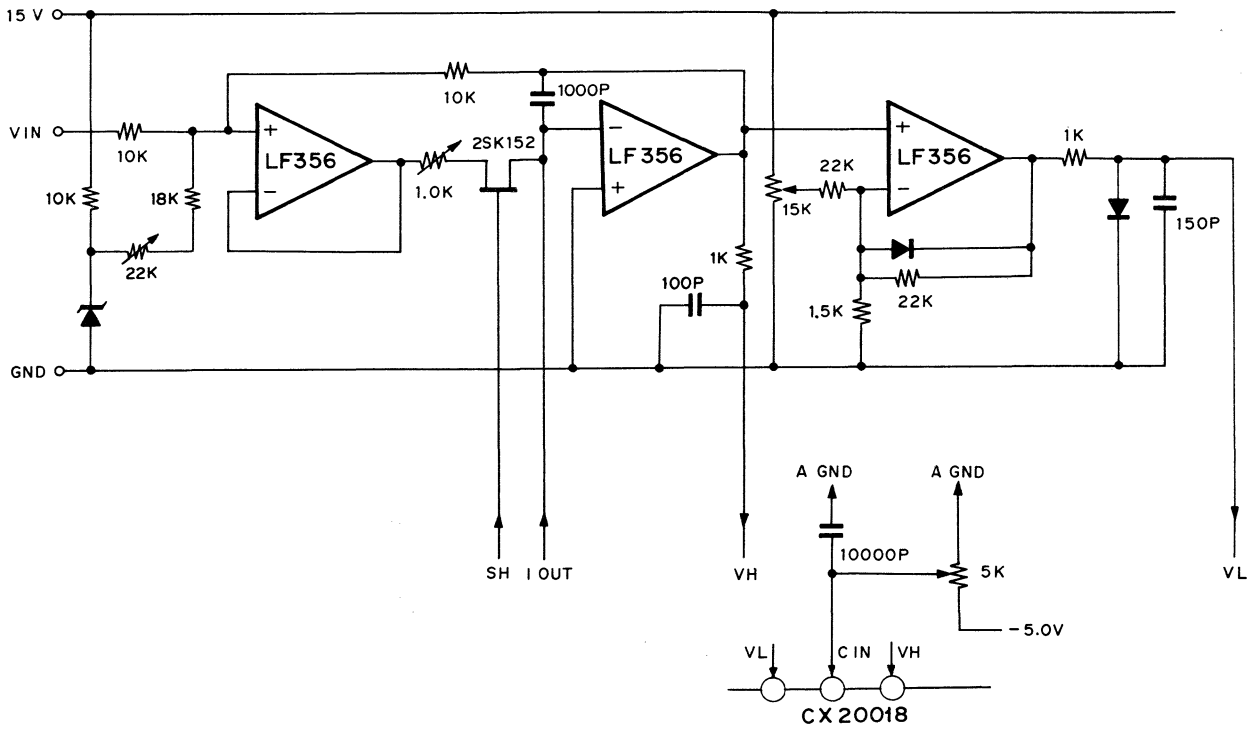
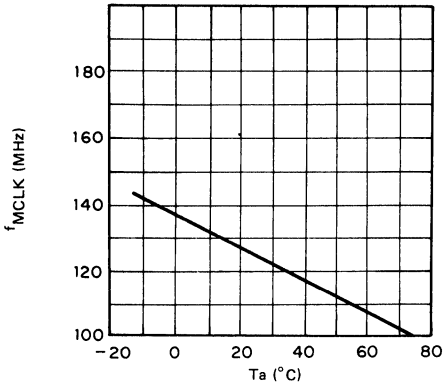
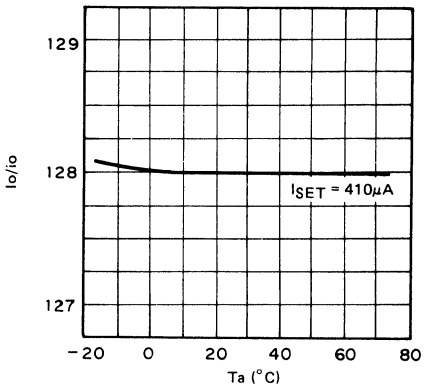


Fig. 7 Application Circuit (Non-inverting Circuit)

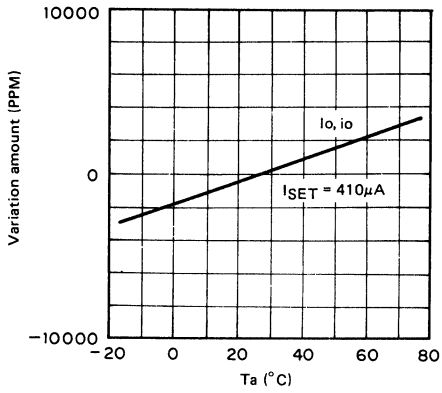
fMCLK temperature characteristics



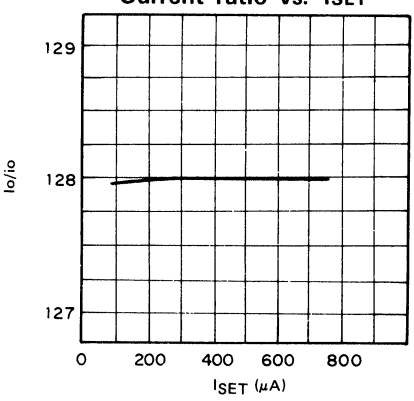
Current ratio temperature characteristics



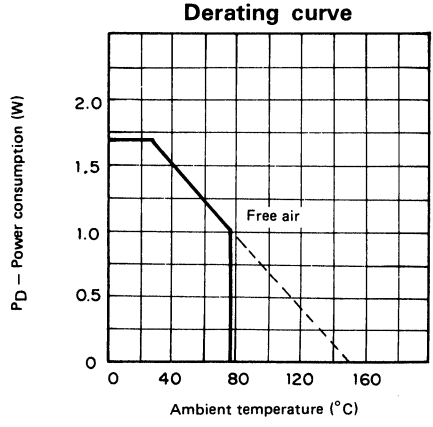
Output current temperature characteristics



Current ratio vs. ISET



Derating curve



16 bit D/A Converter

Description

The CX20133 is a 16 bit D/A converter IC for PCM audio using the integrating formula. Analog signal is reproduced from the 16 bit digital signal by combining an integrator, analog switch and low-pass filter to the IC exterior. Following circuits are also built-in so that it can be operated in sync with the CX23035, LSI for CD (compact disc) system.

- Integrating current output
- Two channels of discharge signal output
- Level shifting for interface direct with TTL/MOS LSIs.
- Analog switch drive.

Features

- Miniature flat package requires only small mounting area.
- Conversion frequency of 44.1 kHz.
- Serial data input.
- Low distortion factor typically at 0.003%.

Structure

- Bipolar Silicon Monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

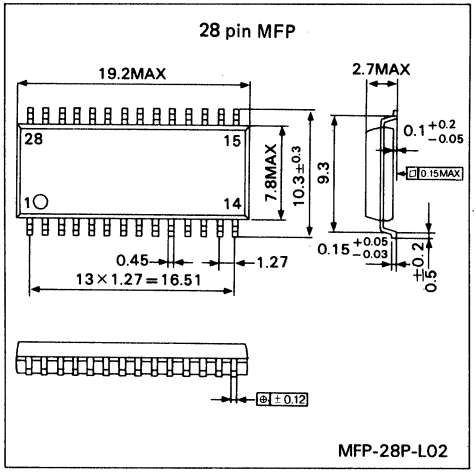
• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	T_{opr}	−10 to +75	°C
• Storage temperature	T_{stg}	−50 to +125	°C
• Allowable power dissipation	P_D	1.1	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ± 0.25	V
	V_{EE}	−5 ± 0.25	V

Package Outline

Unit: mm



Block Diagram

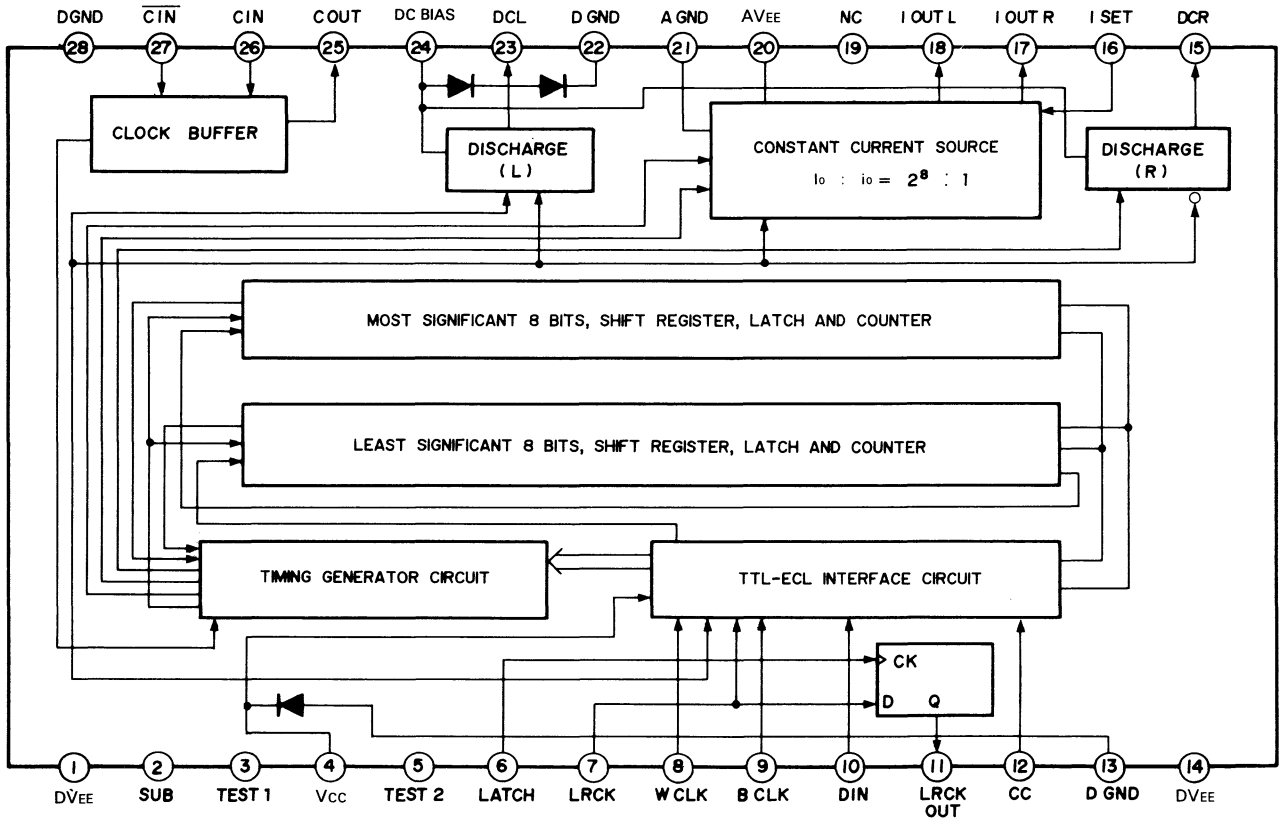


Fig. 1

SONY

Pin Description

No.	Symbol	Description
1	DV_{EE}	Power supply pin for the digital circuit. Applied with −5 V.
2	SUB	IC substrate. Always connected to 1 pin.
3	TEST 1	Test pin, normally open.
4	V_{CC}	Power supply pin for the digital circuit. Applied with +5 V.
5	TEST 2	Test pin, normally open.
6	LATCH	Clock pin of D-type clutch.
7	LRCK	LRCK input pin.
8	WCLK	WCLK input pin.
9	BCLK	BCLK input pin.
10	DIN	DIN (data input pin).
11	LRCK OUT	LRCK output pin.
12	CC	CC input pin.
13	DGND	Ground pin for the digital circuit.
14	DV_{EE}	Power supply pin for the digital circuit. Applied with −5 V.
15	DCR	Output pin of R-channel discharge driving signal.
16	ISET	Pin for setting integration current.
17	IOUTR	Output pin for R-channel current.
18	IOUTL	Output pin for L-channel current.
19	NC	No connection.
20	AV_{EE}	Power supply pin for the analog circuit.
21	AGND	Ground pin for the analog circuit.
22	DGND	Ground pin for the digital circuit.
23	DCL	Output pin for L-channel discharge driving signal.
24	DCBIAS	Bias pin for the discharge circuit.
25	COUT	Output pin for the clock oscillator.
26	CIN	Positive input pin for the clock oscillator.
27	$\overline{CIN}$	Negative input pin for the clock oscillator.
28	DGND	Ground pin for the digital circuit.

Electrical Characteristics

(Ta = 25°C, V_{EE} = −5.0V, V_{CC} = 1.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Circuit current	I_{EE}	1, 2, 14, 20	−112	−85		mA	1
Circuit current	I_{CC}	4		9.5	12.5	mA	1
Input threshold voltage	V_{TH}	6, 7, 8, 9, 10, 12		2.1		V	
High-level input voltage	V_{IH}	6, 7, 8, 9, 10, 12	2.8			V	
Low-level input voltage	V_{IL}	6, 7, 8, 9, 10, 12			0.8	V	
High-level input current	I_{IH}	6, 7, 8, 9, 10, 12 V_{IH} = 4.5V			500	μA	
Low-level input current	I_{IL}	6, 7, 8, 9, 10, 12 V_{IL} = 0V			500	μA	
High-level output voltage	V_{LRCKH}	11 Pin 7 = 4.5V I_{OH} = −100μA Pin 6:1 clock input:0V−5V−0V	2.7			V	
Low-level output voltage	V_{LRCKL}	11 Pin 7 = 0V I_{OL} = 100μA Pin 6:1 clock input: 0V−5V−0V			−2.7	V	
Clock input bias voltage	V_{CIN}	26, 27		−1.3		V	
Clock high-level output voltage	V_{CCR}	25		−0.8		V	
Clock low-level output voltage	V_{COL}	25		−1.6		V	
Current output pin leak	$I_{O\ LEAK}$	17, 18 Pins 17, 18: voltage = 0V when current output is off.			1.5	μA	
I_{OUT} output current	I_{OUT}	17, 18 Pins 17, 18: voltage = 0V Pin 16 I_{SET} = 500μA (I_{OUT} = Io − io)		2.008		mA	
Current ratio*1	Io/io	17, 18 Pin 16 I_{SET} = 250μA	255.0	256.0	257.5	−	2
Discharge circuit current dissipation	I_{DC}	24 Set Pin 24 to 0V.	1.35	1.9	2.5	mA	
Discharge circuit high-level output voltage	V_{DCH}	15, 23 Pin 24 voltage = 1.4V Load current = −100μA	0.27	0.45	0.77	V	
Discharge circuit low-level output voltage	V_{DCL}	15, 23 Pin 24 voltage = 1.4V Load current = −100μA		−4.2	−3.5	V	
Maximum I_{SET} current	$I_{SET\ MAX}$	16 In the range when the $I_{OUTL(R)}$ current ratio satisfies 255 < Io/io < 257			575	μA	
Distortion factor	THD	Both right and left, 0dB (full scale) reproduction 680Hz		0.003	0.005	%	3
		Both right and left, −20dB reproduction 680Hz		0.02	0.025	%	3
Operating clock frequency	f_{CLK}	Self-activating/Activated			36	MHz	

Note 1) Ground Pins 13, 17, 18, 21, 22, 24 and 28. Connect Pin 16 via a resistor of 5.1 kΩ and keep other pins open.

2) Io and io must satisfy the relation below in the Current Ratio Test Circuit (Fig. 3):
$-3.9\ (mV) < 1\ (k\Omega) \times Io\ (\mu A) - 256\ (k\Omega) \times io\ (\mu A) < 5.9\ (mV)$

3) See the Test Circuit (Fig. 2).
Conversion frequency: 44.1 kHz
Input data: Use the 16 bit full-scale data (0 dB) generated by the data generator.
Distortion meter: Use the HP339A (with all filters on) or the like provided with 80 kHz LPF, 30 kHz LPF and 400 Hz HPF.

*1 In the Current Ratio Test Circuit (Fig. 3),
$-3.9(mV) < 1(k\Omega) \times Io(\mu A) - 256(k\Omega) \times io(\mu A) < 5.9(mV)$

Description of the Conversion Operation

(1) Data call (BCLK, DIN, WCLK, LRCK). Refer to Fig. 6.

The data comes in 16 bit serial signal with 2's compliment. The data is sent sequencially into the IC beginning from MSB in sync with the rise of the bit clock (BCLK). (The data change represents the BCLK fall).

When the word clock (WCLK) is changed from the high-level to low-level at the 17th fall of BCLK, the 16 bit data is transferred from the shift register to the latch by the fall signal.

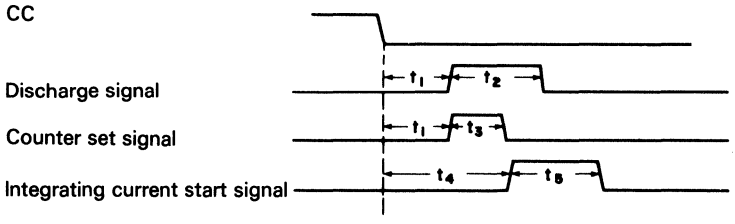
When the CX20133 is used in the stereo mode, data from other channels are sent in from the 17th BCLK.

In the stereo mode, Rch data is called when LRCK at the low level and Lch data is called in when the LRCK is at the high level. IOUTL and DCL operate only when LRCK is at the low level and IOUTR and DCR operate only when LRCK is at the high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are input from the clock input (CIN) with conversion command at the high level, all inner timing circuits are reset.

After resetting, the inner timing circuit starts operation when a clock is input from CIN with CC at the low level. The three signal generated this way are the discharge signal, counter set signal and integrating signal. Time of these three signals is determined depending on the clock cycle and their number of quantity:



$t_1 = .34 \times \tau o$
$t_2 = 67 \times \tau o$
$t_3 = 31 \times \tau o$
$t_4 = 65 \times \tau o$
t_5 Min $= 45 \times \tau o$ (input data 01 to 1)
t_5 Max $= 302 \times \tau o$ (input data 10 to 0)

The counter set signal is to set the data input to the latch to the counter and it is not output externally.

The discharge signal is output from DCL and DCR and it is controlled by LRCK. It is output from DCL when LRCK is at the low level and from the DCR when LRCK is at the high level.

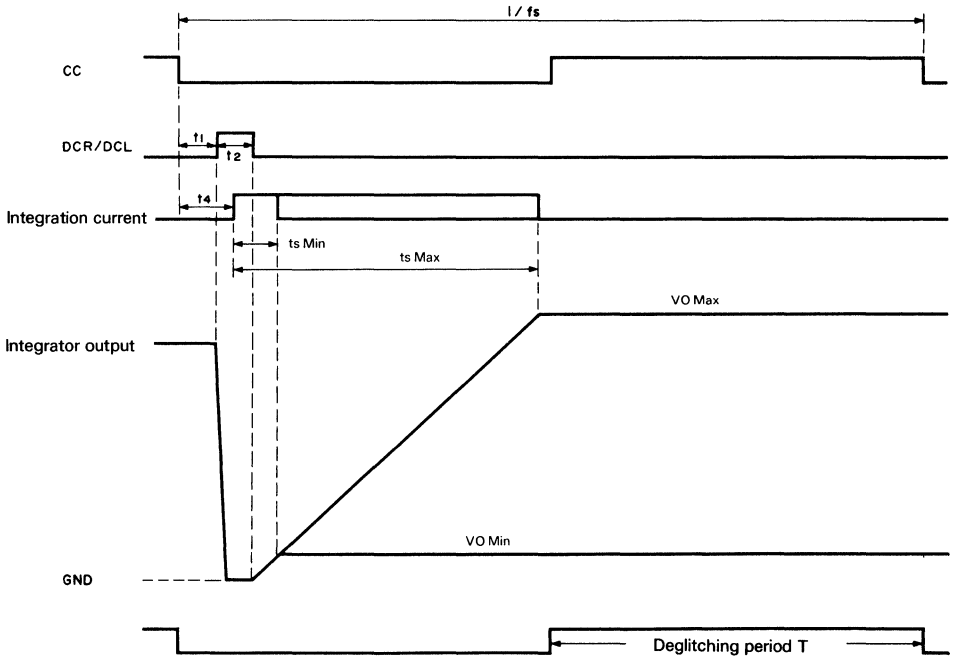
By the integrating current start signal, the upper current Io and lower current io start flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, measures the 11 offsets after completion of counting and outputs a signal to stop the integrating current.

The t5 value is varied between 0 and 255 by the preset input data in the counter.

Therefore, the conversion time from the start of low CC level to the completion of integrating requires t4 + t5 sec max.

The integrating current, like the discharge signal, is controlled by LRCK; IOUTL is output when LRCK is at the low level and IOUTR is output when LRCK is at the high level.

The Relation between Sampling Frequency fs and Clock



The maximum and minimum values of the integration voltage output, V_O Max and V_O Min, are expressed as follows:

$$V_O\,\text{Max} = \frac{I_O}{C} * \tau_O * 267 + \frac{i_O}{C} * \tau_O * 266 \qquad (t_4 + t_5\,\text{Max})$$

$$V_O\,\text{Min} = \frac{I_O}{C} * \tau_O * 12 + \frac{i_O}{C} * \tau_O * 11 \qquad (t_4 + t_5\,\text{Min})$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.

The relation between the conversion frequency fs and the clock frequency f_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$fs = \frac{f_{CLK}}{2 \times (t_4 + t_5\,\text{Max})} = \frac{f_{CLK}}{734}$$

where fs=44.1 kHz results in 32.4 MHz of f_{CLK}.

It is, however, recommendable to specify fs as the follow for the practical use because a settling time of 0.5 to 1.0 μs is required for the integrator after the current for t_5 disappears:

$$fs = \frac{f_{CLK}}{(t_4 + t_5\,\text{Max} + 1.0\ (\mu s)) + T}$$

(3) Integration current setting (ISET, IOUTL, LOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$\text{IOUTL (R)} = I_0 + i_0$$
$$= (4 + \frac{1}{64})\ \text{ISET}$$

where i_0 and I_0 are integration currents corresponded to the ILSB and 2^8·LSB, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_0 is given by the following equation:

$$V_0 = \frac{I_0}{C}(D_0 * 2^7 + \overline{D}_1 * 2^7 + \cdots\cdots + \overline{D}_7 * 2^0 + 12)\,\tau_0$$
$$+ \frac{i_0}{C}(\overline{D}_8 * 2^7 + \overline{D}_9 * 2^6 + \cdots\cdots + \overline{D}_{15} + 2^0 + 11)\,\tau_0$$

where $I_{SET} = 500\mu A$, $\tau_0 = \frac{1}{35\ (MHz)} = 28.6$ (ns) and C = 2000 pF result in the maximum output voltage V_0 Max of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$I_0 = 4 \cdot I_{SET}$

$i_0 = \frac{1}{64} \cdot I_{SET}$,

V_0 Max is calculated as the follow:

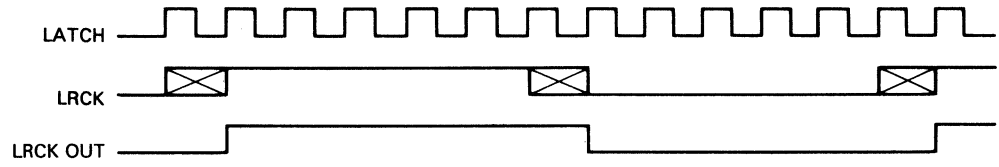
$$V_0\,\text{Max} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} * 267 * 28.6 \times 10^{-9}$$
$$+ \frac{500 * 10^{-6}/64}{2000 \times 10^{-12}} * 266 * 28.6 \times 10^{-9}$$
$$= 7.67\ (V)$$

(4) Operation of LRCK OUT

The LRCK OUT is an output for the analog switch IC (equivalent to MC14053B) drive to clip the output converted by the CX20133 and integrator as a PAM wave.

A PAM wave jitter may cause a conversion error and a D-type flip-flop is incorporated to eliminate this jitter; the LATCH input is used as a clock for the flip-flop.

This D-type flip-flop changes the output status in sync with the clock rise. The LRCK OUT operates only when +5 V is applied to Vcc. The output voltage level ranges from −2.7 V to +2.7 V enough to drive the CMOS analog switch effectively.



Timing of LATCH, LARCK and LRCKO

(5) Clock input/output pin (COUNT, CIN, $\overline{\text{CIN}}$)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased by the internal bias circuit. The (≈ -1.3 V) output amplitude level is 0.8 V.

(6) Bias pin (DVEE, SUB, DGND, VCC, AVEE, AGND, DC BIAS)

SUB is used at the common potential with DVEE. A standard value for the DVEE and AVEE is -5.0 V.

The CX20133 is devised so that it can operate when voltage at the digital input pin has a value between either 0 to -5 V or 0 to $+5$ V. When operated with an input between 0 and $+5$ V, $+5$ V must be applied to VCC. In this case, LRCK OUT is output as mentioned above.

When operated with an input between 0 to -5 V, VCC must be set open.

DC BIAS is for the bias circuit of the discharge signal output circuit. Supply current of (2.5 mA $+\alpha$) from a power supply of $+5$ V or above, because this pin requires approx. 2.5 mA current as a standard value. The potential at the pin is biased at 2 Vf.

A value α can be determined according to the following procedures. Approx. 0.5 mA current is necessary to retain 2 Vf (approx. 1.4 V) at this pin. The maximum current that flows through the load resistor RL attached to DCR (15 Pin) and DCL (23 Pin) is calculated as the follow:

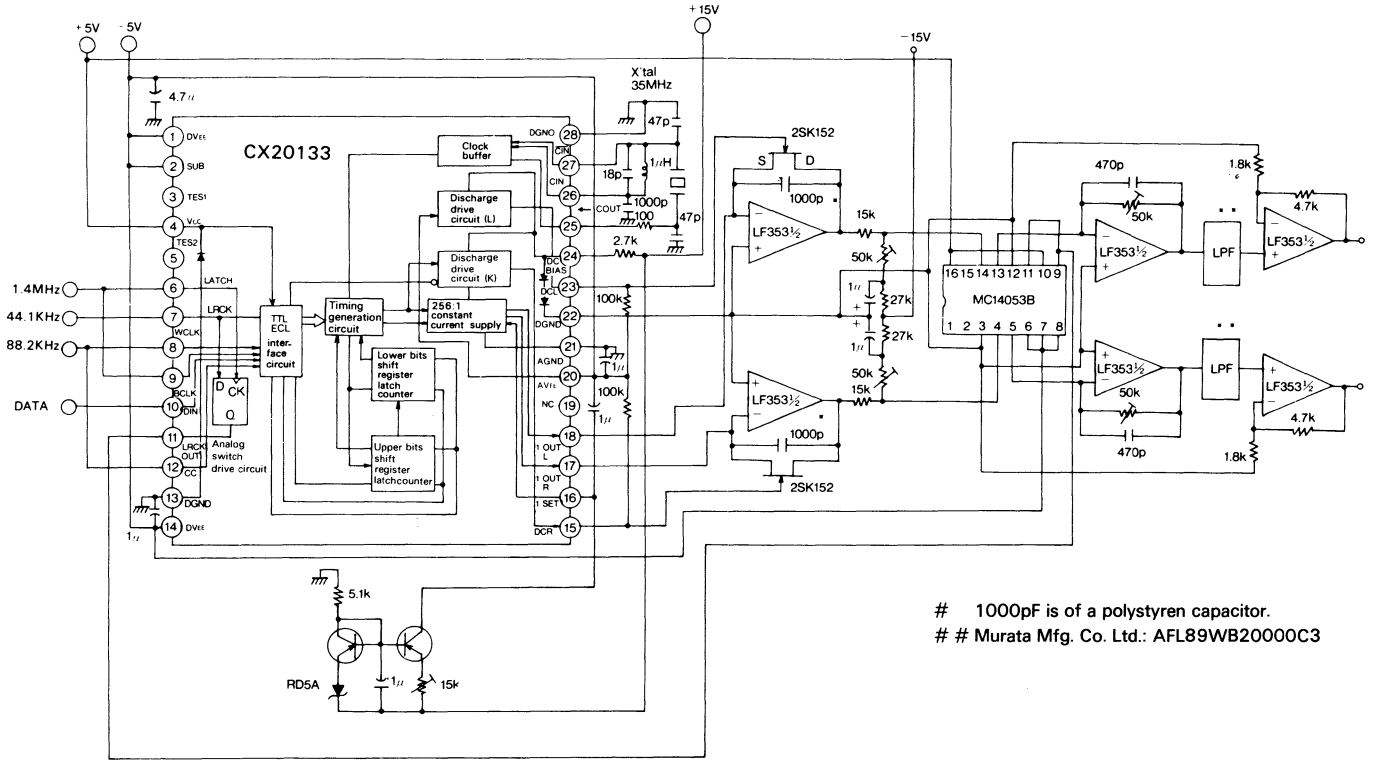
$$1/R_L \times (V_{DCH} + |DV_{EE}|)$$

The above equation results in 1.15 V where $R_L = 4.7\ k\Omega$, $V_{DCH} = 0.4$ V and $DV_{EE} = -5$ V are specified. Then α is calculated as

$$\alpha = 0.5 + 1.15 = 1.65\ (mA),$$

and required current is then obtained as 4.15 mA. Recommended value is 5 mA for $R_L = 4.7\ k\Omega$.

Application Circuit and Test Circuit

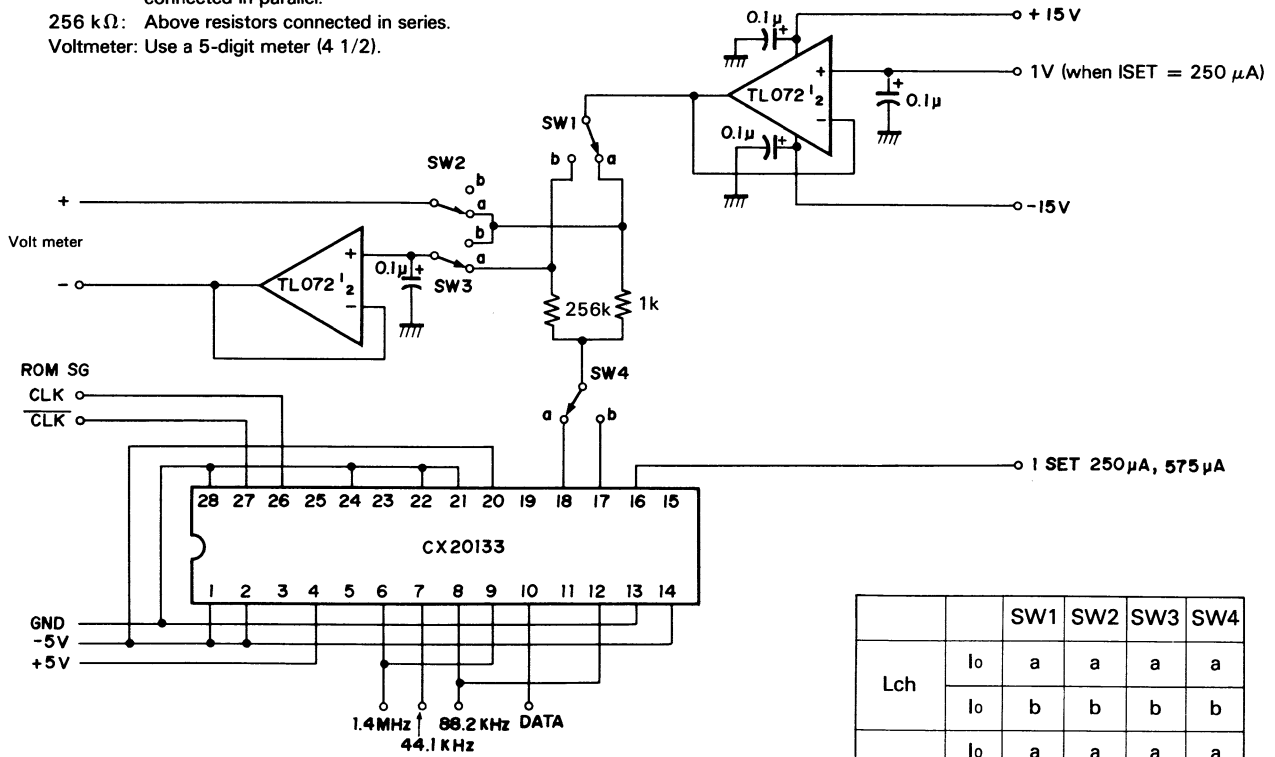


1000pF is of a polystyren capacitor.
Murata Mfg. Co. Ltd.: AFL89WB20000C3

Fig. 2

Current Ratio Test Circuit

1 kΩ: 16 kΩ ± 0.5%, 16 resistors connected in parallel.
256 kΩ: Above resistors connected in series.
Voltmeter: Use a 5-digit meter (4 1/2).



		SW1	SW2	SW3	SW4
Lch	Io	a	a	a	a
	Io	b	b	b	b
Rch	Io	a	a	a	a
	Io	b	b	b	b

Fig. 3

Sample/Hold Circuit for Deglitching

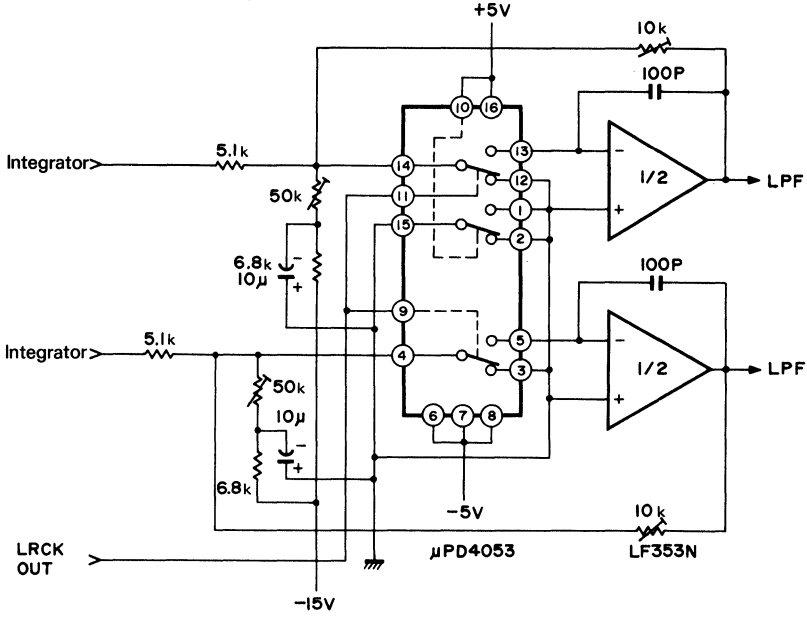
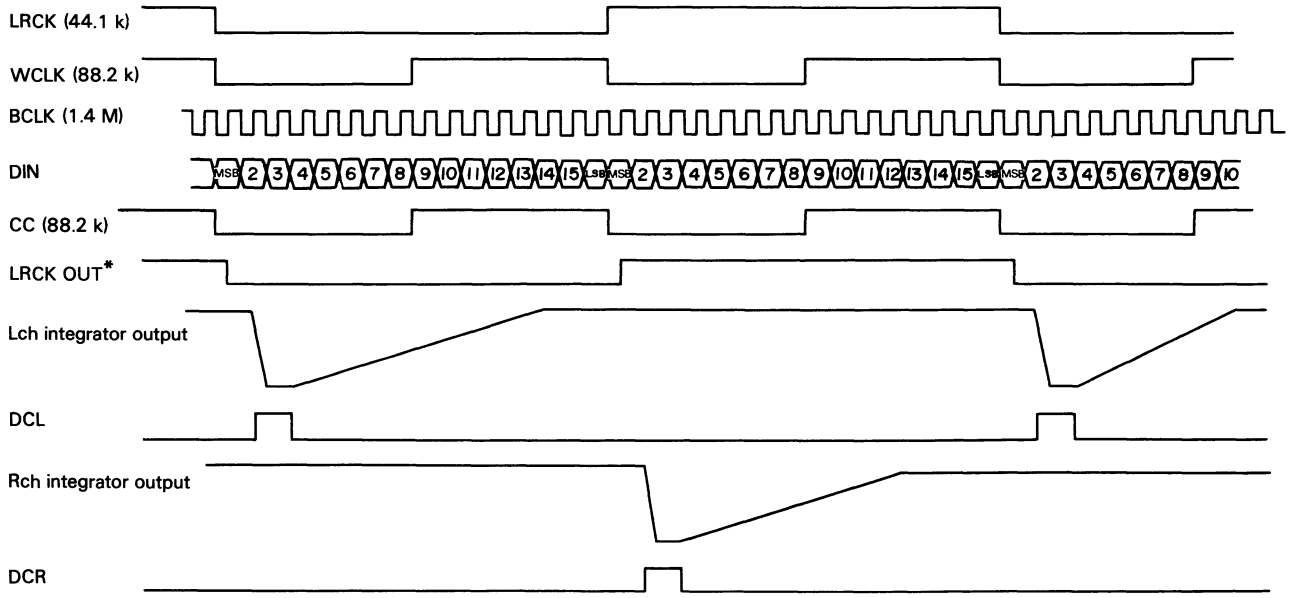


Fig. 4

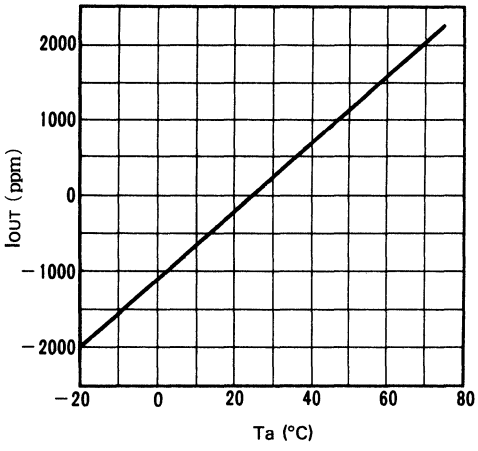
Timing Chart in the Stereo Mode



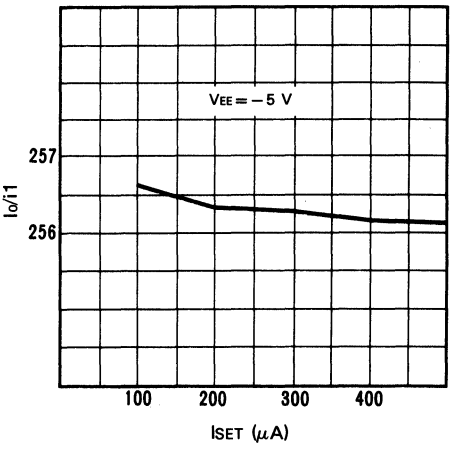
* When LATCH input is used as BCLK.

Fig. 5

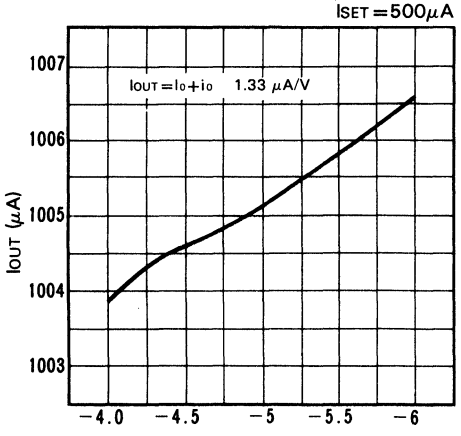
Temperature characteristics of I_{OUT} (I_O+i_O) (R, Lch common)



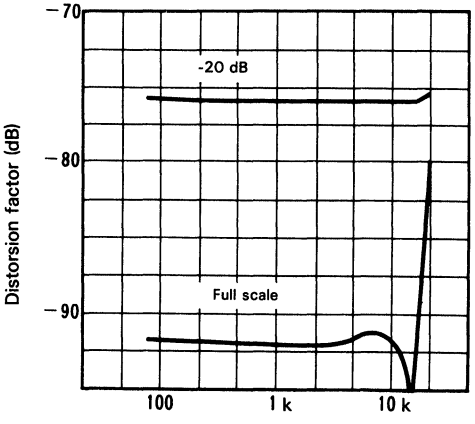
I_O/i_O vs. I_{SET}



Output current vs. Supply voltage (V_{EE})



Distortion factor



SONY CX20152

Dual 16 bit 88 kHz Multiplexed D/A

Description

CX20152 is a 16-bit D/A converter IC for PCM audio. It uses an integration system consisting of the following circuits.

- Clock signal generator
- TTL-ECL interface circuit
- Discharge drive circuit
- Analog switch drive circuit
- 1/4 frequency divider output circuit

By adding an integrator, analog switch and low pass filter externally to the IC, analog signal is reproduced from the 16-bit digital data.

Features

- Conversion frequency 88.2kHz
- Serial data input
- Low distortion factor 0.003% (typ.)
- 1/4-division output of the master clock is available for the clock of the CX23035, an single-chip LSI for CD, and the digital filter CX23034.

Structure

Bopolar Sillicon Monolithic IC

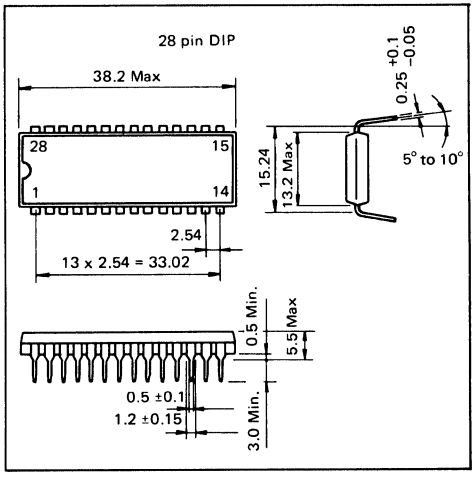
Absolute Maximum Rating

• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	2.1	W

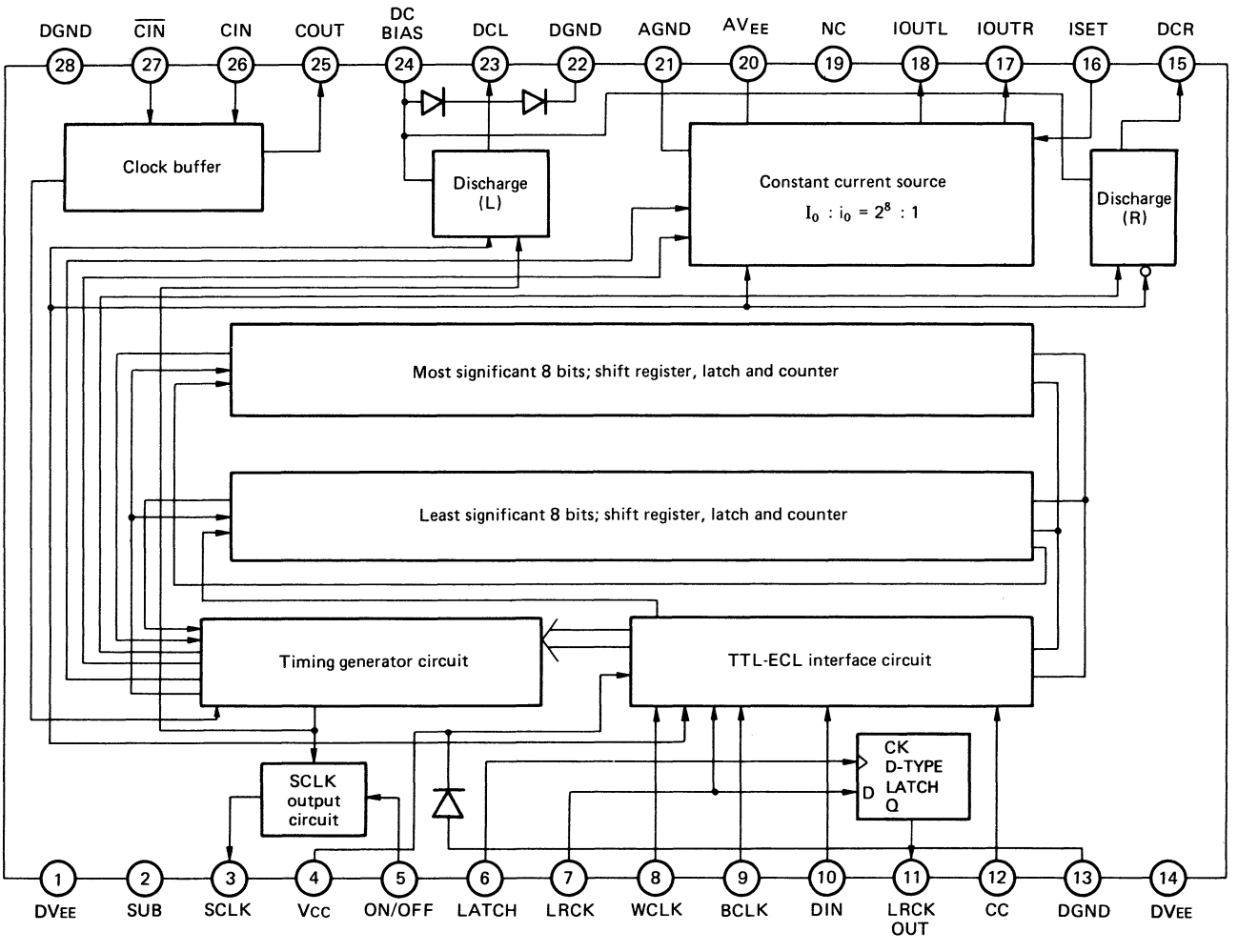
Recommended Operating Conditions

• Supply voltage	V_{CC}	5 ±0.25	V
	V_{EE}	−5 ±0.25	V

Package Outline Unit: mm



Block Diagram

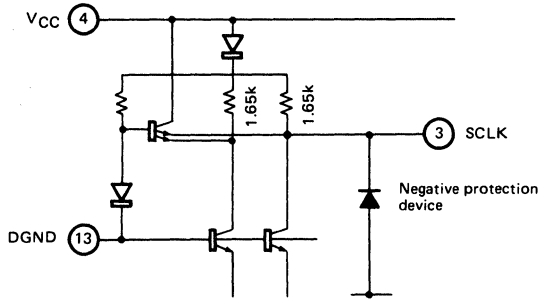
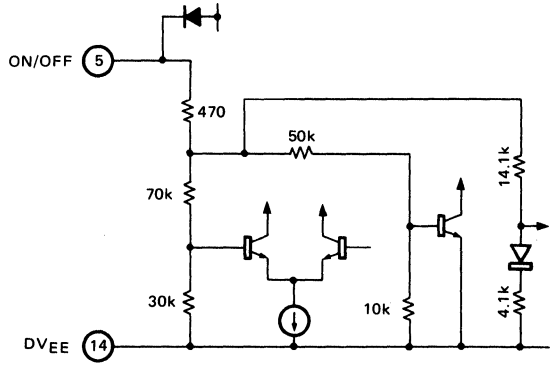


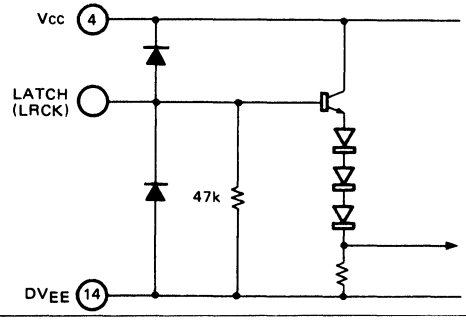
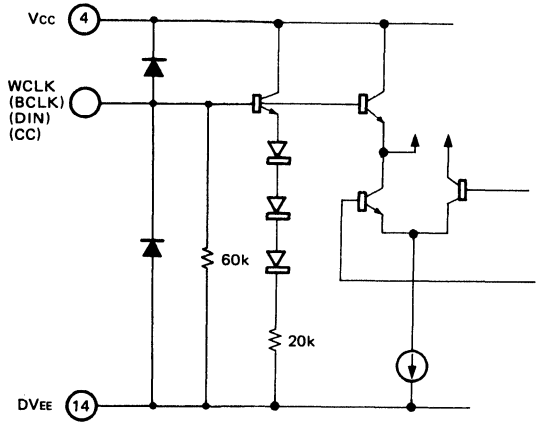
SONY

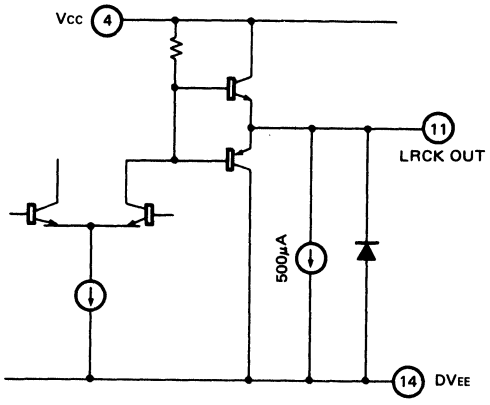
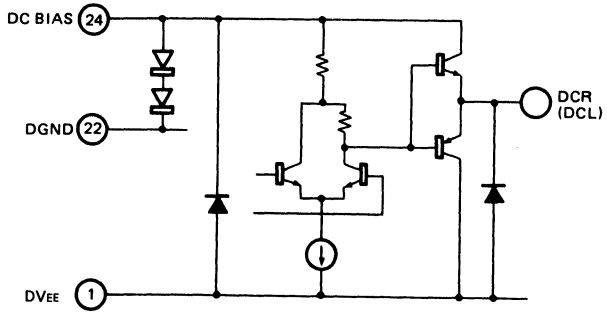
Pin Description

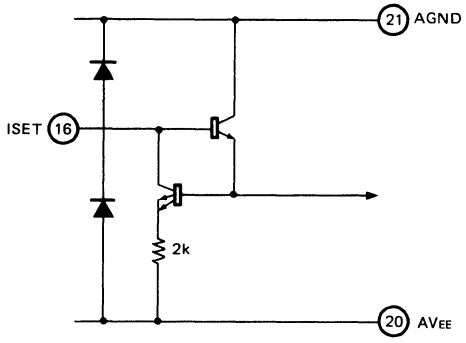
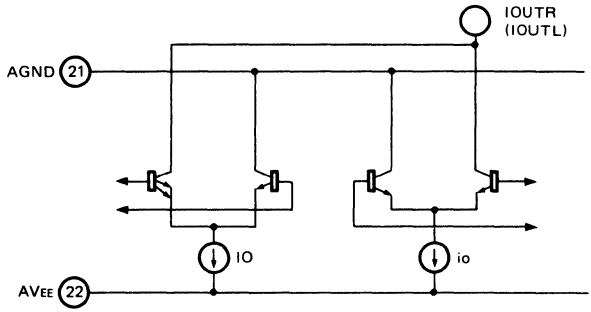
No.	Symbol	Description
1	DVEE	Digital VEE: −5V
2	SUB	IC substrate: Be sure to connect to Pin 1.
3	SCLK	System clock output pin
4	VCC	Digital VCC: +5V
5	ON/OFF	Pin to determine the system clock on/off
6	LATCH	Clock pin of D type latch
7	LRCK	LRCK input pin
8	WCLK	WCLK input pin
9	BCLK	BCLK input pin
10	DIN	DIN (data input pin): MSB first
11	LRCK OUT	LRCK output pin
12	CC	CC input pin
13	DGND	Digital ground
14	DVEE	Digital VEE: −5V
15	DCR	Right channel discharge drive signal output pin
16	ISET	Integration current setting pin
17	IOUTR	Right channel current output pin
18	IOUTL	Left channel current output pin
19	NC	No connection
20	AVEE	Analog VEE
21	AGND	Analog GND
22	DGND	Digital GND
23	DCL	Left channel discharge drive signal output pin
24	DC BIAS	Discharge circuit bias pin
25	COUT	Clock generator output pin
26	CIN	Clock generator positive input pin
27	$\overline{\text{CIN}}$	Clock generator negative input pin
28	DGND	Digital GND

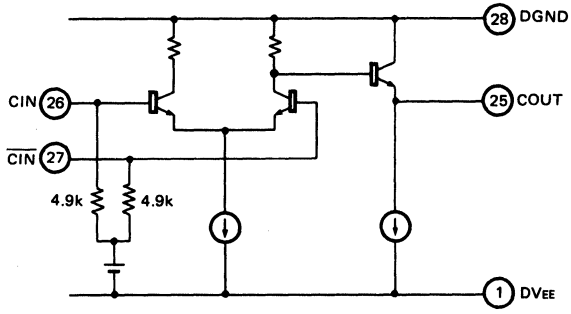
CX20152 Input/Output Pin Equivalent Circuits

No.	Symbol	Equivalent Circuits
1	DVEE	
2	SUB	
3	SCLK	
4	VCC	
5	ON/OFF	

No.	Symbol	Equivalent Circuit
6	LATCH	
7	LRCK	
8	WCLK	
9	BCLK	
10	DIN	
12	CC	

No.	Symbol	Equivalent Circuits
11	LRCK OUT	
13	DGND	
14	DVEE	
15	DCR	
23	DCL	
24	DC BIAS	

No.	Symbol	Equivalent Circuits
22	DGND	
16	ISET	
17	IOUTR	
18	IOUTL	
19	NC	
20	AVEE	
21	AGND	

No.	Symbol	Equivalent Circuit
25	COUT	
26	CIN	
27	$\overline{\text{CIN}}$	
28	DGND	

Electrical Characteristics

($Ta = 25°C$, $V_{EE} = -5.0V$, $V_{CC} = 5.0V$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Circuit current	I_{EE}	1, 2, 14, 20 Pins 4, 5 = 5V	−125	−95		mA
Circuit current	I_{CC1}	4 Pin 5 = 5V (6, 7, 8, 9, 10, 12, GND)		12.6	15.5	mA
Circuit current	I_{CC2}	4 Pin 5 = 0V (6, 7, 8, 9, 10, 12, GND)		5.9	10.0	mA
Input threshold voltage	V_{TH}	6, 7, 8, 9, 10, 12		2.1		V
High level input voltage	V_{IH}	6, 7, 8, 9, 10, 12	2.9			V
Low level input voltage	V_{IL}	6, 7, 8, 9, 10, 12			0.9	V
High level input current 1	I_{IH1}	5 $V_{IH} = 5V$		0.7	1.3	mA
High level input current 2	I_{IH2}	6, 7, 8, 9, 10, 12 $V_{IH} = 5V$		250	550	μA
Low level input current 1	I_{IL1}	5 $V_{IH} = 0V$		0.35	0.8	mA
Low level input current 2	I_{IL2}	6, 7, 8, 9, 10, 12 $V_{IL} = 0V$		120	550	μA
High level output voltage	V_{LRCKH}	11 With Pin 7 at 4.5V, set $I_{OH} = -100\mu A$ and input a clock of 0V–5V–0V to Pin 6.	2.7	4.2		V
Low level output voltage	V_{LRCKL}	11 With Pin 7 at 0V, set $I_{OL} = 100\mu A$ and input a clock of 0V–5V–0V to Pin 6.		−3.1	−2.7	V
SCLK output, high level	V_{SCLKH}	3 $I_{OH} = -10\mu A$	3.4	4.2		V
SCLK output, low level	V_{SCLKL}	3 $I_{OL} = 400\mu A$		0.5	1.6	V
Discharge circuit power dissipation current	I_{DCBIAS}	24 $V_{DCBIAS} = 0V$		1.9	2.5	mA
Discharge circuit high level output voltage	V_{DCH}	15, 23 Pin 24 voltage = 1.3V Load current = 1.2mA	0	0.4	0.65	V
Discharge circuit low level output voltage	V_{DCL}	15, 23 Pin 24 voltage = 1.3V Load current = 1.2mA		−4.2	−3.4	V
I_{SET} current	I_{SET}	16		0.5	1.0	mA
I_{OUT} output current	I_{OUT}	17, 18 Pins 17, 18: Voltage = 0V Pin 16: $I_{SET} = 500\mu A$ ($I_{OUT} = Io + io$)		2.008		mA
Clock input bias voltage	V_{CIN}	26, 27		−1.3		V
Clock high level output voltage	V_{COH}	25		−0.8		V
Clock low level output voltage	V_{COL}	25		−1.6		V
Current output pin leakage	Io_{LEAK}	17, 18 Pins 17, 18: Voltage = 0V when the current output is off.			1.5	μA
Current ratio	Io/io	17, 18 Pin 16: $I_{SET} = 500\mu A$	255.0	256.0	257.5	—
Distortion factor	THD1	Both right and left; 0dB (full scale) when reproduced.		0.003	0.005	%
	THD2	Both right and left; −20dB when reproduced.		0.02	0.025	%
Operation clock frequency	f_{CLK1}	Both self-drive & external-drive Ta = −20 ~ +70°C		68	80	MHz
Operation clock frequency	f_{CLK2}	Both self-drive & external-drive Ta = −20 ~ +75°C		68	75	MHz

Description of Conversion Operation

(1) Data pickup (BCLK, DIN, WCLK, LRCK)

Data consist of 16-bit serial signals in 2's complement. They are transmitted into the IC sequentially from the MSB in synchornization with the rise edge of the bit clock (BCLK). (The BCLK delay will change the data. The falling edge changes the data.)

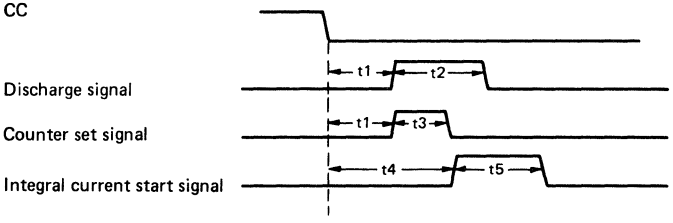
When the word clock (WCLK) is changed from high level to low level at the 17th BCLK, the 16-bit data is transferred from the shift register to the latch with the decay signal. When CX20152 is used in the stereo mode, other-channel data are transmitted from the 17th BCLK.

In the stereo mode, the Rch data is picked up when LRCK is at a low level and the Lch data is picked up when LRCK is at a high level. IOUTL and DCL operate only when LRCK is at a low level, and IOUTR and DCR operate only when LRCK is at a high level.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

When more than 3 clocks are fed from the clock input (CIN) with the conversion command (CC) at a high level, all the internal timing circuits are reset.

After the resetting, the internal timing circuit starts operation when a clock is input from CIN with CC at a low level. From this operation, three signals, Discharge, Counter set and Integral current Start, are generated. Timing of these signals is determined as follows by the clock interval τ_0 and its quantity.



$t1 = 35 \times \tau_0$
$t2 = 67 \times \tau_0$
$t3 = 31 \times \tau_0$
$t4 = 65 \times \tau_0$
$t5\ Min = 47 \times \tau_0$ (When the input data is 01 — 1)
$t5\ Max = 302 \times \tau_0$ (When the input data is 10 — 0)

The counter set signal is used to set the data input in the latch to the counter but does not output externally.

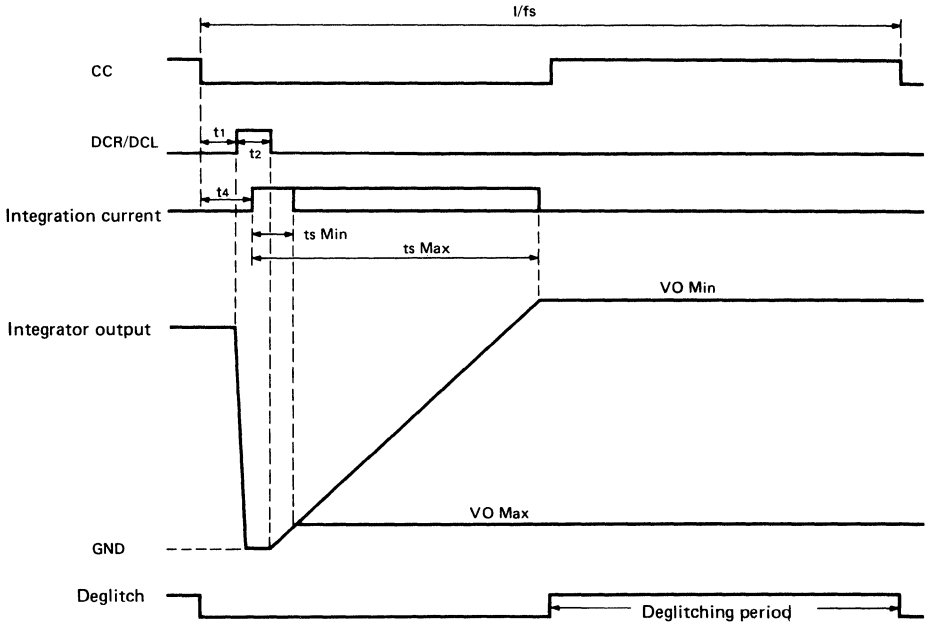
The discharge signal is output from DCL and DCR and controlled by LRCK. It is output from DCL when LRCK is at a low level and from DCR when LRCK is at a high level.

The integral current start signal starts the upper current Io and lower current io flowing. The counter starts counting from the preset value simultaneously when the discharge signal is off, counts 11 offsets after the end of the counting and outputs a signal to stop the integration current. The value t_5 is varied between 0 to 255 by the input data value preset to the counter.

Therefore, the time before the end of the integration after the low level has been set, i.e. the conversion time, requires the maximum ($t_4 + t_{5\ Max} = 367 \times \tau_0$) seconds.

The integration current of IOUTL is output, as with the discharge signal, when LRCK is at a low level; IOUTR is output when LRCK is at a high level.

(3) The relation between sampling frequency f_S and clock



The maximum and minimum values of the integration voltage output, $V_{O\ Max}$ and $V_{O\ Min}$, are expressed as follows.

$$V_{O\ Max} = \frac{I_0}{C} * \tau * 267 + \frac{i_0}{C} * \tau * 266 \qquad (t_4 + t_{5\ Max})$$

$$V_{O\ Min} = \frac{I_0}{C} * \tau * 12 + \frac{i_0}{C} * \tau * 11 \qquad (t_4 + t_{5\ Min})$$

where f_{CLK} is a clock frequency and τ is a period.

The integration voltage is held by the capacitor C in the integrator when the current is switched off. This voltage is used as D/A conversion output during the deglitching period T which is given according to the settling time of the deglitching circuit.
The relation between the conversion frequency f_S and the clock frequency F_{CLK} is given as below assuming that the conversion time and deglitching period are equivalent:

$$f_S = \frac{f_{CLK}}{2 \times (t_4 + t_{5\ Max})} = \frac{f_{CLK}}{734}$$

where f_S = 44.1 kHz results in 32.4 MHz of f_{CLK}

It is, however, recommendable to specify f_S as the follow for the practical use because a settling time of 0.5 to 1.0 μs is required for the integrator after the current for t_5 disappears:

$$fs = \frac{fCLK}{(t_4 + t_5\ Max + 1.0(\mu s) + T}$$

(4) Integration current setting (ISET, IOUTL, IOUTR)

Integration current is determined by a constant current value input through the ISET pin, which is given as below:

$$IOUTL\ (R) = I_0 + i_0 = (4 + \frac{1}{64})\ ISET$$

where i_0 and I_0 are integration currents corresponded to the ILSB and $2^8 \cdot$LSB, respectively.

If D_0 and D_{15} are specified as MSB and LSB, respectively, integrator output voltage V_0 is given by the following equation:

$$V_0 = \frac{I_0}{C}(D_0 * 2^7 + \overline{D}, * 2^7 + \ldots\ldots + \overline{D}_7 * 2^0 + 12)\tau_0$$

$$+ \frac{i_0}{C}(\overline{D_8} * 2^7 + \overline{D_9} * 2^6 + \cdots\cdots + \overline{D_{15}} * 2^0 + 11)\tau_0$$

where I_{SET} = 500 μA, $\tau = \frac{1}{35\ (MHz)}$ = 28.6 (ns) and C=2000 pF result in the maximum output voltage $V_{O\ Max}$ of the integrator when any of a value from 10 to 0 is given as an input data. Based on the relations below,

$$I_0 = 4 * I_{SET}$$

$$i_0 = \frac{1}{64} * I_{SET}$$

$V_{O\ Max}$ is calculated as the follow:

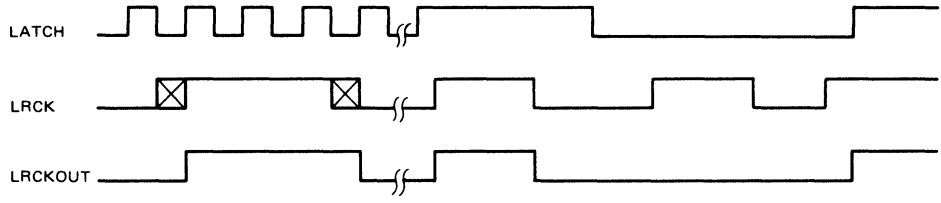
$$V_{O\ Max} = \frac{2.0 \times 10^{-3}}{2000 \times 10^{-12}} * 267 * 28.6 \times 10^{-9}$$

$$+ \frac{400 * 10^{-6}/64}{2000 \times 10^{-12}} * 266 * 28.6 \times 10^{-9}$$

$$= 7.67\ (V)$$

(5) LRCK OUT operation (LATCH, LRCK, LRCK OUT)

The LRCK OUT is a drive output of the analog switch IC (equivalent to MC14053B) to clip the output converted by CX20152 and the integrator so that the converted output can be a PAM wave. When the PAM wave has a jitter, a conversion error results. To absorb this jitter, a D-type latch is built-in and the LATCH input is used as its clock. The D-type latch varies the output state in synchronization with the rise of the clock. In the high-speed conversion (with sampling frequency of 88.2kHz), the clock frequency is as high as about 70MHz. This will affect the delay time of the analog switch IC; it is possible the delay time becomes equal to t_1. Then, the last part of the PAM wave overlasps on the discharge time causing a considerable conversion error. In such a case, LRCK can output its level by keeping LATCH at a high level. The output voltage level ranges from −2.7V to +2.7V, enable to drive CMOS analog switch.



Timing of LATCH, LRCK and LRCKOUT

(6) Clock input/output Pin (COUT, CIN and $\overline{\text{CIN}}$)

The clock buffer consists of a circuit equivalent to a general-purpose ECL logic circuit, with its input pin biased with an internal bias circuit (= −1.3V). The output amplitude level is 0.8V.

(7) Bias Pin (DVEE, SUB, DGND, VCC, AVEE, AGND and DC BIAS)

SUB denotes the IC substrate and its voltage potential should be common to that of DV_{EE}. The standard value of DV_{EE} and AV_{EE} is −5.0V.

V_{CC} is the power supply for the interface circuit from a CMOS or TTL level to the internal ECL logic. Its standard value is +5V.

DC BIAS is the bias circuit of the discharge signal output circuit. As it requires about 2.5mA as its standard current, supply current should be 2.5mA + α. This pin voltage is biased to $2Vf$ and the value of α is determined as follows.

To maintain the pin voltage at $2Vf$ ($\approx$ 1.4V), about 0.5 mA of current is required. Additionally, the maximum current flowing through the load resistor R_L attached to DCR (Pin 15) and DCL (Pin 23) is obtained from the following equation.

$$1/R_L \times (V_{DCH} + |DV_{EE}|) \times 2, \text{ where } R_L = 4.7\text{kohm}, V_{DCH} = 0.4\text{V and } DV_{EE} = -5\text{V}$$

Hence, $\alpha = 0.5 + 1.32 = 1.82$ (mA)

Therefore, the total current will be 4.32mA.

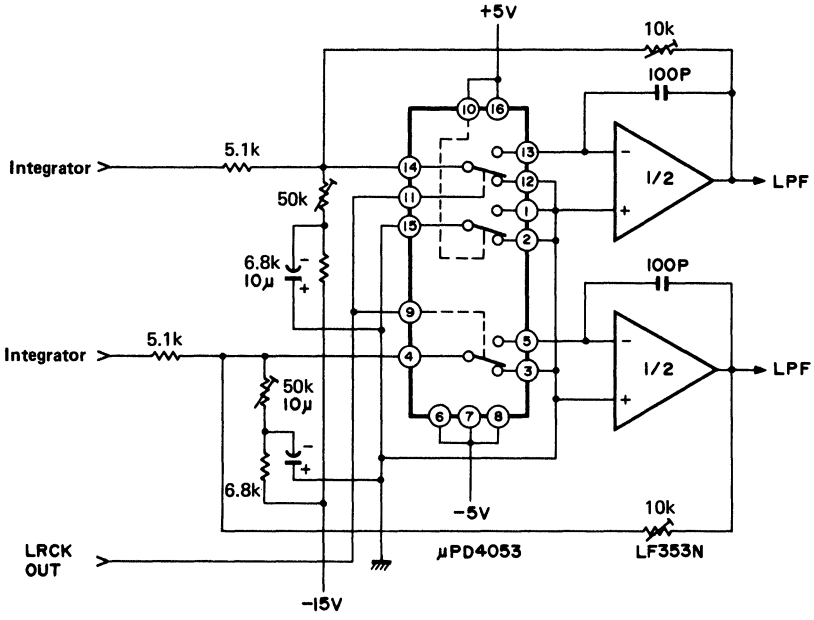
We recommend 5mA with R_L at 4.7 kΩ.

(8) System clock output pin, ON/OFF (SCKL, ON/OFF)

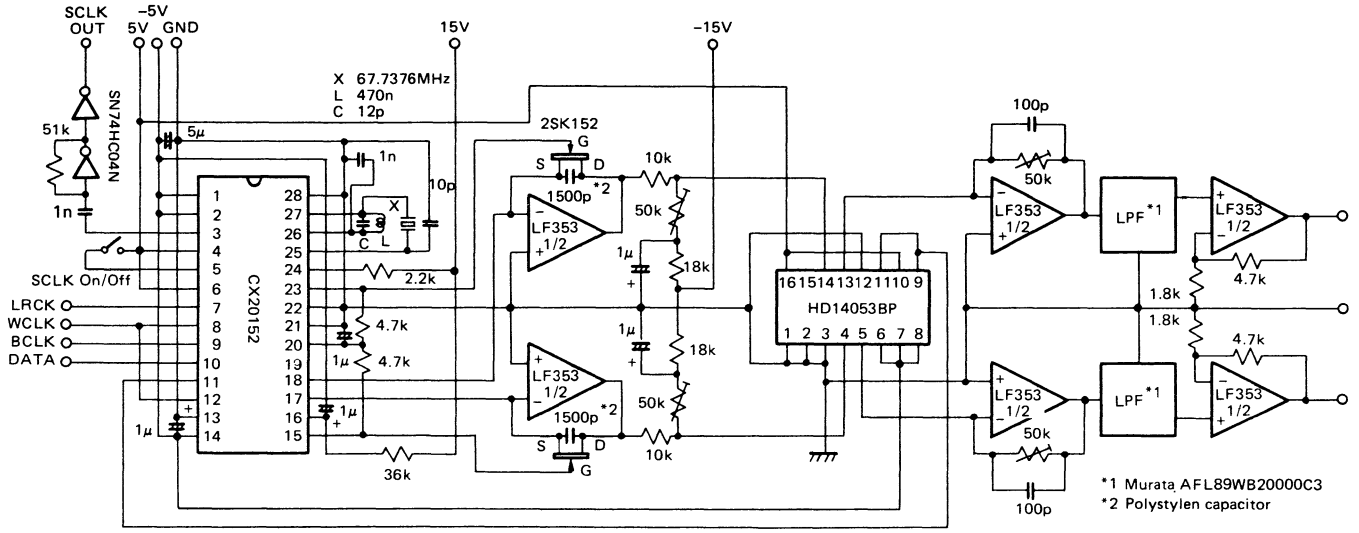
SCLK is the output pin of the 1/4 frequency divider of the oscillation circuit's master clock frequency. The frequency outputs when the ON/OFF pin is supplied with 5V (V_{CC}) and stops when the ON/OFF pin is supplied with 0V or set to open.

As its output amplitude is 2V and too low to be connected directly to a TTL or CMOS, be sure to amplify before connection.

Application Circuit for Operating Deglitcher in Sample/Hold Type

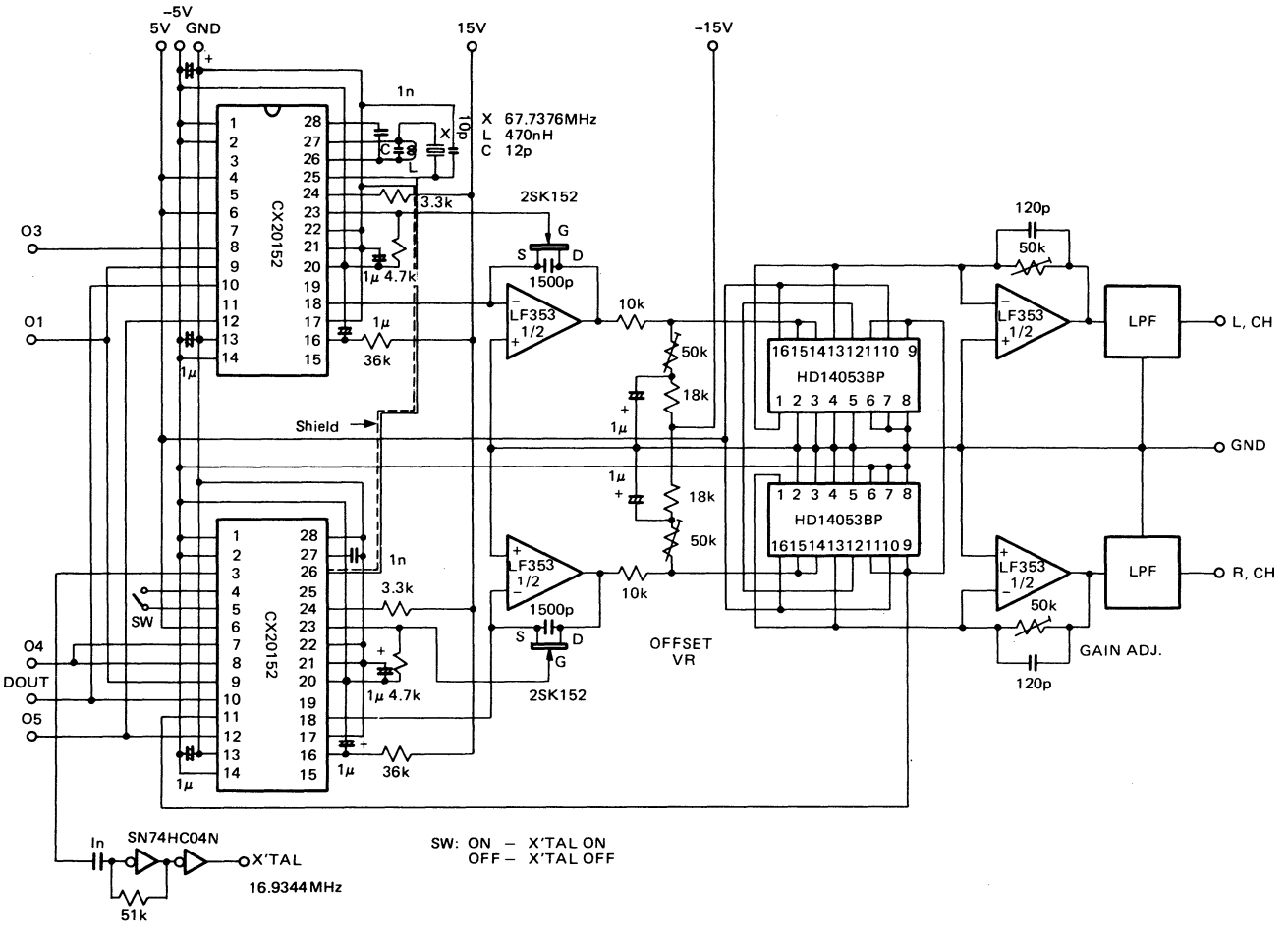


Application Circuit (Example 1)

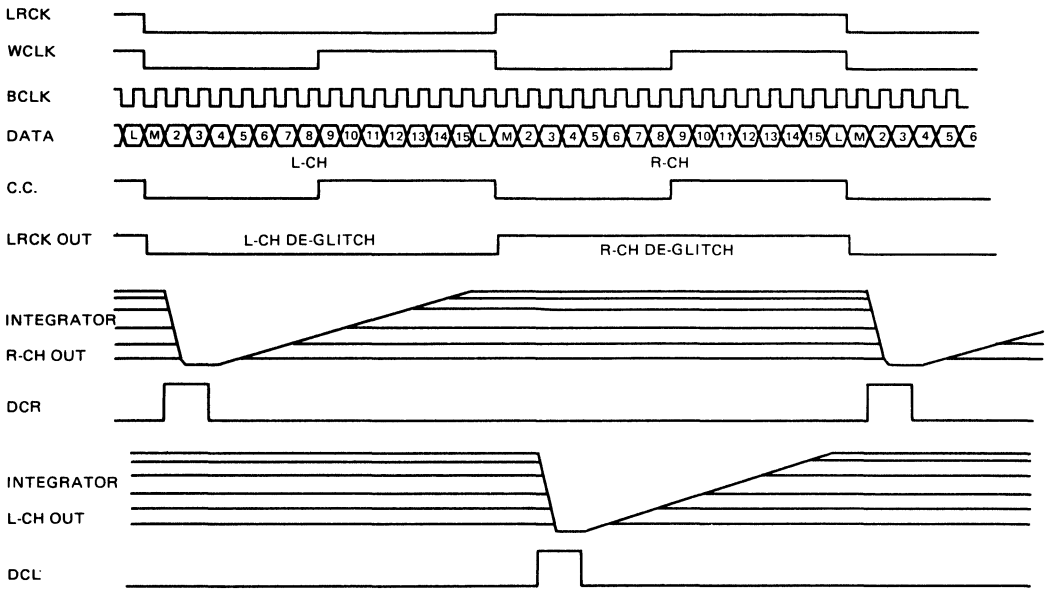


SONY

Application Circuit (Example 2)

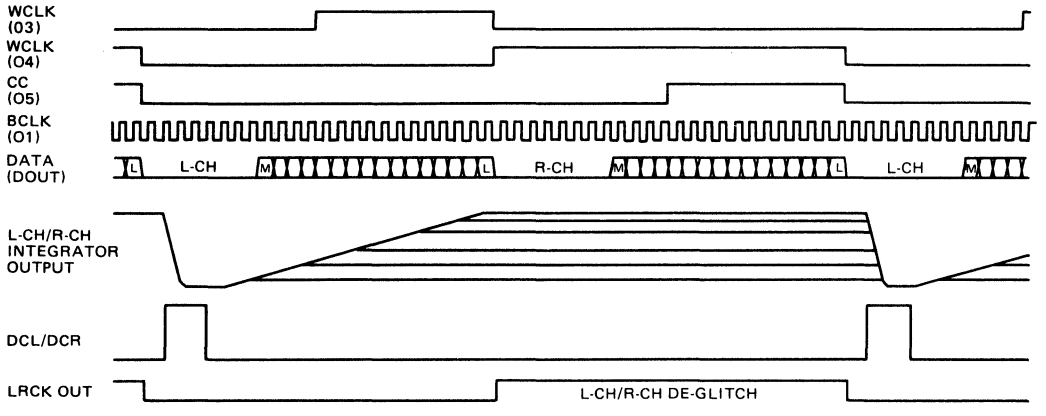


Timing Chart



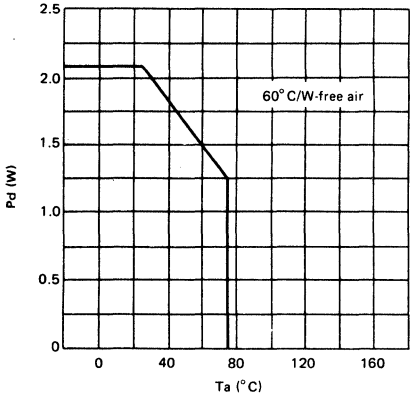
Timing Chart II

(See Application Circuit Ex. 1)

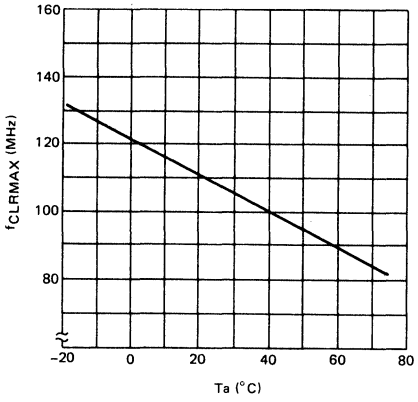


(See Application Circuit Ex. 2)

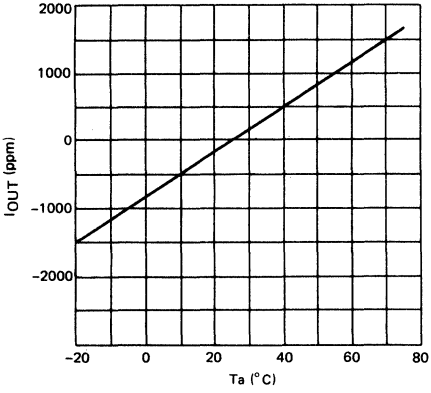
Maximum allowable power dissipation decrement curve



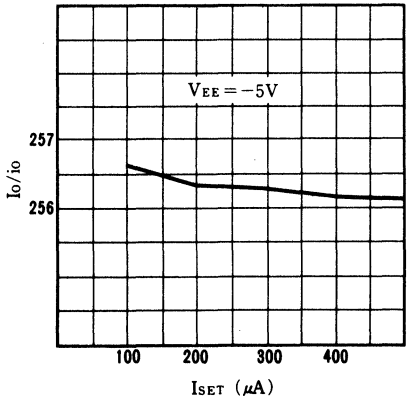
Maximum clock frequency temperature characteristics



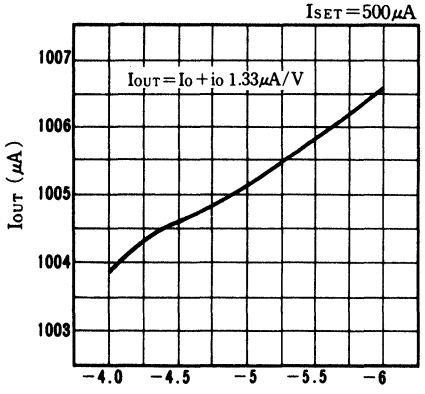
Iout temperarure characteristics (Io + io) (Both of R, Lch)



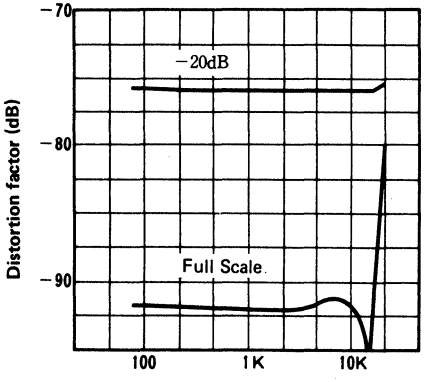
Io/io vs. ISET



Output current vs. Supply voltage (VEE)



Distortion factor



Dual 10 bit 50 KHz Multiplexed A/D + D/A

Description

The CX23010/CX23060 are the 10 bit, 50 kHz CMOS A/D, D/A Converters for Auido digital signal processing, using a coarse-fine integration technique. Both Analog to Digital and Digital to Analog Conversions are capable with selecting the mode. It can be separated into 2 blocks. One is a digital block includes

- Digital block includes
  - — A digital limiter
  - — A counter
  - — A timing generation circuit
- Analog block includes
  - — A current source
  - — An operational amplifier
  - — A comparator
  - — A multiplexer (2-channel)

Features

- A Single Power Supply: V_{DD} 5V
- Minimum number of external parts required (Around one-third compared with our current A/Ds)
- Two channel audio A/D, D/A processing (L and R Channels)
- 2's Complementary digital code is employed
- Low Power consumption (Less than 50 mW)

Structure

- Silicon Gate CMOS IC

Applications

- Digital Audio Signal Processing
- PCM Audio Processing
- Telecommunications Digitizing
- Computer Interface System

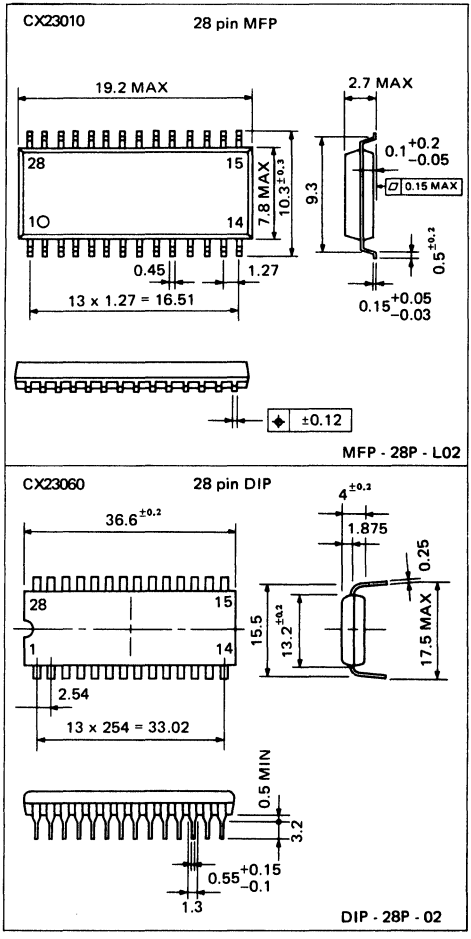
Absolute Maximum Ratings (T_a = 25°C)

• Supply voltage	V_{DD}	−0.3 to 7.0	V
• Analog input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	650 mW for CX23010	
	P_D	800 mW for CX23060	

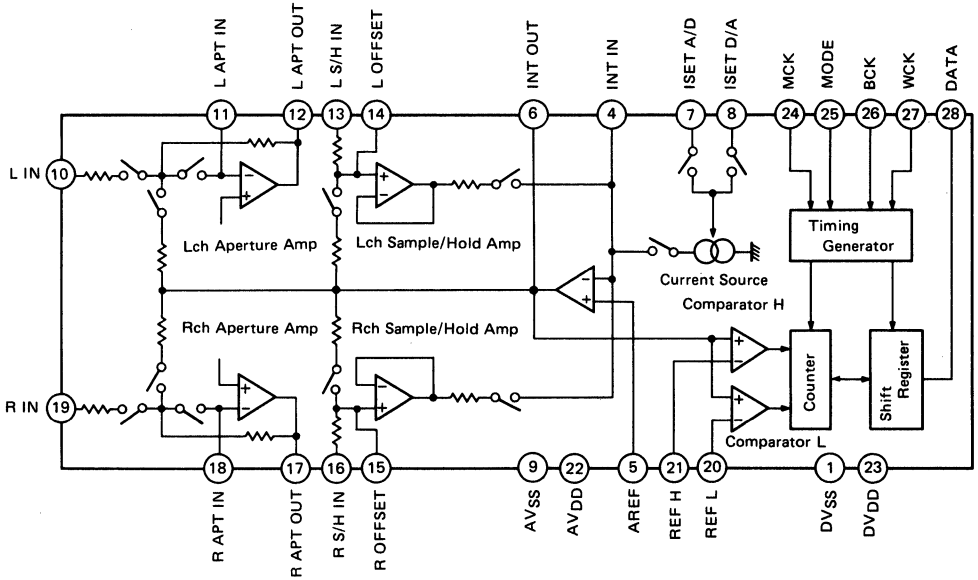
Recommended Operating Conditions

(1) AV_{DD}, DV_{DD}	4.5 to 5.5	V
(2) $AV_{DD} \leqq DV_{DD}$ + 0.5		V

Package Outline Unit: mm



Block Diagram



Pin Description

No.	Symbol	I/O	Description	DC potential
1	DV_{SS}		Digital ground pin.	
4	INT IN	I	Operational amplifier inverted input pin for integrator, and connection pin for constant current switching.	2.44 to 2.57V
5	AREF	I	Operational amplifier non-inverted input pin for integrator and aperture. Analog reference voltage V_A is input.	2.44 to 2.57V
6	INT OUT	O	Operational amplifier output pin for integrator. Connecting a capacitor between this and INT IN (Pin 4) will make an integrator.	
7	ISET A/D	I	Integrating current setting pin during A/D conversion. 5μA reference current is input.	1.2 to 1.3V
8	ISET D/A	I	Integrating current setting pin during D/A conversion. 2.8μA reference current is input.	1.1 to 1.2V
9	AV_{SS}		Analog ground pin.	
10 19	L IN R IN	I	L/R channel analog signal input pins. Less than −10dBs is proper for the maximum input level. Input impedance is about 3.5KΩ.	
11 18	L APT IN R APT IN	I	L/R channel operational amplifier inverted input pins for aperture. Input inpedance is about 4.4 k Ω.	
12 17	L APT OUT R APT OUT	O	L/R channel operational amplifier output pins for aperture. Connecting capacitors with L/R APT IN (pins 11 & 18) will make aperture amplifiers.	
13 16	L S/H IN R S/H IN	I	L/R channel sample-hold amp input pins. Input impedance is about 10 kΩ. Less than −4.6dBs is suitable for the maximum input level.	
14 15	L OFFSET R OFFSET	I	L/R channel DC offset correction pins during A/D conversion. Connecting variable resistors to the external reference power supply will correct the DC offset.	
20	REFL	I	Lower comparator comparison voltage input pin.	3.50 to 3.67V
21	REF H	I	Higher comparator comparison voltage input pin.	3.30 to 3.50V (When REF = 2.7V)
22	AV_{DD}		Analog power supply voltage pin. Latch-up prevention resistor 10 Ω is recommended.	
23	DV_{DD}		Digital power supply voltage pin.	
24	MCK	I	Master clock input pin. About 11.6 MHz ($736f_H$) is suitable for 8 mm video.	
25	MODE	I	Mode select input pin. Selectable between A/D conversion at "L" level and D/A conversion at "H" level.	
26	BCK	I	Bit clock input pin. It is used as a shift clock to transfer data by shift register. About 630 kHz ($40f_H$) is suitable for 8 mm video.	
27	WCK	I	Word clock input pin. It is used as an L/R channel identification signal of data. (R channel at "L" level and L channel at "H" level). About 31.5 kHz ($2f_H$) is proper for 8 mm video. It must be input in sync with the rise edge of BCK.	
28	DATA	I/O	Data input/output pin. When MODE is "L", LSB-leading 10-bit data is output in sync with the rise edge of BCK. When MODE is "H". LSB-leading 10-bit data is input in sync with the fall edge of BCK. The data coding is in 2's complement.	

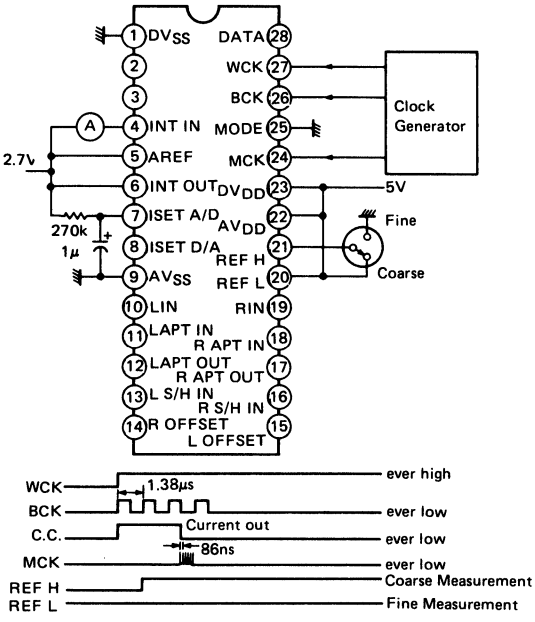
Electrical Characteristics

(Ta = 25°C AV_{DD}, DV_{DD} = 5.0V)

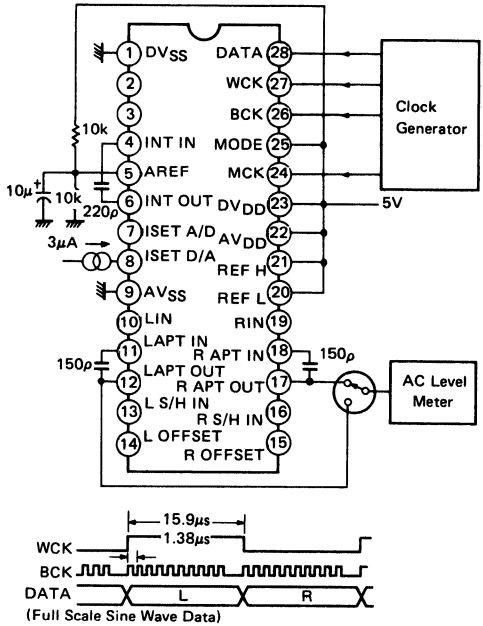
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Master Clock	Frequency	FMCK			11.6	19.0	MHz
	Input Voltage	VMCK		2.5	3.0	5.3	V_{P-P}
	Input Threshold	THMCK		1.0	1.5	2.0	V
	Duty	DMCK		30	50	70	%
Word Clock	Frequency	FMCK			31.5	50	kHz
	Input Voltage	VWCK		3.5	5.0	5.3	V_{P-P}
	Input Threshold	THWCK		2.0	2.5	3.0	V
Bit Clock	Frequency	FBCK			630	1000	kHz
	Input Voltage	VBCK		3.5	5.0	5.3	V_{P-P}
	Input Threshold	THBCK		2.0	2.5	3.0	V
Mode Select	Input Voltage	VMOD		0		5.3	V
	Input Threshold	THMODE		2.0	2.5	3.0	V
Input Voltage	Analog Signal Input	LIN / RIN				–10	dBs
	Sample Hold Input	L S/H IN / R S/H IN				–4.6	dBs
	Upper Comparator Reference Input	V_H	V_L = 3.6V	3.31	3.40	3.50	V
	Lower Comparator Reference Input	V_L		3.50	3.60	3.67	V
	Analog Reference Voltage	V_A	V_L = 3.6V	2.44	2.50	2.57	V
Input Current	A/D Integration	$I_{A/D}$	FMCK = 11.6 MHz, C = 220PF	4.5	5.0	5.6	μA
	D/A Integration	$I_{D/A}$	FMCK = 11.6 MHz, C = 220PF	2.3	2.8	3.3	μA
Output Voltage	A/D Integration	V_I	L S/H IN/R S/H IN = –4.6 dBs	1.9	2.0	2.1	V_{P-P}
	D/A Integration	V_I	FMCK = 11.6 MHz, C = 220PF 0 dB	0.9	1.1	1.3	V_{P-P}
	D/A Aperture	L APT OUT / R APT OUT	FMCK = 11.6 MHz, C = 220PF 0 dB	1.3	1.6	2.0	V_{P-P}
Gain	A/D Gain	$G_{V\ A/D}$		16.0	16.5	17.0	dB
	D/A Gain	$G_{V\ D/A}$		2.8	3.3	3.8	dB
Coarse/Fine Current ratio		Io/io	I A/D = 3.0 μA	15.5	16.0	16.5	
Resolution					10		bit
Distortion Factor		THD	– 6 dB input, 1 kHz	–52	–54	–56	dB
Conversion time	A/D	TCV A/D	FWCK = 31.5 kHz			12.45	μs
	D/A	TCV D/A	FWCK = 31.5 kHz			8.28	μs
Frequency Response	A/D*	RESP A/D	Operating input frequency $\frac{FWCK}{2}$, 0dB at 1kHz		0		dB
	D/A*	RESP D/A	Operating input frequency $\frac{FWCK}{2}$, 0dB at 1kHz		–3.6		dB
Supply Current		I_D (total)			9	10	mA

*Note) Assuming the frequency response is 0 dB when Analog Input Freq. = 1 kHz

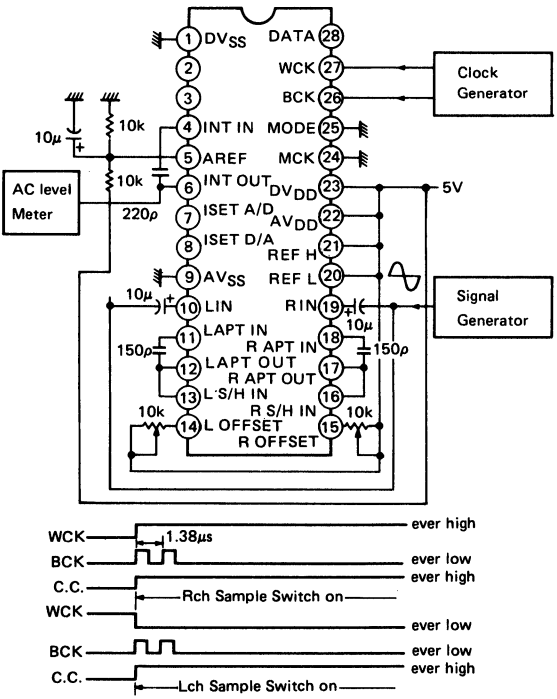
Constant Current Ratio Test Circuit

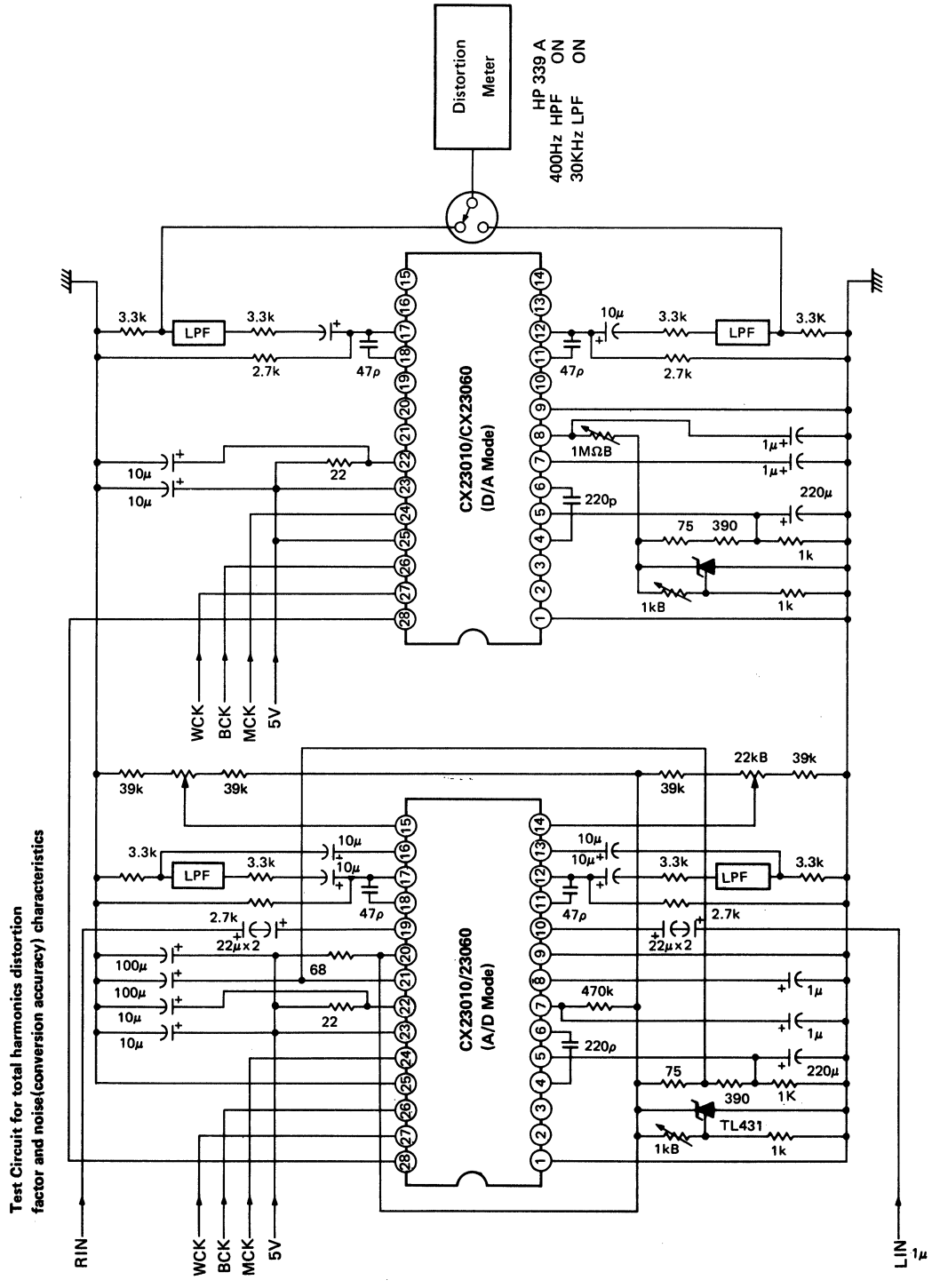


D/A conversion mode/Operational amplifier/ Amplification Gain Test Circuit



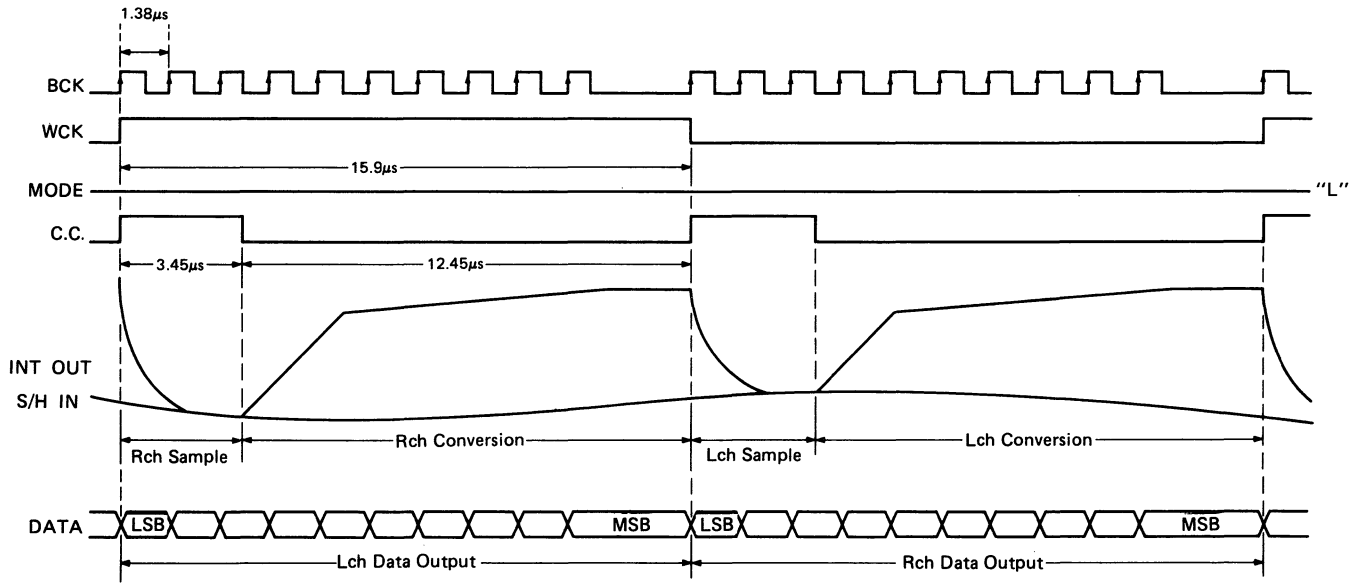
A/D conversion mode/Operational amplifier/ Amplification Gain Test Circuit





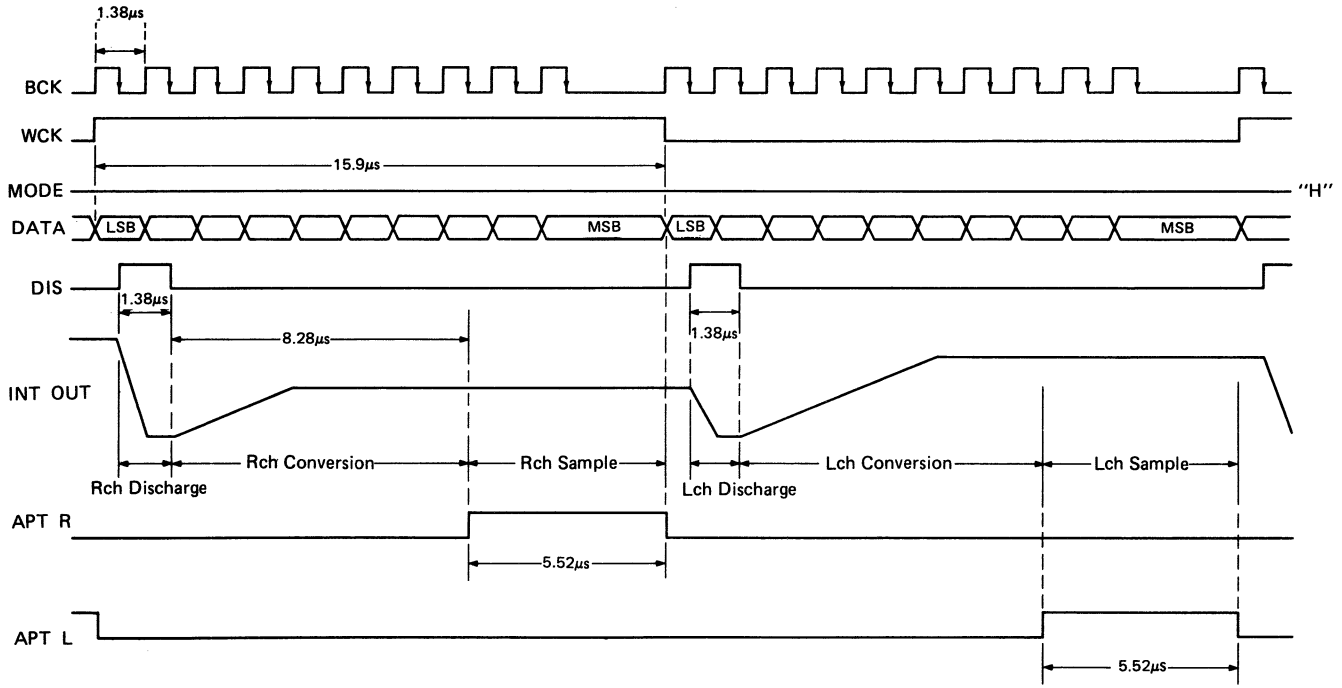
Test Circuit for total harmonics distortion factor and noise(conversion accuracy) characteristics

Timing Chart of A/D Conversion Mode



When Mode Select of the CX23010/CX23060 is set to "L", A/D conversion mode is selected. When BCK (46fH, 723.776kHz for NTSC) and WCK (2fH, 31.46853kHz for NTSC) are input from CX23012(AD/DA interface LSI) in this mode, C.C (Convert Command) is generated internally in CX23010/CX23060. While this C.C is at "H" level, the analog signal input is sampled; the A/D conversion is executed during "L" level. The sampling and conversion operations are performed in time division for each of the R and L channel analog signals. The converted final data is output serially with the LSB data leading in sync with the rise edge of BCK when the C.C becomes "H" level again.

Timing Chart of D/A Conversion Mode



When Mode Select of the CX23010/CX23060 is set to "H", D/A conversion mode is selected. When BCK (46fH, 723.776kHz for NTSC) and WCK (2fH, 31.4685kHz for NTSC) are input from CX23012 (AD/DA interface LSI) in this mode, DIS (Discharge clock) and APT R/L (Aperture clock) are generated internally in the CX23010/CX23060. At the same time, the serial data input with the LSB leading is stored in sync with the fall edge of BCK. After DIS has discharged at "H" level the integrating charge resulting from the previous D/A conversion, D/A conversion starts when DIS goes to "L" level. The discharge and conversion operations are performed in time division for each of the R and L channel data inputs. The final integrated output after conversion is sampled while APT R/L is at "H" and held at "L" level.

Description of Function

The CX23010/CX23060 are one-chip 10 bit A/D, D/A converter provided with every function required in A/D and D/A conversion. When combined with CX23011 (for modulation, demodulation and error correction), CX23012 (for 8-10 bits compression and expansion) and CX20099 (analog noise reduction), they are used in the PCM processor for 8 mm video.

1 A/D Conversion

- **Selection of operational mode**

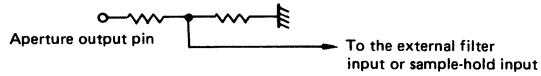
A/D conversion mode is selected by setting the mode select input (MODE) to "L".

- **Analog block operation and gain**

The input signal applied to the analog signal input pins (L_{IN}, R_{IN}) is amplified about 12.5 dB by the aperture amp and output to the aperture output pins (L APT OUT, R APT OUT). After component out of band area is removed from the output signal by the external attenuation filter, it is added to the sample-hold input pins (L S/H IN, R S/H IN) and output to the integrating output pin (INT OUT) after amplification of about 4dB by the sample-hold amplifier.

This gain is obtained assuming that the external filter's insertion loss is −7.3dB. Therefore, the overall gain will be 9.2dB when the A/D conversion filter is included.

When the external filter's insertion loss is different from the above value or its insertion position is different, the aperture amp gain may be too high. In such case, it is effective to divide the aperture output as follows:



When the divided output is supplied directly to the sample-hold input pin, a division resistance value of 3.3 kΩ is suitable for use.

- **Digital block operation and clock frequency**

The Convert Command (C.C.) is generated internally by inputting the wordclock (WCK) and bit clock (BCK). While C.C. is at "H", the analog signal added to the sample-hold amp is sampled and while C.C. is at "L", the constant current weighted with inverse polarity against the input signal is integrated for conversion. The 10 bit data is performed by calculating the integrating time of the coarse constant current and fine constant current separately using a counter. The data is loaded in the shift register when C.C. becomes "H" again and is output serially with LSB leading in sync with the rise edge of BCK. The data is coded in 2's complement.

The master clock frequency (FMCK) required in excuting a full-scale A/D conversion in the CX23010/CX23060 is obtained from the following equation.

$$FMCK \geqq \left\{ \frac{(TWCK/2) - 2.5TBCK}{69} \right\}^{-1}$$

TWCK = word clock frequency.
TBCK = bit clock frequency.

When combining with CX23012, a master clock of more than about 6 MHz is required, as TWCK is 31.7μs and TBCK is 1.38μs. With the CX23010/CX23060, a master clock of about 11.6MHz will be suitable as the margin is about double.

As the conversion operation is required to be in sync with the master clock in the CX23010/CX23060, the master clock, word clock and bit clock must be synchronous each other. They don't have to be in phase, however.

• **Integrating current**

The integrating current value $I_{A/D}$ required to perform a full-scale A/D conversion in the CX23010/CX23060 is obtained by the following equation.

$$I_{A/D} = \frac{C \cdot V_I}{1023\tau_O}$$

where C = Integral capacity,
V_I = Integral output voltage and
τ_O = Master clock cycle

Supposing C=220$_p$F, V_I=2$V_{p\text{-}p}$ and τ_O=86ns (FMCK= 11.6MHz), a desirable integrating current value is about 5μA. The integrating current setting is done by applying an external constant current to the integrating current setting pin (ISET A/D) during A/D conversion.
When a constant current is applied through a setting resistor $R_{A/D}$ from an external reference voltage, this resistor value is calculated from the following equation.

$$R_{A/D} = \frac{V_{REF} - 1.25V}{5\mu A}$$

Supposing V_{REF}=3.6V, a setting resistor value will be 470 KΩ. Using a resistor with tolerance of 1%, variation of the playback output level will be less than ±1.0dB. A bypass capacitor of more than 1μF should be used for the integrating current setting pin to avoid stray noise to the pin.

• **Comparison voltage**

Switching between the upper conversion and lower conversion is performed by the integrating output surpassing the comparison voltages, V_H and V_L, in the next stage comparator. The two comparison voltages have following relationship.

$$\frac{67\, I_{A/D} \cdot \tau_O}{C} \leqq V_L - V_H \leqq \frac{131\, I_{A/D} \cdot \tau_O}{C}$$

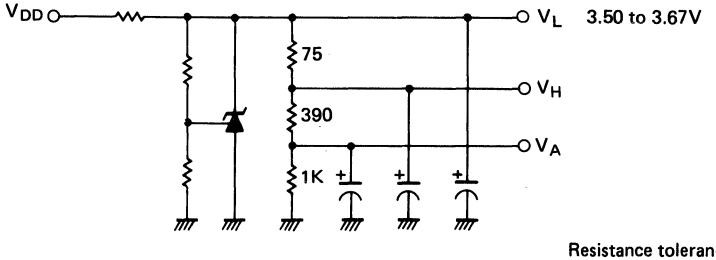
As the lower comparison voltage V_L needs a small ripple particularly, it is suggested to use a reference voltage made by th external reference power supply. Set the reference voltage at 3.50 V to 3.67 V (3.60V typ.). The upper comparison voltage V_H is made from resistance division as the following diagram in this reference voltage.

• **Analog reference voltage**

As the CX23010/CX23060 are operated with a single 5V power supply, non-inverted input of the internal operational amp must be biased to around half of the power supply. The analog reference voltage V_A gives this bias and it can be divided from the comparator's lower comparison voltage V_L. The ripple filter capacitor to suppress time variation of V_A is suggested to have about 220μF.

• **Offset adjustment**

As 8mm video uses a non-linear quantization by 10 bit, 8 bit compression/expansion, compatibility is affected when a DC offset component is included in the A/D converter data output. To correct this DC offset, the integrating output's center voltage must be shifted by applying an offset current from the offset input pins (L OFFSET, R OFFSET). As it is desirable to keep the offset voltage constant regardless of the power supply voltage changes, the offset voltage should be applied via an offset resistor from the external reference voltage (3.50V to 3.67V) in this case in adjusting the DC offset, set the offset resistor value so that the data output will be "0000000000" when the center voltage is added to the sample-hold input. The lowest bits (LSB–2SB) of the data output are sometimes not determined due to an analog drift or stray noise, but in practice this is not matter.



Resistance tolerance of 5% is recommended.

2. D/A Conversion Operation

• Selection of operation mode

By setting the mode select input (MODE) to "H", the D/A conversion mode is selected.

• Digital block operation and clock frequency

Discharge clock (DIS) and aperture clock are generated internally, by inputting word clock (WCK) and bit clock (BVCK). The serial data input with LSB leading is stored in the shift register in sync with the falling edge of bit clock and set in the counter just before the rise and falling of word clock. When the discharge clock becomes "L", the counter starts counting, beginning from the value set in it and at the same time a constant current weighted corresponding to data is output. When the counter outputs the carry signal, the counting and constant current output stop. The master clock frequency required to perform a fullscale D/A conversion in CX23010/CX23060 obtained from the following equation.

$$FMCK \geqq \left\{\frac{6 \cdot TBCK}{37}\right\}^{-1}$$

When combined with CX23012, a master clock of more than about 4.5 MHz is required since TBCK=1.38μs.

• Analog block operation and gain

The integrating charge resulting from the previous conversion will be discharged while the discharge clock is "H", the integrating output potential is initialized to the analog reference voltage (V_A). When the discharge clock goes to "L", D/A conversion operation is executed by integrating the constant current output. Which the constant current output stops, integrating also stops and the pin voltage of the integrated capacitor at this moment is the D/A converted value. The integrated output held in the capacitor is output, after being gained by about 3.3 dB from the aperture amp, to the aperture output pins (L APT OUT, R APT OUT). Output signal's out-of-band components are removed by an external interpolation filter. The aperture amp gain is set supposing the external filter's insertion loss at −7.3 dB. The gain is not varied externally unlike A/D conversion mode.

• Integrating current

With the CX23010/CX23060, relationship between the integrating output V_I and integrating current $I_{D/A}$ is determined from the following equation.

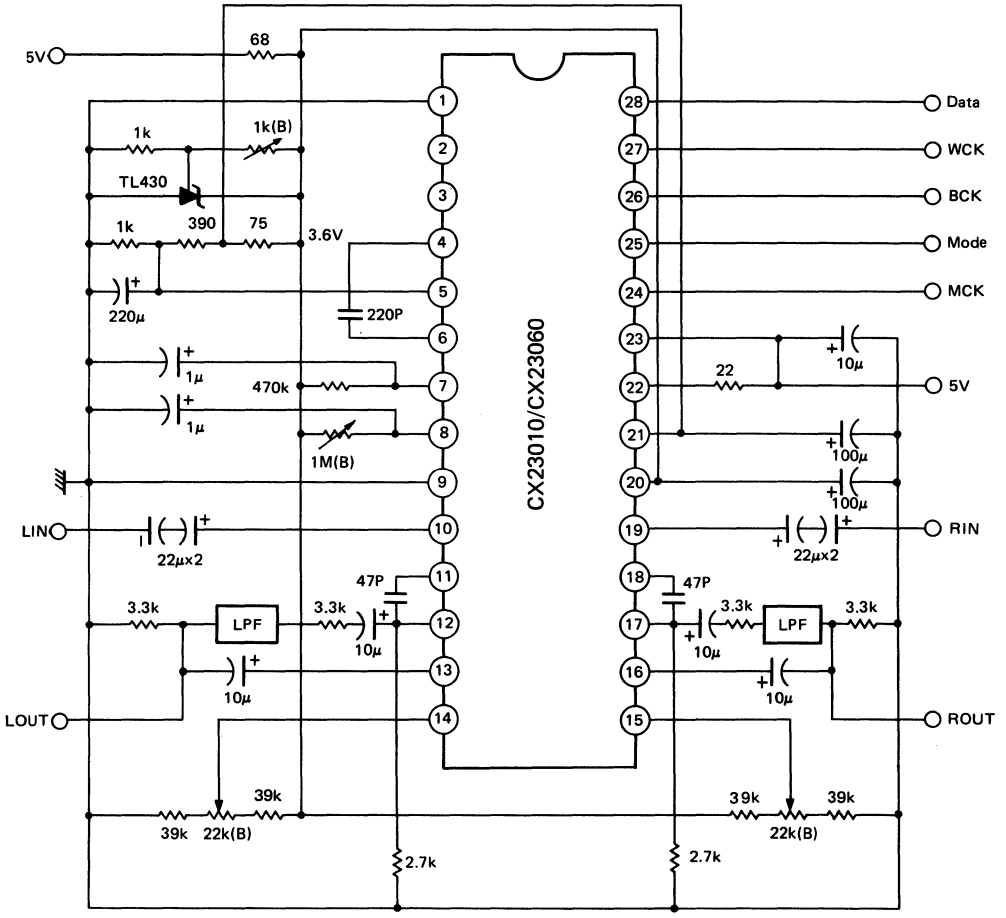
$$I_{D/A} = \frac{C \cdot V_I}{1023\tau o}$$

Supposing C=220$_p$F, V_I=1.1$V_{p\text{-}p}$ and τo=86ns, a proper integrating current will be about 2.8μA. If the external filter loss is supposed to be −7.3dB, −10dBs will be obtained as the filter output level Setting of the integrating current is executed by applying a constant current externally to the integrating current setting pin (ISET D/A) during D/A conversion. When constant current is applied through a setting resistor R_{DA} from the external reference voltage, the resistor value is determined from the following equation.

$$R_{D/A} = \frac{V_{REF} - 1.15V}{2.8\mu A}$$

Supposing V_{REF}=3.6V, the setting resistor will be 880KΩ Using a resistor of 1% tolerance, the playback output level variation will be held within ±1.5dB. Applying a bypass capacitor of more than 1 μF to the integrating current setting pin is recommended to avoid a stray noise to it.

Typical Application Circuit



Selection of Parts to be Used

(1) For an integrating capacitor between Pin 4 and Pin 6, use a type with little dielectric absorption. (e.g. styrene, etc.)

(2) Adjust the semi-fixed resistor 1KB so that the reference voltage generated from the reference voltage IC (TI's TL430 or TL431) is 3.6V.

(3) Accuracy tolerance of the three divided resistors, 75Ω, 390Ω and 1KΩ, supplying voltage to Pins 5,20, and 21 is 5%. Voltages of each pin are 2.5V for Pin 5, 3.6V for Pin 20 and 3.4V for Pin 21 approximately.

(4) We recommend 1% accuracy tolerance of 470KΩ for the integrating current setting resistor to be connected to Pin 7, which will give a recording level during A/D conversion.

Adjustment Methods

(1) In adjustment of the play back level during D/A conversion, use the 1 Mega-Ω B semi-fixed resistor connected to Pin 8. Input to Pin 28 a full-scale level digital sine wave data (1 kHz) and adjust the semi-fixed resistor so the playback level of L OUT and R OUT becomes −10dBs (0.245Vrms). The maximum level deviation between L OUT and R OUT channels is ±0.3dB.

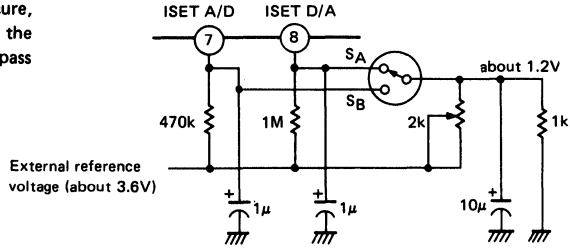
(2) Adjustment of the recording level during A/D conversion is not shown in separate illustration but the playback level of the reference playback DAC (a separate DAC must be prepared adjusted to have −10dBs playback output level when full-scale data is input as in (1) above) must have −10dBs when the analog input level fed to Pins 10 and 19 is set at −10dBs (0.245Vrms). In practice, however, it is effective to vary the analog input level of Pins 10 and 19 properly or provide a level adjustment amp for Pins 13 and 16, since the level ratio of 1 to 1 between an analog input and digital output is unobtainable due to variation in the ADC conversion gain.

(3) In the offset adjustment during A/D conversion, use the 22KB semi-fixed resistor out of the three divided resistors 39K, 22KB and 10K from the reference voltage 3.6V. In practice, adjust the 22KB so the data output of Pin 28 becomes "0000000000" when the analog inputs of L IN and R IN are shorted. At this time the lowest two or three bits may be affected due to stray noise but they pose practically no problem.

Application

• Mode switching in after recording

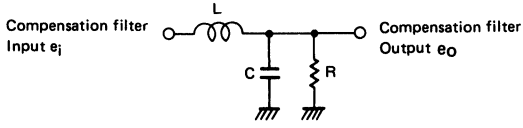
With the CX23010/CX23060, a bypass capacitor of more than 1 μF is recommended to prevent degradation of S/N ratio due to stray noise from the integrating current setting pin. It takes 0.3–0.4 sec (when a 1μF bypass capacitor is used) before the integrating current becomes stable and the data during this period becomes insecure, generating a click noise in playback. To minimize the table period, it is most effective to precharge the bypass capacitor in the following circuit.



Note) Select S_A for A/D conversion.
Select S_B for D/A conversion.

• Frequency characteristics

The CX23010/CX23060 frequency characteristics during A/D conversion is determined by an input attenuation filter. Meanwhile the frequency characteristics during D/A conversion is determined by an aperture effect and output interpolation filter. With the CX23010/CX23060, degradation of high area frequency characteristics due to the aperture effect is unavoidable. This is because a sample-hold aperture circuit is used to obtain −10dBs as the interpolation filter output level during full-scale D/A conversion. To compensate the degradated characteristics, add a compensation filter, shown below, after the interpolation filter passed.



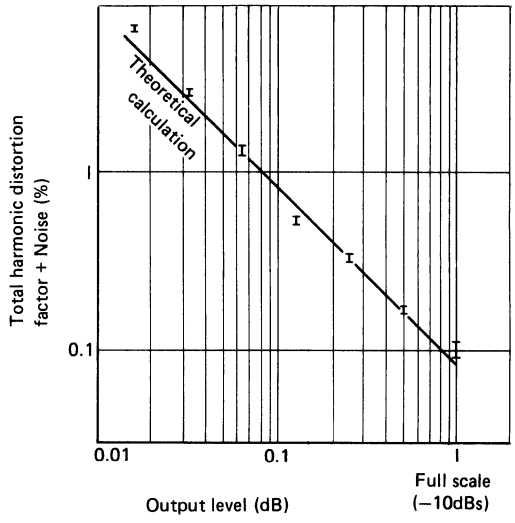
Note) $$\frac{e_O}{e_i} = \frac{1}{\sqrt{1-2(1-2a^2)x^2+x^4}}$$

where $x = \omega/\omega_c$ $L/R = 2a/\omega_c$ $LC = (1/\omega_c)^2$

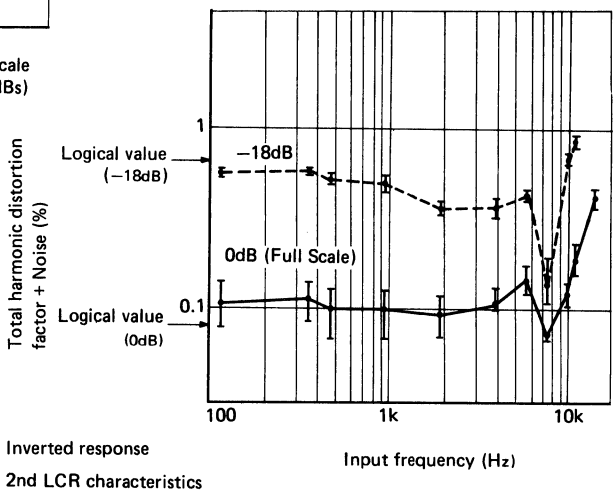
when f_c = 25kHz, L = 2.2 mH, C = 0.015μF and R = 1 kΩ

With this compensation filter, the total recording/playback frequency characteristics is determined only by an external filter. With the CX23010/CX23060, note the pass band ripple is magnified double, whereas double attenuation is obtained for the stop and suppress bands since the input attenuation filter and the output interpolation filter are used in common.

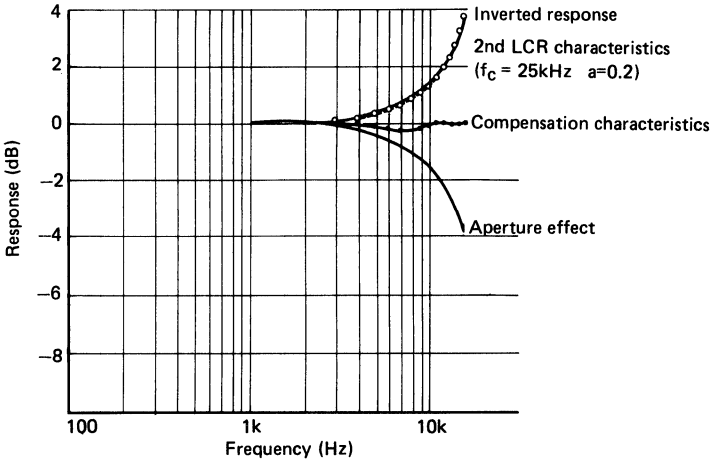
Total harmonic distortion factor + Noise vs. Output level (D/A conversion mode)



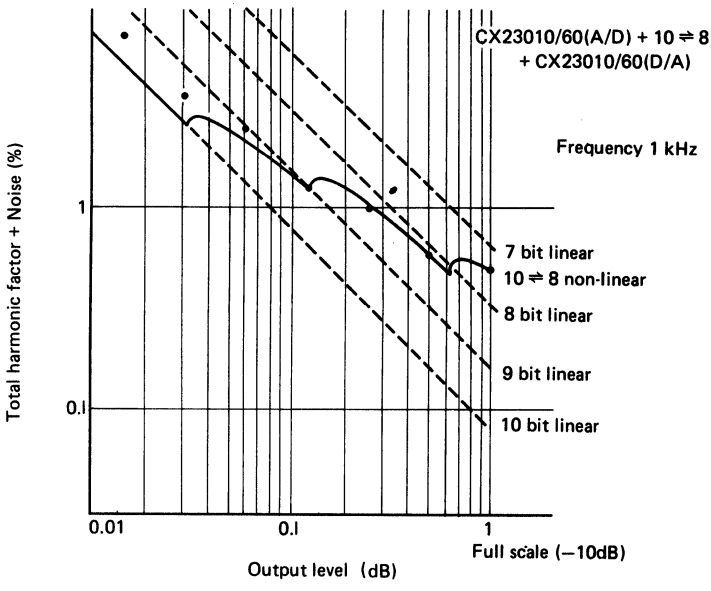
Total harmonic distortion factor + Noise vs. In frequency (D/A conversion mode)



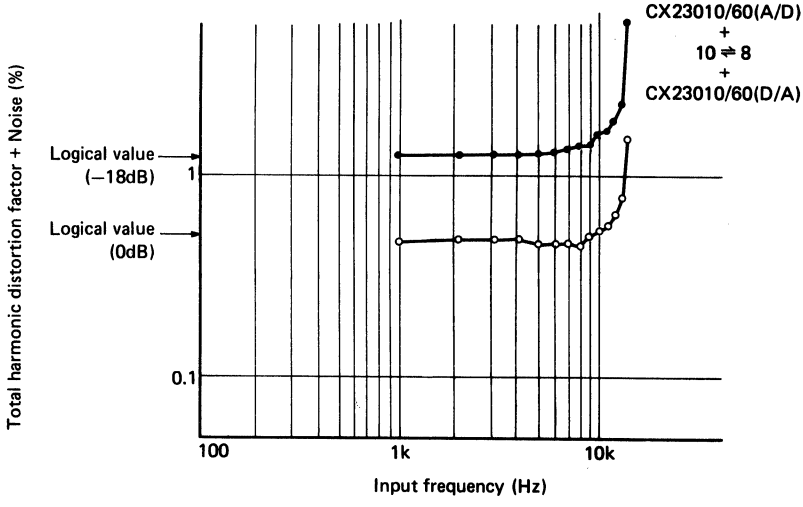
Compensation characteristics of aperture effect



Total harmonic distortion factor + Noise vs. Output level (A/D conversion mode)



Total harmonic distortion factor + Noise vs. Input frequency (A/D conversion mode)



A/D,D/A Converters Video

2) A/D, D/A Converters — Video —

Type	Function	Page
CX20051A	10bit 30MHz D/A Converter	105
CX20052A	8bit 20MHz Sub-ranging A/D Converter	116
CX20116/U CXA1066K/UK	8bit 100MHz Flash A/D Converter	125
CX20201A-1/-2/-3 CX20202A-1/-2/-3	10/ 9/ 8bit 160MHz D/A Converter	132
CX20206	8bit 35MHz RGB 3-channel D/A Converter	144
CX20220A-1/-2	10/ 9bit 20MHz Sub-ranging A/D Converter	160
CXA1008P/1009P	High-speed Sample and Hold Amplifier	174
CXA1016P/K/UK CXA1056P/K/UK	8bit 30/50MHz Flash A/D Converter	186
CXA1096P	8bit 20MHz Flash A/D Converter (P)	196
CXA1106P	8bit 35MHz High-speed D/A Converter (P)	203
BX-1300	8bit 20MHz A/D Converter Module	208

(P) : Preliminary

10 bit 30 MHz D/A Converter

Description

CX20051A is 10 bit, 30 MHz D/A Converter, designed for a video signal processing. The broadcasting application will require the fairly high resolution for D/A. CX20051A is suitable for the high definition TV application, too.

The external resistor can control the voltage output range of the D/A. The CX20051A requires −5V single power supply, the ECL digital inputs, and the differencial ECL clocks, to operate.

Features

- Maximum conversion frequency 30 MHz
- High resolution 10 bit
- Low power consumption 550 mW
- −5V single power supply
- Clock input and digital input are in ECL level

Structure

Bipolar Silicon Monolithic IC.

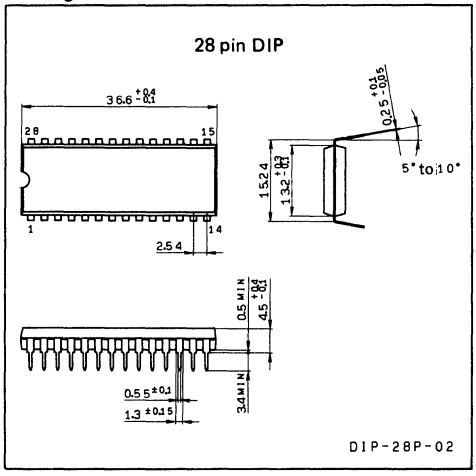
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	−12	V
• Digital input voltage	V_{IN}	V_{EE} to 0	V
• Operating temperature	Topr	−10 to +70	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation		1.47	W

Recommended Operating Conditions

• Supply voltage	V_{EE}	−5.0 ± 0.25	V
• Digital input voltage	V_{IH}	−0.89 ± 0.15	V
	V_{IL}	−1.75 ± 0.15	V
• Dynamic range	V_O	−1.5 to −0.5	V
• Bias current	I_{SET}	1.0 ± 0.5	mA

Package Outline Unit: mm



Block Diagram and Pin Connection

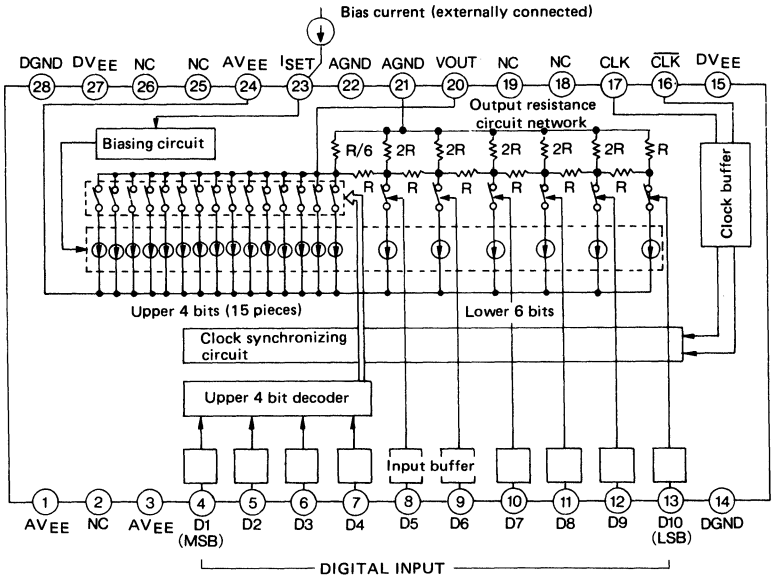
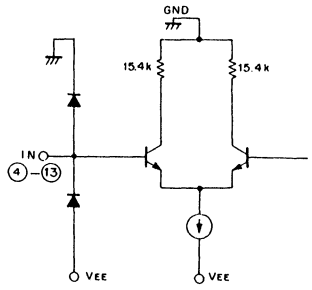
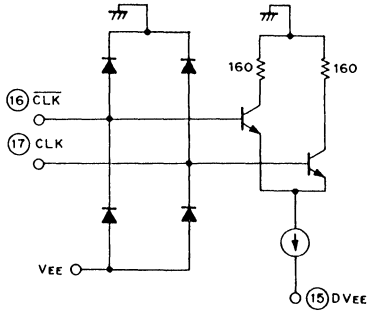
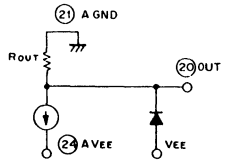
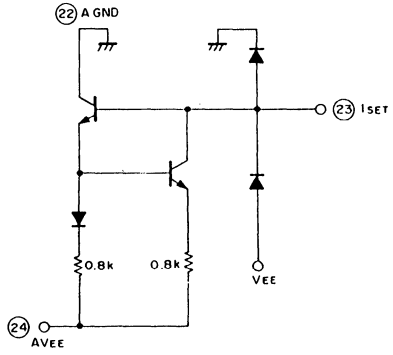


Fig. 1

Pin Description

No.	Symbol	Description	Equivalent circuit
1	A VEE	Analog VEE power supply (−5V)	
2	NC	Non-connection	
3	A VEE	Analog VEE power supply (−5V)	
4	NSB	10-bit digital input (MSB: Uppermost order, LSB: Lower most order)	
5	BIT2		
6	BIT3		
7	BIT4		
8	BIT5		
9	BIT6		
10	BIT7		
11	BIT8		
12	BIT9		
13	LSB		
14	D GND	Digital GND	
15	D VEE	Digital VEE power supply (−5V)	

No.	Symbol	Description	Equivalent circuit
16	$\overline{CLK}$	Clock bar input	
17	CLK	Clock input	
18	NC	Non-connection	
19	NC		
20	OUT	D/A output	
21	A GND	Analog GND Directly connected to the output resistance circuit network (ROUT)	
22	A GND	Analog GND For analog circuit system other than the output resistance circuit network	
23	ISET	Dynamic range adjusting pin	
24	A VEE	Analog VEE power supply (−5V)	
25	NC	Non-connection	
26	NC		
27	D VEE	Digital VEE power supply (−5V)	
28	D GND	Digital GND	

Electrical Characteristics

(Ta=25°C AGND=DGND=0V, AV_{EE}=DV_{EE}=−5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential linearity	D.L.	*1	−0.8	0	0.8	LSB
Maximum operating clock frequency	f_{MAX}	*2	30			MHz
Differential gain	D.G.	NTSC 40IRE mod. ramp f_{CLK}=14.3 MHz		0.7		%
Differential phase	D.P.			0.2		deg
Circuit current	I_{EE}		88	110	132	mA
Output impedance	R_{OUT}		52	62	72	Ω
Input current	I_{IH}	Measured in the high level input voltage of the individual pins 4 to 13	1	3	10	μA
Input current	I_{IL}	Measured in the low level input voltage of the individual pins 4 to 13	0	20	300	nA

Note) As for the test circuit, see Fig. 2a to 2d.

*1 Input signal is digital ramp with 1 MHz clock.
Glitches are not the subject of the measurement.

*2 The maximum operating clock frequency which shows no bit error. Input signal is digital ramp.
Glitches are not the subject of the measurement.

Electrical Characteristics Test Circuit

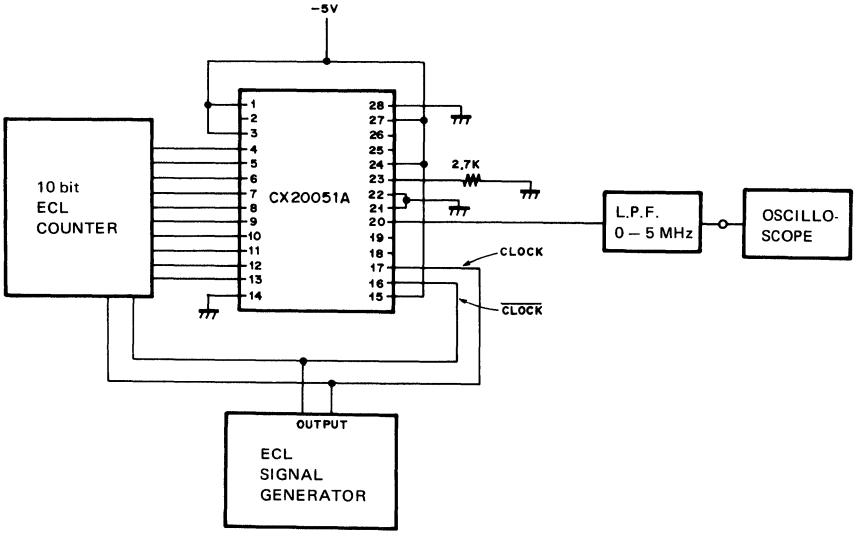


Fig. 2a Block diagram of differential linearity and maximum operating frequency test circuit

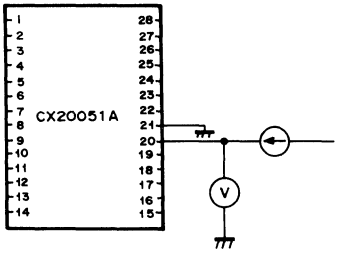


Fig. 2b Block diagram of output impedance test circuit

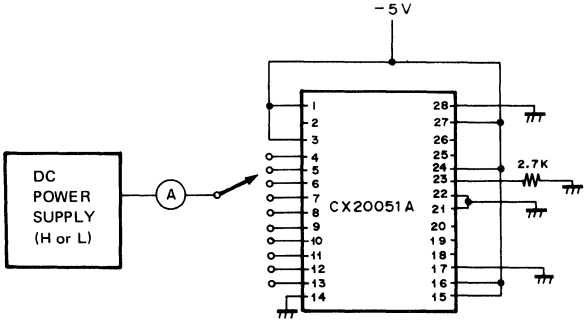


Fig. 2c Block diagram of input current test circuit

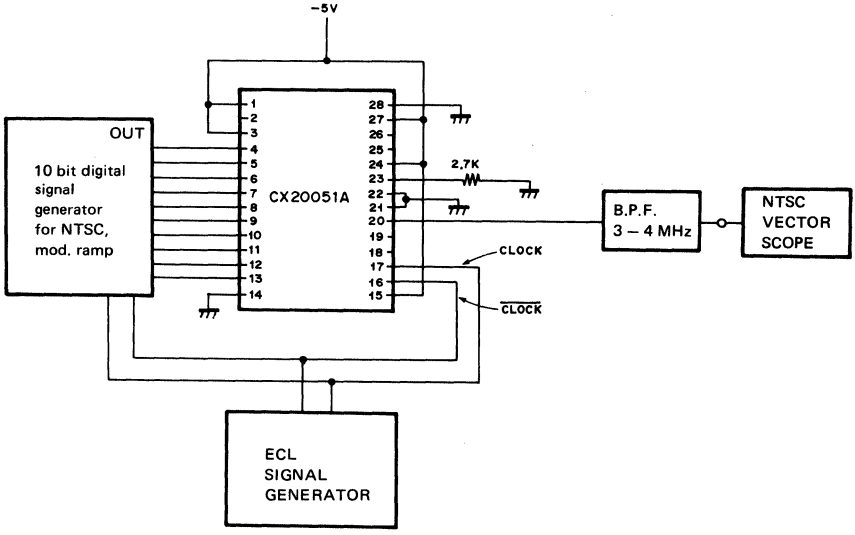


Fig. 2d Block diagram of DG and DP test circuit

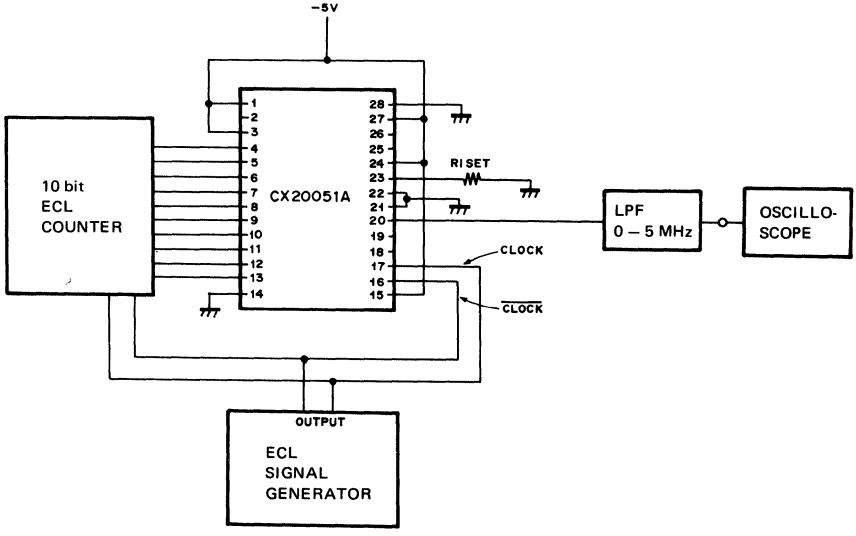


Fig. 2e Block diagram of dynamic range test circuit

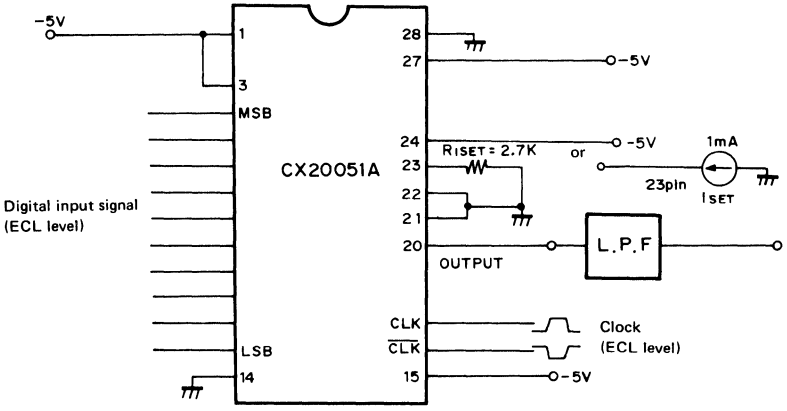


Fig. 3 Typical circuit connection

When changing the dynamic range of the output, change the value of R or the constant current supply value when a constant current supply is inserted in place of R. Both input and clock are in ECL level. Regarding the clock waveform, see the Note on Application.

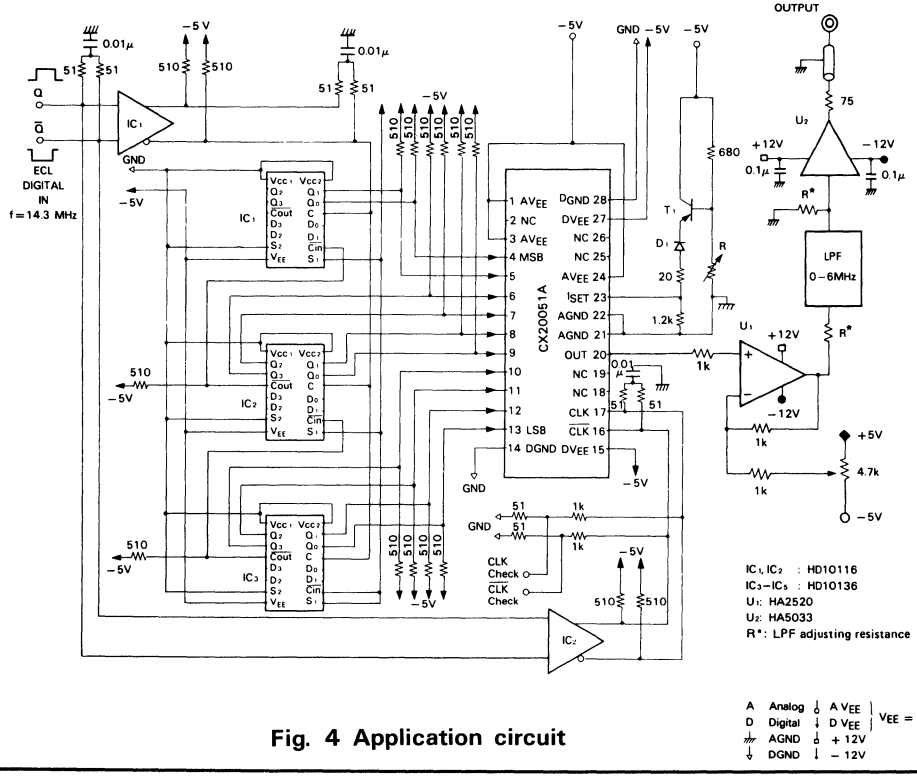


Fig. 4 Application circuit

Note on Application

(1) Applying clocks

(a) To pins 16 and 17, clock signals denoted as $\overline{\text{CLOCK}}$ and CLOCK are to be fed respectively. Both of their levels are ECL compatible levels.

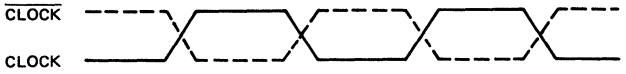


Fig. 5a CLOCK and $\overline{\text{CLOCK}}$ waveforms

(b) Alternatively single-end method is usable to apply clock signal to the device. A clock signal of ECL level is to be fed to one of pin 16 or pin 17, with the other pin fixed to the ECL threshold level.

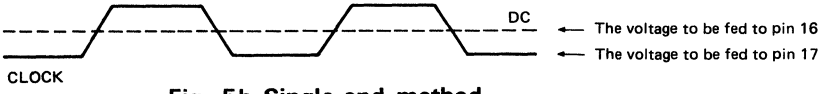
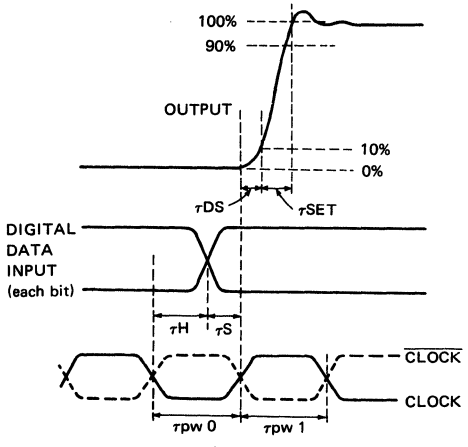


Fig. 5b Single-end method

(2) Timing chart

The timing between the CLOCK signal and 10 bit Digital Data Input signal is shown in the diagram below.



(Recommended operating condition)

$\tau H > 2$ ns

$\tau S > 10$ ns

$\tau PW0 = \tau PW > 20$ ns

The typical values of τDS and τSET under the above-mentioned condition are

$\tau DS \approx 7$ ns

$\tau SET \approx 4$ ns

for Z_L (load resistance) > 10 kΩ

Fig. 5c Timing chart

(3) Dynamic range (I_{SET} pin, pin 23)

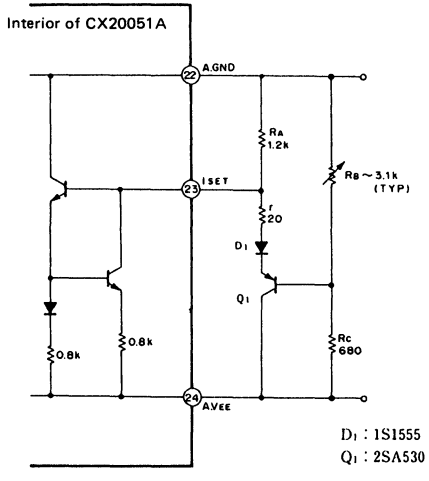
Dynamic range can be determined by connecting an external resistor (R_{ISET}) between the I_{SET} pin (pin 23) and the A GND pin (pin 22), or by applying a current source (I_{SET}) to the I_{SET} pin (pin 23). Typical values to obtain 1 V of dynamic range are 2.7 kΩ and 1 mA, for R_{ISET} and I_{SET} respectively (for a load resistance $Z_L > 10$ kΩ). (See the Dynamic range vs. R_{ISET} on page 11.)

(4) Input coding

STEPS	DIGITAL INPUT	ANALOG OUTPUT	
		CASE ①	CASE ②
0000	MSB1111111111LSB	−0.003V	−0.003V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
0511	1000000000	−0.4825V	−0.503V
0512	0111111111	−0.4835V	−0.504V
0513	0111111110	−0.4844V	−0.505V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
1023	0000000000	−0.963V	−1.003V

CASE ①: R_{ISET}=2.7 kΩ
(Output voltage is typical value.)
CASE ②: R_{ISET} is adjusted to obtain 1.000V full scale of analog output voltage.

(5) Temperature fluctuation compensation method of D/A output voltage dynamic range
When the temperature fluctuation of the outout voltage dynamic range poses a problem, a simple temperature compensation can be performed by adding a simple circuit externally.
Connecting diagram of the external circuit for temperature compensation is shown below. In this way, the temperature fluctuation may be limited to within ±150 ppm/°C.



(6) When the analog output level is at full scale 1 Vp-p, the 1LSB becomes approximately 1 mV. In order to obtain the predesignated characteristics, due care should be exercised in the designing of the CX20051A periphery circuit.

[Note on mounting onto the printed board]

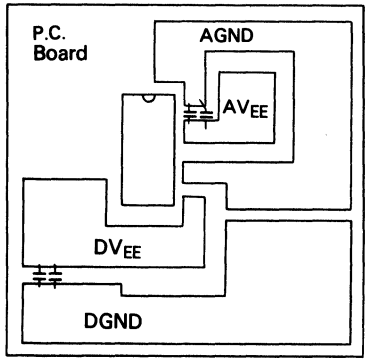
The external connection diagram of CX20051A is basically as shown in Fig. 3. In this regard, take note to the points mentioned below.

(1) AGND and DGND as also AV_{EE} and DV_{EE} are not connected internally. It is also desired to separate the analog block and digital block externally.

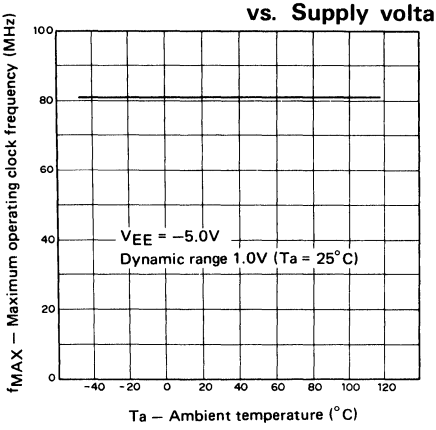
(2) Take as much space as possible of the ground surface on the printed board to reduce parasitic inductance and resistance.

(3) Insert a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor in parallel between the V_{EE} surface and the ground surface most adjacent to it on the printed board and reduce the noise. In addition, it is also desired to insert a capacitor between the V_{EE} surface and the GND surface near the IC. (See Fig. below)

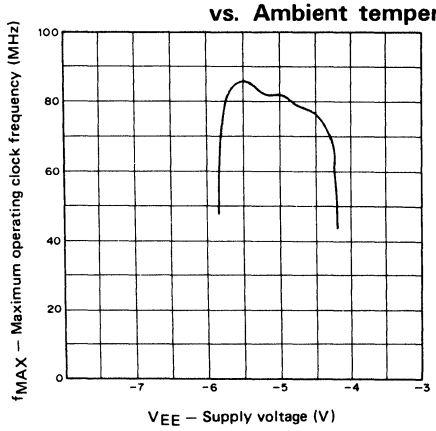
GND and V_{EE} pattern arrangement



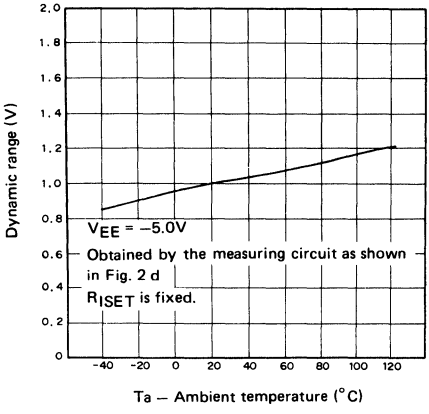
Maximum operating clock frequency vs. Supply voltage



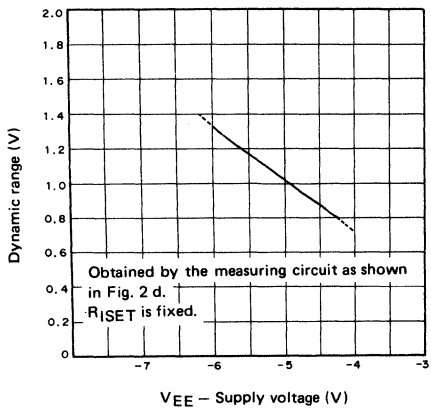
Maximum operating clock frequency vs. Ambient temperature



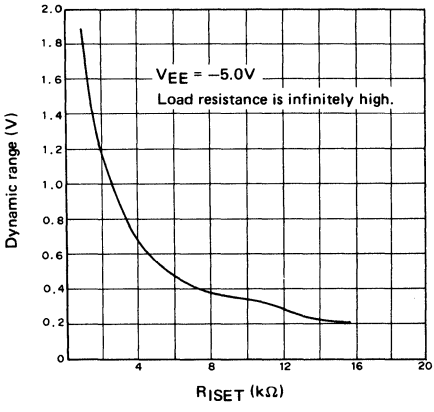
Dynamic range vs. Ambient temperature



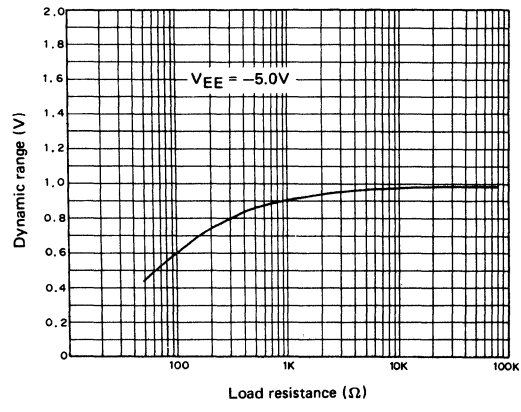
Dynamic range vs. Supply voltage



Dynamic range vs. RISET



Dynamic range vs. Load resistance



SONY **CX20052A**

8 bit 20MHz Sub-ranging A/D Converter

Description

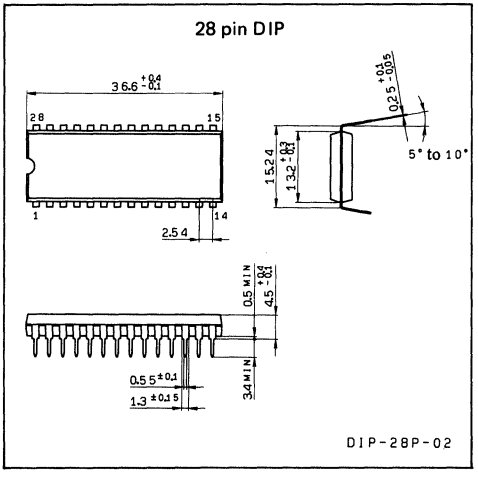
CX20052A is a serial-parallel type high speed A/D converter with a resolution of 8 bit for processing video signals driven by a single −5.0V power source.

It performs an A/D conversion of video signals with an external sample & holding circuit. A reference voltage and a clock should be added external to it.

The digital output is provided in 8 bit parallel with an open emitter. Both the clock and the digital output are in ECL level.

Package Outline

Unit : mm



Features

- Maximum sampling frequency of 20 MHz (Min.)
- Low power consumption 700 mW (Typ.)
- Non-linearity error ±½ LSB
- −5.0V single power supply
- Both clock input and digital output are in ECL level

Structure

Bipolar Silicon Monolithic IC.

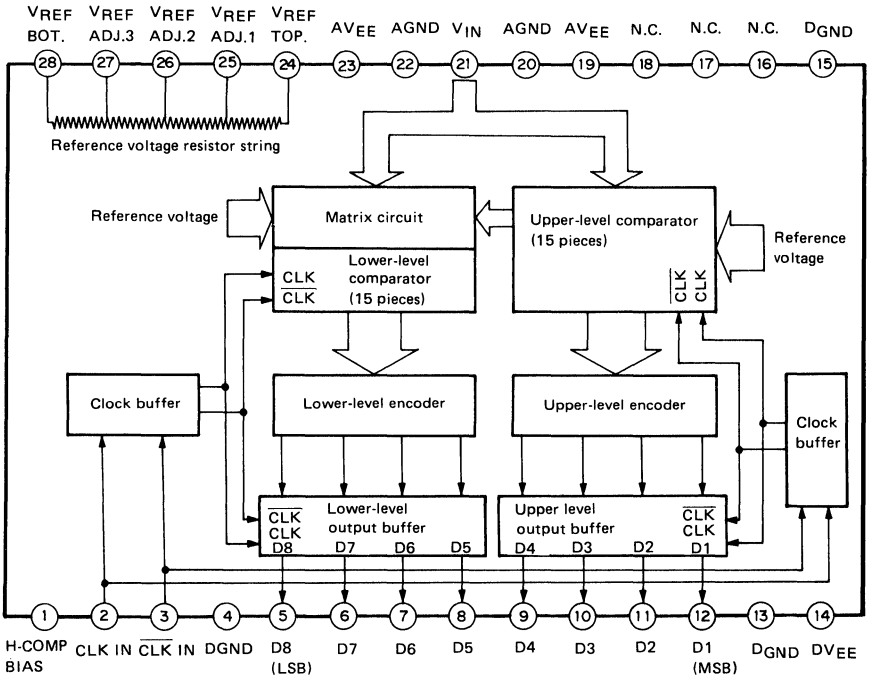
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	−9.0	V
• Clock voltage	V_{CLK}	V_{EE} to +0.3	V
• Input signal voltage	V_{IN}	V_{EE} to +0.3	V
• Reference voltage	V_{REF}	V_{EE} to +0.3	V
• Digital output current	I_{OH}	10	mA
• Operating temperature	Topr	−10 to +70	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation	P_D	1.47	W

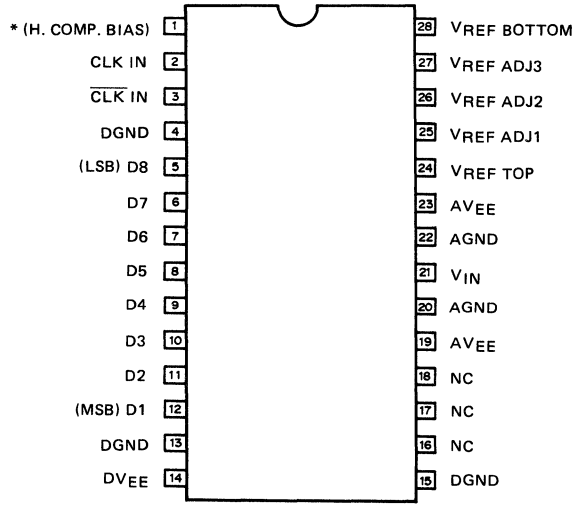
Recommended Operating Conditions

• Supply voltage	V_{EE}	−5.25 to −4.75	V
• Clock voltage	V_{IH}	−1.04 to −0.74	V
	V_{IL}	−1.9 to −1.6	V
• Input signal voltage	V_{IN}	−2.0 to 0	V
• Reference voltage	V_{REF}	−2.1 to −1.9	V

Block Diagram



Pin Configuration (Top View)



* Pin-1 to be used open.

Pin Description

No.	Symbol	Description
1	H-COMP BIAS	Pin connected to internal comparator. It should not be connected to outer circuit.
2	CLK IN	CLOCK input pin.
3	$\overline{\text{CLK}}$ IN	$\overline{\text{CLOCK}}$ input pin.
4	DGND	Ground pin of digital circuit.
5	D8	Digital output pin. (LSB)
6	D7	Digital output pin.
7	D6	
8	D5	
9	D4	
10	D3	
11	D2	
12	D1	Digital output pin. (MSB)
13	DGND	Ground pin of digital circuit.
14	DVEE	Power supply pin of digital circuit. (−5.0V)

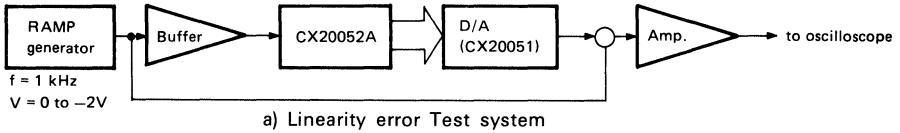
No.	Symbol	Description
15	DGND	Ground pin of digital circuit.
16	NC	Non-connection.
17	NC	
18	NC	
19	AVEE	Power supply pin of analog circuit. (−5.0V)
20	AGND	Ground pin of analog circuit.
21	VIN	Analog input signal pin (0 to −2V)
22	AGND	Ground pin of analog circuit.
23	AVEE	Power supply pin of analog circuit. (−5.0V)
24	VREF (T)	Reference voltage pin. (0V)
25	VREF ADJ1	Reference voltage adjusting pin. (Usually it should be connected to GND through 0.047 μF capacitor.)
26	VREF ADJ2	
27	VREF ADJ3	
28	VREF (B)	Reference voltage pin. (−2.0V)

Electrical Characteristics

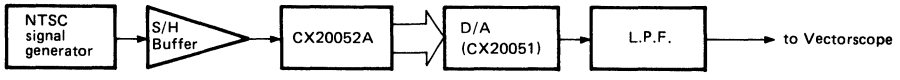
(Ta=25°C, AGND, DGND=0V, AV_{EE}, DV_{EE}=−5V)

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Linearity error	L.E.	V_{IN}: f=1 kHz, 0 to −2V ramp. CLK: 20 MHz ECL level			±½	LSB
2	Differential gain	D.G.	V_{IN}: NTSC 40 IRE mod. ramp CLK: 20 MHz ECL level		0.7		%
3	Differential phase	D.P.	V_{IN}: NTSC 40 IRE mod. ramp CLK: 20 MHz ECL level		0.3		deg.
4	Max. actuating clock frequency	f_{CLK} (MAX)	V_{IN}: f=1 kHz, 0 to −2V ramp. Linearity error ±½ LSB Max.	20	30		MHz
5	Power consumption	I_D	Output pin R_L=4.3 kΩ Including current flowing to R_L	110	140	160	mA
6	Clock input pin current	I_O	V_{CLK}=−0.885V $V_{\overline{CLK}}$=−1.75V		20.0	34.5	μA
7	Analog input pin current	I_{IN}	V_{IN}=0V V_{CLK}=−0.885V $V_{\overline{CLK}}$=−1.75V		70	110	μA
8	Digital output voltage-High	V_{OH}	V_{IN}=0V R_L=4.3 kΩ Output data is "11111111"	−0.90	−0.75		V
9	Digital output voltage-Low	V_{OL}	V_{IN}=−2.0V R_L=4.3 kΩ Output data is "00000000"		−1.50	−1.35	V
10	Reference resistor	R_{REF}	$V_{REF\ T}$=0V $V_{REF\ B}$=−2.0V	45	50	56	Ω
11	Input capacitance	C_{IN}	V_{IN}=−0.2V+0.07 Vrms		70		PF

Note) To measure linearity error, differential gain, differential phase, max. frequency, the digital outputs of CX20052A are reconverted into an analog signal with a 10 bit D/A converter CX20051.

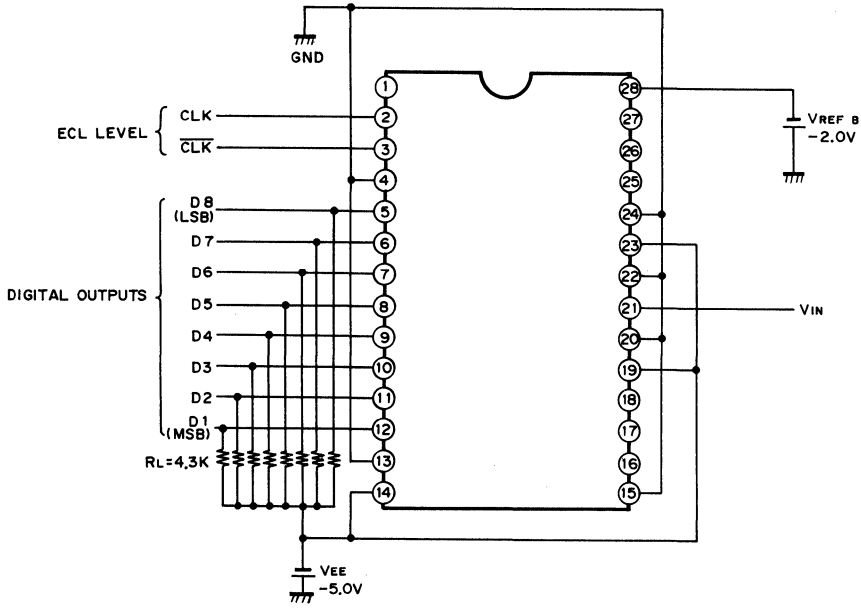


a) Linearity error Test system



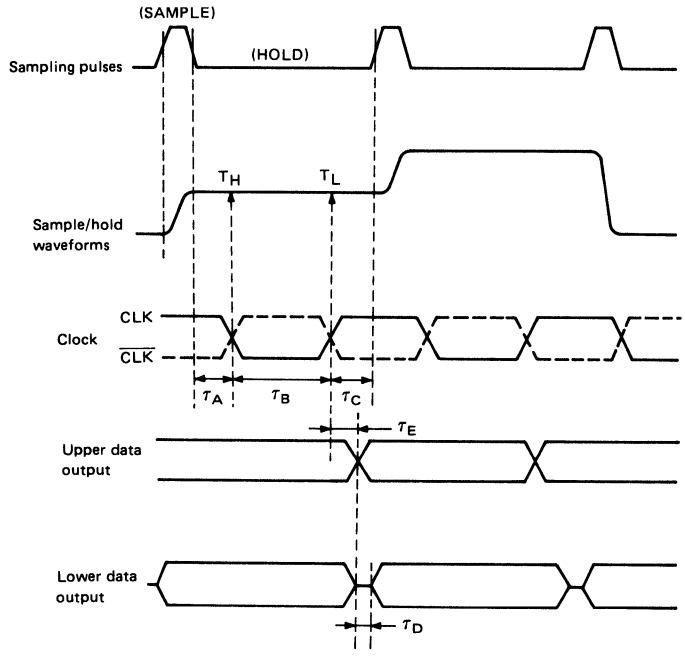
b) DG. DP Test system

Electrical Characteristics Test Circuit



Notes on Application

1. CX20052A, a serial-parallel type A/D converter, requires an external sample & holding circuit, and precautions should be taken for the sampling pulse and the timing of clock.
   Output data can be provided τ_D after T_L, but it is more reliable and simple to latch the results at rising edge of CLK.
   Duty of clock pulse should be set to the best point of DG and DP.



$\tau_A \geqq T_A$ (aperture time of S/H circuit + settling time)
$\tau_B \geqq 22$ ns
$\tau_C \geqq 2$ ns
$\tau_D \leqq 4$ ns
$\tau_E \leqq 8$ ns

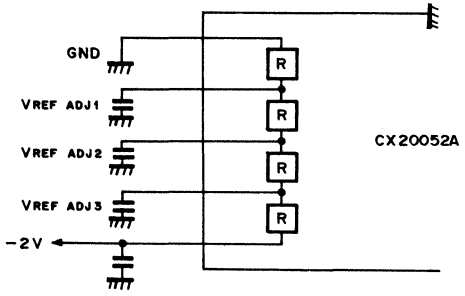
* Ta=−10°C to +70°C
T_H is the timing of the upper-level comparator for comparing V_{IN} with V_{REF} and latching the results.
T_L is the timing of the lower-level comparator for comparing V_{IN} with V_{REF} and latching the results.

2. Digital output pin of CX20052A is provided with an open emitter. Although the level is ECL compatible but the current must be less than 10 mA in operation. Output current is about 1 mA, when R_L is 4.3 kΩ. R_L is 4.3 kΩ.
   The reference table of analog input signal and digital output codes are shown below. D1 is MSB and D8 is LSB.

Step	Input signal voltage	Output digital code
		MSB LSB
000	0.0000V	11111111
.	.	.
.	.	.
.	.	.
127	−0.9961V	10000000
128	−1.0039V	01111111
129	−1.0118V	01111110
.	.	.
.	.	.
.	.	.
255	−2.0000V	00000000

3. Usually, clock input pin should be driven by complementary ECL signal. nal.

4. Reference resistors have adjusting pins as shown below. Usually these pins are connected to GND through 0.047 μF capacitors. When an adjustment is required, they should be connected to GND or $V_{REF\ (B)}$ through resistors.

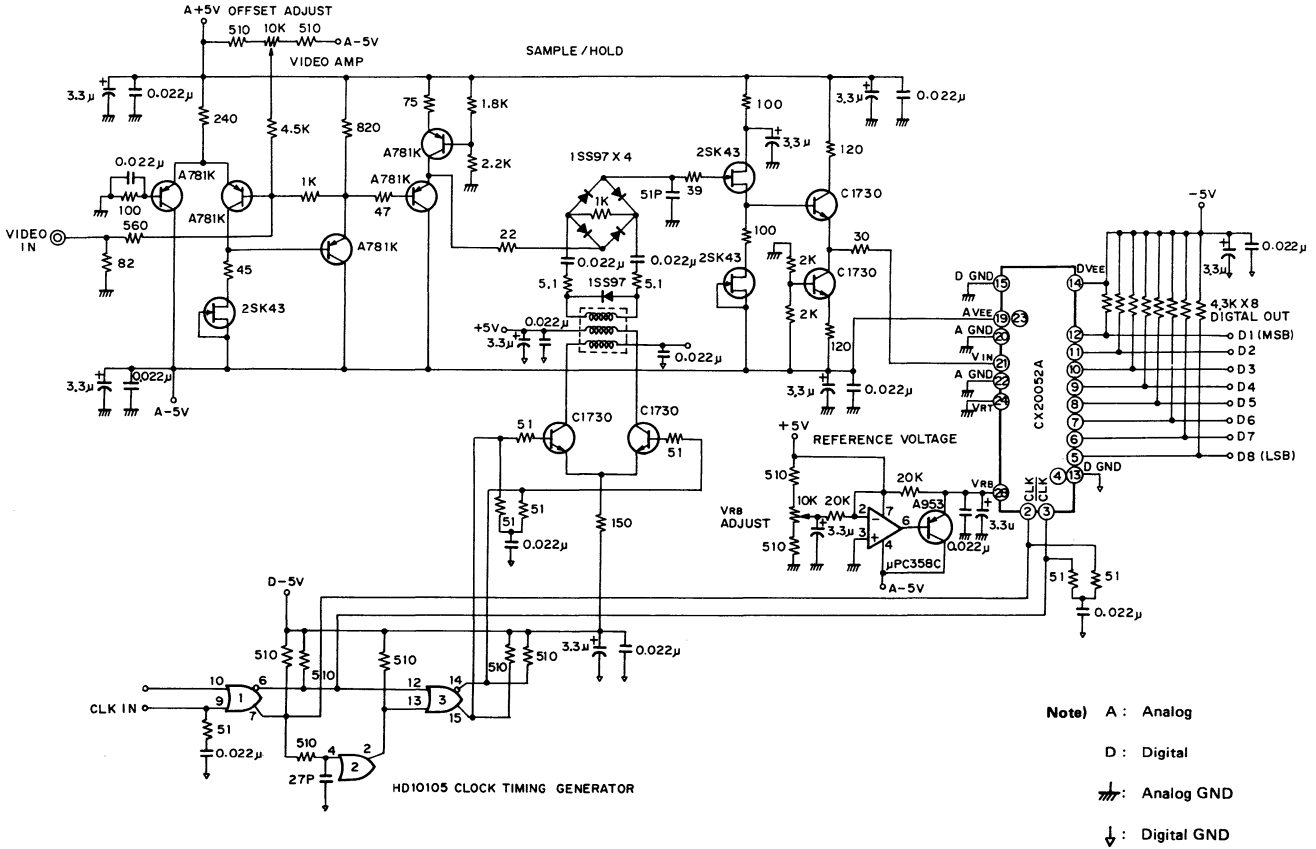


5. For reducing parasitic inductance and resistance, the wider area of GND pattern of the printed circuit board is the better.
   As ANALOG GND and DIGITAL GND are prepared, separated GND patterns can be designed.

6. Use a sampling and hold circuit which has short T_A for accurate sampling. (see the timing chart)

7. Although pin-1 (H, COMP, BIAS) is an idle pin, it is connected to internal circuit, so it should not be connected to GND, power supply or other pins. Pin-16, 17, 18 (NC) is not connected to internal circuit.

Application Circuit



Note) A : Analog

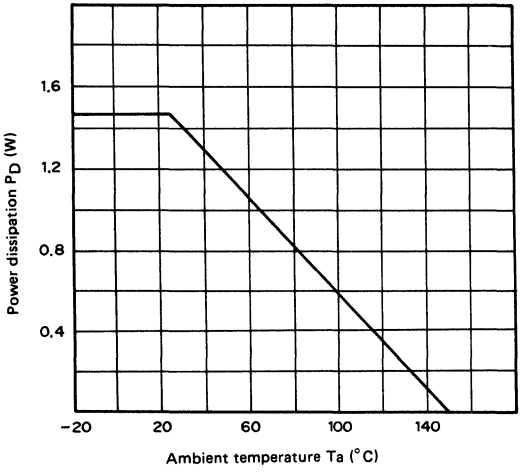
D : Digital

: Analog GND

: Digital GND

SONY

Derating Curve



8 bit 100 MHz Flash A/D Converter

Description

The CX20116/CX20116U/CXA1066K/CXA1066UK are the 8 bit ultra high speed A/D Converter Integrated Circuit capable of digitizing analog signals at rates from DC to 100 MHz. These A/Ds can be utilized in many varied applications. A wide analog input band width satisfies the characteristics for high definition television systems. Power consumption is approximately 1.2 Watts at 100 MHz sampling speed.

The CX20116U/CXA1066UK are high reliability version of CX20116/CXA1066K with extended temperature (−55 to 125°C) and bias burn-in (75 hours at 125°C).

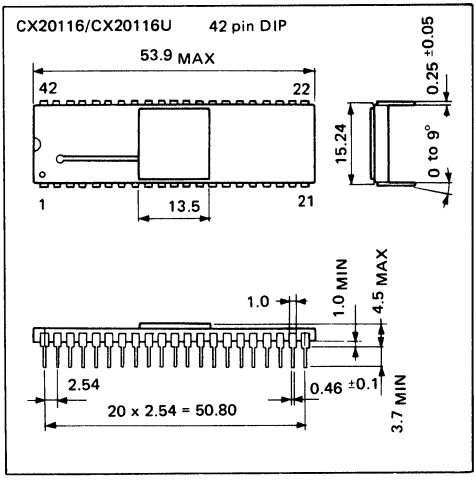
Features

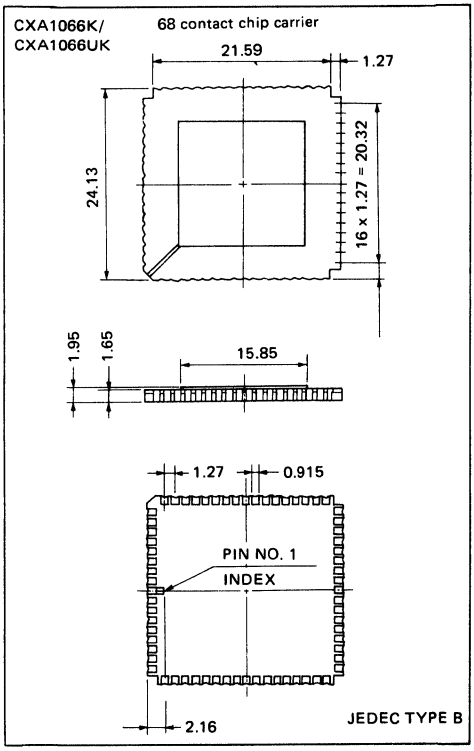
- Resolution at 8 bit ±½ LSB
- Ultra high speed operation with maximum conversion rate of 100 MHz
- Full scale input band width of 40 MHz (−3 dB)
- Low input capacitance at 40 pF (max.)
- Low power consumption at 1.2W (Typ)

Applications

- Digital video signal processing
- Radar/sonar and acquisition systems
- Medical electronics
- Digital measurement systems

Package Outline Unit: mm





Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}		0 to −7	V
• Analog input voltage	V_{IN}		0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}		0.5 to V_{EE}	V
	$\lvert V_{RT}-V_{RB}\rvert$		2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV		0.5 to −4	V
• V_{RM} pin input current	IVRM		−3 to 3	mA
• Digital output current	I_{D0} to I_{D7}		0 to −10	mA
• Operating temperature	Ta	CX20116	−20 to +100	°C
	Tc	CXA1066K	−25 to +125	°C*1
	Tc	CX20116U/CXA1066UK	−55 to +125	°C*1
• Strage temperature	Tstg		−55 to +150	°C
• Allowable power dissipation	P_D	CX20116/CX20116U	3.1	W
		CXA1066K/CXA1066UK	2.3	W

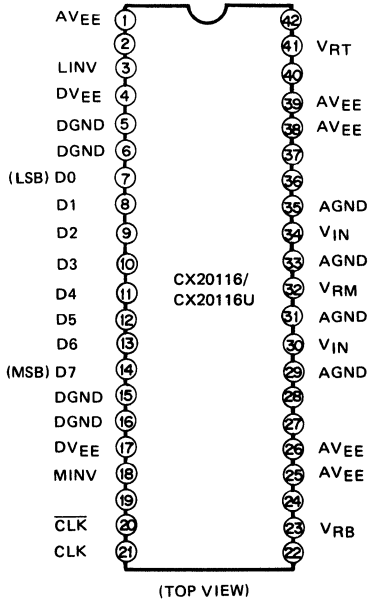
*1 Heat sinking is required for CXA1066K/CXA1066UK above 54°C ambient.

Recommended Operating Conditions

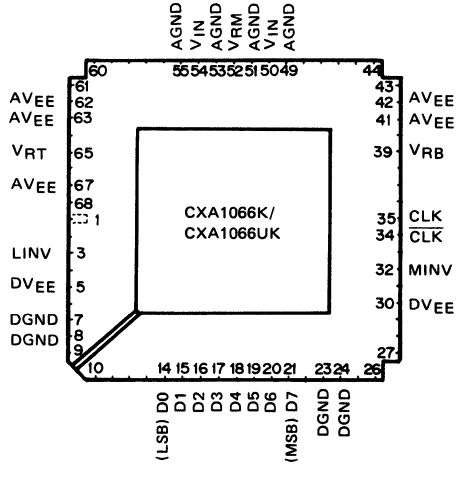
		Min.	Typ.	Max.	Unit.
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}—DV_{EE}	−0.05	0	0.05	V
	AGND—DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	7.5			ns
	Tpw0	2.5			ns

Pin Configuration

The pin numbers without indication are empty pins. (not connected)

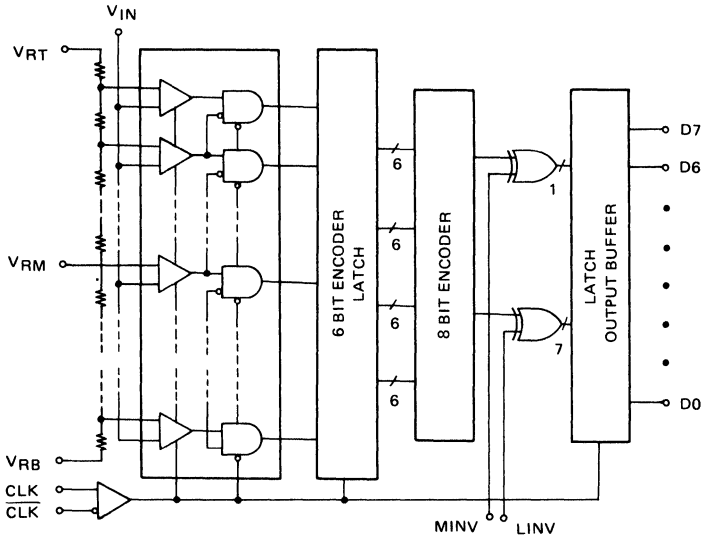


(TOP VIEW)



(TOP VIEW)

Block Diagram



Pin Description

Symbol	Function
AVEE	Analog VEE, −5.2V (typ). Coupled with ~6Ω between DVEE.
LINV	Input pin for output polarity inversion of D0 (LSB)−D6. (See the code table)
DVEE	Digital VEE, −5.2V (typ).
DGND	Digital GND, which is separated from the Analog GND.
D0−D7	Digital data output pin, ECL level. D0: LSB−D7: MSB. Pull-down resistors are necessary externally.
MINV	Input pin for output polarity inversion of D7 (MSB) (See the code table). ECL level. "0" level is held when it is released.
$\overline{CLK}$	Inverse clock input pin, ECL level.
CLK	Clock input pin, ECL level.
VRB	Reference voltage (bottom), −2V (typ).
AGND	Analog GND
VIN	Analog input, input range is VRT−VRB
VRM	Middle point of the reference voltage, it can be used as a linearity correction pin.
VRT	Reference voltage (top), 0V (typ).
	Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.

Electrical Characteristics

(Ta=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

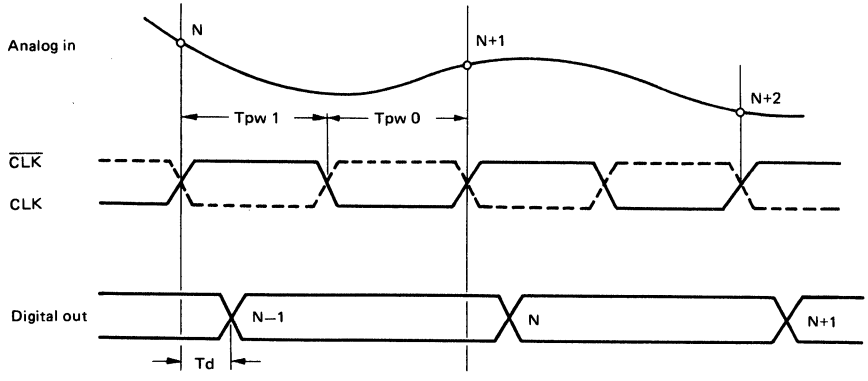
Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		Fc	V_{IN}=0 to −2V fin=1 kHz, ramp	100			MS/s
Supply Current		I_{EE}		−180	−220	−260	mA
Analog Input Capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	V_{IN}=−1V		150	220	μA
Reference Resistor		Rr (V_{RT} − V_{RB})		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	Rℓ=620Ω to V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	Rℓ=620Ω to V_{EE}	3.0	3.5	4.2	ns
Non-linearity Error			Fc=100 MS/s, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			Fc=35 MS/s, 1/16 LSB step ramp			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, Fc=100 MS/s			1.5	%
Differential Phase		DP				0.5	deg.
Aperture Jitter					15		ps

Output Coding

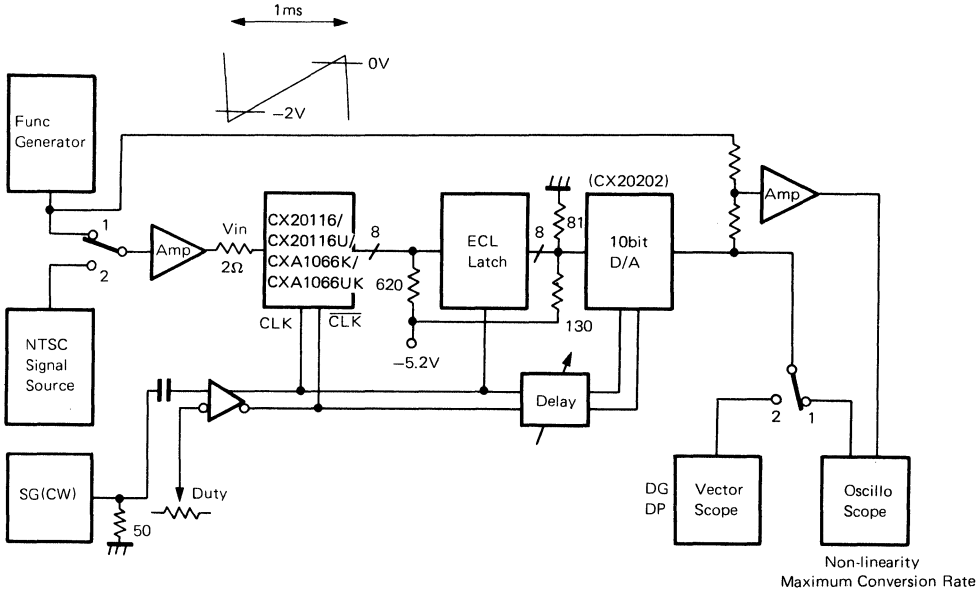
MINV / LINV	0 / 0	0 / 1	1 / 0	1 / 1
0V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
−2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}

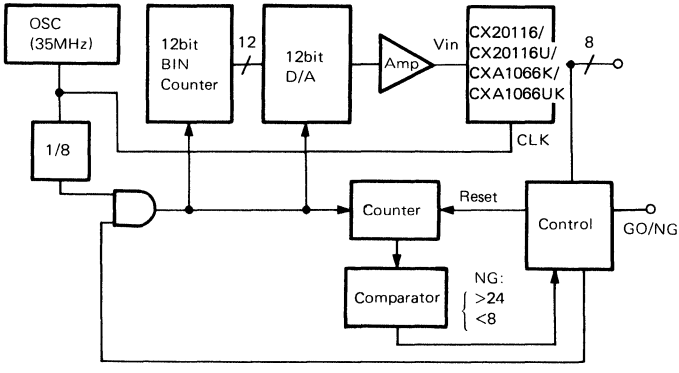
Timing Chart



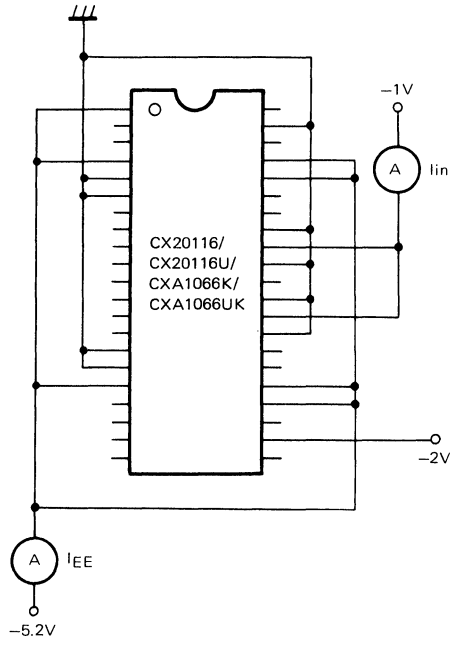
Electrical Characteristics Measuring Circuit
Maximum Conversion Frequency Measuring Circuit
Non-linearity Measuring Circuit
Differential Gain Error Measuring Circuit
Differential Phase Error Measuring Circuit



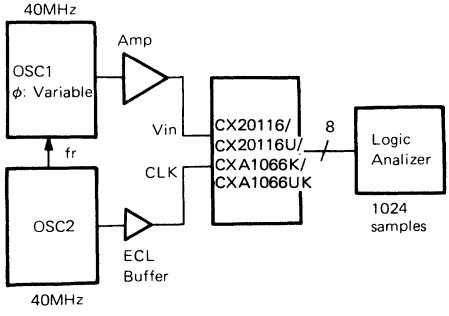
Differential Non-linearity Measuring Circuit



Power Supply Current Measuring Circuit
Analog Input Bias Current Measuring Circuit



Aperture Jitter Measuring Circuit



10/9/8 bit 160 MHz D/A Converter

Descriptions

A series of D/A converters CX20201A/CX20202A convert binary data into an analog signal at rates higher than 160 MHz. The devices include input data registers and have a capability of driving 75 ohms load. Three versions with linearity specifications of 10, 9 or 8 bits are available for each model.

These D/A converter ICs can be used in signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems, digital measurement instruments and radars.

CX20201A-1/CX20202A-1	10-bit
CX20201A-2/CX20202A-2	9-bit
CX20201A-3/CX20202A-3	8-bit

Features

- High speed — 160 MHz
- High accuracy — 10 bit (CX20201A-1/CX20202A-1)
- Low glitch energy — 15 pVsec
- Low power consumption — 420 mW
- Logic invert input
- 75-Ω direct drive capability
- Analog multiplying function

Structure

Bipolar silicon monolithic IC.

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{EE}	−7	V
• Digital input voltage	V_I	+0.3 to V_{EE}	V
• Reference input voltage	V_{REF}	+0.3 to V_{EE}	
• Analog output current	I_{OUT}	20	mA
• Operating temperature	T_{ope}	−20 to + 75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D		
CX20201A-1/-2/-3		870	mW
CX20202A-1/-2/-3		1430	mW

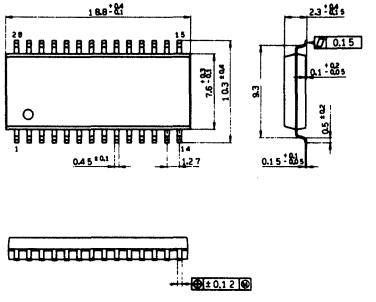
Recommended Operating Conditions

• Supply voltage	AV_{EE}, DV_{EE}	−4.75	to	−5.45	V
	AV_{EE}-DV_{EE}	−0.05	to	+0.05	V
• Digital input voltage	V_{IH}	−1.0	to	−0.7	V
	V_{IL}	−1.9	to	−1.6	V
• Reference input voltage	V_{REF}	V_{EE}+0.5	to	V_{EE}+1.4	V
• Load resistance	R_L	above 75			Ω
• Output voltage	$V_{O(FS)}$	0.8	to	1.2	V

Package Outline

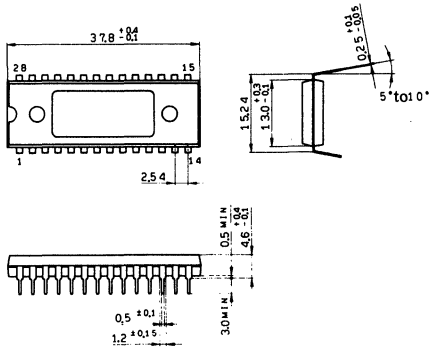
Unit: mm

CX20201A 28 Pin MFP



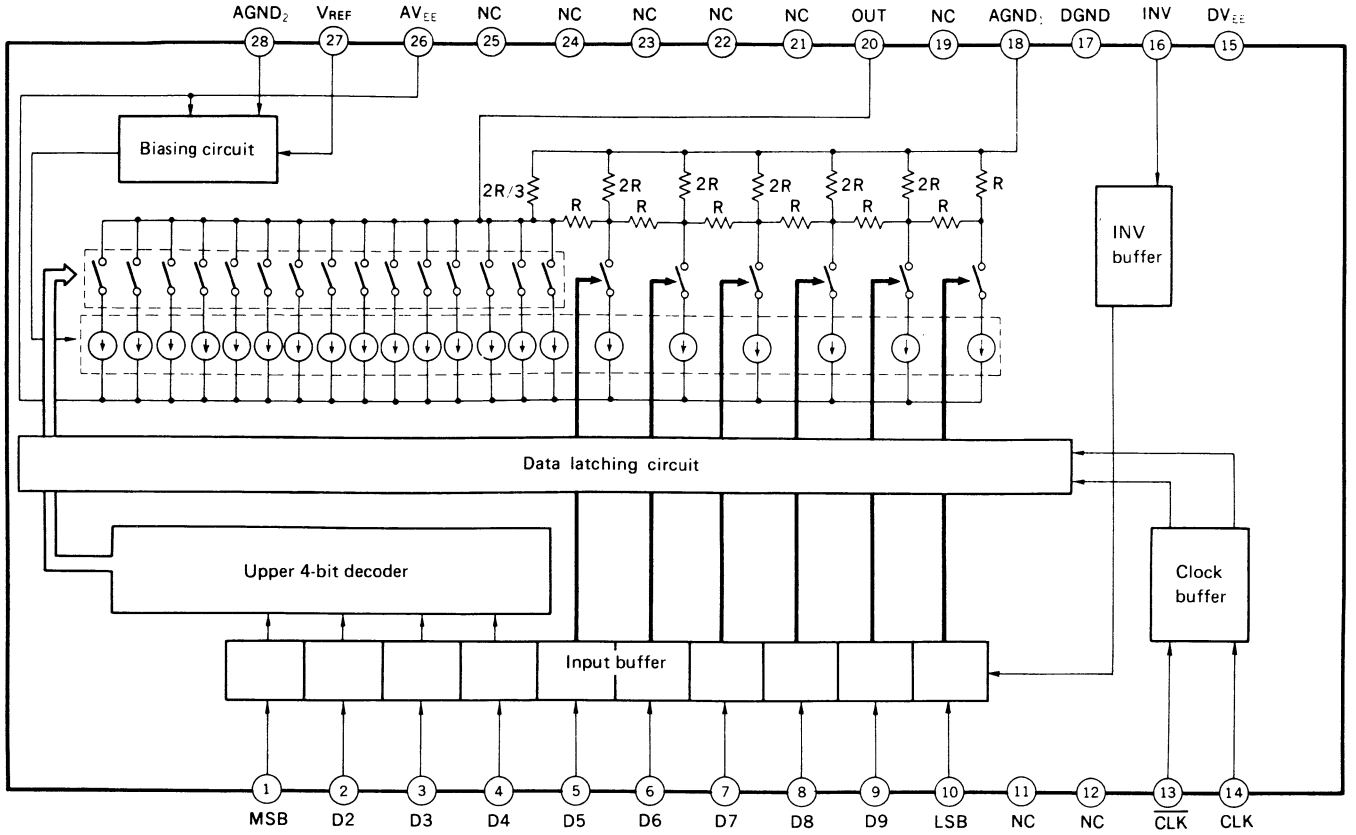
MFP-28P-L02

CX20202A 28 Pin DIP



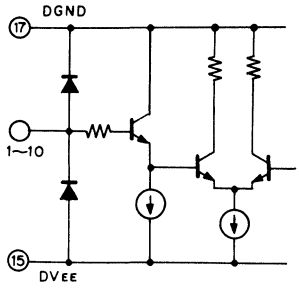
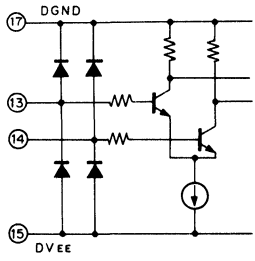
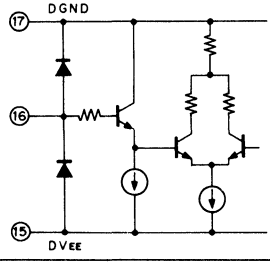
DIP-28P-03

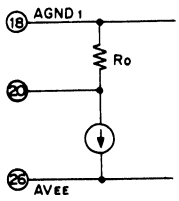
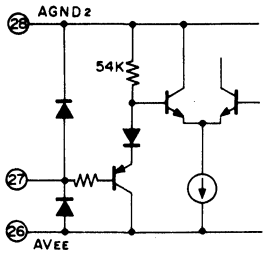
Block Diagram and Pin Configuration (top view)



SONY

Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 3 4 5 6 7 8 9 10	MSB D2 D3 D4 D5 D6 D7 D8 D9 LSB		Input pin for digital data. MSB and LSB are corresponded to the most significant bit and least significant bit, respectively. Pins not used should be left open or connected to DVEE.
11 12	NC		Non-connection
13 14	$\overline{\text{CLK}}$ CLK		Pins for clock inputs.
15	DVEE		Power supply pin for digital circuit.
16	INV		Code invert input pin which inverts the relationship between the binary code of digital data and D/A output voltage level.
17	DGND		Grounding pin for digital circuit.
18	AGND 1		Grounding pin directly connected to the R-2R output resistor circuit network in the IC. Grounding for analog circuit system.
19	NC		Non-connection

No.	Symbol	Equivalent circuit	Description
20	OUT		D/A analog output.
21 22 23 24 25	NC		Non-connection
26	AVEE		Power supply pin for analog circuit.
27	VREF		Bias pin which controls D/A output range. The output scale is set by the potential difference between VREF and AVEE.
28	AGND3		Grounding pin for analog circuit system other than the R-2R output resistor circuit network in the IC

Electrical Characteristics (1) Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

CX20201A-1/CX20202A-1

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		10		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.1		+0.1	% of FS
Settling time	ts		5.2		ns

CX20201A-2/CX20202A-2

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		9		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.1		+0.1	% of FS
Settling time	ts		4.7		ns

CX20201A-3/CX20202A-3

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		8		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.2		+0.2	% of FS
Settling time	ts		4.3		ns

Electrical Characteristics (2) Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

Item		Symbol	Measuring condition*1	Min.	Typ.	Max.	Unit
Power supply current	CX20201A	IEE		−60	−75	−90	mA
	CX20202A			−65	−82	−100	
Data input current (for upper 4 bits)		IIH(U)	VIH = −0.89V	0.1	1.5	6.0	μA
		IIL(U)	VIL = −1.75V	0.1	1.5	6.0	μA
Data input current (for lower 6 bits)		IIH(L)	VIH = −0.89V	0.1	0.75	3.0	μA
		IIL(L)	VIL = −1.75V	0	0.75	3.0	μA
Clock input current		ICLKH	VIH = −0.89V	2	23	70	μA
Invert input current		IINVH	VIH = −0.89V	0.1	1.5	6.0	μA
Reference input current		IREF	VREF = −4.38V	−3	−0.4	−0.1	μA
Output resistance		RO	IO = −1mA	52	65	78	Ω
Maximum conversion rate		fC	RL = 75Ω	160			MSPS

*1 See Figs. 3 to 5.

Data for Typical Application

Ta = 25°C, AV_{EE} = DV_{EE} = −5.2V, AGND = DGND = 0V, R_L = ∞, $V_{O(FS)}$ = −1V

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Output voltage zero offset	EZS	$R_L \geqq 10k\Omega$	0	−7	−21	mV
		$R_L = 75\Omega$	0	−7	−21	
Output voltage full-scale temperature coefficient	$T_{C(FS)}$	$R_L \geqq 10k\Omega$	0	−140	−280	ppm/°C
		$R_L = 75\Omega$	0	−580	−1200	
Output voltage zero offset temperature coefficient	$T_{C(ZS)}$	$R_L \geqq 10k\Omega$	6	16	22	μV/°C
Output voltage full-scale dynamic range	$V_{O(FS)}$	$R_L \geqq 10k\Omega$	0.8	1.0	1.6	V
		$R_L = 75\Omega$	0.8	1.0	1.2	
Glitch energy	GE	Digital ramp		15		pVsec
Rise time	tr	$R_L = 75\Omega$		1.5		ns
Fall time	tf			1.5		ns
Propagation delay	td			3.8		ns
Band width for multiplying	BW_{MUL}	$R_L = 75\Omega$, −3dB	10	14		MHz
Set-up time	tsu				5.0	ns
Hold time	thd				1.0	ns

Timing Chart

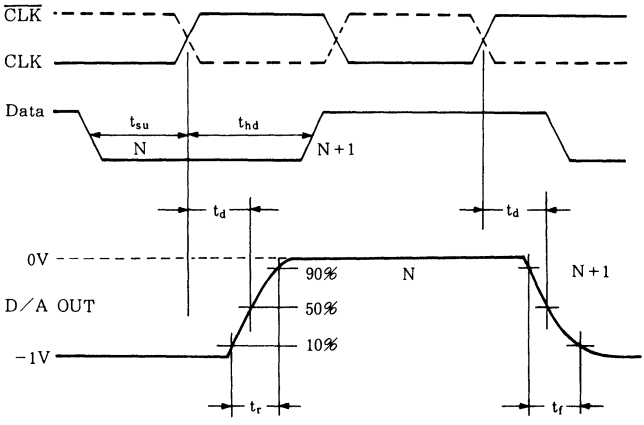


Fig. 1

Input Coding Table

Input code	Output code (V)	
	INV = 0	INV = 1
0 0 0 ····· 0 0	0	−1
0 1 1 ····· 1 1	−0.5	−0.5
1 0 0 ····· 0 0		
1 1 1 ····· 1 1	−1	0

Measuring Conditions for Current Consumption, Input Current and Output Resistance (See Fig. 2.)

Test item	Symbol	Switch condition																					Test point
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	
Current consumption	I_{EE}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b	I1
Data input current for upper 4 bits (H level)	$I_{IH(U)}$	a	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	I2
		b	a	b	b																		
		b	b	a	b																		
		b	b	b	a																		
Data input current for lower 4 bits (L level)	$I_{IL(U)}$	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	I2
		b	a	b	b																		
		b	b	a	b																		
		b	b	b	a																		
Data input current for upper 6 bits (H level)	$I_{IH(L)}$	b	b	b	b	a	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	I2
						b	a	b	b	b	b												
						b	b	a	b	b	b												
						b	b	b	a	b	b												
						b	b	b	b	a	b												
						b	b	b	b	b	a												
Data input current for lower 6 bits (L level)	$I_{IL(L)}$	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	I2
						b	a	b	b	b	b												
						b	b	a	b	b	b												
						b	b	b	a	b	b												
						b	b	b	b	a	b												
						b	b	b	b	b	a												
Clock input current (H level)	I_{CLKH}	b	b	b	b	b	b	b	b	b	b	b	a	b	b	a	b	b	b	b	b	b	I3
Clock-bar input current (H level)	$I_{\overline{CLK}H}$	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	b	b	b	b	I4
Invert input current (H level)	I_{INVH}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	I5
Referecnce input current	I_{REF}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	I6
Output resistance	R_O	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	V1

Electrical Characteristics Test Circuit

Test Circuit for Current Consumption, Input Current and Output Resistance

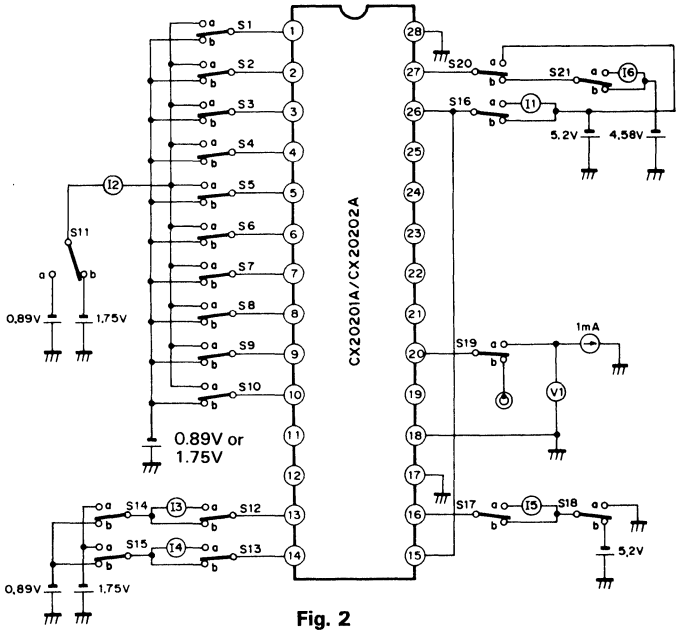
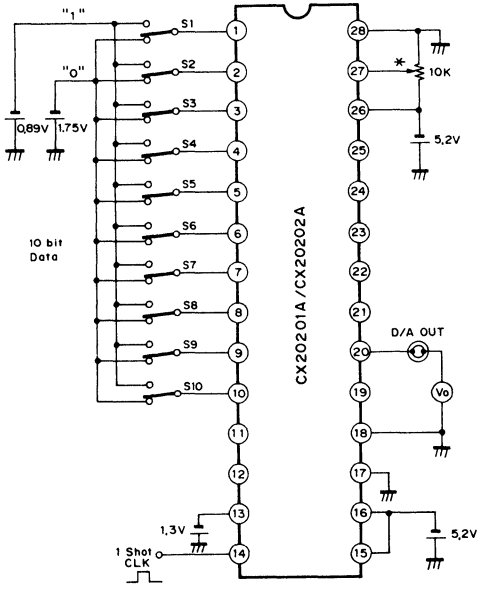


Fig. 2

Test Circuit for Differential Linearity Error and Linearity Error



* Adjust so that the full scale of DC voltage at Pin 20 becomes 1.023V, that is, to satisfy $V_O - V_{1023} = 1.023V$.

Fig. 3

Linearity errors are measured as follows.

S1	S2	S3	·····	S9	S10	D/A out
0	0	0	·····	0	0	V_0
0	0	0	·····	0	1	V_1
0	0	0	·····	1	0	V_2
			⋮			⋮
1	1	1	·····	1	1	V_{1023}

Linearity error	Differential linearity error
V_0	
V_1	$V_1 - V_0$
V_2	$V_2 - V_1$
V_4	$V_4 - V_3$
V_8	$V_8 - V_7$
V_{16}	$V_{16} - V_{15}$
V_{32}	$V_{32} - V_{31}$
V_{64}	$V_{64} - V_{63}$
V_{128}	$V_{128} - V_{127}$
V_{192}	$V_{192} - V_{191}$
⋮	⋮
V_{960}	$V_{960} - V_{959}$
V_{1023}	

Errors at individual measurement points are calculated according to the following definition.

$(V_{1023} - V_0)/1023 = V_{O(FS)}/1023 \equiv 1$ LSB.

Test circuits for { Maximum conversion rate, Rise time, Fall time, Propagation delay, Set-up time, Hold time, Settling time }

DL: delay line (ELMEC VDS1110)
Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

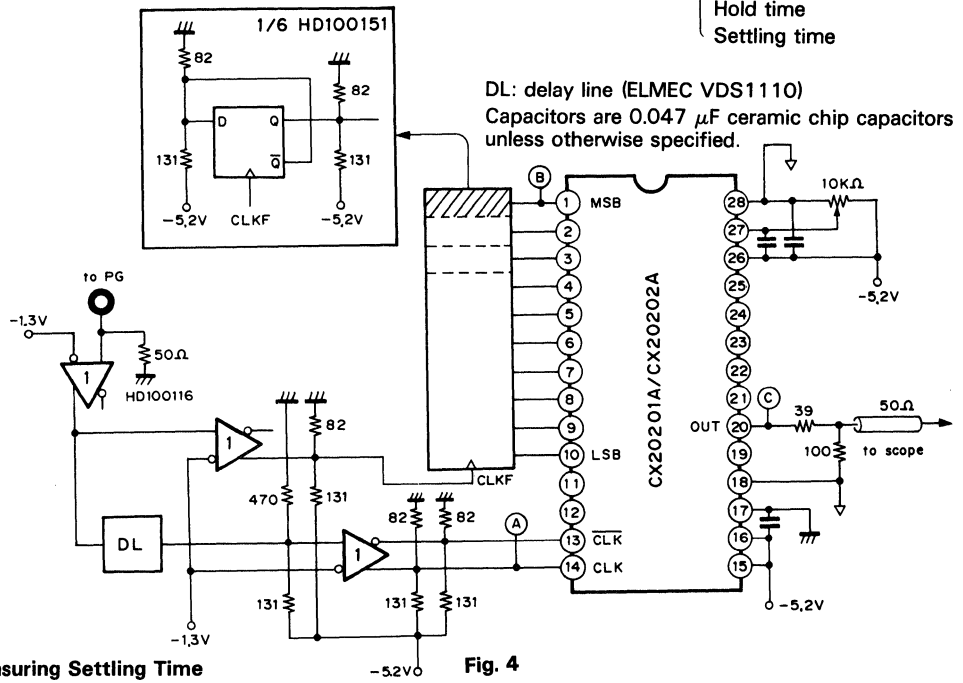


Fig. 4

Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{O(FS)}$ as shown in the D/A output waveform in Fig. 5 is expressed as

$V = V_{O(FS)} (1 - e^{-t/\tau})$.

The settling time for respective accuracy of 10 , 9 and 8-bit is specified as

$V = 0.9995\ V_{O(FS)}$

$V = 0.999\ V_{O(FS)}$

$V = 0.998\ V_{O(FS)}$

which results in the following:

$t_s = 7.60\tau$ for 10-bit,

$t_s = 6.93\tau$ for 9-bit, and

$t_s = 6.24\tau$ for 8-bit

Rise time (t_r) and fall time (t_f) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{O(FS)}$):

$V = 0.1\ V_{O(FS)}$

$V = 0.9\ V_{O(FS)}$

and calculated as $t_r = t_f = 2.20\ \tau$.

The settling time is obtained by combining these expressions:

$t_s = 3.45 t_r$ for 10-bit,

$t_s = 3.15 t_r$ for 9-bit, and

$t_s = 2.84 t_r$ for 8-bit

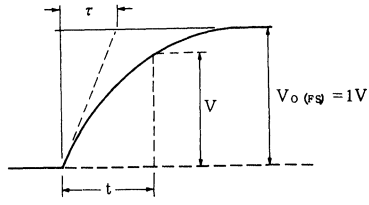


Fig. 5

Test Circuit for Multiplying Band Width

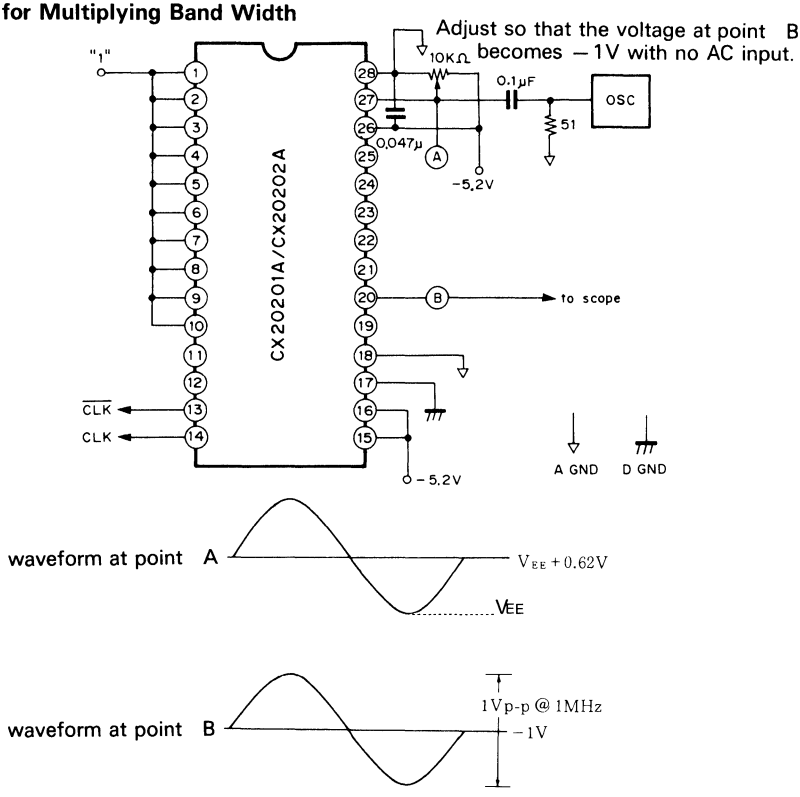


Fig. 6

Typical Application Circuit

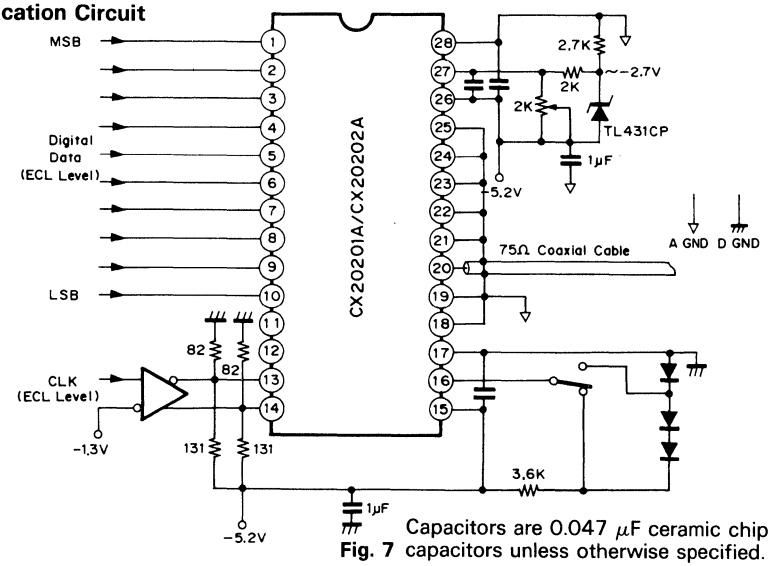


Fig. 7 Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

Notes on Applications

(1) Setting of full-scale output voltage

The full-scale output voltage ($V_{O(FS)}$) is set by the pin 27 (V_{REF}). $V_{O(FS)}$ varies in proportion to the voltage difference between pin 27 and pin 26 (AV_{EE}) as shown in Fig. 9.

$V_{O(FS)}$ can be set by simply dividing the supply voltage using resistors as shown in Fig. 8, but in this simple set up the voltage deviation of the supply voltage result in a deviation of $V_{O(FS)}$. This influence can be avoided by using a stabilization circuit as shown in Fig. 7 to allow stable full-scale output.

Pin 27 (V_{REF}) should be stabilized against high-frequency noise by sufficient by passing using a capacitor with low lead inductance such as ceramic chip capacitors. The stabilization capacitor should be inserted between pin 27 (V_{REF}) and pin 26 (AV_{EE}) as $V_{O(FS)}$ is direct proportion to the voltage across these two terminals.

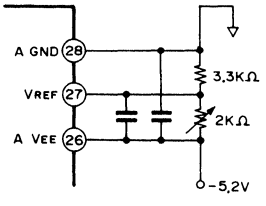


Fig. 8

(2) Noise reduction

An external digital noise should be minimized because the system handles small analog voltage (1 LSB corresponds 1 mV of analog output voltage for 10 bit resolution). Refer to the following notes to minimize the system noise contamination.

- Ground plane and V_{EE} plane on a printed circuit board should be made as wide as possible to reduce parasitic inductance and resistance.
- The patterns AGND and DGND should be separated on the printed circuit board. AV_{EE} and DV_{EE} should be separated too. The connections between analog system and digital system are to be made at the I/O ports of the printed circuit board.
- AV_{EE} and DV_{EE} should be bypassed to respective GND by using a tantalum capacitor of 1 μF and a ceramic chip capacitor of 47μF positioned as close as to terminals of the IC.
- Pins not in sure are to be connected to the ground plane.

(3) Load resistance and temperature coefficient

Temperature coefficient of the full-scale output voltage and zero offset voltage depend on the load resistance (value and type). Generally, the larger the load resistance the better the temperature coefficient value. Temperature characteristics at $R_L \geqq 10\ k\Omega$ and $R_L = 75\ \Omega$ are shown in Fig. 10.

(4) Input data and internal latching circuit

CX20201A/CX20202A incorporates a latching circuit as shown in the block diagram. This latching circuit has a two-stage configuration (master-slave type) and fetches input data only at the rising edge of the clock; the output is not affected by the changes in input data at any other timings. This mechanism allows stable operation against any changes in input data at any timings, except for the set-up time immediately before and the hold time immediately after the clock change from L to H.

(5) Driving input data and clock

CX20201A/CX20202A are designed to be operated at very high speed. It is, therefore, necessary to drive it with a high-speed ICs such as an ECL100K for full performance. Also the output port of the data and clock drivers should be terminated with 50-Ω systems. See Figs. 4 and 7.

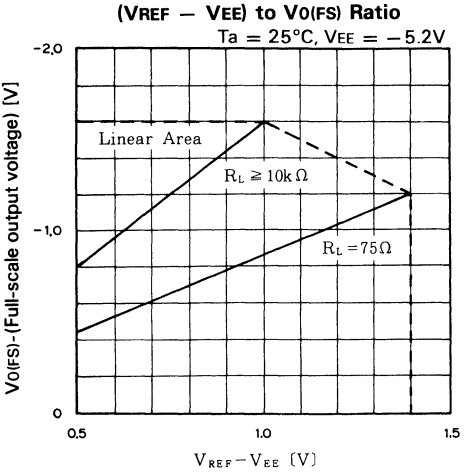


Fig. 9

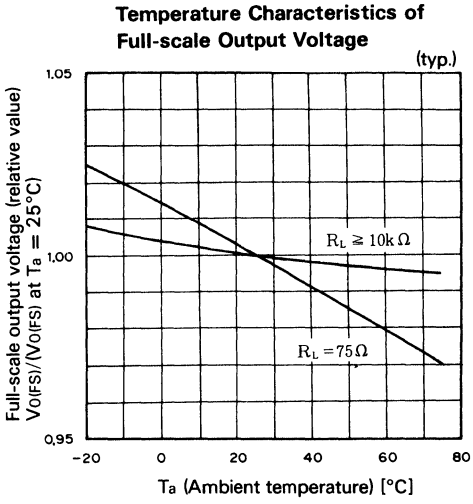


Fig. 10

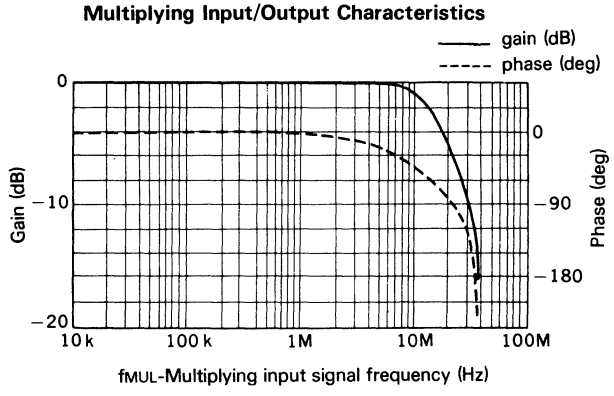


Fig. 11

8 bit 35 MHz RGB 3-channel D/A Converter

Description

The CX20206 is an 8 bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

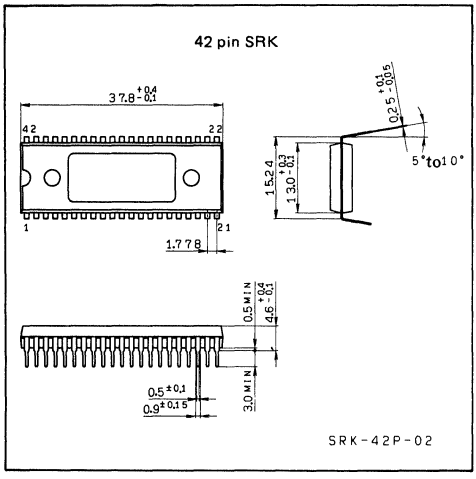
Features

- Resolution: 8 bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

Structure

Bipolar silicon monolithic IC

Package Outline Unit: mm



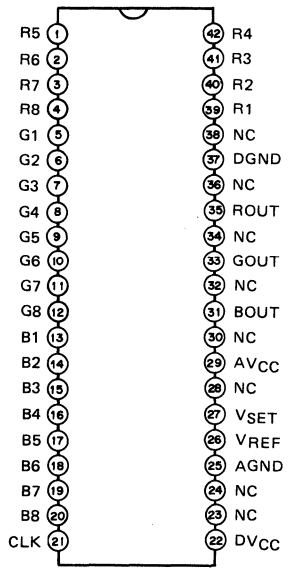
Absolute Maximum Ratings (Ta=25°C)

• Power supply voltage	V_{CC}	0 to 7	V
• Input voltage (digital)	V_I	−0.3 to V_{CC}	V
	V_{CLK}	−0.3 to V_{CC}	V
• Input voltage (V_{SET} pin)	V_{SET}	−0.3 to V_{CC}	V
• Output voltage (analog)	V_{OUT}	V_{CC}−2.1 to V_{CC}	V
• Output current (analog)	I_{OUT}	−3 to +10	mA
(V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.5	W

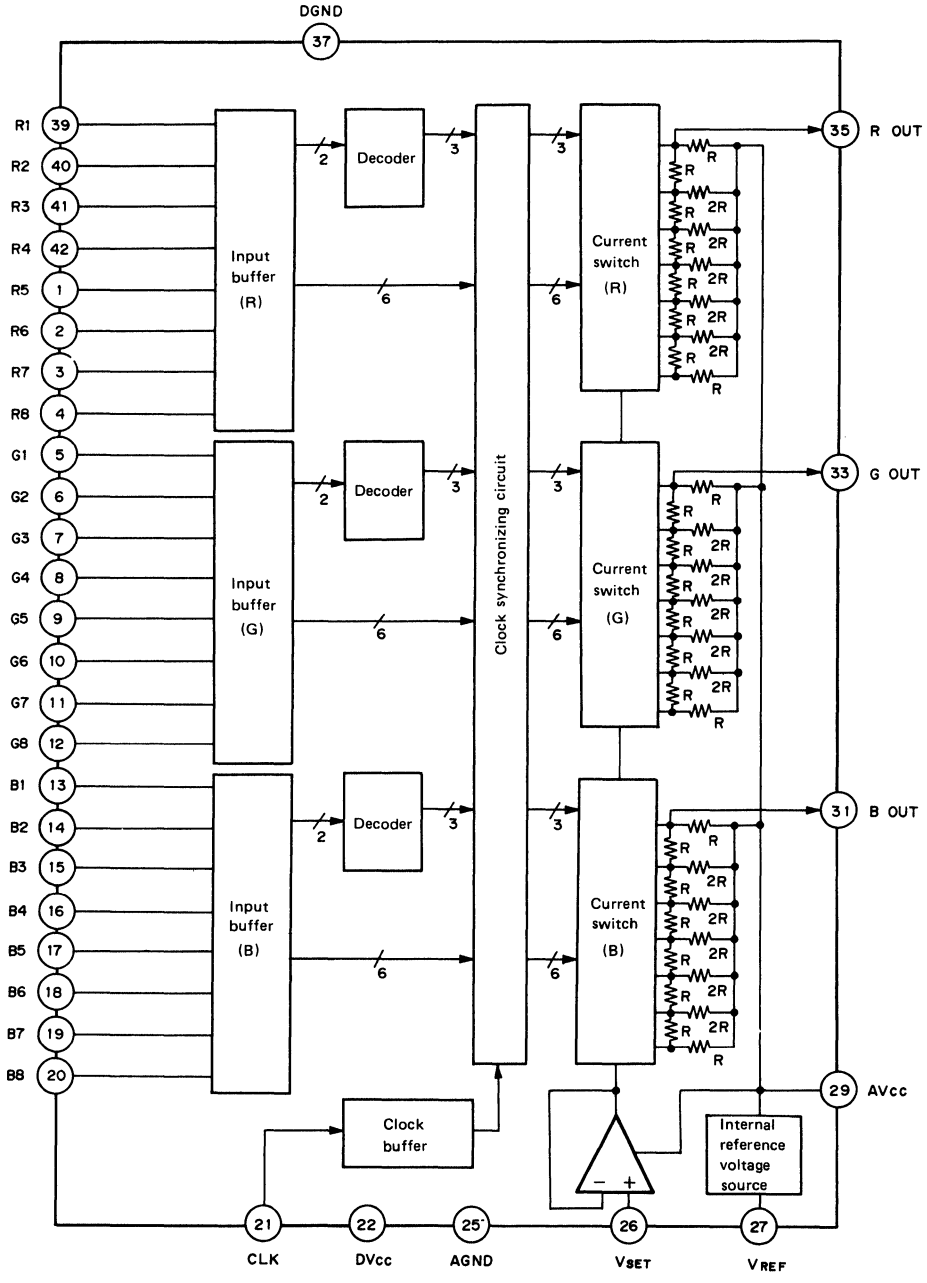
Recommended Operating Conditions

• Power supply voltage	AV_{CC}, DV_{CC}	4.5 to 5.5	V
	AV_{CC}–DV_{CC}	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	V_{IH}, V_{CLKH}	2.0 to DV_{CC}	V
L level	V_{IL}, V_{CLKL}	DGND to 0.8	V
• V_{SET} input voltage	V_{SET}	0.7 to 0.9	V
• V_{REF} pin current	I_{REF}	−3 to −0.4	mA
• Clock pulse width	T_{pw1}	15	ns
	T_{pw0}	10	ns

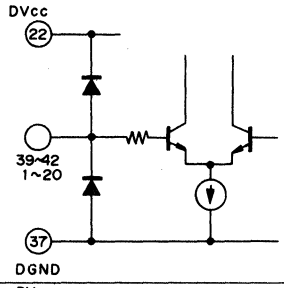
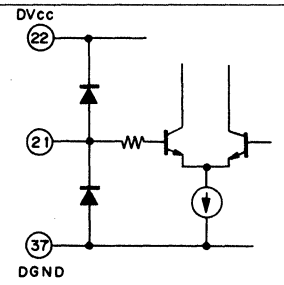
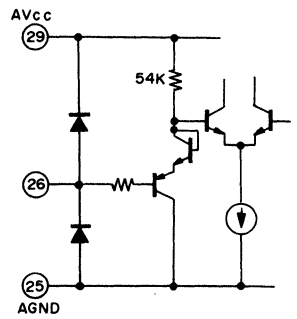
Pin Configuration (TOP VIEW)

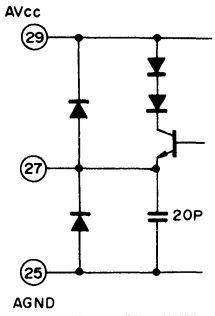
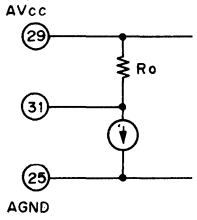
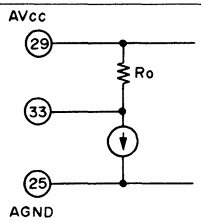
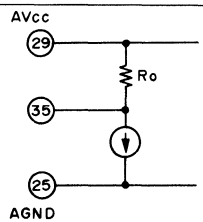


Block Diagram



Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 1 to 20	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 1 to 4 are for RED. R1 is MSB and R8 is LSB. From pins 5 to 12 are for GREEN. G1 is MSB and G8 is LSB. From pins 13 to 20 are for BLUE. B1 is MSB and B8 is LSB.
21	CLK		Clock input pin.
22	DVcc		Digital Vcc.
23 24	NC		Vacant pin (non-connection)
25	AGND		Analog GND.
26	VSET		Bias input pin. Normally, apply 0.8V. See "Note on use".

No.	Symbol	Equivalent circuit	Description
27	VREF		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use".
28	NC		Vacant pin (non-connection)
29	AVcc		Analog Vcc
30	NC		Vacant pin but connect to AVcc*
31	BOUT		Analog output pin for BLUE.
32	NC		Vacant pin but connect to AVcc*
33	GOUT		Analog output pin for GREEN.
34	NC		Vacant pin but connect to AVcc*
35	ROUT		Analog output pin for RED.
36	NC		Vacant pin but connect to AVcc*
37	DGND		Digital GND
38	NC		Vacant pin (non-connection)

*: Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics (Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item			Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	V_{SET}−AGND=0.8V R_L>10kΩ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			fMAX	V_{SET}−AGND=0.8V R_L>10kΩ C_L<20pF	35			MSPS
Full-scale output voltage(note 1)			VOFS		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio(note 2)			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			RO		270	340	420	Ω
Consumption current			ID	V_{SET}−AGND=0.8V R_L>10kΩ I_{REF}=−400μA	54	72	90	mA
Digital data input current	H level	Upper 2 bits	$I_{IH(U)}$	V_I=DVcc		1.2	20	μA
		Lower 6 bits	$I_{IH(L)}$			0.6	10	μA
	L level	Upper 2 bits	$I_{IL(U)}$	V_I=DGND	−10	0	10	μA
		Lower 6 bits	$I_{IL(L)}$		−10	0	10	μA
Clock input current		H level	I_{CLKH}	V_{CLK}=DVcc		3	30	μA
		L level	I_{CLKL}	V_{CLK}=DGND	−10	0	10	μA
V_{SET} input current			ISET	V_{SET}−AGND=0.8V	−5	−0.3	0	μA
Internal reference voltage			VREF	I_{REF}=−400μA	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

Note 1) AVcc−Vo

2) Maximum value among

$$100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|, \quad 100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|, \text{ or } 100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$$

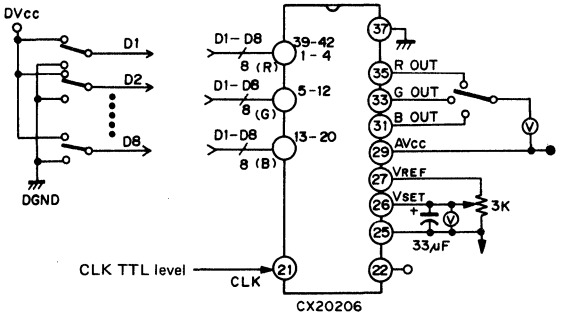
Input corresponding table

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	Vcc+Voffset
.	.
.	.
.	.
1 0 0 0 0 0 0 0	Vcc+Voffset−0.5V
.	.
.	.
.	.
0 0 0 0 0 0 0 0	Vcc+Voffset−1.0V

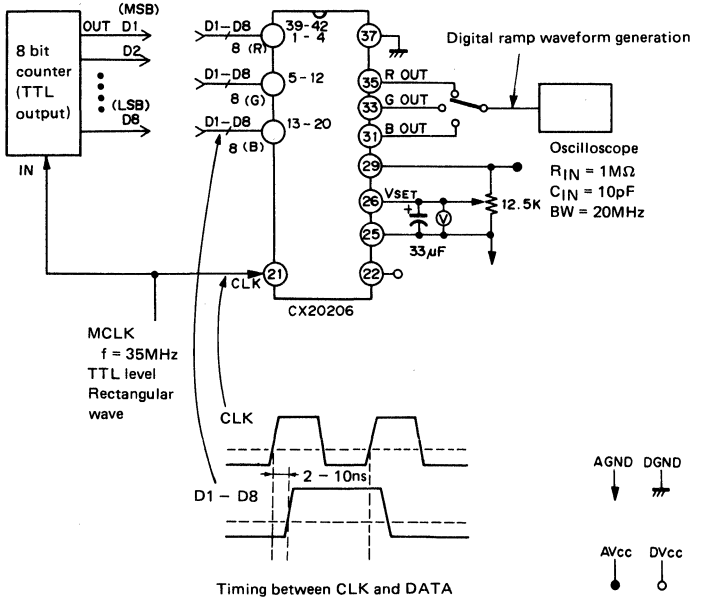
In case the output voltage full-scale is 1.00V. (1LSB=3.92 mV)

Electrical Characteristics Measuring Circuit

Differential linearity and integral linearity measuring circuits



Maximum conversion speed measuring circuit



Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage measuring circuits

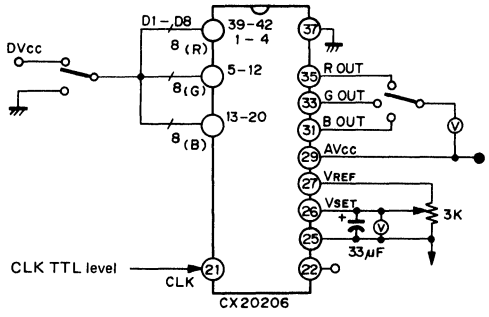
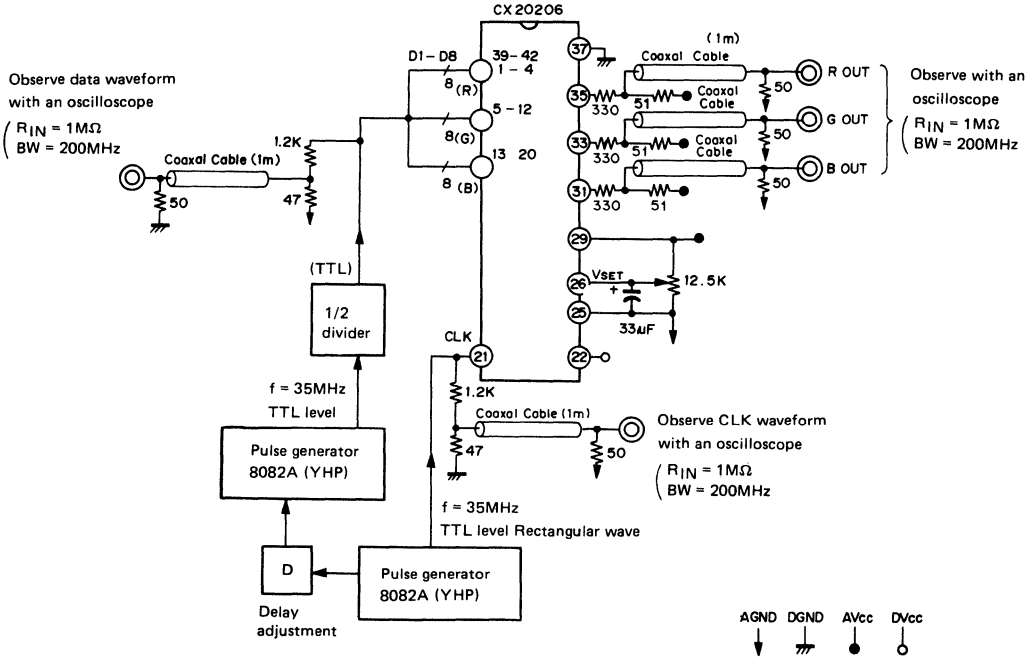


Fig. 1 Set-up time, hold time, and rise and fall time measuring circuits



Standard Circuit Design Data (Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p R_L>10kΩ C_L<20pF f_{DATA}=7MHz f_{CLK}=14MHz See Fig.2		−40	−33	dB
Glitch energy	GE	V_{SET}−AGND=0.8V R_L>10kΩ f_{CLK}=1MHz Digital ramp output See Fig.3(note 1)		160		pV-s
Rise time(note 2)	tr	V_{SET}−AGND=0.8V See Fig. 1.		5.5		ns
Fall time(note 2)	tf			5.0		ns
Settling time	tset			16		ns

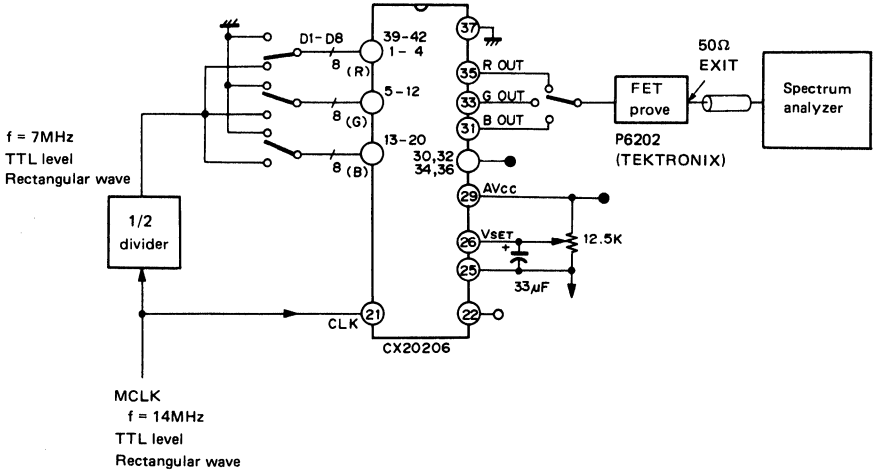
Note 1) Observe the glitch which is generated when the digital input varies as follows:

0 0 1 1 1 1 1 1 → 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 → 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 → 1 1 0 0 0 0 0 0

2) The time required for the D/A OUT to arrive at 90% of its final value from 10%.

Standard Circuit Design Data Measuring Circuit

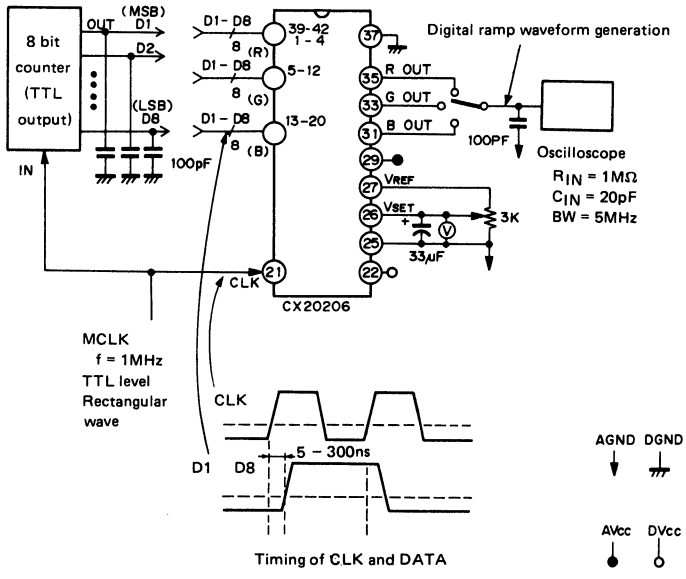
Fig. 2 Crosstalk among R, G and B measuring circuit



[Measuring method]
In case the measuring crosstalk of G → R

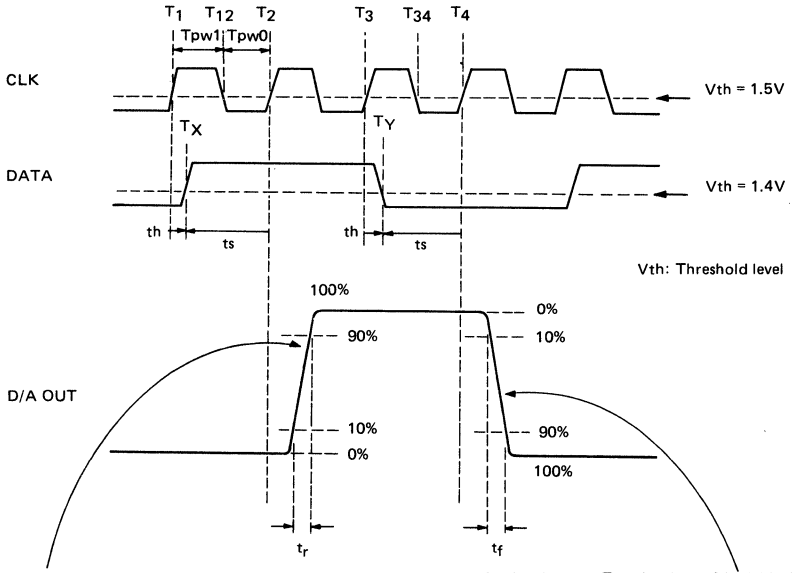
1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.
2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.
3 Take the difference of the above two powers. The unit is in dB.

Fig. 3 Glitch energy measuring circuit



Operation Description

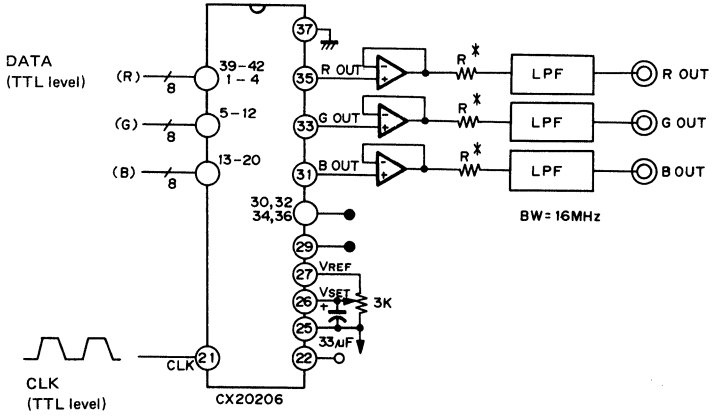
Timing chart



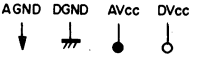
At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_4)).

Applied Circuit Example

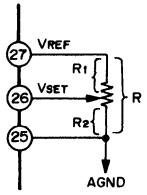


R* is matching resistance for LPF



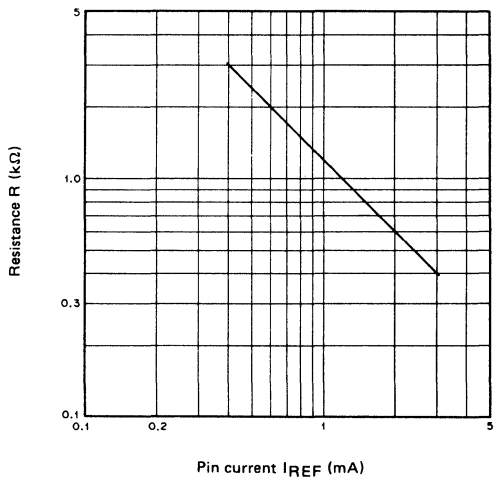
Note on Use

(1) Setting of pin 26 (V_{SET})
The full-scale of the D/A output voltage changes by applying voltage to pin 26 (V_{SET}). When load is connected to pin 27 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.8V by resistance division.
When the 0.8V is applied to pin 26 (V_{SET}), the D/A output of 1 Vp-p can be obtained.
(Example of use)



(Adjustment method)
1 The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
$R = V_{REF}/I_{REF}$
2 Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
(At this point, it becomes R1:R2=1:2)

Fig. 4 Resistance vs. V_{REF} pin current



(2) Phase relationship between data and clock
In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.
Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.
Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

(3) Regarding the load of D/A output pin

Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:

$R_L > 10\ k\Omega$

$C_L < 20\ pF$

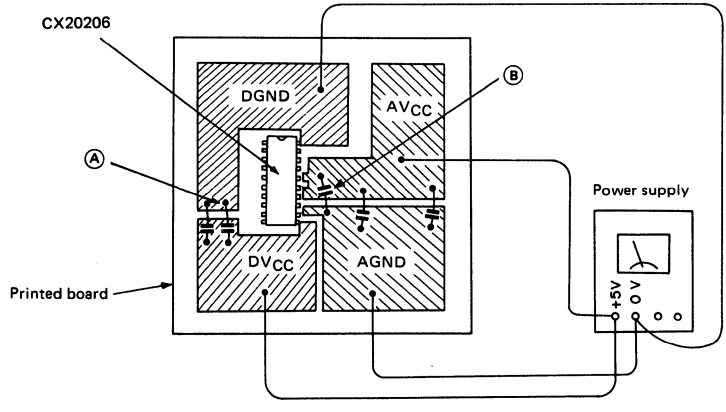
The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20\ pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

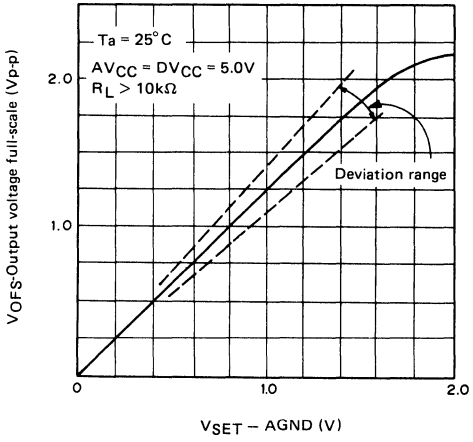
(4) Noise reduction measures

As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.

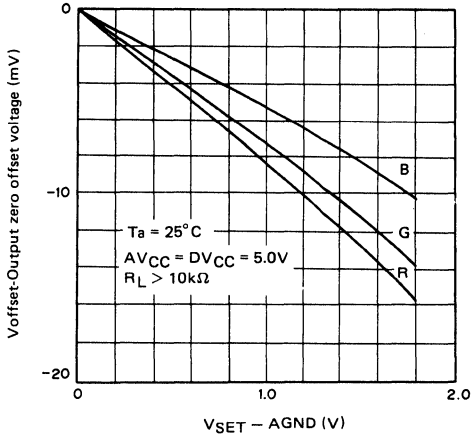
- When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC}. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the V_{CC} surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 25 (AGND) and pin 26 (V_{SET}).



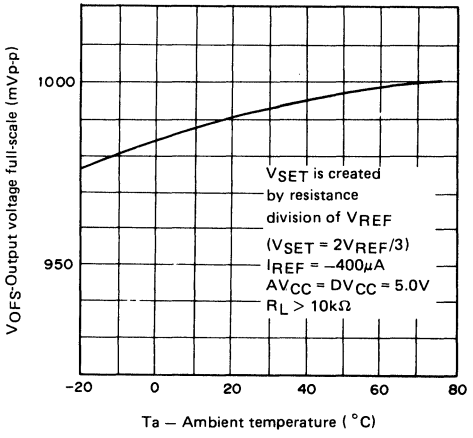
Output voltage full-scale vs. VSET—AGND



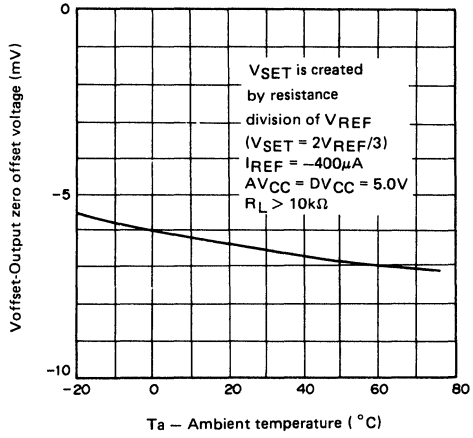
Output zero offset voltage vs. VSET—AGND



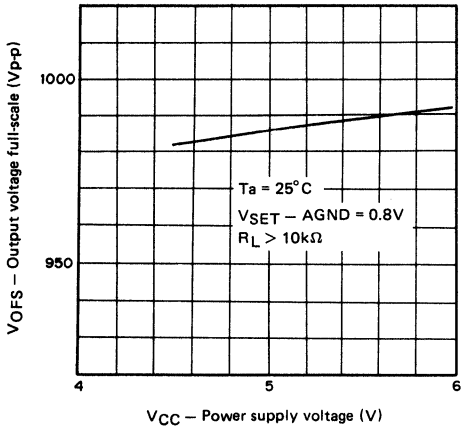
Output voltage full-scale vs. Ambient temperature



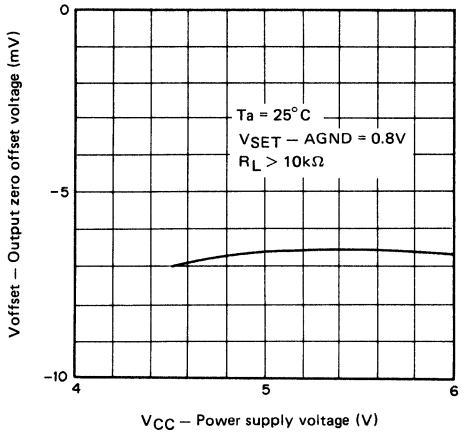
Output zero offset voltage vs. Ambient temperature



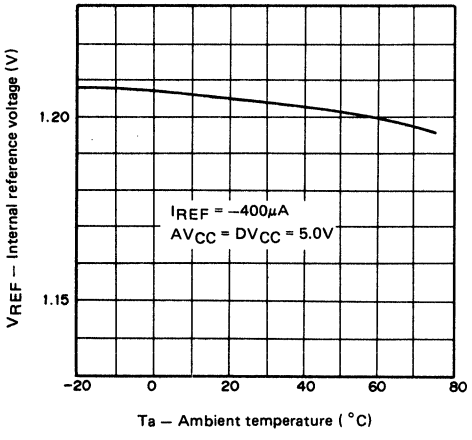
Output voltage full-scale vs. Power supply voltage



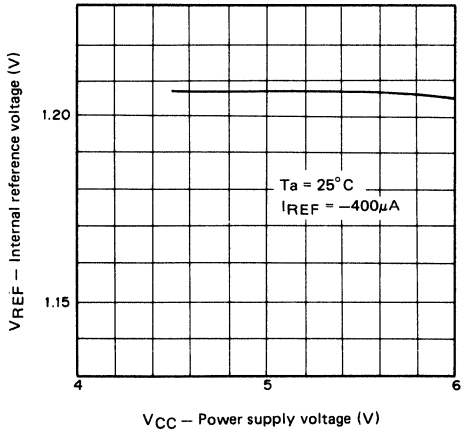
Output zero offset voltage vs. Power supply voltage



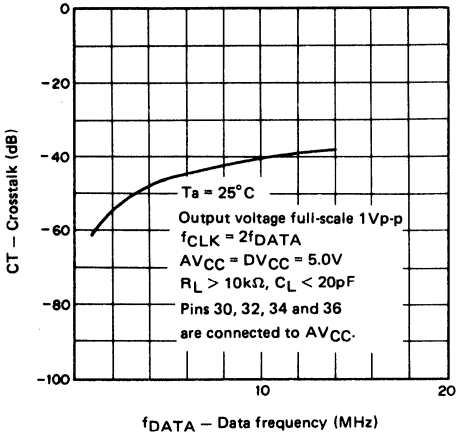
Internal reference voltage vs. Ambient temperature



Internal reference voltage vs. Power supply voltage



Crosstalk among R, G and B vs. Data frequency



10/9 bit 20 MHz Sub-ranging A/D Converter

Description

The CX20220A series is a high-speed, 20-MHz A/D converter which comes in two types of resolution, 10-bit and 9-bit, that are distinguished by the number suffixed to the name. Since a series-parallel system is used, an external sample hold circuit is required.

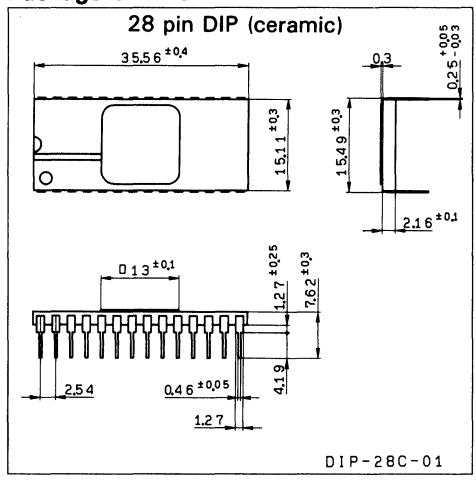
- Resolution: 10 bits (CX20220A-1)
  9 bits (CX20220A-2)
- Maximum conversion rate: 20 MHz
- Digitizing range: 0 to −2V
- Digital input/output: ECL level
- Output code: binary
- Low power consumption: 360 mW

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



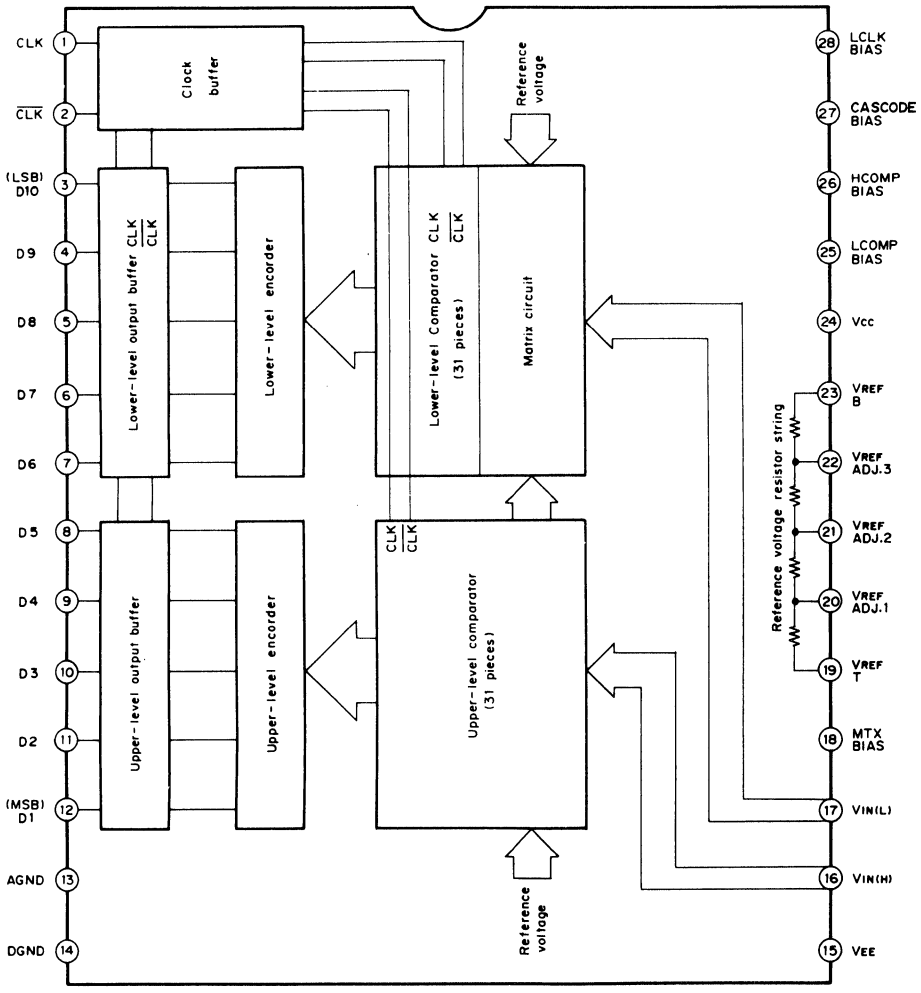
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	2.5	V
	V_{EE}	−7	V
• Analog voltage	V_I	V_{EE} to 0.3	V
• Clock input voltage	V_{CLK}, $V_{\overline{CLK}}$	V_{EE} to 0.3	V
• Reference voltage	V_{REF}	V_{EE} to 0.3	V
• Digital output current	V_{O1} to V_{O10}	0 to −20	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.23	W

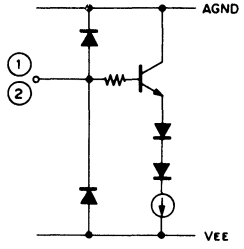
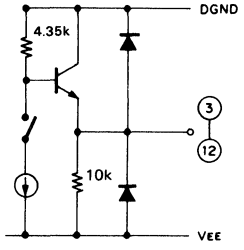
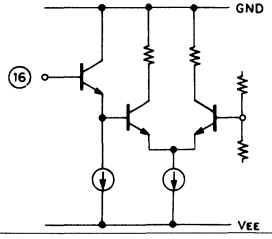
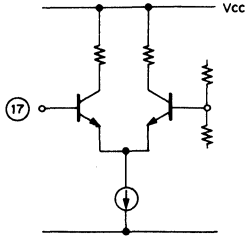
Recommended Operating Conditions

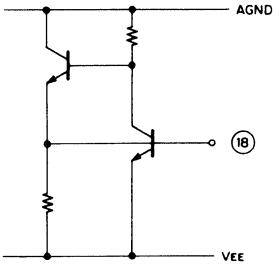
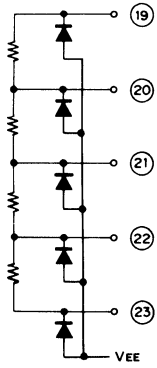
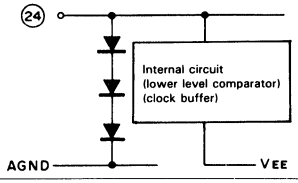
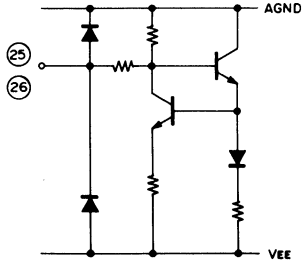
• Supply voltage	V_{CC}	1.6 to 2.1	V
	V_{EE}	−5.25 to −4.75	V
	A_{GND}-D_{GND}	−0.05 to +0.05	V
• Reference voltage	$V_{REF.T}$	0	V
	$V_{REF.B}$	−2.0	V
• Analog input voltage	V_I	$V_{REF.B}$ to $V_{REF.T}$	V
• Clock input voltage	V_{IH}	−1.1 min.	V
	V_{IL}	−1.4 max.	V
• Clock pulse width	T_{PW1}	20 min.	ns
	T_{PW0}	22 min.	ns

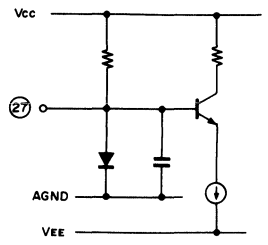
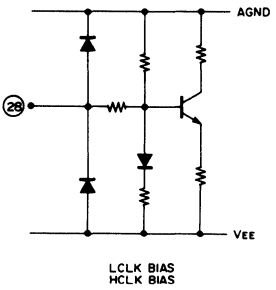
Block Diagram and Pin Configuration (Top View)



Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	CLK		Clock input pin, ECL level.
2	$\overline{\text{CLK}}$		Inverse clock input pin, ECL level
3	D10(LSB)		Digital output pin, ECL level, pull-down resistor (10KΩ) built in.
4	D9		
5	D8		
6	D7		
7	D6		
8	D5		
9	D4		
10	D3		
11	D2		
12	D1(MSB)		
13	AGND		Analog ground pin
14	DGND		Digital ground pin
15	VEE		Power supply pin. To be grounded with ceramic chip capacitor of 0.1 μF or over.
16	VIN(H)		Analog input pin (Upper level)
17	VIN(L)		Analog input pin (Lower level)

No.	Symbol	Equivalent circuit	Description
18	MTX BIAS		Pin connected internal matrix, which is normally used open.
19	VREF.T		Reference voltage pin (top), 0 V (typ.)
20	VREF ADJ. 1		Reference voltage adjusting pin. To be grounded with ceramic chip capacitor of 0.1μF or over.
21	VREF ADJ. 2		
22	VREF ADJ. 3		
23	VREF.B		Reference voltage pin (bottom), −2 V (typ.) To be grounded with ceramic chip capacitor of 0.1 μF or over.
24	VCC		Internal power supply pin. Three diodes are incorporated in series, so that by connecting pull-up resistor to +5V.
25	LCOMP BIAS		Pin connected internal lower level comparator, which is normally used open.
26	HCOMP BIAS		Pin connected internal upper level comparator which is normally used open.

No.	Symbol	Equivalent circuit	Description
27	CASCODE BIAS		Cas code bias pin. To be bypassed to GND with ceramic capacitor of 0.1 μF or over.
28	LCLK BIAS		Pin connected internal lower level buffer, which is normally used open.

Electrical Characteristics 1 (See the Electrical Characteristics Test Circuit)

CX2022A-1 (Ta = 25°C, VCC = 1.6V, VEE = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								10		bit
Differential linearity error	EO	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	EL	A	A	A	D	Differential waveform output				±1	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc = 14.32 MHz nonlock		0.7		%
Differential phase error	DP	A	A	A		DA output			0.3		deg

CX2022A-2

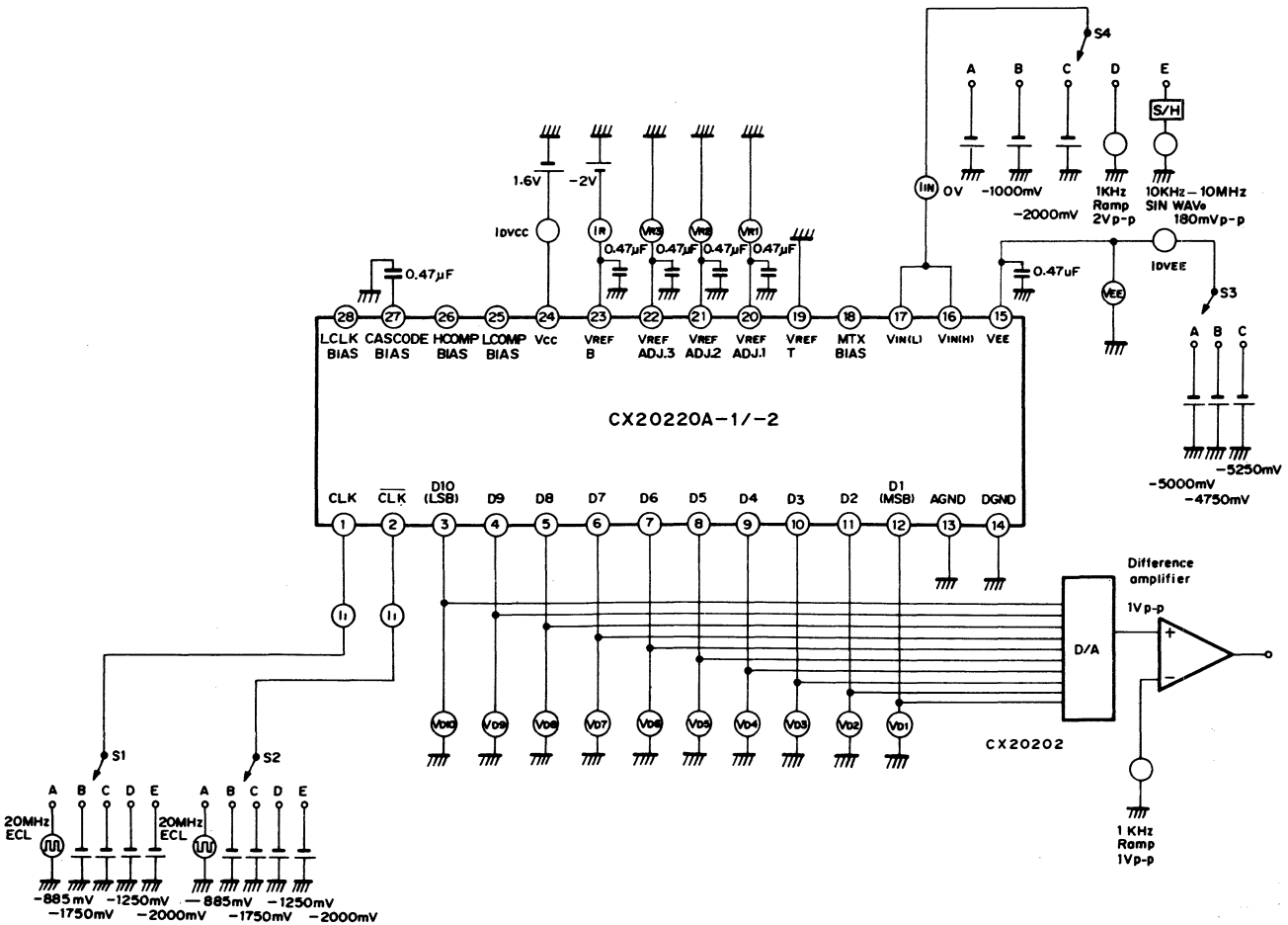
Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								9		bit
Differential linearity error	EO	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	EL	A	A	A	D	Differential waveform output				±1/2	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc = 14.32 MHz nonlock		1.0		%
Differential phase error	DP	A	A	A		DA output			0.5		deg

Electrical Characteristics 2 (See the Electrical Characteristics Test Circuit)

($Ta = 25°C$, $V_{CC} = 1.6V$, $V_{EE} = -5V$)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Conversion rate	f_{max}	A	A	A	D	DA output		20			MSPS
Power consumption(1)	I_{DVCC}	B	D	A	A	I_{DVCC}			17	25	mA
Power consumption(2)	I_{DVEE}	B	D	A	A	I_{DVEE}		−80	−60		mA
Resistor string current	I_{REF}	B	D	A	A	I_R		−14	−12.5		mA
Resistor string pin voltage (1)	V_{R1}	B	D	A	A	V_{RI}		−0.51	−0.5	−0.49	V
Resistor string pin voltage (2)	V_{R2}	B	D	A	A	V_{R2}		−1.01	−1.0	−0.99	V
Resistor string pin voltage (3)	V_{R3}	B	D	A	A	V_{R3}		−1.51	−1.5	−1.49	V
Offset voltage, V_{RT} side	E_{OT}	B	C	A	A				2		mV
Offset voltage, V_{RB} side	E_{OB}	B	C	A	A				4		mV
Analog input current	I_{IN}	B	D	A	A	I_{IN}			40	80	μA
Analog input capacity (1)	C_{IN}	A	A	A			SW4: V_{IN} = 0V + 0.07 Vrms 4 MHz		230		pF
Analog input capacity (2)	C_{IN}	A	A	A			V_{IN} = −2V + 0.07 Vrms 4 MHz		190		pF
Analog input bandwidth	BW	A	A	A	E	DA output	Measurement of output amplitude		10		MHz
Digital input current (1)	I_{IH}	B	C	A	A	I_I			5	8	μA
Digital input current (2)	I_{IL}	E	D	A	A	I_I			5	8	μA
Inverse digital input current (1)	I_{IH}	C	B	A	A	I_I			5	8	μA
Inverse digital input current (2)	I_{IL}	D	E	A	A	I_I			5	8	μA
Digital output voltage, H level (1)	V_{IL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor.	−0.9	−0.8		V
Digital output voltage, H level (2)	V_{OH}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.0		V
Digital output voltage L level (1)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		−1.6	−1.5	V
Digital output voltage, L level (2)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.9		V
Output data delay (1)	T_d	A	A	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		10		ns
Output data delay (2)	T_d	A	A	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω		5		ns

Electrical Characteristic Test Circuit

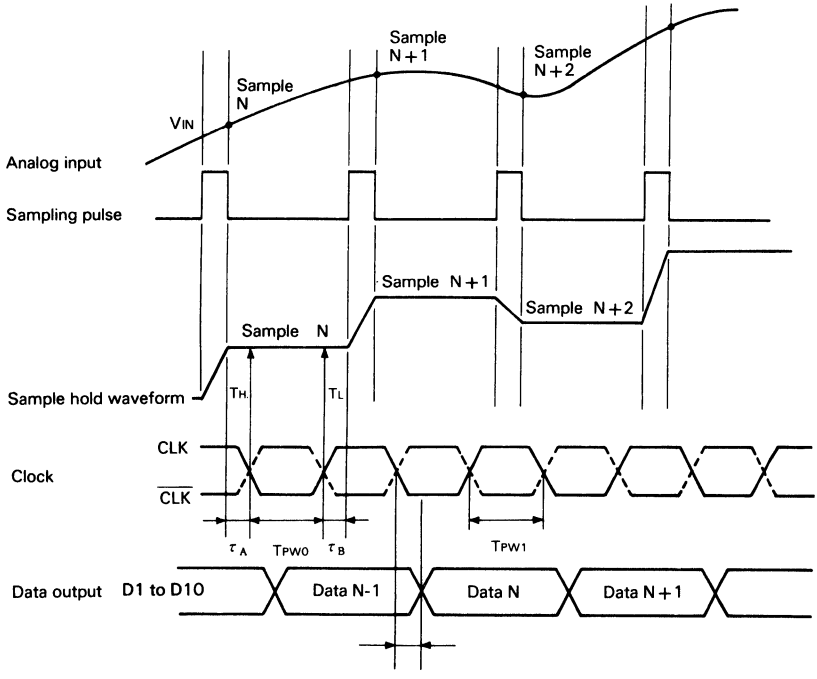


SONY.

Reference Data for Standard Circuit Design

Clock Timing

CX20220A-1/-2 is a series-parallel-type A/D converter, and therefore an external sample and hold circuit is required. Careful timing, design should be made according to the timing chart shown below. The timing design between the S/H output and the A/D clock is important.



Clock Timing

$\tau_A \geqq \tau_A$ (Aperture time + setting time of sample and hold circuit)

$\tau_B \geqq$ 2ns

$\tau_{PW0} \geqq$ 22ns

$\tau_{PW1} \geqq$ 20ns

TH is the timing in which the upper level comparator compares VIN and VREF and latches the result. TL is the timing in which the lower level comparator compares VIN and VREF and latches the result. The simple method is for output data to be latched upon rising edge of CLK. Clock duty should be chosen so that the DG and DP perform the best result.

Digital Output (CX20220A-1)

In the output stages (pins 3 through 12), 10 kΩ pull-down resistors are built in. A 1kΩ or larger resistance can further be connected to it externally.

D1 = MSB, D10 = LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB 1 2 3 4 5 6 8 8 9 10 LSB
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1 1
.	1	1 1 1 1 1 1 1 1 1 0
.	2	1 1 1 1 1 1 1 1 0 1
.	.	.
.	.	.
.	.	.
.	5 1 1	1 0 0 0 0 0 0 0 0 1
.	5 1 2	1 0 0 0 0 0 0 0 0 0
.	5 1 3	0 1 1 1 1 1 1 1 1 1
.	.	.
.	.	.
.	.	.
.	1 0 2 2	0 0 0 0 0 0 0 0 0 1
$V_{REF.B}$	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Digital Output (CX20220A-2)

D1 = MSB, D9 = LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB 1 2 3 4 5 6 8 8 9 LSB
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1
.	1	1 1 1 1 1 1 1 1 0
.	2	1 1 1 1 1 1 1 0 1
.	.	.
.	.	.
.	.	.
.	2 5 5	1 0 0 0 0 0 0 0 1
.	2 5 6	1 0 0 0 0 0 0 0 0
.	2 5 7	0 1 1 1 1 1 1 1 1
.	.	.
.	.	.
.	.	.
.	5 1 0	0 0 0 0 0 0 0 0 1
$V_{REF.B}$	5 1 1	0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Ground Pin (AGND, DGND)

When mounting the converter on a printed circuit board, take as much space as possible for GND, to reduce impedance and resistance.

Power Supply Pin (VEE)

The VEE pin should be bypassed in the shortest way to AGND with a 0.1 μF or larger ceramic chip capacitor.

Power Supply Pin (VCC)

This is an internal power supply pin. Three diodes are incorporated in it in series, as shown in the equivalent circuit diagram, and its lower end is connected to AGND. Therefore, any desired VCC can be obtained by connecting a pull-up resistor to +5V. Be careful not to connect a capacitor between this pin and GND, because oscillation may result.

Reference Voltage Pin

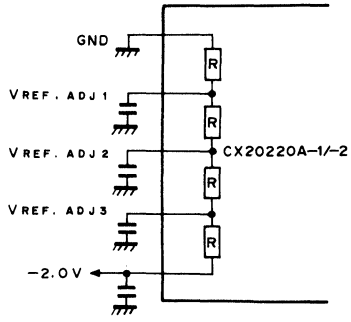
From this pin the reference voltage is supplied to the upper level and lower level comparators. Normally, VREF.T should be connected to GND, and VREF.B to −2.0V, respectively.

The interval between VREF.T and VREF.B constitutes a resistance of approximately 150 Ω, and upon application of −2.0V a current of approximately 13 mA will flow in it.

Any leakage of CLK to the reference voltage will deteriorate the characteristics of the converter. To avoid this, it should be bypassed to AGND with a tantalum capacitor of 47 μF or over plus a ceramic chip capacitor of 0.1 μF or over.

Linearity Adjusting Pin (VREF.ADJ)

Adjusting pins are extended from reference resistors as shown below. Normally, these pins are connected to AGND with a 0.1 μF or larger ceramic chip capacitor. When adjustments are needed, connect them to AGND or VREF.B via resistance.



Sample & Hold Circuit

As noted in the explanation of the clock timing, it is desirable that the sample and hold circuit has some allowance for TA. A sample and hold circuit based on a diode bridge switch may be used which performs the best result.

For more information, see Application Circuit (2).

Analog Input

Since CX20220A-1/-2 has an analog input capacitance of approximately 230pF, the buffer amplifier used to drive it must have a sufficient drive capability. Note that, if driven by a low-output-impedance buffer amplifier, a parasitic oscillation may result. This can be prevented by inserting a resistor of about 10 to 30 Ω between the output of the buffer amplifier and the A/D input in series.

Clock Input

The clock input is a complementary configuration.
Normally it should be driven with ECL circuit with complementary output.

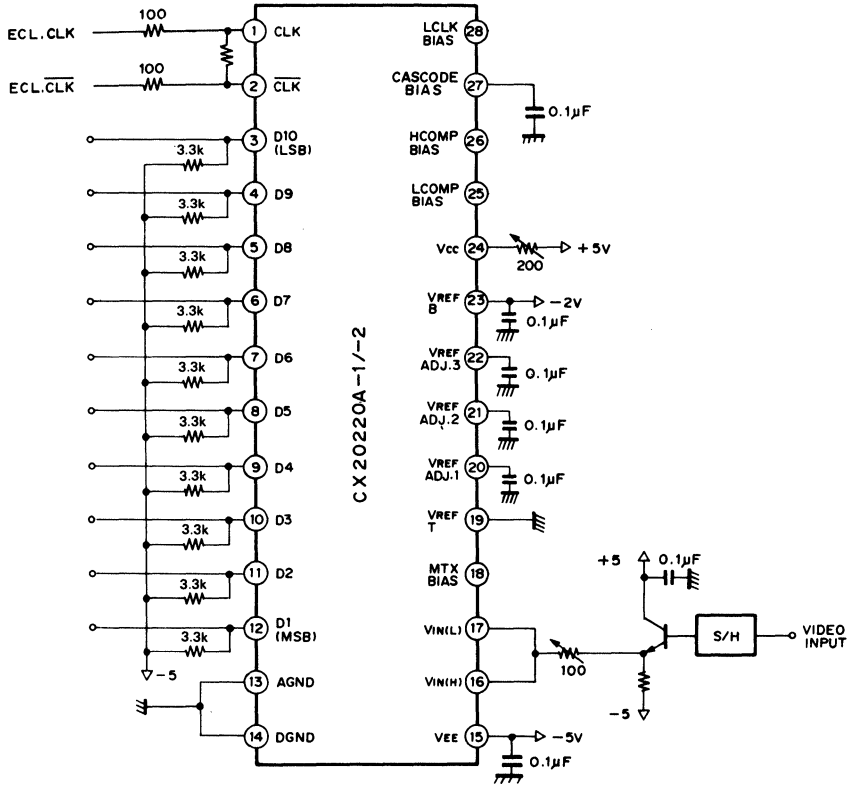
Digital Output (D1 through D10)

Although a 10k Ω pull-down resistor is built into the digital output stage, a 1k Ω or larger resistor can further be connected to it externally. In this case, however, care must be taken about changes in output level.

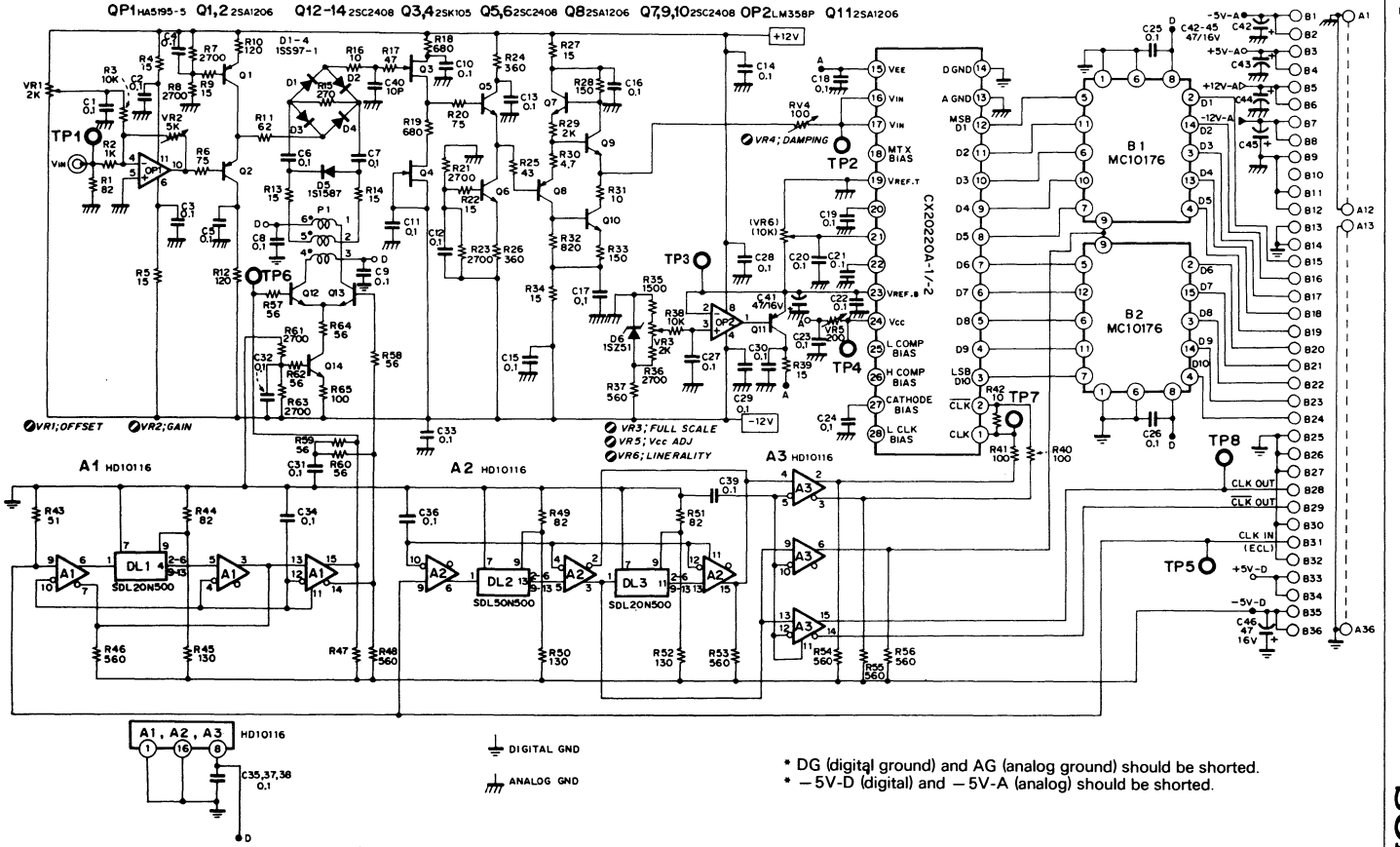
Other

Pin 18 (MTX BIAS), pin 25 (LCOM BIAS), pin 26 (HCOMP BIAS) and pin 28 (LCLK BIAS) are not used. These pins should never be connected to GND, power supply or any other pins.

Application Circuit (1)



Application Circuit (2)



* DG (digital ground) and AG (analog ground) should be shorted.
* −5V-D (digital) and −5V-A (analog) should be shorted.

SONY

Comparative Description of the System

CX20220A-1/-2 is based on a new series-parallel type. The following is a comparative explanation of the conventional and the new series-parallel types.

Series-Parallel Type (Conventional)

The series-parallel-type A/D converter is designed to accomplish A/D conversion in two steps, as shown in Fig. 1. With a 10-bit device, the level of the analog signal held in the sample hold (S/H) circuit is converted into a first set of parallel 5-bit digital output. This digital output is at the same time converted back into an analog signal, corresponding to the upper 5 bits. The difference between this signal and the level held at input is converted into digital signals in the parallel 5-bit A/D converter at the next stage, resulting in digital output for the lower 5 bits.

The number of comparators required for this system is $(2^5 - 1) \times 2 = 62$ pcs., bringing about a dramatic reduction in circuit size as compared to the 10-bit parallel type. However, since it does A/D conversion twice, once for the upper level and then again for the lower level, it takes longer conversion time, and also requires an S/H circuit to hold the input analog signal so that its level does not change when the lower 5 bits are being converted, in addition both the 5-bit D/A converter and the subtractor, shown in Fig. 1, are required to possess a 10-bit equivalent accuracy.

New Series-Parallel Type

Essentially the new series-parallel-type A/D converter aims to reduce the number of comparators by doing A/D conversion twice, once for the upper bits and again for the lower bits, as in the case of the conventional series-parallel type. The distinguishing feature of this system, however, is that it does not require the D/A converter and the subtractor as shown in Fig. 2. Simply speaking this system is designed so that the input level held in the S/H circuit is first A/D converted for the upper 5 bits, and upon receipt of control signal from the upper level encoder, the lower level A/D converter is operated.

To simplify the operating principle of this system, Fig. 3 shows an example which consists of an upper 2 bits and lower 2 bits, a total of 4 bits. The upper and lower level circuits each consist of three comparators, switch trains S1 through S4, a single 16-segmented resistor, and an encoder.

Input level V_{IN} held by the S/H circuit is determined by the upper level comparator to be at a level of $V_{REF.T}$ to V_1, V_1 to V_1 to V_2, V_2 to V_3, or V_3 to $V_{REF.B}$. The result of judgement is converted into upper 2-bit digital output through the upper level encoder. At the same time, one of the switch trains S1 to S4 is turned on, according to the level of V_{IN}. As it switches on, reference voltage is supplied to the lower level comparator, and elaborate comparative judgement is made at the interval of ($V_{REF}/4$), resulting in output of the lower 2 bits from the lower level encoder.

Since this system uses the same resistor strings in common for the upper and lower levels, simplicity is maintained. Furthermore, since this system requires fewer comparators, input bias current for the comparators is reduced accordingly.

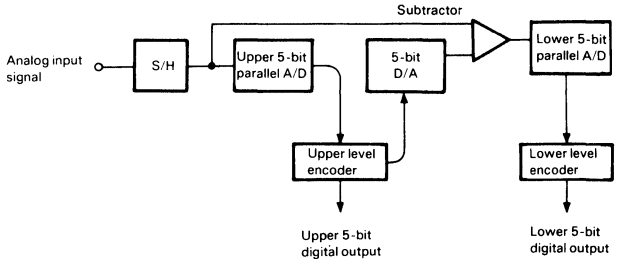


Fig. 1 Configuration of Series-Parallel 10-Bit A/D Converter

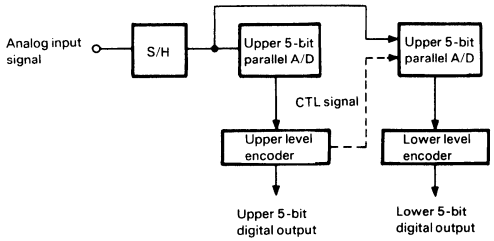


Fig. 2 Configuration of the New Series-Parallel 10-Bit A/D Converter

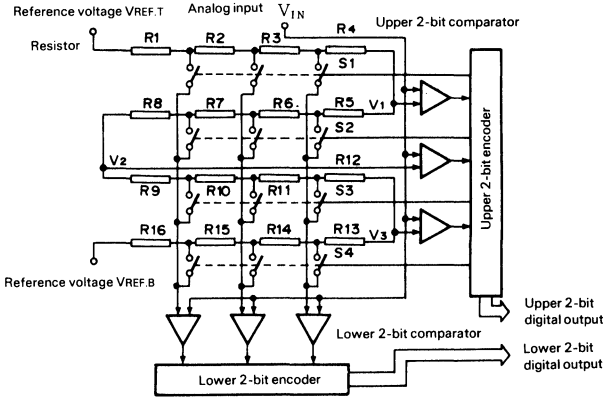


Fig. 3 Operating Principle of the New Series-Parallel Type (Ex.: 4-bit device)

High-speed Sample and Hold Amplifier

Description

CXA1008P/1009P are bipolar IC's developed for the purpose of sample holding video signals and other signals at high-speed.

Features

- Maximum sampling frequency
  - CXA1008P 35 MHz
  - CXA1009P 18 MHz
- Linearity 0.08% (Typ.)
- Clock input level ECL compatible
- Low power consumption
  - CXA1008P 680 mW (Typ.)
  - CXA1009P 420 mW (Typ.)

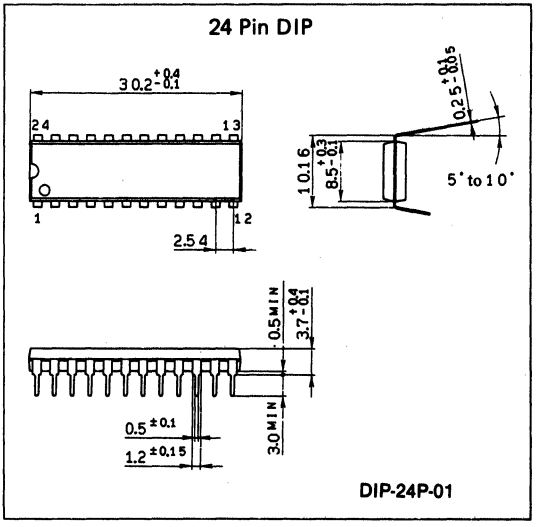
Structure

- Monolithic silicon bipolar IC.

Applications

- A/D converter and other analog signal processing
- Other general applications.

Package Outline Unit: mm



Function

High-speed hold circuit, wide band 6 dB amplifier, A/D reference power supply, A/D clock output circuit.

Absolute Maximum Ratings ($T_a = 25°C$)

• Supply voltage	V_{CC}	+5.5	V
	V_{EE}	−6.0	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	1.2	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	+4.75 to 5.25V
	V_{EE}	−4.75 to −5.45V

Block Diagram

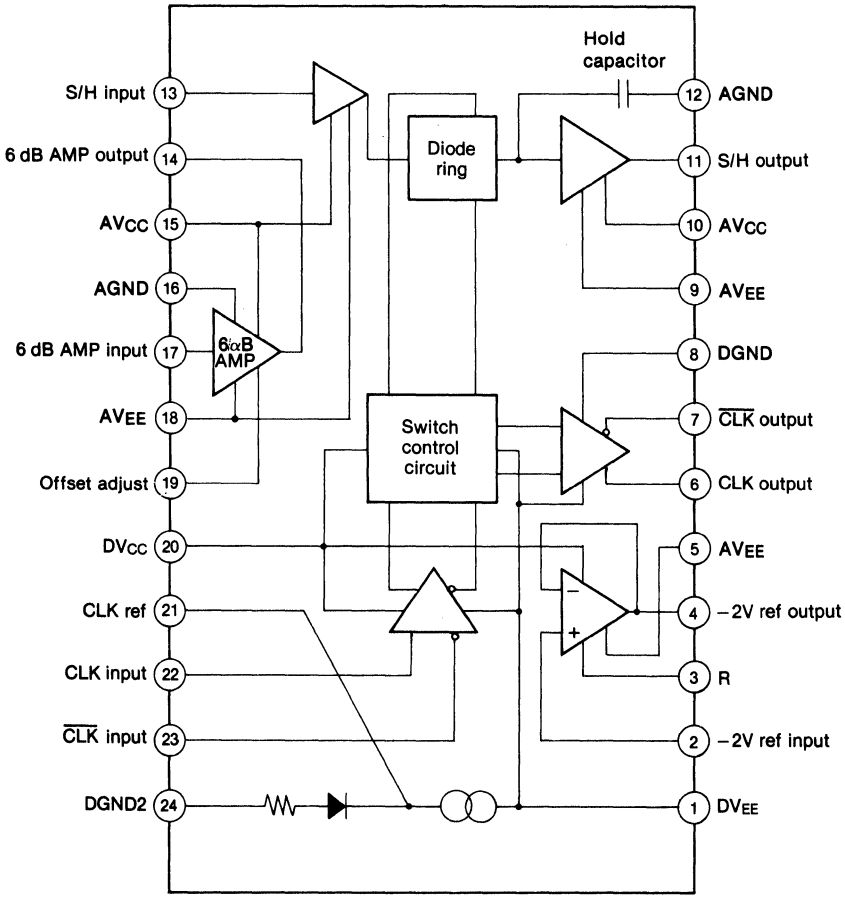
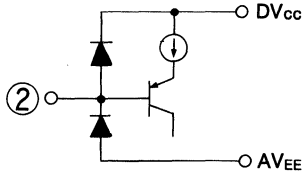
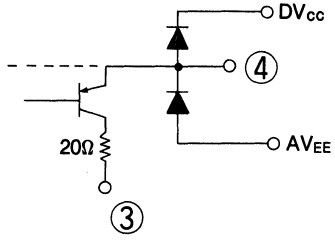
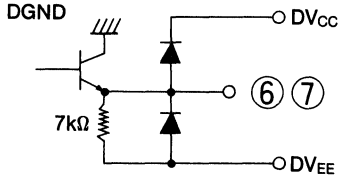
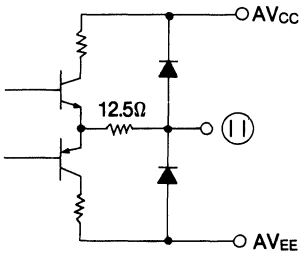
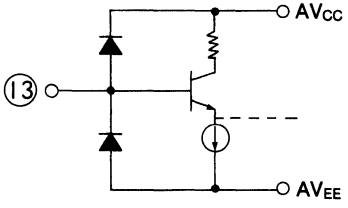
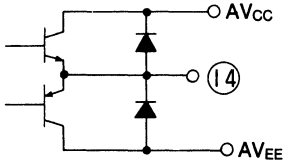
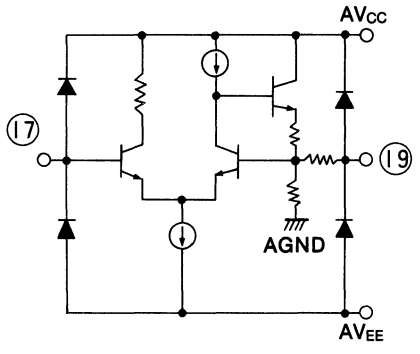
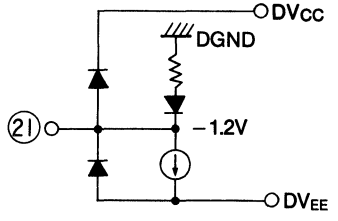
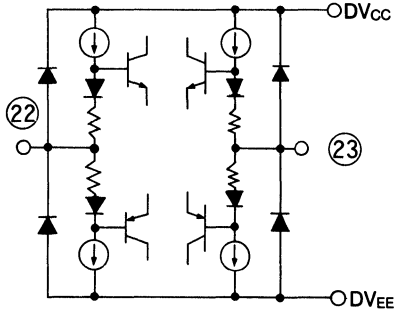


Fig. 1

Terminal Function and Equivalent Circuits

Pin No.	Symbol	Equivalent circuit	Function
1	DV_{EE}		Digital V_{EE} (−5V)
2	−2V ref input		reference voltage input for A/D converter
3	R		Pulldown terminal for external R (30Ω typically)
4	−2V ref output		reference voltage output for A/D converter
5	AV_{EE}		Analog V_{EE} (−5V)
6	CLK output		CLK output for A/D converter
7	$\overline{CLK}$ output		$\overline{CLK}$ output for A/D converter
8	DGND		Digital GND
9	AV_{EE}		Analog V_{EE} (−5V)
10	AV_{CC}		Analog V_{CC} (+5V)

Pin No.	Symbol	Equivalent circuit	Function
11	S/H output		S/H output
12	AGND		Analog GND
13	S/H input		S/H input
14	6dB AMP output		Olutput terminal of 6dB amplifier
15	AVCC		Analog VCC (+5V)
16	AGND		Analog GND

Pin No.	Symbol	Equivalent circuit	Function
17	6dB AMP input		6dB AMP input
18	AV_{EE}		Analog V_{EE} (−5V)
19	offset adjust		6dB AMP DC offset adjust terminal
20	DV_{CC}		Digital V_{CC} (+5V)
21	CLK ref		CLK reference output
22	CLK input		CLK input (Note: connect to (21) PIN or input ECL CLK signal)
23	$\overline{CLK}$ input		$\overline{CLK}$ input (Note: input ECL $\overline{CLK}$ signal)
24	DGND		Digital GND

CXA1008P

Electrical Characteristics

S/H section (see Fig. 3) (Ta = 25°C, V_{CC} = +5V, V_{EE} = −5V)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		$V_{CLK\ REF}$	−1.3	−1.2	−1.1	V
Analog input voltage range	△V < 1.2V *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power Supply		I_{CC}	48	60	78	mA
	without −2V ref.	I_{EE1}	48	60	78	mA
	with −2V ref. R_{LI} = 50Ω *2	I_{EE2}	80	100	125	mA
Input bias current	−2V < V_{in} < 2V	I_{Biass}		15	30	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	V_{in} = $2V_{p-p}$ (−3dB)	BW		12		MHz
Power supply rejection ratio		SVR_S		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	V_{in} = 0V	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	20	mV/μs
Acquisition time	△V = 1.2V	Taq		8	12	ns
Settling time	see the TIMING CHART	T_{set}		25		ns
DC offset voltage	f_{CLK} = 5MHz	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	35			MHz
Minimum sampling frequency		f_{CLKL}			5	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE mode ramp. f_{CLK} = 20MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

(R_{LI} = 50Ω. see Fig. 3)

CXA1009P

Electrical Characteristics

S/H section (see Fig. 3)

(Ta = 25°C, V_{CC} = +5V, V_{EE} = −5V)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		$V_{CLK\ REF}$	−1.3	−1.2	−1.1	V
Analog input voltage range	△V < 1.2V *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power supply		I_{CC}	25	35	45	mA
	without −2V ref.	I_{EE1}	25	35	45	mA
	with −2V ref. R_{LI} = 50Ω *2	I_{EE2}	60	75	98	mA
Input bias current	−2V < Vin < 2V	I_{Biass}		9	18	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	V_{in} = $2V_{p-p}$ (−3dB)	BW		6		MHz
Power supply rejection ratio		SVRs		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	Vin = 0V	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	10	mV/μs
Acquisition time	△V = 1.2V	Taq		12	20	ns
Settling time	see the Timing Chart	T_{set}		36		ns
DC offset voltage	f_{CLK} = 5MHz	V_{offset}		±15	±100	mV
Maximum sampling frequency	MHz	f_{CLKH}	18			MHz
Minimum sampling frequency		f_{CLKL}			2	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE more ramp f_{CLK} = 15MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

*1 △V is voltage change during one sampling period.

*2 Power consumption is I_{CC} × 5V + I_{EE1} × 5V + 40mA × 1.8V.

*3 Input voltage waveform

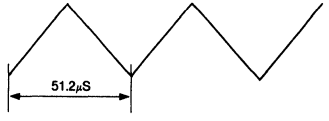


Fig. 2

6dB amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Intput voltage range	*3	V_{INA}	−1.3		+0.8	−1.3		+0.8	V
Band width (−3dB)	V_{in} = IV_{pp}	W	45	55		15	25		MHz
Input bias current	−1V < V_{in} < 1V	$I_{Bias\ A}$		9	20		5	10	μA
Output impedance		Z_{OA}		4	10		4	10	Ω
Voltage gain	*4	G_{VA}	5.1	6.0	6.9	5.1	6.0	6.9	dB
Power supply rejection ratio		SVR_A		−40			−40		dB

*3 2ndary harmonic: −40dB f_{in} = 3.58MHz
*4 f_{in} = 3.58MHz V_{in} = $1V_{p-p}$

CLK OUT section (see Fig. 3)

Item		Condition	Symbol	CXA1008P			CXA1009P			Unit
				Min.	Typ.	Max.	Min	Typ.	Max.	
Output voltage	Amplitude	R_{L2} = 1.5 KΩ see Fig. 3	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low level		V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time			tr		7	10		7	10	ns
Fall time			tf		5	8		5	8	ns
CLK Delay 1			τ_{D1}	20	28	34	36	38	45	ns
CLK Delay 2			τ_{D2}	14	22	28	24	26	33	ns

$-2V_{ref}$ amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Voltage gain ratio	V_{ref} = −2V R_{LI} = 50Ω	G_{VR}	0.9	1.0	1.1	0.9	1.0	1.1	
Input bias current	−3V < V_{in} < 0V	$I_{Bias\ R}$		5	10		5	10	μA
Output impedance		Z_{OR}		2	10		2	10	Ω

Electrical Characteristics Measuring Circuit

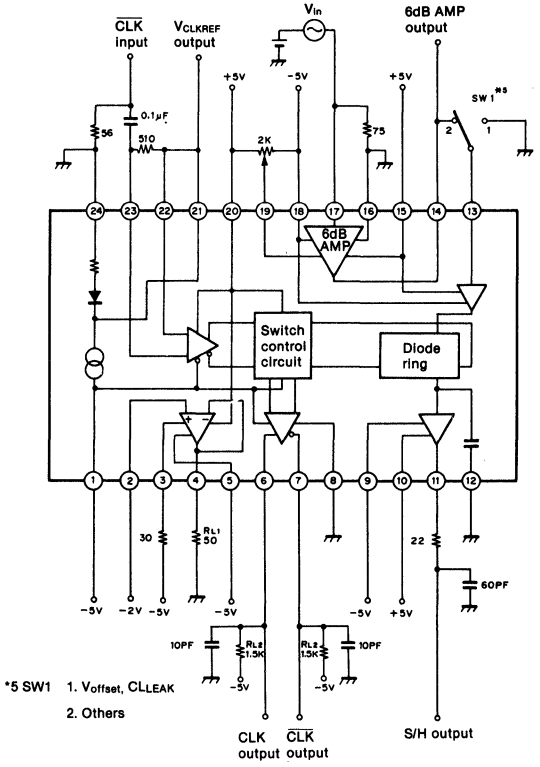


Fig. 3

Timing Chart

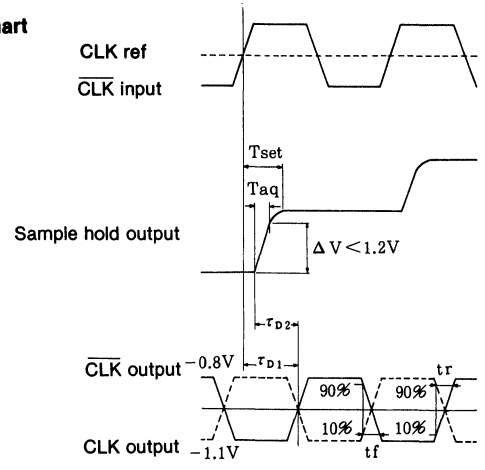


Fig. 4

Description of Functions

CXA1008P/1009P are the monolithic ICs incorporating a high-speed sample hold circuit, a wide band 6 dB amp, reference power supply for A/D converter, and a clock output section, and operate up to a sampling frequency of 35/18 MHz.

CXA1008P/1009P can compose in 20/15 MS/s A/D converter system in combination with a CX20052A. CXA1008P/1009P form, with the input of a single phase or 2-phase ECL clock input, a new sampling signal. For this reason, the sampling period remain unchanged even when the frequency or duty of the input sampling CLK signal changes.

- Wide band 6 dB AMP.

  In-phase amp with a band width over 45/15 MHz amplifies ordinary TV signal (1Vp-p) to a 2Vp-p signal which gives the highest accuracy when processed in CX20052A.

- CLK output section

  When used in combination with an A/D converter such as CX20052A, the CLK timing between the S/H circuit and the A/D converter needs to be adjusted, and up to 20/15 MHz, CXA1008P/1009P generate CLK timing signals for driving the A/D converter, and output 2-phase CLK at 300 mVp-p from pins 6 and 7. With this output, no separate CLK is required to combine with an A/D converter.

- CXA1008P/1009P incorporate a buffer amp to provide a reference voltage for the A/D converter.

Application Circuit

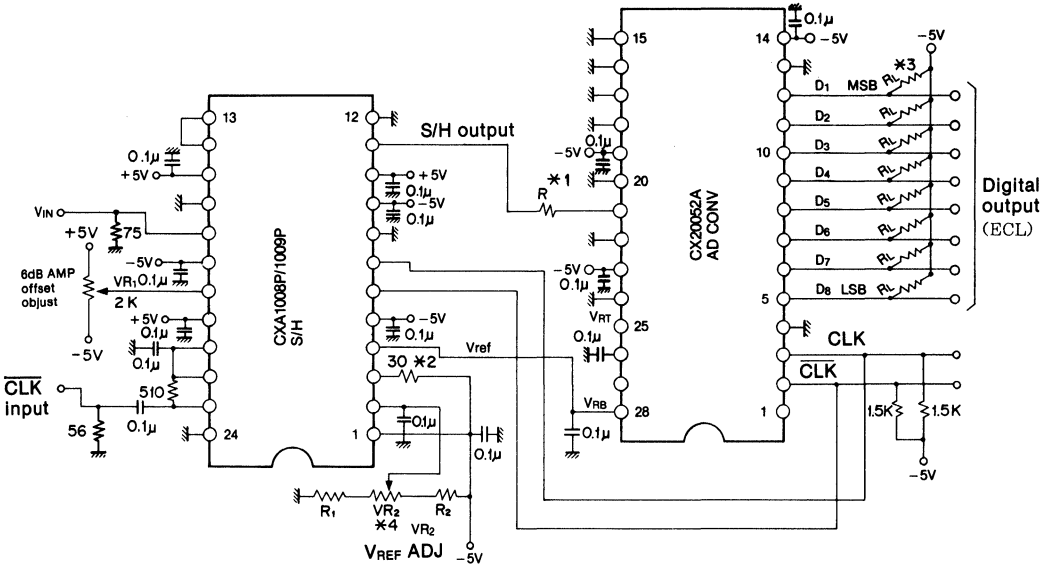


Fig. 5 Connection of CXA 1008P/1008P with CX20052A (1)

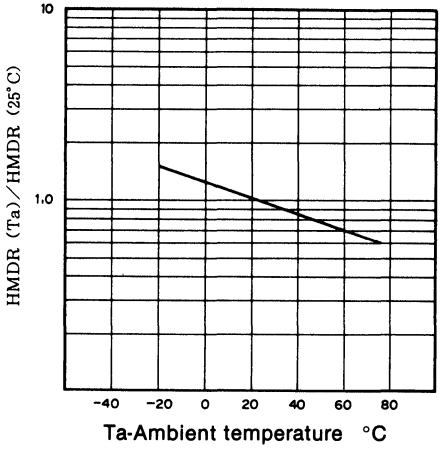
*1 R is a ringing preventing resistor. Select between 10 to 50Ω
*2 Pulldown R for V_{ref}
*3 R_L = 4.3kΩ
*4 R_1 = 1kΩ, VR_2 = 2kΩ, R_2 = 2kΩ

Notes on Application

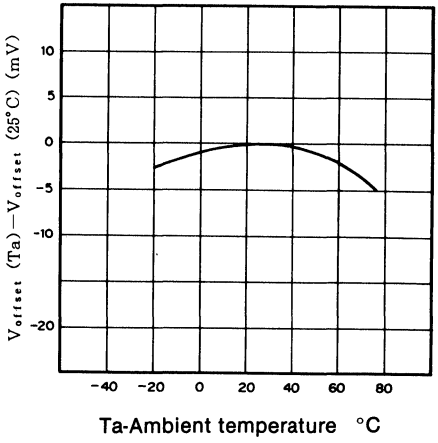
1. Unless sufficiently stable power supply and GND voltage in the high-frequency range are used, the device characteristics deteriorates. For this reason, bring the power supply bypass capacitor as near to this IC as possible, and make the pattern to the power supply and to the earth terminal as wide as feasible.
2. To reduce CLK leak, use waveforms similar to sine waves as far as possible, up to the CLK input. For satisfactory operation, a CLK input ampritude of around 300mV is enough.
3. When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

Changes in Characteristics with Temperature

Hold Mode Droop Rate

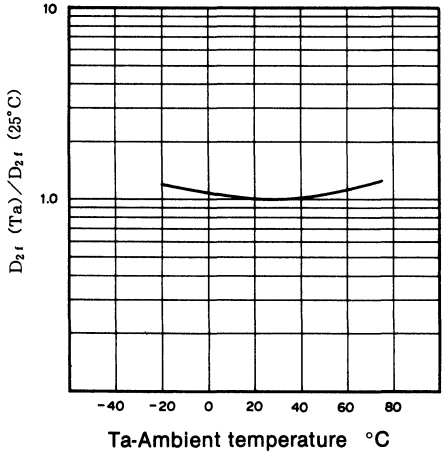


Offset Voltage Between S/H Input & Output

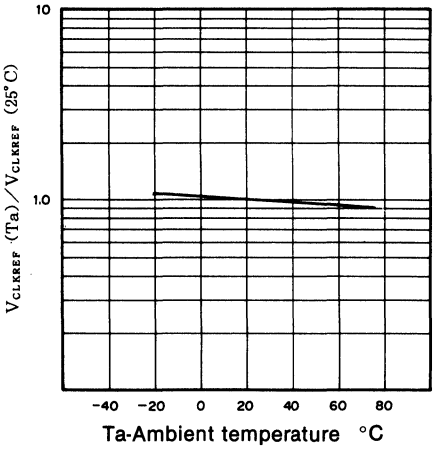


6dB AMP 2ndary Harmonic Level

(3.58MHz, Vin = $1V_{pp}$)



CLK Ref Voltage



SONY

CXA1016P/CXA1016K/CXA1016UK/ CXA1056P/CXA1056K/CXA1056UK

8 bit 30/50 MHz Flash A/D Converter

Description

CXA1016P/CXA1016K/CXA1016UK/CXA1056P/ CXA1056K/CXA1056UK are 8 bit high-speed A/D converter ICs for various applications. They can be used widely for various purposes which require high-speed A/D conversions.

CXA1016P/CXA1056P are assembled in the plastic DIP packages and CXA1016K/CXA1056K are in the ceramic lead-less chip carriers.

CXA1016UK/CXA1056UK are high reliability versions of CXA1016K/CXA1056K with extended temperature range (−55 to +125°C) and bias burn-in (72 hours at 125°C).

Features (CXA1016P/CXA1016K/CXA1016UK)

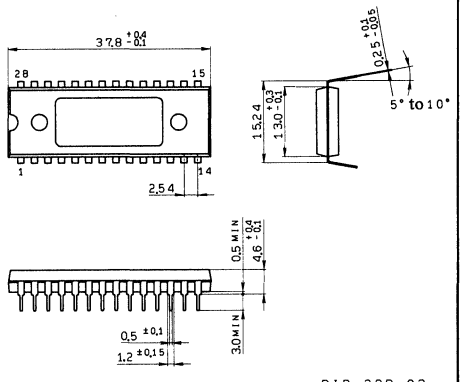
- Resolution 8 bits ± 1/2 LSB
- High-speed operation Maximum conversion Rate 30 MS/s
- Wide analog input bandwidth 15 MHz (−3 dB)
- Low input capacitance 35 pF (typ)
- Low power consumption 420 mW (typ)

Features (CXA1056P/CXA1056K/CXA1056UK)

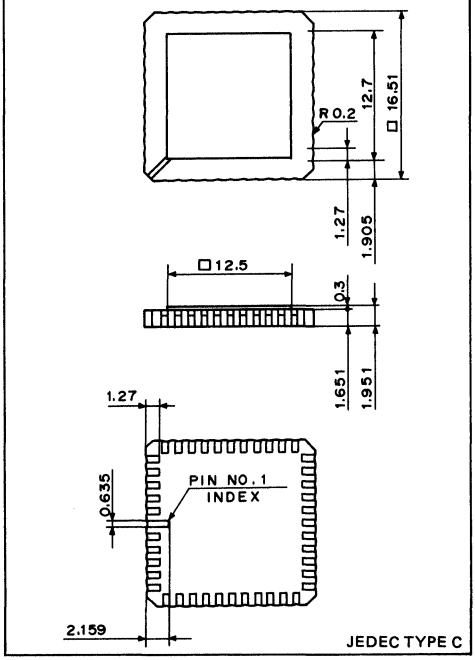
- Resolution 8 bits ± 1/2 LSB
- High-speed operation Maximum conversion Rate 50 MS/s
- Wide analog input bandwidth 25 MHz (−3 dB)
- Low input capacitance 35 pF (typ)
- Low power consumption 550 mW (typ)

Package Outline Unit: mm

CXA1016P/CXA1056P 28 Pin DIP



CXA1016K/CXA1016UK
CXA1056K/CXA1056UK 44 Pin contact chipcarrier



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	0 to −7	V
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	0.5 to V_{EE}	V
	$\lvert V_{RT}-V_{RB} \rvert$	2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to −4	V
• VRM pin input current	I_{VRM}	−3 to +3	mA
• Digital output current	ID_0 to ID_7	0 to −10	mA
• Operating temperature	Ta	−20 to +100	°C (CXA1016P/CXA1056P)
	Tc	−25 to +125	°C (CXA1016K/CXA1056K)*1
	Tc	−55 to +125	°C (CXA1016UK/CXA1056UK)*1
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.48	W (CXA1016P/CXA1056P)
		1.08	W (CXA1016K/CXA1016UK/CXA1056K/CXA1056UK)

*1 Heat sinking is required above 100°C (CXA1016K/CXA1016UK)/86°C (CXA1056K/CXA1056UK).

Recommended Operating Conditions (CXA1016P/CXA1016K/CXA1016UK)

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}-DV_{EE}	−0.05	0	0.05	V
	AGND-DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	25			ns
	Tpw0	8			ns

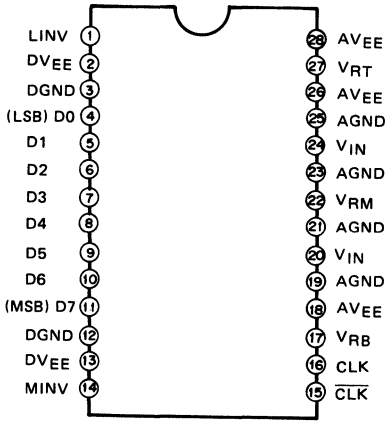
Recommended Operating Conditions (CXA1056P/CXA1056K/CXA1056UK)

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}—DV_{EE}	−0.05	0	0.05	V
	AGND—DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	15			ns
	Tpw0	5			ns

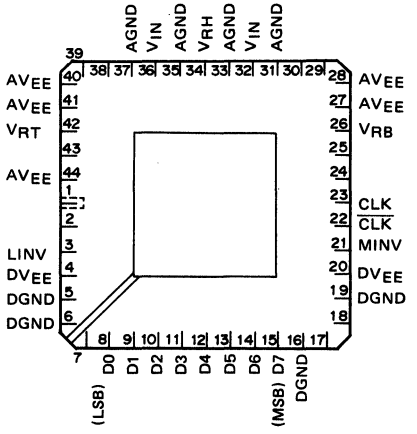
Pin Configuration (Top View)

The pin numbers without indication are empty pins. (not connected)

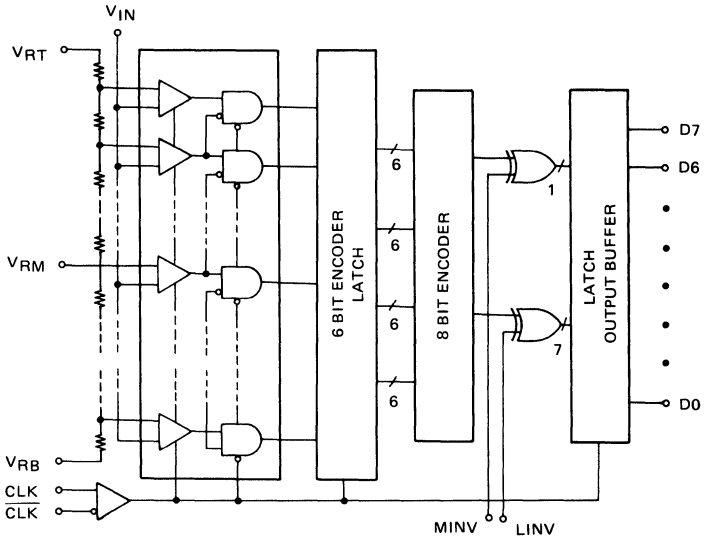
CXA1016P/CXA1056P



CXA1016K/CXA1016UK/
CXA1056K/CXA1056UK



Block Diagram



Pin Description

Symbol	Function
AVEE	Analog VEE, −5.2V (typ). Coupled with −6Ω between DVEE.
LINV	Input pin for output polarity inversion of D0 (LSB) − D6. (See the code table)
DVEE	Digital VEE, −5.2V (typ).
DGND	Digital GND, which is separated from the Analog GND.
D0 − D7	Digital data output pin, ECL level. D0: LSB − D7: MSB. Pull-down resistors are necessary externally.
MINV	Input pin for output polarity inversion of D7 (MSB) (See the code table). ECL level. "0" level is held when it is released.
$\overline{CLK}$	Inverse clock input pin, ECL level.
CLK	Clock input pin, ECL level.
VRB	Reference voltage (bottom), −2V (typ).
AGND	Analog GND
VIN	Analog input, input range is VRT − VRB
VRM	Middle point of the reference voltage, it can be used as a linearity correction pin.
VRT	Reference voltage (top), 0V (typ).
	Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.

Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
−2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}

Electrical Characteristics (CXA1016P/CXA1016K/CXA1016UK)

($Ta=25°C$, $V_{EE}=-5.2V$, $V_{RT}=0V$, $V_{RB}=-2V$)

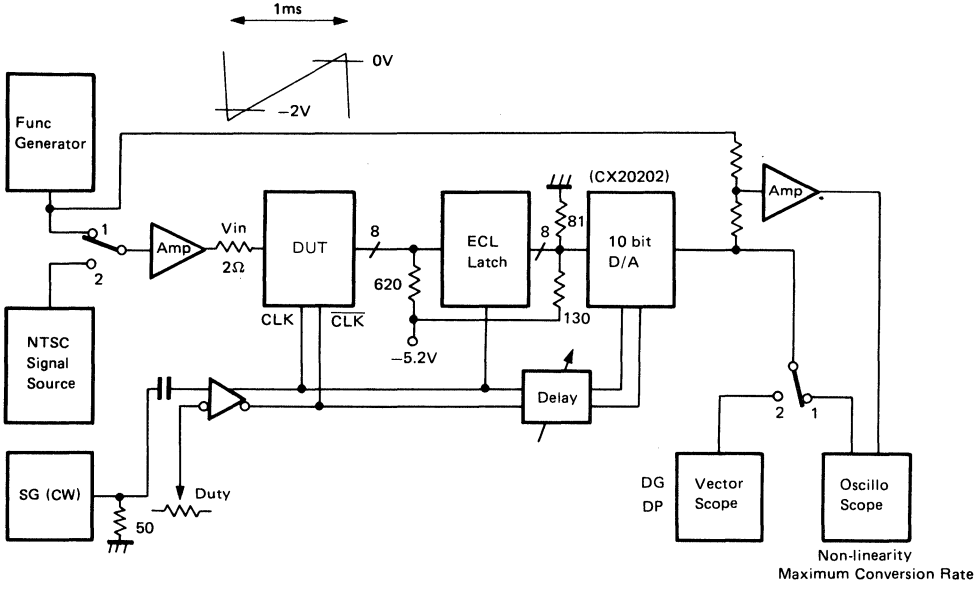
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		F_C	V_{IN}=0 to −2V, fin=1 kHz, ramp	30			MS/s
Supply Current		I_{EE}			−75	−100	mA
Analog Input Capacitance		C_{IN}	$V_{IN}=-1V+0.07$ Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	$V_{IN}=-1V$		60	90	μA
Reference Resistor		Rr ($V_{RT}-V_{RB}$)		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	$V_{IH}=-0.9V$	0		0.4	mA
		I_{IL}	$V_{IL}=-1.75V$	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	$R\ell$=620Ω − V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	$R\ell$=620Ω − V_{EE}		4.0	5.0	ns
Non-linearity Error			F_C=30 MS/s, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			F_C=30 MS/s, 1/16 LSB step ramp			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, F_C=30 MS/s			1.5	%
Differential Phase		DP				0.5	deg.
Aperture Jitter					45		ps

Electrical Characteristics (CXA1056P/CXA1056K/CXA1056UK)

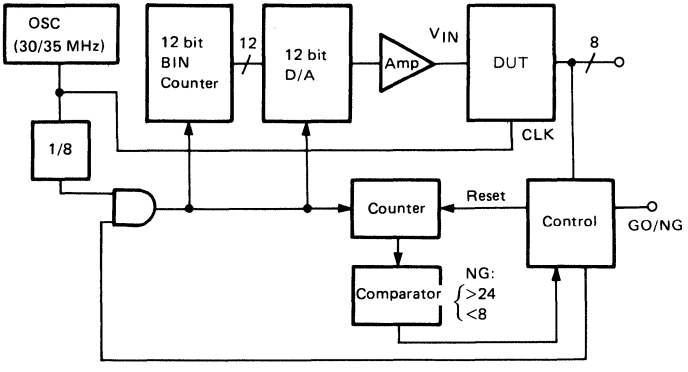
(Ta=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	50			MS/s
Supply Current		I_{EE}			−95	−120	mA
Analog Input Capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	V_{IN}=−1V		75	115	μA
Reference Resistor		Rr (V_{RT}−V_{RB})		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	Rℓ=620Ω − V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	Rℓ=620Ω − V_{EE}		4.0	5.0	ns
Non-linearity Error			Fc=50 MS/s, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			Fc=30 MS/s, 1/16 LSB step ramp			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, Fc=50 MS/s			1.5	%
Differential Phase		DP				0.5	deg.
Aperture Jitter					30		ps

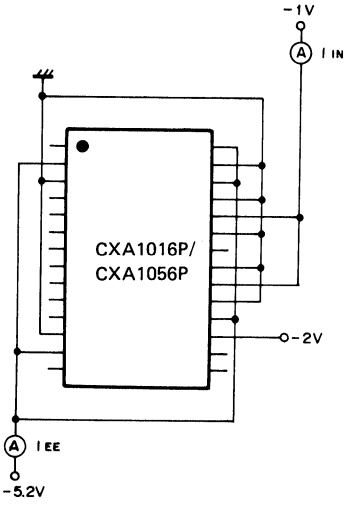
Electrical Characteristics Measuring Circuit
Maximum Conversion Frequency Measuring Circuit
Non-linearity Measuring Circuit
Differential Gain Error Measuring Circuit
Differential Phase Error Measuring Circuit

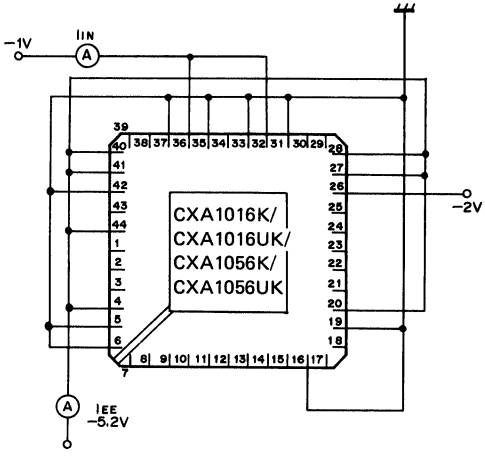


Differential Non-linearity Measuring Circuit

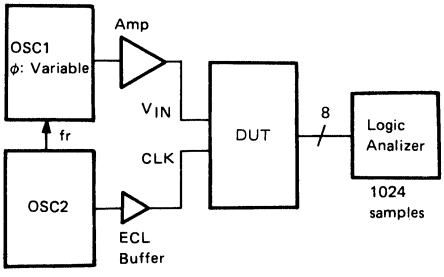


Power Supply Current Measuring Circuit
Analog Input Bias Current Measuring Circuit





Aperture Jitter Measuring Circuit



Description of Function (See the block diagram and timing chart.)

1. The reference voltage, which is obtained by dividing equally the voltage across V_{RT} to V_{RB} into 256 by the reference resistor ledder, is applied to the respective ⊕ (positive) input sides of 256 clocked comparators. An analog input is applied to the ⊖ (negative) input sides of all the 256 clocked comparators from the V_{IN} pin.

2. When the state of CLK is in Low, the master (front stage) of the comparator compares the respective reference voltage and the analog input voltage which is ever-changing.

3. When the CLK moves from Low into Hi, each master latches the state immediately prior to the above simultaneously, and as a result, it provides conditions of "11 .... 1100 .. 0" in sequence from the V_{RT} side to the V_{RB} side.

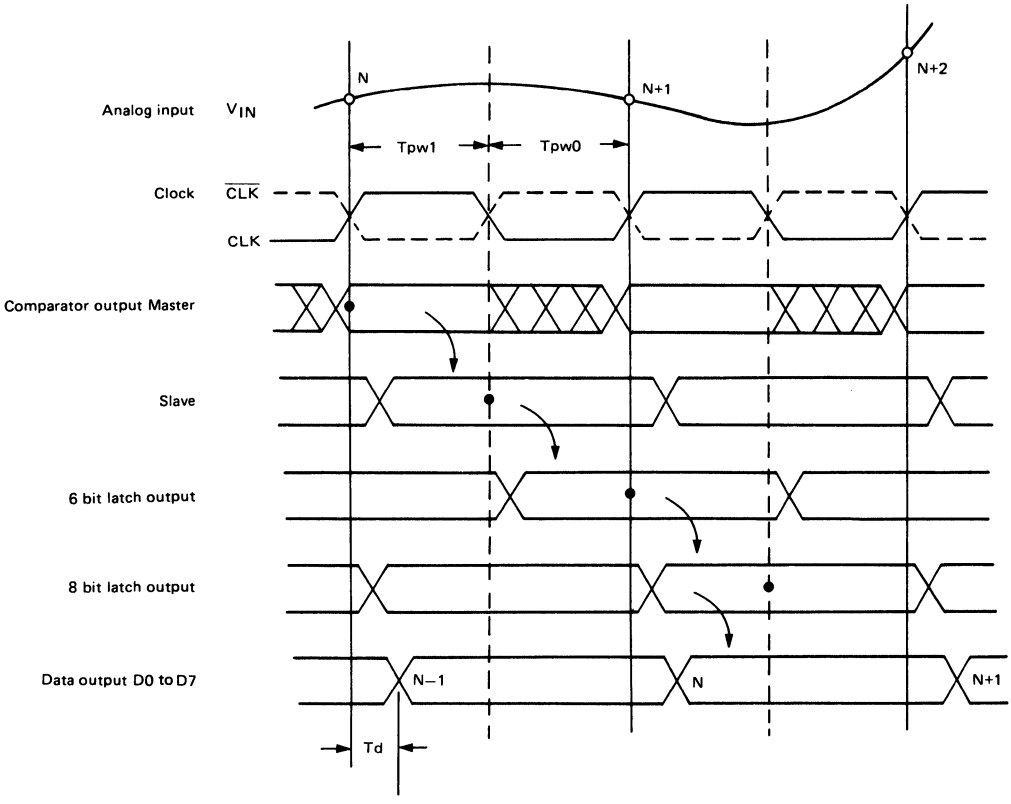
4. The output of the master is ANDed between the respective adjacent outputs, and "1" stands only when neighboring 2 outputs become "10", and the all other outputs become "0".

5. The result of the AND is latched when CLK moves from Hi into Low. Output of the slave is divided into 4 blocks and each block has 32 clocked comparators, and they are coded into binary codes of 6 bits respectively by the transistor matrix circuit.

6. The 6 bit codes are further coded into 8 bit codes by the transistor matrix circuit after they are respectively latched, and they are then output into the ECL level by the output buffer after being 8 bit latched. The output data is delayed 1 clock from the data sampling point and appears at the output pin.

7. Two polarity inversion inputs such as MINV and LINV are fed externally to the output buffer, and each of them selects output polarity of MSB and other polarity than MSB respectively.

Timing Chart



Dots (•) in the chart demote respective latch timings.

SONY **CXA1096P**

8 bit 20 MHz Flash A/D Converter

Preliminary

Description

CXA1096P is an 8 bit 20 MHz high speed A/D converter IC. This IC is suitable for applicated such as digital TV and graphic display.

Features

- Resolution 8 bit ±1/2 LSB
- High speed operation 20MS/s
- Wide band analog input 8MHz (−3dB)
- Low input capacity
- Low power consumption 320mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or Dual +5V, −5.2V)

Function

8 bit, 20MS/s parallel A/D converter

Structure

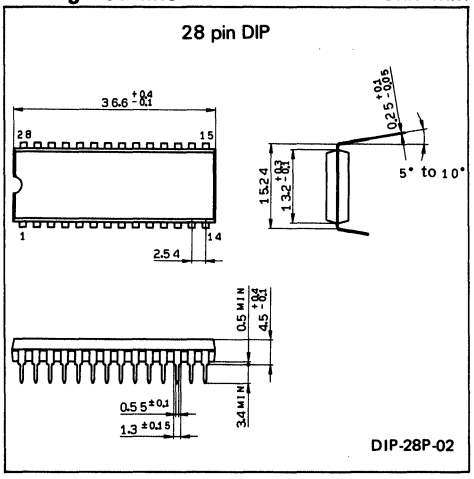
Bipolar silicon monolithic IC

Application

- Digital TV
- High speed signal processing

Package Outline

Unit: mm



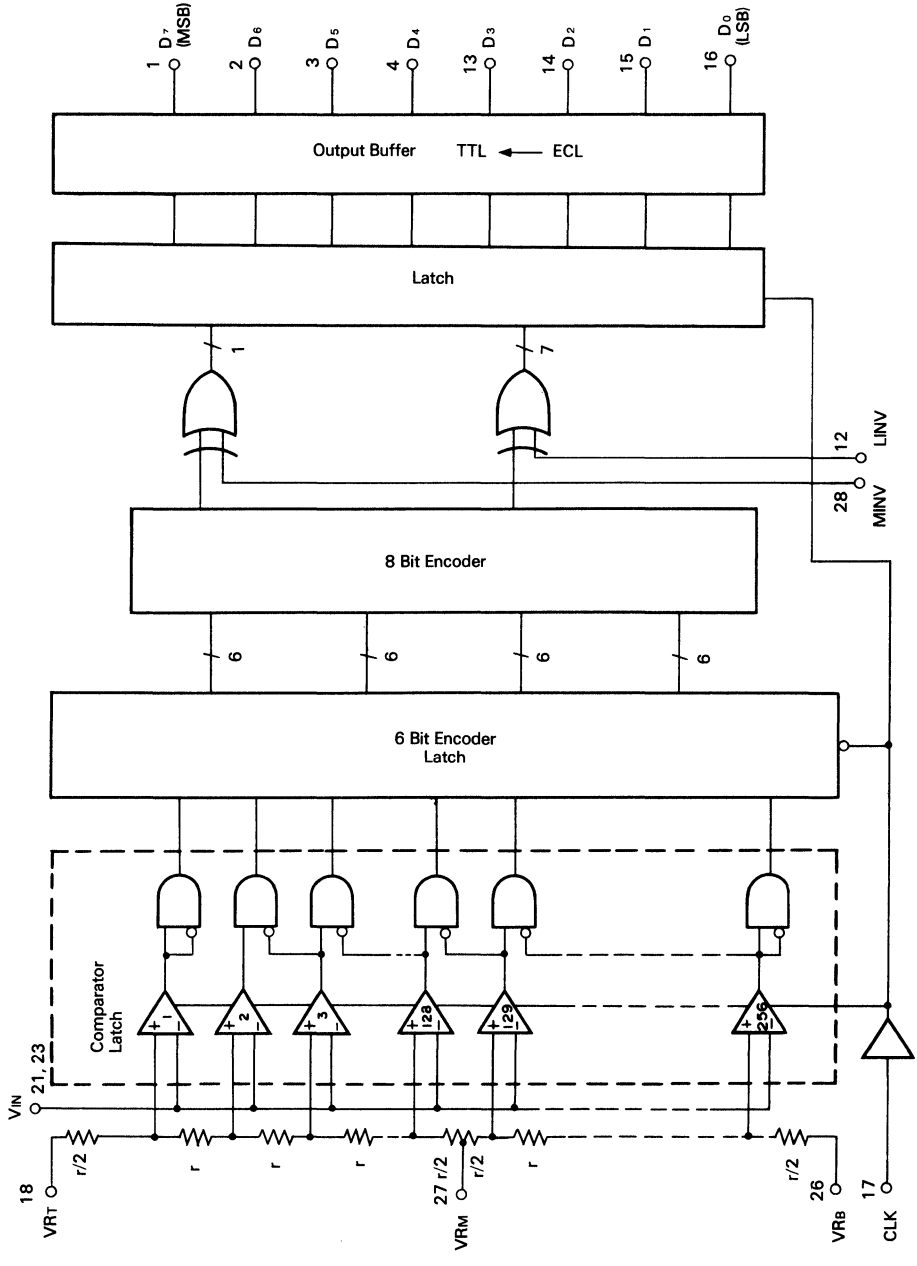
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC} − GND	0 to +6	V
	V_{EE} − GND	0 to −6	V
• Input voltage (analog)	V_{IN}		
	(+5V single power supply)	−0.5 to V_{CC}	V
	(dual power supply)	0.5 to V_{EE}	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}		V
	(+5 single power supply)	−0.5 to V_{CC}	
	(dual power supply)	0.5 to V_{EE}	V
	V_{RT} − V_{RB}	2.5	V
• Operating temperature	Topr	−20 to 75	°C
• Storage temperature	Tstg	−55 to 150	°C

Recommended Operating Conditions

• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
• Reference input	V_{RT}	AGND −0.1 to AGND +0.1	V
	V_{RB}	AGND −2.2 to AGND −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	30	ns
• Clock pulse width	T_{PW0}	10	ns

Block Diagram



Output coding

MINV LINV	0 0	0 1	1 0	1 1
AGND	111 ... 11 111 10	100 ... 00 100 ... 01	011 ... 11 011 ... 10	000 ... 00 000 ... 01
VIN	100 ... 00 011 ... 11	111 ... 11 000 ... 00	000 ... 00 111 ... 11	011 ... 11 100 ... 00
AGND − 2V	000 ... 01 000 ... 00	011 ... 10 011 ... 11	100 ... 01 100 ... 00	111 ... 10 111 ... 11

1: VIH, VOH
0: VIL, VOL

Electrical Characteristics (Single power supply)

(VCC = +5V, DGND = 0V, AGND = +5V, VEE = 0V, VRT = +5V, VRB = +3V, Ta = 25°C)

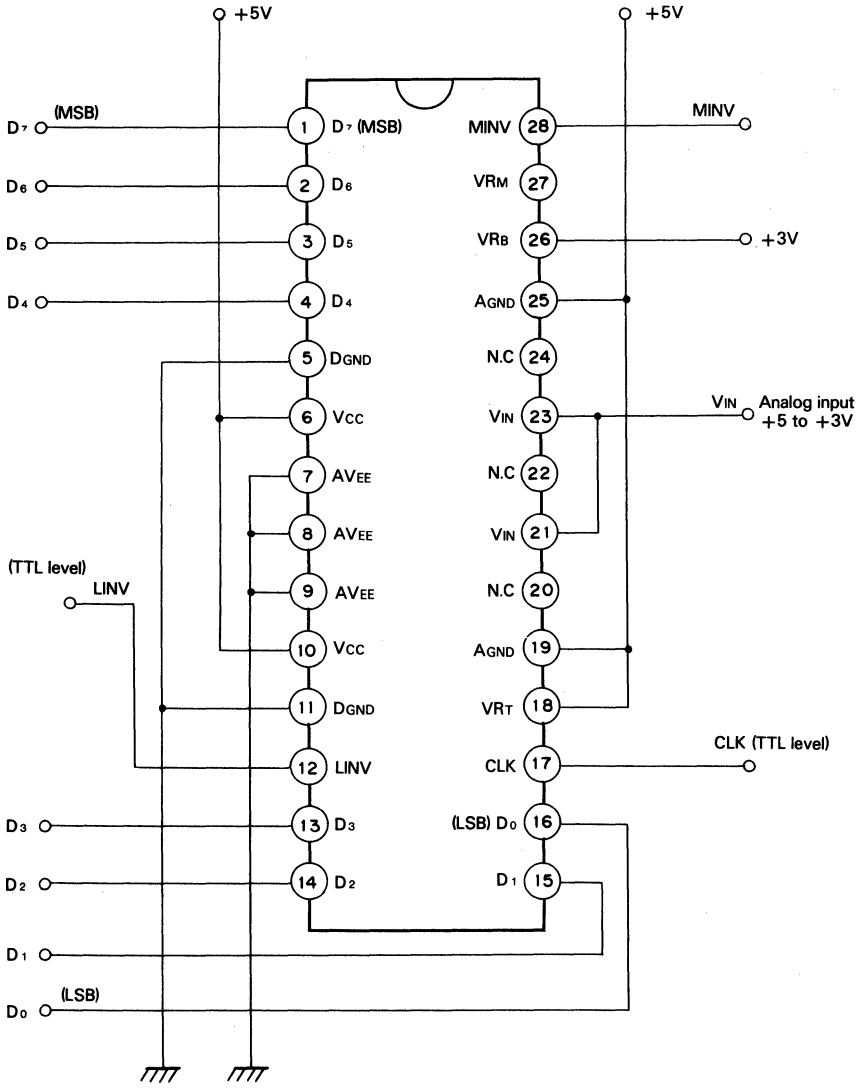
Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
Maximum conversion frequency		FC		20			MS/s
Power supply current		ICC + IEE			58	70	mA
Reference pin current		Iref			14	16	mA
Analog input capacity		CIN			30	35	pF
Analog input bias current		IIN			50	100	μA
Reference resistance rate (VRT to VRB)		Rr (VRT to VRB)			130		Ω
Off set voltage	VRT			11	13	15	mV
	VRB			3	5	7	mV
Digital input voltage		VIH		2.0			V
		VIL				0.8	V
Digital input current		IIH				10	μA
		IIL				−0.3	mA
Digital output voltage		VOH		2.7	3.4		V
		VOL				0.5	V
Output data delay		TDLH			23	28	ns
		VDHL			35	40	ns
Non linearity		DLE	FC = 20 MS/s			±1/2	LSB
Differential non linearity		ILE	FC = 20 MS/s,			±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, FC = 14.3MS/s			1.5	%
Differential phase error		DP				0.5	deg.
Aperture jitter							ps

Electrical Characteristics (Dual power supply)

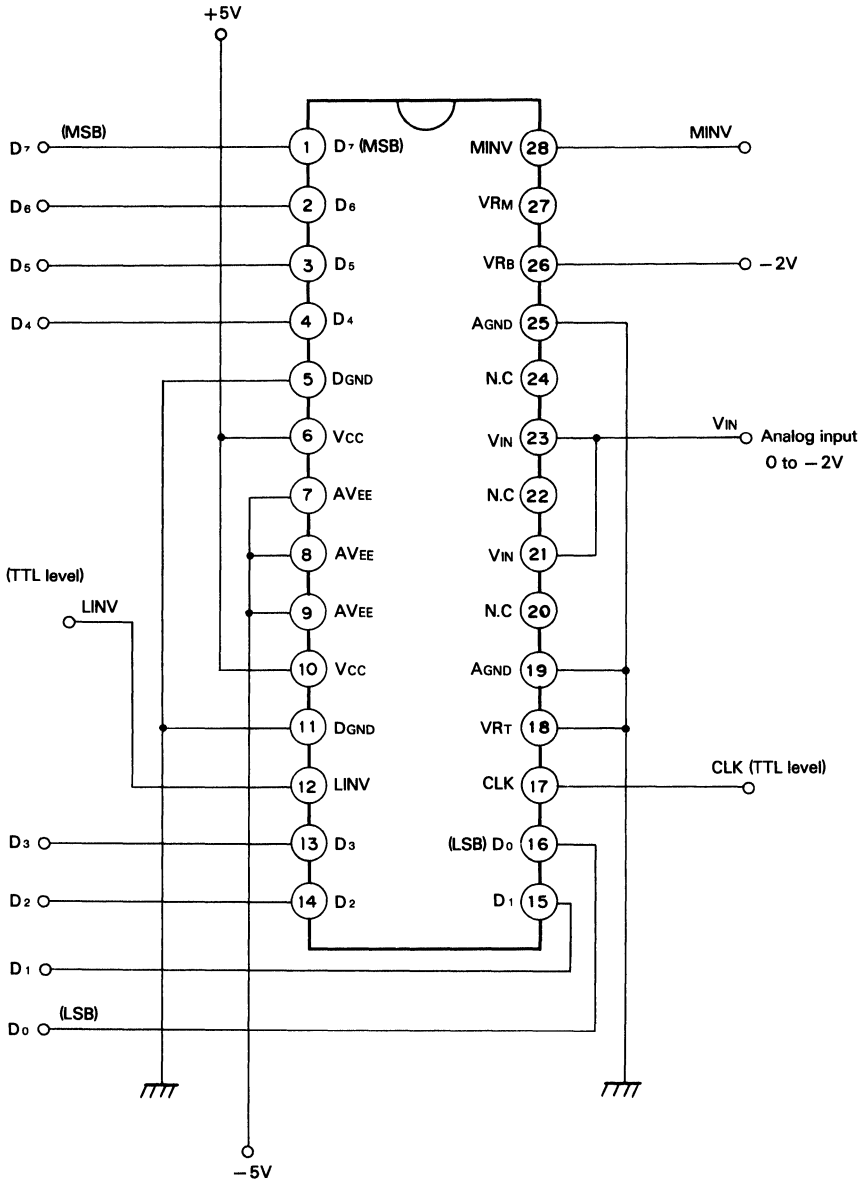
(V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Maximum conversion frequency	Fc	fin = 1 kHz, ramp	20			MS/s
Supply current	Icc			8	9.5	mA
Supply current	Iee			53	63.5	mA
Reference pin current	Iref			14	16	mA
Analog input capacity	Cin	V_{IN} = −1V + 0.07 Vrms		30	35	pF
Analog input bias current	Iin	V_{IN} = −1V		50	100	μA
Reference resistance rate (V_{RT} to V_{RB})	Rr (V_{RT} to V_{RB})			130		Ω
Off set voltage V_{RT}			11	13	15	mV
Off set voltage V_{RB}			3	5	7	mV
Digital input voltage	V_{IH}		2.0			V
	V_{IL}				0.8	V
Digital input current	I_{IH}				10	μA
	I_{IL}				−0.3	mA
Digital output voltage	V_{OH}		2.7	3.4		V
	V_{OL}				0.5	V
Output data delay	T_{DLH}			23	28	nS
	T_{DHL}			35	40	nS
Non linearity	DLE	Fc = 20 MS/s			±1/2	LSB
Differential non linearity	ILE	Fc = 20 MS/s,			±1/2	LSB
Differential gain error	DG	NTSC 40 IRE mod. ramp, Fc = 14.3MS/s			1.5	%
Differential phase error	DP				0.5	deg.
Aperture jitter						ps

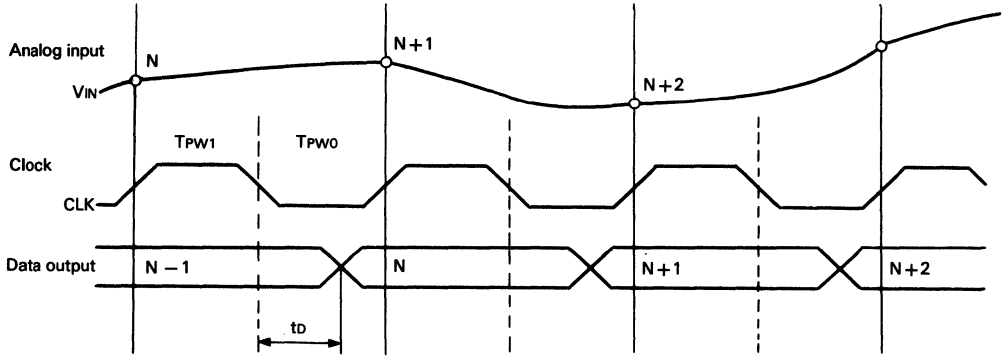
Application Circuit
(Single power supply)



(Dual power supply)



Timing chart



SONY

CXA1106P

8 bit 35 MHz High-speed D/A Converter

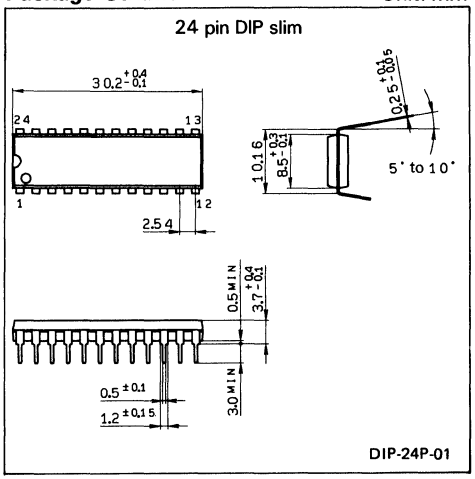
Preliminary

Description

CXA1106P is an 8 bit 35 MHz high speed D/A converter IC. This IC is suitable for application such as digital TV and graphic display.

Package Outline

Unit: mm



Features

- Resolution 8 bit
- High speed operation 35MSPS (max. conversion speed)
- Non linear error less than ±1/2LSB
- TTL compatible input
- +5 V single power supply or ±5V power supply
- Low power consumption +5V single power supply 200 mW (Typ.)
  ±5V dual power supply 400 mW (Typ.)

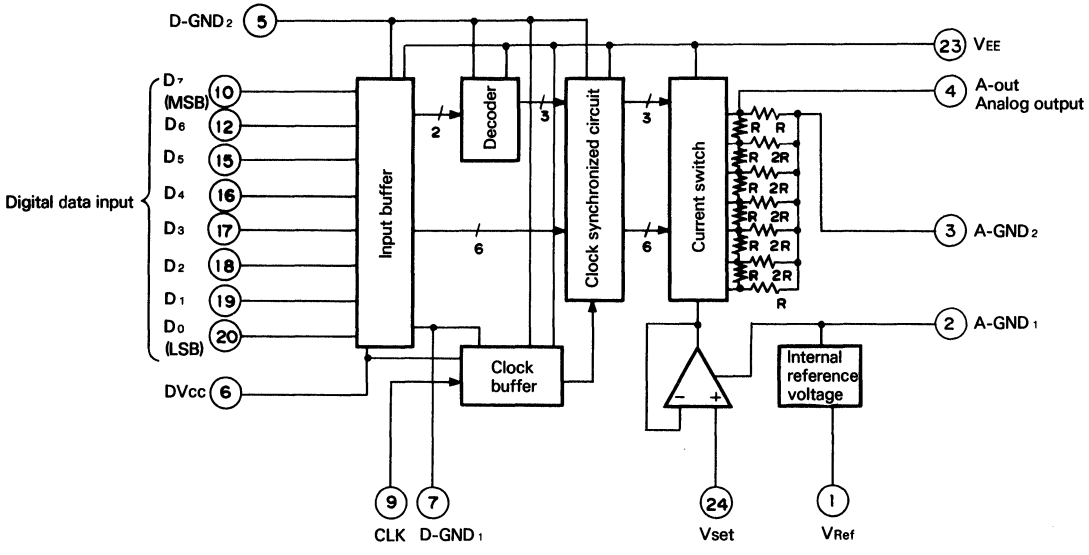
Absolute Maximum Ratings

• Supply voltage	V_{CC}	6	V
	V_{EE}	−6	V

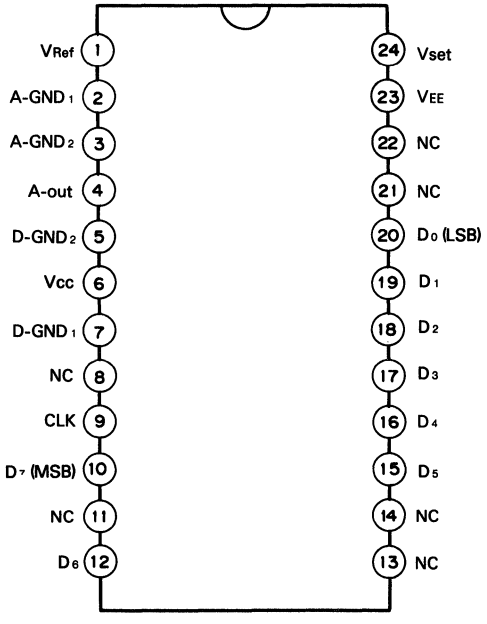
Recommended Operating Range

• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V

Block Diagram



Pin Configuration (Top View)



Electrical Characteristics

Single power supply (V_{CC} = $DGND_2$ = AGND = +5V, $DGND_1$ = V_{EE} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Current consumption	$I_{CC}+I_{EE}$		29		mA
Output impedance	Zo		350		Ω
Full scale output voltage	$V_{(FS)}$		1		Vp-p
Maximum conversion frequency	fc	35			MHz
Differential linear error	DLE	−1/2	0	+1/2	LSB
Integral linear error	ILE	−1/2	0	+1/2	LSB
Internal reference voltage	V_{Ref}		1.2		V
Digital input	Di		TTL level		

Dual power supply (V_{CC} = +5V, $DGND_1$ = D-GND_2 = A-GND = 0V, V_{EE} = −5V)

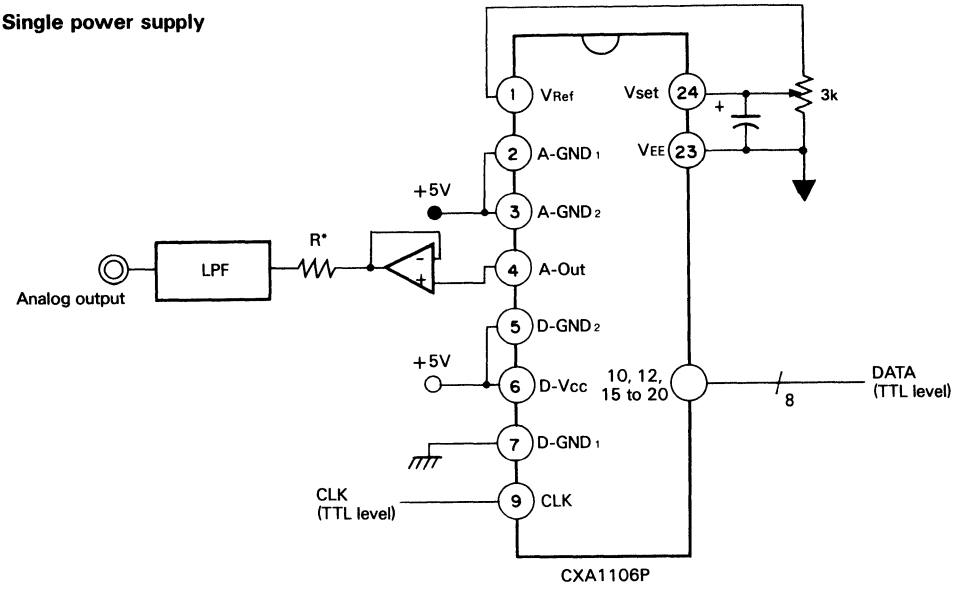
Item	Symbol	Min.	Typ.	Max.	Unit
Current consumption (Vcc)	I_{CC}		29		mA
Current consumption (V_{EE})	I_{EE}		−39		mA
Output impedance	Zo		350		Ω
Full scale output	$V_{(FS)}$		1		Vp-p
Maximum conversion frequency	fc	35			MHz
Differential linear error	DLE	−1/2	0	+1/2	LSB
Integral liner error	ILE	−1/2	0	+1/2	LSB
Internal reference voltage	V_{Ref}		1.2		V
Digital input	Di		TTL level		

I/O Table (Full scale output voltage 1.0V)

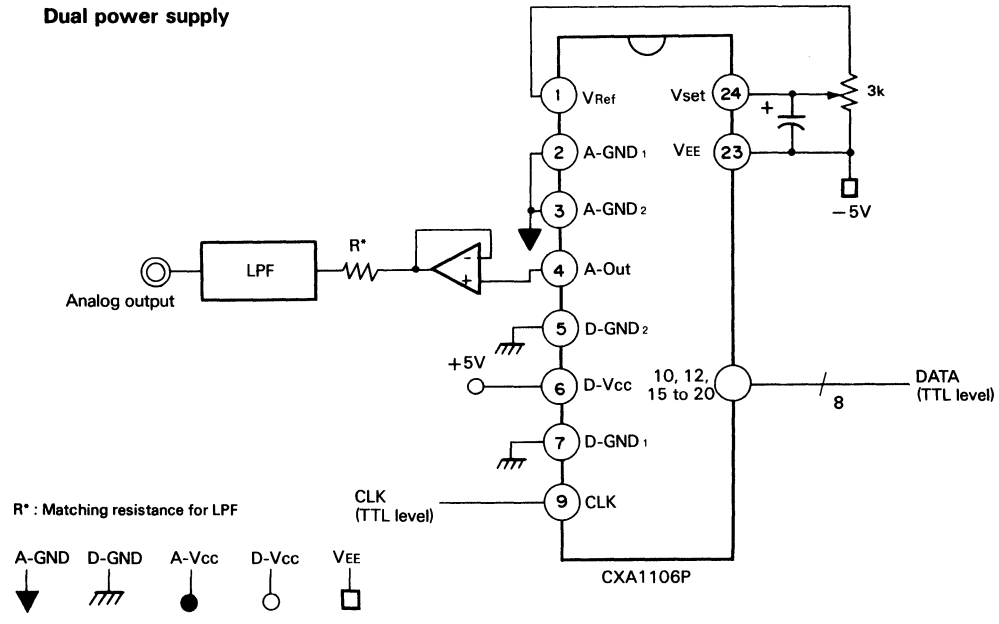
	Input code								Output voltage
Single power supply	MSB							LSB	
	1	1	1	1	1	1	1	1	Vcc
					⋮				⋮
	1	0	0	0	0	0	0	0	Vcc − 0.5V
					⋮				⋮
	0	0	0	0	0	0	0	0	Vcc − 1.0V
Dual power supply	MSB							LSB	
	1	1	1	1	1	1	1	1	0V
					⋮				⋮
	1	0	0	0	0	0	0	0	−0.5V
					⋮				⋮
	0	0	0	0	0	0	0	0	−1.0V

Application Circuit

Single power supply



Dual power supply



R* : Matching resistance for LPF

A-GND D-GND A-Vcc D-Vcc VEE

SONY BX-1300

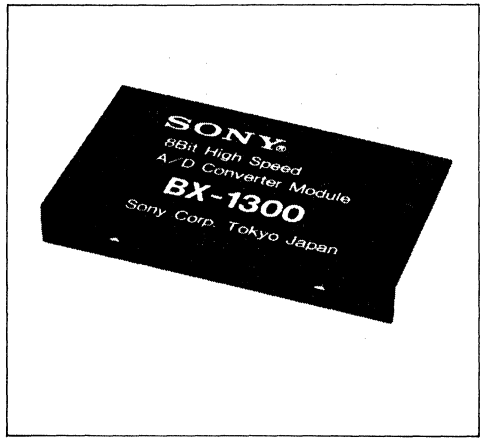
8 bit 20 MHz A/D Converter Module

Description

BX-1300 is an 8-bit A/D converter Module for video signal processing, in which CX20052A (8-bit serial-parallel type high-speed A/D converter IC) and necessary peripheral circuits are combined. It can be operated only by connecting a clock pulse circuit and the power supply.

Its digital output is 8-bit parallel output at TTL level.

Package Outline



Features

- Offset adjustment available. Built-in buffer amplifier
- Clock input and digital output at TTL level
- Operation possible only by connecting a clock pulse circuit and the power supply

Structure

Hybrid IC

Functions

• Resolution	8 bit±1/2 LSB
• Maximum conversion rate	20 MHz (MIN)
• Analog input level	1 Vp-p
• Digital output level	TTL level

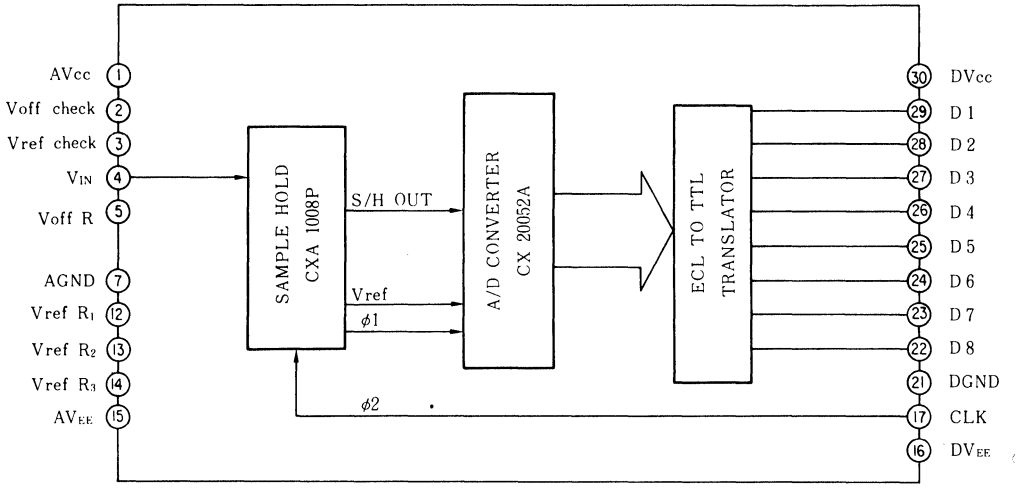
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	+5.5	V
	V_{EE}	−5.5	V
• Operating temperature	Topr	−10 to +65	°C
• Storage temperature	Tstg	−20 to +80	°C

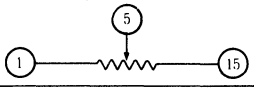
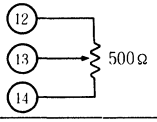
Recommended Operating Conditions

• Supply voltage	V_{CC}	+5.0 ± 0.25	V
	V_{EE}	−5.0 ± 0.25	V
• Clock input voltage	V_{CLK}	at TTL level	
• Input signal voltage	V_{IN}	1	Vp-p
• Reference voltage	V_{REF}	−2	V

Block Diagram



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	AVcc	Analog +5 V	16	DVEE	Digital −5 V
2	Voff check	Offset check pin	17	CLK	Clock input (TTL level)
3	Vref check	Reference voltage check pin	21	DGND	Digital GND
4	VIN	Signal input pin	22	D8 (LSB)	Digital output (TTL)
5	Voff R	Offset VR pin (2 kΩ) 	23	D7	
			24	D6	
			25	D5	
7	AGND	Analog GND	26	D4	
12	Vref R1	Reference VR pin 	27	D3	
13	R2		28	D2	
14	R3		29	D1 (MSB)	
15	AVEE	Analog −5 V	30	DVcc	Digital +5 V

Electrical Characteristics Ta = 25°C, V_{CC} = 5V, V_{EE} = −5 V

Item	Symbol	Min.	Typ.	Max.	Unit
Linearity error[1]	LE			±1/2	LSB
Differential gain[2]	DG		1.0		%
Differential phase[3]	DP		0.5		%
Maximum conversion rate	$F_{CLK\ MAX}$	20			MHz
Minimum conversion rate	$F_{CLK\ MIN}$			5	MHz
Current consumption	I_{CC}	105	140	175	mA
	I_{EE}	240	300	350	mA
Analog input impedance	R_{IN}	71.3	75	78.8	Ω
Clock input impedance	R_{CLK}		2.5		kΩ
Variable range of input offset*)	V_{IN}	−1.3		0.8	V

Digital output voltage V_{OD}: at TTL level

Measurement conditions
1) V_{IN}: −0.3 to +0.7 Vramp f: 1 kHz CLK: 20 MHz
2), 3) V_{IN}: NTSC 40IRE mode ramp CLK: 20 MHz

*) Input amplitude 1 Vp-p max. See Fig. 1.

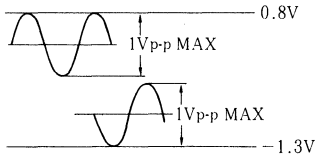
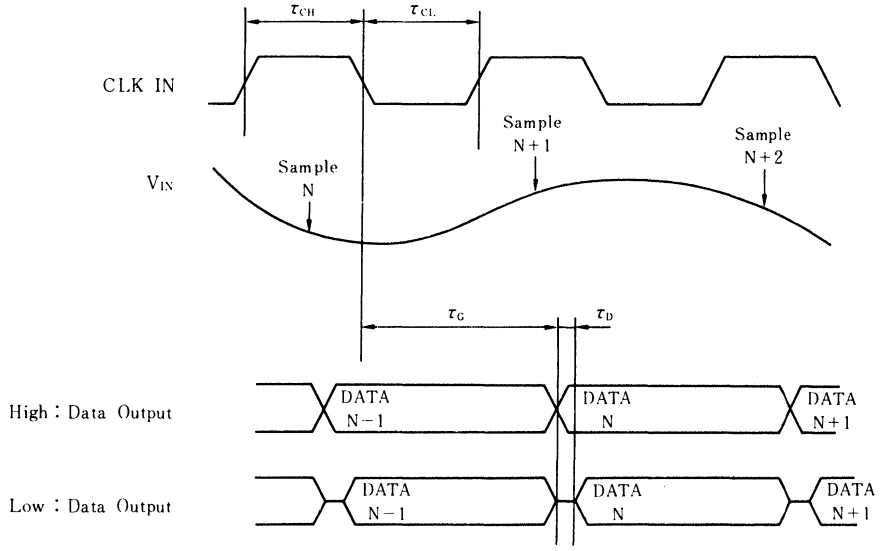


Fig. 1 Variable Range of Input Offset

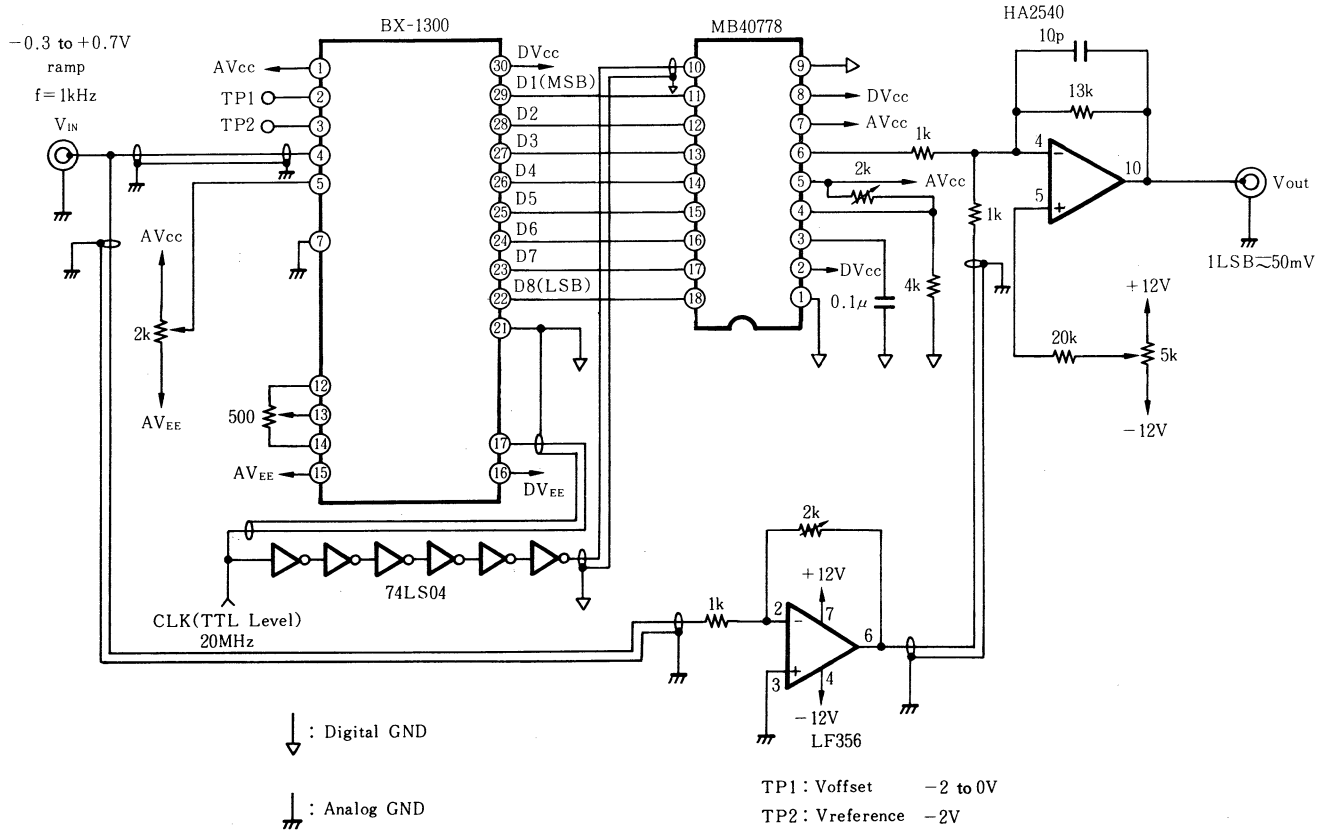
Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
Clock input	τCH	22	25	100	ns
	τCL	22	25	–	ns
Data delay	τG	–	40	48	ns
	τD	–	3	4	ns

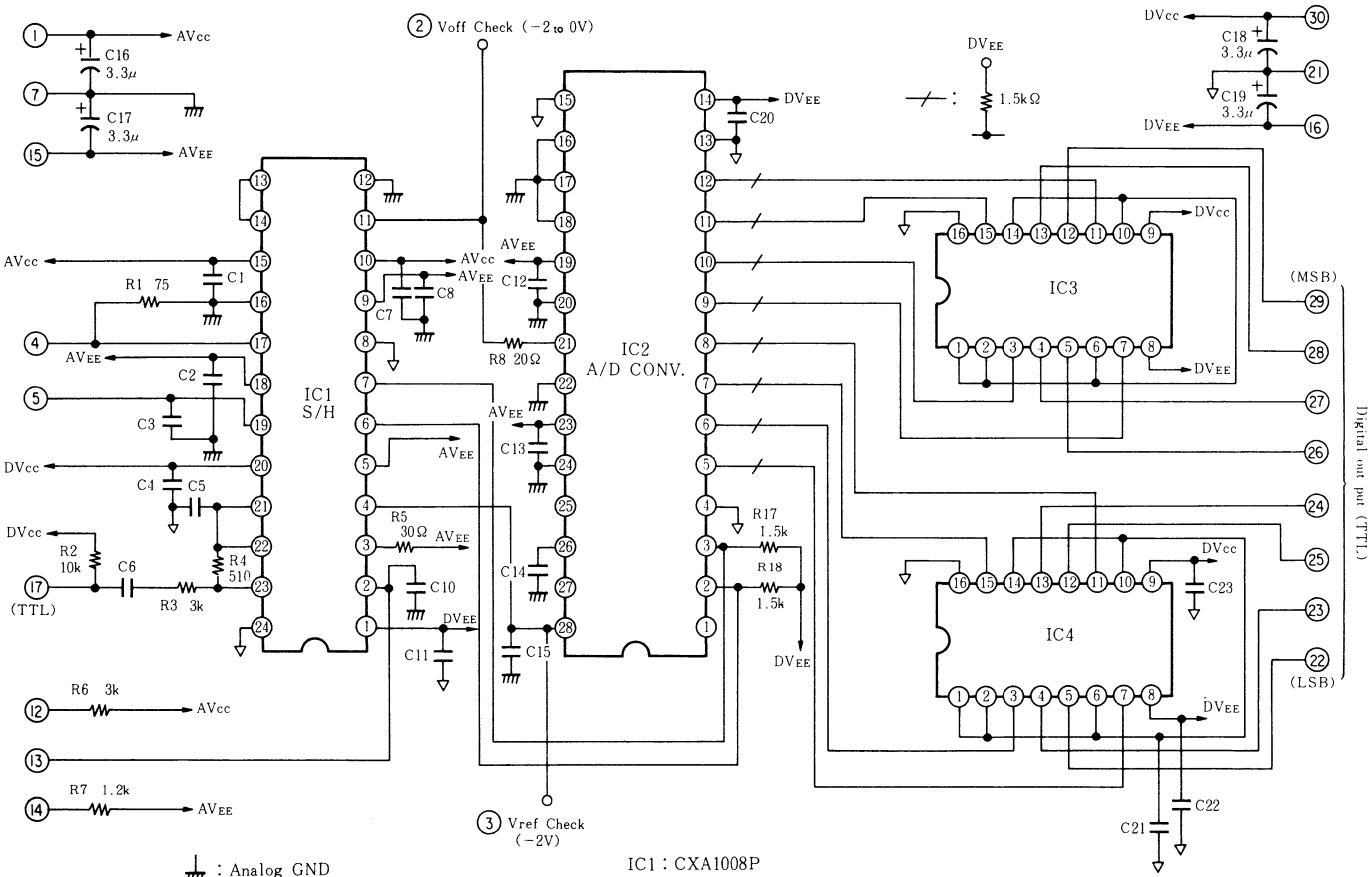
Note) Set clock duty at the optimum point as long as the above conditions are satisfied.

Measuring Circuit



SONY

Equipment Circuit



: Analog GND

: Digital GND

No marked C : 0.1μF

IC1 : CXA1008P
IC2 : CX20052A
IC3, IC4 : HD10125
C16, C17, C18, C19 : tantalum condenser 3.3μF, 16V
Other C : Y5V characteristics, ±80%, −20%, 0.1μF, 25V
R : All chip resistor

SONY

Adjusting Method

(1) Voff check : Terminal for checking offset voltage.
Adjust the variable resistor connected to the Voff R terminal so that Sample Hold output falls within the input voltage range (0 to −2 V) of the A/D converter.

(2) Vref check : Terminal for adjusting reference voltage of A/D converter.
Adjust the reference variable resistor (500 Ω) so that the reference voltage (Vref check) of the A/D converter becomes −2 V.

Output Data Format

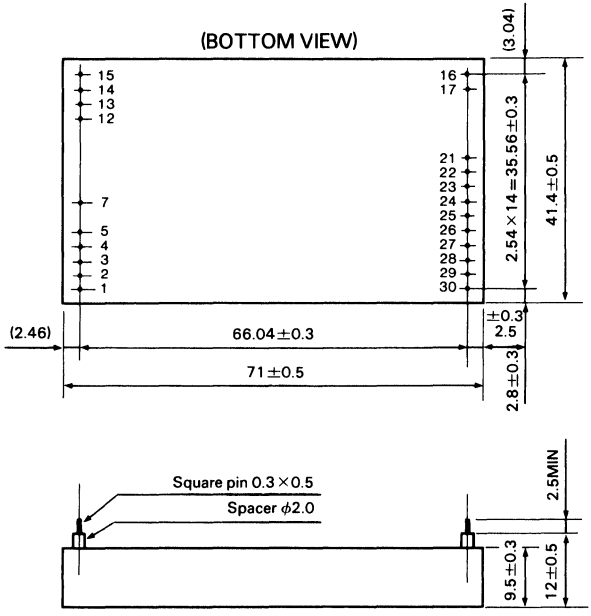
Input to the A/D converter (output from the Sample Hold) is quantized into an 8-bit format within the range of reference voltage (GND to Vref check).

Step	A/D input signal voltage (Voff check)	Digital Output code
		MSB LSB
	over 0.0000V	11111111
000	0.0000V	11111111
•	•	•
•	•	•
•	•	•
127	−0.9961V	10000000
129	−1.0039V	01111111
•	•	•
•	•	•
•	•	•
255	−2.0000V	00000000
	under −2.0000V	00000000

Notes on Applications

(1) Output data is regulated by the trailing edge of the CLK input. Adjust latch timing referring to the timing chart.
(2) Sufficient accuracy may not be achieved for output waveform if fluctuation above 0.6 V occurs in analog input (VIN) during one sample period.

Package Outline

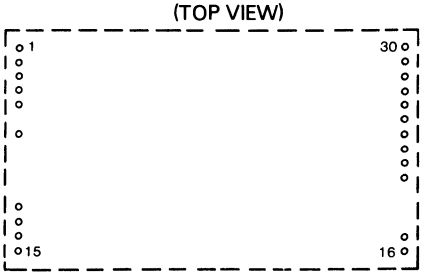


Unit: mm

Note 1)
Recommended hold diameter for board mounting is $\phi 1$.

Note 2)
Pins 1, 15, 16 and 30 come with spacers, and others are square pins only.

Pattern Layout



Digital Signal Processors

3) Digital Signal Processors

Type	Function	Page
CX-7997	10 × 10bit 15MHz Multiplier/Adder	219
CX23024 CX23067	8bit S-P-S Converter	230
CX23034	Digital Filter for CD	238
CX23038	Programmable Shift Register	249
CX23043	10bit Synchronous Binary Counter	257
CXD1018G	Degital Signal Processing Multipler	266
CXK1201P	Double Scan Converter (P)	283
CXK1202S	Digital Delay Line	295

(P) : Preliminary

10 × 10 bit 15 MHz Multiplier/Adder

Description

Sony CX-7997 is a CMOS 10 × 10 +16 parallel multiplier/adder characterized by high speed, high performance, and low power consumption. It has the following functions:

1) Multiplication D ← A × B
2) Addition D ← BA* + C
3) Multiplication-Addition D ← A × B + C
4) Delay Function D ← A, B, BA, C

Features

- Single power supply 5.0 V
- Low power consumption (At 14.4 MHz clock) 300 mW (typ.)
- Operating Modes 16
- Delay control function
- TTL compatible for both inputs & outputs
- Word length (2's complement)
  - Input A, B 10 bits
  - BA, C 16 bits
  - Output D 16 bits

* A and B inputs are used as 16 bit data input.

Absolute Maximum Ratings (Ta = 25°C)

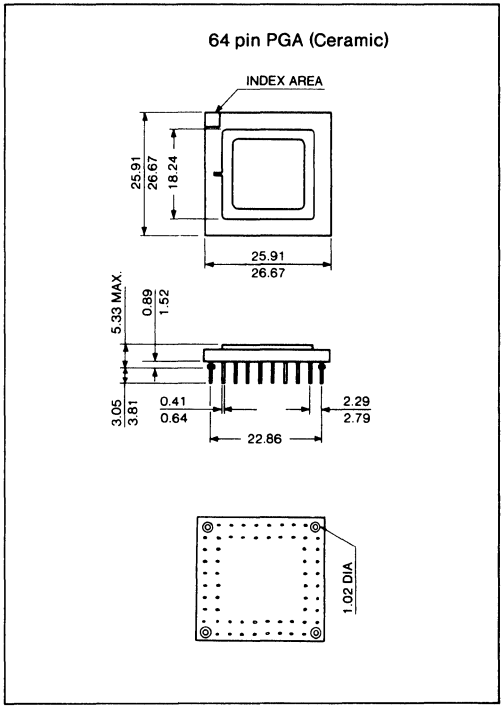
• Supply voltage	V_{DD}	−0.5 to +7.0	V
• I/O voltage	$V_{I/O}$	−0.5 to V_{DD} + 0.5	V
• Operating temperature	T_{opr}	0 to + 70	°C
• Storage temperature	T_{stg}	−55 to +150	°C

Recommended Operating Condition

• Supply voltage	V_{DD}	4.75 to 5.25	V

Package outline

Unit: mm



Block Diagram

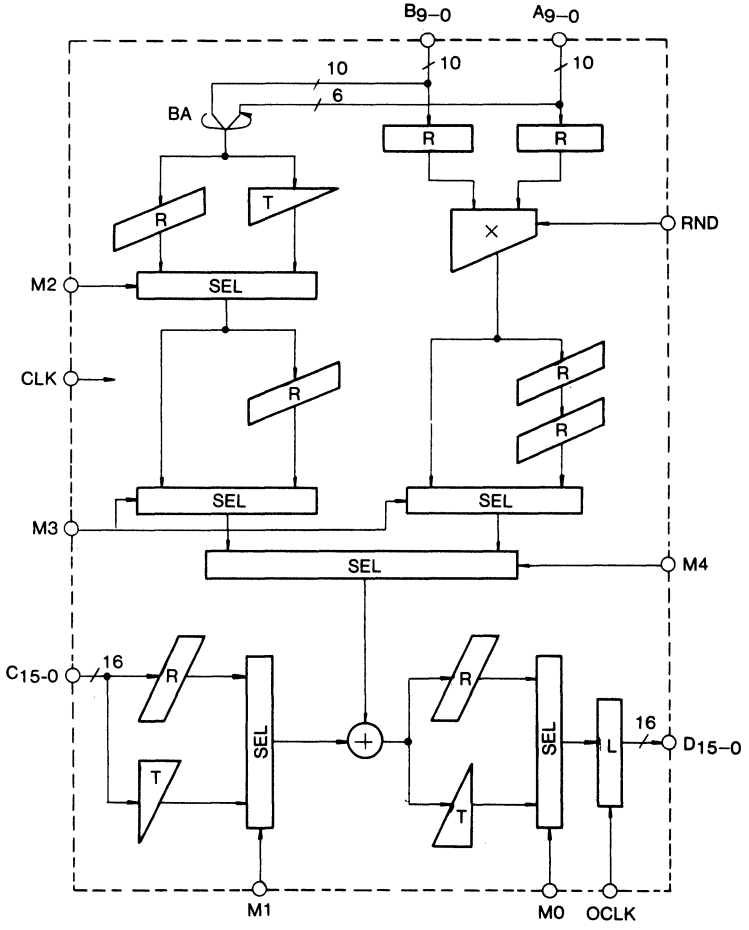


Fig. 1

Notes) R : Register
L : Transparent Latch
T : Triangular Delay
SEL : Selector
× : Multiplier
+ : Adder

All possible combinations of the mode assign inputs M4 – M0 are shown in Fig. 1.

Pin Connections (Top View)

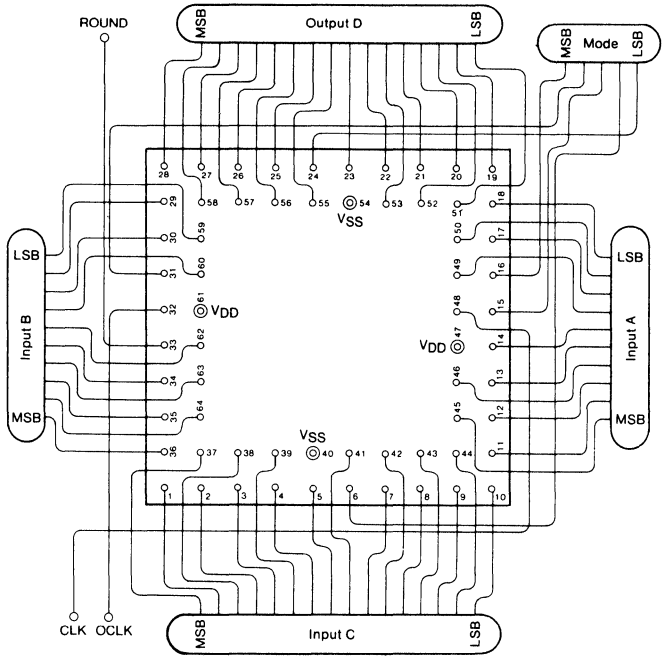


Fig. 2

No.	I/O	Name	No.	I/O	Name	No.	I/O	Name	No.	I/O	Name
1	I	C14	17	I	A2	33	I	RND	49	I	A3
2	I	C12	18	I	A0	34	I	B5	50	I	A1
3	I	C11	19	O	D1	35	I	B7	51	O	D0
4	I	C9	20	O	D3	36	I	B9	52	O	D2
5	I	C8	21	O	D4	37	I	C15	53	O	D5
6	I	M1	22	O	D6	38	I	C13	54	V_{SS}	–
7	I	C6	23	O	D7	39	I	C10	55	O	D8
8	I	C4	24	I	M0	40	V_{SS}	–	56	O	D10
9	I	C2	25	O	D9	41	I	C7	57	O	D12
10	I	C0	26	O	D11	42	I	C5	58	O	D14
11	I	A8	27	O	D13	43	I	C3	59	I	B0
12	I	A7	28	O	D15	44	I	C1	60	I	B3
13	I	A5	29	I	B1	45	I	A9	61	V_{DD}	–
14	I	A4	30	I	B2	46	I	A6	62	I	B4
15	I	M2	31	I	M3	47	V_{DD}	–	63	I	B6
16	I	M4	32	I	OCLK	48	I	CLK	64	I	B8

DC Characteristics

(V_{DD} = 5.0 V ±5%, T_{opr} = 0 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply	I_{DDS}	Non-operating state $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$	0		0.1	mA
Output Voltage Level	V_{OH}	$I_{OH} = -0.4$ mA	4.0		V_{DD}	V
	V_{OL}	$I_{OL} = 3.2$ mA	V_{SS}		0.4	
Input Voltage Level	V_{IH}		2.2			V
	V_{IL}				0.8	
Input Leakage Current	I_{LI}	$V_I = 0$ to V_{DD}	−10		10	μA

I/O Capacitance

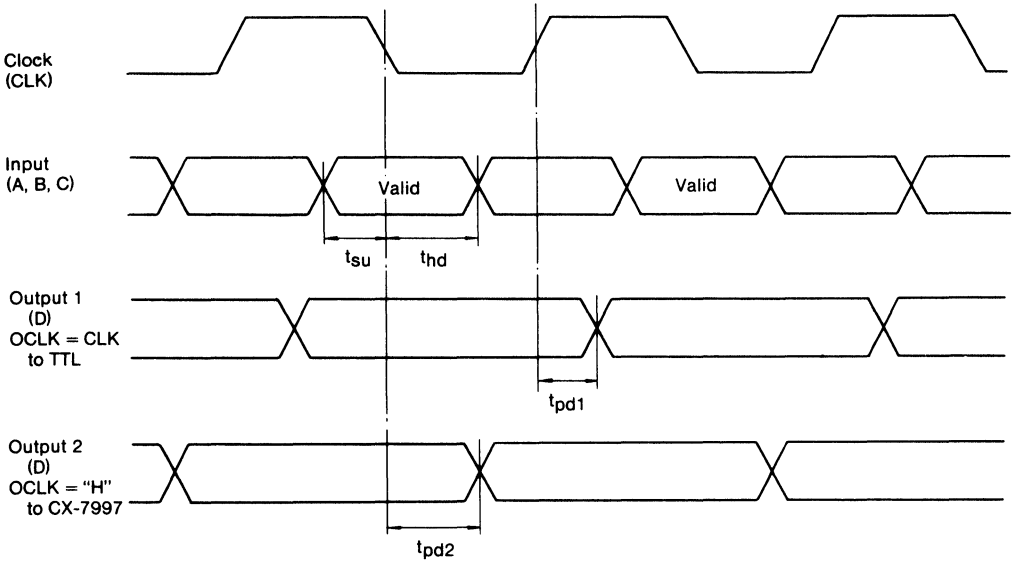
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input pin	C_{IN}	$V_{DD} = V_I = 0$ V, $f_M = 1$ MHz			9	pF
Output pin	C_{OUT}	$V_{DD} = V_I = 0$ V, $f_M = 1$ MHz			9	pF

I/O Timing

(V_{DD} = 5.0 V ±5%, T_{opr} = 0 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Clock Frequency	CLK, OCLK	f_{ck}	14.4			MHz
Input Data Set UP Time	A9 to A0, B9 to B0, C15 to C0	t_{su}	2			ns
Input Data Hold Time	A9 to A0, B9 to B0, C15 to C0	t_{hd}	24			ns
Data Output from OCLK (Note 1)	D15 to D0	t_{pd1}			36	ns
Data Output from CLK (Note 2)	D15 to D0	t_{pd2}	24		60	ns

Note 1) OCLK = CLK output load 30 pF
2) OCLK = "H" output load 60 pF



The above timing chart defines tpd, tsu and thd for the clock (CLK).
The actual input/output operations are performed with a throughput delay having the number of clocks as shown in the operation mode throughput delay (Fig. 7).

Fig. 3 CX-7997 Timing Chart

Pin Functions

(1) CLK (Clock Input Pin)
Clock input is distributed to data input register, internal pipeline register, and delay register. Data are transferred at falling edge of CLK ("H" → "L").

(2) OCLK (Clock Input Pin)
OCLK is enable signal to control data output latch.
When OCLK = "L", output data are latched.
When OCLK = "H", latch is in 'through' state.
Data are sampled at falling edge of CLK, and they are transferred to the output pins. (See the I/O timing specification).
When output data of CX-7997 are to an external device, transfer of data can be performed by setting OCLK from the external device.

(i) When the external device fetches data with the falling edge of the clock, wire each connection as shown in Fig. 4.

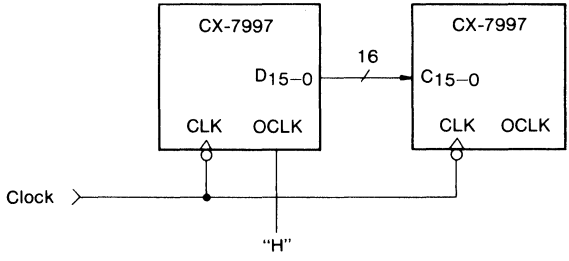


Fig. 4 External Device Interface (1)

(ii) When the external device fetches data at the rising edge of clock (i.e. 74LS374) wire each connection as shown in Fig. 5.

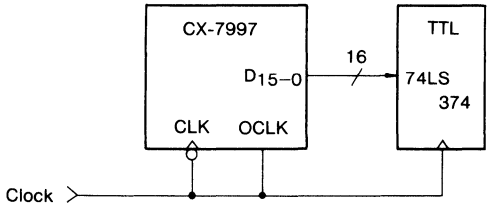


Fig. 5 External Device Interface (2)

(3) A9 to A0, B9 to B0 (Data Input Pin)
In multiplication-addition mode (M4 = "L"), A and B inputs are used as the 10 bit multiplier data input pins. (A9, B9 → MSB, A0, B0 → LSB).
In addition mode (M4 = "H"), A and B inputs are used as the 16 bit adder data input pins (BA) in the following configuration.

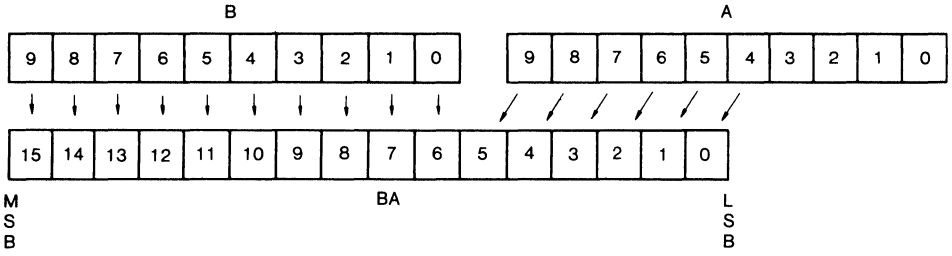


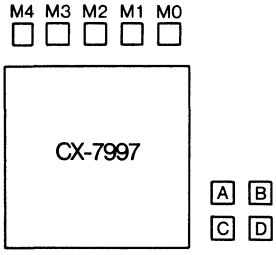
Fig. 6 "BA" Pin Configuration

(4) C15 to C0 (Data Input Pins)
Used as 16 bit adder data input pins in multiplication-addition mode and addition mode.
(C15 → MSB, C0 → LSB)

(5) D15 to D0 (Data Output Pins)
16 bit data output pins.
(D15 → MSB, D0 → LSB)

(6) M4 to M0 (Mode Assign Inputs)
Control signal inputs to assign the operating mode of the CX-7997 among the 16 possible functions. (Shown in Fig. 7).
When mode assign inputs M4 to M0 are switched, output D15 to D0 becomes unstable for 18 clock cycle times maximum, so attention must be paid.
Any mode cannot be utilized except for the assigned modes shown in Fig. 7.

(7) RND (Round Control Input)
When RND = "L", P4 to P0 (2^{-14} to 2^{-18}: See Fig. 3) of internal multiplier output are discarded.
When RND = "H" (2^{-14}) and internal multiplier output is added and P4 to P0 are discarded.

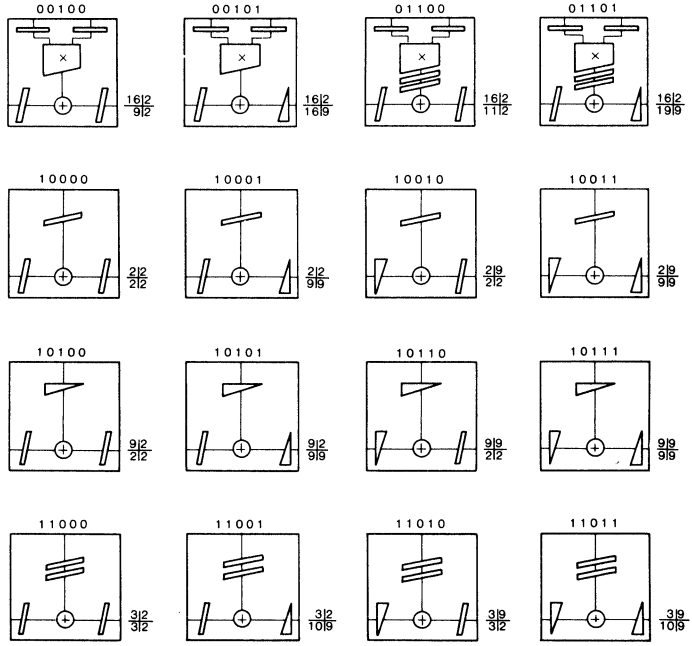


Operation Mode Throughput Delay

	0	1
M4	Multiplication-Addition	Addition
M3	No delay is added before adder.	If M4=0, multiplication result is delayed by 2 clocks. If M4=1, BA input is delayed by 1 clock.
M2	A, B, BA inputs need bit delay. **	No delay is needed for A, B, BA inputs.
M1	C input needs bit delay. **	No delay is needed for C input.
M0	D output has bit delay. **	D output has no bit delay. **

Number of Clock Delays

A	Delay from A, B and BA inputs to D_{MSB}	B	Delay from C input to D_{MSB}
C	Delay from A, B and BA inputs to D_{LSB}	D	Delay from C input to D_{LSB}



Note) When mode signal is changed for a maximum of 18 clock cycle times, the output is unstable.

Fig. 7 Operating Mode, Throughput Delay

Example of I/O Timing (When M4, M3, M2, M1, M0 = 00100)

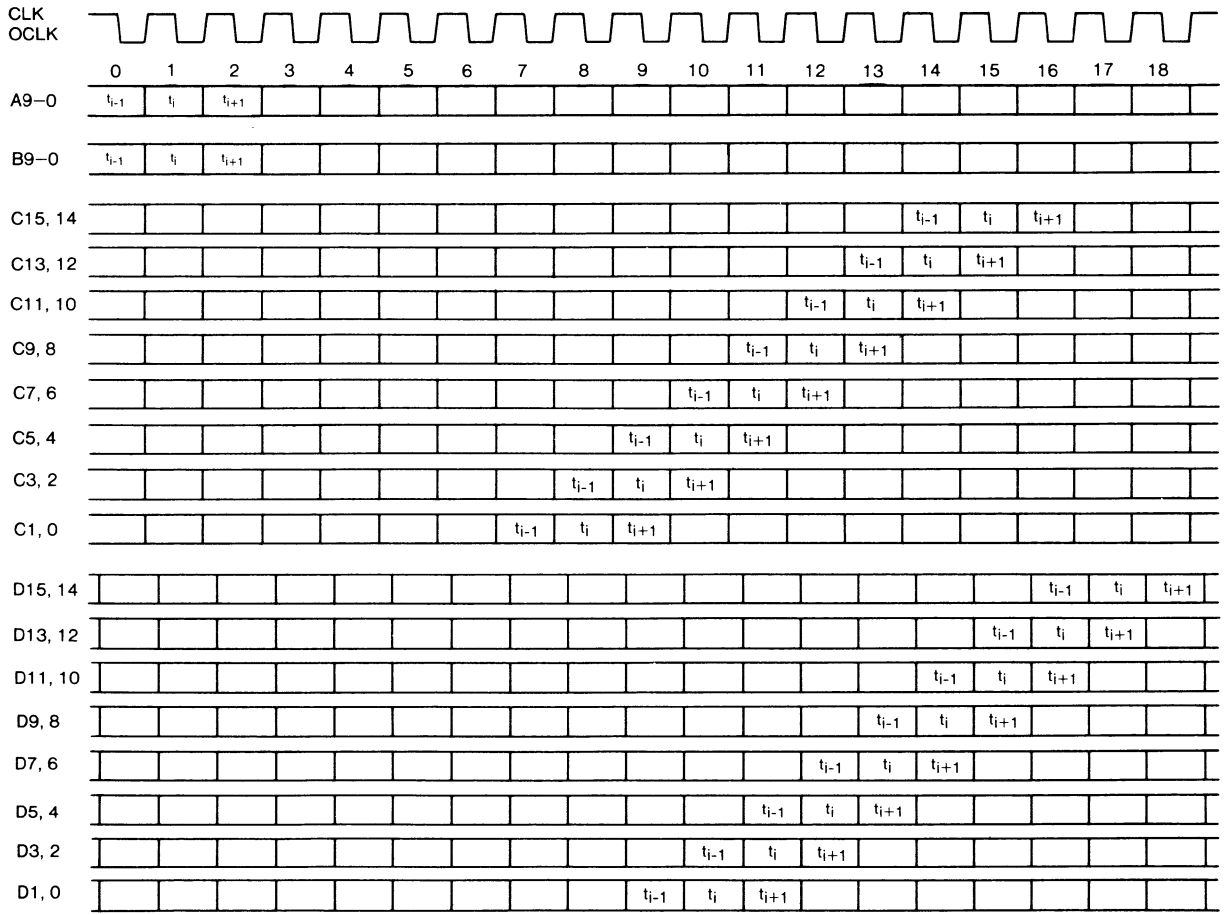


Fig. 8

** Bit Delay – A clock delay among the input bits or output bits.

Internal calculation is done for each 2 bit data starting from LSB. For example, Fig. 8 shows the I/O timing of the mode (M4, M3, M2, M1, M0) = (0, 0, 1, 0, 0). In this case, A and B inputs do not have a clock delay. However, C input must have a clock delay for each 2 bit data. Multiplication is done for each 2 bit data starting from LSB. Adder needs to adjust the timing between the output bits of the multiplier and C input bits. This is called pipeline method and CX-7997 can achieve high speed operation with clock rate, 14.4 MHz using this technique.

D output also has this "bit delay" among each 2 bit data at this mode.

In Fig. 8, t_{i-1} represents the timing of 2 bit data which are supplied in A and B inputs at "0" clock timing.

2 bit data from LSB of the multiplied data are added to C1, 0 at "7" clock timing; next 2 bit data are added to C3, 2 at "8" clock timing. 2 bit output data, D1, 0 are transferred to D output at "9" clock timing. In this way, the other data are calculated and are transferred to D output step by step.

The "bit delay" at D output can be compensated by setting the mode (M4, M3, M2, M1, M0) = (00101).

In this mode the triangular delay circuit designated T in Fig. 1, which is connected to M0, compensates the "bit delay".

Internal Operation Word Length

Fig. 9 shows the word length of the data utilized for internal operations in CX-7997. Multiplication results P4 to P0 are discarded (with RND control), and upper data P18 to P5 are added to C input. Since overflow detection is not performed on the operation result, care must be taken with the value of the input data. When the data is in 2's complement form, the decimal values of inputs and outputs must have the following limit

Input $-1 \leqq A < 1$ $-4 \leqq C < 1$
$-1 \leqq B < 1$ $-4 \leqq BA < 4$
$-1 < A \times B < 1$

Output $-4 \leqq D < 4$

When the value of A and B inputs are both -1, the multiplication result does not become 1 (it becomes -1), so that input data should not be provided in this combination.

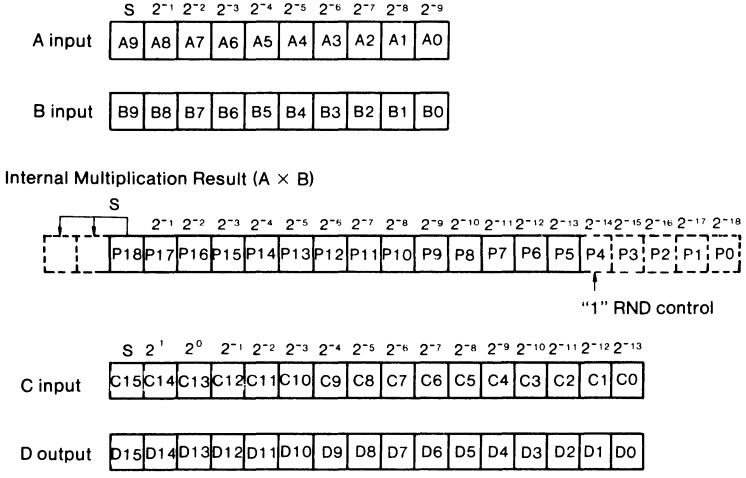


Fig. 9 Operation Word Length

SONY CX23024/CX23067

8 bit S-P-S Converter

Description

The CX23024/CX23067 is a general 8-bit structured serial/parallel/serial data conversion NMOS IC. It can be applied to high-speed digital processing of various kinds of signals for digital video system, etc.

Features

- Operation clock frequency: 50 MHz is guaranteed
- 5V single power supply
- Input/output level is compatible with TTL

Structure

N-channel Silicon Gate E/D MOS

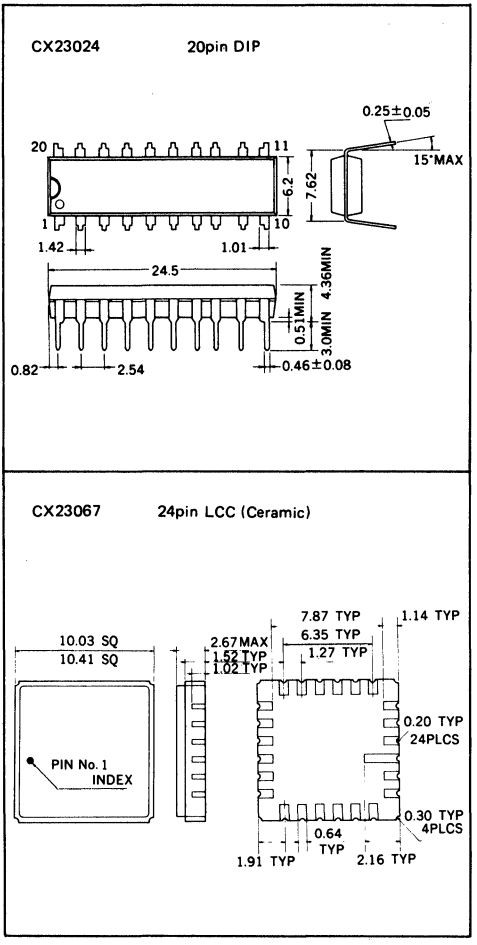
Absolute Maximum Ratings (Ta=25°C, Vss=0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Input voltage	V_{IN}	−1 to +7	V
• Operation temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D CX23024	500	mW
	CX23067	1000	mW

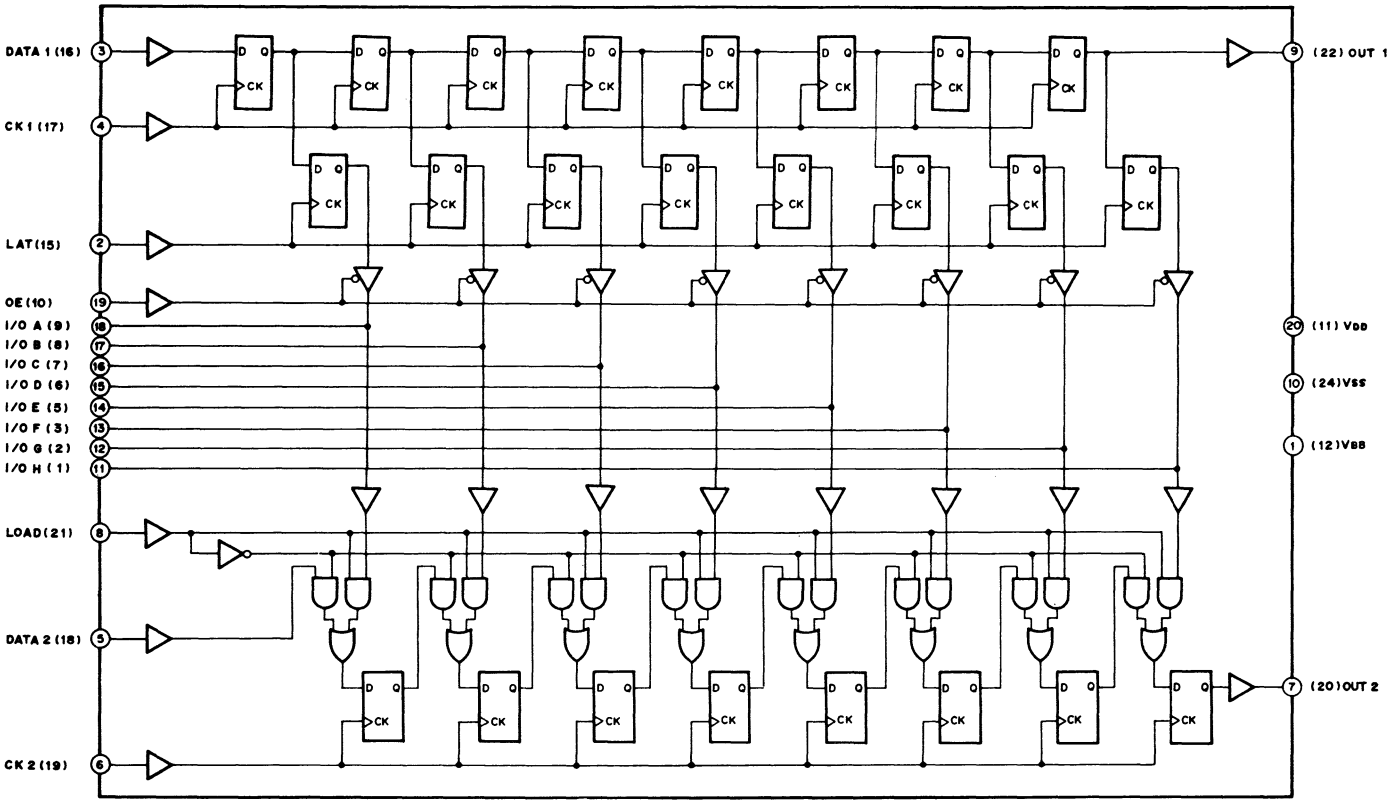
Recommended Operating Conditions (Vss=0V)

• Supply voltage	V_{DD}	+4.5 to +5.5	V
• High level input voltage	V_{IH}	+2.0 to V_{DD}+0.5	V
• Low level input voltage	V_{IL}	−1.0 to 0.8	V

Package Outline Unit: mm



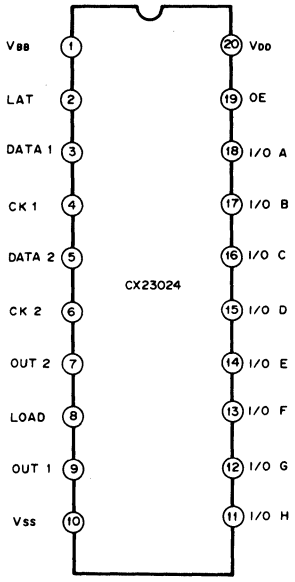
Block Diagram



The numbers in parentheses are the pin numbers of CX23067.

SONY

Pin Configuration (Top View)

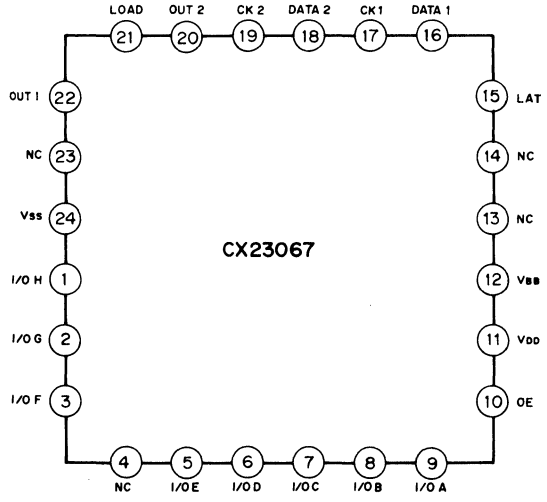


Pin Description

No.	Symbol	Description	
1	V_{BB}	Substrate (Connect a capacitor of 1000pF between this pin and ground)	
2	LAT	Data latch signal input pin of shift register 1	*
3	DATA1	Serial data input pin of shift register 1	*
4	CK1	Serial data shift clock input pin of shift register 1	*
5	DATA2	Serial data input pin of shift register 2	*
6	CK2	Serial data shift clock input pin of shift register 2	*
7	OUT2	Serial data output pin of shift register 2 Output buffer is of E/E structure	*
8	LOAD	Parallel data input selection input pin of shift register 2	*
9	OUT1	Serial data output pin of shift register 1 Output buffer is of E/E structure	*
10	V_{SS}	Ground	
11 to 18	I/O H to I/O A	Parallel data input/output pin Output buffer is of E/E structure	
19	OE	Output enable	
20	V_{DD}	Power supply (+5V)	

***Note)** Shift register 1 is a shift register which determines CK1 as the shift clock.
Shift register 2 is a shift register which determines CK2 as the shift clock.

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	
1 to 9	I/O H to I/O A	Parallel data input/output pin Output buffer is of E/E structure	
10	OE	Output enable	
11	V_{DD}	Power supply (+5V)	
12	V_{BB}	Substrate (Connect a capacitor of 1000pF between this pin and ground)	
15	LAT	Data latch signal input pin of shift register 1	*
16	DATA1	Serial data input pin of shift register 1	*
17	CK1	Serial data shift clock input pin of shift register 1	*
18	DATA2	Serial data input pin of shift register 2	*
19	CK2	Serial data shift clock input pin of shift register 2	*
20	OUT2	Serial data output pin of shift register 2 Buffer is of E/E structure	*
21	LOAD	Parallel data input selection input pin of shift register 2	*
22	OUT1	Serial data output pin of shift register 1 Buffer is of E/E structure	*
24	Vss	Ground	

***Note)** Shift register 1 is a shift register which determines CK1 as the shift clock.
Shift register 2 is a shift register which determines CK2 as the shift clock.

Electrical Characteristics

DC Characteristics

(Ta=−20 to +75°C, Vss=0V The condition is determined above-mentioned recommended operating condition otherwise specified.)

Parameter	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	V_{DD}	I_{DD}			30	50	mA
High level output current	All output pins	I_{OH}	V_{OUT}=2.7V			−0.5	mA
Low level output current	All output pins	I_{OL}	V_{OUT}=0.4V	3			mA
High level output voltage	All output pins	V_{OH}	I_{OH}=−0.5mA	2.7			V
Low level output voltage	All output pins	V_{OL}	I_{OL}=3mA			0.4	V
Input leakage current	All input pins	I_{IL}	V_{IN}=0 to 5V	−10		10	μA
High impedance leakage current	I/O A to I/O H	I_{HZ}	V_{OUT}=0 to 5V	−10		10	μA

Switching Characteristics

(Ta=−20 to +75°C, V_{DD}=4.5 to 5.5V)
See next page on Timing chart

Parameter	Pin, remarks	Min.	Typ.	Max.	Unit
DATA1 setup time	to CK1	5			ns
DATA1 hold time	to CK1	5			ns
CK1 setup time 1	to LAT	10			ns
CK1 setup time 2	to LAT	5			ns
LAT setup time	to OE	0			ns
LOAD setup time	to CK2	7			ns
LOAD hold time	to CK2	5			ns
I/O DATA and DATA2 setup time	to CK2	7			ns
I/O DATA and DATA2 hold time	to CK2	5			ns
LAT pulse width		20			ns
OE pulse width		25			ns
LOAD pulse width		20			ns
Clock pulse width	Low level and high level of CK1 and CK2	10			ns

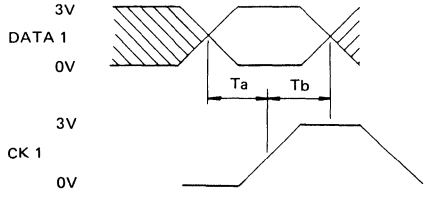
Parameter	From(Input)	To (Output)	Condition	Min.	Typ.	Max.	Unit
Maximum clock frequency	CK1, CK2	OUT1, OUT2				50	MHz
I/O DATA	LAT	I/O A to I/O H	C_L=15pF			25	ns
I/O DATA	OE	I/O A to I/O H	C_L=15pF			17	ns
OUT DATA	CK2	OUT2	C_L=45pF			22	ns
I/O high Z Note)	OE	I/O A to I/O H				20	ns

Note) I/O high Z means the time required for the I/O to become high impedance after the OE signal is inputted.

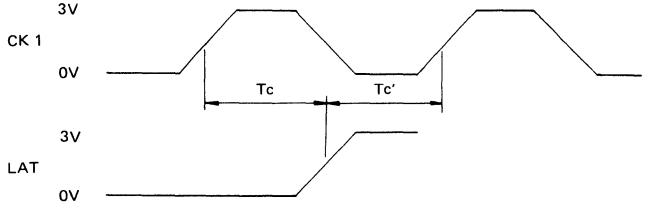
Timing Chart

Note) The input signal level is low level=0V and high level=3V, and 5 ns for both rise and fall. The voltage judgment level for both low level and high level is 1.5V.

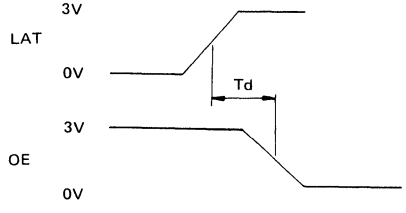
Ta: DATA1 setup time
Tb: DATA1 hold time



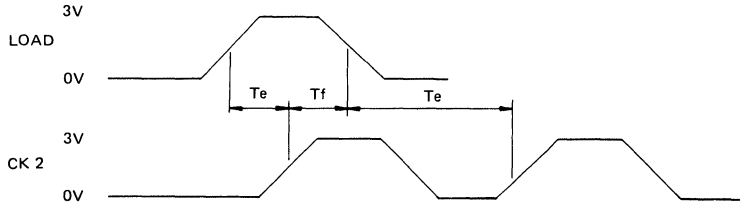
Tc: CK1 setup time 1
Tc': CK1 setup time 2



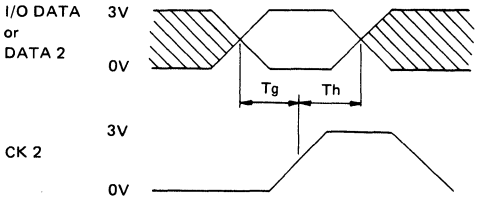
Td: LAT setup time



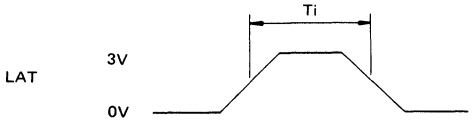
Te: LOAD setup time
Tf: LOAD hold time



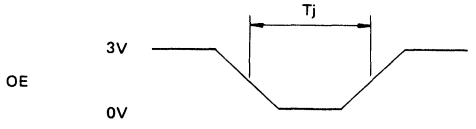
Tg: I/O DATA and DATA2 setup time
Th: I/O DATA DATA2 hold time



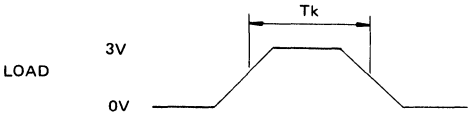
Ti: LAT pulse width



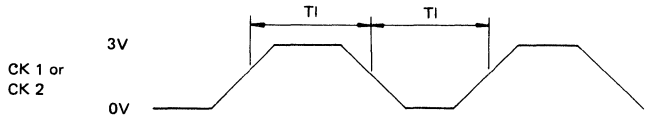
Tj: OE pulse width



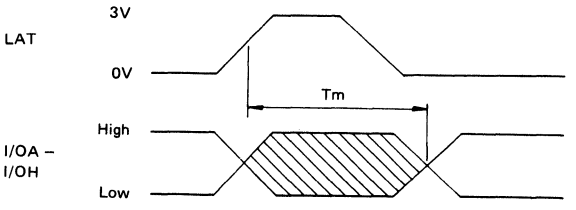
Tk: LOAD pulse width



Tl: Clock pulse width

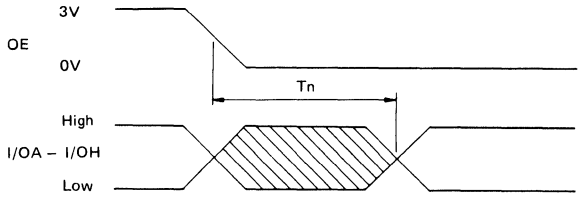


Tm: Time required for I/O DATA confirmation from LAT input

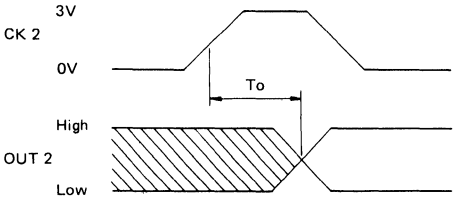


Note The low level and high level are output level of CX23024/CX23067.

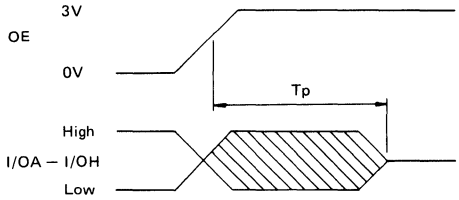
Tn: Time required for I/O DATA confirmation from OE input



To: Time required for OUT2 DATA confirmation from CK2 input



Tp: Time required for I/O to become high impedance from OE input



Description of Operation

(1) Serial data/parallel data conversion mode
Input the 8-bit serial data into the DATA1 pin and its input clock into the CK1 pin and fetch the 8-bit data. The fetched data is latched to the latch circuit by inputting the latch signal to the LAT pin. Thereafter, by inputting the output control signal to the OE pin, the 8-bit serial data is converted to the parallel data and is output to the I/O A through I/O H.

(2) Parallel data/serial data conversion mode
The 8-bit parallel data is fetched by inputting the 8-bit parallel data to the I/O A through I/O H and inputting the load signal into the LOAD pin. By inputting the shift clock into the CK2 pin, the parallel data is converted to the serial data and is output to OUT2 pin.

Digital Filter for CD

Description

The CX23034 is a silicon gate CMOS LSI which has been developed as a digital filter for compact disc player. Excellent filter characteristics can easily be realized by inserting CX23034 between digital signal processing LSI CX23035 for CD and D/A converter.

Features

- Composition of filter:
  - Stereo signal processing with 1 chip
  - Two times sampling rate conversion
  - FIR filter with 16-bit coefficient
  - Filter length 96
- Characteristics of filter:
  - Linear phase
  - Band passing ripple lower than +0.01 dB
  - Stopband attenuation higher than 80 dB
  - Frequency characteristics designed to correct the aperture effect of D/A converter
- Overflow limiter
- Formmats of the output data can be selected either to two's complement or offset binary
- Interface possible with 16-bit serial input D/A converter
- Use together with CX23035 in pair

Structure

Silicon gate CMOS

Absolute Maximum Ratings (Ta=25°C)

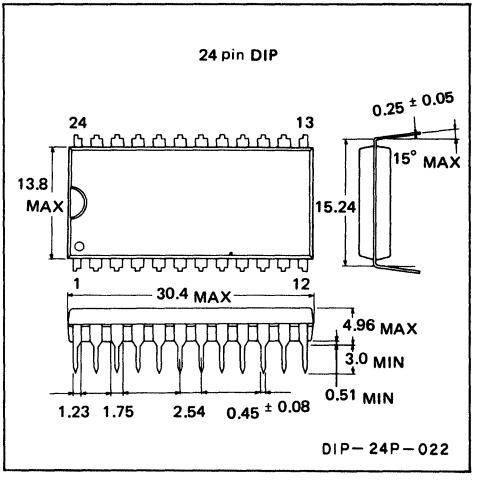
• Power supply voltage	V_{DD}	V_{SS}*	−0.3 to +7.0	V
• Input voltage	V_{IN}	V_{SS}*	−0.3 to +7.0	V
• Output voltage	V_{OUT}	V_{SS}*	−0.3 to +7.0	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

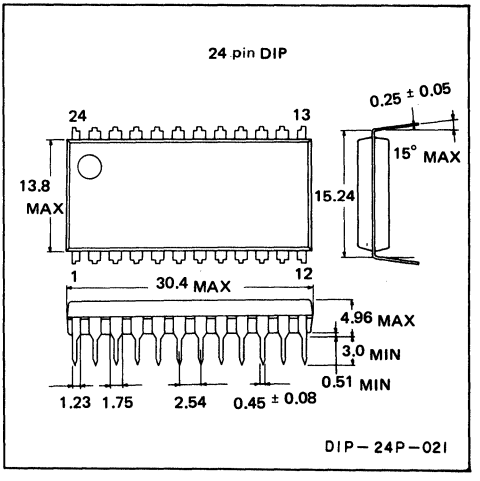
* V_{SS} = 0V

Recommended Operating Conditions

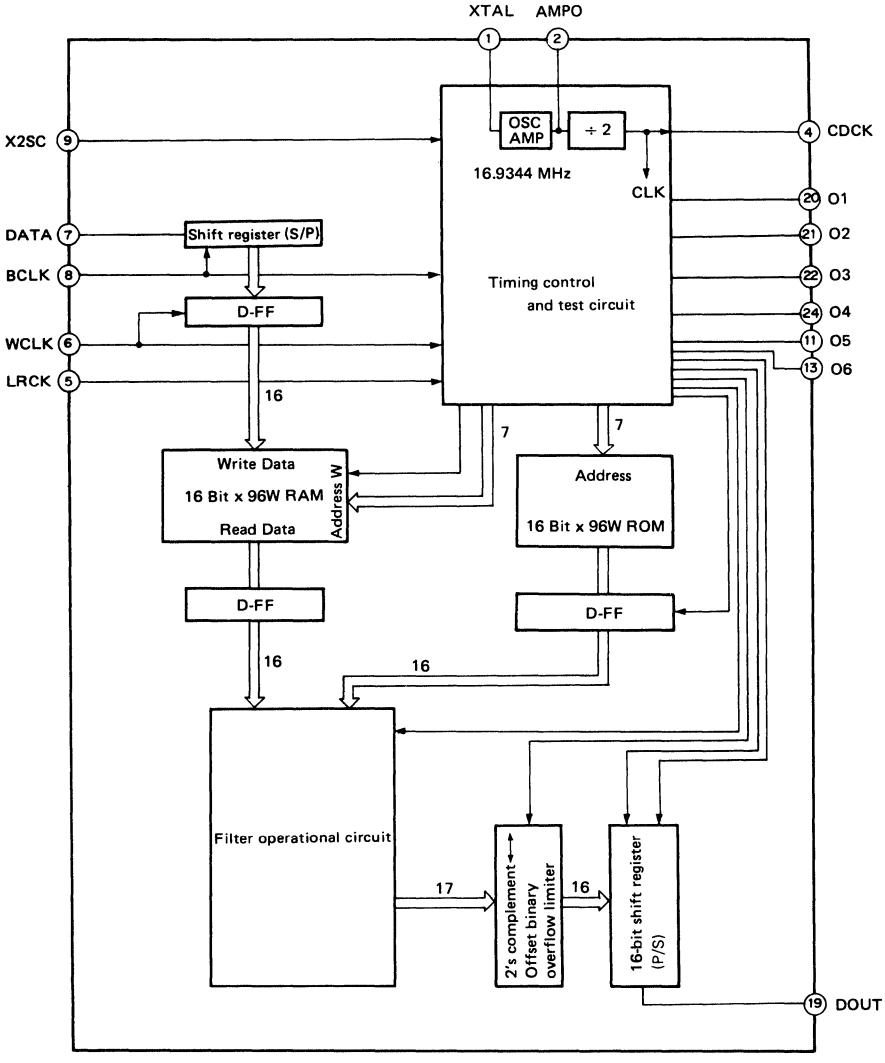
• Power supply voltage	V_{DD}		4.5 to 5.5	V
• Input voltage	V_{IN}	V_{SS}	−0.3 to V_{DD} +0.3	V
• Operating temperature	Topr		−20 to +75	°C

Package Outline Unit: mm

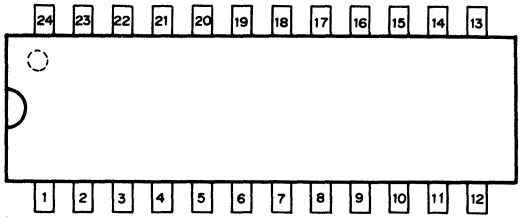




Block Diagram



Pin Configuration (TOP VIEW)



Pin Description

No.	Symbol	I/O	Description
1	XTAL	I	Input for crystal oscillator (16.9344 MHz)
2	AMPO	O	Output for crystal oscillator (16.9344 MHz)
3	TSET1	I	Input for testing (Normally connected to Vss)
4	CDCK	O	Clock output (8.4672 MHz)
5	LRCK	I	44.1 kHz strobe input
6	WCLK	I	88.2 kHz strobe input
7	DATA	I	Serial data input (Two's complement, MSB first)
8	BCLK	I	Bit clock input (input for serial data)
9	X2SC	I	Input for output format selection (High offset binary, low two's complement)
10	TEST2	I	Input for test (normally connected to Vss)
11	O5	O	Timing signal
12	Vss	—	GND pin (0V)
13	O6	O	Timing signal
14	TEST3	O	Test data output (normally open)
15	TEST4	O	Test data output (normally open)
16	TEST5	O	Test data output (normally open)
17	TEST6	O	Test data output (normally open)
18	TEST7	O	Test data output (normally open)
19	DOUT	O	Serial data output (MSB first)
20	O1	O	Timing signal
21	O2	O	Timing signal
22	O3	O	Timing signal
23	O4	O	Timing signal
24	VDD	—	Power supply pin (+5V)

Note) The frequencies shown are values to be used for CD.

Input/Output Capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}		8	12	pF
Output pin	C_{OUT}		10	12	pF

Measuring condition: V_{DD}=V_{IN}=0V, FM=1 MHz

Electrical Characteristics

DC characteristics

V_{DD}=5V±10%, Vss=0V, Topr=−20 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	V_{DD}=5.0V		35		mA
		I_{DDS}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=Vss			0.1	mA
Input voltage (1) H level	A group (note)	V_{IH1}		0.7V_{DD}			V
Input voltage (1) L level		V_{IL1}				0.3V_{DD}	V
Input voltage (2) H level	B group (note)	V_{IH2}		2.2			V
Input voltage (2) L level		V_{IL2}				0.8	V
Output voltage H level	C group (note)	V_{OH}	I_{OH}=1 mA	V_{DD}−0.5		V_{DD}	V
Output voltage L level		V_{OL}	I_{OL}=1 mA	0		0.4	V
Input leakage current	B group (note)	I_{LI}		−5		5	μA

Note) Pins of from A to C groups are shown as below.

A group	XTAL
B group	TEST1, TEST2, X2SC, DATA, BCLK, WCLK, LRCK
C group	CDCK, O1, O2, O3, O4, O5, O6, DOUT, TEST3, TEST4, TEST5, TEST6, TEST7

AC Characteristics

Input AC characteristics Topr=−20 to +75°C, V_{DD}=5V±10%

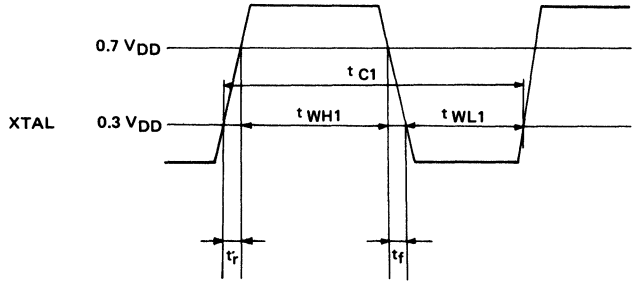
(1) XTAL pin

① In the event crystal oscillator is used

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillating frequency	f_{MAX}			18.432	MHz

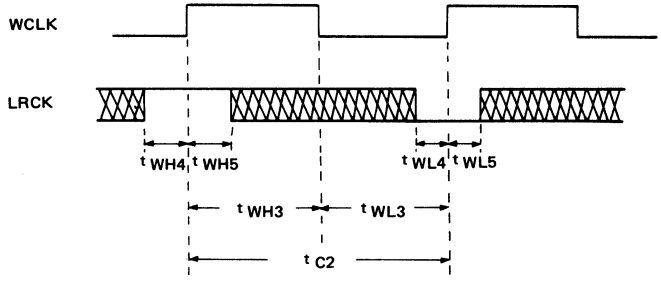
② In the event pulse is input while crystal oscillator is not being used

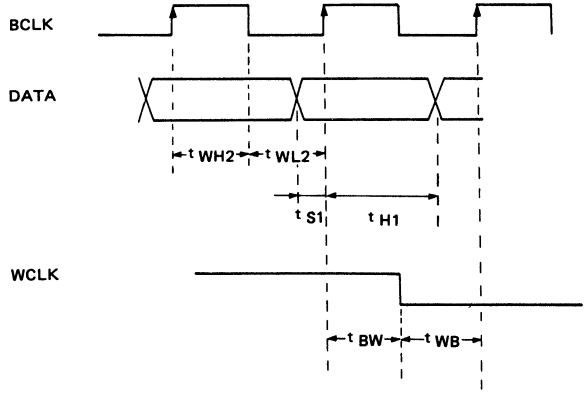
Item	Symbol	Min.	Typ.	Max.	Unit
Pulse cycle	t_{C1}	54	59		ns
"H" level pulse width	t_{WH1}	12	19.5		ns
"L" level pulse width	t_{WL1}	12	19.5		ns
Rising time	t_r		10	15	ns
Falling time	t_f		10	15	ns



(2) DATA, BCLK, WCLK and LRCK pins

Item	Symbol	Min.	Typ.	Max.	Unit
BCLK "H" level pulse width	t_{WH2}	59			ns
BCLK "L" pulse level width	t_{WL2}	48			ns
DATA hotting-up time	t_{S1}	13			ns
DATA holding time	t_{H1}	59			ns
WCLK "H" level pulse width	t_{WH3}	3543		7795	ns
WCLK "L"level pulse width	t_{WL3}	3543		7795	ns
WCLK pulse cycle	t_{C2}		11338		ns
From rising of BCLK to falling of WCLK	t_{BW}	65			ns
From falling of WCLK to rising of BCLK	t_{WB}	22			ns
LRCK "H" level pulse width 1	t_{WH4}	0			ns
LRCK "H" level pulse width 2	t_{WH5}	473			ns
LRCK "L" level pulse width 1	t_{WL4}	0			ns
LRCK "L" level pulse width 2	t_{WL5}	473			ns





Function Explanation

(1) Oscillation circuit

Connect a crystal oscillator with a oscillation frequency of 384 fs (16.9344 MHz) between XTAL pin and AMPO pin, as shown in Fig. 1. In the event crystal oscillation is not used, input clock signal with a frequency of 384 fs to the XTAL pin.

The clock signal of 192fs (8.4672 MHz), which is divided-by 2 of the crystal oscillation frequency, is output from the CDCK pin.

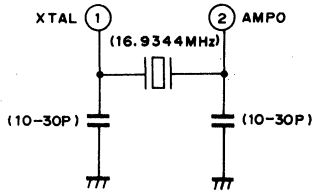


Fig. 1 Oscillation circuit

[The values shown in parentheses are those used for CD]

(2) Regarding initialization

The initialization of this LSI requires a XTAL time of approx. 770 clocks after the power supply is turned on, provided that all inputs are in normal condition. (It takes approx. 46 μs when XTAL 16.9344 MHz.) The output is not valid until the initialization is completed.

(3) Interface with signal processing LSI

Interfacing with the signal processing LSI can be carried out as shown in Fig. 2.

The input data 16 bit (two's complement) is input to DATA pin with MSB first, and individual bits of DATA input are fetched into the shift register within the IC at rising of BCLK. Accordingly, individual bits of DATA input should be changed at the falling of BCLK. Thus, 16 bits of data in the shift register within the LSI at the falling of WCLK is latched as a writting data of RAM.

Therefore, BCLK signal requires at least 16 pulses during its falling time of WCLK to the next falling time of same. If the BCLK signal has 17 pulses or over during its falling time of WCLK to the next falling time of same, 16 bits before WCLK falling time become writting data of RAM.

The input data becomes L-ch signal when LRCK is "H", and R-ch signal when LRCK is "L".

(4) Interface with D/A converter

It enables to be interfaced with various D/A converter by using X2SC pin. The output timing chart is as shown in Fig. 2.

X2SC (Switchover of offset binary two's complement)

X2SC = "H" offset binary

X2SC = "L" two's complement

Offset binary is MSB inverse of two's complement.

(5) Regarding synchronizing with input and output signals

If the relative relation between rising of WCLK when LRCK is "L" and output signal differs by more than 2 clocks of CDCK (236 ns), the operation within the IC is momentarily stopped, and synchronization of input signal and output signal is performed again.

(6) Regarding frequency characteristics of filter

The frequency characteristics of this LSI are as shown in Figs. 3 and 4.

(7) Correction of aperture effect frequency characteristics of D/A converter

The digital output of this LSI is output after correcting the frequency characteristics against the aperture effect of the D/A converter. In addition, this correction is carried out on the assumption that the sample and hold type DEGRETCHER is used as an analog output of the D/A converter.

Timing Chart

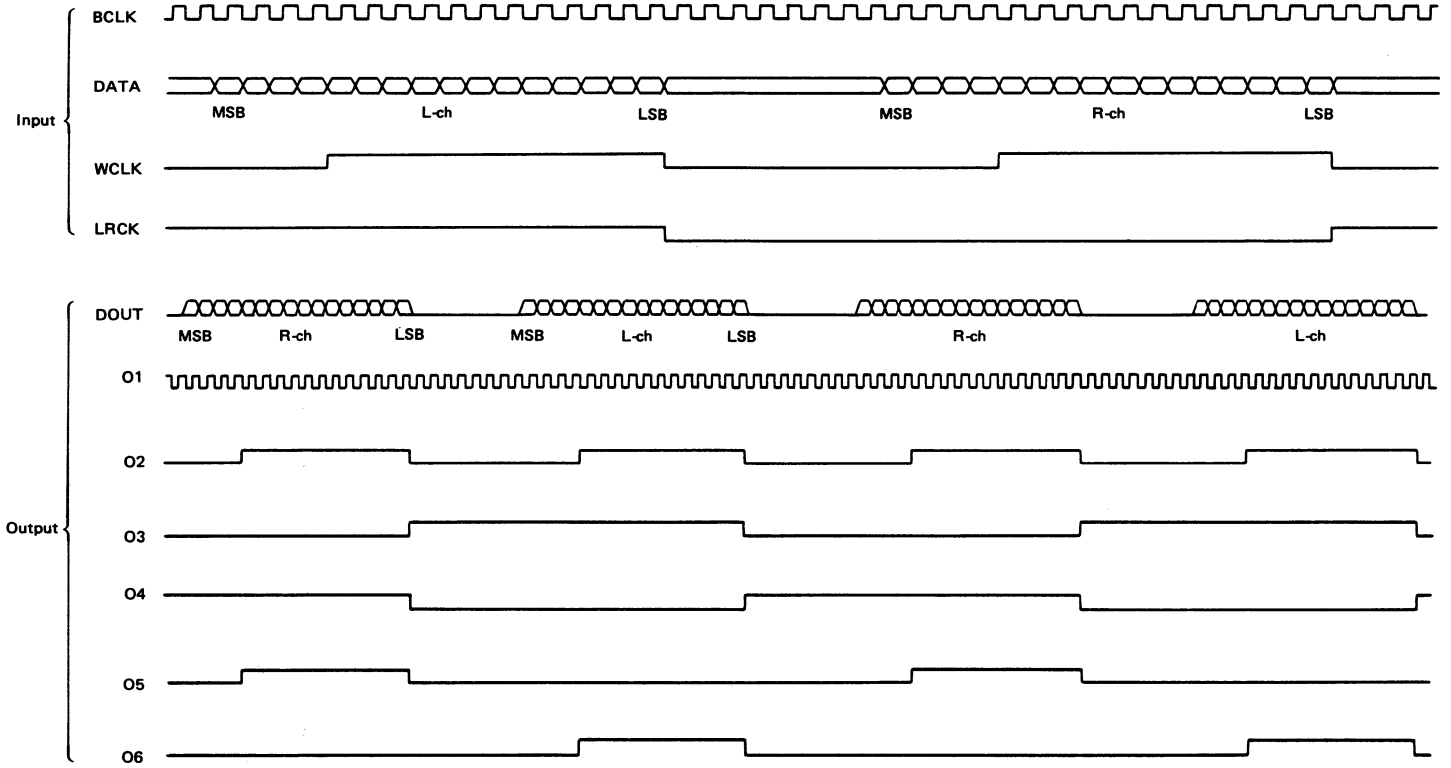


Fig. 2 CX23034 timing chart

SONY

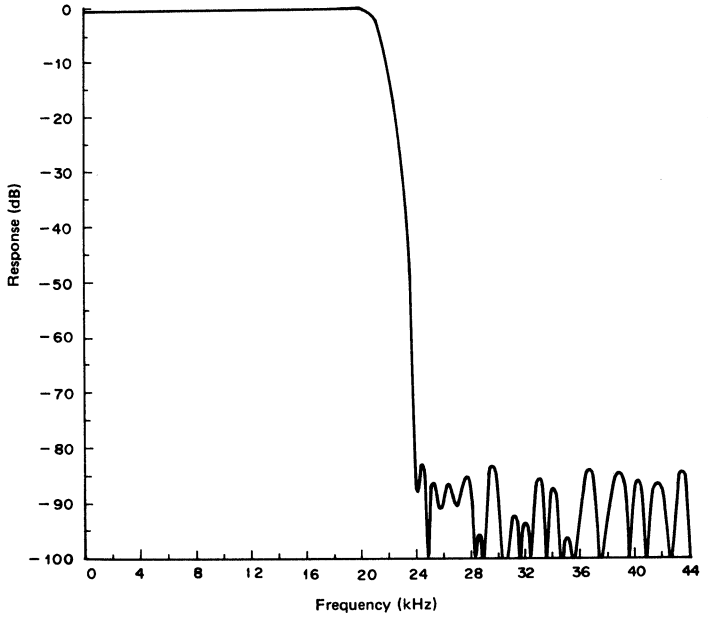


Fig. 3 Frequency characteristics

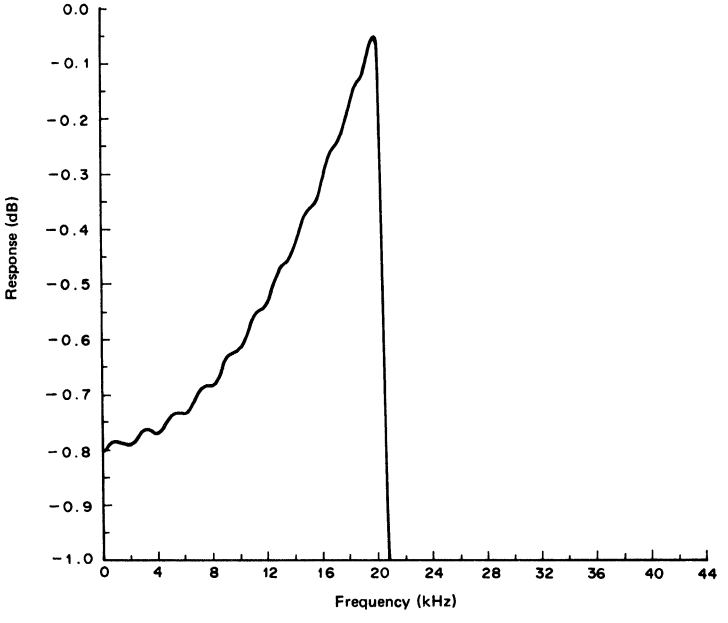
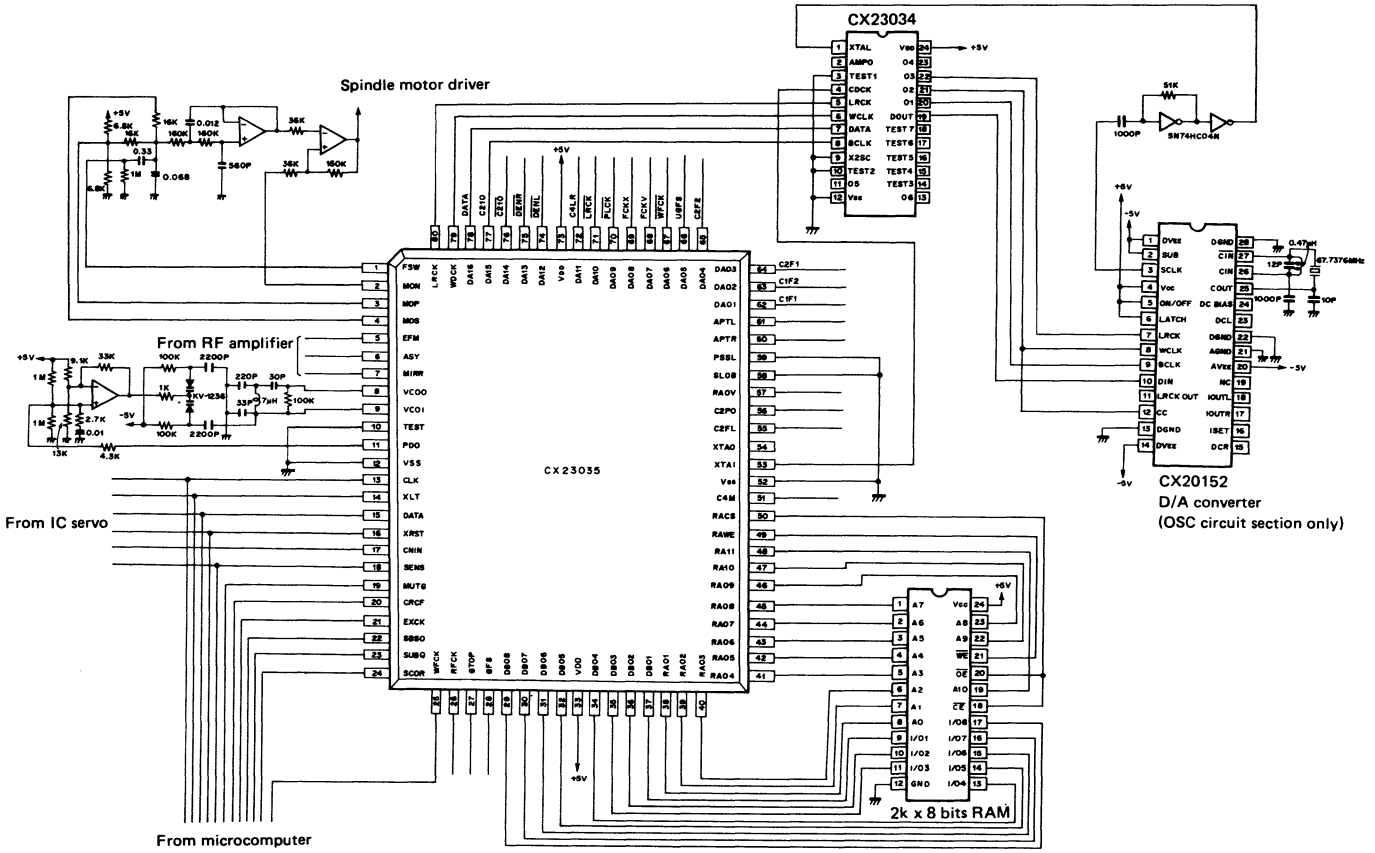


Fig. 4 Band passing characteristics

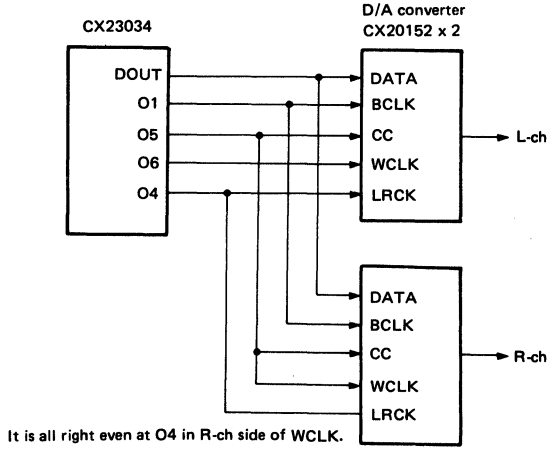
Example of Application Circuit

(1) Connection of CX23034, CX23035 and CX20152



SONY

(2) L-ch and R-ch same phase connection method

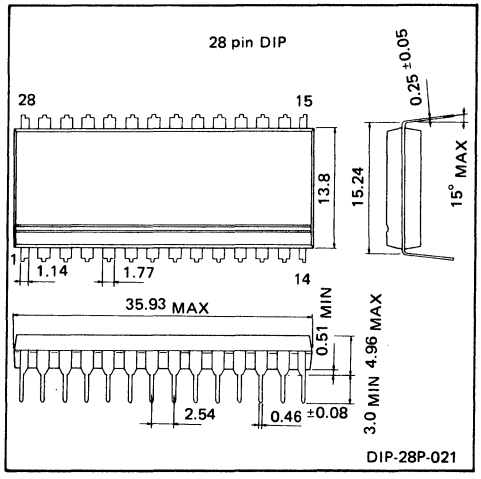


Programmable Shift Register

Description

The CX23038 is an LSI which has a programmable shift register (PSR) circuit, bit slice delay PSR circuit, and number of dynamic stages selecting function.

Package Outline Unit: mm



Features

- 5V single power supply
- Low power consumption 250 mW (Typ.)
- Operates by the sampling signal (14.3 MHz) of the standard TV signal.
- Capable of setting various kinds of operating modes

Structure

Silicon gate CMOS

Absolute Maximum Rating (Ta=25°C)

• Supply voltage	V_{DD}	V_{SS}−0.5 to +7.0	V
• Input voltage	V_I	V_{SS}−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}−0.5 to V_{DD}+0.5	V
• Operating temperature	Topr	0 to +70	°C
• Storage temperature	Tstg	−55 to +150	°C

Note) V_{SS}=0V

Recommended Operating Conditions

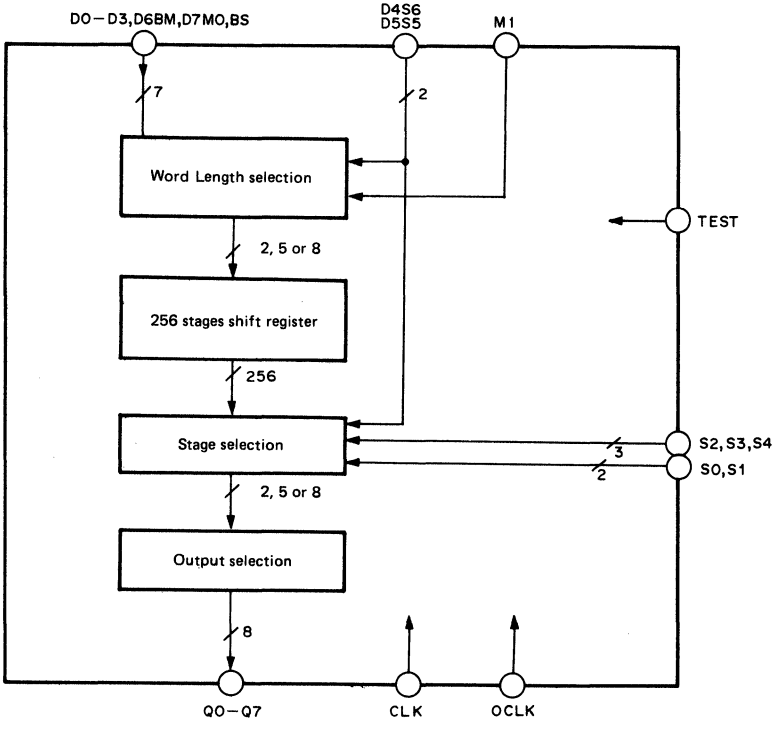
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	0 to +70	°C

Input/Output Capacity

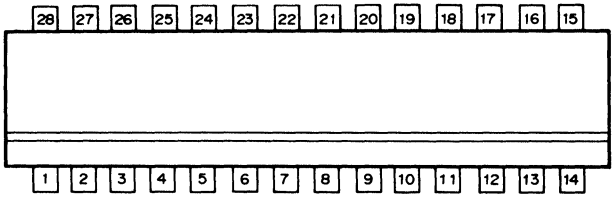
• Input pin	C_{IN}	9	pF
• Output pin	C_{OUT}	9	pF
• I/O pin	$C_{I/O}$	11	pF

Measuring condition V_{DD}=V_I=0V, f_M=1 MHz

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	D0	I	Data input pin
2	D1	I	Data input pin
3	D2	I	Data input pin
4	D3	I	Data input pin
5	D4S6	I	Data or stage selecting signal input pin
6	D5S5	I	Data or stage selecting signal input pin
7	GND	—	GND pin
8	CLK	I	Main clock input pin
9	D6BM	I	Data or bit slice delay form determining signal input pin
10	D7M0	I	Data or word length selecting signal input pin
11	M1	I	Word length selecting signal input pin
12	S4	I	Stage selecting signal input pin
13	S3	I	Stage selecting signal input pin
14	S2	I	Stage selecting signal input pin
15	TEST	I	Test input pin Normally at "L".
16	BS	I	Bit slice delay switching signal input pin
17	S1	I	Stage selecting signal input pin
18	S0	I	Stage selecting signal input pin
19	Q7	O	Data output pin
20	Q6	O	Data output pin
21	V_{DD}	—	+5V power supply
22	OCLK	I	Output clock pin
23	Q5	O	Data output pin
24	Q4	O	Data output pin
25	Q3	O	Data output pin
26	Q2	O	Data output pin
27	Q1	O	Data output pin
28	Q0	O	Data output pin

Electrical Characteristics

DC characteristics

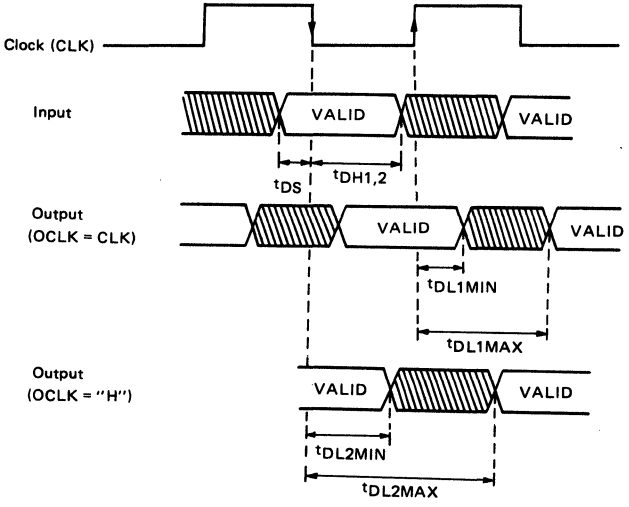
V_{DD}=5V ±5%, V_{SS}=0V, Topr=0 to 70°C

Item		Symbol	Condition	Min.	Max.	Unit
Power supply current		I_{DDS}	Static state $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	0	0.1	mA
Output voltage	H level	V_{OH}	I_{OH}=−0.4mA	4.0	V_{DD}	V
	L level	V_{OL}	I_{OL}=3.2mA	V_{SS}	0.4	V
Input voltage	H level	V_{IH}		2.2		V
	L level	V_{IL}			0.8	V
Input leakage current		I_{LI}	V_I=0V to V_{DD}	−10	10	μA
Input leakage current (During the tri-state pin input)		I_{LZ}		−40	40	μA

AC characteristics

V_{DD}=5V ±5%, V_{SS}=0V, Topr=0 to 70°C, C_L=60 pF

Item	Pin name	Symbol	Min.	Max.	Unit
Maximum clock frequency	CLK, OCLK	f_{CK}	14.32		MHz
Input data set up time	D0 to D3, D4S6, D5S5, D6BM, D7M0, M1, BS, S0 to S4	t_{DS}	4		ns
Input data hold time	D0 to D3, D4S6, D5S5, D6BM, D7M0, M1, BS	t_{DH1}	22		ns
	S0 to S4	t_{DH2}	14		
Output data delay from OCLK (Note 1 OCLK=CLK)	Q0 to Q7	t_{DL1}	7	36	ns
Output data delay from CLK (Note 2 OCLK=H)	Q0 to Q7	t_{DL2}	22	58	ns



Description of Functions

The CX23038 has the following modes.

(1) PSR 2-bit mode
(2) PSR 5-bit mode
(3) PSR 8-bit mode

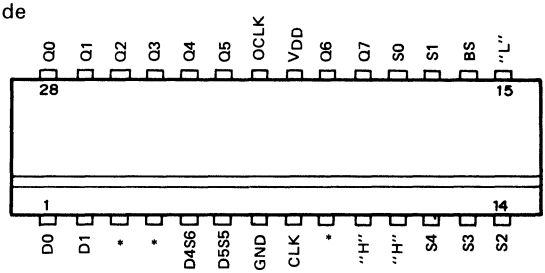
The relationship between each modes and D7M0 and M1 pins is as follows:

	D7M0	M1
PSR 2-bit mode	H	H
PSR 5-bit mode	L	H
PSR 8-bit mode	d	L

Here d denotes that it is an input pin of data.

<Description of respective mode>

① 2-bit mode



* Fixed at "L" or "H"

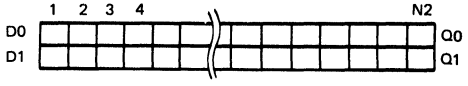
The data is input from D0 and D1 and output from the respective Q0 and Q1 after passing through the stages which specified by the stage selecting signal.
The S0, S1, S2, S3, S4, D5S5 and D4S6 are the input pins of the stage selecting signal. Here, assuming that

(i) D4S6="H" $N_2=2^6+2^4\times S4+2^3\times S3+2^2\times S2+2\times S1+S0+4$

(ii) D4S6="L" $N_2=2^5\times D5S5+2^4\times S4+2^3\times S3+2^2\times S2+2\times S1+S0+4$

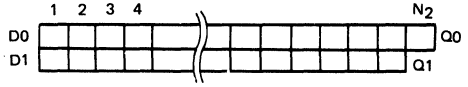
At this point, the number of stages of the shift registers become as shown in figure below.

(i) BS=L



Where, $4 \leqq N_2 \leqq 131$

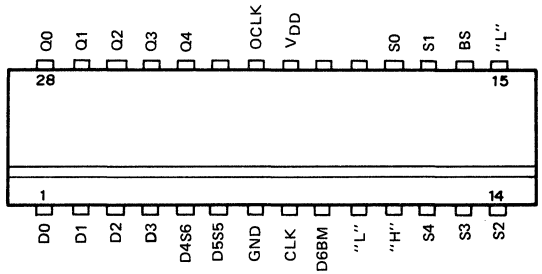
(ii) BS=H



Where, $5 \leqq N_2 \leqq 131$

In addition, the stage selecting signal determines number of the output stages after 3 clocks. Moreover, the data input from D0 and D1 are output from Q2 and Q3 respectively, after passing through the 128 stages DFF (When BS="H", D1 is 127 stages). $\overline{Q0}$ and $\overline{Q1}$ are output respectively from Q4 and Q5. From Q6 and Q7, similar data to Q0 and Q1 are output respectively.

② 5-bit mode



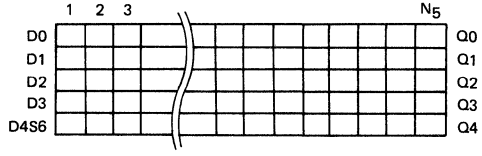
The data is input from D0, D1, D2, D3 and D4S6 and output from Q0, Q1, Q2, Q3 and Q4 respectively, after passing through the stages which is specified by the stage selecting signal. The S0 to S4 and D5S5 are the input pins of the stage selecting signal. Now, assuming that

(i) D5S5="H" $N_5=2^5+2^2\times S2+2S1+S0+4$

(ii) D5S5="L" $N_5=2^4S4+2^3\times S3+2^2\times S2+2\times S1+S0+4$

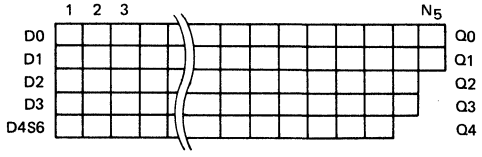
At this point, the number of stages of the shift register become as shown in figure below.

(i) BS=L



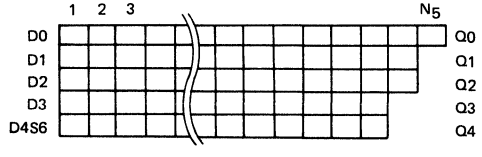
Where, $4 \leqq N_5 \leqq 51$

(ii) BS=H and D6BM=L



Where, $6 \leqq N_5 \leqq 51$

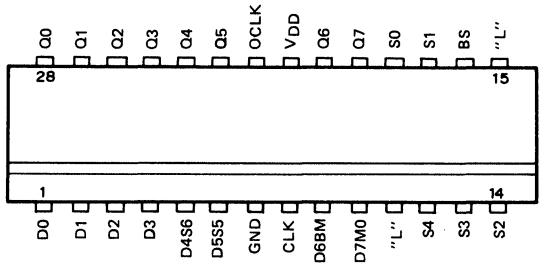
(iii) BS=H and D8BM=H



Where, $6 \leqq N_5 \leqq 51$

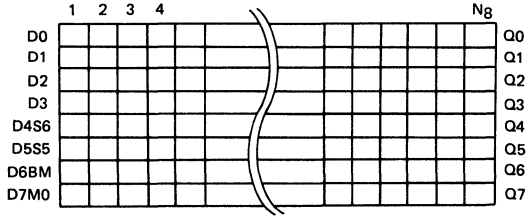
The stage selecting signal determines the number of the output stages after 3 clocks.

③ 8-bit mode



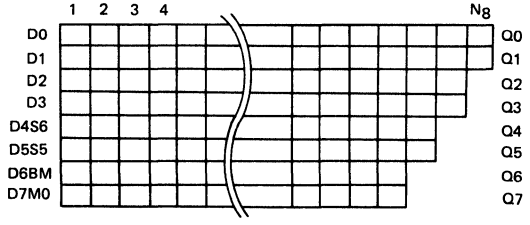
The data is input from D0, D1, D2, D3, D4S6, D5S5, D6BM and D7M0 pins and output from Q0, Q1, Q2, Q3, Q4, Q5, Q6 and Q7 respectively, after passing through the stages specified by the stage selecting signal. The S0 to S4 are the input pins of the stage selecting signal. The S0 to S4 determine the number of the output stages after 3 clocks. Now, assuming that $N_8=2^4\times S4+2^3\times S3+2^2\times S2+2\times S1+S0+4$, the number of stages of the shift register become as shown in figure below.

(i) BS=L



Where, $4 \leqq N_8 \leqq 35$

(ii) BS=H

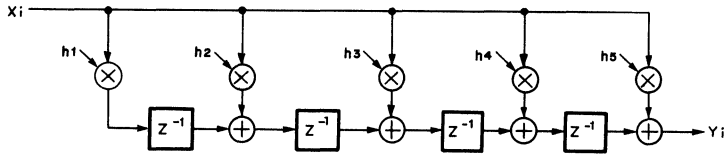


Where, $7 \leqq N_8 \leqq 35$

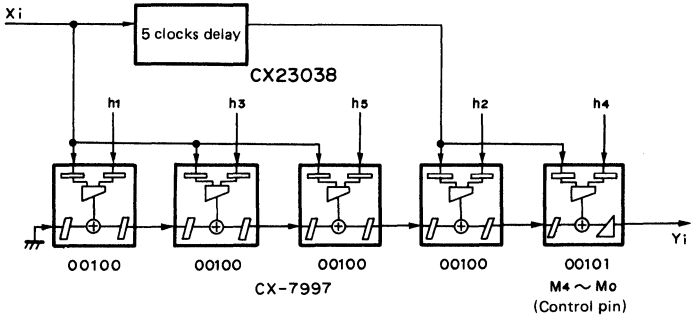
Application Circuits

(1) Example of FIR Digital Filter

$$5\ TAP\ Yi = \sum_{j=0}^{4} h_{(5-j)} \cdot X_{(i-j)}$$



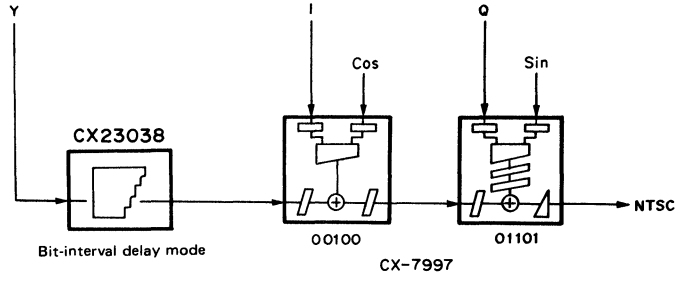
Combination of the CX-7997 and CX23038



(2) Example of NTSC Encoder

$$NTSC = Y + I \cdot \cos(Wsc \cdot t + \phi) + Q \cdot \sin(Wsc \cdot t + \phi)$$

Combination of the CX-7997 and CX23038



* When the chroma signal is picked up which has been modulated as shown in Fig. above, the CX23038 of the bit-interval delay mode is used.

10 bit Synchronous Binary Counter

Description

The CX23043 is a 10 bit synchronous binary counter designed using SONY's high-speed N-channel silicon-gate MOS technology.

Features

- The maximum operating clock frequency of 30 MHz is warranted.
- Single +5V supply.
- Directly TTL compatible: All inputs and outputs
- Low power consumption (Typ. 100 mW).
- Provided with ENABLE T and ENABLE P input.
- Provided with $\overline{\text{LOAD}}$ input.
- Provided with $\overline{\text{OE}}$ input.
- Plural cascade connections are possible.

Structure

N-channel silicon-gate E/D MOS

Applications

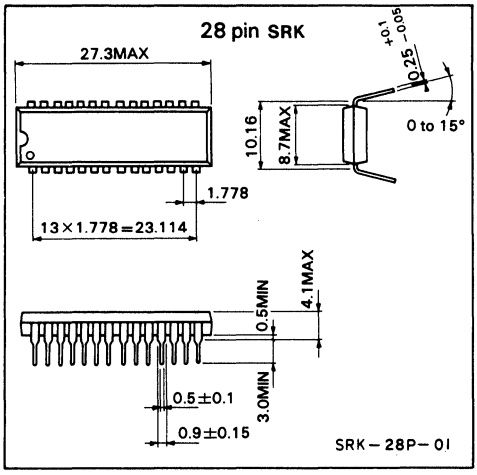
- Programmable counter
- Memory address generation

Functions

Synchronous 10 bit binary counter

Package Outline

Unit: mm



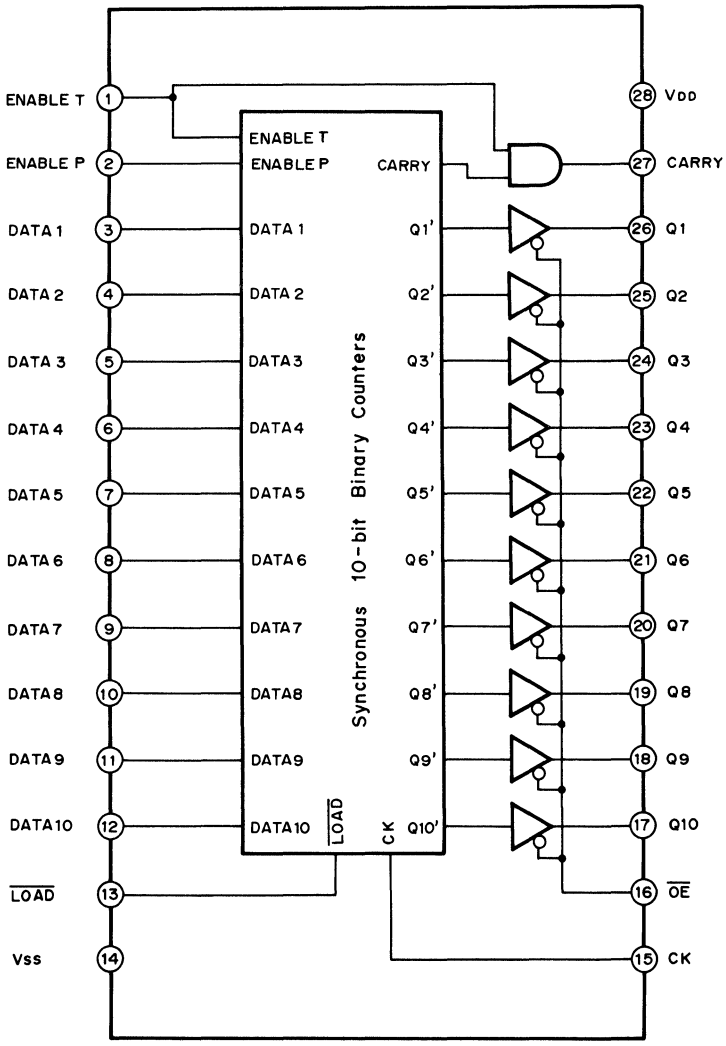
Absolute Maximum Ratings (Vss = 0V, Ta = 25°C)

• Power supply voltage	VDD	−0.5 to +7	V
• Input terminal voltage	VIN	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	500	mW

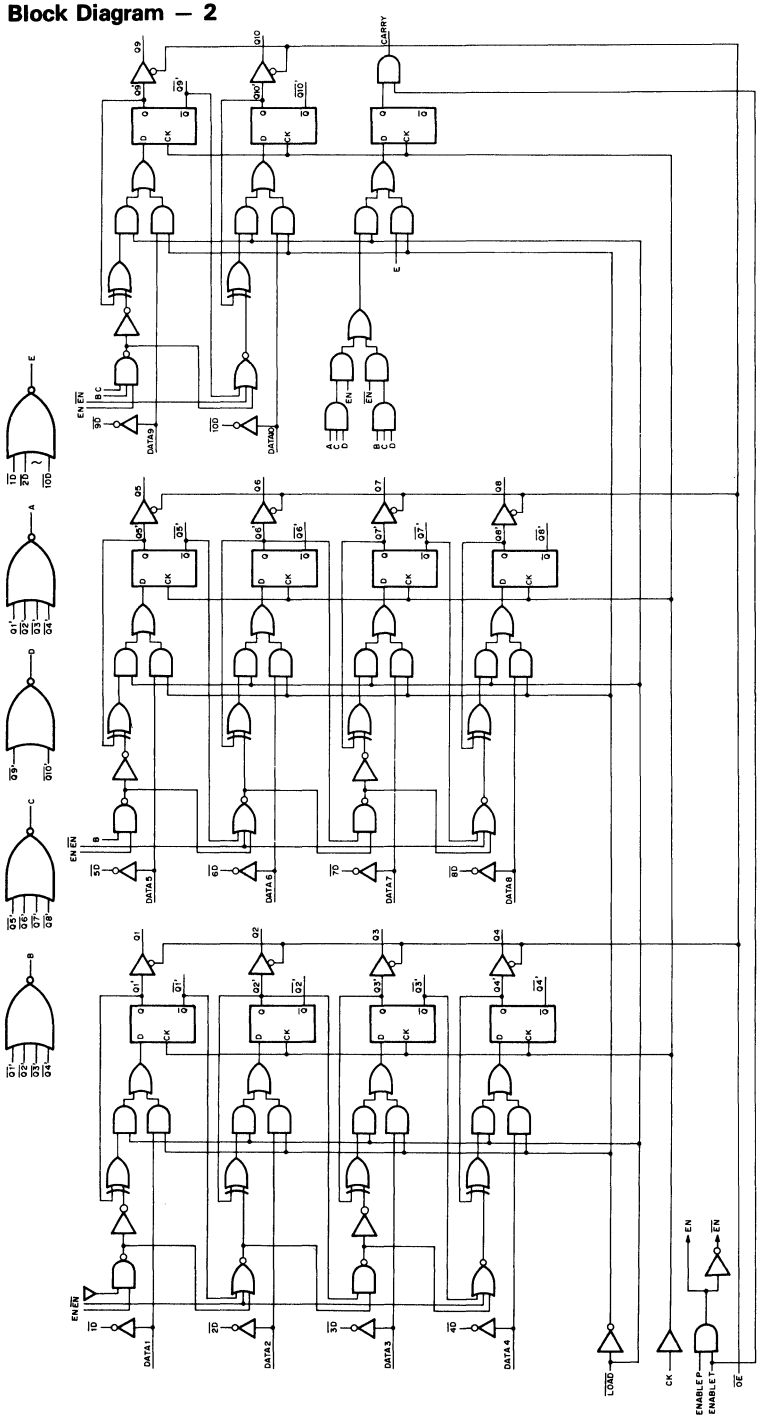
Recommended Operating Conditions (Vss = 0V)

• Power supply voltage	VDD	+4.5 to +5.5	V
• Operating temperature	Topr	−20 to +75	°C
• High level input voltage	VIH	+2.0 to VDD+0.5	V
• Low level input voltage	VIL	−1.0 to +0.8	V

Block Diagram – 1



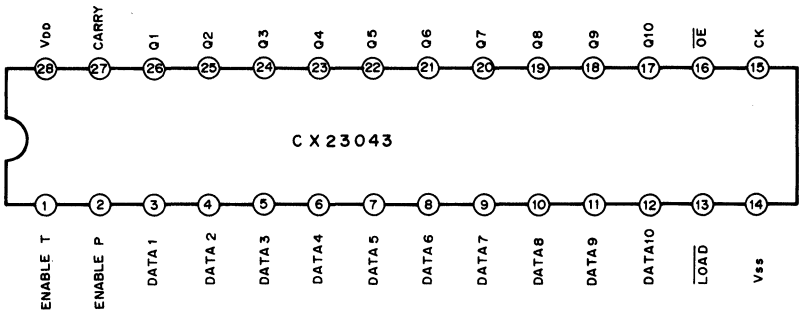
Block Diagram – 2



FUNCTION TABLE

ENABLE T	ENABLE P	COUNTER	CARRY
L	L	INACTIVE	L
L	H	INACTIVE	L
H	L	INACTIVE	ACTIVE
H	H	ACTIVE	ACTIVE

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description
1	ENABLE T	Counter enable input terminal (CK, CARRY controlled)
2	ENABLE P	Counter enable input terminal (CK only controlled)
3 to 12	DATA1 to DATA10	Data input terminal
13	$\overline{\text{LOAD}}$	Data input control terminal
14	V_{SS}	Ground terminal
15	CK	Clock input terminal
16	$\overline{\text{OE}}$	Data output control terminal
17 to 26	Q10 to Q1	Data output terminal; output buffer is E/E composed.
27	CARRY	Carry output terminal; output buffer is E/E composed.
28	V_{DD}	Power supply (+5V)

Electrical Characteristics

(1) D.C Electrical Characteristics

(V_{SS} = 0V. Unless otherwise specified, the conditions are as per the recommended operating conditions described above.)

Item	Terminal	Symbol	Condition	Min	Typ	Max	Unit
Power supply current	V_{DD}	I_{DD}	Note 2		20	30	mA
High level output current	All output terminals	I_{OH}	Vout = 2.7V			−0.1	mA
Low level output current	All output terminals	I_{OL}	Vout = 0.4V	3			mA
High level output voltage	All output terminals	V_{OH}	I_{OH} = −0.1mA	2.7			V
Low level output voltage	All output terminals	V_{OL}	I_{OL} = 3mA			0.4	V
Input leakage current	All input terminals	I_{IL}	V_{IN} = 0 to V_{DD} Note 1	−10		10	μA
Hi-impedance leakage current	Q1 to Q10	I_{HZ}	V_{OUT} = 0 to V_{DD} Note 1	−10		10	μA

Note 1 Ta = 25°C
Note 2 V_{DD} = 5V, Ta = 25°C

(2) A.C Electrical Characteristics

(Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, see next page for timing chart)

Item	Terminal note	Min	Typ	Max	Unit
ENABLE T setup time	to CK	20			ns
ENABLE T holding time	to CK	5			ns
ENABLE P setup time	to CK	20			ns
ENABLE P holding time	to CK	5			ns
DATA setup time	to CK	10			ns
DATA holding time	to CK	10			ns
$\overline{\text{LOAD}}$ setup time	to CK	10			ns
$\overline{\text{LOAD}}$ holding time	to CK	10			ns
Clock pulse width	Low or High	15			ns

Item	Input	Output	Condition	Min	Typ	Max	Unit
Maximum operating frequency	CK	Q1 to Q10 CARRY	C_L = 30pF	30			MHz
Data	CK	Q1 to Q10	C_L = 30pF			27	ns
Carry	CK	CARRY	C_L = 30pF			30	ns
Carry	ENABLE T	CARRY	C_L = 30pF			25	ns
Data	$\overline{OE}$	Q1 to Q10	C_L = 30pF			27	ns
HIGH Z Note 1	$\overline{OE}$	Q1 to Q10	C_L = 30pF			20	ns

Note 1) Time required for the output Q1 to Q10 to go from $\overline{OE}$ to a high impedance.

(3) A.C Electrical Characteristics

(Ta = +25°C, V_{DD} = 5.0V, V_{SS} = 0V, see next page for timing chart)

Item	Terminal note	Min	Typ	Max	Unit
ENABLE T setup time	to CK		10		ns
ENABLE T holding time	to CK		−2		ns
ENABLE P setup time	to CK		10		ns
ENABLE P holding time	to CK		−2		ns
DATA setup time	to CK		1		ns
DATA holding time	to CK		3		ns
$\overline{LOAD}$ setup time	to CK		3		ns
$\overline{LOAD}$ holding time	to CK		2		ns
Clock pulse width	Low or High		10		ns

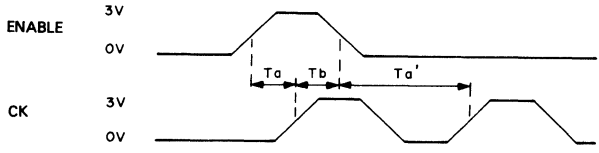
Item	Input	Output	Condition	Min	Typ	Max	Unit
Maximum operating frequency	CK	Q1 to Q10 CARRY	C_L = 30pF		50		MHz
Data	CK	Q1 to Q10	C_L = 30pF		18		ns
Carry	CK	CARRY	C_L = 30pF		20		ns
Carry	ENABLE T	CARRY	C_L = 30pF		16		ns
Data	$\overline{OE}$	Q1 to Q10	C_L = 30pF		18		ns
HIGH Z Note 1	$\overline{OE}$	Q1 to Q10	C_L = 30pF		10		ns

Note 1) Time required for the output Q1 to Q10 from to go $\overline{OE}$ to a high impedance.

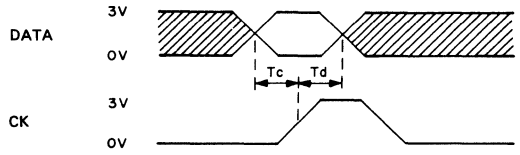
Timing Chart

Note 1) Input signal level is Low level = 0V, High level = 3V, 5 nsec both for rise and fall.
2) Voltage determination level is 1.5V for Low and High levels.

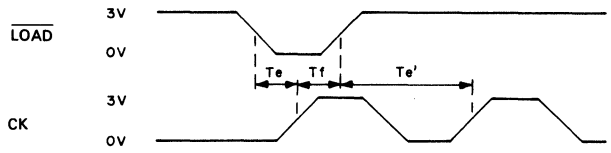
Ta, Ta' : ENABLE T setup time, ENABLE P setup time
Tb : ENABLE T holding time, ENABLE P holding time



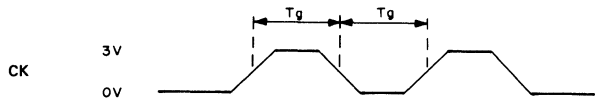
Tc : DATA setup time
Td : DATA holding time



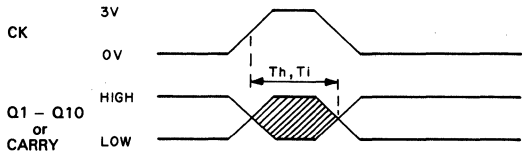
Te, Te' : $\overline{\text{LOAD}}$ setup time
Tf : $\overline{\text{LOAD}}$ holding time



Tg : Clock pulse width

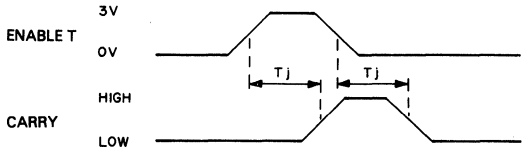


Th : Time from clock input to the determination of binary data
Ti : Time from clock input to the determination of carry data

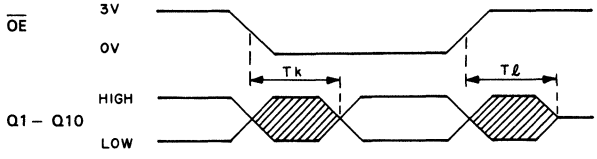


Note) Low and High are the CX23043 output level.

Tj : Time from the ENABLE T input to the determination of carry data



Tk : Time from $\overline{OE}$ input to the determination of binary data
Tℓ : Time from $\overline{OE}$ input to the output high impedance



Description of Operations

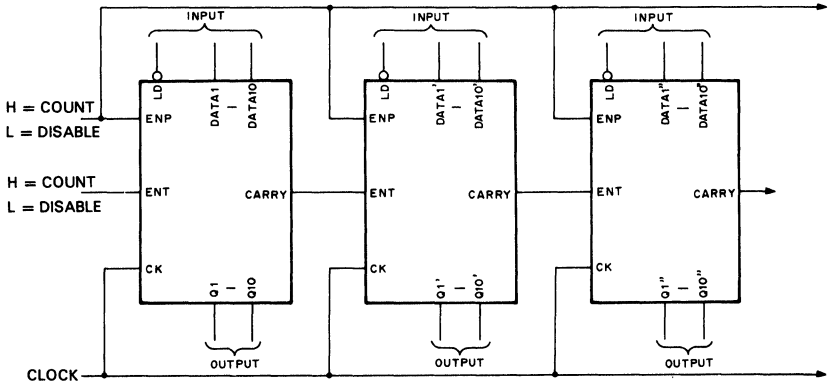
The CX23043 is a synchronous 10 bit binary counter. Data is input to DATA1 to DATA10 with the $\overline{\text{LOAD}}$ at low level, then CK is input and data is loaded in the output terminals Q1 to Q10 with the rise of CK regardless of the ENABLE level (high or low).

When the ENABLE T and P are at high level, the counter is in operation. When either ENABLE is at low level, the counter is in recess. When the ENABLE T is at low level, the CARRY output enters low level.

When $\overline{\text{OE}}$ is at low level, the output buffer (Q1 to Q10) is in operation. When the $\overline{\text{OE}}$ is at high level, the output buffer (Q1 to Q10) outputs high impedance.

Application Example

Connection of plural cascades is as follows.



SONY **CXD1018G**

Digital Signal Processing Multiplier

Description

The CXD1018G is a 16-bit·32-bit→36-bit parallel multiplier.

Features

- For X inputs (16-bit), either one of two types, 2'S complements and unsigned straight binaries, may be selected.
- By employing a Booth algorithm + Wallace tree + CLA adder structure, this LSI enables high speed operations (at 75 ns typ.)
- Incorporates a 36-bit accumulator.
- With its mode selection, the LSI serves either as the multiplier for an CX23015 (audio signal processor) (also corresponds to a two CX23015s employing mode), or as a general purpose multiplier-adder.
- When its extension output pins (PSGN and ARCO) are utilized to have a 4-bit full adder and a 4-bit register connected externally, a 40-bit accumulator structure may be enabled.
- Low power consumption (at 100 mW typ.)

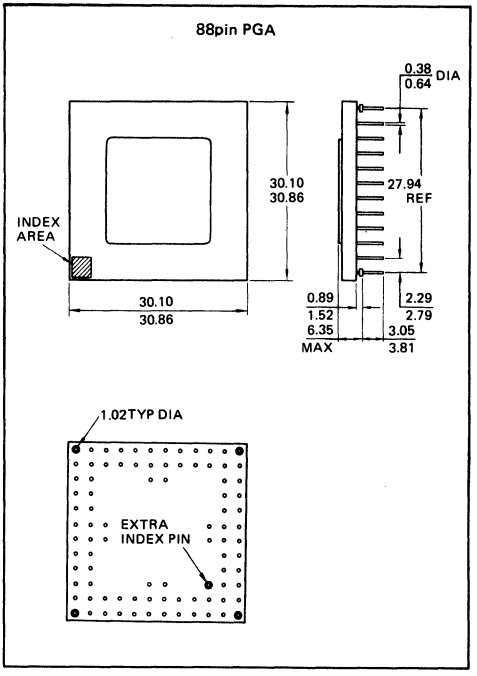
Function

Multiplier

Structure

Silicon gate CMOS IC

Package Outline Unit: mm



Absolute Maximum Ratings (Ta=25°C)

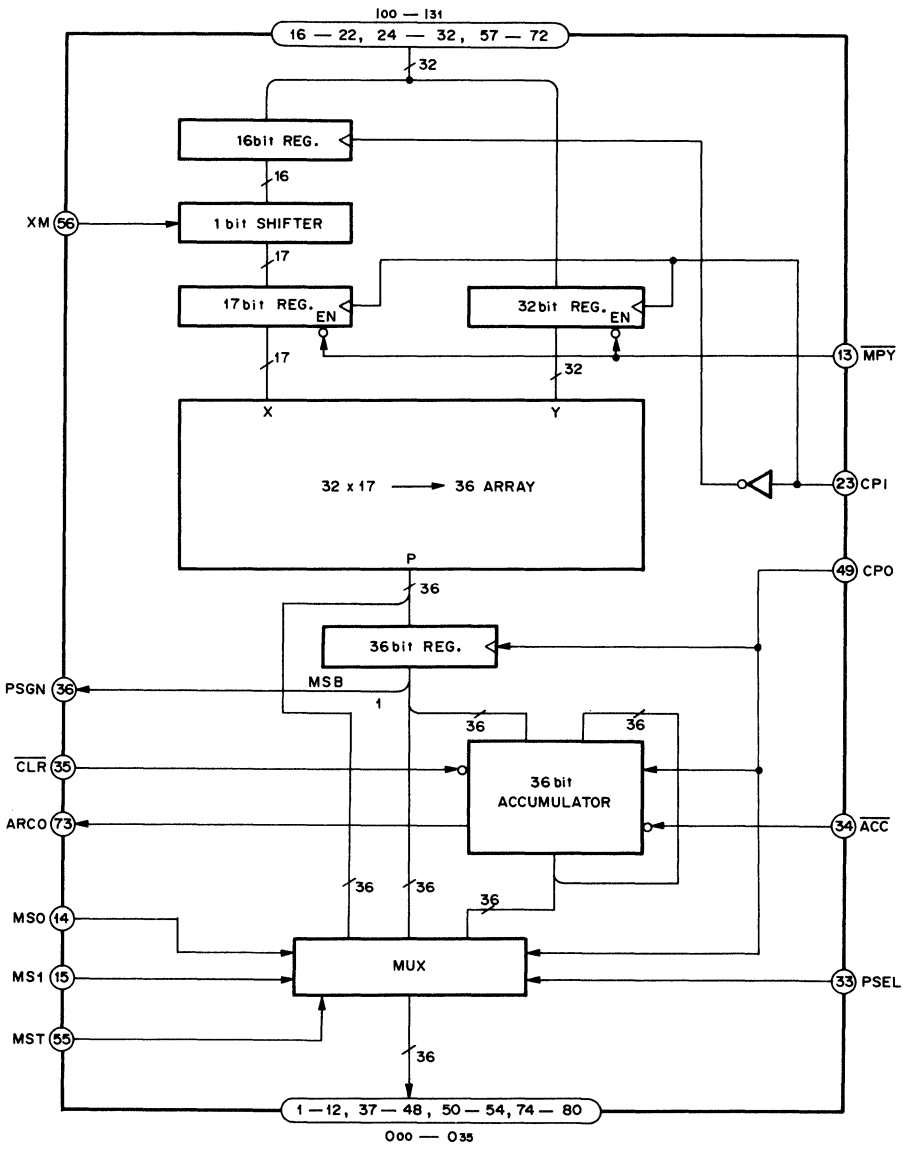
• Supply voltage	V_{DD}	V_{SS}* −0.5 to 7.0	V
• Input voltage	V_I	V_{SS}* −0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}* −5.0 to V_{DD}+0.5	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−40 to +125	°C

* V_{SS}=0V

Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0±0.25	V
• Operating temperature	Topr	−20 to +75	°C

Block Diagram



Electrical Characteristics

1. DC characteristics

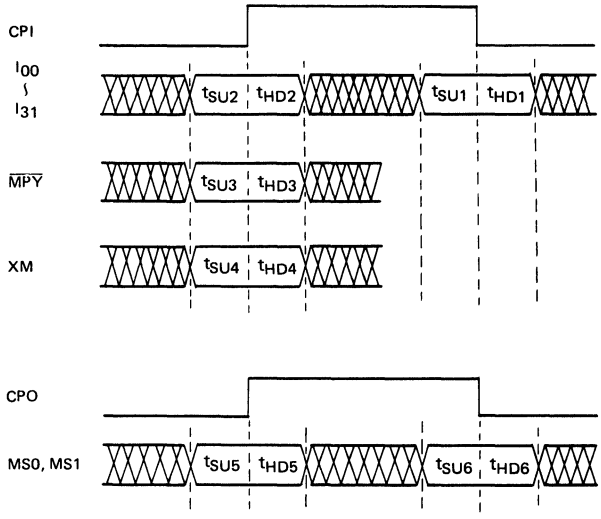
V_{DD}=5V±5% Vss=0V Topr=−20 to 75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current		I_{DD}			20		mA
		I_{DDS}	Standby state*			0.1	mA
Output voltage	H level	V_{OH}	I_{OH}=−0.4 mA	4.0		V_{DD}	V
	L level	V_{OL}	I_{OL}=3.2 mA	Vss		0.4	V
Input voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{LI}	V_I=0V to V_{DD}	−10		10	μA

* $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$

2. AC characteristics

Item	Symbol	Typ.	Max.	Unit	Remark
I_{00} to I_{31} Set-up time 1	t_{SU1}	0	5	ns	Multiplicand X (16-bit)
I_{00} to I_{31} Hold time 1	t_{HD1}	7	14	ns	Multiplicand X (16-bit)
I_{00} to I_{31} Set-up time 2	t_{SU2}	5	10	ns	Multiplier Y (32-bit)
I_{00} to I_{31} Hold time 2	t_{HD2}	0	11	ns	Multiplier Y (32-bit)
$\overline{MPY}$ Set-up time	t_{SU3}	15	26	ns	
$\overline{MPY}$ Hold time	t_{HD3}	0	5	ns	
XM Set-up time	t_{SU4}	15	25	ns	
XM Set-up time	t_{HD4}	0	6	ns	
MS_0, MS_1 Set-up time 1	t_{SU5}	4	9	ns	MST=H mode
MS_0, MS_1 Hold time 1	t_{HD5}	1	7	ns	MST=H mode
MS_0, MS_1 Set-up time 2	t_{SU6}	0	6	ns	MST=L mode
MS_0, MS_1 Hold time 2	t_{HD6}	6	12	ns	MST=L mode

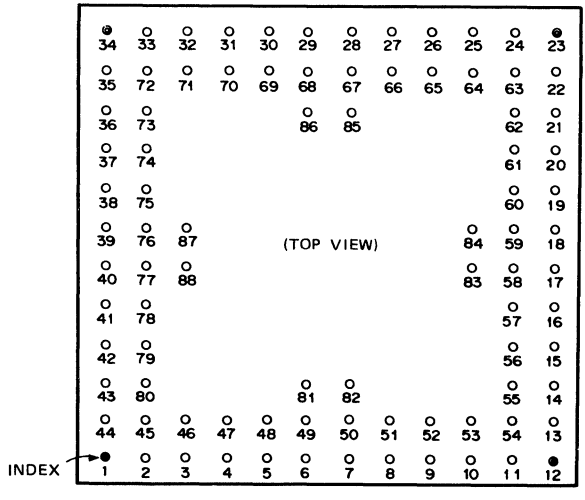


3. Input/output capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			9	pF

Test condition V_{DD}=V_I=0V, f_M=1 MHz

Pin Configuration



No.	Pin Name	I/O	No.	Pin Name	I/O	No.	Pin Name	I/O	No.	Pin Name	I/O
1	O_{22}	O	23	CPI	I	45	O_{27}	O	67	I_{21}	I
2	O_{28}	O	24	I_{07}	I	46	O_{30}	O	68	I_{20}	I
3	O_{29}	O	25	I_{08}	I	47	O_{31}	O	69	I_{19}	I
4	O_{32}	O	26	I_{09}	I	48	O_{34}	O	70	I_{18}	I
5	O_{33}	O	27	I_{10}	I	49	CPO	O	71	I_{17}	I
6	O_{35}	O	28	I_{11}	I	50	O_{21}	O	72	I_{16}	I
7	O_{20}	O	29	I_{12}	I	51	O_{18}	O	73	ARCO	O
8	O_{19}	O	30	I_{13}	I	52	O_{17}	O	74	O_{00}	O
9	O_{16}	O	31	I_{14}	I	53	O_{14}	O	75	O_{03}	O
10	O_{15}	O	32	I_{15}	I	54	O_{13}	O	76	O_{04}	O
11	O_{12}	O	33	PSEL	I	55	MST	I	77	O_{07}	O
12	O_{11}	O	34	$\overline{ACC}$	I	56	XM	I	78	O_{08}	O
13	$\overline{MPY}$	I	35	$\overline{CLR}$	I	57	I_{31}	I	79	O_{25}	O
14	MS_0	I	36	PSGN	O	58	I_{30}	I	80	O_{26}	O
15	MS_1	I	37	O_{01}	O	59	I_{29}	I	81	V_{SS}	—
16	I_{00}	I	38	O_{02}	O	60	I_{28}	I	82	V_{DD}	—
17	I_{01}	I	39	O_{05}	O	61	I_{27}	I	83	V_{DD}	—
18	I_{02}	I	40	O_{06}	O	62	I_{26}	I	84	V_{SS}	—
19	I_{03}	I	41	O_{09}	O	63	I_{25}	I	85	V_{SS}	—
20	I_{04}	I	42	O_{10}	O	64	I_{24}	I	86	V_{DD}	—
21	I_{05}	I	43	O_{24}	O	65	I_{23}	I	87	V_{DD}	—
22	I_{06}	I	44	O_{23}	O	66	I_{22}	I	88	V_{SS}	—

Description of Individual Blocks

The detailed structure of the internal circuits is described below, broken down into four blocks: Input block that includes input registers and shifters, multiply array block that performs actual multiplyig operations, accumulator block that performs accumulating operations, and output block that switches outputs in accordance with the designated output format.

1. Input block

This block separately latches multiplicand X and multiplier Y that have been input through pins I00 through I31 by time sharing, and after aligning their timings together, outputs X and Y to multiply array. The block is composed of registers and 1-bit shifters.

[Registers]

After being latched at the negative edge of CPI, multiplicand X is latched again at the positive edge thereof, while multiplier Y is latched directly at the positive edge. For all the registers and equivalent, type D FFs (flip-flops) have been employed, and to the second stage X latch registers and Y latch registers, enable pins have been provided to enable latching operations exclusively in "L" $\overline{MPY}$ modes. These enable pins have been built in by providing a selector on the D input side of each FF, as shown in Fig. 1.

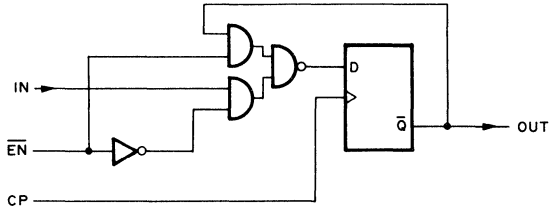


Fig. 1

[1-bit shifters]

A 1-bit shifter has been provided between the first and second stage latch units of · circuits, and serves for switching · values in accordance with whether the · is a 2'S complement or an unsigned straight binary. Specifically, because multiply array block in the next stage is capable only of 2'S comp. · 2'S comp. multiplying operations, it will add a 1-bit sign bit "0" onto the upper MSB when · is unsigned, to convert it into a 17-bit 2'S complement. When on the other hand, · is a 2'S complement, the shifter will add a 1-bit "0" to trail behind the LSB side to make it 17-bits in length. There operations are performed by the hardware shown in Fig. 2.

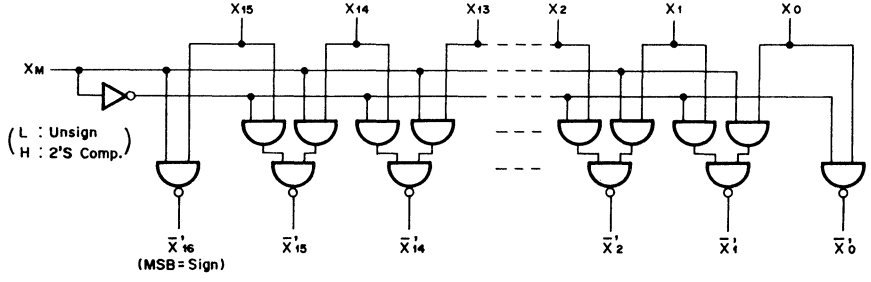


Fig. 2

2. Multiply block

This block actually multiplies multiplicand x and multiplier Y together that have been aligned together in the input block, and consists of three sections as shown in Fig.3; namely, partial product generator section, Wallace tree section, and CLA adder section.

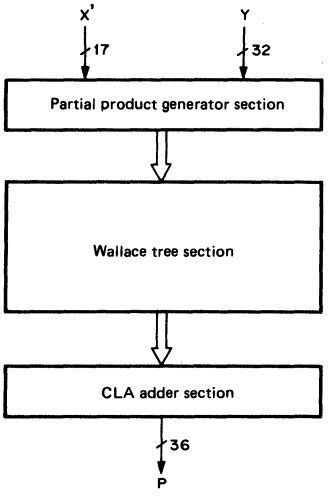


Fig. 3

3. Accumulator block

This block performs the so-called accumulating operation of adding earlier multiplied results (36 bits) and newly multiplied results (36 bits) together and providing the cumulative sum of such added results, and is basically constructed of 36-bit+36-bit adders and registers that hold earlier added results (Fig. 4).

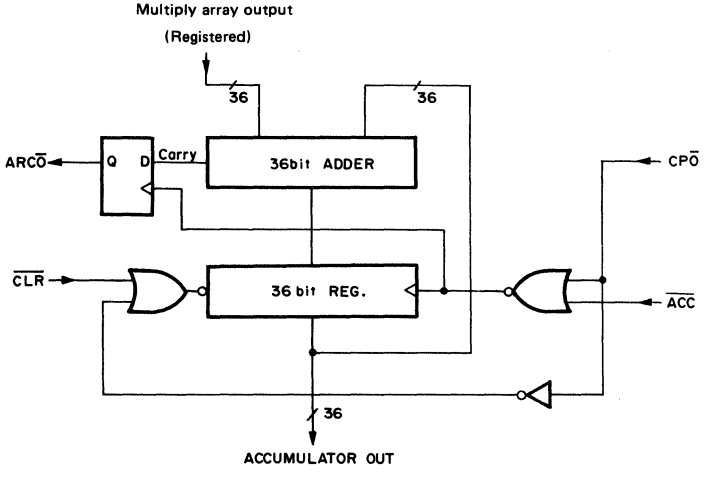


Fig. 4

4. Output block

This block switches its output in accordance with the mode selected by MS0 and MS1 and delivers O_{00} through O_{35} to the output pin. The block consists of a decoder and multiplexers. Its block diagram is shown in Fig. 5. It has two stages of multiplexers, one for mode switching and the other for switching between P_L and P_H.

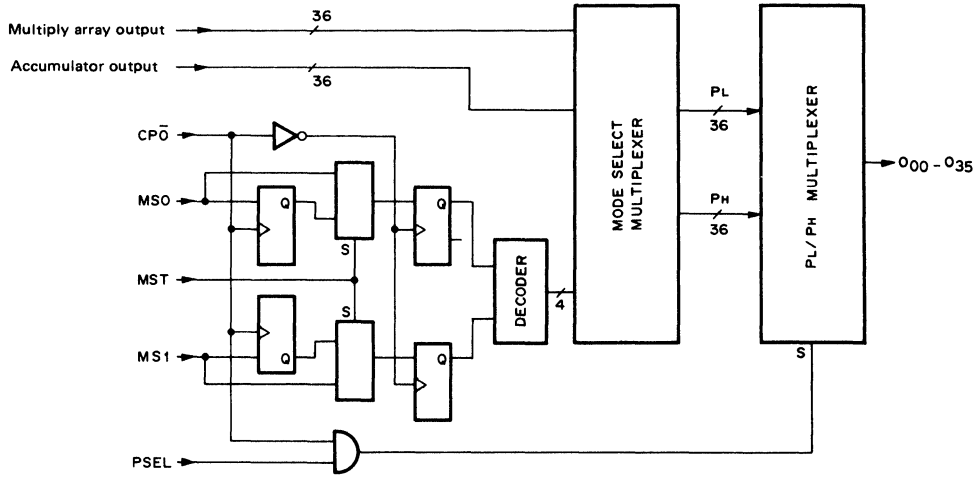


Fig. 5

Terminal Explanation

I_{00} through I_{31} (pins 16 through 22, 24 through 32, and 57 through 72)

These pins serve for inputting multiplicand X (16-bit) and multiplier Y (32-bit) by time sharing. Specifically, at the negative edge of a signal input to the CPI pin (pin 23), X is latched internally, as shown in Fig. 7, where 16-bit of X are input by the use of I_{08} serving as LSB through I_{23}, and 32-bit of Y input by the use of I_{00} serving as LSB through I_{31}, with the two inputs in 32-bit parallel with each other.

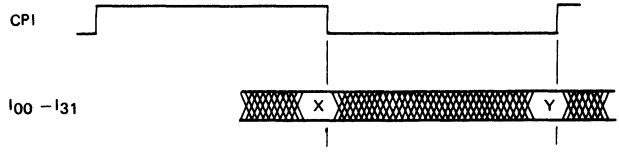


Fig. 6

I31	I30	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	
—	—	—	—	—	—	—	—	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	—	—	—	—	—	—	—	—	—X
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	—Y

Fig. 7

The data formats for multiplicand X and multiplier Y are shown below, where XM is the pin for switching the X expression between a 2'S complement and an unsigned straight binary and its further details will be given in the paragraph on "XM (pin 56)".

$$X=-1*X_{15}+\sum_{n=0}^{14}2^{-(15-n)}*X_n \qquad (XM="H")$$

$$X=\sum_{n=0}^{15}2^{-(16-n)}*X_n \qquad (XM = "L")$$

$$Y=-1*Y_{31}+\sum_{n=0}^{30}2^{-(31-n)}*Y_n$$

Multiplied P results will be given by:

$$P=-1*P_{35}+\sum_{n=0}^{34}2^{-(35-n)}*P_n$$

This LSI is capable of multiplying all X and Y combinations except just one (when X=−1, Y=−1) where multiplied results will overflow and become:

$X(-1)*Y(-1)=P(-1)$

calling for due caution.

$\overline{\text{MPY}}$ (pin 13)

This pin serves for inputting a multiplying operations starting command. When this pin is "L" and the positive edge of a signal input to the CPI pin (pin 23) has arrived, multiplying operations will commence. As multiplier Y for the operations, a signal input from I00 through I31 at the CPI positive edge is employed, and multiplicand X employs a signal input at the negative edge immediately preceding it. (Fig. 8)

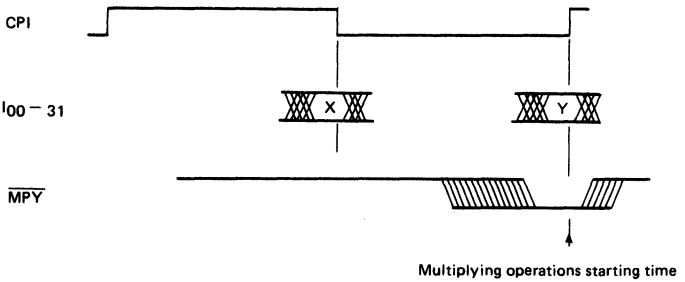


Fig. 8

XM (pin 56)

This pin serves for inputting the signal with which to switch the multiplicand X expression between a 2'S complement and an unsigned straight binary. X is made a 2'S complement at XM="H" or an unsigned straight binary at XM="L". The signal is latched internally at the CPI positive edge in an $\overline{\text{MPY}}$ (pin 13)="L" mode, and may be made to determine the expression for an X input at the immediately preceding negative edge.

CPI (pin 23) and CPO (pin 49)

These pins serve as the system clock input that determines operating cycles of the multiplier, and input a 50% duty square wave at 6 MHz max. CPI serves for latching multiplicand X and multiplier Y as well as the $\overline{MPY}$ and XM signals, while CPO serves for the MSO, MS1, and MST latching, the output multiplexer switching, and the determination of accumulator operating cycles (internal generation of $\overline{ACC}$ and $\overline{CLR}$ signals). Normally, the same signal is input to CPI and CPO, but the two inputs may be mutually phase-shifted depending on the external circuitry for control of the LSI.

* For example, when X, Y, control signals $\overline{MPY}$, XM, etc., and the timing for fetching the multiplied results P that have been output by this LSI all synchronize with CPO, CPI may be made to lead CPO as shown in Fig. 9. Such an arrangement offers the advantage of a shorter cycle time (CPI/CPO cycle).

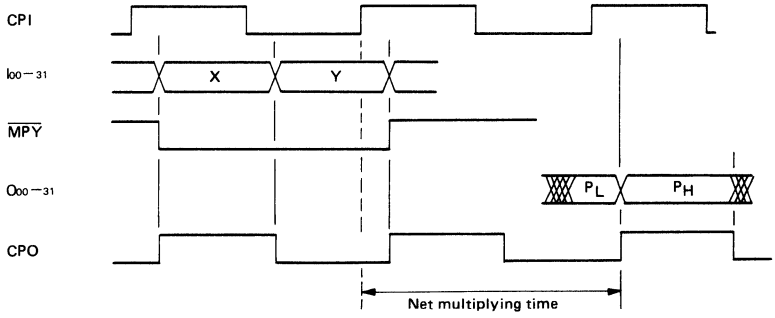


Fig. 9

MSO (pin 14), MS1 (pin 15), and MST (pin 55)

These pins serve as mode switching inputs that determine bit assignments for the output of multiplied results P to O00 through O35 (pins 1 through 12, 37 through 48, 50 through 54, and 74 through 80), and the modes switched include those shown in Fig. 10. Bit assignments and similar other aspects will be discussed in greater detail in the paragraph on "O00 through O35".

Mode	MS1	MSO	Function
0	0	0	CX23015: Standard (28-bit) or extended (36-bit with two CX23015 employed)
1	0	1	CX23015-extended 12-bit right shift mode
2	1	0	General purpose 16×32→36-bit with no ACC
3	1	1	General purpose 16×32→36-bit with ACC output

Fig. 10

In the above, MST (pin 55) is the input pin that dictates the timing for internally latching MSO and MS1. At MST="L", MSO and MS1 are latched at the negative edge of a signal input to the CPO pin (pin 49), and immediately afterward, the O00 through O35 signals will continue to be output in that mode until the next negative edge arrives. At MST="H", MSO and MS1 are latched at the positive edge of CPO, and the mode for O00 through O35 are maintained unaltered for the interval starting with a negative edge that immediately follows the said positive edge and ending with the next negative edge (Fig. 11).

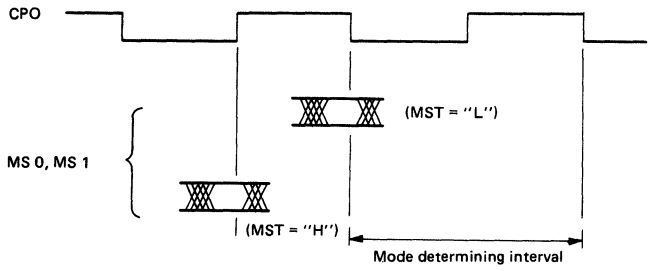


Fig. 11

O_{00} through O_{35} (pins 1 through 12, 37 through 48, 50 through 54, and 74 through 80), and PSEL (pin 33)

Pins O_{00} through O_{35} output either multiplied results P or the accumulator data, and when PSEL (pin 33) is made "L", the output will emerge at O_{00} through O_{35} that has been time-multiplexed by CPO to permit its direct connection to an ADSP. Specifically, when CPO is "L" the LSB side of P, or P_L, is output, and when it is "H", the MSB side of P, or P_H, is output. When no time-multiplexing is required for general purpose applications, PSEL may be set at "H" to fix the output at P_H. These output timings are shown in Fig. 12. In addition, the detailed output format at individual pins is shown in Fig. 13.

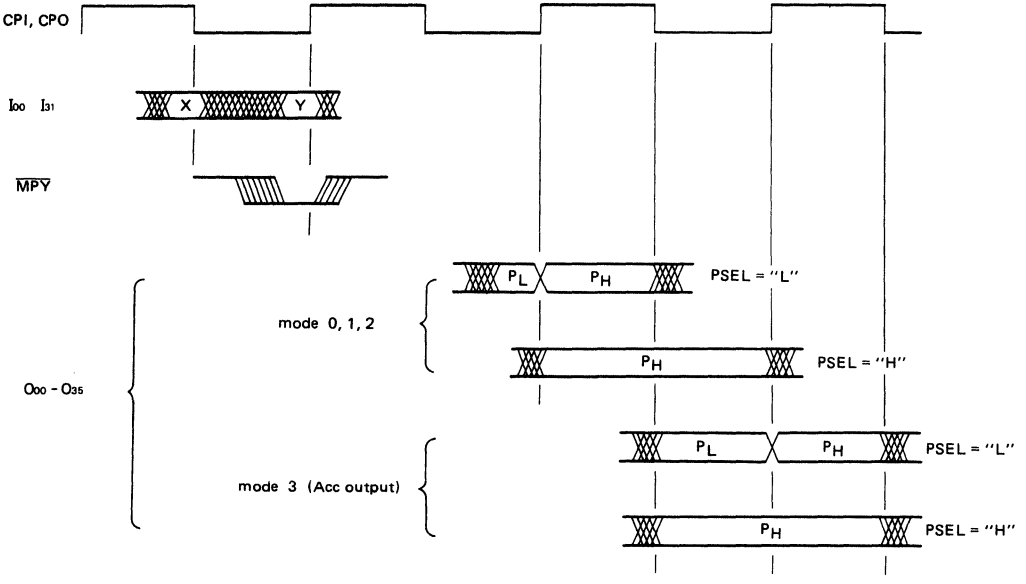


Fig. 12

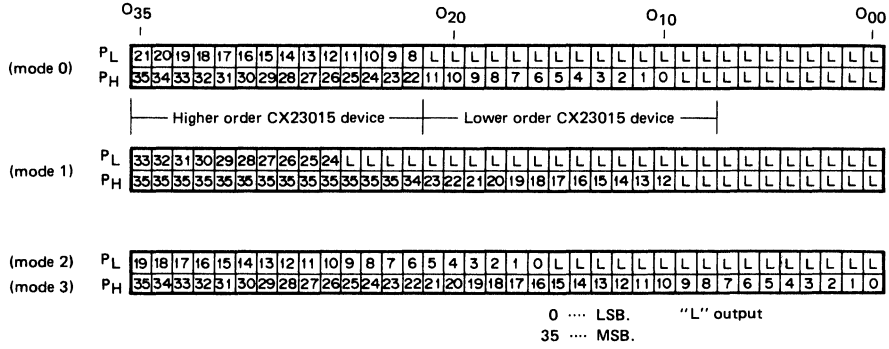


Fig. 13

$\overline{ACC}$ (pin 34) and $\overline{CLR}$ (pin 35)

$\overline{ACC}$ is the input pin through which adding commands are issued to the accumulator within, and when $\overline{ACC}$ is "L", the internal accumulator register contents and the immediately preceding multiplied results that have been summed together are freshly latched by the accumulator register as soon as CPO is made "L". $\overline{CLR}$ is the input pin that reduces the accumulator register contents all to "0", and similarly to $\overline{ACC}$, "0" is loaded to the accumulator register as soon as $\overline{CLR}$ and CPO have together been made "L".

Note that the internal accumulation and accumulator register clear operations are not executed by the negative edge of CPO at $\overline{ACC}$ (or $\overline{CLR}$)="L", but at the simultaneous "L" levels of CPO and $\overline{ACC}$ (or $\overline{CLR}$), so that in a case illustrated in Fig. 14, internal operations will be performed not only at timing "a" but at timing "b" as well. With $\overline{ACC}$, in particular, since a spurious addition unrelated to the CPO cycle is made at timing "b", utmost caution should be exercised.

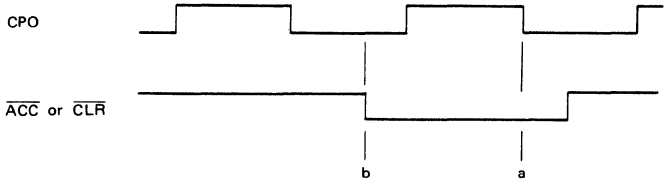


Fig. 14

Fig. 15 shows normal $\overline{CLR}$ and $\overline{ACC}$ operational timings.

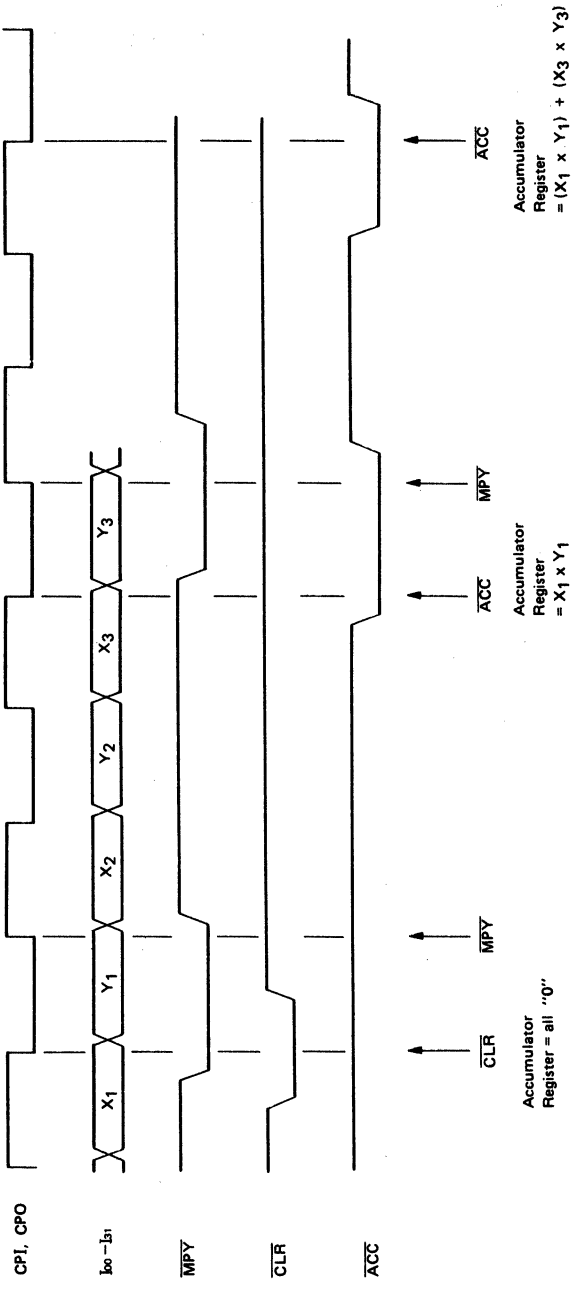

CPI, CPO
I00 - I31
MPY
CLR
ACC
X1
Y1
X2
Y2
X3
Y3
CLR
MPY
ACC
MPY
ACC
Accumulator Register = all "0"
Accumulator Register = X1 x Y1
Accumulator Register = (X1 x Y1) + (X3 x Y3)

Fig. 15

PSGN (pin 36) and ARCO (pin 73)

PSGN and ARCO are the exit pins for the extension of accumulator beyond 36-bit, and an example 40-bit accumulator that has been constructed by the use of these pins is shown in Fig. 16, together with its timing chart in Fig. 17.

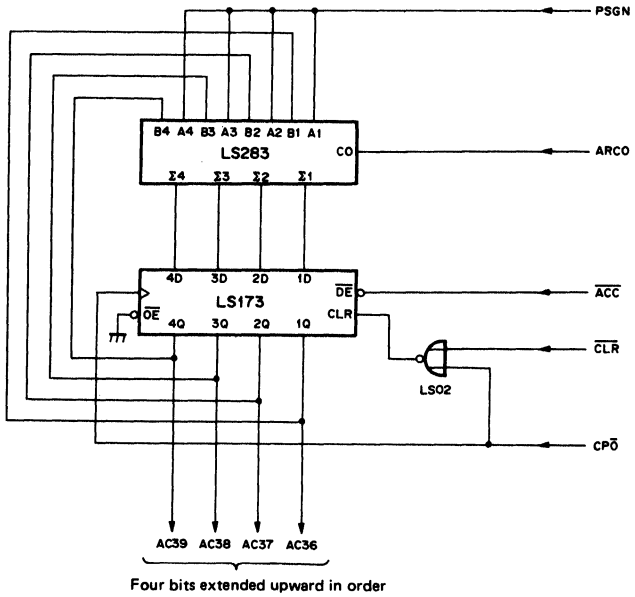


Fig. 16

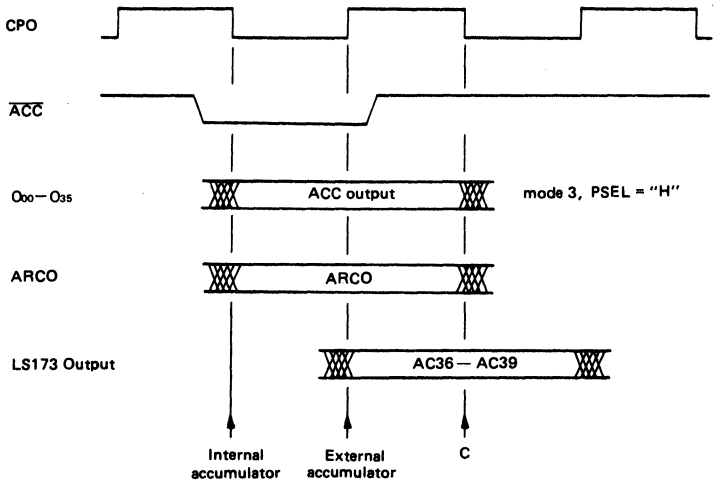
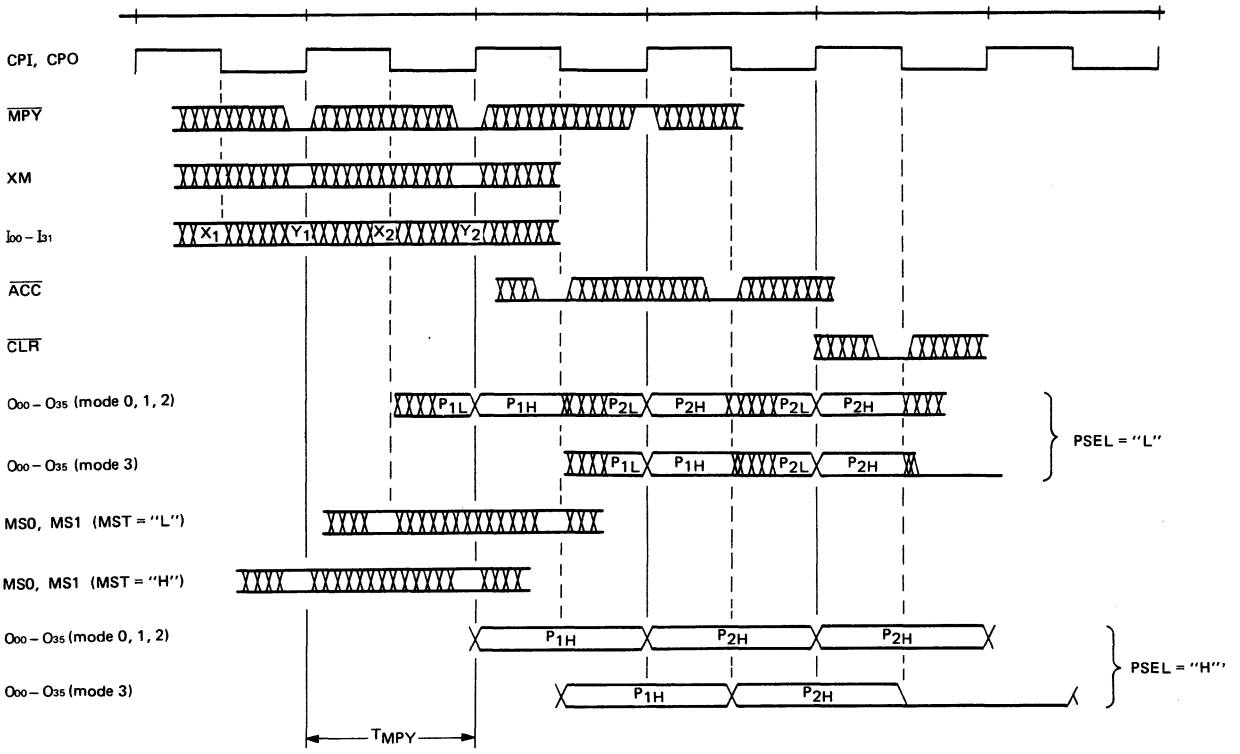


Fig. 17

Note that accumulations in the external circuit are made at the positive edge of CPO so that, as shown in Fig. 17, the $\overline{ACC}$ signal will have to be held at an 'L" level at the positive edge of CPO as well. Because the externally accumulated results are made valid after the positive edge, 40-bit accumulations that have been extended upward beyond MSB by 4-bit may be achieved by latching O00 through O35 and the four outputs of LS173 at timing "C" of Fig. 17, and thereby expanding the overflow limit of the 36-bit accumulator.



Overall Timing Chart

Supplementary Presentations

[Supplement 1] Booth algorithms

Booth algorithms represent a technique for the multiplication of binary numbers expressed in 2'S complements, and will not only reduce the number of partial products involved but also eliminate the need for corrections that accompany the 2'S complement expression.

When multiplying binary numbers in general, partial products equal in quantity to the bits in Y and marked in Fig. 18 with double underlines are generated. By deriving partial products for every two bits of multiplier as shown in Fig. 19, their quantity may be reduced in half. When simply employed, however this approach will generate partial products that take on one of four values of 0, X, 2X, and 3X. Of these, 0, X, and 2X may readily be obtained as X itself or in its shifted form, but 3X presents quite a challenge for hardware to generate.

Now, a (n+1)−bit multiplier, Y, expressed in 2'S comple-ments, may be written as:

$$Y=-Y_n 2^n+\sum_{k=0}^{n-1} Y_k 2^k \qquad (1)$$

By assuming for simplicity's sake, the length of Y (n:1) to be an even number, and $Y_{-1}=0$ to hold true, the above equation may be rewritten as follows:

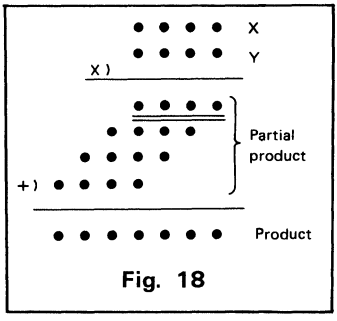


Fig. 18

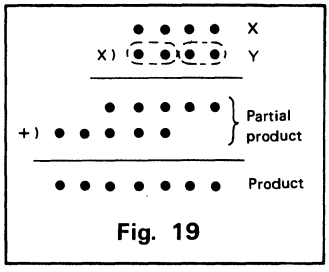


Fig. 19

$$\begin{aligned}Y&=-Y_n\cdot 2^n+Y_{n-1}\cdot 2^{n-1}+Y_{n-2}\cdot 2^{n-2}\\&\quad+\ldots+Y_3\cdot 2^3+Y_2\cdot 2^2+Y_1\cdot 2^1+Y_0\cdot 2^0\\&=(Y_{n-2}+Y_{n-1}-2Y_n)\,2^{n-1}+(Y_{n-4}+Y_{n-3}-2Y_{n-2})\cdot 2^{n-3}\\&\quad+\ldots+(Y_1+Y_2-2Y_3)\cdot 2^2+(Y_{-1}+Y_0-2Y_1)\cdot 2^0\\&=\sum_{k=0}^{n-1/2}(Y_{2k-1}+Y_{2k}-2Y_{2k+1})\cdot 2^{2k} \qquad (2)\end{aligned}$$

Accordingly, multiplied result $P=X\cdot Y$ may be written as:

$$\begin{aligned}P&=X\cdot Y\\&=\sum_{k=0}^{n-1/2}(Y_{2k-1}+Y_{2k}-2Y_{2k+1})X\cdot 2^{2k} \qquad (3)\end{aligned}$$

where $(Y_{2k-1}+Y_{2k}-2Y_{2k+1})X\cdot 2^{2k}$ represents the partial products under discussion. From equation (3), their quantity will be (n+1)/2 or half the number of bits in Y.

Since $(Y_{2k-1}+Y_{2k}-2Y_{2k+1})$ takes on the values at 0, ±1, and ±2 against three sucessive bits (Y_{2k-1}, Y_{2k}, Y_{2k+1}), partial products $(Y_{2k-1},+Y_{2k}-2Y_{2k+1})X$ will take on one of five values of 0, ±X, and ±2X. Of these, 2X may be generated by a single bit shift, and for negative number −X, obtaining $\overline{X}$ and adding 1 to LSB will suffice due to its 2'S complement expression.

Accordingly, by designating the operational format out of 0, ±X, and +2X from three successive bits, the generation will be enabled with relatively simple hardware of the partial products whose quantity equals half the bits in Y, or half the quantity involved in normal calculations.

Given in Table 1 below is a list of types of operations against three suceessive bits if Y, and Fig. 20 shows how to fetch three successive bits out of Y that is 8 bits in length.

Y_{2k+1}	Y_{2k}	Y_{2k-1}	Operation
0	0	0	0
0	0	1	+X
0	1	0	+X
0	1	1	+2X
1	0	0	−2X
1	0	1	−X
1	1	0	−X
1	1	1	0

Table 1

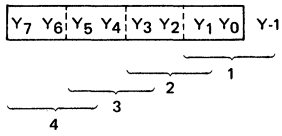


Fig. 20

Since as is evident in Fig. 20, the three bits (Y_{2k-1}, Y_{2k}, Y_{2k+1}) each have one bit overlapping with their neighbors, they appear as if Y has been segmented at every other bit. This is the reason why this process is known as the second order Booth algorithms.

[Supplement 2] +1 algorithm

When in multiplying binary numbers expressed in 2'S complements, partial products are obtained by Booth algorithms, each individual partial product is also expressed in 2'S complements so that the MSB of the lower order partial products will have to be sign-extended as shown in Fig. 21 to yield a valid product. Such sign extensions, however, will increase the number of bits in partial products, levying a large burden on the partial products adding hardware and lowering its multiplying speed. Accordingly, the partial product MSB (= sign bit) is inverted and "1" added on at the prescribed locations, to enable the addition with no sign extensions that in turn brings about higher speed operations. This process is known as the +1 algorithm.

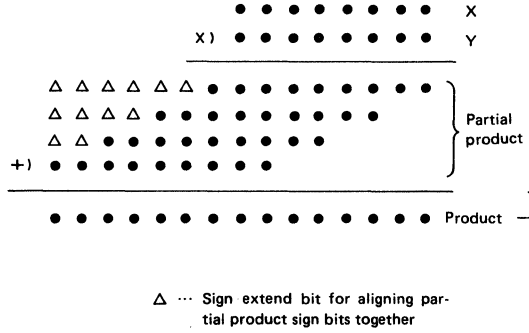


Fig. 21

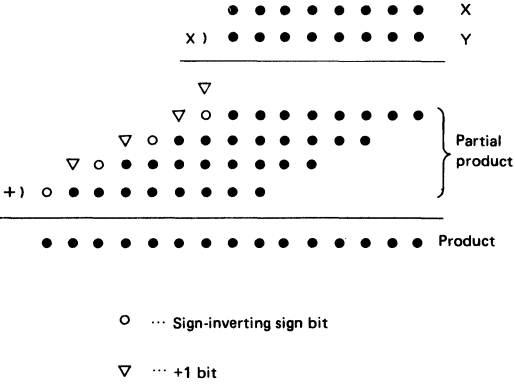


Fig. 22

SONY

CXK1201P

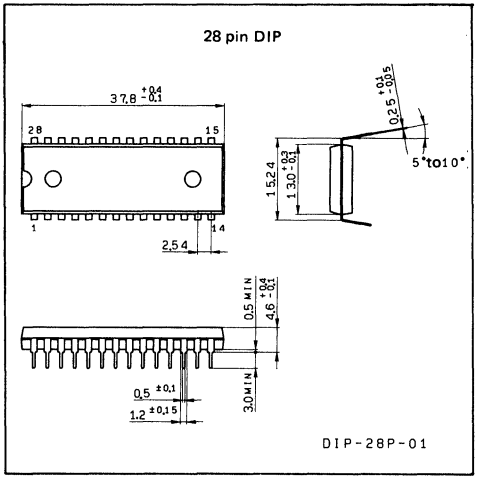
Double Scan Converter

Preliminary

Description

The CXK1201P is a digital line memory for non-interlace TV 8-bit structure which employs silicon gate CMOS process. It is enabled to perform line interpolation and scan conversion of horizontal frequency.

Package Outline Unit: mm



Features

- Most suitable to the digital TV system of its sampling frequency of 4 fsc (NTSC).
- Incorporates H sync, H blanking, clock for A/D converter and clear signal generation circuit to synchronize with external circuit.
- Memory structure 910×8×2 bit
- High speed cycle time
  Minimum write cycle time 66 ns
  Minimum read cycle time 33 ns
- I/O level Compatible with TTL level
- Data output three states
- 5V single power supply
- Low power consumption 200 mW (typ.)

Structure

Silicon gate CMOS

Application

Double scan monitior

Function

Double scan conversion

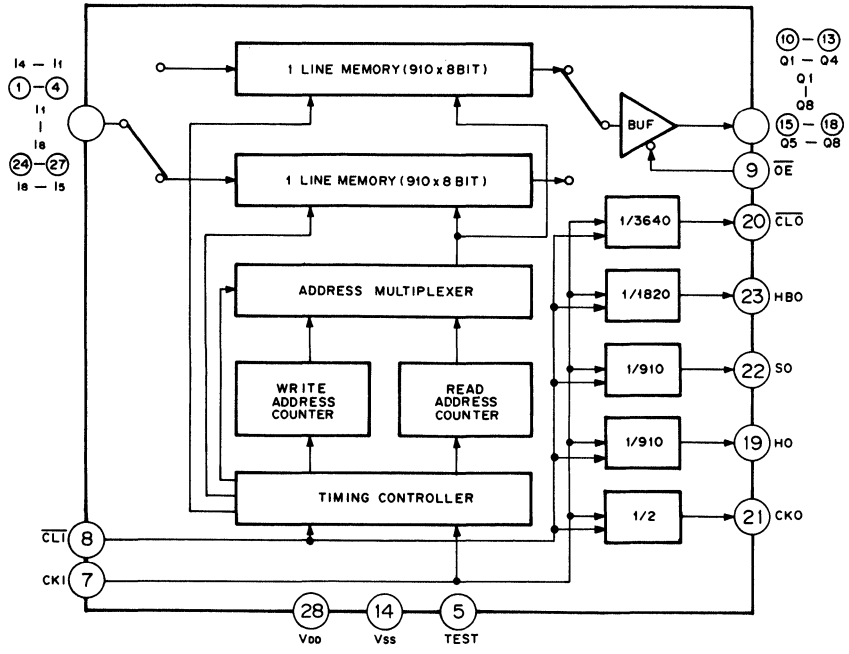
Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to +7.0	V
• Operating temperature	Topr	−10 to +85	°C
• Storage temperature	Tstg	−55 to 150	°C
• Power consumption	P_D	500	mW

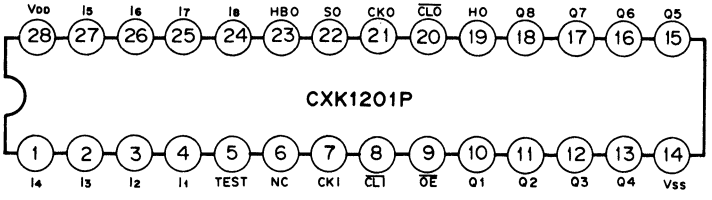
Recommended Operating Conditions (Ta=0 to +70°C)

• Supply voltage	V_{DD}	4.5 to 5.5	V (5.0V Typ.)
• Supply voltage	V_{SS}	0	V
• Input voltage "H" level	V_{IH}	2.4 to V_{DD}+0.3	V
• Input voltage "L" level	V_{IL}	−0.3 to +0.8	V

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	Description
1 – 4	$I_4 - I_1$	Data input
5	TEST	Test signal input
6	NC	Non-connection
7	CKI	Clock input
8	$\overline{CLI}$	Clear input
9	$\overline{OE}$	Output enable input
10 – 13	$Q_1 - Q_4$	Data output
14	V_{SS}	Ground
15 – 18	$Q_5 - Q_8$	Data output
19	HO	2H output (The same frequency as H sync, duty 50%)
20	$\overline{CLO}$	Clear output
21	CKO	Clock output (Frequency is 1/2 of CKI)
22	SO	H sync output
23	HBO	H blanking output
24 – 27	$I_8 - I_5$	Data input
28	V_{DD}	Power supply (+5V)

Pin Function

(1) I1 to I8 (Input)
The data inputs. The data set up time and hold time are determined from the rising edge of the clock.

(2) Q1 to Q8 (Output)
The data outputs. The access time is determined from the rising edge of the clock.

(3) CKI (Input)
A lock input. The I/O timing of the respective signals are defined against the clock which has been input from this pin.

(4) $\overline{CLI}$ (Input)
A clear input. The input which is used in order to initialize the write address and read address. When it is necessary to synchronize with the externals (data inputs), there are two ways, the one is to use this clear input and the other is to use the H blanking signal which will be described later in this description.

(5) $\overline{OE}$ (Input)
An output enable. When it is at "L" level, the data outputs ($Q_1 - Q_8$) become into output mode. When at "H" level, they become into high impedance state.

(6) $\overline{CLO}$ (Output)
A clear output. When plural numbers of this LSI are used in parallel, it is possible to synchronize with the respective LSIs by inputting the clear output of which is specified as the reference, to the clear inputs of other LSIs.

(7) CKO (Output)
A clock output pin. The frequency is 1/2 that of the input colck signal and is possible to be used as clock of the A/D converter.

(8) SO (Output)
An H SYNC signal output pin. It is possible to be used as a signal to synchronize the data output and monitor. However, this signal is an H SYNC signal during double speed (The frequency is twice as much as that of normal.)

(9) HO (Output)
A signal output pin which outputs the signal of 50% duty and whose frequency is equivalent to the H SYNC signal.

(10) HBO (Output)
A H blanking signal output pin. It is possible to be used as a synchronizing signal with the data input signal.

(11) TEST (Input)
A test signal input pin. It is a pin used during the test of LSI and is normally used at "H" level.

(12) V_{DD}
The power supply pin. (+5V)

(13) V_{SS}
The grounding pin.

Electrical Characteristics

DC characteristics

V_{DD}=5.0V, Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply current (active)	I_{DD}			70	mA	
Input leakage current	I_{IL}	−2		2	μA	V_{IN}=0V − V_{DD}
Output leakage current	I_{OL}	−2		2	μA	V_{OUT}=0V − V_{DD}
Output voltage "H" level	V_{OH}	2.7			V	I_{OH}=−400μA
Output voltage "L" level	V_{OL}			0.4	V	I_{OL}=4.0mA

AC characteristics

V_{DD}=4.5V to 5.5V, Ta=0°C to 70°C
(See the timing chart on next page)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Data set up time	tdsu	0			ns	
Data hold time	tdh	25			ns	
$\overline{CLI}$ set up time	tcsu	10			ns	
$\overline{CLI}$ hold time	tch	5			ns	
Clock pulsewidth	tckw	15			ns	Low or high

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	f			30	MHz	C_L=30pF
From clock input to determination of Q_1 – Q_8	tpda	7		25	ns	
From $\overline{OE}$ input to determination of Q_1 – Q_8	tpdb	7		25	ns	
From clock input to determination of CKO	tpdc	7		25	ns	
From clock input to determination of $\overline{CLO}$	tpdd	7		25	ns	
From clock input to determination of SO	tpde	7		25	ns	
From clock input to determination of HBO	tpdf	7		25	ns	
From clock input to determination of HO	tpdg	7		25	ns	
Output disable time (from $\overline{OE}$)	tpdh	7		25	ns	
Output enable time (from $\overline{OE}$)	tpdi	7		25	ns	

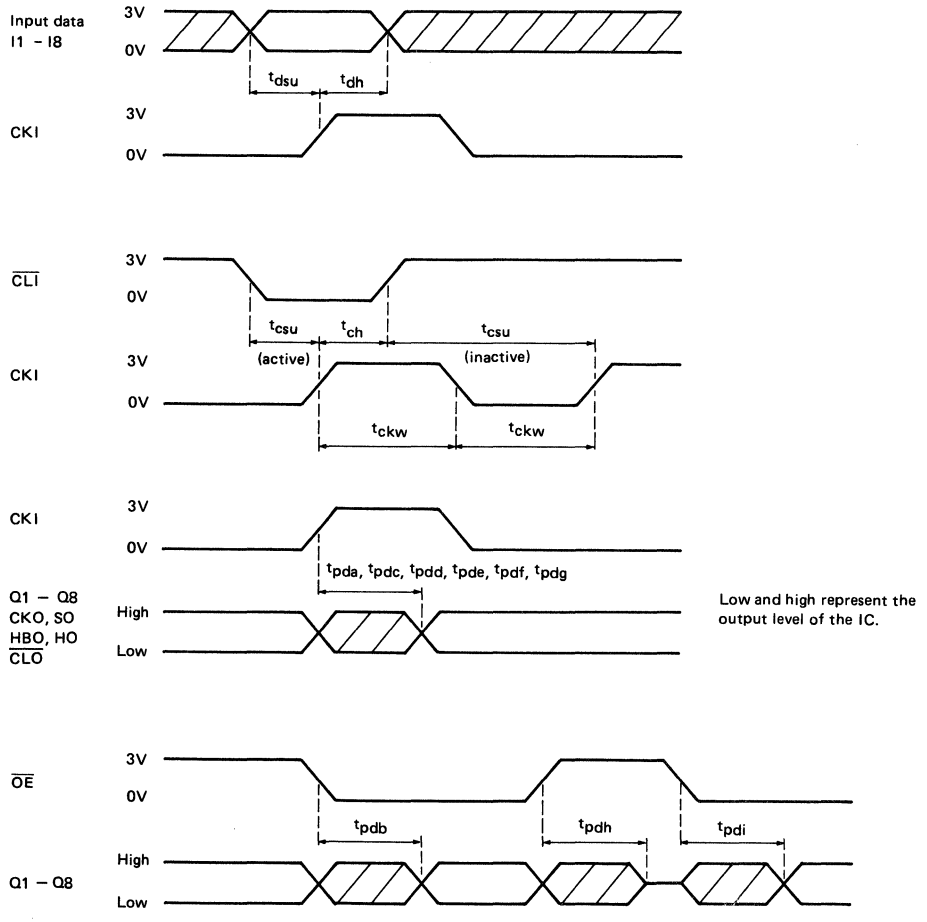
Pin capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Input capacitance	C_{IN}			7	pF	Ta=25°C, f=1MHz
Output capacitance	C_{OUT}			10	pF	V_{IN}=V_{OUT}=0V

Timing chart

(1) Input signal levels are at the low level = 0V and at the high level = 3V, and 5 ns for both rising and falling time.

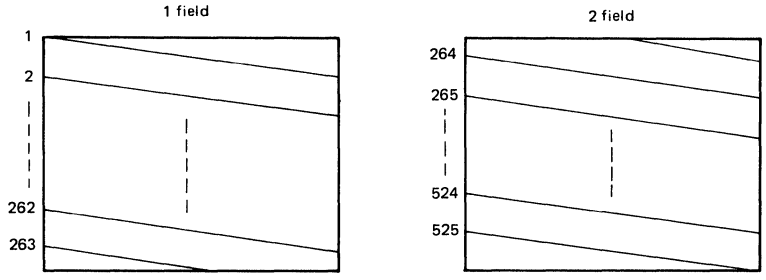
(2) The voltage judging levels of both low and high are 1.5V.



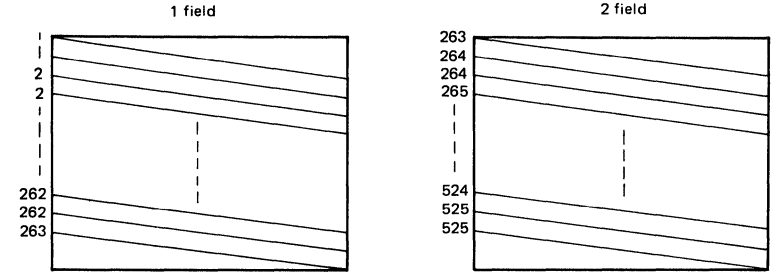
Description of Operation

The video signal of the NTSC format performs interlacing with one field 525/2 scanning lines. Accordingly, to perform scan conversion of horizontal frequency (one field 525 scanning lines), it is required to make line interpolation and the horizontal scanning frequency twice as much. The conceptual diagrams when performing the scan conversion by using a CXK1201P are as shown below.

NTSC format video signal

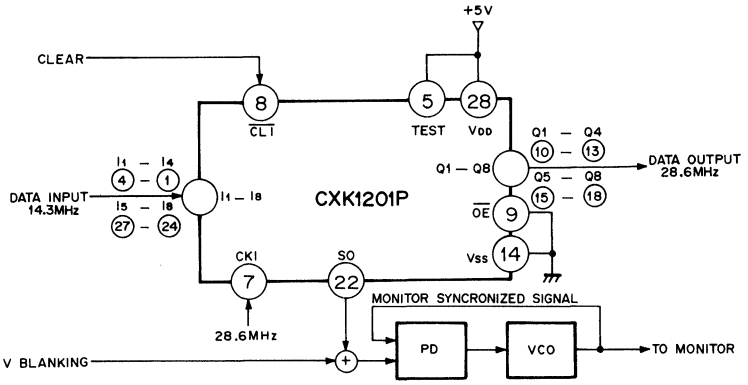


Video signal after being converted into scan conversion



An application example, which is provided as a reference in order to operate the converter in the manner as shown in the conceptual diagrams, is as shown in Fig. 1, and its timing chart is as shown in Fig. 2. At first, initialize the write address and read address of the CXK1201P by inputting clear signal. After that, by inputting the digital data having been sampled by $4f_{SC}$ (14.3 MHz), the data having been converted by double speed can be obtained in synchronization with the clock at $8f_{SC}$ (28.6 MHz).

Moreover, to synchronize with the monitor, carry out the phase comparison with the composite sync signal which is provided by adding the H sync signal generated from the CXP1201P and the V blanking signal extracted from the input data and the composite sync signal within the monitor, and by changing the frequency and phase of the composite sync signal within the monitor so as to make no differences in the phases.



PD : Phase Detector
VCO : Voltage Controlled Oscillator

Fig. 1 Application circuit, No. 1

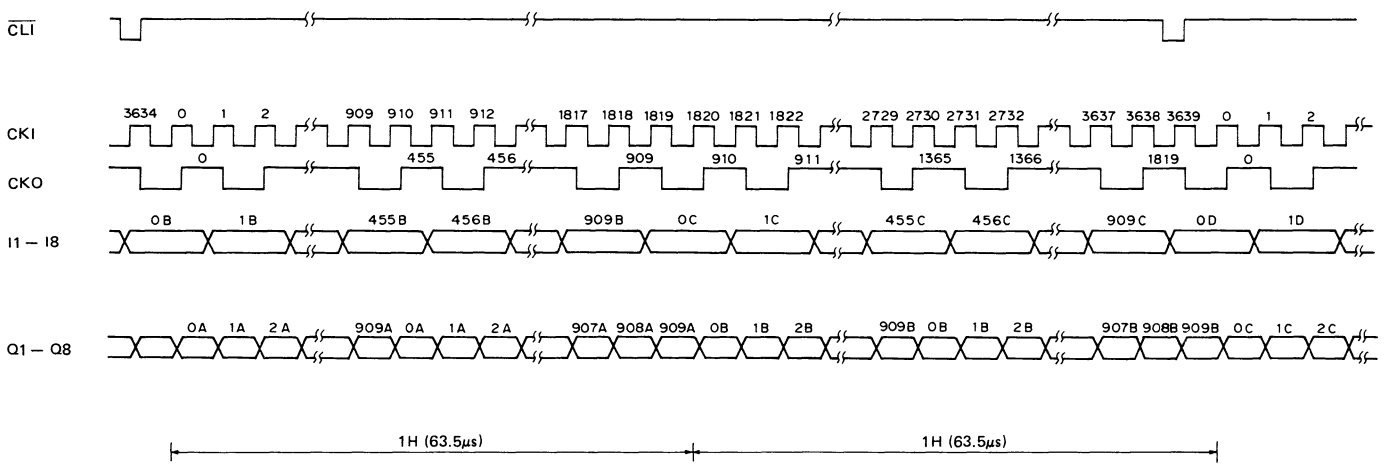


Fig. 2 Double speed conversion timing chart

Moreover, an application example when the clear input is not used is as shown in Fig. 3. In this case, extract the H sync signal from the input video signal and make the sync signal having the same frequency as the input H sync by the H blanking signal and HO signal from the CXP1201P. Perform the phase comparison of thus provided sync signal and change the frequency and phase of the clock (28.6 MHz) so as to make no difference in the phase.
In addition, the method to synchronize it with the composite signal of the monitor, the same procedures as using the clear input mentioned above should be taken.

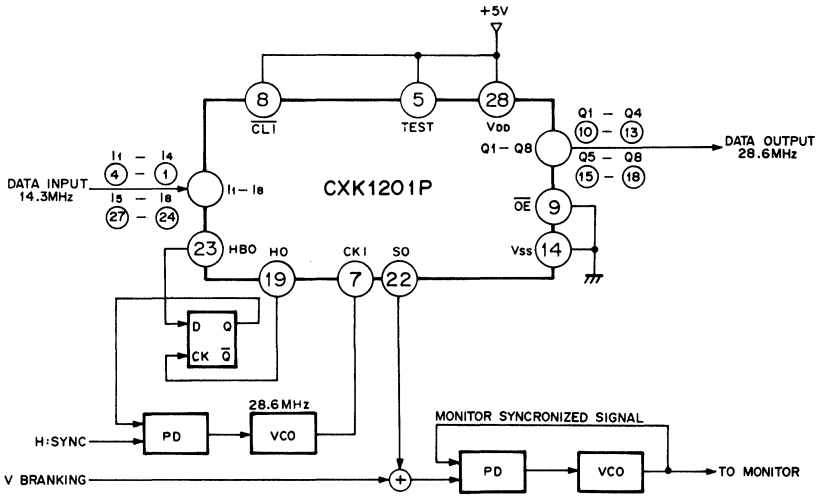


Fig. 3 Application circuit, No. 2

The CXK1201P generates various kinds of synchronizing signals in order to synchronize with the external signals. The phase relationship between the synchronizing signals and their respective timings are shown in Figs. 4 and 5 respectively.

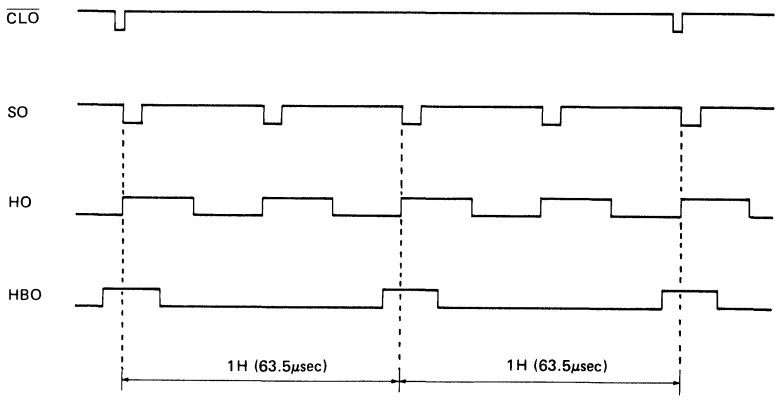


Fig. 4 The phase relationship between the respective outputs

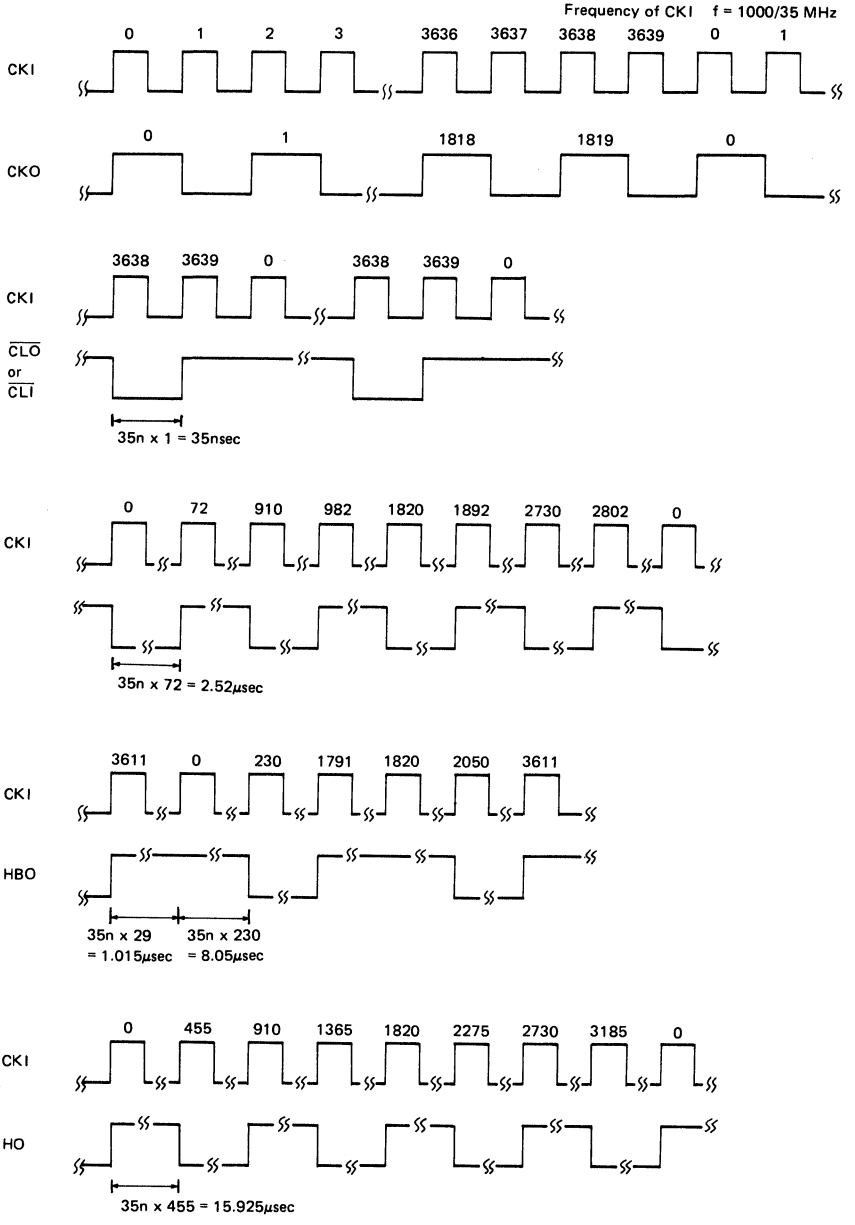


Fig. 5 The respective output timings against the input CKI

Digital Delay Line

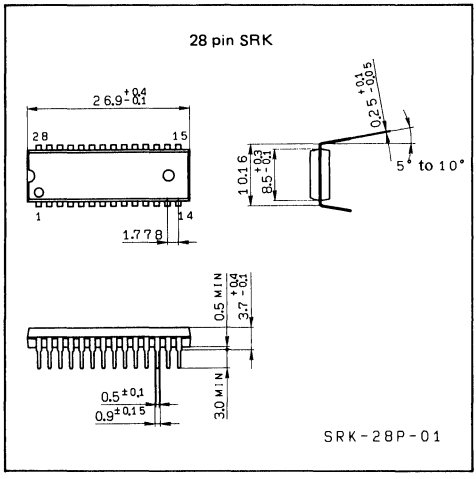
Description

The CXK1202S is a digital line memory pertaining to 8-bit structure which employs silicon gate CMOS process. It can easily be used to realize compensation for dropout of VTR and used as a digital filter, noise reduction, etc.

Features

- 1144 words × 8 bit structure
- Number of delay steps is 17 to 1144 bits and variable.
- Possible to select the following 16 delay lines (Peripheral circuit is unnecessary) for NTSC, PAL and SECAM
  - 905 to 912 bits
  - 1129 to 1136 bits
- High speed cycle time
  - Minimum write cycle time 25ns
  - Minimum read cycle time 25ns
- I/O level Compatible with TTL level
- Data output three-states
- 5V single power supply operation
- Low power dissipation (200 mW typ.)

Package Outline Unit: mm



Structure

Silicon gate CMOS

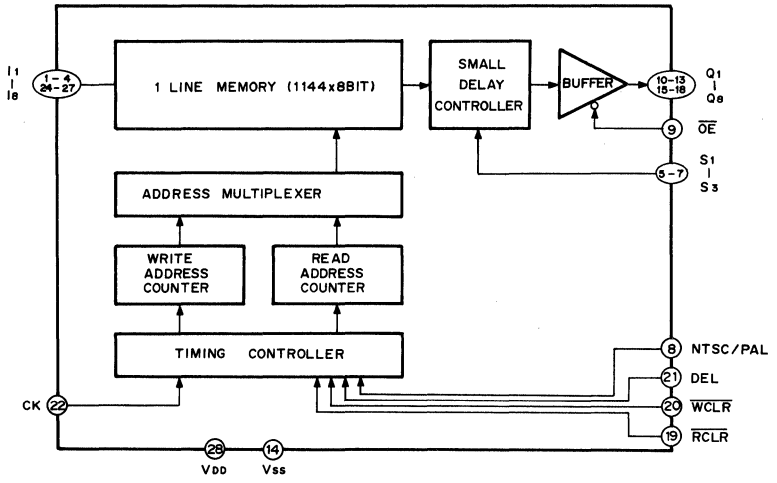
Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.5 to +7.0	V
• Input voltage	V_{IN}	−0.3 to +7.0	V
• Operating temperature	Topr	−10 to +85	°C
• Storage temperature	Tstg	−55 to 150	°C
• Power consumption	P_D	500	mW

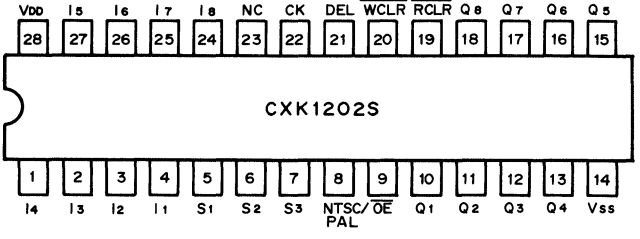
Recommended Operating Conditions (Ta=0°C to 70°C)

• Supply voltage	V_{DD}	4.5 to 5.5	V (5.0V typ.)
• Supply voltage	V_{SS}	0	V
• Input voltage "H" level	V_{IH}	2.4 to V_{DD}+0.3	V
• Input voltage "L" level	V_{IL}	−0.3 to +0.8	V

Block Diagram



Pin Configuration (Top view)



Pin Description

No.	Symbol	Description
1 – 4	I_4 – I_1	Data input pins. Data set up time and hold time are determined from the rising edge of the clock.
5 – 7	S_1 – S_3	These are small delay steps setting input pins. The setting number of the delay steps is determined by the cycle of the clear signal and the level of S_1 to S_3. At this point, the clear signal sets rough number of delay steps of every multiple of 8 bits. However, pins S_1 to S_3 set delay step of 1 bit-unit with 8-bit width.
8	NTSC/PAL	An input pin which selects the number of delay steps either 905 to 912 bits or 1129 to 1136 bits when the DEL pin is set at "H" level. The 905 to 912 bits of delay steps are selected when it is at "H" level and 1129 to 1136 bits of delay steps are selected when it is at "L" level.
9	$\overline{OE}$	An output enable input pin. The data output pins (Q_1 to Q_8) become into output mode when they are at "L" level. They become into high impedance state when they are at "H" level.
10 – 13	Q_1 – Q_4	These are data output pins. The outputs against the respective inputs of I_1 to I_4 correspond to Q_1 to Q_4. The access time is determined from the rising edge of the clock.
14	V_{SS}	A grounding pin.
15 – 18	Q_5 – Q_8	Data output pins. The outputs against the respective inputs of I_5 to I_8 correspond to Q_5 to Q_8. The access time is determined from the rising edge of the clock.
19	$\overline{RCLR}$	A clear signal input pin of the read address counter. It becomes into input mode when the DEL pin is at "L" level. The signal is input into IC at the rising edge of the CK. The signal input from the $\overline{RCLR}$ pin is ignored when the DEL pin is at "H".
20	$\overline{WCLR}$	A clear signal input pin of the write address counter. It becomes into input mode when the DEL pin is at "L" level. The signal is input into IC at the rising edge of the CK. The signal input from the $\overline{WCLR}$ pin is ignored when the DEL pin is at "H".
21	DEL	An input pin which selects the external and internal clear signals. When at "L", it becomes into external clear signal input mode and the number of delay steps can be set at any bit from 17 to 1144 bits. When at "H", it becomes into internal clear signal using mode and the number of delay steps can be set at any bit from 905 to 912 bits and from 1129 to 1136 bits.
22	CK	A clock input pin. The I/O timing of the respective signals and the delay step, etc. can be defined against the clock input from this pin.
23	NC	Non-connection
24 – 27	I_8 – I_5	Data input pins. The data set up time and hold time are determined from the rising edge of the clock.
28	V_{DD}	The power supply pin (+5V).

Electrical Characteristics

(1) DC characteristics

V_{DD}=5.0V, Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply current (Active)	I_{DD}	—	—	70	mA	
Input leakage current	I_{IL}	−2	—	2	μA	V_{IN}=0V V_{DD}
Output leakage current	I_{OL}	−2	—	2	μA	V_{OUT}=0V V_{DD}
Output voltage "H" level	V_{OH}	2.7	—		V	I_{OH}=−400μA
Output voltage "L" level	V_{OL}	—	—	0.4	V	I_{OL}=4.0mA

(2) AC characteristics

V_{DD}=4.5V to 5.5V, Ta=0°C to 70°C
(Regarding the timing chart, see next page.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Data set up time	t_{dsu}	5	—	—	ns	
Data hold up time	t_{dh}	5	—	—	ns	
$\overline{WCLR}$, $\overline{RCLR}$ set up time	t_{csu}	15	—	—	ns	
$\overline{WCLR}$, $\overline{RCLR}$ hold time	t_{ch}	5	—	—	ns	
Clock pulse width	t_{ckw}	10	—	—	ns	Low or high

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	f	—	—	40	MHz	C_L=30pF
From clock input to output data determination	t_{pda}	—	—	25	ns	
From $\overline{OE}$ input to output data determination	t_{pdb}	—	—	25	ns	
Output disable time (from $\overline{OE}$)	t_{pdh}	—	—	25	ns	
Output enable time (from $\overline{OE}$)	t_{pdi}	—	—	25	ns	

(3) Pin capacity

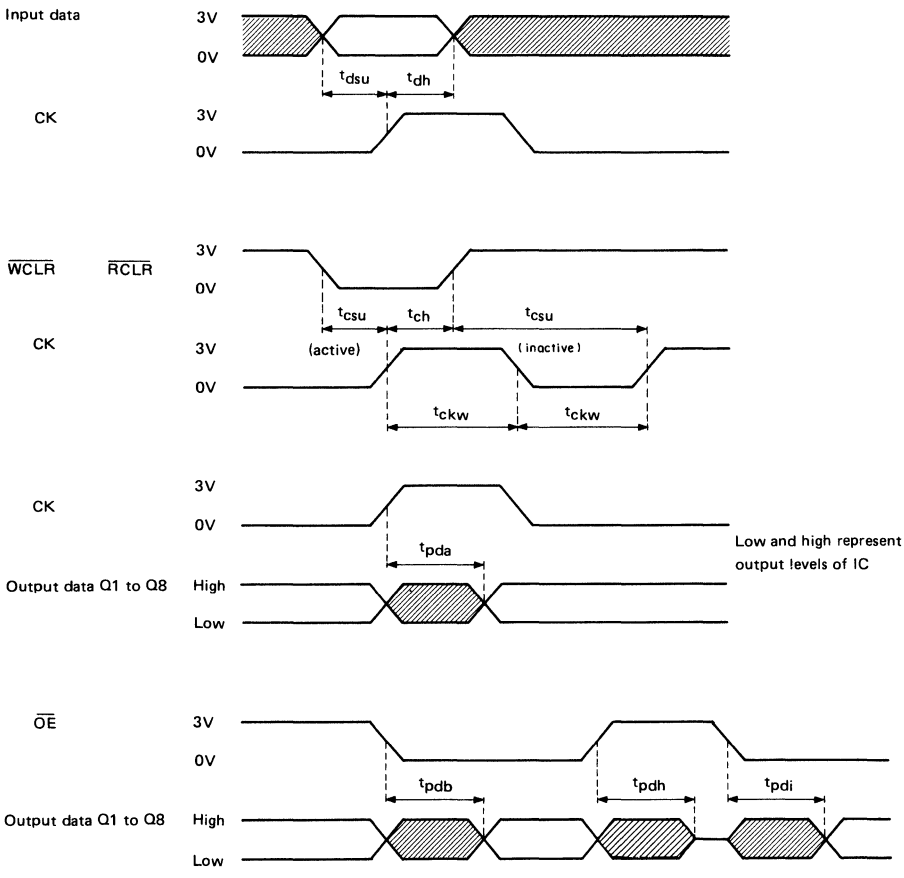
Ta=25°C, fM=1MHz, V_{IN}=V_{OUT}=0V

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacity	C_{IN}	—	—	7	pF
Output pin capacity	C_{OUT}	—	—	10	pF

Timing Chart

(1) The input signal levels are at the low level = 0V and at the high level = 3V, and 5ns for both rising and falling edges.

(2) The voltage judging level of the low and high levels is 1.5V



Application

1. 1H delay line (Delay steps 905 to 912 bits, 1129 to 1136 bits)

Since a clear signal generation circuit is incorporated in the CXK1202S, an external clear signal is unnecessary when it is used as an 1 H delay line. By selecting the DEL pin (pin 21) to "H" level and the $\overline{OE}$ pin (pin 9) to "L" level, they can be used as the delay lines of the delay steps as shown in Tables 1 and 2.

A circuit and timing chart when they are used as the delay line of the delay step 908 bits are as shown in Figs. 1 and 2.

NTSC/PAL (pin 8) pin is at "H"			
S_1	S_2	S_3	Delay step
L	L	L	905
H	L	L	906
L	H	L	907
H	H	L	908
L	L	H	909
H	L	H	910
L	H	H	911
H	H	H	912

Table 1. Delay steps when NTSC mode

NTSC/PAL (pin 8) pin is at "L"			
S_1	S_2	S_3	Delay step
L	L	L	1129
H	L	L	1130
L	H	L	1131
H	H	L	1132
L	L	H	1133
H	L	H	1134
L	H	H	1135
H	H	H	1136

Table 2. Delay steps when PAL mode

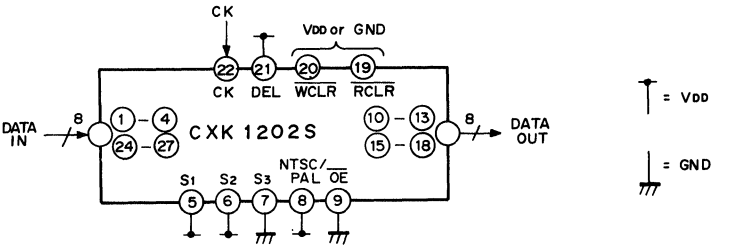


Fig. 1 Circuit of 908 bits delay

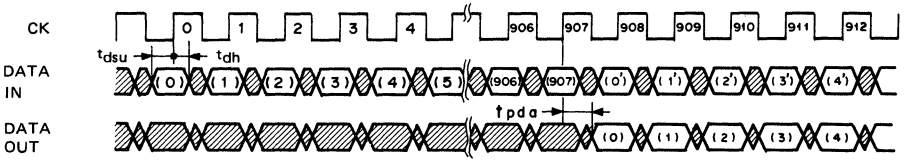


Fig. 2 Timing chart of 908 bits delay

2. Delay line (Delay step 17 to 1144 bits)

By setting the DEL pin (pin21), NTSC/PAL pin (pin 8), and $\overline{OE}$ pin (pin 9) to "L" level, they can be used as a delay line of delay steps 17 to 1144 bits.

The delay steps can be determined by the clear signal and the input level of S_1 to S_3. The clear signal is input always every 8n (n is an integer: n=1, 2, ... 141) clocks. At that time, the obtained delay step is either one from 8 steps of 8(n+1)+1 to 8(n+2) bits. The selection is performed by S_1 to S_3 pins. The number of delay steps to be obtained by the input levels of S_1 to S_3 are tabulated in Table 3.

For example, when used as a delay line of delay step of 123, it is written as 123=8(14+1)+3 and it becomes n=14. Accordingly, input the clear signal every 8×14=112 clocks and set the S_1, S_2 and S_3 pins respectively to "L", "H" and "L" levels and it can be used as a delay line of delay step of 123 bits. The circuit and timing chart at that time are respectively as shown in Figs. 3 and 4.

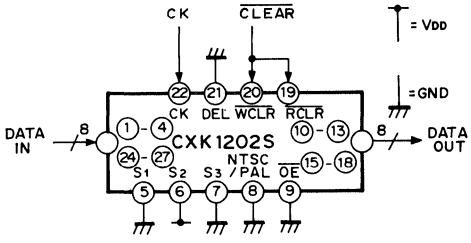


Fig. 3 Circuit of 123 bits delay

n=1, 2, . . . 141

S_1	S_2	S_3	Delay step
L	L	L	8(n+1)+1
H	L	L	8(n+1)+2
L	H	L	8(n+1)+3
H	H	L	8(n+1)+4
L	L	H	8(n+1)+5
H	L	H	8(n+1)+6
L	H	H	8(n+1)+7
H	H	H	8(n+2)

Table 3. Delay steps when clear signal is input every 8n clocks

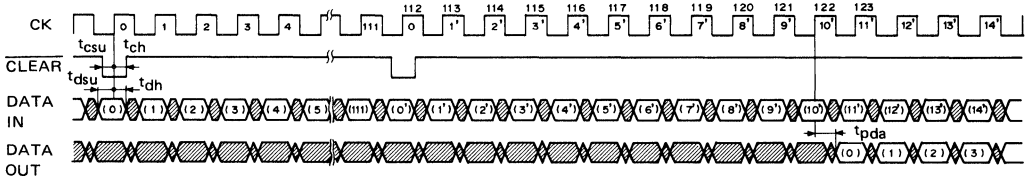


Fig. 4 Timing chart of 123 bits delay

3. Special Application Example — Data Holding

Since SRAM is incorporated in the CXK1202S, data holding can be carried out. However, it is unable to perform random access of the held data. The maximum data holding amount is 1120 words × 8 bit.

The data holding can be carried out by controlling the input timing and clock of the $\overline{WCLR}$ and $\overline{RCLR}$ signals. Set to $\overline{WCLR}$ and $\overline{RCLR}$ signals input modes by selecting the DEL pin (pin 21) to "L" level. By selecting the NTSC/PAL pin (pin 8) to "L" level, the maximum data holding amount of it becomes 1120 words × 8 bit.

- Data writing in

  When the $\overline{WCLR}$ signal is input so as to fetch it at the rising edge of the clock signal, the write address counter is cleared and the data input at that moment is written into the top address. After the $\overline{WCLR}$ signal has been transferred to "H" level from "L" level, the write address counter is incremented and the data are recorded in the order they have been input. If there are data, which are desired to be written in, up to i-th (i is an integer: i=0, 1, 2 . . . 1119) and when the condition is $8m \leqq i \leqq 8m+7$ (m is an integer: m=0, 1, 2, . . . 139), input the clock signals up to $8(m+1)+2$ to $8(m+1)+7$ counted from the $\overline{WCLR}$ signal input and it becomes necessary to stop the input of the clock signal there-after. (Fig. 6)

  Note)
  - Be sure that if the clock signal after $8(m+1)+7$th clock signal is not stopped, it keeps counting on as if there are input data.
  - When the clock is stopped at other than $8(m+1)+2$ to $8(m+1)+7$, the power supply current is somewhat increased so it is desired not to stop it.

- Data read out

  When the $\overline{RCLR}$ signal is input so as to fetch it at the rising edge of the clock signal, the data having been held commence to output data after 8 to 15 clocks from that clock. The data are output in the same order as they have been written in. The data output commencing period is dependent on the levels of S_1 to S_3 as shown in Table 4.

  A circuit example when data is output from after 11 clocks is as shown in Fig. 5 and its timing chart is as shown in Fig. 7.

  Moreover, the data read out once is held unless it is rewritten.

  Note)
  - If the $\overline{RCLR}$ signal is input during data writing, reading out from after 8 to 15 clocks is possible. At that time, input the $\overline{RCLR}$ signal after 8k clocks (k is an integer: k=1, 2, 3, . . . 141) from the $\overline{WCLR}$ signal input. (Fig. 8)
  - Do not stop the clock while reading the data is being performed.

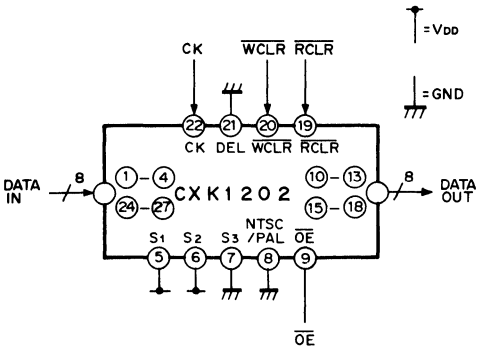
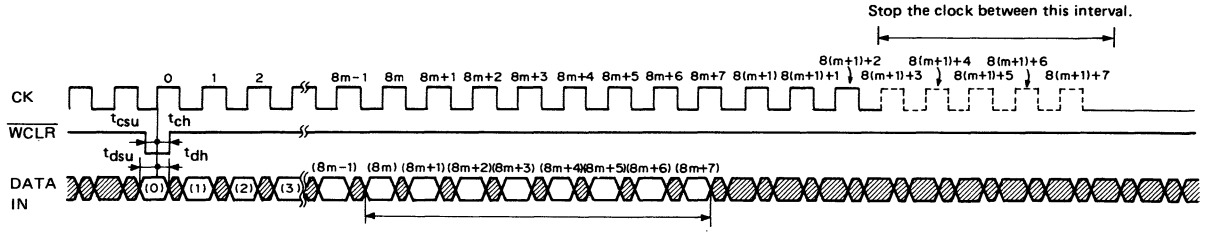


Fig. 5 A circuit from the $\overline{\text{RCLR}}$ signal is input to the data output commencement

S_1	S_2	S_3	Output commencing period
L	L	L	After 8 clocks
H	L	L	After 9 clocks
L	H	L	After 10 clocks
H	H	L	After 11 clocks
L	L	H	After 12 clocks
H	L	H	After 13 clocks
L	H	H	After 14 clocks
H	H	H	After 15 clocks

Table 4. Number of clocks when the $\overline{\text{RCLR}}$ signal is input to the data output commencement (Make clock in which $\overline{\text{RCLR}}$ signal has been input to 0)



Note) • i = 0, 1, 2, . . . 1119
• m = 0, 1, 2, . . . 139

Fig. 6 The data write in timing when they are being held

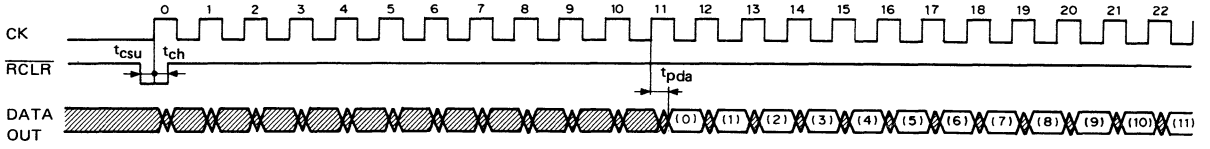


Fig. 7 The data read OUT timing
(When S1="H", S2="H" and S3="L"
After 11 clocks outputs commencing period in Table 4.)

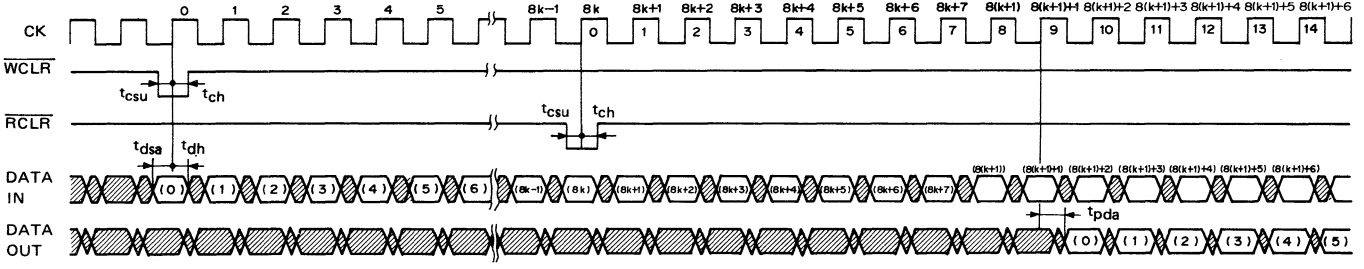
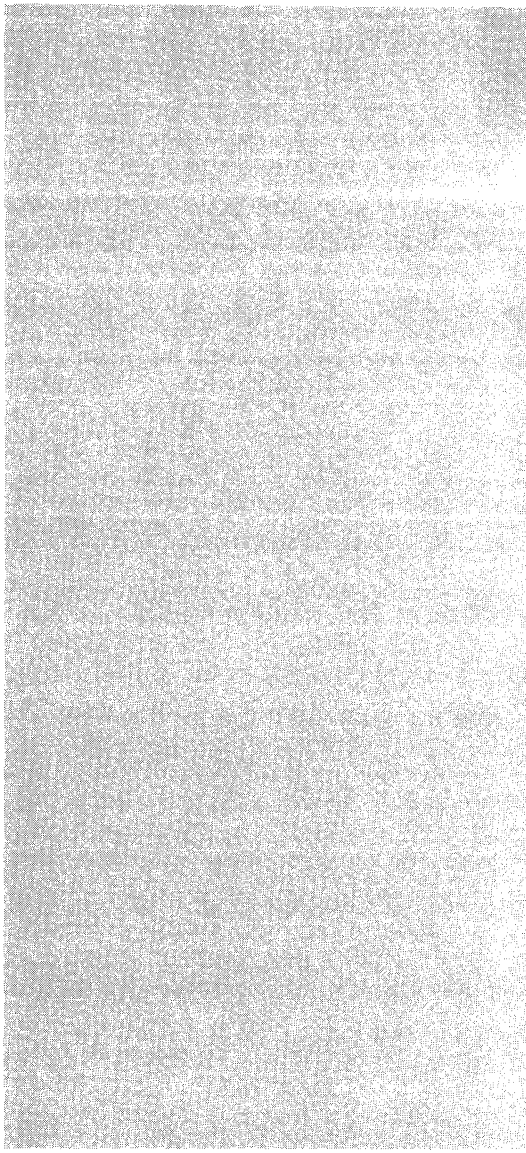
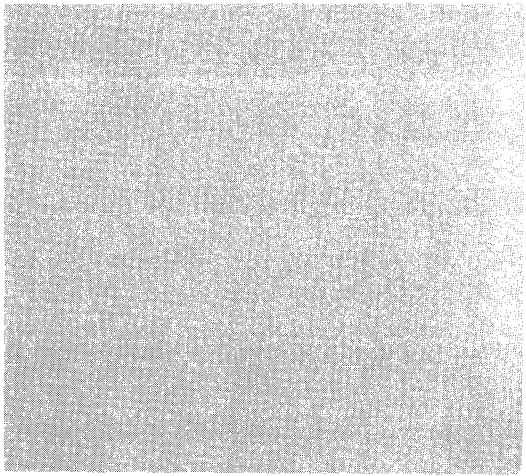


Fig. 8 The timing of data read out while writing in data
(When S1="H", S2="L" and S3="L")

Note) k = 1, 2, . . . 141



Evaluation Printed Circuit Boards



4) Evaluation Printed Circuit Boards

Type	Function	Page
CX20017 PCB	CX20017 Evaluation Board	307
CX20018 PCB	CX20018 Evaluation Board	311
CX20052A PCB-3A/3B	8bit 20/15MHz A/D Converter Evaluation Board	322
CX20116/U CXA1066K/UK } PCB	8bit 100MHz A/D Evaluation Board	328
CX23060 PCB	CX23060 Evaluation Board	336
CXA1016P/K/UK CXA1056P/K/UK } PCB	8bit 50MHz/30MHz A/D Evaluation Board	343
FCX20220A-1/-2	10bit/9bit 20MHz Sub-ranging A/D Converter Evaluation Board	352

SONY CX20017PCB

CX20017 Evaluation Board

Description

CX20017PCB is the evaluation board for CX20017, Dual 16 bit, 44 kHz, Multiplexed D/A. This board consists of CX20017, a pair of Sample Hold Amplifiers (Deglitchers), an Analog switch, a pair of LPF, and a pair of output drive Amps.

1) This PCB requires the following Input signals and power supplies

1. The digital control signals
   - BCLK TTL input
   - WCLK TTL input
   - LRCK TTL input
2. Data input
   - DATA TTL input
3. Power supplies
   - ±15V (+15V – 100mA, −15V – 200mA)

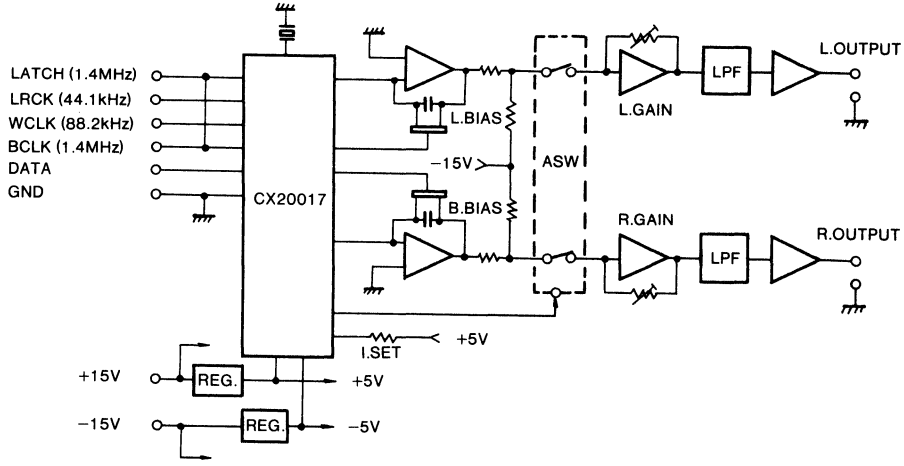
2) The interface connectors

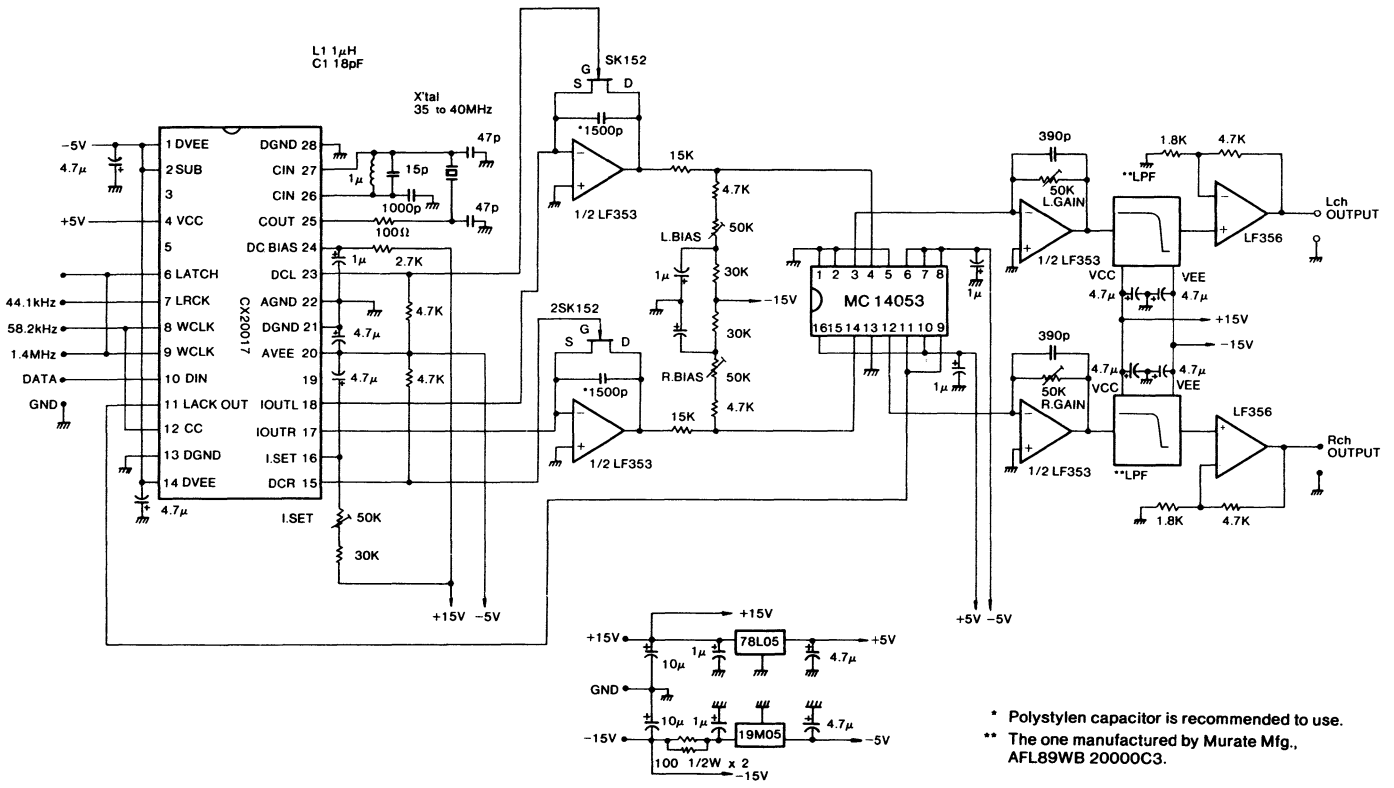
AMP, Inc MTA-100 Closed End Housings
- 6 Pin Connector
- 3 Pin Connector
- 2 Pin Connector (× 2)

3) The output from the PCB

1. L.OUTPUT
2. R.OUTPUT

4) CX20017PCB Block Diagram





* Polystylen capacitor is recommended to use.

** The one manufactured by Murate Mfg., AFL89WB 20000C3.

Fig. 1 CX20017PCB Schematic Diagram

Unit: mm

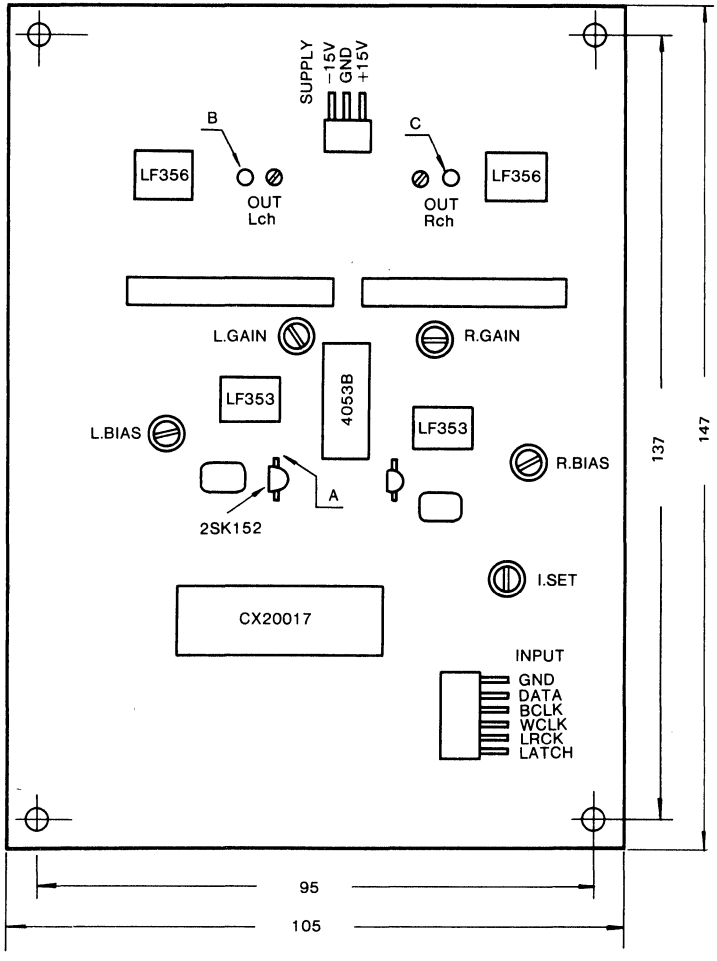


Fig. 2 CX20017PCB Check Points

1. CX20017 Adjustment

Fig. 2 shows the adjustment points (A, B, C). Point A is the drain of the FET (2SK152). Points B and C are the Lch and Rch Outputs respectively. LRCK is the same signal as WCLK in A/D Converter. When the maximum Input (10 Vp-p) is supplied to A/D, a max. digital input data (01 – 1 to 10 – 0) is supplied to D/A data input (10 pin of CX20017). We will adjust both outputs to 10 Vp-p. The following are the adjustment procedures:

1) I. SET

Check point A. Adjust the variable resistor I. SET to get the 6 Vp-p output level. (See Fig. 3).

2) L. BIAS and L. GAIN

Check point B. Turn the input level to 0 Vrms and adjust the variable resistor L.BIAS to get the 0 level output offset.

Supply the max. input 10 Vp-p to A/D and adjust the output level to 10 Vp-p with L.GAIN variable resistor.

3) R.BIAS and R.GAIN19c

Change the check point to point C, and repeat adjustments with R.BIAS and R.GAIN variable resistors.

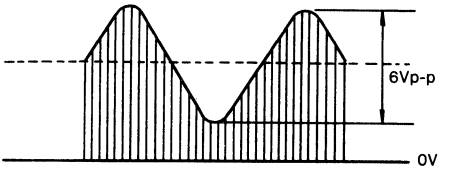


Fig. 3 The Waveform at Point A

SONY CX20018PCB

CX20018 Evaluation Board

Description

CX20018PCB is an evaluation board for CX20018, Dual 16 bit, 44 kHz, Multiplexed A/D. This board consists of CX20018, a pair of Sample Hold Amplifiers, 84.6 MHz MCLK Oscillator Circuit, and ±5V Voltage Regulators.

1) This PCB requires the following Input signals and power supplies

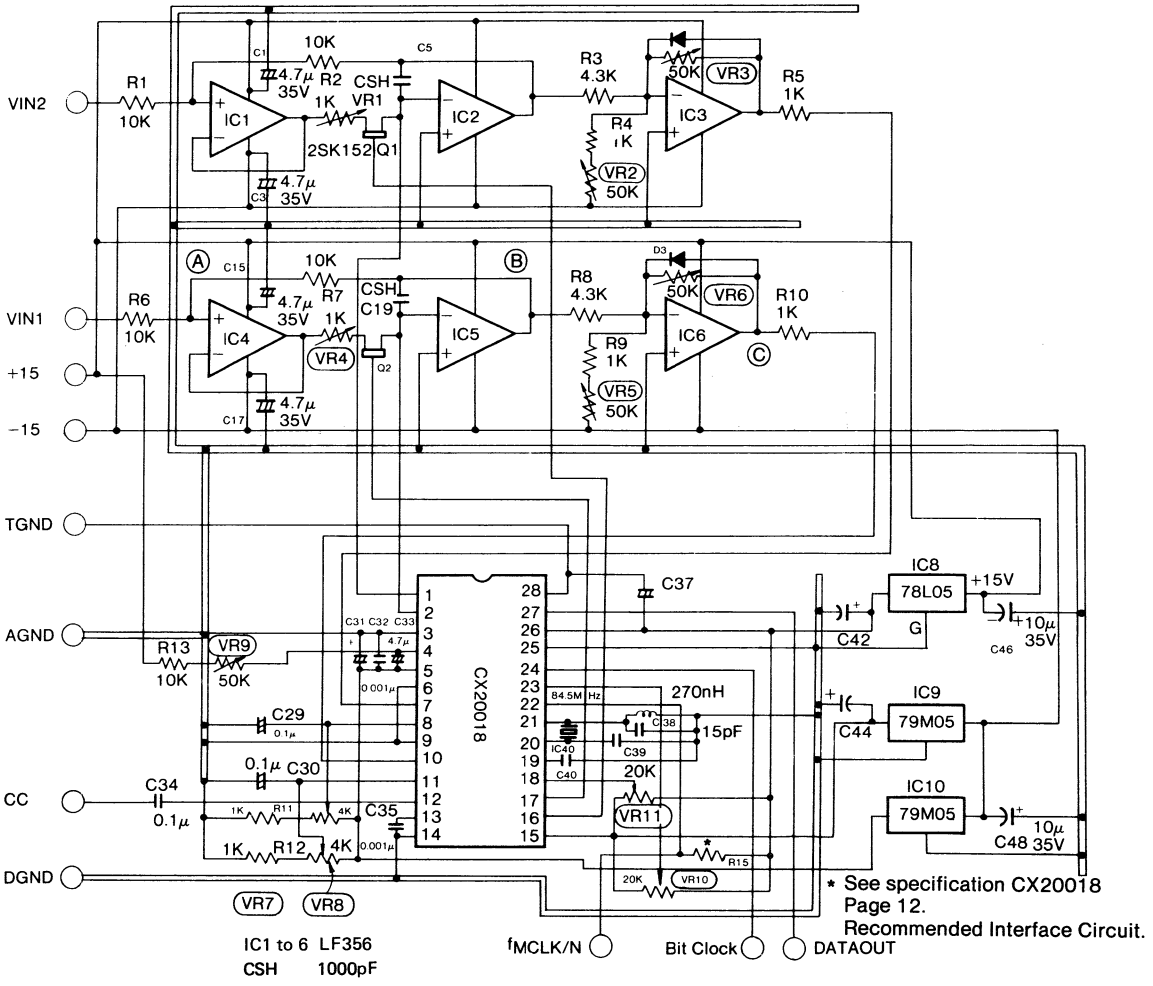
1. The digital control signals
   - BCLK TTL input
   - CC TTL input
2. Analog Inputs
   - Vin1, Vin2 10 Vp-p max.
3. Power supplies
   - ±15V (+15V – 100mA, −15V – 200mA)

The interface connector for the PCB is recommended to use 22 positions edge connector, supplied by AMP, Inc or the other vendors.

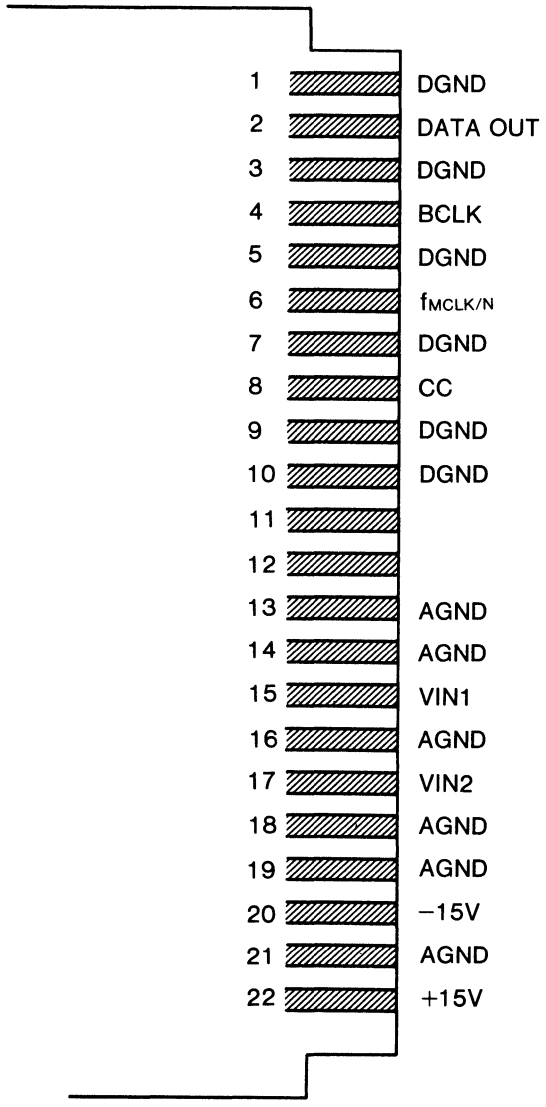
2) The output from the PCB

1. DATA OUT TTL output
2. $f_{MCLK/n}$ Check CX20018 data sheet

CX20018PCB Schematic Diagram



SONY



Pin Configuration for PCB

CX20017/18 Adjustment Procedure

Fig. 1 shows the test system for CX20018PCB and CX20017PCB.

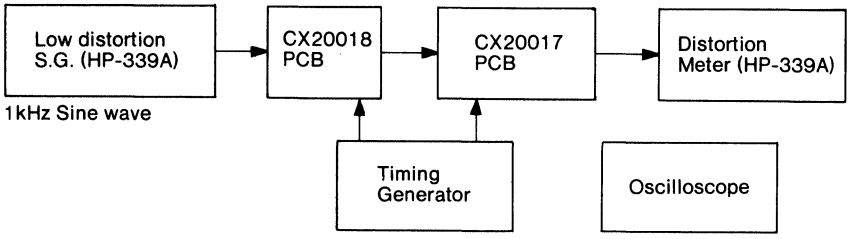


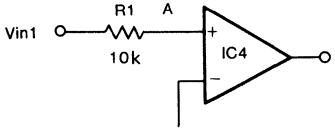
Fig. 1 Test System

1. CX20018PCB Adjustment

CX20018PCB consists of 2 S/H and A/D, and 2 channel signal can be converted to a serial digital signal. Adjustment should be achieved for both S/H respectively. At first adjust Vin1.

1) Check point A. (IC4 Input)

Input analog signal level at point A should be adjusted to 10 Vp-p. (See Fig. 2)



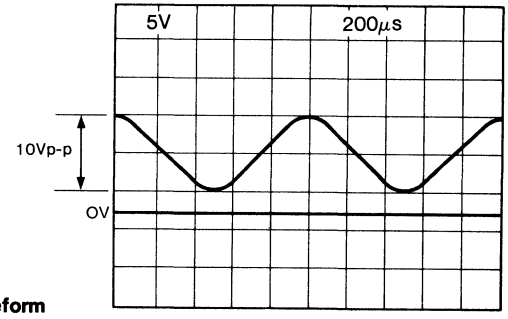


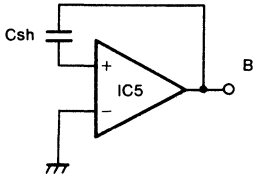
Fig. 2 Point A Waveform

2) Check either L.OUTPUT or R.OUTPUT of CX20017PCB.

Adjust VR5 and VR9 to get the maximum output by eliminating a clipping waveform. VR5 is DC offset adjustment volume and VR9 is Iset adjustment volume.

3) Check point B (IC5 output) and CC. (Pin8 of CX20018PCB)

Adjust VR4 to get the integrated waveform. (See Fig. 3) VR4 is the adjustment volume for the settling time of S/H.



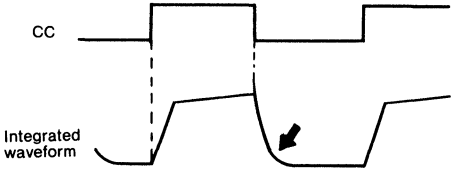


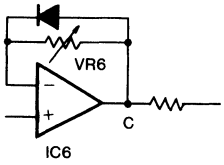
Fig. 3 Integrated Waveform

When the sinusoidal waveform is observed at point B, magnify the range of time base. Then, the integrated waveform will be observed.

4) Check point C. (IC6 output)

Adjust VR6 to get the waveform at point C as the waveform in Fig. 4. After this adjustment, check CX20017PCB output.

If the output waveform is clipped, adjust VR5 to eliminate this clipping.



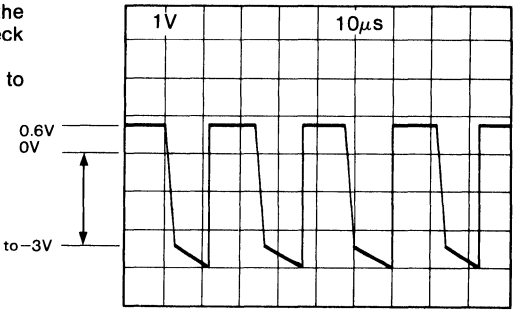


Fig. 4 Point C Waveform

5) Check the waveform at the monitor output of the distortion meter. VR8 is the refference voltage adjustment volume.
Adjust VR8 to get approximately −90 dB distortion level.

6) Adjust VR4 again and get the distortion level less than −90dB.
(See Fig. 5)

7) Adjustment procedure for Vin2 and the other S/H circuit is just the same as the procedure (1 through 6). However do not touch VR9, because this volume is shared for S/H1 and S/H2.

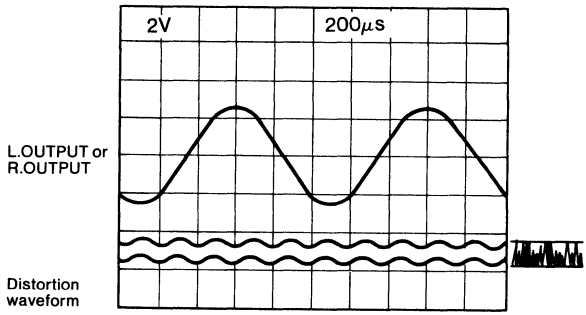


Fig. 5 Distortion Level (−90dB)

CX20018PCB Block Diagram

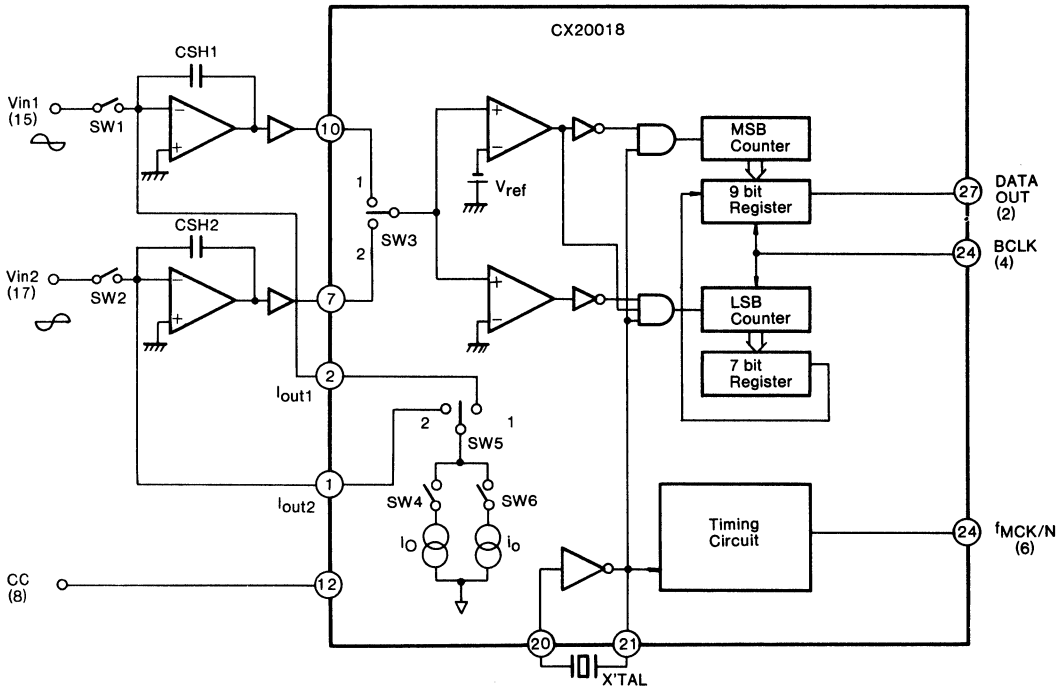


Fig. 6 ( ) - - - Pin Number of CX20018PCB

2. CX20017PCB Adjustment

Fig. 1 is also the measurement system for CX20017PCB. Fig. 8 shows the adjustment points (A, B, C). Point A is the drain of the FET (2SK152). Points B and C are the Lch and Rch Outputs respectively. LRCK is the same signal as CC in A/D converter. When the maximum input (10 Vp-p) is supplied to A/D, a maximum digital input data (01 – 1 to 10 – 0) is supplied to D/A data input (10 pin of CX20017). We will adjust both outputs to 10 Vp-p. The following are the adjustment procedures:

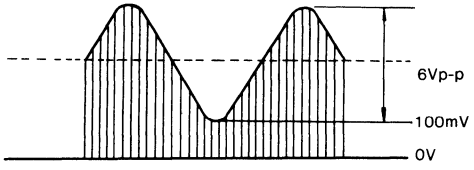


Fig. 7 The Waveform at Point A

1) I. SET

Check point A. Adjust the variable resistor I.SET to get the 6Vp-p output level. (See Fig. 7.)

2) L.BIAS and L.GAIN

Check point B. Turn the input level to 0 Vrms and adjust the variable resistor L.BIAS to get the 0 level output offset.

Supply the maximum input 10 Vp-p to A/D and adjust the output level to 10 Vp-p with L.GAIN variable resistor.

3) R.BIAS and R.GAIN

Change the check point to point C, and repeat adjustments with R.BIAS and R.GAIN variable resistors.

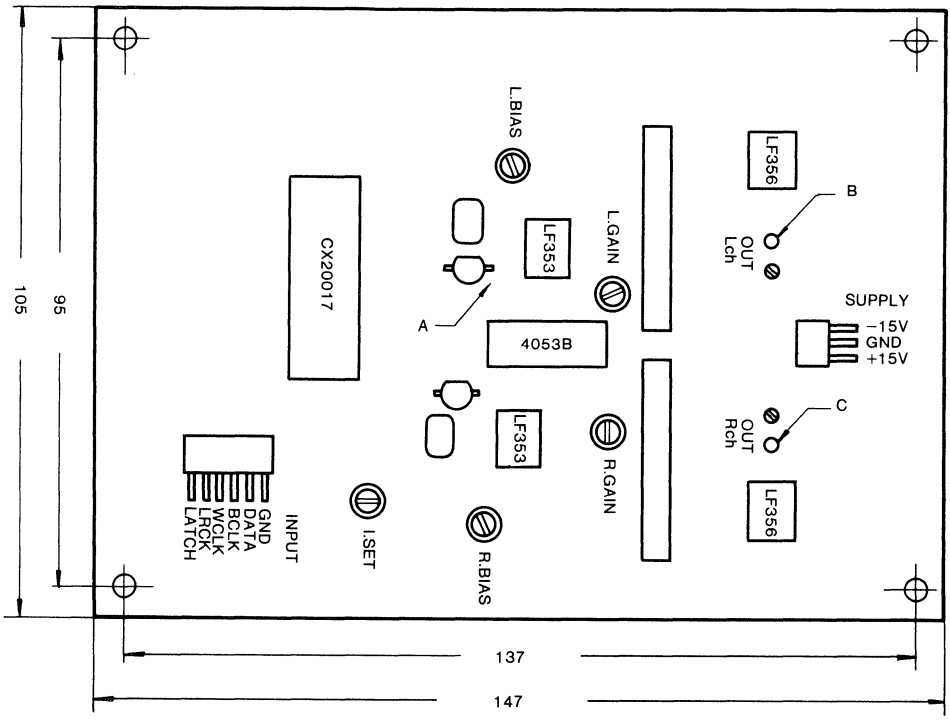


Fig. 8 CX20017PCB Check Points

3. Timing Generater

Fig. 9 shows the example of the Timing Generater circuit. Fig. 10 is the timing chart for this circuit.

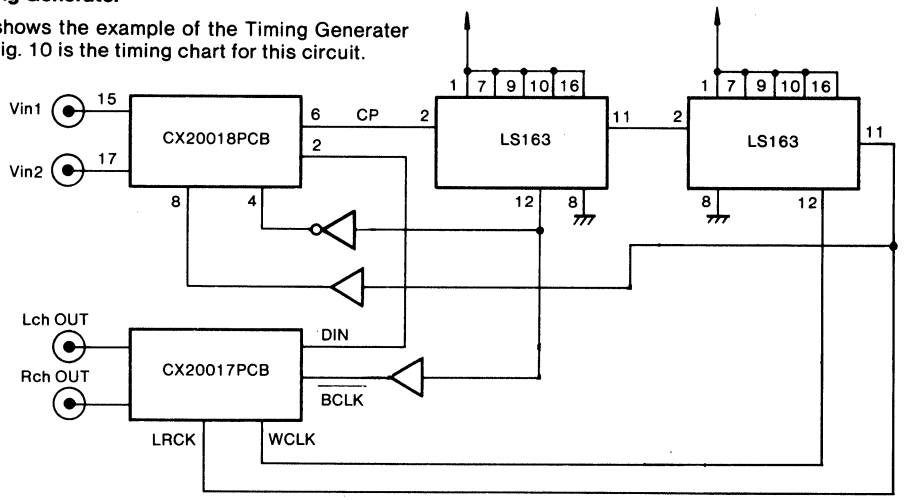


Fig. 9 Timing Generater

* The frequency of CP is 10.58MHz when VR10 of CX20018PCB is adjusted to −4V.

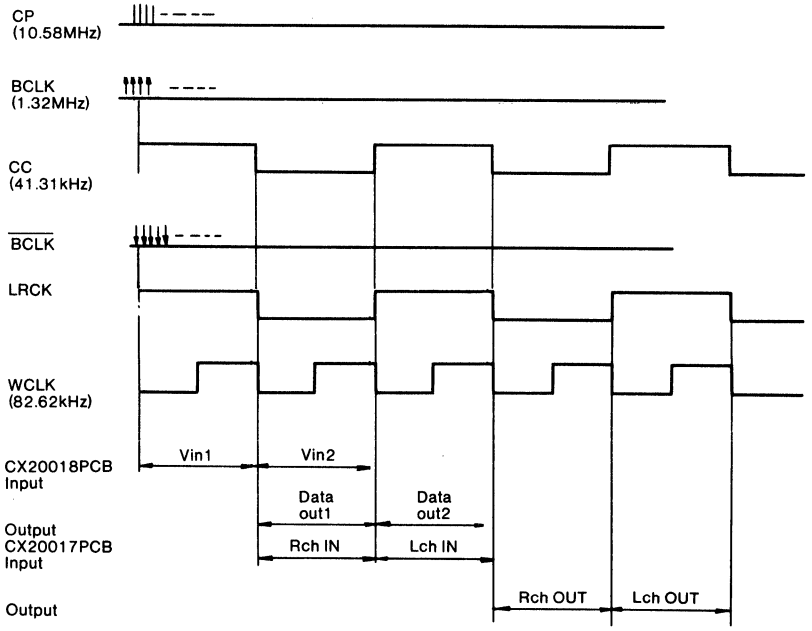


Fig. 10 Timing Chart

CX20018PCB DC Offset Compensation Circuit

Monolithic A/D Converter CX20018 claims 16 bit resolutions for audio signal processing. However, if the fairly high temperature stability is required, the following two issues should be considered:

1. Temperature characteristics for the integration current
2. DC offset compensation

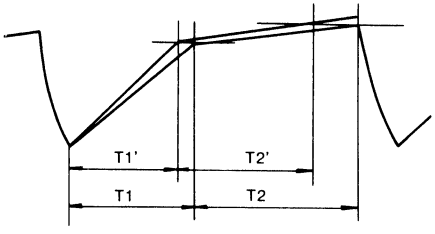
1. Temperature characteristics for the integration current

The pair of integration current, Io and io has temperature dependence. If the current source Iset is held in the fixed current level, and measured the current ratio Io/Iset and io/Iset, both the temperature coefficients are around 90ppm/°C (typ.). As shown in the following figure, the integration time will be reduced for the same Input signal level when temperature comes up.

Assumes the following parameters:
T: integration time
V: threshold voltage
Csh: Sample-hold capacitance
I: Integration current

$$I \cdot T = Csh \cdot V$$

$$V = \frac{I}{Csh} \cdot T$$



I/Csh should be kept constant for temperature change. If the temperature coefficient for Io/Iset, Iset, and Csh are defined as EI(Ei), Es, and Ec Total temperature coefficient is

$$Etotal = EI + Es - Ec$$

Because of insuring high reliability CX20018PCB adopted the polystyrene capacitors for Csh. The temperature coefficient is around −160 ppm/°C (typ.). Current source Iset is adjusted by the volume VR9. To minimize the value of Etotal, this volume should be replaced by the fixed value resistor having the positive temperature coefficient.

For example, a metal film resistor has around 100 ppm/°C temperature coefficient. Etotal will be around 150 ppm/°C. To minimize the value Etotal, use the polycarbonate capacitor having the positive temperature coefficient.

2. DC offset compensation

There are several factors to be considered to compensate DC offset, including the offset of CX20018 internal comparators, external OP amplifier's DC offset drift, and so forth.

There is one idea to compensate the total offset drift.

The recommended circuit is shown in Fig. 1.

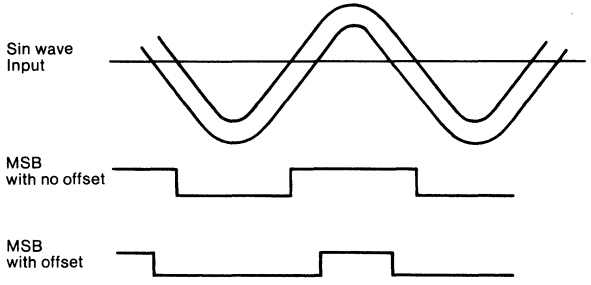
* Circuit operation

Any audio signals can be separated into several components of the sine wave signal.

Pick up one sine wave signal.

When this signal is digitized, MSB will be high level for the signal portion above ϕ level and MSB will be low level for the signal portion below ϕ level. (See A in Fig. 11)

If there is DC offset, MSB waveform will change to B)



In Fig. 11, integration OP amplifier output.

Stays ϕ level when there is no DC offset.

If there is positive DC offset, the negative feedback signals come back to the limiter amplifier, IC3 or IC6 respectively.

Adjust the trimming resistor (1 MΩ) to get to the minimal DC offset.

Fig. 12 shows the timing chart of the compensation circuit.

D Flip Flops are used to sample MSB digital output for Vin1 and Vin2. The signal output at point B and C are corresponding to the DC offsets for Vin1 and Vin2.

Test Circuit

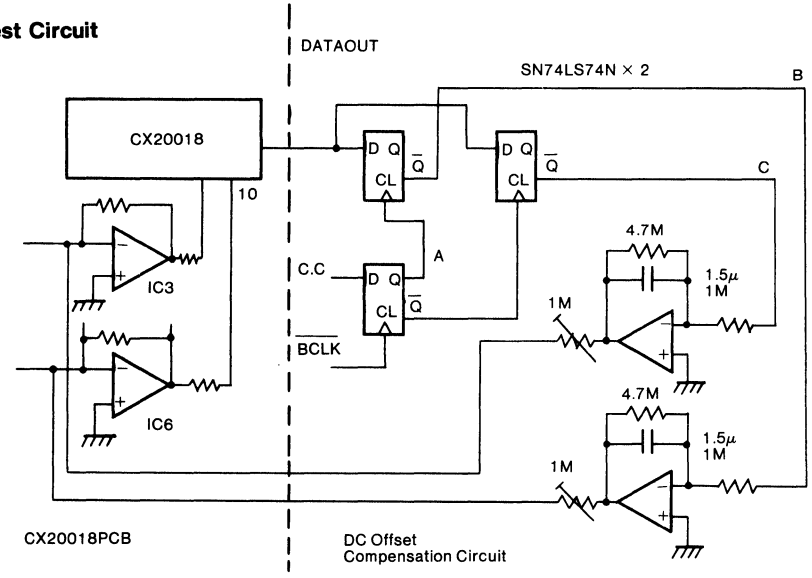


Fig. 11

Timing Chart

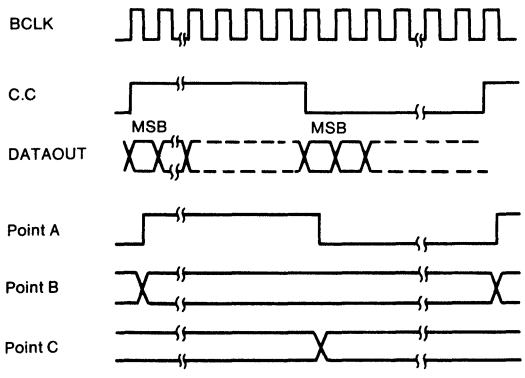


Fig. 12

SONY CX20052A PCB-3A/3B

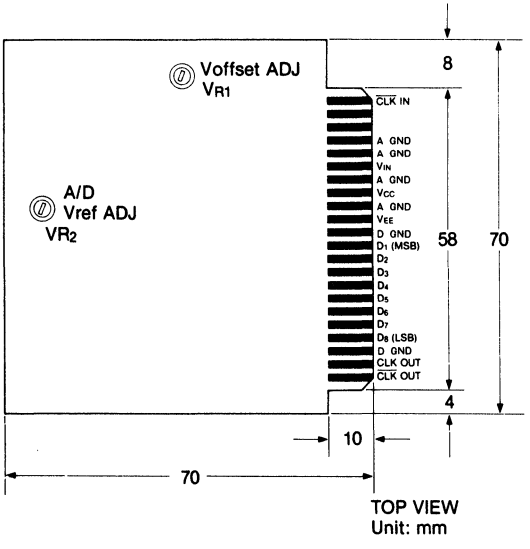
8 bit 20/15 MHz A/D Converter Evaluation Board

Description

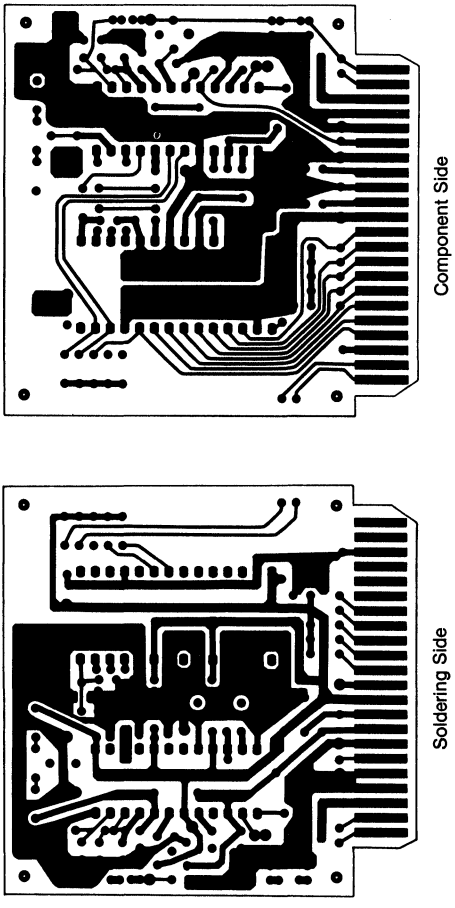
CX20052A PCB-3A/3B is an 8 bit A/D converter board for video signal processing. A high speed S/H IC CXA1008P/1009P and a high speed 8 bit A/D converter CX20052A are assembled on single small printed circuit board.
CX20052A PCB-3A with CXA1008P mounted, operates up to 20 MHz of conversion rate, and CX20052A PCB-3B with CXA1009P mounted, operates up to 15 MHz of conversion rate.

Features

•Resolution	8 bit ±1/2 LSB
•Conversion rate	20 MHz CX20052A PCB-3A
	15 MHz CX20052A PCB-3B
•Analog input level	1Vp-p
•Digital output level	ECL level
•Power supply	±5V

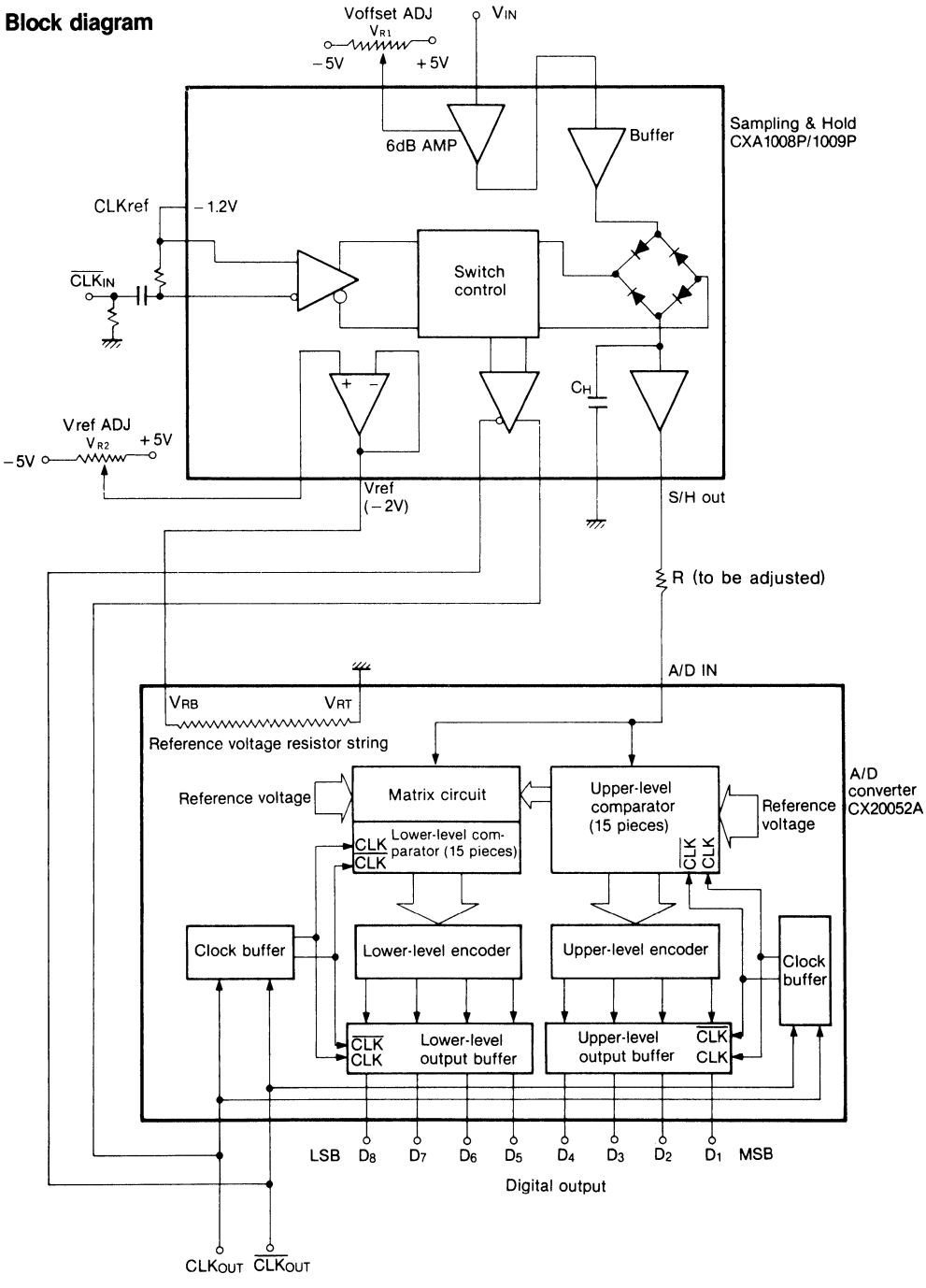


TOP VIEW
Unit: mm



CX20052A PCB-3A/3B Pattern

1. Block diagram



2. Characteristics

1. Supply Voltage

($Ta = 25°C$, $V_{EE} = -5V$, $V_{CC} = 5V$)

Item			Symbol	Min	Typ	Max	Unit
V_{CC}	+5V	CX20052A	I_{CC}		70	80	mA
		PCB-3A	I_{EE}		220	240	mA
V_{EE}	−5V	CX20052A	I_{CC}		50	60	mA
		PCB-3B	I_{EE}		200	220	mA

2. Analog Input (V_{IN})

Item	Symbol	Min	Typ	Max	Unit
AC Input Voltage Amplitude	V_{IN}			1	V
Offset Adjustable Range		±1.5	±2.0		V
Input Impedance	Z_{in}				
CX20052APCB-3A			75		Ω
CX20052APCB-3B			75		Ω

3. Digital Input ($\overline{CLK}$ IN)

Item	Symbol	Min	Typ	Max	Unit
Input Voltage (p-p)	V_{CLK}	0.3	0.8	4	V
Input Impedance	Z_{INCL}		50		Ω

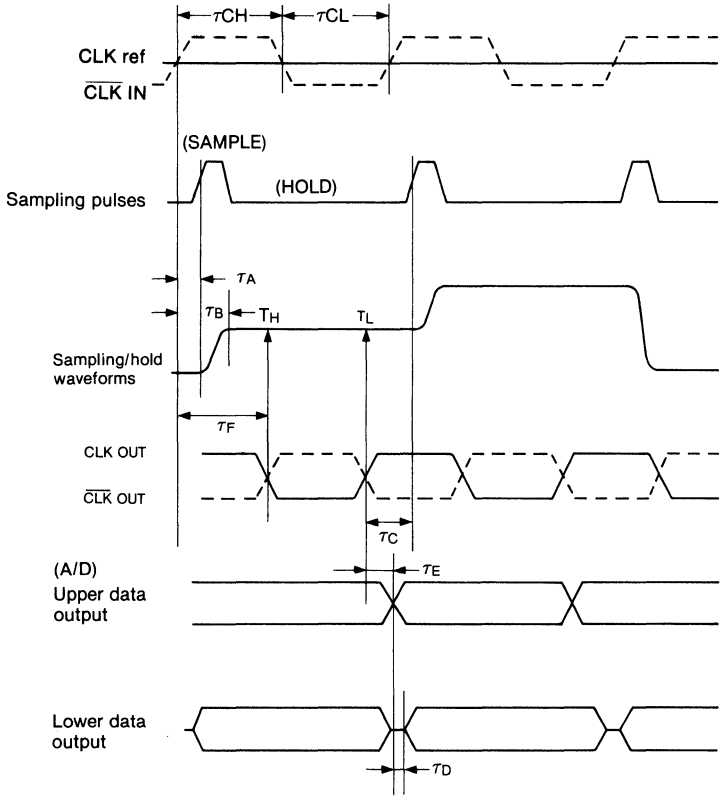
4. Digital Output (D1 − D8) (1.5kΩ to V_{EE})

Item	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OH}	−0.90	−0.75		V
	V_{OL}		−1.50	−1.35	V

5. Clock Output (CLK_{OUT}, $\overline{CLK}_{OUT}$) (See timing chart)

Item		Symbol	CX20052A PCB-3A			CX20052A PCB-3B			Unit
			Min	Typ	Max	Min	Typ	Max	
Output voltage	Amplitude	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low Level	V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time		tr		6	10		6	10	ns
Fall time		tf		12	15		12	15	ns
CLK Delay		τ_F	20	28	34	36	38	45	ns

3. Timing Chart



T_H shows a timing when the A/D latches upper 4 bits.
T_L shows a timing when the A/D latches lower 4 bits.

Item	Symbol	CX20052A PCB-3A			CX20052A PCB-3B			
		Min	Typ	Max	Min	Typ	Max	Unit
Clock in	τ_{CH}		25			33		ns
	τ_{CL}		25			33		ns
Sampling delay	τ_A		6			12		ns
	τ_B		25			36		ns
Clock out	τ_F	20	28	34	36	38	45	ns
Data delay	τ_E			8			8	ns
	τ_D			4			4	ns

4. Adjustment

(1) Offset Voltage (Voffset ADJ)
VR_1 should be adjusted so that the S/H output meets the input voltage range of the A/D (0 to −2V).
(2) A/D reference voltage (Vref ADJ).
The reference voltage of the A/D (TP5) is to be −2V. VR_2 should be adjusted.

5. Output Data Format

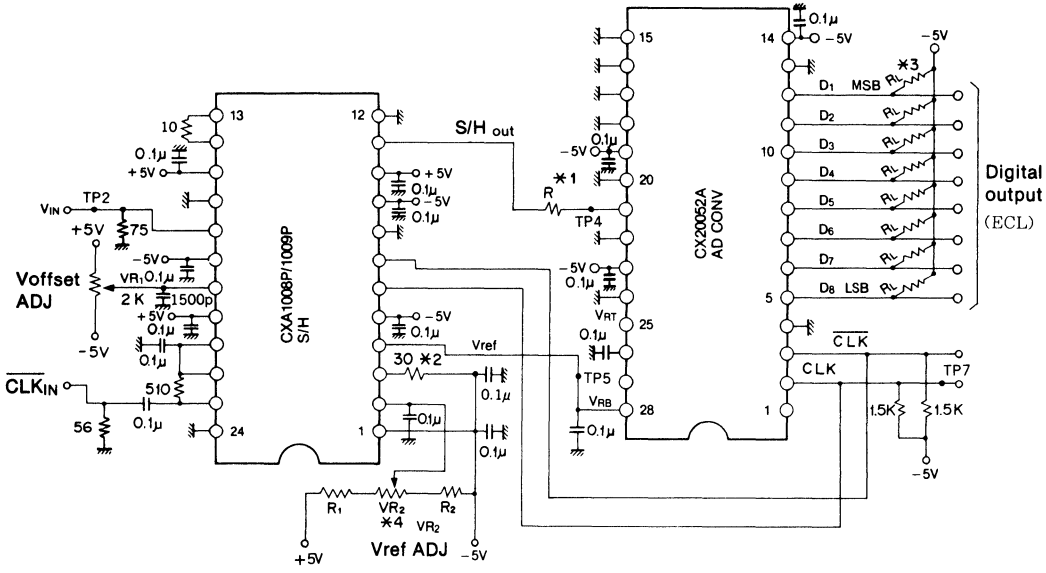
The input of the A/D converter IC (S/H out) is quantized in 8 bit within the reference voltage range of V_{RT} and V_{RB}. The V_{RT} and V_{RB} are set at 0V and −2V respectively on the printed circuit board.

Step	A/D input signal voltage		Digital output code
			MSB LSB
	over	0.0000V	1 1 1 1 1 1 1 1
0 0 0		0.0000V (V_{RT})	1 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
1 2 7		−0.9961V	1 0 0 0 0 0 0 0
1 2 9		−1.0039V	0 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
2 5 5		−2.0000V (V_{RB})	0 0 0 0 0 0 0 0
	under	−2.0000V	0 0 0 0 0 0 0 0

6. Note on application

(1) Although the pull down resistors (RL: 4.3kΩ) are mounted on the PCB, additional pull down is recommended in an external circuit. The output current at the A/D output terminal should not exceed 10 mA.
(2) Digital output data should be latched by an external circuit to achieve a rated performance. Output data can be latched at a rising edge of CLK_{OUT}.
CLK_{OUT} AND $\overline{CLK}_{OUT}$ should be reshaped by an ECL line receiver such as MC10116 in an external circuit.
(3) The reference voltage is derived from the V_{EE} by a simple resistor dividing network. The power supply (±5V) should be stabilized to reduce voltage drift of the reference voltage.
(4) To reduce CLK leak, use waveforms similar to sine waves as far as possible up to the CLK input. For satisfactory operation, a CLK input amplitude of around 300m V_{PP} is enough.
(5) When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

CX20052A PCB-3A/3B Circuit

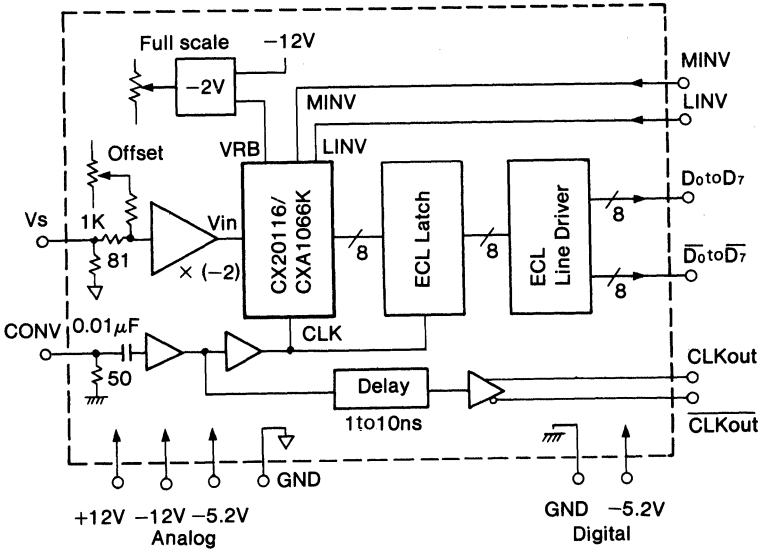


*1. R is a ringing preventing resistor. Select between 10 to 50Ω according to pattern length.
*2. Pulldown R for Vref.
*3. $R_L = 4.3k\Omega$
*4. $R_1 = 2k\Omega$, $VR_2 = 2k\Omega$, $R_2 = 1k\Omega$

8 bit 100 MHz A/D Evaluation Board

Description

The CX20116 PCB/CX20116U PCB/CXA1066K PCB/CXA1066UK PCB are the evaluation printed circuit boards for 8 bit high speed A/D converter CX20116/CX20116U/CXA1066K/CXA1066UK. On this one board, A/D, driver, standard voltage source, latches and ECL line drivers are mounted, and this PCB is designed to achieve the best performance of the A/D converter.



PCB Characteristics

- Analog input band width 40 MHz (at −3 dB)
- Analog input impedance 75Ω
- Complementary ECL output
- Clock output (Delay time 0 to 10ns adjustable)

Supply Voltage

• Analog	+12V	80 (Max.)	mA
	−12V	80 (Max.)	mA
	−5.2V	250 (Max.)	mA
• Digital	−5.2V	460 (Max.)	mA

1. Analog Input (Vs)

Item	Min.	Typ.	Max.	Unit
AC Input Voltage Amplitude*	–	1	1.1	V
Offset Adjustable Range	−0.25	0	1	V
Input Impedance	–	75	–	Ω

* peak to peak

2. Convert Input Signal (CONV)

Item		Min.	Typ.	Max.	Unit
Input Voltage*		0.6		1.0	V
Input Impedance		–	50	–	Ω
DC Level		–3		3	V
Pulse Width	Tcw 1	7.5			ns
	Tcw 0	2.5			ns

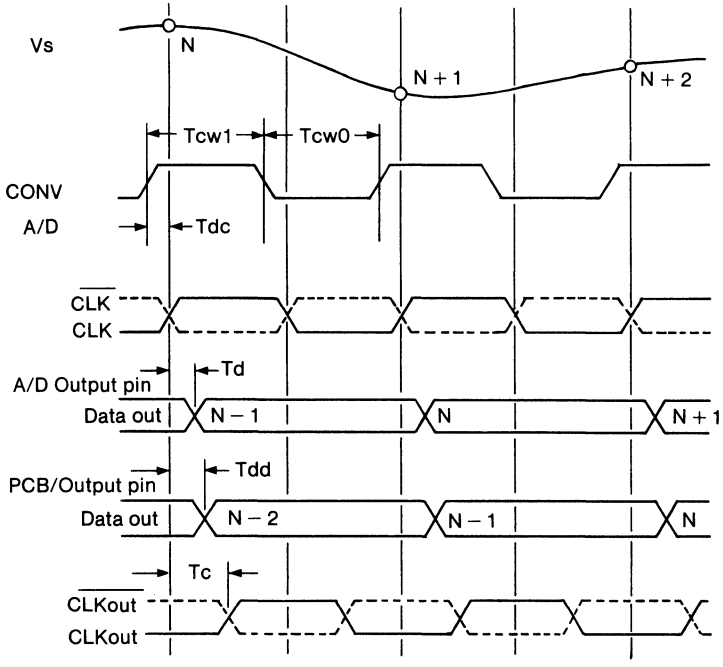
* peak to peak

3. Control Input (MINV, LINV)
ECL 10K compatible

4. Digital Output (D_0 to D_7, $\overline{D}_0$ to $\overline{D}_7$)
ECL 10K compatible, complementary output

5. Clock Output
ECL 10K compatible, complementary output
Delay time adjustable

6. Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
Conversion Delay	Tdc		3.5		ns
Data Delay	Tdd		5.5		ns
Clock Delay Adjustable Range*	Tc	1		10	ns

* Adjustable in 1ns step by taps

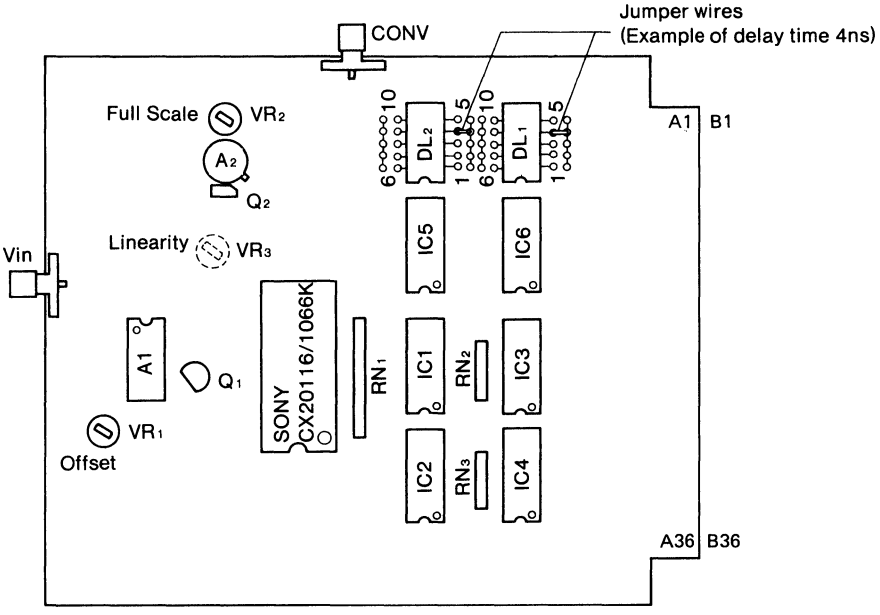
7. Output Coding

	MINV LINV	0 0	0 1	1 0	1 1
	0V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
	.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
Vin	.	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
	.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
	−2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1 : V_{IH}
0 : V_{IL}

8. Adjusting Method of Clock Output Delay Time

Clock output delay time can be adjusted by jumper wires position on the PCB.
Tap positions should be changed simultaneously in CLK and $\overline{CLK}$, avoiding the effect of waveform distortion.
Delay time in each taps are 1ns.



9. Note on Application

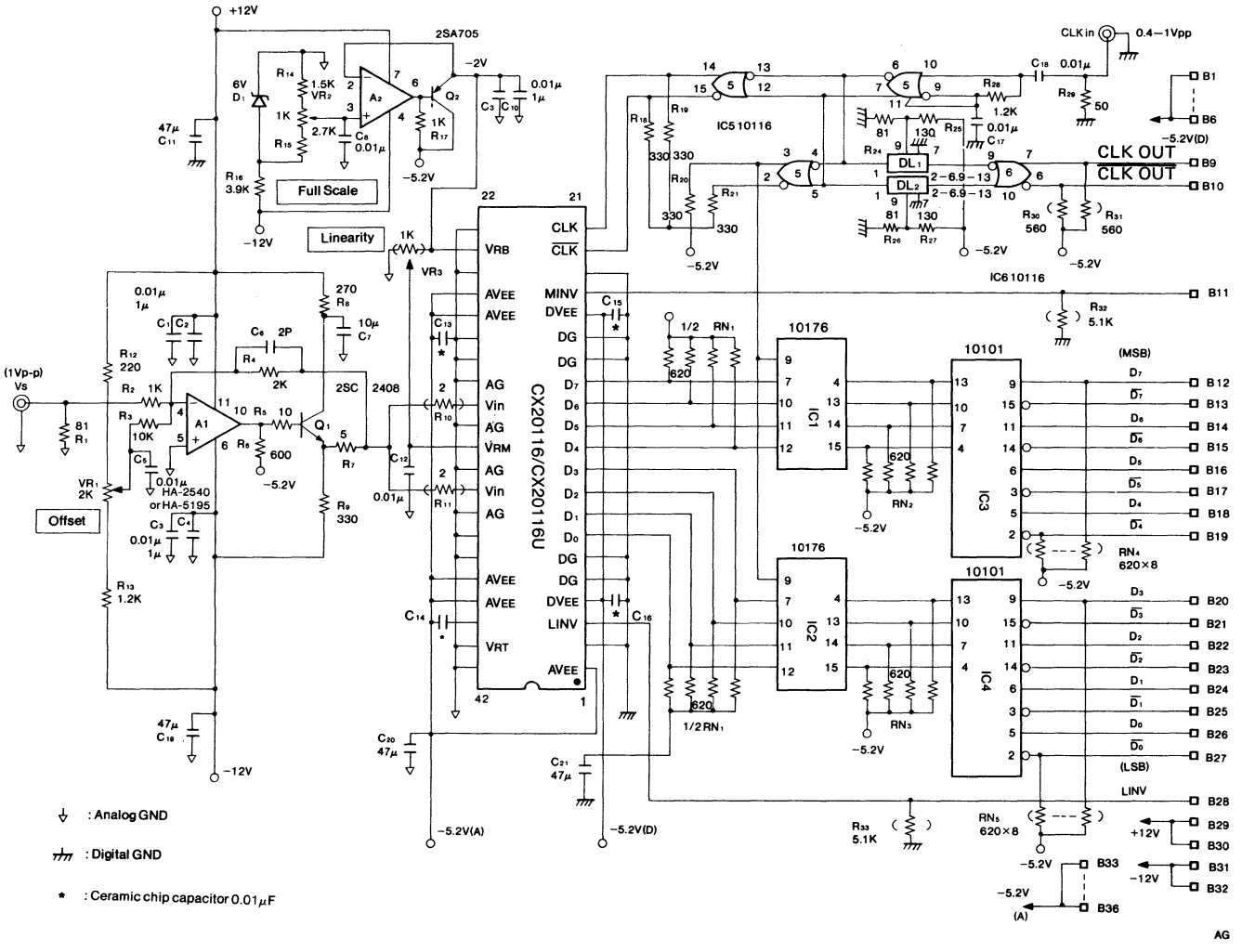
9-1. GND, VEE

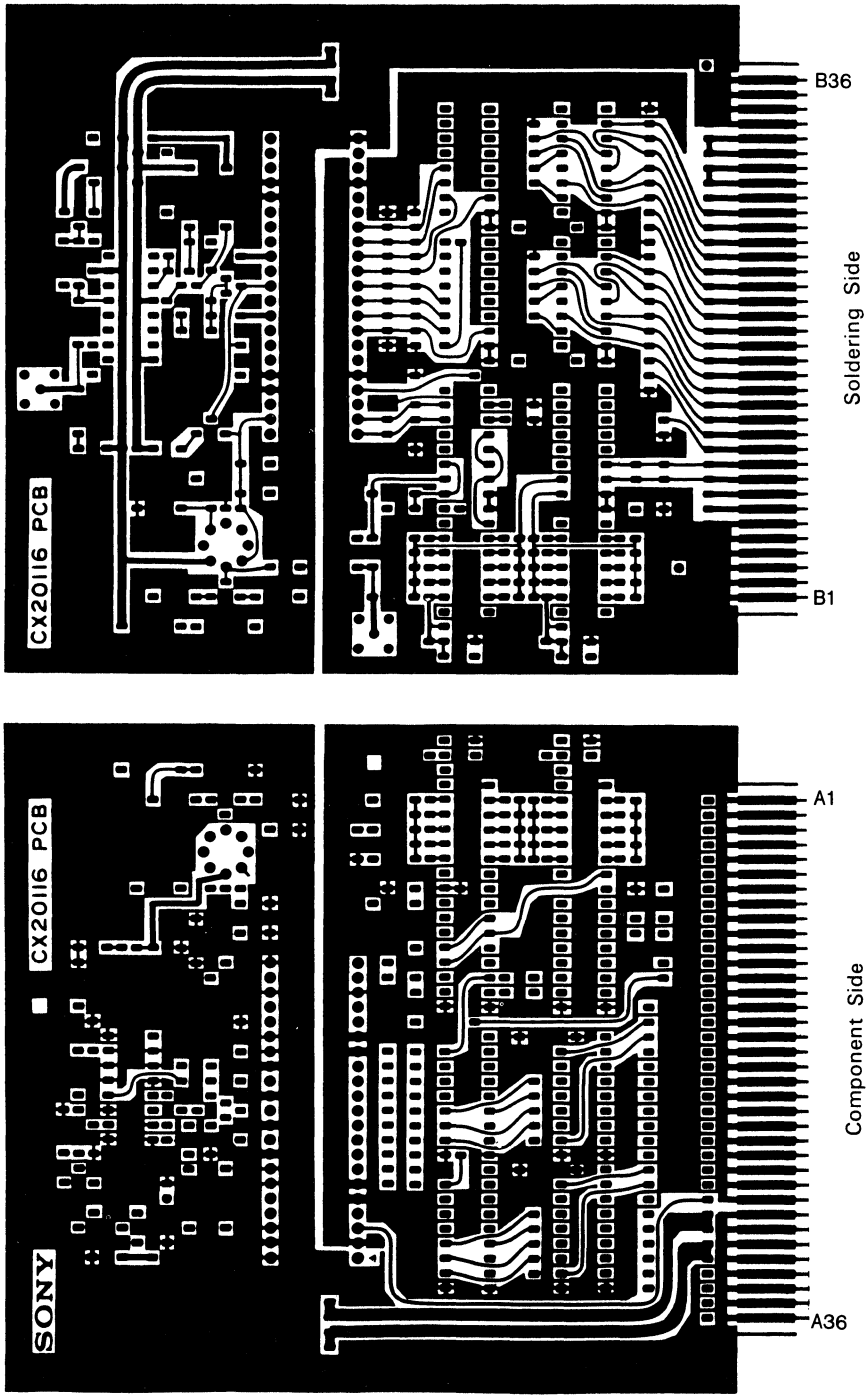
Avoiding the noise effect, GND and V_{EE} are separated in the analog and the digital system respectively. Take care not to happen potential difference more than 50 mV between the both systems.

9-2. Termination of Digital Output

Termination resistance of digital output is not mounted on the PCB. To prevent waveform distortions by reflection, it is recommended to terminate on a PCB that receives the signal.

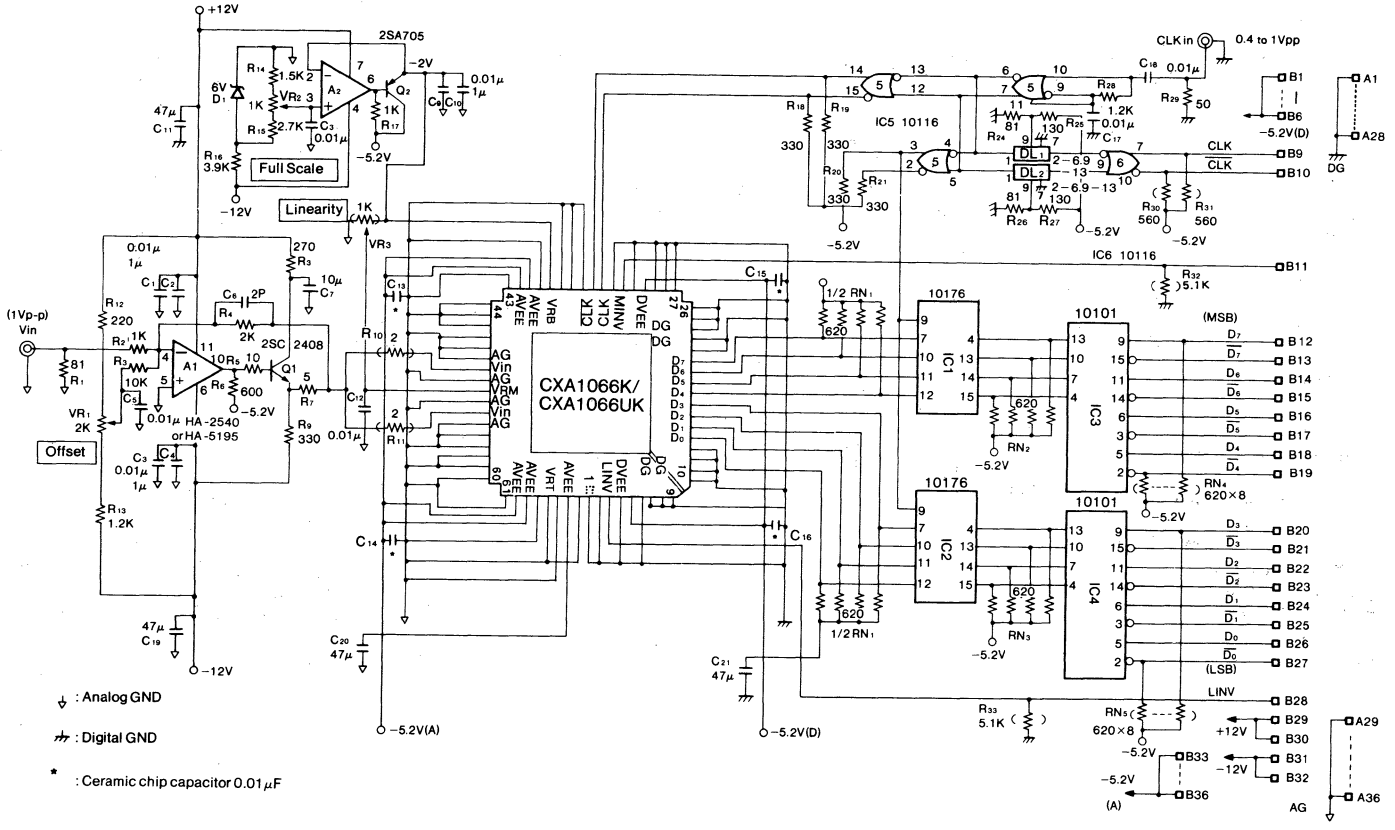
CX20116 PCB/CX20116U PCB



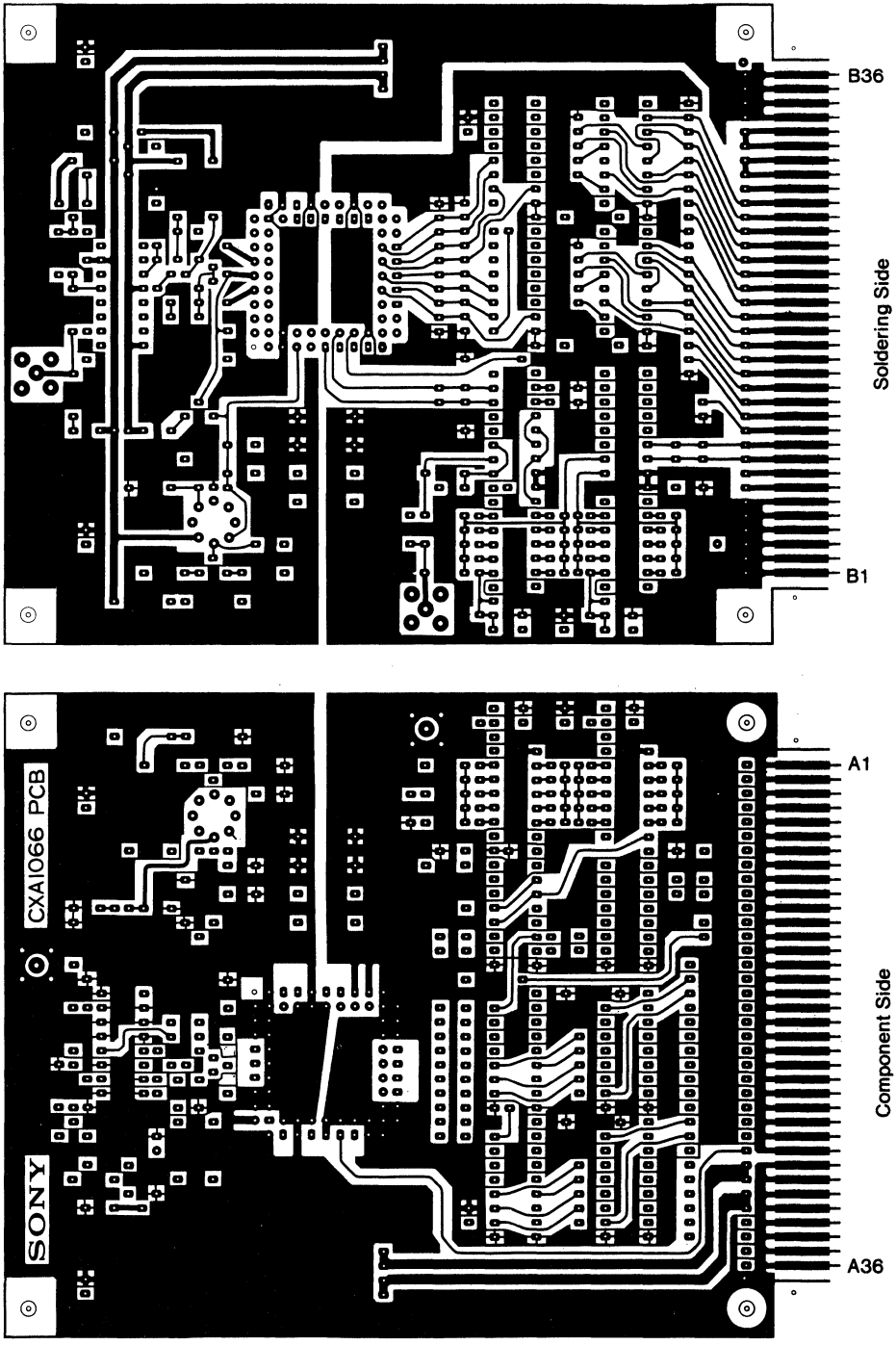


CX20116PCB/CX20116U PCB Pattern

CXA1066K PCB/CXA1066UK PCB



SONY



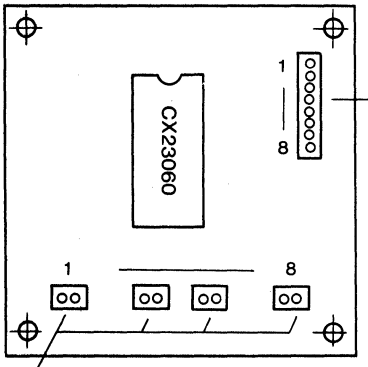
CXA1066K PCB/CXA1066UK PCB Pattern

CX23060 Evaluation Board

Description

The CX23060PCB is an evaluation board for the 10 bit 1 chip A/D-D/A converter CX23060. It incorporates all parts required for the conversion operation and the variable resistors on the board have been preset to a reference value before shipment from the factory, allowing users to evaluate the 10 bit D/A-A/D conversion by supplying the control clock in accordance with a specified timing format.

CX23060PCB I/O Assignment (Top View)



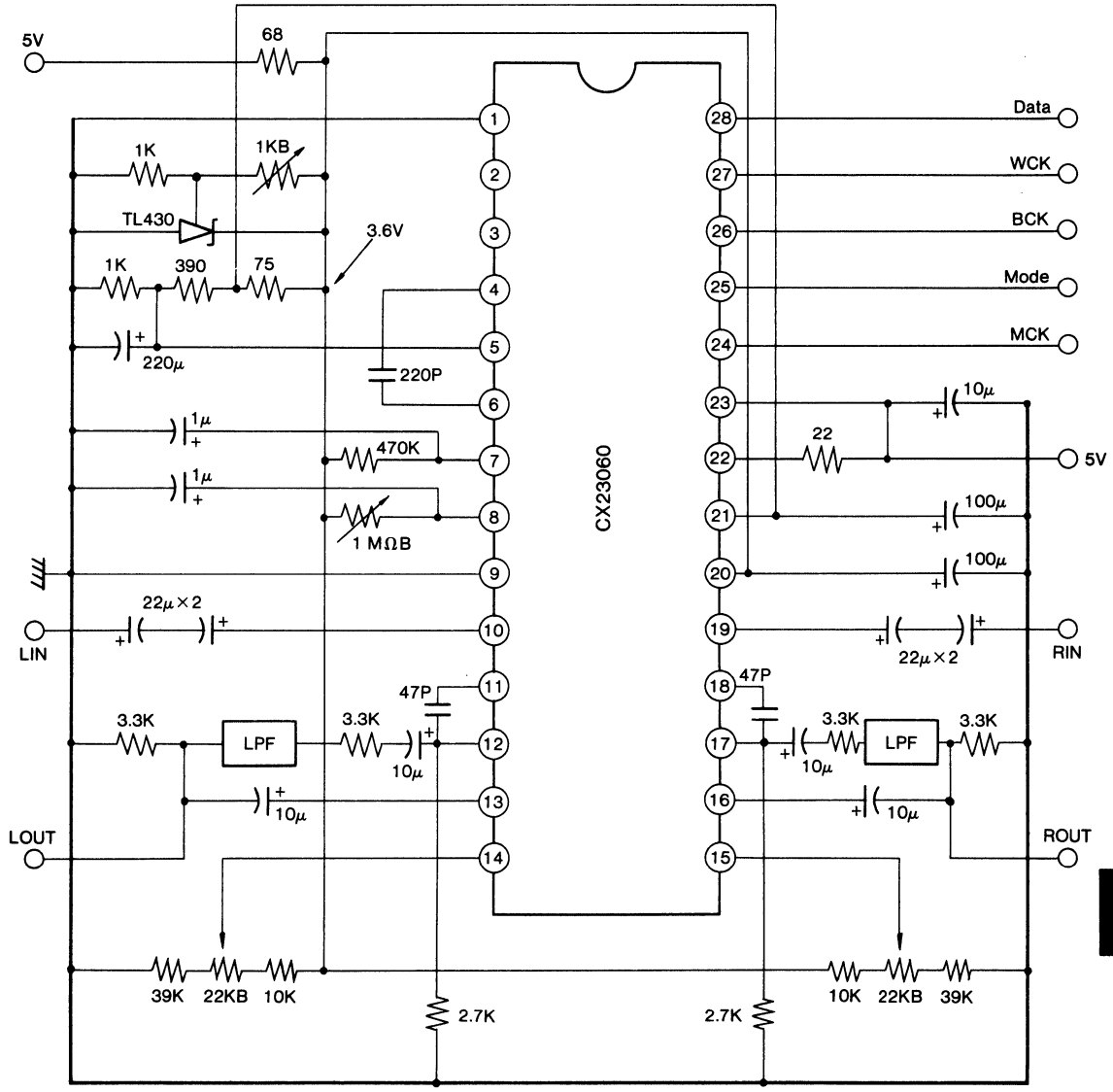
8 pin connector for the input/output of control clock

1. Data I/O
2. Word Clock
3. Bit Clock
4. Mode Select
5. Master Clock
6. NC
7. +5V
8. GND

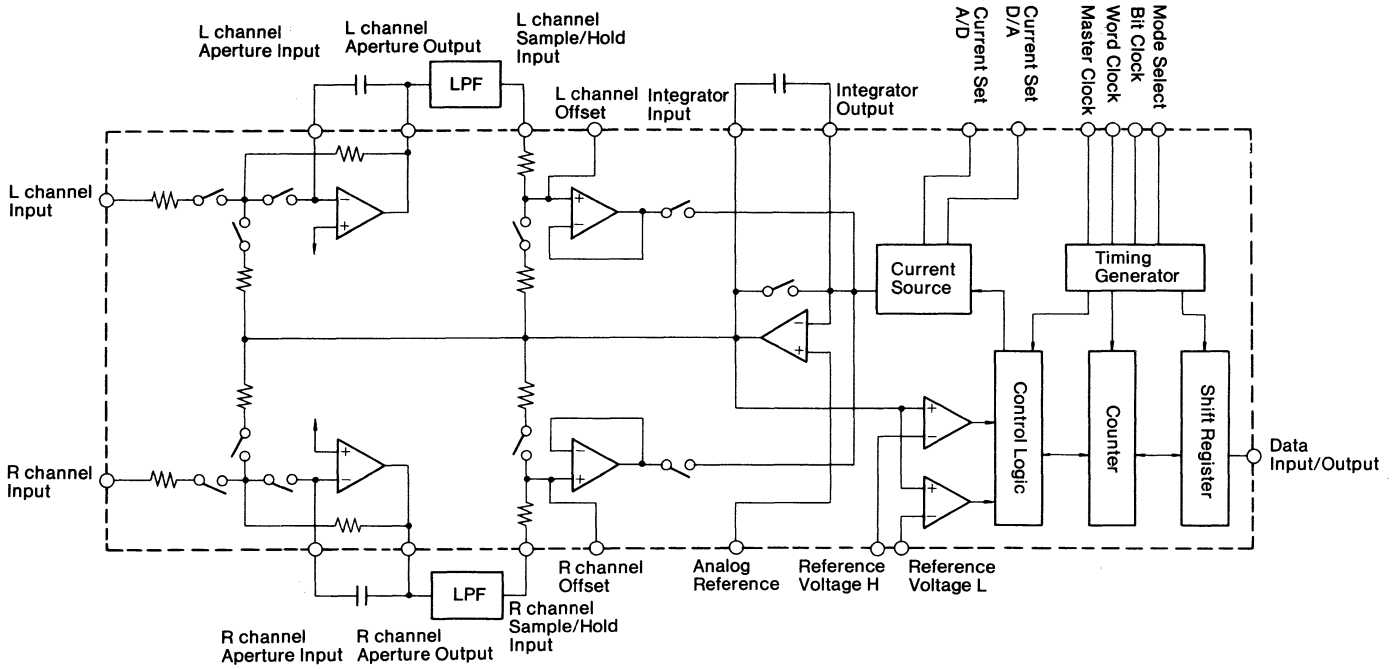
2 pin ×4 connectors for the input/output of analog signal

1. GND
2. Ch.1 Analog Input
3. GND
4. Ch.1 Analog Output
5. GND
6. Ch.2 Analog Output
7. GND
8. Ch.2 Analog Input

CX23060 PCB Circuit

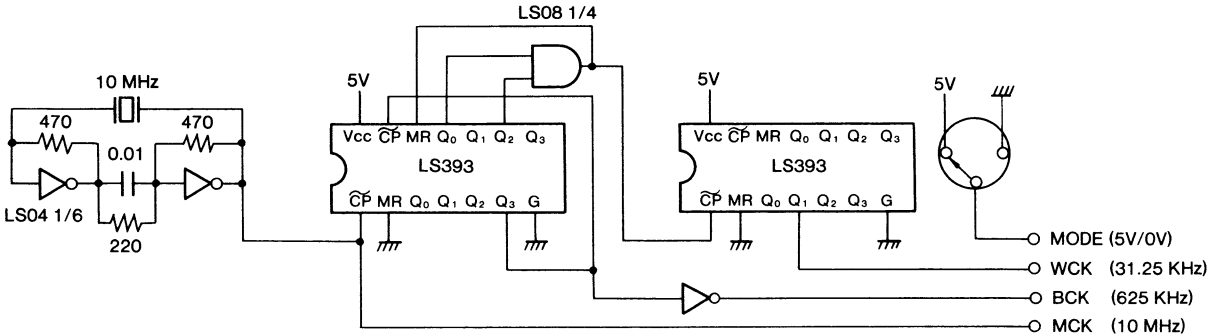


Block Diagram of 10 bit AD/DA CONVERTER



SONY

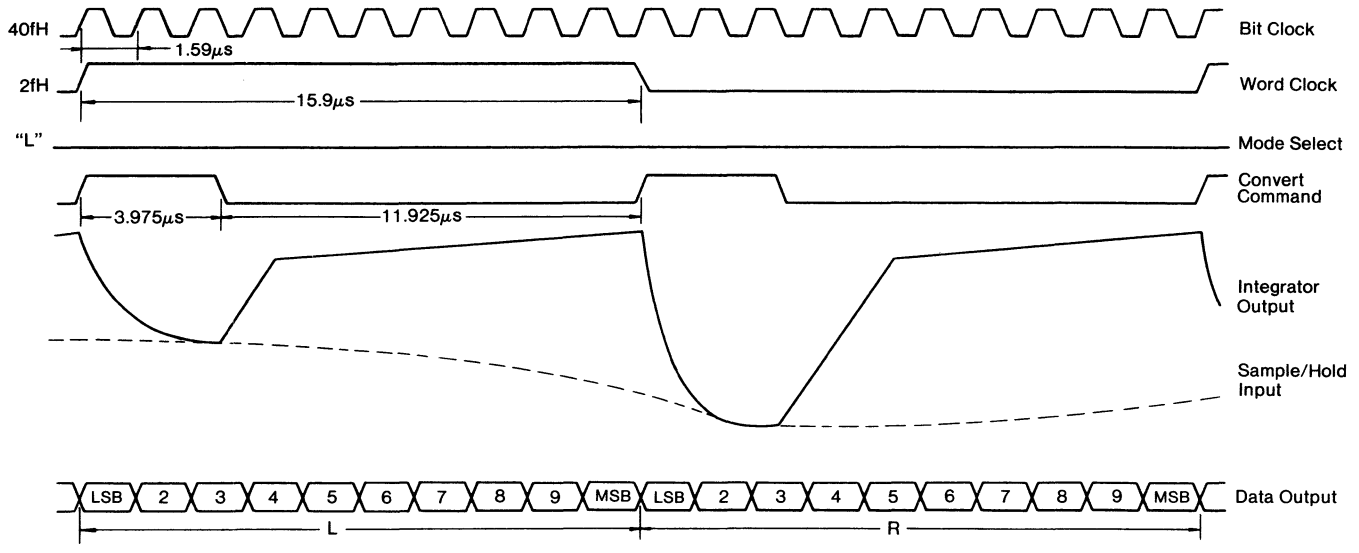
CX23060 Test Signal Generation Circuit



- The CX23060 operates as a D/A converter by setting the MODE signal to 5V and as an A/D converter by setting to 0 V. Its DATA I/O terminal is connected to the internal tri-state buffer allowing external data to be input in the D/A mode and output in the A/D mode. Input/Output data are 10 bit serial data starting with LSB and coded in 2's complement.
- It is desirable for the above test circuit, where 10 MHz is used as MCK, to use an external resistor of 470 kΩ for pin 7. However, to obtain the optimum A/D conversion gain, this external resistor should be 510 kΩ. A/D conversion gain will increase about 5% of full scale level.
- The current set A/D analog input/output level is set to −10 dBs IN/OUT (about 0.245 Vrms). This means full-scale data are obtained when −10 dBs analog input is added to the LIN or RIN in the A/D mode. In the D/A mode, −4 dBs analog output is obtained when full-scale data are added to the DATA I/O terminal. The analog output level becomes −10 dBs a low pass filter 6dB insertion loss.

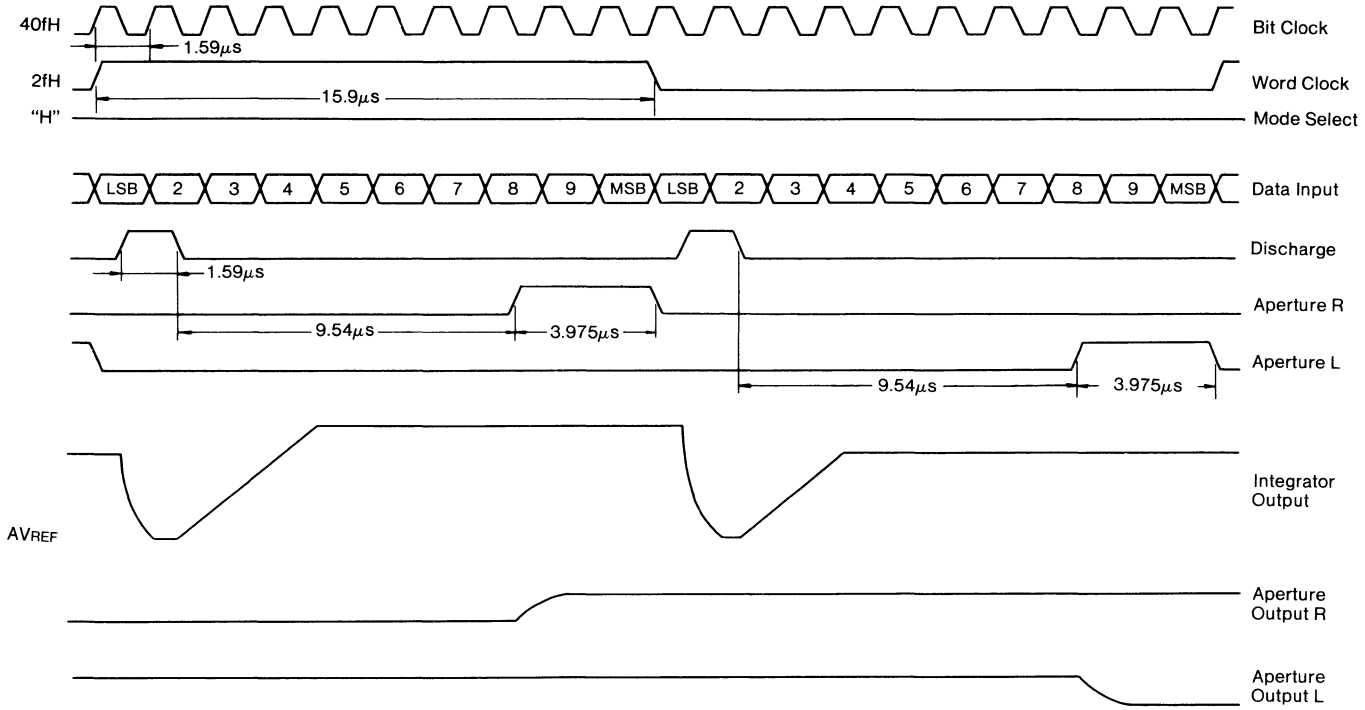
SONY

Timing Format for A/D Conversion



"Convert Command" is generated in the IC when Mode Select is set to "L" state with Bit Clock (625 kHz) and Word Clock (31.25 kHz) input to the CX23060. When this "Convert Command" is at "H" state, sampling the analog input is performed, and the A/D conversion is performed at "L" state. Since the CX23060 has a coarse-fine integrating A/D conversion system, analog signal to the Sample/Hold Input while the Convert Command is at "H" state is sampled, and then the constant current weighted with the inverted analog signal is integrated when the Convert Command becomes at "L" state. By measuring the time integrated by coarse and fine constant currents, preset data on, the upper 6 bits and the lower 4 bits counters are determined. The counter data are set to the shift register when the Convert Command becomes "H" state again, and they are output serially with the LSB data leading in sync with the rising edge of the Bit Clock.

Timing Format for D/A Conversion



Discharge Clock and Aperture Clock are generated in the IC when Mode Select is set to "H" state with Bit Clock (625 kHz) and Word Clock (31.25 kHz) input to the CX23060. The DATA input starting with LSB are loaded into the shift register in sync with the fall edge of the Bit Clock and they are divided into the upper 6 bits MSBs and lower 4 bits LSBs respectively and preseting the upper/lower counters. They start counting when Discharge Clock becomes "L" state and simultaneously the coarse and fine constant currents corresponding to the upper and lower counters are output. When the constant current output is integrated by an integrator, the D/A conversion is performed. When the counters are filled up, the counting will stop and integrating is simultaneously stopped, and the terminal voltage of the integrating capacitor at this time is sampled by the Sample/Hold aperture in the next stage while Aperture Clock is at "H" state and held while at "L" state.

Selection of parts to be used

(1) Use an integrating capacitor of less dielectric absorption (e.g.polystyrene) between Pin 4 and Pin 6.

(2) Adjust the 1 KB semi-fixed resistor so the reference voltage to be generated by the reference voltage IC (TI's TL430 or TL431) becomes 3.6 V.

(3) Tolerance of the three-division resistors, 75Ω, 390Ω and 1 kΩ to give voltage to Pins 5, 20 and 21 is 5% respectively. Approximate values of each terminal voltage is 2.5 V for Pin 5, 3.6 V for Pin 20 and 3.4 V for Pin 21.

(4) Tolerance 1% is recommended for a 470 kΩ resistor (to be connected to Pin 7) which is an integrating current setting resistor giving the A/D conversion gain during the A/D conversion.

Adjustment method

(1) Use the 1MΩB semi-fixed resistor connected to Pin 8 to adjust the playback level during the D/A conversion. (910 K is provided with CX23060PCB). Input digital data corresponding to the sine wave (1 kHz) of full-scale level to Pin 28 and adjust the 1 MΩB so that the D/A output level of Lout and Rout becomes −10 dBs (0.245 Vrms). The maximum level difference between Lout and Rout channel is ±0.3 dB.

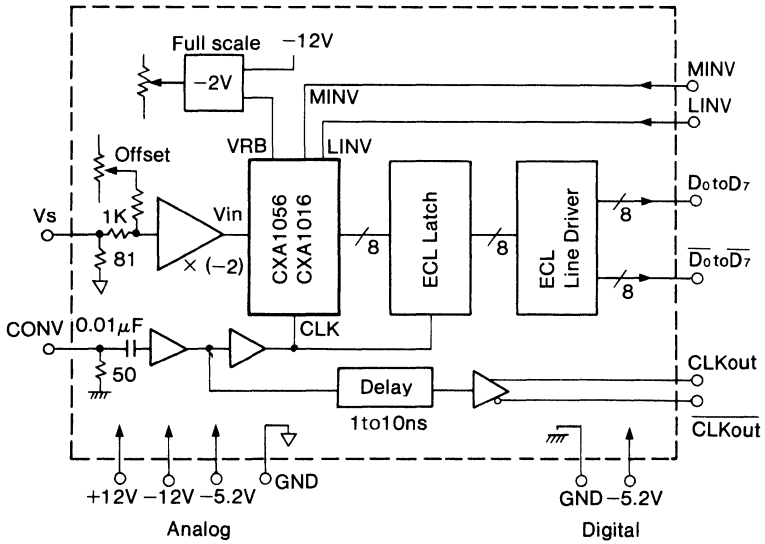
(2) Adjustment of the A/D conversion gain during the A/D conversion is not described, but adjust the D/A output level of the reference DAC (adjusted to become −10 dBs output level described in (1)), when the analog input to be given to Pins 10 and 19 is also set to −10 dBs (0.245 Vrms). In practice, there are no correlation between analog input level of A/D and analog output level of separate D/A, because both A/D and D/A have deviations in conversion gain. So it is effective to change the analog input level of Pins 10 and 19 properly, or to provide a level adjustment amp to Pins 13 and 16.

(3) For the offset adjustment during A/D conversion, adjust the variable resistor (22KB), which is used with the resistors of 10 and 39K. In practice, adjust the 22KB so that the data output of pin 28 becomes "0000000000" when the analog input of LIN and RIN are shorted to the ground. Least significant 2 to 3 bits may be affected by noise.

8 bit 50 MHz/30 MHz A/D Evaluation Board

Description

The CXA1056P PCB/CXA1056K PCB/CXA1056UK PCB/CXA1016P PCB/CXA1016K PCB/CXA1016UK PCB are the evaluation printed circuit boards for 8 bit high speed A/D converter CXA1056P/CXA1056K/CXA1056UK/CXA1016P/CXA1016K/CXA1016UK. On this one board, A/D converter, driver, reference voltage source, latches and ECL line drivers are mounted, and this PCB is designed to achieve the best performance of the A/D converter.



PCB Characteristics

- Analog input band width — 20 MHz (at −3 dB): CXA1056P PCB; 15 MHz (at −3 dB): CXA1016P PCB
- Analog input impedance — 75Ω
- Complementary ECL output
- Clock output (Delay time 0 to 10ns adjustable)

Supply Voltage

• Analog	+12V	80 (Max.)	mA
	−12V	80 (Max.)	mA
	−5.2V	250 (Max.)	mA
• Digital	−5.2V	460 (Max.)	mA

1. Analog Input (Vs)

Item	Min.	Typ.	Max.	Unit
AC Input Voltage Amplitude*		1	1.1	V
Offset Adjustable Range	−0.25	0	1	V
Input Impedance	–	75	–	Ω

* peak to peak

2. Convert Input Signal (CONV)

Item			Min.	Typ.	Max.	Unit
Input Voltage*			0.6		1.0	V
Input Impedance			–	50	–	Ω
DC Level Range			−3		3	V
Pulse Width	CXA1056P PCB CXA1056K PCB CXA1056UK PCB	Tcw 1	14.0			ns
		Tcw 0	4.5			ns
	CXA1016P PCB CXA1016K PCB CXA1016UK PCB	Tcw 1	22.5			ns
		Tcw 0	7.5			ns

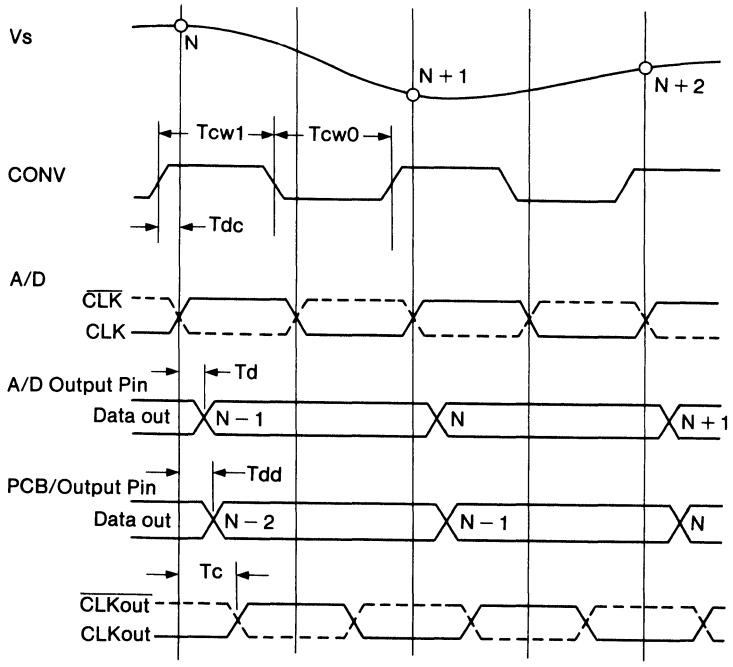
* peak to peak

3. Control Input (MINV, LINV)
ECL 10K compatible

4. Digital Output (D_0 to D_7, $\overline{D_0}$ to $\overline{D_7}$)
ECL 10K compatible, complementary output

5. Clock Output
ECL 10K compatible, complementary output
Delay time adjustable

6. Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
Conversion Delay	Tdc		4.0		ns
Data Delay	Tdd		5.5		ns
Clock Delay Adjustable Range*	Tc	1		10	ns

* Adjustable in 1ns step by taps

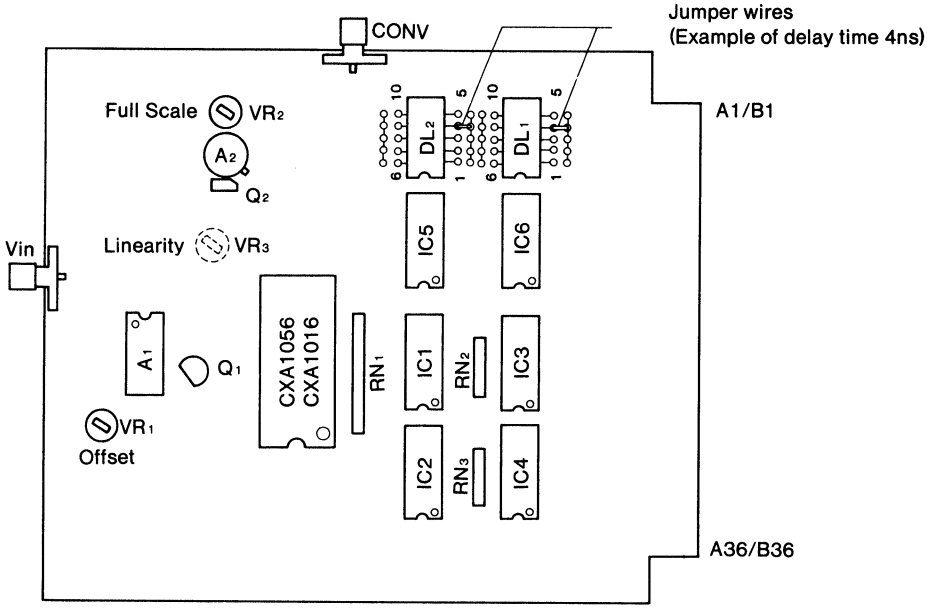
7. Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
	111 . . . 01	100 . . . 01	011 . . . 10	000 . . . 01
	.	.	.	.
	.	.	.	.
	.	.	.	.
Vin	.	.	.	.
	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
	.	.	.	.
	.	.	.	.
	.	.	.	.
	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
−2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1 : V_{IH}
0 : V_{IL}

8. Adjusting Method of Clock Output Delay Time

Clock output delay time can be adjusted by jumper wires position on the PCB.
Tap positions should be changed simultaneously in CLK and $\overline{CLK}$, avoiding the effect of waveform distortion.
Delay time in each taps are 1ns.



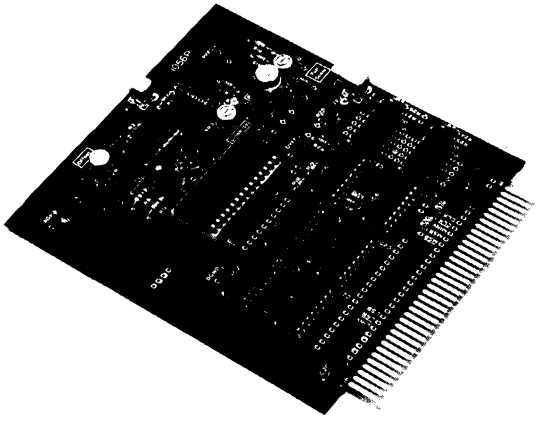
9. Note on Application

9-1. GND, V_{EE}

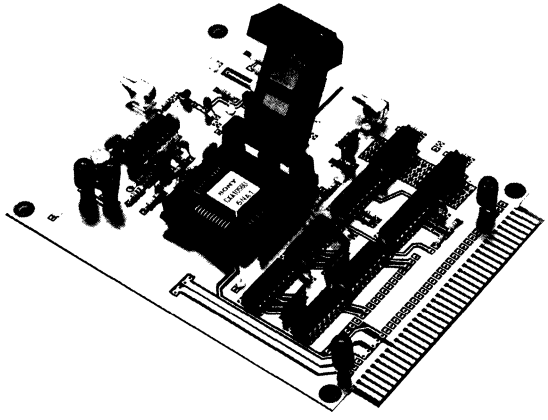
Avoiding the noise effect, GND and V_{EE} are separated in the analog and the digital system respectively. Take care not to happen potential difference more than 50 mV between the both systems.

9-2. Termination of Digital Output

Termination resistance of digital output is not mounted on the PCB. To prevent waveform distortions by reflection, it is recommended to terminate on a PCB that receives the signal.

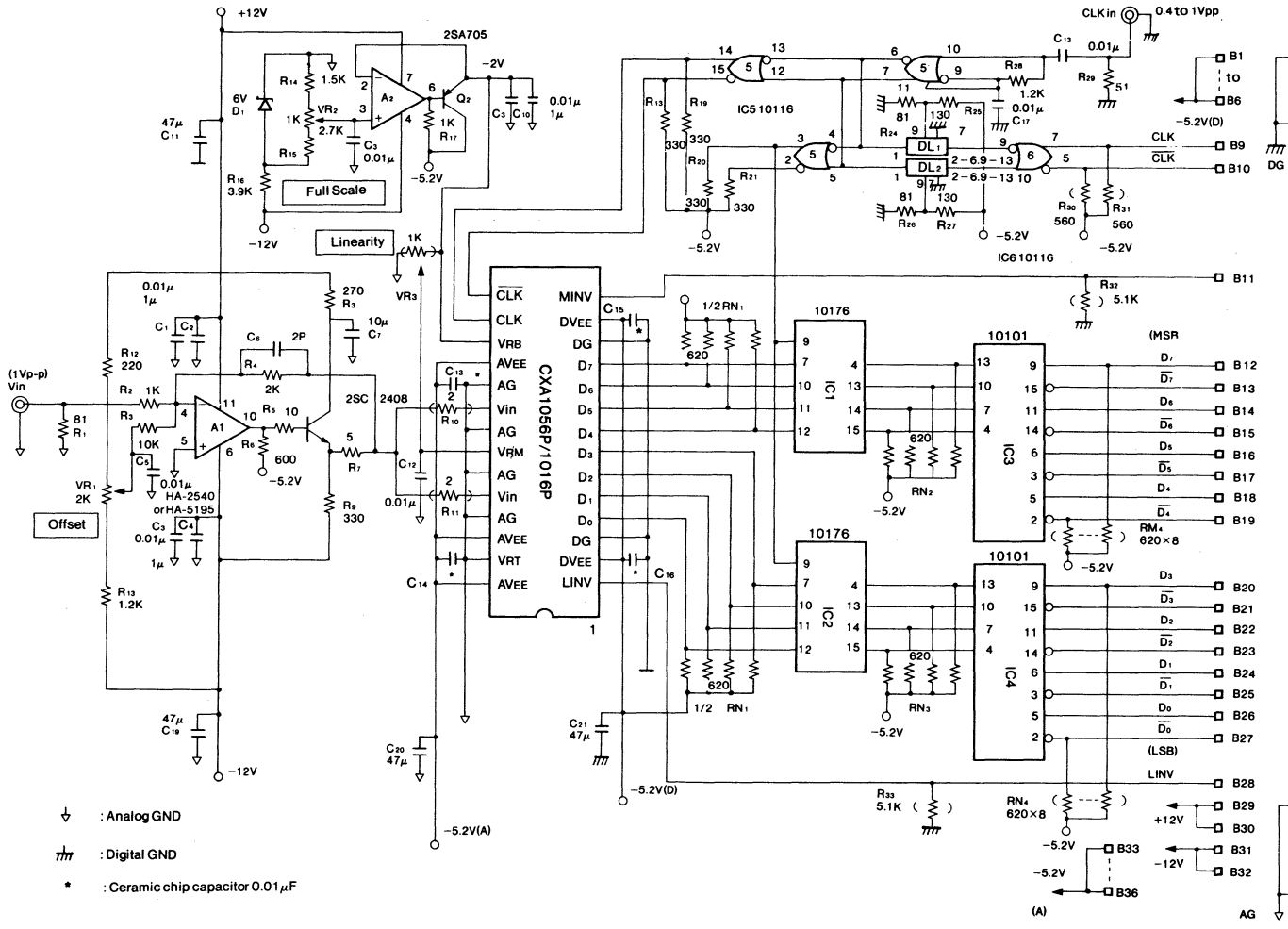


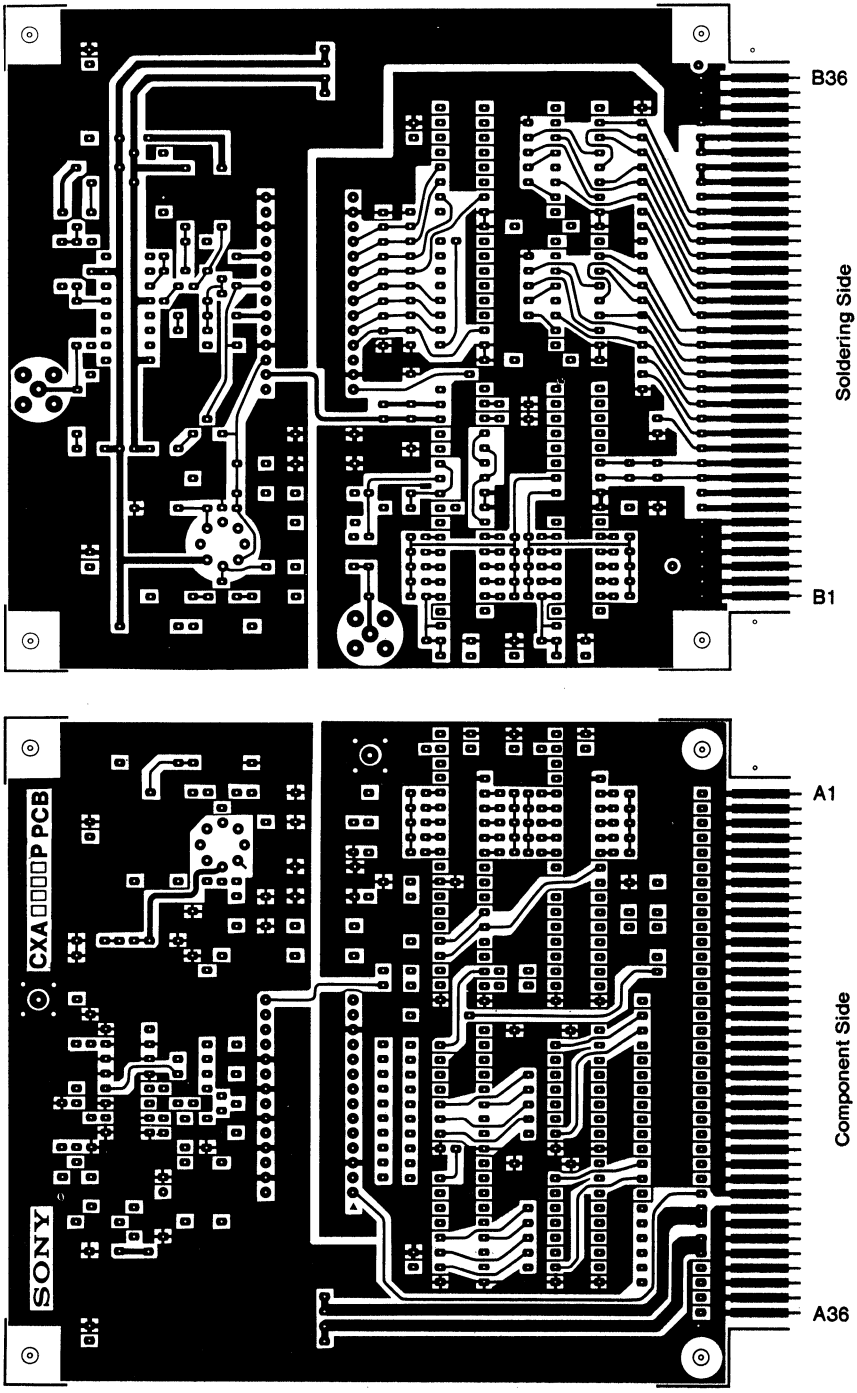
CXA1056P/CXA1016P



CXA1056K PCB/CXA1056UK PCB/CXA1016K PCB/CXA1016UK PCB

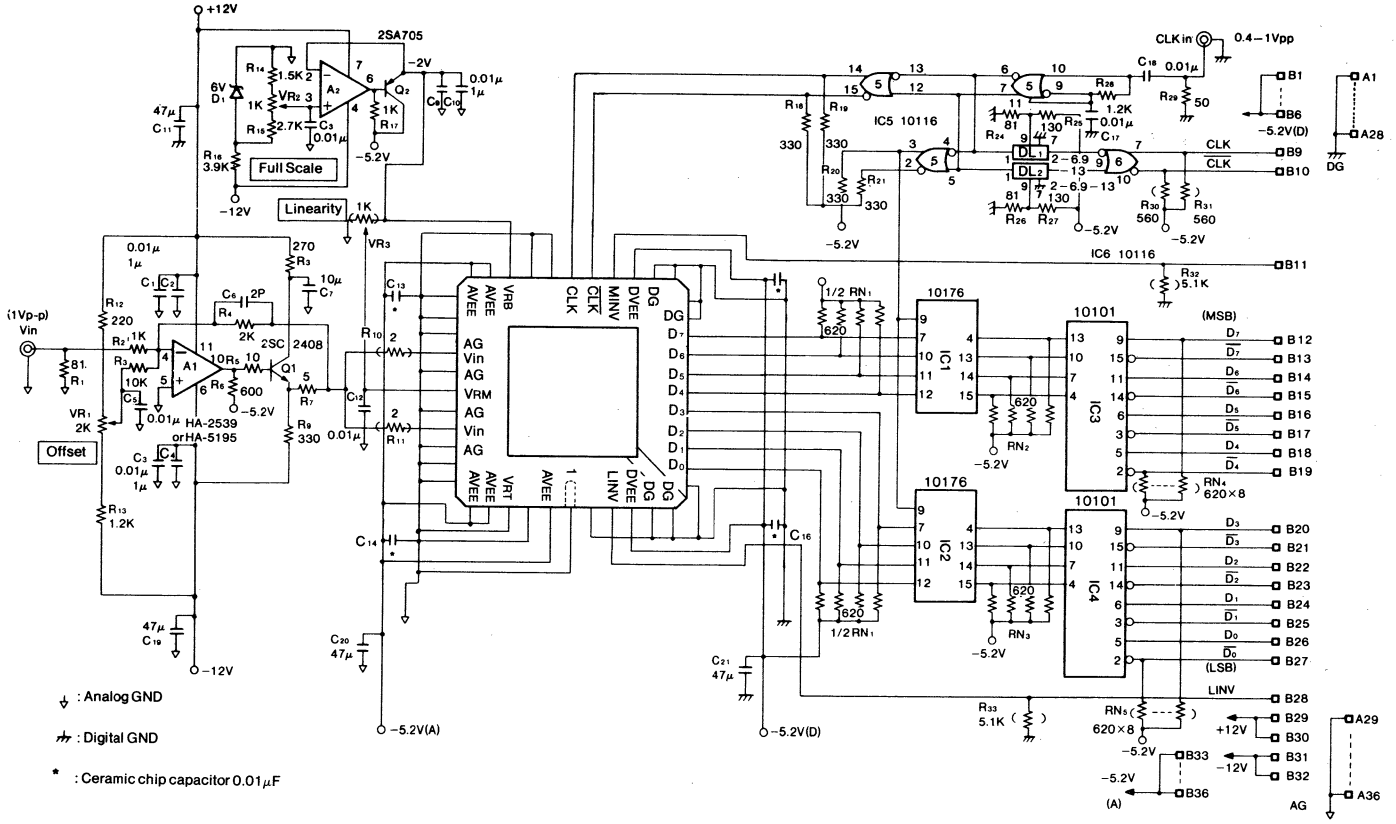
CXA1056P PCB/CXA1016P PCB



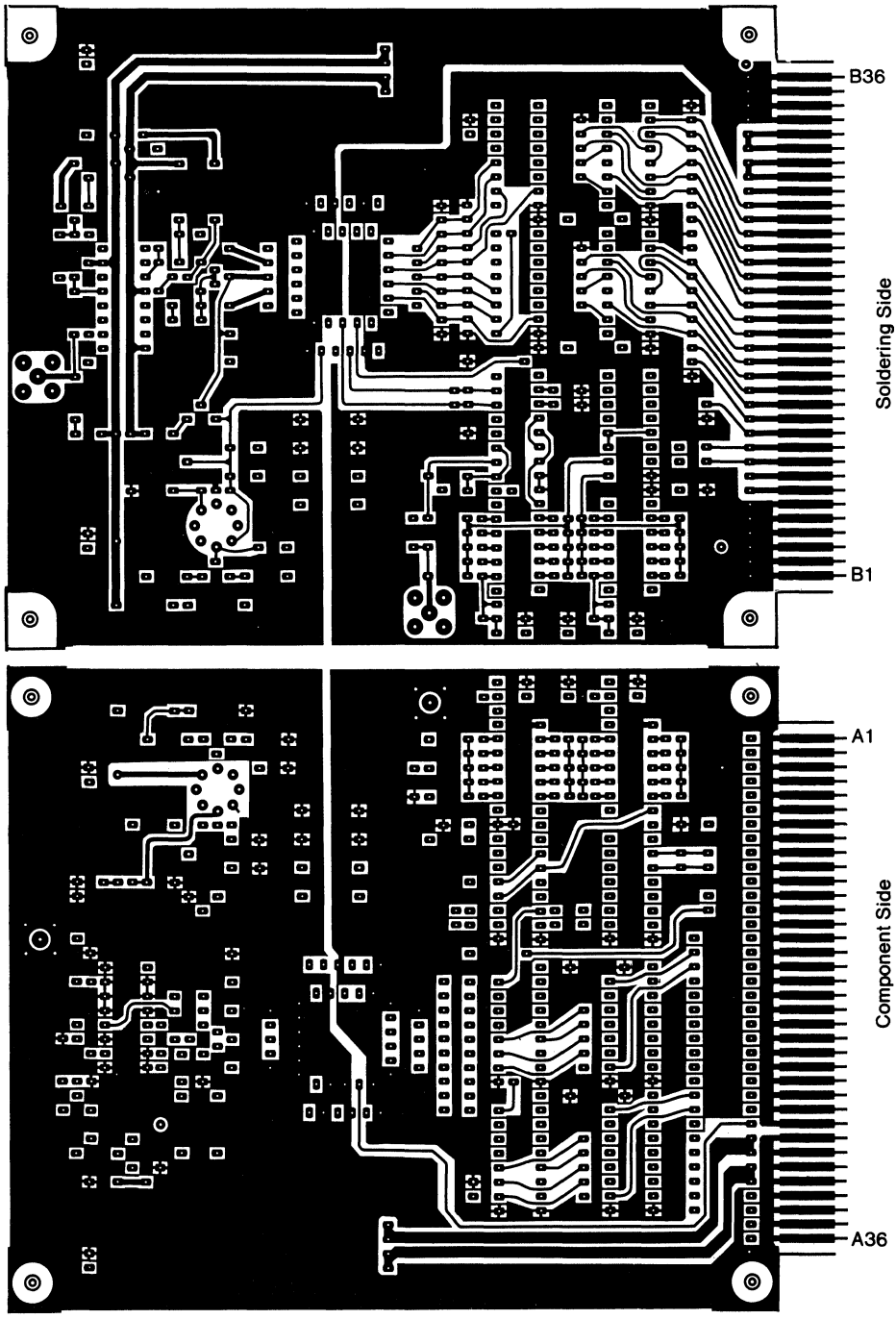


CXA1056P PCB/CXA1016P PCB

CXA1056K PCB/CXA1056UK PCB/CXA1016K PCB/CXA1016UK PCB



SONY



CXA1056K PCB/CXA1056UK PCB/CXA1016K PCB/CXA1016UK PCB Pattern

SONY FCX20220A-1/-2

10/9 Bit 20 MHz Sub-ranging A/D Converter Evaluation Board

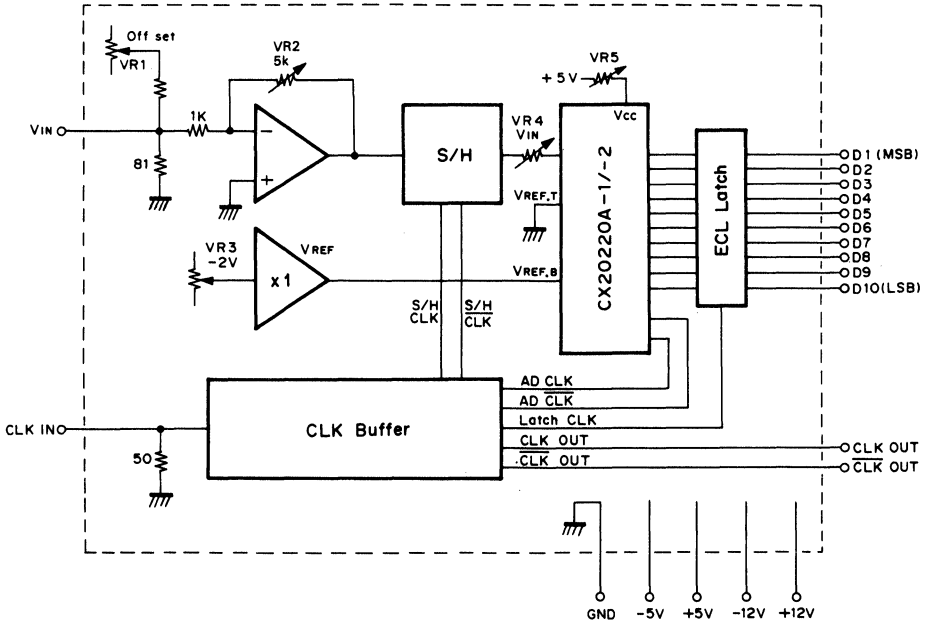
Description

The FCX20220A-1/-2 is an evaluation printed circuit board for the 10/9-bit high speed A/D converter CX20220A-1/-2. On this one board, A/D converter, sample hold, voltage reference and ECL line drivers are mounted, and this PCB is designed to achieve the best performance of the A/D converter. Conversion up to 20 MHz is possible.

Features

• Resolution	10 bit ± 1 LSB (FCX20220A-1) 9 bit ± 1 LSB (FCX20220A-2)
• Maximum conversion rate	20 MHz
• Analog input level	1 Vp-p
• Digital input level	ECL level
• Digital output level	ECL level
• Supply voltage	±12 ±5V
• Analog input band width	10 MHz
• Analog input impedance	75 Ω

Block Diagram



Supply Voltage

Item	Symbol	Min.	Typ.	Max.	Unit
+12V	I_{VCC1}		110	130	mA
−12V	I_{VEE1}		−170	−200	mA
+5V	I_{VCC2}		80	100	mA
−5V	I_{VEE2}		−450	−520	mA

Analog Input

Item	Symbol	Min.	Typ.	Max.	Unit
AC input voltage amplitude	V_{IN}		1	2	V
Offset adjustable range		−2		+2	V
Input impedance	Z_{IN}		75		Ω

Digital Input

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage	$V_{CLK\,H}$	−1.1			V
	$V_{CLK\,L}$			−1.5	V
Input impedance	$Z_{IN\,CLK}$		50		Ω

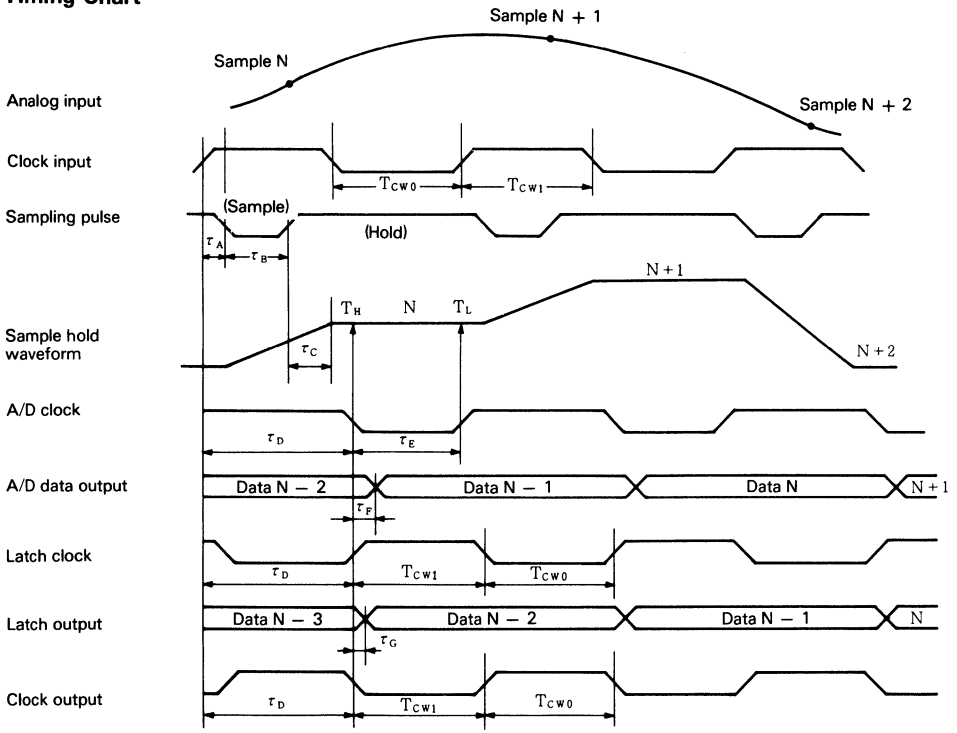
Digital Output (D1 to D10)

ECL 10K compatible (open emitter)

Clock Output

ECL 10K compatible, complementary output (open emitter).

Timing Chart



TH is the timing in which the upper level comparator compares VIN and VREF and latch the result.
TL is the timing in which the lower level comparator compares VIN and VREF and latches the result.

Item	Symbol	Min.	Typ.	Max.	Unit
Input clock pulse width	TPW0	25			ns
	TPW1	25			ns
Sampling pulse delay	τA		2		ns
Sampling pulse width *1	τB		10		ns
Sampling delay	τC		5		ns
A/D clock delay *2	τD		30		ns
A/D clock pulse width *3	τE		22		ns
A/D output data delay	τF		10		ns
Latch output data delay	τG		2		ns
Clock output delay	τD		30		ns

Note) ***1 Adjustable in 2ns step using taps of delay line 1 (DL1).**
***2 Adjustable in 5ns step using taps of delay line 2 (DL2).**
***3 Adjustable in 2ns step using taps of delay line 3 (DL3).**

Output Data Format

A/D converter input (S/H out) is quantized to 10/9 bit under the reference voltage range of $V_{REF.T}$ to $V_{REF.B}$. $V_{REF.T}$ = 0V, $V_{REF.B}$ = −2V are set on this PCB.

(FCX20220A-1)

A/D input signal voltage	Step	Digital output coding MSB 1 2 3 4 5 6 8 9 0 LSB 10
$V_{REF.T}$	0 0 0 0	1 1 1 1 1 1 1 1 1 1
	0 0 0 1	1 1 1 1 1 1 1 1 1 0
	5 1 1	1 0 0 0 0 0 0 0 0 1
	5 1 2	1 0 0 0 0 0 0 0 0 0
	5 1 3	0 1 1 1 1 1 1 1 1 1
	1 0 2 3	0 0 0 0 0 0 0 0 0 1
$V_{REF.B}$	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1: V_{OH}
0: V_{OL}

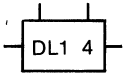
Adjusting Procedure

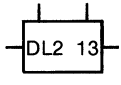
1. V_{REF} (Full Scale) adjustment
   Adjust VR3 (Full Scale), monitoring TP3 ($V_{REF.B}$), for the voltage reading of −2V.
2. Offset adjustment
   Apply sine wave of 1 Vp-p to V_{IN} pin, and monitor TP2 (A/D input). Adjust VR2 (offset) so that the input voltage for the A/D is centered at −1V.
3. Vgain adjustment
   Adjust VR2 (Gain) monitoring TP2 so that the input voltage for the A/D falls into the range of 0V to −2V.
4. V_{CC} adjustment
   Check TP4 (V_{CC}) and adjust VR5 (V_{CC} adj) so that the voltage reading is around +2V.
5. Dumping resistance adjustment
   Adjust VR4 (Damping) so that the A/D performs best result for the electrical characteristics (Linearity, DG, DP and so on).

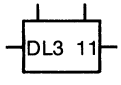
Notes on Application

1. Termination resistance of digital output is not mounted on the PCB. To prevent waveform distortion by reflection, it is recommended to terminate on a PCB that receives the signal.
2. (Adjustment around DL1, DL2 and DL3)
   See Application Circuit on page 6.

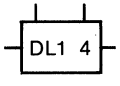
1. In case of 20 MHz, sampling frequency

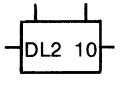


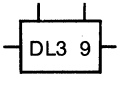




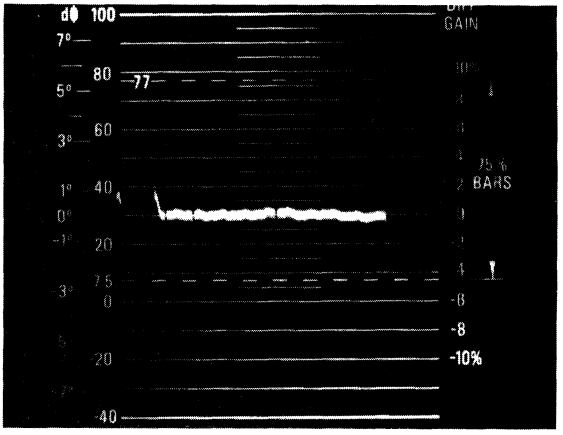
2. In case of 14 MHz, sampling frequency



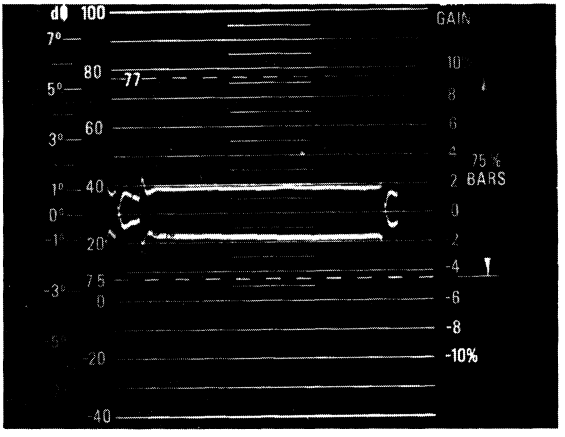




Differential Gain Wave Form

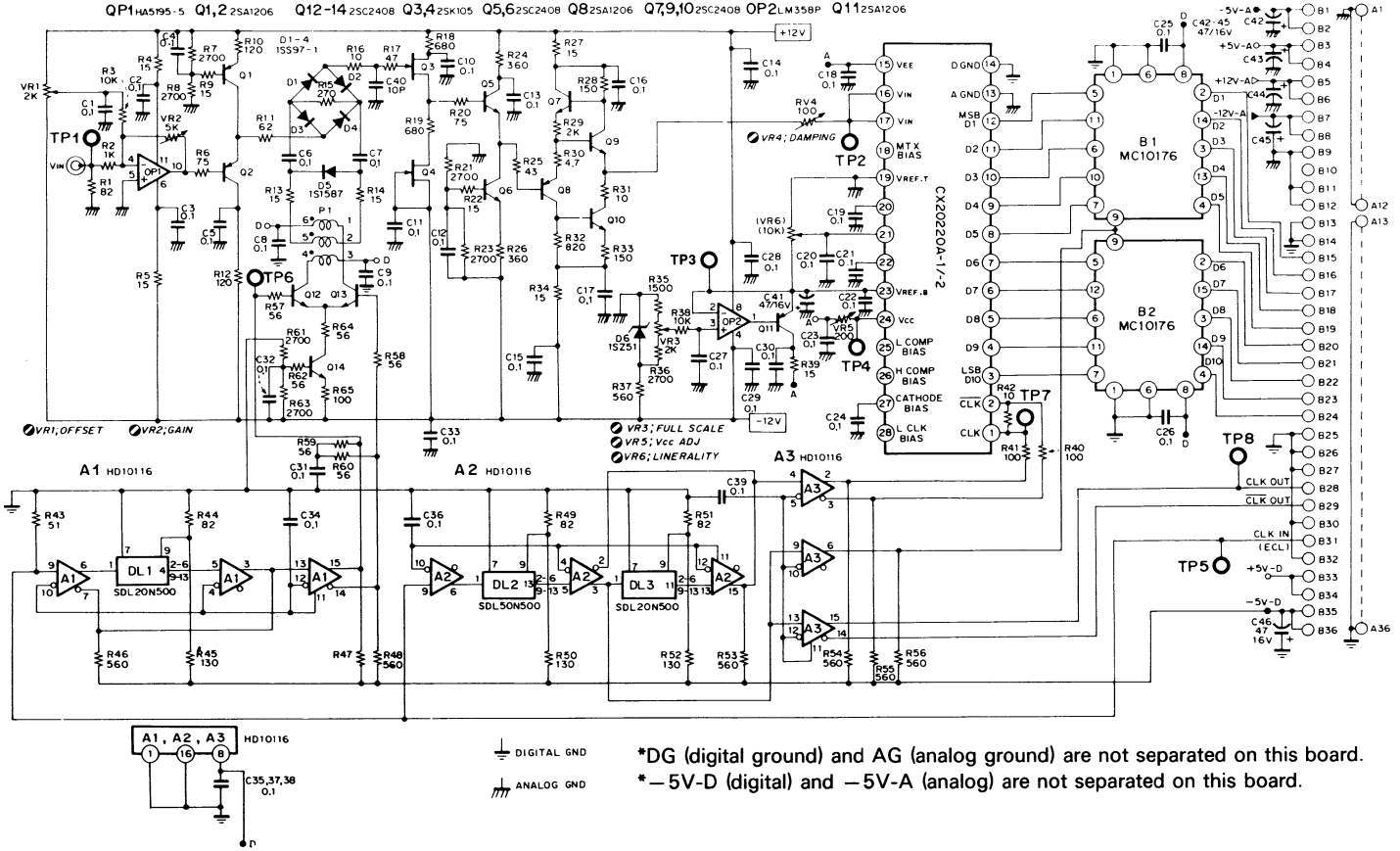


Differential Phase Wave Form



Condition Clock: 20 MHz
Signal: NTSC. 40IRE mod. ramp.

Application Circuit



*DG (digital ground) and AG (analog ground) are not separated on this board.

*—5V-D (digital) and —5V-A (analog) are not separated on this board.

SONY

List of Parts

Resistance		
R1	82Ω	Carbon
R2	1kΩ	〃
R3	10kΩ	〃
R4	15Ω	〃
R5	15Ω	〃
R6	75Ω	〃
R7	2.7kΩ	〃
R8	2.7kΩ	〃
R9	15Ω	〃
R10	120Ω	〃
R11	62Ω	〃
R12	120Ω	〃
R13	15Ω	〃
R14	15Ω	〃
R15	270Ω	〃
R16	10Ω	〃
R17	47Ω	〃
R18	680Ω	〃
R19	680Ω	〃
R20	75Ω	〃
R21	2.7kΩ	〃
R22	15Ω	〃
R23	2.7kΩ	〃
R24	360Ω	〃
R26	360Ω	〃
R27	15Ω	〃
R28	150Ω	〃
R29	2kΩ	〃
R30	4.7Ω	〃
R31	10Ω	〃
R32	820Ω	〃
R33	150Ω	〃
R34	15Ω	〃
R35	1.5kΩ	〃
R36	2.7kΩ	
R37	560Ω	〃
R39	15Ω	〃
R40	100Ω	〃
R41	100Ω	〃
R42	10Ω	〃
R43	51Ω	〃
R44	82Ω	〃
R45	130Ω	〃
R46	560Ω	〃
R47	560Ω	〃
R48	560Ω	〃
R49	82Ω	〃
R50	130Ω	〃
R51	82Ω	〃
R52	130Ω	〃
R53	560Ω	〃
R54	560Ω	〃
R55	560Ω	〃
R56	560Ω	〃
R57	56Ω	〃
R58	56Ω	〃
R59	56Ω	〃
R60	56Ω	〃
R61	2.7kΩ	〃
R62	56Ω	〃
R63	2.7kΩ	〃
R64	56Ω	〃
R65	100Ω	〃

Semi-constant resistance	
VR1	2kΩ
VR2	5kΩ
VR3	2kΩ
VR4	100Ω
VR5	200Ω

Capacitor		
C1	0.1μF	Ceramic
C39	0.1μF	Ceramic
C40	10pF	Ceramic
C41	47μ/16V	Tantalum
C46	47μ/16V	tantalum

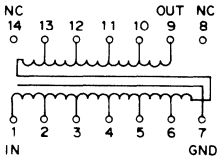
Transistor	
Q1	2SA1206
Q2	2SA1206
Q3	2SK105
Q4	2SK105
Q5	2SC2408
Q6	2SC2408
Q7	2SC2408
Q8	2SA1206
Q9	2SC2408
Q10	2SC2408
Q11	2SA1206
Q12	2SC2408
Q13	2SC2408
Q14	2SC2408

Diode	
D1	1SS97-1
D2	1SS97-1
D3	1SS97-1
D4	1SS97-1
D5	1S1587
D6	1SZ51

IC	
OP1	HA5195-5
OP2	LM358P
A1	HD10116
A2	HD10116
A3	HD10116
B1	MC10176
B2	MC10176

Others		
DL1	SDL20N500	*1
DL2	SDL50N500	*1
DL3	SDL20N500	*1
P1		Pulse transformer *2
TP1		Test pin
TPS		Test pin
	NS-LR020	Connector*3

*1 The following is the delay line connection.



*2 The inductance of the pulse transformer is as folows:

(1)—(6) $7 \pm 3\,\mu H$

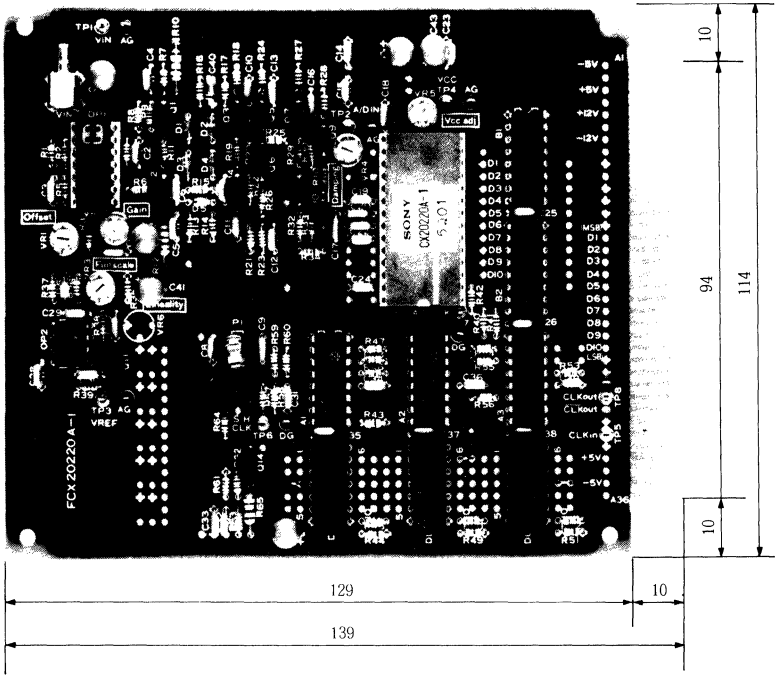
(2)—(5) $7 \pm 3\,\mu H$

(3)—(4) $7 \pm 3\,\mu H$

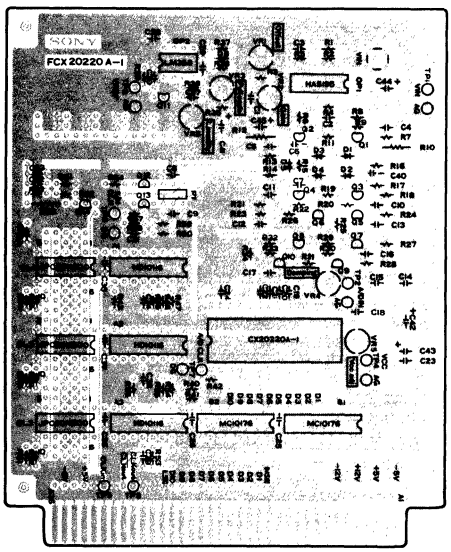
*3 The recommended connectors are NS-P006 and NS-LP017.

*4 The recommended connectors for PCB are KELCORP4610-072-112.

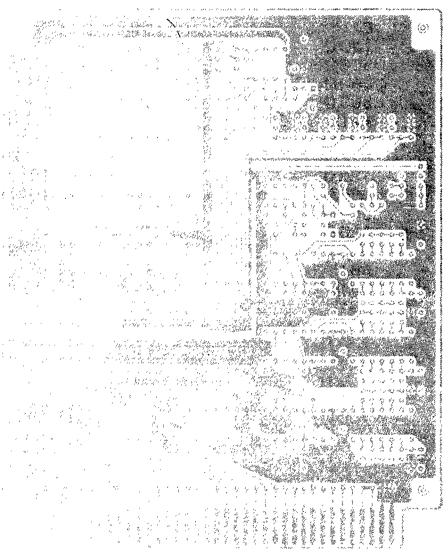
The PCB Pattern and Dimensions (unit: mm, general tolerance ± 0.3 mm)



Component Side



Soldering Side



Application Notes

5) Application Notes

Type	Function	Page
CX20052A	8bit 20MHz Sub-ranging A/D Converter	363
CX20116/U CXA1066K/UK CXA1056P/K/UK CXA1016P/K/UK	8bit High-speed A/D Converter	370

8 bit 20 MHz Sub-ranging A/D Converter CX20052A

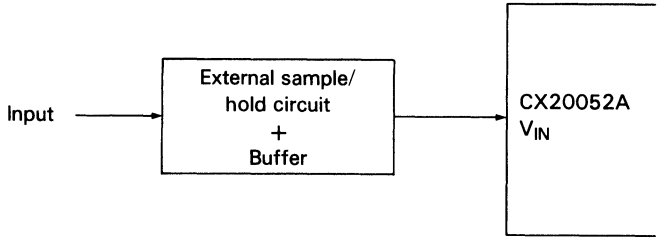
The CX20052A is a serial/parallel A/D converter designed for video signal processing. Because it works on both high-speed clock and 7.8 mV-step analog voltage (at −2.0V full scale) as input signal, care should be taken to the design of a peripheral circuit to obtain a good performance. In addition, attention should also be paid to the relation-between the sampling pulse and the clock of the CX20052A since it requires an external sample/hold circuit.

1. Terminals

1-1. Analog voltage input terminal V_{IN}

Only the signals that have been held in the external sample/hold circuit should be input to the V_{IN}.

The input bias current is about 20μA and the input capacity is about 70pF.

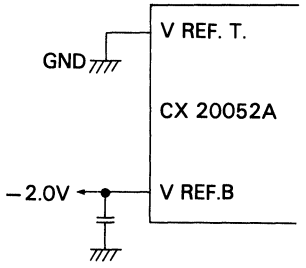


* Details on the sample/hold circuit will be described later.

1-2. Reference voltage terminals $V_{REF.T}$, $V_{REF.B}$

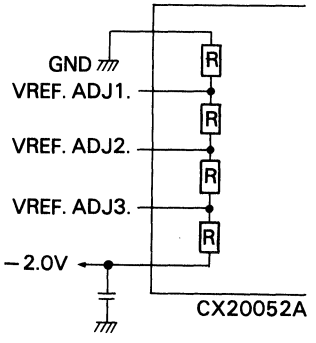
The reference voltage is applied to both the upper and lower comparators by these terminals. The $V_{REF.T}$ and $V_{REF.B}$ should always be connected with the GND and −2.0V, respectively.

There is a resistance value of approximately 50 ohms in between the $V_{REF.T}$ and $V_{REF.B}$. Current of about 40 mA will flow when voltage of −2.0V is applied there. Because the converter's characteristics may deteriorate if the reference voltage is affected by the clock a by-pass capacitor of which capacity is 1μF (tantalum) + 1,000pF (ceramic) should also be used.



1-3. Reference voltage adjustment terminals $V_{REF.ADJ1}$, $V_{REF.ADJ2}$, $V_{REF.ADJ3}$

As shown in the figure below, adjustment terminals are provided in the reference resistance as described in the 1-2 section. They are usually opened, and are connected with the GND or the $V_{REF.B}$ through each resistance if an adjustment is required.



1-4. Grounding terminals ANALOG GND, DIGITAL GND

There should be as much GND space as possible for reduced inductance and resistance when the converter is mounted on a printed circuit board. Because both ANALOG GND and DIGITAL GND are provided, it is sometimes recommended that they should be separately positioned on the surface of the printed circuit board.

1-5. Power voltage terminal V_{EE}

The terminal should be connected with −5.0V. In addition, a by-pass capacitor should also be used for GND.

1-6. Digital output terminals D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8

All the digital output terminals are provided as an open emitter. Load resistance should be selected so that the output current does not exceed the 10 mA (4.3 kohms are equivalent to about 1 mA)
The D_1 denotes MSB, while the D_8 means LSB. The following table shows the relation between analog input voltages and digital output codes.

Step	Input signal voltage (2V, FS)	Digital output code MSB LSB
000	0.0000V	11111111
.	.	.
.	.	.
.	.	.
127	0.9961V	10000000
128	1.0039V	01111111
129	1.0118V	01111110
.	.	.
.	.	.
.	.	.
255	−2.0000V	00000000

1-7. Clock input terminals CLOCK IN, $\overline{\text{CLOCK IN}}$

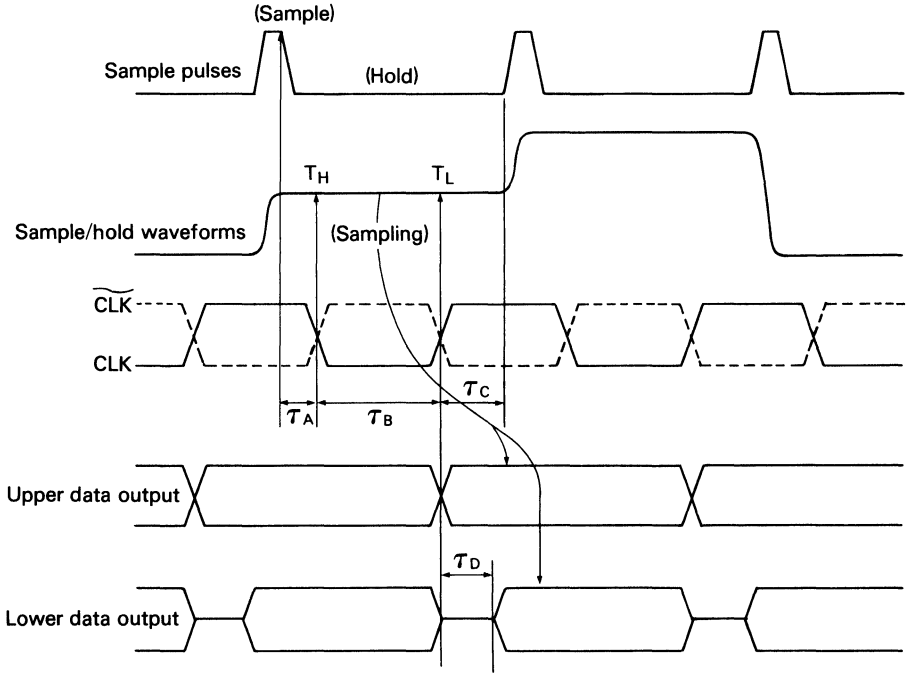
The clock input is complementary and is usually driven by the ECL of the complementary output.

1-8. Other terminals

Although the Pin 1 (H.COMP.BIAS) terminal is not used in the CX20052A, bias voltage keeps generating in the internal circuitry. Therefore, the terminal should not be connected with the GND, power voltage or any other terminals. The Pins 16, 17, and 18 (N.C) are always disconnected.

2. Clock timing

Basically, the CX20052 is a serial/parallel A/D converter so that an external sample/hold circuit is required. Care should therefore be taken to a timing between the clock of the CX20052A and waveforms of the sample/hold circuit.



T_H means a timing where V_{IN} and V_{REF} are compared and latched by the upper comparator, while T_L denotes a timing where V_{IN} and V_{REF} are compared and latched by the lower comparator.

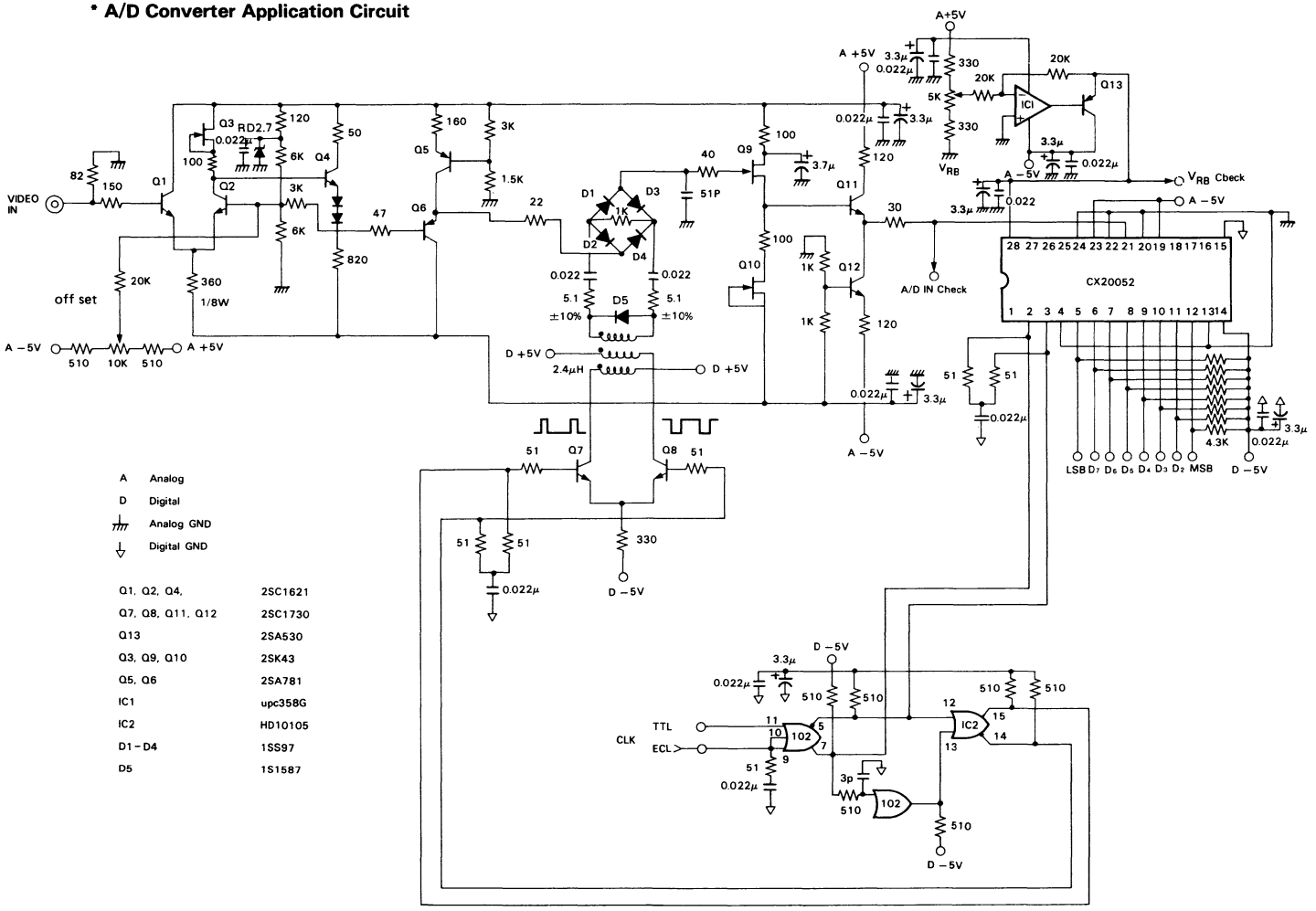
$\tau_A = T_A$ (aperture time + settling time of the sample/hold circuit used)

Although the output data can be picked up as it passes through τD from T_L, it is easier and more accurate to latch it by judging from the rise-up time of the clock. The clock duty should be set at a point where DG and DP are considered optimum.

3. Sample/hold circuit

Refer to the following pages for circuit applications. In addition, a printed circuit board is also available for evaluation, on which a sample/hold IC CXA1008P/1009P and the CX20052A are mounted.

* A/D Converter Application Circuit



8 bit High-Speed A/D Converter

CX20116/CX20116U/CXA1066K/CXA1066UK/
CXA1056P/CXA1056K/CXA1056UK/
CXA1016P/CXA1016K/CXA1016UK

The 8 bit A/Ds for which the flash system has been employed require no externally connected circuits that call for complicated adjustments, and thus make it easy to use. However, because of the high speed conversion they enable, careful design on PCB patterns will be needed to be exercised at relatively high frequencies when operating them.

1. V_{EE}, GND

V_{EE}'s and GND's of the A/Ds have been circuitally separated within the IC into those for the digital circuit and those for the analog circuit. Up to about 50 MHz of clock frequencies the PC board patterns need not be separated, but when employing a higher frequency clock, the separated use of patterns is recommended for noise suppression.

When employing V_{EE}'s separated into digital and analog applications, devices may be destroyed if one end of the V_{EE}'s is turned on with the other left connected to GND via a low impedance for one second or longer.

Both the digital and analog V_{EE} terminals should be bypassed to their respective GNDs with two capacitors each, one 1μF and the other 0.01μF, at a location as close to the terminal as possible. For the 0.01μF, a ceramic chip capacitor is best suited.

2. Timing

The analog input will be sampled at the rising edge of CLK, and digital data is output at the next rising edge of 1CLK cycle later. The delay from the rising edge of CLK to the digital data, Td, is typically 3.5ns, thus it will be possible to latch data with a 10K or 100K series positive edge triggered ECL latch at the same CLK timing and phase as that of the A/Ds.

3. Analog Input (Vin) (See Fig. 1.)

A slew rate of 250V/μs will be required to take full advantage of the wide 40 MHz and above input frequency band of CX20116/CX20116U/CXA1066/CXA1066UK. Although the analog input capacitance has been reduced to be 35pF or vastly smaller than that of the conventional flash type A/D converters, the A/Ds have to be driven with an input amplifier that has a wide frequency band and

sufficient drive capabilities.

For a simple hook-up, a combination of Harris HA-2540, 5195 or equivalent with an appropriate buffer may be used.

As the input impedance of the devices is capacitive, the driving amplifier occasionally falles into an instable condition and oscillates locally. This instability can be prevented with a resistor added between the output terminal of the amplifier and the input terminal of the A/D. For this application, a resistor from 2 to 10 ohms is recommended.

4. Clock Inputs (CLK, $\overline{CLK}$) (See Fig. 2.)

The clock is usually used to be differentially supplied to two terminals, CLK and $\overline{CLK}$, but it may also be used as a single input CLK by adding on a capacitor of 1,000pF between the $\overline{CLK}$ terminal and GND. In this case, the $\overline{CLK}$ terminal will be held at the threshold potential of the ECL (−1.3V).

5. Logic Control Inputs (MINV, LINV) (See Fig. 3.)

The selection of output codes in response to the analog input will be enabled by the logic states assigned to the MINV and LINV terminals, and will facilitate the application of this converter.

The MINV and LINV terminals will be held at a "LOW" level (= "0") when they are in an open state.

Their "High" level may be obtained by a pullup to GND with either a single diode stage or 3.9kΩ.

6. Digital Outputs (D0 to D7) (See Fig. 4.)

Digital outputs require external pull-down resistors. To pull down to V_{EE} = −5.2V, resistors in a range of 500Ω to 1kΩ are recommended.

7. Reference Inputs (V_{RT}, V_{RM}, V_{RS}) (See Fig. 5.)

The V_{RT} to V_{RB} inter-terminal voltage corresponds to the A/Ds input dynamic range. While slight offsets are presented on the V_{RT} and V_{RB} terminal sides, adjustments will be possible within the range of V_{RT} = 0V±0.1V and V_{RB} = −2V±0.2V.

The V_{RB} terminal should be bypassed to GND with 1μF and 0.01μF capacitors in parallel.

When the V_{RM} terminal has been bypassed to GND with a 0.01μF capacitor, high frequency characteristics of the converter will be further stabilized. The V_{RM} terminal may also be utilized as a trimming terminal for more accurate linearity compensation.

8. Blank Terminals

Operations with all blank terminals connected to GND are recommended.

9. Others

The converters are very sensitive to noise level because the comparator hysterisis has been designed extremely small to enable high speed operations. The PC board must be designed carefully to reduce ground plane impedance.

Equivalent input and output circuits

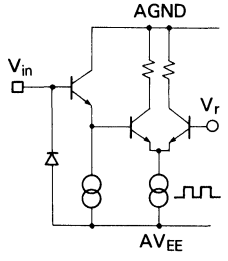


Fig. 1 Analog input

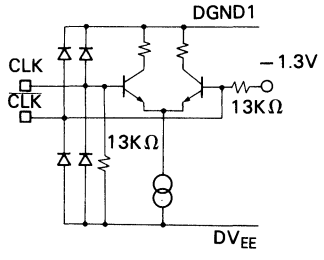


Fig. 2 CLK, $\overline{CLK}$ input

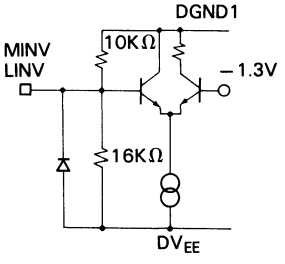


Fig. 3 MINV, LINV input

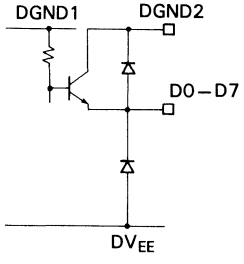


Fig. 4 Digital output

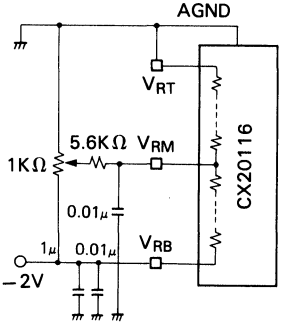


Fig. 5 Linearity compensation

10. Operation (See the block diagram and timing chart.)

1. The reference voltage, which has been obtained by dividing equally the voltage across V_{RT} to V_{RB} into 256 by the reference resistance, is applied to the respective + (positive) input sides of 256 clocked comparators. An analog input is applied to the − (negative) input sides of all the 256 clocked comparators from the V_{IN} terminal.

2. When the state of CLK is in Low, the master (front stage) of the comparator compares the respective reference voltage and the analog input voltage which is ever-changing.
3. When the CLK moves from Low into Hi, each master simultaneously latches the state prior to the CLK transition, and as a result, it provides conditions of "11 ... 1100 .. 0" in sequence from the V_{RT} side to the V_{RB} side.
4. The output of the master is ANDed between the respective adjacent outputs, and "1" stands only when neighboring 2 outputs become "10", and the all other outputs become "0".
5. The result of the AND is latched in the slave latch when CLK moves from Hi into Low. Output of the slave is divided into 4 blocks and each block has 32 clocked comparators, and they are coded into binary codes of 6 bits respectively by the transistor matrix circuit.
6. The 6 bit codes are further coded into 8 bit codes by the transistor matrix circuit after they are respectively latched, and they are then output into the ECL level by the output buffer after being 8 bit latched. The output data is delayed 1 clock from the data sampling point and appears at the output pin.
7. Two polarity inversion inputs such as MINV and LINV are fed externally to the output buffer, and each of them selects output polarity of MSB and LSB's, respectively.

Block Diagram

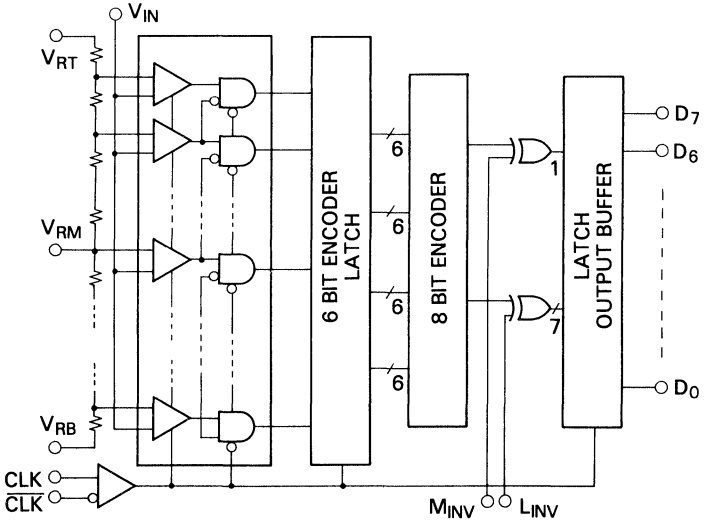


Fig. 6

Timing Chart

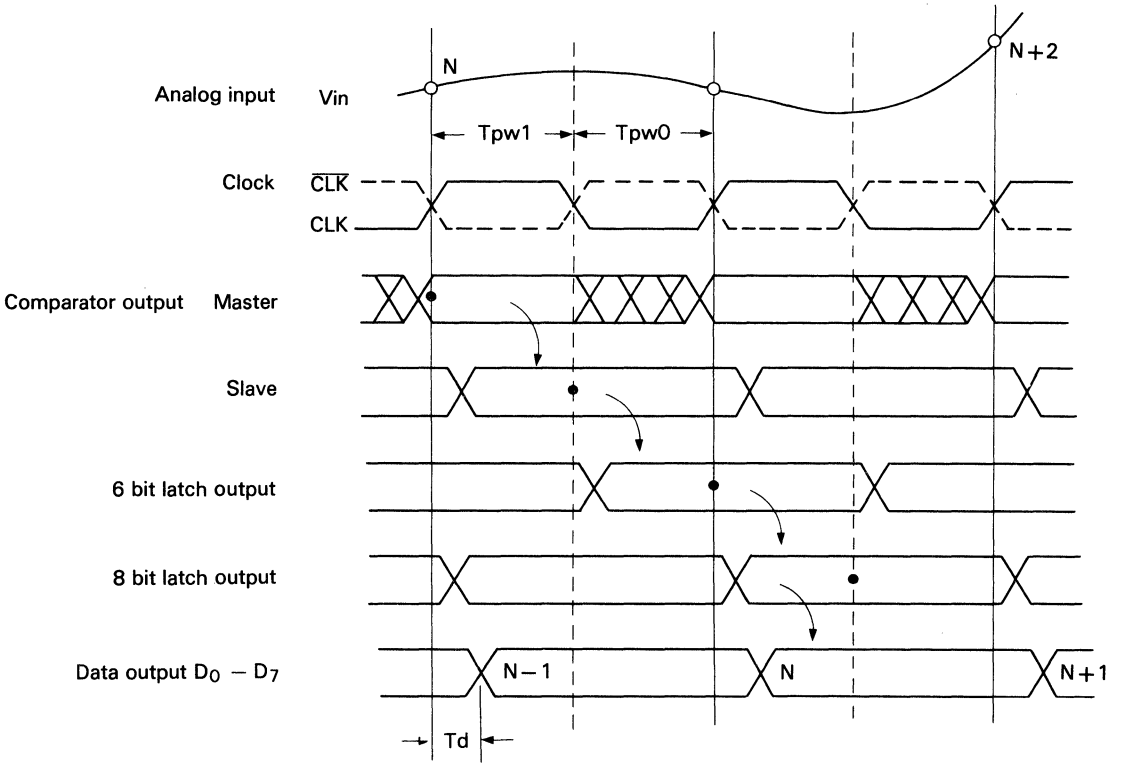


Fig. 7 Dots (●) in the chart demote respective latch timings.

11. Dynamic Performance

Figures 8 to 18 show the dynamic performance of the A/D's. The performance is measured with the aid of the digital signal processing in which the parameters are derived directly from the A/D's digital output data. SNR is defined as RMS Signal to RMS Noise.

Fig. 8(a) shows the signal to noise ratio (SNR) of the CX20116/CX20116U/CXA1066K/CXA1066UK at a sampling rate of 102.4 MHz and 81.92 MHz. The FFT spectrum is shown in Fig. 9 and Fig. 10.

The effective bit is shown in Fig. 8 (b), which is derived from the difference between the measured data and an ideal sine-wave best fitted to the measured data.

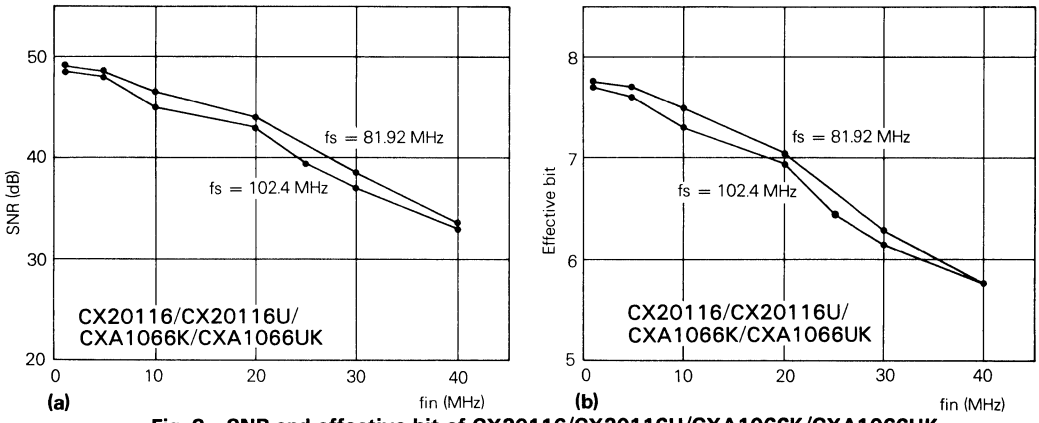


Fig. 8 SNR and effective bit of CX20116/CX20116U/CXA1066K/CXA1066UK

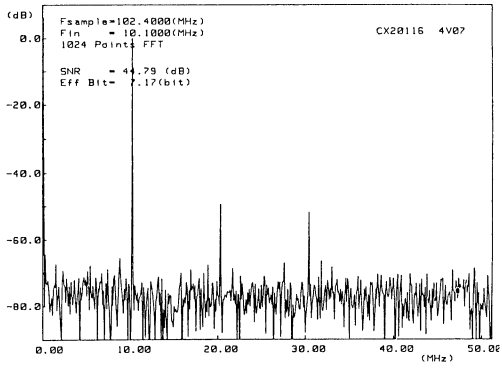


Fig. 9 CX20116/CX20116U Spectrum with the aid of FFT at 102.4 MHz sampling and 10.1 MHz input.

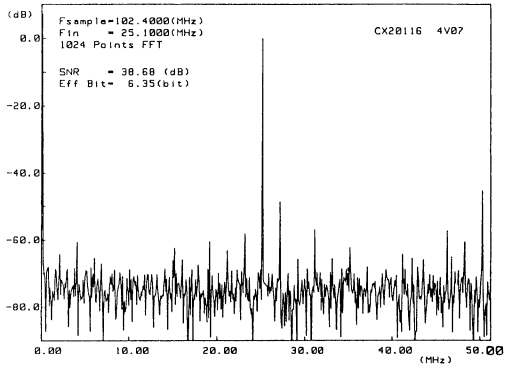


Fig. 10 CX20116/CX20116U Spectrum with the aid of FFT at 102.4 MHz sampling and 25.1 MHz input.

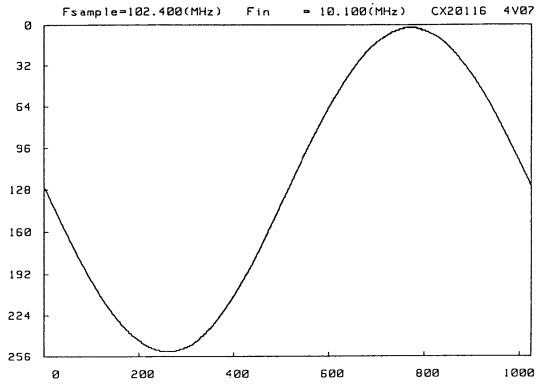


Fig. 11 CX20116/CX20116U
Reconstructed waveform. 102.4 MHz sampling, 10.1 MHz input.

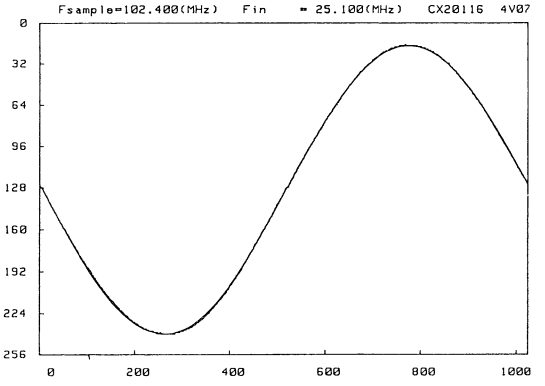


Fig. 12 CX20116/CX20116U
Reconstructed waveform with the best fitted sine wave. 102.4 MHz sampling, 25.1 MHz input.

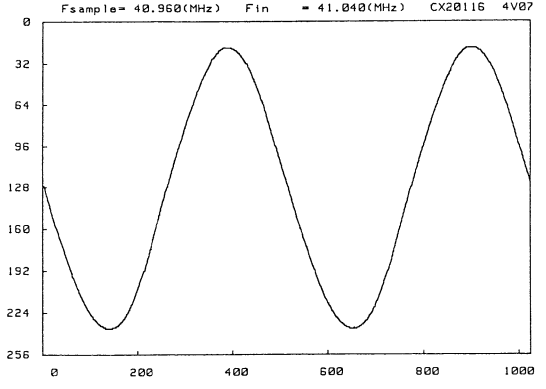


Fig. 13 CX20116/CX20116U
Beat waveform at 41 MHz, $\triangle f = 0.08$ MHz.

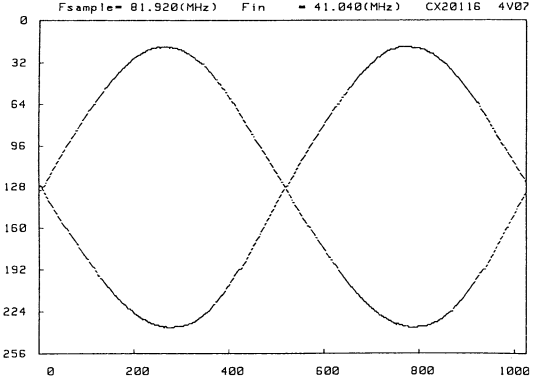


Fig. 14 CX20116/CX20116U
Envelope test waveform at 41.04 MHz input and 81.92 MHz sampling.

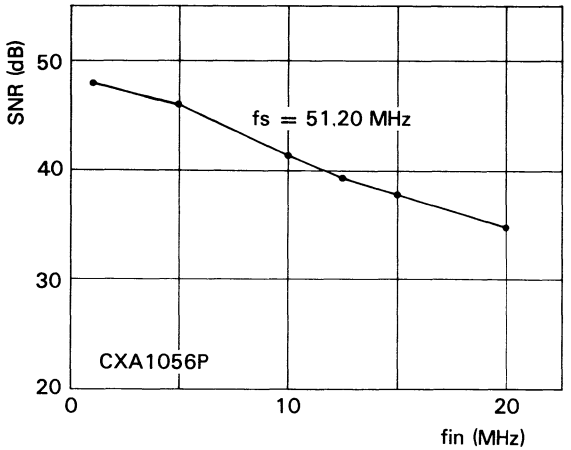


Fig. 15 SNR of CXA1056P/CXA1056K/CXA1056UK

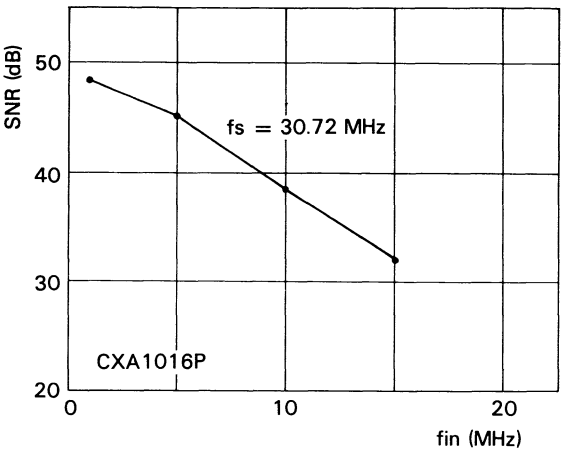


Fig. 16 SNR of CXA1016P/CXA1016K/CXA1016UK

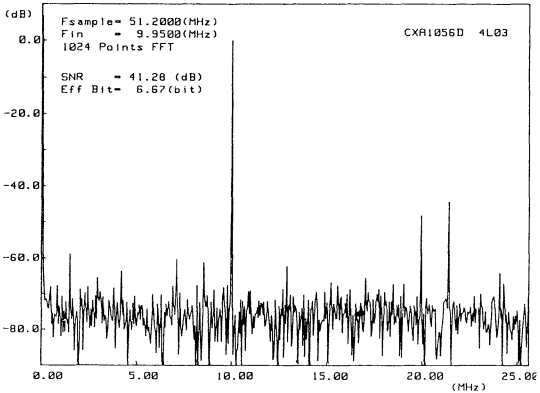


Fig. 17 CXA1056P/CXA1056K/CXA1056UK Spectrum with the aid of FFT at 51.2 MHz sampling and 9.95 MHz input.

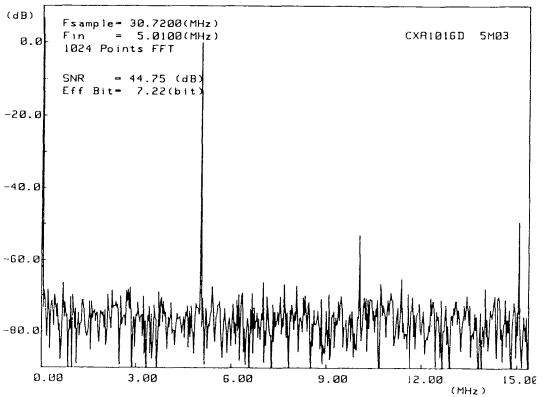


Fig. 18 CXA1016P/CXA1016K/CXA1016UK Spectrum with the aid of FFT at 30.72 MHz sampling and 5.01 MHz input.

Sony SALES OFFICES:

Sites	Address	Phone	Fax
Corporate & Administration Western Office	23430 Hawthorne Blvd. Suite No. 330 Torrance, CA 90505	213-373-9425	213-375-8358
South East Office	3175 A. Northwoods Pkwy Norcross, GA 30071	404-263-9888	404-446-3615
North East Office	57 Wells Avenue Newton MA 02159	617-527-4560	617-244-2518
Central Office	3201 Premier Drive Suite 100 Irving. TX 75063	214-550-5200	214-550-5300

AREA SALES OFFICES:

NORTHEAST AREA: Sony Corporation of America (617) 527-4540
SOUTHEAST AREA: Sony Corporation of America (404) 263-9888
CENTRAL AREA: Sony Corporation of America (214) 550-5200
WESTERN AREA: Sony Corporation of America (213) 373-9425

REPRESENTATIVE OFFICES:

ALABAMA: Interep Assoc., Inc., (205) 478-1036, (205) 533-1730
ARIZONA: Shefler-Kahn, (602) 257-9015
ARKANSAS: B.P. Sales, (918) 744-9964
CALIFORNIA: (San Diego and Imperial) Addem Sales, (619) 729-9216; (Southern Ca., excluding San Diego) Varigon, Inc., (714) 855-0233, (Northern Ca. Counties: Monterey/kings/Tulare/Inyo) Brooks Technical Group, (415) 960-3880
COLORADO: Electrodyne, (303) 695-8903
CONNECTICUT: New England Technical Sales, (203) 237-8827
DELAWARE: Beacon North, Inc., (800) 336-3747
DISTRICT OF COLUMBIA: Beacon North, Inc., (703) 478-2480
FLORIDA: Donato & Assoc., (305) 352-0727
GEORGIA: Interep Assoc., Inc., (404) 449-8680
HAWAII: Brooks Technical Group, (415) 960-3880
IDAHO: Electrodyne, (801) 486-3801
ILLINOIS: (Northern) Micro-Tex, Inc., (312) 382-3001; (Southern) Kebco, (314) 576-4111
INDIANA: Giesting & Assoc., (317) 844-5222
IOWA: J.R. Sales, (319) 393-2232
KANSAS: Kebco, (913) 541-8431 or (316) 733-1301
KENTUCKY: Giesting & Assoc., (513) 385-1105
LOUISIANA: B.P. Sales, (214) 234-8438
MAINE: New England Technical Sales, (617) 272-0434
MARYLAND: Beacon North, Inc., (800) 336-3747
MASSACHUSETTS: New England Technical Sales, (617) 272-0434
MICHIGAN: Giesting & Assoc., (313) 478-8106
MINNESOTA: High-Tech Sales, (612) 944-7274
MISSISSIPPI: Interep Assoc., Inc., (205) 533-1730
MISSOURI: Kebco, (314) 576-4111
MONTANA: Electrodyne, (801) 486-3801
NEBRASKA: J.R. Sales, (319) 393-2232
NEVADA: (Clark County) Shefler-Kahn, (602) 257-9015, Brooks Technical Group, (916) 477-8096
NEW HAMPSHIRE: New England Technical Sales, (617) 272-0434
NEW JERSEY: S.J. Assoc., Inc. (718) 291-3232, (609) 866-1234
NEW MEXICO: Shefler-Kahn, (505) 345-3591
NEW YORK: (Manhattan) S.J. Assoc., Inc., (718) 291-3232 (Upstate) Advance Comp. Corp., (315) 699-2671
NORTH CAROLINA: Naylor Assoc., Inc., (919) 544-6630
NORTH DAKOTA: High-Tech Sales, (612) 944-7274

OHIO: Giesting & Assoc., (513) 385-1105, (216) 261-9705, or (513) 433-5832
OKLAHOMA: B. P. Sales, (918) 744-9964
OREGON: Vantage Corp., (503) 620-3280
PENNSYLVANIA: (East) S.J. Assoc., Inc., (609) 866-1234; (West) Giesting & Assoc., (513) 385-1105
RHODE ISLAND: New England Technical Sales, (617) 272-0434
SOUTH CAROLINA: Naylor Assoc., Inc., (919) 544-6630
SOUTH DAKOTA: High-Hech Sales, (612) 944-7274
TENNESSEE: Interep Assoc., Inc., (615) 639-3491
TEXAS: B.P. Sales, (214) 234-8438, (713) 531-4144, or (512) 346-9186; (El Paso County) Shefler-Kahn (505) 345-3591
UTAH: Electrodyne, (801) 486-3801
VERMONT: New England Technical Sales, (617) 272-0434
VIRGINIA: Beacon North, Inc., (703) 478-2480, (804) 239-8486
WASHINGTON: Vantage Corp., (206) 455-3460
WEST VIRGINIA: Giesting & Assoc., (513) 385-1105
WISCONSIN: (Lower) Micro-Tex, Inc., (414) 542-5352; (West Wisconsin Counties: Polk/Barron/Dunn/St. Croix/Pierce/Pepin/Chippewa, Eua Claire) High-Tech Sales, (612) 944-7274
WYOMING: Electrodyne, (801) 486-3801

DISTRIBUTOR OFFICES:

ALABAMA: Huntsville ·····Hammond Electronics, (205) 830-4764
Huntsville ·····Marshall Industries, (205) 881-9235
ARIZONA: Phoenix ·····Marshall Industries, (602) 968-6181
Scottsdale·····Western Micro, (602) 948-4240
Tempe ·····Insight, (602) 829-1800
CALIFORNIA: Chatsworth ·····Diplomat Electronics, (818) 700-8700
Irvine ·····Marshall Industries, (714) 458-5399
Cupertino ·····Western Micro, (408) 725-1660
Los Angeles ···Marshall Industries, (818) 407-0101
Northridge·····Western Micro, (818) 700-9922, (800) 538-3401
Orange ·····Ryno Electronics, (714) 637-0200
Sacramento ·····Marshall Industries, (916) 635-9700
San Diego ·····Insight, (619) 587-0471
San Diego ·····Marshall Industries, (619) 578-9600
San Diego ·····Ryno Electronics, (619) 453-8430
San Francisco···Marshall Industries, (408) 943-4600
Sunnyvale·····Diplomat Electronics, (408) 737-0204
COLORADO: Denver ·····Marshall Industries, (303) 427-1818
CONNECTICUT: Danbury·····Diplomat Electronics, (203) 797-9674
Wallingford ·····Marshall Industries, (203) 265-3822
FLORIDA: Clearwater·····Diplomat Electronics, (813) 443-4514
Ft. Lauderdale ···Diplomat Electronics, (305) 974-8700
Ft. Lauderdale ···Hammond Electronics, (305) 973-7103
Ft. Lauderdale ···Marshall Industries, (305) 928-0661
Ft. Lauderdale ···Reptron, (305) 979-8227
Orlando ·····Hammond Electronics, (305) 841-1010
Orlando ·····Marshall Industries, (305) 841-1878
Tampa ·····Marshall Industries, (813) 576-1399
Tampa ·····Reptron, (813) 855-4656
GEORGIA: Atlanta ·····Marshall Industries, (404) 923-5750
Norcross ···Hammond Electronics, (404) 449-1996
Norcross ···Reptron, (404) 446-1300
ILLINOIS: Chicago·····Marshall Industries, (312) 490-0155
Schaumburg···Reptron, (312) 882-1700
INDIANA: Indianapolis···Marshall Industries, (317) 297-0483
KANSAS: Kansas City···Marshall Industries, (913) 492-3121

MARYLAND: Baltimore ·····Hammond Electronics, (301) 583-2525
Columbia ·····Diplomat Electronics, (301) 995-1226
Columbia ·····Vantage Components, (301) 720-5100
Gaithersburg·····Marshall Industries, (301) 840-9450
MASSACHUSETTS: Boston ·····Marshall Industries, (617) 272-8200
Burlington·····Western Micro, (617) 229-5819
Billercia ·····Diplomat Electronics, (617) 667-4670
MICHIGAN: Livonia···Marshall Industries, (313) 525-5850
Livonia···Reptron, (313) 525-2700
MINNESOTA: Minneapolis ···Marshall Industries, (612) 559-2211
Minnetonka ···Reptron, (612) 938-0000
Plymouth ·····Diplomat Electronics, (612) 559-2500
NEW JERSEY: Clifton ·····Vantage Components, (201) 777-4100
Fairfield ·····Marshall Industries, (201) 882-0320
Totowa ·····Diplomat Electronics, (201) 785-1830
NEW YORK: Binghamton ·····Marshall Industries, (607) 798-1611
Commack ·····Vantage Components, (516) 543-2000
Henrietta ·····Diplomat Electronics, (716) 359-4400
Liverpool ·····Diplomat Electronics, (315) 652-5000
Long Island·····Marshall Industries, (516) 273-2424
Melville ·····Diplomat Electronics, (516) 454-6400
Rochester ·····Marshall Industries, (716) 235-7620
NORTH CAROLINA: Greensboro ···Hammond Electronics, (919) 275-6391
Raleigh ·····Marshall Industries, (919) 878-9882
OHIO: Cleveland ·····Marshall Industries, (216) 248-1788
Dayton ·····Marshall Industries, (513) 236-8088
Worthington···Reptron, (614) 436-6675
OREGON: Beaverton ···Western Micro, (503) 629-2082
Portland·····Marshall Industries, (503) 644-5050
PENNSYLVANIA: Philadelphia ·····Marshall Industries, (609) 234-9100
Pittsburgh·····Marshall Industries, (412) 963-0441
TEXAS: Austin·····Diplomat Electronics, (512) 836-8707
Austin·····Marshall Industries, (512) 837-1991
Dallas·····Diplomat Electronics, (214) 980-1888
Dallas·····Marshall Industries, (214) 233-5200
Houston·····Marshall Industries, (713) 895-9200
UTAH: Salt Lake City···Diplomat Electronics, (801) 486-4134
Salt Lake City···Marshall Industries, (801) 261-0901
WASHINGTON: Redmond ···Western Micro (206) 881-6737
Seattle ·····Marshall Industries, (206) 747-9100
WISCONSIN: Milwaukee···Marshall Industries, (414) 797-8400

Sony Semiconductor Integrated Circuit Data Book

1986. Sept. 1st Edition

SONY®

Sony Semiconductor