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Semiconductor IC

Data Book 1991 Memory

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Semiconductor Integrated Circuit Data Book

1991

Preface

This is the 1991 version of the Sony Semiconductor IC Memory Databook. This book covers all the memory semiconductors marketed by Sony Corporation of America.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write, we welcome suggestions and comments.

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

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1) Static RAM (con't)

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CXK58267ATM-L/LL CXK58267AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 $\overline{CE}$	MIX CMOS	205
CXK59288P CXK59288J	32,768 word x 9bits, 15/20/25ns SRAM	MIX CMOS	216
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CXK581001P-L/LL CXK581001M-L/LL	131,072 word x 8bits, 70/85ns SRAM	MIX CMOS	243
CXK581000P-L/LL CXK581000M-L/LL	131,072 word x 8bits, 100/120/150ns SRAM	MIX CMOS	252
CXK581000P-LX/LLX CXK581000M-LX/LLX	131,072 word x 8bits, 100/120/150ns SRAM -25°C to +85°C (Extended Temp.)	MIX CMOS	263
CXK581000P-12LB CXK581000M-12LB	131,072 word x8bits, 120ns at V_{CC}=5V 240ns at V_{CC}=3V	MIX CMOS	272
CXK581100TM-L/LL CXK581100YM-L/LL	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	283
CXK581100TM-LX/LLX CXK581100YM-LX/LLX	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	294
CXK581100TM-12LB CXK581100YM-12LB	131,072 word x8bits, 120ns at V_{CC}=5V 240ns at V_{CC}=3V	MIX CMOS	303
CXK541000J	262,144 words x 4bits, 25/30/35ns SRAM	MIX CMOS	314

2) ASM (Application Specific Memory)

CXK7701J	8,192 word x 16bits, 30/35/45ns SRAM	MIX CMOS	324
CXK77910J	131,072 word x 9 bits, 17/20ns SRAM (Synchronous)	MIX CMOS	339

3) Mask ROM

CXK384001	524,288 word x 8bits, 200ns	CMOS	350

2. Product Over View

1) SRAM

Density	Organization	Product Name		Speed (ns)	Package	Process	Page
64K	64Kx1	CXK5164P	-25	25	22pin	MIX CMOS	29
			-30	30	300mil DIP		
			-35	35			
		CXK5164J	-25	25	24pin	MIX CMOS	29
			-30	30	300mil SOJ		
			-35	35			
	16Kx4	CXK5466P	-15	15	22pin	MIX CMOS	45
			-20	20	300mil DIP		
		CXK5466J	-15	15	24pin	MIX CMO8	45
			-20	20	300mil SOJ		
		CXK5464AP	-25	25	22pin	MIX CMOS	37
			-30	30	300mil DIP		
			-35	35			
		CXK5464AJ	-25	25	24pin	MIX CMOS	37
			-30	30	300mil SOJ		
			-35	35			
		CXK5467P	-15	15	24pin	MIX CMOS	61
		w/OE	-20	20	300mil DIP		
		CXK5467J	-15	15	24pin	MIX CMOS	61
		w/OE	-20	20	300mil SOJ		
		CXK5465P	-25	25	24pin	MIX CMOS	53
		w/OE	-30	30	300mil DIP		
			-35	35			
		CXK5465J	-25	25	24pin	MIX CMOS	53
		w/OE	-30	30	300mil SOJ		
			-35	35			
	8Kx8	CXK5863AP	-20	20	28pin	FULL CMOS	69
			-25	25	300mil DIP		
		CXK5863AJ	-20	20	28pin	FULL CMOS	69
			-25	25	300mil SOJ		
		CXK5863P	-25	25	28pin	FULL CMOS	76
			-30	30	300mil DIP		
			-35	35			
		CXK5863M	-25	25	28pin	FULL CMOS	76
			-30	30	450mil SOP		
			-35	35			
		CXK5863J	-25	25	28pin	FULL CMOS	76
			-30	30	300mil SOJ		
			-35	35			
		CXK5864BP	-70L/LL	70	28pin	MIX CMOS	86
			-10L/LL	100	600mil DIP		
			-12L/LL	120			
		CXK5864BSP	-70L/LL	70	28pin	MIX CMOS	86
			-10L/LL	100	300mil DIP		
			-12L/LL	120			
		CXK5864BM	-70L/LL	70	28pin	MIX CMOS	86
			-10L/LL	100	450mil SOP		
			-12L/LL	120			

Density	Organization	Product Name		Speed (ns)	Package	Process	Page
72K	8Kx9	CXK5971P	-25	25	28pin	FULL CMOS	96
			-30	30	300mil DIP		
			-35	35			
		CXK5971M	-25	25	28pin	FULL CMOS	96
			-30	30	450mil SOP		
			-35	35			
			-35	35			
		CXK5971J	-25	25	28pin	FULL CMOS	96
			-30	30	300mil SOJ		
			-35	35			
256K	256Kx1	CXK51256P	-35	35	24pin	MIX CMOS	106
			-45	45	300mil DIP		
			-55	55			
	64Kx4	CXK54256P	-35	35	24pin	MIX CMOS	114
			-45	45	300mil DIP		
			-55	55			
	32Kx8	CXK58258AP	-15	15	28pin	MIX CMOS	122
			-20	20	300mil DIP		
			-25	25			
		CXK58258AJ	-15	15	28pin	MIX CMOS	122
			-20	20	300mil SOJ		
			-25	25			
		CXK58258BP	-20L/LL	20	28pin	MIX CMOS	129
			-25L/LL	25	300mil DIP		
			-35L/LL	35			
		CXK58258BM	-20L/LL	20	28pin	MIX CMOS	129
			-25L/LL	25	450mil SOP		
			-35L/LL	35			
		CXK58258BJ	-20L/LL	20	28pin	MIX CMOS	129
			-25L/LL	25	300mil SOJ		
			-35L/LL	35			
		CXK58258P	-35	35	28pin	MIX CMOS	137
			-45	45	600mil DIP		
			-55	55			
		CXK58258SP	-35	35	28pin	MIX CMOS	137
			-45	45	300mil DIP		
			-55	55			
		CXK58257AP	-70L/LL	70	28pin	MIX CMOS	146
			-85L/LL	85	600mil DIP		
			-10L/LL	100			
			-12L/LL	120			
		CXK58257ASP	-70L/LL	70	28pin	MIX CMOS	146
			-85L/LL	85	300mil DIP		
			-10L/LL	100			
			-12L/LL	120			
		CXK58257AM	-70L/LL	70	28pin	MIX CMOS	146
			-85L/LL	85	450mil SOP		
			-10L/LL	100			
			-12L/LL	120			
		CXK58257AP	-70LX/LLX	70	28pin	MIX CMOS	156
			-85LX/LLX	85	600mil DIP		
			-10LX/LLX	100			
			-12LX/LLX	120			
		CXK58257ASP	-70LX/LLX	70	28pin	MIX CMOS	156
			-85LX/LLX	85	300mil DIP		
			-10LX/LLX	100			
			-12LX/LLX	120			
		CXK58257AM	-70LX/LLX	70	28pin	MIX CMOS	156
			-85LX/LLX	85	450mil SOP		
			-10LX/LLX	100			
			-12LX/LLX	120			

Density	Organization	Product Name		Speed (ns)	Package	Process	Page
256K (Con't)	32Kx8	CXK58257ATM	-70L/LL	70	28pin	MIX CMOS	166
			-85L/LL	85	TSOP		
			-10L/LL	100	TM: Normal		
			-12L/LL	120			
		CXK58257AYM	-70L/LL	70	28pin	MIX CMOS	166
			-85L/LL	85	TSOP		
			-10L/LL	100	YM: Reverse		
			-12L/LL	120			
		CXK58257ATM	-70LX/LLX	70	28pin	MIX CMOS	176
			-85LX/LLX	85	TSOP		
			-10LX/LLX	100	TM: Normal		
			-12LX/LLX	120			
		CXK58257AYM	-70LX/LLX	70	28pin	MIX CMOS	176
			-85LX/LLX	85	TSOP		
			-10LX/LLX	100	YM: Reverse		
			-12LX/LLX	120			
		CXK58257P	-70L/LL	70	28pin	MIX CMOS	186
			-85L/LL	85	600mil DIP		
			-10L/LL	100			
			-12L/LL	120			
		CXK58257SP	-70L/LL	70	28pin	MIX CMOS	186
			-85L/LL	85	300mil DIP		
			-10L/LL	100			
			-12L/LL	120			
		CXK58257M	-70L/LL	70	28pin	MIX CMOS	186
			-85L/LL	85	450mil SOP		
			-10L/LL	100			
			-12L/LL	120			
		CXK58267AP	-70L/LL	70	28pin	MIX CMOS	194
			-85L/LL	85	600mil DIP		
			-10L/LL	100	2CE		
			-12L/LL	120			
		CXK58267ASP	-70L/LL	70	28pin	MIX CMOS	194
			-85L/LL	85	300mil DIP		
			-10L/LL	100	2CE		
			-12L/LL	120			
		CXK58267AM	-70L/LL	70	28pin	MIX CMOS	194
			-85L/LL	85	450mil SOP		
			-10L/LL	100	2CE		
			-12L/LL	120			
		CXK58267ATM	-70L/LL	70	28pin	MIX CMOS	205
			-85L/LL	85	TSOP		
			-10L/LL	100	TM: Normal		
			-12L/LL	120	2CE		
		CXK58267AYM	-70L/LL	70	28pin	MIX CMOS	205
			-85L/LL	85	TSOP		
			-10L/LL	100	YM: Reverse		
			-12L/LL	120	2CE		
288K	32Kx9	CXK59288P	-15	15	32pin	MIX CMOS	216
			-20	20	300mil DIP		
			-25	25			
		CXK59288J	-15	15	32pin	MIX CMOS	216
			-20	20	300mil SOJ		
			-25	25			
		CXK59290M	-70L	70	32pin	MIX CMOS	223
			-10L	100	450mil SOP		
			-12L	120			
		CXK59290TM	-70L	70	32pin	MIX CMOS	223
			-10L	100	TSOP		
			-12L	120			

Density	Organization	Product Name		Speed (ns)	Package	Process	Page
1M	128Kx8	CXK581020SP	-35	35	32pin	MIX CMOS	234
			-45	45	400mil DIP		
			-55	55			
		CXK581020J	-35	35	32pin	MIX CMOS	234
			-45	45	400mil SOJ		
			-55	55			
		CXK581001P	-70L/LL	70	32pin	MIX CMOS	243
			-85L/LL	85	600mil DIP		
		CXK581001M	-70L/LL	70	32pin	MIX CMOS	243
			-85L/LL	85	525mil SOP		
		CXK581000P	-10L/LL	100	32pin	MIX CMOS	252
			-12L/LL	120	600mil DIP		
			-15L/LL	150			
		CXK581000M	-10L/LL	100	32pin	MIX CMOS	252
			-12L/LL	120	525mil SOP		
			-15L/LL	150			
		CXK581000P	-10LX/LLX	100	32pin	MIX CMOS	263
			-12LX/LLX	120	600mil DIP		
			-15LX/LLX	150			
		CXK581000M	-10LX/LLX	100	32pin	MIX CMOS	263
			-12LX/LLX	120	525mil SOP		
			-15LX/LLX	150			
		CXK581000P	-12LB	120	32pin	MIX CMOS	273
			-12LB	240 (V_{CC}=3V)			
		CXK581000M	-12LB	120	32pin	MIX CMOS	273
			-12LB	240 (V_{CC}=3V)			
		CXK581100TM	-10L/LL	100	32pin	MIX CMOS	283
			-12L/LL	120	TSOP		
			-15L/LL	150	(EIAJ Standard)		
		CXK581100YM	-10L/LL	100	32pin	MIX CMOS	283
			-12L/LL	120	TSOP		
			-15L/LL	150	(EIAJ Standard)		
		CXK581100TM	-10LX/LLX	100	32pin	MIX CMOS	294
			-12LX/LLX	120	TSOP		
			-15LX/LLX	150	(EIAJ Standard)		
		CXK581100YM	-10LX/LLX	100	32pin	MIX CMOS	294
			-12LX/LLX	120	TSOP		
			-15LX/LLX	150	(EIAJ Standard)		
		CXK581100TM	-12LB	120	TSOP		303
			-12LB	240 (V_{CC}=3V)			
		CXK581100YM	-12LB	120	TSOP		303
			-12LB	240 (V_{CC}=3V)			
		CXK541000J	-25	25	32pin	MIX CMOS	314
			-30	30	400mil SOJ		
			-35	35			

2) ASM (Application Specific Memory)

128K	4Kx16x2way 8Kx16	CXK7701J	-30	30	52pin	MIX CMOS	324
			-35	35	PLCC		
			-45	45			
1.1M	128Kx9	CXK77910J	-17	17	32pin	MIX CMOS	339
		(Synchronous)	-20	20	400mil SOJ		

3) Mask ROM

4M	512Kx8	CXK384001	200	32pin 600mil DIP	CMOS	350

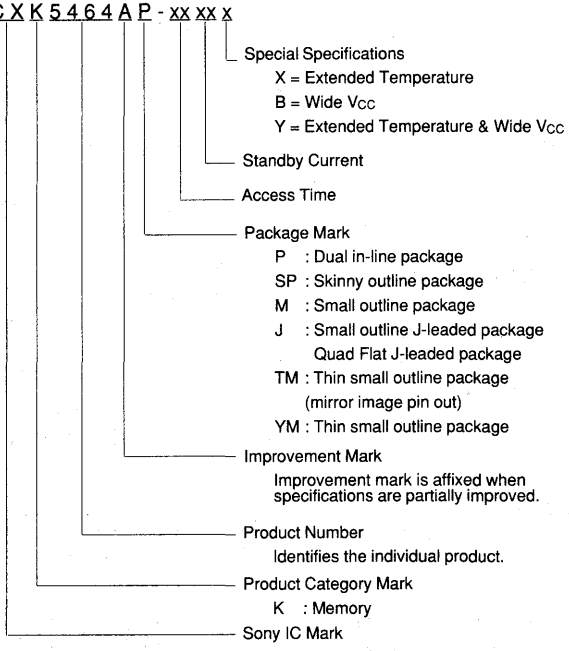
3. IC Nomenclature

1) Nonmenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

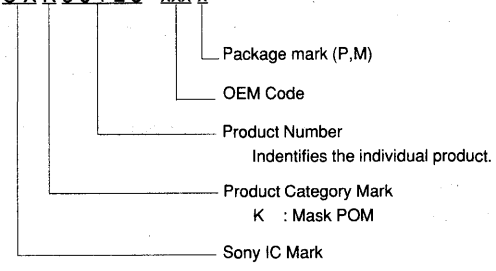
a) Memory Nomenclature

(Example) CXK5464AP-xxxxx



b) Mask ROM Nomenclature

(Example) CXK38128-xxxx



2

4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

Maximum rating must never be reached for any TWO items at the SAME time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit, the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

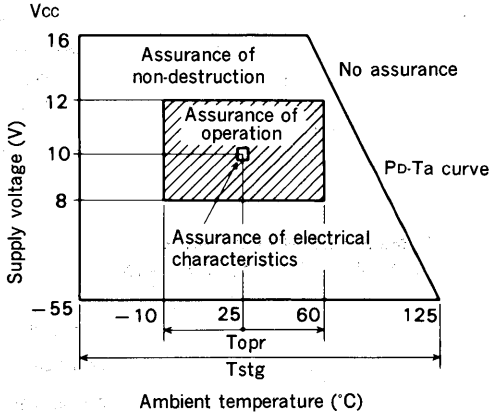
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

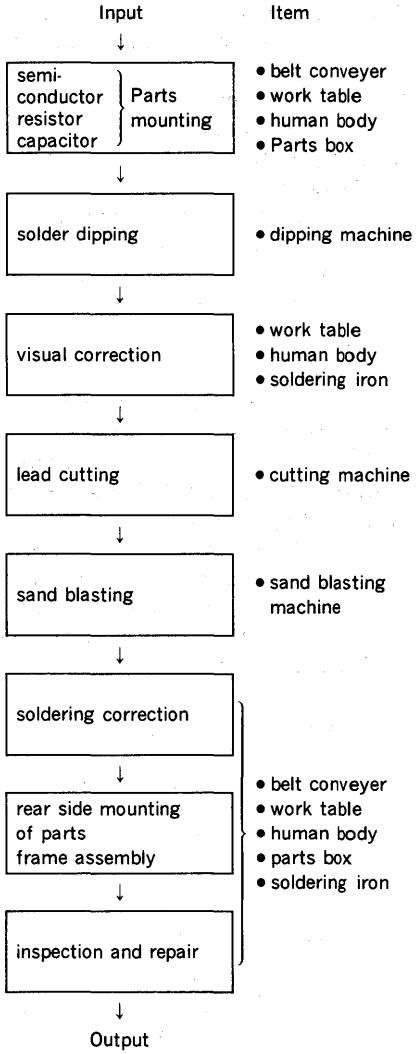
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.

One method is keeping relative humidity in the work room to about 50%.

Operator

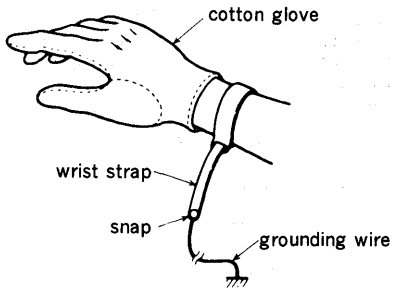
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

example of grounding band

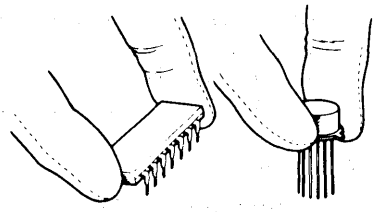


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

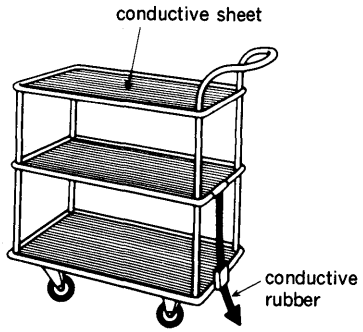
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

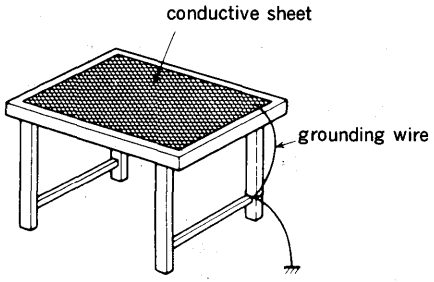
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

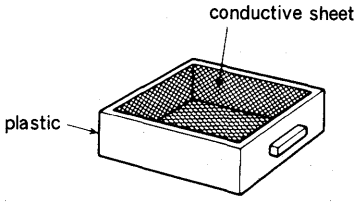
grounding of work table



(3) Semiconductor device case

Use a metal case, or an antistatic plastic case (lined with conductive sheet).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or on a wood or on a metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

(6) Other points of caution

Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

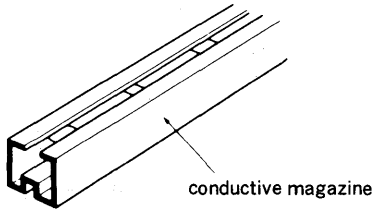
Transporting, storing and packaging methods

(1) Magazine

Use metal, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.

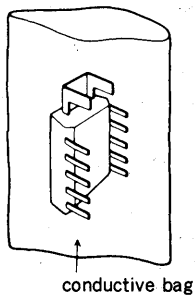
magazine



(2) Bag

Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.

bag

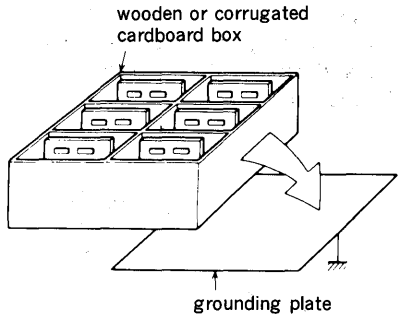


2

(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



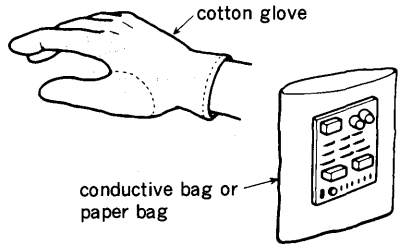
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

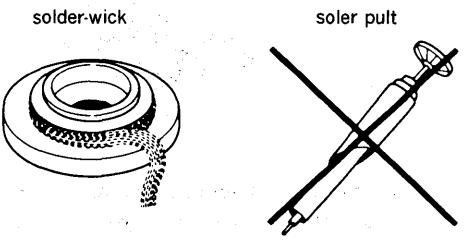
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

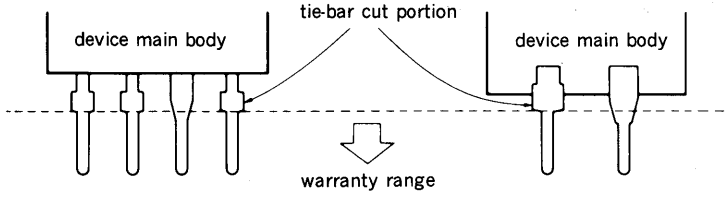
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

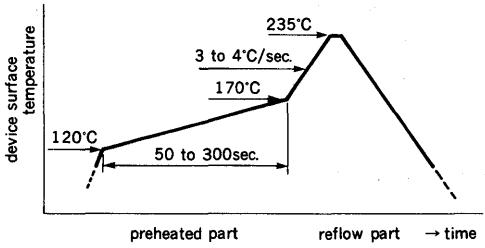
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

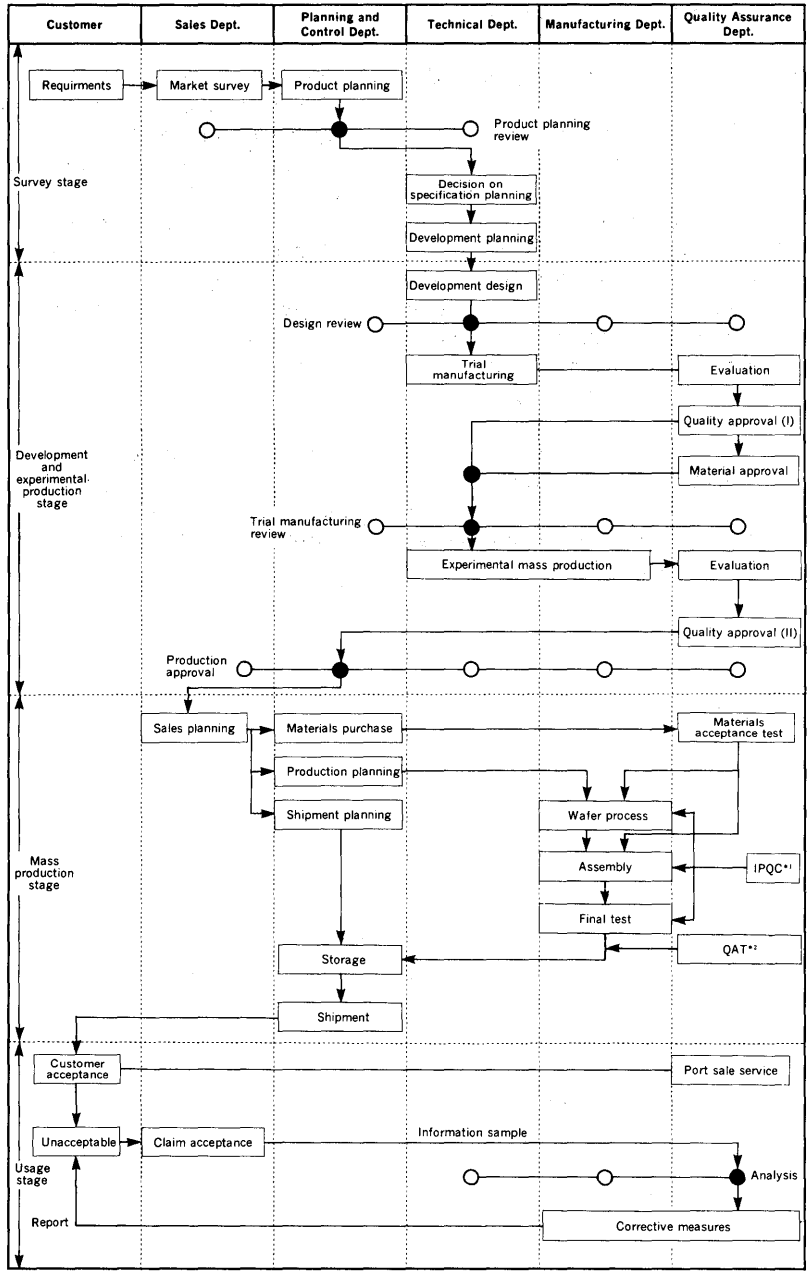
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

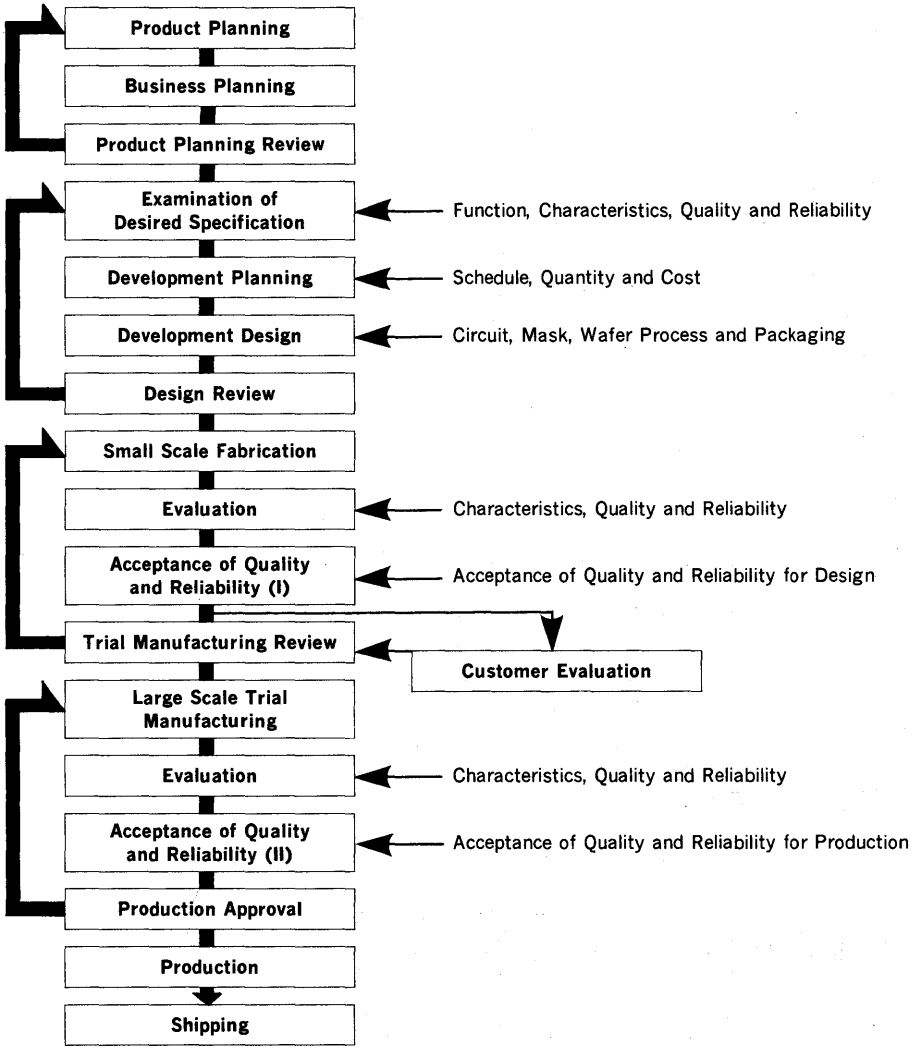
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



6. SRAM Cross Reference Guide

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers									
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
16K	2Kx8	CXK5816PN-10L	100	24pin	HM6116AP									
		-12L	120	600mil DIP										
		-15L	150											
		CXK5816M-10L	100	24 pin	HM6116AFP									
		-12L	120	450mil SOP										
		-15L	150											
64K	64Kx1	CXK5164P-25	25	22 pin	HM6287HP	TC5562P	M5M5187AP	CY7C187	IDT7187	MT5C6401	MB81C71A			MCM6287
		-30	307	300mil DIP										
		-35	35											
		CXK5164J-25	25	22 pin	HM6287HJP	TC5562J	M5M5187AJ			MT5C6401DJ	MB81C71A			MCM6287
		-30	30	300mil SOJ										
		-35	35											
	16Kx4	CXK5464AP-25	25	22 pin	HM6788P	TC55416P	M5M5188AP	CY7C164	IDT7188	MT5C6404	MB81C71			
		-30	30	300mil DIP										
		-35	35											
		CXK5464AJ-25	25	24 pin			M5M5188AJ			MT5C6404DJ				
		-30	30	300mil SOJ										
		-35	35											
		CXK5466P-15	15	22 pin	HM6788HP		M5M5188BP	CY7C164	IDT7188	MT5C6404	MB81C74			MCM6288
		-20	20	300mil DIP										
		CXK5466J-15	15	24 pin			M5M5188BJ			MT5C6404DJ				MCM6288
		-20	20	300mil SOJ										
		CXK5465P-25	25	24 pin	HM6789P	TC55417P	M5M5189AP	CY7C166	IDT6198	MT5C6405	MB81C75			
		-30	30	300mil DIP										
		-35	35											
		CXK5465J-25	25	24 pin		TC55417J	M5M5189AJ	CY7C166		MT5C6405DJ				
		-30	30	300mil SOJ										
		-35	35											
		CXK5467P-15	15	24 pin	HM6789H		M5M5189BP	CY7C166	IDT6198	MT5C6405	MB81C75			MCM6290
		-20	20	300mil DIP										
		CXK5467J-15	15	24 pin			M5M5189BJ			MT5C6405DJ				MCM6290
		-20	20	300mil SOJ										

SRAM Cross Reference Guide (con't)

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers									
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
64K (Con't)	8Kx8	CXK5866P-12 -15 -20	12 15 20	28 pin 300mil DIP		TC5588D		CY7C185	IDT7164	MT5C6408				MCM6264
		CXK5866J-12 -15 -20	12 15 20	28 pin 300mil SOJ		TC5588J		CY7C185		MT5C6408DJ				MCM6264
		CXK5863AP-20 -25	20 25	28 pin 300mil DIP		TC5588P		CY7C185	IDT7164	MT5C6408				MCM6264
		CXK5863AJ-20 -25	20 25	28 pin 300mil SOJ		TC588J		CY7C185		MT5C6408DJ				MCM6264
		CXK5863P-25 -30 -35	25 30 35	28 pin 300mil DIP		TC5588P		CY7C185	IDT7164	MT5C6408	MB81C78A			MCM6264
		CXK5863M-25 -30 -35	25 30 35	28 pin 450mil SOP										
		CXK5863J-25 -30 -35	25 30 35	28 pin 300mil SOJ		TC5588J		CY7C185		MT5C6408DJ				MCM6264
		CXK5864BP-70L -10L -12L	70 100 120	28 pin 600mil DIP	HM6264AP	TC5563AP	M5M5165P				MB8464A	MPD4364	KM6264AP	
		CXK5864SP-70L -10L -12L	70 100 120	28 pin 300mil DIP	HM6264ASP								KM6264AG	
		CXK5864BM-70L -10L -12L	70 100 120	28 pin 450mil SOP	HM6264AFP	TC5563AF	M5M5165FP				MB8464A			
72K	8Kx9	CXK5971P-25 -30 -35	25 30 35	28 pin 300mil DIP		TC5589P					MB81C79A			MCM6265
		CXK5971J-25 -30 -35	25 30 35	28 pin 300mil SOJ		TC5589J								MCM6265
		CXK5971M-25 -30 -35	25 30 35	28pin 450mil SOP							MB81C79A			
		CXK5972P-12 -15 -20	12 15 20	28 pin 300mil DIP		TC5589P					MB82B79			MCM6265
		CXK5972J-12 -15 -20	12 15 20	28pin 300mil SOJ		TC5589J								MCM6265

SRAM Cross Reference Guide (con't)

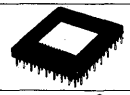
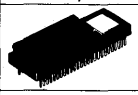
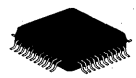
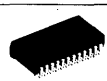
Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers									
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
256K	256Kx1	CXK51256P-35	35	24 pin	HM6207		M5M5257P	CY7C197	IDT71257	MT5C2561	MB81C81	MPD43254	KM61257P	
		-45	45	300mil DIP										
		-55	55											
	64Kx4	CXK54256P-35	35	24 pin	HM6208	TC55465P	M5M5258P	CY7C194	IDT71258	MT5C2564	MB81C86		KM64257P	
		-45	45	300mil DIP										
		-55	55											
	32Kx8	CXK58258P-35	35	28 pin				CY7C198	IDT71256	MT5C2568W				
		-45	45	600mil DIP										
		-55	55											
		CXK58258SP-35	35	28 pin	HM62832	TC55328P		CY7C199		MT5C2568				
		-45	45	300mil DIP										
		-55	55											
		CXK58258AJ-15	15	28 pin		T55328J				MT5C2568				
		-20	20	300mil SOJ										
		-25	25											
		CXK58258AP-15	15	28 pin		T55328P		CY7C199		MT5C2568				MCM6206
		-20	20	300mil DIP										
		-25	25											
		CXK58258BP-20L	20	28 pin					IDT712564L					
		-25L	25	300mil DIP										
		-35L	35											
		CXK58258BJ-20L	20	28 pin										
		-25L	25	300mil SOJ										
		-35L	35											
		CXK58258BM-20L	20	28 pin					IDT712564L					
		-25L	25	450mil SOP										
		-35L	35											
		-70L	70											
		CXK58257P-85L	85	28 pin	HM62256P	TC55257	M5M255P				MB84256	MPD43256A	KM62256AP	
		CXK58257AP-10L	100	600mil DIP		AP	M5M256P							
		-12L	120											
		-70L	70											
		CXK58257SP-85L	85	28 pin										
		CXK58257ASP-10L	100	300mil DIP										
		-12L	120											
		-70L	70											
		CXK58257M-85L	85	28 pin	HM62256FP	TC55257	M5M255FP				MB84256		KM62256AG	
		CXK58257AM-10L	100	450mil SOP		AF	M5M256FP							
		-12L	120											
		-70L	70				M5M5256							
		CXK58257ATM-85L	85	28 pin			BVP/VP							
		CXK58257AYM-10L	100	(*) TSOP			M5M5256							
		-12L	120				BRV/RV							

(*) Mitsubishi Pin Compatible

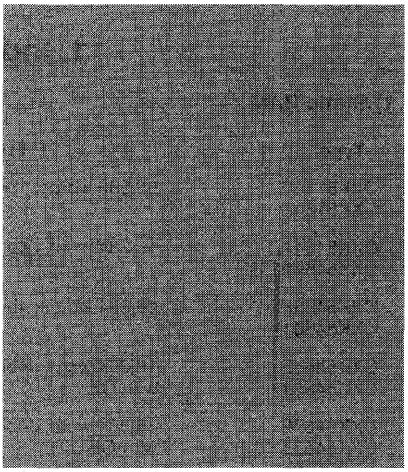
SRAM Cross Reference Guide (con't)

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers								
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
288K	32Kx9	CXK59288P-15 -20 -25	15 20 25	32 pin 300mil DIP		T55329P			IDT71259					MCM6205
		CXK59288J-15 -20 -25	15 20 25	32 pin 300mil SOJ		T55329J								MCM6205
1M	128Kx8	CXK581020SP-35 -45 -55	35 45 55	32 pin 400mil DIP						MT5C1008				
		CXK581020J-35 -45 -55	35 45 55	32 pin 400mil SOJ										
		CXK581001P-70L -85L	70 85	32pin 600mil DIP	HM628128P	TC551001P	M5M51008P						KM581000P	
		CXK581001M-70L -85L	70 85	32pin 525mil SOP	HM628128FP		M5M51008FP						KM581000G	
		CXK581000P-10L -12L -15L	100 120 150	32 pin 600mil DIP	HM628128P	TC551001P	M5M51008P						KM581000P	
		CXK58000M-10L -12L -15L	100 120 150	32 pin 525mil SOP	HM628128FP		M5M51008FP						KM581000G	
		CXK581100TM-10L CXK581100YM-12L -15L	100 120 150	TSOP (EIAJ Standard)	HM628128TS		M5M51008VP M5M51008RV							
126K	4Kx16x 2 way & 8Kx16	CXK7701J-30 -35 -45 -55	30 35 45 55	52 pin PLCC	HM62A168	TC55168T		CY7C184		MT56C2416EJ	V63C328 (Vitelic)			
		CXK7701AJ-25 -35 -45	25 35 45	52 pin PLCC	HM62A168	TC55168T		CY7C184		MT56C2416EJ	V63C328 (Vitelic)			

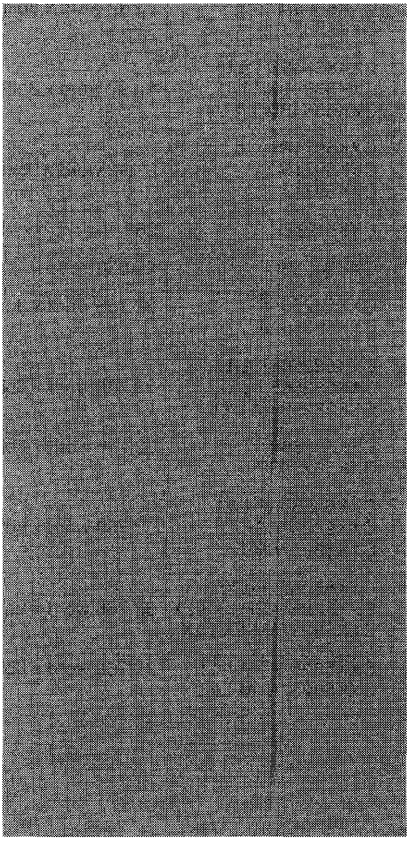
7. Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	Zig-Zag IN-LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK Zig-Zag IN-LINE PACKAGE		P	1.778mm (70MIL) Zig Zag inline	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE		P	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
	Standard chip carrier	Q F J (PLCC)	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		Q F N (LCC)	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package side

*P……Plastic, C……Ceramic



Static RAM



1. Index by Usage

1) Static RAM

Type	Function	Process	Page
CXK5164P CXK5164J	65,536 word x 1bit, 25/30/35ns SRAM	MIX CMOS	29
CXK5464AP CXK5464AJ	16,384 word x 4bits, 25/30/35ns SRAM	MIX CMOS	37
CXK5466P CXK5466J	16,384 word x 4bits, 15/20ns SRAM	MIX CMOS	45
CXK5465P CXK5465J	16,384 word x 4bits, 25/30/35ns SRAM with $\overline{OE}$	MIX CMOS	53
CXK5467P CXK5467J	16,384 word x 4bits, 15/20ns SRAM with $\overline{OE}$	MIX CMOS	61
CXK5863AP CXK5863AJ	8,192 word x 8bits, 20/25/30ns SRAM	FULL CMOS	69
CXK5863P CXK5863M CXK5863J	8,192 word x 8bits, 25/30/35ns SRAM	FULL CMOS	76
CXK5864BP-L/LL CXK5864BSP-L/LL CXK5864BM-L/LL	8,192 word x 8bits, 70/100/120ns SRAM	MIX CMOS	86
CXK5971P CXK5971M CXK5971J	8,192 word x 9bits, 25/30/35ns SRAM	FULL CMOS	96
CXK51256P	262,144 word x 1bit, 35/45/55ns SRAM	MIX CMOS	106
CXK54256P	65,536 word x 4bits, 35/45/55ns SRAM	MIX CMOS	114
CXK58258AP CXK58258AJ	32,768 word x 8bits, 15/20/25ns SRAM	MIX CMOS	122
CXK58258BP-L/LL CXK58258BJ-L/LL CXK58258BM-L/LL	32,768 word x 8bits, 20/25/35ns SRAM	MIX CMOS	129
CXK58258P CXK58258SP	32,768 word x 8bits, 35/45/55ns SRAM	MIX CMOS	137
CXK58257AP-L/LL CXK58257ASP-L/LL CXK58257AM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	146
CXK58257AP-LX/LLX CXK58257ASP-LX/LLX CXK58257AM-LX/LLX	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	156
CXK58257ATM-L/LL CXK58257AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	166

1) Static RAM (con't)

Type	Function	Process	Page
CXK58257ATM-LX/LLX CXK58257AYM-LX/LLX	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	176
CXK58257P-L/LL CXK58257SP-L/LL CXK58257M-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	186
CXK58267AP-L/LL CXK58267ASP-L/LL CXK58267AM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 $\overline{CE}$	MIX CMOS	194
CXK58267ATM-L/LL CXK58267AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 $\overline{CE}$	MIX CMOS	205
CXK59288P CXK59288J	32,768 word x 9bits, 15/20/25ns SRAM	MIX CMOS	216
CXK59290M-L CXK59290TM-L	32,768 word x 9 bits, 70/10/120ns SRAM	MIX CMOS	223
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CXK581000P-LX/LLX CXK581000M-LX/LLX	131,072 word x 8bits, 100/120/150ns SRAM -25°C to +85°C (Extended Temp.)	MIX CMOS	263
CXK581000P-12LB CXK581000M-12LB	131,072 word x8bits, 120ns at V_{CC}=5V 240ns at V_{CC}=3V	MIX CMOS	272
CXK581100TM-L/LL CXK581100YM-L/LL	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	283
CXK581100TM-LX/LLX CXK581100YM-LX/LLX	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	294
CXK581100TM-12LB CXK581100YM-12LB	131,072 word x8bits, 120ns at V_{CC}=5V 240ns at V_{CC}=3V	MIX CMOS	303
CXK541000J	262,144 words x 4bits, 25/30/35ns SRAM	MIX CMOS	314

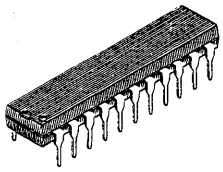
65,536-word × 1-bit High Speed CMOS Static RAM

Description

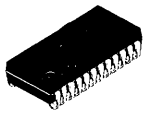
CXK5164P/J are 65,536 bits high speed CMOS static RAMs organized as 65,536 words by 1 bit and operate from a single 5V supply.

These devices have separate Data input and Data Output pins.

CXK5164P
24 pin SOJ (Plastic)



CXK5164J
24 pin SOJ (Plastic)



Features

- Fast access time :
  CXK5164P/J-25 25ns (Max.)
  CXK5164P/J-30 30ns (Max.)
  CXK5164P/J-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single + 5V supply : +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Separate I/O pins
- Three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 22 pin plastic DIP
  300mil 24 pin plastic SOJ

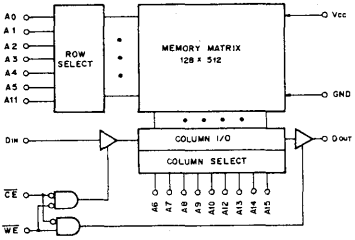
Function

65,536-word × 1-bit static RAM

Structure

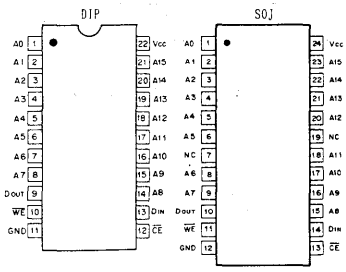
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
Din	Data input
Dout	Data output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

3

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature	Tsolder	260 • 10	℃ • sec
Voltage applied to output	V_{OUT}	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W

***Note**) V_{CC}, V_{IN}, V_{OUT} = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	Dout	V_{CC} Current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	I_{CC1}, I_{CC2}
L	L	Write	High Z	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*2	—	0.8	V

Note) *1. V_{CC} = 25C°

*2. V_{IL} = − 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70℃)

Item	Symbol	Test conditions	−25/30/35			Unit
			Min.	Typ.	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA V_{IN} = V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100% I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V, V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

***Note**) V_{CC} = 5.0V, Ta = 25℃

I/O capacitance

(Ta = 25℃, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

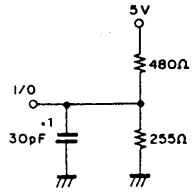
AC characteristics

• AC test conditions

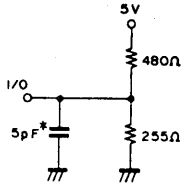
(V_{CC} = 5V ± 10%, Ta = 0 to +70℃)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



*1. Including scope and jig
*2. For t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

● **Read cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	25	ns

* **Note**) Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

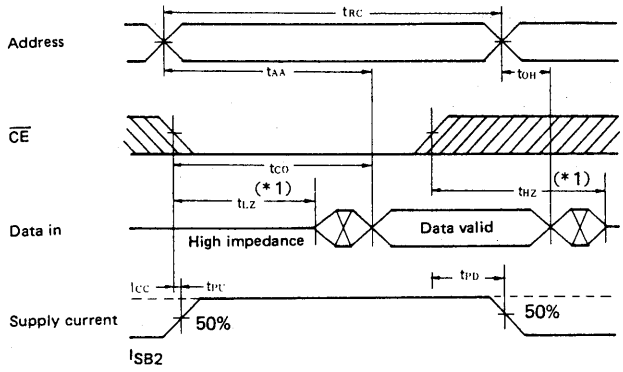
● **Write cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

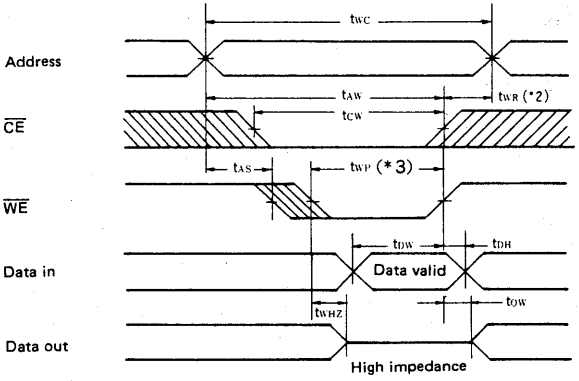
* **Note**) Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

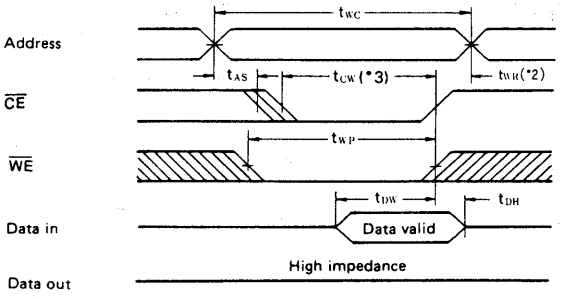
• Read cycle : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control

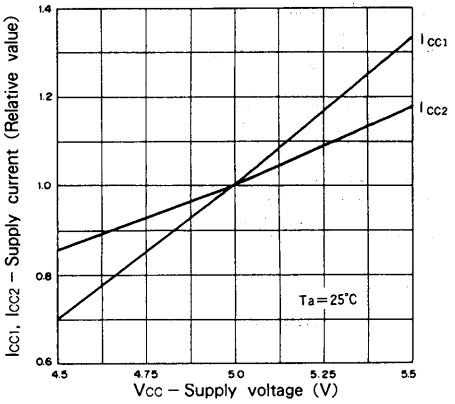


*** Note)**

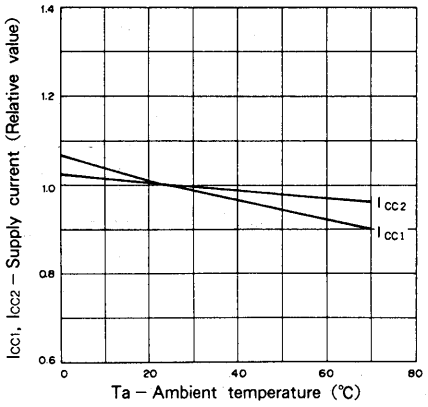
1. At any conditions, t_{HZ} is less than t_{LZ}.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.

Example of Representative Characteristics

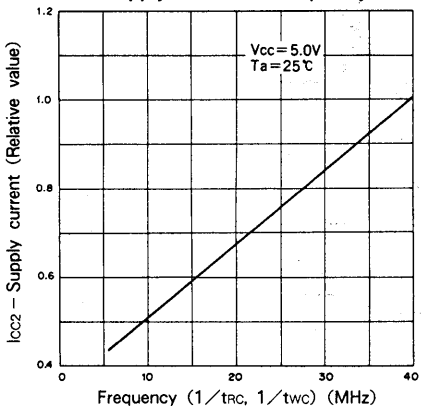
Supply current vs. Supply voltage



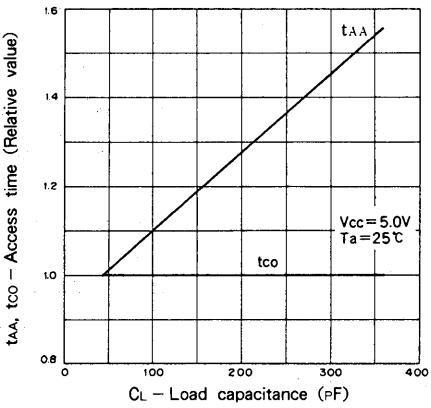
Supply current vs. Ambient temperature



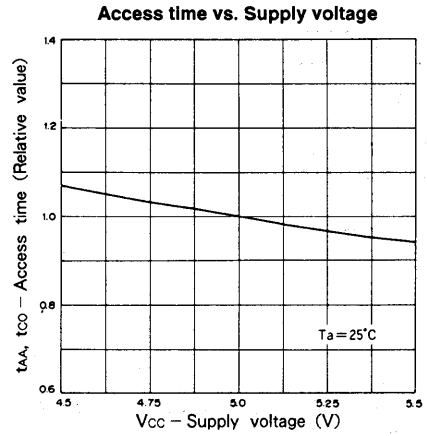
Supply current vs. Frequency



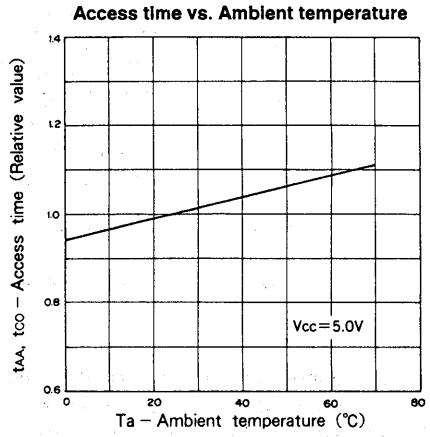
Access time vs. Load capacitance



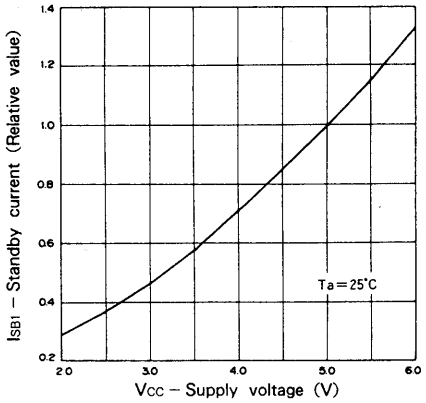
Access time vs. Supply voltage



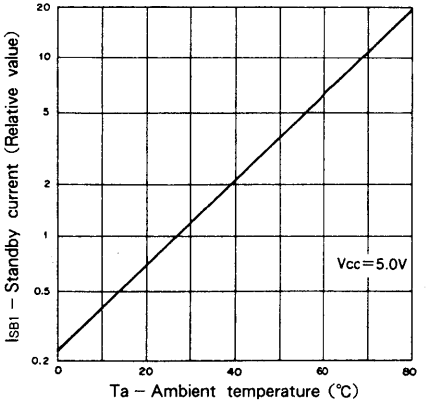
Access time vs. Ambient temperature



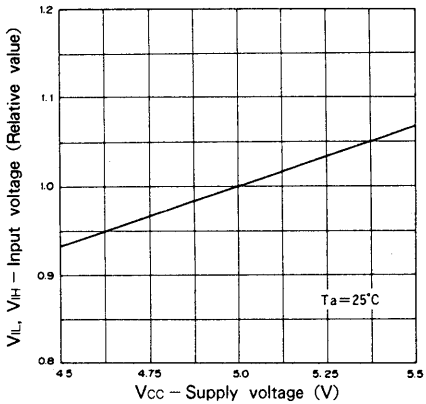
Standby current vs. Supply voltage



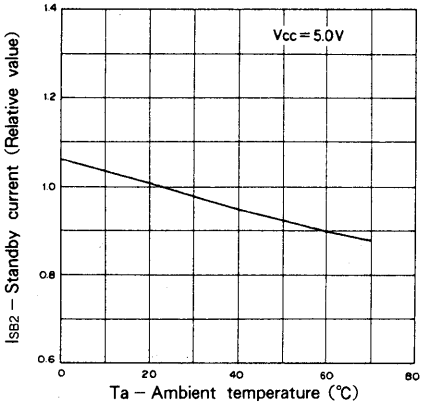
Standby current vs. Ambient temperature



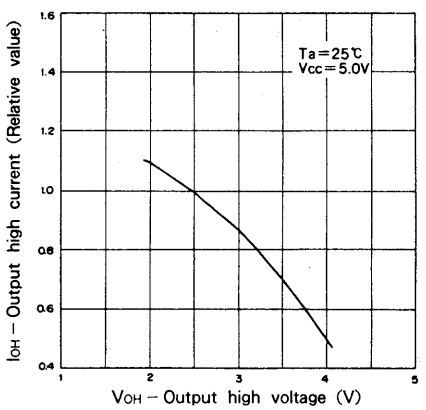
Input voltage level vs. Supply voltage



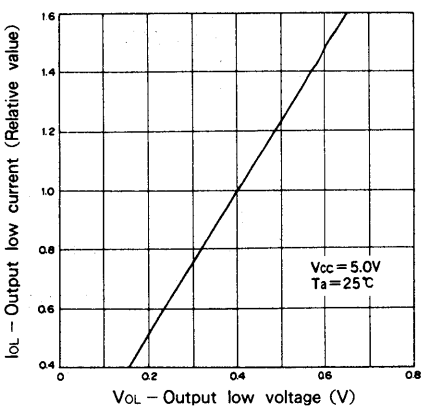
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



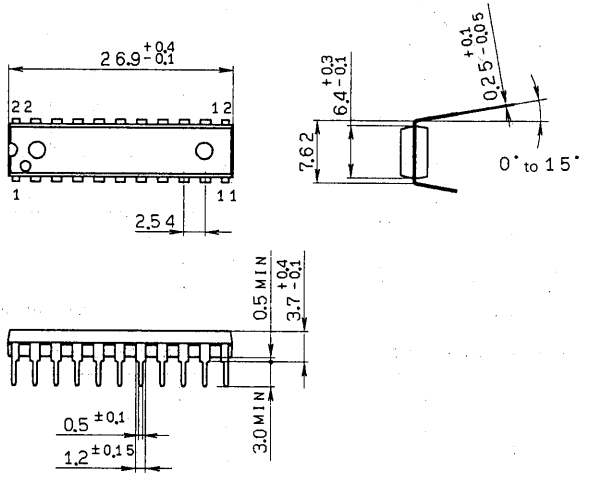
Output low current vs. Output low voltage



3

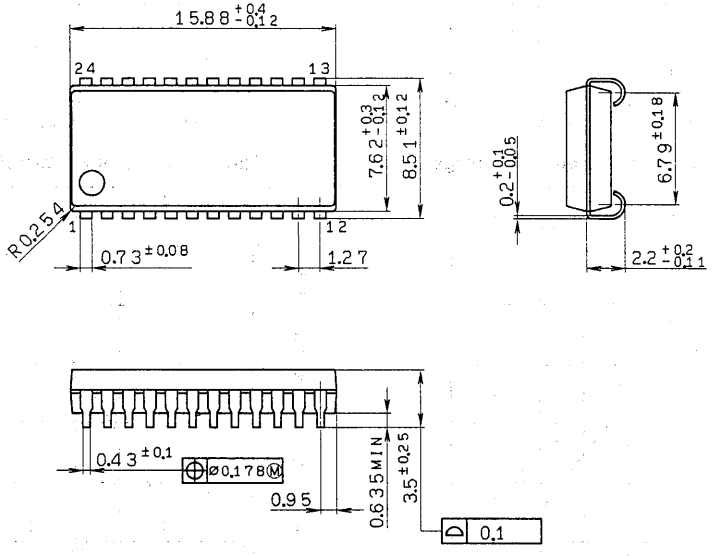
Package Outline Unit : mm

CXK5164P 22 pin DIP (Plastic) 300mil 1.3g



DIP-22P-02

CXK5164J 24 pin SOJ (Plastic) 300mil 0.7g



SOJ-24P-01

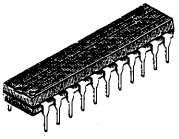
SONY CXK5464AP/AJ 25/30/35

16,384-word × 4-bit High Speed CMOS Static RAM

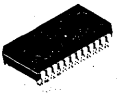
Description

CXK5464AP/AJ are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

CXK5464AP
22 pin DIP (Plastic)



CXK5464AJ
24 pin SOJ (Plastic)



Features

- Fast access time :
  CXK5464AP/AJ-25 25ns (Max.)
  CXK5464AP/AJ-30 30ns (Max.)
  CXK5464AP/AJ-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : Three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 22 pin plastic DIP
  300mil 24 pin plastic SOJ

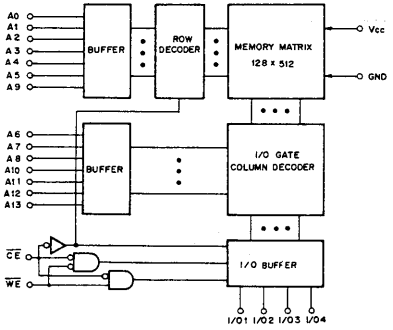
Function

16,384-word × 4-bit static RAM

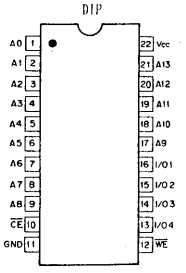
Structure

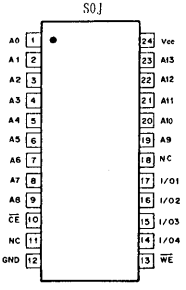
Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)





Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

3

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature	Tsolder	260 • 10	℃ • sec
Allowable power dissipation	P_D	1.0	W

* V_{CC}, V_{IN}, $V_{I/O}$ = −3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} Current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	I_{CC1}, I_{CC2}
L	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70℃, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

*1. V_{CC} = 5V, Ta = 25℃

*2. V_{IL} = −3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	−25/30/35			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN} = GND to Vcc	−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc	−1	—	1	μA
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA V_{IN} = V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100% I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* Vcc = 5.0V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

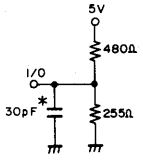
AC characteristics

• AC test conditions

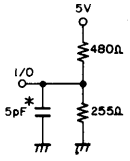
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

● Read cycle

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip enable to power down time	t_{PD}	—	20	—	25	—	25	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

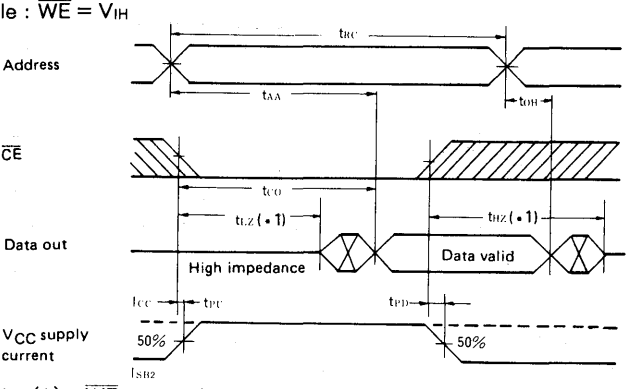
● Write cycle

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

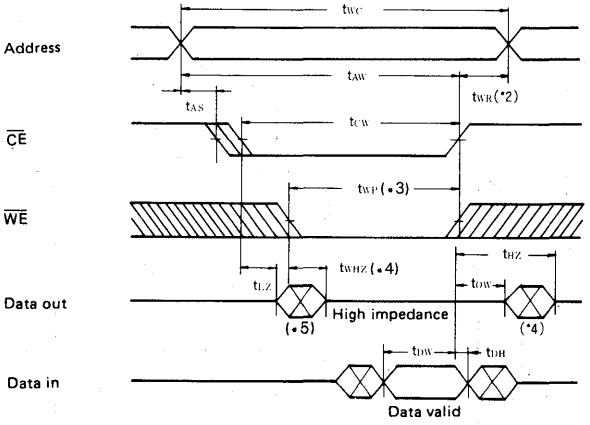
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

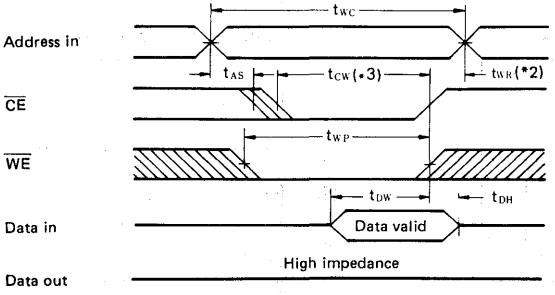
• Read cycle : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



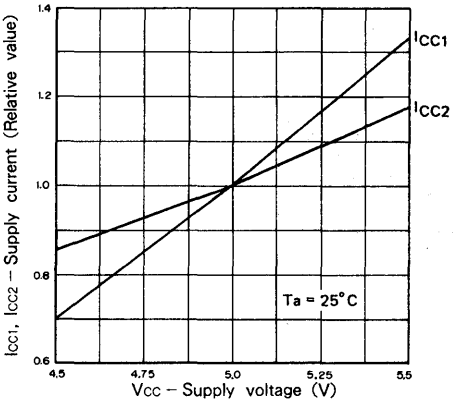
***Note)**

1. At any conditions, t_{HZ} is less than t_{LZ}.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

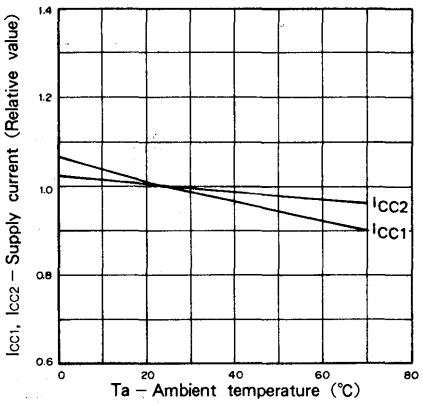
3

Example of Representative Characteristics

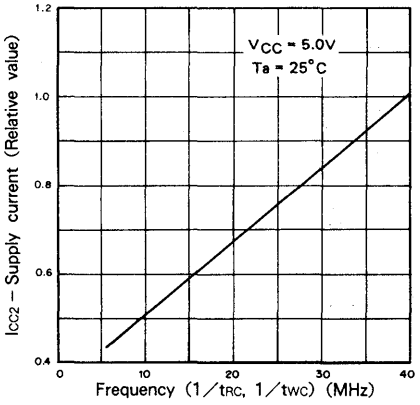
Supply current vs. Supply voltage



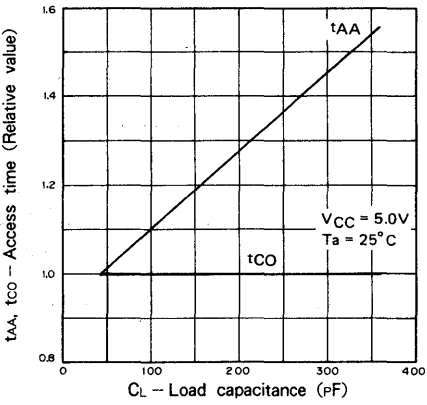
Supply current vs. Ambient temperature



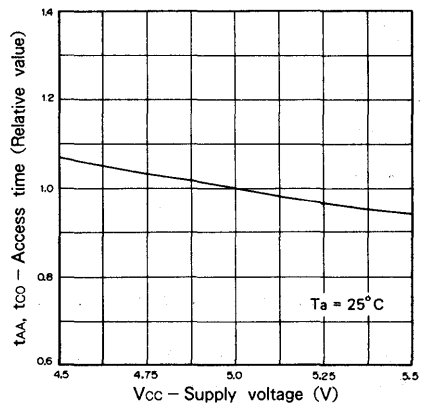
Supply current vs. Frequency



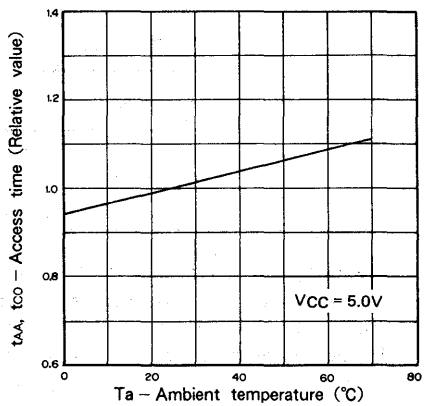
Access time vs. Load capacitance



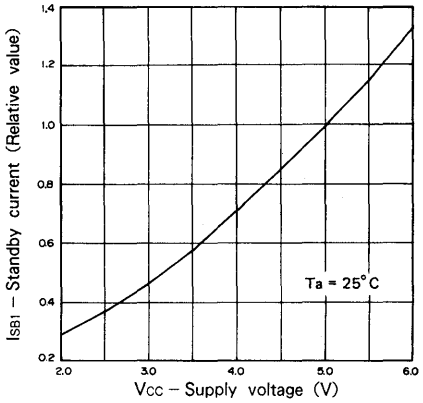
Access time vs. Supply voltage



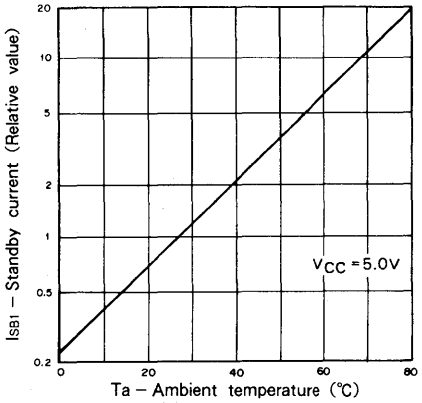
Access time vs. Ambient temperature



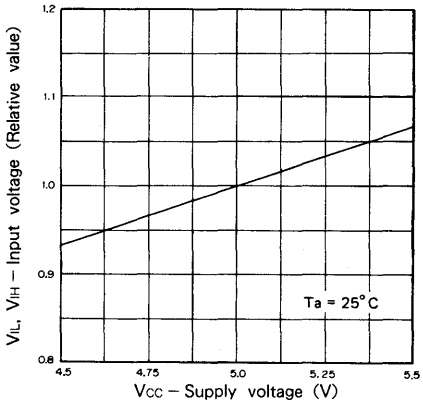
Standby current vs. Supply voltage



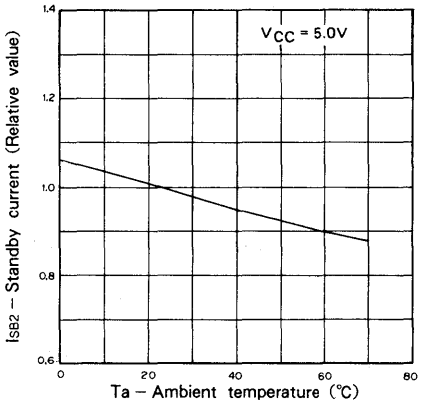
Standby current vs. Ambient temperature



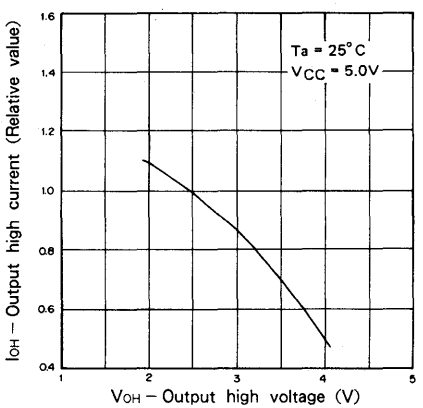
Input voltage level vs. Supply voltage



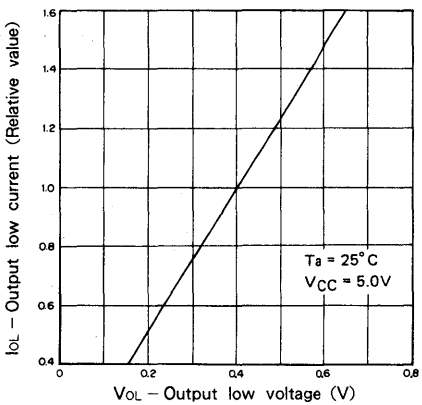
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



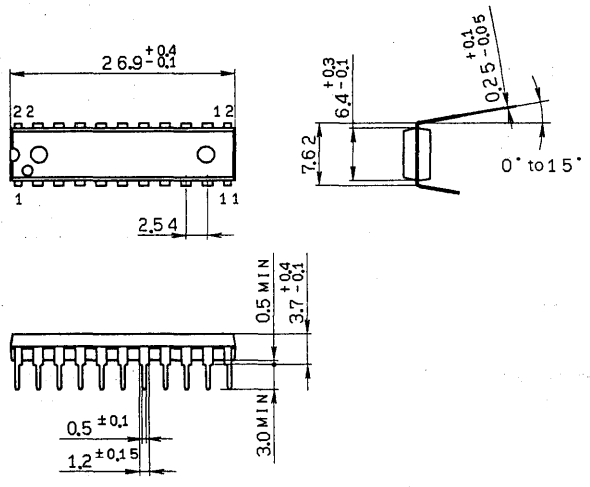
Output low current vs. Output low voltage



3

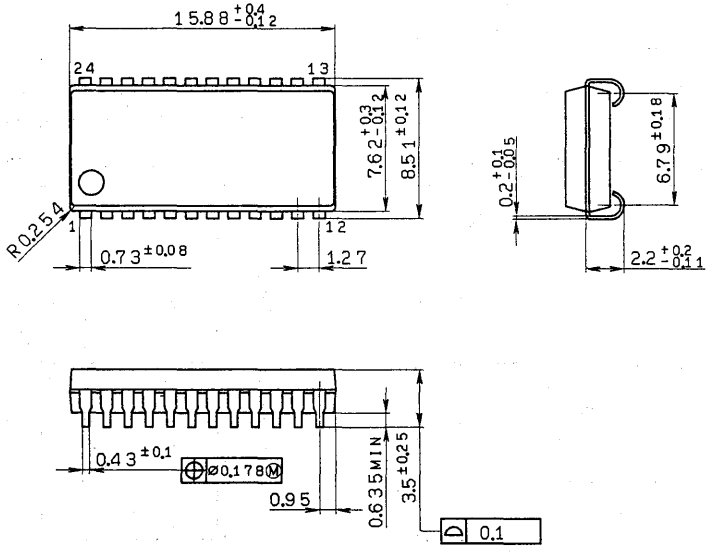
Package Outline Unit : mm

CXK5464AP 22 pin DIP (Plastic) 300mil 1.3g



DIP-22P-02

CXK5464AJ 24 pin SOJ (Plastic) 300mil 0.7g



SOJ-24P-01

16,384 word × 4-bit High Speed CMOS Static RAM

Description

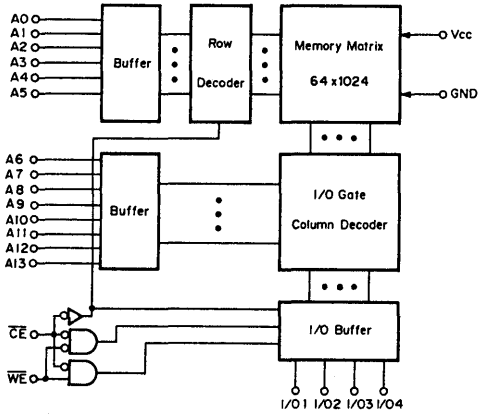
CXK5466P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal.

Features

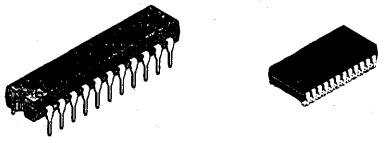
- Fast access time :
  CXK5466P/J-15 15ns (Max.)
  CXK5466P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
  During operation
- Single +5V supply : +5V ± 10%
- Fully static memory
  ···No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :
  three-state output
- Directly TTL compatible :
  All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 22 pin plastic DIP
  300 mil 24 pin plastic SOJ

Block Diagram



CXK5466P
22 pin DIP (Plastic)

CXK5466J
24 pin SOJ (Plastic)



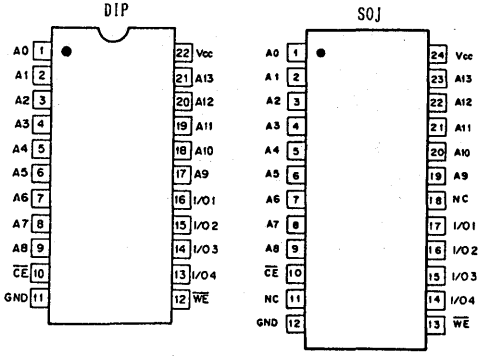
Functions

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

3

E89520B02 – ST

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ Min. = −3.5V for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} current
H	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data output	I_{CC1}, I_{CC2}
L	L	Write	Data input	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

*1) V_{CC} = 5V, Ta = 25°C

*2) V_{IL} Min. = −3.0V for pulse width less than 20ns.

DC Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leak current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, V_{IN} = V_{IH} or V_{IL}		—	30	55	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100%, I_{OUT} = 0mA	−15	—	95	150	mA
			−20	—	90	140	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V		—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL} Cycle = Min.		—	—	85	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

* Vcc = 5.0V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

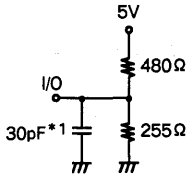
AC characteristics

• AC test conditions

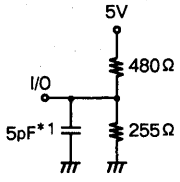
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance
*2 for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	15	—	20	ns
Output hold from address change	t_{OH}	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	2	—	3	—	ns
Chip disable to output in high Z	t_{HZ}*	0	6	0	8	ns
Chip enable to power up time	t_{PU}	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at ±200mV (See Fig. 1)

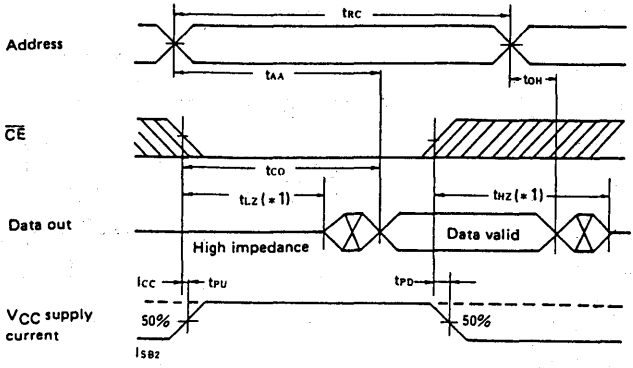
• **Write cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	15	—	20	—	ns
Address valid to end of write	t_{AW}	13	—	18	—	ns
Chip enable to end of write	t_{CW}	13	—	18	—	ns
Data to write time overlap	t_{DW}	8	—	11	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	13	—	18	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output active from end of write	t_{OW}*	2	—	3	—	ns
Write to output in high Z	t_{WHZ}*	0	5	0	7	ns

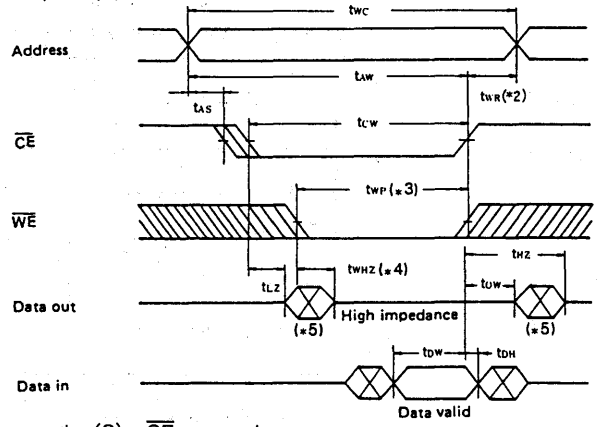
* Transition is tested by means of load conditions (2), from stationary condition at ±200mV (See Fig. 1)

Timing Waveform

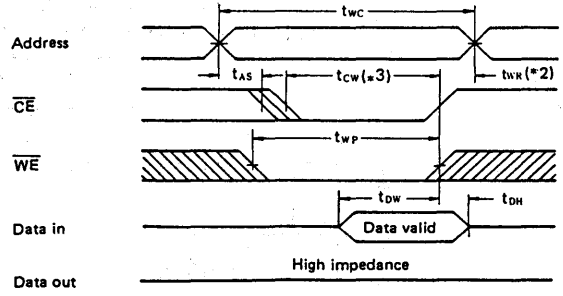
• Read cycle : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



*1) Whatever the conditions, t_{HZ} is smaller than t_{LZ}.

*2) t_{WR} is tested from either $\overline{CE}$ or $\overline{WE}$ rise, whichever comes earlier, until the end of write cycle.

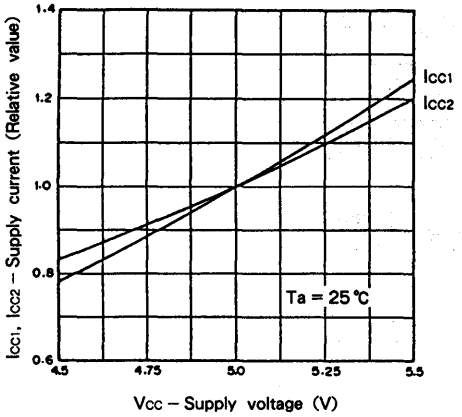
*3) Write is performed when both $\overline{CE}$ and $\overline{WE}$ are in the low overlap.

*4) When $\overline{WE}$ fall is performed simultaneously with $\overline{CE}$ fall, or before, output is kept to high impedance.

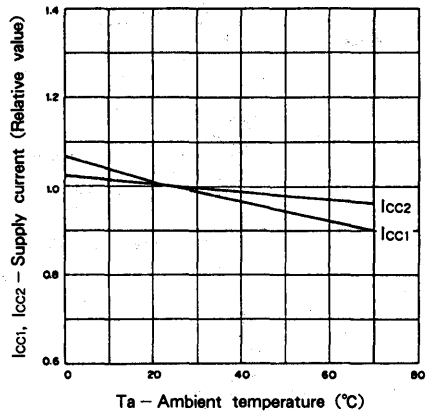
*5) While I/O pins are in output state, do not apply data input signals with a phase opposite to that of the output.

Example of Represeutative Characteristics

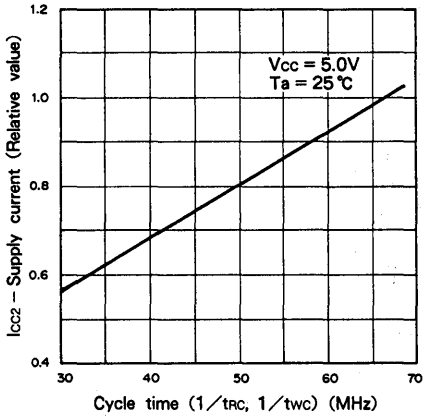
Supply current vs. Supply voltage



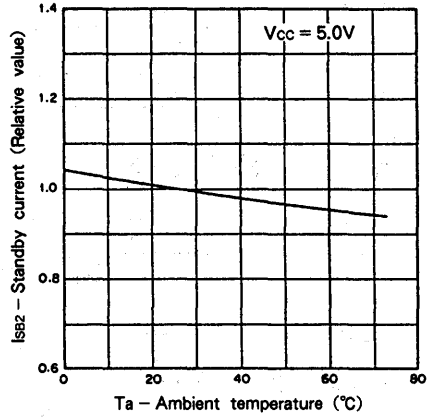
Supply current vs. Ambient temperature



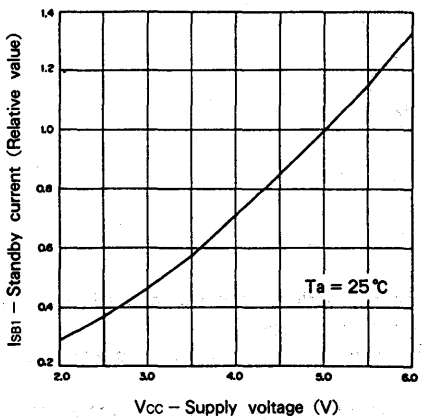
Supply current vs. Cycle time



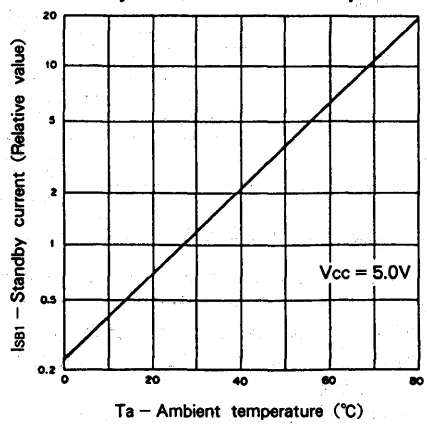
Standby current vs. Ambient temperature



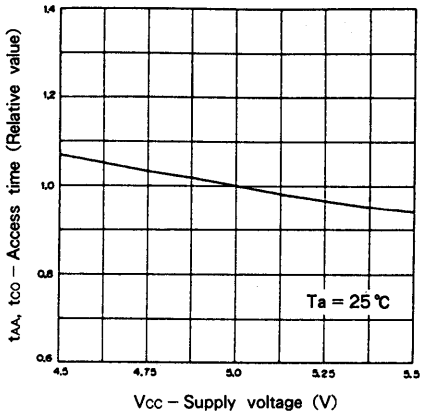
Standby current vs. Supply voltage



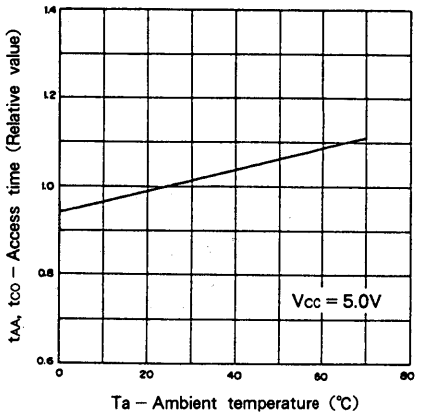
Standby current vs. Ambient temperature



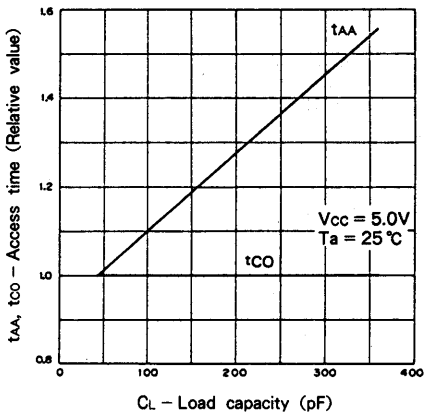
Access time vs. Supply voltage



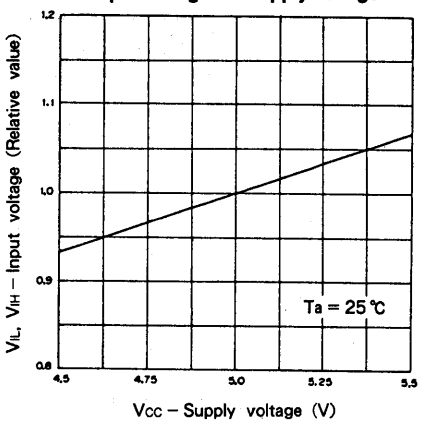
Access time vs. Ambient temperature



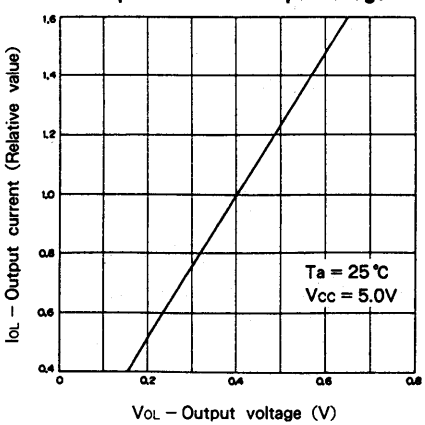
Access time vs. Load capacity



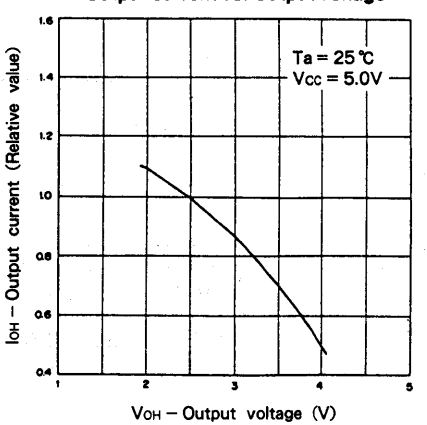
Input voltage vs. Supply voltage



Output current vs. Output voltage



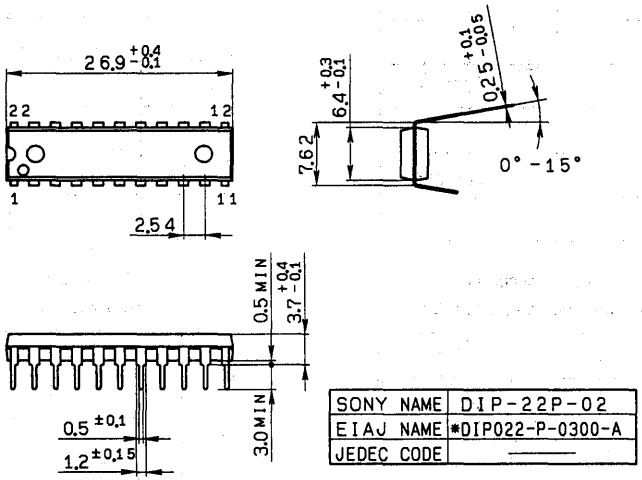
Output current vs. Output voltage



3

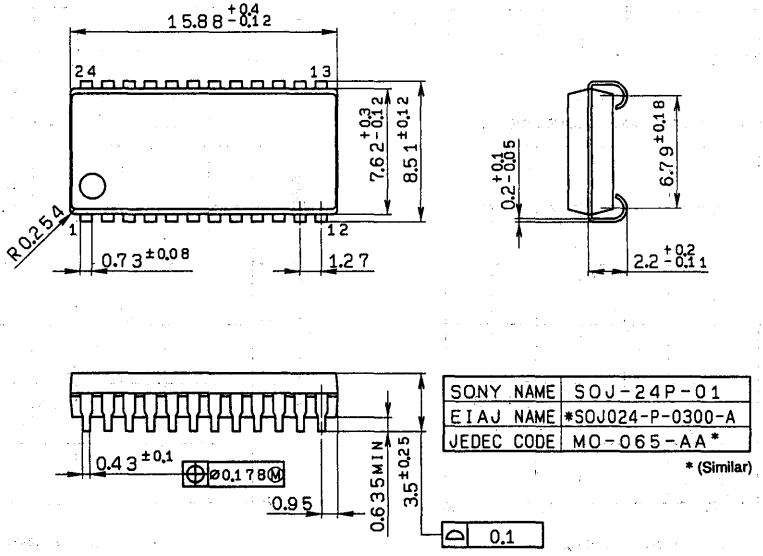
Package Outline Unit : mm

CXK5466P 22 pin DIP (Plastic) 300mil 1.3g



SONY NAME	DIP-22P-02
EIAJ NAME	*DIP022-P-0300-A
JEDEC CODE	

CXK5466J 24 pin SOJ (Plastic) 300mil 0.7g



SONY NAME	SOJ-24P-01
EIAJ NAME	*SOJ024-P-0300-A
JEDEC CODE	MO-065-AA*

* (Similar)

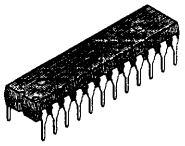
16,384-word × 4-bit High Speed CMOS Static RAM

Description

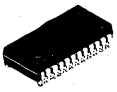
CXK5465P/J are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

These devices feature Output Enable ($\overline{OE}$) to enhance their flexibility in high-speed memory applications.

CXK5465P
24 pin DIP (Plastic)



CXK5465J
24 pin SOJ (Plastic)



Features

- Fast access time :
  - CXK5465P/J-25 25ns (Max.)
  - CXK5465P/J-30 30ns (Max.)
  - CXK5465P/J-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Output Enable ($\overline{OE}$) control available.
- Equal access and cycle time.
- Common data input and output : three-state output.
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 24 pin plastic DIP
  300mil 24 pin plastic SOJ

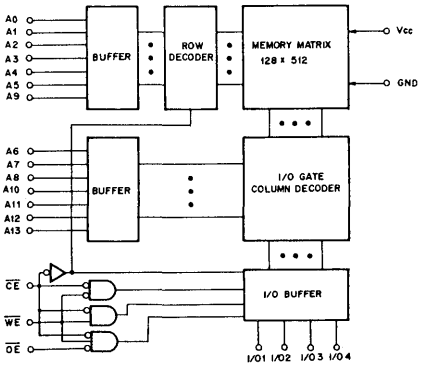
Function

16,384-word × 4-bit static RAM

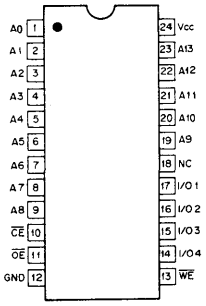
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

3

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature	Tsolder	260 • 10	℃ • sec
Allowable power dissipation	P_D	1.0	W

* V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*2	—	0.8	V

*1. V_{CC} = 5V, Ta = 25℃

*2. V_{IL} = − 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	−25/30/35			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN} = GND to Vcc	−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or OE = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc	−1	—	1	μA
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA V_{IN} = V_{IH}/V_{IL}	—	25	45	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100% I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V	—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

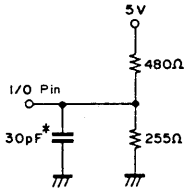
AC characteristics

• AC test conditions

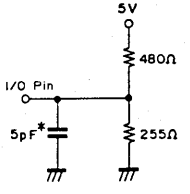
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

● Read cycle

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output enable to output valid	t_{OE}	—	12	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z	t_{HZ}*	0	10	0	15	0	15	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	10	0	10	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	25	ns

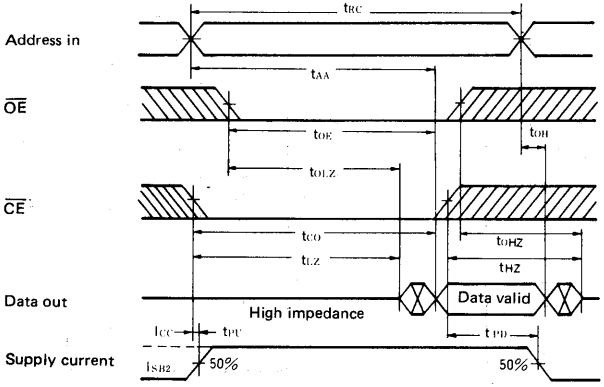
● Write cycle

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	10	0	15	ns

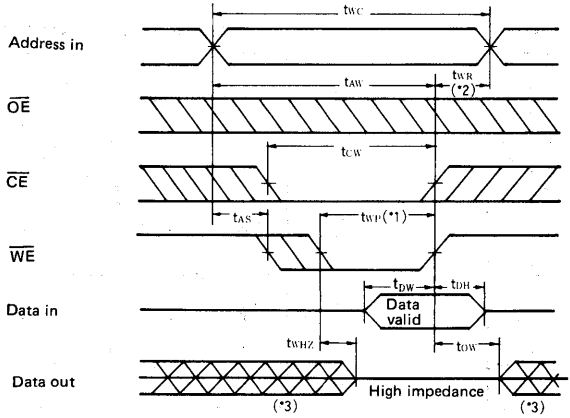
* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

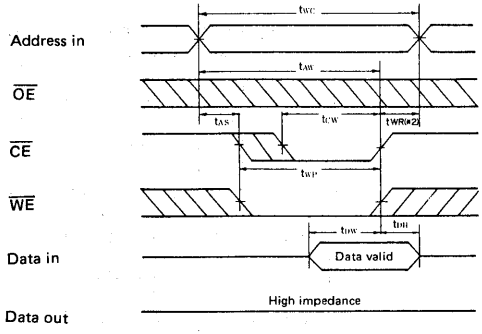
• Read cycle : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



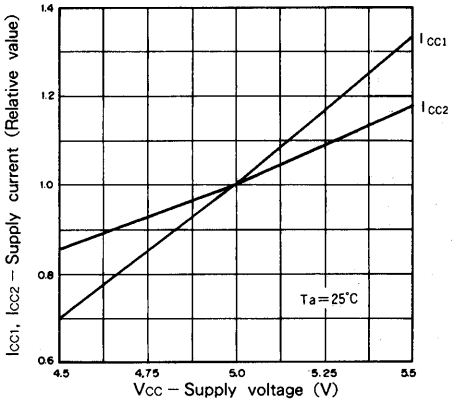
***Note)**

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the rising of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.
3. While I/O pins are in output state, a data input voltage of a phase opposite to the output must not be applied.

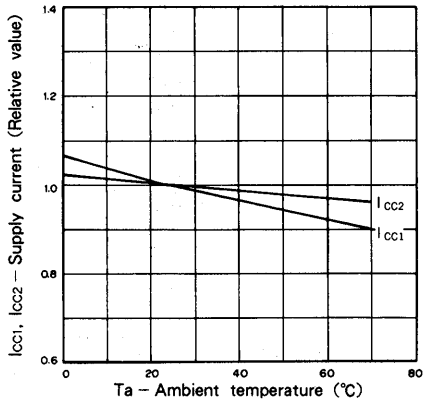
3

Example of Representative Characteristics

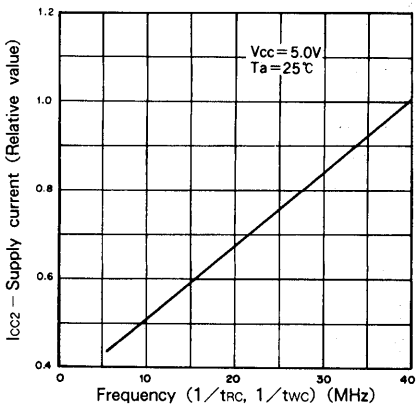
Supply current vs. Supply voltage



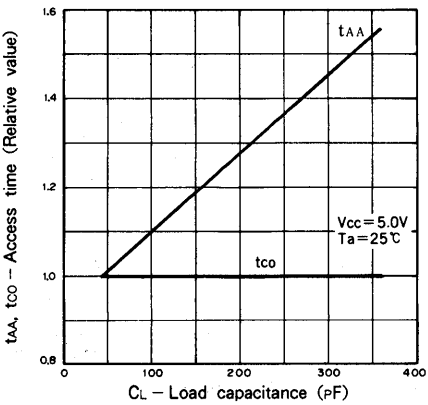
Supply current vs. Ambient temperature



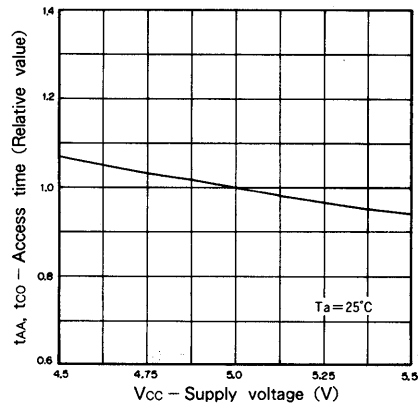
Supply current vs. Frequency



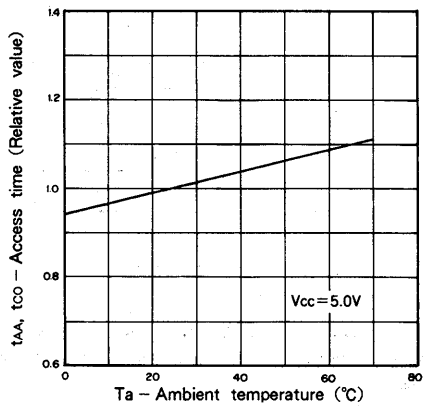
Access time vs. Load capacitance



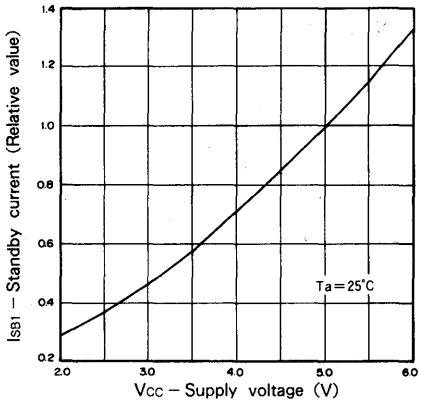
Access time vs. Supply voltage



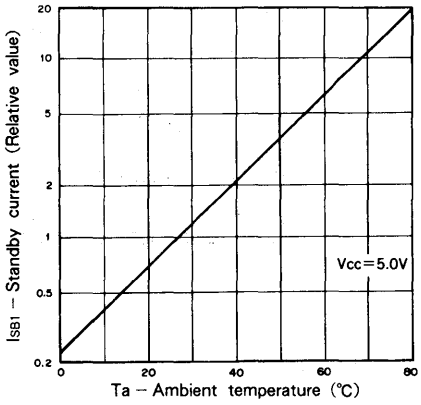
Access time vs. Ambient temperature



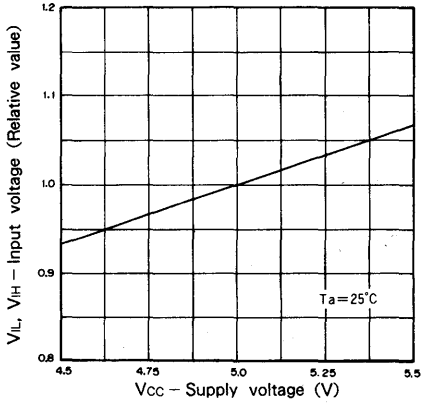
Standby current vs. Supply voltage



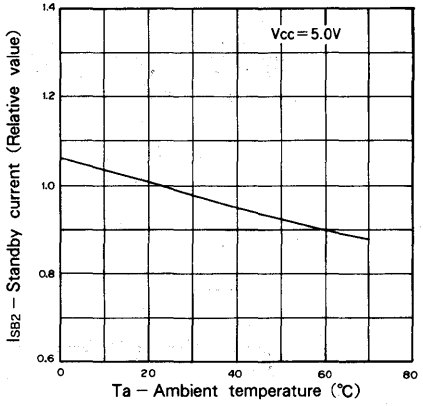
Standby current vs. Ambient temperature



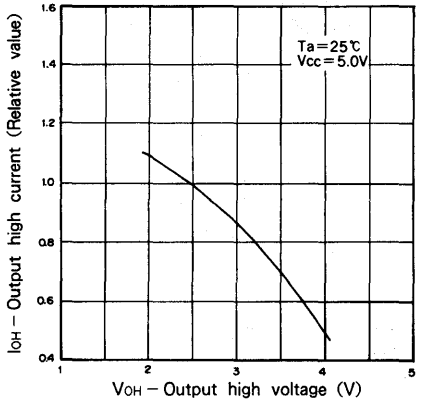
Input voltage level vs. Supply voltage



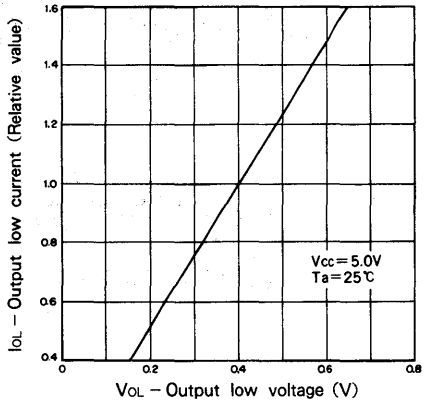
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



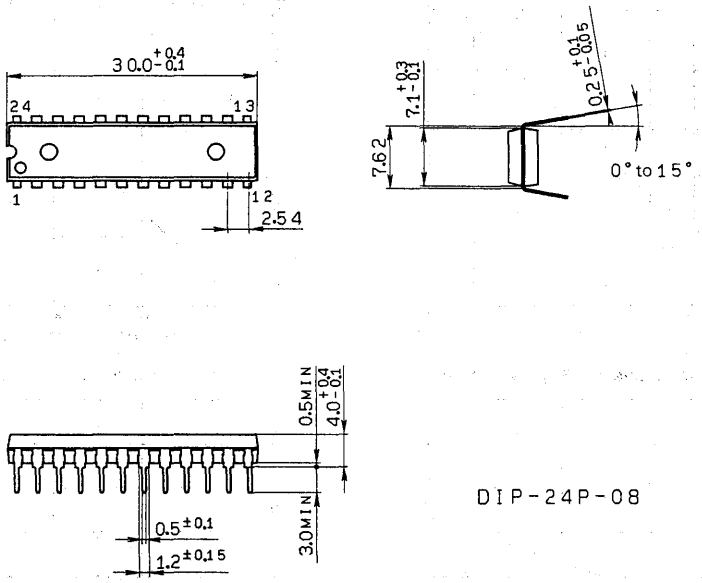
Output low current vs. Output low voltage



3

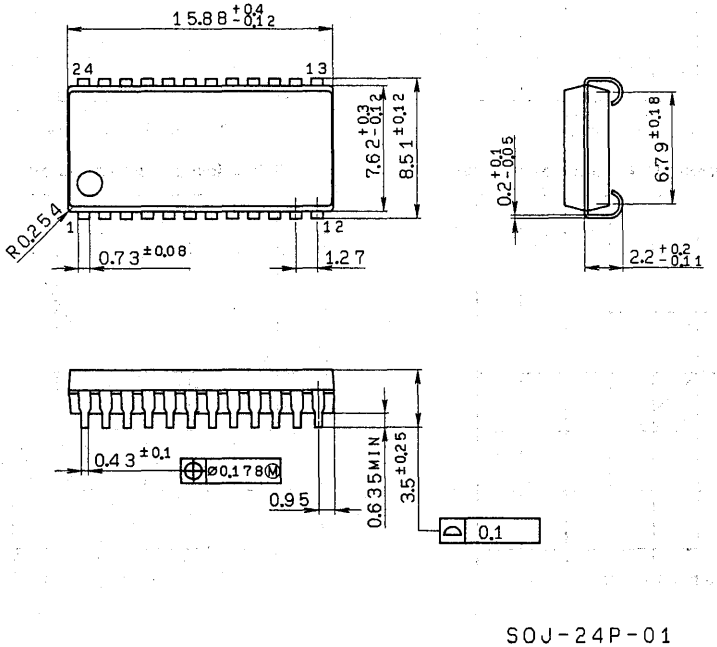
Package Outline Unit : mm

CXK5465P 24 pin DIP (Plastic) 300mil 1.5g



DIP-24P-08

CXK5465J 24 pin SOJ (Plastic) 300mil 0.7g



SOJ-24P-01

16,384 word × 4-bit High Speed CMOS Static RAM

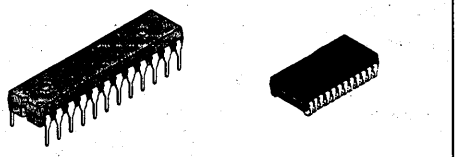
Description

CXK5467P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal. An output enable pin controls the output.

CXK5467P
24 pin DIP (Plastic)

CXK5467J
24 pin SOJ (Plastic)



Features

- Fast access time :
  CXK5467P/J-15 15ns (Max.)
  CXK5467P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
  During operation
- Single + 5V supply : + 5V ± 10%
- Fully static memory
  ···No clock or timing strobe required
- Output Enable ($\overline{OE}$) control available
- Equal access and cycle time
- Common data input and output :
  three-state output
- Directly TTL compatible : All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 24 pin plastic DIP
  300 mil 24 pin plastic SOJ

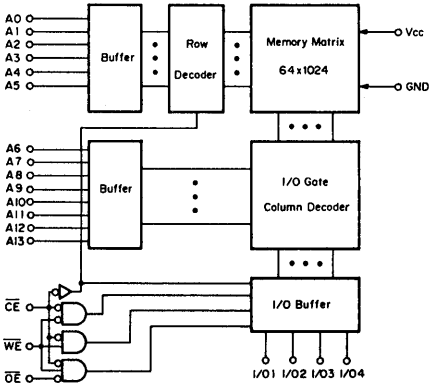
Functions

16,384 word × 4-bit static RAM

Structure

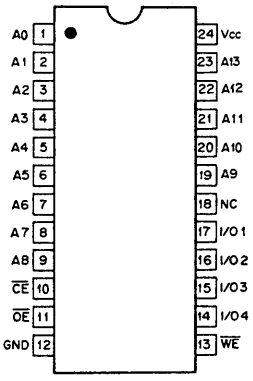
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+ 5V power supply
GND	Ground
NC	No connection

3

E89521B02 – ST

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ Min. = −3.5V for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data output	I_{CC1}, I_{CC2}
L	×	L	Write	Data input	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

*1) V_{CC} = 5V, Ta = 25°C

*2) V_{IL} Min. = −3.0V for pulse width less than 20ns.

DC Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leak current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, V_{IN} = V_{IH} or V_{IL}		—	30	55	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100%, I_{OUT} = 0mA	−15	—	95	150	mA
			−20	—	90	140	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V		—	—	1	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL} Cycle = Min.		—	—	85	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

* Vcc = 5.0V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

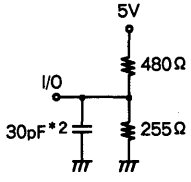
Note) This parameter is sampled and is not 100% tested.

• AC test conditions

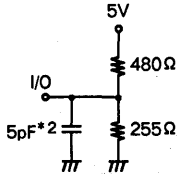
(Vcc = 5V ± 10%*1, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*3



*1 Vcc = 5V ± 5% for CXK5467P/J-15
*2 including scope and jig capacitance
*3 for t_{LZ}, t_{OLZ}, t_{HZ}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

3

• **Read cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	15	—	20	ns
Output enable to output valid	t_{OE}	—	8	—	10	ns
Output hold from address change	t_{OH}	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	2	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	2	—	3	—	ns
Chip disable to output in high Z	t_{HZ}*	0	6	0	8	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	6	0	8	ns
Chip enable to power up time	t_{PU}	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at ±200mV (See Fig. 1)

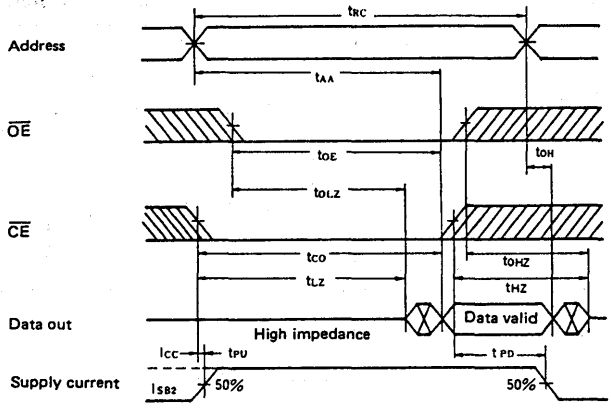
• **Write cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	15	—	20	—	ns
Address valid to end of write	t_{AW}	13	—	18	—	ns
Chip enable to end of write	t_{CW}	13	—	18	—	ns
Data to write time overlap	t_{DW}	8	—	11	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	13	—	18	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output active from end of write	t_{OW} *	2	—	3	—	ns
Write to output in high Z	t_{WHZ}	0	5	0	7	ns

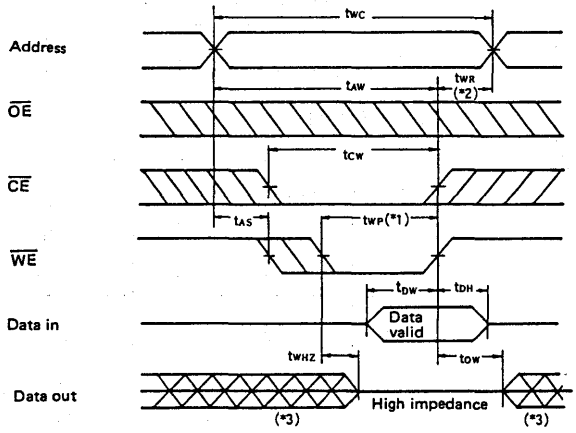
* Transition is tested by means of load conditions (2), from stationary condition at ±200mV (See Fig. 1)

Timing Waveform

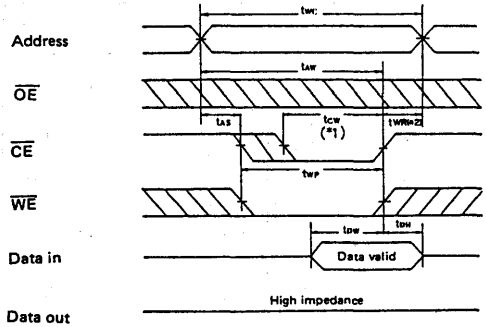
• Read cycle : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



*1) Write is performed during the low overlap of $\overline{CE}$ and $\overline{WE}$.

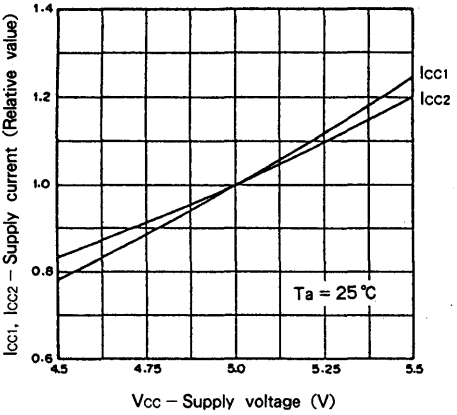
*2) t_{WR} is measured from the rising of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.

*3) While I/O pins are in output state, a data input voltage of a phase opposite to the output must not be applied.

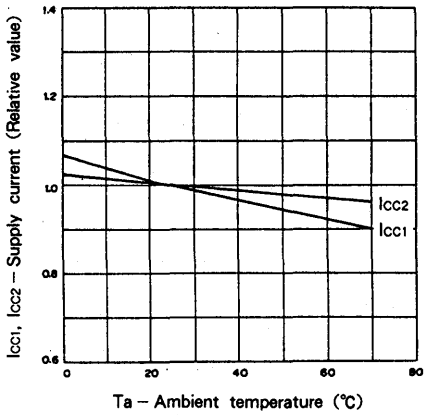
3

Example of Represeutative Characteristics

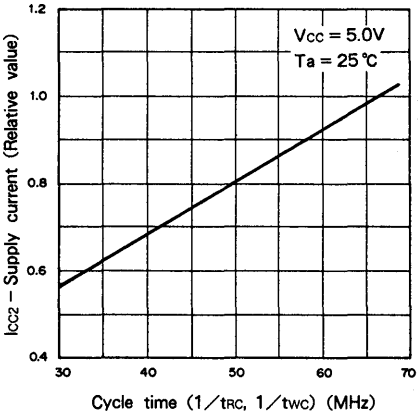
Supply current vs. Supply voltage



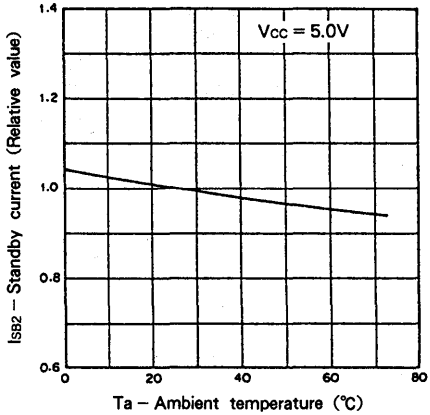
Supply current vs. Ambient temperature



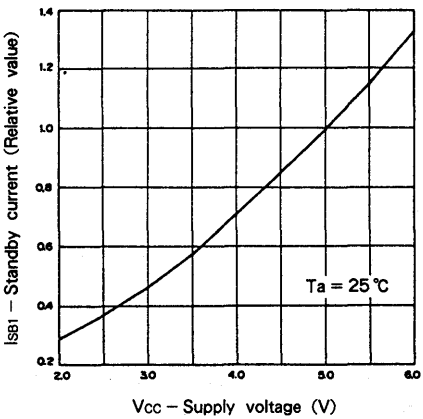
Supply current vs. Cycle time



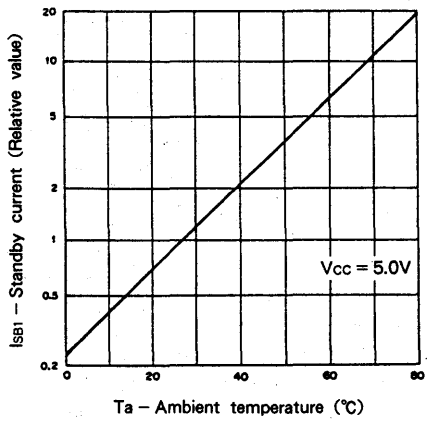
Standby current vs. Ambient temperature



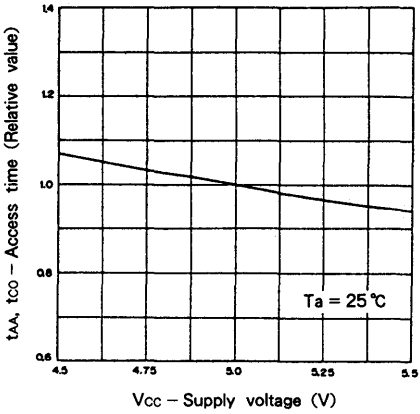
Standby current vs. Supply voltage



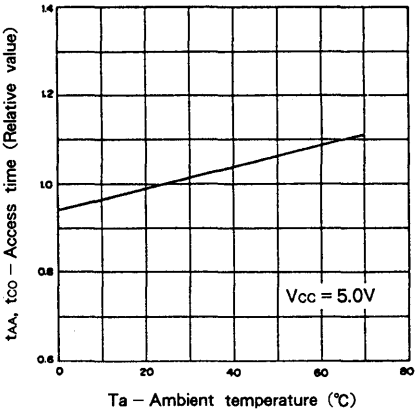
Standby current vs. Ambient temperature



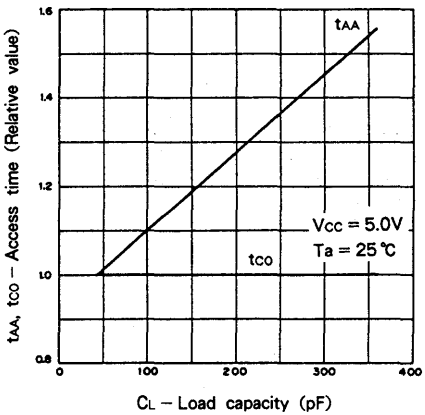
Access time vs. Supply voltage



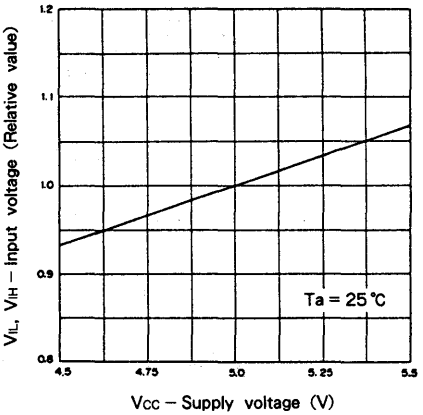
Access time vs. Ambient temperature



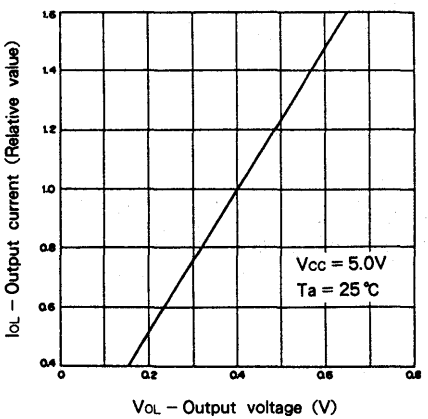
Access time vs. Load capacity



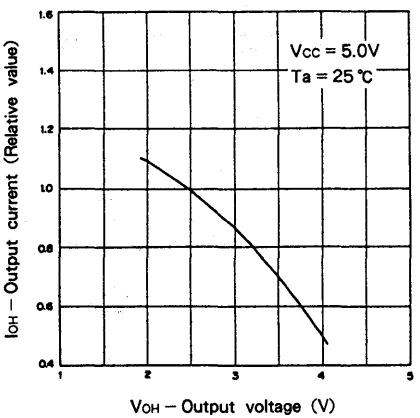
Input voltage vs. Supply voltage



Output current vs. Output voltage



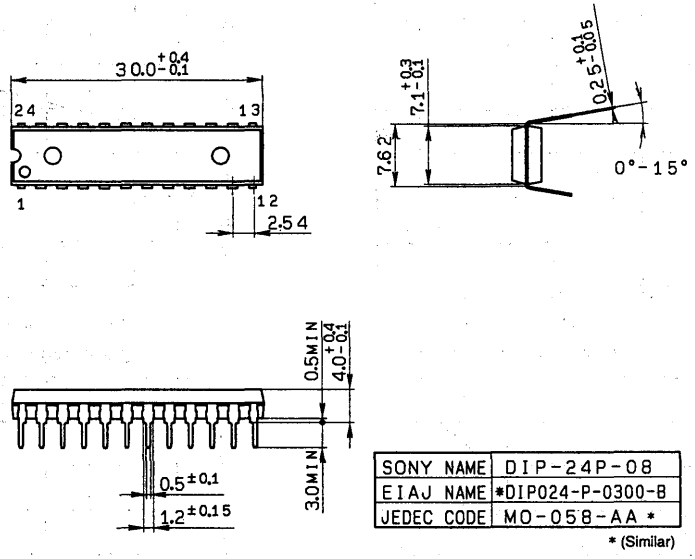
Output current vs. Output voltage



3

Package Outline Unit : mm

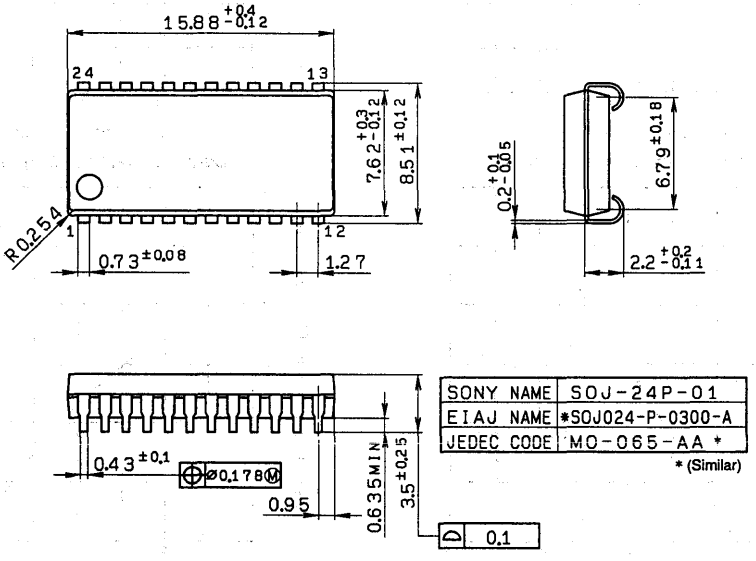
CXK5467P 24pin DIP (Plastic) 300mil 1.5g



SONY NAME	DIP-24P-08
EIAJ NAME	*DIP024-P-0300-B
JEDEC CODE	MO-058-AA *

* (Similar)

CXK5467J 24pin SOJ (Plastic) 300mil 0.7g



SONY NAME	SOJ-24P-01
EIAJ NAME	*SOJ024-P-0300-A
JEDEC CODE	MO-065-AA *

* (Similar)

SONY CXK5863AP/AJ -20/25/30

8192 word × 8-bit High Speed CMOS Static RAM

Description

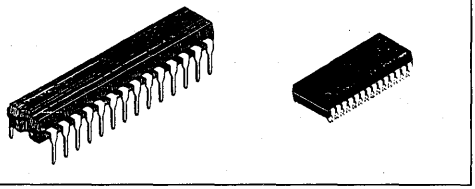
CXK5863AP/AJ are 65,536 bits high speed CMOS static RAMS organized as 8,192 words by 8-bits and operate from a single 5V supply. These devices are suitable for use in high speed applications such as cash memory.

Features

- Fast access time 20ns/25ns/30ns (Max.)
- Low power operation 250mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory··· No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Full CMOS.
- Compatible with various types of packages
  CXK5863AP 300mil 28pin DIP package
  CXK5863AJ 300mil 28pin SOJ package

CXK5863AP
28 pin DIP (Plastic)

CXK5863AJ
28 pin SOJ (Plastic)



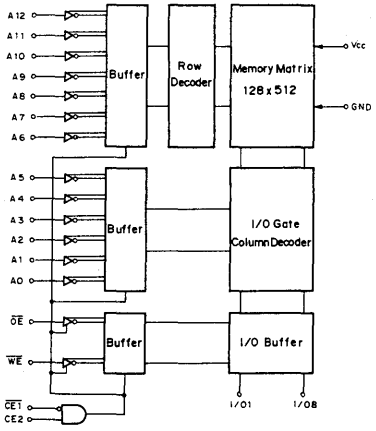
Structure

Silicon gate CMOS IC

Function

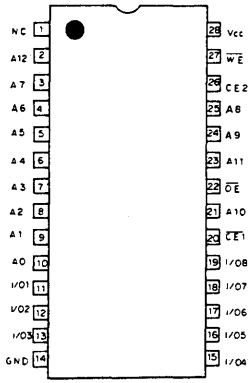
8192 word × 8-bit static RAM

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

3

E89704A02 – ST

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ = −3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test condition	−20			−25/−30			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−1	—	1	−1	—	−1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	−1	—	1	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	—	50	80	—	50	80	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	—	95	130	—	70	90	mA
Standby current	I_{SB1}	$\overline{CE1}$ ≧ V_{CC} − 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	—	1	—	—	1	mA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{IN} = V_{IL} or V_{IH}	—	10	25	—	10	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

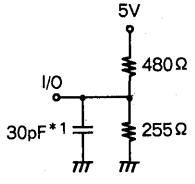
AC characteristics

- **AC test conditions**

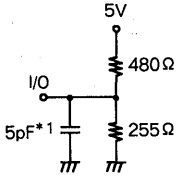
(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2) *2



*1 including scope and jig capacitance
*2 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	−20		−25		−30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	20	—	25	—	30	—	ns
Address access time	t_{AA}	—	20	—	25	—	30	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	20	—	25	—	30	ns
Chip enable access time (CE2)	t_{CO2}	—	20	—	25	—	30	ns
Output enable to output valid	t_{OE}	—	10	—	12	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}*, t_{LZ2}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	0	10	0	12	0	12	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	8	0	10	0	10	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	20	—	20	—	20	ns

2) Write cycle

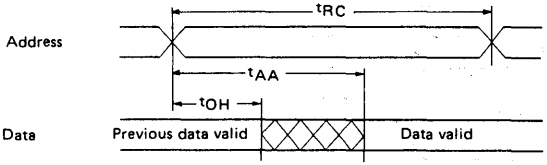
Item	Symbol	−20		−25		−30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	20	—	25	—	30	—	ns
Address valid to end of write	t_{AW}	15	—	20	—	20	—	ns
Chip enable to end of write	t_{CW}	15	—	20	—	20	—	ns
Data to write time overlap	t_{DW}	10	—	12	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	20	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	10	0	12	0	12	ns

* Transition is measured ±500mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

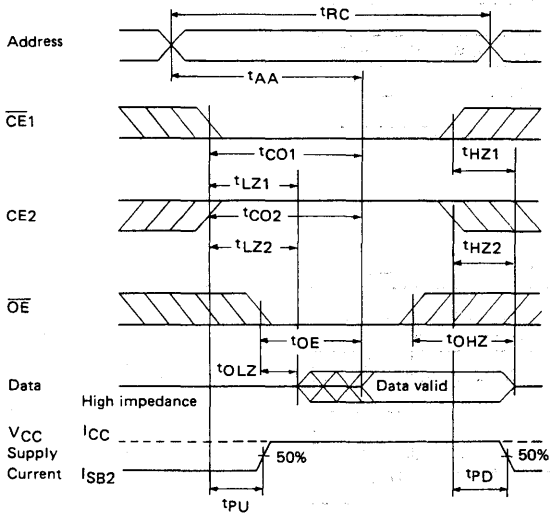
Timing Waveform

1) Read cycle

- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, CE2 = V_{IH}, $\overline{WE} = V_{IH}$

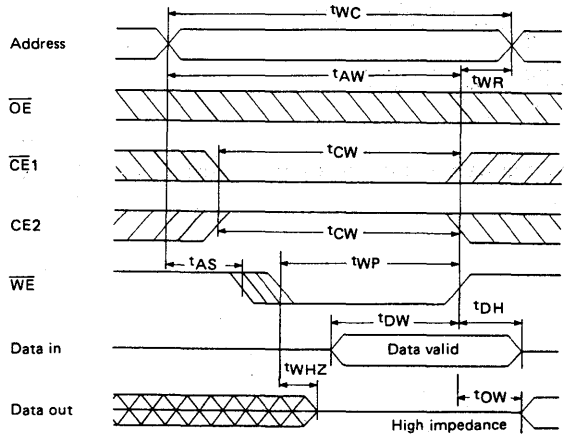


- Read cycle (2) : $\overline{WE} = V_{IH}$



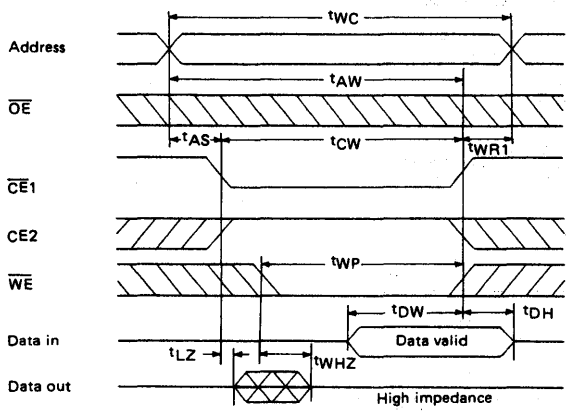
2) Write cycle

- Write cycle (1) : $\overline{WE}$ control

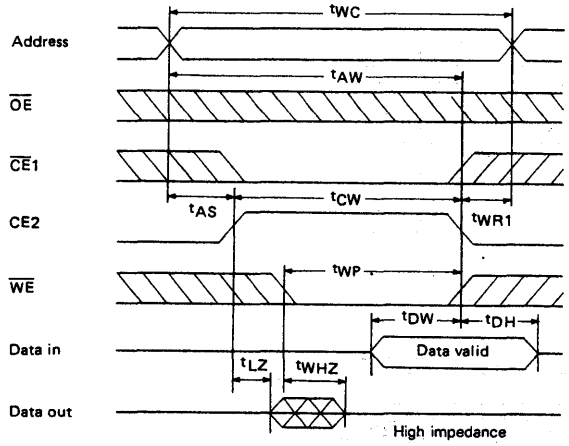


3

• Write cycle (2) : $\overline{CE1}$ control



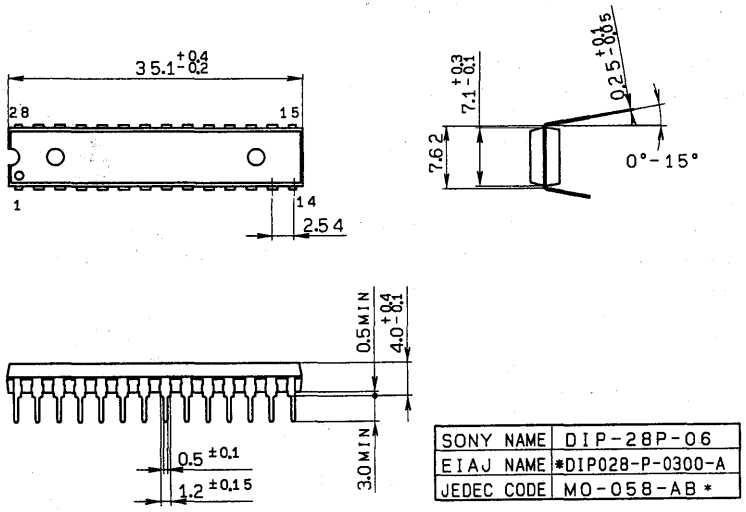
• Write cycle (3) : CE2 control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

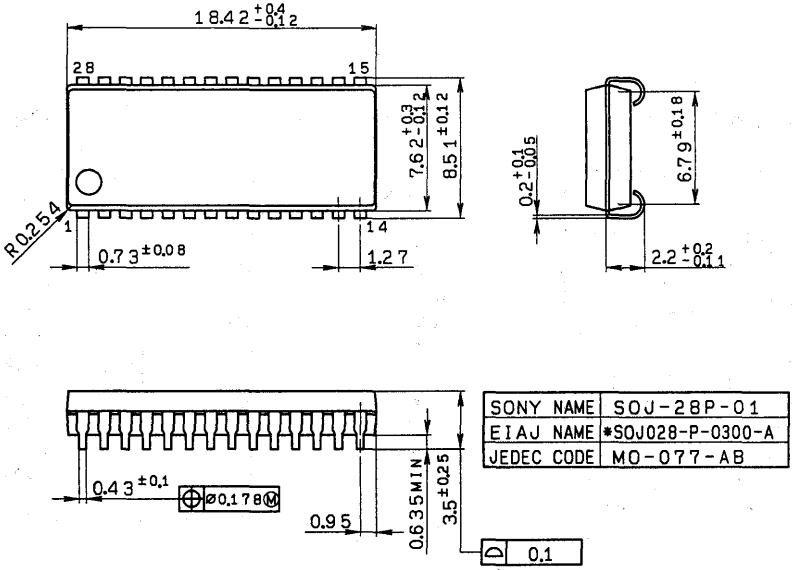
CXK5863AP 28pin DIP (Plastic) 300mil 2.0g



SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB*

* (Similar)

CXK5863AJ 28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB

SONY CXK5863P/M/J 25/30/35

8192-word × 8-bit High Speed CMOS Static RAM

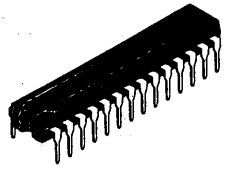
Description

CXK5863P/M/J are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

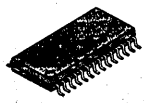
Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μW (Typ.)
- Low power operation 150mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory···No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.
- Available in 28 pin 300mil DIP, 450mil SOP, 300mil SOJ.

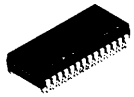
CXK5863P
28 pin DIP (Plastic)



CXK5863M
28 pin SOP (Plastic)



CXK5863J
28 pin SOJ (Plastic)



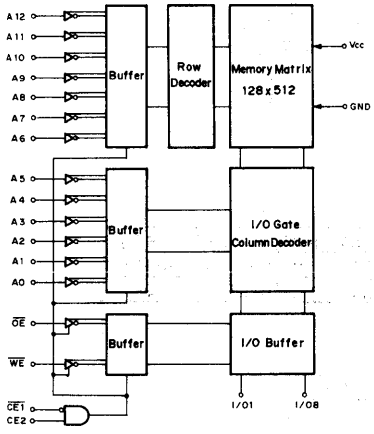
Structure

Silicon gate CMOS IC

Function

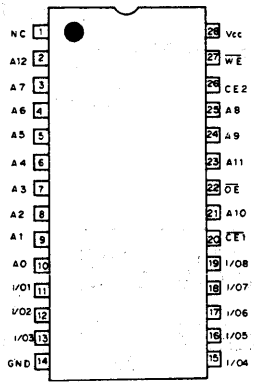
8192-word × 8-bit static RAM

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

E89739 – ST

Absolute Maximum Ratings Ta = 25℃, GND = 0V

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5* to + 7.0	V
Input voltage	V_{IN}		− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK5863P/J	1.0	W
		CXK5863M	0.7	W
Operating temperature	Topr		0 to + 70	℃
Storage temperature	Tstg		− 55 to + 150	℃
Soldering temperature	Tsolder		260 • 10	℃ • sec

***Note)** V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions Ta = 0 to + 70℃, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

***Note)** V_{IL} = − 3.0V Min. for pulse width less than 20ns.

3

Electrical Characteristics

DC and operating characteristics

V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70℃

Item	Symbol	Test condition	−25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1}$ ≧ V_{CC} − 0.2V or CE2 ≦ 0.2V V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	1	100	μA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{IN} = V_{IL} or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, Ta = 25℃

I/O capacitance

Ta = 25℃, f = 1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	10	pF

Note) This parameter is sampled and is not 100% tested.

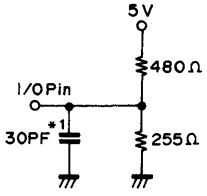
AC characteristics

● **AC test conditions**

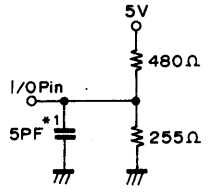
V_{CC} = 5V ± 10%, Ta = 0 to +70℃

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



* 1. including scope and jig capacitance

* 2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t_{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t_{OE}	—	15	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}* t_{LZ2}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}* t_{HZ2}*	0	15	0	15	0	20	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	13	0	13	0	15	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	20	—	20	—	20	ns

• **Write cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	13	0	13	0	15	ns

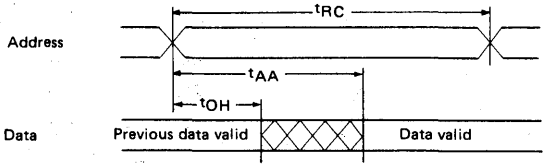
* Transition is measured ±500mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

3

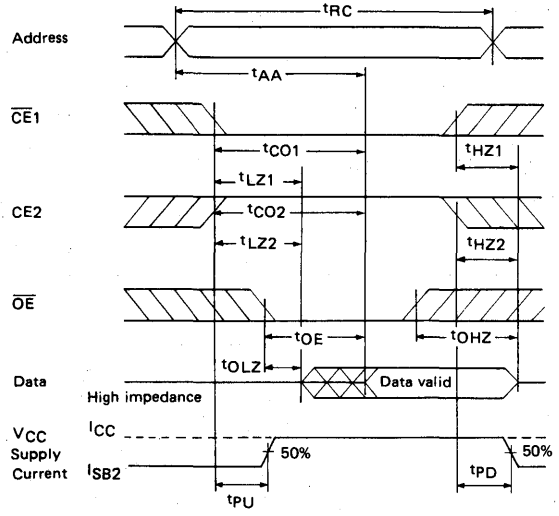
Timing Waveform

1) Read cycle

• Read cycle No. 1 : [$\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}]

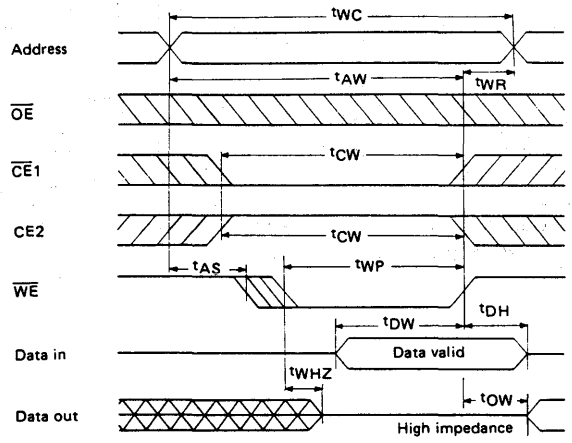


• Read cycle No. 2 : [$\overline{WE}$ = V_{IH}]

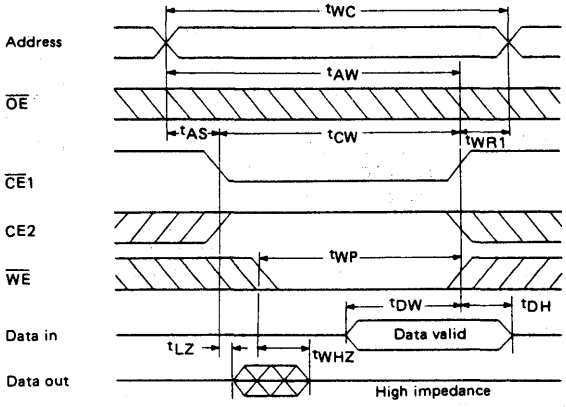


2) Write cycle

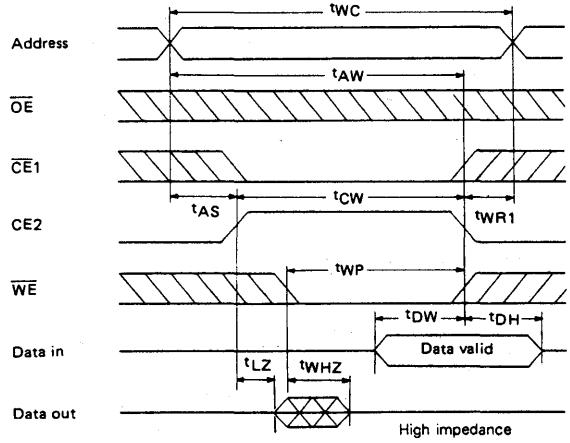
• Write cycle No. 1 : [$\overline{WE}$ control]



• Write cycle No. 2 : [$\overline{CE1}$ control]



• Write cycle No. 3 : [CE2 control]



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

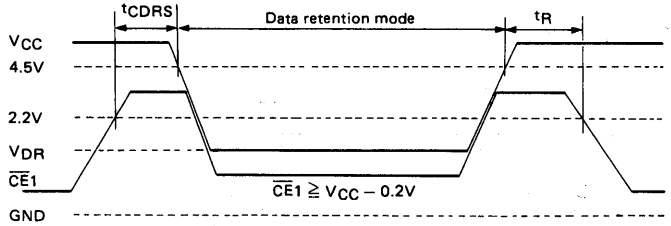
3

Data Retention Characteristics Ta = 0 to + 70°C

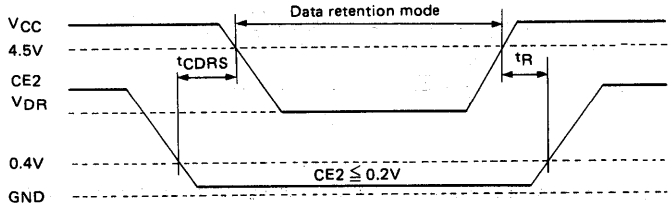
Item	Symbol	Test condition	−25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V *1	—	0.5	50	µA
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V *1	—	1.0	100	µA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

*1 $\overline{CE1} \geqq V_{CC} - 0.2V$ or $CE2 \leqq 0.2V$, $V_{IN} \geqq V_{CC} - 0.2V$ or $V_{IN} \leqq 0.2V$
*2 t_{RC} : Read cycle time

Data Retention Waveform (1) : [$\overline{CE1}$ control]

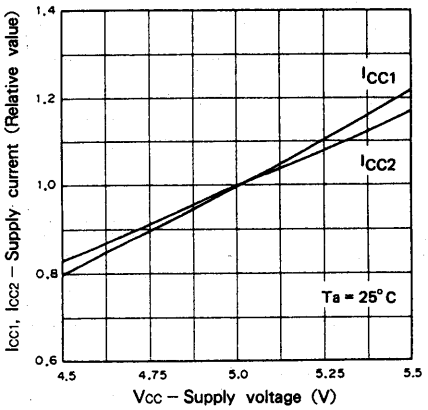


Data Retention Waveform (2) : [CE2 control]

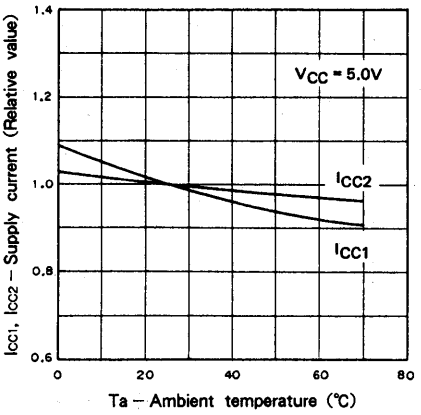


Example of Representative Characteristics

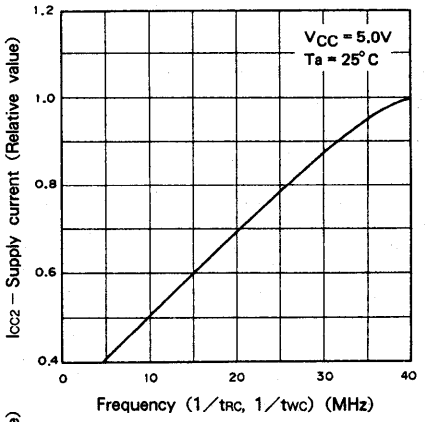
Supply current vs. Supply voltage



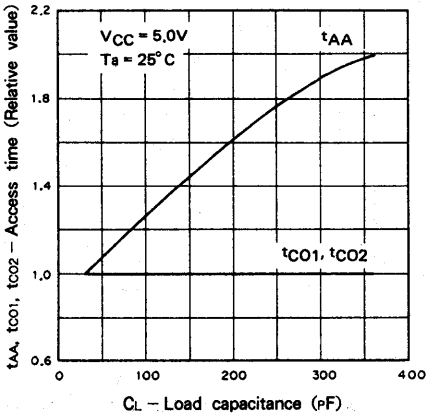
Supply current vs. Ambient temperature



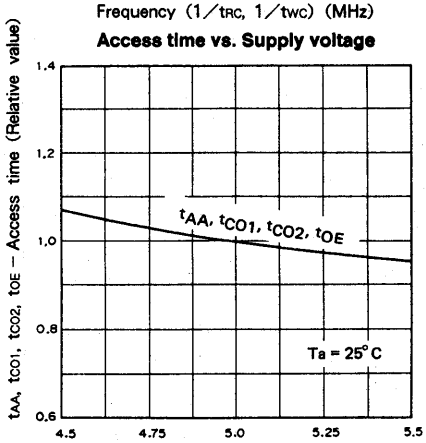
Supply current vs. Frequency



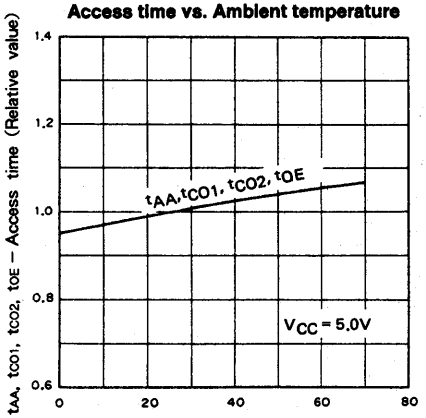
Access time vs. Load capacitance



Access time vs. Supply voltage

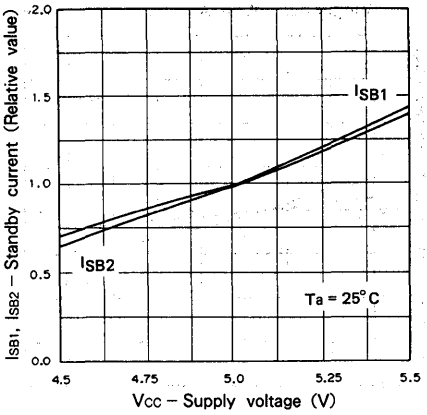


Access time vs. Ambient temperature

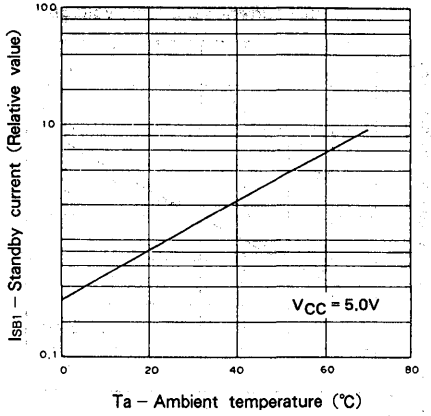


3

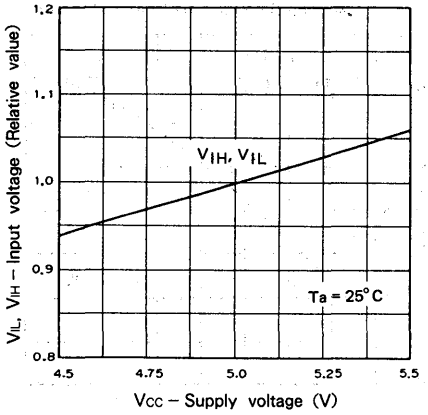
Standby current vs. Supply voltage



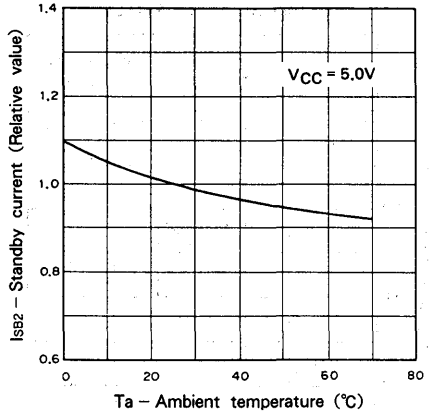
Standby current vs. Ambient temperature



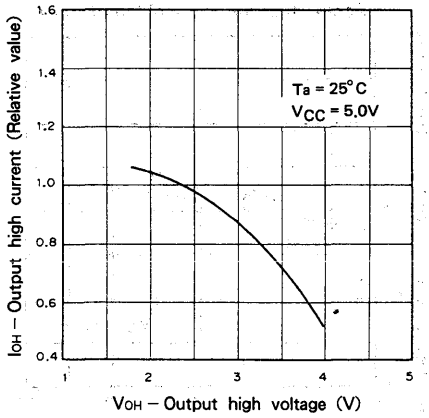
Input voltage vs. Supply voltage



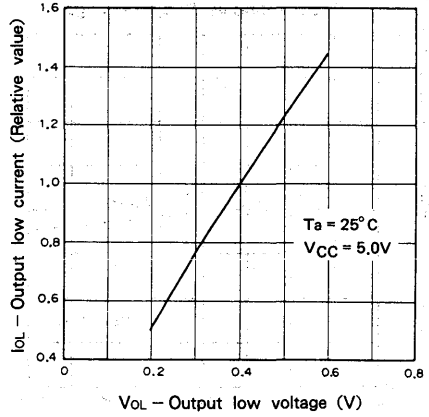
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

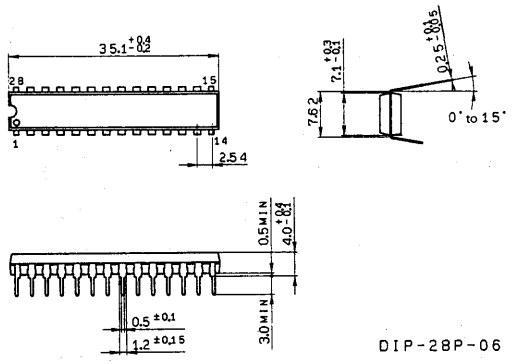


Output low current vs. Output low voltage



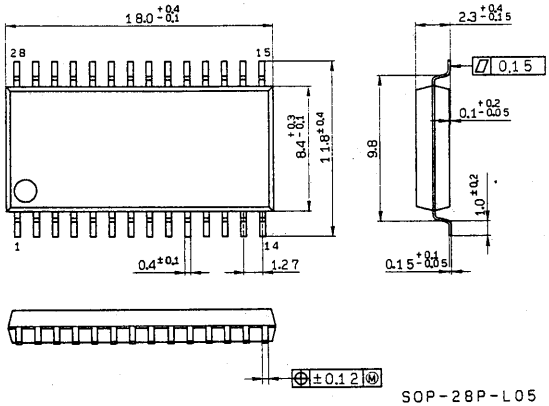
Package Outline Unit : mm

CXK5863P 28 pin DIP (Plastic) 300mil 2.0g



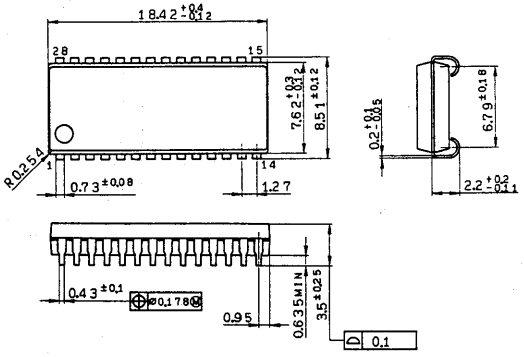
DIP-28P-06

CXK5863M 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5863J 28 pin SOJ (Plastic) 300mil 0.8g



SOJ-28P-01

3

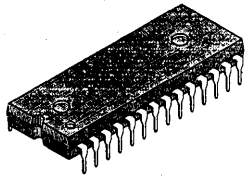
SONY CXK5864BP/BSP/BM 70L/10L/12L/ 70LL/10LL/12LL

8,192-word × 8-bit High Speed CMOS Static RAM

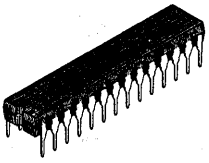
Description

CXK5864BP/BSP/BM are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8 bits and operates from a single 5V supply. These IC are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

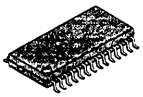
CXK5864BP
28 pin DIP (Plastic)



CXK5864BSP
28 pin DIP (Plastic)



CXK5864BM
28 pin SOP (Plastic)



Features

- Fast access time (Access time)
  CXK5864BP/BSP/BM-70L, 70LL 70ns(Max.)
  CXK5864BP/BSP/BM-10L, 10LL 100ns(Max.)
  CXK5864BP/BSP/BM-12L, 12LL 120ns(Max.)
- Low power operation :
  CXK5864BP/BSP/BM-70LL, 10LL, 12LL ;
  Standby/Operation : 5 μW (Typ.) /40mW (Typ.)
  CXK5864BP/BSP/BM-70L, 10L, 12L ;
  Standby/Operation : 10 μW (Typ.) /40mW (Typ.)
- Single power supply 5V : +5V ± 10%
- Fully static memory ··· No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs
- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

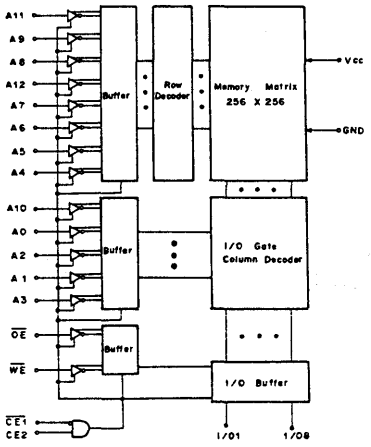
Function

8,192-word × 8-bit static RAM

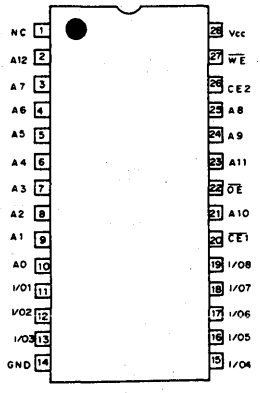
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

E89720A01 – ST

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to + 7.0	V
Input voltage	V_{IN}		− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK5864BP/BSP	1.0	W
		CXK5864BM	0.7	
Operating temperature	Topr		0 to + 70	℃
Storage temperature	Tstg		− 55 to + 150	℃
Soldering temperature • time	Tsolder		260 • 10	℃ • sec

* V_{IN}, $V_{I/O}$ = − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		−70L/10L/12L −70LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN} = GND to Vcc		−500	—	500	nA
Output leak current	I_{LO}	$V_{I/O}$ = GND to Vcc $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		−500	—	500	nA
Operating supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	8	15	mA
Average operating current	I_{CC2}	Min. cycle Duty = 100%, I_{OUT} = 0mA		—	30	50	mA
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc − 0.2V, CE2 ≧ Vcc − 0.2V	− L	—	2	60	μA
			− LL	—	1	30	
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		—	0.1	2	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V

* Vcc = 5V, Ta = 25°C

Pin capacitance (Ta = 25°C, f = 1MHz)

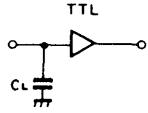
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	10L/10LL/12L/12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL



* C_L includes scope and jig capacitances.

● Read cycle

Item	Symbol	−70L/70LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{CE1}$, CE2)	t_{CO1} t_{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	50	—	60	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1} t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}* t_{HZ2}*	0	30	0	35	0	45	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	35	0	45	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

● Write cycle

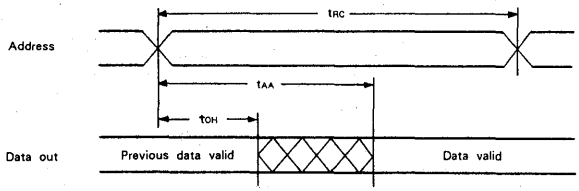
Item	Symbol	−70L/70LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	60	—	80	—	85	—	ns
Chip enable to end of write	t_{CW}	60	—	80	—	85	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	50	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	40	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	30	0	35	0	45	ns

* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

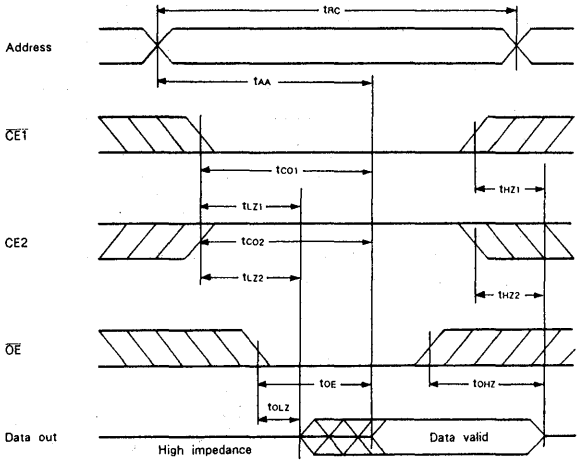
3

Timing Waveform

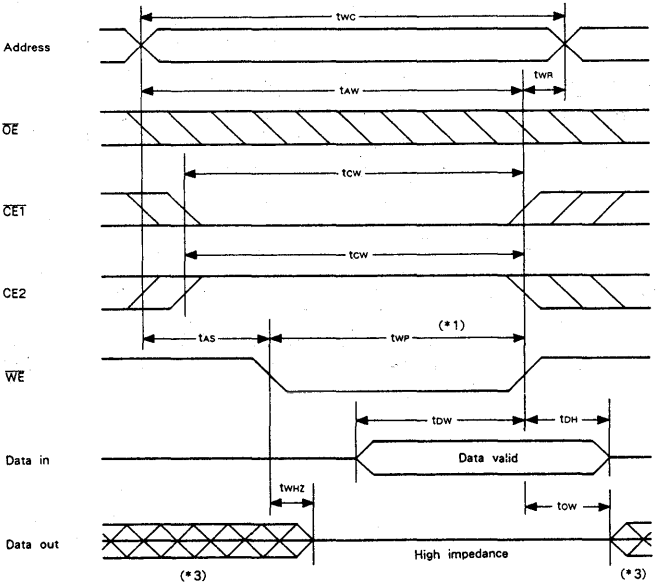
• Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, CE2 = V_{IH}, $\overline{WE} = V_{IH}$



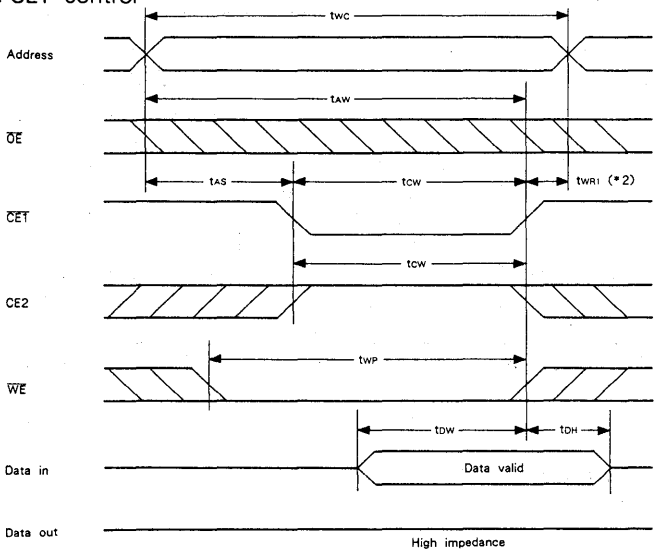
• Read cycle (2) : $\overline{WE} = V_{IH}$



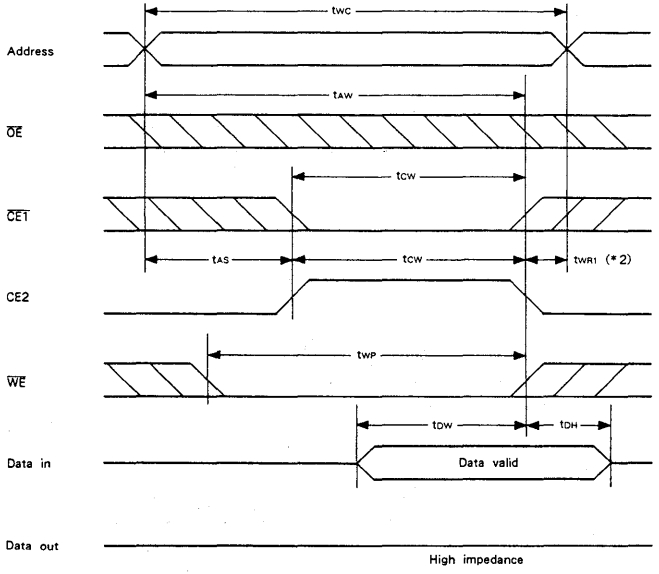
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

*3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

Data Retention Characteristics

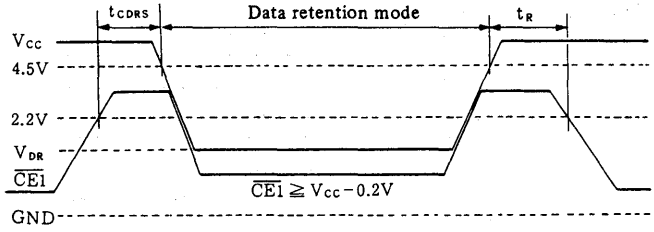
(Ta = 0 to + 70°C)

Item	Symbol	Test conditions		-70L/10L/12L			-70LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	*1 Vcc = 3.0V	Ta = 0°C to 70°C	—	1	35	—	0.5	15	µA
			Ta = 0°C to 40°C	—	—	—	—	—	3	
	I_{CCDR2}	Vcc = 2.0 to 5.5V, *1		—	2	60	—	1	30	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

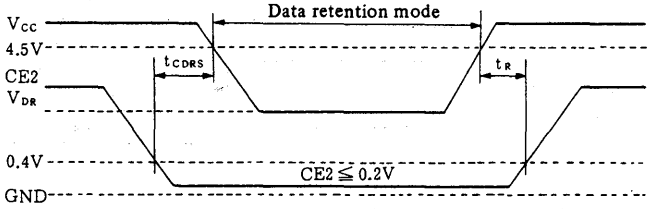
* 1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ [$\overline{CE1}$ Control] or $CE2 \leqq 0.2V$ [CE2 Control]
* 2. t_{RC} : Read cycle time

Data Retention Waveform

1. $\overline{CE1}$ control

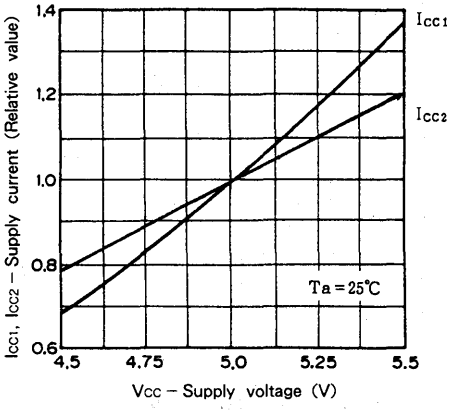


2. CE2 control

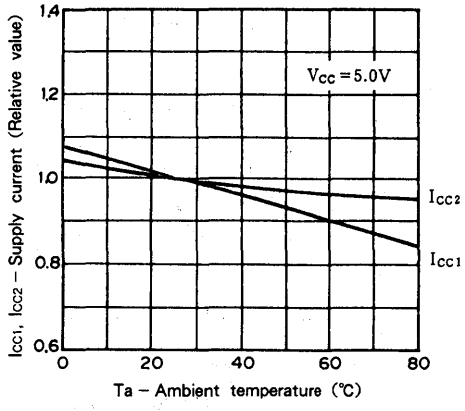


Example of Representative Characteristics

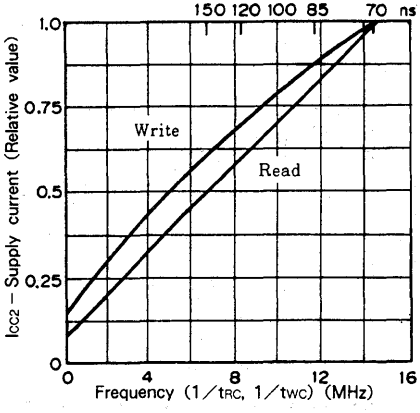
Supply current vs. Supply voltage



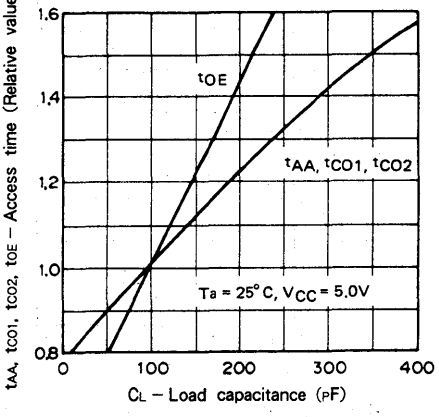
Supply current vs. Ambient temperature



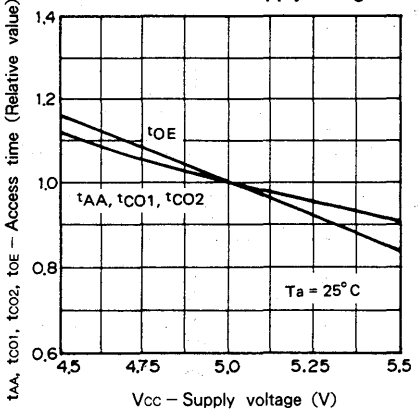
Supply current vs. Frequency



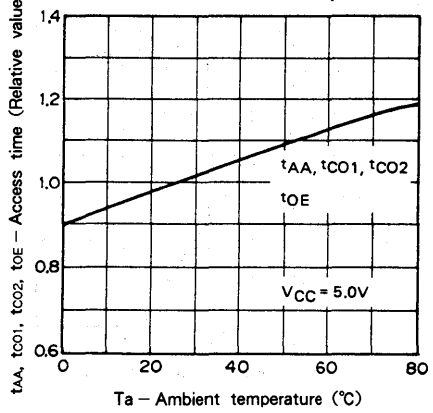
Access time vs. Load capacitance



Access time vs. Supply voltage



Access time vs. Ambient temperature



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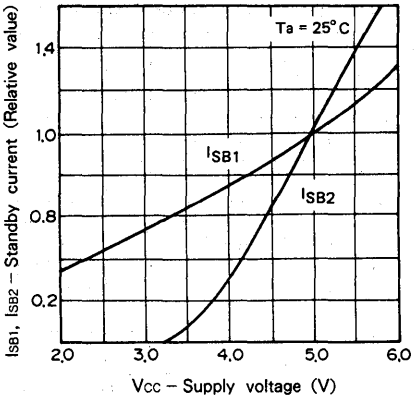
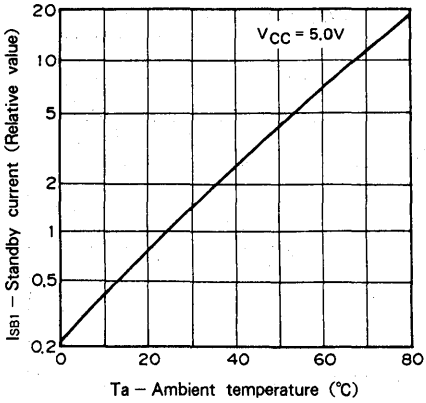
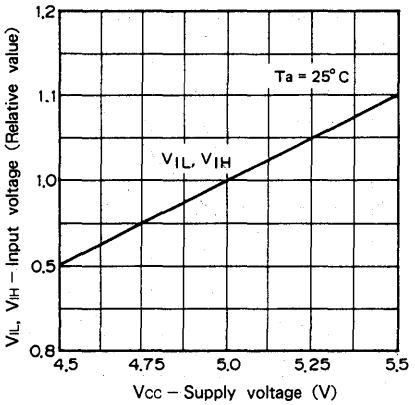
Standby current vs. Supply voltage



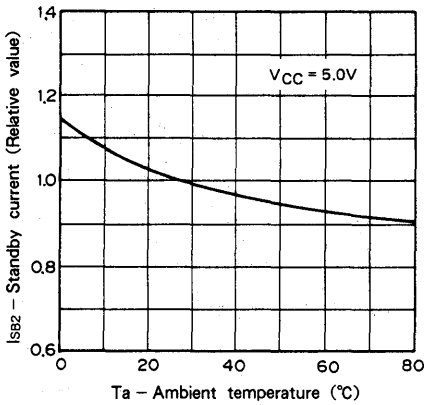
Standby current vs. Ambient temperature



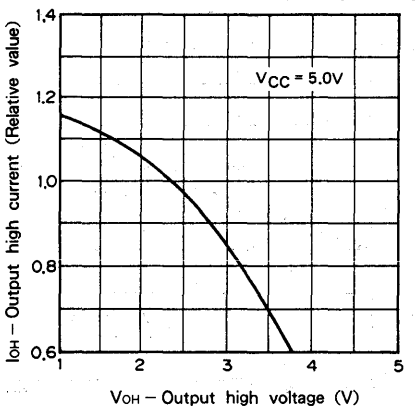
Input voltage level vs. Supply voltage



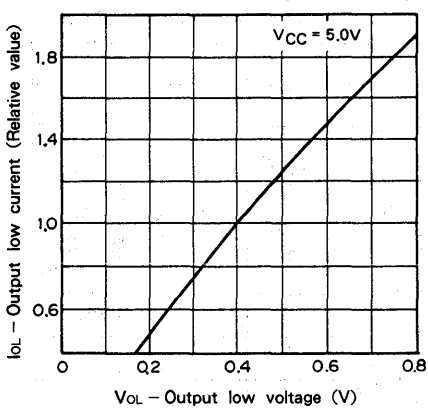
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

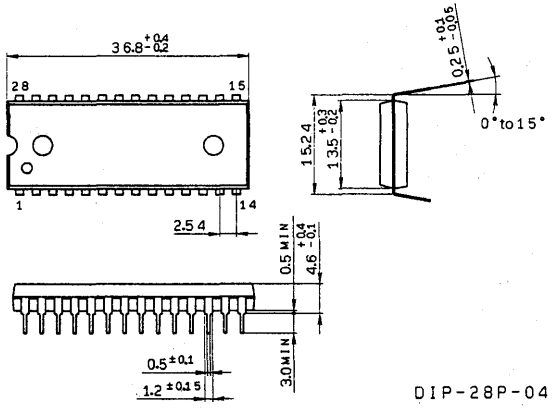


Output low current vs. Output low voltage



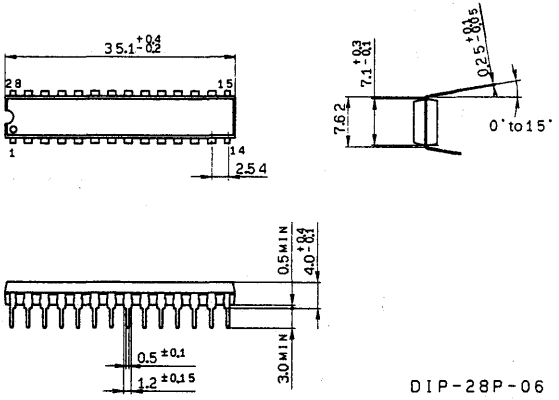
Package Outline Unit : mm

CXK5864BP 28 pin DIP (Plastic) 600mil 4.2g



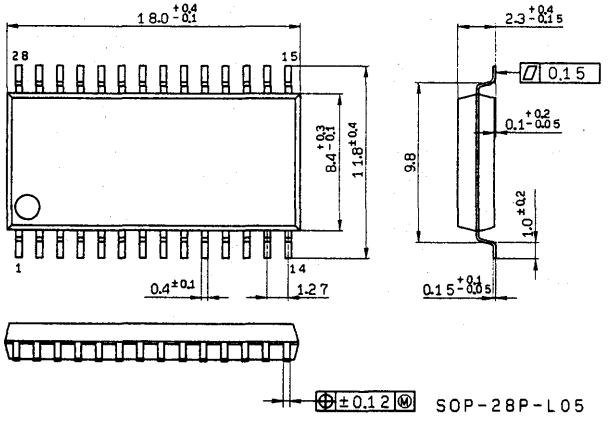
DIP-28P-04

CXK5864BSP 28 pin DIP (Plastic) 300mil 2.0g



DIP-28P-06

CXK5864BM 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

3

8192-word × 9-bit High Speed CMOS Static RAM

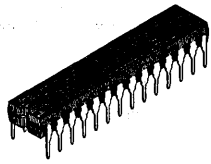
Description

CXK5971P/M/J are 73,728 bits high speed CMOS static RAMs organized as 8,192-word by 9-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

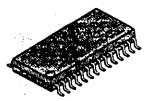
Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μW (Typ.)
- Low power operation 150mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.
- Available in 28 pin 300mil DIP, 450mil SOP and 300 mil SOJ.

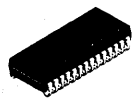
CXK5971P
28 pin DIP (Plastic)



CXK5971M
28 pin SOP (Plastic)



CXK5971J
28 pin SOJ (Plastic)



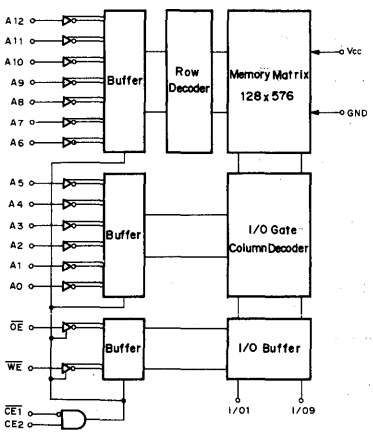
Structure

Silicon gate CMOS IC

Function

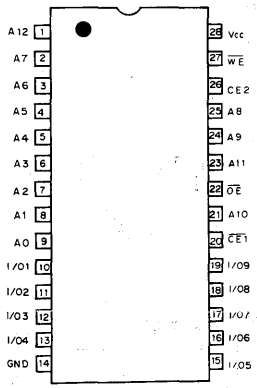
8192-word × 9-bit static RAM

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground

Absolute Maximum Ratings Ta = 25℃, GND = 0V

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5* to + 7.0	V
Input voltage	V_{IN}		− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK5971P/J	1.0	W
		CXK5971M	0.7	
Operating temperature	Topr		0 to + 70	℃
Storage temperature	Tstg		− 55 to + 150	℃
Soldering temperature • time	Tsolder		260 • 10	℃ • sec

***Note**) V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	V_{CC} Current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions Ta = 0 to + 70℃, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

***Note**) V_{IL} = − 3.0V Min. for pulse width less than 20ns.

3

Electrical Characteristics

DC and operating characteristics

V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70℃

Item	Symbol	Test condition	−25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geqq V_{CC} - 0.2V$ or CE2 ≦ 0.2V $V_{IN} \geqq V_{CC} - 0.2V$ or $V_{IN} \leqq 0.2V$	—	1	100	μA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{IN} = V_{IL} or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, Ta = 25℃

I/O capacitance

Ta = 25℃, f = 1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	10	pF

Note) This parameter is sampled and is not 100% tested.

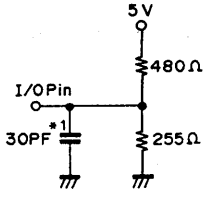
AC characteristics

- **AC test conditions**

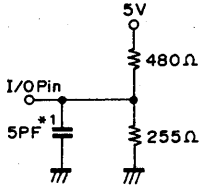
V_{CC} = 5V ± 10%, Ta = 0 to +70℃

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*²



* 1. including scope and jig capacitance
* 2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t_{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t_{OE}	—	15	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}* t_{LZ2}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}* t_{HZ2}*	0	15	0	15	0	20	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	13	0	13	0	15	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	20	—	20	—	20	ns

2) Write cycle

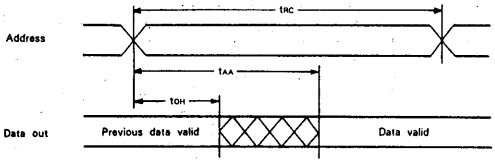
Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	13	0	13	0	15	ns

* Transition is measured ±500mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

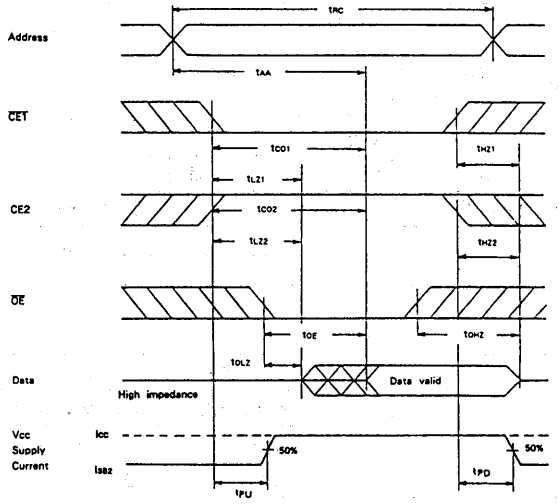
Timing Waveform

1) Read cycle

- Read cycle No. 1 : [$\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$]

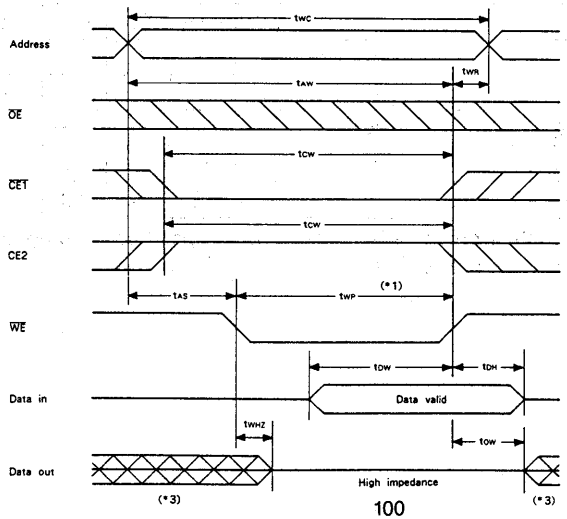


- Read cycle No. 2 : [$\overline{WE} = V_{IH}$]

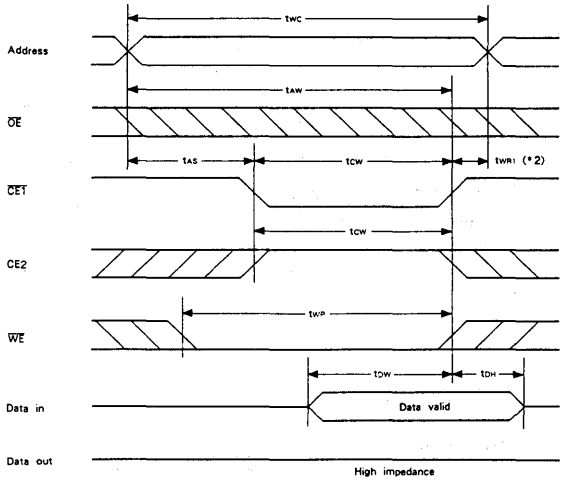


2) Write cycle

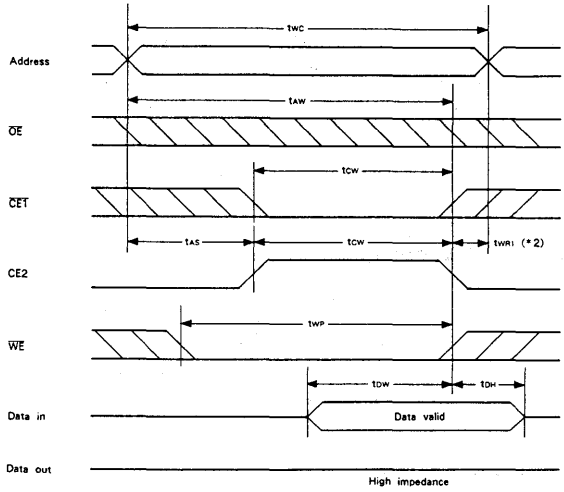
- Write cycle No. 1 : [$\overline{WE}$ control]



• Write cycle No. 2 : [$\overline{CE1}$ control]



• Write cycle No. 3 : [CE2 control]



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

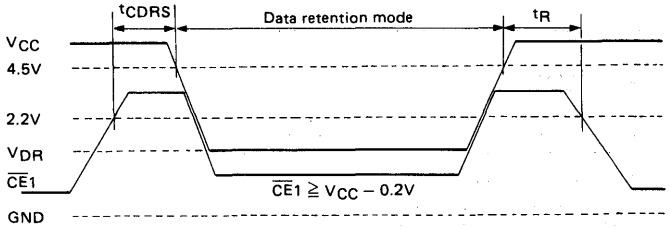
*3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

Data Retention Characteristics Ta = 0 to + 70°C

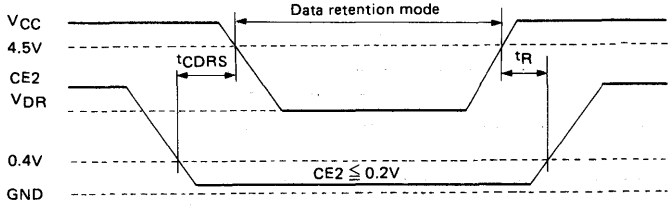
Item	Symbol	Test condition	−25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V *1	—	0.5	50	µA
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V *1	—	1.0	100	µA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

*1 $\overline{CE1} \geqq V_{CC} - 0.2V$ or $CE2 \leqq 0.2V$, $V_{IN} \geqq V_{CC} - 0.2V$ or $V_{IN} \leqq 0.2V$
*2 t_{RC} : Read cycle time

Data Retention Waveform (1) : [$\overline{CE1}$ control]

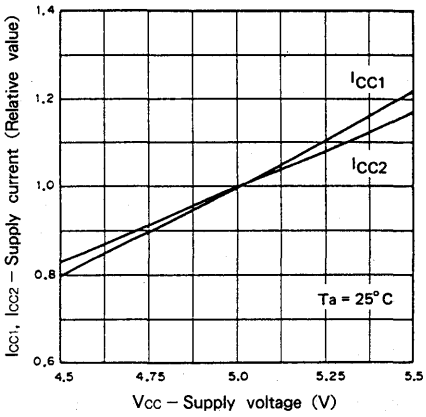


Data Retention Waveform (2) : [CE2 control]

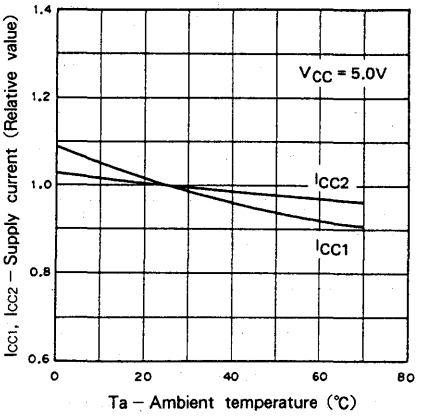


Example of Representative Characteristics

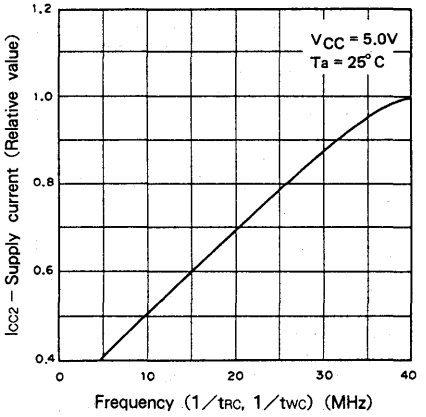
Supply current vs. Supply voltage



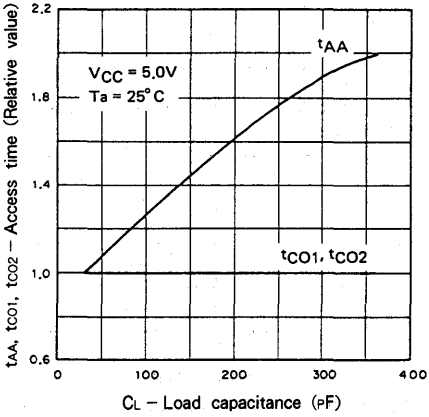
Supply current vs. Ambient temperature



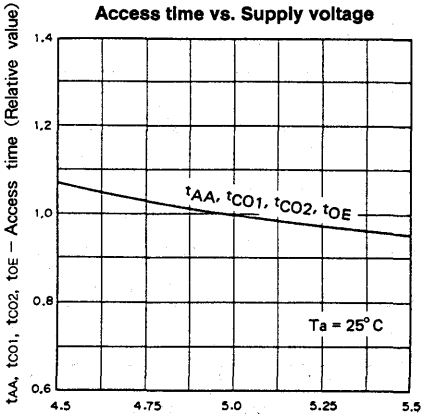
Supply current vs. Frequency



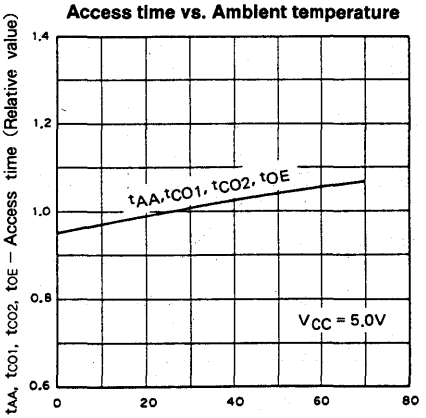
Access time vs. Load capacitance



Access time vs. Supply voltage

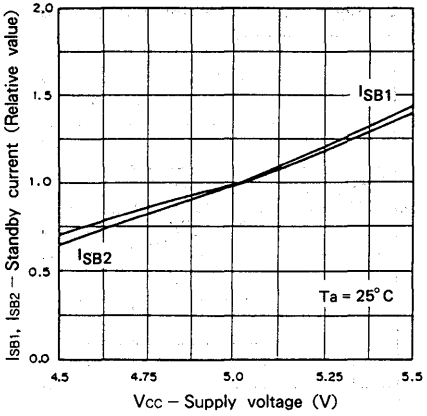


Access time vs. Ambient temperature

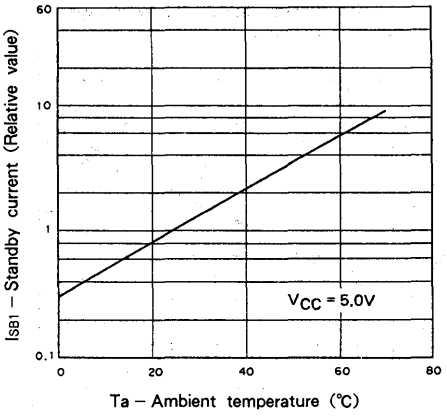


3

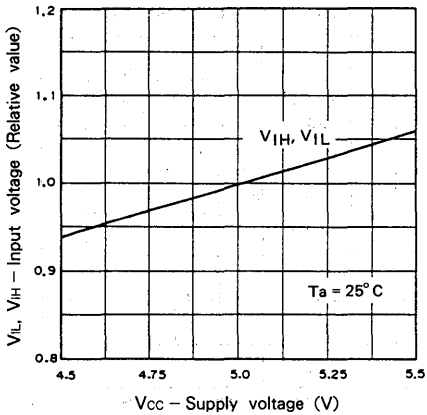
Standby current vs. Supply voltage



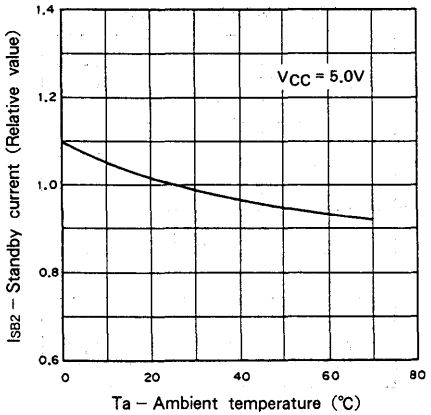
Standby current vs. Ambient temperature



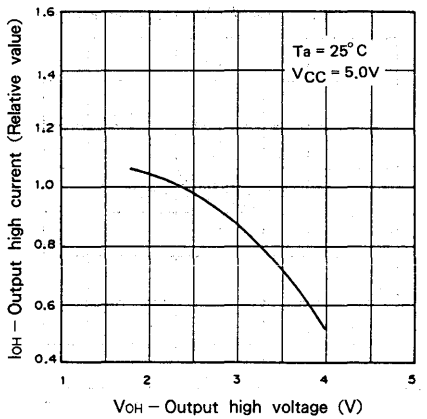
Input voltage level vs. Supply voltage



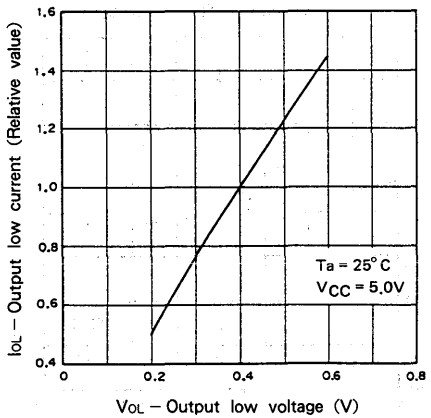
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

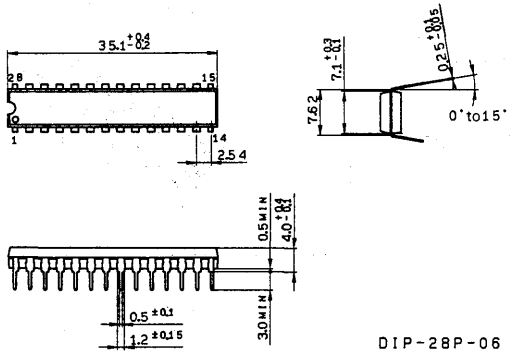


Output low current vs. Output low voltage



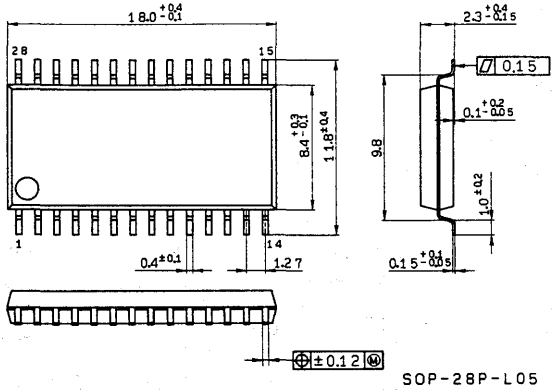
Package Outline Unit : mm

CXK5971P 28 pin DIP (Plastic) 300mil 2.0g



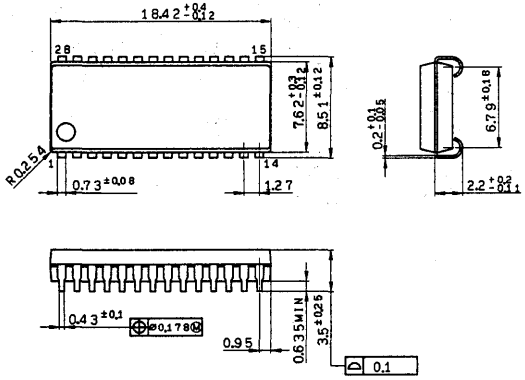
DIP-28P-06

CXK5971M 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5971J 28 pin SOJ (Plastic) 300mil 0.8g



SOJ-28P-01

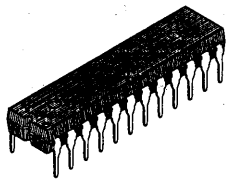
3

262,144-word × 1 bit High Speed CMOS Static RAM

Description

CXK51256P is 262,144-word × 1 bit high speed CMOS static RAM organized as 262,144-word by 1 bit and operates from a single 5V supply.
This device is suitable for use in high speed and low power applications.

24 pin DIP (Plastic)



Features

- Fast access time (Access time)
  CXK51256P-35 35ns (Max.)
  CXK51256P-45 45ns (Max.)
  CXK51256P-55 55ns (Max.)
- Low power consumption (operation) : 100mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Separate data input and output.
- Three-state output.
- Directly TTL compatible : All input and output.
- High density : 300mil 24 pin plastic package

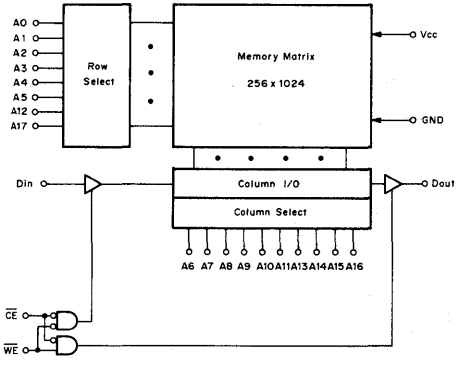
Function

262,144-word × 1 bit static RAM

Structure

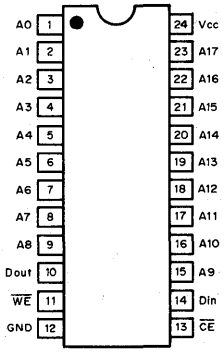
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
Din	Data input
Dout	Data output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V Power supply
GND	Ground

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} +0.5	V
Voltage applied to output	V_{OUT}	−0.5* to V_{CC} +0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature	Tsolder	260 • 10	℃ • sec

***Note**) V_{CC}, V_{IN}, V_{OUT} min = −3.5V for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	Data out	V_{CC} Current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	I_{CC1}, I_{CC2}
L	L	Write	High Z	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions Ta = 0 to +70℃, GND = 0V

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*2	—	0.8	V

Note) *1. V_{CC} = 5V, Ta = 25℃
*2. V_{IL} min = −3.0V for pulse width less than 20ns.

3

Electrical Characteristics

DC and operating characteristics

Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70℃

Item	Symbol	Test condition	−35/45/55			Unit
			Min.	Typ.	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC} V_{CC} = 5.5V	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} V_{OUT} = GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, V_{IN} = V_{IH}/V_{IL}	—	20	45	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100% I_{OUT} = 0mA	—	55	85	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V, V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	—	2	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

I/O capacitance

Ta = 25℃, f = 1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

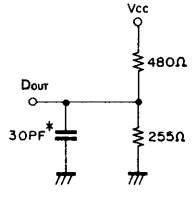
AC characteristics

• AC test conditions

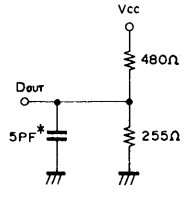
Vcc = 5V ± 10%, Ta = 0 to +70℃

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	t_R = 5ns
Input fall time	t_F = 5ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)**



* Including scope and jig

** For t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

Read cycle

Item	Symbol	−35		−45		−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	—	45	—	55	—	ns
Address access time	t_{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	35	—	45	—	55	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	20	0	20	0	25	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	30	—	30	—	30	ns

* **Note**) Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

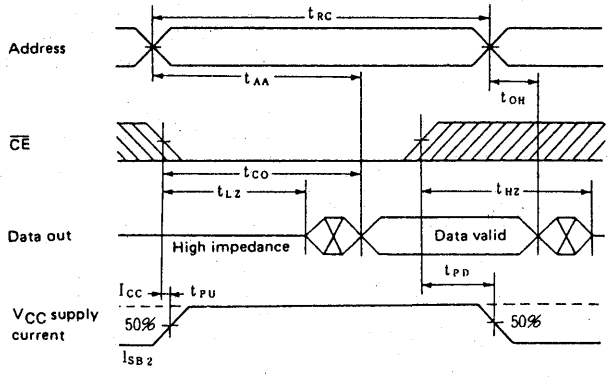
Write cycle

Item	Symbol	−35		−45		−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t_{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t_{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t_{DW}	20	—	25	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	25	—	25	—	35	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	20	0	20	0	25	ns

* **Note**) Transition is measured ±200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

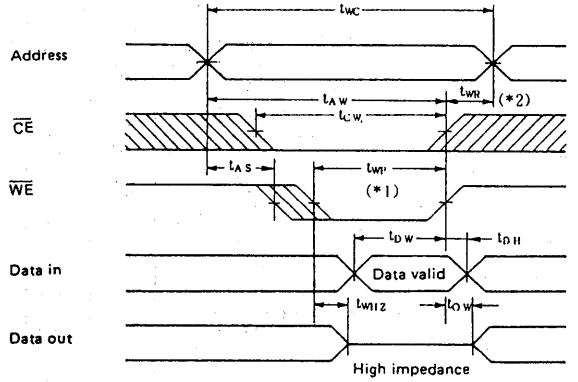
Timing Waveform

1) Read cycle [$\overline{WE}$ = V_{IH}]

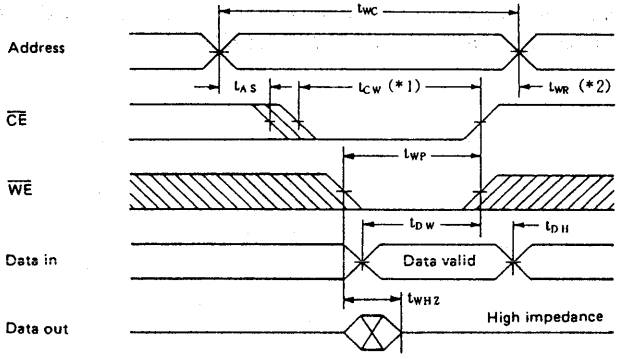


2) Write cycle

- Write cycle 1 : $\overline{WE}$ control



- Write cycle 2 : $\overline{CE}$ control

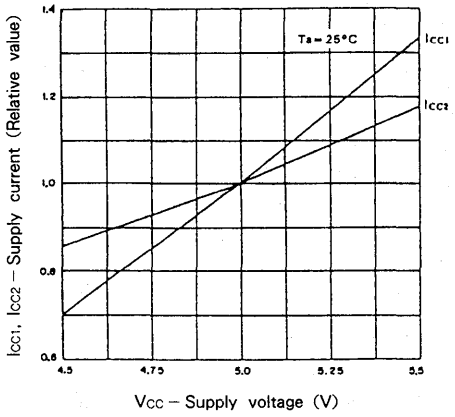


***Note)**

1. A write occures during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

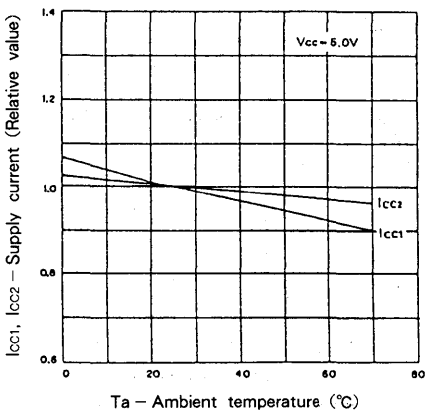
Example of Representative Characteristics

Supply current vs. Supply voltage



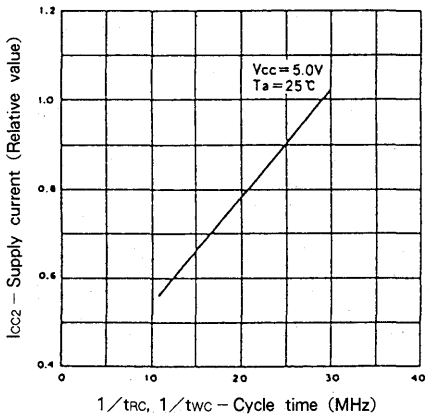
VCC – Supply voltage (V)

Supply current vs. Ambient temperature



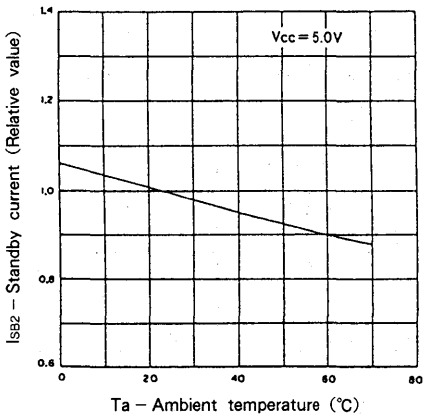
Ta – Ambient temperature (°C)

Supply current vs. Cycle time



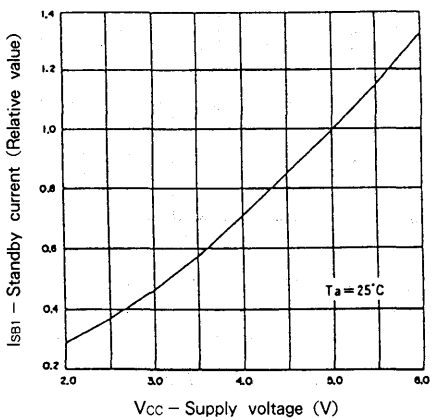
1/tRC, 1/tWC – Cycle time (MHz)

Standby current vs. Ambient temperature



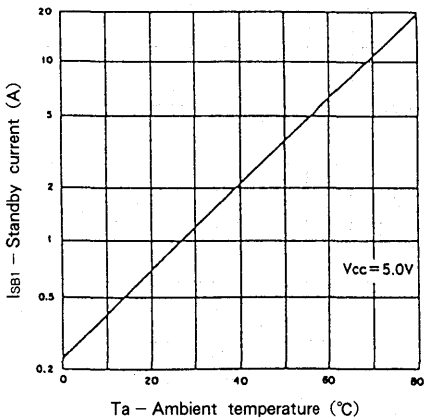
Ta – Ambient temperature (°C)

Standby current vs. Supply voltage



VCC – Supply voltage (V)

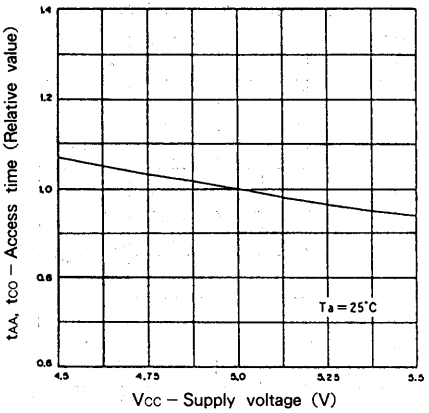
Standby current vs. Ambient temperature



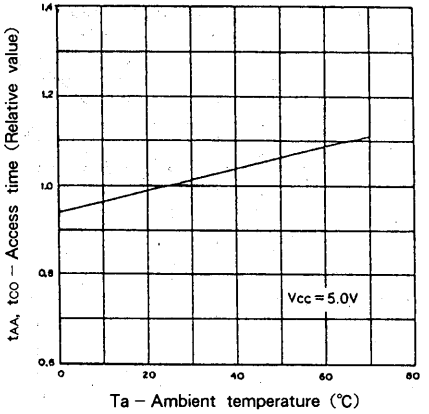
Ta – Ambient temperature (°C)

3

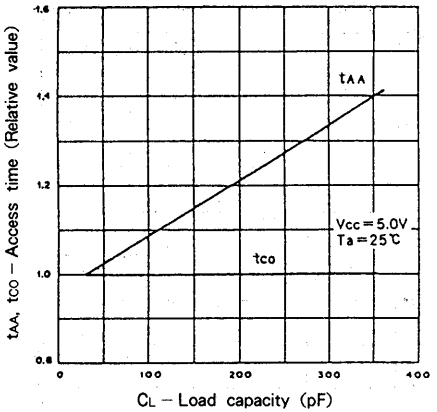
Access time vs. Supply voltage



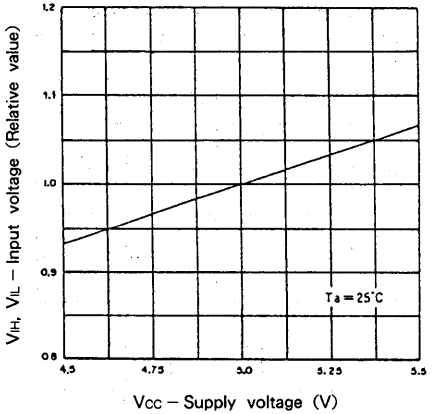
Access time vs. Ambient temperature



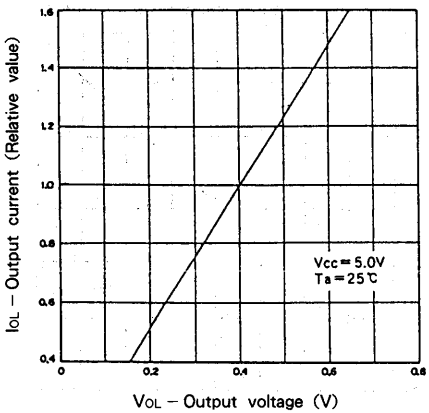
Access time vs. Load capacity



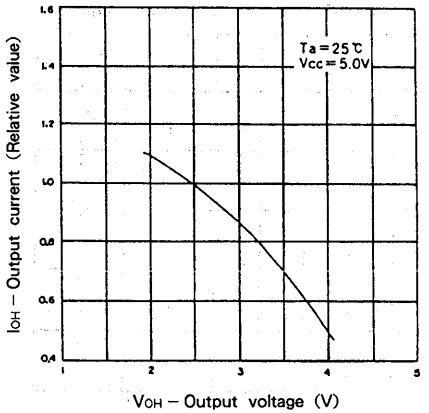
Input voltage vs. Supply voltage



Output current vs. Output voltage

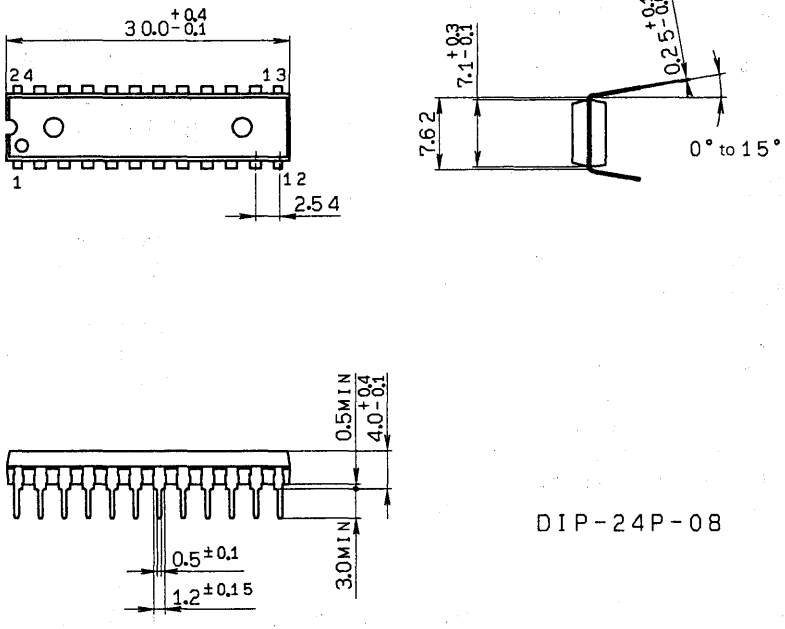


Output current vs. Output voltage



Package Outline Unit : mm

24 pin DIP (Plastic) 300mil 1.5g



DIP-24P-08

3

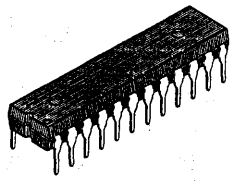
65,536-word × 4-bit High Speed CMOS Static RAM

Description

CXK54256P is a 262,144 bits high speed CMOS static RAM organized as 65,536 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

24 pin DIP (Plastic)



Features

- Fast access time (Access time)
  CXK54256P-35 35ns (Max.)
  CXK54256P-45 45ns (Max.)
  CXK54256P-55 55ns (Max.)
- Low power consumption (operation) :100mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300 mil 24 pin plastic package

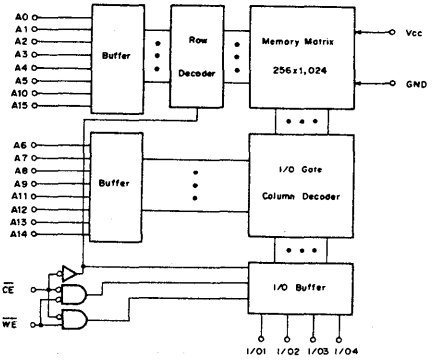
Structure

Silicon gate CMOS IC

Function

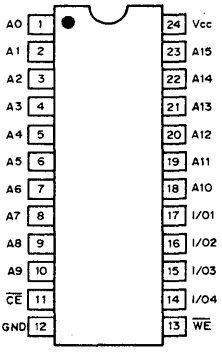
65,536-word × 4-bit static RAM

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O4	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+ 5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature • time	Tsolder	260 • 10	℃ • sec

***Note**) V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} Current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	I_{CC1}, I_{CC2}
L	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

***Note**) V_{IL} = − 3.0V Min. for pulse width less than 20ns.

3

Electrical Characteristics

• DC and operating characteristics (V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test condition	−35/45/55			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN} = GND to V_{CC} V_{CC} = 5.5V	−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA V_{IN} = V_{IH}/V_{IL}	—	20	45	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100% I_{OUT} = 0mA	—	55	85	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V, V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	—	2	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	15	30	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

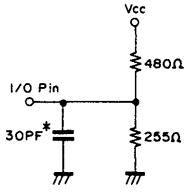
AC characteristics

• AC test conditions

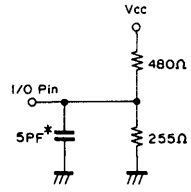
(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

● **Read cycle**

Item	Symbol	−35		−45		−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	—	45	—	55	—	ns
Address access time	t_{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	35	—	45	—	55	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	15	0	15	0	20	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	30	—	30	—	30	ns

***Note**) Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

● **Write cycle**

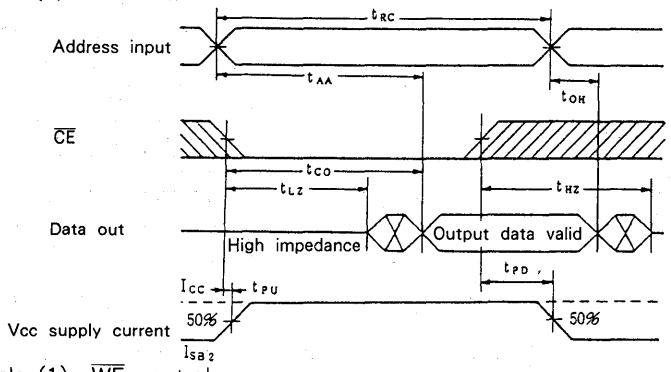
Item	Symbol	−35		−45		−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t_{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t_{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t_{DW}	15	—	20	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	30	—	35	—	45	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	15	0	15	0	20	ns

***Note**) Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

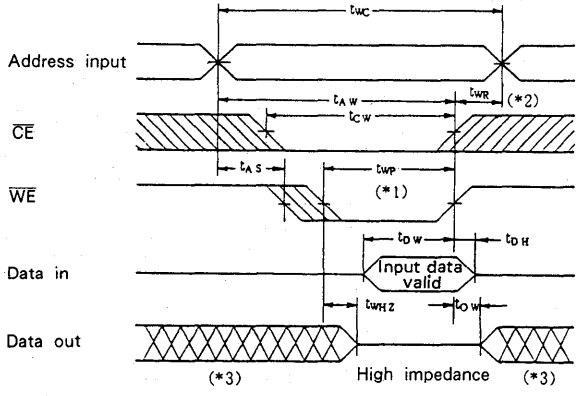
3

Timing Waveform

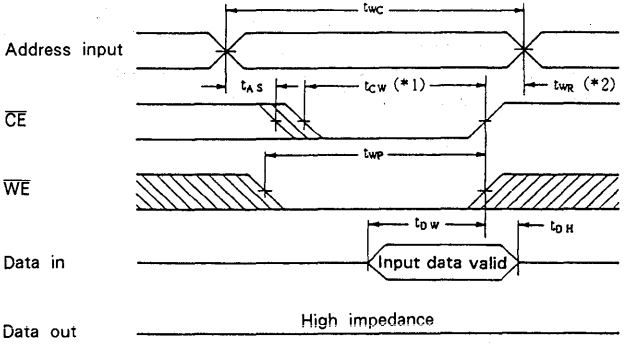
• Read cycle (1) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control

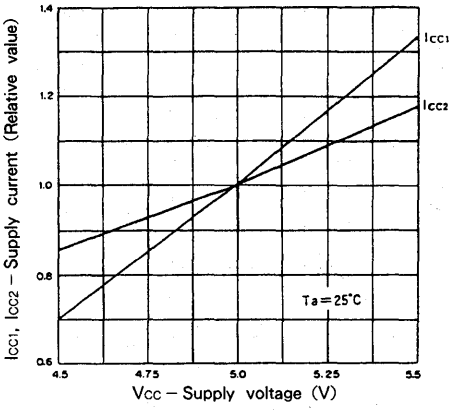


*** Note)**

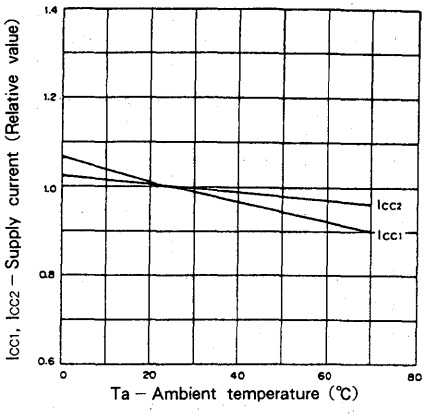
1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

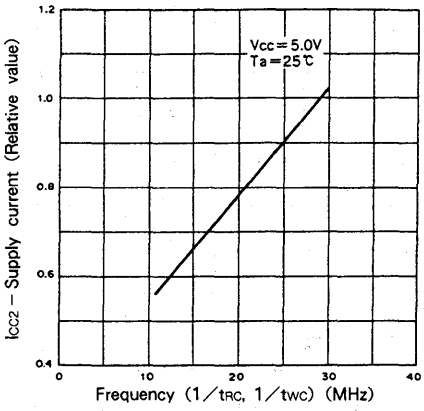
Supply current vs. Supply voltage



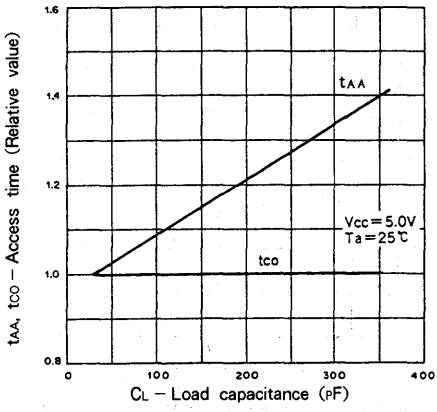
Supply current vs. Ambient temperature



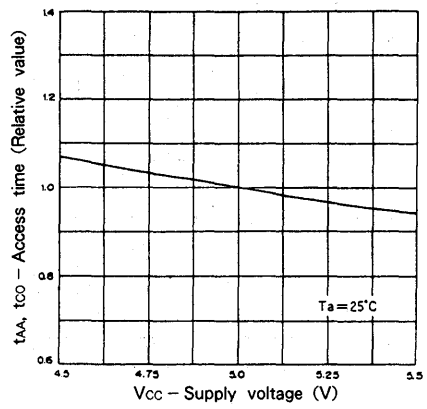
Supply current vs. Frequency



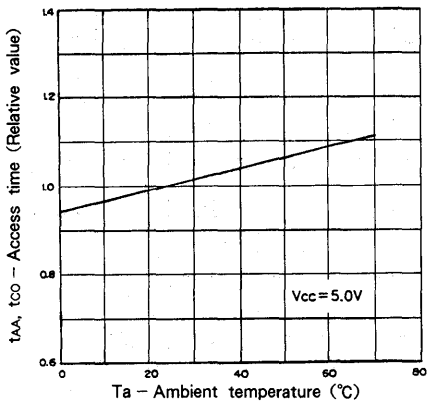
Access time vs. Load capacitance



Access time vs. Supply voltage



Access time vs. Ambient temperature



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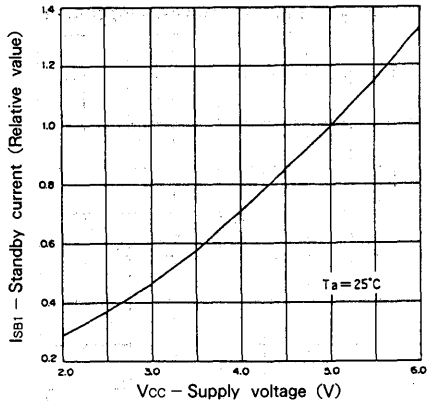
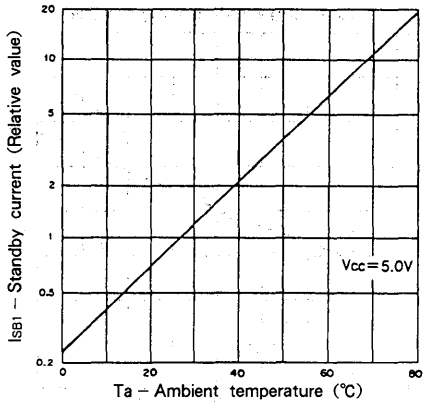
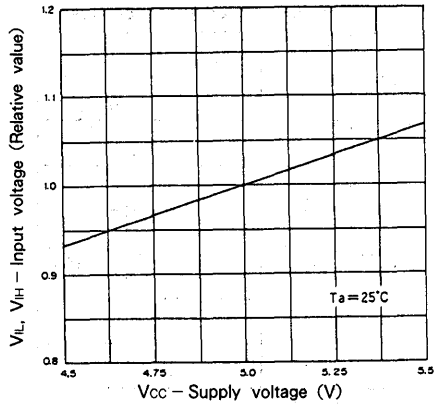
Standby current vs. Supply voltage



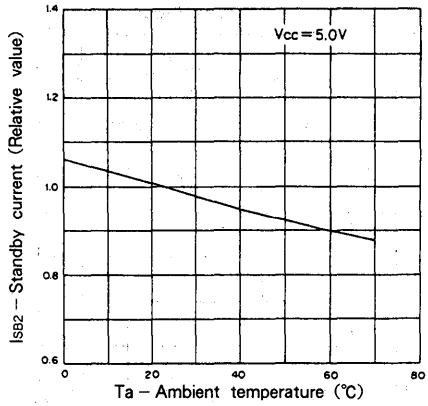
Standby current vs. Ambient temperature



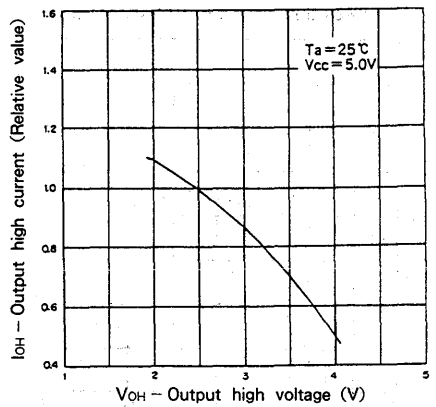
Input voltage level vs. Supply voltage



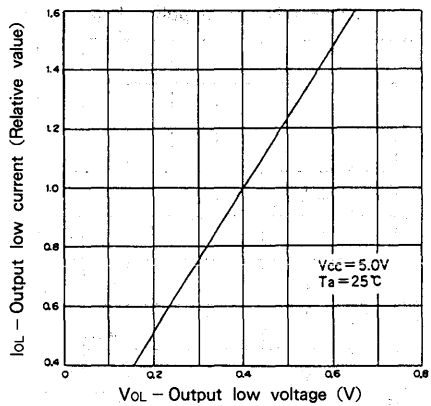
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

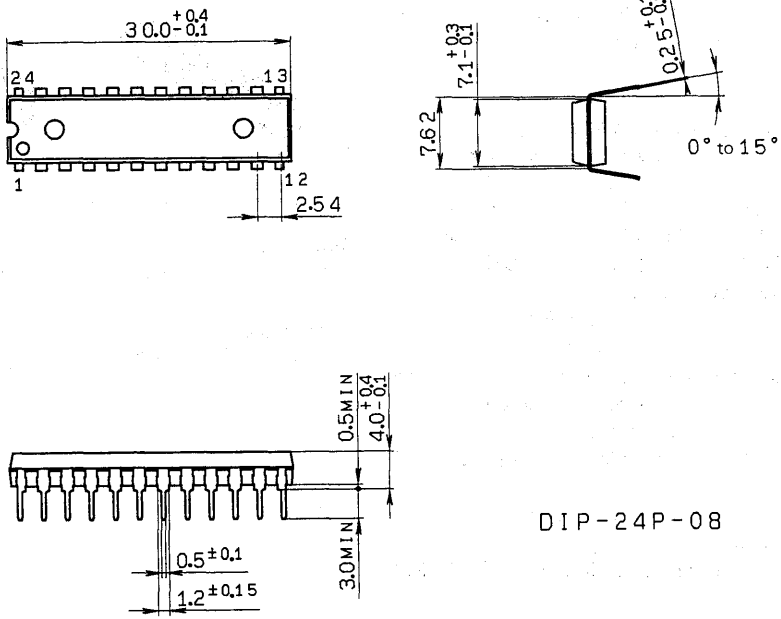


Output low current vs. Output low voltage



Package Outline Unit : mm

CXK54256P 24 pin DIP (Plastic) 300mil 1.5g



DIP-24P-08

3

SONY CXK58258AP/AJ -15/20/25

32,768-word × 8-bit High Speed CMOS Static RAM

Description

The CXK58258AP/AJ is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 15/20/25ns access time from 5V single power supply.

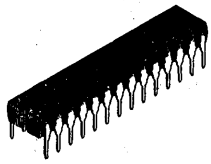
Features

- High speed, low power consumption :

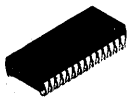
	Access time (Max.)	Power consumption (Typ., Cycle = Min.)
CXK58258AP/AJ-15	15ns	500mW
CXK58258AP/AJ-20	20ns	425mW
CXK58258AP/AJ-25	25ns	375mW

- Single +5V power supply :
  −15 5V ± 5%
  −20/25 5V ± 10%
- Fully static memory···No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output : three state output
- Available in 28 pin 300mil DIP, 300mil SOJ package.

CXK58258AP
28 pin DIP (Plastic)



CXK58258AJ
28 pin SOJ (Plastic)



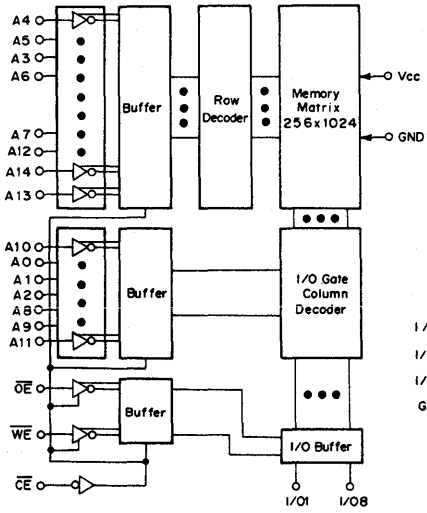
Function

32,768-word × 8-bit static RAM

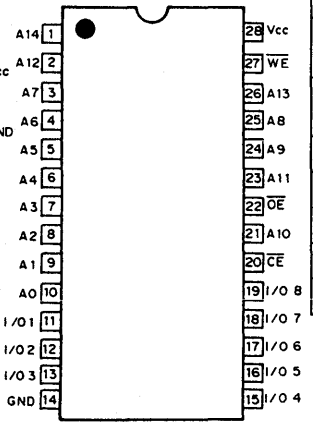
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ = −3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	−15	V_{CC}	4.75	5.0	5.25	V
	−20/25		4.5	5.0	5.5	
Input high voltage		V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage		V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 20ns.

3

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%*, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.**	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to Vcc, $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	—	—	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}	−15	—	100	130	mA
			−20	—	85	120	
			−25	—	75	120	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V		—	—	1	mA
	I_{SB2}	Cycle = Min, Duty = 100%, $\overline{CE}$ = V_{IH}, V_{IN} = V_{IL} or V_{IH}		—	15	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

* Vcc = 5V ± 5% for CXK58258AP/AJ-15

** Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

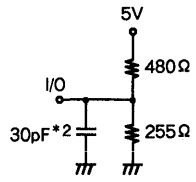
AC characteristics

• AC test conditions

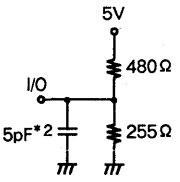
(Vcc = 5V ± 10%*1, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*3



*1 Vcc = 5V ± 5% for CXK58258AP/AJ-15

*2 including scope and jig capacitance

*3 for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	−15		−20		−25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	15	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	20	—	25	ns
Chip enable access time	t_{CO}	—	15	—	20	—	25	ns
Output enable to output valid	t_{OE}	—	8	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	—	8	—	9	—	10	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	7	—	8	—	9	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	15	—	20	—	25	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

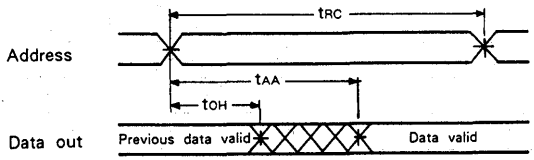
• **Write cycle**

Item	Symbol	−15		−20		−25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	15	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	10	—	13	—	15	—	ns
Chip enable to end of write	t_{CW}	11	—	14	—	16	—	ns
Data to write time overlap	t_{DW}	8	—	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	13	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	3	—	3	—	3	—	ns
Write to output in high Z	t_{WHZ}*	—	8	—	9	—	10	ns

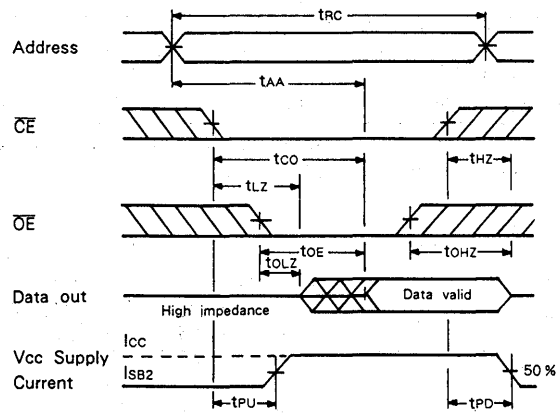
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

Timing Waveform

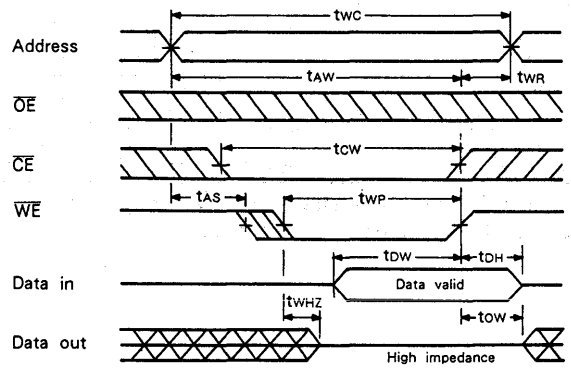
• Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



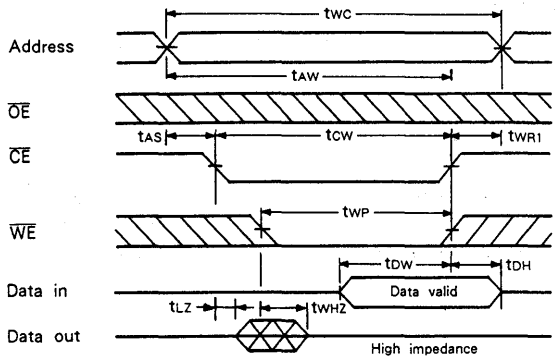
• Read cycle (2) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



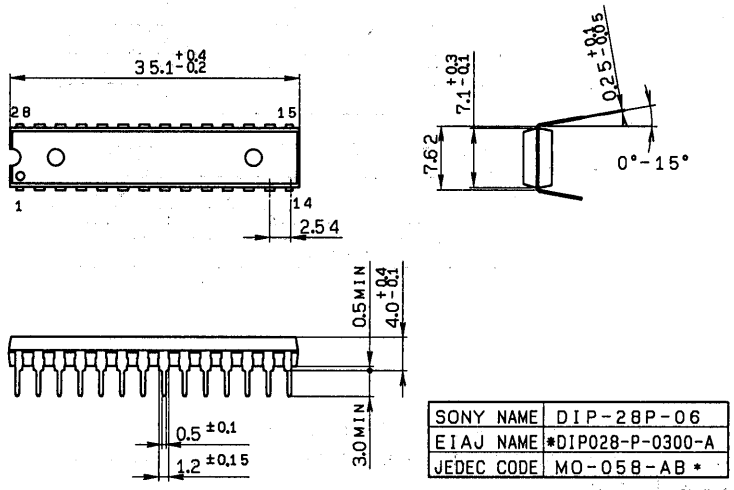
Note)

1. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

CXK58258AP

28pin DIP (Plastic) 300mil 2.0g

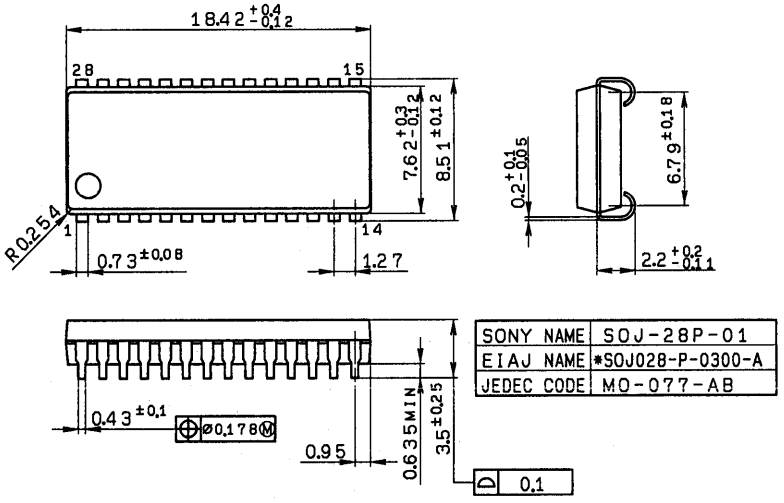


SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB *

* (Similar)

CXK58258AJ

28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB

SONY CXK58258BP/BJ/BM -20L/25L/35L -20LL/25LL/35LL

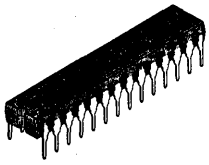
32,768-word × 8-bit High Speed CMOS Static RAM

Description

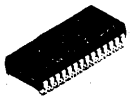
The CXK58258BP/BJ is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 20/25/35ns access time from 5V single power supply.

This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

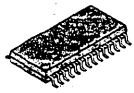
CXK58258BP
28 pin DIP (Plastic)



CXK58258BJ
28 pin SOJ (Plastic)



CXK58258BM
28 pin SOP (Plastic)



Features

- Fast access time

	(Access time)
CXK58258BP/BJ-20L, 20LL	20ns (Max.)
CXK58258BP/BJ-25L, 25LL	25ns (Max.)
CXK58258BP/BJ-35L, 35LL	35ns (Max.)

- Low power operation

	Standby (Max.)	Operation (Typ., Min. Cycle)
CXK58258BP/BJ-20LL	5 µW	425mW
CXK58258BP/BJ-25LL	5 µW	375mW
CXK58258BP/BJ-35LL	5 µW	325mW
CXK58258BP/BJ-20L	10 µW	425mW
CXK58258BP/BJ-25L	10 µW	375mW
CXK58258BP/BJ-35L	10 µW	325mW

- Single +5V power supply : 5V ± 10%
- Fully static memory···No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output : three state output
- Available in 28 pin 300mil DIP, 300mil SOJ package.

Function

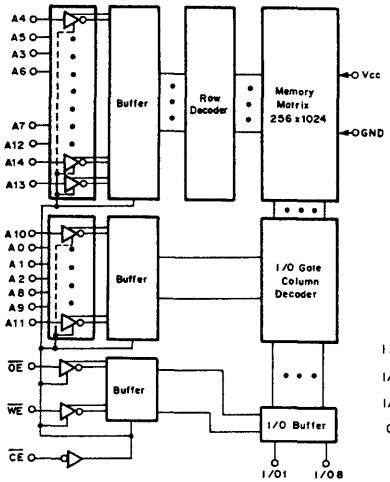
32,768-word × 8-bit static RAM

Structure

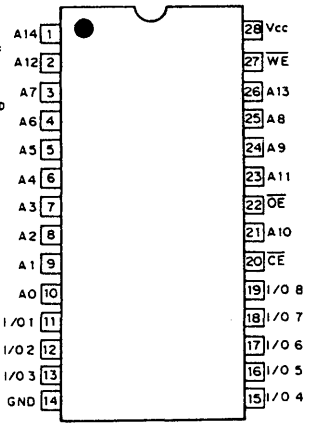
Silicon gate CMOS IC

3

Block Diagram



Pin Configuration (Top view)



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Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature • time	Tsolder	260 • 10	℃ • sec

* V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to Vcc, $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}		−1	—	1	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	—	—	—	—	—	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}	-20L/20LL	—	85	120	—	85	120	mA
			-25L/25LL	—	75	120	—	75	120	
			-35L/35LL	—	65	100	—	65	100	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V		—	0.002	0.1	—	0.001	0.05	mA
	I_{SB2}	Cycle = Min, Duty = 100%, $\overline{CE}$ = V_{IH}		—	1.5	5	—	1.5	5	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

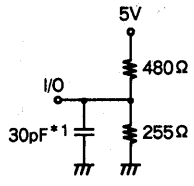
AC characteristics

• AC test conditions

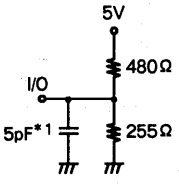
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance
*2 for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	20	—	25	—	35	—	ns
Address access time	t_{AA}	—	20	—	25	—	35	ns
Chip enable access time	t_{CO}	—	20	—	25	—	35	ns
Output enable to output valid	t_{OE}	—	10	—	12	—	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	—	9	—	10	—	15	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	8	—	9	—	12	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	—	35	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

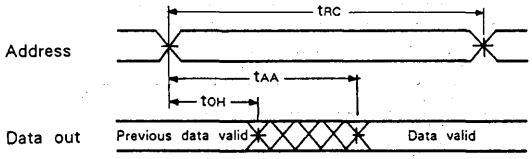
• Write cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	20	—	25	—	35	—	ns
Address valid to end of write	t_{AW}	13	—	15	—	20	—	ns
Chip enable to end of write	t_{CW}	14	—	16	—	20	—	ns
Data to write time overlap	t_{DW}	10	—	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	13	—	15	—	20	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	3	—	3	—	3	—	ns
Write to output in high Z	t_{WHZ}*	—	9	—	10	—	12	ns

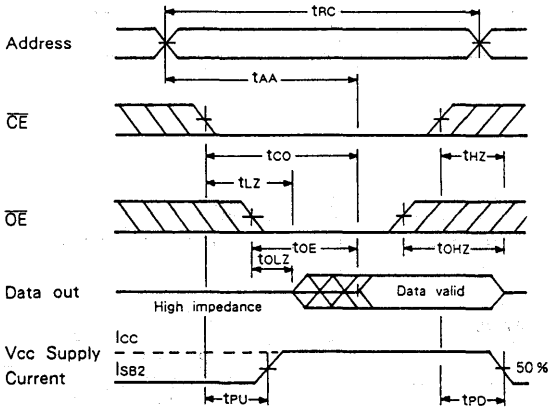
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

Timing Waveform

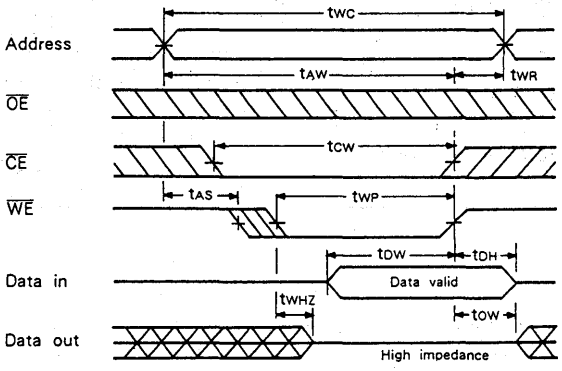
• Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



• Read cycle (2) : $\overline{WE} = V_{IH}$

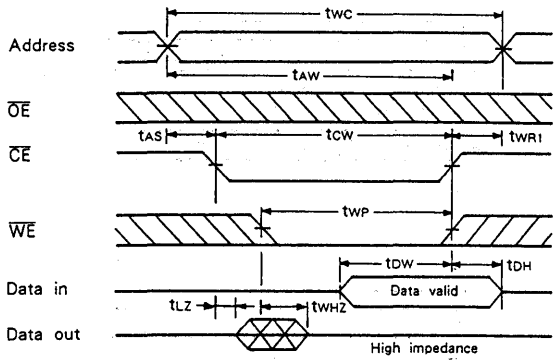


• Write cycle (1) : $\overline{WE}$ control



3

• Write cycle (2) : $\overline{CE}$ control



Note)

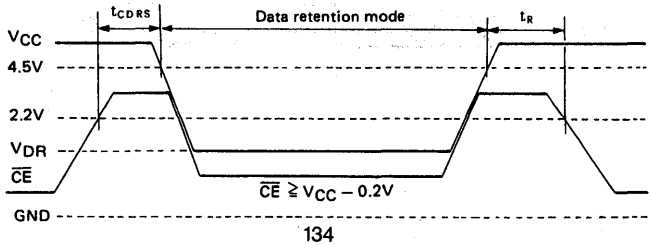
1. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta = 0 to +70°C)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geqq 2.8V$	Ta = 0 to 70°C	—	—	50	—	—	10	µA
			Ta = 0 to 40°C	—	—	10	—	—	4	
			25°C	—	1	3	—	0.5	1	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geqq V_{CC} - 0.2V$		—	0.002	0.1	—	0.001	0.05	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

* t_{RC} : Read cycle time

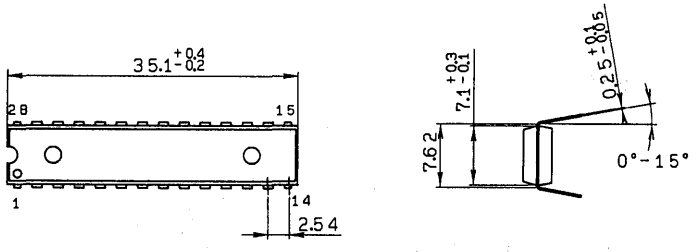
Data retention time



Package Outline Unit : mm

CXK58258BP

28pin DIP (Plastic) 300mil 2.0g

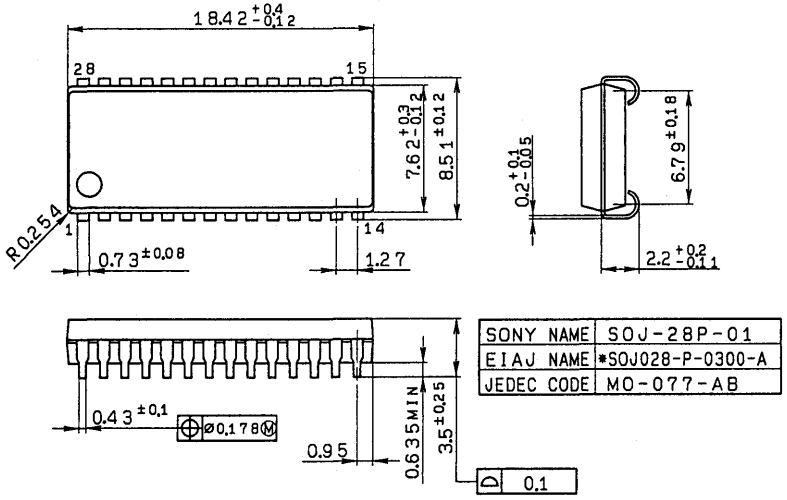


SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB *

* (Similar)

CXK58258BJ

28pin SOJ (Plastic) 300mil 0.8g



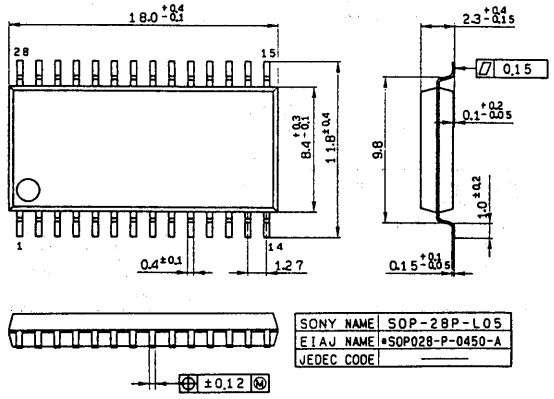
SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB

3

Package Outline Unit : mm

CXK58258BM

28pin SOP (Plastic) 450mil 0.7g



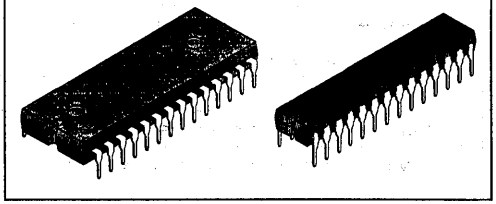
32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58258P/SP are 262,144 bits high speed CMOS static RAMs suitable for use in high speed and low power applications. Organized as 32,768 words by 8-bit, it operates from a single 5V supply.

CXK58258P
28 pin DIP (Plastic)

CXK58258SP
28 pin DIP (Plastic)



Features

- Fast access time : (Access time)
  CXK58258P/SP-35 35ns (Max.)
  CXK58258P/SP-45 45ns (Max.)
  CXK58258P/SP-55 55ns (Max.)
- Low power operation : (Standby) (Operation)
  CXK58258P/SP-35, 45, 55
  50μW (Typ.) 250mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 28 pin 600mil DIP and 300mil DIP.

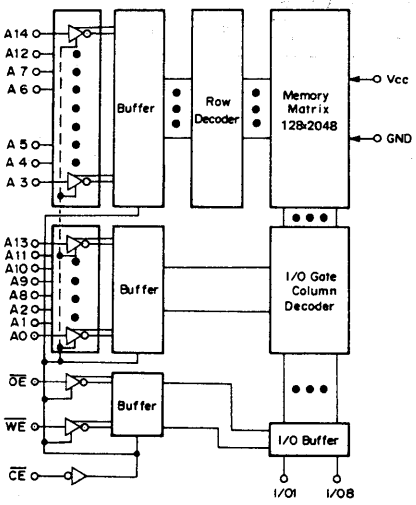
Function

32,768-word × 8-bit static RAM

Structure

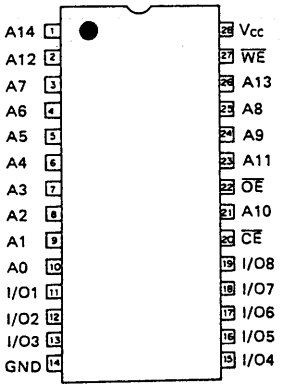
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground

3

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature • time	Tsolder	260 • 10	℃ • sec

* V_{CC}, V_{IN}, $V_{I/O}$ = −3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test condition	−35/45/55			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	V_{IN} = GND to V_{CC}	−2	—	2	μA
Output leak current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}	−2	—	2	μA
Operating supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	—	50	80	mA
Average operating current	I_{CC2}	Min. cycle Duty = 100%, I_{OUT} = 0mA	—	90	140	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V	—	0.01	2	mA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	—	10	
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	5	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

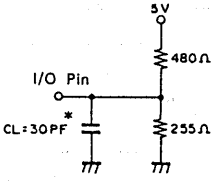
AC characteristics

• AC test conditions

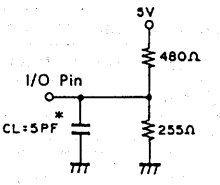
(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig capacitance

** for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

● **Read cycle**

Item	Symbol	−35		−45		−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	—	45	—	55	—	ns
Address access time	t_{AA}	—	35	—	45	—	55	ns
Chip enable access time	t_{CO}	—	35	—	45	—	55	ns
Output enable to output valid	t_{OE}	—	20	—	25	—	30	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	—	15	—	20	—	25	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	15	—	20	—	25	ns
Power up time	t_{PU}	0	—	0	—	0	—	ns
Power down time	t_{PD}	—	35	—	45	—	55	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

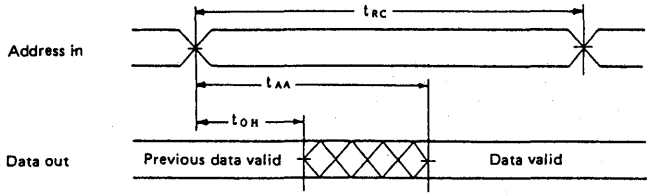
● **Write cycle**

Item	Symbol	−35		−45		−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t_{AW}	30	—	40	—	45	—	ns
Chip enable to end of write	t_{CW}	35	—	40	—	45	—	ns
Data to write time overlap	t_{DW}	18	—	20	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	30	—	35	—	35	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	—	12	—	15	—	15	ns

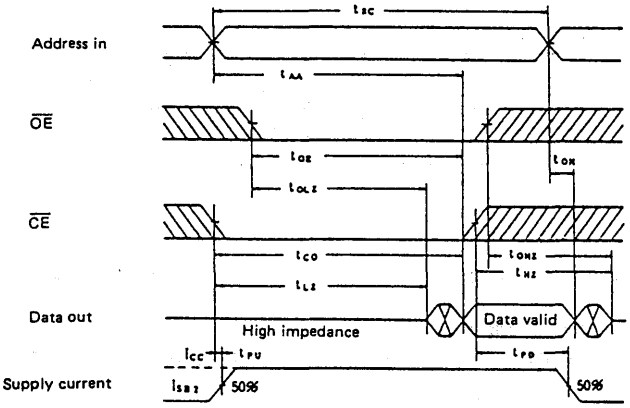
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

Timing Waveform

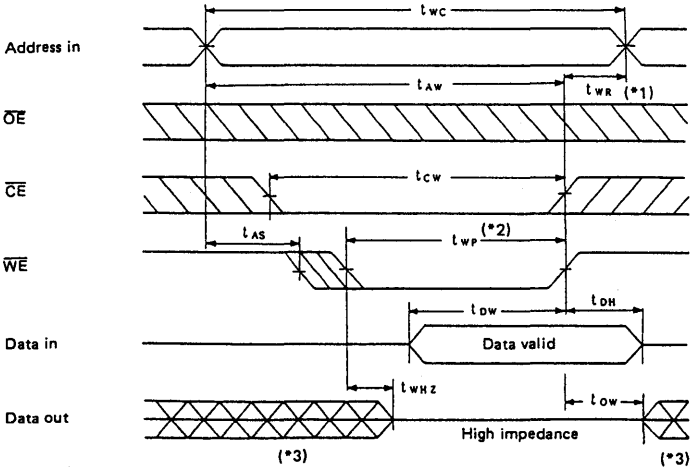
• Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



• Read cycle (2) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



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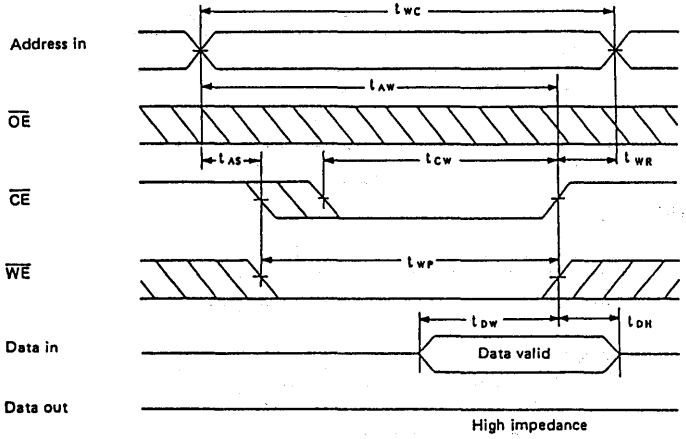
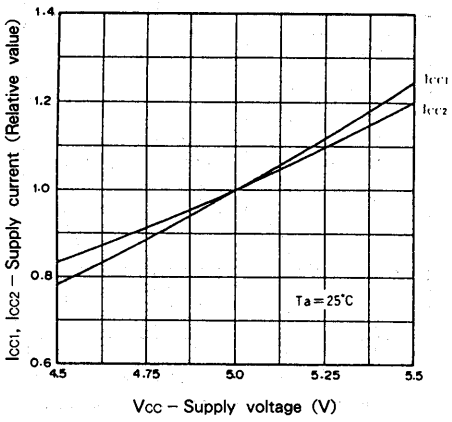
• Write cycle (2) : $\overline{CE}$ control



* 1. t_{WR} is measured from the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.
* 2. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
* 3. While I/O pins are in the output state, do not apply data input signals of opposite phase to the output.

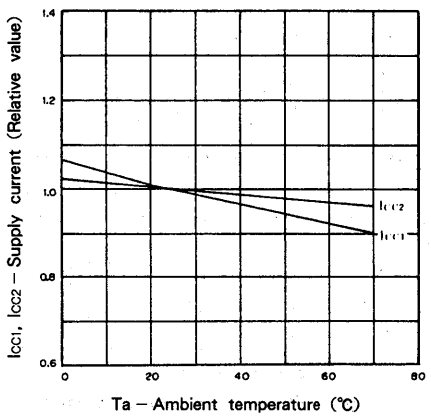
Example of Representative Characteristics

Supply current vs. Supply voltage



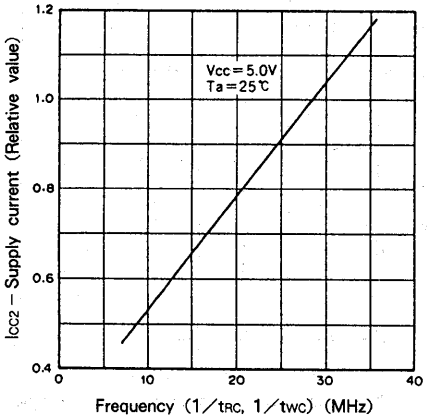
VCC – Supply voltage (V)

Supply current vs. Ambient temperature



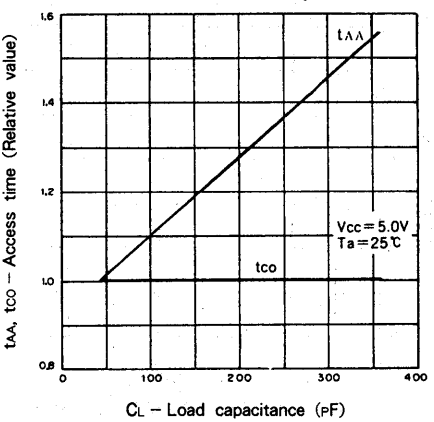
Ta – Ambient temperature (°C)

Supply current vs. Frequency



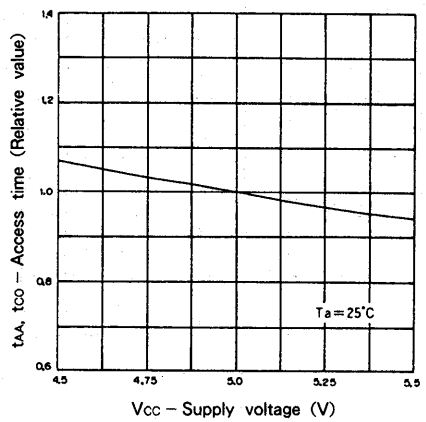
Frequency (1/tRC, 1/tWC) (MHz)

Access time vs. Load capacitance



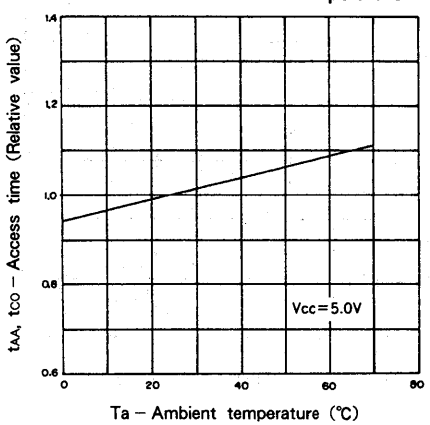
CL – Load capacitance (pF)

Access time vs. Supply voltage



VCC – Supply voltage (V)

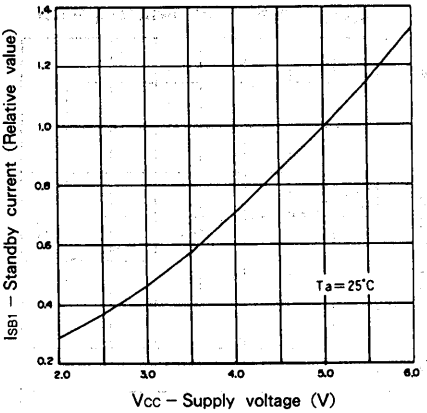
Access time vs. Ambient temperature



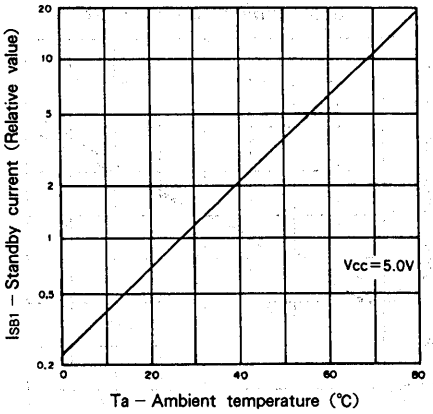
Ta – Ambient temperature (°C)

3

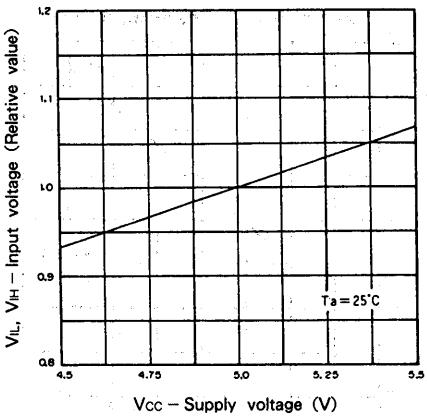
Standby current vs. Supply voltage



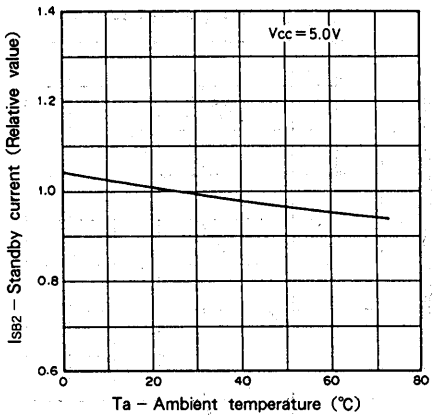
Standby current vs. Ambient temperature



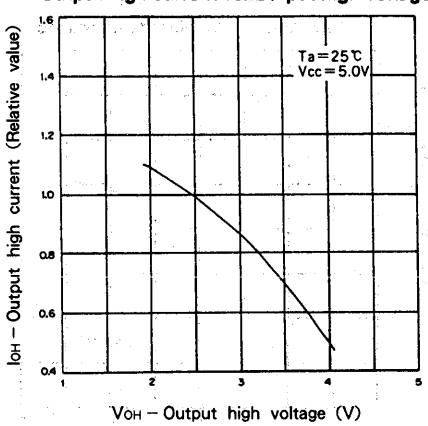
Input voltage level vs. Supply voltage



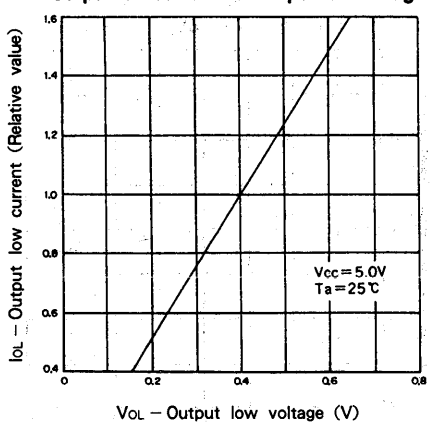
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

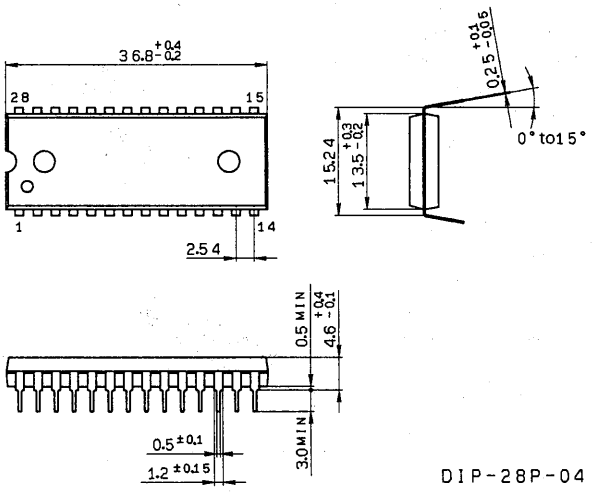


Output low current vs. Output low voltage



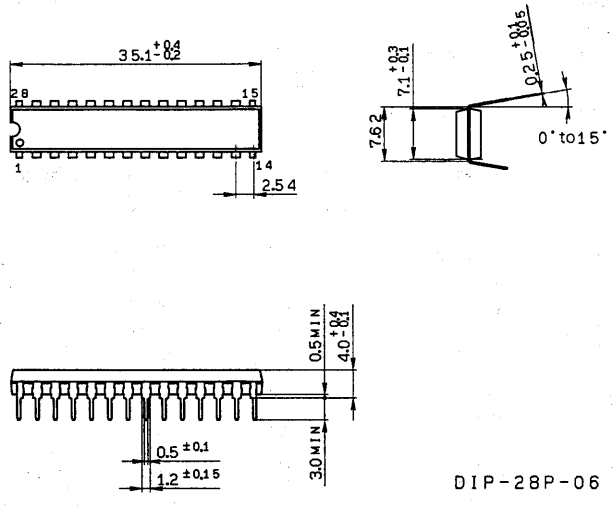
Package Outline Unit : mm

CXK58258P 28 pin DIP (Plastic) 600mil 4.2g



DIP-28P-04

CXK58258SP 28 pin DIP (Plastic) 300mil 2.0g



DIP-28P-06

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SONY CXK58257AP/ASP/AM -70L/85L/10L/12L -70LL/85LL/10LL/12LL

32768-word × 8-bit High Speed CMOS Static RAM

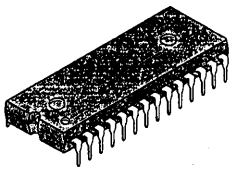
Description

CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

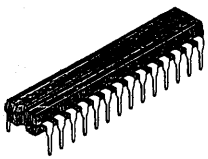
Features

- Fast access time : (Access time)
  CXK58257AP/ASP/AM-70L, 70LL 70ns(Max.)
  CXK58257AP/ASP/AM-85L, 85LL 85ns(Max.)
  CXK58257AP/ASP/AM-10L, 10LL 100ns(Max.)
  CXK58257AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
  CXK58257AP/ASP/AM-70LL, 85LL, 10LL, 12LL ;
  Standby : 1 µW (Typ.)
  Operation : 15mW (Typ.)
  CXK58257AP/ASP/AM-70L, 85L, 10L, 12L ;
  Standby : 2.5 µW (Typ.)
  Operation : 15mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory···No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs

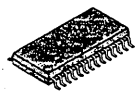
CXK58257AP
28 pin DIP (Plastic)



CXK58257ASP
28 pin DIP (Plastic)



CXK58257AM
28 pin SOP (Plastic)



- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

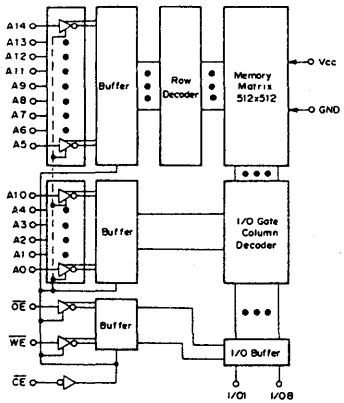
Function

32768-word × 8-bit static RAM

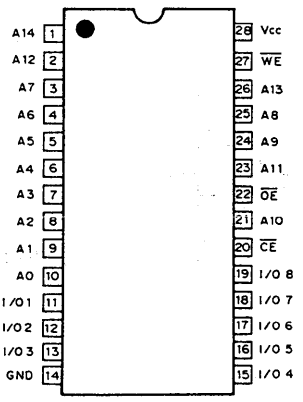
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK58257AP/ASP	1.0	W
		CXK58257AM	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260 • 10	°C • sec

* V_{IN}, $V_{I/O}$ = −3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Not selected	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 50ns.

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Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		−0.5	—	0.5	−0.5	—	0.5	μA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}		−0.5	—	0.5	−0.5	—	0.5	μA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE}$ ≦ 0.2V V_{IN} ≦ 0.2V or ≧ V_{CC} − 0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$ = V_{IH}		—	0.4	2	—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

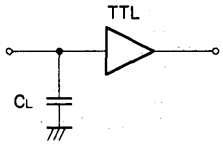
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL



* C_L includes scope and jig capacitances.

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• Read cycle

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t_{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t_{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

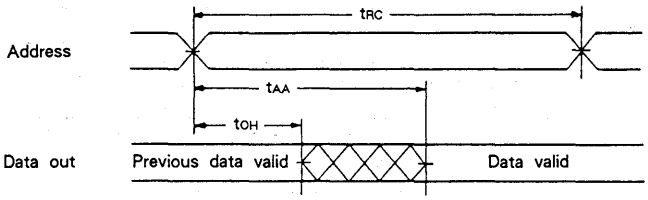
• Write cycle

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	0	25	ns

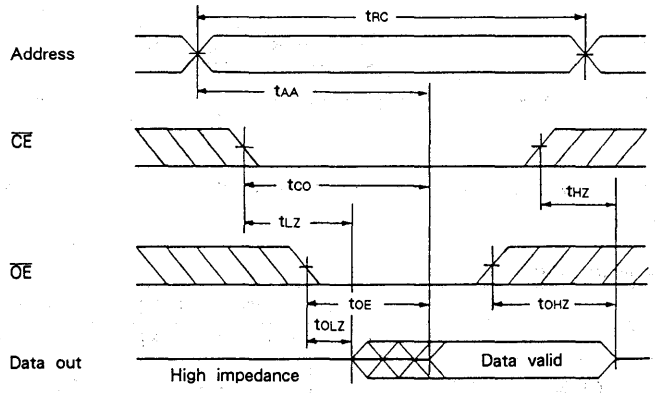
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

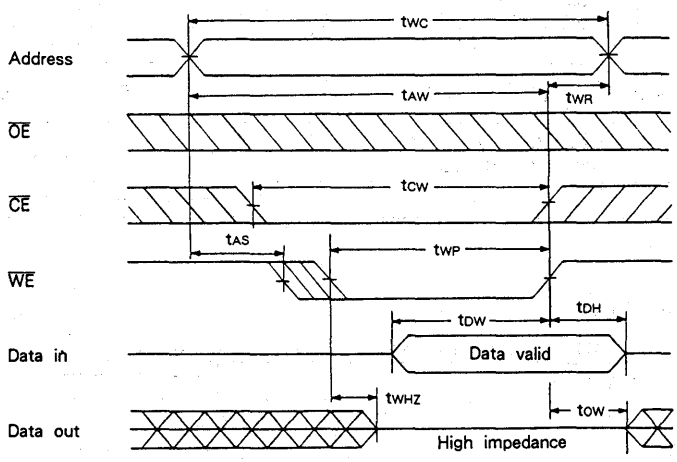
• Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



• Read cycle (2) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



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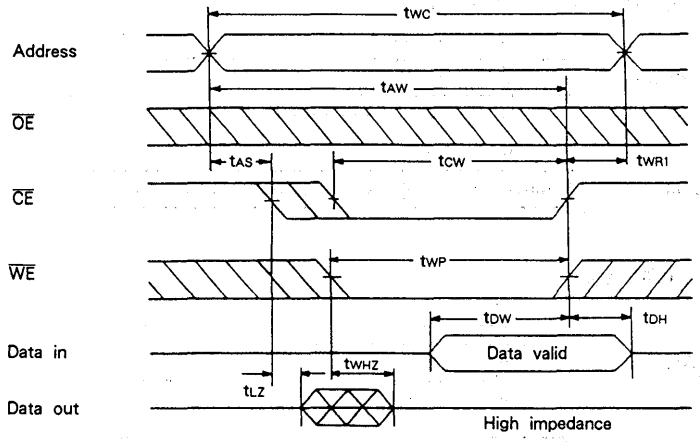
• Write cycle (2) : $\overline{CE}$ control



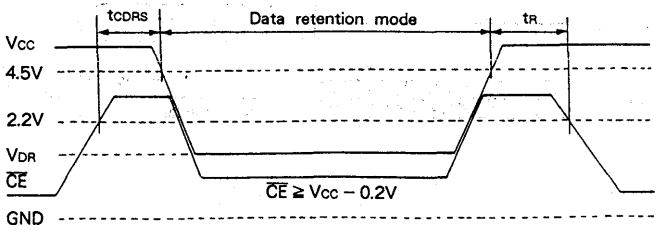
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta = 0 to 70°C)

Item	Symbol	Test conditions		−70L/85L/10L/12L			−70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CE} \geqq 2.8V$	Ta = 0 to 70°C	—	—	10	—	—	3	µA
			Ta = 0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V, $\overline{CE} \geqq V_{CC} - 0.2V$		—	0.5	25	—	0.2	5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

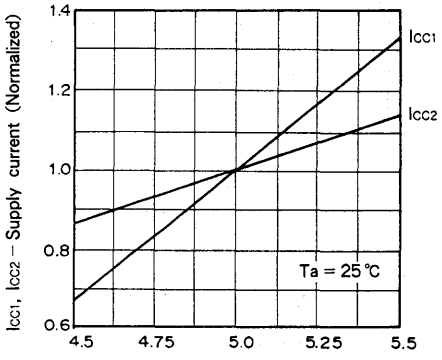
* t_{RC} : Read cycle time

Data retention waveform

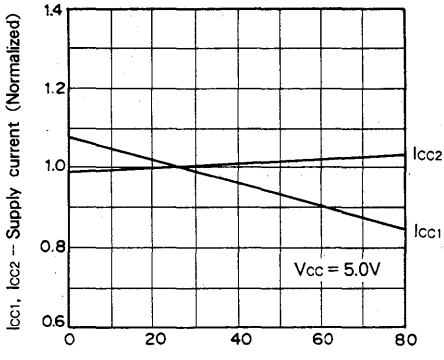


Example of Representative Characteristics

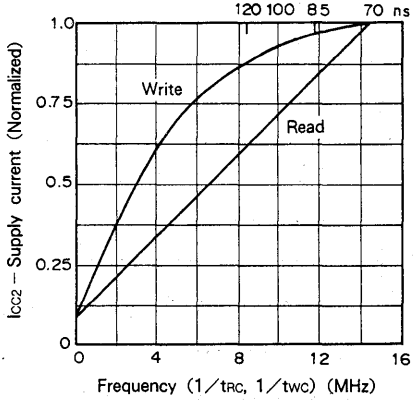
Supply current vs. Supply voltage



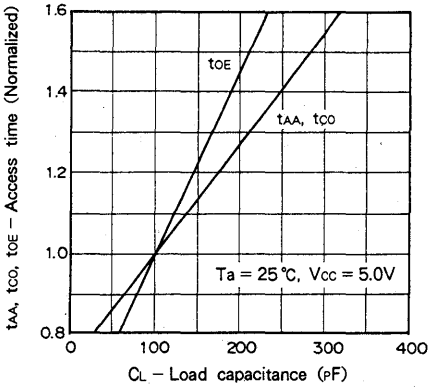
Supply current vs. Ambient temperature



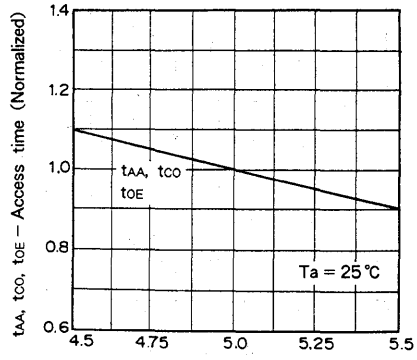
Supply current vs. Frequency



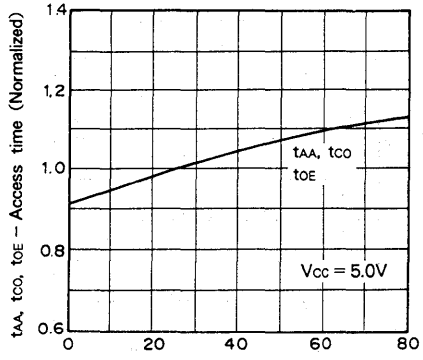
Access time vs. Load capacitance



Access time vs. Supply voltage



Access time vs. Ambient temperature



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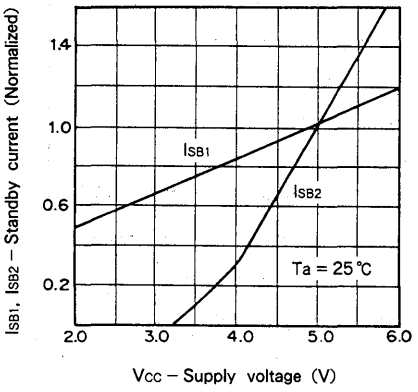
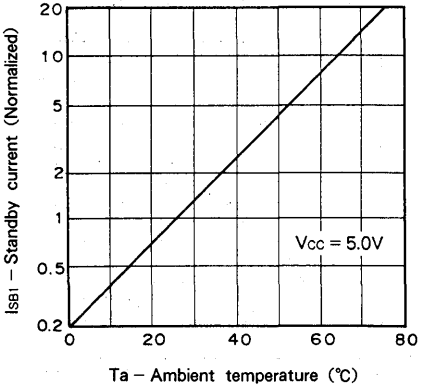
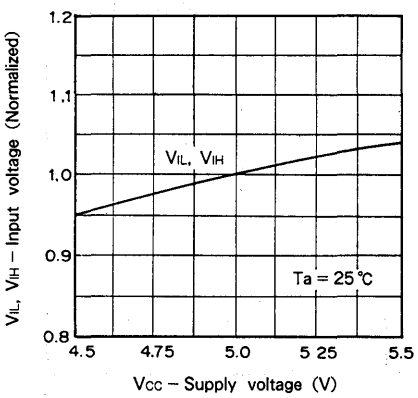
Standby current vs. Supply voltage



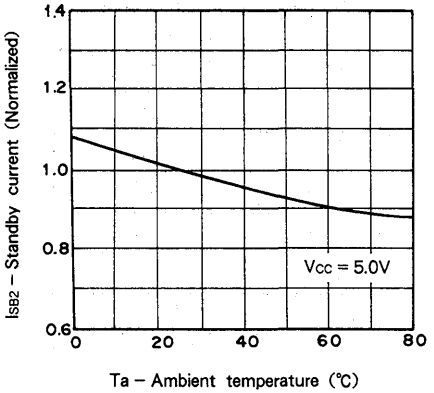
Standby current vs. Ambient temperature



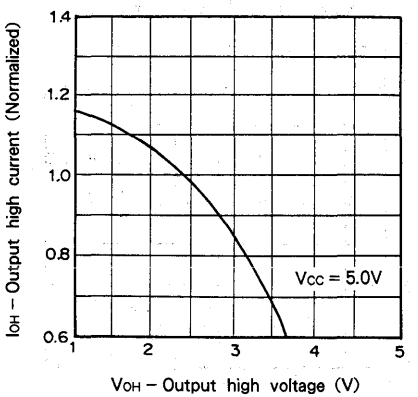
Input voltage level vs. Supply voltage



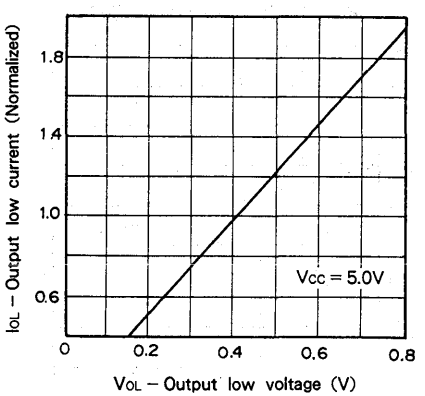
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

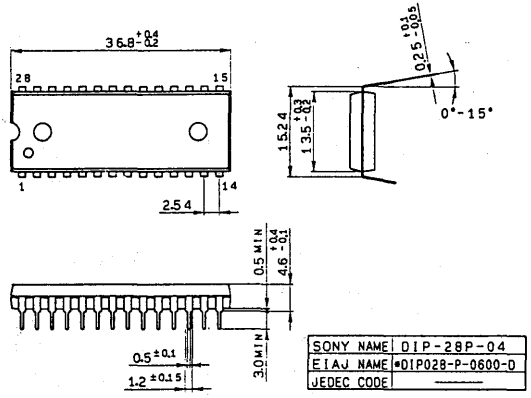


Output low current vs. Output low voltage

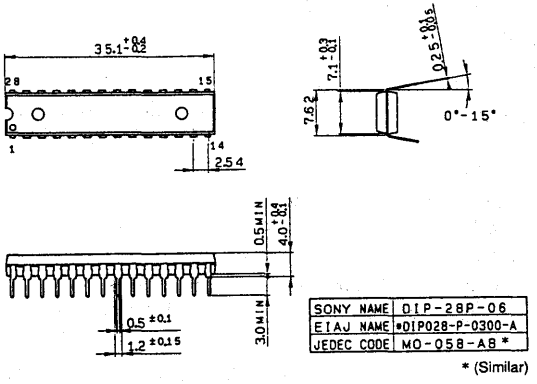


Package Outline Unit : mm

CXK58257AP 28pin DIP (Plastic) 600mil 4.2g

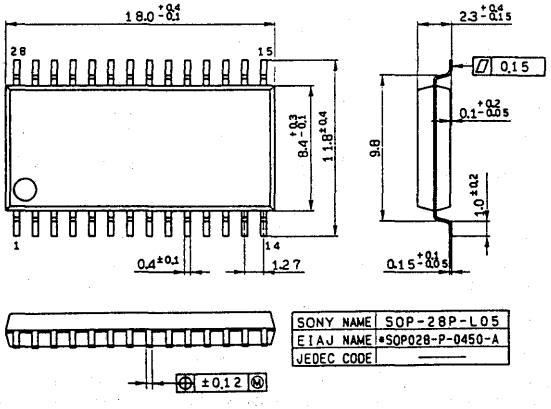


CXK58257ASP 28pin DIP (Plastic) 300mil 2.0g



* (Similar)

CXK58257AM 28pin SOP (Plastic) 450mil 0.7g



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SONY CXK58257AP/ASP/AM -70LX/85LX/10LX/12LX -70LLX/85LLX/10LLX/12LLX

32768-word × 8-bit High Speed CMOS Static RAM

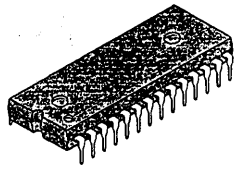
Description

CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

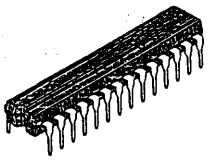
Features

- Extended operating temperature range: –25 to 85 °C
- Fast access time: (Access time)
  CXK58257AP/ASP/AM-70LX,70LLX 70ns (Max.)
  CXK58257AP/ASP/AM-85LX,85LLX 85ns (Max.)
  CXK58257AP/ASP/AM-10LX,10LLX 100ns (Max.)
  CXK58257AP/ASP/AM-12LX,12LLX 120ns (Max.)
- Low power operation:
  CXK58257AP/ASP/AM-70LLX, 85LLX,10LLX,12LLX;
  Standby : 1 μW (Typ.)
  Operation : 15mW (Typ.)
  CXK58257AP/ASP/AM-70LX, 85LX,10LX,12LX;
  Standby : 2.5 μW (Typ.)
  Operation : 15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs

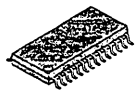
CXK58257AP
28 pin DIP (Plastic)



CXK58257ASP
28 pin DIP (Plastic)



CXK58257AM
28 pin SOP (Plastic)



- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

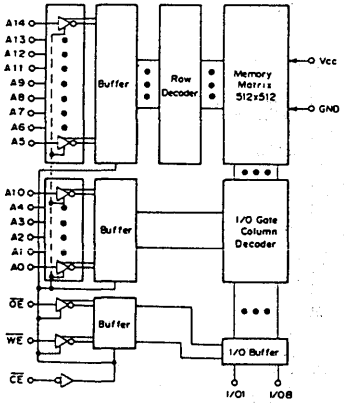
Function

32768-word × 8-bit static RAM

Structure

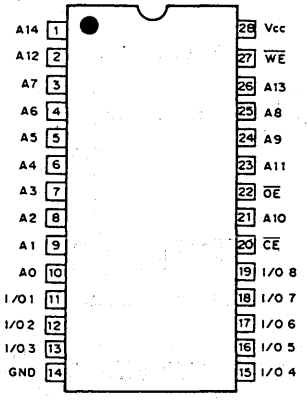
Silicon gate CMOS IC

Block diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A_0 to A_{14}	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to +7.0	V
Input voltage	V_{IN}		− 0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to Vcc +0.5	V
Allowable power dissipation	P_D	CXK58257AP/ASP	1.0	W
		CXK58257AM	0.7	
Operating temperature	Topr		− 25 to +85	℃
Storage temperature	Tstg		− 55 to +150	℃
Soldering temperature • time	Tsolder		260 • 10	℃ • sec

* V_{IN}, $V_{I/O}$= − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Not selected	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

×: "H" or "L"

DC Recommended Operating Conditions (Ta= − 25 to +85℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

* V_{IL}= − 3.0V Min. for pulse width less than 50ns.

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Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta= − 25 to +85°C)

Item	Symbol	Test conditions		−70LX/85LX/10LX/12LX			−70LLX/85LLX/10LLX/12LLX			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		− 0.5	—	0.5	− 0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to Vcc		− 0.5	—	0.5	− 0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		—	3	10	—	3	10	mA
		$\overline{CE}$ ≦ 0.2V V_{IN} ≦ 0.2V or ≧ Vcc−0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0mA	70LX/70LLX	—	30	60	—	30	60	mA
			85LX/85LLX	—	25	60	—	25	60	
			10LX/10LLX	—	23	60	—	23	60	
			12LX/12LLX	—	20	60	—	20	60	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc−0.2V	−25 to 85°C	—	—	50	—	—	10	µA
			−25 to 70°C	—	—	25	—	—	5	
			−25 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$=V_{IH}		—	0.4	2	—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

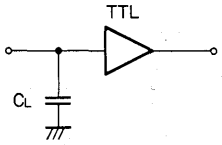
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=–25 to +85°C)

Item		Conditions
Input pulse high level		V_{IH}=2.4V
Input pulse low level		V_{IL}=0.6V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load conditions	85LX/85LLX/10LX/ 10LLX/12LX/12LLX/	C_L * =100pF, 1TTL
	70LX/70LLX	C_L * =30pF, 1TTL



* C_L includes scope and jig capacitances.

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• Read cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t_{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

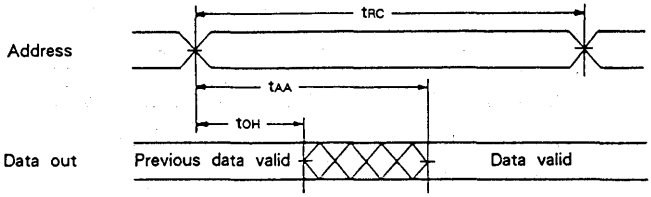
• Write cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	0	25	ns

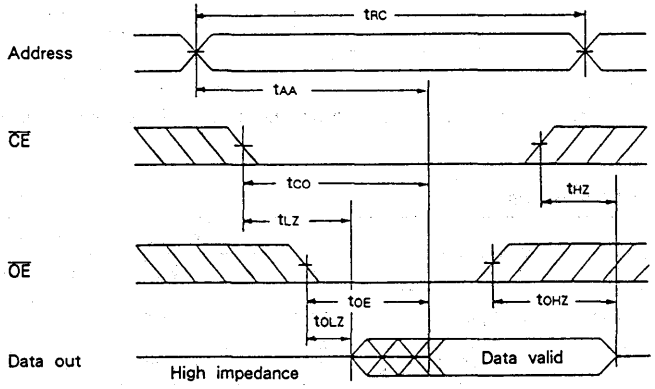
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

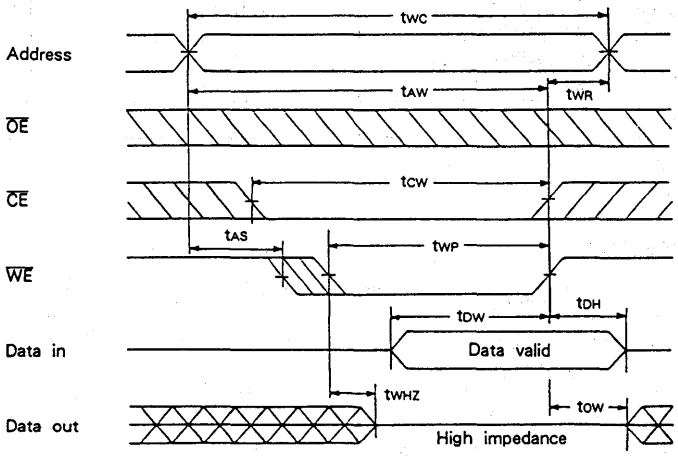
• Read cycle (1) : $\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}



• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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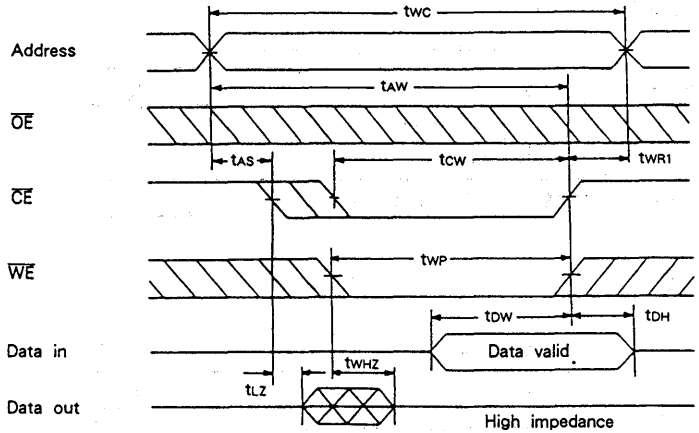
• Write cycle (2) : $\overline{CE}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

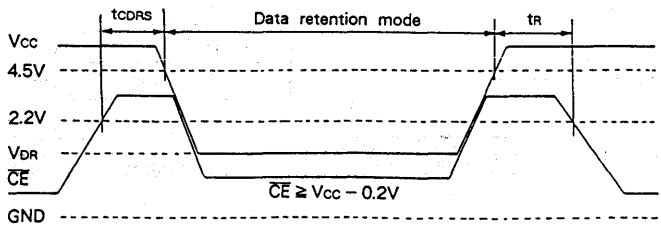
(Ta=–25 to 85 °C)

Item	Symbol	Test conditions		–70LX/85LX/10LX/12LX			–70LLX/85LLX/10LLX/12LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V $\overline{CE} \geqq 2.8V$	–25 to 85 °C	—	—	20	—	—	6	µA
			–25 to 70 °C	—	—	10	—	—	3	
			–25 to 40 °C	—	—	2	—	—	0.6	
			25 °C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V $\overline{CE} \geqq V_{CC}-0.2V$		—	0.5**	50	—	0.2**	10	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

* t_{RC} : Read cycle time

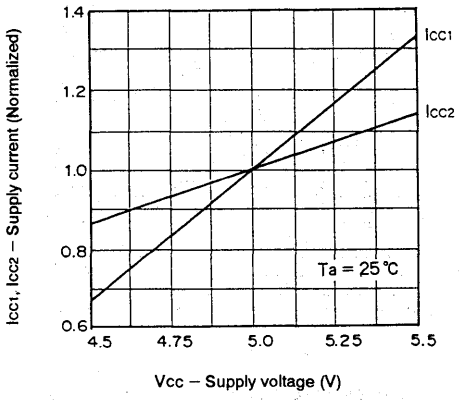
** V_{CC}=5V, Ta=25 °C

Data retention waveform

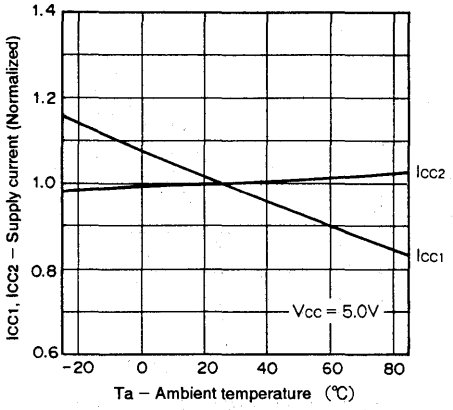


Example of Representative Characteristics

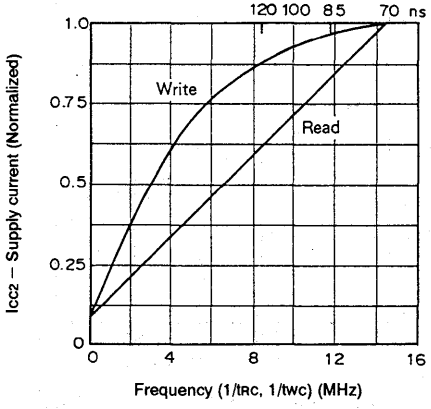
Supply current vs. Supply voltage



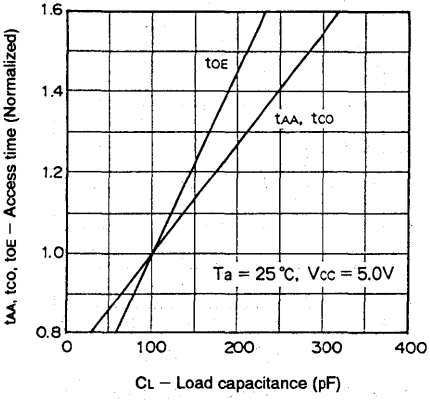
Supply current vs. Ambient temperature



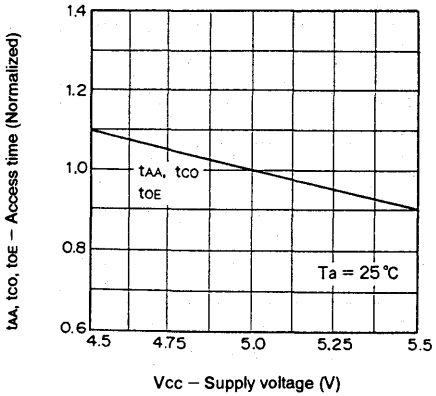
Supply current vs. Frequency



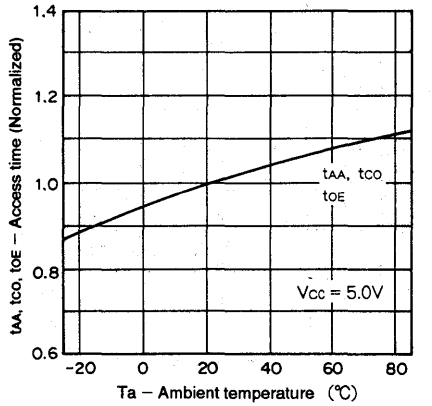
Access time vs. Load capacitance



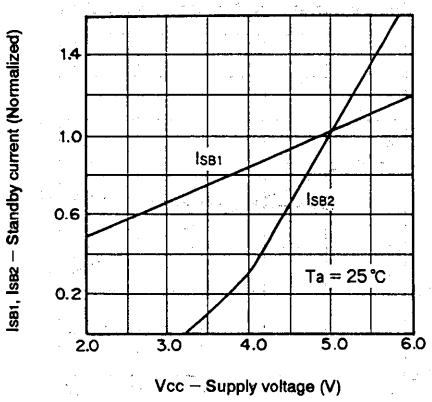
Access time vs. Supply voltage



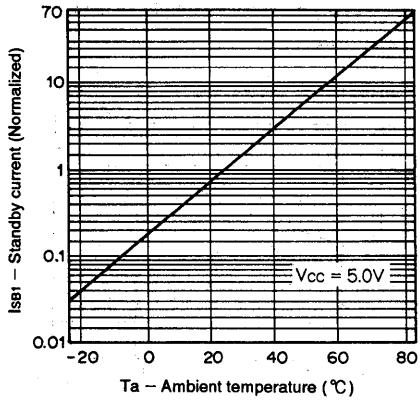
Access time vs. Ambient temperature



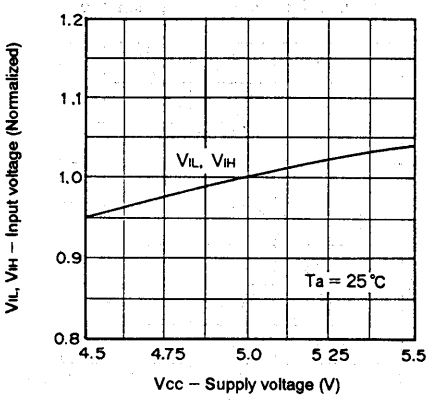
Standby current vs. Supply voltage



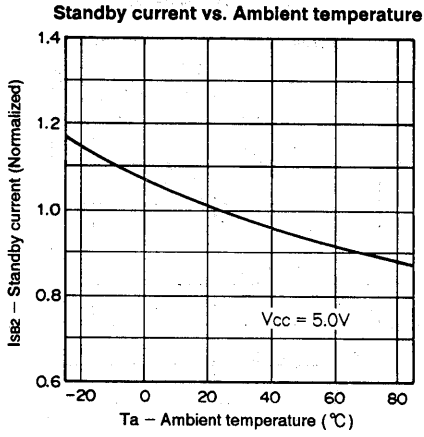
Standby current vs. Ambient temperature



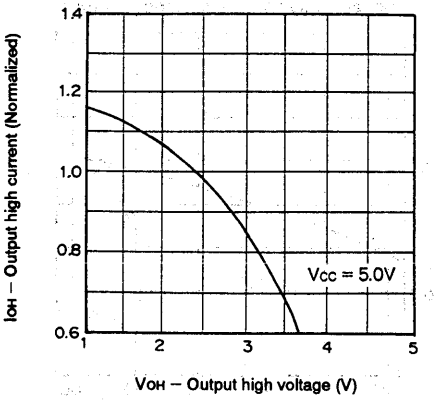
Input voltage level vs. Supply voltage



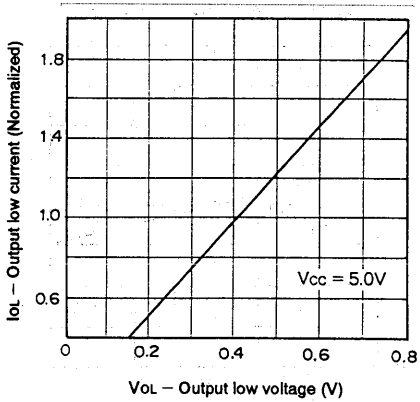
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



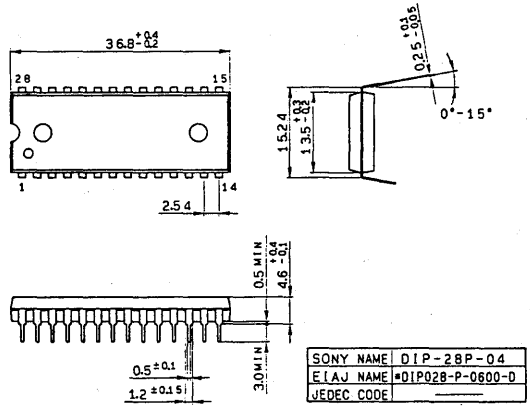
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58257AP

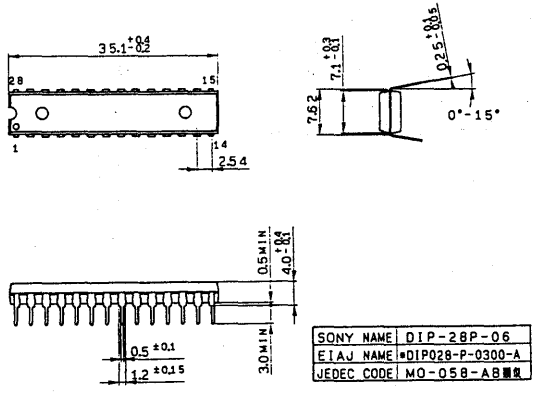
28pin DIP (Plastic) 600mil 4.2g



SONY NAME	DIP-28P-04
EIAJ NAME	*DIP028-P-0600-D
JEDEC CODE	

CXK58257ASP

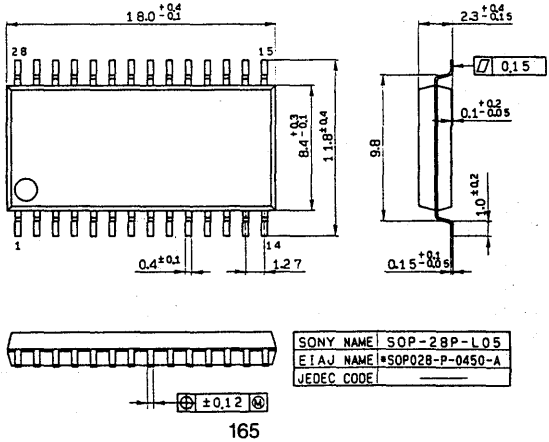
28pin DIP (Plastic) 300mil 2.0g



SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB

CXK58257AM

28pin SOP (Plastic) 450mil 0.7g



SONY NAME	SOP-28P-L05
EIAJ NAME	*SOP028-P-0450-A
JEDEC CODE	

SONY CXK58257ATM/AYM -70L/85L/10L/12L -70LL/85LL/10LL/12LL

32768-word × 8-bit High Speed CMOS Static RAM

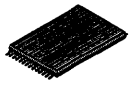
Description

CXK58257ATM/AYM is a 256K bits, 32,768 words by 8 bits, CMOS static RAM.

It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

CXK58257ATM
28 pin TSOP (Plastic)

CXK58257AYM
28 pin TSOP (Plastic)



Features

- Thin Small-outline package :
  CXK58257ATM : 8mm×13.4mm 28 pin TSOP
  CXK58257AYM : 8mm×13.4mm 28 pin TSOP
  (Mirror image pinout)
- Low stand-by current :
  L-Version :
  25 µA (Max.) @Vcc = 5.5V, Ta = 0 to 70℃
  LL-Version :
  5 µA (Max.) @Vcc = 5.5V, Ta = 0 to 70℃
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
  CXK58257ATM/AYM-70L, -70LL 70ns (Max.)
  CXK58257ATM/AYM-85L, -85LL 85ns (Max.)
  CXK58257ATM/AYM-10L, -10LL 100ns (Max.)
  CXK58257ATM/AYM-12L, -12LL 120ns (Max.)
- Single +5V Supply : 5V ± 10%

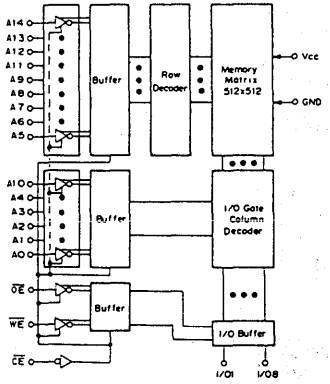
Function

32768-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

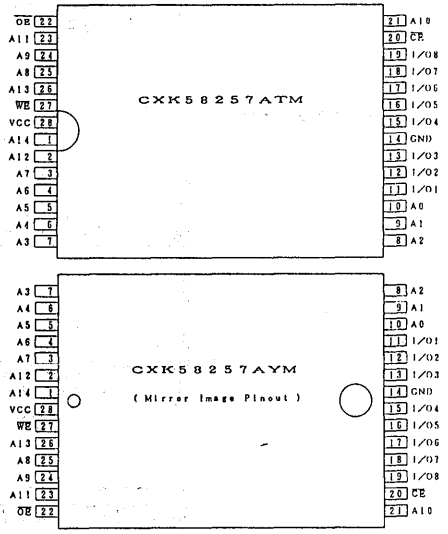


Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

Pin Configuration

(Top View)



Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature	Tsolder	235 • 10	°C • sec

* V_{IN}, $V_{I/O}$ = −3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Not selected	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		−70L/85L/10L/12L			−70LL/85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−0.5	—	0.5	−0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to Vcc		−0.5	—	0.5	−0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE}$ ≦ 0.2V V_{IN} ≦ 0.2V or ≧ Vcc − 0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc − 0.2V	0 to 70°C	—	—	25	—	—	5	µA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$ = V_{IH}		—	0.4	2	—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

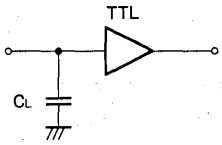
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10%, Ta = 0 to + 70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL	C_L*= 100pF, 1TTL
	70L/70LL	C_L*= 30pF, 1TTL



* C_L includes scope and jig capacitances.

3

• Read cycle

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t_{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t_{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	35	0	40	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

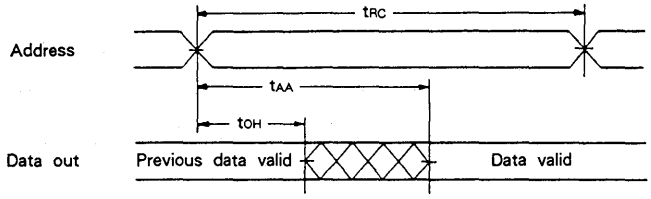
• Write cycle

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	0	25	ns

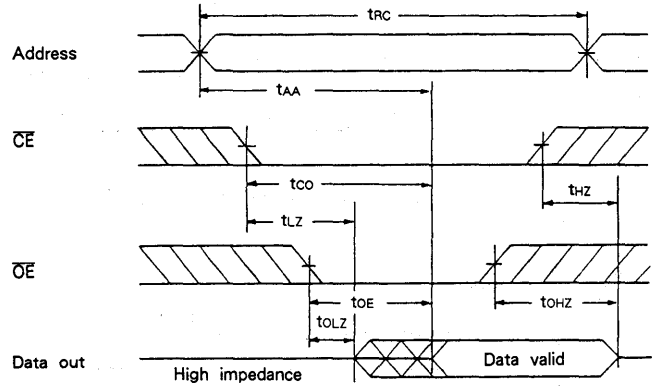
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

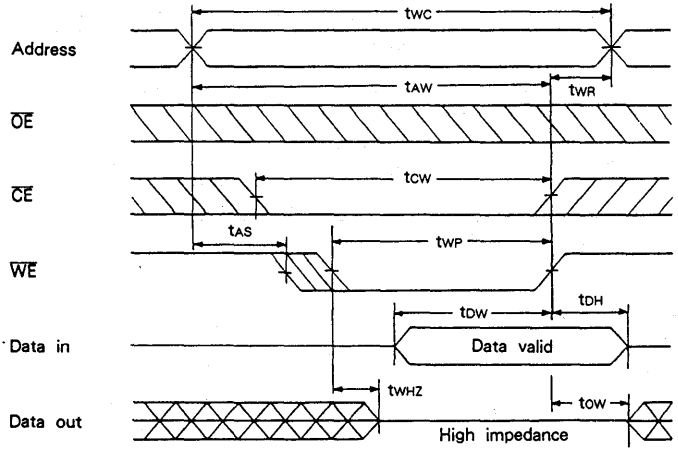
• Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



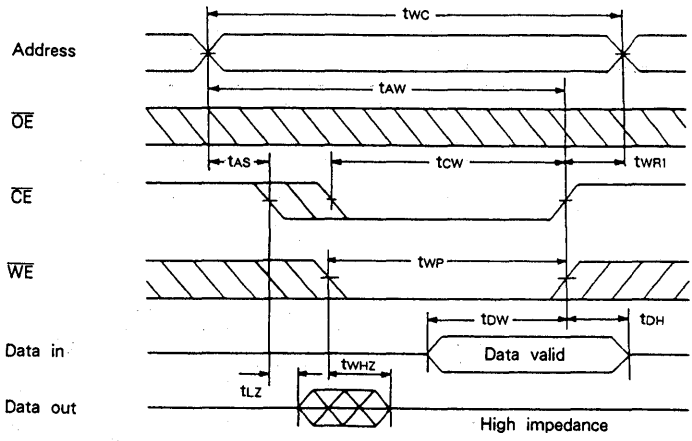
• Read cycle (2) : $\overline{WE} = V_{IH}$



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



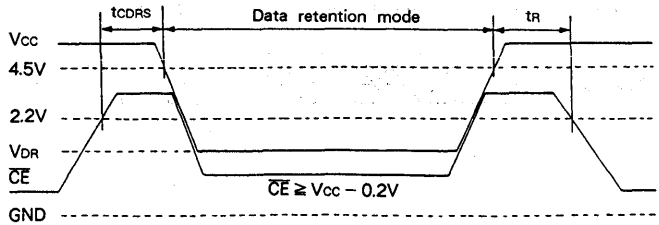
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta = 0 to 70°C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC} - 0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V, $\overline{CE} \geqq 2.8V$	Ta = 0 to 70°C	—	—	10	—	—	3	µA
			Ta = 0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V, $\overline{CE} \geqq V_{CC} - 0.2V$		—	0.5	25	—	0.2	5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

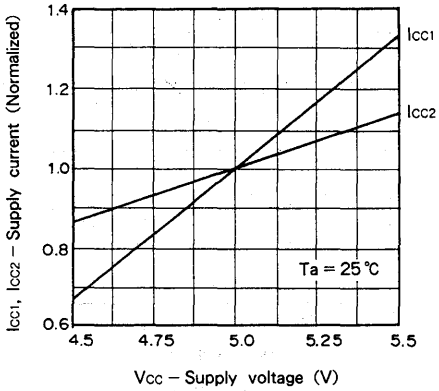
* t_{RC} : Read cycle time

Data retention waveform

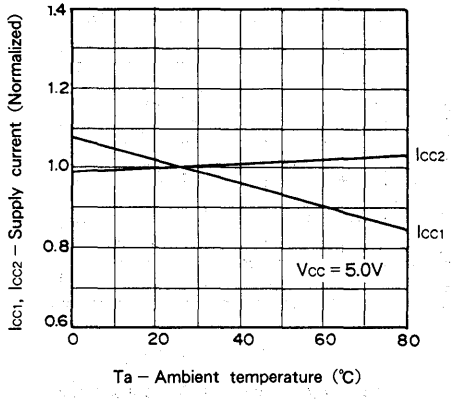


Example of Representative Characteristics

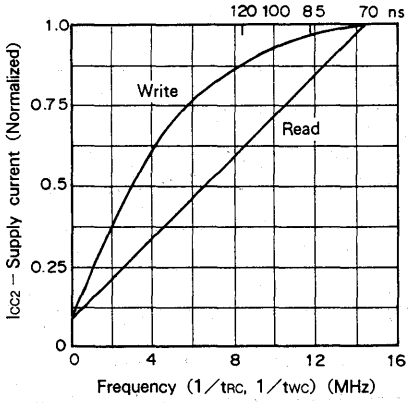
Supply current vs. Supply voltage



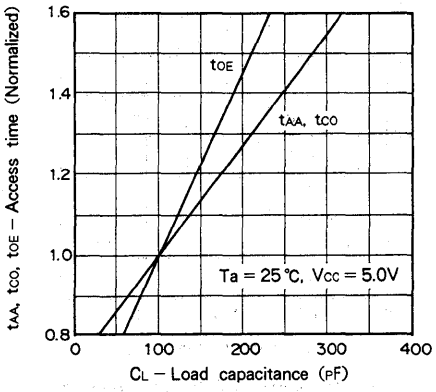
Supply current vs. Ambient temperature



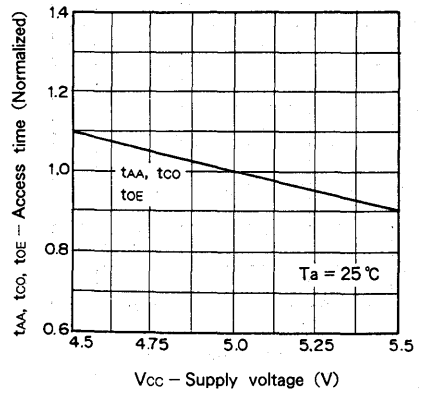
Supply current vs. Frequency



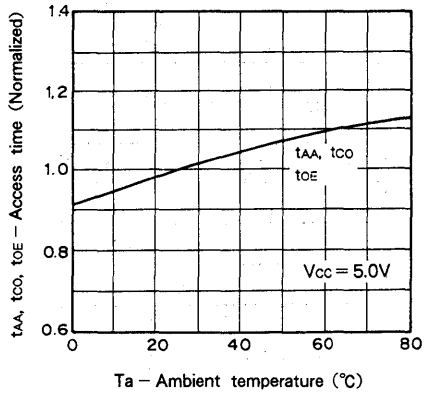
Access time vs. Load capacitance



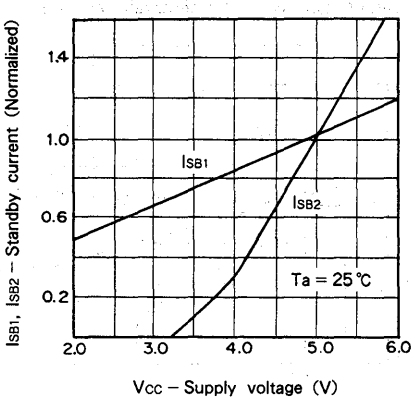
Access time vs. Supply voltage



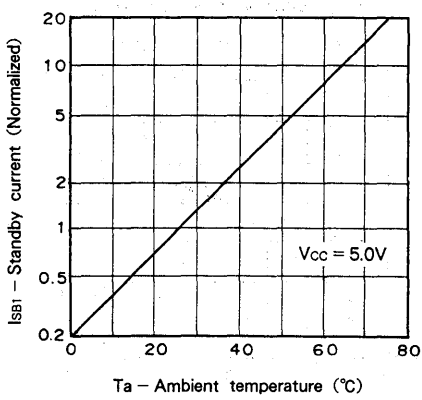
Access time vs. Ambient temperature



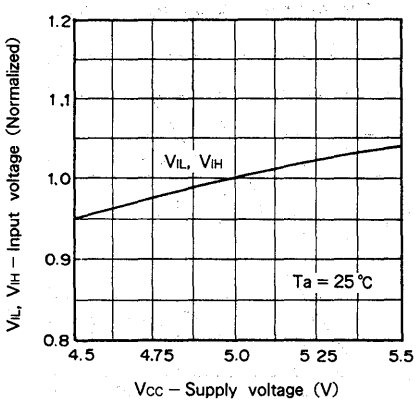
Standby current vs. Supply voltage



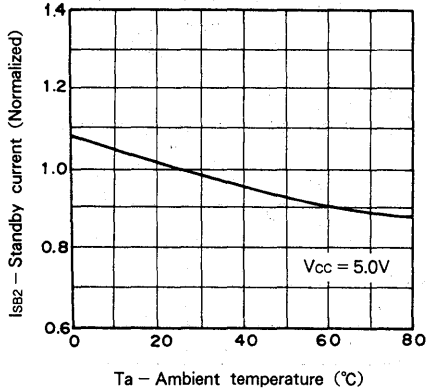
Standby current vs. Ambient temperature



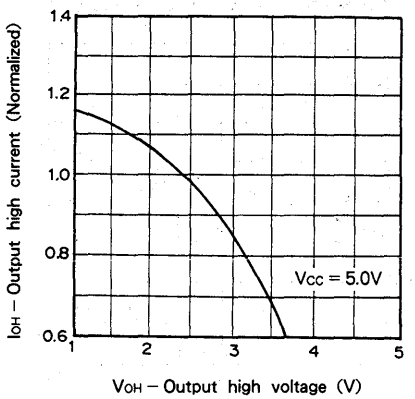
Input voltage level vs. Supply voltage



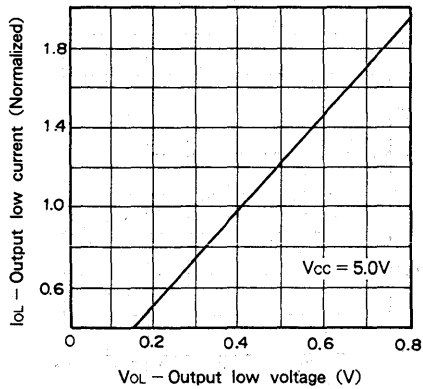
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



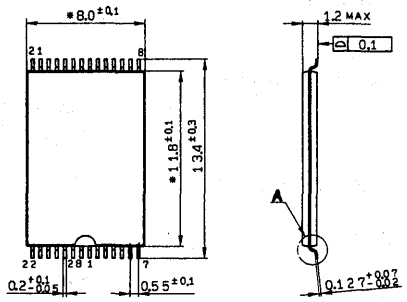
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58257ATM

28pin TSOP (Plastic)

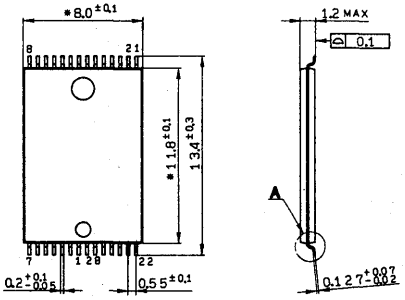


SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	

Note) Dimensions marked with * do not include resin residue.

CXK58257AYM

28pin TSOP (Plastic)



SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	

Note) Dimensions marked with * do not include resin residue.

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SONY CXK58257ATM/AYM -70LX/85LX/10LX/12LX -70LLX/85LLX/10LLX/12LLX

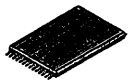
32768-word × 8-bit High Speed CMOS Static RAM

Description

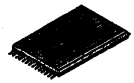
CXK58257ATM/AYM is a 256K bits, 32,768 words by 8 bits, CMOS static RAM.

It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

CXK58257ATM
28 pin TSOP (Plastic)



CXK58257AYM
28 pin TSOP (Plastic)



Features

- Extended operation temperature range: –25 to +85 °C
- Thin small-outline package:
  CXK58257ATM: 8mm × 13.4mm 28 pin TSOP
  CXK58257AYM: 8mm × 13.4mm 28 pin TSOP
  (Mirror image pinout)
- Low stand-by current:
  L-Version:
  50 µA (Max.) @Vcc=5.5V, Ta=–25 to +85 °C
  LL-Version:
  10 µA (Max.) @Vcc=5.5V, Ta=–25 to +85 °C
- Low voltage data retention: 2.0V (Min.)
- Fast access time: (Access time)
  CXK58257ATM/AYM-70LX, -70LLX 70ns (Max.)
  CXK58257ATM/AYM-85LX, -85LLX 85ns (Max.)
  CXK58257ATM/AYM-10LX, -10LLX 100ns (Max.)
  CXK58257ATM/AYM-12LX, -12LLX 120ns (Max.)
- Single +5V Supply: 5V ± 10%

Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground

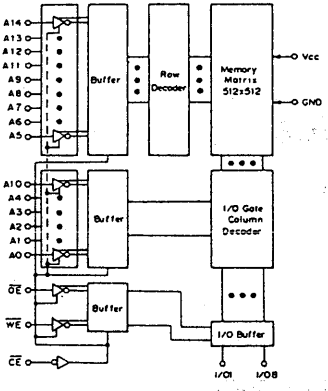
Function

32768-word × 8-bit static RAM

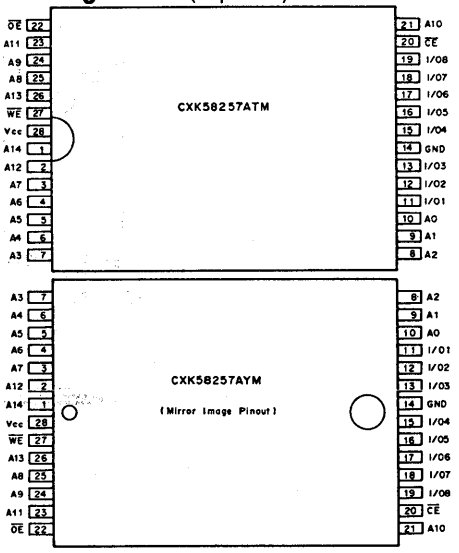
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc +0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	−25 to +85	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature • time	Tsolder	235 • 10	℃ • sec

* V_{IN}, $V_{I/O}$=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Not selected	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=−25 to +85℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	V

* V_{IL}=−3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=–25 to +85°C)

Item	Symbol	Test conditions		–70LX/85LX/10LX/12LX			–70LLX/85LLX/10LLX/12LLX			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–0.5	—	0.5	–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to Vcc		–0.5	—	0.5	–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		—	3	10	—	3	10	mA
		$\overline{CE}$ ≦ 0.2V V_{IN} ≦ 0.2V or ≧ Vcc–0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Cycle=Min, Duty=100% I_{OUT}=0mA	70LX/70LLX	—	30	60	—	30	60	mA
			85LX/85LLX	—	25	60	—	25	60	
			10LX/10LLX	—	23	60	—	23	60	
			12LX/12LLX	—	20	60	—	20	60	
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc–0.2V	–25 to +85°C	—	—	50	—	—	10	µA
			–25 to +70°C	—	—	25	—	—	5	
			–25 to +40°C	—	—	5	—	—	1	
			+25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	$\overline{CE}$=V_{IH}		—	0.4	2	—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

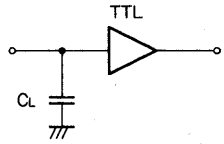
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=–25 to +85°C)

Item		Conditions
Input pulse high level		V_{IH}=2.4V
Input pulse low level		V_{IL}=0.6V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load conditions	85LX/85LLX/10LX/ 10LLX/12LX/12LLX	C_L * =100pF, 1TTL
	70LX/70LLX	C_L * =30pF, 1TTL



* C_L includes scope and jig capacitances.

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• Read cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t_{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t_{OH}	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

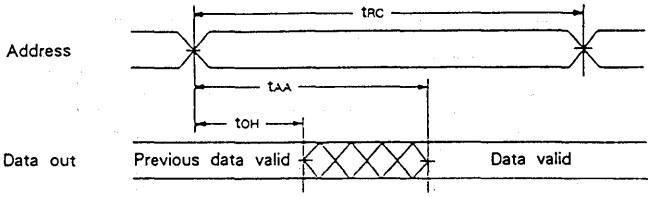
• Write cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	0	25	ns

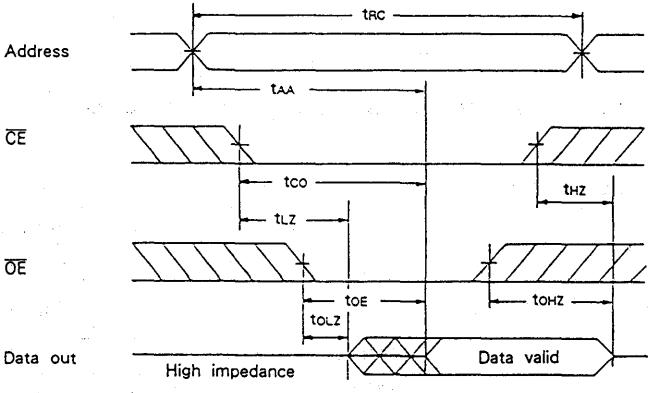
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

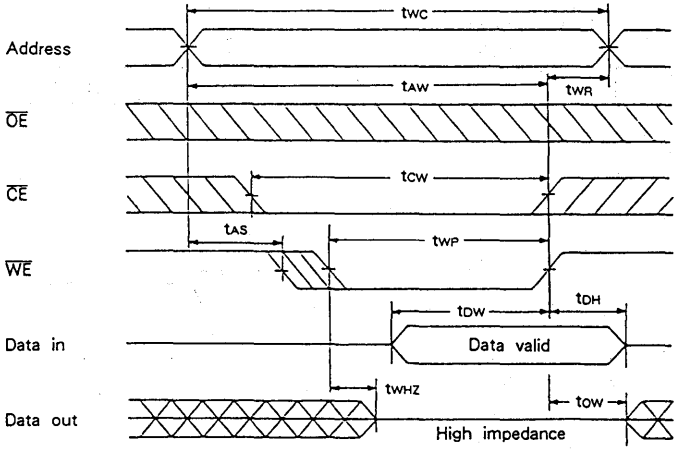
• Read cycle (1) : $\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}



• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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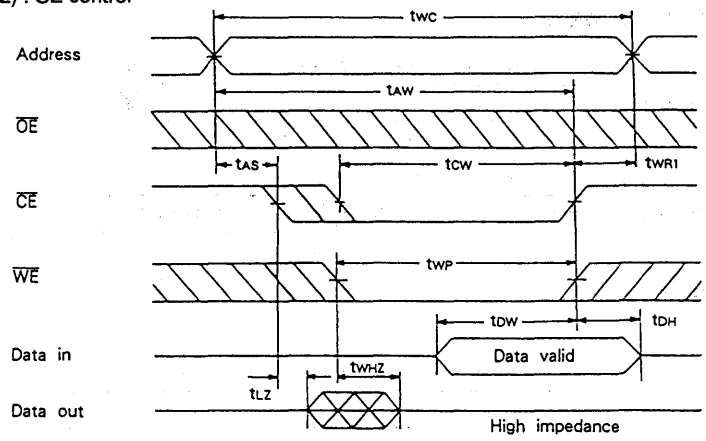
• Write cycle (2) : $\overline{CE}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

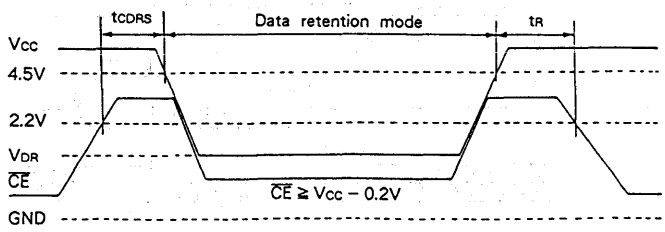
(Ta=–25 to +85 °C)

Item	Symbol	Test conditions		–70LX/85LX/10LX/12LX			–70LLX/85LLX/10LLX/12LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V $\overline{CE} \geqq 2.8V$	–25 to +85 °C	—	—	20	—	—	6	µA
			–25 to +70 °C	—	—	10	—	—	3	
			–25 to +40 °C	—	—	2	—	—	0.6	
			+25 °C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V $\overline{CE} \geqq V_{CC}-0.2V$		—	0.5**	50	—	0.2**	10	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

* t_{RC} : Read cycle time

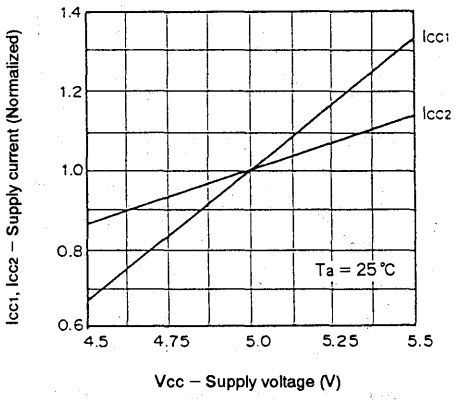
** V_{CC}=5V, Ta=25 °C

Data Retention Waveform

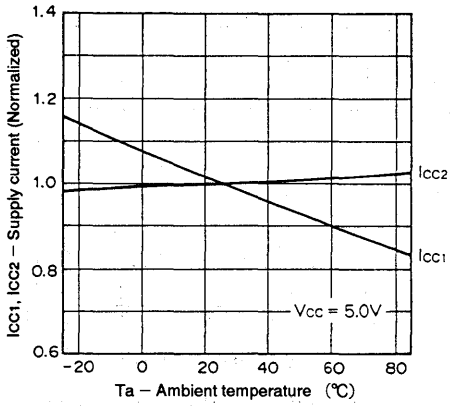


Example of Representative Characteristics

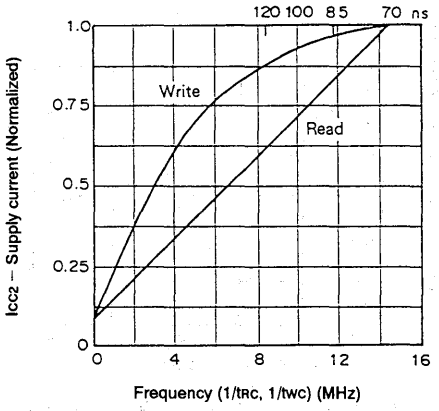
Supply current vs. Supply voltage



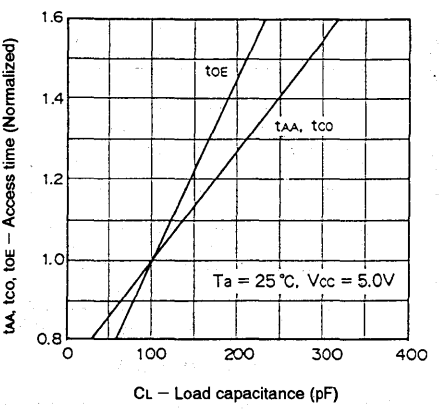
Supply current vs. Ambient temperature



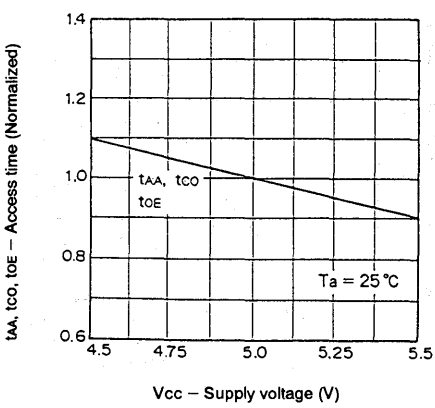
Supply current vs. Frequency



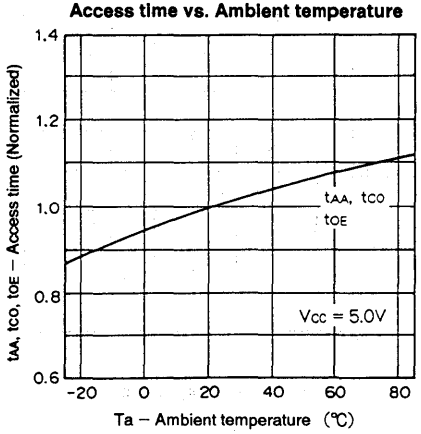
Access time vs. Load capacitance



Access time vs. Supply voltage



Access time vs. Ambient temperature



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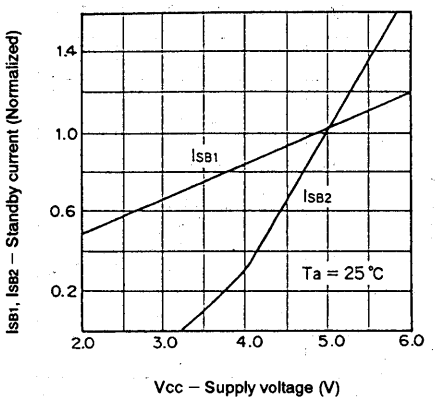
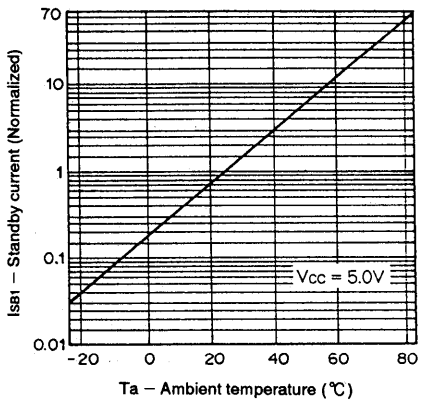
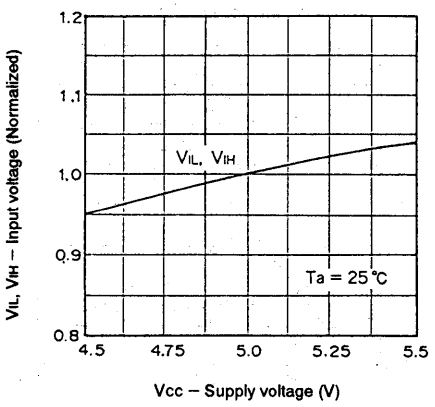
Standby current vs. Supply voltage



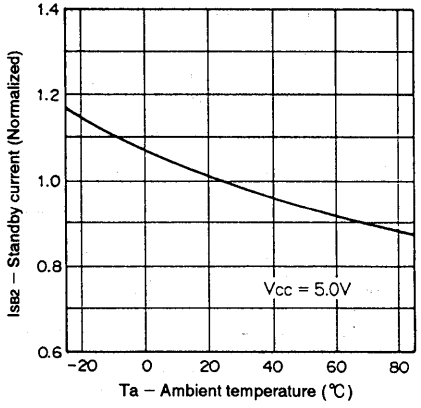
Standby current vs. Ambient temperature



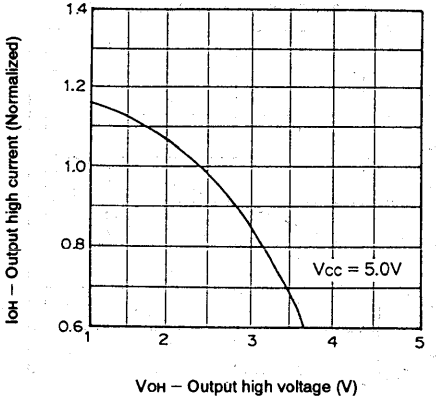
Input voltage level vs. Supply voltage



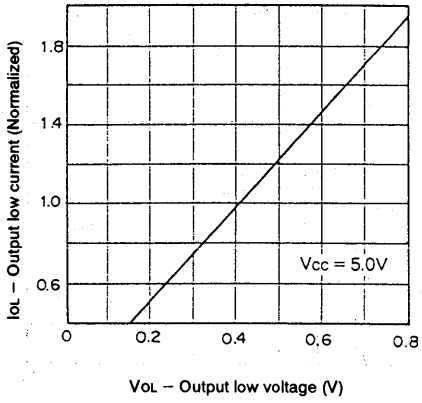
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



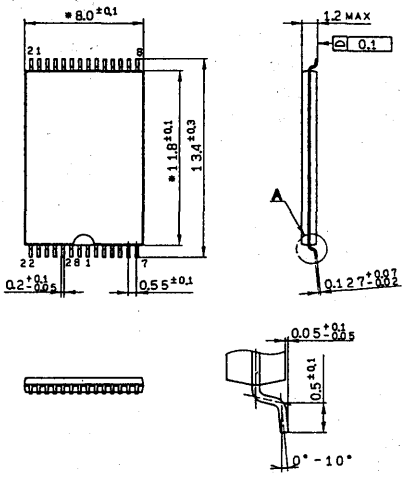
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58257ATM

28pin TSOP (Plastic)



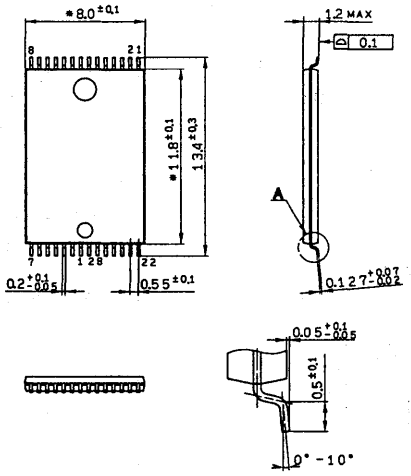
Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	———

CXK58257AYM

28pin TSOP (Plastic)



Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	———

32768-word × 8 bit High Speed CMOS Static RAM

Description

CXK58257P/SP/M is a 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
  - CXK58257P/SP/M–70L, 70LL: 70ns (Max.)
  - CXK58257P/SP/M–85L, 85LL: 85ns (Max.)
  - CXK58257P/SP/M–10L, 10LL: 100ns (Max.)
  - CXK58257P/SP/M–12L, 12LL: 120ns (Max.)
- Low power operation:
  CXK58257P/SP/M–70LL, 85LL, 10LL, 12LL:
  Standby/Operation: 5 μW (Typ.)/40 mW (Typ.)
  CXK58257P/SP/M–70L, 85L, 10L, 12L:
  Standby/Operation: 10 μW (Typ.)/40 mW (Typ.)
- Single +5V supply: +5V ±10%
- Fully static memory . . . No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28pin 600-mil DIP, 300-mil DIP and 450-mil SOP

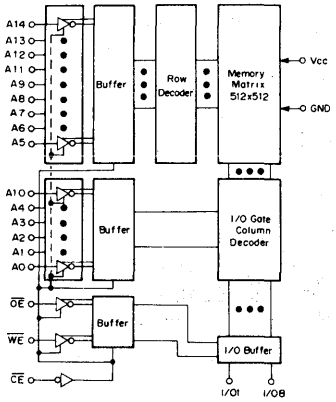
Function

32768-word × 8 bit static RAM

Structure

Silicon gate CMOS IC

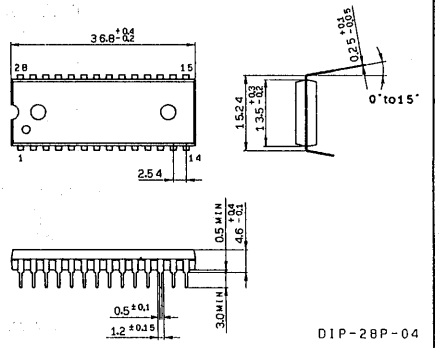
Block Diagram



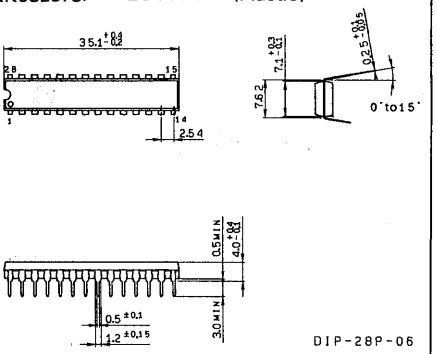
Package Outline

Unit: mm

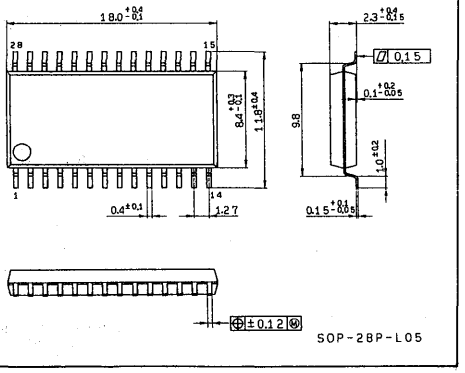
CXK58257P 28 Pin DIP (Plastic)



CXK58257SP 28 Pin DIP (Plastic)

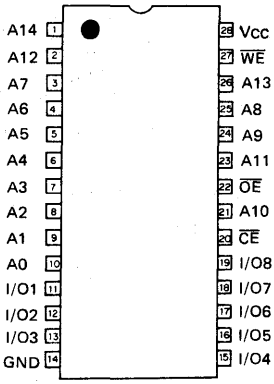


CXK58257M 28 Pin SOP (Plastic)



70707B-ST

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	Vcc		−0.5 to +7.0	V
Input voltage	VIN		−0.5* to Vcc+0.5	V
Input and output voltage	VI/O		−0.5* to Vcc+0.5	V
Allowable power dissipation	PD	CXK58257P/SP	1.0	W
		CXK58257M	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature	Tsolder		260·10	°C·sec

***Note)** VIN, VI/O=−3.0V Min. for pulse width less than 50 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not Selected	High Z	ISB1, ISB2
L	H	H	Output Disable	High Z	ICC1, ICC2
L	L	H	Read	Data out	ICC1, ICC2
L	X	L	Write	Data in	ICC1, ICC2

Note) X: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	VIH	2.2	−	Vcc+0.3	V
Input low voltage	VIL	−0.3*	−	0.8	V

***Note)** VIL=−3.0V Min. for pulse width less than 50 ns.

Electrical Characteristics

DC and operating characteristics

(Vcc=5V±10%, GND=0V, Ta=0 to+70°C)

Item	Symbol	Test condition		CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}		−0.5	−	0.5	−0.5	−	0.5	μA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} $V_{I/O}$=GND to V_{CC}		−0.5	−	0.5	−0.5	−	0.5	μA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		−	8	15	−	8	15	mA
		$\overline{CE}$≦0.2V V_{IN}≦0.2V or≧V_{CC}−0.2V		−	3	7	−	3	7	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	70L/70LL	−	45	70	−	45	70	mA
			85L/85LL	−	40	70	−	40	70	mA
			10L/10LL	−	35	70	−	35	70	mA
			12L/12LL	−	30	70	−	30	70	mA
Standby current	I_{SB1}	$\overline{CE}$≧V_{CC}−0.2V		−	0.002	0.1	−	0.001	0.05	mA
	I_{SB2}	$\overline{CE}$=V_{IH}		−	0.2	2	−	0.2	2	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.4	−	−	2.4	−	−	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		−	−	0.4	−	−	0.4	V

***Note)** V_{CC}=5V, Ta=25°C

Capacitance

(Ta=25°C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	−	6	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0V	−	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (V_{CC}=5V±10%, Ta=0 to +70°C)

Item		Condition
Input pulse high level		V_{IH}=2.2V
Input pulse low level		V_{IL}=0.8V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load	85L/85LL/10L/10LL 12L/12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL

* C_L includes scope and jig capacitances.

• **Read cycle**

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	–	85	–	100	–	120	–	ns
Address access time	t_{AA}	–	70	–	85	–	100	–	120	ns
Chip enable access time	t_{CO}	–	70	–	85	–	100	–	120	ns
Output enable to output valid	t_{OE}	–	35	–	45	–	50	–	60	ns
Output hold from address change	t_{OH}	5	–	5	–	10	–	10	–	ns
Chip enable to output in low Z($\overline{CE}$)	t_{LZ}	10	–	10	–	10	–	10	–	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	0	30	0	30	0	35	0	40	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	30	0	30	0	35	0	40	ns

***Note)** t_{HZ} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

• **Write cycle**

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	–	85	–	100	–	120	–	ns
Address valid to end of write	t_{AW}	65	–	75	–	80	–	100	–	ns
Chip enable to end of write	t_{CW}	65	–	75	–	80	–	100	–	ns
Data to write time overlap	t_{DW}	30	–	40	–	40	–	50	–	ns
Data hold from write time	t_{DH}	0	–	0	–	0	–	0	–	ns
Write pulse width	t_{WP}	55	–	60	–	70	–	80	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	–	0	–	0	–	0	–	ns
Write recovery time ($\overline{CE}$)	t_{WR1}	0	–	0	–	0	–	0	–	ns
Output active from end of write	t_{OW}	5	–	5	–	10	–	10	–	ns
Write to output in high Z	t_{WHZ}*	0	30	0	30	0	30	0	30	ns

***Note)** t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

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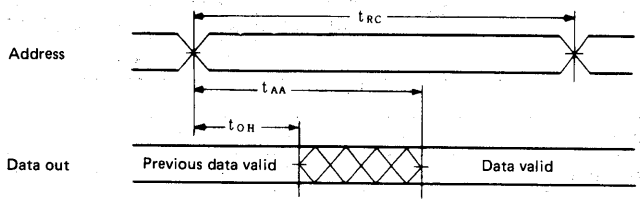
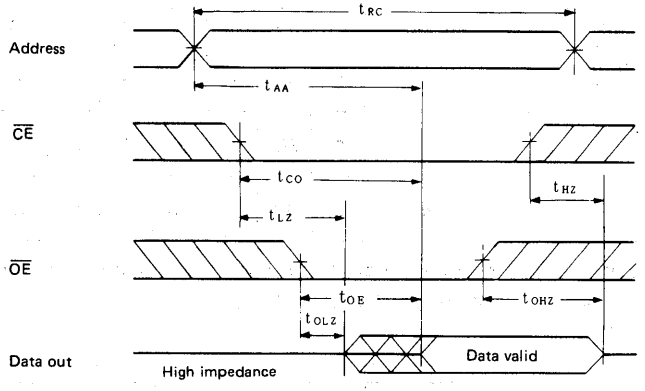
Timing Waveform

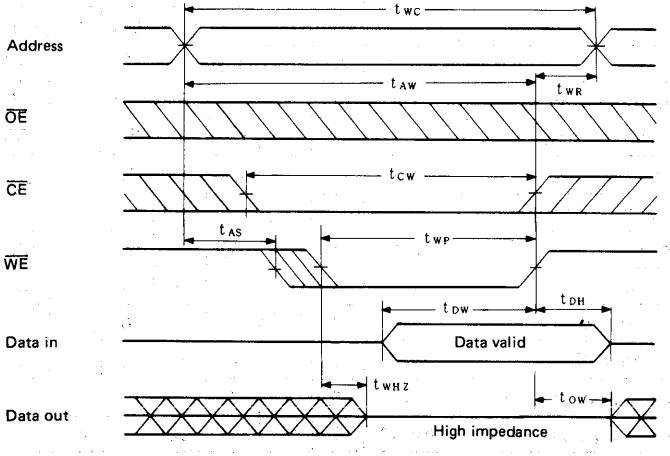
- Read cycle (1): $\overline{CE}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$



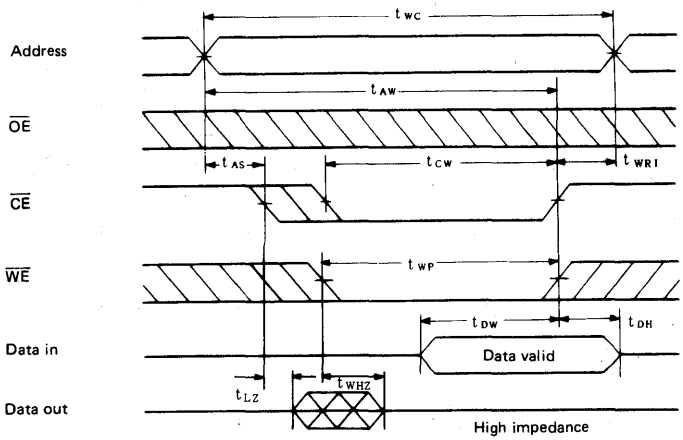
- Read cycle (2): $\overline{WE}=V_{IH}$



- Write cycle (1): $\overline{WE}$ control



- Write cycle (2): $\overline{CE}$ control



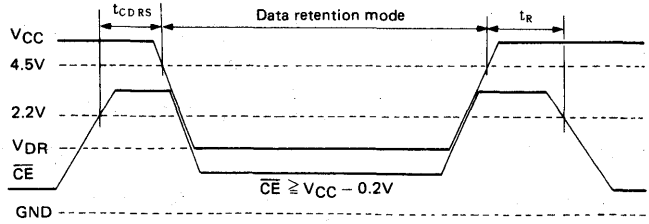
During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics (Ta=0 to 70°C)

Item	Symbol	Test condition		CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geqq V_{CC}-0.2V$		2.0	–	5.5	2.0	–	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V, $\overline{CE} \geqq 2.8V$	Ta=0°C to 70°C	–	1	50	–	0.4	10	μA
			Ta=0 C to 50°C	–	–	–	–	0.4	5	
			25°C	–	–	–	–	0.4	1	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V, $\overline{CE} \geqq V_{CC}-0.2V$		–	0.002	0.1	–	0.001	0.05	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	–	–	0	–	–	ns
Recovery time	t_R			t_{RC}*	–	–	t_{RC}*	–	–	ns

* t_{RC}: Read cycle time

- **Data retention waveform**



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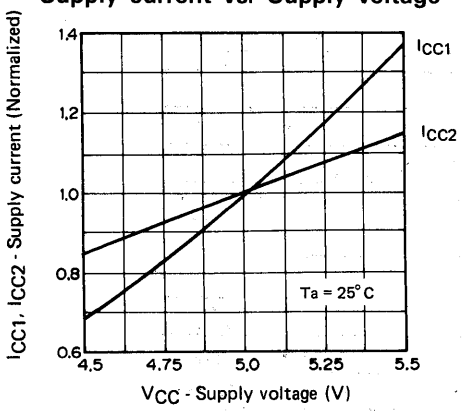
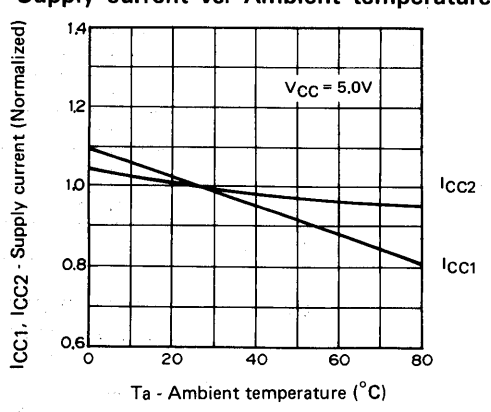
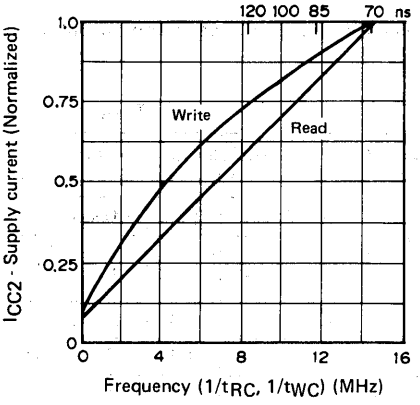
Supply current vs. Supply voltage



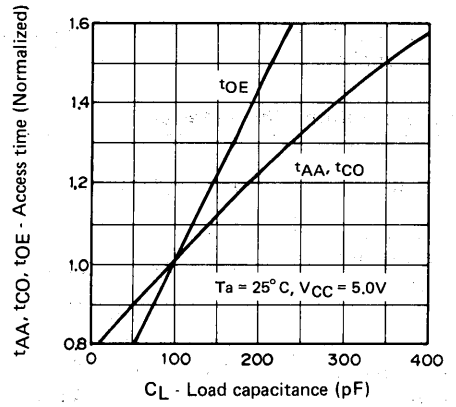
Supply current vs. Ambient temperature



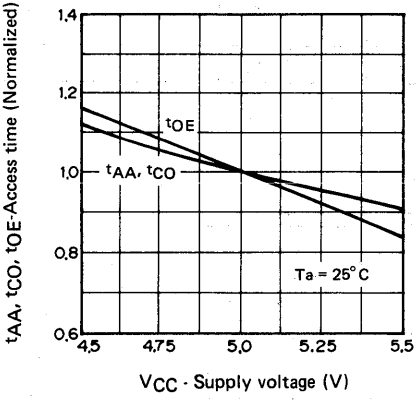
Supply current vs. Frequency



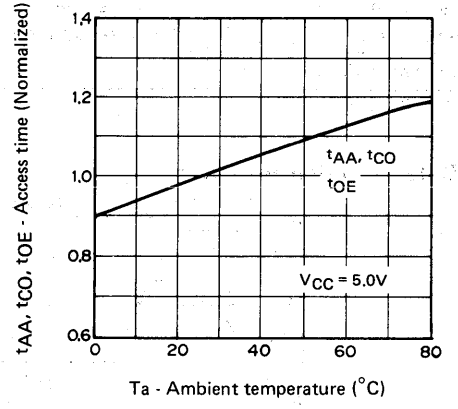
Access time vs. Load capacitance



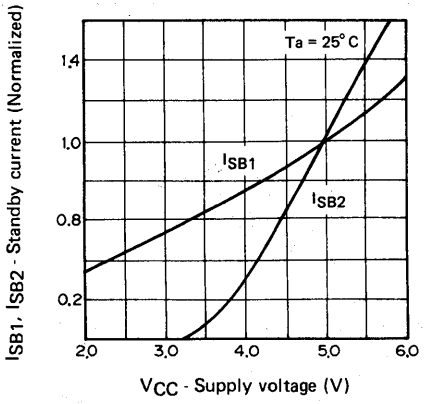
Access time vs. Supply voltage



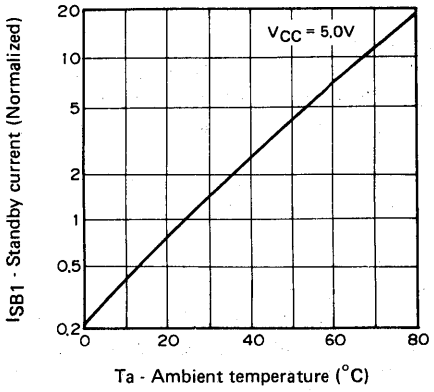
Access time vs. Ambient temperature



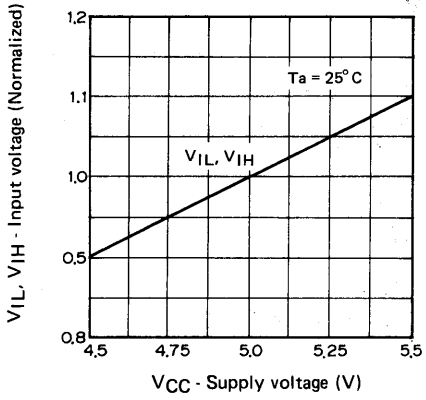
Standby current vs. Supply voltage



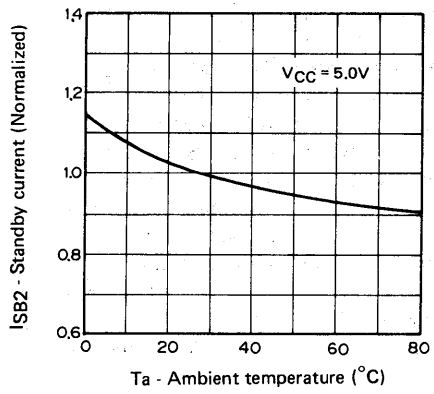
Standby current vs. Ambient temperature



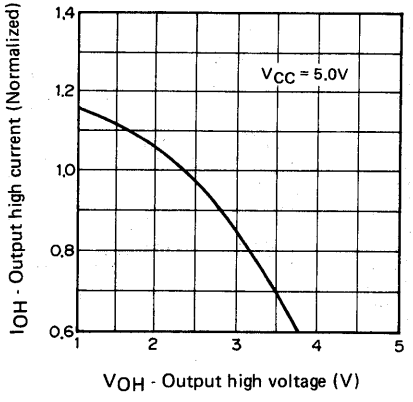
Input voltage vs. Supply voltage



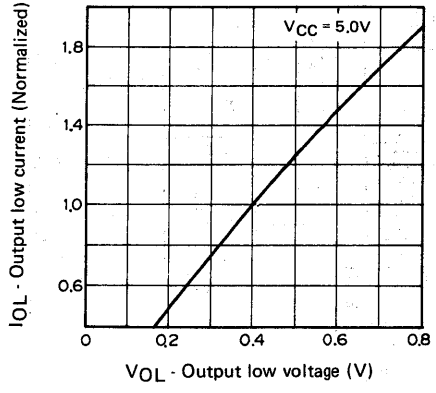
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



3

SONY CXK58267AP/ASP/AM -70L/85L/10L/12L -70LL/85LL/10LL/12LL

32768-word × 8-bit High Speed CMOS Static RAM

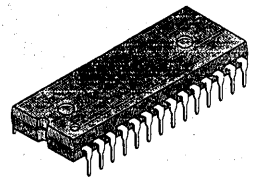
Description

CXK58267AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. The CXK58267AP/ASP/AM's two chip enable inputs are useful for battery back up operation for nonvolatility.

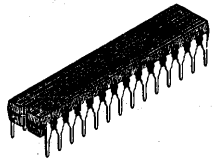
Features

- Fast access time : (Access time)
  CXK58267AP/ASP/AM-70L, 70LL 70ns(Max.)
  CXK58267AP/ASP/AM-85L, 85LL 85ns(Max.)
  CXK58267AP/ASP/AM-10L, 10LL 100ns(Max.)
  CXK58267AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
  CXK58267AP/ASP/AM-70LL, 85LL, 10LL, 12LL ;
  Standby : 1 μW (Typ.)
  Operation : 15mW (Typ.)
  CXK58267AP/ASP/AM-70L, 85L, 10L, 12L ;
  Standby : 2.5 μW (Typ.)
  Operation : 15mW (Typ.)
- Single +5V supply : +5V ± 10%
- Fully static memory···No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs

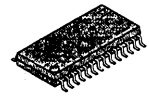
CXK58267AP
28 pin DIP (Plastic)



CXK58267ASP
28 pin DIP (Plastic)



CXK58267AM
28 pin SOP (Plastic)



- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

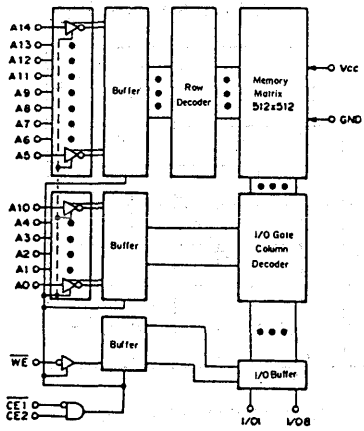
Function

32768-word × 8-bit static RAM

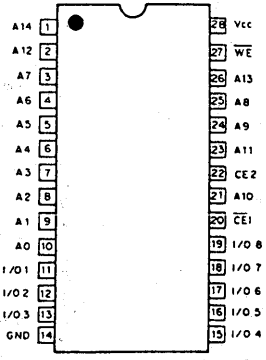
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
Vcc	+5V power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to + 7.0	V
Input voltage	V_{IN}		− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK58267AP/ASP	1.0	W
		CXK58267AM	0.7	
Operating temperature	Topr		0 to + 70	℃
Storage temperature	Tstg		− 55 to + 150	℃
Soldering temperature • time	Tsolder		260 • 10	℃ • sec

* V_{IN}, $V_{I/O}$ = − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−0.5	—	0.5	−0.5	—	0.5	μA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to Vcc		−0.5	—	0.5	−0.5	—	0.5	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, I_{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE1}$ = 0.2V, CE2 = Vcc − 0.2V V_{IN} = 0.2V or Vcc − 0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Min. cycle Duty = 100%, I_{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I_{SB1}	CE2 ≦ 0.2V or ($\overline{CE1}$ ≧ Vcc − 0.2V, CE2 ≧ Vcc − 0.2V)	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	CE2 = V_{IL}, or $\overline{CE1}$ = V_{IH}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

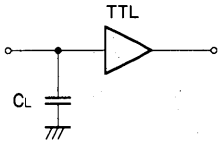
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions (Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	85L / 85LL / 10L / 10LL / 12L / 12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL



* C_L includes scope and jig capacitances.

• **Read cycle**

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time ($\overline{CE1}$, CE2)	t_{CO1}, t_{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t_{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

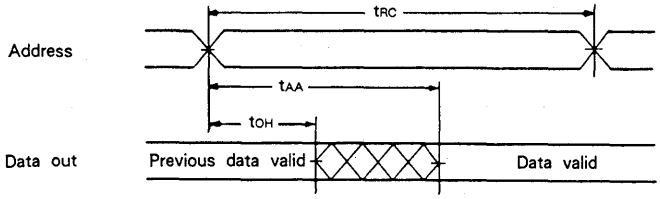
• **Write cycle**

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	0	25	ns

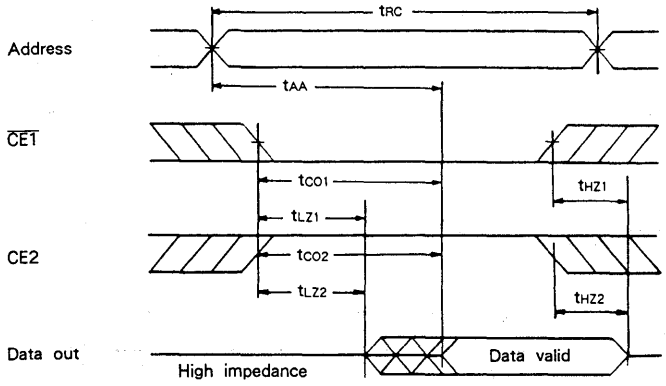
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

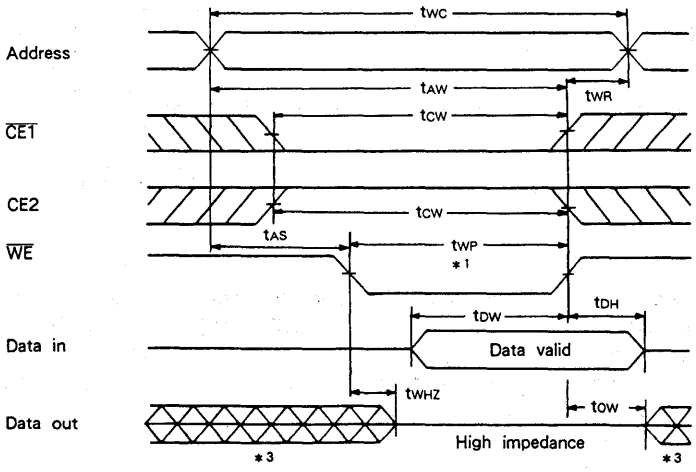
• Read cycle (1) : $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}



• Read cycle (2) : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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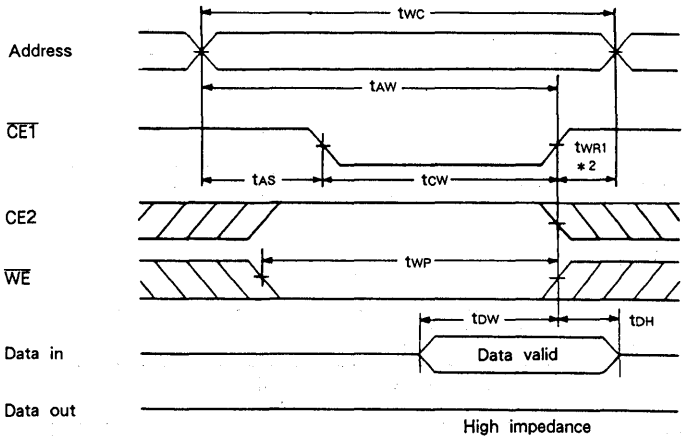
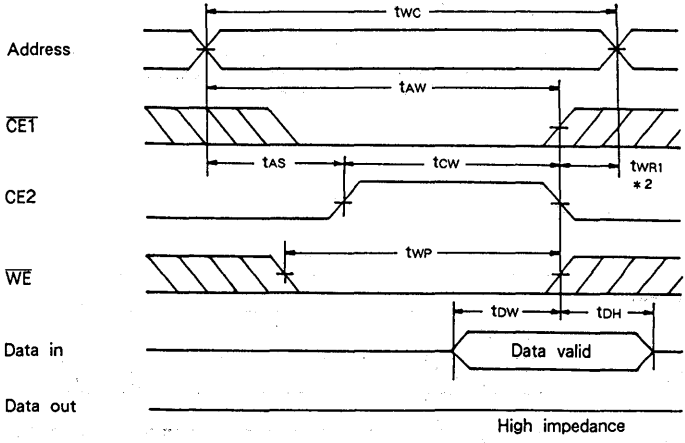
• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. A write occurs during the period of $\overline{CE1}$ and $\overline{WE}$ being low and CE2 being high.
*2. t_{WR1} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high and CE2 going low to the end of write cycle.
*3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

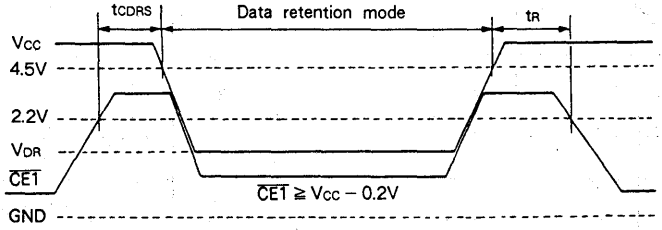
Data Retention Characteristics (Ta = 0 to 70°C)

Item	Symbol	Test conditions		−70L/85L/10L/12L			−70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc = 3.0V*1	0 to 70°C	—	—	10	—	—	3	µA
			0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	Vcc = 2.0 to 5.5V*1		—	0.5	25	—	0.2	5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

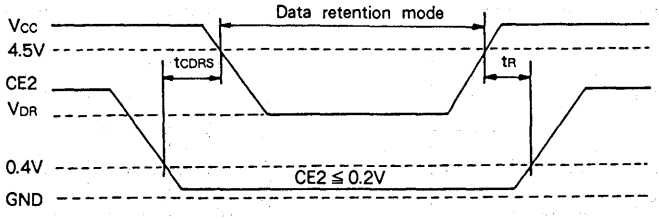
*1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)
*2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) (CE1 control)



- Low supply voltage data retention waveform (2) (CE2 control)



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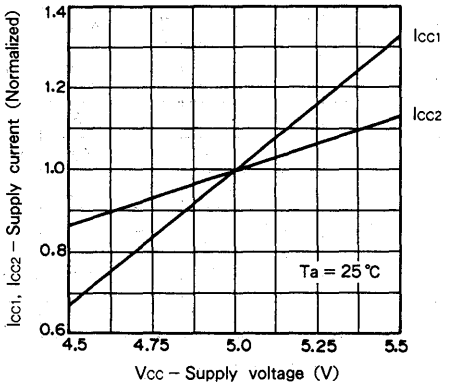
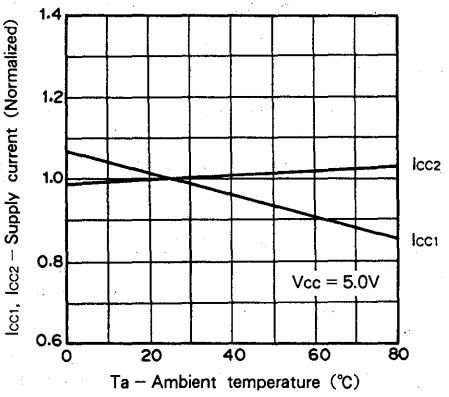
Example of Representative Characteristics

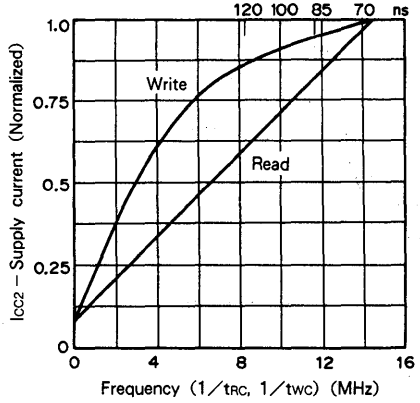
Supply current vs. Supply voltage



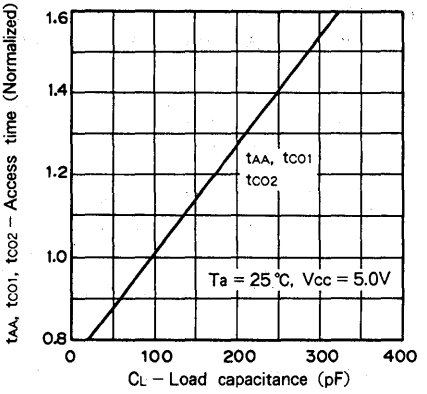
Supply current vs. Ambient temperature



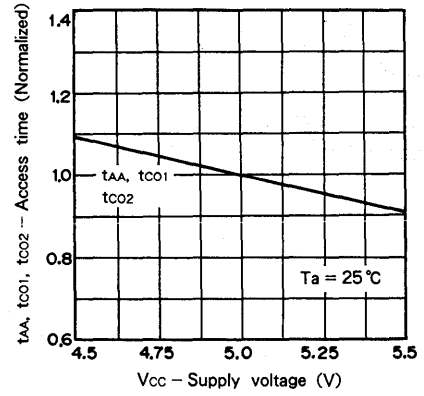
Supply current vs. Frequency



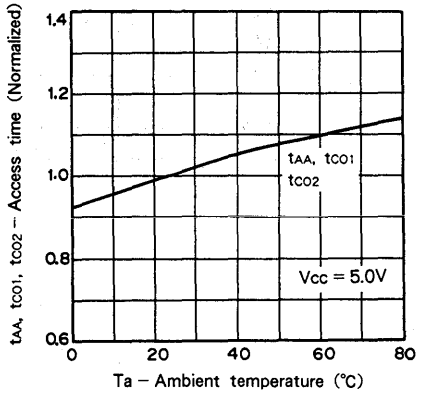
Access time vs. Load capacitance



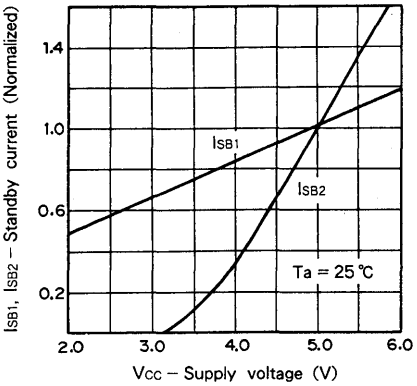
Access time vs. Supply voltage



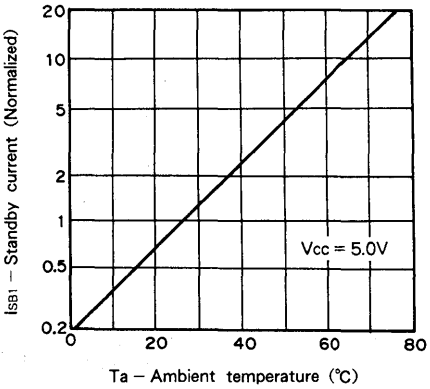
Access time vs. Ambient temperature



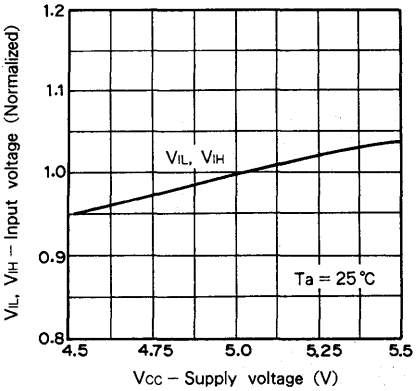
Standby current vs. Supply voltage



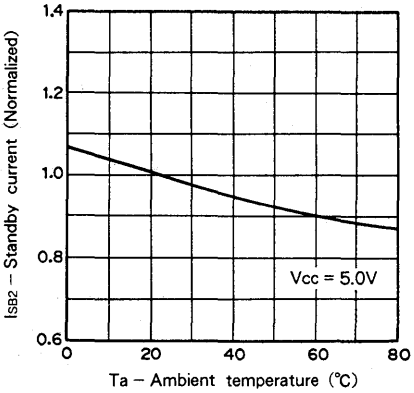
Standby current vs. Ambient temperature



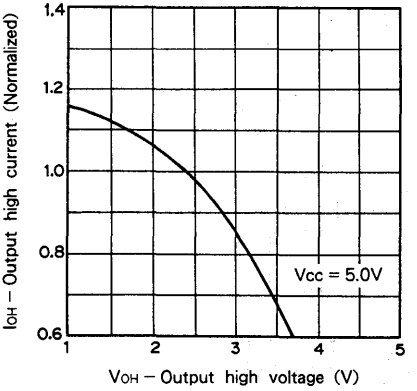
Input voltage level vs. Supply voltage



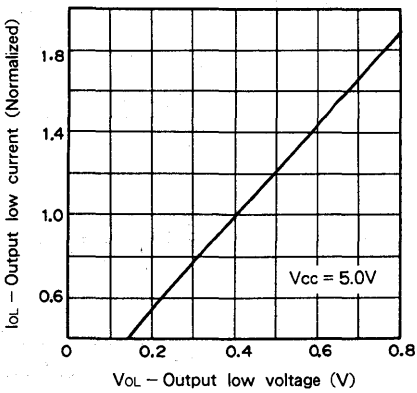
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



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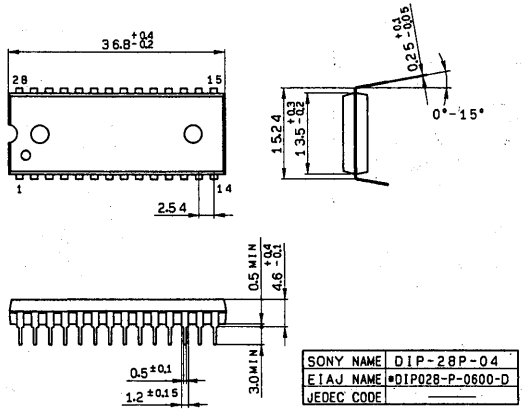
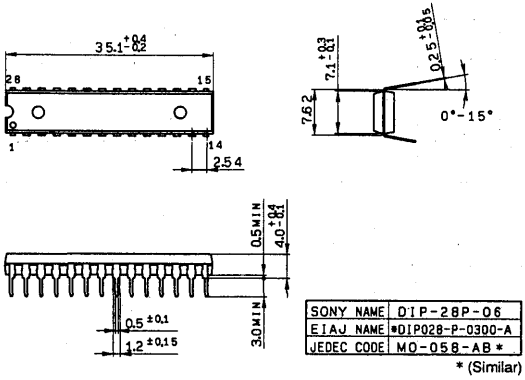
Package Outline Unit : mm

CXK58267AP 28pin DIP (Plastic) 600mil 4.2g



SONY NAME	DIP-28P-04
EIAJ NAME	*DIP028-P-0600-D
JEDEC CODE	

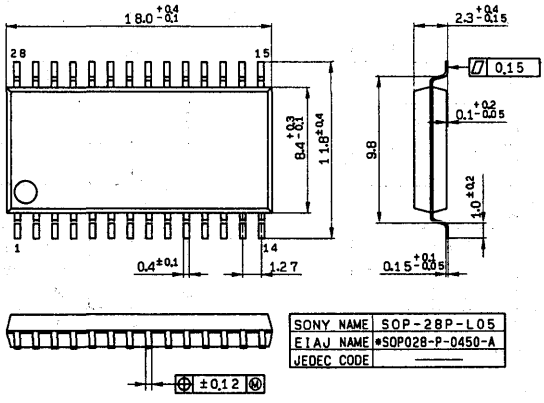
CXK58267ASP 28pin DIP (Plastic) 300mil 2.0g



SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB*

* (Similar)

CXK58267AM 28pin SOP (Plastic) 450mil 0.7g



SONY NAME	SOP-28P-L05
EIAJ NAME	*SOP028-P-0450-A
JEDEC CODE	

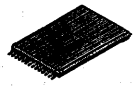
SONY CXK58267ATM/AYM -70L/85L/10L/12L -70LL/85LL/10LL/12LL

32768-word × 8-bit High Speed CMOS Static RAM

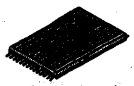
Description

CXK58267ATM/AYM is a 256K bits, 32768 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current. It has two chip enable control inputs, $\overline{CE1}$ & CE2, which allow to achieve multiple memory use with battery back-up applications.

CXK58267ATM
28 pin TSOP (Plastic)



CXK58267AYM
28 pin TSOP (Plastic)



Features

- Two Chips Enable Control Inputs
  Provide Stand-by/Data Retention Mode
  $\overline{CE1}$: Low Active
  CE2 : High Active
- Thin Small-outline Packages :
  CXK58267ATM : 8mm × 13.4mm 28 pin TSOP
  CXK58267AYM : 8mm × 13.4mm 28 pin TSOP
  (Mirror image pinout)
- Low stand-by current :
  L-Version :
  25 µA (Max.) @Vcc = 5.5V, Ta = 0 to 70℃
  LL-Version :
  5 µA (Max.) @Vcc = 5.5V, Ta = 0 to 70℃
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
  CXK58267ATM/AYM-70L, -70LL 70ns (Max.)
  CXK58267ATM/AYM-85L, -85LL 85ns (Max.)
  CXK58267ATM/AYM-10L, -10LL 100ns (Max.)
  CXK58267ATM/AYM-12L, -12LL 120ns (Max.)
- Single +5V Supply : +5V ± 10%

Function

32768-word × 8-bit static RAM

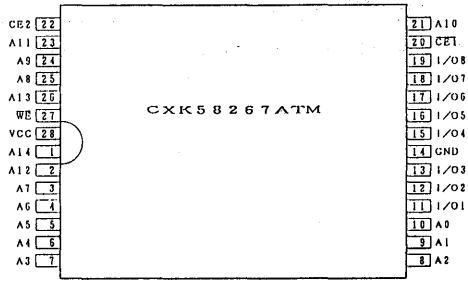
Structure

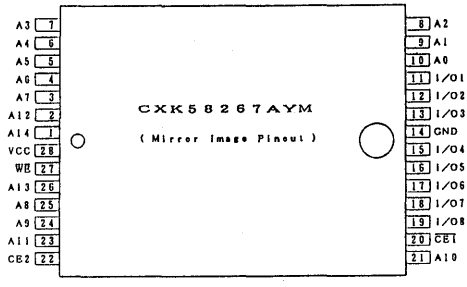
Silicon gate CMOS IC

Pin Description

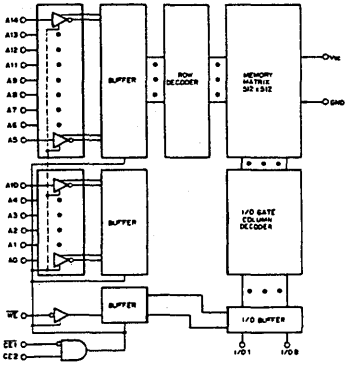
Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
Vcc	+5V power supply
GND	Ground

Pin Configuration (Top View)





Block Diagram



E90524 – ST

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	235 • 10	°C • sec

* V_{IN}, $V_{I/O}$ = −3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−0.5	—	0.5	−0.5	—	0.5	μA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to Vcc		−0.5	—	0.5	−0.5	—	0.5	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, I_{OUT} = 0mA		—	3	10	—	3	10	mA
		$\overline{CE1}$ = 0.2V, CE2 = Vcc − 0.2V, V_{IN} = 0.2V or Vcc − 0.2V		—	1	5	—	1	5	
Average operating current	I_{CC2}	Min. cycle, Duty = 100%, I_{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I_{SB1}	CE2 ≦ 0.2V or ($\overline{CE1}$ ≧ Vcc − 0.2V, CE2 ≧ Vcc − 0.2V)	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I_{SB2}	CE2 = V_{IL}, or $\overline{CE1}$ = V_{IH}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = −1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

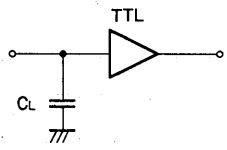
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions (Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.8V
Input rise time		tr = 5ns
Input fall time		tf = 5ns
Input and output reference level		1.5V
Output load conditions	85L / 85LL / 10L / 10LL / 12L / 12LL	C_L* = 100pF, 1TTL
	70L/70LL	C_L* = 30pF, 1TTL



* C_L includes scope and jig capacitances.

• **Read cycle**

Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time ($\overline{CE1}$, CE2)	t_{CO1}, t_{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t_{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• **Write cycle**

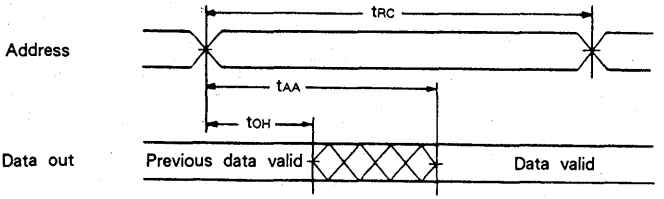
Item	Symbol	−70L/70LL		−85L/85LL		−10L/10LL		−12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	0	25	0	25	0	25	0	25	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

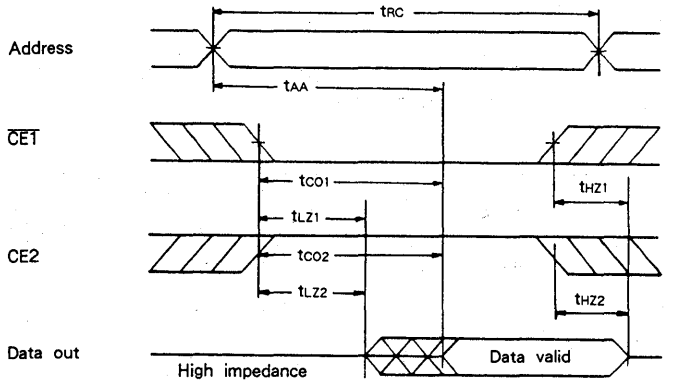
3

Timing Waveform

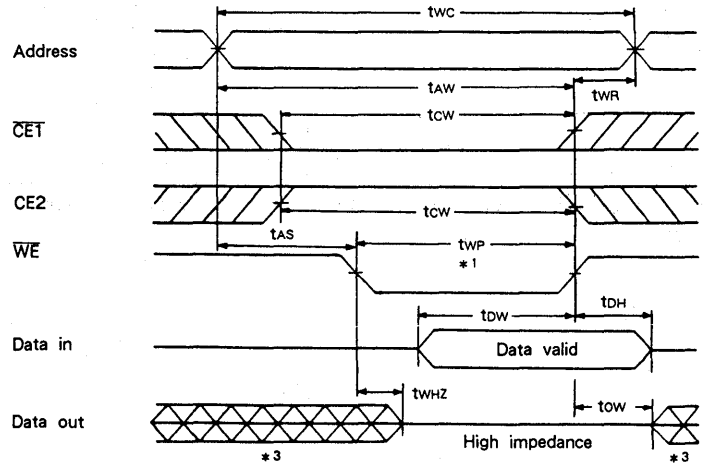
• Read cycle (1) : $\overline{CE1} = V_{IL}$, CE2 = V_{IH}, $\overline{WE} = V_{IH}$



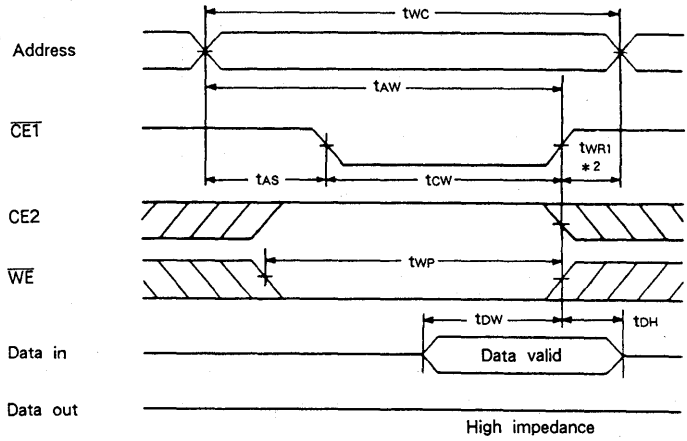
• Read cycle (2) : $\overline{WE} = V_{IH}$



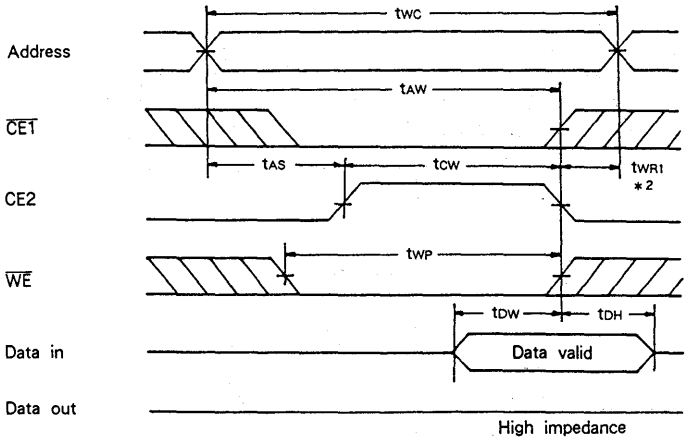
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. A write occurs during the period of $\overline{CE1}$ and $\overline{WE}$ being low and CE2 being high.
*2. t_{WR1} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high and CE2 going low to the end of write cycle.
*3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

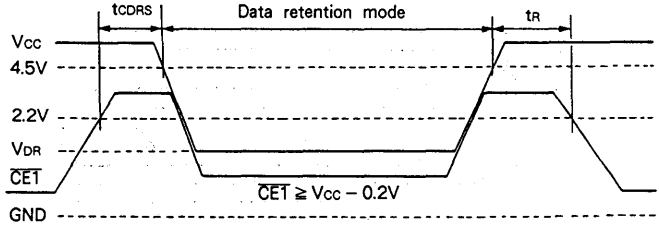
Data Retention Characteristics (Ta = 0 to 70°C)

Item	Symbol	Test conditions		−70L/85L/10L/12L			−70LL/85LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc = 3.0V*1	0 to 70°C	—	—	10	—	—	3	µA
			0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	Vcc = 2.0 to 5.5V*1		—	0.5	25	—	0.2	5	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

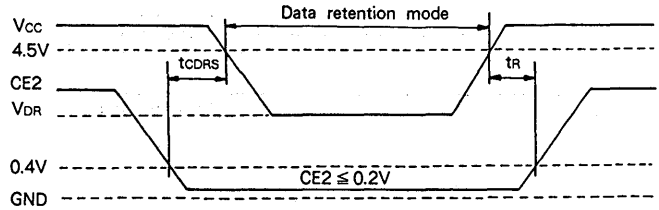
*1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)
*2. t_{RC} : Read cycle time

Data retention waveform

• Low supply voltage data retention waveform (1) (CE1 control)

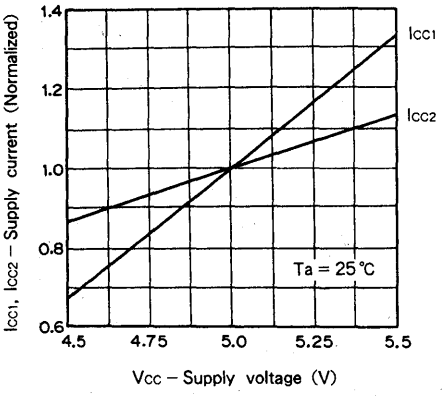


• Low supply voltage data retention waveform (2) (CE2 control)

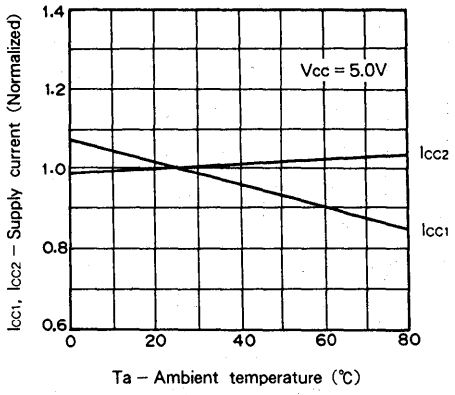


Example of Representative Characteristics

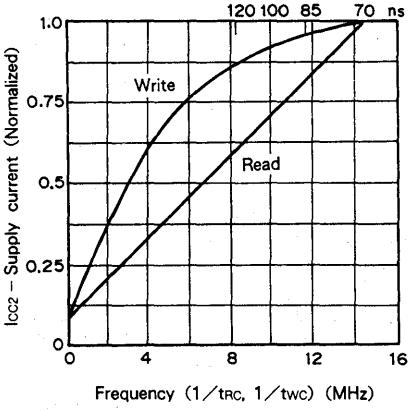
Supply current vs. Supply voltage



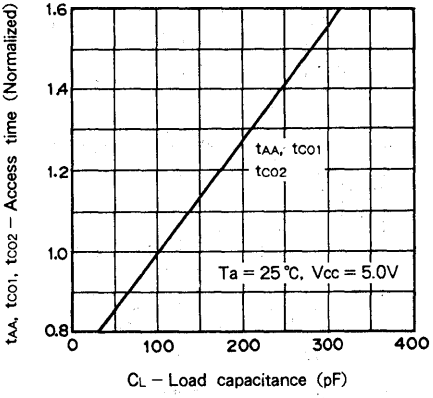
Supply current vs. Ambient temperature



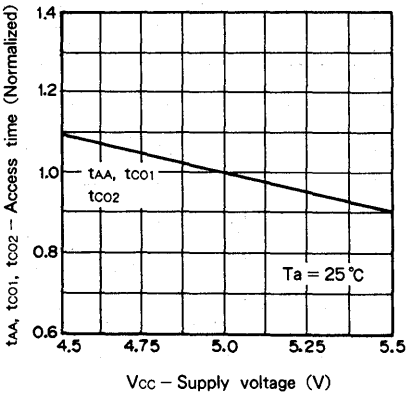
Supply current vs. Frequency



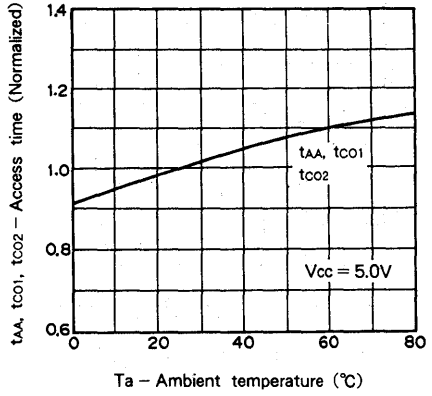
Access time vs. Load capacitance



Access time vs. Supply voltage



Access time vs. Ambient temperature



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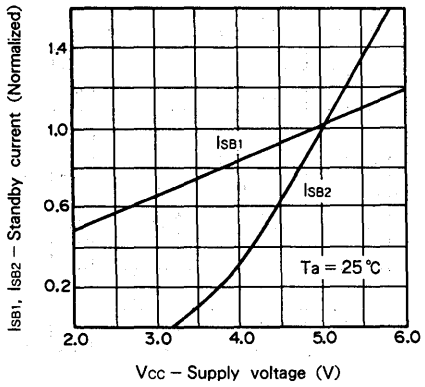
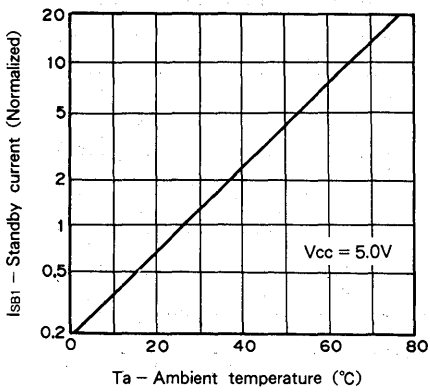
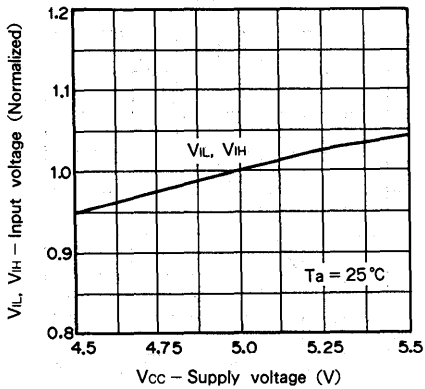
Standby current vs. Supply voltage



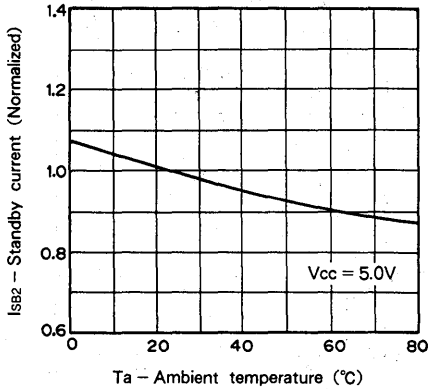
Standby current vs. Ambient temperature



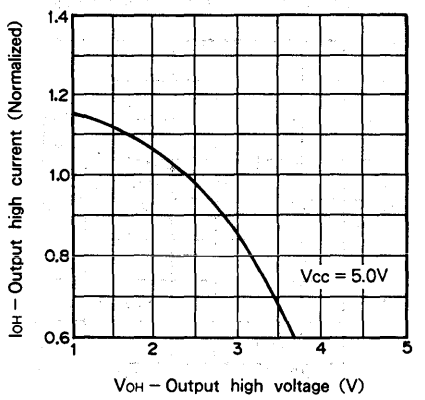
Input voltage level vs. Supply voltage



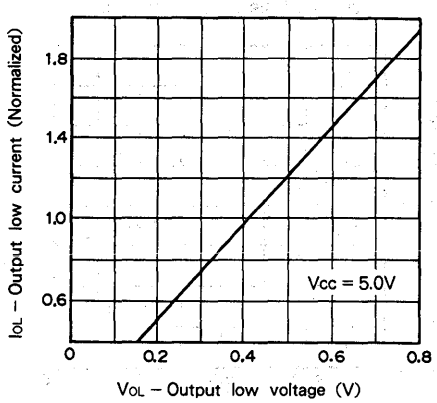
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

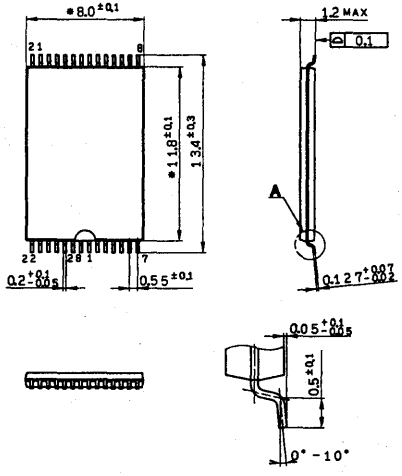


Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58267ATM 28pin TSOP (Plastic)

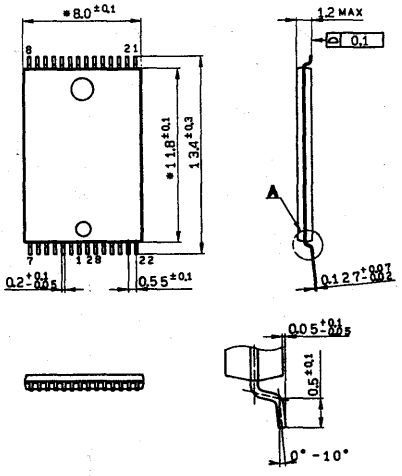


Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	———

CXK58267AYM 28pin TSOP (Plastic)



Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	———

32768-word × 9-bit High Speed CMOS Static RAM

Description

The CXK59288P/J is a high speed CMOS static RAM which consists of 32768-word × 9-bit. It operates at 15ns/20ns/25ns access time from 5V single power supply.

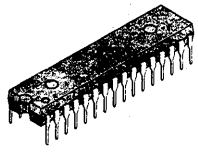
Features

- High speed, low power consumption :

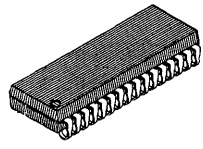
	Access time (Max.)	Power consumption (Typ., Cycle=Min.)
CXK59288P/J-15	15ns	500mW
CXK59288P/J-20	20ns	425mW
CXK59288P/J-25	25ns	375mW

- Single +5V power supply :
  −15 5V ± 5%
  −20/25 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Available in 32 pin 300mil DIP, 300mil SOJ package.

CXK59288P
32 pin DIP (Plastic)



CXK59288J
32 pin SOJ (Plastic)



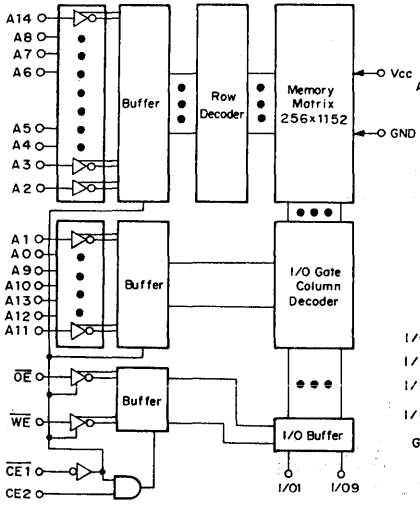
Function

32768-word × 9-bit static RAM

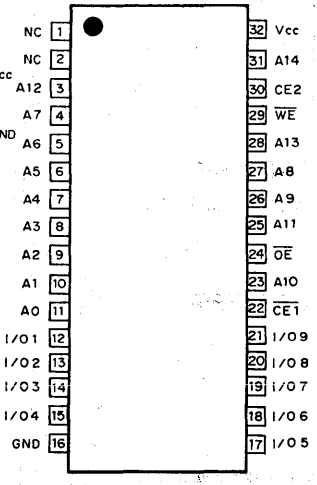
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5* to +7.0	V
Input voltage	V_{IN}	−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* V_{CC}, V_{IN}, $V_{I/O}$ = −3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	V_{CC} Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	L	×	×	Not selected	High Z	I_{CC1}, I_{CC2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	−15	V_{CC}	4.75	5.0	5.25	V
	−20/25		4.5	5.0	5.5	
Input high voltage		V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage		V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 20ns.

3

Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%*, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.**	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to Vcc, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	—	—	
Average operating current	I_{CC2}	Cycle = Min., Duty = 100%, I_{OUT} = 0mA	−15	—	100	130	mA
			−20	—	85	120	
			−25	—	75	120	
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc − 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V		—	—	1	mA
	I_{SB2}	$\overline{CE1}$ = V_{IH}, V_{IN} = V_{IH}/V_{IL}, Cycle = Min.		—	15	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

* Vcc = 5V ± 5% for CXK59288P/J-15
** Vcc = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

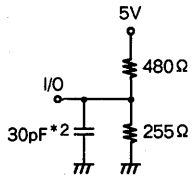
AC characteristics

• AC test conditions

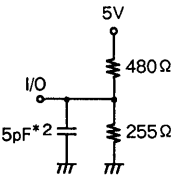
(Vcc = 5V ± 10%*1, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*3



*1 Vcc = 5V ± 5% for CXK59288P/J-15
*2 including scope and jig capacitance
*3 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	−15		−20		−25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	15	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	20	—	25	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	15	—	20	—	25	ns
Chip enable access time (CE2)	t_{CO2}	—	8	—	10	—	12	ns
Output enable to output valid	t_{OE}	—	8	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}*, t_{LZ2}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	—	8	—	9	—	10	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	7	—	8	—	9	ns
Chip enable to power up time ($\overline{CE1}$)	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$)	t_{PD}	—	15	—	20	—	25	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

• **Write cycle**

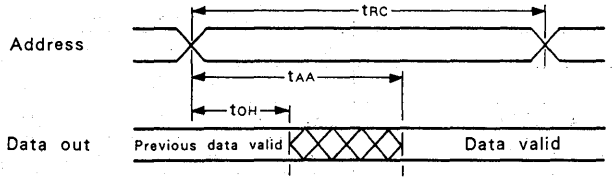
Item	Symbol	−15		−20		−25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	15	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	10	—	13	—	15	—	ns
Chip enable to end of write	t_{CW}	11	—	14	—	16	—	ns
Data to write time overlap	t_{DW}	8	—	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	10	—	13	—	15	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	3	—	3	—	3	—	ns
Write to output in high Z	t_{WHZ}*	0	8	0	9	0	10	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

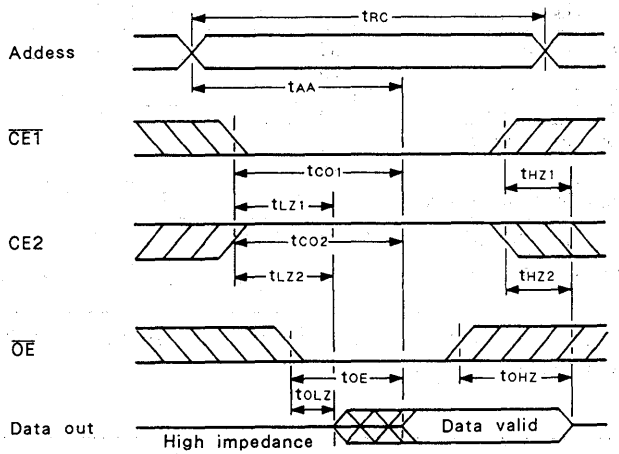
3

Timing Waveform

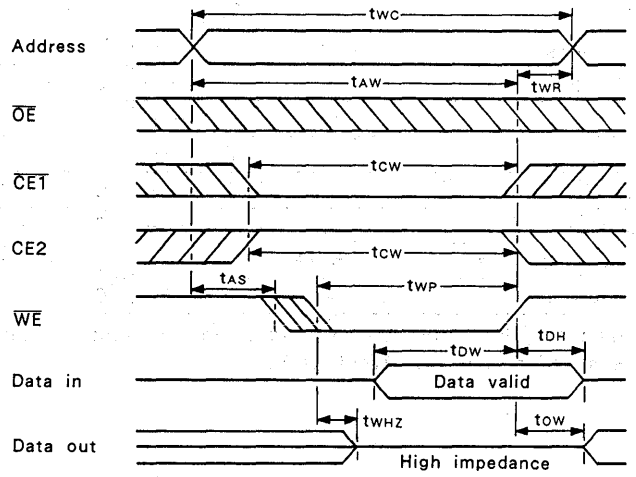
• Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



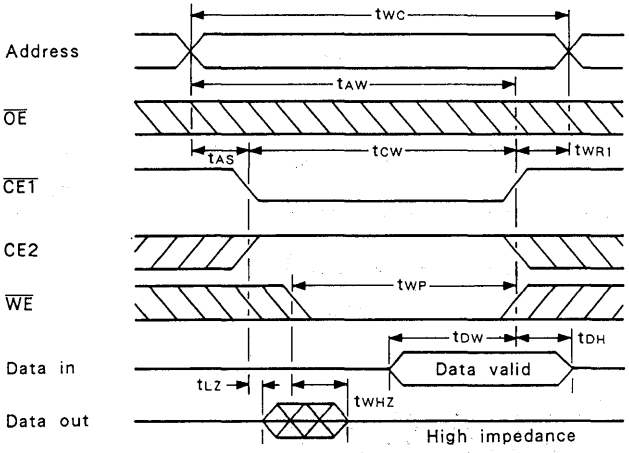
• Read cycle (2) : $\overline{WE} = V_{IH}$



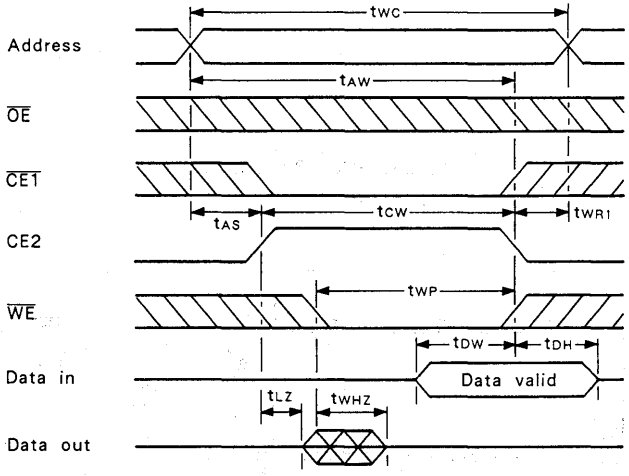
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



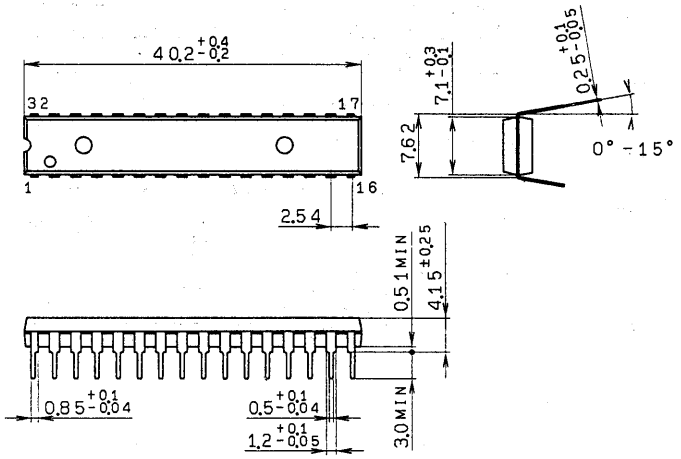
• Write cycle (3) : CE2 control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

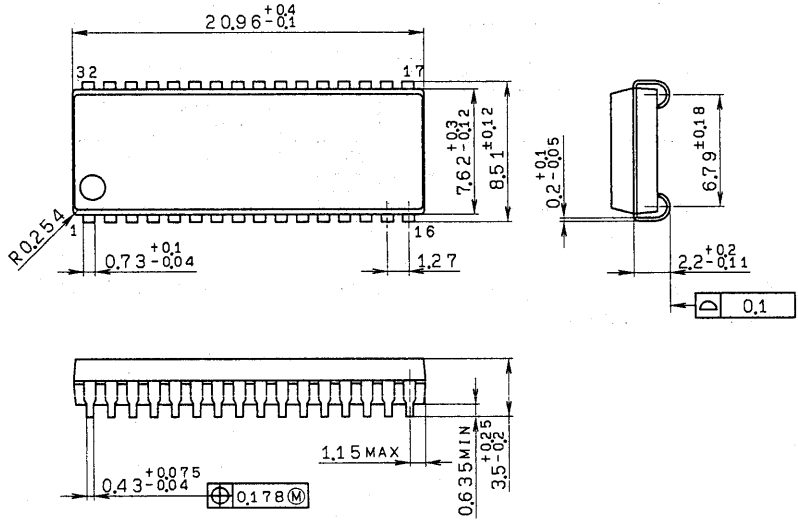
Package Outline Unit : mm

CXK59288P 32 pin DIP (Plastic) 300mil
Preliminary



DIP-32P-03

CXK59288J 32 pin SOJ (Plastic) 300mil
Preliminary



SOJ-32P-02

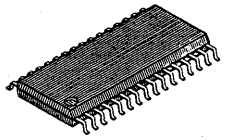
SONY CXK59290M/TM -70L/10L/12L

32768-word × 9-bit High Speed CMOS Static RAM

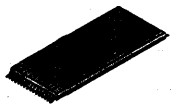
Description

The CXK59290M/TM is a 294912 bits high speed CMOS static RAM organized as 32768 words by 9 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

CXK59290M
32 pin SOP (Plastic)



CXK59290TM
32 pin TSOP (Plastic)



Features

- Fast access time: (Access time)
  CXK59290M/TM-70L 70ns (Max.)
  CXK59290M/TM-10L 100ns (Max.)
  CXK59290M/TM-12L 120ns (Max.)
- Low power operation: Standby/Operation
  CXK59290M/TM-70L, 10L, 12L:
  2.5μW (Typ.)/15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 32 pin 450mil SOP and
  32 pin 8mm × 20mm TSOP (EIAJ Standard)

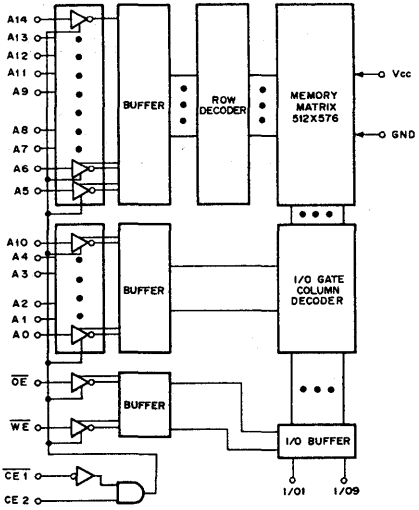
Function

32768-word × 9-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

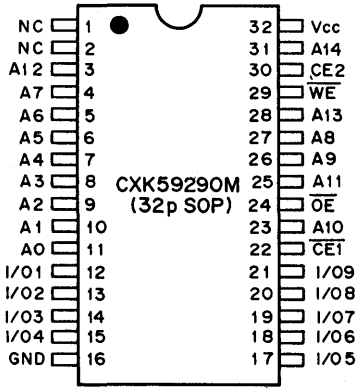


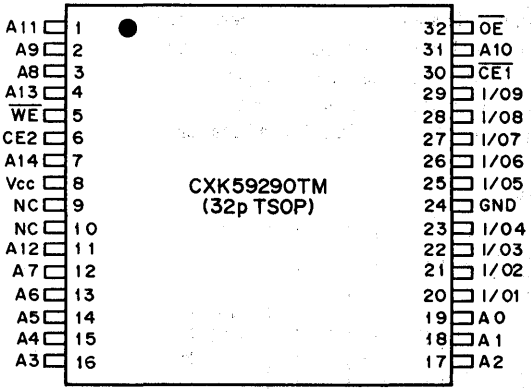
Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration

(Top View)





Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		–0.5 to +7.0	V
Input voltage	V_{IN}		–0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		–0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D		0.7	W
Operating temperature	Topr		0 to +70	℃
Storage temperature	Tstg		–55 to +150	℃
Soldering temperature	Tsolder	M	260 • 10	℃ • sec
		TM	235 • 10	

* V_{IN}, $V_{I/O}$=–3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	——	Vcc+0.3	V
Input low voltage	V_{IL}	–0.3 *	——	0.8	V

* V_{IL}=–3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC and operating characteristics (Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to Vcc		–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, I_{OUT}=0mA V_{IN}=V_{IH} or V_{IL}		—	3	10	mA
		$\overline{CE1}$ ≦ 0.2V, CE2 ≧ Vcc–0.2V V_{IN} ≦ 0.2V or ≧ Vcc–0.2V		—	1	5	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	70L	—	—	60	mA
			10L	—	—	60	
			12L	—	—	60	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc–0.2V CE2 ≧ Vcc–0.2V	0 to +70°C	—	—	25	µA
			0 to +40°C	—	—	5	
			25°C	—	0.5	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.4	2	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance (Ta=25°C, f=1MHz)

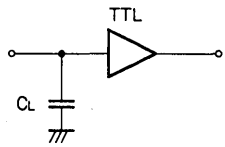
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (Vcc=5V ± 10%, Ta=0 to +70°C)

Item		Conditions
Input pulse high level		V_{IH}=2.2V
Input pulse low level		V_{IL}=0.8V
Input rise time		tr=5ns
Input fall time		tf=5ns
Input and output reference level		1.5V
Output load conditions	10L/12L	C_L*=100pF, 1TTL
	70L	C_L*=30pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	100	—	120	—	ns
Address access time	t_{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	70	—	100	—	120	ns
Chip enable access time (CE2)	t_{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t_{OE}	—	35	—	50	—	60	ns
Output hold from address change	t_{OH}	5	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2} *	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

• Write cycle

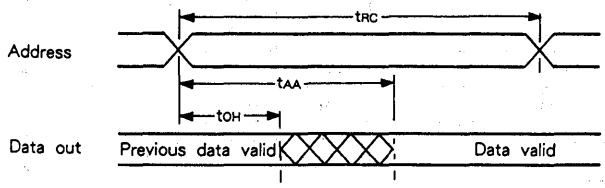
Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t_{AW}	65	—	80	—	100	—	ns
Chip enable to end of write	t_{CW}	65	—	80	—	100	—	ns
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	60	—	70	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ} *	0	25	0	25	0	25	ns

* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

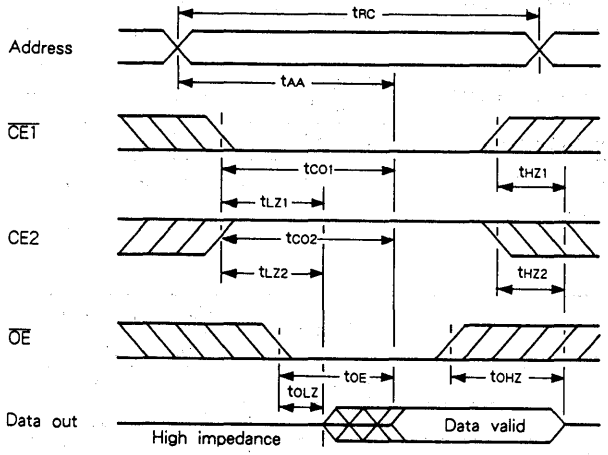
3

Timing Waveform

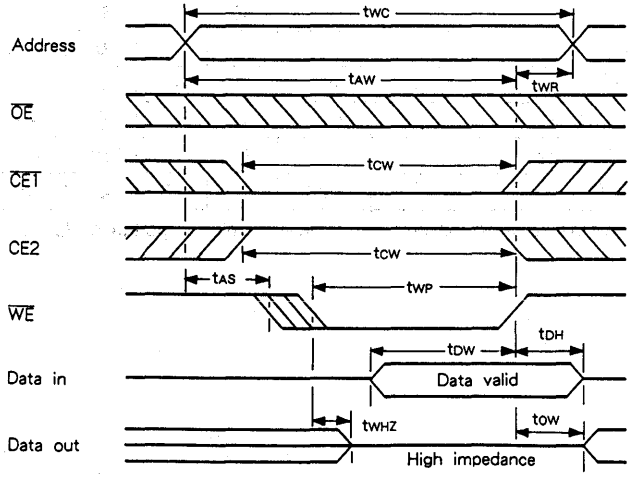
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



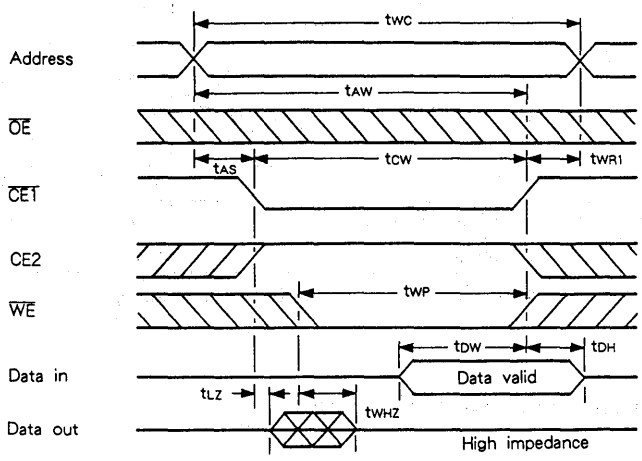
• Read cycle (2) : $\overline{WE}$=V_{IH}



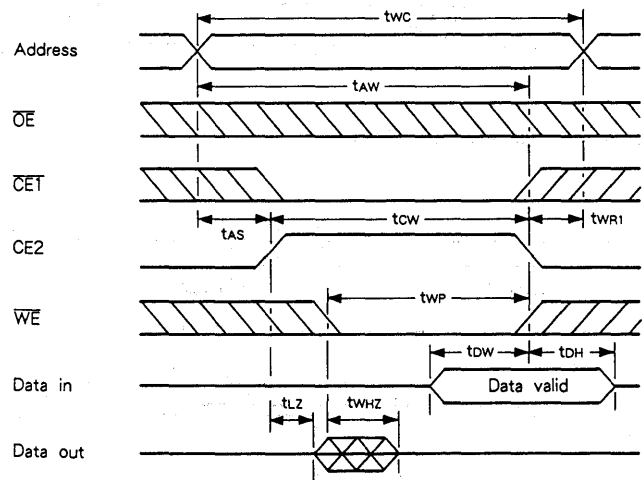
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

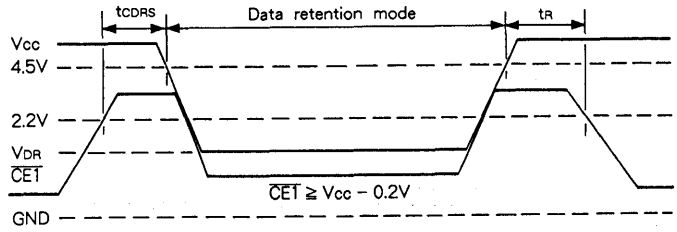
Data Retention Characteristics

(Ta=0 to +70 °C)

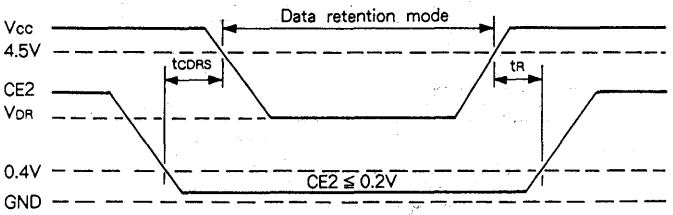
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V*1	0 to +70 °C	—	—	10	μA
			0 to +40 °C	—	—	2	
			25 °C	—	0.25	1	
	I_{CCDR2}	Vcc=2.0 to 5.5V*1		—	0.5*3	25	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention		0	—	—	ns
Recovery time	t_R	mode		t_{RC}*2	—	—	ns

*1. $\overline{CE1} \geqq$ Vcc–0.2V, CE2 ≧ Vcc–0.2V ($\overline{CE1}$ control) or CE2 ≦ 0.2V (CE2 control)
*2. t_{RC} : Read cycle time
*3. Vcc=5V, Ta=25 °C

• Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

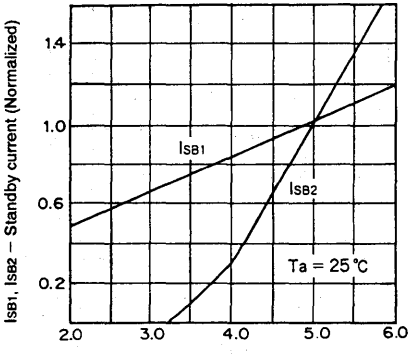


• Low supply voltage data retention waveform (2) : CE2 control

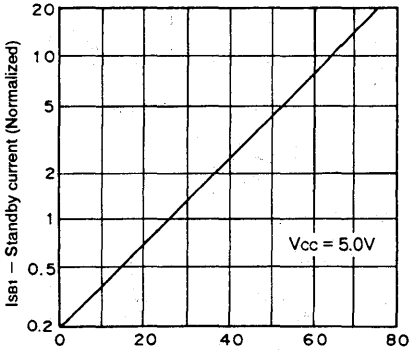


Example of Representative Characteristics

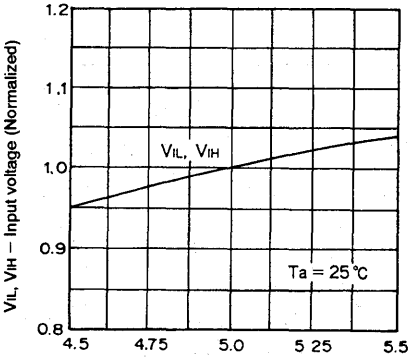
Standby current vs. Supply voltage



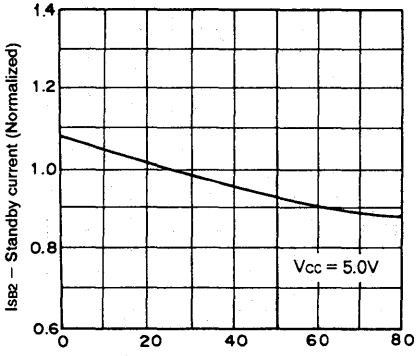
Standby current vs. Ambient temperature



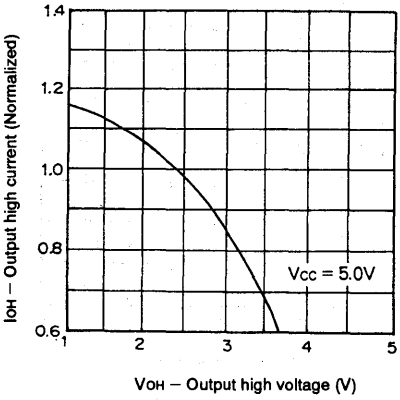
Input voltage level vs. Supply voltage



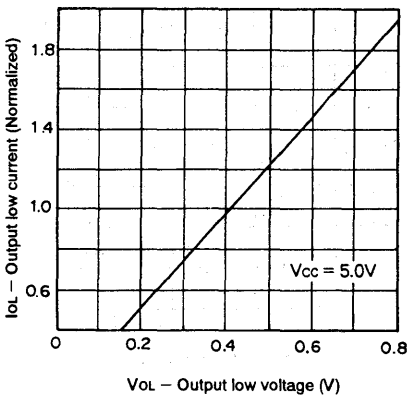
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

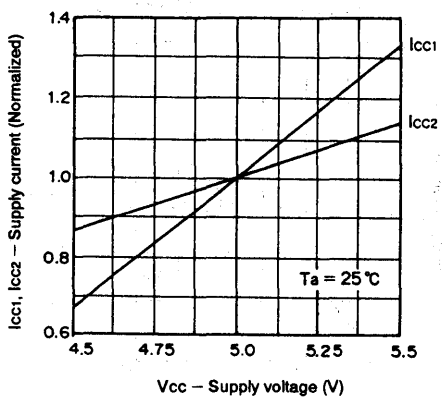


Output low current vs. Output low voltage

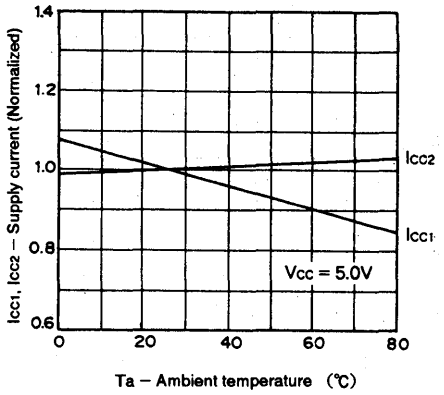


3

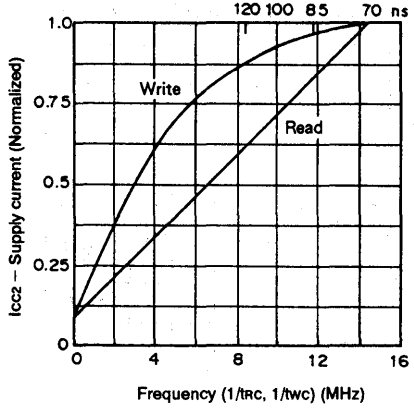
Supply current vs. Supply voltage



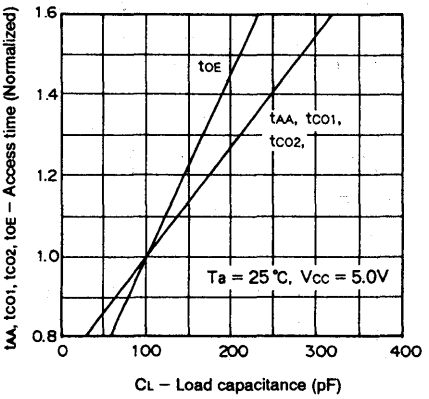
Supply current vs. Ambient temperature



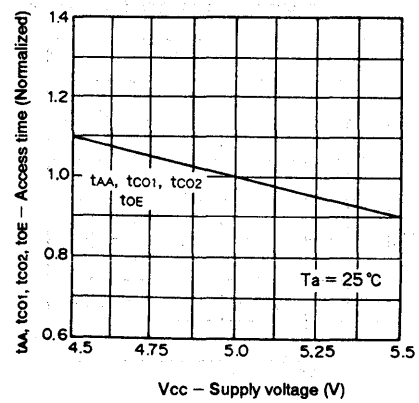
Supply current vs. Frequency



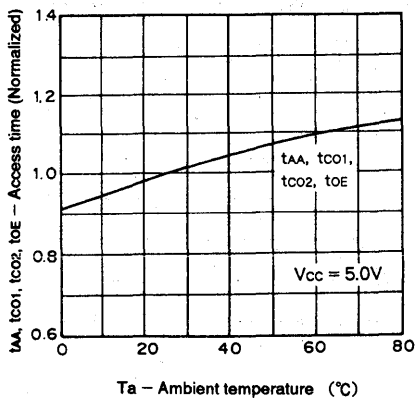
Access time vs. Load capacitance



Access time vs. Supply voltage



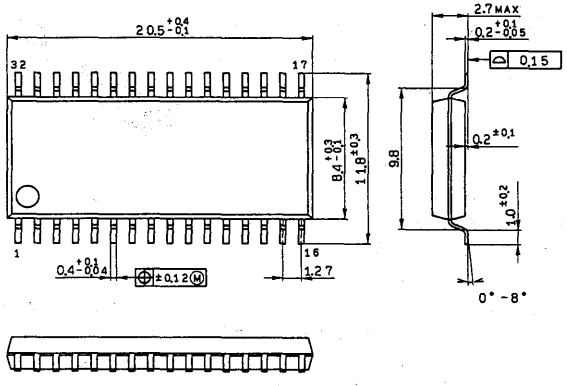
Access time vs. Ambient temperature



Package Outline Unit : mm

CXK59290M

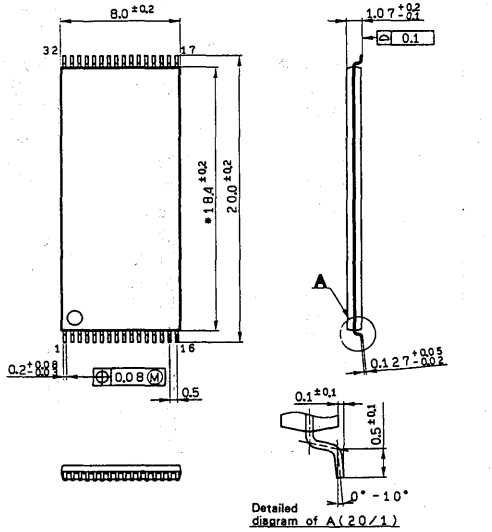
32pin SOP (Plastic) 450mil



SONY NAME	SOP-32P-L03
EIAJ NAME	*SOP032-P-0450-B
JEDEC CODE	

CXK59290TM

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

SONY CXK581020SP/J -35/45/55

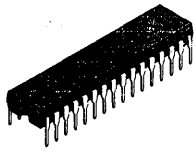
131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581020SP/J are 131,072-word × 8-bit high speed CMOS static RAMs suitable for use in high speed and low power applications.

Organized as 131,072 words by 8 bits, it operates from a single 5V supply.

CXK581020SP
32 pin DIP (Plastic)



CXK581020J
32 pin SOJ (Plastic)

Features

- Fast access time : (Access time)
  CXK581020SP/J-35 35ns (Max.)
  CXK581020SP/J-45 45ns (Max.)
  CXK581020SP/J-55 55ns (Max.)
- Low power operation : (Operation)
  CXK581020SP/J-35, 45, 55
  300mW (Typ, Cycle = Min.)
- Single +5V supply : +5V ± 10%
- Fully static memory ··· No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 32 pin 400-mil DIP and 400-mil SOJ

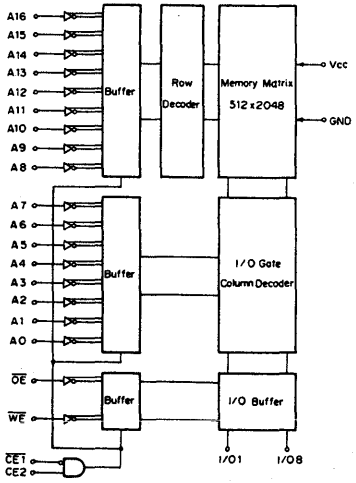
Function

131,072-word × 8-bit static RAM

Structure

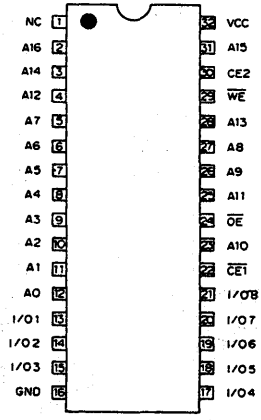
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

E89612A99 – ST

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature • time	Tsolder	260 • 10	℃ • sec

* **Note)** V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC2}
L	H	L	H	Read	Data out	I_{CC2}
L	H	X	L	Write	Data in	I_{CC2}

Note) X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

* **Note)** V_{IL} = − 3.0V Min. for pulse width less than 20ns.

3

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−2	—	2	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	−2	—	2	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	—	—	—	mA
Average operating current	I_{CC2}	Cycle = Min., Duty = 100%, I_{OUT} = 0mA	—	60	120	mA
Standby current	I_{SB1}	$\overline{CE1} \geqq V_{CC} - 0.2V$ or CE2 ≦ 0.2V, $V_{IN} \geqq V_{CC} - 0.2V$ or $V_{IN} \leqq 0.2V$	—	0.01	2	mA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, Cycle = Min.	—	5	35	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* **Note**) V_{CC} = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	7	pF

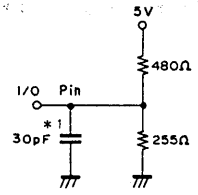
Note) This parameter is sampled and is not 100% tested.

AC characteristics

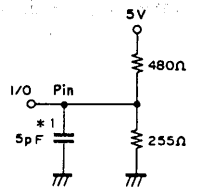
• **AC test conditions** (V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



*1. C_L includes scope and jig capacitances.
*2. For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	35	—	45	—	55	—	ns
Address access time	t_{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	35	—	45	—	55	ns
Chip enable access time (CE2)	t_{CO2}	—	35	—	45	—	55	ns
Output enable to output valid	t_{OE}	—	20	—	25	—	30	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}*, t_{LZ2}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	0	15	0	20	0	25	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	15	0	20	0	25	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	0	—	ns
Chip enable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	35	—	45	—	55	ns

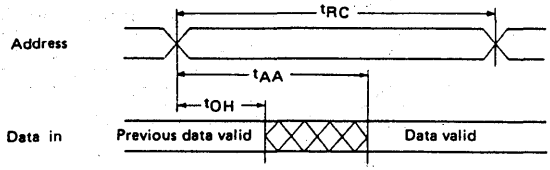
• **Write cycle**

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t_{AW}	30	—	40	—	45	—	ns
Chip enable to end of write	t_{CW}	30	—	40	—	45	—	ns
Data to write time overlap	t_{DW}	18	—	20	—	25	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	30	—	35	—	40	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$, $\overline{CE1}$)	t_{WR1}	3	—	3	—	3	—	ns
Write recovery time (CE2)	t_{WR2}	5	—	5	—	5	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	15	0	15	0	15	ns

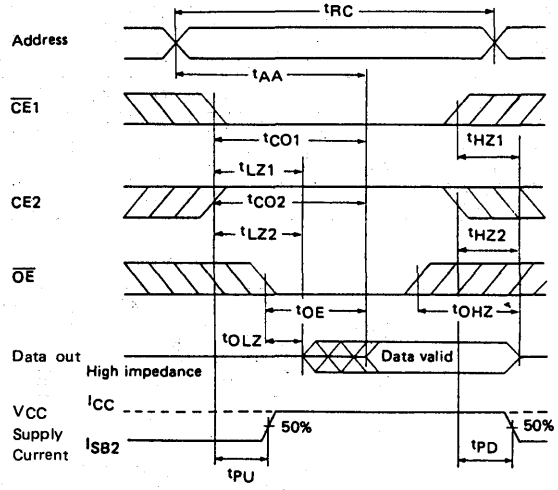
* Transition is measured ±500mV from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and not 100% tested.

Timing Waveform

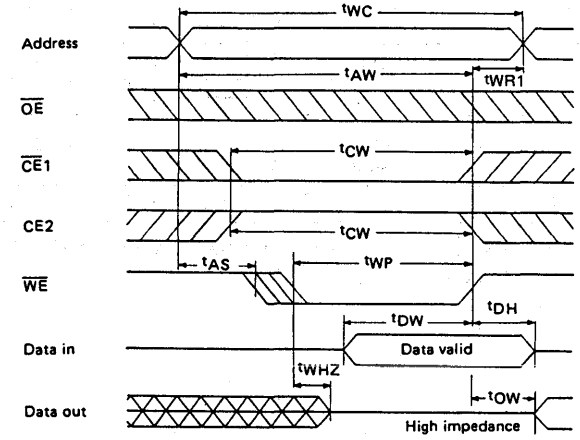
• Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, CE2 = V_{IH}, $\overline{WE} = V_{IH}$



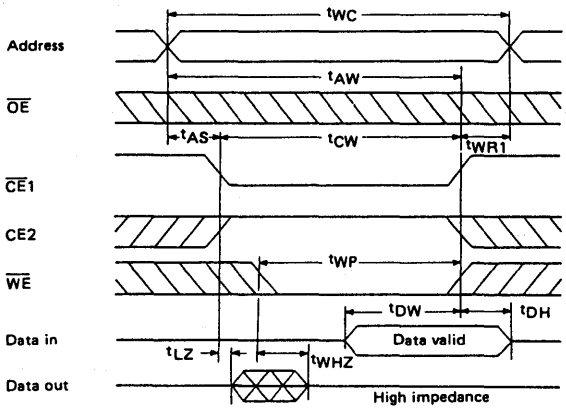
• Read cycle (2) : $\overline{WE} = V_{IH}$



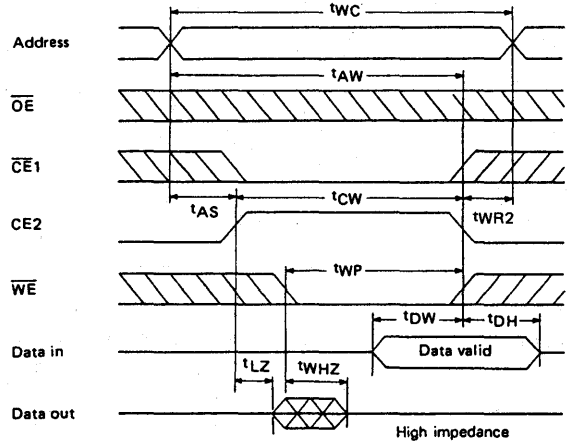
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



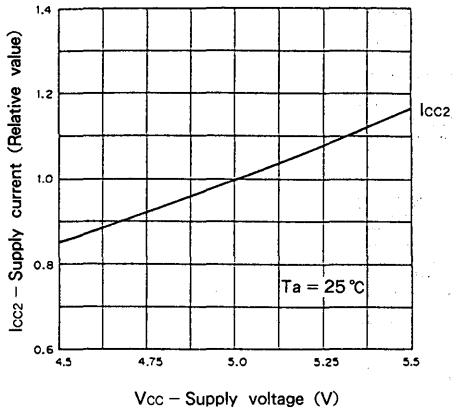
• Write cycle (3) : CE2 control



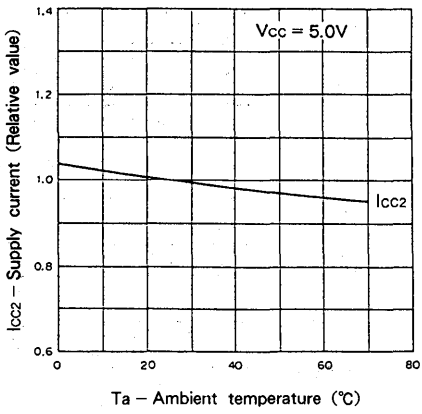
Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

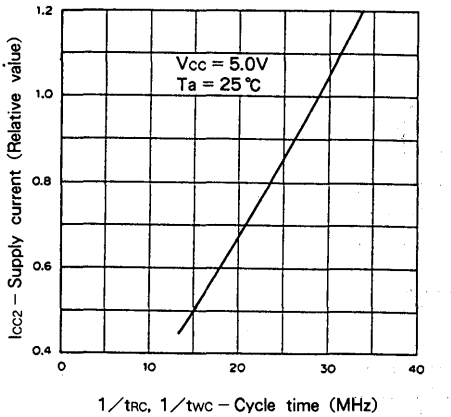
Supply current vs. Supply voltage



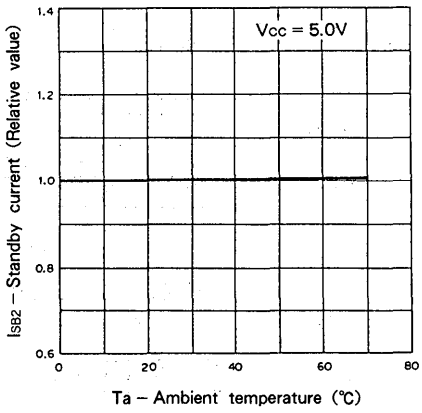
Supply current vs. Ambient temperature



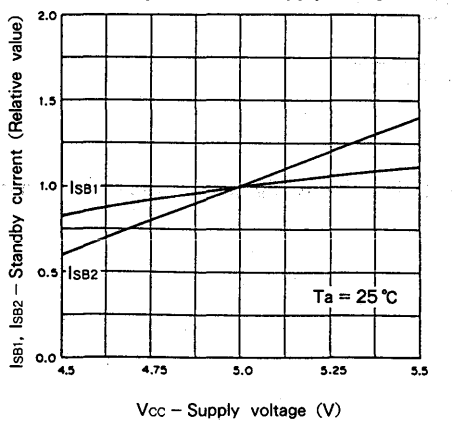
Supply current vs. Cycle time



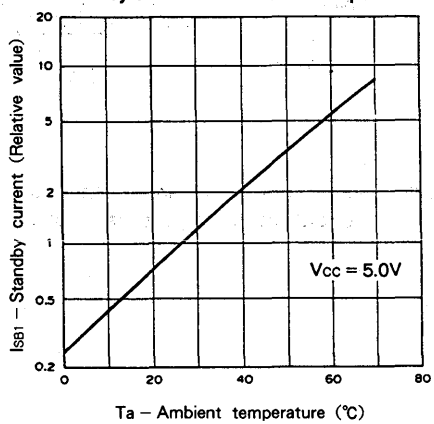
Standby current vs. Ambient temperature



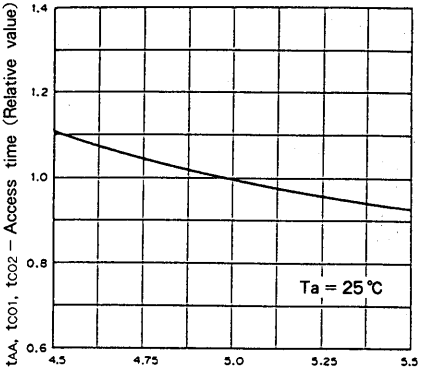
Standby current vs. Supply voltage



Standby current vs. Ambient temperature

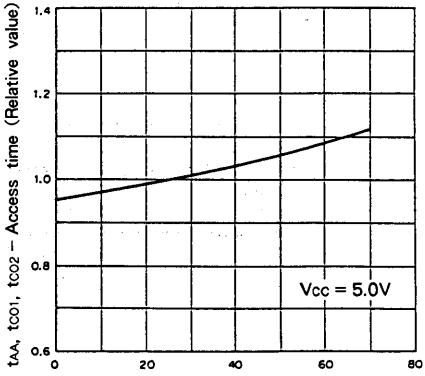


Access time vs. Supply voltage



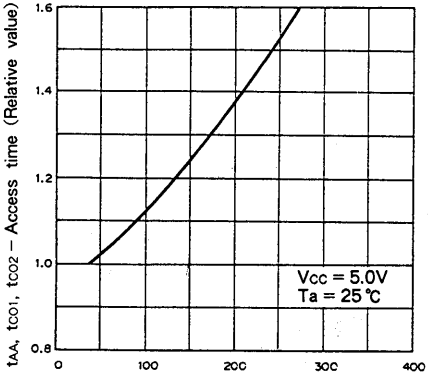
V_{CC} – Supply voltage (V)

Access time vs. Ambient temperature



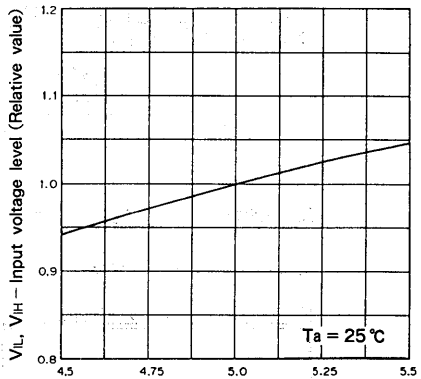
Ta – Ambient temperature (°C)

Access time vs. Load capacitance



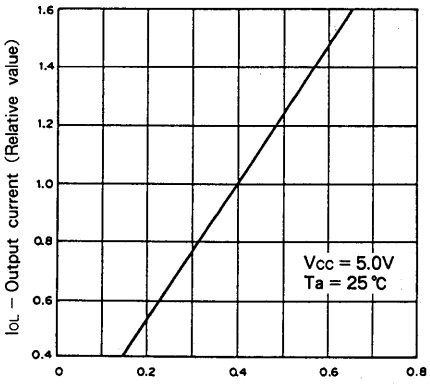
C_L – Load capacitance (pF)

Input voltage level vs. Supply voltage



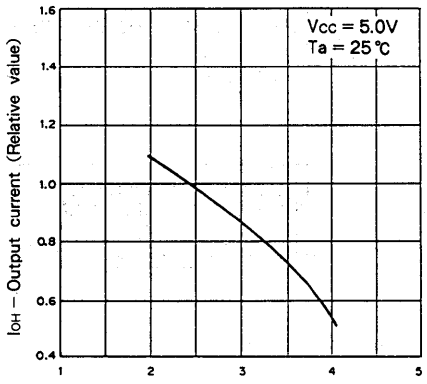
V_{CC} – Supply voltage (V)

Output current vs. Output voltage



V_{OL} – Output voltage (V)

Output current vs. Output voltage

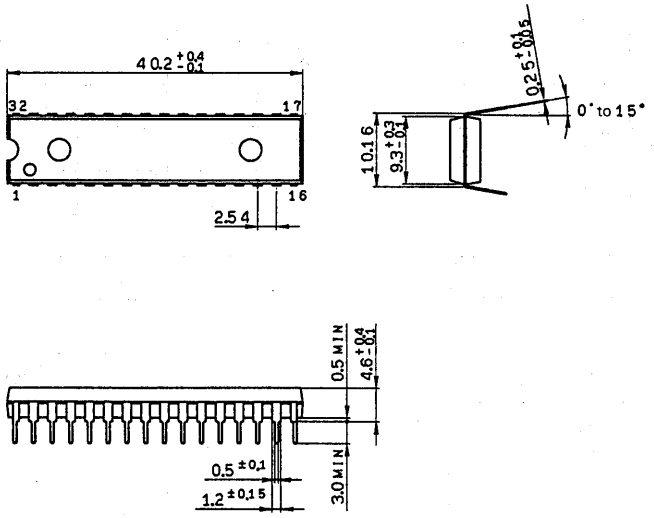


V_{OH} – Output voltage (V)

3

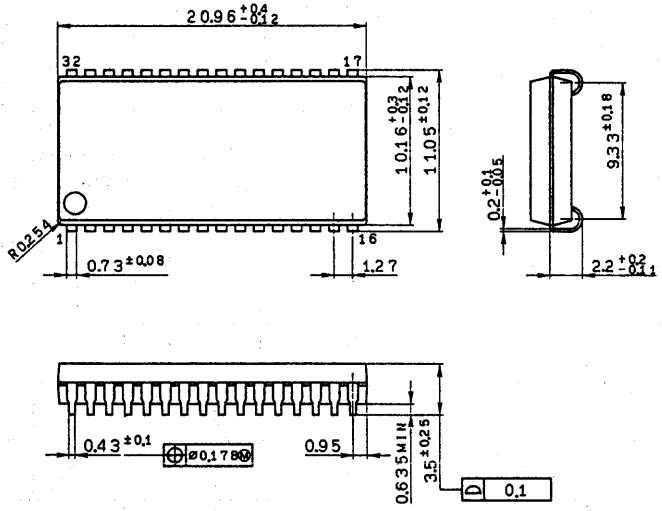
Package Outline Unit : mm

CXK581020SP 32 pin DIP (Plastic) 400mil 3.2g



DIP-32P-02

CXK581020J 32 pin SOJ (Plastic) 400mil 1.3g



SOJ-32P-01

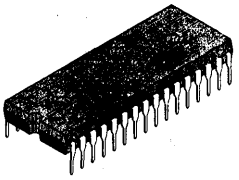
SONY CXK581001P/M -70L/85L 70LL/85LL

131,072-word × 8-bit High Speed CMOS Static RAM

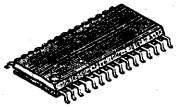
Description

CXK581001P/M is a 1,048,576 bits high speed CMOS static RAMs organized as 131,072 words by 8-bit and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

CXK581001P
32 pin DIP (Plastic)



CXK581001M
32 pin SOP (Plastic)



Features

- Fast access time: (Access time)
  CXK581001P/M-70L/70LL 70ns (Max.)
  CXK581001P/M-85L/85LL 85ns (Max.)
- Low power operation :
  CXK581001P/M Standby/Operation
  –70L/85L : 10 µW (Typ.)/237.5mW (Typ., Cycle=Min.)
  –70LL/85LL : 3.5 µW (Typ.)/237.5mW (Typ., Cycle=Min.)
- Single + 5V supply : +5V ± 10%
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581001P 600mil 32 pin DIP package
- CXK581001M 525mil 32 pin SOP package

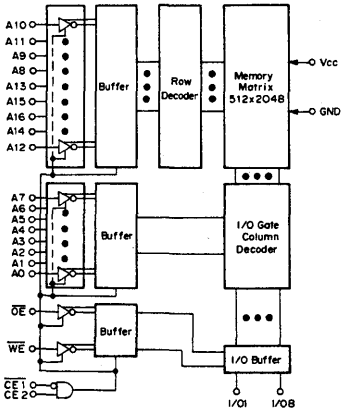
Function

131,072-word × 8-bit static RAM

Structure

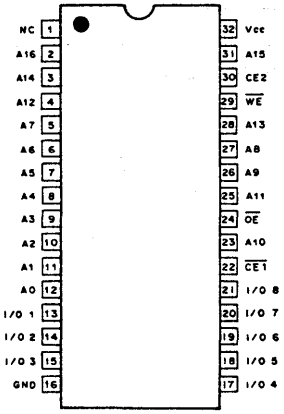
Silicon gate CMOS IC

Block diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A_0 to A_{16}	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	+5V power supply
GND	Ground
NC	No connection

3

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to +7.0	V
Input voltage	V_{IN}		− 0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to Vcc +0.5	V
Allowable power dissipation	P_D	CXK581001P	1.0	W
		CXK581001M	0.7	
Operating temperature	Topr		0 to +70	℃
Storage temperature	Tstg		− 55 to +150	℃
Soldering temperature • time	Tsolder		260 • 10	℃ • sec

* V_{IN}, $V_{I/O}$= − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	Icc
L	H	L	H	Read	Data out	Icc
L	H	×	L	Write	Data in	Icc

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	——	Vcc+0.3	V
Input low voltage	V_{IL}	− 0.3 *	——	0.8	V

* V_{IL}= − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		− 70L/85L			− 70LL/85LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		− 1	—	1	− 1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		− 1	—	1	− 1	—	1	µA
Average operating current	I_{CC}	Cycle=Min, Duty=100% I_{OUT}=0mA		—	47.5	80	—	47.5	80	mA
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc − 0.2V, CE2 ≦ 0.2V or CE2 ≧ Vcc − 0.2V	0 to 70°C	—	—	100	—	—	20	µA
			0 to 40°C	—	—	20	—	—	4	
			+25°C	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	1.2	3	—	1.2	3	mA
Output high voltage	V_{OH}	I_{OH}= − 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

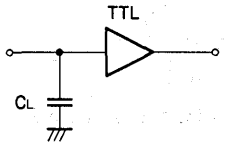
AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.8V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L*=100pF, 1TTL

* C_L includes scope and jig capacitances.



• Read cycle ($\overline{WE}$="H")

Item	Symbol	– 70L/70LL		– 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	ns
Address access time	t_{AA}	—	70	—	85	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	70	—	85	ns
Chip enable access time (CE2)	t_{CO2}	—	70	—	85	ns
Output enable to output valid	t_{OE}	—	40	—	45	ns
Output hold from address change	t_{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2} *	—	25	—	25	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	25	—	25	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

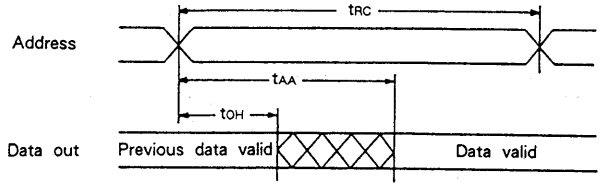
• Write cycle

Item	Symbol	– 70L/70LL		– 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	ns
Address valid to end of write	t_{AW}	60	—	75	—	ns
Chip enable to end of write	t_{CW}	60	—	75	—	ns
Data to write time overlap	t_{DW}	25	—	30	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	60	—	ns
Address set up time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$, $\overline{CE1}$)	t_{WR}	5	—	5	—	ns
Write recovery time (CE2)	t_{WR1}	10	—	10	—	ns
Output active from end of write	t_{OW}	5	—	5	—	ns
Write to output in high Z	t_{WHZ} *	—	25	—	30	ns

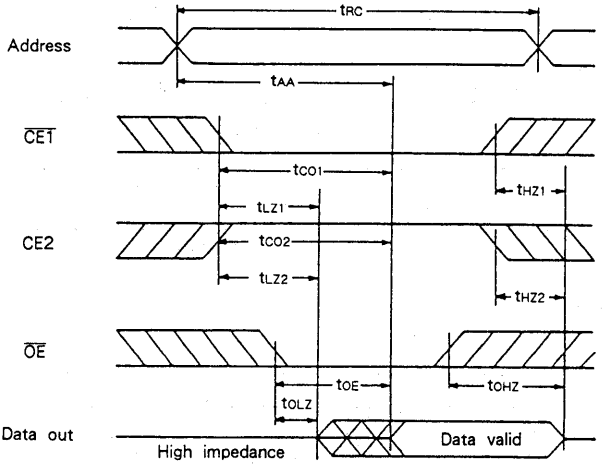
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

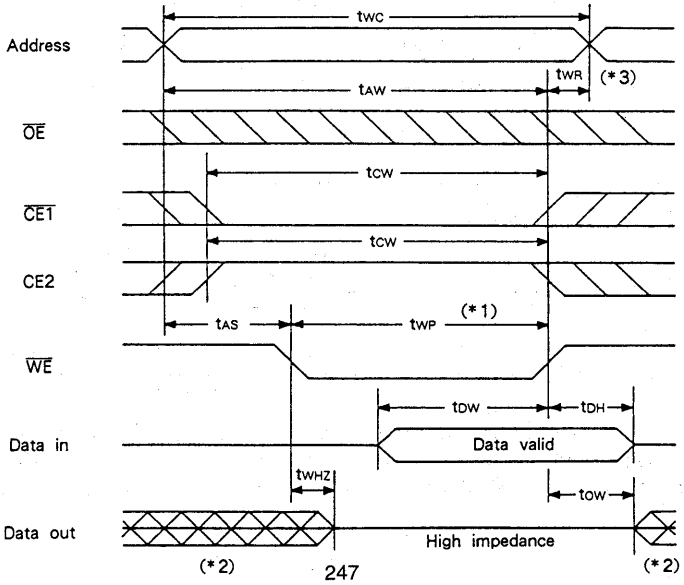
• Read cycle (1): $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



• Read cycle (2): $\overline{WE}$=V_{IH}



• Write cycle (1): $\overline{WE}$ control



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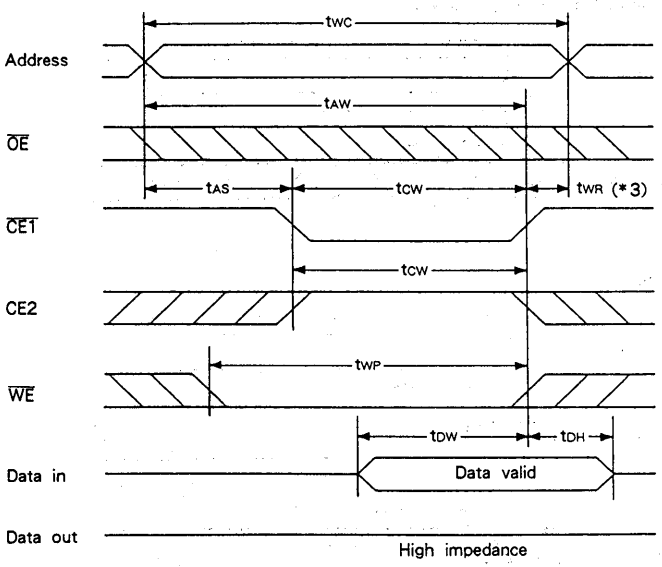
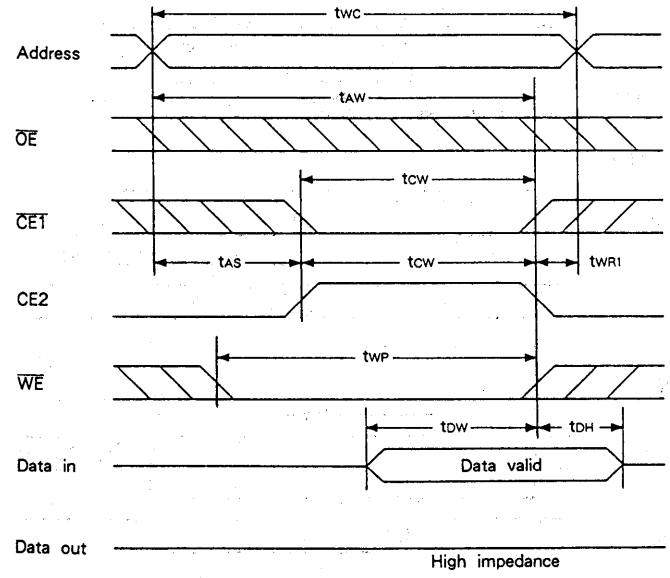
• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): CE2 control



*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
*2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
*3. t_{WR} is tested from the rising edge of $\overline{WE}$ or $\overline{CE1}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70°C)

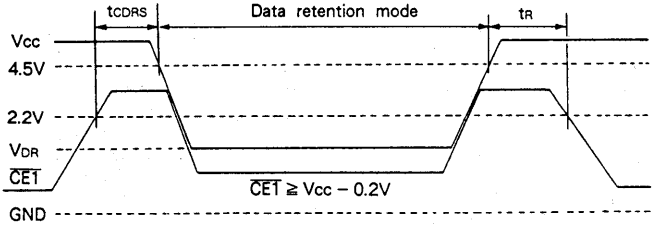
Item	Symbol	Test conditions		− 70L/85L			− 70LL/85LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=0.3V*1	0 to 70°C	—	—	50	—	—	12	µA
			0 to 40°C	—	—	10	—	—	2.4	
			+25°C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	Vcc=2.0 to 5.5V*1		—	2	100	—	0.7	20	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

*1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)

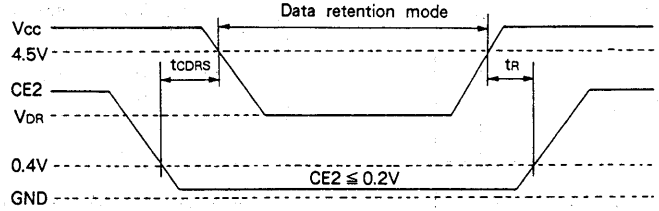
*2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

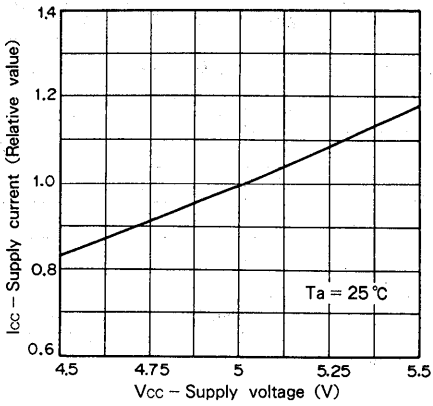


- Low supply voltage data retention waveform (2) (CE2 control)

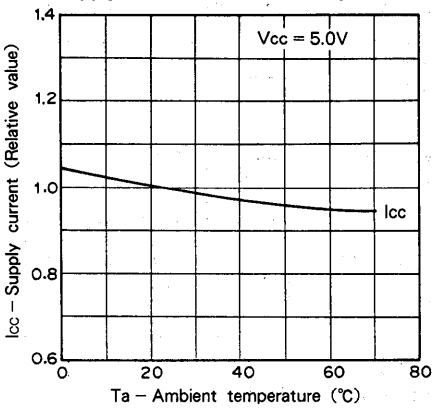


Example of Representative Characteristics

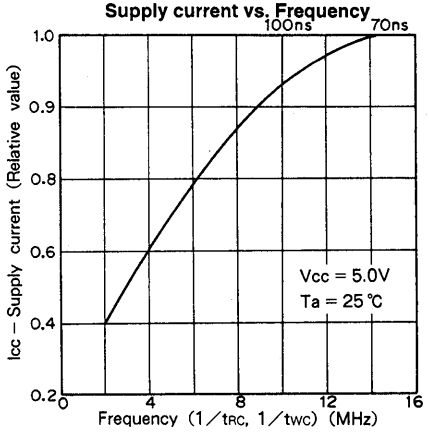
Supply current vs. Supply voltage



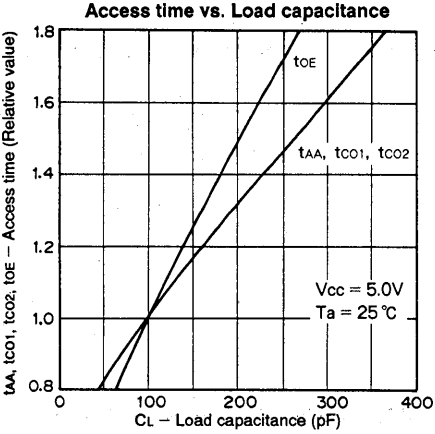
Supply current vs. Ambient temperature



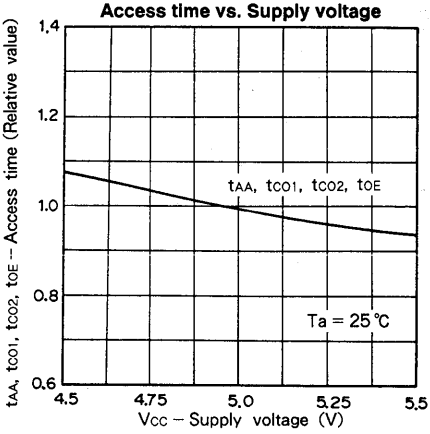
Supply current vs. Frequency



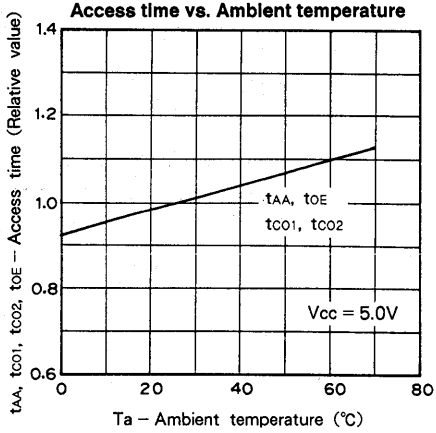
Access time vs. Load capacitance



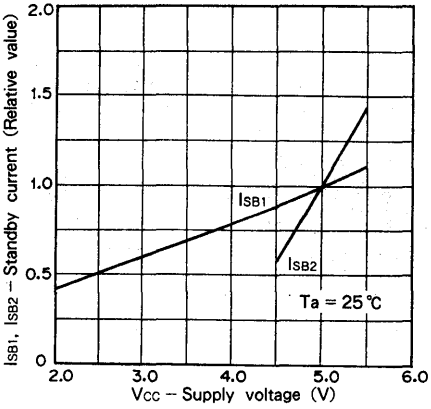
Access time vs. Supply voltage



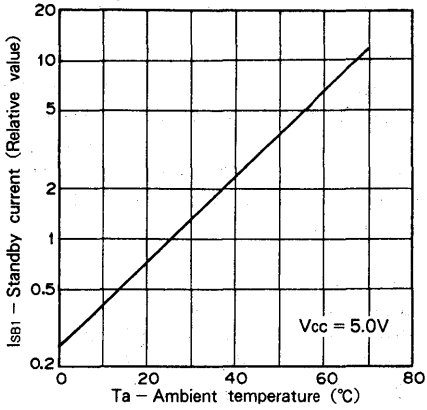
Access time vs. Ambient temperature



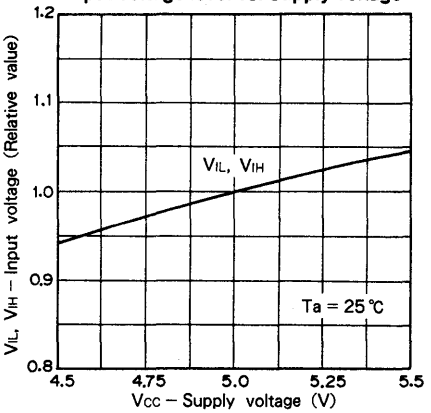
Standby current vs. Supply voltage



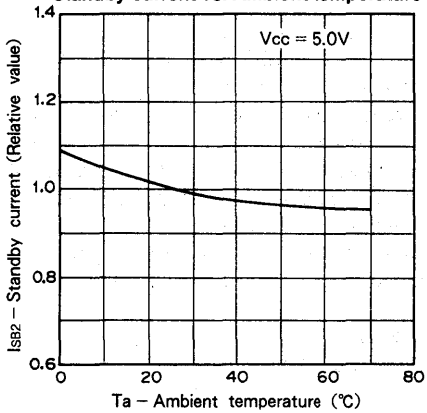
Standby current vs. Ambient temperature



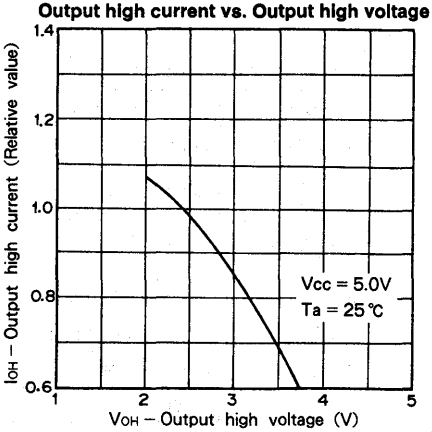
Input voltage level vs. Supply voltage



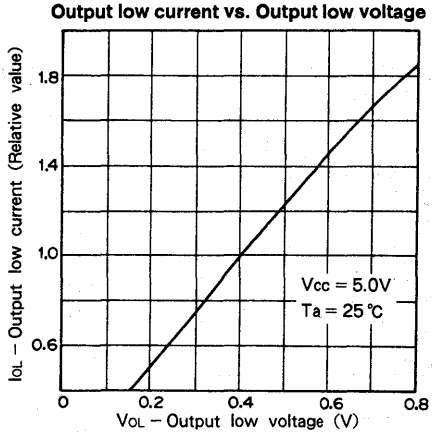
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



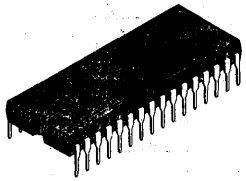
SONY CXK581000P/M -10L/12L/15L -10LL/12LL/15LL

131072-word × 8-bit High Speed CMOS Static RAM

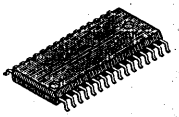
Description

CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131, 072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

CXK581000P
32 pin DIP (Plastic)



CXK581000M
32 pin SOP (Plastic)



Features

- Fast access time : (Access time)
  CXK581000P/M-10L/10LL 100ns (Max.)
  CXK581000P/M-12L/12LL 120ns (Max.)
  CXK581000P/M-15L/15LL 150ns (Max.)
- Low power consumption operation :

	Standby	/DC operation
CXK581000P/M-10L, 12L, 15L ;	10 µW (Typ.)	/35mW (Typ.)
10LL, 12LL, 15LL ;	3.5 µW (Typ.)	/35mW (Typ.)

- Single +5V supply : +5V ± 10%
- Fully static memory ··· No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output:three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
  CXK581000M 525mil 32 pin SOP package

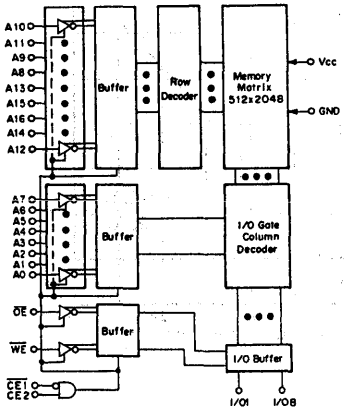
Functions

131,072 word × 8 bit static RAM

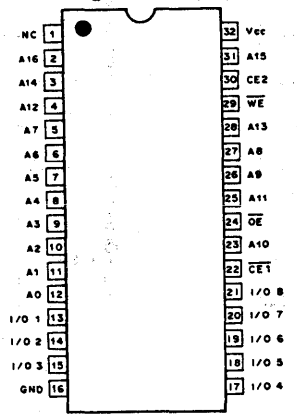
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

E89322C06 – ST

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5 to +7.0	V
Input voltage	V_{IN}		− 0.5 * to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to V_{CC}+0.5	V
Allowable power dissipation	P_D	CXK581000P	1.0	W
		CXK581000M	0.7	
Operating temperature	Topr		0 to +70	℃
Storage temperature	Tstg		− 55 to +150	℃
Soldering temperature	Tsolder		260•10	℃ • sec

* V_{IN}, $V_{I/O}$= − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

* V_{IL}= − 3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		− 10L/12L/15L			− 10LL/12LL/15LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}		−1	—	1	−1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to V_{CC}		−1	—	1	−1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	7	15	—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I_{CC3}	Cycle time 1 µs Duty=100% I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ V_{CC} − 0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ V_{CC} − 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ V_{CC} − 0.2V CE2 ≧ V_{CC} − 0.2V	0 to 70°C	—	—	100	—	—	20	µA
			0 to 40°C	—	—	20	—	—	4	
			+25°C	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}= − 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

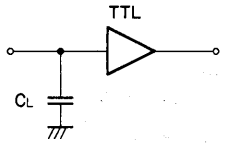
AC characteristics

• AC test conditions (Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.8V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L*=100pF, 1TTL

* C_L includes scope and jig capacitances.

• Test circuit



• Read cycle ($\overline{WE}$="H")

Item	Symbol	−10L/10LL		−12L/12LL		−15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	—	35	—	40	—	50	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

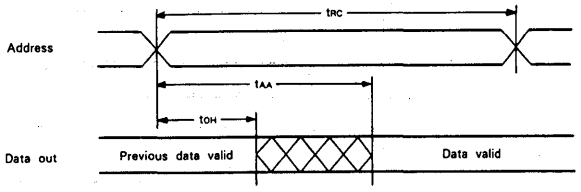
• Write cycle

Item	Symbol	−10L/10LL		−12L/12LL		−15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	—	30	—	30	—	30	ns

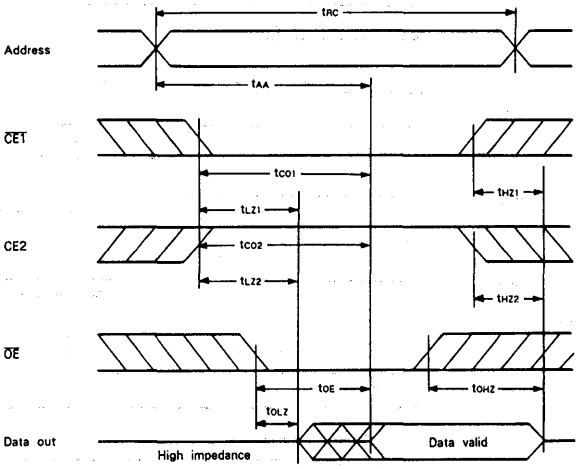
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

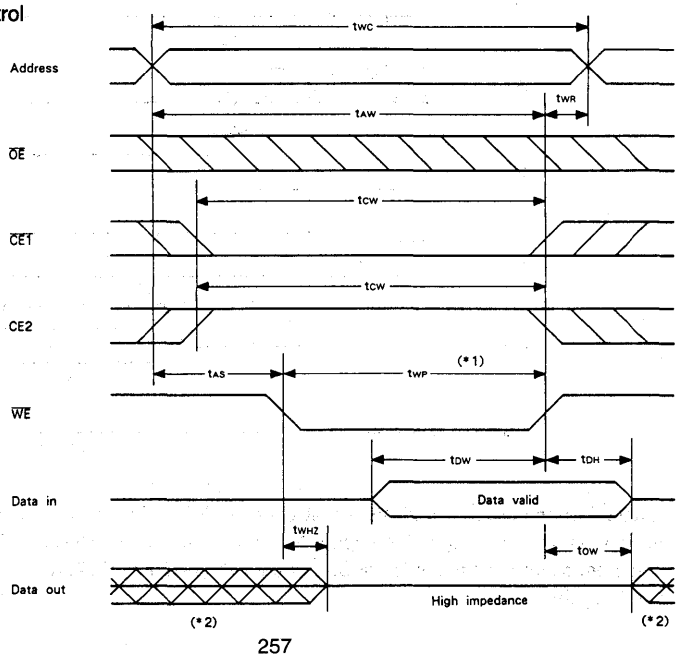
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=VIL, CE2=VIH, $\overline{WE}$=VIH



• Read cycle (2) : $\overline{WE}$=VIH



• Write cycle (1) : $\overline{WE}$ control



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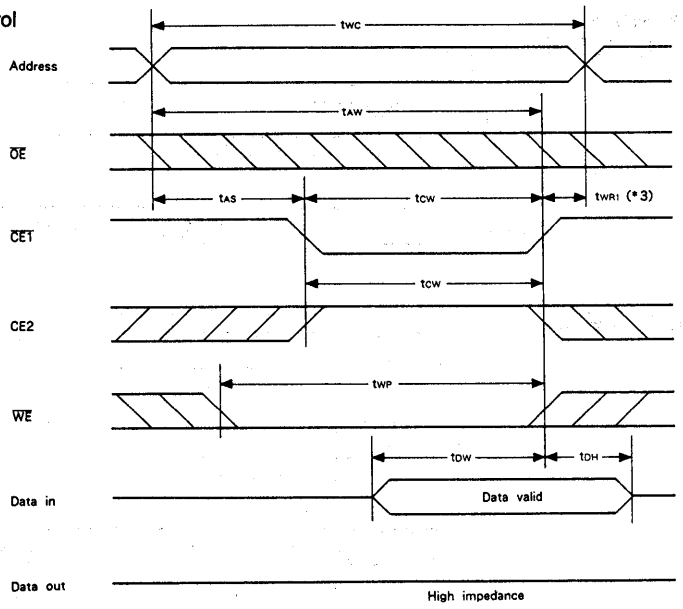
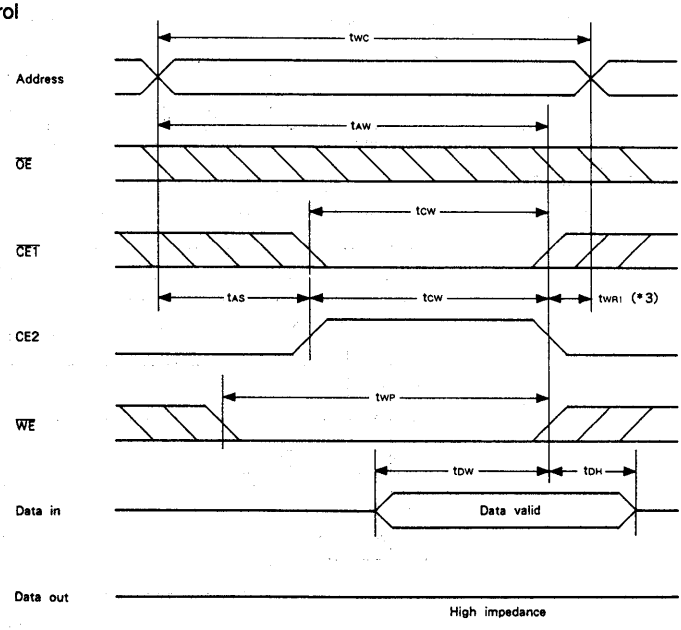
• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

* 1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
* 2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.
* 3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

Item	Symbol	Test conditions		– 10L/12L/15L			– 10LL/12LL/15LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V*1	0 to 70 °C	—	—	50	—	—	12	µA
			0 to 40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V*1		—	2	100	—	0.7	20	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

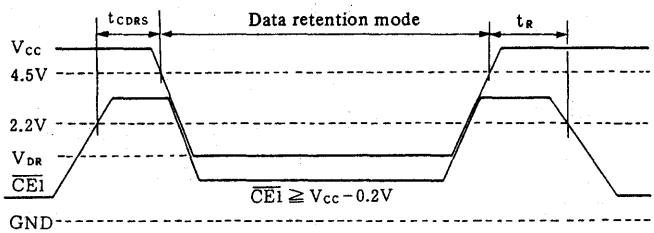
Note)

*1. $\overline{CE1} \geqq V_{CC} - 0.2V$, $CE2 \geqq V_{CC} - 0.2V$ [$\overline{CE1}$ control] or $CE2 \leqq 0.2V$ [CE2 control]

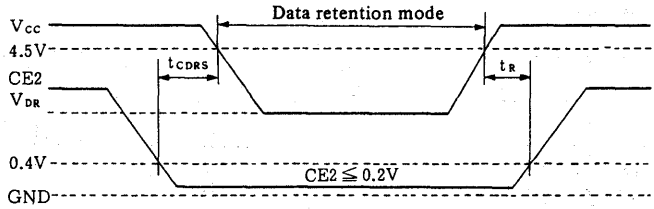
*2. t_{RC} : Read cycle time

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

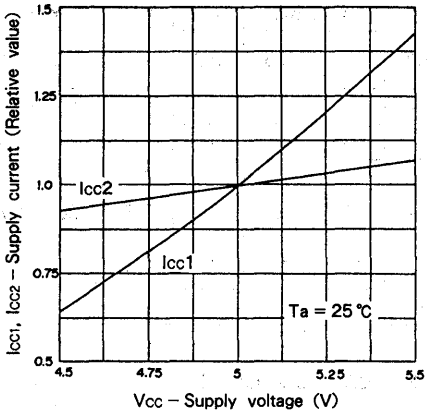


• Low supply voltage data retention waveform (2) (CE2 control)

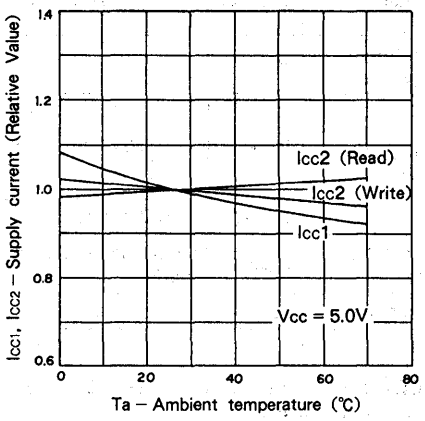


Example of Represeutative Characteristics

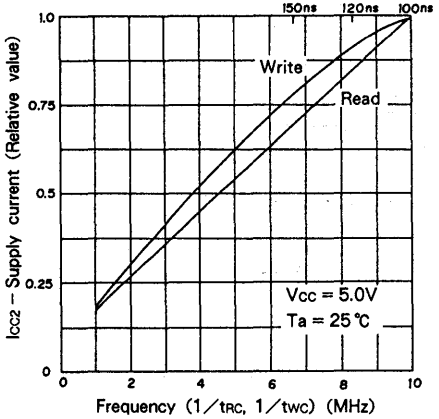
Supply current vs. Supply voltage



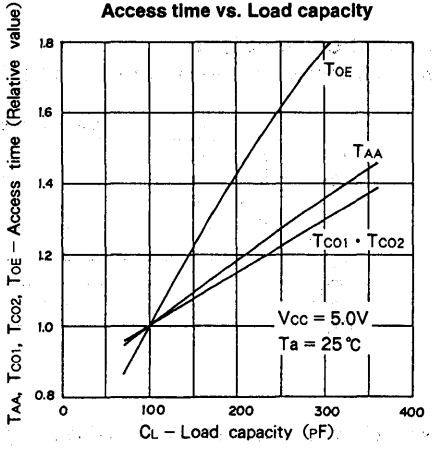
Supply current vs. Ambient temperature



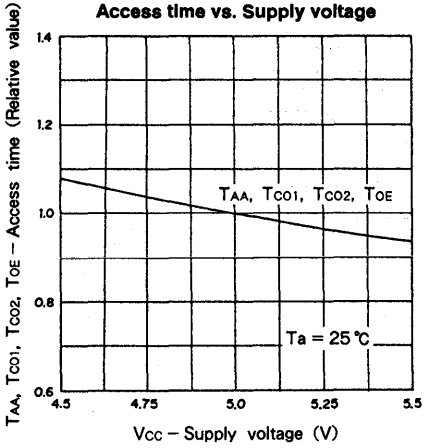
Supply current vs. Frequency



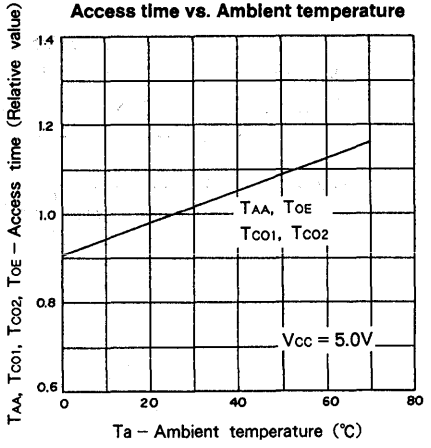
Access time vs. Load capacity



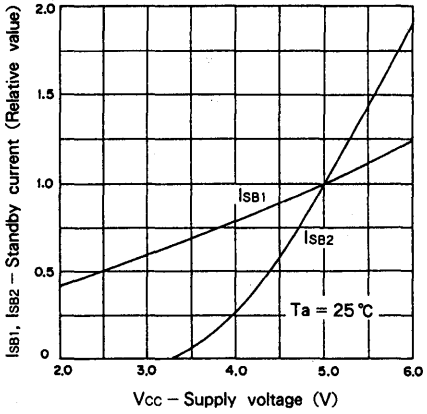
Access time vs. Supply voltage



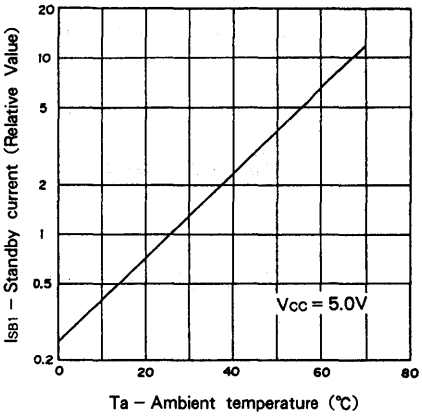
Access time vs. Ambient temperature



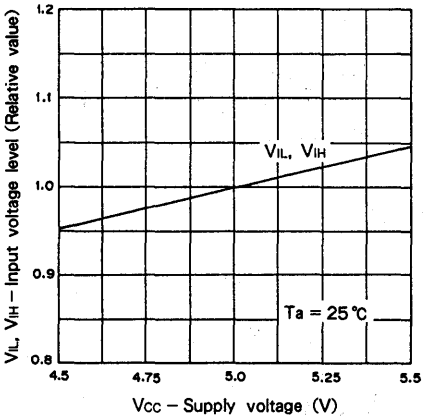
Standby current vs. Supply voltage



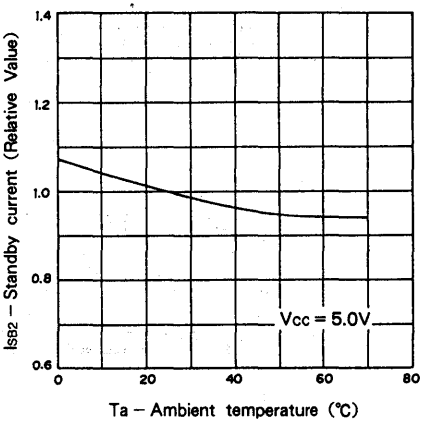
Standby current vs. Ambient temperature



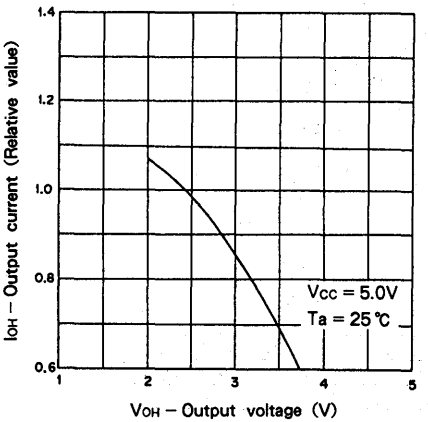
Input voltage level vs. Supply voltage



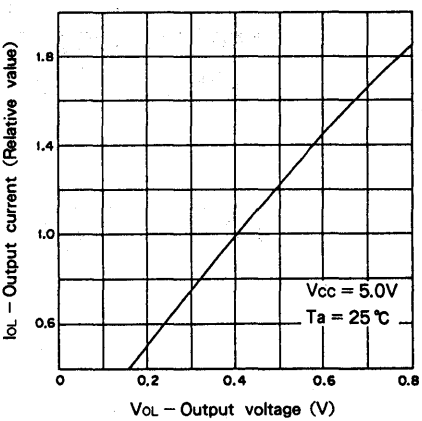
Standby current vs. Ambient temperature



Output current vs. Output voltage



Output current vs. Output voltage



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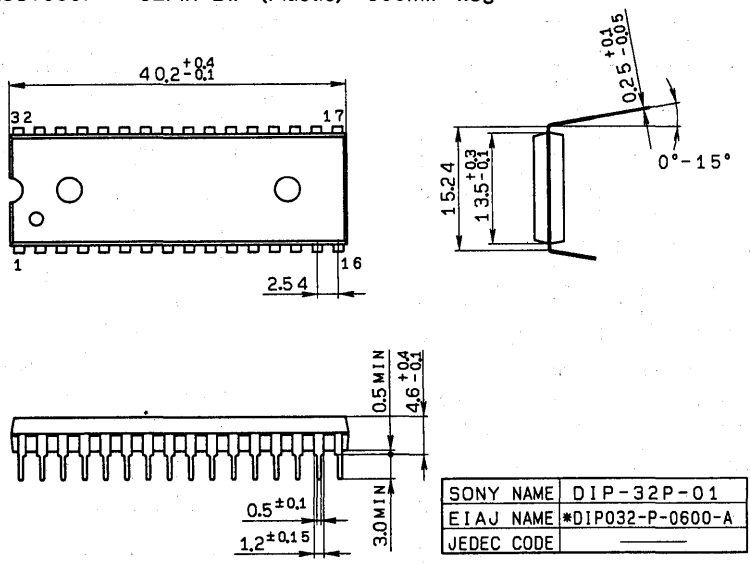
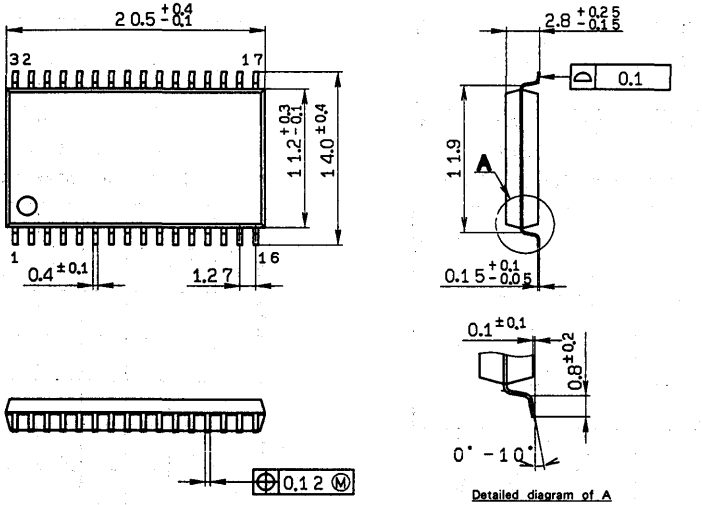
Package Outline Unit : mm

CXK581000P 32Pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	———

CXK581000M 32Pin SOP (Plastic) 525mil 1.2g



SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	———

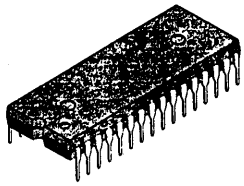
SONY CXK581000P/M -10LX/12LX/15LX/ 10LLX/12LLX/15LLX

131072-word × 8-bit High Speed CMOS Static RAM

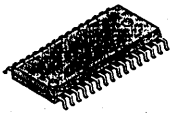
Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

CXK581000P
32 pin DIP (Plastic)



CXK581000M
32 pin SOP (Plastic)



Features

- Extended operating temperature range (−25℃ to +85℃)
- Fast access time (Access time)

CXK581000P/M-10LX/10LLX	100ns (Max.)
CXK581000P/M-12LX/12LLX	120ns (Max.)
CXK581000P/M-15LX/15LLX	150ns (Max.)

- Low power consumption operation

	Standby/DC operation
CXK581000P/M-10LX, 12LX, 15LX	10 μW(Typ.)/35mW(Typ.)
CXK581000P/M-10LLX, 12LLX, 15LLX	3.5 μW(Typ.)/35mW(Typ.)

- Single +5V power supply : +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.2V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package

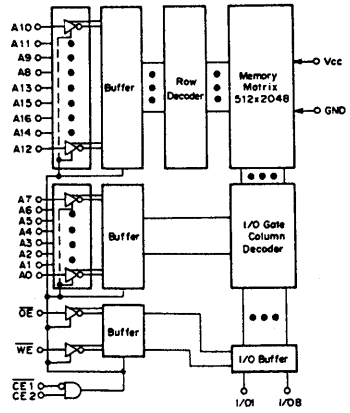
Function

131072-word × 8-bit static RAM

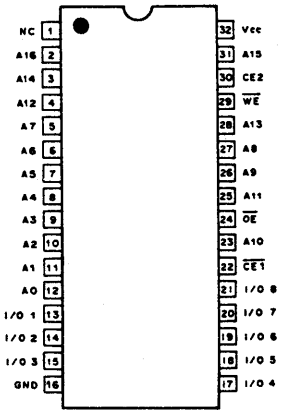
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

3

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		−0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK581000P	1.0	W
		CXK581000M	0.7	
Operating temperature	Topr		−25 to +85	°C
Storage temperature	Tstg		−55 to +150	°C
Soldering temperature • time	Tsolder		260 • 10	°C • sec

* V_{IN}, $V_{I/O}$ = −3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = −25 to +85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.6	V

* V_{IL} = −3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = − 25 to + 85°C)

Item	Symbol	Test conditions		−10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		−1	—	1	−1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}		−1	—	1	−1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	7	15	—	7	15	mA
Average operating current	I_{CC2}	Cycle = Min. Duty = 100%, I_{OUT} = 0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I_{CC3}	Cycle time 1 µs Duty = 100%, I_{OUT} = 0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ V_{CC} − 0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ V_{CC} − 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ V_{CC} − 0.2V CE2 ≧ V_{CC} − 0.2V	− 25 to 85°C	—	—	200	—	—	40	µA
			− 25 to 70°C	—	—	100	—	—	20	
			− 25 to 40°C	—	—	20	—	—	4	
			+ 25°C	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = − 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

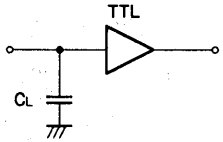
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(Vcc = 5V ± 10%, Ta = − 25 to + 85℃)

Item	Conditions
Input pulse high level	V_{IH} = 2.4V
Input pulse low level	V_{IL} = 0.6V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	C_L* = 100pF, 1TTL



* CL includes scope and jig capacitances

• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	−10LX/10LLX		−12LX/12LLX		−15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

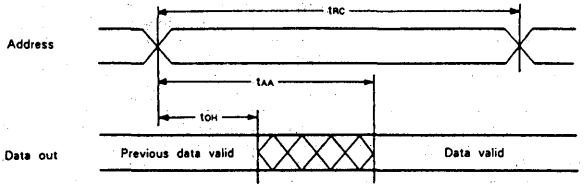
• **Write cycle**

Item	Symbol	−10LX/10LLX		−12LX/12LLX		−15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	—	30	—	30	—	30	ns

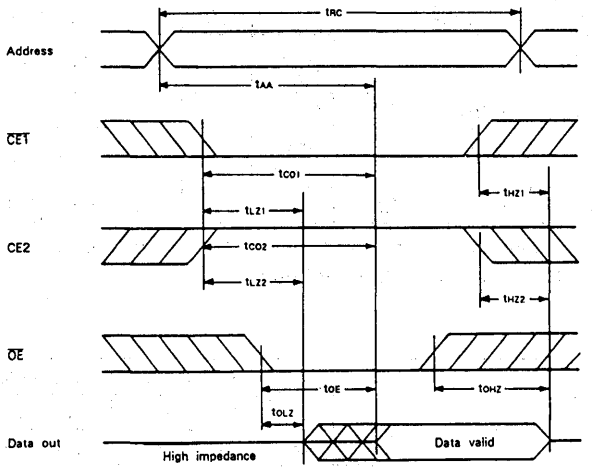
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

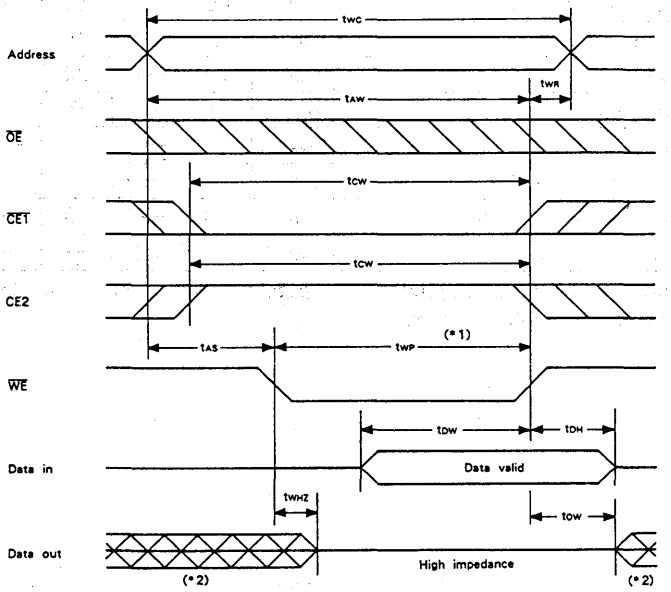
• Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



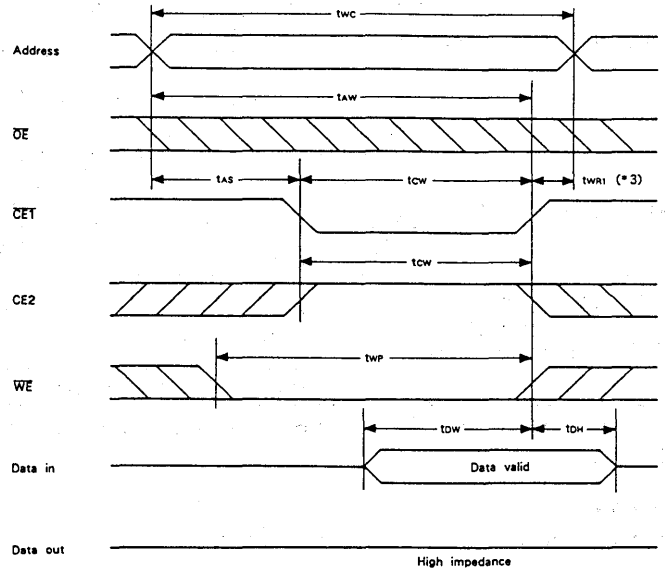
• Read cycle (2) : $\overline{WE} = V_{IH}$



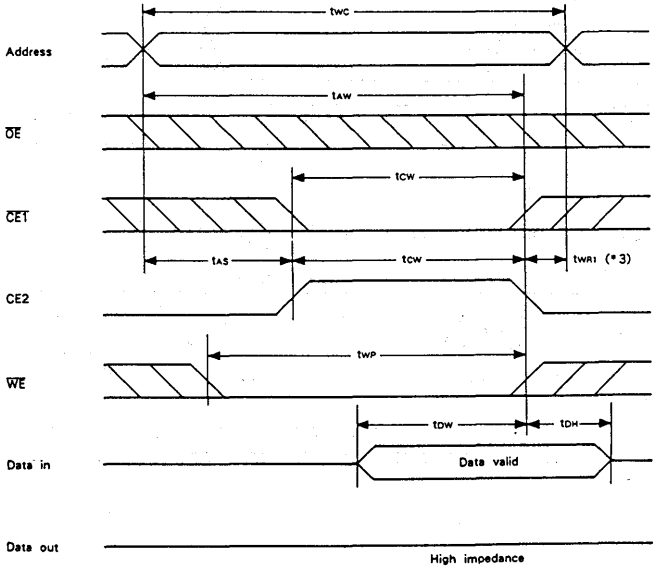
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.

*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

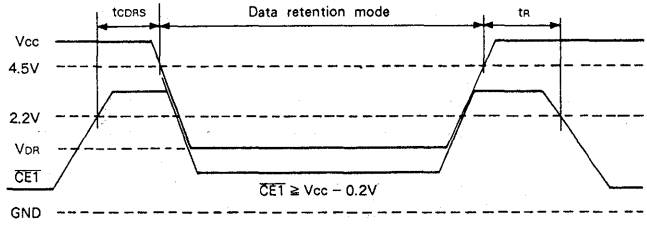
(Ta = −25 to 85°C)

Item	Symbol	Test conditions		−10LX/12LX/15LX			−10LLX/12LLX/15LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.2	—	5.5	2.2	—	5.5	V
Data retention current	I_{CCDR1}	Vcc = 3.0V*1	−25 to 85°C	—	—	100	—	—	24	µA
			−25 to 70°C	—	—	50	—	—	12	
			−25 to 40°C	—	—	10	—	—	2.4	
			+25°C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	Vcc = 2.2 to 5.5V*1		—	2	200	—	0.7	40	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

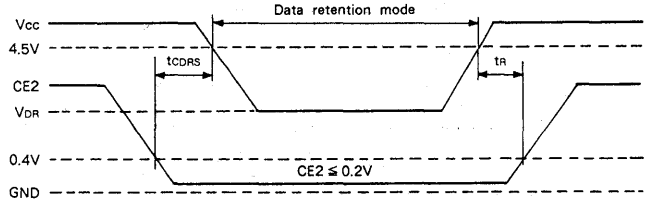
*1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)
*2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

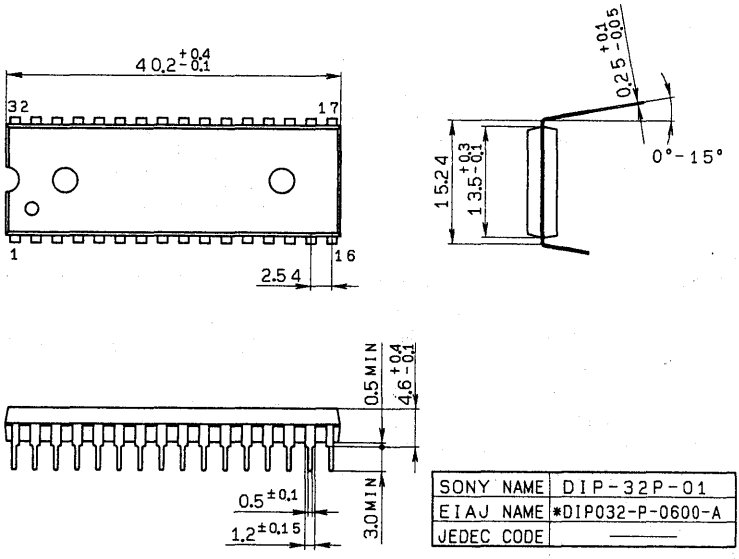


- Low supply voltage data retention waveform (2) (CE2 control)



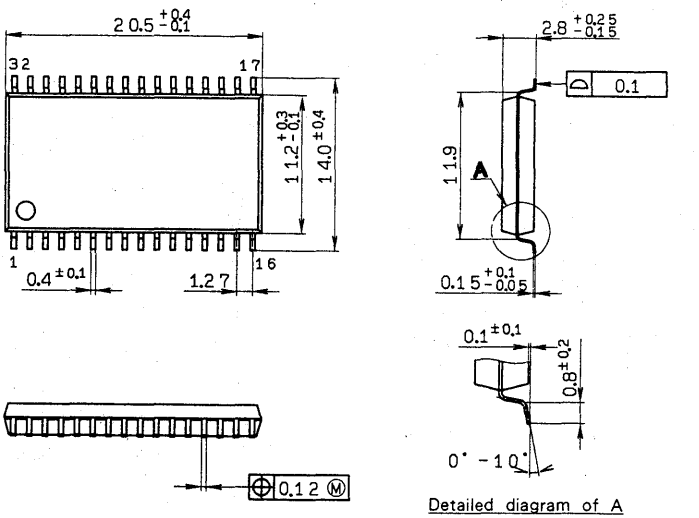
Package Outline Unit : mm

CXK581000P 32 pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	———

CXK581000M 32 pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	———

SONY

CXK581000P/M -12LB

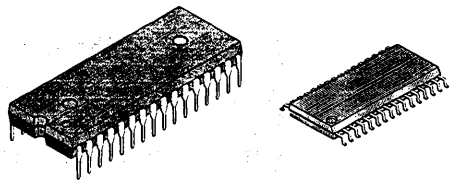
131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

CXK581000P
32 pin DIP (Plastic)

CXK581000M
32 pin SOP (Plastic)



Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Fast access time: (Access time)
  3V Operation; 240ns (Max.)
  5V Operation; 120ns (Max.)
- Low power consumption operation:
  Standby/ DC operation
  3V Operation; 3 µW (Typ.) / 1.2mW (Typ.)
  5V Operation; 10 µW (Typ.) / 35mW (Typ.)
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
  CXK581000M 525mil 32 pin SOP package

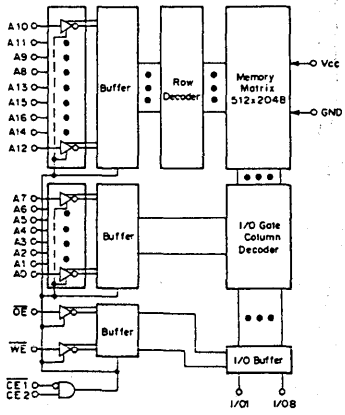
Function

131,072-word × 8-bit static RAM

Structure

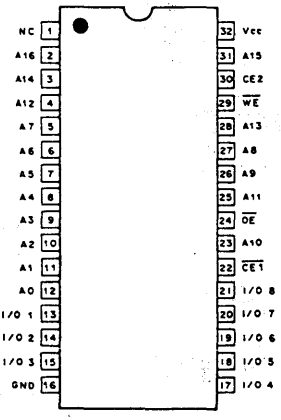
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		–0.5 to +7.0	V
Input voltage	V_{IN}		–0.5 * to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$		–0.5 * to V_{CC}+0.5	V
Allowable power dissipation	P_D	CXK581000P	1.0	W
		CXK581000M	0.7	
Operating temperature	Topr		0 to +70	°C
Storage temperature	Tstg		–55 to +150	°C
Soldering temperature • time	Tsolder		260 • 10	°C • sec

* V_{IN}, $V_{I/O}$=–3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Vcc=5V ± 10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	–0.3 *	—	0.8	–0.3 *	—	0.4	V

* V_{IL}=–3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		−1	—	1	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	0.4	0.8	—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	Write cycle	—	10	15	—	35	60	mA
			Read cycle	—	10	15	—	25	40	
	I_{CC3}	Cycle time 1 μs Duty=100% I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ Vcc−0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ Vcc−0.2V	Write cycle	—	5	10	—	10	20	mA
			Read cycle	—	2.5	5	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc−0.2V CE2 ≧ Vcc−0.2V	0 to +70°C	—	—	60	—	—	100	μA
			0 to +40°C	—	—	12	—	—	20	
			+25°C	—	1.2	5	—	2	8	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.06	0.3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

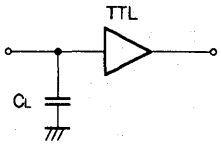
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=2.7 to 5.5V, Ta=0 to +70°C)

Item	Conditions	
	Vcc=3V	Vcc=5V
Input pulse high level	V_{IH}=2.2V	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.4V	V_{IL}=0.8V
Input rise time	tr=5ns	tr=5ns
Input fall time	tf=5ns	tf=5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C_L*=100pF, 1TTL	C_L*=100pF, 1TTL



* C_L includes scope and jig capacitances.

• **Read cycle** ($\overline{WE}$="H")

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	240	—	120	—	ns
Address access time	t_{AA}	—	240	—	120	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	240	—	120	ns
Chip enable access time (CE2)	t_{CO2}	—	240	—	120	ns
Output enable to output valid	t_{OE}	—	120	—	60	ns
Output hold from address change	t_{OH}	30	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	20	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	10	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1} *, t_{HZ2} *	—	80	—	40	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	80	—	40	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

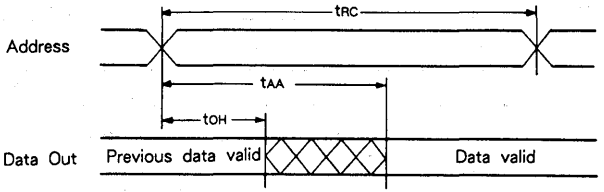
• **Write cycle**

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	240	—	120	—	ns
Address valid to end of write	t_{AW}	170	—	85	—	ns
Chip enable to end of write	t_{CW}	170	—	85	—	ns
Data to write time overlap	t_{DW}	100	—	50	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	160	—	80	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}	20	—	10	—	ns
Write to output in high Z	t_{WHZ} *	—	60	—	30	ns

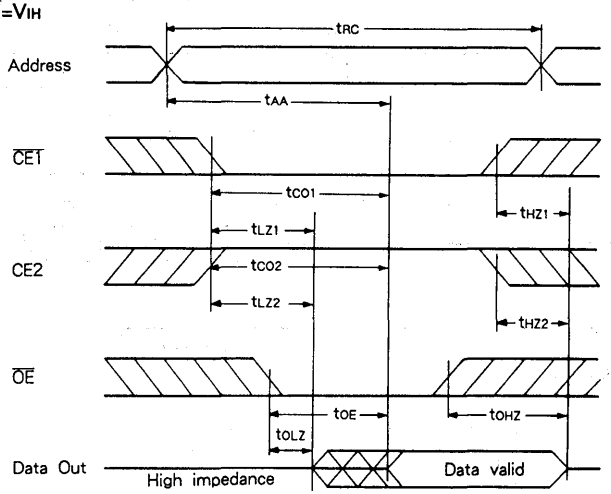
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

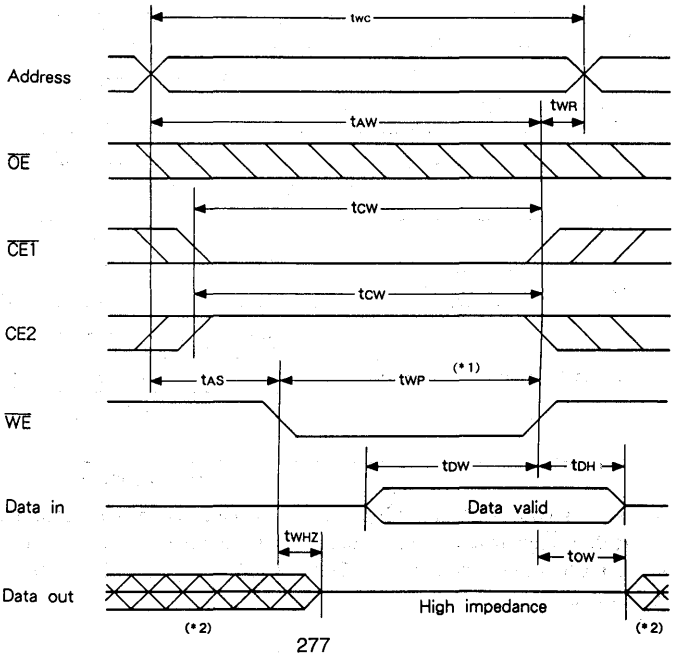
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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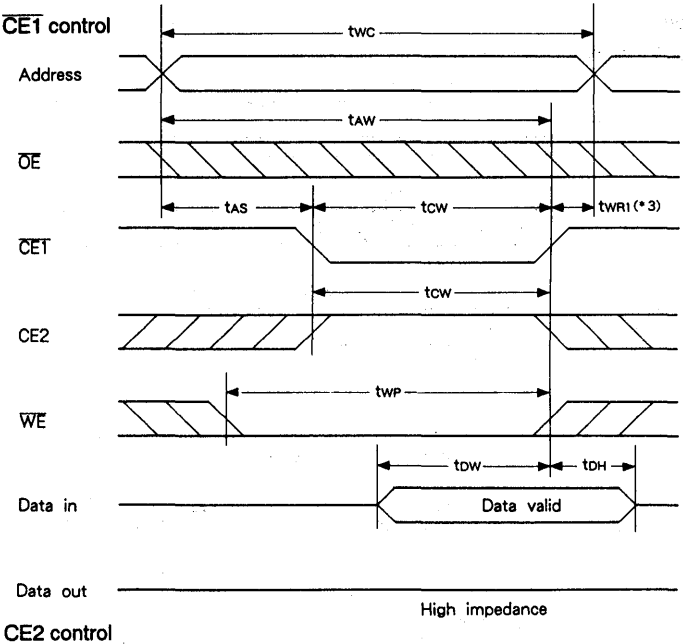
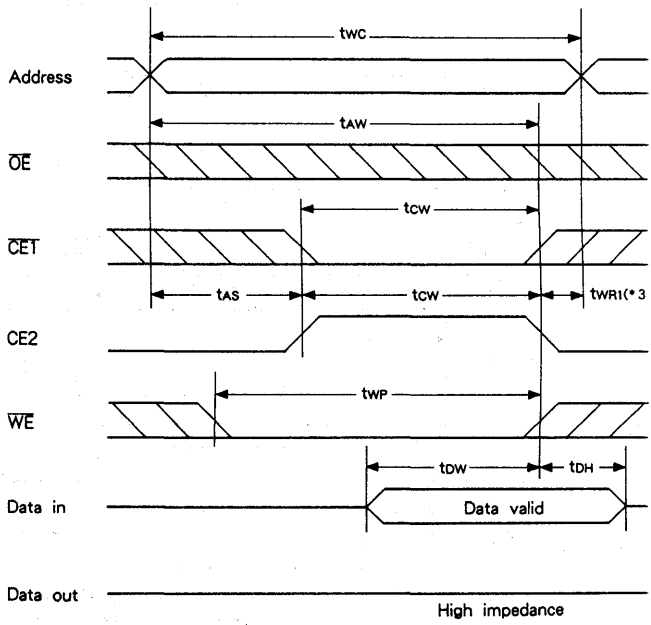
• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
*2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.
*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to +70°C)

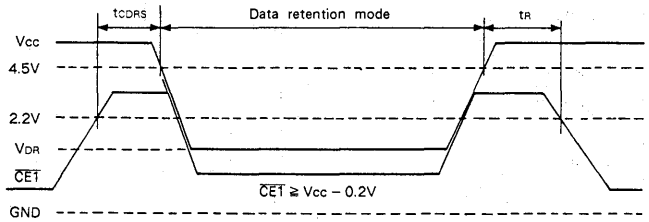
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V *1	0 to +70°C	—	—	50	μA
			0 to +40°C	—	—	10	
			+25°C	—	1	4	
	I_{CCDR2}	Vcc=2.0 to 5.5V *1		—	2	100	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			t_{RC} *2	—	—	ns

*1. $\overline{CE1} \geqq V_{CC}-0.2V$, $CE2 \geqq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)

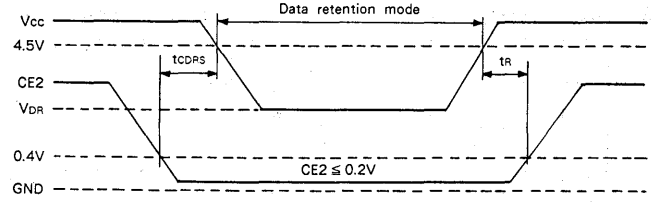
*2. t_{RC} : Read cycle time

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



- Low supply voltage data retention waveform (2) : CE2 control



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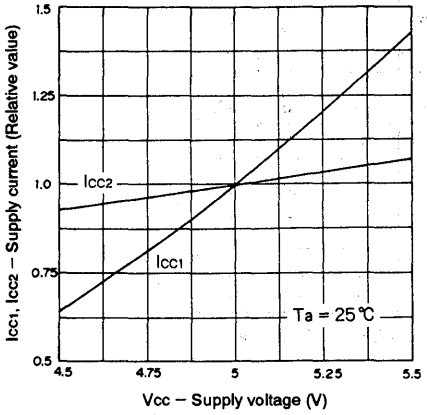
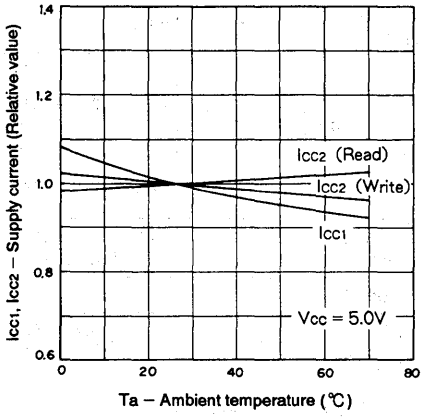
Example of Representative Characteristics

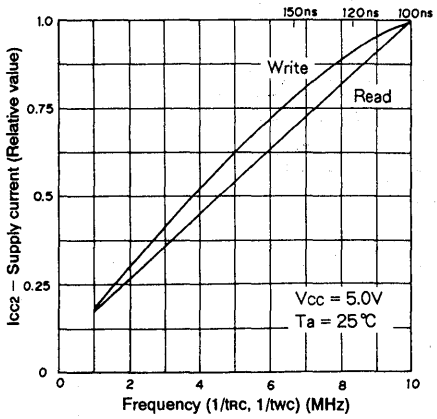
Supply current vs. Supply voltage



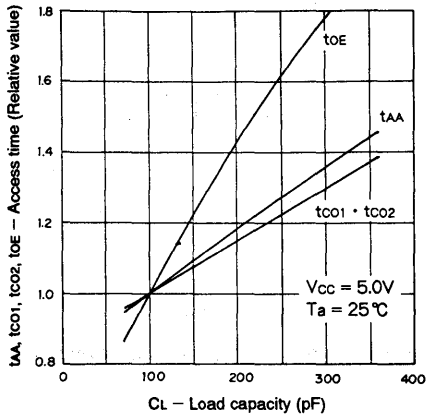
Supply current vs. Ambient temperature



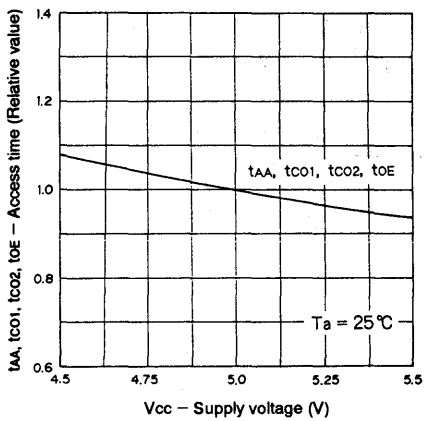
Supply current vs. Frequency



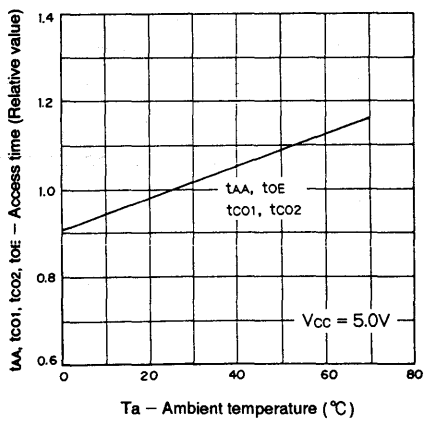
Access time vs. Load capacity



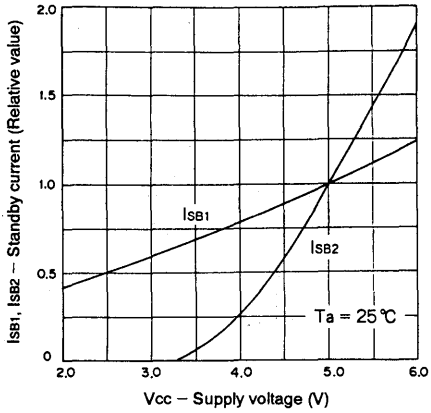
Access time vs. Supply voltage



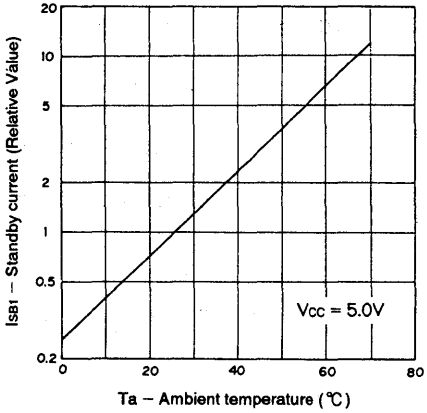
Access time vs. Ambient temperature



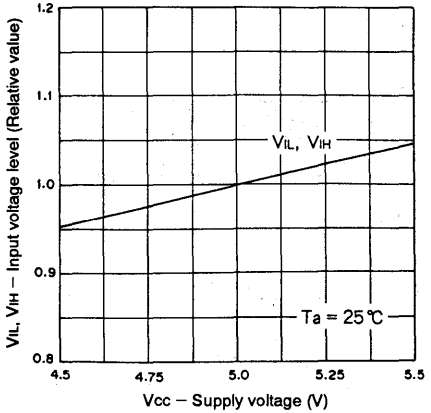
Standby current vs. Supply voltage



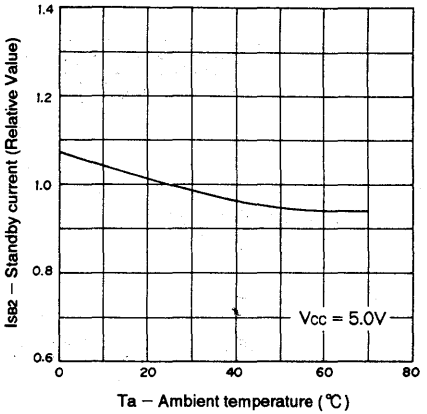
Standby current vs. Ambient temperature



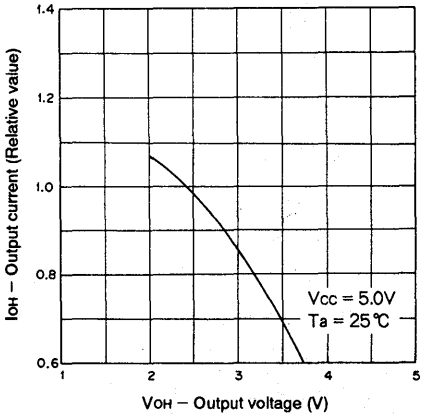
Input voltage level vs. Supply voltage



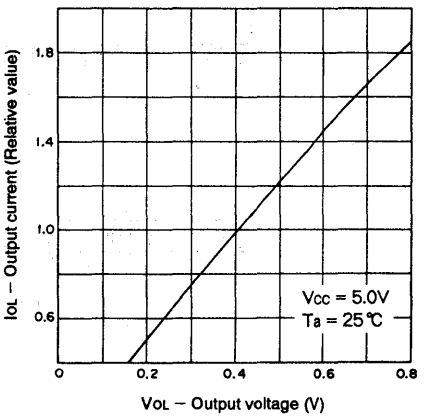
Standby current vs. Ambient temperature



Output current vs. Output voltage



Output current vs. Output voltage



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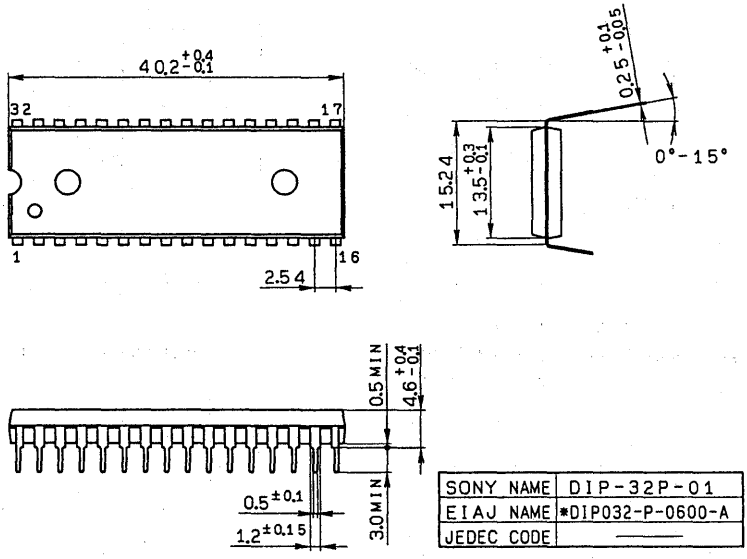
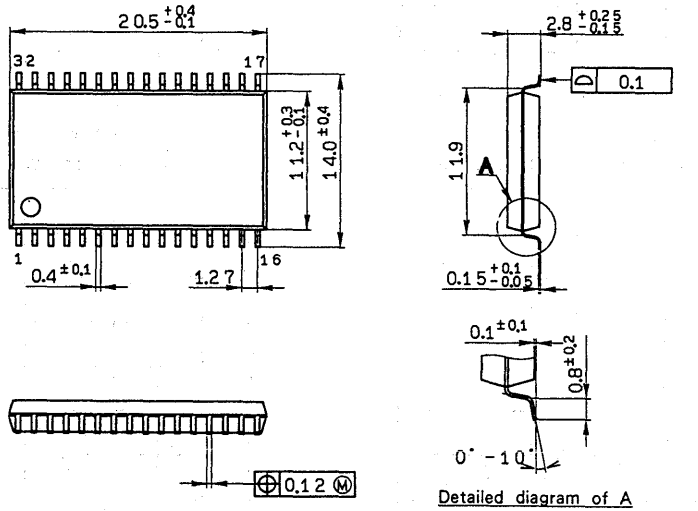
Package Outline Unit : mm

CXK581000P 32pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	———

CXK581000M 32pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	———

SONY CXK581100TM/YM -10L/12L/15L -10LL/12LL/15LL

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a 1M bits, 131072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Thin Small-outline Packages of EIAJ standard :
  CXK581100TM :
  8mm × 20mm 32 pin TSOP
  CXK581100YM :
  8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current :
  L-Version :
  100 µA (Max.) @Vcc=5.5V, Ta=0 to 70°C
  LL-Version :
  20 µA (Max.) @Vcc=5.5V, Ta=0 to 70°C
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
  CXK581100TM/YM-10L, -10LL 100ns (Max.)
  CXK581100TM/YM-12L, -12LL 120ns (Max.)
  CXK581100TM/YM-15L, -15LL 150ns (Max.)
- Single +5V Supply : +5V ± 10%

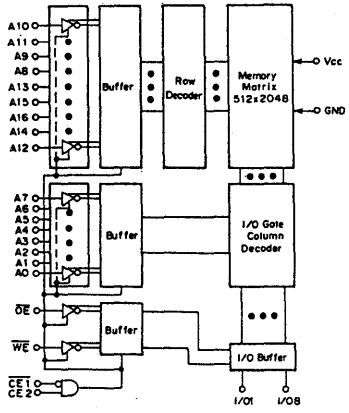
Function

131072-word × 8-bit static RAM

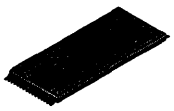
Structure

Silicon gate CMOS IC

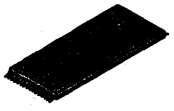
Block Diagram



CXK581100TM
32 pin TSOP (Plastic)



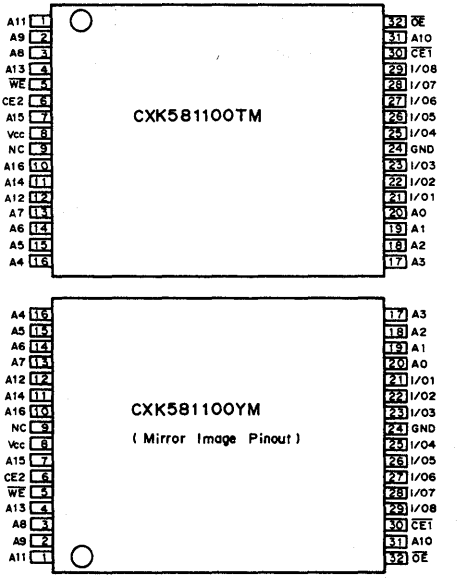
CXK581100YM
32 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



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Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5 * to +7.0	V
Input voltage	V_{IN}	− 0.5 * to V_{CC} +0.5	V
Input and output voltage	$V_{I/O}$	− 0.5 * to V_{CC} +0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	− 55 to +150	℃
Soldering temperature • time	Tsolder	235 • 10	℃ • sec

* V_{IN}, $V_{I/O}$= − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

* V_{IL}= − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		− 10L/12L/15L			− 10LL/12LL/15LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}		−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to V_{CC}		−1	—	1	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	7	15	—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I_{CC3}	Cycle time 1 μs Duty=100% I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ V_{CC} − 0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ V_{CC} − 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ V_{CC} − 0.2V CE2 ≧ V_{CC} − 0.2V	0 to 70°C	—	—	100	—	—	20	μA
			0 to 40°C	—	—	20	—	—	4	
			+25°C	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}= − 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

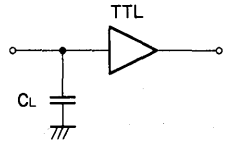
AC characteristics

• AC test conditions (Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.8V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L*=100pF, 1TTL

* C_L includes scope and jig capacitances.

• Test circuit



• Read cycle ($\overline{WE}$="H")

Item	Symbol	− 10L/10LL		− 12L/12LL		− 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	—	35	—	40	—	50	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

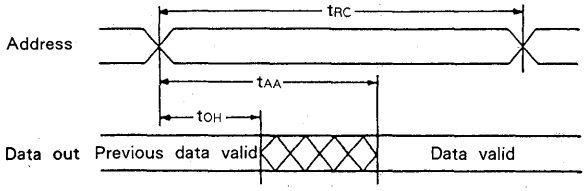
• Write cycle

Item	Symbol	− 10L/10LL		− 12L/12LL		− 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	—	30	—	30	—	30	ns

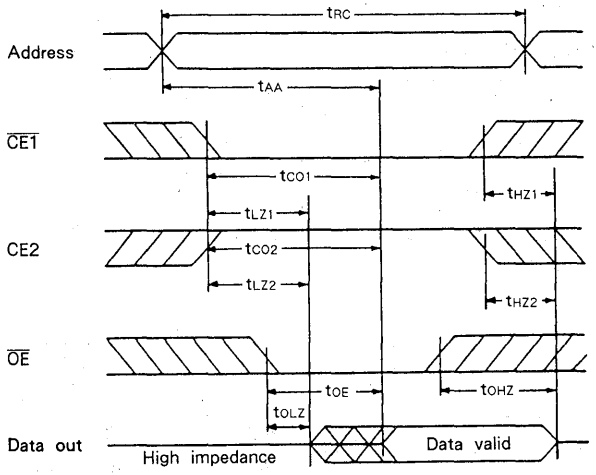
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

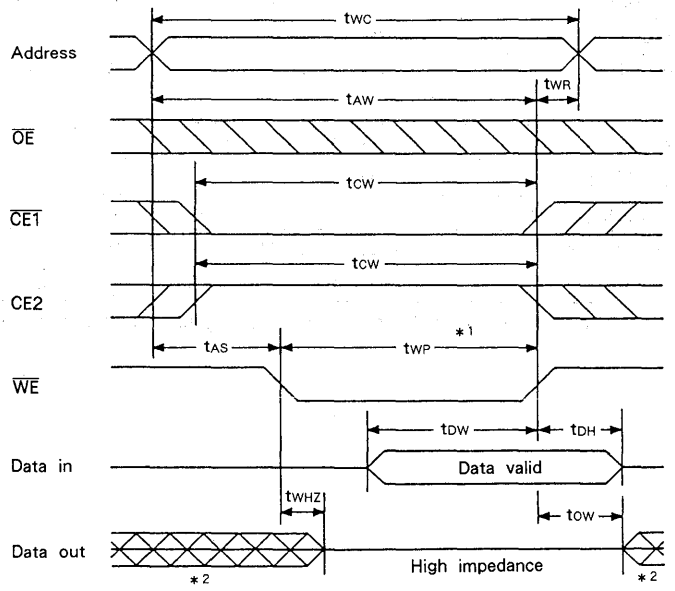
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



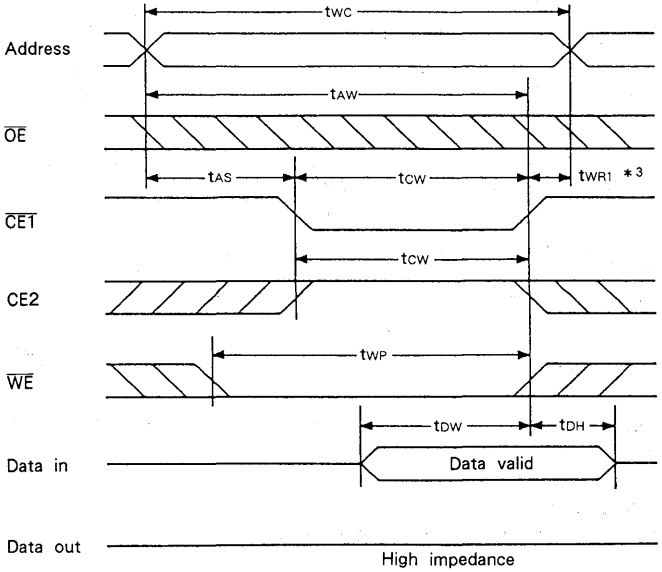
• Read cycle (2) : $\overline{WE}$=V_{IH}



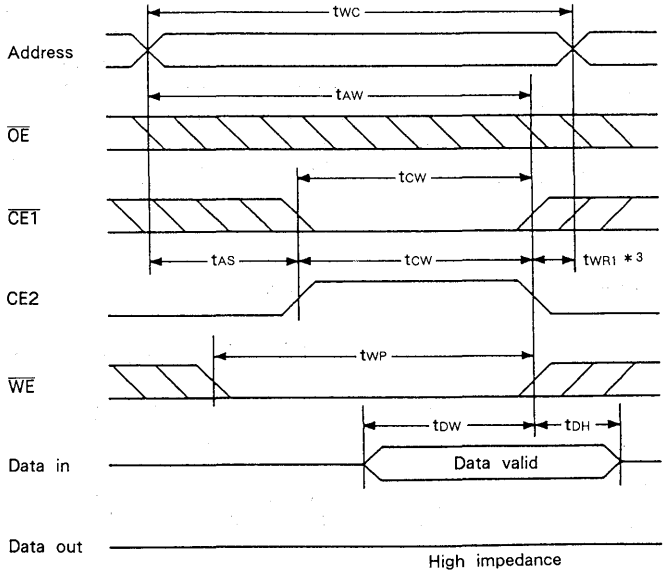
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.

*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70°C)

Item	Symbol	Test conditions		– 10L/12L/15L			– 10LL/12LL/15LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC}=3.0V*1	0 to 70°C	—	—	50	—	—	12	μA
			0 to 40°C	—	—	10	—	—	2.4	
			+25°C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	V_{CC}=2.0 to 5.5V*1		—	2	100	—	0.7	20	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

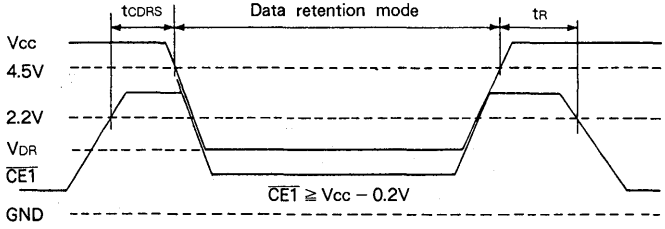
Note)

*1. $\overline{CE1} \geqq V_{CC} - 0.2V$, $CE2 \geqq V_{CC} - 0.2V$ [$\overline{CE1}$ control] or $CE2 \leqq 0.2V$ [CE2 control]

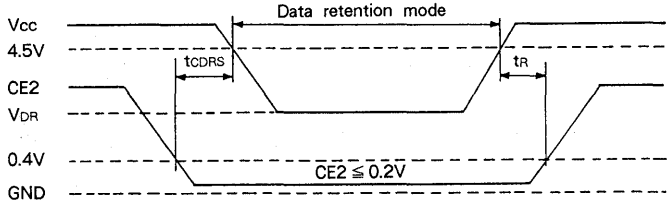
*2. t_{RC} : Read cycle time

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

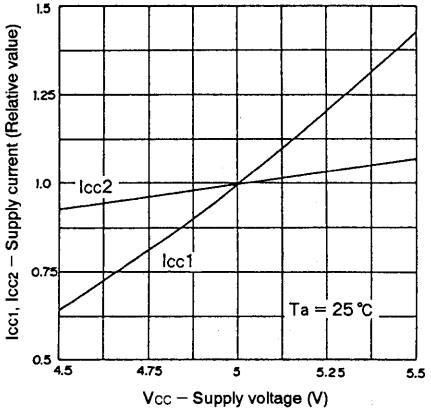


• Low supply voltage data retention waveform (2) (CE2 control)

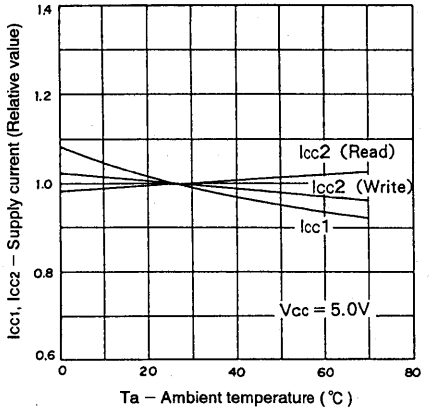


Example of Represeutative Characteristics

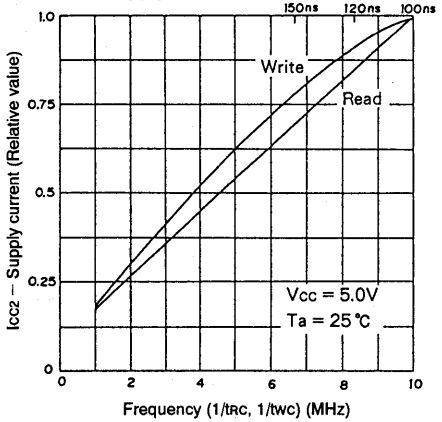
Supply current vs. Supply voltage



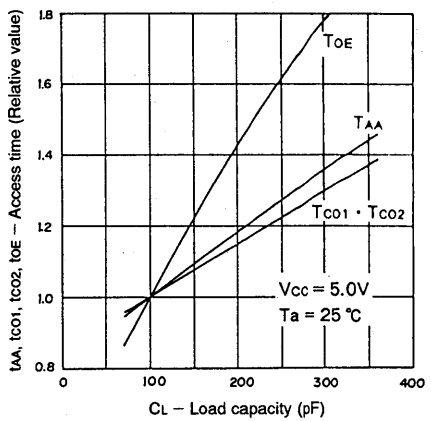
Supply current vs. Ambient temperature



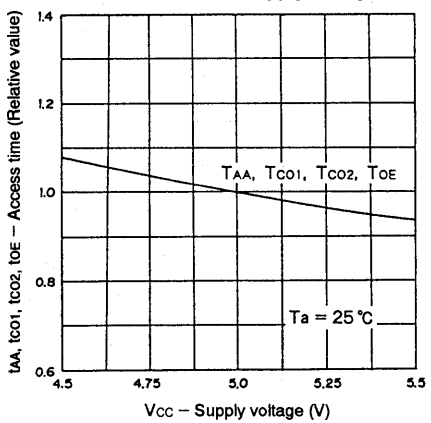
Supply current vs. Frequency



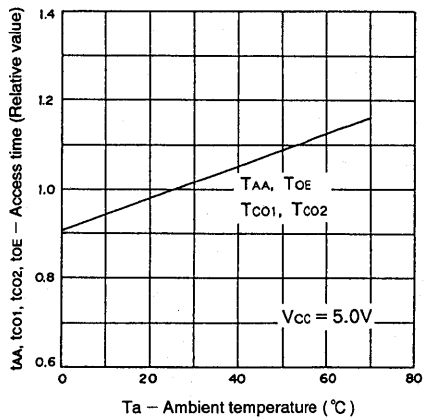
Access time vs. Load capacity



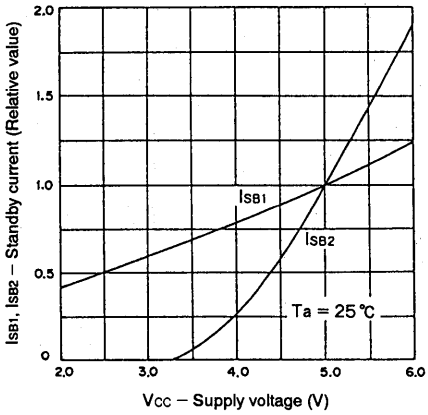
Access time vs. Supply voltage



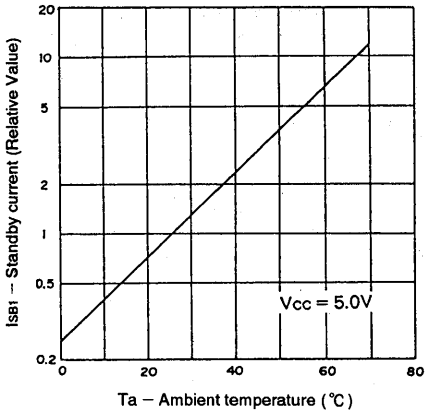
Access time vs. Ambient temperature



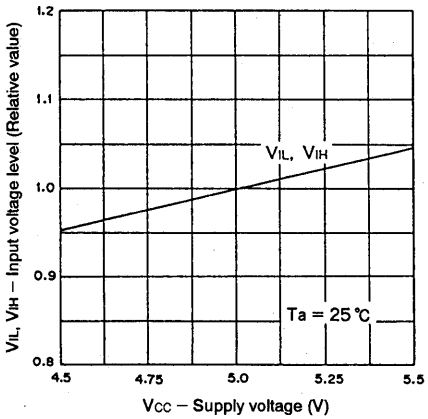
Standby current vs. Supply voltage



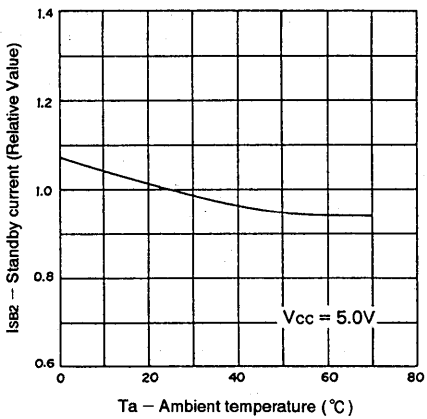
Standby current vs. Ambient temperature



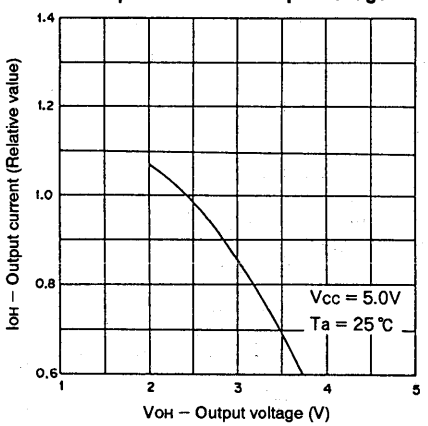
Input voltage level vs. Supply voltage



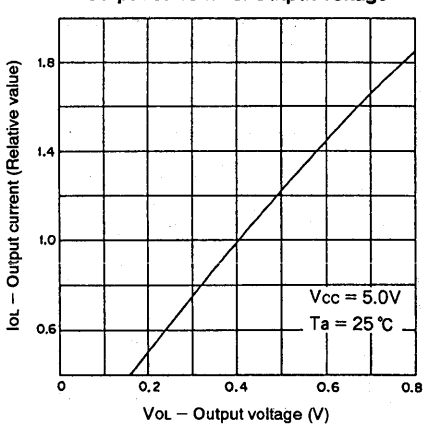
Standby current vs. Ambient temperature



Output current vs. Output voltage



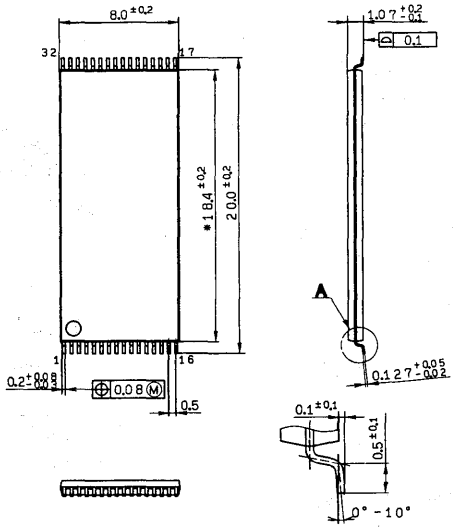
Output current vs. Output voltage



Package Outline Unit: mm

CXK581100TM

32pin TSOP (Plastic)

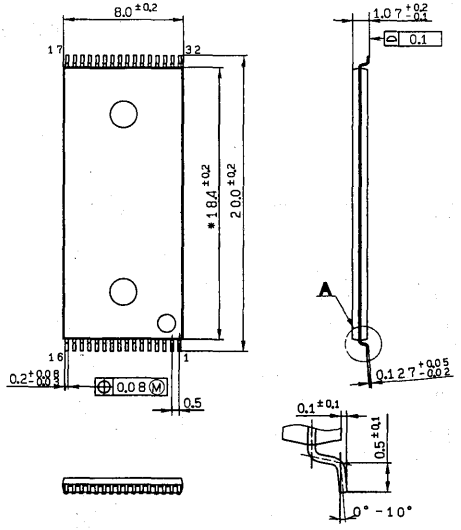


Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581100YM

32pin TSOP (Plastic)



Note) Dimensions marked with * do not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	

3

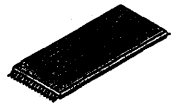
SONY CXK581100TM/YM -10LX/12LX/15LX -10LLX/12LLX/15LLX

131072-word × 8-bit High Speed CMOS Static RAM

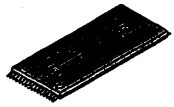
Description

CXK581100TM/YM is a 1M bits, 131,072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to extending operating temperature range and low power consumption.

CXK581100TM
32 pin TSOP (Plastic)



CXK581100YM
32 pin TSOP (Plastic)



Features

- Extended operating temperature range (–25 to +85 °C)
- Thin small-outline packages of EIAJ standard:
  CXK581100TM:
  8mm × 20mm 32 pin TSOP
  CXK581100YM:
  8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current:
  LX-Version:
  200 µA (Max.) @Vcc=5.5V, Ta=–25 to +85 °C
  LLX-Version:
  40 µA (Max.) @Vcc=5.5V, Ta=–25 to +85 °C
- Low voltage data retention: 2.2V (Min.)
- Fast access time: (Access time)
  CXK581100TM/YM-10LX, -10LLX 100ns (Max.)
  CXK581100TM/YM-12LX, -12LLX 120ns (Max.)
  CXK581100TM/YM-15LX, -15LLX 150ns (Max.)
- Single +5V Supply: +5V ± 10%

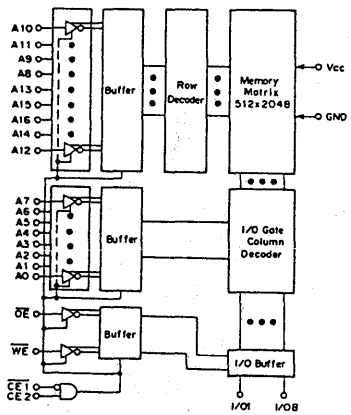
Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

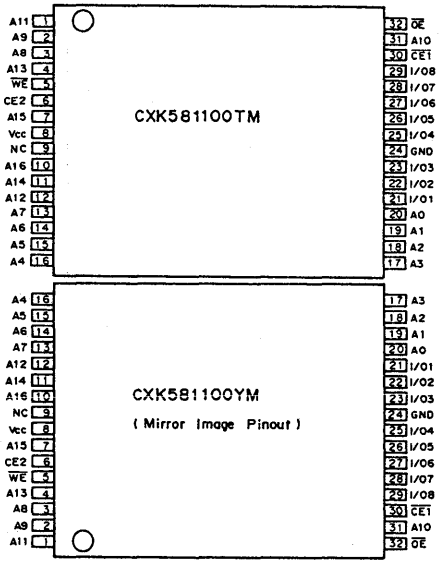
Block Diagram



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	−25 to +85	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	235 • 10	°C • sec

* V_{IN}, $V_{I/O}$=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions

(Ta=−25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.6	V

* V_{IL}=−3.0V Min. for pulse width less than 50ns.

3

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=–25 to +85°C)

Item	Symbol	Test conditions		–10LX/12LX/15LX			–10LLX/12LLX/15LLX			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–1	—	1	–1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=GND to Vcc		–1	—	1	–1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		—	7	15	—	7	15	mA
Average operating current	I_{CC2}	Cycle=Min. Duty=100%, I_{OUT}=0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I_{CC3}	Cycle time 1 µs Duty=100%, I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ Vcc–0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ Vcc–0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc–0.2V CE2 ≧ Vcc–0.2V or CE2 ≦ 0.2V	–25 to +85°C	—	—	200	—	—	40	µA
			–25 to +70°C	—	—	100	—	—	20	
			–25 to +40°C	—	—	20	—	—	4	
			+25°C	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.6	3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}=–1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

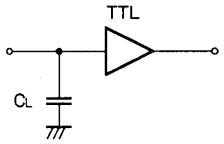
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=–25 to +85°C)

Item	Conditions
Input pulse high level	V_{IH}=2.4V
Input pulse low level	V_{IL}=0.6V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L * =100pF, 1TTL



* C_L includes scope and jig capacitances

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• Read cycle ($\overline{WE}$="H")

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

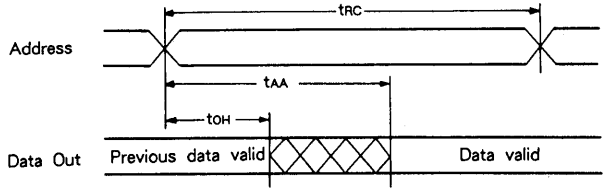
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	—	30	—	30	—	30	ns

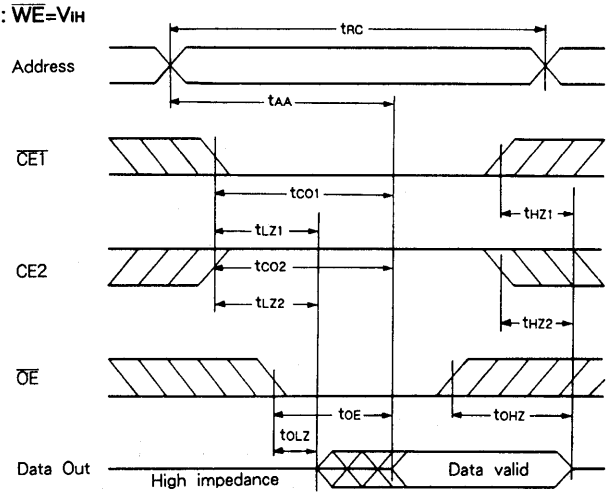
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

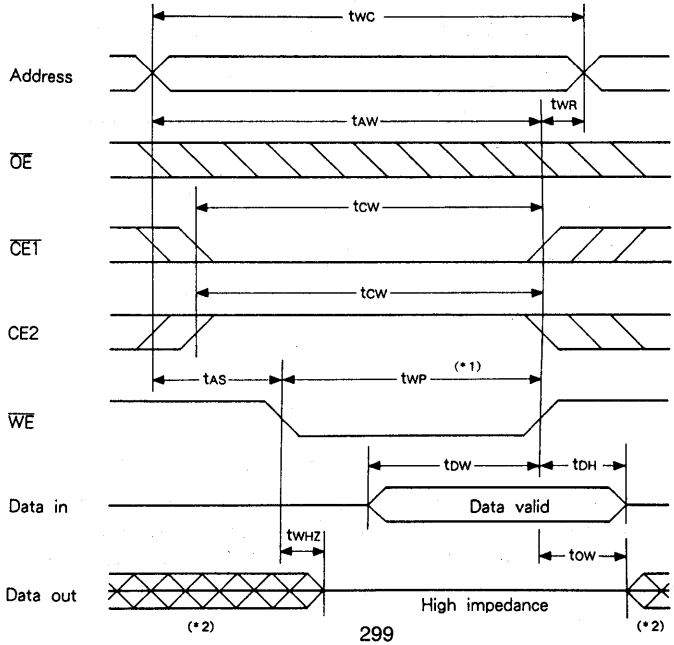
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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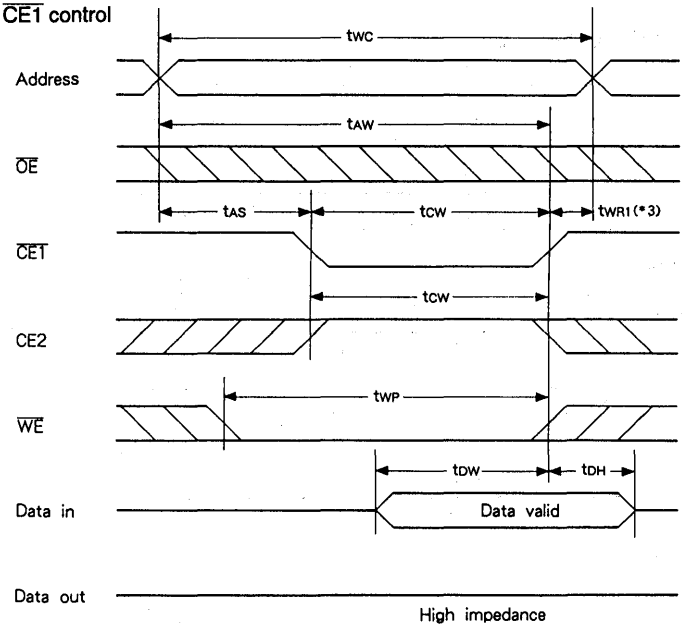
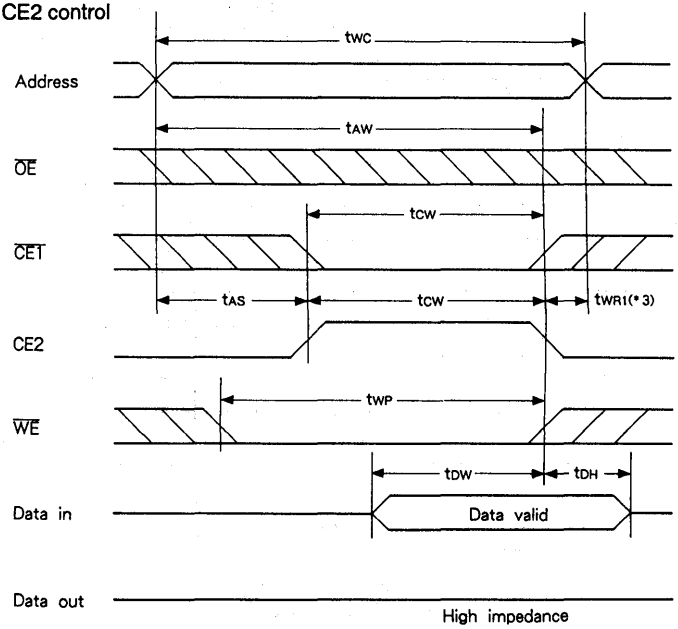
• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
*2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.
*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

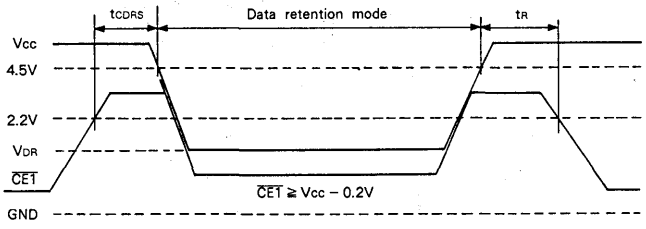
(Ta=–25 to +85 °C)

Item	Symbol	Test conditions		–10LX/12LX/15LX			–10LLX/12LLX/15LLX			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.2	—	5.5	2.2	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V*1	–25 to +85 °C	—	—	100	—	—	24	µA
			–25 to +70 °C	—	—	50	—	—	12	
			–25 to +40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	Vcc=2.2 to 5.5V*1		—	2*3	200	—	0.7*3	40	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	t_{RC}*2	—	—	ns

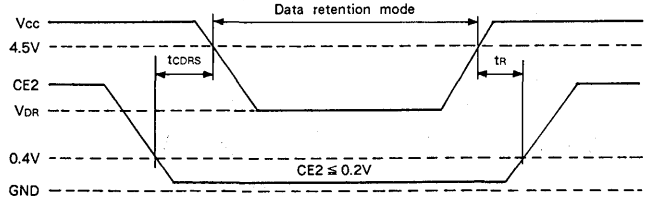
*1. $\overline{CE1} \geqq$ Vcc–0.2V, CE2 $\geqq$ Vcc–0.2V ($\overline{CE1}$ control) or CE2 $\leqq$ 0.2V (CE2 control)
*2. t_{RC}: Read cycle time
*3. Vcc=5V, Ta=25 °C

Data Retention Waveform

• Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



• Low supply voltage data retention waveform (2) : CE2 control



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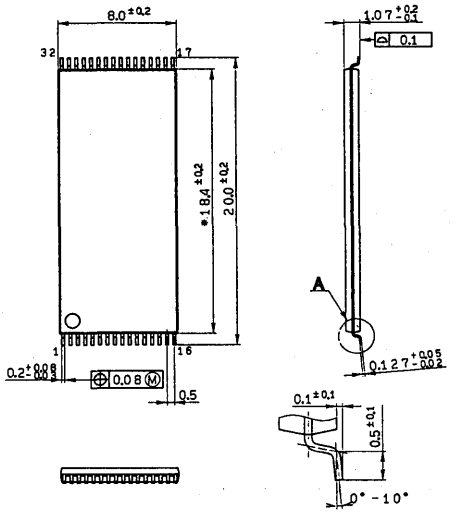
Package Outline Unit : mm

CXK581100TM

32pin TSOP (Plastic)



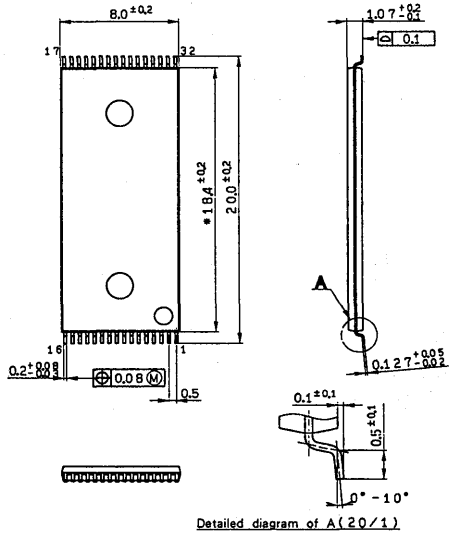
Detailed diagram of A(20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	————

CXK581100YM

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	————

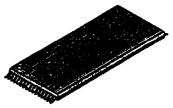
SONY CXK581100TM/YM -12LB

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to 2.7 to 5.5V power supply operation and low power consumption.

CXK581100TM
32 pin TSOP (Plastic)



CXK581100YM
32 pin TSOP (Plastic)

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Thin small-outline packages of EIAJ standard:
  CXK581100TM:
  8mm × 20mm 32 pin TSOP
  CXK581100YM:
  8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low power consumption operation:

	Standby / DC operation
3V operation;	3 μW (Typ.) / 1.2mW (Typ.)
5V operation;	10 μW (Typ.) / 35mW (Typ.)

- Fast access time: (Access time)
  3V operation; 240ns (Max.)
  5V operation; 120ns (Max.)
- Low voltage data retention: 2.0V (Min.)

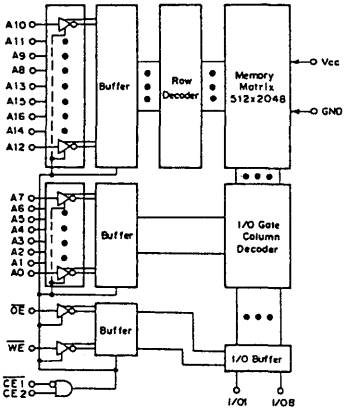
Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

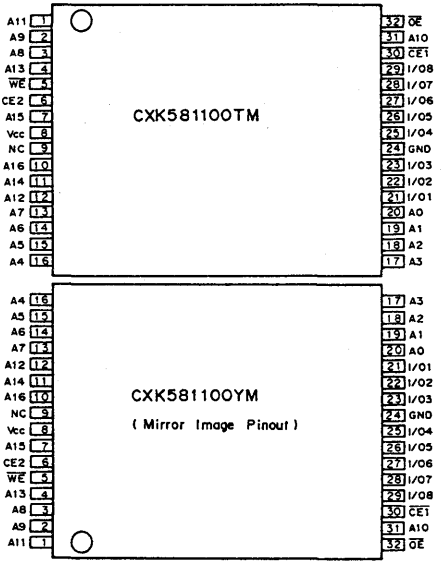
Block Diagram



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



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Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 * to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc +0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc +0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C
Soldering temperature • time	Tsolder	235 • 10	°C • sec

* V_{IN}, $V_{I/O}$=−3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

×: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Vcc=5V ± 10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	−0.3 *	—	0.4	V

* V_{IL}=−3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		−1	—	1	−1	—	1	µA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		−1	—	1	−1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA		—	0.4	0.8	—	7	15	mA
Average operating current	I_{CC2}	Min. cycle Duty=100% I_{OUT}=0mA	Write cycle	—	10	15	—	35	60	mA
			Read cycle	—	10	15	—	25	40	
	I_{CC3}	Cycle time 1 µs Duty=100% I_{OUT}=0mA $\overline{CE1}$ ≦ 0.2V, CE2 ≧ Vcc−0.2V V_{IL} ≦ 0.2V, V_{IH} ≧ Vcc−0.2V	Write cycle	—	5	10	—	10	20	mA
			Read cycle	—	2.5	5	—	5	10	
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc−0.2V CE2 ≧ Vcc−0.2V	0 to +70°C	—	—	60	—	—	100	µA
			0 to +40°C	—	—	12	—	—	20	
			+25°C	—	1.2	5	—	2	8	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	0.06	0.3	—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	8	pF

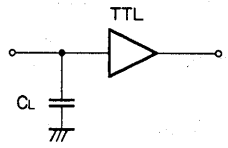
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions

(Vcc=2.7 to 5.5V, Ta=0 to +70°C)

Item	Conditions	
	Vcc=3V	Vcc=5V
Input pulse high level	V_{IH}=2.2V	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.4V	V_{IL}=0.8V
Input rise time	tr=5ns	tr=5ns
Input fall time	tf=5ns	tf=5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C_L*=100pF, 1TTL	C_L*=100pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE}$="H")

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	240	—	120	—	ns
Address access time	t_{AA}	—	240	—	120	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	240	—	120	ns
Chip enable access time (CE2)	t_{CO2}	—	240	—	120	ns
Output enable to output valid	t_{OE}	—	120	—	60	ns
Output hold from address change	t_{OH}	30	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	20	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	10	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1} *, t_{HZ2} *	—	80	—	40	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	80	—	40	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	240	—	120	—	ns
Address valid to end of write	t_{AW}	170	—	85	—	ns
Chip enable to end of write	t_{CW}	170	—	85	—	ns
Data to write time overlap	t_{DW}	100	—	50	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	160	—	80	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}	20	—	10	—	ns
Write to output in high Z	t_{WHZ} *	—	60	—	30	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

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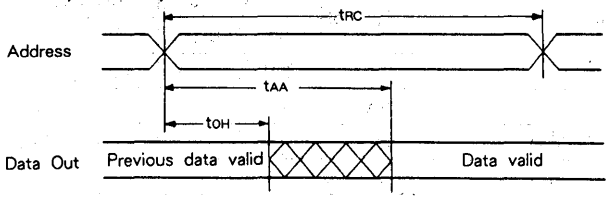
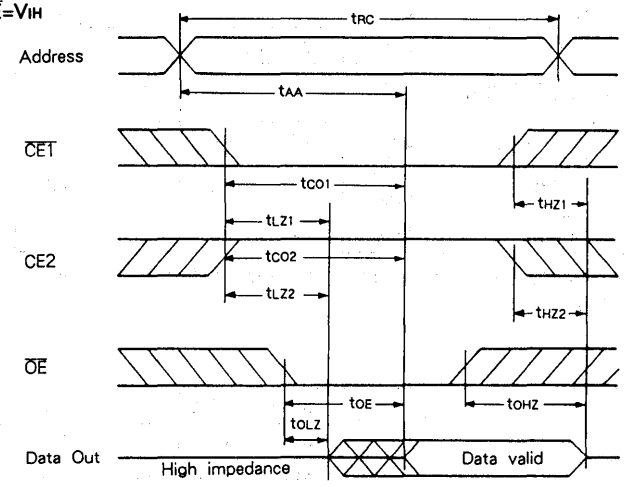
Timing Waveform

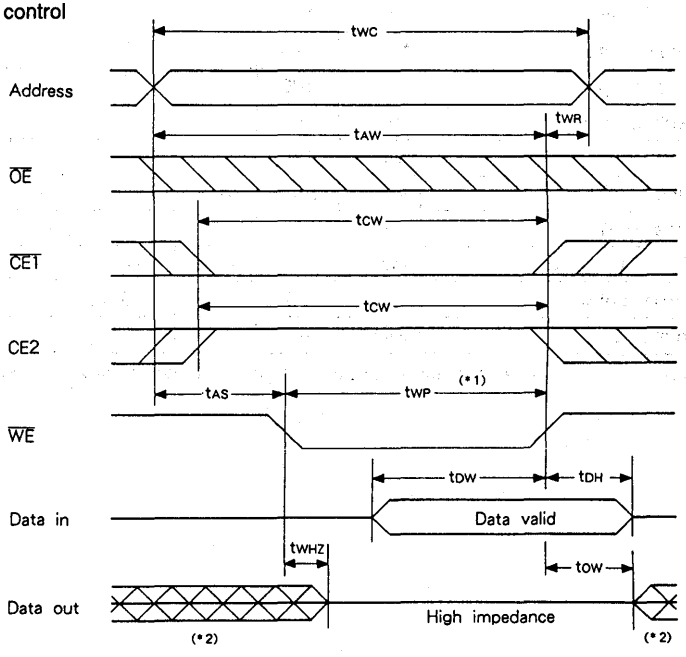
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



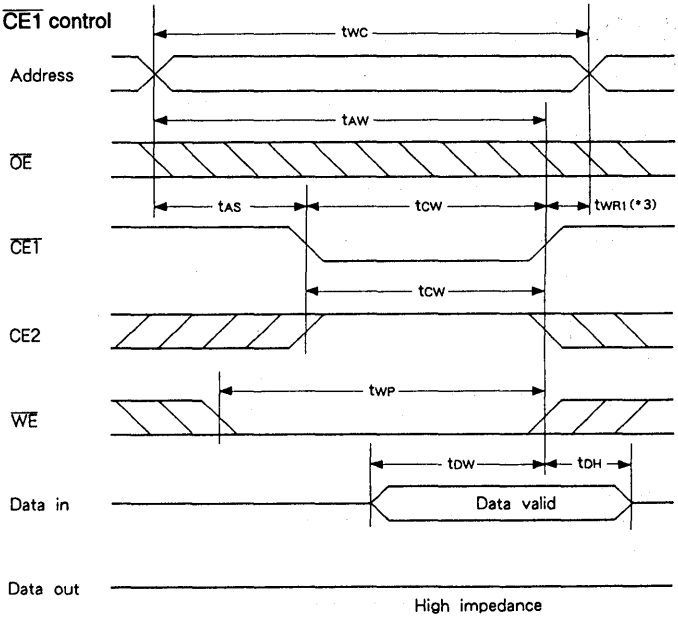
• Read cycle (2) : $\overline{WE}$=V_{IH}



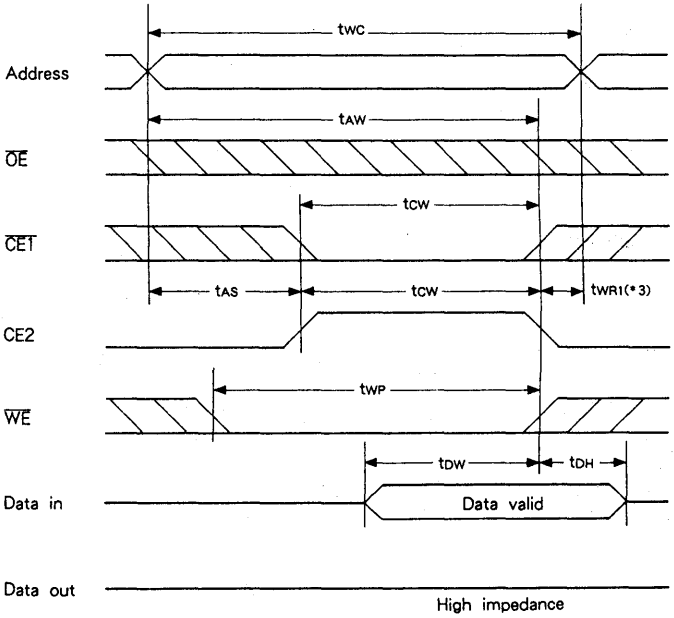
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
*2. Do not apply the data input valtage of the opposite phase to the output while I/O pin is in output condition.
*3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to +70°C)

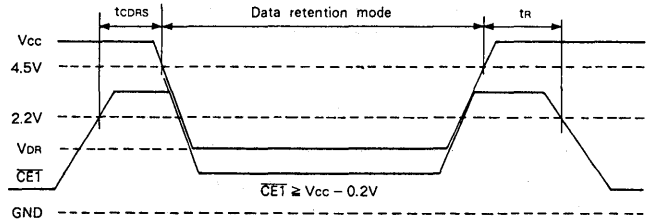
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V*1	0 to +70°C	—	—	50	μA
			0 to +40°C	—	—	10	
			+25°C	—	1	4	
	I_{CCDR2}	Vcc=2.0 to 5.5V*1		—	2	100	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			t_{RC}*2	—	—	ns

*1. $\overline{CE1} \geqq V_{CC}-0.2V$, $CE2 \geqq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)

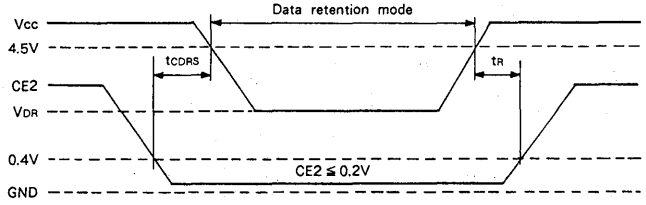
*2. t_{RC} : Read cycle time

Data Retention Waveform

• Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

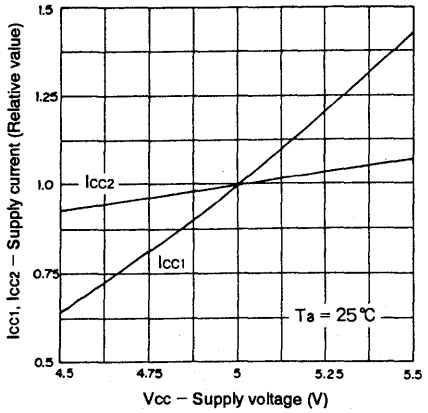


• Low supply voltage data retention waveform (2) : CE2 control

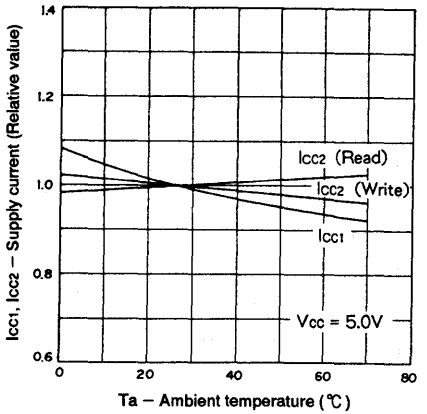


Example of Representative Characteristics

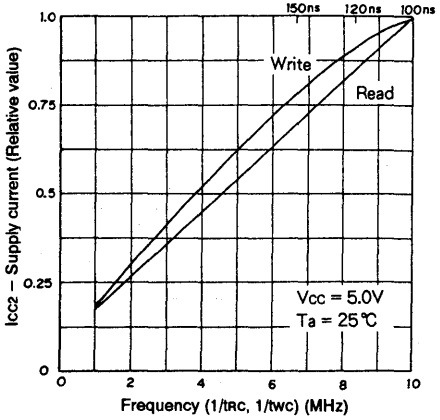
Supply current vs. Supply voltage



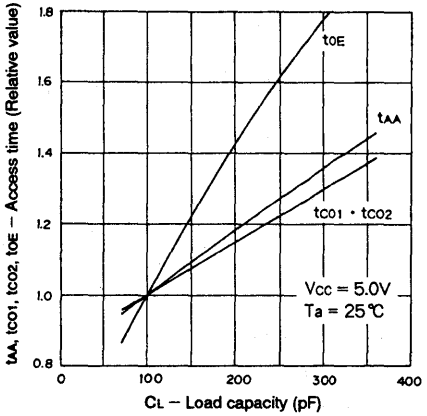
Supply current vs. Ambient temperature



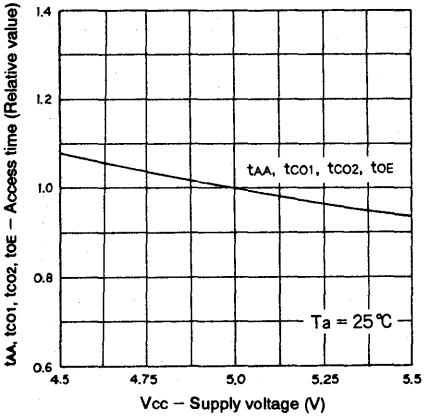
Supply current vs. Frequency



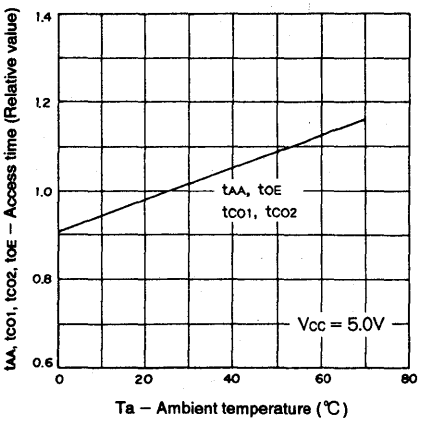
Access time vs. Load capacity



Access time vs. Supply voltage

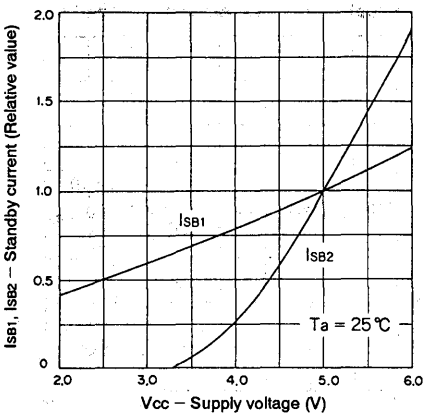


Access time vs. Ambient temperature

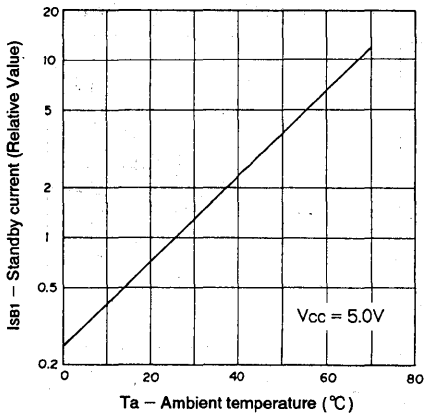


3

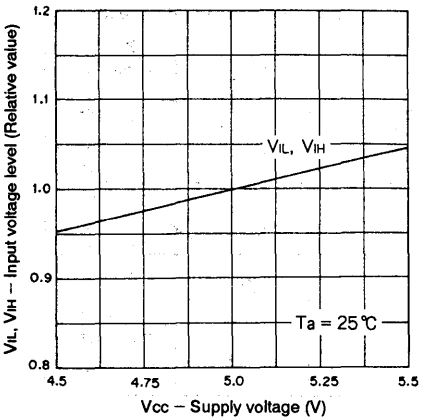
Standby current vs. Supply voltage



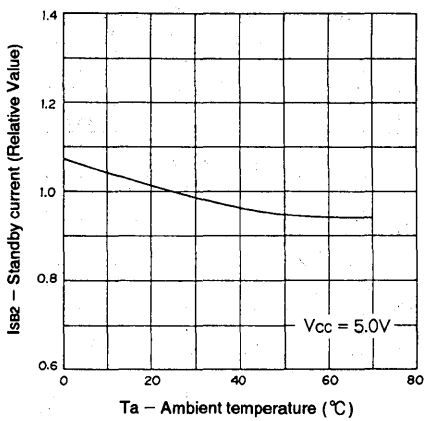
Standby current vs. Ambient temperature



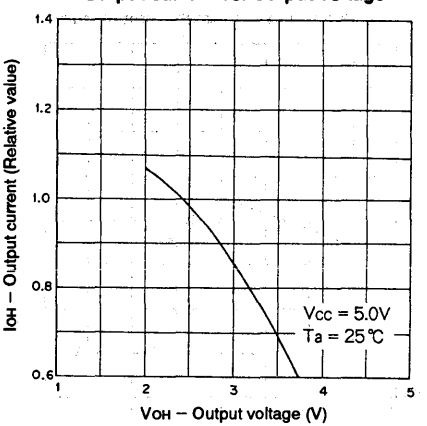
Input voltage level vs. Supply voltage



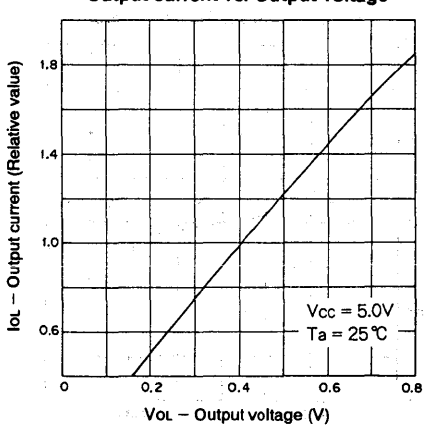
Standby current vs. Ambient temperature



Output current vs. Output voltage

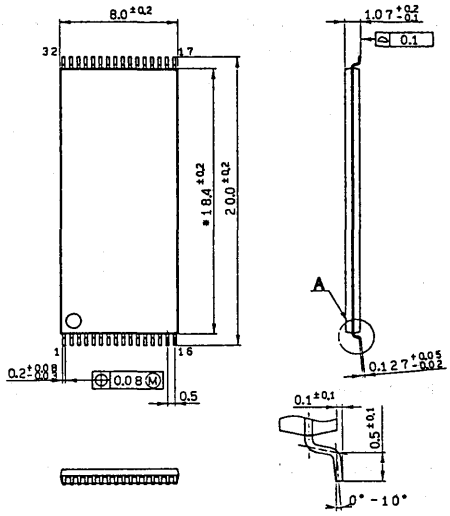


Output current vs. Output voltage



Package Outline Unit : mm

CXK581100TM 32pin TSOP (Plastic)

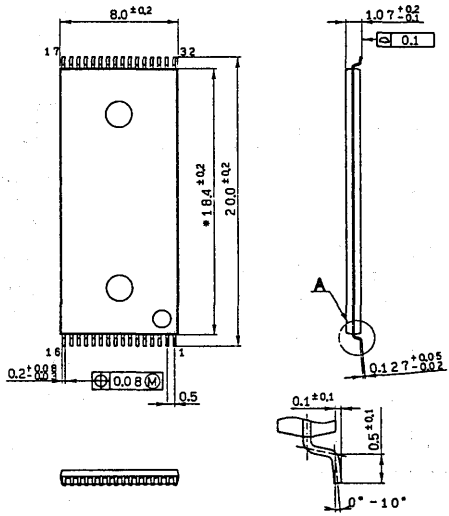


Detailed diagram of A (20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	————

CXK581100YM 32pin TSOP (Plastic)



Detailed diagram of A (20/1)

Note) Dimensions marked with * does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	————

SONY CXK541000J -25/30/35

262144-word × 4-bit High Speed CMOS Static RAM *Preliminary*

Description

CXK541000J is a 1048576 bits high speed CMOS static RAM organized as 262144 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

32 pin SOJ (Plastic)

Features

- Fast access time (Access time)
  - CXK541000J-25 25ns (Max.)
  - CXK541000J-30 30ns (Max.)
  - CXK541000J-35 35ns (Max.)
- Low power consumption (operation) : 350mW (Typ.)
- Single +5V power supply: 5V ± 10%
- Fully static memory ····· No clock or timing strobe required.
- Equal access and cycle time.
- Separated data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- High density: 400 mil 32 pin SOJ plastic package

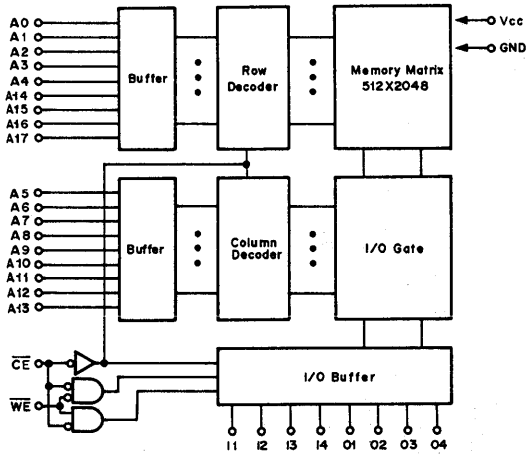
Function

262144-word × 4-bit static RAM

Structure

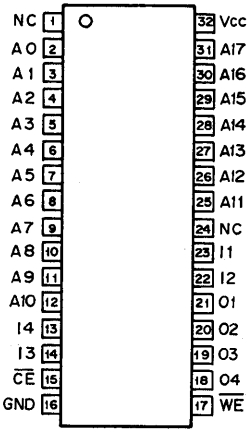
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
I1 to I4	Data input
O1 to O4	Data output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 * to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	−10 to +85	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature•time	Tsolder	260•10	℃•sec

* V_{CC}, V_{IN}, $V_{I/O}$=+7.5V Max. for pulse width less than10ns.
V_{CC}, V_{IN}, $V_{I/O}$=−3.5V Min. for pulse width less than10ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	Data Output	Vcc Current
H	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	I_{CC}
L	L	Write	High Z	I_{CC}

×: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.5	V
Input low voltage	V_{IL}	−0.5 *	—	0.8	V
Input rise time	tr	—	5	100	ns
Input fall time	tf	—	5	100	ns

* V_{IH}=+7.0V Max. for pulse width less than 10ns.
V_{IL}=−3.0V Min. for pulse width less than 10ns.

3

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leak current	I_{LI}	V_{IN}=GND to Vcc Vcc=5.5V	−1	—	1	μA
Output leak current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=GND to Vcc	−1	—	1	μA
Average operating current	I_{CC}	Cycle=Min, Duty=100% I_{OUT}=0mA	—	70	120	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc−0.2V, V_{IN} ≧ Vcc−0.2V or V_{IN} ≦ 0.2V	—	—	2	mA
	I_{SB2}	$\overline{CE}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, min. cycle	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Output capacitance	C_{OUT}	V_{OUT}=0V	—	10	pF

Note) This parameter is sampled and is not 100% tested.

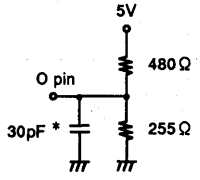
AC characteristics

• AC test conditions

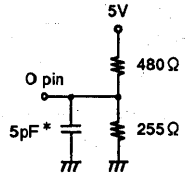
(Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, tow, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	15	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	25	—	30	—	35	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

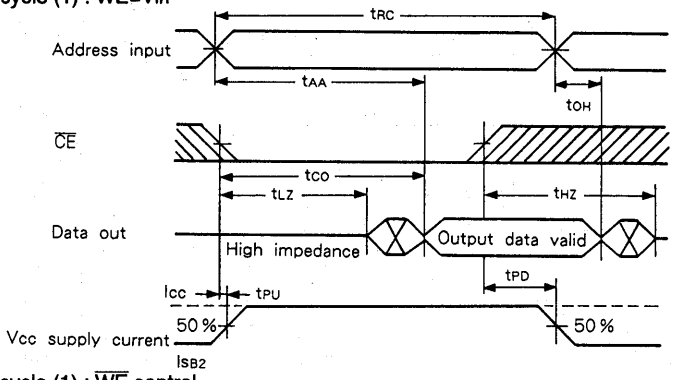
• Write cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	18	—	20	—	20	—	ns
Chip enable to end of write	t_{CW}	18	—	20	—	20	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	18	—	18	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	2	—	2	—	2	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	15	0	15	0	15	ns

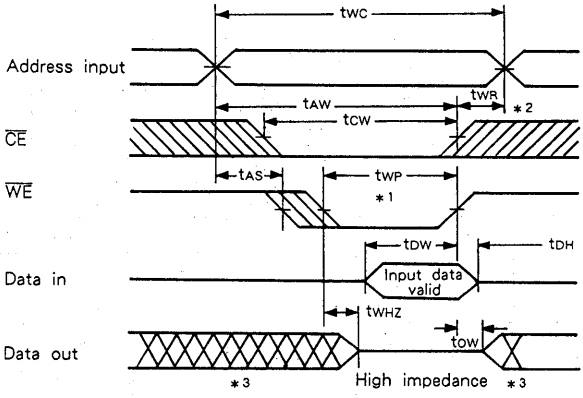
* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

Timing Waveform

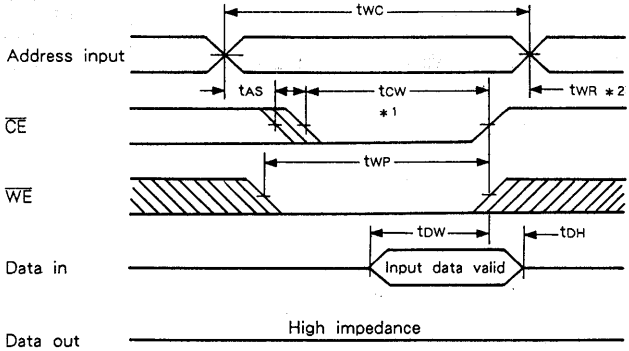
• Read cycle (1) : $\overline{WE}$=VIH



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



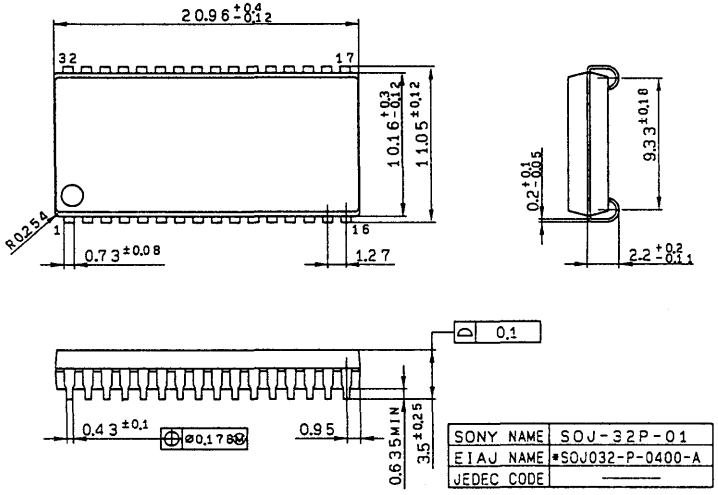
*1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.

*2. tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

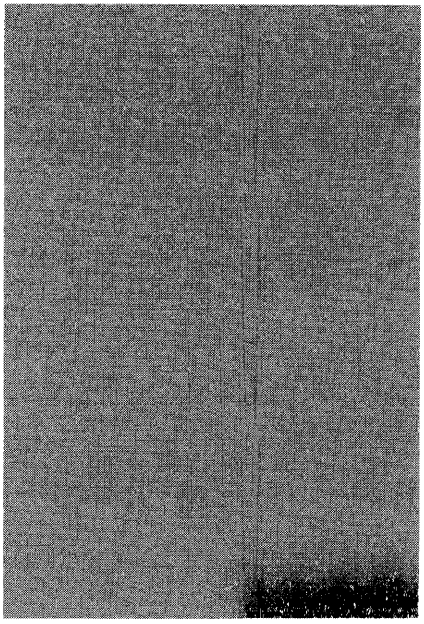
Package Outline Unit : mm

32pin SOJ (Plastic) 400mil 1.3g

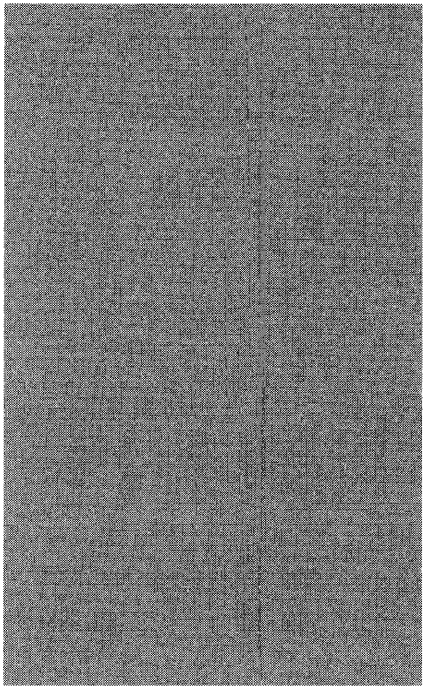


SONY NAME	SOJ-32P-01
EIAJ NAME	*SOJ032-P-0400-A
JEDEC CODE	———

3



ASM (Application Specific Memory)



2) ASM (Application Specific Memory)

Type	Function	Process	Page
CXK7701J	8,192 word x 16bits, 30/35/45ns SRAM	MIX CMOS	324
CXK77910J	131,072 word x 9 bits, 17/20ns SRAM (Synchronous)	MIX CMOS	339

SONY®

CXK7701J -30/35/45

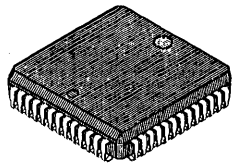
High-Speed Latched Cache-SRAM

Description

The CXK7701J is a 131,072-bit high speed latched Cache-SRAM suitable for use in high speed cache configurations and low power applications.

Organized as 8192 word × 16-bit or 4096 word × 16-bit × 2 WAY selected by mode control pin, it operates from a single 5V supply.

52 pin PLCC (Plastic)



Features

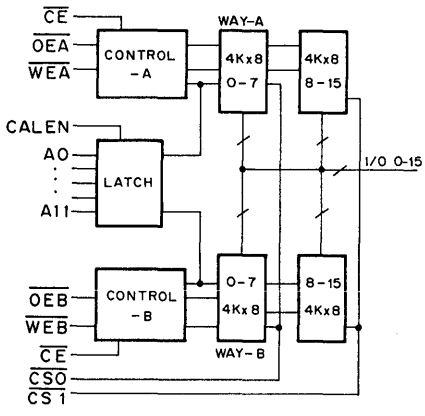
- Best fit for Cache configurations
  Intel 82385 Cache Controller (for 80386-33 MHz, 25MHz, 20MHz)
- Fast access time : (Access time)
  CXK7701J-30 30ns (Max.)
  CXK7701J-35 35ns (Max.)
  CXK7701J-45 45ns (Max.)
- Fast output Enable
  CXK7701J-30 10ns (Max.)
  CXK7701J-35 13ns (Max.)
  CXK7701J-45 16ns (Max.)
- Available in 52 pin PLCC
- Internal 12-bit address latch (A0 – A11)
- Directly TTL compatible : All inputs and outputs

Structure

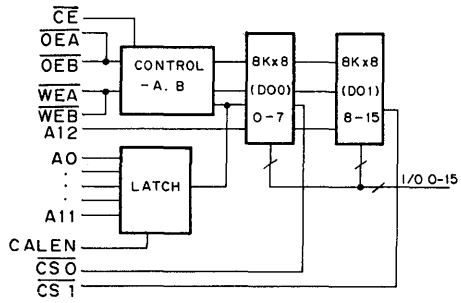
Silicon gate CMOS IC

Block Diagram

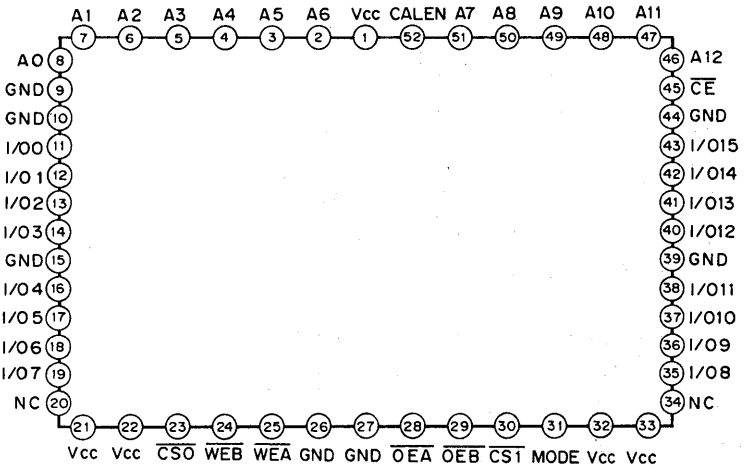
• 2 WAY SET ASSOCIATIVE (MODE = "High")



• DIRECT MAP (MODE = "Low")



Pin Configuration



Pin Description

Symbol	Description
A0 to A12	Address Input
I/O0 to I/O15	Data Input Output
$\overline{CE}$	Global Chip Enable Input
$\overline{CS0}$, $\overline{CS1}$	Chip Enable Input for I/O 0 – 7, I/O 8 – 15
$\overline{OEA}$, $\overline{OEB}$	Output Enable Input for Bank-A, Bank-B
$\overline{WEA}$, $\overline{WEB}$	Write Enable Input for Bank-A, Bank-B
CALEN	Address Latch Enable Input
MODE	Mode Control
Vcc	+5V Power Supply
GND	Ground
NC	No Connection

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	− 0.5 * to + 7.0	V
Input Voltage	V_{IN}	− 0.5 * to Vcc + 0.5	V
Input & Output Voltage	$V_{I/O}$	− 0.5 * to Vcc + 0.5	V
Power Dissipation	P_D	2.5	W
Operating Temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering Temperature	Tsolder	260 • 10	℃ • sec

***Note**) Vcc, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V_{IL}	− 0.3 *	—	0.8	V

***Note**) V_{IL} = − 3.0V Min. for pulse width less than 20ns.

DC and Operating Characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to + 70℃)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = GND to Vcc	− 2	2	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = GND to Vcc, $\overline{CE}$ = V_{IH} or $\overline{CS0}$, $\overline{CS1}$ = V_{IH} or $\overline{OEA}$, $\overline{OEB}$ = V_{IH} or $\overline{WEA}$, $\overline{WEB}$ = V_{IL}	− 2	2	μA
Operating Supply Current	I_{CC1}	$\overline{CS0}$, $\overline{CS1}$ & $\overline{CE}$ = V_{IL} V_{IN} = V_{IL} or V_{IH} I_{OUT} = 0mA	—	180	mA
Average Operating Current	I_{CC2}	100% Duty Cycle V_{IN} = GND to Vcc I_{OUT} = 0mA	—	240	mA
	I_{CC3}	50% Duty Cycle V_{IN} = GND to Vcc I_{OUT} = 0mA	—	220	mA
Output High Voltage	V_{OH}	I_{OH} = − 1.0mA	2.4	—	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA	—	0.4	V

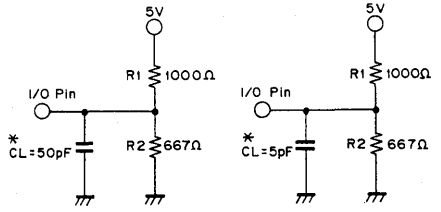
A. C. Test Condition (Applies to Read & Write Cycle Timing)

(Vcc = 5V ± 10%, Ta = 0 to +70℃)

Item		Conditions	Unit
Input Pulse High Level		V_{IH} = 3.0	V
Input Pulse Low Level		V_{IL} = 0.0	V
Input Rise Time		tr = 3	ns
Input Fall Time		tf = 3	ns
Input and Output Reference Level		1.5	V
Output Load (See Test Circuit Fig-1)	R1	1000	Ω
	R2	667	Ω
	C_L	50	pF

Fig-1

Output Load (1) Output Load (2) **



* Including scope and jig capacitance

** For t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{WLZ}, t_{WHZ}

Truth Tables

Two-Way Mode (Mode = High)

$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	Operation	
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled	
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled	
X	X	X	H	H	X	X	Outputs High-Z	
X	X	X	L	L	X	X	Outputs High-Z	
L	L	H	L	H	H	H	Read I/O 0 – 7	Way A
L	L	H	H	L	H	H	Read I/O 0 – 7	Way B
L	H	L	L	H	H	H	Read I/O 8 – 15	Way A
L	H	L	H	L	H	H	Read I/O 8 – 15	Way B
L	L	L	L	H	H	H	Read I/O 0 – 15	Way A
L	L	L	H	L	H	H	Read I/O 0 – 15	Way B
L	L	H	X	X	L	H	Write I/O 0 – 7	Way A
L	L	H	X	X	H	L	Write I/O 0 – 7	Way B
L	H	L	X	X	L	H	Write I/O 8 – 15	Way A
L	H	L	X	X	H	L	Write I/O 8 – 15	Way B
L	L	L	X	X	L	H	Write I/O 0 – 15	Way A
L	L	L	X	X	H	L	Write I/O 0 – 15	Way B
L	L	H	X	X	L	L	Write I/O 0 – 7	Way A & B
L	H	L	X	X	L	L	Write I/O 8 – 15	Way A & B
L	L	L	X	X	L	L	Write I/O 0 – 15	Way A & B

Note) X : "H" or "L"

4

Truth Tables

Direct Mode (Mode = Low)

$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O 0 – 7
L	H	L	L	L	H	H	Read I/O 8 – 15
L	L	L	L	L	H	H	Read I/O 0 – 15
L	L	H	X	X	L	L	Write I/O 0 – 7
L	H	L	X	X	L	L	Write I/O 8 – 15
L	L	L	X	X	L	L	Write I/O 0 – 15

Note) X : "H" or "L"

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	9	pF

Note) This parameter is sampled and is not 100% tested.

• Write Cycle Timing (Vcc = 5V ± 10 %)

Item	Symbol	−30		−35		−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	30	—	35	—	45	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	35	—	ns
A12 Valid to End of Write	t_{A12W}	18	—	22	—	30	—	ns
Chip Select to End of Write	t_{CW}	18	—	22	—	30	—	ns
Data Valid to End of Write	t_{DW}	10	—	12	—	15	—	ns
Data Hold from End of Write	t_{DH}	0	—	0	—	0	—	ns
Write Enable Active to High-Z	t_{WHZ}*	—	15	—	15	—	20	ns
WRITE Enable Inactive to Low-Z	t_{WLZ}*	3	—	3	—	3	—	ns
Write Pulse Width	t_{WP}	18	—	22	—	30	—	ns
$\overline{CE}$ Pulse Width During Chip Enable Controlled Write	t_{CP}	18	—	22	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	2	—	ns
Address Latch Enable Pulse Width	t_{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t_{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and is not 100 % tested.

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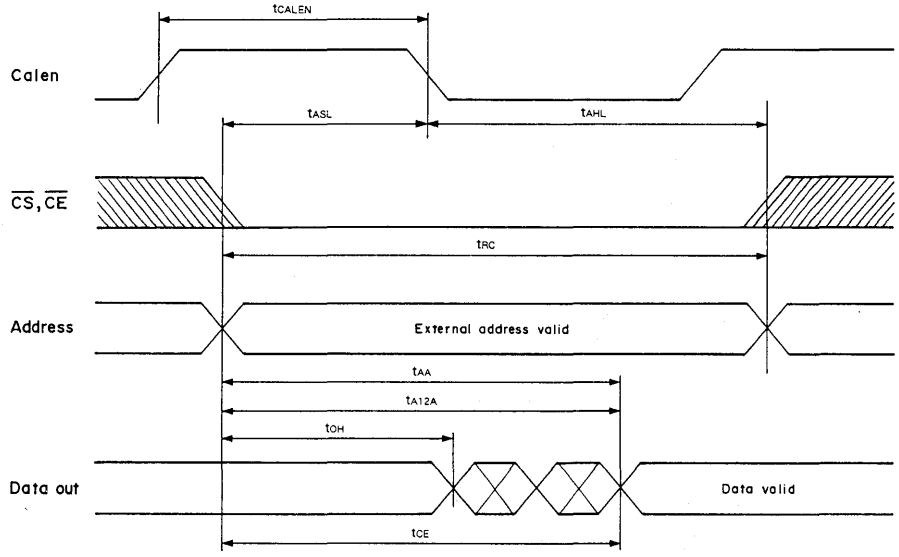
• **Read Cycle Timing** (Vcc = 5V ± 10%)

Item	Symbol	−30		−35		−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	30	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	30	—	35	—	45	ns
A12 Address Access Time	t_{A12A}	—	17	—	25	—	30	ns
Chip Select Access Time	t_{CS} t_{CE}	—	20	—	25	—	35	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	16	ns
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	t_{LZ}*	3	—	3	—	3	—	ns
Output Enable to Output Low-Z	t_{OLZ}*	2	—	2	—	2	—	ns
Chip Deselect to Output High-Z	t_{HZ}*	—	15	—	25	—	30	ns
Output Disable to Output High-Z	t_{OHZ}*	—	10	—	14	—	14	ns
Address Latch Enable Pulse Width	t_{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t_{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	ns

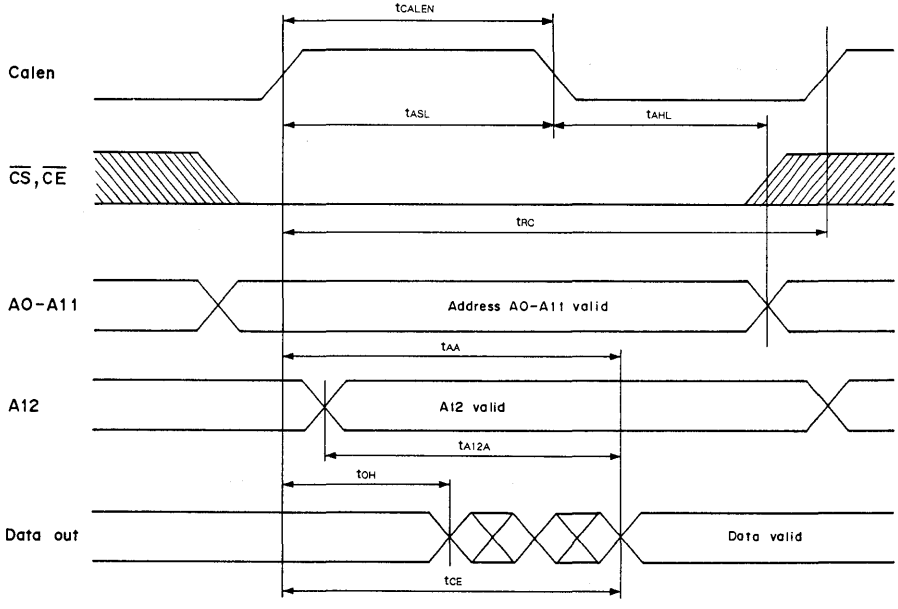
* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and is not 100% tested.

Timing Waveform

• Read cycle (1) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



• Read cycle (2) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



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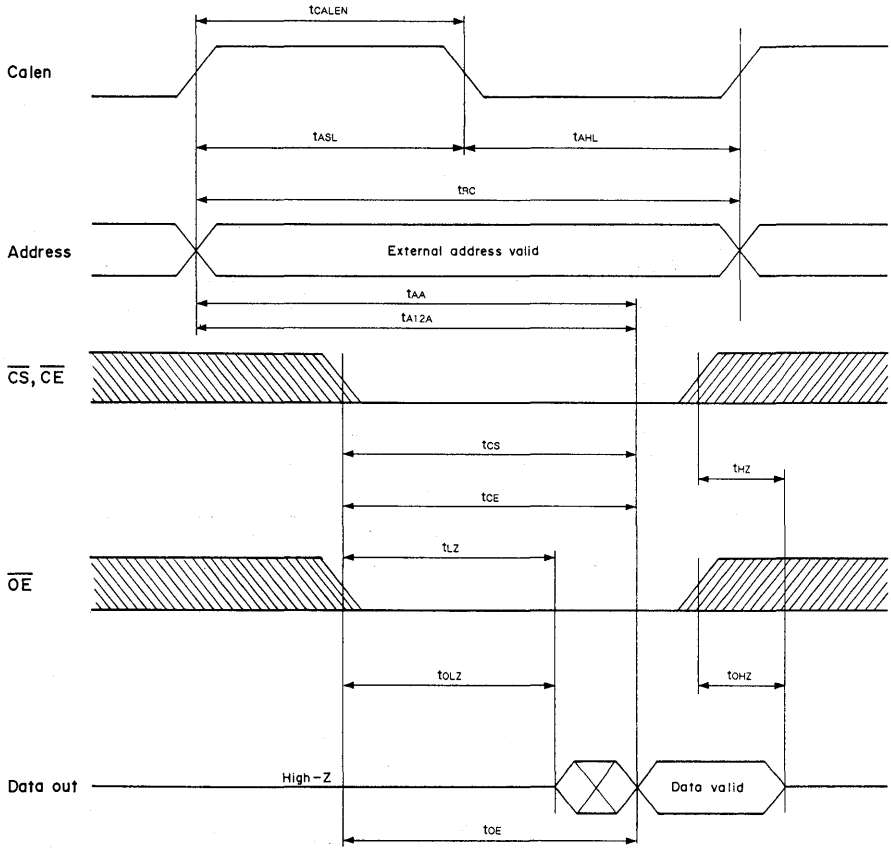
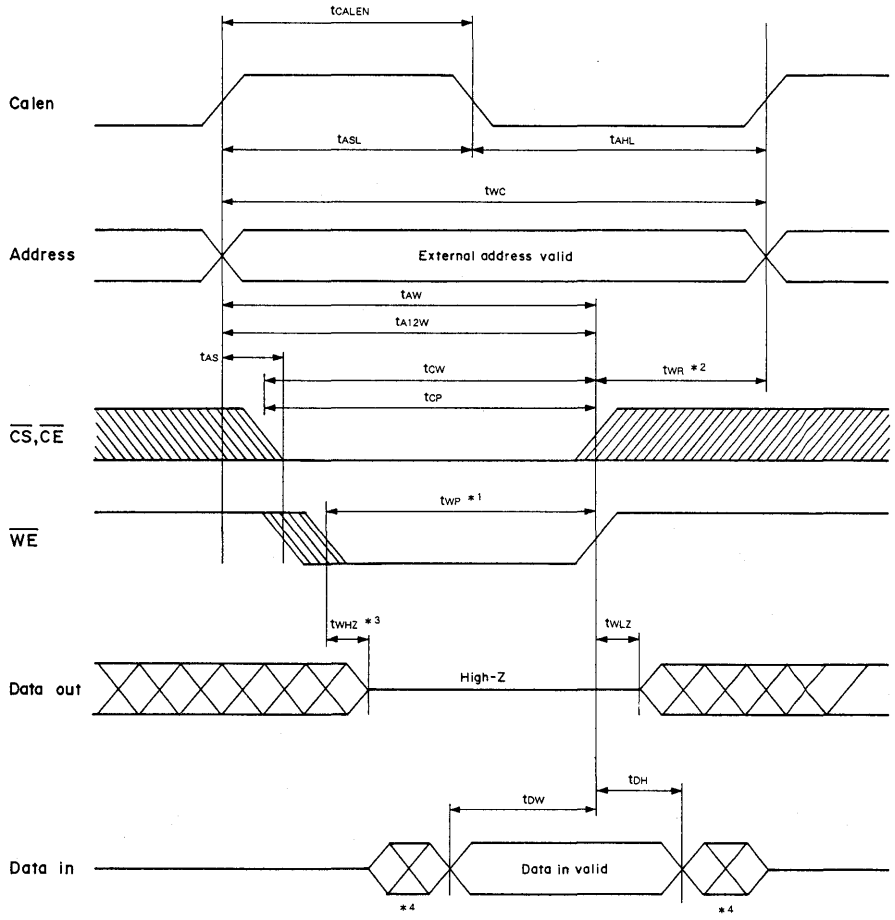
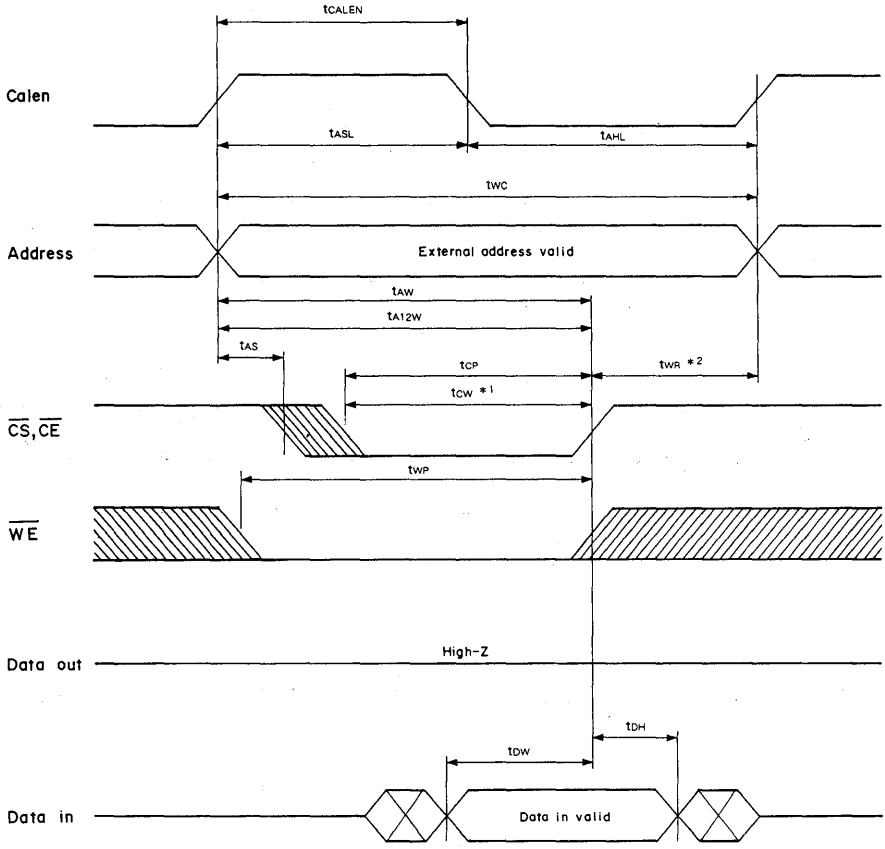
• Read cycle (3) : $\overline{WE}$ = V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



*1. A write occurs during the low overlap of $\overline{CS}$, $\overline{CE}$ and $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
*3. If $\overline{CE}$ and $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
*4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Control Pin Description

CALEN (Cache Address Latch Enable)

This signal controls the internal address latch that resides between the address inputs and the memory array. When CALEN is high the latch is transparent. The falling edge of CALEN latches the current address inputs.

MODE

This signal controls whether the memory device is to be used in a direct mapped (8k × 16) configuration or a two-way set associative (2-4k × 16) configuration. When the mode signal is high, the device is placed in two-way mode. When the mode pin is low, the device is placed in direct mode.

$\overline{CS0}$, $\overline{CS1}$ (Cache Chip Selects)

These active low signals tie to the cache ram chip selects and individually enable the two bytes of the memory. $\overline{CS0}$ enables bits I/O0 – I/O7 and, $\overline{CS1}$ enables bits I/O8 – I/O15.

$\overline{CE}$ (Cache Chip Enable)

This active low signal, when active, enable writes to the data ram or reads from the data ram. It is a global signal, and controls both cache bank A and cache bank B. It's function is the same in both the set associative mode and the direct mapped mode. This input also functions as a chip enable controlled write.

$\overline{OEA}$, $\overline{OEB}$ (Cache Output Enables)

In two-way mode, these active low signals enable cache bank A or B to drive the data bus. Either $\overline{OEA}$ or $\overline{OEB}$ is active during a read hit, depending on which bank is selected. Activation of $\overline{OEA}$ simultaneous with $\overline{OEB}$ will cause both banks ot become deselected. In direct mode, these inputs will be externally wired together and A12 will determine which 4K × 16 memory bank is enabled.

$\overline{WEA}$, $\overline{WEB}$ (Cache Write Enables)

In two-way mode, these active low signals enable cache bank A or B to receive data from the data bus. Either $\overline{WEA}$ or $\overline{WEB}$ is enabled in a read miss update or write hit. In direct mode, these inputs will be externally wired together and A12 will determine which 4K × 16 memory bank will be enabled for writing.

A0 – A11 (Addresses)

The address input provide the address into the SRAM array. These signals are latched on the trailing edge of CALEN.

A12 (Address)

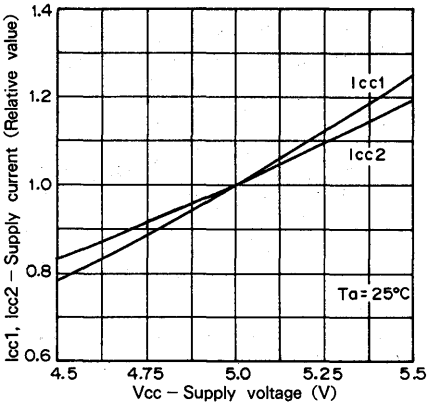
In two-way mode, the upper address input A12 will be a "don't care" and will be externally wired to ground.

In direct mode, A12 will determine which 4K × 16 memory bank is enabled by $\overline{WEA}$ and $\overline{WEB}$, and $\overline{OEA}$ and $\overline{OEB}$.

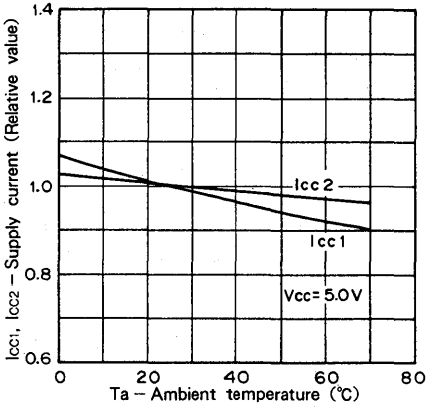
Unlike the other address lines, A12 is not latched.

Example of Representative Characteristics

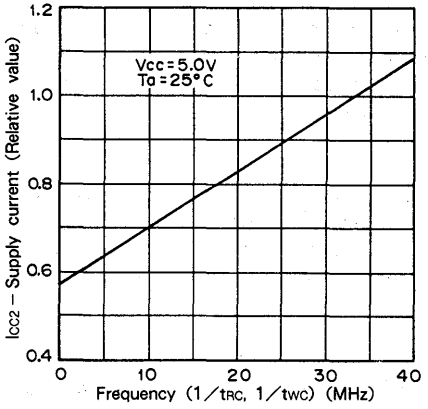
Supply current vs. Supply voltage



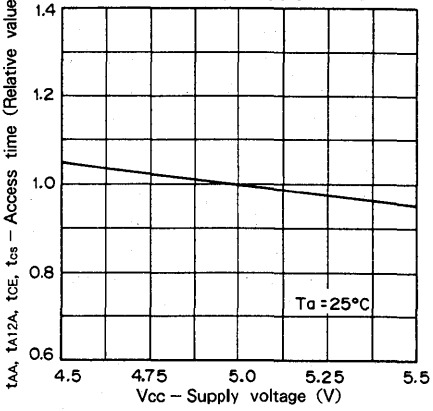
Supply current vs. Ambient temperature



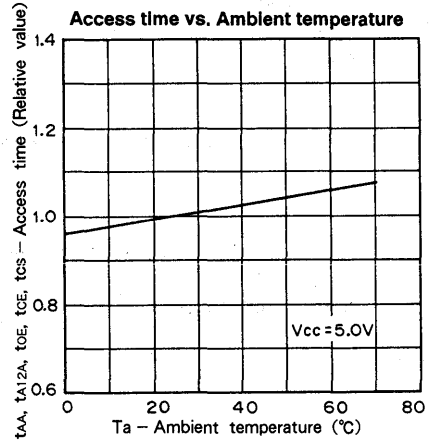
Supply current vs. Frequency



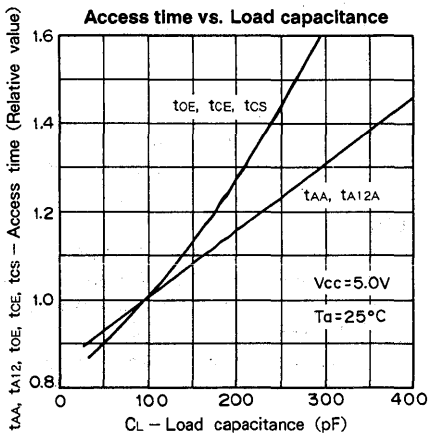
Access time vs. Supply voltage



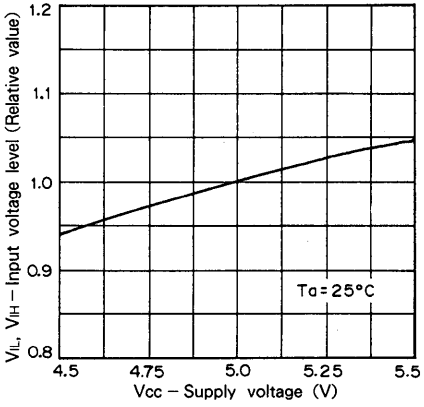
Access time vs. Ambient temperature



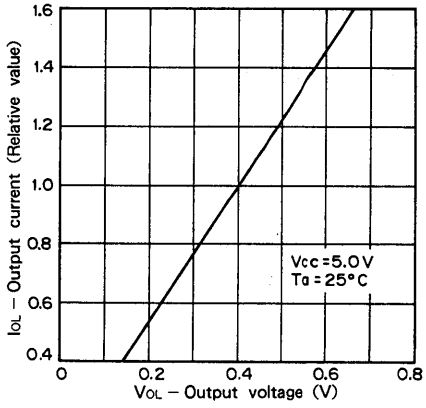
Access time vs. Load capacitance



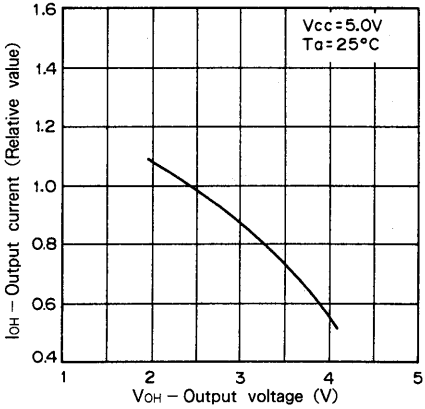
Input voltage level vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



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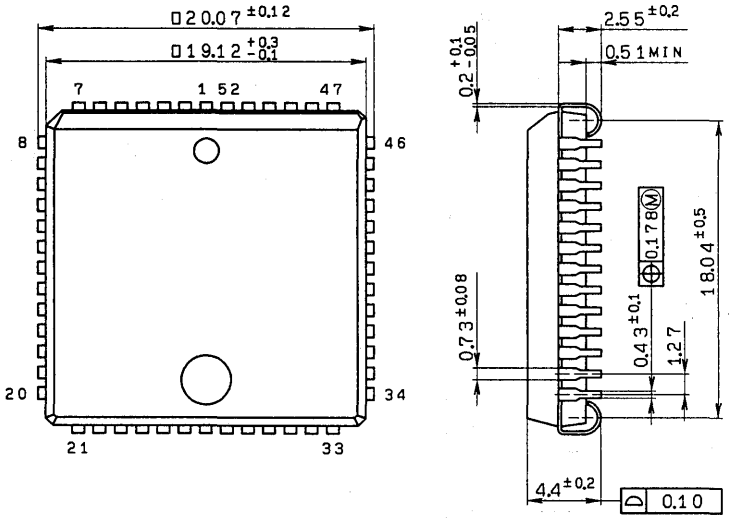
Package Outline Unit : mm

52 pin PLCC (Plastic)



SONY NAME	PLCC-52P-01
EIAJ NAME	*QFJ052-P-S750-A
JEDEC CODE	MO-047-AD

131072 words × 9-bit Self-Timed Static Random Access Memory *Preliminary*

Description

The CXK77910J is a 1,179,648 bit Self-Timed Static Random Access Memory organized as 128K words by 9 bits. This STRAM integrates Input Registers, High Speed SRAM and Output Registers onto a single monolithic circuit. All Registers are triggered with the positive edge of an external clock (CLK). At the positive edge of CLK, the RAM data of the previous CLK cycle is presented. Write operation is initiated by the positive edge of CLK and internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Function

There are three possible user transactions with the STRAM. (Read operation, write operation and deselect operation.)

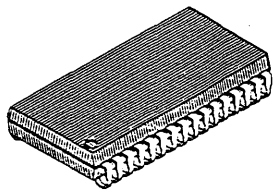
The read operation requires $\overline{WE}$="HIGH" and $\overline{OE}$=$\overline{CE}$="low" on the positive edge of CLK.
The memory location pointed to by the contents of the Address registers is read internally and the contents of the location are captured in the Data-out registers on the next positive edge of CLK. The state of Data-out will reflect the contents of the Data-out registers.

The write operation requires $\overline{CE}$=$\overline{WE}$="LOW" on the positive edge of CLK. The memory location pointed to by the contents of the Address registers is written with the contents of the Data-in registers. The write operation is entirely self-timed, eliminating critical timing edges.

The deselect cycle requires $\overline{CE}$="HIGH" or $\overline{OE}$=$\overline{WE}$="HIGH" on the positive edge of CLK. Write operation and internal read operation are disabled during the clock cycle. The data outputs are forced to a high impedance state during the next clock cycle. During the deselect cycle by $\overline{CE}$="HIGH", STRAM turns to power down mode.

The write cycle needs three preceding deselect cycles since the data for the write cycle must be supplied to I/O terminals during high impedance state. But immediately after power-on of the STRAM, the write operation can start on the first positive edge of CLK since the I/O terminals are initialized to be in high-impedance state.

32 pin SOJ (Plastic)



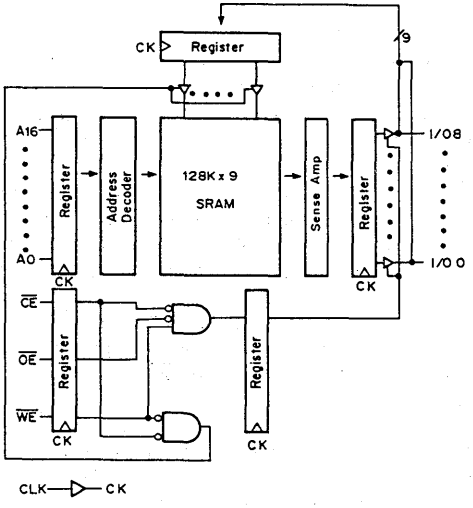
Features

- Fast Cycle Time: (Cycle) (Frequency)
  CXK77910J-17 16.6ns 60MHz
  CXK77910J-20 20.0ns 50MHz
- Fast Clock to Data Valid
  CXK77910J-17/20 10ns
- Available in Plastic 32 pin 400mil SOJ
- All inputs and outputs registered with clock
- Direct TTL compatible
- Low power consumption (min. cycle, 100% duty)
  CXK77910J-17/20 715mW (Max.)

Structure

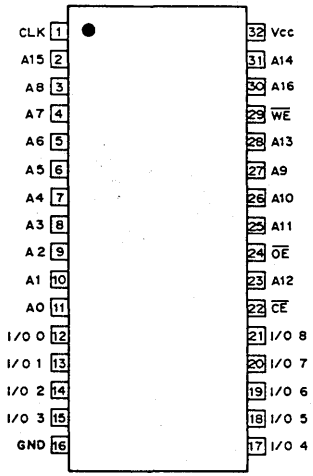
Silicon gate CMOS IC

Block Diagram



4

Pin Configuration (Top View)



Pin Description (1)

Symbol	Description
A_0 to A_{16}	Address input
I/O0 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
CLK	Clock input
Vcc	+5V power supply
GND	Ground

Pin Description (2)

CLK (Clock, positive edge triggered)
All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK with set-up and hold times referenced to that edge.
Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A0 to A16 (Address)
The Address inputs are decoded on-chip to select one of 131,072 words.
The state of the Address inputs is registered into the Address register on the positive edge of CLK.
The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

I/O0 to 8 (I/O Common)
I/O terminals are three-state and data-input/data-output common.
The state is defined by the Control block. The data inputs for write operation must be valid during every positive edge of CLK with all set-up and hold times referenced to that edge. The data outputs are triggered by the edge of CLK and the contents in Output-Registers are presented.

$\overline{WE}$ (Synchronous Write Enable, active low)
The $\overline{WE}$ is used to indicate whether a read or write operation is to be performed. If the STRAM is selected, $\overline{WE}$ is LOW to perform a write operation. The $\overline{WE}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

$\overline{OE}$ (Synchronous Output Enable, active low)
The $\overline{OE}$ is used to indicate that a read operation is to be performed. If the STRAM is selected, the $\overline{OE}$ is LOW to perform a read operation. The $\overline{OE}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

$\overline{CE}$ (Synchronous Chip Enable, active low)
The $\overline{CE}$ is used to select the STRAM when LOW (or deselect when HIGH). When selected, the STRAM will perform a read or write operation. The state of the $\overline{CE}$ is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to Vcc +0.5	V
Input and output voltage	$V_{I/O}$	−0.5 to Vcc +0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +150	°C

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	V

* V_{IL}=−1V Min. for 3ns per cycle.

Electrical Characteristics

• DC and operating characteristics (Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=GND to Vcc	−1	1	µA
Output leakage current	I_{LO}	$V_{I/O}$=GND to Vcc, $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	−1	1	µA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	—	100	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100%, I_{OUT}=0mA	—	130	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc−0.2V V_{IN} ≧ Vcc−0.2V or V_{IN} ≦ 0.2V	—	1	mA
	I_{SB2}	$\overline{CE}$=V_{IH}, I_{OUT}=0mA Cycle=Min, Duty=100%	—	80	mA
Output high voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL}=4.0mA	—	0.4	V

4

Truth tables

CLK	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Operation
↓	H	×	×	Outputs High-Z, Write Disabled, Power Down
↓	×	H	H	Outputs High-Z, Write Disabled
↓	L	L	H	Read I/O 0 to 8
↓	L	×	L	Write I/O 0 to 8

× : "H" or "L"

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	5	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

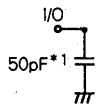
AC characteristics

• AC test conditions

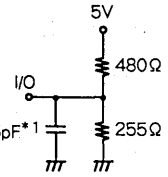
(V_{CC}=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	t_r=3ns
Input fall time	t_f=3ns
Input and output reference level	1.5V
Output load (See test circuit below)	Fig. 1

Output Load (1)



Output Load (2)*2



*1 including scope and jig capacitance
*2 for t_{CKHQZ}, t_{CKHQX2}

Fig. 1

• Read cycle

Item	Symbol	–17		–20		Unit
		Min	Max	Min	Max	
Read cycle time	t_{CKHCKH}	16.6	—	20	—	ns
Clock high pulse width	t_{CKHCKL}	5	—	5	—	ns
Clock low pulse width	t_{CKLCKH}	5	—	5	—	ns
Clock to data valid	t_{CKHQV}	—	10	—	10	ns
Address setup to clock high	t_{AVCKH}	3	—	3	—	ns
Address hold from clock high	t_{CKHAX}	0.5	—	1	—	ns
Chip enable setup to clock high	t_{CEVCKH}	3	—	3	—	ns
Chip enable hold from clock high	t_{CKHCEX}	0.5	—	1	—	ns
Output enable setup to clock high	t_{OEVCKH}	3	—	3	—	ns
Output enable hold from clock high	t_{CKHOEX}	0.5	—	1	—	ns
Output hold from clock high	t_{CKHQX1}	2	—	3	—	ns
Clock high to output low-Z	t_{CKHQX2} *	0	—	0	—	ns
Clock high to output high-Z	t_{CKHQZ} *	—	8	—	10	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

• Write cycle

Item	Symbol	–17		–20		Unit
		Min	Max	Min	Max	
Write cycle time	t_{CKHCKH}	16.6	—	20	—	ns
Clock high pulse width	t_{CKHCKL}	5	—	5	—	ns
Clock low pulse width	t_{CKLCKH}	5	—	5	—	ns
Address setup to clock high	t_{AVCKH}	3	—	3	—	ns
Address hold from clock high	t_{CKHAX}	0.5	—	1	—	ns
Chip enable setup to clock high	t_{CEVCKH}	3	—	3	—	ns
Chip enable hold from clock high	t_{CKHCEX}	0.5	—	1	—	ns
Write enable setup to clock high	t_{WEVCKH}	3	—	3	—	ns
Write enable hold from clock high	t_{CKHWEX}	0.5	—	1	—	ns
Input data setup to clock high	t_{DVCKH}	3	—	3	—	ns
Input data hold from clock high	t_{CKHDX}	0.5	—	1	—	ns

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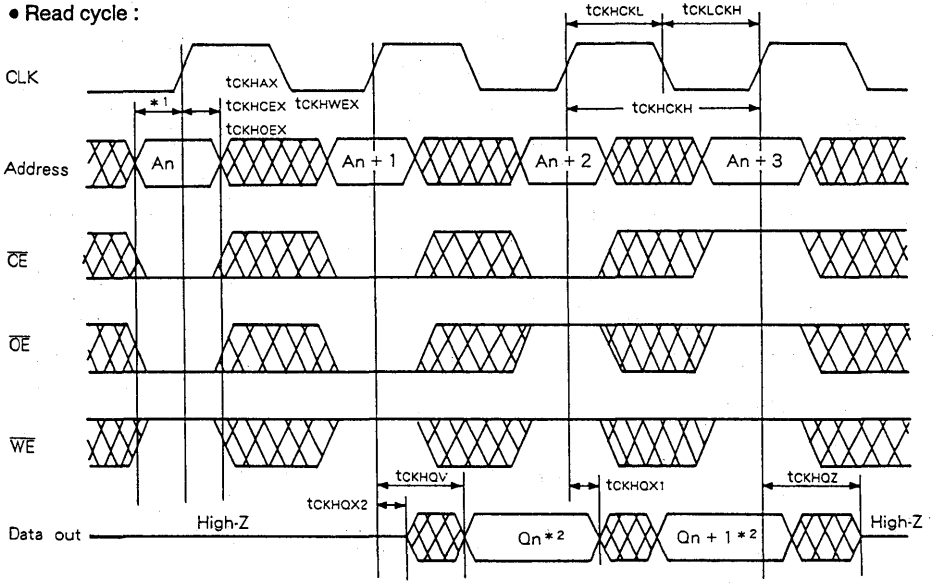
Timing Waveform

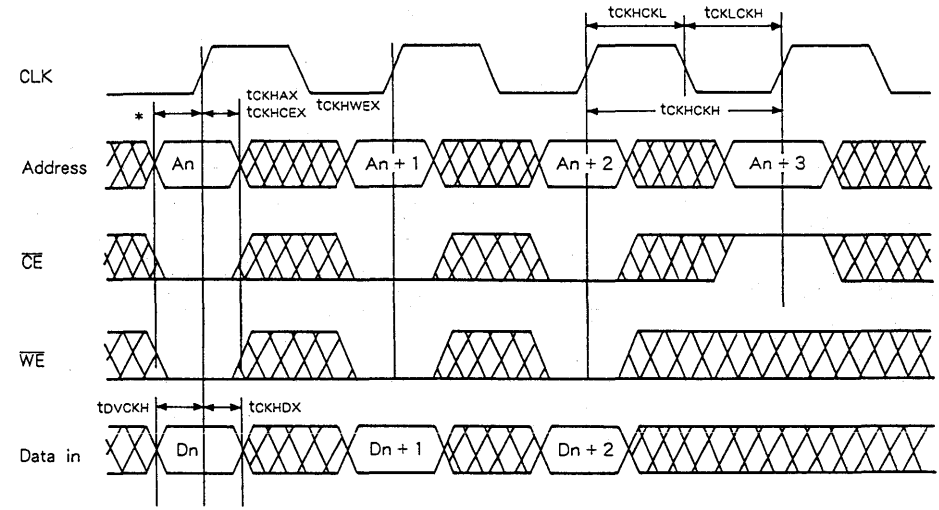
• Read cycle :



*1 tAVCKH, tCEVCKH, tOEVCKH, tWEVCKH

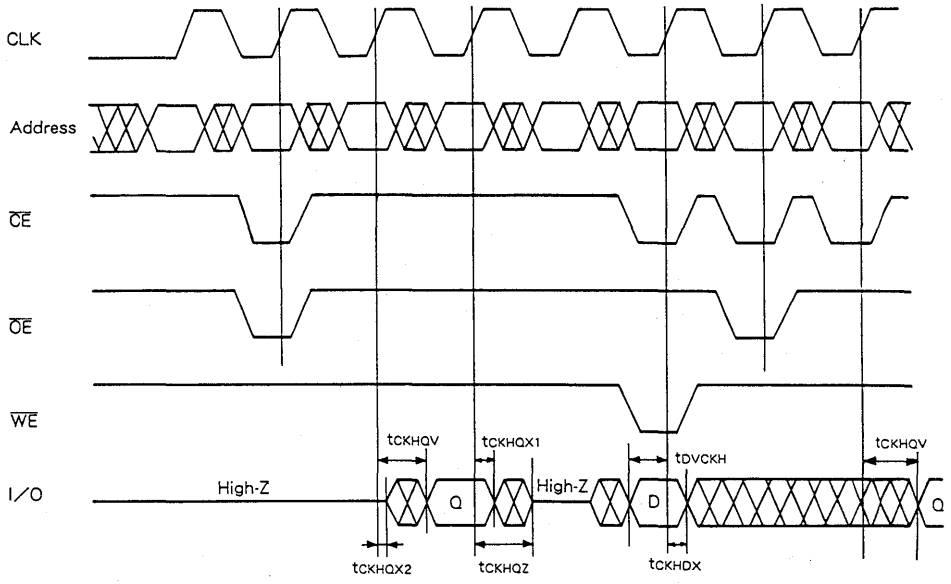
*2 Valid data from CLK high is the data from the previous cycle.

• Write cycle: $\overline{OE}$=VIH or VIL



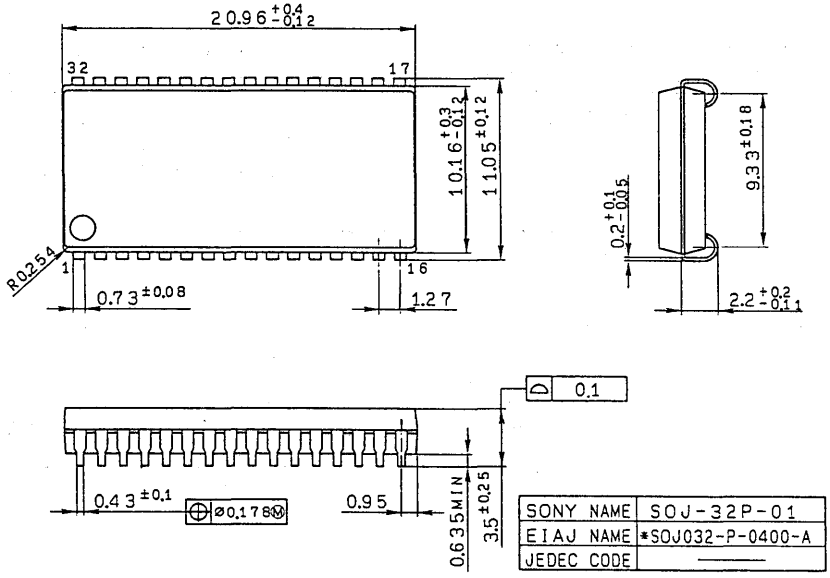
* tAVCKH, tCEVCKH, tWEVCKH

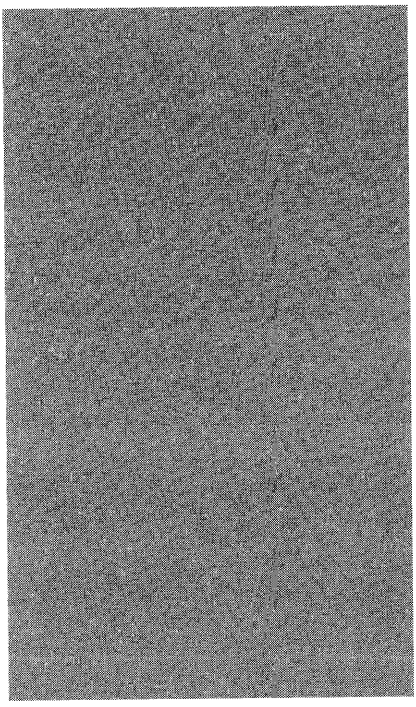
• Alternate Read/Write cycle



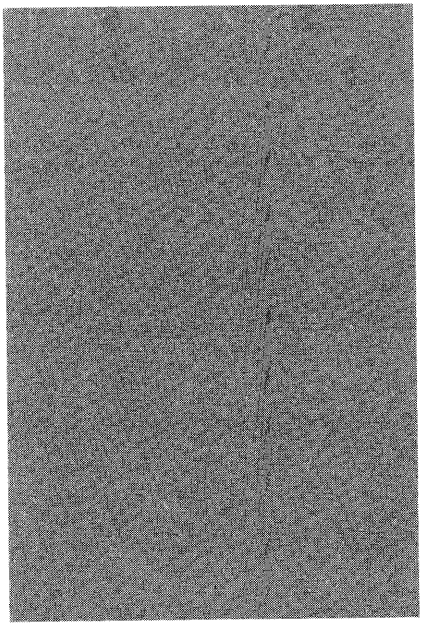
Package Outline Unit : mm

32pin SOJ (Plastic) 400mil 1.3g





Mask ROM



3) Mask ROM

Type	Function	Process	Page
CXK384001	524,288 word x 8bits, 200ns	CMOS	350

SONY CXK384001/382001

524,288 /262,144-word × 8-bit CMOS Mask Programmable ROM

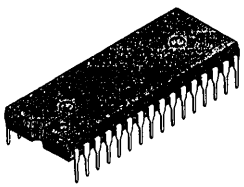
Description

CXK384001 / 382001 is a CMOS mask-programmable ROM organized as 524,288 words by 8-bit (CXK384001) and 262,144 words by 8-bit (CXK382001). The chip enable input disable outputs and sets the chip to low power standby mode.

Features

- Access time (Max.)
  - Address access time 200ns
  - Chip enable access time 200ns
  - Output enable access time 70ns
- Power consumption (Typ.)
  - 100mW (Operation)
  - 0.5mW (Standby TTL input level)
  - 5.0nW (Standby CMOS input level)
- Static operation
- I/O TTL compatible
- Tri-state output
- Single +5V power supply operation

32 pin DIP (Plastic)



Functions

CXK384001

524,288-word × 8-bit mask programmable ROM

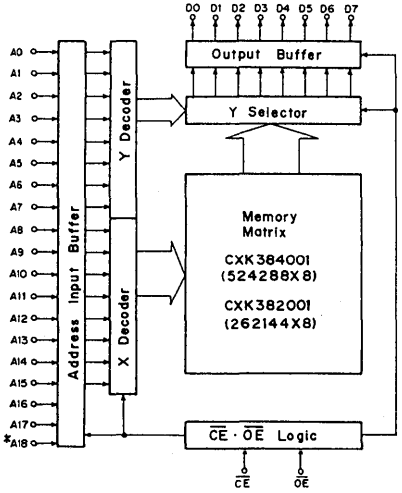
CXK382001

262,144-word × 8-bit mask programmable ROM

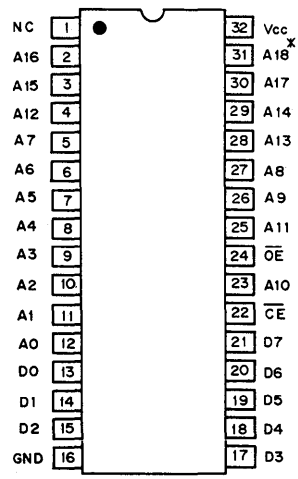
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A18*	Address input
D0 to D7	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Note)* See the below table.

Typ.	Block Diagram	Pin Configuration	Pin Description
CXK384001	A18	A18	A0 to A18
CXK382001	No A18	NC	A0 to A17

E89439A – 97ST

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Output voltage	V_{OUT}	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature • time	Tsolder	260 • 10	℃ • sec

Note) * V_{IN}, V_{OUT} = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	Mode	Output pin	V_{CC} current
H	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	Selected	Data output	I_{CC1}, I_{CC2}

Note) X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.*	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3**	—	0.8	V

Note) * V_{CC} = 5V, Ta = 25℃
** V_{IL} = − 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC characteristics (V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to + 70℃)

Item	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	0V ≦ V_{IN} ≦ V_{CC}	− 1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} 0V ≦ V_{OUT} ≦ V_{CC}	− 1	—	1	μA
Operating current (DC)	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA	—	10	40	mA
Average operating current	I_{CC2}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Duty = 100%, Minimum cycle	—	20	50	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ V_{CC} − 0.2V	—	0.001	30	μA
	I_{SB2}	$\overline{CE}$ = V_{IH}	—	0.1	2.0	mA
Output high voltage	V_{OH}	I_{OH} = − 400 μA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	V

Note) * V_{CC} = 5V, Ta = 25℃

Capacitance (Ta = 25℃, f = 1MHz)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	8	15	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	—	6	15	pF

Note) This parameter is sampled and is not 100% tested.

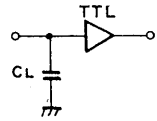
AC characteristics

AC test condition (V_{CC} = 5V ± 10%, Ta = 0 to +70℃)

Item	Condition
Input pulse high level	V_{IH} = 2.4V
Input pulse low level	V_{IL} = 0.6V
Input rise time	tr = 10ns
Input fall time	tf = 10ns
Input timing reference level	V_{IL} = V_{IH} = 1.5V
Output timing reference level	V_{OL} = V_{OH} = 1.5V
Output load	C_L* = 100pF, 1TTL

Note) C_L includes scope and jig capacitances.

• **Test circuit**



AC characteristics

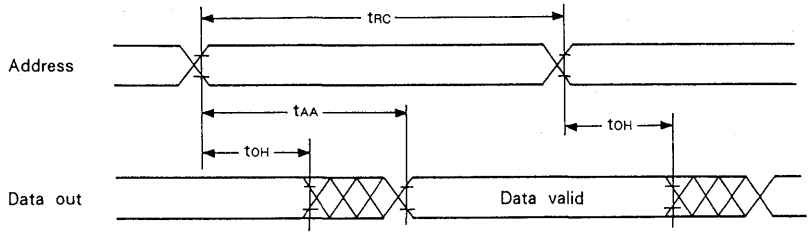
Item	Symbol	Min.	Typ.**	Max.	Unit
Read cycle time	t_{RC}	200	130	—	ns
Address access time	t_{AA}	—	120	200	ns
Chip enable access time	t_{CO}	—	130	200	ns
Output enable access time	t_{OE}	—	40	70	ns
Output data hold time	t_{OH}	0	—	—	ns
Output enable time (from $\overline{CE}$)	t_{LZ}	0	—	—	ns
Output enable time (from $\overline{OE}$)	t_{OLZ}	0	—	—	ns
Output disable time (from $\overline{CE}$)	t_{HZ}*	—	40	70	ns
Output disable time (from $\overline{OE}$)	t_{OHZ}*	—	40	70	ns

Note) * t_{HZ} and t_{OHZ} are defined as the time required for the outputs to turn to high impedance state and are not referred to as output voltage levels.

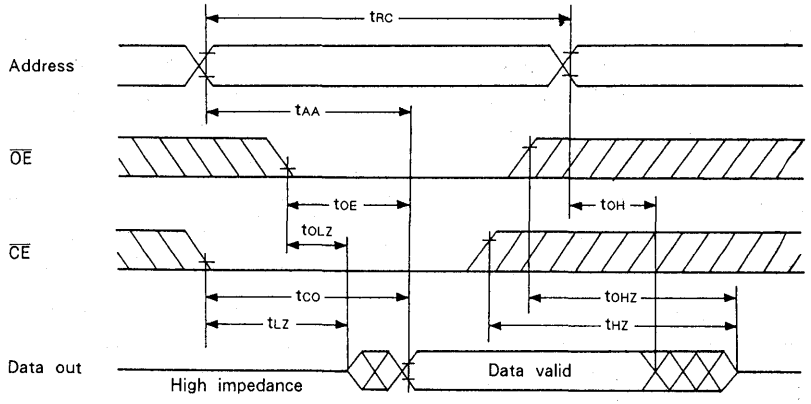
** V_{CC} = 5V, Ta = 25℃

Timing Waveform

- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$



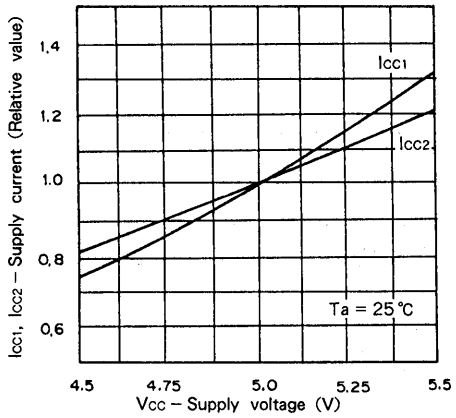
- Read cycle (2)



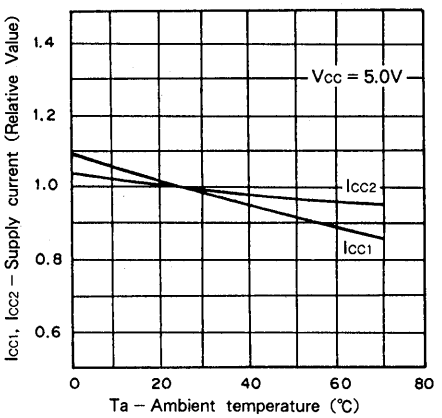
5

Example of Representative Characteristics

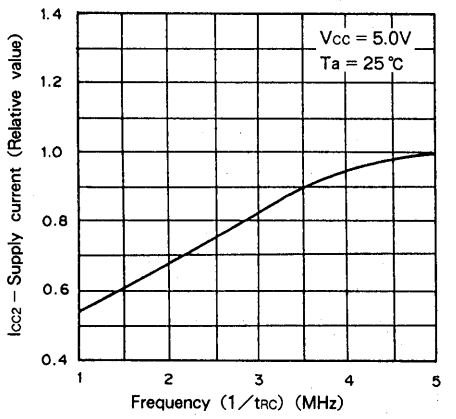
Supply current vs. Supply voltage



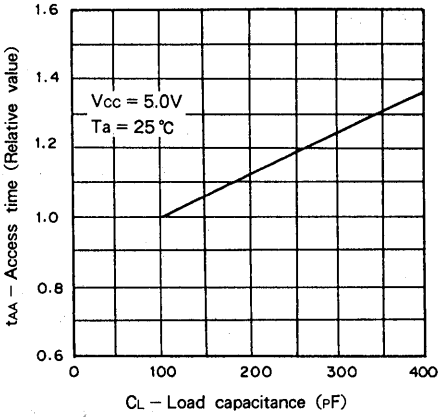
Supply current vs. Ambient temperature



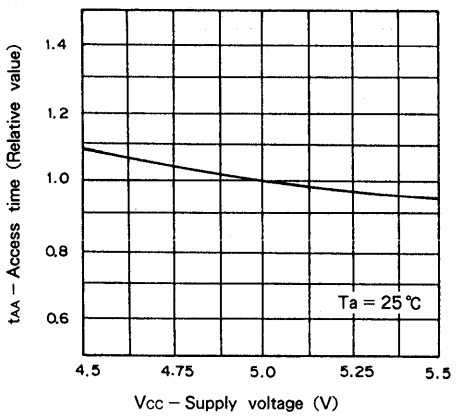
Supply current vs. Frequency



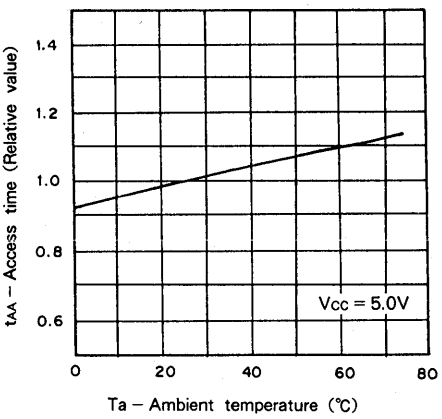
Access time vs. Load capacitance



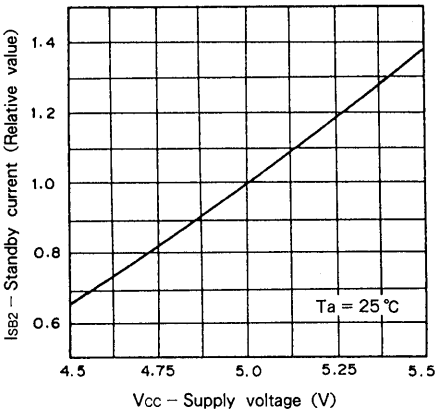
Access time vs. Supply voltage



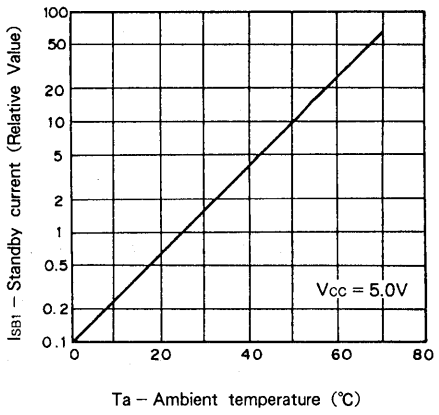
Access time vs. Ambient temperature



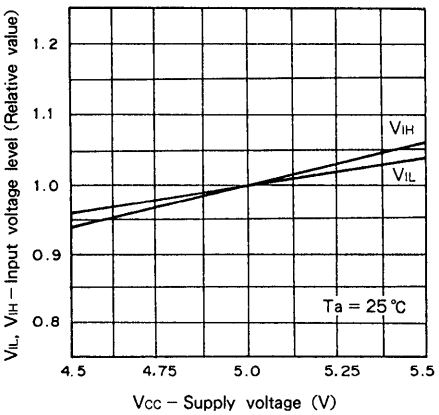
Standby current vs. Supply voltage



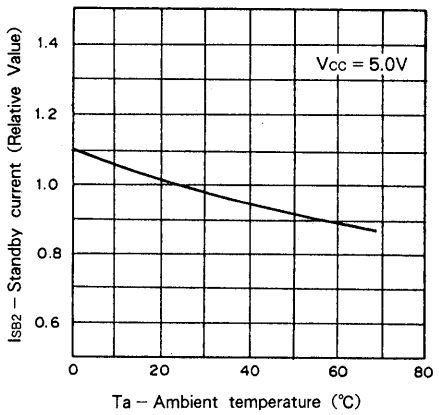
Standby current vs. Ambient temperature



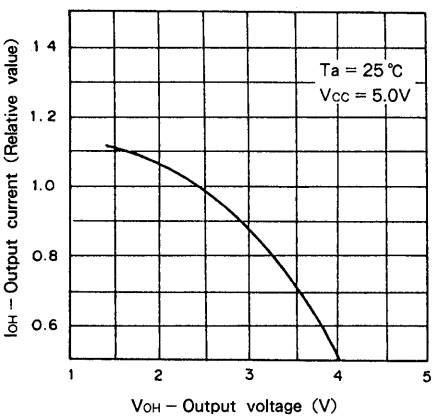
Input voltage level vs. Supply voltage



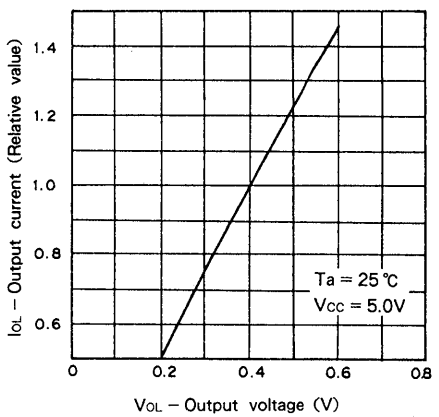
Standby current vs. Ambient temperature



Output current vs. Output voltage



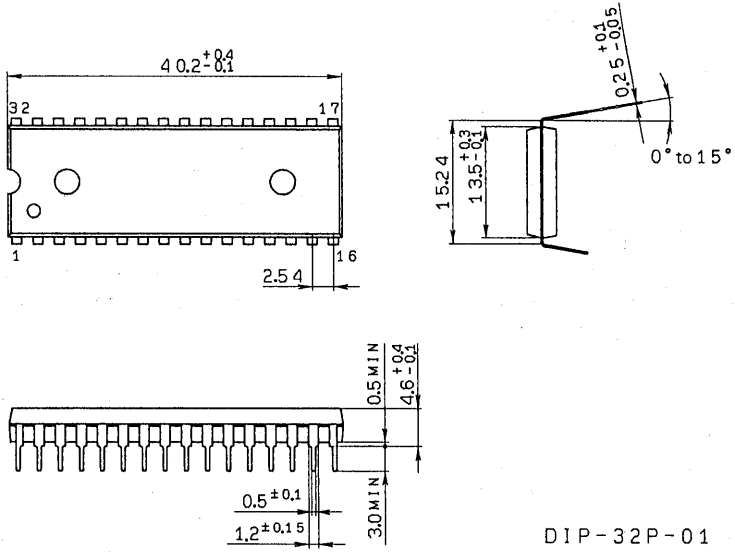
Output current vs. Output voltage



5

Package Outline Unit : mm

32 pin DIP (Plastic) 600mil 4.5g



DIP-32P-01

9. Sales Offices

Area Office	Address	Phone	Fax
Southwest	10833 Valley View Street Cypress, CA 90630-0016	714/229-4442	714/229-4333
Northwest	655 River Oaks Parkway San Jose, CA 95134	408/944-4314	408/433-0834
North Central	1200 N. Arlington Heights Road Itasca, IL 60143	708/773-6072	708/773-6068
Northeast	85 Wells Avenue Newton, MA 02159	617/630-8812	617/630-8890
Canada	1602 Tricot Ave. Whitby, Ontario LIN 5S6	416/686-2201	416/686-4802

Sales Representative Offices:

Alabama: Rep, Inc., 205/881-9270
Alaska: Sony, 408/432-0190
Arkansas: B-P Sales, 214/234-8438
Arizona: Sony, 714/229-4442
California: (San Diego) Addem, 619/729-9216
(Los Angeles) HT Sales, 714/583-1488
(Bay Area) Brooks, 415/960-3880
(Sacramento) Brooks, 916/676-2025
Colorado: Electrodyne, 303/695-8903
Connecticut: Tech Rep, 617/272-5965
Delaware: S-J Assoc., 703/533-2233
District of Columbia: S-J Assoc., 703/533-2233
Florida: Sigma, 813/789-5522
Georgia: Rep, Inc., 404/938-4358
Hawaii: Brooks, 415/960-3880
Idaho: Electrodyne, 801/264-8050
Illinois: (Northern) Micro-Tex, 708/382-3001
(Southern) Sony, 708/773-6072
Indiana: Giesting, 317/844-5222
Iowa: J.R. Sales, 319/393-2232
Kansas: Sony, 708/773-6072
Kentucky: Giesting, 606/873-2330
Louisiana: B-P Sales, 214/234-8438
Maine: Tech Rep, 617/272-5965
Maryland: S-J Assoc., 703/533-2233
Massachusetts: Tech Rep, 617/272-5965
Michigan: Giesting, 313/478-8106
Minnesota: Sony, 708/773-6072
Mississippi: Rep, Inc., 205/881-9270
Missouri: Sony, 708/773-6072
Montana: Electrodyne, 801/264-8050
Nebraska: Sony, 708/773-6072
Nevada: (Northern) Brooks, 415/960-3880
(Southern) Sony, 714/229-4442
New Hampshire: Tech Rep, 617/272-5965
New Jersey: (Northern) S-J Assoc., 516/536-4242
(Southern) S-J Assoc., 609/866-1234
New Mexico: FP Sales, 505/345-5553
New York: (Metropolitan) S-J Assoc., 516/536-4242
(Upstate) Tri Tech, 716/385-6500
North Carolina: (East) Rep, Inc., 919/469-9997
(West) Rep, Inc., 704/563-5554
North Dakota: Sony, 708/773-6072
Ohio: (Cleveland) Giesting, 216/261-9705
(Cincinnati) Giesting, 513/385-1105
Oklahoma: B-P Sales, 214/234-8438
Oregon: Vantage, 503/620-3280
Pennsylvania: (East) S.J. Assoc., 609/866-1234
(West) Giesting, 412/828-3553
Rhode Island: Tech Rep, 617/272-5965
South Carolina: Rep, Inc., 704/563-5554
South Dakota: Sony, 708/773-6072
Texas: (Austin) B-P Sales, 512/346-9186
(Dallas) B-P Sales, 214/234-8438
(Houston)B-P Sales, 713/782-4144
Tennessee: Rep, Inc., 615/475-9012
Utah: Electrodyne, 801/264-8050
Vermont: Tech Rep, 617/272-5965
Virginia: S-J Assoc., 703/533-2233
Washington: Vantage, 206/455-3460
West Virginia: Giesting, 513/385-1105
Wisconsin: (Northern) Sony, 708/773-6072
(Southern) Micro-Tex, 414/542-5352
Wyoming: Electrodyne, 801/264-8050

Distributor Offices:

Alabama:	
Huntsville	Marshall, 205/881-9235
Arizona:	
Phoenix	Marshall, 602/496-0290
California:	
Los Angeles	Milgray, 805/484-4055
El Monte	Marshall, 818/459-5500
Ft. Valley	Bell Micro, 714/963-0667
Saratoga	Western Micro, 408/725-1660
Irvine	Marshall, 714/458-5395
Los Angeles	Marshall, 818/878-7000
Los Angeles	Western Micro, 818/707-0377
Milpitas	Bell Micro, 408/434-1150
Orange	Western Micro, 714/637-0200 or 818/356-0180
Sacramento	Marshall, 916/635-9700
San Diego	Ageis, 619/729-2026
San Diego	Marshall, 619/578-9600
San Diego	Western Micro, 619/453-8430
San Jose	Merit, 408/434-0800 (Semiconductor)
San Francisco	Marshall, 408/942-4600
Colorado:	
Denver	Marshall, 303/451-8444
Denver	Robert Waxman, 303/623-1200 (Cameras)
Connecticut:	
Danbury	Phase I, 203/791-9042
Milford	Milgray, 203/878-5538 or 800/922-6911
Wallingford	Marshall, 203/265-3822
Florida:	
Deerfield	Vantage, 305/429-1001 (Semiconductor)
Ft. Lauderdale	Marshall, 305/977-4880
Orlando	Marshall, 407/767-8585
Tampa	Marshall, 813/576-1399
Winter Park	Milgray, 407/647-5747 or 800/432-0645
Georgia:	
Atlanta	Marshall, 404/923-5750
Norcross	Milgray, 404/446-9777 or 800/241-5523
Illinois:	
Chicago	Milgray, 708/253-1212
Chicago	Marshall, 708/490-0155
Indiana:	
Indianapolis	Marshall, 317/297-0483
Kansas:	
Kansas City	Marshall, 913/492-3121
Overland Park	Milgray, 913/236-8800
Maryland:	
Columbia	Milgray, 301/621-8169 or 800/638-6656
Columbia	Vantage, 301/720-5100 (Semiconductor)
Silver Springs	Marshall, 301/622-1118
Massachusetts:	
Andover	Vantage, 508/687-3900 (Semiconductor)
Boston	Marshall, 508/658-0810
Burlington	Western Micro, 617/273-2800 or 800/345-2921
Wilmington	Bell Micro, 508/658-0222
Wilmington	Milgray, 508/657-5900
Michigan:	
Livonia	Marshall, 313/525-5850
Minnesota:	
Minneapolis	Marshall, 612/559-2211 or 1014
Missouri:	
St. Louis	Marshall, 314/291-4650
New Jersey:	
Clifton	Vantage, 201/777-4100 (Semiconductor)
Fairfield	Marshall, 201/882-0320
Fairfield	Western Micro, 201/882-4999
Garfield	Phase 1, 201/403-0002
Mt. Laurel	Marshall, 609/234-9100
Marlton	Milgray, 609/983-5010 or 800/257-7111
Marlton	Western Micro, 609/596-7775
Parsippany	Milgray, 201/335-1766
New York:	
Binghamton	Marshall, 607/798-1611
Farmingdale	Milgray, 516/420-9800 or 800/MILGRAY
Long Island	Marshall, 516/273-2424
N. Lindenhurst	Phase I, 516/957-4900
New York	Chori, 212/563-3264 (Cameras only)
Rochester	Marshall, 716/235-7620
Pittsford	Milgray, 716/834-9405
Smithtown	Vantage, 516/543-2000 (Semiconductor)
North Carolina:	
Raleigh	Marshall, 919/878-9882
Raleigh	Merit, 919/790-8094
Ohio:	
Cleveland	Marshall, 216/248-1788
Cleveland	Milgray, 216/447-1520 or 800/321-0006
Columbus	Marshall, 614/891-7580
Dayton	Marshall, 513/898-4480
Oklahoma:	
Tulsa	Marshall, 918/622-7151
Oregon:	
Tigard	Daitron, 503/620-2870 (Cameras only)
Beaverton	Western Micro, 503/629-2082
Portland	Marshall, 503/644-5050
Pennsylvania:	
Pittsburgh	Marshall, 412/788-0441
Texas:	
Austin	Marshall, 512/837-1991
Brownsville	Marshall, 512/542-4589
Dallas	Marshall, 214/233-5200
Dallas	Milgray, 214/248-1603 or 800/637-7227
Houston	Marshall, 713/895-9200
Utah:	
Salt Lake City	Marshall, 801/485-1551
Salt Lake City	Milgray, 801/272-4999
Washington:	
Redmond	Western Micro, 206/881-6737
Redmond	Merit, 206/869-7557 (Semiconductor)
Seattle	Marshall, 206/486-5747
Wisconsin:	
Milwaukee	Marshall, 414/797-8400
Canada:	
Ontario	Marshall, 416/458-8046 (Semiconductor)

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