Semiconductor IC

Data Book 1993 A/D, D/A Converters

SONY

A/D, D/A Converter Semiconductor Data Book 1993

List of Model Names/ Index by Usage 1

Description 2

A/D Converter for Video Signal Processing 3

A/D Converter for Industries Instruments 4

D/A Converter for Video Signal Processing 5

D/A Converter for Industries Instruments 6

Sample and Hold IC 7

A/D, D/A Converter for Audio Signal Processing 8

Sales Offices 9

Preface

The history of Sony Semiconductor began in 1954, with the first commercial introduction of the transistor in Japan. Since then, Sony has applied this leading edge, innovative technology in the development of the Semiconductors, currently used in most of its consumer and professional electronic products.

This A/D, D/A Converter semiconductor data book has been compiled with the aim of providing the circuit designer with a reference guide describing Sony's presently available A/D, D/A Converter products.

Contents

1. Numerical Index of Model Names 5

2. Functional Index of Model Names 6

3. IC Nomenclature 9

4. Precautions for IC Application 11

    1) Absolute maximum ratings 11

    2) Protection against electrostatic breakdown 12

    3) Mounting method 16

5. Quality Assurance and Reliability 18

6. Data Sheets 25

    A/D Converter for Video Signal Processing 25

    A/D Converter for Industries Instruments 157

    D/A Converter for Video Signal Processing 221

    D/A Converter for Industries Instruments 323

    Sample Hold IC 373

    A/D, D/A Converter for Audio Signal Processing 401

7. Sales Offices 437

Numerical Index

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20051A	10	30	550	ECL Input, 1 Channel	223-234
CX20201A-1/-2/-3	10/9/8	160	420	ECL Input, 1 Channel	325-337
CX20202A-1/-2/-3	10/9/8	160	420	ECL Input, 1 Channel	325-337
CX20206	8	35	360	TTL Input, 3 Channel	235-250
CX20220A-1/-2	10/9	20	360	2 Step, ECL I/O	27-41
CXA1008P	-	35	680	S/H for CX20220A-1/-2	375-393
CXA1009P	-	18	420	S/H for CX20220A-1/-2	375-393
CXA1076AK	8	200	1450	Flash, ECL I/O	159-174
CXA1176AK	8	300	1450	Flash, ECL I/O	159-174
CXA1096M	8	20	390	Flash, TTL I/O	42-57
CXA1096P	8	20	390	Flash, TTL I/O	58-72
CXA1106P/M	8	35	360	TTL Input, 1 Channel	267-285
CXA1156AQ	8	400	1300	ECL Input, 3 Channel	338-344
CXA1166K	8	250	1700	Flash, ECL I/O	175-186
CXA1236Q	8	500	930	ECL Input, 1 Channel	355-371
CXA1260Q-Z	8	35	360	TTL Input, 3 Channel	251-266
CXA1276K	8	500	2200	Flash, ECL I/O	187-197
CXA1296P	8	20	410	Flash, TTL I/O	73-88
CXA1386P/K	8	75	580	Flash, ECL I/O	198-208
CXA1396D/K	8	125	870	Flash, ECL I/O	209-220
CXA1496AQ	10	20	310	2 Step, TTL I/O	89-105
CXA1693Q	-	35	190	S/H for CXA1496AQ	394-400
CXD1077M	10	-	120	TTL I/O A/D, D/A Audio	403-419
CXD1170M	6	40	80	TTL I/O D/A CMOS	286-293
CXD1171M	8	40	80	TTL I/O D/A CMOS	294-301
CXD1172AM/AP	6	20	60	TTL I/O A/D CMOS	106-116
CXD1175AM/AP	8	20	60	TTL I/O A/D CMOS	117-127
CXD1176Q	8	20	60	TTL I/O w/clamp A/D CMOS	128-145
CXD1177Q	8	40	160	TTL I/O 2 channel D/A CMOS	302-311
CXD1178Q	8	40	240	TTL I/O 3 channel D/A CMOS	312-322
CXD1179Q	8	35	90	TTL I/O w/clamp A/D CMOS	146-156
CXD2552Q	18	1024Fs	500	TTL OE Audio D/A	420-427
CXD2555Q	16	256 to 1024Fs		TTL OE Audio A/D, D/A	428-436

Index by Usage

A/D Converter for Video Signal Processing

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20220A-1/-2	10/9	20	360	2 Step, ECL I/O	27-41
CXA1096M	8	20	390	Flash, TTL I/O	42-57
CXA1096P	8	20	390	Flash, TTL I/O	58-72
CXA1296P	8	20	410	Flash, TTL I/O	73-88
CXA1496AQ	10	20	310	2 Step, TTL I/O	89-105
CXD1172AM/AP	6	20	40 or 60	TTL I/O A/D CMOS	106-116
CXD1175AM/AP	8	20	60	TTL I/O A/D CMOS	117-127
CXD1176Q	8	20	60	TTL I/O w/clamp A/D CMOS	128-145
CXD1179Q	8	35	90	TTL I/O w/clamp A/D CMOS	146-156

A/D Converter for Industries Instruments

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CXA1076AK	8	200	1450	Flash, ECL I/O	159-174
CXA1176AK	8	300	1450	Flash, ECL I/O	159-174
CXA1166K	8	250	1700	Flash, ECL I/O	175-186
CXA1276K	8	500	2200	Flash, ECL I/O	187-197
CXA1386P/K	8	75	580	Flash, ECL I/O	198-208
CXA1396D/K	8	125	870	Flash, ECL I/O	209-220

D/A Converter for Video Signal Processing

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20051A	10	30	550	ECL Input, 1 Channel	223-234
CX20206	8	35	360	TTL Input, 3 Channel	235-250
CXA1260Q-Z	8	35	360	TTL Input, 3 Channel	251-266
CXA1106P/M	8	35	360	TTL Input, 1 Channel	267-285
CXD1170M	6	40	80	TTL I/O D/A CMOS	286-293
CXD1171M	8	40	80	TTL I/O D/A CMOS	294-301
CXD1177Q	8	40	160	TTL I/O 2 channel D/A CMOS	302-311
CXD1178Q	8	40	240	TTL I/O 3 channel D/A CMOS	312-322

D/A Converter for Industries Instruments

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20201A-1/-2/-3	10/9/8	160	420	ECL Input, 1 Channel	325-337
CX20202A-1/-2/-3	10/9/8	160	420	ECL Input, 1 Channel	325-337
CXA1156AQ	8	400	1300	ECL Input, 3 Channel	338-344
CXA1236Q	8	500	930	ECL Input, 1 Channel	355-371

Sample and Hold IC

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CXA1008P	-	35	680	S/H for CX20220A-1/-2	375-393
CXA1009P	-	18	420	S/H for CX20220A-1/-2	375-393
CXA1693Q	-	35	190	S/H for CXA1496AQ	394-400

A/D, D/A Converter for Audio Signal Processing

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CXD1077M	10	-	120	TTL I/O A/D, D/A Audio	403-419
CXD2552Q	18	1024Fs	500	TTL OE Audio D/A	420-427
CXD2555Q	16	256 to 1024Fs		TTL OE Audio A/D, D/A	428-436

3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Conventional nomenclature system

[Example] CX 20 011 A

- Improvement mark
  "A" is affixed when specifications are partially improved.
- Product number
  Identifies individual product.
- Category number
  Indicates the product category in one or two digits.
  Bipolar IC: 0, 1, 8, 10, 20, 22
  MOS IC: 5, 7, 23, 79
- Sony IC mark

b) New nomenclature

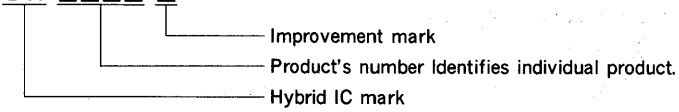
[Example] CX A 1001 A P

- Package mark
  P: Plastic Dual In-line Package
  D: Ceramic Dual In-line Package
  M: Small Outline L-Leaded Package
  L: Single In-line Package
  Q: Quad Flat L-Leaded Package
  S: Shrink Dual In-line Package
  N: Very Small Outline Package (SSOP)
  R: Very Small Quad Flat Package
- Improvement mark
  "A" is affixed when specifications are improved.
- Product number
  Identifies the individual product.
- Product category mark
  A: Bipolar IC
  B: Bipolar digital IC
  D: MOS logic IC
  K: Memory, Mask ROM
  P, Q: Microcomputer, Microprocessor
  L: CCD signal processor
- Sony IC mark

2) Hybrids nomenclature

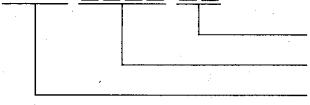
(1) Conventional nomenclature system

[Example] BX-□□□□-□



(2) New nomenclature

[Example] SBX □□□□-□□



Hybirds have carried SBX or BX prefix up to January 1987. i.e. BX-1452, Those developed after the above dute all stand by SBX. i.e. SBX1435/SBX1475.

4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (VDD)

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit. The transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation PD

The maximum power consumption allowed in IC.

Usage beyond the Allowable power dissipation will cause ultimate destruction through the IC's heat generation.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

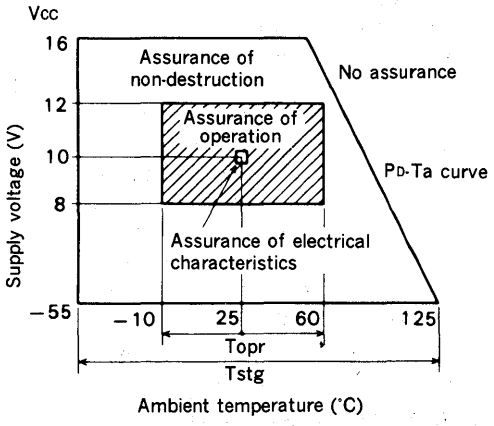
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

A general example on the relation with Absolute Maxium Ratings.



Main points on Circuit design.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

2

2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

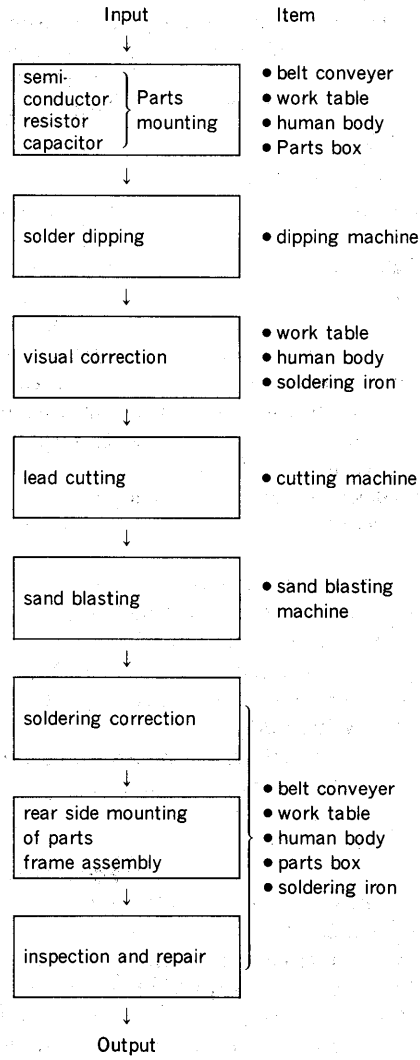
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room to about 50%.

Operator

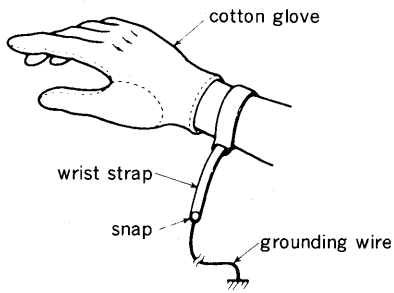
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

example of grounding band

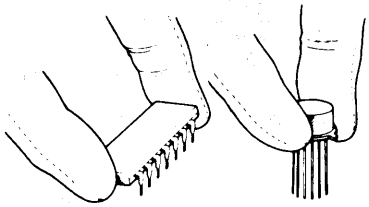


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



DIP type can type

Equipment and tools

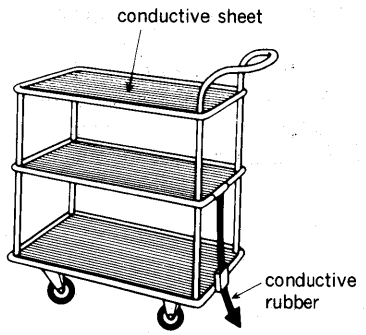
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

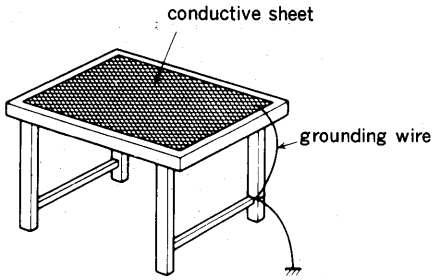
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

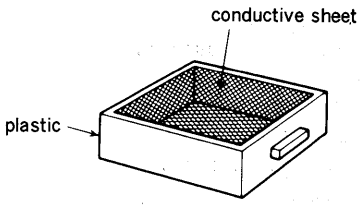
grounding of work table



(3) Semiconductor device case

Use a conductive case, or an antistatic plastic case (lined with conductive sheet).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet.

(5) Other points of caution

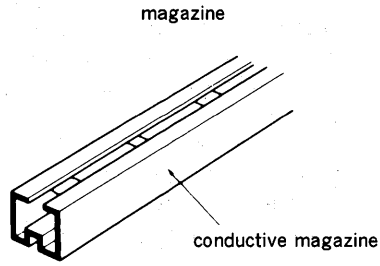
Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

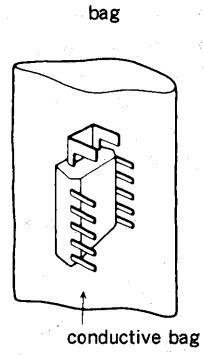
Use conductive, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

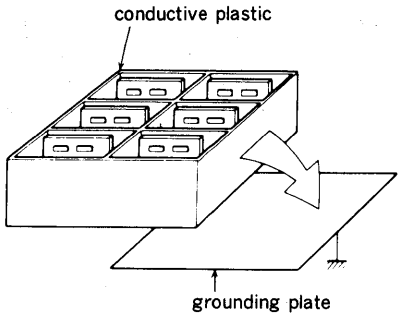
Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of conductive plastic. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



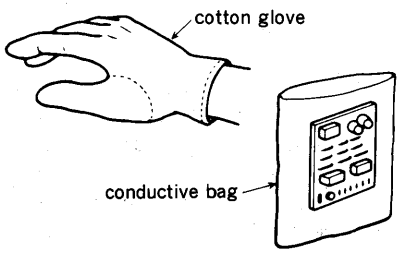
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table for discharging.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

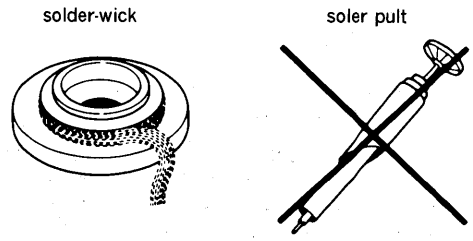
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table for soldering. Do not solder on foam styrol, vinyl, or melamine resin.

2

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

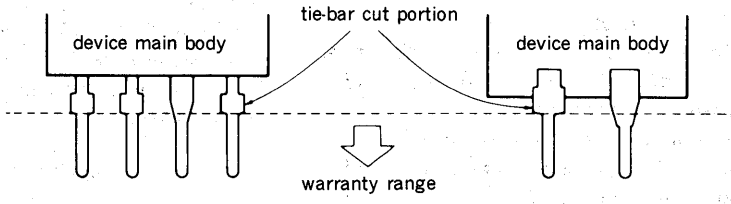
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

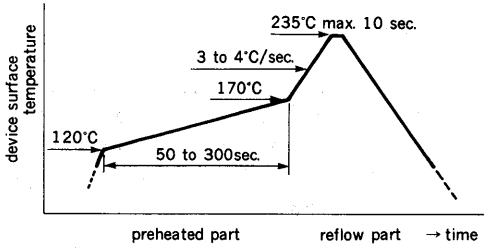
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

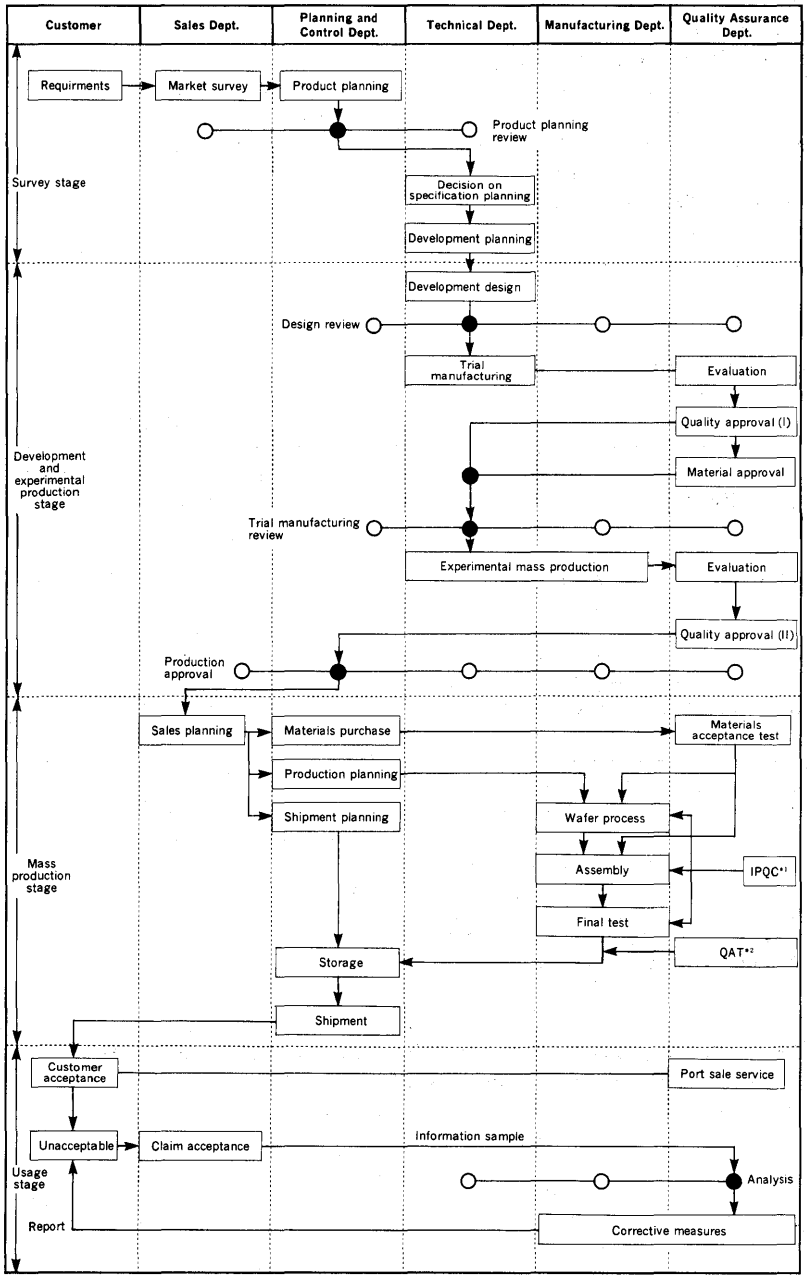
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

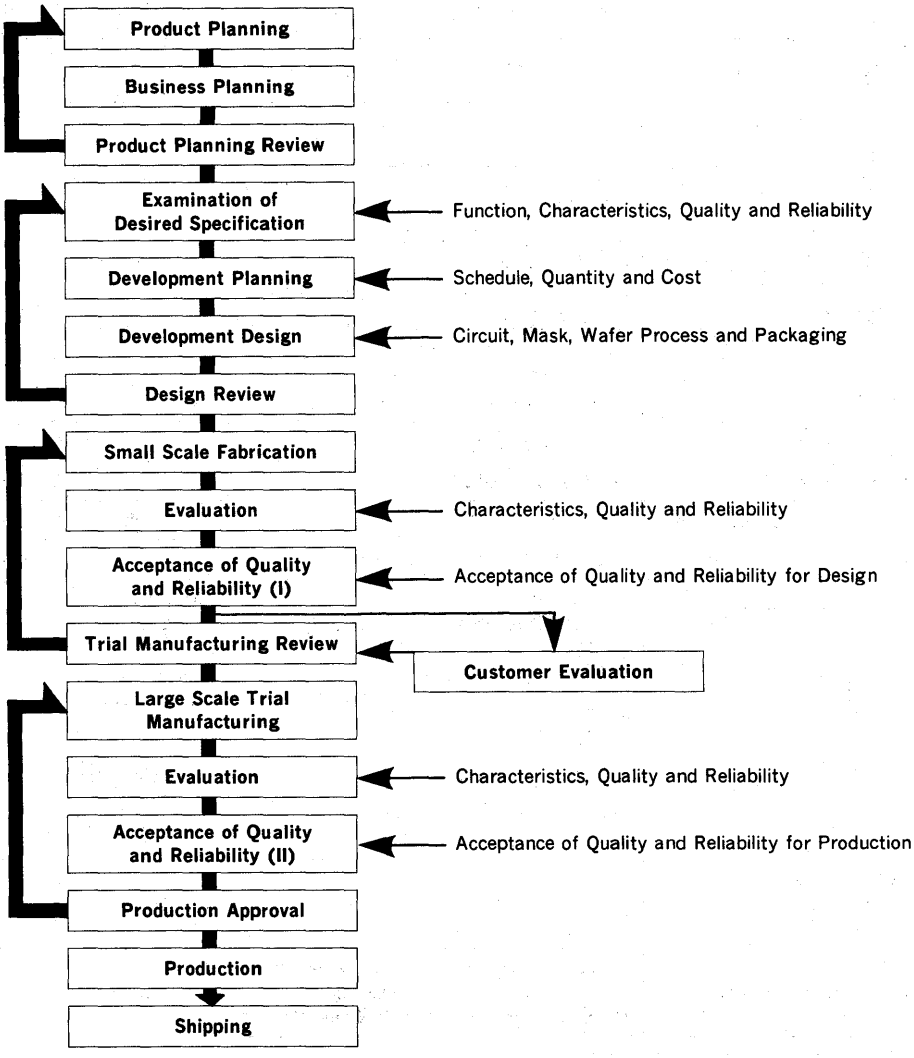
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

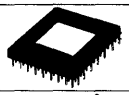
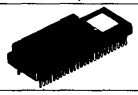
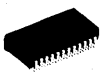
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.

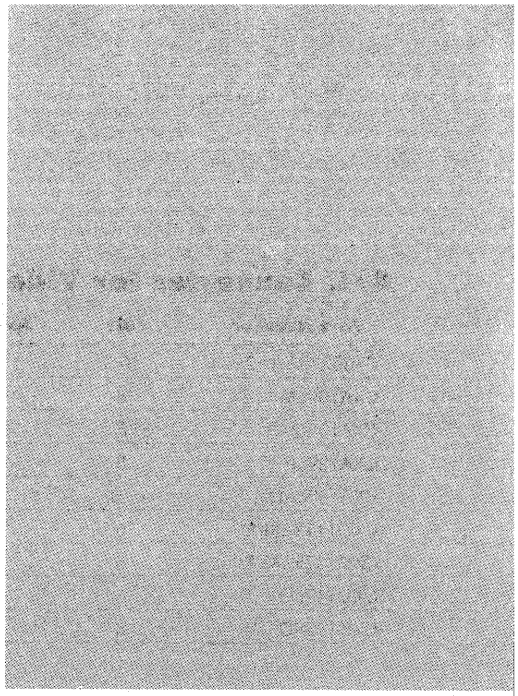


Package Name

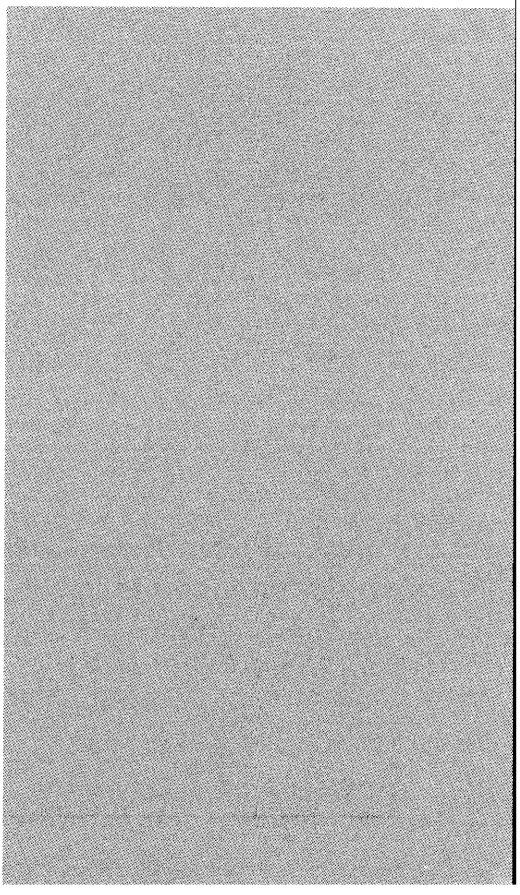
Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	Zig-Zag IN-LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK Zig-Zag IN-LINE PACKAGE		P	1.778mm (70MIL) Zig Zag inline	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE		P	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
	Standard chip carrier	Q F J (PLCC)	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		Q F N (LCC)	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package side

*P……Plastic, C……Ceramic

2



A/D Converter for Video Signal Processing



A/D Converter for Video Signal Processing

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20220A-1/-2	10/9	20	360	2 Step, ECL I/O	27-41
CXA1096M	8	20	390	Flash, TTL I/O	42-57
CXA1096P	8	20	390	Flash, TTL I/O	58-72
CXA1296P	8	20	410	Flash, TTL I/O	73-88
CXA1496AQ	10	20	310	2 Step, TTL I/O	89-105
CXD1172AM/AP	6	20	40 or 60	TTL I/O A/D CMOS	106-116
CXD1175AM/AP	8	20	60	TTL I/O A/D CMOS	117-127
CXD1176Q	8	20	60	TTL I/O w/clamp A/D CMOS	128-145
CXD1179Q	8	35	90	TTL I/O w/clamp A/D CMOS	146-156

SONY CX20220A-1/-2

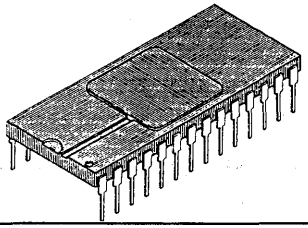
10/9Bit 20MSPS Sub-ranging A/D Converter (ECL I/O)

Description

CX20220A series is a high-speed, 20MSPS A/D converter which comes in two types of resolution, 10-bit and 9-bit, that are distinguished by the number suffixed to the name. Since a series-parallel system is used, an external sample hold circuit is required.

- Resolution: 10 bits (CX20220A-1)
  9 bits (CX20220A-2)
- Maximum conversion rate: 20MSPS
- Digitizing range: 0 to −2V
- Digital input/output: ECL level
- Output code: binary
- Low power consumption: 360 mW

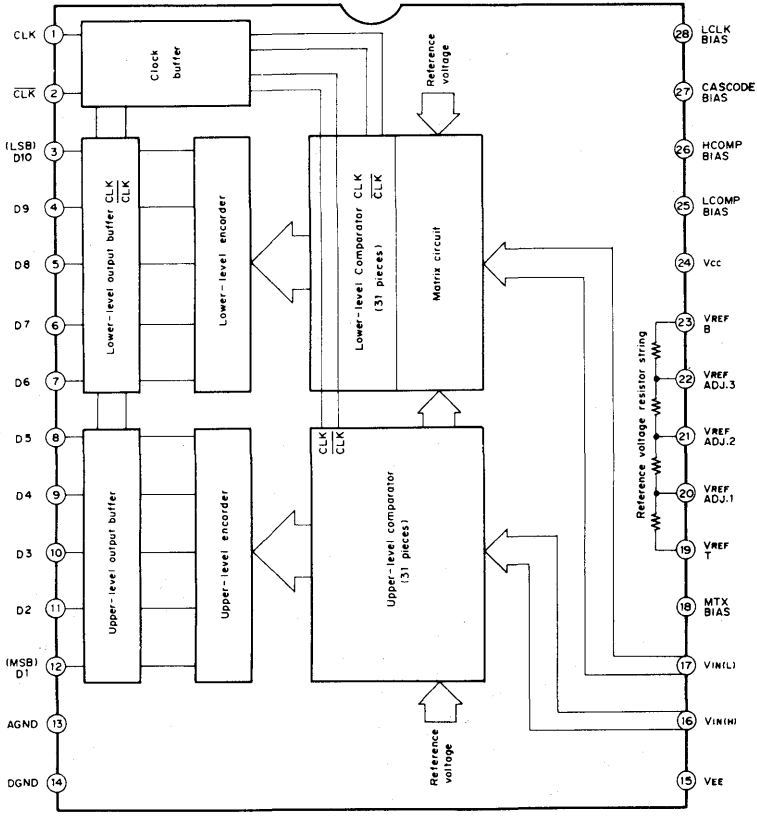
28pin DIP (Ceramic)



Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration (Top View)



E89639-HP

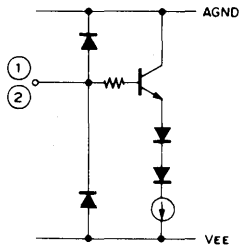
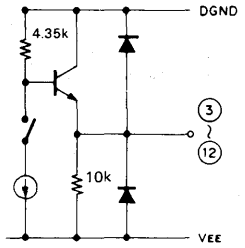
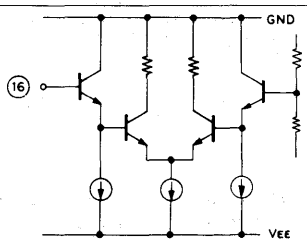
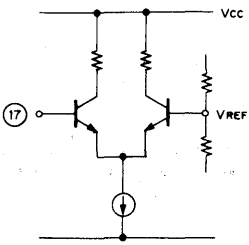
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	2.5	V
	V_{EE}	−7	V
• Analog voltage	V_I	V_{EE} to 0.3	V
• Clock input voltage	V_{CLK}, $V_{\overline{CLK}}$	V_{EE} to 0.3	V
• Reference voltage	V_{REF}	V_{EE} to 0.3	V
• Digital output current	I_{D01} to I_{D10}	0 to −20	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.23	W

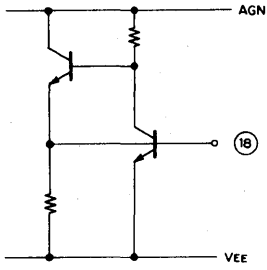
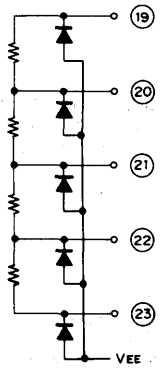
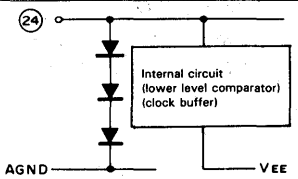
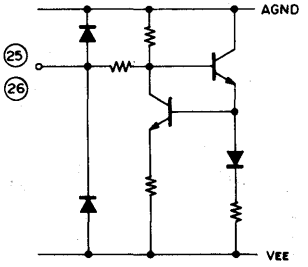
Recommended Operating Conditions

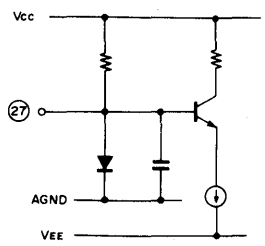
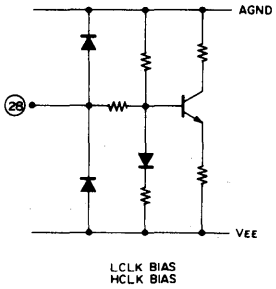
• Supply voltage	V_{CC}	1.6 to 2.1	V
	V_{EE}	−5.25 to −4.75	V
	A_{GND}-D_{GND}	−0.05 to +0.05	V
• Reference voltage	$V_{REF.T}$	0	V
	$V_{REF.B}$	−2.0	V
• Analog input voltage	V_I	$V_{REF.B}$ to $V_{REF.T}$	V
• Clock input voltage	V_{IH}	−1.1 min.	V
	V_{IL}	−1.4 max.	V
• Clock pulse width	T_{PW1}	20 min.	ns
	T_{PW0}	22 min.	ns

Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	CLK		Clock input pin, ECL level.
2	$\overline{\text{CLK}}$		Inverse clock input pin, ECL level
3	D10(LSB)		Digital output pin, ECL level, pull-down resistor (10KΩ) built in
4	D9		
5	D8		
6	D7		
7	D6		
8	D5		
9	D4		
10	D3		
11	D2		
12	D1(MSB)		
13	AGND		Analog ground pin
14	DGND		Digital ground pin
15	VEE		Power supply pin. To be grounded with ceramic chip capacitor of 0.1 μF or over.
16	VIN(H)		Analog input pin (Upper level)
17	VIN(L)		Analog input pin (Lower level)

3

No.	Symbol	Equivalent circuit	Description
18	MTX BIAS		Pin connected internal matrix, which is normally used open.
19	VREF.T		Reference voltage pin (top), 0 V (typ.)
20	VREF ADJ. 1		Reference voltage adjusting pin. To be grounded with ceramic chip capacitor of 0.1μF or over.
21	VREF ADJ. 2		
22	VREF ADJ. 3		
23	VREF.B		Reference voltage pin (bottom), −2 V (typ.) To be grounded with ceramic chip capacifor of 0.1μF or over.
24	VCC		Internal power supply pin. Three diodes are incorporated in series, so that by connecting pull-up resistor to +5 V
25	LCOMP BIAS		Pin connected internal lower level comparator, which is normally used open.
26	HCOMP BIAS		Pin connected internal upper level comparator which is normally used open.

No.	Symbol	Equivalent circuit	Description
27	CASCODE BIAS		Cascode bias pin. To be bypassed to GND with ceramic capacitor of 0.1μF or over.
28	LCLK BIAS		Pin connected internal lower level buffer, which is normally used open.

3

Electrical Characteristics (1) (See the Electrical Characteristics Test Circuit)

CX20220A-1 (10Bit) (Ta = 25°C, VCC = 1.6V, VEE = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								10		bit
Differential linearity error	E_D	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	E_L	A	A	A	D	Differential waveform output				±1	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc=14.32MSPS nonlock		0.7		%
Differential phase error	DP	A	A	A		DA output			0.3		deg

CX20220A-2 (9Bit)

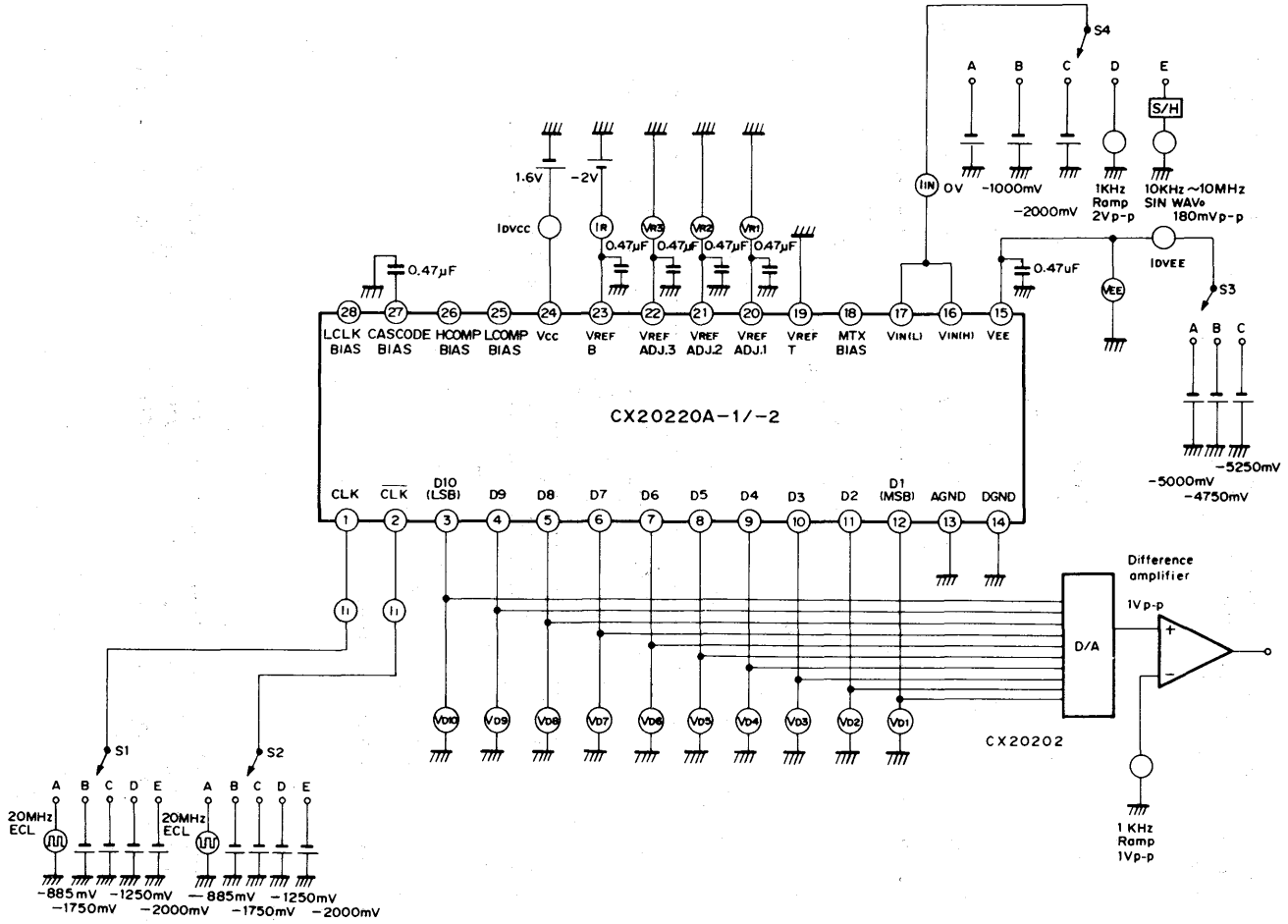
Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Resolution	n								9		bit
Differential linearity error	E_D	A	A	A	D	Differential waveform output				±1	LSB
Integral linearity error	E_L	A	A	A	D	Differential waveform output				±1/2	LSB
Differential gain error	DG	A	A	A		DA output	SW4:NTSC 40IRE mod. ramp fc=14.32MSPS nonlock		1.0		%
Differential phase error	DP	A	A	A		DA output			0.5		deg

Electrical Characteristics (2) (See the Electrical Characteristics Test Circuit)

(Ta = 25°C, V_{CC} = 1.6V, V_{EE} = −5V)

Item	Symbol	SW Condition				Test point	Test condition	Min.	Typ.	Max.	Unit
		SW1	SW2	SW3	SW4						
Conversion rate	f_{max}	A	A	A	D	DA output		20			MSPS
Power consumption(1)	I_{DVCC}	B	D	A	A	I_{DVCC}			17	25	mA
Power consumption(2)	I_{DVEE}	B	D	A	A	I_{DVEE}		−80	−60		mA
Resistor string current	I_{REF}	B	D	A	A	I_R		−14	−12.5		mA
Resistor string pin voltage (1)	V_{R1}	B	D	A	A	V_{RI}		−0.51	−0.5	−0.49	V
Resistor string pin voltage (2)	V_{R2}	B	D	A	A	V_{R2}		−1.01	−1.0	−0.99	V
Resistor string pin voltage (3)	V_{R3}	B	D	A	A	V_{R3}		−1.51	−1.5	−1.49	V
Offset voltage, V_{RT} side	E_{OT}	B	C	A	A				2		mV
Offset voltage, V_{RB} side	E_{OB}	B	C	A	A				4		mV
Analog input current	I_{IN}	B	D	A	A	I_{IN}			40	80	μA
Analog input capacity (1)	C_{IN}	A	A	A			SW4: V_{IN} = 0V + 0.07 Vrms 4 MHz		230		pF
Analog input capacity (2)	C_{IN}	A	A	A			V_{IN} = −2V + 0.07 Vrms 4 MHz		190		pF
Analog input bandwidth	BW	A	A	A	E	DA output	Measurement of output amplitude		10		MHz
Digital input current (1)	I_{IH}	B	C	A	A	I_I			5	8	μA
Digital input current (2)	I_{IL}	E	D	A	A	I_I			5	8	μA
Inverse digital input current (1)	I_{IH}	C	B	A	A	I_I			5	8	μA
Inverse digital input current (2)	I_{IL}	D	E	A	A	I_I			5	8	μA
Digital output voltage, H level (1)	V_{IL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor.	−0.9	−0.8		V
Digital output voltage, H level (2)	V_{OH}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.0		V
Digital output voltage L level (1)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		−1.6	−1.5	V
Digital output voltage, L level (2)	V_{OL}	A	D	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω.		−1.9		V
Output data delay (1)	T_d	A	A	A	A	V_{D1} to V_{D10}	Do not connect pull-down resistor		10		ns
Output data delay (2)	T_d	A	A	A	A	V_{D1} to V_{D10}	Pull-down resistor is 1k Ω		5		ns

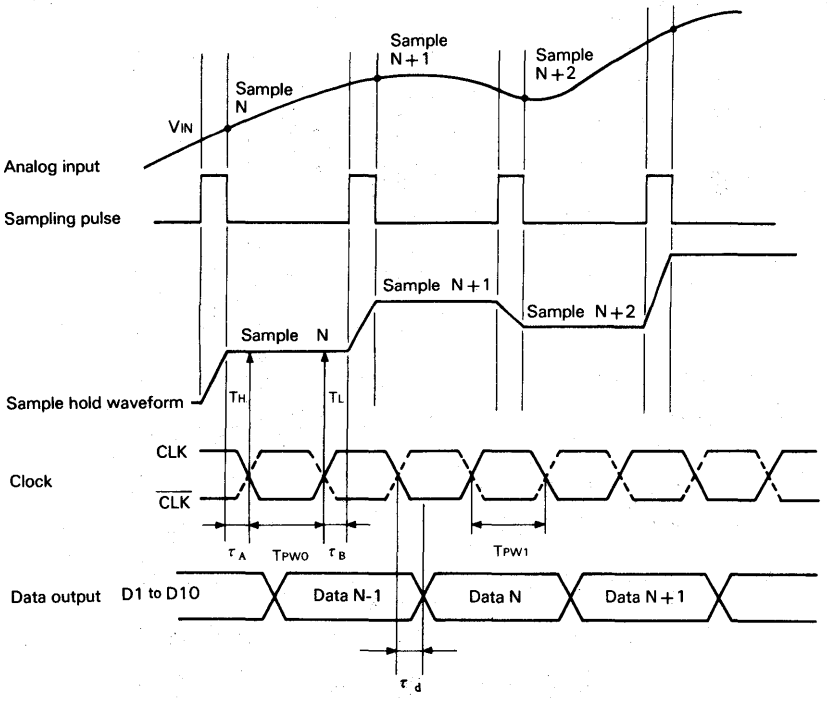
Electrical Characteristic Test Circuit



Reference Data for Standard Circuit Design

Clock Timing

CX20220A-1/-2 is a series-parallel-type A/D converter, and therefore an external sample and hold circuit is required. Careful timing, design should be made according to the timing chart shown below.
The timing design between the S/H output and the A/D clock is important.



Clock Timing

$\tau_A \geqq T_A$ (Aperture time + settling time of sample and hold circuit)

$\tau_B \geqq 2ns$

$T_{PW0} \geqq 22ns$

$T_{PW1} \geqq 20ns$

$\tau_d \leqq$ ns

TH is the timing in which the upper level comparator compares VIN and VREF and latches the result. TL is the timing in which the lower level comparator compares VIN and VREF and latches the result. The simple method is for output data to be latched upon rising edge of CLK. Clock duty should be chosen so that the D G and DP per form the best result.

Digital Output (CX20220A-1)

In the output stages (pins 3 through 12), a10kΩ pull-down resistors are built in. A 1kΩ or larger resistance can further be connected to it externally.

D1 = MSB, D10 = LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB 1 2 3 4 5 6 8 8 9 10 LSB
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1 1
·	1	1 1 1 1 1 1 1 1 1 0
·	2	1 1 1 1 1 1 1 1 0 1
·	·	·
·	·	·
·	·	·
·	5 1 1	1 0 0 0 0 0 0 0 0 1
·	5 1 2	1 0 0 0 0 0 0 0 0 0
·	5 1 3	0 1 1 1 1 1 1 1 1 1
·	·	·
·	·	·
·	·	·
·	1 0 2 2	0 0 0 0 0 0 0 0 0 1
$V_{REF.B}$	1 0 2 3	0 0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

Digital Output (CX20220A-2)

D1=MSB, D9=LSB.

The table below shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code (binary) MSB 1 2 3 4 5 6 8 8 9 LSB
$V_{REF.T}$	0	1 1 1 1 1 1 1 1 1
·	1	1 1 1 1 1 1 1 1 0
·	2	1 1 1 1 1 1 1 0 1
·	·	·
·	·	·
·	·	·
·	2 5 5	1 0 0 0 0 0 0 0 1
·	2 5 6	1 0 0 0 0 0 0 0 0
·	2 5 7	0 1 1 1 1 1 1 1 1
·	·	·
·	·	·
·	·	·
·	5 1 0	0 0 0 0 0 0 0 0 1
$V_{REF.B}$	5 1 1	0 0 0 0 0 0 0 0 0

1 : V_{OH}
0 : V_{OL}

3

Ground Pin (AGND, DGND)

When mounting the converter on a printed circuit board, take as much space as possible for GND, to reduce impedance and resistance.

Power Supply Pin (VEE)

The VEE pin should be bypassed in the shortest way to AGND with a 0.1 μF or larger ceramic chip capacitor.

Power Supply Pin (Vcc)

This is an internal power supply pin. Three diodes are incorporated in it in series, as shown in the equivalent circuit diagram, and its lower end is connected to AGND. Therefore, any desired Vcc can be obtained by connecting a pull-up resistor to +5V. Be careful not to connect a capacitor between this pin and GND, because oscillation may result.

Reference Voltage Pin

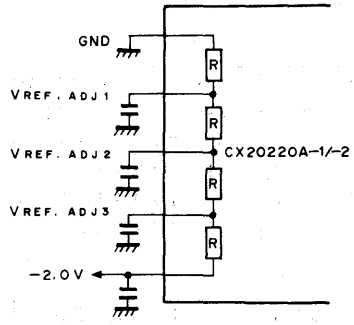
From this pin the reference voltage is supplied to the upper level and lower level comparators. Normally, VREF.T should be connected to GND, and VREF.B to −2.0V, respectively.

The interval between VREF.T and VREF.B constitutes a resistance of approximately 150 Ω, and upon application of −2.0V a current of approximately 13 mA will flow in it.

Any leakage of CLK to the reference voltage, will deteriorate the characteristics of the converter. To avoid this, it should be bypassed to AGND with a tantalum capacitor of 47 μF or over plus a ceramic chip capacitor of 0.1 μF or over.

Linearity Adjusting Pin (VREF.ADJ)

Adjusting pins are extended from reference resistors as shown below. Normally, these pins are connected to AGND with a 0.1 μF or larger ceramic chip capacitor. When adjustments are needed, connect them to AGND or VREF.B via resistance.



Sample & Hold Circuit

As noted in the explanation of the clock timing, it is desirable that the sample and hold circuit has some allowance for TA. A sample and hold circuit based on a diode bridge switch maybe used which performs the best result.

For more information, see Application Circuit (2).

Analog Input

Since CX20220A-1/-2 has an analog input capacitance of approximately 230pF, the buffer amplifier used to drive it must have a sufficient drive capability. Note that, if driven by a low-output-impedance buffer amplifier, a parasitic oscillation may result. This can be prevented by inserting a resistor of about 10 to 30 Ω between the output of the buffer amplifier and the A/D input in series.

Clock Input

The clock input is a complementary configuration.
Normally it should be driven with ECL circuit with complementary output.

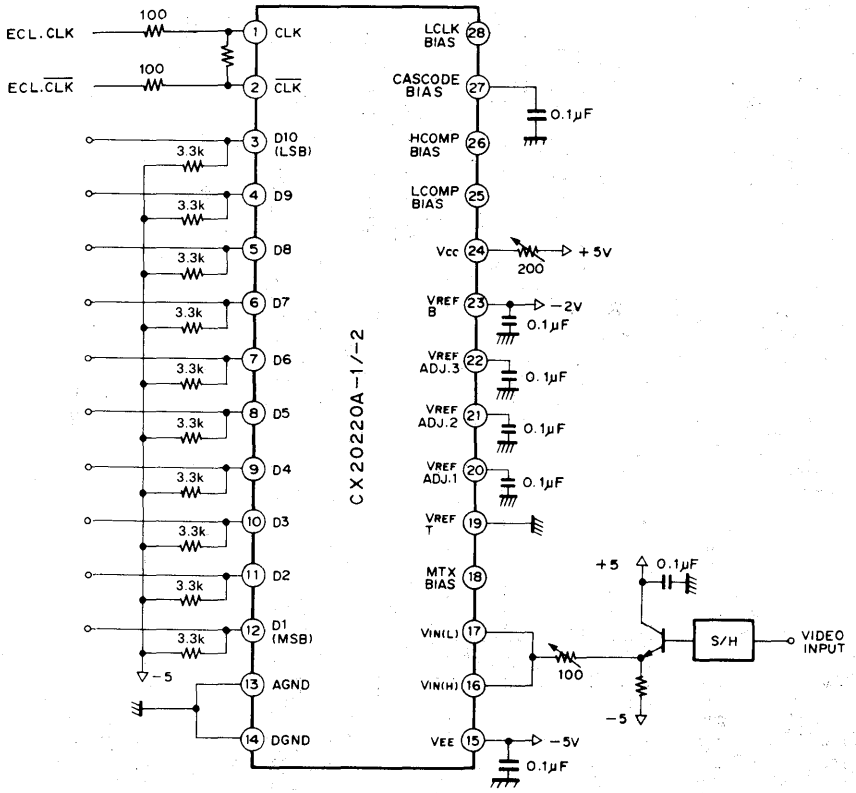
Digital Output (D1 through D10)

Although a 10kΩ pull-down resistor is built into the digital output stage, a 1kΩ or larger resistor can further be connected to it externally. In this case, however, care must be taken about changes in output level.

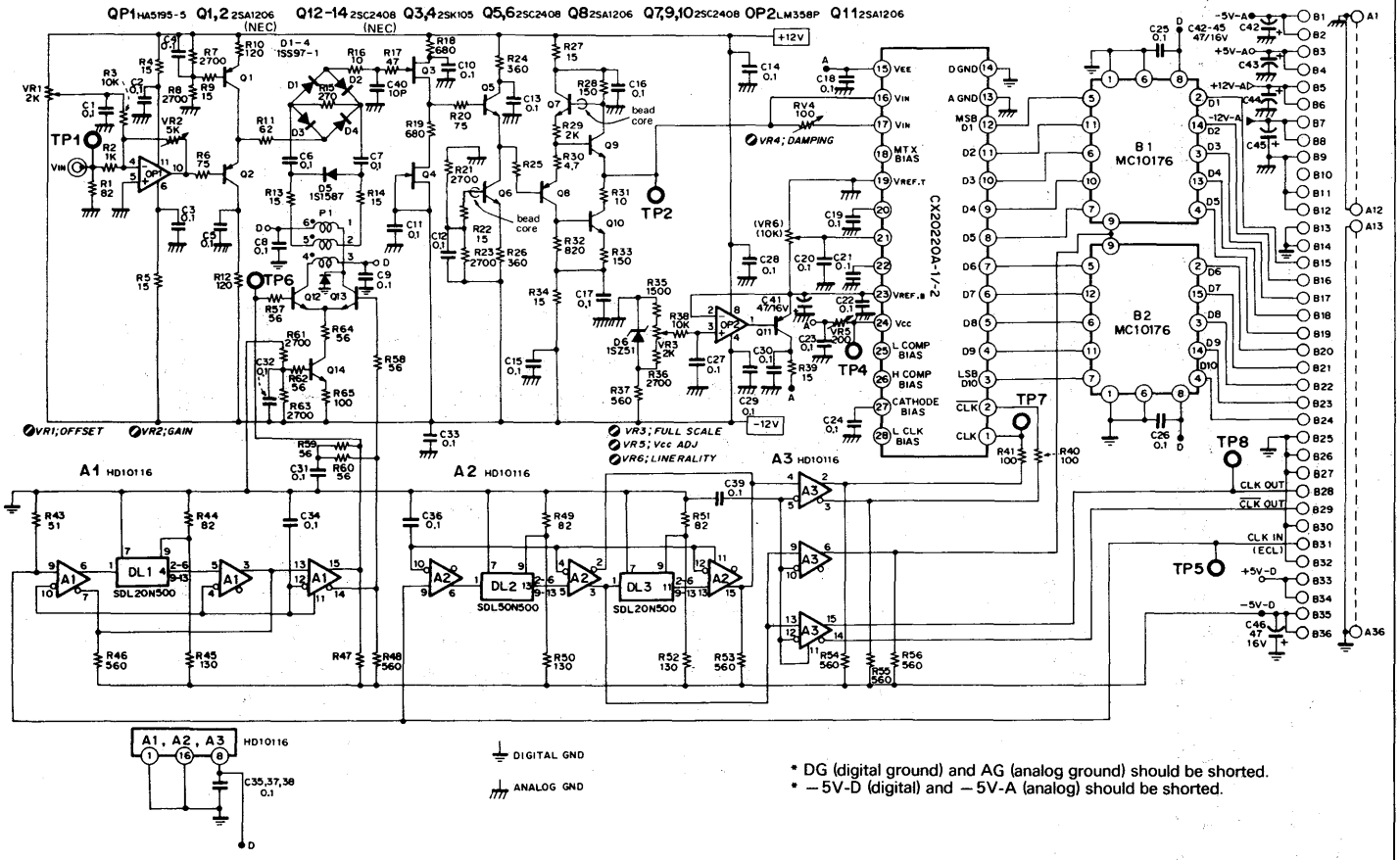
Other

Pin 18 (MTX BIAS), pin 25 (LCOM BIAS), pin 26 (HCOMP BIAS) and pin 28 (LCLK BIAS) are not used. These pins should never be connected to GND, power supply or any other pins.

Application Circuit (1)



Application Circuit (2)



* DG (digital ground) and AG (analog ground) should be shorted.
* −5V-D (digital) and −5V-A (analog) should be shorted.

Comparative Description of the System

CX20220A-1/-2 is based on a new series-parallel type. The following is a comparative explanation of the conventional and the new series-parallel types.

Series-Parallel Type (Conventional)

The series-parallel-type A/D converter is designed to accomplish A/D conversion in two steps, as shown in Fig. 1. With a 10-bit device, the level of the analog signal held in the sample hold (S/H) circuit is converted into a first set of parallel 5-bit digital output. This digital output is at the same time converted back into an analog signal, corresponding to the upper 5 bits. The difference between this signal and the level held at input is converted into digital signals in the parallel 5-bit A/D converter at the next stage, resulting in digital output for the lower 5 bits.

The number of comparators required for this system is $(2^5 - 1) \times 2 = 62$ pcs., bringing about a dramatic reduction in circuit size as compared to the 10-bit parallel type. However, since it does A/D conversion twice, once for the upper level and then again for the lower level, it takes longer conversion time, and also requires an S/H circuit to hold the input analog signal so that its level does not change when the lower 5 bits, are being converted, in addition both the 5-bit D/A converter and the subtractor, shown in Fig. 1, are required to possess a 10-bit equivalent accuracy.

New Series-Parallel Type

Essentially the new series-parallel-type A/D converter aims to reduce the number of comparators by doing A/D conversion twice, once for the upper bits and again for the lower bits, as in the case of the conventional series-parallel type. The distinguishing feature of this system, however, is that it does not require the D/A converter and the subtractor as shown in Fig. 2. Simply speaking this system is designed so that the input level held in the S/H circuit is first A/D converted for the upper 5 bits, and upon receipt of control signal from the upper level encoder, the lower level A/D converter is operated.

To simplify the operating principle of this system, Fig. 3 shows an example which consists of an upper 2 bits and lower 2 bits, a total of 4 bits. The upper and lower level circuits each consist of three comparators, switch trains S1 through S4, a single 16-segmented resistor, and an encoder.

Input level V_{IN} held by the S/H circuit is determined by the upper level comparator to be at a level of $V_{REF.T}$ to V_1, V_1 to V_1 to V_2, V_2 to V_3, or V_3 to $V_{REF.B.}$ The result of judgement is converted into upper 2-bit digital output through the upper level encoder. At the same time, one of the switch trains S1 to S4 is turned on, according to the level of V_{IN}. As it switches on, reference voltage is supplied to the lower level comparator, and elaborate comparative judgement is made at the interval of (V_{REF}/4), resulting in output of the lower 2 bits from the lower level encoder.

Since this system uses the same resistor strings in common for the upper and lower levels, simplicity is maintained. Furthermore, since this system requires fewer comparators, input bias current for the comparators is reduced accordingly.

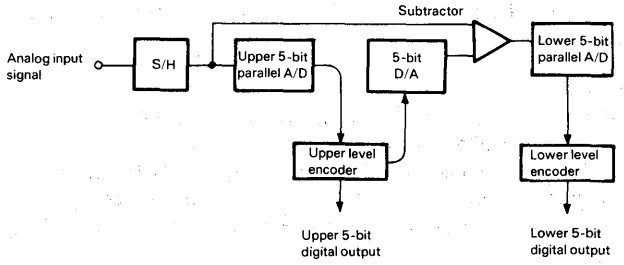


Fig. 1 Configuration of Series-Parallel 10-Bit A/D Converter

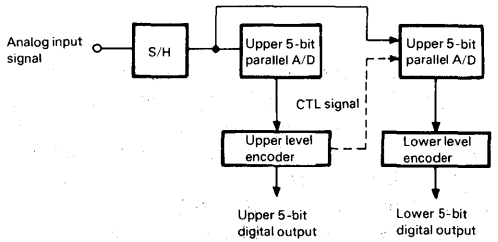


Fig. 2 Configuration of the New Series-Parallel 10-Bit A/D Converter

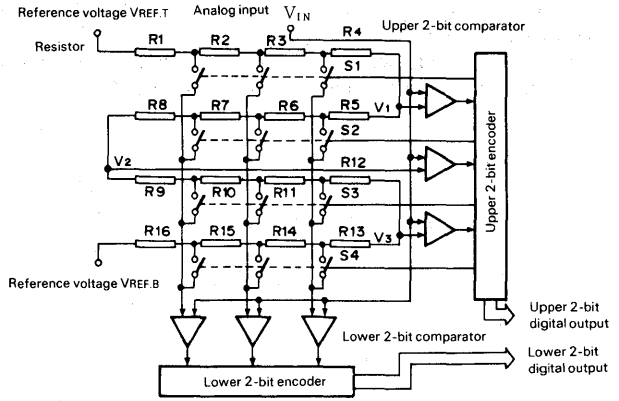
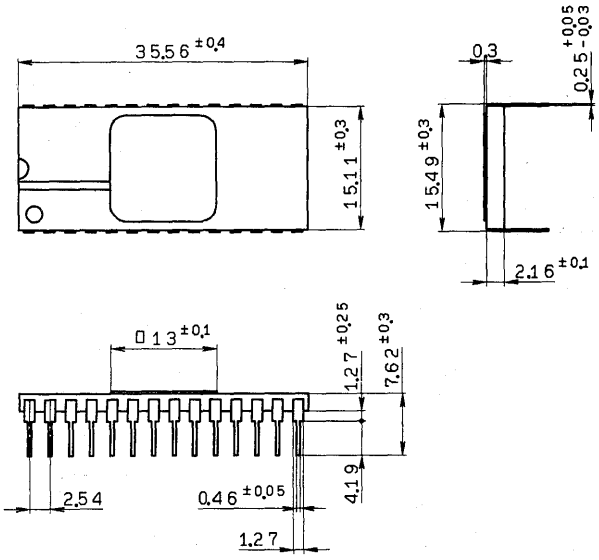


Fig. 3 Operating Principle of the New Series-Parallel Type (Ex.: 4-bit device)

Package Outline Unit : mm

28pin DIP(Ceramic) 600mil 4.8g



DIP-28C-01

3

SONY

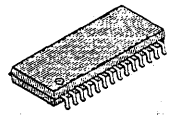
CXA1096M

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Description

The CXA1096M is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

28pin SOP(Plastic)



Features

- Resolution 8-bit ±1/2 LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (−3dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 390mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Over range output

Structure

Bipolar silicon monolithic IC

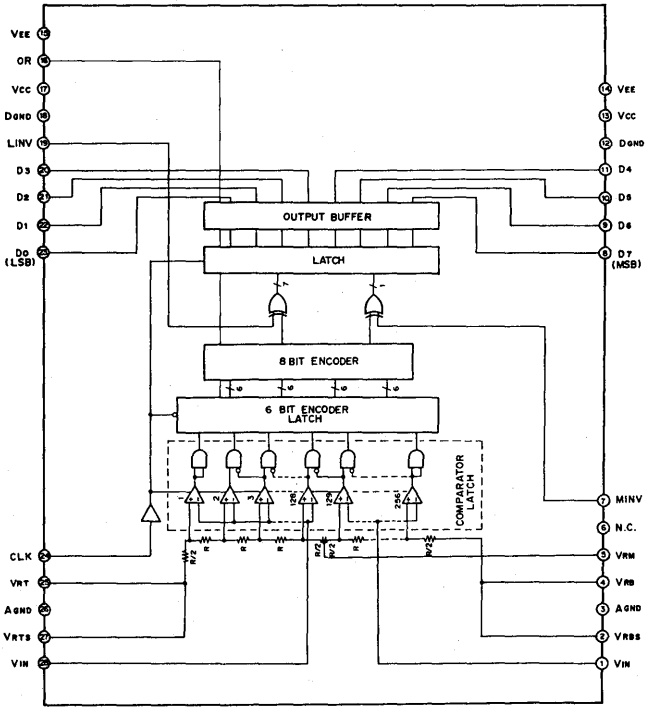
Applications

- Digital TV
- High speed signal processing

Function

8-bit, 20MSPS flash A/D converter

Block Diagram



E89645-HP

Absolute Maximum Ratings (Ta = 25°C)

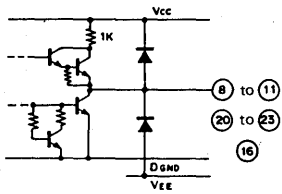
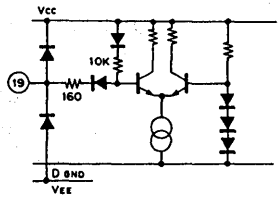
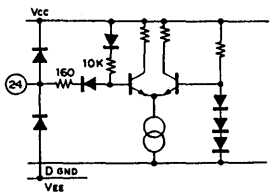
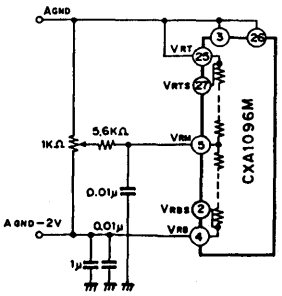
• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage (analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV	D_{GND} −0.5 to V_{CC}	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.83	W

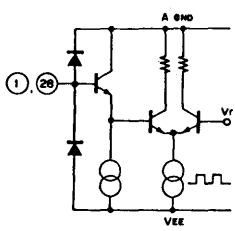
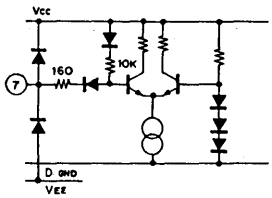
Recommended Operating Conditions

• Supply voltage (Single supply)	V_{CC}, A_{GND}	4.75 to 5.25	V
	D_{GND}, V_{EE}	0	V
(Dual supply)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PWO}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

3

Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
8 to 11 20 to 23	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
16	OR			Over range output pin
12, 18	DGND	GND		Digital GND. Separated from AGND.
13, 17	Vcc	5V (Typ.)		Digital power supply
14, 15	VEE	GND (Single supply) – 5V (Dual supply)		Analog power supply
19	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Input-Output Reference and Output Format) when open "1" is maintained.
24	CLK	TTL		Clock input pin
25	VRT	5V (Typ.) (Single supply)		Reference voltage (Top)
27	VRTS	GND (Dual supply)		Reference voltage sense (Top)
4	VRB	3V (Typ.) (Single supply) – 2V (Typ.) (Dual supply)		Reference voltage (Bottom)
2	VRBS			Reference voltage sense (Bottom)
5	VRM	4V (Typ.) (Single supply) – 1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity

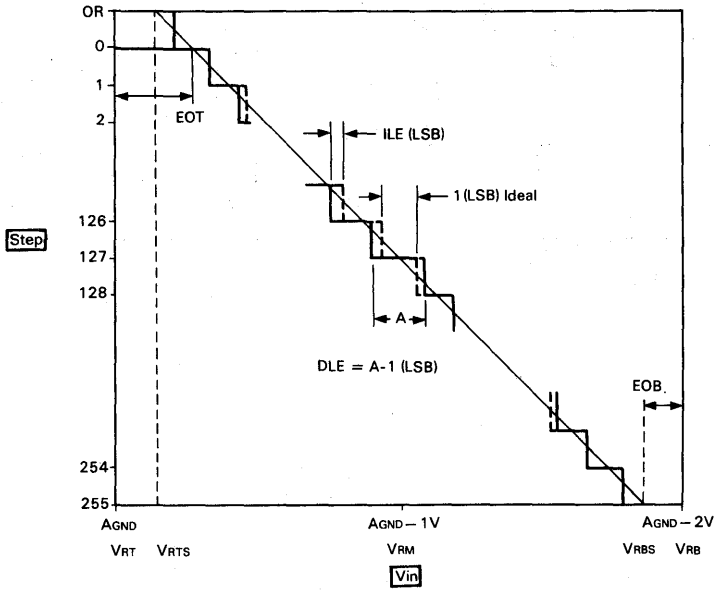
No.	Symbol	Voltage	Equivalent circuit	Description
3, 26	AGND	5V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
1, 28	VIN	VRT to VRB		Analog input Pin 1 and 28 should be connected together.
7	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

3

Input-Output Reference and Output Format

Vin	Step	MINV 1 LINV 1 OR MSB LSB	1 0 OR MSB LSB	0 1 OR MSB LSB	0 0 OR MSB LSB
AGND		0 000···00	0 011···11	0 100···00	0 111···11
	0	1 000···00	1 011···11	1 100···00	1 111···11
	1	1 000···01	1 011···10	1 100···01	1 111···10
AGND −1V	127	1 011···11	1 000···00	1 111···11	1 100···00
	128	1 100···00	1 111···11	1 000···00	1 011···11
	254	1 111···10	1 100···01	1 011···10	1 000···01
AGND −2V	255	1 111···11	1 100···00	1 011···11	1 000···00
		1 111···11	1 100···00	1 011···11	1 000···00

1: V_{IH}, V_{OH}
0: V_{IL}, V_{OL}



Electrical Characteristics (Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V, V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		FC	VIN = 5 to 3V FIN = FC/4 – 1 kHz		20			MSPS
Supply current		ICC + IEE			56	71	91	mA
Reference pin current		IREF			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		CIN	VIN = 4V + 0.07Vms			30	35	pF
Analog input bias current		IIN	VIN = 4V		15	50	110	μA
Reference resistance (VRT to VRB)		RREF				130		Ω
Offset voltage	VRT	EOT			8	13	19	mV
	VRB	EOB			0	5	11	mV
Digital input voltage		VIH			2.0			V
		VIL					0.8	V
Digital input current		IIH	VCC = Max.	VIH = 2.7V	0	–100	–150	μA
		IIL		VIL = 0.5V	–0.1	–0.32	–0.5	mA
Digital output voltage		VOH	VCC = Min.	IOH = –500μA	2.7	3.4		V
		VOL		IOL = 3mA			0.5	V
Output data delay		TDLH	LOAD 1		15	19	22	ns
		TDHL			22	27	31	ns
Non linearity		EL	FC = 20 MSPS VIN = 5 to 3V				± 1/2	LSB
Differential non linearity		ED					± 1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, FC = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		EAP				30		ps
Sampling delay		tds			5	7	9	ns

3

Electrical Characteristics (Dual supply)

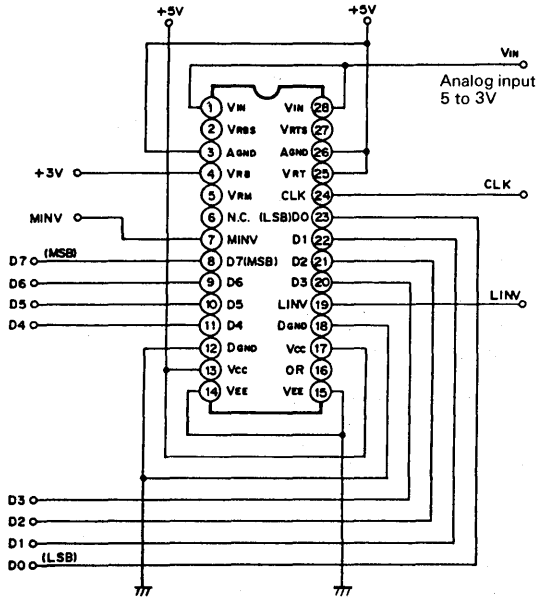
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		F_C	V_{IN} = 0 to −2V F_{IN} = $F_C/4$ − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	62	78	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		E_L	F_C = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		E_D					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, F_C = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

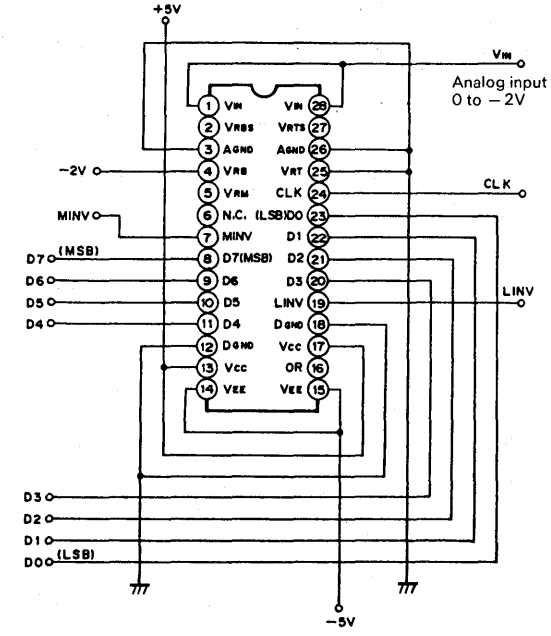
Application Circuit and Electrical Characteristics Test Circuit

1)

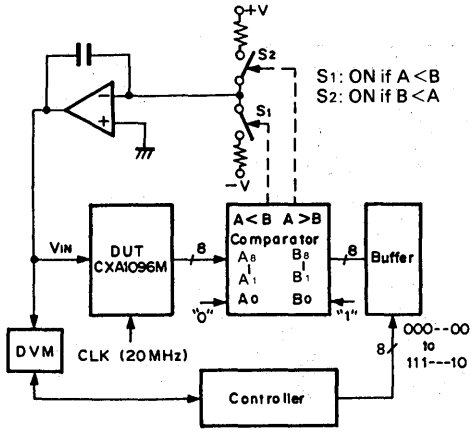
Single supply



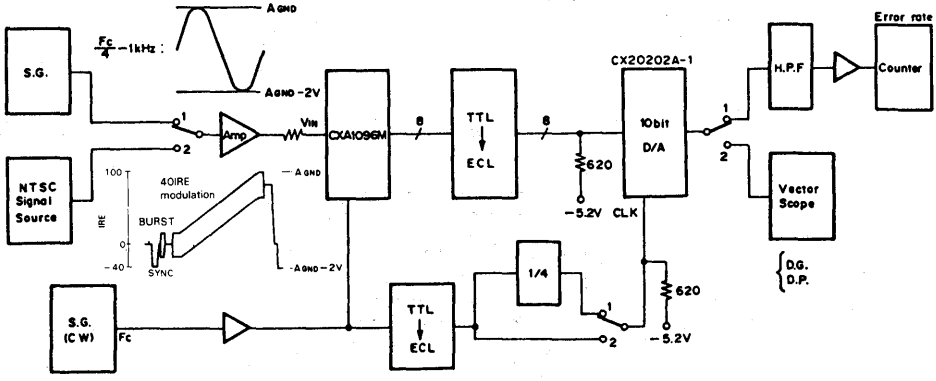
Dual supply



3

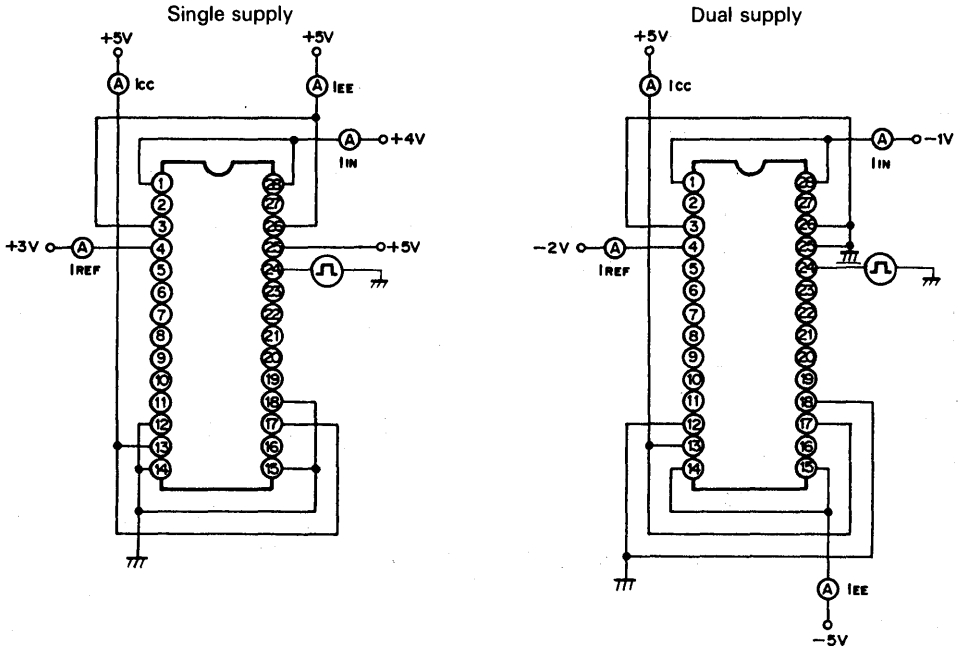


Non linearity
Differential non linearity
} Test circuit



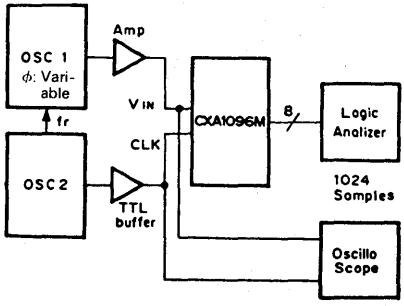
Maximum conversion rate
Differential gain error
Differential phase error
} Test circuit

2)

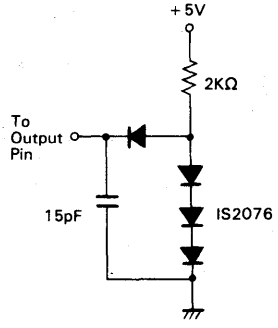


Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

Supply current
Analog input bias current
Reference pin current
} Test circuit

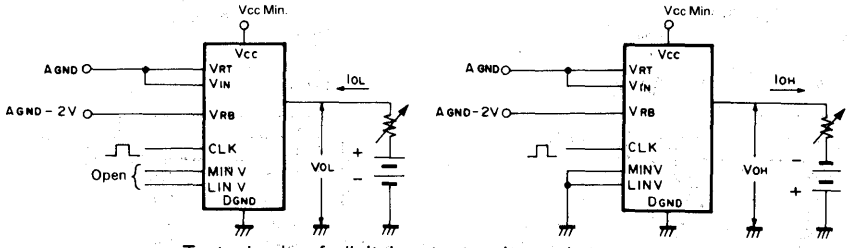


Aperture jitter
Sampling delay
} Test circuit

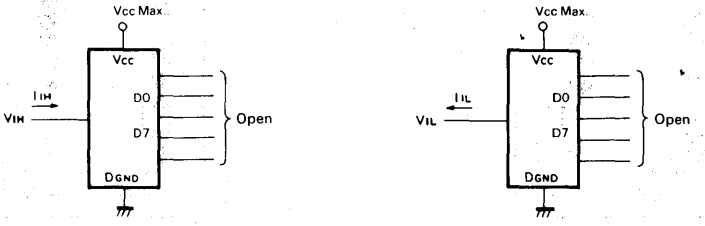


LOAD1 Test Load for Output data delay

3)

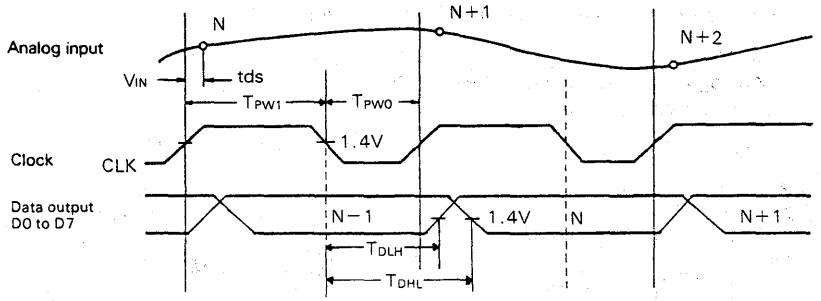


Test circuit of digital output voltage (D0 to D7, OR)

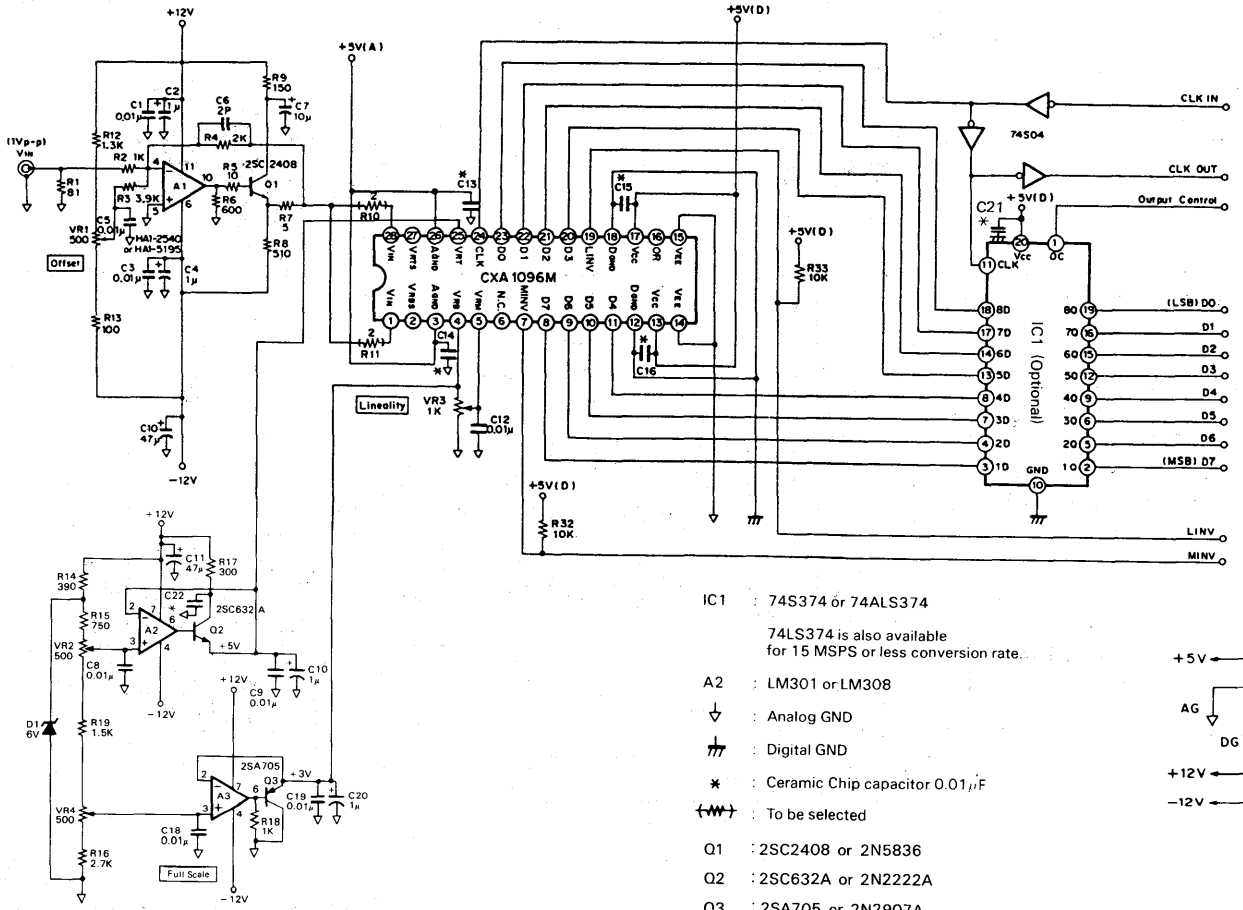


Test circuit of digital input current (CLK, MINV, LINV)

Timing Chart



Application Circuit (Single supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

⏚ : Analog GND

⏚ : Digital GND

* : Ceramic Chip capacitor 0.01 μF

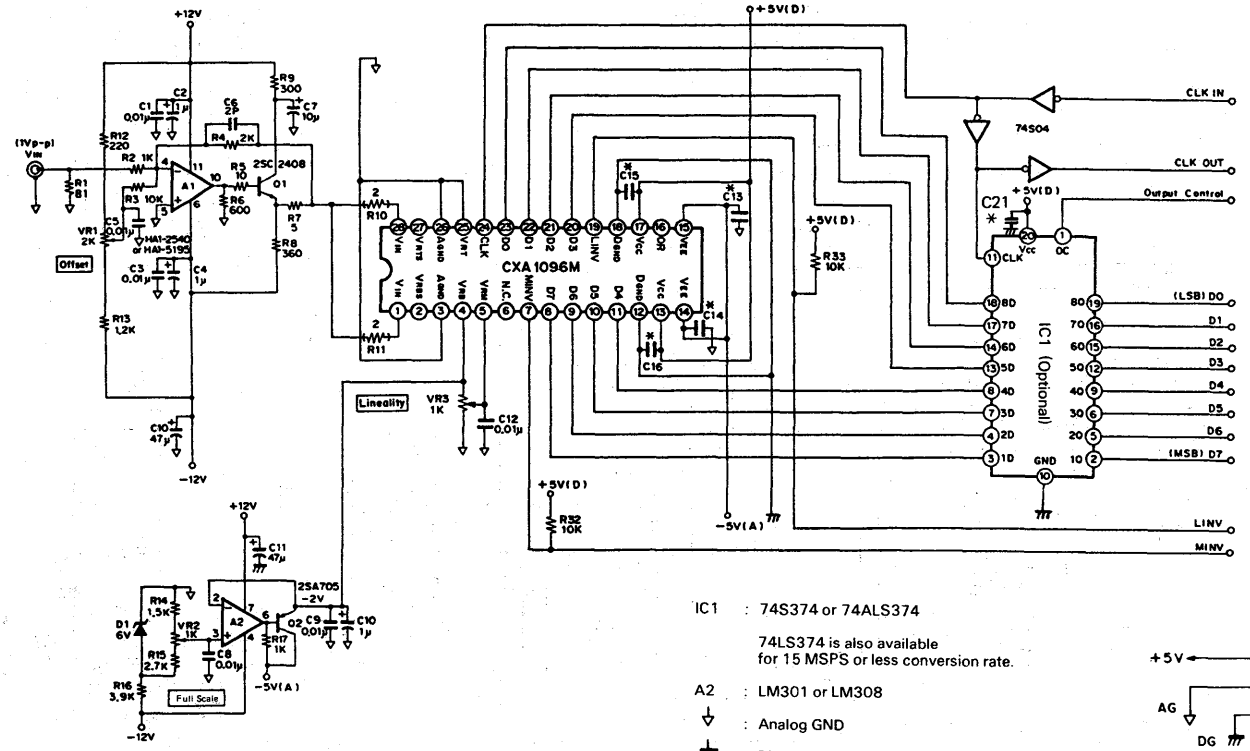
⟿ : To be selected

Q1 : 2SC2408 or 2N5836

Q2 : 2SC632A or 2N2222A

Q3 : 2SA705 or 2N2907A

Application Circuit (Dual supply)



IC1 : 74S374 or 74ALS374

74LS374 is also available for 15 MSPS or less conversion rate.

A2 : LM301 or LM308

: Analog GND

: Digital GND

* : Ceramic Chip capacitor 0.01µF

: To be selected

Q1 : 2SC2408 or 2N5836

Q2 : 2SA705 or 2N2907A

+5V
AG
DG
-5V
+12V
-12V

Notes on Application

1. Each of DGND pins (12, 18) and each of VCC Pins (13, 17) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.
   Pins VIN (1, 28) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

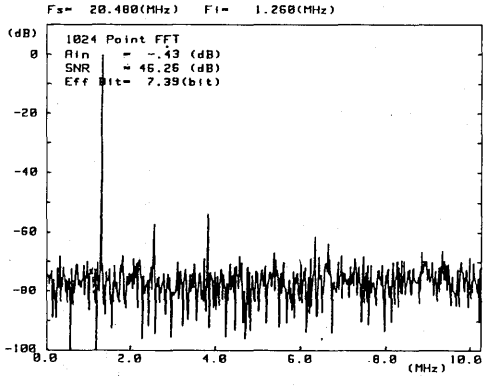
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

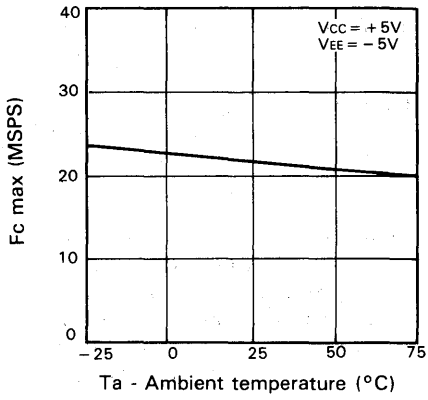
6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).
   If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

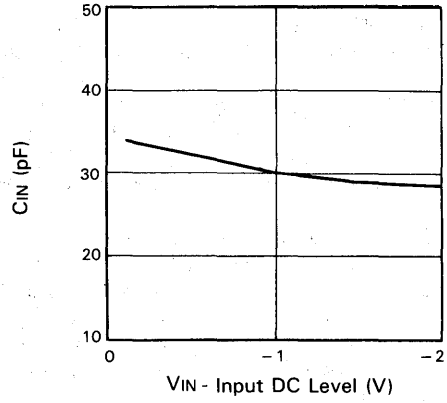
FFT data



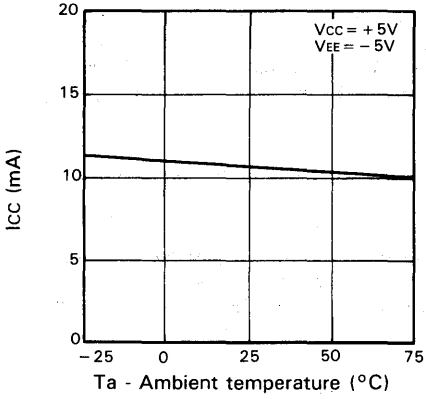
Fc max vs. Ambient temperature



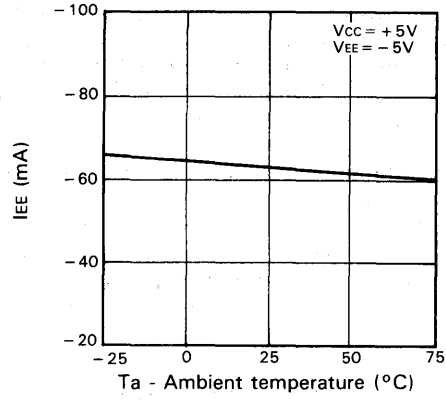
CIN vs. VIN - Input DC level



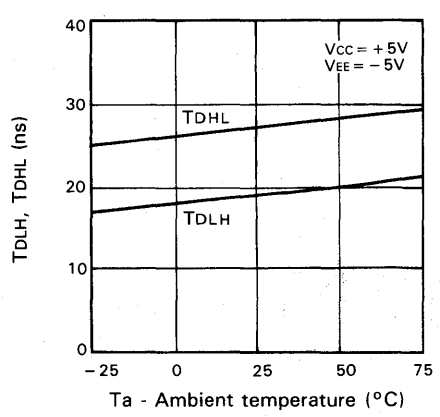
ICC vs. Ambient temperature



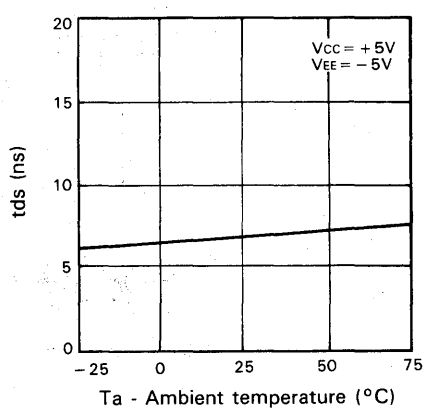
IEE vs. Ambient temperature



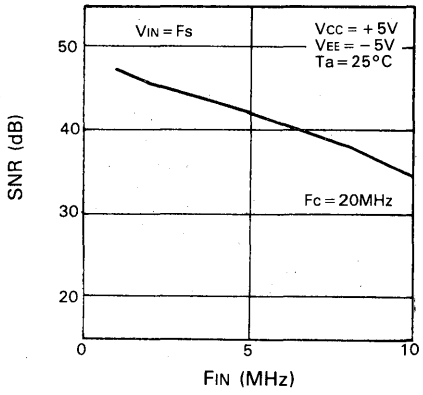
TDLH, TDHL vs. Ambient temperature



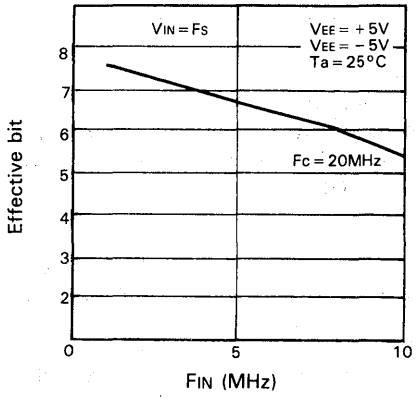
tds vs. Ambient temperature



SNR vs. FIN

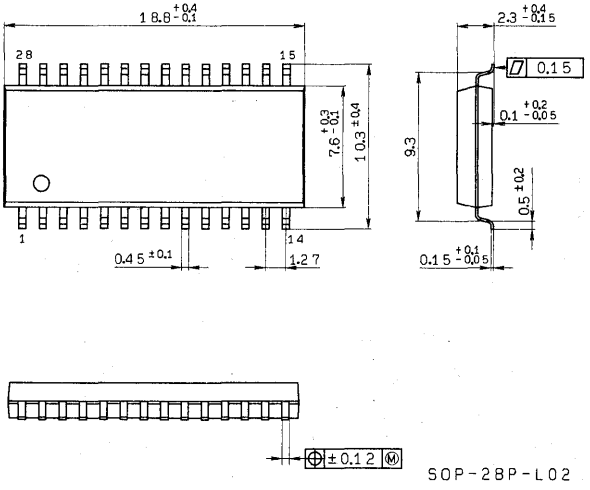


Effective bit vs. FIN



Package Outline Unit : mm

28pin SOP(Plastic) 375mil 0.6g



SONY

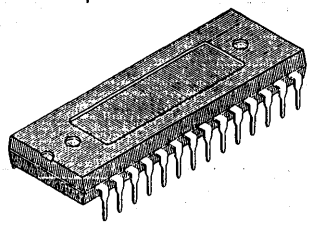
CXA1096P

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Description

CXA1096P is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

28pin DIP(Plastic)



Features

- Resolution 8-bit ±1/2 LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (−3dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 390mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Pin replacable with TDC1048 (TRW)

Structure

Bipolar silicon monolithic IC

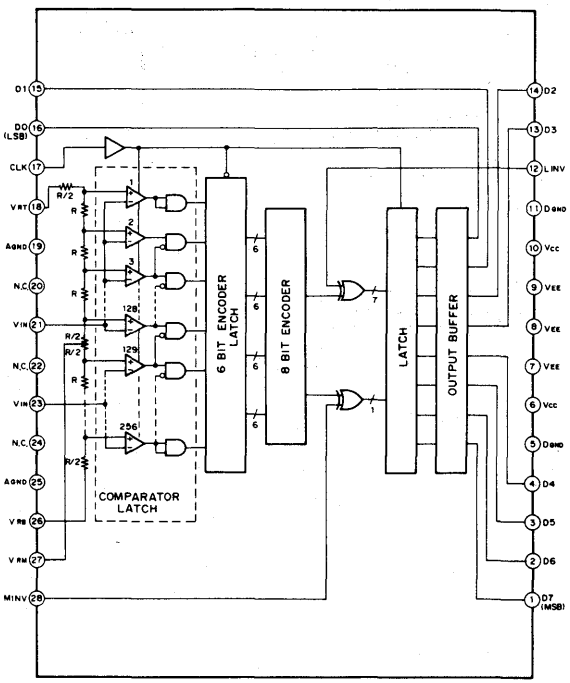
Applications

- Digital TV
- High speed signal processing

Function

8-bit, 20MSPS flash A/D converter

Block Diagram



E89646-HP

Absolute Maximum Ratings (Ta = 25°C)

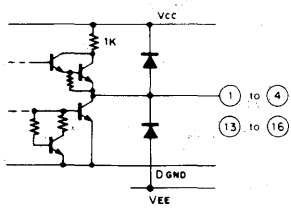
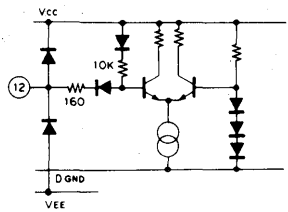
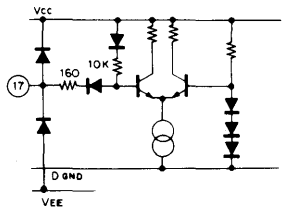
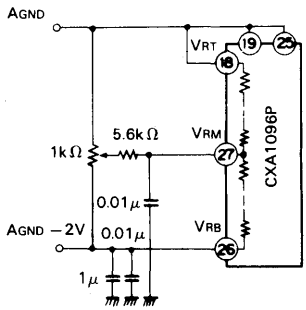
• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage(analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV	D_{GND} −0.5 to V_{CC}	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.48	W

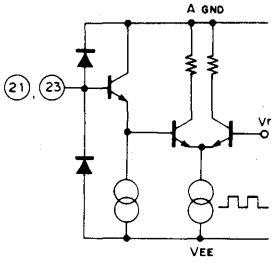
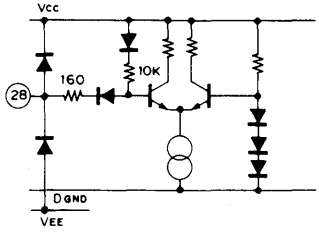
Recommended Operating Conditions

• Supply voltage (Single supply)	V_{CC}, A_{GND}	4.75to5.25	V
	D_{GND}, V_{EE}	0	V
(Dual supply)	V_{CC}	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PWO}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

3

Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
1 to 4 13 to 16	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
5, 11	DGND	GND		Digital GND. Separated from AGND.
6, 10	Vcc	5V (Typ.)		Digital power supply
7,8,9	VEE	GND (Single supply) −5V (Dual supply)		Analog power supply
12	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Output Coding) when open "1" is maintained.
17	CLK	TTL		Clock input pin
18	VRT	5V (Typ.) (Single supply) GND (Dual supply)		Reference voltage (Upper level)
26	VRB	3V (Typ.) (Single supply) −2V (Typ.) (Dual supply)		Reference voltage (Lower level)
27	VRM	4V (Typ.) (Single supply) −1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity

No.	Symbol	Voltage	Equivalent circuit	Description
19, 25	AGND	5V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
21, 23	VIN	VRT to VRB		Analog input Pin 21 and 23 should be connected together.
28	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

3

Output Coding

MINV	0	0	1	1
LINV	0	1	0	1
AGND	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
AGND-2V	000...00	011...11	100...00	111...11

1 : V_{IH}, V_{OH}
0 : V_{IL}, V_{OL}

Electrical Characteristics (Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V, V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 5 to 3V F_{IN} = $F_C/4$ − 1 kHz		20			MSPS
Supply current		I_{CC} + I_{EE}			56	71	91	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = 4V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = 4V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		EL	Fc = 20 MSPS V_{IN} = 5 to 3V				±1/2	LSB
Differential non linearity		ED	Fc = 20 MSPS				±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		EAP				30		ps
Sampling delay		tds			5	7	9	ns

Electrical Characteristics (Dual supply)

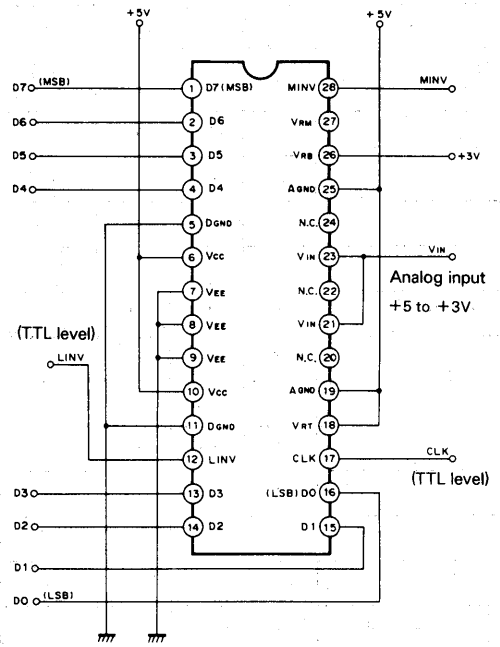
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V,
V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		F_C	V_{IN} = 0 to −2V F_{IN} = $F_C/4$ − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	62	78	mA
Reference pin current		I_{REF}			11	15	18	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	110	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				130		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	−0.1	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		15	19	22	ns
		T_{DHL}			22	27	31	ns
Non linearity		E_L	F_C = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		E_D	F_C = 20 MSPS				±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, F_C = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			5	7	9	ns

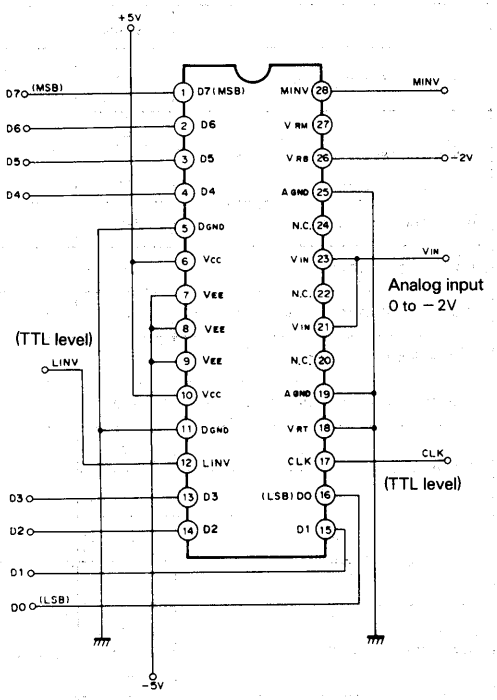
3

Application Circuit

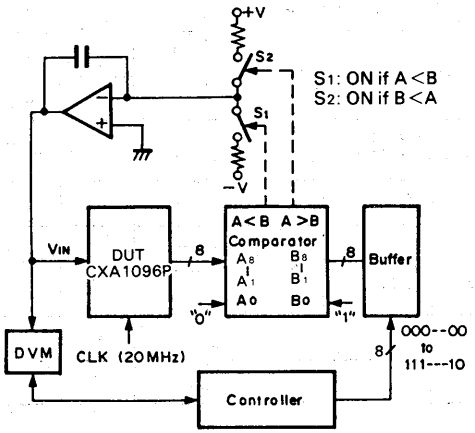
Single supply



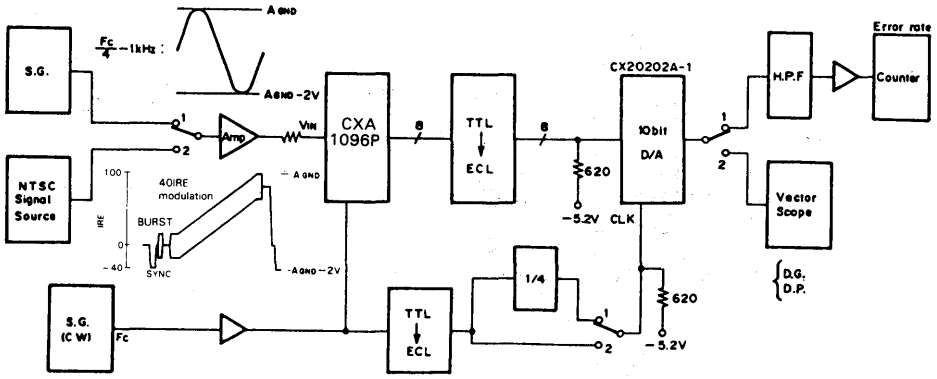
Dual supply



Electrical Characteristics Test Circuit

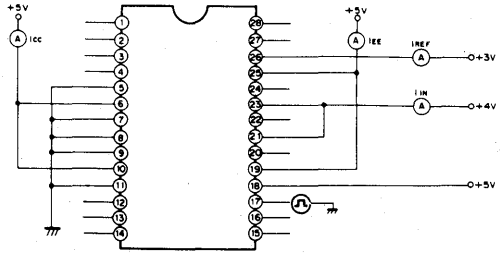


Non linearity
Differential non linearity } Test circuit

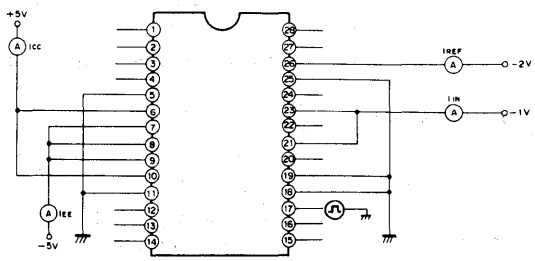


Maximum conversion rate
Differential gain error
Differential phase error
} Test circuit

Single supply

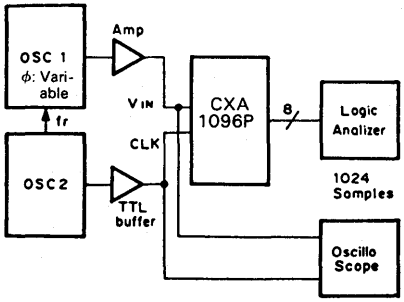


Dual supply

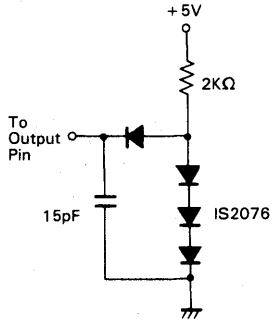


Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

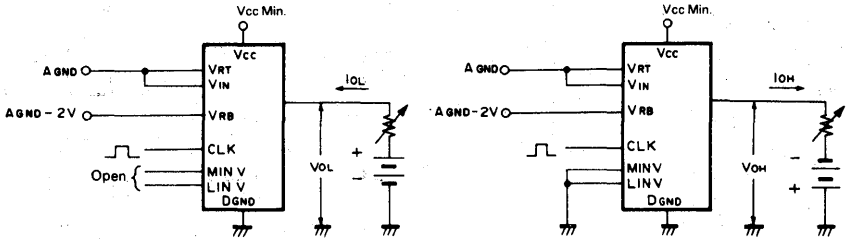
Supply current
Analog input bias current
Reference pin current
} Test circuit



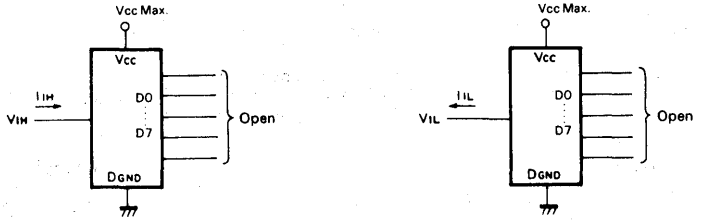
Aperture jitter
Sampling delay
} Test circuit



LOAD1 Test Load for Output data delay

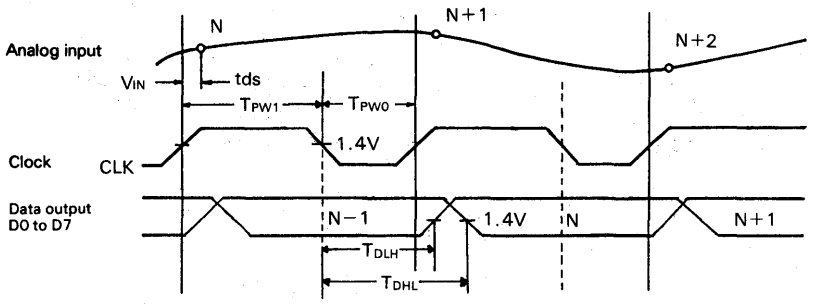


Test circuit of digital output voltage (D0 to D7)

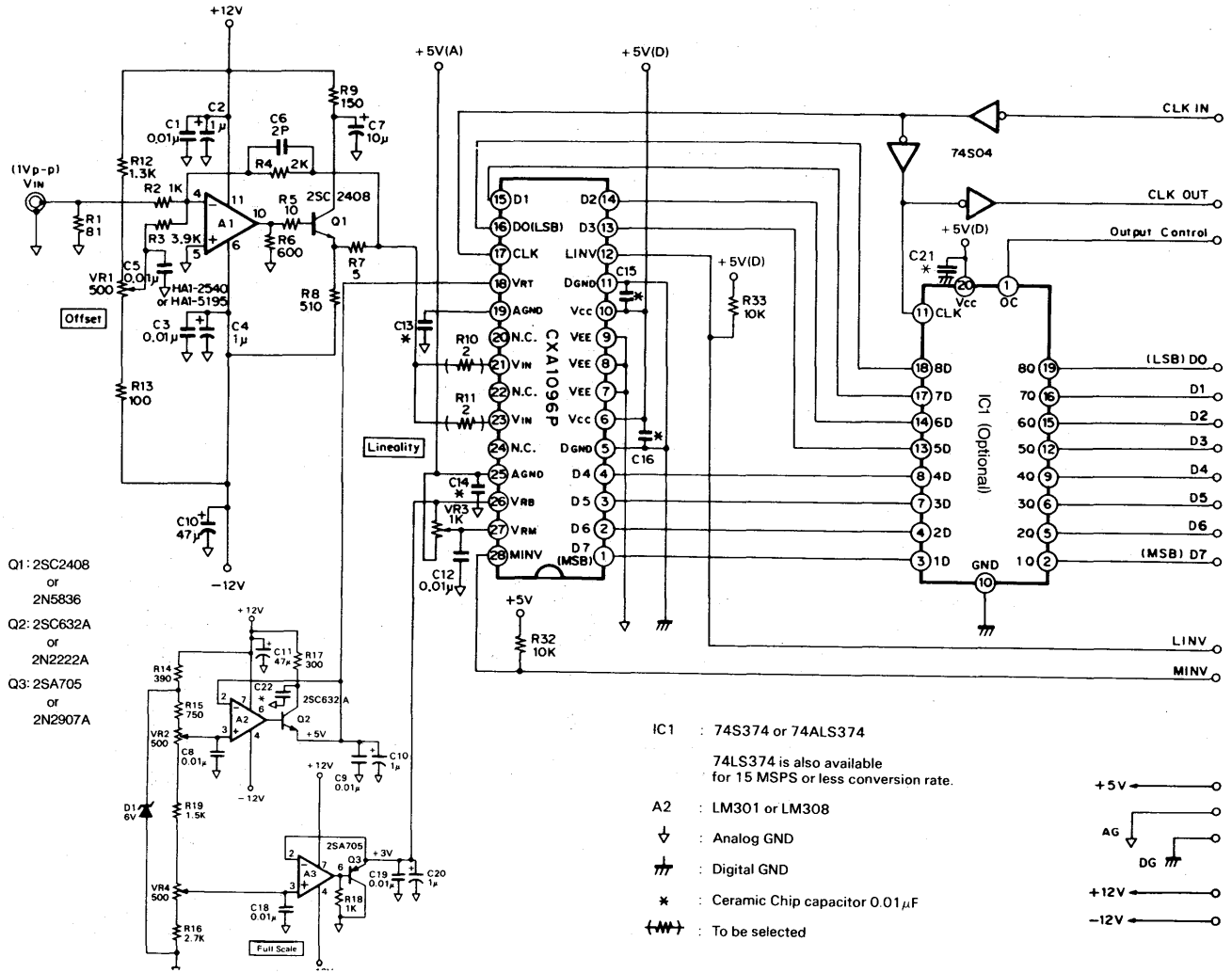


Test circuit of digital input current (CLK, MINV, LINV)

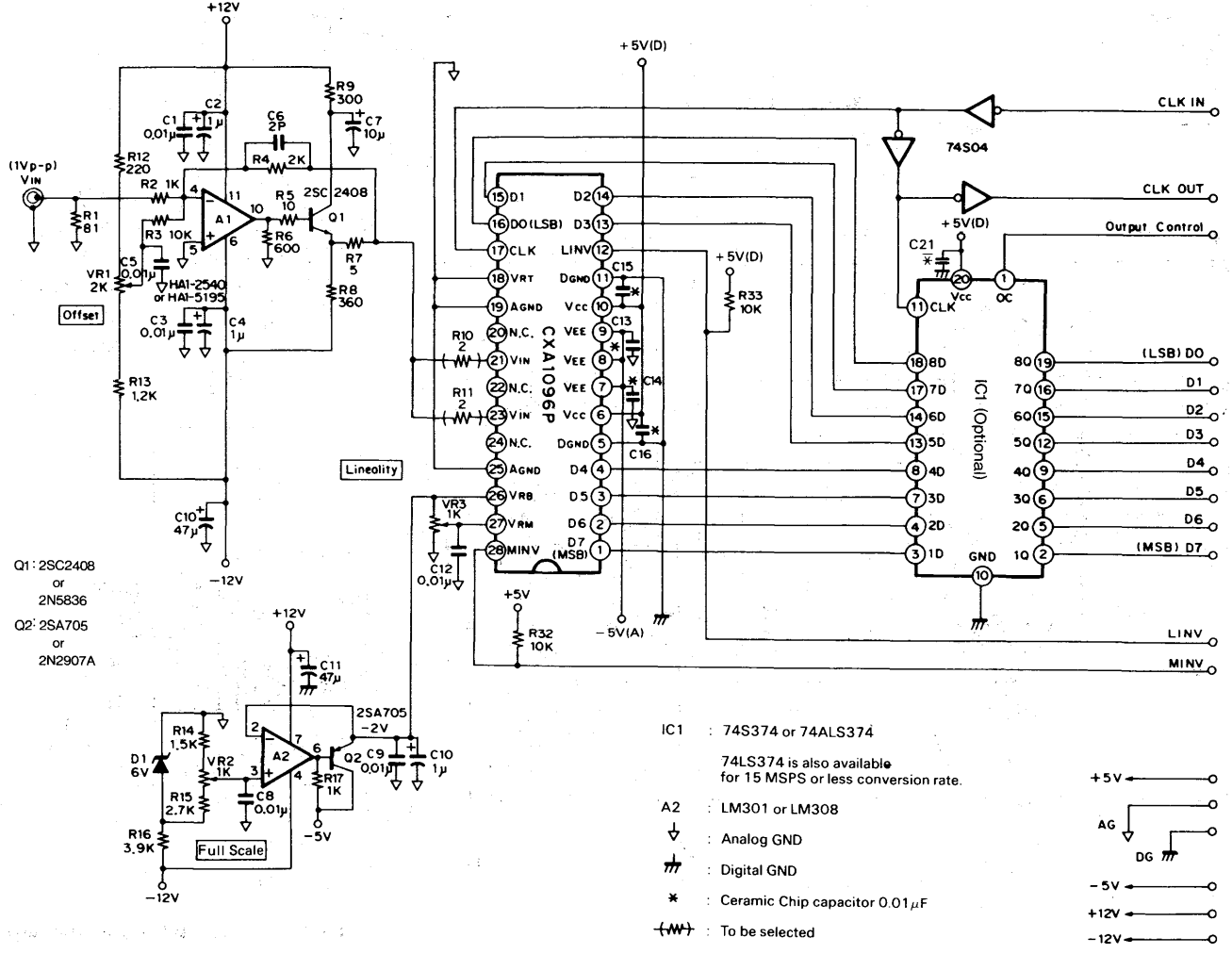
Timing Chart



Application Circuit (Single supply)



Application Circuit (Dual supply)



Notes on Application

1. Each of DGND pins (5, 11) and each of VCC Pins (6, 10) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.
   Pins VIN (21, 23) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

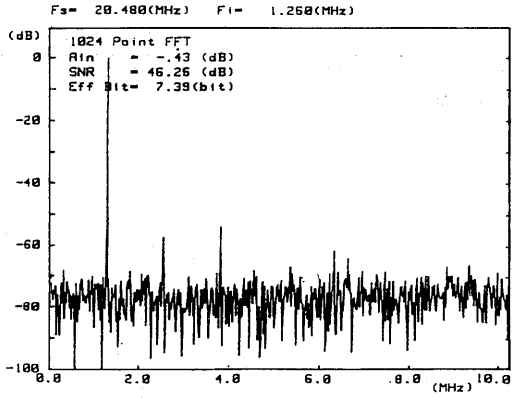
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

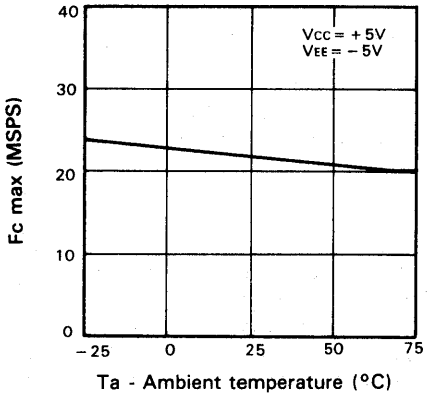
6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).
   If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

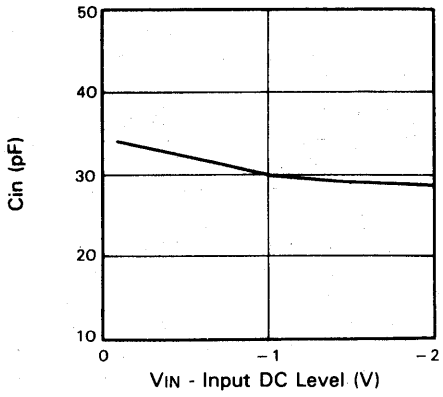
FFT Data



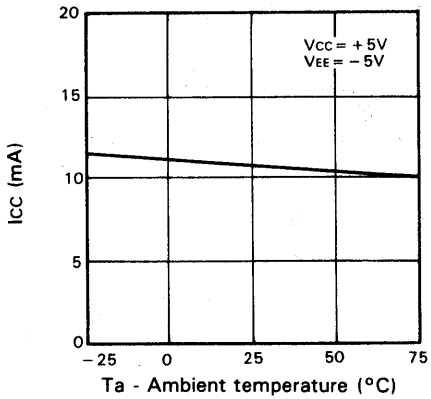
Fc max vs. Ambient temperature



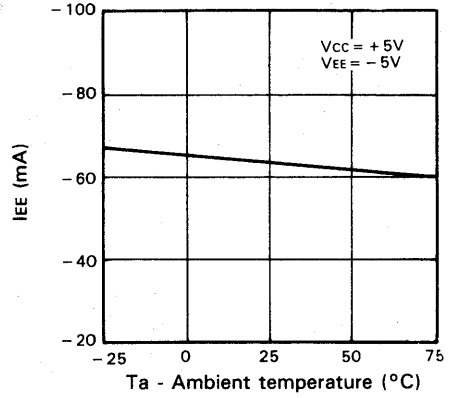
CIN vs. VIN - Input DC level



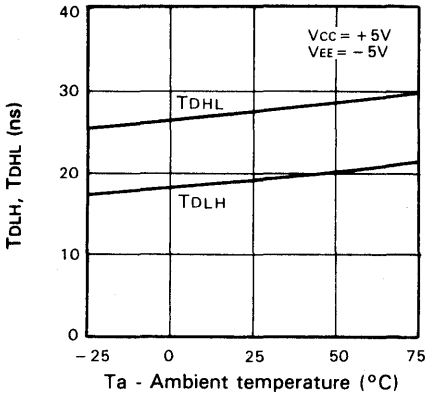
ICC vs. Ambient temperature



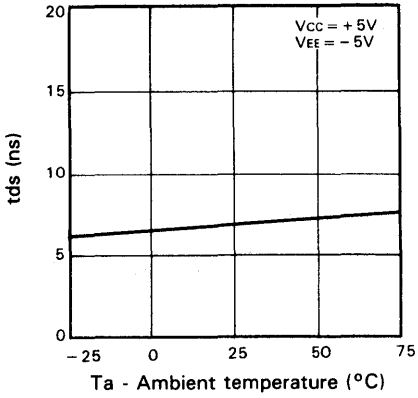
IEE vs. Ambient temperature



TDLH, TDHL vs. Ambient temperature

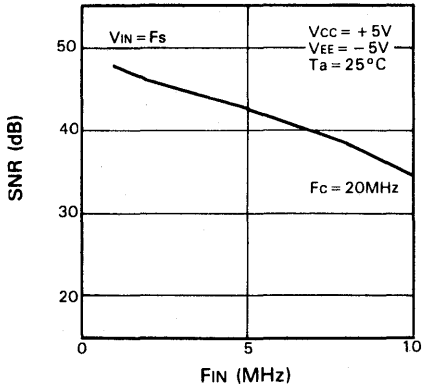


tds vs. Ambient temperature

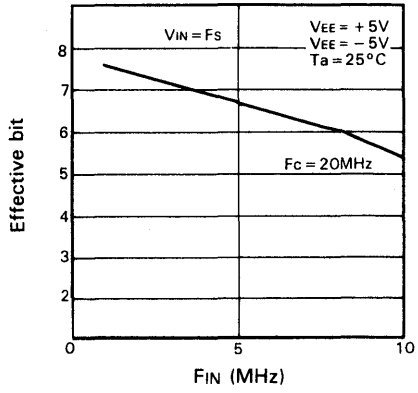


3

SNR vs. FIN

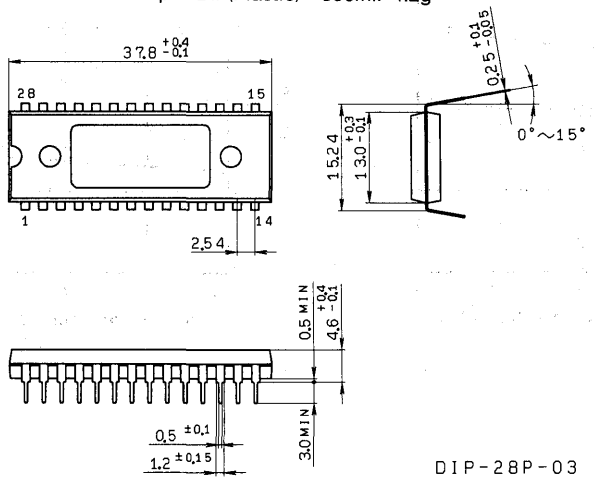


Effective bit vs. FIN



Package Outline Unit : mm

28pin DIP(Plastic) 600mil 4.2g



DIP-28P-03

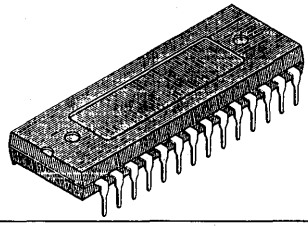
SONY CXA1296P

8-bit 20 MSPS Flash A/D Converter (TTL I/O)

Description

CXA1296P is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

28pin DIP (Plastic)



Features

- Resolution 8-bit ±1/2 LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz (−3dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 410mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/−5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Pin replaceable with TDC1048 (TRW)

Structure

Bipolar silicon monolithic IC

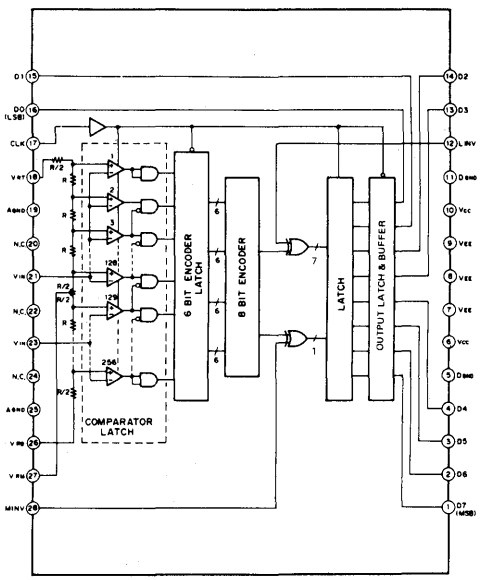
Applications

- Digital TV
- High speed signal processing

Function

8-bit, 20MSPS flash A/D converter

Block Diagram



E89214A96-HP

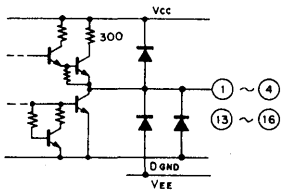
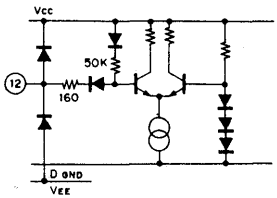
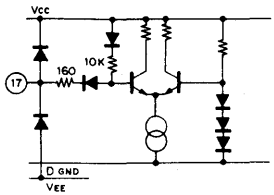
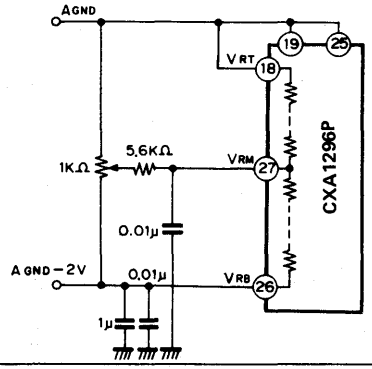
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC}-D_{GND}$	0 to +6	V
	$V_{EE}-A_{GND}$	0 to −6	V
	$A_{GND}-D_{GND}$	0 to +6	V
• Input voltage (analog)	V_{IN}	V_{EE} to A_{GND} +0.3	V
• Input voltage (reference)	V_{RT}, V_{RB}, V_{RM}	V_{EE} to A_{GND} +0.3	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Input current (V_{RM})	I_{VRM}	−3 to +3	mA
• Input voltage (digital)	CLK, MINV, LINV D_{GND}	−0.5 to Vcc	V
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	P_D	1.48	W

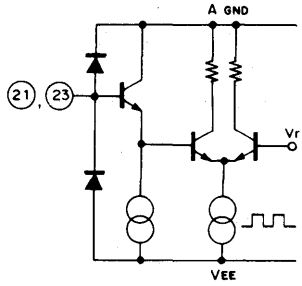
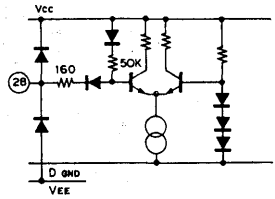
Recommended Operating Conditions

• Supply voltage	Vcc, A_{GND}	4.75 to 5.25	V
(Single supply)	D_{GND}, V_{EE}	0	V
(Dual supply)	Vcc	4.75 to 5.25	V
	V_{EE}	−5.5 to −4.75	V
	D_{GND}, A_{GND}	0	V
• Reference input	V_{RT}	A_{GND} −0.1 to A_{GND} +0.1	V
	V_{RB}	A_{GND} −2.2 to A_{GND} −1.8	V
• Analog input	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PW1}	35 (Min.)	ns
	T_{PW0}	10 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

Pin Description and Equivalent Circuit

No.	Symbol	Voltage	Equivalent circuit	Description
1 to 4 13 to 16	D0 to D7	TTL		Digital data output pin D0 (LSB) to D7 (MSB)
5, 11	DGND	GND		Digital GND. Separated from AGND.
6, 10	Vcc	5V (Typ.)		Digital power supply
7, 8, 9	VEE	GND (Single supply) −5V (Dual supply)		Analog power supply
12	LINV	TTL		Input pins for output polarity inversion of D0 (LSB) to D6 (See the Output Coding) when open "1" is maintained.
17	CLK	TTL		Clock input pin
18	VRT	5V (Typ.) (Single supply) GND (Dual supply)		Reference voltage (Upper level)
26	VRB	3V (Typ.) (Single supply) −2V (Typ.) (Dual supply)		Reference voltage (Lower level)
27	VRM	4V (Typ.) (Single supply) −1V (Typ.) (Dual supply)		Middle point of reference voltage can be used as the compensation pin for linearity.

3

No.	Symbol	Voltage	Equivalent circuit	Description
19, 25	AGND	5 V (Typ.) (Single supply) GND (Dual supply)		Analog power supply
21, 23	VIN	VRT to VRB		Analog input Pin 21 and 23 should be connected together.
28	MINV	TTL		Input pin for output polarity inversion of D7 (MSB) when open "1" is maintained.

Output Coding

MINV LINV	0 0	0 1	1 0	1 1
AGND	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
AGND-2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1: VIH, VOH
0: VIL, VOL

Electrical Characteristics
(Single supply)

V_{CC} = +5V, DGND = 0V, AGND = +5V, V_{EE} = 0V,
V_{RT} = +5V, V_{RB} = +3V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc	V_{IN} = 5 to 3V F_{IN} = $F_{C/4}$ − 1 kHz		20			MSPS
Supply current		I_{CC} + I_{EE}			56	74	93	mA
Reference pin current		I_{REF}			12	16	20	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = 4V + 0.07Vrms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = 4V		15	50	115	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				125		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	0	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		14	18	24	ns
		T_{DHL}			21	27	34	ns
Non linearity		EL	Fc = 20 MSPS V_{IN} = 5 to 3V				±1/2	LSB
Differential non linearity		ED					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, Fc = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			6	8	11	ns

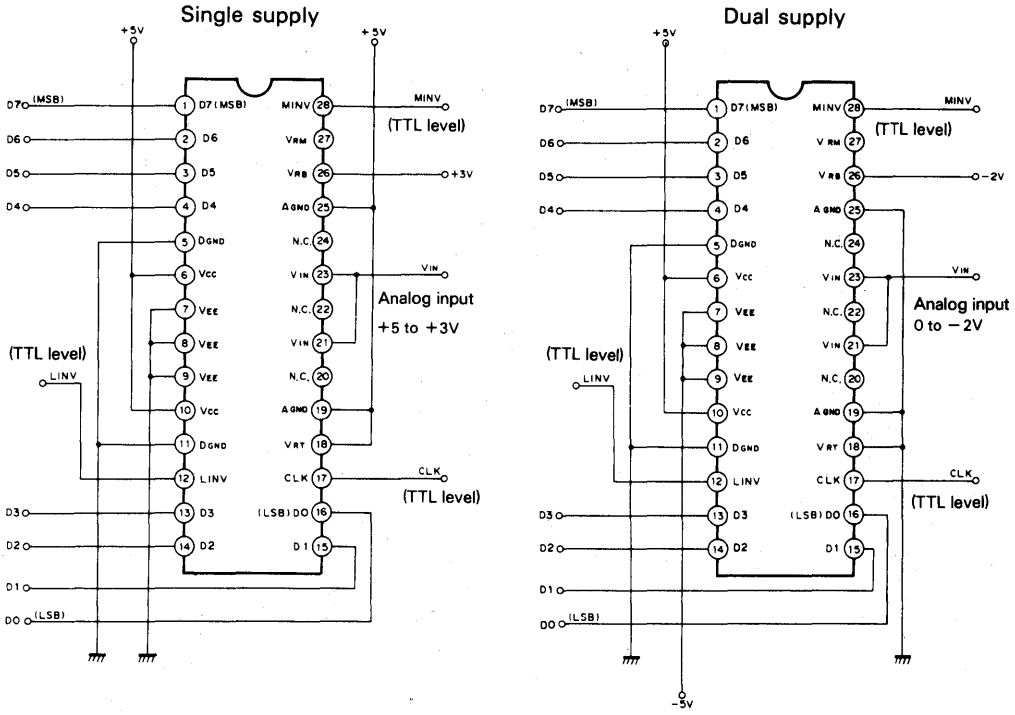
3

Electrical Characteristics (Dual supply)

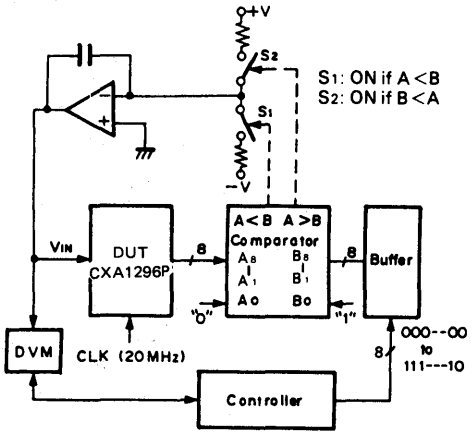
V_{CC} = +5V, DGND = 0V, AGND = 0V, V_{EE} = −5V, V_{RT} = 0V, V_{RB} = −2V, Ta = 25°C

Item		Symbol	Test condition		Min.	Typ.	Max.	Unit
Maximum conversion rate		F_C	V_{IN} = 0 to −2V F_{IN} = $F_C/4$ − 1 kHz		20			MSPS
Supply current		I_{CC}			7	10	14	mA
		I_{EE}			50	65	80	mA
Reference pin current		I_{REF}			12	16	20	mA
Analog input bandwidth		BW			8			MHz
Analog input capacitance		C_{IN}	V_{IN} = −1V + 0.07Vrms			30	35	pF
Analog input bias current		I_{IN}	V_{IN} = −1V		15	50	115	μA
Reference resistance (V_{RT} to V_{RB})		R_{REF}				125		Ω
Offset voltage	V_{RT}	E_{OT}			8	13	19	mV
	V_{RB}	E_{OB}			0	5	11	mV
Digital input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Digital input current		I_{IH}	V_{CC} = Max.	V_{IH} = 2.7V	0	−100	−150	μA
		I_{IL}		V_{IL} = 0.5V	0	−0.32	−0.5	mA
Digital output voltage		V_{OH}	V_{CC} = Min.	I_{OH} = −500μA	2.7	3.4		V
		V_{OL}		I_{OL} = 3mA			0.5	V
Output data delay		T_{DLH}	LOAD 1		14	18	24	ns
		T_{DHL}			21	27	34	ns
Non linearity		E_L	F_C = 20 MSPS V_{IN} = 0 to −2V				±1/2	LSB
Differential non linearity		E_D					±1/2	LSB
Differential gain error		DG	NTSC 40 IRE mod. ramp, F_C = 14.3 MSPS				1.5	%
Differential phase error		DP					0.5	deg.
Aperture jitter		E_{AP}				30		ps
Sampling delay		tds			6	8	11	ns

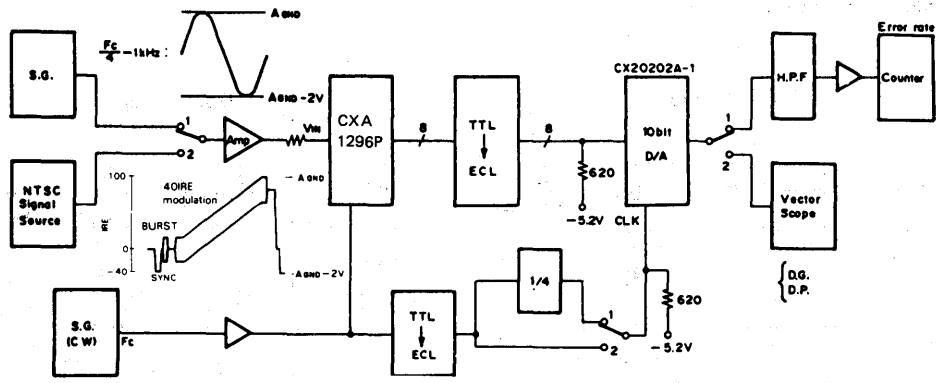
Application Circuit



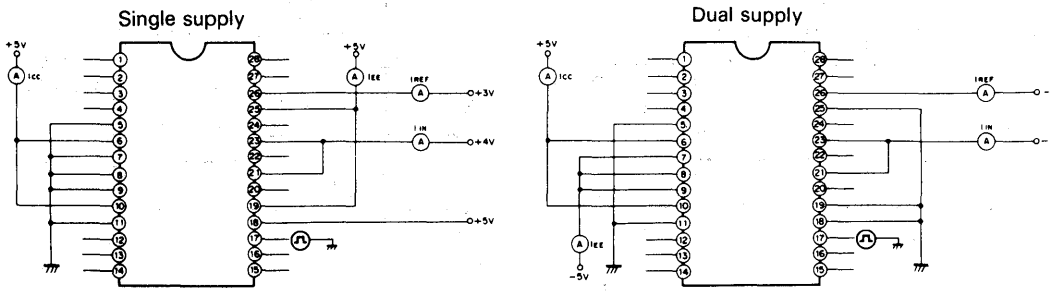
Electrical Characteristics Test Circuit



Non linearity
Differential non linearity } Test circuit

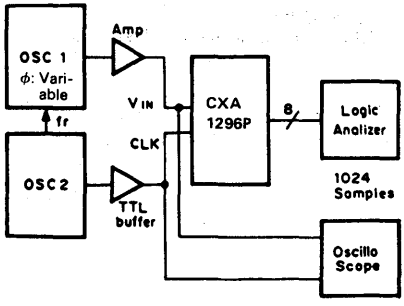


Maximum conversion rate
Differential gain error
Differential phase error
} Test circuit

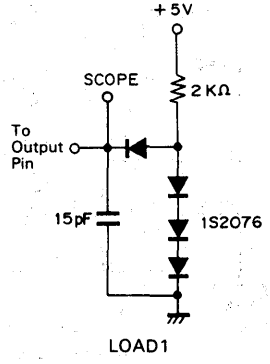


Note) VIN pin is connected to VRT pin for ICC and IEE measurement.

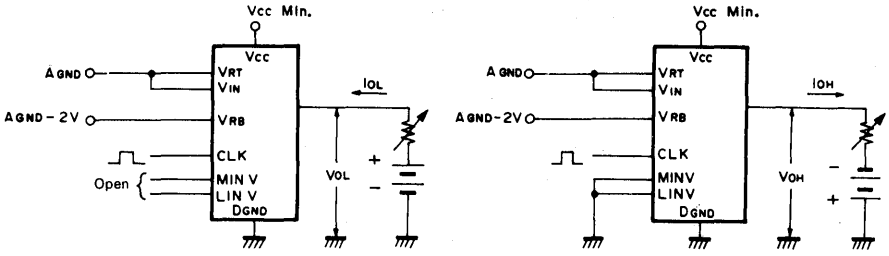
Supply current
Analog input bias current
Reference pin current
} Test circuit



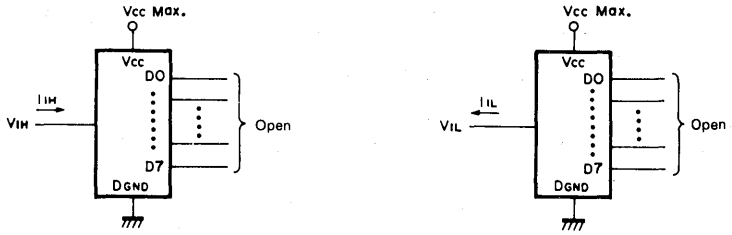
Aperture jitter
Sampling delay
} Test circuit



Test Load for Output data delay

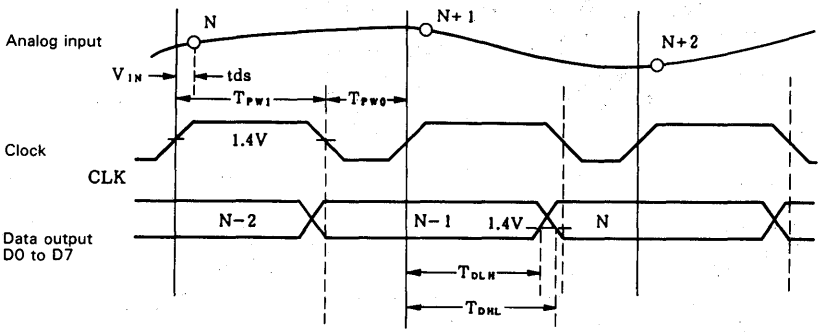


Test circuit of digital output voltage (D0 to D7)

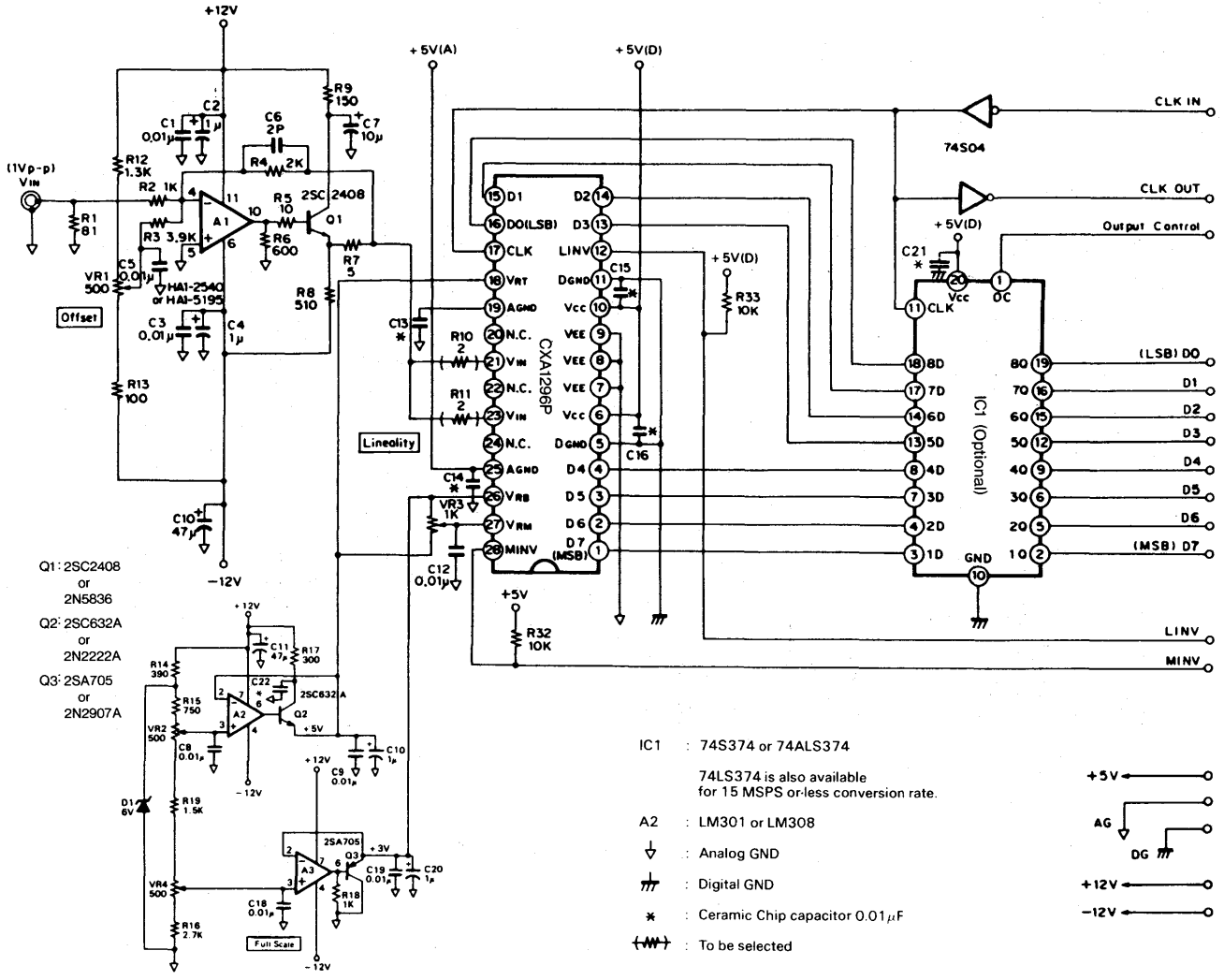


Test circuit of digital input current (CLK, MINV, LINV)

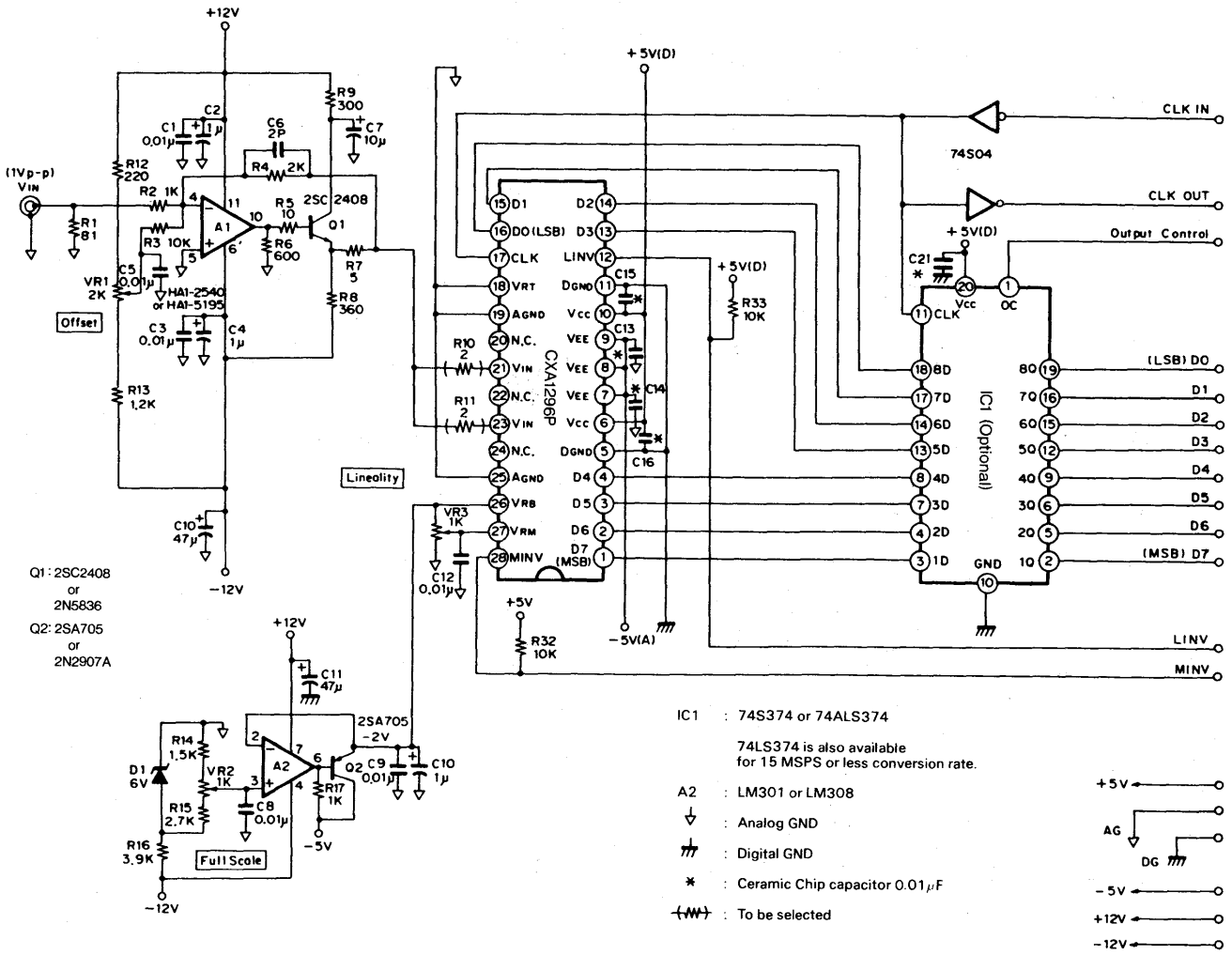
Timing Chart



Application Circuit (Single supply)



Application Circuit (Dual supply)



Notes on Application

1. Each of DGND pins (5, 11) and each of Vcc Pins (6, 10) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.

2. Layout of the analog and digital sections should be separated to reduce noise effect.
   VEE pins to AGND and Vcc pins to DGND should be bypassed as closely as possible by means of 1μF and 0.01μF capacitors.
   For the 0.01μF, a ceramic chip capacitor should be used.

3. The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power. Pins VIN (21, 23) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to 10Ω with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.
   The amplifier output and A/D input should be connected as closely as possible.

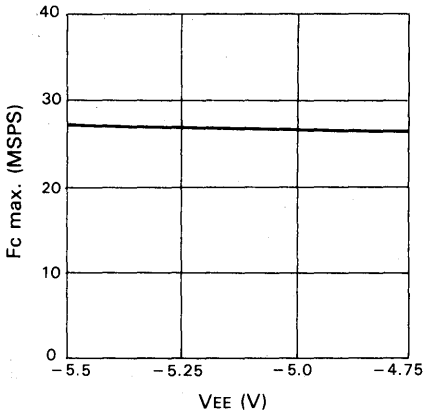
4. Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of 1μF and 0.01μF capacitors.
   Through bypassing VRM pin with a 0.01μF capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.

5. CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.

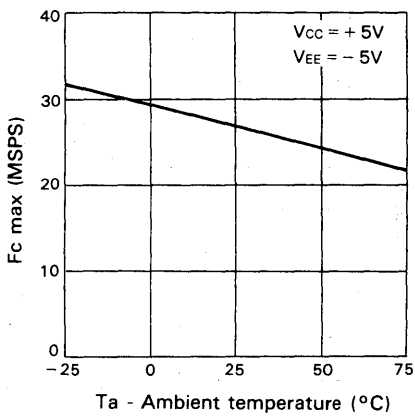
6. Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the positive going edge with a short delay time (TDLH, TDHL). If digital data will be latched externally, it should be latched at the positive going edge. (See the Timing Chart)

7. It is recommended to connect free pins to AGND for prevention of noise effect.

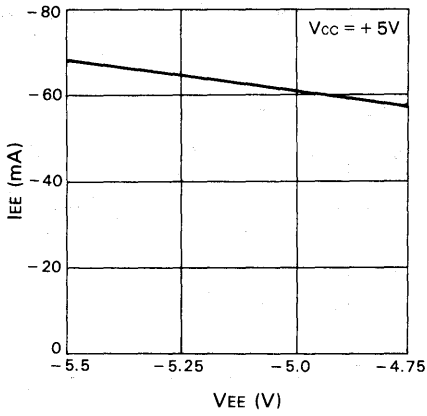
Fc max vs. VEE



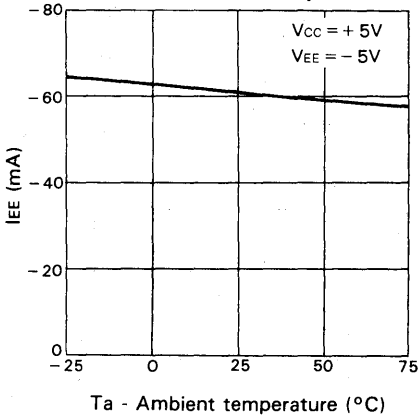
Fc max vs. Ambient temperature



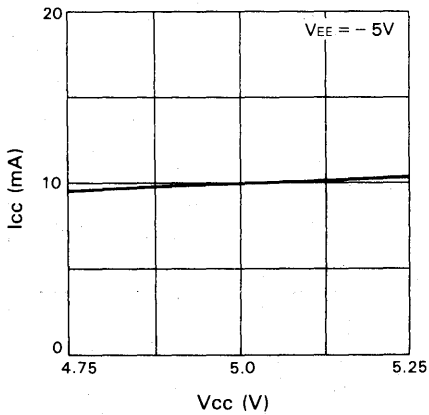
IEE vs. VEE



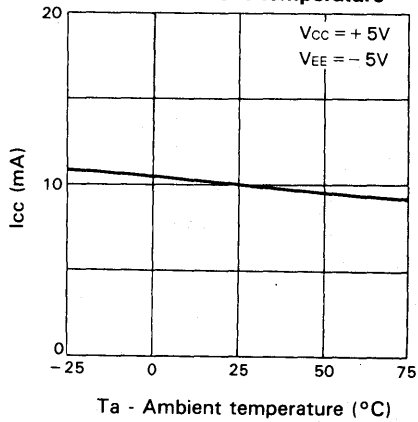
IEE vs. Ambient temperature



Icc vs. Vcc

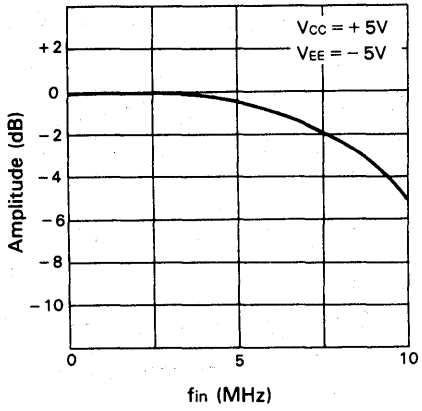


Icc vs. Ambient temperature

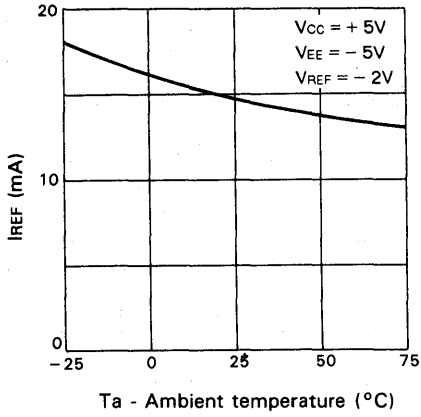


3

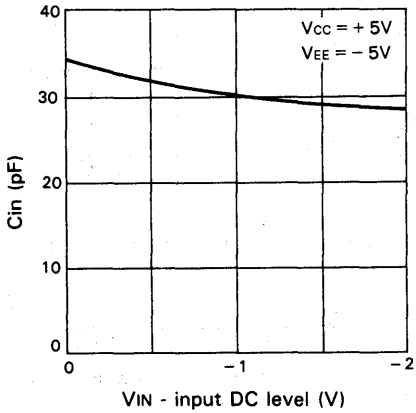
Amplitude deviation of the converted signal vs. The analog frequency



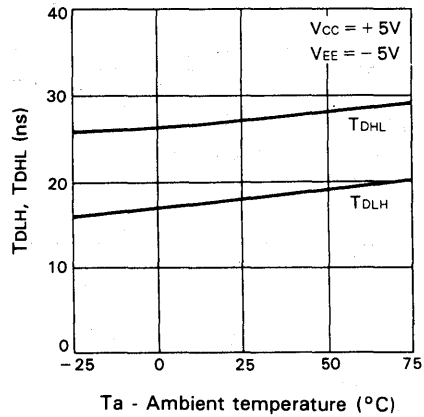
IREF vs. Ambient temperature



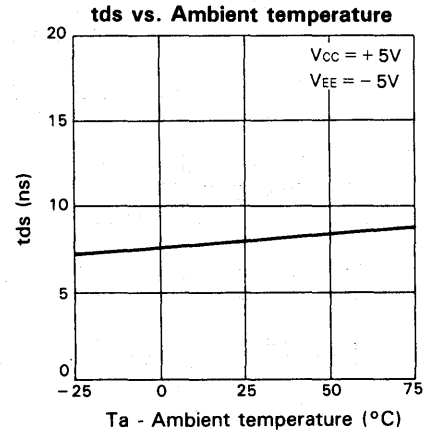
CIN vs. VIN - input DC level



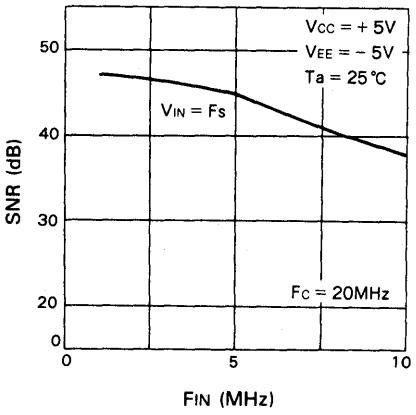
TDLH, TDHL vs. Ambient temperature



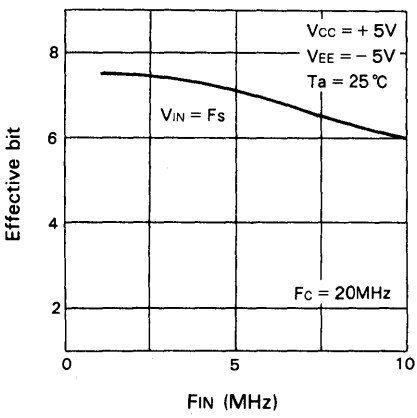
tds vs. Ambient temperature



SNR vs. FIN



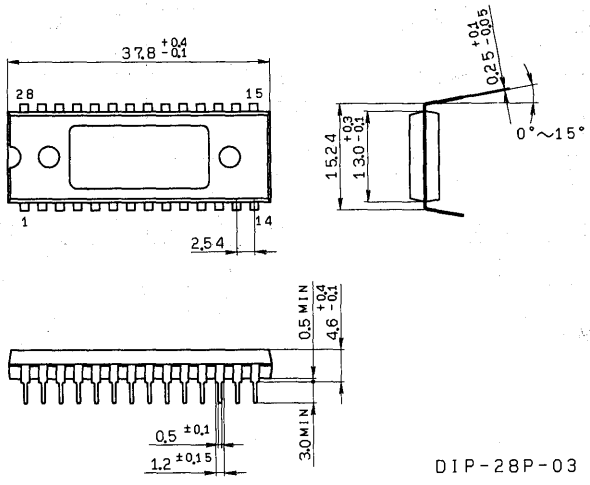
Effective bit vs. FIN



3

Package Outline Unit : mm

28pin DIP (Plastic) 600mil 4.2g



DIP-28P-03

SONY

CXA1496AQ

10-bit 20MSPS A/D Converter

Description

The CXA1496AQ is a 10-bit 20MSPS 2-step parallel type A/D converter for video signal processing.

This A/D converter operates on a dual ±5V power supply. The external addition of sample and hold, reference power supply and clock timing circuits permit the conversion of analog signals into digital signals.

48 pin QFP (Plastic)

Features

- Maximum operating frequency 20MHz (Min.)
- Integral linearity error 10-bit ± 1.5LSB
- Differential linearity error 10-bit ± 1LSB
- Low power consumption 310mW (Typ.)
- Wide band analog input 10MHz
- Low input capacity 150pF (Typ.)
- Built-in digital correction
  (Compensation within a range of ± 16LSB)
- TTL input (CLK only: ECL LIKE)
- TTL output (3-state control)
- Output code Binary/2S complement/
  1S complement

Function

10-bit 20MSPS 2-step parallel type A/D converter

Structure

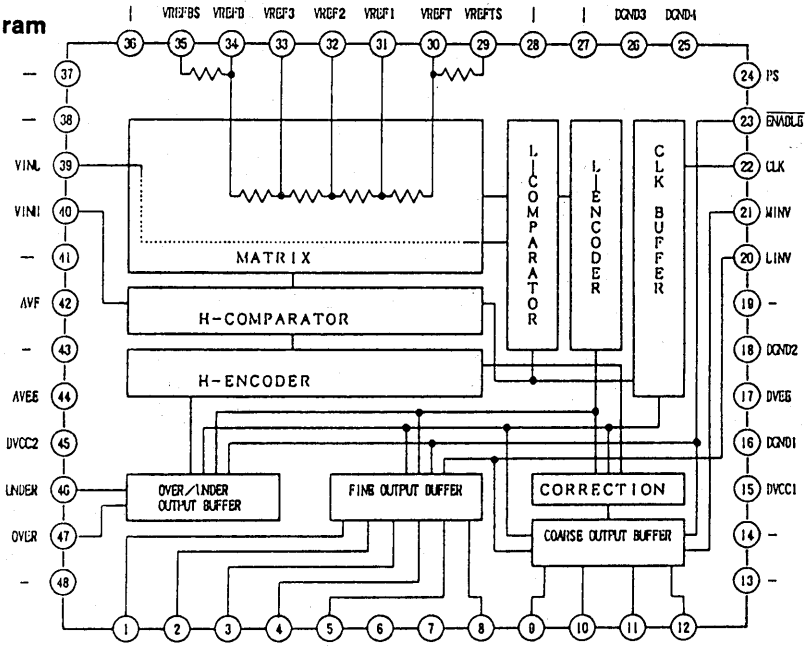
Bipolar silicon monolithic IC

Applications

High resolution video signal processing

3

Block Diagram



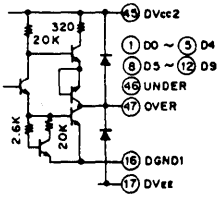
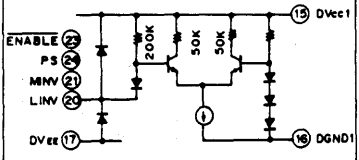
Absolute Maximum Ratings (Ta=25℃)

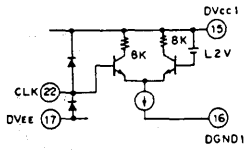
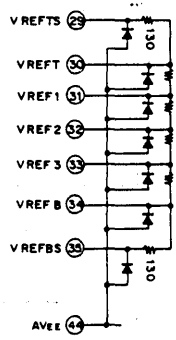
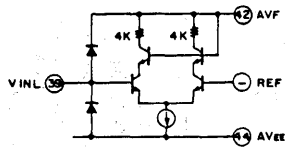
• Supply voltage	DVcc1	0 to +6	V
	DVcc2	0 to +6	V
	AVEE	0 to −6	V
	DVEE	0 to −6	V
• Analog input voltage	VINH	AVEE to AGND+0.3	V
	VINL	AVEE to AGND+0.3	V
• Reference voltage	VRT	AVEE to AGND+0.3	V
	VRB	AVEE to AGND+0.3	V
• Digital input voltage	CLK	DGND1−0.5 to DVcc1	V
	MINV	DGND1−0.5 to DVcc1	V
	LINV	DGND1−0.5 to DVcc1	V
	PS	DGND1−0.5 to DVcc1	V
	$\overline{\text{ENABLE}}$	DGND1−0.5 to DVcc1	V
• Storage temperature	Tstg	−65 to 150	℃

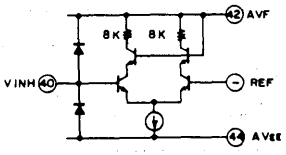
Operating Conditions

		Min.	Typ.	Max.	Unit
• Supply voltage	DVcc1	+4.75	+5	+5.25	V
	DVcc2	+4.75	+5	+5.25	V
	DGND1		0		V
	DGND2		0		V
	DGND3		0		V
	DGND4		0		V
	AVF	+0.5	+0.7	+0.9	V
	AVEE	−5.25	−5	−4.75	V
	DVEE	−5.25	−5	−4.75	V
• Analog input voltage	VINH	−2		0	V
	VINL	−2		0	V
• Reference voltage	VRT	−0.1	0	+0.1	V
	VRB	−2.1	−2.0	−1.9	V
• Digital input voltage (MINV, LINV, PS, $\overline{\text{ENABLE}}$)					
	DIN (H)	+2			V
	DIN (L)			+0.5	V
• Digital input voltage (CLK)	DIN(H)	DVcc1−1	DVcc1−0.8		V
	DIN(L)		DVcc1−1.6	DVcc1−1.4	V
• Clock width	tPWH	25			ns
	tPWL	25			ns
• Operating temperature	Topr	−20		+75	℃

Pin Description

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
1 to 5 8 to 12	D0 to D9	O	TTL		Digital output pins D0 (LSB) to D9 (MSB)
46	UNDER	O			Underflow output pin
47	OVER	O			Overflow output pin
15	DVcc1	—	+5V (Ratings)		Digital power supply
45	DVcc2				
16	DGND1	—	GND		Digital ground
18	DGND2	—	GND		Digital ground
26	DGND3				
25	DGND4				
17	DVEE	—	−5V		Digital negative power supply
44	AVEE	—			Analog negative power supply
20	LINV	I	TTL		This input pin can invert the form of the output from D0 (LSB) to D8. In open condition this pin turns to High level input. (For details, refer to the output formula chart.)
21	MINV	I	TTL		This input pin can invert the form of the output from D9 (MSB). In open condition this pin turns to High level input. (For details, refer to the output formula chart.)
23	$\overline{\text{ENABLE}}$	I	TTL		3-state control pin. Turns to enable when low is input. In open condition this pin turns to High level input.
24	PS	I	TTL		Power save input pin. In open condition this pin turns to High level input.

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
22	CLK	I	ECL LIKE		Clock input pin
29	VREFTS	—	GND		Reference voltage sense pin (Top)
30	VREFT	I			Reference voltage force pin (Top)
31	VREF1	—	–0.5V		
32	VREF2	—	–1.0V		
33	VREF3	—	–1.5V		
34	VREFB	I	–2V		Reference voltage force pin (Bottom)
35	VREFBS	—			Reference voltage sense pin (Bottom)
39	VINL	I	–2V to 0V		Analog input pin (Lower comparator input pin)

Pin No.	Symbol	I/O	Pin voltage	Equivalent circuit	Description
40	VINH	I	–2V to 0V		Analog input pin (Upper comparator input pin)
42	AVF	——	+0.7V		Analog power supply

Electrical Characteristics

(Ta=25 °C, DVcc1, 2=5V, DGND1 to 4=0V, AVF=0.7V, AVEE, DVEE=–5V, VRB=–2V, VRT=0V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Resolution	n				10	10	10	bit
DC characteristics								
Integral linearity error	EIL	FC=20MSPS VIN=0 to –2V			1.5		1.5	LSB
Differential linearity error	EDL				–1		+1	LSB
Analog input								
Analog input current	IIN	VIN=0			0	25	100	µA
Analog input capacity	CIN	VIN=–1V+0.07Vrms				150		pF
Analog input band width	BW	–1dB down				10		MHz
Reference voltage input								
Reference current	IREF				8	10	12	mA
Reference resistance	RREF				160	200	240	Ω
Offset voltage	EOT				3	13	23	mV
	EOB				2	12	22	mV
Reference voltage 1	VREF1				–0.55	–0.5	– 0.45	V
Reference voltage 2	VREF2				–1.05	–1.0	– 0.95	V
Reference voltage 3	VREF3				–1.55	–1.5	– 1.45	V
Digital input								
Digital input voltage H	VIH				2			V
Digital input voltage L	VIL						0.5	V
Digital input current 1H	IIH1	*1	DVcc1 Max.	VIH=DVcc1–0.8V	–10	0.5	+10	µA
Digital input current 1L	IIL1			VIL=DVcc1–1.6V	–1	0	+1	µA
Digital input current 2H	IIH2	*2		VIH=2.7V	–10	0	+10	µA
Digital input current 2L	IIL2			VIL=0.5V	–20	–10	0	µA
Digital input capacity						5		pF

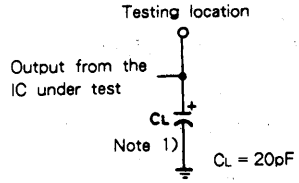
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Switching characteristics						
Max. operating frequency	Fc		20			MSPS
Pulse width H	t_{PWH}	*3	25			ns
Pulse width L	t_{PWL}		25			ns
Sampling delay TS1	t_{SH}			4		ns
Sampling delay TS2	t_{SL}			3		ns
Output rising delay time	t_{DLH}	*3 C_L=20pF	16	24	43	ns
Output falling delay time	t_{DHL}	*5	24	32	52	ns
3-state output disable time H	t_{PHZ}	*4 *6	40	100	500	ns
3-state output disable time L	t_{PLZ}		40	100	500	ns
3-state output enable time H	t_{PZH}		40	150	500	ns
3-state output enable time L	t_{PZL}		40	150	500	ns
Digital output						
Digital output voltage H	V_{OH}	I_{OH}=–500 µA	2.7	3.4		V
Digital output voltage L	V_{OL}	I_{OL}=3mA			0.5	V
Leak current during output OFF	I_{OZ}	*6	–20		20	µA
Dynamic characteristics						
Differential gain error	DG	NTSC 40IRE mod ramp, Fc=14.3MSPS		0.5		%
Differential phase error	DP			0.3		deg
SNR	SNR	Fc=20MHz F_{IN}=1kHz		51		dB
		Fc=20MHz F_{IN}=1MHz		50		dB
		Fc=20MHz F_{IN}=5MHz		48		dB
		Fc=20MHz F_{IN}=10MHz		48		dB

3

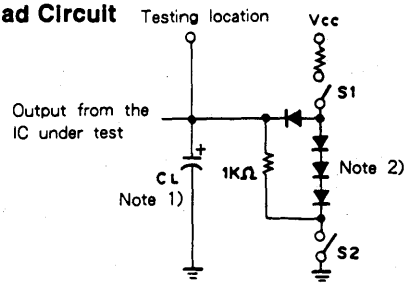
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply						
DVcc1 current	I_{DVCC1}	DVcc1=5V	3	6	10	mA
		At power saving	3	5	11	mA
DVcc2 current	I_{DVCC2}	DVcc2=5V	0	2	5	mA
		At power saving	0	2	4	mA
DGND3 current	I_{DGND3}	DGND3=0V	2	3	5	mA
		At power saving	0	0	0.1	mA
DGND4 current	I_{DGND4}	DGND4=0V	2	3	5	mA
		At power saving	0	0	0.1	mA
DVEE current	I_{DVEE}	DVEE=–5V	–50	–33	–25	mA
		At power saving	–12	–3	–2	mA
AVEE current/AVF current	I_{AVEE} I_{AVF}	AVEE=–5V	–26	–16	–12	mA
		At power saving	–10	–5	0	mA
Power Consumption ($I_{DVCC1}+I_{DVCC2}+\|I_{DVEE}\|+\|I_{AVEE}\|$)		DVcc1, DVcc2=5V DGND1, DGND2, DGND3, DGND4=0V AVF=0.7V DVEE, AVEE=–5V	40	57	80	mA
		At power saving	5	15	37	mA

*1 CLK input
*2 MINV, LINV, $\overline{\text{ENABLE}}$, PS inputs
*3 See Timing Diagram (1)
*4 See Timing Diagram (2)
*5 Load is at the Bi-state Totem-Pole output delay time test load circuit
*6 Load is at the 3-state output test load circuit

Bi-state Totem-Pole Output Delay Time Test Load Circuit



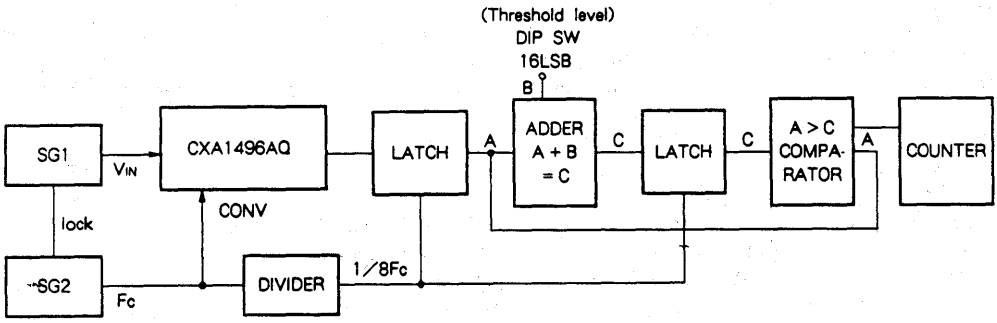
3-state Output Test Load Circuit



Test Conditions	S1	S2
t_{PZL}	Close	Open
t_{PZH}	Open	Close
t_{PLZ} t_{PHZ}	Close	Close

Note 1) C_L includes the probe capacitance and the floating capacitance of the test circuit.
Note 2) All diodes use 1S2076.

Error Rate Testing Circuit



Notes on Operation

1. Analog ground (Analog ground on PCB)
   Keep analog ground surface on PCB as wide as possible with impedance and resistance as low as possible.

2. Digital ground (DGND1, DGND2, DGND3, DGND4)
   Upon mounting to PCB keep ground surface as wide as possible with impedance and resistance as low as possible.
   Moreover, a common analog and digital ground immediately near ADC will help obtain characteristics smoothly.

3. Digital positive power supply (DVcc1, DVcc2)
   Connect to the digital ground with a ceramic capacitor over 0.1 μF and as close to the pins as possible.

4. Analog positive power supply (AVF)
   As the standard circuit example shown in p.16, make it about +0.7V by connecting to the analog ground with a diode and +5V with a pull-up resister respectively.
   Connect to the analog ground on PCB with a ceramic capacitor over 0.1 μF as close to the pin as possible.

5. Analog negative power supply (AV_{EE})
   Connect to the analog ground on PCB with a ceramic capacitor over 0.1 μF as close to the pin as possible.

6. Digital negative power supply (DV_{EE})
   Connect to the digital ground with a ceramic capacitor over 0.1 μF as close to the pin as possible.
   When V_{EE} is divided into digital and analog, there is continuity because of approx. 4Ω resistance between the two inside the IC.
   Accordingly, if an excessive potential difference (more than 100mV) is applied continuously, this may destroy the IC. To prevent the IC destruction, connect AV_{EE} and DV_{EE} with a inductance having good high frequency characteristics. Prevent noise mixing and the generation of potential difference between analog and digital.

7. Reference voltage (VREFTS, VREFT, VREF1, VREF2, VREF3, VREFB, VREFBS)
   These pins provide reference voltage to upper and lower comparators. Voltage between Pins VREFT and VREFB corresponds to input dynamic range.
   There is a 200Ω resistance between VREFT and VREFB. By applying 2V to both pins a current of about 10mA flows. When the reference voltage is destabilized by the clock, ADC characteristics are adversely affected. Connect Pins VREFT and VREFB to the analog ground on PCB by means of a tantalum capacitor over 10 μF and a ceramic capacitor over 0.1 μF respectively. Also, connect each of VREF1, VREF2 and VREF3 pins to the analog ground on PCB using a ceramic capacitor over 0.1 μF. This will provide stability to the characteristics of high frequency. Strictly speaking on reference voltage pins VREFT side and VREFB side there is a respective about 15mV offset. When there is no problem with the usage of those offset voltages, voltage is applied directly to VREFT, VREFB. In case the reference voltage is to be strictly applied, adjust to obtain an offset voltage of 0V, keeping Pins VREFTS and VREBS as sense pins and Pins VREFT and VREFB as force pins to form a feedback loop circuit.
   For details, see Application Circuit.

8. Analog input (VINH, VINL)
VINH is the input pin for the upper comparator while VINL is the input pin for the lower comparator.
Keep the input signal level within the level between VREFT and VREFB.
As this IC's analog input capacitance stands at about 150pF, it is necessary to drive with an buffer amplifier having sufficient driving capability. Also, when driving is done with the buffer amplifier of a low output impedance, as ADC input capacitance is large, ringing is generated and settling time grows longer. Here a small resistance of about 5 to 30Ω is connected in series between the buffer amplifier and each of ADC's VINH and VINL pins, as a dumping resistance. This eliminates ringing and shortens settling time. Also keep wiring between buffer amplifier and ADC as short as possible.

9. Clock input (CLK)
ECL LIKE input. Adds the signal of Vcc1 (5V) –0.8V at high level and Vcc1 (5V) –1.6V at low level.
Clock line wiring should be the shortest possible while distanced from other signal lines to avoid affecting them.
This IC is of the serial parallel type ADC. Accordingly an external sample and hold circuit (SH) is necessary. However the timing between this SH circuit output waveform (ADC analog input waveform) and the ADC clock timing requires attention. In the relation between ADC clock and the ADC analog input signal, with the timing T_H of the rising edge of ADC clock, the upper comparator compares the input signal and the reference voltage to latch the results. After that, with the timing T_L of the falling edge of ADC clock, the lower comparator compares the input signal and reference signal to latch the results. (Strictly speaking, the sampling delay t_{SH} is in T_H and the sampling delay t_{SL} is in T_L.)
In this ADC, the lower comparator features a length of ±32mV (±16LSB) redundance in relation to the upper comparator. At the timing when the lower comparator compares input signal and reference signal to latch at the timing T_L, it is necessary to have the SH output settling performed. But at the timing when the upper comparator compares input signal and reference voltage to latch at the timing T_H, as long as the SH output is within the ± 32mV range to the final settling value, digital correction applies, A/D conversion precisely occurs. As seen from the above, ADC clock rise and fall timing versus SH output waveform should be duly considered. For the clock High level time t_{PWH} and Low level time t_{PWL}, set to a value in excess of the time indicated for the respective operating conditions.
Output data is output synchronously with the clock rising edge. For details on timing, refer to Timing Diagram.

10. MINV input (MINV)
Digital output polarity inversion control pin of D9 (MSB).
TTL input. At open, turns to High level input.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

11. LINV input (LINV)
Digital output polarity inversion control pin of D8 to D0 (LSB).
TTL input. At open, turns to High level input.
For correspondence with analog input voltage and output data code, refer to the Output Formula Chart.

12. 3-state ($\overline{\text{ENABLE}}$)
3-state control pin of digital output (D0 to D9, UNDER, OVER).
TTL input. At open, turns to High level input. At that time digital output turns all to high impedance.

13. Power save input (PS)
Power save control pin of internal circuit.
TTL input. At open, turns to High level input. To set to power save mode, turn both Pins PS and $\overline{\text{ENABLE}}$ to High level input.

14. Digital output (D0 to D9)
Output pin of D9 (MSB) to D0 (LSB).
TTL output.
Output data polarity inversion is executed by means of MINV and LINV signals. Can output in binary, 1S complement and 2S complement.
Also, by turning $\overline{\text{ENABLE}}$ signal to High level, the output can be turned into high impedance output.
For correspondence with analog input voltage and output data code, refer to Output Formula Chart.
For the timing, refer to Timing Chart.

15. Overflow output (OVER)
When the input signal exceeds VREFT, overflow signal is output.
MINV and LINV have no effect on this pin.
Also by turning $\overline{\text{ENABLE}}$ signal to High level, the output can be turned into high impedance output.
For correspondence with analog input voltage and output data code, refer to Output Formula Chart.
For the timing, refer to Timing Chart.

16. Underflow chart (UNDER)
When the input signal turns below VREFB, underflow signal is output.
MINV and LINV have no effect on this pin.
Also by turning $\overline{\text{ENABLE}}$ signal to High level, the output can be turned into high impedance output.
For correspondence with analog input voltage and output data code, refer to Output Formula Chart.
For the timing, refer to Timing Chart.

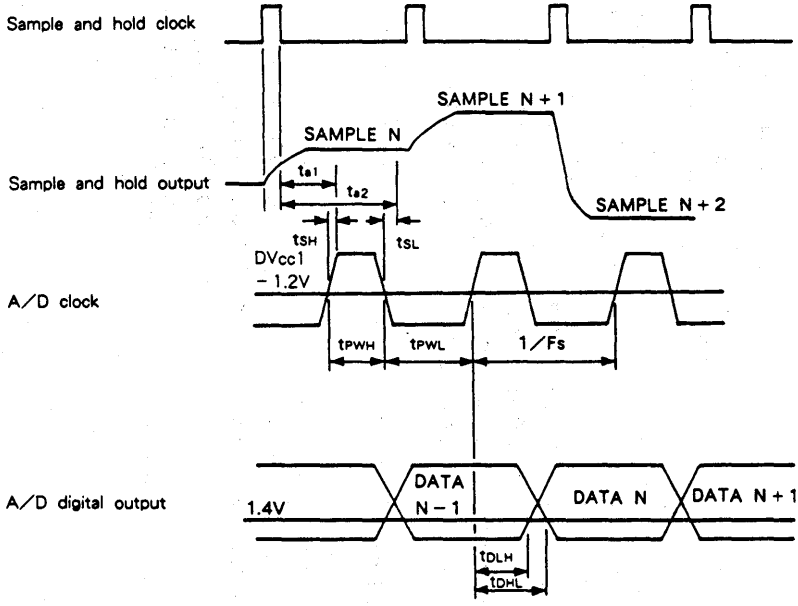
Output Formula Chart

$\overline{\text{ENABLE}}$		0	0	0	0	1 (OPEN)
MINV		1 (OPEN)	1 (OPEN)	0	0	—
LINV		1 (OPEN)	0	1 (OPEN)	0	—
OUTPUT		0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	0F 9 8 7 6 5 4 3 2 1 0 UF (MSB) (LSB)	
0V	0	1 0 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 1 0	1 1 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 0	Z
⋮	1	0 0 0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 1 0	0 1 1 1 1 1 1 1 1 1 0 0	Z
⋮	2	0 0 0 0 0 0 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 0 1 0	0 1 0 0 0 0 0 0 0 1 0 0	0 1 1 1 1 1 1 1 1 0 1 0	Z
⋮	3	0 0 0 0 0 0 0 0 0 1 1 0	0 0 1 1 1 1 1 1 1 0 0 0	0 1 0 0 0 0 0 0 0 1 1 0	0 1 1 1 1 1 1 1 1 0 0 0	Z
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	512	0 1 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 0	0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 0	Z
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	1019	0 1 1 1 1 1 1 1 0 1 1 0	0 1 0 0 0 0 0 0 1 0 0 0	0 0 1 1 1 1 1 1 1 0 1 1 0	0 0 0 0 0 0 0 0 1 0 0 0	Z
⋮	1020	0 1 1 1 1 1 1 1 1 0 0 0	0 1 0 0 0 0 0 0 0 1 1 0	0 0 1 1 1 1 1 1 1 0 0 0	0 0 0 0 0 0 0 0 0 1 1 0	Z
⋮	1021	0 1 1 1 1 1 1 1 1 0 1 0	0 1 0 0 0 0 0 0 0 1 0 0	0 0 1 1 1 1 1 1 1 0 1 0	0 0 0 0 0 0 0 0 0 1 0 0	Z
⋮	1022	0 1 1 1 1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 1 0	0 0 1 1 1 1 1 1 1 1 0 0	0 0 0 0 0 0 0 0 0 1 0	Z
–2V	1023	0 1 1 1 1 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0 0 0 0 1	0 0 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 1	Z

0: VOLTAGE LEVEL-LOW
1: VOLTAGE LEVEL-HIGH
Z: HIGH IMPEDANCE

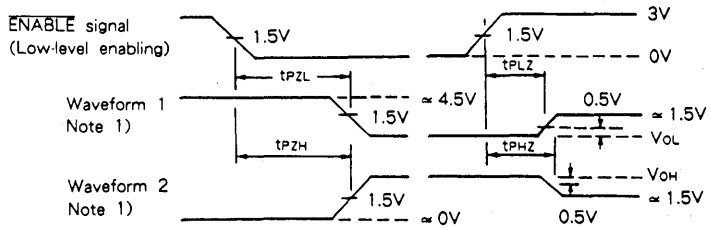
OF: OVER FLOW
UF: UNDER FLOW

Timing Diagram (1)



T_H is the timing of latching result for the comparation of V_{IN} and V_{REF} the upper comparators.
T_L is the timing of latching result for the comparation of V_{IN} and V_{REF} in the lower comparators.

Timing Diagram (2)

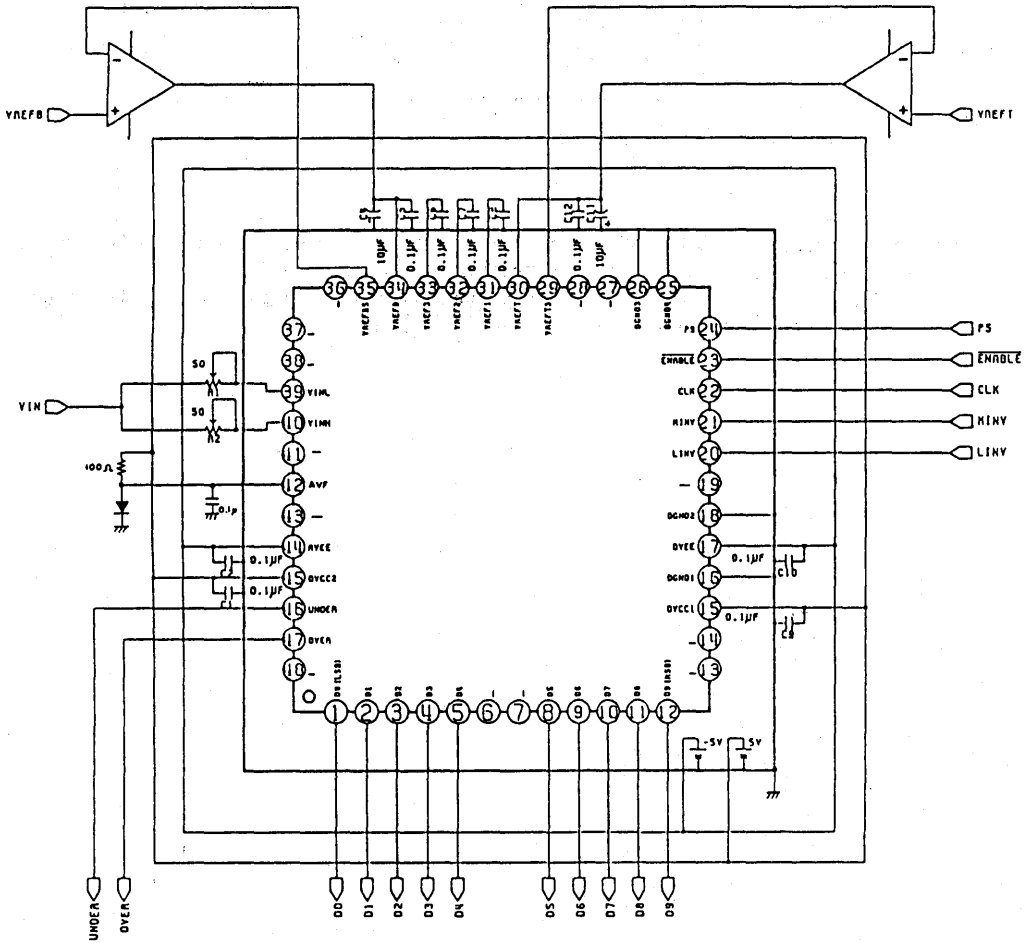


Voltage waveform of 3-state enable and disable time *
(* Enable time=t_{PZL}/t_{PZH}
Disable time=t_{PLZ}/t_{PHZ})

Note) Waveform 1 indicates the output waveform when internal conditions are set to obtain a low level output, with the exception of when output is disabled by means of the $\overline{\text{ENABLE}}$ signal.
Waveform 2 indicates the output waveform when internal conditions are set to obtain a high level output, with the exception of when output is disabled by means of the $\overline{\text{ENABLE}}$ signal.

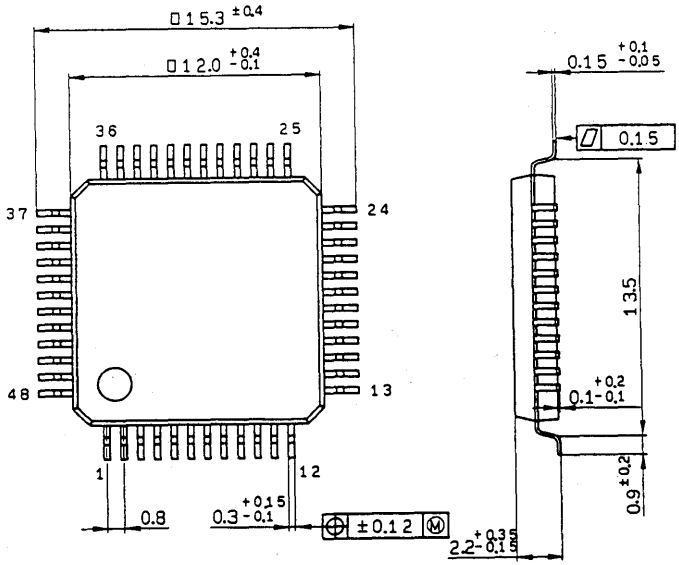
3

Standard Circuit



Package Outline Unit : mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	•QFP048-P-1212-B
JEDEC CODE	———

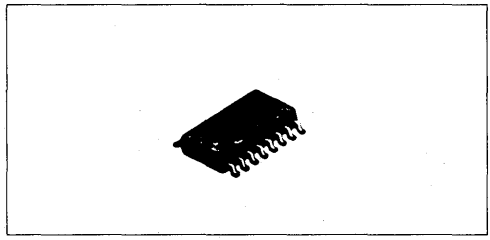
3

SONY CXD1172AM/AP

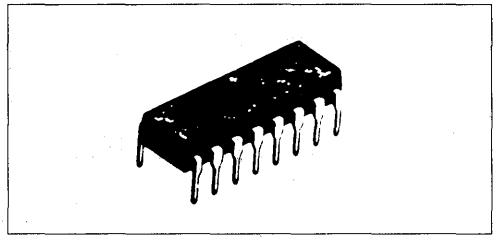
6-bit 20MSPS Video A/D Converter (CMOS)

Description

The CXD1172A is a 6-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low power consumption at a maximum conversion speed of 20MSPS minimum, 35MSPS is typical.



CXD1172AM 16pin SOP (Plastic)



CXD1172AP 16pin DIP (Plastic)

Features

- Resolution 6-bit ± 1/2 LSB
- Max. sampling frequency 20MSPS
- Low power consumption
  40mW (at 20MSPS Typ.)
  (Reference current excluded)
- Built-in sampling and hold circuit.
- Power supply 5V single
- Low input capacity 4pF
- Reference impedance 300Ω (Typ.)
- Pin replaceable with CXD1172.

Structure

Silicon gate CMOS monolithic IC.

Applications

TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

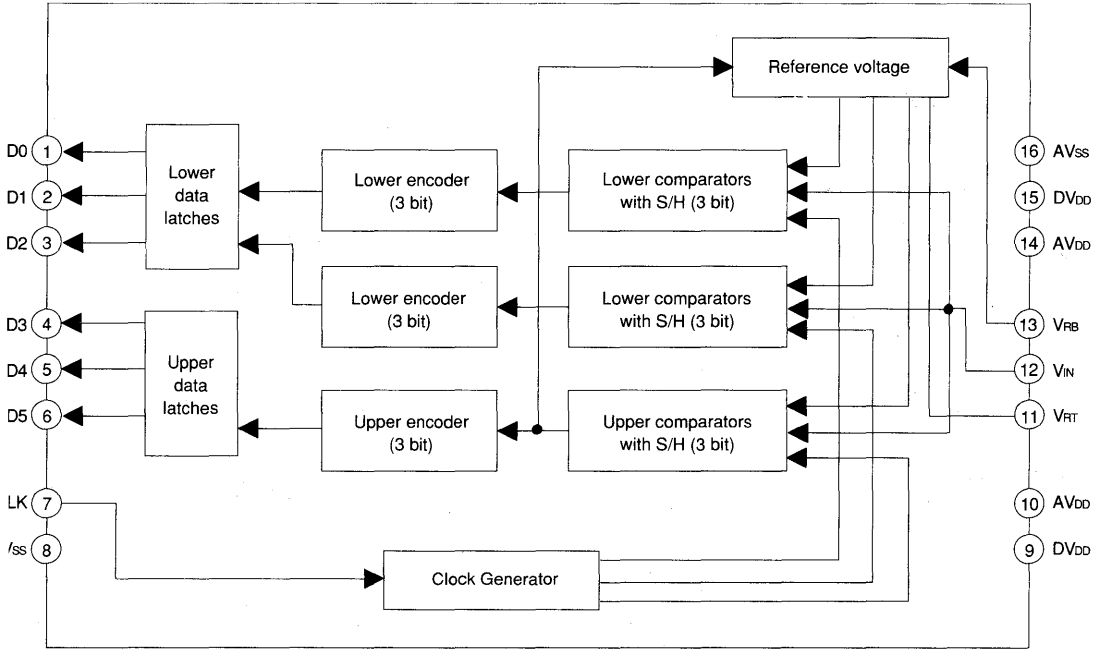
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RS}	V_{DD} to V_{SS}	V
• Analog Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Digital Input voltage	C_{LK}	V_{DD} to V_{SS}	V
• Digital output voltage	V_{CH}, V_{OL}	V_{DD} to V_{SS}	V
• Storage temperature	Tstg	-55 to +150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	
• Reference input voltage	V_{RB}	0 to 4.1	V
	V_{RT}	0.9 to 5.0	V
	VRT-VRB	0.9 to AV_{DD}	V
• Analog input voltage	V_{IN}	V_{RB} to V_{RT}	
• Clock pulse width	T_{PWI}	25(min.)	ns
	T_{PWO}	25(min)	ns
• Operating temperature	T_{OPR}	-20 to +75	°C

Block Diagram and Pin Configuration

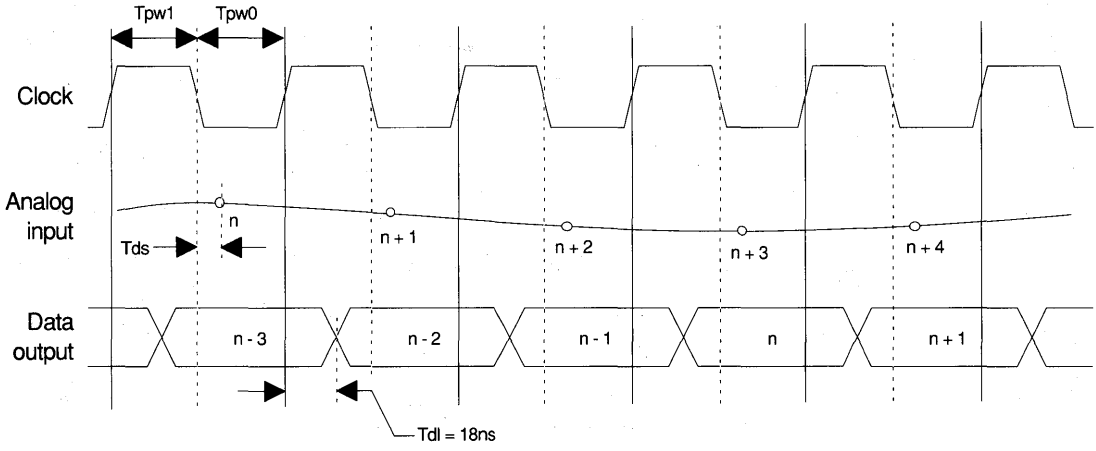


Digital Output

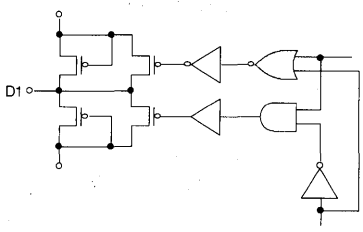
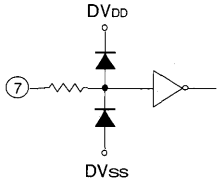
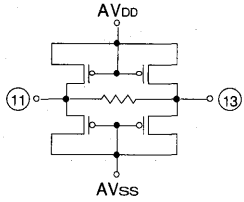
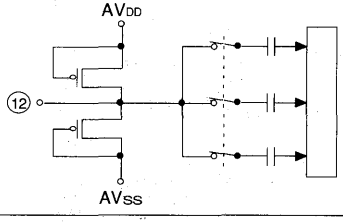
Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

Input Signal Voltage	Step	Digital Output Code					
		MSB					LSB
VRT	0	1	1	1	1	1	1
	31	1	0	0	0	0	0
	32	0	1	1	1	1	1
VRB	63	0	0	0	0	0	0

Timing Chart 1



Pin Description and Equivalent Circuits

No.	Symbol	Equivalent Circuit	Description
1 to 6	D_0 to D_5		D_0 (LSB) to D_5 (MSB) output
7	CLK		Clock input
8	DV_{SS}		Digital GND
9, 15	DV_{DD}		Digital +5V
10, 14	AV_{DD}		Analog +5V
11	V_{RT}		Reference voltage (top)
13	V_{RB}		Reference voltage (bottom)
12	V_{IN}		Analog input
16	AV_{SS}		Analog GND

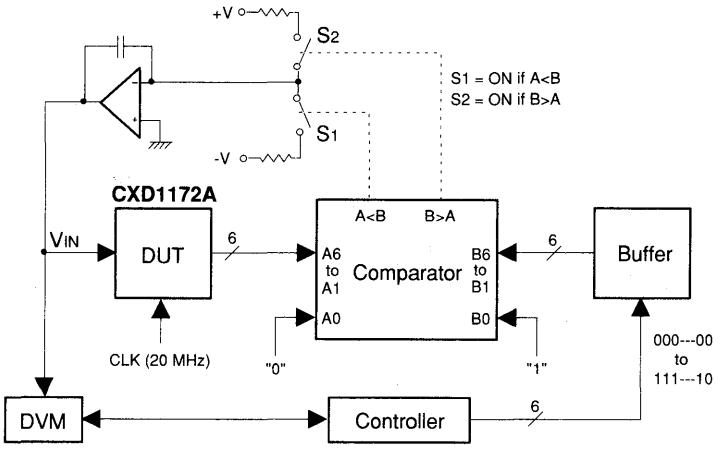
Electrical Characteristics

V_{CC} = +5V, V_{RB} = 1.0V, V_{RT} = 2.0V, Ta = 25°C

Item	Symbol	Conditions		Min.	Type	Max.	Unit
Maximum Conversion Speed	F_C	VIN = 1.0V to 2.0V FIN = 1KHz ramp		20	35		MSPS
Supply Current	I_{DD}	FC = 20MSPS NTSC ramp wave input			8		mA
Reference Pin Current	I_{REF}				3.3		mA
Analog Input Band (-1dB)	BW				20		MHz
Analog Input Capacitance	C_{IN}	V_{IN} = 1.5V + 0.07Vrms			4		pF
Reference Resistance (V_{RT} to V_{RB})	R_{REF}				300		Ω
Offset Voltage	E_{OT}				-20		mV
	E_{OB}				30		
Digital Input Voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital Input Current	I_{IH}	V_{DD} = max.	$V_{IH} = V_{DD}$			5	μA
	I_{IL}		V_{IL} = 0V			5	
Digital Output Delay	I_{OH}	V_{DD} = min.	$V_{OH} = V_{DD}$-0.5V	-1.5			mA
	I_{OL}		V_{OL} = 0.4V	4.0			
Output Data Delay	T_{DL}				18	30	ns
Integral Non-linearity	E_L	FC = 20MSPS V_{IN} = 1.0V to 2.0V			±0.3	±0.5	LSB
Differential Non-linearity	E_D	FC = 20MSPS V_{IN} = 1.0V to 2.0V			±0.3	±0.5	LSB
Differential Gain Error	DG	NTSC 40 IRE mod Ramp, FC = 14.3MSPS			10		%
Differential Phase Error	DP				1.0		deg
Aperture Jitter	Taj				40		ps
Sampling Delay	Tsd				4		ns

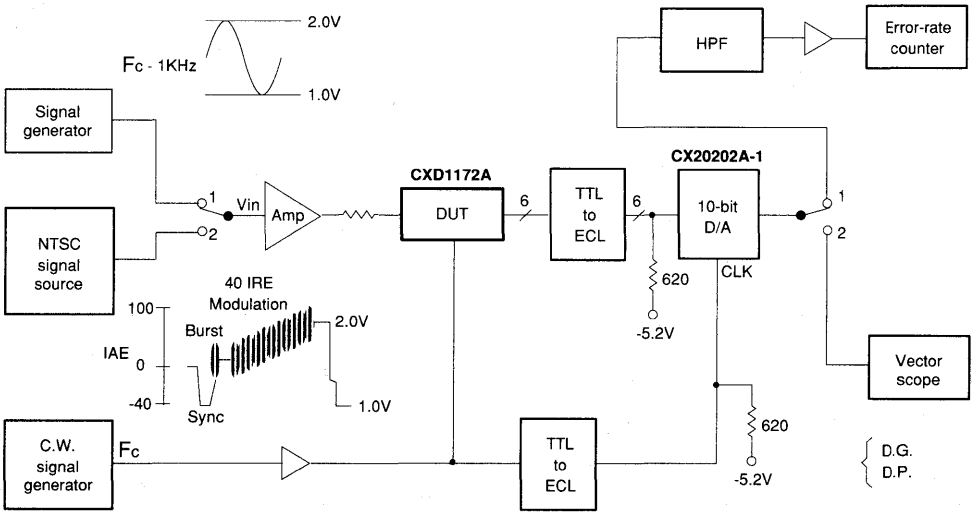
Electrical Characteristics Test Circuit

Integral non-linearity error
Differenvtial non-linearity Test Circuit
Offset voltage



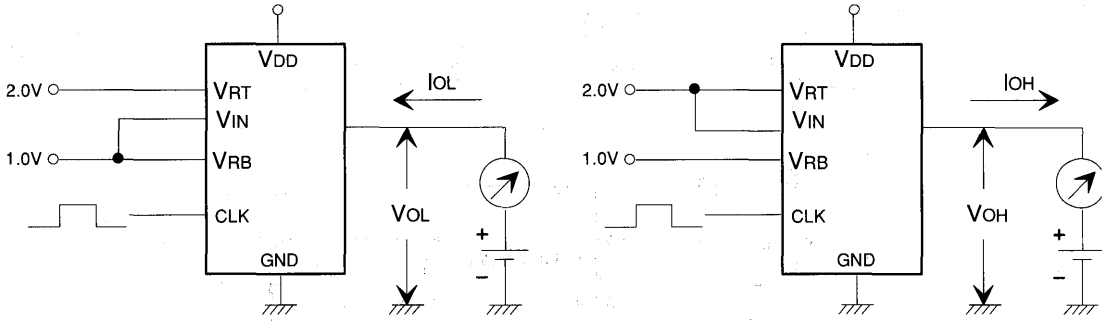
3

Maximum operational speed
Differential gain error Test Circuit
Differential phase error

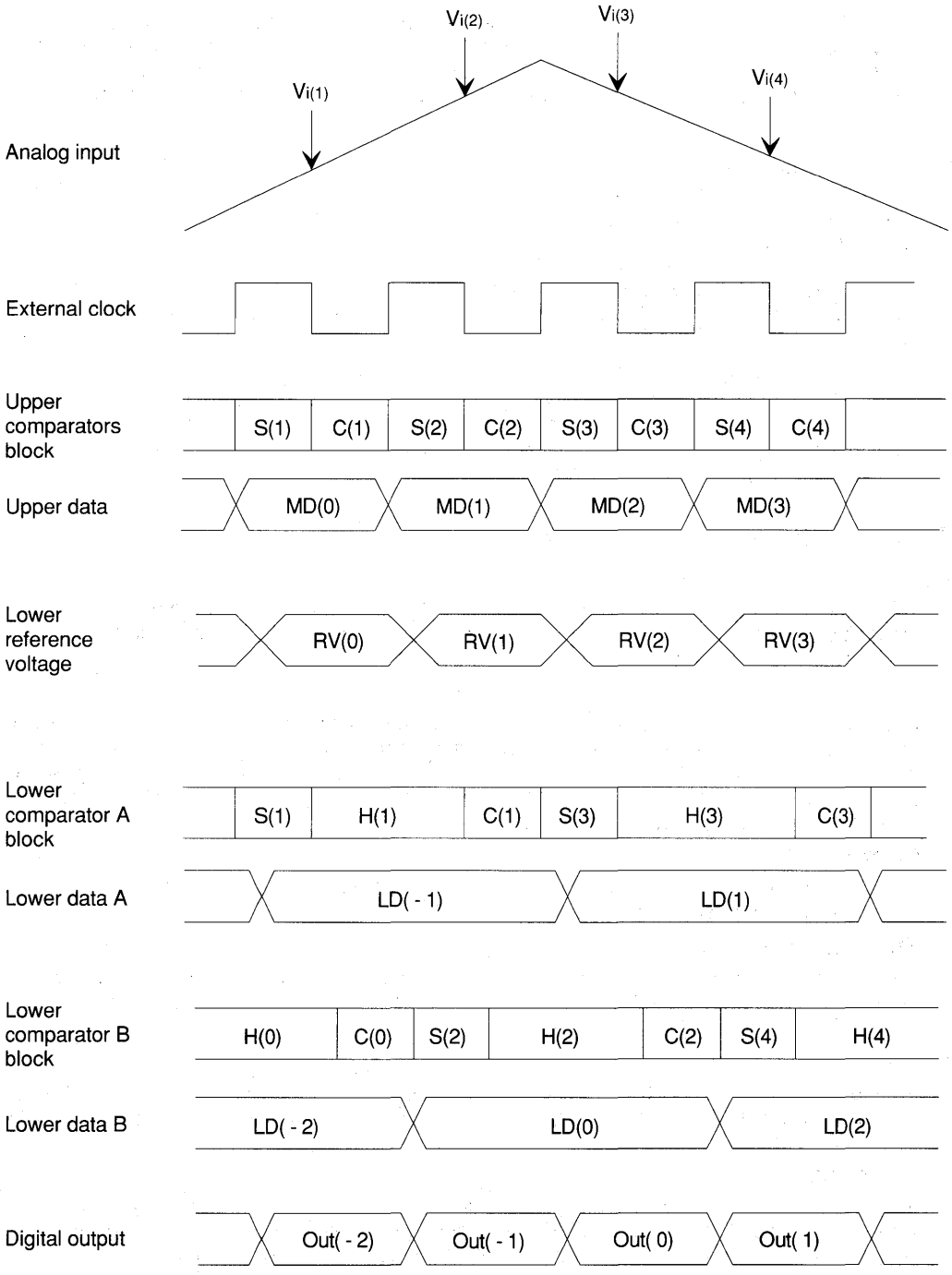


Electrical Characteristics Test Circuit

Digital output current test circuit



Timing Chart 2



3

Operation (See Black Diagram and Timing Chart)

1. CXD1172AM/AP is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between VRT-VRB/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S.H.C. symbols. That is input sampling (auto zero) mode. Input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage VI (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.

   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}

   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog VDD pins, use a ceramic capacitor of about 0.1 F set as close as possible to the pin to bypass to the respective GND's.

2. Analog Input

   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. that may be prevented by inserting a resistance of about 100 W in series between the amplifier output and A/D input.

3. Clock Input

   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference Input

   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1 mF, stable characteristics are obtained.

5. Timing

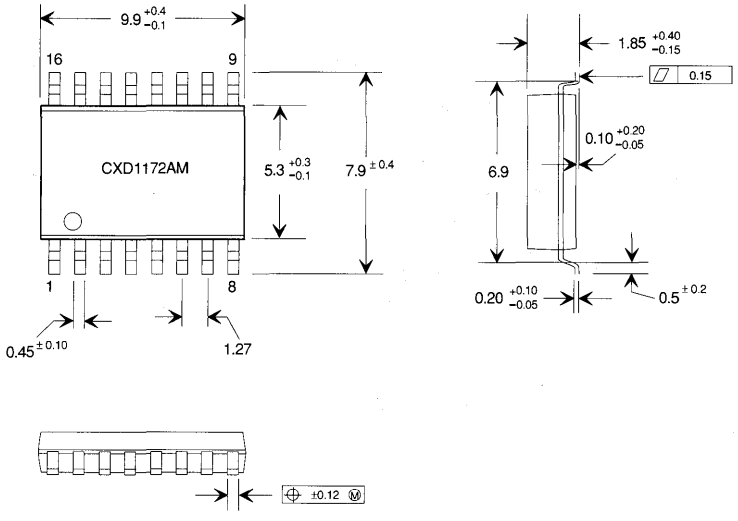
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. About Latch Up

   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply. This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON. See "For latch up prevention" of CXD1172AP/CXA1106P PCB description (Page 6. 7).

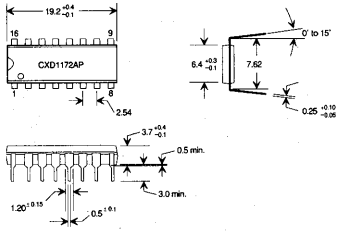
Package Outline Unit: mm

CXD1172AM 16pin SOP (Plastic) 300mil 0.2g



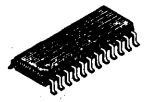
Package Outline Unit: mm

CXD1172AP 16pin DIP (Plastic) 300mil 1.0g

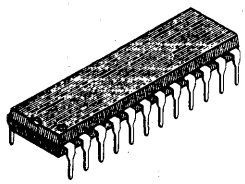


8-bit 20 MSPS Video A/D Converter (CMOS)

CXD1175AM 24 pin SOP (Plastic)



CXD1175AP 24 pin DIP (Plastic)



Description

CXD1175A is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS minimum, 35MSPS typical.

Features

- Resolution ..... 8-bit ± 1/2 LSB (DL)
- Max. sampling frequency .... 20 MSPS
- Low power consumption .... 60 mW (at 20 MSPS Typ.) (Reference current excluded)
- Built-in sampling and hold circuit.
- Built-in reference voltage self bias circuit.
- 3-state TTL compatible output.
- Power supply ..... 5V single
- Low input capacitance ..... 11 pF
- Reference impedance ..... 300Ω (Typ.)

Structure

Silicon gate CMOS monolithic IC

Applications

- TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Absolute Maximum Ratings (Ta=25°C)

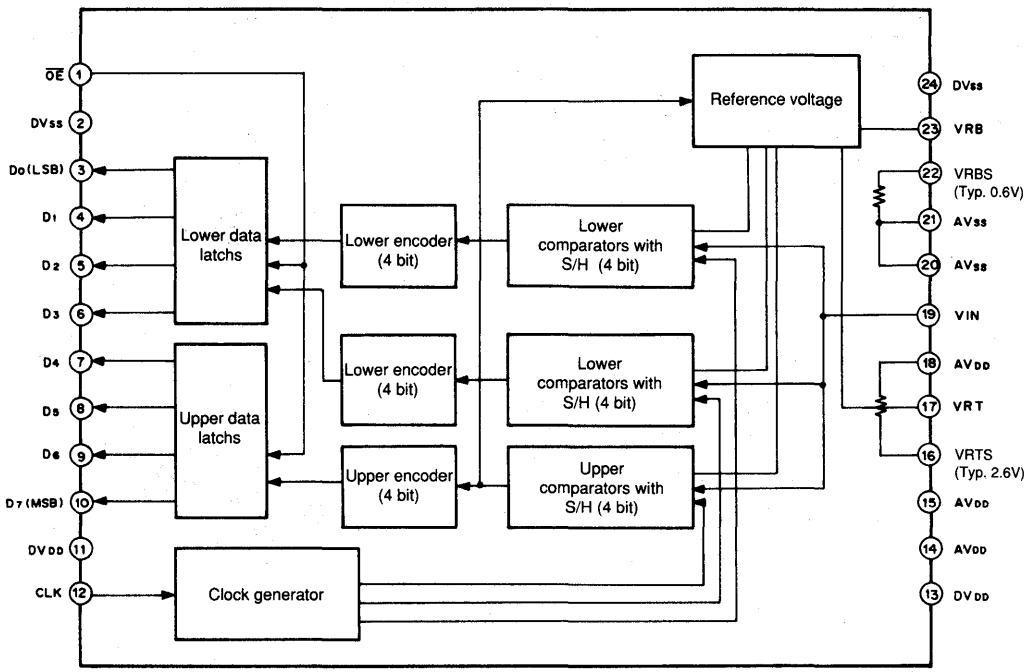
• Supply voltage	V_{DD}		7		V
• Reference voltage	V_{RT}, V_{RB}	V_{DD}	to	V_{SS}	V
• Analog input voltage	V_{IN}	V_{DD}	to	V_{SS}	V
• Digital input voltage	CLK	V_{DD}	to	V_{SS}	V
• Digital output voltage	V_{OH}, V_{OL}	V_{DD}	to	V_{SS}	V
• Storage temperature	Tstg	-55	to	+150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25		V
	DV_{DD}, DV_{SS}			
	|DGND-AGND|	0 to 100		mV
• Reference input voltage	V_{RB}	0 and above		V
	V_{RT}	2.8 and below		V
• Analog input voltage	V_{IN}	V_{RB} to V_{RT}		(1.8Vp-p to AV_{DD})
• Clock pulse width	T_{PWI}	25 (Min.)		ns
	T_{PWO}	25 (Min.)		ns
• Operating temperature	Topr	-20 to +75		°C

E89321A03-YA

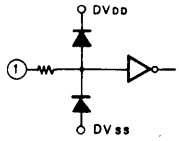
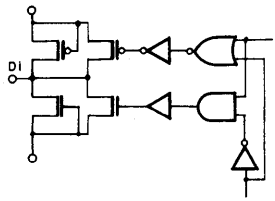
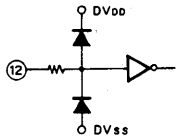
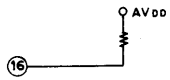
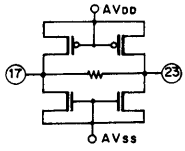
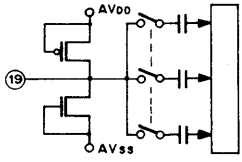
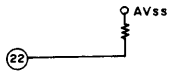
Block Diagram and Pin Configuration



For the following information, please see CXD1175AM/AP portion.

- Pin Description and Equivalent Circuits
- Description of Operation
- Application Circuit

Pin Description and Equivalent Circuits

No.	Symbol	Equivalent Circuit	Description
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is output. When $\overline{OE}$ = High, D_0 to D_7 pins turn to High impedance.
2, 24	DVSS		Digital GND
3 to 10	D_0 to D_7		D_0 (LSB) to D_7 (MSB) output
11, 13	DVDD		Digital +5V
12	CLK		Clock input
16	VRTS		Shorted with VRT generates, +2.6V.
17	VRT		Reference voltage (Top)
23	VRB		Reference voltage (Bottom)
14,15,18	AVDD		Analog +5V
19	VIN		Analog input
20, 21	AVSS		Analog GND
22	VRBS		Shorted with VRB generates +0.6V.

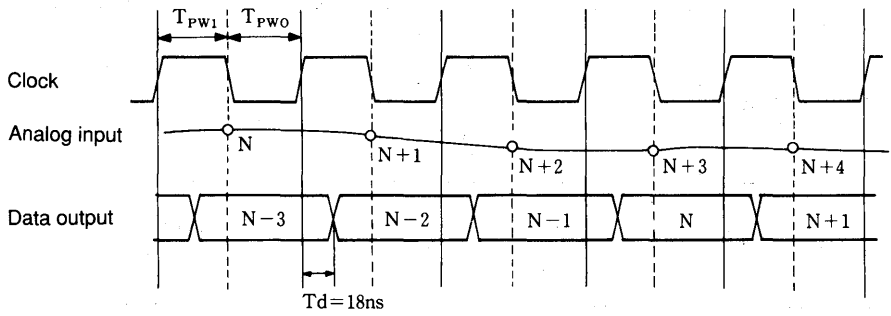
3

Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
	⋮					⋮			
	127	1	0	0	0	0	0	0	0
	128	0	1	1	1	1	1	1	1
	⋮					⋮			
V_{RB}	255	0	0	0	0	0	0	0	0

Timing Chart 1



○: Point for analog signal sampling.

Electrical Characteristics

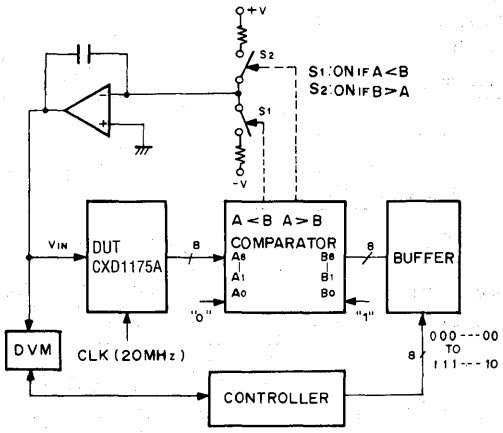
F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.6V, V_{RT} = 2.6V, Ta = 25°C

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion speed	F_C	V_{IN} = 0.6V to 2.6V F_{IN} = 1 kHz ramp		20	35		MSPS
Supply current	I_{DD}	F_C = 20 MSPS NTSC ramp wave input			12	17	mA
Reference pin current	I_{REF}			4.5	6.6	8.7	mA
Analog input band (-1dB)	BW						MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5V + 0.07 Vrms			11		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			450	300	230	Ω
Self bias 1	V_{RB1}	Short V_{RB} and V_{RBS}		0.60	0.64	0.68	V
	$V_{RT1} - V_{RB1}$	Short V_{RT} and V_{RTS}		1.96	2.09	2.21	
Self bias 2	V_{RT2}	VRB = AGND Short V_{RT} and V_{RTS}		2.25	2.39	2.53	V
Offset voltage	E_{OT}			-10	-35	-60	mV
	E_{OB}			0	+15	+45	
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max.	$V_{IH} = V_{DD}$			5	µA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = min.	$V_{OH} = V_{DD} - 0.5V$	-1.1			mA
	I_{OL}		V_{OL} = 0.4V	3.7			
Digital output current	I_{OZH}	$\overline{OE}$= V_{DD}, V_{DD} = max.	$V_{OH} = V_{DD}$			16	µA
	I_{OZL}		V_{OL} = 0V			16	
Output data delay	T_{DL}				18	30	ns
Integral non-linearity	E_L	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V			+0.5	+1.3	LSB
Differential non-linearity	E_D	F_C = 20 MSPS V_{IN} = 0.6V to 2.6V			±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, F_C = 14.3 MSPS			1.0		%
Differential phase error	DP				0.5		deg
Aperture jitter	taj				30		ps
Sampling delay	tds				4		ns

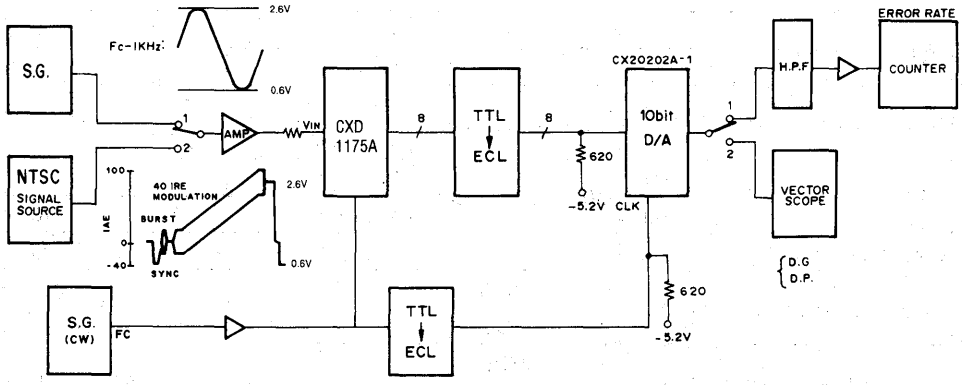
3

Electrical Characteristics Test Circuit

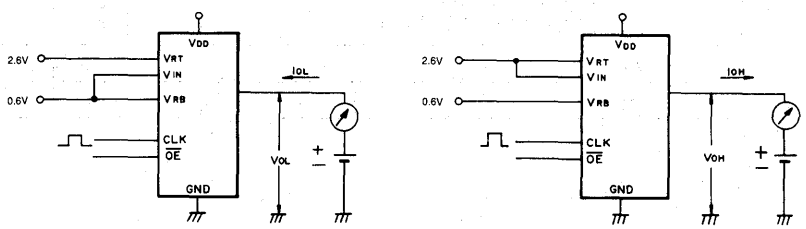
Integral non-linearity error
Differential non-linearity error
Offset voltage
} Test circuit



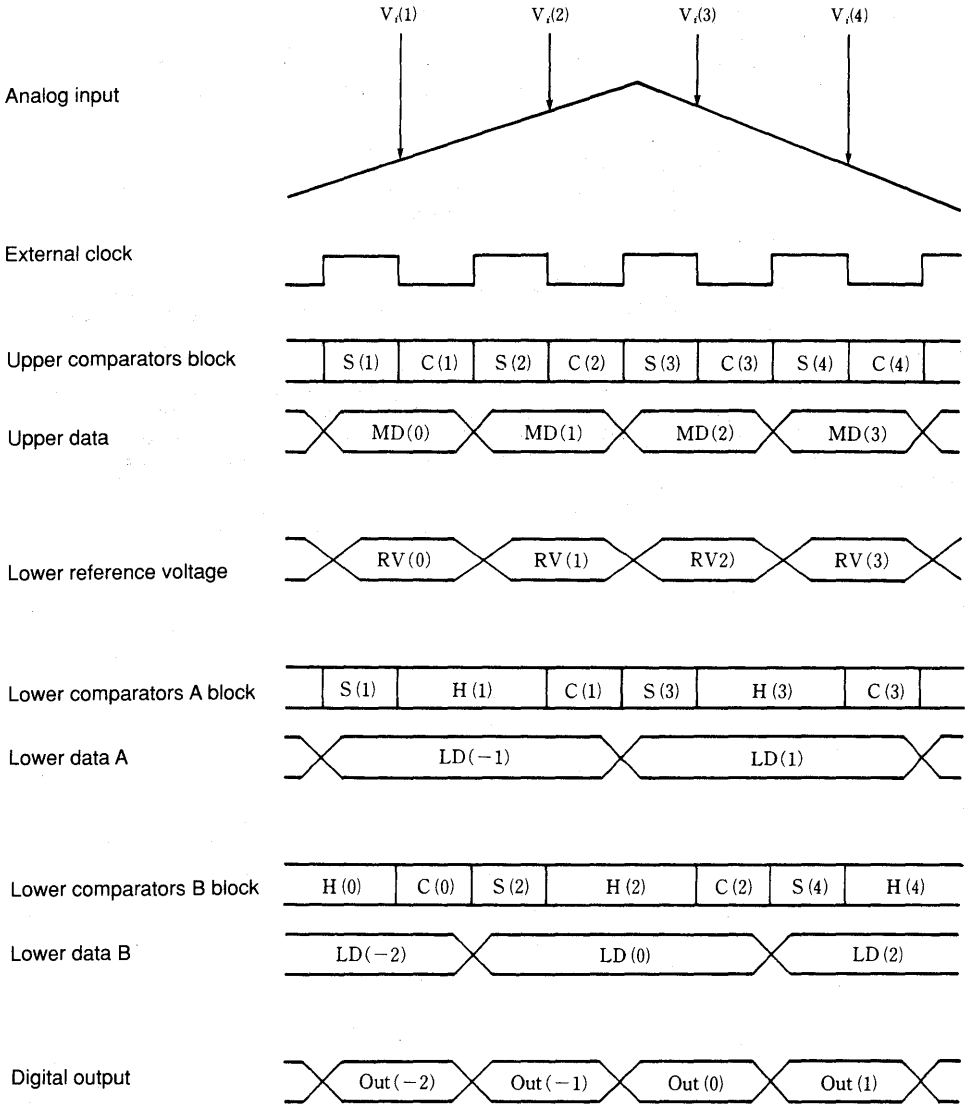
Maximum operational speed
Differential gain error
Differential phase error
} Test circuit



Digital output current test circuit



Timing Chart 2



3

Operation (See Block Diagram and Timing Chart)

1. CXD1175AM/AP is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between VRT-VRB/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins serve for the self generation of VRT (Reference voltage top) and VRB (Reference voltage bottom).

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, V_{SS}
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1μF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1μF, stable characteristics are obtained. By shorting V_{RT} and V_{RTS}, V_{RB} and V_{BRS}, the self bias function that generates V_{RT} = 2.6V and V_{RB} = 0.6V, is activated.

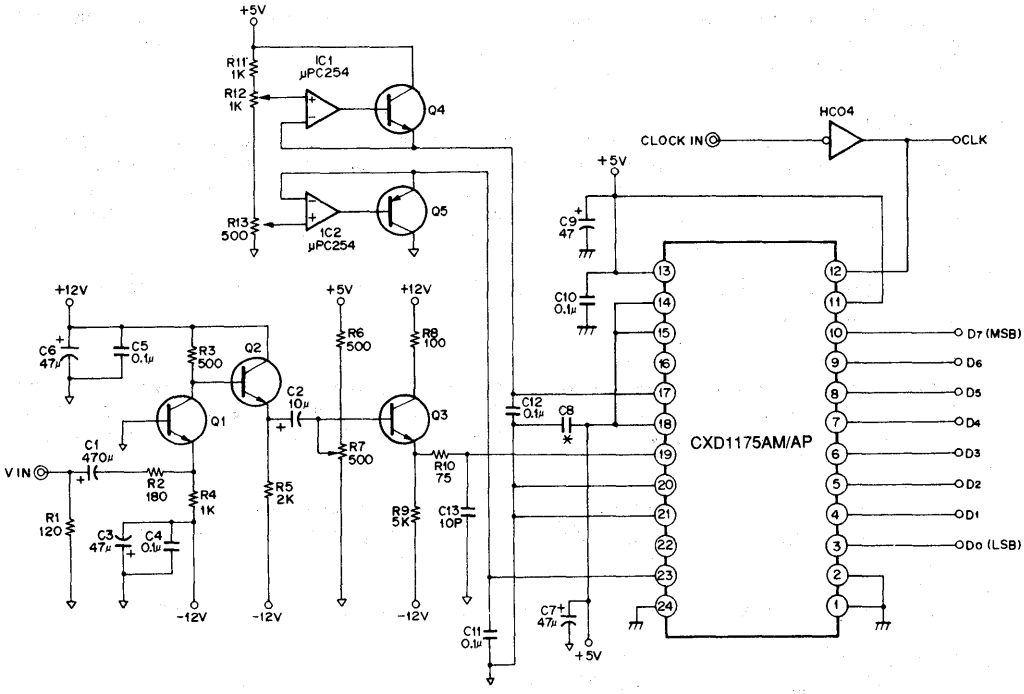
5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

6. $\overline{OE}$ pin
   By connecting $\overline{OE}$ to GND output mode is obtained. By connecting to V_{DD} high impedance is obtained.

7. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.

3

Application Circuit



* : Ceramic Chip Condenser 0.1μF

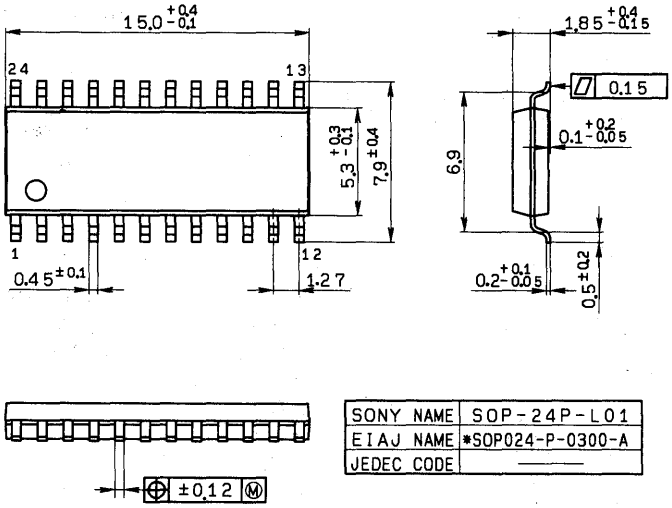
⏚ : Analog GND

⏚ : Digital GND

Note) It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply. The gain of analog input signal can be variable by adjustment of value of R3.

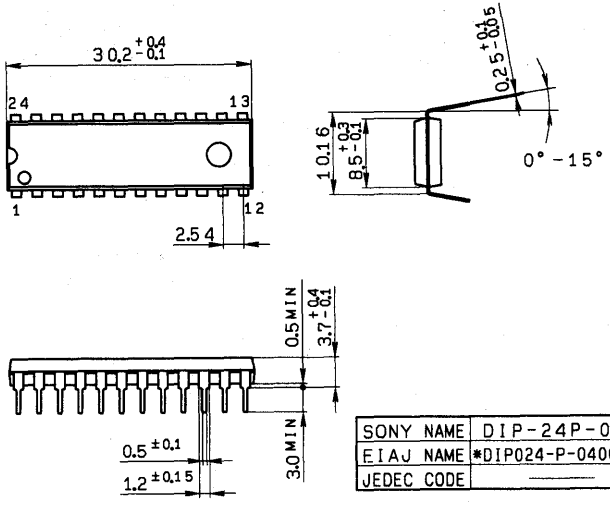
Package Outline Unit: mm

CXD1175AM 24 pin SOP (Plastic) 300 mil 0.3 g



SONY NAME	SOP-24P-L01
EIAJ NAME	*SOP024-P-0300-A
JEDEC CODE	———

CXD1175AP 24 pin DIP (Plastic) 400 mil 2.0 g



SONY NAME	DIP-24P-01
EIAJ NAME	*DIP024-P-0400-A
JEDEC CODE	———

3

SONY

CXD1176Q

8-bit 20MSPS Video A/D converter with Clamp Function

Description

The CXD1176Q is an 8-bit CMOS A/D converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 20MSPS.

Features

- Resolution power···8-bit ± 1/2 LSB (DL)
- Max. sampling frequency···20MSPS
- Low power consumption···60mW
  (at 20MSPS Typ.)
  (Reference current excluded)
- Built-in sync type clamp function
- Built-in monostable multivibrator for clamp pulse generation
- Built-in sync pulse polarity selection function
- Clamp pulse direct input possible
- Built-in clamp ON/OFF function
- Built-in reference voltage self bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 5V power supply
- Low input capacity···11pF
- Reference impedance···300 Ω (Typ.)

Applications

TV and VCR digital systems and a wide range of applications where high speed A/D conversion is required.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)

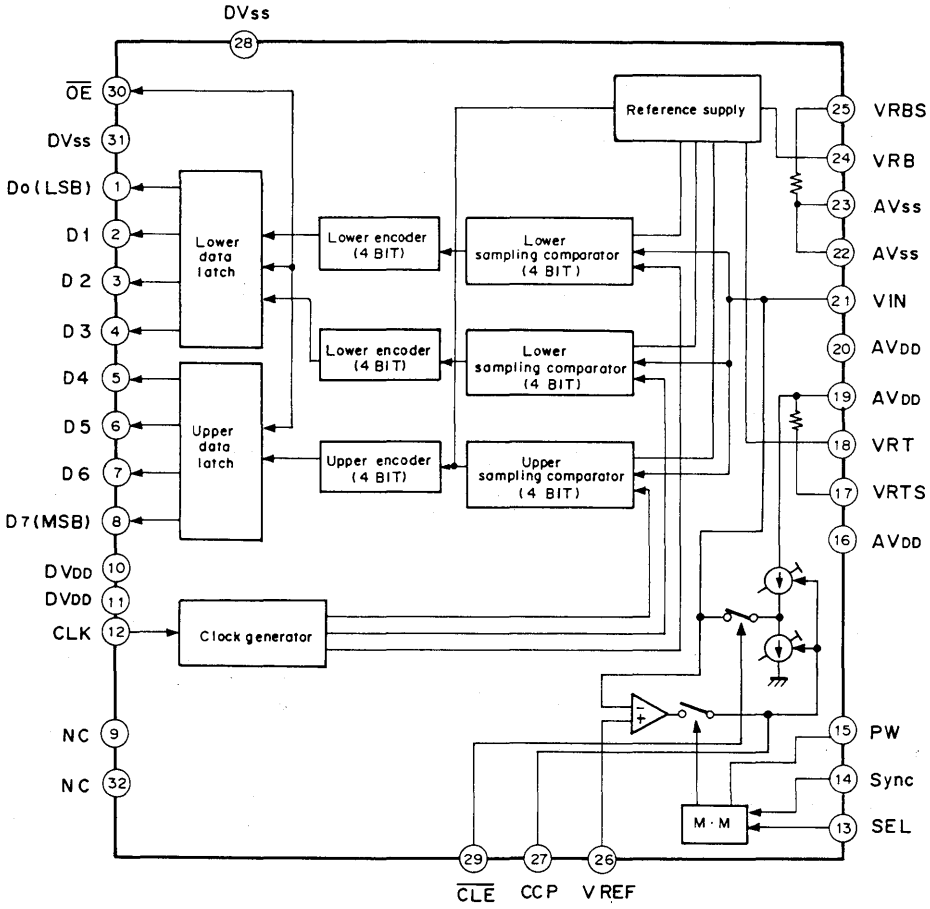
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} to Vss	V
• Input voltage (Analog)	V_{IN}	V_{DD} to Vss	V
• Input voltage (Digital)	V_{IH} V_{IL}	V_{DD} to Vss	V
• Output voltage (Digital)	V_{OH} V_{OL}	V_{DD} to Vss	V
• Storage temperature	Tstg	− 55 to + 150	°C

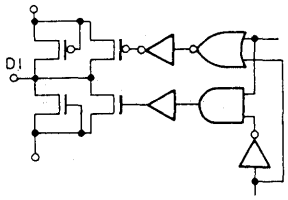
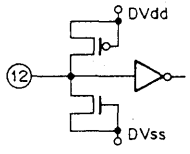
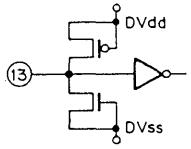
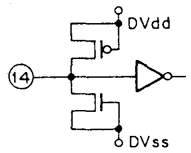
Recommended Operating Conditions

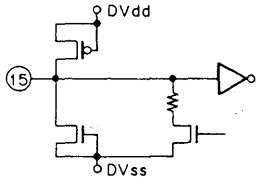
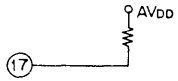
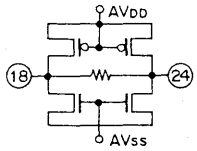
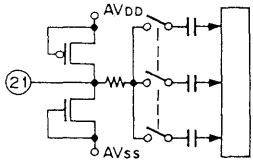
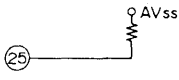
• Supply voltage			
	AV_{DD}, AVss DV_{DD}, DVss	4.75 to 5.25	V
	| DGND − AGND |	0 to 100	mV
• Reference input voltage			
	V_{RB}	0 to	V
	V_{RT}	to 2.7	V
• Analog input	V_{IN}	1.8Vp-p above	
• Clock pulse width	T_{PWI}	···25 (min)	ns
	T_{PWO}	···25 (min)	ns
• Operating ambient temperature	Topr	− 20 to + 75	°C

Block Diagram and Pin Configuration

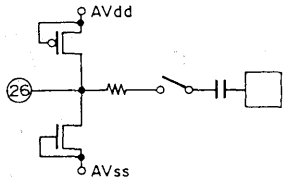
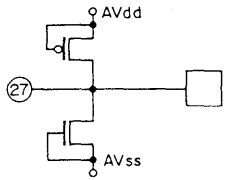
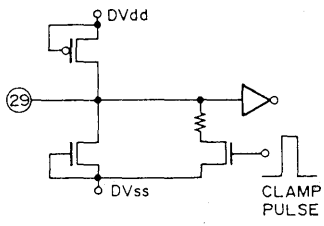
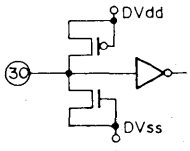


Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D_0 to D_7		D_0 (LSB) to D_7 (MSB) output
10, 11	DV_{DD}		Digital + 5V
12	CLK		Clock input
13	SEL		When SEL is at low, with the falling edge of Pin 14 (sync) as trigger, the monostable multivibrator generates clamp pulses. When SEL is at high, with the rising edge of Pin 14 (sync) as trigger, it generates clamp pulses.
14	Sync		Trigger pulse input to the monostable multivibrator. Trigger polarity can be selected through Pin 13 (SEL).

Pin No.	Symbol	Equivalent circuit	Description
15	PW		When a clamp pulse is generated at the monostable multivibrator, the pulse width is determined by the external R and C. When the clamp pulse is directly input, it is input to Pin 15 (PW). The signal voltage of the low period is clamped. (Here, Pin 14 (sync) is fixed to either low or high.)
16, 19, 20	AV_{DD}		Analog + 5V
17	VRTS		When shorted with VRT, generates approx. + 2.6V.
18	VRT		Reference voltage (Top)
24	VRB		Reference voltage (Bottom)
21	V_{IN}		Analog input
22, 23	AVss		Analog ground
25	VRBS		When shorted with VRB, generates approx. + 0.5V.

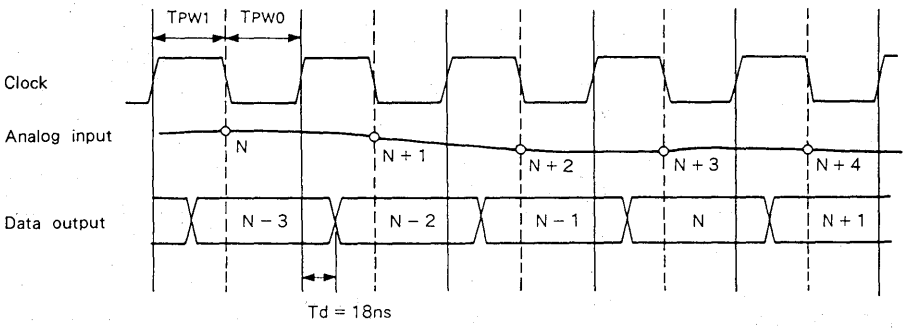
3

Pin No.	Symbol	Equivalent circuit	Description
26	VREF		Clamp reference voltage input. Clamps to provide a clamp period input signal equal to the reference voltage.
27	CCP		Integrates the voltage for clamp control. CCP and V_{IN} voltage changes are in positive phase.
28, 31	DVss		Digital ground.
29	$\overline{CLE}$		When $\overline{CLE}$ is at low, clamp function is activated. When $\overline{CLE}$ is at high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is at low, Data is output. When $\overline{OE}$ is at high, D_0 to D_7 pins turn to high impedance.

Digital Output

Correspondence between the analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
⋮	⋮	⋮
⋮	127	1 0 0 0 0 0 0 0
⋮	128	0 1 1 1 1 1 1 1
⋮	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0



○ : Points where analog signals are sampled

Timing Fig. 1.

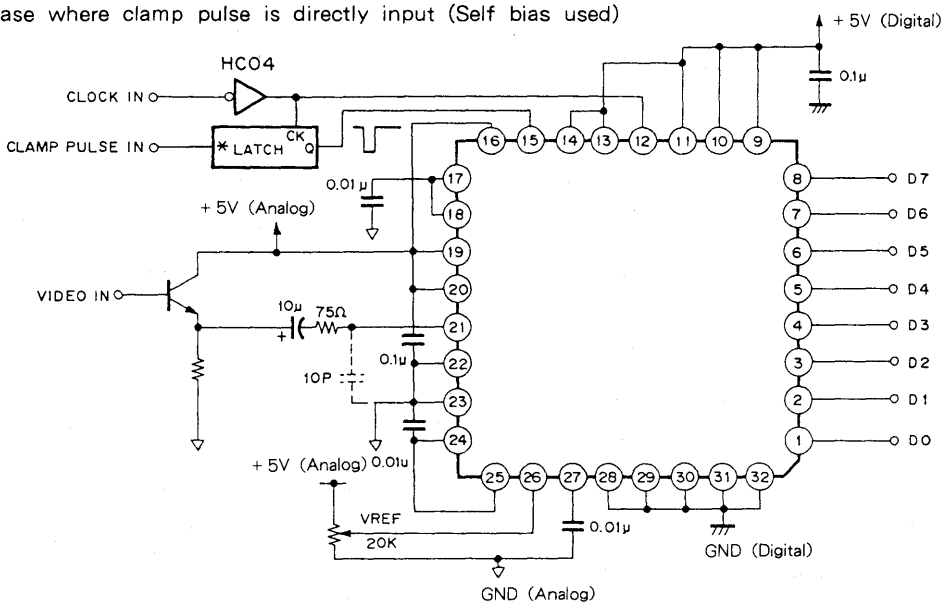
3

Electrical Characteristics (Fc = 20MSPS V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, Ta = 25°C)

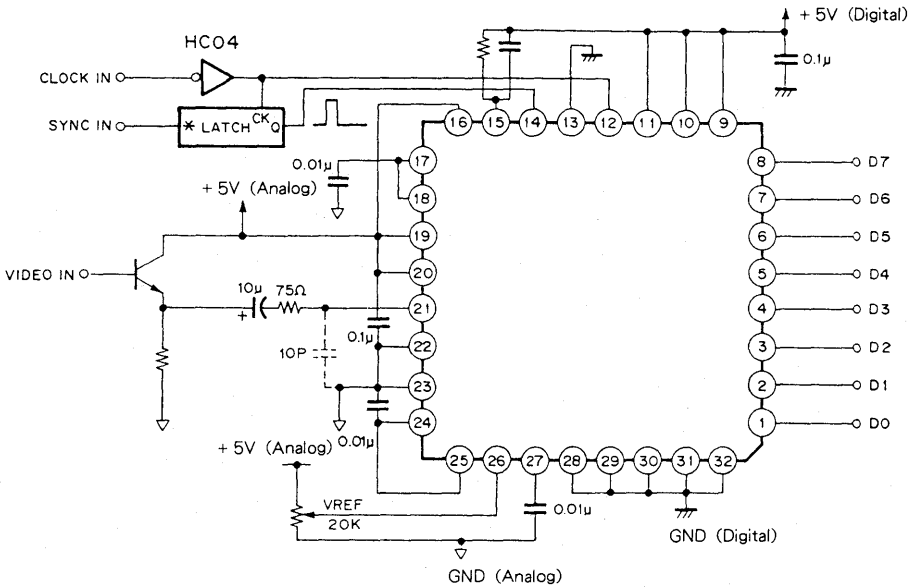
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Max. conversion speed	Fc	V_{IN} = 0.5 to 2.5V f_{IN} = 1kHz ramp		20	35		MSPS
Current power supply	I_{DD}	Fc = 20MSPS NTSC ramp wave input			12	18	mA
Reference pin current	I_{REF}			4.5	6.6	8.7	mA
Analog input band (− 1dB)	BW				18		MHz
Analog input capacity	C_{IN}	V_{IN} = 1.5V + 0.07Vrms			11		pF
Reference resistance value (V_{RT} to V_{RB})	R_{REF}			230	300	450	Ω
Self bias I	VRB_1	VRB and VRBS are shorted VRT and VRTS are shorted		0.48	0.52	0.56	V
	VRT_1 to VRB_1			1.96	2.08	2.22	
Self bias II	VRT_2	VRB = AGND VRT and VRTS are shorted			2.32		V
Offset voltage	E_{OT}			− 60	− 40	− 20	mV
	E_{OB}			+ 20	+ 40	+ 60	
Digital input voltage	V_{IH}			4.0			V
	V_{IL}					1.0	
Digital input current	I_{IH}	V_{DD} = max	$V_{IH} = V_{DD}$			5	μA
	I_{IL}		V_{IL} = 0V			5	
Digital output current	I_{OH}	$\overline{OE}$ = Vss V_{DD} = min	$V_{OH} = V_{DD}$ − 0.5V	− 1.1			mA
	I_{OL}		V_{OL} = 0.4V	3.7			
Digital output current	I_{OZH}	$\overline{OE} = V_{DD}$ V_{DD} = max	$V_{OH} = V_{DD}$			16	μA
	I_{OZL}		V_{OL} = 0V			16	
Output data delay	T_{DL}				18	30	ns
Integral nonlinear error	E_L	Fc = 20MSPS V_{IN} = 0.5 to 2.5V			+ 0.5	+ 1.3	LSB
Differential nonlinear error	E_D	Fc = 20MSPS V_{IN} = 0.5 to 2.5V			± 0.3	± 0.5	LSB
Differential gain error	DG	NTSC 40IRE mod ramp, Fc = 14.3MSPS			1.0		%
Differential phase error	DP				0.5		deg
Aperture jitter	taj				30		ps
Sampling delay	tsd				4		ns
Clamp offset voltage	Eoc	V_{IN} = DC, PWS = 3 μsec	V_{REF} = 0.5V	0	+ 20	+ 40	mV
			V_{REF} = 2.5V	− 50	− 30	− 10	
Clamp pulse width (Sync pin input)	tcpw	C = 100pF, R = 130kΩ (15PIN)		1.75	2.75	3.75	μs
Clamp pulse delay	tcpd				25		ns

Application Circuit

(1) Case where clamp pulse is directly input (Self bias used)

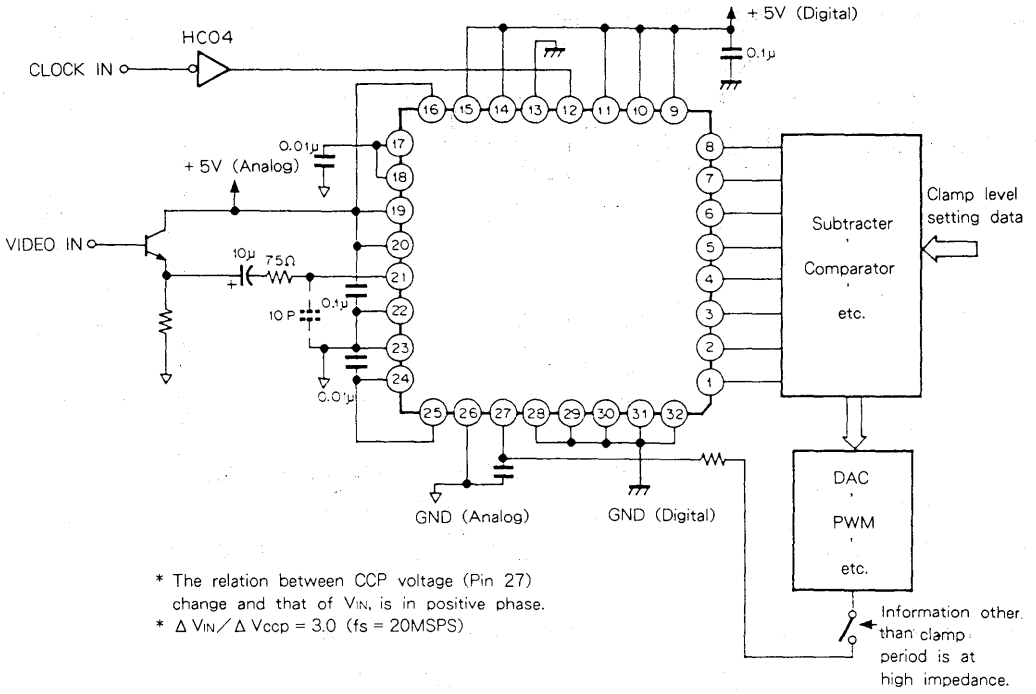


(2) Example where pedestal clamp is executed by sync pulse (Self bias used)



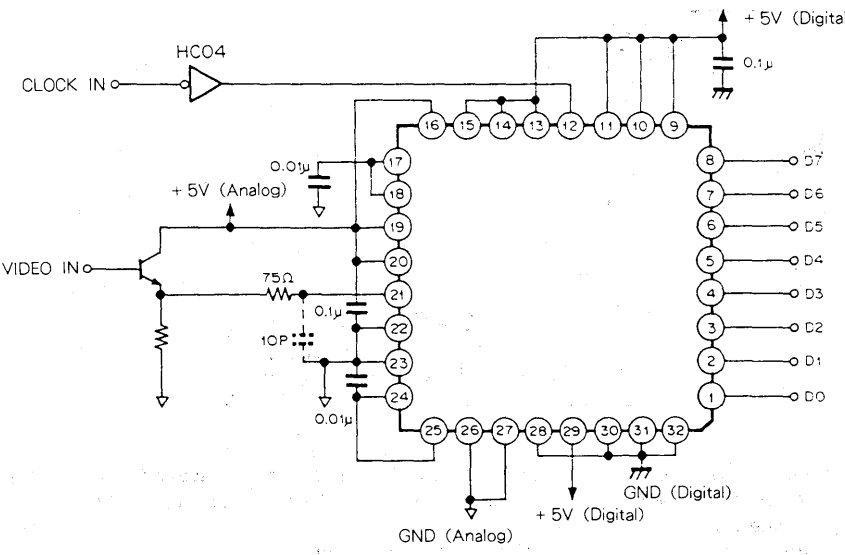
* The clamp pulse is latched by the ADC sampling clock, but that is not necessary for the clamp basic operation. However, slight beat may be generated as vertical sag according to the relation between sampling frequency and clamp pulse frequency.
At such time, the latch circuit is effective. (See Notes on Operation (5).)

(3) Digital clamp (Self bias use)



* The relation between CCP voltage (Pin 27) change and that of V_{IN}, is in positive phase.
* $\Delta V_{IN} / \Delta V_{CCP} = 3.0$ (fs = 20MSPS)

(4) When clamp is not used (Self bias use)



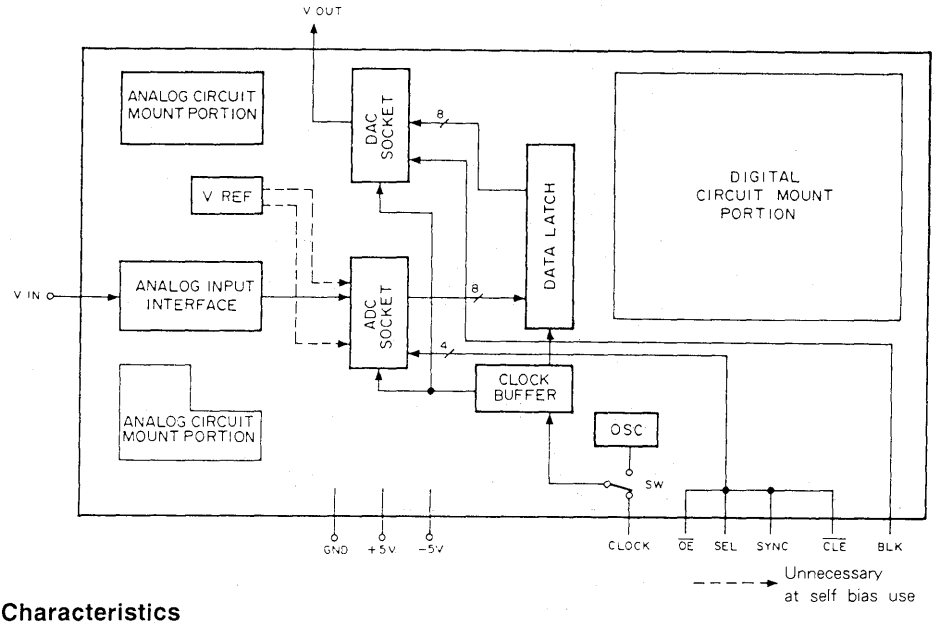
8-bit 20MSPS ADC and DAC Evaluation Board

Evaluation boards are available for the high speed, low power consumption CMOS converters, CXD1176 (8-bit 20MHz, A/D) and CXD1171M (8-bit 40MHz, D/A).

The evaluation board is composed of a main board common to either type, to which is added sub board D1176Q or sub board D1171M. The junction is made through a socket.

To the main board are mounted an input interface, clock buffer and latch. To each of the sub boards is mounted CXD1176Q and CXD1171M respectively. Those IC's are mounted according to recommended print patterns designed to provide maximum performance to the A/D and D/A converters.

Block Diagram



Characteristics

• Resolution	8bit
• Maximum conversion rate	20MHz
• Digital input level	CMOS level
• Supply voltage	±5.0V (Single +5V power supply possible at self bias use)

Supply Voltage

Item	Min.	Typ.	Max.	Unit
+5V −5V			150 20	mA

Clock Input

CMOS compatible

Pulse width T_{CW1} 25ns (min)

T_{CW0} 25ns (min)

Analog Output (CXD1171M) ($R_L > 10k\Omega$)

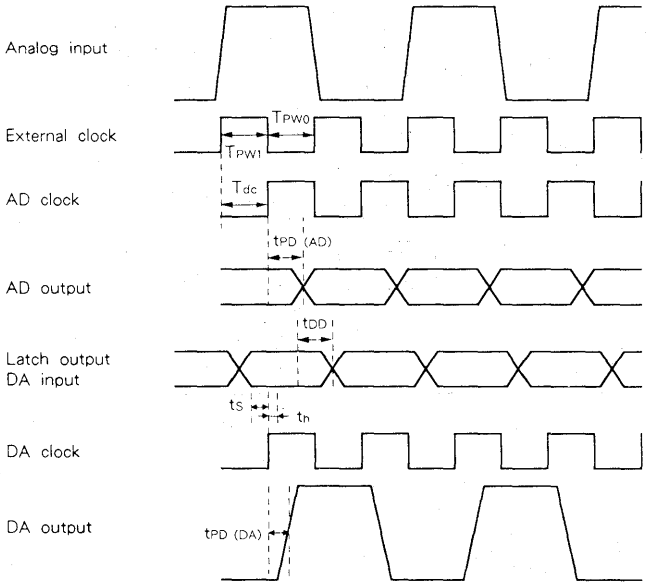
Item	Min.	Typ.	Max.	Unit
Analog output	0.5	2.0	2.1	V

Output Format (CXD1176Q)

The table shows the output format of AD Converter

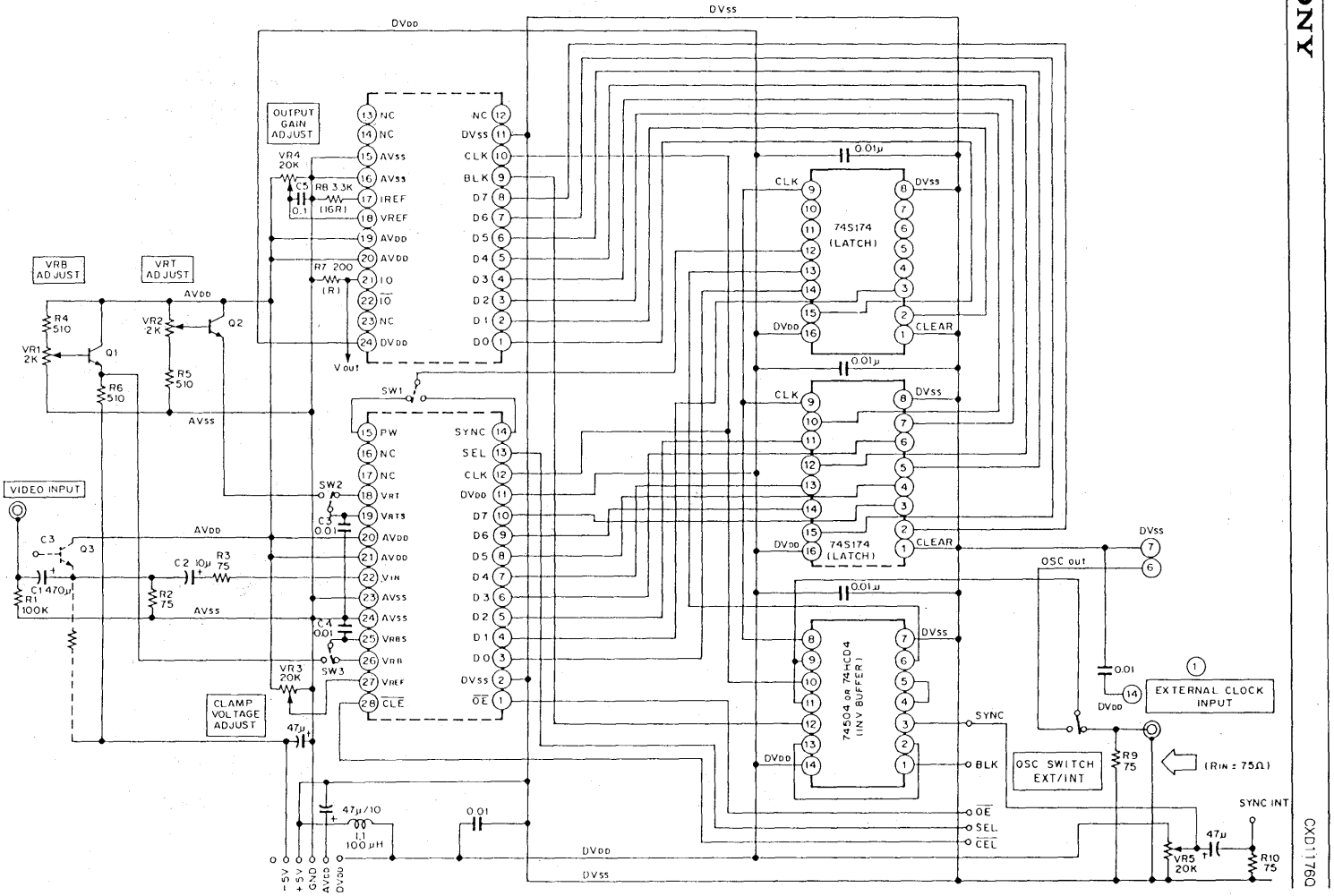
Analog input voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
⋮	⋮	⋮
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
⋮	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0

Timing Chart

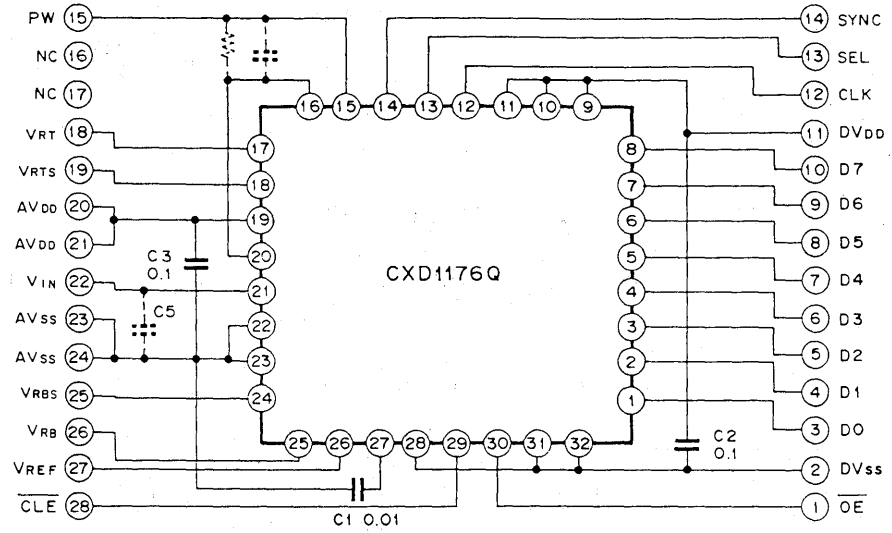


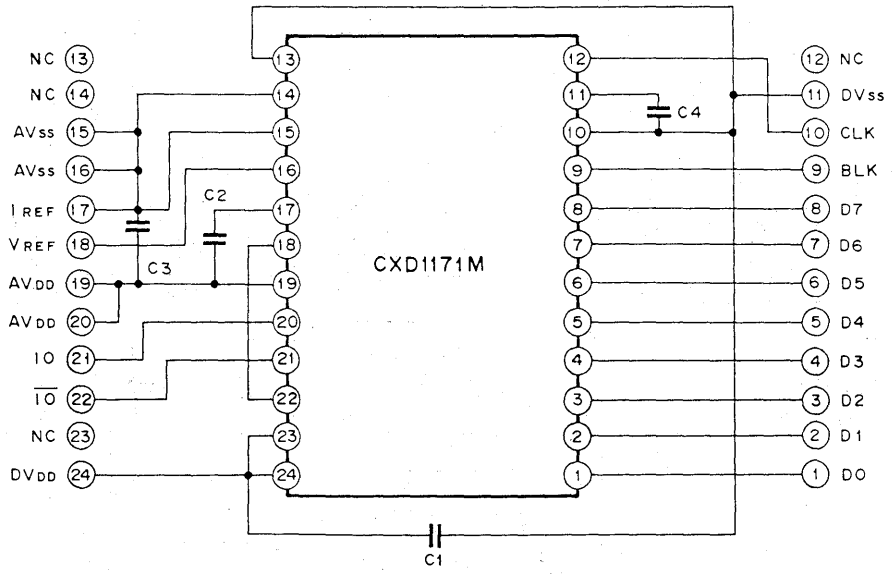
Item	Symbol	Min.	Typ.	Max.	Unit
Clock High time	T_{PW1}	25			ns
Clock Low time	T_{PW0}	25			ns
Clock Delay	Tdc			24	ns
Data delay AD	$t_{PD\ (AD)}$		18	30	ns
Data delay (latch)	t_{DD}			17	ns
Settling time	ts	10			ns
Hold time	th	2			ns
Data delay DA	$t_{PD\ (DA)}$		10		ns

CMOS ADC/DAC Peripheral Circuit Board (Main Board)



CMOS ADC/DAC Peripheral Circuit Board (Sub Board)





List of Parts

resistance	
R1	100K
R2	75 Ω
R3	75 Ω
R4	510 Ω
R5	510 Ω
R6	510 Ω
R7	R = 200
R8	18R ≒ 3.3K
R9	75 Ω
R10	75 Ω
VR1	2K
VR2	2K
VR3	20K
VR4	20K
VR5	20K

capacitance	
C1	470 μF/6.3V (chemical)
C2	10 μF/16V (chemical)
C3	0.01 μF
C4	0.01 μF
C5	0.1 μF
C6	0.1 μF
C7	0.1 μF
C8	0.1 μF
C9	0.1 μF
C10	0.1 μF
C11	47 μF/10V (chemical)
C12	47 μF/10V (chemical)
C13	47 μF/10V (chemical)
C14	0.1 μF

transistor	
Q1	2SC2785
Q2	2SC2785
Q3	2SC2785

IC	
IC1	74S174
IC2	74S174
IC3	74S04

oscillator
OSC

inductance	
L1	100 μH

others	
connector	BNC071
SW	AT1D2M3

3

Adjustment

. Vref adjustment (VR1, VR2)
Adjustment of A/D converter reference voltage. VRB is adjusted through VR1 and VRT through VR2. When self bias is used, there is no need for adjustment. Reference voltage is set through self bias at delivery.

. Setting of clamp reference voltage (VR3)
Clamp reference voltage is set.

. DAC output full scale adjustment (VR4)
Full scale voltage of D/A converter output is adjusted at the PCB shipment, the full scale voltage is adjusted to approx. 2V.

Sync (clamp) pulse interface (VR5)
This adjustment enables interface with the signal generator and others at the PCB shipment, adjustment is performed to obtain a threshold of approx. 2.5V to an H sync of 0 to 5V.

5. $\overline{OE}$, SEL, Sync, BLK, $\overline{CLE}$, Sync INT
   The following pins are set on the main board : $\overline{OE}$, SEL, Sync, $\overline{CLE}$, Sync INT (CXD1176Q) and BLK (CXD1171M). For the pins function, refer to the specifications. The difference between Sync pin and Sync INT pin is that you input a pulse above 3.5Vp-p to Sync INT pin. The pulse threshold is set through VR5. For input through Sync pin, pulse is input at TTL or CMOS level. In this case cut off the junction line between Sync pin and Sync INT pin.
   At the PCB shipment the main board pins are set as follows.
   - $\overline{OE}$ ····· Low (A/D output ON)
   - SEL ····· Low (Pulse generated with Sync falling edge as trigger)
   - Sync ····· Line junction with Sync INT pin
   - $\overline{CLE}$ ····· Low (Clamp function ON)
   - BLK ····· Low (Blanking OFF)

6. Clamp pulse input method
   One method, as shown in Application Circuit examples (1) and (2), is to directly input the clamp pulse. The other is to use the built-in monostable multivibrator. The method is selected through SW1. At the PCB shipment it is set to direct input. To use the built-in monostable multivibrator, it is necessary to mount on the CXD1176Q sub board, R and C that determine pulse width.
   (Ex. R = 130K, C = 100P, Tpw = 2.75 µs Typ.)

Points on the PCB Pattern Layout

1. Set the layout not to have Digital current flow into Analog GND (Part 1). (For 1, see P.17 Component side diagram.)

2. At CXD1176Q sub board, C_2 and C_3 capacitors serve the important role of bringing out CXD1176Q's full performance.
   These are over 0.1 µF (ceramic) capacitors with good high frequency characteristics. Layout as close to the IC as possible.

3. Analog GND (AVss) and Digital GND (DVss) are on a common voltage and power source. Keeping ADC's DVss (Part 2) as close as possible to the voltage supply source will provide better results. That is, a layout where ADC is close to the voltage supply source, is recommended. (For 2, see P.17 Component side diagram.)

4. ADC samples analog signals at the clock falling edge point. Accordingly clocks supplied to ADC should not have any jitter.

5. Inductance L1 seen on the circuit diagram serves to prevent Digital noise from affecting Analog V_{DD} when one common power source is used to supply both Analog and Digital supply systems.

6. The PCB layout shows ADC and DAC's Analog GND independently from the voltage generating source. On this PCB, the layout aims at providing an independent evaluation of ADC and DAC, as much as possible. On the actual board, common use will not cause any problems.

Notes on Operation

1. Reference voltage
   Shorting V_{RT} and V_{RTS}, V_{RB} and V_{RBS} will activate the self bias function that generates $V_{RT} = 2.6V$ and $V_{RB} = 0.5V$. On the PCB, either self bias or the external reference voltage can be selected depending on the junction method of the jumper line. At shipment from the factory, reference voltage is provided in self bias. Also, to provide external reference voltage, adjust the dynamic range ($V_{RT} - V_{RB}$) to above 1.8Vp-p.

2. Clock input
   There are 2 modes for the PCB clock input.
   1) Provided from the external signal generator (External clock)
   2) Using the crystal oscillator (built-in clock driver). (Internal clock)
   The 2 modes are selected using the switch on the PCB.

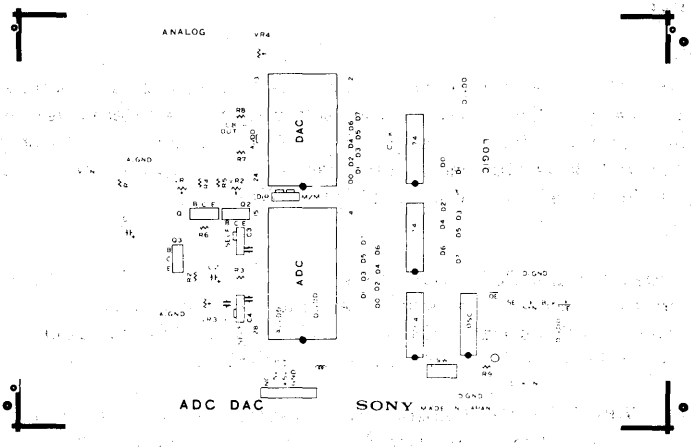
3. The 2 Latch IC's (74S174) are not absolutely necessary for the evaluation of ADC and DAC. That is, operation will still be normal if ADC output data is directly input to DAC input. However, as ADC output data is hardly ever D/A converted without executing Digital signal processing, it was mounted to indicate an example layout of Digital signal processing IC.

4. When clamp is not used
   Turning $\overline{CLE}$ to H will set OFF the clamp function. In this case, the DC element is cut off by means of C_2 on the main board and DC voltage on the ADC side of C_2 turns to about 1/2 ($V_{RT} + V_{RB}$). To transfer DC elements of input signals, short C_2. At that time, it is necessary to bias input signals, but keeping R_2 open, Q_3 can also be used as buffer. Use the open space for the bias circuit.

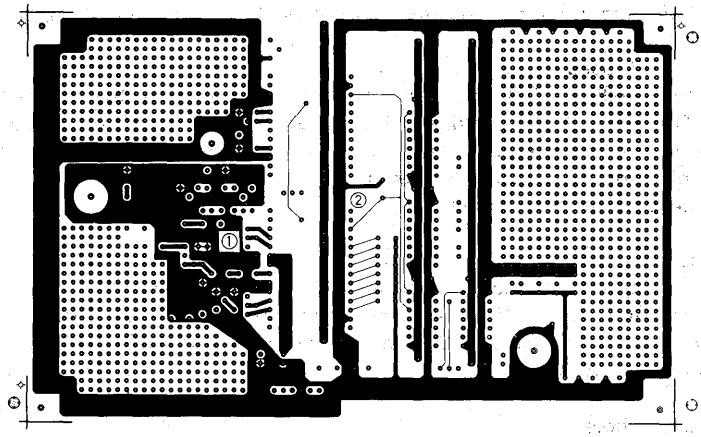
5. Clamp pulse latch
   On the evaluation board, the clamp pulse is latched with ADC sampling CLK and then input to either PW pin or Sync pin. This is to minimize Vsag due the synchronizing of noise and clamp pulse beat elements with GND sampling clock around ADC. If there are no problems with Vsag, latch is not necessary.

6. Peripheral through hole
   There is a group of through holes on the Analog input, output and Logic. These are to be used when mounting additional circuits to the PCB. Use when necessary.
   The connector hole on DAC part is used to mount the test chassis and the mount jack.

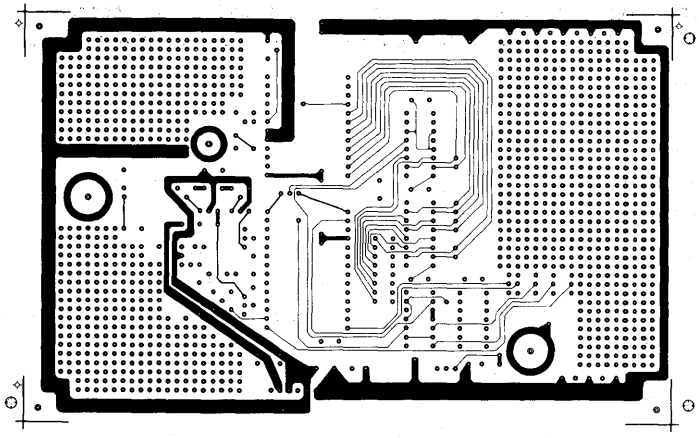
Silk Side



Component Side

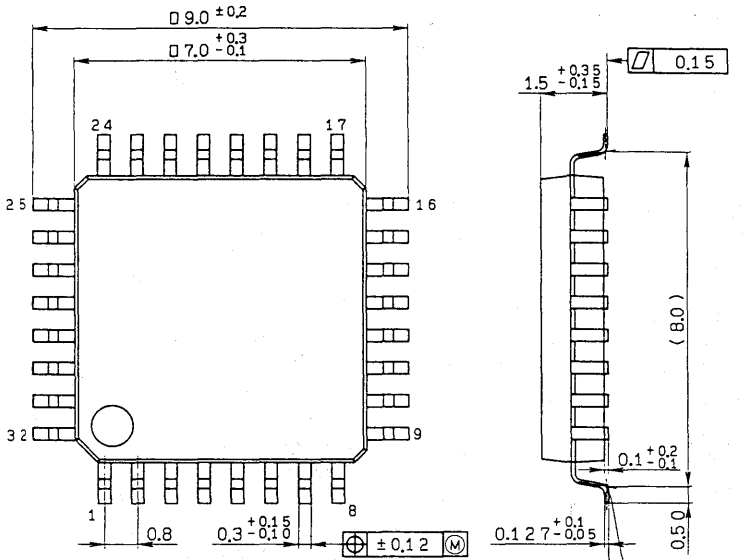


Soldering Side (Diagram seen from the component side)



Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

3

SONY

CXD1179Q

8-bit 35MSPS Video A/D converter with Clamp Function *Preliminary*

Description

The CXD1179Q is an 8-bit CMOS A/D converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 35MSPS.

Features

- Resolution power...8-bit ± 1/2 LSB (DL)
- Max. sampling frequency...35MSPS
- Low power consumption...90mW
  (at 35MSPS Typ.)
  (Reference current excluded)
- Built-in sync type clamp function
- Built-in clamp ON/OFF function
- Built-in reference voltage self bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 5V power supply
- Low input capacity...8pF
- Reference impedance...330 Ω (Typ.)

Applications

TV and VCR digital systems and a wide range of applications where high speed A/D conversion is required.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)

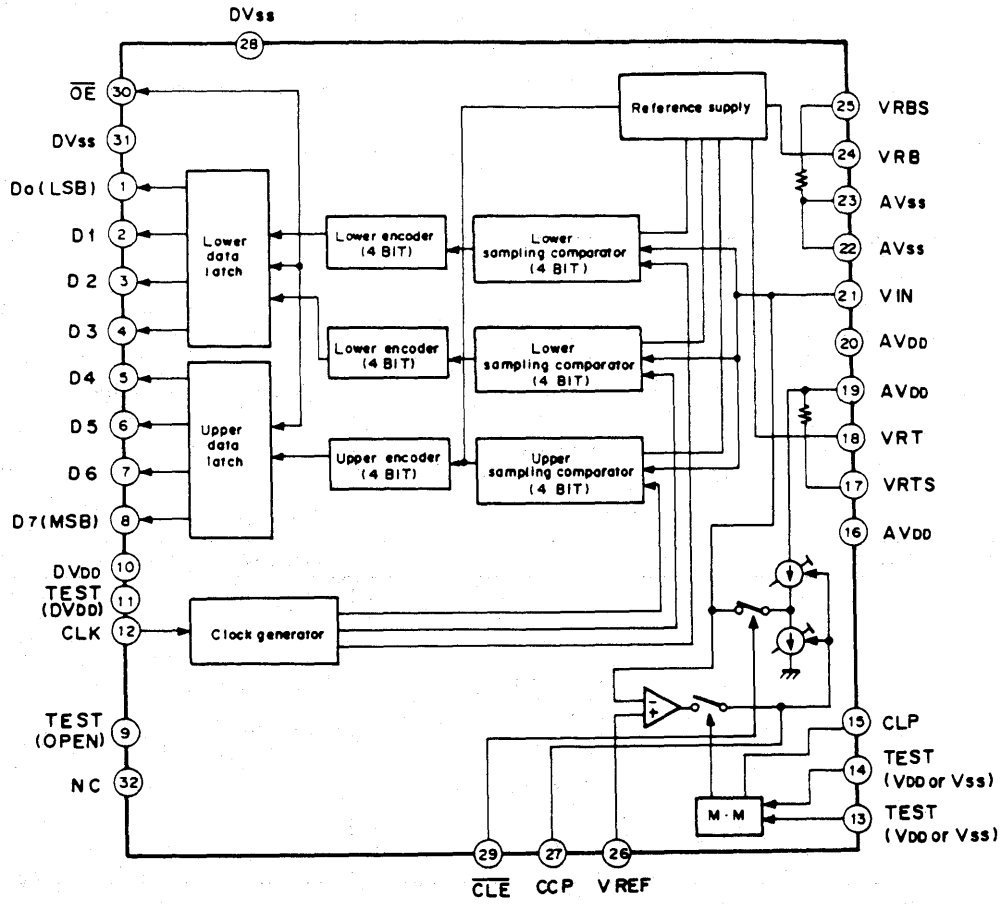
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} to Vss	V
• Input voltage (Analog)	V_{IN}	V_{DD} to Vss	V
• Input voltage (Digital)	V_{IH} V_{IL}	V_{DD} to Vss	V
• Output voltage (Digital)	V_{OH} V_{OL}	V_{DD} to Vss	V
• Storage temperature	Tstg	−55 to +150	°C

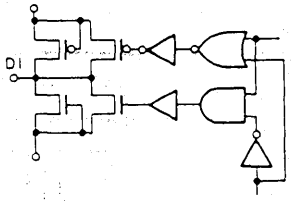
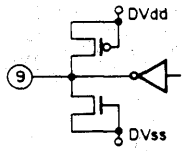
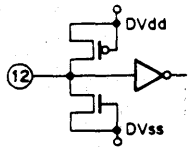
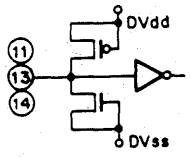
Recommended Operating Conditions

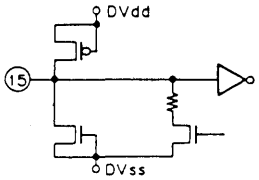
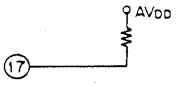
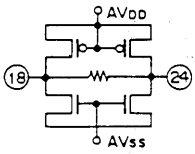
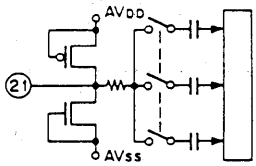
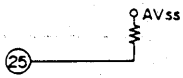
• Supply voltage	AV_{DD}, AVss DV_{DD}, DVss	4.75 to 5.25	V
	|DGND–AGND|	0 to 100	mV
• Reference input voltage	V_{RB}	0 to	V
	V_{RT}	to 2.7	V
• Analog input	V_{IN}	1.8Vp-p above	
• Clock pulse width	T_{PWI}...14 (min)		ns
	T_{PWO}...14 (min)		ns
• Operating ambient temperature	Topr	−20 to +75	°C

Block Diagram and Pin Configuration

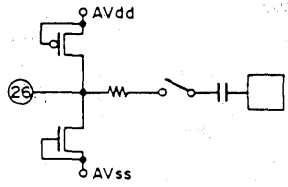
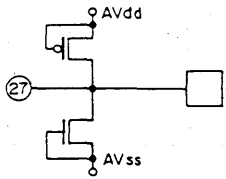
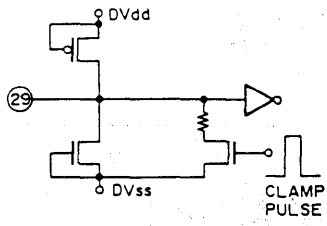
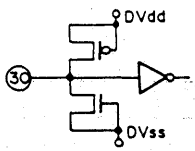


Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D_0 to D_7		D_0 (LSB) to D_7 (MSB) output
9	TEST		Set to open at normally use.
10	DV_{DD}		Digital +5V
12	CLK		Clock input
11, 13, 14	TEST		Under normal operation, Pin 11 is fixed to V_{DD}, and Pins 13 and 14 are fixed to either V_{DD} or Vss.

Pin No.	Symbol	Equivalent circuit	Description
15	CLP		When the clamp pulse is directly input, it is input to Pin 15 (CLP). The signal voltage of the low period is clamped.
16, 19, 20	AVDD		Analog +5V
17	VRTS		When shorted with VRT, generates approx. +2.6V.
18	VRT		Reference voltage (Top)
24	VRB		Reference voltage (Bottom)
21	VIN		Analog input
22, 23	AVss		Analog ground
25	VRBS		When shorted with VRB, generates approx. +0.5V.

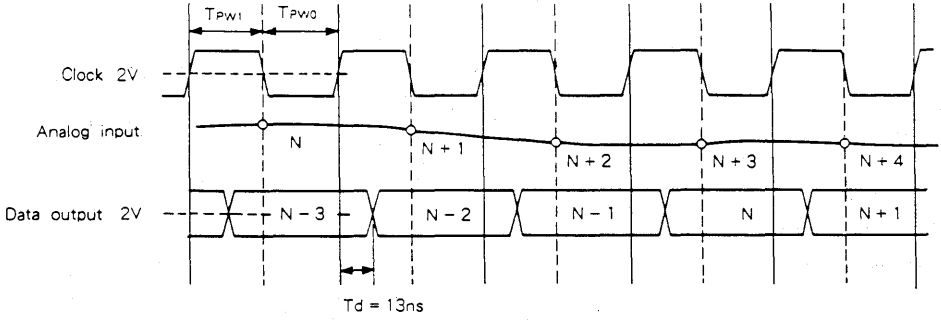
3

Pin No.	Symbol	Equivalent circuit	Description
26	VREF		Clamp reference voltage input. Clamps to provide a clamp period input signal equal to the reference voltage.
27	CCP		Integrates the voltage for clamp control. CCP and V_{IN} voltage changes are in positive phase.
28, 31	DVss		Digital ground.
29	$\overline{CLE}$		When $\overline{CLE}$ is at low, clamp function is activated. When $\overline{CLE}$ is at high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is at low, Data is output. When $\overline{OE}$ is at high, D_0 to D_7 pins turn to high impedance.

Digital Output

Correspondence between the analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
⋮	⋮	⋮
	127	1 0 0 0 0 0 0 0
	128	0 1 1 1 1 1 1 1
⋮	⋮	⋮
V_{RB}	255	0 0 0 0 0 0 0 0



○: Points where analog signals are sampled

Timing Fig. 1.

3

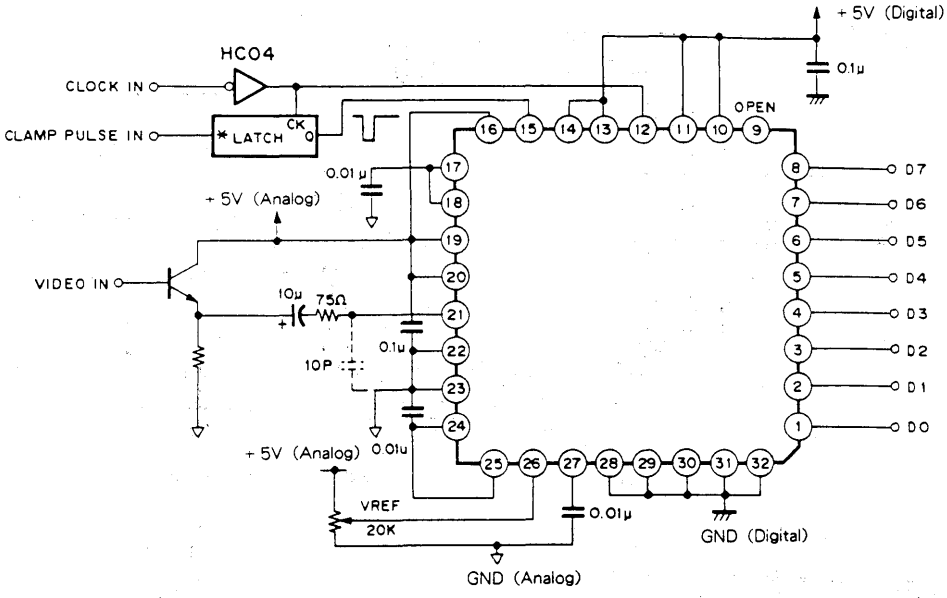
Electrical Characteristics

(F_C=35MSPS V_{DD}=+5V, V_{RB}=0.5V, V_{RT}=2.5V, Ta=25°C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Max. conversion speed	Fc	V_{IN}=0.5 to 2.5V f_{IN}=1kHz ramp		35			MSPS
Current power supply	I_{DD}	Fc=35MSPS NTSC ramp wave input			18		mA
Reference pin current	I_{REF}				6.1		mA
Analog input band (−1dB)	BW						MHz
Analog input capacity	C_{IN}	V_{IN}=1.5V+0.07Vrms			8		pF
Reference resistance value (V_{RT} to V_{RB})	R_{REF}				330		Ω
Self bias I	VRB_1	VRB and VRBS are shorted VRT and VRTS are shorted			0.54		V
	VRT_1 to VRB_1				2.08		
Self bias II	VRT_2	VRB=AGND VRT and VRTS are shorted			2.33		V
Offset voltage	E_{OT}						mV
	E_{OB}						
Digital input voltage	V_{IH}			3.5			V
	V_{IL}					0.5	
Digital input current	I_{IH}	V_{DD}=max	V_{IH}=V_{DD}			5	μA
	I_{IL}		V_{IL}=0V			5	
Digital output current	I_{OH}	$\overline{OE}$=Vss V_{DD}=min	V_{OH}=V_{DD}−0.5V		−2.5		mA
	I_{OL}		V_{OL}=0.4V		6.5		
Digital output current	I_{OZH}	$\overline{OE}$=V_{DD} V_{DD}=max	V_{OH}=V_{DD}			16	μA
	I_{OZL}		V_{OL}=0V			16	
Output data delay	T_{DL}				13		ns
Integral nonlinear error	E_L	Fc=35MSPS V_{IN}=0.5 to 2.5V			+0.5	+1.3	LSB
Differential nonlinear error	E_D	Fc=35MSPS V_{IN}=0.5 to 2.5V			±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40IRE mod ramp, Fc=14.3MSPS					%
Differential phase error	DP						deg
Aperture jitter	taj				30		ps
Sampling delay	tsd				2		ns
Clamp offset voltage	Eoc	V_{IN}=DC, PWS=3 μsec	V_{REF}=0.5V		+10		mV
			V_{REF}=2.5V		−35		
Clamp pulse delay	tcpd				25		ns

Application Circuit

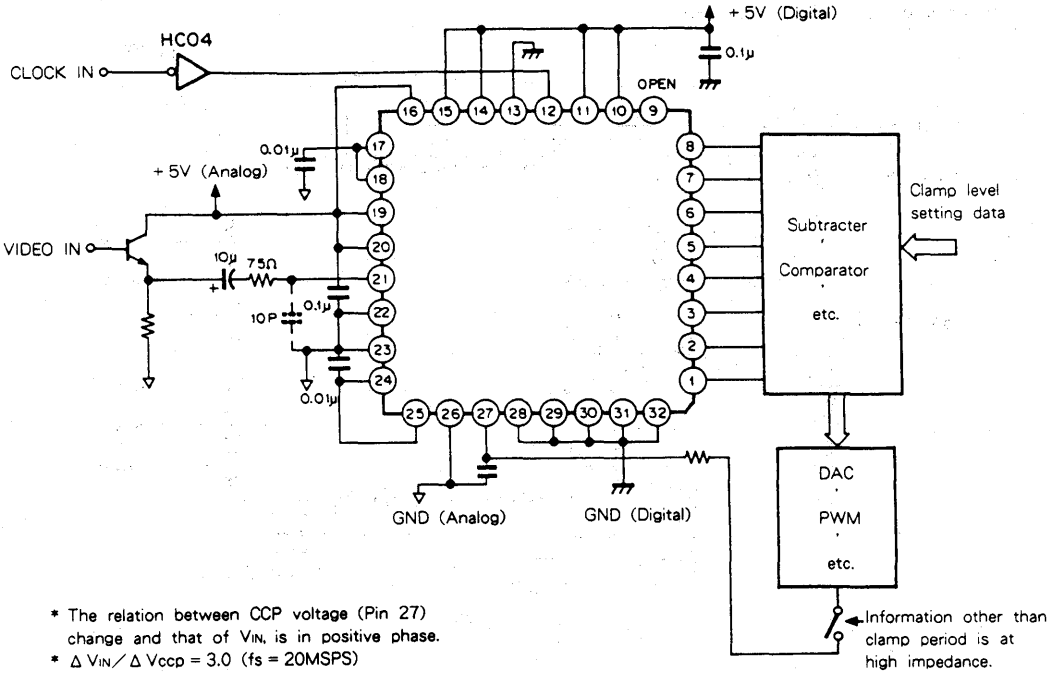
(1) When clamp is used (Self bias used)



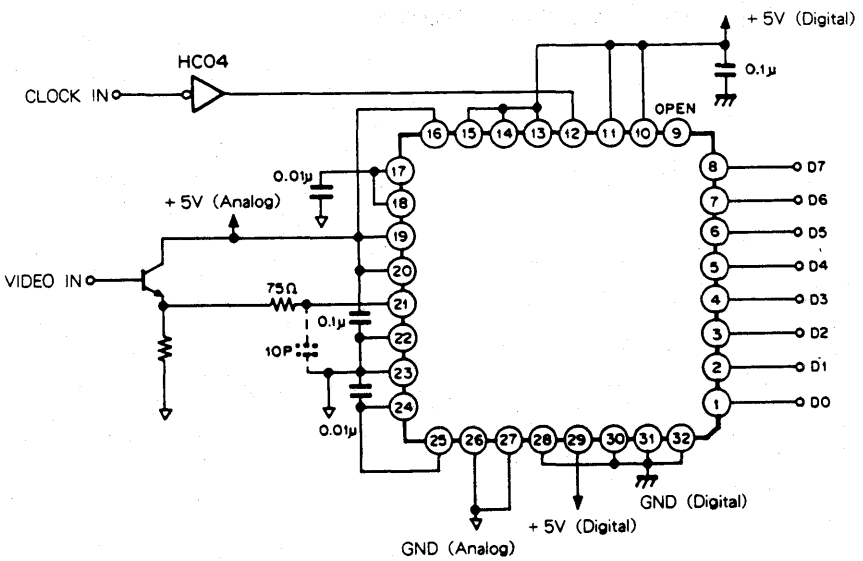
* The clamp pulse is latched by the ADC sampling clock, but that is not necessary for the clamp basic operation. However, slight beat may be generated as vertical sag according to the relation between sampling frequency and clamp pulse frequency.
  At such time, the latch circuit is effective. (See Notes on Operation (5).)

3

(2) Digital clamp (Self bias use)

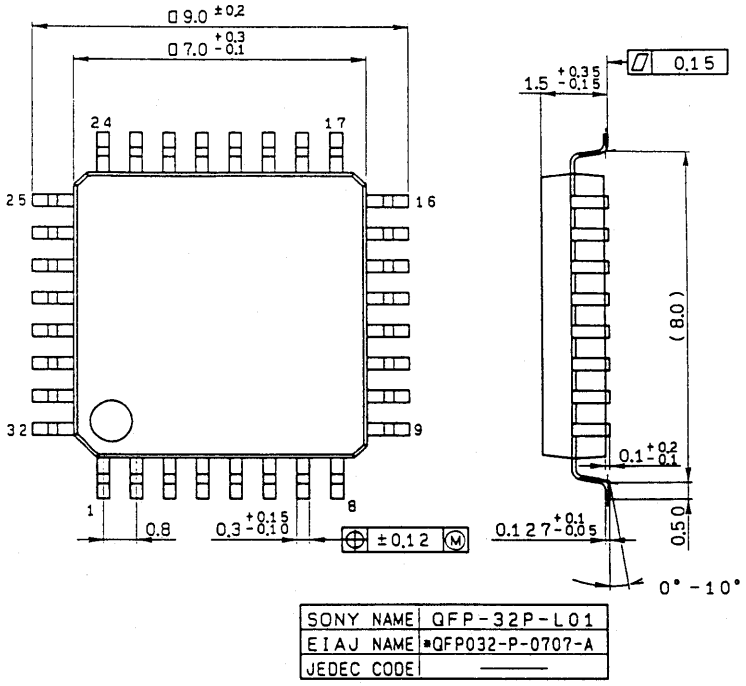


(3) When clamp is not used (Self bias use)

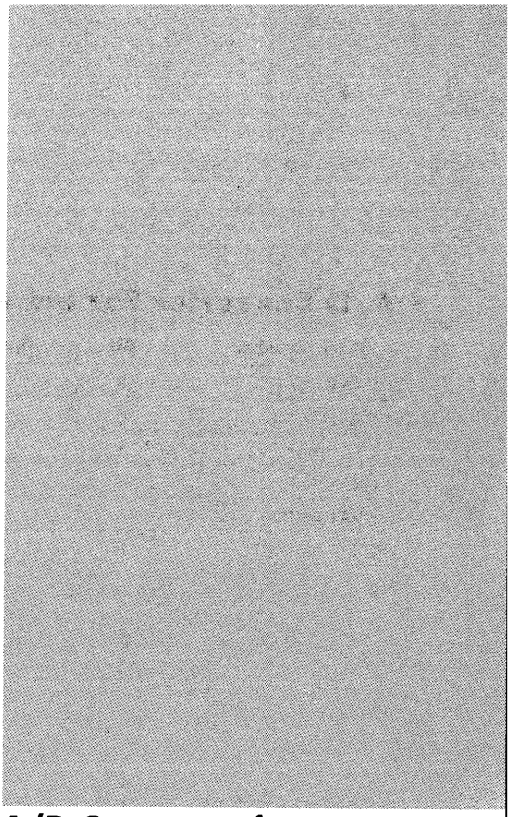


Package Outline Unit : mm

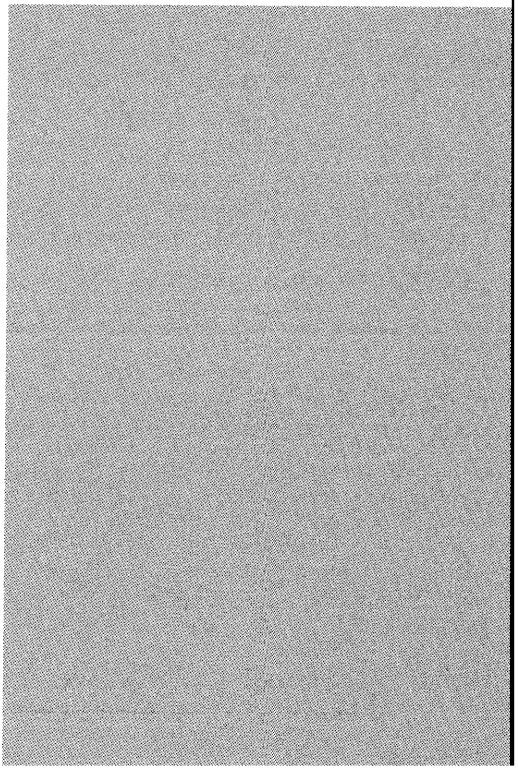
32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———



A/D Converter for Industries Instruments



A/D Converter For Industries Instruments

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CXA1076AK	8	200	1450	Flash, ECL I/O	159-174
CXA1176AK	8	300	1450	Flash, ECL I/O	159-174
CXA1166K	8	250	1700	Flash, ECL I/O	175-186
CXA1276K	8	500	2200	Flash, ECL I/O	187-197
CXA1386P/K	8	75	580	Flash, ECL I/O	198-208
CXA1396D/K	8	125	870	Flash, ECL I/O	209-220

SONY® CXA1076AK/CXA1176AK

8-bit 200/300 MSPS Flash A/D Converter (ECL I/O)

Description

CXA1076AK/CXA1176AK are monolithic flash A/D converters capable of digitizing 0 to −2 V analog input signal into 8-bit binary code at a sampling rate of 200MSPS (CXA1076AK)/ 300MSPS (CXA1176AK).

They operate with a single −5.2 V power supply and consume only 1450 mW.

In addition to 8-bit output data, they have an over range output and two digital inputs which enable to program output format for true or inverse binary and offset two's complement.

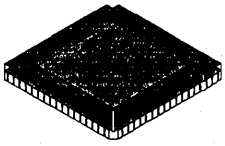
Features (CXA1076AK/CXA1176AK)

- Ultra high speed 200/300 MSPS
- Wide input band width 200/230 MHz
- Low power consumption 1450 mW
- Internal linearity compensation circuit
- Complementary ECL output
- Over range output
- Programmable output format
- Small 68 LCC package
- Pin replacable with CXA1076K/CXA1176K

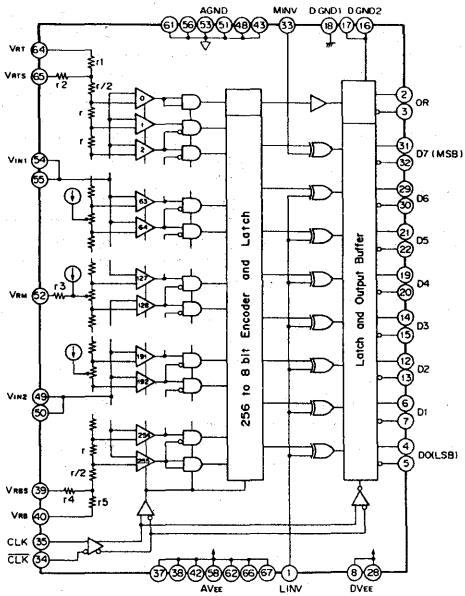
Applications

Digital oscilloscope, radar, image processing, transient capture and fast digital signal processing.

68 pin LCC (Ceramic)



Block Diagram



4

E89730-YA

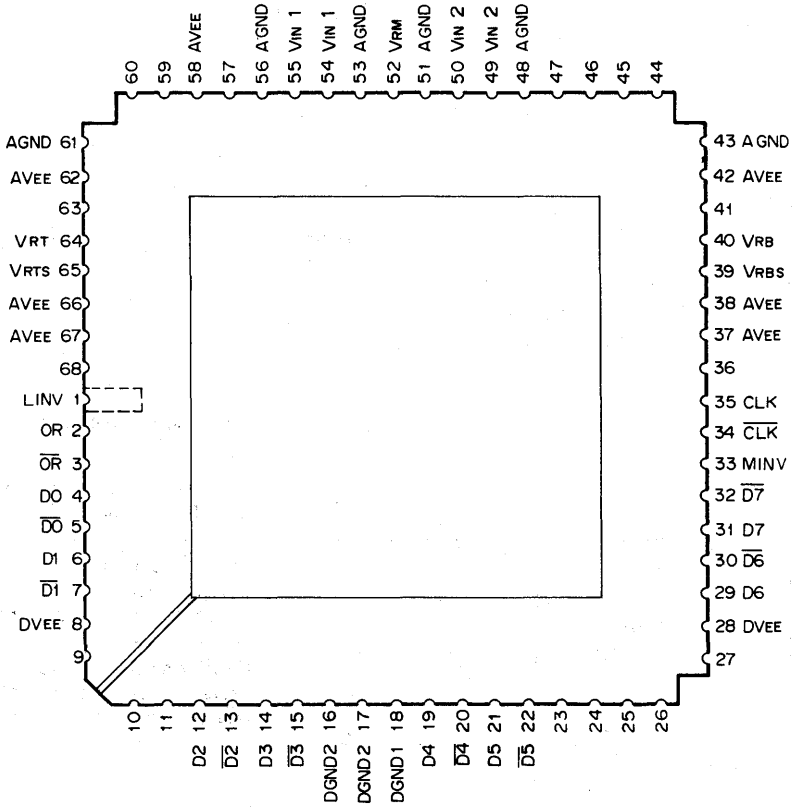
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	+0.5 to −7	V
• Analog input voltage	V_{IN}	+0.5 to V_{EE}	V
• Reference input voltage	V_{RT}, V_{RB}	+0.5 to V_{EE}	V
	V_{RT}-V_{RB}	0 to 2.5	V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	+0.5 to V_{EE}	V
• Digital output current	IDO to ID7, IOR	0 to −30	mA
	$\overline{IDO}$ to $\overline{ID7}$, $\overline{IOR}$	0 to −30	mA
• Operating temperature	T_a	−25 to +75	°C
	T_c	−55 to +125	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1.8	W

Recommended Operating Conditions

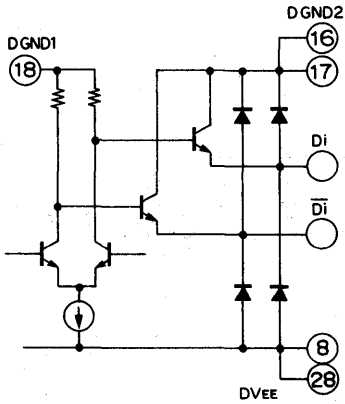
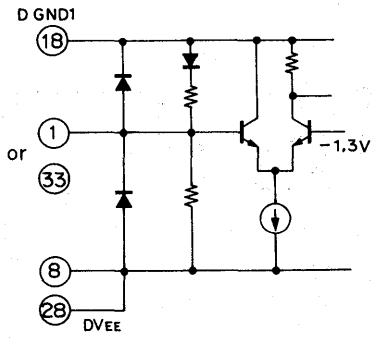
Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	AV_{EE}, DV_{EE}	−4.95	−5.2	−5.5	V
Supply votage	$\lvert AV_{EE} - DV_{EE} \rvert$		0	0.05	V
Ground	| DGND − AGND |		0	0.05	V
Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
Reference input voltage	V_{RT}	−0.1	0	+0.2	V
Reference input voltage	V_{RB}	−2.2	−2	−1.9	V
Digital input voltage	V_{IH}	−1.0		−0.7	V
Digital input voltage	V_{IL}	−1.9		−1.6	V
Clock pulse width	TPW1 (CXA1076AK)	3.5			ns
Clock pulse width	TPW0 (CXA1076AK)	1.5			ns
Clock pulse width	TPW1 (CXA1176AK)	2.5			ns
Clock pulse width	TPW0 (CXA1176AK)	0.8			ns

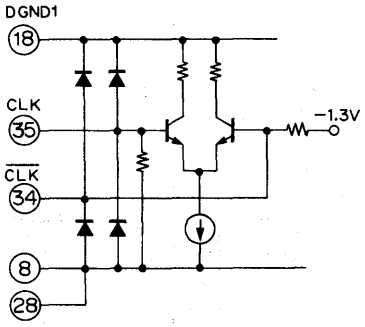
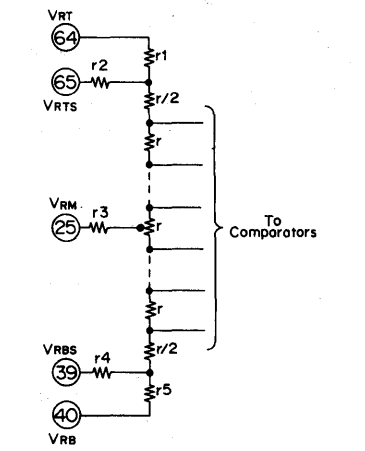
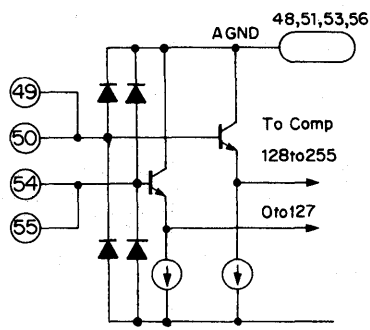
Pin Configulation (Top View)



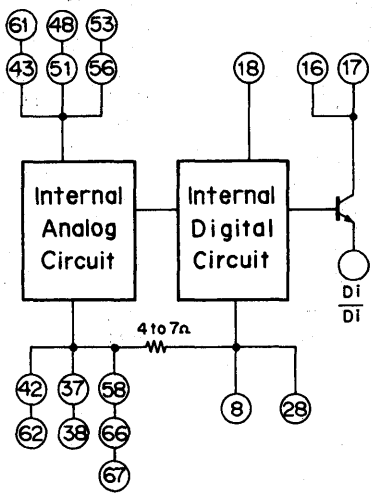
4

Pin Description and I/O Equivalent Circuits

No.	Symbol	Equivalent circuit	Description
4 5	D_0 $\overline{D_0}$		LSB and complementary LSB output
6 7	D_1 $\overline{D_1}$		D_1 to D_6: output $\overline{D_1}$ to $\overline{D_6}$: complementary output
12 13	D_2 $\overline{D_2}$		
14 15	D_3 $\overline{D_3}$		
19 20	D_4 $\overline{D_4}$		
21 22	D_5 $\overline{D_5}$		
29 30	D_6 $\overline{D_6}$		
31 32	D_7 $\overline{D_7}$		MSB and complementary MSB output
2 3	OR $\overline{OR}$		Over Range and complementary Over Range output
33	MINV		Polarity select for MSB (Refer to coding table) L level is maintained with left open.
1	LINV		Polarity select for LSBs (Refer to coding table) L level is maintained with left open.

No.	Symbol	Equivalent circuit	Description
35	CLK		CLK input
34	$\overline{CLK}$		Complementary CLK input V_{BB} (−1.3V) is maintained with left open. It can be used as a reference for single CLK input.
64	V_{RT}		Analog reference voltage (Top) (0V Typ.)
65	V_{RTS}		Reference voltage sense (Top)
52	V_{RM}		Reference voltage mid-point It can be used for linearity compensation.
39	V_{RBS}		Reference voltage sense (Bottom)
40	V_{RB}		Analog reference voltage (Bottom) (−2V Typ.)
49 50 54 55	V_{IN}		Analog input All of the pins must be wired externally.

4

No.	Symbol	Equivalent circuit	Description
43, 48, 51, 53, 56, 61	AGND (*1)		Analog ground
37, 38, 42, 58, 62, 66, 67	AVEE (*1)		Analog supply
18	DGND1		Digital ground
16 17	DGND2 (*1)		Digital ground for output drive
8 28	DVEE (*1)		Digital supply
9, 10 11, 23 24, 25 26, 27 36, 68	NC		No connect pins It is recommended to wire these pins to DGND.
41, 44 45, 46 47, 57 59, 60 63	NC		No connect pins It is recommended to wire these pins to AGND.

(*1) All of these pins must be wired to the respective external circuit.

Timing Chart

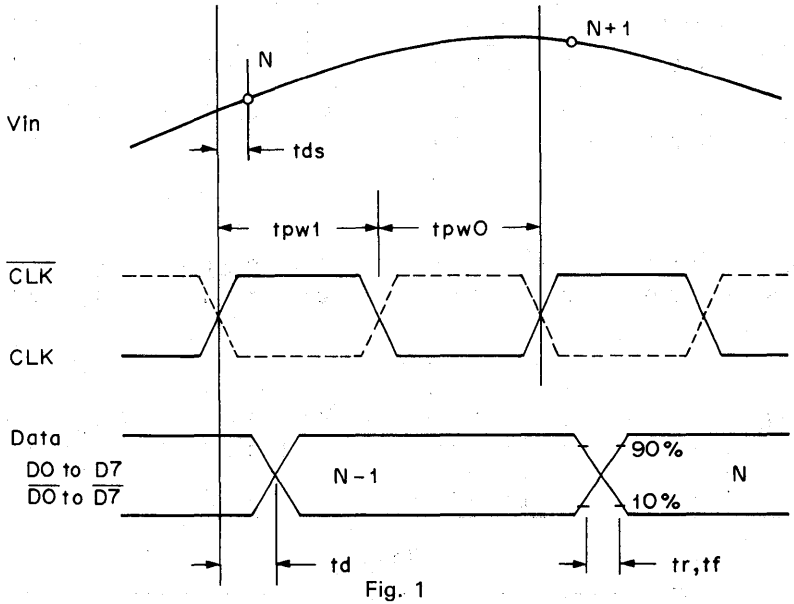


Fig. 1

4

Input-Output Reference and Output Format

Vin	Step	MINV 1 LINV 1 OR MSB LSB	0 1 OR MSB LSB	1 0 OR MSB LSB	0 0 OR MSB LSB
0V		0 0 0 0 · · · 0 0	0 1 0 0 · · · 0 0	0 0 1 1 · · · 1 1	0 1 1 1 · · · 1 1
	0	1 0 0 0 · · · 0 0	1 1 0 0 · · · 0 0	1 0 1 1 · · · 1 1	1 1 1 1 · · · 1 1
	1	1 0 0 0 · · · 0 1	1 1 0 0 · · · 0 1	1 0 1 1 · · · 1 0	1 1 1 1 · · · 1 0
		·	·	·	·
		·	·	·	·
		·	·	·	·
−1V	127	1 0 1 1 · · · 1 1	1 1 1 1 · · · 1 1	1 0 0 0 · · · 0 0	1 1 0 0 · · · 0 0
	128	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0	1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1
		·	·	·	·
		·	·	·	·
		·	·	·	·
	254	1 1 1 1 · · · 1 0	1 0 1 1 · · · 1 0	1 1 0 0 · · · 0 1	1 0 0 0 · · · 0 1
	255	1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0
−2V		1 1 1 1 · · · 1 1	1 0 1 1 · · · 1 1	1 1 0 0 · · · 0 0	1 0 0 0 · · · 0 0

Table 1

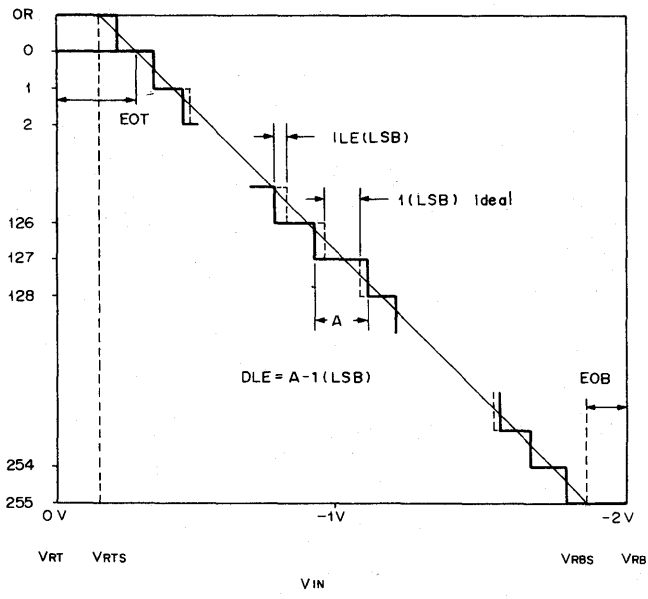


Fig. 2

Electrical Characteristics — CXA1076AK

T_a = 25°C, AV_{EE} = DV_{EE} = −5.2 V
V_{RT} = V_{RTS} = OV, V_{RB} = V_{RBS} = −2 V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate (1)		F_C	V_{IN} = FS, F_{IN} = 1 kHz	200	240		MSPS
Maximum conversion rate (2)		F_C	V_{IN} = FS F_{IN} = 49.999 MHz	200	240	—	MSPS
Resolution			F_C = 200 MSPS		8		bit
Integral linearity error		E_{IL}			±0.3	±0.5	LSB
Differential linearity error		E_{DL}			±0.3	±0.5	LSB
Offset error	V_{RT}	E_{OT}		12.0	14.5	17.0	mV
	V_{RB}	E_{OB}		4.0	6.5	9.0	mV
Analog input capacitance		C_{IN}	V_{IN} = −1 V +0.07 rms	21	25	35	pF
Analog input current		I_{IN}	V_{IN} = OV	70	150	700	μA
Supply current	Analog	I_{EEA}		150	200	260	mA
	Digital	I_{EED}		60	70	90	mA
Referrence resistance		R_{REF}	V_{RT} to V_{RB}	75	90	108	Ω
Residual resistance		r1, r5		0.43	0.52	0.62	Ω
		r2, r4		0.64	0.77	0.92	Ω
		r3		2.8	3.4	4.1	Ω
Input level digital	H	V_{IH}		−1.0	−0.85	−0.7	V
	L	V_{IL}		−1.9	−1.75	−1.6	V
Output level digital	H	V_{OH}	R_L = 50 Ω to −2 V FO = 1 (100 K ECL)	−1.05			V
	L	V_{OL}				−1.6	V
Output data delay		td		1.7	2.0	3.1	ns
Rise time output digital		tr		0.8	1.2	1.5	ns
Fall time output digital		tf		0.8	1.2	1.5	ns
Full scale input BW		BW_F	V_{IN} = FS (*1)	200	220		MHz
Small signal input BW		BW_S	V_{IN} = 0.6 Vp-p (*1)		250		MHz
Aperture jitter		taj			3.0	3.6	ps
Sampling delay		tds		0.6	0.8	1.1	ns
SNR1			F_{IN} = 1 MHz FS F_C = 200MSPS (*1)	45.5	46		dB
SNR2			F_{IN} = 80 MHz, 0.6 Vp-p F_C = 200MSPS (*1)		33		dB
Differential gain		DG	NTSC 40 IRE mod. ramp F_C = 200 MSPS			1.0	%
Differential phase		DP				0.5	deg.
Error rate		E_R	F_C = 200 MSPS F_{IN} = 49.999 MHz V_{IN} = 2 Vp-p tpw1 = 3.5 ns tpw0 = 1.5 ns Error Threshold: 32 LSB			10^{-8}	times/ sample

(*1) Source impedance = 50 Ω.

4

Electrical Characteristics — CXA1176AK

T_a = 25°C, AV_{EE} = DV_{EE} = −5.2 V
V_{RT} = V_{RTS} = OV, V_{RB} = V_{RBS} = −2 V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum conversion rate (1)		Fc	V_{IN} = FS, F_{IN} = 1 kHz	300	340		MSPS
Maximum conversion rate (2)		Fc	V_{IN} = FS F_{IN} = 62.499 MHz	250	290		MSPS
Resolution			Fc = 300 MSPS		8		bit
Integral linearity error		EIL			±0.3	±0.5	LSB
Differential linearity error		EDL			±0.3	±0.5	LSB
Offset error	V_{RT}	EOT		12.0	14.5	17.0	mV
	V_{RB}	EOB		4.0	6.5	9.0	mV
Analog input capacitance		CIN	V_{IN} = −1 V +0.07 rms	21	25	35	pF
Analog input current		IIN	V_{IN} = OV	70	150	700	μA
Supply current	Analog	IEEA		150	200	260	mA
	Digital	IEED		60	70	90	mA
Referrence resistance		RREF	V_{RT} to V_{RB}	75	90	108	Ω
Residual resistance		r1, r5		0.43	0.52	0.62	Ω
		r2, r4		0.64	0.77	0.92	Ω
		r3		2.8	3.4	4.1	Ω
Input level digital	H	VIH		−1.0	−0.85	−0.7	V
	L	VIL		−1.9	−1.75	−1.6	V
Output level digital	H	VOH	RL = 50 Ω to −2 V FO = 1 (100 K ECL)	−1.05			V
	L	VOL				−1.6	V
Output data delay		td		1.7	2.0	3.1	ns
Rise time output digital		tr		0.8	1.2	1.5	ns
Fall time output digital		tf		0.8	1.2	1.5	ns
Full scale input BW		BWF	V_{IN} = FS (*2)	230	250		MHz
Small signal input BW		BWS	V_{IN} = 0.6 Vp-p (*2)		280		MHz
Aperture jitter		taj			3.0	3.6	ps
Sampling delay		tds		0.6	0.8	1.1	ns
SNR1			F_{IN} = 1 MHz FS Fc = 300MSPS (*2)	45.5	46		dB
SNR2			F_{IN} = 80 MHz, 0.6 Vp-p Fc = 250MSPS (*2)		35		dB
Differential gain		DG	NTSC 40 IRE mod. ramp Fc = 300 MSPS			1.0	%
Differential phase		DP				0.5	deg.
Error rate		ER	Fc = 250 MSPS F_{IN} = 62.499 MHz V_{IN} = 2 Vp-p tpw1 = 3.0 ns tpw0 = 1.0 ns Error Threshold: 32 LSB			10^{-8}	times/ sample

(*2) Source impedance = 50 Ω.

Application Circuit

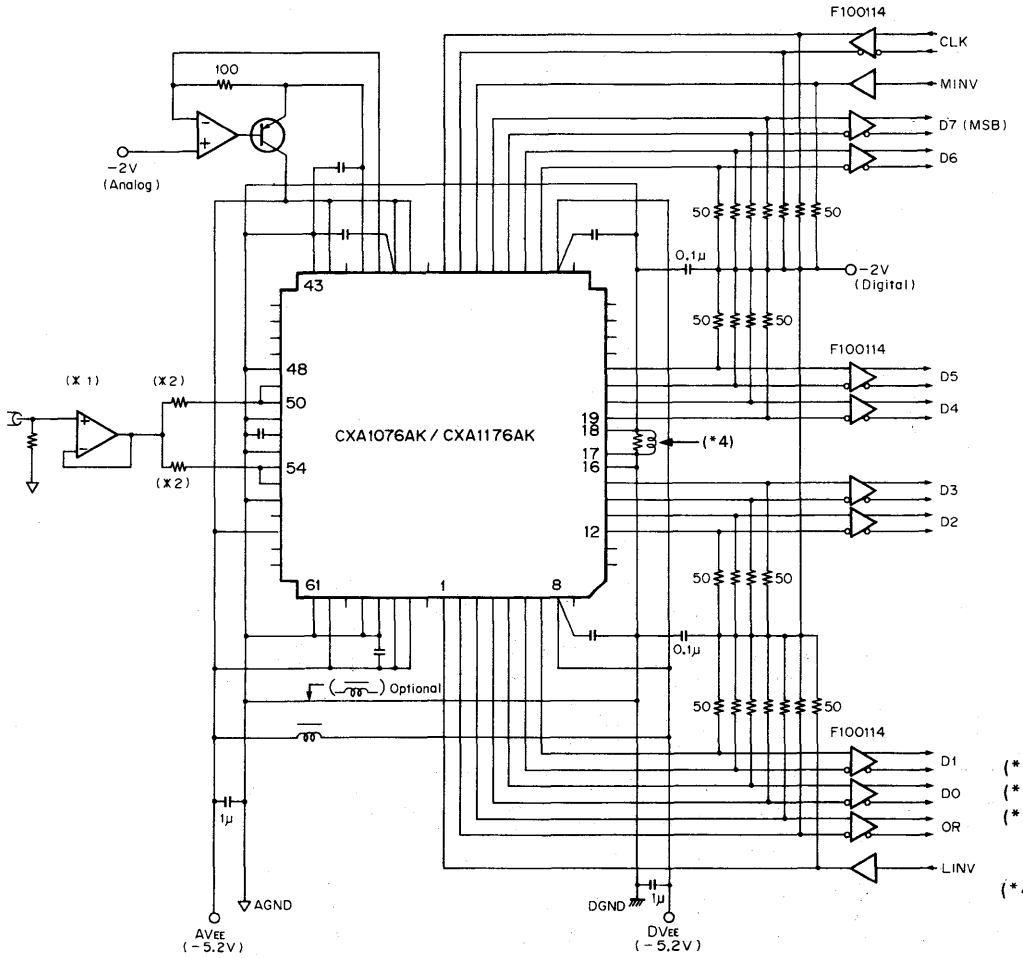


Fig. 3

(*1) Comlinear CLC231 or equiv.
(*2) To be selected (2 to 20Ω)
(*3) Capacitors are 0.01μF ceramic chip not otherwise specified.
(*4) R: 1 Ω with very low inductance
L: 0.22 μH
This is optional for preventing oscillation

Notes on Application

1) AGND, DGND, AV_{EE} and DV_{EE} planes on a PCB should be designed to make those impedance small for the noise suppression benefits. Those planes should be made as wide as possible on the PCB with at least double layer metal patterns.

2) It is recommended to separate the analog and digital V_{EE} on the PCB patterns to make reduce a noise contamination from digital system to analog system.

3) If separate V_{EE} and GND are used, it is recommended to connect the digital and analog planes by a core inductor with good frequency characteristics to avoid the DC voltage difference between analog and digital planes.
The DC voltage difference between AGND and DGND degrades performance and continual voltage difference between AV_{EE} and DV_{EE} may cause destruction of the device.

4) The analog and digital power supply pins should be bypassed as close to the device as possible to their respective grounds with at least a 10 nF ceramic chip chip capacitor. A 1 μF tantalum capacitor can also be used for low frequency bypassing.

5) Pin connections for the device should be made as short as possible. Using of a socket might degrade the performance because of increasing lead inductance. A possible compromise is to use AMP's socket 173257-3 (with heat sink).

6) A wide band drive amplifier with sufficient drivability and stable operation should be used to drive analog input pin. Comlinear's CLC231 may be used with adiquate frequency compensation.

7) As the analog input impedance of the device is capacitive, the driving amplifier occationally falls into unstable condition and oscillates locally. This instability can be prevented with a resistor inserted in series between the output pin of the amplifier and V_{IN} pins of the device. The resistor is to be selected from 2 to 20 Ω. Separate input for V_{IN} as shown in an application circuit (Fig. 3) may give a good result.

8) Digital output is delivered in complementary to make ease to interface in high speed operation. A 50 Ω termination at the endpoint of the wiring for both Di and $\overline{Di}$ is recommended for noise suppression benefits.

9) V_{RTS} and V_{RBS} pins can be used as a sense for precise adjustment of reference voltage. Fig. 4 shows the adjustment scheme.

10) Internal current compensation circuit for the reference resistor is furnished in the device. This circuit compensates input bias current of the comparators to maintain the linearity over wide temperature range.
V_{RM}, the mid-point of the reference resistor can be used as a trimming pin for more accurate linearity as shown in Fig. 4.
V_{RT}, V_{RB} and V_{RM} should be bypassed to AGND with at least a 100 nF ceramic chip capacitor.

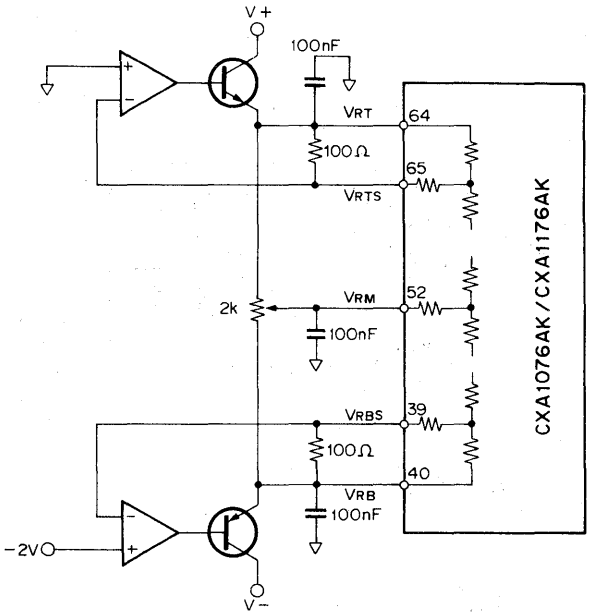


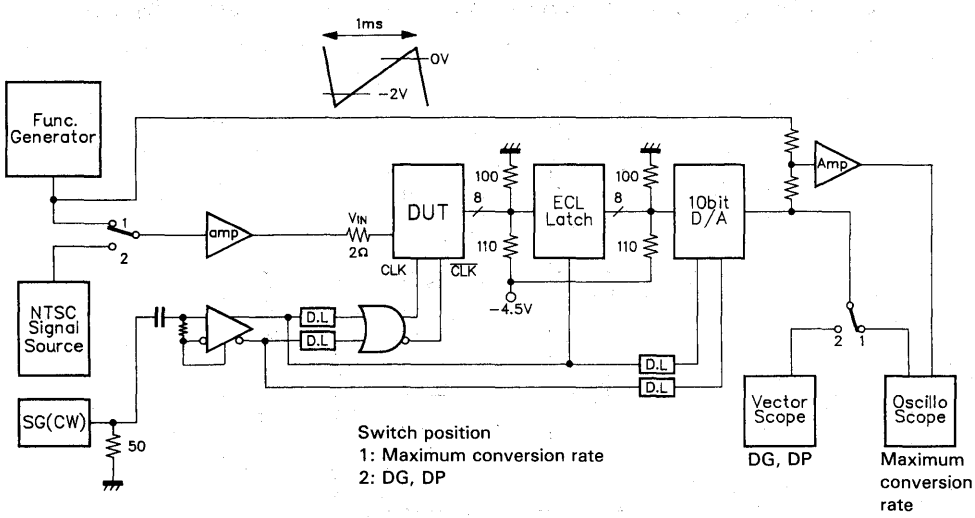
Fig. 4

11) OR and $\overline{OR}$ output indicate that the input signal exceeds positive input range. MINV and LINV are not effective to the polarity of OR and $\overline{OR}$ (Refer to the output format).

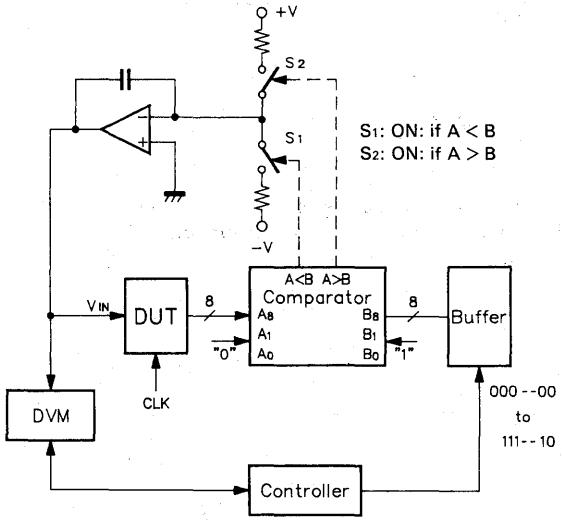
4

Electrical Characteristics Test Circuit

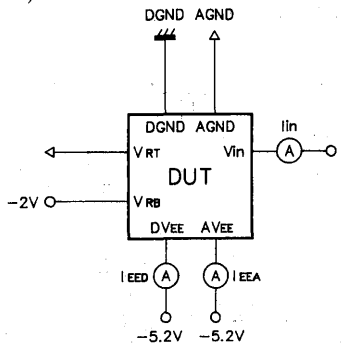
Maximum conversion rate
Differential gain error
Differential phase error
Test circuit



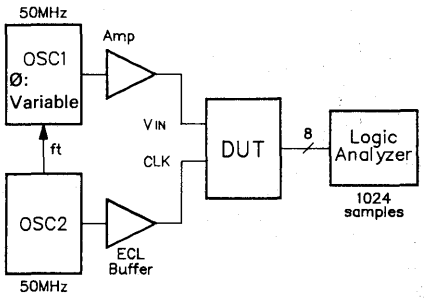
Integral linearity error
Differential linearity error
Test circuit



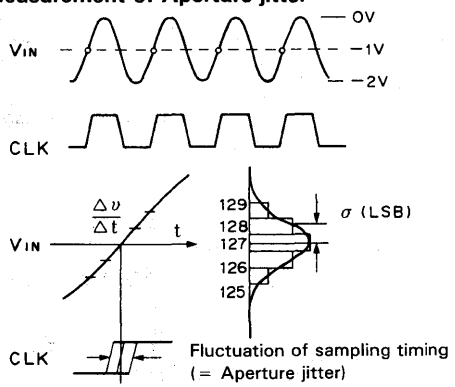
Supply current
Analog input bias current } **Test circuit**



Sampling delay
Aperture jitter } **Test circuit**



Measurement of Aperture jitter

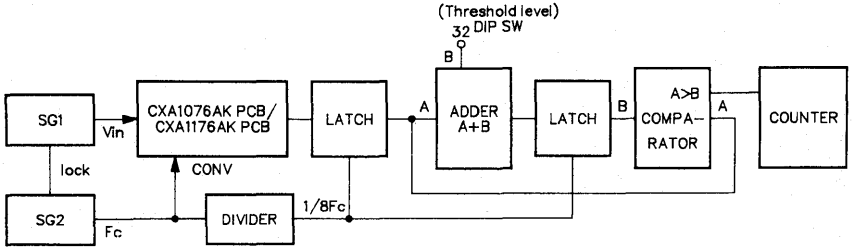


Aperture jitter is defined as follows:

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right),$$

where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

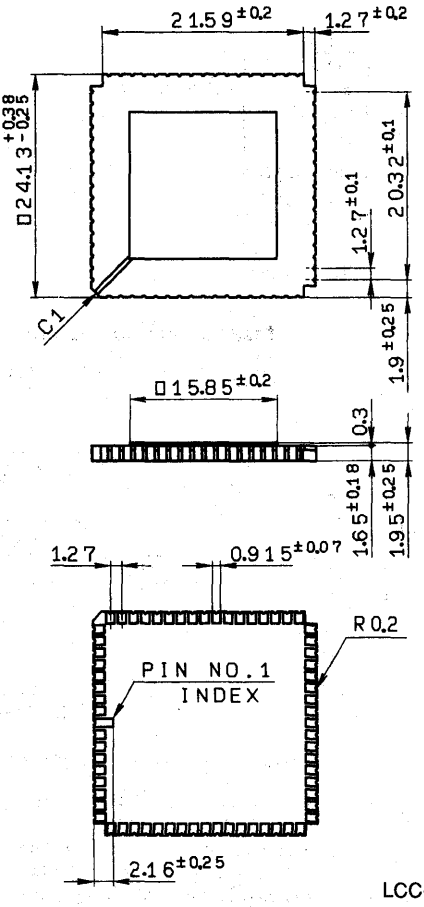
Error rate Test circuit



4

Package Outline Unit: mm

68pin LCC (Ceramic) 3.7g



LCC-68C-01

SONY

CXA1166K

8-bit 250 MSPS Flash A/D Converter

Preliminary

Description

The CXA1166K is an 8-bit ultrahigh-speed flash A/D converter IC capable of digitizing analog signals at a maximum rate of 250 MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

The CXA1166K is pin-compatible with the earlier model CXA1076K/CXA1076AK/CXA1176K/CXA1176AK. They can replace the earlier models without any design changes, in most cases. Compared with the earlier models, these new models have been greatly improved in performance, by using new circuit design and carefully considered layout.

68 pin LCC (Ceramic)

Features

- Differential linearity error: ± 1/2 LSB or less
- Integral linearity error: ± 1/2 LSB or less
- Built-in integral linearity compensation circuit
- Ultrahigh-speed operation with maximum conversion rate of 250 MSPS (Min.)
- Low input capacitance: 15pF (Typ.)
- Wide analog input bandwidth: 250MHz (Typ. for full-scale input)
- Single power supply: –5.2V
- Low power consumption: 1400mW (Typ.)
- Low error rate
- Good temperature characteristics
- Capable of driving 50 Ω loads

Structure

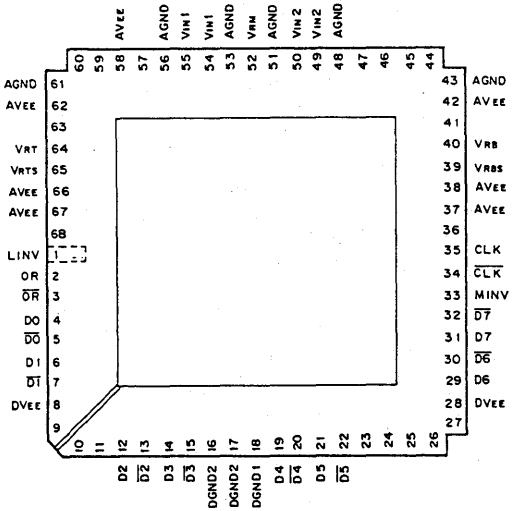
Bipolar silicon monolithic IC

Applications

- Digital oscilloscopes
- Radar
- Other apparatus requiring ultrahigh-speed A/D conversion

Pin Configuration

Pins without name are NC pins (not connected internally).



PE90406 – ST

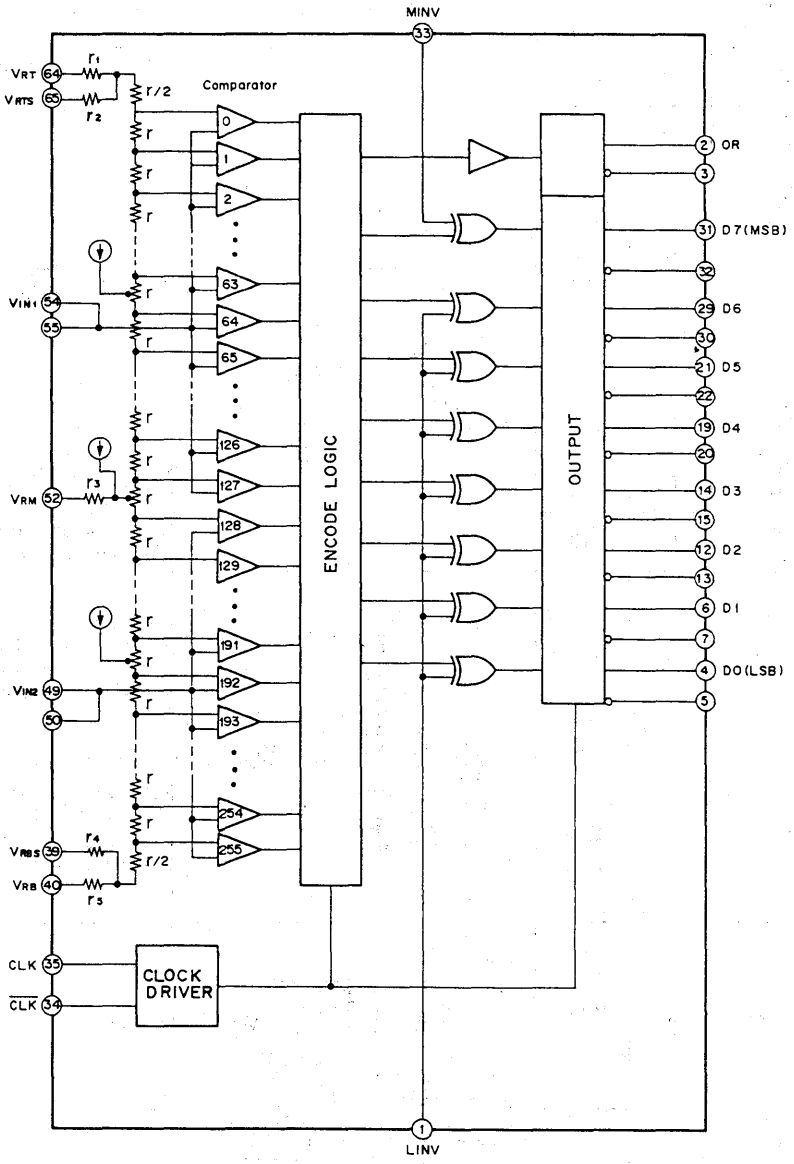
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5	V
• Analog input voltage	V_{IN}	AV_{EE} to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	AV_{EE} to +0.5	V
	$\lvert V_{RT}-V_{RB}\rvert$	2.5	V
• Digital input voltage	MINV, LINV	−4 to +0.5	V
	CLK, $\overline{CLK}$	DV_{EE} to +0.5	V
	$\lvert CLK-\overline{CLK}\rvert$	2.7	V
• V_{RM} pin input current	I_{VRM}	−3 to +3	mA
• Digital output current	ID_0 to ID_7, IOR, $\overline{ID_0}$ to $\overline{ID_7}$, $\overline{IOR}$	−30 to 0	mA
• Operating temperature	Ta	−25 to +100	°C
	Tc	−25 to +125	°C
• Storage temperature	Tstg	−65 to +150	°C

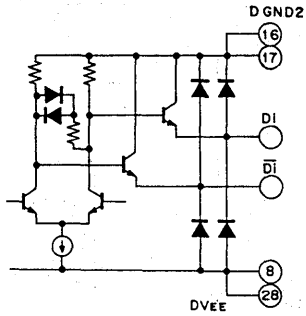
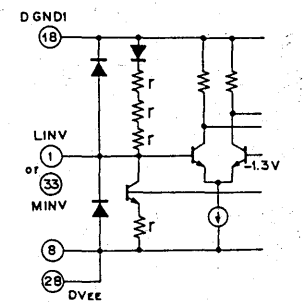
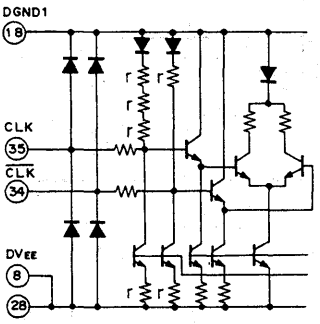
Operating Conditions

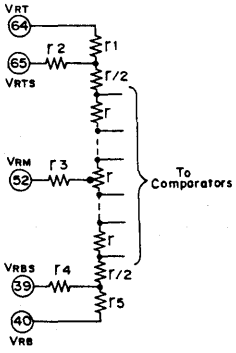
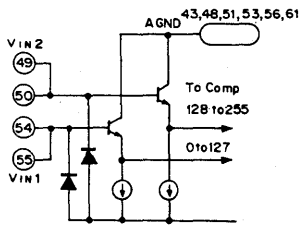
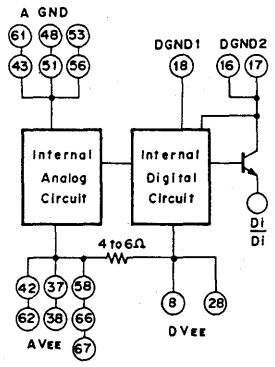
		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.5	−5.2	−4.95	V
	$AV_{EE}-DV_{EE}$	−0.05	0	0.05	V
	AGND–DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2.0	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
4 5	$\overline{D_0}$ D_0	O	ECL		LSB and complementary LSB output
6 7	$\overline{D_1}$ D_1	O	ECL		D_1 to D_6: Output $\overline{D_1}$ to $\overline{D_6}$: Complementary output
12 13	$\overline{D_2}$ D_2	O	ECL		
14 15	$\overline{D_3}$ D_3	O	ECL		
19 20	$\overline{D_4}$ D_4	O	ECL		
21 22	$\overline{D_5}$ D_5	O	ECL		
29 30	$\overline{D_6}$ D_6	O	ECL		
31 32	$\overline{D_7}$ D_7	O	ECL		MSB and complementary MSB output
2 3	$\overline{OR}$ OR	O	ECL		Overrange and complementary Overrange output
33	MINV	I	ECL		Polarity selection for MSB (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
1	LINV	I	ECL		Polarity selection for LSBs. (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
35	CLK	I	ECL		CLK input
34	$\overline{CLK}$	I	ECL		Complementary CLK input V_{BB} (–1.3V) is maintained with left open.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
64	V_{RT}	I	0V		Analog reference voltage (Top) (0V Typ.)
65	V_{RTS}	O	0V		Reference voltage sense (Top)
52	V_{RM}	I	$V_{RB}/2$		Reference voltage mid-point It can be used for linearity compensation.
39	V_{RBS}	O	–2V		Reference voltage sense (Bottom)
40	V_{RB}	I	–2V		Analog reference voltage (Bottom)
49 50	V_{IN2}	I	V_{RTS} to V_{RBS}		Analog input All of the pins must be wired externally.
54 55	V_{IN1}				
43. 48, 51, 53, 56, 61	AGND *		0V		Analog ground
37, 38, 42, 58, 62, 66, 67	AVEE *		–5.2V		Analog supply Internally connected with DVEE (resistance : 4 to 6 Ω).
18	DGND1		0V		Digital ground
16 17	DGND2*		0V		Digital ground for output drive
8 28	DVEE *		–5.2V		Digital supply Internally connected with AVEE (resistance : 4 to 6 Ω).

* All of these pins must be wired to the respective external circiut.

4

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
9, 10, 11, 23, 24, 25, 26, 27, 36, 68	NC		—		No connect pins It is recommended to wire these pins to DGND.
41, 44, 45, 46, 47, 57, 59, 60, 63	NC		—		No connect pins It is recommended to wire these pins to AGND.

Electrical Characteristics

(AV_{EE}=DV_{EE}=–5.2V, V_{RT}, V_{RTS}=0V, V_{RB}, V_{RBS}=–2V)

Item	Symbol	Condition	Test level *1	Min.	Typ.	Max.	Unit
Resolution					8		bits
DC characteristics							
Integral linearity error	E_{IL}	Fc=250MHz	II		± 0.3	± 0.5	LSB
Differential linearity error	E_{DL}	Fc=250MHz	II		± 0.3	± 0.5	LSB
Analog input							
Analog input capacitance	C_{IN}	V_{IN}=–1V+0.07Vrms	IV		15		pF
Analog input resistance	R_{IN}		IV		100		kΩ
Input bias current	I_{IN}	V_{IN}=–1V	IV		240		μA
Reference inputs							
Reference resistance	R_{REF}		II		110		Ω
Frequency characteristic of reference resistance	F_{REF}		IV		10		MHz
Residual resistance *2 r1	r1		IV		0.6		Ω
r2	r2		IV		500		Ω
r3	r3		IV		2.0		Ω
r4	r4		IV		500		Ω
r5	r5		IV		0.6		Ω
Digital inputs							
Logic H level	V_{IH}		IV	–1.165			V
Logic L level	V_{IL}		IV			–1.475	V
Logic H current	I_{IH}	Input connected to GND	IV			100	μA
Logic L current	I_{IL}	Input connected to –2V	IV	–100			μA
Input capacitance			IV		7		pF
Switching characteristics							
Maximum conversion rate	Fc		II	250			MSPS
Aperture jitter	Taj		IV		5		ps
Sampling delay	Tds		IV		1.0		ns
Output delay	Tdo		IV		2.0		ns
H pulse width of clock	T_{PW1}		IV	2.0			ns
L pulse width of clock	T_{PW0}		IV	2.0			ns
Digital outputs							
Logic H level	V_{OH}	R_L=50 Ω	II	–1.025			V
Logic L level	V_{OL}	R_L=50 Ω	II			–1.620	V
Output rising time	Tr	R_L=50 Ω	IV		1.0		ns
Output falling time	Tf	R_L=50 Ω	IV		1.0		ns

4

Item	Symbol	Condition	Test level *1	Min.	Typ.	Max.	Unit
Dynamic characteristics							
Full scale input bandwidth		V_{IN}=2Vp-p	IV		250		MHz
Small-signal input bandwidth		V_{IN}=0.6Vp-p	IV		400		MHz
S/N ratio		Input=1kHz, FS, Clock=250MHz	IV		46		dB
		Input=62.499MHz, FS, Clock=250MHz	IV		40		dB
Error rate		Input=1kHz, FS, Error>16LSB, Clock=250MHz	IV			10^{-12}	TPS *3
		Input=62.499MHz, FS, Error>16LSB, Clock=250MHz	II			10^{-9}	TPS *3
Differential gain error	DG	NTSC 40IRE mod. ramp, Fc=250MSPS	IV			1.0	%
Differential phase error	DP		IV			0.5	deg
Overrange recovery time			IV		1.0		ns
Power supply							
Analog supply current	I_{EEA}		II		210		mA
Digital supply current	I_{EED}		II		50		mA
Power consumption *4	Pd		II		1400		mW

*1 Test levels

I····· All-quantity test over full operating temperature range (Tc=–25 to +125 ℃)

II····· All-quantity test at Tc=+25 ℃

III····· Sampling test only

IV····· Design specifications

V····· Typical values only

*2 See Block Diagram

*3 TPS: times per sample

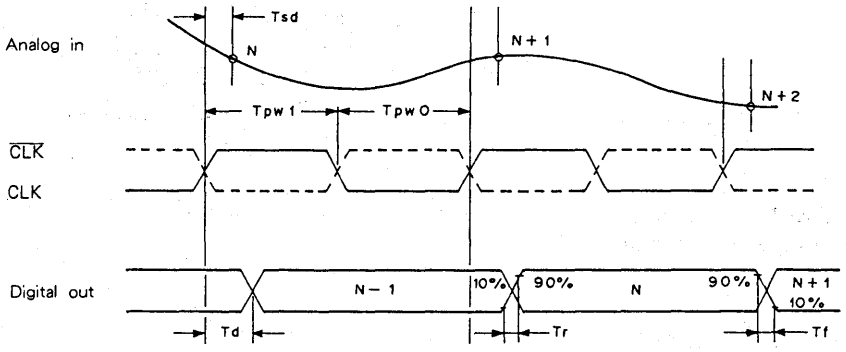
*4 $Pd=I_{EEA} \cdot AV_{EE}+I_{EED} \cdot DV_{EE}+\dfrac{(V_{RT}-V_{RB})^2}{R_{REF}}$

Input Voltage vs. Digital Output

V_{IN} *	Step	MINV 1 LINV 1			0 1			1 0			0 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000·····00		0	100·····00		0	011·····11		0	111·····11	
	0	1	000·····00		1	100·····00		1	011·····11		1	111·····11	
	1	1	000·····01		1	100·····01		1	011·····10		1	111·····10	
			⋮			⋮			⋮			⋮	
−1V	127	1	011·····11		1	111·····11		1	000·····00		1	100·····00	
	128	1	100·····00		1	000·····00		1	111·····11		1	011·····11	
			⋮			⋮			⋮			⋮	
	254	1	111·····10		1	011·····10		1	100·····01		1	000·····01	
	255	1	111·····11		1	011·····11		1	100·····00		1	000·····00	
−2V		1	111·····11		1	011·····11		1	100·····00		1	000·····00	

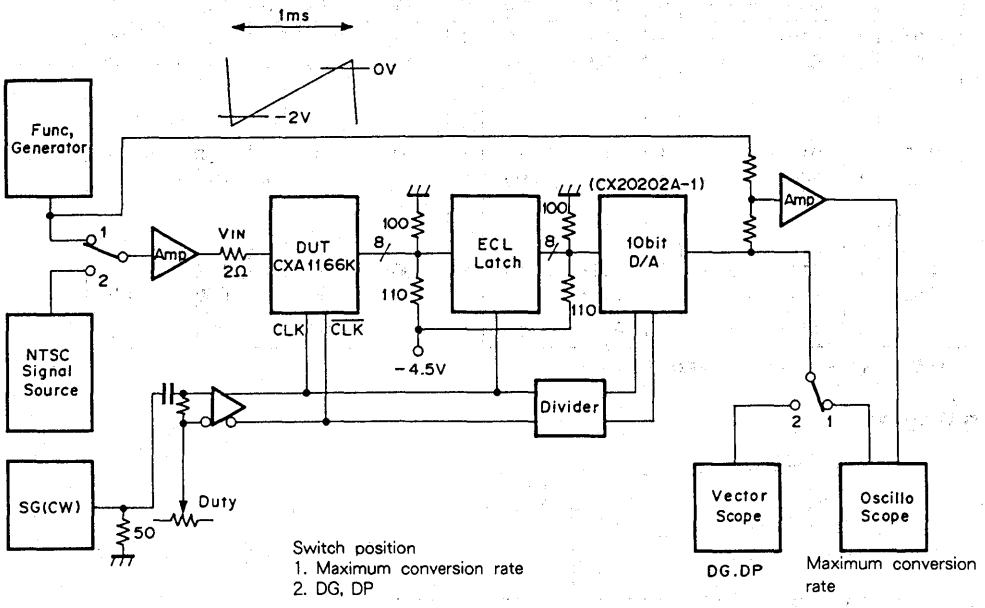
* V_{RT}=V_{RTS}=0V, V_{RM}=−1V or Open, V_{RB}=V_{RBS}=−2V

Timing Diagram

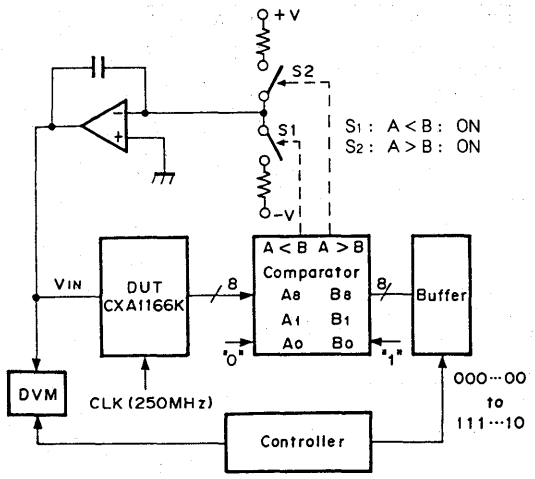


Electrical Characteristics Test Circuit

Maximum conversion rate test circuit
Differential gain error test circuit
Differential phase error test circuit

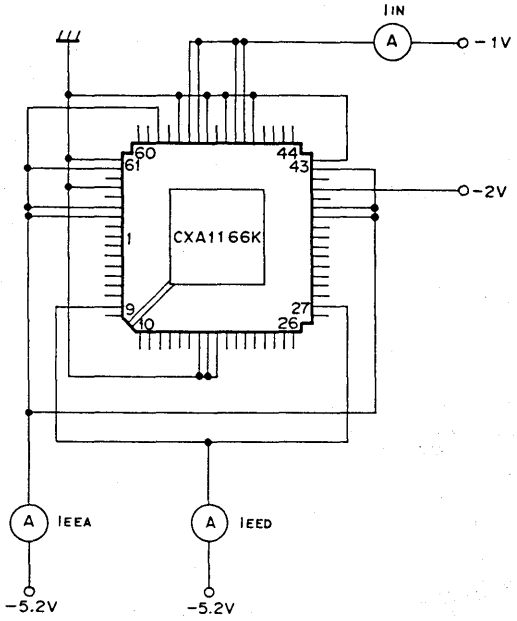


Integral linearity error test circuit
Differential linearity error test circuit

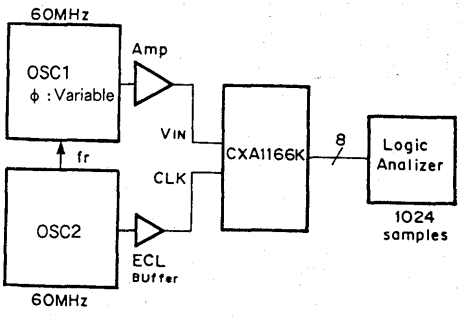


Power Supply Current Test Circuit

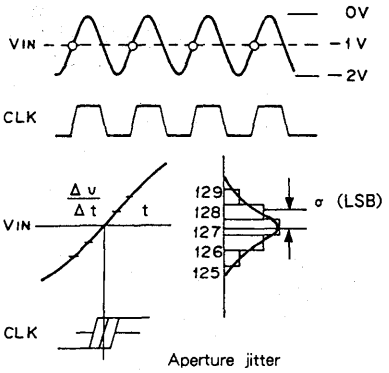
Analog input bias current test circuit



Sampling delay test circuit
Aperture jitter test circuit



Aperture jitter test method



Aperture jitter

Aperture jitter is defined as follows :

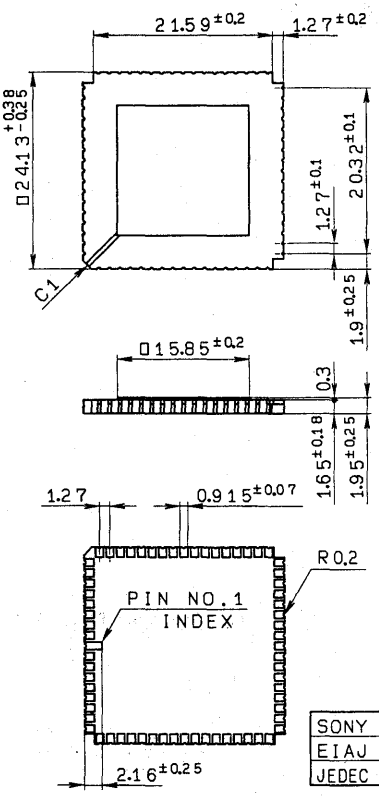
$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right),$$

Where σ (unit : LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

4

Package Outline Unit : mm

68pin LCC (Ceramic) 3.7g



SONY NAME	LCC-68C-01
EIAJ NAME	*QFN068-C-S950-A
JEDEC CODE	———

SONY

CXA1276K

8-bit 500 MSPS Flash A/D Converter

Preliminary

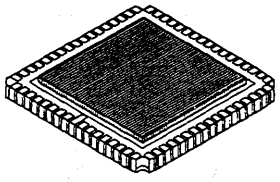
Description

The CXA1276K is a 8-bit ultrahigh-speed flash A/D converter IC capable of Digitizing analog signals at a maximum rate of 500 MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

Features

- Differential linearity error: ± 1/2 LSB or less
- Integral linearity error: ± 1/2 LSB or less
- Built-in integral linearity compensation circuit
- Ultrahigh-speed operation with maximum conversion rate of 500 MSPS (Min.)
- Low input capacitance: 16pF (Typ.)
- Wide analog input bandwidth: 250MHz (Typ. for full-scale input)
- Single power supply: –5.2V
- Low power consumption: 2.2W (Typ.)
- Low error rate
- Good temperature characteristics
- Capable of driving 50 Ω loads

68 pin LCC (Ceramic)



Structure

Bipolar silicon monolithic IC

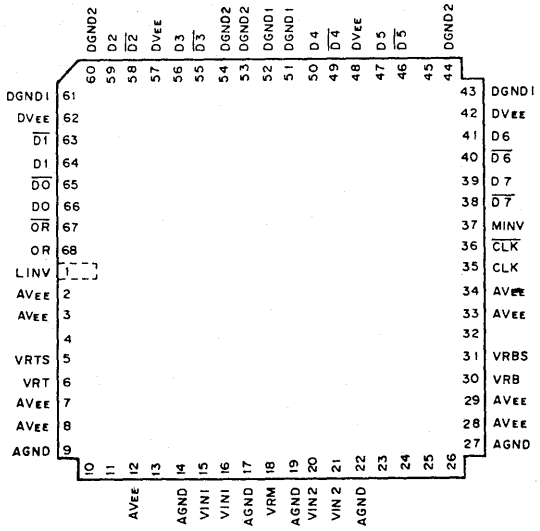
Applications

- Digital oscilloscopes
- Radar
- Other apparatus requiring ultrahigh-speed A/D conversion

4

Pin Configuration

Pins without name are NC pins (not connected internally).



PE90618 – ST

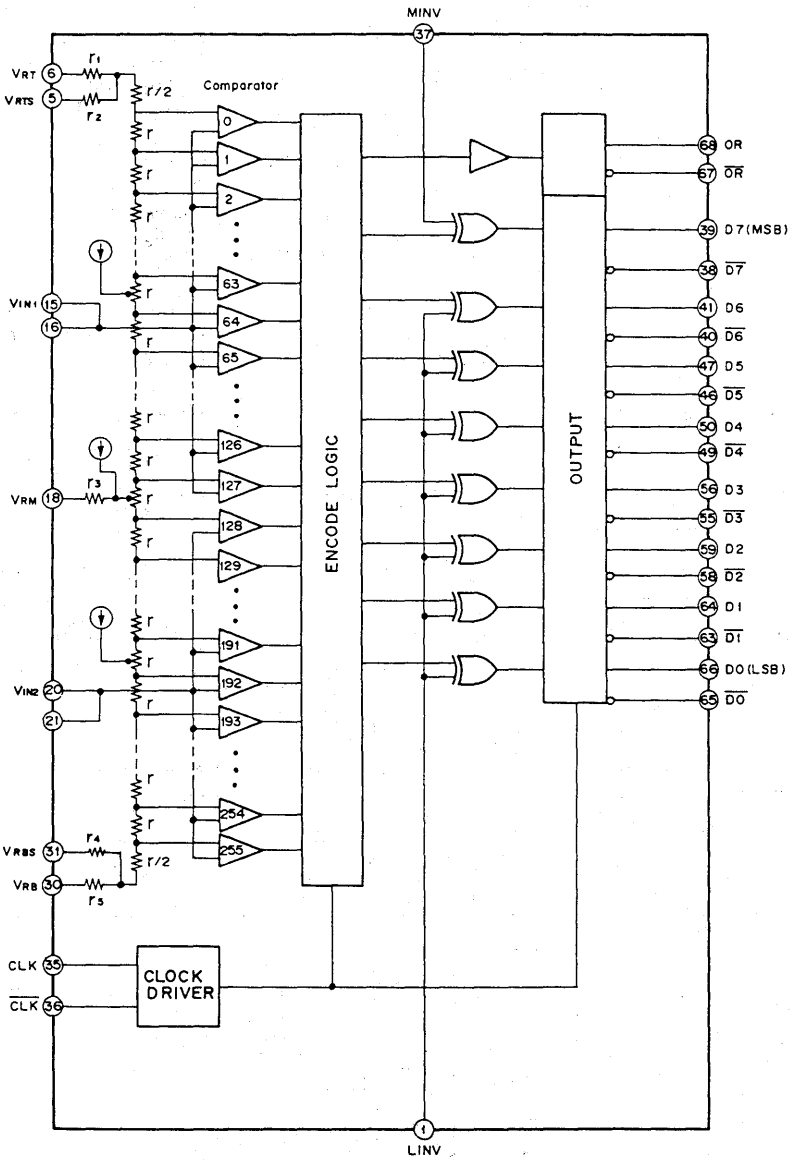
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5	V
• Analog input voltage	V_{IN}	−2.7 to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	AV_{EE} to +0.5	V
	$\lvert V_{RT}-V_{RB}\rvert$	2.5	V
• Digital input voltage	MINV, LINV	−4 to +0.5	V
	CLK, $\overline{CLK}$	DV_{EE} to +0.5	V
	$\lvert CLK-\overline{CLK}\rvert$	2.7	V
• V_{RM} pin input current	I_{VRM}	−3 to +3	mA
• Digital output current	ID_0 to ID_7, IOR, $\overline{ID_0}$ to $\overline{ID_7}$, $\overline{IOR}$	−30 to 0	mA
• Operating temperature	Ta	−25 to +100	°C
	Tc	−25 to +125	°C
• Storage temperature	Tstg	−65 to +150	°C

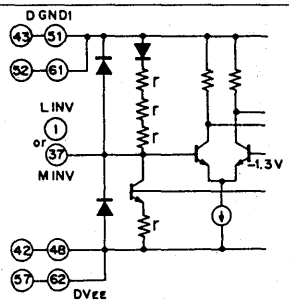
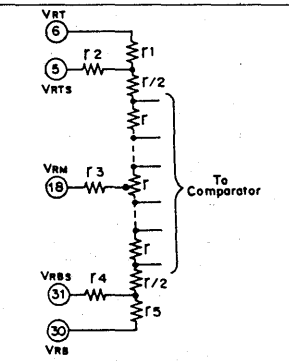
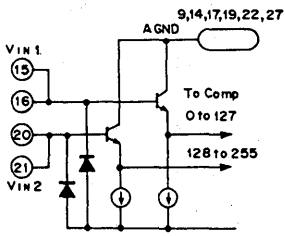
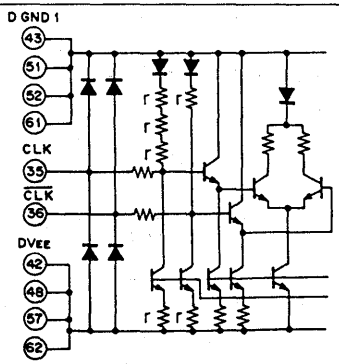
Operating Conditions

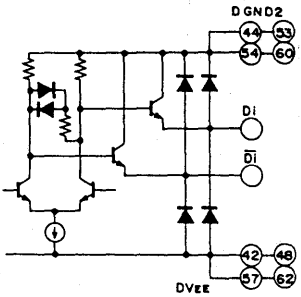
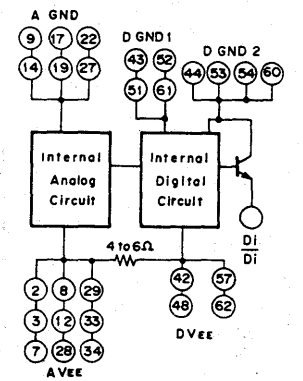
		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.5	−5.2	−4.95	V
	$AV_{EE}-DV_{EE}$	−0.05	0	0.05	V
	AGND–DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2.0	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	LINV	I	ECL		Polarity selection for LSBs. (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
37	MINV	I	ECL		Polarity selection for MSB (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
6	V_{RT}	I	0V		Analog reference voltage (Top) (0V Typ.)
5	V_{RTS}	O	0V		Reference voltage sense (Top)
18	V_{RM}	I	$V_{RB}/2$		Reference voltage mid-point It can be used for linearity compensation.
31	V_{RBS}	O	–2V		Reference voltage sense (Bottom)
30	V_{RB}	I	–2V		Analog reference voltage (Bottom)
15 16	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog input All of the pins must be wired externally.
20 21	V_{IN2}				
35	CLK	I	ECL		CLK input
36	$\overline{CLK}$	I	ECL		Complementary CLK input V_{BB} (–1.3V) is maintained with left open.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
39 38	$\frac{D_7}{D_7}$	O	ECL		MSB and complementary MSB output
41 40	$\frac{D_6}{D_6}$	O	ECL		D_1 to D_6: Output $\overline{D_1}$ to $\overline{D_6}$: Complementary output
47 46	$\frac{D_5}{D_5}$	O	ECL		
50 49	$\frac{D_4}{D_4}$	O	ECL		
56 55	$\frac{D_3}{D_3}$	O	ECL		
59 58	$\frac{D_2}{D_2}$	O	ECL		
64 63	$\frac{D_1}{D_1}$	O	ECL		
66 65	$\frac{D_0}{D_0}$	O	ECL		LSB and complementary LSB output
68 67	$\frac{OR}{OR}$	O	ECL		Overrange and complementary Overrange output
2, 3, 7, 8, 12, 28, 29, 33, 34	AVEE *		−5.2V		Analog supply Internally connected with DVEE (resistance : 4 to 6 Ω).
9, 14, 17, 19, 22, 27	AGND *		0V		Analog ground
42, 48, 57, 62	DVEE *		−5.2V		Digital supply Internally connected with AVEE (resistance : 4 to 6 Ω).
43, 51, 52, 61	DGND1 *		0V		Digital ground
44, 53, 54, 60	DGND2 *		0V		Digital ground for output drive
4, 10, 11, 13, 23, 24, 25, 26, 32	NC		—		No connect pins It is recommended to wire these pins to AGND.
45	NC		—		No connect pins It is recommended to wire these pins to DGND.

* All of these pins must be wired to the respective external circiut.

4

Electrical Characteristics

(AV_{EE}=DV_{EE}=–5.2V, V_{RT}, V_{RTS}=0V, V_{RB}, V_{RBS}=–2V)

Item	Symbol	Condition	Test level *1	Min.	Typ.	Max.	Unit
Resolution					8		bits
DC characteristics							
Integral linearity error	E_{IL}	Fc=500MHz	II		± 0.3	± 0.5	LSB
Differential linearity error	E_{DL}	Fc=500MHz	II		± 0.3	± 0.5	LSB
Analog input							
Analog input capacitance	C_{IN}	V_{IN}=–1V+0.07Vrms	IV		16		pF
Analog input resistance	R_{IN}		IV		100		kΩ
Input bias current	I_{IN}	V_{IN}=–1V	IV			620	µA
Reference inputs							
Reference resistance	R_{REF}		II		110		Ω
Frequency characteristic of reference resistance	F_{REF}		IV		10		MHz
Residual resistance *2 r1	r1		IV		0.6		Ω
r2	r2		IV		500		Ω
r3	r3		IV		2.0		Ω
r4	r4		IV		500		Ω
r5	r5		IV		0.6		Ω
Digital inputs							
Logic H level	V_{IH}		IV	–1.165			V
Logic L level	V_{IL}		IV			–1.475	V
Logic H current	I_{IH}	Input connected to GND	IV			100	µA
Logic L current	I_{IL}	Input connected to –2V	IV	–100			µA
Input capacitance			IV		7		pF
Switching characteristics							
Maximum conversion rate	Fc		II	400			MSPS
Aperture jitter	Taj		IV		5		ps
Sampling delay	Tds		IV		1.0		ns
Output delay	Tdo		IV		2.0		ns
H pulse width of clock	T_{PW1}		IV	1.2			ns
L pulse width of clock	T_{PW0}		IV	1.2			ns
Digital outputs							
Logic H level	V_{OH}	R_L=50 Ω	II	–1.025			V
Logic L level	V_{OL}	R_L=50 Ω	II			–1.620	V
Output rising time	Tr	R_L=50 Ω	IV		1.0		ns
Output falling time	Tf	R_L=50 Ω	IV		1.0		ns

Item	Symbol	Condition	Test level *1	Min.	Typ.	Max.	Unit
Dynamic characteristics							
Full scale input bandwidth		V_{IN}=2Vp-p	IV		300		MHz
Small-signal input bandwidth		V_{IN}=0.6Vp-p	IV		500		MHz
S/N ratio							
		Input=1kHz, FS Clock=500MHz	IV		46		dB
		Input=99.999MHz, FS Clock=500MHz	IV		40		dB
Error rate		Input=1kHz, FS Error>16LSB Clock=99.999MHz	IV			10^{-12}	TPS *3
		Input=62.499MHz, FS Error>16LSB Clock=500MHz	II			10^{-9}	TPS *3
Differential gain error	DG	NTSC 40 IRE mod. ramp, Fc=500MSPS	IV			1.0	%
Differential phase error	DP		IV			0.5	deg
Overrange recovery time			IV		1.0		ns
Power supply							
Analog supply current	I_{EEA}		II		320		mA
Digital supply current	I_{EED}		II		100		mA
Power consumption *4	Pd		II		2200		mW

*1 Test levels
- I ····· All-quantity test over full operating temperature range (Tc=–25 to +125°C)
- II ····· All-quantity test at Tc=+25°C
- III ····· Sampling test only
- IV ····· Design specifications
- V ····· Typical values only

*2 See Block Diagram

*3 TPS: times per sample

*4 $Pd=I_{EEA} \cdot AV_{EE}+I_{EED} \cdot DV_{EE}+\frac{(V_{RT}-V_{RB})^2}{R_{REF}}$

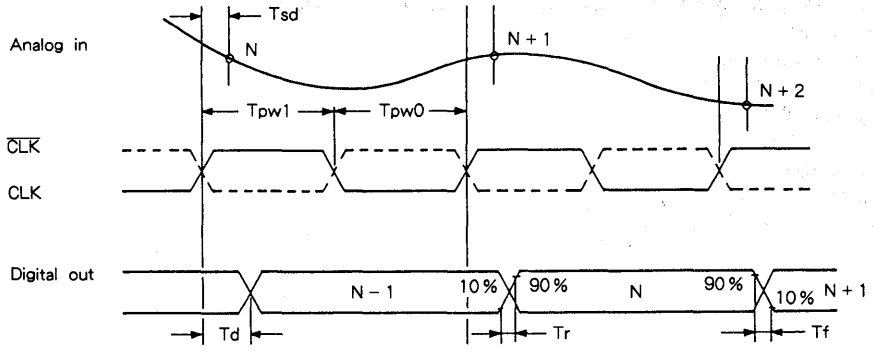
4

Input Voltage vs. Digital Output

V_{IN}*	Step	MINV 1 LINV 1			0 1			1 0			0 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000·····00		0	100·····00		0	011·····11		0	111·····11	
	0	1	000·····00		1	100·····00		1	011·····11		1	111·····11	
	1	1	000·····01		1	100·····01		1	011·····10		1	111·····10	
			⋮			⋮			⋮			⋮	
−1V	127	1	011·····11		1	111·····11		1	000·····00		1	100·····00	
	128	1	100·····00		1	000·····00		1	111·····11		1	011·····11	
			⋮			⋮			⋮			⋮	
	254	1	111·····10		1	011·····10		1	100·····01		1	000·····01	
	255	1	111·····11		1	011·····11		1	100·····00		1	000·····00	
−2V		1	111·····11		1	011·····11		1	100·····00		1	000·····00	

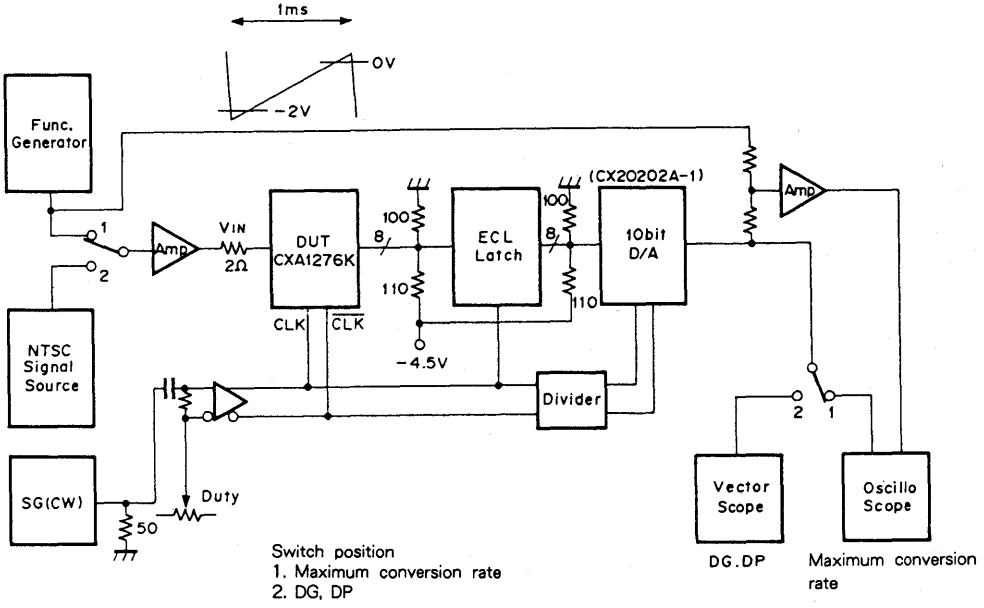
* V_{RT}=V_{RTS}=0V, V_{RM}=−1V or Open, V_{RB}=V_{RBS}=−2V

Timing Diagram

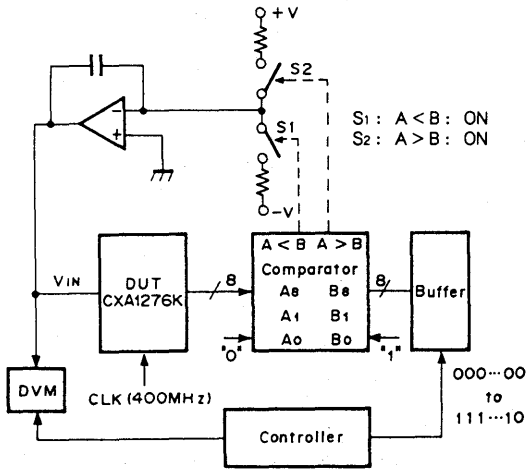


Electrical Characteristics Test Circuit

Maximum conversion rate test circuit
Differential gain error test circuit
Differential phase error test circuit

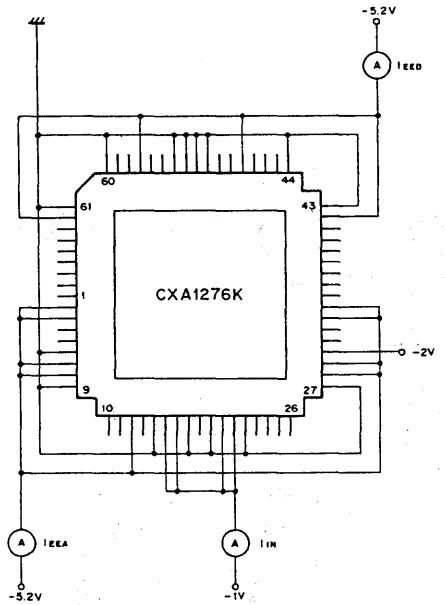


Integral linearity error test circuit
Differential linearity error test circuit

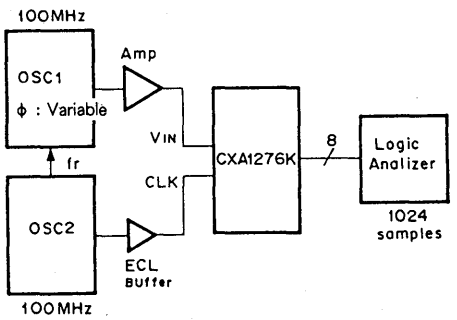


Power Supply Current Test Circuit

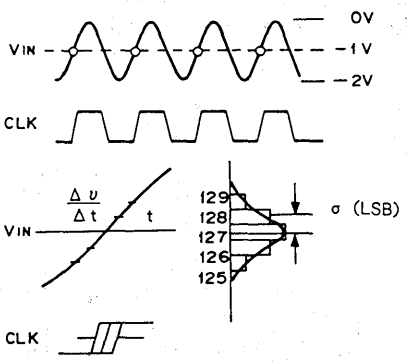
Analog input bias current test circuit



Sampling delay test circuit
Aperture jitter test circuit



Aperture jitter test method



Aperture jitter

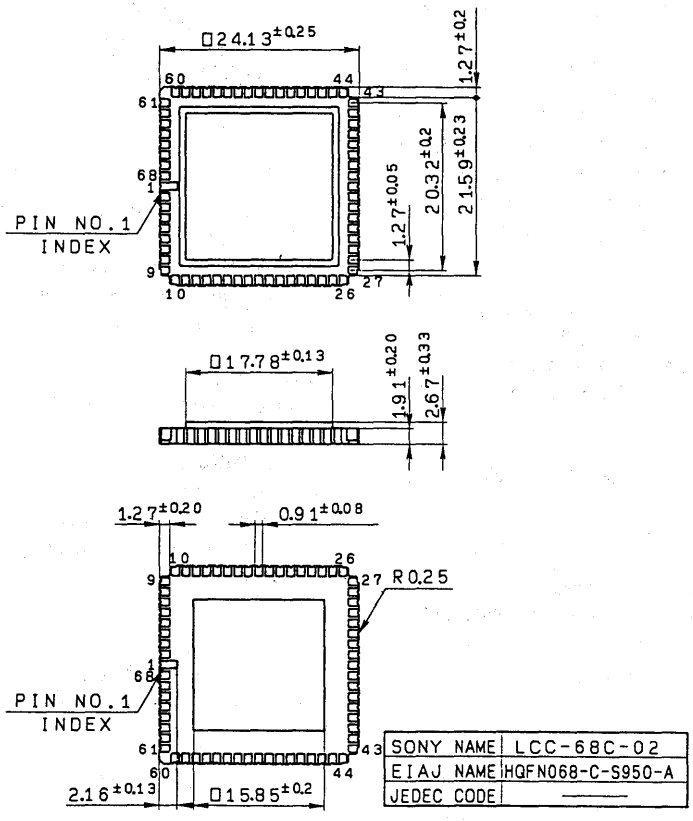
Aperture jitter is defined as follows :

$$Taj = \sigma / \frac{\Delta \upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right),$$

Where σ (unit : LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

Package Outline Unit : mm

68pin LCC (Ceramic)



4

SONY

CXA1386P/K

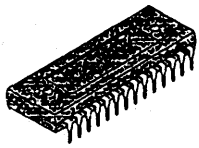
8-bit 75 MSPS Flash A/D Converter

Description

The CXA1386P/K are 8-bit high-speed flash A/D converter ICs capable of digitizing analog signals at the maximum rate of 75 MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

The CXA1386P/K are pin-compatible with the earlier models CXA1056P/K, CXA1016P/K, respectively. These can be replaced by the CXA1386P/K without any design changes in most cases. Compared with the earlier models, these new models have been greatly improved in performance, by incorporating advanced process, new circuit design and carefully considered layout.

CXA1386P
28 pin DIP (Plastic)



CXA1386K
44 pin LCC (Ceramic)

Features

- Differential linearity error: ±1/2 LSB or less
- Integral linearity error: ±1/2 LSB or less
- Built-in integral linearity compensation circuit
- High-speed operation with maximum conversion rate of 75 MSPS (Min.)
- Low input capacitance: 17pF (Typ.)
- Wide analog input bandwidth: 150MHz (Min. for full-scale input)
- Single power supply: –5.2V
- Low power consumption: 580mW (Typ.)
- Low error rate
- Operable at 50% clock duty cycle
- Good temperature characteristics
- Capable of driving 50 Ω loads

Structure

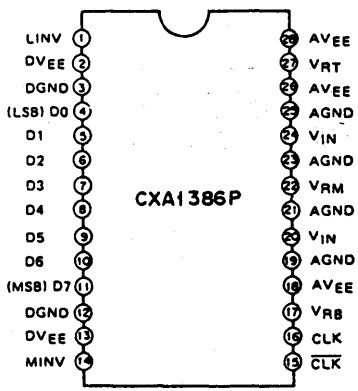
Bipolar silicon monolithic IC

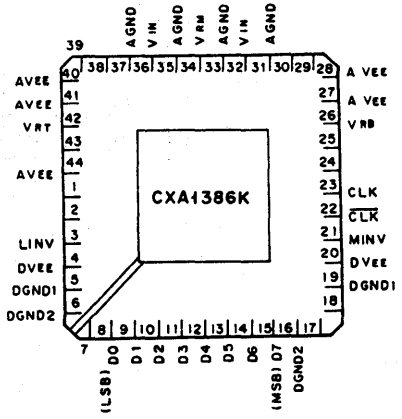
Applications

- Digital oscilloscopes
- HDTV (high-definition TVs)
- Other apparatus requiring high-speed A/D conversion

Pin Configuration (Top View)

Pins without name are NC pins (not connected)





Absolute Maximum Ratings (Ta=25°C)

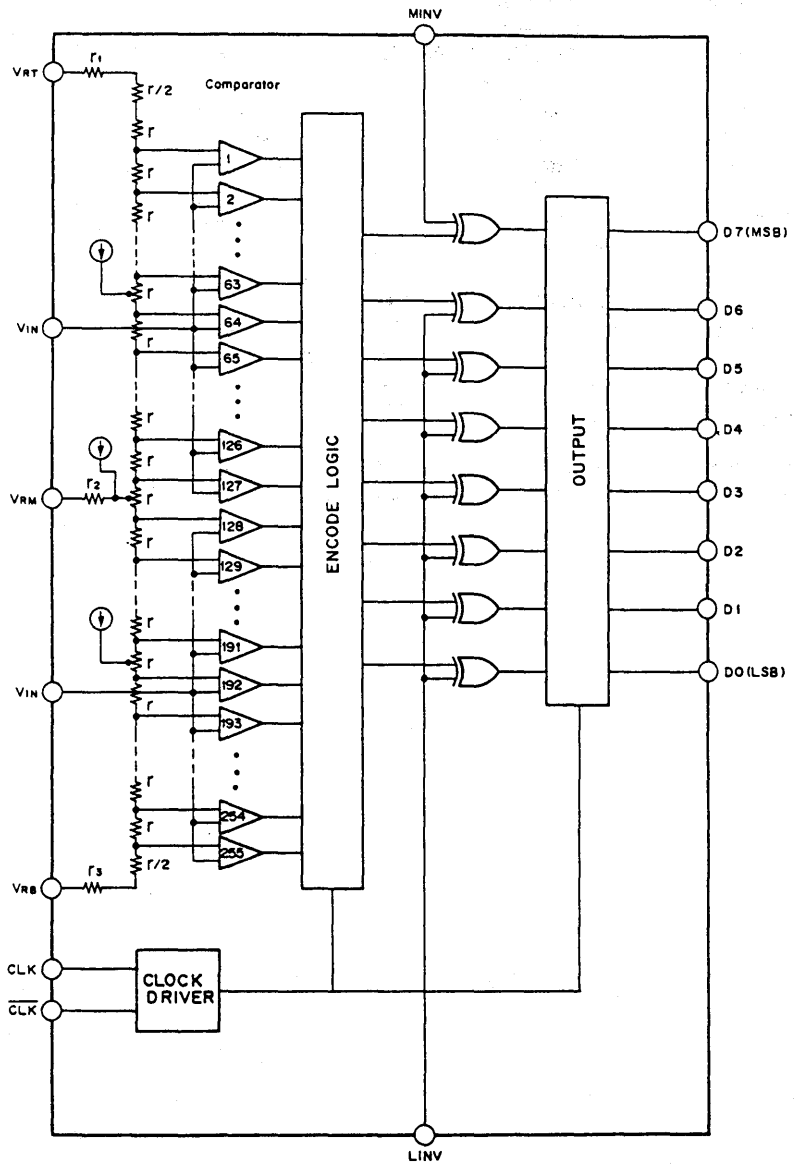
• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5 V
• Analog input voltage	V_{IN}	−2.7 to +0.5 V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	−2.7 to +0.5 V
	$\lvert V_{RT}-V_{RB} \rvert$	2.5 V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	−4 to +0.5 V
	$\lvert CLK-\overline{CLK} \rvert$	2.7 V
• V_{RM} pin input current	I_{VRM}	−3 to +3 mA
• Digital output current	ID_0 to ID_7	−30 to 0 mA
• Storage temperature	Tstg	−65 to +150 °C

Recommended Operating Conditions

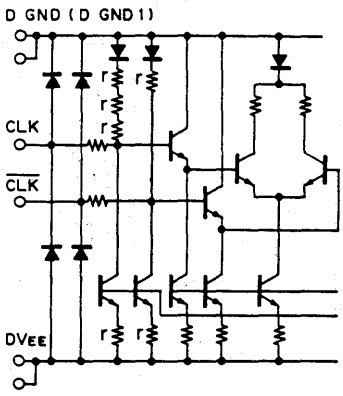
		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.5	−5.2	−4.95	V
	$AV_{EE}-DV_{EE}$	−0.05	0	0.05	V
	AGND−DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2.0	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Pulse width of clock	T_{PW1}	6.6			ns
	T_{PW0}	6.6			ns
• Operating temperature	Ta (CXA1386P)	−20		+75	°C
	Tc (CXA1386K)	−20		+100	°C

4

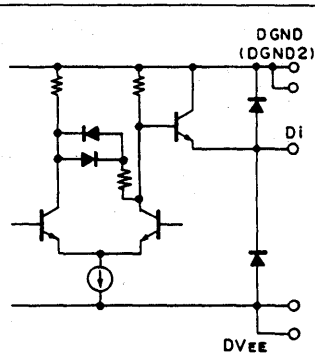
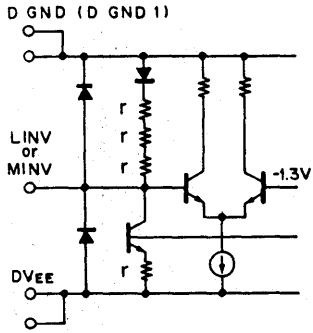
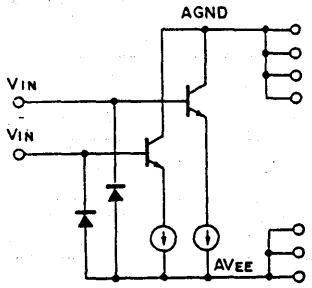
Block Diagram

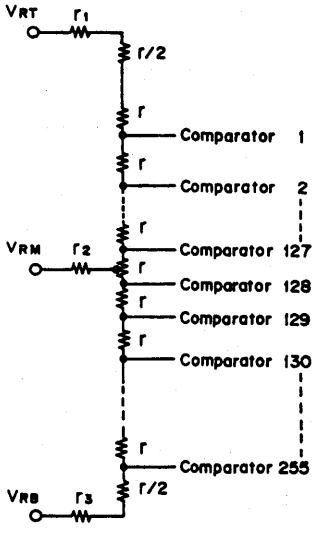


Pin Description and I/O pin Equivalent circuit

Pin No. DIP	Pin No. LCC	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
19, 21, 23, 25	31, 33 35, 37	AGND	—	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND or GND1/2.
18, 26, 28	27, 28 40, 41 44	AVEE	—	–5.2V		Analog VEE. –5.2V (Typ.). Internally connected with DVEE (resistance: 4 to 6Ω). Ceramic chip capacitors of at least 0.1 μF should be used to connect to AGND and be placed near the pins.
16	23	CLK	I	ECL		CLK input
15	22	$\overline{CLK}$				Input complementary to CLK. With open connection, kept at threshold voltage (–1.3V). Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain stable high-speed operation.
3, 12	—	DGND	—	0V		Digital GND (Used for internal circuits and output transistors)
—	5, 19	DGND1	—	0V		Digital GND (Used for internal circuits)
—	6, 16	DGND2	—	0V		Digital GND (Used for output buffers)
2, 13	4, 20	DVEE	—	–5.2V		Digital VEE. Internally connected with AVEE (resistance: 4 to 6Ω). Ceramic chip capacitors of at least 0.1 μF should be used to connect to DGND and be placed near the pins.

4

Pin No. DIP	Pin No. LCC	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
4	8	D0	O	ECL		LSB of data outputs. An external pull-down resistor is required.
5	9	D1				Data outputs. External pull-down resistors are required.
6	10	D2				
7	11	D3				
8	12	D4				
9	13	D5				
10	14	D6				
11	15	D7				MSB of data outputs. An external pull-down resistor is required.
1	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see Output Coding). With open connection, kept at "L" level.
14	21	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see Output Coding). With open connection, kept at "L" level.
20, 24	32, 36	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions.

Pin No. DIP	Pin No. LCC	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
17	26	V_{RB}	I	−2V		Reference voltage (bottom) Typically −2V A ceramic capacitor of at least 0.1 µF and a tantalus capacitor of at least 10 µF should be used to connect to AGND and be placed near the pin.
22	34	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point Can be used as a pin for integral linearity compensation.
27	42	V_{RT}	I	0V		Reference voltage (top) Typically 0V

4

Electrical Characteristics

(Ta=25°C, AVEE=DVEE=–5.2V, VRT=0V, VRB=–2V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n		8	8	8	bits
DC characteristics						
Integral linearity error	EIL	Fc=75MSPS		±0.3	±0.5	LSB
Differential linearity error	EDL	Fc=75MSPS		±0.3	±0.5	LSB
Analog input						
Analog input capacitance	CIN	VIN=–1V+0.07Vrms		17		pF
Analog input resistance	RIN			390		kΩ
Input bias current	IIN	VIN=–1V			200	μA
Reference inputs						
Reference resistance	RREF		75	110	155	Ω
Offset voltage VRT	EOT		8	18	32	mV
VRB	EOB		0	10	24	mV
Digital inputs						
Logic H level	VIH		–1.13			V
Logic L level	VIL				–1.50	V
Logic H current	IIH	–0.8V is applied to input	0		50	μA
Logic L current	IIL	–1.6V is applied to input	–50		50	μA
Input capacitance				7		pF
Switching characteristics						
Maximum conversion rate	Fc	Error rate of 10^{-9} TPS *1	75			MSPS
Aperture jitter	Taj			10		ps
Sampling delay	Tds			3.0		ns
Output delay	Tdo		4.0	6.5	9.0	ns
H pulse width of clock	TPW1		6.6			ns
L pulse width of clock	TPW0		6.6			ns
Digital outputs						
Logic H level	VOH	RL=620 Ω to DVEE	–1.03			V
Logic L level	VOL	RL=620 Ω to DVEE			–1.62	V
Output rising time	Tr	RL=620 Ω to DVEE, 20% to 80%		0.9		ns
Output falling time	Tf	RL=620 Ω to DVEE, 20% to 80%		2.1		ns
Dynamic characteristics						
Input bandwidth		VIN=2Vp-p, Input frequency at –3dB	150			MHz
S/N ratio		Input=1MHz, FS Clock=75MHz		46		dB
		Input=18.75MHz, FS Clock=75MHz		40		dB
Error rate		Input=18.749MHz, FS Error>16LSB Clock=75MHz			10^{-9}	TPS *1
Differential gain error	DG	NTSC 40IRE mod. ramp, Fc=75MSPS		1.0		%
Differential phase error	DP			0.5		deg
Power supply						
Supply current	IEE		–150	–104		mA
Power consumption *2	Pd			580		mW

*1 TPS: times per sample

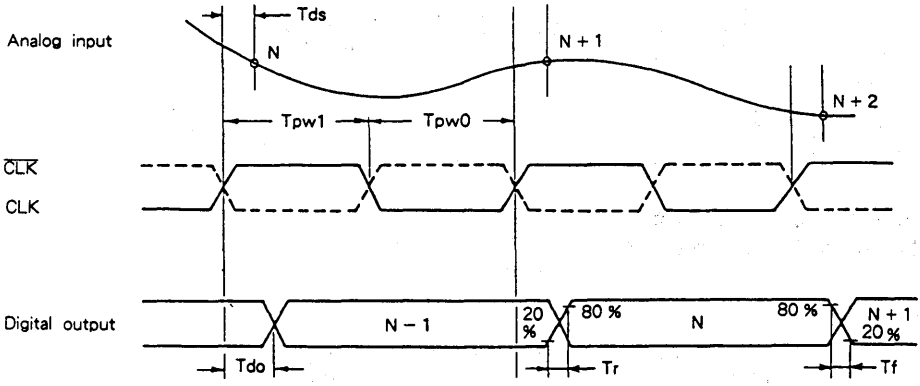
*2 $Pd = I_{EE} \cdot V_{EE} + \frac{(V_{RT}-V_{RB})^2}{R_{REF}}$

Output Coding

V_{IN} *	Step	MINV 1 LINV 1	0 1	1 0	0 0
		D7 D0	D7 D0	D7 D0	D7 D0
0V		000·····00	100·····00	011·····11	111·····11
	0	000·····00	100·····00	011·····11	111·····11
	1	000·····01	100·····01	011·····10	111·····10
		⋮	⋮	⋮	⋮
−1V	127	011·····11	111·····11	000·····00	100·····00
	128	100·····00	000·····00	111·····11	011·····11
		⋮	⋮	⋮	⋮
	254	111·····10	011·····10	100·····01	000·····01
	255	111·····11	011·····11	100·····00	000·····00
−2V		111·····11	011·····11	100·····00	000·····00

* V_{RT}=0V, V_{RB}=−2V

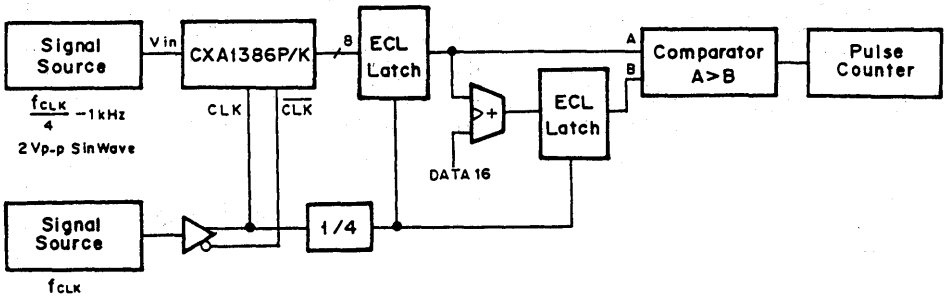
Timing diagram



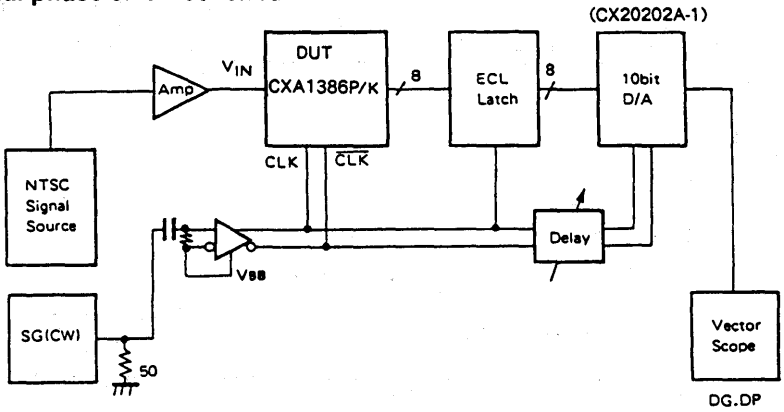
4

Electrical Characteristics Test Circuit

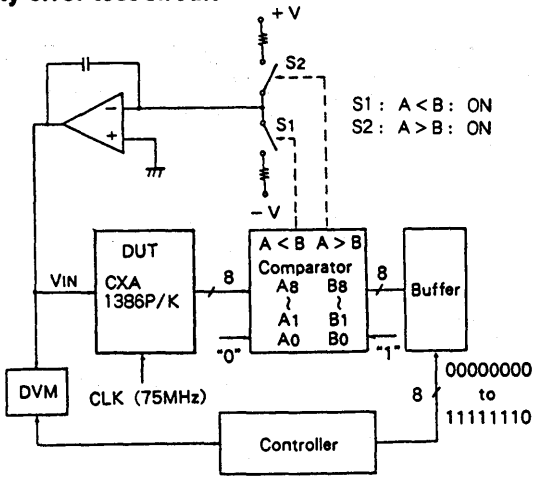
Maximum conversion rate test circuit



Differential gain error test circuit
Differential phase error test circuit

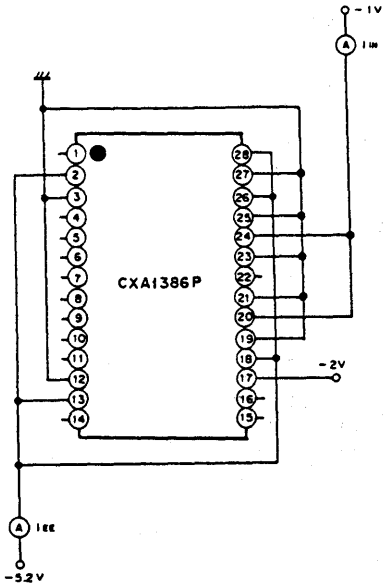


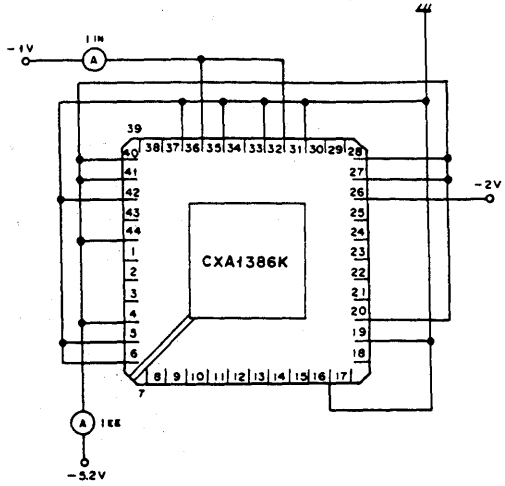
Integral linearity error test circuit
Differential linearity error test circuit



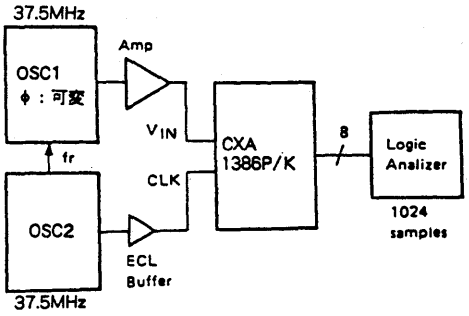
Power Supply Current Test Circuit

Analog Input bias current test circuit

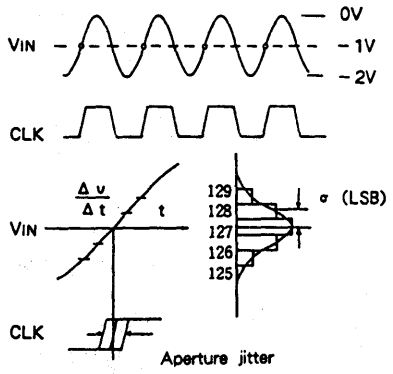




Sampling delay test circuit
Aperture jitter test circuit



Aperture jitter test method



Aperture jitter is defined as follows :

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right),$$

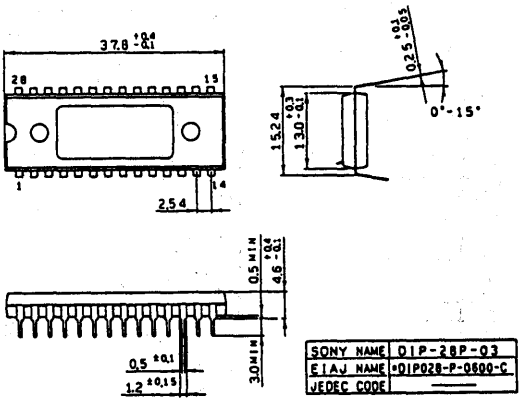
Where σ (unit : LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

4

Package Outline Unit : mm

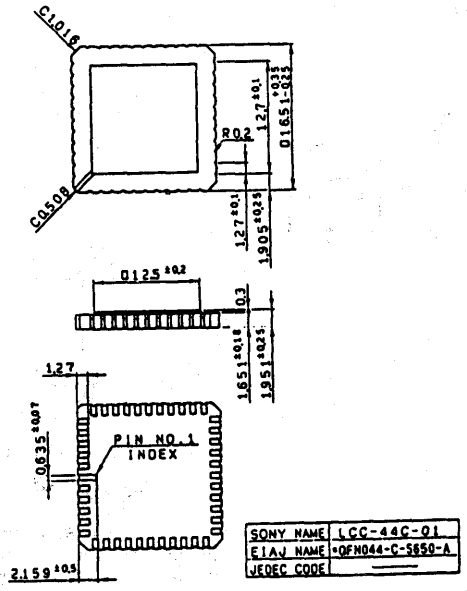
CXA1386P

28pin DIP (Plastic) 600mil 4.2g



CXA1386K

44pin LCC (Ceramic) 1.8g



SONY®

CXA1396D/K

8-bit 125 MSPS Flash A/D Converter

Description

The CXA1396D/K are 8-bit ultrahigh-speed flash A/D converter ICs capable of digitizing analog signals at the maximum rate of 125 MSPS. The digital I/O levels of these A/D converters are compatible with the ECL 100K/10KH/10K.

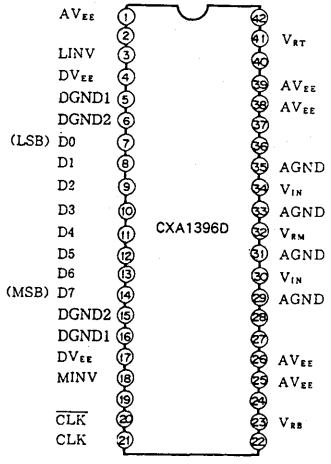
The CXA1396D is pin-compatible with the earlier model CX20116, and the CXA1396K with the CXA1066K. They can replace the earlier models respectively, without any design changes, in most cases. Compared with the earlier models, these new models have been greatly improved in performance, by incorporating advanced process, new circuit design and carefully considered layout.

Features

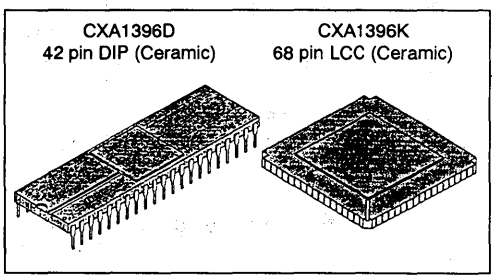
- Differential linearity error: ±1/2 LSB or less
- Integral linearity error: ±1/2 LSB or less
- Built-in integral linearity compensation circuit
- Ultrahigh-speed operation with maximum conversion rate of 125 MSPS (Min.)
- Low input capacitance: 17pF (Typ.)
- Wide analog input bandwidth: 200MHz (Min. for full-scale input)
- Single power supply: –5.2V

Pin Configuration

Pins without name are NC pins (not connected).



(Top View)



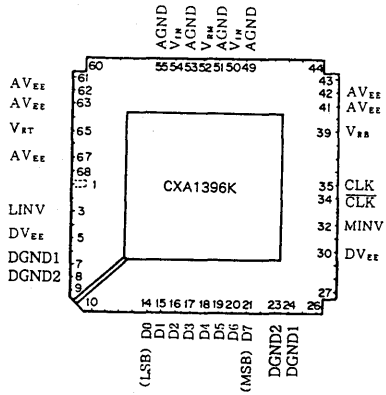
- Low power consumption: 870mW(Typ.)
- Low error rate
- Operable at 50% clock duty cycle
- Good temperature characteristics
- Capable of driving 50 Ω loads
- 2 types of packages for selection according to applications

Structure

Bipolar silicon monolithic IC

Applications

- Digital oscilloscopes
- HDTV(high-definition TVs)
- Other apparatus requiring ultrahigh-speed A/D conversion



(Top View)

4

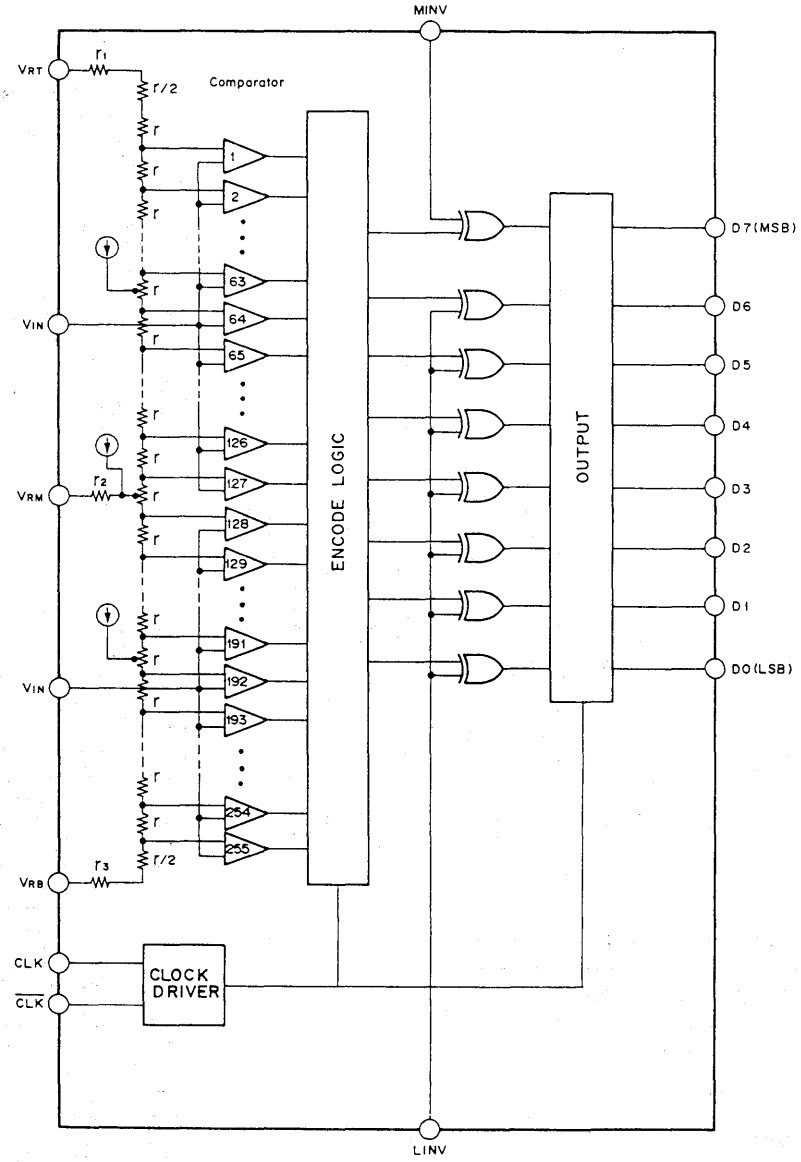
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5 V
• Analog input voltage	V_{IN}	−2.7 to +0.5 V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	−2.7 to +0.5 V
	$\lvert V_{RT}-V_{RB}\rvert$	2.5 V
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	−4 to +0.5 V
	$\lvert CLK-\overline{CLK}\rvert$	2.7 V
• V_{RM} pin input current	I_{VRM}	−3 to +3 mA
• Digital output current	ID_0 to ID_7	−30 to 0 mA
• Storage temperature	Tstg	−65 to +150 °C

Recommended Operating Conditions

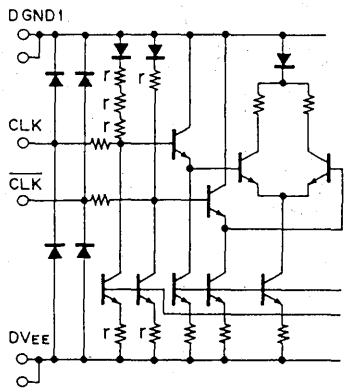
		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.5	−5.2	−4.95	V
	$AV_{EE}-DV_{EE}$	−0.05	0	0.05	V
	AGND−DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2.0	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Pulse width of clock	Tpw_1	4.0			ns
	Tpw_0	4.0			ns
• Operating temperature	Ta (CXA1396D)	−20		+75	°C
	Tc (CXA1396K)	−20		+100	°C

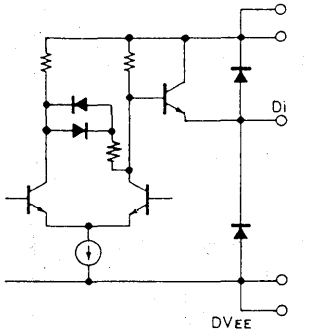
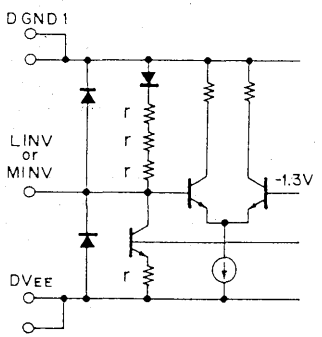
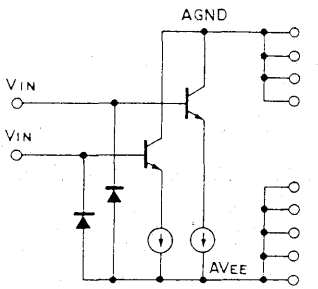
Block Diagram



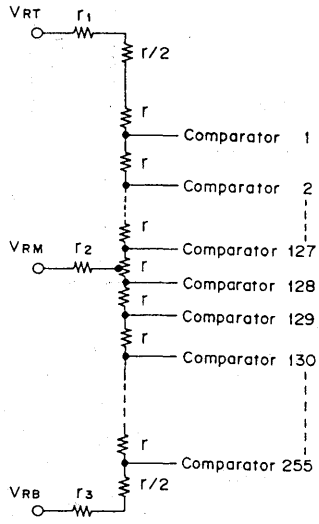
4

Pin Description and I/O pin Equivalent circuit

Pin No. DIP	Pin No. LCC	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
29, 31, 33, 35	49, 51, 53, 55	AGND	—	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND1, DGND2.
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AVEE	—	–5.2V		Analog VEE –5.2V (Typ.). Internally connected with DVEE (resistance: 4 to 6 Ω). A ceramic chip capacitor of at least 0.1 μF should be used to connect to AGND and be placed near the pins.
21	35	CLK	I	ECL		CLK input
20	34	$\overline{CLK}$				Input complementary to CLK. With open connection, kept at threshold voltage (–1.3V). Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain the stable high-speed operation.
5, 16	7, 24	DGND1	—	0V		Digital GND for internal circuits
6, 15	8, 23	DGND2	—	0V		Digital GND for output transistors
4, 17	5, 30	DVEE	—	–5.2V		Digital VEE Internally connected with AVEE (resistance:4 to 6 Ω). A ceramic chip capacitor of at least 0.1 μF should be used to connect to DGND and be placed near the pins.

Pin No. DIP	Pin No. LCC	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
7	14	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
8	15	D1				Data outputs. External pull-down resistors are required.
9	16	D2				
10	17	D3				
11	18	D4				
12	19	D5				
13	20	D6				
14	21	D7				MSB of data outputs. External pull-down resistor is required.
3	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see output code table). With open connection, kept at "L" level.
18	32	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see output code table). With open connection, kept at "L" level.
30, 34	50, 54	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions.

4

Pin No. DIP	Pin No. LCC	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
23	39	V_{RB}	I	–2V		Reference voltage (bottom) Typically –2V A ceramic capacitor of at least 0.1 µF and a tantalus capacitor of at least 10 µF should be used to connect to AGND and be placed near the pins.
32	52	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point Can be used as a pin for integral linearity compensation.
41	65	V_{RT}	I	0V		Reference voltage (top) Typically 0V When a voltage different from AGND is applied to this pin, a ceramic capacitor of at least 0.1 µF and a tantalus capacitor of at least 10 µF should be used to connect to AGND and be placed near the pins.
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9 to 13, 22, 25 to 29, 31, 33, 36 to 38, 40, 43 to 48, 56 to 61, 64, 66, 68	NC	—	—		Unused pins No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended.

Electrical Characteristics

(Ta=25°C, AVEE=DVEE=–5.2V, VRT=0V, VRB=–2V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n			8		bits
DC characteristics						
Integral linearity error	EIL	Fc=125MSPS		±0.3	±0.5	LSB
Differential linearity error	EDL	Fc=125MSPS		±0.3	±0.5	LSB
Analog input						
Analog input capacitance	CIN	VIN=–1V+0.07Vrms		17		pF
Analog input resistance	RIN			190		kΩ
Input bias current	IIN	VIN=–1V		130	320	μA
Reference inputs						
Reference resistance	RREF		75	110	155	Ω
Offset voltage VRT	EOT		16	19	24	mV
VRB	EOB		10	15	20	mV
Digital inputs						
Logic H level	VIH		–1.13			V
Logic L level	VIL				–1.50	V
Logic H current	IIH	Input connected to –0.8V	0		50	μA
Logic L current	IIL	Input connected to –1.6V	0		50	μA
Input capacitance				7		pF
Switching characteristics						
Maximum conversion rate	Fc	Error rate 10^{-9} TPS *1	125			MSPS
Aperture jitter	Taj			10		ps
Sampling delay	Tds			1.5		ns
Output delay	Tdo		3.0	3.6	4.2	ns
H pulse width of clock	TPW1		4.0			ns
L pulse width of clock	TPW0		4.0			ns
Digital outputs						
Logic H level	VOH	RL=50 Ω to –2V	–1.10			V
Logic L level	VOL	RL=50 Ω to –2V			–1.62	V
Output rising time	Tr	RL=50 Ω to –2V, 20% to 80%		0.8		ns
Output falling time	Tf	RL=50 Ω to –2V, 20% to 80%		1.0		ns
Dynamic characteristics						
Input bandwidth		VIN=2Vp-p	200			MHz
S/N ratio		Input=1MHz, FS, Clock=125MHz		46		dB
		Input=31.5MHz, FS, Clock=125MHz		40		dB
Error rate		Input=31.249MHz, FS, Error>16LSB, Clock=125MHz			10^{-9}	TPS *1
Differential gain error	DG	NTSC 40IRE mod. ramp, Fc=125MSPS		1.0		%
Differential phase error	DP			0.5		deg
Power supply						
Supply current	IEE		–230	–160		mA
Power consumption *2	Pd			870		mW

*1 TPS: times per sample

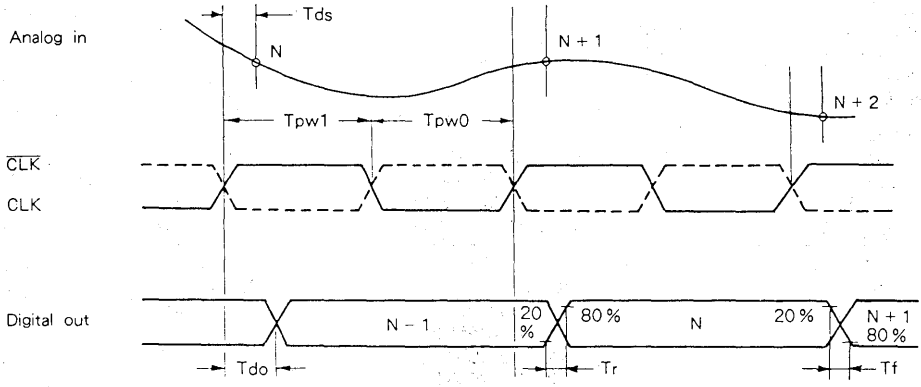
*2 $Pd = I_{EE} \cdot V_{EE} + \frac{(V_{RT}-V_{RB})^2}{R_{REF}}$

Output Code Table

V_{IN} *	Step	MINV 1 LINV 1		0 1		1 0		0 0	
		D7	D0	D7	D0	D7	D0	D7	D0
0V		000·····00		100·····00		011·····11		111·····11	
	0	000·····00		100·····00		011·····11		111·····11	
	1	000·····01		100·····01		011·····10		111·····10	
		⋮		⋮		⋮		⋮	
−1V	127	011·····11		111·····11		000·····00		100·····00	
	128	100·····00		000·····00		111·····11		011·····11	
		⋮		⋮		⋮		⋮	
	254	111·····10		011·····10		100·····01		000·····01	
	255	111·····11		011·····11		100·····00		000·····00	
−2V		111·····11		011·····11		100·····00		000·····00	

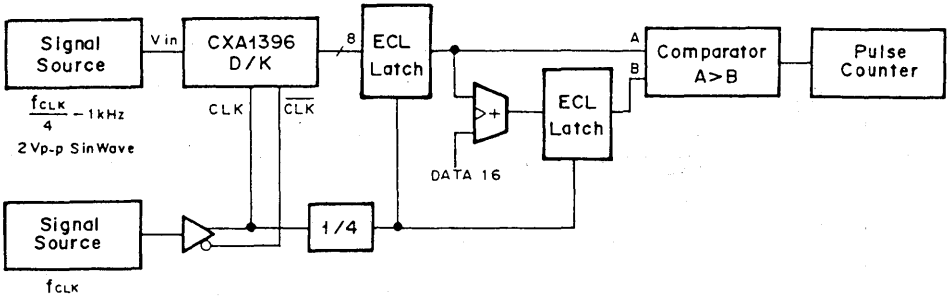
* V_{RT}=0V, V_{RB}=−2V

Timing diagram

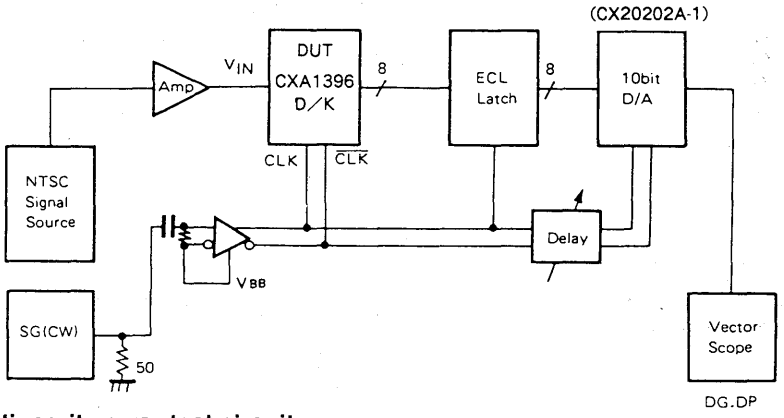


Electrical Characteristics Test Circuit

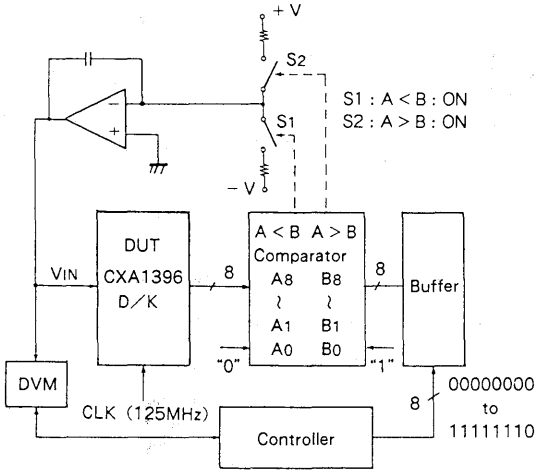
Maximum conversion rate test circuit



Differential gain error test circuit
Differential phase error test circuit

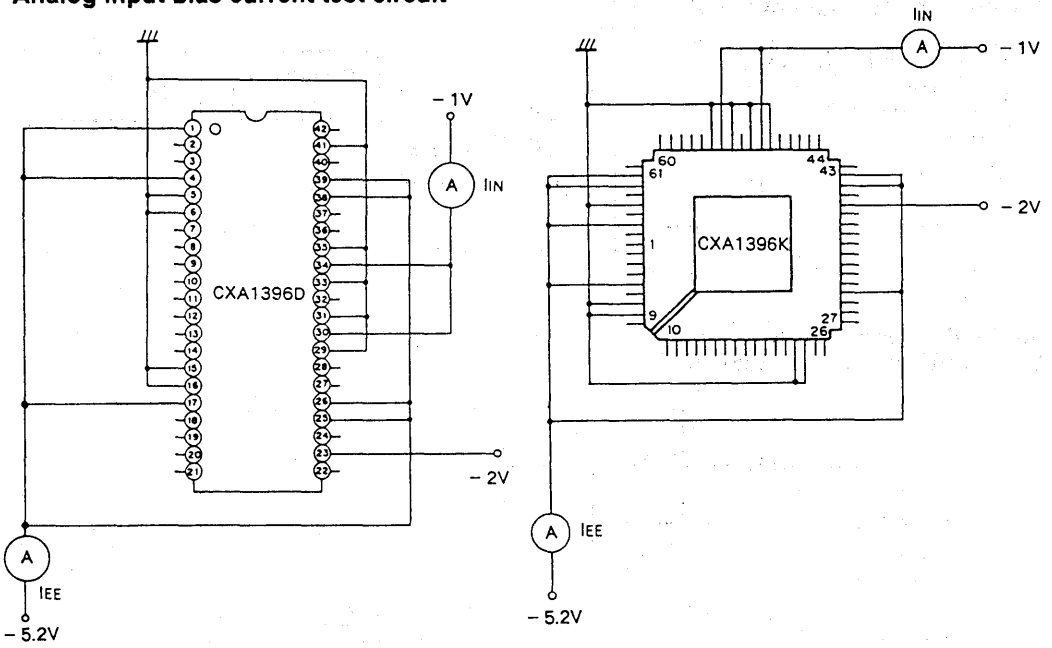


Integral linearity error test circuit
Differential linearity error test circuit

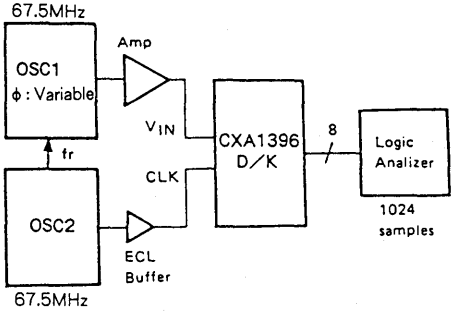


Power Supply Current Test Circuit

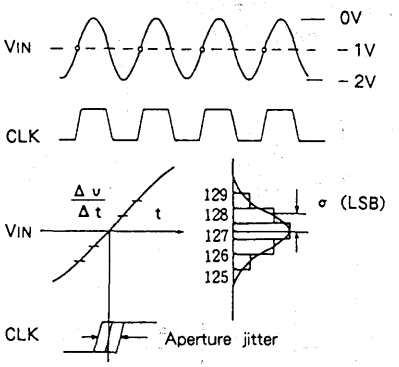
Analog input bias current test circuit



Sampling delay test circuit
Aperture jitter test circuit



Aperture jitter test method



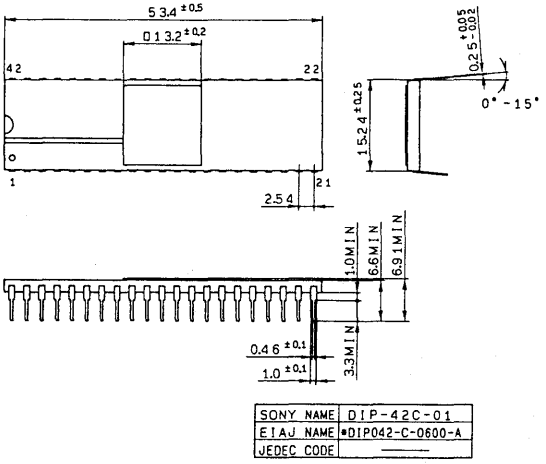
Aperture jitter is defined as follows :

$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right),$$

Where σ (unit : LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

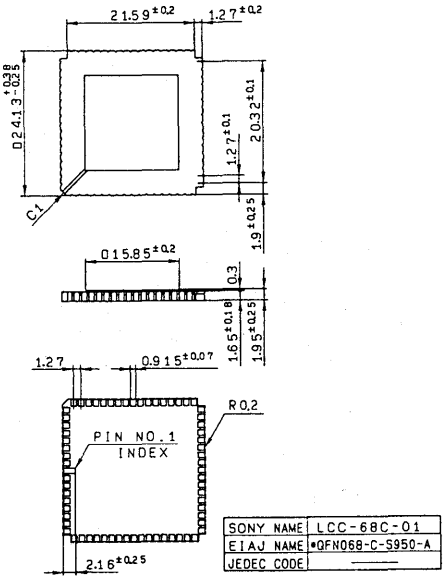
Package Outline Unit : mm

CXA1396D 42pin DIP (Ceramic) 600mil 6.7g

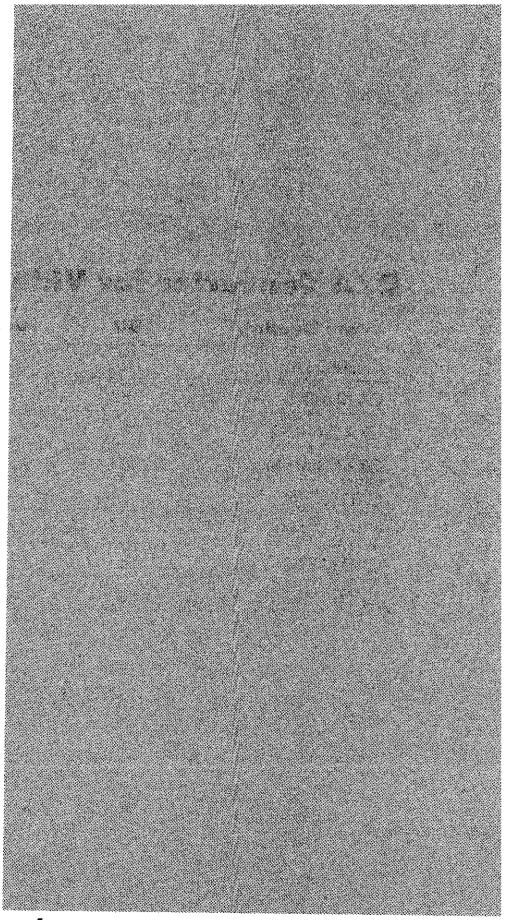


SONY NAME	DIP-42C-01
EIAJ NAME	*DIP042-C-0600-A
JEDEC CODE	———

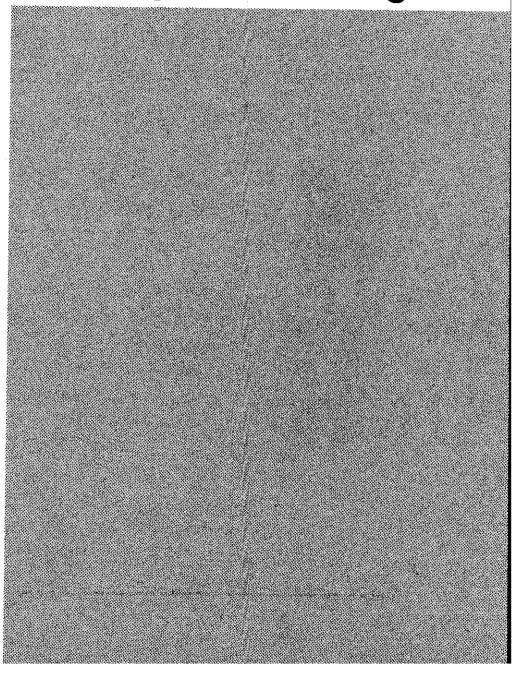
CXA1396K 68pin LCC (Ceramic) 3.7g



SONY NAME	LCC-68C-01
EIAJ NAME	*QFN068-C-S950-A
JEDEC CODE	———



D/A Converter for Video Signal Processing



D/A Converter for Video Signal Processing

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20051A	10	30	550	ECL Input, 1 Channel	223-234
CX20206	8	35	360	TTL Input, 3 Channel	235-250
CXA1260Q-Z	8	35	360	TTL Input, 3 Channel	251-266
CXA1106P/M	8	35	360	TTL Input, 1 Channel	267-285
CXD1170M	6	40	80	TTL I/O D/A CMOS	286-293
CXD1171M	8	40	80	TTL I/O D/A CMOS	294-301
CXD1177Q	8	40	160	TTL I/O 2 channel D/A CMOS	302-311
CXD1178Q	8	40	240	TTL I/O 3 channel D/A CMOS	312-322

SONY

CX20051A

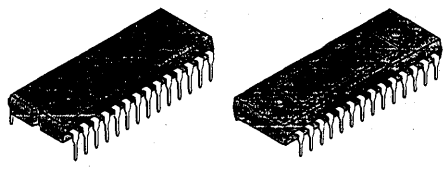
10 bit 30 MSPS D/A Converter (ECL input)

Description

The CX20051A is 10 bit, 30 MSPS D/A Converter, designed for a video signal processing. The broadcasting application will require the fairly high resolution for D/A. The CX20051A is suitable for the high definition TV application, too.

The external resistor can control the voltage output range of the D/A. The CX20051A requires −5V single power supply, the ECL digital inputs, and the differencial ECL clocks, to operate.

28 pin DIP (Plastic)



Features

- Maximum conversion frequency 30 MSPS
- High resolution 10 bit
- Low power consumption 550 mW
- −5V single power supply
- Clock input and digital input are in ECL level

Structure

Bipolar silicon monolithic IC.

Block Diagram and Pin Connection

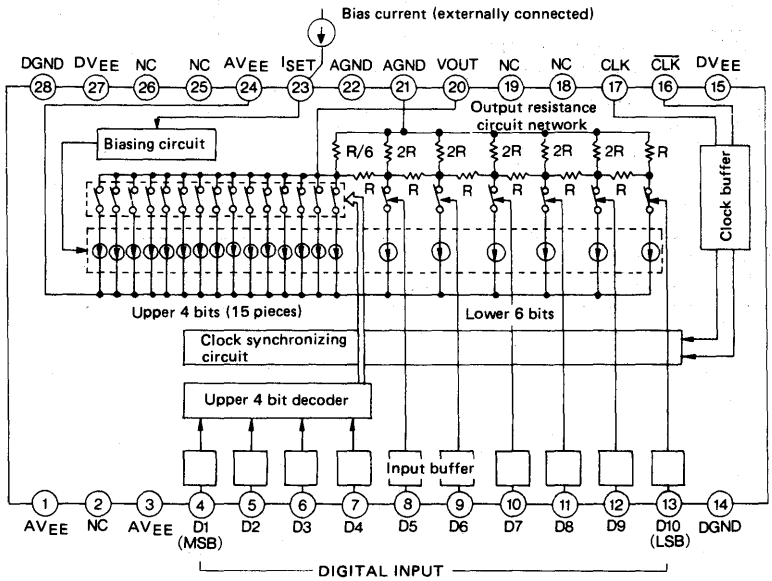


Fig. 1

5

E89Z12 – ST

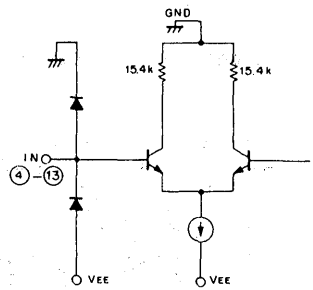
Absolute Maximum Ratings (Ta=25°C)

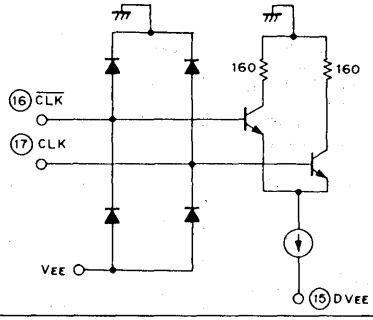
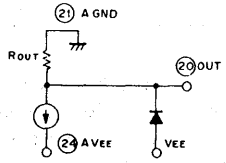
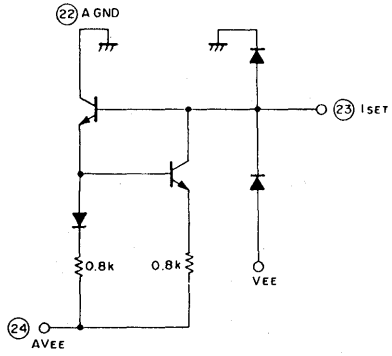
• Supply voltage	V_{EE}	−12	V
• Digital input voltage	V_{IN}	V_{EE} to 0	V
• Operating temperature	Topr	−10 to +70	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation		1.47	W

Recommended Operating Conditions

• Supply voltage	V_{EE}	−5.0 ± 0.25	V
• Digital input voltage	V_{IH}	−0.89 ± 0.15	V
	V_{IL}	−1.75 ± 0.15	V
• Dynamic range	V_O	−1.5 to −0.5	V
• Bias current	I_{SET}	1.0 ± 0.5	mA

Pin Description

No.	Symbol	Description	Equivalent circuit
1	D V_{EE}	Digital V_{EE} power supply (− 5V)	
2	NC	Non-connection	
3	D V_{EE}	Digital V_{EE} power supply (− 5V)	
4	NSB	10-bit digital input (MSB: Uppermost order, LSB: Lower most order)	
5	BIT2		
6	BIT3		
7	BIT4		
8	BIT5		
9	BIT6		
10	BIT7		
11	BIT8		
12	BIT9		
13	LSB		
14	D GND	Digital GND	
15	D V_{EE}	Digital V_{EE} power supply (−5V)	

No.	Symbol	Description	Equivalent circuit
16	$\overline{CLK}$	Clock bar input	
17	CLK	Clock input	
18	NC	Non-connection	
19	NC		
20	OUT	D/A output	
21	A GND	Analog GND Directly connected to the output resistance circuit network (ROUT)	
22	A GND	Analog GND For analog circuit system other than the output resistance circuit network	
23	ISET	Dynamic range adjusting pin	
24	A VEE	Analog VEE power supply (−5V)	
25	NC	Non-connection	
26	NC		
27	D VEE	Digital VEE power supply (−5V)	
28	D GND	Digital GND	

5

Electrical Characteristics

(Ta=25°C AGND=DGND=0V, AV_{EE}=DV_{EE}=−5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential linearity	D.L.	*1	−0.8	0	0.8	LSB
Maximum operating clock frequency	f_{MAX}	*2	30			MSPS
Differential gain	D.G.	NTSC 40IRE mod. ramp f_{CLK}=14.3MSPS		0.7		%
Differential phase	D.P.			0.2		deg
Circuit current	I_{EE}		88	110	132	mA
Output impedance	R_{OUT}		52	62	72	Ω
Input current	I_{IH}	Measured in the high level input voltage of the individual pins 4 to 13	1	3	10	μA
Input current	I_{IL}	Measured in the low level input voltage of the individual pins 4 to 13	0	20	300	nA

Note) As for the test circuit, see Fig. 2a to 2d.

*1 Input signal is digital ramp with 1 MHz clock.
Glitches are not the subject of the measurement.

*2 The maximum operating clock frequency which shows no bit error. Input signal is digital ramp.
Glitches are not the subject of the measurement.

Electrical Characteristics Test Circuit

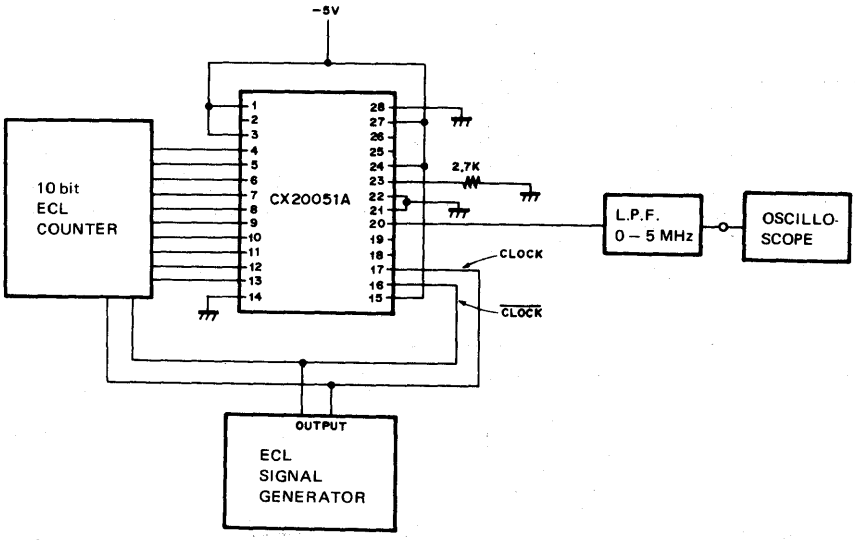


Fig. 2a Block diagram of differential linearity and maximum operating frequency test circuit

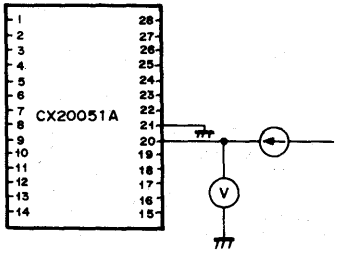


Fig. 2b Block diagram of output impedance test circuit

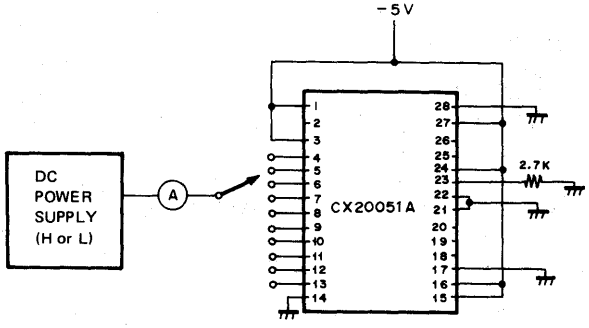


Fig. 2c Block diagram of input current test circuit

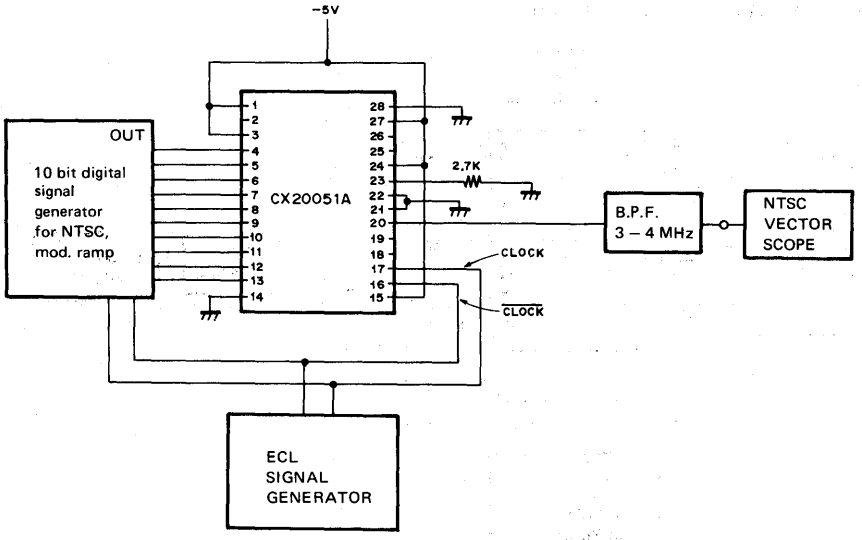


Fig. 2d Block diagram of DG and DP test circuit

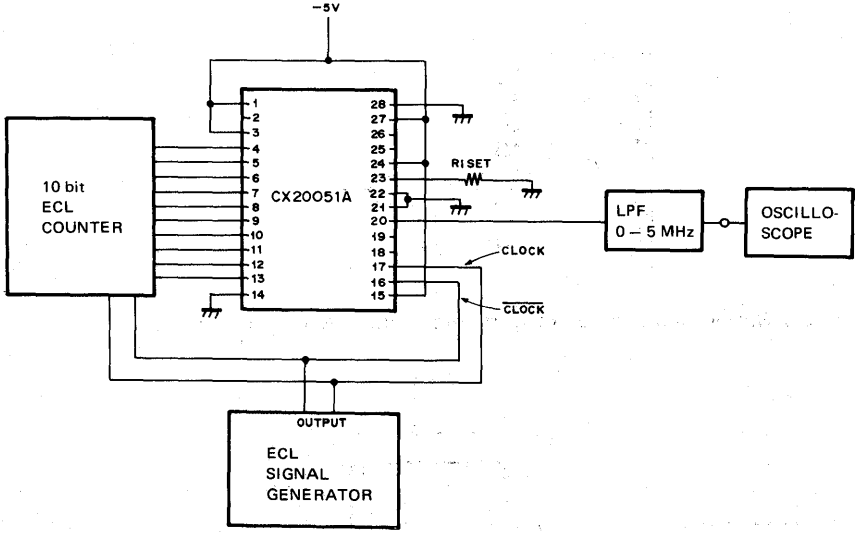


Fig. 2e Block diagram of dynamic range test circuit

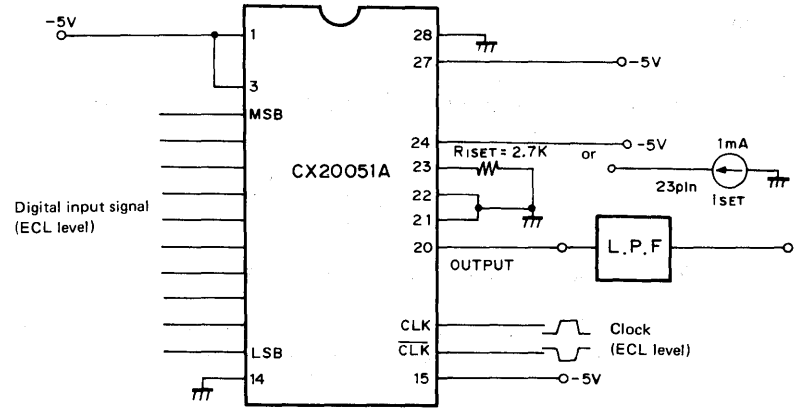


Fig. 3 Typical circuit connection

When changing the dynamic range of the output, change the value of R or the constant current supply value when a constant current supply is inserted in place of R. Both input and clock are in ECL level. Regarding the clock waveform, see the Note on Application.

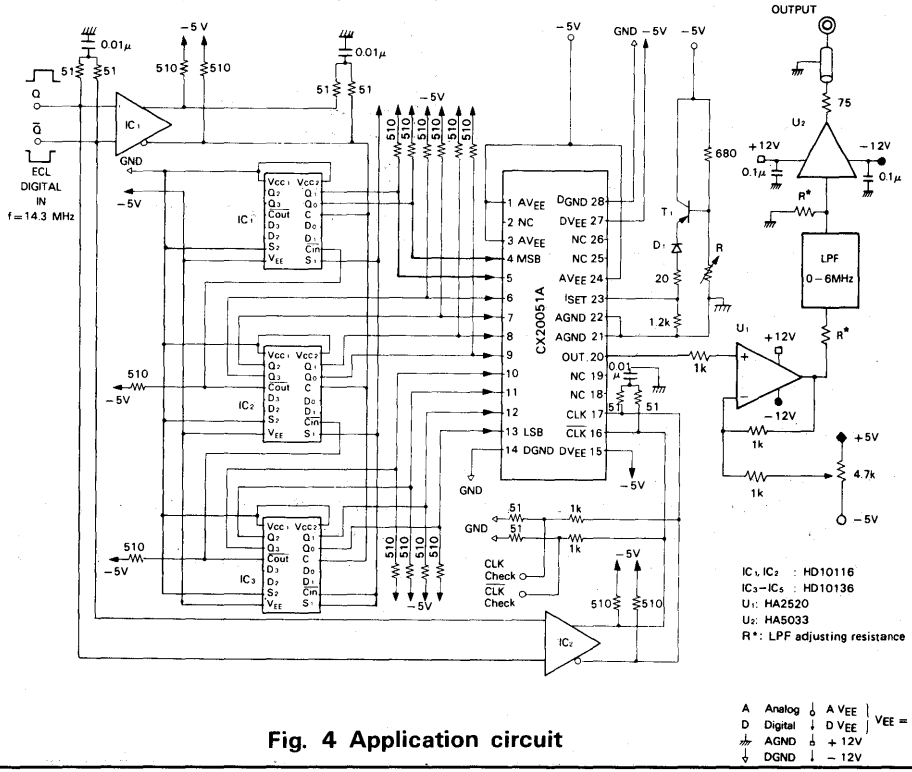


Fig. 4 Application circuit

Note on Application

(1) Applying clocks

(a) To pins 16 and 17, clock signals denoted as $\overline{\text{CLOCK}}$ and CLOCK are to be fed respectively. Both of their levels are ECL compatible levels.

Fig. 5a CLOCK and $\overline{\text{CLOCK}}$ waveforms

(b) Alternatively single-end method is usable to apply clock signal to the device. A clock signal of ECL level is to be fed to one of pin 16 or pin 17, with the other pin fixed to the ECL threshold level.

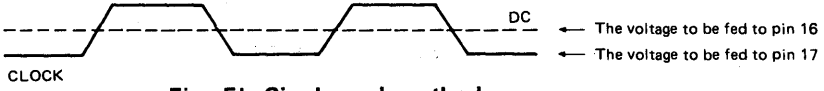
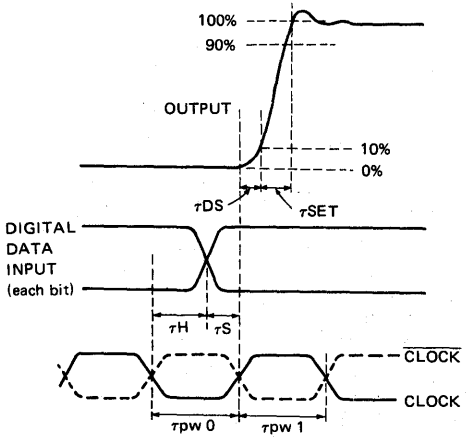


Fig. 5b Single-end method

(2) Timing chart

The timing between the CLOCK signal and 10 bit Digital Data Input signal is shown in the diagram below.



(Recommended operating condition)

$\tau H > 2$ ns

$\tau S > 10$ ns

The typical values of τDS and τSET under the above-mentioned condition are

$\tau DS \approx 7$ ns

$\tau SET \approx 4$ ns

for Z_L (load resistance) $> 10\ k\Omega$

Fig. 5c Timing chart

(3) Dynamic range (I_{SET} pin, pin 23)

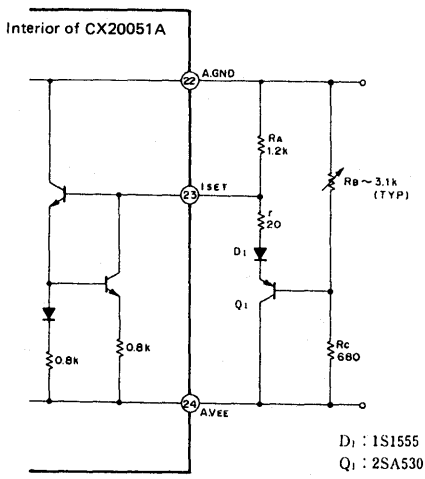
Dynamic range can be determined by connecting an external resistor (R_{ISET}) between the I_{SET} pin (pin 23) and the A GND pin (pin 22), or by applying a current source (I_{SET}) to the I_{SET} pin (pin 23). Typical values to obtain 1 V of dynamic range are 2.7 kΩ and 1 mA, for R_{ISET} and I_{SET} respectively (for a load resistance $Z_L > 10\ k\Omega$). (See the Dynamic range vs. R_{ISET} on page 11.)

(4) Input coding

STEPS	DIGITAL INPUT	ANALOG OUTPUT	
		CASE ①	CASE ②
0000	MSB1111111111LSB	−0.003V	−0.003V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
0511	1000000000	−0.4825V	−0.503V
0512	0111111111	−0.4835V	−0.504V
0513	0111111110	−0.4844V	−0.505V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
1023	0000000000	−0.963V	−1.003V

CASE ① : R_{ISET}=2.7 kΩ
(Output voltage is typical value.)
CASE ② : R_{ISET} is adjusted to obtain 1.000V full scale of analog output voltage.

(5) Temperature fluctuation compensation method of D/A output voltage dynamic range
When the temperature fluctuation of the outout voltage dynamic range poses a problem, a simple temperature compensation can be performed by adding a simple circuit externally.
Connecting diagram of the external circuit for temperature compensation is shown below. In this way, the temperature fluctuation may be limited to within ±150 ppm/°C.



5

(6) When the analog output level is at full scale 1 Vp-p, the 1LSB becomes approximately 1 mV. In order to obtain the predesignated characteristics, due care should be exercised in the designing of the CX20051A periphery circuit.

[Note on mounting onto the printed board]

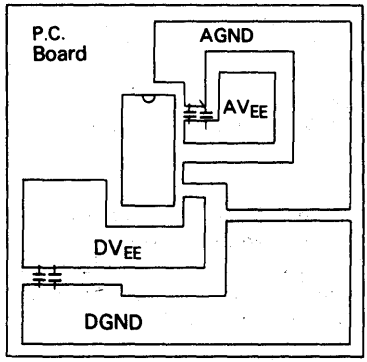
The external connection diagram of CX20051A is basically as shown in Fig. 3. In this regard, take note to the points mentioned below.

(1) AGND and DGND as also AV_{EE} and DV_{EE} are not connected internally. It is also desired to separate the analog block and digital block externally.

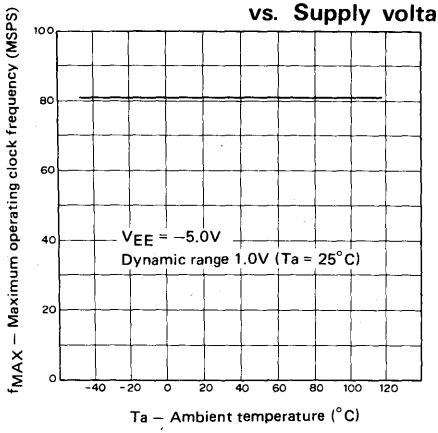
(2) Take as much space as possible of the ground surface on the printed board to reduce parasitic inductance and resistance.

(3) Insert a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor in parallel between the V_{EE} surface and the ground surface most adjacent to it on the printed board and reduce the noise. In addition, it is also desired to insert a capacitor between the V_{EE} surface and the GND surface near the IC. (See Fig. below)

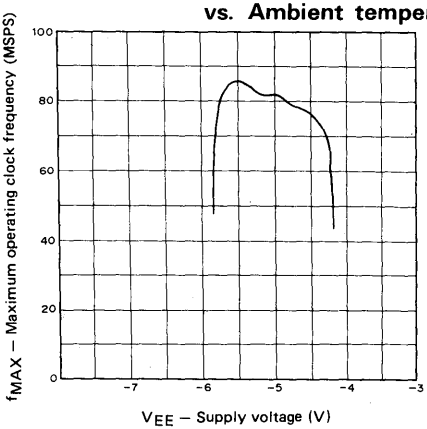
GND and V_{EE} pattern arrangement



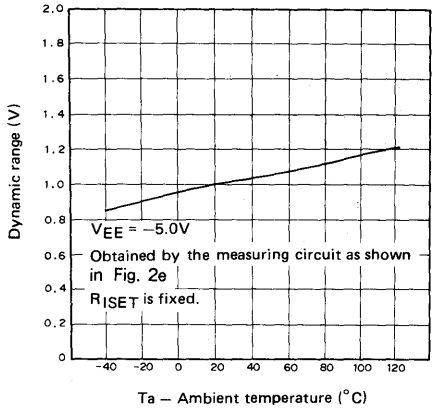
Maximum operating clock frequency vs. Supply voltage



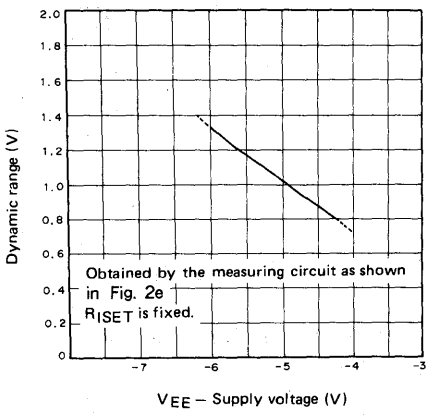
Maximum operating clock frequency vs. Ambient temperature



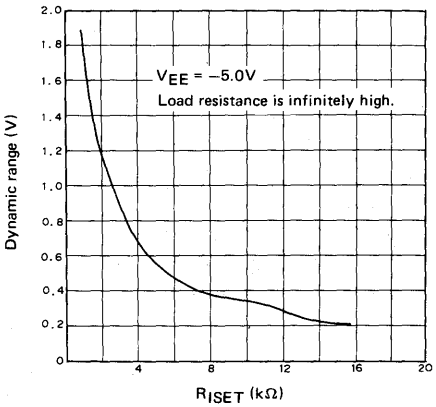
Dynamic range vs. Ambient temperature



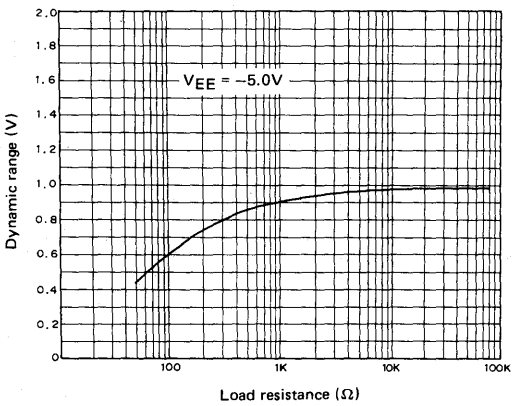
Dynamic range vs. Supply voltage



Dynamic range vs. RISET



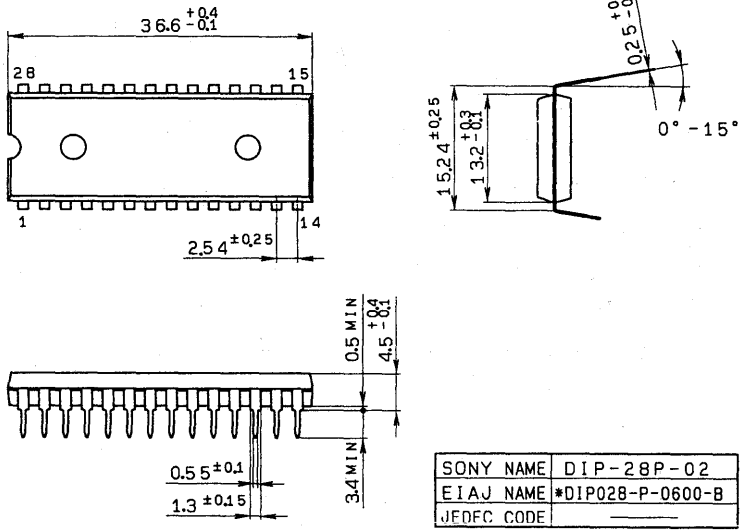
Dynamic range vs. Load resistance



5

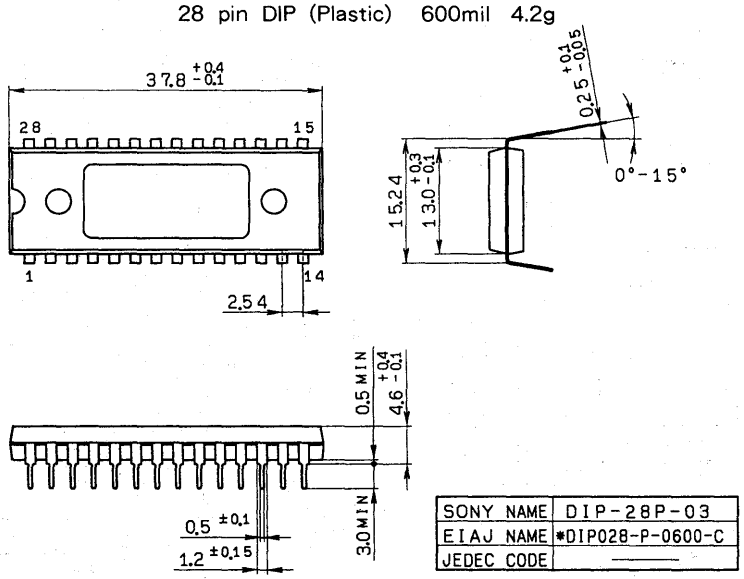
Package Outline Unit : mm

28 pin DIP (Plastic) 600mil 4.0g



SONY NAME	DIP-28P-02
EIAJ NAME	*DIP028-P-0600-B
JEDEC CODE	———

28 pin DIP (Plastic) 600mil 4.2g



SONY NAME	DIP-28P-03
EIAJ NAME	*DIP028-P-0600-C
JEDEC CODE	———

SONY

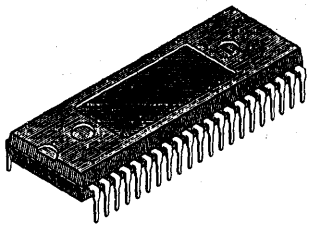
CX20206

8 bit 35 MSPS RGB 3-Channel D/A Converter (TTL input)

Description

CX20206 is an 8 bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

42 pin SDIP (Plastic)



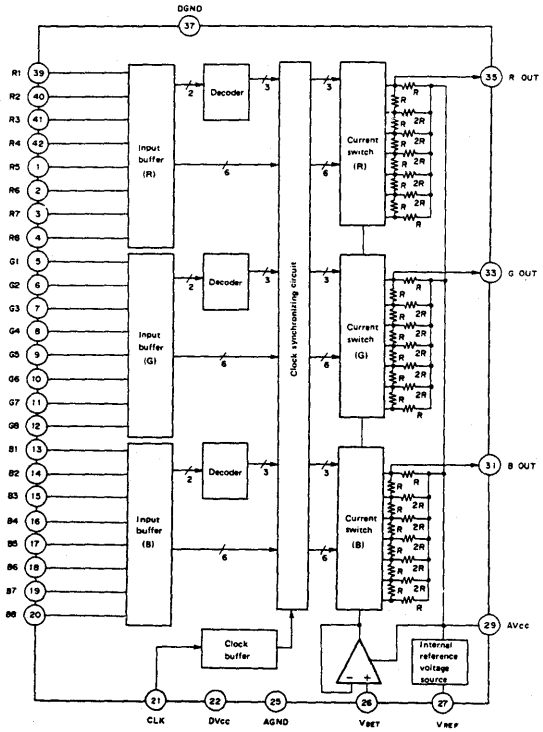
Features

- Resolution: 8 bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

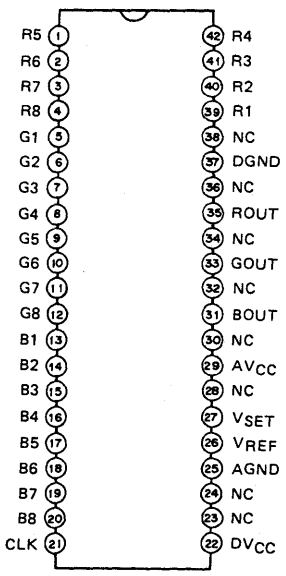
Structure

Bipolar silicon monolithic IC

Block Diagram



Pin Configuration (Top View)



E89638-ST

5

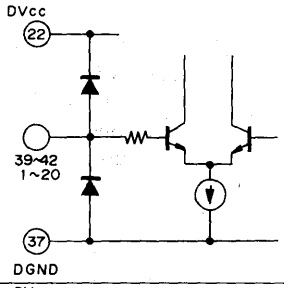
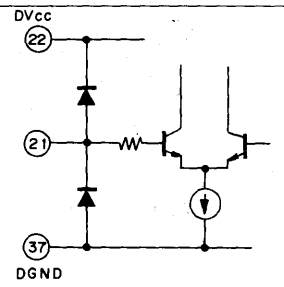
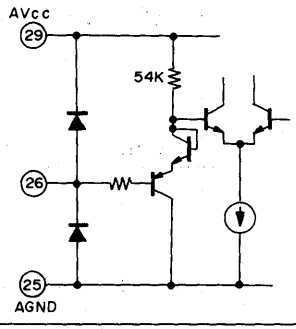
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	0 to 7	V
• Input voltage (digital)	V_I	−0.3 to V_{CC}	V
	V_{CLK}	−0.3 to V_{CC}	V
• Input voltage (V_{SET} pin)	V_{SET}	−0.3 to V_{CC}	V
• Output voltage (analog)	V_{OUT}	V_{CC}−2.1 to V_{CC}	V
• Output current (analog)	I_{OUT}	−3 to +10	mA
(V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.5	W

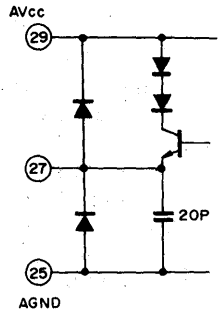
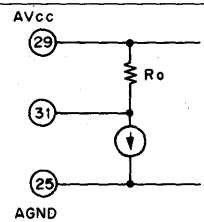
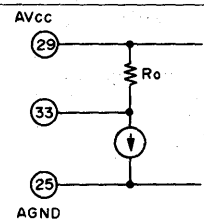
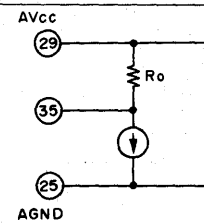
Recommended Operating Conditions

• Supply voltage	AV_{CC}, DV_{CC}	4.5 to 5.5	V
	AV_{CC}–DV_{CC}	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	V_{IH}, V_{CLKH}	2.0 to DV_{CC}	V
L level	V_{IL}, V_{CLKL}	DGND to 0.8	V
• V_{SET} input voltage	V_{SET}	0.7 to 0.9	V
• V_{REF} pin current	I_{REF}	−3 to −0.4	mA
• Clock pulse width	T_{pw1}	15	ns
	T_{pw0}	10	ns

Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 1 to 20	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 1 to 4 are for RED. R1 is MSB and R8 is LSB. From pins 5 to 12 are for GREEN. G1 is MSB and G8 is LSB. From pins 13 to 20 are for BLUE. B1 is MSB and B8 is LSB.
21	CLK		Clock input pin.
22	DVcc		Digital Vcc.
23 24	NC		Vacant pin (non-connection)
25	AGND		Analog GND.
26	VSET		Bias input pin. Normally, apply 0.8V. See "Note on use".

5

No.	Symbol	Equivalent circuit	Description
27	VREF		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use".
28	NC		Vacant pin (non-connection)
29	AVcc		Analog Vcc
30	NC		Vacant pin but connect to AVcc*
31	BOUT		Analog output pin for BLUE.
32	NC		Vacant pin but connect to AVcc*
33	GOUT		Analog output pin for GREEN.
34	NC		Vacant pin but connect to AVcc*
35	ROUT		Analog output pin for RED.
36	NC		Vacant pin but connect to AVcc*
37	DGND		Digital GND
38	NC		Vacant pin (non-connection)

*: Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics (Ta=25°C, AVCC=DVCC=5.0V, AGND=DGND=0.0V)

Item			Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	VSET−AGND=0.8V RL>10kΩ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			fMAX	VSET−AGND=0.8V RL>10kΩ CL<20pF	35			MSPS
Full-scale output voltage(note 1)			VOFS		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio(note 2)			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			RO		270	340	420	Ω
Consumption current			ID	VSET−AGND=0.8V RL>10kΩ IREF=−400μA	54	72	90	mA
Digital data input current	H level	Upper 2 bits	IIH(U)	VI=DVCC		1.2	20	μA
		Lower 6 bits	IIH(L)			0.6	10	μA
	L level	Upper 2 bits	IIL(U)	VI=DGND	−10	0	10	μA
		Lower 6 bits	IIL(L)		−10	0	10	μA
Clock input current		H level	ICLKH	VCLK=DVCC		3	30	μA
		L level	ICLKL	VCLK=DGND	−10	0	10	μA
VSET input current			ISET	VSET−AGND=0.8V	−5	−0.3	0	μA
Internal reference voltage			VREF	IREF=−400μA	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

(Note 1) AVCC−VO

(Note 2) Maximum value among

$$100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|,\ 100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|,\ \text{or}\ 100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$$

5

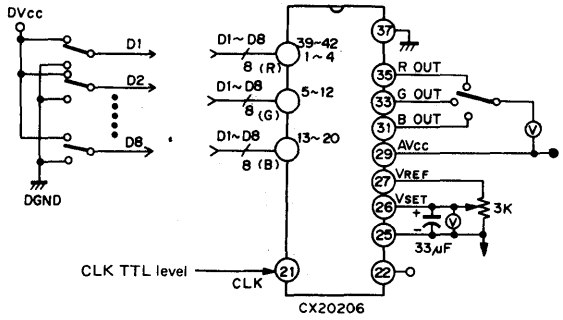
Input corresponding table

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	Vcc+Voffset
.	.
.	.
.	.
1 0 0 0 0 0 0 0	Vcc+Voffset−0.5V
.	.
.	.
.	.
0 0 0 0 0 0 0 0	Vcc+Voffset−1.0V

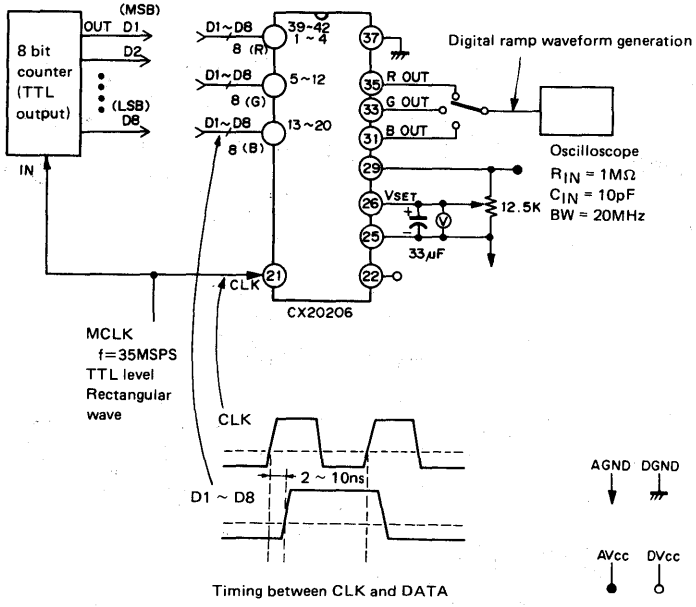
In case the output voltage full-scale is 1.00V. (1 LSB=3.92 mV)

Electrical Characteristics Measuring Circuit

Differential linearity and integral linearity measuring circuits



Maximum conversion speed measuring circuit



5

Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage measuring circuits

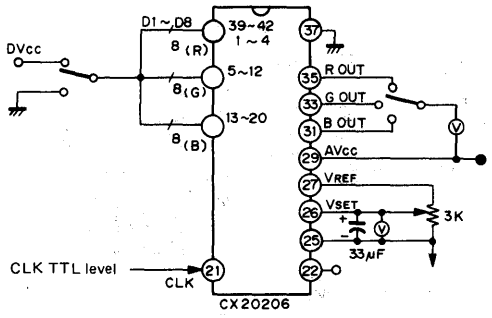
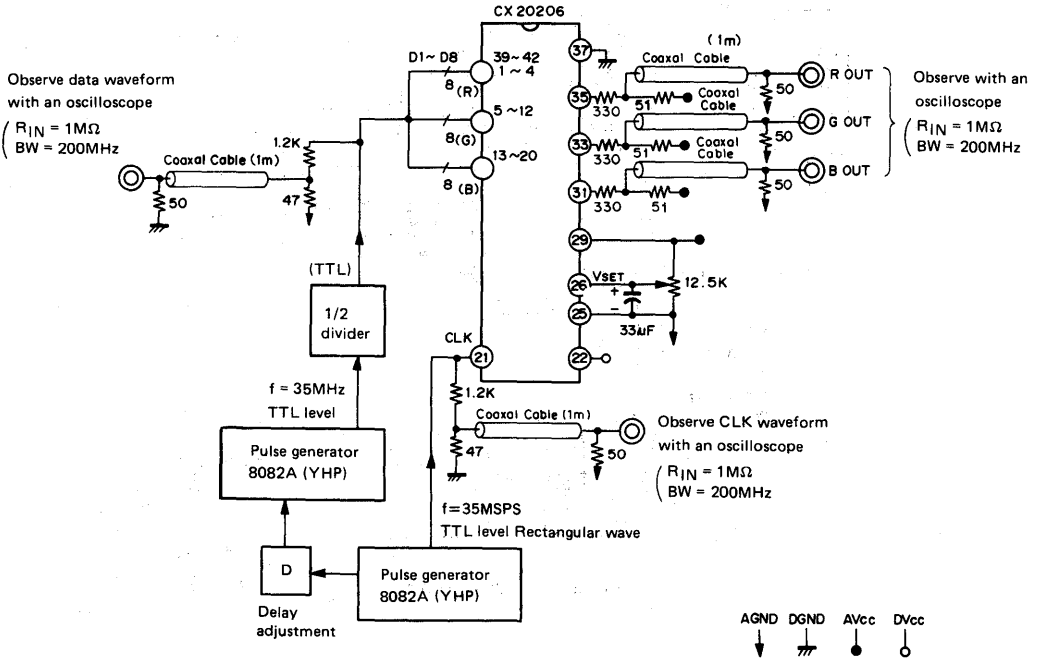


Fig. 1

Set-up time, hold time, and rise and fall time measuring circuits



Standard Circuit Design Data (Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V)

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p R_L>10kΩ C_L<20pF f_{DATA}=7MHz f_{CLK}=14MSPS See Fig.2		−40	−33	dB
Glitch energy	GE	V_{SET}−AGND=0.8V R_L>10kΩ f_{CLK}=1MSPS Digital ramp output See Fig.3(note 1)		160		pV-s
Rise time(note 2)	tr	V_{SET}−AGND=0.8V See Fig. 1.		5.5		ns
Fall time(note 2)	tf			5.0		ns
Settling time	tset			16		ns

(Note 1) Observe the glitch which is generated when the digital input varies as follows:

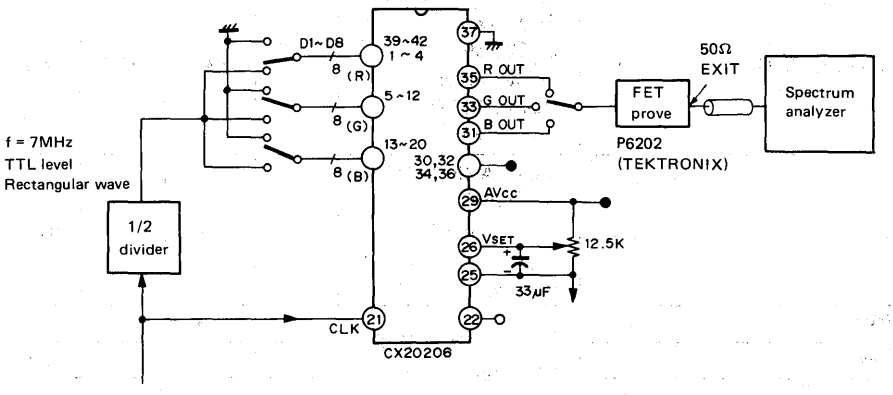
0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0

(Note 2) The time required for the D/A OUT to arrive at 90% of its final value from 10%.

5

Standard Circuit Design Data Measuring Circuit

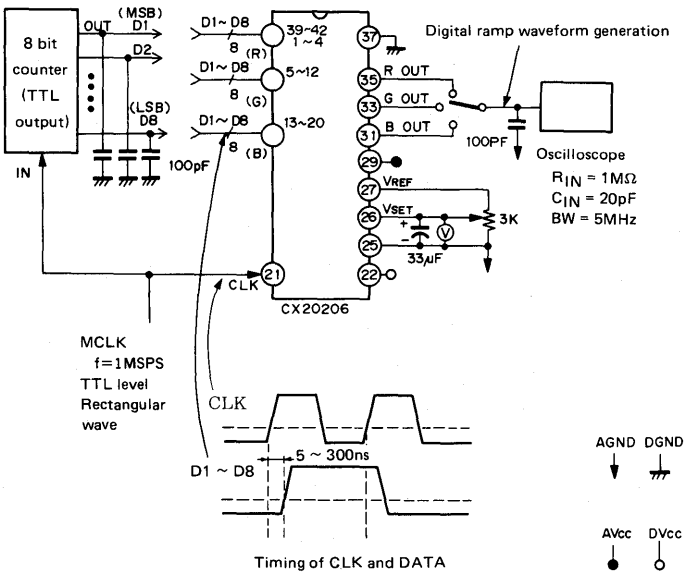
Fig. 2 Crosstalk among R, G and B measuring circuit



[Measuring method]
In case the measuring crosstalk of G → R

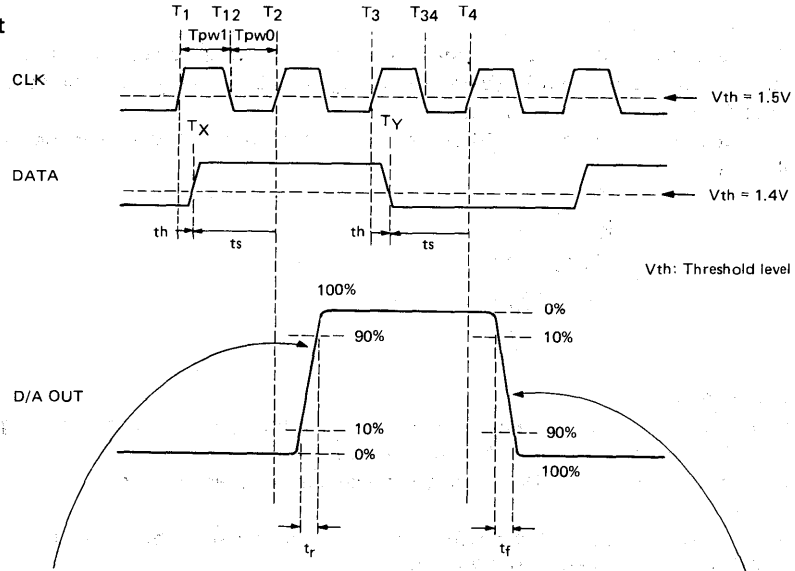
1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.
2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.
3 Take the difference of the above two powers. The unit is in dB.

Fig. 3 Glitch energy measuring circuit



Operation Description

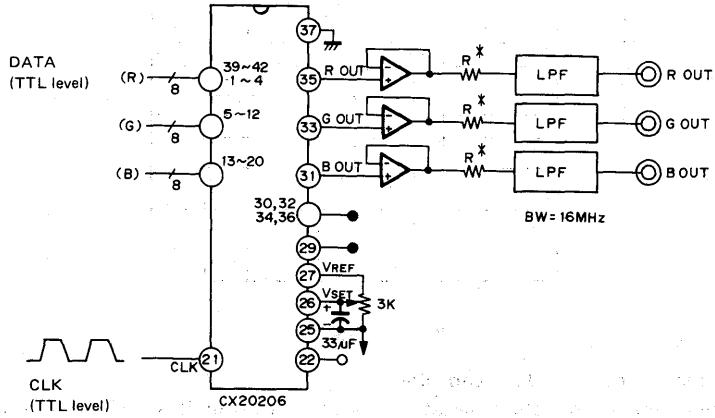
Timing chart



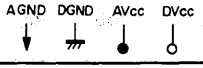
At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_4)).

Applied Circuit Example



R* is matching resistance for LPF



5

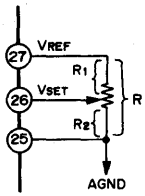
Note on Use

(1) Setting of pin 26 (V_{SET})

The full-scale of the D/A output voltage changes by applying voltage to pin 26 (V_{SET}). When load is connected to pin 27 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.8V by resistance division.

When the 0.8V is applied to pin 26 (V_{SET}), the D/A output of 1 Vp-p can be obtained.

(Example of use)

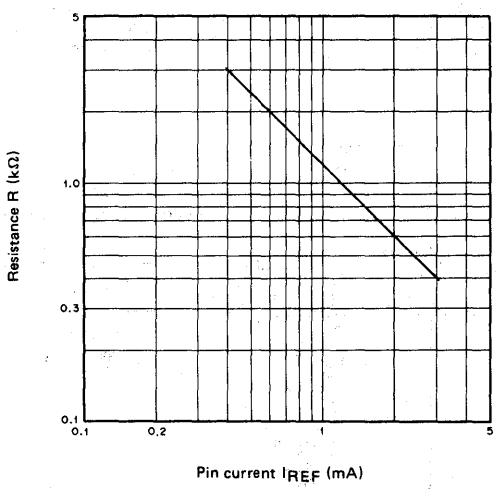


(Adjustment method)

1 The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
$R = V_{REF}/I_{REF}$

2 Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
(At this point, it becomes R1:R2=1:2)

Fig. 4 Resistance vs. V_{REF} pin current



(2) Phase relationship between data and clock

In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.

Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

(3) Regarding the load of D/A output pin

Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:

$R_L > 10\ k\Omega$

$C_L < 20\ pF$

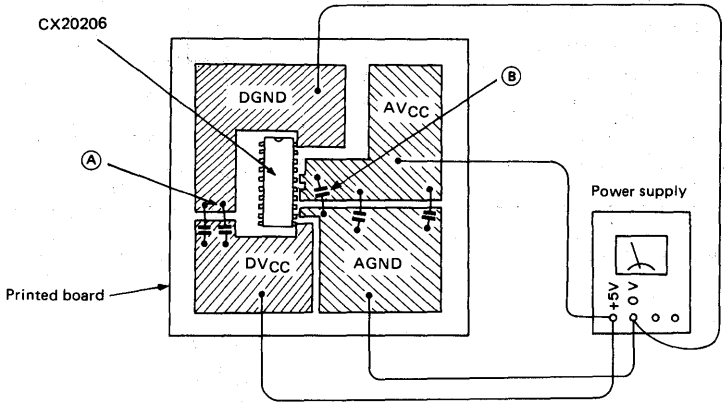
The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20\ pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

(4) Noise reduction measures

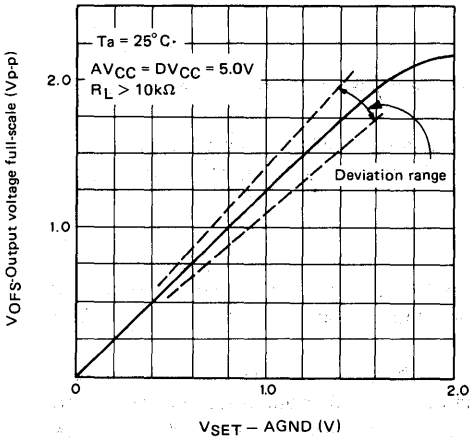
As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.

- When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC}. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the V_{CC} surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 25 (AGND) and pin 26 (V_{SET}).

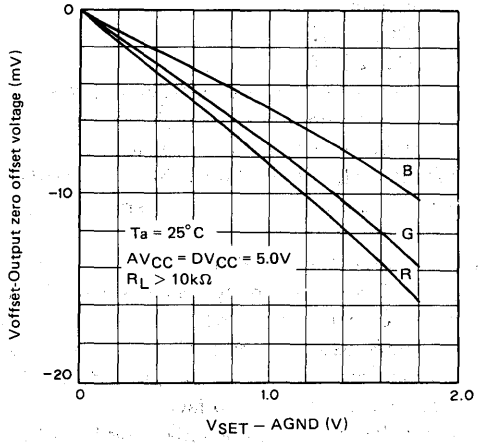


5

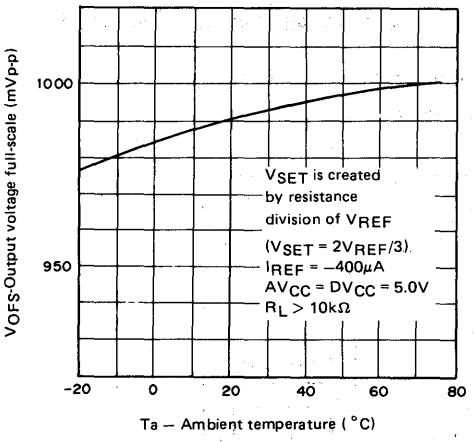
Output voltage full-scale vs. V_{SET}—AGND



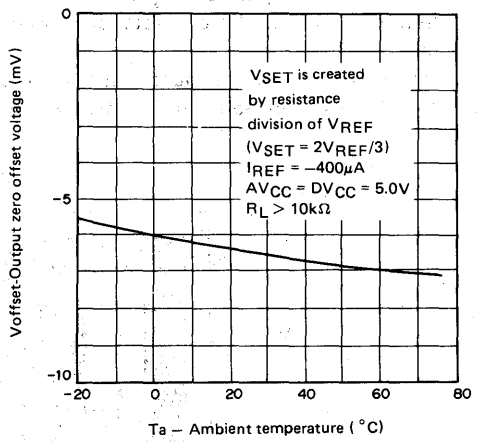
Output zero offset voltage vs. V_{SET}—AGND



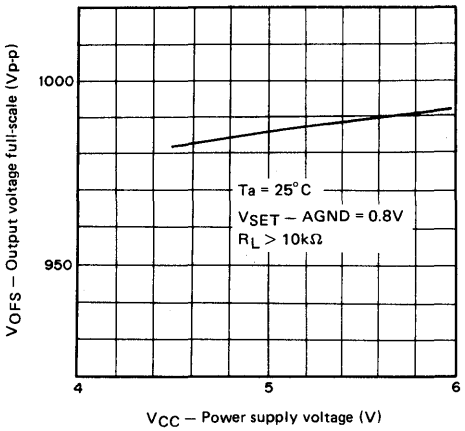
Output voltage full-scale vs. Ambient temperature



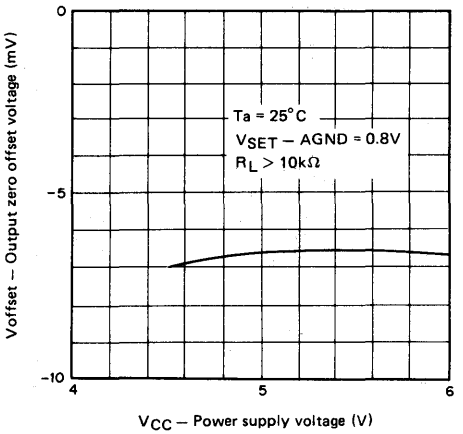
Output zero offset voltage vs. Ambient temperature



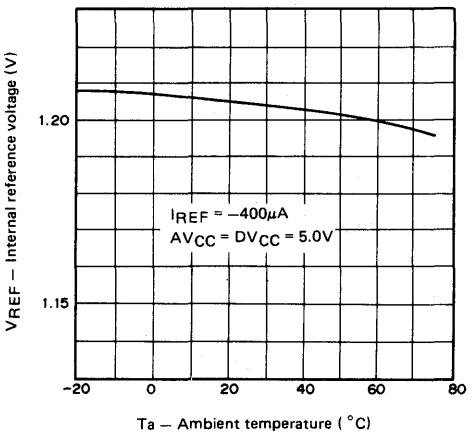
Output voltage full-scale vs. Power supply voltage



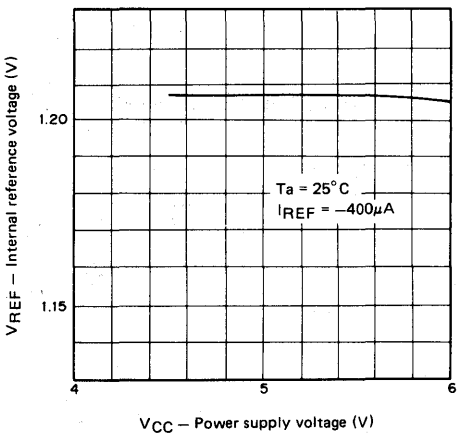
Output zero offset voltage vs. Power supply voltage



Internal reference voltage vs. Ambient temperature

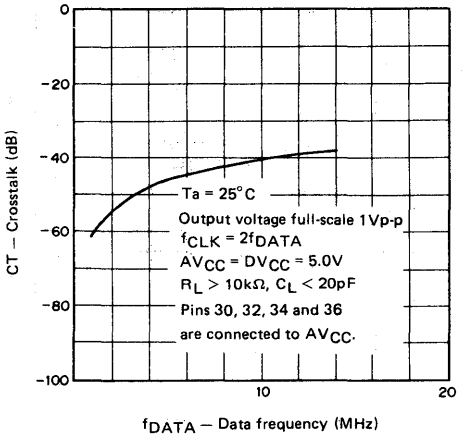


Internal reference voltage vs. Power supply voltage



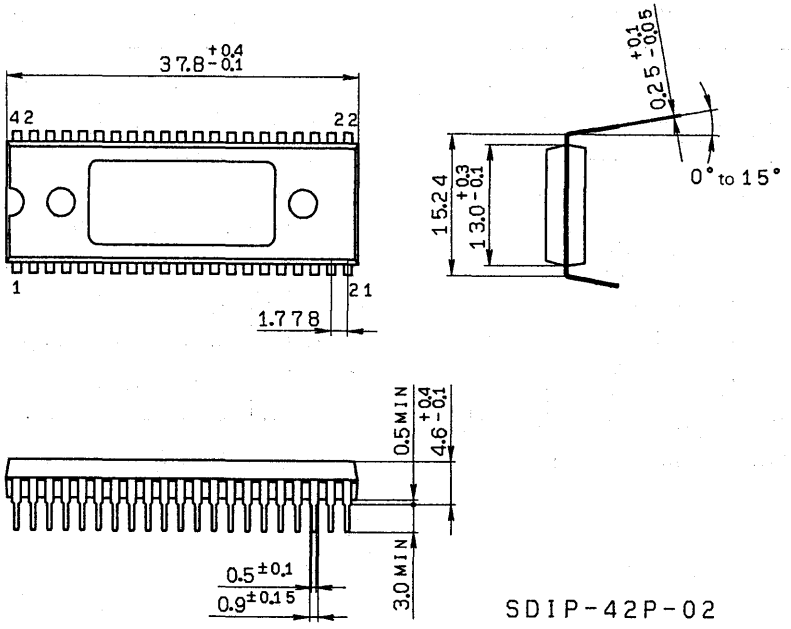
5

Crosstalk among R, G and B vs. Data frequency



Package Outline **Unit: mm**

42 pin SDIP (Plastic) 600 mil 4.4g



SONY®

CXA1260Q-Z

8 bit 35 MSPS RGB 3-Channel D/A Converter (TTL input)

Description

CXA1260Q-Z is an 8-bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

48 pin QFP (Plastic)

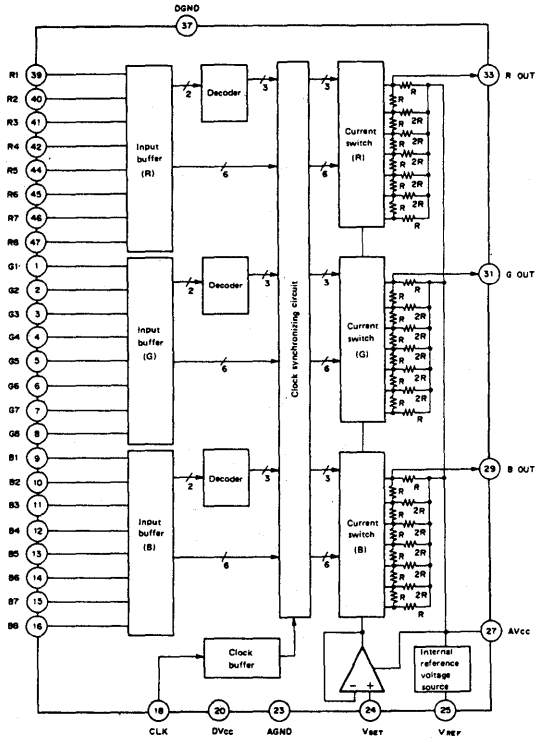
Features

- Resolution: 8-bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

Structure

Bipolar silicon monolithic IC

Block Diagram



E89648-ST

5

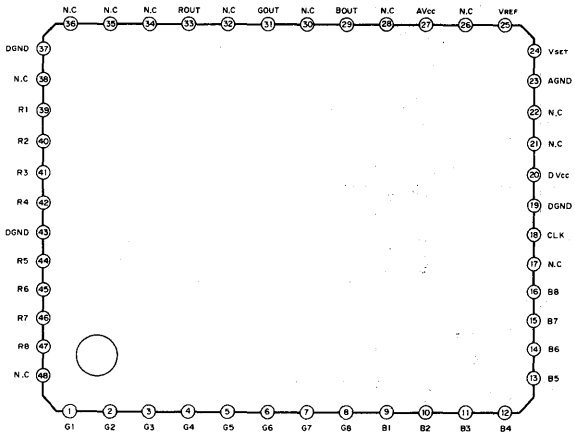
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	0 to 7	V
• Input voltage (digital)	V_I	−0.3 to V_{CC}	V
	V_{CLK}	−0.3 to V_{CC}	V
• Input voltage (V_{SET} pin)	V_{SET}	−0.3 to V_{CC}	V
• Output voltage (analog)	V_{OUT}	V_{CC}−2.1 to V_{CC}	V
• Output current (analog)	I_{OUT}	−3 to +10	mA
(V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.7	W

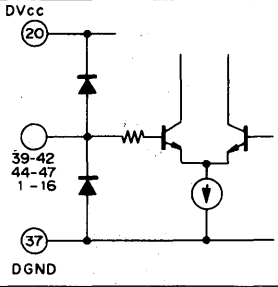
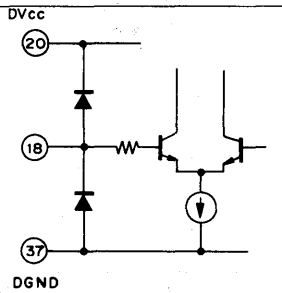
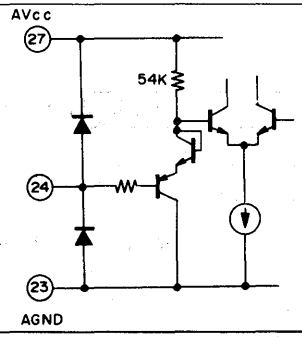
Recommended Operating Conditions

• Supply voltage	AV_{CC}, DV_{CC}	4.5 to 5.5	V
	AV_{CC}–DV_{CC}	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	V_{IH}, V_{CLKH}	2.0 to DV_{CC}	V
L level	V_{IL}, V_{CLKL}	DGND to 0.8	V
• V_{SET} input voltage	V_{SET}	0.7 to 1.0	V
• V_{REF} pin current	I_{REF}	−3 to −0.4	mA
• Clock pulse width	T_{pw1}	15	ns
	T_{pw0}	10	ns

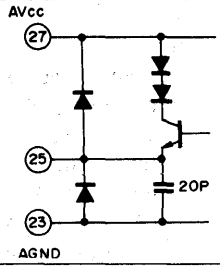
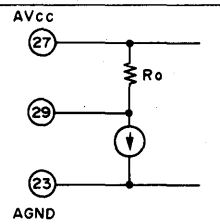
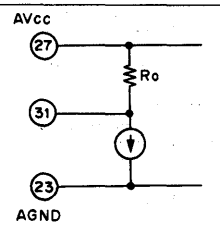
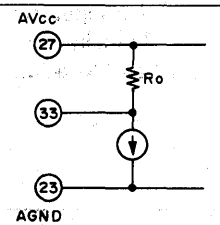
Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 44 to 47 1 to 16	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 44 to 47 are for RED. R1 is MSB and R8 is LSB. From pins 1 to 8 are for GREEN. G1 is MSB and G8 is LSB. From pins 9 to 16 are for BLUE. B1 is MSB and B8 is LSB.
18	CLK		Clock input pin.
20	DVcc		Digital Vcc.
17 21 to 22	NC		Vacant pin (non-connection)
23	AGND		Analog GND.
24	VSET		Bias input pin. Normally, apply 0.87V. See "Note on use".

5

No.	Symbol	Equivalent circuit	Description
25	V_{REF}		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use".
26	NC		Vacant pin (non-connection)
27	AVcc		Analog Vcc
28	NC		Vacant pin but connect to AVcc*
29	BOUT		Analog output pin for BLUE.
30	NC		Vacant pin but connect to AVcc*
31	GOUT		Analog output pin for GREEN.
32	NC		Vacant pin but connect to AVcc*
33	ROUT		Analog output pin for RED.
34 to 36	NC		Vacant pin but connect to AVcc*
19 37 43	DGND		Digital GND
48	NC		Vacant pin (non-connection)

***Note)** Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics

Ta=25°C, AVcc=DVcc=5.0V, AGND=DGND=0.0V

Item			Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	V_{SET}−AGND=0.87V R_L>10kΩ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			f_{MAX}	V_{SET}−AGND=0.87V R_L>10kΩ C_L<20pF	35			MSPS
Full-scale output voltage*1			V_{OFS}		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio*2			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			R_O		270	340	420	Ω
Consumption current			I_D	V_{SET}−AGND=0.87V R_L>10kΩ I_{REF}=−400μA	54	72	90	mA
Digital data input current	H level	Upper 2 bits	$I_{IH(U)}$	V_I=DVcc		1.2	20	μA
		Lower 6 bits	$I_{IH(L)}$			0.6	10	μA
	L level	Upper 2 bits	$I_{IL(U)}$	V_I=DGND	−10	0	10	μA
		Lower 6 bits	$I_{IL(L)}$		−10	0	10	μA
Clock input current		H level	I_{CLKH}	V_{CLK}=DVcc		3	30	μA
		L level	I_{CLKL}	V_{CLK}=DGND	−10	0	10	μA
V_{SET} input current			I_{SET}	V_{SET}−AGND=0.87V	−5	−0.3	0	μA
Internal reference voltage			V_{REF}	I_{REF}=−400μA	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

Note) *1. AVcc−Vo

*2. Maximum value among

$$100 \times \left|\frac{V_{OFS(R)}}{V_{OFS(G)}} - 1\right|,\ 100 \times \left|\frac{V_{OFS(G)}}{V_{OFS(B)}} - 1\right|,\ \text{or}\ 100 \times \left|\frac{V_{OFS(B)}}{V_{OFS(R)}} - 1\right|$$

5

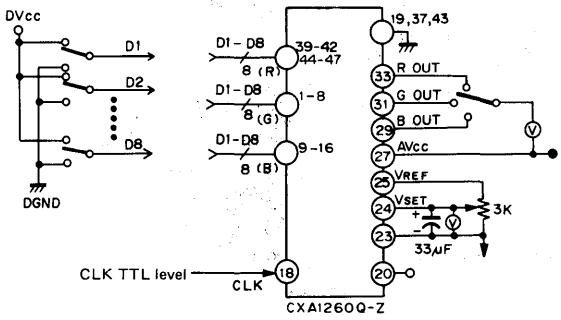
Input corresponding table

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	Vcc+Voffset
.	.
.	.
.	.
1 0 0 0 0 0 0 0	Vcc+Voffset−0.5V
.	.
.	.
.	.
0 0 0 0 0 0 0 0	Vcc+Voffset−1.0V

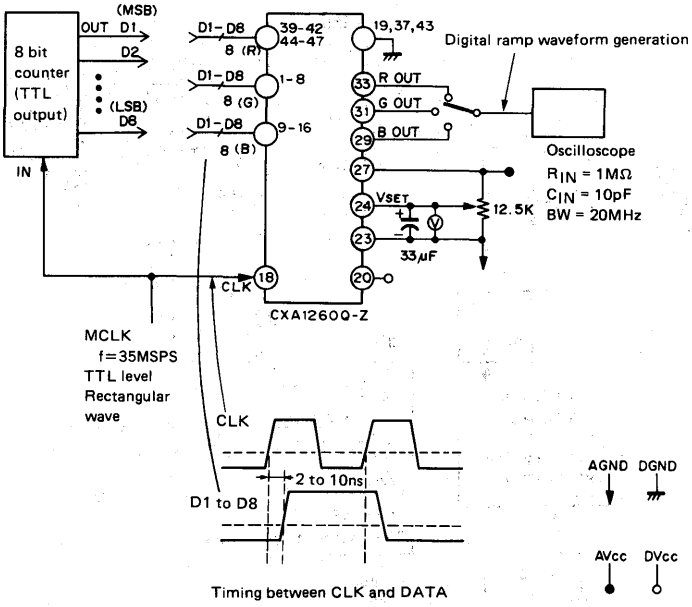
In case the output voltage full-scale is 1.00V. (1LSB=3.92 mV)

Electrical Characteristics Test Circuit

Differential linearity and integral linearity test circuits



Maximum conversion speed test circuit



5

Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage test circuits

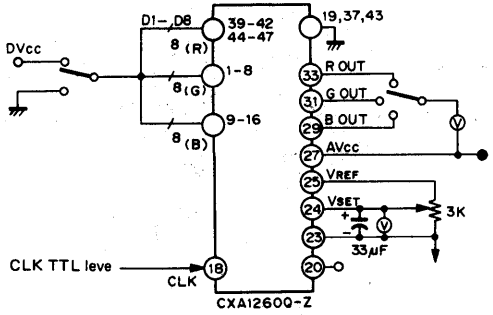
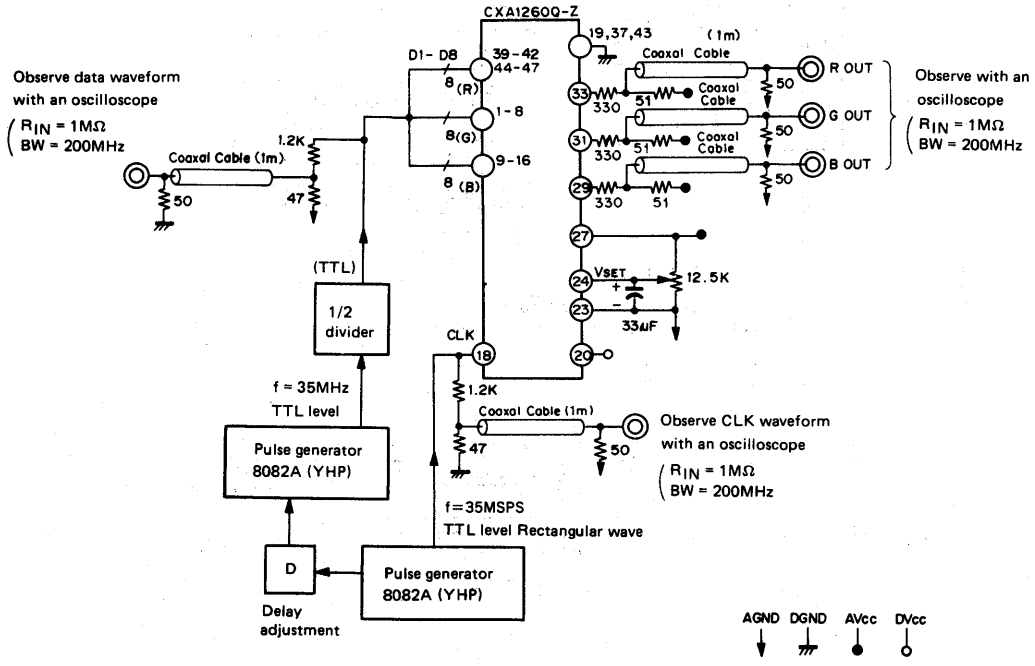


Fig. 1

Set-up time, hold time, and rise and fall time test circuits



Standard Circuit Design Data Ta=25°C, AVCC=DVCC=5.0V, AGND=DGND=0.0V

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p RL>10kΩ CL<20pF fDATA=7MHz fCLK=14MSPS See Fig.2		−40	−35	dB
Glitch energy	GE	VSET−AGND=0.87V RL>10kΩ fCLK=1MSPS Digital ramp output See Fig.3*1		30		pV-s
Rise time*2	tr	VSET−AGND=0.87V See Fig. 1.		5.5		ns
Fall time*2	tf			5.0		ns
Settling time	tset			16		ns

Note) *1. Observe the glitch which is generated when the digital input varies as follows:

0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0

*2. The time required for the D/A OUT to arrive at 90% of its final value from 10%.

5

Standard Circuit Design Data Test Circuit

Crosstalk among R, G and B test circuit

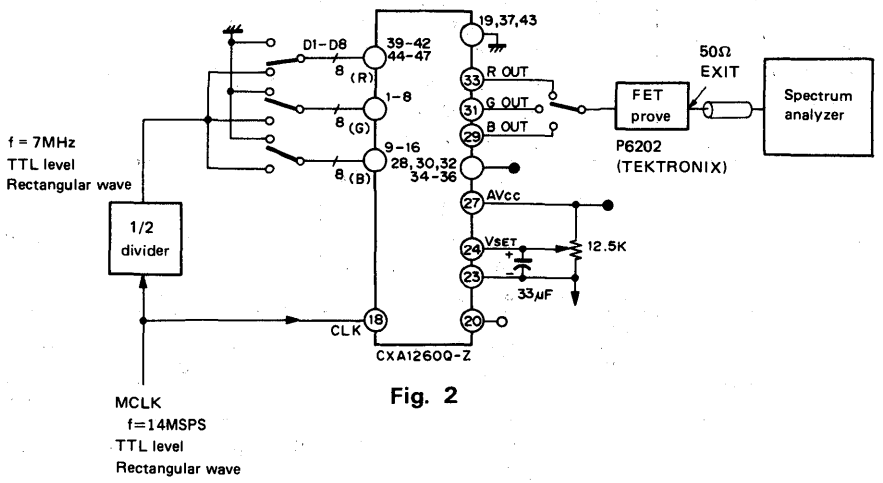
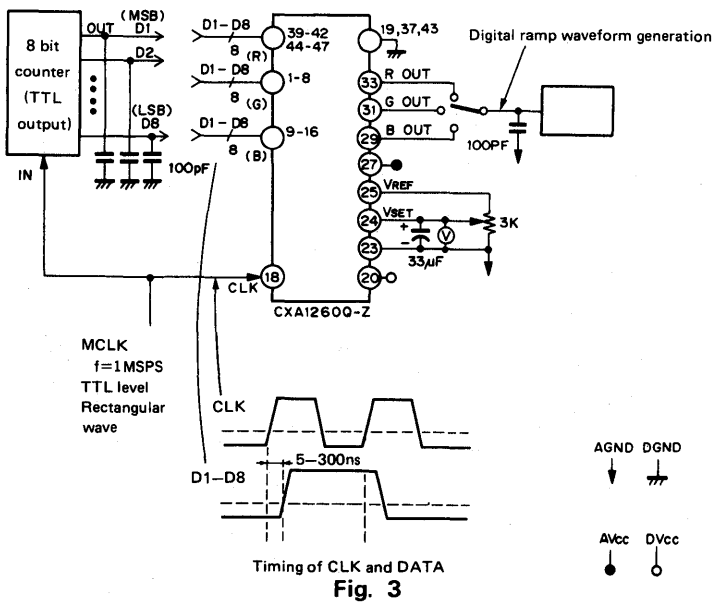


Fig. 2

[Measuring method]
In case the measuring crosstalk of G → R

1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.
2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.
3 Take the difference of the above two powers. The unit is in dB.

Glitch energy test circuit

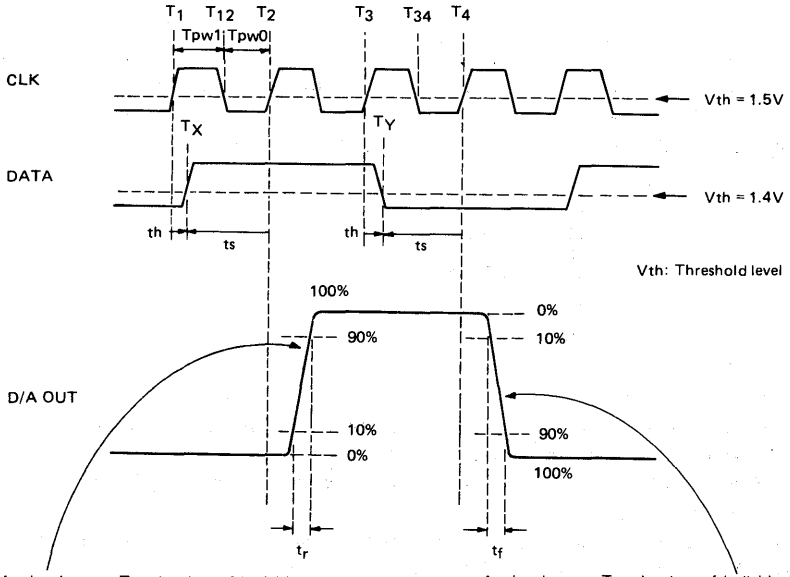


Timing of CLK and DATA

Fig. 3

Operation Description

Timing chart

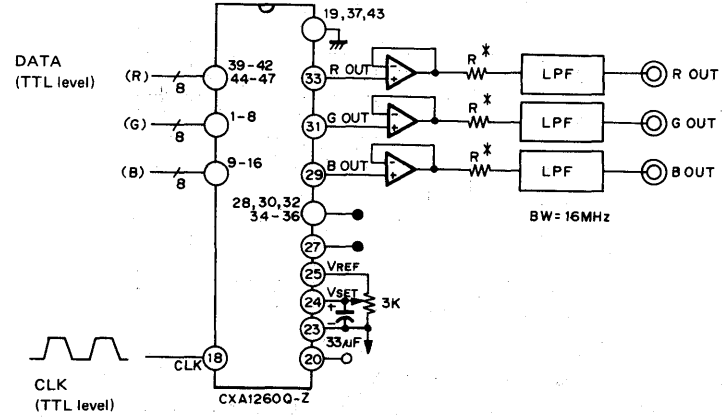


At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

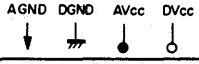
At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t=T_4)).

5

Application Circuit

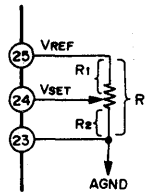


R* is matching resistance for LPF



Note on Use

1. Setting of pin 24 (V_{SET})
   The full-scale of the D/A output voltage changes by applying voltage to pin 24 (V_{SET}). When load is connected to pin 25 (V_{REF}), DC volatage of 1.2V is issued and the said voltage is dropped to 0.87V by resistance division.
   When the 0.87V is applied to pin 24 (V_{SET}), the D/A output of 1 Vp-p can be obtained.
   (Example of use)



   Adjustment method
   1) The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
      See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
      $R = V_{REF}/I_{REF}$
   2) Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
      (At this point, it becomes R1:R2=2:5)

Resistance vs. V_{REF} pin current

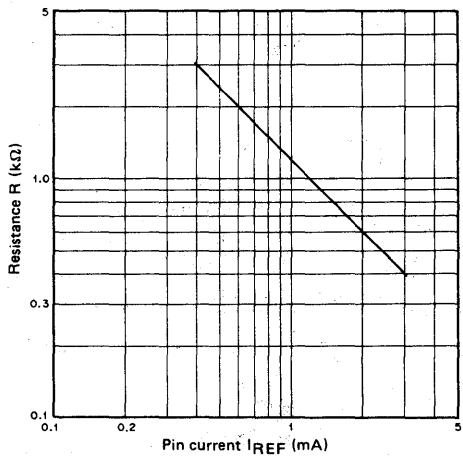
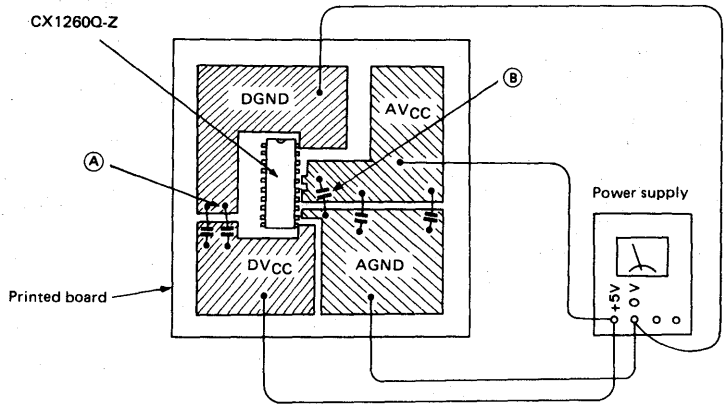


Fig. 4

2. Phase relationship between data and clock
   In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.
   Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.
   Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

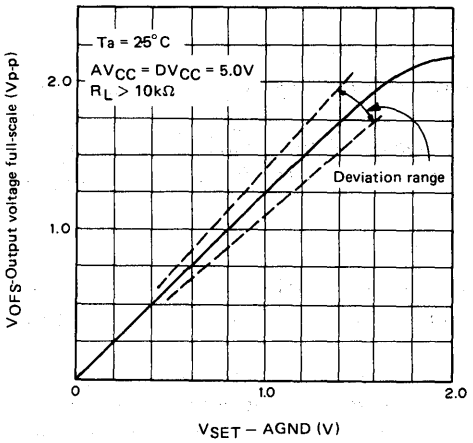
3. Regarding the load of D/A output pin
Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:
$R_L > 10\ k\Omega$
$C_L < 20\ pF$
The temperature characteristics indicated in the characteristics diagram has been measured under this condition.
However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20\ pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

4. Noise reduction measures
As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.
- When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC}. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the V_{CC} surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 23 (AGND) and pin 24 (V_{SET}).

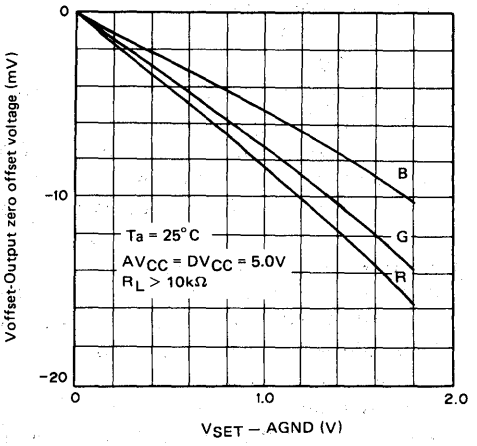


5

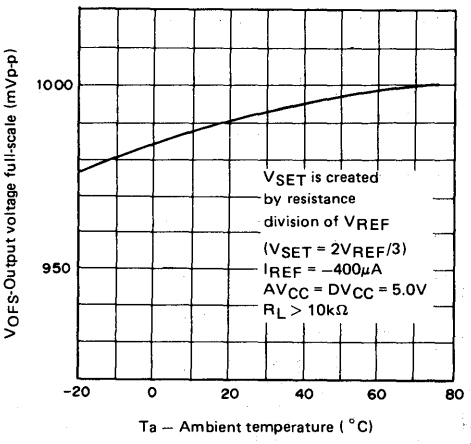
Output voltage full-scale vs. VSET—AGND



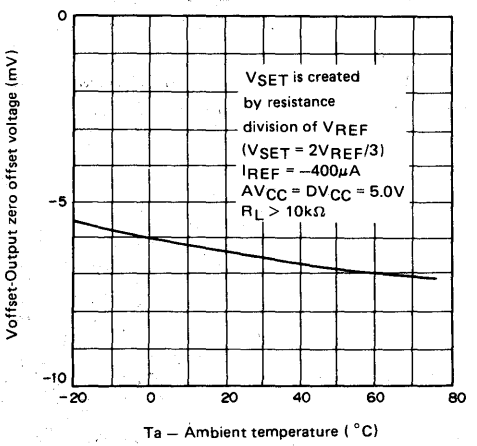
Output zero offset voltage vs. VSET—AGND



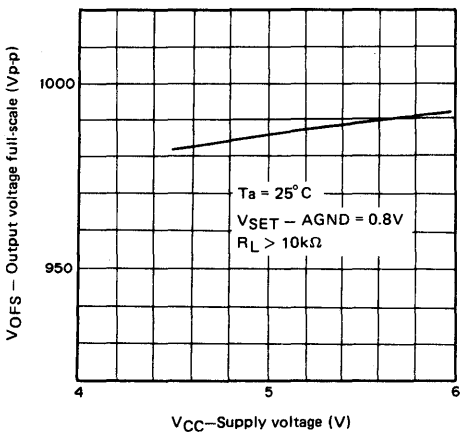
Output voltage full-scale vs. Ambient temperature



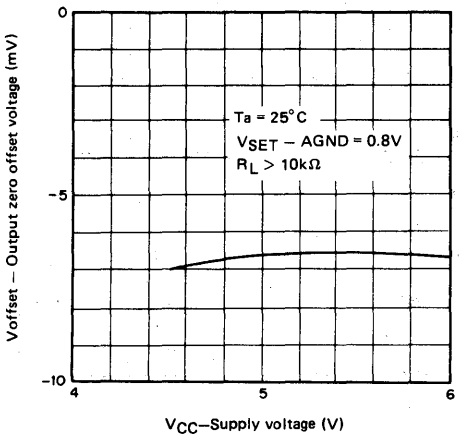
Output zero offset voltage vs. Ambient temperature



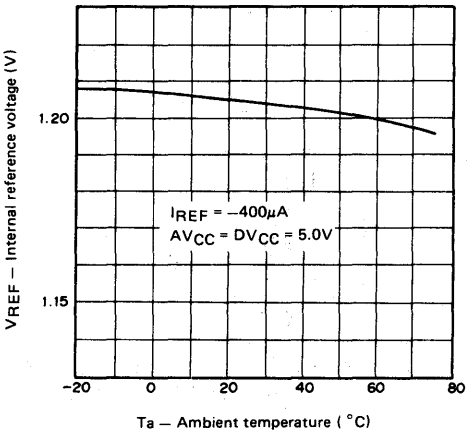
Output voltage full-scale vs. Supply voltage



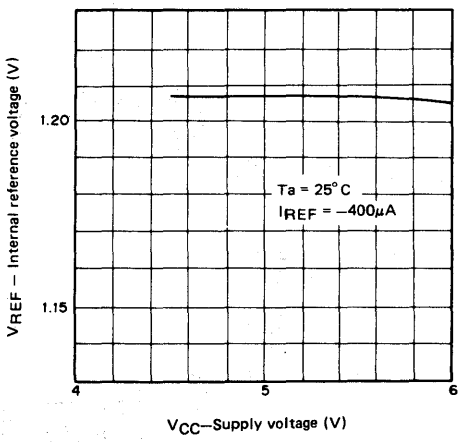
Output zero offset voltage vs. Supply voltage



Internal reference voltage vs. Ambient temperature

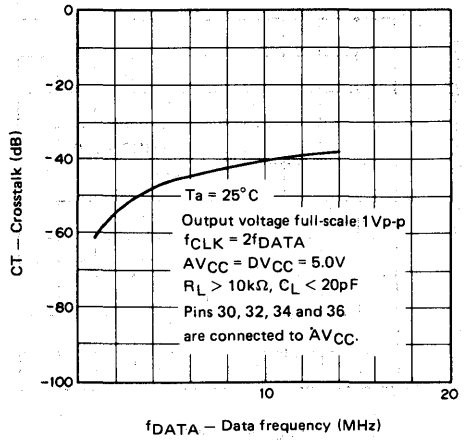


Internal reference voltage vs. Supply voltage



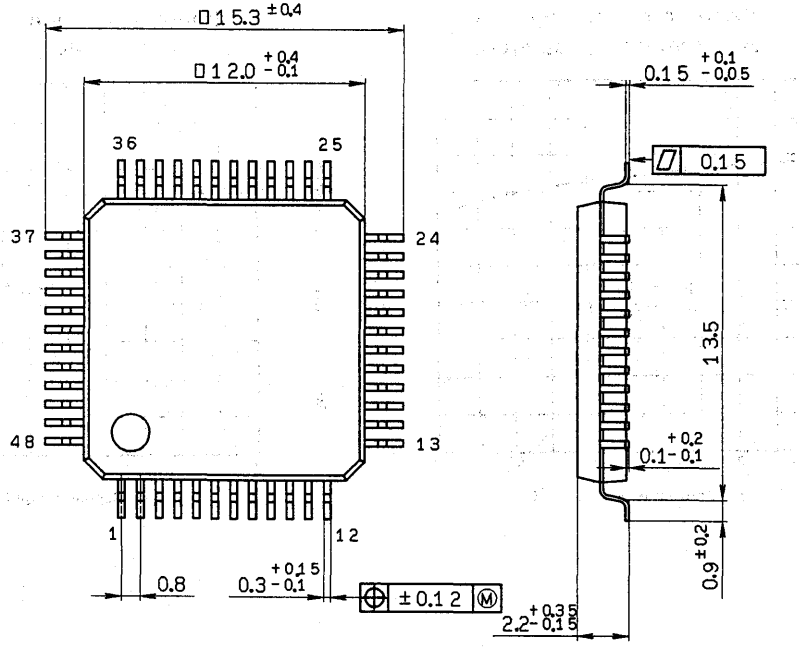
5

Crosstalk among R, G and B vs. Data frequency



Package Outline **Unit: mm**

48 pin QFP (Plastic) 0.6g



QFP-48P-L04

SONY

CXA1106P/M

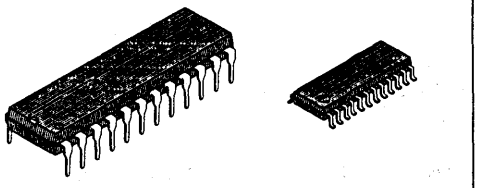
8-bit 35 MSPS High-Speed D/A Converter (TTL input)

Description

CXA1106P/M is an 8-bit 35MSPS high-speed D/A converter IC. Summing type current for the upper 2-bits and ladder type resistance for the lower 6-bits, ensure a low power consumption of 200 mW (Single power supply).
This IC is suitable for digital TV's, graphic displays and other applications.

CXA1106P
24 pin DIP (Plastic)

CXA1106M
24 pin SOP (Plastic)



Features

- Resolution 8-bit
- High speed operation
  35MSPS (Max. conversion speed)
- Non linear error
  less than ±1/2LSB
- Low glitch
- TTL compatible input
- +5V single power supply or ±5V dual power supply
- Low power consumption

+5V single power supply	200 mW (Typ.)
±5V dual power supply	400 mW (Typ.)

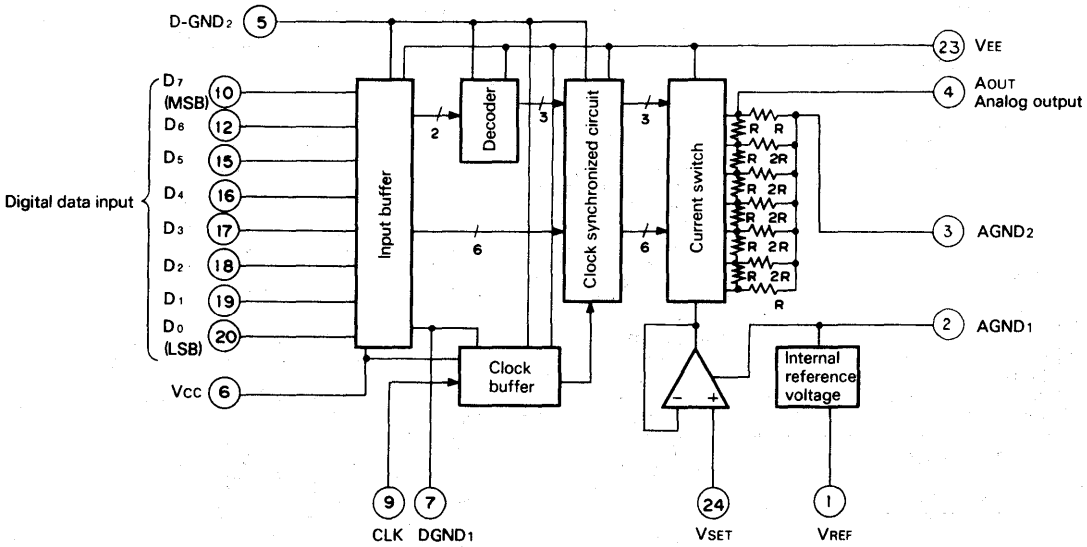
Function

8-bit 35 MSPS D/A converter

Structure

Bipolar silicon monolithic IC

Block Diagram



E89675 – ST

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}-DGND1	0 to 6	V
	V_{EE} – AGND1,2	−6 to 0	V
	DGND2 – DGND1	0 to 6	V
• Digital input voltage	V_I	DGND1 − 0.3 to V_{CC} + 0.3	V
	V_{CLK}	DGND1 − 0.3 to V_{CC} + 0.3	V
• Input voltage (V_{SET} pin)	V_{SET}	V_{EE} − 0.3 to V_{EE} + 2.7	V
• Output current (V_{REF} pin)	I_{REF}	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	1.27	W

Recommended Operating Conditions

Single power supply

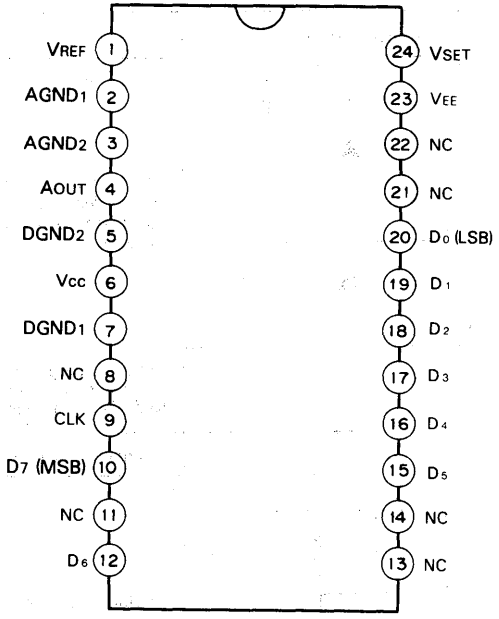
Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}, DGND2 AGND1, AGND2	4.75	5.00	5.25	V
		DGND2 – AGND1 DGND2 – AGND2	−0.2	0	0.2	V
		AGND1 – AGND2	−0.1	0	0.1	V
Digital input voltage	H level	V_{IH}, V_{CLKH}	2.0		VCC	V
	L level	V_{IL}, V_{CLKL}	DGND1		1.0	V
V_{SET} input voltage		V_{SET}	0.70	0.84	1.0	V
V_{REF} pin current		I_{REF}	−3.0		−0.4	mA
Clock pulse width*		T_{PW1}	10			ns
		T_{PW0}	10			ns

***Note)** See Fig. 6. Timing chart

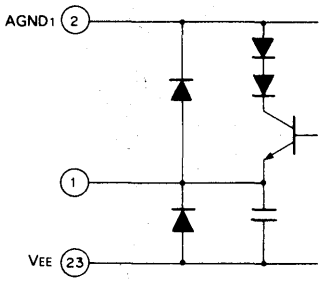
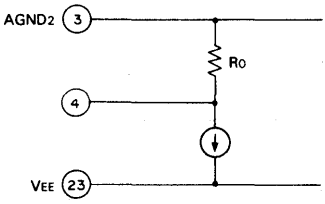
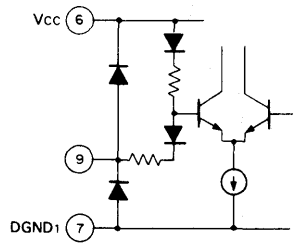
Dual power supply

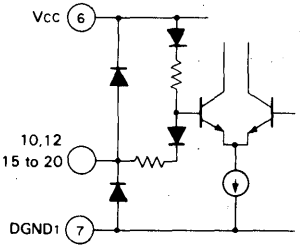
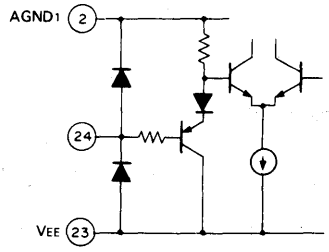
Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
		V_{EE}	−5.5	5.00	−4.75	V
		DGND2 – AGND1 DGND2 – AGND2	−0.2	0	−0.2	V
		AGND1 – AGND2	−0.1	0	0.1	V
Digital input voltage	H level	V_{IH}, V_{CLKH}	2.0		V_{CC}	V
	L level	V_{IL}, V_{CLKL}	DGND1		1.0	V
V_{SET} input voltage		V_{SET}	−4.30	−4.16	−4.00	V
V_{REF} pin current		I_{REF}	−3.0		−0.4	mA
Clock pulse width		T_{PW1}	10			ns
		T_{PW0}	10			ns

Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Description
1	V_{REF}		Internal reference voltage output pin 1.2 V (Typ.) An external pull down resistance is necessary. For reference see Notes on Application 1 on page 15.
2	$AGND_1$		Set to Analog V_{CC} for single power supply and to Analog GND for dual power supply. Connect to $AGND_2$ and use.
3	$AGND_2$		Connect to $AGND_1$
4	A_{OUT}		Analog output pin
5	$DGND_2$		Set to Digital V_{CC} for single power supply and to Digital GND for dual power supply.
6	V_{CC}		Digital V_{CC}
7	$DGND_1$		Digital GND
8	NC		Non-connection
9	CLK		Clock input pin

No.	Symbol	Equivalent circuit	Description
10, 12, 15 to 20	D7, D6, D5 to D0		Digital input pin D1 to MSB, D8 to LSB
11, 13, 14	NC		Non-connection
21, 22	NC		Non connection pin. But connect to AGND or VEE
23	VEE		Set to Analog GND for single power supply and to VEE for dual power supply.
24	VSET		Bias input pin Normally set VSET – VEE to 0.84V. For reference see Notes on Application 1.

See the Application Circuit for reference.

5

Electrical Characteristics (Ta = 25°C)

Single power supply

V_{CC} = DGND2 = AGND1 = AGND2 = 5V, DGND1 = V_{EE} = 0, V_{SET} = 0.84V

Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}	R_L > 10kΩ, C_L < 20pF	35			MSPS
Linearity error		E_L	R_L > 10 KΩ	−0.5		+0.5	LSB
Differential linear error		E_D		−0.5		+0.5	LSB
Full scale output voltage		V_{FS}	R_L > 10KΩ	0.9	1.0	1.1	V
Offset voltage*		V_{OS}	R_L > 10KΩ	0	4	10	mV
Output resistance		R_O		290	350	410	Ω
Power supply current		I_{CC}	R_L > 10KΩ I_{REF} = −400μA	32	40	48	mA
Digital input current	H level	I_{IH}		0		5	μA
	L level	I_{IL}		−400		0	μA
V_{SET} input current		I_{SET}		−3		0	μA
Internal reference output voltage		V_{REF}	I_{REF} = −400μA	1.17	1.25	1.33	V
Accuracy output voltage range		V_{OC}	R_L > 10KΩ	0.5	1.0	1.5	V
Set up time		t_s		10			ns
Hold time		t_h		2			ns
Propagation delay time		t_{PD}	R_L > 10KΩ		11		ns
Glitch energy		GE	R_L > 10KΩ f_{CLK} = 1 MHz Digital lamp output		30		pV-s

***Note)** V_{OS} = AGND2 − V_{255} (V_{255} is the output voltage when full input is at high level)

Dual power supply

V_{CC} = 5V, DGND1 = DGND2 = AGND1 = AGND2 = 0, V_{EE} = −5V, V_{SET} − V_{EE} = 0.84V

Item		Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}	R_L > 10kΩ, C_L < 20pF	35			MSPS
Linearity error		E_L	R_L > 10 KΩ	−0.5		+0.5	LSB
Differential linear error		E_D		−0.5		+0.5	LSB
Full scale output voltage		V_{FS}	R_L > 10KΩ	0.9	1.0	1.1	V
Offset voltage		V_{OS}	R_L > 10KΩ	0	4	10	mV
Output resistance		R_O		290	350	410	Ω
Power supply current		I_{CC}	R_L > 10KΩ I_{REF} = −400μA	24	30	36	mA
		I_{EE}		40	50	60	mA
Digital input current	H level	I_{IH}		0		5	μA
	L level	I_{IL}		−400		0	μA
V_{SET} input current		I_{SET}		−3		0	μA
Internal reference output voltage		V_{REF}	I_{REF} = −400μA	−3.83	−3.75	−3.67	V
Accuracy output voltage range		V_{OC}	R_L > 10KΩ	0.5	1.0	1.5	V
Set up time		t_s		10			ns
Hold time		t_h		2			ns
Propagation delay time		t_{PD}	R_L > 10KΩ		11		ns
Glitch energy		GE	R_L > 10KΩ f_{CLK} = 1 MHz Digital lamp output		30		pV-s

5

Input/Output Chart (when output full scale voltage at 1.00 V)

Table 1

Input code								Output voltage (Single supply)	Output voltage (dual supply)
MSB							LSB		
1	1	1	1	1	1	1	1	Vcc	−0V
1	0	0	0	0	0	0	0	Vcc −0.5V	−0.5V
0	0	0	0	0	0	0	0	Vcc −1.0V	−1.0V

Electrical Characteristics Test Circuit

DC characteristics

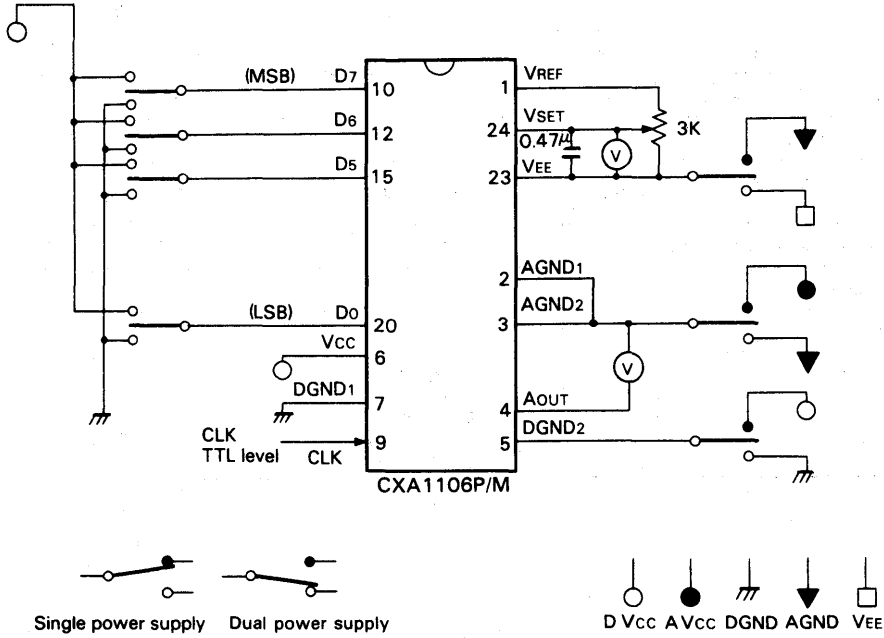
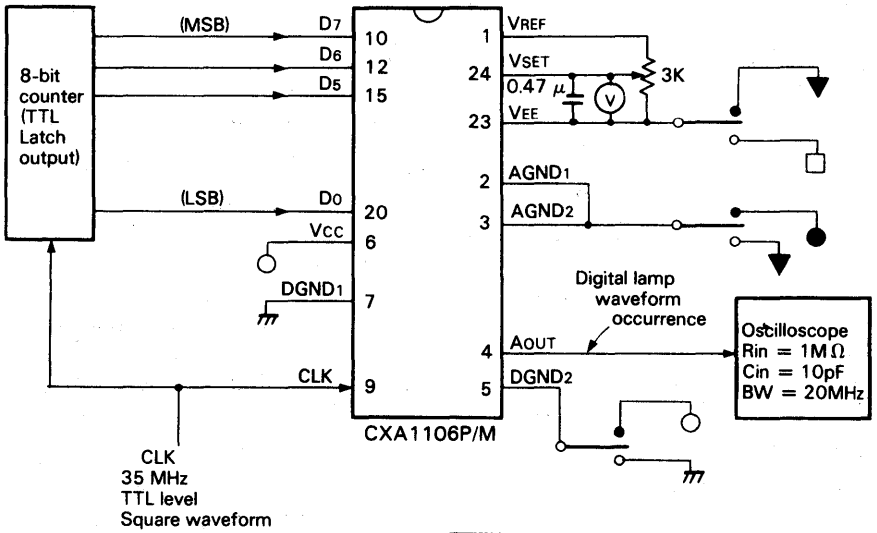
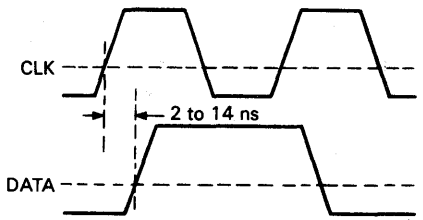


Fig. 1

Test Circuit for Maximum Conversion Speed





Timing between CLK and Data

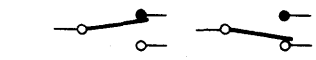


Fig. 2

5

Test Circuit for Set-up Time, Hold Time

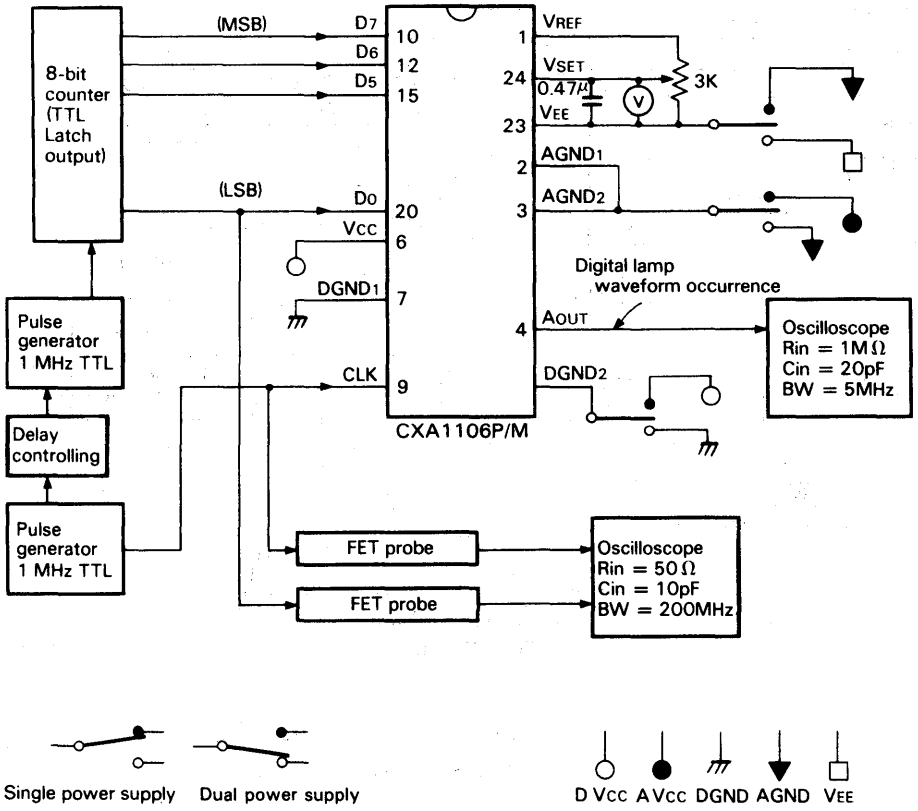
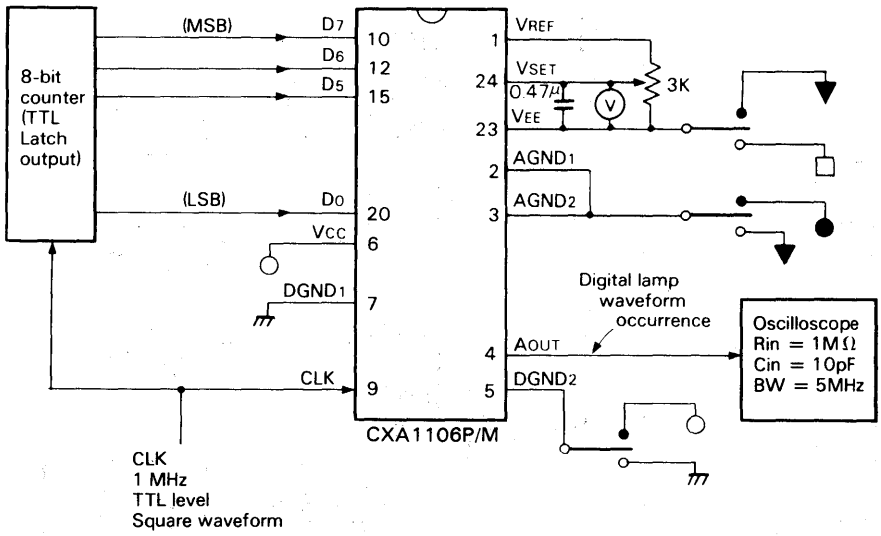
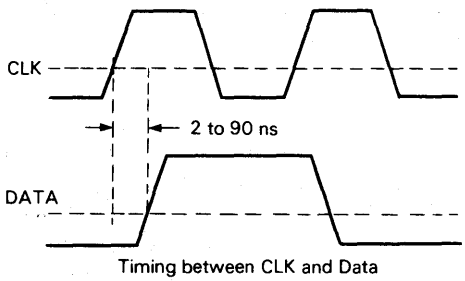


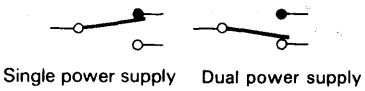
Fig. 3

Test Circuit for Glitch Energy





Timing between CLK and Data



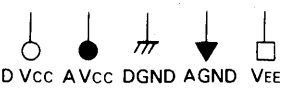
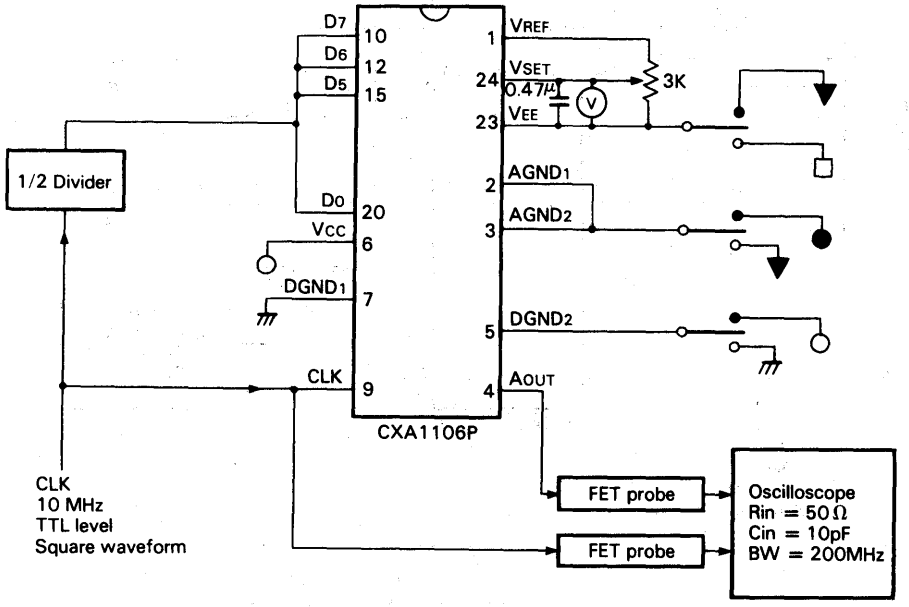
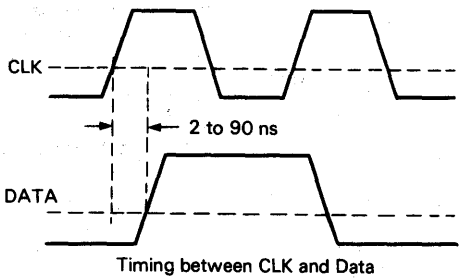


Fig. 4

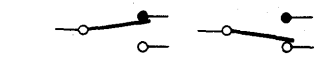
5

Test Circuit for Propagation Delay Time





Timing between CLK and Data



Single power supply Dual power supply

Fig. 5

Operation

Timing chart

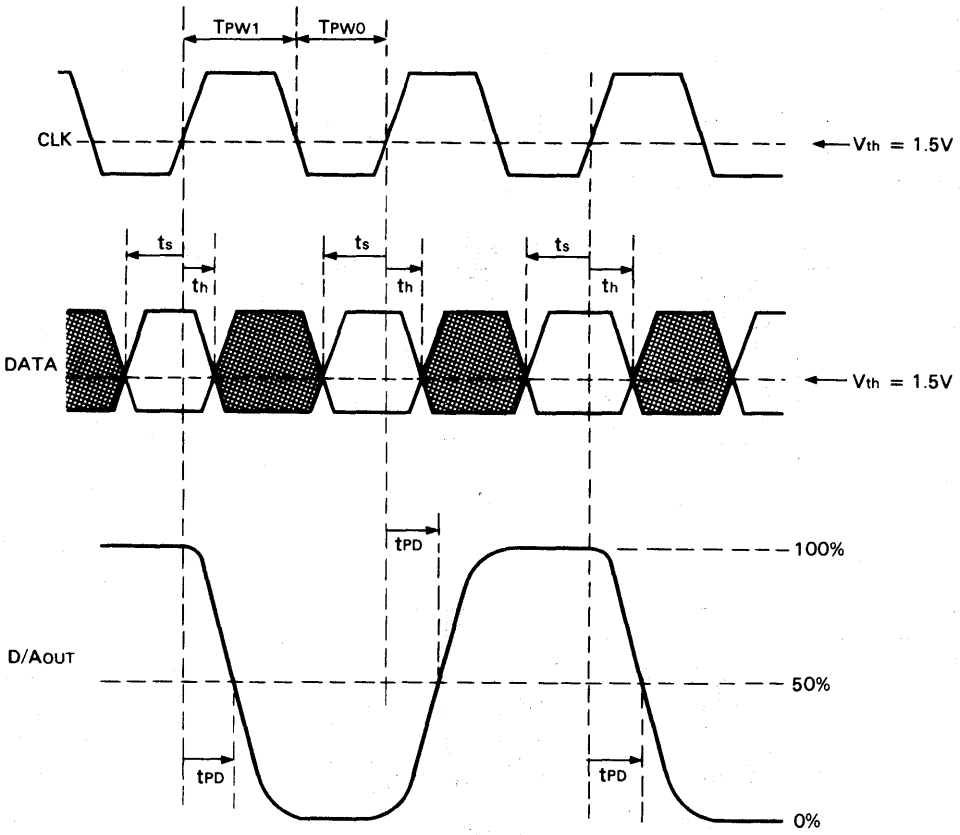
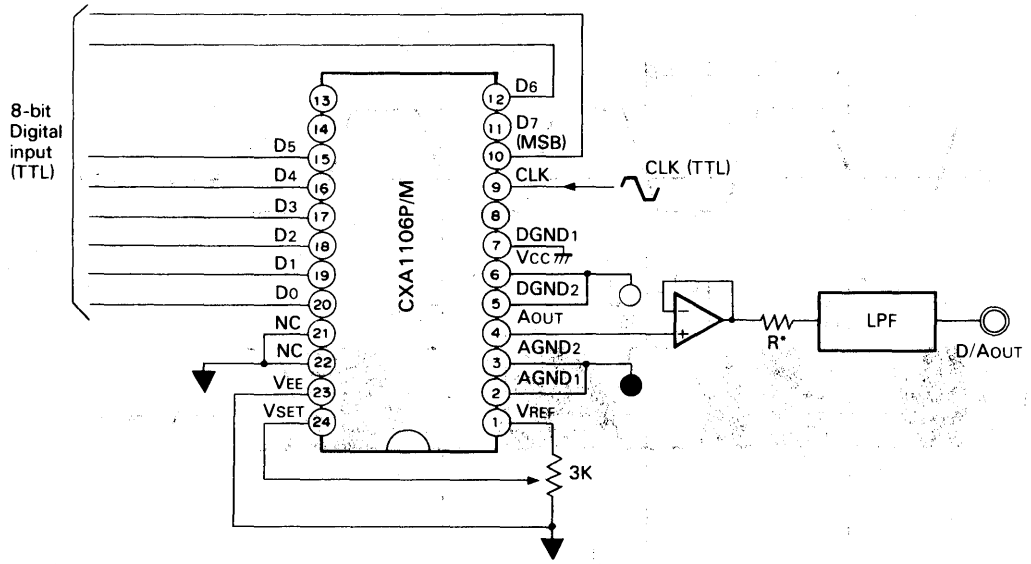


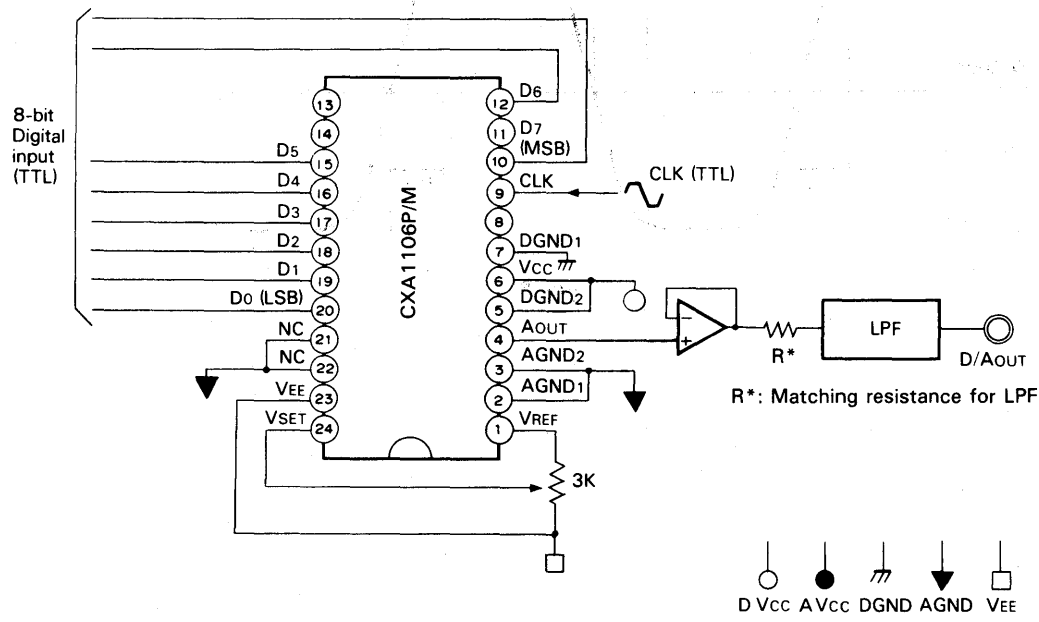
Fig. 6

Application Circuits

Single power supply



Dual power supply



R*: Matching resistance for LPF

Notes on Application

1. Setting of VSET Pin (Pin 24)

   The full-scale voltage of the D/A output is determined by VSET input voltage. As about (1.2V - VEE) DC voltage is generated at VREF pin (Pin 1) by connecting an external resistor from VREF pin to VEE pin (Pin 23), divide this voltage using resistors and apply it to VSET pin as Fig. 7.

(Example of usage)

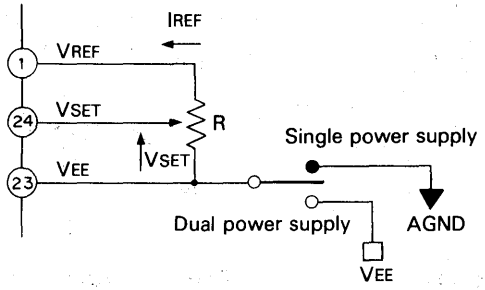


Fig. 7

The full-scale voltage of the D/A output can be determined from the following equation.

$$V_{FS} = 1.2\ (V_{SET} - V_{EE})\ (R_L > 10K\Omega,\ 0.4V \leq V_{SET} \leq 1.2V)$$

Select an external resistor R (Connected to VREF pin) so that IREF (current of an external resistor) is within the value indicated as the Recommended Operational Conditions (-3 mA $< I_{REF} < -0.4$ mA).

2. Phase relation between Data and Clock

   To make the best use of the inherent characteristics of this D/A converter the phase relation between the data and clock applied from the exterior, should be properly set.
   Set up time (ts) and Hold time (th) should be as indicated in the Electrical characteristics. For ts and th refer to Fig. 6 in the Timing Chart.
   Also, set the clock pulse width according to the Recommended Operating Conditions.

3. D/A output pin Load

   Receive the D/A output stage at high impedance, so as to obtain

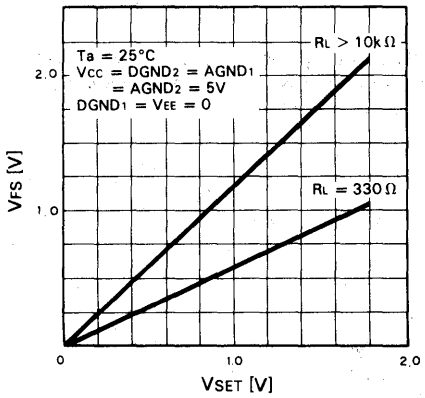
   $R_L > 10K\Omega$
   $C_L < 20pF$

4. Noise reduction

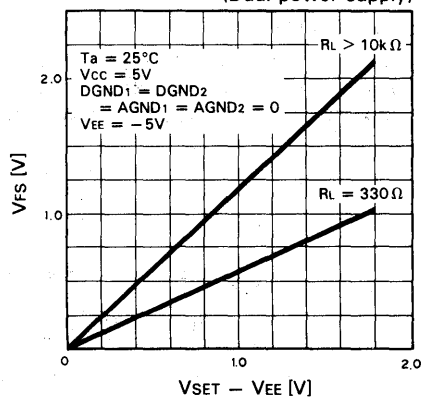
   Refer to the following notes in order to minimize noise contamination that occurs from outside the IC and penatrates D/A output.
   - The power supply line and ground line should be made as wide as possible when fixed to the printed circuit board. Analog and Digital circuits should be separated.
   - Connected a bypass capacitor between each of DVCC (Pin 6) and DGND1 (Pin 7); AGND1,2 (Pins 2, 3) and VEE (Pin 23); VSET (Pin 24) and VEE (Pin 23), respectively.

5

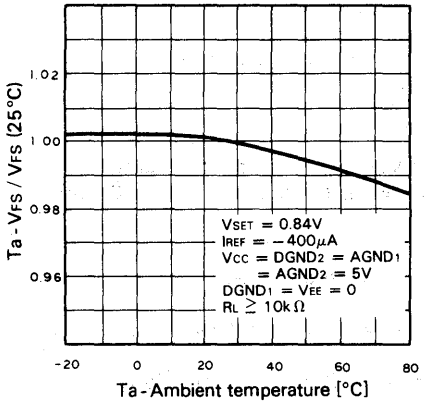
Full-scale output voltage VFS and VSET (Single power supply)



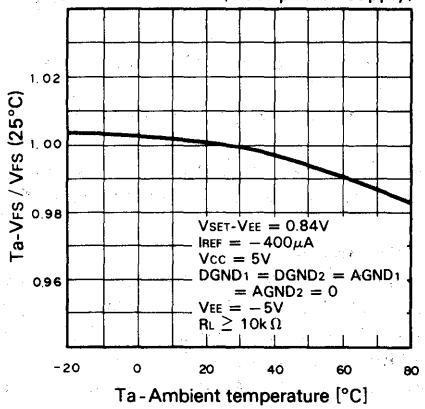
Full-scale output voltage VFS and VSET-VEE (Dual power supply)



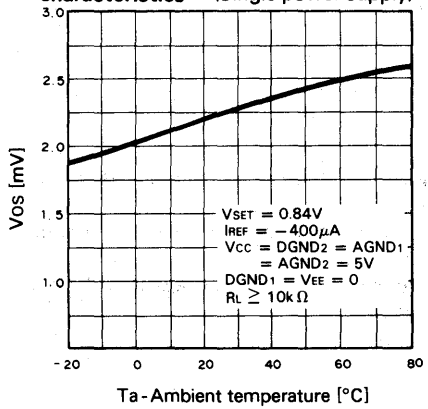
Full-scale output voltage VFS temperature characteristics (Single power supply)



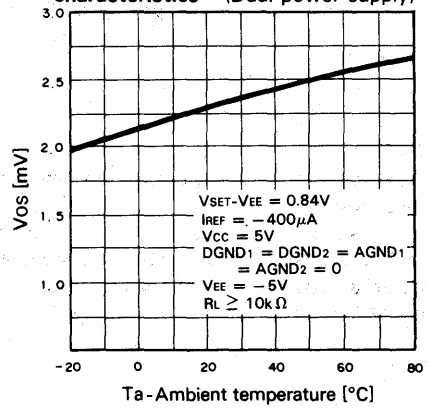
Full-scale output voltage VFS temperature characteristics (Dual power supply)



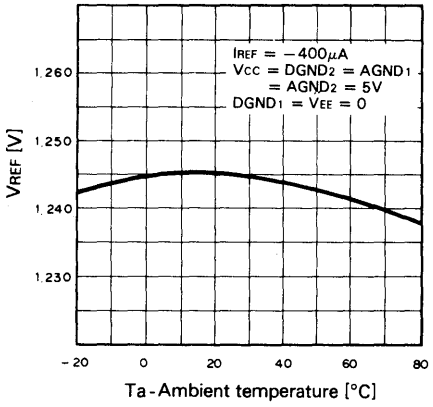
Output offset voltage VOS temperature characteristics (Single power supply)



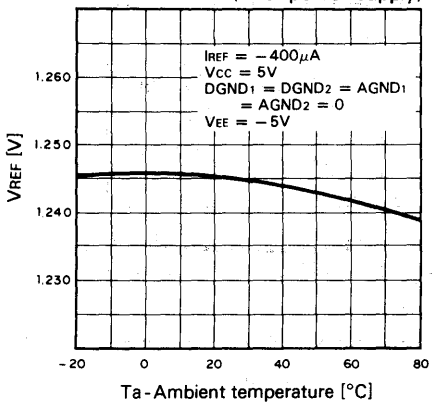
Output offset voltage VOS temperature characteristics (Dual power supply)



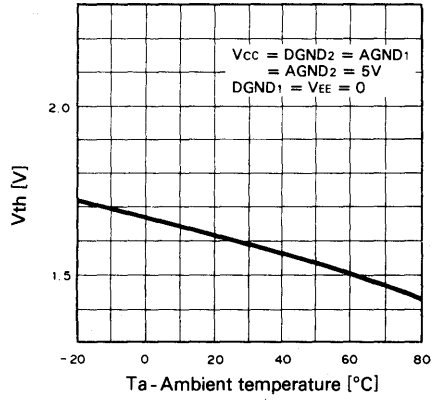
Internal reference voltage VREF temperature characteristics (Single power supply)



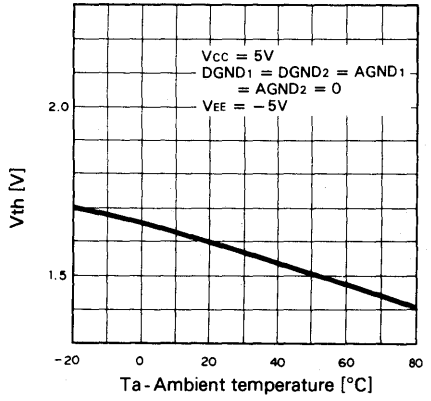
Internal reference voltage VREF temperature characteristics (Dual power supply)



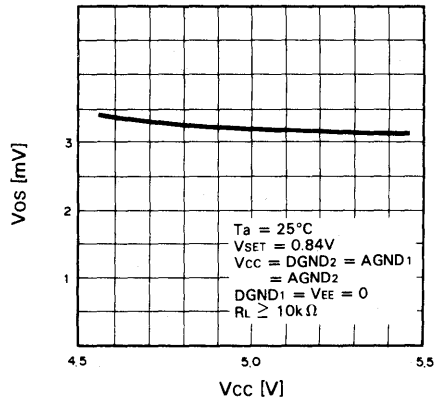
Threshold voltage Vth of digital input temperature characteristics (Single power supply)



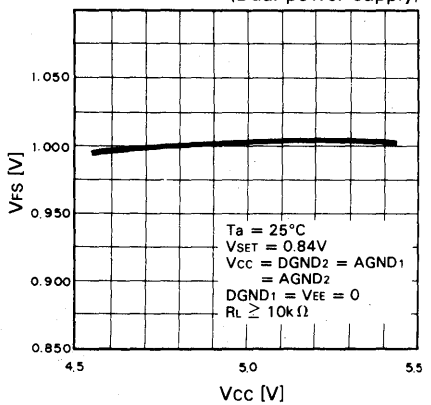
Threshold voltage Vth of digital input temperature characteristics (Dual power supply)



Output offset voltage VOS to Supply voltage (Single power supply)

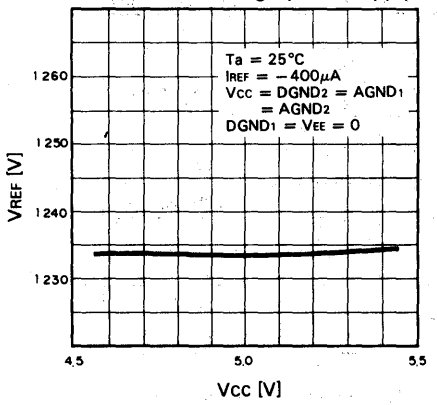


Output full-scale voltage VFS to Supply voltage (Dual power supply)



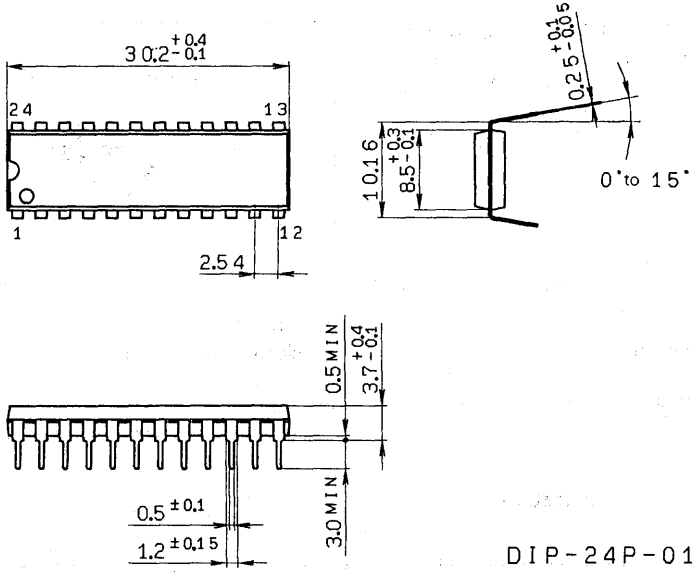
5

Internal reference voltage V_{REF} to supply voltage
(Single power supply)



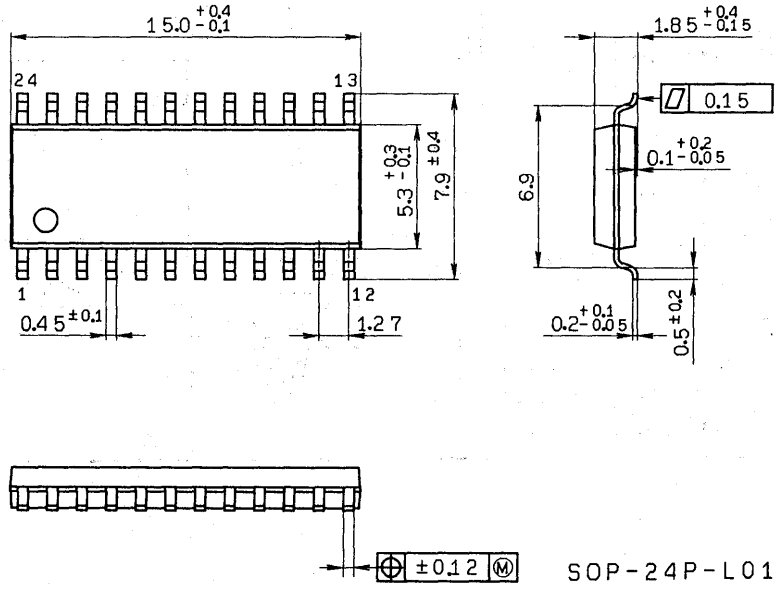
Package Outline Unit : mm

CXA1106P 24 pin DIP (Plastic) 400mil 2.0g



DIP-24P-01

CXA1106M 24 pin SOP (Plastic) 300mil 0.3g



SOP-24P-L01

5

SONY

CXD1170M

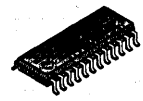
6-bit 40 MSPS High Speed D/A Converter

Description

The CXD1170M is a 6-bit 40MHz high speed D/A converter. The adoption of a current output system reduces power consumption to 80mW (200Ω load at 2Vp-p output).

This IC is suitable for digital TV and graphic display applications.

24pin SOP (Plastic)



Features

- Resolution 6-bit
- Max. conversion speed 40MSPS
- Non linearity error within ±0.1LSB
- Low glitch noise
- TTL CMOS compatible input
- +5V single power supply
- Low power consumption 80mW (200Ω load at 2Vp-p output)

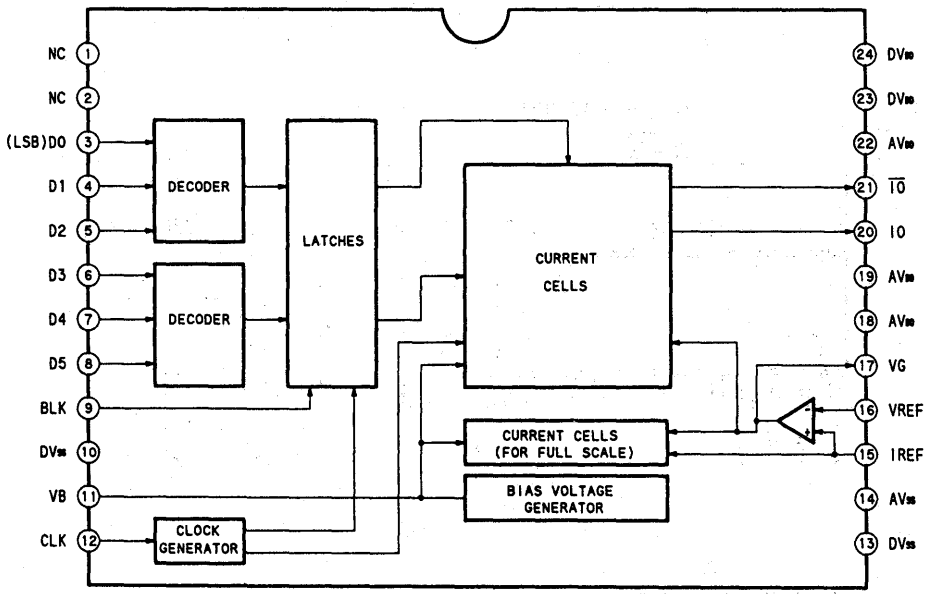
Structure

Silicon gate CMOS IC

Function

6-bit 40MHz D/A converter

Block Diagram and Pin Configuration



E89X37-HP

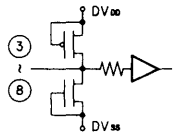
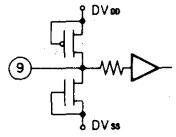
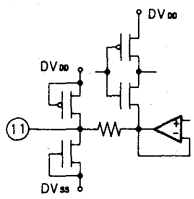
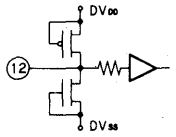
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Output voltage	I_{OUT}	0 to 15	mA
• Storage temperature	T_{stg}	−55 to +150	°C

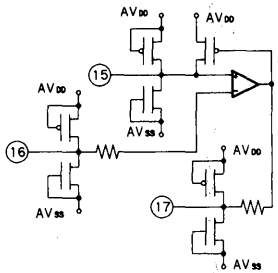
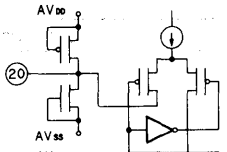
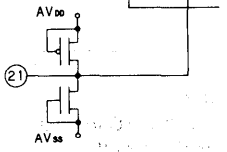
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	T_{PW1}	12.5 (Min)	ns
	T_{PW0}	12.5 (Min)	ns
• Operating temperature	T_{opr}	−20 to +75	°C

Pin Description and I/O Pins Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
3 to 8	D0 to D5		Digital input
9	BLK		Blanking pin No signal at "H" (Output 0V) Output condition at "L"
11	VB		Connect a capacitor of about 0.1μF
12	CLK		Clock pin Moreover all input pins are TTL-CMOS compatible
10, 13	DV_{SS}		Digital GND
14	AV_{SS}		Analog GND

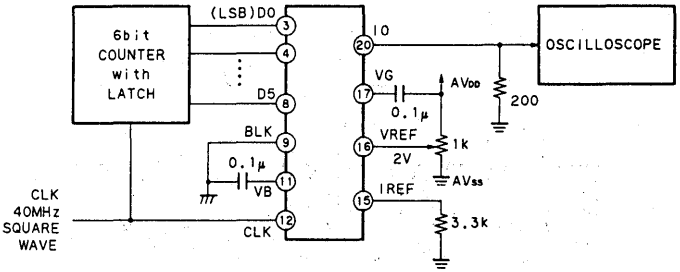
5

No.	Symbol	Equivalent circuit	Description
15	I_{REF}		Connect a resistance 16 times "16R" that of output resistance value "R"
16	V_{REF}		Set full scale output value
17	VG		Connect a capacitor of about 0.1μF
18, 19, 22	AV_{DD}		Analog V_{DD}
20	IO		Current output pin Voltage output can be obtained by connecting a resistance
21	$\overline{IO}$		Inverted current output pin Normally dropped to analog GND
23, 24	DV_{DD}		Digital V_{DD}

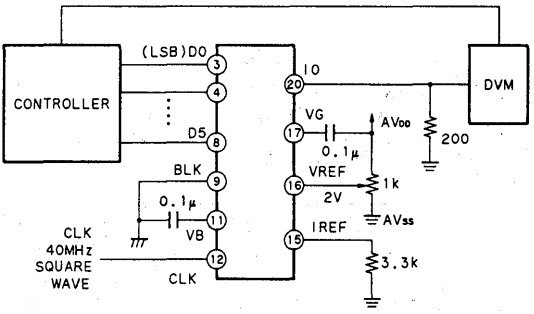
Electrical Characteristics (f_{CLK}=40MHz, V_{DD}=5V, R_{OUT}=200Ω, V_{ref}=2.0V, Ta=25°C)

Item		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Resolution		n			6		bit
Maximum conversion speed		f_{MAX}		40			MSPS
Linearity error		E_L		−0.3		0.5	LSB
Differential linear error		E_D		−0.1		0.1	LSB
Full scale output voltage		V_{FS}		1.85	1.95	2.05	V
Full scale output current		I_{FS}			10	15	mA
Offset output voltage		V_{OS}				1	mV
Power supply current		I_{DD}	14.3MHz, at COLOR BAR DATA input	13	14.5	16	mA
Digital input current	H level	I_{IH}				5	μA
	L level	I_{IL}		−5			μA
Accuracy guaranteed range of output voltage		V_{OC}		0.5	2.0	2.1	V
Set up time		t_S		5			ns
Hold time		t_H		10			ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE	R_{OUT}=75Ω		30		pV-s

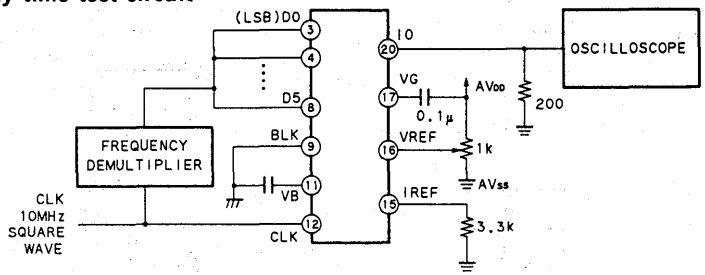
Maximum conversion speed test circuit



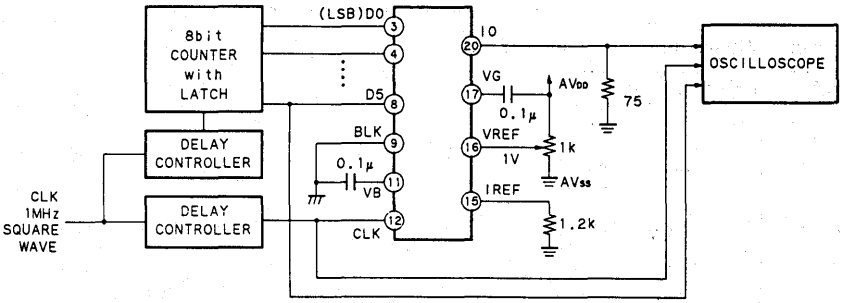
DC characteristics test circuit



Propagation delay time test circuit

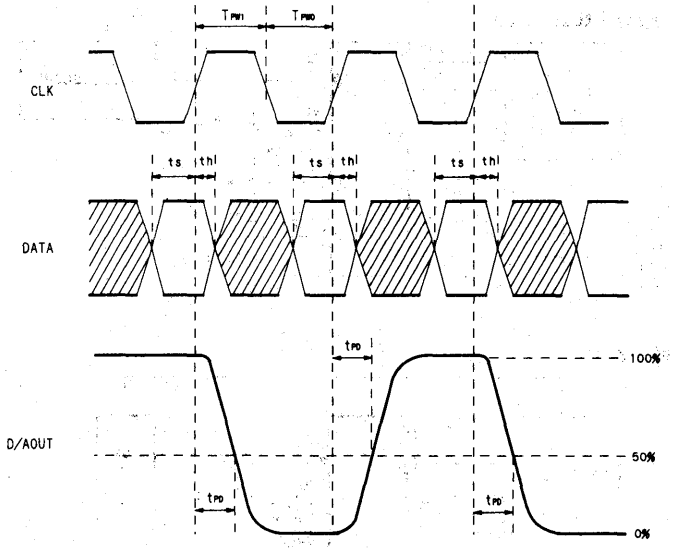


Set up hold time and glitch energy test circuit

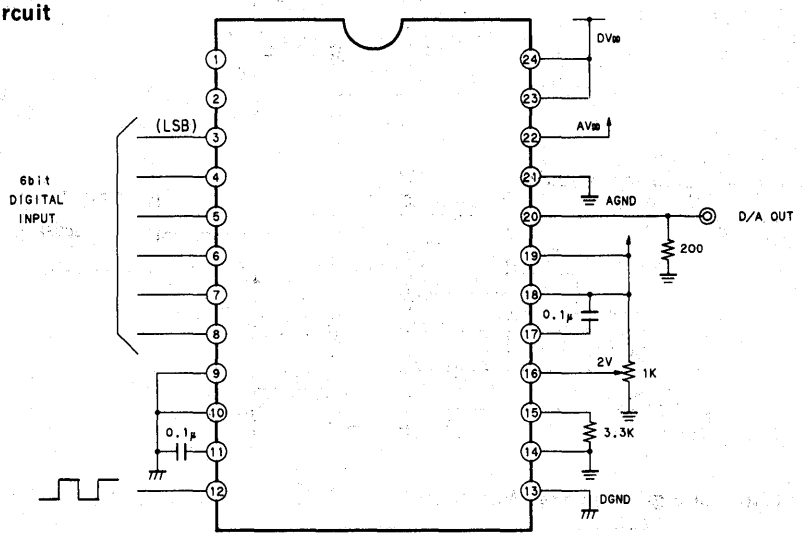


5

Operation Timing Chart



Application Circuit



I/O Chart (when full scale output voltage at 2.00V)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1	2.0V
⋮	
1 0 0 0 0 0	1.0V
⋮	
0 0 0 0 0 0	0V

Notes on Operation

- How to select the output resistance

The CXD1170M is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin. For specifications we have:

Output full scale voltage V_{FS}=0.5 to 2.0 [V]

Output full scale current I_{FS}=0 to 15 [mA]

Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS}=V_{REF} \times 16R/R'$. R is the resistance connected to IO while R′ is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (ts) and hold time (th) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

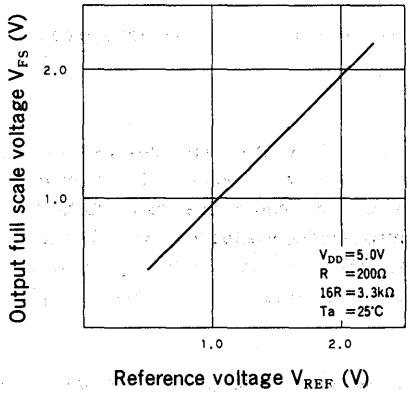
To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1μF, as close as possible to the pin.

- Latch up

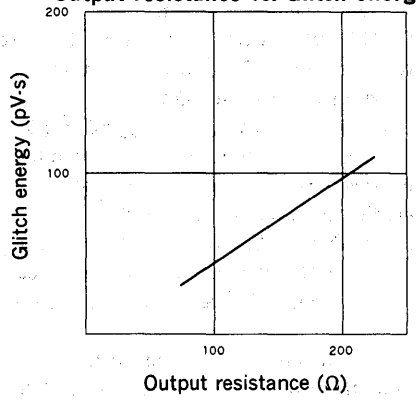
AV_{DD} and DV_{DD} have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

5

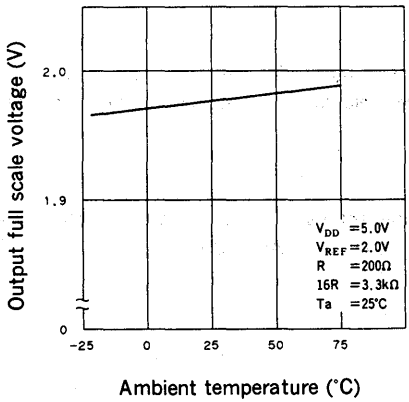
Output full scale voltage vs. Reference voltage



Output resistance vs. Glitch energy

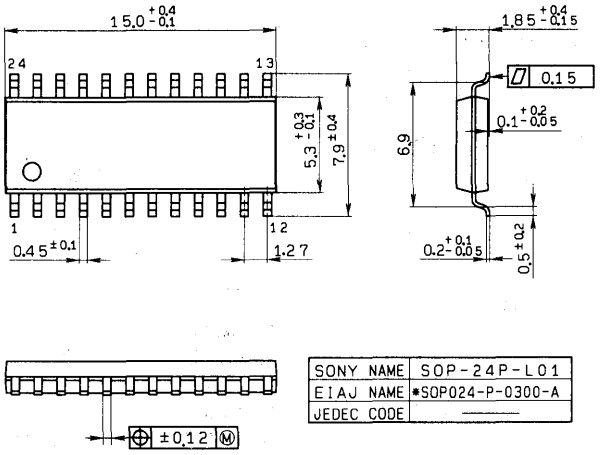


Output full scale voltage vs. Ambient temperature



Package Outline Unit: mm

24pin SOP (Plastic) 300mil 0.3g



SONY NAME	SOP-24P-L01
EIAJ NAME	*SOP024-P-0300-A
JEDEC CODE	———

5

SONY

CXD1171M

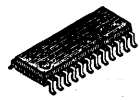
8-bit 40 MSPS High Speed D/A Converter

Description

The CXD1171M is an 8-bit 40MHz high speed D/A converter. The adoption of a current output system reduces power consumption to 80mW (200Ω load at 2Vp-p output).

This IC is suitable for digital TV and graphic display applications.

24pin SOP (Plastic)



Features

- Resolution 8-bit
- Max. conversion speed 40MSPS
- Non linearity error within ±0.25LSB
- Low glitch noise
- TTL CMOS compatible input
- +5V single power supply
- Low power consumption 80mW (200Ω load at 2Vp-p output)

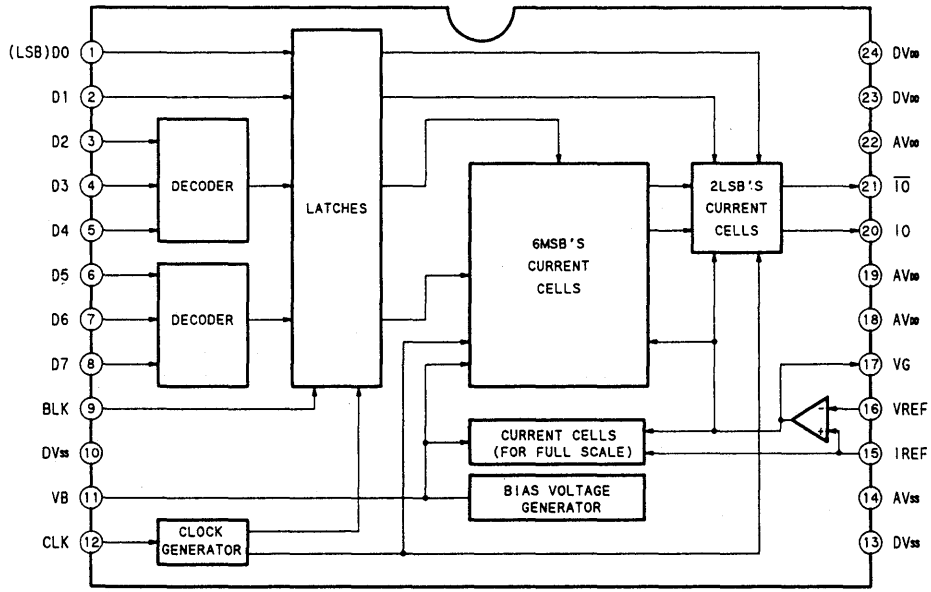
Structure

Silicon gate CMOS IC

Function

8-bit 40MHz D/A converter

Block Diagram and Pin Configuration



E89X38-HP

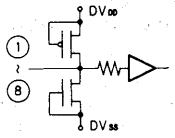
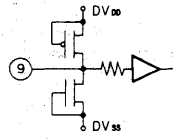
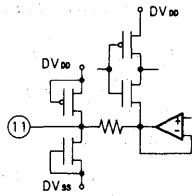
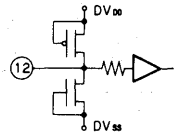
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to V_{SS}	V
• Output voltage	I_{OUT}	0 to 15	mA
• Storage temperature	T_{stg}	−55 to +150	°C

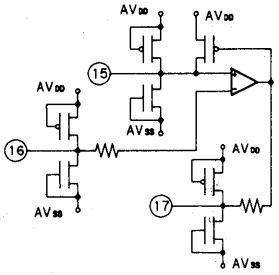
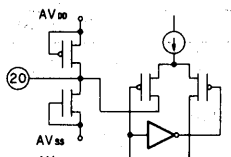
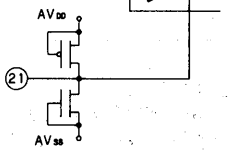
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	T_{PW1}	12.5 (Min)	ns
	T_{PW0}	12.5 (Min)	ns
• Operating temperature	T_{opr}	−20 to +75	°C

Pin Description and I/O Pins Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1 to 8	D0 to D7		Digital input
9	BLK		Blanking pin No signal at "H" (Output 0V) Output condition at "L"
11	VB		Connect a capacitor of about 0.1μF
12	CLK		Clock pin Moreover all input pins are TTL-CMOS compatible
10, 13	DV_{SS}		Digital GND
14	AV_{SS}		Analog GND

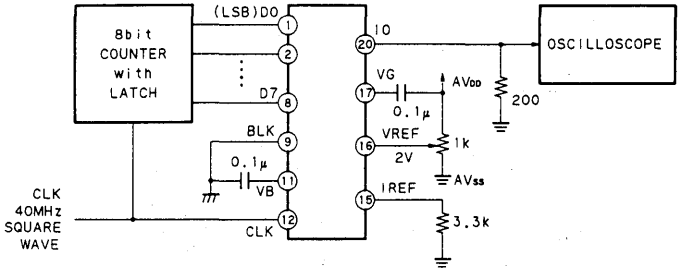
5

No.	Symbol	Equivalent circuit	Description
15	I_{REF}		Connect a resistance 16 times "16R" that of output resistance value "R"
16	V_{REF}		Set full scale output value
17	VG		Connect a capacitor of about 0.1μF
18, 19, 22	AV_{DD}		Analog V_{DD}
20	IO		Current output pin Voltage output can be obtained by connecting a resistance
21	$\overline{IO}$		Inverted current output pin Normally dropped to analog GND
23, 24	DV_{DD}		Digital V_{DD}

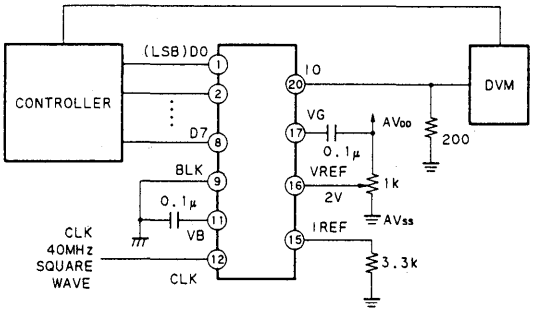
Electrical Characteristics (f_{CLK}=40MHz, V_{DD}=5V, R_{OUT}=200Ω, V_{ref}=2.0V, Ta=25°C)

Item		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}		40			MSPS
Linearity error		E_L		−0.5		1.3	LSB
Differential linear error		E_D		−0.25		0.25	LSB
Full scale output voltage		V_{FS}		1.9	2.0	2.1	V
Full scale output current		I_{FS}			10	15	mA
Offset output voltage		V_{OS}				1	mV
Power supply current		I_{DD}	14.3MHz, at COLOR BAR DATA input	13	14.5	16	mA
Digital input current	H level	I_{IH}				5	μA
	L level	I_{IL}		−5			μA
Accuracy guaranteed range of output voltage		V_{OC}		0.5	2.0	2.1	V
Set up time		t_S		5			ns
Hold time		t_H		10			ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE	R_{OUT}=75Ω		30		pV-s

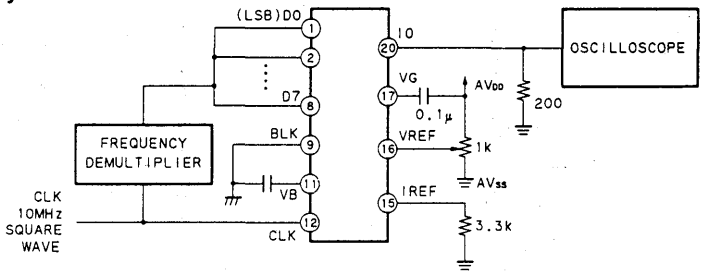
Maximum conversion speed test circuit



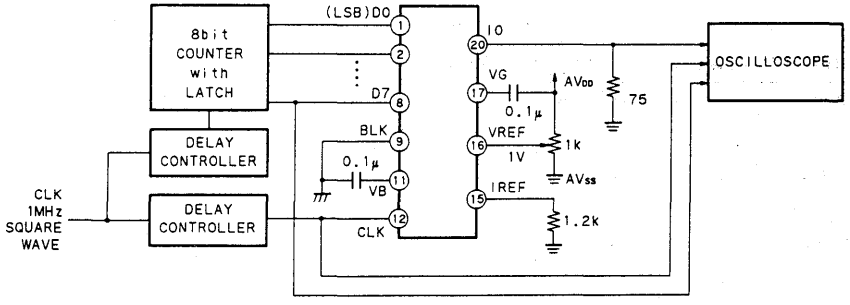
DC characteristics test circuit



Propagation delay time test circuit

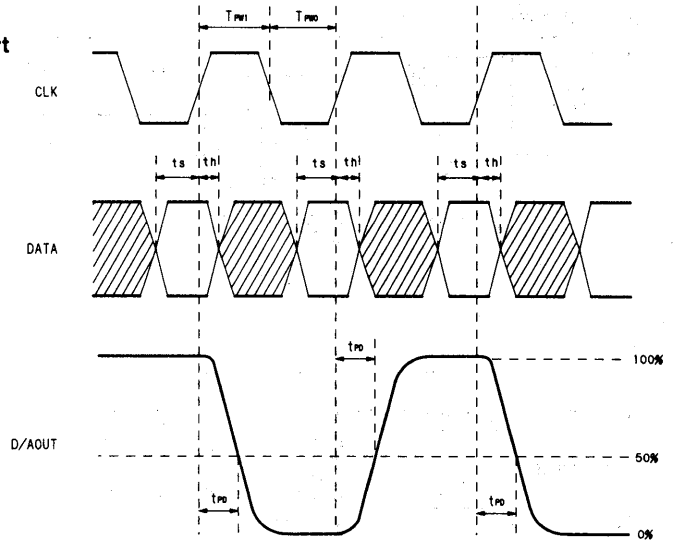


Set up hold time and glitch energy test circuit

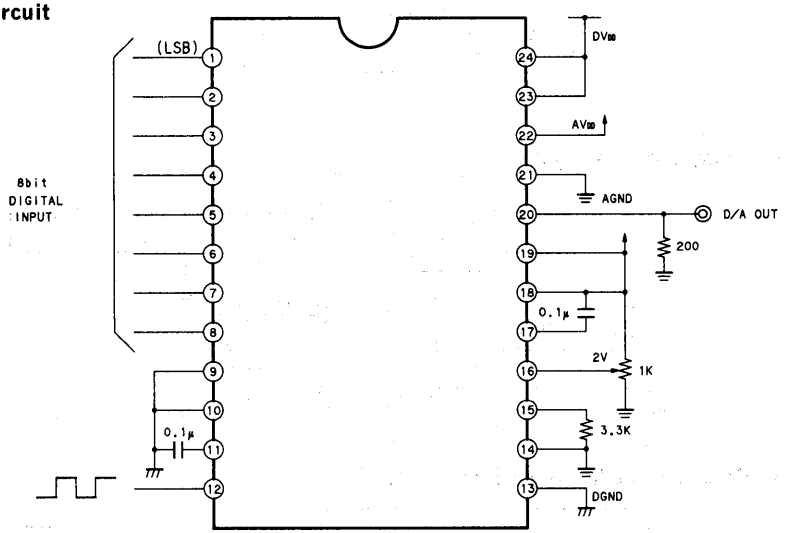


5

Operation Timing Chart



Application Circuit



I/O Chart (when full scale output voltage at 2.00V)

Input code	Output voltage
MSB LSB	
1 1 1 1 1 1 1 1	2.0V
⋮	
1 0 0 0 0 0 0 0	1.0V
⋮	
0 0 0 0 0 0 0 0	0V

Notes on Operation

- How to select the output resistance

The CXD1171M is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin. For specifications we have ;

Output full scale voltage V_{FS}=0.5 to 2.0 [V]

Output full scale current I_{FS}=0 to 15 [mA]

Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS}=V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (ts) and hold time (th) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

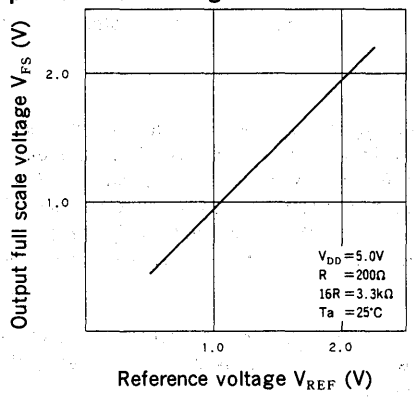
To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1μF, as close as possible to the pin.

- Latch up

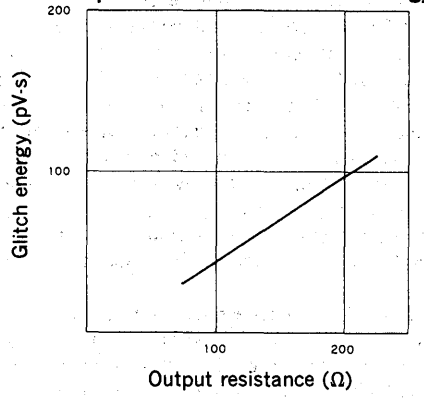
AV_{DD} and DV_{DD} have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

5

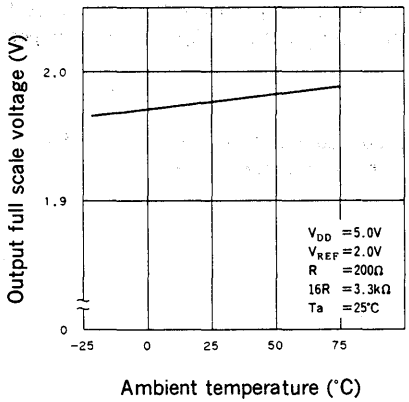
Output full scale voltage vs. Reference voltage



Output resistance vs. Glitch energy

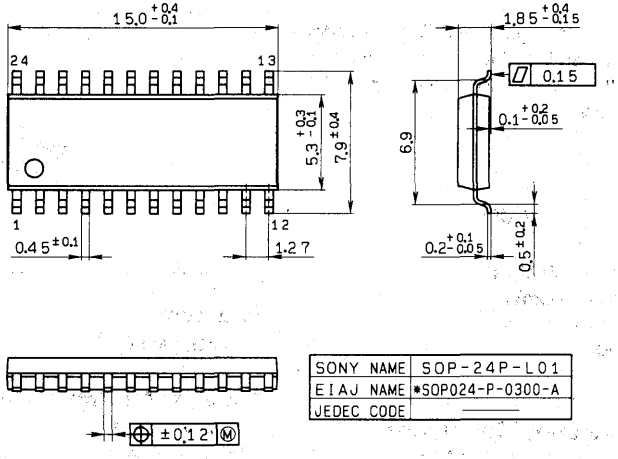


Output full scale voltage vs. Ambient temperature



Package Outline Unit : mm

24pin SOP (Plastic) 300mil 0.3g



SONY NAME	SOP-24P-L01
EIAJ NAME	*SOP024-P-0300-A
JEDEC CODE	

5

SONY

CXD1177Q

8-bit 40MSPS YC 2-Channel D/A Converter

Description

The CXD1177Q is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 2 channels of Y and C. It is suitable for use of digital TV, graphic display, and others.

Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- YC 2-channel input/output
- Differential linearity error ±0.3LSB
- Low power consumption 160mW (200Ω load at 2Vp-p output)
- Single 5V power supply
- Low glitch noise

32 pin QFP (Plastic)

Structure

Silicon gate CMOS IC

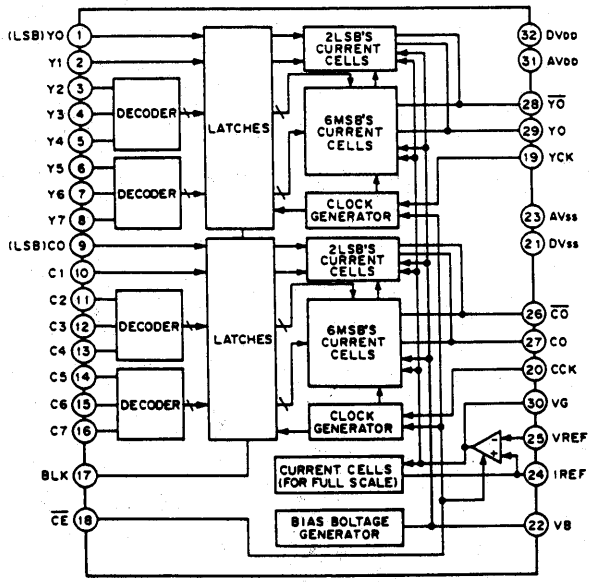
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AVss	4.75 to 5.25	V
	DV_{DD}, DVss	4.75 to 5.25	V
• Reference input voltage	V_{REF}	0.5 to 2.0	V
• Clock pulse width	T_{PW1}	12.5 (Min.)	ns
	T_{PW0}	12.5 (Min.)	ns
• Operating temperature	Topr	−20 to +75	℃

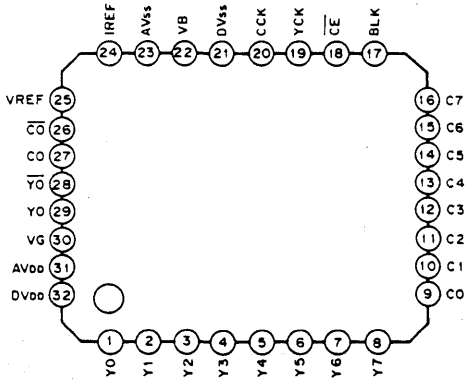
Absolute Maximum Ratings (Ta=25℃)

• Supply voltage	V_{DD}	7	V
• Input voltage	V_{IN}	V_{DD} to Vss	V
• Output current (Every each channel)	I_{OUT}	0 to 15	mA
• Storage temperature	Tstg	−55 to +150	℃

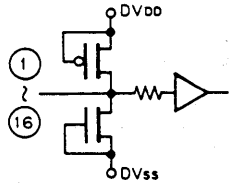
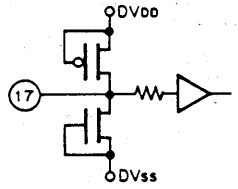
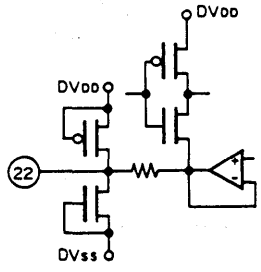
Block Diagram



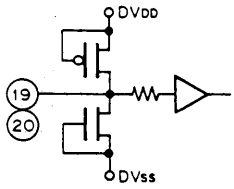
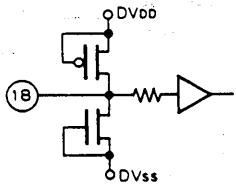
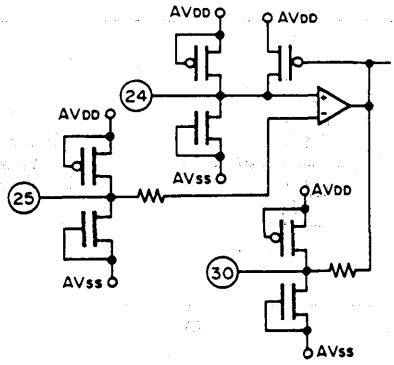
Pin Configuration

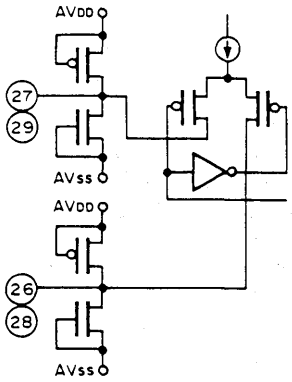


Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	Y0 to Y7		Digital input
9 to 16	C0 to C7		
17	BLK		Blanking pin. No signal at "H" (Output 0V). Output condition at "L".
22	VB		Connect a capacitor of about 0.1 µF.

5

Pin No.	Symbol	Equivalent circuit	Description
19	YCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
20	CCK		
21	DVss		Digital GND
23	AVss		Analog GND
18	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at "H" and minimizes power consumption.
24	IREF		Connect a resistance 16 times "16R" that of output resistance value "R".
25	VREF		Set full scale output value.
30	VG		Connect a capacitor of about 0.1 µF.
31	AVDD		Analog VDD

Pin No.	Symbol	Equivalent circuit	Description
27	CO		Current output pin. Voltage output can be obtained by connecting a resistance.
29	YO		
26	$\overline{CO}$		Inverted current output pin. Normally dropped to analog GND.
28	$\overline{YO}$		
32	DV_{DD}		Digital V_{DD}

Electrical Characteristics

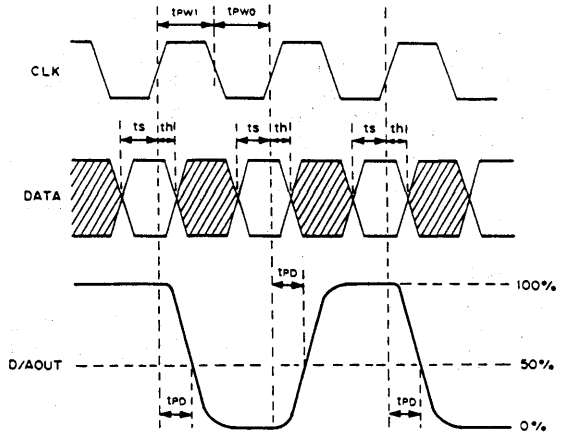
(f_{CLK}=40MHz, V_{DD}=5V, R_{OUT}=200Ω, Vref=2.0V, Ta=25°C)

Item		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}		40			MSPS
Linearity error		E_L		–2.5		2.5	LSB
Differential linearity error		E_D		–0.3		0.3	LSB
Full scale output voltage		V_{FS}		1.9	2.0	2.2	V
Full scale output ratio		F_{SR}		0	1.5	3	%
Full scale output current		I_{FS}			10	15	mA
Offset output voltage		V_{OS}				1	mV
Power supply current		I_{DD}	14.3MHz, at COLOR BAR DATA input			32	mA
Digital input current	H level	I_{IH}				5	µA
	L level	I_{IL}		–5			µA
Accuracy guaranteed range of output voltage		V_{OC}		0.5	2.0	2.2	V
Set up time		ts		5			ns
Hold time		tH		10			ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE	R_{OUT}=75Ω		30		pV-s
Crosstalk		CT	1MHz Sin WAVE OUTPUT		57		dB

5

Description of Operation

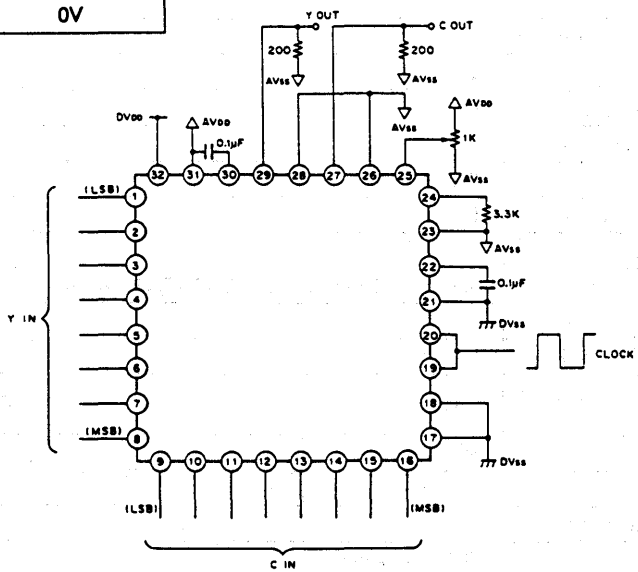
Timing Chart



I/O Chart (When full scale output voltage at 2.00V)

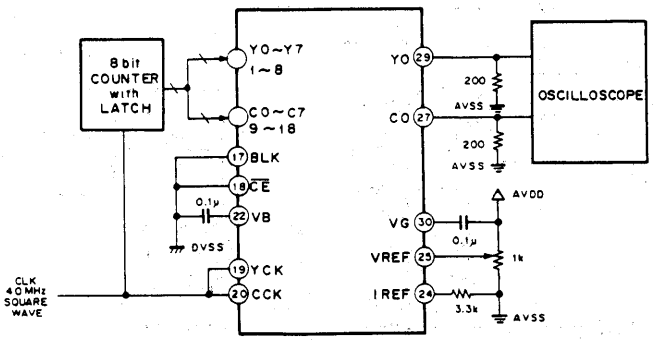
Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1	2.0V
1 0 0 0 0 0 0 0	1.0V
0 0 0 0 0 0 0 0	0V

Application circuit



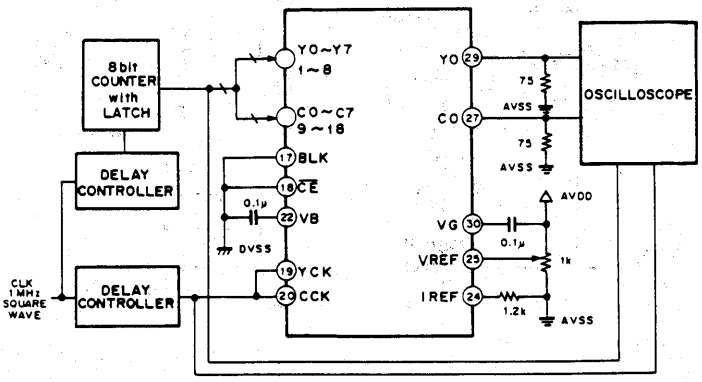
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Maximum conversion velocity test circuit

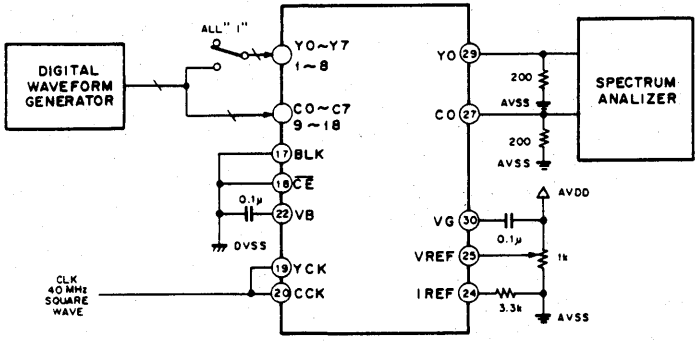


Set up hold time
Glitch energy

Test circuit

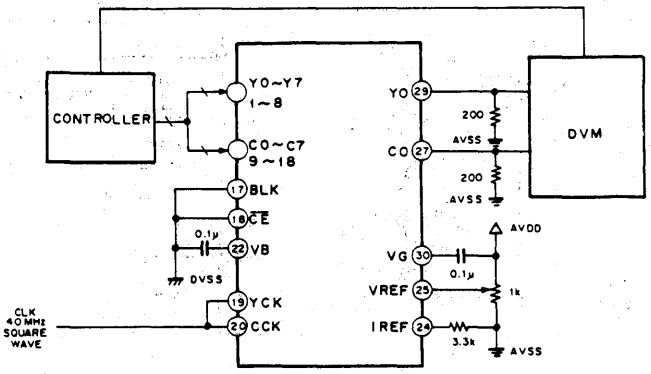


Crosstalk test circuit

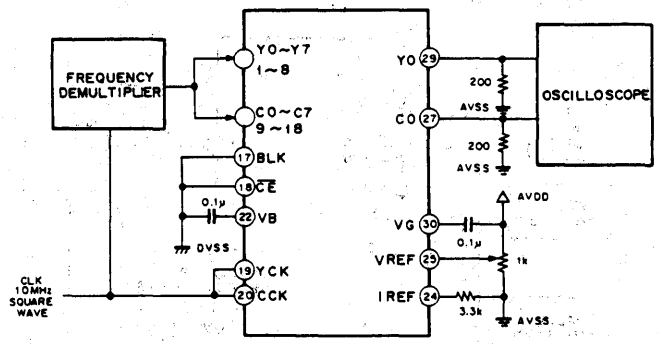


5

DC characteristics test circuit



Propagation delay time test circuit



Notes on Operation

- How to select the output resistance

The CXD1177Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin (Y0, C0). For specifications we have;

Output full scale voltage V_{FS}=0.5 to 2.0 [V]
Output full scale current I_{FS}=0 to 15 [mA]

Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS}=V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (ts) and hold time (th) as stipulated in the Electrical Characteristics.

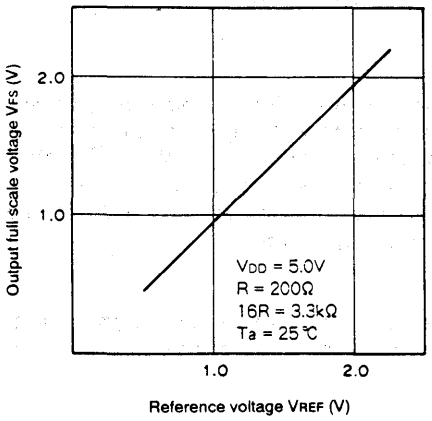
- V_{DD}, Vss

To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1 μF, as close as possible to the pin.

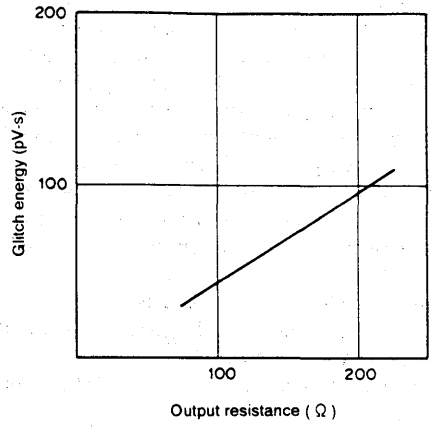
5

Example of Representative Characteristics

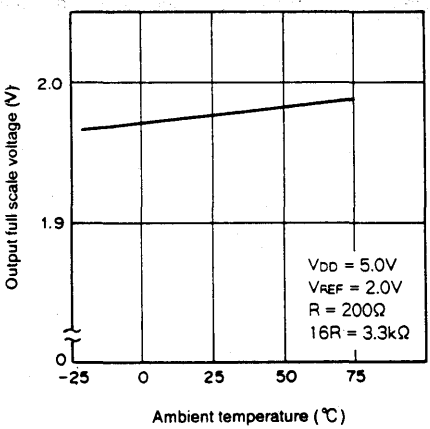
Output full scale voltage vs. Reference voltage



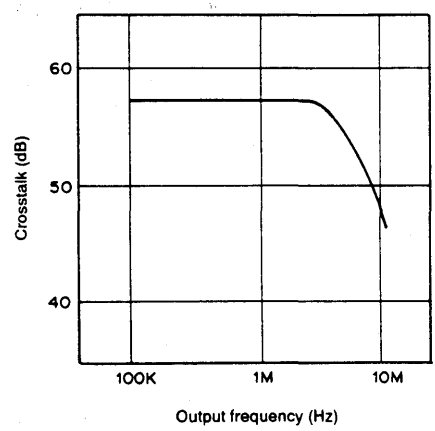
Glitch energy vs. Output resistance



Output full scale voltage vs. Ambient temperature

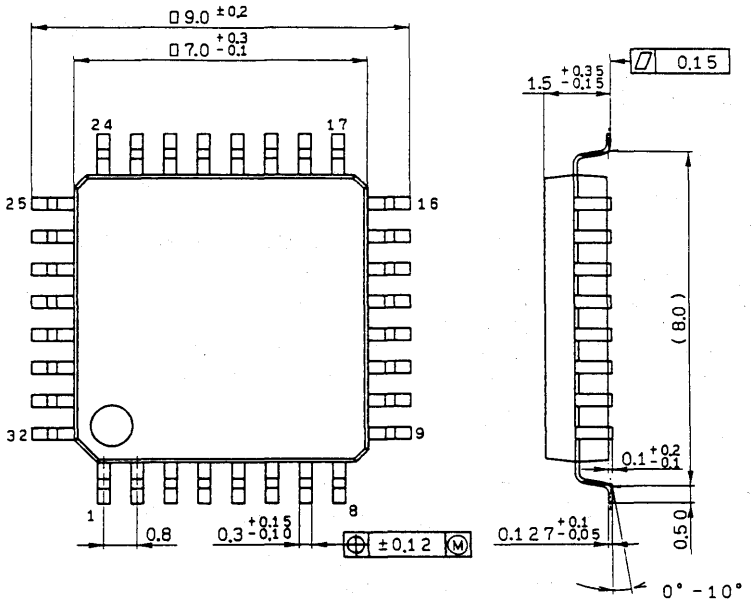


Crosstalk vs. Output frequency



Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

5

SONY

CXD1178Q

8-bit 40MSPS RGB 3-Channel D/A Converter

Description

The CXD1178Q is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, and others.

48 pin QFP (Plastic)

Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- RGB 3-channel input/output
- Differential linearity error +0.3LSB
- Low power consumption 240mW (200Ω load at 2Vp-p output)
- Single 5V power supply
- Low glitch noise

Structure

Silicon gate CMOS IC

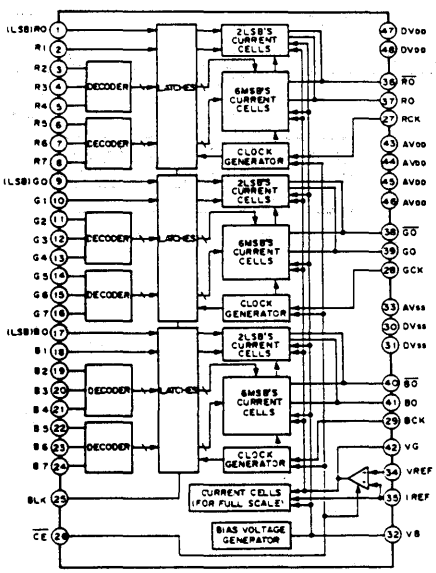
Recommended Operating Conditions

• Supply voltage	AVDD, AVss	4.75 to 5.25	V
	DVDD, DVss	4.75 to 5.25	V
• Reference input voltage	VREF	0.5 to 2.0	V
• Clock pulse width	TpW1	12.5 (Min.)	ns
	TpW0	12.5 (Min.)	ns
• Operating temperature	Topr	−20 to +75	°C

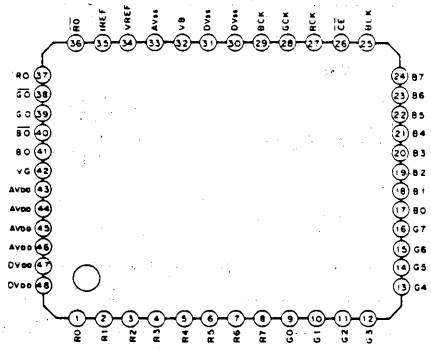
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	VDD	7	V
• Input voltage	VIN	VDD to Vss	V
• Output current (Every each channel)	IOUT	0 to 15	mA
• Storage temperature	Tstg	−55 to +150	°C

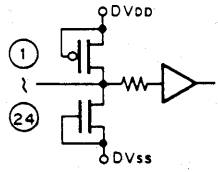
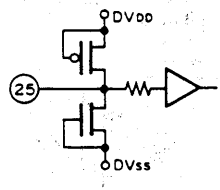
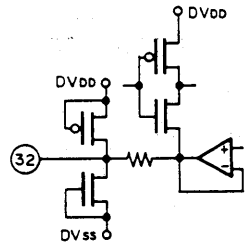
Block Diagram

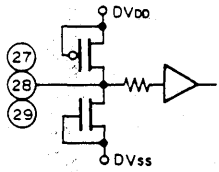
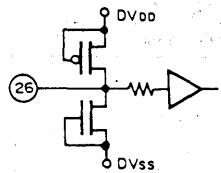
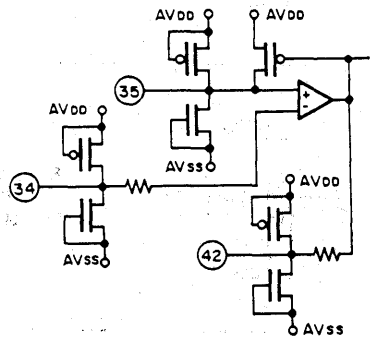


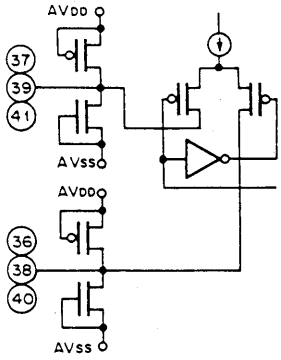
Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	R0 to R7		Digital input
9 to 16	G0 to G7		
17 to 24	B0 to B7		
25	BLK		Blanking pin. No signal at "H" (Output 0V). Output condition at "L".
32	VB		Connect a capacitor of about 0.1 µF.

Pin No.	Symbol	Equivalent circuit	Description
27	RCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
28	GCK		
29	BCK		
30, 31	DVss		Digital GND
33	AVss		Analog GND
26	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at "H" and minimizes power consumption.
35	IREF		Connect a resistance 16 times "16R" that of output resistance value "R".
34	VREF		Set full scale output value.
42	VG		Connect a capacitor of about 0.1 µF.

Pin No.	Symbol	Equivalent circuit	Description
43 to 46	AV_{DD}		Analog V_{DD}
37	RO		Current output pin. Voltage output can be obtained by connecting a resistance.
39	GO		
41	BO		
36	$\overline{RO}$		Inverted current output pin. Normally dropped to analog GND.
38	$\overline{GO}$		
40	$\overline{BO}$		
47, 48	DV_{DD}		Digital V_{DD}

Electrical Characteristics

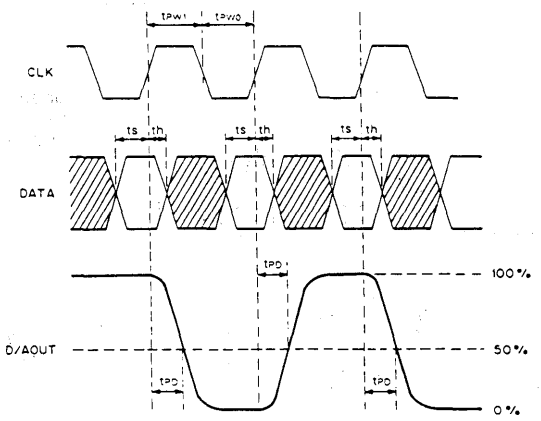
(f_{CLK}=40MHz, V_{DD}=5V, R_{OUT}=200Ω, Vref=2.0V, Ta=25°C)

Item		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Resolution		n			8		bit
Maximum conversion speed		f_{MAX}		40			MSPS
Linearity error		E_L		–2.5		2.5	LSB
Differential linearity error		E_D		–0.3		0.3	LSB
Full scale output voltage		V_{FS}		1.8	2.0	2.2	V
Full scale output ratio		F_{SR}		0	1.5	3	%
Full scale output current		I_{FS}			10	15	mA
Offset output voltage		Vos				1	mV
Power supply current		I_{DD}	14.3MHz, at COLOR BAR DATA input			48	mA
Digital input current	H level	I_{IH}				5	µA
	L level	I_{IL}		–5			µA
Accuracy guaranteed range of output voltage		Voc		0.5	2.0	2.2	V
Set up time		ts		5			ns
Hold time		t_H		10			ns
Propagation delay time		t_{PD}			10		ns
Glitch energy		GE	R_{OUT}=75Ω		30		pV-s
Crosstalk		CT	1MHz Sin WAVE OUTPUT		57		dB

5

Description of Operation

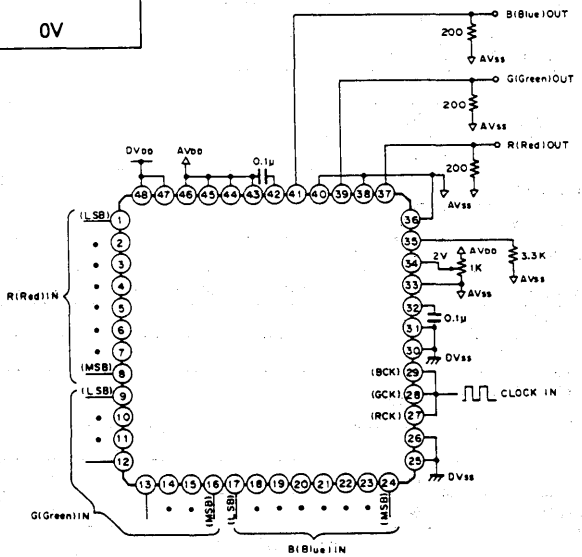
Timing Chart



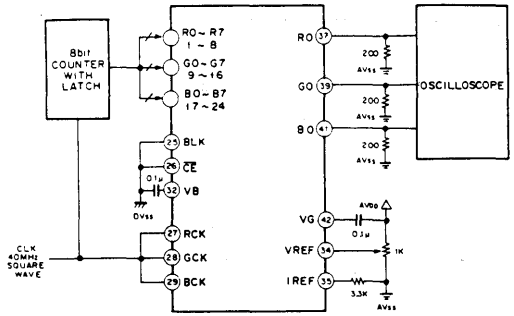
I/O Chart (When full scale output voltage at 2.00V)

Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1	2.0V
1 0 0 0 0 0 0 0	1.0V
0 0 0 0 0 0 0 0	0V

Application circuit

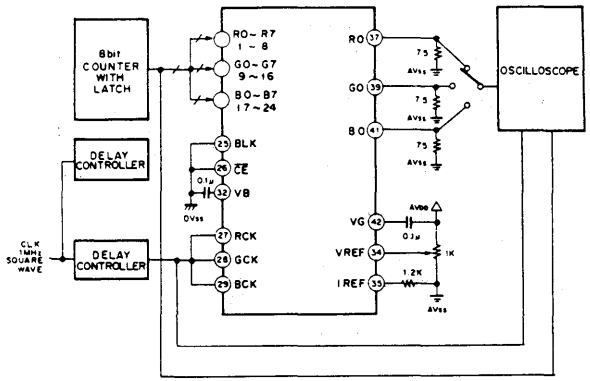


Maximum conversion velocity test circuit

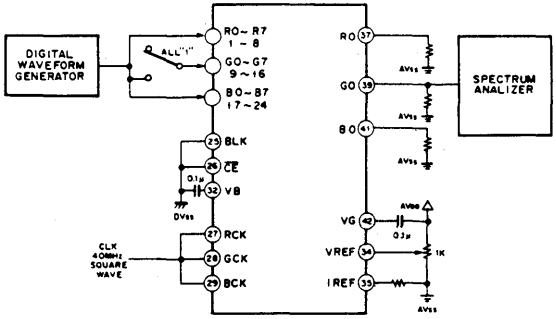


Set up hold time
Glitch energy

Test circuit

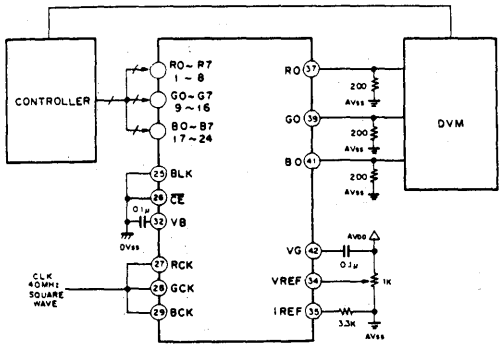


Crosstalk test circuit

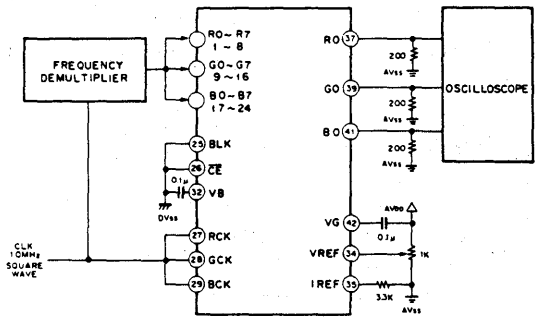


5

DC characteristics test circuit



Propagation delay time test circuit



Notes on Operation

- How to select the output resistance

The CXD1178Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to IO pin (R0, G0, B0). For specifications we have;

Output full scale voltage V_{FS}=0.5 to 2.0 [V]

Output full scale current I_{FS}=0 to 15 [mA]

Calculate the output resistance value from the relation of $V_{FS}=I_{FS} \times R$. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS}=V_{REF} \times 16R/R'$. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (ts) and hold time (th) as stipulated in the Electrical Characteristics.

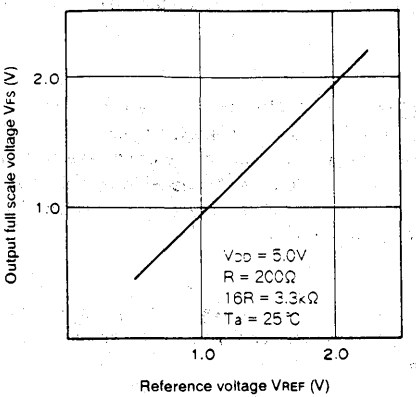
- V_{DD}, Vss

To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of about 0.1 µF, as close as possible to the pin.

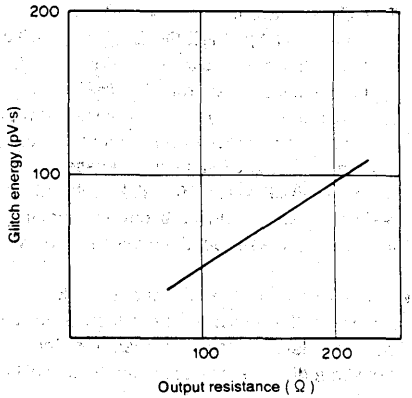
5

Example of Representative Characteristics

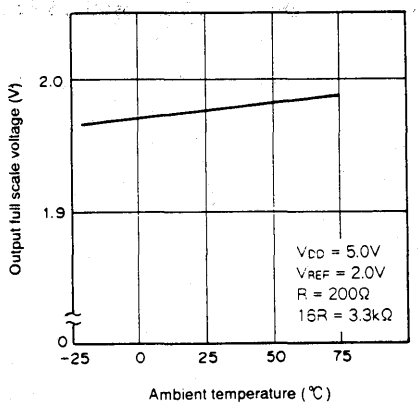
Output full scale voltage vs. Reference voltage



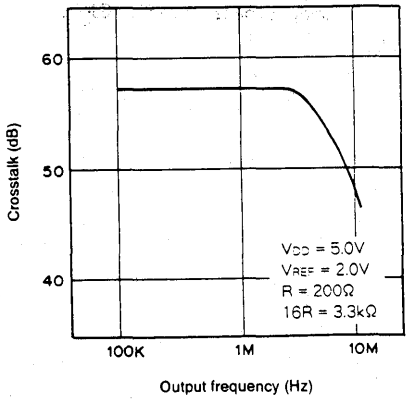
Glitch energy vs. Output resistance



Output full scale voltage vs. Ambient temperature

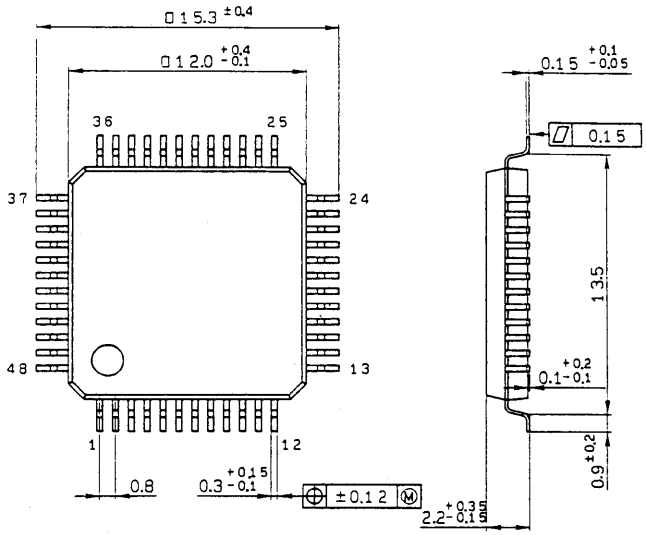


Crosstalk vs. Output frequency



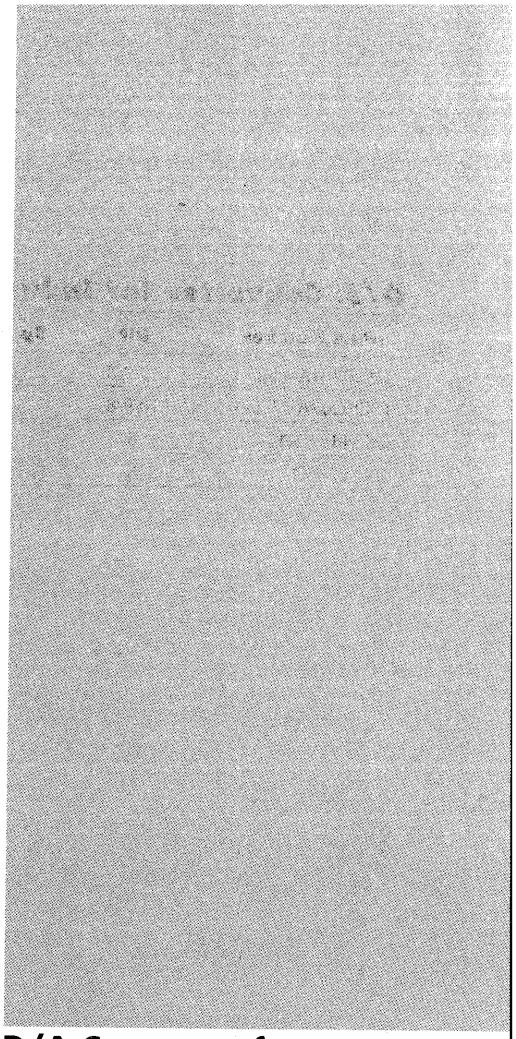
Package Outline Unit : mm

48pin QFP (Plastic) 0.7g

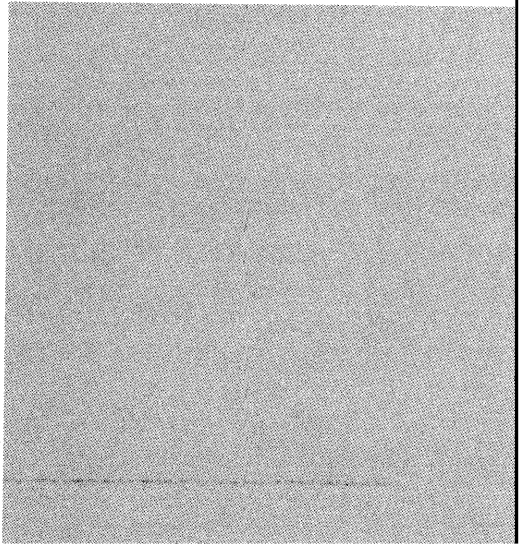


SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-8
JEDEC CODE	———

5



D/A Converter for Industries Instruments



D/A Converter for Industries Instruments

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CX20201A-1/-2/-3	10/9/8	160	420	ECL Input, 1 Channel	325-337
CX20202A-1/-2/-3	10/9/8	160	420	ECL Input, 1 Channel	325-337
CXA1156AQ	8	400	1300	ECL Input, 3 Channel	338-344
CXA1236Q	8	500	930	ECL Input, 1 Channel	355-371

10/9/8-bit 160MSPS D/A Converter

Descriptions

A series of D/A converters CX20201A/CX20202A convert binary data into an analog signal at rates higher than 160 MHz. The devices include input data registers and have a capability of driving 75 ohms load. Three versions with linearity specifications of 10, 9 or 8 bits are available for each model.

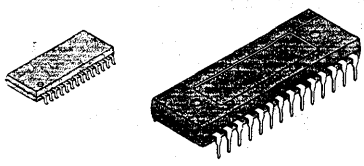
These D/A converter ICs can be used in signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems, digital measurement instruments and radars.

CX20201A-1/CX20202A-1	10-bit
CX20201A-2/CX20202A-2	9-bit
CX20201A-3/CX20202A-3	8-bit

Features

- High speed — 160 MHz
- High accuracy — 10 bit (CX20201A-1/CX20202A-1)

28pin SOP(Plastic) 28pin DIP(Plastic)

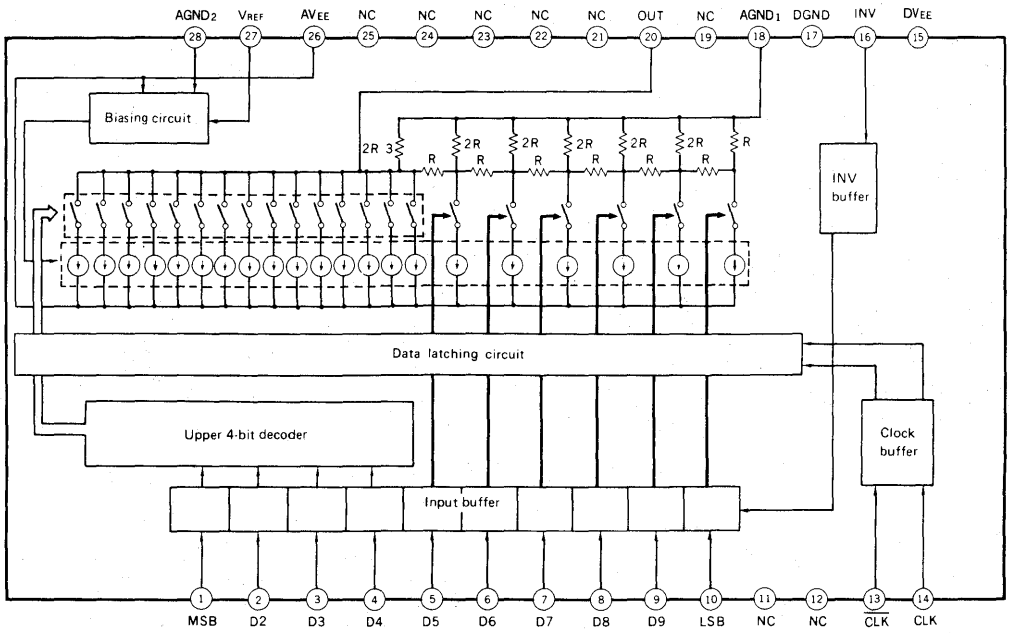


- Low glitch energy — 15 pVsec
- Low power consumption — 420 mW
- Logic invert input
- 75-Ω direct drive capability
- Analog multiplying function

Structure

Bipolar silicon monolithic IC.

Block Diagram and Pin Configuration (Top View)



6

E89667AOX-HP

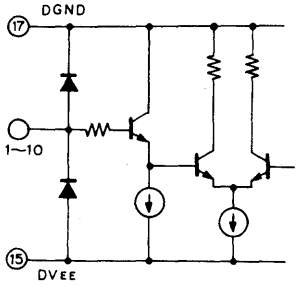
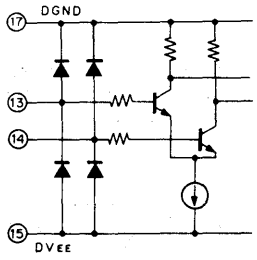
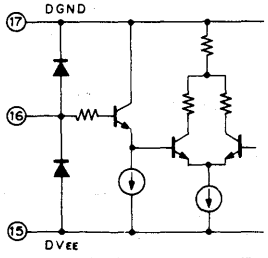
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{EE}	−7	V
• Digital input voltage	V_I	+0.3 to V_{EE}	V
• Reference input voltage	V_{REF}	+0.3 to V_{EE}	
• Analog output current	I_{OUT}	20	mA
• Operating temperature	T_{ope}	−20 to + 75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D		
CX20201A-1/-2/-3		870	mW
CX20202A-1/-2/-3		1430	mW

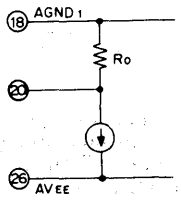
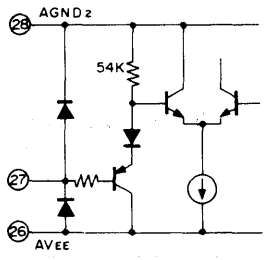
Recommended Operating Conditions

• Supply voltage	AV_{EE}, DV_{EE}	−4.75	to	−5.45	V
	AV_{EE}-DV_{EE}	−0.05	to	+0.05	V
• Digital input voltage	V_{IH}	−1.0	to	−0.7	V
	V_{IL}	−1.9	to	−1.6	V
• Reference input voltage	V_{REF}	V_{EE}+0.5	to	V_{EE}+1.4	V
• Load resistance	R_L	above 75			Ω
• Output voltage	$V_{O(FS)}$	0.8	to	1.2	V

Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 3 4 5 6 7 8 9 10	MSB D2 D3 D4 D5 D6 D7 D8 D9 LSB		Input pin for digital data. MSB and LSB are corresponded to the most significant bit and least significant bit, respectively. Pins not used should be left open or connected to DVEE.
11 12	NC		Non-connection
13 14	$\overline{\text{CLK}}$ CLK		Pins for clock inputs.
15	DVEE		Power supply pin for digital circuit.
16	INV		Code invert input pin which inverts the relationship between the binary code of digital data and D/A output voltage level.
17	DGND		Grounding pin for digital circuit.
18	AGND1		Grounding pin directly connected to the R-2R output resistor circuit network in the IC. Grounding for analog circuit system.
19	NC		Non-connection

6

No.	Symbol	Equivalent circuit	Description
20	OUT		D/A analog output.
21 22 23 24 25	NC		Non-connection
26	AVEE		Power supply pin for analog circuit.
27	VREF		Bias pin which controls D/A output range. The output scale is set by the potential difference between VREF and AVEE.
28	AGND3		Grounding pin for analog circuit system other than the R-2R output resistor circuit network in the IC

Electrical Characteristics (1) Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

CX20201A-1/CX20202A-1

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		10		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.1		+0.1	% of FS
Settling time	ts		5.2		ns

CX20201A-2/CX20202A-2

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		9		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.1		+0.1	% of FS
Settling time	ts		4.7		ns

CX20201A-3/CX20202A-3

Item	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES		8		bit
Differential linearity error	ELD	−1/2		+1/2	LSB
Linearity error	ELI	−0.2		+0.2	% of FS
Settling time	ts		4.3		ns

Electrical Characteristics (2) Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

Item		Symbol	Measuring condition*1	Min.	Typ.	Max.	Unit
Power supply current	CX20201A	I_{EE}		−60	−75	−90	mA
	CX20202A			−65	−82	−100	
Data input current (for upper 4 bits)		$I_{IH(U)}$	V_{IH} = −0.89V	0.1	1.5	6.0	μA
		$I_{IL(U)}$	V_{IL} = −1.75V	0.1	1.5	6.0	μA
Data input current (for lower 6 bits)		$I_{IH(L)}$	V_{IH} = −0.89V	0.1	0.75	3.0	μA
		$I_{IL(L)}$	V_{IL} = −1.75V	0	0.75	3.0	μA
Clock input current		I_{CLKH}	V_{IH} = −0.89V	2	23	70	μA
Invert input current		I_{INVH}	V_{IH} = −0.89V	0.1	1.5	6.0	μA
Reference input current		I_{REF}	V_{REF} = −4.58V	−3	−0.4	−0.1	μA
Output resistance		R_O	Io = −1mA	52	65	78	Ω
Maximum conversion rate		fc	R_L = 75Ω	160			MSPS
Output voltage full-scale deviation		$V_{O(FS)}$	V_{REF} = −4.58V	0.90	1.00	1.10	V
Set-up time		t_{su}		5.0			ns
Hold time		t_{hd}		1.0			ns

*1 See Figs. 3 to 5.

6

Data for Typical Application

Ta = 25°C, AVEE = DVEE = −5.2V, AGND = DGND = 0V, RL = ∞, VO(FS) = −1V

Item	Symbol	Measuring condition	Typ.	Unit
Output voltage zero offset	EZS	$R_L \geqq 10k\Omega$	−7	mV
		$R_L = 75\Omega$	−7	
Output voltage full-scale temperature coefficient	$T_{C(FS)}$	$R_L \geqq 10k\Omega$	−140	ppm/°CV
		$R_L = 75\Omega$	−580	
Output voltage zero offset temperature coefficient	$T_{C(ZS)}$	$R_L \geqq 10k\Omega$	16	μV/°C
Glitch energy	GE	Digital ramp	15	pVsec
Rise time	t_r	$R_L = 75\Omega$	1.5	ns
Fall time	t_f		1.5	ns
Propagation delay	t_d		3.8	ns
Band width for multiplying	BW_{MUL}	$R_L = 75\Omega$, −3dB	14	MHz

Timing Chart

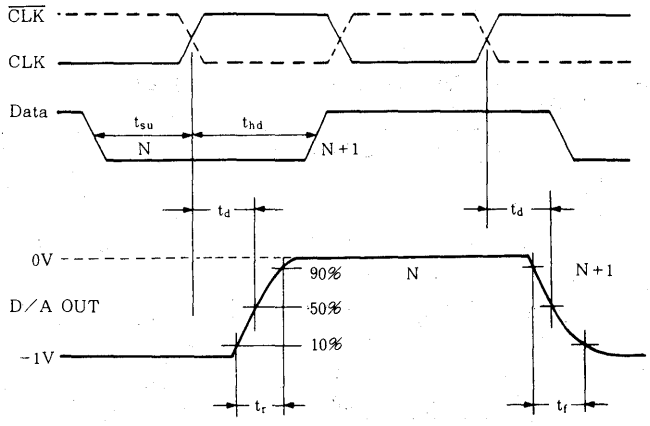


Fig. 1

Input Coding Table

Input code	Output code (V)	
	INV = 1	INV = 0
0 0 0 ····· 0 0	0	−1
0 1 1 ····· 1 1	−0.5	−0.5
1 0 0 ····· 0 0		
1 1 1 ····· 1 1	−1	0

Measuring Conditions for Current Consumption, Input Current and Output Resistance (See Fig. 2.)

Test item	Symbol	Switch condition																					Test point
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	
Current consumption	I_{EE}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b	I1
Data input current for upper 4 bits (H level)	$I_{IH(U)}$	a	b	b	b	b	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	I2
		b	a	b	b																		
		b	b	a	b																		
		b	b	b	a																		
Data input current for lower 4 bits (L level)	$I_{IL(U)}$	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	I2
		b	a	b	b																		
		b	b	a	b																		
		b	b	b	a																		
Data input current for upper 6 bits (H level)	$I_{IH(L)}$	b	b	b	b	a	b	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	I2
						b	a	b	b	b	b												
						b	b	a	b	b	b												
						b	b	b	a	b	b												
						b	b	b	b	a	b												
						b	b	b	b	b	a												
Data input current for lower 6 bits (L level)	$I_{IL(L)}$	b	b	b	b	a	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	I2
						b	a	b	b	b	b												
						b	b	a	b	b	b												
						b	b	b	a	b	b												
						b	b	b	b	a	b												
						b	b	b	b	b	a												
Clock input current (H level)	I_{CLKH}	b	b	b	b	b	b	b	b	b	b	b	a	b	b	a	b	b	b	b	b	b	I3
Clock-bar input current (H level)	$I_{\overline{CLK}H}$	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	b	b	b	b	I4
Invert input current (H level)	I_{INVH}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	b	b	I5
Referecnce input current	I_{REF}	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	I6
Output resistance	R_O	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	a	a	b	V1

Electrical Characteristics Test Circuit

Test Circuit for Current Consumption, Input Current and Output Resistance

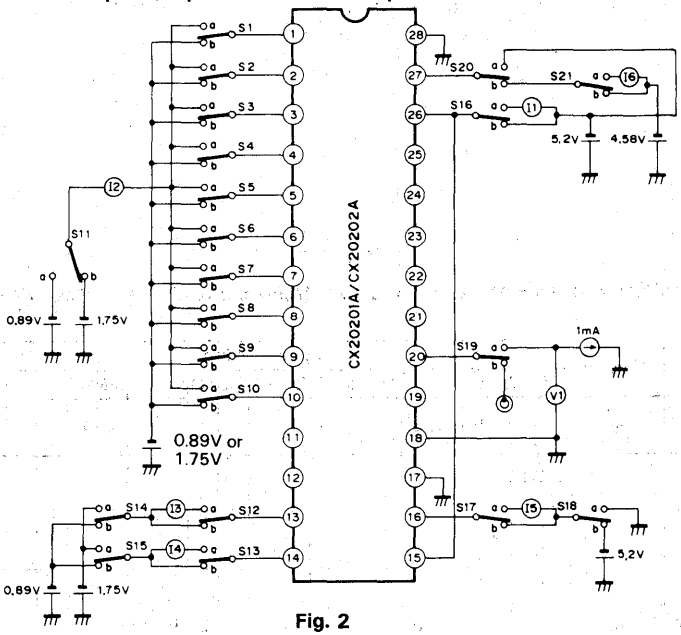
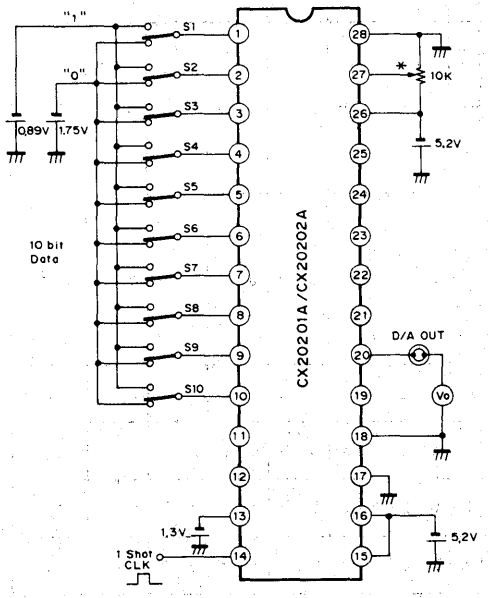


Fig. 2

Test Circuit for Differential Linearity Error and Linearity Error



* Adjust so that the full scale of DC voltage at Pin 20 becomes 1.023V, that is, to satisfy $V_0 - V_{1023} = 1.023V$.

Fig. 3

Linearity errors are measured as follows.

S1	S2	S3	·····	S9	S10	D/A out
0	0	0	·····	0	0	V_0
0	0	0	·····	0	1	V_1
0	0	0	·····	1	0	V_2
⋮						⋮
1	1	1	·····	1	1	V_{1023}

Linearity error	Differential linearity error
V_0	
V_1	$V_1 - V_0$
V_2	$V_2 - V_1$
V_4	$V_4 - V_3$
V_8	$V_8 - V_7$
V_{16}	$V_{16} - V_{15}$
V_{32}	$V_{32} - V_{31}$
V_{64}	$V_{64} - V_{63}$
V_{128}	$V_{128} - V_{127}$
V_{192}	$V_{192} - V_{191}$
⋮	⋮
V_{960}	$V_{960} - V_{959}$
V_{1023}	

Errors at individual measurement points are calculated according to the following definition.

$(V_{1023} - V_0)/1023 = V_{O(FS)}/1023 \equiv 1$ LSB.

Test circuits for
- Maximum conversion rate
- Rise time
- Fall time
- Propagation delay
- Set-up time
- Hold time
- Settling time

DL: delay line (ELMEC VDS1110)
Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

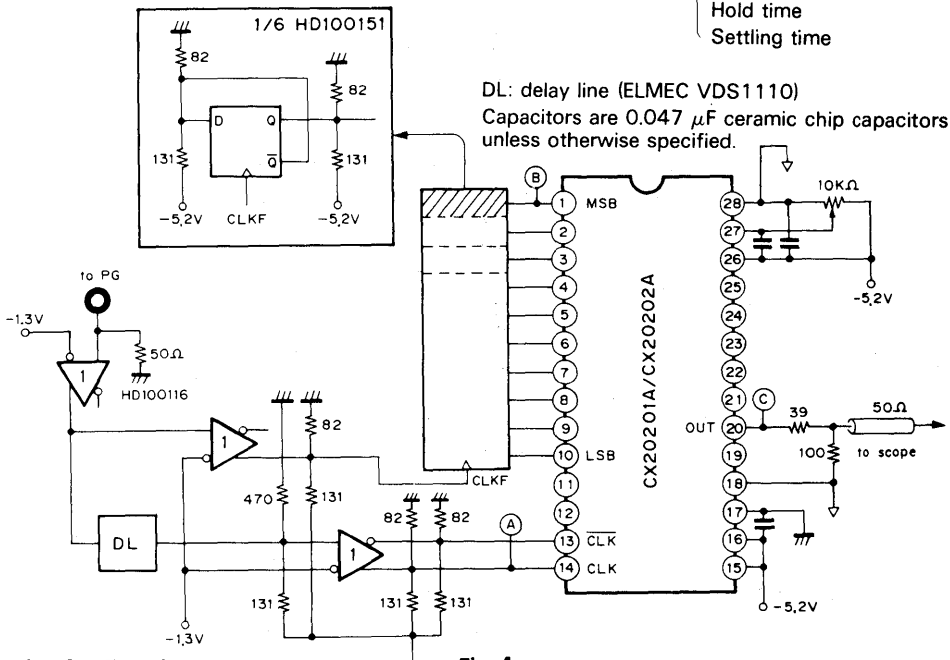


Fig. 4

Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{O(FS)}$ as shown in the D/A output waveform in Fig. 5 is expressed as

$V = V_{O(FS)} (1 - e^{-t/\tau})$.

The settling time for respective accuracy of 10 , 9 and 8-bit is specified as

$V = 0.9995\ V_{O(FS)}$
$V = 0.999\ V_{O(FS)}$
$V = 0.998\ V_{O(FS)}$

which results in the following:

$t_s = 7.60\tau$ for 10-bit,
$t_s = 6.93\tau$ for 9-bit, and
$t_s = 6.24\tau$ for 8-bit

Rise time (t_r) and fall time (t_f) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{O(FS)}$):

$V = 0.1\ V_{O(FS)}$
$V = 0.9\ V_{O(FS)}$

and calculated as $t_r = t_f = 2.20\ \tau$.
The settling time is obtained by combining these expressions:

$t_s = 3.45 t_r$ for 10-bit,
$t_s = 3.15 t_r$ for 9-bit, and
$t_s = 2.84 t_r$ for 8-bit

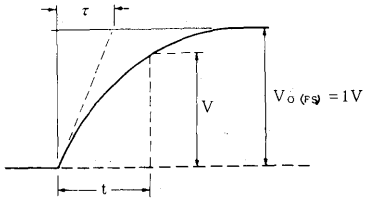


Fig. 5

6

Test Circuit for Multiplying Band Width

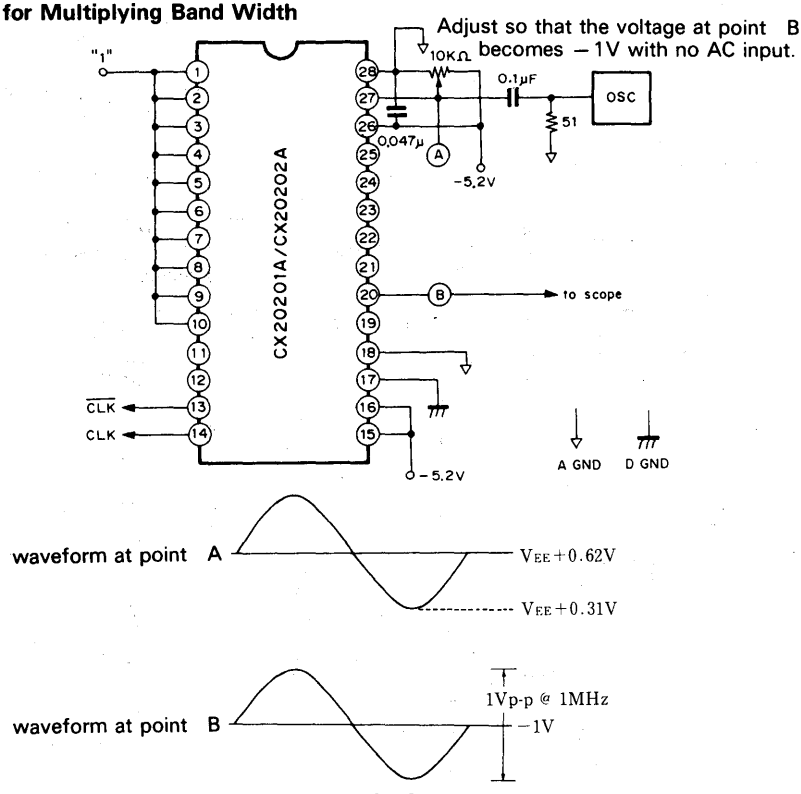
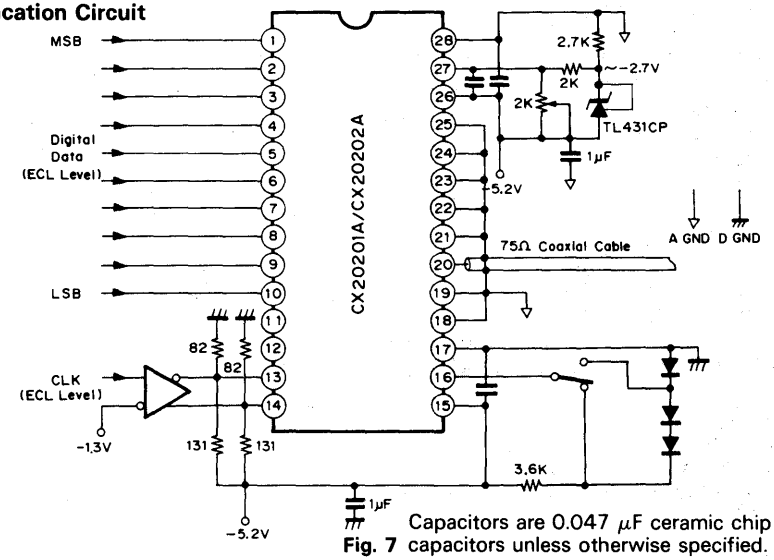


Fig. 6

Typical Application Circuit



Capacitors are 0.047 μF ceramic chip capacitors unless otherwise specified.

Fig. 7

Notes on Applications

(1) Setting of full-scale output voltage

The full-scale output voltage ($V_{O(FS)}$) is set by the pin 27 (V_{REF}). $V_{O(FS)}$ varies in proportion to the voltage difference between pin 27 and pin 26 (AV_{EE}) as shown in Fig. 9.

$V_{O(FS)}$ can be set by simply dividing the supply voltage using resistors as shown in Fig. 8, but in this simple set up the voltage deviation of the supply voltage result in a deviation of $V_{O(FS)}$. This influence can be avoided by using a stabilization circuit as shown in Fig. 7 to allow stable full-scale output.

Pin 27 (V_{REF}) should be stabilized against high-frequency noise by sufficient by passing using a capacitor with low lead inductance such as ceramic chip capacitors. The stabilization capacitor should be inserted between pin 27 (V_{REF}) and pin 26 (AV_{EE}) as $V_{O(FS)}$ is direct proportion to the voltage across these two terminals.

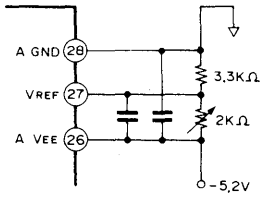


Fig. 8

(2) Noise reduction

An external digital noise should be minimized because the system handles small analog voltage (1 LSB corresponds 1 mV of analog output voltage for 10 bit resolution). Refer to the following notes to minimize the system noise contamination.

- Ground plane and V_{EE} plane on a printed circuit board should be made as wide as possible to reduce parasitic inductance and resistance.
- The patterns AGND and DGND should be separated on the printed circuit board. AV_{EE} and DV_{EE} should be separated too. The connections between analog system and digital system are to be made at the I/O ports of the printed circuit board.
- AV_{EE} and DV_{EE} should be bypassed to respective GND by using a tantalum capacitor of 1 μF and a ceramic chip capacitor of 47μF positioned as close as to terminals of the IC.
- Pins not in sure are to be connected to the ground plane.

(3) Load resistance and temperature coefficient

Temperature coefficient of the full-scale output voltage and zero offset voltage depend on the load resistance (value and type). Generally, the larger the load resistance the better the temperature coefficient value. Temperature characteristics at $R_L \geqq 10\ k\Omega$ and $R_L = 75\ \Omega$ are shown in Fig. 10.

(4) Input data and internal latching circuit

CX20201A/CX20202A incorporates a latching circuit as shown in the block diagram. This latching circuit has a two-stage configuration (master-slave type) and fetches input data only at the rising edge of the clock; the output is not affected by the changes in input data at any other timings. This mechanism allows stable operation against any changes in input data at any timings, except for the set-up time immediately before and the hold time immediately after the clock change from L to H.

(5) Driving input data and clock

CX20201A/CX20202A are designed to be operated at very high speed. It is, therefore, necessary to drive it with a high-speed ICs such as an ECL100K for full performance. Also the output port of the data and clock drivers should be terminated with 50-Ω systems. See Figs. 4 and 7.

6

$V_{O(FS)}$ Ratio vs. (V_{REF}-V_{EE})

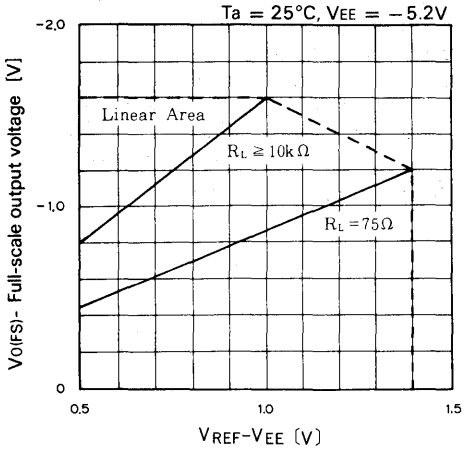


Fig. 9

Full-scale Output Voltage vs. Ambient Temperature

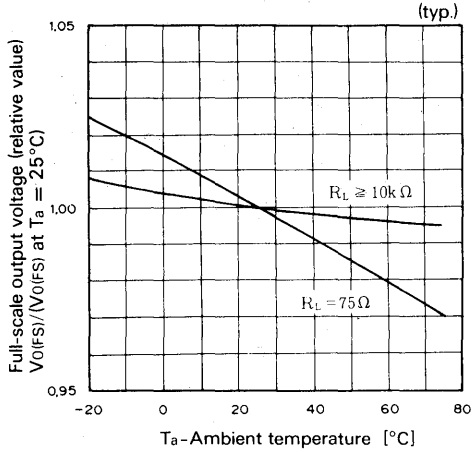


Fig. 10

Outbut Characteristics vs. Multiplying Input Signal Frequency

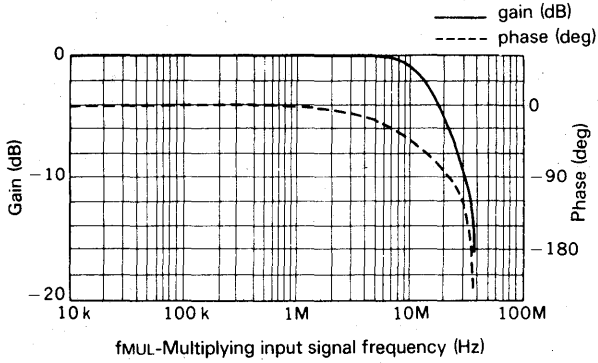


Fig. 11

Glitch Energy vs. Case Temperature (Full Scale−1023mV)

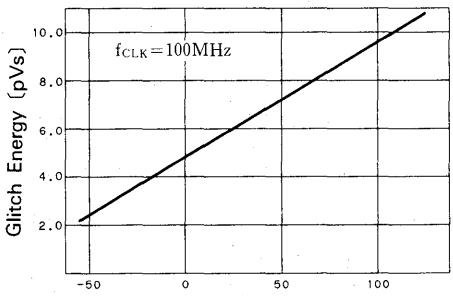
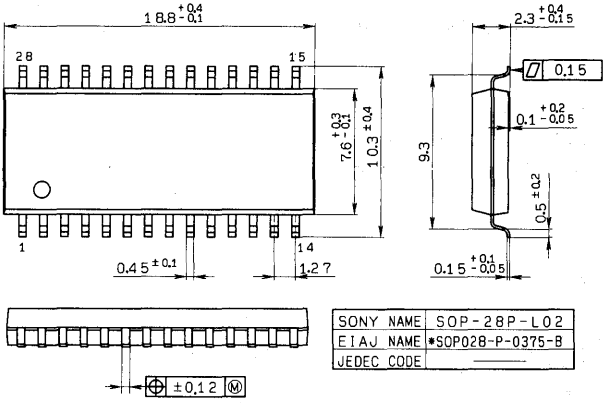


Fig. 12

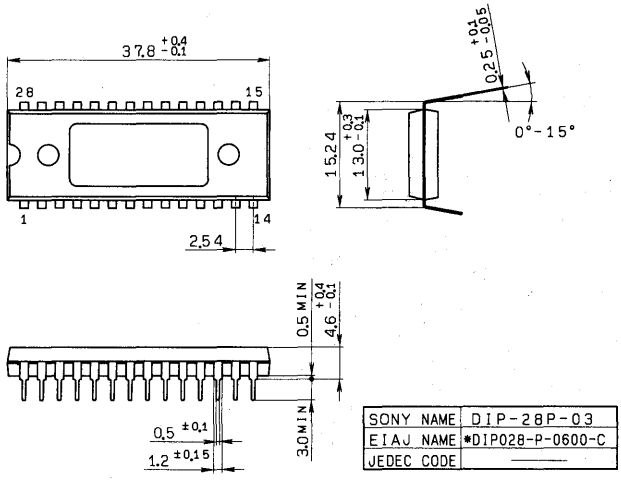
Package Outline Unit : mm

CX20201A 28pin SOP(Plastic) 375mil 0.6g



SONY NAME	SOP-28P-L02
EIAJ NAME	*SOP028-P-0375-B
JEDEC CODE	

CX20202A 28pin DIP(Plastic) 600mil 4.2g



SONY NAME	DIP-28P-03
EIAJ NAME	*DIP028-P-0600-C
JEDEC CODE	

6

SONY

CXA1156AQ

8-bit 400MSPS Triple VIDEO D/A Converter

Description

The CXA1156AQ is an 8-bit high-speed D/A converter with input/output of 3 channels for RGB.

This IC achieves maximum conversion rate of 400MSPS, and is suitable for signal processing applications requiring high speed and resolution such as high resolution monitors and high definition video systems.

44 pin QFP (Ceramic)

Features

- High speed: 400MSPS
- High resolution: 8-bit RGB
- Low power consumption: 1.3W (at V_{EE}=–4.5V)
- Video control inputs: Sync, Blank, Overlay
- ECL 100K and 10K compatible inputs
- 25Ω , 37.5Ω load driving capability
- Differential current output
- RS-343A compatible output

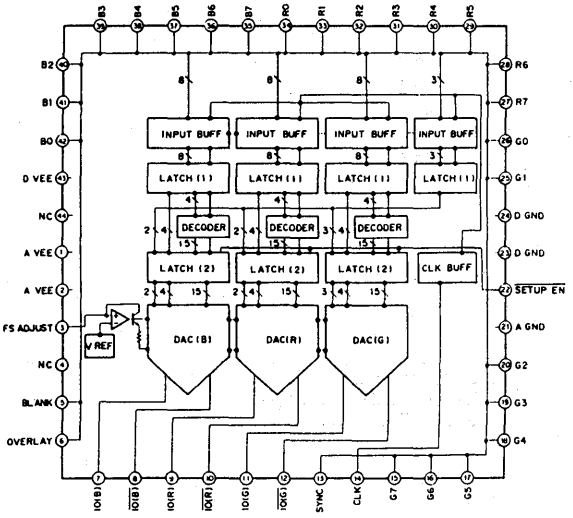
Function

8-bit 400MSPS triple video D/A converter

Structure

Bipolar silicon monolithic IC

Block Diagram/Pin Configuration



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5	V
• Input voltage (digital)	V_I	DV_{EE} to +0.5	V
(FS. ADJ. pin)	V_{REF}	AV_{EE} to +0.5	V
• Input current (FS. ADJ. pin)	I_{REF}	2.0	mA
• Output voltage	V_O	−2.0 to +2.0	V
• Output current	I_O	50	mA
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	P_D	1.3	W

Operating Conditions

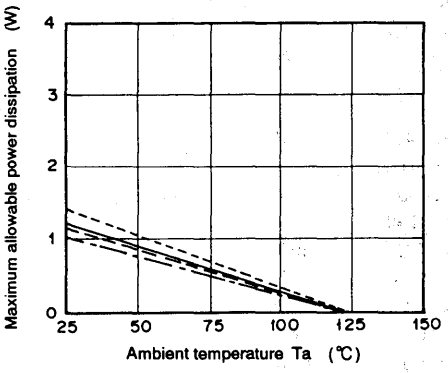
• Supply voltage	AV_{EE}, DV_{EE}	−4.8 to −4.2	V
	AV_{EE}-DV_{EE}	−0.05 to +0.05	V
• Digital input voltage	V_{IH}	−1.05 to −0.7	V
	V_{IL}	−1.9 to −1.49	V
• Reference current	I_{REF}	0.5 to 1.9	mA
• Load resistance	R_L	25 to 37.5	Ω
• Output voltage	V_O (FS.)	0.8 to 1.2	V
• CLK pulse width	tpw_1	1.2 (Min.)	ns
	tpw_0	1.2 (Min.)	ns
• Operating temperature	Tc	−20 to 70	°C

6

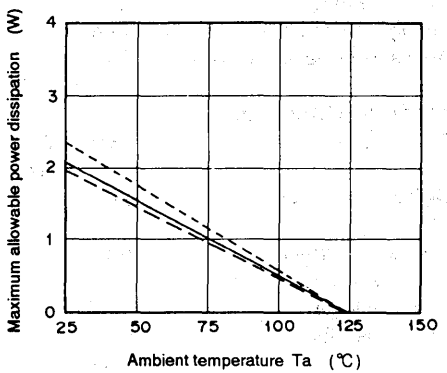
Maximum Allowable Power Dissipation vs. Ambient Temperature

--------- With fin 2290C (*)
——— With fin 2285C (*)
- - - - - - Without fin
—·—·— When not mounted

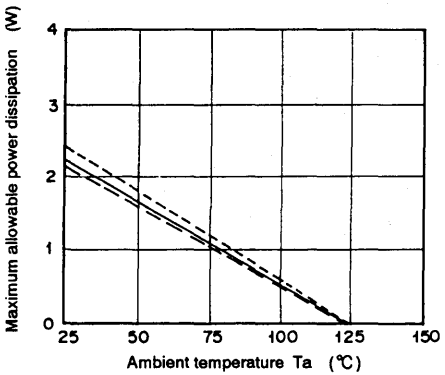
} When mounted on a board (**)



(a) In Still Air



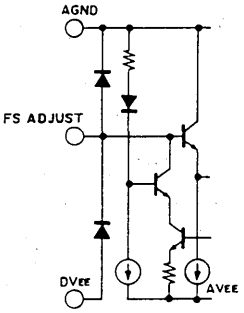
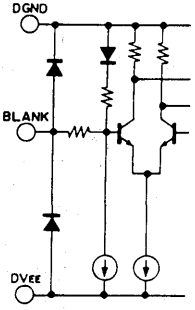
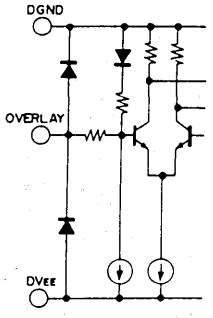
(b) Air Flow Rate 1.5m/sec



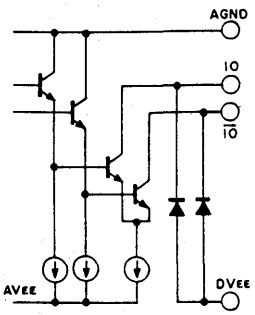
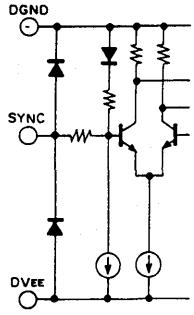
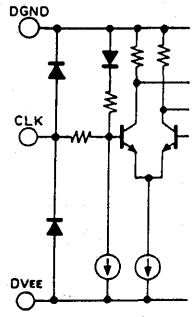
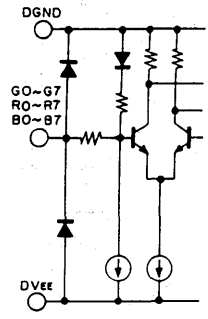
(c) Air Flow Rate 3.0m/sec

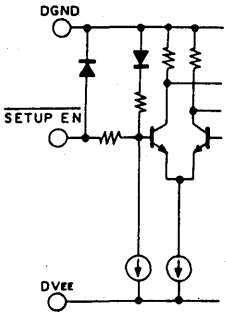
* Manufactured by Thermalloy Inc.
** PCB area 20 × 10 × 1.6mm
1-sided glass fiber epoxy board with 30% copper foil area

Pin Description and Input/Output Equivalent Circuit

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 2	AVEE	–4.5V (typ.)		Analog power supply.
3	FS ADJUST	–1.3V (typ.)		Controls full-scale level for the D/A converter output. Output current can be adjusted by the resistor value externally connected between this pin and AGND. See the section on Description of Operation for details on how the external resistance should be selected.
4	NC			Unconnected pin. Leave this pin open.
5	BLANK	ECL		Control input for "blank". Setting the input to "1" fixes the D/A output to BLANK level regardless of input data for gray level. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)
6	OVERLAY	ECL		Control input for "overlay". Setting the input to "1" enhances the D/A output to level of 10% brighter than WHITE level regardless of input data for gray level. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)

6

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7, 8 9, 10 11, 12	IO (B), $\overline{IO\ (B)}$ IO (R), $\overline{IO\ (R)}$ IO (G), $\overline{IO\ (G)}$	0 to –1071mV (typ.)		Complementary analog current outputs for red, green and blue (RGB). Output voltages are acquired when they are connected to external pull-up resistors.
13	SYNC	ECL		Control input for "composite sync". This functions only for IO (G), $\overline{IO}$ (G) output. Setting the input to "1" fixes the D/A output to SYNC level regardless of input data for gray level. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)
14	CLK	ECL		Clock input. All data and control inputs are latched by the rising edge of CLK. When the pin is left open, it functions as when it is set to "0".
26, 25 20 to 15	G0 to G7	ECL		Digital input for gray level. G0 (LSB) to G7 (MSB) input for GREEN. R0 (LSB) to R7 (MSB) input for RED. B0 (LSB) to B7 (MSB) input for BLUE. When the pin is left open, it functions as when it is set to "0". (See Input / Output Table)
34 to 27	R0 to R7			
42 to 35	B0 to B7			

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	AGND	GND		Analog GND. Separated from DGND.
22	$\overline{\text{SETUP EN}}$			Setting this pin to "1" or DGND makes BLANK level equal to BLACK level. Setting this pin to "0" or open makes BLANK level lower than BLACK level by 7.5IRE. (see Fig. 1 to 4)
23, 24	DGND	GND		Digital GND. Separated from AGND.
43	DV_{EE}	–4.5V (typ.)		Digital power supply. Separated from AV_{EE}.
44	NC			Unconnected pin.

6

Electrical Characteristics

(AV_{EE}=DV_{EE}=–4.5V, Ta=25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		8	8	8	bit
Integral linearity error	E_L	V_{FS}=661mV			± 1/2	LSB
Differential linearity error	E_D				± 1/2	LSB
Digital input current	I_{IH}	V_{IN}=–0.7V	0		180	µA
	I_{IL}	V_{IN}=–1.9V	–100		100	µA
Digital input capacitance	C_{IN}			5		pF
Maximum output current	Io		48			mA
Output compliance voltage	Voc		–1.2		1.5	V
Output resistance	Ro			50		kΩ
Output capacitance	Co			10		pF
Output current						
Full gray scale error	E_{FS}	V_{FS}=661mV	–10	0	10	% of Gray Scale
Full gray scale balance (G, R, B) (Note 1)	E_{FSB}		0	0.5	2.5	% of Gray Scale
Full gray scale temperature coefficient	T_{CFS}			+0.06		% of Gray Scale/°C
Offset current	I_{OF}		0		40	µA
Power supply current	I_{EE}		–430	–310	–200	mA
Maximum conversion rate	$F_{S\,MAX}$		400			MSPS
Set-up time (Note 2)	ts	Digital input/clock threshold voltage =–1.3V R_L=25Ω	1.0			ns
Hold time (Note 2)	th		0.6			ns
Output rise time	tr			0.5	0.9	ns
Output fall time	tf			0.5	0.9	ns
Output delay	td		2.1	2.8	3.4	ns
Output pipeline delay	t_{PLD}		1	1	1	Clock

Note 1) E_{FSB}=Max {|V_{FS} (G) –V_{FS} (R)|, |V_{FS} (R) –V_{FS} (B)|,|V_{FS} (B) –V_{FS} (G)|}
÷ [{V_{FS} (G) +V_{FS} (R) +V_{FS} (B)}/3] × 100
V_{FS} is full gray scale that is voltage difference between WHITE and BLACK level.

Note 2) Specified at –20 ≦ Tc ≦ 70°C

Description of Operation (See Block Diagram / Pin Configuration)

Each of RGB DATA (R0 to R7, G0 to G7, B0 to B7) and CONTROL signals (SYNC, BLANK, OVERLAY) are caught at the rising edge of CLK by LATCH (1).

The upper 4 bits of each DATA, which have been decoded into thermometer code in DECODER section, are transferred to DAC section via LATCH (2), together with the lower 4 bits and CONTROL signals.

DAC section creates analog current output composing of the following portions:

- Weighted lower 4-bit current
- Thermometer-coded upper 4-bit current
- Function output current

The output appears delayed by 1clock after the rising edge of CLK.

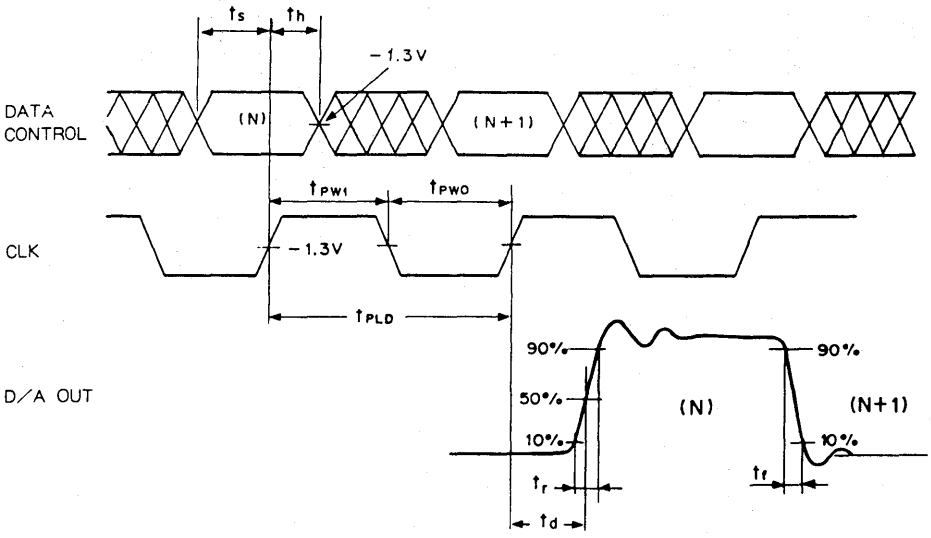
This analog current output is converted to voltage output by load resistor RL that is connected to the output pin.

Output full scale adjustment is possible by setting the value of Rset (shown in the formula below) located between FS ADJUST pin and AGND. The FS ADJUST voltage is produced by an internal band-gap voltage source.

$$Rset = \frac{V_{ADJ}}{\frac{V_{FS}}{R_L} \times \frac{16}{255}} \ [\Omega]$$

Here, V_{FS} represents typical voltage difference between WHITE level and BLACK level. V_{ADJ} is voltage at FS ADJUST pin.

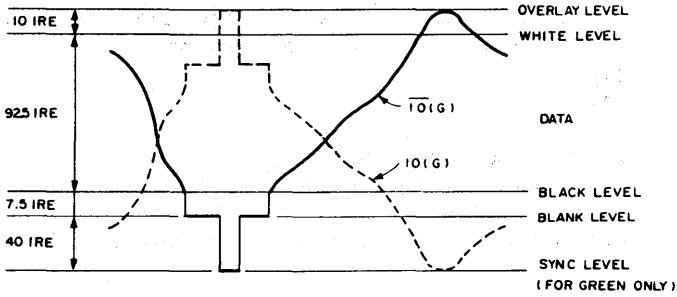
For instance, Rset is approximately 750Ω for V_{FS}=661mV.



Timing Diagram

Output Levels (With SETUP function)

$\overline{IO}$ (G) (mA)	$\overline{VO}$ (G) (V)
0.00	0.000
–2.84	–0.071
–29.28	–0.732
–31.42	–0.785
–42.84	–1.071



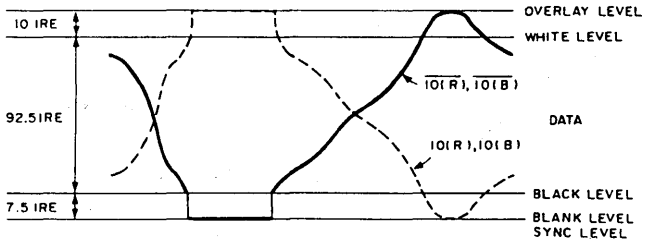
* In case of doubly-terminated 50 Ω load.

Fig. 1. Composite Video Output Level (GREEN)

	$\overline{IO}$ (G) (mA)	IO (G) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	–42.84	0	1	0	0	X X X X X X X X
WHITE	–2.84	–40.00	0	0	0	0	1 1 1 1 1 1 1 1
DATA			0	0	0	0	data
BLACK	–29.28	–13.56	0	0	0	0	0 0 0 0 0 0 0 0
BLANK	–31.42	–11.42	0	X	0	1	X X X X X X X X
SYNC	–42.84	0.00	0	X	1	X	X X X X X X X X

Table 1. Input/Output Table (GREEN)

$\overline{IO(R)}$, $\overline{IO(B)}$ (mA)	$\overline{VO(R)}$, $\overline{VO(B)}$ (V)
0.00	0.000
−2.84	−0.071
−29.28	−0.732
−31.42	−0.785



* In case of doubly-terminated 50 Ω load.

Fig. 2. Composite Video Output Level (RED, BLUE)

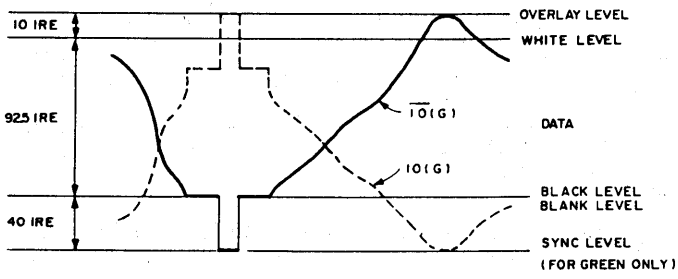
	$\overline{IO(R)}$, $\overline{IO(B)}$ (mA)	IO (R), IO (B) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	−31.42	0	1	0	0	X X X X X X X X
WHITE	−2.84	−28.58	0	0	0	0	1 1 1 1 1 1 1 1
DATA			0	0	0	0	data
BLACK	−29.28	−2.14	0	0	0	0	0 0 0 0 0 0 0 0
BLANK	−31.42	0.00	0	X	0	1	X X X X X X X X
SYNC	−31.42	0.00	0	X	1	X	X X X X X X X X

Table 2. Input/Output Table (RED, BLUE)

6

Output Levels (Without SETUP function)

$\overline{IO}$ (G) (mA)	$\overline{VO}$ (G) (V)
0.00	0.000
–2.84	–0.071
–29.28	–0.732
–40.70	–1.018



* In case of doubly-terminated 50 Ω load.

Fig. 3. Composite Video Output Level (GREEN)

	$\overline{IO}$ (G) (mA)	IO (G) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	–40.70	1	1	0	0	X X X X X X X X
WHITE	–2.84	–37.86	1	0	0	0	1 1 1 1 1 1 1 1
DATA			1	0	0	0	data
BLACK	–29.28	–11.42	1	0	0	0	0 0 0 0 0 0 0 0
BLANK	–29.28	–11.42	1	X	0	1	X X X X X X X X
SYNC	–40.70	0.00	1	X	1	X	X X X X X X X X

Table 3. Input/Output Table (GREEN)

$\overline{IO(R)}$, $\overline{IO(B)}$ (mA)	$\overline{VO(R)}$, $\overline{VO(B)}$ (V)
0.00	0.000
− 2.84	− 0.071
− 29.28	− 0.732

* In case of doubly-terminated 50 Ω load.

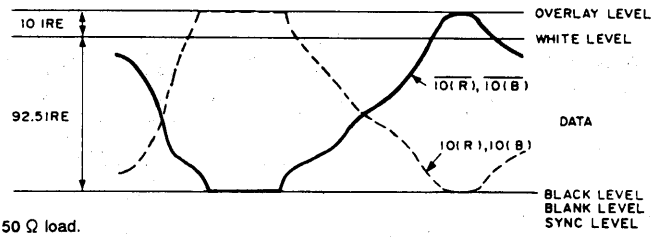


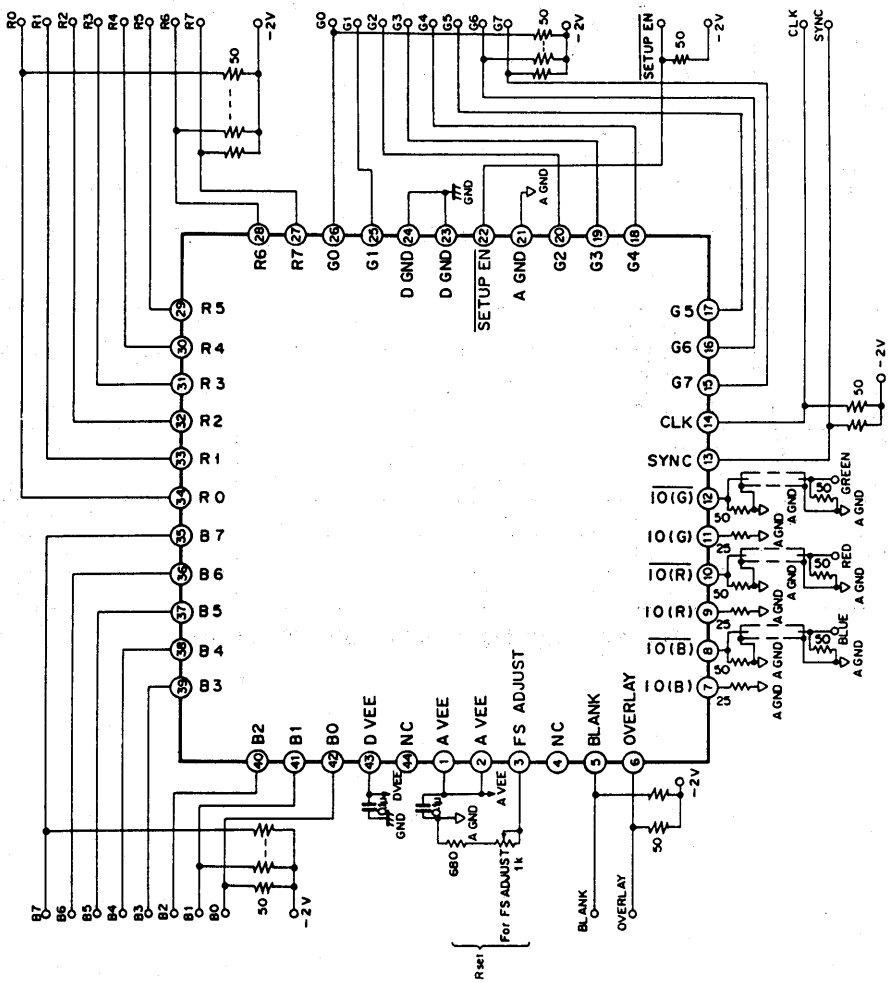
Fig. 4. Composite Video Output Level (RED, BLUE)

	$\overline{IO(R)}$, $\overline{IO(B)}$ (mA)	IO (R), IO (B) (mA)	$\overline{SETUP\ EN}$	OVERLAY	SYNC	BLANK	D/A Input Data
OVERLAY	0.00	−29.28	1	1	0	0	× × × × × × × ×
WHITE	−2.84	−26.44	1	0	0	0	1 1 1 1 1 1 1 1
DATA			1	0	0	0	data
BLACK	−29.28	0.00	1	0	0	0	0 0 0 0 0 0 0 0
BLANK	−29.28	0.00	1	×	0	1	× × × × × × × ×
SYNC	−29.28	0.00	1	×	1	×	× × × × × × × ×

Table 4. Input/Output Table (RED, BLUE)

6

Application Circuit (In case of using 50Ω coaxial cable for output)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

(1) Wiring for Digital Inputs

- All digital inputs are single-ended and ECL compatible. For high-speed operation, it is recommended that line characteristic impedance and termination resistance should be set at 50Ω. The line termination resistors should be placed nearest to the IC input pins.

(2) Noise Reduction Measures

- Use as wide GND plane as possible to reduce parastic inductance and resistance on the board.
- It is advisable to separate AGND and DGND on the board. This also applies for AV_{EE} and DV_{EE}. Also, the connections between AGND and DGND, AV_{EE} and DV_{EE} should respectively be made at the board connector section (entrance/exit of the board).
- AV_{EE} and DV_{EE} pins should be bypassed to AGND/DGND planes of the board as close as possible to the IC, via capacitors of approximately 0.1 µF. Ceramic chip capacitors are recommended.
- V_{TT} (–2V) that is connected with termination resistors should be bypassed to DGND plane via capacitors of approximately 0.1 µF. The capacitors should be located nearest to the termination resistors. Ceramic chip capacitors are recommended.
- An external resistor Rset should be connected as close as possible both to FSADJ pin and AGND. The lead length of the resistor and the pattern length on the board should be as short as possible, in order to minimize noise effect. Also, any capacitors should not be connected with FSADJ pin.

(3) Analog Output Processing

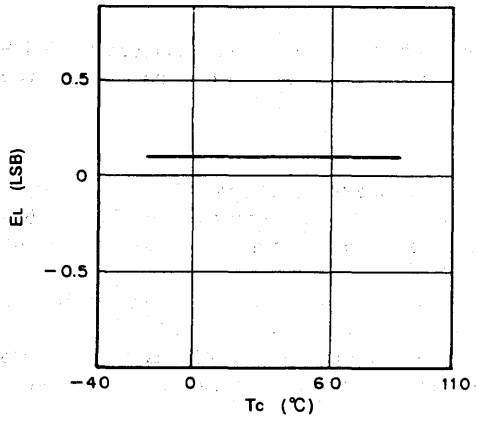
This D/A converter is designed so that it is possible to directly drive 50Ω and 75Ω lines. In order to ensure line matching, it is necessary to terminate both ends of the line with 50Ω (or 75Ω), as indicated in Application Circuit.

In addition, even if some of the following outputs IO (G), $\overline{\text{IO (G)}}$, IO (R), $\overline{\text{IO (R)}}$, IO (B), $\overline{\text{IO (B)}}$ are not used, do not leave the pins open, and be sure to connect them to AGND via 25Ω or directly.

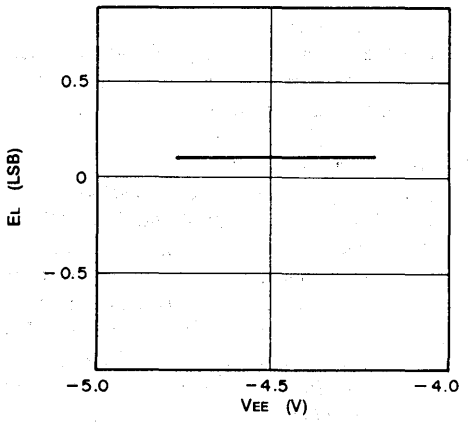
6

Typical Characteristics

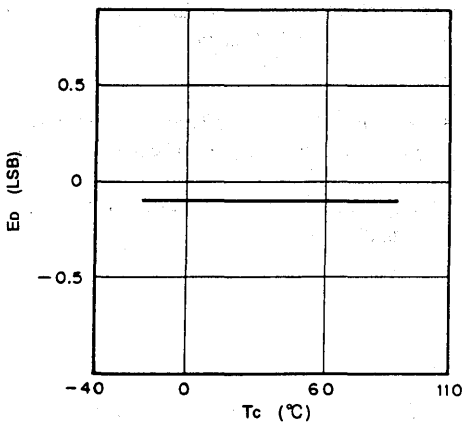
Integral linearity error vs. Tc



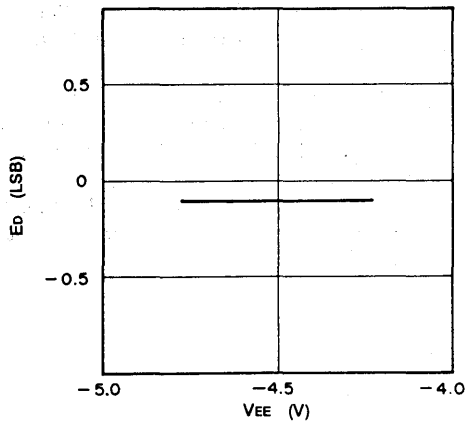
Integral linearity error vs. Supply voltage



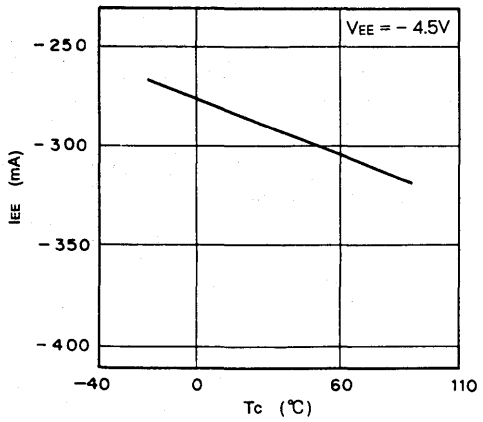
Differential linearity error vs. Tc



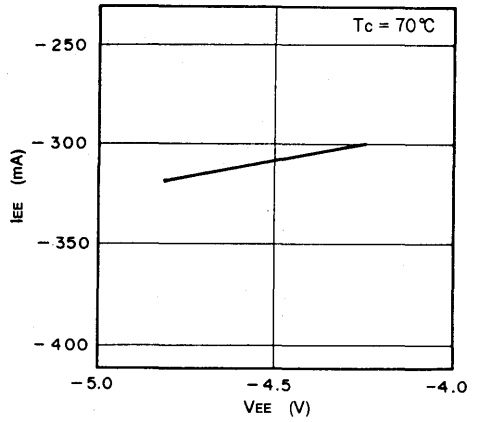
Differential linearity error vs. Supply voltage



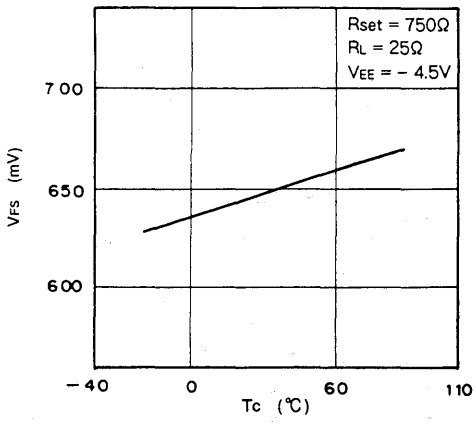
Power supply current vs. Tc



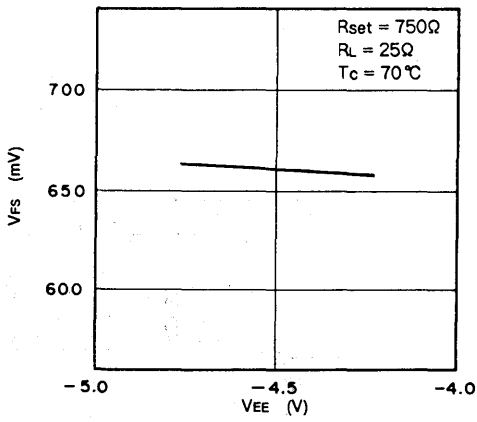
Power supply current vs. Supply voltage



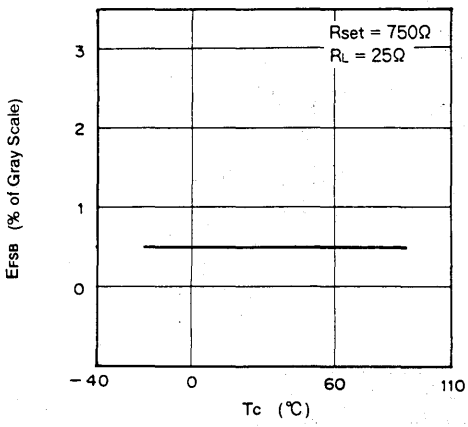
Full gray scale vs. Tc



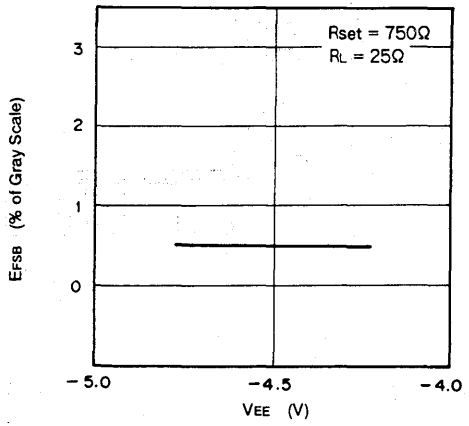
Full gray scale vs. Supply voltage



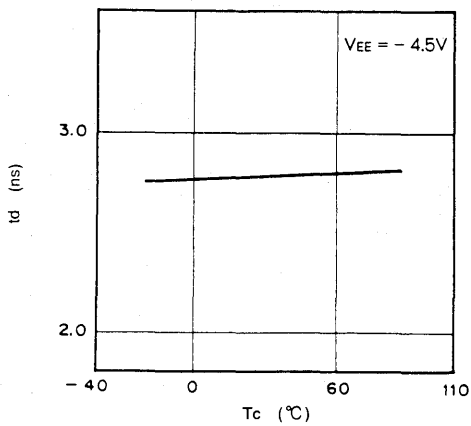
Full gray scale balance vs. Tc



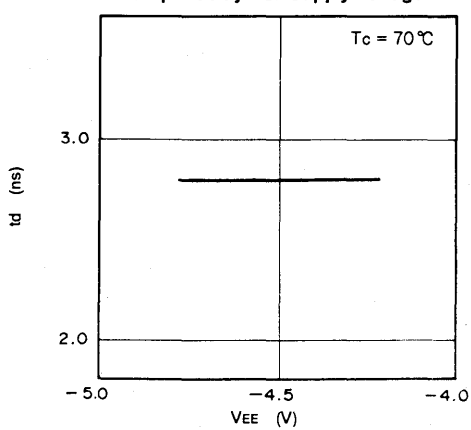
Full gray balance vs. Supply voltage



Output delay vs. Tc



Output delay vs. Supply voltage

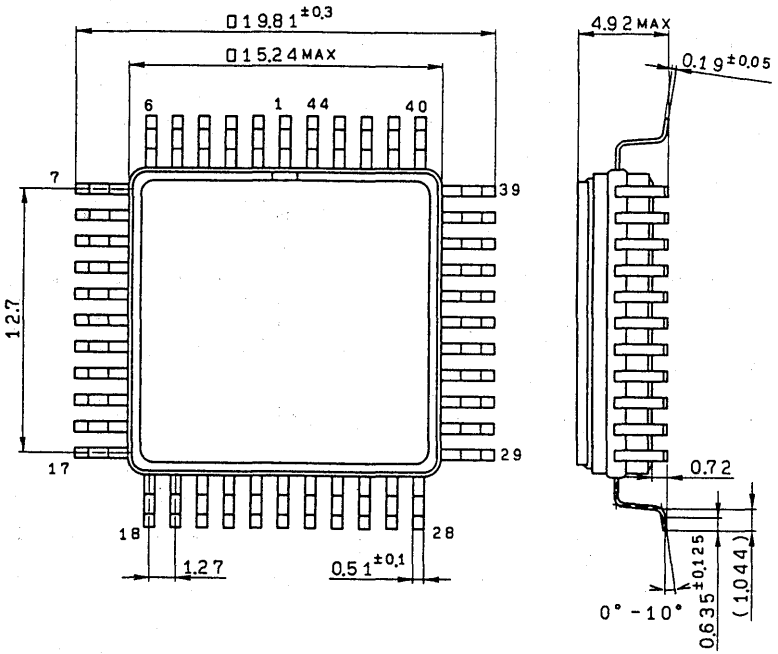


6

Package Outline

Unit : mm

44pin QFP (Ceramic)



SONY NAME	QFP-44C-L01
EIAJ NAME	XQFP044-G-0000-A
JEDEC CODE	MO-084-AB *

* (Similar)

SONY

CXA1236Q

8bit 500MSPS Single VIDEO DAC (ECL input)

Description

The CXA1236Q is an ultra high-speed D/A converter that multiplexes two 8-bit input data.

This IC realizes a maximum conversion speed of 500MSPS and is suitable for signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems and others.

44 pin QFP (Ceramic)

Features

- Ultra high-speed
  : 500MSPS, multiplexed input
- High resolution: 8bit
- Low power consumption
  : 1W (for $V_{EE} = -4.5V$)
- Video control input
  : Sync, Blank, Ref. White, Bright
- ECL 100K and 10K compatible input
- Can drive 25Ω, 37.5Ω, 50Ω, and 75Ω loads
- Differential current output
- RS-343A compatible output
- −5.5 to −4.2V range single power supply operation

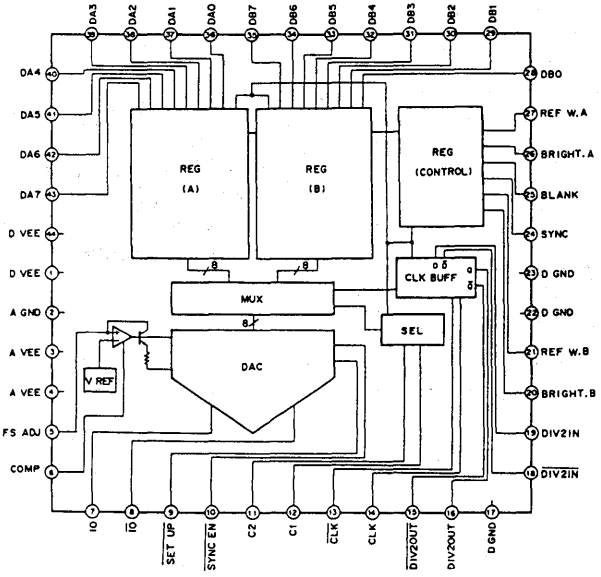
Functions

8bit 500MSPS Single VIDEO D/A Converter

Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration (Top View)



6

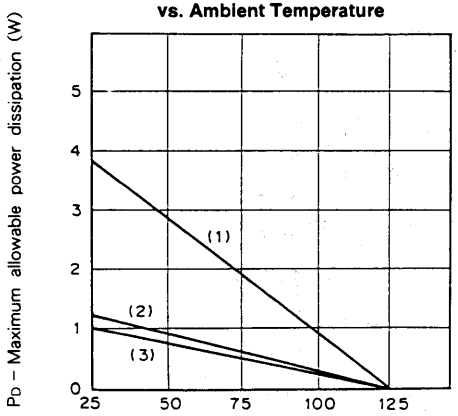
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	− 7 to + 0.5	V
• Input voltage (digital)	V_I	DV_{EE} to + 0.5	V
(FS ADJ pin)	V_{REF}	AV_{EE} to + 0.5	V
• Input current (FS ADJ pin)	I_{REF}	2.0	mA
• Output voltage	V_O	− 2.0 to + 2.0	V
• Output current	I_O	50	mA
• Storage temperature	Tstg	− 65 to + 150	°C
• Allowable power dissipation	P_D	1.3	W

Operating Conditions

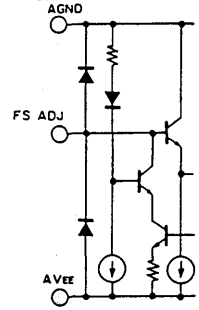
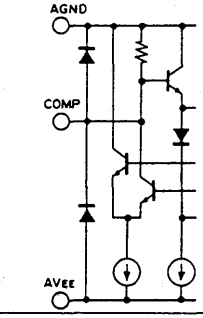
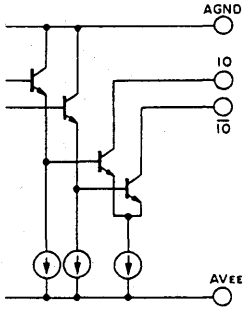
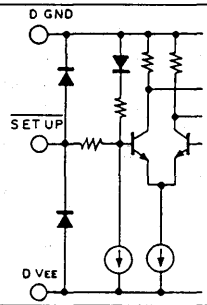
• Supply voltage		AV_{EE}, DV_{EE}	− 5.5 to − 4.2	V
		$AV_{EE} - DV_{EE}$	− 0.05 to + 0.05	V
• Digital input voltage		V_{IH}	− 1.05 to − 0.7	V
		V_{IL}	− 1.9 to − 1.49	V
• Reference current		I_{REF}	0.5 to 1.7	mA
• Load resistance		R_L	25 to 75	Ω
• Output voltage		V_O (FS.)	0.8 to 1.2	V
• CLK pulse width	MUX (1) mode	t_{PW1}	0.9 (Min.)	ns
		t_{PW0}	0.9 (Min.)	ns
	MUX (2) mode	t_{PW1}	1.8 (Min.)	ns
	SELECT mode	t_{PW0}	1.8 (Min.)	ns
• Operating temperature		Tc	− 55 to 70	°C

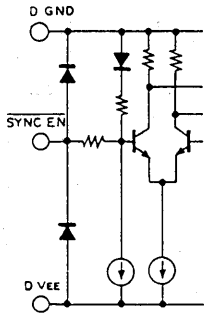
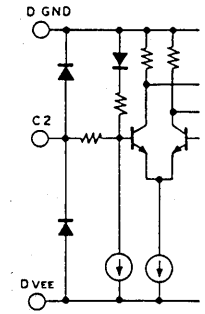
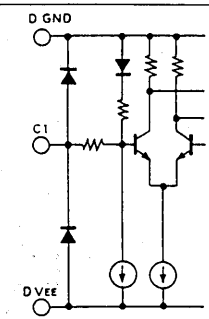
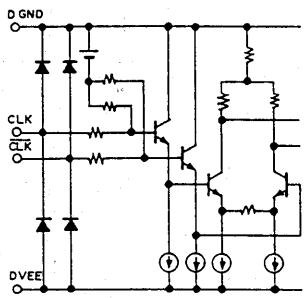
Maximum allowable Power Dissipation vs. Ambient Temperature

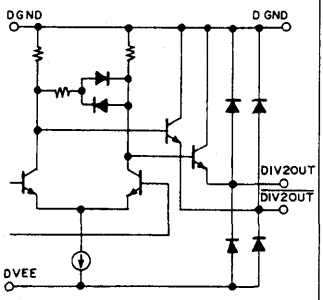
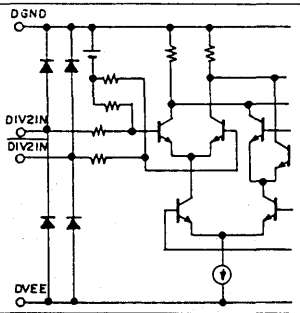
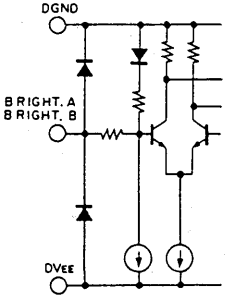
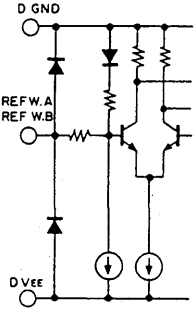


(1) Ta = Tc
(When infinitely large heat sink is used.)
(2) For PCB mounting
(PCB area equivalent to 20 × 10 × 1.6mm and copper foil area covering 30 % of one side.)
(3) Before mounting

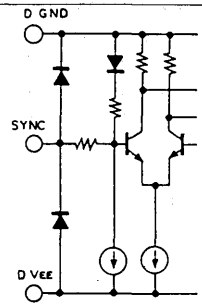
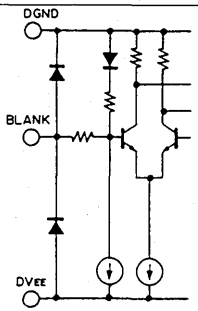
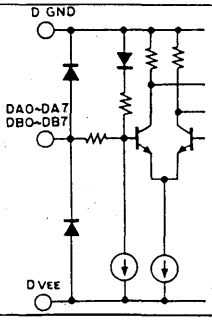
Pin Description and I/O Pin Equivalent Circuits

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1, 44	DV_{EE}	− 4.5V (typ.)		Digital power supply
2	AGND	GND		Analog GND
3, 4	AV_{EE}	− 4.5V (typ.)		Analog power supply
5	FS ADJ	− 1.24V (typ.)		Controls full scale voltage of analog output. Output current can be varied by adjusting the value of the external resistor connected to this pin.
6	COMP			Compensation pin for internal amplifier. Connect capacitor between COMP and AV_{EE}.
7	IO	0 ~ − 1071mV (typ.)		Analog output pin. Function as differential current output.
8	$\overline{IO}$			
9	$\overline{SET\ UP}$	ECL		Control input for SET UP. When "1" is input, output becomes BLANK 1 level ; when this pin is fed with "0" or left open, output becomes BLANK 2 level. (Refer to Table 1.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	$\overline{\text{SYNC EN}}$	ECL		Enable input for Sync output. When "0" is input or left open, output for Sync level is obtained.
11	C2	ECL		Control input for operating mode. For multiplex mode, CLK input frequency can be selected. For data select mode, either input data A or B can be selected. (Refer to Table 2.)
12	C1	ECL		Control input for operating mode. Input of "0" selects multiplex mode and input of "1" selects data select mode. (Refer to Table 2.)
13	$\overline{\text{CLK}}$	ECL		Clock input pin.
14	CLK			

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	$\overline{\text{DIV2OUT}}$	ECL		Outputs 1/2 clock frequency signal. Only when both C1 and C2 inputs are "0", a 1/2 clock frequency signal synchronized with DIV2IN is output. Otherwise, a signal at the clock frequency is output. (Refer to Timing Diagrams.)
16	DIV2OUT			
17, 22, 23	DGND	GND		Digital GND.
18	$\overline{\text{DIV2IN}}$	ECL		In multiplex mode, this converter is able to be synchronized by inputting 1/2 clock as a system clock into these pins. (Refer to Fig. 6. (1)).
19	DIV2IN			
20	BRIGHT. B	ECL		BRIGHT control input for DATA A and DATA B. When "1" is input, D/A output is shifted up by 10 %. (Refer to Table 1.)
26	BRIGHT. A			
21	REF W. B	ECL		Ref. White control input for DATA A and DATA B. When "1" is input, output is set to WHITE Level. (Refer to Table 1.)
27	REF W. A			

6

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	SYNC	ECL		Input control for Sync. Active only when the SYNC EN input is "0". When "1" is input, D/A output is shifted to Sync level regardless of other inputs.
25	BLANK	ECL		Control input for BLANK. When "1" is input, D/A output is shifted to either BLANK 1 or BLANK 2 level.
28~35	DB0~DB7	ECL		Digital input pin. DA0 (LSB) to DA7 (MSB) are for DATA A ; DB0 (LSB) to DB7 (MSB) are for DATA B.
36~43	DA0~DA7			

Electrical Characteristics

($AV_{EE} = DV_{EE} = -4.5V$, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n		8	8	8	bit
Linearity error	E_L	V_{FS} = 1071mV			±1/2	LSB
Differential linearity error	E_D				±1/2	LSB
Digital input current	I_{IH}	$V_{IN} = -0.7V$			100	μA
	I_{IL}	$V_{IN} = -1.9V$	−100			μA
Input capacitance	C_{IN}			5		pF
Digital output voltage	V_{OH}	R_T = 50Ω to −2V	−1.05			V
	V_{OL}				−1.49	V
FS ADJ pin voltage	$V_{ADJ.}$		−1.14	−1.24	−1.34	V
Max. output current	Io		48			mA
Compliance voltage	V_{OC}		−1.2		1.5	V
Output offset current	I_{OF}			7	50	μA
Output resistance	Ro			50		kΩ
Output capacitance	Co			8		pF
Absolute gain error	E_G	$V_{FS} = -1071mV$	−10		+10	% of F.S.
Gain error temperature coefficient	T_{CG}			0.05		% of F.S./°C
Currect consumption	I_{EE}	R_L = 25Ω	−300	−235	−170	mA
Max. conversion rate	Fs		500			MSPS
MUX (1) mode						
DIV2IN setup time	ts_2		0.3			ns
DIV2IN hold time	th_2		1.1			ns
DIV2OUT output delay	tdck	R_T = 50Ω to −2V	1.2		1.6	ns
DATA setup time	ts		0.4			ns
DATA hold time	th		1.4			ns
Analog output delay	td		2.4		4.1	ns
Pipeline delay			3	3	3	clocks
MUX (2), SELECT mode						
DIV2OUT output delay	tdck	R_T = 50Ω to −2V	1.1		1.4	ns
DATA setup time	ts		0.6			ns
DATA hold time	th		1.2			ns
C2 setup time	tsc		0.3			ns
C2 hold time	thc		0.9			ns
Analog output delay	td	R_L = 25Ω	2.3		3.9	ns
Pipeline delay			1.5	1.5	1.5	clocks

6

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog output						
Rise time	tr	R_L = 25Ω		0.4	0.6	ns
Fall time	tf			0.4	0.6	ns
Settling time	t_{SET}			1.5		ns
Glitch energy	GE			5		pVs

Description of Operation (Refer to Block Diagram and Pin Configuration)

Normal multiplex mode (MUX (1) mode) is defined as a state when C1 and C2 are set to "0". When the system clock (CLK/2) is input to DIV2IN, the output signal is in phase with the system clock at the 1/2 CLK frequency. When C1 is set to "0" and C2 to "1", the clock with duty cycle of exactly 50% must be input.

DATA A (DA0 to DA7), DATA B (DB0 to DB7) and all control signal (C2, BRIGHT.A, REF W.A, BRIGHT.B, REF W.B, BLANK, and SYNC) data are latched in internal registers on the rising edge of the internal clock, which has the same frequency as the DIV2OUT.

Internally, the DB, BRIGHT.B, and REF W.B are delayed by 1/2 period of the DIV2OUT output. After the upper 4 bits of DA and DB are decoded into thermometer code, they are multiplexed within MUX block together with the lower 4 bit data and control signals, and then fed to DAC block.

When C1 is "1", DA, BRIGHT.A, and REF W.A can be selected by inputting "0" at C2. In the same way, DB, BRIGHT.B, and REF W.B. can be selected by inputting "1" at C2.

In the DAC block, the input DATA are converted into current. The DAC creates analog output current composing of the following portions :

- Weighted lower 4bit current
- Thermometer-coded upper 4bit current
- Function output currents

The output comes out delayed by 1.5 clocks of DIV2OUT after the rising edge of the CLK.

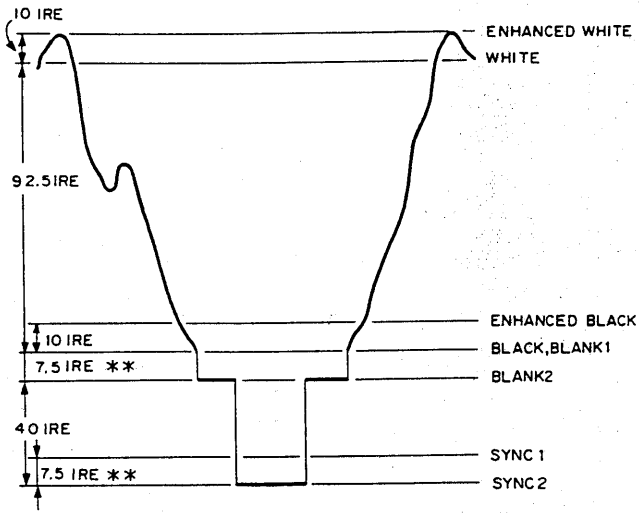
The analog current can be change into a voltage when a load resistor is connected to the output pin.

This IC contains an internal band-gap voltage source which allows adjustment of the output voltage full scale by varying the resistance value Rset externally connected between FS ADJ and AGND. The following formula describes this relationship.

$$Rset = \frac{V_{ADJ.}}{\frac{661mV}{R_L} \times \frac{16}{255}} \ [\Omega]$$

$$V_{ADJ.\ (TYP.)} = -1.24V$$

$\overline{IO}$ (mA) *	V ($\overline{IO}$) (mV)
0	0
− 2.84	− 71
− 26.44	− 661
− 29.28	− 732
− 31.42	− 785.5
− 40.7	− 1017.5
− 42.84	− 1071



* In case of doubly-terminated 50 Ω load
** 7.5 IRE difference·····Available when $\overline{SETUP}$ pin is floating or "0" level, not available when SETUP pin is "1" level.

Fig. 1. Composite Video Output

Description	$\overline{IO}$ (mA)	$\overline{SETUP}$	$\overline{SYNC\ EN}$	BRIGHT	SYNC	BLANK	REF W	Input DATA
Enhanced White	0	×	×	1	0	0	0	11111111
	0	×	×	1	0	0	1	XXXXXXXX
White	− 2.84	×	×	0	0	0	1	XXXXXXXX
	− 2.84	×	×	0	0	0	0	11111111
Enhanced DATA	DATA	×	×	1	0	0	0	DATA
DATA	DATA − 2.84	×	×	0	0	0	0	DATA
Enhanced BLACK	− 26.44	×	×	1	0	0	0	00000000
BLACK, BLANK1	− 29.28	×	×	0	0	0	0	00000000
	− 29.28	1	×	×	0	1	×	XXXXXXXX
	− 29.28	1	1	×	1	×	×	XXXXXXXX
BLANK2	− 31.42	0	×	×	0	1	×	XXXXXXXX
	− 31.42	0	1	×	1	×	×	XXXXXXXX
SYNC1	− 40.7	1	0	×	1	×	×	XXXXXXXX
SYNC2	− 42.84	0	0	×	1	×	×	XXXXXXXX

Table 1. I/O Correspondence Chart

C1	C2	MODE		CLK IN (MHz)	DATA IN (Mbps)	OUT (Mbps)
0	0	MUX	(1)	500	250	500
0	1		(2)	250*	250	500
1	0	A		250	250	250
1	1	B		250	250	250

* The CLK duty cycle must be set to 50%.
A : DA0 to DA7 is selected.
B : DB0 to DB7 is selected.

Table 2. Output Mode Chart

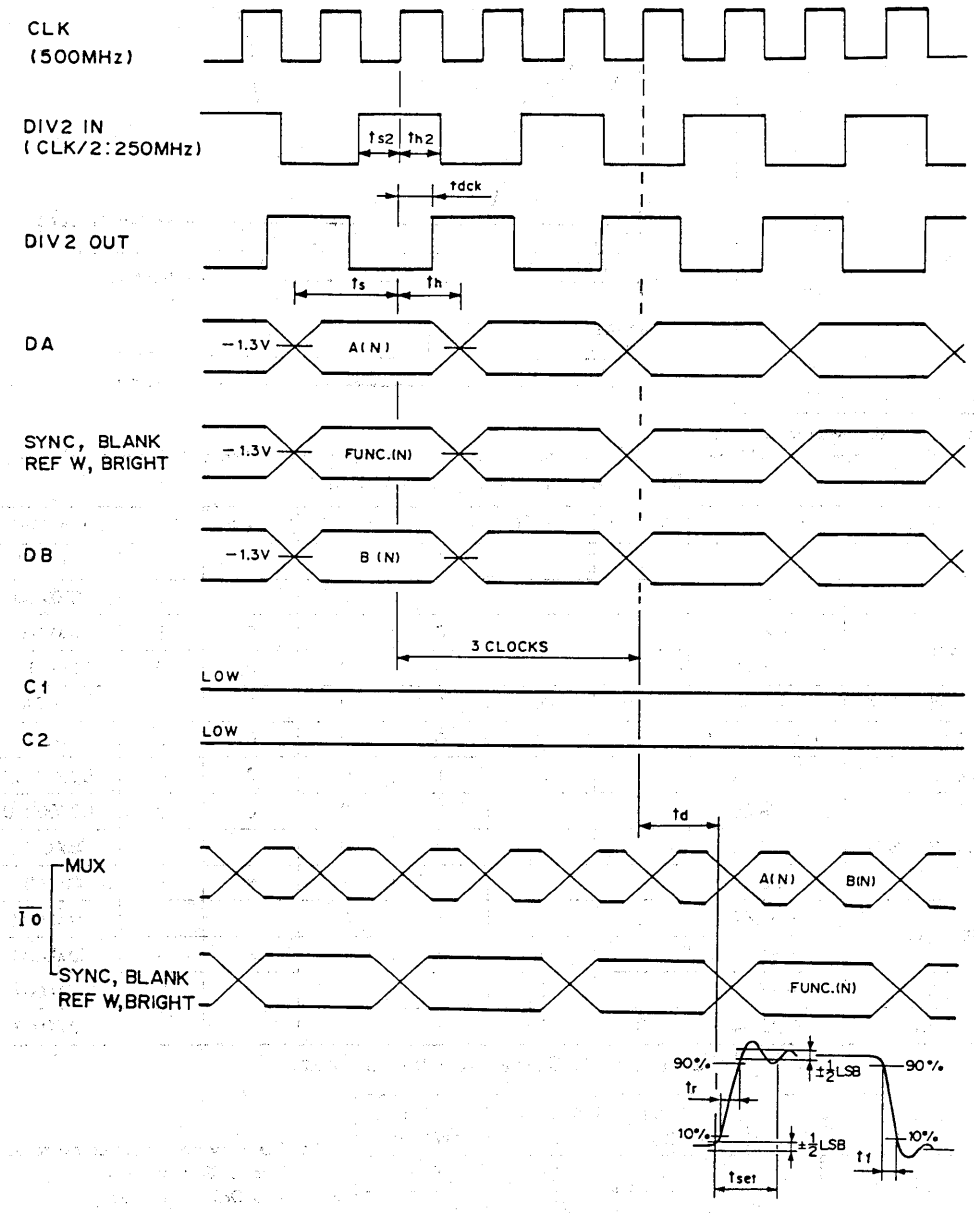


Fig. 2. Timing Diagram – MUX (1) MODE

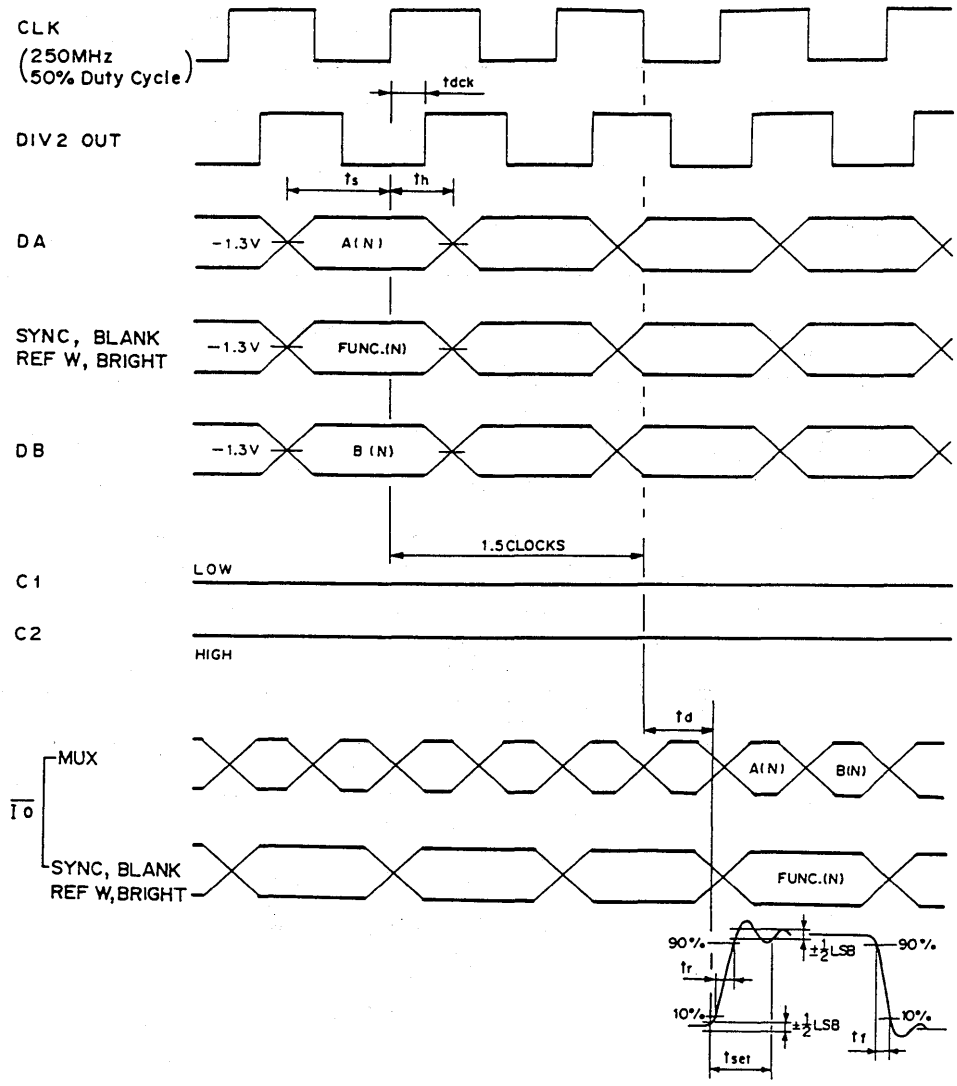


Fig. 3. Timing Diagram – MUX (2) MODE

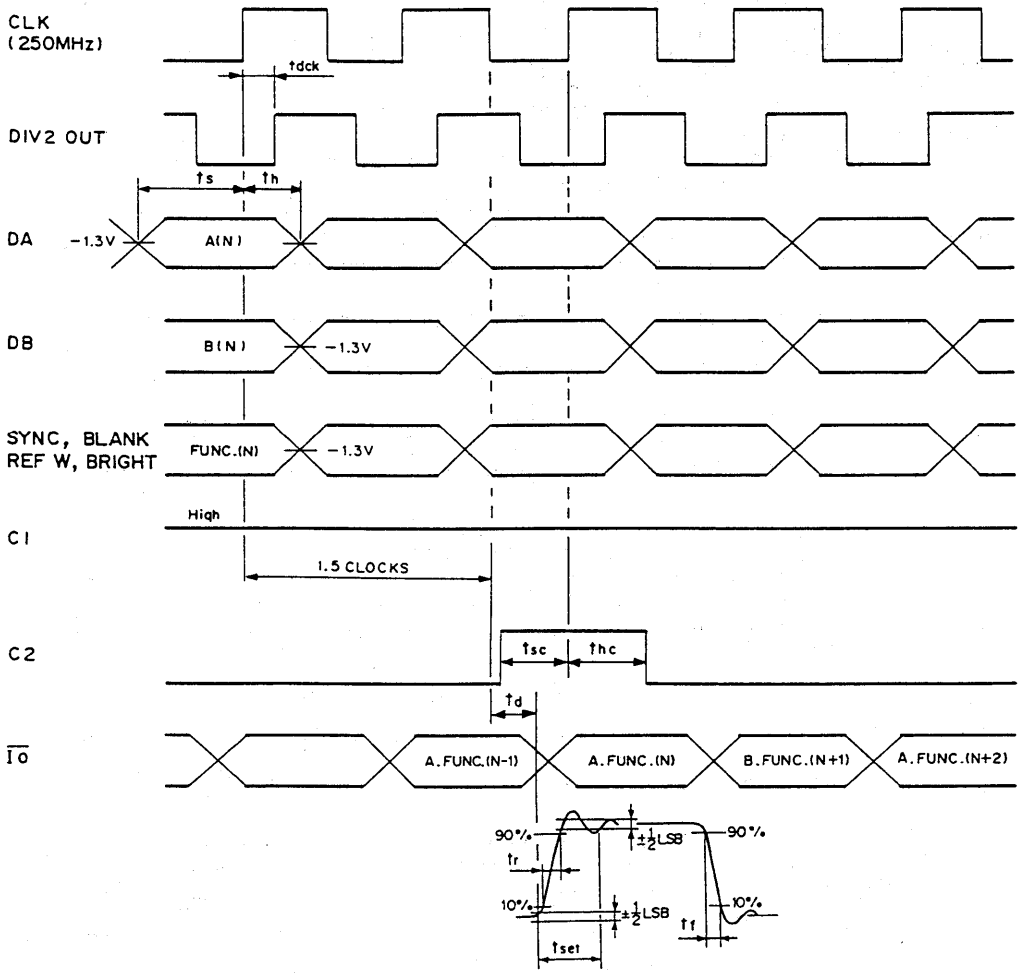
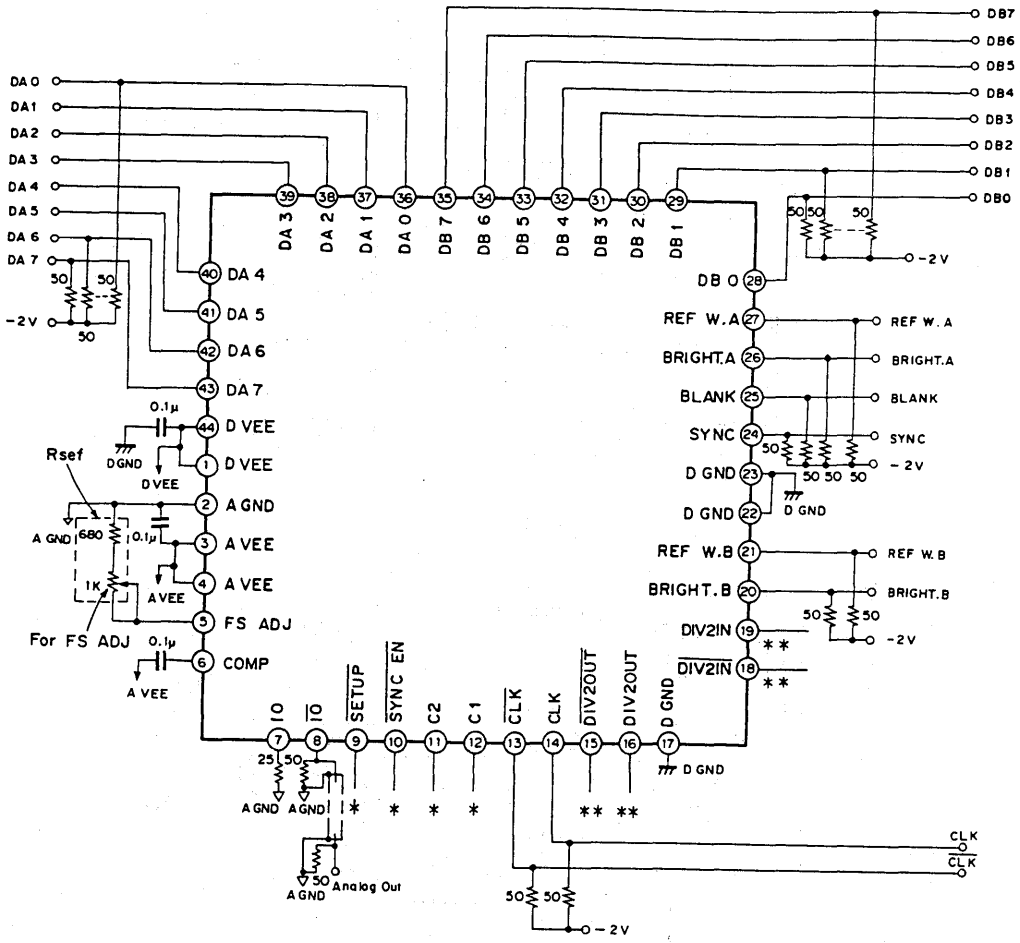


Fig. 4. Timing Diagram – SELECT MODE

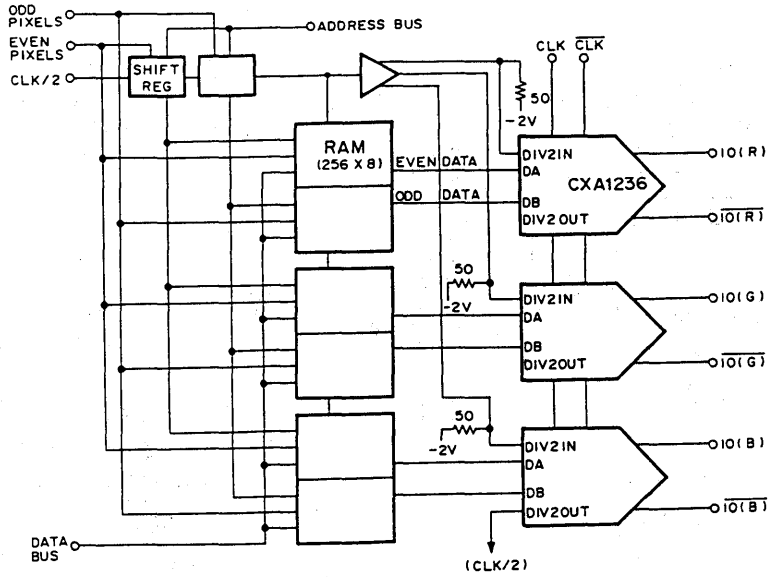


* Refer to Pin Description

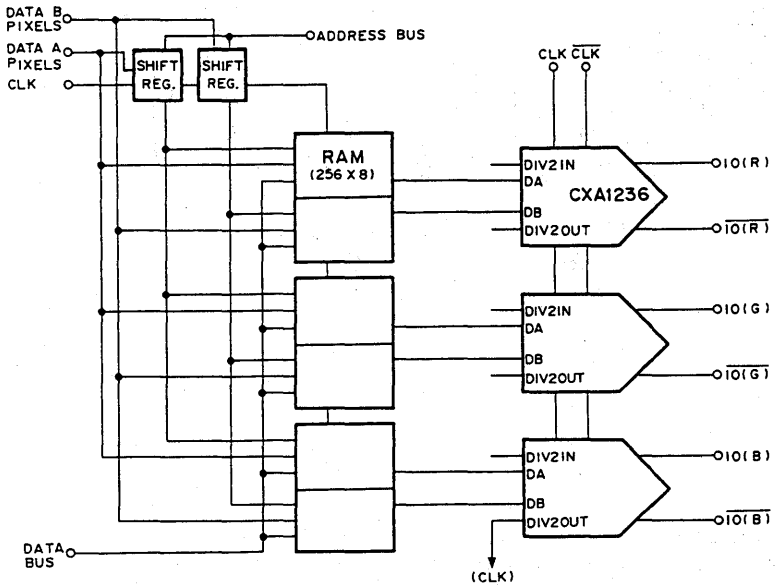
** Refer to Pin Description and Application Circuit

Fig. 5. Typical Usage Circuit Configuration

6



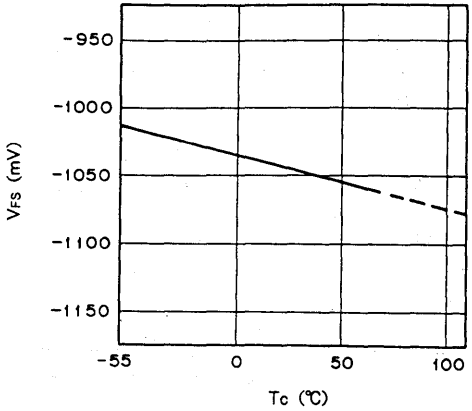
(1) MUX MODE



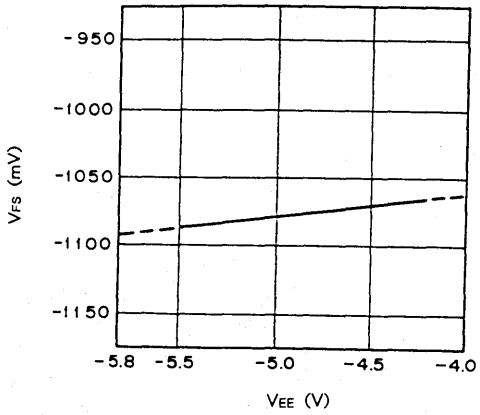
(2) SELECT MODE

Fig. 6. Application Circuit Examples

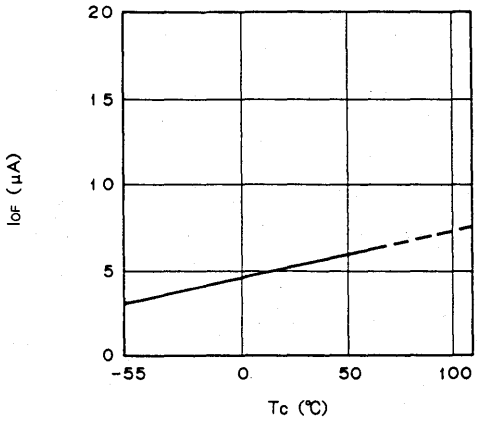
Full Scale Voltage vs. Case Temperature



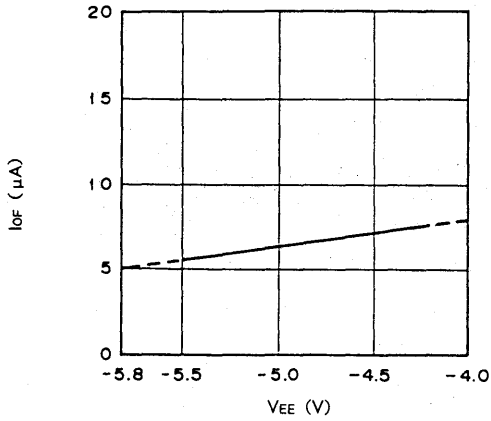
Full Scale Voltage vs. Supply Voltage



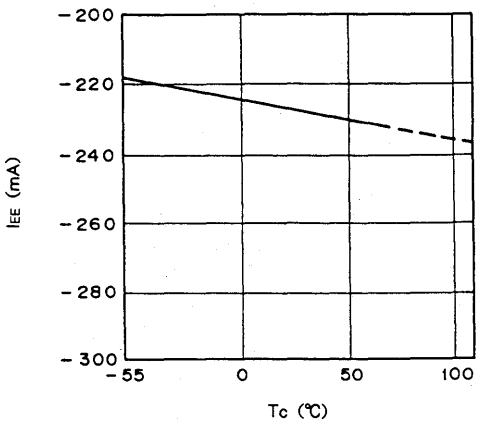
Output Offset Current vs. Case Temperature



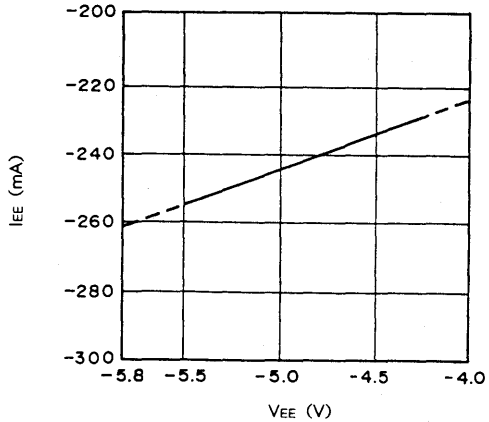
Output Offset Current vs. Supply Voltage



Supply Current vs. Case Temperature



Supply Current vs. Supply Voltage



6

Notes on Usage

(1) Wiring for Digital Input
- All of the digital inputs are single-ended ECL compatible inputs. For high-speed operation, the wiring characteristic impedance and terminal resistance should be about 50Ω and the resistors should be connected to V_{TT} (−2V) which is close to the input pins.

(2) Noise Reduction Measures
- Try to provide grounding widely on the whole board to prevent parasitic inductances and resistances.
- Keep AGND and DGND separated as much as possible. Keep AV_{EE} and DV_{EE} separated as much as possible also. For making connections of AGND and DGND or AV_{EE} and DV_{EE}, using the board connectors is recommended.
- Connect a bypass capacitor of 1 µF and 0.01 µF between the AGND, DGND and the AV_{EE}, DV_{EE} respectively as close as possible to the IC pins. Also, connect a bypass capacitor between the DGND and the VTT (−2V) closely to the terminal resistors. The most suitable capacitor is a 0.01 µF ceramic chip type.
- For the external Rset resistor connected to the FS ADJ pin, the wiring should be as short as possible.

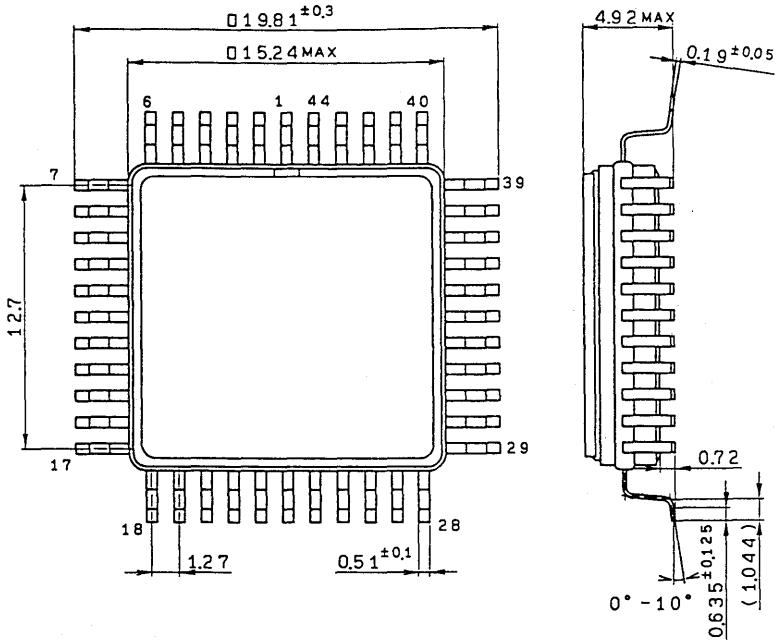
(3) Preventing Output Oscillation
Insert a 0.1 µF capacitor between the COMP and AVEE pins with the shortest distance possible.

(4) Procedures for Analog Output
The D/A converter is designed to directly drive a 50Ω or 75Ω line.
For line matching, both ends of the line must be terminated at 50Ω (or 75Ω) as shown in the application circuit.

(5) When C1 is "0" and C2 is "1", a 50% CLK must be input for the duty cycle. When the CLK duty cycle is off, the ratio of the analog output width for DA and DB is directly affected.

Package Outline Unit : mm

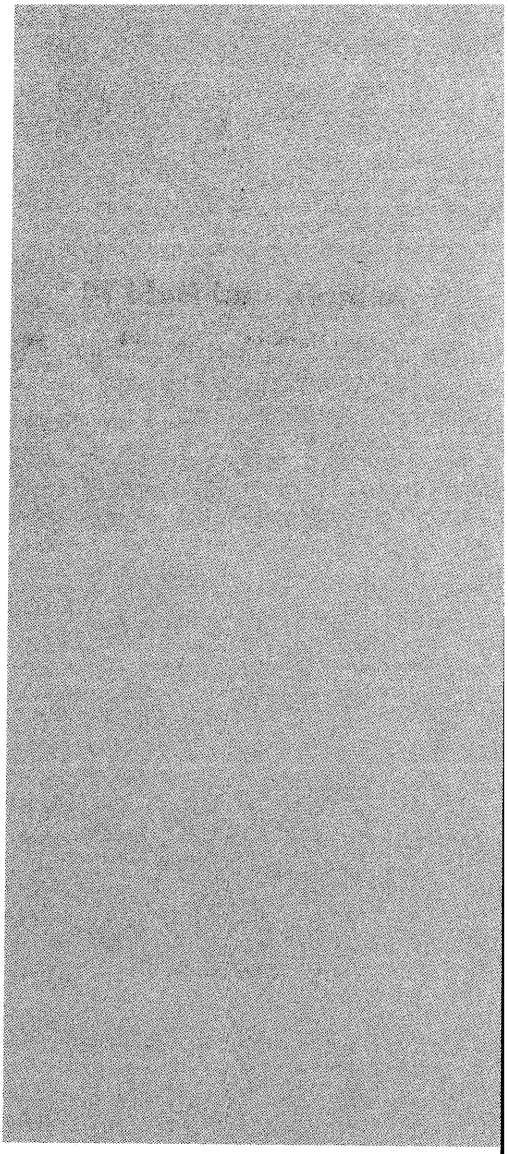
44pin QFP (Ceramic)



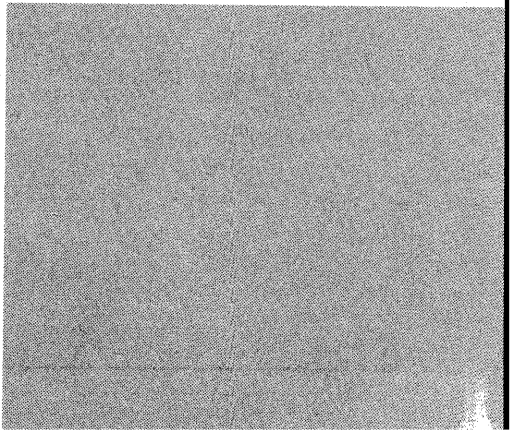
SONY NAME	QFP-44C-L01
EIAJ NAME	XQFP044-G-0000-A
JEDEC CODE	MO-084-AB*

* (Similar)

6



Sample and Hold IC



Sample and Hold IC

Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CXA1008P	-	35	680	S/H for CX20220A-1/-2	375-393
CXA1009P	-	18	420	S/H for CX20220A-1/-2	375-393
CXA1693Q	-	35	190	S/H for CXA1496AQ	394-400

SONY

CXA1008P/1009P

High-speed Sample and Hold Amplifiers

Description

CXA1008P/1009P are bipolar IC's developed for the purpose of sample holding video signals and other signals at high-speed.

Features

- Maximum sampling frequency
  - CXA1008P 35 MHz
  - CXA1009P 18 MHz
- Linearity 0.08% (Typ.)
- Clock input level ECL compatible
- Low power consumption
  - CXA1008P 680 mW (Typ.)
  - CXA1009P 420 mW (Typ.)

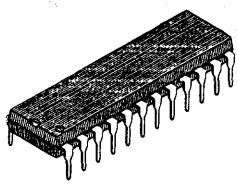
Structure

Bipolar silicon monolithic IC.

Applications

- A/D converter and other analog signal processing
- Other general applications.

24pin DIP(Plastic)



Function

High-speed hold circuit, wide band 6 dB amplifier, A/D reference power supply, A/D clock output circuit.

Block Diagram

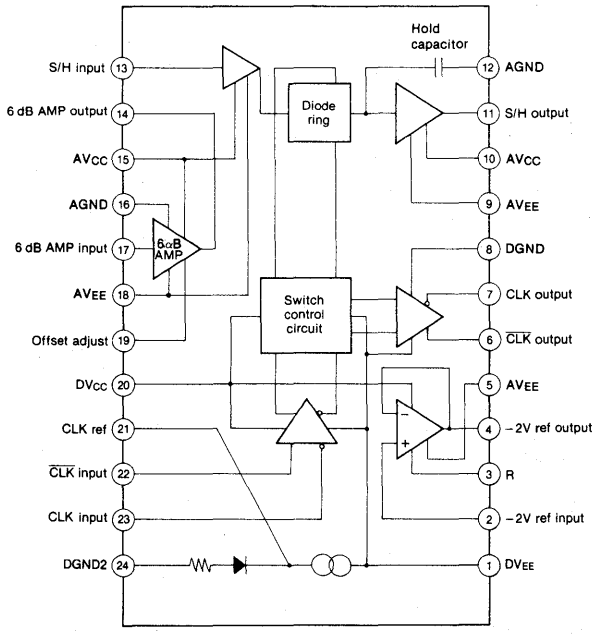


Fig. 1

E89641-HP

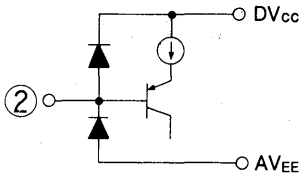
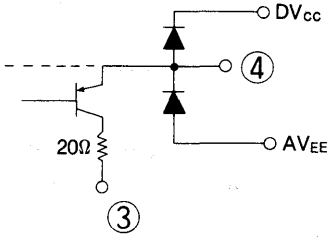
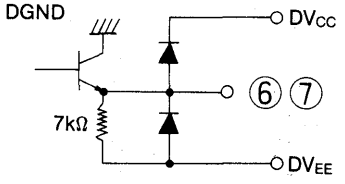
Absolute Maximum Ratings ($T_a = 25°C$)

•Supply voltage	V_{CC}	+5.5	V
	V_{EE}	−6.0	V
•Operating temperature	T_{opr}	−20 to +75	°C
•Storage temperature	T_{stg}	−55 to +150	°C
•Allowable power dissipation	P_D	1.2	W

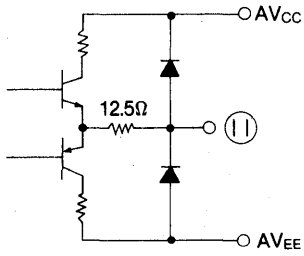
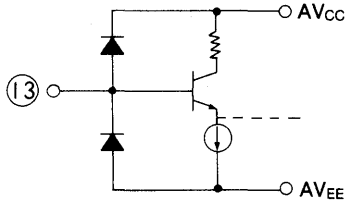
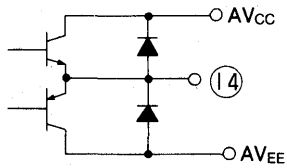
Recommended Operating Conditions

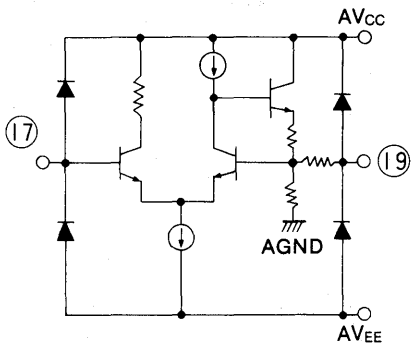
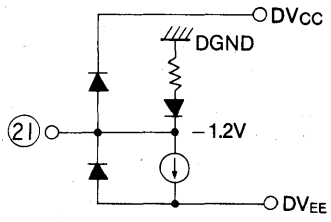
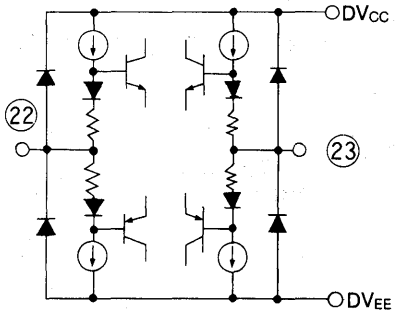
•Supply voltage	V_{CC}	+4.75 to 5.25V
	V_{EE}	−4.75 to −5.45V

Pin Description

No.	Symbol	Equivalent circuit	Description
1	DV_{EE}		Digital V_{EE} (−5V)
2	−2V ref input		reference voltage input for A/D converter
3	R		Pulldown terminal for external R (30Ω typically)
4	−2V ref output		reference voltage output for A/D converter
5	AV_{EE}		Analog V_{EE} (−5V)
6	CLK output		CLK output for A/D converter
7	$\overline{CLK}$ output		$\overline{CLK}$ output for A/D converter
8	DGND		Digital GND
9	AV_{EE}		Analog V_{EE} (−5V)
10	AV_{CC}		Analog V_{CC} (+5V)

7

No.	Symbol	Equivalent circuit	Description
11	S/H output		S/H output
12	AGND		Analog GND
13	S/H input		S/H input
14	6dB AMP output		Olutput terminal of 6dB amplifier
15	AV_{CC}		Analog V_{CC} (+5V)
16	AGND		Analog GND

No.	Symbol	Equivalent circuit	Description
17	6dB AMP input		6dB AMP input
18	AV_{EE}		Analog V_{EE} (−5V)
19	offset adjust		6dB AMP DC offset adjust terminal
20	DV_{CC}		Digital V_{CC} (+5V)
21	CLK ref		CLK reference output
22	CLK input		CLK input (Note: connect to (21) PIN or input ECL CLK signal)
23	$\overline{CLK}$ input		$\overline{CLK}$ input (Note: input ECL $\overline{CLK}$ signal)
24	DGND		Digital GND

7

CXA1008P

Electrical Characteristics ($Ta = 25°C$, $V_{CC} = +5V$, $V_{EE} = -5V$)
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		V_{CLKREF}	−1.3	−1.2	−1.1	V
Analog input voltage range	$\triangle V < 1.2V$ *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power Supply		I_{CC}	48	60	78	mA
	without −2V ref.	I_{EE1}	48	60	78	mA
	with −2V ref. $R_{LI} = 50\Omega$ *2	I_{EE2}	80	100	125	mA
Input bias current	$-2V < V_{in} < 2V$	I_{Biass}		15	30	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	$V_{in} = 2V_{p-p}$ (−3dB)	BW		12		MHz
Power supply rejection ratio		SVR_S		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	$V_{in} = 0V$	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	20	mV/μs
Acquisition time	$\triangle V = 1.2V$	Taq		8	12	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T_{set}		25		ns
DC offset voltage	$f_{CLK} = 5MHz$	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	35			MHz
Minimum sampling frequency		f_{CLKL}			5	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE mode ramp. f_{CLK} = 20MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

($R_{LI} = 50\Omega$. see Fig. 3)

CXA1009P

Electrical Characteristics ($Ta = 25°C$, $V_{CC} = +5V$, $V_{EE} = -5V$)
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V_{IH}	−0.9	−0.8		V
		V_{IL}		−1.6	−1.5	V
CLK Reference voltage (pin 21)		V_{CLKREF}	−1.3	−1.2	−1.1	V
Analog input voltage range	$\triangle V < 1.2V$ *1	V_{INS}	−3		3	V
Output voltage range		V_{outs}	−3		3	V
Power supply		I_{CC}	25	35	45	mA
	without −2V ref.	I_{EE1}	25	35	45	mA
	with −2V ref. $R_{LI} = 50\Omega$ *2	I_{EE2}	60	75	98	mA
Input bias current	$-2V < Vin < 2V$	I_{Biass}		9	18	μA
Output impedance		Z_{OS}		20	40	Ω
Voltage gain ratio		G_{VS}	0.99	1.0	1.01	
Full power bandwidth	$V_{in} = 2V_{p\text{-}p}$ (−3dB)	BW		6		MHz
Power supply rejection ratio		SVR_S		−40		dB
Hold mode feed through	fin = 4MHz Vin = 1 Vp-p, CLK open	HMTH		−50	−40	dB
Clock leak	Vin = 0V	CL_{LEAK}		10	50	mV
Linearity	fin = 19.53kHz (10/512MHz) f_{CLK} = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to −2V	HMDR		2	10	mV/μs
Acquisition time	$\triangle V = 1.2V$	Taq		12	20	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T_{set}		36		ns
DC offset voltage	f_{CLK} = 5MHz	V_{offset}		±15	±100	mV
Maximum sampling frequency		f_{CLKH}	18			MHz
Minimum sampling frequency		f_{CLKL}			2	MHz
Differential gain (D.G.)	Vin = NTSC 40 IRE more ramp f_{CLK} = 15MHz	DG		0.5	1.0	%
Differential phase (D.P.)		DP		0.5	1.0	deg

*1 $\triangle V$ is voltage change during one sampling period.
*2 Power consumption is $I_{CC} \times 5V + I_{EE1} \times 5V + 40mA \times 1.8V$.
*3 Input voltage waveform

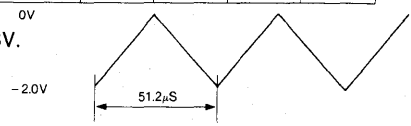


Fig. 2

6dB amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Intput voltage range	*3	V_{INA}	−1.3		+0.8	−1.3		+0.8	V
Band width (−3dB)	V_{in} = IV_{pp}	W	45	55		15	25		MHz
Input bias current	−1V < V_{in} < 1V	$I_{Bias\ A}$		9	20		5	10	μA
Output impedance		Z_{OA}		4	10		4	10	Ω
Voltage gain	*4	G_{VA}	5.1	6.0	6.9	5.1	6.0	6.9	dB
Power supply rejection ratio		SVR_A		−40			−40		dB

*3 2ndary harmonic: −40dB f_{in} = 3.58MHz
*4 f_{in} = 3.58MHz V_{in} = $1V_{p\text{-}p}$

CLK OUT section (see Fig. 3)

Item		Condition	Symbol	CXA1008P			CXA1009P			Unit
				Min.	Typ.	Max.	Min	Typ.	Max.	
Output voltage	Amplitude	R_{L2} = 1.5 KΩ see Fig. 3	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low level		V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time			tr		7	10		7	10	ns
Fall time			tf		5	8		5	8	ns
CLK Delay 1			τ_{D1}	20	28	34	36	38	45	ns
CLK Delay 2			τ_{D2}	14	22	28	24	26	33	ns

−2V_{ref} amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Voltage gain ratio	V_{ref} = −2V R_{LI} = 50Ω	G_{VR}	0.9	1.0	1.1	0.9	1.0	1.1	
Input bias current	−3V < V_{in} < 0V	$I_{Bias\ R}$		5	10		5	10	μA
Output impedance		Z_{OR}		2	10		2	10	Ω

Electrical Characteristics Test Circuit

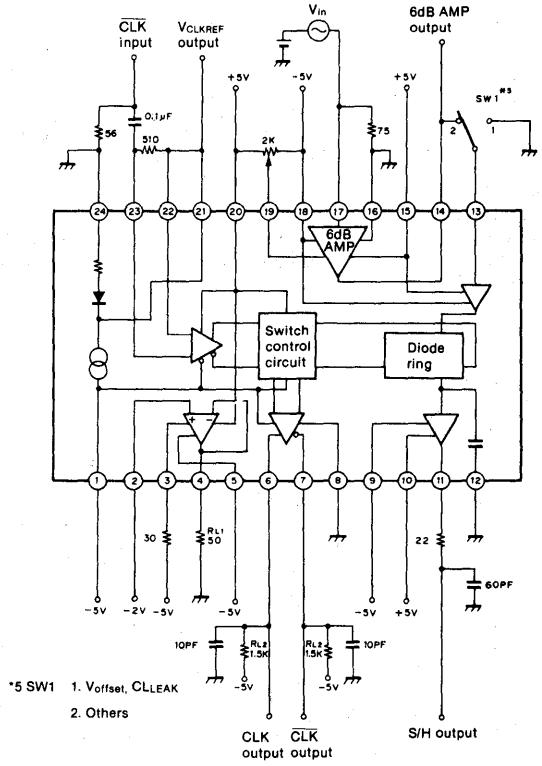


Fig. 3

Timing Chart

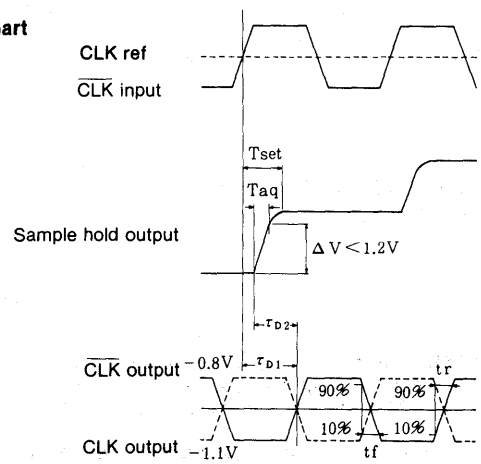


Fig. 4

7

Description of Functions

CXA1008P/1009P are the monolithic ICs incorporating a high-speed sample hold circuit, a wide band 6 dB amp, reference power supply for A/D converter, and a clock output section, and operate up to a sampling frequency of 35/18 MHz.

CXA1008P/1009P can compose in 20/15 MS/s A/D converter system in combination with a CX20052A. CXA1008P/1009P form, with the input of a single phase or 2-phase ECL clock input, a new sampling signal. For this reason, the sampling period remain unchanged even when the frequency or duty of the input sampling CLK signal changes.

- Wide band 6 dB AMP.

  In-phase amp with a band width over 45/15 MHz amplifies ordinary TV signal (1Vp-p) to a 2Vp-p signal which gives the highest accuracy when processed in CX20052A.

- CLK output section

  When used in combination with an A/D converter such as CX20052A, the CLK timing between the S/H circuit and the A/D converter needs to be adjusted, and up to 20/15 MHz, CXA1008P/1009P generate CLK timing signals for driving the A/D converter, and output 2-phase CLK at 300 mVp-p from pins 6 and 7. With this output, no separate CLK is required to combine with an A/D converter.

- CXA1008P/1009P incorporate a buffer amp to provide a reference voltage for the A/D converter.

Application Circuit

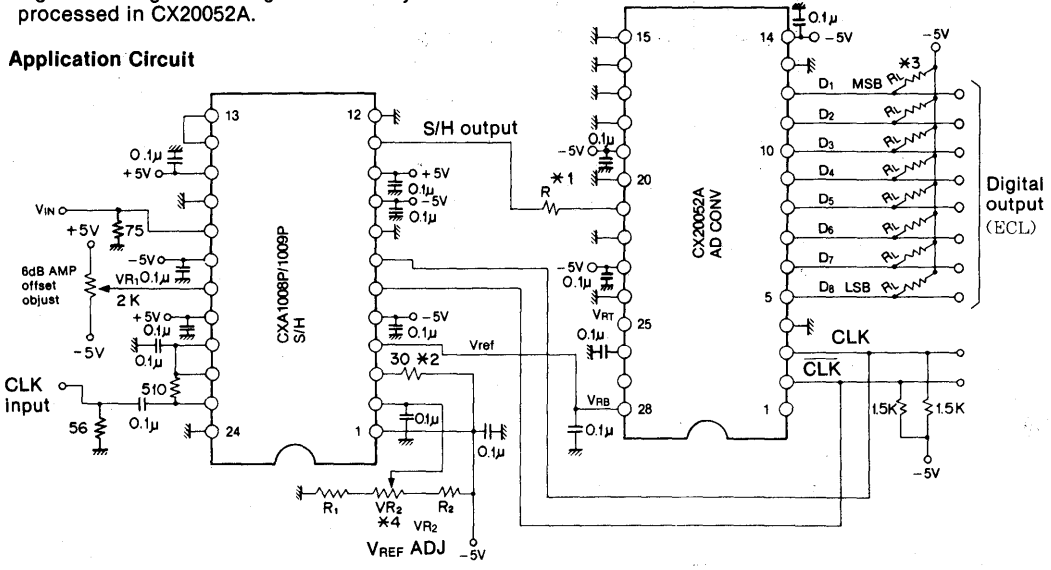


Fig. 5 Connection of CXA 1008P/1008P with CX20052A (1)

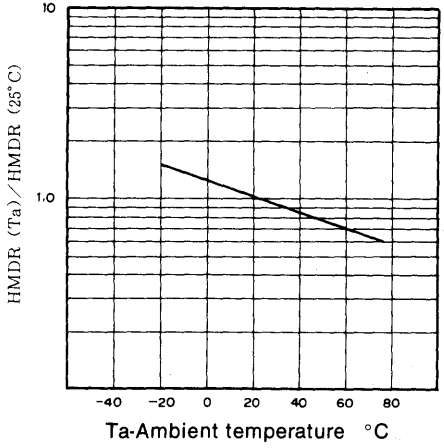
*1 R is a ringing preventing resistor. Select between 10 to 50Ω
*2 Pulldown R for V_{ref}
*3 R_L = 4.3kΩ
*4 R_1 = 1kΩ, VR_2 = 2kΩ, R_2 = 2kΩ

Notes on Application

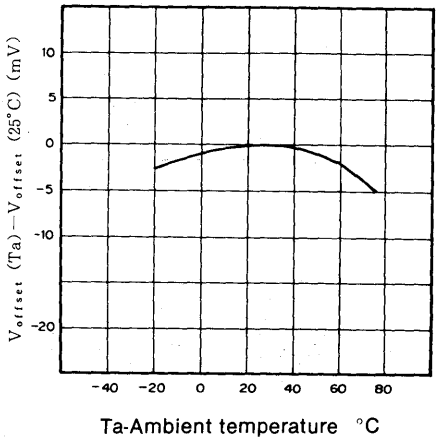
1. Unless sufficiently stable power supply and GND voltage in the high-frequency range are used, the device characteristics deteriorates. For this reason, bring the power supply bypass capacitor as near to this IC as possible, and make the pattern to the power supply and to the earth terminal as wide as feasible.
2. To reduce CLK leak, use waveforms similar to sine waves as far as possible, up to the CLK input. For satisfactory operation, a CLK input ampritude of around 300mV is enough.
3. When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

Changes in Characteristics with Temperature

Hold Mode Droop Rate

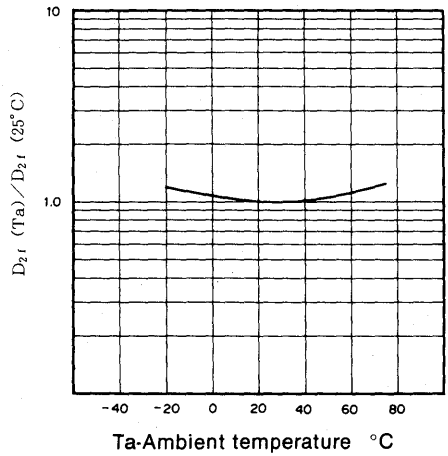


Offset Voltage Between S/H Input & Output

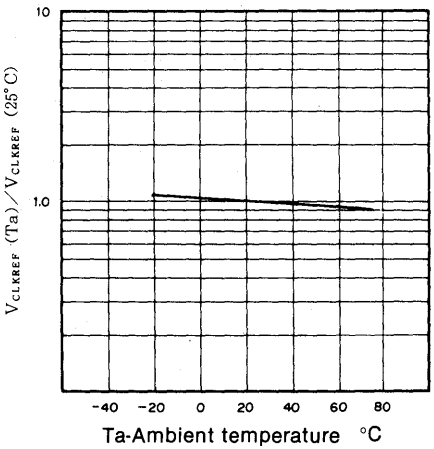


6dB AMP 2ndary Harmonic Level

(3.58MHz, Vin = $1V_{pp}$)



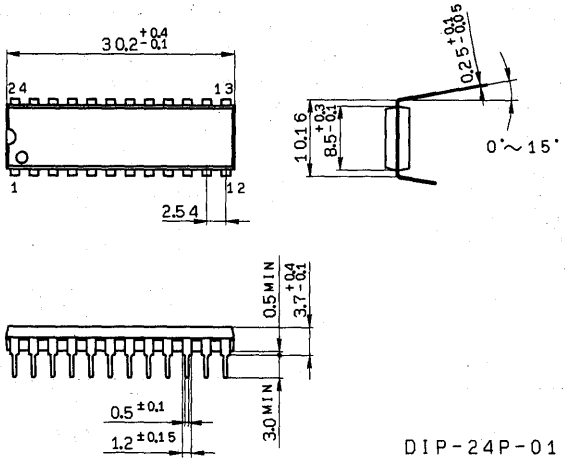
CLK Ref Voltage



7

Package Outline Unit : mm

24pin DIP(Plastic) 400mil 2.0g



DIP-24P-01

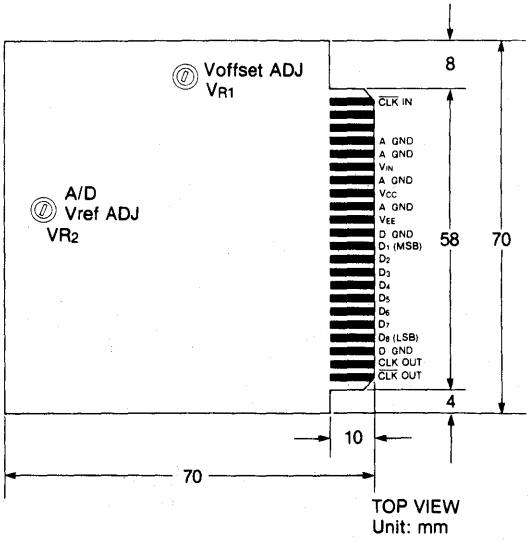
8bit, 20/15MHz A/D Converter Evaluation Board with CXA1008P/CXA1009P S/H.

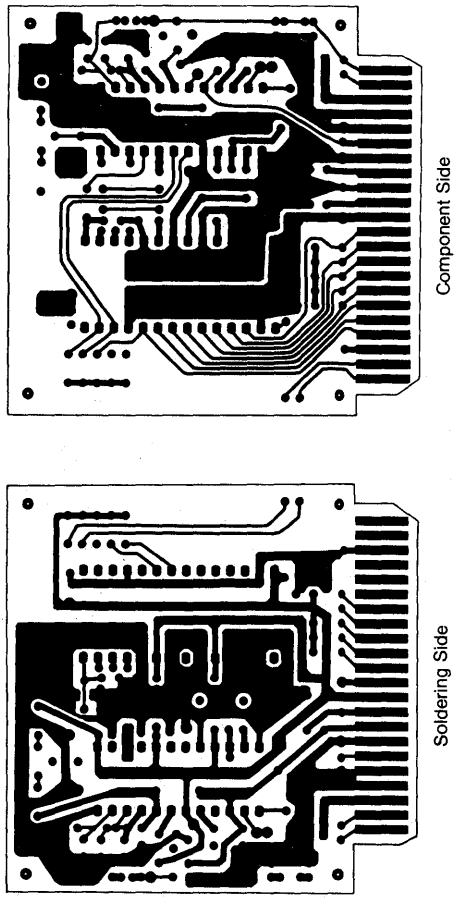
Description

CX20052A PCB-3A/3B is an 8 bit A/D converter board for video signal processing. A high speed S/H IC CXA1008P/1009P and a high speed 8 bit A/D converter CX20052A are assembled on single small printed circuit board.
CX20052A PCB-3A with CXA1008P mounted, operates up to 20 MHz of conversion rate, and CX20052A PCB-3B with CXA1009P mounted, operates up to 15 MHz of conversion rate.

Features

•Resolution	8 bit ±1/2 LSB
•Conversion rate	20 MHz CX20052A PCB-3A
	15 MHz CX20052A PCB-3B
•Analog input level	1Vp-p
•Digital output level	ECL level
•Power supply	±5V

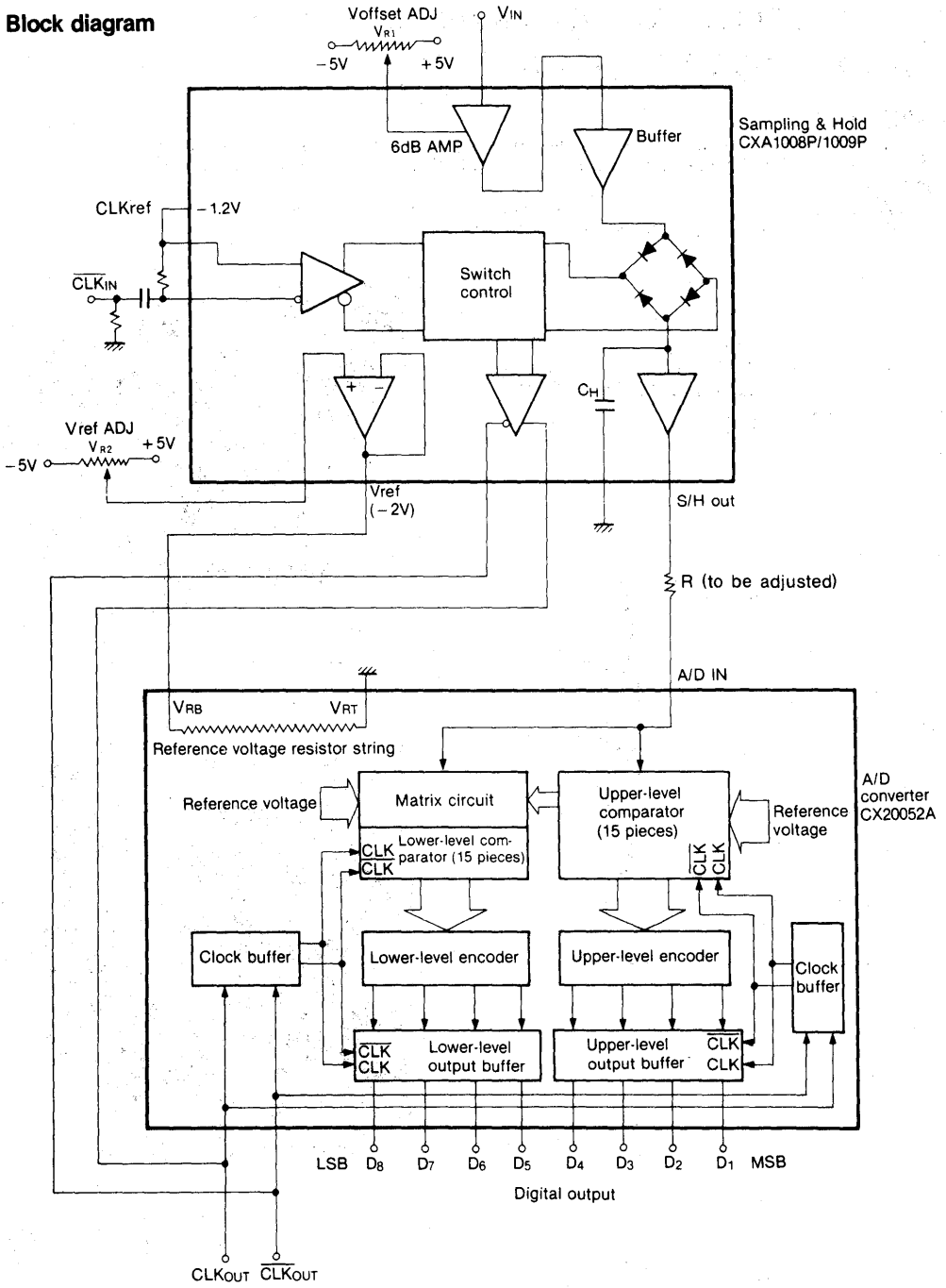




CX20052A PCB-3A/3B Pattern

7

1. Block diagram



2. Characteristics

1. Supply Voltage

(Ta = 25°C, V_{EE} = −5V, V_{CC} = 5V)

Item			Symbol	Min	Typ	Max	Unit
V_{CC}	+5V	CX20052A	I_{CC}		70	80	mA
		PCB-3A	I_{EE}		220	240	mA
V_{EE}	−5V	CX20052A	I_{CC}		50	60	mA
		PCB-3B	I_{EE}		200	220	mA

2. Analog Input (V_{IN})

Item	Symbol	Min	Typ	Max	Unit
AC Input Voltage Amplitude	V_{IN}			1	V
Offset Adjustable Range		±1.5	±2.0		V
Input Impedance	Z_{in}				
CX20052APCB-3A			75		Ω
CX20052APCB-3B			75		Ω

3. Digital Input ($\overline{CLK}$ IN)

Item	Symbol	Min	Typ	Max	Unit
Input Voltage (p-p)	V_{CLK}	0.3	0.8	4	V
Input Impedance	Z_{INCL}		50		Ω

4. Digital Output (D1 ~ D8) (1.5kΩ to V_{EE})

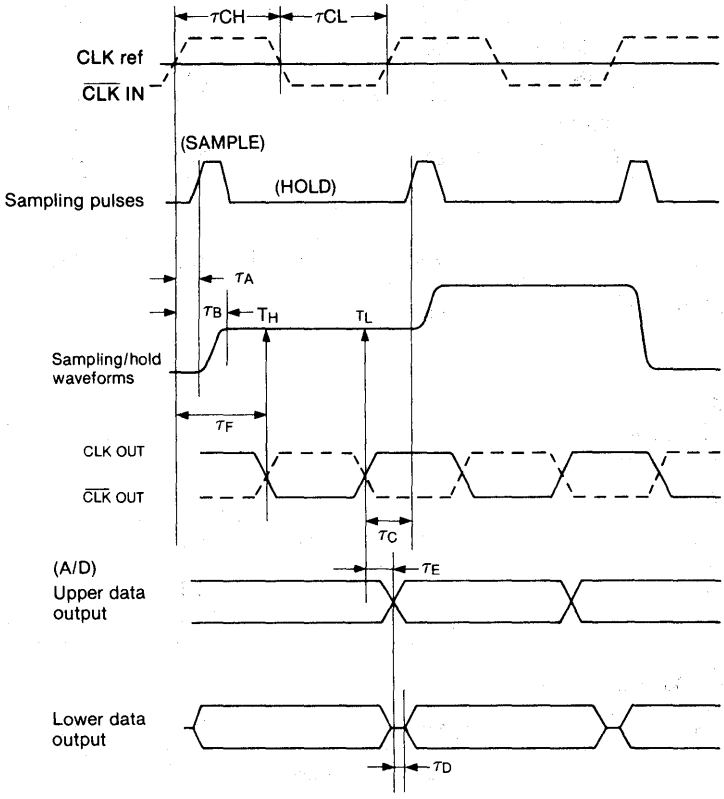
Item	Symbol	Min	Typ	Max	Unit
Output Voltage	V_{OH}	−0.90	−0.75		V
	V_{OL}		−1.50	−1.35	V

5. Clock Output (CLK_{OUT}, $\overline{CLK}_{OUT}$) (See timing chart)

Item		Symbol	CX20052A PCB-3A			CX20052A PCB-3B			Unit
			Min	Typ	Max	Min	Typ	Max	
Output voltage	Amplitude	V_{CLK}	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low Level	V_{CLKL}	−1.2	−1.1	−0.9	−1.2	−1.1	−0.9	V
Rise time		tr		6	10		6	10	ns
Fall time		tf		12	15		12	15	ns
CLK Delay		τ_F	20	28	34	36	38	45	ns

6

3. Timing Chart



T_H shows a timing when the A/D latches upper 4 bits.
T_L shows a timing when the A/D latches lower 4 bits.

Item	Symbol	CX20052A PCB-3A			CX20052A PCB-3B			
		Min	Typ	Max	Min	Typ	Max	Unit
Clock in	τCH		25			33		ns
	τCL		25			33		ns
Sampling delay	τA		6			12		ns
	τB		25			36		ns
Clock out	τF	20	28	34	36	38	45	ns
Data delay	τE			8			8	ns
	τD			4			4	ns

4. Adjustment

(1) Offset Voltage (Voffset ADJ)
VR_1 should be adjusted so that the S/H output meets the input voltage range of the A/D (0 to −2V).
(2) A/D reference voltage (Vref ADJ).
The reference voltage of the A/D (TP5) is to be −2V. VR_2 should be adjusted.

5. Output Data Format

The input of the A/D converter IC (S/H out) is quantized in 8 bit within the reference voltage range of V_{RT} and V_{RB}. The V_{RT} and V_{RB} are set at 0V and −2V respectively on the printed circuit board.

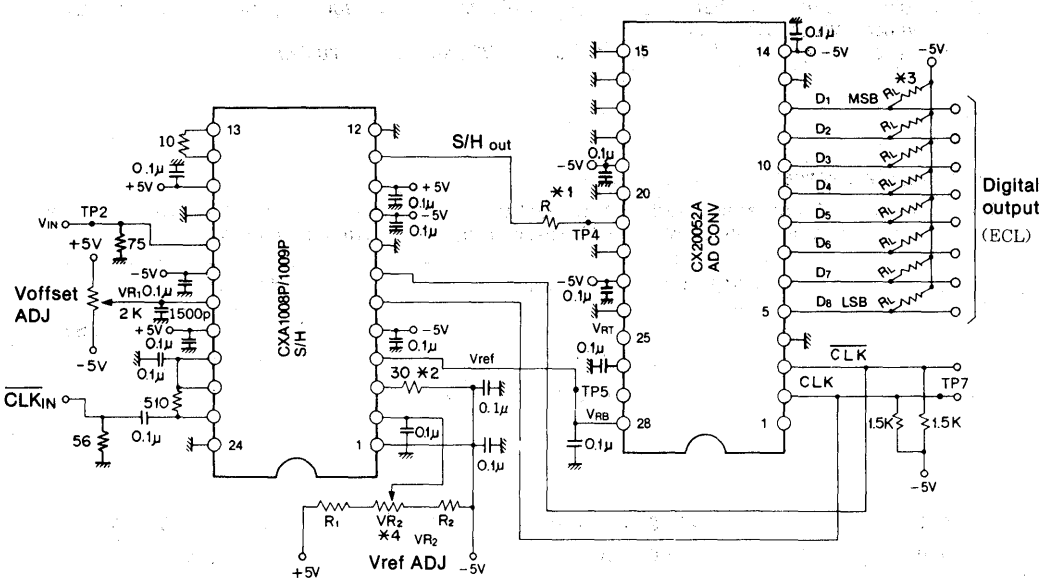
Step	A/D input signal voltage		Digital output code
			MSB LSB
	over	0. 0 0 0 0 V	1 1 1 1 1 1 1 1
0 0 0		0. 0 0 0 0 V (V_{RT})	1 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
1 2 7		−0. 9 9 6 1 V	1 0 0 0 0 0 0 0
1 2 9		−1. 0 0 3 9 V	0 1 1 1 1 1 1 1
.		.	.
.		.	.
.		.	.
2 5 5		−2. 0 0 0 0 V (V_{RB})	0 0 0 0 0 0 0 0
	under	−2. 0 0 0 0 V	0 0 0 0 0 0 0 0

6. Note on application

(1) Although the pull down resistors (RL: 4.3kΩ) are mounted on the PCB, additional pull down is recommended in an external circuit. The output current at the A/D output terminal should not exceed 10 mA.
(2) Digital output data should be latched by an external circuit to achieve a rated performance. Output data can be latched at a rising edge of CLK_{OUT}.
CLK_{OUT} AND $\overline{CLK}_{OUT}$ should be reshaped by an ECL line receiver such as MC10116 in an external circuit.
(3) The reference voltage is derived from the V_{EE} by a simple resistor dividing network. The power supply (±5V) should be stabilized to reduce voltage drift of the reference voltage.
(4) To reduce CLK leak, use waveforms similar to sine waves as far as possible up to the CLK input. For satisfactory operation, a CLK input amplitude of around 300m V_{PP} is enough.
(5) When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

7

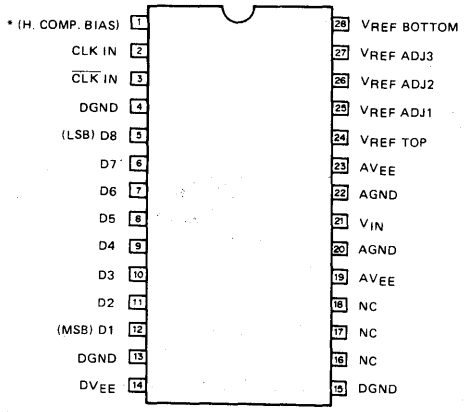
CX20052A PCB-3A/3B Circuit



*1. R is a ringing preventing resistor. Select between 10 to 50Ω according to pattern length.
*2. Pulldown R for Vref.
*3. $R_L = 4.3k\Omega$
*4. $R_1 = 2k\Omega$, $VR_2 = 2k\Omega$, $R_2 = 1k\Omega$

Additional Information on CX20052A

Pin Configuration (Top View)

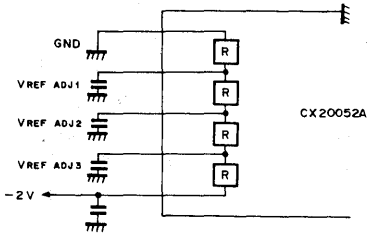


* Pin-1 to be used open.

Pin Description

No.	Symbol	Description
1	H-COMP BIAS	Pin connected to internal comparator. It should not be connected to outer circuit.
2	CLK IN	CLOCK input pin.
3	$\overline{\text{CLK}}$ IN	$\overline{\text{CLOCK}}$ input pin.
4	DGND	Ground pin of digital circuit.
15	DGND	Ground pin of digital circuit.
17	NC	Non-connection.
18	NC	
24	$V_{REF\ (T)}$	Reference voltage pin. (0V)
25	$V_{REF\ ADJ1}$	Reference voltage adjusting pin. (Usually it should be connected to GND through 0.047 μF capacitor.)
26	$V_{REF\ ADJ2}$	
27	$V_{REF\ ADJ3}$	
28	$V_{REF\ (B)}$	Reference voltage pin. (−2.0V)

(*) Reference resistors have adjusting pins as shown below. Usually these pins are connected to GND through 0.047 μF capacitors. When an adjustment is required, they should be connected to GND or $V_{REF\ (B)}$ through resistors.



Output Coding

Step	Input signal voltage	Output digital code (MSB LSB)
000	0.0000V	11111111
.	.	.
.	.	.
.	.	.
127	−0.9961V	10000000
128	−1.0039V	01111111
129	−1.0118V	01111110
.	.	.
.	.	.
.	.	.
255	−2.0000V	00000000

7

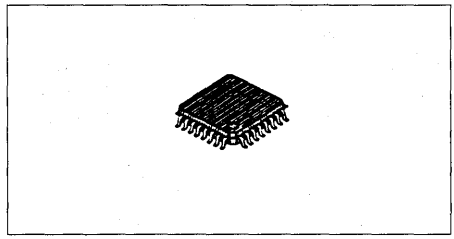
SONY **CXA1693Q**

Advanced Information

High Speed Sample and Hold IC

Description

The CXA1693Q performs high speed sample and hold of video and various type of signals.



32 pin QFP (Plastic)

Features

- Maximum sampling frequency
  40MHz (Minimum)
- Built-in -2V constant voltage circuit.
- Built-in clock pulse generating circuit for
  A/D converter
- Low power consumption
  180mW (Typical)

Absolute Maximum Ratings (Ta=25 °C)

• Supply Voltage	V_{CC}	7	V
	Vee	-7	V
• Write current	I_W	50	mA
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-65 to +150	°C
• Allowable power dissipation	P_D	375	mW

Structure

BiPolar silicon monolithic IC.

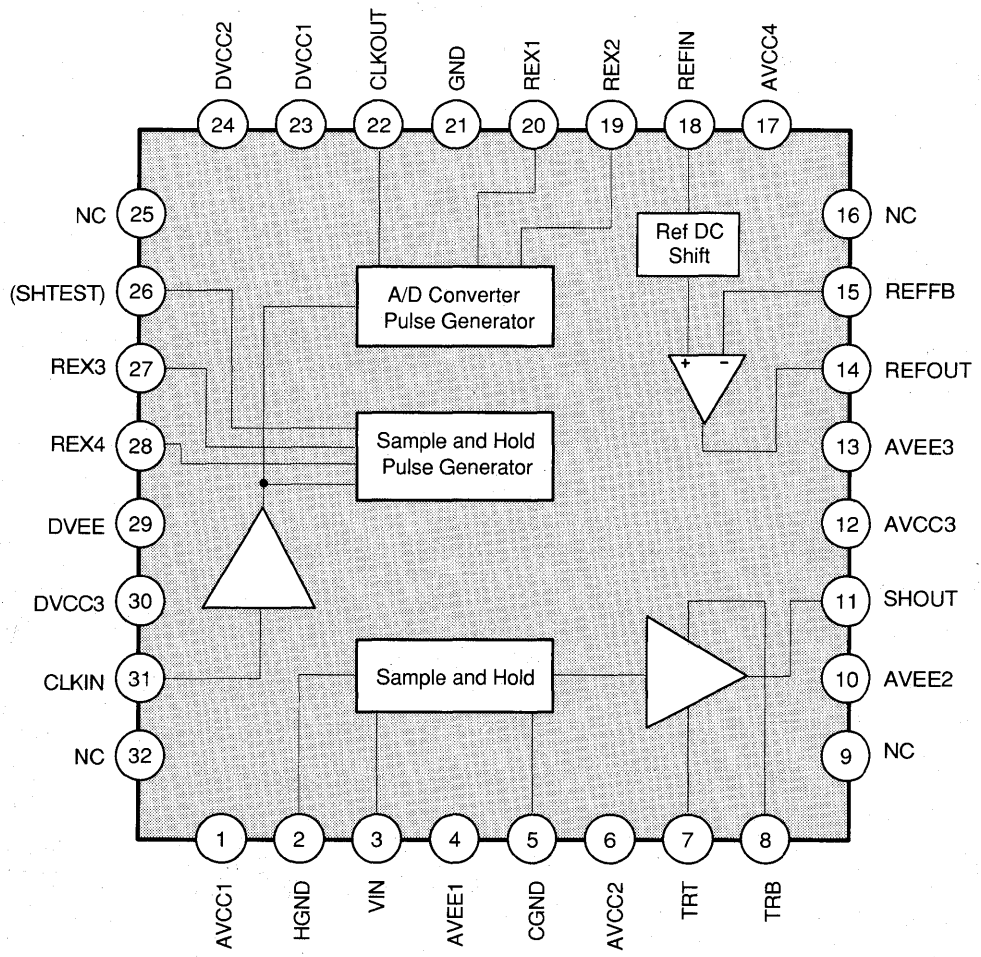
Operating Conditions

• Supply Voltage	V_{CC}	4.75 to 5.25	V
	Vee	-4.75 to 5.25	V

Application

Usage in combination with the CXA1694Q or CXA1496Q can simplify peripheral circuit design for A/D conversion.

Block Diagram

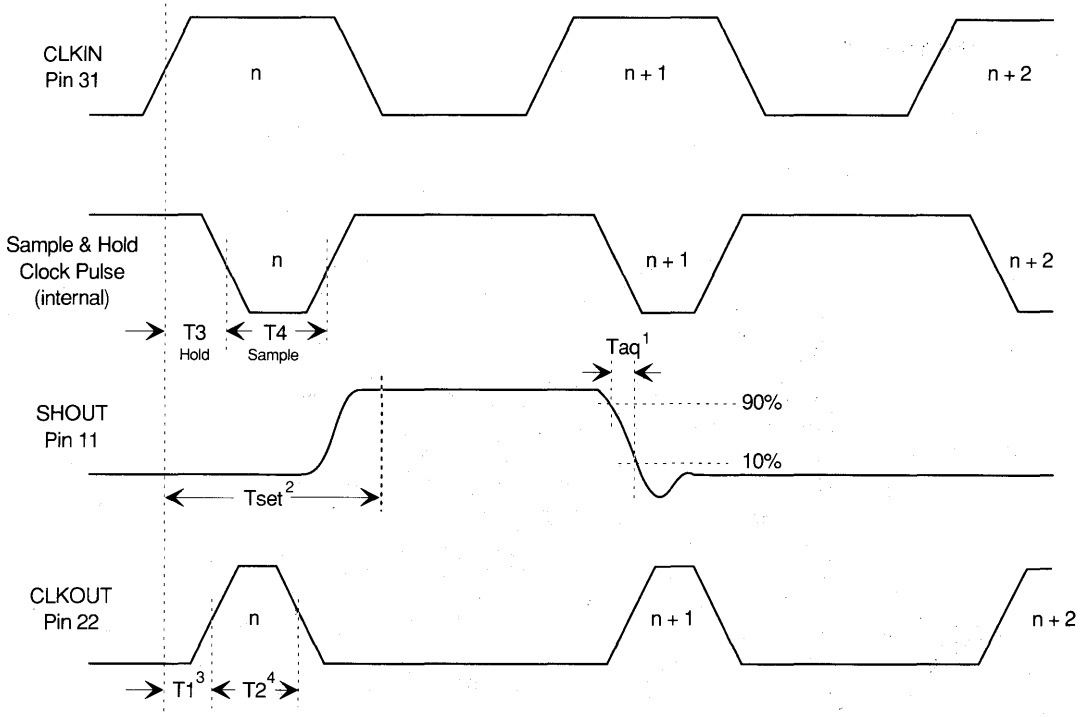


7

Electrical Characteristics

(V_{cc}=5V, V_{cc}= -5V, T_a=25 °C)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Maximum Operating Frequency	Fc		40			MHz
Curent Consumtion	Icc			20		mA
	Iee			16		mA
Acquisition time	Taq			8.7		nS*1
Settling time	Tset			42		nS*2
Droop rate	HMDR	Vin = -1V		6.7	20	mV/uS
Feed through	HMTH	Fin = 5MHz, Vin = 1Vp-p		-63		dB
SHOUT gain	Gsh	Vin = 2Vp-p, Fin = 100KHz		0		dB
SHOUT frequency responce	Fsh	20log (V(8M)/V(100K))		-0.1		dB
Input voltage range	Vin	Fin = 1KHz, Dist<-55dB	-2.5		0.2	V
Input current of VIN	Ivin	Vin = -1V			30	uA
CLKIN input voltage	Vclkl				1.5	V
	Vclkh		3.5			V
Input current of CLKIN	Iclk	Vclk = 0.5V	-300			uA
A/D Clock location	T1			20		nS*3
A/D Clock width	T2			12		nS*2
A/D clock high level	Vadch		Vcc -0.8			V
A/D Clock low level	Vadcl		Vcc -1.6			V
Pin 18 input current	Irefin				10	uA
Pin 15 output voltage	Vreffb		-2.2	-2.0	-1.8	V

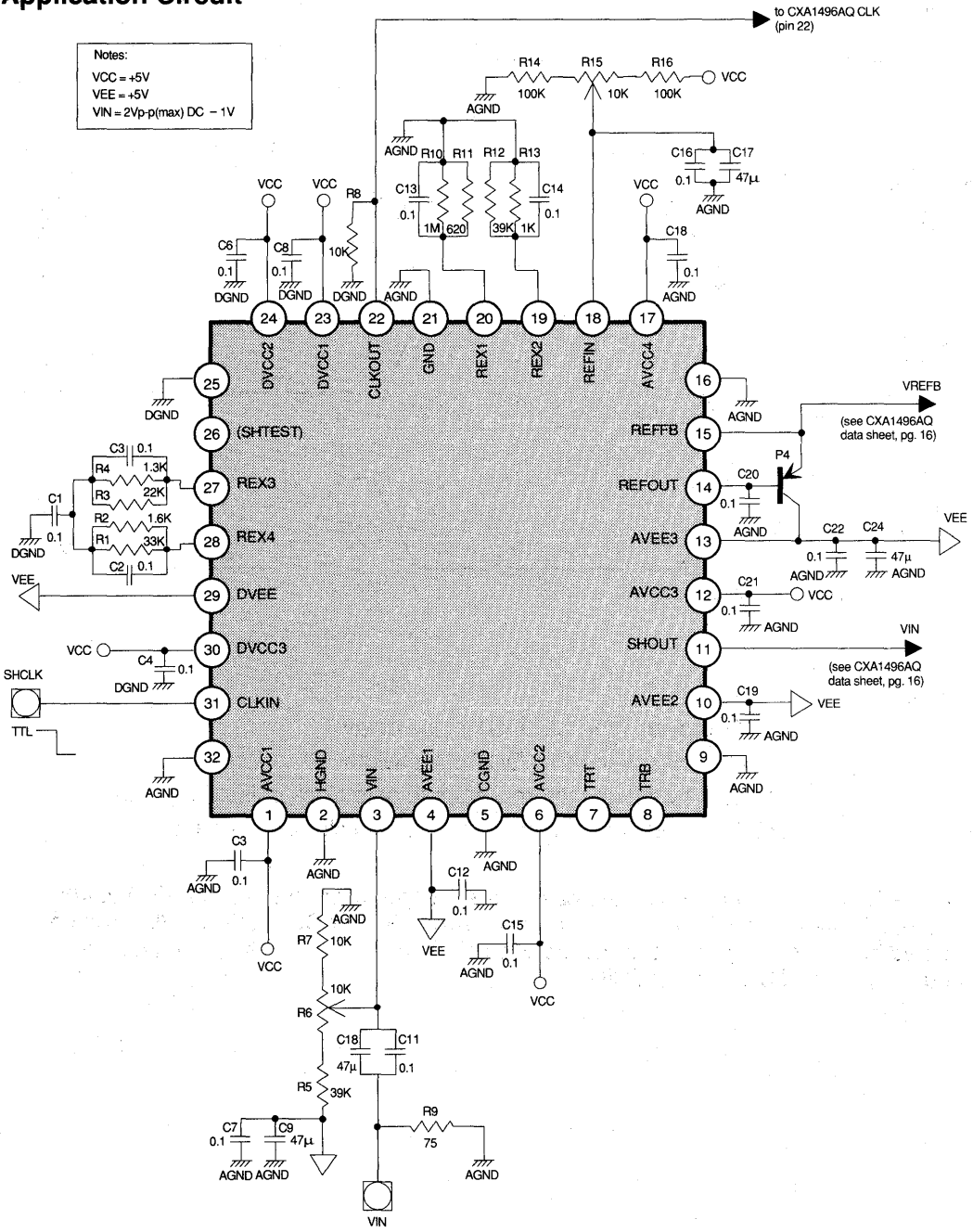


Note:

REX1 provides the CLKOUT pulse delay T1
REX2 provides the CLKOUT pulse width T2
REX3 provides the internal sample/hold clock pulse delay T3
REX4 provides the internal sample/hold clock pulse width T4

REFOUT (Pin 14) can drive up the base current of an external transistor (P1) to 400 uA. In order to give bias voltage at Pin 34 of the CXA1496Q or CXA1694Q. Pin 34 is connected to the emitter of the external transistor. (The external transistor must have enough gain and current capability.)

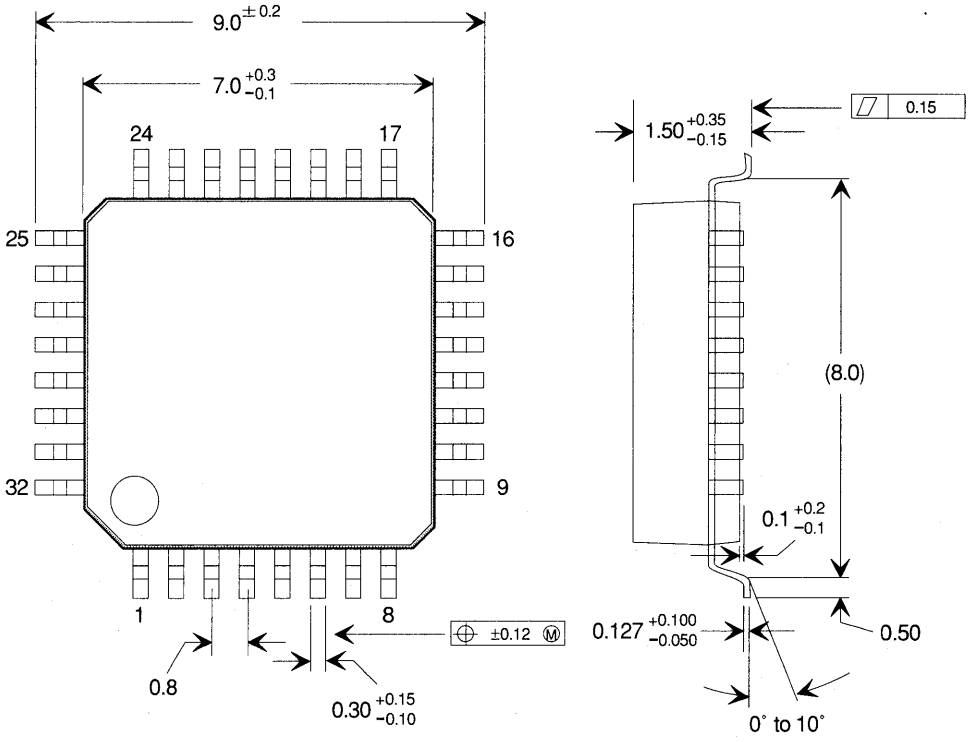
Application Circuit



Package Outline

Unit mm

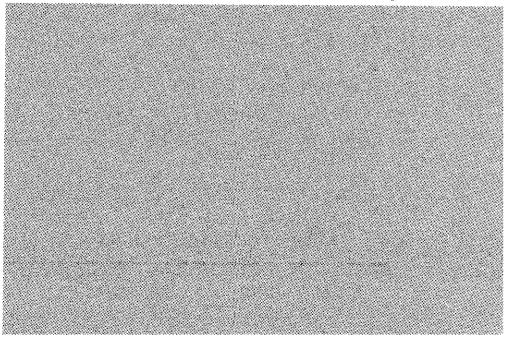
32-pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

7

A/D, D/A Converter for Audio Signal Processing



A/D, D/A Converter for Audio Signal Processing

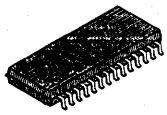
Part Number	Bit	Speed (MSPS)	P_D (mW)	Functions	Page
CXD1077M	10	-	120	TTL I/O A/D, D/A Audio	403-419
CXD2552Q	18	1024Fs	500	TTL OE Audio D/A	420-427
CXD2555Q	16	256 to 1024Fs		TTL OE Audio A/D, D/A	428-436

SONY

CXD1077M

8-mm Video AD/DA Converter

28 pin SOP (Plastic)



Description

CXD1077M is a 10-bit A/D, D/A converter developed for PCM audio of 8-mm video. It permits configuration of a PCM recording/playback system by combining it with the digital signal processing LSIs CX23011 and CX23012 and the analog noise reduction IC CX20099.

Features

- 5V single power supply
- Adoption of the integrating method achieves a low distortion factor 0.1% (Typ.), 5V in operation.
- The built-in integrator and sample-hold circuit reduces the number of external parts.
- The REC mode and the PB mode can be set with external signals.

Functions

- Sample-hold of input analog signal in the REC mode, and resample-hold of output analog signal in the PB mode.
- R time sharing A/D and D/A conversion based on the integrating method.
- Serial data input/output with LSB data leading.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to (V_{DD} + 0.3)	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

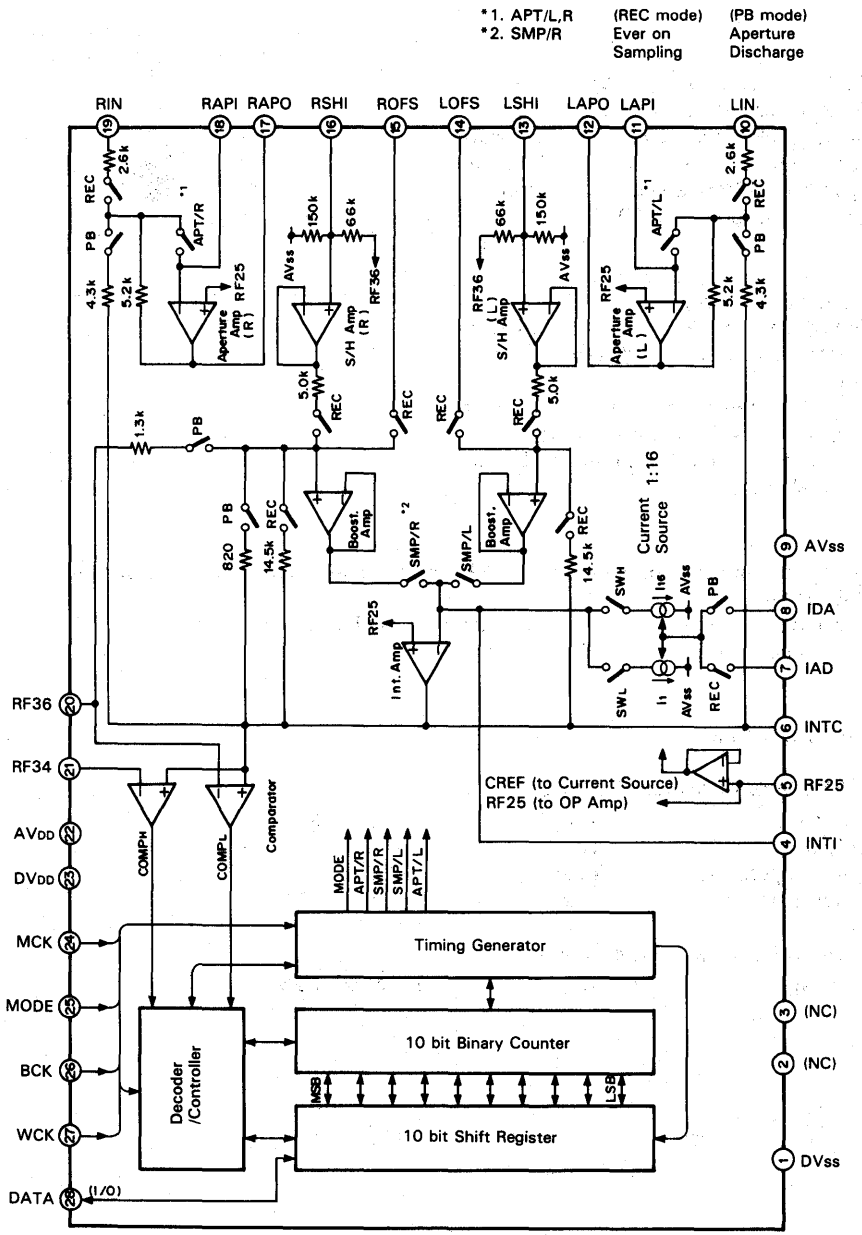
Recommended Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V

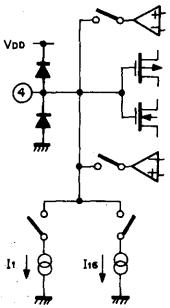
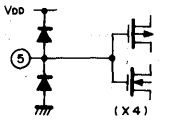
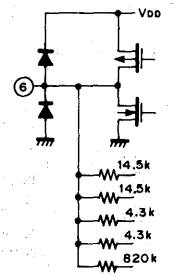
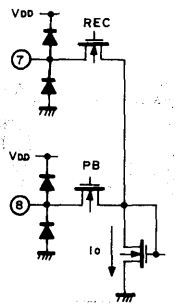
8

E89Z06 – ST

Block Diagram



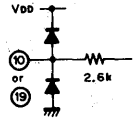
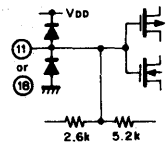
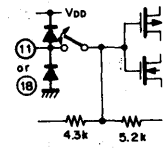
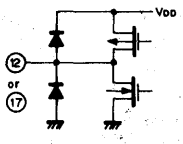
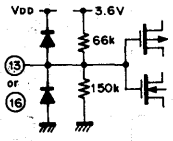
Pin Description

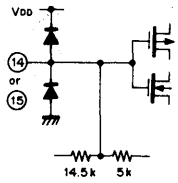
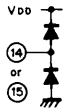
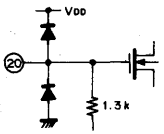
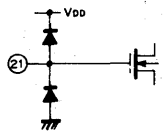
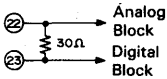
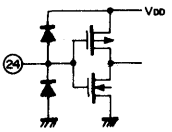
No.	Symbol	Voltage	I/O	Equivalent circuit	Description
1	DVss	0V			Digital ground pin
2	NC				Non connection
3	NC				Non connection
4	INTI	2.5V	I		Amplifier input pin for integrator (common to L and R). Integrating capacitor is externally connected between this pin and 6 INTO. Connected to forestage buffer amplifiers (separately for L and R) and two constant current supplies via respective analog switches. I1: 5 µA in REC mode, 3 µA in PB mode I16: 80 µA in REC mode, 48 µA in PB mode
5	RF25	*2.5V	I		Virtual ground potential setting pin for four inverted operational amplifiers. Externally supplies DC2.5V. Requires external connection of coupling capacitor.
6	INTO		O		Amplifier output pin for integrator (common to L and R). Integrating capacitor is externally connected between this pin and 4 INTI. (This pin permits observation of integrated wave form.)
7 8	IAD IDA	1.6 to 2.2V 1.3 to 1.9V	I I		Integrating current setting pins: 7 IAD for REC mode, and 8 IDA for PB mode. Current Io proportional to integrating current can be provided by externally connecting resistors between these pins and external reference voltage 3.6V. Io: 3.6 µA in REC mode 2.1 µA in PB mode A coupling capacitor of about 1 µF is externally attached to each of 7 and 8.

*) External voltage

8

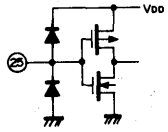
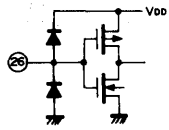
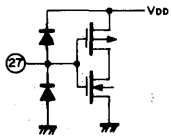
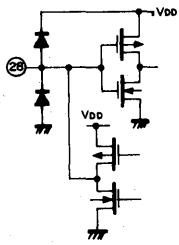
Pin Description

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
9	AVss				Analog ground pin.
10 19	L IN R IN		I I		Analog signal input pin (L, R). Appropriate full-scale input level is −10 dBs (0.693Vpp).
11 18	LAPI RAPI		I I	[REC mode]  [PB mode] 	Amplifier input pins (L, R) for aperture. Sample-hold circuit in PB mode (in the IC, the amplifier for sample & hold of PB is called "aperture amplifier," for the discrimination from the amplifier for sample & hold of REC "S/H amplifier") is configured by externally attaching a capacitor between 11 LAPI and 12 LAPO, or between 18 RAPI and 17 RAPO. The aperture amplifier serves as a simple input amplifier in REC mode, and Pins 11 and 18 make almost no sense.
12 17	LAPO RAPO		O O		Aperture amplifier (L, R) output pins. [In REC] Analog signal entered from 10 L IN and 19 R IN is amplified by about 6 dB and output from there. [In PB] Sample & hold wave form of DA conversion is output.
13 16	LSHI RSHI		I I		S/H Amplifier (Sample & Hold Amplifier: L, R) input pins. In REC, analog signal output from 12 LAPO or 17 RAPO passes through an externally connected low-pass filter and then is returned to IC from this pin. The value of AC level is substantially the same as that of 10 L IN and 19 R IN (−10 dBs full scale).

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
14 15	LOFS ROFS		I I	[REC mode]  [PB mode] 	Offset correction pins in REC (L, R). Offset in A/D conversion can be corrected by externally connecting a semi-fixed resistor between these pins and external reference voltage 3.6V and adjusting the DC level of these pins.
20	RF36	*3.6V	I		Pin for setting lower rank comparator comparison voltage in REC or discharge voltage in PB. Externally feeds DC3.6V. Requires external connection of a coupling capacitor.
21	RF34	*3.4V	I		Pin for setting upper rank comparator comparison voltage in REC. Externally feeds DC3.4V. Requires external connection of a coupling capacitor.
22 23	AVDD DVDD	*5V *5V			Analog power supply voltage pin and digital power supply pin. Externally supply DC5V. Requires external connection of a coupling capacitor.
24	MCK		I		Master clock input pin. (11.58 MHz) Only MCK is TTL-compatible.

*) External voltage

8

No.	Symbol	Voltage	I/O	Equivalent circuit	Description
25	MODE		I		REC mode/PB mode select input pin. "H" level: REC mode (A/D conversion) "L" level: PB mode (D/A conversion)
26	BCK		I		Bit clock input pin. Uses Pin 17 (BCK) output of CX23012 (CX23062) as shift clock for serial data.
27	WCK		I		Word clock input pin. (31.5 kHz) Used as an L/R channel identification signal of data, and "H" level: L channel data "L" level: R channel data in both REC (data output) and PB (data input). Uses output of Pin 18 (WCK) of CX23012 (CX23062) (in synchronization with the rise edge of BCK).
28	DATA		I/O		Data input/output pin. (2's complement) In REC: outputs 10-bit data in sync with the rise edge of BCK in the sequence of LSB, 2SB, ... MSB. In PB: inputs 10-bit data in sync with the fall edge of BCK in the sequence of LSB, 2SB, ..., MSB. L/R channels are alternately switched over in accordance with H/L of WCK.

Electrical Characteristics

Ta = 25°C Vpp = 5V (See Fig. 1 to 3)

Item		Symbol	Condition	Pin	Min.	Typ.	Max.	Unit
REC mode	Input impedance	Zin		10, 19		2.6		kΩ
	Full-scale input level	Vin		10, 19		−10		dBs
	Analog input gain	Gin	Aperture amplifier gain			6.0		dB
	Total harmonics distortion + noise	THD_1	Level = 1 dB, see Test method in 8-1.			0.10	0.14	%
		THD_2	Level = 6 dB, see Test method in 8-1.			0.18	0.20	%
PB mode	Total harmonics distortion + noise	THD_2	Level = 0 dB, see Test method in 8-2.			0.10	0.14	%
		THD_4	Level = 6 dB, see Test method in 8-2.			0.18	0.20	%
Power consumption		I_{DD}				24	36	mA

Test method of total harmonics distortion + noise in PB mode

The total harmonics distortion + noise characteristics (D/A conversion characteristics) in PB mode is measured by a method as shown in Fig. 1. Enter WCK and BCK generated by MCK (11.58 MHz) and CX23012 into CXD1077M, and at the same time, enter 0 dB (full-scale level) or −6 dB digital sine-wave data (1 kHz), and measure the total harmonics distortion + noise at this moment. Set −10 dBs (0.245 Vms) upon 0 dB input as the PB output level (interpolation filter output level) by adjusting the semi-fixed resistor 1 MΩ connected to the PB mode integrating current setting pin 8.

Test method of total harmonics distortion + noise in REC mode

The total harmonics distortion + noise characteristics (A/D conversion characteristics) in REC mode is measured by a method as shown in Fig. 2. Enter WCK and BCK generated by MCK (11.58 MHz) and CX23012 into CXD1077M, and at the same time, enter −11 dBs (full-scale level −1 dB) or −16 dBs (full-scale level −6 dB) sine-wave (1 kHz) as analog signal, and DA-convert the A/D-converted data with the reference playback DAC (provide another DAC previously adjusted so that a PB output level of −10 dBs is reached upon input of full-scale data, by the method described in the above). Make setting by adjusting the semi-fixed resistor 4.7Ω connected to S/H amplifier input Pins 13 and 16 so that the analog level becomes equal to the analog output level (interpolation filter output) of reference playback DAC (REC level adjustment). It is however necessary to previously adjust offset so that the wave form may not be clipped by the semi-fixed resistor 22Ω connected to the offset correction Pins 14 and 15, while observing the output wave form of the reference playback DAC when the input is near the full scale (offset adjustment is possible also by the method shown in the DC offset adjustment in REC on page 15).

After the completion of the adjustment as described above, measure the sum of total harmonics distortion + noise of analog output (interpolation filter output) of the reference playback DAC, and use the result as the REC mode conversion characteristics of the tested device.

8

Electrical Characteristics Test Circuit
(For total harmonics distortion factor and noise characteristics in PB mode)

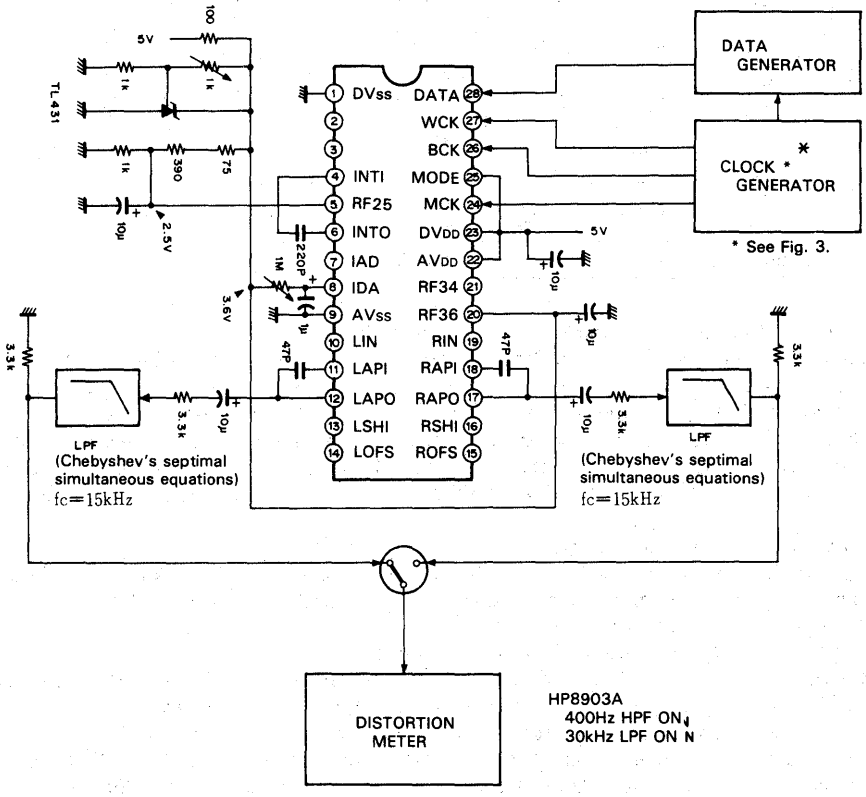
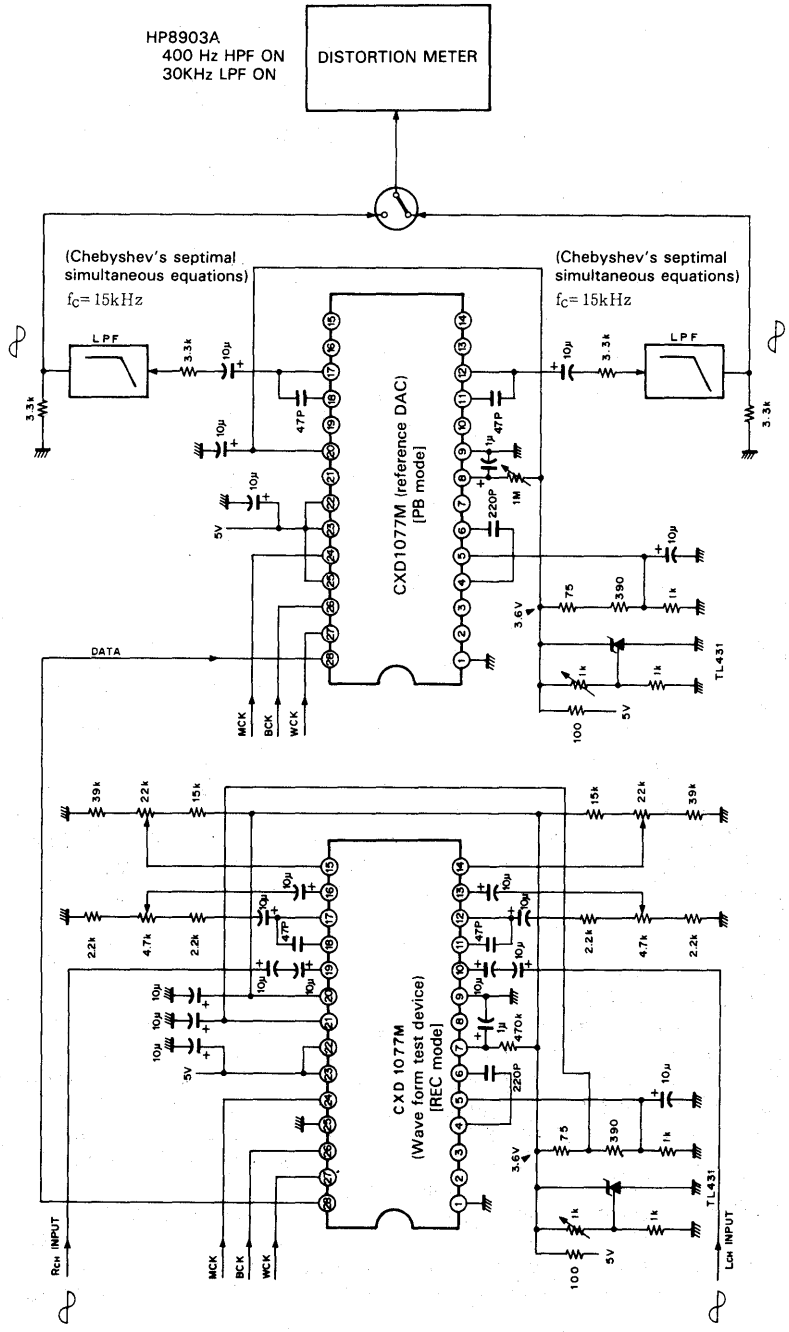


Fig. 1

Electrical Characteristics Test Circuit
(For total harmonics distortion factor and noise characteristics in REC mode)



Clock Generator Circuit
(For testing total harmonics distortion factor and noise characteristics)

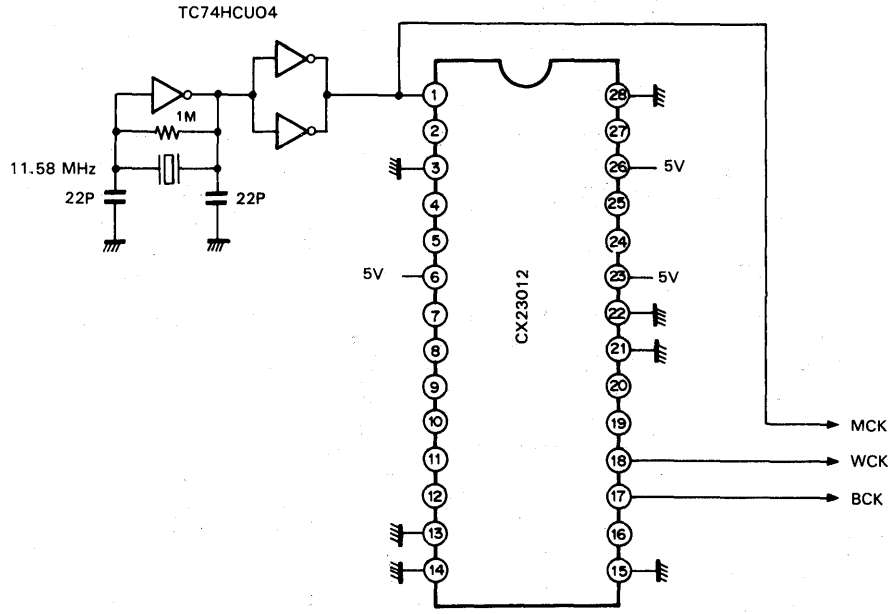


Fig. 3

Description of Function

The CXD1077M is a single-chip 10-bit A/D, D/A converter provided with every function required in A/D and D/A conversion. Particularly when combined with CX23011 (for modulation, demodulation and error correction), CX23012 (A/D, D/A interface) and CX20099 (analog noise reduction), it is used in the PCM processor for 8-mm video.

Description of REC mode function

1) Selection of operational mode
   REC mode (A/D conversion mode) is selected by setting the MODE signal to "L".
2) Analog block operation and gain
   The input signal applied to the analog signal input pins 10 and 19 is amplified by about 6 dB by the aperture amplifier and output to the aperture output pins 12 and 17. After component out of band area is removed from the output signal by the external attenuation filter, it is added to the sample-hold input pins 13 and 16 and output to the integrating output pin 6 after amplification by about 9.25 dB by the sample-hold amplifier.
   This gain is obtained assuming that the external filter's insertion loss is −6 dB. Therefore, the overall gain will be about 9.25 dB when the filter is included. Even when the external filter's insertion loss is different from the above value, or its insertion position is different, it is necessary to achieve an overall gain of about 9.25 dB. For details, refer to the REC level adjustment on page 16.

3) Digital block operation and clock (see Fig. 4: REC mode timing chart)
The Convert Command (C.C.) is generated internally by entering WCK and BCK. While C.C. is at "H", the analog signal applied to the S/H amplifier is sampled, and while C.C. is at "L", the constant current weighted with inverse polarity against the input signal is integrated by the integrating circuit for conversion. The 10-bit data is performed by calculating the integrating time of the coarse constant current and fine constant current separately using a counter. An MCK frequency of 11.58 MHz is used for 8-mm video as the counter clock frequency required when conducting full-scale A/D conversion. In the CXD1077M, it is necessary to maintain mutual synchronization of MCK, WCK and BCK because of the necessity of converting operation to be in synchronization with MCK, irrespective of the phase relationship of MCK with WCK or BCK. The data is loaded, on the other hand, in the shift register when C.C. becomes "H" again and is output serially with LSB leading in synchronization with the rise edge of BCK. The data is coded in 2's complement.

4) Integrating current in REC
The integrating current value $I_{A/D}$ required when performing a full-scale A/D conversion in the CXD1077M is obtained by the following equation:

$$I_{A/D} = \frac{C \cdot V_I}{1023 \tau_o}$$

where, C : Integration Capacitance
V_I : Integrator output voltage, and
τ_o : MCK cycle.

According to Fig. 6 representing an example of application circuit, C = 220pF, V_I = 2Vp-p' and τ_o = 86 ns (MCK frequency: 11.58 MHz), leading to an integrating current value of about 5 μA. The integrating current setting is done by applying an external constant current to the Rec mode integrating current setting pin 7 through a resistor from an external reference voltage (3.6V). Supposing a setting resistor value of 470 kΩ, the constant current applied to pin 7 has a value of about 3.6 μA (reference value), corresponding to an integrating current value of about 5 μA.

5) Comparison voltage and virtual ground voltage
Switching between the upper conversion and lower conversion is performed by the integrating output 6 surpassing the comparison voltages 20 RF36 and 21 RF34 in the next stage comparator. The integrating output based coarse constant current surpassing RF34 (about 3.4V) causes switching from the upper to lower conversion, and the integrating output based on fine constant current surpassing RF36 (about 3.6V) causes the lower conversion to end.
Since the CXD1077M operates with a single 5-V power supply, it is necessary to apply a virtual ground voltage of 2.5V to a non-inverted input of the internal operational amplifier. This voltage is applied to 5 RF25.

6) DC offset
As 8-mm video uses a non-linear quantization by 10-bit ⇋ 8-bit compression/expansion, compatibility is affected when a DC offset component is included in the A/D conversion data in recording. When the analog signal input is so large as being close to the full-scale level, the A/D conversion data may be clipped on a single side of positive or negative. To correct this DC offset, the integrating output's center voltage must be shifted by applying an offset voltage to the offset correcting pins 14 and 15. As to details, refer to the DC offset adjustment in REC mode on page 15.

8

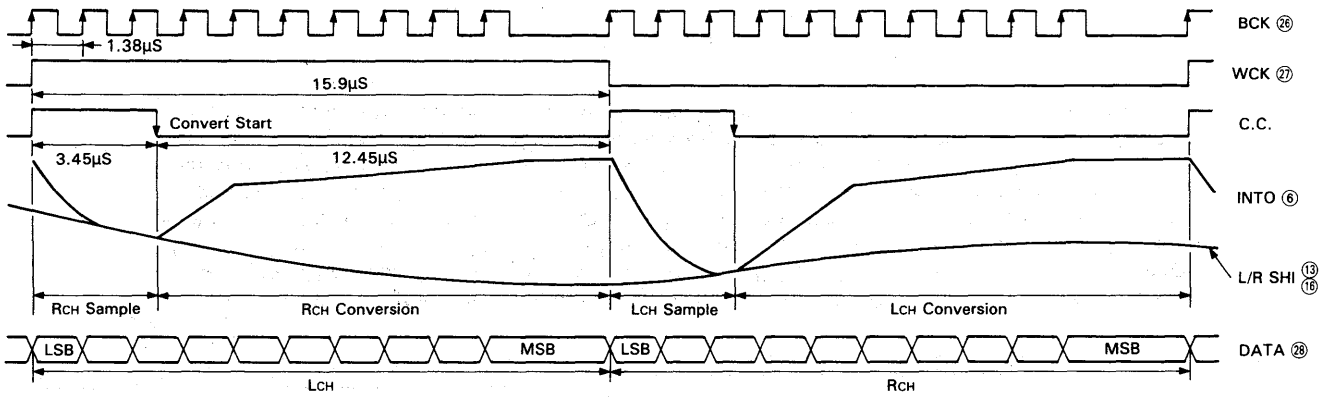
Description of PB mode operation

1) Selection of operation mode
   By setting the MODE signal to "H", the PB mode (D/A conversion mode) is selected.
2) Digital block operation and clock (refer to Fig. 5: PB mode timing chart)
   DIS (Discharge clock) and APT (Aperture clock) are generated internally in the CXD1077M, by entering WCK and BCK. The serial data input with LSB leading is stored in the shift register in synchronization with the falling edge of BCK and set in the counter while DIS is "H". When DIS becomes "L", the counter starts counting, beginning from the value set in it, and at the same time, a constant current weighted corresponding to data is output. When the counter outputs the carry signal, the counting and constant current output stop. The counter clock frequency required when performing a full-scale D/A conversion is 11.58 MHz (MCK frequency) for 8-mm video.
3) Analog block operation and gain
   The integrating charge resulting from the previous conversion is discharged while DIS is "H" by sampling the external reference voltage 3.6V applied to 20 RF36 by means of the integrator. As a result, the integrating output in the discharge region is initialized to about 1.8V, and the output center voltage in input of sine-wave data becomes about 2.5V. When DIS goes to "L", D/A conversion operation is executed by integrating the constant current output. When the constant current output stops, integrating also stops, and the pin voltage held in the integrated capacitor at this moment takes the D/A converted value. This pin voltage is output, after being amplified by about 1.6 dB by the aperture amplifier, to the aperture output pins 12 and 17. Output signal's out-of-band components are removed by an external interpolation filter.
4) PB integrating current
   Integrating current $I_{D/A}$ required when performing full-scale D/A conversion in the CXD1077M is determined from the following equation:

$$I_{D/A} = \frac{C \cdot V_I}{1023\tau_o}$$

   According to Fig. 6 representing an example of application circuit, C = 220pF, V_I = 1.2Vp-p' and τ_o = 86 ns, leading to an integrating current value of about 3μA. The integrating current setting is one by applying an external constant current to the playback mode integrating current setting pin 8 through a resistor from an external reference voltage (3.6V). Supposing a setting resistor value of 910 kΩ, the constant current applied to pin 8 has a value of about 2.1 μA (reference value), corresponding to an integrating current value of about 3 μA. It is possible to adjust the D/A conversion output level by altering this setting resistor. For details, refer to the PB level adjustment on page 15.

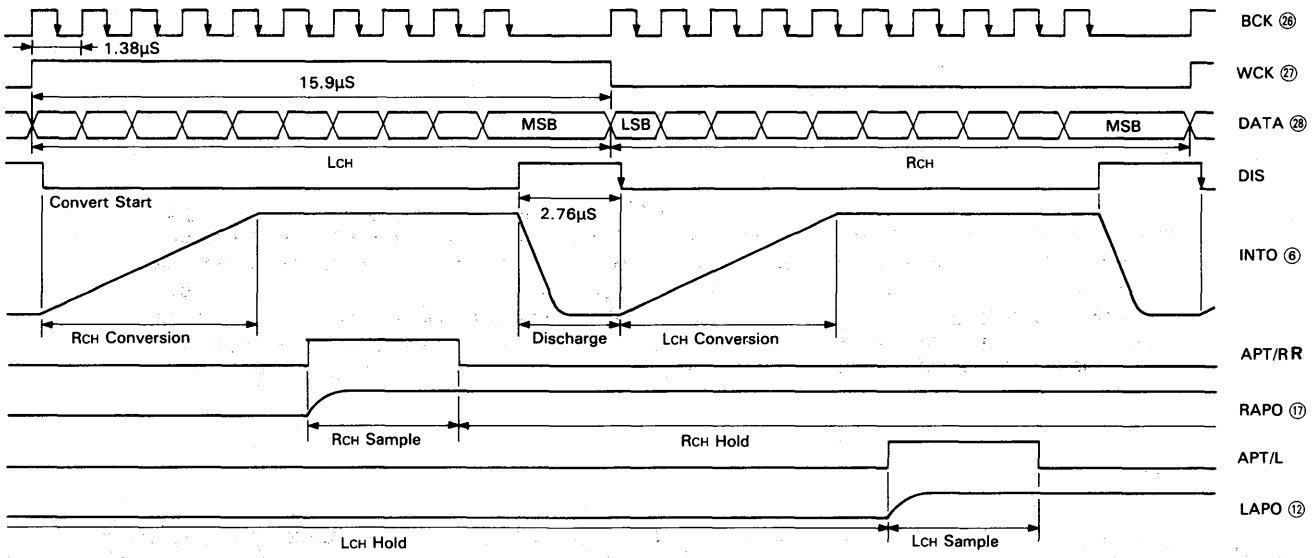
Timing Chart of REC Mode



When the MODE signal (pin 25) of the CXD1077M is set to "L", REC mode (A/D conversion mode) is selected. When BCK and WCK are entered from CX23012 (AD/DA interface LSI) in this mode, C.C. (Convert Command) is generated internally in the CXD1077M. While this C.C. is at "H" level, the analog signal input is sampled; A/D conversion is executed during "L" level. The sampling and conversion operations are performed in time division for each of the R and L channel analog signals. The converted final data is output serially with the LSB data leading in synchronization with the rise edge of BCK when the C.C. becomes "H" level again.

Fig. 4

Timing Chart of PB Mode



When the MODE signal (pin 25) of the CXD1077M is set to "H", PB mode (D/A conversion mode) is selected. When BCK and WCK are entered from CX23012 (A/D, D/A interface LSI) in this mode, DIS (Discharge clock) and APT R/L (Aperture clock) are generated internally in the CXD1077M. At the same time, the serial data input with the LSB leading is stored in synchronization with the fall edge of BCK. After DIS has discharged at "H" level, the integrating charge resulting from the previous D/A conversion, D/A conversion starts when DIS goes to "L" level. The discharge and conversion operations are performed in time division for each of the R and L channel data inputs. The final integrated output after conversion is sampled while APT R/L is at "H" and held at "L" level.

Fig. 5

Notes for Application and Adjustment Methods

(see Fig. 6. Application circuit)

As the conversion accuracy obtained is affected by the accuracy of parts used and adjustment in the CXD1077M, attention should be given to the following points:

Selection of parts to be used

1) For the integrating capacitor between pins 4 and 6, use a type with little dielectric absorption (e.g. styrol capacitor).
2) Adjust the semi-fixed resistor 1 kΩ so that the reference voltage generated from the reference voltage IC (TI's TL431) is 3.6V.
3) For the low-pass filters to be inserted between pins 12 and 13 and between pins 16 and 17, use passive-type ones with an input/output impedance of 3.3 kΩ, respectively.
4) Accuracy tolerance of the three divided resistors, 75 Ω, 390 Ω, and 1 kΩ, supplying voltage to pins 5 and 21 is 5%.

PB level adjustment

In adjustment of the PB level during D/A conversion, use a 470 kΩ semi-fixed resistor connected to pin 8. Input to pin 28 a full-scale level digital sine-wave data (1 kHz), and adjust the semi-fixed resistor so that the PB level (interpolation filter output level) becomes −10 dBs (0.245 Vrms).

REC level adjustment

Adjustment of REC level during A/D conversion can be accomplished by the use of a 470 kΩ semi-fixed resistor connected to pin 7 as well, in addition to the method described in 8-2 above. Apply a −16 dBs (−6 dB of full-scale level) sine wave (1 kHz) to pins 10 and 19 as the analog input signal, and conduct D/A conversion of the A/D-converted data by means of a reference playback DAC (prepare another DAC adjusted previously by the method mentioned in the PB level adjustment above so that the playback output level becomes −10 dBs when entering full-scale data). Adjust the semi-fixed resistor so that the reference playback DAC output level becomes equal to the analog signal input level (−16 dBs) to the tested A/D converter.

DC offset adjustment in REC

In the offset adjustment of A/D-converted data during A/D conversion, use a 22 kΩ semi-fixed resistor connected to pins 14 and 15. In practice, adjust the semi-fixed resistor so that the data output of pin 28 becomes "0000000000" when DC2.5V is applied as the analog input level of pins 10 and 19. In this adjustment, do not fail to conduct offset adjustment only after the completion of REC level adjustment as described in the REC level adjustment above.

Frequency characteristics

The CXD1077M frequency characteristics in REC is determined by an input attenuation filter. Meanwhile the frequency characteristics in PB is determined by the aperture effect and output interpolation filter. With the CXD1077M, degradation of high area frequency characteristics caused by the aperture effect is unavoidable. This is because a sample-hold aperture circuit is used to obtain −10 dBs as the interpolation filter output level during full-scale D/A conversion. To compensate the degraded characteristics, add a compensation filter, as shown in Fig. 7, with inverted response characteristics.

8

Application Circuit

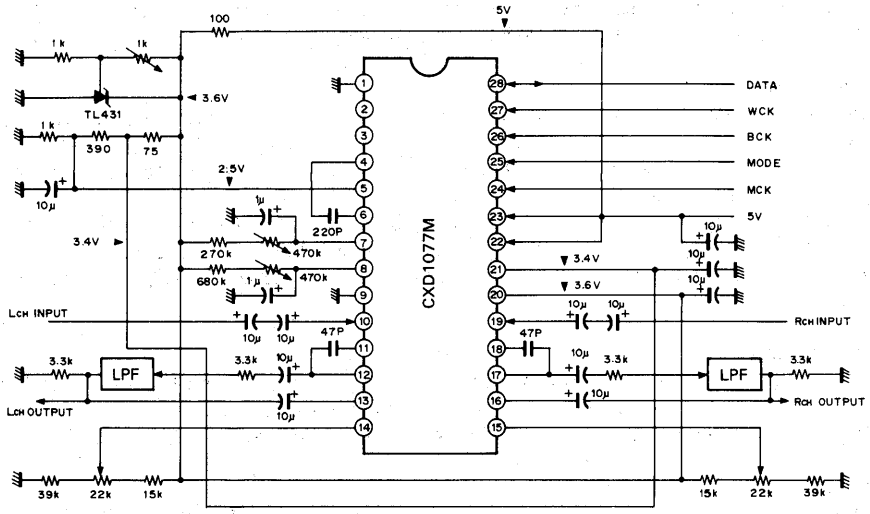


Fig. 6

Compensation characteristics of aperture effect

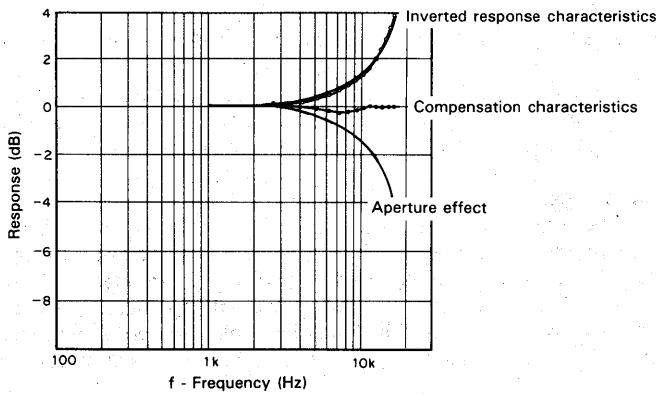
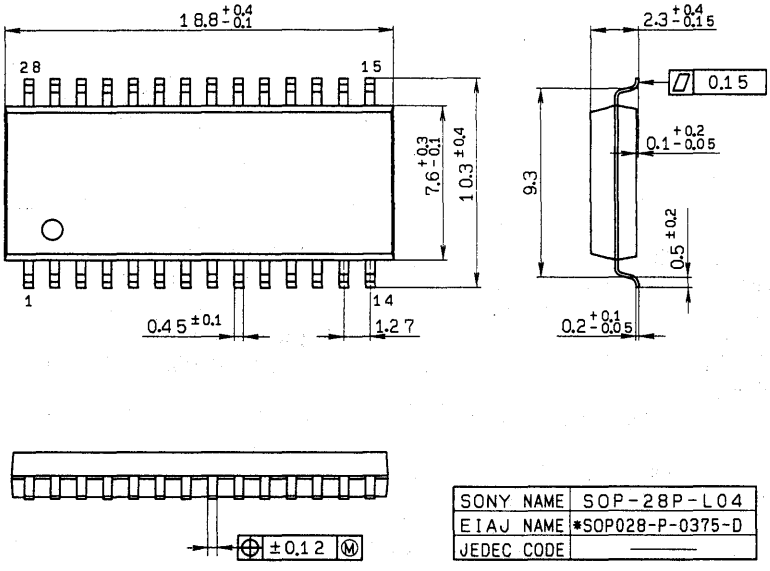


Fig.7

Package Outline Unit : mm

28 pin SOP (Plastic) 375mil 0.7g



SONY NAME	SOP-28P-L04
EIAJ NAME	*SOP028-P-0375-D
JEDEC CODE	———

8

SONY®

CXD2552Q

1 Bit D/A Converter

Description

The CXD2552Q is 1 bit type D/A converter developed for digital audio products; compact disc player and others.

44 pin QFP (Plastic)

Features

- PLM pulse converter
- 3rd order noise shaper
- Direct digital sync
- Master clock 1024Fs
- 2 channel built in

Absolute Maximum Ratings

- Supply voltage V_{DD} −0.5 to +6.5 V
- Input voltage V_I −0.3 to V_{DD}+0.3 V
- Allowable power dissipation
  P_D 500 mW (Ta=60°C)
- Storage temperature
  Tstg −55 to +150 °C

Structure

Silicon gate CMOS IC

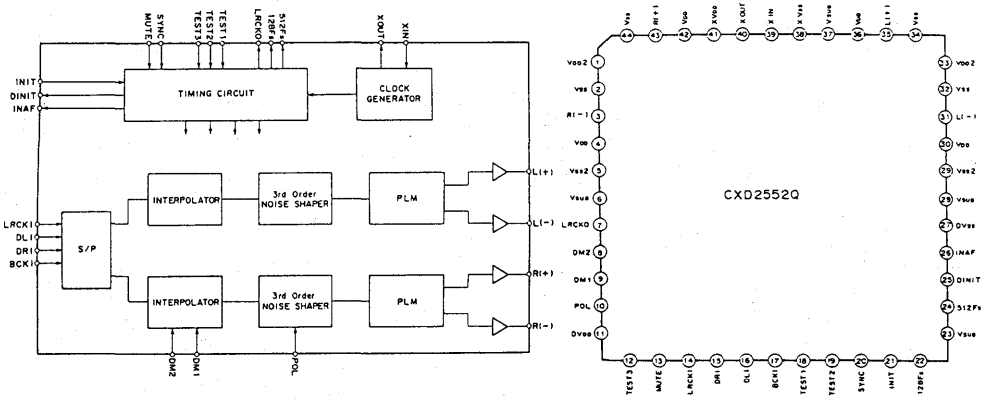
Applications

Compact disc player, digital amplifier, BS tuner

Recommended Operating Conditions

- Supply voltage V_{DD} 4.75 to 5.25 V
- Operating temperature Topr −10 to 60 °C
- OSC frequency fx 32.0 to 49.7 MHz
- Supply voltage difference
  V_{DD}–V_{DD2}, V_{DD}–DV_{DD}, V_{DD}–XV_{DD} ± 0.1V
  V_{SS}–V_{SS2}, V_{SS}–DV_{SS}, V_{SS}–XV_{SS} ± 0.1V

Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	V_{DD2}	——	Analog power supply
2	Vss	——	Analog GND
3	R (–)	O	Rch PLM output (Opposite phase)
4	V_{DD}	——	Analog power supply
5	V_{SS2}	——	Analog GND
6	V_{SUB}	——	Sub straight. Connect to GND.
7	LRCKO	O	LRCK output
8	DM2	I	Dither polarity
9	DM1	I	Dither designation
10	POL	I	PLM output polarity "L" : Positive phase "H" : Opposite phase
11	DV_{DD}	——	Digital power supply
12	TEST3	I	Test pin. Fixed at "L" level in normal operation mode.
13	MUTE	I	Turns interpolator output into 0 data. Effective at "H".
14	LRCKI	I	LRCK input
15	DRI	I	Rch data input
16	DLI	I	Lch data input
17	BCKI	I	BCK input
18	TEST1	I	Test pin. Fixed at "L" level in normal operation mode.
19	TEST2	I	Test pin.Fixed at "L" level in normal operation mode.
20	SYNC	I	Sync control pin
21	INIT	I	Resynchronized by rising edge of this signal
22	128Fs	O	128Fs output
23	V_{SUB}	——	Sub straight. Connect to GND.
24	512Fs	O	512Fs output
25	DINIT	O	Delay INIT signal output
26	INAF	O	When I/O sync is missed "H" is output.
27	DVss	——	Digital GND
28	V_{SUB}	——	Sub straight. Connect to GND.
29	V_{SS2}	——	Analog GND
30	V_{DD}	——	Analog power supply
31	L (–)	O	Lch PLM output (Opposite phase)
32	Vss	——	Analog GND
33	V_{DD2}	——	Analog power supply
34	Vss	——	Analog GND
35	L (+)	O	Lch PLM output (Positive phase)
36	V_{DD}	——	Analog power supply
37	V_{SUB}	——	Sub straight. Connect to GND.

Pin No.	Symbol	I/O	Description
38	XVss	——	Clock GND
39	XIN	I	Crystal oscillation input pin (1024Fs)
40	XOUT	O	Crystal oscillation output pin
41	XV_{DD}	——	Clock power supply
42	V_{DD}	——	Analog power supply
43	R (+)	O	Rch PLM output (Positive phase)
44	Vss	——	Analog GND

Electrical Characteristics

DC Characteristics

(V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V ± 5%, Vss=V_{SS2}=DVss=XVss=0V, Topr=–10 to 60°C)

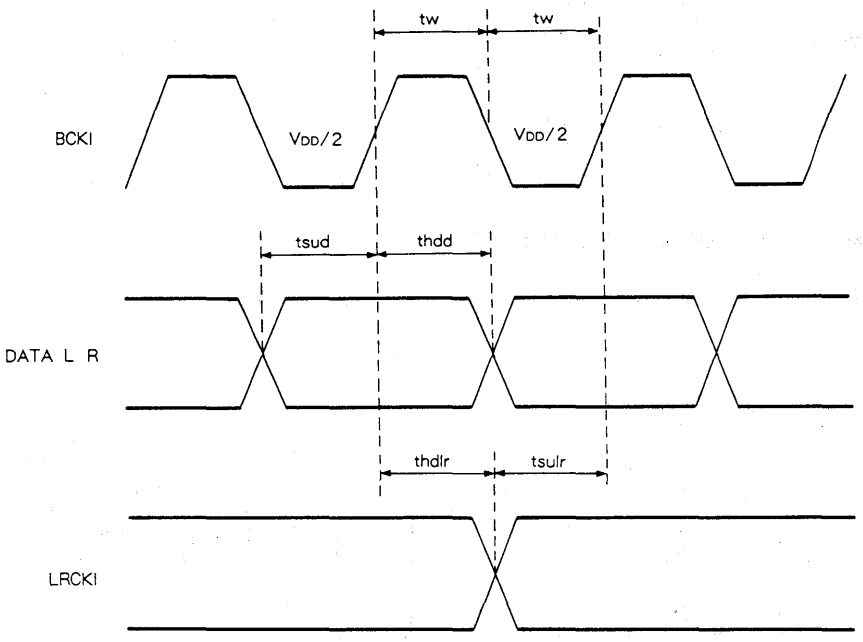
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	——	0.76V_{DD}			V
"L" input voltage	V_{IL}	——			0.24V_{DD}	V
Input leak current	I_{LI}	——			± 5.0	µA
"H" output voltage (DINIT, INAF)	V_{OH}	Io=–1mA	V_{DD}–0.5			V
"L" output voltage (DINIT, INAF)	V_{OL}	Io=1mA			0.4	V
"H" output voltage (512Fs, LRCKO)	V_{OH}	Io=–0.4mA	V_{DD}–0.5			V
"L" output voltage(512Fs, LRCKO)	V_{OL}	Io=0.4mA			0.4	V
"H" output voltage (128Fs)	V_{OH}	Io=–0.3mA	V_{DD}–0.5			V
"L" output voltage (128Fs)	V_{OL}	Io=0.3mA			0.4	V
"H" output voltage (R+, R–, L+, L–)	V_{OH}	Io=–15mA	V_{DD}–0.5			V
"L" output voltage (R+, R–, L+, L–)	V_{OL}	Io=15mA			0.5	V
"H" output voltage (XOUT)	V_{OH}	Io=–2.0mA	V_{DD}–0.5			V
"L" output voltage (XOUT)	V_{OL}	Io=2.0mA			0.4	V
Current consumption	I_{DD}	——		55	80	mA

AC Characteristics

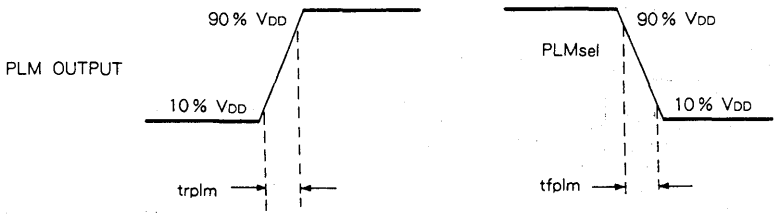
(V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V ± 5%, Vss=V_{SS2}=DVss=XVss=0V, Topr=–10 to 60°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BCKI pulse width	tw		38			nsec
DATAL, R set up time	tsud		18			nsec
DATAL, R hold time	thdd		18			nsec
LRCKI set up time	tsulr		18			nsec
LRCKI hold time	thdlr		18			nsec
PLM output rise/fall time	tr, tf	CL=300pF		10		nsec

• **Input**



• **Output**



8

Analog Characteristics ($V_{DD}=V_{DD2}=DV_{DD}=XV_{DD}=5.0V$, $V_{SS}=V_{SS2}=DV_{SS}=XV_{SS}=0V$, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Total harmonic distortion	THD	1kHz, 0dB data (Fs=44.1kHz)			0.0030	%
S/N ratio	S/N	1kHz, 0dB/– ∞ dB data (Fs=44.1kHz) (A filte used)	96			dB

Electrical Characteristics Testing Method

The testing of total harmonic distortion and S/N ratio is shown in Fig. 1. and 2.

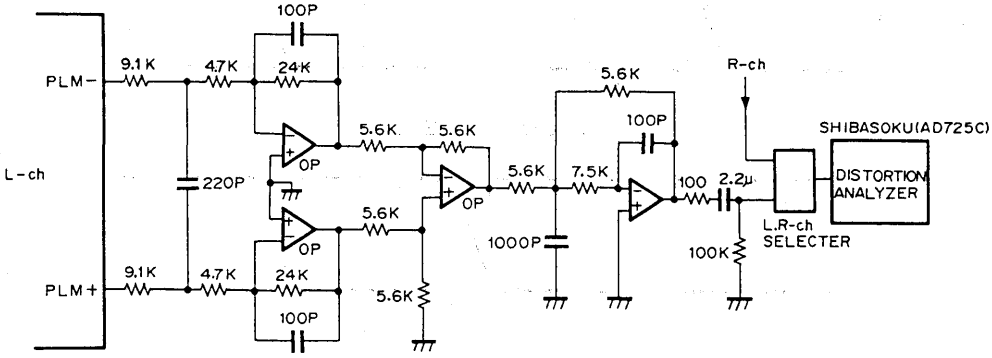


Fig. 1.

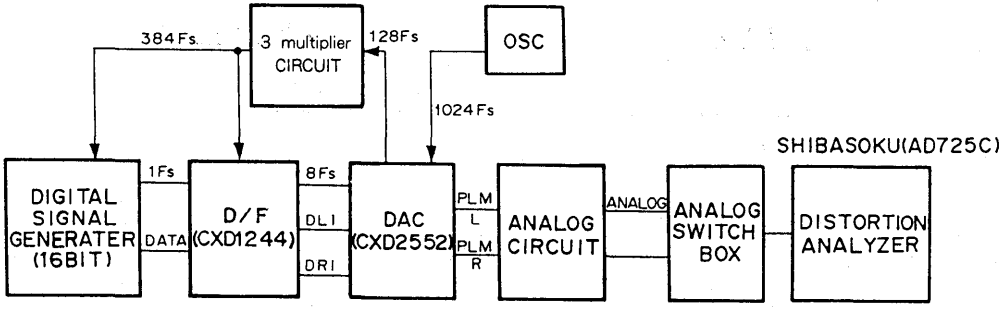


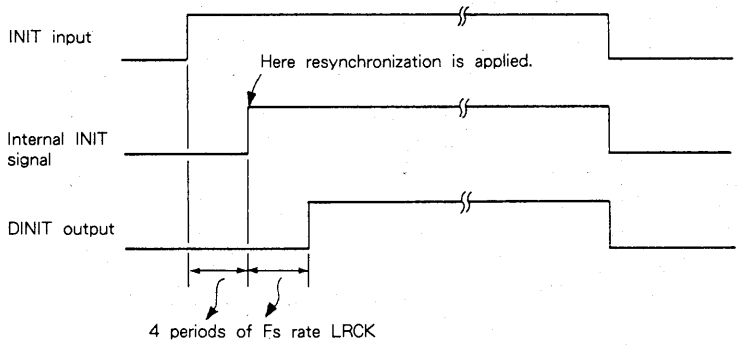
Fig. 2.

Description of Function

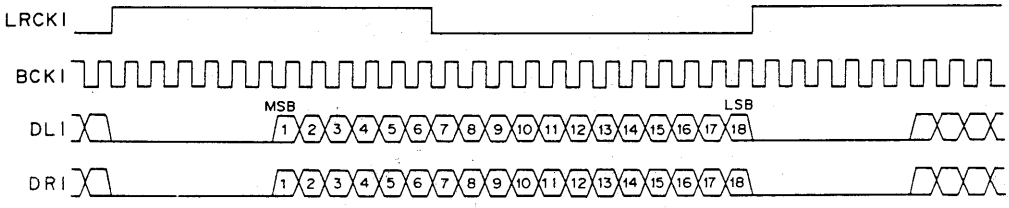
I/O Synchronizing Circuit

1) Theory of operation
A window featuring 8 internal clocks (256Fs) is set. The sync circuit observes whether the rising edge (LRCK ⌐) of the LRCK input has entered the window or not.
When power supply is turned on, should LRCK ⌐ be out of the window, the sync circuit stops the internal processing in timing with the center of the window. The processing is started synchronously with the appearance of the next LRCK ⌐. Synchronization between the exterior system and this LSI is established through this operation.

2) Resynchronization by means of INIT
Even when LRCK ⌐ is inside the window but located close to one of the two edges of the window, synchronization may be upset by the mingling of external noise. To this effect, it is necessary to apply resync without fail after power supply is turned on. Resync operation is executed from the rising edge of INIT and timed after 4 periods of Fs rate LRCK. The sync circuit is initialized and LRCK ⌐ is located at the center of the window.
Moreover, when synchronization falls out of the window, INAF output turns to "H" level.

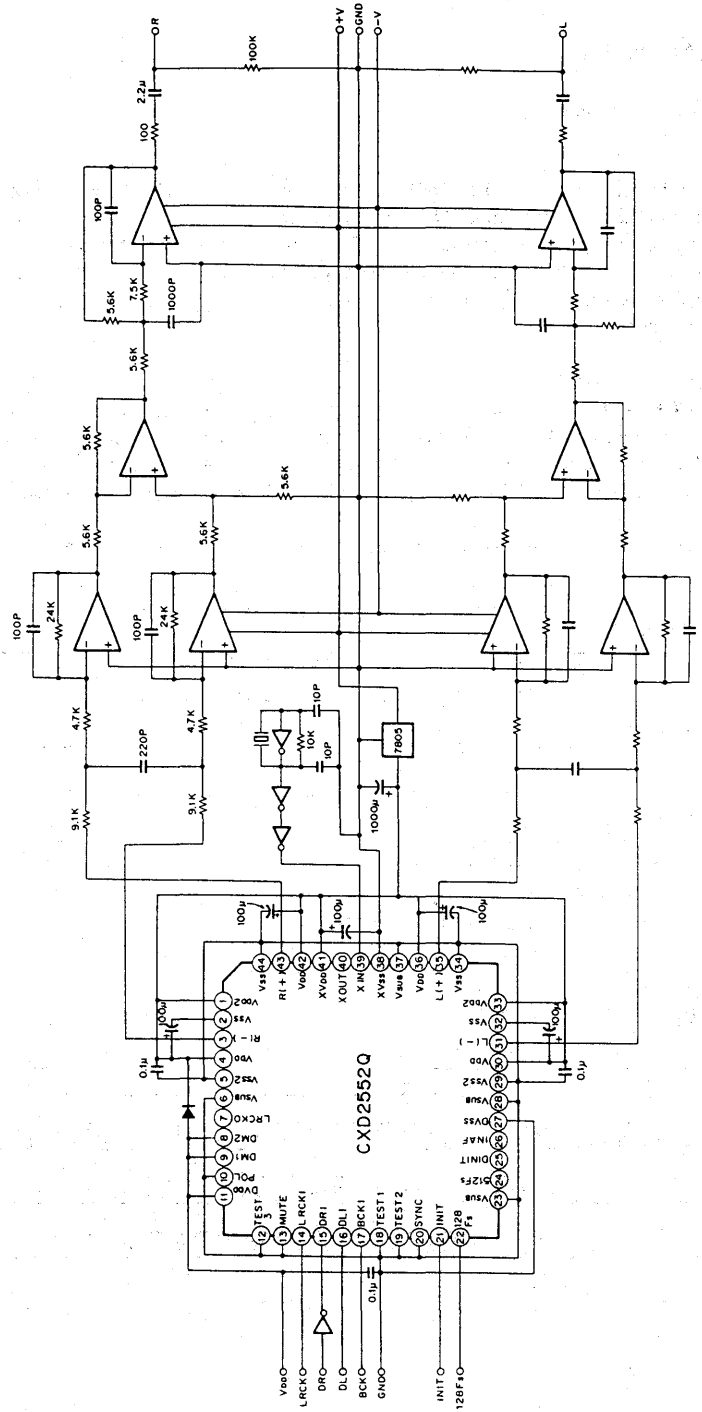


Input Timing (8fs rate)



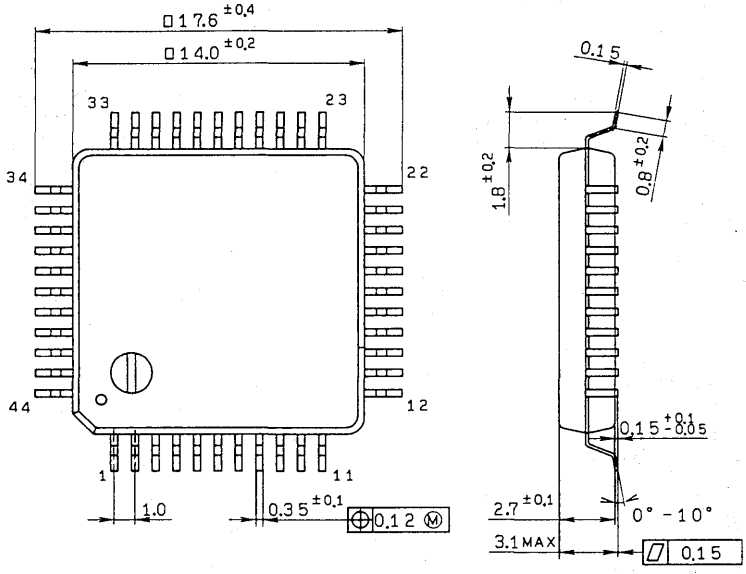
8

Application Circuit



Package Outline Unit : mm

44pin QFP (Plastic) 1.1g



SONY NAME	QFP-44P-L122
EIAJ NAME	*QFP044-P-1414-AX
JEDEC CODE	———

8

Audio Delta Sigma Type A/D+D/A+D/F

ADVANCED INFORMATION

CXD2555Q is a delta sigma type (2nd order delta sigma noise shaping) A/D & D/A with a digital filter.

48pin QFP (Plastic)

Features

- Two Channel A/D, D/A with over-sampling, Decimation digital filter.
- Analog circuit for A/D included
- Distortion level: 0.01% (A/D, D/A)
- S/N: 90dB for D/A
  80dB for A/D

Functions

- 1 Fs data rate I/O possible
- Multi chip system possible
- Serial data inter face:32 slot
  Right/Left Adjusted Data
  MSB/LSB first in selections
- Master clock Selection:
  256Fs/512Fs/768Fs/1024Fs
- Fs selection:
  8KHz/16KHz/32KHz/44.1KHz/48KHz
- Provides several clock outputs, devided by a masterclock

Description of Operation

1. Serial Data Interface LRCK, BCK, SOUT, SIN, MASL, MLSL

Serial data format is same for both SIN and SOUT - 2's complementary 2 channel serial data. Each channel has 16bit data at 32bit slot. MASL mode select the 16bit data timing - data comes first or later. MLSL mode select MSB first or LSB first.

MASL	
H	Data First
L	Data Late

MASL	
H	MSB first
L	LSB first

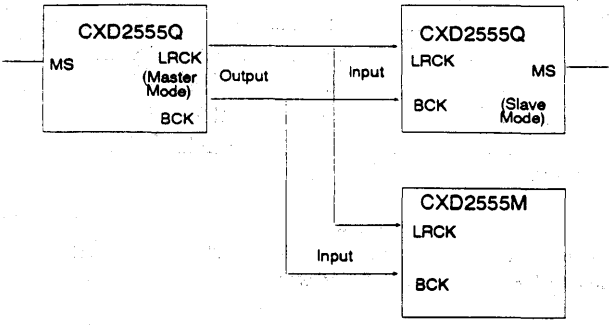
2. Master Mode/Slave Mode MS, LRCK, BCK

When multiple chips are used together, one of the ICs is used as "Master" and output LRCK, BCK. Other ICs are receiveing these clocks as "Slave" chips.

MS	Mode	LRCK, BCK I/O
H	Master Mode	Output
L	Slave Mode	Input

2. (Con't) Slave Mode

(Example)



3. Crystal Oscillation Frequency Select XTLI, XTLO, XSLO, XSL1, UCLK, XCLK.

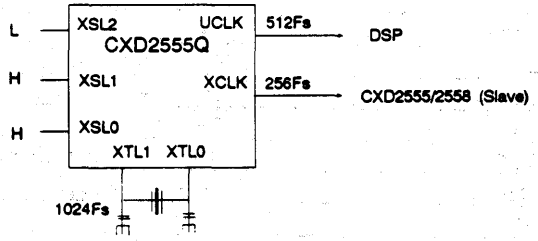
If XSL2 = "L" the crystal frequency is selected by XSL0 and XSL1 as shown in Table 1.

If XTLI receives CMOS level input signal, XTL0 should open.

XSL2	XSL1	XSL0	Crystal Freq	XCLK	UCLK
L	L	L	256Fs	256Fs	128Fs
L	L	H	512Fs	256Fs	256Fs
L	H	L	768Fs	256Fs	384Fs
L	H	H	1024Fs	256Fs	512Fs

Table 1 - Crystal Frequency Select

(Example)



8

4. Low Frequency Fs Mode XTLI, XTL0, XSL0, XSL1, XSL2

If XSL2 = "H", Low frequency sample rate (Fs=8KHz, 16KHz) can be selected as shown in Table 2.

XSL2	XSL1	XSL0	Crystal Freq.	*Low Freq. Fs Mode
H	L	L	256x32KHz	16KHz
H	L	H	256x32KHz	8KHz
H	H	L	512x32KHz	16KHz
H	H	H	512x32KHz	8KHz

Table 2 - Low Fequency Fs Mode Select.

*32KHz based crystal frequency gives these Fs frequencies.
If 44.1KHz is base frequency then Low Frequency Fs are either 22.05KHz or 11.025KHz.
If 48KHz is base frequency then Low Frequency Fs are either 24KHz or 12KHz.

5. D/A Output Mode Selection

D/A Output Mode	Common	Differential
DASL0	L	H
DASL1	L	L

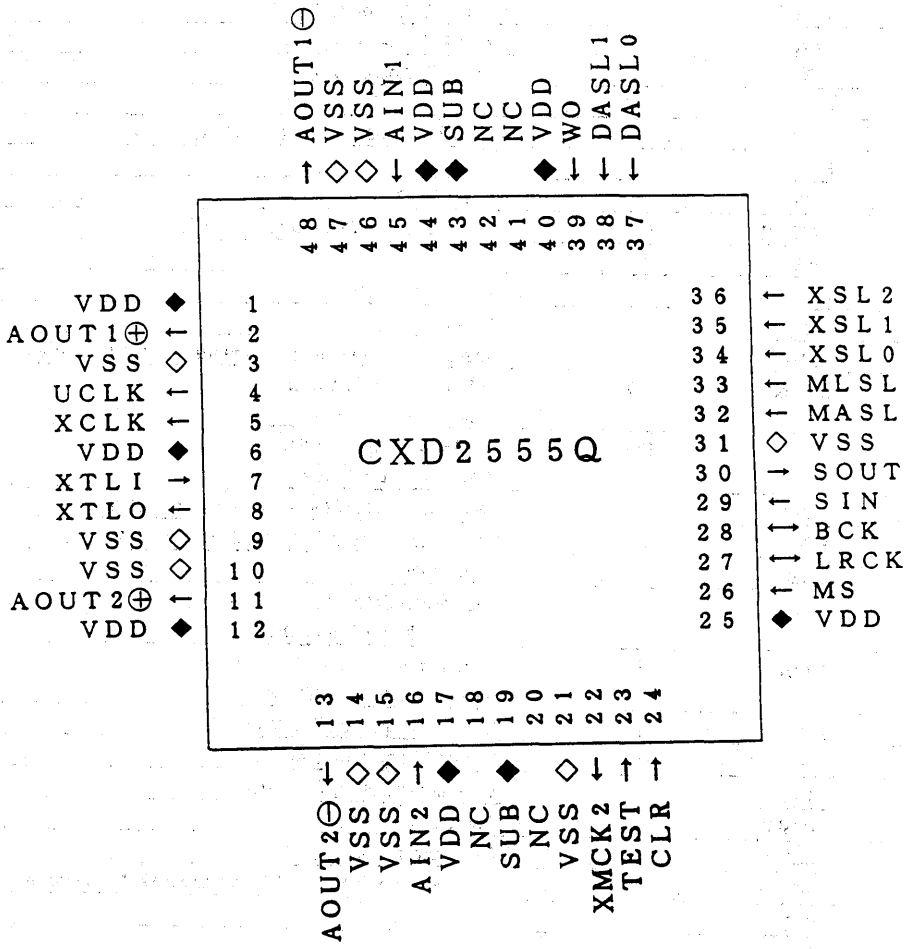
Mode Application
Common: Low output impedance, use "+" pin only.
Differential: Common noise cancel.

Pin Description

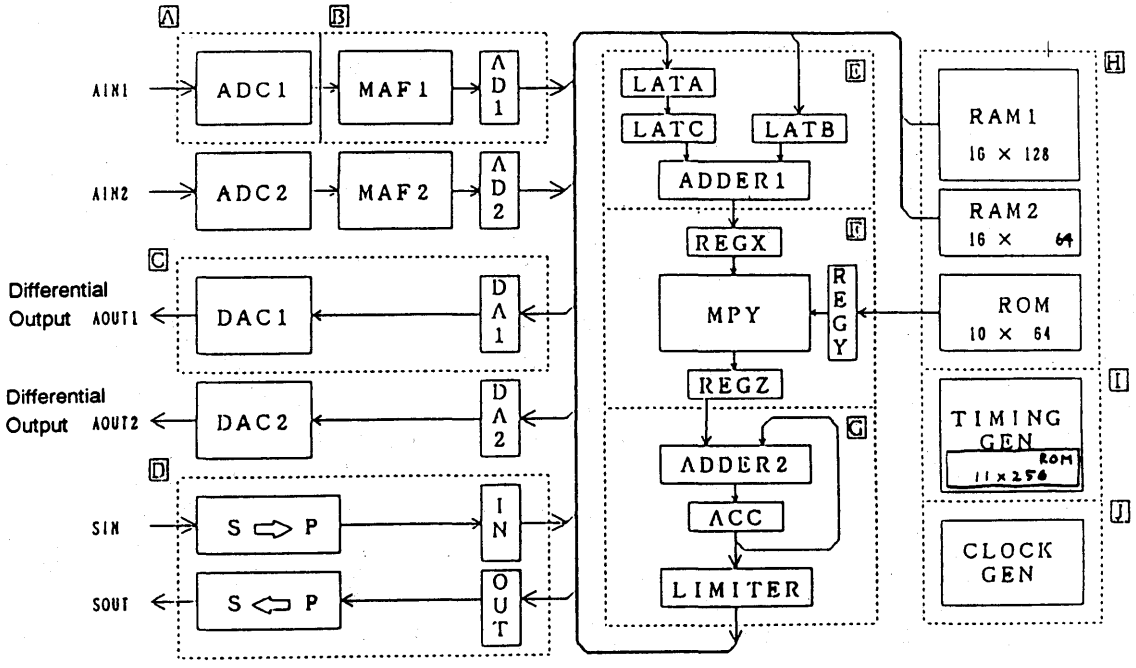
Pin No.	Symbol	I/O	Description
1	VDD	-	CH-1 D/A Analog Vcc
2	AOUT1+	O	CH-1 D/A Analog Output (+)
3	VSS	-	CH-1 D/A Analog GND
4	UCLK	O	User clock output 1/2 of master clock frequency
5	XCLK	O	256Fs Clock output
6	VDD	-	Digital Vcc
7	XTLI	I	Oscillating input for Master Clock. Crystal freq. is dependent upon the selection of XSLO 0~2
8	XTLO	O	Oscillating output for Master Clock
9	VSS	-	Digital GND
10	VSS	-	CH-2 D/A Analog GND
11	AOUT2+	O	CH-2 D/A Analog Output (+)
12	VDD	-	CH-2 D/A Analog Vcc
13	AOUT2-	O	CH-2 D/A Analog Output (-)

Pin Description (Con't)

Pin No.	Symbol	I/O	Description
14	VSS	-	CH-2 D/A Analog GND
15	VSS	-	CH-2 A/D Analog GND
16	AIN2	I	CH-2 A/D Analog Input
17	VDD	-	CH-2 A/D Analog Vcc
18	NC	-	
19	SUB	-	IC SUB terminal AC couple to GND
20	NC	-	
21	VSS	-	Digital GND
22	XMCK2	O	Over Sampling Clock Output (128Fs)
23	TEST	I	Test Pin
24	$\overline{CLR}$	I	$\overline{Clear}$ (Active Low)
25	VDD	-	Digital Vcc
26	MS	I	Master/Slave Selection "H"-Master Mode, "L"-Slave Mode
27	LRCK	I/O	If MS="H" Output Mode. If MS="L" Input Mode
28	BCK	I/O	If MS="H" Output Mode. If MS="L" Input Mode
29	SIN	I	Serial Data Input (2's complementary, 32bit slot)
30	SOUT	O	Serial Data Output (2's complementary, 32bit slot)
31	VSS	-	Digital GND
32	MASL	I	16bit serial data slot selection "H"-data first "L"-data late
33	MLSL	I	Selection for MSB first or LSB first "H"-MSB first "L"-LSB first
34	XSLO	I	Crystal Frequency Selection
35	XSL1	I	Crystal Frequency Selection
36	XSL2	I	Crystal Frequency Selection
37	DASL0	I	D/A Output Select
38	DASL1	I	D/A Output Select
39	WO	I	Window Open Mode "H"-Window Mask, "L"-Window Open
40	VDD	-	Digital Vcc
41	NC	-	
42	NC	-	
43	SUB	-	IC Subterminal AC Couple to GND
44	VDD	-	CH-1 A/D Analog Vcc
45	AIN1	I	CH-1 A/D Analog Input
46	VSS	-	CH-1 A/D Analog GND
47	VSS	-	CH-1 D/A Analog GND
48	AOUT1-	O	CH-1 D/A Analog Output (-)


CXD2555Q
1 VDD
2 AOUT1⊕
3 VSS
4 UCLK
5 XCLK
6 VDD
7 XTLI
8 XTLO
9 VSS
10 VSS
11 AOUT2⊕
12 VDD
13 AOUT2⊖
14 VSS
15 VSS
16 AIN2
17 VDD
18 NC
19 SUB
20 NC
21 VSS
22 XMCK2
23 TEST
24 CLR
25 VDD
26 MS
27 LRCK
28 BCK
29 SIN
30 SOUT
31 VSS
32 MASL
33 MLSL
34 XSL0
35 XSL1
36 XSL2
37 DASL0
38 DASL1
39 WO
40 VDD
41 NC
42 NC
43 SUB
44 VDD
45 AIN1
46 VSS
47 VSS
48 AOUT1⊖

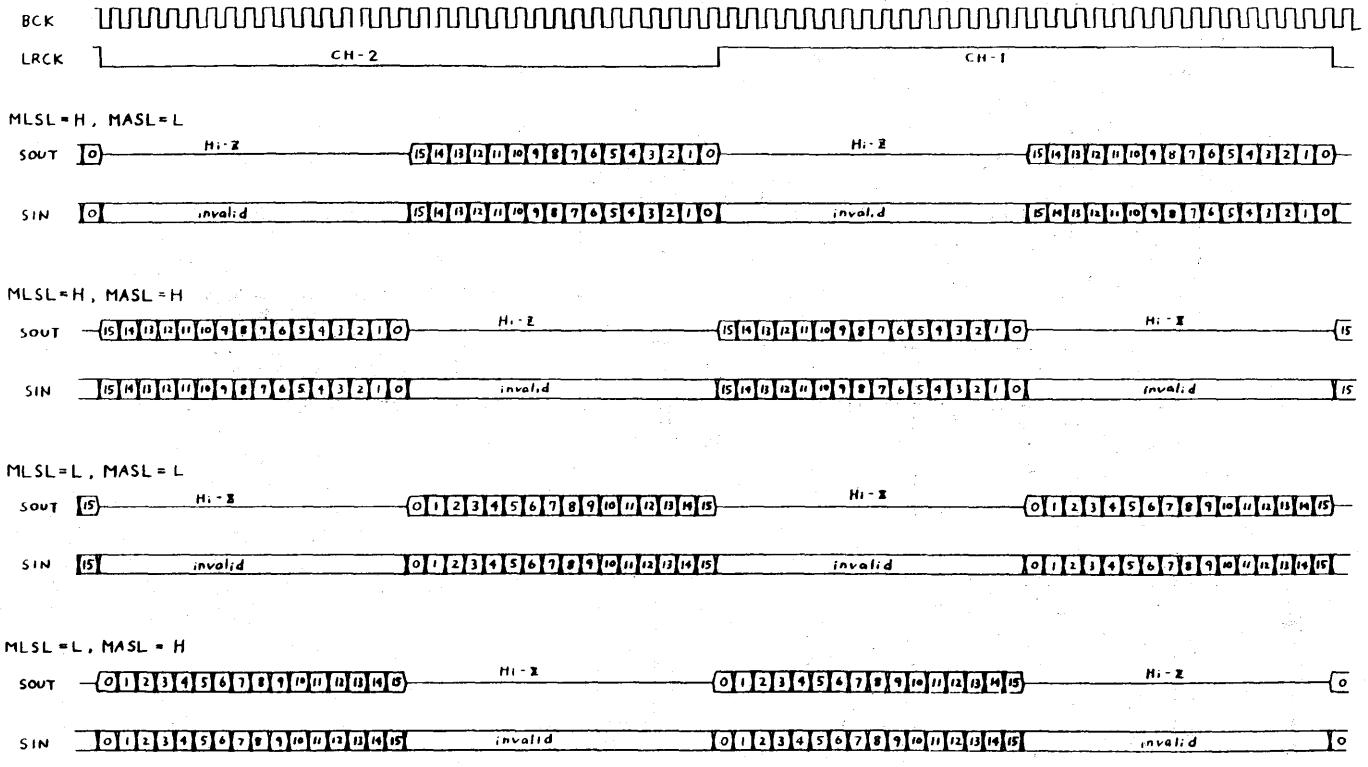
ADC/DAC Block Diagram



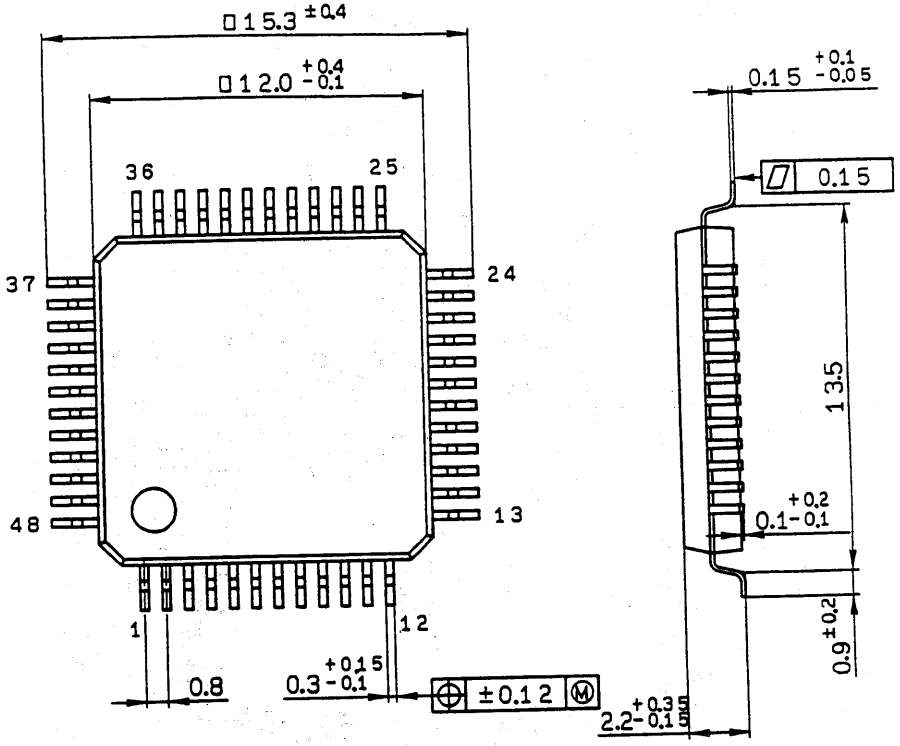
Block Name

A : ADC
B : MAF
C : DAC
D : I/F
E : ADD
F : MPY
G : ACC
H : MEM
I : TIM
J : CLK

8


BCK
LRCK
CH-2
CH-1
MLSL=H, MASL=L
SOUT
SIN
Hi-Z
invalid
MLSL=H, MASL=H
SOUT
SIN
Hi-Z
invalid
MLSL=L, MASL=L
SOUT
SIN
Hi-Z
invalid
MLSL=L, MASL=H
SOUT
SIN
Hi-Z
invalid

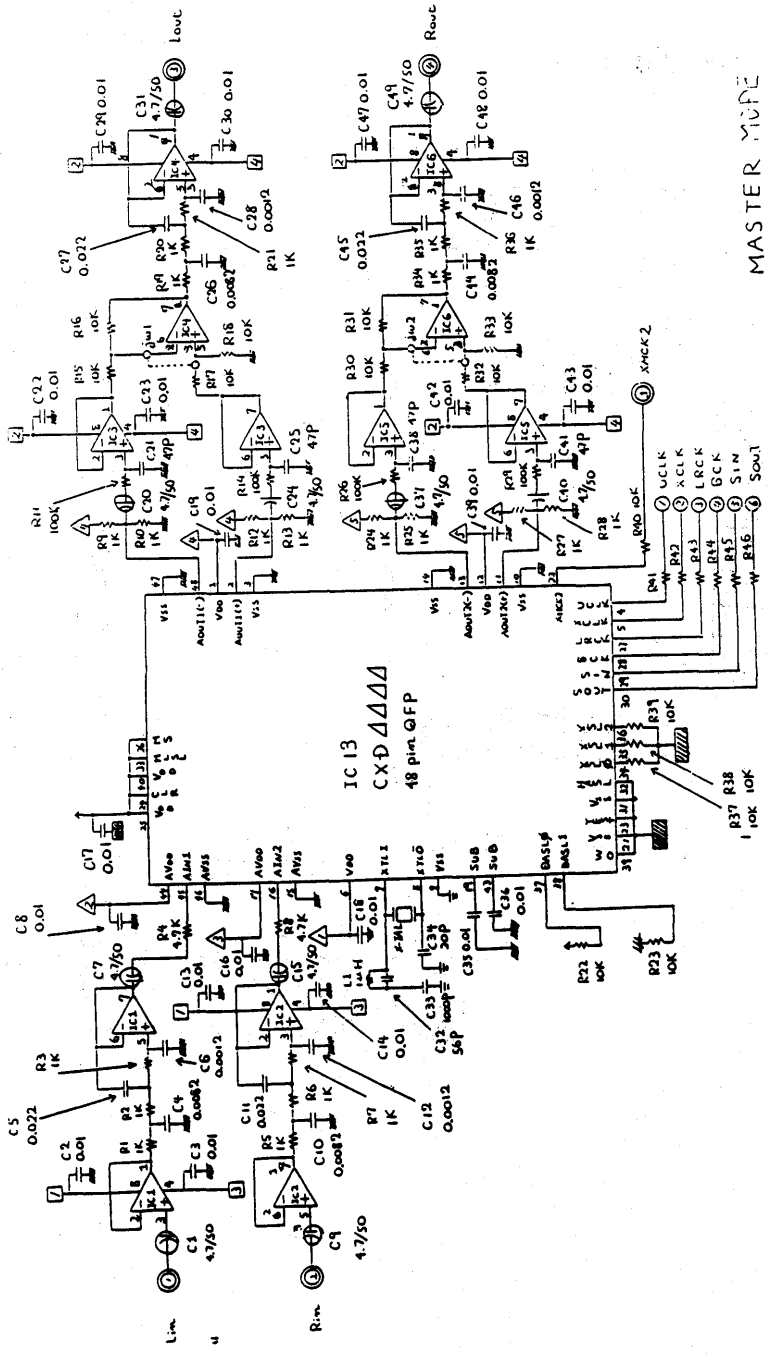
48pin QFP (Plastic) 0.7g

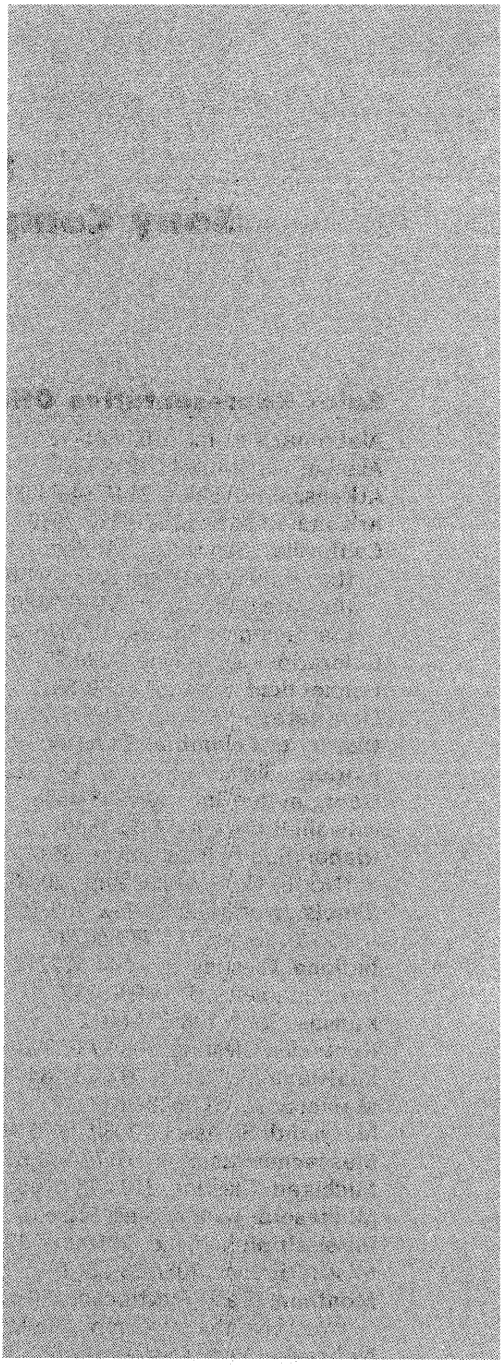


SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	———

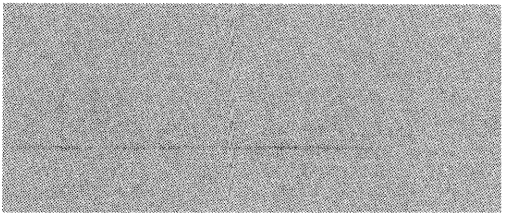
8

Test System


IC 13
CXD4444
48 pin QFP
MASTER MODE
Test Circuit
Lout
Rout
XMCK2
UCLK
XCLK
LRCK
BCK
SIN
SOUT
R41~R46 : 10K
100



Sales Offices



(800)288-Sony
Sony Component Products Company
Sales Offices

Sales Representative Offices:

Alabama: Rep, Inc., 205/881-9270
Alaska: Sony, 408/432-0190
Arkansas: B-P Sales, 214/234-8438
Arizona: Reptronix, 602/230-2630
California: (San Diego) Addem, 619/729-9216
(Los Angeles) H-Tech Sales, 714/753-7810
(Bay Area) Brooks, 415/960-3880
(Sacramento) Brooks, 916/676-2025
Colorado: Electrodyne, 303/695-8903
Connecticut: Sony, 617/630-8812
Delaware: S-J Assoc., 703/533-2233
District of Columbia: S-J Assoc., 703/533-2233
Florida: Sigma Tech, 813/789-5522
Georgia: Rep, Inc., 404/938-4358
Hawaii: Brooks, 415/960-3880
Idaho: (South) Electrodyne, 801/264-8050
(North) Northwest Comp., 206/828-2104
Illinois: (North) Micro-Tex, 708/765-3000
(South) Sony, 708/773-6072
Indiana: Giesting, 317/844-5222
Iowa: J.R. Sales, 319/393-2232
Kansas: Sony, 708/773-6072
Kentucky: Giesting, 606/873-2330
Louisiana: B-P Sales, 214/234-8438
Maine: Sony, 617/630-8812
Maryland: S-J Assoc., 703/533-2233
Massachusetts: Sony, 617/630-8812
Michigan: Giesting, 313/478-8106
Minnesota: Vector Sales, 612/631-1334
Mississippi: Rep, Inc., 205/881-9270
Missouri: Sony, 708/773-6072
Montana: (East) Electrodyne, 801/264-8050
(West) Northwest Comp., 206/828-2104
Nebraska: Vector Sales, 612/631-1334
Nevada: (North) Brooks, 415/960-3880
(South) Reptronix, 602/345-4580
New Hampshire: Sony, 617/630-8812
New Jersey: (North) S-J Assoc., 516/536-4242
(South) S-J Mid-Atlantic, 609/866-1234
New Mexico: Reptronix, 505/292-1718
New York: (Metro) S-J Assoc., 516/536-4242
(Upstate) S-J Assoc., 716/394-3281
North Carolina: Rep, Inc., 919/469-9997
North Dakota: Vector Sales, 612/631-1334
Ohio: (Cleveland) Giesting, 216/261-9705
(Cincinnati) Giesting, 513/385-1105
Oklahoma: B-P Sales, 214/234-8438
Oregon: Solsten Microelectronics, 503/620-3285
Pennsylvania: (East) S.J. Assoc., 609/866-1234
(West) Giesting, 412/828-3553
Puerto Rico: Sony, 919/380-0786
Rhode Island: Sony, 617/630-8812
South Carolina: Rep, Inc., 704/563-5554
South Dakota: Vector Sales, 612/631-1334
Texas: (Austin) B-P Sales, 512/346-9186
(Dallas) B-P Sales, 214/234-8438
(Houston)B-P Sales, 713/782-4144
(El Paso County) Reptronix, 505/292-1718
Tennessee: Rep, Inc., 615/475-4105
Utah: Electrodyne, 801/264-8050
Vermont: Sony, 617/630-8812
Virginia: S-J Assoc., 703/533-2233
Washington: Northwest Comp., 206/828-2104
West Virginia: Giesting, 513/385-1105
Wisconsin: (West) Vector Sales, 612/631-1334
(East) Micro-Tex, 414/542-5352
Wyoming: Electrodyne, 801/695-8903

Distributor Offices:

Alabama:	
Huntsville	Marshall, 205/881-9235
Arizona:	
Phoenix	Marshall, 602/496-0290
California:	
Los Angeles	Milgray, 805/484-4055
El Monte	Marshall, 818/307-6000
Ft. Valley	Bell Micro, 714/963-0667
Saratoga	Western Micro, 408/725-1660
Irvine	Marshall, 714/458-5395
Irvine	Milgray, 714/753-1282
Los Angeles	Marshall, 818/878-7000
Los Angeles	Western Micro, 818/707-0377
Orange	Western Micro, 714/637-0200
Sacramento	Marshall, 916/635-9700
San Diego	Aegis, 619/729-2026
San Diego	Marshall, 619/627-4184
San Diego	Western Micro, 619/453-9670
San Jose	Merit, 408/434-0800
San Jose	Bell Micro, 408/451-9400
San Francisco	Marshall, 408/942-4600
Westlake Vill.	Bell Micro, 805/496-2606
Colorado:	
Denver	Marshall, 303/451-8444
Connecticut:	
Danbury	Phase I, 203/791-9042
Milford	Milgray, 203/878-5538
Wallingford	Marshall, 203/265-3822
Florida:	
Deerfield	Vantage, 305/429-1001
Ft. Lauderdale	Marshall, 305/977-4880
Orlando	Marshall, 407/767-8585
Tampa	Marshall, 813/576-1399
Lake Mary	Milgray, 407/321-2555
Georgia:	
Atlanta	Marshall, 404/923-5750
Norcross	Milgray, 404/446-9777
Illinois:	
Chicago	Milgray, 708/202-1900
Chicago	Marshall, 708/490-0155
Indiana:	
Indianapolis	Marshall, 317/297-0483
Kansas:	
Kansas City	Marshall, 913/492-3121
Overland Park	Milgray, 913/236-8800
Maryland:	
Columbia	Milgray, 301/621-8169
Columbia	Vantage, 301/720-5100
Silver Springs	Marshall, 301/622-1118
Massachusetts:	
Billerica	Vantage, 508/667-2400
Boston	Marshall, 508/658-0810
Massachusetts (Con't):	
Burlington	Western Micro, 617/273-2800
Wilmington	Bell Micro, 508/658-0222
Wilmington	Milgray, 508/657-5900
Michigan:	
Livonia	Marshall, 313/525-5850
Minnesota:	
Minneapolis	Marshall, 612/559-2211
Missouri:	
St. Louis	Marshall, 314/291-4650
New Jersey:	
Clifton	Vantage, 201/777-4100
Fairfield	Marshall, 201/882-0320
Elmwood Park	Phase 1, 201/791-2990
Mt. Laurel	Marshall, 609/234-9100
Marlton	Milgray, 609/983-5010
Marlton	Western Micro, 609/596-7775
Parsippany	Milgray, 201/335-1766
New York:	
Binghamton	Marshall, 607/798-1611
Farmingdale	Milgray, 516/420-9800
Long Island	Marshall, 516/273-2424
Deer Park	Phase I, 516/254-2600
Rochester	Marshall, 716/235-7620
Pittsford	Milgray, 716/834-9405
Smithtown	Vantage, 516/543-2000
North Carolina:	
Raleigh	Marshall, 919/878-9882
Raleigh	Milgray, 919/790-8094
Ohio:	
Cleveland	Marshall, 216/248-1788
Cleveland	Milgray, 216/447-1520
Columbus	Marshall, 614/891-7580
Dayton	Marshall, 513/898-4480
Oregon:	
Beaverton	Western Micro, 503/629-2082
Portland	Marshall, 503/644-5050
Pennsylvania:	
Pittsburgh	Marshall, 412/788-0441
Texas:	
Austin	Marshall, 512/837-1991
Dallas	Marshall, 214/233-5200
Dallas	Milgray, 214/248-1603
Houston	Marshall, 713/895-9200
Houston	Milgray, 713/240-5360
Utah:	
Salt Lake City	Marshall, 801/973-2288
Salt Lake City	Milgray, 801/261-2999
Washington:	
Redmond	Western Micro, 206/881-6737
Seattle	Marshall, 206/486-5747
Wisconsin:	
Milwaukee	Marshall, 414/797-8400

SONY

Sony Corporation of America
Component Products Division
Semiconductor Division
10833 Valley View Street, Cypress, California 90630