SONY CXD2500AQ/AQZ

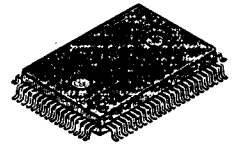
CD Digital Signal Processor

Description

The CXD2500AQ/AQZ is a digital signal processing LSI designed for use in compact disc players. It has the following functions:

- A wide frame jitter margin (±28 frames) realized by a built-in 32K RAM.
- Generation by the use of a digital PLL of bit clock pulses for strobing the EFM signal with a capture range of ±150kHz or more.
- EFM data demodulation
- Enhanced protection of EFM Frame Sync signals
- Powerful error correction based on a refined super strategy
  Error correction C1 : Double correction C2: Quadruple correction
- Double-speed play back and vari-pitch play back
- Reduced noise generation at track jumping
- Auto zero-cross muting
- Subcode demodulation and subcode Q data error detection
- Digital spindle servo system (incorporating an oversampling filter)
- 16-bit traverse counter
- Built-in asymmetry correction circuit
- CPU interface using a serial bus

80pin QFP (Plastic)



- Servo auto sequencer
- Output for digital audio interface
- Digital level meter and peak meter
- Bilinguality

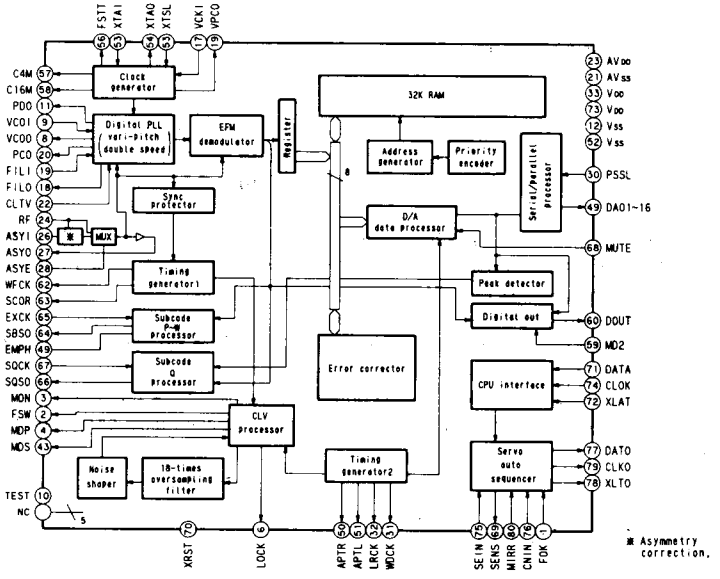
Features

- All digital signals for regeneration are processed using one chip.
- The built-in RAM enables high-integration mounting.

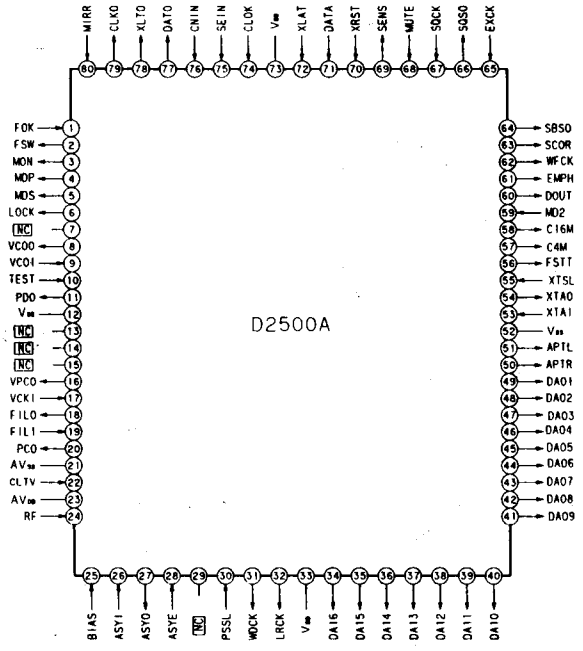
Structure

Silicon-gate CMOS IC

Block Diagram



Pin Configuration



Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_I	−0.3 to +7.0	V
• Output voltage	V_O	−0.3 to +7.0	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−40 to +125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75*1 to 5.25*3 (5.0V typ.)	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Input voltage	V_{IN}	V_{SS}−0.3V to V_{DD}+0.3	V
• Supply voltage differences	$V_{SS}-AV_{SS}$	−0.1 to +0.1	V
	$V_{DD}-AV_{DD}$	−0.1 to +0.1	V

* 1 The minimum V_{DD} value of 4.75V is for the double-speed play back mode with vari-pitch control reset. It is 3.6V in the low power consumption, special regeneration mode. * 2 In normal-speed play back mode the minimum V_{DD} value is 4.5V

* 2 Low power comsumption, special play back mode
This is a normal-speed play back mode entered when the LSI is set for double-speed internal operation whereas the crystal oscillation frequency is halved.

* 3 The maximum V_{DD} value of 5.25V is for the double-speed play back mode with vari-pitch control reset. For normal-speed play back and low power consumption special play back mode, the maximum V_{DD} value is 5.5V.

I/O Capacity

• Input pins	CI	12pF max.
• Output pins	CO	12pF max. at high impedance

Note: Test Conditions
$V_{DD}=V_I=0V$
$f_M=1MHz$

Pin Description

Pin No.	Symbol	I/O		Description
1	FOK	I		Focus OK input pin. Used for SENS output and servo auto sequencer.
2	FSW	O	Z.0	Output used to switch the spindle motor output filter.
3	MON	O	1.0	Output for spindle motor ON/OFF control
4	MDP	O	1,Z,0	Output for spindle motor servo control
5	MDS	O	1,Z,0	Output for spindle motor servo control
6	LOCK	O	1,0	The output of this pin is "H" when the GFS signal sampled at 460Hz is "H". It turns "L" when the GFS signal turns out "L" 8 or more times in succession.
7	NC	———		
8	VCOO	O	1,0	Output of oscillation circuit for analog EFM PLL
9	VCOI	I		Input to oscillation circuit for analog EFM PLL. f_{LOCK}=8.6436MHz
10	TEST	I		Test pin. Normally at 0V (GND).
11	PDO	O	1,Z,0	Output of charge pump for analog EFM PLL
12	V_{SS}			GND
13	NC	———		
14	NC	———		
15	NC	———		
16	VPCO	O	1,Z,0	Output of charge pump for vari-pitch PLL
17	VCKI	I		Clock input from external VCO for vari-pitch control. fc_{center}=16.9344MHz
18	FILO	O	Analog	Output of filter for master PLL (Slave=Digital PLL)
19	FILI	I		Input to filter for master PLL
20	PCO	O	1,Z,0	Output of charge pump for master PLL
21	AV_{SS}			Analog GND
22	CLTV	I		VCO control voltage input for master PLL
23	AV_{DD}			Analog power supply (+5V)
24	RF	I		EFM signal input
25	BIAS	I		Asymmetry circuit constant current input
26	ASYI	I		Asymmetry comparator circuit voltage input
27	ASYO	O	1,0	EFM full-swing output
28	ASYE	I		At "L" asymmetry circuit OFF. At "H" asymmetry circuit ON
29	NC	———		
30	PSSL	I		Input used to switch the audio data output mode. "L" for serial output, "H" for parallel output.
31	WDCK	O	1,0	D/A interface for 48-bit slot. Word clock f=2Fs
32	LRCK	O	1,0	D/A interface for 48-bit slot. LR clock f=Fs
33	V_{DD}			Power supply (+5V)
34	DA16	O	1,0	Outputs DA16(MSB) when PSSL=1 or serial data from 48-bit slot (2's complements, MSB first) when PSSL=0.
35	DA15	O	1,0	Outputs DA15 when PSSL=1 or bit clock from 48-bit slot when PSSL=0.

Pin No.	Symbol	I/O		Description
36	DA14	O	1,0	Outputs DA14 when PSSL=1 or serial data from 64-bit slot (2's complements, LSB first) when PSSL=0.
37	DA13	O	1,0	Outputs DA13 when PSSL=1 or bit clock from 64-bit slot when PSSL=0.
38	DA12	O	1,0	Outputs DA12 when PSSL=1 or LR clock from 64-bit slot when PSSL=0.
39	DA11	O	1,0	Outputs DA11 when PSSL=1 or GTOP when PSSL=0.
40	DA10	O	1,0	Outputs DA10 when PSSL=1 or XUGF when PSSL=0.
41	DA09	O	1,0	Outputs DA9 when PSSL=1 or XPLCK when PSSL=0.
42	DA08	O	1,0	Outputs DA8 when PSSL=1 or GFS when PSSL=0.
43	DA07	O	1,0	Outputs DA7 when PSSL=1 or RFCK when PSSL=0.
44	DA06	O	1,0	Outputs DA6 when PSSL=1 or C2PO when PSSL=0.
45	DA05	O	1,0	Outputs DA5 when PSSL=1 or XRAOF when PSSL=0.
46	DA04	O	1,0	Outputs DA4 when PSSL=1 or MNT3 when PSSL=0.
47	DA03	O	1,0	Outputs DA3 when PSSL=1 or MNT2 when PSSL=0.
48	DA02	O	1,0	Outputs DA2 when PSSL=1 or MNT1 when PSSL=0.
49	DA01	O	1,0	Outputs DA1 when PSSL=1 or MNT0 when PSSL=0.
50	APTR	O	1,0	Control output for aperture correction. "H" for R-ch.
51	APTL	O	1,0	Control output for aperture correction. "H" for L-ch.
52	V_{SS}			GND
53	XTAI	I		Input to 16.9344MHz Xtal oscillation circuit or 33.8688MHz input
54	XTAO	O	1,0	Output of 16.9344MHz Xtal oscillation circuit
55	XTSL	I		Xtal selection input pin. "L" for 16.9344MHz Xtal, "H" for 33.8688MHz Xtal.
56	FSTT	O	1,0	2/3 divided output of Pins 53 or 54. Unaffected by vari-pitch control.
57	C4M	O	1,0	4.2336MHz output. Subject to vari-pitch control.
58	C16M	O	1,0	16.9344MHz output. Subject to vari-pitch control.
59	MD2	I		Digital-Out ON/OFF control. "H" for ON, "L" for OFF.
60	DOUT	O	1,0	Digital-Out output pin
61	EMPH	O	1,0	Stays "H" for regeneration disc provided with emphasis or "L" for that without emphasis.
62	WFCK	O	1,0	WFCK(Write Frame Clock) output
63	SCOR	O	1,0	Turns "H" when subcode Sync S0 or S1 is detected.
64	SBSO	O	1,0	Serial output of Sub P to W
65	EXCK	I		Clock input for reading SBSO
66	SQSO	O	1,0	Outputs 80-bit Sub Q and 16-bit PCM peak-level data.
67	SQCK	I		Clock input for reading SQSO
68	MUTE	I		"H" for muting, "L" for release.
69	SENS	—	1,Z,0	SENS output to CPU
70	XRST	I		System reset. "L" for resetting.
71	DATA	I		Inputs serial data from CPU.
72	XLAT	I		Latches serial data input from CPU at falling edge.

Pin No.	Symbol	I/O		Description
73	V_{DD}			Power supply (+5V)
74	CLOK	I		Inputs serial data transfer clock from CPU.
75	SEIN	I		Inputs SENSE from SSP.
76	CNIN	I		Inputs track jump count signal.
77	DATO	O	1,0	Outputs serial data to SSP.
78	XLTO	O	1,0	Latches serial data output to SSP at falling edge.
79	CLKO	O	1,0	Outputs serial data transfer clock to SSP.
80	MIRR	I		Inputs mirror signal to be used by auto sequencer when jumping 128 or more tracks.

Notes:
- The data at the 64-bit slot is output in 2's complements on an LSB-first basis. The data at the 48-bit slot is output in 2's complements on an MSB-first basis.
- GTOP monitors the state of Frame Sync protection. ("H": Sync protection window released)
- XUFG is a negative Frame Sync pulse obtained from the EFM signal before Frame Sync protection is effected.
- XPLCK is an inversion of the EFM PLL clock. The PLL is designed so that the falling edge of XPLCK coincides with a change point of the EFM signal.
- The GFS signal turns "H" upon coincidence between Frame Sync and the timing of interpolation protection.
- RFCK is a signal generated at 136-μs periods using a crystal oscillator.
- C2PO is a signal to indicate a data error.
- XRAOF is a signal issued when a jitter margin of $\pm$28F is exceeded by the 32K RAM.

Electrical Characteristics

DC characteristics (V_{DD}=AV_{DD}=5.0V±5%, V_{SS}=A V_{SS}=0V, T_{opr}=−20 to +75°C)

Item			Condition	Min.	Typ.	Max.	Unit	Related pins
Input voltage (1)	Input voltage "H" level	V_{IH}(1)		0.7V_{DD}			V	* 1
	Input voltage "L" level	V_{IL}(1)				0.3V_{DD}	V	
Input voltage (2)	Input voltage "H" level	V_{IN}(2)		0.8V_{DD}			V	* 2
	Input voltage "L" level	V_{IN}(2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN}(3)	Analog input	V_{DD}		V_{SS}	V	* 3
Output voltage (1)	Output voltage "H" level	V_{OH}(1)	I_{OH}=−1mA	V_{DD}−0.5		V_{DD}	V	* 4
	Output voltage "L" level	V_{OL}(1)	I_{OL}=1mA	0		0.4	V	
Output voltage (2)	Output voltage "H" level	V_{OH}(2)	I_{OH}=−1mA	V_{DD}−0.5		V_{DD}	V	* 5
	Output voltage "L" level	V_{OL}(2)	I_{OL}=2mA	0		0.4	V	
Output voltage (3)	Output voltage "L" level	V_{OL}(3)	I_{OL}=2mA	0		0.4	V	* 6
Output voltage (4)	Output voltage "H" level	V_{OH}(4)	I_{OH}=−1mA	V_{DD}−0.5		V_{DD}	V	* 7
	Output voltage "L" level	V_{OL}(4)	I_{OL}=2mA	0		0.4	V	
Input leak current		I_{LI}	VI=0 to 5.25V			±5	μA	* 1, * 2, * 3
Tristate pin output leak current		I_{LO}	V_O=0 to 5.25V			±5	μA	* 8

Related pins

* 1 XTSL, DATA, XLAT, MD2, PSSL
* 2 CLOK, XRST, EXCK, SQCK, MUTE, FOK, SEIN, CNIN, MIRR, VCKI, ASYE
* 3 CLTV, FILI
* 4 MDP, PDO, PCO, VPCO
* 5 ASYO, DOUT, FSTT, C4M, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO,CLKO, XLTO, SENS, MDS, DA01 to DA16, APTR, APTL, LRCK, WFCK
* 6 FSW
* 7 FILO
* 8 SENS, MDS, MDP, FSW, PDO, PCO, VPCO

2. AC Characteristics

① XTAI and VCOI pins

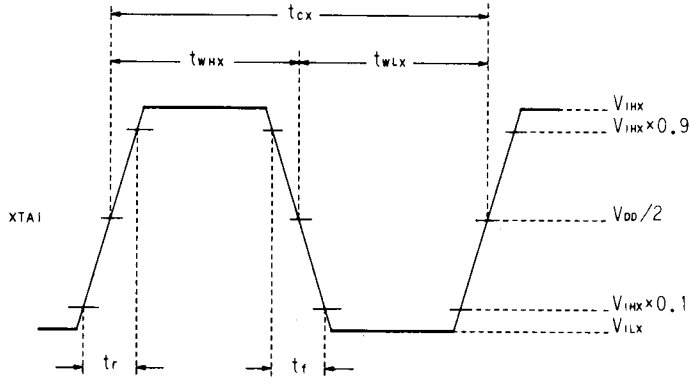
(1)During self-oscillation (T_{opr} = −20 to +75°C, V_{DD} = AV_{DD} = 5.0V±5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7MHz		18	MHz

(2)With pulses input to XTAL and VCOI pins

(T_{opr} = −20 to +75°C, V_{DD} = AV_{DD} = 5.0V±5%)

Item	Symbol	Min.	Typ.	Max.	Unit
"H" level pulse width	t_{WHX}	13		500	ns
"L" level pulse width	t_{WLX}	13		500	ns
Pulse period	t_{CX}	26		1,000	ns
Input "H" level	V_{IHX}	V_{DD}−1.0			V
Input "L" level	V_{ILX}			0.8	V
Rising time Falling time	t_R, t_F			10	ns



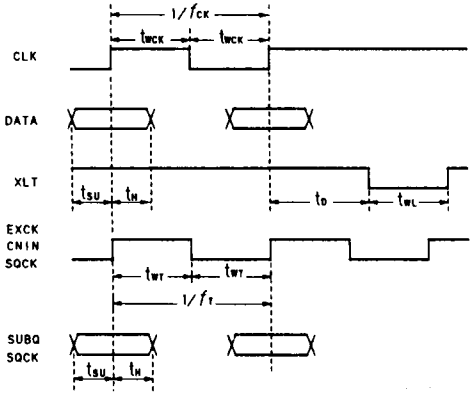
(3)With sine waves input to XTAI and VCOI pins via capacitor

(T_{opr} = −20 to +75°C, V_{DD} = AV_{DD} = 5.0V±5%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD}+0.3	Vp-p

② CLOK, DATA, XLAT, CNIN, SQCK, and EXCK pins
(V_{DD}=AV_{DD}=5.0V±5%, V_{SS}=AV_{SS}=0V, T_{opr}=−20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK, CNIN, SQCK frequency	f_T			1	MHz
EXCK, CNIN, SQCK pulse width	t_{WT}	300			ns

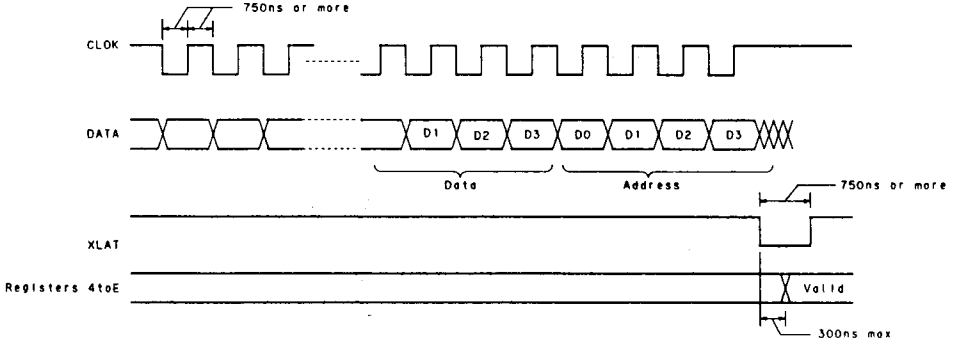


Description of Functions

§ 1 CPU Interface and Commands

○ CPU interface

This interface is used to set various modes using DATA, CLK, and XLAT.
The interface timing chart is shown below.



○ The command addresses of the CXD2500 and the data that can be set there are shown in Table 1-1.

○ When XRST is set to 0, the CXD2500 is reset, causing its internal registers to be initialized to the values listed in Table 1-2.

CXD2500A Commands

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind(A,E), Overflow(C)	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	—	—	—	—	—	—	—	—	—	—	—	—
	Brake (B)					0.36ms	0.18ms	0.09ms	0.045ms												
6	KICK(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer track jump (N) setting	0	1	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CDROM	0	D OUT Mute-F	WSEL	—	—	—	—	—	—	—	—	—	—	—	—
9	Func specification	1	0	0	1	D CLV ON-OFF	DSPB ON-OFF	A SEQ ON-OFF	D PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	Vari UP	Vari Down	Mute	ATT	PCT1	PCT2	—	—	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
C	Servo factor setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CRTL	1	1	0	1	DCLV PWMMD	TB	TP	CLVS Gain	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-1

CXD2500A Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind(A,E), Overflow(C) Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	KICK(D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer track jump (N) setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
9	Func specification	1	0	0	1	1	0	0	1	0	0	0	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	—	—	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Servo factor setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CRTL	1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-2

§ 1-2 Meanings of Data Set at Command Addresses

$4X Command

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2NTRACK JUMP	1	1	0	RXF
N TRACK MOVE	1	1	1	RXF

RXF=0 FORWARD
RXF=1 REVERSE

- If a Focus-ON command ($47) being executed is canceled, $02 is issued and the auto sequence operation is discontinued.
- If a Track Jump or Track Move command ($48 to $4F) being executed is canceled, the auto sequence operation is discontinued.

$5X Command

Used to set timers for the auto sequencer.
Timers set: A, E, C, and B

Command	D3	D2	D1	D0
Blind(A,E), Over flow(C)	0.18ms	0.09ms	0.045ms	0.022ms
Brake(B)	0.36ms	0.18ms	0.09ms	0.045ms

Example: D2=D0=1, D3=D1=0 (Initial Reset)
A=E=C=0.112ms
B=0.225ms

$6X Command

Used to set a timer for the auto sequencer.
Timer set: D

Command	D3	D2	D1	D0
KICK(D)	11.6ms	5.8ms	2.9ms	1.45ms

Example: D3=0 D2=D1=D0=1 (Initial Reset)
D=10.15ms

$7X Command

Used to set the number (N) of auto sequencer track jumps/moves.

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequencer track jump number setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set the value of "N" for execution of a 2N track jump or N track move.

- The maximum number of tracks that can be counted is 65,535. However, in the case of 2N track jumps, it is subject to the mechanical restrictions due to the optical system.
- When the number of tracks to be jumped is smaller than 16, the signals input from the CNIN pin are counted. When it is 16 or larger, the signals input from the MIRR pin are counted. This count signal selection contributes toward improving the accuracy of high-speed track jumping.

$8X Command

Command	D3	D2	D1	D0
MODE specification	CDROM	0	D. OUT Mute-F	WSEL

Command bit	C2PO timing	Processing
CDROM=1	1-3	CDROM mode is entered. In this mode, average value interpolation and preceding value holding are not performed.
CDROM=0	1-3	Audio mode is entered. In this mode, average value interpolation and preceding value holding are performed.

Command bit	Processing
D.out Mute F=1	When Digital Out is ON (pin MD2=1), DA output is muted.
D.out Mute F=0	DA output muting is unaffected by the setting of Digital Out.

D/A Out D.out Mute with F=1

	MD2=1 (D. out-ON)	MD2=0 (D. out-OFF)
Mute-ON	−∞dB	−∞dB
Mute-OFF	−∞dB	0dB

Command bit	Sync protection window width	Application
WSEL=1	±26 channel clock pulses *	Antirollingness is enhanced.
WSEL=0	±6 channel clock pulses	Sync window protection is enhanced.

* In normal-speed play back, the channel clock frequency is 4.3218MHz.

$9X Command

Command	Data 1				Data 2		
	D3	D2	D1	D0	D3	D2	D1
Func specification	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL Sub	FLFC

Command bit	CLV mode	Contents	
DCLV ON-OFF=0	In CLVS mode	FSW=L, MON=H, MDS=Z, MDP=servo control signal with carrier frequency of 230Hz at T_B =0 or 460Hz at T_B =1	
	In CLVP mode	FSW=Z, MON=H, MDS= speed control signal with carrier frequency of 7.35kHz, MDP=phase control signal with carrier frequency of 1.84kHz	
DCLV ON-OFF=1 (FSW and MON are unnecessary)	In CLVS or CLVP mode	DCLV When PWM, MD=1	MDS=PWM polarity signal, Carrier frequency=132kHz MDS=PWM absolute value output (binary), Carrier frequency=132kHz
		DCLV When PWM, MD=0	MDS=Z MDP=ternay PWM output Carrier frequecy=132kHz

In the Digital CLV servo mode with DCLV ON-OFF set to 1, the sampling frequency of the internal digital filter is switched at the same time as switching between CLVP and CLVS.
Therefore, for CLVS, the cut-off frequency fC is 70Hz with T_B set to 0 or 140Hz with T_B set to 1.

Command bit	Processing
DSPB=0	Normal-speed play back. ECC quadruple correction is made. Vari-pitch control is enabled.
DSPB=1	Double-speed play back. ECC double correction is made. Vari-pitch control is disabled.

However, during PLL lock in FLFC can be set to 0.

SENS Output

Microcomputer serial register values (Latching unnecessary)	ASEQ=0	ASEQ=1
$0X	Z	SEIN(FZC)
$1X	Z	SEIN(A.S)
$2X	Z	SEIN(T.Z.C)
$3X	Z	SEIN(SSTOP)
$4X	Z	XBUSY
$5X	Z	FOK
$6X	Z	SEIN(Z)
$AX	GFS	GFS
$BX	COMP	COMP
$CX	COUT	COUT
$EX	$\overline{OV64}$	$\overline{OV64}$
$7X, 8X, 9X, DX, FX	Z	0

Description of SENS signals

SENS output	Meaning
Z	SENS pin is at high-Z state.
SEIN	Output of the SEIN signal input from the SSP to the CXD2500
XBUSY	Turns "H" when auto sequencer operation is terminated.
FOK	Output of the signal (normally FOK input from RF) input to the FOK pin. Turns "H" when Focus OK is received.
GFS	Turns "H" when regenerated Frame Sync is obtained at the correct time.
COMP	Used in counting the number of tracks set in register B. This output turns "H" when the count is latched in register B then the count is latched in register B once more. It is reset to "L" level when the count of CNIN inputs reaches the value set in the first register B.
COUT	Used in counting the number of tracks set in register B. This output turns "H" when the count is latched in register B then the count is latched in register C. It is toggled every time the count of CNIN inputs reaches the value set in register B.
$\overline{OV64}$	Turns "L" when the channel clock pulse count has exceeded 64 after passage of the EFM signal through the sync detection filter.

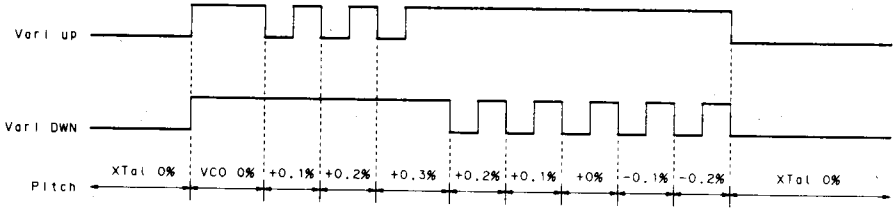
Command bit	Meaning
DPLL=0	RFPLL enters analog mode. PDO, VCOI, and VCOO are used.
DPLL=1	RFPLL enters digital mode. PDO becomes Z.

Command bit	BiliGL MAIN=0	BiliGL MAIN=1
BiliGL SUB=0	STEREO	MAIN
BiliGL SUB=1	SUB	Mute

Definition of Bilingual MAIN, SUB, and STEREO
MAIN: The input L-ch signal is output to both L-ch and R-ch.
SUB: The input R-ch signal is output to both L-ch and R-ch.
STEREO: The input L-ch signal is output to both L-ch and R-ch.

$AX Command

Command	Data 1				Data 2	
	D3	D2	D1	D0	D3	D2
Audio CTRL	Vari UP	Vari DWN	Mute	ATT	PCT1	PCT2



Command bit	Meaning
Mute=0	Muting is off unless condition to make muting occurs.
Mute=1	Muting is on. Peak register reset.

Command bit	Meaning
ATT=0	Attenuation is off.
ATT=1	−12dB

Condition for Muting CXD2500A

① Mute=1 in register A
② Pin Mute=1
③ D.OUT Mute F=1 in register 8 with D.Out ON (pin MD2=1)
④ Elapse of over 35ms after the turning low of GFS
⑤ BiliGL MAIN=Sub=1 in register 9
⑥ PCT1=1 and CPT2=2 in register A
In the case of ①~④, zero-cross muting not exceeding 1 ms is performed.

Command bit		Meaning	PCM Gain	ECC correction capacity
PCT1	PCT2			
0	0	Normal mode	×0dB	C1 : Double, C2 : Quadruple
0	1	Level meter mode	×0dB	C1 : Double, C2 : Quadruple
1	0	Peak meter mode	Mute	C1 : Double, C2 : Double
1	1	Normal mode	×0dB	C1 : Double, C2 : Double

Level Meter Mode (See timing chart 1-4.)

- This mode makes the digital level meter function available.
- Inputting 96 clock pulses to SQCK causes 96bits of data to be output to SQSO. Of the output data, the first 80bits comprise Sub-Q data communicating the data format to the Sub Code interface. The next 15 bits constitute PCM data (absolute value) ordered LSB-first. The last bit identifies the channel involved. That is, if the last bit is "H", the PCM data has been generated in L-ch. If it is "L", the data has been generated in R-ch.
- The PCM data is reset once it is read. At the same time, the L/R flag is reversed. While this state is kept until the next read operation is started, maximum value detection is continued ; the detected maximum value is subsequently output.

Peak Meter Mode (See timing chart 1-5.)

- In this mode, the maximum value of PCM data is detected whether the channel involved is L-ch or R-ch. To read the detected maximum value, it is necessary to input 96 clock pulses to SQCK.
- When 96 clock pulses have been input to SQCK, 96bits of data is output to SQSO. At the same time, the data is re-set in an internal register of the LSI.
  That is, the PCM peak detection register is not reset when it is read.
- To reset the PCM peak register, set both PCT1 and PCT2 to 0. Or, Set $AX mute.
- In this mode, the absolute time of Subcode Q is controlled automatically.
  Namely, every time a peak value is detected, the absolute time when the CRC was passed is stored. The program time operation is performed in the normal way.
- The last bit (L/R flag) of the 96-bit data stays 0.
- In this mode, the preceding value holding and average value interpolation data are fixed to level ($-\infty$).

$CX Command

Command	D3	D2	D1	D0	Explanation
Servo factor setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Only DCLV=1 is effective.
CLV CTRL ($DX)				Gain CLVS	DCLV=1 and DCLV=0 are both effective.

This command is used to externally set the spindle servo gain when DCLV=1.

- Gain setting for CLVS mode: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	−12dB
0	0	1	−6dB
0	1	0	−6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note: When DCLV=0, the CLVS gain is determined as follows:
If Gain CLVS=0, then GCLVS=−12dB.
If Gain CLVS=1, then GCLVS=0dB

- Gain setting for CLVP mode: GMDP, GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	−6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	−6dB
0	1	0dB
1	0	+6dB

$DX Command

Command	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	CLVS Gain

See "$CX Command."

Command bit	Explanation (See timing chart 1-6.)
DCLV PWM MD=1	Specification of PWM mode for digital CLV. Both MDS and MDP are used.
DCLV PWM MD=0	Specification of PWM mode for digital CLV. Ternary MDP values are output.

Command bit	Explanation
TB=0	In CLVS or CLVH mode, bottom value is held at periods of RFCK/32.
TB=1	In CLVS or CLVH mode, bottom value is held at periods of RFCK/16.
TP=0	In CLVS mode, peak value is held at periods of RFCK/4.
TP=1	In CLVS mode, peak value is held at periods of RFCK/2.

In CLVH mode, peak holding is made at 34kHz.

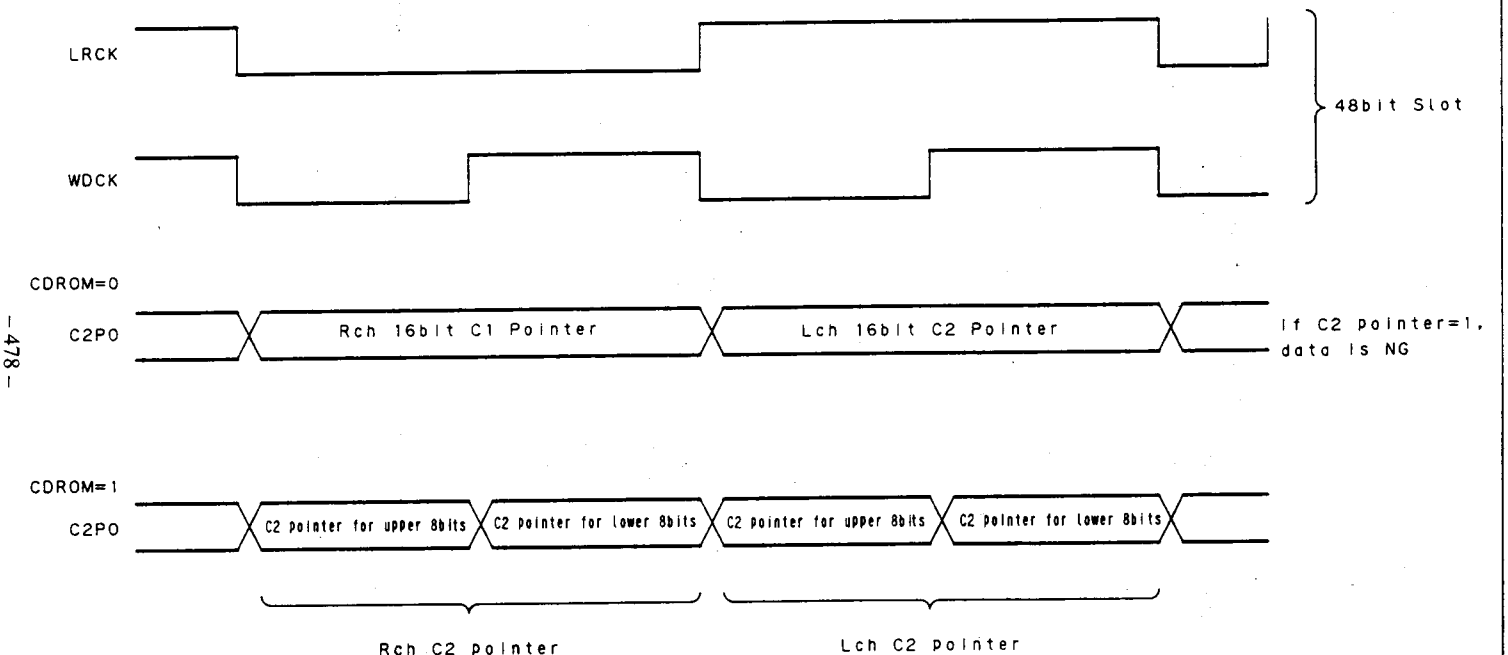
$EX Command

Command	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0

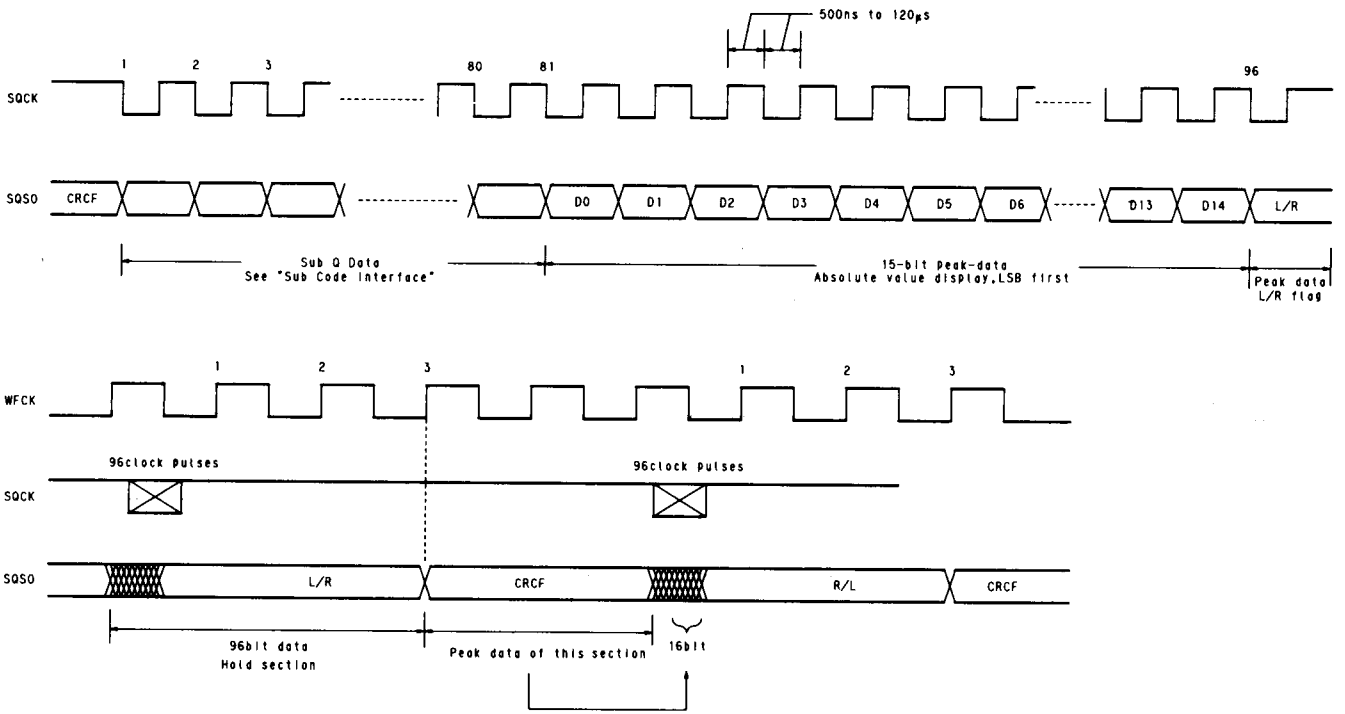
CM3	CM2	CM1	CM0	Mode	Explanation
0	0	0	0	STOP	See Timing Chart 1-7.
1	0	0	0	KICK	See Timing Chart 1-8.
1	0	1	0	BRAKE	See Timing Chart 1-9.
1	1	1	0	CLVS	
1	1	0	0	CLVH	
1	1	1	1	CLVP	
0	1	1	0	CLVA	

STOP : Spindle motor stop mode
KICK : Spindle motor forward run mode
BRAKE : Spindle motor reverse run mode
CLVS : Rough servo mode for use for drawing disc run into RF-PLL capture range when the RF-PLL circuit lock has been disengaged
CLVP : PLL servo mode
CLVA : CLVS and CLVP are automatically switched modes during normal player status.

Timing Chart 1-3

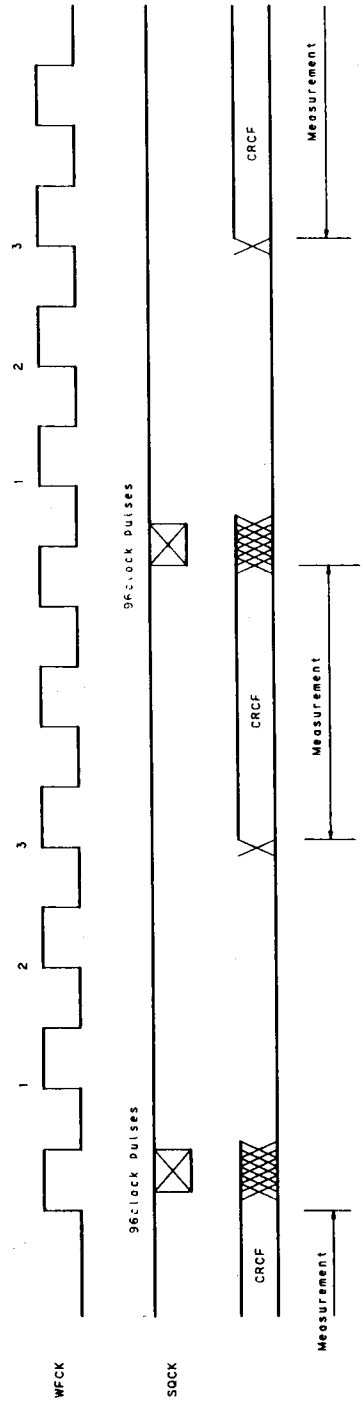


Timing Chart 1-4



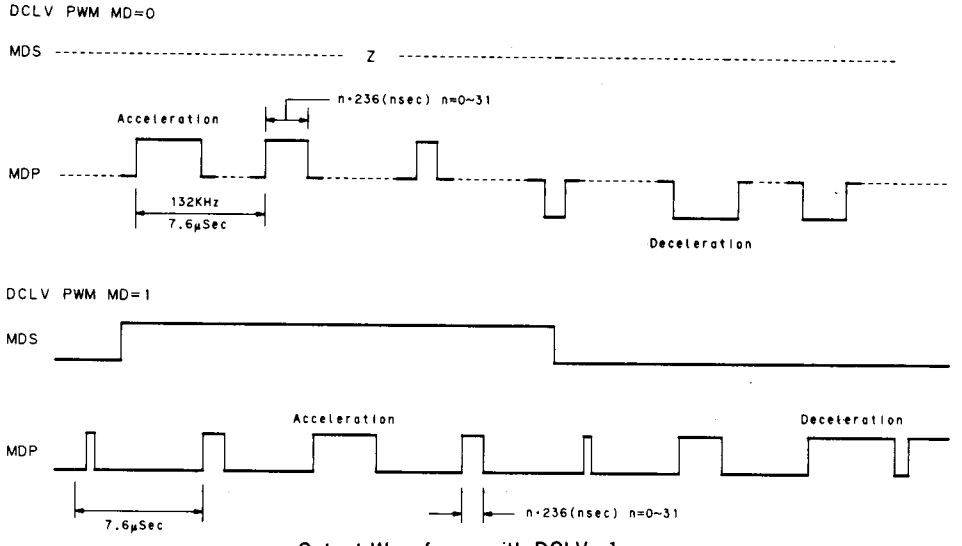
Level Meter Timing

Timing Chart 1-5



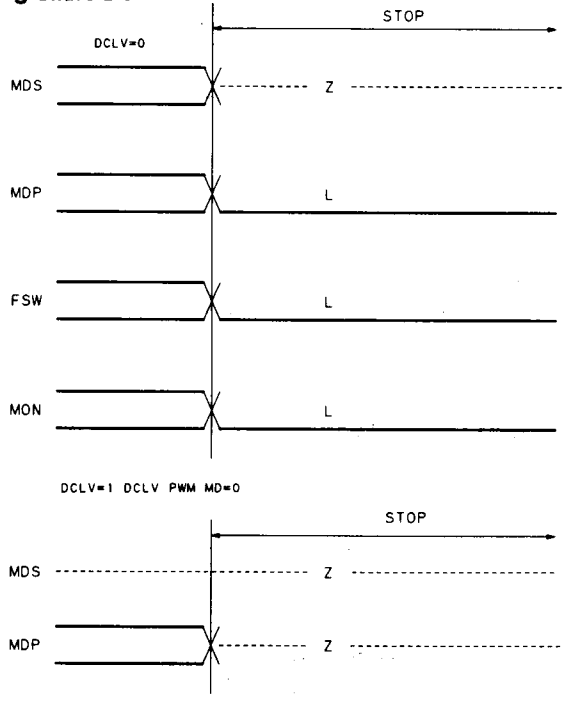
Peak Meter Timing

Timing Chart 1-6

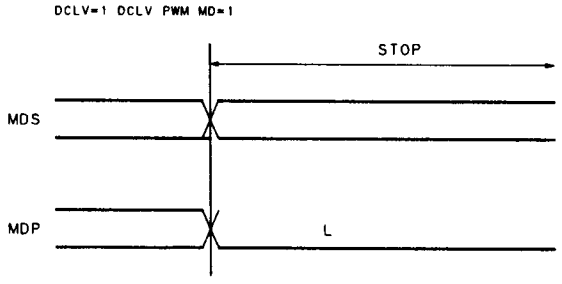


Output Waveforms with DCLV=1

Timing Chart 1-7

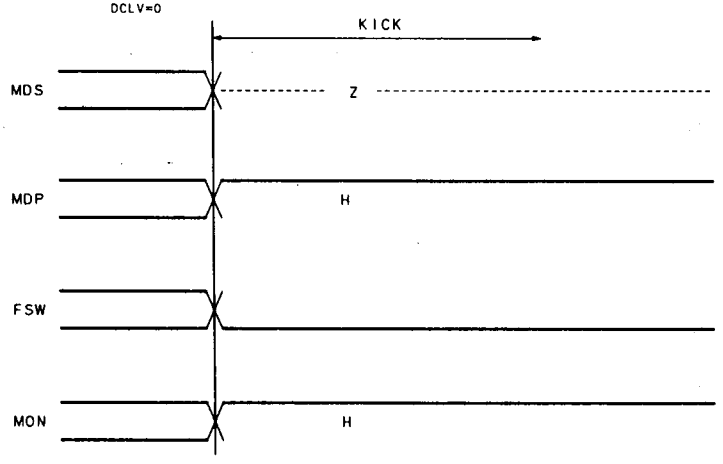


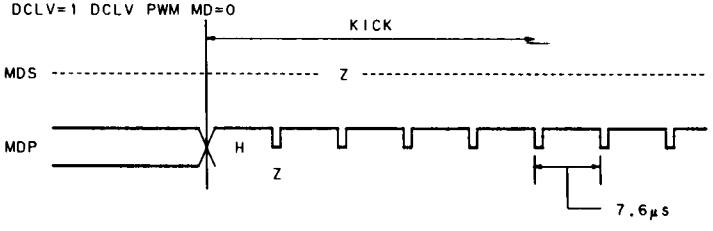
FSW and MON are the same as for DCLV=0



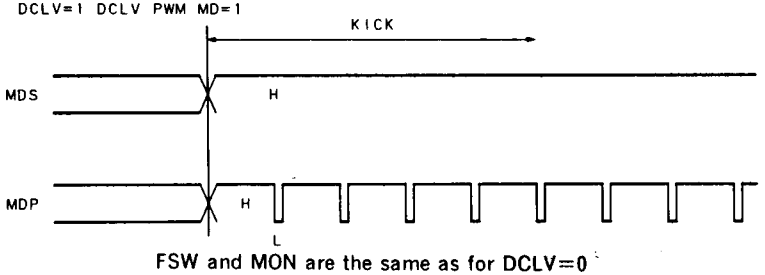
FSW and MON are the same as for DCLV=0

Timing Chart 1-8



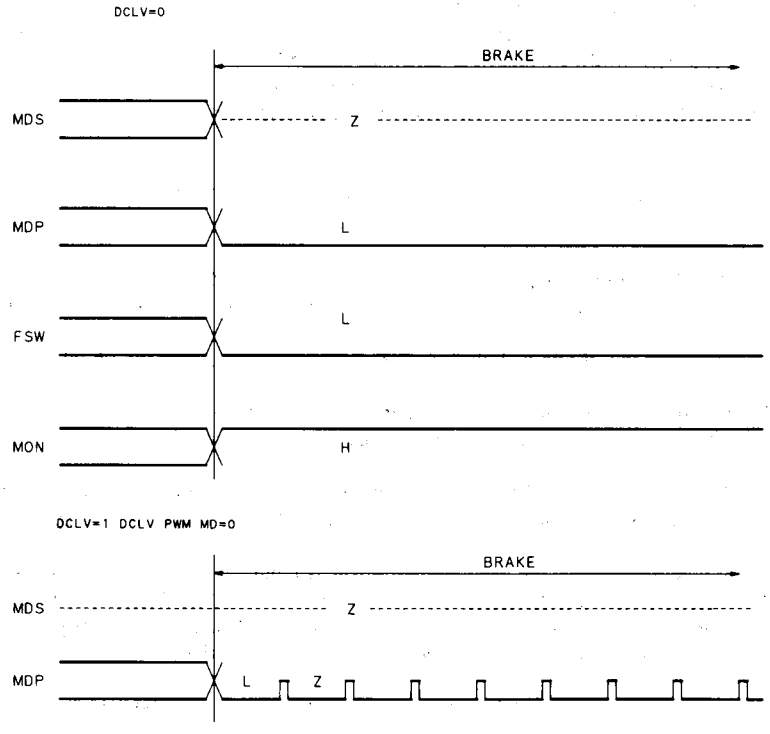


FSW and MON are the same as for DCLV=0

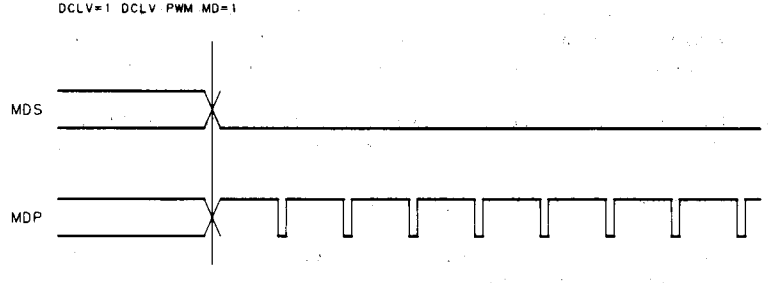


FSW and MON are the same as for DCLV=0

Timing Chart 1-9



FSW and MON are the same as for DCLV=0



FSW and MON are the same as for DCLV=0

§ 2 Subcode Interface

In this section, the subcode interface will be explained.

The contents of the subcode interface can be externally read in two ways. The subcodes P through W totaling 8bits can be read from SBSO by inputting EXCK to the CXD2500.

Sub Q can be read after conducting a CRC check on the 80bits of information in the subcode frame. First, check SCOR and CRCF, then input 80 clock pulses to SQCK and read the data.

§ 2-1 P-W Subcode Read

These subcodes can be read by entering EXCK immediately after the fall of WFCK. (See Figure 2-1).

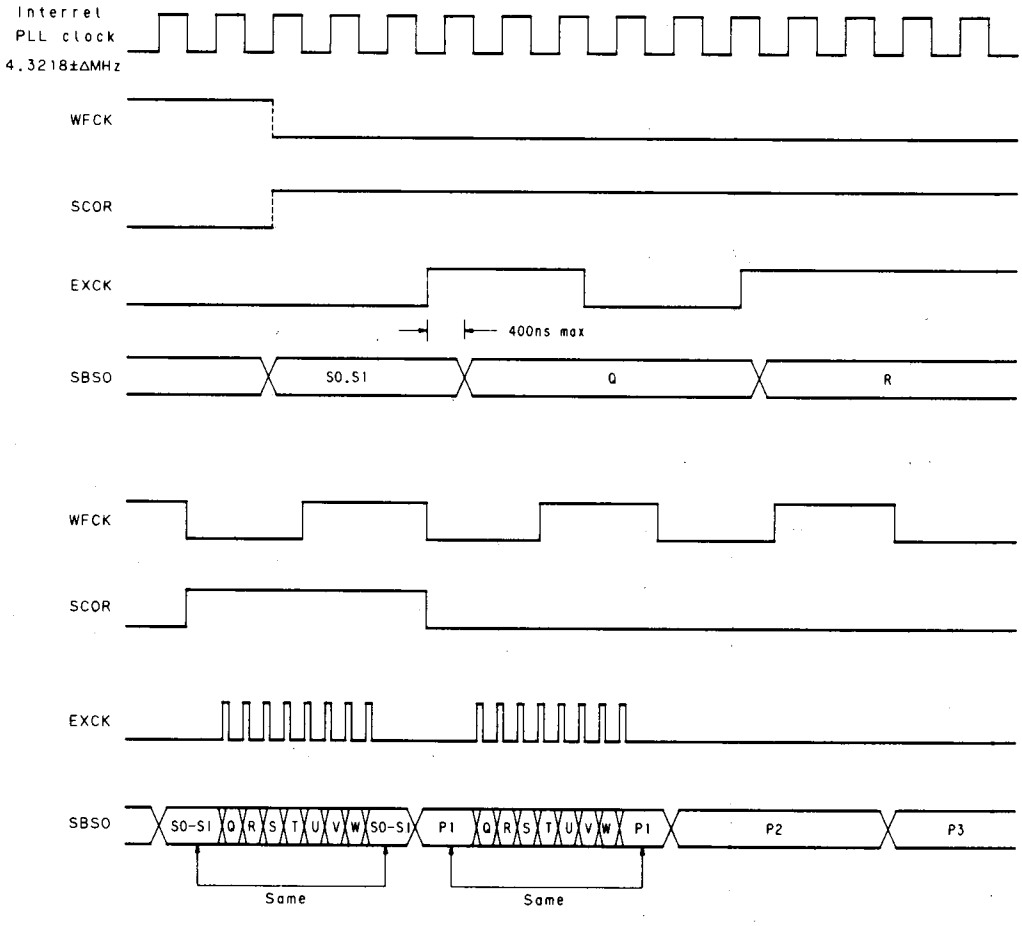
§ 2-2 80bit Sub Q Read

Figure 2-2 shows a block diagram of the peripheral part of the 80-bit Sub Q register.

- The Sub Q regenerated on a bit-per-frame basis is input to the 80-bit serial/parallel register and the CRC circuit.
- When the results of a CRC on the 96bits of Sub Q are OK, CRCF is set to 1 and the 96-bit data is output to SQSO.
  Furthermore, the 80-bit data is loaded into the 80-bit, parallel/serial register.
  If SQSO is found "H" after the output of SCOR, the CPU realizes that a new set of data has been loaded after passing a CRC.
- When 80-bit data is loaded CXD2500A, the bit arrangement is reversed within each byte of the data. Therefore, the bits are ordered LSB-first within each byte, even though the byte arrangement is kept unchanged.
- When 80bits of data are confirmed to have been loaded, SQCK is input to read the data. Subsequently in the CXD2500A, the input of SQCK is detected and the retriggerable Mono/Multi is reset during Low.
- The time constant of the retriggerable Mono/Multi ranges from 270 to 400 us. During SQCK High if it is less than this time constant, the Mono/Multi is kept being reset, preventing the contents of the P/S register from being loaded into the P/S register.
- While the Mono/Multi is kept reset, data loading into the peak detection parallel/serial register and 80-bit parallel/serial register is forbidden.
  Therefore, while data read operation is carried out at clock periods not exceeding the time constant for the Mono/Multi, the contents of these registers are retained without being rewritten, for example, when a CRC is passed.
- The CXD2500A permits the peak detection register to be connected to the shift-in of the 80-bit P/S register. The input and output terminals of Ring Control 1 are interconnected in the peak meter mode as well as level meter mode, while those of Ring Control 2 are interconnected only in the peak meter mode.
  The purpose of these Ring Control arrangements is to reset the registers every time their contents are read in the level meter mode, while preventing their contents from being destroyed by read operation during the peak meter mode.
  To enable this control, it is essential to input 96 clock pulses for read operation in the peak meter mode.
- As mentioned earlier, the detection of a peak value in the peak meter mode is followed by the storing of the next absolute time.
  A timing chart for these operations is shown in Figure 2-3.

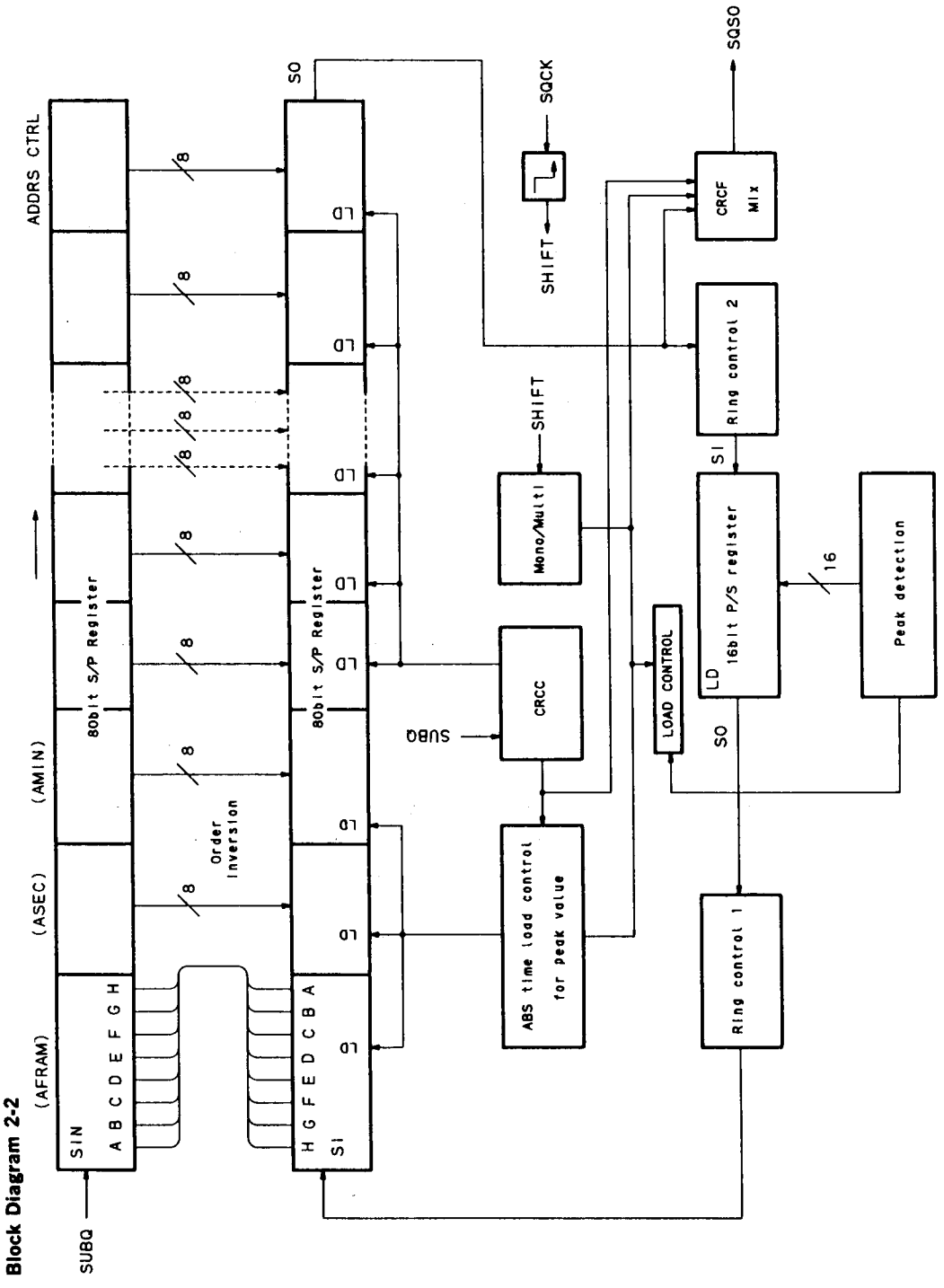
Note: The "H" as well as "L" duration of the clock pulses to be input to the SQCK pin to perform the above-described operations must be between 750ns and 120μs.

Timing Chart 2-1

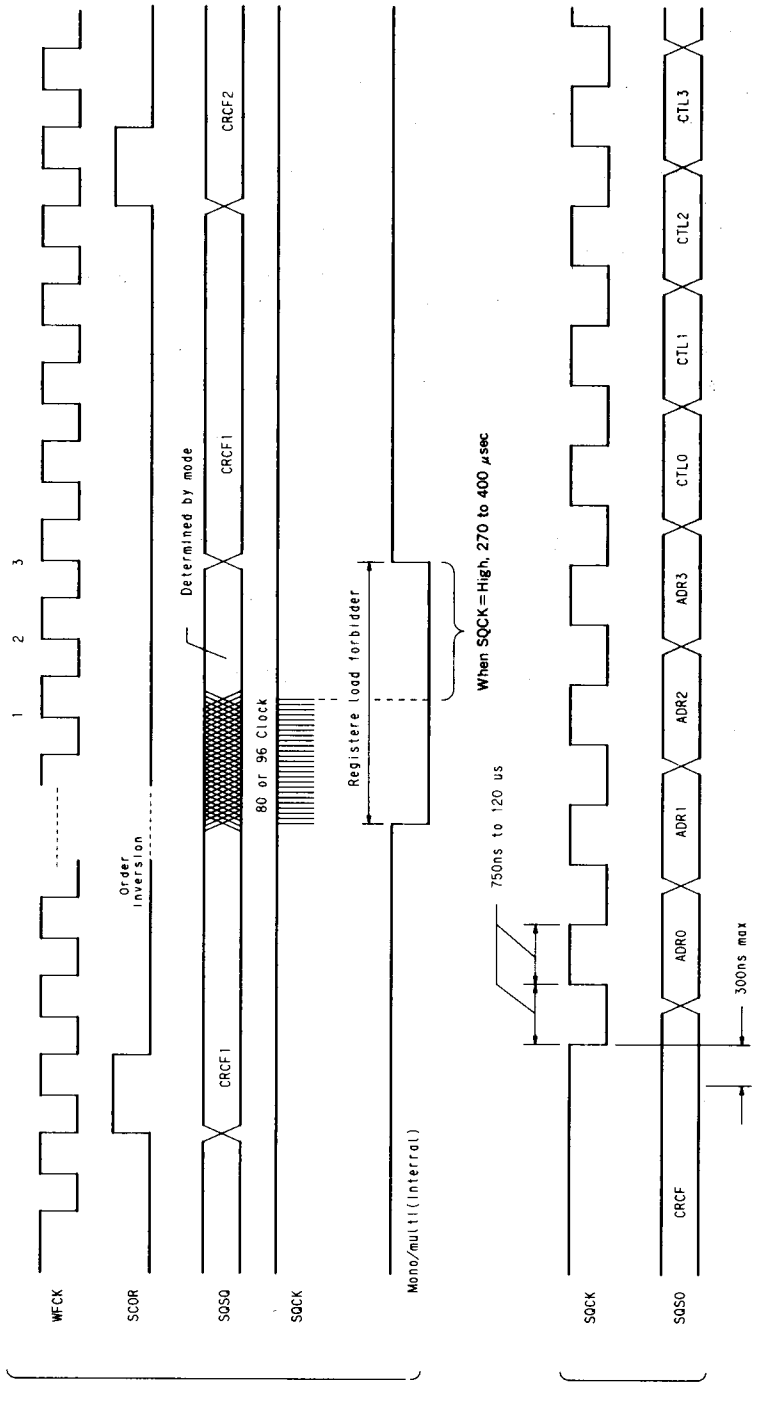


Subcode P. Q. R. S. T. U. V. W Read Timing

Block Diagram 2-2



Timing Chart 2-3



§ 3 Other Functions

§ 3-1 Channel Clock Regeneration Using Digital PLL Circuit

○ Demodulation of the EFM signal regenerated using an optical system requires the use of channel clock pulses.
The EFM signal to be demodulated has been modulated into an integer multiple of the channel clock period T, ranging from 3T to 11T.
To read the information conveyed by the EFM signal, it is essential to correctly recognize the value of the integer and, hence, to use channel clock pulses.
In a real CD player, the pulse width of the EFM signal fluctuates being affected by fluctuations of the disc rotation. For this reason, it is necessary to use a PLL in regenerating channel clock pulses.

Figure 3-1 shows a block diagram of the 3-stage PLL contained in the CXD2500A.

○ The 1st-stage PLL is used for vari-pitch regeneration. To use this PLL, it is necessary to prepare an LPF and a VCO as external parts.
The minimum pitch variation achievable is 0.1%. The output of this 1st-stage PLL is used as the base signal for all the clock pulses to be used in the LSI.
When vari-pitch control is not performed, connect the output pin of XTAO to the VCKI pin.

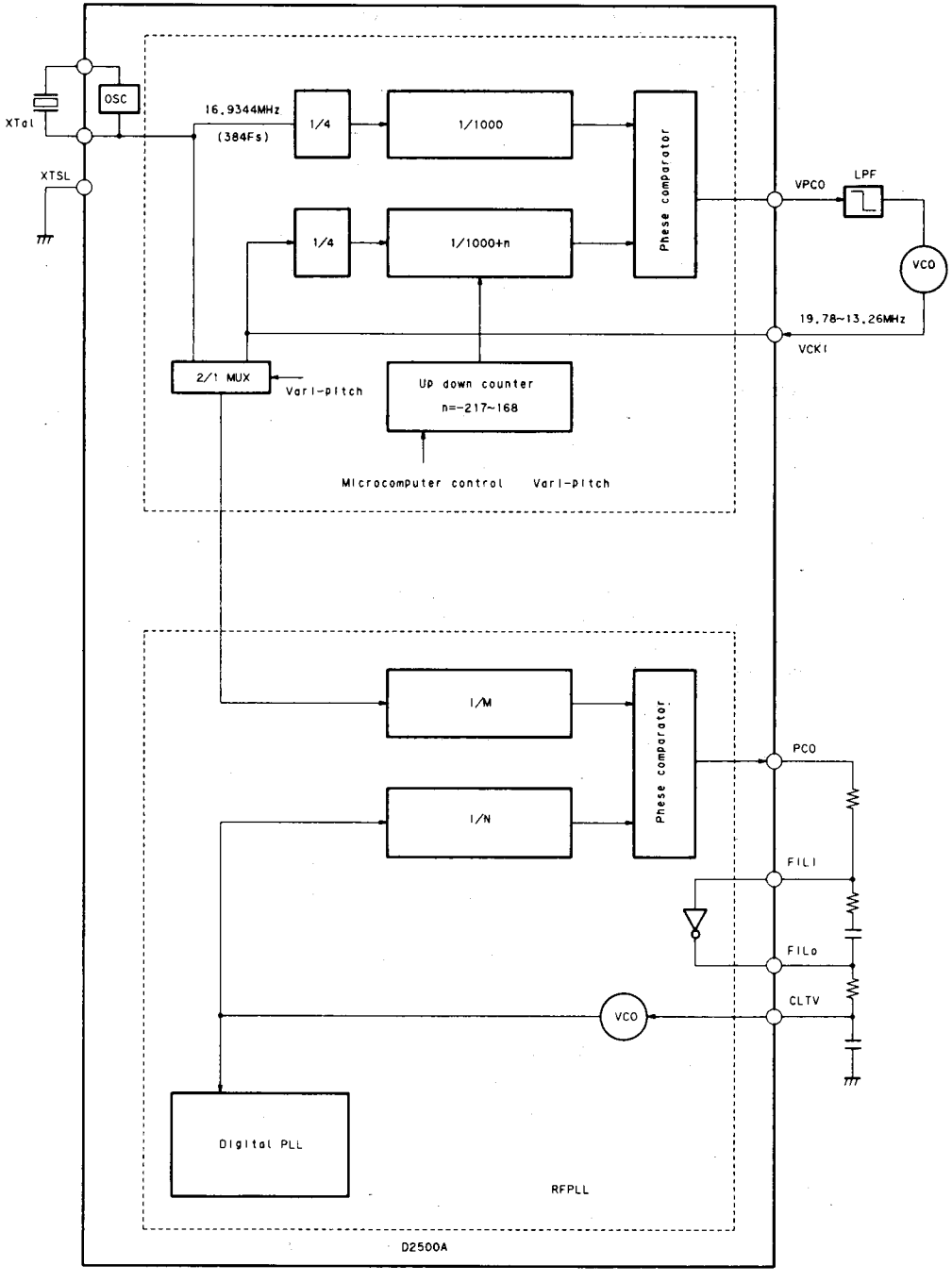
○ The 2nd-stage PLL generates R.F. clock pulses for use by the 3rd-stage digital PLL.

○ The 3rd-stage comprises a digital PLL used to regenerate channel clock pulses. It realizes a capture range of ±150kHz (normal condition) or more.

○ The digital PLL features a secondary loop. It is controlled through the primary loop (phase) and secondary loop (frequency).
When FLFC=1, the secondary loop can be turned off.

○ When high frequency components such as 3T, 4T or else, are offset, turning off the secondary loop will provide better play ability.
In this case, however, capture range reaches 50kHz.

Block Diagram 3-1



§ 3-2 Frame Sync Protection

- During CD player operation at normal speed, Frame Sync is recorded about every 136μs (at 7.35kHz). This signal can be used to identify the data within each frame. When Frame Sync cannot be recognized for any data, the data cannot be identified and, as a result, it is treated as an error. Therefore, correct Frame Sync recognition is very important to ensure high playability for the CD player.
- For Frame Sync protection, the CXD2500A employs window protection, front protection and rear protection. These measures combined realize powerful Frame Sync protection. The CXD2500 offers two window widths, one for use when the player is subjected to rotational disturbance and the other for use without such disturbance involved (WSEL=0/1).
  The front portection counter is fixed at count 13 and the rear protection counter at 3. Therefore, if, while Frame Sync signals are regenerated normally, regenerated signals cannot be detected, for example, due to flaws on the disc, up to 13 frames can be interpolated. If the number of frames with undetected Frame Sync exceeds 13, the window is released and the Frame Sync signals are re-synchronized. If no Frame Sync is correctly detected in 3 successive frames immediately after Frame Sync re-synchronization performed following a window release, the window is released at once.

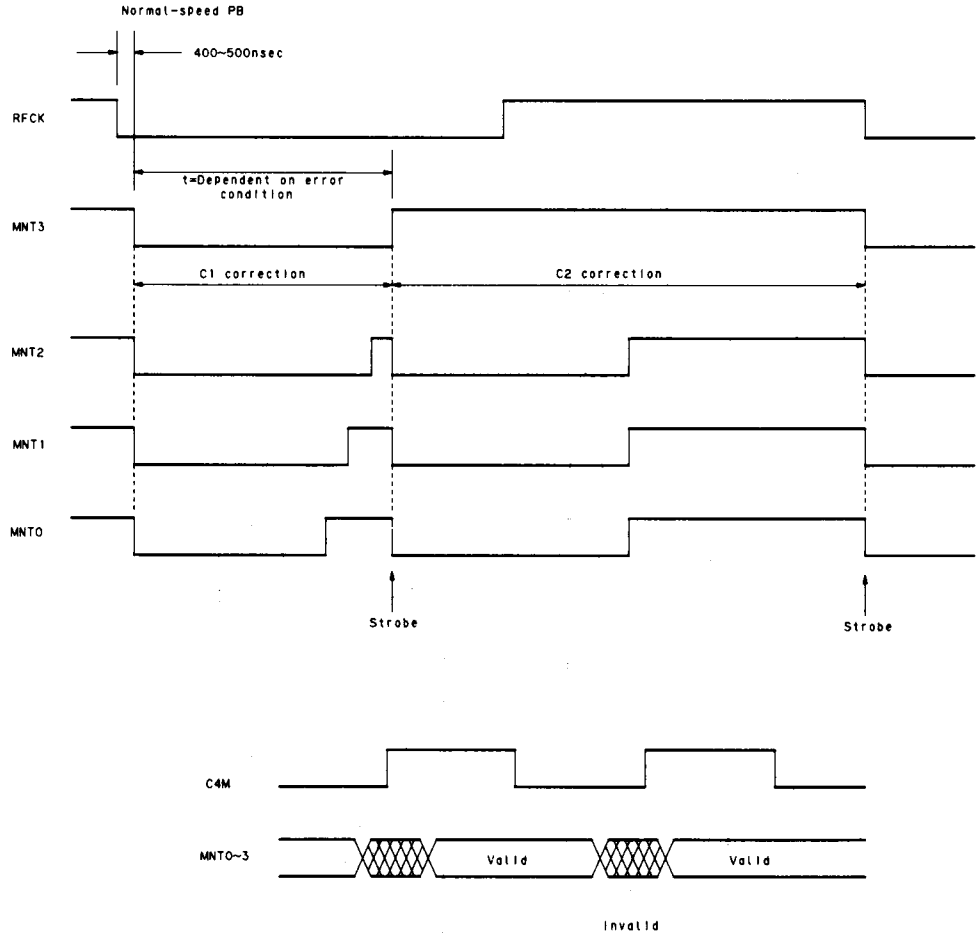
§ 3-3 Error Correction

- On CDs, each data unit (8bits) is formated so that it is contained in two correction codes, C1 and C2. C1 consists of 28 bytes of information and a 4-byte parity, whereas C2 are made up of 24 bytes of information and a 4-byte parity. Both C1 and C2 comprise a reed Solomon code with a minimum distance of 5.
- C1 realizes double corrections and C2 quadruple corrections, both, by the refined superstrategy method.
- When correction by C1 is made, a C1 pointer determined according to the contents of the error, the status of EFM signal regeneration and the condition of CD player operation is attached to the corrected data so as to prevent erroneous correction by C2.
- The status of error correction can be monitored from outside the LSI. It is indicated as shown in Table 3-2.
- If an uncorrectable data error is detected, the previous data that has been held is substituted for the erroneous data or substitute data is created by average-value interpolation. In either case, a C2 pointer attached to the substitute data is set high.

MNT3	MNT2	MNT1	MNT0	Description	
0	0	0	0	C1 : No error detected.	C1 pointer reset.
0	0	0	1	C1 : 1 error corrected.	C1 pointer reset.
0	0	1	0	———	
0	0	1	1	———	
0	1	0	0	C1 : No error detected.	C1 pointer set.
0	1	0	1	C1 : 1 error corrected.	C1 pointer set.
0	1	1	0	C1 : 2 errors corrected.	C1 pointer set.
0	1	1	1	C1 : Uncorrectable error.	C1 pointer set.
1	0	0	0	C2 : No error detected.	C2 pointer reset.
1	0	0	1	C2 : 1 error corrected.	C2 pointer reset.
1	0	1	0	C2 : 2 errors corrected.	C2 pointer reset.
1	0	1	1	C2 : 3 errors corrected.	C2 pointer reset.
1	1	0	0	C2 : 4 errors corrected.	C2 pointer reset.
1	1	0	1	———	
1	1	1	0	C2 : Uncorrectable error.	C1 pointer copied.
1	1	1	1	C2 : Uncorrectable error.	C2 pointer set.

Table 3-2 Indication of error correction status

Timing Chart 3-3



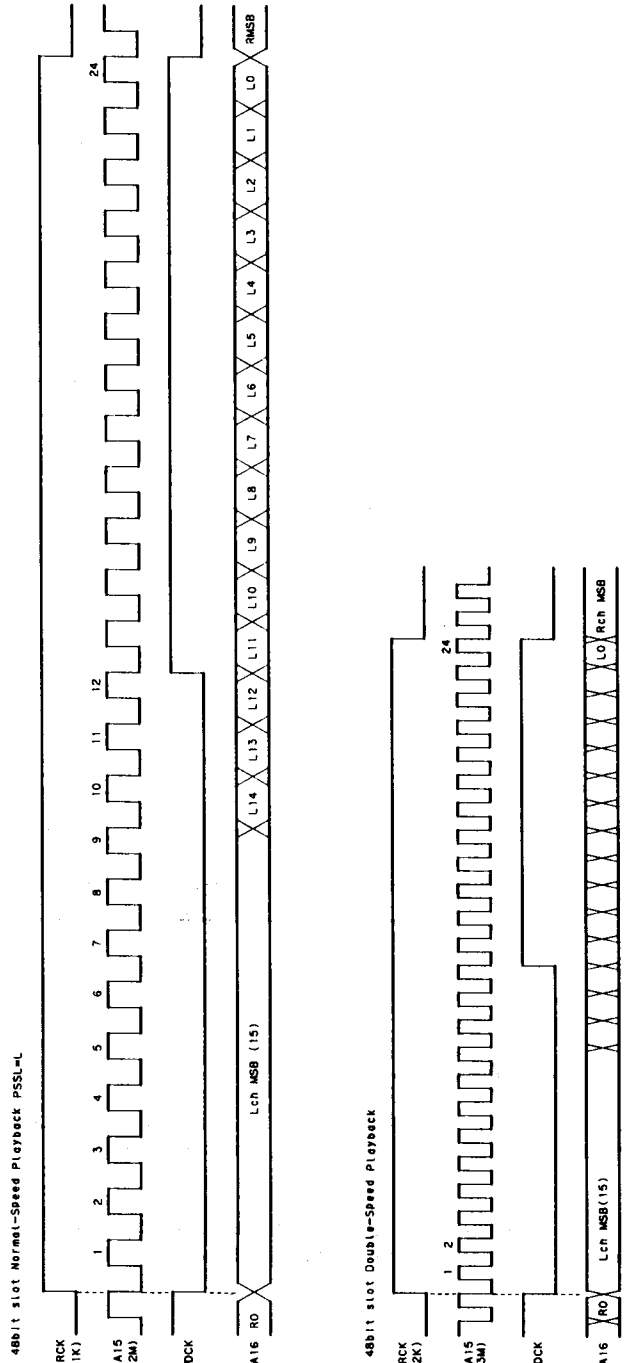
§ 3-4 DA Interface

○ The CXD2500A has two modes of DA interface.

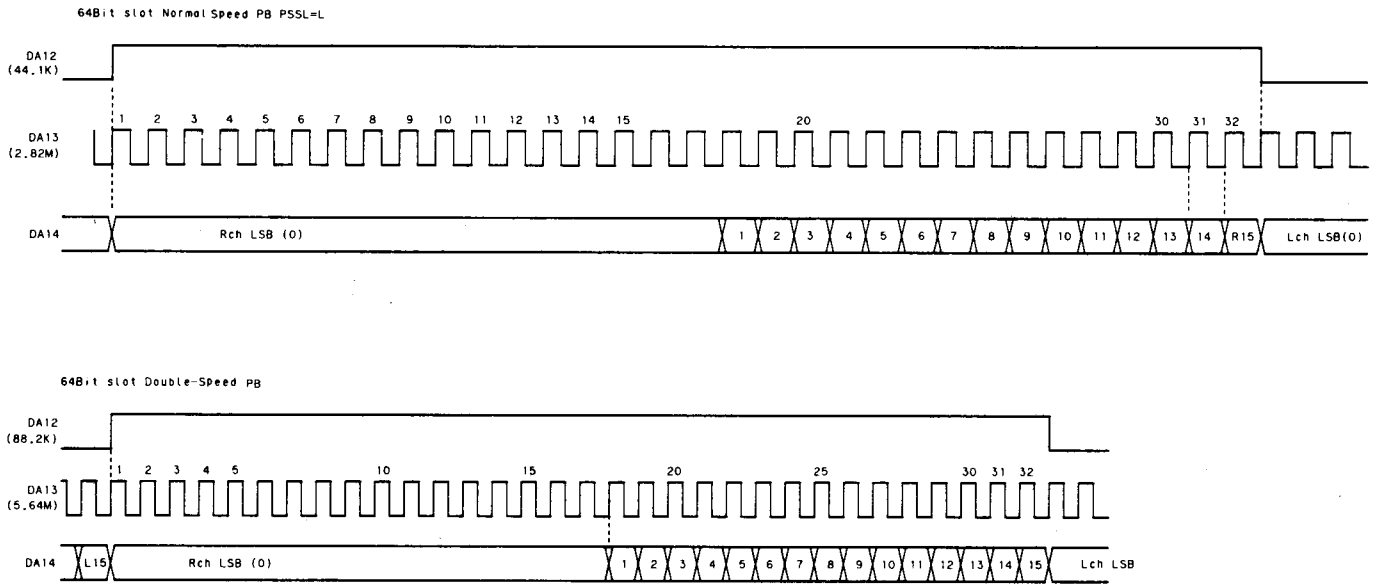
a). 48-bit slot interface
This is an MSB-first interface made up of LRCK signals with 48bit clock cycles per LRCK cycle. While the LRCK signal is high, the data going through this interface is of the left channel.

b). 64-bit slot interface
This is an LSB-first interface made up of LRCK signals with 64bit clock cycles per LRCK cycle. While the LRCK signal is low, the data going through this interface is of the left channel.

Timing Chart 3-4



Timig Chart 3-5



§ 3-5 Digital Out

There are three digital-out formats: type 1 for use at broadcasting stations, type 2, form 1 for use in general civil applications, and type 2, form 2 for use in software production. The CXD2500A supports type 2, form 1.

The clock accuracy for the channel status is automatically set at level II when the Xtal clock is used or level III when vari-pitch control is made.

CRC checks are conducted on the Sub Q data on the first 4 bits (bits 0-3). The data is input only after two checks are passed in succession.

The Xtal clock is set to 32MHz, and variable pitch is reset. When DSPB is set to 1, as D out is output, set MD2 to 0 and D out to off.

Digital Out C bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	IDO	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

Bits 0-3: Sub Q control bits required to pass the CRC twice in succession.
bit 29 : Varipitch: 1 Xtal: 0

Table 3-6 Digital Out C bits

§ 3-6 Servo Auto Sequencer

The servo auto sequencer controls a series of operation including auto-focusing and track jumping. When an auto sequence command is received from the CPU, the servo auto sequencer automatically executes auto-focusing, 1-track jumping, 2N track jumping and N track moving.

During auto sequence execution (X Busy=Low), as SSP (servo signal processing LSI) is used exclusively, commands from the CPU are not transferred to SSP. Still, commands can be sent to CXD2500A.

To make this servo auto sequencer usable, connect a CPU, RF and SSP to the CXD2500Q as shown in Figure 3-7 and set A.SEQ ON-OFF of register 9 to ON.

When X Busy is at Low, as the clock turns from Low to High, from there and for a maximum of 100μsec, X Busy does not turn to High.

As this clock is at Low (when X Busy is at Low), and through the monostable multivibrator that is reset, when X Busy changes from Low to High, transfer of error data to SSP is prevented.

(a) Auto Focus ($47)

In auto focus operation, 'focus search up' is perfomed, FOK and FZC are checked, and the focus servo is turned on. When a $47 is received from the CPU, the focus servo is turned on through the steps shown in Figure 3-8. Since this auto focus sequence bigins with 'focus search up,' it requires the pickup to be put down (focus search down) beforehand.

Blind E of register 5 is used to prevent FZC from flapping. The focus servo is turned on when FZC goes low after staying high for a period longer than E.

CXD2500Q System Configuration for Auto Sequencer Operation (Example)

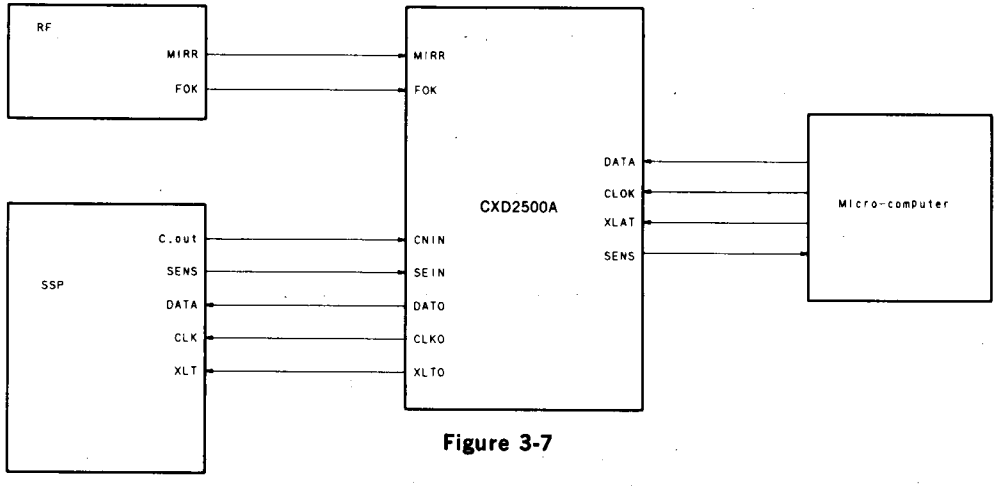


Figure 3-7

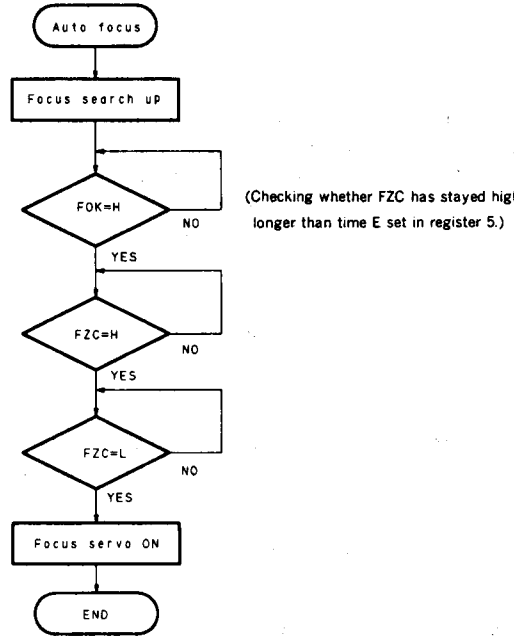


Figure 3-8 (a) Flowchart of auto focus operation

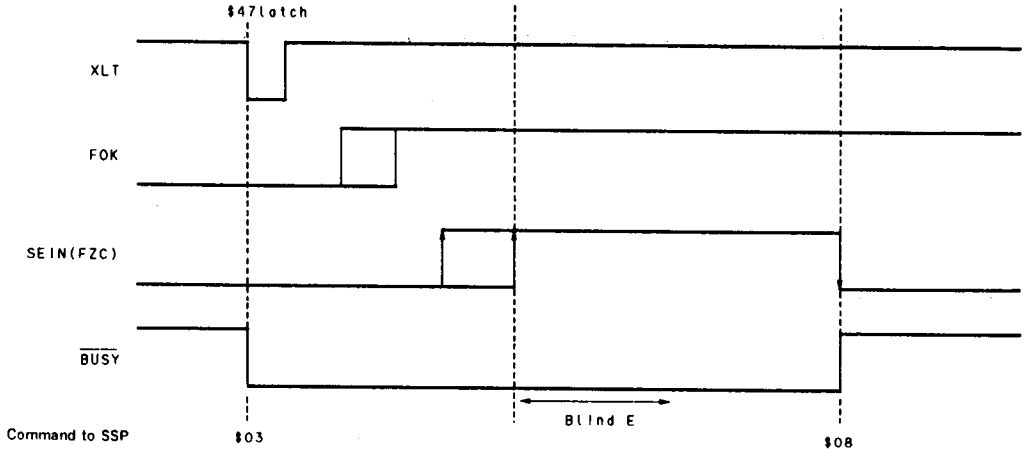


Figure 3-8 (b) Timing chart for auto focus operation

(b) Track Jump

Track jump operation includes 1, 10 and 2N track jumps. Do not perform this track jump unless the focus, tracking and sled servos are on. Such steps as tracking gain up and braking are not included in this track jump. Therefore, the commands for tracking gain up and brake on ($17) must be issued in advance.

○ 1-track jump

When a $48 (or a $49 for a REV jump) is received from the CPU, the servo auto sequencer executes a FWD (REV) 1-track jump as shown in Figure 3-9. The values of blind A and brake B must be set in register 5.

○ 10-track jump

When a $4H (or a $4B for a REV jump) is received from the CPU, the servo auto sequencer executes a FWD (REV) 10-track jump as shown in Figure 3-10. The principal difference between the 1-track and 10-track jumps is whether the sled is kicked or not. In the 10-track jump, the actuator after being kicked is braked when CNINs have been counted for 5 tracks. When the actuator has adequately slowed down as a result of braking, the tracking and sled servos are turned on (this actuator slow-down is detected by checking whether the CNIN period has exceeded the time specified as overflow C in register 5).

○ 2N track jump

When a $4C (or a $4D for a REV jump) is received, the servo auto sequencer executes a FWD (REV) 2N track jump. The number of tracks to be jumped is determined by N whose value is to be set in register 7 beforehand. The maximum permissible number is 2^{16}. In reality, however, it is subject to limitation imposed by the actuator.

When N is smaller than 16, the jumps are counted by means of counting CNIN signals. If N is not smaller than 16, MIRR signals are counted instead of the CNIN signals.

The 2N track jump sequence is basically the same as the 10-track jump sequence. The only difference between them is that, in the 2N track jump sequence, the sled is kept moving for time D specified in register 6 after the tracking servo is turned on.

○ N track move

When a $4E (or a $4F for a REV move) is received from the CPU, the servo auto sequencer executes a FWD (REV) N-track move as shown in Figure 3-12. The maximum value that can be set for N is 2^{16}. The track moves are counted in the same way as for 2N track jumps. That is, when N is smaller than 16, the moves are counted by means of counting CNIN signals. If N is not smaller than 16, MIRR signals are counted instead of the CNIN signals. In this N track move, only the sled is moved. This method is suitable for a large track move ranging from several thousand to several tens of thousand of tracks.

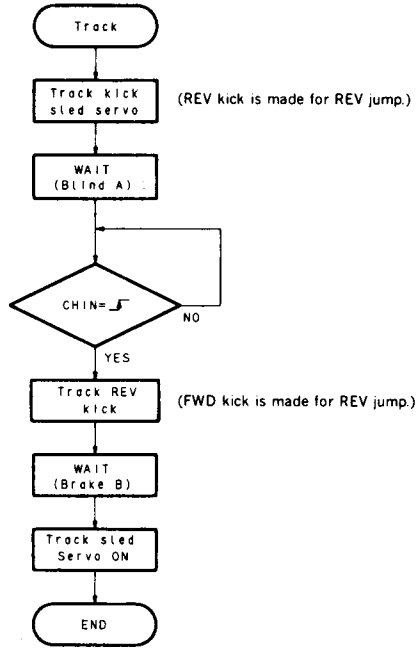


Figure 3-9 (a) Flowchart of 1-track jump

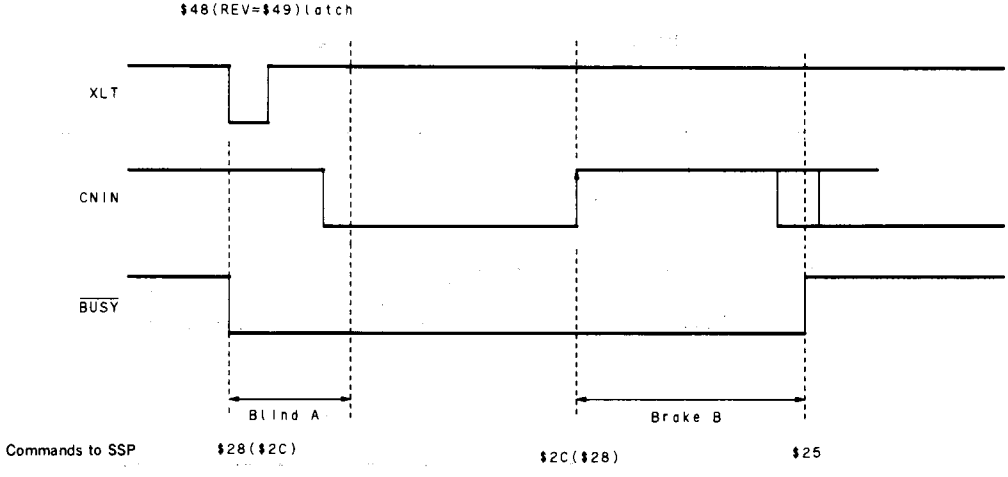


Figure 3-9 (b) Timing chart for 1-track jump

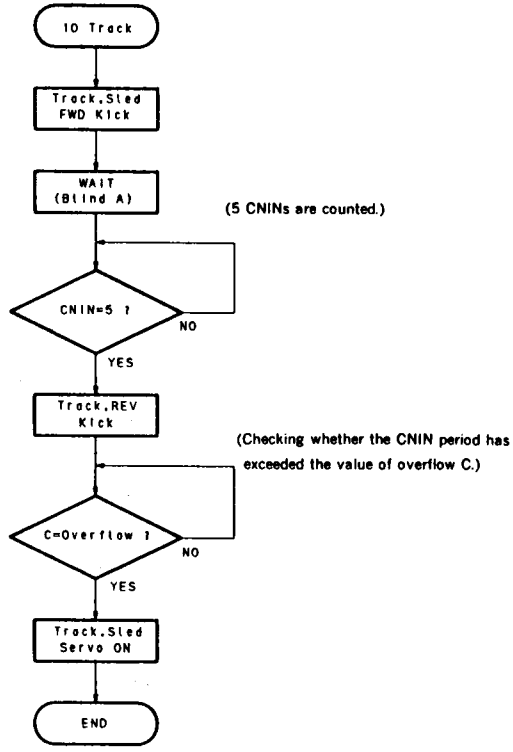


Figure 3-10 (a) Flowchart of 10-track jump

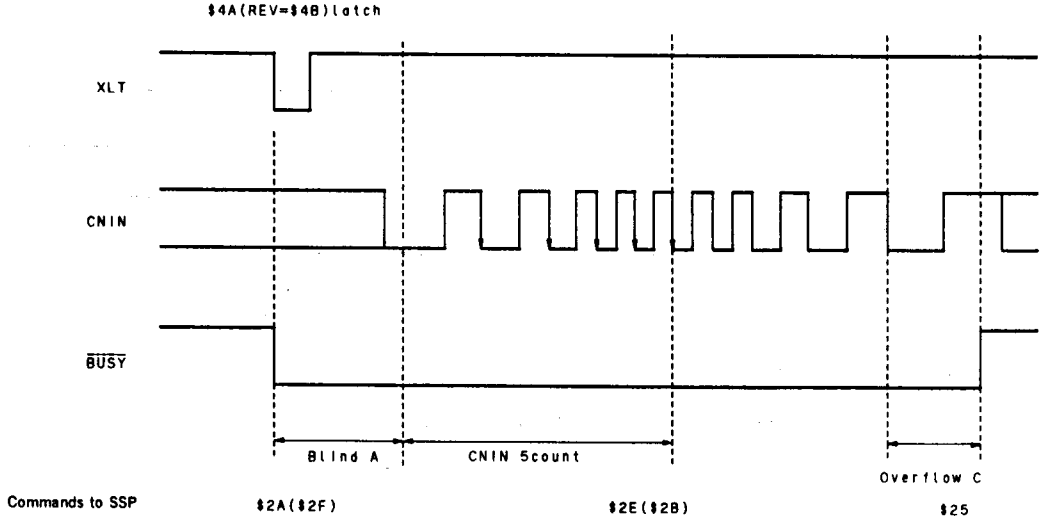


Figure 3-10 (b) Timing chart for 10-track jump

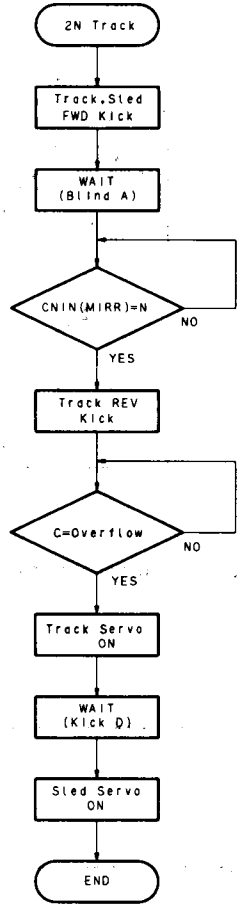


Figure 3-11 (a) Flowchart of 2N track jump

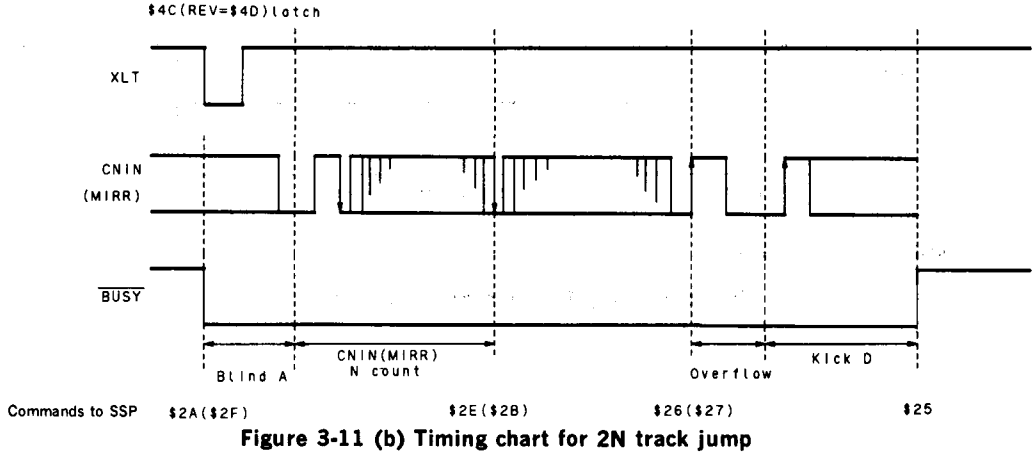
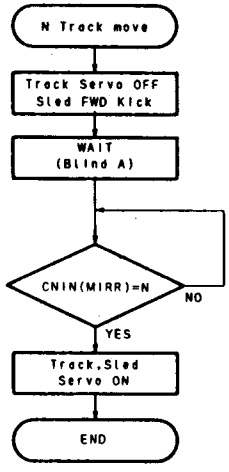


Figure 3-11 (b) Timing chart for 2N track jump



(Up to N<16 CNIN is counted while MIRR is counted until N≧16.)

Figure 3-12 (a) Flowchart of N track move

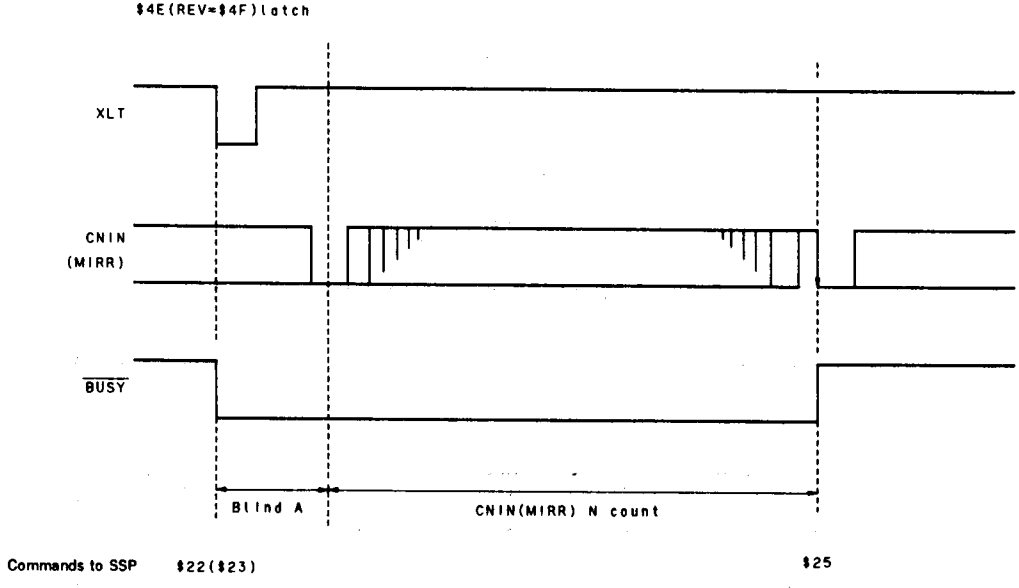


Figure 3-12 (b) Timing chart for N track move

§ 3-7 Digital CLV

The digital CLV is a digital spindle servo, a block diagram of which is shown in Figure 3-14. It is capable of outputting MDS or MDP error signals by the PWM method after raising the sampling frequency up to 130kHz based on the normal speed in the CLVS, CLVP or another appropriate mode. It permits gain setting, also.

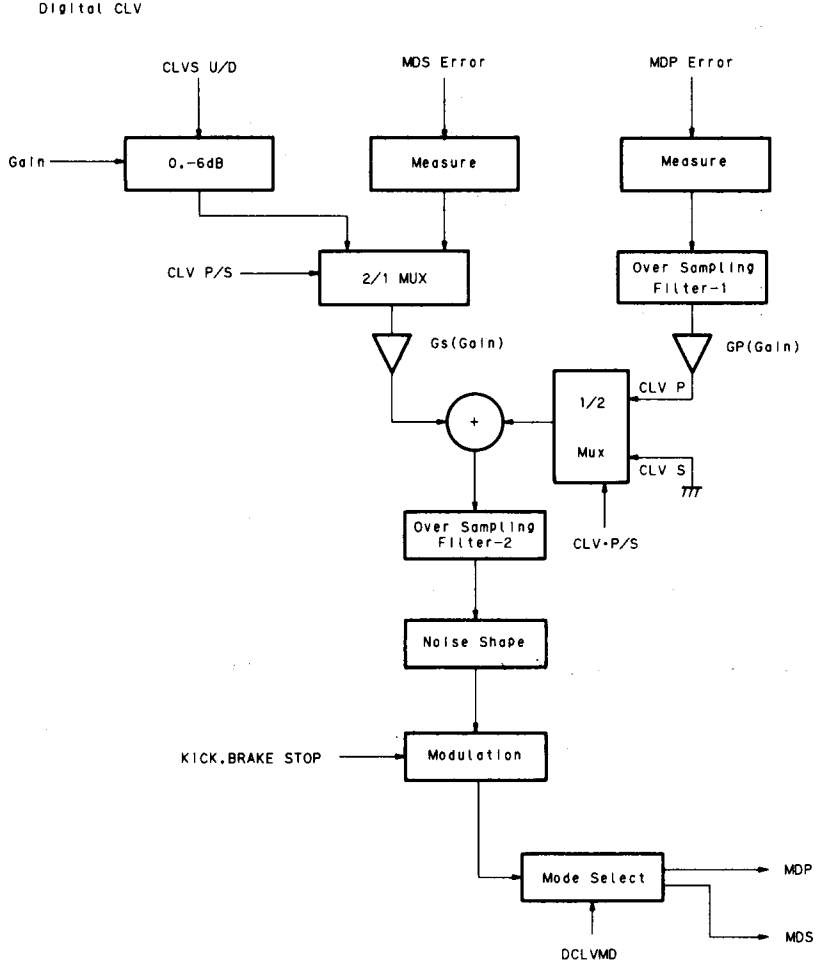


Figure 3-14 Block diagram

§ 3-8 Asymmetry correction

Block diagram and circuit example are shown on Fig. 3-15.

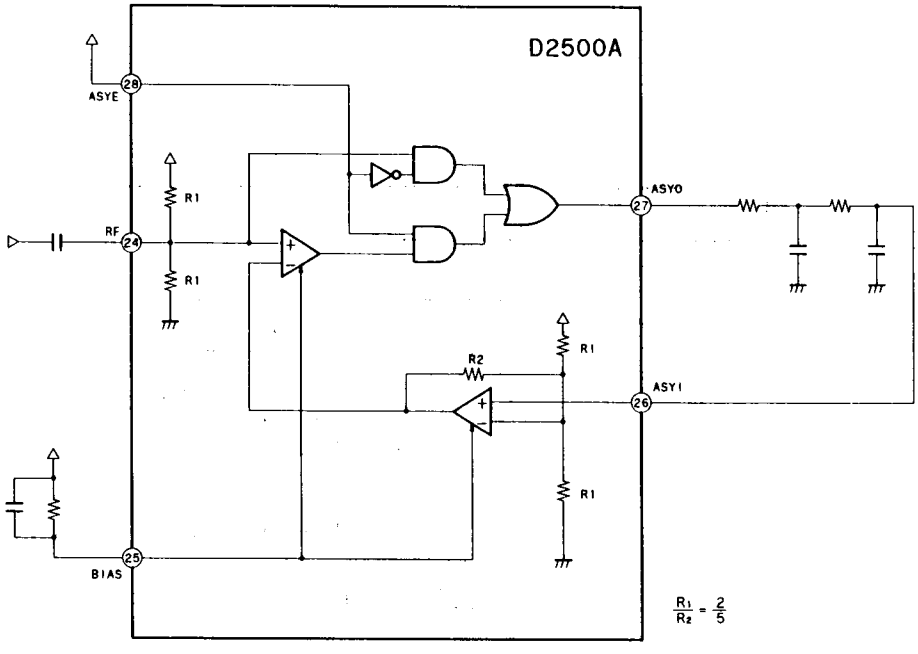
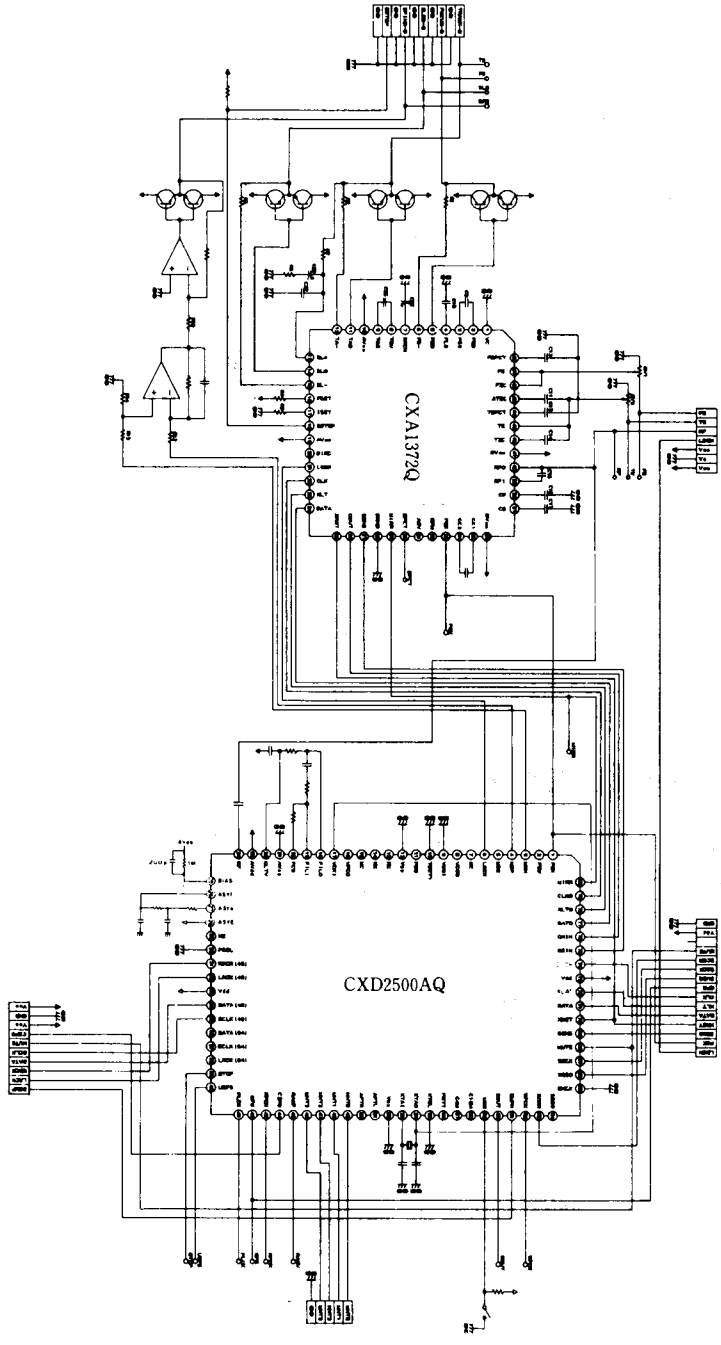


Figure 3-15 Asymmetry correction application circuit example

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

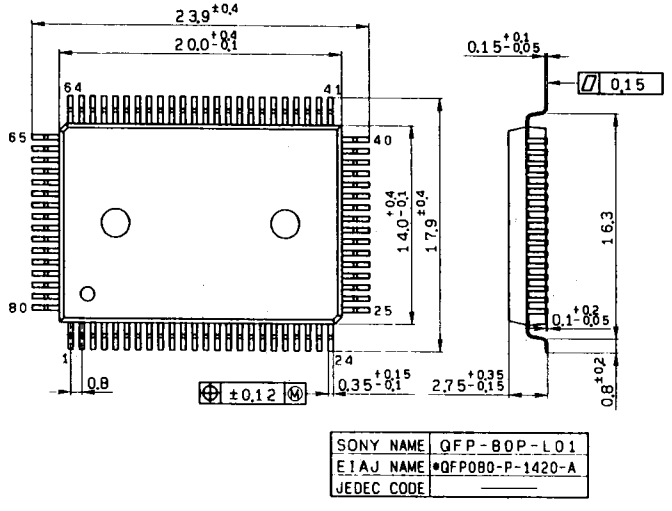


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit : mm

CXD2500AQ

80pin QFP (Plastic) 1.6g



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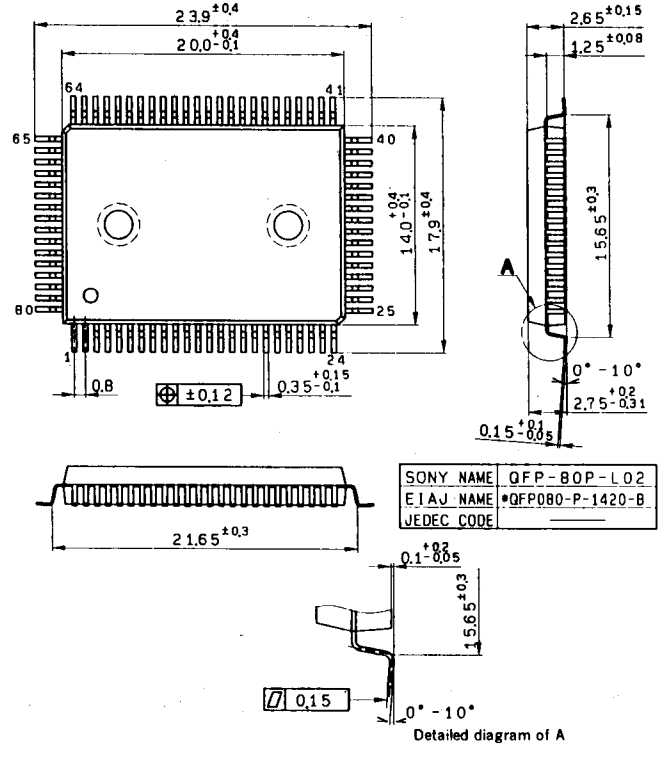
JEDEC CODE	

CXD2500AQZ

80pin QFP (Plastic) 1.6g

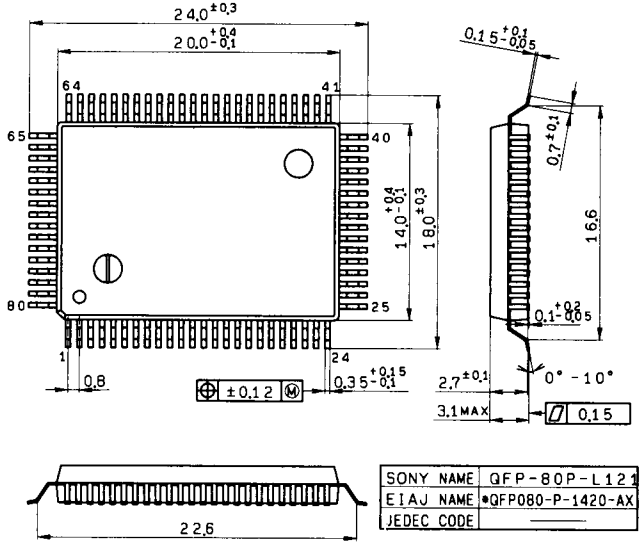


SONY NAME	QFP-80P-L02
EIAJ NAME	•QFP080-P-1420-B
JEDEC CODE	

Detailed diagram of A

CXD2500AQ

80pin QFP (Plastic)



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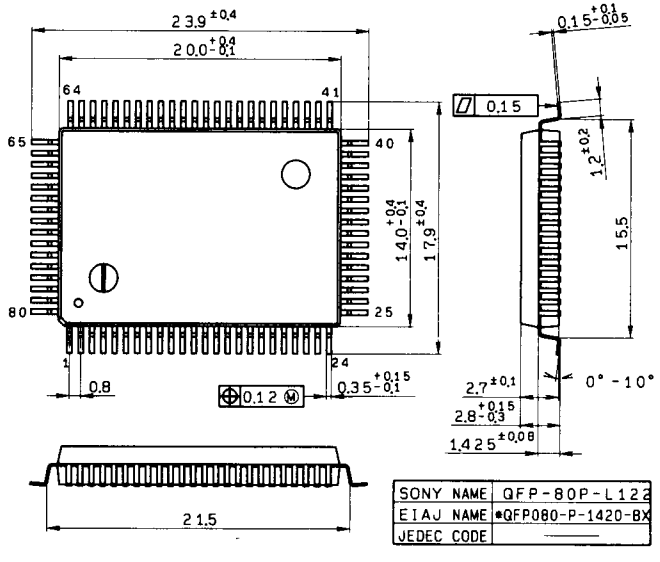
CXD2500AQZ

80pin QFP (Plastic)



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