STANDARD MICROSYSTEMS CORPORATION

APPLICATION NOTE 4.14

FDC37C6XX DMA IDE SUPPORT

This note demonstrates two possible implementations of the IDE DMA option using the FDC37C651/625, FDC37C661/662, FDC37C663/664, and FDC37C665/666.

OVERVIEW

The IDE DMA option can be implemented by adding a small amount of logic around the FDC37CXX chip. The attached schematic shows some additions to the SIO6001 schematic to add the IDE DMA option.

OPERATION

To implement the DMA IDE option, nDACK/ is used to enable the IDE data bus to the ISA bus. IOR/ is used to control the direction of the transfer.

Implementation 1

The IDE DMA Implementation 1 is shown in Figure 1. This implementation shows the addition of U2 and U4A to implement the DMA option. U2 is used to connect the low byte of the DMA transfer and U4A is used to add the DMA control to U3 to connect the high byte of the DMA transfer during DMA cycles.

Implementation 2

The IDE DMA Implementation 2 is shown in Figure 2. This implementation shows the addition of U7A, U7B, U4B, U4C, U8A, U8B, and U9A to implement the DMA option. In this implementation, U4B and U4C are used to add the DMA control to U5 and U6 to connect the IDE data bus to the ISA data bus during DMA cycles. Because bit IDED7 must only be connected to the ISA bus during the DMA transfers, a 1 bit bidirectional buffer is constructed using U7A, U7B, U8A, U8B and U9A.

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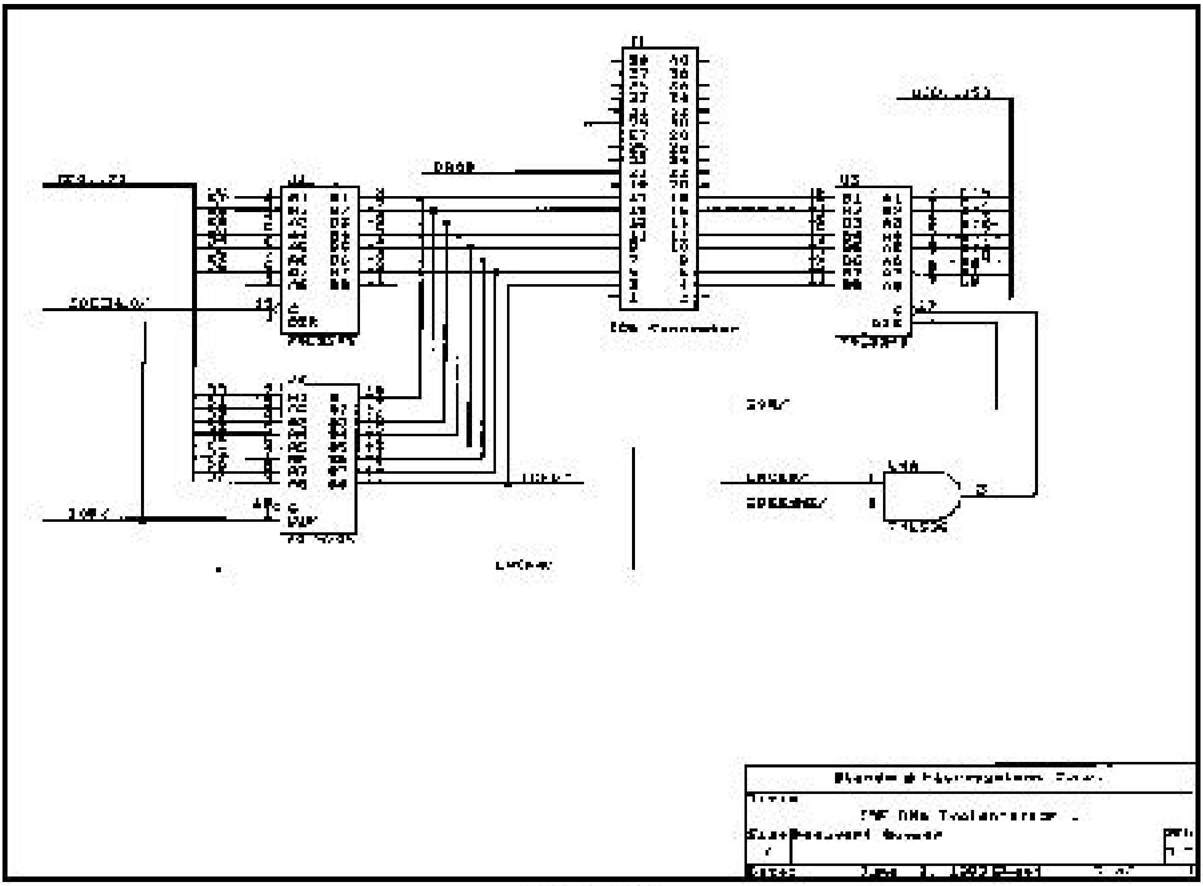

FIGURE 1

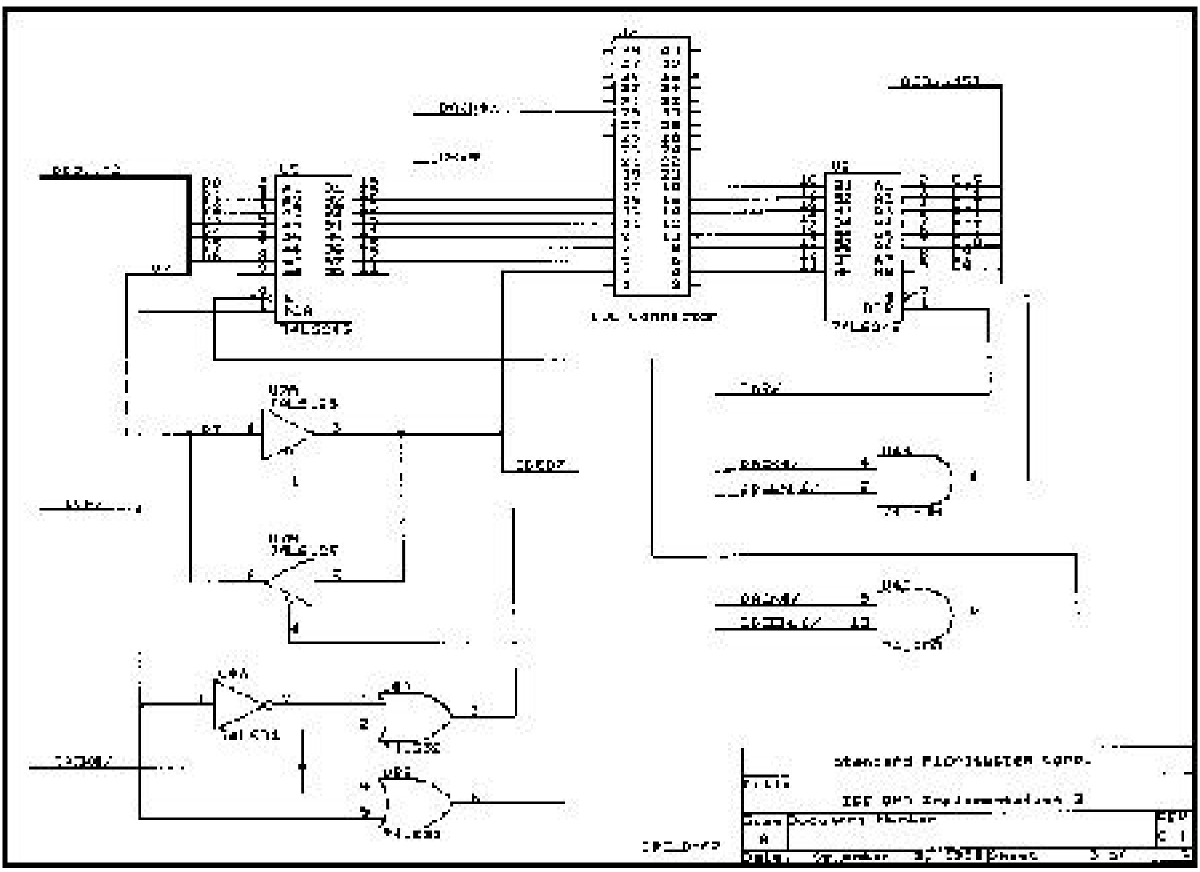

FIGURE 2