STANDARD
MICROSYSTEMS
CORPORATION

APPLICATION NOTE 6.6

FDC37C93xFR DESIGN GUIDE

By Robert Schoepflin

This application note is a design guide for the FDC37C93xFR. It describes the pins, including the different modes and functions available in the part and their associated pin functions. There are two sections that describe some of the applications of the GPI/Os and Soft Power Management features. Appendix A contains a table of the multifunction pins on the FDC37C93xFR for quick reference. A schematic of the FDC37C93xFR evaluation board is also included at the end of this application note for reference.

INTRODUCTION

The FDC37C93xFR is an Ultra I/O controller with an extensive feature set in a 160 pin QFP package. This part incorporates the basic features of an Ultra I/O controller, including a floppy disc controller, two 16550 compatible UARTs, a parallel port with ECP and EPP support, IDE interface, a keyboard interface and real-time clock. It also includes a IR functionality, soft power management, SMI support and ACCESS.bus support. The FDC37C93xFR also provides 42 GPI/O pins, two group interrupts, three general purpose address decoders, Port 92 support, 24/48MHz output option, and the ability to relocate the configuration registers to any I/O address.

The IR support includes the Fast IrDA at 1.152Mbps and 4Mbps, Consumer IR and support for TV type remote controls. The soft power management allows the chip to directly control the power supply and turn the computer on and off under software control or user inputs. The enhanced RTC includes a 100 year alarm and a century byte to keep track of the centuries. The soft power management combined with the enhanced RTC allows the implementation of new capabilities to the machine. The machine will be able to wakeup (i.e., turn itself on) at a predetermined time (within the next 100 years) or once a minute, hour, day week month or year to do regular maintenance such as performing a tape back-up, or send out a fax when the telephone rates are the lowest. It will also be able to shut itself off at any time, such as when the user exits Windows 95 instead of having the user wait for the “OK to Shut Off the Machine” and doing it manually.

80 Arkay Drive
Hauppauge, NY 11788
(516) 435-6000
FAX (516) 273-3123

FEATURES/PINS

The main features of the FDC37C93xFR are listed in the table below with their corresponding pins.

FEATURE	PINS
Processor/Host Interface	22, 35-39, 41-59, 61-70, 72-90
FDC Interface	2-7, 9-20
Serial Port 1	145-152
Serial Port 2	153-160
IDE1	23-26, 30, 31
IDE2	27-29
Parallel Port	126-129, 131-138, 140-144
Real Time Clock	121, 122, 123, 124
Keyboard/Mouse	91-94 (8042 pins: 105, 110, 113-118)
General Purpose I/O	19, 20, 23-26, 30, 31, 33, 34, 96-100, 102-120, 153-160
BIOS Buffers	111-120
IR / Fast IR	19, 98, 99, 120, 155, 156
Soft Power Management	33, 34 (VTR: 32)
SMI Support	31
ACCESS.bus	106, 107
Watch Dog Timer Output	30, 98, 112
Power LED Output	30, 99, 111
Serial EEPROM	106-109
GP Address Decoders	24, 25, 100

PIN DESCRIPTION/INTERFACE

Pin 1. Ground.

Pin 2: DRVDEN0. Drive density select 0, open drain output. Connect to the floppy connector pin 2.

Pin 3: DRVDEN1. Drive density select 1, open drain output. Connect to the floppy connector pin 6.

Pin 4: nMTR0. Motor on 0, active low open drain output. Connect to floppy connector pin 10.

Pin 5: nods. Drive select 1, active low open drain output. Connect to floppy connector pin 12.

Pin 6: nDS0. Drive select 0, active low open drain output. Connect to floppy connector pin 14.

Pin 7: nMTR1. Motor on 1, active low open drain output. Connect to floppy connector pin 16.

Pin 8: Ground.

Pin 9: nDIR. Step direction, active low open drain output. Connect to floppy connector pin 18.

Pin 10: nSTEP. Step pulse, active low open drain output. Connect to floppy connector pin 20.

Pin 11: nWDATA. Write disk data, active low open drain output. Connect to floppy connector pin 22.

Pin 12: nWGATE. Write gate, active low open drain output. Connect to floppy connector pin 24.

Pin 13: nHDSEL. Head select, active low open drain output. Connect to floppy connector pin 32.

Pin 14: nINDEX. Index pulse input, active low input with Schmitt trigger. Connect to floppy connector pin 8.

Pin 15: nTR0. Track 0, active low input with Schmitt trigger. Connect to floppy connector pin 26.

Pin 16: nWPROT. Write protected, active low input with Schmitt trigger. Connect to floppy connector pin 28.

Pin 17: nRDATA. Read disk data, active low input with Schmitt trigger. Connect to floppy connector pin 30.

Pin 18: nDSKCHG. Disk change, active low input with Schmitt trigger. Connect to floppy connector pin 34.

Pin 19: MEDIA_ID1/GP40/IR Mode/IRR3.
MEDIA_ID1: Media id input 1, active low input with Schmitt trigger. Connect to floppy connector pin 33. Note: this input is only used for floppy enhanced mode 2, otherwise it is grounded.
GP40: General purpose I/O, input/output. See GPI/O Applications Section.
IR Mode: IR mode pin, output. This pin is used by Fast IR modules that require an input to set the receiver's bandwidth. (Used to control TEMIC Fast IR modules). See Application Note 5-17, "Multiple Footprint for FDC37C93X, FDC37C93XPM and FDC37C93XFR" for a description of the proper use of this pin for Fast IR.
IRR3: IR Receive 3, input. Fast IR receive data input. This pin is used by Fast IR modules that employ a second receive data output when high data rate (4Mbps) is used. (Used for HP Fast IR modules).

Pin 20: MEDIA_ID0/GP41.
MEDIA_ID0: Media id input 0, active low input with Schmitt trigger. Connect to floppy connector pin 29. Note: this input is only used for floppy enhanced mode 2, otherwise it is grounded.
GP41: General purpose I/O, input/output. See GPI/O Applications Section.

Pin 21: Vcc

Pin 22: CLOCKI. 14.318MHz clock input. Connect to 14.318MHz crystal oscillator.

Pin 23: nIDE1_OE/GP42.
nIDE1_OE: IDE1 enable, active low output. Connect to pin 19 of both the high and low byte buffer chips (74LS245) for IDE1 header.
GP42: General purpose I/O, input/output. See GPI/O Applications Section.

Pin 24: nHDCS0/GP43.
nHDCS0: IDE1 chip select 0, active low output. Connect to pin 37 of IDE1 header. Also connect to pin 17 of the 8584 ACCESS.bus controller chip through a 3 pin header, if used (see Note 1).
GP43: General purpose I/O, input/output. See GPI/O Applications Section.

Pin 25: nHDCS1/GP44.
nHDCS1: IDE1 chip select 1, active low output. Connect to pin 38 of IDE1 header.
GP44: General purpose I/O, input/output. See GPI/O Applications Section.

Pin 26: IDE1_IRQ/GP45.
IDE1_IRQ: IDE1 interrupt request, input. Connect to pin 31 of IDE1 header.
GP45: General purpose I/O, input/output. See GPI/O Applications Section.

Pin 27: nHDCS2/SA13.
nHDCS2: IDE2 chip select 2 active low output. Connect to pin 37 of IDE2 header. Note: requires a pull up to ensure a logic high at power-up when used for IDE2 until the active bit is set to 1.
SA13: System address line 13 (if 16-bit extended addressing is to be used), input. Connect to pin 1 of 3x2 alternate 16-bit address qualification header, pin 18 of ISA A connector, pin 1 of boot ROM address buffer chip (L1027), pin 26 of boot ROM chip (L1130). Also connect to the circuitry used to "OR" the address lines SA[12:15] (see pin 53 description).

Pin 28: nHDCS2/SA14.

nHDCS2: IDE2 chip select 3 active low output. Connect to pin 38 of IDE2 header. Note: requires a pull up to ensure a logic high at power-up when used for IDE2 until the active bit is set to 1.

SA14: System address line 14 (if 16-bit extended addressing is to be used), input. Connect to pin 3 of 3x2 alternate 16-bit address qualification header, pin 17 of ISA A connector, pin 2 of boot ROM address buffer chip (L1027). Also connect to the circuitry used to "OR" the address lines SA[12:15] (see pin 53 description).

Pin 29: IDE2_IRQ/SA15.

IDE2_IRQ: IDE2 interrupt request input. Connect to pin 31 of IDE2 header.

SA15: System address line 15 (if 16-bit extended addressing is to be used), input. Connect to pin 5 of 3x2 alternate 16-bit address qualification header pin 16 of ISA A connector, pin 3 of boot ROM address buffer chip (L1027). Also connect to the circuitry used to "OR" the address lines SA[12:15] (see pin 53 description).

Pin 30: nIOROP/GP46/Power LED Output/WDT.

nIOROP: IOR output, active low output. Connect to pin 25 of IDE1 and IDE2 header.

GP46: General purpose I/O, input/output. See GPI/O Applications Section.

Power LED Output: Connect to GPI/O LED.

WDT: Watch Dog Timer output.

Pin 31: nIOWOP/GP47/nSMI.

nIOWOP: IOW output, active low output. Connect to pin 23 of IDE1 and IDE2 header.

GP47: General purpose I/O, input/output. See GPI/O Applications Section.

nSMI: System Management Interrupt, active low group interrupt output.

Pin 32: VTR. Trickle voltage input (5 volts at 2mA maximum). Connect to trickle voltage output of "smart" power supply. Used by soft power management control logic to power chip in low power (standby) mode. See Application Note 5-17, "Multiple Footprint for FDC37C93X, FDC37C93XPM and FDC37C93XFR" for a description of the proper use of this pin for soft power management.

Pin 33: nPowerOn/GP51, defaults to active low open collector output for nPowerOn.

nPowerOn: Power on output, active low output. Connect to "smart" power supply on/off input. nPowerOn is used by soft power management control logic to turn the power supply on/off (power the system up from low power mode and to enter low power mode). This pin will go to a logic low (turn power supply on) when Button_In goes from logic high to logic low. Other wakeup events (pressing a key, touching the mouse, receiving data from one of the UARTs, etc.) will also be used to activate this pin. See configuration section of data sheet for soft power management register description. Also see Application Note 5-17, "Multiple Footprint for FDC37C93X, FDC37C93XPM and FDC37C93XFR" for a description of the proper use of this pin for soft power management.

GP51: General purpose I/O, input/output. See GPI/O Applications Section.

Pin 34: Button_In/GP50, defaults to input for Button_In.

Button_In: Button input, input. Connect to main power switch. Button_In is used by soft power management control logic to turn the system on or off (power the system up from low power mode and to enter low power mode). A transition on this pin from logic high to logic low will cause nPowerOn pin to go low. See configuration section of data sheet for soft power management register description. Also see Application Note 5-17, "Multiple Footprint for FDC37C93X, FDC37C93XPM and FDC37C93XFR" for a description of the proper use of this pin for soft power management.

GP50: General Purpose I/O, input/output.

Pin 35: HCLK. High speed (24/48MHz) clock output.

Pin 36: 16CLK. 16MHz clock output.

Pin 37: CLK01. 14.318MHz clock output 1.

Pin 38: CLK02. 14.318MHz clock output 2.

Pin 39: CLK03. 14.318MHz clock output 3.

Pin 40: Ground

Pins 41-52: SA[0:11]. System address bus lines 0-11, input. Connect to ISA A connector pins 31-20. Also connect to boot ROM chip (L1130) address pins 10-3, 25, 24, 21, 23. SA0, SA1, and SA2 are also connected to the IDE1 and IDE2 connectors, pins 35, 33 and 36 respectively (after being buffered through the 74LS244 chip).

Pin 53: nCS/SA12. This pin is the active low chip select input; it must be low for all chip accesses. For 12 bit addressing, SA[0:11], this pin should be tied to ground. For 16 bit address qualification, address bits SA[12:15] can be ORed together and applied to this pin. If IDE2 is not used, SA12 can be connected to this pin (and also SA13 to pin 27, SA14 to pin 28 and SA15 to pin 29). Connect to pin 19 of ISA A connector, pin 2 of boot ROM chip (L1130). Also connect to the circuitry used to "OR" the address lines SA[12:15]. Note: 16 bit address qualification is an external decode of the upper 4 address bits; that is, if bits A12-A15 are zero, the chip gets a chip select.

Pin 54: IRQ15. Interrupt request 15, open drain output. Connect to resource header pin 42; this pin is connected through this header to pin 6 of the ISA bus connector extension, ISA D.

Pin 55: IRQ14. Interrupt request 14, open drain output. Connect to resource header pin 40; this pin is connected through this header to pin 7 of the ISA bus connector extension, ISA D.

Pin 56: IRQ12. Interrupt request 12, open drain output. Connect to resource header pin 38; this pin is connected through this header to pin 5 of the ISA bus connector extension, ISA D.

Pin 57: IRQ11. Interrupt request 11, open drain output. Connect to resource header pin 36; this pin is connected through this header to pin 4 of the ISA bus connector extension, ISA D.

Pin 58: IRQ10. Interrupt request 10, open drain output. Connect to resource header pin 34; this pin is connected through this header to pin 3 of the ISA bus connector extension, ISA D.

Pin 59: IRQ9. Interrupt request 9, open drain output. Connect to resource header pin 32; this pin is connected through this header to pin 4 of the ISA B connector.

Pin 60: Vcc

Pin 61: IRQ8. Interrupt request 8, open drain output. Connect to resource header pin 30.

Pin 62: IRQ7. Interrupt request 7, open drain output. Connect to resource header pin 28; this pin is connected through this header to pin 21 of the ISA B connector.

Pin 63: IRQ6. Interrupt request 6, open drain output. Connect to resource header pin 26; this pin is connected through this header to pin 22 of the ISA B connector.

Pin 64: IRQ5. Interrupt request 5, open drain output. Connect to resource header pin 24; this pin is connected through this header to pin 23 of the ISA B connector.

Pin 65: IRQ4. Interrupt request 4, open drain output. Connect to resource header pin 22; this pin is connected through this header to pin 24 of the ISA B connector.

Pin 66: IRQ3. Interrupt request 3, open drain output. Connect to resource header pin 20; this pin is connected through this header to pin 25 of the ISA B connector.

Pin 67: IRQ1. Interrupt request 1, open drain output. Connect to resource header pin 18.

Pin 68: nIOR. I/O read, input. Connect to ISA B connector pin 14, and the SMC34C759* buffer chip pin 14. (*THIS PART HAS BEEN DISCONTINUED). Connect to pin 25 of the IDE1 and IDE2 connectors (after being buffered through the 74LS244 chip). Also connect to pin 16 of the 8584 ACCESS.bus controller chip, if used (see Note 1).

Pin 69: nIOW. I/O write, input. Connect to ISA B connector pin 13, and the SMC34C759 buffer chip pin 15. Connect to pin 23 of the IDE1 and IDE2 connectors (after being buffered through the 74LS244 chip). Also connect to pin 18 of the 8584 ACCESS.bus controller chip if used (see Note 1).

Pin 70: AEN. Address enable, input. Connect to pin 11 of the ISA A connector.

Pin 71: Ground

Pin 72-79: SD[0:7]. System data bus, input/output. Connect to ISA A connector pins 9-2. Connect to the general purpose read/write chip (74LS374) as follows: SD0: pins 2 and 3, SD1: pins 4 and 5, SD2: pins 6 and 7, SD3: pins 8 and 9, SD4: pins 12 and 13, SD5: pins 14 and 15, SD6: pins 16 and 17, SD7: pins 18 and 19. Also connect to the low byte buffer chips (74LS245) for IDE1 and IDE2, pins 2-9. Connect SD0-6 to the SMC34C759 buffer chip, pins 7-13. Connect SD0-2 to pins 7-9 of the 8584 ACCESS.bus controller chip and SD3-7 to pins 11-15 of the 8584 ACCESS.bus controller chip, if used (see Note 1).

Pin 80: RESET_DRV. Reset drive, input with Schmitt trigger. Connect to ISA B connector pin 2, and the SMC34C759 buffer chip pin 6. Also connect to pin 5 of the 74LS00 to invert this signal for connection to pin 19 of the 8584 ACCESS.bus controller chip, if used (see Note 1).

Pin 81: nDACK0. DMA Acknowledge 0, input. Connect to resource header pin 2; this pin is connected through this header to pin 8 of the ISA bus connector extension ISA D.

Pin 82: DRQ0. DMA Request 0, output. Connect to resource header pin 4; this pin is connected through this header to pin 9 of the ISA bus connector extension ISA D.

Pin 83: nDACK1. DMA Acknowledge 1, input. Connect to resource header pin 6; this pin is connected through this header to pin 17 of the ISA B connector.

Pin 84: DRQ1. DMA Request 1, output. Connect to resource header pin 8; this pin is connected through this header to pin 18 of the ISA B connector.

Pin 85: nDACK2. DMA Acknowledge 2, input. Connect to resource header pin 10; this pin is connected through this header to pin 26 of the ISA B connector.

Pin 86: DRQ2. DMA Request 2, output. Connect to resource header pin 12; this pin is connected through this header to pin 6 of the ISA B connector.

Pin 87: nDACK3. DMA Acknowledge 3, input. Connect to resource header pin 14; this pin is connected through this header to pin 15 of the ISA B connector.

Pin 88: DRQ3. DMA Request 3, output. Connect to resource header pin 16; this pin is connected through this header to pin 16 of the ISA B connector.

Pin 89: TC. Terminal count, input. Connect to pin 27 of ISA B connector.

Pin 90: IOCHRDY. I/O channel ready, open drain output. Connect to pin 27 of IDE1 connector and pin 27 of IDE2 connector. Connect to pin 10 of ISA A connector.

Pin 91: KDAT. Keyboard data, input/output. Connect to a 3.3kΩ pull-up resistor to Vcc, a 100pF capacitor to ground and an inductor to the KDATA pin (pin 1) of the 6 pin keyboard connector.

Pin 92: KCLK. Keyboard clock, input/output. Connect to a 3.3kΩ pull-up resistor to Vcc, a 100pF capacitor to ground and an inductor to the KCLK pin (pin 5) of the 6 pin keyboard connector.

Pin 93: MDAT. Mouse data, input/output. Connect to a 3.3kΩ pull-up resistor to Vcc, a 100pF capacitor to ground and an inductor to the MDATA pin (pin 1) of the 6 pin mouse connector.

Pin 94: MCLK. Mouse clock, input/output. Connect to a 3.3kΩ pull-up resistor to Vcc, a 100pF capacitor to ground and an inductor to the MCLK pin (pin 5) of the 6 pin mouse connector.

Pin 95: Ground.

Pin 96: GP10, IRQ in.
GP10: General Purpose I/O, input/output. See GPI/O Applications Section.
IRQ in: If configured as input, the input signal is steered to the selected IRQ. See configuration section of FDC37C93xFR data sheet, Table 74 - Aux I/O, logical device 8.

Pin 97: GP11, IRQ in.
GP11: General Purpose I/O, input/output. See GPI/O Applications Section.
IRQ in: If configured as input, the input signal is steered to the selected IRQ. See configuration section of FDC37C93xFR data sheet, Table 74 - Aux I/O, logical device 8.

Pin 98: GP12, WDT Output/IRRX.
GP12: General Purpose I/O, input/output. See GPI/O Applications Section.
WDT Output/IRRX: Configurable as Watch dog timer output or IR receive input. As IRRX, connect to pin 1 of IR connector 2.

Pin 99: GP13, Power LED Output/IRTX.
GP13: General Purpose I/O, input/output. See GPI/O Applications Section.
Power LED Output/IRTX: Configurable as Power LED output or IR transmit output. As Power LED output, connect to GPI/O LED. As IRTX, connect to pin 3 of IR connector 2.

Pin 100: GP14, GP Address Decode.
GP14: General Purpose I/O, input/output. See GPI/O Applications Section.
GP Address Decode: General purpose address decode. Connect to pin 17 of the 8584 ACCESS.bus controller chip (if used) through a 3 pin header to select either this pin or nHDCS0 (see Note 1).

Pin 101: Vcc

Pin 102: GP15, GP Write Strobe.
GP15: General Purpose I/O, input/output. See GPI/O Applications Section.
GP Write Strobe: General purpose write strobe, output.

Pin 103: GP16, Joy Read Strobe, JOYCS.
GP16: General Purpose I/O, input/output. See GPI/O Applications Section.
Joy Read Strobe: Joystick read strobe, output.
JOYCS: Joystick chip select, output.

Pin 104: GP17, Joy Write Strobe.
GP17: General Purpose I/O, input/output. See GPI/O Applications Section.
Joy Write Strobe: Joystick write strobe, output.

Pin 105: GP20, IDE2 Output Enable, 8042 P20.
GP20: General Purpose I/O, input/output. See GPI/O Applications Section.
IDE2 Output Enable: IDE2 Output Enable, output. Connect to pin 19 of both the high and low byte buffer chips (74LS245) for IDE2 header.
8042 P20: 8042 P2.0, keyboard reset, output.

Pin 106: GP21, Serial EEPROM Data In, AB_DATA.

GP21: General Purpose I/O, input/output. See GPI/O Applications Section.
Serial EEPROM Data In: Serial EEPROM Data Input, input. Connect to pin 5 of the 4x2 pin header which (if jumpered) connects to pin 4 of XL93C46 EEPROM chip.
AB_DATA: ACCESS.bus data, input/output. Connect to pin 3 of 4-pin ACCESS.bus connector. Also connect to pin 2 of the 8584 ACCESS.bus controller and pin 5 of the 24C02 ACCESS.bus EPROM, if used (see Note 1).

Pin 107: GP22, Serial EEPROM Data Out, AB_CLK.

GP22: General Purpose I/O, input/output. See GPI/O Applications Section.
Serial EEPROM Data Out: Serial EEPROM data output, output. Connect to pin 7 of the 4x2 pin header which (if jumpered) connects to pin 3 of XL93C46 EEPROM chip.
AB_CLK: ACCESS.bus clock, input/output. Connect to pin 1 of 4-pin ACCESS.bus connector. Also connect to pin 3 of the 8584 ACCESS.bus controller and pin 6 of the 24C02 ACCESS.bus EPROM, if used (see Note 1).

Pin 108: GP23, Serial EEPROM Clock.

GP23: General Purpose I/O, input/output. See GPI/O Applications Section.
Serial EEPROM Clock: Connect to pin 3 of the 4x2 pin header which (if jumpered) connects to pin 2 of XL93C46 EEPROM chip.

Pin 109: GP24, Serial EEPROM Enable.

GP24: General Purpose I/O, input/output. See GPI/O Applications Section.
Serial EEPROM Enable: Connect to pin 1 of the 4x2 pin header which (if jumpered) connects to pin 1 of XL93C46 EEPROM chip.

Pin 110: GP25, 8042 P21.

GP25: General Purpose I/O, input/output. See GPI/O Applications Section.
8042 P21: 8042 P2.1, GATEA20, output.

Pin 111: RD0, GP60, Power LED Output.

RD0: ROM bus 0, input/output to the SD bus. Connect to pin 11 of L1130 ROM chip.
GP60: General Purpose I/O, input/output. See GPI/O Applications Section.
Power LED Output: Power LED output.

Pin 112: RD1, GP61, WDT.

RD1: ROM bus 1, input/output to the SD bus. Connect to pin 12 of L1130 ROM chip.
GP61: General Purpose I/O, input/output. See GPI/O Applications Section.
WDT: Watch dog timer, output.

Pin 113: RD2, GP62, 8042 P12.

RD2: ROM bus 2, input/output to the SD bus. Connect to pin 13 of L1130 ROM chip.
GP62: General Purpose I/O, input/output. See GPI/O Applications Section.
8042 P12: 8042 P1.2.

Pin 114: RD3, GP63, 8042 P13.

RD3: ROM bus 3, input/output to the SD bus. Connect to pin 15 of L1130 ROM chip.
GP63: General Purpose I/O, input/output. See GPI/O Applications Section.
8042 P13: 8042 P1.3.

Pin 115: RD4, GP64, 8042 P14.

RD4: ROM bus 4, input/output to the SD bus. Connect to pin 16 of L1130 ROM chip.
GP64: General Purpose I/O, input/output. See GPI/O Applications Section.
8042 P14: 8042 P1.4.

Pin 116: RD5, GP65, 8042 P15.

RD5: ROM bus 5, input/output to the SD bus. Connect to pin 17 of L1130 ROM chip.
GP65: General Purpose I/O, input/output. See GPI/O Applications Section.

8042 P15: 8042 P1.5

Pin 117: RD6, GP66, 8042 P16.
RD6: ROM bus 6, input/output to the SD bus. Connect to pin 18 of L1130 ROM chip.
GP66: General Purpose I/O, input/output. See GPI/O Applications Section.
8042 P16: 8042 P1.6

Pin 118: RD7, GP67, 8042 P17.
RD7: ROM bus 7, input/output to the SD bus. Connect to pin 19 of L1130 ROM chip.
GP67: General Purpose I/O, input/output. See GPI/O Applications Section.
8042 P17: 8042 P1.7

Pin 119: nROMCS, GP53.
nROMCS: ROM chip select, input. Connect to pin 20 of boot ROM chip (L1130) and pin 15 of boot ROM address buffer chip (L1027).
GP53: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 120: nROMOE, GP54, IR Mode, IRR3.
nROMOE: ROM output enable, input. Connect to pin 22 of boot ROM chip (L1130). Also connect to pin 9 of the ISA bus connector extension ISA C.
GP54: General Purpose I/O, input/output.
IR Mode: IR mode pin, output. This pin is used by Fast IR modules that require an input to set the receiver's bandwidth. (Used to control TEMIC Fast IR modules). See Application Note 5-17, "Multiple Footprint for FDC37C93X, FDC37C93XPM and FDC37C93XFR" for a description of the proper use of this pin for Fast IR.
IRR3: IR Receive 3, input. Fast IR receive data input. This pin is used by Fast IR modules that employ a second receive data output when high data rate (4Mbps) is used. (Used for HP Fast IR modules).

Pin 121: VBAT. Battery Voltage. Note: see Application Note 5-13 Rev 1.2, "Real Time Clock Considerations for SMC Ultra I/O Devices" for a description of the proper layout of the clock circuit. (There is no need for a 1 Meg resistor for this part.)

Pin 122: XTAL1. 32kHz crystal input, clock input. See note for Pin 121.

Pin 123: Ground. Battery Ground. See note for Pin 121.

Pin 124: XTAL2. 32kHz crystal output, clock output. See note for Pin 121.

Pin 125: Vcc

Pin 126: SLCT. Printer selected, input. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 13 of 25-pin parallel port connector.

Pin 127: PE. Paper end, input. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 12 of 25-pin parallel port connector.

Pin 128: BUSY. Busy signal, input. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 11 of 25-pin parallel port connector.

Pin 129: nACK. Acknowledge handshake, input. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 10 of 25-pin parallel port connector.

Pin 130: Ground.

Pin 131-138: PD7-PD0. Parallel port data bus, input/output. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pins 9-2 of 25-pin parallel port connector (through a 33Ω resistor).

Pin 139: Vcc

Pin 140: nSLCTIN. Printer select, output or open drain output. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 17 of 25-pin parallel port connector (through a 33Ω resistor).

Pin 141: nINIT. Initiate output, output or open drain output. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 16 of 25-pin parallel port connector (through a 33Ω resistor).

Pin 142: nERROR. Error at printer, input. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 15 of 25-pin parallel port connector.

Pin 143: nALF. Auto line feed, output or open drain output. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 14 of 25-pin parallel port connector (through a 33Ω resistor).

Pin 144: nSTB. Strobe signal, output or open drain output. See data sheet for alternate functions for EPP, ECP and FDC. Connect to pin 1 of 25-pin parallel port connector (through a 33Ω resistor).

Pin 145: RXD1. Receive serial data 1, input. Connect to pin 51 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 2 of the 9-pin COMM 1 connector.

Pin 146: TXD1. Transmit serial data 1, output. Connect to pin 54 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 3 of the 9-pin COMM 1 connector.

Pin 147: nDSR1. Data set ready 1, input. Connect to pin 52 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 6 of the 9-pin COMM 1 connector.

Pin 148: nRTS1. Request to send 1, output. Connect to pin 56 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 7 of the 9-pin COMM 1 connector.

Pin 149: nCTS1. Clear to send 1, input. Connect to pin 53 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 8 of the 9-pin COMM 1 connector.

Pin 150: nDTR1. Data terminal ready 1, output. Connect to pin 55 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 4 of the 9-pin COMM 1 connector.

Pin 151: nRI1. Ring indicator 1, input. Connect to pin 57 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 9 of the 9-pin COMM 1 connector.

Pin 152: nDCD1. Data carrier detect 1, input. Connect to pin 49 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 1 of the 9-pin COMM 1 connector.

Pin 153: nRI2, GP70.

nRI2: Ring indicator 2, input. Connect to pin 3 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 9 of the 5x2 pin COMM 2 header.

GP70: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 154: nDCD2, GP71.

nDCD2: Data carrier detect 2, input. Connect to pin 62 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 1 of the 5x2 pin COMM 2 header.
GP71: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 155: RXD2, GP72.

RXD2: Receive serial data 2, input. Connect to pin 63 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 2 of the 5x2 pin COMM 2 header. Also connect to pin 1 of IR Connector 1 to use for IR receive input, if desired.
GP72: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 156: TXD2, GP73.

TXD2: Transmit serial data 2, output. Connect to pin 59 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 3 of the 5x2 pin COMM 2 header. Also connect to pin 3 of IR Connector 1 to use for IR transmit output, if desired.
GP73: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 157: nDSR2, GP74.

nDSR2: Data set ready 2, input. Connect to pin 64 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 6 of the 5x2 pin COMM 2 header.
GP74: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 158: nRTS2, GP75.

nRTS2: Request to send 2, output. Connect to pin 61 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 7 of the 5x2 pin COMM 2 header.
GP75: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 159: nCTS2, GP76.

nCTS2: Clear to send 2, input. Connect to pin 1 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 8 of the 5x2 pin COMM 2 header.
GP76: General Purpose I/O, input/output. See GPI/O Applications Section.

Pin 160: nDTR2, GP77.

nDTR2: Data terminal ready 2, output. Connect to pin 60 of the SMC34C759 buffer chip. This signal is buffered through this chip to pin 4 of the 5x2 pin COMM 2 header.
GP77: General Purpose I/O, input/output. See GPI/O Applications Section.

Note 1: The 8584 ACCESS.bus controller chip and 24C02 ACCESS.bus EPROM is included on the FDC37C93XFR evaluation board for testing of the ACCESS.bus slave mode.

GPI/O Applications

This section outlines some of the applications for the GPI/O pins on the FDC37C93xFR. The GPI/O pins can be configured for many uses, including wake-up functions through the Group Interrupts. Functions such as Power LED, Watch Dog Timer (WDT), IR receive and transmit (IRRX and IRTX), General Purpose address decode or write strobe, Joystick read/write strobe, serial EEPROM interface, 8042 pins, nSMI, ACCESS.bus clock and data can be used through the alternate functions on some of the GPI/O pins (see Appendix A). In addition, IRQs can be mapped to any of the IRQ pins on the chip through GP10 and GP11 (IRQ in) or by enabling the GPI/Os to one of the group interrupts. These group interrupts can then be steered to any of the IRQ pins through the Group Interrupt Registers, GPINT1 and GPINT2, at 0xF0 and 0xEF of Logical Device 8. Note: GPINT is for any of the GPI/Os; GPINT2 is only for the GPI/Os GP4x - GP7x.

Some possible additional applications for the GPI/Os include I^2C or microwire interfaced A/D, D/A converter or pulse width modulator; I^2C EEPROM; software control of motherboard jumper settings or "open collector" switches (front panel controls); or card presence detect inputs.

In addition, the GPI/O pins can be configured for wake-up functions by enabling them onto one of the group interrupts. One example of this would be using a motion sensor, configured through a GPI/O pin enabled onto a group interrupt, to turn the PC on upon entering a room, and turning it off after some delay upon leaving the room.

Soft Power Management/Real-Time Clock Applications

This section outlines some of the applications for the FDC37C93xFR through the use of the soft power management and RTC features. Soft power management allows a variety of wakeup functions, including the Button_In pin, UART1,2 ring indicator pin, UART1,2 receive data pin, keyboard clock, mouse clock, IRRX2 pin, RTC alarm, RTC Alarm 2, and the group interrupt signals (GPINT1 and GPINT2). Soft power management also allows "user friendly" system shutdown through the software control of power off. In addition, by using the Button_In pin to power the entire system, a low cost power switch can be used (5V instead of 120V switch).

The enhanced RTC, along with the soft power management functions will allow the machine to be able to wakeup (i.e., turn itself on) at a predetermined time or once a minute, hour, day, week, month or year to do regular maintenance such as performing a tape back-up, or send out a fax when the telephone rates are the lowest and then shut itself off when it is finished.

The second alarm, alarm 2, provides another wakeup function to the system. Even if power is lost and the time that alarm 2 is set for has passed, the system will wakeup upon return of VTR if the alarm 2 enable bit is enabled.

Using the combined features of soft power management and the real-time clock, there are three ways to turn on the system: Manually, by pressing the button (through Button_In), through an event (wakeup function) or an alarm (enabled through the Soft Power Enable Registers). Using the features of soft power management, there are two ways to turn off the system: Manually, by pressing the button (through Button_In) or through software, by setting the SPOFF bit (bit 7 in the WDT_CTRL register).
Note that there is a programmable off-timer delay, programmed through the Delay 2 Time Set Register at 0xB8 in Logical Device 8. In addition, this delay can be extended or terminated via the Restart_Cnt and Stop_Cnt bits (Bits[6,7]) in the WDT_CTRL register.

There are two other bits in Soft Power Enable Register 2 that should be noted. Bit 7, OFF_EN, allows the software to enable or disable the button control of power off. Bit 6 allows the nPowerOn pin to be used as power good for the chip. If this bit is set (enabled), when nPowerOn goes inactive (float), all Super IO blocks and clocks are disabled, all outputs tristate and all inputs are high-z, except those for wakeup functions, which are still active.

Notes:
1. As most of the Soft Power Management Status Register bits are cleared by a read of these status registers, it is a good practice to read these registers upon power-up and prior to power-down. This will ensure that any enabled wakeup events have been cleared.
2. Any circuitry on the board that is to be used for a wakeup event must be run under VTR.

APPENDIX A

Multifunction Pins

Pin No.	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Buffer Type	Default	Index Register	GPI/O
19	MEDIA_ID1	GPI/O	IR Mode	IRR3	I/O8	float	GP4	GP40
20	MEDIA_ID0	GPI/O	-	-	I/O8	float	GP4	GP41
23	nIDE1_OE	GPI/O	-	-	I/O4	high	GP4	GP42
24	nHDCS0	GPI/O	-	-	I/O24	high	GP4	GP43
25	nHDCS1	GPI/O	-	-	I/O24	high	GP4	GP44
26	IDE1_IRQ	GPI/O	-	-	I/O8	float	GP4	GP45
30	nIOROP	GPI/O	Power LED Output	WDT	I/O24	float	GP4	GP46
31	nIOWOP	GPI/O	nSMI	-	I/O24	float	GP4	GP47
33	nPowerOn	GPI/O	-	-	I/O24	active low open collector output	GP5	GP51
34	Button_In	GPI/O	-	-	I/O24	input	GP5	GP50
111	RD0	GPI/O	Power LED Output	-	I/O4	RD0 (1) (4)	GP6	GP60
112	RD1	GPI/O	WDT	-	I/O4	RD1 (1) (4)	GP6	GP61
113	RD2	GPI/O	8042 - P12	-	I/O4	RD2 (1) (4)	GP6	GP62
114	RD3	GPI/O	8042 - P13	-	I/O4	RD3 (1) (4)	GP6	GP63
115	RD4	GPI/O	8042 - P14	-	I/O4	RD4 (1) (4)	GP6	GP64
116	RD5	GPI/O	8042 - P15	-	I/O4	RD5 (1) (4)	GP6	GP65
117	RD6	GPI/O	8042 - P16	-	I/O4	RD6 (1) (4)	GP6	GP66
118	RD7	GPI/O	8042 - P17	-	I/O4	RD7 (1) (4)	GP6	GP67
119	nROMCS	GPI/O	-	-	I/O8	nROMCS(1)	GP5	GP53
120	nROMOE	GPI/O	IR Mode	IRR3	I/O8	nROMOE(1)	GP5	GP54
153	nRI2	GPI/O	-	-	I/O8	input (2)	GP7	GP70
154	nDCD2	GPI/O	-	-	I/O8	input (2)	GP7	GP71
155	RXD2	GPI/O	-	-	I/O8	input (2)	GP7	GP72
156	TXD2	GPI/O	-	-	I/O8	input (2) (4)	GP7	GP73
157	nDSR2	GPI/O	-	-	I/O8	input (2)	GP7	GP74
158	nRTS2	GPI/O	-	-	I/O8	input (2) (4)	GP7	GP75
159	nCTS2	GPI/O	-	-	I/O8	input (2)	GP7	GP76
160	nDTR2	GPI/O	-	-	I/O8	input (2) (4)	GP7	GP77
27	nHDCS2	SA13	-	-	I/O24	float	-	-
28	nHDCS3	SA14	-	-	I/O24	float	-	-
29	IDE2_IRQ	SA15	-	-	I	float	-	-
53	nCS/SA12	-	-	-	I	input	-	-
96	GPI/O	IRQ in	-	-	I/O4	input	GP1	GP10
97	GPI/O	IRQ in	-	-	I/O4	input	GP1	GP11
98	GPI/O	WDT Timer Output/ IRRX	-	-	I/O4	input	GP1	GP12
99	GPI/O	Power LED Output/ IRTX	-	-	I/O24	input	GP1	GP13
100	GPI/O	GP Address Decode	-	-	I/O4	input	GP1	GP14

Pin No.	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Buffer Type	Default	Index Register	GPI/O
102	GPI/O	GP Write Strobe	-	-	I/O4	input	GP1	GP15
103	GPI/O	Joy Read Strobe	JOYCS	-	I/O4	input	GP1	GP16
104	GPI/O	Joy Write Strobe	-	-	I/O4	input	GP1	GP17
105	GPI/O	IDE2 Output Enable	8042 P20	-	I/O4	input	GP2	GP20
106	GPI/O	Serial EEPROM Data In	AB_DATA	-	I/O8 /OD8 (EN1)	input	GP2	GP21
107	GPI/O	Serial EEPROM Data Out	AB_CLK	-	I/O8 /OD8 (EN1)	input	GP2	GP22
108	GPI/O	Serial EEPROM Clock	-	-	I/O4	input	GP2	GP23
109	GPI/O	Serial EEPROM Enable	-	-	I/O4	input	GP2	GP24
110	GPI/O	8042 P21	-	-	I/O4	input	GP2	GP25