Data Book.

1985

Synertek.

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Numerical Index

Cell Library. 1

SSI/MSI

Cell Identifier	Description	Area (sq. μm)
BAM00000	Inverter	1.1K
BAM00001	Inverter/Buffer	1.6K
BAM00002	Inverter/Buffer	3.2K
BAM00003	Inverter/Buffer	9.1K
BAM00004	3-State Inverter/Buffer	2.1K
BAM00005	Slow Inverter for Pulse Generator	3.2K
BAM00006	TTL Compatible Inverter/Buffer	3.2K
BAM00007	3-State Inverter/Buffer	4.3K
BAM00008	3-State Inverter/Buffer	2.1K
BAM00009	Non-Inverting TTL Compatible Buffer	TBD
BAM00010	2-In NAND	1.6K
BAM00011	3-In NAND	2.1K
BAM00012	4-In NAND	2.7K
BAM00013	5-In NAND	3.2K
BAM00014	6-In NAND	3.7K
BAM00015	7-In NAND	4.3K
BAM00016	8-In NAND	4.8K
BAM00020	2-In NOR	1.6K
BAM00021	3-In NOR	2.7K
BAM00022	4-In NOR	2.7K
BAM00023	5-In NOR	3.7K
BAM00024	6-In NOR	3.7K
BAM00025	7-In NOR	4.3K
BAM00026	8-In NOR	4.8K
BAM00030	2-In AND	2.1K
BAM00031	3-In AND	2.7K
BAM00032	4-In AND	3.2K
BAM00033	5-In AND	3.7K
BAM00034	6-In AND	4.3K
BAM00035	7-In AND	4.8K
BAM00036	8-In AND	5.3K
BAM00040	2-In OR	2.2K
BAM00041	3-In OR	2.7K
BAM00042	4-In OR	3.2K
BAM00043	5-In OR	4.3K
BAM00044	6-In OR	4.3K
BAM00045	7-In OR	4.8K
BAM00046	8-In OR	5.3K
BAM00050	XOR	2.7K
BAM00051	XNOR	2.7K
BAM00055	P-Channel Pull-up Transistor	1.1K
BAM00056	N-Channel Pull-down Transistor	1.1K
BAM00060	2,2 AND-NOR	2.7K
BAM00061	2,1 AND-NOR	2.1K
BAM00062	2,2 OR—NAND	2.7K

SSI/MSI (cont.)

Cell Identifier	Description	Area (sq. μm)
BAM00063	2,1 OR-NAND	2.3K
BAM00070	Transmission Gate	2.1K
BAM00071	Transmission Gate with Enable Inverter	2.1K
BAM00072	2-to-1 Mux	2.7K
BAM00073	4-to-1 Mux	2.7K
BAM00074	8-to-1 Mux	27.3K
BAM00076	Mux Driver for BAM00072	2.1K
BAM00077	Mux Decoder/Driver for BAM00073	20.3K
BAM00078	Mux Decoder/Driver for BAM00074	52K
BAM00080	D-Latch without Reset	3.7K
BAM00081	D-Latch with Reset	4.3K
BAM00082	D/FF with Reset	13.9K
BAM00083	D/FF with Reset	8.5K
BAM00084	D/FF with Set/Reset	9.1K
BAM00086	T/FF with Reset	12.8K
BAM00087	T/FF with Reset	8.5K
BAM00088	T/FF with Set/Reset	11.7K
BAM00089	T/FF with Set/Reset	9.6K
BAM00090	J-K/FF with Set/Reset	17.1K
BAM00091	J-K/FF with Set/Reset	14.9K
BAM00092	Set/Reset Latch	2.7K
BAM00093	Shift Register Front-end	8.5K
BAM00094	Parallel Load Shift Register	12.8K
BAM00095	D-Latch with 3-State O/P	11.7K
BAM00096	D-Latch with 3-State O/P	7.5K
BAM00097	BAM00095/96 with Data Select I/P	22.4K
BAM00098	BAM00095/96 with Data Select I/P	12.8K
BAM00099	Look-ahead Carry Counter	TBD
BAM00100	Look-ahead Carry Counter	TBD
BAM00101	Look-ahead Carry/Borrow Up/Down Counter	TBD
BAM00102	Look-ahead Carry/Borrow Up/Down Counter	TBD
BAM00103	D/FF without Reset	6.4K
BAM00104	D/FF with Reset	8.5K
BAM00105	Binary Adder	16.0K
BAM00106	Synchronous Clock Gate	TBD
BAM00107	Data Synchronizer	TBD
BAM00108	Serial In/Out Shift Register	10.1K
BAM00109	Serial In/Out Shift Register	10.1K
BAM00110	Serial In/Out Shift Register	10.1K
BAM00200	Power-on Reset Generator	14.4K
BAM00210	Pull-up Load	1.6K
BAM00220	Pull-down Load	1.6K
BAM00230	Capacitor to Ground	4.3K
BAM00300	Internal Schmitt Trigger	4.7K

SSI/MSI (cont.)

Cell Identifier	Description	Area (sq. μm)
BAM00800	V_{SS} Pad	44.3K
BAM00801	V_{SS} Pad	73K
BAM00810	V_{DD} Pad	44.3K
BAM00811	V_{DD} Pad	73K
BAM00820	TTL/CMOS O/P Driver	153K
BAM00822	TTL/CMOS O/P Driver	76.4K
BAM00823	TTL/CMOS O/P Driver	113K
BAM00824	Versatile O/P Pad Driver	136K
BAM00830	TTL/CMOS 3-State O/P Driver	153K
BAM00832	TTL/CMOS 3-State O/P Driver	129K
BAM00840	Open-Drain O/P Driver	93K
BAM00841	Open-Drain O/P Driver	73K
BAM00845	Open-Drain O/P Driver	50K
BAM00846	Open-Drain O/P Driver	73K
BAM00850	TTL Compatible I/P Buffer	77K
BAM00851	TTL Compatible I/P Buffer	73K
BAM00860	Schmitt Trigger I/P Buffer	101K
BAM00861	Schmitt Trigger I/P Buffer	96K
BAM00870	Fast TTL Compatible I/P Latch	89K
BAM00880	I/P Pad with Protection Device	75K
BAM00881	I/P Pad with Protection Device	73K
BAM00890	Open-Drain Driver with Pull-up	137K
BAM00891	LED Driver	239K
BAM00900	Input Pad with Pull-up	78.3K
BAM00901	Input Pad with Pull-up	TBD
BAM00910	I/O Pad with Open-Drain O/P	79K
BAM00911	I/O Pad with Open-Drain O/P	136K
BAM00920	O/P Driver Pad for Clock Osc	109K
BAM00921	Crystal Osc with Pads	143K
BAM00923	O/P Driver Pad for Clock Osc	126.2K
BAM00930	I/O Pad with 3-State O/P	185K
BAM00932	I/O Pad with 3-State O/P	144.4K
BAMVDD	V_{DD} Connection Cell	1.1K
BAMGND	GND Connection Cell	1.1K

SSI/MSI High-Speed Cells

Cell Identifier	Function	Area (sq. μm)
BAM02001	Inverter/Buffer	1.6K
BAM02002	Inverter/Buffer	3.2K
BAM02003	Inverter/Buffer	9.1K
BAM02004	3-State Inverter/Buffer	2.1K
BAM02007	3-State Inverter/Buffer	4.3K
BAM02008	3-State Inverter/Buffer	2.1K
BAM02010	2-In NAND	2.1K
BAM02011	3-In NAND	2.7K
BAM02012	4-In NAND	5.4K
BAM02013	5-In NAND	TBD
BAM02014	6-In NAND	4.3K
BAM02020	2-In NOR	TBD
BAM02021	3-In NOR	TBD
BAM02022	4-In NOR	3.2K
BAM02023	5-In NOR	5.9K
BAM02024	6-In NOR	7.5K
BAM02030	2-In AND	TBD
BAM02031	3-In AND	TBD
BAM02032	4-In AND/NAND	5.9K
BAM02040	2-In OR/NOR	4.3K
BAM02041	3-In OR/NOR	6.4K
BAM02042	4-In OR/NOR	8.0K
BAM02050	XOR	3.7K
BAM02051	XNOR	3.7K
BAM02060	2,2 AND-NOR	3.2K
BAM02061	2,1 AND-NOR	2.7K
BAM02062	2,2 OR-NAND	3.2K
BAM02063	2,1 OR-NAND	2.7K
BAM02070	Transmission Gate	2.1K
BAM02080	D-Latch, Transparent	5.4K
BAM02082	D/FF with Reset	17.1K
BAM02083	D/FF with Reset	11.7K
BAM02084	D/FF with Set/Reset	20.3K
BAM02085	D/FF with Set/Reset	20.3K
BAM02086	T/FF with Reset	18.1K
BAM02087	T/FF with Reset	18.1K
BAM02088	T/FF with Set/Reset	20.3K
BAM02089	T/FF with Set/Reset	20.3K
BAM02092	SR-Latch	3.7K
BAM02093	Shift Register	8.5K
BAM02094	Shift Register	8.5K
BAM02110	D-Latch with Reset	9.1K
BAM02111	D-Latch with Reset	9.1K

MSI Cells

Cell Identifier	Function	Area (sq. μm)
BAM04160	4-Bit Decade Counter (74160)	TBD
BAM04161	4-Bit Binary Counter (74161)	TBD
BAM04162	4-Bit Decade Counter (74162)	TBD
BAM04163	4-Bit Binary Counter (74163)	TBD

MSI Schematic Macros

Cell Identifier	Function	Area (sq. μm)
BAM74042	BCD-to-Decimal Decoder	35.2K
BAM74083	4-Bit Full Adder with Carry Look-Ahead	79K
BAM74085	4-Bit Magnitude Comparator	74.2K
BAM74090	4-Bit Decade Counter	56K
BAM74093	4-Bit Binary Counter	66.7K
BAM74138	3-to-8 Line Decoder	48K
BAM74151	8-to-1 Multiplexer	82.8K
BAM74153	4-to-1 Multiplexer	32K
BAM74157	Quad 2-to-1 Multiplexers	22.4K
BAM74160	4-Bit Decade Counter	112.1K
BAM74161	4-Bit Binary Counter	110.4K
BAM74162	4-Bit Decade Counter	120.6K
BAM74163	4-Bit Binary Counter	115.8K
BAM74164	8-Bit Serial-In/Parallel-Out Shift Register	95K
BAM74165	8-Bit Parallel-In/Serial-Out Shift Register	172.4K
BAM74182	4-Bit Look-Ahead Generator	53.9K
BAM74192	4-Bit Decade Up/Down Counter	121.9K
BAM74193	4-Bit Binary Up/Down Counter	121.7K
BAM74280	9-Bit Odd/Even Parity Generator	68.8K
BAM76610	7-Bit Universal Asynchronous Transmitter	330.8K
BAM76611	7-Bit Universal Asynchronous Receiver	331.2K

Memory Cells

Cell Identifier	Function	Area (sq. μm)
BAM6010	8 x 8 Static RAM	380K
BAM6140	64 x 4 Static ROM	227K
BAM6141	64 x 8 Static ROM	278K
BAM6142	64 x 12 Static ROM	325K

Analog Cells

	Area (sq. μm)
*Operational Amplifier	TBD
*Voltage Comparator	TBD
*8-Bit A/D Converter	TBD
*8-Bit D/A Converter	TBD
*Voltage Regulator	TBD
*Voltage Reference	TBD
*Analog Switch (Pad Cell)	TBD
*3-State Input (Pad Cell)	TBD

Microprocessor Core

	Area (sq. μm)
*6502 Core Microprocessor	TBD
*BAM06610 UART (Transmitter Section)	TBD
*BAM06611 UART (Receiver Section)	TBD

To receive Synertek's Cell Library Data Book, call or write your local sales office from listing in back of this book.

*Available 4Q'84

TTL Cross Reference

TTL Equivalent	Cell Identifier	Function	Comment
7400	BAM00010	2-Input NAND	
7400	BAM02010	Fast 2-Input NOR	
7402	BAM00020	2-Input NOR	
7404	BAM00000	Inverter	
7404	BAM00001-3	Inverter/Buffer	
7404	BAM00006	TTL-Compatible Buffer	Functional Equivalent
7408	BAM00030	2-Input AND	
7410	BAM00011	3-Input NAND	
7410	BAM02011	Fast 3-Input NAND	
7411	BAM00031	3-Input AND	
7420	BAM00012	4-Input NAND	
7421	BAM00032	4-Input AND	
7425	BAM00022	3-Input NOR	
7427	BAM00021	3-Input NOR	
7432	BAM00040	2-Input OR	
7442	BAM74042	BCD-Decimal Decoder	
7451	BAM00060	2,2 AND-NOR	
7474	BAM00084	D Flip-Flop with Set-Reset	
7483	BAM00105	Binary Adder	
7483	BAM74083	4-Bit Full Adder	
7485	BAM74085	4-Bit Magnitude Comparator	
7486	BAM00050	Exclusive-OR	
7490	BAM74090	4-Bit Decade Counter	
7493	BAM74093	4-Bit Binary Counter	
7496	BAM00093/94	Parallel-Load Shift Register	Cell without Clear
74107	BAM00090/91	J-K Flip-Flop with Set/Reset	
74125	BAM00004,7,8	3-State Inverter/Buffer	
74138	BAM00078	3-to-8 Line Decoder	
74138	BAM74138	3-to-8 Decoder	
74151	BAM74151	1-of-8 Data Selector	
74152	BAM00074+78	8-to-1 Multiplexer	
74153	BAM00073+77	4-to-1 Multiplexer	Cell without Strobe
74153	BAM74153	1-of-4 Data Selector	
74155	BAM00077	2-to-4 Line Decoder	Cell without Strobe
74157	BAM00072+76	2-to-1 Multiplexer	Cell without Strobe
74157	BAM74157	1-of-2 Data Selector	
74160	BAM74160	4-Bit Decade Counter	
74161	BAM74161	4-Bit Binary Counter	
74162	BAM74162	4-Bit Decade Counter	
74163	BAM00099/100	Look-Ahead Carry Counter	Cell without Count Enable

TTL Cross Reference (cont.)

TTL Equivalent	Cell Identifier	Function	Comment
74163	BAM74163	4-Bit Binary Binary Counter	
74164	BAM74164	8-Bit Serial-In Shift Register	
74165	BAM74165	8-Bit Serial-In Shift Register	
74182	BAM74182	Look-Ahead Carry Generator	
74192	BAM74192	Syncr Up/Down 4-Bit Counter	
74193	BAM00101/102	Look-Ahead Up/Down Counter	
74193	BAM74193	Syncr Up/Down 4-Bit Counter	
74260	BAM00023	5-Input NOR	
74266	BAM00051	Exclusive-NOR	
74279	BAM00092	Set-Reset Latch	
74280	BAM74280	9-Bit Odd/Even Parity Generator	
74363	BAM00095/96	Transparent D-Latch with 3-State	
74373	BAM00080	D-Latch without Reset	Cell without 3-State and Enable
74373	BAM02080	Fast D-Type Flip-Flop	Cell without 3-State and Enable

CMOS Cross Reference

CMOS Equivalent	Cell Identifier	Function	Comment
4001	BAM00020	2-Input NOR	
4002	BAM00022	4-Input NOR	
4008	BAM00105	Binary Adder	
4011	BAM00010	2-Input NAND	
4011	BAM02010	Fast 2-Input NAND	Functional Equivalent
4012	BAM00012	4-Input NAND	
4013	BAM00084	D Flip-Flop with Set/Reset	
4020	BAM00086/87	T Flip-Flop with Reset	
4021	BAM00093/94	Parallel-Load Shift Register	
4023	BAM00011	3-Input NAND	
4023	BAM02011	Fast 3-Input NAND	Functional Equivalent
4025	BAM00021	3-Input NOR	
4027	BAM00090/91	J-K Flip-Flop with Set/Reset	
4029	BAM00101/102	Look-Ahead Up/Down Counter	Cell has only Binary-Count
4042	BAM00080	D-Latch without Reset	Cell without Clock Polarity Select
4042	BAM02080	D-Latch, Transparent, High Speed	Cell without Clock Polarity Select
4044	BAM00092	Set-Reset Latch	Cell without 3-State
4049	BAM00001-3	Inverter/Buffer	
4049	BAM00006	TTL-Compatible Buffer	
4051	BAM00074+75	8-to-1 Multiplexer	Cell without Inhibit
4052	BAM00073+77	4-to-1 Multiplexer	Cell without Inhibit
4053	BAM00072+76	2-to-1 Multiplexer	Cell without Inhibit
4069	BAM00000	Inverter	
4070	BAM00050	Exclusive-OR	
4071	BAM00040	2-Input OR	
4072	BAM00042	4-Input OR	
4073	BAM00031	3-Input AND	
4075	BAM00041	3-Input OR	
4077	BAM00051	Exclusive-NOR	
4081	BAM00030	2-Input AND	
4082	BAM00032	4-Input AND	
4085	BAM00060	2,2 AND-NOR	Cell without Inhibit
4502	BAM00004,7,8	3-State Inverter/Buffer	Cell without Inhibit
4555	BAM00077	2-to-4 Line Decoder	Cell without Enable
40161	BAM00099/100	Look-Ahead Carry Counter	
40174	BAM00082/83	D Flip-Flop with Reset	

I. General Description

The Synertek Cell Library combines the dense layout characteristics of the HCMOS process technology with the automation achieved by standard cell system design. The cells adhere to a well-defined set of design and layout structure rules, thereby relieving the chip designer of the burden of electrical and physical considerations and permitting a focus on system and logic design efforts.

In general, the cells utilize a constant height and a variable width and allow for placement adjacent to each other in the horizontal direction The structure rules are compatible with standard CAD interactive layout software by including feedthroughs on all inputs and outputs, and by accounting for power connections by cell abutment. Interactive layout systems can utilize the supplied physical outlines for each cell to minimize layout data. In some cases, individual cells may have a non-standard height or may not have feedthroughs for all inputs and outputs in order to achieve a higher level of packing density.

The HCMOS Cell Library incorporates this structured approach to provide fundamental logic functions for high speed, low power applications

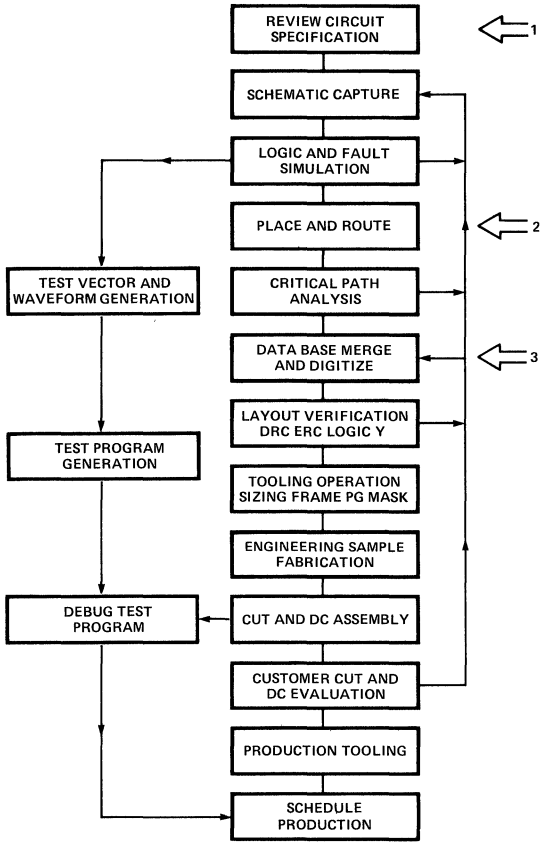
The Synertek Cell Library

The Synertek Cell Library currently contains approximately 200 cells. These consist of gates, inverters, multiplexers, flip-flops, shift registers, counters, adders, I/O circuits (pad cells), and LSI type functions, such as RAMs and ROMs. Also included are analog functions which permit direct interfacing to analog signal environments (OP AMPs, Comparators, etc.). Finally, a complete set of high-speed cells is also available for those applications that need faster operation (at the expense of somewhat larger cells). With this library of cells to select from, nearly any conceivable circuit may be constructed and designed in a very quick and low cost fashion.

Hardware

Synertek uses a VAX based system to implement its Standard Cell Library approach to semi-custom design. The Library of cells resides on the computer and is accessed via Genisco and Tektronix graphics terminals for the schematic capture and place and route design states. Alphanumeric terminals can also be used for the Data Base access required during netlist extraction and simulation. Digitizing and layout of new cells is achieved on Calma graphics systems as is the merging of the cell structures into the design. The Synertek Cell Library will be ported over to a range of popular workstations and is already available on the Silvar Lisco and Daisy systems.

Design Flow



Software

Synertek's comprehensive family of software packages provides the customer with a "thoroughly checked to specification product" laid out in a state of the art process by the best router available. These user friendly packages cover schematic capture, logic and circuit simulation through to 100% place and route and a complete range of error checking.

Customer Interfaces

Three levels of sophistication in interfacing with Synertek are open to the Cell Library designer. This allows him to do as little or as much of the chip design as he chooses.

Level 1:
The customer provides Synertek's engineering staff with a schematic diagram of the design along with a comprehensive specification Synertek engineers then enter the design into the computer, extract the netlist and logically simulate it before placement and routing. Critical path analysis is then carried out to ensure that the layout meets the timing specification. After the cell structures have been merged with the design, Electrical Rule and Design Rule checks are made. The final check compares the layout with the original netlist. After PG tape and tooling generation, engineering samples are run off and cut and go's given back to the customer for evaluation. Test program generation occurs in parallel with the data base development so as to be ready for the final phase of the design program production scheduling.

Synertek offers all of the training necessary for the first time Cell Library designer to develop his design at one of the six demonstration centers maintained throughout the country.

Level 2:
This level allows the customer to develop his netlist on a workstation and provide it to Synertek in either the simulated or unsimulated form. Synertek then takes the design through the rest of the development described in Level 1

Level 3:
The most sophisticated interface level, Level 3 provides for a customer who has a place and route capability either on his VAX or workstation. He gives his data base tape to Synertek who merges the cells and creates the PG tape for the mask vendor.

Electrical Requirements

A. Absolute Maximum Ratings:

Parameter	Value
Power Supply (V_{DD})	+6 V
Input Voltage	−0 3 V to V_{DD} + 0 3 V
Output Voltage	−0 3 V to V_{DD} + 0 3 V
Temperature	−55 to +150° C

B. Maximum Operating Conditions:

Parameter	Value
Power Supply (V_{DD})	2 0 V to 6 0 V
Input Voltage	0 V to V_{DD}
Output Voltage	0 V to V_{DD}
Temperature	−55 to +125° C

C. Recommended Operating Conditions:

Parameter	Value
Power Supply (V_{DD})	5 0 V ± 10%
Temperature	−55 to +125° C

D. Nominal Conditions:

Parameter	Value
Power Supply (V_{DD})	5 0 V
Temperature	25° C

II. Physical Specifications

A. Cell Height: 69.3, and 98.7 μm.

B. Cell Width: Increments of 7 7 μm

C. Power: 5.6 μm metal lines horizontally routed through each cell.

D. Metal Interconnections: 2 8 μm width, 3 5 μm spacing.

E. Polysilicon Interconnections: 2 1 μm width, 2 5 μm spacing.

Electrical Specifications for Individual Cells

A. Propagation Delay

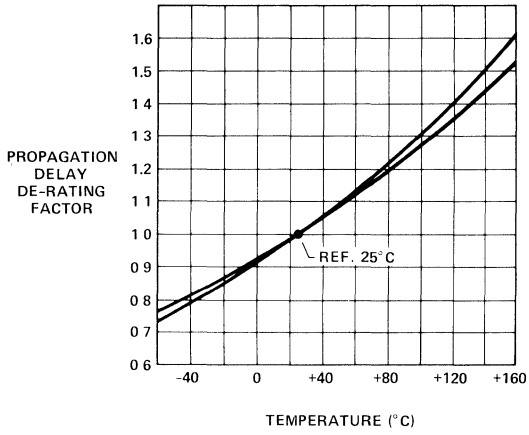
The output propagation delay for each cell is indicated in the individual cell data sheet. Both low-to-high and high-to-low transitions are specified. Delays are consistently measured at the 50% points. Individual cell propagation delays are specified as a function of the cell output load capacitance, C_L, in pF. Further, the equation is valid at nominal conditions, only (V_{DD} = 5.0 V, T = 25° C, nominal process). Actual delays at other than nominal conditions are determined by utilizing derating factors, as shown below:

(t_{PD}) actual = (t_{PD}) nominal • (X_1) • (X_2) • (X_3)

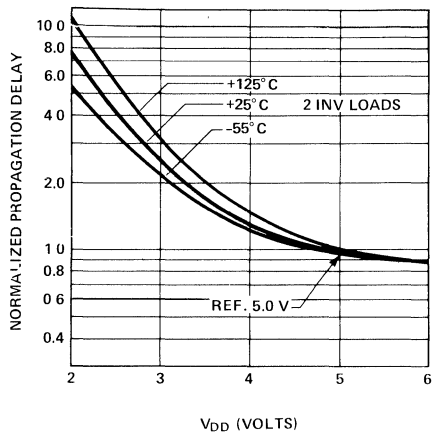
X_1 = derating factor for temperature.
X_2 = derating factor for V_{DD}
X_3 = derating factor for process variations.

The derating factors for temperature and V_{DD} level are taken from the following curves.

PROPAGATION DELAY DE-RATING FACTOR VS TEMPERATURE



PROPAGATION DELAY VS V_{DD}



The derating factor for process variation is taken from the following table:

Process	Derating Factor
Worst Cast	1.50
Nominal	1.00
Best Case	0.65

B. Power Dissipation

There are two components of power dissipation in the HCMOS Cell Library cells. The first component is the static or DC power and consists of three effects:

- Internal leakage paths between V_{DD} and V_{SS}. In most cases, the currents are less than 1 nA, but sometimes they can be as high as 1 μA
- Output loads. Output loads (resistive elements with a current path to ground) require substantial currents when they are driven.
- TTL input level effects. Inputs to the TTL-compatible Input Buffer cell may cause significant power drain This results from both the pull-up and the pull-down devices being simultaneously conducting when an input level below V_{DD} and above V_{SS} is applied The data sheet for this cell shows this effect quantitatively

The second component of power dissipation is the transient or AC power and consists of three parts

- Internal capacitance charging. Whenever internal levels change state from low to high levels, energy is required to charge the node capacitance This occurs only at the time of transition and is a function of the amount of node capacitance and the V_{DD} level
- Output load capacitance. When external levels change state from low to high, energy is also required for charging. In this case, however, node capacitance is typically orders of magnitude higher than internal nodes and consequently, power dissipation effects can be quite substantial
- Transitional push/pull currents Internal cells will experience current paths between V_{DD} and V_{SS} when undergoing a high-to-low or low-to-high transition. This occurs for very short periods when both the p-channel and n-channel transistors simultaneously conduct

The data sheets for each cell indicate the cell power dissipation for internal node capacitance charging and for transitional push/pull currents Output loads, TTL input level effects, and output load capacitance must be accounted for additionally Internal leakage paths will not exceed 1 μA in total and hence, can usually be neglected

Cell data sheets indicate power dissipation at fixed loading (usually 0.050 pF) and at nominal operating conditions. Note that the power is given in units of μW/MHz In this way, the frequency of edge transitions directly effects power and can be readily calculated.

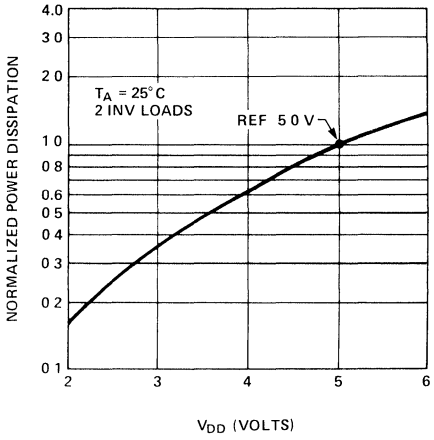
In a like fashion, additional loading (greater than 0.050 pF) increases power dissipation according to the following relation

$$P_{DISS} = P_{DISS}\ \text{nominal} + 25\ (C_L - 0.050)$$

where,

P_{DISS} nominal = Nominal Power Dissipation (from data sheet)
C_L = Load Capacitance on Node (pF)

POWER DISSIPATION VS. V_{DD}



By this relation, power dissipation at any particular loading condition may be calculated. Further, the effect of V_{DD} on power dissipation needs to be determined for situations that call for V_{DD} levels other than nominal (V_{DD} = 5.0 V). For this, the above curve is used.

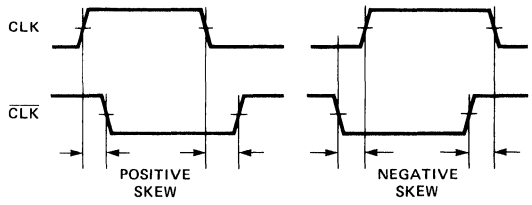
Finally, it should be noted that temperature and process variations have no substantial effects on power dissipation.

C. Other Timings

There are other timing parameters sometimes specified besides propagation delay Some examples are pulse widths, clock rates, set-up and hold times, and three-state turn-on and turn-off delays For these parameters, the same derating factors are used as for propagation delays, unless otherwise noted

D. Clock Skews

Many cells require complementary clock input signals Some examples are latches, flip-flops, and shift registers. For these cells, some degree of clock skew is permitted, as shown below:



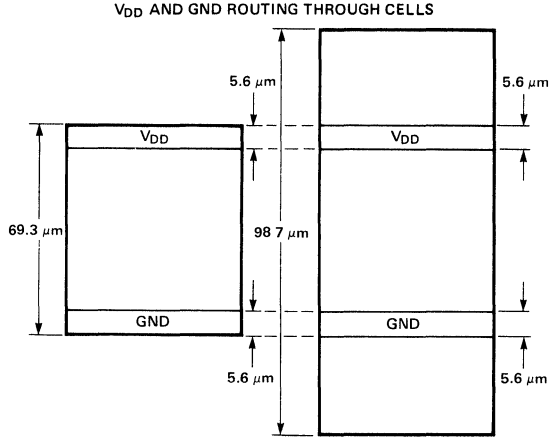
The maximum tolerable clock skew at nominal conditions (V_{DD} = 5.0 V, T = 25°C, nominal process parameters) is ± 10 nsec. Skew effects get worse as V_{DD} goes higher, T goes lower, and as the process parameters increase the speed of the MOS transistors. In short, unless otherwise indicated, maximum tolerable clock skew at the worst-case conditions may not exceed ± 5 nsec. This is not as bad as it seems, however, since clock drivers get faster as the conditions for worst-case skew are approached, a self-compensating situation. Thus, if the nominal condition is met (± 10 nsec), then the worst-case condition will be met as well.

III. Cell Structures

A. Power and Ground Connections Through Cells

V_{DD} and GND connections are routed through rows of cells by means of cell abutment. Both V_{DD} and GND (V_{SS}) are bussed through the cells in the horizontal direction by 5.6 μm wide metal lines. The following diagram illustrates the bussing for both 69.3 and 98.7 μm

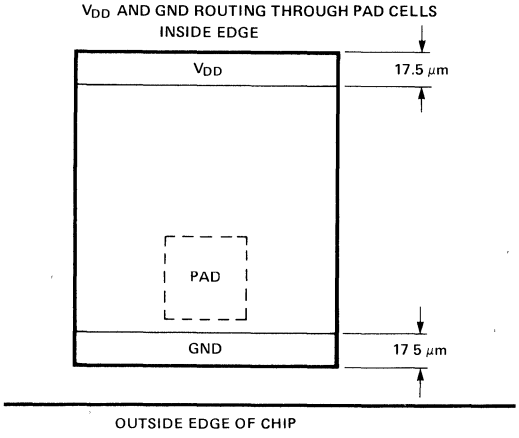
V_{DD} AND GND ROUTING THROUGH CELLS



Note that the busses will be routed through a row of cells, even when cell heights are mixed, providing that the cells are centered the same. Connections to V_{DD} and GND can be made at the ends of the cell rows. This may be done either automatically (if the router software is capable) or by manual edits.

B. Power and Ground Connections in Pad Cells

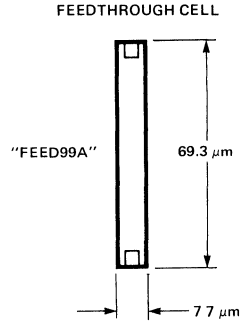
The same principle applies for pad cells as for internal cells, as diagrammed below.



Connections between adjacent cells for V_{DD} and GND are made by means of cell abutment. However, one difference exists for pad cells. That difference is that pad cells with different heights still have V_{DD} and GND busses on the top and bottom of the cell. This means that, if cells of different heights are used, a gap must be provided between the cells and the V_{DD} and GND busses must be entered manually. In addition, the V_{DD} and GND busses have standard widths of 17.5 μm (5.6 μm is the bus width for internal cells).

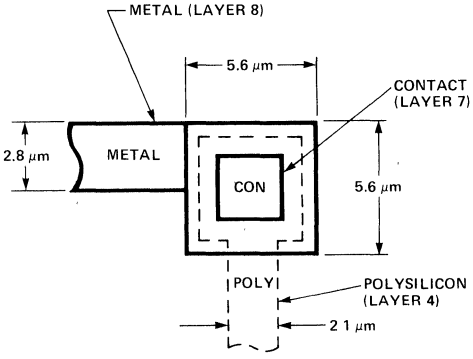
C. Feedthrough Cell

A feedthrough cell is required by most router software packages to permit routing a connection through a row of contiguous cells to some point beyond. To achieve this, a feedthrough cell is used, whose outline drawing is shown below.



D. Contacts

Connections between metal and polysilicon lines are achieved by means of contacts. The following figure illustrates the required dimensions of the contact.



The polysilicon stripes (lines) are 2.1 microns wide and the metal lines are 2.8 microns wide. The size of both the metal and polysilicon contact coverage is 5.6 x 5.6 microns. The contact opening is 2.8 x 2.8 microns. The layer numbers are indicated on the figure.

Memories.

2

RAM Selection Guide

Commercial $T_A = 0°C$ to $70°C$)

Part Number	Organization	Access Time (ns)	Maximum Current (mA)		Power Supply (Volts)	Number of Pins	Package Type (Note 1)	Page No.
			Operating	Standby				
SY2148H	1024 x 4	70	150	30	+5	18	P	2-39
SY2148H-2	1024 x 4	45	150	30	+5	18	P	2-39
SY2148H-3	1024 x 4	55	150	30	+5	18	P	2-39
SY2148HL	1024 x 4	70	125	20	+5	18	P	2-39
SY2148HL-3	1024 x 4	55	125	20	+5	18	P	2-39
SY2149H	1024 x 4	70	150	--	+5	18	P	2-43
SY2149H-2	1024 x 4	45	150	--	+5	18	P	2-43
SY2149H-3	1024 x 4	55	150	--	+5	18	P	2-43
SY2149HL	1024 x 4	70	125	--	+5	18	P	2-43
SY2149HL-3	1024 x 4	55	125	--	+5	18	P	2-43
SY2147H-2	4096 x 1	45	180	30	+5	18	P	2-35
SY2147H-3	4096 x 1	55	180	30	+5	18	P	2-35
SY2147H	4096 x 1	70	160	20	+5	18	P	2-35
SY2147HL-3	4096 x 1	55	125	15	+5	18	P	2-35
SY2147HL	4096 x 1	70	140	15	+5	18	P	2-35
SY2150	512 x 9	45	132	—	+5	24	C	2-47
SY2132-1	512 x 8[6]	100	170	40/110[5]	+5	48	C, P	2-24
SY2132-2	512 x 8[6]	120	170	40/110[5]	+5	48	C, P	2-24
SY2132-3	512 x 8[6]	150	170	40/110[5]	+5	48	C, P	2-24
SY2132-4	512 x 8[6]	200	170	40/110[5]	+5	48	C, P	2-24
SY2133-1	512 x 8[6]	100	170	N A [4]	+5	48	C, P	2-24
SY2133-2	512 x 8[6]	120	170	N A [4]	+5	48	C, P	2-24
SY2133-3	512 x 8[6]	150	170	N A [4]	+5	48	C, P	2-24
SY2133-4	512 x 8[6]	200	170	N A [4]	+5	48	C, P	2-24
SY2130-1	1024 x 4[6]	100	170	40/110[5]	+5	48	C, P	2-13
SY2130-2	1024 x 4[6]	120	170	40/110[5]	+5	48	C, P	2-13
SY2130-3	1024 x 4[6]	150	170	40/110[5]	+5	48	C, P	2-13
SY2130-4	1024 x 4[6]	200	170	40/110[5]	+5	48	C, P	2-13
SY2131-1	1024 x 4[6]	100	170	N A [4]	+5	48	C, P	2-13
SY2131-2	1024 x 4[6]	120	170	N A [4]	+5	48	C, P	2-13
SY2131-3	1024 x 4[6]	150	170	N A [4]	+5	48	C, P	2-13
SY2131-4	1024 x 4[6]	200	170	N A [4]	+5	48	C, P	2-13
SY2158-2	1024 x 8	120	100	30	+5	24	P	2-48
SY2158-3	1024 x 8	150	100	30	+5	24	P	2-48
SY2158-4	1024 x 8	200	100	30	+5	24	P	2-48
SY2128-1	2048 x 8	100	100	20	+5	24	P	2-9
SY2128-2	2048 x 8	120	100	20	+5	24	P	2-9
SY2128-3	2048 x 8	150	100	20	+5	24	P	2-9
SY2128-4	2048 x 8	200	100	20	+5	24	P	2-9
SY2128L-2	2048 x 8	120	80	15	+5	24	P	2-9
SY2128L-3	2048 x 8	150	80	15	+5	24	P	2-9
SY2128L-4	2048 x 8	200	80	15	+5	24	P	2-9
SY2168-70[2]	4096 x 4	70	120	30	+5	20	P	2-56
SY2168-55	4096 x 4	55	120	30	+5	20	P	2-56
SY2168-45	4096 x 4	45	120	30	+5	20	P	2-56
SY2169-70[2]	4096 x 4	70	120	--	+5	20	P	2-60
SY2169-55	4096 x 4	55	120	--	+5	20	P	2-60
SY2169-45	4096 x 4	45	120	30	+5	20	P	2-60
SY2167-70	16,384 x 1	70	120	30	+5	20	P	2-52
SY2167-55	16,384 x 1	55	120	30	+5	20	P	2-52
SY2167-45	16,384 x 1	45	120	30	+5	20	P	2-52

NOTES:
1 P = Molded DIP, C = Ceramic
2 Preliminary Information

ROM Selection Guide

Part Number	Organization	Access Time (ns) Max	Maximum Current (mA)		Power Supply (Volts)	Number of Pins	Package Type	Compatible EPROM/ PROM	Page No
			Operating	Standby					
SY2316B	2048 x 8	450	98	—	+5	24	P	2716	2-67
SY2316B-2	2048 x 8	200	98	—	+5	24	P	2716	2-67
SY2316B-3	2048 x 8	300	98	—	+5	24	P	2716	2-67
SYM2332	4096 x 8	450	100	—	+5	24	P	TMS2532	2-70
SY2332-2	4096 x 8	200	100	—	+5	24	P	TMS2532	2-70
SY2332-3	4096 x 8	300	100	—	+5	24	P	TMS2532	2-70
SY2333	4096 x 8	450	100	—	+5	24	P	2732/A	2-70
SY2333-2	4096 x 8	200	100	—	+5	24	P	2732/A	2-70
SY2333-3	4096 x 8	300	100	—	+5	24	P	2732/A	2-70
SY2364	8192 x 8	450	100	—	+5	24	P	TMS2564	2-73
SY2364-2	8192 x 8	200	100	—	+5	24	P	TMS2564	2-73
SY2364-3	8192 x 8	300	100	—	+5	24	P	TMS2564	2-73
SY2364A	8192 x 8	450	100	12	+5	24	P	TMS2564	2-73
SY2364A-2	8192 x 8	200	100	12	+5	24	P	TMS2564	2-73
SY2364A-3	8192 x 8	300	100	12	+5	24	P	TMS2564	2-73
SY2365	8192 x 8	450	100	—	+5	28	P	2764	2-76
SY2365-2	8192 x 8	200	100	—	+5	28	P	2764	2-76
SY2365-3	8192 x 8	300	100	—	+5	28	P	2764	2-76
SY2365A	8192 x 8	450	100	12	+5	28	P	2764	2-76
SY2365A-2	8192 x 8	200	100	12	+5	28	P	2764	2-76
SY2365A-3	8192 x 8	300	100	12	+5	28	P	2764	2-76
SY23128-2[2]	16,384 x 8	200	100	—	+5	28	P	27128	2-79
SY23128-3[2]	16,384 x 8	300	100	—	+5	28	P	27128	2-79
SY23128[2]	16,384 x 8	450	100	—	+5	28	P	27128	2-79
SY23128A-2[2]	16,384 x 8	200	100	10	+5	28	P	27128	2-79
SY23128A-3[2]	16,384 x 8	300	100	10	+5	28	P	27128	2-79
SY23128A[2]	16,384 x 8	450	100	10	+5	28	P	27128	2-79
SY23256-2[2]	32K x 8	200	100	—	+5	28	P	27256	2-82
SY23256-3[2]	32K x 8	300	100	—	+5	28	P	27256	2-82
SY23256[2]	32K x 8	450	100	—	+5	28	P	27256	2-82
SY23256A-2[2]	32K x 8	200	100	10	+5	28	P	27256	2-82
SY23256A-3[2]	32K x 8	300	100	10	+5	28	P	27256	2-82
SY23256A[2]	32K x 8	450	100	10	+5	28	P	27256	2-82

P = Molded DIP

Synertek RAM Cross Reference Guide

Synertek	SY2128/	SY2147H	SY2148H/ SY2149H	SY2158/	SY2167	SY2168/ SY2169
AMD	AM9128	AM9247	AM2148/ AM2149			
Fujitsu	MB8128	MBM2147H	MBM2148/ MBM2149		MB8167A	MB8168
Intel		2147	2148/ 2149		2167	2168
Mostek		MK4104		MK4118A/ MK4801A		
National	NMC2116	NMC2147H	NMC2148H			
NEC	μPD446	μPD2147				
Toshiba	TMM2016	TMM315				
Hitachi	HM6116		HM6148		HM6167	
T.I.	TMS4016	TMS2147H	TMS2149		TMS2167	TMS2168/ TMS2169
Mitsubishi	M58725					

Synertek ROM Cross Reference Guide

Synertek	SY2316B	SY2332	SY2333	SY2364	SY2365	SY23128	SY23256
AMD	AM9216 AM9218	AM9232	AM9233	AM9264	AM9265	AM92128	
AMI	S68A316 S6831B	S68332	S2333	S68A364	S2364	S23128	
G.I.	R0-3-9316	R0-3-9332	R0-3-9333	R0-3-9364	R0-3-9365	R0-9128	
MOSTEK	MK34000			MK36000	MK37000		MK38000
Motorola	MCM68316E	MCM68A332		MCM68364 MCM68365 MCM68366			MCM63256
National	MM52116	MM52132		MM52164			
NEC	μPD2316E	μPD2332		μPD2364			
Signetics	2616	2632		2664A or 2664		26128A	
Toshiba	TMM334	TMM333 TMM2332			TMM2364P		TMM23256
Rockwell	R-03-1316						
EA	EA8316	EA8332	EA8333				
TI		TMS4732		TMS4764			
Fairchild	3516						
Hitachi		HN46332		HN48364			
Intel	2316E	2332			2364A		
Mitsubishi		M58333		M58334			
OKI	MSM3870						
Panasonic		MN2332					
Siemens	SAB8316	SAB8332					

RAMs.

Synertek

SY2128

2048 x 8 Static Random Access Memory

Features

- 100 nsec Maximum Access Time
- Fully Static Operation
  No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (± 10%)
- Pin Compatible with 16K ROMs, EPROMs, and EEPROMs
- Totally TTL Compatible
  All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- JEDEC Approved Pinout

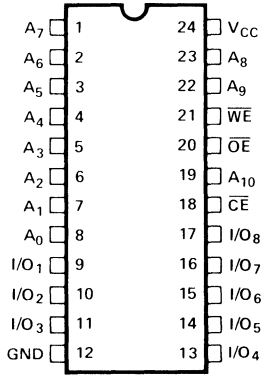
Description

The Synertek SY2128 is a 16,384 bit static Random Access Memory organized 2048 words by eight bits and is fabricated using Synertek's new scaled n-channel silicon gate technology It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus.

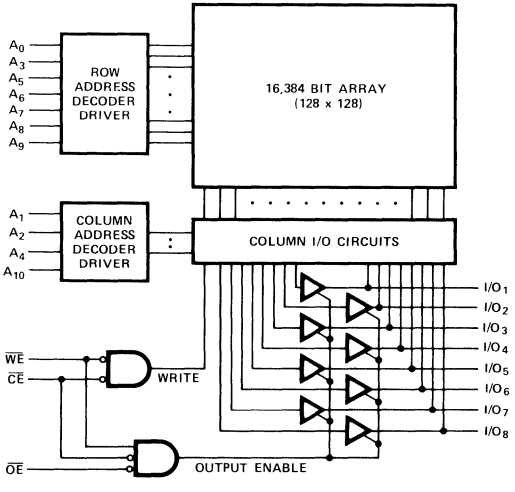
The SY2128 offers an automatic power down feature under the control of the chip enable ($\overline{CE}$) input When $\overline{CE}$ goes high, deselecting the chip, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This feature provides significant system level power savings

The SY2128 is configured in the JEDEC approved pinout for 24 pin byte organized memories and is pin compatible with 16K ROMs, EPROMs and EEPROMs This offers the user the flexibility of being able to switch between RAM, ROM, EPROM, or EEPROM as his needs dictate with a minimum of board changes

Pin Configuration



Block Diagram



MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5V to +7V
Power Dissipation 1.0W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	2128-1/-2/-3/-4 Min.	2128-1/-2/-3/-4 Max.	2128L-2/L-3/L-4 Min.	2128L-2/L-3/L-4 Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	μA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		10		10	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max, V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		95		75	mA	$T_A = 25°C$; V_{CC} = Max, $\overline{CE} = V_{IL}$, Outputs Open
			100		80	mA	$T_A = 0°C$; V_{CC} = Max, $\overline{CE} = V_{IL}$, Outputs Open
I_{SB}	Standby Current		20		15	mA	V_{CC} = Min to Max, $\overline{CE} = V_{IH}$
I_{PO}	Peak Power-on Current Note 6		40		30	mA	V_{CC} = Gnd to V_{CC} Min, $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = -1.0mA

Capacitance

$T_A = 25°C$, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 7)

READ CYCLE

Symbol	Parameter	2128-1 Min.	2128-1 Max.	2128-2/L-2 Min.	2128-2/L-2 Max.	2128-3/L-3 Min.	2128-3/L-3 Max.	2128-4/L-4 Min.	2128-4/L-4 Max.	Unit	Conditions
t_{RC}	Read Cycle Time	100		120		150		200		ns	
t_{AA}	Address Access Time		100		120		150		200	ns	
t_{ACE}	Chip Enable Access Time		100		120		150		200	ns	
t_{AOE}	Output Enable Access Time		40		50		60		700	ns	
t_{OH}	Output Hold from Address Change	10		10		10		10		ns	
t_{LZ}	Output Low Z Time	10		10		10		10		ns	
t_{HZ}	Output High Z Time	0	35	0	40	0	50	0	60	ns	
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns	
t_{PD}	Chip Disable to Power Down Time		50		60		80		100	ns	

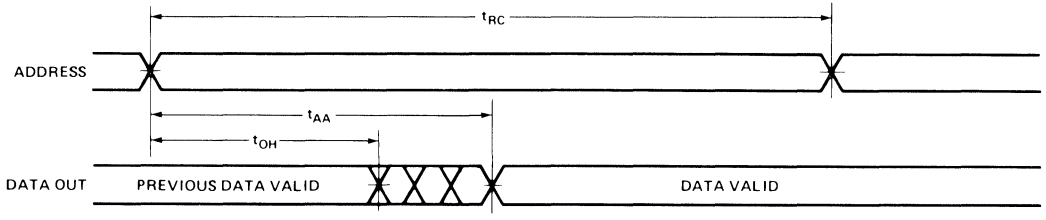
WRITE CYCLE

t_{WC}	Write Cycle Time	100		120		150		200		ns	
t_{CW}	Chip Enable to End of Write	80		90		120		150		ns	
t_{AW}	Address Valid to End of Write	80		90		120		150		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{WP}	Write Pulse Width	60		70		90		120		ns	
t_{WR}	Write Recovery Time	0		0		0		0		ns	
t_{DW}	Data Valid to End of Write	40		50		70		90		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	35	0	40	0	50	0	60	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		0		0		ns	Note 5

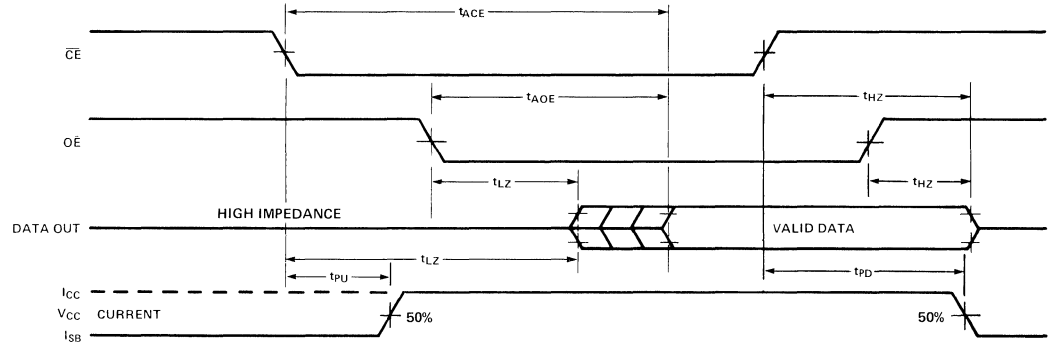
(See following page for notes)

Timing Diagrams

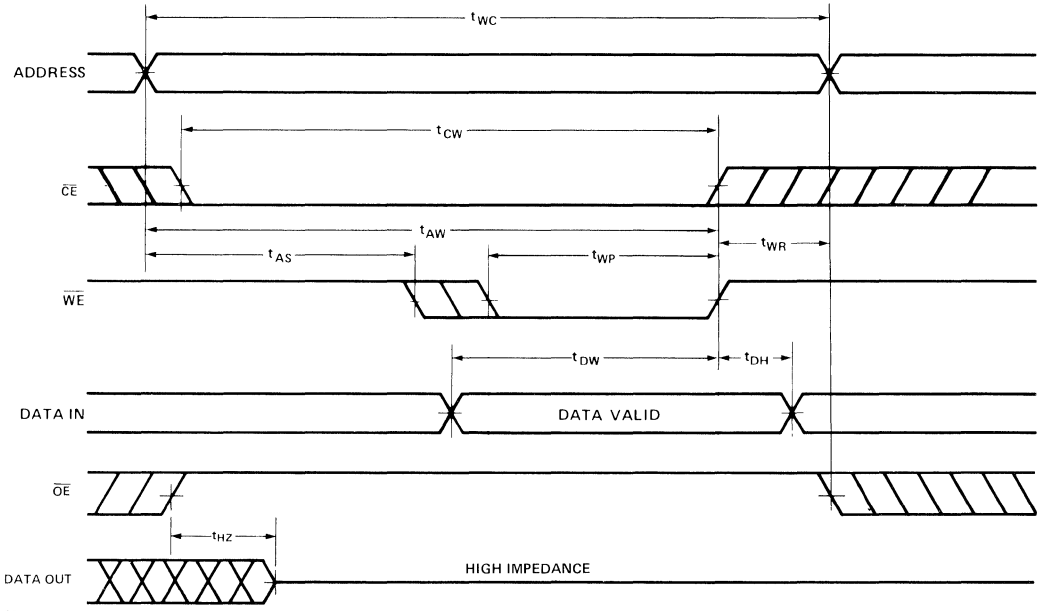
READ CYCLE NO. 1 (NOTES 1 and 2)



READ CYCLE NO. 2 (NOTES 1 and 3)



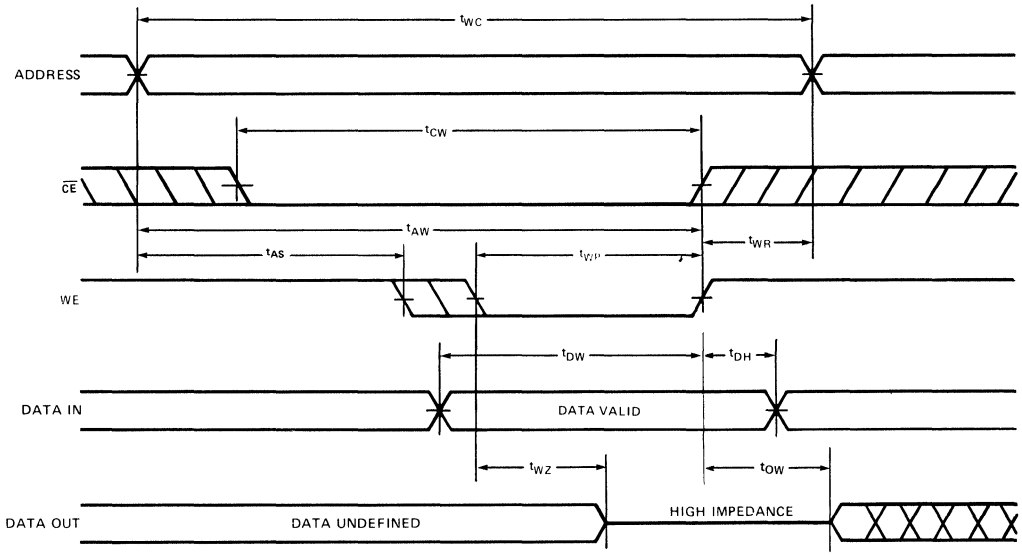
WRITE CYCLE NO. 1 (NOTE 4)



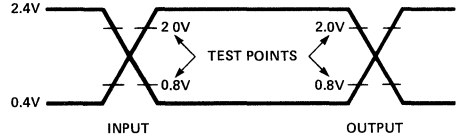
Notes:

1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CE} = \overline{OE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper operation is achieved.

WRITE CYCLE NO. 2 ($\overline{OE}$ = V_{IL}) (NOTE 4)

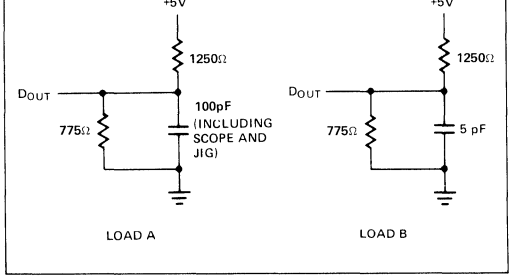


A.C. Testing Input, Output Waveform



AC TESTING. INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability 18 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYP2128-1	100ns	100mA	20mA	Molded DIP
SYP2128-2	120ns	100mA	20mA	Molded DIP
SYP2128-3	150ns	100mA	20mA	Molded DIP
SYP2128-4	200ns	100mA	20mA	Molded DIP
SYP2128L-2	120ns	80mA	15mA	Molded DIP
SYP2128L-3	150ns	80mA	15mA	Molded DIP
SYP2128L-4	200ns	80mA	15mA	Molded DIP

Synertek.

SY2130/SY2131

1024 x 8 Dual Port Random Access Memory

PRELIMINARY

Features

- 100 ns Address Access Time
- Fully Static Operation
- Full TTL Compatibility
- Interrupt Function ($\overline{INT}$) Open Drain for OR-tied Operation
- Easy Microprocessor Interface
- $\overline{BUSY}$ Function to Handle Contention. Open Drain for OR-tied Operation
- SY2130 — Transparent Power Down ($\overline{CE}$)
- SY2131 — Non-Power Down ($\overline{CS}$)
- Output Enable Function ($\overline{OE}$)
- Both Ports Operate Independently

Description

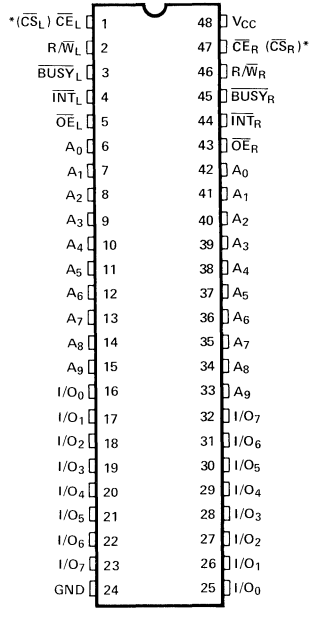
The Synertek SY2130 and SY2131 are 8192 Bit Dual Port Static Random Access Memories organized 1024 words by 8 bits They are designed using fully static circuitry and fabricated using Synertek's n-channel double poly silicon gate technology

The SY2130 and SY2131 feature two separate I/O ports that each allow independent access for read or write to any location in the memory The only situation where contention can occur is when both ports are active and both addresses match Two modes of operation are provided for this situation In one mode, contention is ignored and both operations are allowed to proceed In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed A $\overline{BUSY}$ flag is sent to the side whose operation is delayed $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data

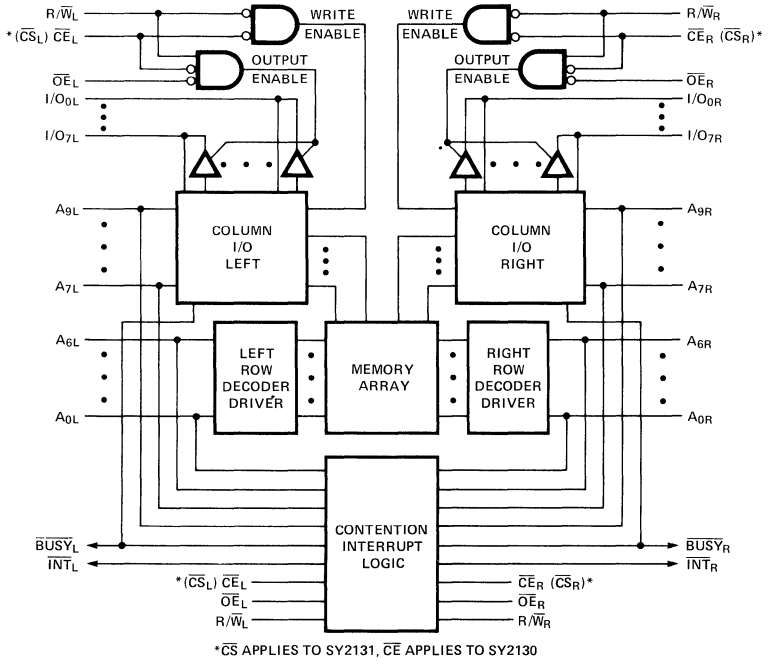
An interrupt function ($\overline{INT}$) is also provided to allow communication between systems This function acts like a writable flag When the flag's location is written from one

(continued next page)

Pin Configuration



Block Diagram



*$\overline{CS}$ APPLIES TO SY2131, $\overline{CE}$ APPLIES TO SY2130

MEMORIES

side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. Both the $\overline{BUSY}$ and $\overline{INT}$ pins are open drain outputs to allow OR-tied operation.

The SY2130 has an automatic power down feature which is controlled by the Chip Enable inputs. Each Chip Enable controls automatic power-down circuitry that allows it's respective side of the device to remain in a standby power mode.

The SY2131 chip select (no power down) access has been designed to be faster than it's address access so that the chip select decode time will not add to the memory's overall access time. This feature significantly improves system performance.

Pin Definitions

$\overline{CE}_L$[10] — Left Port Chip Enable. When $\overline{CE}_L$ goes HIGH, the left port of the RAM is deselected and the left port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CE}_L$ remains HIGH.

$\overline{CE}_R$[10] — Right Port Chip Enable. When $\overline{CE}_R$ goes HIGH, the right port of the RAM is deselected and the right port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CE}_R$ remains HIGH.

$\overline{CS}_L$[11] — Left Port Chip Select. When $\overline{CS}_L$ goes HIGH, the left port of the RAM is deselected.

$\overline{CS}_R$[11] — Right Port Chip Select. When $\overline{CS}_R$ goes HIGH, the right port of the RAM is deselected.

$A0_L$-$A9_L$ — Left Port Address Inputs. The 10-bit field presented at the left port Address Inputs selects one of the 1024 memory locations to be read from or written into via the left port Data Input/Output Lines.

$A0_R$-$A9_R$ — Right Port Address Inputs The 10-bit field presented at the right port Address Inputs selects one of the 1024 memory locations to be read from or written into via the right port Data Input/Output Lines.

$\overline{OE}_L$ — Output Enable for Left Port When $\overline{OE}_L$ is HIGH, the left port outputs are disabled, when $\overline{OE}_L$ is LOW, the left port outputs are enabled. Also controls contention mode for left port

$\overline{OE}_R$ — Output Enable for Right Port. When $\overline{OE}_R$ is HIGH, the right port outputs are disabled. When $\overline{OE}_R$ is LOW, the right port outputs are enabled. Also controls contention mode for right port

$I/O0_L$-$I/O7_L$ — Left Port Data Input/Output Lines

$I/O0_R$-$I/O7_R$ — Right Port Data Input/Output Lines.

$R/\overline{W}_L$ — Left Port Read/Write Enable. When $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, data from the RAM location selected by the left address field is present at the left port Data Input/Output Lines When $R/\overline{W}_L$ is LOW, data present on the left port Data Input/Output Lines is written into the RAM location selected by the left address field irregardless of the state of $\overline{OE}_L$. These operations can be affected by contention. (See Functional Description on page 9).

$R/\overline{W}_R$ — Right Port Read/Write Enable. When $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ is HIGH, data from the RAM location selected by the left address field is present at the right port Data Input/Output Lines When $R/\overline{W}_R$ is LOW, data present on the right port Data Input/Output Lines is written into the RAM location selected by the right address field irregardless of the state of $\overline{OE}_R$. These operations can be affected by contention. (See Functional Description page 9).

$\overline{BUSY}_L$[12] — Left Port Busy Flag. $\overline{BUSY}_L$ remains HIGH at all times unless both ports initiate an operation to the same address location and the left port is operating in contention mode with the right port receiving priority. When this occurs, the right port operation will be completed first and $\overline{BUSY}_L$ will go LOW until the right port operation is completed.

$\overline{BUSY}_R$[12] — Right Port Busy Flag $\overline{BUSY}_R$ remains HIGH at all times unless both ports initiate an operation to the same address location and the right port is operating in contention mode with the left port receiving priority. When this occurs, the left port operation will be completed first and $\overline{BUSY}_R$ will go LOW until the left port operation is completed Both $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are open drain outputs allowing OR-tied operation.

$\overline{INT}_L$[12] — Left Port Interrupt Flag. If the right port writes to memory location 3FE then $\overline{INT}_L$ is latched LOW until the left port reads data from memory location 3FE.

$\overline{INT}_R$[12] — Right Port Interrupt Flag. If the left port writes to memory location 3FF, then $\overline{INT}_R$ is latched LOW until the right port reads data from memory location 3FF Both $\overline{INT}_L$ and $\overline{INT}_R$ are open drain allowing OR-tied operation.

(see page 2-16 for notes)

Absolute Maximum Ratings*

Temperature Under Bias ..... −10°C to 85°C
Storage Temperature ..... −65°C to 150°C
Voltage on any Pin with Respect to Ground ..... −3 5V to +7V
Power Dissipation 1 0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	SY2130/SY2131-1/-2/-3/-4 Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} =Max , V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max. V_{OUT} = GND to 4.5V
I_{CC}	Power Supply Current (Both Ports Active)		150	mA	$T_A = 25°C$; V_{CC} = Max , $\overline{CE} = V_{IL}$ Outputs Open
			170	mA	$T_A = 0°C$
I_{SB1}	Standby Current (Both Ports Standby)		40	mA	V_{CC} = Min. to Max., $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$ (Note 10)
I_{SB2}	Standby Current (One Port Standby)		110	mA	V_{CC} = Min. to Max., $\overline{CE}_L$ or $\overline{CE}_R = V_{IH}$ (Note 10)
V_{IL}	Input Low Voltage	-0 5	0 8	V	
V_{IH}	Input High Voltage	2 2	6 0	V	
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 3 2 mA (Note 12)
V_{OH}	Output High Voltage	2 4		V	I_{OH} = −1.0 mA (Note 12)

Capacitance $T_A = 25°C$, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

READ CYCLE (Note 12)

Symbol	Parameter	SY2130-1 SY2131-1 Min.	Max.	SY2130-2 SY2131-2 Min.	Max.	SY2130-3 SY2131-3 Min.	Max.	SY2130-4 SY2131-4 Min.	Max.	Units	Conditions
t_{RC}	Read Cycle Time	100		120		150		200		ns	
t_{AA}	Address Access Time		100		120		150		200	ns	
t_{ACE}	Chip Enable Access Time		100		120		150		200	ns	[10]
t_{AOE}	Output Enable Access Time		40		50		60		80	ns	
t_{OH}	Output Hold from Address Change	10		10		10		20		ns	
t_{LZ}	Output Low Z Time	10		10		10		20		ns	[5]
t_{HZ}	Output High Z Time	0	40	0	50	0	60	0	80	ns	[5]
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns	[10]
t_{PD}	Chip Disable to Power Down Time		50		60		70		100	ns	[10]
t_{ACS}	Chip Select Access Time		80		100		110		160	ns	[11]

(see page 2-16 for notes)

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$ (continued) (Note 12)

WRITE CYCLE

Symbol	Parameter	SY2130-1 SY2131-1 Min.	SY2130-1 SY2131-1 Max.	SY2130-2 SY2131-2 Min.	SY2130-2 SY2131-2 Max.	SY2130-3 SY2131-3 Min.	SY2130-3 SY2131-3 Max.	SY2130-4 SY2131-4 Min.	SY2130-4 SY2131-4 Max.
t_{WC}	Write Cycle Time	100		120		150		200	
t_{EW}	Chip Enable to End of Write	90		105		120		180	[10]
t_{SW}	Chip Select to End of Write	70		85		90		140	[11]
t_{AW}	Address Valid to End of Write	90		105		120		180	
t_{AS}	Address Setup Time	0		0		0		0	
t_{WP}	Write Pulse Width	60		70		80		120	
t_{WR}	Write Recovery Time	0		0		0		0	
t_{DW}	Data Valid to End of Write	40		50		60		80	
t_{DH}	Data Hold Time	0		0		0		0	
t_{WZ}	Write Enabled to Output in High Z	0	40	0	50	0	60	0	80 [5]
t_{OW}	Output Active from End of Write	0		0		0		0	[5]

BUSY TIMING

t_{RC}	Read Cycle Time	100		120		150		200	
t_{WC}	Write Cycle Time	100		120		150		200	
t_{OEH}	Output Enable Hold Time	20		25		30		40	
t_{OER}	Output Enable Recovery Time	0		0		0		0	
t_{BAA}	$\overline{BUSY}$ Access Time to Address		40		50		60		80
t_{BDA}	$\overline{BUSY}$ Disable Time to Address		40		50		60		80
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable or Chip Select		40		50		60		80
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable or Chip Select		40		50		60		80
t_{APS}	Arbitration Priority Set Up Time	20		25		30		40	
t_{AOS}	Arbitration Override Set Up Time	20		25		30		40	

INTERRUPT TIMING (Note 12)

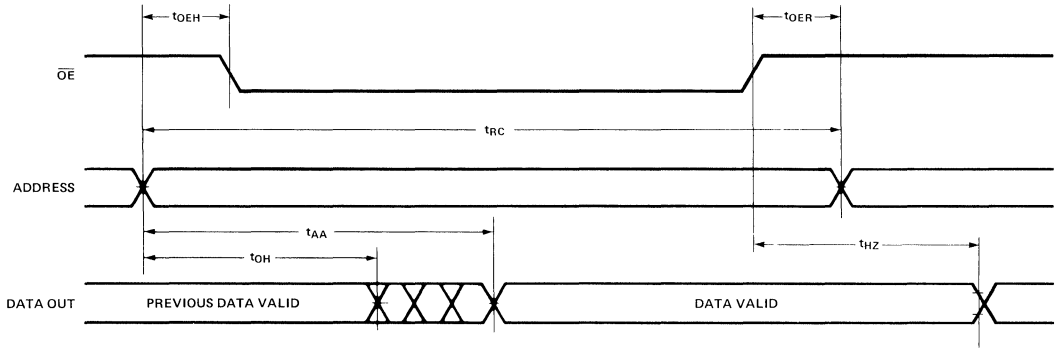
t_{AS}	Address Set Up Time	0		0		0		0	
t_{AW}	Write Recovery Time	0		0		0		0	
t_{INS}	Interrupt Set Time		40		50		60		80
t_{INR}	Interrupt Reset Time		40		50		60		80

NOTES

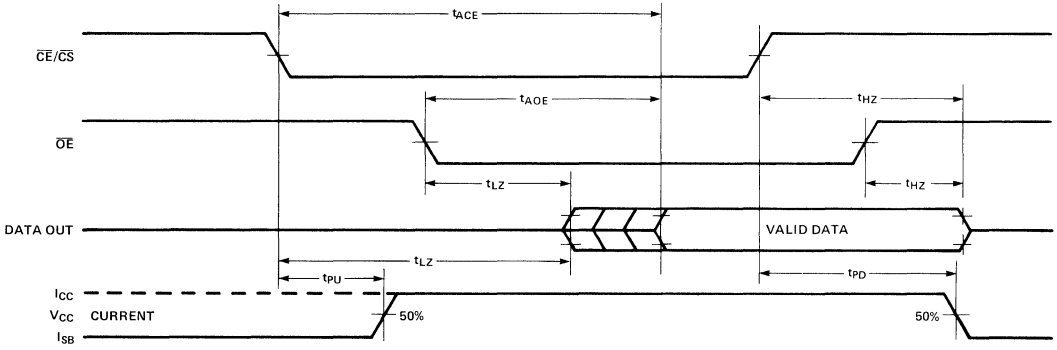
1 R/$\overline{W}$ is high for Read Cycles
2 Device is continuously enabled/selected, $\overline{CE} = V_{IL}$ or $\overline{CS} = V_{IL}$
3 Addresses valid prior to or coincident with $\overline{CE}$ or $\overline{CS}$ transition low
4 If $\overline{CE}$ or $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state
5 Transition is measured ±500 mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
6 A pullup resistor to V_{CC} on the $\overline{CE}$ or $\overline{CS}$ input is required to keep the device deselected otherwise, power-on current approaches I_{CC} active
7 $\overline{OE}$ can be V_{IH} when contention arbitration mode occurs or V_{IL} when contention override mode occurs, see Tables 2 and 3
8 $\overline{CE}_L = \overline{CE}_R = V_{IL}$ or $\overline{CS}_L = \overline{CS}_R = V_{IL}$
9 Busy timing is identical to Contention Cycle Nos 1 and 2
10 Applies to SY2130 version (power down) only
11 Applies to SY2131 version (non-power down) only
12 The interrupt and busy signals (pins 3, 4, 44 and 45) are open drain outputs A pull-up resistor is required for system operation Load C is used for A C testing these pins All other outputs use load A
13 Read or Write Cycle Timing after $\overline{BUSY}$ inactive as shown in previous timing diagrams

Timing Diagrams

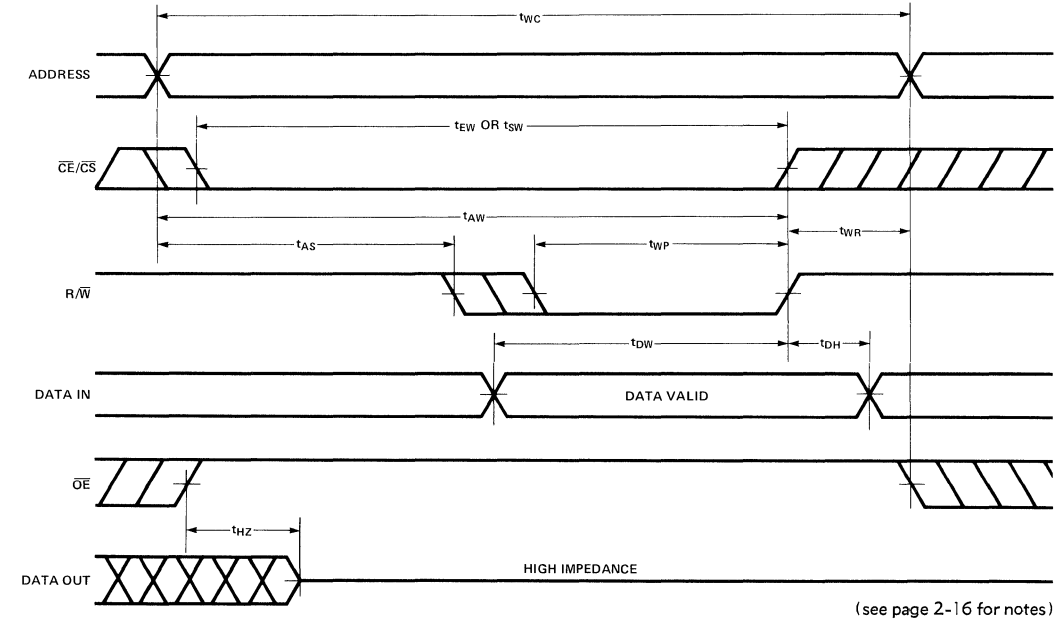
READ CYCLE NO. 1 EITHER SIDE (Notes 1 and 2)



READ CYCLE NO. 2 EITHER SIDE (Notes 1 and 3)

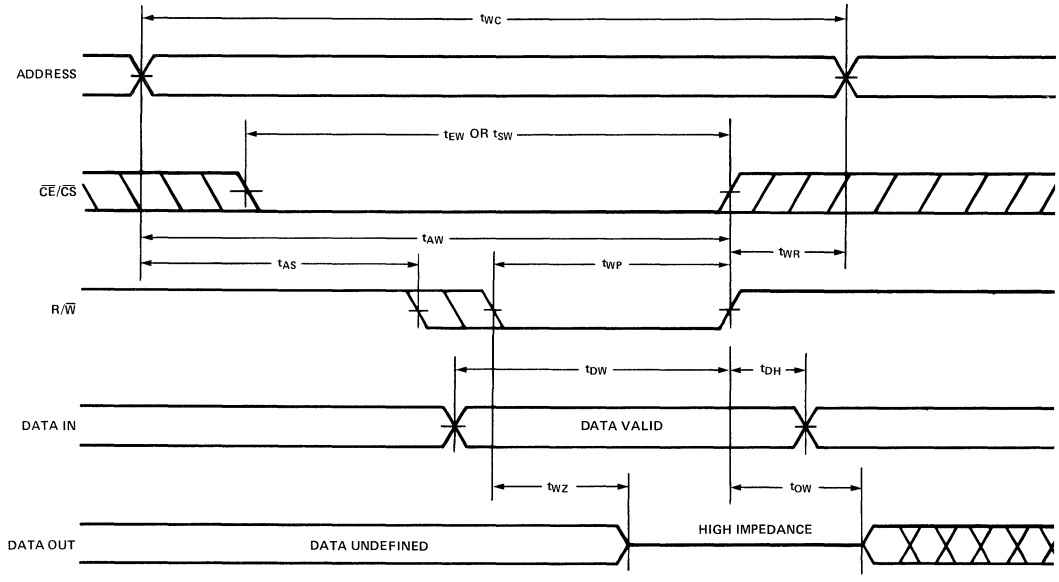


WRITE CYCLE NO. 1 EITHER SIDE (Note 4)



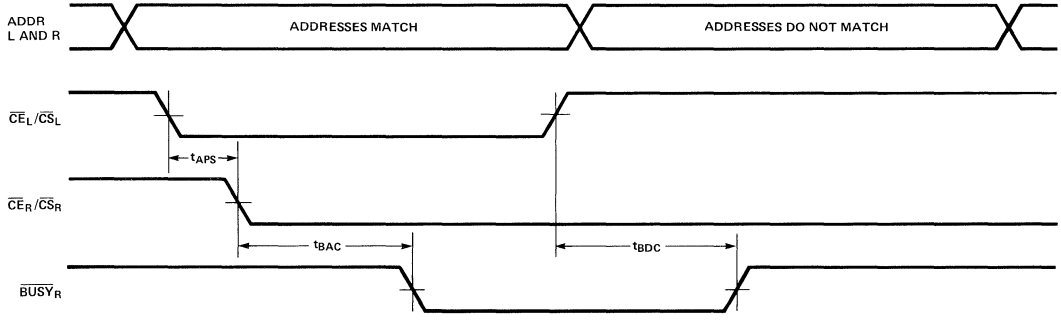
(see page 2-16 for notes)

WRITE CYCLE NO. 2 EITHER SIDE ($\overline{OE}$ = V_{IL}) (Note 4)

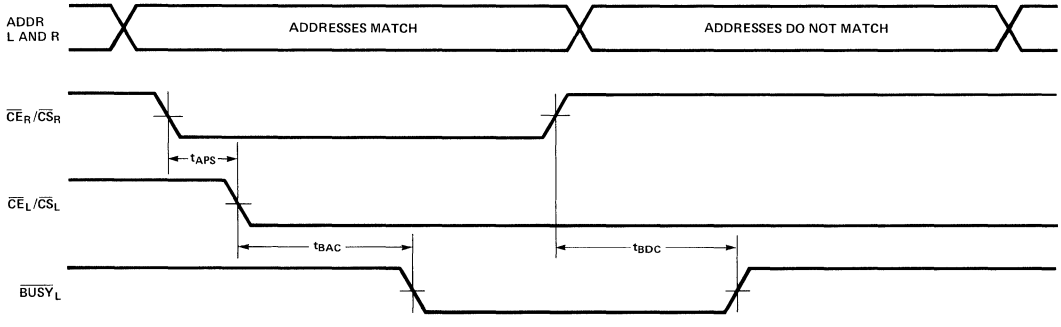


CONTENTION CYCLE NO. 1 ($\overline{CE}$/$\overline{CS}$ CONTENTION ARBITRATION MODE) (Note 7)

$\overline{CE}_L$/$\overline{CS}_L$ VALID FIRST:



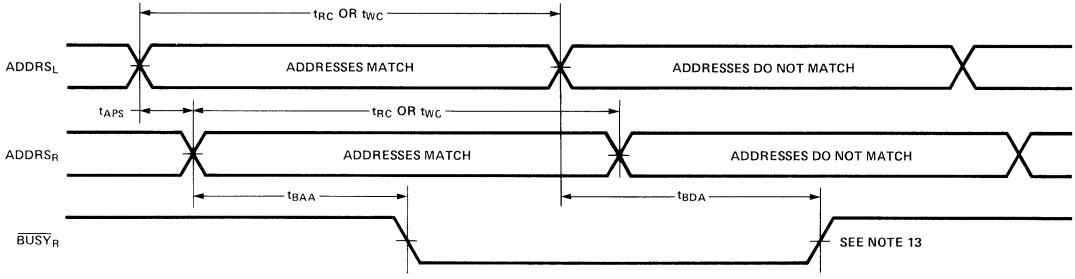
$\overline{CE}_R$/$\overline{CS}_R$ VALID FIRST:



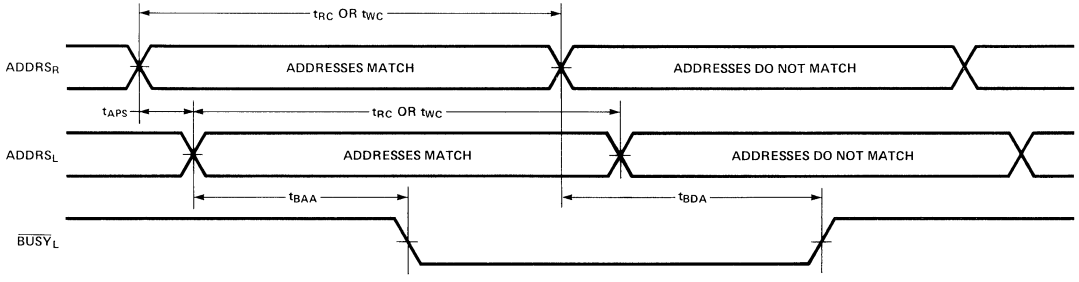
(see page 2-16 for notes)

CONTENTION CYCLE NO. 2 (ADDRESS CONTENTION ARBITRATION MODE) (Notes 7 and 8)

$ADDRESS_L$ VALID FIRST:

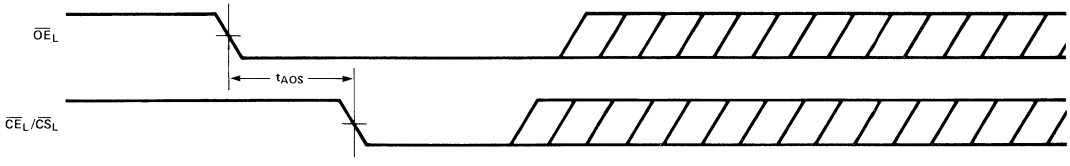


$ADDRESS_R$ VALID FIRST:

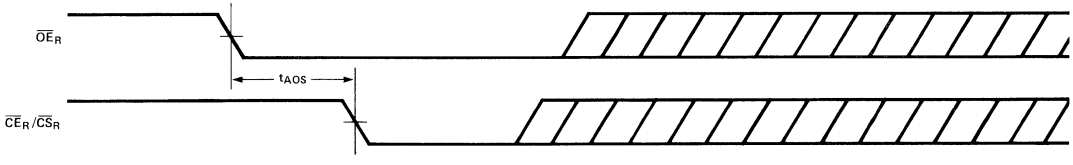


CONTENTION CYCLE NO. 3 (CONTENTION OVERRIDE MODE) (Note 9)

LEFT PORT CONTENTION IGNORED:



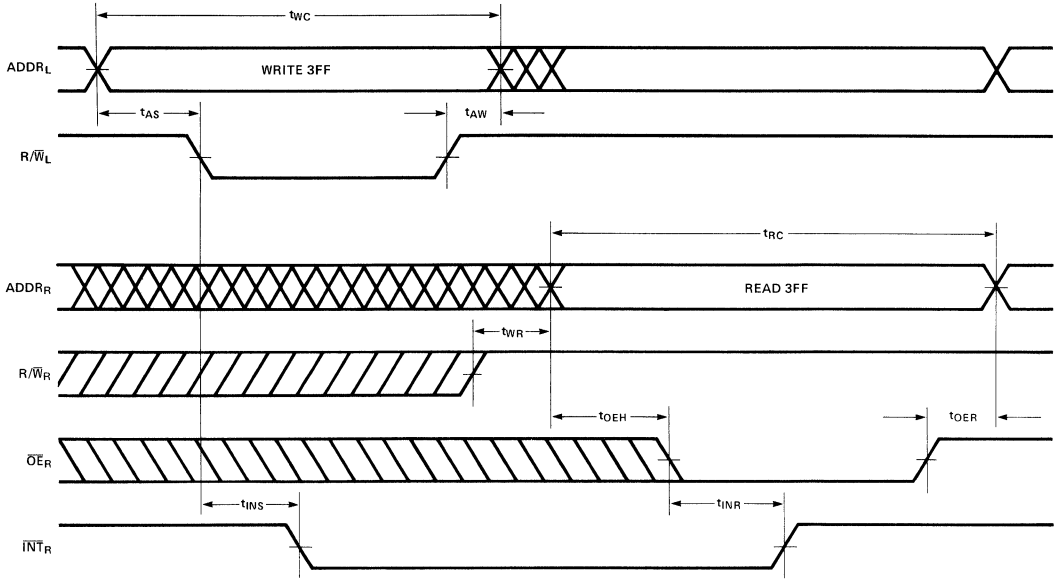
RIGHT PORT CONTENTION IGNORED:



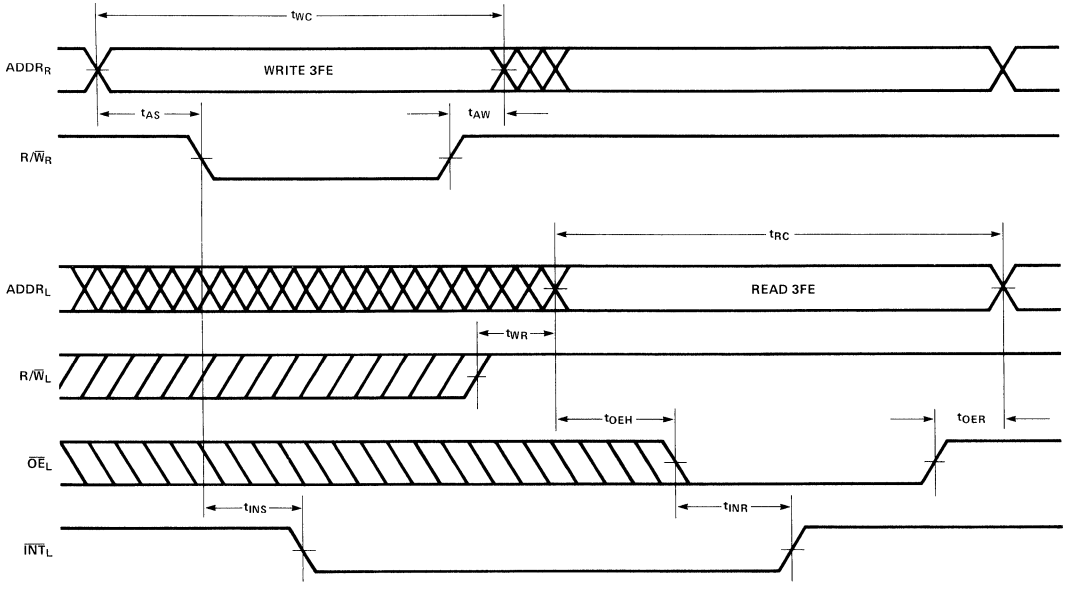
(see page 2-16 for notes)

INTERRUPT MODE (Note 8)

LEFT SIDE FLAGS RIGHT SIDE:



RIGHT SIDE FLAGS LEFT SIDE:



(see page 2-16 for notes)

Functional Description

The SY2130 and SY2131 are 1024-word by 8-bit dual port RAMs that feature two separate I/O ports Each port allows independent access for read or write to any location in the memory

The SY2130 features separate left and right port Chip Enable controls ($\overline{CE}_L$ and $\overline{CE}_R$) Each Chip Enable activates its respective port when it goes LOW and controls automatic power-down circuitry that allows it's respective side of the device to remain in a standby power mode as long as it remains HIGH When a port is active, it is allowed access to the entire memory array

The SY2131 features separate left and right port Chip Select controls ($\overline{CS}_L$ and $\overline{CS}_R$) Each Chip Select activates its respective port when it goes LOW and allows its respective side of the device to remain selected as long as it remains LOW. When a port is active, it is allowed access to the entire memory array.

Each port has an Output Enable control ($\overline{OE}_L$ and $\overline{OE}_R$) that keeps its respective output in a high impedance mode when HIGH When a port's $\overline{OE}$ is LOW, that port's output drivers are turned on providing its R/$\overline{W}$ control is HIGH

Separate Read/Write Enable inputs (R/$\overline{W}_L$ and R/$\overline{W}_R$) control writing of new data into any location in the RAM from either port When R/$\overline{W}_L$ is LOW, new data is written into the location selected by the left address field Likewise, when R/$\overline{W}_R$ is LOW, new data is written into the location selected by the right address field When a port's Read/Write Enable is HIGH, data can be read from that port if its respective $\overline{OE}$ is LOW When R/$\overline{W}_L$ is HIGH and $\overline{OE}_L$ is LOW, data is read from the location selected by the left address field When R/$\overline{W}_R$ is HIGH and $\overline{OE}_R$ is LOW, data is read from the location selected by the right address field

There is one situation where contention can occur It is when both left and right ports are active and both addresses match Two modes of operation are provided for this situation (i) on-chip control logic arbitrates the situation, or (ii) contention is ignored and both ports are given access to that memory location $\overline{OE}$ controls the mode of operation

If $\overline{CE}$ or $\overline{CS}$ is LOW before $\overline{OE}$ goes LOW when both addresses match, then on-chip control logic arbitrates the situation Priority is given to the port whose $\overline{CE}$ or $\overline{CS}$ became valid first, the other port will not be allowed access to the memory core until that port's operation is completed

If both port's $\overline{CE}$ or $\overline{CS}$ controls became valid at the same time while their $\overline{OE}$s are HIGH, then the left port is given priority If both $\overline{CE}$ or $\overline{CS}$ pins are valid before their respective $\overline{OE}$ controls and an address change causes an address match while $\overline{OE}$ is HIGH, then priority is given to the port whose address became valid first; the other port is not allowed access to the memory until that port's operation is completed If both addresses became valid at the same time and match, and $\overline{OE}$ is HIGH, then the left port is given priority

In the other mode, contention is ignored and one or both ports have access to the memory core at all times This is accomplished by having $\overline{OE}$ LOW when the contention occurs That is, the RAM core is accessible from a port even if the on-chip control logic would have delayed its access provided (a) the port's $\overline{OE}$ is LOW when its $\overline{CE}$ or $\overline{CS}$ goes LOW during an address match, or (b) both ports are active and its $\overline{OE}$ is LOW when an address change causes an address match Therefore, it is possible for both ports to have access to the same memory location at the same time, even in a $WRITE_L$-$WRITE_R$ situation

Separate Busy Flags ($\overline{BUSY}_L$ and $\overline{BUSY}_R$) are provided to signal when a port's access to the memory core has been delayed When both ports try to access the same memory location, the on-chip arbitration logic causes the Busy Flag to go LOW on the side that is delayed These flags are provided to allow the user to stop the processor if desired. $\overline{BUSY}$ is driven out fast enough for the processor's address and data to be preserved if desired. The Busy Flags are operational even when the device is operating in the mode where contention is ignored and function the same as described for contention mode operation. This permits their use to signal that contention has occurred and data may have been changed

Interrupt logic is included on-chip to provide a means for two processors to communicate to one another If the left port writes to memory location 3FF, then the right port Interrupt Flag ($\overline{INT}_R$) is latched LOW until the right port reads data from that same location If the right port writes to location 3FE, then the left port Interrupt Flag ($\overline{INT}_L$) is latched LOW until the left port reads data from that location If both ports are enabled and contention occurs, the Busy circuitry will disable the address decoder from setting or resetting the Interrupt Flags

Table 1. Non-Contention Read/Write Control

Left Port Inputs				Right Ports Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L/\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A9_L$	$R/\overline{W}_R$	$\overline{CE}_R/\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A9_R$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	H	X	X	X	X	X	X	H	X	H	X	Left Port in Power Down Mode
X	X	X	X	X	H	X	X	H	X	H	X	Right Port in Power Down Mode
L*	L	X	X	X	X	X	X	H	X	H	X	Data on Left Port Written to Memory Location $A0_L$-$A9_L$
H	L	L	X	X	X	X	X	H	X	H	X	Data in Memory Location $A0_L$-$A9_L$ Output on Left Port
X	X	X	X	L	L	X	X	H	X	H	X	Data on Right Port Written to Memory Location $A0_R$-$A9_R$
X	X	X	X	H	L	L	X	H	X	H	X	Data in Memory Location $A0_R$-$A9_R$ Output on Right Port
L	L	X	3FF	X	X	X	X	H	X	H	L	Left Side Flags Right Side to Read Memory Location 3FF
X	X	X	X	L	L	X	3FE	H	L	H	X	Right Side Flags Left Side to Read Memory Location 3FE

H = HIGH L = LOW X = Don't Care

Table 2. $\overline{CE}/\overline{CS}$ Contention Arbitration

Left Port Inputs			Right Port Inputs			Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L/\overline{CS}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R/\overline{CS}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	L1	X	X	L	LAC	H	X	L	X	Left Operation Allowed RAM Inaccessible from Right
X	L	LAC	X	L1	X	L	X	H	X	Right Operation Allowed RAM Inaccessible from Left
X	Both	X	X	Both	LAC	H	X	L	X	Left Operation Allowed RAM Inaccessible from Right
X	L1	X	X	L	LBC	H	X	L	X	Left Operation Allowed RAM Accessible from Right*
X	L	LBC	X	L1	X	L	X	H	X	Right Operation Allowed RAM Accessible from Left*
X	Both	X	X	Both	LBC	H	X	L	X	Left Operation Allowed RAM Accessible from Right*

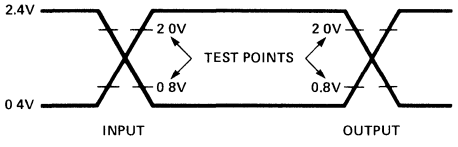
1 = Pin active before equivalent pin on other port
LAC = LOW after chip enable
LBC = LOW before chip enable
Both = Equivalent pins on both ports become active at the same time
*See Contention Override Mode Timing on page 7

Table 3. Address Contention Arbitration

Left Port Inputs				Right Ports Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L/\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A9_L$	$R/\overline{W}_R$	$\overline{CE}_R/\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A9_R$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	L	X	Match1	X	L	X	Match	H	X	L	X	Left Operation Allowed**
X	L	X	Match	X	L	X	Match1	L	X	H	X	Right Operation Allowed**
X	L	X	Both	X	L	X	Both	H	X	L	X	Left Operation Allowed**

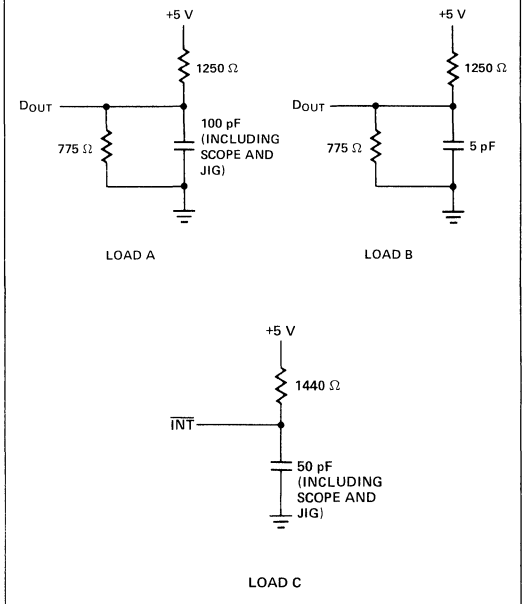
Match = Addresses on left and right ports are identical
Match 1 = Address valid on the port before becoming valid on opposite port
Both = Addresses match and become valid on both ports at the same time
**RAM inaccessible from other port unless that ports $\overline{OE}$ was low when the match occurred Also see Note 7

A.C. Testing Input, Output Waveform



AC TESTING INPUTS ARE DRIVEN AT 2 4V FOR A LOGIC "1" AND 0 4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2 0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" INPUT PULSE RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)†	Package Type
SYP2130-1 SYC2130-1	100 ns 100 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2131-1 SYC2131-1	100 ns 100 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic
SYP2130-2 SYC2130-2	120 ns 120 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2131-2 SYC2131-2	120 ns 120 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic
SYP2130-3 SYC2130-3	150 ns 150 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2131-3 SYC2131-3	150 ns 150 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic
SYP2130-4 SYC2130-4	200 ns 200 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2131-4 SYC2131-4	200 ns 200 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic

*Not applicable
†Both ports standby/one port standby.

Synertek.

SY2132/SY2133

512 x 8 Dual Port Random Access Memory

ADVANCED INFORMATION

Features

- 100 ns Address Access Time
- Fully Static Operation
- Full TTL Compatibility
- Interrupt Function ($\overline{INT}$). Open Drain for OR-tied Operation
- Easy Microprocessor Interface
- $\overline{BUSY}$ Function to Handle Contention
- SY2132 — Transparent Power Down ($\overline{CE}$)
- SY2133 — Non-Power Down ($\overline{CS}$)
- Output Enable Function ($\overline{OE}$)
- Both Ports Operate Independently
- Each Port Accesses Entire Memory

Description

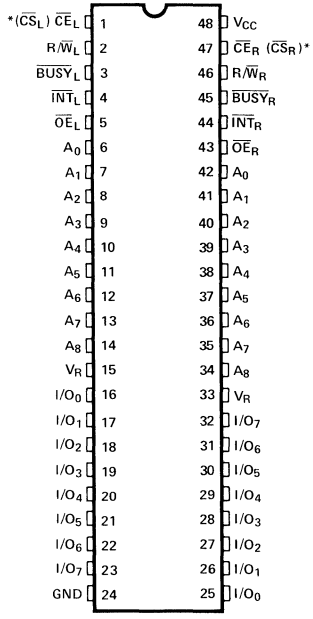
The Synertek SY2132 and SY2133 are 4096 Bit Dual Port Static Random Access Memories organized 512 words by 8 bits. They are designed using fully static circuitry and fabricated using Synertek's n-channel double poly silicon gate technology

The SY2132 and SY2133 feature two separate I/O ports that each allow independent access for read or write to any location in the memory The only situation where contention can occur is when both ports are active and both addresses match. Two modes of operation are provided for this situation. In one mode, contention is ignored and both operations are allowed to proceed. In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed A $\overline{BUSY}$ flag is sent to the side whose operation is delayed $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data

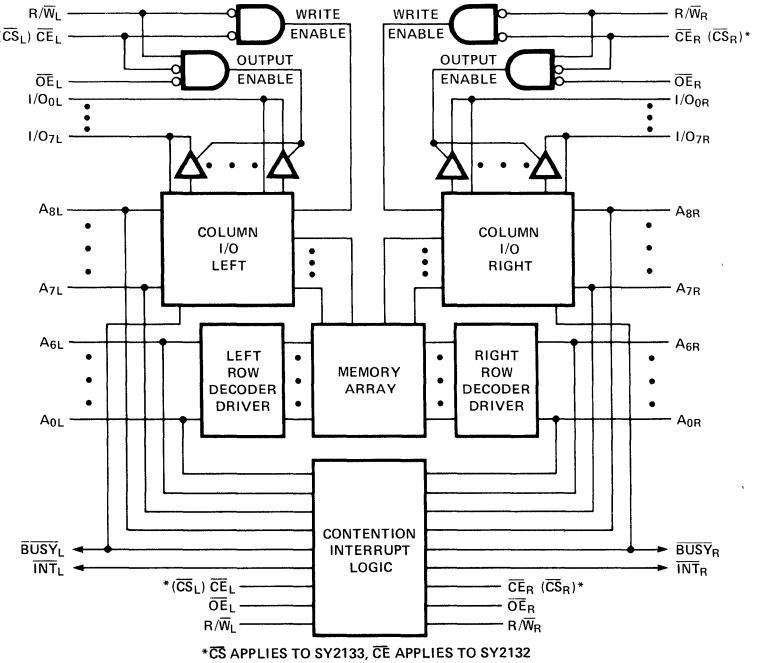
An interrupt function ($\overline{INT}$) is also provided to allow communication between systems This function acts like a writable flag When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side The $\overline{INT}$s have open drain drivers to

(continued next page)

Pin Configuration



Block Diagram



*$\overline{CS}$ APPLIES TO SY2133, $\overline{CE}$ APPLIES TO SY2132

allow OR-tied operation

The SY2132 has an automatic power down feature which is controlled by the Chip Enable inputs Each Chip Enable controls automatic power-down circuitry that allows it's respective side of the device to remain in a standby power mode.

The SY2133 chip select (no power down) access has been designed to be faster than its address access so that the chip select decode time will not add to the memory's overall access time This feature significantly improves system performance

Pin Definitions

$\overline{CE}_L$ Left Port Chip Enable When $\overline{CE}_L$ goes HIGH, the left port of the RAM is deselected and the left port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CE}_L$ remains HIGH

$\overline{CE}_R$ Right Port Chip Enable When $\overline{CE}_R$ goes HIGH, the right port of the RAM is deselected and the right port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CE}_R$ remains HIGH

$\overline{CS}_L$(11) Left Port Chip Select When $\overline{CS}_L$ goes HIGH, the left port of the RAM is deselected

$\overline{CS}_R$(11) Right Port Chip Select When $\overline{CS}_R$ goes HIGH, the right port of the RAM is deselected

$A0_L$-$A8_L$ Left Port Address Inputs The 9-bit field presented at the left port Address Inputs selects one of the 512 memory locations to be read from or written into via the left port Data Input/Output Lines

$A0_R$-$A8_R$ Right Port Address Inputs The 9-bit field presented at the right port Address Inputs selects one of the 512 memory locations to be read from or written into via the right port Data Input/Output Lines

$\overline{OE}_L$ Output Enable for Left Port When $\overline{OE}_L$ is HIGH, the left port outputs are disabled, when $\overline{OE}_L$ is LOW, the left port outputs are enabled Also controls contention mode for left port

$\overline{OE}_R$ Output Enable for Right Port When $\overline{OE}_R$ is HIGH, the right port outputs are disabled When $\overline{OE}_R$ is LOW, the right port outputs are enabled Also controls contention mode for right port

$I/O0_L$-$I/O7_L$ Left Port Data Input/Output Lines

$I/O0_R$-$I/O7_R$ Right Port Data Input/Output Lines

$R/\overline{W}_L$ Left Port Read/Write Enable When $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, data from the RAM location selected by the left address field is present at the left port Data Input/Output Lines When $R/\overline{W}_L$ is LOW, data present on the left port Data Input/Output Lines is written into the RAM location selected by the left address field irregardless of the state of $\overline{OE}_L$ These operations can be affected by contention

$R/\overline{W}_R$ Right Port Read/Write Enable When $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ is HIGH, data from the RAM location selected by the left address field is present at the right port Data Input/Output Lines When $R/\overline{W}_R$ is LOW, data present on the right port Data Input/Output Lines is written into the RAM location selected by the right address field irregardless of the state of $\overline{OE}_R$ These operations can be affected by contention

$\overline{BUSY}_L$ Left Port Busy Flag $\overline{BUSY}_L$ remains HIGH at all times unless both ports initiate an operation to the same address location and the left port is operating in contention mode with the right port receiving priority When this occurs, the right port operation will be completed first and $\overline{BUSY}_L$ will go LOW until the right port operation is completed

$\overline{BUSY}_R$ Right Port Busy Flag. $\overline{BUSY}_R$ remains HIGH at all times unless both ports initiate an operation to the same address location and the right port is operating in contention mode with the left port receiving priority When this occurs, the left port operation will be completed first and $\overline{BUSY}_R$ will go LOW until the left port operation is completed Both $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are open drain outputs allowing OR-tied operation

$\overline{INT}_L$ Left Port Interrupt Flag If the right port writes to memory location 1FE then $\overline{INT}_L$ is latched LOW until the left port reads data from memory location 1FE

$\overline{INT}_R$ Right Port Interrupt Flag If the left port writes to memory location 1FF, then $\overline{INT}_R$ is latched LOW until the right port reads data from memory location 1FF Both $\overline{INT}_L$ and $\overline{INT}_R$ are open drain allowing OR-tied operation

V_R Pins 15 and 33 are reference inputs and should be tied to V_{CC} for normal operation

MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... −10°C to 85°C
Storage Temperature ..... −65°C to 150°C
Voltage on any Pin with Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	SY2132/SY2133-1/-2/-3/-4 Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} =Max., V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max V_{OUT} = GND to 4 5V
I_{CC}	Power Supply Current (Both Ports Active)		150	mA	$T_A = 25°C$ | V_{CC} = Max , $\overline{CE} = V_{IL}$ Outputs Open
			170	mA	$T_A = 0°C$
I_{SB1}	Standby Current (Both Ports Standby)		40	mA	V_{CC} = Min to Max , $\overline{CE_L}$ and $\overline{CE_R} = V_{IH}$ (Note 10)
I_{SB2}	Standby Current (One Port Standby)		110	mA	V_{CC} = Min. to Max , $\overline{CE_L}$ or $\overline{CE_R} = V_{IH}$ (Note 10)
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2 2	6.0	V	
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 3 2 mA (Note 12)
V_{OH}	Output High Voltage	2 4		V	I_{OH} = −1 0 mA (Note 12)

Capacitance $T_A = 25°C$, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

READ CYCLE (Note 12)

Symbol	Parameter	SY2132-1 SY2133-1 Min.	Max.	SY2132-2 SY2133-2 Min.	Max.	SY2132-3 SY2133-3 Min.	Max.	SY2132-4 SY2133-4 Min.	Max.	Units	Conditions
t_{RC}	Read Cycle Time	100		120		150		200		ns	
t_{AA}	Address Access Time		100		120		150		200	ns	
t_{ACE}	Chip Enable Access Time		100		120		150		200	ns	[10]
t_{AOE}	Output Enable Access Time		40		50		60		80	ns	
t_{OH}	Output Hold from Address Change	10		10		10		20		ns	
t_{LZ}	Output Low Z Time	10		10		10		20		ns	[5]
t_{HZ}	Output High Z Time	0	40	0	50	0	60	0	80	ns	[5]
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns	[10]
t_{PD}	Chip Disable to Power Down Time		50		60		70		100	ns	[10]
t_{ACS}	Chip Select Access Time		80		100		110		160	ns	[11]

(see page 2-27 for notes)

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$ (continued) (Note 12)

WRITE CYCLE

Symbol	Parameter	SY2132-1 SY2133-1 Min.	SY2132-1 SY2133-1 Max.	SY2132-2 SY2133-2 Min.	SY2132-2 SY2133-2 Max.	SY2132-3 SY2133-3 Min.	SY2132-3 SY2133-3 Max.	SY2132-4 SY2133-4 Min.	SY2132-4 SY2133-4 Max.
t_{WC}	Write Cycle Time	100		120		150		200	
t_{EW}	Chip Enable to End of Write	90		105		120		180	[10]
t_{SW}	Chip Select to End of Write	70		85		90		140	[11]
t_{AW}	Address Valid to End of Write	90		105		120		180	
t_{AS}	Address Setup Time	0		0		0		0	
t_{WP}	Write Pulse Width	60		70		80		120	
t_{WR}	Write Recovery Time	0		0		0		0	
t_{DW}	Data Valid to End of Write	40		50		60		80	
t_{DH}	Data Hold Time	0		0		0		0	
t_{WZ}	Write Enabled to Output in High Z	0	40	0	50	0	60	0	80 [5]
t_{OW}	Output Active from End of Write	0		0		0		0	[5]

BUSY TIMING

t_{RC}	Read Cycle Time	100		120		150		200	
t_{WC}	Write Cycle Time	100		120		150		200	
t_{OEH}	Output Enable Hold Time	20		25		30		40	
t_{OER}	Output Enable Recovery Time	0		0		0		0	
t_{BAA}	$\overline{BUSY}$ Access Time to Address		40		50		60		80
t_{BDA}	$\overline{BUSY}$ Disable Time to Address		40		50		60		80
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable or Chip Select		40		50		60		80
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable or Chip Select		40		50		60		80
t_{APS}	Arbitration Priority Set Up Time	20		25		30		40	
t_{AOS}	Arbitration Override Set Up Time	20		25		30		40	

INTERRUPT TIMING (Note 12)

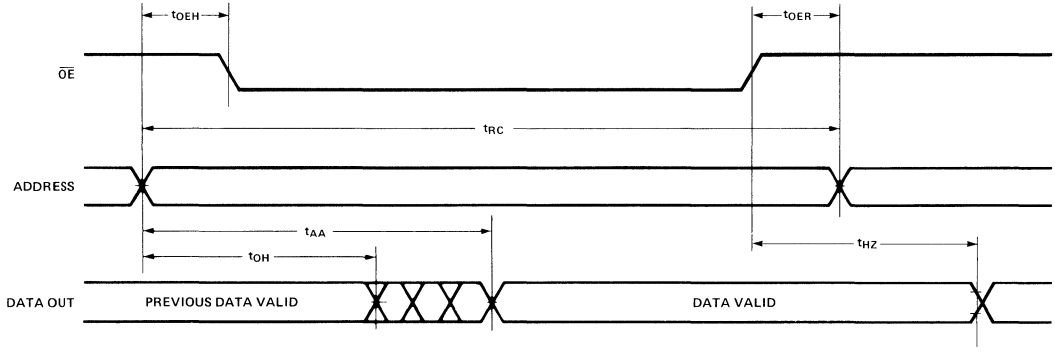
t_{AS}	Address Set Up Time	0		0		0		0	
t_{AW}	Write Recovery Time	0		0		0		0	
t_{INS}	Interrupt Set Time		40		50		60		80
t_{INR}	Interrupt Reset Time		40		50		60		80

NOTES

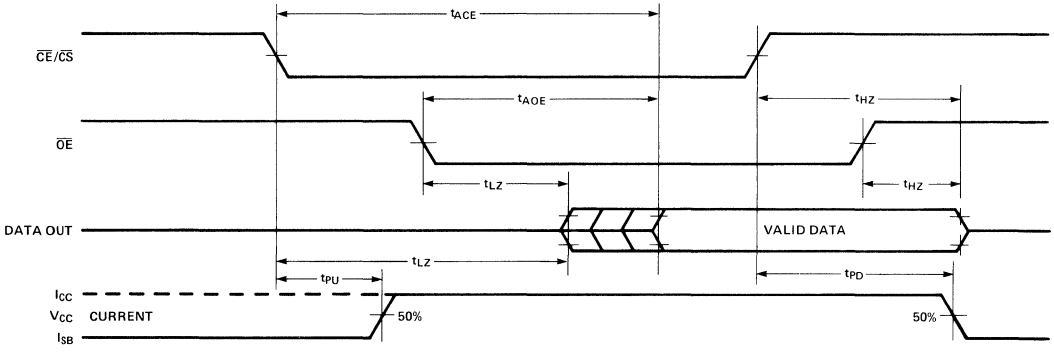
1 R/$\overline{W}$ is high for Read Cycles
2 Device is continuously enabled/selected, $\overline{CE} = V_{IL}$ or $\overline{CS} = V_{IL}$
3 Addresses valid prior to or coincident with $\overline{CE}$ or $\overline{CS}$ transition low
4 If $\overline{CE}$ or $\overline{CS}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state
5 Transition is measured ±500 mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
6 A pullup resistor to V_{CC} on the $\overline{CE}$ or $\overline{CS}$ input is required to keep the device deselected otherwise, power-on current approaches I_{CC} active
7 $\overline{OE}$ can be V_{IH} when contention arbitration mode occurs or V_{IL} when contention override mode occurs, see Tables 2 and 3
8 $\overline{CE}_L = \overline{CE}_R = V_{IL}$ or $\overline{CS}_L = \overline{CS}_R = V_{IL}$
9 Busy timing is identical to Contention Cycle Nos 1 and 2
10 Applies to SY2132 version (power down) only
11 Applies to SY2133 version (non-power down) only
12 The interrupt and busy signals (pins 3, 4, 44 and 45) are open drain outputs A pull-up resistor is required for system operation Load C is used for A C testing these pins All other outputs use load A
13 Read or Write Cycle Timing after $\overline{BUSY}$ inactive as shown in previous timing diagrams

Timing Diagrams

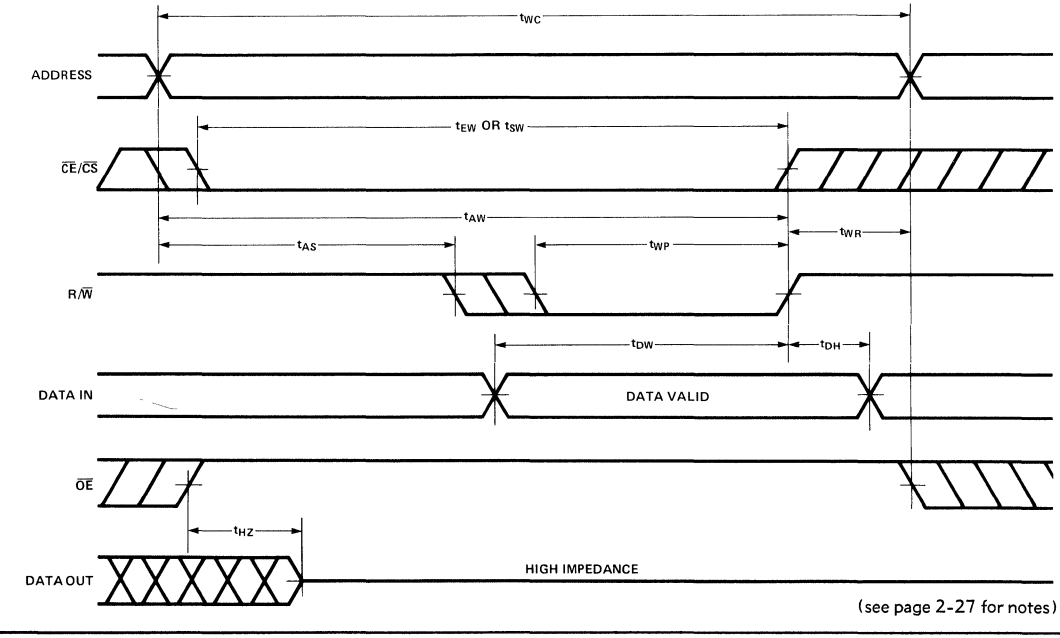
READ CYCLE NO. 1 EITHER SIDE (Notes 1 and 2)



READ CYCLE NO. 2 EITHER SIDE (Notes 1 and 3)

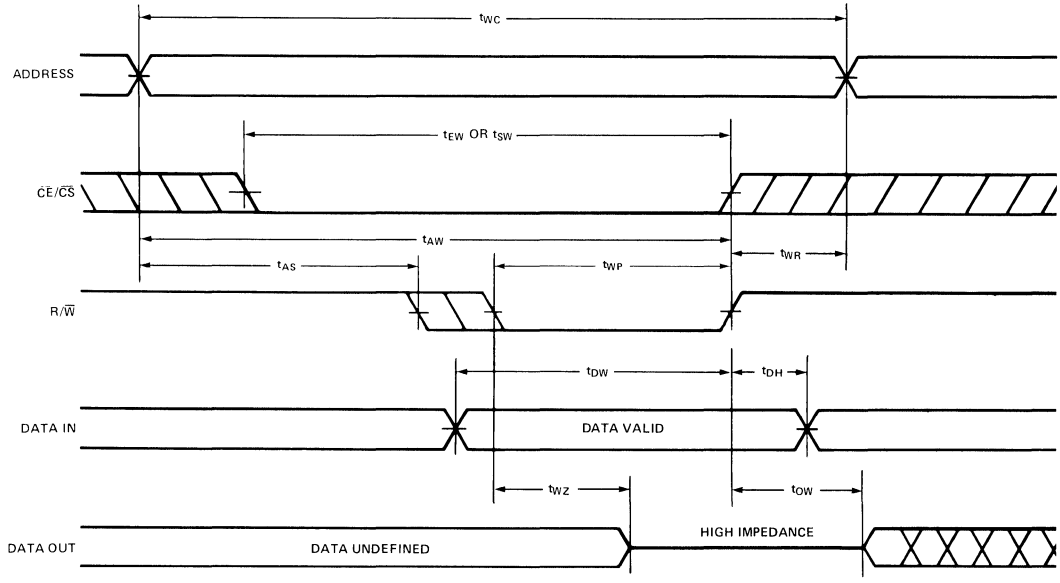


WRITE CYCLE NO. 1 EITHER SIDE (Note 4)



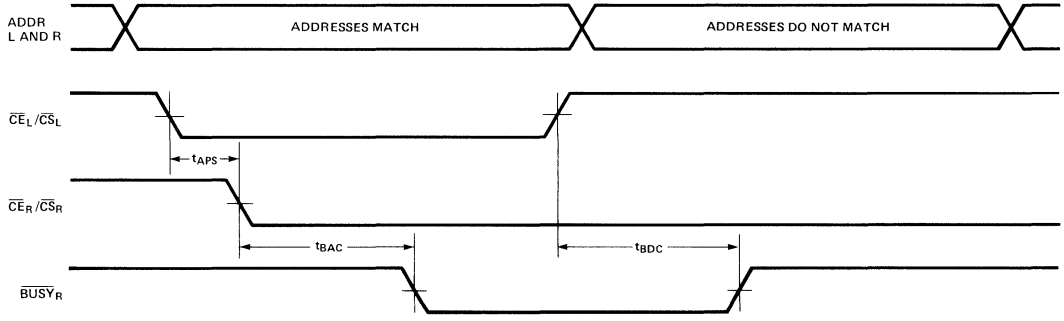
(see page 2-27 for notes)

WRITE CYCLE NO. 2 EITHER SIDE ($\overline{OE}$ = V_{IL}) (Note 4)

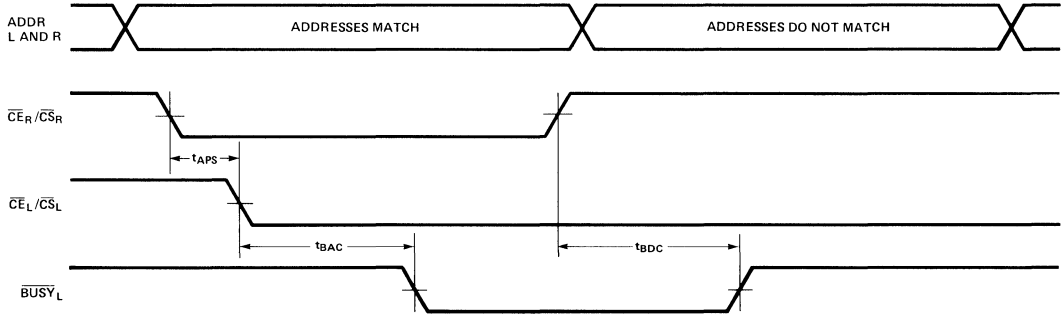


CONTENTION CYCLE NO. 1 ($\overline{CE}$/$\overline{CS}$ CONTENTION ARBITRATION MODE) (Note 7)

$\overline{CE}_L$/$\overline{CS}_L$ VALID FIRST:



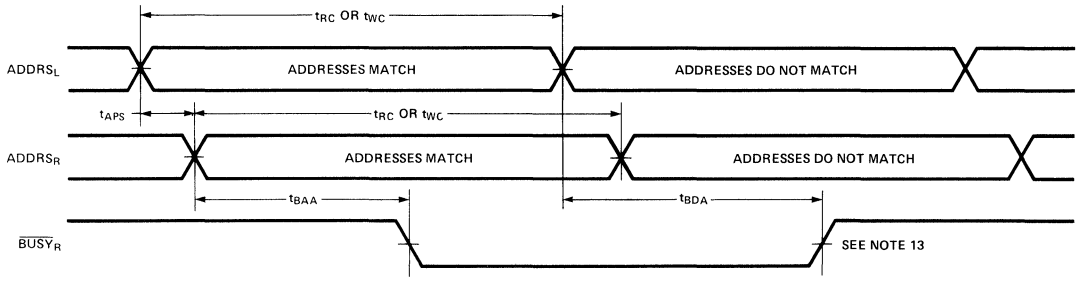
$\overline{CE}_R$/$\overline{CS}_R$ VALID FIRST:



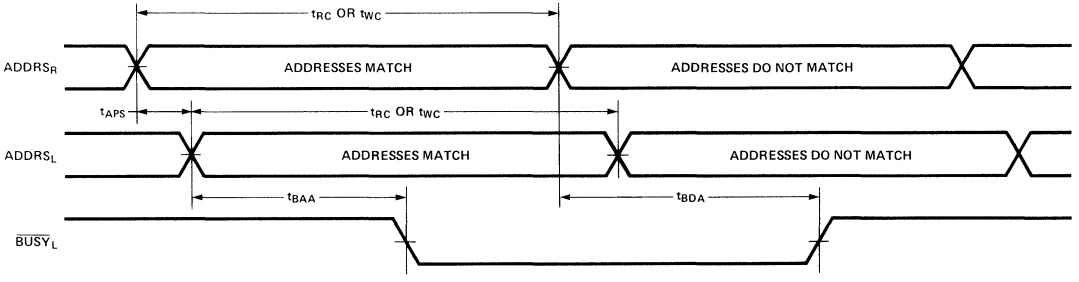
(see page 2-27 for notes)

CONTENTION CYCLE NO. 2 (ADDRESS CONTENTION ARBITRATION MODE) (Notes 7 and 8)

ADDRESS$_L$ VALID FIRST:

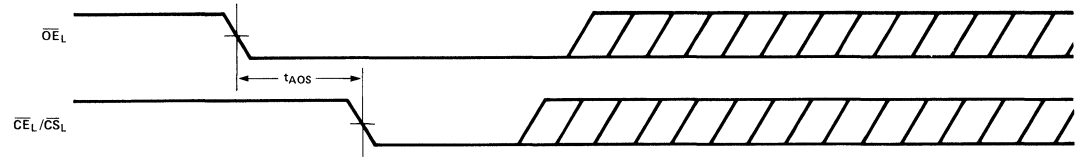


ADDRESS$_R$ VALID FIRST:

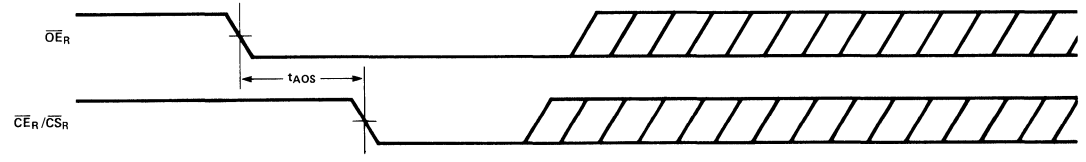


CONTENTION CYCLE NO. 3 (CONTENTION OVERRIDE MODE) (Note 9)

LEFT PORT CONTENTION IGNORED:



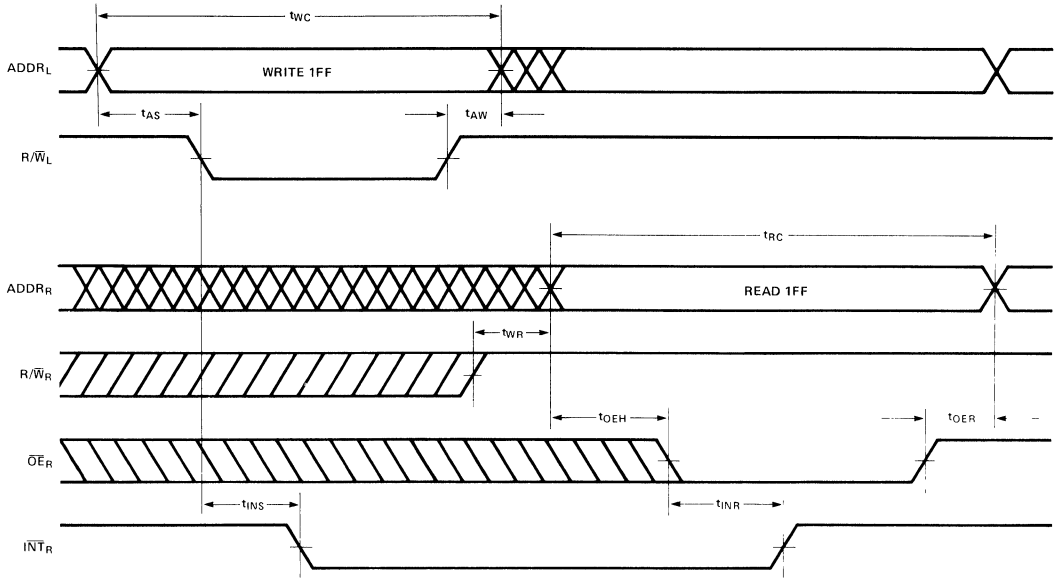
RIGHT PORT CONTENTION IGNORED:



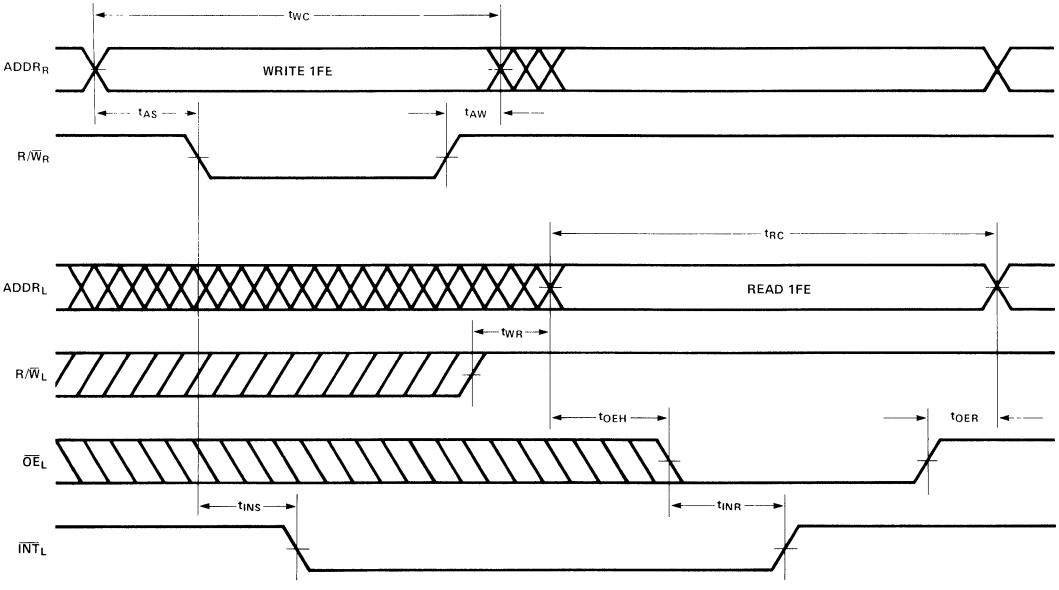
(see page 2-27 for notes)

INTERRUPT MODE (Note 8)

LEFT SIDE FLAGS RIGHT SIDE:



RIGHT SIDE FLAGS LEFT SIDE:



(see page 2-27 for notes)

Functional Description

The SY2132 and SY2133 are 512 word by 8-bit dual port RAMs that feature two separate I/O ports. Each port allows independent access for read or write to any location in the memory.

The SY2132 features separate left and right port Chip Enable controls ($\overline{CE}_L$ and $\overline{CE}_R$). Each Chip Enable activates its respective port when it goes LOW and controls automatic power-down circuitry that allows it's respective side of the device to remain in a standby power mode as long as it remains HIGH. When a port is active, it is allowed access to the entire memory array.

The SY2133 features separate left and right port Chip Select controls ($\overline{CS}_L$ and $\overline{CS}_R$) Each Chip Select activates its respective port when it goes LOW and allows its respective side of the device to remain selected as long as it remains LOW When a port is active, it is allowed access to the entire memory array.

Each port has an Output Enable control ($\overline{OE}_L$ and $\overline{OE}_R$) that keeps its respective output in a high impedance mode when HIGH When a port's $\overline{OE}$ is LOW, that port's output drivers are turned on providing its R/$\overline{W}$ control is HIGH

Separate Read/Write Enable inputs (R/$\overline{W}_L$ and R/$\overline{W}_R$) control writing of new data into any location in the RAM from either port When R/$\overline{W}_L$ is LOW, new data is written into the location selected by the left address field Likewise, when R/$\overline{W}_R$ is LOW, new data is written into the location selected by the right address field. When a port's Read/Write Enable is HIGH, data can be read from that port if its respective $\overline{OE}$ is LOW When R/$\overline{W}_L$ is HIGH and $\overline{OE}_L$ is LOW, data is read from the location selected by the left address field. When R/$\overline{W}_R$ is HIGH and $\overline{OE}_R$ is LOW, data is read from the location selected by the right address field

There is one situation where contention can occur It is when both left and right ports are active and both addresses match Two modes of operation are provided for this situation. (i) on-chip control logic arbitrates the situation, or (ii) contention is ignored and both ports are given access to that memory location $\overline{OE}$ controls the mode of operation

If $\overline{CE}$ or $\overline{CS}$ is LOW before $\overline{OE}$ goes LOW when both addresses match, then on-chip control logic arbitrates the situation Priority is given to the port whose $\overline{CE}$ or $\overline{CS}$ became valid first; the other port will not be allowed access to the memory core until that port's operation is completed

If both port's $\overline{CE}$ or $\overline{CS}$ controls became valid at the same time while their $\overline{OE}$s are HIGH, then the left port is given priority If both $\overline{CE}$ or $\overline{CS}$ pins are valid before their respective $\overline{OE}$ controls and an address change causes an address match while $\overline{OE}$ is HIGH, then priority is given to the port whose address became valid first, the other port is not allowed access to the memory until that port's operation is completed If both addresses became valid at the same time and match, and $\overline{OE}$ is HIGH, then the left port is given priority.

In the other mode, contention is ignored and one or both ports have access to the memory core at all times. This is accomplished by having $\overline{OE}$ LOW when the contention occurs. That is, the RAM core is accessible from a port even if the on-chip control logic would have delayed its access provided. (a) the port's $\overline{OE}$ is LOW when its $\overline{CE}$ or $\overline{CS}$ goes LOW during an address match, or (b) both ports are active and its $\overline{OE}$ is LOW when an address change causes an address match Therefore, it is possible for both ports to have access to the same memory location at the same time, even in a $WRITE_L$-$WRITE_R$ situation

Separate Busy Flags ($\overline{BUSY}_L$ and $\overline{BUSY}_R$) are provided to signal when a port's access to the memory core has been delayed When both ports try to access the same memory location, the on-chip arbitration logic causes the Busy Flag to go LOW on the side that is delayed These flags are provided to allow the user to stop the processor if desired $\overline{BUSY}$ is driven out fast enough for the processor's address and data to be preserved if desired The Busy Flags are operational even when the device is operating in the mode where contention is ignored and function the same as described for contention mode operation This permits their use to signal that contention has occurred and data may have been changed

Interrupt logic is included on-chip to provide a means for two processors to communicate to one another If the left port writes to memory location 1FF, then the right port Interrupt Flag ($\overline{INT}_R$) is latched LOW until the right port reads data from that same location If the right port writes to loation 1FE, then the left port Interrupt Flag ($\overline{INT}_L$) is latched LOW until the left port reads data from that location If both ports are enabled and contention occurs, the Busy circuitry will disable the address decoder from setting or resetting the Interrupt Flags

Table 1. Non-Contention Read/Write Control

Left Port Inputs				Right Ports Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L/\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A8_L$	$R/\overline{W}_R$	$\overline{CE}_R/\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A8_R$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	H	X	X	X	X	X	X	H	X	H	X	Left Port in Power Down Mode
X	X	X	X	X	H	X	X	H	X	H	X	Right Port in Power Down Mode
L	L	X	X	X	X	X	X	H	X	H	X	Data on Left Port Written to Memory Location $A0_L$-$A8_L$
H	L	L	X	X	X	X	X	H	X	H	X	Data in Memory Location $A0_L$-$A8_L$ Output on Left Port
X	X	X	X	L	L	X	X	H	X	H	X	Data on Right Port Written to Memory Location $A0_R$-$A8_R$
X	X	X	X	H	L	L	X	H	X	H	X	Data in Memory Location $A0_R$-$A8_R$ Output on Right Port
L	L	X	1FF	X	X	X	X	H	X	H	L	Left Side Flags Right Side to Read Memory Location 1FF
X	X	X	X	L	L	X	1FE	H	L	H	X	Right Side Flags Left Side to Read Memory Location 1FF

H = HIGH L = LOW X = Don't Care

Table 2. $\overline{CE}/\overline{CS}$ Contention Arbitration

Left Port Inputs			Right Port Inputs			Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L/\overline{CS}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R/\overline{CS}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	L1	X	X	L	LAC	H	X	L	X	Left Operation Allowed RAM Inaccessible from Right
X	L	LAC	X	L1	X	L	X	H	X	Right Operation Allowed RAM Inaccessible from Left
X	Both	X	X	Both	LAC	H	X	L	X	Left Operation Allowed RAM Inaccessible from Right
X	L1	X	X	L	LBC	H	X	L	X	Left Operation Allowed RAM Accessible from Right*
X	L	LBC	X	L1	X	L	X	H	X	Right Operation Allowed RAM Accessible from Left*
X	Both	X	X	Both	LBC	H	X	L	X	Left Operation Allowed RAM Accessible from Right*

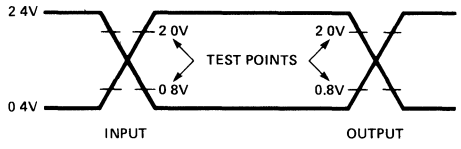
1 = Pin active before equivalent pin on other port
LAC = LOW after chip enable
LBC = LOW before chip enable
Both = Equivalent pins on both ports become active at the same time
*See Contention Override Mode Timing on page 7

Table 3. Address Contention Arbitration

Left Port Inputs				Right Ports Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L/\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A8_L$	$R/\overline{W}_R$	$\overline{CE}_R/\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A8_R$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	L	X	Match1	X	L	X	Match	H	X	L	X	Left Operation Allowed**
X	L	X	Match	X	L	X	Match1	L	X	H	X	Right Operation Allowed**
X	L	X	Both	X	L	X	Both	H	X	L	X	Left Operation Allowed**

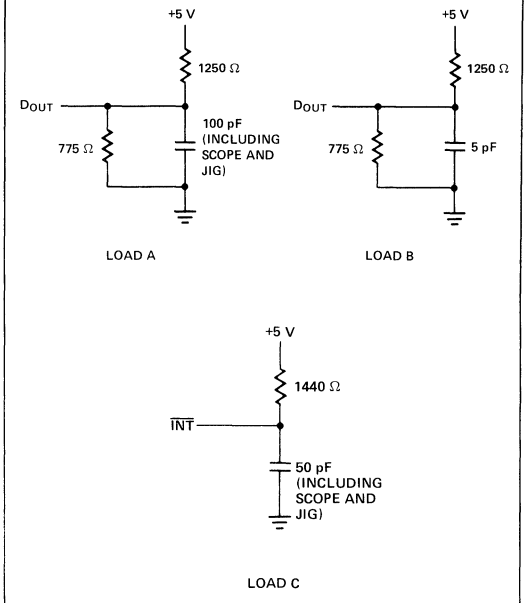
Match = Addresses on left and right ports are identical
Match 1 = Address valid on the port before becoming valid on opposite port
Both = Addresses match and become valid on both ports at the same time
**RAM inaccessible from other port unless that ports $\overline{OE}$ was low when the match occurred Also see Note 7

A.C. Testing Input, Output Waveform



AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2 0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)†	Package Type
SYP2132-1 SYC2132-1	100 ns 100 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2133-1 SYC2133-1	100 ns 100 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic
SYP2132-2 SYC2132-2	120 ns 120 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2133-2 SYC2133-2	120 ns 120 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic
SYP2132-3 SYC2132-3	150 ns 150 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2133-3 SYC2133-3	150 ns 150 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic
SYP2132-4 SYC2132-4	200 ns 200 ns	170 mA 170 mA	40 mA/110 mA 40 mA/110 mA	Molded DIP Ceramic
SYP2133-4 SYC2133-4	200 ns 200 ns	170 mA 170 mA	N A * N A	Molded DIP Ceramic

*Not applicable
†Both ports standby/one port standby

Synertek.

SY2147H

4096 x 1 Static Random Access Memory

Features

- 45 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pinout and Function Compatible to SY2147
- Direct Performance Upgrade for SY2147
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

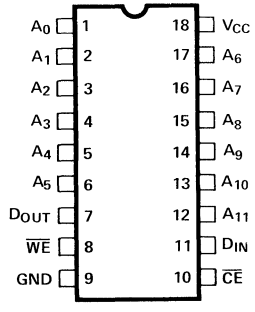
Description

The Synertek SY2147H is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new scaled n-channel silicon gate technology It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data Separate data input and output pins provide maximum design flexibility The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices

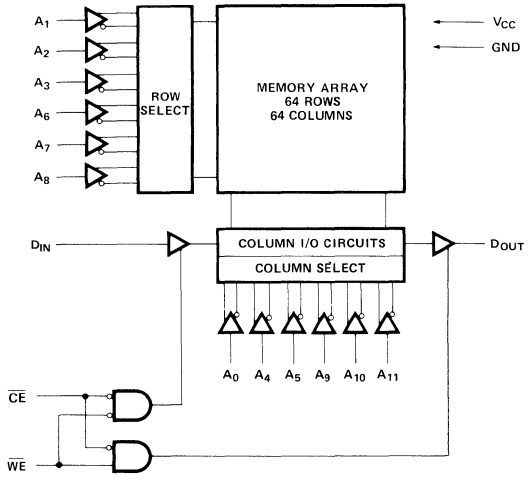
The SY2147H offers an automatic power down feature Power down is controlled by the Chip Enable input When Chip Enable ($\overline{CE}$) goes high, thus deselecting the SY2147H, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high This unique feature provides system level power savings as much as 80%

The SY2147H is packaged in an 18-pin DIP for the highest possible density The device is fully TTL compatible and has a single +5V power supply

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5 V to +7 V
Power Dissipation ..... 1.2 W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 8)

Symbol	Parameter	2147HL/L-3 Min.	2147HL/L-3 Max.	2147H-2/-3 Min.	2147H-2/-3 Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50		50	µA	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{OUT} = Gnd to 4 5V
I_{CC}	Power Supply Current		115 125		150 160	mA mA	T_A = 25°C V_{CC} = Max, $\overline{CE}$ = V_{IL} T_A = 0°C Outputs Open
I_{SB}	Standby Current		15		20	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}
I_{PO}	Peak Power-on Current (Note 9)		15		50	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3 0	0 8	-3 0	0 8	V	
V_{IH}	Input High Voltage	2 0	6 0	2 0	6 0	V	
V_{OL}	Output Low Voltage		0 4		0 4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2 4		2 4		V	I_{OH} = -4 0 mA

Capacitance T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested.

A.C. Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Notes 8, 10)

READ CYCLE

Symbol	Parameter	2147H-2 Min.	2147H-2 Max.	2147H-3/HL-3 Min.	2147H-3/HL-3 Max.	2147H/HL Min.	2147H/HL Max.	Unit	Notes
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACE1}	Chip Enable Access Time		45		55		70	ns	1
t_{ACE2}	Chip Enable Access Time		45		65		80	ns	2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		10		10		ns	7
t_{HZ}	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns	7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		20		20		30	ns	

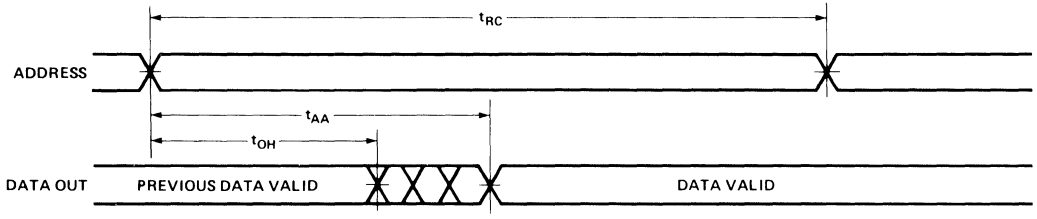
WRITE CYCLE

t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Enabled to End of Write	45		45		55		ns	
t_{AW}	Address Valid to End of Write	45		45		55		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	25		25		40		ns	
t_{WR}	Write Recovery Time	0		10		15		ns	
t_{DW}	Data Valid to End of Write	25		25		30		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	25	0	35	ns	7
t_{OW}	Output Active from End of Write	0		0		0		ns	7

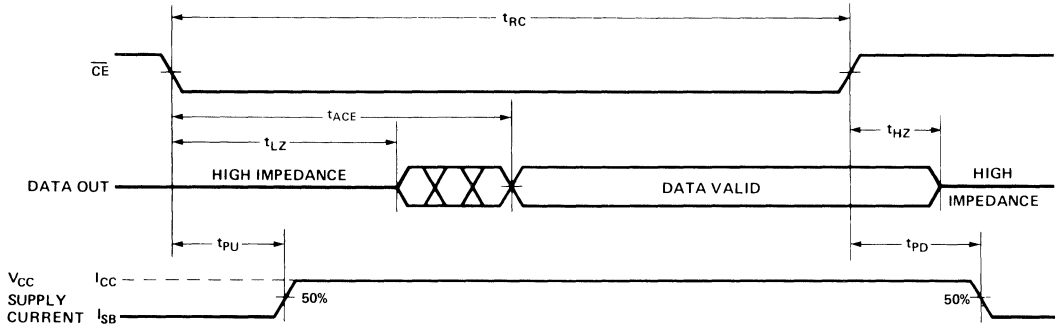
(see following page for notes)

Timing Diagrams

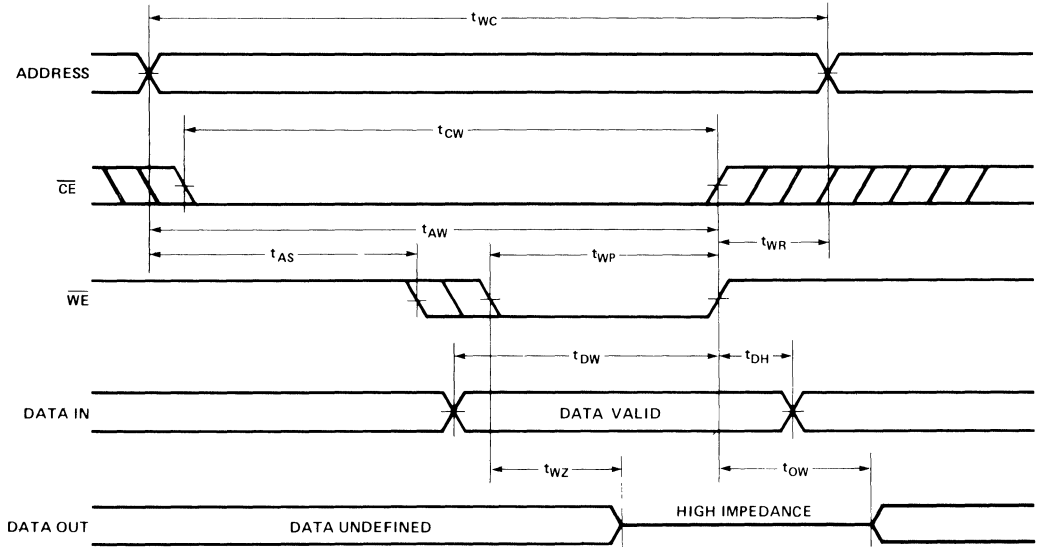
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)

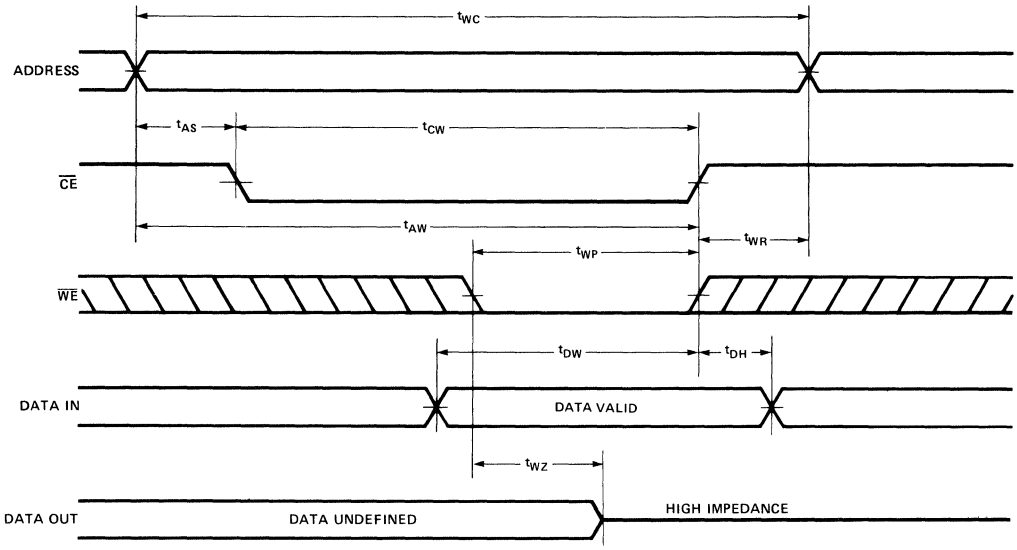


WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)

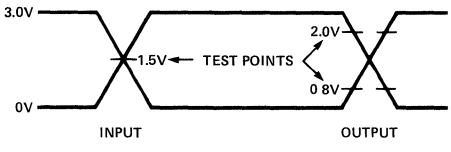


NOTES

1. Chip deselected for greater than 55ns prior to selection
2. Chip deselected for a finite time that is less than 55ns prior to selection (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No 1)
3. $\overline{WE}$ is high for Read Cycles
4. Device is continuously selected, $\overline{CE} = V_{IL}$
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low
6. If $\overline{CE}$ goes high simultaneously with WE high, the outputs remain in the high impedance state
7. Transition is measured ±500mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected otherwise, power-on current approaches I_{CC} active
10. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

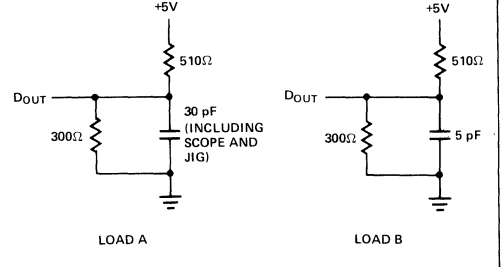


A.C. Testing Input, Output Waveform



A.C. TESTING INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0 0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1 5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availibility

18 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
SYP2147H-2	45ns	160mA	30mA	Molded DIP
SYP2147H-3	55ns	160mA	30mA	Molded DIP
SYP2147HL-3	55ns	125mA	15mA	Molded DIP
SYP2147H	70ns	160mA	20mA	Molded DIP
SYP2147HL	70ns	125mA	15mA	Molded DIP

Synertek.

SY2148H

1024 x 4 Static Random Access Memory

Features

- 45 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pinout and Function Compatible to SY2148
- Performance Upgrade for SY2148
- Industry Standard 2114 Pinout
- Totally TTL Compatible all Inputs and Outputs
- Common Data Input and Output
- High Density 18-Pin Package
- Three-State Output

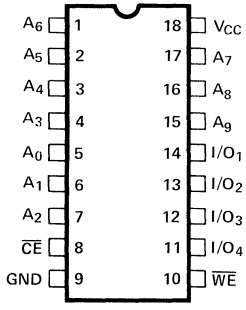
Description

The Synertek SY2148H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new scaled n-channel silicon gate technology It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data Common data input and output pins provide maximum design flexibility The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

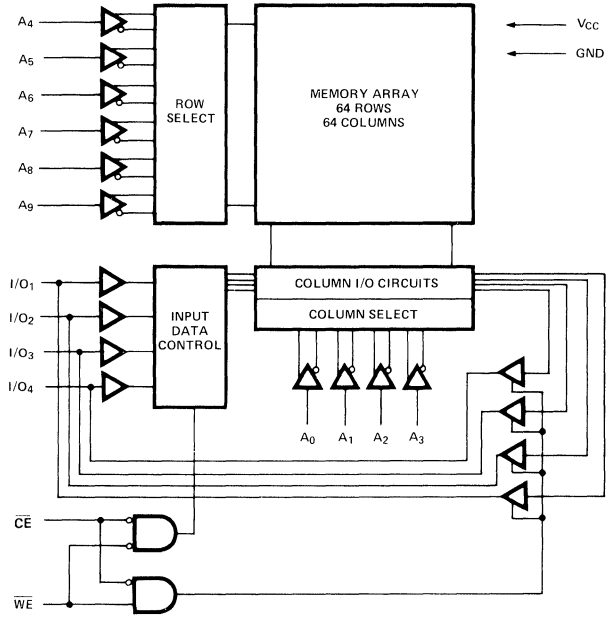
The SY2148 offers an automatic power down feature Power down is controlled by the Chip Enable input When Chip Enable ($\overline{CE}$) goes high, thus deselecting the SYM2148H, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high This unique feature provides system level power savings as much as 85%.

The SY2148H is packaged in an 18-pin DIP for the highest possible density The device is fully TTL compatible and has a single +5V power supply

Pin Configuration



Block Diagram



MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

D.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (note 8)

Symbol	Parameter	2148H/H-2/H-3 Min.	2148H/H-2/H-3 Max.	2148HL/HL-3 Min.	2148HL/HL-3 Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50		50	µA	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		140		115	mA	T_A = 25°C; V_{CC} = Max, $\overline{CE}$ = V_{IL}, Outputs Open
			150		125	mA	T_A = 0°C; V_{CC} = Max, $\overline{CE}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		30		20	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}
I_{PO}	Peak Power-on Current (Note 9)		50		30	mA	V_{CC} = Gnd to V_{CC} Min, $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = -4mA

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (note 8)

READ CYCLE

Symbol	Parameter	2148H-2 Min.	2148H-2 Max.	2148H-3/HL-3 Min.	2148H-3/HL-3 Max.	2148H/HL Min.	2148H/HL Max.	Unit	Conditions
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
tACE1	Chip Enable Access Time		45		55		70	ns	Note 1
tACE2	Chip Enable Access time		55		65		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		10		10		ns	Note 7
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	Note 7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

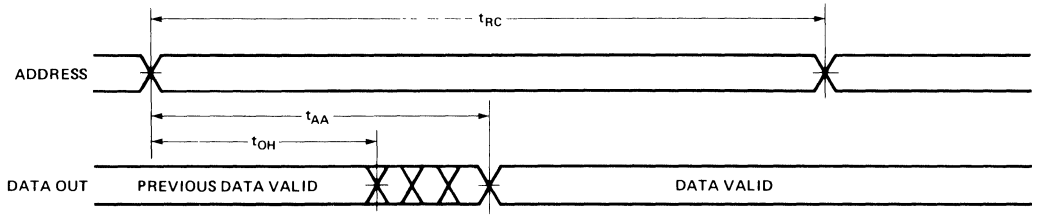
WRITE CYCLE

t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Enabled to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	Note 7
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 7

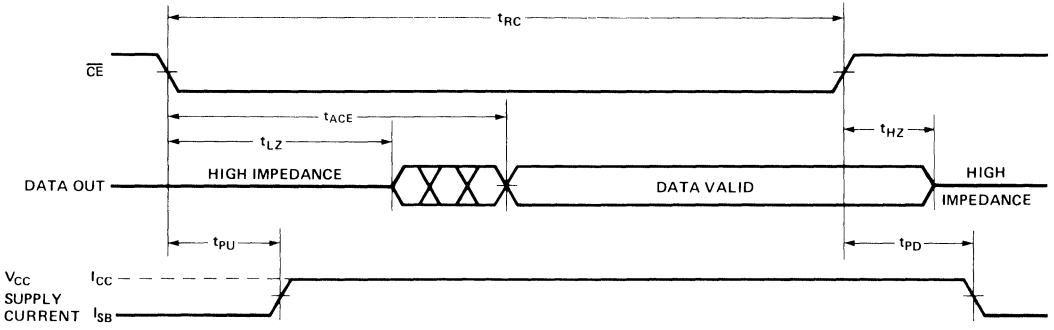
(See following page for notes)

Timing Diagrams

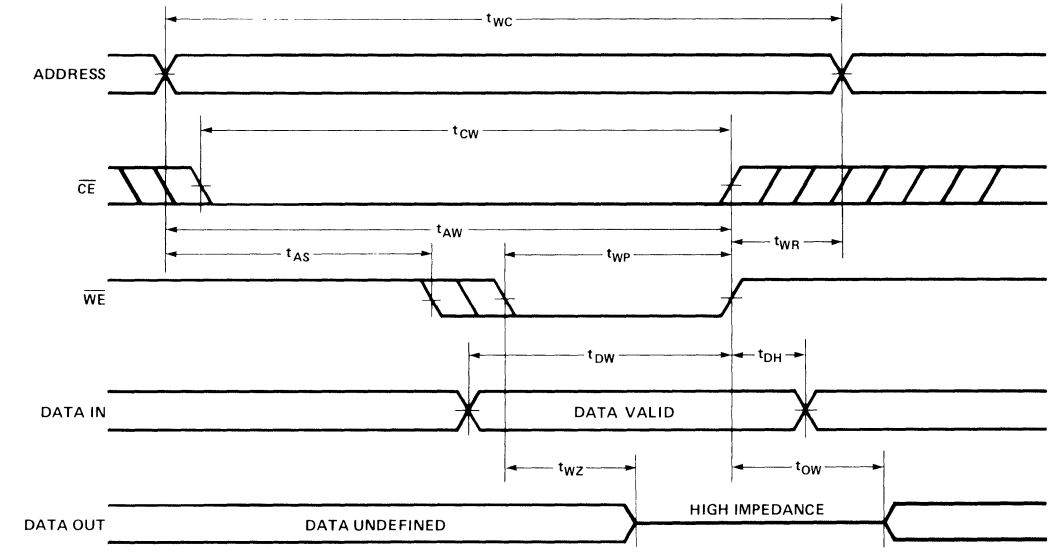
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)



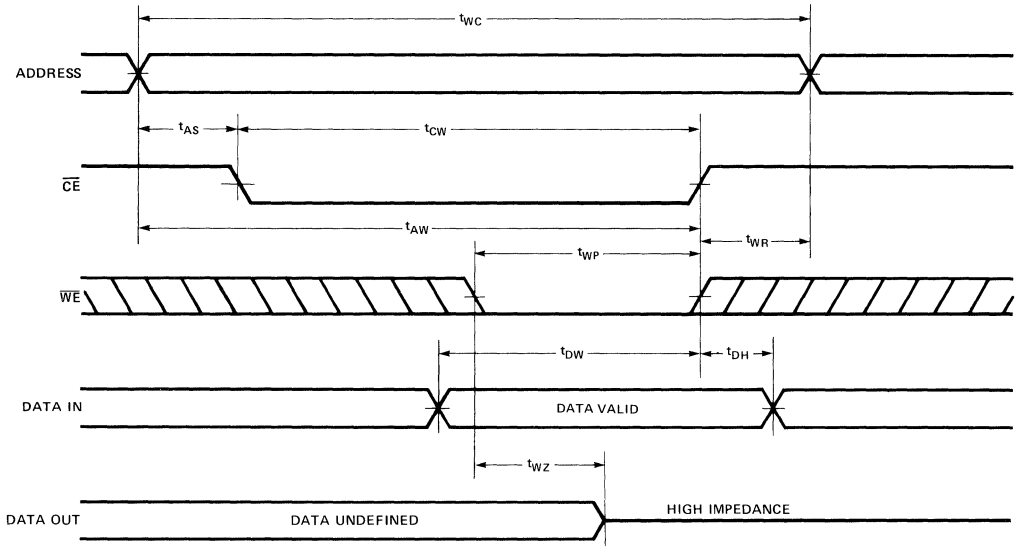
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



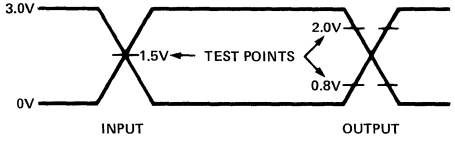
NOTES

1. Chip deselected for greater than 55ns prior to selection
2. Chip deselected for a finite time that is less than 55ns prior to selection (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No 1)
3. WE is high for Read Cycles
4. Device is continuously selected, $\overline{CE} = V_{IL}$
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low
6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
7. Transition is measured ±500mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected otherwise, power-on current approaches I_{CC} active
10. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (NOTE 6)

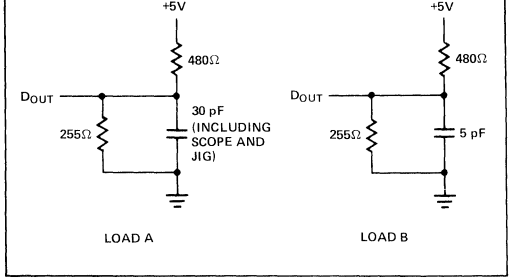


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability

18 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
SYP2148H	70ns	150mA	30mA	Molded DIP
SYP2148H-2	45ns	150mA	30mA	Molded DIP
SYP2148H-3	55ns	150mA	30mA	Molded DIP
SYP2148HL	70ns	125mA	20mA	Molded DIP
SYP2148HL-3	55ns	125mA	20mA	Molded DIP

Synertek.

SY2149H

1024 x 4 Static Random Access Memory

Features

- 45 ns Maximum Address Access
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access Time: 20ns Max.
- Identical Cycle and Access Times
- Single +5V Supply
- Industry Standard 2114 Pinout
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Outputs
- High Density 18-Pin Package
- Three-State Output

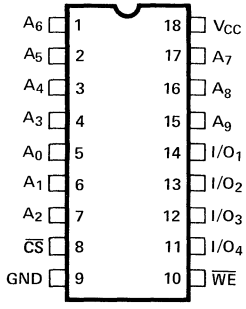
Description

The Synertek SY2149H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

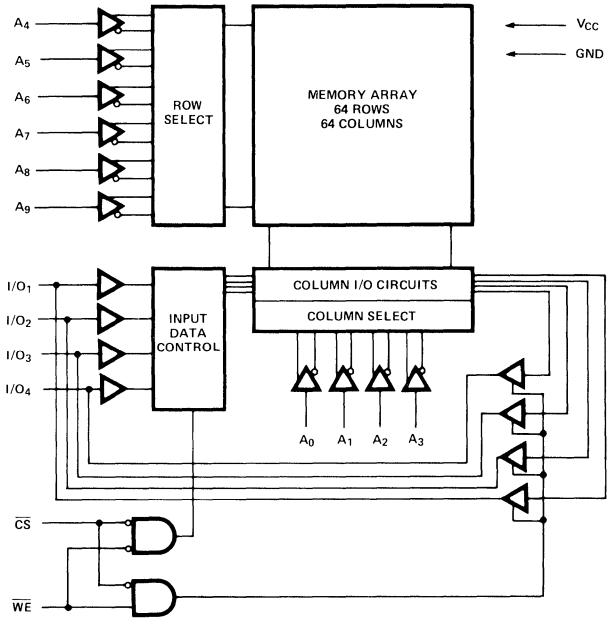
The SY2149H offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

The SY2149H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 6)

Symbol	Parameter	2149HL-3, 2149HL Min.	2149HL-3, 2149HL Max.	2149H-2, 2149H-3, 2149H Min.	2149H-2, 2149H-3, 2149H Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins).		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		115		140	mA	T_A = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs Open
			125		150	mA	T_A = 0°C; V_{CC} = Max, $\overline{CS}$ = V_{IL} Outputs Open
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = -4.0 mA
I_{OS}	Output Short Circuit Current		±200		±200	mA	V_{OUT} = GND to V_{CC} (Note 7)

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Notes 6, 8)

READ CYCLE

Symbol	Parameter	2149H-2 Min.	2149H-2 Max.	2149HL-3 2149H-3 Min.	2149HL-3 2149H-3 Max.	2149HL 2149H Min.	2149HL 2149H Max.	Unit	Conditions
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACS}	Chip Select Access Time		20		25		30	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		5		5		ns	Note 5
t_{HZ}	Chip Deselectio to Output in High Z	0	15	0	15	0	15	ns	Note 5

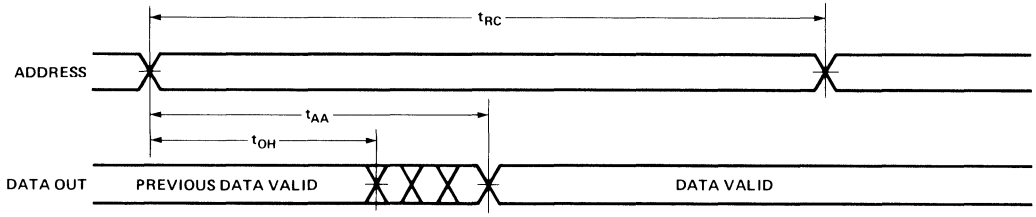
WRITE CYCLE

t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Selection to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 5

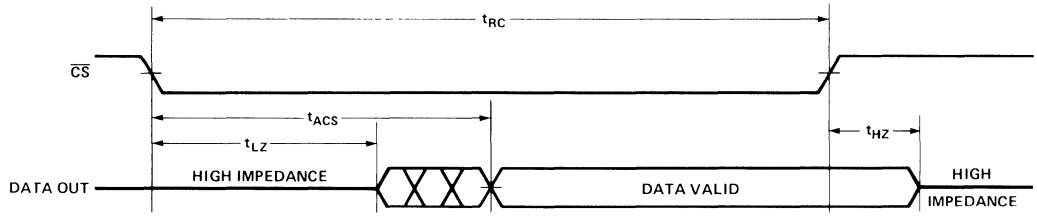
(See following page for notes)

Timing Diagrams

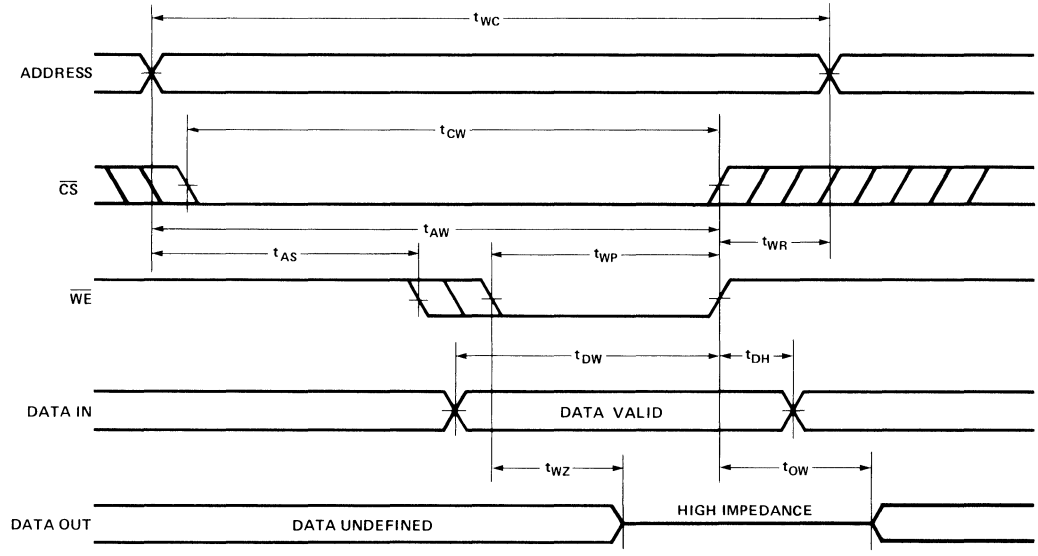
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



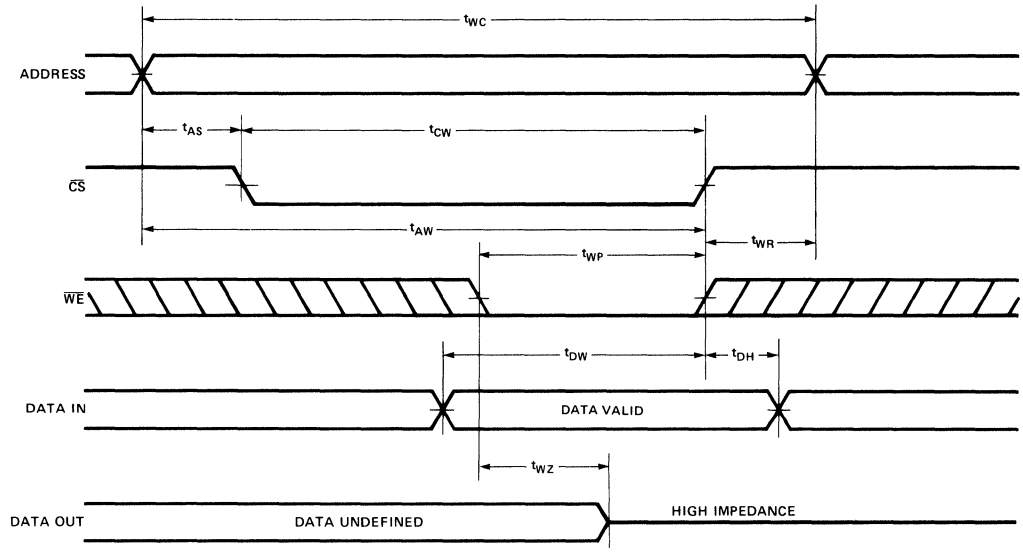
WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 4)



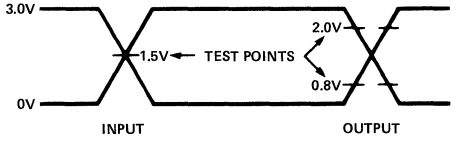
NOTES:

1 $\overline{WE}$ is high for Read Cycles.
2 Device is continuously selected, $\overline{CS} = V_{IL}$
3 Addresses valid
4 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
5 Transition is measured ±500 mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
6 The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
7 Duration not to exceed one minute
8 A minimum 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

WRITE CYCLE NO. 2 ($\overline{CS}$ controlled) (Note 4)

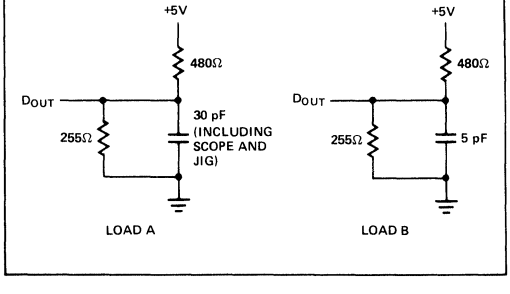


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0 0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability 18 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max.)	Supply Current (Max.)	Package Type
SYP2149H-2	45nsec	150mA	Molded DIP
SYP2149H-3	55nsec	150mA	Molded DIP
SYP2149HL-3	55nsec	125mA	Molded DIP
SYP2149H	70nsec	150mA	Molded DIP
SYP2149HL	70nsec	125mA	Molded DIP

Synertek

SY2150
Cache Address Comparator

ADVANCED INFORMATION

Features

- Fast Address to Match Valid Delay — Two Speed Ranges. 45 ns, 55 ns
- 512 x 9 Internal RAM
- 300-Mil 24-Pin Ceramic Side Brazed Package
- Maximum Power Dissipation· 660 mW
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static, TTL Compatible

Description

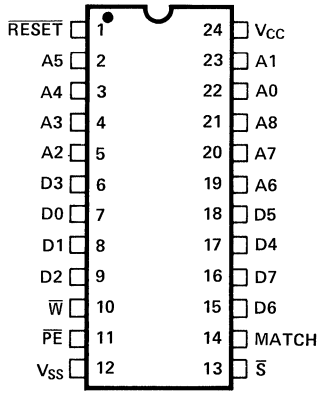
The 8-bit slice cache address comparator consists of a high-speed 512 x 9 static RAM array, parity generator, and parity checker, and 9-bit high-speed comparator It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity An equality is indicated by a high level on the MATCH output A low-level output from $\overline{PE}$ signifies a parity ity error in the internal RAM data $\overline{PE}$ is an N-channel open drain output for easy OR-tieing During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low

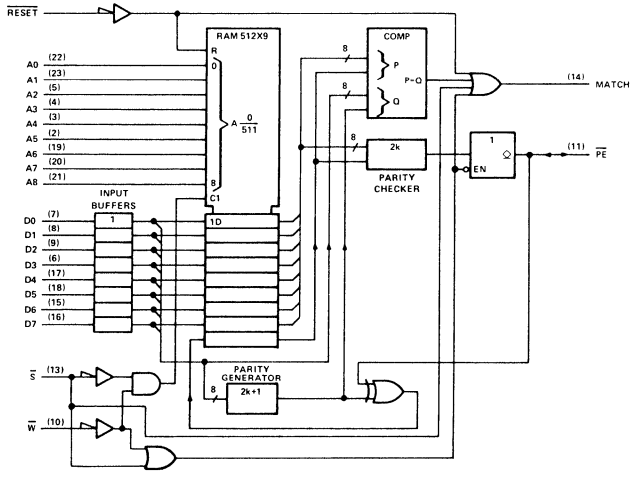
A $\overline{RESET}$ input is provided for initialization When $\overline{RESET}$ goes low, all 512 x 9 RAM locations will be cleared and the MATCH output will be forced high

The cache address comparator operates from a single +5 V supply and is offered in a 24-pin 300-mil side brazed package The device is fully TTL compatible and is guaranteed to operate from 0° to 70° C

Pin Configuration



Block Diagram



MEMORIES

Synertek.

SY2158

1024 x 8 Static Random Access Memory

Features

- 120nsec Maximum Access Time
- Fully Static Operation: No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (± 10%)
- Pin Compatible with 2716 16K EPROM
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- Output Enable Function ($\overline{OE}$)

Description

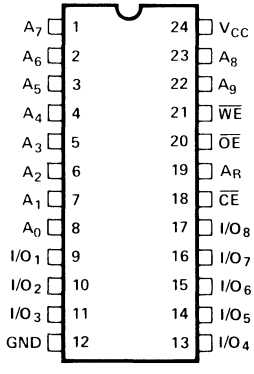
The Synertek SY2158 is a 8192 bit static Random Access Memory organized 1024 words by eight bits and is fabricated using Synertek's new scaled n-channel silicon gate technology It is designed using fully static circuitry, therefore requiring no clocks or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus

The SY2158 offers an automatic power down feature under the control of the chip enable ($\overline{CE}$) input When $\overline{CE}$ goes high, deselecting the chip, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This feature provides significant system level power savings.

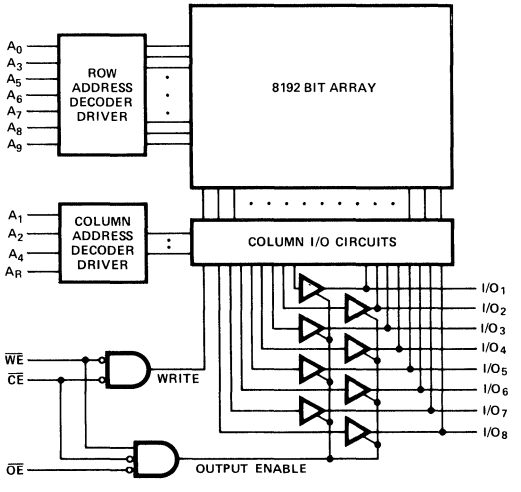
The SY2158 is available in two versions. For the "A" version, the select reference input (A_R) must be at V_{IL} and for the "B" version A_R must be at V_{IH}.

The SY2158 is pin compatible with 16K ROMs, EPROMs and E^2PROMs thus offering the user the flexibility of switching between RAM, ROM, EPROM, and E^2PROM with a minimum of board layout changes.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin with Respect to Ground ..... -3 5V to +7V
Power Dissipation 1 0W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified)

Symbol	Parameter	2158-2/-3/-4 Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{OUT} = Gnd to 4 5V
I_{CC}	Power Supply Current		95	mA	T_A = 25°C; V_{CC} = Max, $\overline{CE}$ = V_{IL}
			100	mA	T_A = 0°C; Outputs Open
I_{SB}	Standby Current		20	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}
I_{PO}	Peak Power-on Current Note 6		40	mA	V_{CC} = Gnd to V_{CC} Min, $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3 0	0 8	V	
V_{IH}	Input High Voltage	2.0	6 0	V	
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 3 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1.0 mA

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Note 7)

READ CYCLE

Symbol	Parameter	2158-2 Min.	2158-2 Max.	2158-3 Min.	2158-3 Max.	2158-4 Min.	2158-4 Max.	Unit	Conditions
t_{RC}	Read Cycle Time	120		150		200		ns	
t_{AA}	Address Access Time		120		150		200	ns	
t_{ACE}	Chip Enable Access Time		120		150		200	ns	
t_{AOE}	Output Enable Access Time		50		60		70	ns	
t_{OH}	Output Hold from Address Change	10		10		10		ns	
t_{LZ}	Output Low Z Time	10		10		10		ns	Note 5
t_{HZ}	Output High Z Time	0	40	0	50	0	60	ns	Note 5
t_{PU}	Chip Enable to Power Up Time	0		0		0		ns	
t_{PD}	Chip Disable to Power Down Time		60		80		100	ns	

WRITE CYCLE

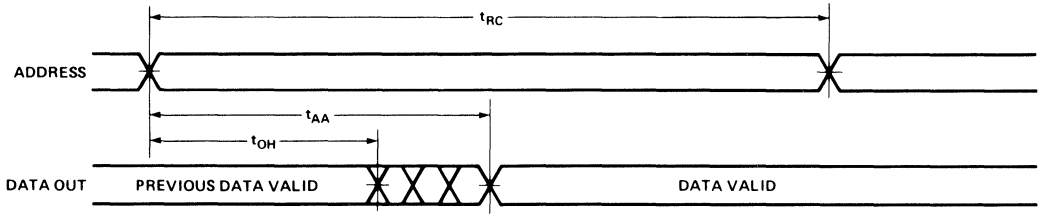
t_{WC}	Write Cycle Time	120		150		200		ns	
t_{CW}	Chip Enable to End of Write	90		120		150		ns	
t_{AW}	Address Valid to End of Write	90		120		150		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	70		90		120		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DW}	Data Valid to End of Write	50		70		90		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	40	0	50	0	60	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 5

(See following page for notes)

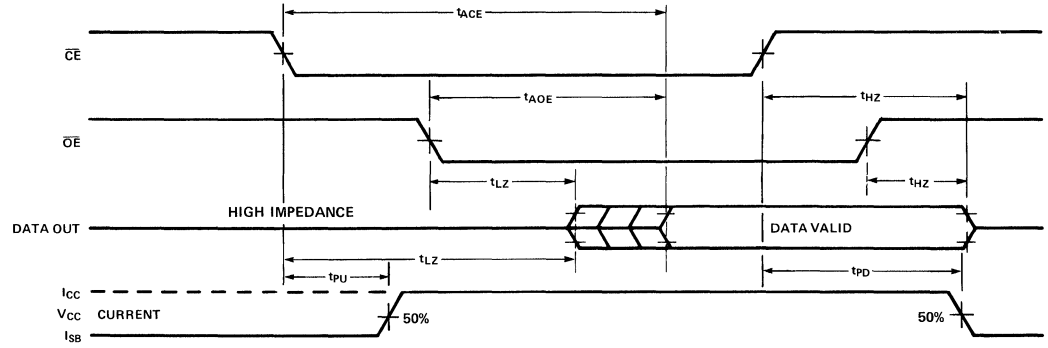
MEMORIES

Timing Diagrams

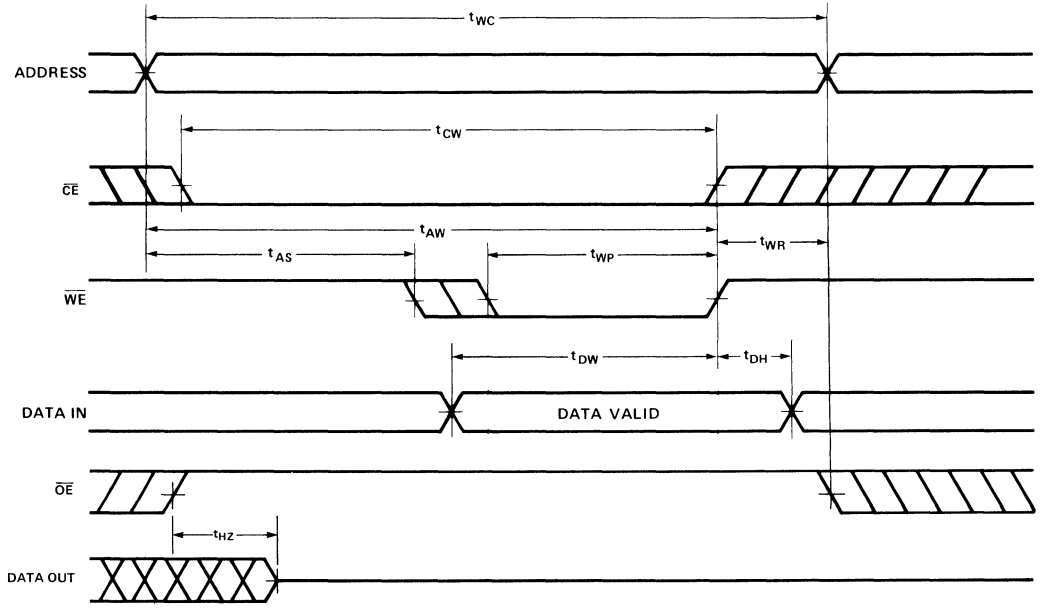
READ CYCLE NO. 1 (NOTES 1 and 2)



READ CYCLE NO. 2 (NOTES 1 and 3)



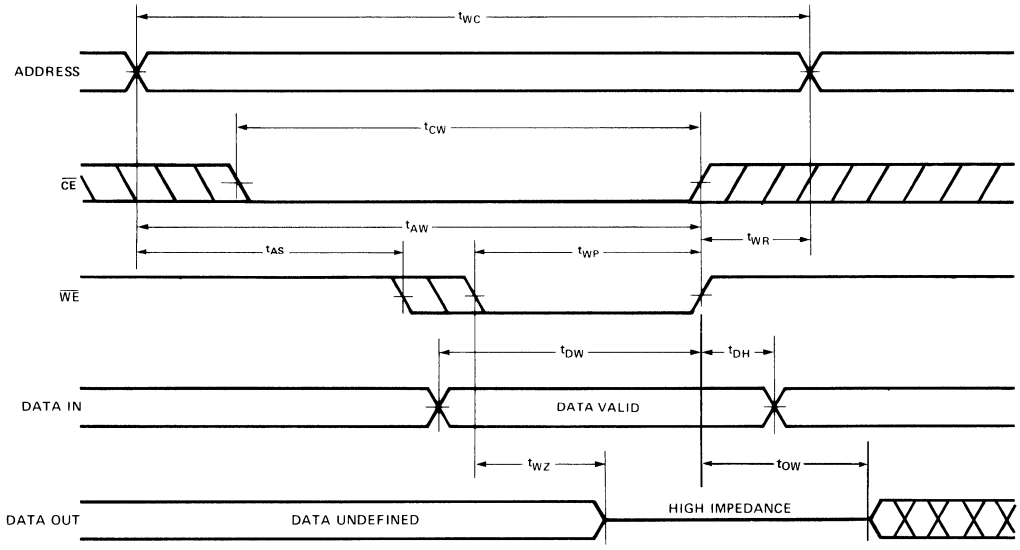
WRITE CYCLE NO. 1 (NOTE 4)



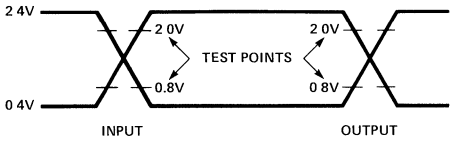
Notes:

1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CE} = \overline{OE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

WRITE CYCLE NO. 2 ($\overline{OE}$ = V_{IL}) (NOTE 4)

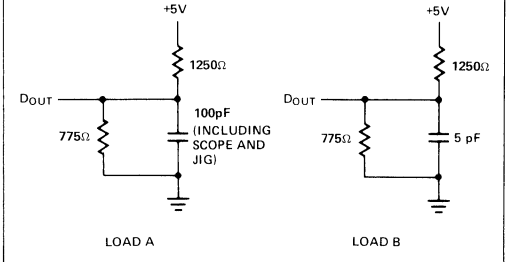


A.C. Testing Input, Output Waveform



AC TESTING INPUTS ARE DRIVEN AT 2 4V FOR A LOGIC "1" AND 0 4V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" INPUT PULSE RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Package Availability

24 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type	A_R
SYP2158A-2	120ns	100mA	20mA	Molded DIP	IL
SYP2158A-3	150ns	100mA	20mA	Molded DIP	V_{IL}
SYP2158A-4	200ns	100mA	20mA	Molded DIP	V_{IL}
SYP2158B-4	120ns	100mA	20mA	Molded DIP	V_{IL}
SYP2158B-3	150ns	100mA	20mA	Molded DIP	V_{IL}
SYP2158B-2	200ns	100mA	20mA	Molded DIP	V_{IL}

Synertek.

SY2167

16,384 x 1 Static Random Access Memory

ADVANCED INFORMATION

Features

- 45 nsec Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 20 Pin Package
- Three-State Output

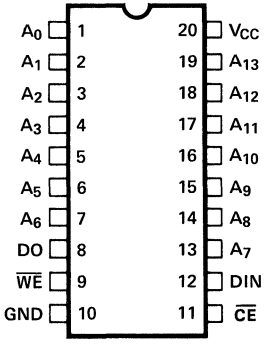
Description

The Synertek SY2167 is a 16,384-Bit Static Random Access Memory organized 16,384 words by 1-bit and is fabricated using Synertek's new N-Channel Double Polysilicon Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibilty The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

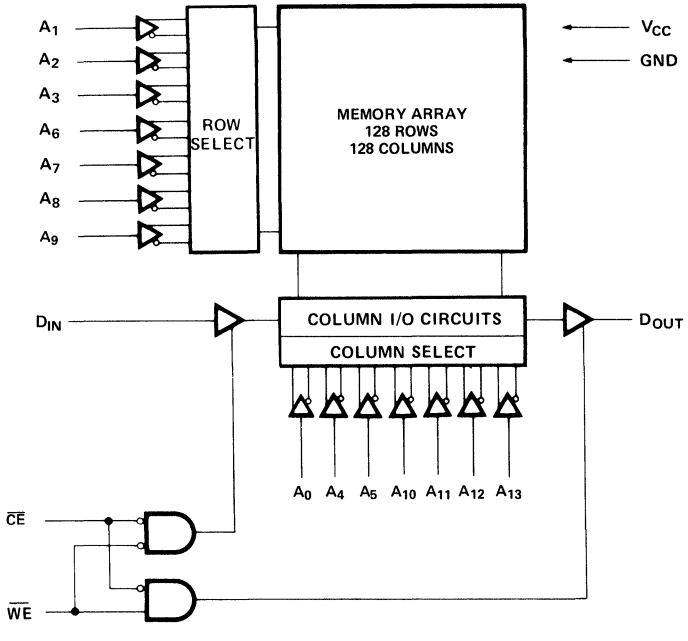
The SY2167 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus de-selecting the SY2167, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 80%.

The SY2167 is packaged in a 20-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin with
Respect to Ground ..... -3 5V to +7V
Power Dissipation 1 2W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max V_{OUT} = Gnd to 4 5V
I_{CC}	Power Supply Current		110	mA	$T_A = 25°C$ | V_{CC} = Max, $\overline{CE} = V_{IL}$
			120	mA	$T_A = 0°C$ | Outputs Open
I_{SB}	Standby Current		20	mA	V_{CC} = Min to Max $\overline{CE} = V_{IH}$
I_{PO}	Peak Power-on Current (Note 7)		50	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3 0	0 8	V	
V_{IH}	Input High Voltage	2 0	6 0	V	
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 16 mA
V_{OH}	Output High Voltage	2 4		V	I_{OH} = -4 0 mA
I_{OS}	Output Short Circuit Current (Note 8)	-150	300	mA	V_{OUT} = GND to V_{CC} (Note 8)

Capacitance $T_A = 25°C$, f = 1 0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested

A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Notes 6, 9)

READ CYCLE

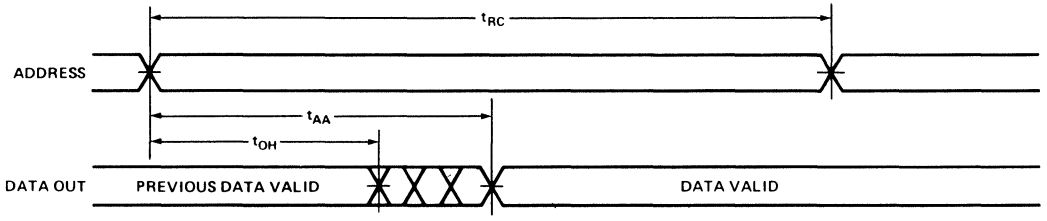
		2167		2167-3		2167-2		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{RC}	Read Cycle Time	70		55		45		ns
t_{AA}	Address Access Time		65		55		45	ns
t_{ACE}	Chip Enable Access Time		70		50		40	ns
t_{OH}	Output Hold from Address Change	5		5		3		ns
t_{LZ}	Chip Selection to Output in Low Z	5		5		5		ns
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	30	0	25	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		70		55		45	ns

WRITE CYCLE

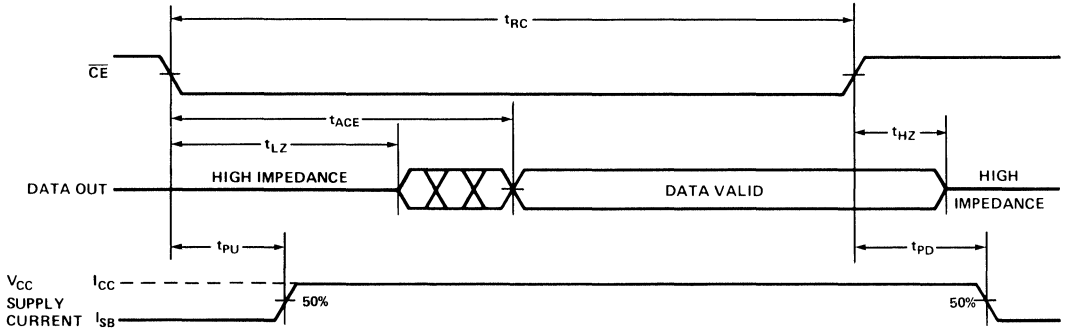
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{WC}	Write Cycle Time	70		55		45		ns
t_{CW}	Chip Enabled to End of Write	65		50		40		ns
t_{AW}	Address Valid to End of Write	65		50		40		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	35		25		20		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	30		20		15		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enabled to Output in High Z	0	35	0	25	0	20	ns
t_{OW}	Output Active from End of Write	0	40	0	30	0	25	ns

Timing Diagrams

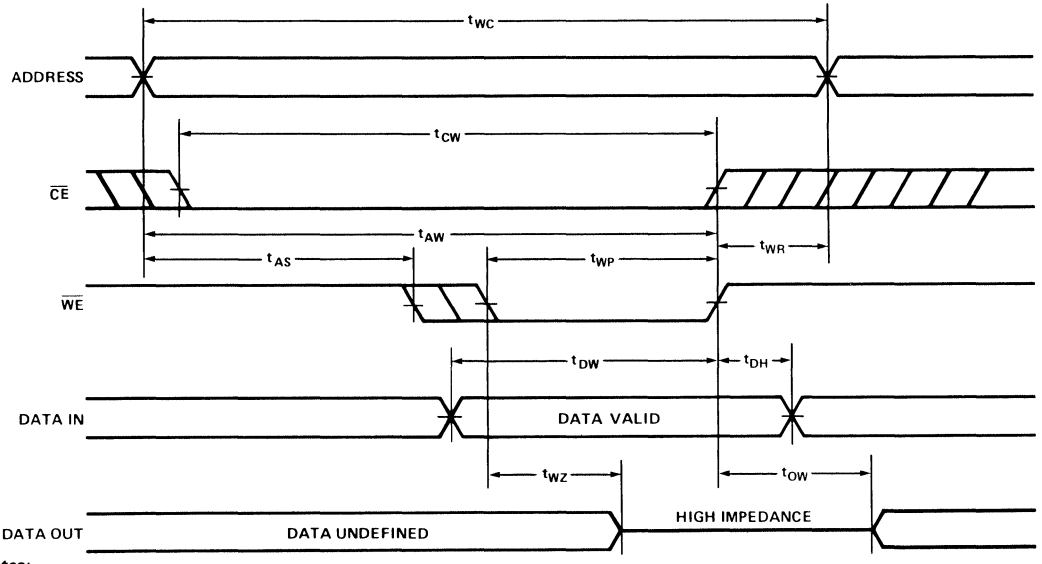
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



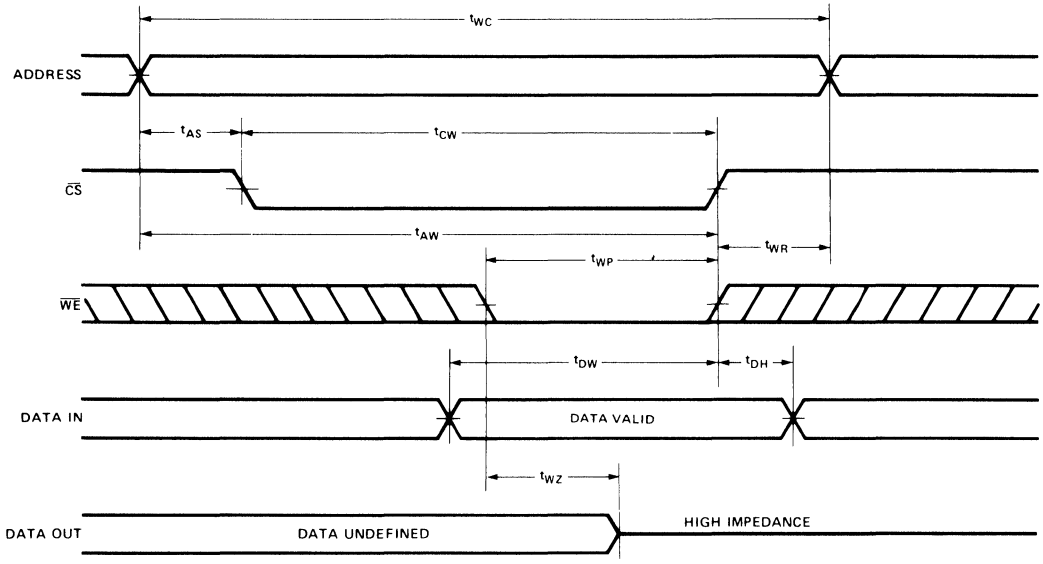
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled) (Note 4)



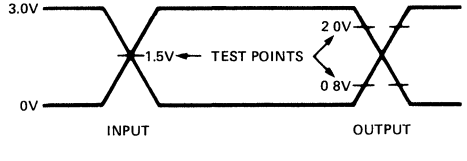
Notes:

1. $\overline{WE}$ is high for Read Cycles
2. Device is continuously selected, $\overline{CE} = V_{IL}$
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
5. Transition is measured ±500 mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
7. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected otherwise, power-on current approaches I_{CC} active
8. Duration not to exceed one second
9. A minimum 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled) (Note 4)

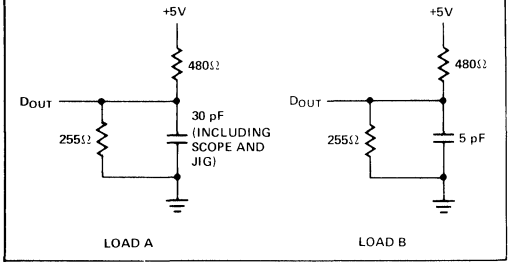


A.C. Testing Input, Output Waveform



A.C TESTING INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS THE INPUTS ARE MEASURED AT 1.5V INPUT RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Package Availability 20 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYP2167-70	70 ns	120 mA	20 mA	Molded DIP
SYP2167-55	55 ns	120 mA	20 mA	Molded DIP
SYP2167-45	45 ns	120 mA	20 mA	Molded DIP

Synertek.

SY2168

4096 x 4 Static Random Access Memory

ADVANCED INFORMATION

Features

- 45 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- JEDEC Standard Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 20-Pin Package
- Three-State Output

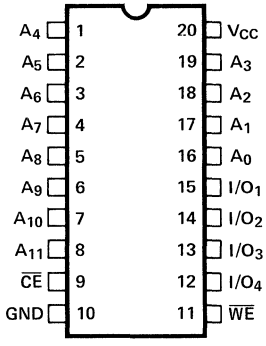
Description

The Synertek SY2168 is a 16,384-Bit Static Random Access Memory organized 4096 words by 4 bits and is fabricated using Synertek's scaled n-channel double poly silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

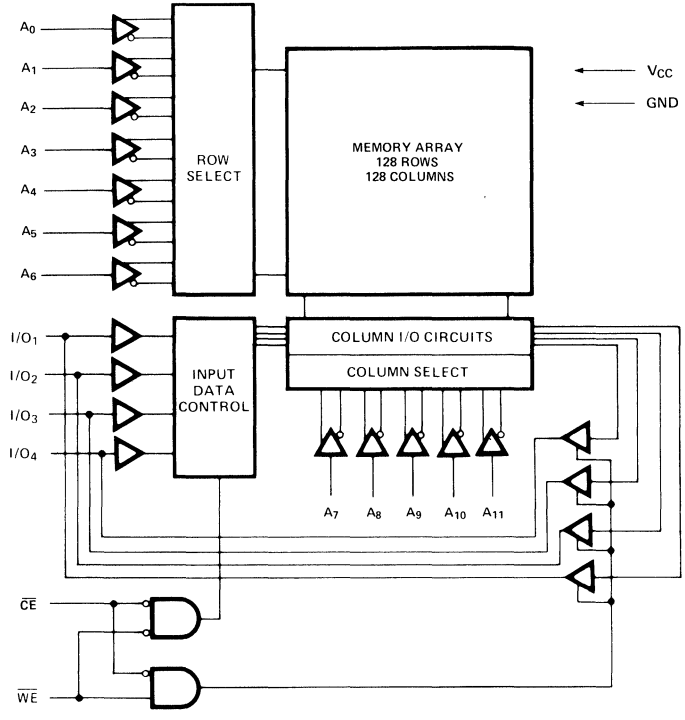
The SY2168 offers an automatic power down feature Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus de-selecting the SY2168, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 85%.

The SY2168 is packaged in a 20-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max V_{OUT} = Gnd to 4 5V
I_{CC}	Power Supply Current		110	mA	$T_A = 25°C$ | V_{CC} = Max, $\overline{CE} = V_{IL}$
			120	mA	$T_A = 0°C$ | Outputs Open
I_{SB}	Standby Current		30	mA	V_{CC} = Min to Max, $\overline{CE} = V_{IH}$
I_{PO}	Peak Power-on Current (Note 7)		50	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3 0	0 8	V	
V_{IH}	Input High Voltage	2 0	6 0	V	
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2 4		V	I_{OH} = -4 mA
I_{OS}	Output Short Circuit Current	−200	+200	mA	V_{OUT} = GND to V_{CC} (Note 9)

Capacitance $T_A = 25°C$, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested

A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Notes 6, 8)

READ CYCLE

		2168-3		2168		2168-2	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.
t_{RC}	Read Cycle Time	55		70		45	
t_{AA}	Address Access Time		55		70		45
t_{ACE}	Chip Enable Access Time		45		50		40
t_{OH}	Output Hold from Address Change	3		5		3	
t_{LZ}	Chip Selection to Output in Low Z	20		20		20	
t_{HZ}	Chip Deselection to Output in High Z	0	25	0	30	0	20
t_{PU}	Chip Selection to Power Up Time	0		0		0	
t_{PD}	Chip Deselection to Power Down Time		55		70		45

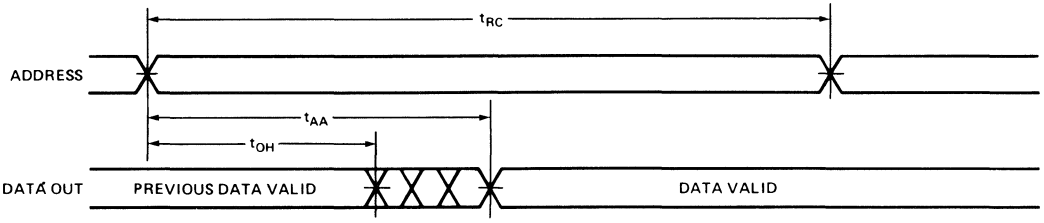
WRITE CYCLE

Symbol	Parameter	Min.	Max.	Min.	Max	Min.	Max.
t_{WC}	Write Cycle Time	55		70		45	
t_{CW}	Chip Enabled to End of Write	45		60		35	
t_{AW}	Address Valid to End of Write	45		60		35	
t_{AS}	Address Setup Time	0		0		0	
t_{WP}	Write Pulse Width	45		60		35	
t_{WR}	Write Recovery Time	3		5		3	
t_{DW}	Data Valid to End of Write	20		25		15	
t_{DH}	Data Hold Time	0		0		0	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	30	0	20
t_{OW}	Output Active from End of Write	0		0		0	

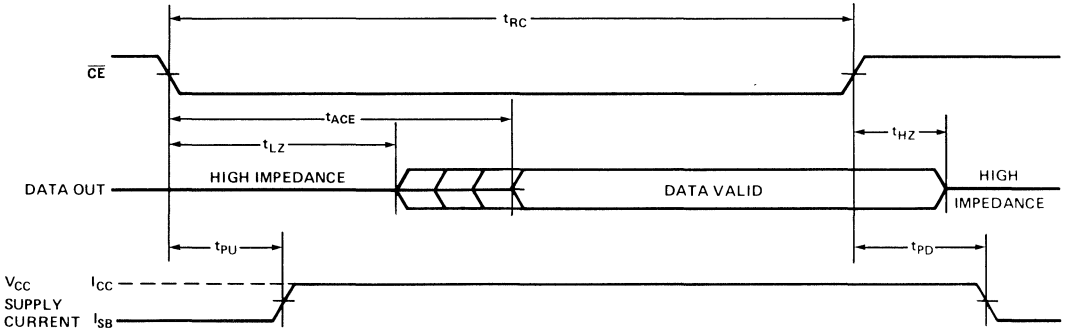
(See following page for notes)

Timing Diagrams

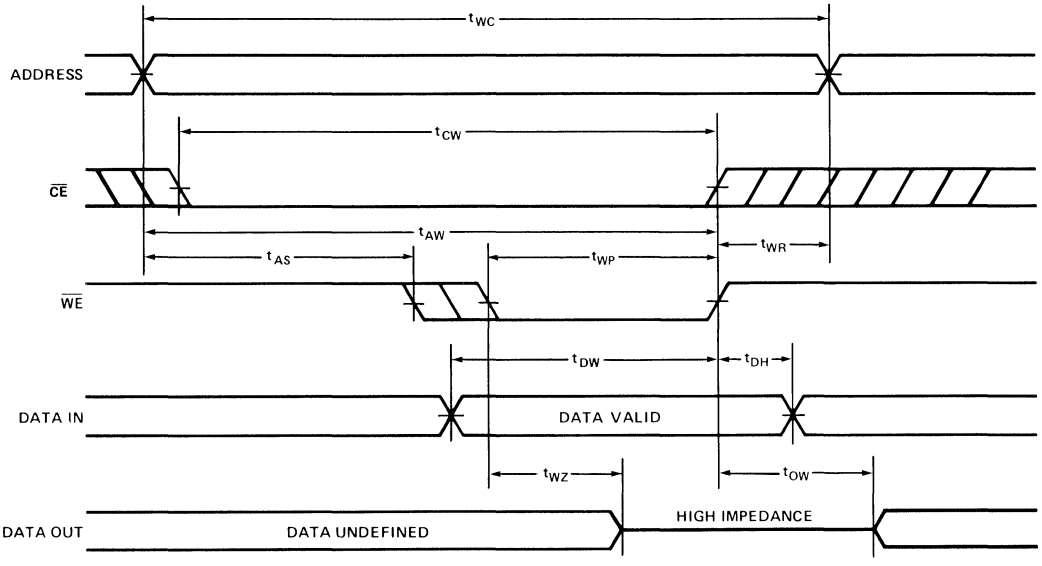
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



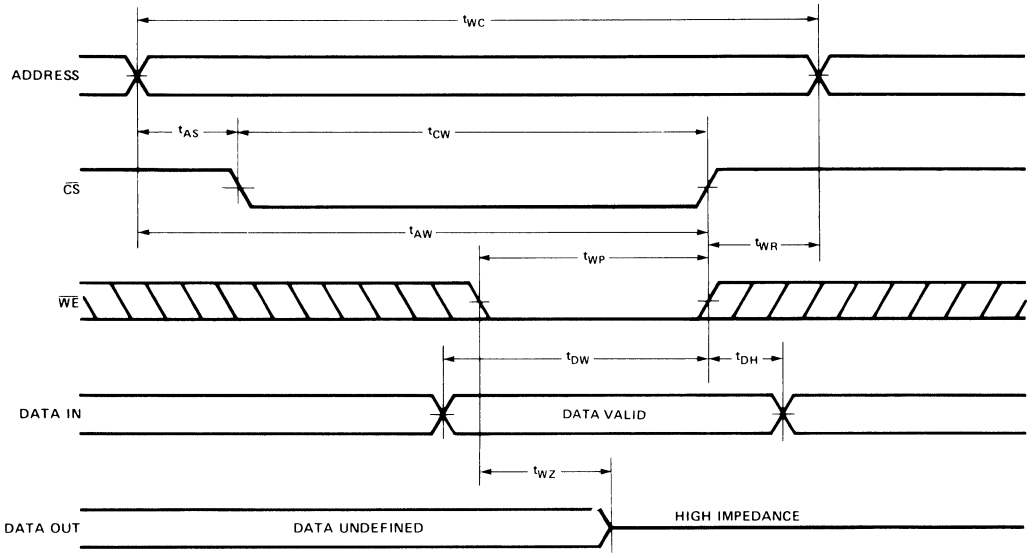
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled) (Note 4)



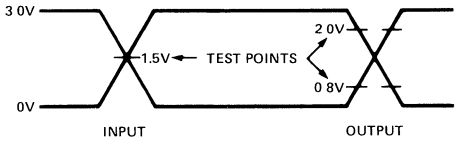
NOTES

1 $\overline{WE}$ is high for Read Cycles
2 Device is continuously selected, $\overline{CE} = V_{IL}$
3 Addresses valid prior to or coincident with $\overline{CE}$ transition low
4 If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
5 Transition is measured ±500 mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
7 A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected. otherwise, power-on current approaches I_{CC} active
8 A minimum of 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved
9 Duration not to exceed one second

WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled) (Note 4)

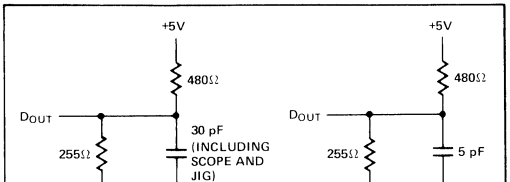


A.C. Testing Input, Output Waveform



A C TESTING INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0 0V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2 0V FOR A LOGIC "1" AND 0 8V FOR A LOGIC "0" AT THE OUTPUTS THE INPUTS ARE MEASURED AT 1 5V INPUT RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Package Availability 20 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYP2168-70	70 ns	120 mA	30 mA	Molded DIP
SYP2168-55	55 ns	120 mA	30 mA	Molded DIP
SYP2168-45	45 ns	120 mA	30 mA	Molded DIP

Synertek.

SY2169

4096 x 4 Static Random Access Memory

ADVANCED INFORMATION

Features

- 45 ns Maximum Address Access Times
- Fully Static Operation. No Clocks or Strobes Required
- Fast Chip Select Access Time. 40 ns Max.
- Identical Cycle and Access Times
- Single +5V Supply
- JEDEC Standard Pinout
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Outputs
- High Density 20-Pin Package
- Three-State Output

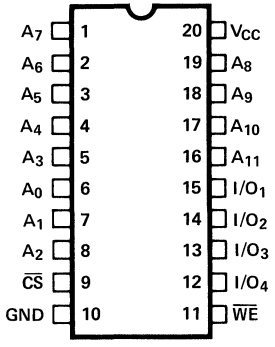
Description

The Synertek SY2169 is a 16,384-Bit Static Random Access Memory organized 4096 words by 4 bits and is fabricated using Synertek's N-Channel double poly silicon gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data Common data input and output pins provide maximum design flexibilty. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

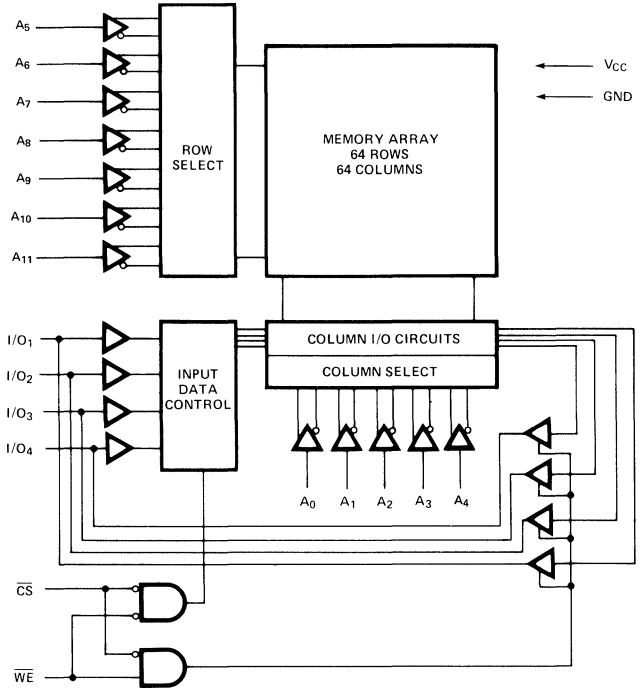
The SY2169 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance

The SY2169 is packaged in a 20-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to 85°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5V to +7V
Power Dissipation 1 0W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		50	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4 5V
I_{CC}	Power Supply Current		110	mA	T_A = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}; Outputs Open
			120	mA	T_A = 0°C
V_{IL}	Input Low Voltage	-3 0	0 8	V	
V_{IH}	Input High Voltage	2 0	6 0	V	
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2 4		V	I_{OH} = -4 mA
I_{OS}	Output Short Circuit Current	-200	+200	mA	V_{OUT} = Gnd to V_{CC} (Note 7)

Capacitance T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested

A.C. Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 6, 8)

READ CYCLE

		2169-3		2169		2169-2	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.
t_{RC}	Read Cycle Time	55		70		45	
t_{AA}	Address Access Time		50		65		40
t_{ACS}	Chip Select Access Time		55		70		45
t_{OH}	Output Hold from Address Change	3		5		3	
t_{LZ}	Chip Selection to Output in Low Z	20		20		20	
t_{HZ}	Chip Deselection to Output in High Z	0	25	0	30	0	20

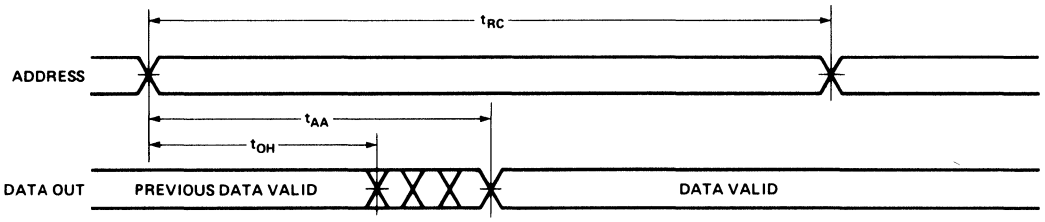
WRITE CYCLE

Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.
t_{WC}	Write Cycle Time	55		70		45	
t_{CW}	Chip Selection to End of Write	45		60		35	
t_{AW}	Address Valid to End of Write	45		60		35	
t_{AS}	Address Setup Time	0		0		0	
t_{WP}	Write Pulse Width	45		60		35	
t_{WR}	Write Recovery Time	3		5		3	
t_{DW}	Data Valid to End of Write	20		25		15	
t_{DH}	Data Hold Time	0		0		0	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	30	0	20
t_{OW}	Output Active from End of Write	0		0		0	

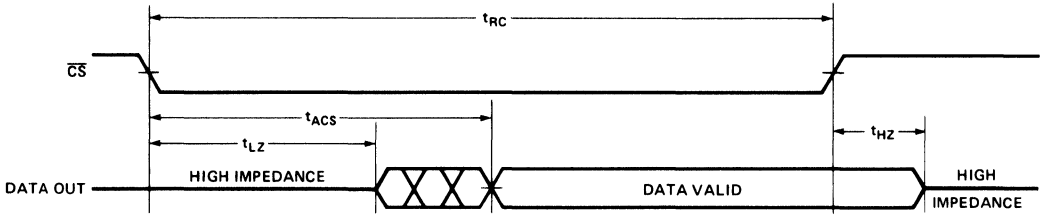
(See following page for notes)

Timing Diagrams

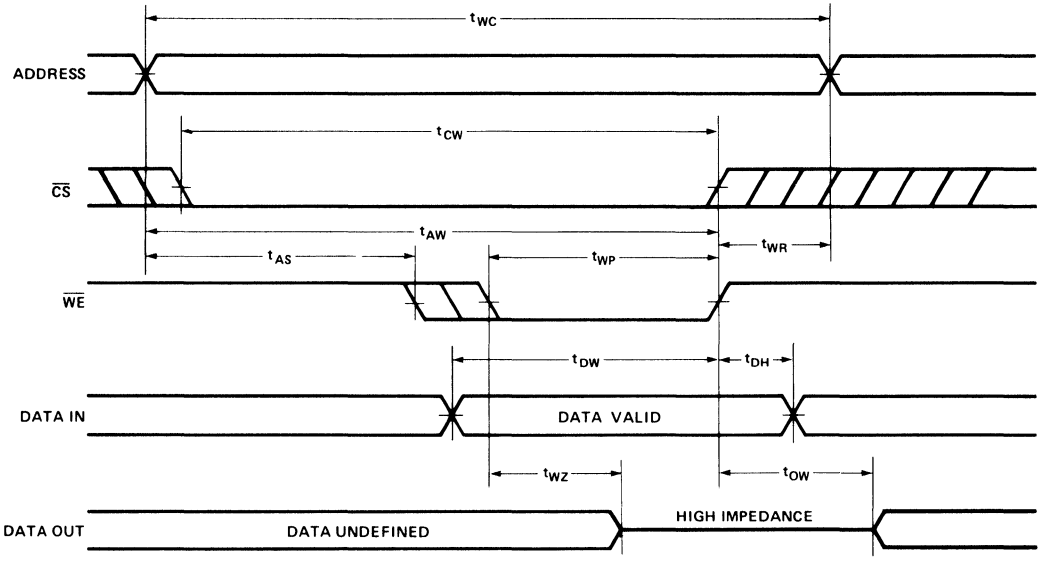
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



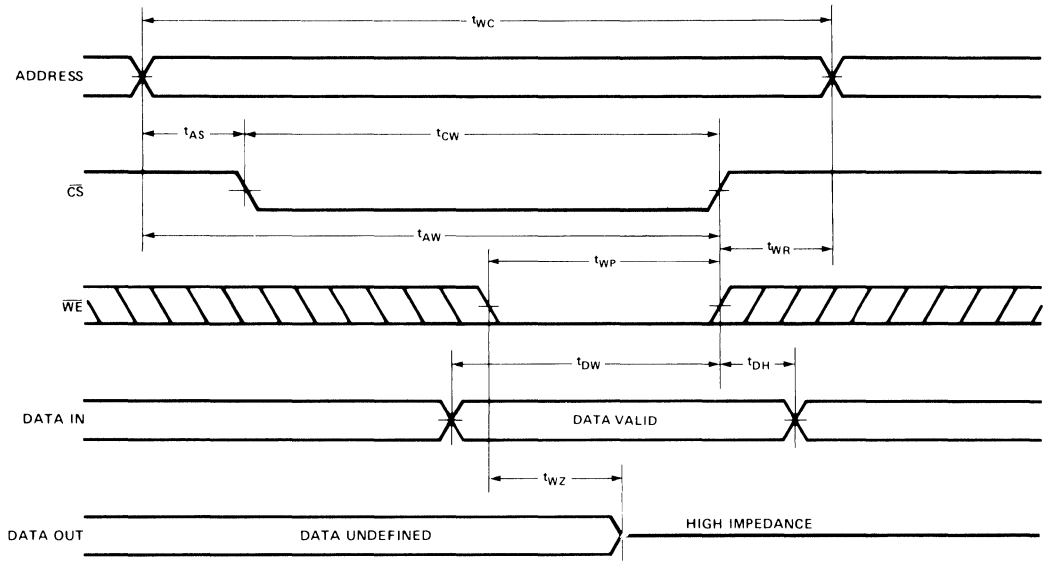
WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 4)



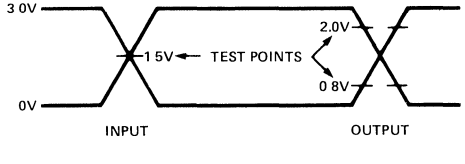
Notes:

1 $\overline{WE}$ is high for Read Cycles.
2 Device is continuously selected, $\overline{CE} = V_{IL}$.
3. Addresses valid
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
5 Transition is measured ±500 mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested
6 The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
7 Duration not to exceed one second.
8 A minimum of 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled) (Note 4)

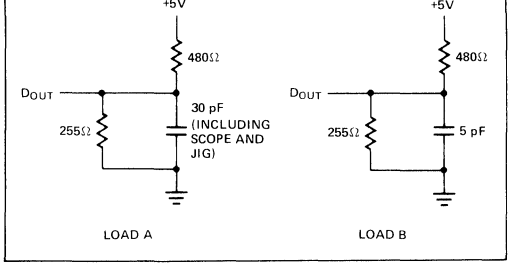


A.C. Testing Input, Output Waveform



A C TESTING INPUTS ARE DRIVEN AT 3 0V FOR A LOGIC "1" AND 0 0V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2 0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS THE INPUTS ARE MEASURED AT 1 5V INPUT RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Package Availability 20 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYP2169-70	70 ns	120 mA	20 mA	Molded DIP
SYP2169-55	55 ns	120 mA	20 mA	Molded DIP
SYP2169-45	45 ns	120 mA	20 mA	Molded DIP

ROMs.

Synertek.

SY2316B

2048 x 8 Static Read Only Memory

Features

- Access Time 200/300/450 ns (max)
- 2048 x 8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- JEDEC Approved Pinout
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Pin Compatible with 2716 EPROM
- Replacement for Two 2708s

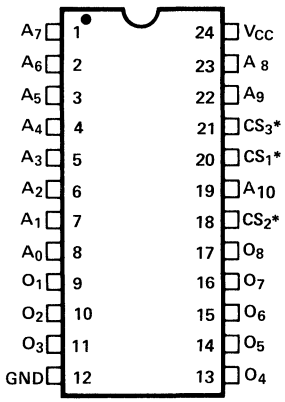
Description

The SY2316B high performance Read Only Memories are organized 2048 words by 8 bits with access times from 200 to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

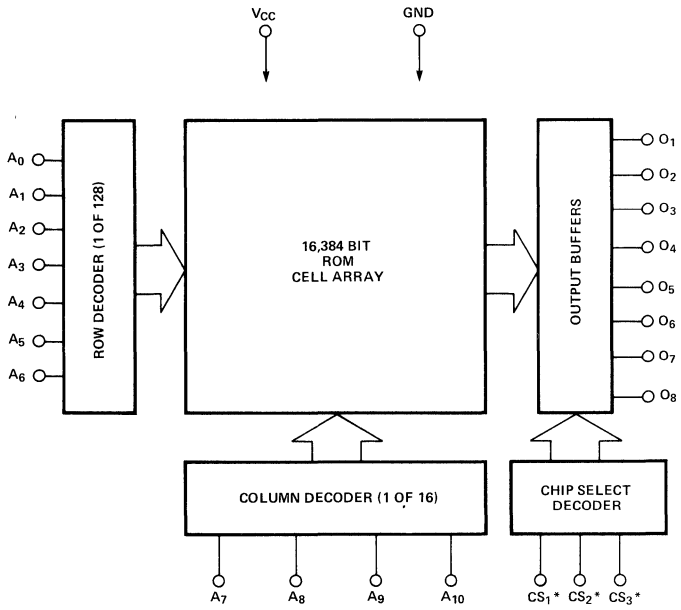
The SY2316B operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding The device offers three-state output buffers for memory expansion

Designed to replace the 2716 EPROM, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE, OR DON'T CARE

MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -0.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	$V_{CC} = 4.75V$, $I_{OH} = -200\ \mu A$
V_{OL}	Output LOW Voltage		0.4	Volts	$V_{CC} = 4.75V$, $I_{OL} = 2.1$ mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	$V_{CC} = 5.25V$, $0V \leqslant V_{in} \leqslant 5.25V$
I_{LO}	Output Leakage Current		10	uA	Chip Deselected $V_{out} = +0.4V$ to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded $V_{CC} = 5.25V$, $V_{in} = V_{CC}$

A.C. Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ (unless otherwise specified) (Note 3)

		2316B-2		2316B-3		2316B		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Test Conditions
t_{ACC}	Address Access Time		200		300		450	Output Load: 1 TTL load
t_{CO}	Chip Select Delay		100		130		150	and 100 pF
t_{DF}	Chip Deselect Delay		100		100		150	Input transition time: 20 ns
t_{OH}	Previous Data Valid After Address Change Delay	10		10		10		Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

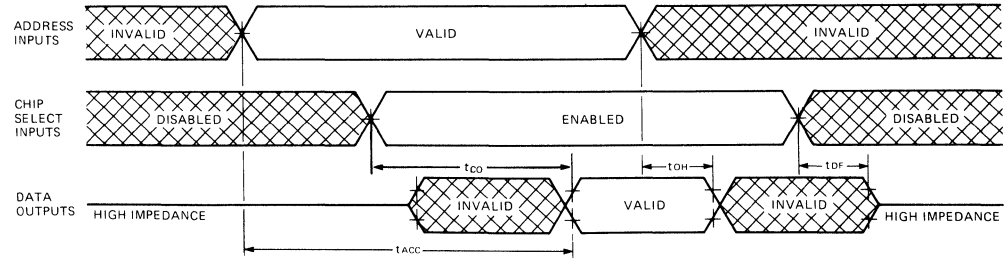
Capacitance

$t_A = 25°C$, f = 1.0MHz, See Note 2

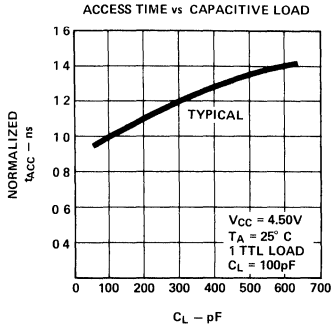
Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

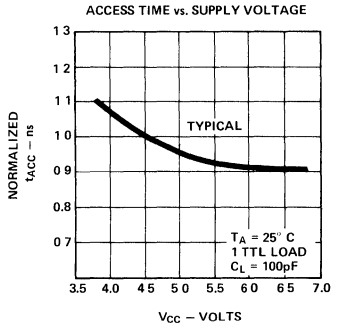
Notes:
1. Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device
2. This parameter is periodically sampled and is not 100% tested
3. A minimum 0.5 ns time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

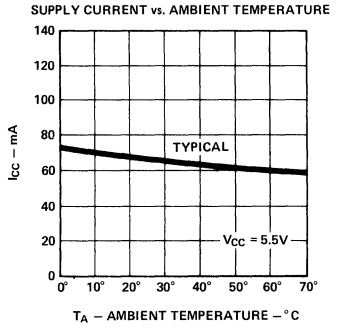
Timing Diagram

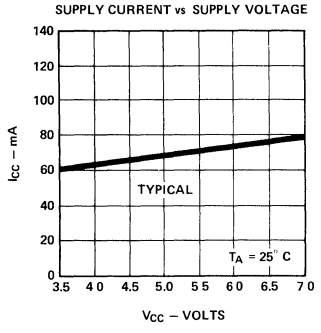


Typical Characteristics









Programming Instructions

All Synertek Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to Synertek in a number of different ways. Synertek can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your Synertek sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability 24 Pin Molded DIP

Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Package Type
SYP2316B	450 ns	98 mA	Molded DIP
SYP2316B-2	200 ns	98 mA	Molded DIP
SYP2316B-3	300 ns	98 mA	Molded DIP

Synertek.

SY2332/SY2333

4096 x 8 Static Read Only Memory

Features

- SY2332 is 2532 EPROM Pin Compatible
- 4096 x 8-Bit Organization
- Single +5 Volt Supply (±10%)
- Access Time 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- SY2333 is 2732 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- EPROMS Accepted as Program Data Inputs
- JEDEC Approved Pinouts

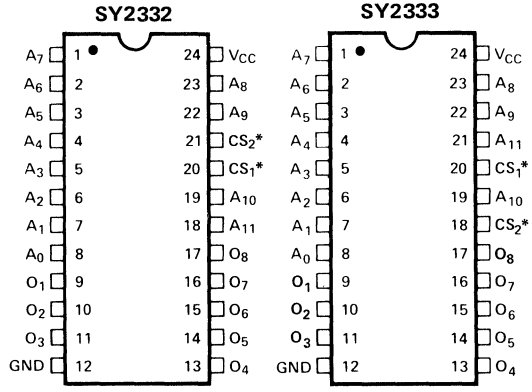
Description

The SY2332 and SY2333 high performance read only memories are organized 4096 words by 8 bits with access times from 200 ns to 450 ns They are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0 4 Volt noise immunity in conjunction with a +5 Volt power supply

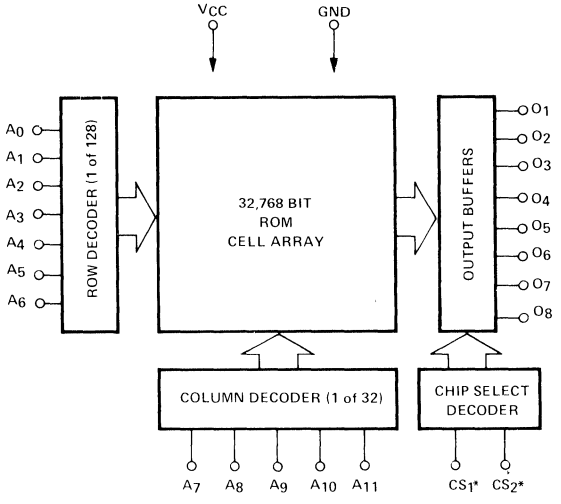
The SY2332 and SY2333 operate totally asynchronously No clock input is required The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding Both devices offer three-state output buffers for memory expansion

Designed to replace 32K EPROMs, the SY2332 and SY2333 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -3.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	$V_{CC} = 4.5V$, $I_{OH} = -400\mu A$
V_{OL}	Output LOW Voltage		0.4	Volts	$V_{CC} = 4.5V$, $I_{OL} = 2.1$ mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-3.0	0.8	Volts	
I_{LI}	Input Load Current		10	μA	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$
I_{LO}	Output Leakage Current		10	μA	Chip Deselected $V_{OUT} = +0.4$ V to V_{CC}
I_{CC}	Power Supply Current		100	mA	Output Unloaded, Chip Enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$

A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$ (unless otherwise specified) (Note 1)

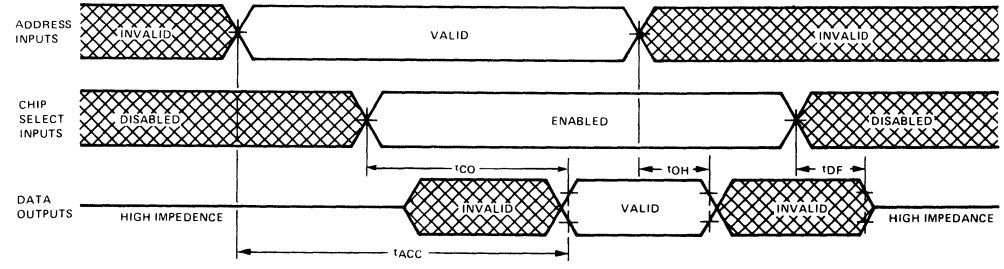
		SY2332-2 SY2333-2		SY2332-3 SY2333-3		SY2332 SY2333		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{ACC}	Address Access Time		200		300		450	ns
t_{CO}	Chip Select Delay		100		100		150	ns
t_{DF}	Chip Deselect Delay		100		100		150	ns
t_{OH}	Previous Data Valid After Address Change Delay	20		20		20		ns

Capacitance $t_A = 25°C$, f = 1.0 MHz (Note 2)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

1 A minimum 0.5 mstime delay is required after application of V_{CC} (+5V) before proper device operation is achieved
2 This parameter is periodically sampled and is not 100% tested.

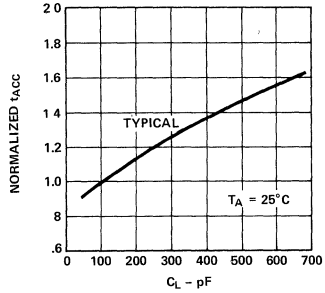
Timing Diagram



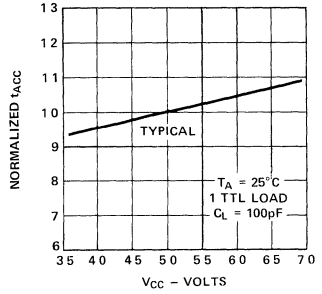
MEMORIES

Typical Characteristics

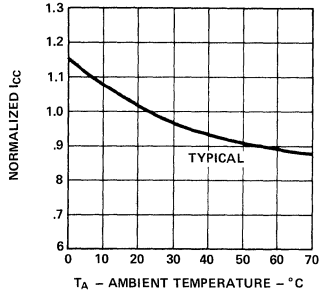
NORMALIZED ACCESS TIME vs. CAPACITIVE LOAD



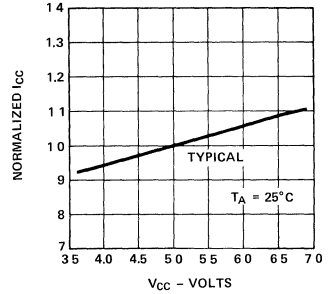
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



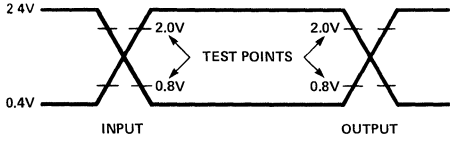
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

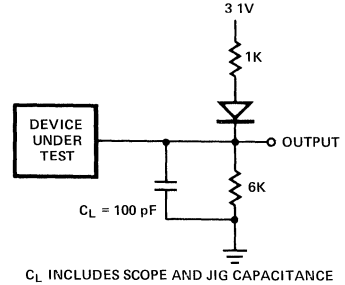


A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



C_L INCLUDES SCOPE AND JIG CAPACITANCE

Programming Instructions

All Synertek Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to Synertek in a number of different ways. Synertek can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your Synertek sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Secton.

Package Availability 24 Pin Molded DIP

Ordering Information

Order Number	Access Time	Operating Current	Package Type
SYP2332	450 ns	100 mA	Molded DIP
SYP2332-2	200 ns	100 mA	Molded DIP
SYP2332-3	300 ns	100 mA	Molded DIP
SYP2333	450 ns	100 mA	Molded DIP
SYP2333-2	200 ns	100 mA	Molded DIP
SYP2333-3	300 ns	100 mA	Molded DIP

A custom number will be assigned by Synertek.

Synertek.

SY2364/SY2364A

8192 x 8 Static Read Only Memory

Features

- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 24 Pin JEDEC Approved Pinout
- SY2364A — Automatic Power Down ($\overline{CE}$)
- SY2364 — Non Power Down Version
  — Programmable Chip Select ($\overline{CS}$)
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input
- 2564 EPROM Compatible

Description

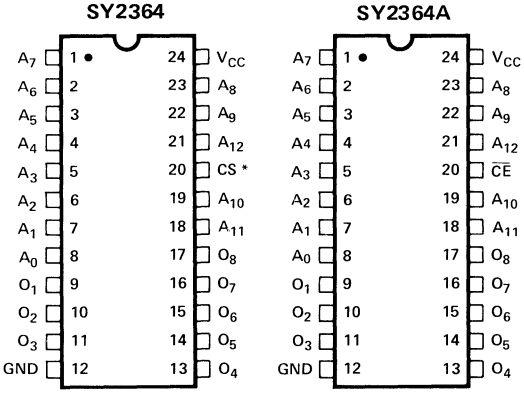
The SY2364 and SY2364A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations Both ROMs conform to the JEDEC approved pinout for 24 pin 64K ROMs

The SY2364 offers the simplest operation (no power down) Its programmable chip select allows two 64K ROMs to be OR-tied without external decoding

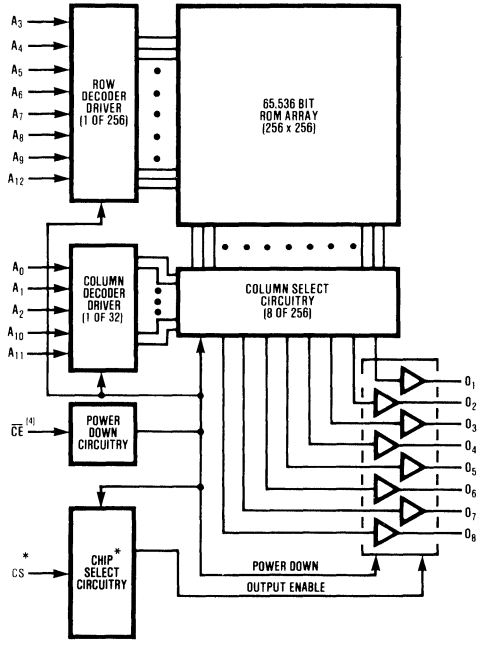
The SY2364A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high This unique feature provides system level power savings as much as 90%.

Both the SY2364 and SY2364A are pin compatible with the 2564 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations



Block Diagram



*CHIP SELECT (CS) IS PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE

MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -0.5V to +7 V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = -1 0 mA
V_{OL}	Output LOW Level			0 4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2 0		V_{CC}	V	
V_{IL}	Input LOW Level	-0.5		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance $T_A = 25°C$, f = 1 0 MHz

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

Note This parameter is periodically sampled and is not 100% tested

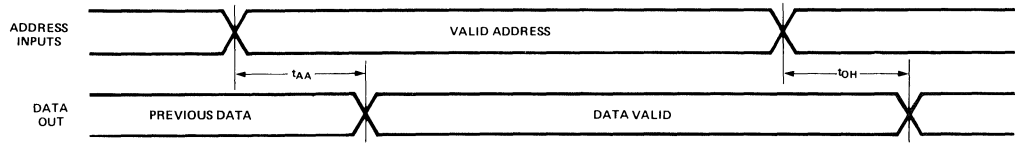
A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ (Note 7)

Symbol	Parameter	2364-2 2364A-2		2364-3 2364A-3		2364 2364A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

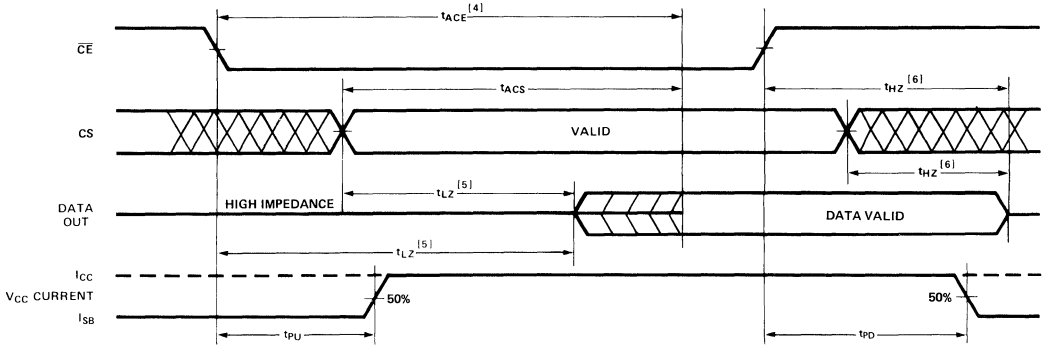
Notes:
1 Measured with device selected and outputs unloaded
2 Applies to "A" versions only and measured with $\overline{CE}$ = 2 0V
3 For a duration not to exceed one second
4 Applies to "A" versions (power down) only
5 Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ going low or CS going active
6 Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ going high or CS going inactive
7 A minimum 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

Timing Diagrams

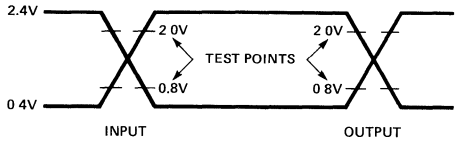
Propagation Delay from Address ($\overline{CE}$ LOW or CS = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit

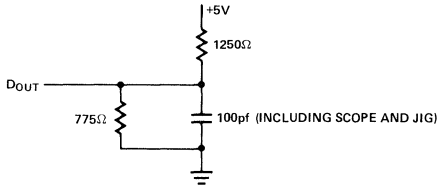


Figure 1.

Programming Instructions

All Synertek Read Only Memories (ROM) utilize computer asided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to Synertek in a number of different ways. Synertek can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your Synertek sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability 24 Pin Molded DIP

Ordering Information

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYP2364	450 ns	100 mA	N A *	Molded DIP
SYP2364-3	300 ns	100 mA	N A	Molded DIP
SYP2364-2	200 ns	100 mA	N A	Molded DIP
SYP2364A	450 ns	100 mA	12 mA	Molded DIP
SYP2364A-3	300 ns	100 mA	12 mA	Molded DIP
SYP2364A-2	200 ns	100 mA	12 mA	Molded DIP

*Not Applicable

Synertek.

SY2365/SY2365A

8192 x 8 Static Read Only Memory

Features

- 2764 EPROM Pin Compatible
- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY2365A — Automatic Power Down ($\overline{CE}$)
  - Output Enable Function ($\overline{OE}$)
  - Two Programmable Chip Selects (CS)
- SY2365 — Non Power Down Version
  - Four Programmable Chip Selects (CS)
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

Description

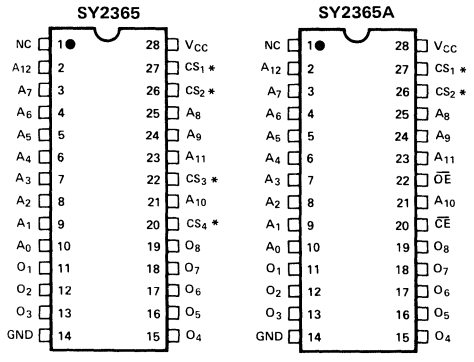
The SY2365 and SY2365A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations Both ROMs conform to the JEDEC approved pinout for 28 pin 64K ROMs

The SY2365 offers the simplest operation (no power down) Its four programmable chip selects allow up to sixteen 64K ROMs to be OR-tied without external decoding

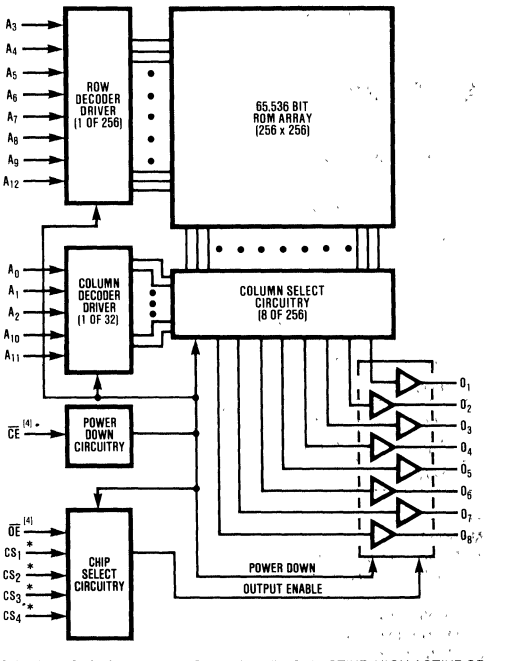
The SY2365A offers an automatic power down feature Power down is controlled by the Chip Enable ($\overline{CE}$) input When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high This unique feature provides system level power savings as much as 90% An additional feature of the SY 2365A is the Output Enable ($\overline{OE}$) function This eliminates bus contention in multiple bus microprocessor systems. The two programmable Chip Selects (CS) allow up to four 64K ROMs to be OR-tied without external decoding.

Both the SY2365 and SY 2365A are pin compatible with the 2764 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs

Pin Configurations



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE

Absolute Maximum Ratings*

Temperature Under Bias ..... -10°C to +80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... -0.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability

D.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2 4		V_{CC}	V	$I_{OH} = -1$ 0 mA
V_{OL}	Output LOW Level			0 4	V	$I_{OL} = 3$ 2 mA
V_{IH}	Input HIGH Level	2 0		V_{CC}	V	
V_{IL}	Input LOW Level	-0.5		0 8	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0V$ to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			70	mA	Note 3

Capacitance $T_A = 25°C$, $f = 1$ 0 MHz

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	$V_{IN} = 0V$
C_O	Output Capacitance		5	pf	$V_{OUT} = 0V$

Note This parameter is periodically sampled and is not 100% tested

A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ (Note 7)

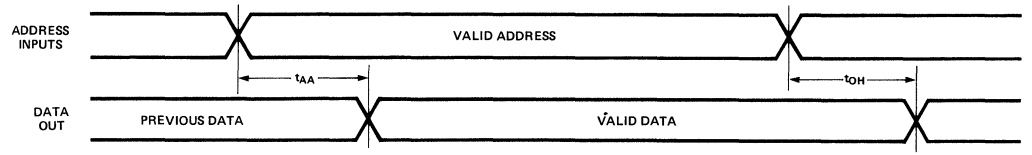
Symbol	Parameter	2365-2 2365A-2		2365-3 2365A-3		2365 2365A		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

Notes:
1 Measured with device selected and outputs unloaded
2 Applies to "A" versions only and measured with $\overline{CE}$ = 2 0V
3 For a duration not to exceed one second
4 Applies to "A" versions (power down) only
5 Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last
6 Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first
7 A minimum 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

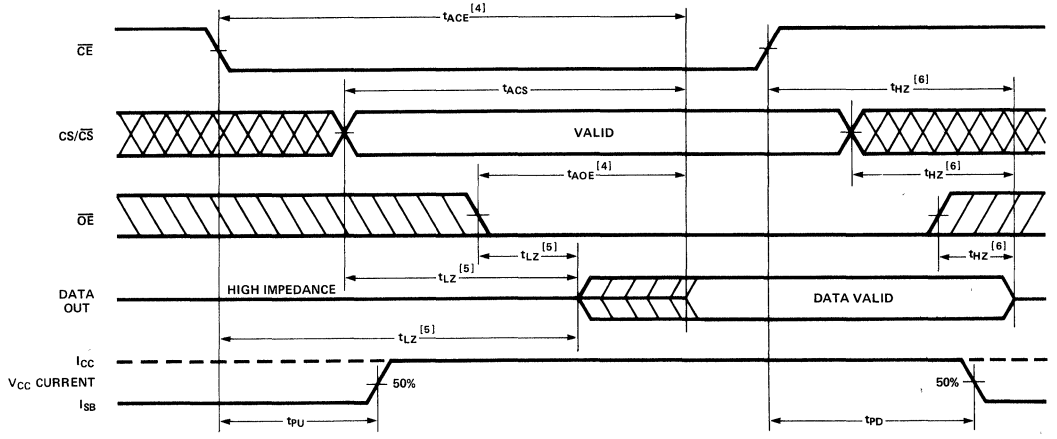
MEMORIES

Timing Diagrams

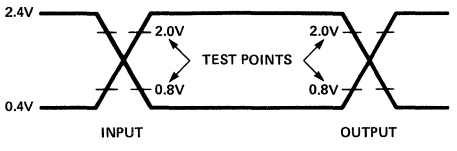
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0 4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

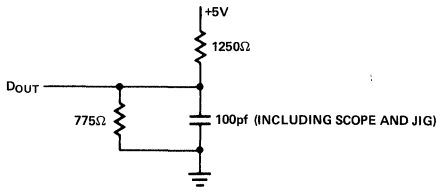


Figure 1.

Programming Instructions

All Synertek Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to Synertek in a number of different ways. Synertek can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your Synertek sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability

28 Pin Ceramic DIP
28 Pin Molded DIP

Ordering Information

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYP2365	450 ns	100 mA	N.A.*	Molded DIP
SYP2365-3	300 ns	100 mA	N.A.	Molded DIP
SYP2365-2	200 ns	100 mA	N.A.	Molded DIP
SYP2365A	450 ns	100 mA	12 mA	Molded DIP
SYP2365A-3	300 ns	100 mA	12 mA	Molded DIP
SYP2365A-2	200 ns	100 mA	12 mA	Molded DIP

*Not applicable

Synertek.

SY23128/SY23128A
16,384 x 8 Static Read Only Memory

PRELIMINARY

Features

- EPROM Pin Compatible
- 16,384 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY23128A — Automatic Power Down ($\overline{CE}$)
  - Output Enable Function ($\overline{OE}$)
  - One Programmable Chip Select ($\overline{CS}$)
- SY23128 — Non Power Down Version
  - Three Programmable Chip Selects
- Three State Outputs for Wire-OR Expansion
- EPROMS Accepted as Program Data Input

Description

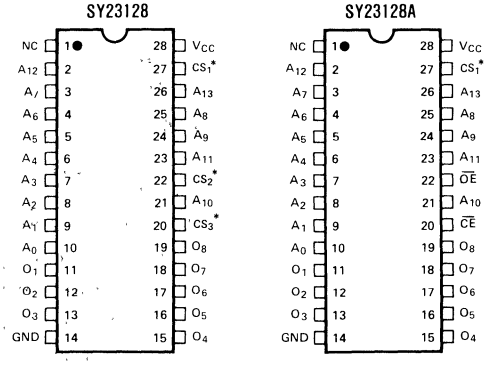
The SY23128 and SY23128A high performance Read Only Memories are organized 16,384 words by 8 bits with access times from 200 ns to 450 ns The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations Both ROMs conform to the JEDEC approved pinout for 28 pin 128K ROMs

The SY23128 offers the simplest operation (no power down) Its three programmable chip selects allow up to eight 128K ROMs to be OR-tied without external decoding

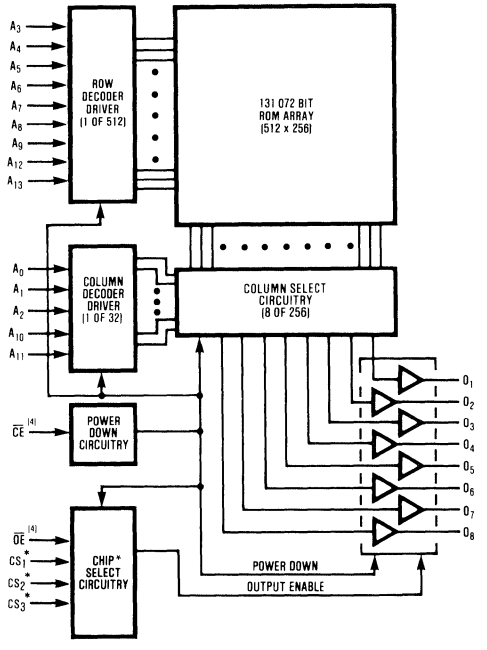
The SY23128A offers an automatic power down feature Power down is controlled by the Chip Enable ($\overline{CE}$) input When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high This unique feature provides system level power savings as much as 90% An additional feature of the SY23128A is the Output Enable ($\overline{OE}$) function This eliminates bus contention in multiple bus microprocessor systems The programmable chip select allows two 128K ROMs to be OR-tied without external decoding

Both the SY23128 and SY23128A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs

Pin Configurations



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE, OR DON'T CARE

MEMORIES

Absolute Maximum Ratings*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2mA
V_{IH}	Input HIGH Level	2.2		V_{CC}	V	
V_{IL}	Input LOW Level	−3.0		0 8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			10	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Max.	Units	Conditions
C_I	Input Capacitance		5	pF	V_{IN} = 0V
C_O	Output Capacitance		5	pF	V_{OUT} = 0V

Note: This parameter is periodically sampled and is not 100% tested

A.C. Characteristics

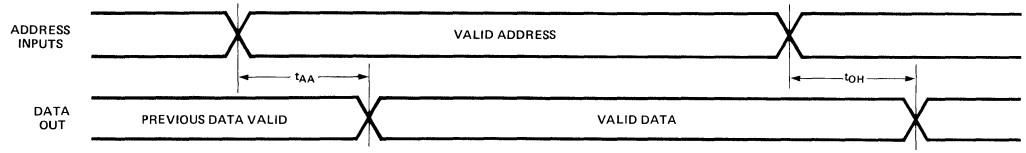
T_A = 0°C to +70°C, V_{CC} = +5V ±10% (Note 7)

		23128-2 23128A-2		23128-3 23128A-3		23128 23128A			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Conditions
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		100		120		150	ns	Note 4

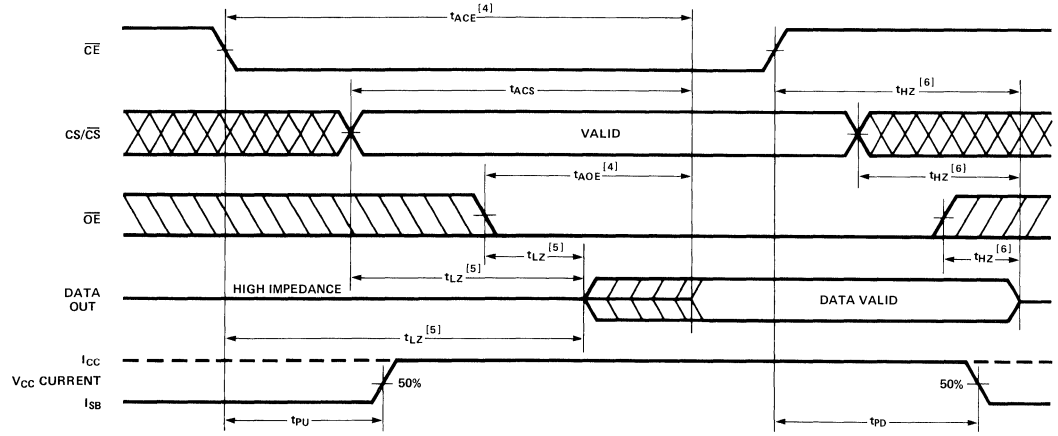
Notes:
1 Measured with device selected and outputs unloaded.
2 Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed one second with V_{OUT} = 0V.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low or CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
7. A minimum 0.5ms time delay is required after application of V_{CC} (±5V) before proper device operation is achieved

Timing Diagrams

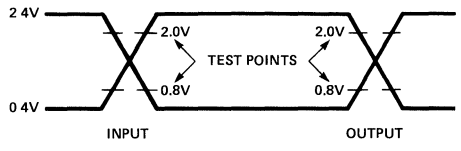
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0". INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

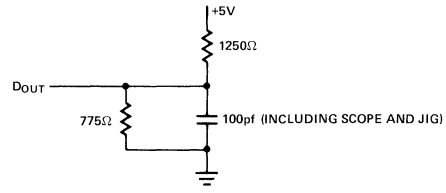


Figure 1.

Programming Instructions

All Synertek Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to Synertek in a number of different ways. Synertek can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your Synertek sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability 28 Pin Molded DIP

Ordering Information

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYP23128	450 ns	100 mA	N A	Molded DIP
SYP23128-3	300 ns	100 mA	N A	Molded DIP
SYP23128-2	200 ns	100 mA	N A	Molded DIP
SYP23128A	450 ns	100 mA	10 mA	Molded DIP
SYP23128A-3	300 ns	100 mA	10 mA	Molded DIP
SYP23128A-2	200 ns	100 mA	10 mA	Molded DIP

Synertek.

SY23256/SY23256A

32,768 x 8 Static Read Only Memory

PRELIMINARY

Features

- EPROM Pin Compatible
- 32,768 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY23256A— Automatic Power Down ($\overline{CE}$)
  — Output Enable Function ($\overline{OE}$)
- SY23256 — Non Power Down Version
  — Two Programmable Chip Selects (CS)
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

Description

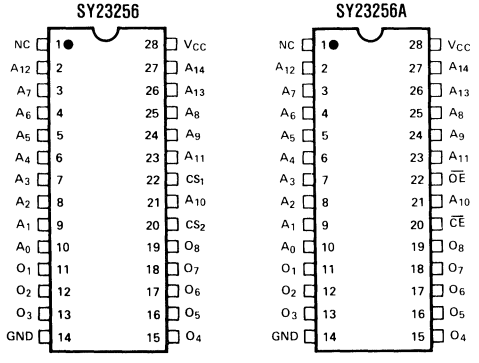
The SY23256 and SY23256A high performance Read Only Memories are organized 16,384 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 256K ROMs.

The SY23256 offers the simplest operation (no power down). Its two programmable Chip Selects allow up to four 256K ROMs to be OR-tied without external decoding.

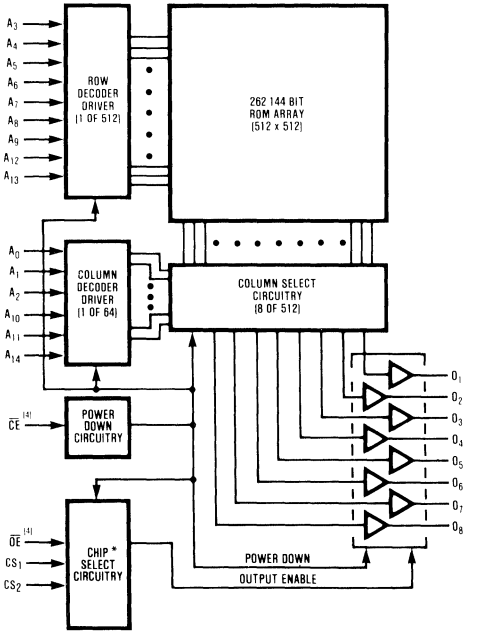
The SY23256A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the SY23256A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems.

Both the SY23256 and SY23256A are pin compatible with EPROMs, thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE, OR DON'T CARE

Absolute Maximum Ratings*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground .. .. −3.5V to +7V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = −1.0mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	−3.0		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			10	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

Capacitance

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Max.	Units	Conditions
C_I	Input Capacitance		5	pF	V_{IN} = 0V
C_O	Output Capacitance		5	pF	V_{OUT} = 0V

Note. This parameter is periodically sampled and is not 100% tested

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±10% (Note 7)

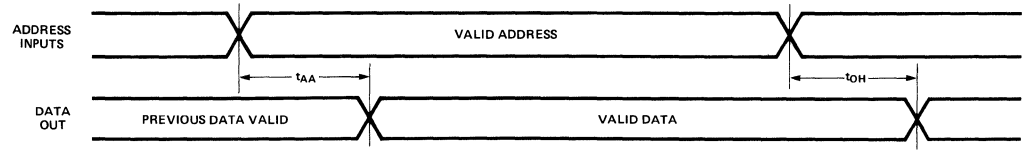
		23256-2 23256A-2		23256-3 23256A-3		23256 23256A			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Conditions
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		100		120		150	ns	Note 4

Notes

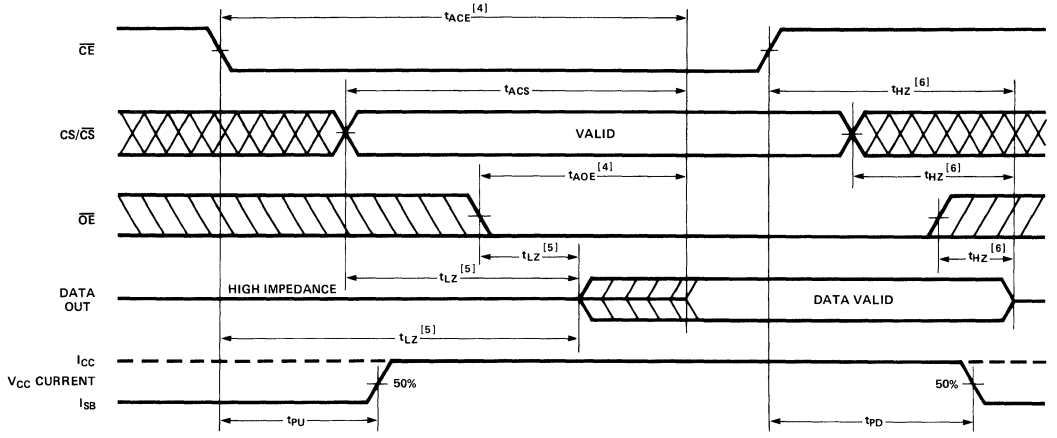
1 Measured with device selected and outputs unloaded
2 Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V
3 For a duration not to exceed one second with V_{OUT} = 0V
4 Applies to "A" versions (power down) only
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low or CS going active, whichever occurs last.
6 Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
7 A minimum 0.5ms time delay is required after application of V_{CC} (±5V) before proper device operation is achieved.

Timing Diagrams

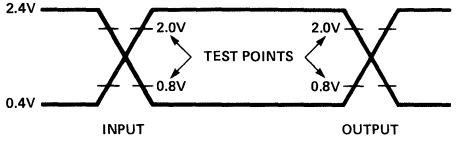
Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select (Address Valid)



A.C. Testing Input, Output Waveform



AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" INPUT PULSE RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit

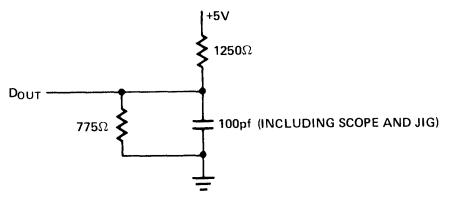


Figure 1.

Programming Instructions

All Synertek Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to Synertek in a number of different ways. Synertek can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact your Synertek sales representative for complete details on each of the various data input formats.

Programming instructions are listed at the end of the Memory Section.

Package Availability 28 Pin Molded DIP

Ordering Information

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYP23256	450 ns	100 mA	N A	Molded DIP
SYP23256-3	300 ns	100 mA	N A	Molded DIP
SYP23256-2	200 ns	100 mA	N A	Molded DIP
SYP23256A	450 ns	100 mA	10 mA	Molded DIP
SYP23256A-3	300 ns	100 mA	10 mA	Molded DIP
SYP23256A-2	200 ns	100 mA	10 mA	Molded DIP

All Synertek Read Only Memories utilize computer aided techniques to manufacture and test custom bit patterns The custom bit pattern and address information are supplied on standard 80 column computer cards in the format described below

All addresses and related output patterns must be completely defined Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards Positive logic is generally used on all input cards a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs Consult your Synertek representative for details

Title Cards

A set of four Title Cards should accompany each data deck These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information

	Column	Information
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank — pattern number to be assigned by Synertek
	29	CS chip select logic level (if LOW selects chip, punch "0", if HIGH selects chip, punch "1", if DON'T CARE, punch "2")
	30	CS chip select logic level
	31	CS chip select logic level
	32	CS chip select logic level
Fourth Card	1-8	Data Format Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one
	15-28	Logic format, punch "POSITIVE LOGIC" or "NEGATIVE LOGIC "
	35-57	Truth table verification code, punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

Synertek Data Card Format

All addresses are coded in decimal form (0 through 2047) All output words are coded both in binary and octal forms Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	Column	Information
Data Cards	1-4	Decimal address
	6-13	Output (MSB-LSB)
	15-17	Octal equivalent of output data
	22-25	Decimal address
	27-34	Output (MSB-LSB)
	36-38	Octal equivalent of output data
	43-46	Decimal address
	48-55	Output (MSB-LSB)
	57-59	Octal equivalent of output data
	64-67	Decimal address
	69-76	Output (MSB-LSB)
	78-80	Octal equivalent of output data

Intel Data Card Format

Output data is punched as either a "P" or an "N", a "P" is defined as a HIGH, and an "N" is defined as a LOW Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	Column	Information
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card This is the initial input address The address is right justified, i e 00000, 00008, 00016, etc
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2.
	34-41	Output data for initial input address +3.
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:
Synertek — ROM
P.O. Box 552
Santa Clara, CA 95052

Third Card Chip Select Setups

Column	SY2316B	SY2332/3	SY2364	SY2365/A	SY23128	SY23256	SY3308	SY3316
29					CS3/$\overline{CS3}$*	CS1/$\overline{CS1}$	CS4/$\overline{CS4}$	
30	CS3/$\overline{CS3}$	CS2/$\overline{CS2}$		CS3/$\overline{CS3}$*	CS2/$\overline{CS2}$	CS2/$\overline{CS2}$*	CS3/$\overline{CS3}$	CS3/$\overline{CS3}$
31	CS2/$\overline{CS2}$	CS1/$\overline{CS1}$		CS2/$\overline{CS2}$	CS1/$\overline{CS1}$		CS2/$\overline{CS2}$	CS2/$\overline{CS2}$
32	CS1/$\overline{CS1}$		CS/$\overline{CS}$	CS1/$\overline{CS1}$			CS1/$\overline{CS1}$	CS1/$\overline{CS1}$

*For "A" version leave blank

Intel Paper Tape Format

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization. NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing Bs or Fs may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Hexadecimal Program Tape Format

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1,2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.
Frames 7,8	Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.
Frames 9 to 9+2* (Record Length) -1	Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).
Frames 9+2* (Record Length) to 9+2* (Record Length) +1	Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

:0300010053F8ECC5

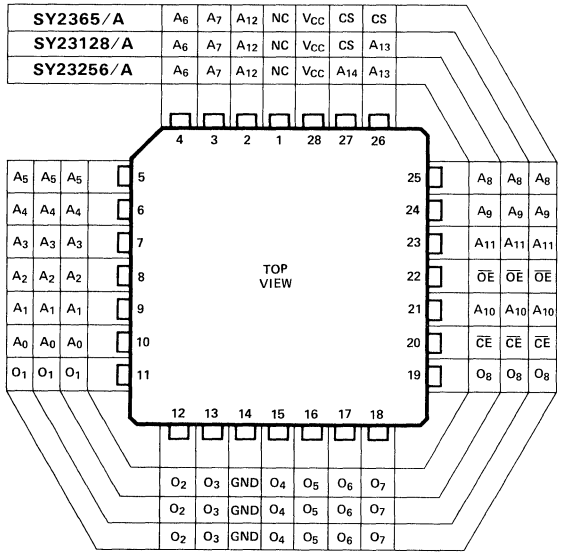
Send bit pattern data to the following special address:

Synertek — ROM
P.O. Box 552
Santa Clara, CA 95052

SYPJ2365/A
SYPJ23128/A
SYPJ23256/A

Packaging Information

28 Lead Surface Mounted Device *



*Available second half '85

Military.

3

Military Selection Guide

Part Number	Organization	Access Time (ns)	Maximum Current (mA)		Power Supply (Volts)	Number of Pins	Package Type (Note 1)	Compatible EPROM/ PROM	Page No.
			Operating	Standby					
SYM2148H-3	1024 x 4	55	150	30	+5	18	C, D, F, K		3-13
SYM2148H	1024 x 4	70	150	30	+5	18	C, D, F, K		3-13
SYM2149H-3	1024 x 4	70	150	30	+5	18	C, D, F, K		3-17
SYM2149H	1024 x 4	70	150	30	+5	18	C, D, F, K		3-17
SYM2147H-3	1024 x 4	70	160	30	+5	18	C, D, F, K		3-9
SYM2147H	1024 x 4	70	160	30	+5	18	C, D, F, K		3-9
SYM2128-3	2048 x 8	150	100	30	+5	24	C, D, K		3-3
SYM2128-4	2048 x 8	200	100	30	+5	24	C, D, K		3-3
SYM2168[2]	4096 x 4	70	[3]	[3]	+5	24	C, D, K		3-21
SYM2169[2]	4096 x 4	70	[3]	—	+5	24	C, D, K		3-25
SYM2167[2]	16,348 x 1	70	[3]	[3]	+5	24	C, D, K		3-29
SYM2130	1024 x 8	150	[3]	[3]	+5	40	C		3-7

Synertek.

SYM2128

Military 2048 x 8 Static Random Access Memory

Extended Temperature Range (-55° C to +125° C)

Features

- 150 nsec Maximum Access Time
- Fully Static Operation: No Clocks or Strobes Required
- Automatic CE Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pin Compatible with 2716 16K EPROM
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- JEDEC Approved Pinout

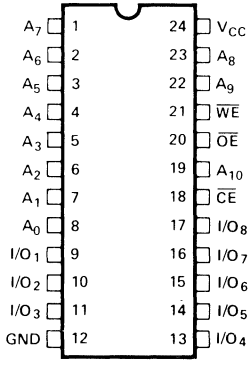
Description

The Synertek SYM2128 is a 16,384 bit static Random Access Memory organized 2048 words by eight bits and is fabricated using Synertek's new scaled n-channel silicon gate technology It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus

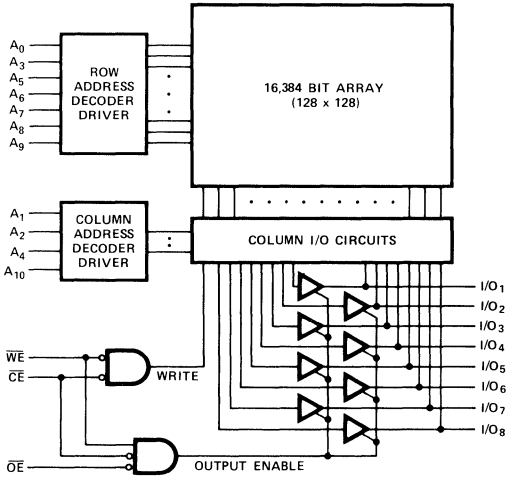
The SYM2128 offers an automatic power down feature under the control of the chip enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, deselecting the chip, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This feature provides significant system level power savings.

The SYM2128 is configured in the JEDEC approved pinout for 24 pin byte organized memories and is pin compatible with 16K ROMs, EPROMs and EEPROMs. This offers the user the flexibility of being able to switch between RAM, ROM, EPROM, or EEPROM as his needs dictate with a minimum of board changes.

Pin Configuration



Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin with
Respect to Ground ..... -1.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	SYM2128-3/-4 Min.	SYM2128-3/-4 Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$\overline{CE}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current			mA	T_A = 25°C | V_{CC} = Max, $\overline{CE}$ = V_{IL}
			100	mA	T_A = -55°C | Outputs Open
I_{SB}	Standby Current		30	mA	V_{CC} = Min to Max, $\overline{CE}$ = V_{IH}
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -1.0mA

Capacitance

T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ±10%

READ CYCLE

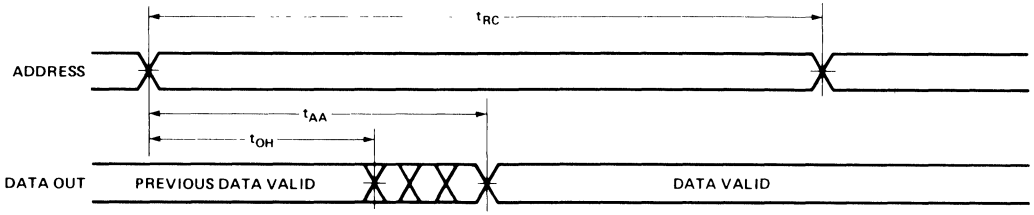
Symbol	Parameter	SYM2128-3 Min.	SYM2128-3 Max.	SYM2128-4 Min.	SYM2128-4 Max.	Unit	Conditions
t_{RC}	Read Cycle Time	150		200		ns	
t_{AA}	Address Access Time		150		200	ns	
t_{ACE}	Chip Enable Access Time		150		200	ns	
t_{AOE}	Output Enable Access Time		60		70	ns	
t_{OH}	Output Hold from Address Change	10		10		ns	
t_{LZ}	Output Low Z Time	10		10		ns	Note 5
t_{HZ}	Output High Z Time	0	50	0	60	ns	Note 5
t_{PU}	Chip Enable to Power Up Time	0		0		ns	
t_{PD}	Chip Disable to Power Down Time		80		100	ns	

WRITE CYCLE

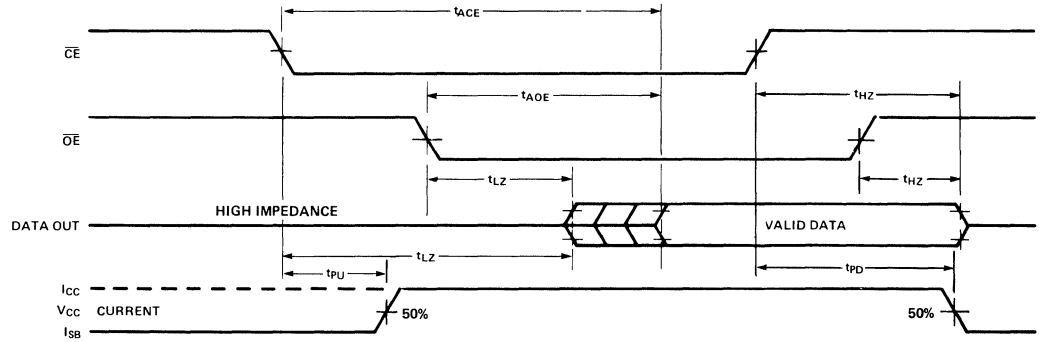
t_{WC}	Write Cycle Time	150		200		ns	
t_{CW}	Chip Enable to End of Write	120		150		ns	
t_{AW}	Address Valid to End of Write	120		150		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	90		120		ns	
t_{WR}	Write Recovery Time	0		0		ns	
t_{DW}	Data Valid to End of Write	70		90		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	50	0	60	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		ns	Note 5

Timing Diagrams

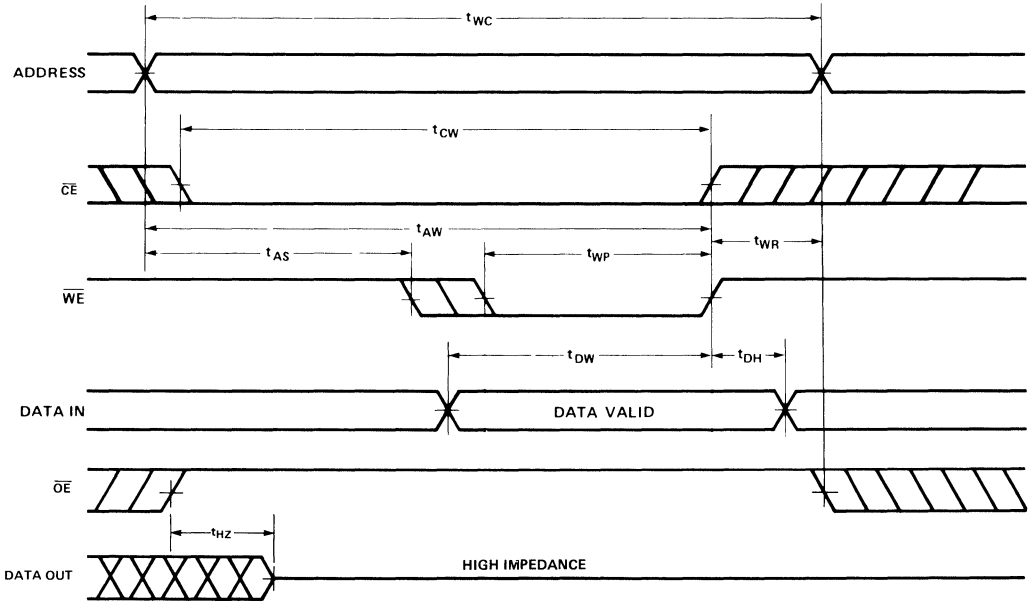
READ CYCLE NO. 1 (NOTES 1 and 2)



READ CYCLE NO. 2 (NOTES 1 and 3)



WRITE CYCLE NO. 1 (NOTE 4)

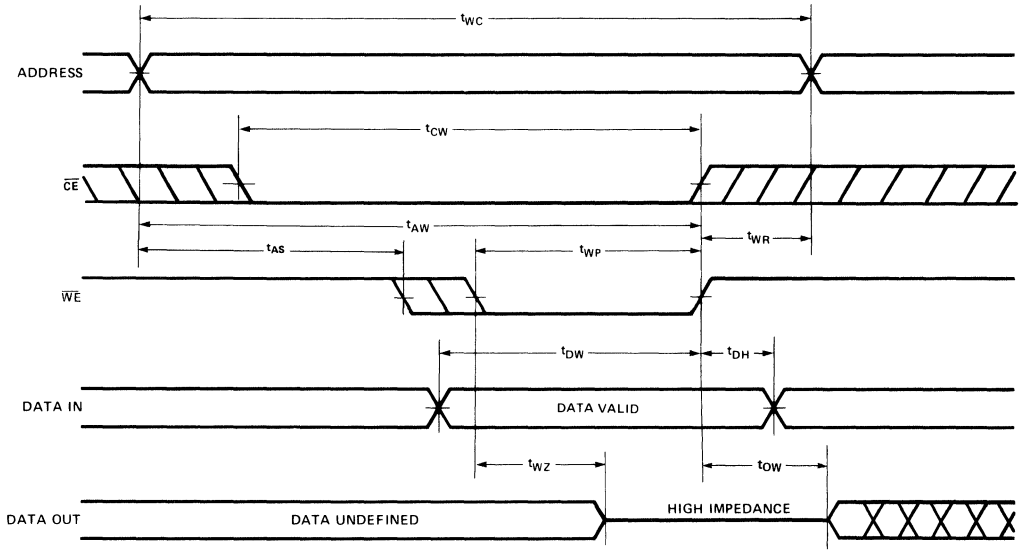


Notes:

1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CE} = \overline{OE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.

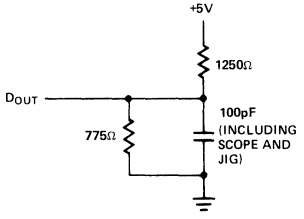
MILITARY

WRITE CYCLE NO. 2 ($\overline{OE}$ = V_{IL}) (NOTE 4)

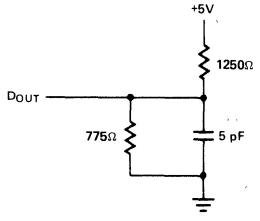


A.C. TEST CONDITIONS

INPUT PULSE LEVELS	0.8 to 2.4V VOLTS
INPUT RISE AND FALL TIMES	10 nsec
INPUT AND OUTPUT TIMING REFERENCE LEVELS	1 5 VOLTS
OUTPUT LOAD	SEE LOAD A



LOAD A



LOAD B

Package Availability

24 lead Cerdip
24 lead Ceramic

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYMD2128-3	150 ns	100 mA	30 mA	Cerdip
SYMC2128-3	150 ns	100 mA	30 mA	Ceramic
SYMD2128-4	200 ns	100 mA	30 mA	Cerdip
SYMC2128-4	200 ns	100 mA	30 mA	Ceramic

Synertek

SYM2130/SYM2131

Military 1024 x 8 Dual Port Random Access Memory

Temperature Range (-55°C to +125°C)

ADVANCED INFORMATION

Features

- 150 ns Address Access Time
- Fully Static Operation
- Full TTL Compatibility
- Interrupt Function ($\overline{INT}$): Open Drain for OR-tied Operation
- Easy Microprocessor Interface
- $\overline{BUSY}$ Function to Handle Contention: Open Drain for OR-tied Operation
- SYM2130 — Transparent Power Down ($\overline{CE}$)
- SYM2131 — Non-Power Down ($\overline{CS}$)
- Output Enable Function ($\overline{OE}$)
- Both Ports Operate Independently

Description

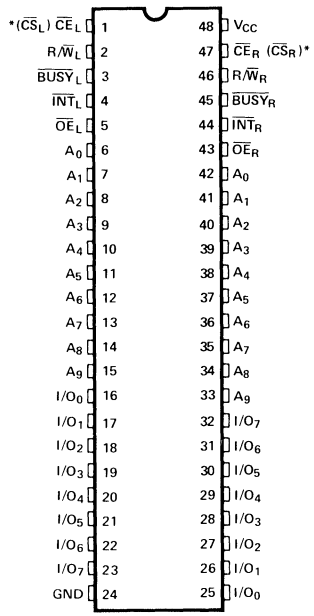
The Synertek SYM2130 and SYM2131 are 8192 Bit Dual Port Static Random Access Memories organized 1024 words by 8 bits They are designed using fully static circuitry and fabricated using Synertek's n-channel double poly silicon gate technology

The SYM2130 and SYM2131 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The only situation where contention can occur is when both ports are active and both addresses match. Two modes of operation are provided for this situation. In one mode, contention is ignored and both operations are allowed to proceed. In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed. A $\overline{BUSY}$ flag is sent to the side whose operation is delayed. $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data.

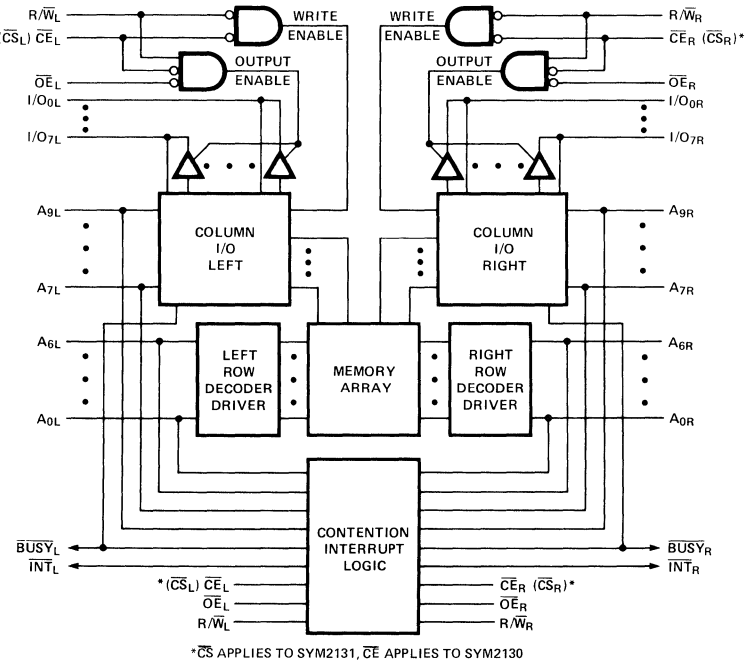
An interrupt function ($\overline{INT}$) is also provided to allow communication between systems. This function acts like a writable flag When the flag's location is written from one

(continued next page)

Pin Configuration



Block Diagram



*$\overline{CS}$ APPLIES TO SYM2131, $\overline{CE}$ APPLIES TO SYM2130

MILITARY

side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. Both the $\overline{BUSY}$ and $\overline{INT}$ pins are open drain outputs to allow OR-tied operation.

The SYM2130 has an automatic power down feature which is controlled by the Chip Enable inputs Each Chip Enacle controls automatic power-down circuitry that allows it's respective side of the device to remain in a standby power mode.

The SYM2131 chip select (no power down) access has been designed to be faster than it's address access so that the chip select decode time will not add to the memory's overall access time This feature significantly improves system performance

Pin Definitions

$\overline{CE}_L$(10) Left Port Chip Enable When $\overline{CE}_L$ goes HIGH, the left port of the RAM is deselected and the left port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CE}_L$ remains HIGH

$\overline{CE}_R$(10) Right Port Chip Enable. When $\overline{CE}_R$ goes HIGH, the right port of the RAM is deselected and the right port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CE}_R$ remains HIGH.

$\overline{CS}_L$(11) Left Port Chip Select. When $\overline{CS}_L$ goes HIGH, the left port of the RAM is deselected

$\overline{CS}_R$(11) Right Port Chip Select When $\overline{CS}_R$ goes HIGH, the right port of the RAM is deselected.

$A0_L$-$A9_L$ Left Port Address Inputs The 10-bit field presented at the left port Address Inputs selects one of the 1024 memory locations to be read from or written into via the left port Data Input/Output Lines

$A0_R$-$A9_R$ Right Port Address Inputs. The 10-bit field presented at the right port Address Inputs selects one of the 1024 memory locations to be read from or written into via the right port Data Input/Output Lines

$\overline{OE}_L$ Output Enable for Left Port When $\overline{OE}_L$ is HIGH, the left port outputs are disabled, when $\overline{OE}_L$ is LOW, the left port outputs are enabled. Also controls contention mode for left port

$\overline{OE}_R$ Output Enable for Right Port When $\overline{OE}_R$ is HIGH, the right port outputs are disabled When $\overline{OE}_R$ is LOW, the right port outputs are enabled Also controls contention mode for right port

$I/O0_L$-$I/O7_L$ Left Port Data Input/Output Lines.

$I/O0_R$-$I/O7_R$ Right Port Data Input/Output Lines

$R/\overline{W}_L$ Left Port Read/Write Enable When $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, data from the RAM location selected by the left address field is present at the left port Data Input/Output Lines When $R/\overline{W}_L$ is LOW, data present on the left port Data Input/Output Lines is written into the RAM location selected by the left address field irregardless of the state of $\overline{OE}_L$. These operations can be affected by contention (See Functional Description on page 9).

$R/\overline{W}_R$ Right Port Read/Write Enable When $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ is HIGH, data from the RAM location selected by the left address field is present at the right port Data Input/Output Lines When $R/\overline{W}_R$ is LOW, data present on the right port Data Input/Output Lines is written into the RAM location selected by the right address field irregardless of the state of $\overline{OE}_R$. These operations can be affected by contention (See Functional Description page 9).

$\overline{BUSY}_L$(12) Left Port Busy Flag $\overline{BUSY}_L$ remains HIGH at all times unless both ports initiate an operation to the same address location and the left port is operating in contention mode with the right port receiving priority When this occurs, the right port operation will be completed first and $\overline{BUSY}_L$ will go LOW until the right port operation is completed

$\overline{BUSY}_R$(12) Right Port Busy Flag $\overline{BUSY}_R$ remains HIGH at all times unless both ports initiate an operation to the same address location and the right port is operating in contention mode with the left port receiving priority When this occurs, the left port operation will be completed first and $\overline{BUSY}_R$ will go LOW until the left port operation is completed Both $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are open drain outputs allowing OR-tied operation

$\overline{INT}_L$(12) Left Port Interrupt Flag If the right port writes to memory location 3FE then $\overline{INT}_L$ is latched LOW until the left port reads data from memory location 3FE

$\overline{INT}_R$(12) Right Port Interrupt Flag If the left port writes to memory location 3FF, then $\overline{INT}_R$ is latched LOW until the right port reads data from memory location 3FF Both $\overline{INT}_L$ and $\overline{INT}_R$ are open drain allowing OR-tied operation

(see page 4 for notes)

Synertek.

SYM2147H

Military 4096 x 1 Static Random Access Memory

Extended Temperature Range (-55°C to +125°C)

Features

- 55 ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

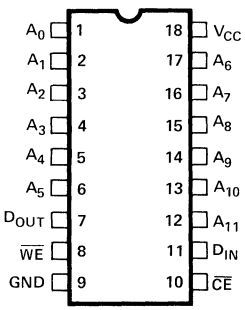
Description

The Synertek SYM2147H is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

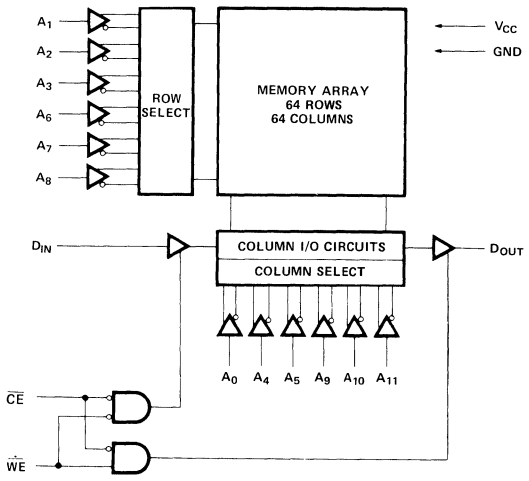
The SYM2147H offers an automatic power down feature Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus deselecting the SYM2147H, the device will automatically power down and remain in a standby power mode as long as CE remains high This unique feature provides system level power savings as much as 80%

The SYM2147H is packaged in an 18-pin DIP for the highest possible density The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground (under bias) ..... -3.5 V to +7 V
Power Dissipation ..... 1.2 W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% (Unless otherwise specified) (Note 8)

Symbol	Parameter	M2147H-3 Min.	M2147H-3 Max.	Unit	Conditions	
I_{LI}	Input Load Current (All input pins)		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}	
I_{LO}	Output Leakage Current		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4 5 V	
I_{CC}	Power Supply Current		140	mA	T_A = 25°C	V_{CC} = Max, $\overline{CS}$ = V_{IL}
			160	mA	T_A = -55°C	Outputs Open
I_{SB}	Standby Current		30	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}	
I_{PO}	Peak Power-on Current (Note 9)		50	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min	
V_{IL}	Input Low Voltage	-3 0	0.8	V		
V_{IH}	Input High Voltage	2 0	6 0	V		
V_{OL}	Output Low Voltage		0 4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2 4		V	I_{OH} = -4 0 mA	

Capacitance T_A = 25°C, f = 1.0 MHz

NOTE This parameter is periodically sampled and not 100% tested.

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

A.C. Test Conditions T_A = -55°C to +125°C, V_{CC} = 5V ± 10% (Unless otherwise specified) (Note 8)

READ CYCLE

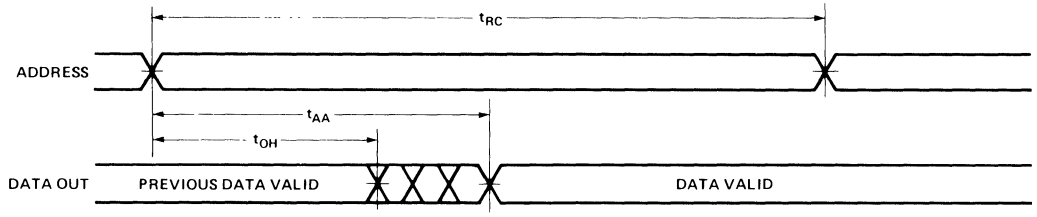
Symbol	Parameter	M2147H-2 Min.	M2147H-2 Max.	M2147H Min.	M2147H Max.	Unit	Conditions
t_{RC}	Read Cycle Time	55		70		ns	
t_{AA}	Address Access Time		55		70	ns	
t_{ACE1}	Chip Enable Access Time		55		70	ns	Note 1
t_{ACE2}	Chip Enable Access Time		65		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}	Chip Enabled to Output in Low Z	10		10		ns	Note 7
t_{HZ}	Chip Disabled to Output in High Z	0	40	0	40	ns	Note 7
t_{PU}	Chip Enabled to Power Up Time	0		0		ns	
t_{PD}	Chip Disabled to Power Down Time		30		30	ns	

WRITE CYCLE

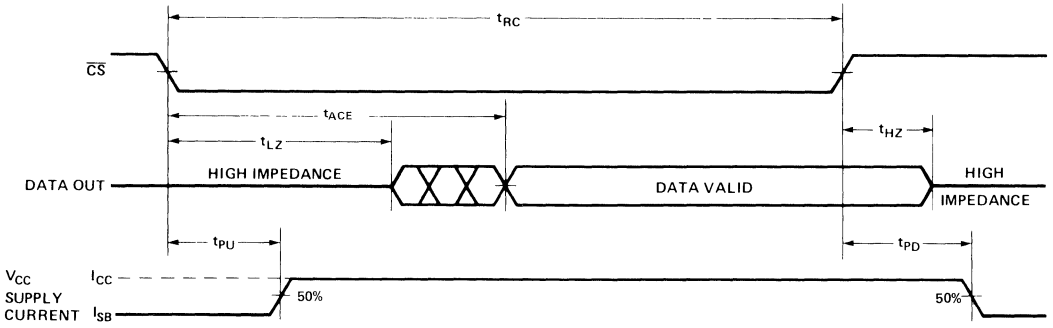
t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Enabled to End of Write	45		55		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	35		40		ns	
t_{WR}	Write Recovery Time	10		15		ns	
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	30	0	35	ns	Note 7
t_{OW}	Output Active from End of Write	0		0		ns	Note 7

Timing Diagrams

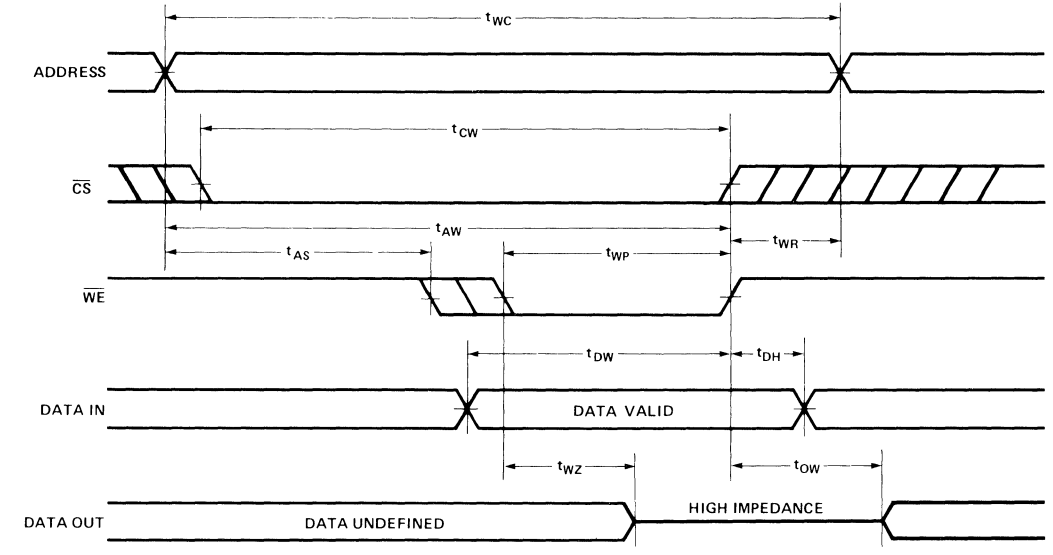
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)



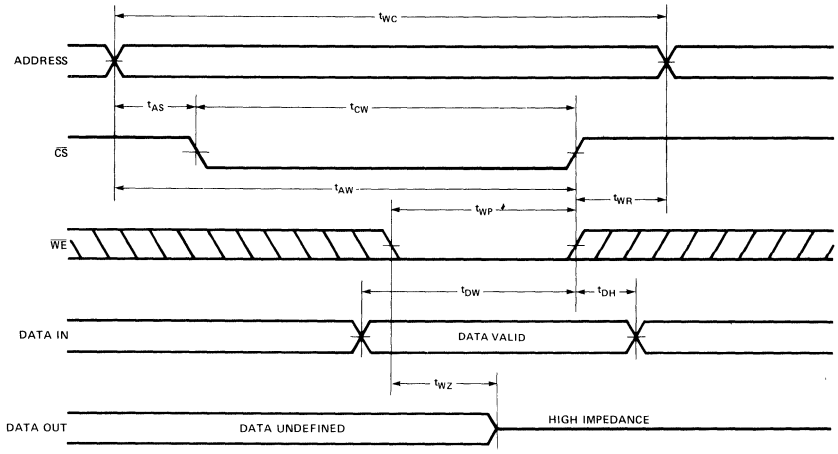
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



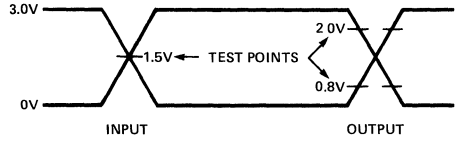
NOTES

1. Chip disabled for greater than 55ns prior to selection
2. Chip disabled for a finite time that is less than 55ns prior to selection (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No 1)
3. $\overline{WE}$ is high for Read Cycles
4. Device is continuously selected, $\overline{CE} = V_{IL}$
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low
6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
7. Transition is measured ±500mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected otherwise, power-on current approaches I_{CC} active
10. A minimum of 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (NOTE 6)

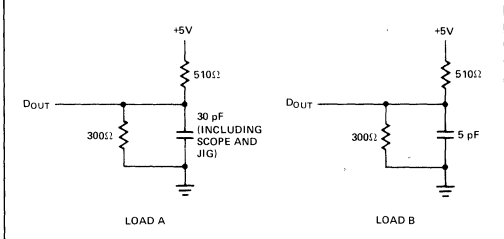


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability

18 Pin Cerdip
18 Pin Ceramic
18 Pin Leadless Chip Carrier

Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
SYMC2147H-3	55 ns	160 mA	30 mA	Ceramic
SYMD2147H-3	55 ns	160 mA	30 mA	Cerdip
SYMF2147H-3	55 ns	160 mA	30 mA	Flatpak
SYMC2147H	70 ns	160 mA	30 mA	Ceramic
SYMD2147H	70 ns	160 mA	30 mA	Cerdip
SYMF2147H	70 ns	160 mA	30 mA	Flatpak

Synertek.

SYM2148H

Military 1024 x 4 Static Random Access Memory

Extended Temperature Range (-55° C to +125° C)

Features

- 55ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Industry Standard 2114 Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 18-Pin Package
- Three-State Output

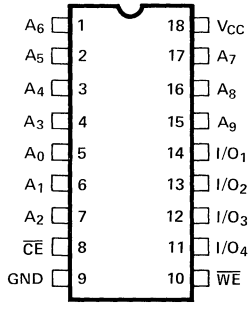
Description

The Synertek SYM2148H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data Common data input and output pins provide maximum design flexiblity The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices

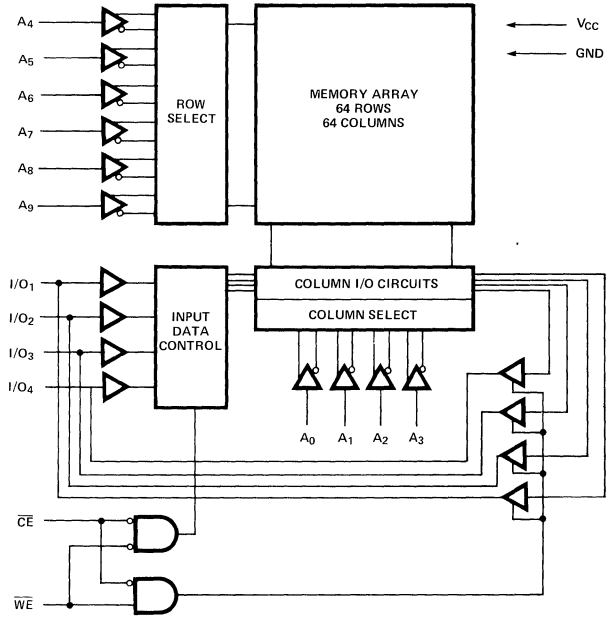
The SYM2148H offers an automatic power down feature Power down is controlled by the Chip Enable input When Chip Enable ($\overline{CE}$) goes high, thus deselecting the SY2148H, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high This unique feature provides system level power savings as much as 85%

The SYM2148H is packaged in an 18-pin DIP for the highest possible density The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground (under bias) ..... -3.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characterisitcs

T_A = -55°C to +125°C, V_{CC} = 5V ± 10% (Unless otherwise specified) (note 8)

Symbol	Parameter	Min.	Max.	Unit	Condition
I_{LI}	Input Load Current (All input pins)		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		130	mA	T_A = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}
			150	mA	T_A = -55°C; Outputs Open
I_{SB}	Standby Current		30	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
I_{PO}	Peak Power-on Current (Note 9)		50	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.1	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -4mA

Capacitance

T_A = 25°C, f = 1.0 MHz NOTE This parameter is periodically sampled and not 100% tested.

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

A.C. Characteristics

T_A = -55°C to +125°C, V_{CC} = 5V ± 10% (Unless otherwise specified) (note 8)

READ CYCLE

		M2148H-3		M2148H		
Symbol	Parameter	Min.	Max.	Min.	Max.	Conditions
t_{RC}	Read Cycle Time	55		70		
t_{AA}	Address Access Time		55		70	
t_{ACE1}	Chip Enable Access Time		55		70	Note 1
t_{ACE2}	Chip Enable Access Time		65		80	Note 2
t_{OH}	Output Hold from Address Change	5		5		
t_{LZ}	Chip Enabled to Output in Low Z	10		10		Note 7
t_{HZ}	Chip Disable to Output in High Z	0	20	0	20	Note 7
t_{PU}	Chip Enabled to Power Up Time	0		0		
t_{PD}	Chip Disable to Power Down Time		30		30	

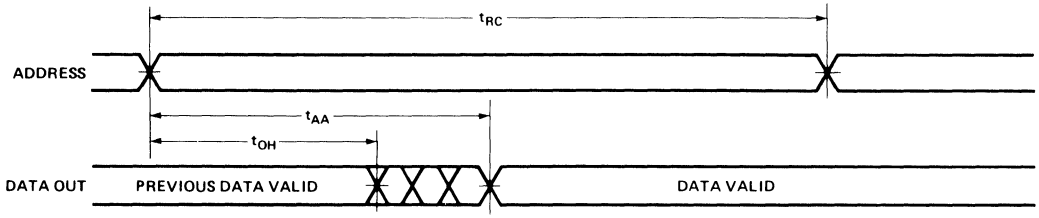
WRITE CYCLE

t_{WC}	Write Cycle Time	55		70		
t_{CW}	Chip Enabled to End of Write	50		65		
t_{AW}	Address Valid to End of Write	50		65		
t_{AS}	Address Setup Time	0		0		
t_{WP}	Write Pulse Width	40		50		
t_{WR}	Write Recovery Time	5		5		
t_{DW}	Data Valid to End of Write	20		25		
t_{DH}	Data Hold Time	0		0		
t_{WZ}	Write Enabled to Output in High Z	0	20	0	25	Note 7
t_{OW}	Output Active from End of Write	0		0		Note 7

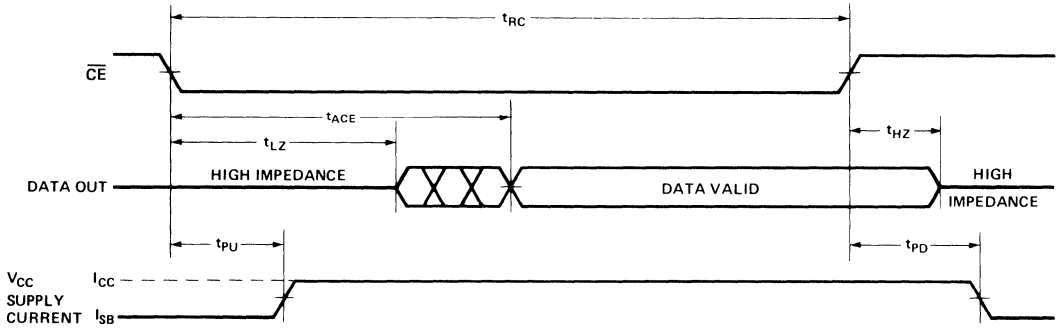
(See following page for notes)

Timing Diagrams

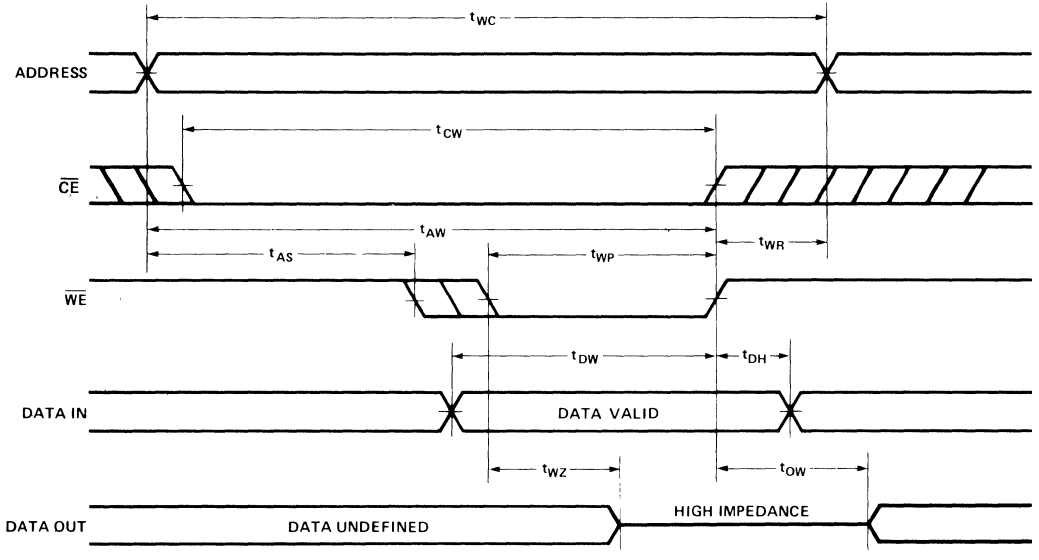
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)



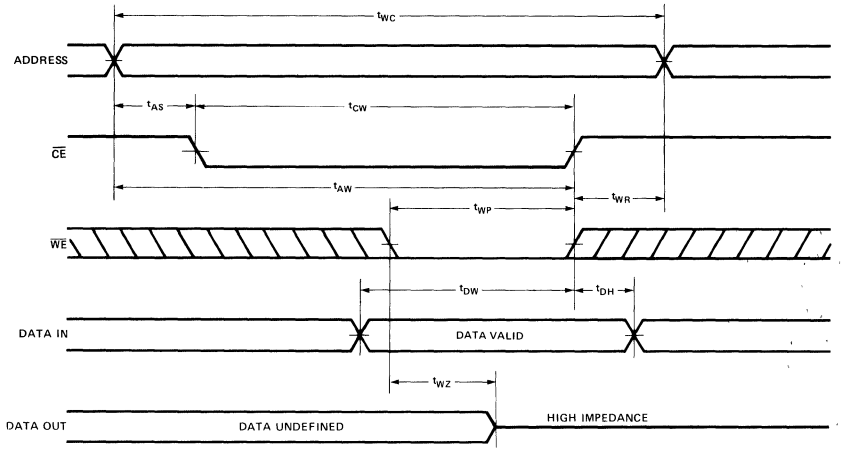
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



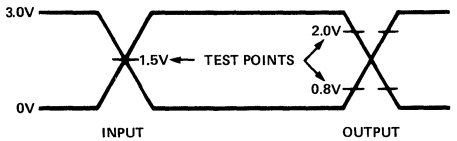
NOTES
1. Chip disabled for greater than 55ns prior to selection
2. Chip disabled for a finite time that is less than 55 ns prior to selection (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No 1)
3. $\overline{WE}$ is high for Read Cycles
4. Device is continuously selected, $\overline{CE} = V_{IL}$
5. Addresses valid prior to or coincident with $\overline{CE}$ transition low
6. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state
7. Transition is measured ±500mV from low or high impedance voltage with load B This parameter is sampled and not 100% tested
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute
9. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected. otherwise, power-on current approaches I_{CC} active
10. A minimum of 0 5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved

MILITARY

WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED) (NOTE 6)

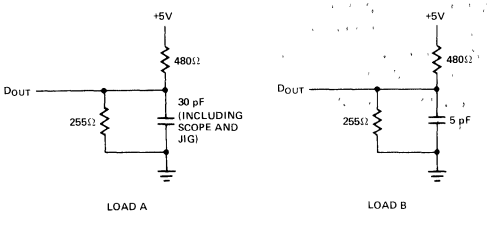


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability

18 Pin Cerdip
18 Pin Ceramic

Ordering Information

Order Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
SYMC2148H-3	55 ns	150 mA	30 mA	Ceramic
SYMD2148H-3	55 ns	150 mA	30 mA	Cerdip
SYMC2148H	70 ns	150 mA	30 mA	Ceramic
SYMD2148H	70 ns	150 mA	30 mA	Cerdip

Synertek.

SYM2149H

Military 1024 x 4 Static Random Access Memory

Extended Temperature Range (-55° C to +125° C)

Features

- 55 ns Maximum Address Access
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access Time: 25 ns Max.
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Industry Standard 2114 Pinout
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Outputs
- High Density 18-Pin Package
- Three-State Output

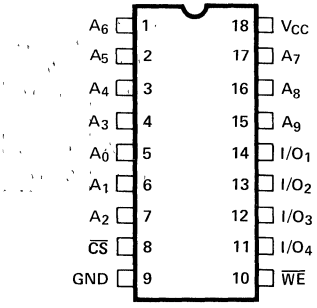
Description

The Synertek SYM2149H is a 4096-Bit Static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data Common data input and output pins provide maximum design flexibility The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices

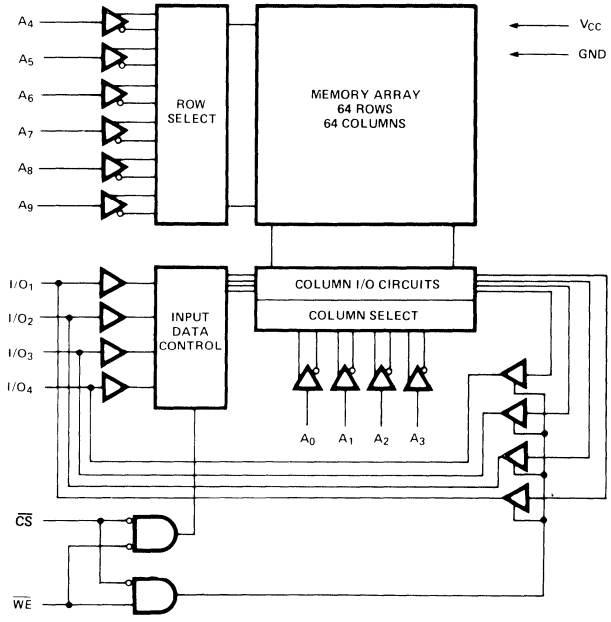
The SYM2149H offers a chip select access that is faster than address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, the decode time will not add to the overall access time thus significantly improving system performance

The SYM2149H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with
Respect to Ground (under bias) ..... -3.5 V to +7 V
Power Dissipation ..... 1.0 W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. Characterisitcs T_A = -55°C to +125°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{LI}	Input Load Current (all input pins).		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT}= Gnd to 4.5V
I_{CC}	Power Supply Current		130	mA	T_A = 25°C | V_{CC} = Max, $\overline{CS}$ = V_{IL}
			150	mA	T_A = -55°C | Outputs Open
V_{IL}	Input Low Voltage	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -4.0mA
I_{OS}	Output Short Circuit Current		±200	mA	V_{OUT} = GND to V_{CC} (Note 8)

Capacitance T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics T_A = -55°C to +125°C, V_{CC} = 5V ± 10% (Unless otherwise specified) (Note 6)

READ CYCLE

		M2149H-3		M2149			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle Time	55		70		ns	
t_{AA}	Address Access Time		55		70	ns	
t_{ACS}	Chip Select Access Time		25		30	ns	
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		5		ns	Note 5
t_{HZ}	Chip Deselection to Output in High Z	0	15	0	15	ns	Note 5

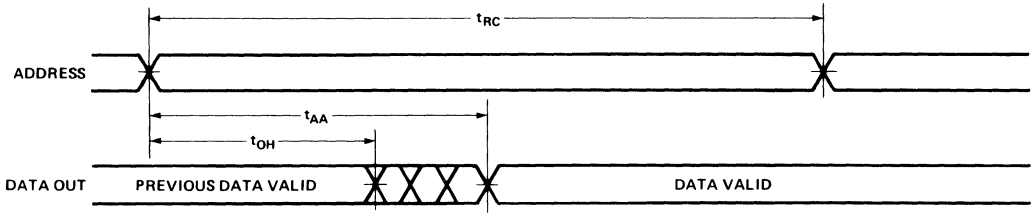
WRITE CYCLE

t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Selection to End of Write	50		65		ns	
t_{AW}	Address Valid to End of Write	50		65		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	40		50		ns	
t_{WR}	Write Recovery Time	5		5		ns	
t_{DW}	Data Valid to End of Write	20		25		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	20	0	25	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		ns	Note 5

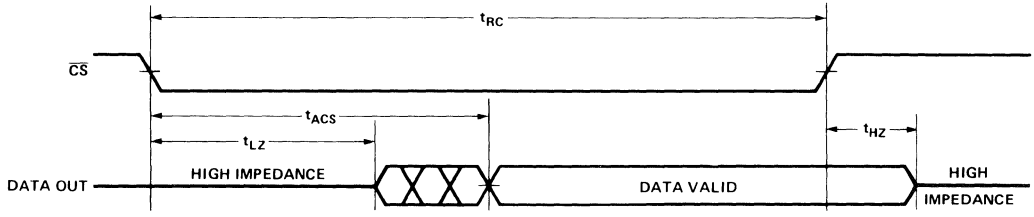
(See following page for notes)

Timing Diagrams

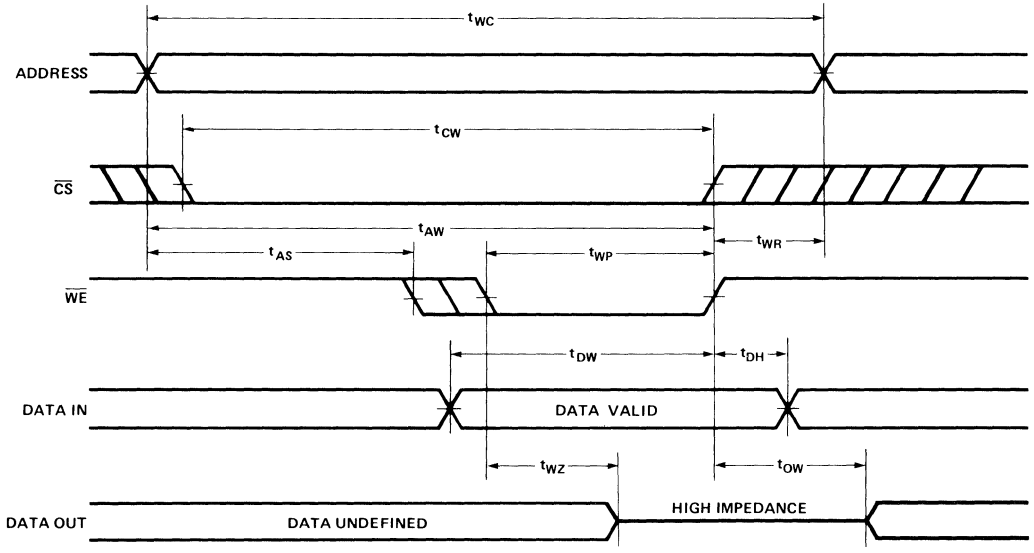
READ CYCLE NO. 1 (NOTES 1 AND 2)



READ CYCLE NO. 2 (NOTES 1 AND 3)

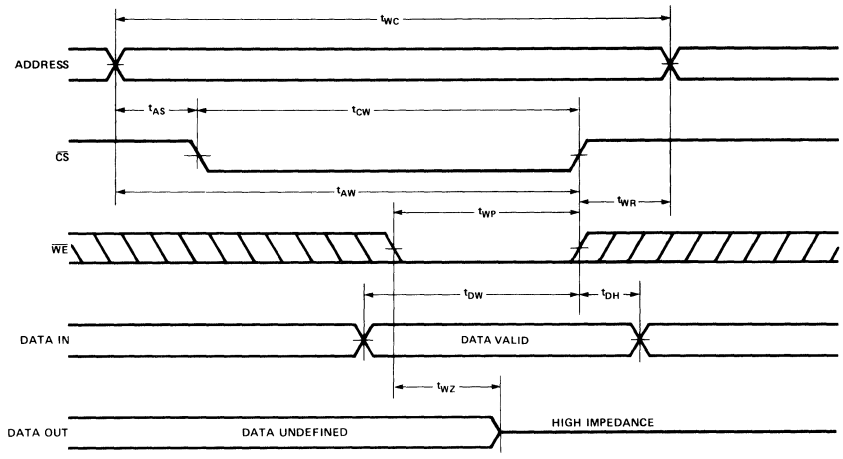


WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 4)

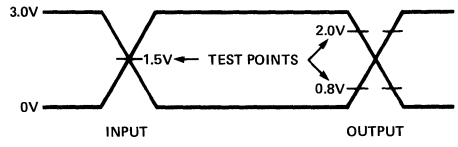


NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid.
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
7. A minimum of 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.
8. Duration not to exceed one minute.

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (NOTE 4)

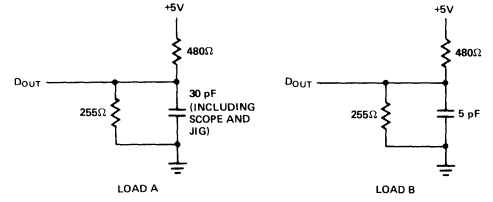


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability

18 Pin Cerdip
18 Pin Ceramic

Ordering Information

Order Number	Access Time (Max)	Supply Current (Max)	Package Type
SYMC2149H-3	55 nsec	150 mA	Ceramic
SYMD2149H-3	55 nsec	150 mA	Cerdip
SYMC2149H	70 nsec	150 mA	Ceramic
SYMD2149H	70 nsec	150 mA	Cerdip

Synertek.

SYM2167

Military 16,384 x 1 Static Random Access Memory

Extended Temperature Range (-55°C to +125°C)

PRELIMINARY INFORMATION

Features

- 55 ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply
- Available in Ceramic (C), Cerdip (D), Flatpack (F), and Leadless Chip Carrier (K)
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 20 Pin Package
- Three-State Output

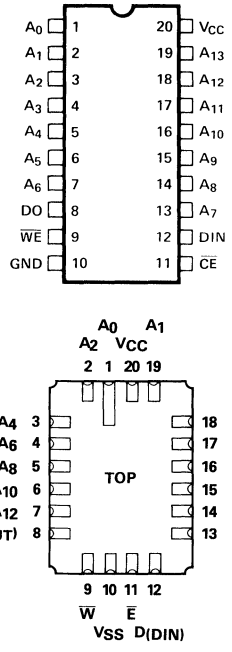
Description

The Synertek SYM2167 is a 16,384-bit Static Random Access Memory organized 16,384 words by 1-bit and is fabricated using Synertek's new N-channel Double Polysilicon Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices

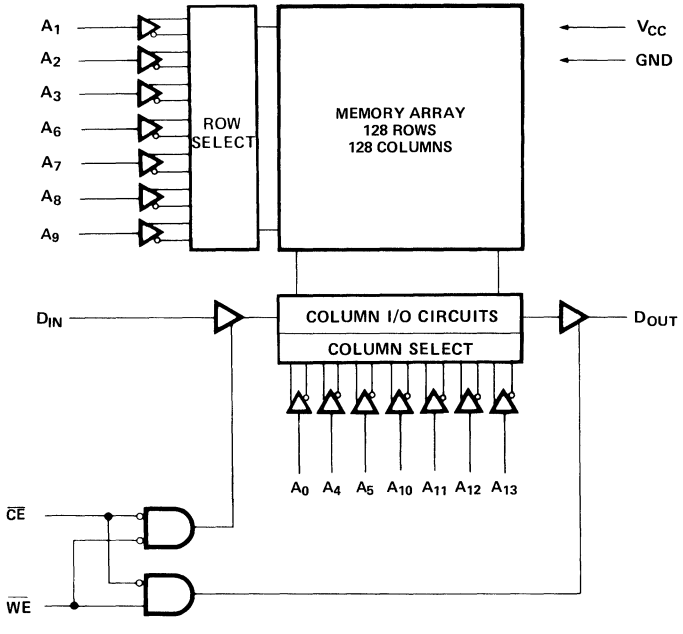
The SYM2167 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus deselecting the SYM2167, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 80%.

The SYM2167 is available in 20-pin DIP and 20-lead Leadless Chip Carrier packages for the highest possible density. The device is fully TTL compatible and has a single +5 V power supply.

Pin Configuration



Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Units	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} = Max., V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max. V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		110	mA	$T_A = 25°C$ | V_{CC} = Max., $\overline{CE} = V_{IL}$
			150	mA	$T_A = -55°C$ | Outputs Open
I_{SB}	Standby Current		30	mA	V_{CC} = Min. to Max., $\overline{CE} = V_{IH}$
I_{PO}	Peak Power-on Curent (Note 7)		60	mA	V_{CC} = Gnd to V_{CC} Min. $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	−3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 16mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4mA
I_{OS}	Output Short Circuit Current (Note 8)	−150	300	mA	V_{OUT} = GND to V_{CC} (Note 8)

Capacitance

$T_A = 25°C$, f = 1.0MHz

Note: This parameter is periodically sampled and not 100% tested.

Symbol	Test	Typ.	Max.	Units
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

A.C. Characteristics

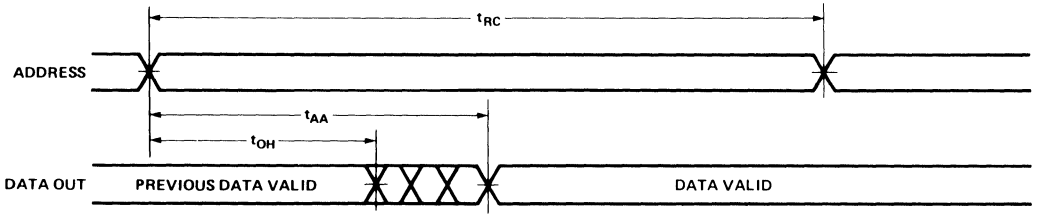
$T_A = -55°C$, to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Notes 6, 9)

		2167-70		2167-55			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	Conditions
READ CYCLE							
t_{RC}	Read Cycle Time	65		55		ns	
t_{AA}	Address Access Time		65		50	ns	
t_{ACE}	Chip Enable Access Time		70		55	ns	
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		5		ns	
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	30	ns	
t_{PU}	Chip Selection to Power Up Time	0		0		ns	
t_{PD}	Chip Deselection to Power Down Time	0	70		55	ns	
WRITE CYCLE							
t_{WC}	Write Cycle Time	65		55		ns	
t_{CW}	Chip Selection to End of Write	60		50		ns	
t_{AW}	Address Valid to End of Write	55		50		ns	
t_{AS}	Address Setup Time	8		0		ns	
t_{WP}	Write Pulse Width	30		25		ns	
t_{WR}	Write Recovery Time	10		0		ns	
t_{DW}	Data Valid to End of Write	23		20		ns	
t_{DH}	Data Hold Time	8		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	28	0	25	ns	
t_{OW}	Output Active from End of Write	0	40	0	30	ns	

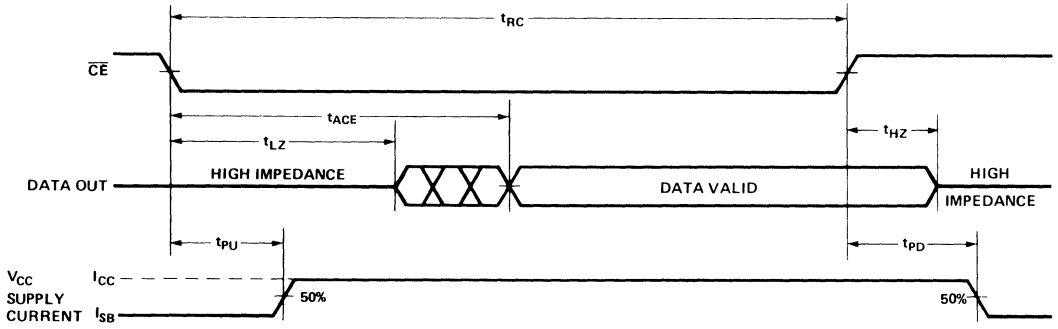
(See following page for notes)

Timing Diagrams

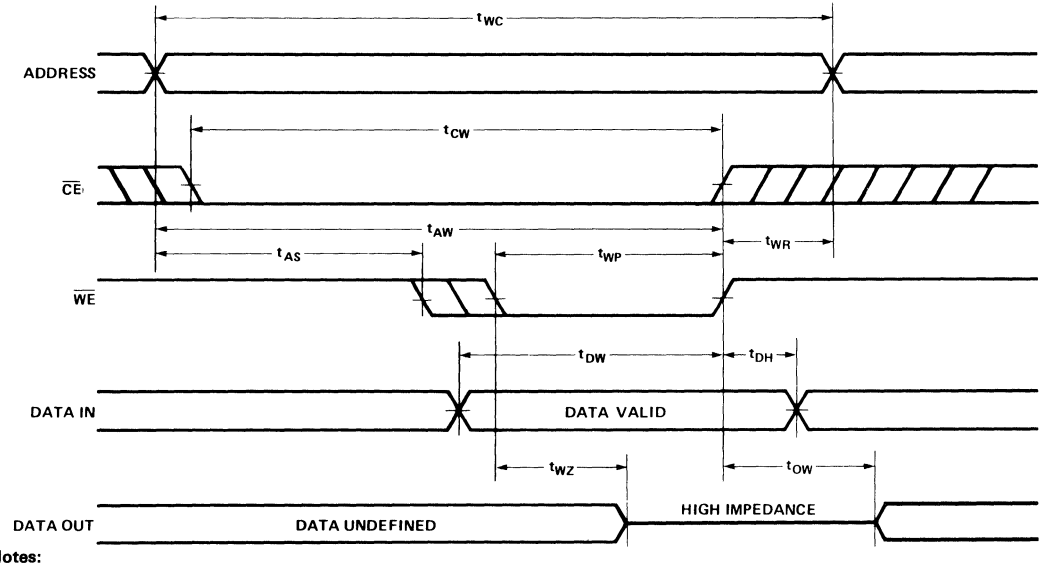
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



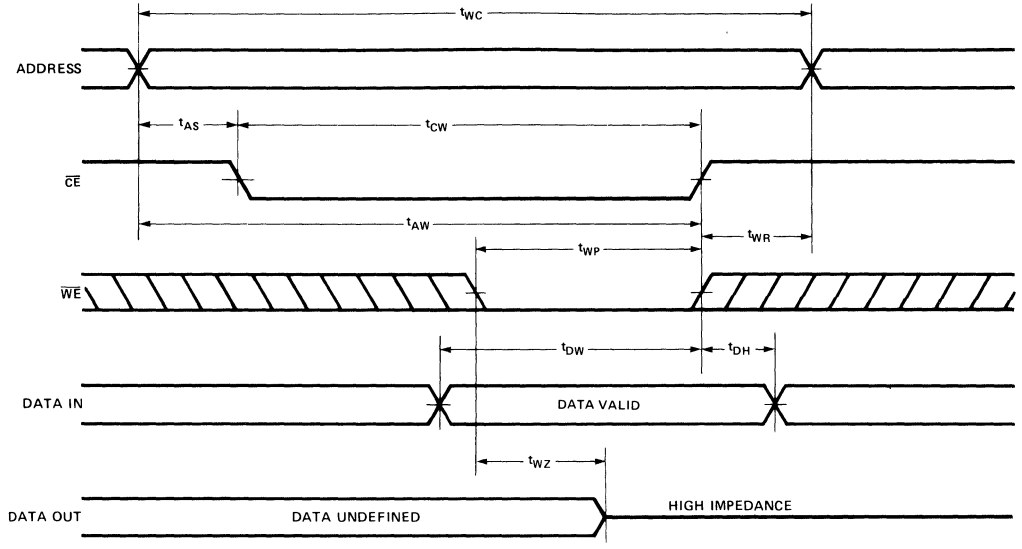
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled) (Note 4)



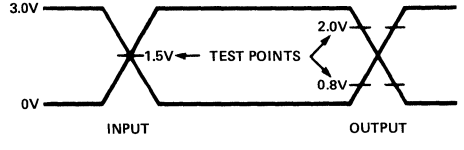
Notes:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. The operating ambient temperature range is guaranteed with transverse air flow excedding 400 linear feet per minute.
7. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
8. Duration not to exceed one second.
9. A minimum 0.5ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

MILITARY

WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled) (Note 4)

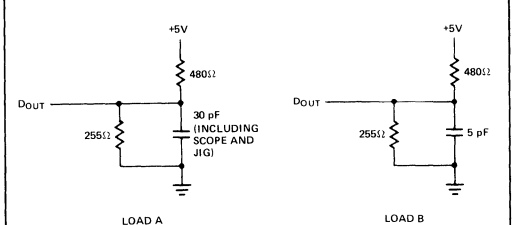


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns

A.C. Testing Load Circuit



Package Availability

20 Lead Cerdip
20 Lead Ceramic
20 Lead Flatpack
20 Lead LCC

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYMC2167-70	70 ns	150 mA	30 mA	Ceramic
SYMD2167-70	70 ns	150 mA	30 mA	Cerdip
SYMK2167-70	70 ns	150 mA	30 mA	LCC
SYMF2167-70	70 ns	150 mA	30 mA	Flatpack
SYMC2167-55	55 ns	150 mA	30 mA	Ceramic
SYMD2167-55	55 ns	150 mA	30 mA	Cerdip
SYMK2167-55	55 ns	150 mA	30 mA	LCC
SYMF2167-55	55 ns	150 mA	30 mA	Flatpack

Synertek.

SYM2168
Military 4096 x 4 Static Random Access Memory
Extended Temperature Range (-55° C to +125° C)

PRELIMINARY INFORMATION

Features

- 55 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Available in Ceramic (C), Cerdip (D), Flatpack (F), and Leadless Chip Carrier (K)
- JEDEC Standard Pinout
- TTL Compatible: Inputs and Outputs
- Common Data Input and Output
- High Density 20-Pin Package
- Three-State Output

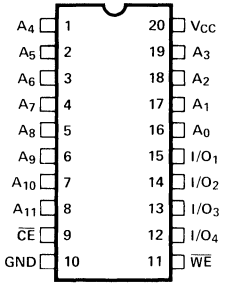
Description

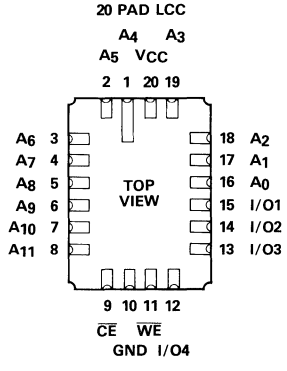
The Synertek SYM2168 is a 16,384-bit Static Random Access Memory organized 4096 words by 4 bits and is fabricated using Synertek's scaled N-channel double poly silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

The SYM2168 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable (CE) goes high, thus deselecting the SYM2168, the device will automatically power down and remain in a standby power mode as long as CE remains high. This unique feature provides system level power savings as much as 85%.

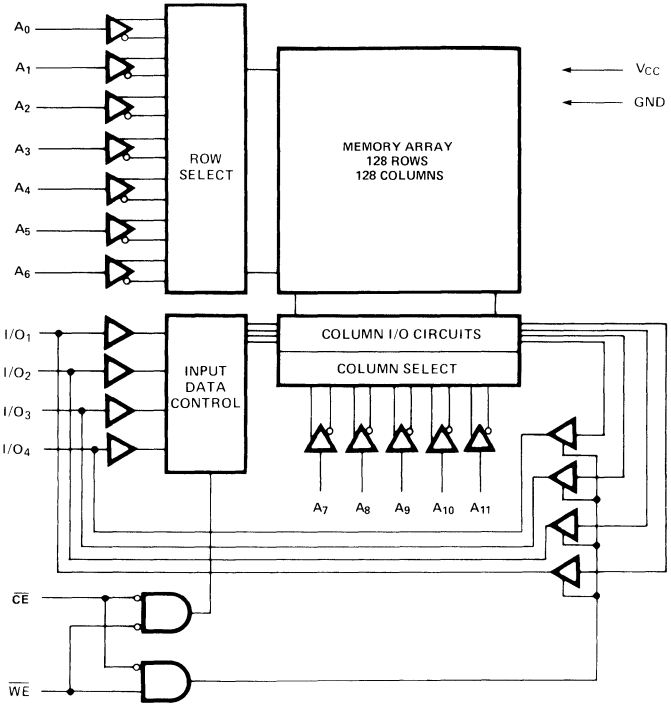
The SYM2168 is available in 20-pin DIP and 20-lead Leadless Chip Carrier packages for the highest possible density. The device is fully TTL compatible and has a single +5 V power supply.

Pin Configuration





Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Units	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} = Max., V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50	μA	$\overline{CE} = V_{IH}$, V_{CC} = Max. V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		110	mA	$T_A = 25°C$ | V_{CC} = Max., $\overline{CE} = V_{IL}$
			150	mA	$T_A = -55°C$ | Outputs Open
I_{SB}	Standby Current		30	mA	V_{CC} = Min. to Max., $\overline{CE} = V_{IH}$
I_{PO}	Peak Power-on Curent (Note 7)		60	mA	V_{CC} = Gnd to V_{CC} Min. $\overline{CE}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	−3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4mA
I_{OS}	Output Short Circuit Current	−200	+200	mA	V_{OUT} = GND to V_{CC} (Note 9)

Capacitance

$T_A = 25°C$, f = 1.0MHz

Symbol	Test	Typ.	Max.	Units
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

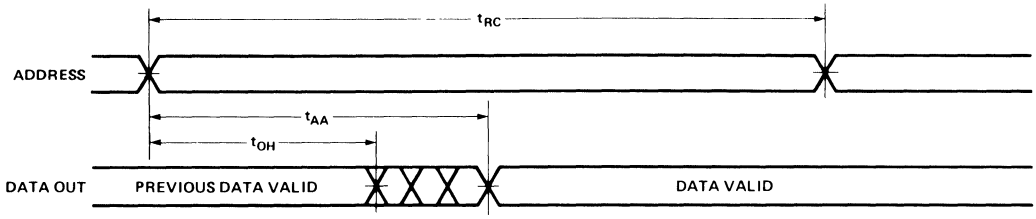
$T_A = -55°C$, to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Notes 6, 8)

		2168-70		2168-55			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	Conditions
READ CYCLE							
t_{RC}	Read Cycle Time	70		55		ns	
t_{AA}	Address Access Time		70		55	ns	
t_{ACE}	Chip Enable Access Time		70		55	ns	
t_{OH}	Output Hold from Address Change	3		3	0	ns	
t_{LZ}	Chip Selection to Output in Low Z	20		20		ns	
t_{HZ}	Chip Deselection to Output in High Z	0	30	0	25	ns	
t_{PU}	Chip Selection to Power Up Time	0		0		ns	
t_{PD}	Chip Deselection to Power Down Time	0	70		55	ns	
WRITE CYCLE							
t_{WC}	Write Cycle Time	70		55		ns	
t_{CW}	Chip Enabled to End of Write	65		45		ns	
t_{AW}	Address Valid to End of Write	65		45		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	65		45		ns	
t_{WR}	Write Recovery Time	5		3		ns	
t_{DW}	Data Valid to End of Write	30		20		ns	
t_{DH}	Data Hold Time	5		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	30	0	25	ns	
t_{OW}	Output Active from End of Write	0		0		ns	

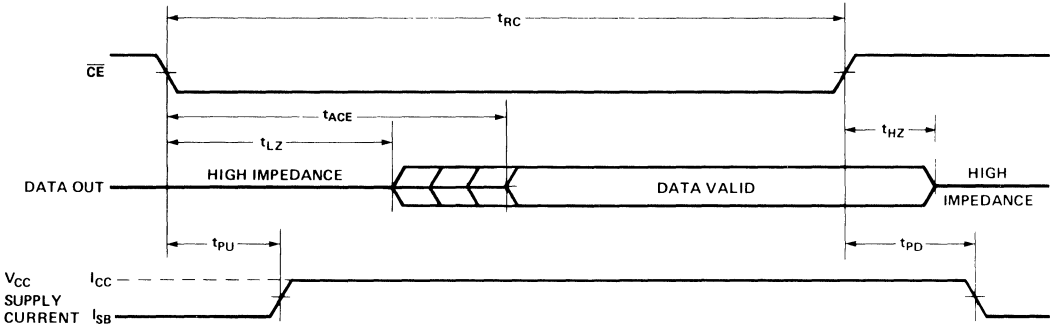
(See following page for notes)

Timing Diagrams

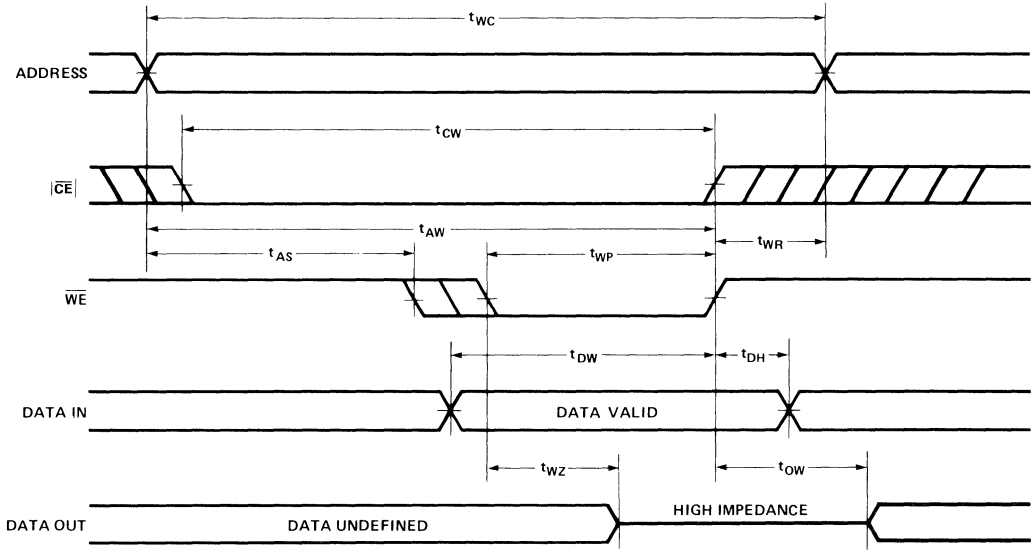
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)



WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled) (Note 4)

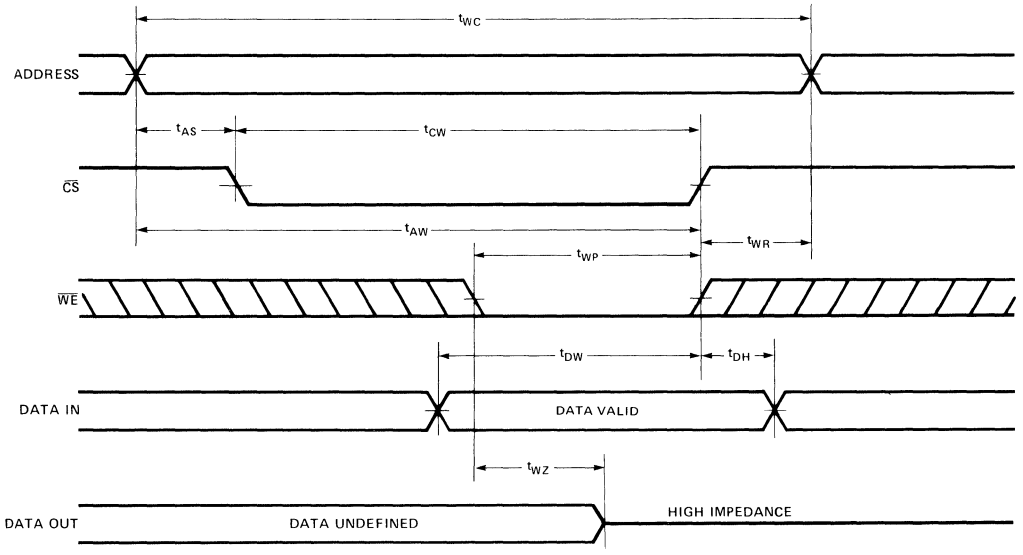


NOTES

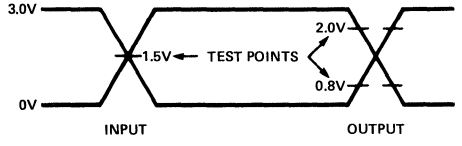
1. $\overline{WE}$ is high for Read Cycles
2. Device is continuously selected, $\overline{CE} = V_{IL}$
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low
4. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500 mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
7. A pullup resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.
8. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

MILITARY

WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled) (Note 4)

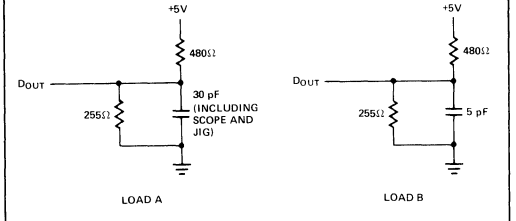


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V. INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability

20 Pin Ceramic
20 Pin Cerdip
20 Pin Flatpack
20 Lead LCC

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYMC2168-70	70 ns	150 mA	30 mA	Ceramic
SYMD2168-70	70 ns	150 mA	30 mA	Cerdip
SYMF2168-70	70 ns	150 mA	30 mA	Flatpack
SYMK2168-70	70 ns	150 mA	30 mA	LCC
SYMC2168-55	55 ns	150 mA	30 mA	Ceramic
SYMD2168-55	55 ns	150 mA	30 mA	Cerdip
SYMF2168-55	55 ns	150 mA	30 mA	Flatpack
SYMK2168-55	55 ns	150 mA	30 mA	LCC

Synertek.

SYM2169
Military 4096 x 4 Static Random Access Memory
Extended Temperature Range (-55°C to +125°C)

ADVANCED INFORMATION

Features

- 55 ns Maximum Address Access Times
- Fully Static Operation. No Clocks or Strobes Required
- Fast Chip Select Access Time 50 ns Max
- Identical Cycle and Access Times
- Single +5V Supply
- Available in Ceramic (C), Cerdip (D), Flatpack (F), and Leadless Chip Carrier (K)
- JEDEC Standard Pinout
- TTL Compatible Inputs and Outputs
- Common Data Input and Outputs
- High Density 20-Pin Package
- Three-State Output

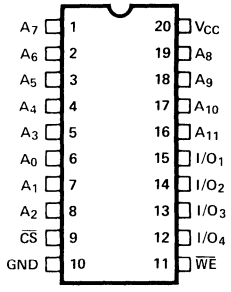
Description

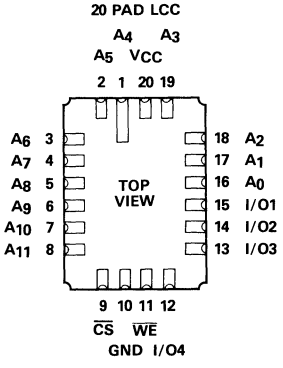
The Synertek SYM2169 is a 16,384-bit Static Random Access Memory organized 4096 words by 4 bits and is fabricated using Synertek's N-channel double poly silicon gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices

The SYM2169 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance

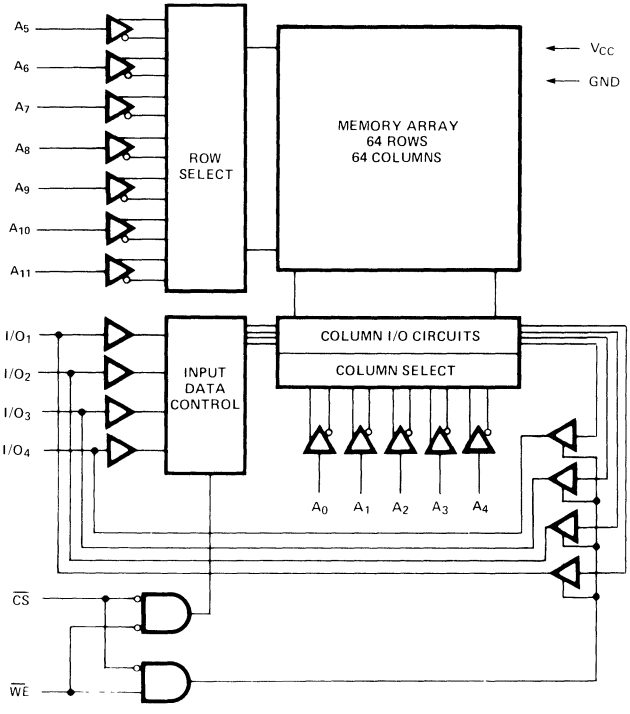
The SYM2169 is available in 20-pin DIP and 20-lead Leadless Chip Carrier packages for the highest possible density. The device is fully TTL compatible and has a single +5 V power supply.

Pin Configuration





Block Diagram



MILITARY

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.0W

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Note 6)

Symbol	Parameter	Min.	Max.	Units	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{CC} = Max., V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		50	μA	$\overline{CS} = V_{IH}$, V_{CC} = Max. V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		110	mA	$T_A = 25°C$ | V_{CC} = Max., $\overline{CS} = V_{IL}$
			150	mA	$T_A = -55°C$ | Outputs Open
V_{IL}	Input Low Voltage	−3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −4mA
I_{OS}	Output Short Circuit Current	−200	+200	mA	V_{OUT} = Gnd to V_{CC} (Note 7)

Capacitance

$T_A = 25°C$, f = 1.0MHz

Symbol	Test	Typ.	Max.	Units
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

Note: This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

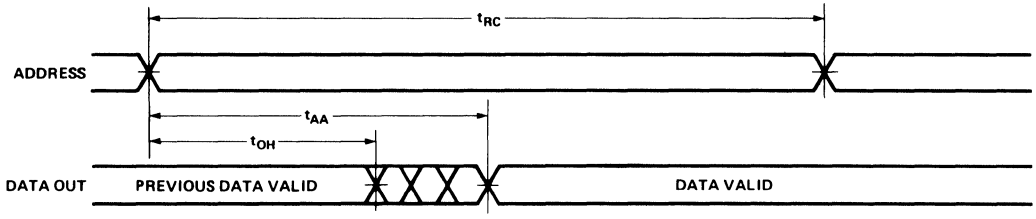
$T_A = -55°C$, to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified) (Notes 6, 8)

		2169-70		2169-55			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Condition
READ CYCLE							
t_{RC}	Read Cycle Time	70		55		ns	
t_{AA}	Address Access Time		65		50	ns	
t_{ACE}	Chip Select Access Time		70		55	ns	
t_{OH}	Output Hold from Address Change	5		3		ns	
t_{LZ}	Chip Selection to Output in Low Z	20		20		ns	
t_{HZ}	Chip Deselection to Output in High Z	0	30	0	25	ns	
WRITE CYCLE							
t_{WC}	Write Cycle Time	70		55		ns	
t_{CW}	Chip Selection to End of Write	60		45		ns	
t_{AW}	Address Valid to End of Write	60		45		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	60		45		ns	
t_{WR}	Write Recovery Time	5		3		ns	
t_{DW}	Data Valid to End of Write	25		20		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	30	0	25	ns	
t_{OW}	Output Active from End of Write	0		0		ns	

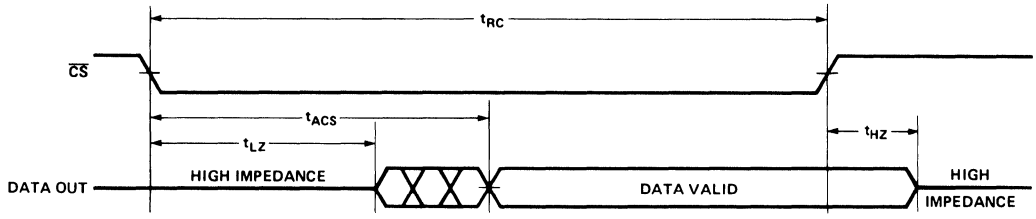
(See following page for notes)

Timing Diagrams

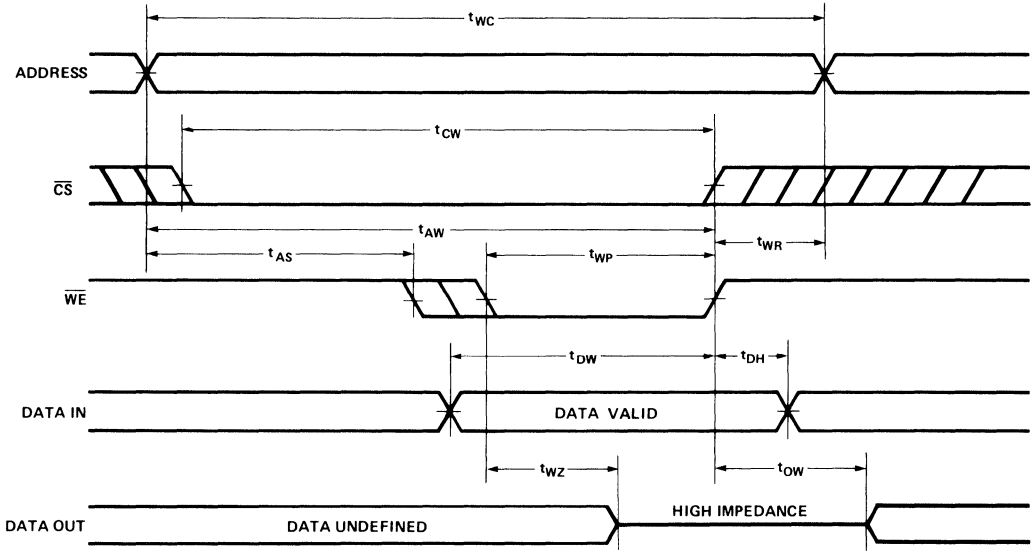
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)

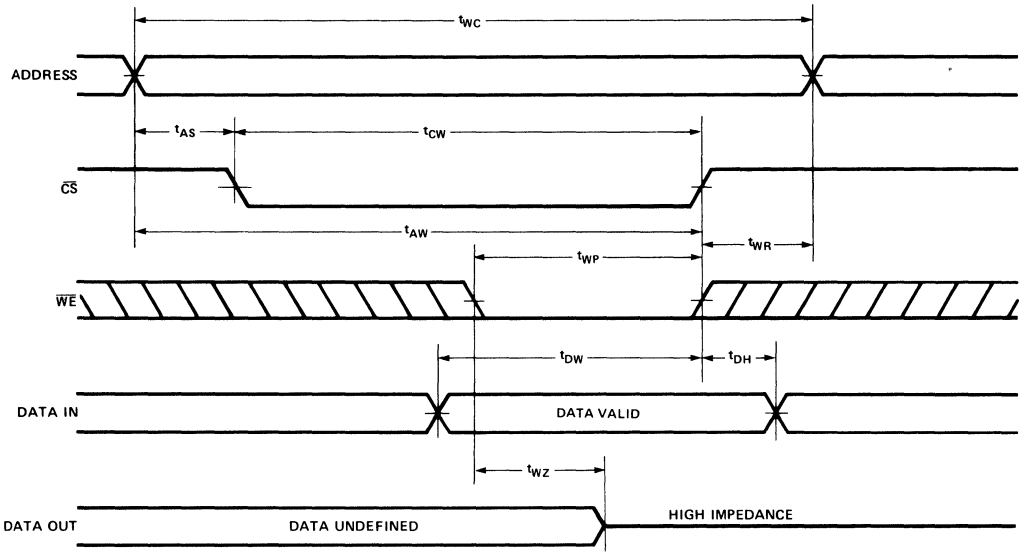


WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 4)

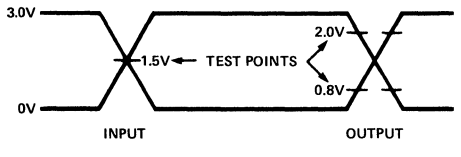


Notes:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid.
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
7. Duration not to exceed one second.
8. A minimum 0.5ms time delay is required after application of V_{CC} (±5V) before proper device operation is achieved.

WRITE CYCLE NO. 2 ($\overline{CS}$ controlled) (Note 4)

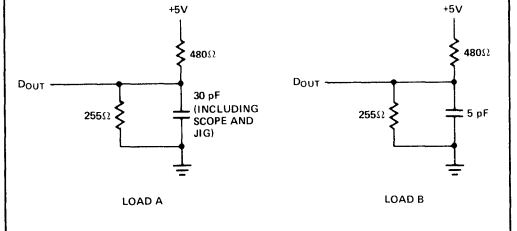


A.C. Testing Input, Output Waveform



A.C. TESTING: INPUTS ARE DRIVEN AT 3.0V FOR A LOGIC "1" AND 0.0V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0" AT THE OUTPUTS. THE INPUTS ARE MEASURED AT 1.5V INPUT RISE AND FALL TIMES ARE 5 ns.

A.C. Testing Load Circuit



Package Availability

20 Pin Ceramic
20 Pin Cerdip
20 Pin Flatpack
20 Lead LCC

Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Package Type
SYMC2169-70	70 ns	150 mA	Ceramic
SYMD2169-70	70 ns	150 mA	Cerdip
SYMF2169-70	70 ns	150 mA	Flatpack
SYMK2169-70	70 ns	150 mA	LCC
SYMC2169-55	55 ns	150 mA	Ceramic
SYMD2169-55	55 ns	150 mA	Cerdip
SYMF2169-55	55 ns	150 mA	Flatpack
SYMK2169-55	55 ns	150 mA	LCC

Microprocessors. 4

Microprocessor Cross Reference Guide

Synertek Part Number	SY6502-7	SY6512	SY6522	SY6551	SY6545R	SY2661-1	SY2661-2	SY2661-3	SYZ8601
Rockwell	6502-7	6512	6522	6551					
Motorola					6845R	68661A	68661B	68661C	
MOSTEC	6502-7	6512	6522	6551					
Zilog									Z8601
SGS									Z8601
Sharpe									Z8601
SMC						2661-1	2661-2	2661-3	
AMI				6551					
Signetics						2661A	2661B	2661C	
Hitachi					6845R				

Synertek.

SY2661

Enhanced Programmable Communications Interface

Features

SYNCHRONOUS OPERATION

- 5 to 8-bit characters plus parity
- Single or double SYN operation
- Internal or external character synchronization
- Transparent or non-transparent mode
- Transparent mode DLE stuffing (Tx) and detection (Rx)
- Automatic SYN or DLE-SYN insertion
- SYN, DLE and DLE-SYN stripping
- Odd, even, or no parity
- Local or remote maintenance loop back mode
- Baud rate: dc to 1M bps (1X clock)

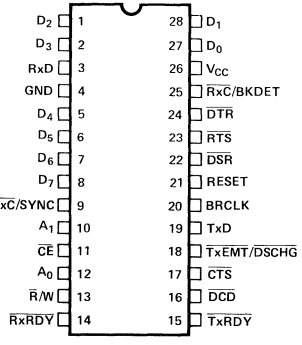
ASYNCHRONOUS OPERATION

- 5 to 8-bit characters plus parity
- 1, 1½ or 2 stop bits transmitted
- Odd, even, or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loop back mode
- Baud rate: dc to 1M bps (1X clock)
  - — dc to 62.5K bps (16X clock)
  - — dc to 15 625K bps (64X clock)

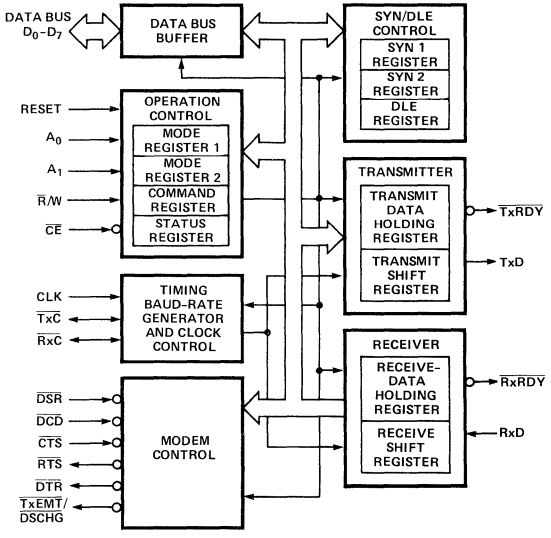
OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets (2661-1, -2, -3)
- 16 internal rates for each set
- Double buffered transmitter and receiver
- Dynamic character length switching
- Full or half duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short circuit protected
- 3 open drain MOS outputs can be wire-ORed
- Single 5V power supply
- No system clock required
- 28-pin dual-in-line package

Pin Configuration



Block Diagram



MICRO-PROCESSORS

Table 1 Baud Rate Generator Characteristics

2661-1 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	—	6144
0	0	0	1	75	1 2	—	4096
0	0	1	0	110	1.7598	-0.01	2793
0	0	1	1	134.5	2 152	—	2284
0	1	0	0	150	2.4	—	2048
0	1	0	1	200	3 2	—	1536
0	1	1	0	300	4.8	—	1024
0	1	1	1	600	9.6	—	512
1	0	0	0	1050	16 8329	0.196	292
1	0	0	1	1200	19.2	—	256
1	0	1	0	1800	28.7438	-0.19	171
1	0	1	1	2000	31.9168	-0.26	154
1	1	0	0	2400	38.4	—	128
1	1	0	1	4800	76 8	—	64
1	1	1	0	9600	153.6	—	32
1	1	1	1	19200	307.2	—	16

2661-2 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	45 5	0.7279	0.005	6752
0	0	0	1	50	0.8	—	6144
0	0	1	0	75	1.2	—	4096
0	0	1	1	110	1.7598	-0.01	2793
0	1	0	0	134 5	2.152	—	2284
0	1	0	1	150	2.4	—	2048
0	1	1	0	300	4.8	—	1024
0	1	1	1	600	9 6	—	512
1	0	0	0	1200	19.2	—	256
1	0	0	1	1800	28 7438	-0.19	171
1	0	1	0	2000	31 9168	-0.26	154
1	0	1	1	2400	38.4	—	128
1	1	0	0	4800	76.8	—	64
1	1	0	1	9600	153 6	—	32
1	1	1	0	19200	307.2	—	16
1	1	1	1	38400	614.4	—	8

2661-3 (BRCLK = 5.0688 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	—	6336
0	0	0	1	75	1.2	—	4224
0	0	1	0	110	1.76	—	2880
0	0	1	1	134.5	2.1523	0 016	2355
0	1	0	0	150	2.4	—	2112
0	1	0	1	300	4 8	—	1056
0	1	1	0	600	9.6	—	528
0	1	1	1	1200	19 2	—	264
1	0	0	0	1800	28.8	—	176
1	0	0	1	2000	32 081	0.253	158
1	0	1	0	2400	38 4	—	132
1	0	1	1	3600	57.6	—	88
1	1	0	0	4800	76,8	—	66
1	1	0	1	7200	115 2	—	44
1	1	1	0	9600	153 6	—	33
1	1	1	1	19200	316 8	3 125	16

Note 16X CLK is used in asynchronous mode In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC

Signal Descriptions

CPU Interface

RESET (Reset)

A high on this input performs a master reset on the SY2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words

A_0, A_1 (Address 0, 1)

Address lines used to select the internal registers.

$\overline{R}/W$ (Read/Write)

The direction of data transfers between the EPCI and the CPU is controlled by the $\overline{R}/W$ input. When $\overline{CE}$ and $\overline{R}/W$ are both low the contents of the selected registers will be transferred to the data bus. With $\overline{CE}$ low and $\overline{R}/W$ high a write to the selected register is performed

$\overline{CE}$ (Chip Enable)

When low, the selected register will be accessed When high the D_0-D_7 lines will be placed in the high impedance state

DB_0-DB_7 (Data Bus)

An 8-bit three-state positive true data bus used to transfer commands, data and status between the EPCI and the CPU

$\overline{TxRDY}$ (Transmitter Ready)

This output is the complement of status register bit SR0 When low, it indicates that the transmit data holding register (TxHR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled It is an open drain output which can be "wire-ORed" to the CPU interrupt.

$\overline{RxRDY}$ (Receiver Ready)

This output is the complement of status register bit SR1 When low, it indicates that the receive data holding register (RxHR) has a character ready for input to the CPU It goes high when the RxHR is read by the CPU and also when the receiver is disabled It is an open drain output which can be "wire-ORed" to the CPU interrupt line

$\overline{TxEMT}/\overline{DSCHG}$

This output is the complement of status register bit SR2 When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred This output goes high when the status register is read by the CPU if the TxEMT condition does not exist Otherwise, the TxHR must be loaded by the CPU for this line to go high It is an open drain output which can be "wire OR-ed" to the CPU interrupt line

Transmitter/Receiver Signals

BRCLK (Baud Rate Clock)

Clock input to the internal baud rate generator. This is not required when external receiver and transmitter clocks are used.

$\overline{RxC}$/BKDET (Receiver Clock, Break Detect)

When the EPCI is programmed for External Receiver Clock, this pin will act as an input and control the rate at which a character is received The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate Data are sampled on the rising edge. If internal Receiver Clock is programmed this pin will provide an output, either a 1X/16X clock or Break Detect signal determined by programming Mode Register 2

$\overline{TxC}$/XSYNC (Transmitter Clock/External SYNC)

When the EPCI is programmed for External Transmitter clock, this pin will act as an input and control the rate at which the character is transmitted The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate Data changes on the falling edge of this clock. If the UPCI is programmed for Internal Transmitter clock, this pin can be either an output providing a 1X/16X clock or an input for External Synchronization determined by Mode Register 2 programming.

RxD (Receive Data)

RxD is the serial data input to the receiver.

TxD (Transmit Data)

TxD is the serial data output from the transmitter. When the transmitter is disabled the output will be in the high, "Mark", state

$\overline{DSR}$ (Data Set Ready)

$\overline{DSR}$ is an input that can be used to indicate to the UPCI Data Set Ready or Ring Indicator. Its complement appears in the Status Register as bit SR7. A change of state on $\overline{DSR}$ will cause $\overline{TxEMT}/\overline{DSCHG}$ to go low if either CR0 or CR2 = 1.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input must be low for the receiver to operate If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited The complement of $\overline{DCD}$ appears in the Status Register as bit SR6 A change of state in $\overline{DCD}$ will cause $\overline{TxEMT}/\overline{DSCHG}$ to go low if either CR0 or CR2 = 1.

$\overline{CTS}$ (Clear To Send)

The $\overline{CTS}$ input must be low for the transmitter to operate. If $\overline{CTS}$ goes high while transmitting, the character currently in the Transmit Shift Register will be transmitted before termination TxD will then go to the high level (Mark)

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output is the complement of CR1 It is normally used to indicate Data Terminal Ready

$\overline{RTS}$ (Request To Send)

The $\overline{RTS}$ output is the complement of CR5. If the Transmit Shift Register is not empty when CR5 is reset, $\overline{RTS}$ will not go high until one TxC after the last serial bit is transmitted.

Functional Description

The internal organization of the EPCI consists of six major blocks, (see Fig 1) These are the Transmitter, Receiver, Clock Control, Operation Control, Modem Control and SYN/DLE Control These blocks internally communicate over common data and control buses The data bus is also linked to the CPU via a bi-directional three-state interface

Briefly, these blocks perform the following functions:

Transmitter

The Transmitter receives parallel data from the CPU and converts it to a serial bit stream, inserting Start, Stop, and Parity bits, as selected by the user, and outputs a composite serial data stream

Receiver

The Receiver accepts serial data from the sending device, converts it to a parallel format checking for appropriate Start, Stop and Parity bits and Control Characters, as selected by the user, and sends the assembled character to the CPU.

Timing Control

The Timing Control block contains a programmable Baud Rate Generator (BRG) which is able to accept external Transmit ($\overline{TxC}$) or Receive ($\overline{RxC}$) clocks or to divide external clock (BRCLK) for controlling data transfers. The BRCLK input allows the user to program one of 16 commonly used baud rates.

Operating Control

The Operation Control block contains four registers; Mode Registers 1 and 2, (MR1, MR2) the Command Register (CR) and Status Register (SR). These registers are used to store configuration and operation commands from the CPU. They generate the necessary internal control signals for proper device operation, and maintain status information for the CPU.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE character provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Operation

The EPCI's operation is determined by programming the Mode and Command Registers. Baud rate, asynchronous or synchronous communication, and SYN characters are determined before enabling the transmitter or receiver

Asynchronous Receiver Operation

After the Mode Registers are configured the receiver is enabled when the RxEN bit in the Command Register (CR2) is set to a 1 and $\overline{DCD}$ is low. The EPCI then monitors the RxD input waiting for a high to low transition If a transition is detected, the RxD input is again sampled one-half bit time later. If RxD is now high, a search for a valid start bit is begun again If RxD is still low a valid start bit is assumed and the receiver continues to sample the RxD input at one bit time intervals until the correct number of data bits, parity bit and one stop bit have been assembled. The character is then transferred to the Receive Data Holding Register (RxHR); RxRDY in the status Register is set (SR1); the $\overline{RxRDY}$ output goes low. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundry. See Figure 6 and 8

If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins See Figure 9

Pin 25 can be programmed as a Break Detect (BKDET) output by setting both bits 4 and 7 of Mode Register 2 (MR2). When these bits are set and a break is detected, the BKDET output will go high. If RxD returns high for at least one RxD time, BKDET will return low.

Synchronous Receiver Operation

When the EPCI is programmed for synchronous operation the receiver will remain idle until the receiver enable bit (CR2) is set. At this time the EPCI enters the hunt mode Data are shifted into the receive data shift register (RxSR) one bit at a time. The contents of RxSR are then compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). See Figure 6

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register Note the SYN characters used to establish initial synchronization are not transferred to the holding register in any case

By setting MR24 (MR2 bit 4) and MR27 = 1 pin 9 ($\overline{RxC}$/XSYNC) will be programmed as an external jam synchronization input When XSYNC is selected internal SYN1, SYN1-SYN2 and DLE-SYN1 detection is disabled Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse Character assembly will start with the RxD input at this edge. XSYNC must be lowered prior to the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read Refer to XSYNC timing diagram.

Asynchronous Transmitter Operation

When the EPCI is programmed to transmit the transmitter will remain idle until $\overline{CTS}$ is low and the TxEN bit (CR0) is set The EPCI will respond by setting status register (SR) bit 0 and asserting the $\overline{TxRDY}$ output When the CPU writes a character into the transmit data holding register (TxHR), SR0 is reset and $\overline{TxRDY}$ returns high. The character is then transferred to the transmit shift register (TxSR) when it is idle or has completed transmission of the previous character. SR0 is again set, and $\overline{TxRDY}$ goes low See Figure 7.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted Transmission resumes when the CPU loads a new character into the holding register The transmitter can be forced to output a continuous low (BREAK) condition by setting CR3

Synchronous Transmitter Operation

When the EPCI is initially programmed for synchronous transmission it will remain in the idle state (RxD high) until TxEN is set At this point TxD remains high, $\overline{\text{TxRDY}}$ will go low and both will stay in this state until the first character (usually a SYN character) is written into the TxHR This starts transmission, with $\overline{\text{TxRDY}}$ going low each time a character is shifted from the TxHR to the TxSR If $\overline{\text{TxRDY}}$ is not serviced before the previous character is shifted out of the TxSR, the $\overline{\text{TxEMT}}$ output will go low and the EPCI will automatically fill the pending gap with SYN1, SYN1, SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR6 and MR17 Transmission will be continuous until TxEN is reset to 0 See Figure 7

If the send DLE bit (CR3) is set, the DLE character is automatically transmitted prior to the transmission of any character stored in the TxHR Since this is a one time command, CR3 does not have to be reset

EPCI Programming

Before data communications can be started the EPCI must be programmed by writing to its mode and command registers Additionally, if synchronous communication has been selected the appropriate SYN1, SYN2 and DLE registers must be loaded Reference the Register Addressing Table and Initialization Flow Chart for address requirements and programming procedure

The Register Addressing table shows MR1 and MR2 at the same address The EPCI has an internal pointer that initially directs the first read or write to MR1, then on the next access at that same address the pointer directs the operation to MR2 A similar sequence occurs for the SYN and DLE registers, first SYN1 then SYN2 then DLE. If more than the required number of accesses are made the internal pointer resets to the first register The pointer is also reset to MR1 and SYN1 by a RESET input or a read of the Command Register, but unaffected by any other read or write operation.

Register Formats

The register formats are summarized in Figures 2 through 5. MR1 and MR2 define the general operating characteristics The Command Register controls the basic operation defined by MR1 and MR2 The Status Register indicates the EPCI operating status and the condition of external inputs These registers are cleared by a RESET input (SR6 and SR7 excepted).

Mode Register 1 (MR1)

MR11 and MR10 select the communication mode and baud rate multiplier Note. the multiplier in asynchronous mode applies only if the external input option is selected by MR24 and MR25

MR13 and MR12 select Character length. Character length does not include the parity bit, when selected, and does not include the start and stop bits in asynchronous operation

MR14, when set, selects parity A parity bit will be transmitted with each character, and a parity check will be performed on each character received.

MR15 selects either odd or even parity.

In the asynchronous mode MR16 and MR17 select the number of stop bits; 1, 1 5 or 2. If 1X baud rate is programmed 1.5 stop bits defaults to 1 on transmit

In the synchronous mode MR17 controls the number of SYN characters used to establish synchronization, and the number of fill characters to be transmitted when $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are 0

MR16 controls selection of the transparent mode When MR16 is set (transparent selected) DLE-SYN1 is used for character fill and SYN detect (SR 5), but the normal synchronization sequence is used to establish character sync When transmitting in the synchronous transparent mode, a DLE character in the TxHR will cause a second DLE character to be transmitted Note: if the send DLE command (CR3) is active when a DLE character is in the TxHR only one additional DLE will be transmitted

The bits in the mode register affecting character assembly and disassembly (MR12-MR16) can be changed dynamically (during active receive/transmit operation) The character mode register affects both the transmitter and receiver, therefore in synchronous mode, changes should be made only in half duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1) In asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half duplex mode (RxEN = 0)

To effect assembly/disassembly of the next received/transmitted character, MR12-15 must be changed within n bit times of the active going state of $\overline{\text{RxRDY}}$/$\overline{\text{TxRDY}}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active (n = smaller of the new and old character lengths)

Mode Register 2 (MR2)

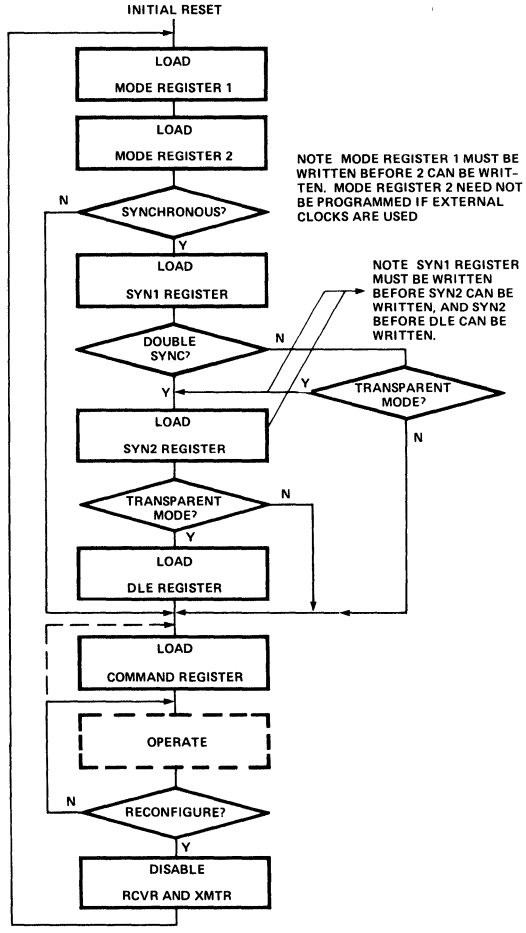
MR20 through MR23 select the internal Baud Rate Generator (BRG) There are sixteen selectable rates for each version as outlined in Table 1.

MR24 through MR27 define the receive and transmit clock source and the function of pins 9 and 25. Reference Figure 3

Table 2 SY2661 Register Addressing

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	Function
1	X	X	X	Three-state Data Bus
0	0	0	0	Read Receive Holding Register (RxHR)
0	0	0	1	Write Transmit Holding Register (TxHR)
0	0	1	0	Read Status Register (SR)
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers (MR1, MR1/MR2)
0	1	0	1	Write Mode Registers (MR1, MR1/MR2)
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

EPCI Initialization Flow Chart



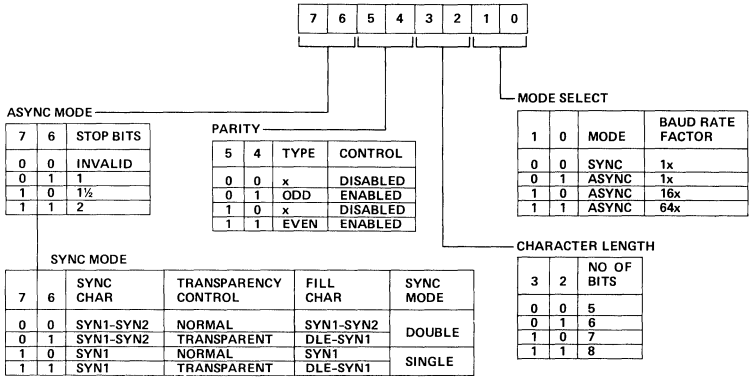


Figure 2. Mode Register 1

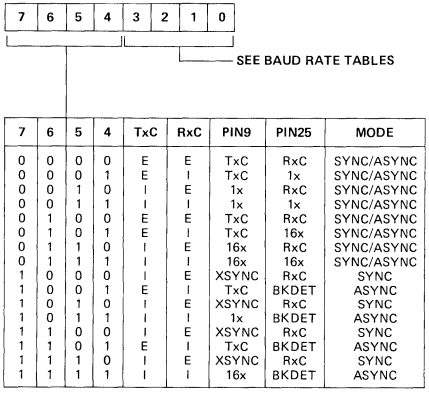


Figure 3. Mode Register 2

Command Register (CR)

CR0 (TxEN) will enable or disable the transmitter When TxEN = 0, TxD, $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are all high, the transmitter is disabled When TxEN goes active, $\overline{\text{TxRDY}}$ will go low requesting the first character to be written to the TxHR, and the TxD output will be enabled to transmit When TxEN goes inactive, the UPCI will complete transmission of any character still in the TxSR TxD will then go to the marking state and $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ will go high. Refer to Transmit timing diagram

CR1 controls the $\overline{\text{DTR}}$ output. The $\overline{\text{DTR}}$ output is a logical complement of CR1

CR2 (RxEN) will enable or disable the receiver. When RxEN = 0, the receiver is in an idle mode with $\overline{\text{RxRDY}}$ high. A 0 to 1 transition of RxEN will initiate a start bit search in asynchronous mode or initiate the hunt mode in synchronous transmission A 1 to 0 transition of RxEN immediately terminates receiver operation

In the asynchronous mode setting CR3 will force the TxD output low (break condition) at the end of the current transmitted character TxD will then remain low until CR3 is cleared; at that time TxD will go high for a minimum 1 bit time before resuming normal transmission.

In the synchronous mode setting CR3 will force the transmission of the DLE character prior to sending the character in the TxHR Because this is a one-time command, bit 3 will automatically reset.

CR5 controls the state of the $\overline{\text{RTS}}$ output. When CR5 = 1, $\overline{\text{RTS}}$ will go low and the transmit logic will be enabled. A 1 to 0 transition of CR5 will cause $\overline{\text{RTS}}$ to go high one TxC time after the last serial bit is transmitted, (if the TxSR was not already empty)

CR7 and CR6 provide four alternate modes of operation in both synchronous and asynchronous operation When both bits are 0 normal operation is selected

In the asynchronous mode, when only CR6 is set automatic echo mode is selected Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues The receiver must be enabled

(CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{\text{TxRDY}}$ output = 1.
4. The $\overline{\text{TxEMT/DSCHG}}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In the synchronous mode, when only CR6 is set automatic SYN/DLE stripping is performed. The state of MR17 and MR16 controls which characters are stripped. Reference Figure 6 for a detailed example of the characters stripped. Note: automatic stripping does not affect setting of the SYN and DLE detect status bits.

Two diagnostic modes are achievable in both synchronous and asynchronous operation; local loop back with CR7 = 1 and CR6 = 0, and remote loopback with both bits = 1.

Local Loop Back

1. The transmitter output is connected to the receiver input
2. $\overline{\text{DTR}}$ is connected to $\overline{\text{DCD}}$ and $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$.
3. Transmit clock is connected to the receive clock.
4. The $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ and $\overline{\text{TxD}}$ outputs are held high.
5. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and RxD inputs are ignored.

Note: CR bits 0, 1 and 5 must be set, CR2 is a don't care.

Remote Loop Back

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. Receive clock is connected to the transmit clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT/DSCHG}}$ outputs are held high
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

SR0 is the transmitter ready (TxRDY) status, it is the logical complement of the $\overline{\text{TxRDY}}$ output. This bit indicates the state of the TxHR when the transmitter is enabled (TxEN = 1). A 0 indicates TxHR is full, a 1 indicates TxHR is empty and requires servicing by the CPU. This bit is cleared by writing to TxHR or by disabling the transmitter (TxEN = 0). Note: SR0 is not set in either the auto echo or remote loop back modes.

SR1 is the receiver ready (RxRDY) status, it is the logical complement of the $\overline{\text{RxRDY}}$ output. This bit indicates the state of the RxHR when the receiver is enabled (RxEN = 1). A 0 indicates the RxHR is empty, a 1 indicates the RxHR is full and requires servicing by the CPU. This bit is cleared by writing to the TxHR or by disabling the receiver. (RxEN = 0).

SR2 indicates a change of state of either $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ or that the TxSR is empty. This bit is the logical complement of the $\overline{\text{TxEMT/DSCHG}}$ output. A read of the status register will clear bit 2 if a state change on $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ has occurred. If a

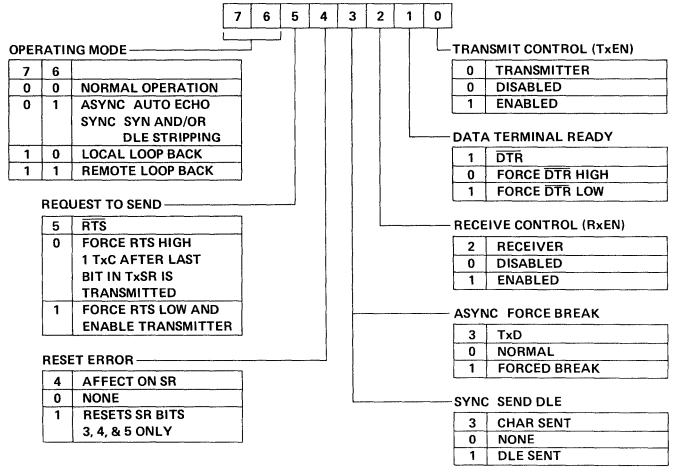


Figure 4. Command Register

second successive read of the status register indicates bit 2 = 0, then $\overline{DCD}$ or $\overline{DSR}$ changed If bit 2 is still set, then the TxSR is empty. Because the transmitter does not start until the first character has been written to the TxHR, $\overline{TxEMT}$ status will not be reflected until transmission of the first character is complete, $\overline{TxEMT}$ status is cleared by writing to the TxHR or disabling the transmitter. Note. $\overline{TxEMT}$ status will be set in synchronous mode even though "fill" characters are being transmitted

SR3 when set reflects a parity error when parity checking is enabled in both the synchronous and asynchronous modes In the synchronous transparent mode, (MR16 = 1) and the parity enable bit (MR14) is 0, SR3 will then indicate DLE detect when set This indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE This bit is cleared when the next character following the above sequence is loaded into the RxHR, when the receiver is disabled or by a reset error command.

SR4 indicates an overrun error when set An overrun condition exists when the CPU does not read the RxHR before the next received character is transferred to it. (The previous character is lost.) SR4 is cleared by the reset error command and when the receiver is disabled

In the asynchronous mode SR5 indicates that the received character was not framed by a stop bit. If the RxHR is all 0's when bit 5 is set, a break condition was present. In synchronous non-transparent mode, it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode In synchronous transparent mode this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode

SR6 and SR7 reflect the condition of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. Their state is the logical complement of their respective inputs

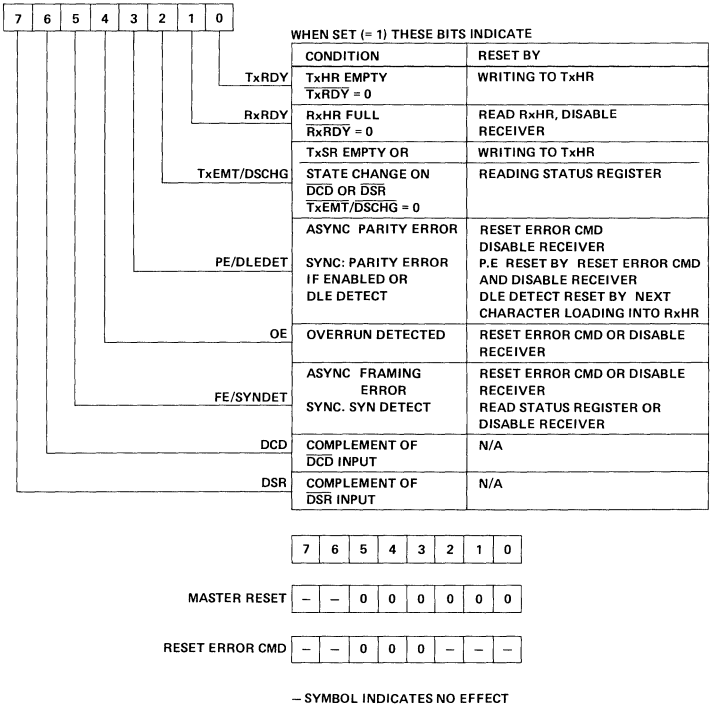


Figure 5. Status Register

Absolute Maximum Ratings*

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	—0.3V to +7.0V
Input/Output Voltage	V_{IN}	—0.3V to +7.0V
Operating Temperature	T_{OP}	0°C to 70°C
Storage Temperature	T_{STG}	—55°C to 150°C

Comment*

All inputs contain protection circuitry to prevent damage to high static charges Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

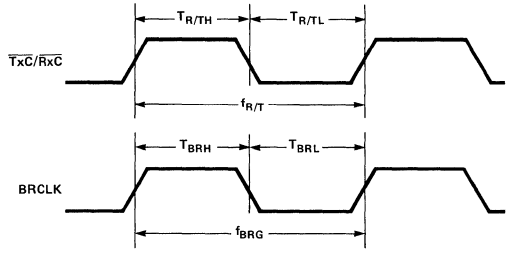
D.C. Characteristics

V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted

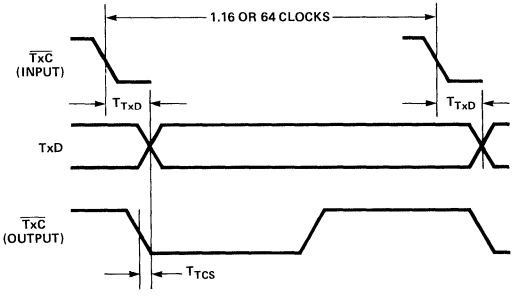
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current V_{IN} = 0 to 5.5V	I_{IN}			10	μA
Input Leakage Current for High Impedance State	I_{TSI}			10	μA
Output High Voltage: I_{LOAD} = —400 μA	V_{OH}	2 4			V
Output Low Voltage: I_{LOAD} = 2.2 mA	V_{OL}			0 4	V
Input Capacitance· f_C = 1 MHz	C_{IN}			20	pF
Output Capacitance	C_{OUT}			20	pF
Power Dissipation (V_{CC} = 5.25V)	P_D			650	mW

Receiver/Transmitter Signal Timing

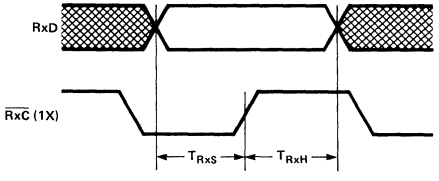
Clocks



Transmit Timing



Receive Timing

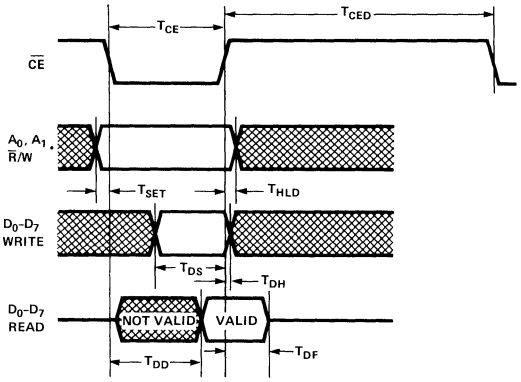


Symbol	Characteristic	MIN	TYP	MAX	UNIT
T_R/TH	TxC or RxC HIGH	500			ns
T_R/TL	TxC or RxC LOW	500		1.0	ns
f R/T	TxC or RxC freq.	DC		1.0	MHz
T_{BRH}	BRCLK HIGH	70			ns
T_{BRL}	BRCLK LOW	70			ns
f BRG	BRCLK freq. [1]		4,9152		MHz
T_{RxS}	RxD SETUP	300			ns
T_{RxH}	RxD HOLD	350			ns
T_{TxD}	TxD DELAY FROM TxC C_L = 150 pF			650	ns
T_{TCS}	SKEW TxD vs TxC C_L = 150 pF		0		ns

Note
1 F_{BRG} = 4 9152 applicable for -1 and -2, F_{BRG} = 5 0688 for -3

Read/Write Timing Characteristics

V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted



Symbol	Characteristic	MIN	MAX	UNIT
T_{CE}	$\overline{CE}$ Pulse Width	250		ns
T_{CED}	$\overline{CE}$ to $\overline{CE}$ Delay	600		ns
T_{SET}	Address and R/$\overline{W}$ Set Up	10		ns
T_{HLD}	Address and R/$\overline{W}$ Hold	10		ns
T_{DS}	Write Data Set Up	150		ns
T_{DH}	Write Data Hold	0		ns
T_{DD}	Read Data Delay C_L = 150 pF		200	ns
T_{DF}	READ DATA HOLD C_L = 150 pF	10	100	ns

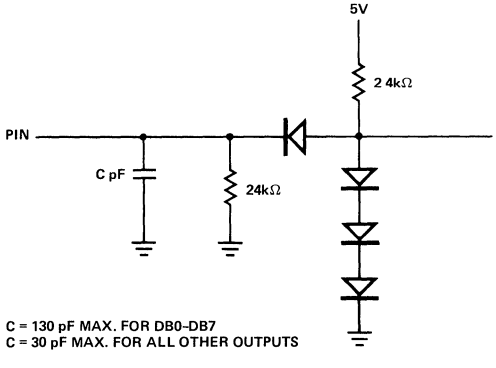
Table 3 Effect of MR17 and MR16 on Character Fill and Character Stripping (Synchronous Mode)

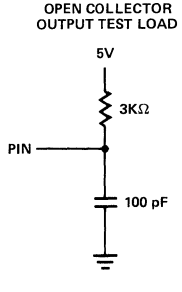
MR17	MR16	Mode	Synchronizing Sequence	Character Fill	Character(s) Stripped CR7 = 0, CR6 = 1
0	0	Double SYN Normal	SYN1-SYN2	SYN1-SYN2	SYN1 SYN1-SYN2[1]
1	0	Single SYN Normal	SYN1	SYN1	SYN1[1]
0	1	Double SYN Transparent	SYN1-SYN2	DLE-SYN1	DLE-SYN1[1] SYN1-SYN2[1] (Only Initial Synchronizing Sequence) DLE (also Sets SR3 if Parity Disabled and it is not Following a DLE or SYN1) In a DLE-DLE Sequence Only the First DLE is Stripped
1	1	Single SYN Transparent	SYN1	DLE-SYN1	DLE-SYN1[1] SYN1 (only Initial Synchronizing Sequence) DLE and DLE-DLE same as Double SYN Transparent

Note

1 Symbol indicates SYN DET status set upon detection of initial synchronizing characters and after SYNC has been achieved by detection of a DLE-SYN1 pair

Test Load





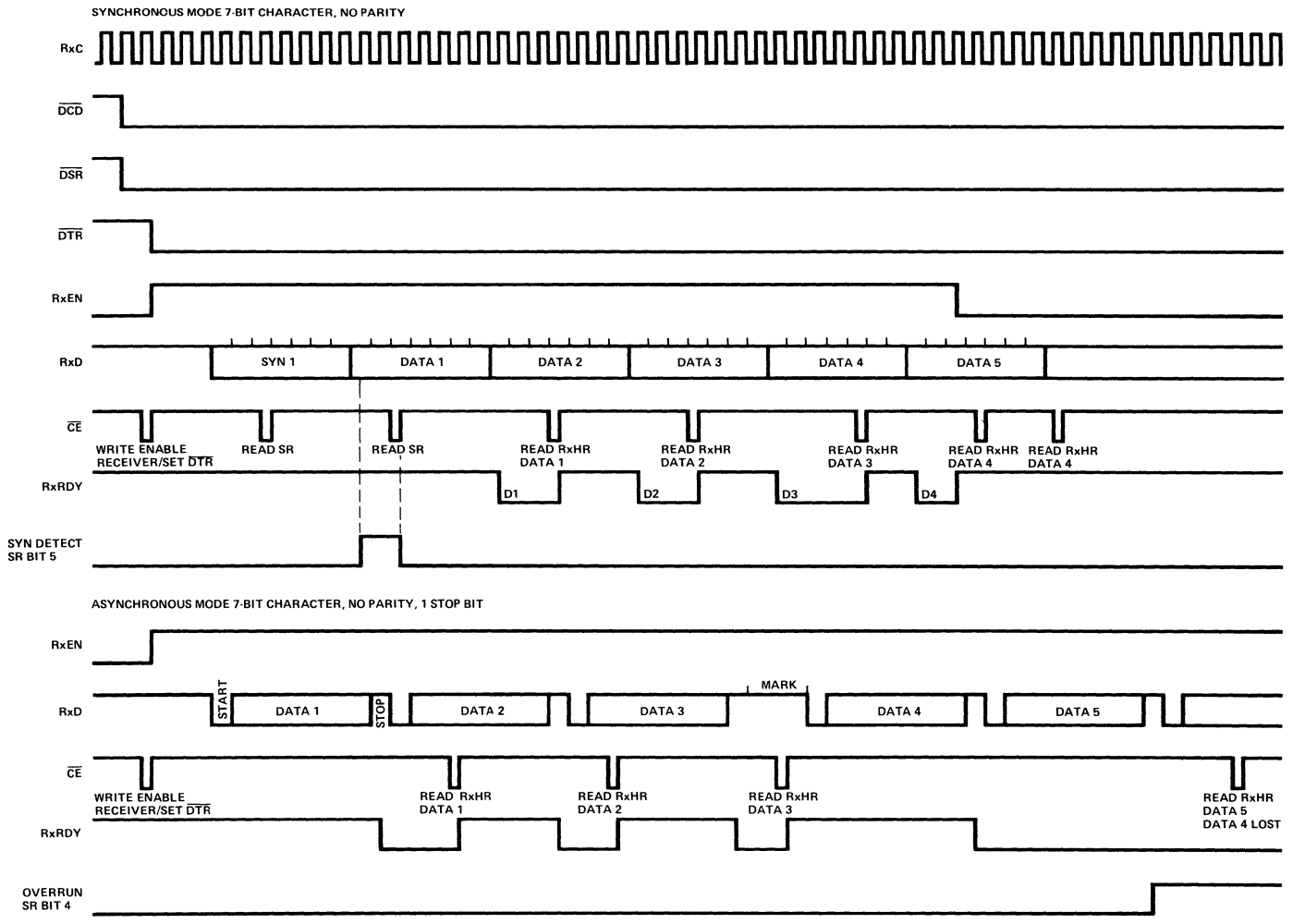


Figure 6. Receiver Operation Timing Diagram

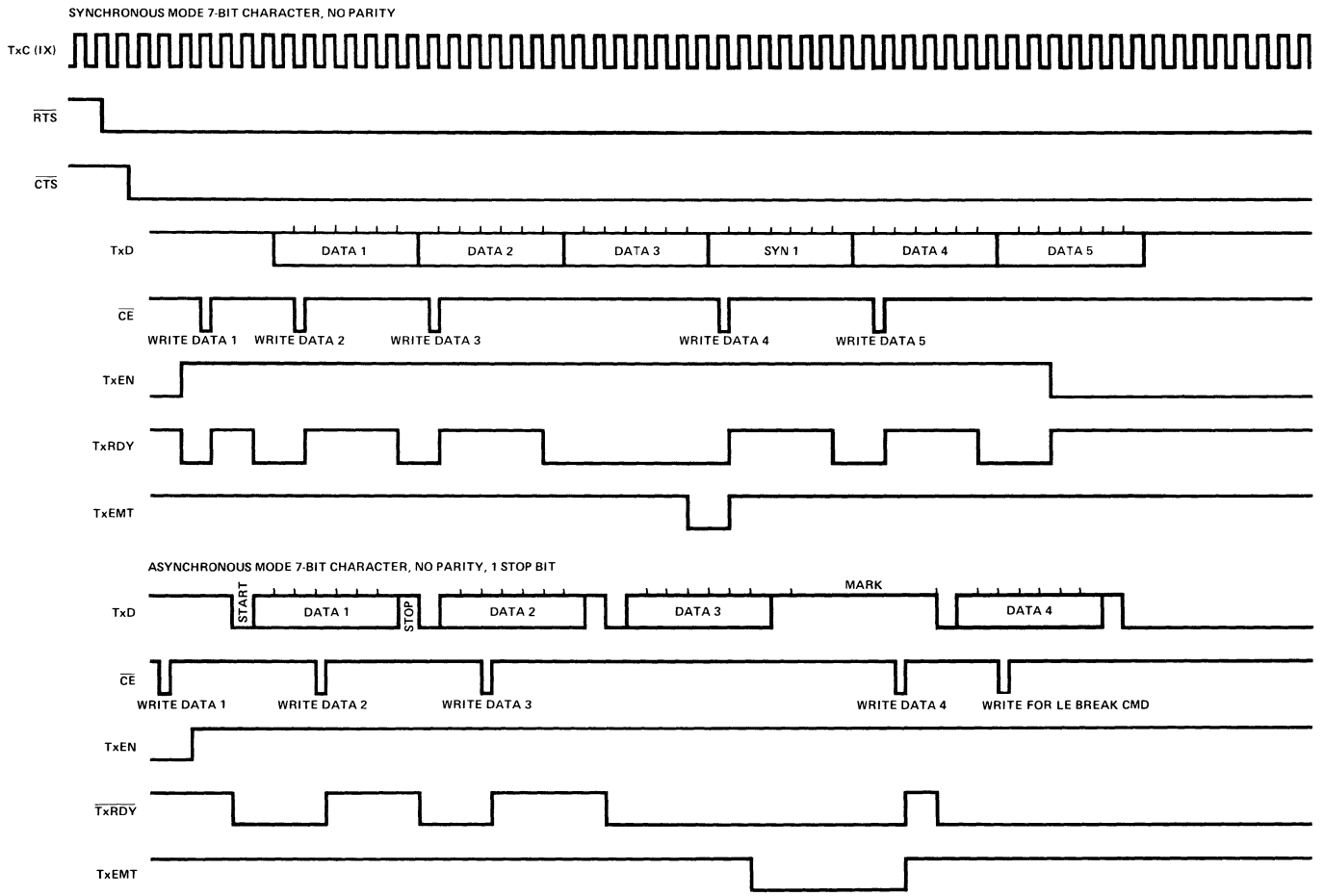


Figure 7. Transmitter Operation Timing Diagram

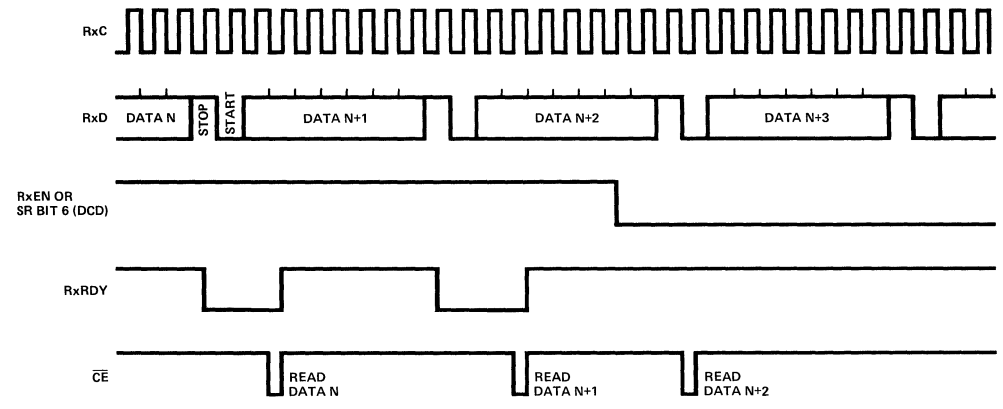


Figure 8. Asynchronous Receiver Operation with Loss of $\overline{DCD}$ or Disabling RxEN

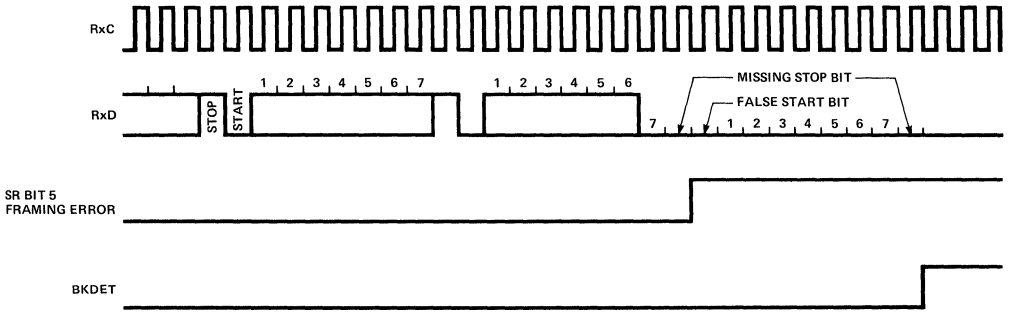


Figure 9. Framing Error and Break Detection Timing

Package Availability 40 Pin Molded DIP

Ordering Information

Part No.	Package
SYP2661-X	Molded DIP

X = 1, 2 or 3
(See Table 1)

Synertek.

SY6500

8-Bit Microprocessor Family

Features

- Single 5 V ±5% Power Supply
- N Channel, Silicon Gate, Depletion Load Technology
- Eight Bit Parallel Processing
- 56 Instructions
- Decimal and Binary Arithmetic
- Thirteen Addressing Modes
- True Indexing Capability
- Programmable Stack Pointer
- Variable Length Stack
- Interrupt Capability
- Non-maskable Interrupt
- Use with Any Type or Speed Memory
- Bi-directional Data Bus
- Instruction Decoding and Control
- Addressable Memory Range of up to 65K Bytes
- "Ready" Input
- Direct Memory Access Capability
- Bus Compatible with MC6800
- Choice of External or On-board Clocks
- 1 MHz, 2 MHz Operation
- On-chip Clock Options
  - — External Single Clock Input
  - — Crystal Time Base Input
- 40 and 28 Pin Package Versions
- Pipeline Architecture

Description

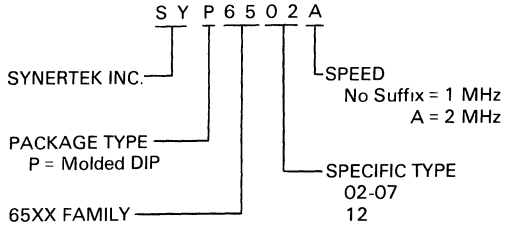
The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the SY6500 family are software compatible within the group and are bus compatible with the MC6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers for four microprocessors driven by external clocks The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The external clock versions are geared for the multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz, 3 MHz and 4 MHz maximum operating frequencies.

Members of the Family

Part Number	Clocks	Pins	IRQ	NMI	RYD	Addressing
SY6502	On-Chip	40	√	√	√	64K
SY6507	"	28			√	8K
SY6512	External	40	√	√	√	64K

Ordering Information

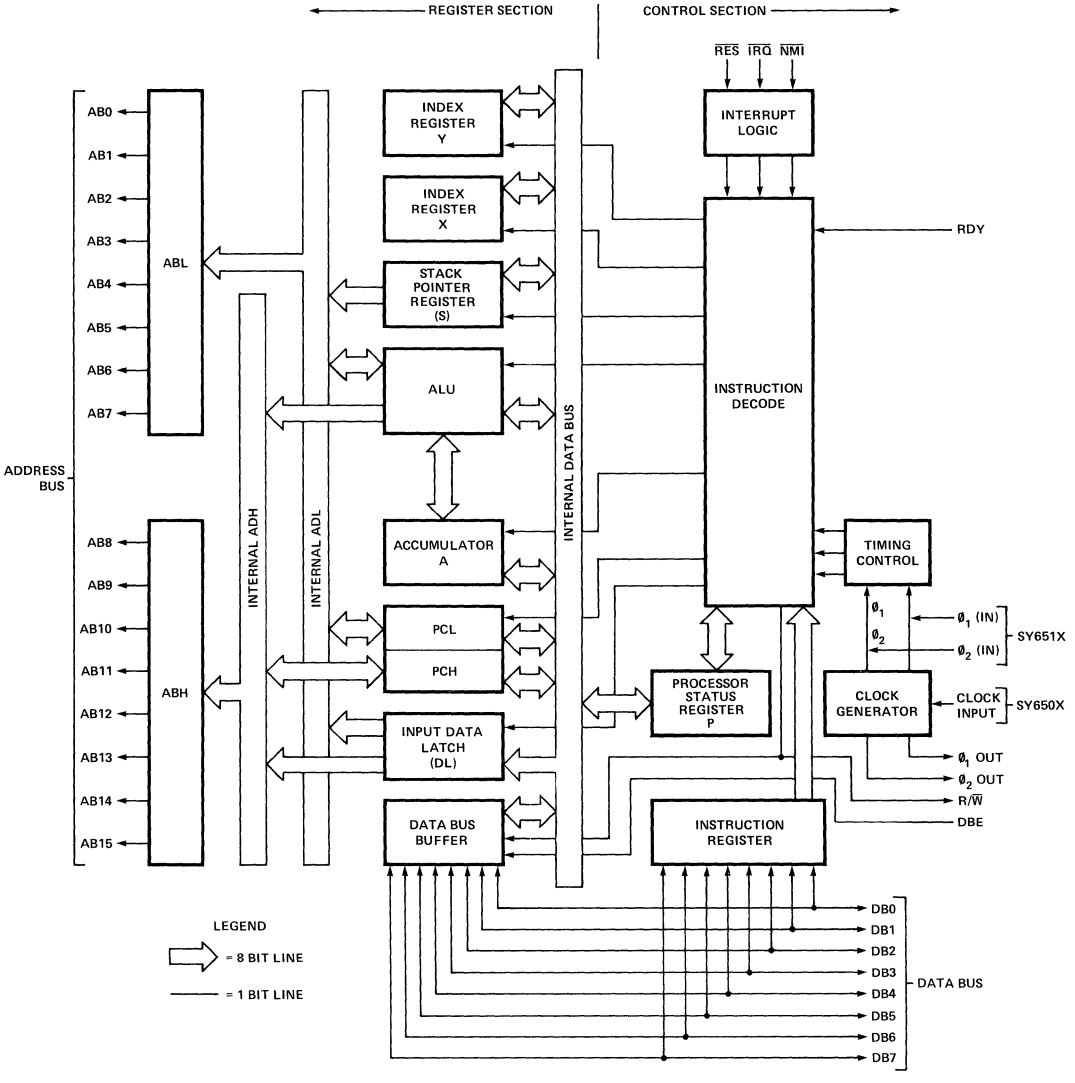


MICRO-PROCESSORS

Comments on the Data Sheet

The data sheet is constructed to review the basic "Common Characteristics" — those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

SY6500 Internal Architecture



NOTE
1 CLOCK GENERATOR IS NOT INCLUDED ON SY651X
2 ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE SY6500 PRODUCTS

Absolute Maximum Ratings*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

Comment*

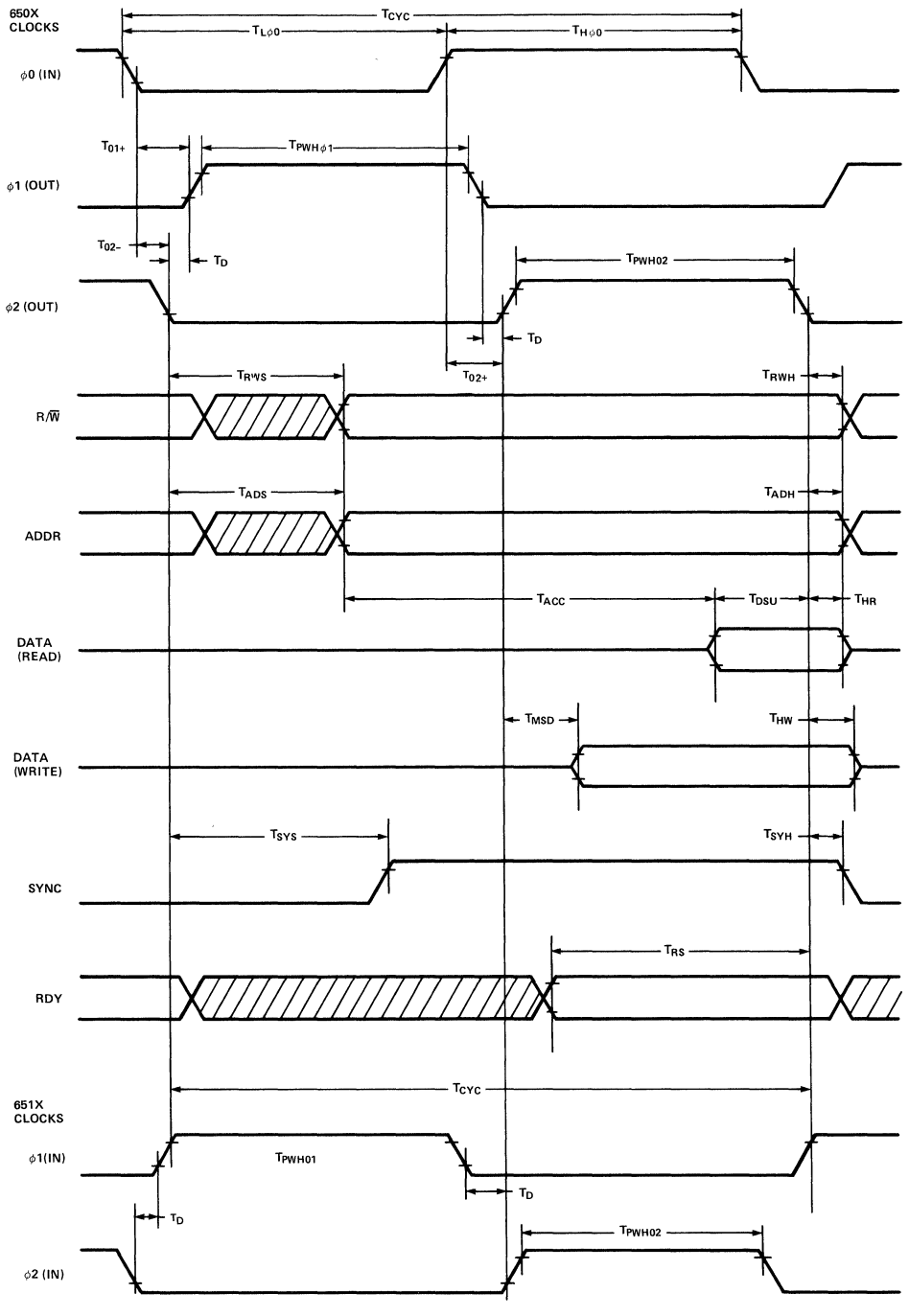
This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

D.C. Characteristics (V_{CC} = 5.0V ±5%, T_A = 0-70°C)

(ϕ_1, ϕ_2 applies to SY651X, $\phi_{o\,(in)}$ applies to SY650X)

Symbol	Characteristic		Min.	Max.	Unit
V_{IH}	Input High Voltage				
	Logic and ϕ_o (in) for all 650X devices	1,2,3 MHz	+2.0	V_{CC}	V
		4 MHz	+3.3	V_{CC}	V
	ϕ_1 and ϕ_2 only for all 651X devices. Logic as 650X	All Speeds	V_{CC} −0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage				
	Logic, $\phi_{o\,(in)}$	(650X)	−0.3	+0.8	
	ϕ_1, ϕ_2	(651X)	−0.3	+0.2	V
I_{IL}	Input Loading (V_{in} = 0 V, V_{CC} = 5.25 V) RDY, S.O.		−10	−300	μA
I_{in}	Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 0)				
	Logic (Excl. RDY, S.O.)		—	2.5	μA
	ϕ_1, ϕ_2	(651X)	—	100	μA
	$\phi_{o\,(in)}$	(650X)	—	10.0	μA
I_{TSI}	Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V) DB0-DB7		—	±10	μA
V_{OH}	Output High Voltage (I_{LOAD} = −100μAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	1, 2 MHz	2.4	—	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1 6mAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	1, 2 MHz	—	0.4	V
P_D	Power Dissipation (V_{CC} = 5.25V)	1 MHz and 2 MHz	—	700	mW
C	Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)				
C_{in}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE		—	10	pF
	DB0-DB7		—	15	
C_{out}	A0-A15, R/$\overline{W}$, SYNC		—	12	
$C_{\phi_{o(in)}}$	$\phi_{o\,(in)}$	(650X)	—	15	
C_{ϕ_1}	ϕ_1	(651X)	—	50	
C_{ϕ_2}	ϕ_2	(651X)	—	80	

MICRO-PROCESSORS


650X CLOCKS
T_{CYC}
$T_{L\phi0}$
$T_{H\phi0}$
$\phi0$ (IN)
T_{01+}
$T_{PWH\phi1}$
$\phi1$ (OUT)
T_{02-}
T_D
T_{PWH02}
$\phi2$ (OUT)
T_D
T_{02+}
T_{RWS}
T_{RWH}
R/$\overline{W}$
T_{ADS}
T_{ADH}
ADDR
T_{ACC}
T_{DSU}
T_{HR}
DATA (READ)
T_{MSD}
T_{HW}
DATA (WRITE)
T_{SYS}
T_{SYH}
SYNC
T_{RS}
RDY
651X CLOCKS
T_{CYC}
$\phi1$(IN)
T_{PWH01}
T_D
T_D
T_{PWH02}
$\phi2$ (IN)

Dynamic Operating Characteristics

(V_{CC} = 5.0 ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz Min.	1 MHz Max.	2 MHz Min.	2 MHz Max.	Units
651X						
Cycle Time	T_{CYC}	1 00	40	0 50	40	μs
$Ø_1$ Pulse Width	$T_{PWHØ_1}$	430	—	215	—	ns
$Ø_2$ Pulse Width	$T_{PWHØ_2}$	470	—	235	—	ns
Delay Between $Ø_1$ and $Ø_2$	T_D	0	—	0	—	ns
$Ø_1$ and $Ø_2$ Rise and Fall Times[1]	T_R, T_F	0	25	0	20	ns
650X						
Cycle Time	T_{CYC}	1 00	40	0 50	40	μs
$Ø_{o(IN)}$ Low Time[2]	$T_{LØ_o}$	480	—	240	—	ns
$Ø_{o(IN)}$ High Time[2]	$T_{HØ_o}$	460	—	240	—	ns
$Ø_o$ Neg to $Ø_1$ Pos Delay[5]	T_{01+}	10	70	10	70	ns
$Ø_o$ Neg to $Ø_2$ Neg Delay[5]	T_{02-}	5	65	5	65	ns
$Ø_o$ Pos to $Ø_1$ Neg Delay[5]	T_{01-}	5	65	5	65	ns
$Ø_o$ Pos to $Ø_2$ Pos Delay[5]	T_{02+}	15	75	15	75	ns
$Ø_{o(IN)}$ Rise and Fall Time[1]	T_{RO}, T_{FO}	0	30	0	20	ns
$Ø_{1(OUT)}$ Pulse Width	$T_{PWHØ_1}$	$T_{LØ_o}$-20	$T_{LØ_o}$	$T_{LØ_o}$-20	$T_{LØ_o}$	ns
$Ø_{2(OUT)}$ Pulse Width	$T_{PWHØ_2}$	$T_{LØ_o}$-40	$T_{LØ_o}$-10	$T_{LØ_o}$-40	$T_{LØ_o}$-10	ns
Delay Between $Ø_1$ and $Ø_2$	T_D	5	—	5	—	ns
$Ø_1$ and $Ø_2$ Rise and Fall Times[1,3]	T_R, T_F	—	25	—	25	ns
650X, 651X						
R/$\overline{W}$ Setup Time	T_{RWS}	—	225	—	140	ns
R/$\overline{W}$ Hold Time	T_{RWH}	30	—	30	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	ns
Address Hold Time	T_{ADH}	30	—	30	—	ns
Read Access Time	T_{ACC}	—	650	—	310	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	ns
Write Data Hold Time	T_{HW}	60	150	60	150	ns
Sync Setup Time	T_{SYS}	—	350	—	175	ns
Sync Hold Time	T_{SYH}	30	—	30	—	ns
RDY Setup Time[4]	T_{RS}	200	—	200	—	ns

Notes:
1. Measured between 10% and 90% points.
2. Measured at 50% points
3. Load = 1 TTL load +30 pF.
4. RDY must never switch states within T_{RS} to end of ϕ_2.
5. Load = 100 pF
6. The 2 MHz devices are identified by an "A" suffix.

Timing Diagram Note:
Because the clock generation for the SY650X and SY651X is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters are referred to these lines and scale variations in the diagrams are of no consequence.

Pin Functions

Clocks (ϕ_1, ϕ_2)

The SY651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The SY650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (A_0-A_{15})

(See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB_0-DB_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the SY6512, only.

Ready (RDY)

This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one, (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read opeation. Ready transitions must not be permitted during ϕ_2 time.

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At the time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no futher interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)

This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for the data transfer out of the processor.

Programming Characteristics

INSTRUCTION SET — ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag

SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Pointer
TYA Transfer Index Y to Accumulator

ADDRESSING MODES

Accumulator Addressing

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory

Zero page Addressing

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing — (X, Y indexing)

This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y " The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing — (X, Y indexing)

This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

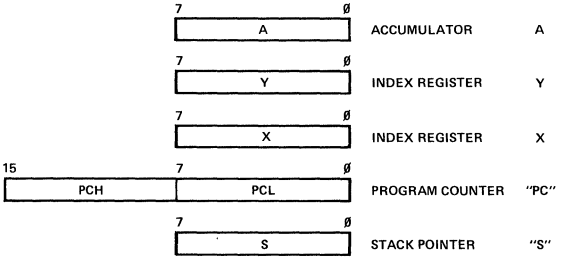
In indirect indexed addressing (referred to as [Indirect], Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being hte high order eight bits of the effective address.

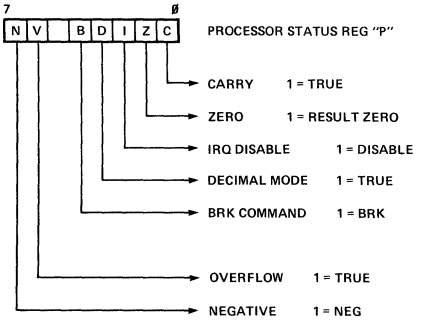
Absolute Indirect

The second byte of the instruction contains the lwo order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

Programming Characteristics

PROGRAMMING MODEL





INSTRUCTION SET – OP CODES, EXECUTION TIME, MEMORY REQUIREMENTS

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND X)			(IND) Y			Z PAGE X			ABS X			ABS Y			RELATIVE			INDIRECT			Z PAGE Y			CONDITION CODES						
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	–	–	✓
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	–	–	–	–
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	–	–	–
BCC	BRANCH ON C=0 (2)																															90	2	2												
BCS	BRANCH ON C=1 (2)																															B0	2	2							–	–	–	–	–	–
BEQ	BRANCH ON Z=1 (2)																															F0	2	2							–	–	–	–	–	–
BIT	A ∧ M				2C	4	3	24	3	2																															M_7	✓	–	–	–	M_6
BMI	BRANCH ON N=1 (2)																															30	2	2							–	–	–	–	–	–
BNE	BRANCH ON Z=0 (2)																															D0	2	2							–	–	–	–	–	–
BPL	BRANCH ON N=0 (2)																															10	2	2							–	–	–	–	–	–
BRK	(See Fig 1)													00	7	1																									–	–	–	✓	–	–
BVC	BRANCH ON V=0 (2)																															50	2	2							–	–	–	–	–	–
BVS	BRANCH ON V=1 (2)																															70	2	2							–	–	–	–	–	–
CLC	0 → C													18	2	1																									–	–	–	0	–	–
CLD	0 → D													D8	2	1																									–	–	–	–	0	–
CLI	0 → I													58	2	1																									–	–	–	0	–	–
CLV	0 → V													B8	2	1																									–	–	–	–	–	0
CMP	A-M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	–	–	–
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																															✓	✓	✓	–	–	–
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																															✓	✓	✓	–	–	–
DEC	M-1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	–	–	–	–
DEX	X-1 → X													CA	2	1																									✓	✓	–	–	–	–
DEY	Y-1 → Y													88	2	1																									✓	✓	–	–	–	–
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	–	–	–	–
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	–	–	–	–
INX	X + 1 → X													E8	2	1																									✓	✓	–	–	–	–
INY	Y + 1 → Y													C8	2	1																									✓	✓	–	–	–	–
JMP	JUMP TO NEW LOC				4C	3	3																													6C	5	3				–	–	–	–	–	–
JSR	(See Fig 2) JUMP SUB				20	6	3																																		–	–	–	–	–	–
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	–	–	–	–

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND X)			(IND) Y			Z PAGE X			ABS X			ABS Y			RELATIVE			INDIRECT			Z PAGE Y			CONDITION CODES						
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3										✓	✓	–	–	–	–
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													✓	✓	–	–	–	–
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓	–	–	–
NOP	NO OPERATION													EA	2	1																									–	–	–	–	–	–
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	–	–	–	–
PHA	A → Ms S-1 → S													48	3	1																									–	–	–	–	–	–
PHP	P → Ms S-1 → S													08	3	1																									–	–	–	–	–	–
PLA	S + 1 → S Ms → A													68	4	1																									✓	✓	–	–	–	–
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)					
ROL	[7 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	–	–	–
ROR	[C] → [7 0] →				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓	–	–	–
RTI	(See Fig 1) RTRN INT													40	6	1																									(RESTORED)					
RTS	(See Fig 2) RTRN SUB													60	6	1																									–	–	–	–	–	–
SBC	A-M-$\bar{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	(3)	–	–	✓
SEC	1 → C													38	2	1																									–	–	1	–	–	–
SED	1 → D													F8	2	1																									–	–	–	–	1	–
SEI	1 → I													78	2	1																									–	–	–	1	–	–
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										–	–	–	–	–	–
STX	X → M				8E	4	3	86	3	2																															96	4	2	–	–	–	–	–	–
STY	Y → M				8C	4	3	84	3	2													94	4	2																	–	–	–	–	–	–
TAX	A → X													AA	2	1																									✓	✓	–	–	–	–
TAY	A → Y													A8	2	1																									✓	✓	–	–	–	–
TSX	S → X													BA	2	1																									✓	✓	–	–	–	–
TXA	X → A													8A	2	1																									✓	✓	–	–	–	–
TXS	X → S													9A	2	1																									–	–	–	–	–	–
TYA	Y → A													98	2	1																									✓	✓	–	–	–	–

(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BELOW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

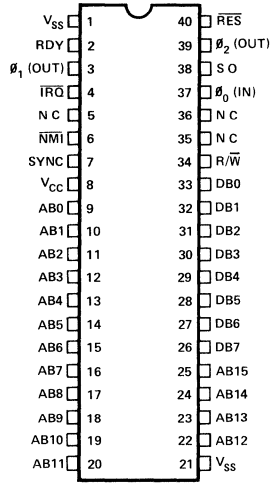
X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
-- SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
✓ MODIFIED

– NOT MODIFIED
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
N NO CYCLES
NO BYTES

MICRO-PROCESSORS

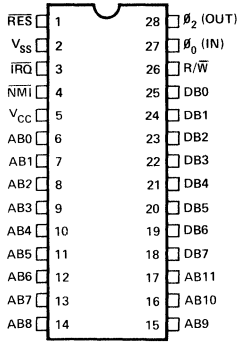
SY6502 — 40 Pin Package



Features

- 65K Addressable Bytes of Memory
- IRQ Interrupt
- NMI Interrupt
- On-the-chip Clock
  - √ TTL Level Single Phase Input
  - √ Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used for single cycle execution)
- Two Phase Output Clock for Timing of Support Chips

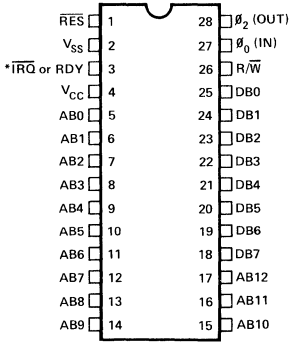
SY6503 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bi-Directional Data Bus

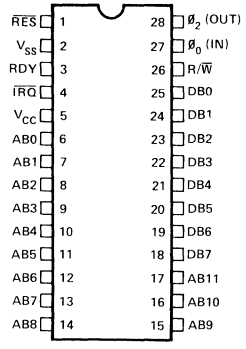
SY6504 & SY6507 — 28 Pin Package



Features

- IRQ Interrupt (6504 only)
- RDY Signal (6507 only)
- 8K Addressable Bytes of Memory (AB00-AB12)
- On-the-chip Clock
- 8 Bit Bi-Directional Data Bus

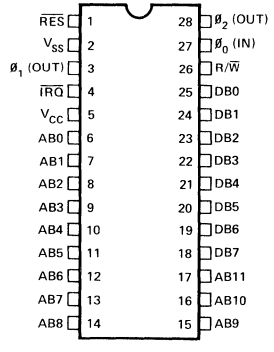
SY6505 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus

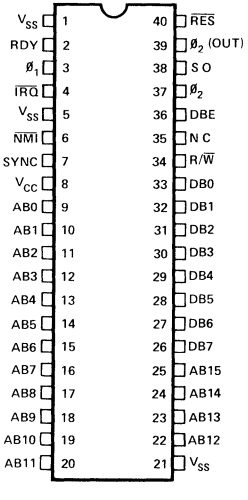
SY6506 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phases off
- 8 Bit Bi-Directional Data Bus

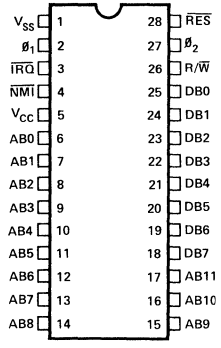
SY6512 — 40 Pin Package



Features

- 65K Addressable Bytes of Memory
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus
- SYNC Signal
- Two phase input
- Data Bus Enable

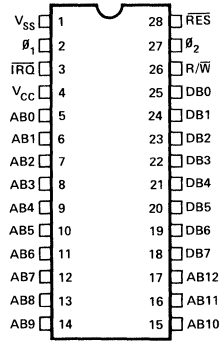
SY6513 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bi-Directional Data Bus

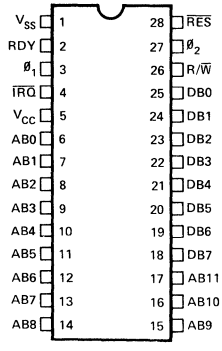
SY6514 — 28 Pin Package



Features

- 8K Addressable Bytes of Memory (AB00-AB12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bi-Directional Data Bus

SY6515 — 28 Pin Package

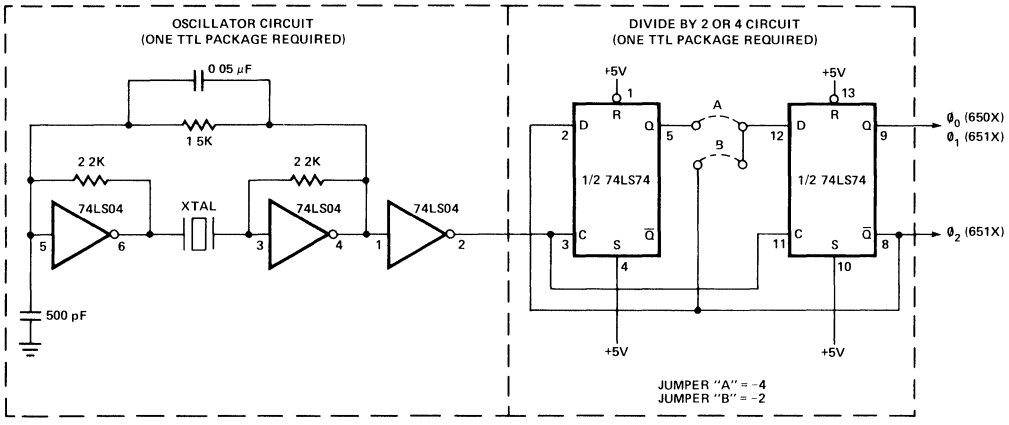


Features

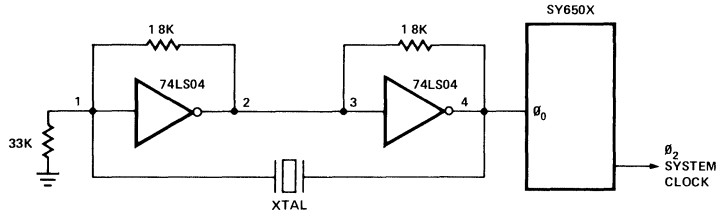
- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bi-Directional Data Bus

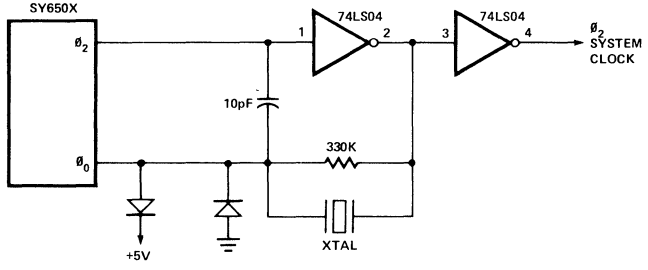
Clock Generation Circuits*

*For further details refer to Synertek SY6500 Applications Information Note AN2. Crystals used are CTS Knight MP Series or equivalents. (Series Mode)



CRYSTAL FREQUENCY	OUTPUT FREQUENCY	
	-2	-4
3 579545 MHz	1 7897 MHz	0 894886 MHz
4 194304 MHz	2 097152 MHz	1 048576 MHz





MICRO-PROCESSORS

Synertek.

SY6522/SY6522A

Versatile Interface Adapter (VIA)

.Features

- Two 8-Bit Bidirectional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS Compatible Peripheral Port A lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz and 2 MHz Operation

Description

The SY6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

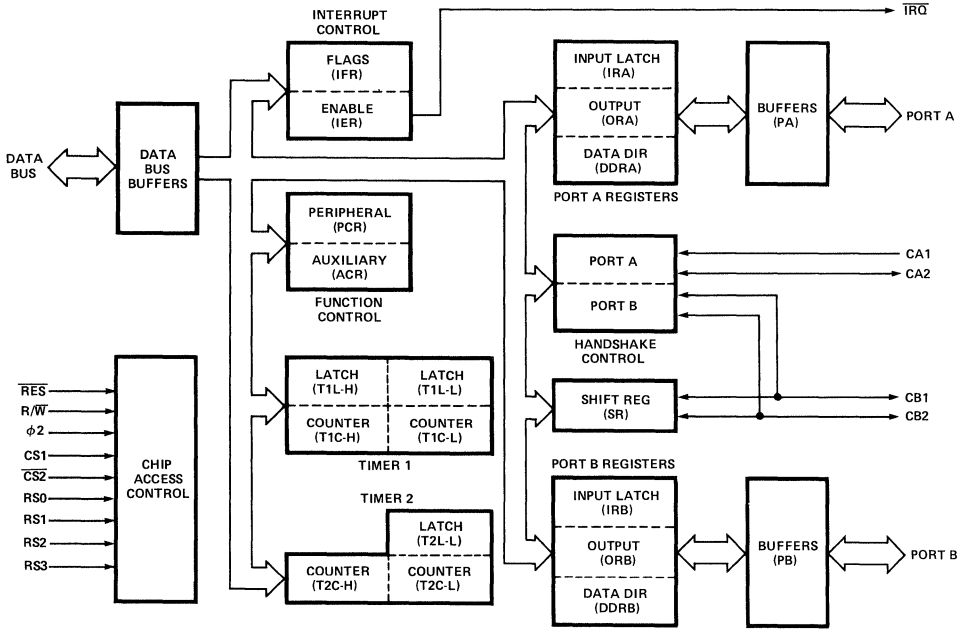


Figure 1. SY6522 Block Diagram

Absolute Maximum Ratings*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Comment*

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

Electrical Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0–70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.4	V
I_{IN}	Input Leakage Current — V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\Phi 2$	—	±2.5	μA
I_{TSI}	Off-state Input Current — V_{IN} = .4 to 2.4V V_{CC} = Max, D0 to D7	—	±10	μA
I_{IH}	Input High Current — V_{IH} = 2.4V PA0–PA7, CA2, PB0–PB7, CB1, CB2	-100	—	μA
I_{IL}	Input Low Current — V_{IL} = 0.4 Vdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	—	-1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = -100 μAdc PA0–PA7, CA2, PB0–PB7, CB1, CB2	2.4	—	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	—	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0–PB7)	 -100 -1.0	 — —	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	—	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	—	10	μA
C_{IN}	Input Capacitance — T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7) (CB1, CB2) ($\Phi 2$ Input)	 — — —	 7.0 10 20	 pF pF pF
C_{OUT}	Output Capacitance — T_A = 25°C, f = 1 MHz	—	10	pF
P_D	Power Dissipation (V_{CC} = 5.25V)	—	700	mW

Test Load

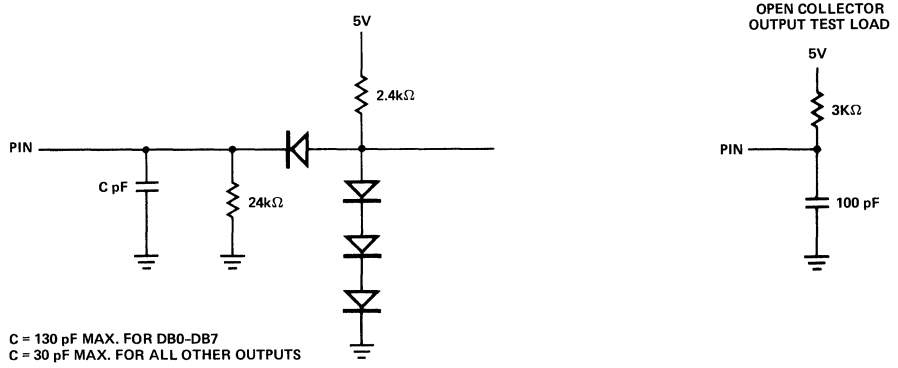


Figure 2. Test Load (for all Dynamic Parameters)

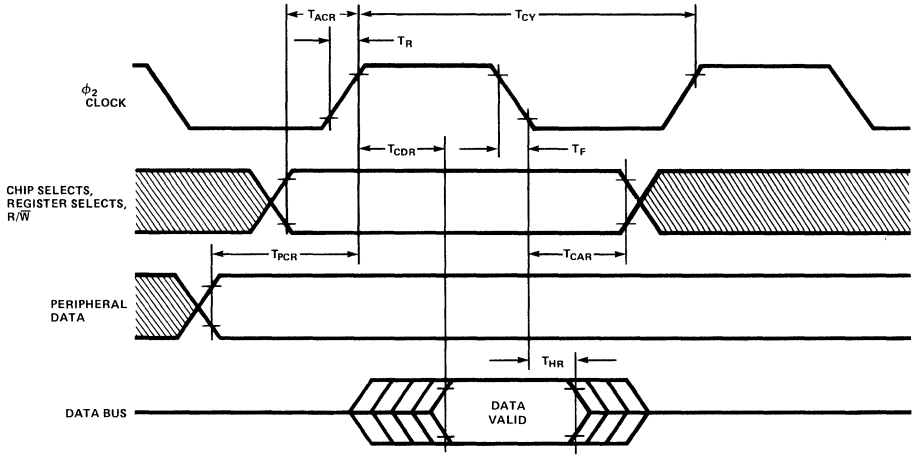


Figure 3. Read Timing Characteristics

Read Timing Characteristics (Figure 3)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

NOTE: tr, tf = 10 to 30ns.

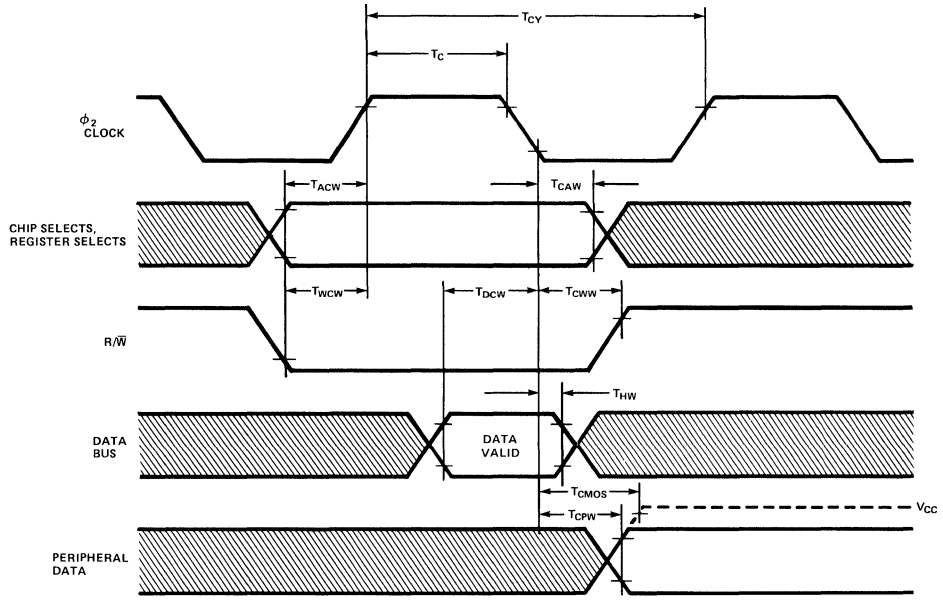


Figure 4. Write Timing Characteristics

Write Timing Characteristics (Figure 4)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	φ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

NOTE: tr, tf = 10 to 30ns.

Peripheral Interface Characteristics

Symbol	Characteristic	Min.	Max.	Typ.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	—	1.0		μs	—
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0		μs	5a, 5b
T_{RS}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0		μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0		μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0		μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5		μs	5c, 5d
T_{RS3}	Delay Time, Clock Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0		μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0		μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—		ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—		ns	5e
T_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300		ns	5f
T_{SR2}	Shift-In Setup Time — Time from CB2 Data in to ϕ_2 Rising Edge	300	—		ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}		ns	5g
T_{IPW}	Pulse Width — PB6 Input Pulse	$2 \times T_{CY}$	—			5i
T_{ICW}	Pulse Width — CB1 Input Clock	$2 \times T_{CY}$	—			5h
T_{IPS}	Pulse Spacing — PB6 Input Pulse	$2 \times T_{CY}$	—			5i
T_{ICS}	Pulse Spacing — CB1 Input Pulse	$2 \times T_{CY}$	—			5h
T_{AL}	CA1, CB1 Set Up Prior to Transition to Arm Latch	$T_C + 50$	—		ns	5e
T_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—		ns	5e
T_{PWI}	Set Up Required on CA1, CB1, CA2 or CB2 Prior to Triggering Edge	$T_C + 50$	—		ns	5j
	Shift Register Clock – Delay from ϕ_2					
T_{DPR}	to CB1 Rising Edge			200	ns	5k
T_{DPL}	to CB1 Falling Edge			125	ns	5k

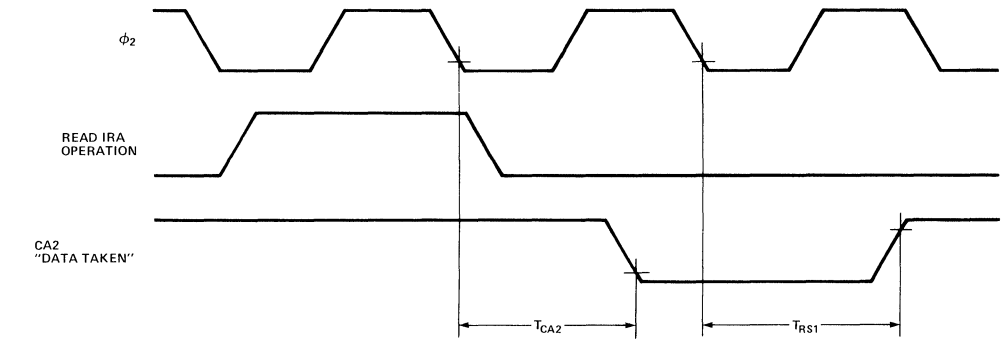


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

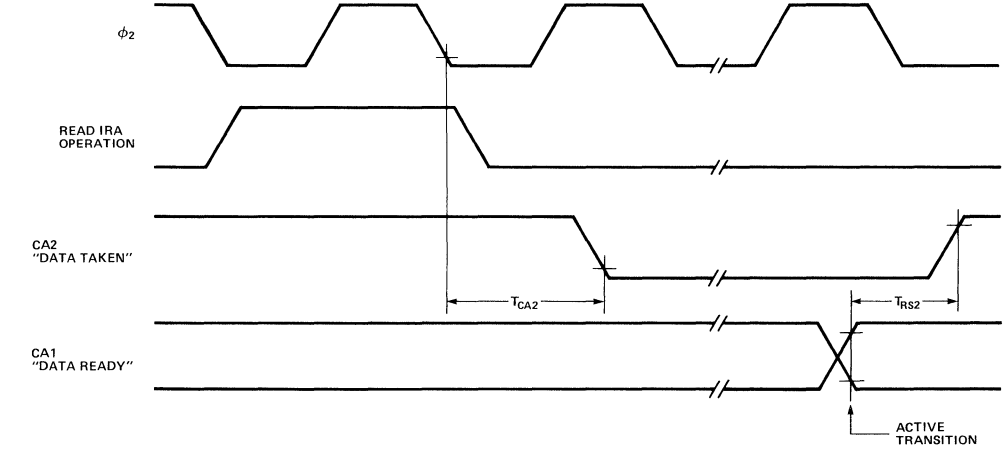


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

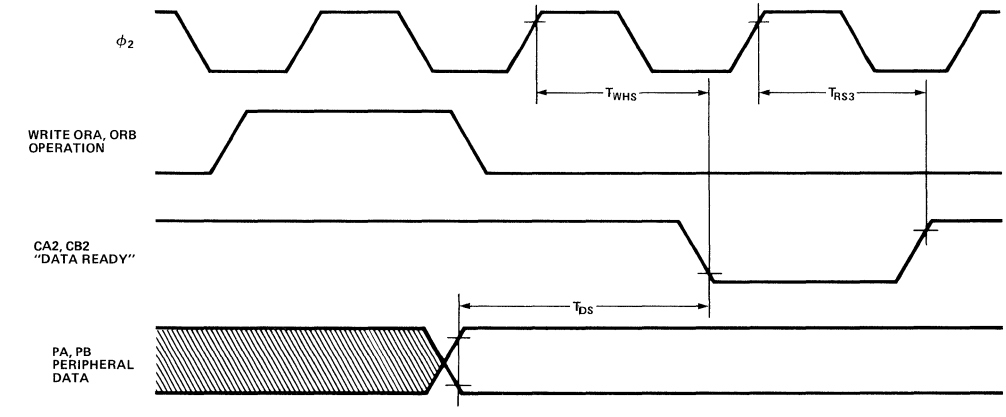


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

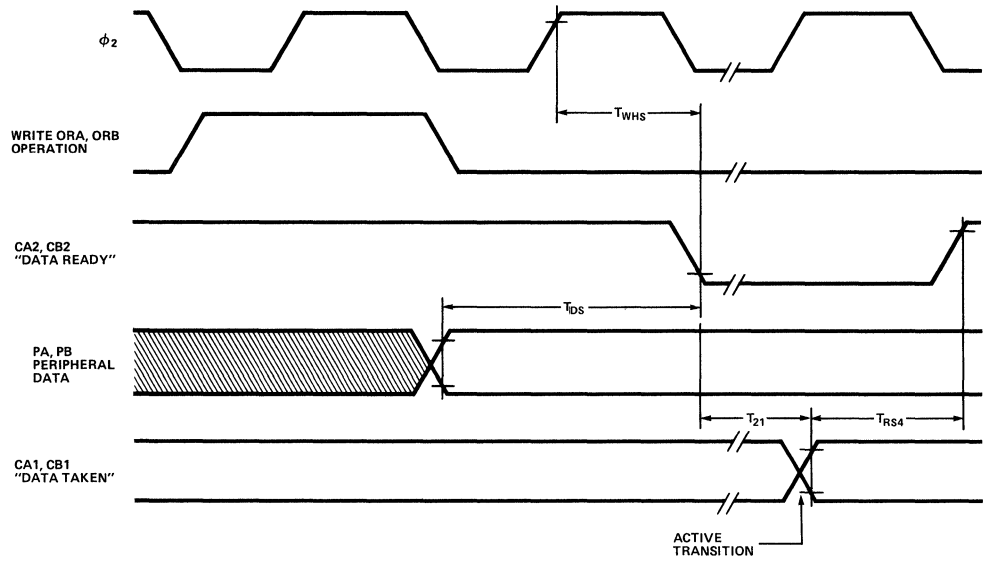


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

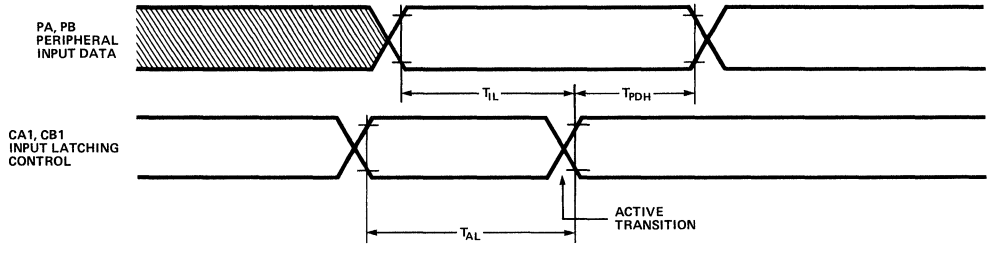


Figure 5e. Peripheral Data Input Latching Timing

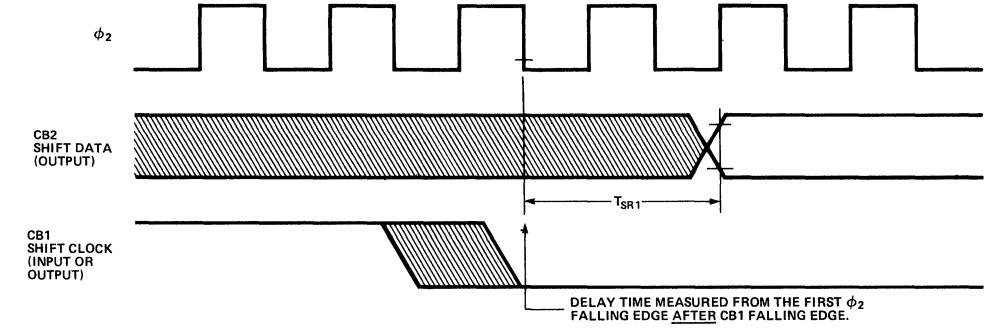


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

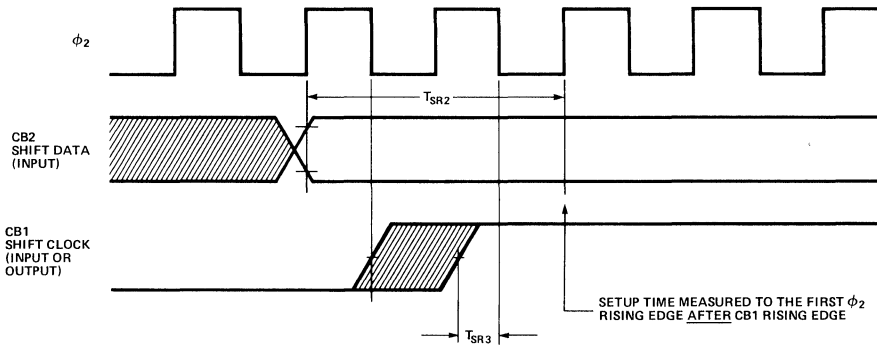


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

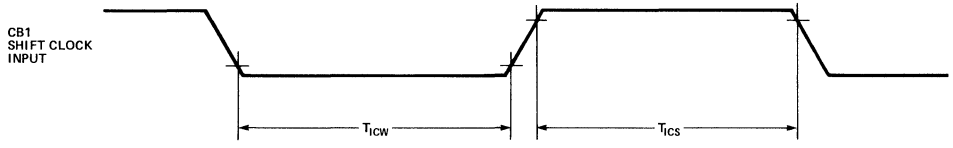


Figure 5h. External Shift Clock Timing

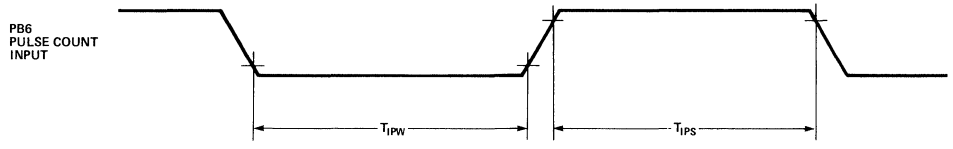


Figure 5i. Pulse Count Input Timing

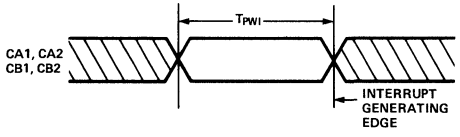


Figure 5j. Setup Time to Triggering Edge

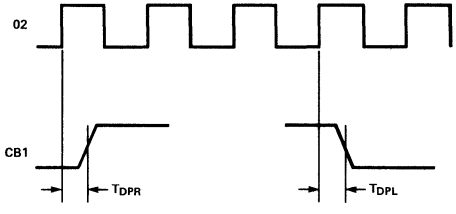


Figure 5k. Shift-in/out with Internal Clock Delay CD2 to CB1 Edge

Pin Descriptions

RES (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

ϕ2 (Input Clock)

The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system processor and the SY6522.

R/$\overline{W}$ (Read/Write)

The direction of the data transfers between the SY6522 and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected SY6522 register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the SY6522 (read operation).

DB0–DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the SY6522 and the system processor. During read cycles, the contents of the selected SY6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the SY6522 is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected SY6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

RS0–RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the SY6522, as shown in Figure 6.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

Figure 6. SY6522 Internal Register Summary

IRQ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high-impedance input only; while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

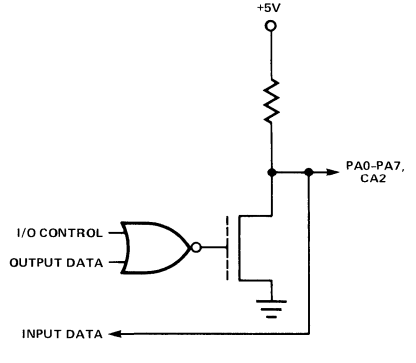


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits.

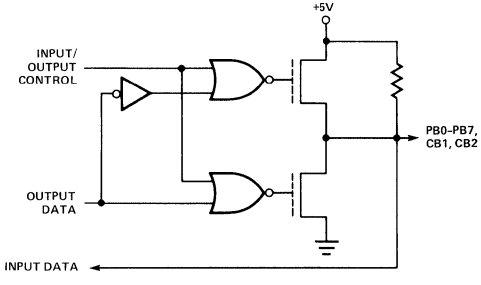


Figure 8. Peripheral B Port Output Circuit

FUNCTIONAL DESCRIPTION

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

When programmed as an output each peripheral pin is also controlled by a corresponding bit in the Output Register (ORA, ORB). A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are pro-

grammed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled and the selected active transition on CA1 having occurred, IRA will contain the data present on the PA lines at the time of the transition. Once IRA is read, however, it will appear transparent, reflecting the current state of the PA lines until the next "latching" transition.

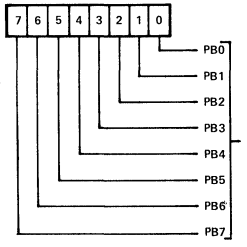
The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10, and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

Handshake Control of Data Transfers

The SY6522 allows positive control of data transfers between the system processor and peripheral devices

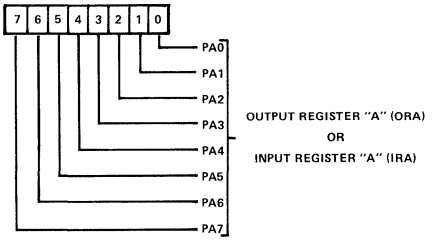
REG 0 – ORB/IRB



Pin Data Direction Selection	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no affect
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed	MPU reads input level on PB pin
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition

Figure 9. Output Register B (ORB), Input Register B (IRB)

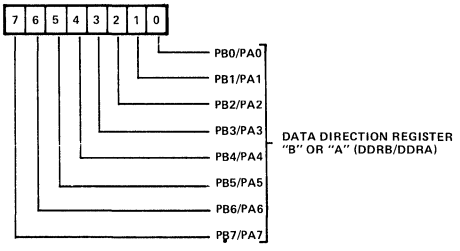
REG 1 – ORA/IRA



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed	MPU reads level on PA pin
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)



"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH IMPEDANCE)

"1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT

Figure 11. Data Direction Registers (DDRB, DDRA)

through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

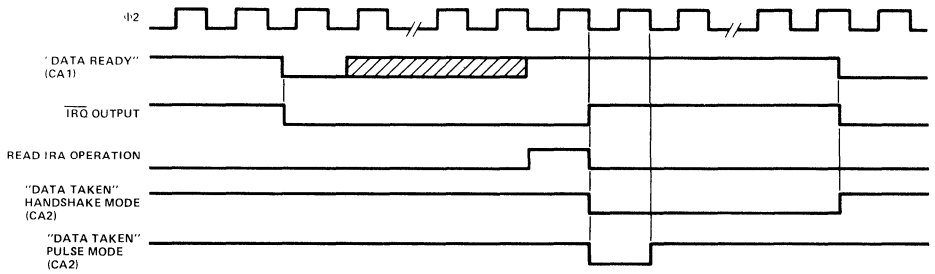


Figure 12. Read Handshake Timing (Port A, Only)

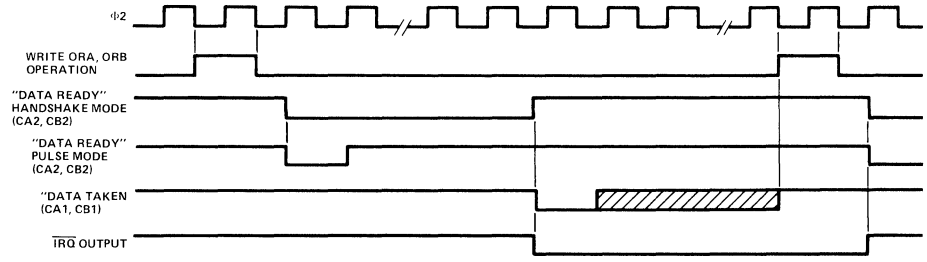


Figure 13. Write Handshake Timing

In the SY6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the SY6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the SY6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or (when programmed to) will automatically transfer the contents of the latches into the counter and begin to decrement again. In addition, the timer may be programmed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

REG 12 – PERIPHERAL CONTROL REGISTER

7	6	5	CB2 CONTROL
0	0	0	INPUT-NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT-NEG EDGE *
0	1	0	INPUT-POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT-POS EDGE *
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

CB1 INTERRUPT CONTROL
0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

3	2	1	CA2 CONTROL
0	0	0	INPUT-NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT-NEG EDGE *
0	1	0	INPUT-POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT-POS EDGE *
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

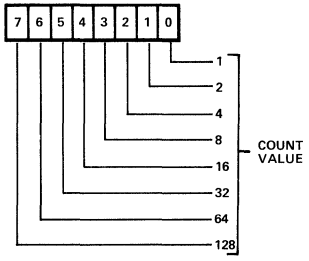
CA1 INTERRUPT CONTROL
0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

*SEE NOTE ACCOMPANYING FIGURE 25

Figure 14. CA1, CA2, CB1, CB2 Control

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

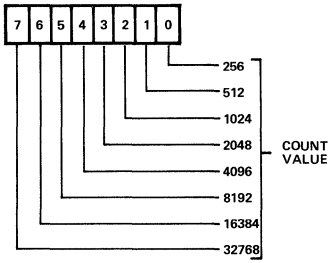
REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER)

REG 5 – TIMER 1 HIGH-ORDER COUNTER

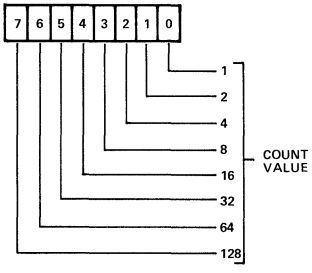


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER, AND INITIATES COUNTDOWN. T1 INTERRUPT FLAG ALSO IS RESET

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

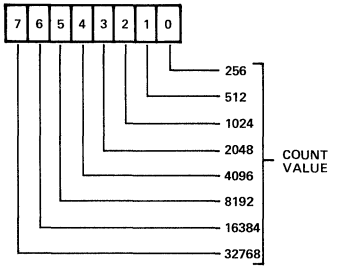
REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG

REG 7 – TIMER 1 HIGH-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

REG 11 – AUXILIARY CONTROL REGISTER

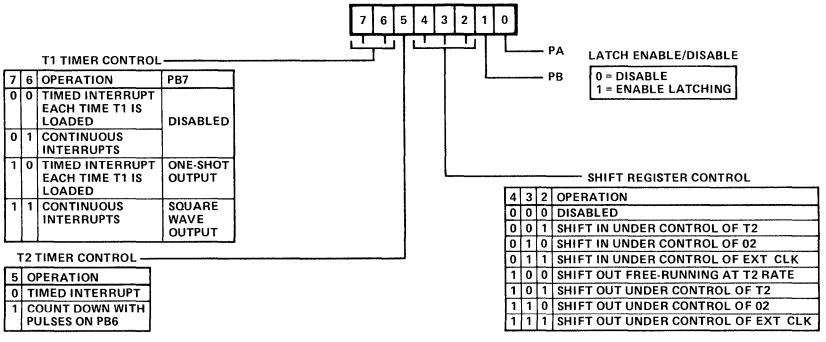


Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

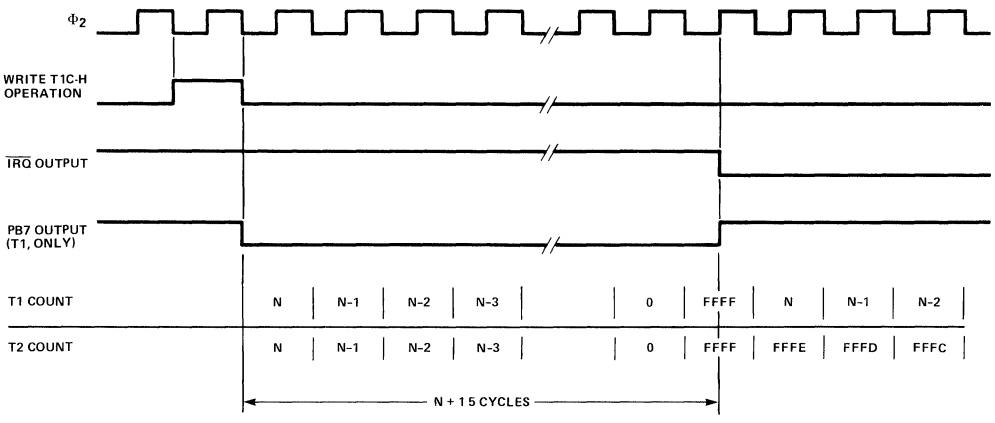


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each Timer load operation. In addition, Timer 1 can be programmed to produce a single negative pulse on PB7.

To generate a single interrupt ACR bits 6 and 7 must be 0 then either TIL-L or TIC-L must be written with the low-order count value. (A write to TIC-L is effectively a Write to TIL-L). Next the high-order count value is written to TIC-H, (the value is simultaneously written into TIL-H), and TIL-L is transferred to TIC-L. Countdown begins on the ϕ_2 following the write TIC-H and decrements at the ϕ_2 rate. T1 interrupt occurs when the counters reach 0. Generation of a negative pulse on PB7 is done in the same manner except ACR bit 7 must be a one. PB7 will go low after a Write TIC-H and go high again when the counters reach 0.

The T1 interrupt flag is reset by either writing TIC-H (starting a new count) or by reading TIC-L.

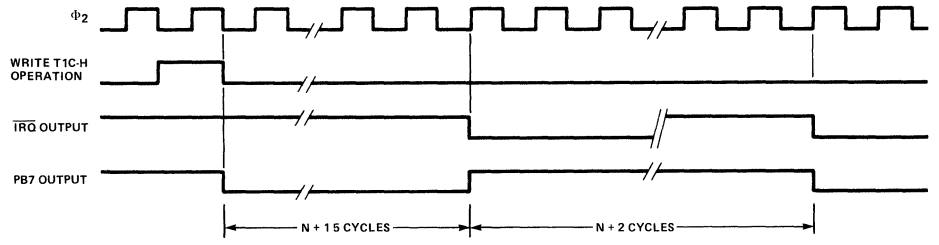
Timing for the one-shot mode is illustrated in Figure 18.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. The interrupt flag can be cleared by reading TIC-L, by writing directly into the flag as described later, or if a new count value is desired by a write to TIC-H.

All interval timers in the SY6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 19. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at Φ2 rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, (reading 0) the counters "roll-over" to all 1's ($FFFF_{16}$) and continue decrementing, allowing the user to read them and determine how long T2 interrupt has been set. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

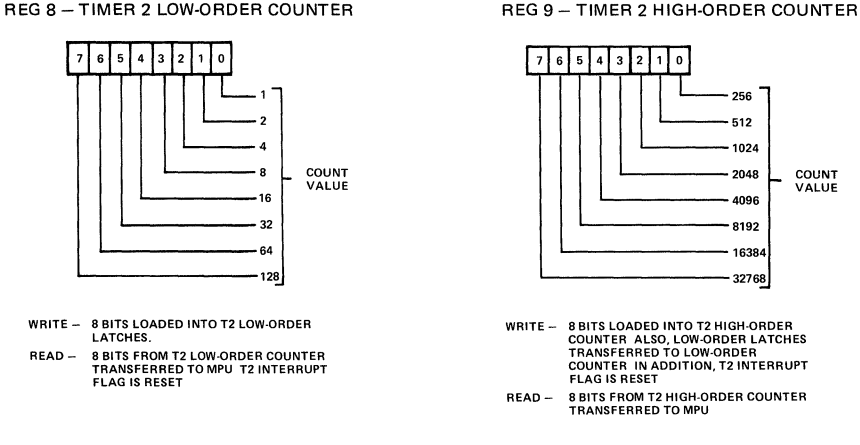


Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of $\Phi 2$.

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the SY6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the SY6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

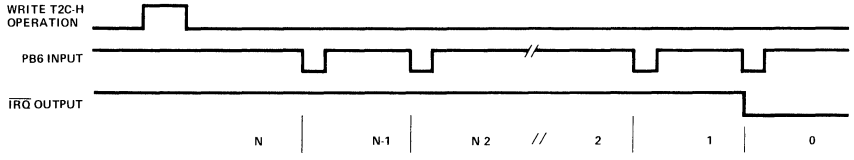
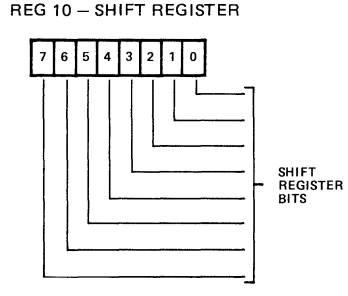
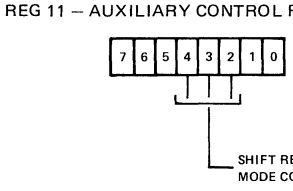


Figure 21. Timer 2 Pulse Counting Mode



NOTES
1 WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0
2 WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Φ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Φ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

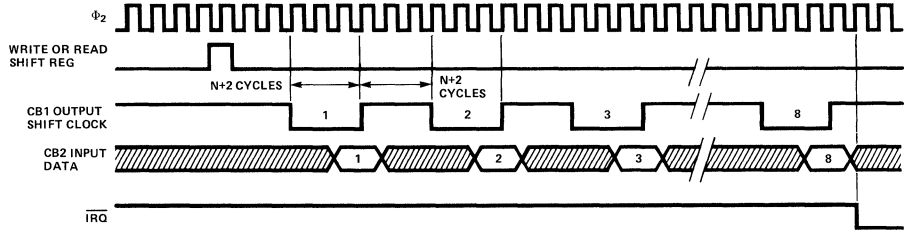
SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

Shift in Under Control of T2 (001)

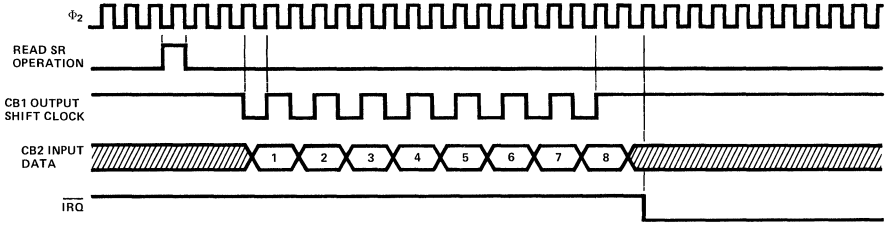
In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the ϕ_2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.



Shift in Under Control of ϕ_2 (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ_2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.



Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

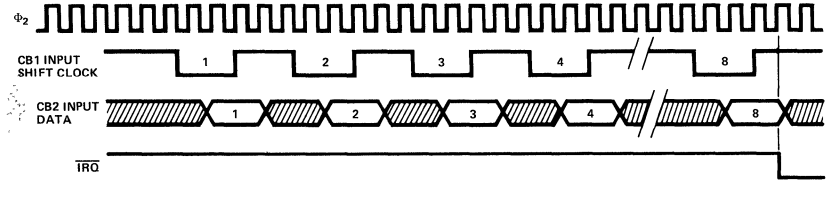
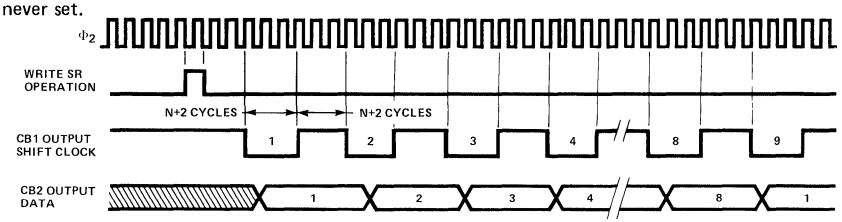


Figure 23. Shift Register Input Modes

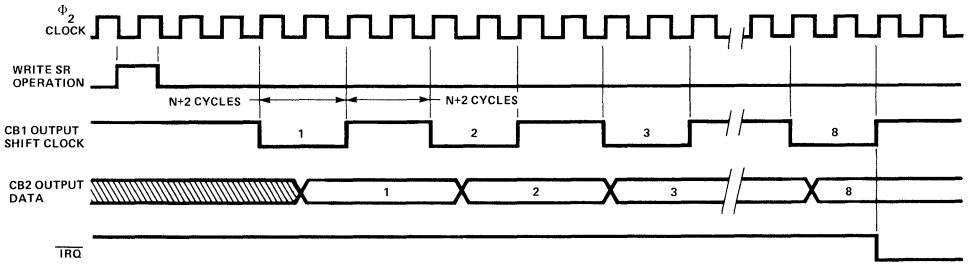
Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CR2 repetitively. In this mode the shift register counter is disabled, and $\overline{IRQ}$ is never set.



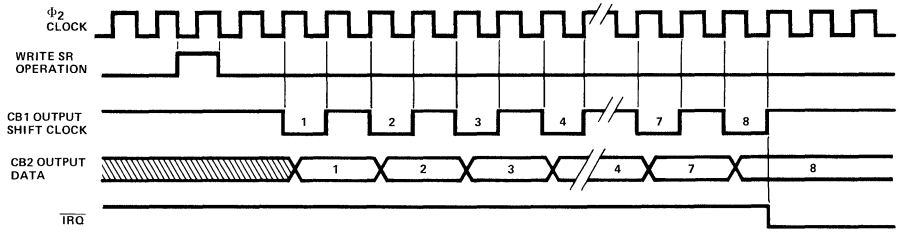
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of ϕ_2 (110)

In mode 110, the shift rate is controlled by the ϕ_2 system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

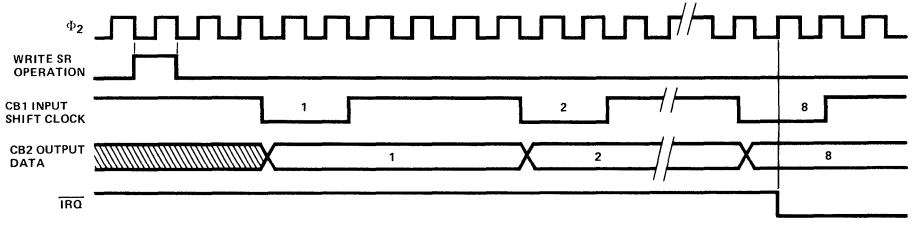


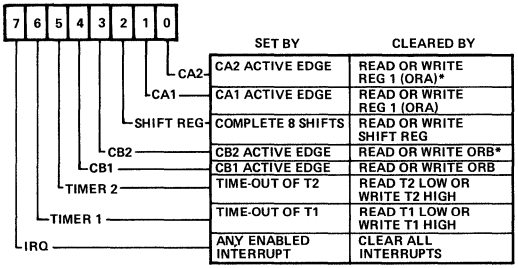
Figure 24. Shift Register Output Modes

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

REG 13 – INTERRUPT FLAG REGISTER



* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY

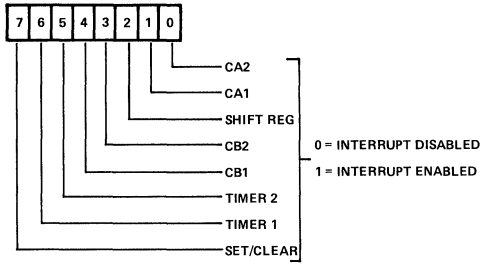
Figure 25. Interrupt Flag Register (IFR)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a logic 1.

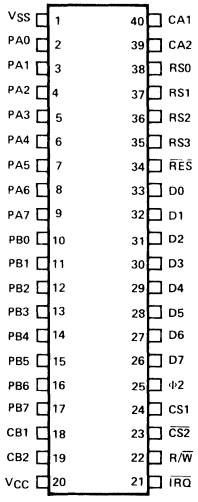
REG 14 – INTERRUPT ENABLE REGISTER



NOTES:
1 IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3 IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE

Figure 26. Interrupt Enable Register (IER)

Pin Configuration



Package Availability 40 Pin Molded DIP

Ordering Information

Order Numbrer	Package Type	Frequency Option
SYP6522	Molded DIP	1 MHz
SYP6522A	Molded DIP	2 MHz
SYPJ6522	Molded J Lead	1 MHz
SYPJ6522A	Molded J Lead	2 MHz

Synertek.

SY6532

RAM, I/O, Timer Array

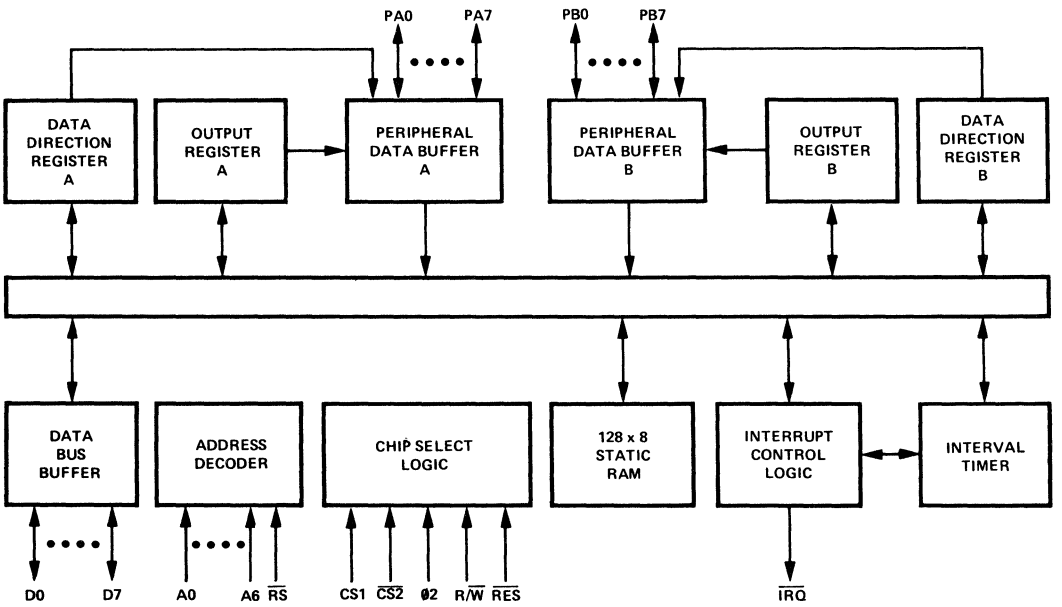
Features

- 8-Bit Bi-directional Data Bus for Direct Communication with the Microprocessor
- Programmable Edge-sensitive Interrupt
- 128 x 8 Static RAM
- Two 8-bit Bi-directional Data Ports for Interface to Peripherals
- Two Programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS Compatible Peripheral Lines
- Peripheral Pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins

Description

The SY6532 is designed to operate in conjunction with the SY6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8-bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices. a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

Block Diagram



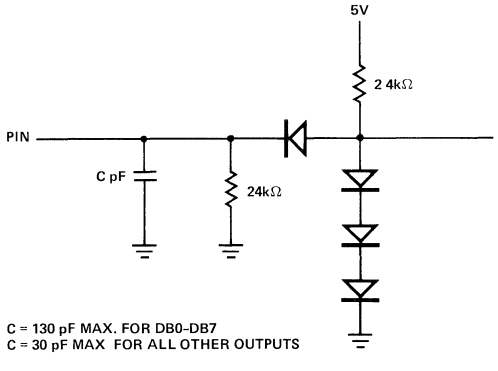
Maximum Ratings

Rating	Symbol	Voltage	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input/Output Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 7 0	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

D.C. Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0 - 70°C)

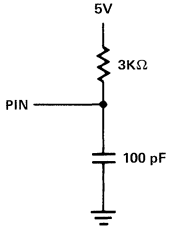
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	-0.3		0.4	V
Input Leakage Current, V_{IN} = V_{SS} +5V A0-A6, $\overline{RS}$, R/$\overline{W}$, RES, 02, CS1, CS2	I_{IN}		1 0	2.5	μA
Input Leakage Current; for High Impedance State (Three State), V_{IN} = 0.4V to 2 4V, D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current, V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	-100	-300		μA
Input Low Current; V_{IN} = 0 4V PA0-PA7, PB0-PB7	I_{IL}		1.0	1.6	mA
Output High Voltage V_{CC} = MIN, I_{LOAD} ≤ -100 μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} ≤ 3 mA(PB0-PB7)	V_{OH}	2 4 1.5			V
Output Low Voltage; V_{CC} = Min , I_{LOAD} ≤ 1 6 mA	V_{OL}			0.4	V
Output High Current (Sourcing), V_{OH} ≥ 2 4V (PA0-PA7, PB0-PB7, D0-D7) ≥ 1.5V Available for direct transistor drive (PB0-PB7)	I_{OH}	-100 3 0	-1000 5.0		μA mA
Output Low Current (Sinking); V_{OL} ≤ 0.4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CLK}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}		10		pF
Power Dissipation (V_{CC} = 5.25V)	P_D			680	mW

Test Load

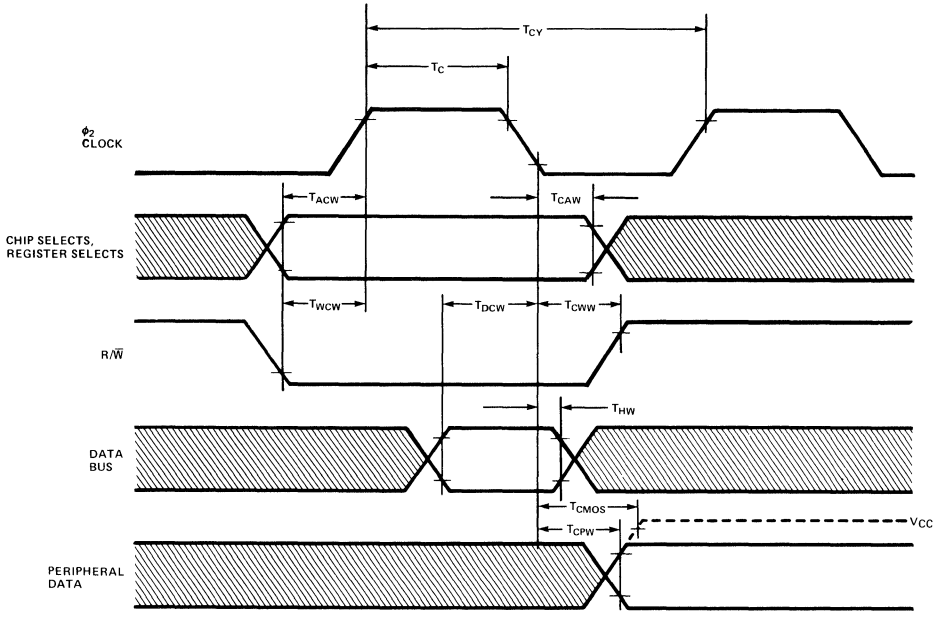


C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX FOR ALL OTHER OUTPUTS

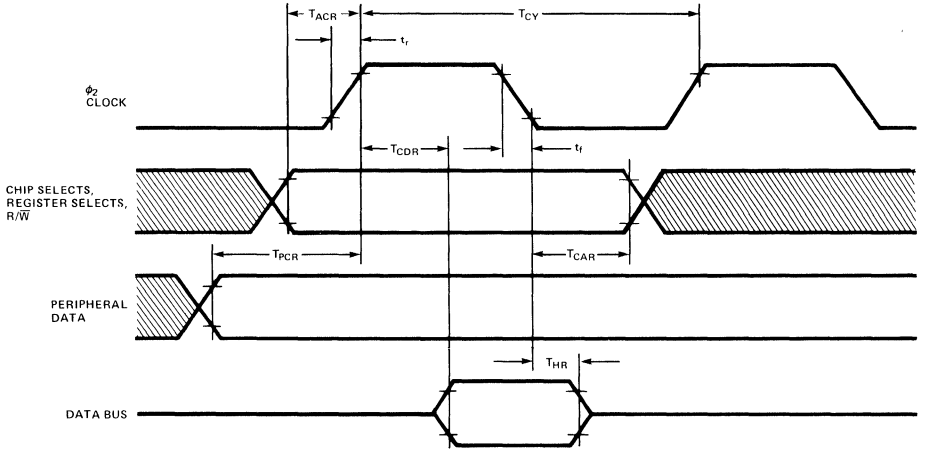
OPEN COLLECTOR OUTPUT TEST LOAD



Write Timing Characteristics



Read Timing Characteristics



Write Timing Characteristics

Symbol	Parameter	SY6532 Min.	SY6532 Max.	SY6532A Min.	SY6532A Max.	Unit
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	φ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	265	–	100	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

NOTE tr, tf = 10 to 30ns.

Read Timing Characteristics

Symbol	Parameter	SY6532 Min.	SY6532 Max.	SY6532A Min.	SY6532A Max.	Unit
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

NOTE: tr, tf = 10 to 30ns.

Interface Signal Description

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc \begin{smallmatrix}+.3\\-.2\end{smallmatrix}$).

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and is used to control the transfer of data to and from the SY6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the SY6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the SY6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is derived from the interrupt control logic. It will normally be high with a low indicating an interrupt from the SY6532. $\overline{IRQ}$ is an open-drain output, permitting several units to be wire-or'ed to the common $\overline{IRQ}$ microprocessor input pin. The $\overline{IRQ}$ output may be activated by a transition on PA7 or timeout of the Interval Timer.

Data Bus (D0-D7)

The SY6532 has eight bi-directional data lines (D0-D7). These lines connect to the system's data bus and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The SY6532 has two 8-bit peripheral I/O Ports, Port A (lines PA0-PA7) and Port B (lines PB0-PB7). Each line is individually programmable as either an input or an output. By writing a "0" to any bit position of the Data Direction Register (DDRA or DDRB) the corresponding line will be programmed as an input. Likewise, by writing a "1" to any bit position in DDRA or DDRB will cause the corresponding line to act as an output.

When a Port line is programmed as an input and its ouput register (ORA or ORB) is read by the MPU, the TTL level on the Port line will be transferred to the data bus. When the Port lines are programmed as outputs, the lines will reflect the data written by the MPU into the output registers. See Edge Sense Interrupt Section for an additional use of PA7.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)

A0-A6 and $\overline{RS}$ are used to address the RAM, I/O registers, Timer and Flag register. CS1 and $\overline{CS2}$ are used to select (enable access to) the SY6532.

Internal Organization

A block diagram of the internal architecture is shown in Figure 1. The SY6532 is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8 static RAM is contained on the SY6532. It is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1, and $\overline{CS2}$.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral I/O. A logic zero in a bit of the data direction register (DDRA and DDRB) causes the corresponding line of the I/O port to act as an input. A logic one causes the corresponding line to act as an output. The voltage on any line programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA lines during a peripheral read operation. For a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the line is allowed to be $\geqslant 2.4$ volts for a logic one and $\leqslant 0.4$ volts for a zero. If the loading on the line does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB lines are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB lines.

Interval Timer

The Timer section of the SY6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 2.

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T, or 1024T increments, where T is the system clock period. When a full count is reached, the interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock continues counting down, but at a 1T rate to a maximum of -255T. This allows the user to read the counter and then determine how long the interrupt has been set.

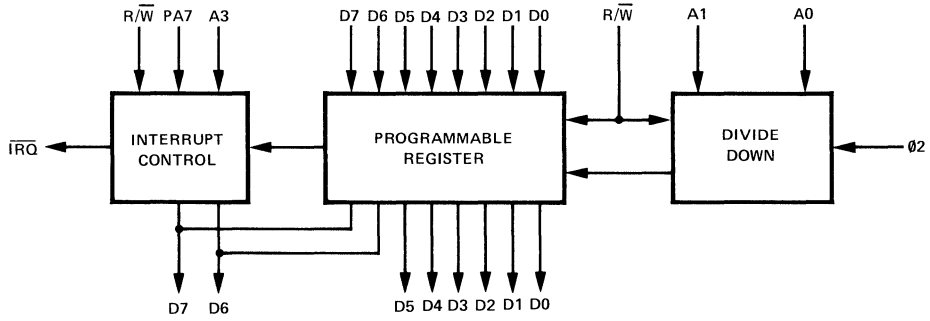
The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of $\overline{IRQ}$, i.e., $A_3 = 1$ enables $\overline{IRQ}$, $A_3 = 0$ disables $\overline{IRQ}$. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read from or written to by the processor. If $\overline{IRQ}$ is enabled by A3 and an interrupt occurs $\overline{IRQ}$ will go low. When the Timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the Timer has counted down to 0 0 0 0 0 0 0 0 an interrupt will occur on the next count time and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the Timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read	= 1 1 1 0 0 1 0 0
Complement	= 0 0 0 1 1 0 1 1
Add 1	= 0 0 0 1 1 1 0 0 = 28.

Figure 2. BASIC ELEMENTS OF INTERVAL TIMER

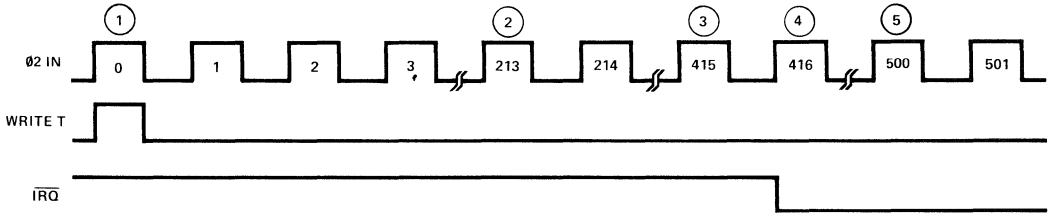


Thus, to arrive at the total elapsed time, merely do a two's complement and add to the original time written into the Timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After an interrupt, whenever the Timer is written or read the interrupt is reset. However, the reading of the Timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 3 illustrates an example of interrupt.

Figure 3. TIMER INTERRUPT TIMING



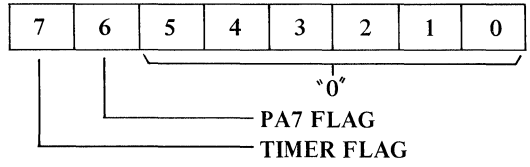
1. Data written into Interval Timers is $0\,0\,1\,1\,0\,1\,0\,0 = 52_{10}$
2. Data in Interval timer is $0\,0\,0\,1\,1\,0\,0\,1 = 25_{10}$
   $52 - \frac{213}{8} - 1 = 52-26-1 = 25$
3. Data in Interval Timer is $0\,0\,0\,0\,0\,0\,0\,0 = 0_{10}$
   $52 - \frac{415}{8} - 1 = 52-51-1 = 0$
4. Interrupt has occurred at $\phi 2$ pulse #416
   Data in Interval Timer = $1\,1\,1\,1\,1\,1\,1\,1$
5. Data in Interval Timer is $1\,0\,1\,0\,1\,1\,0\,0$
   two's complement is $0\,1\,0\,1\,0\,1\,0\,0 = 84_{10}$
   $84 + (52 \times 8) = 500_{10}$

When reading the Timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.

Figure 4. INTERRUPT FLAG REGISTER



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

Addressing

Addressing of the SY6532 is accomplished by the 7 address inputs, the $\overline{RS}$ input and the two chip select inputs CS1 and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and Interval Timer CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O-Timer Section the $\overline{RS}$ input is used. When this input is low the RAM is addressed, when high the I/O Interval Timer section is addressed. To distinguish between Timer and I/O, address line A2 is utilized. When A2 is high the Interval Timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Table 1.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register.

I/O Register - Timer Addressing

Table 1 illustrates the address decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition, Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

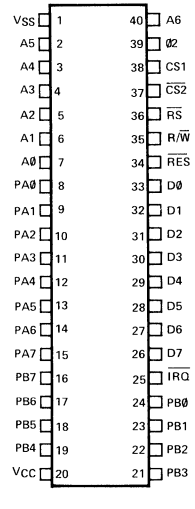
Table 1 ADDRESSING DECODE

FUNCTION	$\overline{RS}$	A6	A5	A4	A3	A2	A1	A0	WR	RD
RAM	L	X	X	X	X	X	X	X	√	√
ORA	H	–	–	–	–	L	L	L	√	√
DDRA	H	–	–	–	–	L	L	H	√	√
ORB	H	–	–	–	–	L	H	L	√	√
DDRB	H	–	–	–	–	L	H	H	√	√
Timer, ÷1, IRQ ON	H	–	–	H	H	H	L	L	√	
Timer, ÷8, IRQ ON	H	–	–	H	H	H	L	H	√	
Timer, ÷64, IRQ ON	H	–	–	H	H	H	H	L	√	
Timer, ÷1024, IRQ ON	H	–	–	H	H	H	H	H	√	
Timer, ÷1, IRQ OFF	H	–	–	H	L	H	L	L	√	
Timer, ÷8, IRQ OFF	H	–	–	H	L	H	L	H	√	
Timer, ÷64, IRQ OFF	H	–	–	H	L	H	H	L	√	
Timer, ÷1024, IRQ OFF	H	–	–	H	L	H	H	H	√	
Read Timer, IRQ ON	H	–	–	–	H	H	–	L		√
Read Timer, IRQ OFF	H	–	–	–	L	H	–	L		√
Read Interrupt Flags	H	–	–	–	–	H	–	H		√
PA7 IRQ OFF, NEG EDGE	H	–	–	L	–	H	L	L	*	
PA7 IRQ OFF, POS EDGE	H	–	–	L	–	H	L	H	*	
PA7 IRQ ON, NEG EDGE	H	–	–	L	–	H	H	L	*	
PA7 IRQ ON, POS EDGE	H	–	–	L	–	H	H	H	*	

NOTES: X = ADDRESS – = ADDRESS BITS DON'T CARE * = DATA BITS ARE "DON'T CARE"

Package Availability 40 Pin Molded DIP

Pin Configuration



Ordering Information

Part Number	Package	Speed
SYP6532	Molded DIP	1 MHz
SYP6532A	Molded DIP	2 MHz

MICRO-PROCESSORS

Synertek.

SY6845R
CRT Controller

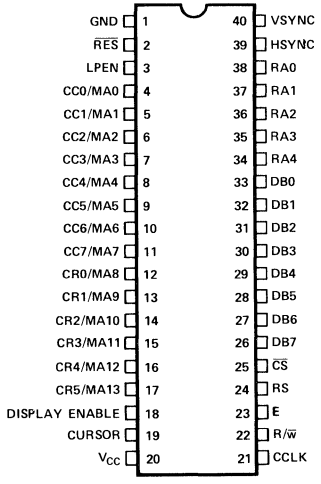
Features

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Compatible with MC6845R.
- Straight-binary addressing for Video Display RAM.

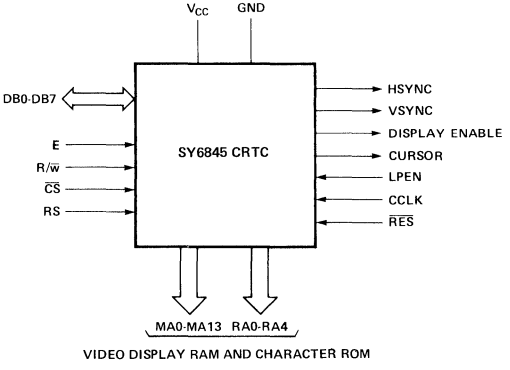
Description

The SY6845 is a CRT Controller intended to provide capability for interfacing any microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Designation



Interface Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

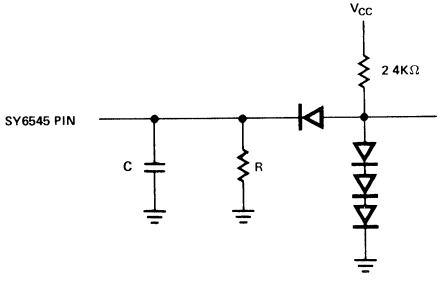
Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

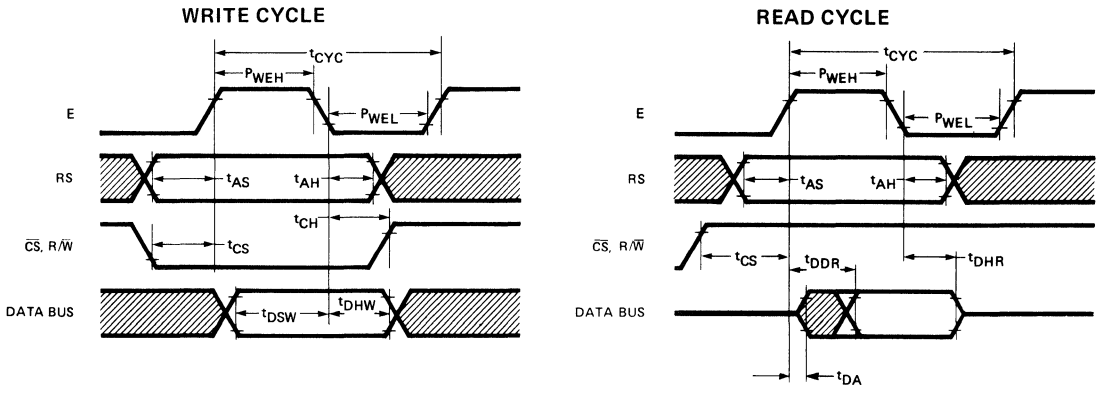
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	–		±10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4		–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–		0.4	V
P_D	Power Dissipation	–	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	– –		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	–		10.0	pF

Test Load



R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D_0-D_7
C = 30 pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics



Write Timing Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845R		SY6845RA		SY6845RB		SY6845RC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	μs
P_{WEH}	E Pulse Width, High	440	—	200	—	150	—	115	—	ns
P_{WEL}	E Pulse Width, Low	420	—	190	—	140	—	100	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{AH}	Address Hold Time	0	—	0	—	0	—	0	—	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{CH}	R/$\overline{W}$, $\overline{CS}$ Hold Time	0	—	0	—	0	—	0	—	ns
t_{DSW}	Data Bus Set-Up Time	165	—	60	—	60	—	60	—	ns
t_{DHW}	Data Bus Hold Time	10	—	10	—	10	—	10	—	ns

(t_r and t_f = 10 to 30ns)

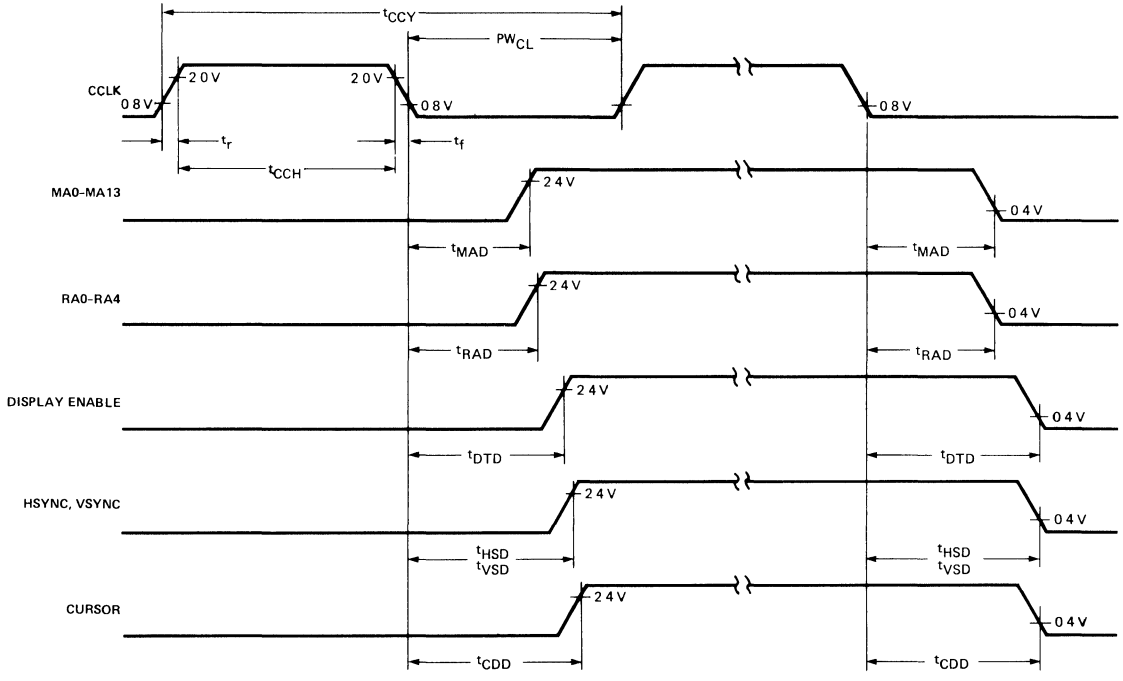
Read Timing Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845R		SY6845RA		SY6845RB		SY6845RC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	μs
P_{WEH}	E Pulse Width, High	440	—	200	—	150	—	115	—	ns
P_{WEL}	E Pulse Width, Low	420	—	190	—	140	—	100	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{AH}	Address Hold Time	0	—	0	—	0	—	0	—	ns
t_{CS}	R/$\overline{W}$, $\overline{CS}$ Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{DDR}	Read Access Time (Valid Data)	—	290	—	150	—	100	—	85	ns
t_{DHR}	Read Hold Time	20	60	20	60	20	60	20	60	ns
t_{DA}	Data Bus Active Time (Invalid Data)	40	—	40	—	40	—	40	—	ns

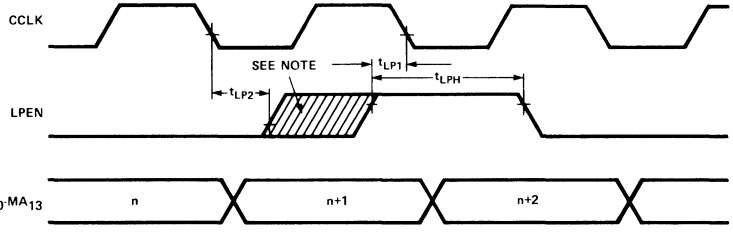
(t_r and t_f = 10 to 30ns)

Memory and Video Interface Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)



Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{CCH}	Minimum Clock Pulse Width, High	200			ns
T_{CCV}	Clock Frequency			2.5	MHz
t_{Cr}, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	300	ns
t_{HSD}	Horizontal Sync Delay Time		160	300	ns
t_{VSD}	Vertical Sync Delay Time		160	300	ns
t_{CDD}	Cursor Display Timing Delay Time		160	300	ns

Light Pen Strobe Timing



NOTE
"Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register
t_{LP2} and t_{LP1} are time positions causing uncertain results

Symbol	Characteristic	SY6845R		SY6845RA		SY6845RB		SY6845RC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	—	100	—	100	—	100	—	ns
t_{LP1}	LPEN to CCLK Delay	—	120	—	120	—	120	—	120	ns
t_{LP2}	CCLK to LPEN Delay	—	0	—	0	—	0	—	0	ns

t_r and t_f = 20ns (max.)

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the SY6845. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6845 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6845; a low on the R/$\overline{W}$ pin allows a write to the SY6845.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6845 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6845. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal.

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable.

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0–MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

- Binary Addressing
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

Description of Internal Registers

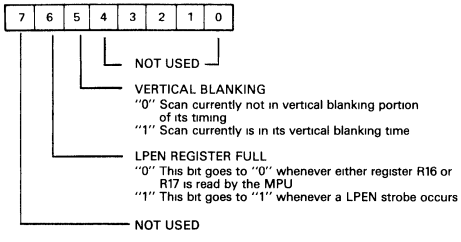
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6845 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6845 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 2-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

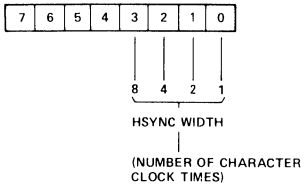
This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

Horizontal and Vertical SYNC Widths (R3)

This 4-bit register programs the width of HSYNC.



VSYNC width is set to 16 scan line times.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

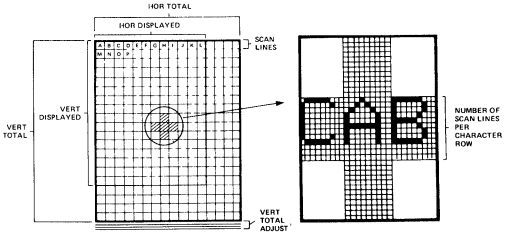


Figure 1. Video Display Format

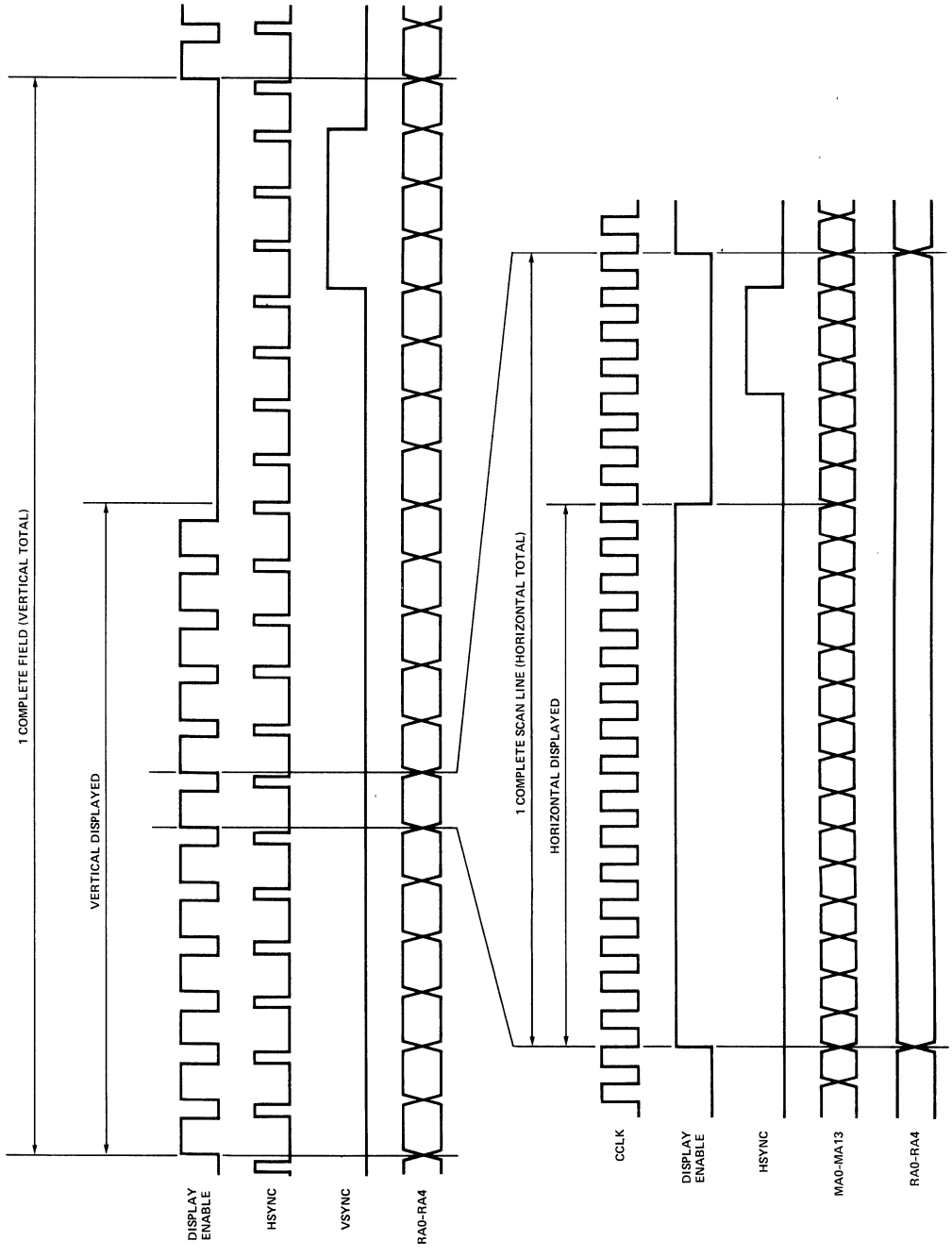


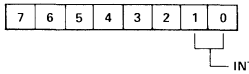
Figure 2. Vertical and Horizontal Timing

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6845 and is outlined as follows:



BIT 1	BIT 0	OPERATION
X	0	Non-Interlace
0	1	Interlace SYNC Raster Scan
1	1	Interlace SYNC and Video Raster Scan

Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT 6	BIT 5	CURSOR MODE
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16x field rate
1	1	Blink at 32x field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

$\overline{CS}$	RS	Address Reg 4	3	2	1	0	Reg No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg	Reg No		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√			L	V					
0	1	0	0	0	0	0	R0	Horiz Total	# Charac. -1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz Displayed	# Charac		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz Sync Position	# Charac		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		√					H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert Total	# Charac. Row -1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert Total Adjust	# Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert Displayed	# Charac Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert Sync Position	# Charac Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√							I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines -1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●

Notes: ● Designates binary bit
▨ Designates unused bit. Reading this bit is always "0"

Figure 3. Internal Register Summary.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6845 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	- - -	- - -	77	78	79	80	81	- - -	89
80	81	82	- - -	- - -	157	158	159	160	161	- - -	169
160	161	162	- - -	- - -	237	238	239	240	241	- - -	249
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1760	1761	1762	- - -	- - -	1837	1838	1839	1840	1841	- - -	1849
1840	1841	1842	- - -	- - -	1917	1918	1919	1920	1921	- - -	1929
1920	1921	1922	- - -	- - -	1997	1998	1999	2000	2001	- - -	2009
2000	2001	2002	- - -	- - -	2077	2078	2079	2080	2081	- - -	2089
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2640	2641	2642	- - -	- - -	2717	2718	2719	2720	2721	- - -	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

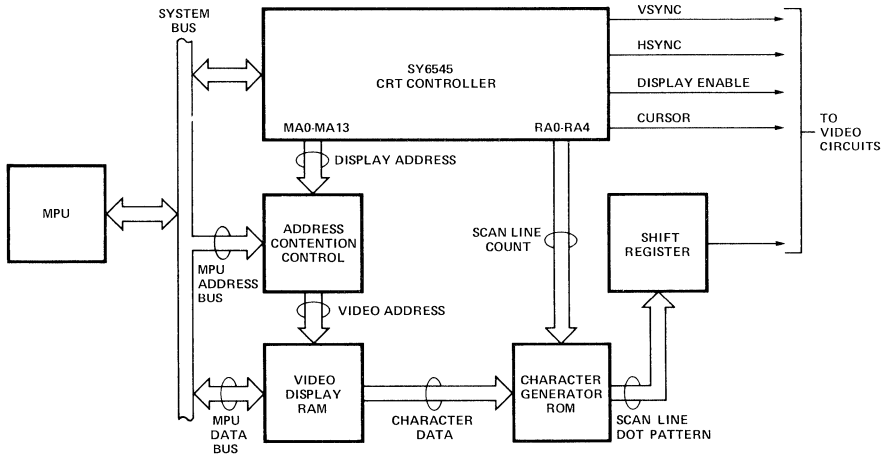


Figure 5. Shared Memory System Configuration

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 5, it is clear that both the SY6845 and the system MPU must be capable of addressing the video display memory The SY6845 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6845 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6845 and the MPU has immediate access.

- $\phi 1/\phi 2$ Memory Interleaving

  This method permits both the SY6845 and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when E is low), the SY6845 address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the SY6845 and the MPU have unimpeded access to the memory. Figure 6 illustrates the timings.

Interlace Modes

There are three raster-scan display modes (see Figure 7).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 8 and is the only difference in the SY6845 operation in this mode

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

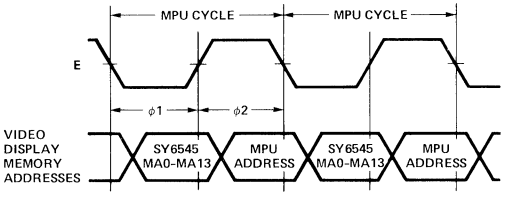


Figure 6. $\phi 1/\phi 2$ Interleaving.

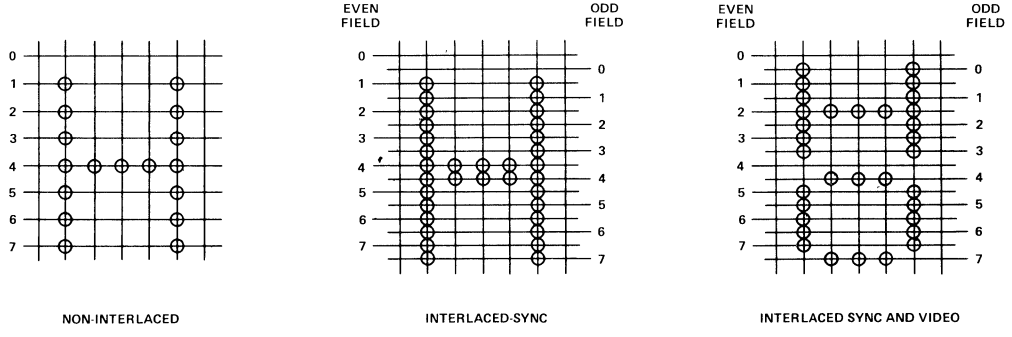


Figure 7. Comparison of Display Modes.

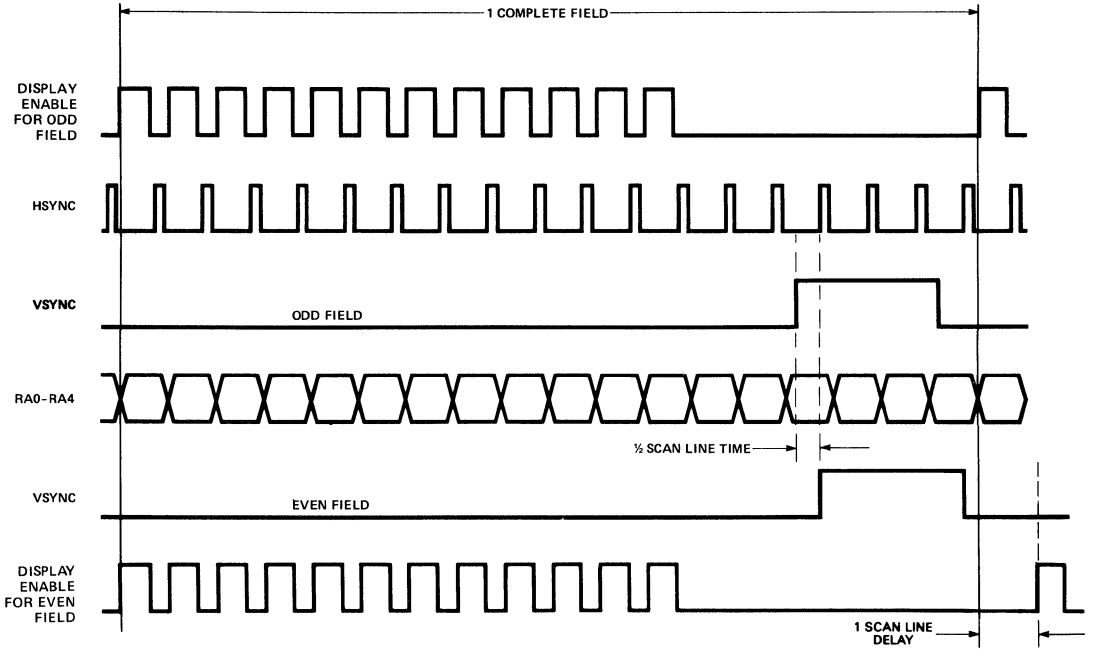


Figure 8. Interface Sync Mode and Interface Sync & Video Mode Timing

Package Availability

40 Pin Molded DIP

Ordering Information

Part Number	Package	CPU Clock Rate
SYP6845	Molded DIP	1 MHz
SYP6845RA	Molded DIP	2 MHz
SYP6845RB	Molded DIP	3 MHz

Synertek.

SY6845E
CRT Controller

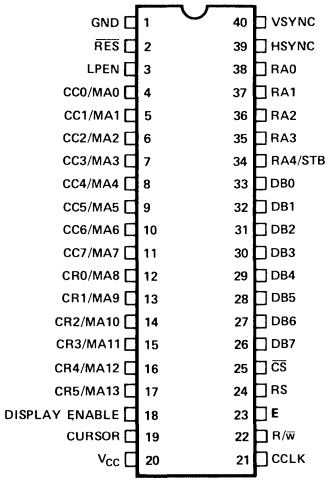
Features

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845R.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6845
- Internal status register.
- 3.7 MHz Character Clock
- Transparent Address Mode

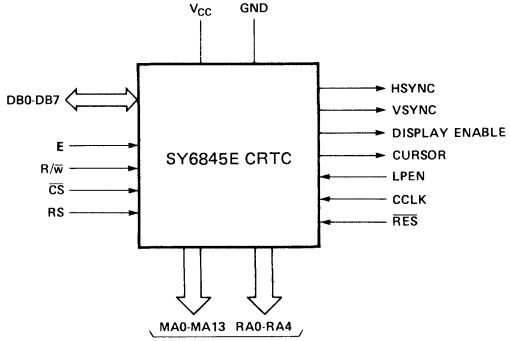
Description

The SY6845E is a CRT Controller intended to provide capability for interfacing any 8 or 16 bit microprocessor family to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

Pin Configuration



Interface Diagram



VIDEO DISPLAY RAM AND CHARACTER ROM

MICRO-PROCESSORS

Absolute Maximum Ratings*

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

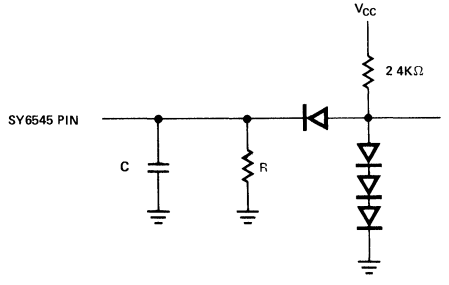
Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0-70° C, unless otherwise noted)

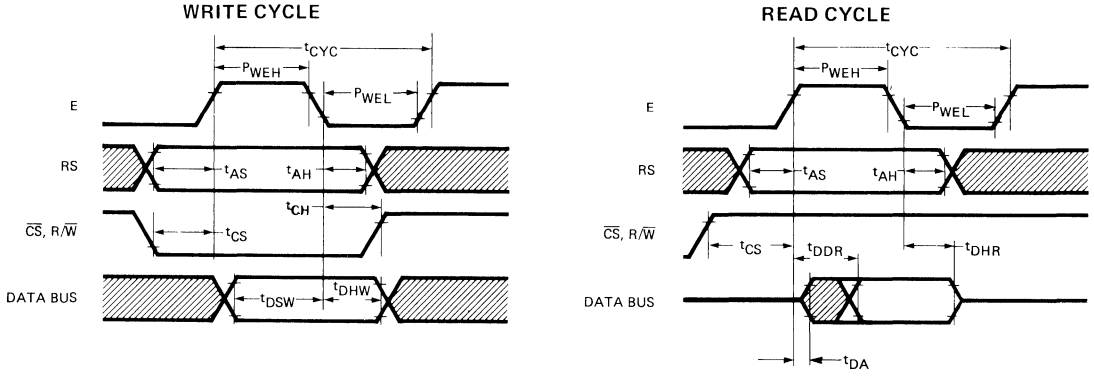
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
I_{IN}	Input Leakage (ϕ2, R/W, RES, CS, RS, LPEN, CCLK)	—		2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	—		±10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = −205μA (DB0-DB7) I_{LOAD} = −100μA (all others)	2.4		—	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	—		0.4	V
P_D	Power Dissipation	—	325	650	mW
C_{IN}	Input Capacitance ϕ2, R/W, RES, CS, RS, LPEN, CCLK DB0-DB7	— —		10.0 12.5	pF pF
C_{OUT}	Output Capacitance	—		10.0	pF

Test Load



R = 11KΩ FOR DB_0-DB_7
R = 24KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR D_0-D_7
C = 30 pF ALL OTHER OUTPUTS

MPU Bus Interface Characteristics



Write Timing Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	μs
P_{WEH}	E Pulse Width, High	440	—	200	—	150	—	115	—	ns
P_{WEL}	E Pulse Width, Low	420	—	190	—	140	—	100	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{AH}	Address Hold Time	0	—	0	—	0	—	0	—	ns
t_{CS}	R/W, CS Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{CH}	R/W, CS Hold Time	0	—	0	—	0	—	0	—	ns
t_{DSW}	Data Bus Set-Up Time	165	—	60	—	60	—	60	—	ns
t_{DHW}	Data Bus Hold Time	10	—	10	—	10	—	10	—	ns

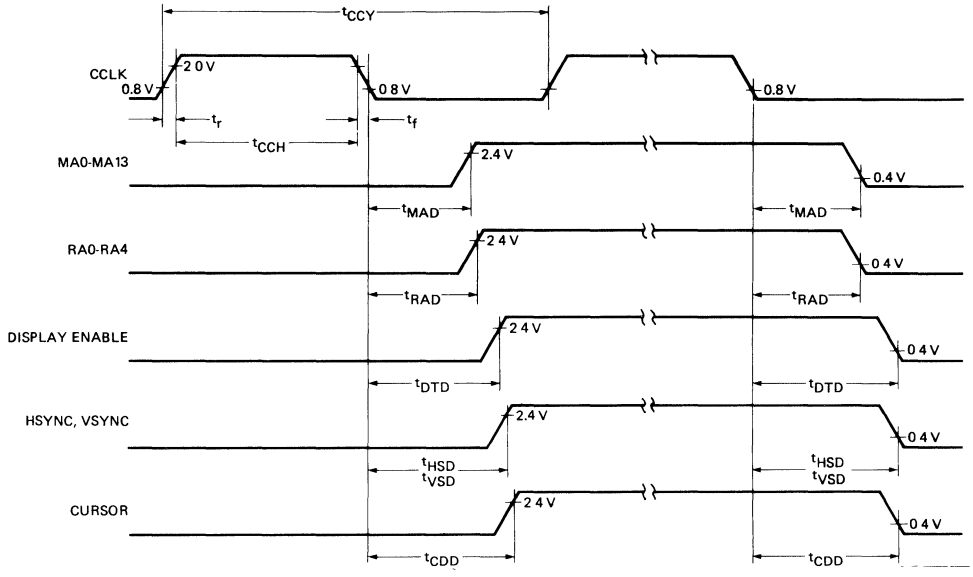
(t_r and t_f = 10 to 30ns)

Read Timing Characteristics (V_{CC} = 5.0V ±5%, T_A = 0 – 70°C, unless otherwise noted)

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	0.33	—	0.25	—	μs
P_{WEH}	ϕ2 Pulse Width, High	440	—	200	—	150	—	115	—	ns
P_{WEL}	ϕ2 Pulse Width, Low	420	—	190	—	140	—	100	—	ns
t_{AS}	Address Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{AH}	Address Hold Time	0	—	0	—	0	—	0	—	ns
t_{CS}	R/W, CS Set-Up Time	80	—	40	—	30	—	20	—	ns
t_{DDR}	Read Access Time (Valid Data)	—	290	—	150	—	100	—	85	ns
t_{DHR}	Read Hold Time	10	—	10	—	10	—	10	—	ns
t_{DA}	Data Bus Active Time (Invalid Data)	20	60	20	60	20	60	20	60	ns
t_{TAD}	MA0-MA13 Switching Delay (Refer to Figure Trans. Addressing)	100 typ.	160	100 typ.	160	90 typ.	130	60 typ.	95	ns

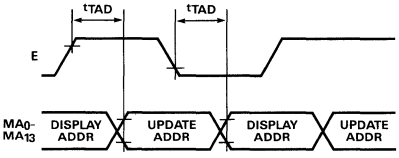
(t_r and t_f = 10 to 30ns)

Memory and Video Interface Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

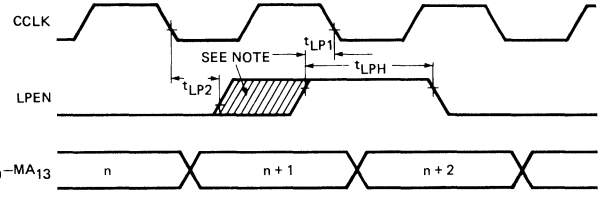


Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CCH}	Minimum Clock Pulse Width, High	130			ns
t_{CCY}	Clock Frequency			3.7	MHz
t_r, t_f	Rise and Fall Time for Clock Input			20	ns
t_{MAD}	Memory Address Delay Time		100	160	ns
t_{RAD}	Raster Address Delay Time		100	160	ns
t_{DTD}	Display Timing Delay Time		160	250	ns
t_{HSD}	Horizontal Sync Delay Time		160	250	ns
t_{VSD}	Vertical Sync Delay Time		160	250	ns
t_{CDD}	Cursor Display Timing Delay Time		160	250	ns

Transparent Addressing (Φ1/Φ2 Interleaving)



Light Pen Strobe Timing



NOTE "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register
t_{LP2} and t_{LP1} are time positions causing uncertain results

Symbol	Characteristic	SY6845E		SY6845EA		SY6845EB		SY6845EC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{LPH}	LPEN Strobe Width	100	—	100	—	100	—	100	—	ns
t_{LP1}	LPEN to CCLK Delay	—	120	—	120	—	120	—	120	ns
t_{LP2}	CCLK to LPEN Delay	—	0	—	0	—	0	—	0	ns

t_r and t_f = 20ns (max.)

MPU Interface Signal Description

E (Enable)

The enable signal is the system input and is used to trigger all data transfers between the system microprocessor and the SY6845. Since there is no maximum limit to the allowable E cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6845 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6845; a low on the R/$\overline{W}$ pin allows a write to the SY6845.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6845 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6845. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

Video Interface Signal Description

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6845 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

Memory Address Signal Description

MA0–MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0–MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0–MA7 function as column addresses CC0–CC7, and MA8–MA13, as row addresses CR0–CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6845 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6845 with only a small amount of external circuitry.

Description of Internal Registers

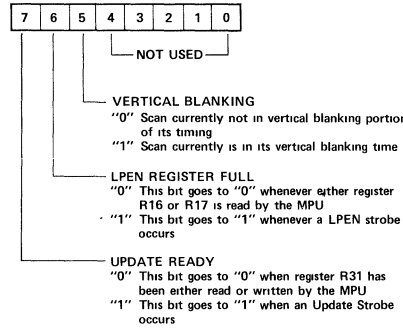
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6845 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6845 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

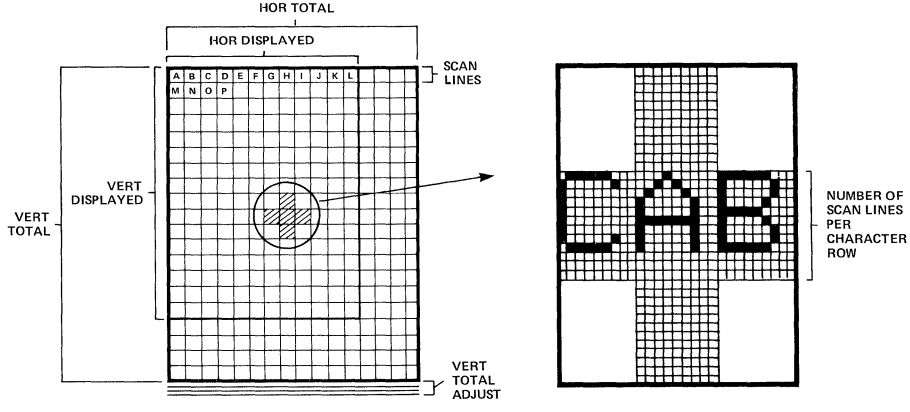


Figure 1. Video Display Format

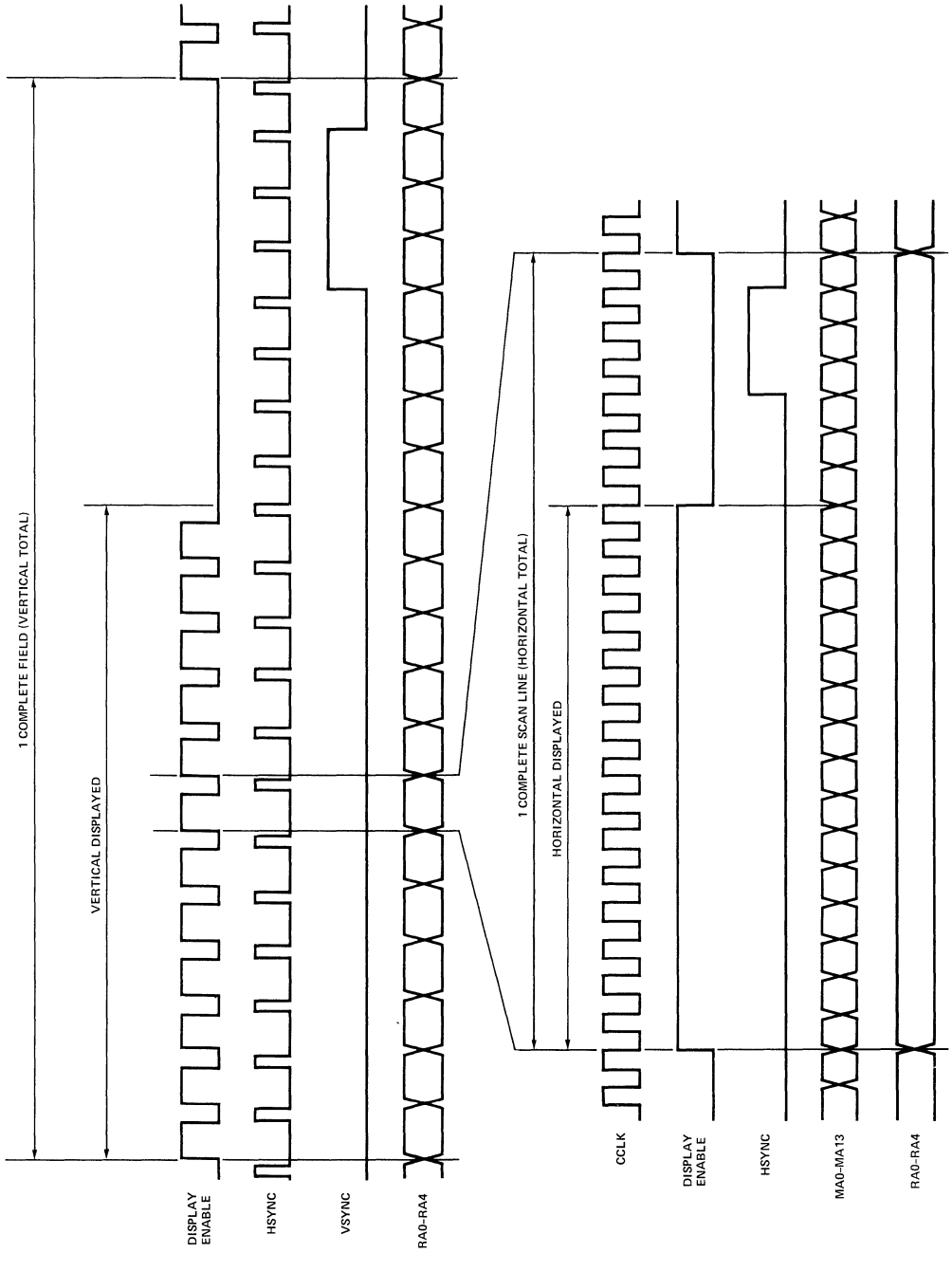
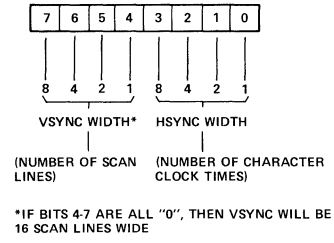


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE

Control of these parameters allows the SY6845 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg	Reg No		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz Total	# Charac. -1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz Displayed	# Charac		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz Sync Position	# Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert Total	# Charac. Row -1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert Total Adjust	# Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert Displayed	# Charac Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert Sync Position	# Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines -1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)	Row		√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)	Col		√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)	Row	√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)	Col	√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			√				●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes ● Designates binary bit

▨ Designates unused bit Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

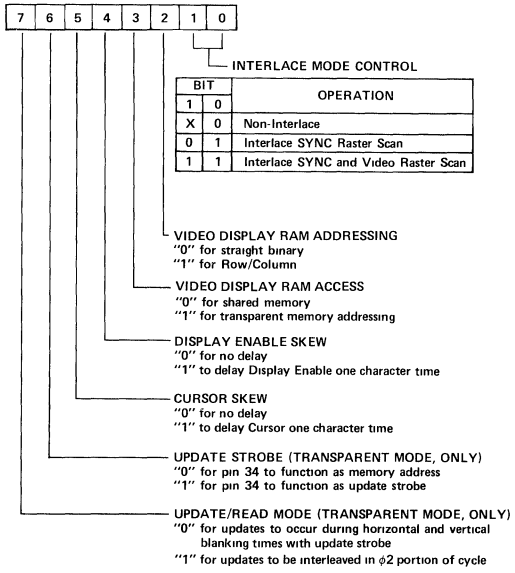
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6845 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 16x field rate (fast)
1	1	Blink at 32x field rate (slow)

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6845 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

Description of Operation

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	- - -	- - -	77	78	79	80	81	- - -	89
80	81	82	- - -	- - -	157	158	159	160	161	- - -	169
160	161	162	- - -	- - -	237	238	239	240	241	- - -	249
⋮							⋮				⋮
1760	1761	1762	- - -	- - -	1837	1838	1839	1840	1841	- - -	1849
1840	1841	1842	- - -	- - -	1917	1918	1919	1920	1921	- - -	1929
1920	1921	1922	- - -	- - -	1997	1998	1999	2000	2001	- - -	2009
2000	2001	2002	- - -	- - -	2077	2078	2079	2080	2081	- - -	2089
⋮							⋮				⋮
2640	2641	2642	- - -	- - -	2717	2718	2719	2720	2721	- - -	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34

DISPLAY = 24

ROW ADDRESS (MA8-MA13)

	0	1	2			77	78	79	80	81		89
0	0	1	2	- - -	- - -	77	78	79	80	81	- - -	89
1	256	257	258	- - -	- - -	333	334	335	336	337	- - -	345
2	512	513	514	- - -	- - -	589	590	591	592	593	- - -	601
⋮								⋮				⋮
21												
22	5632	5633	5634	- - -	- - -	5709	5710	5711	5712	5713	- - -	5721
23	5888	5889	5890	- - -	- - -	5965	5966	5967	5968	5969	- - -	5977
24	6144	6145	6146	- - -	- - -	6221	6222	6223	6224	6225	- - -	6233
25	6400	6401	6402	- - -	- - -	6477	6478	6479	6480	6481	- - -	6489
⋮								⋮				⋮
33	8448	8449	8450	- - -	- - -	8525	8526	8527	8528	8529	- - -	8537

ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6845 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6845 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6845. All MPU accesses are made via the SY6845 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

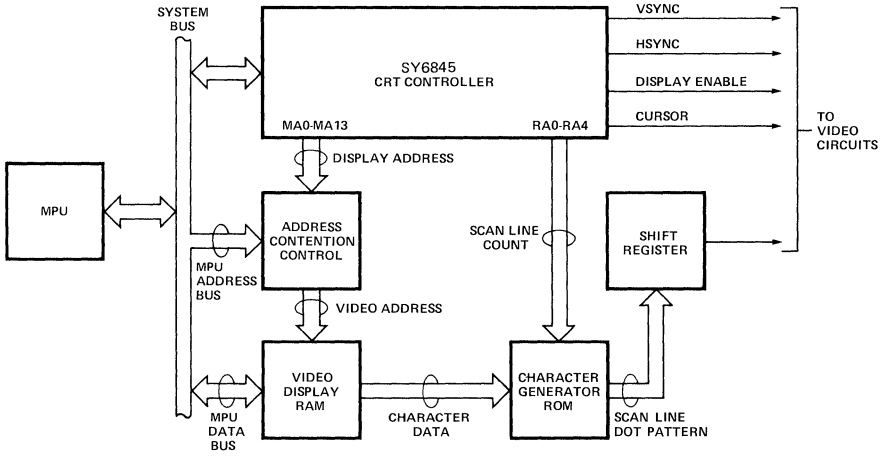


Figure 5. Shared Memory System Configuration

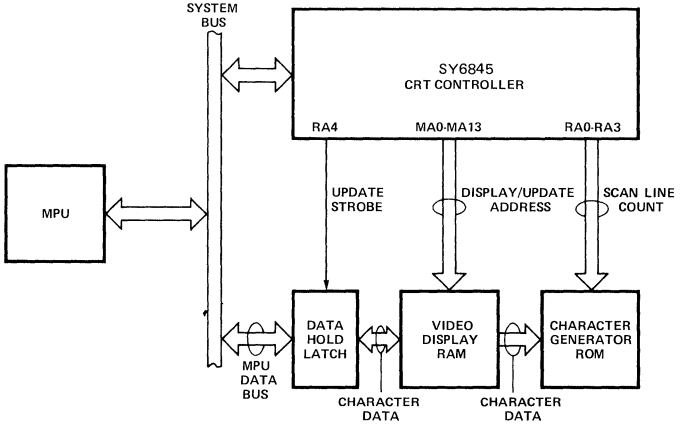


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the SY6845 and the system MPU must be capable of addressing the video display memory. The SY6845 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6845 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6845 and the MPU has immediate access.

- $\phi1/\phi2$ Memory Interleaving

  This method permits both the SY6845 and the MPU access to the video display memory by time-sharing via the system $\phi1$ and $\phi2$ clocks. During the $\phi1$ portion of each cycle (the time when E is low), the SY6845 address outputs are gated to the video display memory. In the $\phi2$ time, the MPU address lines are switched in. In this way, both the SY6845 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

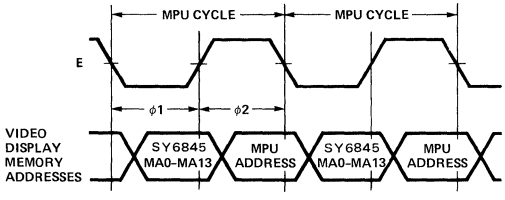


Figure 7. $\phi1/\phi2$ Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the SY6845. In effect, the contention is handled by the SY6845. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi1/\phi2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi2$ address is generated from the Update Address Register (Registers R18 and R19) in the SY6845. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi2$. Figure 8 shows the timing.

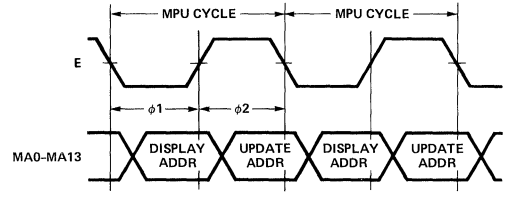


Figure 8. $\phi1/\phi2$ Transparent Interleaving

- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation. The details of their application are covered thoroughly in a related Technical Note available from Synertek.

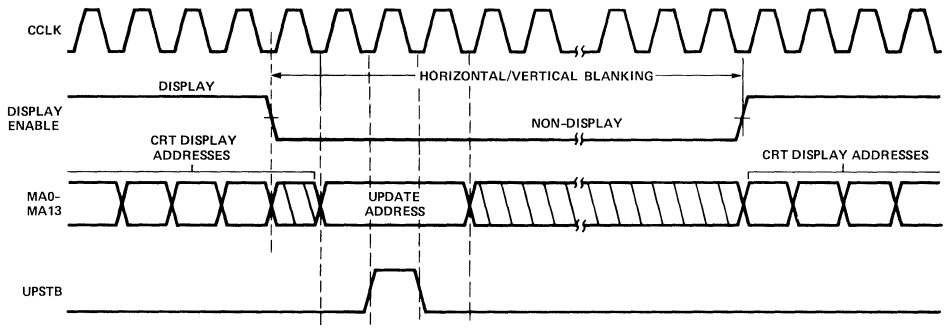


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the SY6845 operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered.

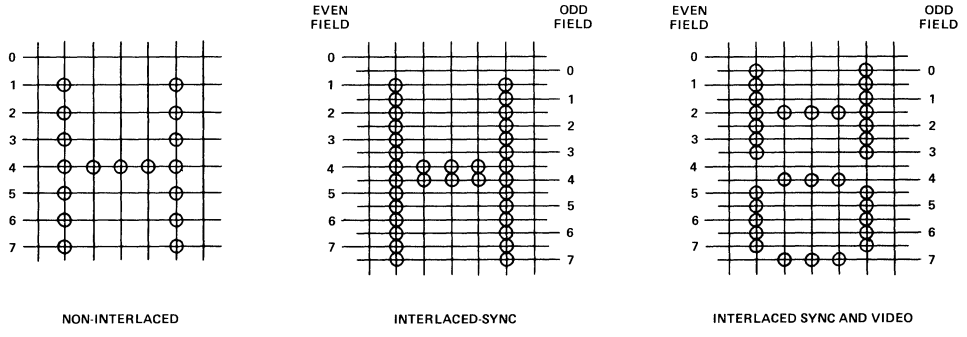


Figure 10. Comparison of Display Modes.

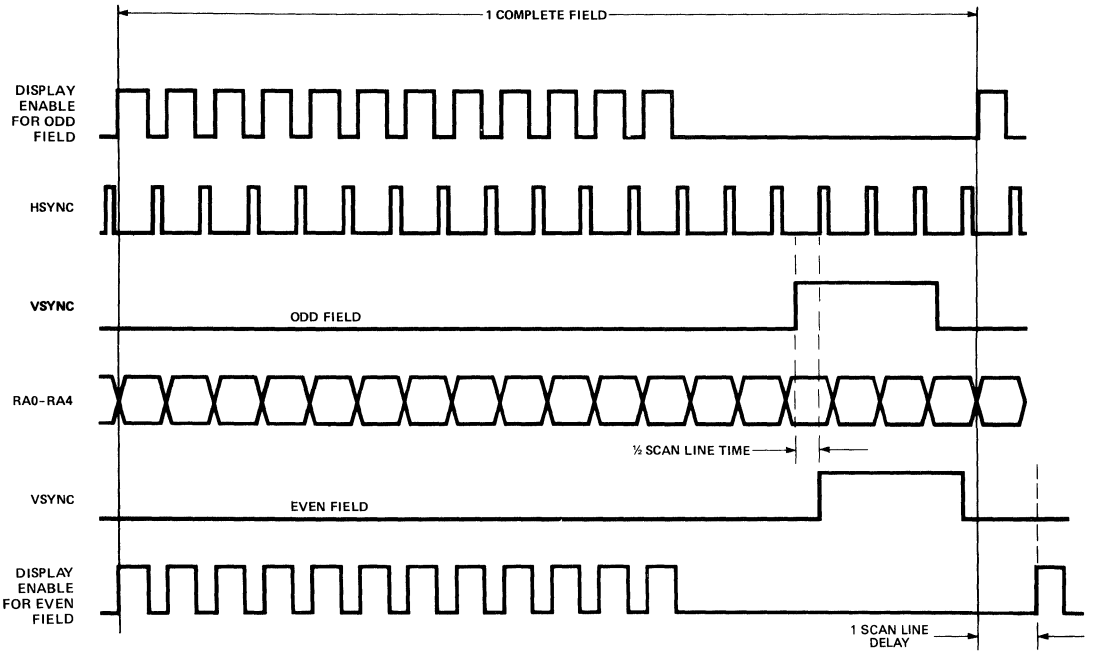


Figure 11. Interlace Sync Mode and Interlace Sync & Video Mode Timing

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 12 illustrates the effect of the delays.

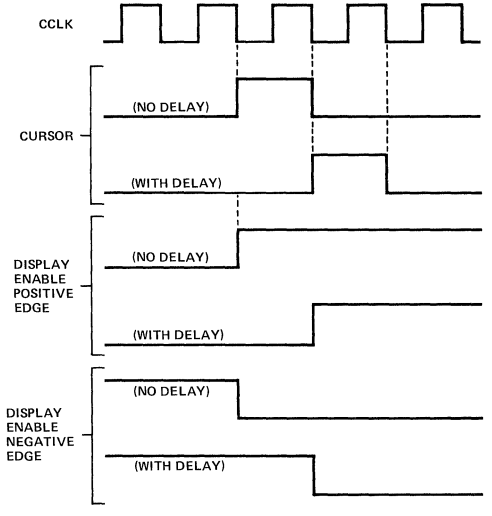


Figure 12. Cursor and Display Enable Skew

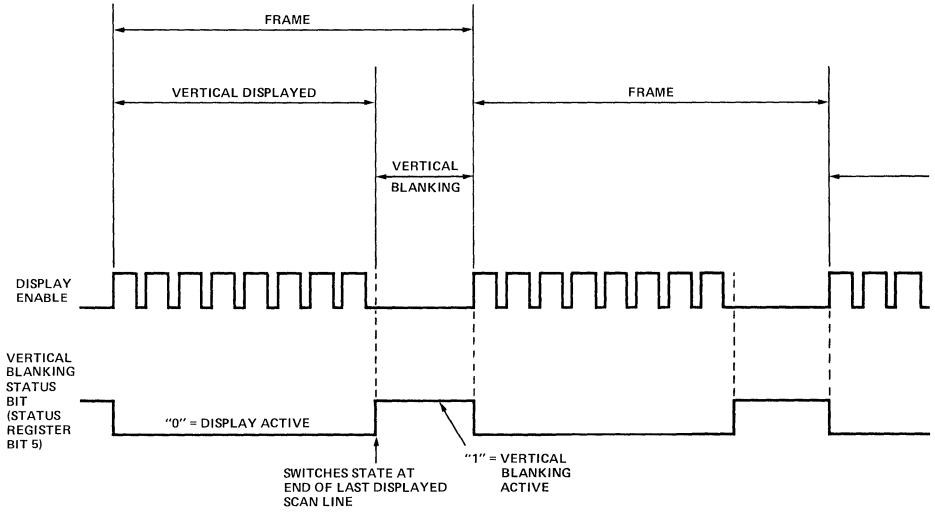


Figure 13. Operation of Vertical Blanking Status Bit

Package Availability 40 Pin Molded DIP

Ordering Information

Part Number	Package	CPU Clock Rate
SYP6845E	Molded DIP	1 MHz
SYP6845EA	Molded DIP	2 MHz
SYP6845EB	Molded DIP	3 MHz

Detailed help in Application Notes 7 and 8 available from Synertek sales offices.

CRTC Register Comparison

NON-INTERLACE

REGISTER	SY6845R	MC6845R HD6845R	HD6845S	SY6545-1	SY6845E
R0 HORIZONTAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R1 HORIZONTAL DISP	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R2 HORIZONTAL SYNC	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R3 HORIZONTAL AND VERT SYNC WIDTH	HORIZONTAL	HORIZONTAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL	HORIZONTAL AND VERTICAL
R4 VERTICAL TOT	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R5 VERTICAL TOT ADJ	ANY VALUE	ANY VALUE	ANY VALUE	ANY VALUE EXCEPT R5 = (R9H) • X	ANY VALUE
R6 VERTICAL DISP	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4	ANY VALUE <R4
R7 VERTICAL SYNC POS	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL-1
R8 MODE REG BITS 0 AND 1	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT	INTERLACE MODE SELECT
BITS 2	—	—	—	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING	ROW/COLUMN OR STRAIGHT BINARY ADDRESSING
BITS 3	—	—	—	SHARED OR TRANSPARENT ADDR	SHARED OR TRANSPARENT ADDR
BITS 4	—	—	DISPEN SKEW	DISPEN SKEW	DISPEN SKEW
BITS 5	—	—	DISPEN SKEW	CURSOR SKEW	CURSOR SKEW
BITS 6	—	—	CURSOR SKEW	RA4/UPSTB	RA4/UPSTB
BITS 7	—	—	CURSOR SKEW	TRANSPARENT MODE SELECT	TRANSPARENT MODE SELECT
R9 SCAN LINES	TOT-1	TOT-1	TOT-1	TOT-1	TOT-1
R10 CURSOR START	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R11 CURSOR END	ACTUAL	ACTUAL	ACTUAL	ACTUAL	ACTUAL
R12/R13 DISP ADDR	WRITE ONLY	WRITE ONLY	READ/WRITE	WRITE ONLY	WRITE ONLY
R14/R15 CURSOR POS	READ/WRITE	WRITE ONLY	READ/WRITE	READ/WRITE	READ/WRITE
R16/R17 LPEN REG	READ ONLY	READ ONLY	READ ONLY	READ ONLY	READ ONLY
R18/R19 UPDATE ADDR REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
R31 DUMMY REG	N/A	N/A	N/A	TRANSPARENT MODE ONLY	TRANSPARENT MODE ONLY
STATUS REG	YES	NO	NO	YES	YES
INTERLACE SYNC					
R0	TOT-1 = ODD OR EVEN	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD	TOT-1 = ODD OR EVEN
INTERLACE SYNC AND VIDEO					
R4 VERTICAL	TOT-1	TOT-1	TOT-1	TOT/2-1	TOT-1
R6 VERT DISP	TOT	TOT/2	TOT	TOT/2	TOT
R7 VERT SYNC	ACTUAL-1	ACTUAL-1	ACTUAL-1	ACTUAL/2	ACTUAL-1
R9 SCAN LINES	TOT-1 ODD/EVEN	TOT-1 ONLY EVEN	TOT-2 ODD/EVEN	TOT-1 ODD/EVEN	TOT-1 ODD/EVEN
R10 CURSOR START R11 CURSOR END	ODD/EVEN ODD/EVEN	BOTH ODD OR BOTH EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN	ODD/EVEN ODD/EVEN
CCLK	2.5 MHz	2.5 MHz	3.7 MHz	2.5 MHz	3.7 MHz

Synertek.

SY6551

Asynchronous Communication Interface Adapter

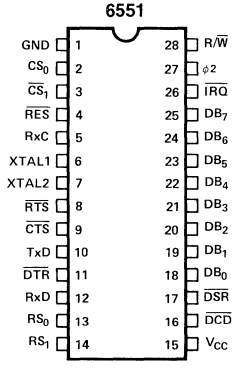
Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable. word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

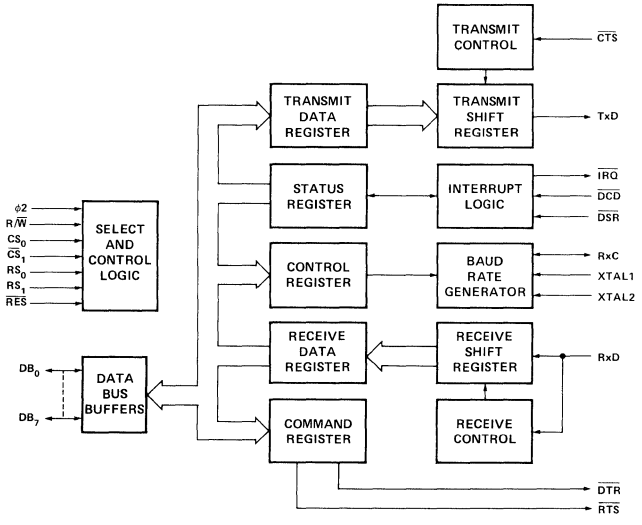
Description

The SY6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Pin Configuration



Block Diagram



MICRO-PROCESSORS

Absolute Maximum Ratings*

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to +7.0V
Operating Temperature	T_{OP}	0°C to 70°C
Storage Temperature	T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

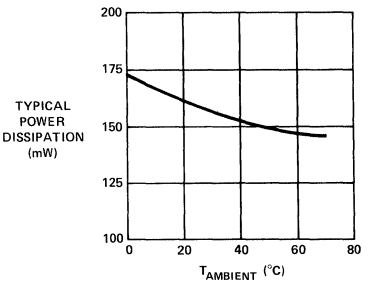
Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V
Input Leakage Current: V_{IN} = 0 to 5V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–	±1.0	±2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–	±2.0	±10.0	μA
Output High Voltage: I_{LOAD} = -100μA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-100	–	–	μA
Output Low Current (Sinking): V_{OL} = 0.4V (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–	1.0	10.0	μA
Clock Capacitance (ϕ2)	C_{CLK}	–	–	20	pF
Input Capacitance (Except XTAL1 and XTAL2)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} = 5.25V	P_D	–	170	300	mW

Power Dissipation vs. Temperature



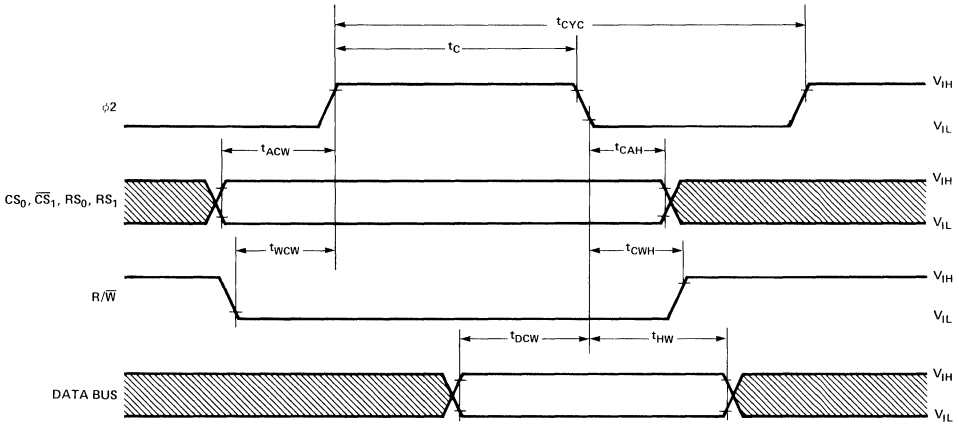


Figure 2. Write Timing Characteristics

Write Cycle (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
φ2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACW}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/W Set-Up Time	t_{WCW}	120	–	70	–	ns
R/W Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns

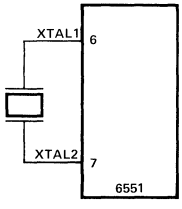
(t_r and t_f = 10 to 30 ns)

Crystal Specification

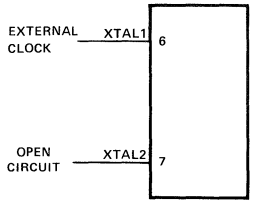
1. Temperature stability ± 0.01% (0° to 70°C)
2. Characteristics at 25°C ± 2°C
   a. Frequency (MHz) 1.8432
   b. Frequency tolerance (±%) 0.02
   c. Resonance mode Series
   d. Equivalent resistance (ohm) 400 max.
   e. Drive level mW 2
   f. Shunt capacitance pF 7 max.
   g. Oscillation mode Fundamental

No other external components should be in the crystal circuit

Clock Generation



INTERNAL CLOCK



EXTERNAL CLOCK

MICRO-PROCESSORS

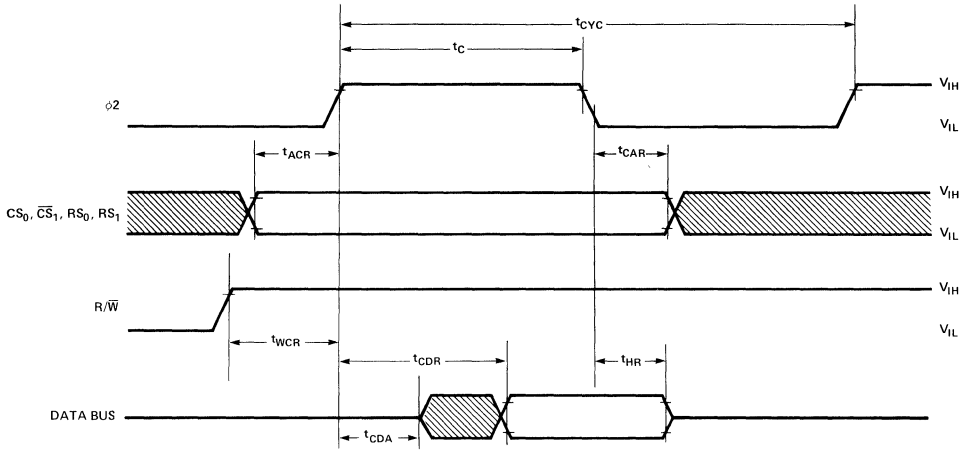
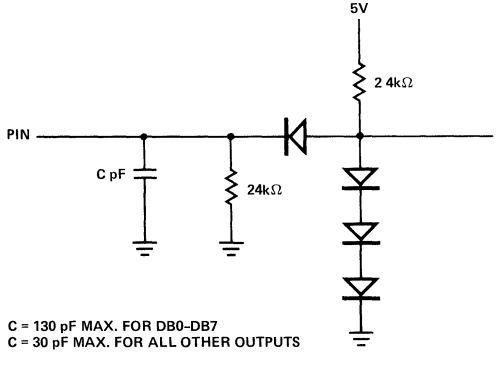


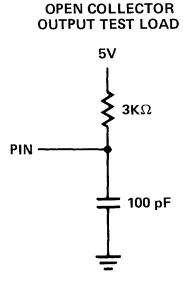
Figure 3. Read Timing Characteristics

Read Cycle (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
Pulse Width (φ2)	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACR}	120	–	70	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCR}	120	–	70	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Data Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

Test Load





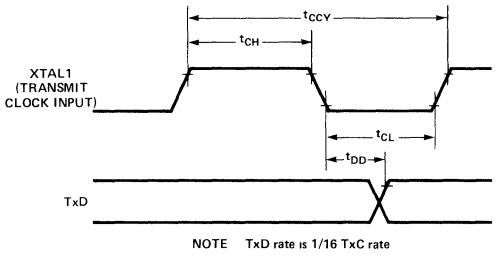


Figure 4a. Transmit Timing with External Clock

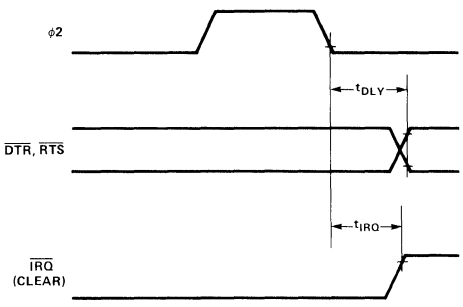


Figure 4b. Interrupt and Output Timing

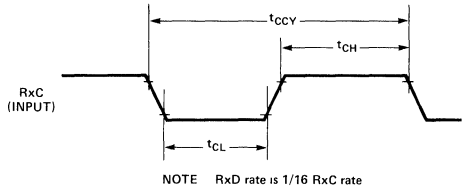


Figure 4c. Receive External Clock Timing

Transmit/Receive Characteristics

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTAL1 to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

(t_r, t_f = 10 to 30 ns input clocks only)

*The baud rate with external clocking is: $\text{Baud Rate} = \frac{1}{16 \times T_{CCY}}$

Interface Signal Description

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6551. A low on the R/$\overline{W}$ pin allows a write to the SY6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0 - DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, $\overline{CS_1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The SY6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_ϕ, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various SY6551 internal registers. The following table indicates the internal register select coding:

MICRO-PROCESSORS

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the SY6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the SY6551 to the modem. A low on $\overline{DTR}$ indicates the SY6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the SY6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the SY6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Internal Organization

The Transmitter/Receiver sections of the SY6551 are depicted by the block diagram in Figure 5.

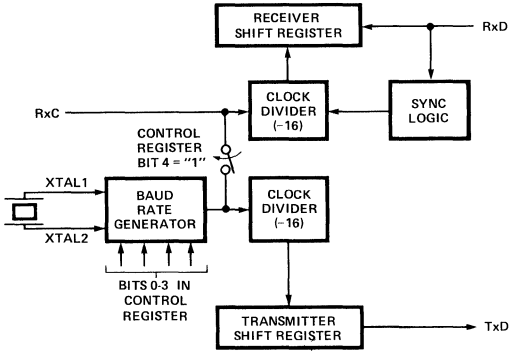


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the SY6551.

Control Register

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

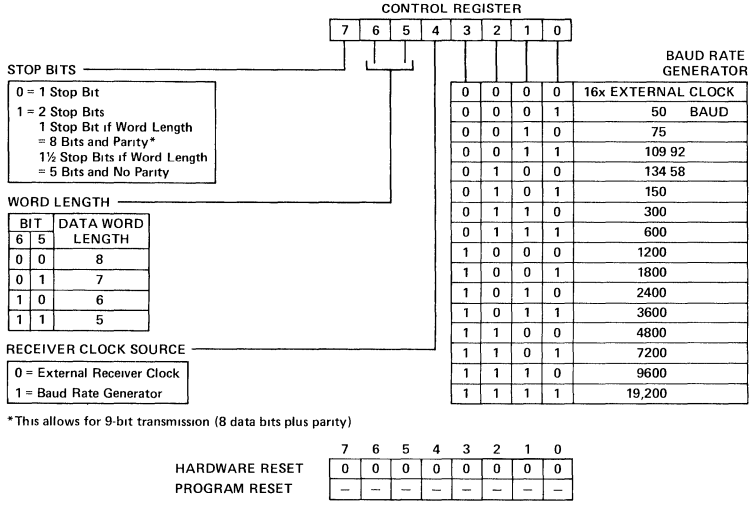


Figure 6. Control Register Format

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

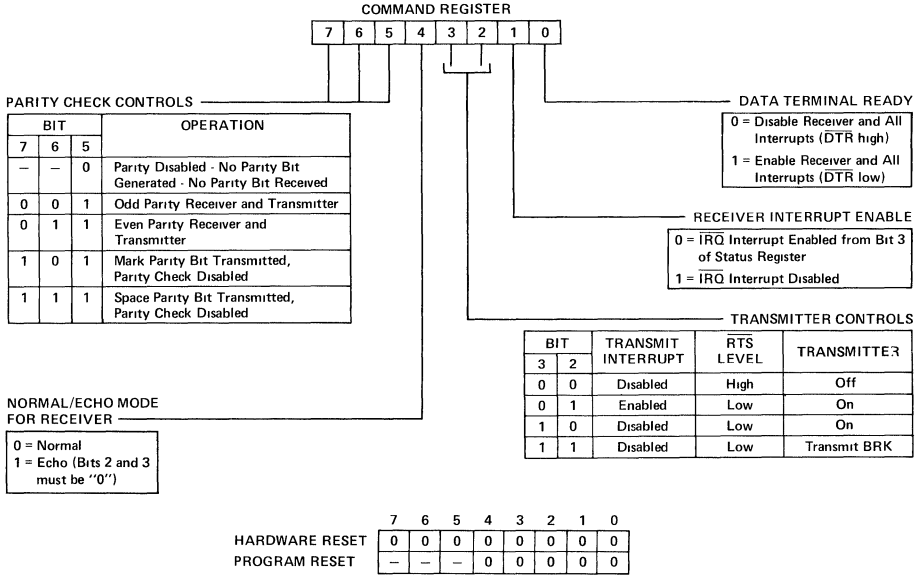
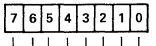


Figure 7. Command Register Format

Status Register

The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.



STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	0 = $\overline{DSR}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Figure 8. Status Register Format

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

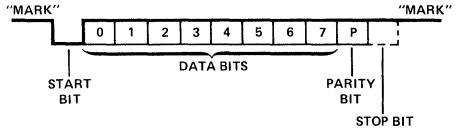


Figure 9. Serial Data Stream Example

Package Availability 28 Pin Molded DIP

Ordering Information

Part No.	Package	Clock Rate
SYP6551	Molded DIP	1 MHz
SYP6551A	Molded DIP	2 MHz

Synertek.

SY65C02
CMOS 8-Bit Microprocessor Family

PRELIMINARY

Features

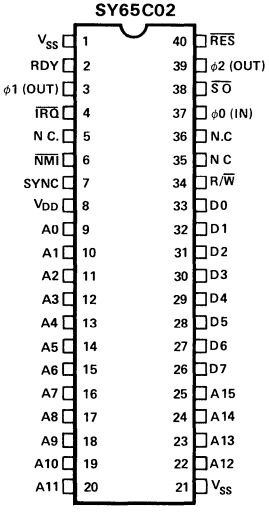
- High Performance n-Well HCMOS Family of Microprocessors
- Low Power Consumption, 4 mA at 1 MHz, 10 μA in Standby Operation Allowing Battery Operation
- Pin and Software Compatible with the NMOS 6500
- Improved Software Performance
  - 27 New Operation Codes
  - 15 Addressing Modes
  - 66 Microprocessor Instructions
  - 178 Total Operation Codes
- External or On-Board Clock Generation
  - On-Board Clock Generator can be Driven by an External Single-Phase Clock Input, an RC Network, or a Crystal Circuit
- 1,2,3 or 4 MHz Operation
- Advanced Memory Access Timing Option
  - Early Address Valid Allows High Speed Microprocessor Use with Slow Memories
  - Early Write Data for Dynamic Memories
- Decimal and Binary Arithmetic
- Programmable Stack Pointer
- Variable Length Stack
- Improved Operational Capabilities

Description

The CMOS 65C02 microprocessor is compatible with the NMOS 6500 family of microprocessors This 8-bit microprocessor unit designed in Synertek's proprietary high performance N-well silicon gate technology offers higher performance than the original NMOS 6502 The design allows for operating frequencies up to 4 MHz, and below 1 MHz further reducing its already low power consumption

Not only is the 65C02 a low power version of the popular 6500 microprocessor, it also has these new features Ability to tri-state the R/W line, address and data bus for DMA applications Improved T_{ACC} specs allowing use with slower memory devices A new optional output enhancing multiprocessing capabilityies Two new addressing modes, an a larger instruction set providing the user with more compact programming capabilities

Pin Configuration



Block Diagram

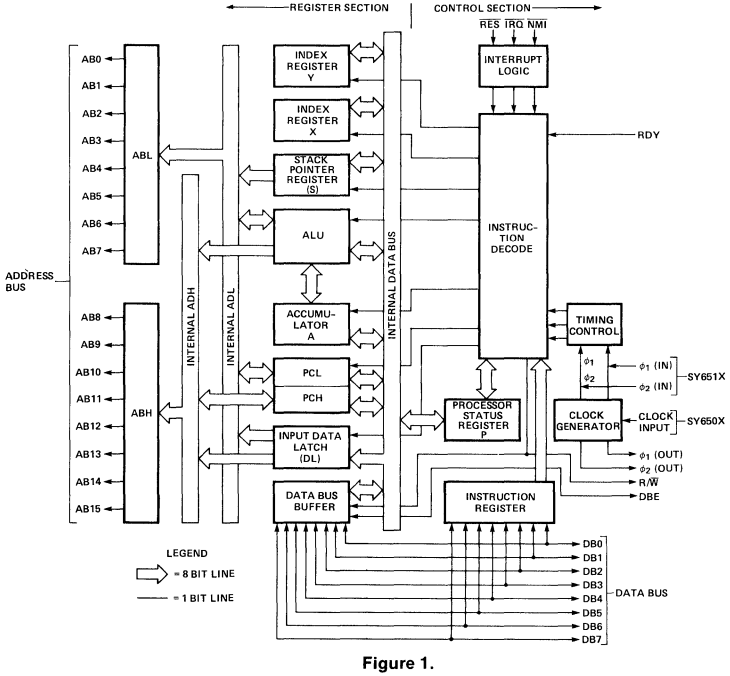


Figure 1.

MICRO-PROCESSORS

Absolute Maximum Ratings

(V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0° C to 70° C)

Supply Voltage (V_{DD}) ..... −0.3 to +7.0V
Input Voltage (V_{IN}) ..... −0.3 to +7.0V
Operating Temperature (T_A) ..... 0° C to +70° C
Storage Temperature (T_{STG}) ..... −55° C to +150° C

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied

Pin Function

Pin	Function
A_0-A_{15}	Address Bus
D_0-D_7	Data Bus
$\overline{IRQ}$*	Interrupt Request
RDY*	Ready
$\overline{ML}$	Memory Lock
$\overline{NMI}$*	Non-Maskable Interrupt
SYNC	Synchronize
$\overline{RES}$*	Reset

Pin	Function
$\overline{SO}$*	Set Overflow
NC	No Connection
R/$\overline{W}$	Read/Write
V_{DD}	Power Supply (+5V)
V_{SS}	Internal Logic Ground
ϕ_0	Clock Input
ϕ_1, ϕ_2	Clock Output

*This pin has an optional internal pullup for a No Connect condition

DC Characteristics

	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage					
ϕ_0 (IN)	V_{IH}	V_{SS} + 2.4	—	V_{DD}	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		V_{SS} + 2.0	—	—	V
Input Low Voltage					
ϕ_0 (IN)	V_{IL}	V_{SS} − 0.3	—	V_{SS} + 0.4	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		—	—	V_{SS} + 0.8	V
Input Leakage Current (V_{IN} = 0 to 5.25V, V_{DD} = 5.25V)	I_{IN}				
With Pullups		−30	—	+10	μA
Without Pullups		—	—	+1.0	μA
Three State (Off State) Input Current (V_{IN} = 0.4 to 2.4V, V_{CC} = 5.25V)					
Data Lines	I_{TSI}	—	—	10	μA
Output High Voltage (I_{OH} = −100 μAdc, V_{DD} = 4.75V, SYNC, Data, A_0-A_{15}, R/W)	V_{OH}	V_{SS} + 2.4	—	—	V
Output Low Voltage (I_{OL} = 1.6 mAdc, V_{DD} = 4.75V, SYNC, Data, A_0-A_{15}, R/W)	V_{OL}	—	—	V_{SS} + 0.4	V
Supply Current f = 1 MHz	I_{DD}	—	—	4	mA
Supply Current f =2 MHz	I_{DD}	—	—	8	mA
Capacitance	C				pF
(V_{IN} = 0, T_A = 25° C, f = 1 MHz)					
Logic	C_{IN}	—	—	5	
Data		—	—	10	
A_0-A_{15}, R/W, SYNC	C_{OUT}	—	—	10	
ϕ_0 (IN)	$C\phi_0$ (IN)	—	—	10	

Microprocessor Operational Enhancements

Function	NMOS 6502 Microprocessor	SY65C02 Microprocessor
Indexed addressing across page boundary	Extra read of invalid address	Extra read of last instruction byte
Execution of invalid op codes	Some terminate only by reset Results are undefined	All are NOPs (reserved for future use) Op Code — Bytes — Cycles X2 — 2 — 2 X3, X7, XB, XF — 1 — 1 44 — 2 — 3 54, D4, F4 — 2 — 4 5C — 3 — 8 DC, FC — 3 — 4
Jump indirect, operand = XXFF	Page address does not increment	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address	One read and two write cycles	Two read and one write cycle
Decimal flag	Indeterminate after reset	Initialized to binary mode (D = 0) after reset and interrupts
Flags after decimal operation	Invalid N, V and Z flags	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction	Interrupt vector is loaded, BRK vector is ignored	BRK is executed, then interrupt is executed

Microprocessor Hardware Enhancements

Function	NMOS 6502	SY65C02
Assertion of Ready RDY during write operations	Ignored	Stops processor during ϕ_2
Unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, $\overline{SO}$)	Must be connected to low impedance signal to avoid noise problems	Connected internally by a high-resistance to V_{DD} (approximately 250K ohm).

New Instruction Mnemonics

HEX	Mnemonic	Description
80	BRA	Branch relative always [Relative]
3A	DEA	Decrement accumulator [Accum]
1A	INA	Increment accumulator [Accum]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied]
7A	PLY	Pull Y from stack [Implied]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [Zero Page]
74	STZ	Store zero [ZPG, X]
1C	TRB	Test and reset memory bits with accumulator [Absolute]
14	TRB	Test and reset memory bits with accumulator [Zero page]
0C	TSB	Test and set memory bits with accumulator [Absolute]
04	TSB	Test and set memory bits with accumulator [Zero page]
89	BIT	Test immediate with accumulator [IMMEDIATE]

Additional Instruction Addressing Modes

HEX	Mnemonic	Description
72	ADC	Add memory to accumulator with carry [(ZPG)]
32	AND	"AND" memory with accumulator [(ZPG)]
3C	BIT	Test memory bits with accumulator[ABS, X]
34	BIT	Test memory bits with accumulator [ZPG, X]
D2	CMP	Compare memory and accumulator [(ZPG)]
52	EOR	"Exclusive OR" memory with accumulator [(ZPG)]
7C	JMP	Jump (New addressing mode) [ABS(IND, X)]
B2	LDA	Load accumulator with memory [(ZPG)]
12	ORA	"OR" memory with accumulator [(ZPG)]
F2	SBC	Subtract memory from accumulator with borrow [(ZPG)]
92	STA	Store accumulator in memory [(ZPG)]

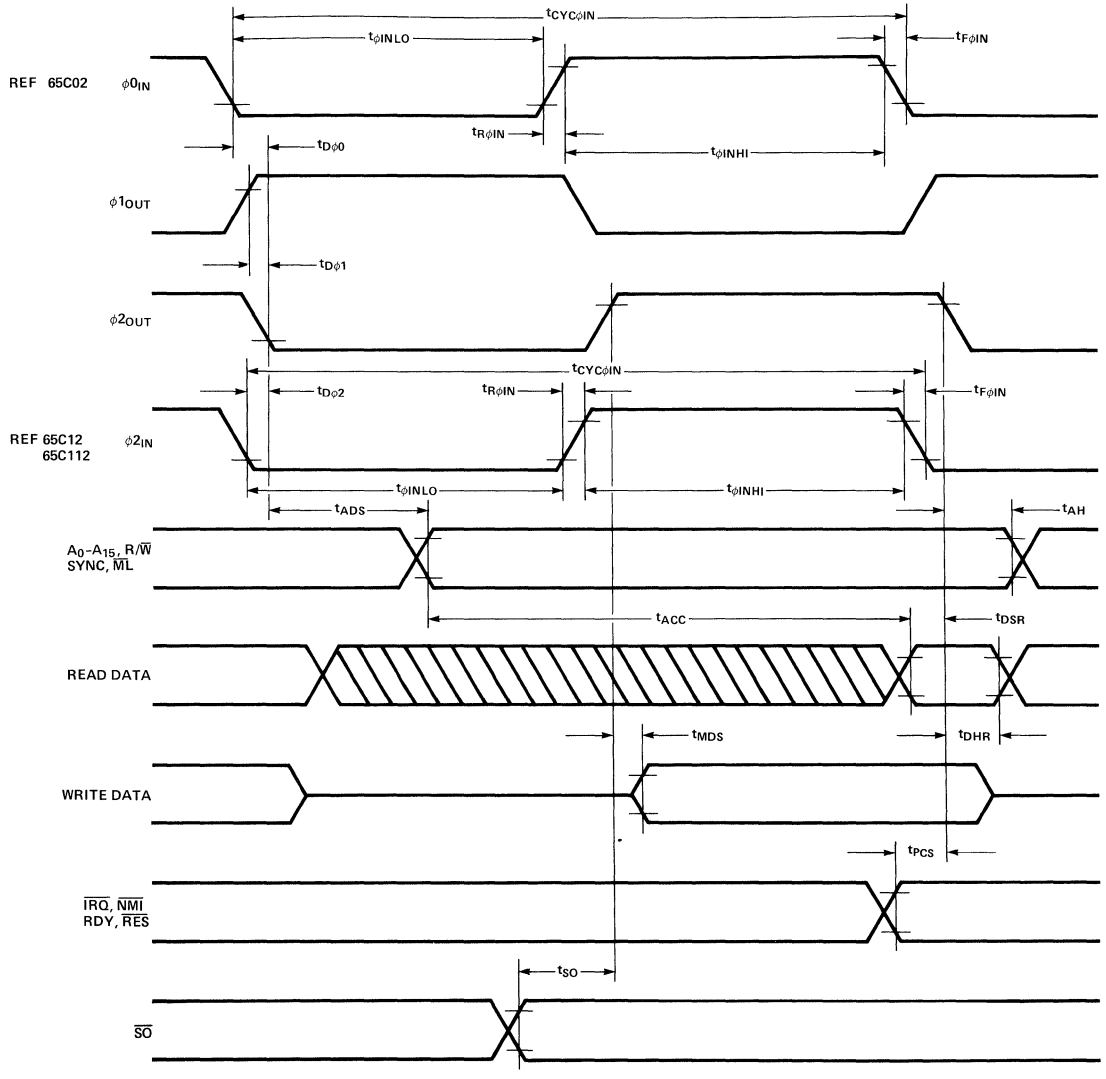


Figure 2. AC Characteristics, SY65C02

AC Characteristics, SY65C02 $V_{DD} = 5.0\ V \pm 5\%$, $T_A = -40°C$ to $+85°C$

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Delay Time, $\phi 0$ (IN) to $\phi 2$ (OUT)	$t_{D\phi 0}$	—	100	—	100	—	100	—	100	ns
Delay Time, $\phi 2$ (IN) to $\phi 2$ (OUT)	$t_{D\phi 2}$	—	75	—	75	—	75	—	75	ns
Delay Time, $\phi 1$ (OUT) to $\phi 2$ (OUT)	$t_{D\phi 1}$	—	50	—	50	—	50	—	50	ns
Cycle Time	$t_{CYC\phi IN}$	1.0	DC	0.50	DC	0.33	DC	0.25	DC	μs
Clock Pulse Width Low	$t_{PW(\phi)INLO}$	470	—	240	—	160	—	115	—	ns
Clock Pulse Width High	$t_{PW(\phi)INHI}$	470	—	240	—	160	—	115	—	ns
Fall Time, Rise Time	$t_{F\phi IN}$, $t_{R\phi IN}$	—	25	—	25	—	15	—	15	ns
Address Hold Time	t_{AH}	30	—	30	—	15	—	10	—	ns
Address Setup Time	t_{ADS}	—	225	—	140	—	110	—	90	ns
Access Time	t_{ACC}	650	—	310	—	170	—	110	—	ns
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	ns
Read Data Setup Time	t_{DSR}	100	—	50	—	50	—	50	—	ns
Write Data Delay Time	t_{MDS}	—	175	—	100	—	75	—	70	ns
Write Data Hold Time	t_{DHW}	30	—	30	—	30	—	30	—	ns
$\overline{SO}$ Setup Time	t_{SO}	100	—	50	—	35	—	25	—	ns
Processor Control Setup Time	t_{PCS}	200	—	200	—	150	—	120	—	ns

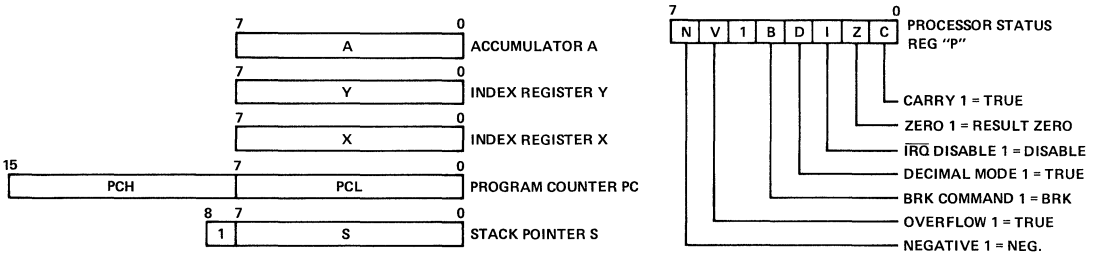


Figure 4. Microprocessor Programming Model

Functional Description

Timing Control

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation Pre-or post-indexing of indirect addresses is possible (see addressing modes).

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur

Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags (see microprocessor programming model).

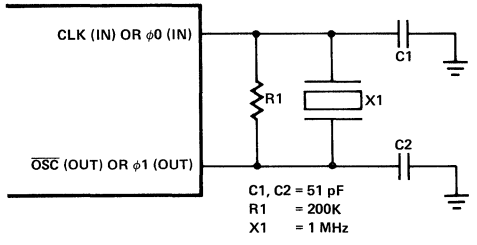


Figure 5 (a). Crystal Circuit for Internal Oscillator

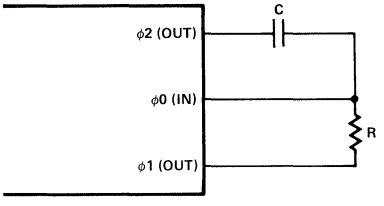


Figure 5 (b). Suggested RC Network Configuration for Internal Oscillator

Addressing Modes

Fifteen addressing modes are available to the user of the SY65C02 microprocessor The addressing modes are described in the following paragraphs

Implied Addressing (Implied)
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction

Accumulator Addressing (Accum)
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator

Immediate Addressing (Immediate)
With immediate addressing, the operand is contained in the second byte of the instruction, no further memory addressing is required

Absolute Addressing (Absolute)
For absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits Therefore, this addressing mode allows access to the total 64K bytes of addressable memory

Zero Page Addressing (Zero Page)
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte The careful use of zero page addressing can result in significant increase in code efficiency

Absolute Indexed Addressing (ABS, X or ABS, Y)
Absolute indexed addressing is used in conjunction with X or Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction This mode allows the index register to contain the index or count value and the instruction to contain the base address This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time

Zero Page Indexed Addressing (ZPG, X or ZPG, Y)
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or Zero Page, Y " The effective address is calculated by adding the second byte to the contents of the index register Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high-order eight bits of memory, and crossing of page boundaries does not occur

Relative Addressing (Relative)
Relative addressing is used only with branch instructions; it establishes a destination for the conditional branch. The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction The range of the offset is −128 to +127 bytes from the next instruction

Zero Page Indexed Indirect Addressing [(IND, X)]
With zero page indexed indirect addressing (usually referred to as indirect X) the second byte of the instruction is added to the contents of the X index register, the carry is discarded The result of this addition points to a memory location on page zero whose contents is the low-order eight bits of the effective address The next memory location in page zero contains the high-order eight bits of the effective address Both memory locations specifying the high- and low-order bytes of the effective address must be in page zero

***Absolute Indexed Indirect Addressing [ABS(IND, X)]**
(Jump Instruction Only)
With absolute indexed indirect addressing the contents of the second and third instruction bytes are added to the X register The result of this addition, points to a memory location containing the lower-order eight bits of the effective address The next memory location contains the higher-order eight bits of the effective address

Indirect Indexed Addressing [(IND), Y]
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

***Zero Page Indirect Addressing [(ZPG)]**
In the zero page indirect addressing mode, the second byte of the instruction points to a memory location on page zero containing the low-order byte of the effective address. The next location on page zero contains the high-order byte of the effective address

Absolute Indirect Addressing [(ABS)]
(Jump Instruction Only)
The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location is contained in the third byte of the instruction The contents of the fully specified memory location is the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address which is loaded into the 16 bit program counter

NOTE * = New Address Modes

Signal Description

Address Bus (A_0-A_{15})
A_0-A_{15} forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

Clocks (ϕ_0, ϕ_1, and ϕ_2)
ϕ_0 is a TTL level input that is used to generate the internal clocks in the 6502. Two full level output clocks are generated by the 6502. The ϕ_2 clock output is in phase with ϕ_0. The ϕ_1 output pin is 180° out of phase with ϕ_0. (See timing diagram.)

Data Bus (D_0-D_7)
The data lines (D_0-D_7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF.

Interrupt Request ($\overline{IRQ}$)
This TTL compatible input requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during ϕ_2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during ϕ_1. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further $\overline{IRQ}$s may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

Memory Lock ($\overline{ML}$)
In a multiprocessor system, the $\overline{ML}$ output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during ϕ_2; the current instruction is completed and the interrupt sequence begins during ϕ_1 The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

NOTE: Since this interrupt is non-maskable, another $\overline{NMI}$ can occur before the first is finished. Care should be taken when using $\overline{NMI}$ to avoid this.

Ready (RDY)
This input allows the user to single-cycle the microprocessor on all cycles including write cycles A negative transition to the low state, during or coincident with phase one (ϕ_1), will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ_2) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

Reset ($\overline{RES}$)
This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on $\overline{RES}$.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

Read/Write (R/$\overline{W}$)
This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location

Set Overflow ($\overline{SO}$)
A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of ϕ_1.

Synchronize (SYNC)
This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Instruction Set — Alphabetical Sequence

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift One Bit Left
BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Memory Bits with Accumulator
BMI Branch on Result Minus
BNE Branch on Result Not Zero
BPL Branch on Result Plus
• BRA Branch Always
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set
CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y
DEC Decrement by One
DEX Decrement Index X by One
DEY Decrement Index Y by One
EOR "Exclusive-or" Memory with Accumulator
INC Increment by One
INX Increment Index X by One
INY Increment Index Y by One
JMP Jump to New Location
JSR Jump to New Location Saving Return Address
LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right
NOP No Operation
ORA "OR" Memory with Accumulator
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
• PHX Push Index X on Stack
• PHY Push Index Y on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack
• PLX Pull Index X from Stack
• PLY Pull Index Y from Stack
ROL Rotate One Bit Left
ROR Rotate One Bit Right
RTI Return from Interrupt
RTS Return from Subroutine
SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Bit
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory
• STZ Store Zero in Memory
TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
• TRB Test and Reset Memory Bits with Accumulator
• TSB Test and Set Memory Bits with Accumulator
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Pointer
TYA Transfer Index Y to Accumulator

Note • = New Instruction

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			**TSB zpg**	ORA zpg	ASL zpg		PHP	ORA imm	ASL A		**TSB abs**	ORA abs	ASL abs		0
1	BPL rel	ORA ind, Y	**ORA ind**		**TRB zpg**	ORA zpg, X	ASL zpg, X		CLC	ORA abs, Y	**INC A**		**TRB abs**	ORA abs, X	ASL abs, X		1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg		PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs		2
3	BMI rel	AND ind, Y	**AND ind**		**BIT zpg,X**	AND zpg, X	ROL zpg, X		SEC	AND abs, Y	**DEC A**		**BIT abs,X**	AND abs, X	ROL abs, X		3
4	RTI	EOR ind, X				EOR zpg	LSR zpg		PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs		4
5	BVC rel	EOR ind, Y	**EOR ind**			EOR zpg, X	LSR zpg, X		CLI	EOR abs, Y	**PHY**			EOR abs, X	LSR abs, X		5
6	RTS	ADC ind, X			**STZ zpg**	ADC zpg	ROR zpg		PLA	ADC imm	ROR A		JMP ind	ADC abs	ROR abs		6
7	BVS rel	ADC ind, Y	**ADC ind**		**STZ zpg,X**	ADC zpg, X	ROR zpg, X		SEI	ADC abs, Y	**PLY**		**JMP ind,X**	ADC abs, X	ROR abs, X		7
8	**BRA rel**	STA ind, X			STY zpg	STA zpg	STX zpg		DEY	**BIT imm**	TXA		STY abs	STA abs	STX abs		8
9	BCC rel	STA ind, Y	**STA ind**		STY zpg, X	STA zpg, X	STX zpg, Y		TYA	STA abs, Y	TXS		**STZ abs**	STA abs, X	**STZ abs,X**		9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg		TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs		A
B	BCS rel	LDA ind, Y	**LDA ind**		LDY zpg, X	LDA zpg, X	LDX zpg, Y		CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y		B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg		INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs		C
D	BNE rel	CMP ind, Y	**CMP ind**			CMP zpg, X	DEC zpg, X		CLD	CMP abs, Y	**PHX**			CMP abs, X	DEC abs, X		D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg		INX	SBC imm	NOP		CPX abs	SBC abs	INC abs		E
F	BEQ rel	SBC ind, Y	**SBC ind**			SBC zpg, X	INC zpg, X		SED	SBC abs, Y	**PLX**			SBC abs, X	INC abs, X		F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note ■ = New Op Codes

Figure 6. Microprocessor Op Code Table

Operational Codes, Execution Time, and Memory Requirements

MNE	OPERATION		IMME-DIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM OP	n	#	IMPLIED OP	n	#	(IND, X) OP	n	#	(IND, Y) OP	n	#	ZPG, X OP	n	#	ZPG, Y OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#	RELATIVE OP	n	#	(ABS) OP	n	#	ABS (IND, X) OP	n	#	(ZPG) OP	n	#	PROCESSOR STATUS CODES 7 6 5 4 3 2 1 0 N V B D I Z C	MNE
ADC	A + M + C → A	(1,3)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2				7D	4	3	79	4	3											72	5	2	N V Z C	ADC
AND	A ∧ M → A	(1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2				3D	4	3	39	4	3											32	5	2	N Z	AND
ASL	C ← 7 ← 0 ← 0	(1)				OE	6	3	06	5	2	0A	2	1										16	6	2				1E	6	3														N Z C	ASL
BCC	Branch if C=0	(2)																																		90	2	2										BCC
BCS	Branch if C=1	(2)																																		B0	2	2										BCS
BEQ	Branch if Z=1	(2)																																		F0	2	2										BEQ
BIT	A ∧ M	(4)	89	2	2	2C	4	3	24	3	2													34	4	2				3C	4	3														M_7M_6 Z	BIT
BMI	Branch if N=1	(2)																																		30	2	2										BMI
BNE	Branch if Z=0	(2)																																		D0	2	2										BNE
BPL	Branch if N=0	(2)																																		10	2	2										BPL
BRA	Branch Always	(2)																																		80	2	2										BRA
BRK	Break														00	7	1																													1 1		BRK
BVC	Branch if V=0	(2)																																		50	2	2										BVC
BVS	Branch if V=1	(2)																																		70	2	2										BVS
CLC	0 → C														18	2	1																													0		CLC
CLD	0 → D														D8	2	1																													0		CLD
CLI	0 → I														58	2	1																													0		CLI
CLV	0 → V														B8	2	1																													0		CLV
CMP	A − M	(1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2				DD	4	3	D9	4	3											D2	5	2	N Z C	CMP
CPX	X − M		E0	2	2	EC	4	3	E4	3	2																																			N Z C	CPX
CPY	Y − M		C0	2	2	CC	4	3	C4	3	2																																			N Z C	CPY
DEA	A − 1 → A											3A	2	1																															N Z	DEA
DEC	M − 1 → M	(1)				CE	6	3	C6	5	2													D6	6	2				DE	6	3														N Z	DEC
DEX	X − 1 → X														CA	2	1																													N Z	DEX
DEY	Y − 1 → Y														88	2	1																													N Z	DEY
EOR	A ⊻ M → A		49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2				5D	4	3	59	4	3											52	5	2	N Z	EOR
INA	A + 1 → A											1A	2	1																															N Z	INA
INC	M + 1 → M	(1)				EE	6	3	E6	5	2													F6	6	2				FE	6	3														N Z	INC
INX	X + 1 → X														E8	2	1																													N Z	INX
INY	Y + 1 → Y														C8	2	1																													N Z	INY
JMP	Jump to new loc					4C	3	3																																	6C	6	3	7C	6	3				JMP
JSR	Jump Subroutine					20	6	3																																								JSR
LDA	M → A	(1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2				BD	4	3	B9	4	3											B2	5	2	N Z	LDA
LDX	M → X	(1)	A2	2	2	AE	4	3	A6	3	2																B6	4	2	BE	4	3														N Z	LDX
LDY	M → Y	(1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2				BC	4	3														N Z	LDY
LSR	0 → 7 → 0 → C	(1)				4E	6	3	46	5	2	4A	2	1										56	6	2				5E	6	3														0 Z C	LSR
NOP	PC + 1 → PC														EA	2	1																														NOP
ORA	A ∨ M → A	(1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2				1D	4	3	19	4	3											12	5	2	N Z	ORA
PHA	A → M_S S − 1 → S														48	3	1																														PHA
PHP	P → M_S S − 1 → S														08	3	1																														PHP
PHX	X → M_S S − 1 → S														DA	3	1																														PHX
PHY	Y → M_S S − 1 → S														5A	3	1																														PHY
PLA	S + 1 → S M_S → A														68	4	1																												N Z		PLA
PLP	S + 1 → S M_S → P														28	4	1																												N V 1 D I Z C		PLP
PLX	S + 1 → S M_S → X														FA	4	1																														PLX
PLY	S + 1 → S M_S → Y														7A	4	1																														PLY
ROL	C ← 7 ← 0 ← C	(1)				2E	6	3	26	5	2	2A	2	1										36	6	2				3E	6	3														N Z C		ROL
ROR	C → 7 → 0 → C	(1)				6E	6	3	66	5	2	6A	2	1										76	6	2				7E	6	3														N Z C		ROR
RTI	Return from Inter														40	6	1																													N V 1 D I Z C		RTI
RTS	Return from Subr														60	6	1																														RTS
SBC	A − M − $\overline{C}$ → A	(1,3)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2				FD	4	3	F9	4	3											F2	5	2	N V		SBC
SEC	1 → C														38	2	1																													1		SEC
SED	1 → D														F8	2	1																														SED
SEI	1 → I														78	2	1																														SEI
STA	A → M					8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2				9D	5	3	99	5	3											92	5	2			STA
STX	X → M					8E	4	3	86	3	2																96	4	2																		STX
STY	Y → M					8C	4	3	84	3	2													94	4	2																						STY
STZ	00 → M					9C	4	3	64	3	2													74	4	2				9E	5	3															STZ
TAX	A → X														AA	2	1																													N Z		TAX
TAY	A → Y														A8	2	1																													N Z		TAY
TRB	$\overline{A}$ ∧ M → M	(4)				1C	6	3	14	5	2																																			M_7M_6 Z		TRB
TSB	A ∨ M → M	(4)				0C	6	3	04	5	2																																			M_7M_6 Z		TSB
TSX	S → X														BA	2	1																													N Z		TSX
TXA	X → A														8A	2	1																													N Z		TXA
TXS	X → S														9A	2	1																															TXS
TYA	Y → A														98	2	1																													N Z		TYA

Notes

1. Add 1 to "n" if page boundary is crossed
2. Add 1 to "n" if branch occurs to same page
   Add 2 to "n" if branch occurs to different page
3. Add 1 to "n" if decimal mode.
4. V bit equals memory bit 6 prior to execution
   N bit equals memory bit 7 prior to execution

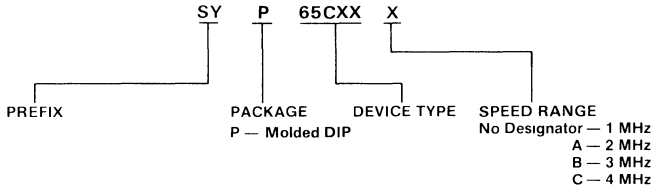
X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
− Subtract
∧ And
∨ Or
⊻ Exclusive or

n No. Cycles
No. Bytes
M_6 Memory bit 6
M_7 Memory bit 7

Package Availability 40 Pin Molded DIP

Ordering Information



Synertek.

SY65C22

CMOS Versatile Interface Adapter (VIA)

PRELIMINARY

Features

- Two 8-Bit Bi-directional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS Compatible Peripheral Port A Lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz, 2 MHz Bus Operation

Description

The SY65C22 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

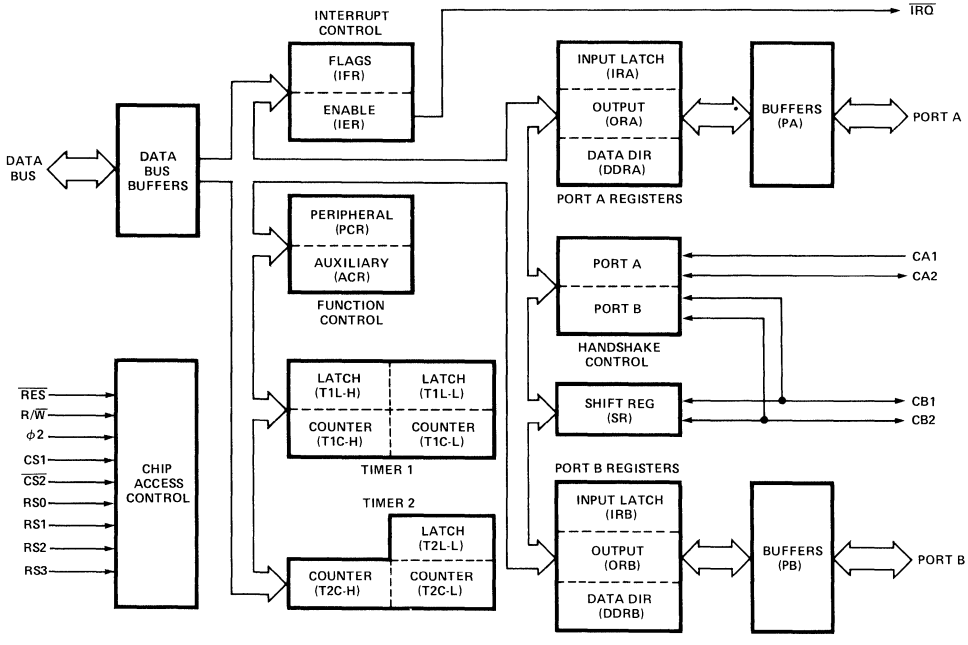


Figure 1. SY65C22 Block Diagram

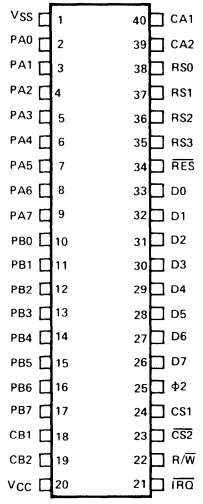
Absolute Maximum Ratings*

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0 3 to +7 0	V
Input Voltage	V_{IN}	-0 3 to V_{DD} +0 3	V
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Comment*

This device contains circuitry to protect the inputs against damage due to high static voltages However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages

Pin Configuration



Electrical Characteristics (V_{DD} = 5 0 V ± 10%, T_A = -40 to 85° C, unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2 4	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
I_{IN}	Input Leakage Current, V_{IN} = 0.4 to 2.4 V R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\Phi 2$	—	±1 0	μA
I_{TSI}	Off-state Input Current, V_{IN} = 0.4 to 2.4 V V_{CC} = Max., D0 to D7	—	±10 0	μA
I_{IH}	Input High Current, V_{IH} = 2 4 V PA0-PA7, CA2, PB0-PB7, CB1, CB2	-200	—	μA
I_{IL}	Input Low Current, V_{IL} = 0 4 V PA0-PA7, CA2, PB0-PB7, CB1, CB2	—	-2.4	mA
V_{OH}	Output High Voltage, V_{CC} = min, I_{LOAD} = —200 μA PA0-PA7, CA2, PB0-PB7, CB1, CB2	2.4	—	V
V_{OL}	Output Low Voltage, V_{CC} = min, I_{LOAD} = 3 2 mA	—	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 1 5 V (PB0-PB7)	-3.0	-10.0	mA
P_D	Power Dissipation, V_{DD} = 5.5 V, f = 1 MHz	—	11.0	mW
P_{SBY}	Standby Power Dissipation ($\phi 2$ = V_{IN}, Inputs = V_{SS} or V_{DD}, No Loads)	—	11.0	μW
I_{DD}	Supply Current f = 1 MHz f = 2 MHz	— —	2.0 4.0	mA mA
C_{OUT}	Output Capacitance, f = 1 MHz	—	10	pF
C_{IN}	Input Capacitance, f = 1 MHz	—	5.0	pF

Test Load

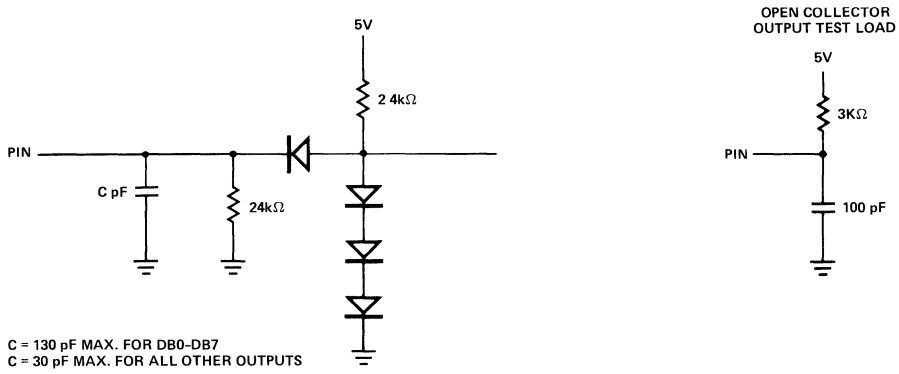


Figure 2. Test Load (for all Dynamic Parameters)

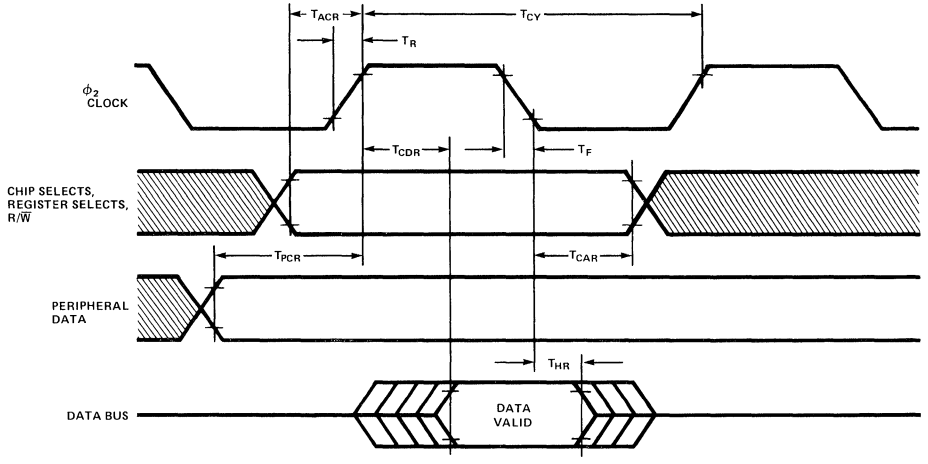


Figure 3. Read Timing Characteristics

AC Characteristics — Processor Interface Timing: V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = −40°C to +85°C

		65C22		65C22A		65C22B		
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	ns
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	ns
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	ns
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	ns
Read Timing (Figure 3)								
Select, R/$\overline{W}$ Set-Up	t_{ACR}	160	—	90	—	65	—	ns
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	ns
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	ns
Data Bus Hold	t_{HR}	10	—	10	—	10	—	ns
Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	ns

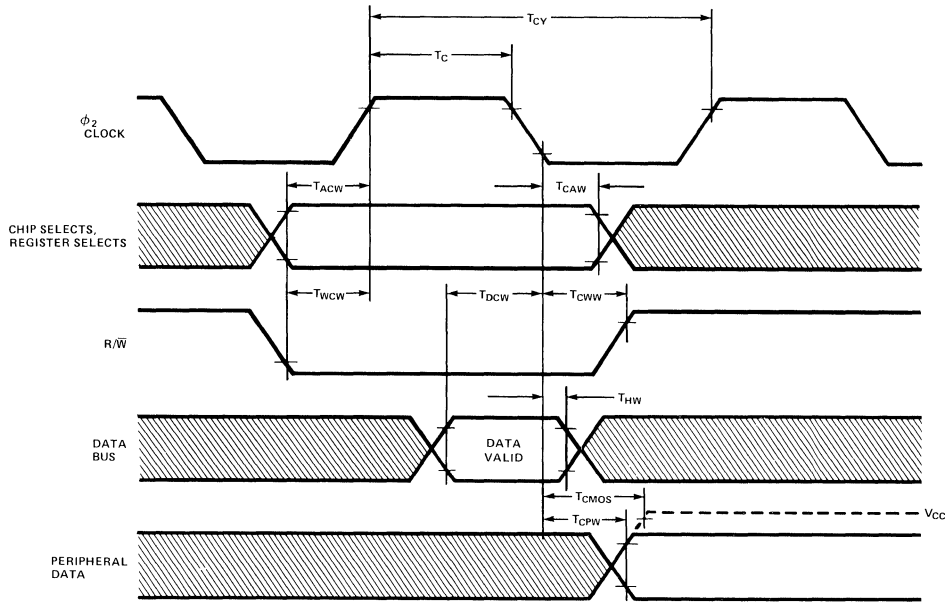


Figure 4. Write Timing Characteristics

AC Characteristics — Processor Interface Timing: V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = −40 to +85°C

		65C22		65C22A		65C22B		
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	ns
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	ns
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	ns
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	ns
Write Timing (Figure 4)								
Select, R/$\overline{W}$ Set-Up	t_{ACR}	160	—	90	—	65	—	ns
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	ns
Data Bus Setup	t_{DCW}	—	195	—	90	—	65	ns
Data Bus Hold	t_{HR}	10	—	10	—	10	—	ns
Peripheral Data Set-Up	t_{PCR}	—	1000	—	500	—	330	ns

MICRO-PROCESSORS

Peripheral Interface Characteristics

Symbol	Characteristic	Min.	Max.	Typ.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	—	1.0		μs	—
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	—	1.0		μs	5a, 5b
T_{RS}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	—	1.0		μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	—	2.0		μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0 05	1.0		μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1 5		μs	5c, 5d
T_{RS3}	Delay Time, Clock Transition to CA2 or CB2 Positive Transition (pulse mode)	—	1.0		μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	—	2.0		μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	—		ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	—		ns	5e
T_{SR1}	Shift-Out Delay Time — Time from ϕ_2 Falling Edge to CB2 Data Out	—	300		ns	5f
T_{SR2}	Shift-In Setup Time — Time from CB2 Data in to ϕ_2 Rising Edge	300	—		ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative to ϕ_2 Trailing Edge	100	T_{CY}		ns	5g
T_{IPW}	Pulse Width — PB6 Input Pulse	2 x T_{CY}	—			5i
T_{ICW}	Pulse Width — CB1 Input Clock	2 x T_{CY}	—			5h
T_{IPS}	Pulse Spacing — PB6 Input Pulse	2 x T_{CY}	—			5i
T_{ICS}	Pulse Spacing — CB1 Input Pulse	2 x T_{CY}	—			5h
T_{AL}	CA1, CB1 Set Up Prior to Transition to Arm Latch	T_C + 50	—		ns	5e
T_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	—		ns	5e
T_{PWI}	Set Up Required on CA1, CB1, CA2 or CB2 Prior to Triggering Edge	T_C + 50	—		ns	5j
	Shift Register Clock – Delay from ϕ_2					
T_{DPR}	to CB1 Rising Edge			200	ns	5k
T_{DPL}	to CB1 Falling Edge			125	ns	5k

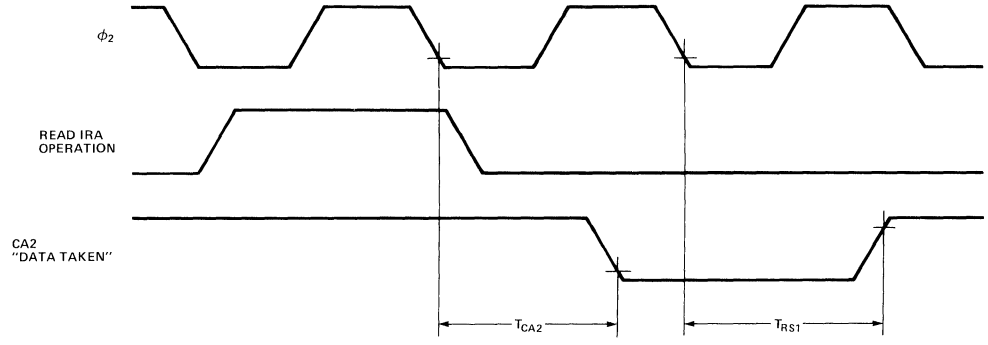


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

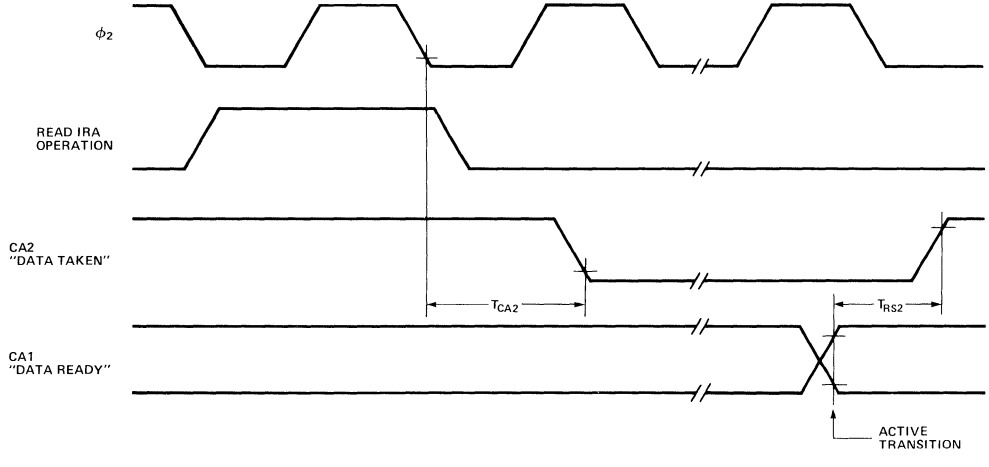


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

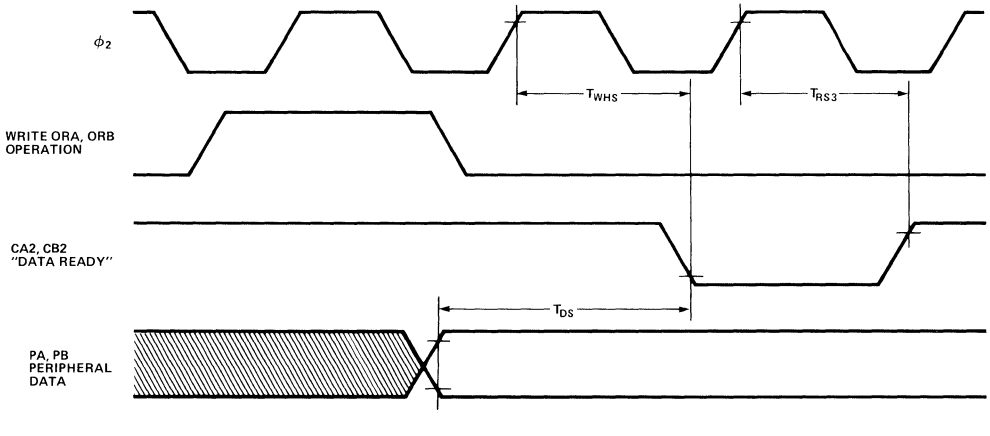


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

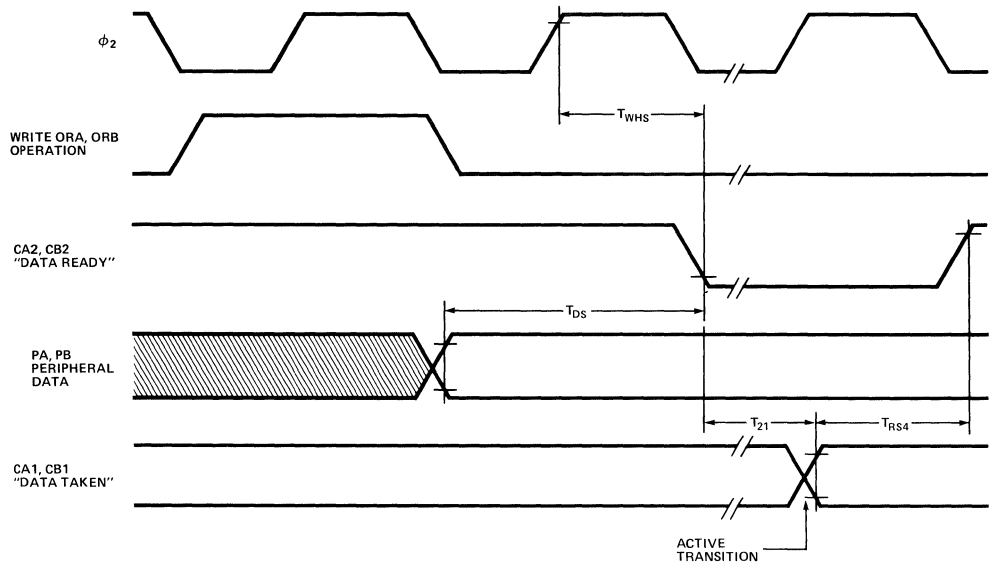


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

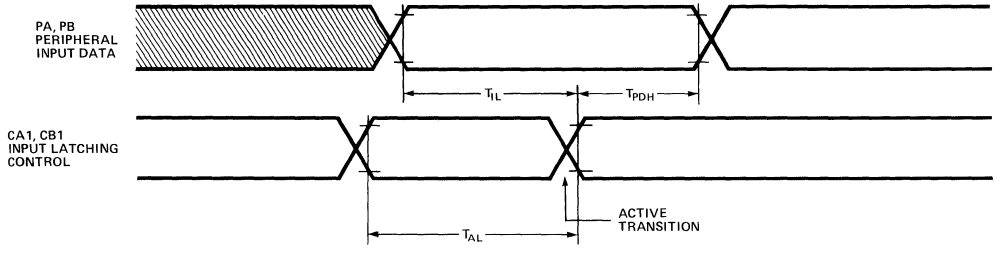


Figure 5e. Peripheral Data Input Latching Timing

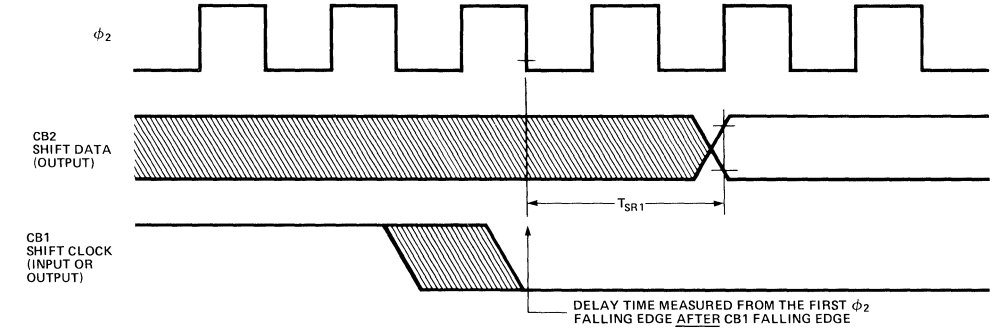


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

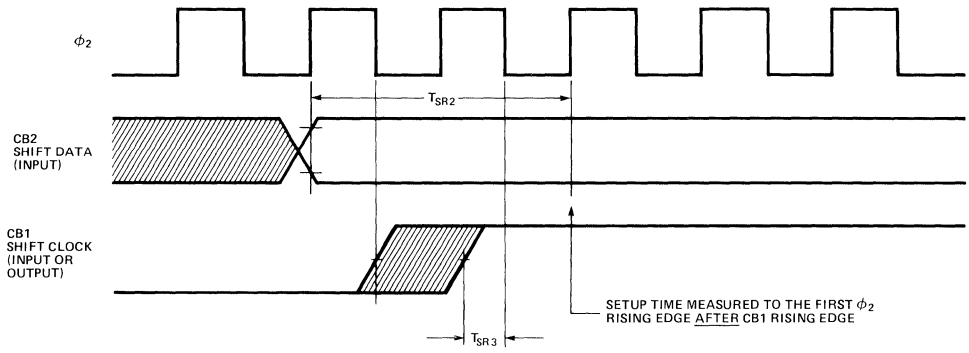


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

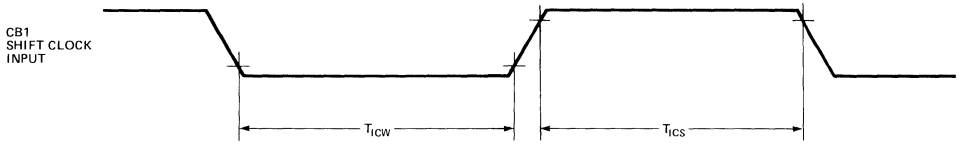


Figure 5h. External Shift Clock Timing

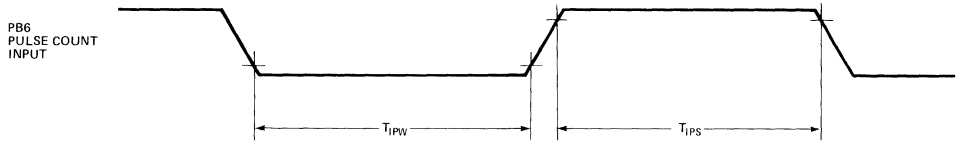


Figure 5i. Pulse Count Input Timing

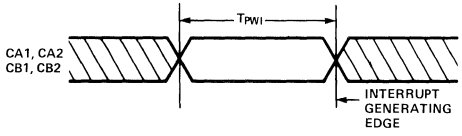


Figure 5j. Setup Time to Triggering Edge

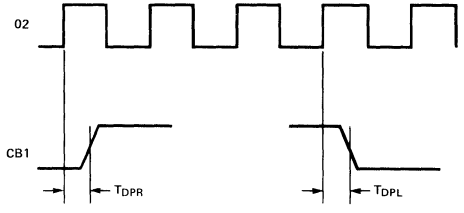


Figure 5k. Shift-in/out with Internal Clock Delay CD2 to CB1 Edge

Pin Descriptions

$\overline{RES}$ (Reset)
The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip

ϕ2 (Input Clock)
The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system processor and the SY65C22

R/$\overline{W}$ (Read/Write)
The direction of the data transfers between the SY65C22 and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected SY65C22 register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the SY65C22 (read operation).

DB0-DB7 (Data Bus)
The eight bi-directional data bus lines are used to transfer data between the SY65C22 and the system processor. During read cycles, the contents of the selected SY65C22 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the SY65C22 is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)
The two chip select inputs are normally connected to processor address lines either directly or through decoding The selected SY65C22 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

RS0-RS3 (Register Selects)
The four Register Select inputs permit the system processor to select one of the 16 internal registers of the SY65C22, as shown in Figure 6

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

Figure 6. SY65C22 Internal Register Summary

$\overline{IRQ}$ (Interrupt Request)
The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1 This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system

PA0-PA7 (Peripheral A Port)
The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line All of these modes of operation are controlled by the system processor through the internal control registers These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode Figure 7 illustrates the output circuit

CA1, CA2 (Peripheral A Control Lines)
The two Peripheral A control lines act as interrupt inputs or as handshake outputs Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines CA1 is a high-impedance input only, while CA2 represents one standard TTL load in the input mode CA2 will drive one standard TTL load in the output mode

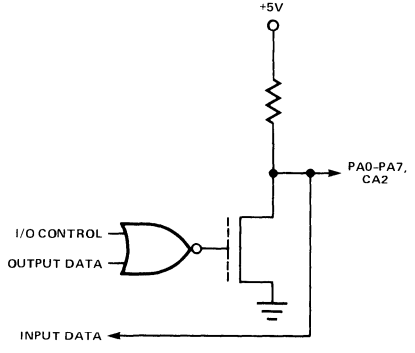


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)
The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode In addition, they are capable of sourcing 1 0 mA at 1 5 V DC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic

CB1, CB2 (Peripheral B Control Lines)
The Peripheral B control lines act as interrupt inputs or as handshake outputs As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits

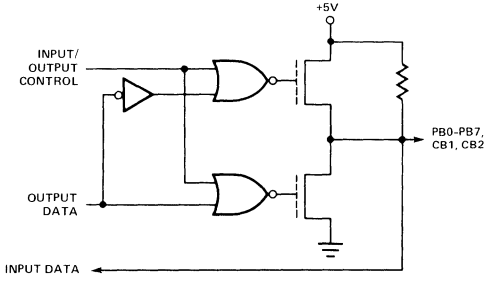


Figure 8. Peripheral B Port Output Circuit

Functional Description

Port A and Port B Operation
Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

When programmed as an output each peripheral pin is also controlled by a corresponding bit in the Output Register (ORA, ORB). A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are programmed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred on to the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled and the selected active transition on CA1 having

occurred, IRA will contain the data present on the PA lines at the time of the transition. Once IRA is read, however, it will appear transparent, reflecting the current state of the PA lines until the next "latching" transition.

The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10, and 11 illustrate the formats of the port registers In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

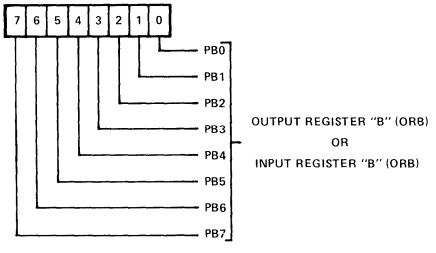
Handshake Control of Data Transfers

The SY65C22 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid

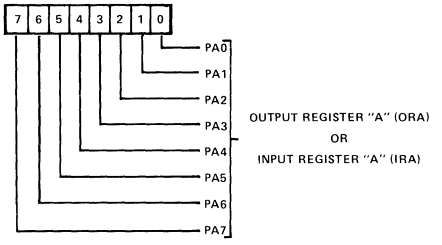
REG 0 – ORB/IRB



Pin Data Direction Selection	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB Pin level has no affect
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed	MPU reads input level on PB pin
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition

Figure 9. Output Register B (ORB), Input Register B (IRB)

REG 1 – ORA/IRA



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed	MPU reads level on PA pin
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)

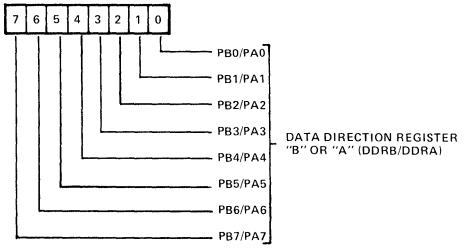


Figure 11. Data Direction Registers (DDRB, DDRA)

data is present on the peripheral port This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the SY65C22, automatic "Read" Handshaking is possible on the Peripheral A port only The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control The

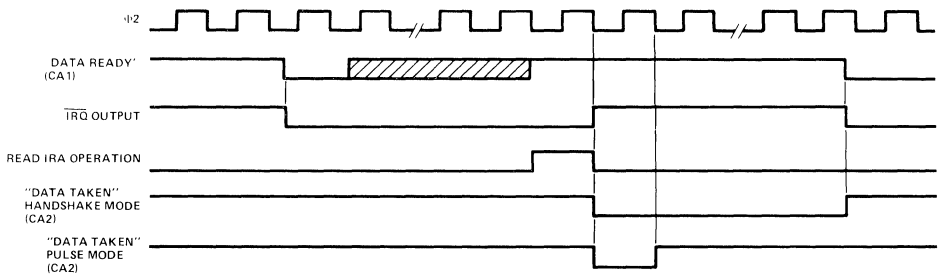


Figure 12. Read Handshake Timing (Port A Only)

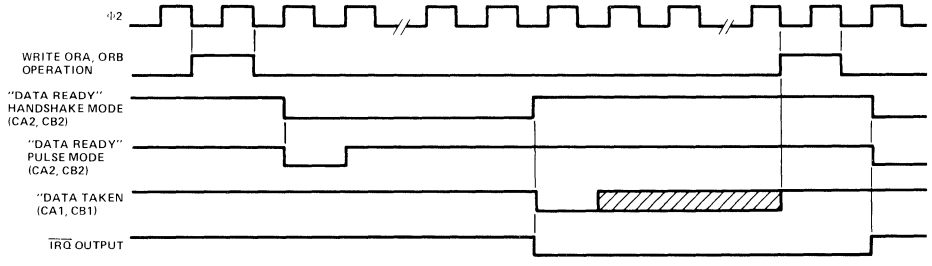


Figure 13. Write Handshake Timing

"Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking However, for Write Handshaking, the SY65C22 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal This can be accomplished on both the PA port and the PB port on the SY65C22 CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output This sequence is shown in Figure 13

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14)

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter The latches are used to store data which is to be loaded into the counter After loading, the counter decrements at $\phi 2$ clock rate Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low if the interrupt is enabled The timer will then disable any further interrupts, or (when programmed to) will automatically transfer the contents of the latches into the counter and begin to decrement again In addition, the timer may be programmed to invert the output signal on a peripheral pin each time it "times-out" Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes The four possible modes are depicted in Figure 17

REG 12 – PERIPHERAL CONTROL REGISTER

7	6	5	CB2 CONTROL
0	0	0	INPUT-NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE *
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT-POS EDGE *
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

CB1 INTERRUPT CONTROL

0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

3	2	1	CA2 CONTROL
0	0	0	INPUT NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT NEG EDGE *
0	1	0	INPUT POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT POS EDGE *
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

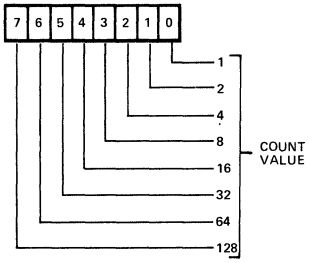
CA1 INTERRUPT CONTROL

0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

*SEE NOTE ACCOMPANYING FIGURE 25

Figure 14. CA1, CA2, CB1, CB2 Control

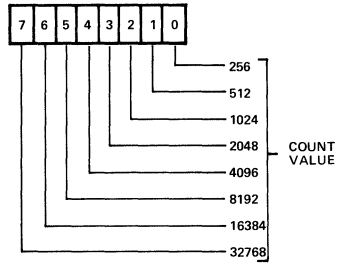
REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER)

REG 5 – TIMER 1 HIGH-ORDER COUNTER

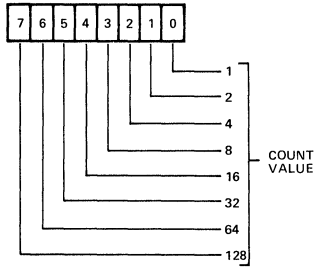


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER, AND INITIATES COUNTDOWN. T1 INTERRUPT FLAG ALSO IS RESET

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU

Figure 15. T1 Counter Registers

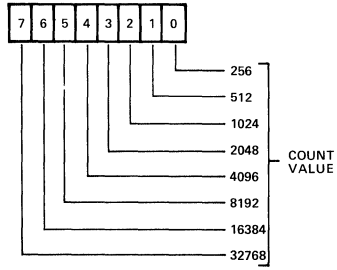
REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG

REG 7 – TIMER 1 HIGH-ORDER LATCHES

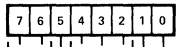


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU

Figure 16. T1 Latch Registers

REG 11 – AUXILIARY CONTROL REGISTER



LATCH ENABLE/DISABLE

0 = DISABLE 1 = ENABLE LATCHING

T1 TIMER CONTROL

7	6	OPERATION	PB7
0	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	DISABLED
0	1	CONTINUOUS INTERRUPTS	
1	0	TIMED INTERRUPT EACH TIME T1 IS LOADED	ONE-SHOT OUTPUT
1	1	CONTINUOUS INTERRUPTS	SQUARE WAVE OUTPUT

T2 TIMER CONTROL

5	OPERATION
0	TIMED INTERRUPT
1	COUNT DOWN WITH PULSES ON PB6

SHIFT REGISTER CONTROL

4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF 02
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF 02
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 17. Auxiliary Control Register

Note. The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

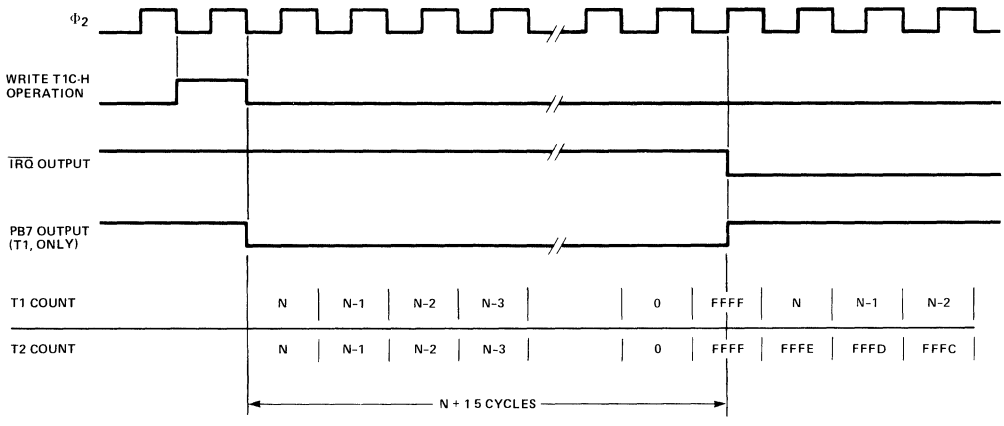


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each Timer load operation In addition, Timer 1 can be programmed to produce a single negative pulse on PB7

To generate a single interrupt ACR bits 6 and 7 must be 0 then either TIL-L or TIC-L must be written with the low-order count value (A write to TIC-L is effectively a Write to TIL-L) Next the high-order count value is written to TIC-H, (the value is simultaneously written into TIL-H), and TIL-L is transferred to TIC-L Countdown begins on the ϕ_2 following the write TIC-H and decrements at the ϕ_2 rate T1 interrupt occurs when the counters reach 0 Generation of a negative pulse on PB7 is done in the same manner except ACR bit 7 must be a one PB7 will go low after a Write TIC-H and go high again when the counters reach 0

The T1 interrupt flag is reset by either writing TIC-H (starting a new count) or by reading TIC-L.

Timing for the one-shot mode is illustrated in Figure 18

Timer 1 Free-Run Mode

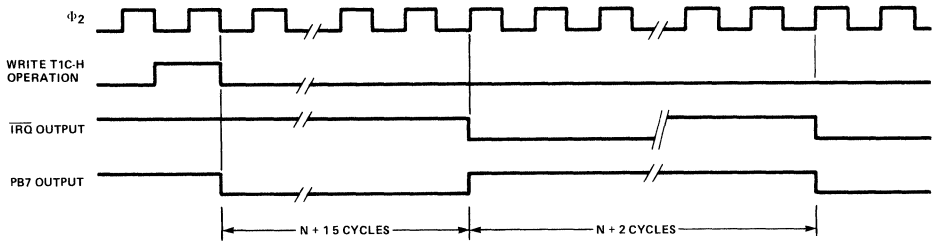
The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time This is accomplished in the "free-running" mode

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there, It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out The interrupt flag can be cleared by reading TIC-L, by writing directly into the flag as described later, or if a new count value is desired by a write to TIC-H.

All interval timers in the SY65C22 are "re-triggerable" Rewriting the counter will always re-initialize the time-out period In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period This capability is particularly valuable in the free-running mode with the output enabled In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7 In this manner, very complex waveforms can be generated Timing for the free-running mode is shown in Figure 19

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at Φ2 rate Figure 20 illustrates the T2 Counter Registers.



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 19. Timer 1 Free-Run Mode Timing

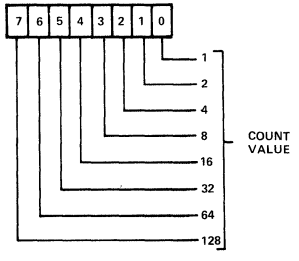
Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1, In this mode, T2 provides a single interrupt for each "write T2C-H" operation After timing out, (reading 0) the counters "roll-over" to all 1's ($FFFF_{16}$) and continue decrementing, allowing the user to read them and determine how long T2 interrupt has been set. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interruput flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations Timing for this mode is shown in Figure 21 The pulse must be low on the leading edge of Φ2

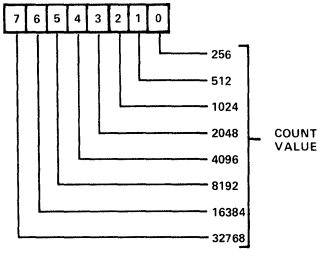
REG 8 – TIMER 2 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T2 LOW ORDER LATCHES

READ – 8 BITS FROM T2 LOW-ORDER COUNTER TRANSFERRED TO MPU T2 INTERRUPT FLAG IS RESET

REG 9 – TIMER 2 HIGH-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T2 HIGH ORDER COUNTER ALSO, LOW-ORDER LATCHES TRANSFERRED TO LOW-ORDER COUNTER IN ADDITION, T2 INTERRUPT FLAG IS RESET

READ – 8 BITS FROM T2 HIGH-ORDER COUNTER TRANSFERRED TO MPU

Figure 20. T2 Counter Registers

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the SY65C22 involves three principal operations These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the SY65C22, all interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

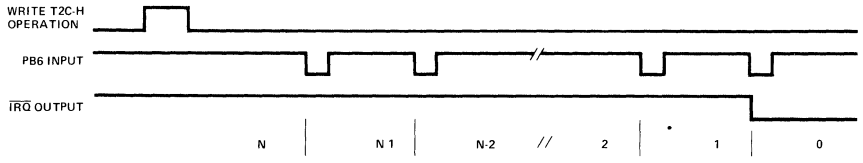
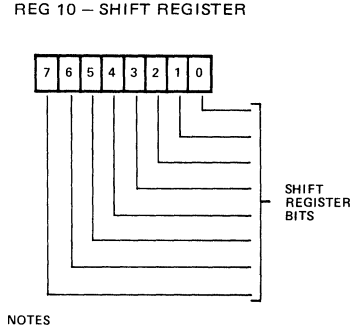
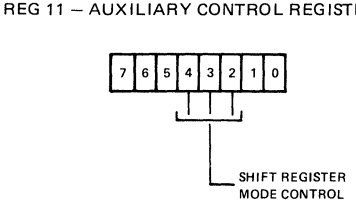


Figure 21. Timer 2 Pulse Counting Mode



NOTES
1 WHEN SHIFTING OUT BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0
2 WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7



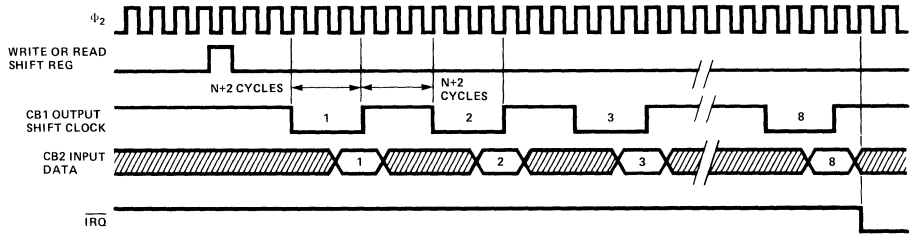
4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF ϕ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF ϕ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

Shift in Under Control of T2 (001)

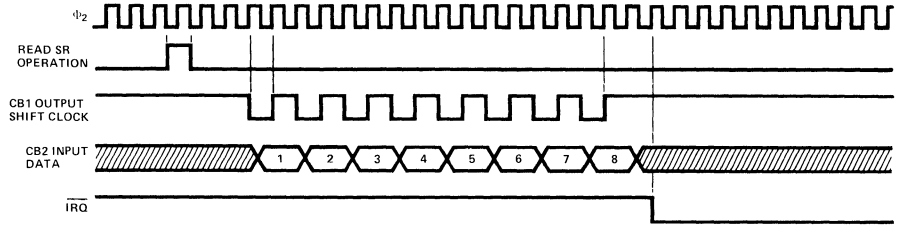
In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the ϕ_2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.



Shift in Under Control of ϕ_2 (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ_2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.



Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

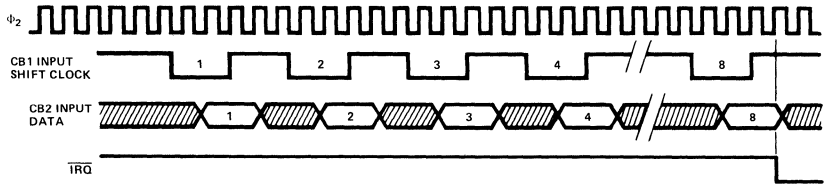
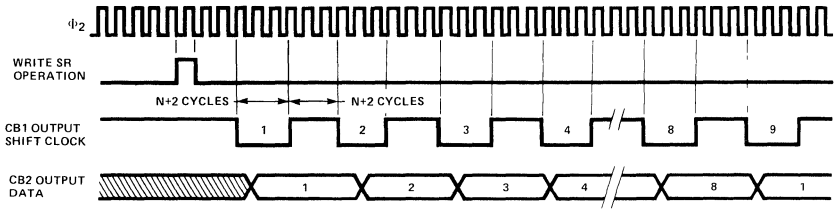


Figure 23. Shift Register Input Modes

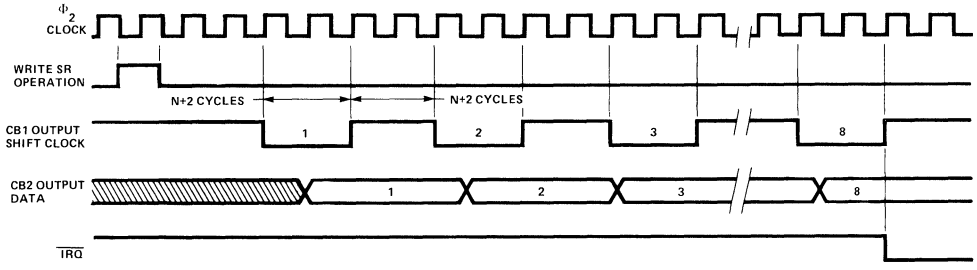
Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CR2 repetitively. In this mode the shift register counter is disabled and $\overline{IRQ}$ is never set.



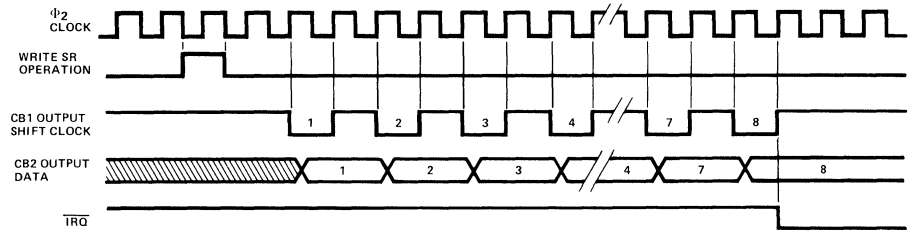
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of ϕ_2 (110)

In mode 110, the shift rate is controlled by the ϕ_2 system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

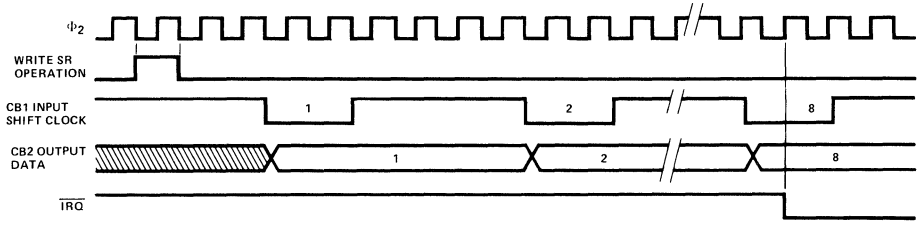


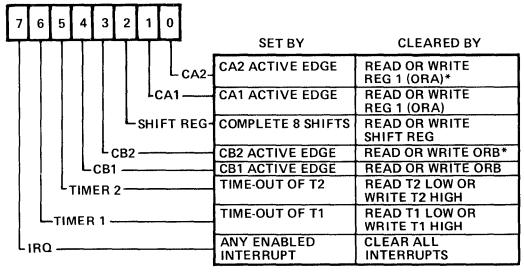
Figure 24. Shift Register Output Modes

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note X = logic AND, + = Logic OR.

The IFR bit 7 is not a flag Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

REG 13 – INTERRUPT FLAG REGISTER



	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY

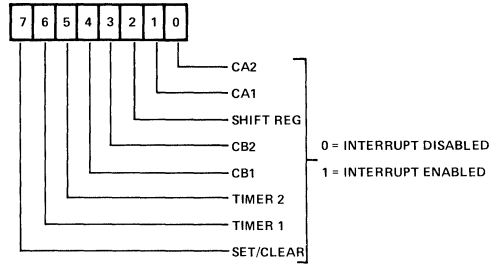
Figure 25. Interrupt Flag Register (IFR)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register, For each zero in bits 6 through 0, the corresponding bit is unaffected

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a logic 1.

REG 14 – INTERRUPT ENABLE REGISTER

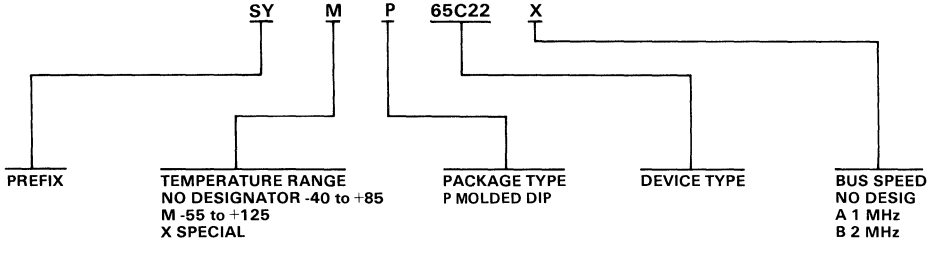


NOTES
1 IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT
2 IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT
3 IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE

Figure 26. Interrupt Enable Register (IER)

Package Availability 40 Pin Molded DIP

Ordering Information



Synertek.

SY65C51
CMOS Asynchronous Communication Interface Adapter

PRELIMINARY

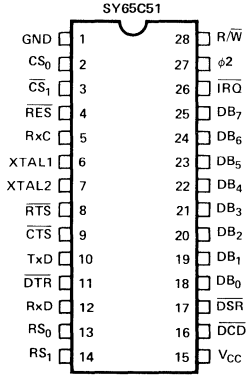
Features

- On-Chip Baud Rate Generator 15 Programmable Baud Rates Derived from a Standard 1 8432 MHz External Crystal (50 to 19,200 Baud)
- Programmable Interrupt and Status Register to Simplify Software Design
- Single Power Supply, 3 to 6 V_{DC}
- Serial Echo Mode
- False Start Bit Detection
- 8 Bit Bi-Directional Data Bus for Direct Communication with the Microprocessor
- External 16x Clock Input for Non-Standard Baud Rates (Up to 125 Kbaud)
- Programmable Word Lengths, Number of Stop Bits, and Parity Bit Generation and Detection
- Data Set and Modem Control Signals Provided
- Parity (Odd, Even, None, Mark, Space)
- Full-Duplex or Half Duplex Operation
- 5, 6, 7, 8 and 9 Bit Transmission
- Low Power Consumption
- 1, 2, 3, or 4 MHz MPU Bus Operation

Description

The SY65C51 is a CMOS Asynchronous Communications Adapter Its inherent low power requirements and noise immunity make it an ideal communications device for remote site monitoring installations, military, industrial and harsh environment applications. It was initially intended for interfacing the 6500 and 6800 microprocessors to serial communication data sets and modems, but is easily interfaced to all popular microprocessors A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required

Pin Configuration



Block Diagram

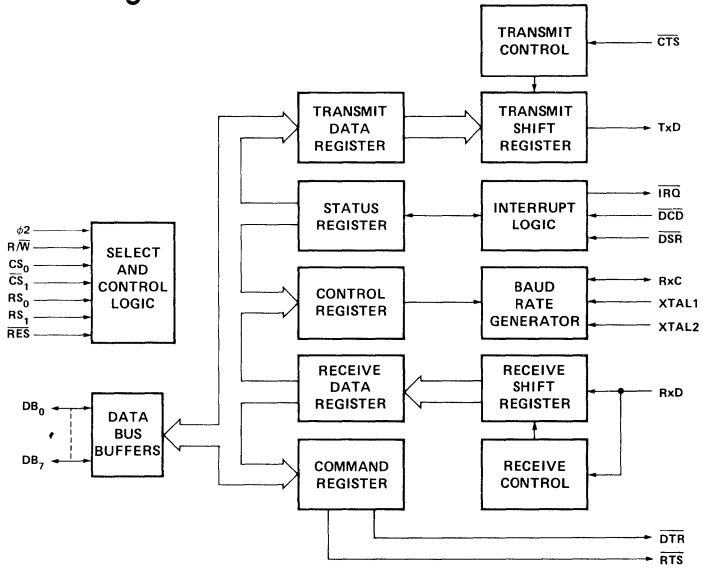


Figure 1. Block Diagram

MICRO-PROCESSORS

Absolute Maximum Ratings*

Rating	Symbol	Allowable Range
Supply Voltage	V_{DD}	-0.3 V to +7.0 V
Input/Output Voltage	V_{IN}	-0.3 V to +7.0 V
Operating Temperature	T_{OP}	0°C to +70°C
Storage Temperature	T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits

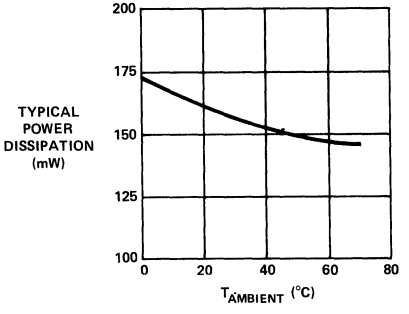
Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Characteristics (V_{DD} = 5.0 V ± 5%, T_A = −40 to +85°C, unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Input Leakage Current: V_{IN} = 0.4 to 2.4 V, V_{DD} = 5.25 V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	—		±1.0	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	—	—	±10.0	μA
Output High Voltage: I_{LOAD} = −200 μA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	—	—	V
Output Low Voltage: I_{OL} = 3.2 mA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	—	—	0.4	V
Supply Current (No Loads) f = 1 MHz	I_{DD}			2	mA
f = 2 MHz	I_{DD}			4	mA
Standby Power Dissipation (ϕ2 = V_{IN}, Inputs = V_{SS} or V_{DD}, No Loads, with Internal XTAL Feedback Disconnected	P_{SBY}	—	—	11	μW
Output Leakage Current (Off State): V_{OUT} = 5 V ($\overline{IRQ}$)	I_{OFF}	—	1.0	10.0	μA
Clock Capacitance (ϕ2)	C_{CLK}	—	—	20	pF
Input Capacitance (Except XTAL1 and XTAL2)	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	5.0	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} =	P_D	—	170	300	

Power Dissipation vs. Temperature



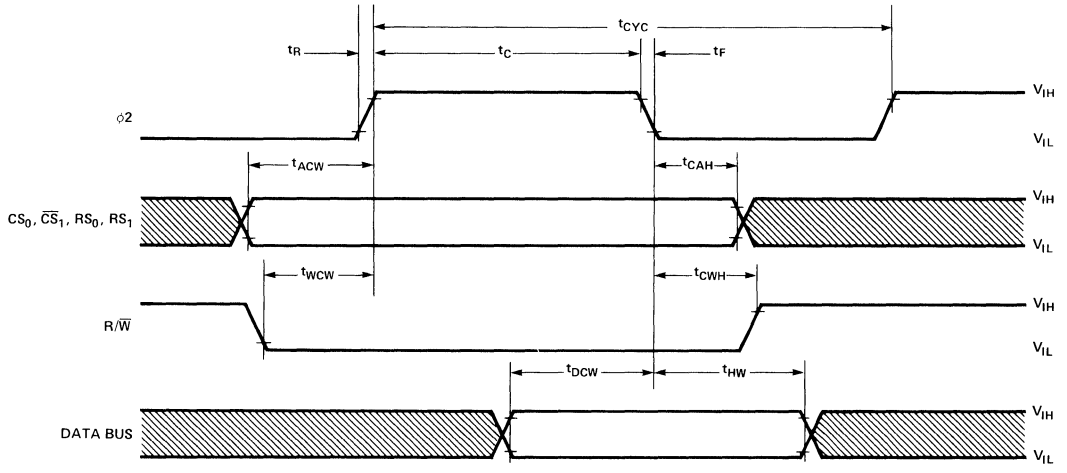


Figure 2. Write Timing Characteristics

Write Cycle (V_{DD} = 5.0 V ± 5%, T_A = −40 to +85° C, unless otherwise noted)

Characteristic	Symbol	SY65C51		SY65C51A		Unit
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYC}	1 0	—	0 5	—	μs
φ2 Pulse Width	t_C	470	—	240	—	ns
Address Set-Up Time	t_{ACW}	160	—	90	—	ns
Address Hold Time	t_{CAH}	0	—	0	—	ns
R/W Set-Up Time	t_{WCW}	160	—	90	—	ns
R/W Hold Time	t_{CWH}	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	195	—	90	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	ns

(t_R and t_F = 30 ns MAX)

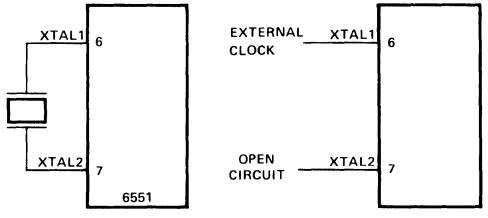
Crystal Specification

1. Temperature stability ± 0.01% (0° C to 70° C)
2. Characteristics at 25° C ± 2° C

a. Frequency (MHz)	1 8432
b. Frequency tolerance (±%)	0.02
c. Resonance mode	Series
d. Equivalent resistance (ohm)	400 max.
e. Drive level mW	2
f. Shunt capacitance pF	7 max
g. Oscillation mode	Fundamental

No other external components should be in the crystal circuit.

Clock Generation



INTERNAL CLOCK EXTERNAL CLOCK

MICRO-PROCESSORS

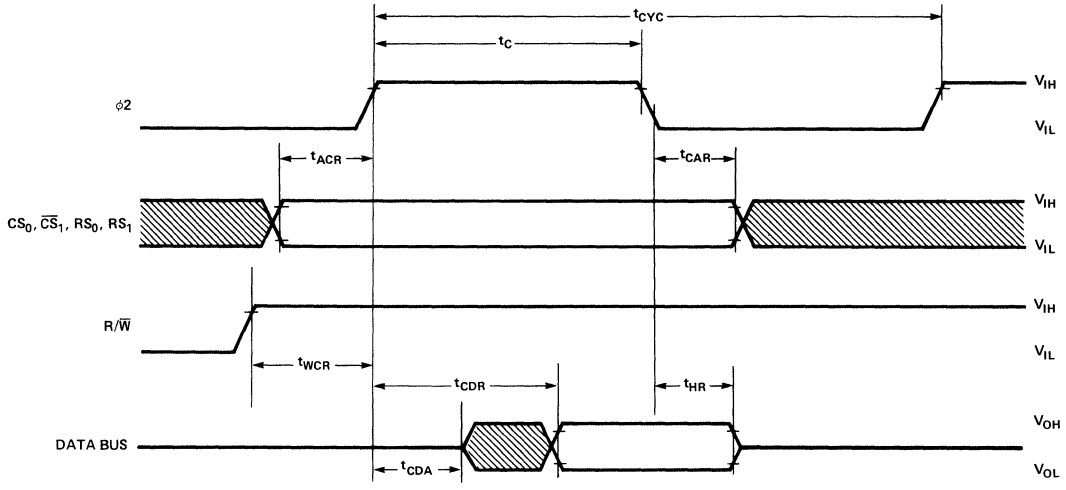
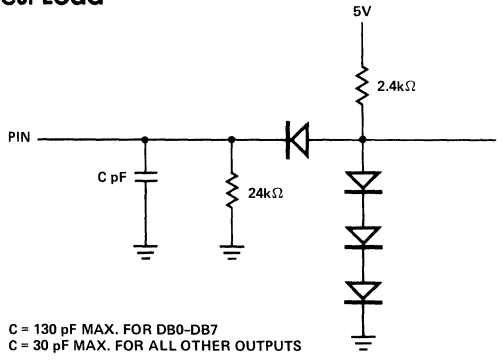


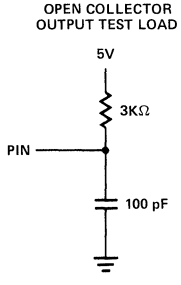
Figure 3. Read Timing Characteristics

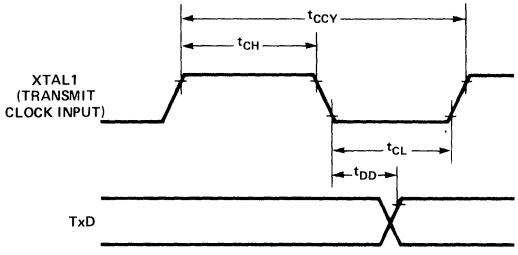
Read Cycle (V_{DD} = 5.0 V ± 5%, T_A = −40 to +85° C, unless otherwise noted)

Characteristic	Symbol	SY65C51 Min.	SY65C51 Max.	SY65C51A Min.	SY65C51A Max.	Unit
Cycle Time	t_{CYC}	1.0	—	0.5	—	μs
Pulse Width (φ2)	t_C	470	—	240	—	ns
Address Set-Up Time	t_{ACR}	160	—	90	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	ns
R/W Set-Up Time	t_{WCR}	160	—	90	—	ns
Read Access Time (Valid Data)	t_{CDR}	—	320	—	190	ns
Read Data Hold Time	t_{HR}	10	—	10	—	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	—	40	—	ns

Test Load







NOTE. TxD rate is 1/16 TxC rate.

Figure 4a. Transmit Timing with External Clock

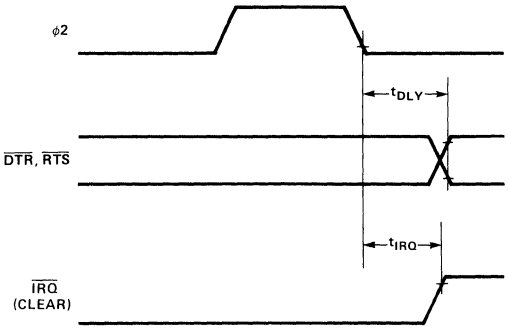
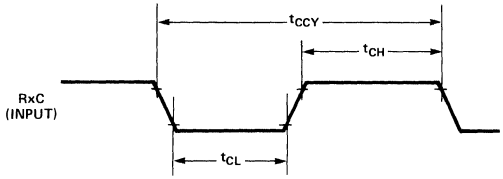


Figure 4b. Interrupt and Output Timing



NOTE RxD rate is 1/16 RxC rate.

Figure 4c. Receive External Clock Timing

Transmit/Receive Characteristics

Characteristic	Symbol	Min.	Max.	Unit
Transmit/Receive Clock Rate	t_{CCY}	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	ns
XTAL1 to TxD Propagation Delay	t_{DD}	—	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	ns

*The baud rate with external clocking is. Baud Rate $= \frac{1}{16 \times T_{CCY}}$

Interface Signal Description

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

ϕ2 (Input Clock)

The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the SY65C51.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY65C51. A low on the R/$\overline{W}$ pin allows a write to the SY65C51.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY65C51. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, $\overline{CS}_1$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The SY65C51 is selected when CS_0 is high and $\overline{CS}_1$ is low.

RS_0, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various SY65C51 internal registers. The following table indicates the internal register select coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the SY65C51 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the SY65C51 to the modem. A low on $\overline{DTR}$ indicates the SY65C51 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the SY65C51 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note. If Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the SY65C51 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note. If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Internal Organization

The Transmitter/Receiver sections of the SY65C51 are depicted by the block diagram in Figure 5.

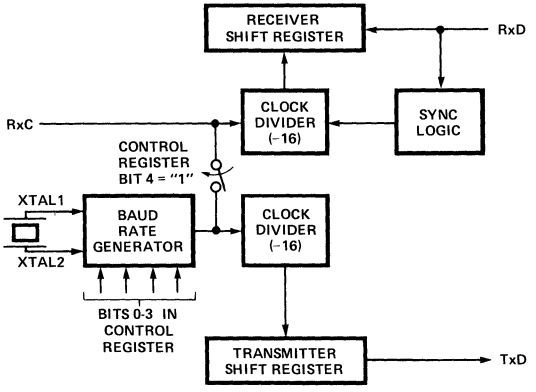


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the SY65C51.

Control Register

The Control Register is used to select the desired mode for the SY65C51. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

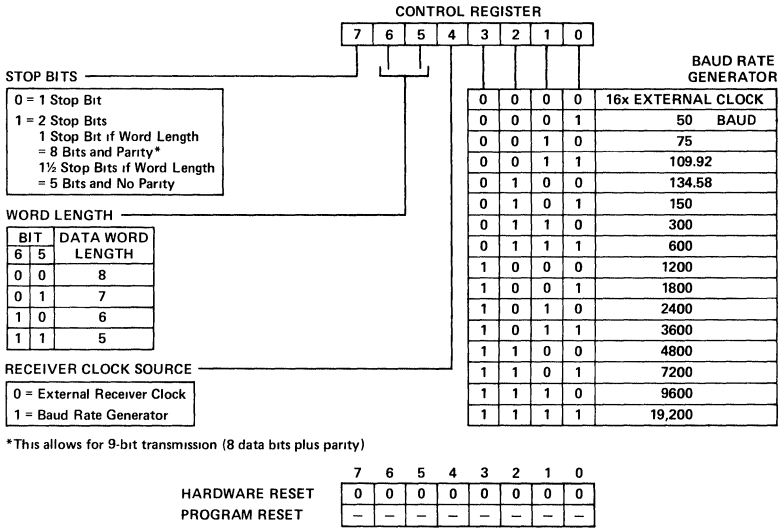


Figure 6. Control Register Format

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

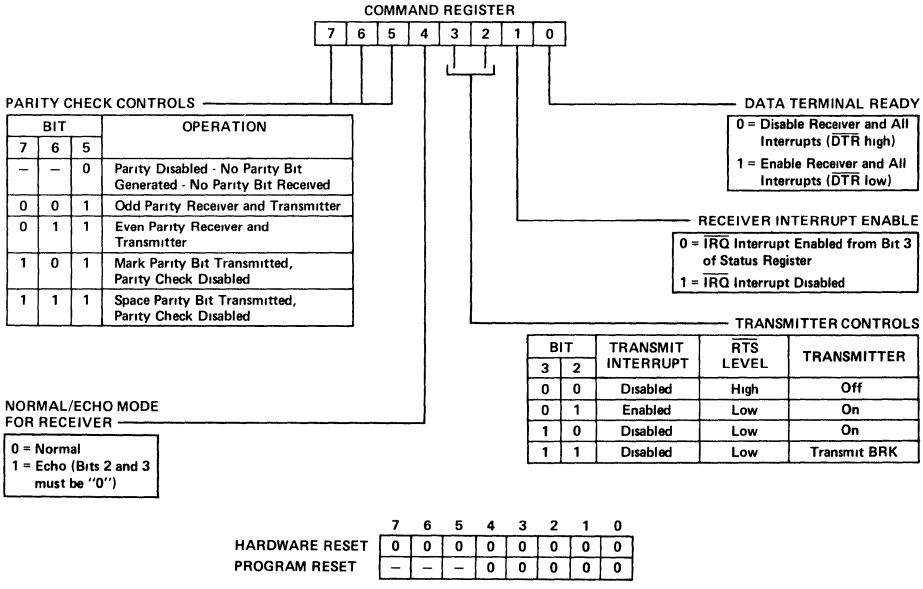


Figure 7. Command Register Format

Status Register

The Status Register is used to indicate to the processor the status of various SY65C51 functions and is outlined in Figure 8.

STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	0 = $\overline{DSR}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Figure 8. Status Register Format

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 65C51 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

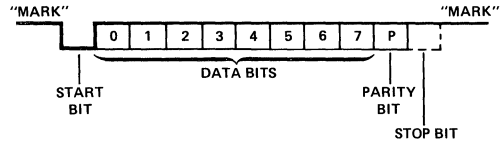
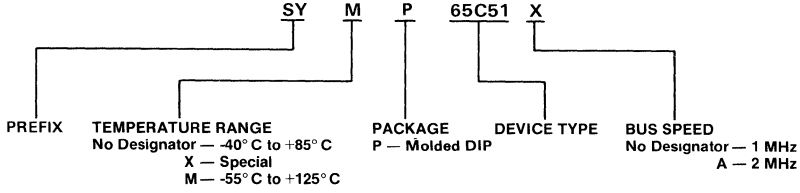


Figure 9. Serial Data Stream Example

Package Availability 28 Pin Molded DIP

Ordering Information



Synertek.

Z8601

Z8 Family of Single-Chip Microcomputers

Features

- Complete microcomputer with on-chip RAM, ROM and I/O
  - 128 bytes of on-chip RAM
  - 2K bytes of on-chip ROM
  - 32 I/O lines
- Two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler
- Full-duplex UART clocked by an internal timer
- 144-byte register file includes
  - 124 general-purpose registers, each of which can be used as an accumulator, index register, storage element, address register or part of the internal stack
  - Four I/O port registers
  - Sixteen status and control registers
- Register pointer permits shorter, faster instructions to access one of nine working-register groups
- Vectored, prioritized interrupts for I/O, counter/timers and UART
- Expandable bus interfaces up to 62K bytes each of external program memory and external data memory
- On-chip oscillator can be driven by a crystal, RC, LC or external clock source
- High-speed instruction execution
  - Working-register operations = 1 5 μs
  - Average instruction execution = 2 2 μs
  - Longest instruction = 5 μs
- Low-power standby mode retains contents of general-purpose registers
- Single +5 V supply
- All I/O pins TTL compatible

Description

The Z8 microcomputer introduces a new level of sophistication to single-chip architecture Compared to earlier single-chip microcomputers, the Z8 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output and bit-manipulation capabilities, and easier system expansion

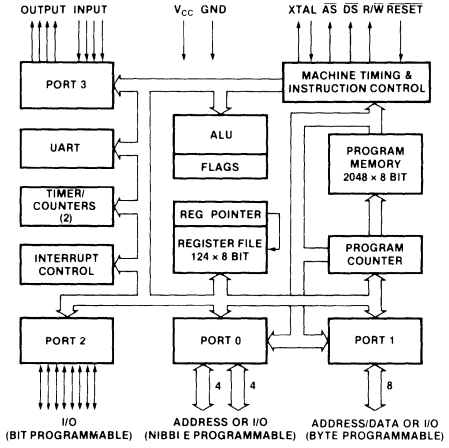


Figure 1. Block Diagram

Under program control, the Z8 can be tailored to the needs of its user It can be configured as a stand-alone microcomputer with 2K of internal ROM, a traditional microprocessor that manages up to 124K of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-Bus. In all configurations, a large number of pins remain available for I/O

Pin Description

$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$. *I/O Port Lines* (Input/Outputs, TTL compatible) These 32 lines are divided into four 8-bit I/O ports that can be configured under program control for I/O or external memory interface

$\overline{AS}$. *Address Strobe* (output, active Low) Address Strobe is pulsed once at the beginning of each machine cycle Addresses are output via Ports 0 and 1 for internal and external program fetches and external data memory transfers The addresses for all external program or data memory transfers are valid at the trailing edge of $\overline{AS}$ Under program control, $\overline{AS}$ can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe and Read/Write

$\overline{DS}$. *Data Strobe* (output, active Low) Data Strobe is activated once for each external memory transfer

R/$\overline{W}$. *Read/Write* (output) R/$\overline{W}$ is Low when the Z8 is writing to external program or data memory

*Z8 is a trademark of Zilog Inc

Pin Description (Cont.)

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-base input and output). These pins connect a series-resonant crystal (8 MHz maximum), LC network, RC network or an external single-phase clock (8 MHz maximum) to the on-chip clock oscillator and buffer.

$\overline{\text{RESET}}$. *Reset* (input, active Low). $\overline{\text{RESET}}$ initializes the Z8. When $\overline{\text{RESET}}$ is deactivated, the Z8 begins program execution from internal program location $000C_H$.

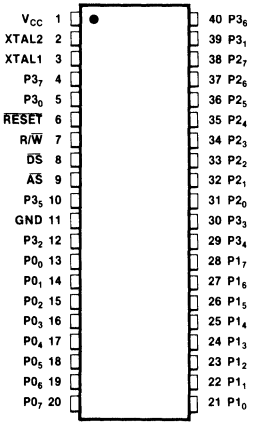


Figure 2. Pin Assignments

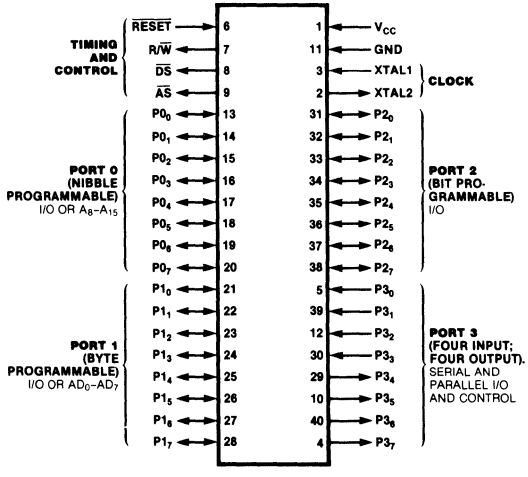


Figure 3. Pin Functions

Architecture

Z8 architecture is characterized by a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features that are helpful in many applications.

Microcomputer applications demand powerful I/O capabilities. The Z8 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

Because the multiplexed address/data bus is merged with the I/O-oriented ports, the Z8 can assume many different memory and I/O configurations. These configurations range from a self-contained microcomputer to a microprocessor that can address 120K of external memory

The Z8 offers three basic address spaces to support this wide range of configurations: program memory (internal and external), data memory (external) and the register file (internal). The 144-byte random-access register file is composed of 124 general-purpose registers, 4 I/O port registers, and 16 control and status registers.

To unburden the program from coping with real-time problems such as serial data communication and counting/timing, the Z8 offers an on-chip asynchronous receiver/transmitter (UART), and two counter/timers with a large number of user-selectable modes. Hardware support for the UART is minimized because one of the on-chip timers supplies the bit clock with selectable baud rates

Address Spaces

Program Memory. The 16-bit program counter addresses 64K bytes of program memory space. Program memory can be located in two areas: one internal and the other external (Figure 4). The first 2048 bytes consist of on-chip mask-programmed ROM. At addresses 2048 and greater, the Z8 executes external program memory fetches.

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts.

Data Memory. The Z8 can address 62K bytes of external data memory beginning at locations 2048 (Figure 5). External data memory may be included with or separated from the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on pin $P3_4$, is used to distinguish between data and program memory space.

Register File. The 144-byte register file includes four I/O port registers (R0-R3), 124 general-purpose registers (R4-R127) and sixteen control and status registers (R240-R255). These registers are assigned the address locations shown in Figure 6.

Address Spaces (Cont.)

Z8 instructions can access registers directly or indirectly with an 8-bit address field. The Z8 also allows short 4-bit register addressing using the register pointer (one of the control registers). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying sixteen contiguous locations (Figure 7). The register pointer addresses the starting location of the active working-register group.

Stacks. Either the internal register file or the external data memory can be used for the stack. A 16-bit stack pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory between locations 2048 and 65535. An 8-bit stack pointer (R255) is used for the internal stack which resides within the 124 general-purpose registers (R4-R127).

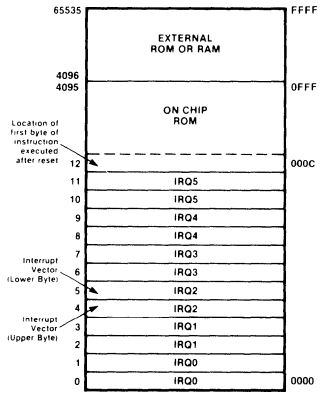


Figure 4. Program Memory Map

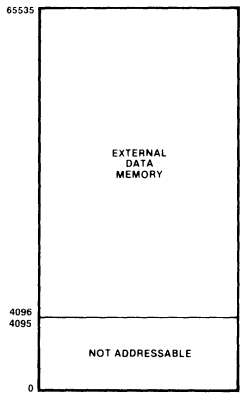


Figure 5. Data Memory Map

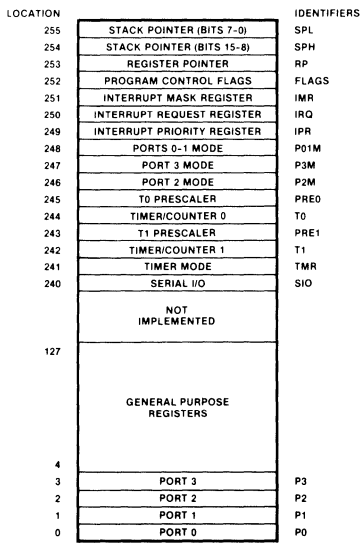


Figure 6. The Register File

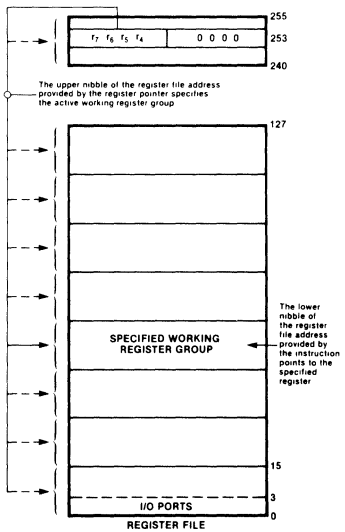


Figure 7. The Register Pointer

I/O Ports

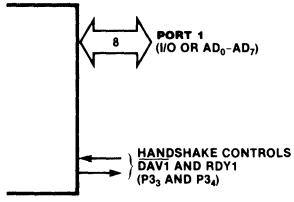
The Z8 has 32 lines dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable as input, output or address/data. Under software control, the ports can be programmed to provide address outputs, timing, status signals, serial I/O, and parallel I/O with or without handshake All ports have active pull-ups and pull-downs compatible with TTL loads.

Port 1

Port 1 can be programmed as a byte I/O port or as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control In this configuration, Port 3 lines $P3_3$ and $P3_4$ are used as the handshake controls RDY1 and $\overline{DAV1}$ (Ready and Data Available)

Memory locations greater than 2048 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed address/data mode (AD_0-AD_7) If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning $P3_3$ as a Bus Acknowledge input, and $P3_4$ as a Bus Request output

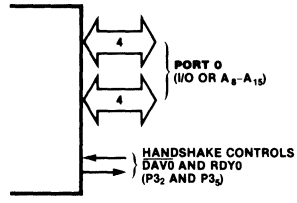


PORT 1

Port 0

Port 0 can be programmed as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3 lines $P3_2$ and $P3_5$ are used as the handshake controls $\overline{DAV0}$ and RDY0.

For external memory references, Port 0 can provide address bits A_8-A_{11} (lower nibble) or A_8-A_{15} (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. When Port 0 nibbles are defined as address bits, they can be set to the high-impedance state along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$.

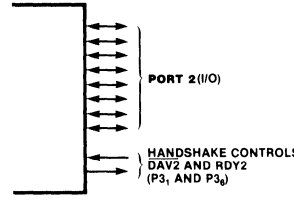


PORT 0

Port 2

Each bit of Port 2 can be programmed independently as an input or an output, and is always available for I/O operations. In addition, Port 2 can be configured to provide open-drain outputs.

Like Ports 0 and 1, Port 2 may also be placed under handshake control. In this configuration, Port 3 lines $P3_1$ and $P3_6$ are used as the handshake controls lines $\overline{DAV2}$ and RDY2. The handshake signal assignment for Port 3 lines $P3_1$ and $P3_6$ is dictated by the direction (input or output) assigned to bit 7 of Port 2.

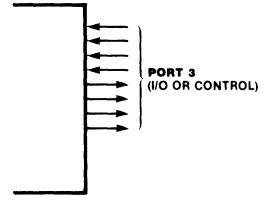


PORT 2

Port 3

Port 3 lines can be configured as I/O or control lines. In either case, the direction of the eight lines is fixed as four input ($P3_0$-$P3_3$) and four output ($P3_4$-$P3_7$). For serial I/O, lines $P3_0$ and $P3_7$ are programmed as serial in and serial out respectively

Port 3 can also provide the following control functions: handshake for Ports 0, 1 and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ0-IRQ3); timer input and output signals (T_{IN} and T_{OUT}) and Data Memory Select ($\overline{DM}$).



PORT 3

Serial Input/Output

Port 3 lines $P3_0$ and $P3_7$ can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by counter/timer 0, with a maximum rate of 62 5 kilobits per second.

The Z8 automatically adds a start bit and two stop bits to transmitted data (Figure 8) The Z8 can also provide odd parity Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit If parity is on, bit 7 of the received data is replaced by a parity error flag Received characters generate the IRQ3 interrupt request

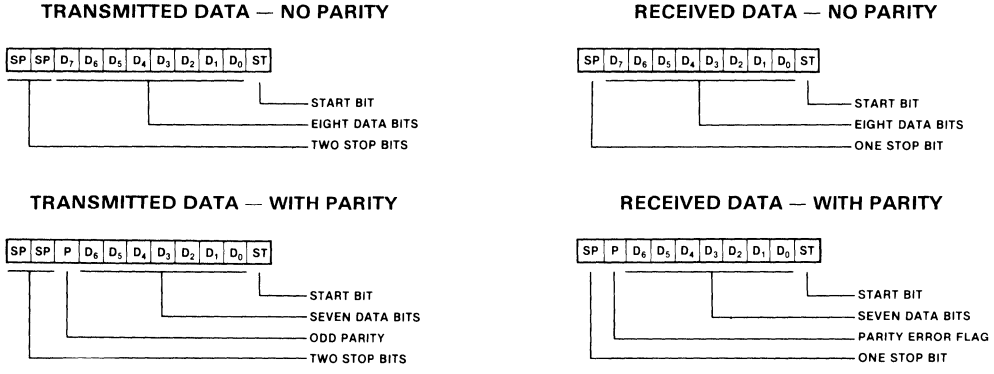


Figure 8. Serial Data Formats.

Counter/Timers

The Z8 contains two 8-bit programmable counter/timers (T_0 and T_1), each driven by its own 6-bit programmable prescaler The T_1 prescaler can be driven by internal or external clock sources, however, the T_0 prescaler is driven by the internal clock only

The 6-bit prescalers can divide the input frequency of the clock source by any number from 1 to 64 Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter When the counter reaches the end of count, a timer interrupt request — IRQ4 (T_0) or IRQ5 (T_1) — is generated

The counters can be started, stopped, restarted to continue, or restarted from the initial value The counters can also be programmed to stop upon reaching zero (single-pass mode), or to automatically reload the initial value and continue counting (modulo-n continuous mode) The counters, but not the prescalers, can be read any time without disturbing their value or count mode

The clock source for T_1 is user-definable and can be the internal microprocessor clock (4 MHz maximum) divided by four, or an external signal input via Port 3 The Timer Mode register configures the external timer input as an external clock (1 MHz maximum), a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be programmably cascaded by connecting the T_0 output to the input of T_1

Port 3 line $P3_6$ also serves as a timer output (T_{OUT}) through which T_0, T_1 or the internal clock can be output

Interrupts

The Z8 allows six different interrupts from eight sources· the four Port 3 lines $P3_0$-$P3_3$, Serial In, Serial Out, and the two counter/timers. These interrupts are both maskable and prioritized The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register.

All Z8 interrupts are vectored When an interrupt request is granted, the Z8 enters an interrupt machine cycle that disables all subsequent interrupts, saves the program counter and status flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

The Z8 also supports polled systems. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request Register polled to determine which of the interrupt requests needs service.

Clock

The on-chip oscillator has a high-gain, series-resonant amplifier for connection to a crystal or to any suitable external clock source (XTAL1 = Input, XTAL2 = Output).

The crystal source is connected across XTAL1 and XTAL2, using the recommended capacitors (C_1 = 15 pF) from each pin to ground. The specifications for the crystal are as follows:

— AT cut, series resonant

— Fundamental type, 8 MHz maximum

— Series resistance $R_S \leq 100\Omega$

Power Down Standby Option

The low-power standby mode allows power to be removed without losing the contents of the 124 general-purpose registers. This mode is available to the user as a bonding option whereby pin 2 (normally XTAL2) is replaced by the V_{MM} (standby) power supply input. This necessitates the use of an external clock generator (input = XTAL1) rather than a crystal source.

The removal of power, whether intended or due to power failure, must be preceded by a software routine that stores the appropriate status into the register file. Figure 9 shows the recommended circuit for a battery back-up supply system

Z8602 Development Device

The 64-pin development version of the 40-pin mask-programmed Z8 allows the user to prototype the system in hardware with an actual Z8 device, and develop the code that is eventually mask-programmed into the on-chip ROM of the Z8601.

The Z8602 is identical to the Z8601 with the following exceptions:

— The internal ROM has been removed

— The ROM address lines and data lines are buffered and brought out to external pins

— Control lines for the new memory have been added

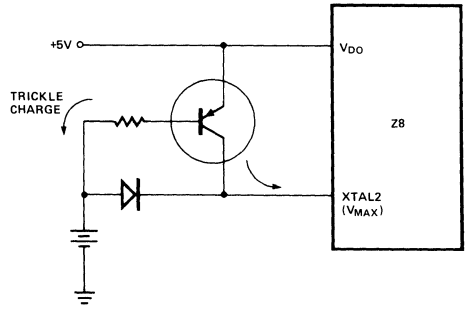


Figure 9. Recommended Driver Circuit for Power Down Operation.

Addressing Modes

The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

IRR Indirect register pair or indirect working-register pair address

Irr Indirect working-register pair only

X Indexed address

DA Direct address

RA Relative address

IM Immediate

R Register or working-register address

r Working-register address only

IR Indirect-register or indirect working-register address

Ir Indirect working-register address only

RR Register pair or working register pair address

Symbols

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
SP	Stack pointer (control registers 254-255)
PC	Program counter
FLAGS	Flag register (control register 252)
RP	Register pointer (control register 253)
IMR	Interrupt mask register (control register 251)

Assignment of a value is indicated by the symbol "←" For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example,

dst (7)

refers to bit 7 or the destination operand.

Flags

Control Register R252 contains the following six flags

C Carry flag
Z Zero flag
S Sign flag
V Overflow flag
D Decimal-adjust flag
H Half-carry flag

Affected flags are indicated by:

0 Cleared to zero
1 Set to one
***** Set or cleared according to operation
— Unaffected
X Undefined

Condition Codes

Condition Codes Value	Mnemonic	Meaning	Flags Set
1000		Always true	---
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 and Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C or Z) = 1
0000		Never true	---

Instruction Formats

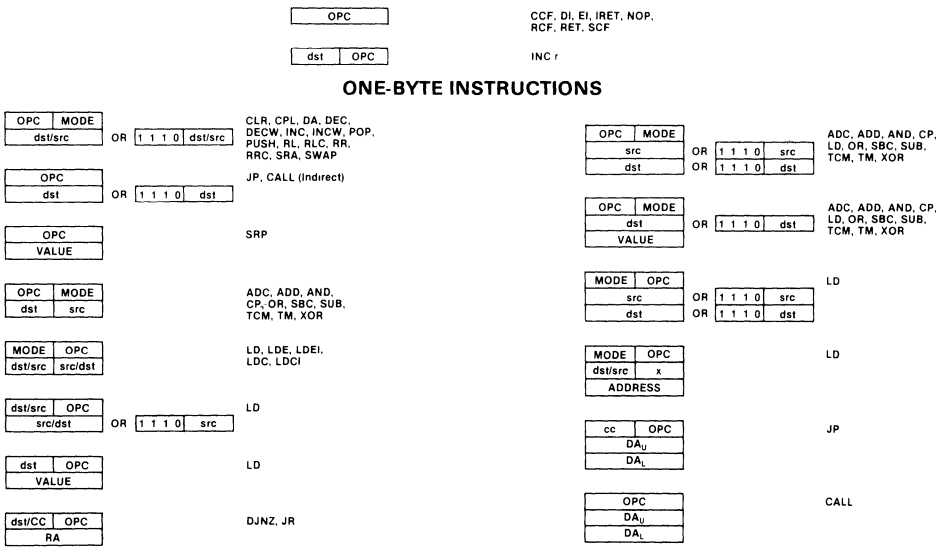
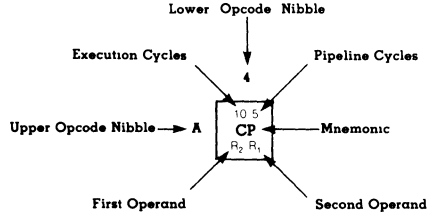


Figure 11. Instruction Formats.

Z8 Opcode Map

Upper Nibble (Hex) \ Lower Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6,5 **DEC** R1	6,5 **DEC** IR1	6,5 **ADD** r1,r2	6,5 **ADD** r1,Ir2	10,5 **ADD** R2,R1	10,5 **ADD** IR2,R1	10,5 **ADD** R1,IM	10,5 **ADD** IR1,IM	6,5 **LD** r1,R2	6,5 **LD** r2,R1	12/10,5 **DJNZ** r1,RA	12/10,0 **JR** cc,RA	6,5 **LD** r1,IM	12/10,0 **JP** cc,DA	6,5 **INC** r1	
1	6,5 **RLC** R1	6,5 **RLC** IR1	6,5 **ADC** r1,r2	6,5 **ADC** r1,Ir2	10,5 **ADC** R2,R1	10,5 **ADC** IR2,R1	10,5 **ADC** R1,IM	10,5 **ADC** IR1,IM								
2	6,5 **INC** R1	6,5 **INC** IR1	6,5 **SUB** r1,r2	6,5 **SUB** r1,Ir2	10,5 **SUB** R2,R1	10,5 **SUB** IR2,R1	10,5 **SUB** R1,IM	10,5 **SUB** IR1,IM								
3	8,0 **JP** IRR1	6,1 **SRP** IM	6,5 **SBC** r1,r2	6,5 **SBC** r1,Ir2	10,5 **SBC** R2,R1	10,5 **SBC** IR2,R1	10,5 **SBC** R1,IM	10,5 **SBC** IR1,IM								
4	8,5 **DA** R1	8,5 **DA** IR1	6,5 **OR** r1,r2	6,5 **OR** r1,Ir2	10,5 **OR** R2,R1	10,5 **OR** IR2,R1	10,5 **OR** R1,IM	10,5 **OR** IR1,IM								
5	10,5 **POP** R1	10,5 **POP** IR1	6,5 **AND** r1,r2	6,5 **AND** r1,Ir2	10,5 **AND** R2,R1	10,5 **AND** IR2,R1	10,5 **AND** R1,IM	10,5 **AND** IR1,IM								
6	6,5 **COM** R1	6,5 **COM** IR1	6,5 **TCM** r1,r2	6,5 **TCM** r1,Ir2	10,5 **TCM** R2,R1	10,5 **TCM** IR2,R1	10,5 **TCM** R1,IM	10,5 **TCM** IR1,IM								
7	10/12,1 **PUSH** R2	12/14,1 **PUSH** IR2	6,5 **TM** r1,r2	6,5 **TM** r1,Ir2	10,5 **TM** R2,R1	10,5 **TM** IR2,R1	10,5 **TM** R1,IM	10,5 **TM** IR1,IM								
8	10,5 **DECW** RR1	10,5 **DECW** IR1	12,0 **LDE** r1,Irr2	18,0 **LDEI** Ir1,Irr2												6,1 **DI**
9	6,5 **RL** R1	6,5 **RL** IR1	12,0 **LDE** r2,Irr1	18,0 **LDEI** Ir2,Irr1												6,1 **EI**
A	10,5 **INCW** RR1	10,5 **INCW** IR1	6,5 **CP** r1,r2	6,5 **CP** r1,Ir2	10,5 **CP** R2,R1	10,5 **CP** IR2,R1	10,5 **CP** R1,IM	10,5 **CP** IR1,IM								14,0 **RET**
B	6,5 **CLR** R1	6,5 **CLR** IR1	6,5 **XOR** r1,r2	6,5 **XOR** r1,Ir2	10,5 **XOR** R2,R1	10,5 **XOR** IR2,R1	10,5 **XOR** R1,IM	10,5 **XOR** IR1,IM								16,0 **IRET**
C	6,5 **RRC** R1	6,5 **RRC** IR1	12,0 **LDC** r1,Irr2	18,0 **LDCI** Ir1,Irr2				10,5 **LD** r1,x,R2								6,5 **RCF**
D	6,5 **SRA** R1	6,5 **SRA** IR1	12,0 **LDC** r2,Irr1	18,0 **LDCI** Ir2,Irr1	20,0 **CALL*** IRR1		20,0 **CALL** DA	10,5 **LD** r2,x,R1								6,5 **SCF**
E	6,5 **RR** R1	6,5 **RR** IR1		6,5 **LD** r1,Ir2	10,5 **LD** R2,R1	10,5 **LD** IR2,R1	10,5 **LD** R1,IM	10,5 **LD** IR1,IM								6,5 **CCF**
F	6,7 **SWAP** R1	6,7 **SWAP** IR1		6,5 **LD** Ir1,r2		10,5 **LD** R2,IR1										6,0 **NOP**
Bytes Per Instruction	2				3				2					3	1	



Legend:
R = 8-Bit Address
r = 4-Bit Address
R_1 or r_1 = Dst Address
R_2 or r_2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank areas are reserved instructions

*2 byte instruction, fetch cycle appears as a 3 byte instruction

Instruction Summary

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst,src dst ← dst + src + C	(Note 1)		1□	* * * * 0 *
ADD dst,src dst ← dst + src	(Note 1)		0□	* * * * 0 *
AND dst,src dst ← dst AND src	(Note 1)		5□	- * * 0 - -
CALL dst SP ← SP - 2 @SP ← PC, PC ← dst	DA IRR		D6 D4	- - - - - -
CCF C ← NOT C			EF	* - - - - -
CLR dst dst ← 0	R IR		B0 B1	- - - - - -
COM dst dst ← NOT dst	R IR		60 61	- * * 0 - -
CP dst,src dst - src	(Note 1)		A□	* * * * - -
DA dst dst ← DA dst	R IR		40 41	* * * X - -
DEC dst dst ← dst - 1	R IR		00 01	- * * * - -
DECW dst dst ← dst - 1	RR IR		80 81	- * * * - -
DI IMR (7) ← 0			8F	- - - - - -
DJNZ r,dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range +127, -128	RA		rA r = 0-F	- - - - - -
EI IMR (7) ← 1			9F	- - - - - -
INC dst dst ← dst + 1	r R IR		rE r = 0-F 20 21	- * * * - -
INCW dst dst ← dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS ← @SP, SP ← SP + 1 PC ← @SP, SP ← SP + 2, IMR (7) ← 1			BF	* * * * * *
JP cc,dst if cc is true PC ← dst	DA IRR		cD c = 0-F 30	- - - - - -
JR cc,dst if cc is true, PC ← PC + dst Range +127, -128	RA		cB c = 0-F	- - - - - -
LD dst,src dst ← src	r r R r X r Ir R R R IR IR	IM R r X r Ir r R IR IM IM R	rC r8 r9 r = 0-F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst,src dst ← src	r Irr	Irr r	C2 D2	- - - - - -
LDCI dst,src dst ← src r ← r + 1, rr ← rr + 1	Ir Irr	Irr Ir	C3 D3	- - - - - -
LDE dst,src dst ← src	r Irr	Irr r	82 92	- - - - - -
LDEI dst,src dst ← src r ← r + 1, rr ← rr + 1	Ir Irr	Irr Ir	83 93	- - - - - -
NOP			FF	- - - - - -
OR dst,src dst ← dst OR src	(Note 1)		4□	- * * 0 - -
POP dst dst ← @SP SP ← SP + 1	R IR		50 51	- - - - - -
PUSH src SP ← SP - 1, @SP ← src		R IR	70 71	- - - - - -
RCF C ← 0			CF	0 - - - - -
RET PC ← @SP, SP ← SP + 2			AF	- - - - - -
RL dst 	R IR		90 91	* * * * - -
RLC dst 	R IR		10 11	* * * * - -
RR dst 	R IR		E0 E1	* * * * - -
RRC dst 	R IR		C0 C1	* * * * - -
SBC dst,src dst ← dst - src - C	(Note 1)		3□	* * * * 1 *
SCF C ← 1			DF	1 - - - - -
SRA dst 	R IR		D0 D1	* * * 0 - -
SRP src RP ← src		IM	31	- - - - - -
SUB dst,src dst ← dst - src	(Note 1)		2□	* * * * 1 *
SWAP dst 	R IR		F0 F1	X * * X - -
TCM dst,src (NOT dst) AND src	(Note 1)		6□	- * * 0 - -
TM dst,src dst AND src	(Note 1)		7□	- * * 0 - -
XOR dst,src dst ← dst XOR src	(Note 1)		B□	- * * 0 - -

Note 1

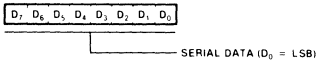
These instructions have an identical set of addressing modes, which are encoded for brevity in this table The higher opcode nibble is found in the instruction set table above The lower nibble is expressed symbolically by a in the table above, and its value is found in the following table to the right of the applicable addressing mode pair

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13

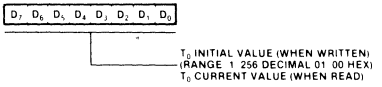
Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

Z8 Control Registers

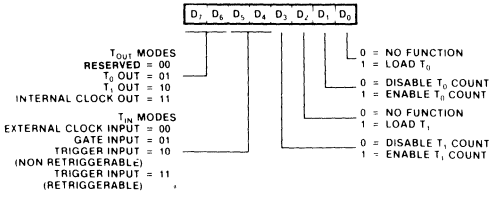
R240 SIO
SERIAL I/O REGISTER
(FO_H; READ/WRITE)



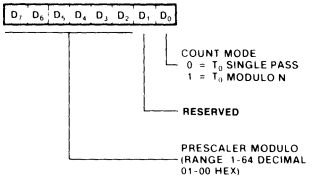
R244 T0
COUNTER/TIMER 0 REGISTER
($F4_H$; READ/WRITE)



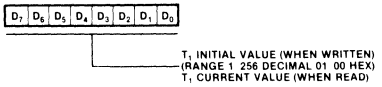
R241 TMR
TIMER MODE REGISTER
($F1_H$; READ/WRITE)



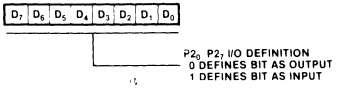
R245 PRE0
PRESCALER 0 REGISTER
($F5_H$; WRITE ONLY)



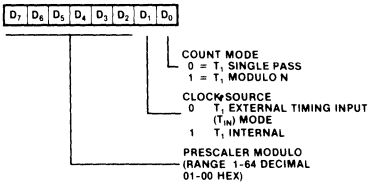
R242 T1
COUNTER TIMER 1 REGISTER
($F2_H$; READ/WRITE)



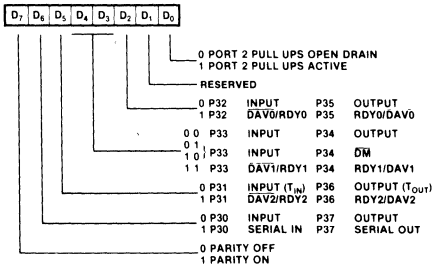
R246 P2M
PORT 2 MODE REGISTER
($F6_H$; WRITE ONLY)



R243 PRE1
PRESCALER 1 REGISTER
($F3_H$, WRITE ONLY)

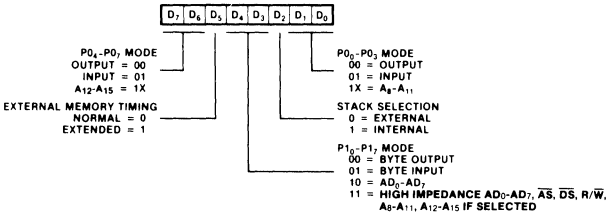


R247 P3M
PORT 3 MODE REGISTER
($F7_H$; WRITE ONLY)

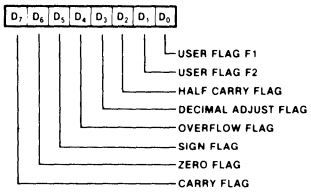


Z8 Control Registers

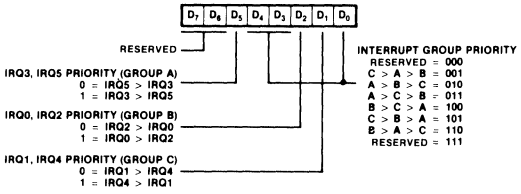
R248 P01M
PORT 0 AND 1 MODE REGISTER
($F8_H$; WRITE ONLY)



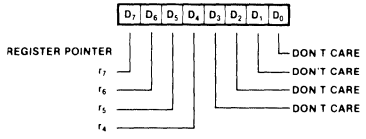
R252 FLAGS
FLAG REGISTER
(FC_H; READ/WRITE)



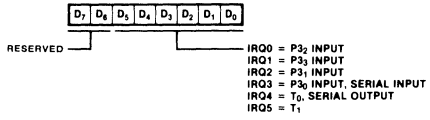
R249 IPR
INTERRUPT PRIORITY REGISTER
($F9_H$, WRITE ONLY)



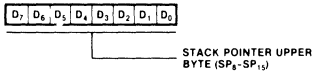
R253 RP
REGISTER POINTER
(FD_H; READ/WRITE)



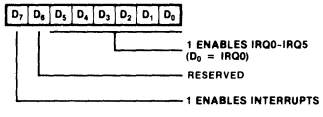
R250 IRQ
INTERRUPT REQUEST REGISTER
(FA_H; READ/WRITE)



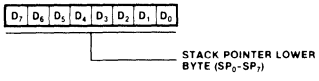
R254 SPH
STACK POINTER
(FE_H: READ/WRITE)



R251 IMR
INTERRUPT MASK REGISTER
(FB_H; READ/WRITE)



R255 SPL
STACK POINTER
(FF_H, READ/WRITE)



MICRO-PROCESSORS

Absolute Maximum Ratings*

Voltages on All Inputs and Outputs with Respect to Ground ..... -0.3V to +7.0V
Operating Ambient Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C

Comment*
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted All voltages are referenced to GND Positive current flows into the reference pin. Standard conditions are as follows:

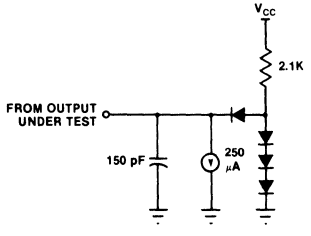
— $+4.75V \leq V_{CC} \leq 5.25V$
— GND = 0V
— $0°C \leq T_A \leq +70°C$

DC Characteristics

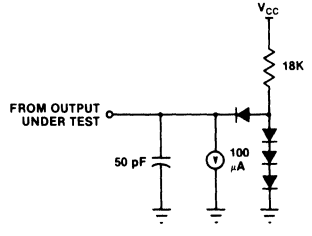
Symbol	Parameter	Min.	Max.	Unit	Condition	Notes
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	V	Driven by External Clock Generator	1
V_{CL}	Clock Input Low Voltage	-0 3	0.8	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0	V_{CC}	V		
V_{IL}	Input Low Voltage	-0.3	0 8	V		
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	V		
V_{RL}	Reset Input Low Voltage	-0.3	0.8	V		
V_{OH}	Output High Voltage	2 4		V	$I_{OH} = 250\ \mu A$	1
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = +2.0$ mA	1
I_{IL}	Input Leakage		±10	μA	$0V \leq V_{IN} \leq +5\ 25V$	
I_{OL}	Output Leakage		±10	μA	$0V \leq V_{IN} \leq +5.25V$	
I_{IR}	Reset Input Current		-50	μA	$V_{CC} = +5\ 25V$, $V_{RL} = 0V$	
I_{CC}	V_{CC} Supply Current		180	mA	$V_{CC} = 5.25V$	
I_{MM}	V_{MM} Supply Current		10	mA	Power Down Mode	
V_{MM}	Backup Supply Voltage	3.0	V_{CC}	V	Power Down Mode	

1 For A_0-A_{11}, $\overline{MDS}$, $\overline{SYNC}$, SCLK and IACK on the Z8602 version, I_{OH} = -100 μA and I_{OL} = 1 0 mA.

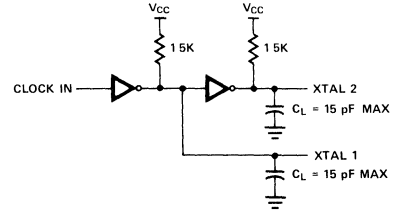
Test Load Circuits



TEST LOAD 1



TEST LOAD 2

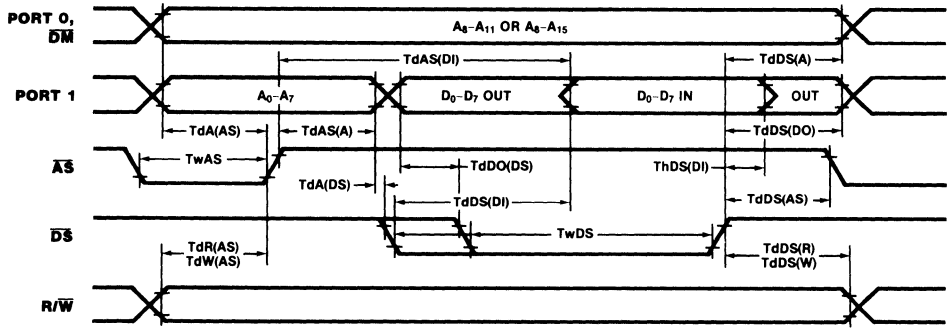


EXTERNAL CLOCK INTERFACE CIRCUIT

External I/O or Memory Read and Write Cycle

Symbol	Parameter	8601/02 Min.	8601/02 Max.	8601A/02A Min.	8601A/02A Max.	Units	Notes
TdA(AS)	Address Valid to $\overline{AS}$↑ Delay	50		35		ns	1,2
TdAS(A)	$\overline{AS}$↑ to Address Float Delay	60		45		ns	1,2
TdAS(DR)	$\overline{AS}$↑ to Read Data Required Valid		320		220	ns	1,2,3,4
TwAS	$\overline{AS}$ Low Width	80		55		ns	1,2
TdA(DI)	Address Float to $\overline{DS}$↓	0		0		ns	1
TwDS	$\overline{DS}$ (Read) Low Width	250		185		ns	1,2,3,4
TwDS	$\overline{DS}$ (Write) Low Width	160		110		ns	1,2,3,4
TdDS(DI)	$\overline{DS}$↓ to Read Data Required Valid		200		130	ns	1,2,3,4
ThDS(DI)	Read Data to $\overline{DS}$↑ Hold Time	0		0		ns	1
TdDS(A)	$\overline{DS}$↑ to Address Active Delay	70		45		ns	1,2,3
TdDS(AS)	$\overline{DS}$↑ to $\overline{AS}$↓ Delay	70		55		ns	1,2,3
TdR/W(AS)	R/$\overline{W}$ Valid to $\overline{AS}$↑ Delay	50		30		ns	1,2,3
TdDS(R/W)	$\overline{DS}$↑ to R/$\overline{W}$ Not Valid	60		35		ns	1,2,3
TdDO(DS)	Write Data Valid to $\overline{DS}$ (Write)↓ Delay	50		35		ns	1,2,3
TdDS(DO)	$\overline{DS}$↑ to Write Data Not Valid Delay	70		45		ns	1,2,3
TdA(DR)	Address Valid to Read Data Required Valid		410		255	ns	1,2,3,4
TdAS(DS)	$\overline{AS}$↑ to $\overline{DS}$↓ Delay	80			55	ns	

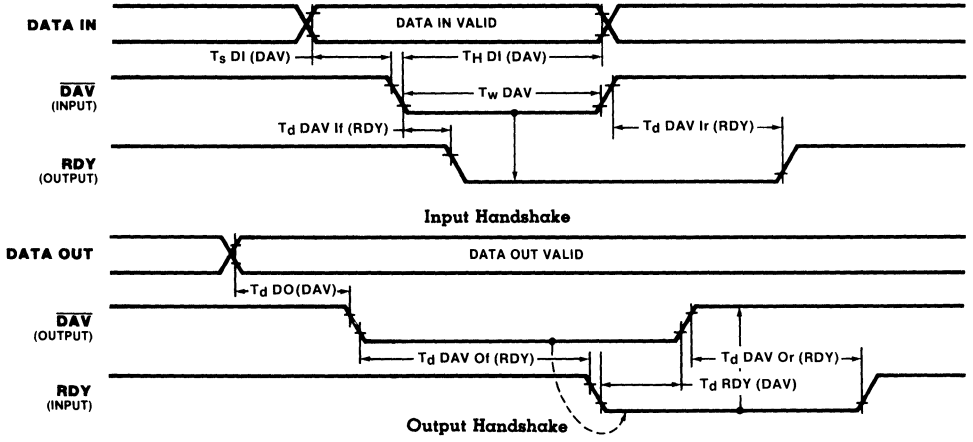
Notes:
1 Test Load 1
2 Timing numbers given are for minimum TpC
3 Also see Clock Cycle Time Dependent Characteristics Table
4 When using extended memory timing add 2 TpC
5. All timing references use 2 0V for a logic "1" and 0 8V for a logic "0"



Handshake Timing

Symbol	Parameter	Z8601/02		Z8601A/02A		Units	Notes
		Min.	Max.	Min.	Max.		
TsDI(DAV)	Data In Set Up Time	0		0		ns	
ThDI(DAV)	Data In Hold Time	230		160		ns	
TwDAV	Data Available Width	175		120		ns	
TdDAVIf(RDY)	$\overline{DAV}$↓ Input to RDY↓ Delay		175		120	ns	1,2
TdDAVOf(RDY)	$\overline{DAV}$↓ Output to RDY↓ Delay	0		0		ns	1,3
TdDAVIr(RDY)	$\overline{DAV}$↑ Input to RDY↑ Delay		175		120	ns	1,2
TdDAVOr(RDY)	$\overline{DAV}$↑ Output to RDY↑ Delay	0		0		ns	1,3
TdDO(DAV)	Data Out to $\overline{DAV}$↓ Delay	50		30		ns	1
TdRDY(DAV)	RDY↓ Input to $\overline{DAV}$↑ Delay	0	200	0	140	ns	1

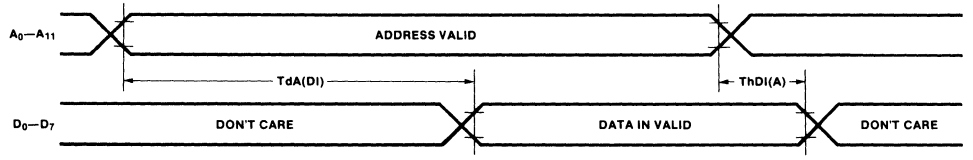
Notes:
1 Test Load 1
2 Input handshake
3 Output handshake
4 All timing references use 2 0V for a logic "1" and 0 8V for a logic "0"



Memory Port Timing Z8602, Z8603

Symbol	Parameter	Z8602		Z8602A		Units	Notes
		Min.	Max.	Min.	Max.		
TdA(DI)	Address Valid to Data Input Delay		460		320	ns	1,2
ThDI(A)	Data In Hold Time	0		0		ns	1

Notes:
1 Test Load 2
2 This is a clock cycle dependent parameter For clock frequencies other than maximum frequency use the following formula
Z8602 and Z8603 = 5TpC — 165
Z8602A and Z8603A = 5TpC — 95.



Package Availability 40 Pin Molded DIP

Ordering Information

Part Number	Temperature Range	Number of Pins	Package	Description
Z8601 PS	0°C to +70°C	40	Plastic	8-Bit Single-Chip Microcomputer Circuit
Z8601A PS	0°C to +70°C	40	Plastic	12 MHz Single-Chip Microcomputer Circuit

Synertek.

Z8681

Z8 Family
Z8681 Microcomputer

Features

- "ROMless" version of the Z8601 Single-Chip Microcomputer, capable of Addressing up to 128K Bytes of External Memory Space
- Up to 24 Programmable I/O Lines
- 40-pin Package, Single +5 V supply, all Pins TTL Compatible

Description

The Z8681 MCU is the "ROMless" version of the Z8601 single-chip microcomputer and offers all the outstanding features of the Z8 Family architecture Using the Z8681, it is possible to design a powerful microprocessor system incorporating a minimum number of support devices

Port 1 is configured to function as a multiplexed Address/Data bus (AD_0-AD_7), while Port 0 is software configurable to output address bits A_8-A_{15} This provides for program memory and data memory space of up to 64K bytes each Located on-chip are 144 bytes of RAM, organized as a register file of 124 general-purpose registers, 16 control and status registers, and three I/O port registers (Port 1 cannot be utilized as an I/O register.) This file is divided into groups of working registers in such a way that short format instructions may be used to quickly access a register within a certain group

Pin Configuration

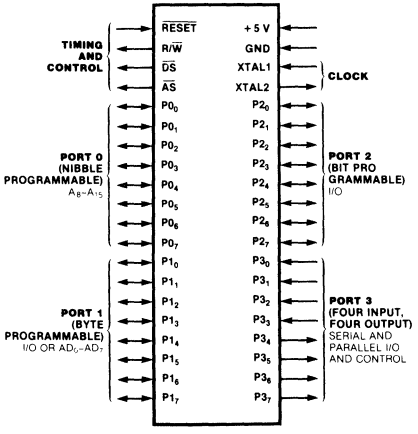


Figure 1. Pin Functions

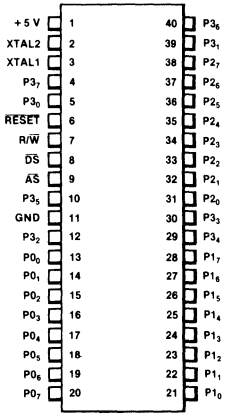


Figure 2. Pin Assignments

*Z8 is a trademark of Zilog Inc

Functional Description

Register File. The internal register organization of the Z8681 centers around a 144-byte random-access register file composed of 124 general-purpose registers, 16 control registers, and the three I/O port registers Any general-purpose register can be an accumulator, address pointer, index register, or part of the internal stack The register file is divided into nine groups of 16 working registers A register pointer uses short-format instructions to quickly access any one of the nine groups, resulting in fast and easy task-switching

I/O Ports. The I/O ports (Ports 0, 2, and 3) are software configurable as input, output, or additional address lines These ports can also provide timing, status signals, and serial or parallel I/O (with or without handshake)

I/O port space is mapped into the register file, creating an efficient and convenient means of moving data

Interrupts. The Z8681 can respond to six separate interrupts from eight sources The interrupts are maskable and prioritized by software control, thus allowing greater design flexibility

Using vectored interrupts, control is automatically passed to the appropriate service routine The interrupts are organized as four external lines and four internal status signals The internal interrupts control the serial port handshake and the two counter/timers

UART. The Z8681 also offers the serial I/O capability of interfacing to asynchronous data communications The on-chip counter (T0) is used to supply the baud rate for the serial data transfer The UART is capable of transferring data at a rate of up to 62 5K b/s

Counter/Timers. Also on-chip are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler Both counter/timers can operate independently of the processor instruction sequence, thereby unburdening the program from such time-critical operations as event-counting or elapsed-time calculations The counters can be started, stopped, continued, or restarted from the initial value by program control.

Instruction Set for the Z8681

The basic instruction set for the Z8681 consists of 47 instruction types and utilizes seven addressing modes The instructions can operate on several types of data elements, including individual bits, 4-bit BCD characters, bytes, or words

All 124 general-purpose registers can be used as accumulators, address pointers, index registers, or as internal stack, resulting in fast data manipulation for real-time applications The internal pipelining of instructions dramatically increases throughput by allowing instruction fetches during the previous instruction execution cycles.

Z8681 Applications

The Z8681 is a Z-BUS-compatible device and can be interfaced to various Z-BUS peripherals such as the Z-CIO, Z-SCC, or FIO Due to the flexibility of Port 0 and the data memory select feature, the Z8681 can also support a great variety of memory configurations Figures 3 and 4 illustrate two design approaches using the Z8681

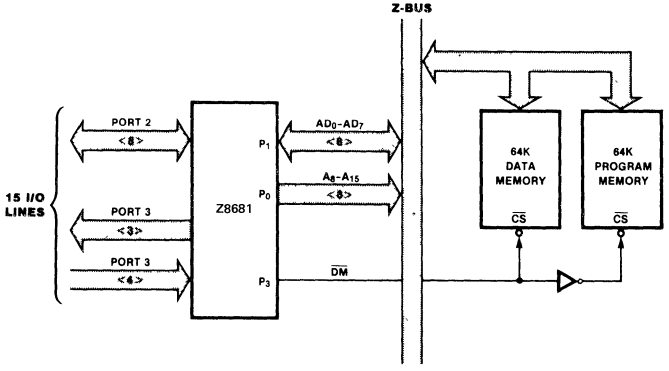


Figure 3. Z8681 Interfacing to External Memory.

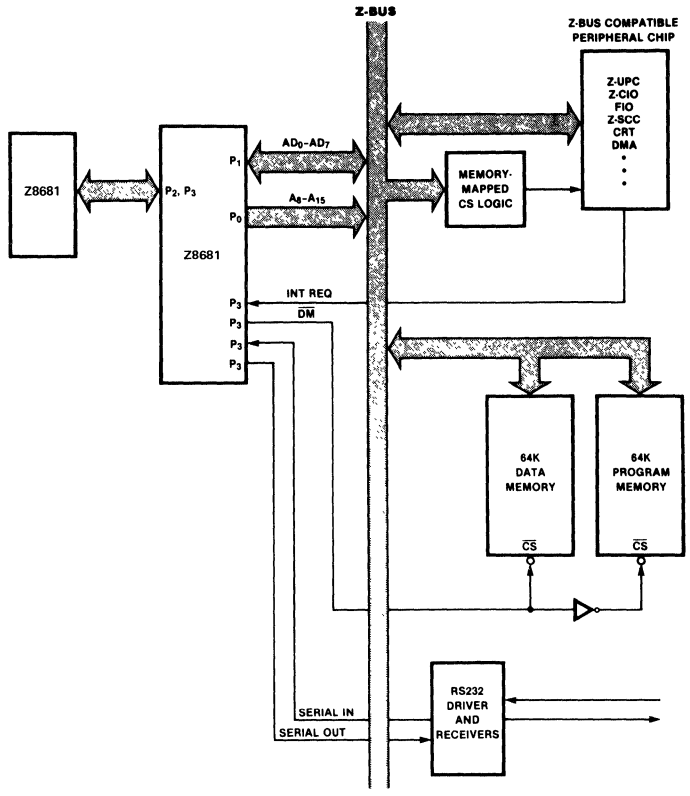


Figure 4. Z8681 Interfacing to Memory-Mapped I/O.

Ordering Information

Product Number	Package/ Temp.	Speed	Description	Product Number	Package/ Temp.	Speed	Description
Z8681	CE	8 0 MHz	Z8 MCU (ROMless, 40-pin)	Z8681	DS	8.0 MHz	Z8 MCU (ROMless, 40-pin)
Z8681	CS	8 0 MHz	Same as above	Z8681	PE	8.0 MHz	Same as above
Z8681	DE	8 0 MHz	Same as above	Z8681	PS	8 0 MHz	Same as above

Notes C = Ceramic, D = Cerdip, P = Plastic, E = -40°C to +85°C, S = 0°C to +70°C

Synertek.

SY8048/SY8035

Single Component 8-Bit Microcontroller

ADVANCED INFORMATION

Features

- On-Chip Oscillator Circuit and Clock (or External Source)
- 27 I/O Lines
- Expandable Memory and I/O
- 8-Bit Timer/Counter
- Single-Level Interrupt
- 96 Instructions (Most Single-Byte)
- Binary and BCD Arithmetic
- Single +5V Power Supply
- Low Standby Power Mode
- Low Voltage Standby
- 8-Bit CPU, RAM, ROM, I/O in a Single Package
- 2.5 μsec Cycle, 6 MHz Clock, 1.36 μsec Cycle, 11 MHz Clock

General Description

The SY8048/SY8035 are totally self-sufficient 8-bit parallel computers fabricated on single silicon chips using Synertek's advanced N-channel silicon gate MOS process. The SY8048 contains a 1Kx8 program memory, a 64x8 data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting predominantly of single byte instructions and no instructions over two bytes in length. For systems requiring extra capability, the SY8048 can be expanded using standard memory and peripheral devices. The SY8035 is the equivalent of the SY8048 without resident program memory and can be used with external ROM and RAM.

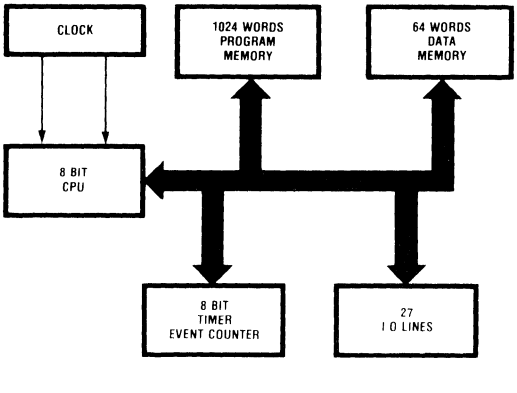


FIGURE 1
SY8048 Block Diagram

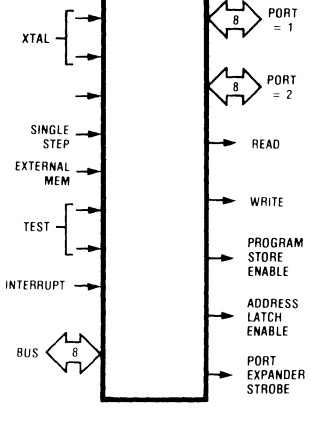


FIGURE 2.
SY8048 Logic Symbol

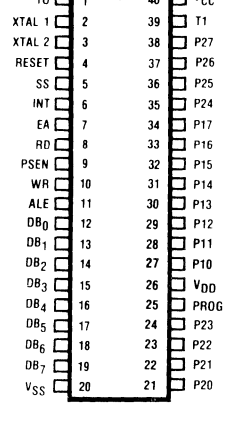


FIGURE 3. SY8048
Pin Configuration
(top view)

MICRO-PROCESSORS

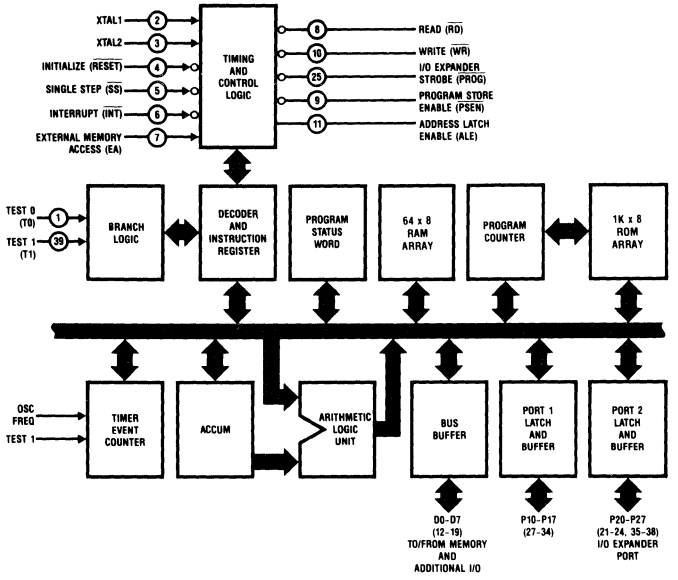


FIGURE 4. SY8048 Detailed Block Diagram

Functional Pin Description

Input Signals

Reset ($\overline{\text{RESET}}$): An active low (0) input that initializes the processor and is used to verify program memory.

Single Step ($\overline{\text{SS}}$): Active low (0) input which, in conjunction with ALE, can single step the processor through each instruction

External Access (EA): An active high (1) input that forces all program memory fetches to reference external program memory.

Testable Input 0 (T0): Testable input pin using conditional branch functions JT0 (T0 = 1) or JNT0 (T0 = 0) T0 can be designated as the clock output using instruction ENT0 CLK

Testable Input 1 (T1): Testable input pin using conditional branch functions JT1 (T1 = 1) or JNT1 (T1 = 0) T1 can be designated as the Timer/Counter input from an external source using instruction STRT CNT

Interrupt ($\overline{\text{INT}}$): An active low input that initiates an interrupt when interrupt is enabled Interrupt is disabled after a RESET Also can be tested with instruction JNI (INT = 0)

Output Signals

Read Strobe ($\overline{\text{RD}}$): An active low output strobe activated during a Bus read Can be used to enable data onto the Bus from an external device Used as a Read Strobe to External Data Memory

Write Strobe ($\overline{\text{WR}}$): An active low output strobe activated during a Bus write Used as a Write Strobe to External Data Memory

Program Store Enable ($\overline{\text{PSEN}}$): An active low output that occurs only during an external program memory fetch

Address Latch Enable (ALE): An active high output that occurs once during each cycle and is useful as a clock output The negative going edge of ALE strobes the address into External Data or Program Memory

Program ($\overline{\text{PROG}}$): This output (active out) provides the output strobe for an 8243 I/O Expander

Input/Output Signals

Crystal Input (XTAL1, XTAL2): These two pins connect the crystal for internal oscillator operation. XTAL1 is the timing input for external source

Port 1 (P10–P17): 8-bit quasi-bidirectional port

Port 2 (P20–P27): 8-bit quasi-bidirectional port. During an external program memory fetch, the 4 high-order program counter bits occur at P20–P23. They also serve as a 4-bit I/O Expander Bus when an 8243 I/O Expander is used

Bus (DB_0–DB_7): True bidirectional port, either statically latched or synchronous. Can be written to using $\overline{\text{WR}}$ Strobe, or Read from using $\overline{\text{RD}}$ Strobe. During an External Program Memory fetch, the 8 lower-order program counter bits are present at this port The addressed instruction appears on this bus when PSEN is low During an external RAM data transaction, this port presents address and data under control of ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$

V_{SS}: Processor Ground potential

V_{DD}: V_{DD} functions as the Low Power Standby Voltage Can be tied to V_{CC} if power-down operation is not required

V_{CC} (Pin 40): Primary power source for the SY8048

Functional Description

The following paragraphs contain the functional description of the major elements of the SY8048 microcomputer/controller The SY8048 contains the system timing and control logic necessary to implement dedicated control functions The data paths are illustrated in simplified form (see *Figure 4*) to show how the various logic elements communicate with each other to implement the SY8048 instruction set

Program Memory

The Program Memory (ROM) contained on the SY8048 is comprised of 1024 bytes As seen by examining the SY8048 instruction set, these bytes may be program instructions, program data or ROM addressing data The ROM for the SY8048 must be mask programmed at the Synertek factory The SY8035 ROMless microcomputer uses external program memory ROM addressing, up to a maximum of 4K bytes, is accomplished by a 12-bit Program Counter (PC) The SY8048 will automatically address external memory when the boundary of the internal 1K memory is exceeded The binary value of the address selects one of the 8-bit bytes contained in ROM A new address is loaded into the PC register during each instruction cycle Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential binary count value

With reference to the Program Memory Map (see *Figure 5*) there are three ROM addresses which provide for the control of the microcomputer

1 Memory Location 0000 — Asserting the RESET (negative true) input to the microcomputer forces the first instruction to be fetched from address 0000

2 Memory Location 0003 — Asserting the interrupt (negative true) input to the microcomputer (when interrupt is enabled) forces a jump to subroutine

3 Memory Location 0007 — A Timer/Counter interrupt that results from Timer/Counter overflow (when enabled) forcing a jump to subroutine

Data Memory (RAM)

The resident RAM data memory is arranged as 64 bytes RAM addressing is implemented indirectly via either of two 8-bit RAM pointer registers R0 or R1 These pointer registers are essentially the first two locations in the RAM (see *Figure 6*), addresses 00 and 01 RAM addressing may also be performed directly by 11 direct register instructions The register area of the RAM array is made up of eight working registers that occupy either the first bank (0), locations 0 to 7, or the second bank (1), locations 24 to 31 The second bank of working registers is selected by using the Register Bank Switch instruction (SEL RB) If this bank is not used for working registers, it can be used as user RAM

There is an 8-level stack after Bank 0 that occupies address locations 8 to 23 These RAM locations are addressed indirectly through R0, R1 or the 3-bit Stack Pointer (SP) The stack pointer keeps track of the return address and pushes each return address down into the stack There are 8 levels of subroutine nesting possible in the stack because each address occupies 10 bits or more using two bytes in RAM When the level of subroutine nesting is less than 8, the stacks not used may be utilized as user RAM locations

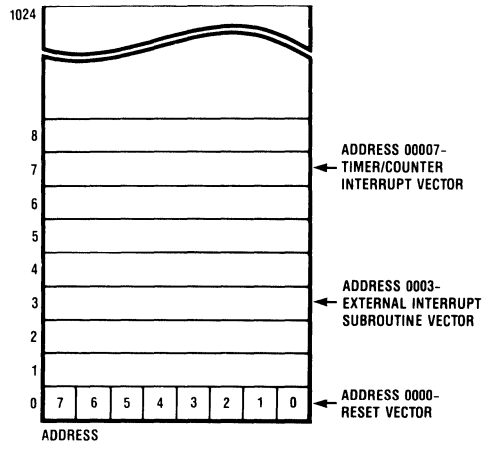


FIGURE 5. SY8048 Resident ROM Program Memory Map

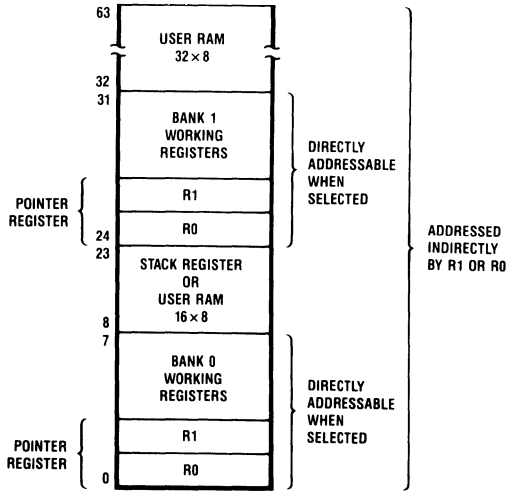


FIGURE 6. SY8048 Resident RAM Data Memory Map

MICRO-PROCESSORS

Functional Description (Continued)

Input/Output

The SY8048 has 27 lines of input/output organized as three 8-bit ports plus three test inputs. The three ports may be used as inputs, outputs or bidirectional ports. Ports 1 and 2 differ from Port 3 (Bus Port) in that they are quasi-bidirectional ports Ports 1 and 2 can be used as input and output while being statically latched If more I/O lines are required, Port 2 can also serve as a 4-bit I/O bus expander when used in conjunction with an 8243 I/O Expander

The bus port is a true bidirectional port and is either statically latched or synchronous It can be written to using $\overline{WR}$ strobe or read from using $\overline{RD}$ strobe During an external program memory fetch, the 8 lower-order program counter bits are present at this port. The addressed instruction appears on this bus when $\overline{PSEN}$ is low During an external RAM data transaction, this port presents address and data under control of ALE, $\overline{RD}$, and $\overline{WR}$

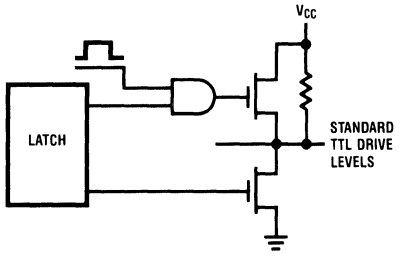


FIGURE 7. Ports 1 and 2 Input/Output Circuit

Power-Down Mode

During the power-down mode, V_{DD}, which normally maintains the RAM cells, is the only pin that receives power V_{CC}, which serves the CPU and ports, is dropped from a voltage of nominal 5 to 0 after the CPU is reset, so that the RAM cells are unaltered by the loss of power When power is restored, the processor goes through the normal power-on procedure

Instruction Set

Table 1 details the 96 instructions common to both the microcomputers and the microprocessors The table provides the mnemonic, function, and description, instruction code, number of cycles and, where applicable, flag settings

TABLE 1. Instruction Set

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
CONTROL								
EN I		Enable the External Interrupt input.	1	1				
DIS I		Disable the External Interrupt input.	1	1				
ENT0 CLK		Enable T0 as the Clock Output.	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0-2047) of Program Memory.	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048-4095 of Program Memory.	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0-7) of Data Memory.	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24-31) of Data Memory.	1	1				
DATA MOVES								
MOV A, #data	(A) ← data	Move Immediate the specified data into the Accumulator.	2	2				
MOV A, Rr	(A) ← (Rr); r = 0-7	Move the contents of the designated registers into the Accumulator.	1	1				
MOV A, @ Rr	(A) ← ((Rr)), r = 0-1	Move Indirect the contents of data memory location into the Accumulator.	1	1				

TABLE 1. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
DATA MOVES (Continued)								
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1				
MOV Rr, #data	(Rr) ← data; r = 0-7	Move Immediate the specified data into the designated register.	2	2				
MOV Rr, A	(Rr) ← (A), r = 0-7	Move Accumulator contents into the designated register.	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0-1	Move Indirect Accumulator contents into data memory location.	1	1				
MOV @ Rr, #data	((Rr)) ← data; r = 0-7	Move Immediate the specified data into data memory.	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the Program Status Word.	1	1	•	•	•	
MOVP A, @ A	(PC 0-7) ← (A) (A) ← ((PC))	Move the content of program memory location in the current page addressed by the content of Accumulator into the Accumulator.	2	1				
MOVP3 A, @ A	(PC 0-7) ← (A) (PC 8-10) ← 011 (A) ← ((PC))	Move the content of program memory location in page 3 addressed by the content of Accumulator into the Accumulator.	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0-1	Move Indirect the contents of external data memory into the Accumulator.	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0-1	Move Indirect the contents of the Accumulator into external data memory.	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0-7	Exchange the Accumulator and designated register's contents.	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0-1	Exchange Indirect contents of Accumulator and location in data memory.	1	1				
XCHD A, @ Rr	(A0-A3) ← (((Rr)) 0-3); R = 0-1	Exchange Indirect 4-bit contents of Accumulator and data memory.	1	1				
TIMER COUNTER								
EN TCNTI		Enable Internal Interrupt Flag for Timer/Counter output.	1	1				
DIS TCNTI		Disable Internal Interrupt Flag for Timer/Counter output.	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	1	1				
STOP TCNT		Stop Count for Event Counter.	1	1				
STRT CNT		Start Count for Event Counter.	1	1				
STRT T		Start Count for Timer.	1	1				

TABLE 1. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
ACCUMULATOR								
ADD A, #data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	2	2	•	•		
ADD A, Rr	(A) ← (A) + (Rr) for r = 0-7	Add contents of designated register to the Accumulator.	1	1	•	•		
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0-1	Add Indirect the contents of data memory location of the Accumulator.	1	1	•	•		
ADDC A, #data	(A) ← (A) (C) + data	Add Immediate with carry the specified data to the Accumulator.	2	2	•	•		
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0-7	Add with carry the contents of the designated register to the Accumulator.	1	1	•	•		
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0-1	Add Indirect with carry the contents of data memory location to the Accumulator.	1	1	•	•		
ANL A, #data	(A) ← (A) AND data	Logical AND specified Immediate Data with Accumulator.	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0-7	Logical AND contents of designated register with Accumulator.	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0-1	Logical AND Indirect the contents of data memory with Accumulator.	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	1	1				
CLR A	A ← 0	CLEAR the contents of the Accumulator.	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	1	1	•			
DEC A	(A) ← (A) − 1	DECREMENT by 1 the Accumulator's contents.	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	1	1				
ORL A, #data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0-7	Logical OR contents of designated register with Accumulator.	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0-1	Logical OR Indirect the contents of data memory location with Accumulator.	1	1				
RLA	(An + 1) ← (An) for n = 0-6 (A0) ← (A7)	Rotate Accumulator left by 1-bit without carry.	1	1				
RLC A	(An + 1) ← (An); n = 0-6 (A0) ← (C) (C) ← (A7)	Rotate Accumulator left by 1-bit through carry	1	1	•			
RR A	(An) ← (An + 1), n = 0-6 (A7) ← (A0)	Rotate Accumulator right by 1-bit without carry	1	1				
RRC A	(An) ← (An + 1), n + 0-6 (A7) ← (C) (C) ← (A0)	Rotate Accumulator right by 1-bit through carry.	1	1	•			

TABLE 1. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
ACCUMULATOR (Continued)								
SWAP	(A4-A7) ↔ (A0-A3)	Swap the 2 4-bit nibbles in the Accumulator.	1	1				
XRL A, #data	(A) ← (A) XOR data	Logical XOR Immediate specified data with Accumulator.	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0-7	Logical XOR contents of designated register with Accumulator.	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0-1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1				
BRANCH								
DJNZ Rr, addr	(Rr) ← (Rr) −, r = 0-7 if (Rr) ≠0, (PC 0-7) ← addr	Decrement the specified register and test contents.	2	2				
JBb addr	(PC 0-7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	2	2				
JC addr	(PC 0-7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	2	2				
JFO addr	(PC 0-7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	2	2				
JFI addr	(PC 0-7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	2	2				
JMP addr	(PC 8-10) ← 8-10 (PC 0-7) ← addr 0-7 (PC 11) ← DBF	Direct Jump to specified address with the 2K address block.	2	2				
JMPP @ A	(PC 0-7) ← ((A))	Jump Indirect to specified address pointed to by the Accumulator in current page.	2	1				
JNC addr	(PC 0-7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	2	2				
JNI addr	(PC 0-7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	2	2				
JNT0 addr	(PC 0-7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	2	2				
JNT1 addr	(PC 0-7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	2	2				
JNZ addr	(PC 0-7) ← addr if A ≠0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	2	2				
JFT addr	(PC 0-7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	2	2				
JT0 addr	(PC 0-7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	2	2				
JT1 addr	(PC 0-7) ← if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	2	2				
JZ addr	(PC 0-7) ← addr if A = 0 (PC) ← (PC) + 1 if A = 1	Jump to specified address if Accumulator is 0.	2	2				

TABLE 1. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
INPUT/OUTPUT								
ANL BUS, #data	(BUS) ← (BUS) AND data	Logical AND Immediate specified data with contents of BUS	2	2				
ANL Pp, #data	(Pp) ← (Pp) AND data; p = 1-2	Logical AND Immediate specified data with designated port (1 or 2).	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A0-A3); p = 4-7	Logical AND contents of Accumulator with designated port (4-7).	2	1				
IN A, Pp	(A) ← (Pp); p = 1-2	Input data from designated port (1-2) into Accumulator	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	2	1				
MOVD A, Pp	(A0-A3) ← (Pp); p = 4-7 (A4-A7) ← 0	Move contents of designated port (4-7) into Accumulator.	2	1				
MOVD Pp, A	(Pp) ← (A0-A3); p = 4-7	Move contents of Accumulator to designated port (4-7).	2	1				
ORL BUS, #data	(BUS) ← (BUS) OR data	Logical OR Immediate specified data with contents of BUS.	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A0-A3); p = 4-7	Logical OR contents of Accumulator with designated port (4-7).	2	1				
ORL Pp, #data	(Pp) ← (Pp) OR data; p = 1-2	Logical OR Immediate specified data with designated port (1-2)	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	2	1				
OUTL Pp, A	(Pp) ← (A), p = 1-2	Output contents of Accumulator to designated port (1-2).	2	1				
REGISTERS								
DEC Rr	(Rr) ← (Rr) − 1, r = 0-7	Decrement by 1 contents of designated register.	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0-7	Increment by 1 contents of designated register.	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0-1	Increment Indirect by 1 the contents of data memory location	1	1				
SUBROUTINE								
CALL addr	((SP)) ← (PC) ((SP)) ← (PSW 4-7) (SP) ← (SP) + 1 (PC 8-10) ← addr 8-10 (PC 0-7) ← addr 0-7 (PC 11) ← DBF	Call designated Subroutine.	2	2				
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	2	1				
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW 4-7) ← ((SP))	Return from Subroutine restoring Program Status Word.	2	1	•	•		

TABLE 1. Instruction Set (Continued)

Mnemonic	Function	Description	Cycles	Bytes	Flags			
					C	AC	F0	F1
FLAGS								
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0	1	1				•
MISCELLANEOUS								
NOP		No operation	1	1				

Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
b	Bit Designator (b = 0–7)
BS	Bank Switch
Bus	Bus Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

Symbol	Description
p	Port Designator (p = 1, 2 or 4–7)
PSW	Program Status Word
r	Register Designator (r = 0, 1 or 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of Register
((xx))	Contents of Memory Location Addressed by the Contents of Register
	Replaced by

Absolute Maximum Ratings

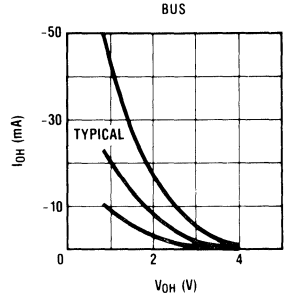
Temperature Under Bias	−20°C to +85°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7V
Power Dissipation	1.5 Watt

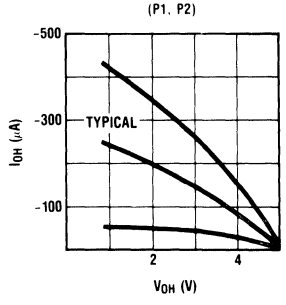
Note Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

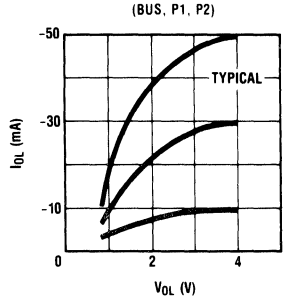
DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage (Except XTAL1, XTAL2, $\overline{RESET}$)		-0.5		0.8	V
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, $\overline{RESET}$)		-0.5		0.6	V
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, $\overline{RESET}$)		2.0		V_{CC}	V
V_{IH1}	Input High Voltage (XTAL1, XTAL2, $\overline{RESET}$)		3.8		V_{CC}	V
V_{OL}	Output Low Voltage (Bus)	I_{OL} = 2 mA			.45	V
V_{OL1}	Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OL} = 1.8 mA			.45	V
V_{OL2}	Output Low Voltage ($\overline{PROG}$)	I_{OL} = 1.0 mA			45	V
V_{OL3}	Output Low Voltage (Ports and Others)	I_{OL} = 1.6 mA			.45	V
V_{OH}	Output High Voltage (Bus)	I_{OH} = -400 μA	2 4			V
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH} = -100 μA	2.4			V
V_{OH2}	Output High Voltage (Ports and Others)	I_{OH} = -40 μA	2.4			V
I_{LI}	Input Leakage Current (T1, $\overline{INT}$, EA)	$V_{SS} \le V_{IN} \le V_{CC}$			±10	μA
I_{LI1}	Input Leakage Current Ports	V_{SS} + 0.45 ≤ $V_{IN} \le V_{CC}$			-500	μA
I_{LI2}	Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	V_{SS} + 0.45 ≤ $V_{IN} \le V_{CC}$			-300	μA
I_{LO}	Output Leakage Current (Bus, T_0) High Impedance State	V_{SS} + 0.45 ≤ $V_{IN} \le V_{CC}$			±10	μA
I_{DD}	Standby Current			4	8	mA
I_{DD} + I_{CC}	Total Supply			55	80	mA
V_{DD}	Standby Power Supply		2 2		V_{CC}	V







AC Characteristics T_A = 0°C to +70°C, V_{CC} = V_{DD} = 5V ±10%, V_{SS} = 0V

Symbol	Parameter	f (t_{CY}) (Note 3)	11 MHz		Units
			Min	Max	
t_{LL}	ALE Pulse Width (Note 1)	7/30 t_{CY} – 170	150		ns
t_{AL}	Address Setup to ALE (Note 1)	2/15 t_{CY} – 110	70		ns
t_{LA}	Address Hold from ALE (Note 1)	1/15 t_{CY} – 40	50		ns
t_{CC1}	Control Pulse Width ($\overline{RD}$, $\overline{WR}$) (Note 1)	1/2 t_{CY} – 200	480		ns
t_{CC2}	Control Pulse Width ($\overline{PSEN}$) (Note 1)	2/5 t_{CY} – 200	350		ns
t_{DW}	Data Setup Before $\overline{WR}$ (Note 1)	13/30 t_{CY} – 200	390		ns
t_{WD}	Data Hold After $\overline{WR}$ (Notes 1, 2)	1/15 t_{CY} – 50	40		ns
t_{DR}	Data Hold ($\overline{RD}$, $\overline{PSEN}$) (Notes 1, 4)	1/10 t_{CY} – 30	0	110	ns
t_{RD1}	$\overline{RD}$ to Data In (Note 1)	2/5 t_{CY} – 170		370	ns
t_{RD2}	$\overline{PSEN}$ to Data In (Note 1)	3/10 t_{CY} – 170		240	ns
t_{AW}	Address Setup to $\overline{WR}$ (Note 1)	1/3 t_{CY} – 150	300		ns
t_{AD1}	Address Setup to Data ($\overline{RD}$) (Note 1)	21/30 t_{CY} – 220		730	ns
t_{AD2}	Address Setup to Data ($\overline{PSEN}$) (Note 1)	1/2 t_{CY} – 200		480	ns
t_{AFC1}	Address Float to $\overline{RD}$, $\overline{WR}$ (Notes 1, 2)	2/15 t_{CY} – 40	140		ns
t_{AFC2}	Address Float to $\overline{PSEN}$ (Notes 1, 2)	1/30 t_{CY} – 40	10		ns
t_{LAFC1}	ALE to Control ($\overline{RD}$, $\overline{WR}$) (Note 1)	1/5 t_{CY} – 75	200		ns
t_{LAFC2}	ALE to Control ($\overline{PSEN}$) (Note 1)	1/10 t_{CY} – 75	60		ns
t_{CA1}	Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$) (Note 1)	1/15 t_{CY} – 40	50		ns
t_{CA2}	Control to ALE ($\overline{PSEN}$) (Note 1)	4/15 t_{CY} – 40	320		ns
t_{CP}	Port Control Setup to $\overline{PROG}$ (Note 1)	1/10 t_{CY} – 80	50		ns
t_{PC}	Port Control Hold from $\overline{PROG}$ (Note 1)	4/15 t_{CY} – 260	100		ns
t_{PR}	$\overline{PROG}$ to P2 Input Valid (Note 1)	17/30 t_{CY} – 140		630	ns
t_{PF}	Input Data Hold from $\overline{PROG}$ (Notes 1, 4)	1/10 t_{CY}	0	140	ns
t_{DP}	Output Data Setup (Note 1)	2/5 t_{CY} – 290	260		ns
t_{PD}	Output Data Hold (Note 1)	1/10 t_{CY} – 90	40		ns
t_{PP}	$\overline{PROG}$ Pulse Width (Note 1)	7/10 t_{CY} – 250	700		ns
t_{PL}	Port 2 I/O Setup to ALE (Note 1)	4/15 t_{CY} – 200	160		ns
t_{LP}	Port 2 I/O Hold to ALE (Note 1)	1/10 t_{CY} – 120	15		ns
t_{PV}	Port Output From ALE (Note 1)	3/10 t_{CY} + 100		510	ns
t_{CY}	Cycle Time (Note 3)		1.36	15	μs
t_{OPRR}	T_0 Rep Rate	3/15 t_{CY}	270		ns

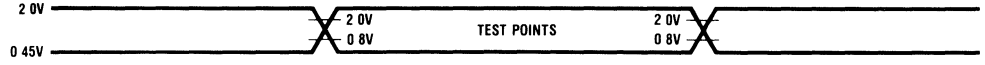
Note 1: Control outputs C_L = 80 pF, Bus outputs C_L = 150 pF

Note 2: Bus High Impedance Load = 20 pF

Note 3: t_{CY} = 15/f (assumes 50% duty cycle)

Note 4: Maximum spec listed is for user information only to prevent system bus contention

Note 5: V_{IH} = 3.8V, V_{IL} = 0.45V

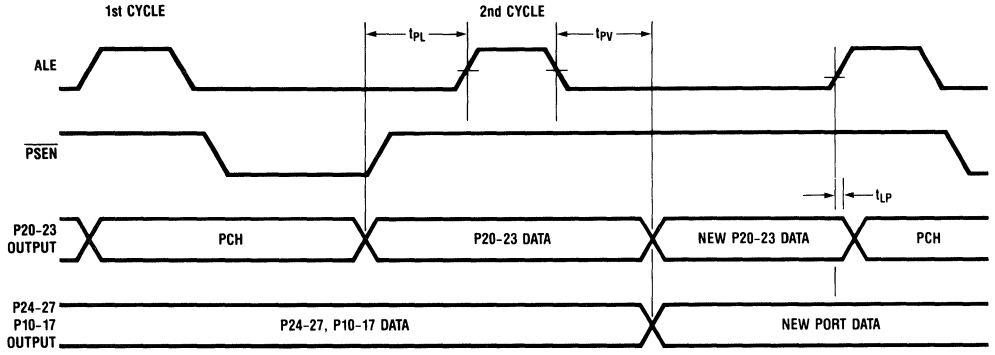


Note: AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0" Output timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0" (except X1, X2, and $\overline{RESET}$) (Note 5)

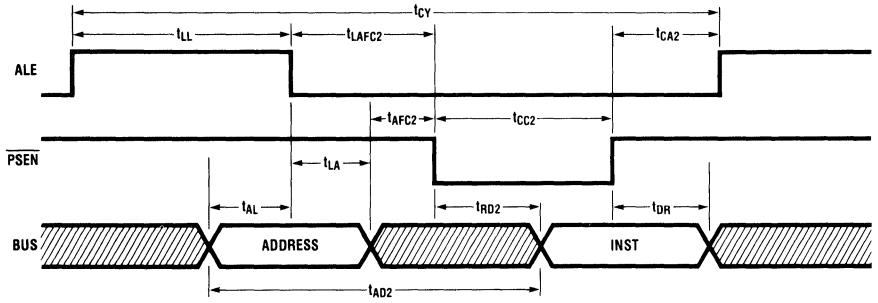
Input and Output for AC Tests

MICRO-PROCESSORS

Timing Waveforms

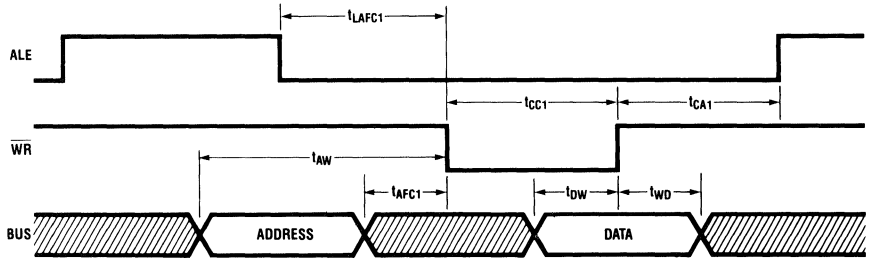


I/O Port Timing



Note: Diagonal lines indicate interval of high impedance

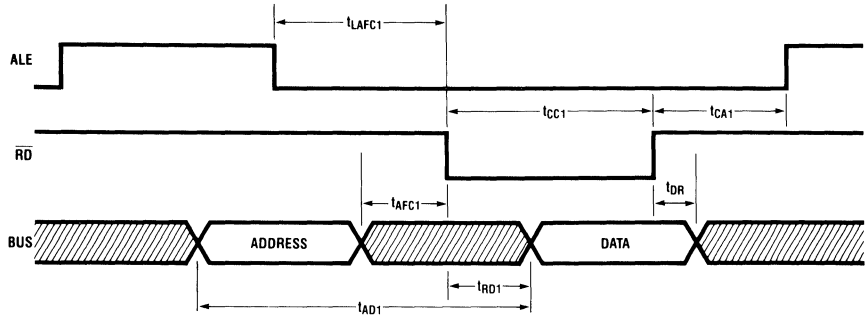
Instruction Fetch from External Program Memory



Note: Diagonal lines indicate interval of high impedance

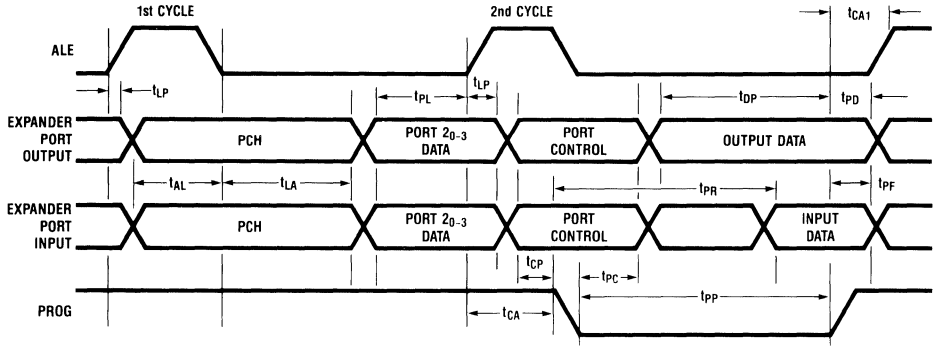
Write to External Data Memory

Timing Waveforms (Continued)

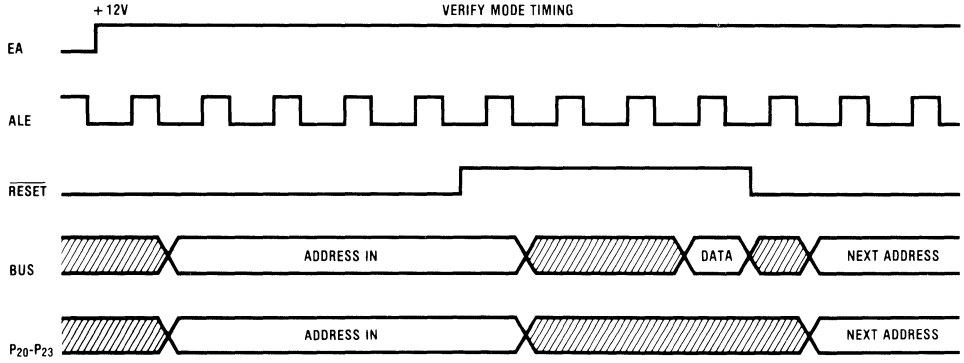


Note: Diagonal lines indicate interval of high impedance

Read from External Data Memory



Port 2 Timing



Recommended Test Methods.

1 $\overline{\text{RESET}}$ must be low before EA goes high
2 Sync to falling edge of ALE. Falling edge of ALE is machine cycle 4
3 Force address in with $\overline{\text{RESET}}$ low for 21 machine cycles starting machine cycle 5
4 Force address in with $\overline{\text{RESET}}$ high for 4 machine cycles
5 Force $\overline{\text{RESET}}$ high for 12 machine cycles
6 Force $\overline{\text{RESET}}$ high for 4 machine cycles. Data is valid on bus
7 Force $\overline{\text{RESET}}$ low for 4 machine cycles
8 Repeat steps 3 through 7 for other addresses

ROM Verify Mode Timing

Typical Application

Figure 8 shows a typical way to use the SY8048 microcontroller in a stand-alone system Crystal used is parallel resonant, AT cut and 1MHz to 6MHz All outputs are standard TTL compatible at 5V

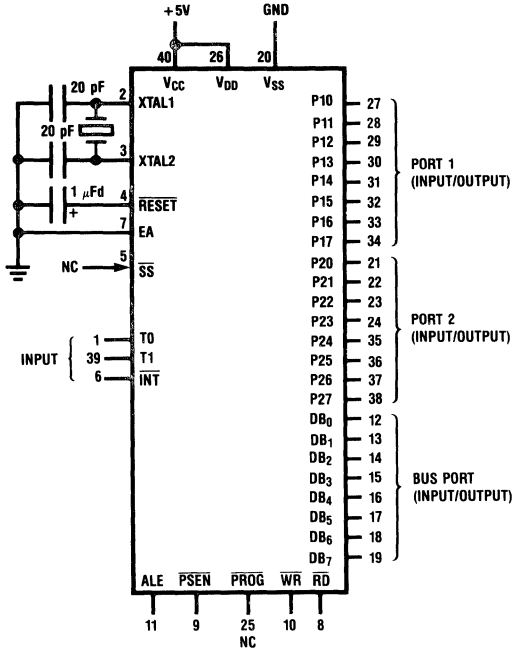


FIGURE 8. Stand-Alone SY8048 System

Package Availability 40 Pin Molded DIP

Synertek.

SY66C016
High-Speed 16 x 16 CMOS Parallel Multiplier

PRELIMINARY

Features

- High-Speed 16 x 16 Parallel Array Multiplier
- 145 nsec Typical Multiply Time
- Low Power (I_{CC} = 30 mA Typical)
- Full Product Multiplexed at Output
- 2's Complement, Unsigned or Mixed Operands
- Input/Output Latches Selectable for Clocked or Transparent Mode of Operation
- Advanced CMOS Technology
- Input/Output Levels TTL Compatible
- Single +5V Power Supply
- 64-Pin Package
- SY66C016 Pin-for-Pin Functional Replacement for TRW TRW MPY 16HJ and AMD 29516

Description

The SY66C016 is a parallel array multiplier built using Synertek's advanced CMOS process technology By use of a modified Booths algorithm and the state-of-the-art 2 μ design rules, the SY66C016 provides a performance comparable to existing bipolar TTL multipliers at a fraction of the power consumption (I_{CC} = 30 mA typical)

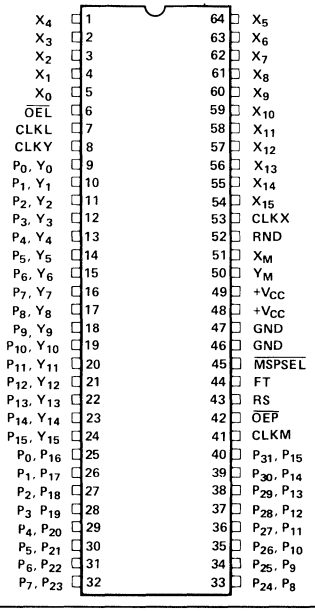
Input data is accepted in the form of 16-bit 2's complement and unsigned magnitude or mixed operands. At the output of the array a format adjust control (FA) allows the user to select a full 32-bit product or a left shifted 31-bit product suitable for 2's-complement only.

The two halves of the product may be routed to a 16-bit three-state output port via a multiplexer. In addition, the LSP is connected to the Y-input through a separate three-state buffer.

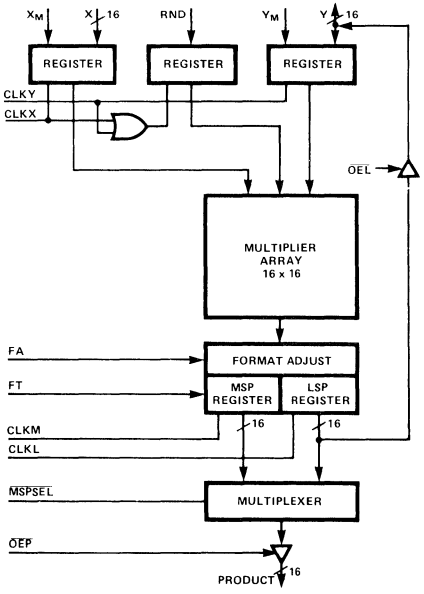
Applications of the SY66C016 multiplier include a variety of digital signal-processing systems including floating-point processors, FFT processors, array processors, image/video processors, speech recognition and synthesis, digital filtering, modems, missile guidance, etc.

In the SY66C016 the X, Y, MSP and LSP registers have independent clocks (CLKX, CLKY, CLKM, CLKL). The output multiplexer control ($\overline{\text{MSPSEL}}$) uses a pin which is a supply ground in the TRW MPY 16HJ. When this control is LOW the function is that of the MPY 16HJ, thus allowing full compatibility.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage, V_{CC} ..... −0.3V to +7.0V
Input/Output Voltage, V_{IN} ..... −0.3V to +7.0V
Operating Temperature, T_{OP} ..... 0 to 70°C
Storage Temperature, T_{STG} ..... −55°C to +150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Comment*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics (V_{CC} = −5.0V ±5%, V_{SS} = 0, T_A = 0 to 70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{LI}	Input Leakage Current (V_{CC} = 5V)			10	μA
I_{LO}	Output Leakage Current (3-State: V_{CC} = 0.4V)			−10	μA
I_{LO}	Output Leakage Current (3-State: V_{CC} = 2.4V)			20	μA
V_{OH}	Output High Voltage (V_{CC} = Min., I_{OH} = −100μA)	2.4			V
V_{OL}	Output Low Voltage (V_{CC} = Min., I_{OL} = 1.6μA)			0.4	V
I_{CC}	Supply Current (V_{CC} = 5.25V		300	400	mA

Pin Description

X_0-X_{15}
These 16 lines are the Multiplicand and Data inputs. Data are loaded on the rising edge of CLKX.

Y_0-Y_{15}
These 16 pins share functions between the Multiplier Data inputs (Y_0-Y_{15}) and least significant product, LSP (P_0-P_{15}), outputs. The input data are loaded on the rising edge of CLKY. The output (LSP) data are loaded on the rising edge of CLKL.

X_M, Y_M
Mode control inputs for each data word.

(TCX, TCY)*
X_M,Y_M = 0; unsigned data
X_M,Y_M = 1; 2's complement data
X_M is clocked by CLKX; Y_M is clocked by CLKY.

FA (RS)*
Format Adjust control selects either a full 32-bit product (HIGH) or a left shifted 31-bit product with the sign bit replicted in the LSP (LOW). This control is normally high except for certain fractional 2's complement applications.

FT
Feedthrough control (HIGH) makes both MSP and LSP registers transparent.

$\overline{\text{MSPSEL}}$
Selects either MSP (LOW) or LSP (HIGH) to be available at the product output port.

RND
Round control for the rounding of the MSP by adding 1 to the least significant product output. RND is strobed by CLKX or CLKY.

$\overline{\text{OEP}}$ (TRIM)*
Three-state enable for product output (MSP) port.

$\overline{\text{OEL}}$ (TRIL)*
Three-state enable for routing LSP through Y input/output port.

CLKX
Register Clock for X_0-X_{15}, X_M, RND

CLKY
Register Clock for Y_0-Y_{15}, Y_M, RND

CLKM
MSP Register Clock

CLKL
LSP Register Clock

*TRW MPY 16HJ pin designation.

Synertek.

SY4x2901B
16-bit CMOS Microprocessor Slice

ADVANCED INFORMATION

Distinctive Characteristics

- Quad Replacement for 2901B with On-board Look-ahead Carry Generation
- Extremely Low Power Consumption
- Full TTL Compatibility
- Single +5 V Power Supply
- Expandable
  — Any number of SY4x2901Bs can be cascaded together to form longer word lengths[1]
- Speed
  — 100 ns cycle time (typical)
- Eight-function ALU
  — Performs addition, two subtraction operations, and five logic operations
- Two-address Architecture
  — Independent simultaneous access to two working registers saves machine cycles
- Flexible Data Source Selection
  — ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function
- Left/right Shift Independent of ALU
  — ADD and SHIFT operations take only one cycle
- Microprogrammable
  — Three groups of three bits each for source operand, ALU function, and destination control
- Four STATUS FLAGS
  — Carry, overflow, zero, and negative
- Operating Range
  — Both commercial and military temperature ranges available
- Packaging
  — 64-pin Molded and Ceramic DIP
  — 68-pin ceramic leadless chip carrier

Description

The SY4x2901B is a CMOS Quad implementation of the industry standard 2901B 4-bit microprocessor slice with on-board multilevel look-ahead carry generation capability It is designed to provide a high-speed cascadable ALU, intended for use in CPUs, peripheral controllers, programmable microprocessors, or any application where performance and hardware/software flexibility are system prerequisites

The SY4x2901B provides all the features of its bipolar counterparts, in addition to the inherent advantages of its low power requirements, 16-bit data I/O, and on-board look-ahead carry capabilities. It is also microcode compatible with the 2901B This is a definite advantage, since existing software can be utilized in a new or upgraded hardware design The microinstruction flexibility of this device will allow efficient emulation of almost any digital computing machine. In addition, it also has three-state outputs and provides various STATUS FLAG outputs from the ALU

(continued on next page)

Block Diagram

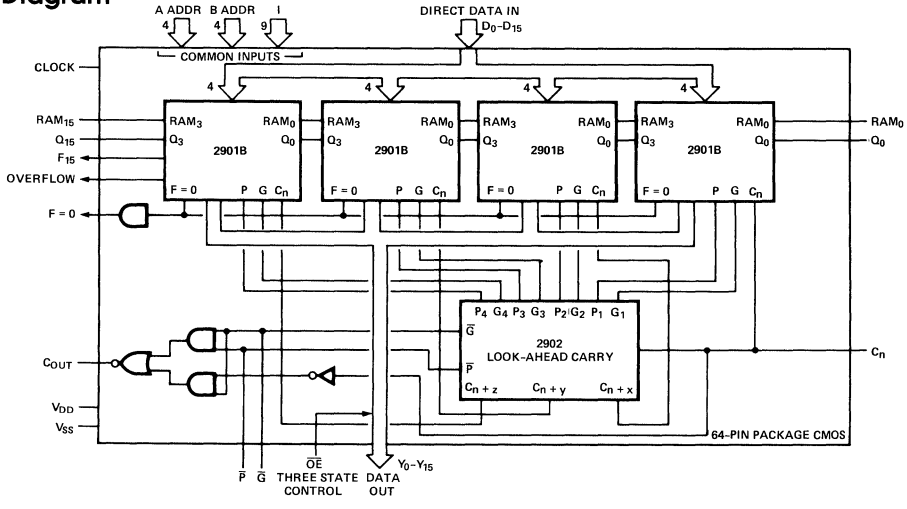


Figure 1. SY4x2901B General Block Diagram

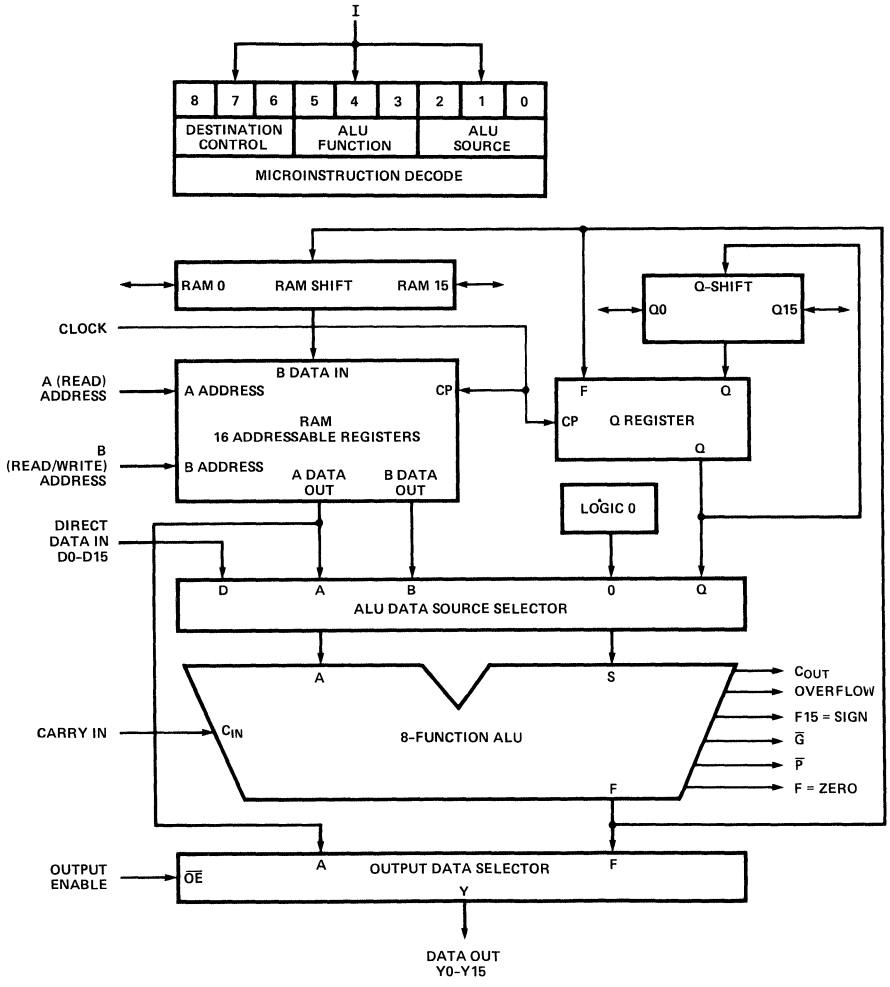


Figure 2. Functional Block Diagram

The SY4x2901B, as shown in Figure 1, consists of four 4-bit 2901s, and one and one-quarter 2902s As shown in Figure 2, the device consists of a 16-word by bit two-port RAM, and eight function ALU, and the associated shifting, decoding, and multiplexing circuitry The 9-bit microinstruction word is organized into three groups of three bits each which select the ALU source operands, the ALU functions, and the ALU destination register

The partial 2902 (Figure 1) is provided so as to reduce chip count when implementing either a 24-bit or 32-bit design. The three signals provided by the look-ahead carry circuitry are C_{OUT}, propagate (P), and generate (G). Moreover, C_{OUT} is the only carry signal needed when cascading with either a SY2x2901B[1], or another SY4x2901B device (24-bit and 32-bit configurations respectively) — thus eliminating the need for an additional look-ahead carry device For system configurations greater than 32-bits, the carry propagate and generate signals can be used This on-board look-ahead carry capability provides the user with a truly economical and versatile alternative for design

Note 1:
The SY2x2901B is an 8-bit CMOS processor slice which is available in a 48-pin package The SY2x2901B may be cascaded with a SY4x2901B to form word lengths in any multiple of 8-bits

Pin Definitions

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678})

Q_{15} RAM_{15} A shift line at the MSB of the Q register (Q_{15}) and the register stack (RAM_{15}) Electrically these lines are three-state outputs connected to TTL inputs internal to the device When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_{15} and RAM_{15}, but at the LSB of the Q-register and RAM. These pins are tied to the Q_{15} and RAM_{15} pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-15} Direct data inputs A 16-bit data field which may be selected as one of the ALU data sources for entering data into the device D_0 is the LSB.

Y_{0-15} The 16 data outputs. These are three-state output lines. When enabled, they display either the 16 outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}

$\overline{OE}$ Output Enable When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW)

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals can be used with another 2902 for carry-lookahead of word lengths greater than 32-bits

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open drain output which goes HIGH (OFF) if the data on the 16 ALU outputs F_{0-15} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_{15} The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{OUT} The carry-out of the SY4x2901B.

CP The clock input The Q register and register stack outputs change on the clock LOW-to-HIGH transition The clock LOW time is internally the write enable to the 16 x 4 RAM.

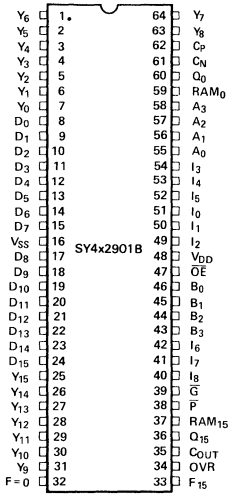
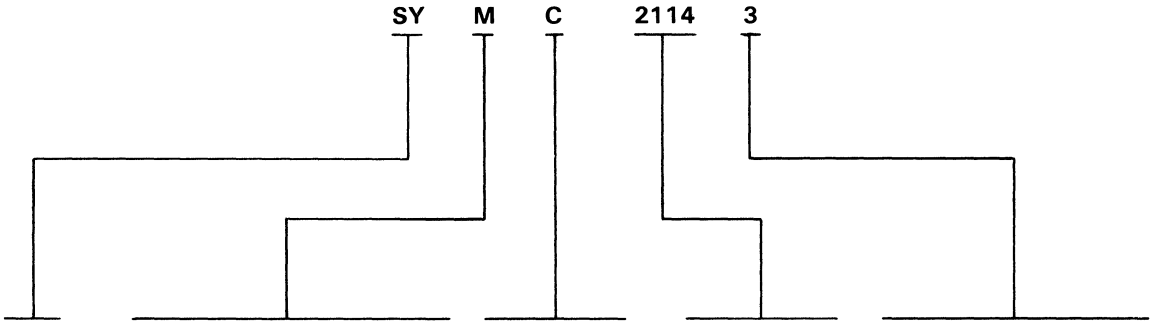


Figure 3. Pin Configuration

General Information. 5

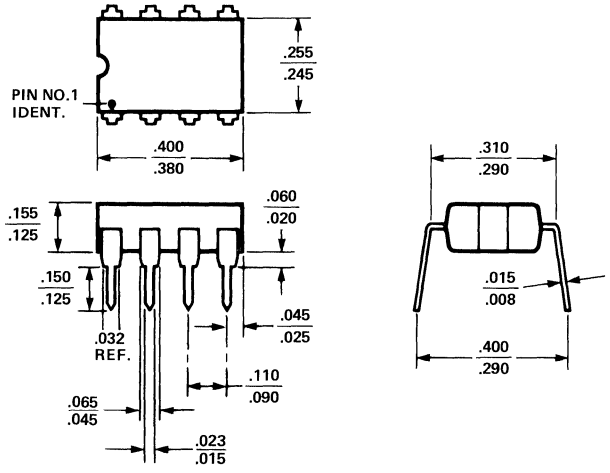
Ordering Information



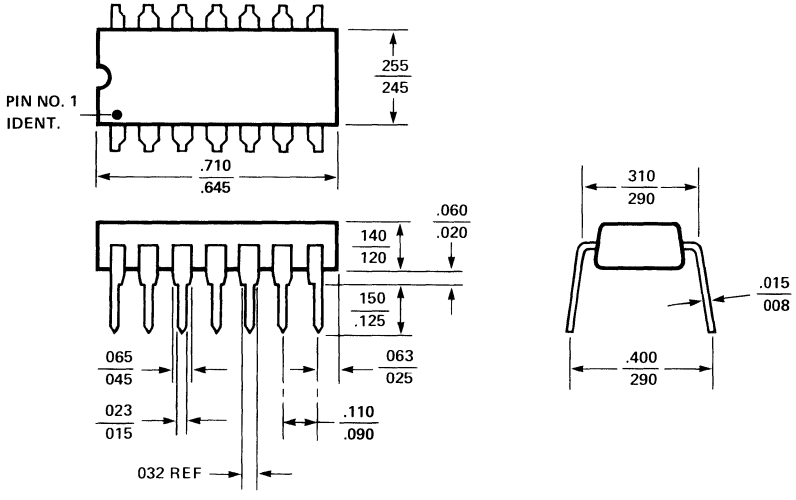
Please make note of the Leadless Chip Carrier (LCC) designator.

Packaging Information

Molded DIP—
8 Leads



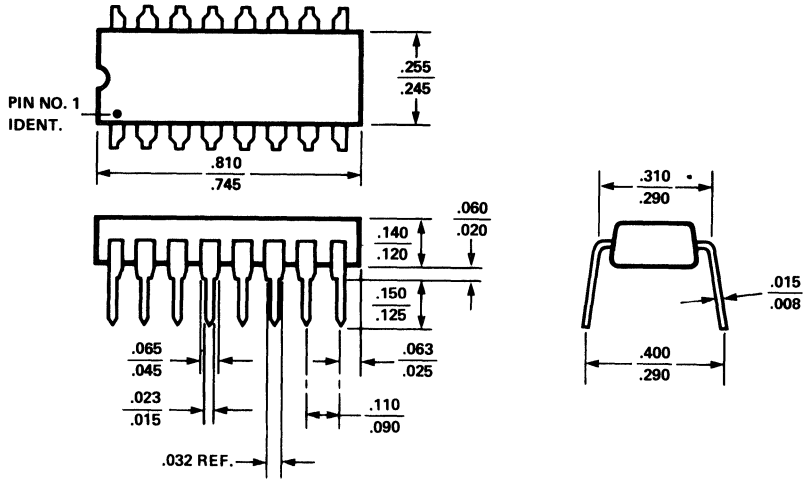
Molded DIP—
14 Leads



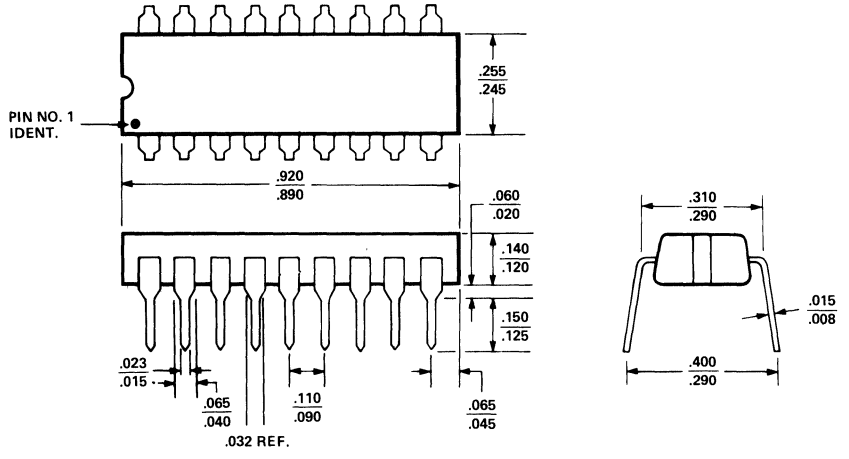
GENERAL INFORMATION

Packaging Information

Molded DIP—
16 Leads

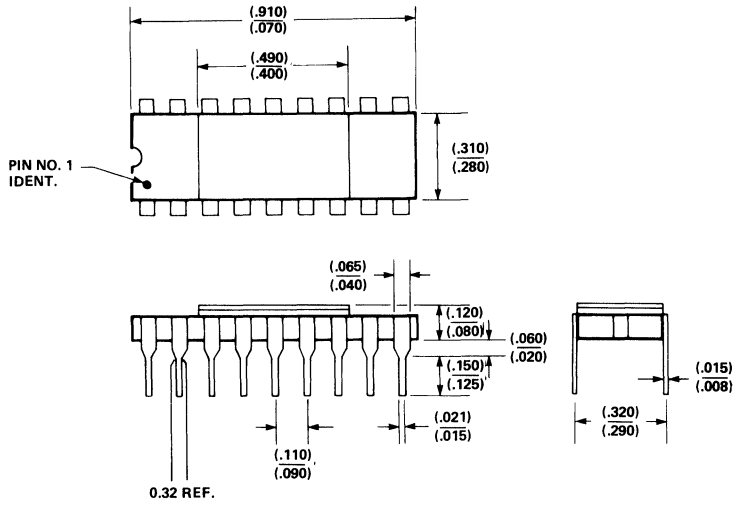


Molded DIP—
18 Leads

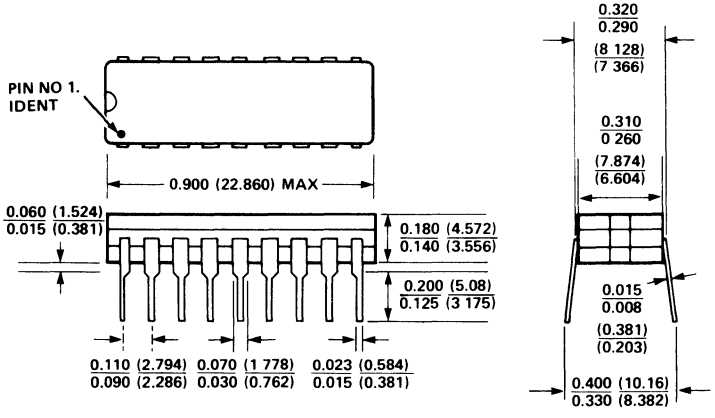


Packaging Information

Ceramic—
18 Leads



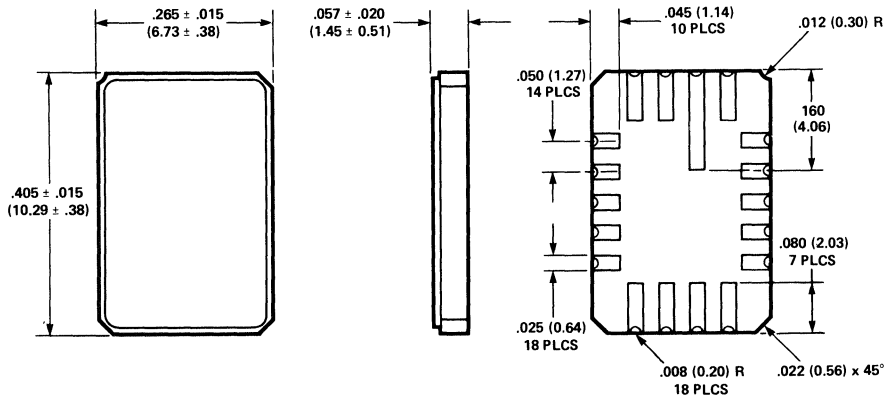
Cerdip—
18 Leads



GENERAL INFORMATION

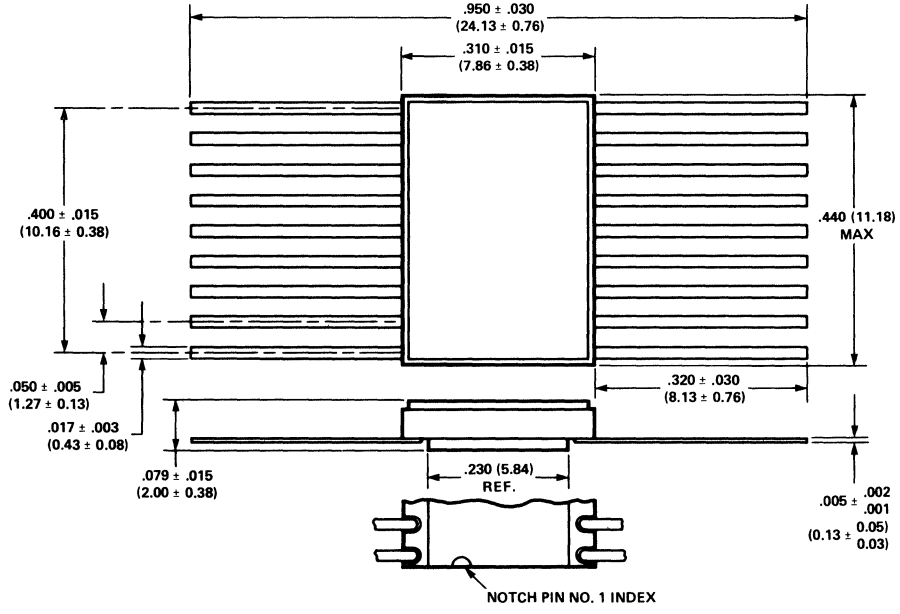
Packaging Information

Chip Carrier—
18 Leads



DIMENSIONS IN INCHES AND (MILLIMETERS).

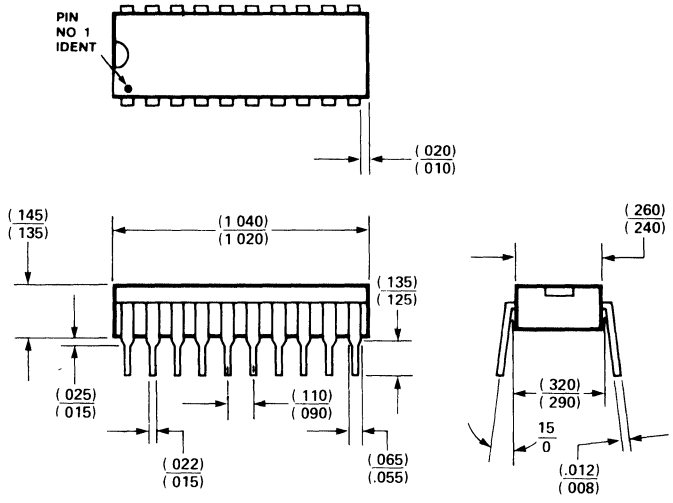
Flat Package—
18 Leads



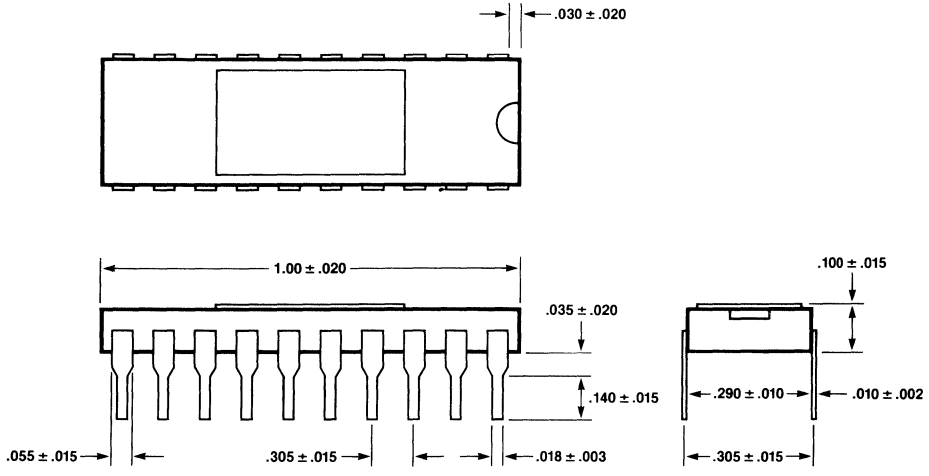
DIMENSIONS IN INCHES AND (MILLIMETERS).

Packaging Information

Molded DIP—
20 Leads

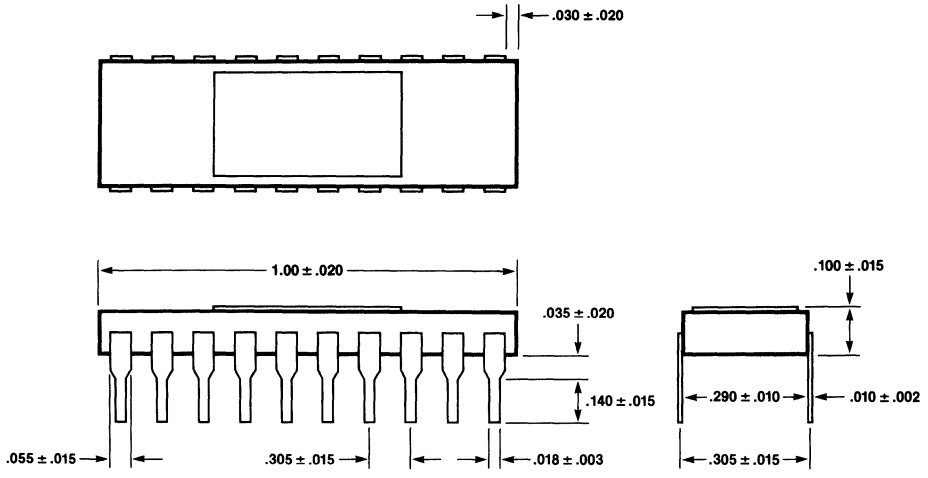


Ceramic—
20 Leads

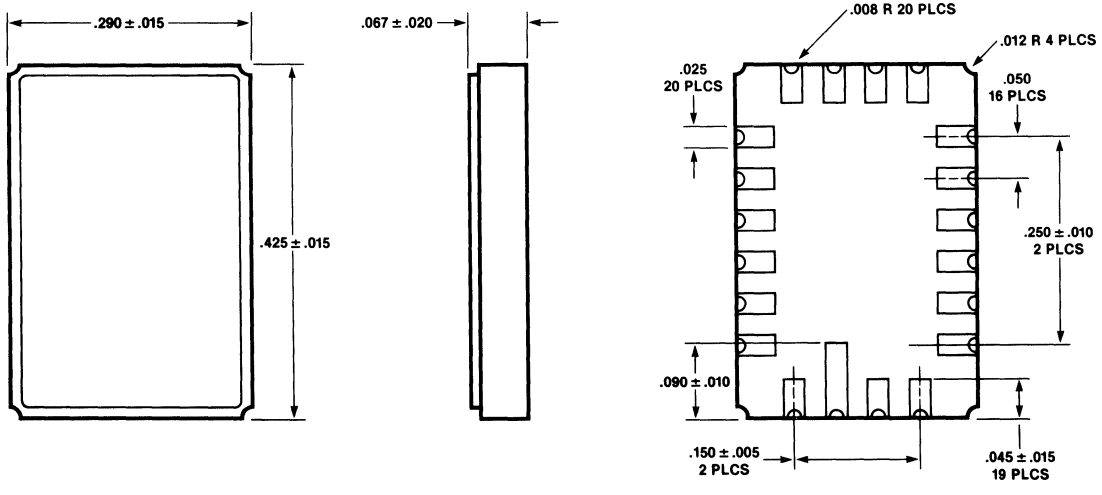


Packaging Information

Cerdip—
20 Leads

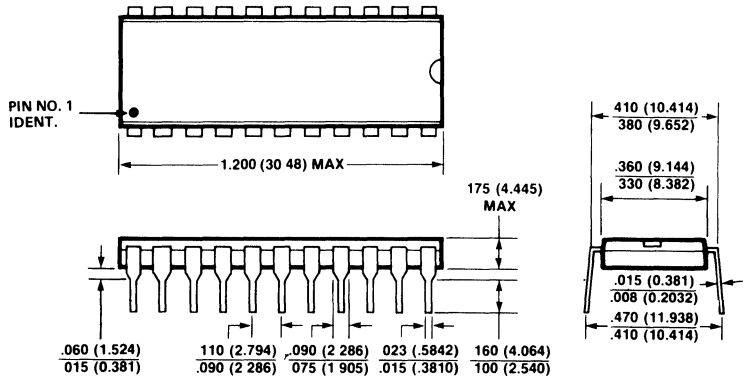


Chip Carrier—
20 Leads



Packaging Information

Molded DIP—
22 Leads



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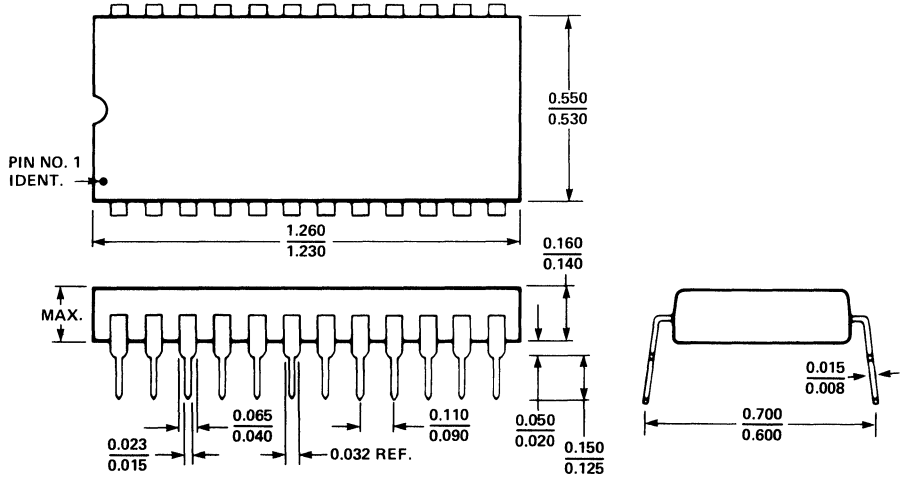
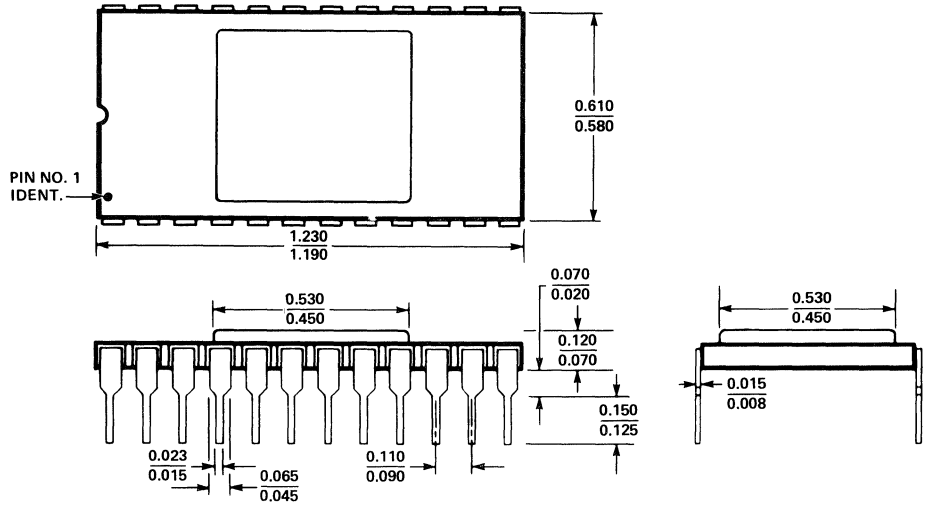
24 Leads

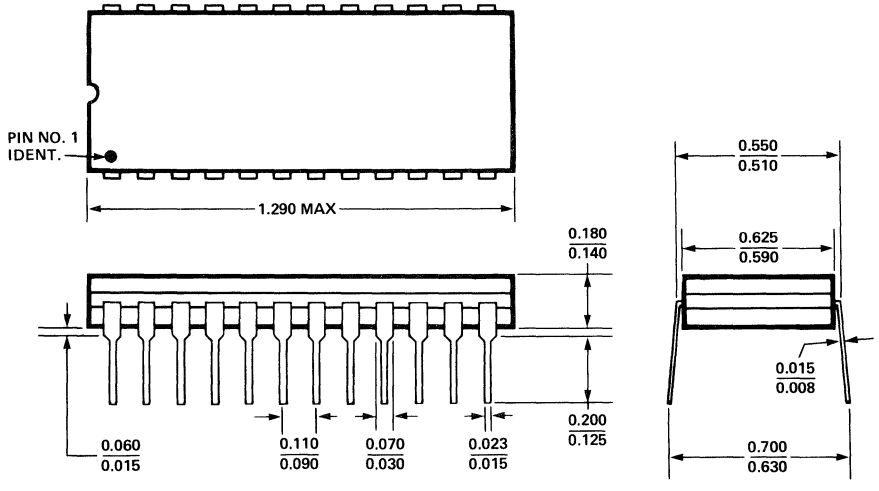


Packaging Information

Ceramic—
24 Leads



Cerdip—
24 Leads



Packaging Information

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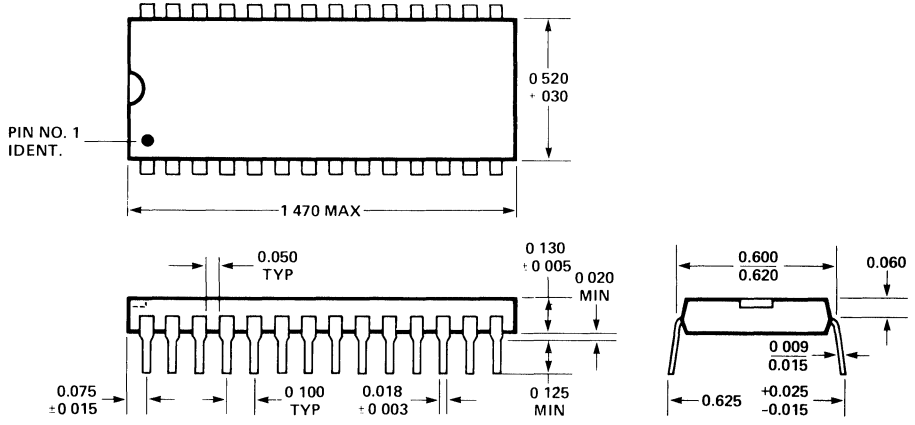
28 Leads



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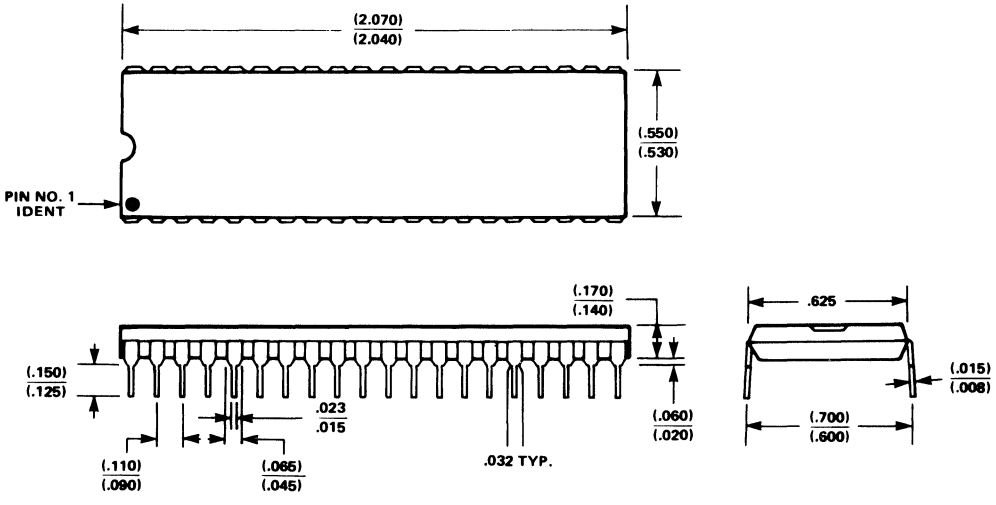
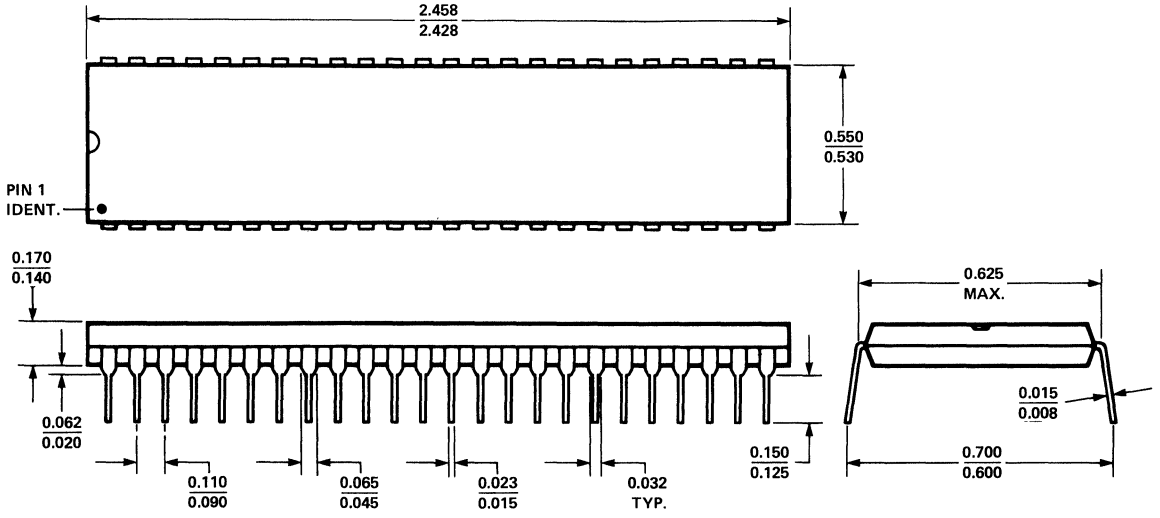
40 Leads



GENERAL INFORMATION

Packaging Information

Molded DIP—
48 Leads



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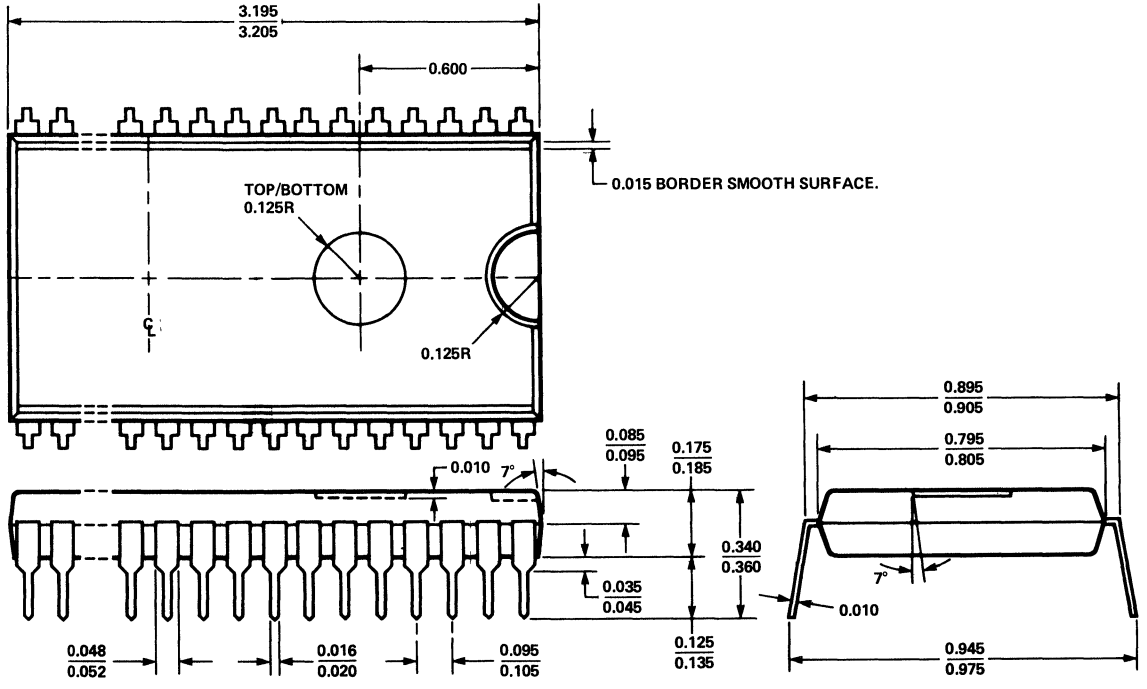
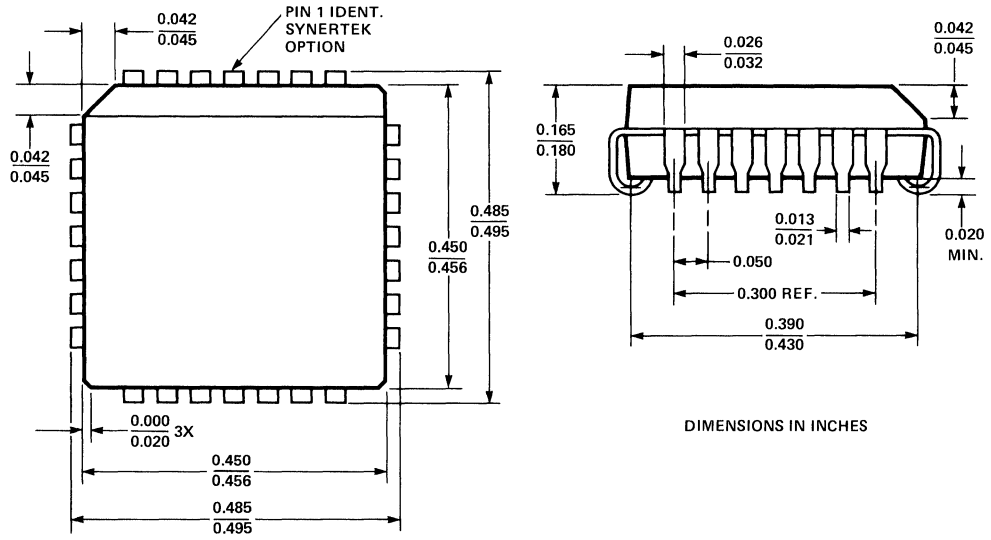
64 Leads



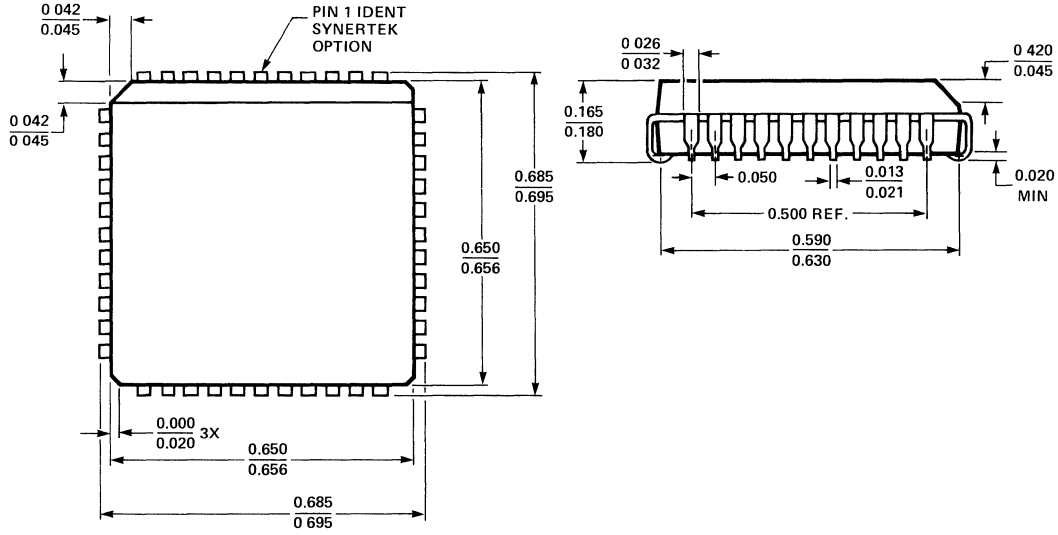
Packaging Information

Surface Mounted Device—
28 Leads *



DIMENSIONS IN INCHES

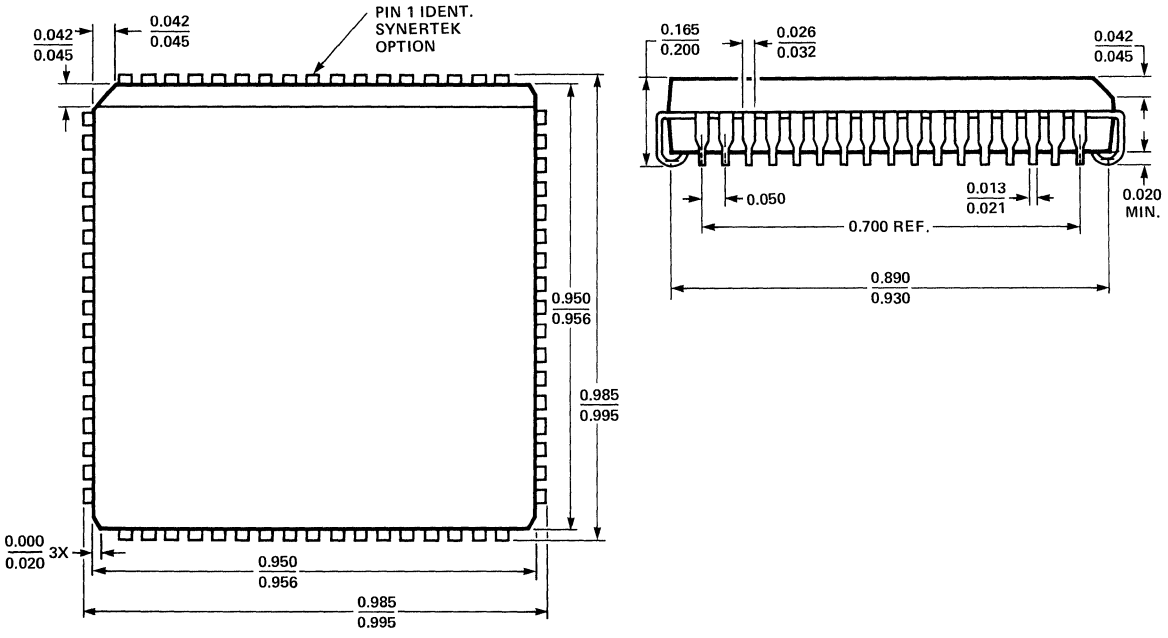
Surface Mounted Device—
44 Leads *



*Available second half '85

Packaging Information

Surface Mounted Device—
68 Leads*



*Available second half '85

Synertek Application Notes

Below is a listing of Synertek Applications Information available. These Notes are available in their entirety from your local Synertek Sales Office, nearest Sales Representative, or Distributor.

Microprocessor Application Notes

Application Note Number	Title
AN1	SY6551 Asynchronous Communications Interface Adapter (ACIA)
AN2	SY6500 Microprocessor Family
AN5	SY6522 Versatile Interface Adapter (VIA)
AN7	SY6845 Smooth Scrolling with the 6545
AN8	SY6845 CRTC Design and Applications Manual
AN10	SY2661 EPCI Implements Binary Synchronous Protocol
AN11	SY66016 High Speed 16 x 16 Parallel Multiplier

Memory Application Notes

Application Note Number	Title
AN6	SY2128/2129 2K x 8-Bit Static RAM Access Memory
AN12	SY2130/2131 1024 x 8 Dual Port Random Access Memory

Conversion Tables

1. Convert Hexadecimal to Decimal

$1AF6_{16} = 1 \times 16^3 + A \times 16^2 + F \times 16^1 + 6 \times 16^0 = 4096 + 2560 + 240 + 6 = 6902_{10}$

2. Convert Octal to Decimal

$2147_8 = 2 \times 8^3 + 1 \times 8^2 + 4 \times 8^1 + 7 \times 8^0 = 1024 + 64 + 32 + 7 = 1127$

3. Convert Binary to Decimal

$101101_2 = 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 32 + 0 + 8 + 4 + 1 = 45_{10}$

4. Convert Decimal to Hexadecimal

$1207_{10} \rightarrow$

$$\begin{array}{r} 0 \\ 16^3 \overline{)\,1207} \\ 0 \\ \hline 1207 \end{array} \rightarrow \begin{array}{r} 4 \\ 16^2 \overline{)\,1207} \\ 1024 \\ \hline 183 \end{array} \rightarrow \begin{array}{r} B \\ 16^1 \overline{)\,183} \\ 176 \\ \hline 7 \end{array} \rightarrow \begin{array}{r} 7 \\ 16^0 \overline{)\,7} \\ \end{array} = 4B7_{16}$$

5. Convert Decimal to Octal

$153_{10} \rightarrow$

$$\begin{array}{r} 2 \\ 8^2 \overline{)\,153} \\ 128 \\ \hline 25 \end{array} \rightarrow \begin{array}{r} 3 \\ 8^1 \overline{)\,25} \\ 24 \\ \hline 1 \end{array} \rightarrow \begin{array}{r} 1 \\ 8^0 \overline{)\,1} \\ \end{array} = 231_8$$

6. Convert Decimal to Binary

$53_{10} \rightarrow$

$$\begin{array}{r} 1 \\ 2^5 \overline{)\,53} \\ 32 \\ \hline 21 \end{array} \rightarrow \begin{array}{r} 1 \\ 2^4 \overline{)\,21} \\ 16 \\ \hline 5 \end{array} \rightarrow \begin{array}{r} 0 \\ 2^3 \overline{)\,5} \\ 0 \\ \hline 5 \end{array} \rightarrow \begin{array}{r} 1 \\ 2^2 \overline{)\,5} \\ 4 \\ \hline 1 \end{array} \rightarrow \begin{array}{r} 0 \\ 2^1 \overline{)\,1} \\ 0 \\ \hline 1 \end{array} \rightarrow \begin{array}{r} 1 \\ 2^0 \overline{)\,1} \\ 1 \\ \hline 0 \end{array} = 110101_2$$

Recommended Decimal Multiples and Submultiples

Multiples and Submultiples	Prefixes	Symbols
10^{18}	exa	E
10^{15}	pecta	P
10^{12}	tera	T
10^{9}	gıga	G
10^{6}	mega	M
10^{3}	kılo	k
10^{2}	hecto	h
10	deca	da
10^{-1}	deci	d
10^{-2}	centi	c
10^{-3}	milli	m
10^{-6}	micro	μ (greek mu)
10^{-9}	nano	n
10^{-12}	pico	p
10^{-15}	femto	f
10^{-18}	atto	a

Conversion Tables (cont)

Constants and Conversion Factors

Conversion Factors — General

To Obtain	Multiply	By
Degree (angle)	Radians	57 2958
Ergs	Foot-pounds	$1\ 356 \times 10^{7}$
Feet	Miles	**5280**
Feet of water @ 4°C	Atmospheres	33.90
Foot-pounds	Horsepower-hours	1.98×10^{6}
Foot-pounds	Kilowatt-hours	$2\ 655 \times 10^{6}$
Foot-pounds per min	Horsepower	$3\ 3 \times 10^{4}$
Horsepower	Foot-pounds per sec	1.818×10^{-3}
Inches of mercury @ 0 °C	Pounds per square inch	2 036
Joules	BTU	1054.8
Joules	Foot-pounds	1 35582
Kilowatts	BTU per min	1.758×10^{-2}
Kilowatts	Foot-pounds per min.	2.26×10^{-5}
Kilowatts	Horsepower	0.745712
Knots	Miles per hour	0.86897624
Miles	Feet	1.894×10^{-4}
Nautical miles	Miles	0.86897624
Radians	Degrees	1.745×10^{-2}
Square feet	Acres	**43560**
Watts	BTU per min	17.5796

Temperature Factors

$$°F = 9/5\ (°C) + 32$$

Fahrenheit temperature — 1.8 (temperature in kelvins) -459.67

$$°C = 5/9\ [(°F) - 32]$$

Celsius temperature = temperature in kelvins — 273.15
Fahrenheit temperature = 1 8 (Celsius temperature) + 32

*Boldface numbers are exact, others are given to ten significant figures where so indicated by the multiplier factor

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Conversion Factors — Metric to English

To Obtain	Multiply	By
Inches	Centimeters	0 3937007874
Feet	Meters	3.280839895
Yards	Meters	1 093613298
Miles	Kilometers	0.6213711922
Ounces	Grams	$3\ 527396195 \times 10^{-2}$
Pounds	Kilograms	2.204622622
Gallons (U.S Liquid)	Liters	0.2641720524
Fluid ounces	Milliliters (cc)	$3.381402270 \times 10^{-2}$
Square inches	Square centimeters	0.1550003100
Square feet	Square meters	10.76391042
Square yards	Square meters	1.195990046
Cubic inches	Milliliters (cc)	$6\ 102374409 \times 10^{-2}$
Cubic feet	Cubic meters	35.31466672
Cubic yards	Cubic meters	1.307950619

Conversion Tables (cont.)

Conversion Factors — English to Metric*

To Obtain	Multiply	By
Microns	Mils	**25.4**
Centimeters	Inches	**2.54**
Meters	Feet	**0.3048**
Meters	Yards	**0.9144**
Kilometers	Miles	**1.609344**
Grams	Ounces	28.34952313
Kilograms	Pounds	**0.45359237**
Liters	Gallons (U.S Liquid)	**3.785411784**
Milliliters (cc)	Fluid ounces	29.57352956
Square centimeters	Square inches	**6.4516**
Square meters	Square feet	**0.09290304**
Square meters	Square yards	**0.83612736**
Milliliters (cc)	Cubic inches	**16.387064**
Cubic meters	Cubic feet	$2.831684659 \times 10^{-2}$
Cubic meters	Cubic yards	0.764554858

Conversion Factors — General*

To Obtain	Multiply	By
Atmospheres	Feet of water @ 4°C	$2\,950 \times 10^{-2}$
Atmospheres	Inches of mercury @ 0°C	3.342×10^{-2}
Atmospheres	Pounds per square inch	6.804×10^{-2}
BTU	Foot-pounds	$1\,285 \times 10^{-3}$
BTU	Joules	$9\,480 \times 10^{-4}$
Cubic feet	Cords	**128**

*Boldface numbers are exact, others are given to ten significant figures where so indicated by the multiplier factor

Miscellaneous Constants

Physical Constants

Equatorial radius of the earth = 6378 388 km = 3963.34 miles (statute)
Polar radius of the earth, 6356.912 km = 3949.99 miles (statute)
1 degree of latitude at 40° = 69 miles.
1 international nautical mile = 1.15078 miles (statute) = 1852 m = 6076 115 ft.
Mean density of the earth = 5 522 g/cm^3 = 344.7 lb/ft^3.
Constant of gravitation, $(6\,673 \pm 0\,003) \times 10^{-8}$ cm^3 gm^{-1} S^{-2}
Acceleration due to gravity at sea level, latitude 45° = 980.665cm/s^2 = 32 1740 ft/sec^2
Length of seconds pendulum at sea level, latitude 45° = 99 3574 cm = 39 1171 in
1 knot (international) = 101 269 ft/min = 1.6878 ft/sec = 1.1508 miles (statute)/hr.
1 micron = 10^{-4} cm
1 angstrom = 10^{-8} cm.
Mass of hydrogen atom = $(1.67339 \pm 0\,0031) \times 10^{-24}$ g.
Density of mercury at 0°C = 13.5955 g/ml.
Density of water at 3 98°C = 1 000000 g/ml
Density, maximum, of water, at 3.98°C = 0.999973 g/cm^3
Density of dry air at 0°C, 760 mm = 1 2929 g/liter.
Velocity of sound in dry air at 0°C = 331 36 m/s — 1087 1 ft/sec.
Velocity of light in vacuum = $(2\,997925 \pm 0.000002) \times 10^{10}$ cm/s
Heat of fusion of water 0°C = 79.71 cal/g
Heat of vaporization of water 100°C = 539 55 cal/g.
Electrochemical equivalent of silver 0 001118 g/sec international amp
Absolute wave length of red cadmium light in air at 15°C, 760 mm pressure = 6438 4696 A
Wave length of orange-red line of krypton 86 = 6057 802 A

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