TMS320C2x
DIGITAL SIGNAL PROCESSOR
Programmer's Reference Card

TEXAS INSTRUMENTS

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Instruction Symbols

Symbol	Meaning
AR	Auxiliary register
ARP	Auxiliary register pointer
B	Bit code
BR	Branch address
D	data memory address or indirect addressing control bits (see below)
dma	Data memory address
I	Indirect/direct addressing mode 1 = indirect; 0 = direct addressing
ind	Indirect address: {*|*+|*-|*0+|*0-} for '20; {*|*+|*-|*0+|*0-|*BR0+|*BR0-} for 'C25
K	Immediate value
PA	Port address
pma	Program memory address
S	Shift count
< >	User-defined items
[ ]	Optional items

Status Register ST0 Bits

15-13	12	11	10	9	8 7 6 5 4 3 2 1 0
ARP	OV	OVM	1	NTM	DP

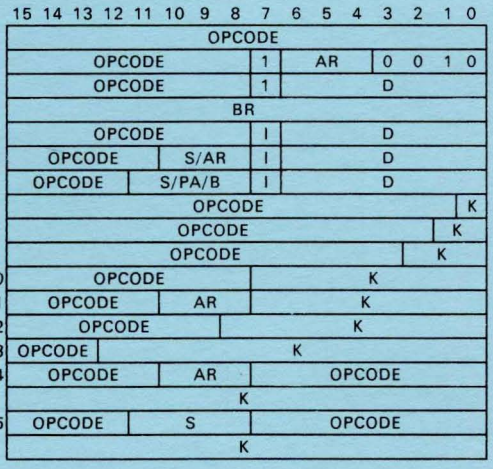
Status Register ST1 Bits

ARB	CNF	TC	SXM	C	1	1	HM	FSM	XF	FO	TXM	PM

NOTE: On the TMS32020, bits 5, 6, and 9 of ST1 are one's.

ARP	Auxiliary register pointer
OV	Accumulator overflow flag bit
OVM	Overflow mode bit
INTM	Interrupt mask bit
DP	Data memory page pointer
ARB	Auxiliary register pointer buffer
CNF	On-chip RAM configuration control bit
TC	Test/control flag bit
SXM	Sign-extension mode bit
C	Carry bit
HM	Hold mode bit
FSM	Frame synchronization mode bit
XF	XF pin status bit
FO	Format bit
TXM	Transmit mode bit
PM	Product shift mode bits

Instruction Format Description



Indirect Addressing Control Bits

6	5	4	3	2 1 0
IDV	INC	DEC	NAR	next ARP

IDV	Increment/decrement value
INC	Increment flag; 1 increments auxiliary register
DEC	Decrement flag; 1 decrements auxiliary register
NAR	New auxiliary register control bit; 1 loads new ARP
ARP	Auxiliary register pointer

6	5	4	Operation	6	5	4	Operation
0	0	0	*	1	0	0	*BR0-
0	0	1	*-	1	0	1	*0-
0	1	0	*+	1	1	0	*0+
0	1	1	Not used	1	1	1	*BR0+

Instruction Set Summary

Instr	Description	Cyc†/Wd	Operand Options	Opcode	Format
ABS	Absolute value of accumulator	1/1	None	0CE1Bh	1
ADD	Add to accumulator with shift	1/1	<dma>[,<shift>] <ind>[,<shift>[,<next ARP>]]	00000h	6
ADDC	Add to accumulator with carry	1/1	<dma>; <ind>[,<next ARP>]	04300h	4
ADDH	Add to high accumulator	1/1	<dma>; <ind>[,<next ARP>]	04800h	4
ADDK	Add to accumulator short immediate	1/1	<constant>	0CC00h	10
ADDS	Add to low accumulator with no sign extension	1/1	<dma> <ind>[,<next ARP>]	04900h	4
ADDT	Add to accumulator with shift specified by T register	1/1	<dma> <ind>[,<next ARP>]	04A00h	4

†Cycles using full-speed, on-chip, external program memory.

Instruction Set Summary (Continued)

Instr	Description	Cyc†/Wd	Operand Options	Opcode	Format
ADLK	Add to accumulator long immediate with shift	2/2	<constant>[,<shift>]	0D002h	15
ADRK	Add to auxiliary register short immediate	1/1	<constant>	07E00h	10
AND	AND with accumulator	1/1	<dma>; <ind>[,<next ARP>]	04E00h	4
ANDK	AND immediate with accumulator with shift	2/2	<constant>[,<shift>]	0D004h	15
APAC	Add P register to accumulator	1/1	None	0CE15h	1
B	Branch unconditionally	3/2	<pma>[,<ind>[,<next ARP>]]	0FF80h	3
BACC	Branch to address specified by accumulator	3/1	None	0CE25h	1
BANZ	Branch on auxiliary register not 0	3/2	<pma>[,<ind>[,<next ARP>]]	0FB80h	3
BBNZ	Branch if TC bit $\neq$ 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F980h	3
BBZ	Branch if TC bit = 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F880h	3
BC	Branch on carry	3/2	<pma>[,<ind>[,<next ARP>]]	05E80h	3
BGEZ	Branch if accumulator $\geq$ 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F480h	3
BGZ	Branch if accumulator > 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F180h	3
BIOZ	Branch on I/O status = 0	3/2	<pma>[,<ind>[,<next ARP]]	0FA80h	3
BIT	Test bit	1/1	<dma>,<bit code> <ind>,<bit code>[,<next ARP>]	09000h	6
BITT	Test bit specified by T register	1/1	<dma>; <ind>[,<next ARP>]	05700h	4
BLEZ	Branch if accumulator $\leq$ 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F280h	3
BLKD	Block move from data memory to data memory	4/2	<dma1>,<dma2> <dma1>,<ind>[,<next ARP>]	0FD00h	4
BLKP	Block move from program memory to data memory	4/2	<pma>,<dma> <pma>,<ind>[,<next ARP>]	0FC00h	4
BLZ	Branch if accumulator < 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F380h	3
BNC	Branch on no carry	3/2	<pma>[,<ind>[,<next ARP>]]	05F80h	3
BNV	Branch on no overflow	3/2	<pma>[,<ind>[,<next ARP>]]	0F780h	3
BNZ	Branch if accumulator $\neq$ 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F580h	3
BV	Branch on overflow	3/2	<pma>[,<ind>[,<next ARP>]]	0F080h	3
BZ	Branch if accumulator = 0	3/2	<pma>[,<ind>[,<next ARP>]]	0F680h	3
CALA	Call subroutine indirect	3/1	None	0CE24h	1
CALL	Call subroutine	3/2	<pma>[,<ind>[,<next ARP>]]	0FE80h	3
CMPL	Complement accumulator	1/1	None	0CE27h	1
CMPR	Compare auxiliary register with AR0	1/1	<constant>	0CE50h	8
CNFD	Configure block as data memory	1/1	None	0CE04h	1
CNFP	Configure block as program memory	1/1	None	0CE05h	1
DINT	Disable interrupt	1/1	None	0CE01h	1
DMOV	Data move in data memory	1/1	<dma>; <ind>[<next ARP>]	05600h	4
EINT	Enable interrupt	1/1	None	0CE00h	1
FORT	Format serial port registers	1/1	<constant>	0CE0Eh	7
IDLE	Idle until interrupt	3/1	None	0CE1Fh	1
IN	Input data from port	2/1	<dma>,<PA> <ind>,<PA>[,<next ARP>]	08000h	6
LAC	Load accumulator with shift	1/1	<dma>[,<shift>] <ind>[,<shift>[,<next ARP>]]	02000h	6
LACK	Load accumulator immediate	1/1	<constant>	0CA00h	10
LACT	Load accumulator with shift specified by T register	1/1	<dma> <ind>[,<next ARP>]	04200h	4
LALK	Load accumulator long immediate with shift	2/2	<constant>[,<shift>]	0D001h	15
LAR	Load auxiliary register	1/1	<AR>,<dma> <AR>,<ind>[,<next ARP>]	03000h	5

†Cycles using full-speed, on-chip, external program memory.

Instruction Set Summary (Continued)

Instr	Description	Cyc†/Wd	Operand Options	Opcode	Format
LARK	Load auxiliary register immediate	1/1	<AR>,<constant>	0C000h	11
LARP	Load auxiliary register pointer	1/1	<constant>	05588h	9
LDP	Load data memory page pointer	1/1	<dma>; <ind>[,<next ARP>]	05200h	4
LDPK	Load data memory page pointer immediate	1/1	<constant>	0C800h	12
LPH	Load high P register	1/1	<dma>; <ind>[,<next ARP>]	05300h	4
LRLK	Load auxiliary register long immediate	2/2	<AR>,<constant>	0D000h	14
LST	Load status register ST0	1/1	<dma>; <ind>[,<next ARP>]	05000h	4
LST1	Load status register ST1	1/1	<dma>; <ind>[,<next ARP>]	05100h	4
LT	Load T register	1/1	<dma>; <ind>[,<next ARP>]	03C00h	4
LTA	Load T register and accumulate previous product	1/1	<dma> <ind>[,<next ARP>]	03D00h	4
LTD	Load T register, accumulate previous product, move data	1/1	<dma> <ind>[,<next ARP>]	03F00h	4
LTP	Load T register and store P register in accumulator	1/1	<dma> <ind>[,<next ARP>]	03E00h	4
LTS	Load T register and subtract previous product	1/1	<dma> <ind>[,<next ARP>]	05B00h	4
MAC	Multiply and accumulate	4/2	<pma>,<dma> <pma>,<ind>[,<next ARP>]	05D00h	4
MACD	Multiply and accumulate with data move	4/2	<pma>,<dma> <pma>,<ind>[,<next ARP>]	05C00h	4
MAR	Modify auxiliary register	1/1	<dma>; <ind>[,<next ARP>]	05500h	4
MPY	Multiply (with T register, store product in P register)	1/1	<dma> <ind>[,<next ARP>]	03800h	4
MPYA	Multiply and accumulate previous product	1/1	<dma> <ind>[,<next ARP>]	03A00h	4
MPYK	Multiply immediate	1/1	<constant>	0A000h	13
MPYS	Multiply and subtract previous product	1/1	<dma> <ind>[,<next ARP>]	03B00h	4
MPYU	Multiply unsigned	1/1	<dma>; <ind>[,<next ARP>]	0CF00h	4
NEG	Negate accumulator	1/1	None	0CE23h	1
NOP	No operation	1/1	None	05500h	1
NORM	Normalize contents of accumulator	1/1	<ind>	0CE82h	2
OR	OR with accumulator	1/1	<dma>; <ind>[,<next ARP>]	04D00h	4
ORK	OR immediate with accumulator with shift	2/2	<constant>[,<shift>]	0D005h	15
OUT	Output data to port	1/1	<dma>,<PA> <ind>,<PA>[,<next ARP>]	0E000h	6
PAC	Load accumulator with P register	1/1	None	0CE14h	1
POP	Pop top of stack to low accumulator	1/1	None	0CE1Dh	1
POPD	Pop top of stack to data memory	1/1	<dma>; <ind>[,<next ARP>]	07A00h	4
PSHD	Push data memory value onto top of stack	1/1	<dma> <ind>[,<next ARP>]	05400h	4
PUSH	Push low accumulator onto stack	1/1	None	0CE1Ch	1
RC	Reset carry bit	1/1	None	0CE30h	1
RET	Return from subroutine	3/1	None	0CE26h	1
RFSM	Reset serial port frame synchronization mode	1/1	None	0CE36h	1
RHM	Reset hold mode	1/1	None	0CE38h	1
ROL	Rotate accumulator left	1/1	None	0CE34h	1
ROR	Rotate accumulator right	1/1	None	0CE35h	1
ROVM	Reset overflow mode	1/1	None	0CE02h	1
RPT	Repeat instruction as specified by data memory value	1/1	<dma> <ind>[,<next ARP>]	04B00h	4
RPTK	Repeat instruction as specified by immediate value	1/1	<constant>	0CB00h	10

†Cycles using full-speed, on-chip, external program memory.

Instruction Set Summary (Concluded)

Instr	Description	Cyc†/Wd	Operand Options	Opcode	Format
RSXM	Reset sign-extension mode	1/1	None	0CE06h	1
RTC	Reset test/control flag	1/1	None	0CE32h	1
RTXM	Reset serial port transmit mode	1/1	None	0CE20h	1
RXF	Reset external flag	1/1	None	0CE0Ch	1
SACH	Store high accumulator with shift	1/1	<dma>[,<shift>] <ind>[,<shift>[<next ARP>]]	06800h	5
SACL	Store low accumulator	1/1	<dma> <ind>[,<shift>[<next ARP>]]	06000h	5
SAR	Store auxiliary register	1/1	<AR>,<dma> <AR>,<ind>[>,<next ARP>]	07000h	5
SBLK	Subtract from accumulator long immediate with shift	2/2	<constant>[,<shift>]	0D003h	15
SBRK	Subtract from auxiliary register short immediate	1/1	<constant>	07F00h	10
SC	Set carry bit	1/1	None	0CE31h	1
SFL	Shift accumulator left	1/1	None	0CE18h	1
SFR	Shift accumulator right	1/1	None	0CE19h	1
SFSM	Set serial port frame synchronization mode	1/1	None	0CE37h	1
SHM	Set hold mode	1/1	None	0CE39h	1
SOVM	Set overflow mode	1/1	None	0CE03h	1
SPAC	Subtract P register from accumulator	1/1	None	0CE16h	1
SPH	Store high P register	1/1	<dma>; <ind>[,<next ARP>]	07D00h	4
SPL	Store low P register	1/1	<dma>; <ind>[,<next ARP>]	07C00h	4
SPM	Set P register output shift mode	1/1	<constant>	0CE08h	8
SQRA	Square and accumulate	1/1	<dma>; <ind>[,<next ARP>]	03900h	4
SQRS	Square and subtract previous product	1/1	<dma>; <ind>[,<next ARP>]	05A00h	4
SST	Store status register ST0	1/1	<dma>; <ind>[,<next ARP>]	07800h	4
SST1	Store status register ST1	1/1	<dma>; <ind>[,<next ARP>]	07900h	4
SSXM	Set sign-extension mode	1/1	None	0CE07h	1
STC	Set test/control flag	1/1	None	0CE33h	1
STXM	Set serial port transmit mode	1/1	None	0CE21h	1
SUB	Subtract from accumulator with shift	1/1	<dma>[,<shift>] <ind>[,<shift>[,<next ARP>]]	01000h	6
SUBB	Subtract from accumulator with borrow	1/1	<dma> <ind>[,<next ARP>]	04F00h	4
SUBC	Conditional subtract	1/1	<dma>; <ind>[,<next ARP>]	04700h	4
SUBH	Subtract from high accumulator	1/1	<dma>; <ind>[,<next ARP>]	04400h	4
SUBK	Subtract from accumulator short immediate	1/1	<constant>	0CD00h	10
SUBS	Subtract from low accumulator with no sign extension	1/1	<dma> <ind>[,<next ARP>]	04500h	4
SUBT	Subtract from accumulator with shift specified by T register	1/1	<dma> <ind>[,<next ARP>]	04600h	4
SXF	Set external flag	1/1	None	0CE0Dh	1
TBLR	Table read	4/1	<dma>; <ind>[,<next ARP>]	05800h	4
TBLW	Table write	3/1	<dma>; <ind>[,<next ARP>]	05900h	4
TRAP	Software interrupt	3/1	None	0CE1Eh	1
XOR	Exclusive-OR with accumulator	1/1	<dma>; <ind>[,<next ARP>]	04C00h	4
XORK	Exclusive-OR immediate with accumulator with shift	2/2	<constant>[,<shift>]	0D006h	15
ZAC	Zero accumulator	1/1	None	0CA00h	1
ZALH	Zero low accumulator and load high accumulator	1/1	<dma> <ind>[,<next ARP>]	04000h	4
ZALR	Zero low accumulator and load high accumulator with rounding	1/1	<dma> <ind>[,<next ARP>]	07B00h	4
ZALS	Zero accumulator, load low accumulator with no sign extension	1/1	<dma> <ind>[,<next ARP>]	04100h	4

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