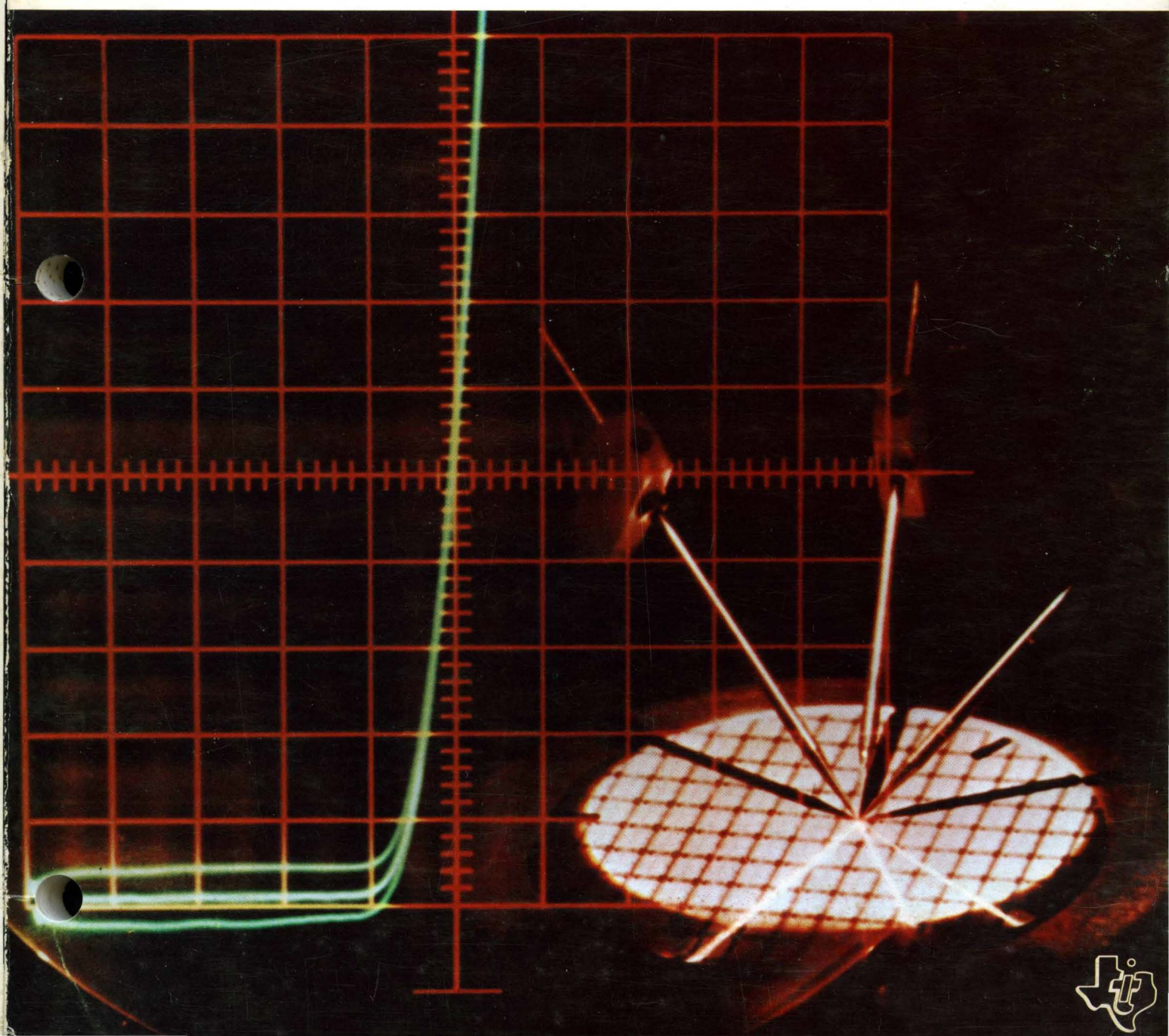
Bulletin CB-126

MOS/LSI from Texas Instruments



MOS/LSI from Texas Instruments

October 1970

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TEXAS INSTRUMENTS
INCORPORATED
COMPONENTS GROUP
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

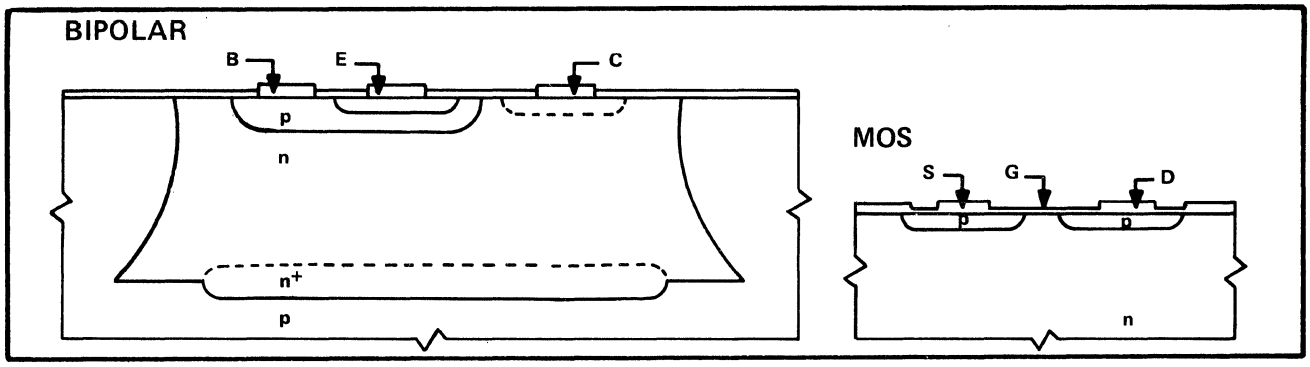
index

MOS . . . . . an innovative technology

Many types of equipment previously not suitable for electronic control can now take full advantage of the latest electronic technology. Equipment costs can be kept low, and equipment size can be easily reduced. MOS (Metal Oxide Silicon) circuits are ideal for digital applications including timers and counters, data transmission and switching equipment, recorders, calculators, controls and computer equipment. MOS is also applicable for analog applications such as telemetry and test equipment.

MOS technology can be applied to hundreds of types of equipment at costs usually lower than other technologies with significant improvements in reliability.

The introduction of MOS/LSI into new classes of equipments is possible since the basic MOS device combines the best attributes of the pentode vacuum tube with all of the advantages of the transistor. MOS devices are high input impedance small, simple to fabricate, and they consume little power; consequently, they offer the highest complexity of large scale integrated circuits.



COMPARISON OF TRANSISTOR CROSS SECTIONS

WHAT IS MOS?

Only one-third of the process steps are needed for MOS ICs as for the standard double diffused bipolar IC. But the most significant feature is the large number of semiconductor circuit elements that can be put on a small chip. This high circuit density means large scale integration, and permits TI to put up to 5,000 devices on a silicon chip only 150 x 150 mils square. Each transistor in the MOS/LSI array requires as little as 1 square mils of chip area, a great reduction over the bipolar transistors requiring 49 to 50 square mils.

introduction

Natural advantages of MOS/LSI include:

- increased circuit complexity per package
- lower cost per circuit function
- fewer parts to assemble and inspect
- fewer subsystems to test
- lower power drain per function
- a choice of standard or custom products to meet specific application requirements.

From the design standpoint, MOS/LSI is a two dimension layout rather than a three dimension. Mathematically you can predict its operation easier, and these mathematical models lend themselves to Computer Aided Design analysis. So the circuit can be laid out and its operation checked before it's built.

With its many applications and its simple fabrication, MOS/LSI is definitely headed for growth and expansion. It is probably the most important electronic innovation since the integrated circuit was developed by TI in 1958.

preliminary information

Preliminary information only is available on some of the products included in this catalog. This is indicated by the following statement on the first page of the specification.

> *The material herein is believed to be accurate and reliable; however, some parameters specified are derived from evaluation units and may change after full characterization.*

This means that a full characterization of the products on which we supply only preliminary information is in process, but has not yet been completed.

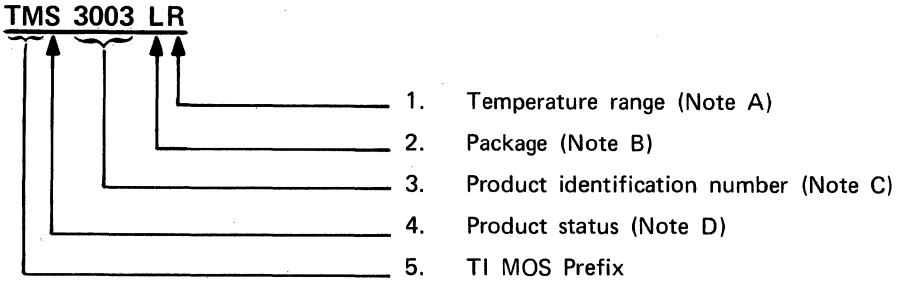
The information contained has been obtained through a thorough engineering evaluation of a large number of units over a period of time. Production units are fully final tested to meet the specifications. All products included in this catalog are in volume production at the present time. A full characterization is in process. Due to the high level of complexity of MOS/LSI a full characterization requires much more time than SSI or MSI integrated circuits. You may design any of these devices into your equipment with full confidence.

mos/lsi numbering system

TEXAS INSTRUMENTS MOS/LSI DEVICE NUMBERING SYSTEM

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading, regardless of package. Factory orders for circuits described in this catalog should include the complete part type numbers listed on each page.

MOS NUMBERING SYSTEM



NOTE A — **Temprature Range**

C	−25°C to +85°C (commercial)
M	−55°C to +125°C (military)
R	−55°C to +85°C (reduced military)
S	Special range (as designated by customer)

NOTE B — **Package**

F	Flat package
J	Ceramic dual-in-line
N	Plastic dual-in-line
L	TO-5 type
U	Unencapsulated (beam lead, etc.)

NOTE C — **Product Identification Number**

Part number unique to each type of device

NOTE D — **Product Status**

S	Standard devices
X	Prototype (all new designs)
C	Custom design
T	High reliability

Due to the high complexity of MOS/LSI, TI has had to innovate in the packaging area. The packages selected by TI are standards of the industry. Accessories for these packages are readily available.

1) Dual-in-line package

a) Pin-to-pin spacing

A pin-to-pin spacing of 100 mils has been selected for all dual-in-line packages.

b) Row-to-row spacing

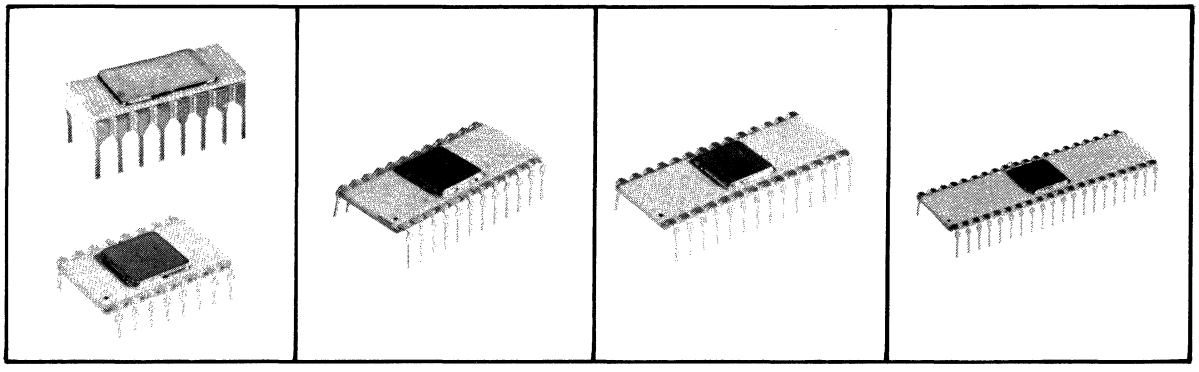
Two spacings are used, 300 mils and 600 mils.

c) Ceramic dual-in-line package types

TI uses several hermetically sealed ceramic dual-in-line packages. These packages consist of a ceramic base, gold plated cap and gold plated lids.

The following packages are presently in use:

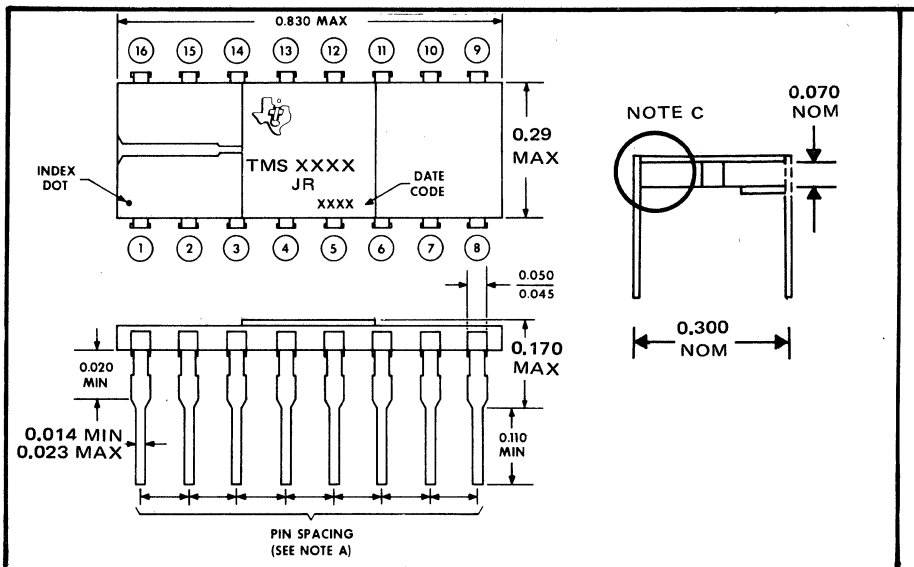
	16 PIN	24 PIN	28 PIN	40 PIN
300 mil between rows	X			
600 mil between rows	X	X	X	X

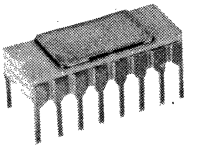


16 PIN | 24 PIN | 28 PIN | 40 PIN

mos/lsi packaging

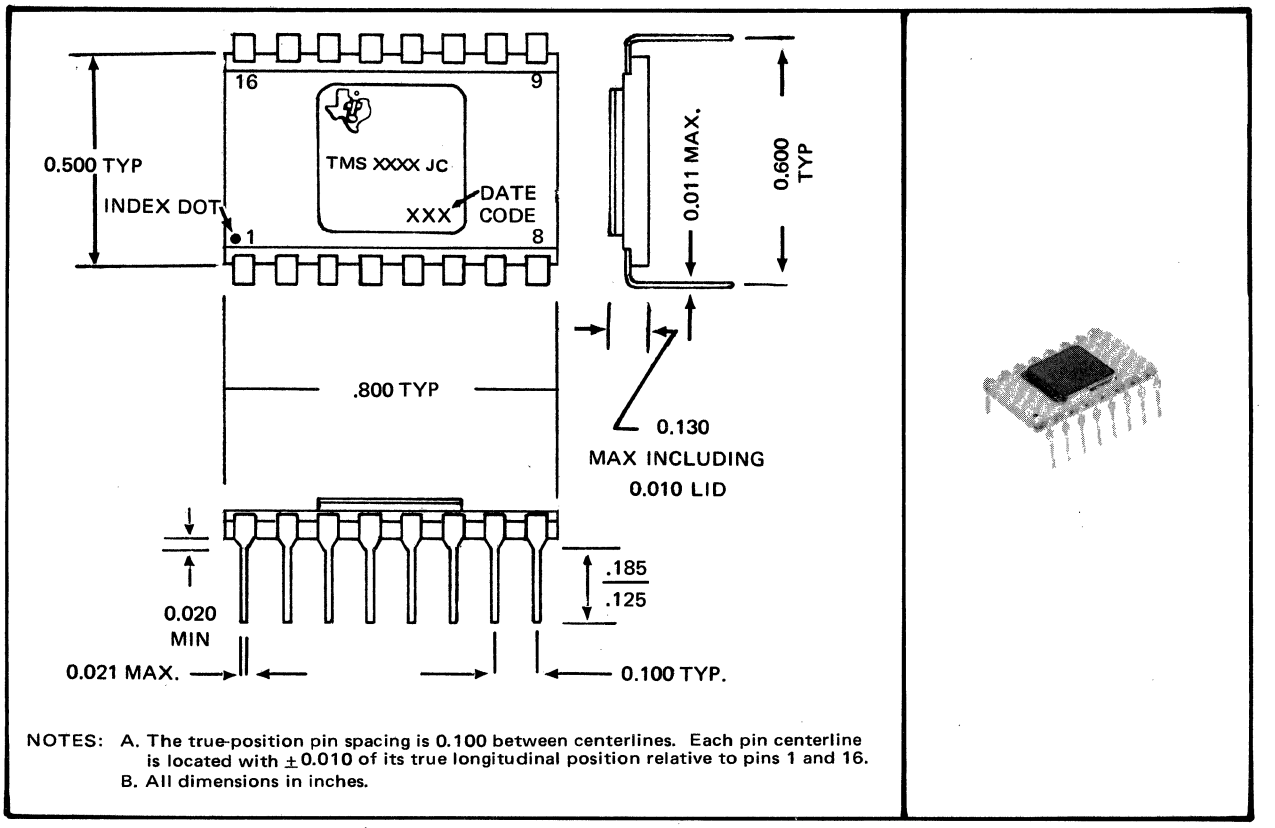
16 pin package (300 mil row spacing)





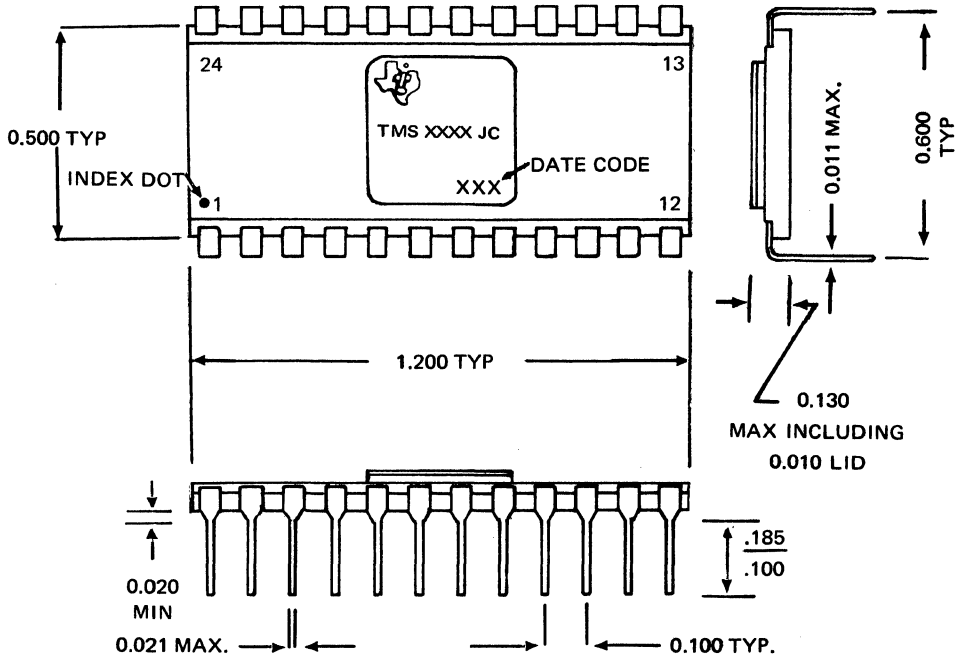
A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions are in inches.
C. LEADS MAY BE BRAZED TO SIDES OR BOTTOM OF PACKAGE

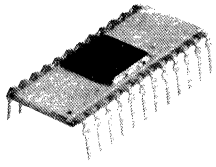
16 pin package (600 mil row spacing)



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located with ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions in inches.

24 pin package

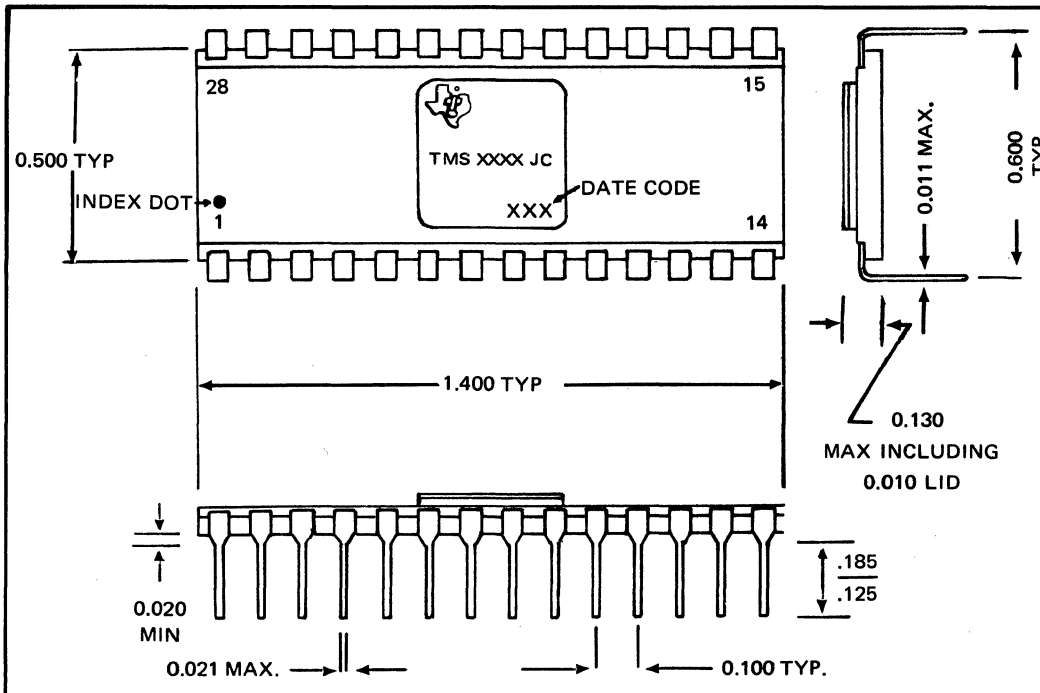


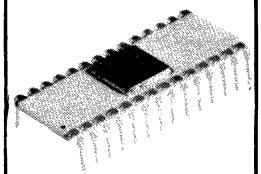


NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.

B. All dimensions in inches.

28 pin package



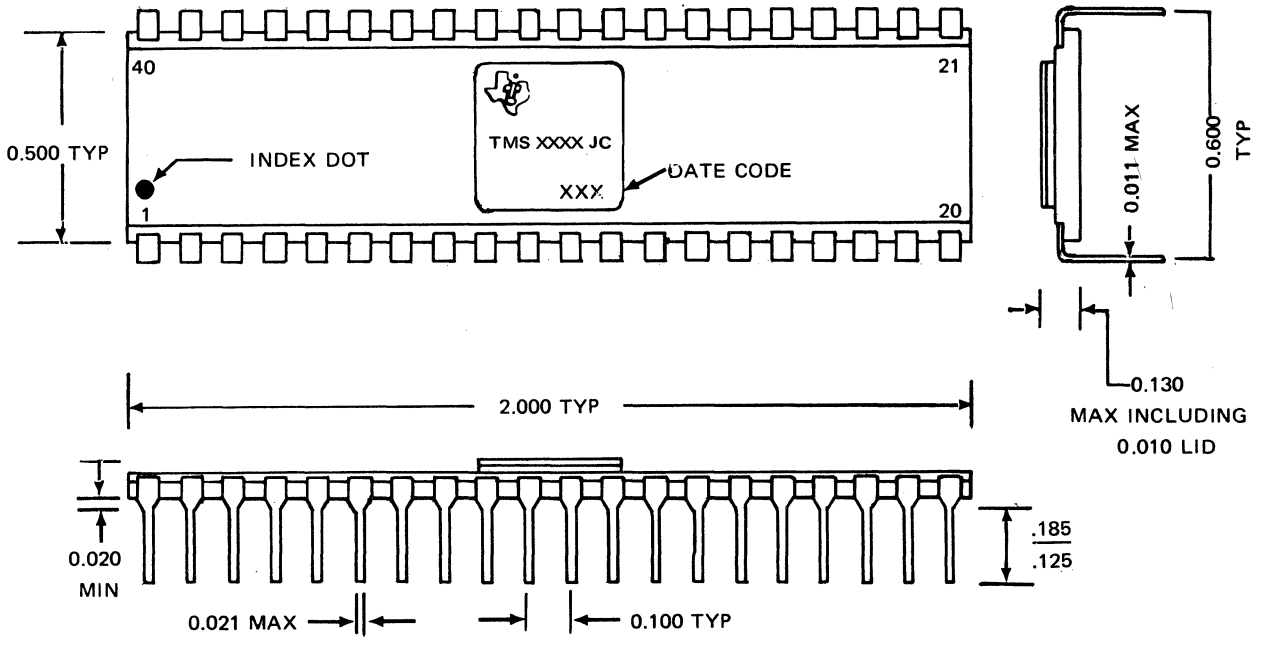


NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 28.

B. All dimensions in inches.

mos/lsi packaging

40 pin package



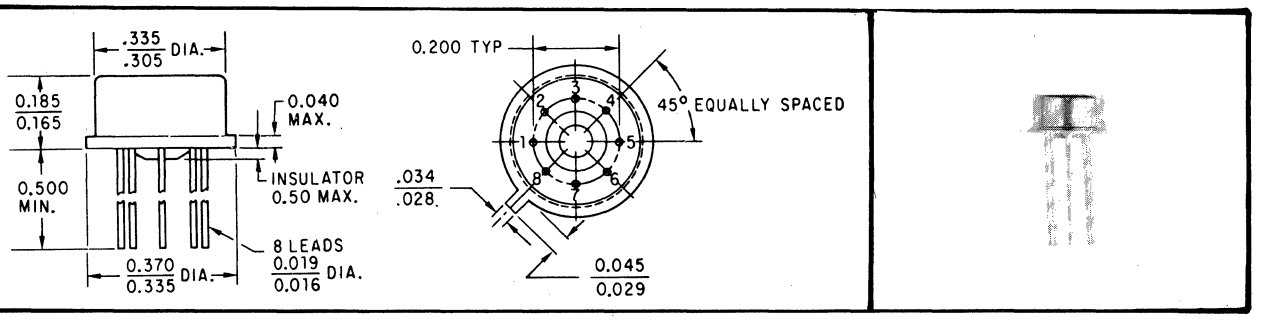
NOTES: 1. A true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins ① and ⑳

2. All dimensions in inches.

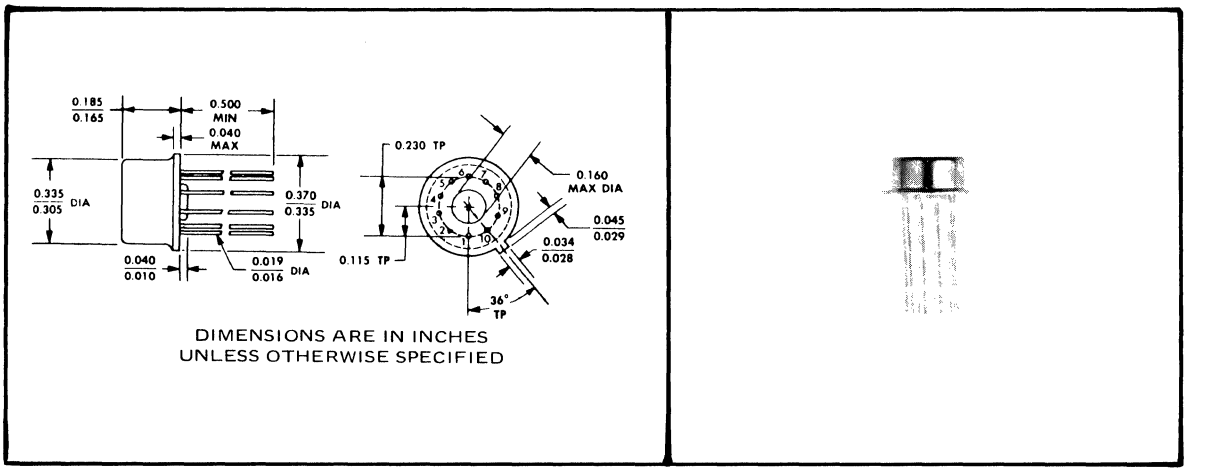
2) 'TO' type packages

For devices such as shift registers requiring few inputs and outputs TI uses two 'TO' type packages.

TO 99 package



TO 100 package



3) Manufacturing information

a) Alloying

Alloying is performed under inert atmosphere. A silicon gold eutectic is formed during the alloying operation.

b) Bonding

Thermal compression bonding is used. Typical bond strength is 5 grams. Bond strength is monitored on a lot to lot basis. Any bond strength of less than 2½ grams causes rejection of the entire lot of devices.

c) Sealing

TI uses a low temperature gold tin brazing to seal ceramic packages.

TO type packages are welded.

Glass leaks are eliminated by using an etheylene glycol solution heated to +150° C.

Fine leak elimination is performed through mass spectrometer techniques.

All MOS/LSI devices produced by TI are capable of withstanding 5×10^{-7} PPM fine leak inspection, and may be screened to 5×10^{-8} PPM fine leak if desired by the customer for special applications.

d) Shock and Vibration

All packages are capable of withstanding a shock of 3,000 Gs.

All devices are capable of passing a 20,000 G acceleration (centrifuge) test in the Y axis.

Pin strength is measured by a pin shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel off direction.

MOS/LSI SYSTEM COMPATIBILITY

MOS/LSI circuits have in the past few years conclusively proven their value to system designers. Most designs presently under consideration use both MOS/LSI and bipolar technologies in order to take full advantage of the low cost and high packaging density of MOS/LSI, as well as the flexibility of bipolar techniques for low complexity functions. With present MOS/LSI devices the task of the designer has been greatly simplified. Present MOS devices do not require separate interface circuits between MOS and MOS circuits or between bipolar and MOS circuits. MOS/MOS and MOS/Bipolar compatibility is demonstrated in each of the data sheets included in this catalog. The following information is general and applicable to all TI MOS/LSI devices.

1) POWER SUPPLIES

Two manufacturing technologies are common in MOS/LSI and prevalent in the industry: High Threshold MOS and Low Threshold MOS. The power supply requirements generally are:

	V_{SS}	V_{DD}	V_{GG}
High Threshold	0	−12 V	−24 V
Low Threshold	0	−5 V	−17 V

Where

V_{SS} is the substrate supply
V_{DD} is the drain supply
V_{GG} is the gate supply

The drain supply will draw most of the current. Some circuits are designed to use only one power supply (saturated logic). V_{DD} and V_{GG} are then common.

To use MOS in a system it is often convenient to translate all the power supply voltages by a certain voltage. The common arrangement is:

	V_{SS}	V_{DD}	V_{GG}
High Threshold	+12 V	0 V	−12 V
Low Threshold	+5 V	0 V	−12 V

NOTE: Some high threshold devices are specified at V_{GG} = −28 V and V_{DD} = −14 V.

2) COMPATIBILITY

Referencing all voltages to V_{SS} the input swing on most MOS circuits is as follows:

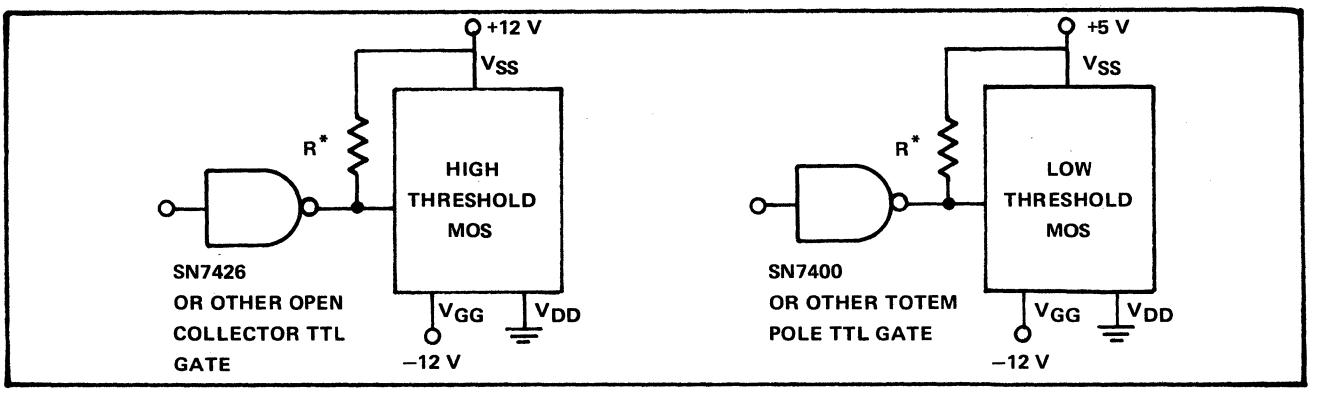
mos/lsi system compatibility

	High Level	Low level
High Threshold	0 to −3 V	−9 V to −24 V
Low Threshold	0 to −1.5 V	−4.2 V to −17 V

Relating to the translated power supplies as above this becomes:

	High Threshold	Low Threshold
V_{SS}	+12 V	+5 V
V_{DD}	0 V	0 V
V_{GG}	−12 V	−12 V
High level	+9 V to +12 V	+3.5 V to +5 V
Low level	+3 V to −12 V	0.8 V to −12 V

In all cases the input of the MOS circuit will look like a very high impedance. The input compatibility is easily achieved.



The value of the R* resistor varies depending on speed-power requirements. In many cases this resistor is diffused on the MOS chip. For low threshold MOS this resistor assures that the worst case TTL output (2.4 V) is pulled up to at least 3.5 V for proper MOS circuit operation.

3) OUTPUT COMPATIBILITY

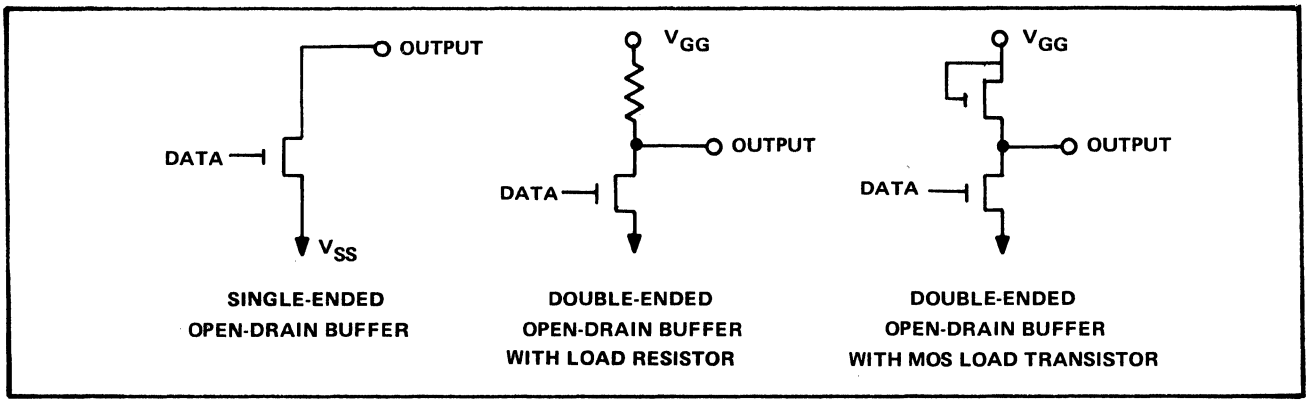
Two types of buffers are commonly used on MOS devices:

Single-ended open-drain buffer

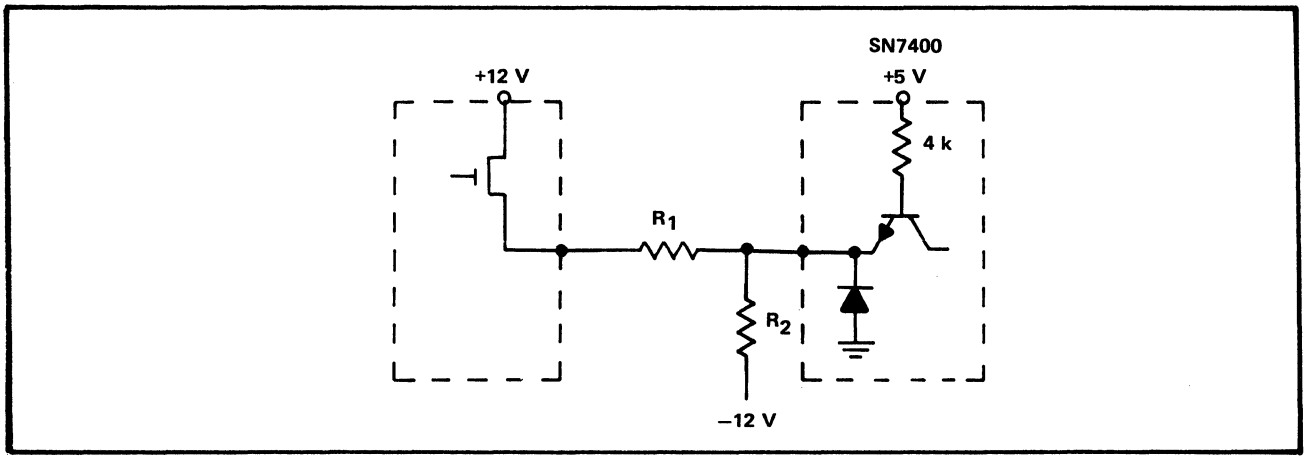
Push-pull buffer

a) Single-ended open-drain

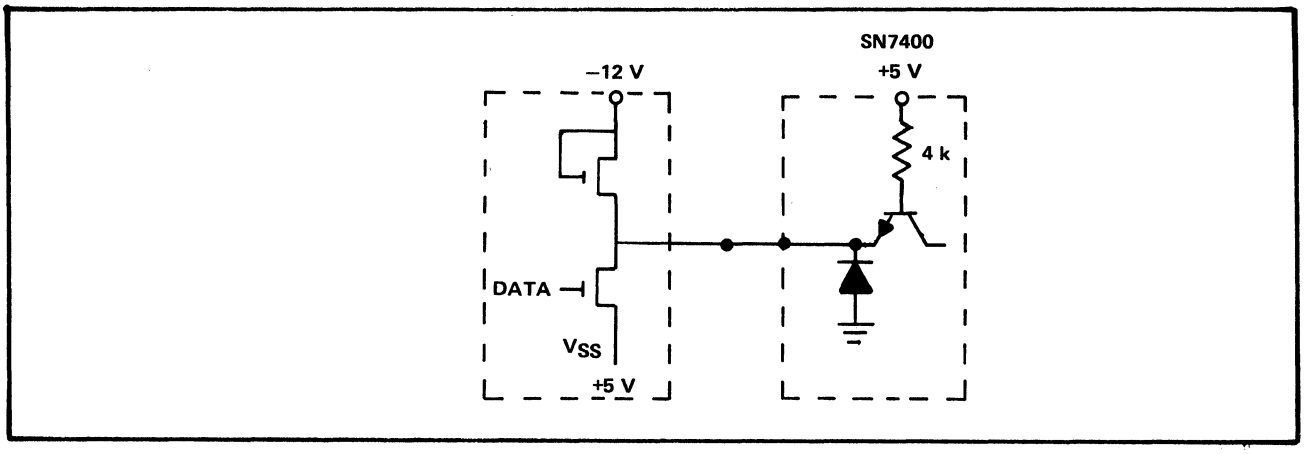
The buffer is simply a current switch. In the "off" state the impedance of the buffer is extremely large while in the "on" state it is typically under 1 kΩ. A discrete resistor or an MOS transistor may be used as a load with a single-ended open-drain buffer. This resistor may be internal to the MOS circuit.



In every case compatibility with MOS is easily achieved. For instance a single-ended buffer with high threshold MOS:

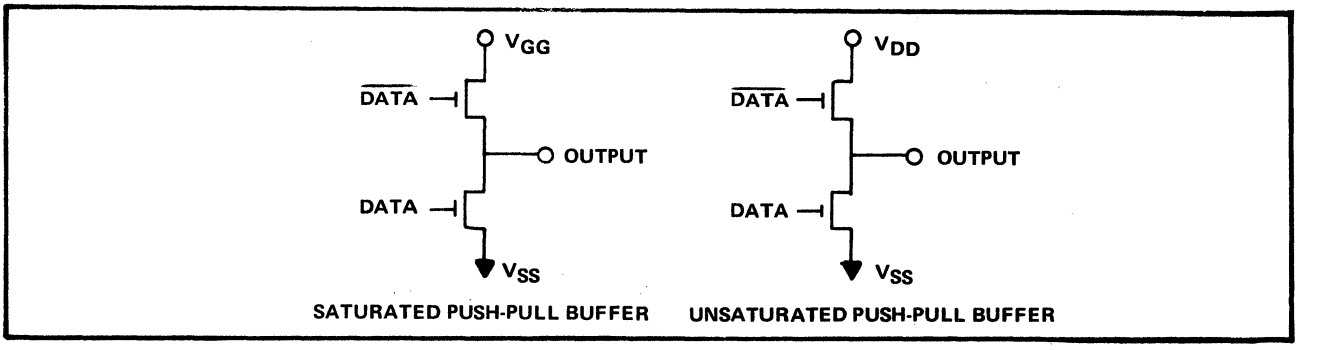


R_2 provides the necessary current sink for the TTL input, R_1 limits the positive excursion to +5 V. If used for low threshold MOS, V_{SS} is translated up to +5 V instead of +12 V and R_1 can be eliminated. If R_2 is on the chip no external components are necessary.



b) Push-pull buffer

Two types are common



The unsaturated push-pull buffer is the most commonly used for low threshold circuits. It permits direct TTL compatibility without external components.

4) CLOCKS

Depending on the type of circuit there are different clock requirements:

No clocks – Static RAM's, ROM's, etc.

1 clock – with other clocks generated internally

2 clocks – most shift registers

4 clocks – very high speed low power dissipation shift registers

a) One external clock

An internal circuit generates the clocks from a single outside clock signal. The outside clock signal has the same swing as the data input signal and the compatibility is identical (see preceeding paragraph 3).

Single clock low threshold MOS circuits will accept a TTL clock without adding additional components.

b) Two or four clocks

The clock signals must swing between V_{SS} and V_{GG}. To go from a single TTL level clock to a multiple MOS level clock two circuits are required: 1) a clock generator to generate the necessary clock pulses, and 2) a clock driver to bring the clock levels to the required values. In most cases only one clock circuit is needed for an entire MOS/LSI system.

In all digital equipment there is a need to temporarily store and transfer data. MOS shift registers are ideally suited for these applications, because they can economically store very large amounts of information.

Basic Configuration

MOS shift registers can be supplied in the following configurations:

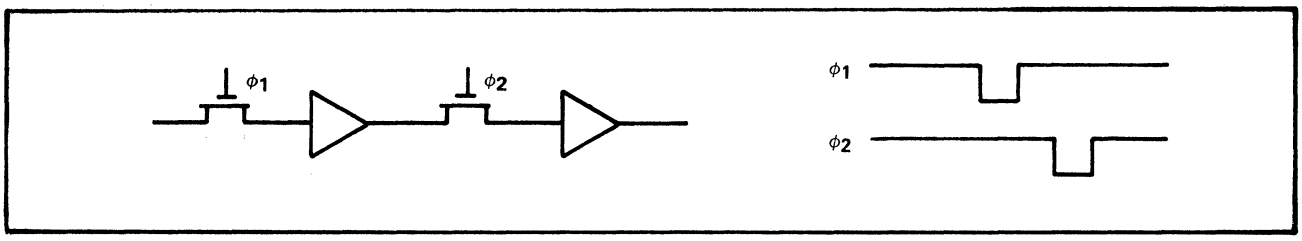
Serial-in/Serial-out

Parallel-in/Serial-out

Serial-in/Parallel-out

The serial-in/serial-out configuration is by far the most popular.

An MOS shift register will be able to store N bits. Each bit is stored on a basic cell consisting of two MOS inverters and of timing devices.



Static or Dynamic?

In a static shift register storage element the two inverters are connected to form a latch. The data can be stored indefinitely. There is no minimum frequency of operation.

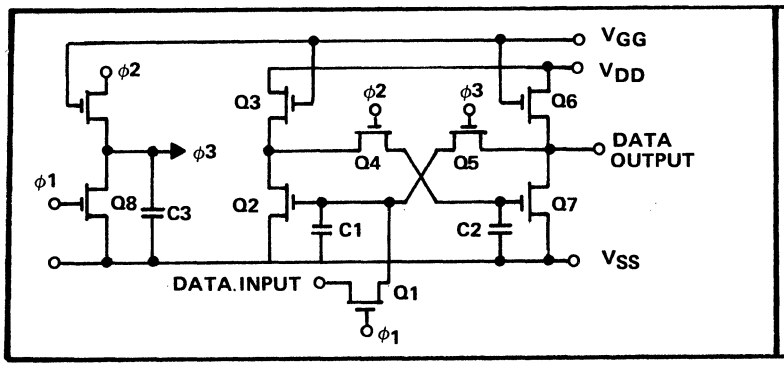
Dynamic shift registers use two independent inverters (not cross-coupled). The data is temporarily stored on a capacitor inherent to an MOS device. The device can not be operated below a certain clock frequency, or the data storage will be lost.

Dynamic shift registers are faster than static registers and dissipate much less power. They are not as flexible to use in a system.

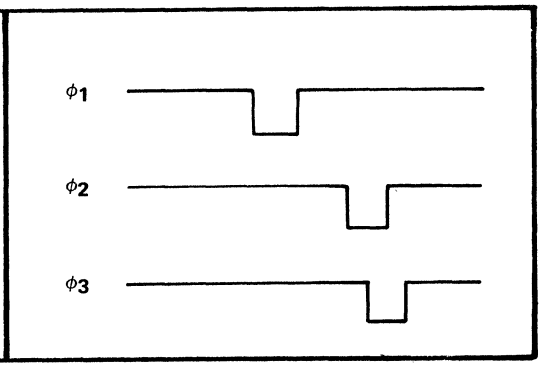
shift registers

Static Shift Registers

A static shift register uses two static MOS inverters. Three phases (clocks) are necessary to operate a static shift register. The third phase clock is always generated internally. The third phase times the feedback loop. The second clock phase is often generated internally.



Basic cell of static shift register and $\phi 3$ internal generation



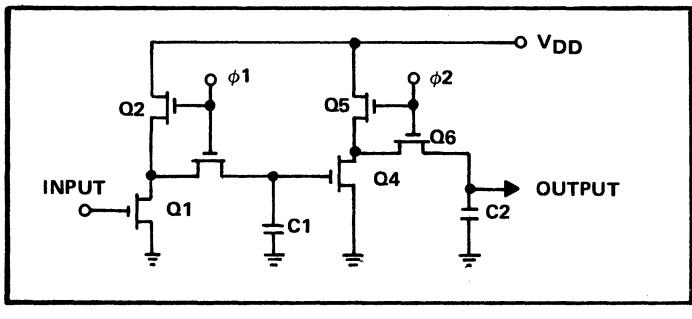
Timing diagram for a static shift register

Static shift registers operate in the 0 to 2 MHz clock range. They are extremely flexible and data can be held indefinitely, as long as power is supplied.

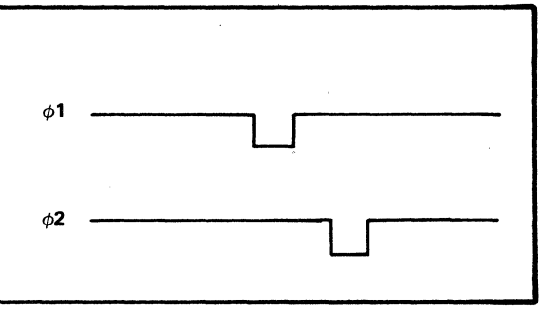
Dynamic Shift Registers

Dynamic shift registers use either two or four phases (clocks). These phases can be generated on the chip or be supplied externally. Two-phase shift registers can be classified as ratio and ratioless circuits.

The two phase ratio type shift register consists of two simple dynamic inverters and of timing devices.



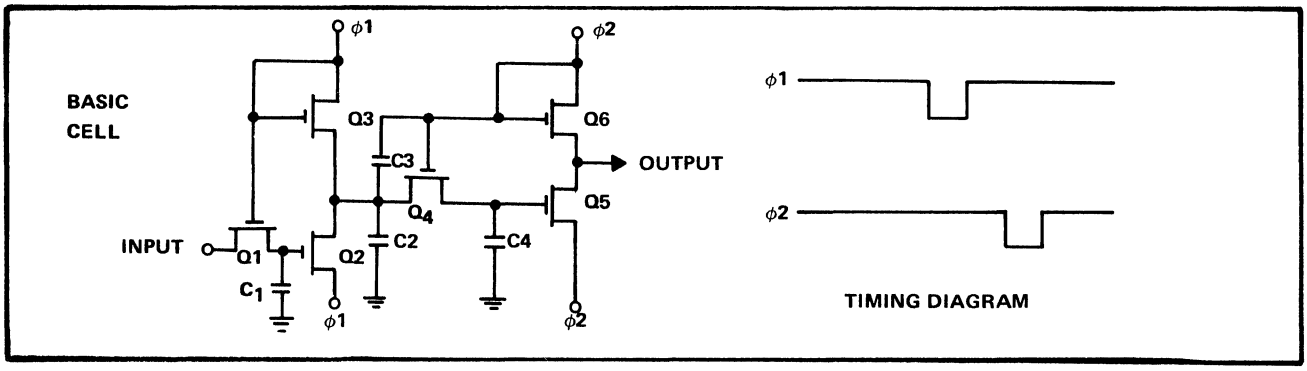
Basic cell for a dynamic shift register



Timing diagram for a 2 phase dynamic shift register

When ϕ_1 is at a logic level 1 (low) the capacitance C_1 charges at the inverse of the data input. Data is transferred out when ϕ_2 goes to 1.

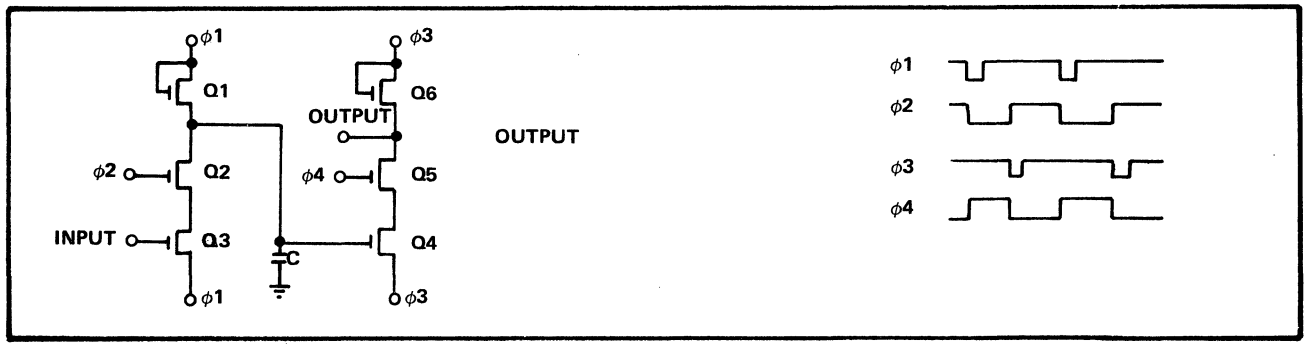
The two phase ratioless dynamic shift register has been designed to decrease the power dissipation and the chip area. In a ratio type circuit current flows through the inverter when the clock and data input are simultaneously at a logic 1. There must be a certain minimum ratio between the size of the two MOS transistors in the inverters (typically >5:1). This will take more chip area than in a ratioless shift register. In a ratioless shift register the MOS devices used are usually of identical size.



2 phase ratioless dynamic shift register

The 2 Phase 'Ratioless' Dynamic Shift Register uses identical transistors throughout and can therefore work at higher clock rates since the precharging paths are of lower impedance than those in the ratio circuit. When ϕ_1 goes to '1' C_2 charges to '1' via Q_3 and C_1 charges to the Data Input level via Q_1. When ϕ_1 returns to '0' transistor Q_2 turns ON if the INPUT level was a '1' and discharges C_2. For a '0' input Q_2 stays OFF and C_2 is not discharged. Now ϕ_2 goes to a '1' and turns on Q_4 so that C_2 shares any charge it has with C_4. C_3 is used to compensate for the loss of potential across C_2 by introducing a small extra charge on the negative edge of ϕ_2. It does not introduce enough to destroy a logic '0' on C_2. When ϕ_2 returns to a '0' the charge on C_4 transfers the Data Input level to the OUTPUT.

Four phase shift registers are used for very high density circuits operated at very high speed.



4 phase shift register basic cell and timing diagram

shift registers

In the basic 4 Phase Dynamic Shift Register C is precharged via Q_1 during ϕ_1. After ϕ_1, ϕ_2 holds Q_2 ON so C takes a level which is the inverse of the input. The process is repeated by the SLAVE section Q_4 – Q_6 so that the INPUT level is transferred to the OUTPUT after ϕ_3 and during ϕ_4. The stage uses similar transistors throughout giving high package density. Power dissipation is low, speed can be high but a relatively complex clock drive circuit is required.

MOS Shift Registers from TI

	CLOCK	LOGIC	POWER SUPPLY	FREQUENCY	NUMBER OF BITS
TMS 3000 LR	2	Static	+14 V – –14 V	0 – 1 MHz	2 x 25
TMS 3001 LR	2	Static	+14 V – –14 V	0 – 1 MHz	2 x 32
TMS 3002 LR	2	Static	+14 V – –14 V	0 – 1 MHz	2 x 50
TMS 3003 LR	2	Static	+14 V – –14 V	0 – 1 MHz	2 x 100
TMS 3012 JR	1	Static	+14 V – –14 V	0 – 1 MHz	2 x 128 (Accumulator)
TMS 3016 LR	2	Static	+14 V – –14 V	0 – 1 MHz	2 x 16
TMS 3026 JC	1	Static	+14 V – –14 V	0 – 250 KHz	6 bit SIPO
TMS 3028 LR	1	Static	+14 V – –14 V	0 – 1 MHz	2 x 128
TMS 3101 LC	2	Static	+5 V – –12 V	0 – 2.5 MZ	2 x 100
TMS 3112 JC	1	Static	+5 V – –12 V	0 – 1 MZ	6 x 32
TMS 3304 LR	2	Dynamic	+14 V – –14 V	10 KHz – 5 MHz	3 x 66
TMS 3305 LR	2	Dynamic	+14 V – –14 V	10 KHz – 5 MHz	3 x 64
TMS 3309 LR	4	Dynamic	+12 V – –12 V	10 KHz – 10 MHz	2 x 512
TMS 3314 JC	2	Dynamic	+14 V – –14 V	10 KHz – 2 MHz	3 (60 +4)
TMS 3401 LC	2	Dynamic	+5 V – –12 V	20 KHz – 5 MHz	1 x 512
TMS 3406 LR	2	Dynamic	+5 V – –12 V	10 KHz – 2 MHz	2 x 100

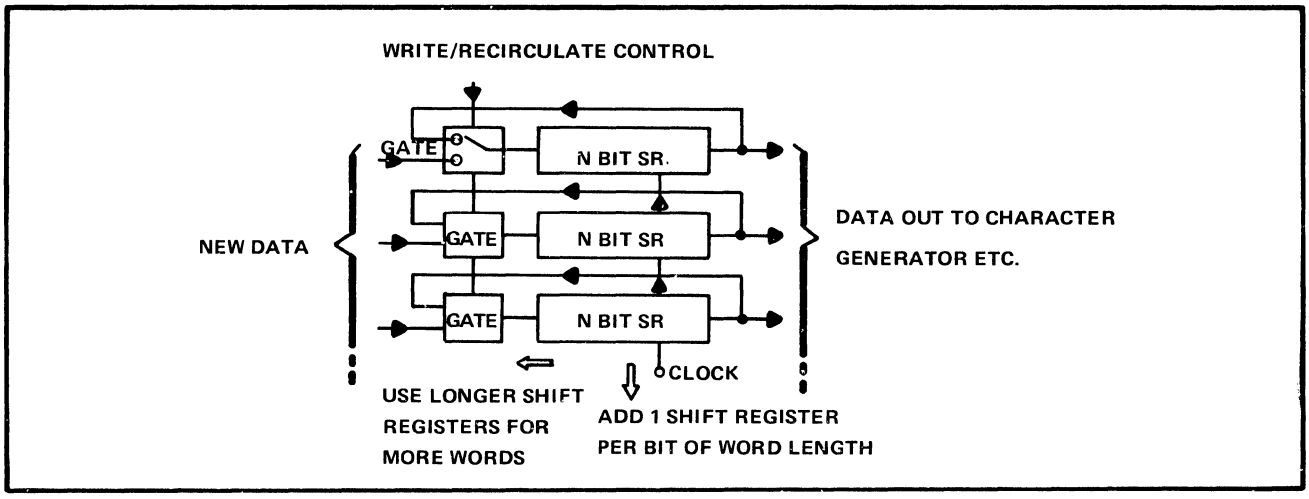
Applications

Main applications of MOS shift registers are refresh memories, scratch pad memories, data handling, and delay lines.

Any N-bit shift register can be used as a Refresh Memory by returning outputs to inputs as shown. A particular bit of information is available at the output every

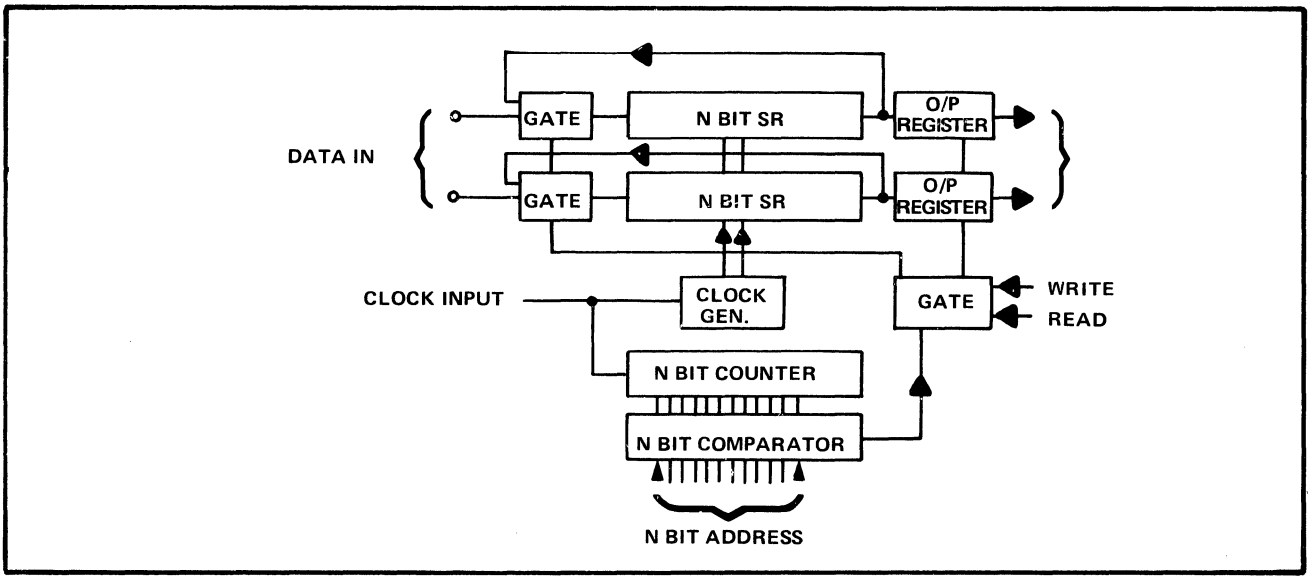
$$\frac{N}{\text{clock frequency}} \text{ seconds.}$$

This is particularly useful for renewing fading displays such as CRT character generator systems. New data is written in via a 2-way input gate circuit.



Shift registers used as refresh memory

By adding an address counter and comparator in the Refresh Memory it becomes a 'Scratch Pad' memory. Data can be written in and read out of any point specified by the input address code. An output register is necessary to store the required output data and to provide a 1 bit delay so that the 'Read' address is the same as the 'Write' address since there is a 1 bit delay between output and input.



Shift registers used as scratch pad memory

TMS3000LR–dual 25-bit static shift register
TMS3001LR–dual 32-bit static shift register

FEATURING

- **Static logic**
- **DC to 1 MHz operation**
- **Low power dissipation**
- **Push-pull output buffers**
- **TTL compatible**

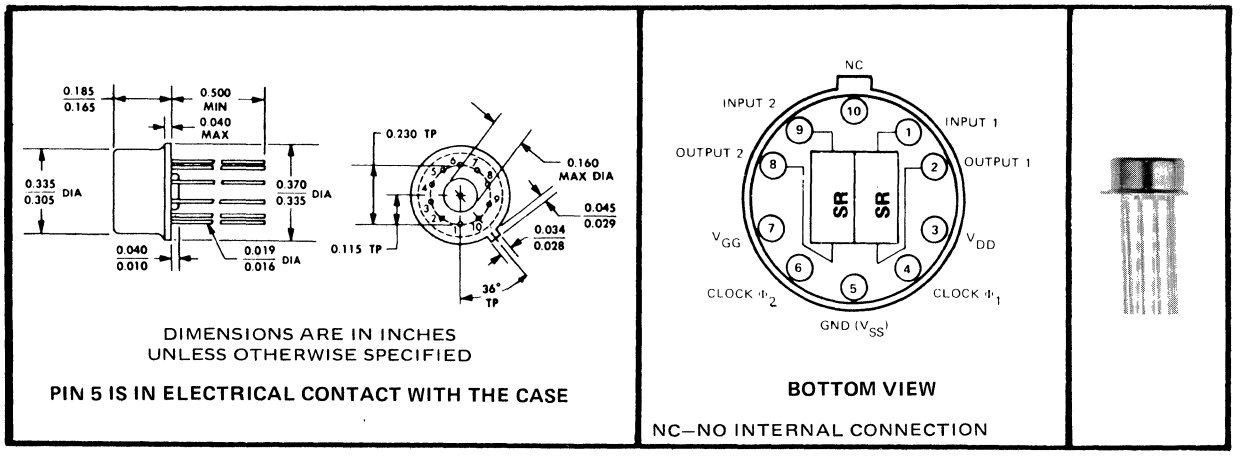
description

The TMS 3000 LR and TMS 3001 LR are dual static shift registers. Each device contains two d-c to 1 MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low output impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The package outline is the same as JEDEC TO-100 except for diameter of standoff.



logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1) . . . . . −30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage V_I range (See Note 1) . . . . . −30 V to 0.3 V
Power dissipation . . . . . 450 mW
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1. These voltage values are with respect to network ground terminal, V_{SS}.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)	0		5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
$\phi 1$ clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
$\phi 2$ clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from $\phi 1$ clock to $\phi 2$ clock input pulse, $t_{\phi 12}$ (See voltage waveforms)	0.01		10	μs
Time interval from $\phi 2$ clock to $\phi 1$ clock input pulse, $t_{\phi 21}$ (See voltage waveforms)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.

3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at V_{DD} = −14 V, V_{GG} = −28 V, and T_A = 25°C.

TMS3000LR–dual 25-bit static shift register
TMS3001LR–dual 32-bit static shift register

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	V_I = −20 V				0.5	μA
$I_{IL(\phi)}$	Logic 1 input current into either clock input	V_ϕ = −28 V, V_{GG} = 0 V				50	μA
V_{OH}	Logic 0 output voltage	I_O = 0 mA				−1	V
		I_O = −2.0 mA			−2.6	−5	V
V_{OL}	Logic 1 output voltage	I_O = 0 mA		−12			V
		I_O = 1.0 mA		−11	−11.6		V
R_{OH}	Output resistance, logic 0	I_O = −2.0 mA				2.5	kΩ
R_{OL}	Output resistance, logic 1	I_O = 1.0 mA				3	kΩ
I_{DD}	Supply current from V_{DD} terminal*		TMS 3000 LR		−14	−20	mA
			TMS 3001 LR		−16	−24	mA
I_{GG}	Supply current from V_{GG} terminal*		TMS 3000 LR		−2	−3.5	mA
			TMS 3001 LR		−2	−3.5	mA
f_{max}	Maximum clock frequency			1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).

‡ All typical values are at T_A = 25°C.

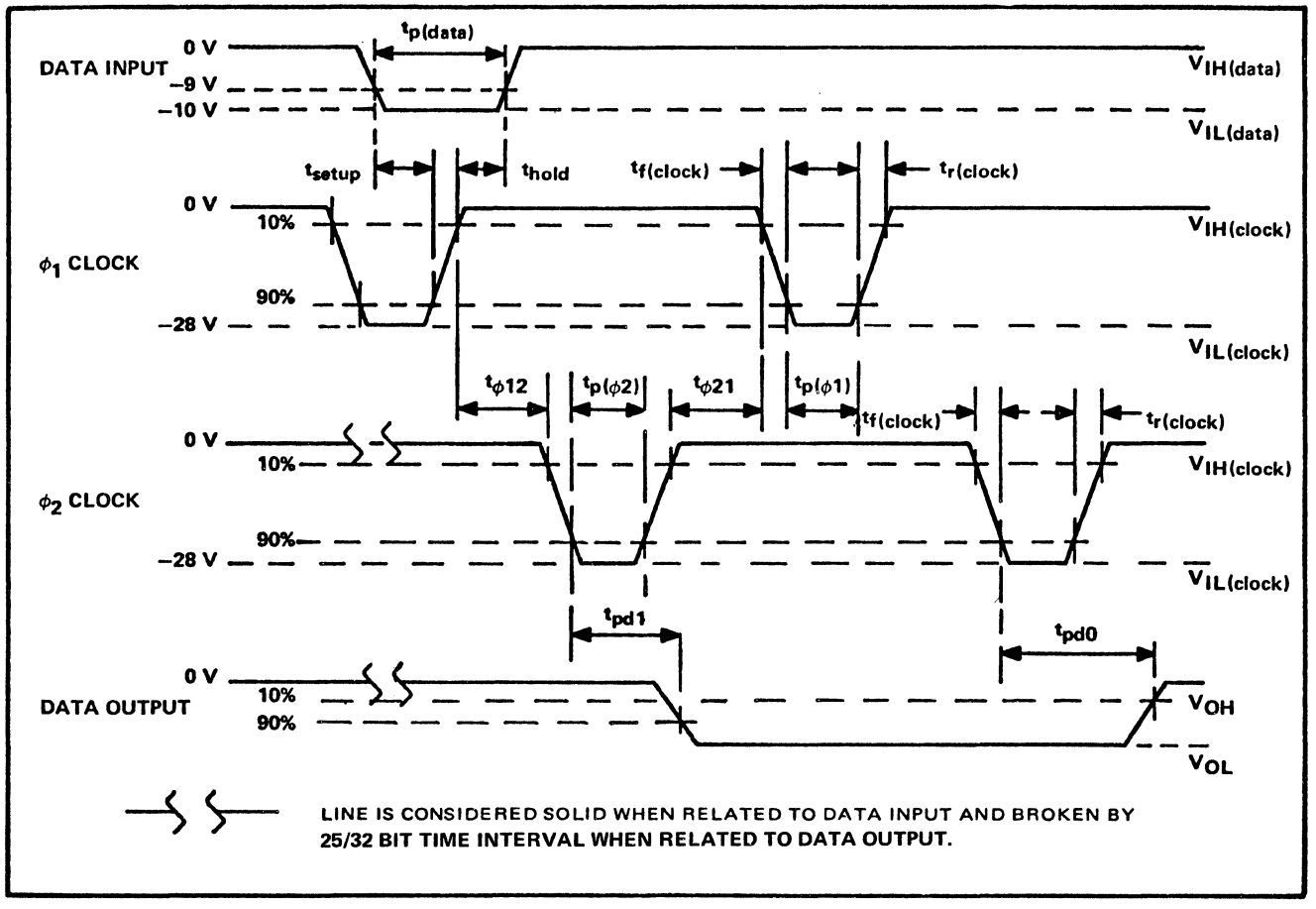
* Current into a terminal is a positive value.

switching characteristics, V_{DD} = −14 V, V_{GG} = −28 V, R_L = 10 mΩ, C_L = 20 pF, T_A = 25°C

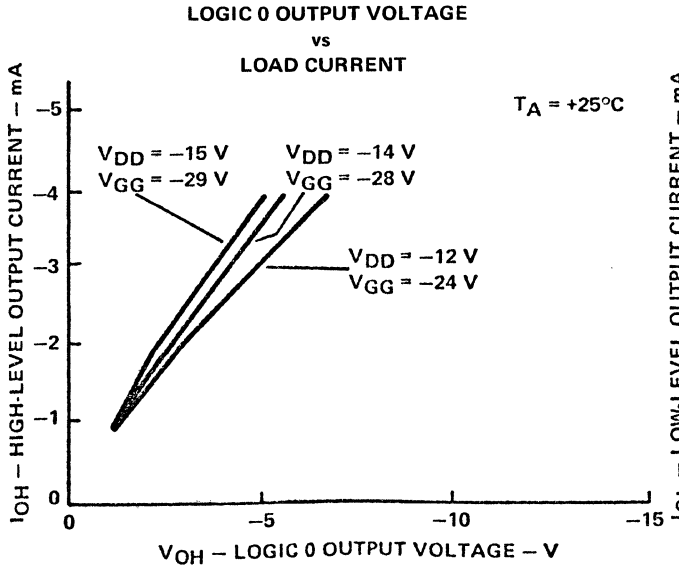
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	V_I = 0 V, $V_{I(\phi2)}$ = 0 V, f = 1 MHz	TMS 3000 LR		8	12	pF
			TMS 3001 LR		11	15	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	V_I = 0 V, $V_{I(\phi1)}$ = 0 V, f = 1 MHz	TMS 3000 LR		15	20	pF
			TMS 3001 LR		20	30	pF
C_{in}	Capacitance of data input	V_I = 0,	f = 1 MHz		5	7	pF

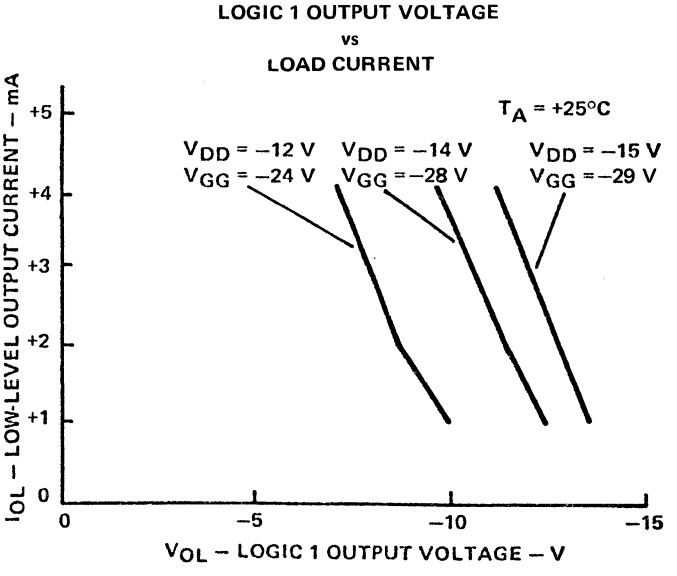
* $C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

voltage waveforms

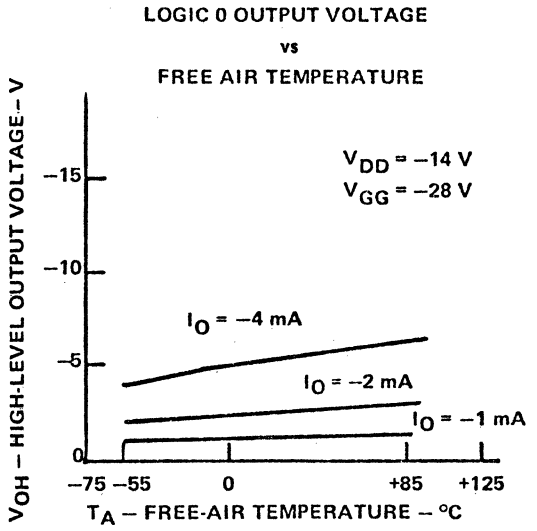


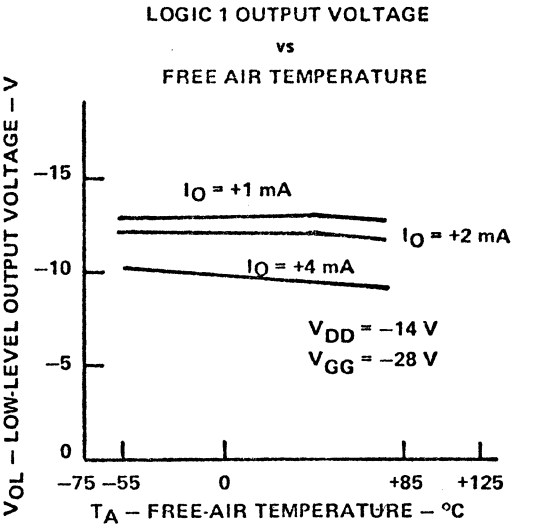
typical characteristics





typical characteristics (continued)

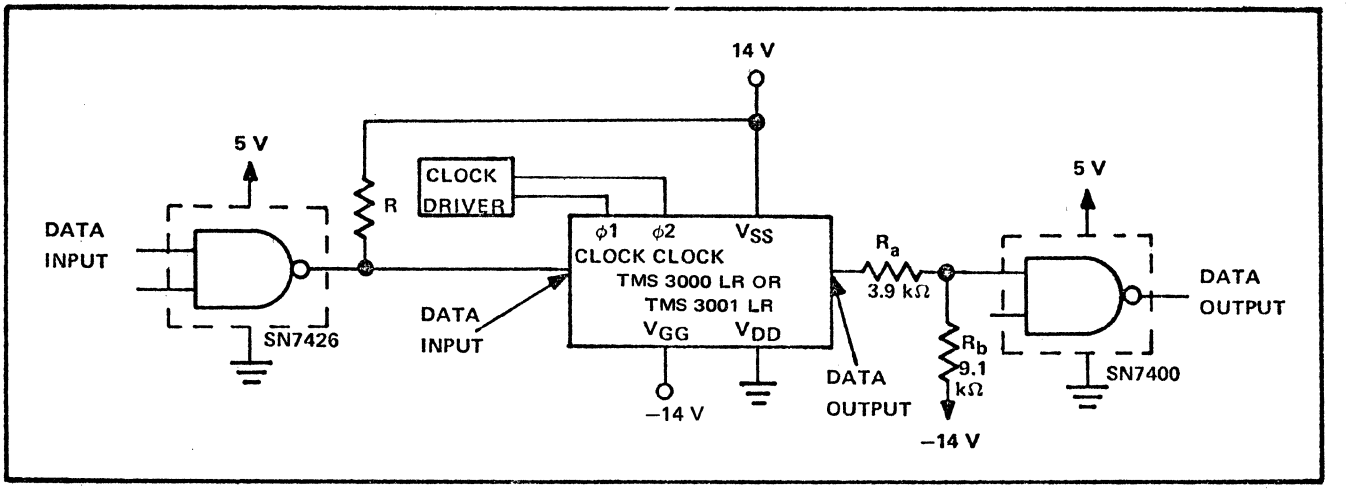




typical application data

1) **MOS/TTL interface**

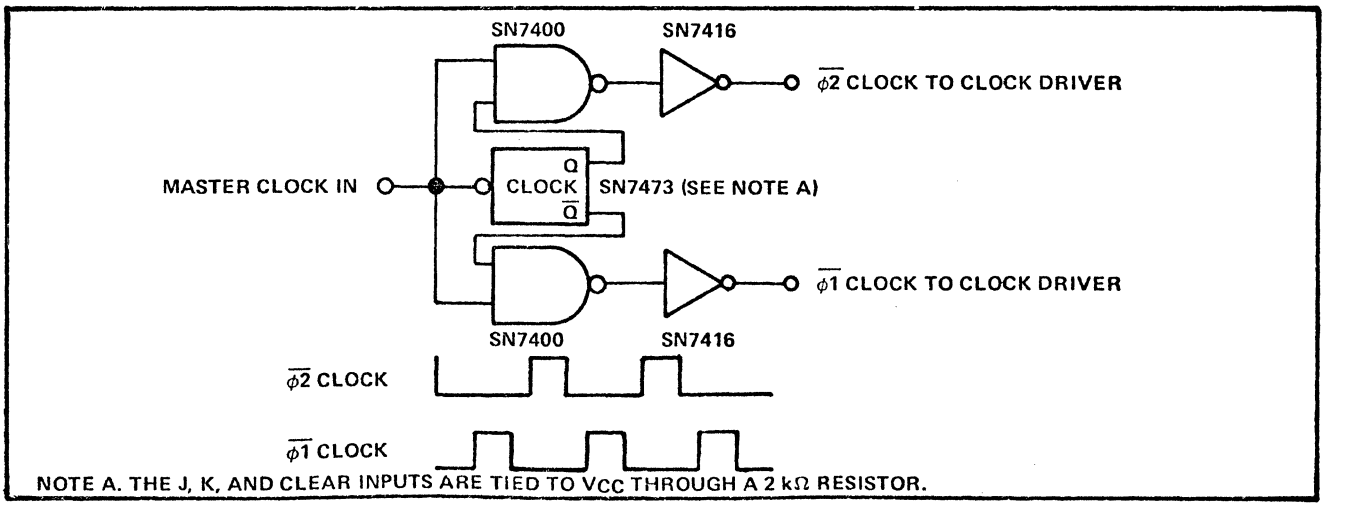
With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



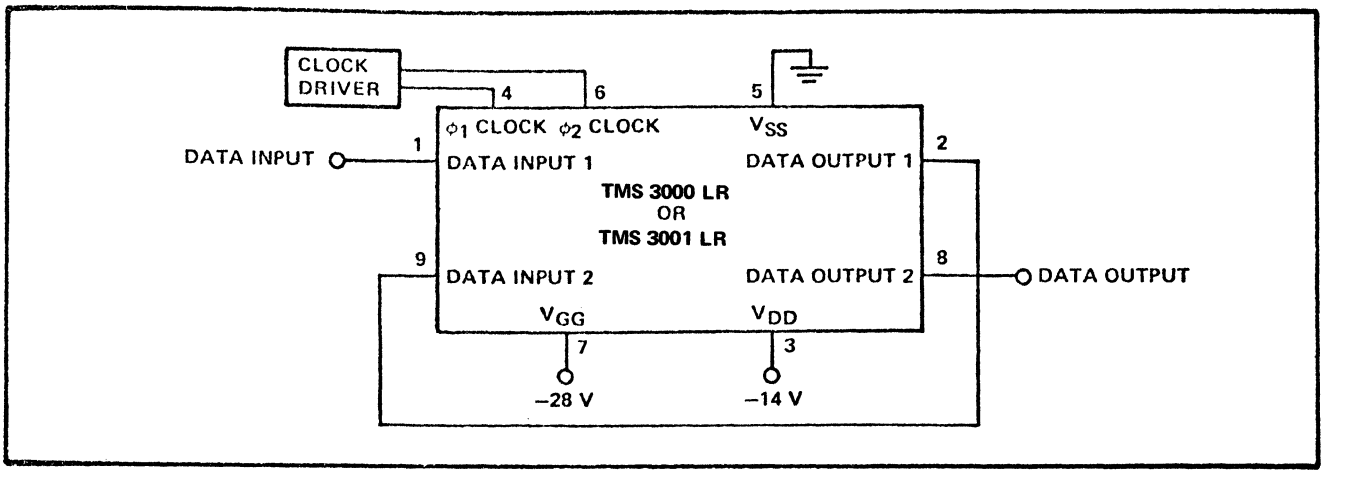
An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements – values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

At the output interface, the 9.1 kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9 kΩ resistor and the 9.1 kΩ resistor to −14 volts. The 3.9 kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

2) **Two-phase clock generator**

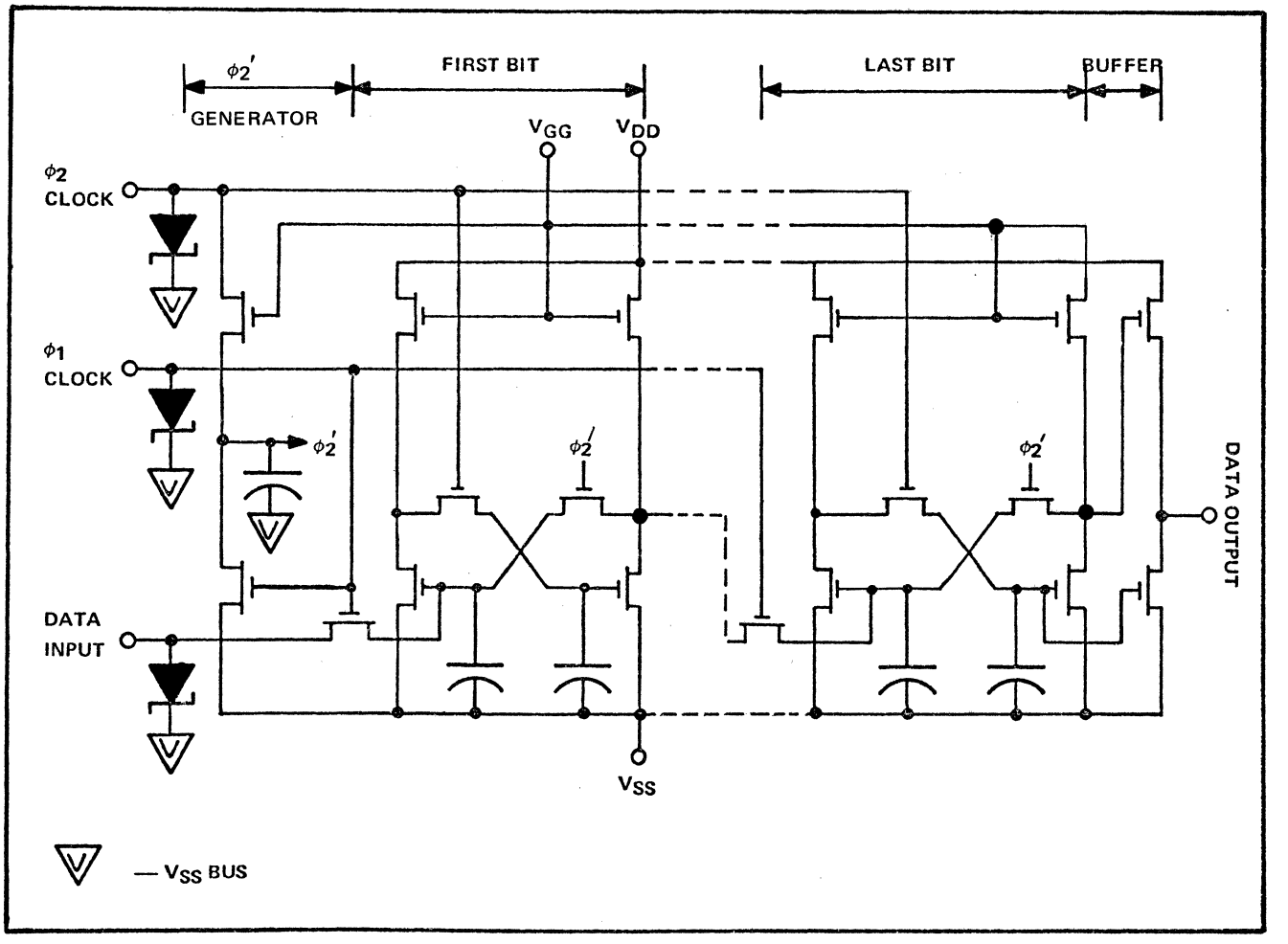


expansion to single 50- or 64-bit register



TMS3000LR–dual 25-bit static shift register
TMS3001LR–dual 32-bit static shift register

schematic (each register)



TMS3002LR - dual 50-bit shift register
TMS3003LR - dual 100-bit shift register

FEATURING

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

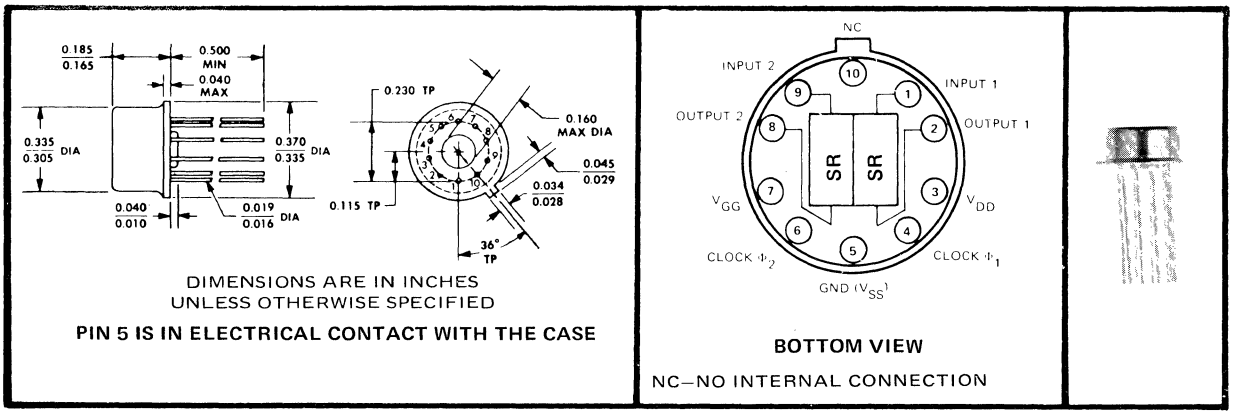
description

The TMS 3002 LR and TMS 3003 LR are dual static shift registers. Each device contains two d-c to 1 MHz shift registers with independent input and output terminals and common clocks and power. MOS thick oxide technology is used to fabricate cross coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low output impedance non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The package outline is the same as JEDEC TO-100 except for diameter of standoff.



TMS3002LR - dual 50-bit shift register
TMS3003LR - dual 100-bit shift register

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1) . . . . . −30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage V_I range (See Note 1) . . . . . −30 V to 0.3 V
Power dissipation . . . . . 450 mW
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1. These voltage values are with respect to network ground terminal, V_{SS}.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)		0	5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See voltage waveforms)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See voltage waveforms)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.
3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at V_{DD} = −14 V, V_{GG} = −28 V, and T_A = 25°C.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	V_I = −20 V			0.5	μA
$I_{IL(\phi)}$	Logic 0 input current into either clock input	V_I = −28 V, V_{GG} = 0 V			50	μA
V_{OH}	Logic 0 output voltage	I_O = 0 mA			−1	V
		I_O = −2.0 mA		−2.6	−5	V
V_{OL}	Logic 1 output voltage	I_O = 0 mA	−12			V
		I_O = 1.0 mA	−11	−11.6		V
R_{OH}	Output resistance, logic 0	I_O = −2.0 mA			2.5	kΩ
R_{OL}	Output resistance, logic 1	I_O = 1.0 mA			3	kΩ
I_{DD}	Supply current from V_{DD} terminal§	TMS 3002 LR		−8.5	−15	mA
		TMS 3003 LR		−16	−26	mA
I_{GG}	Supply current from V_{GG} terminal§	TMS 3002 LR		−2	−3	mA
		TMS 3003 LR		−2	−3	mA
f_{max}	Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).

‡ All typical values are at T_A = 25°C.

§ Current into a terminal is a positive value.

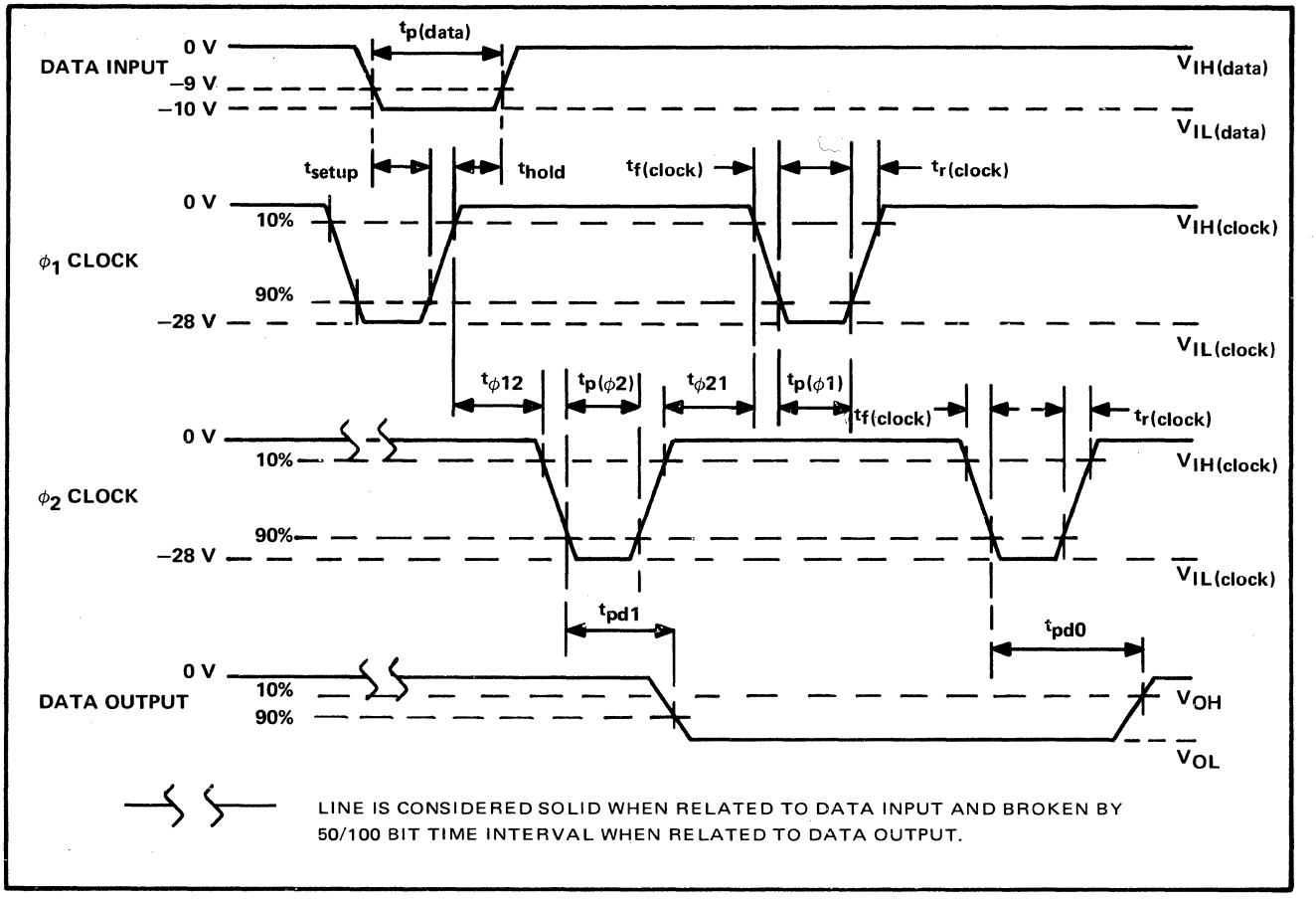
switching characteristics, V_{DD} = −14 V, V_{GG} = −28 V, R_L = 10 mΩ, C_L = 20 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pdo}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			250	400	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock	See voltage waveforms			250	350	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	V_I = 0 V, $V_{I(\phi2)}$ = 0 V, f = 1 MHz	TMS 3002 LR		18	23	pF
			TMS 3003 LR		28	33	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	V_I = 0 V, $V_{I(\phi1)}$ = 0 V, f = 1 MHz	TMS 3002 LR		30	35	pF
			TMS 3003 LR		53	60	pF
C_{in}	Capacitance of data input	V_I = 0,	f = 1 MHz		5	7	pF

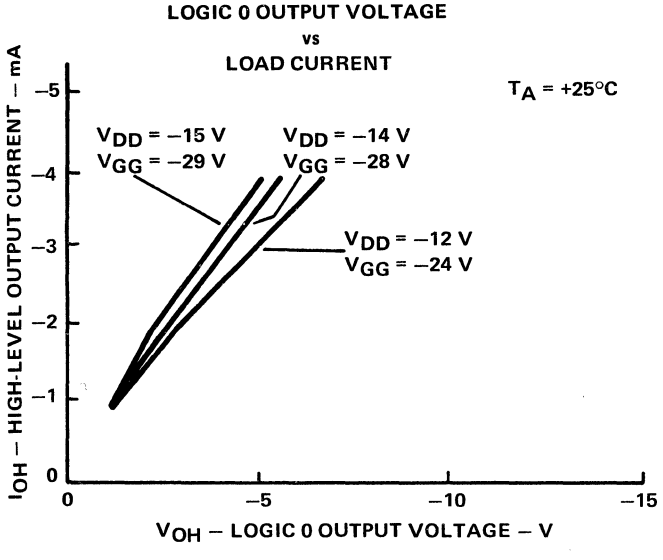
$C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

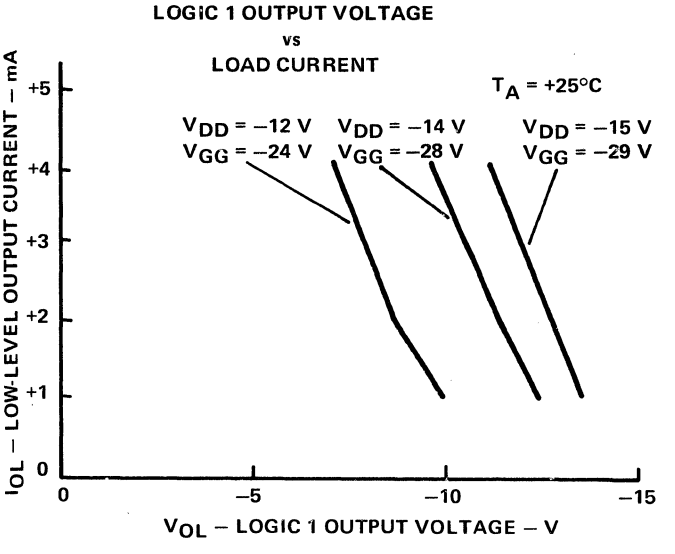
TMS3002LR - dual 50-bit shift register
TMS3003LR - dual 100-bit shift register

voltage waveforms



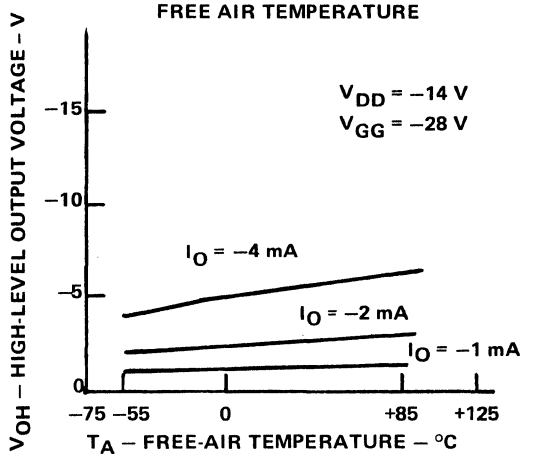
typical characteristics



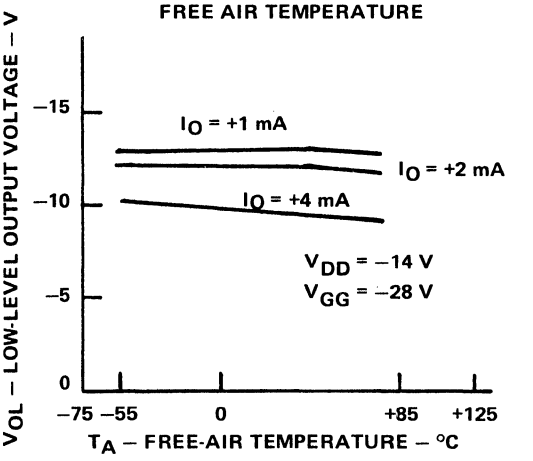


typical characteristics (continued)

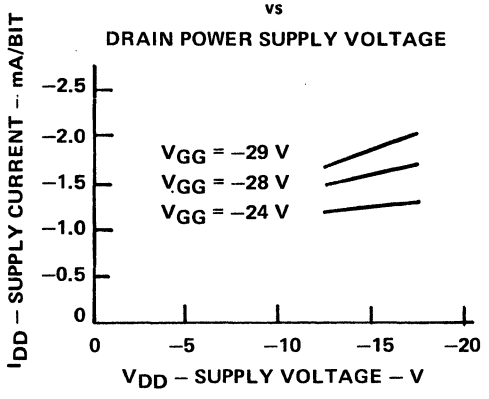
LOGIC 0 OUTPUT VOLTAGE
vs
FREE AIR TEMPERATURE



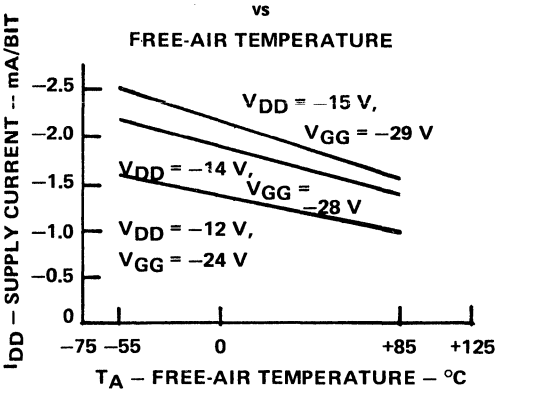
LOGIC 1 OUTPUT VOLTAGE
vs
FREE AIR TEMPERATURE



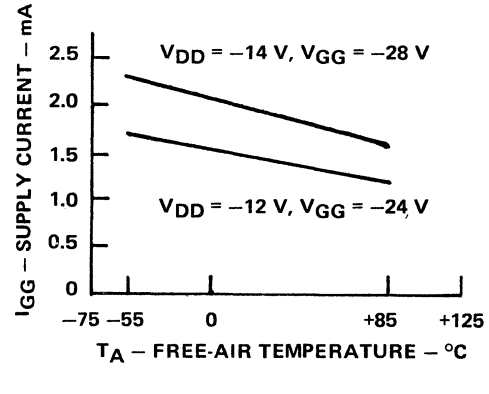
SUPPLY CURRENT (PER BIT)
FROM V_{DD} SUPPLY
vs
DRAIN POWER SUPPLY VOLTAGE



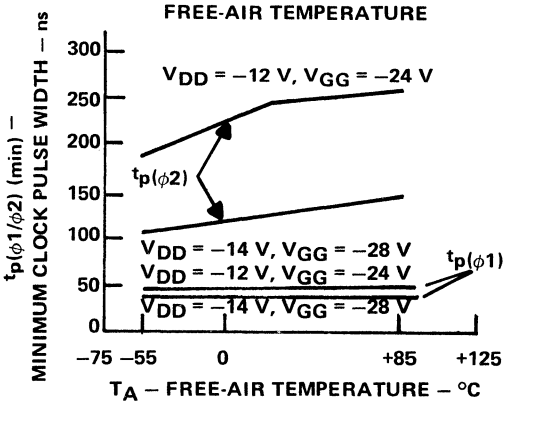
SUPPLY CURRENT (PER BIT)
FROM V_{DD} SUPPLY
vs
FREE-AIR TEMPERATURE



SUPPLY CURRENT FROM V_{GG} SUPPLY
vs
FREE-AIR TEMPERATURE



MINIMUM CLOCK PULSE WIDTH
vs
FREE-AIR TEMPERATURE

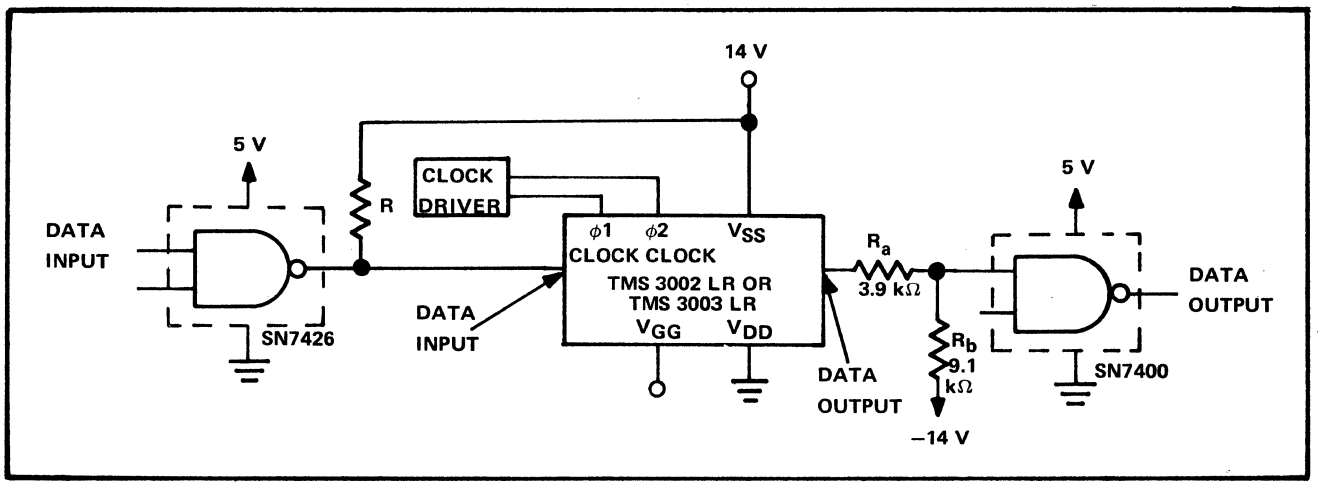


TMS3002LR - dual 50-bit shift register
TMS3003LR - dual 100-bit shift register

typical application data

1) MOS/TTL interface

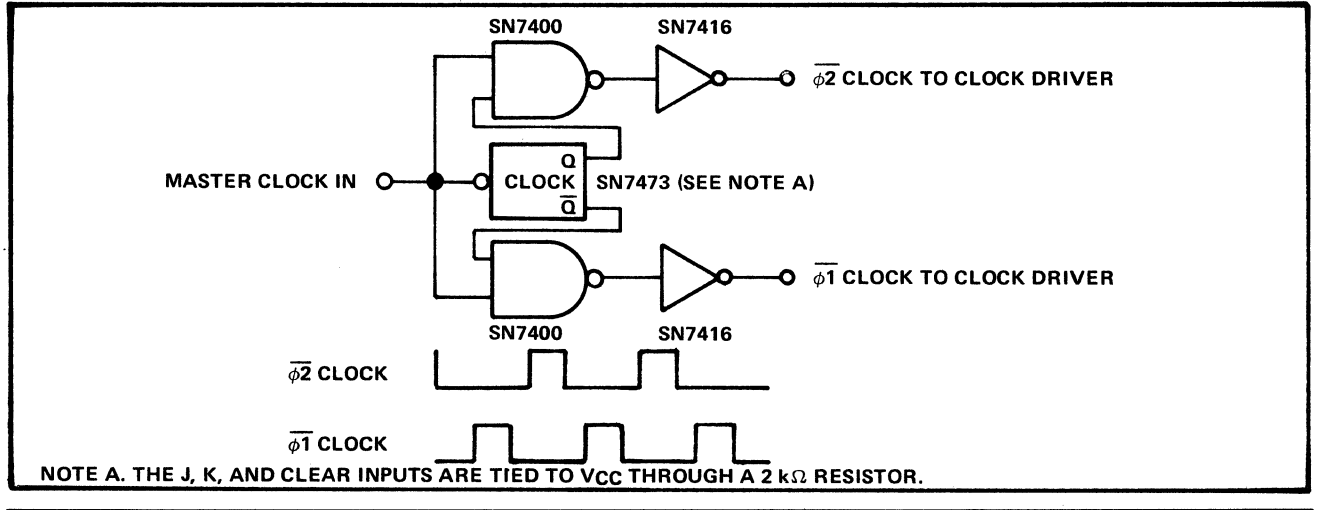
With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



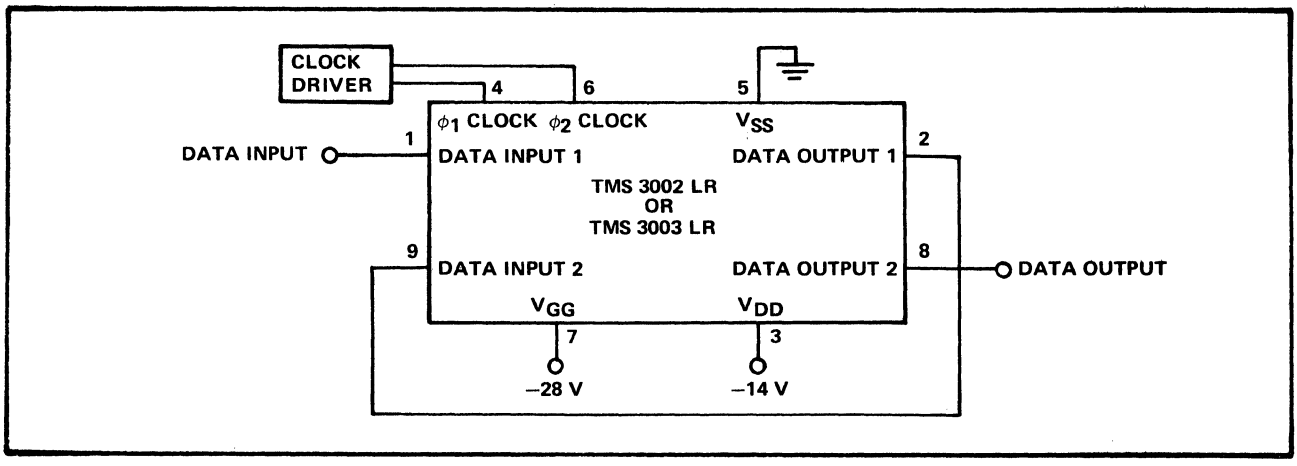
An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements — values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

At the output interface, the 9.1 kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9 kΩ resistor and the 9.1 kΩ resistor to −14 volts. The 3.9 kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

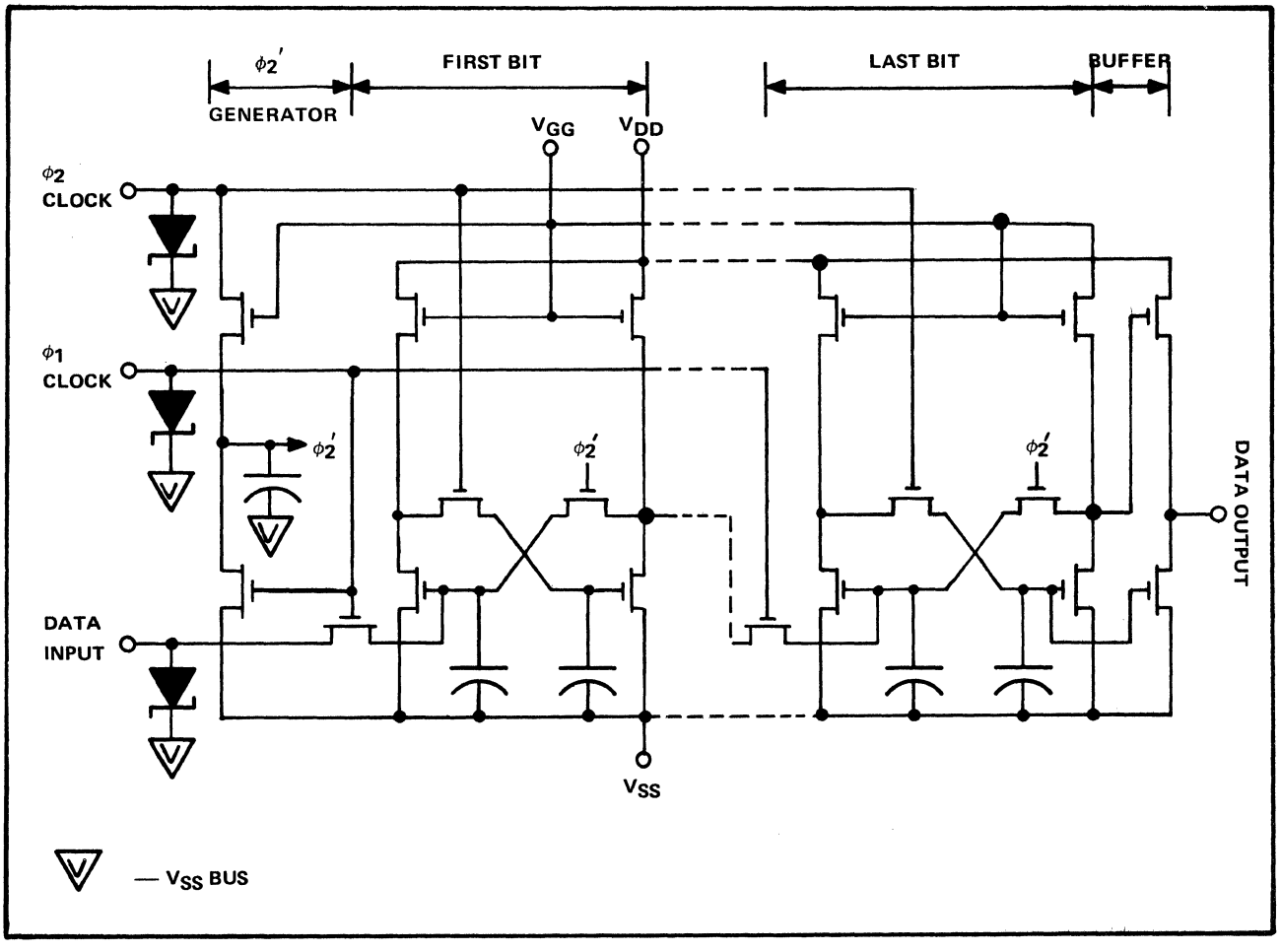
2) Two-phase clock generator



expansion to single 100- or 200-bit register



schematic (each register)



TMS3012JR – dual 128-bit accumulator
TMS3028LR – dual 128-bit shift register

preliminary information

FEATURING

- 256 bits of storage
- Single clock phase
- Static logic
- TTL compatible
- DC to 1 MHz operation
- Push-pull output buffers
- 16-Pin hermetic ceramic dual-in-line package (TMS 3012 JR)
- Recirculating control logic (TMS 3012 JR)

description

The TMS 3012 JR consists of two separate 128-bit static shift registers with independent input and output terminals and logic, within the circuit, for loading and recirculating information. Two power supplies and one external clock are required for operation. Three clocks are generated internally. Cross-coupled flip-flops are used to implement each bit of delay and enable data to be stored indefinitely between two clock pulses. The entire device is constructed on a single monolithic chip using thick-oxide techniques and MOS P-channel enhancement-mode transistors.

The TMS 3028 LR is identical to the TMS 3012 JR except for the fact that recirculate logic is not included on the chip and that the device is mounted in a TO-100 package instead of a ceramic dual-in-line package.

operation

Transferring data into the register and shifting the data in the register are accomplished when the ϕ_{IN} clock is at a logic 1; for long-term data storage, the ϕ_{IN} clock must be held at logic 0. Output appears on the positive-going edge of the ϕ_{IN} clock pulse.

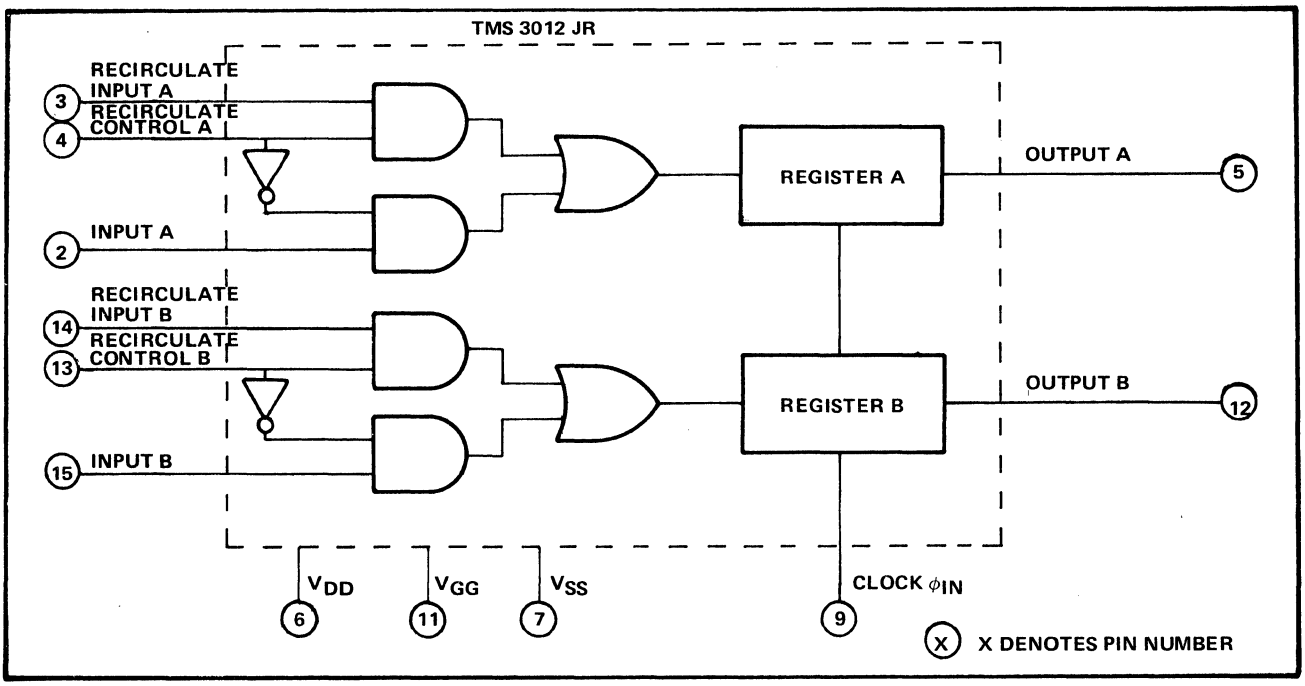
logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

functional diagram and pin breakout



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range* . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range* . . . . . −30 V to 0.3 V
Clock and data input voltage ranges* . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

* These voltage values are with respect to substrate terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−13	−14	−15	V
Supply voltage V_{GG}	−27	−28	−29	V
Width of data pulse, $t_{(data)}$ (See voltage waveforms)	0.4		10	μs
Width of clock pulses: t_p (Logic 1) (See voltage waveforms)	0.3		∞	μs
t_p (Logic 0) (See voltage waveforms)	0.6		5	μs
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)			5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			1	μs
Clock repetition rate	0		1	MHz

— CONTINUED —

recommended operating conditions (continued)

CHARACTERISTICS		MIN	NOM	MAX	UNITS
$V_{in(1)}$*	Data/Recirculate Control Logic 1 voltage	−9	−14	−15	V
$V_{in(0)}$*	Data/Recirculate Control Logic 0 voltage	0	0	−2	V
$V_{in(1)\phi}$*	Logic 1 clock input voltage	−9	−14	−15	V
$V_{in(0)\phi}$*	Logic 0 clock input voltage	0	0	−2	V
Data change time before clock change to 0 (t_{db})		0.2			μs
Data change time after clock change to 0 (t_{da})		0.2			μs
Recirculate control change time before clock change to 0 (t_{rb}) (See Note 2)		0.3			μs
Recirculate control change time after clock change to 0 (t_{ra}) (See Note 2)		0.3			μs

NOTES: 1. All voltages are with respect to V_{SS}.
2. TMS 3012 JR only.

To ensure correct data loading, the input should reach the desired level at least time t_{db} before the clock goes to logic 0, and should remain at that level for a time t_{da} after the clock has changed to 0. Similarly, the recirculate control input should not change state for a period t_{rb} before and t_{ra} after the clock change from logic 1 to logic 0.

electrical characteristics at nominal operating conditions and 25°C

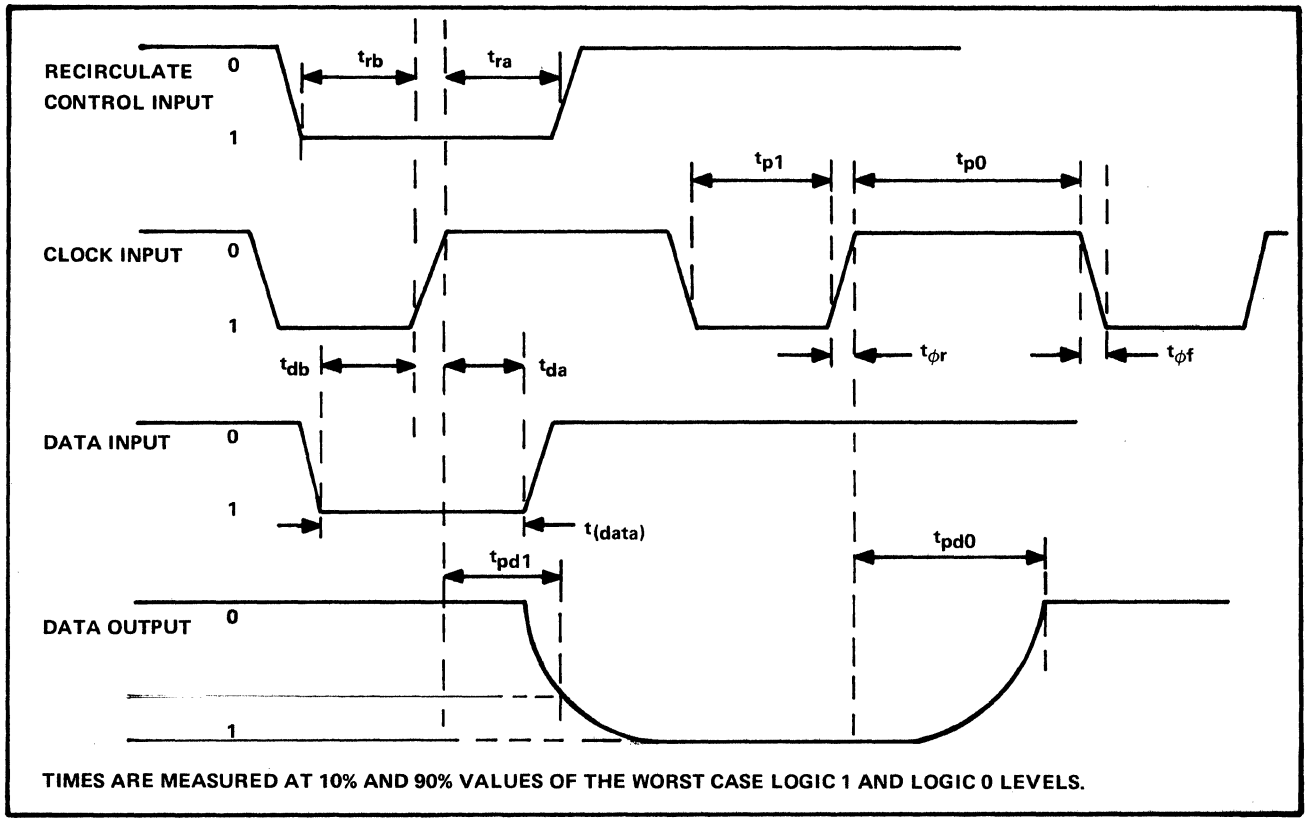
PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
$V_{out(1)}$	Logic 1 output voltage	R_L = 10 kΩ to V_{SS}	−11	−13		V
$V_{out(0)}$	Logic 0 output voltage	R_L = 10 kΩ to V_{SS}		−0.3	−1	V
$I_{in(1)}$	Data input, leakage current	V_{in} = −20 V			−0.5	μA
$I_{in(1)\phi}$	Clock input, leakage current	$V_{in\phi}$ = −20 V, V_{GG} = 0			0.5	μA
Z_{out}	Output impedance to ground	V_{out} = 0 to −1 V		0.7	1.5	kΩ
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −15 V, V_{GG} = −29 V		−23	−30	mA
I_{GG}	Supply current into V_{GG} terminal	V_{DD} = −15 V, V_{GG} = −29 V		−3	−5.5	mA

† Unless otherwise noted, R_L = 10 kΩ, and C_L = 10 pF.
‡ All other pins are at V_{SS}

dynamic electrical characteristics, V_{DD} = −14 V, V_{GG} = −28 V, T_A = 25°C

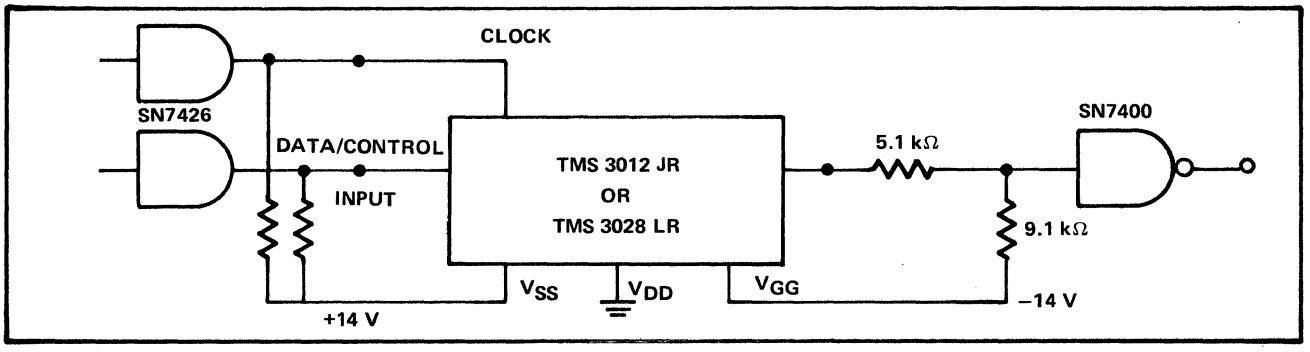
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logic 1 level from clock φ to data output	R_L = 10 kΩ to ground, C_L = 10 pF		500	700	ns
t_{pd0}	Propgation delay time to logic 0 level from clock φ to data output	R_L = 10 kΩ to ground, C_L = 10 pF		400	600	ns
C_{in}	Capacitance of data input	V_{in} = 0, f = 1 MHz, T_A = 25°C		3	5	pF
$C_{in\phi}$	Capacitance of clock input	$V_{in\phi}$ = 0, f = 1 MHz, T_A = 25°C		5	7	pF

voltage waveforms (TMS 3012 LR only)



interface circuits

a) TTL/DTL



b) MOS

No external components are required.

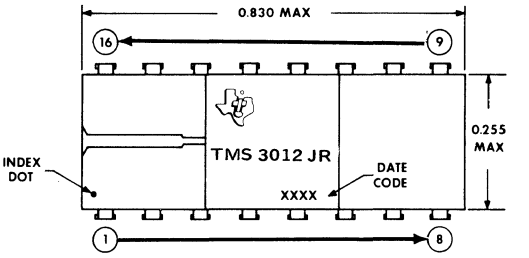
TMS3012JR – dual 128-bit accumulator
TMS3028LR – dual 128-bit shift register

mechanical data

The TMS 3012 JR is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers.

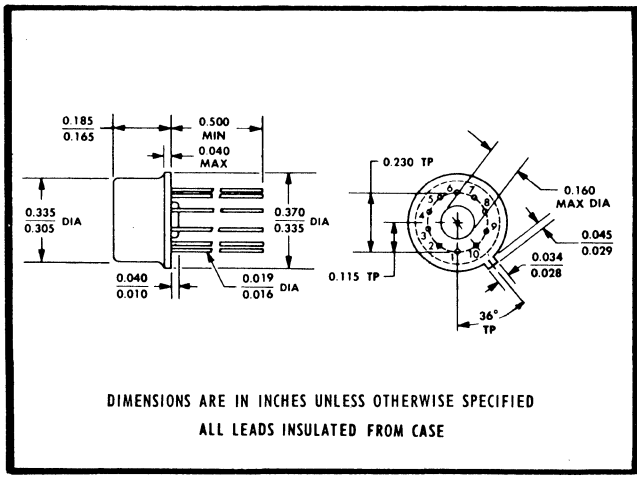
A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16).

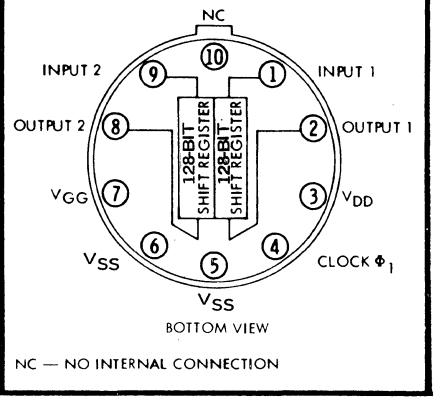
B. All dimensions are in inches.



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	9	Clock ϕ
2	Input A	10	No connection
3	Recirculate Input A	11	V_{GG}
4	Recirculate Control A	12	Output B
5	Output A	13	Recirculate Control B
6	V_{DD}	14	Recirculate Input B
7	V_{SS}	15	Input B
8	No connection	16	No connection

The TMS 3028 LR package outline is same as JEDEC TO-100 except for diameter of standoff.





FEATURING

- **Static logic**
- **DC to 1 MHz operation**
- **Low power dissipation**
- **Push-pull output buffers**
- **TTL compatible**

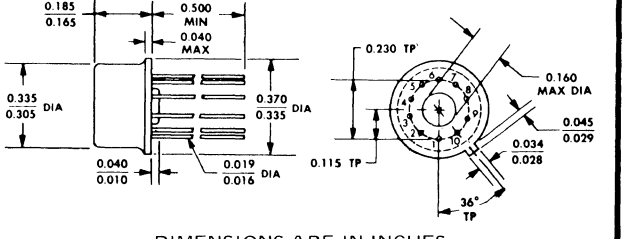
description

The TMS 3016 LR is a dual static shift register. This device contains two d-c to 1 MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low output impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at a logic 0 and the ϕ_2 clock at a logic 1.

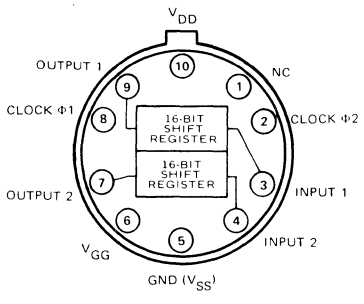
mechanical data and pin configuration

The package outline is the same as JEDEC TO-100 except for diameter of standoff.



DIMENSIONS ARE IN INCHES
UNLESS OTHERWISE SPECIFIED

PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE



BOTTOM VIEW

NC—NO INTERNAL CONNECTION

TMS3016LR
dual 16-bit static shift register

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1) . . . . . −30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage V_I range (See Note 1) . . . . . −30 V to 0.3 V
Power dissipation . . . . . 450 mW
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1. These voltage values are with respect to network ground terminal, V_{SS}.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Notes 2)	−9	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)		0	5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
$\phi 1$ clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
$\phi 2$ clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from $\phi 1$ clock to $\phi 2$ clock input pulse, $t_{\phi 12}$ (See voltage waveforms)	0.01		10	μs
Time interval from $\phi 2$ clock to $\phi 1$ clock input pulse, $t_{\phi 21}$ (See voltage waveforms)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.
3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at V_{DD} = −14 V, V_{GG} = −28 V, and T_A = 25°C.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	$V_I = -29$ V			0.5	μA
$I_{IL(\phi)}$	Logic 0 input current into either clock input	$V_\phi = -29$ V, $V_{GG} = 0$ V			50	μA
V_{OH}	Logic 0 output voltage	$I_O = 0$ mA			−1	V
		$I_O = -2.0$ mA		−2.6	−5	V
V_{OL}	Logic 1 output voltage	$I_O = 0$ mA	−12			V
		$I_O = 1.0$ mA	−11	−11.6		V
R_{OH}	Output resistance, logic 0	$I_O = -2.0$ mA			2.5	kΩ
R_{OL}	Output resistance, logic 1	$I_O = -1.0$ mA			3	kΩ
I_{DD}	Supply current from V_{DD} terminal*			−8	−12	mA
I_{GG}	Supply current from V_{GG} terminal*			−16	−25	mA
f_{max}	Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).

‡ All typical values are at $T_A = 25°C$.

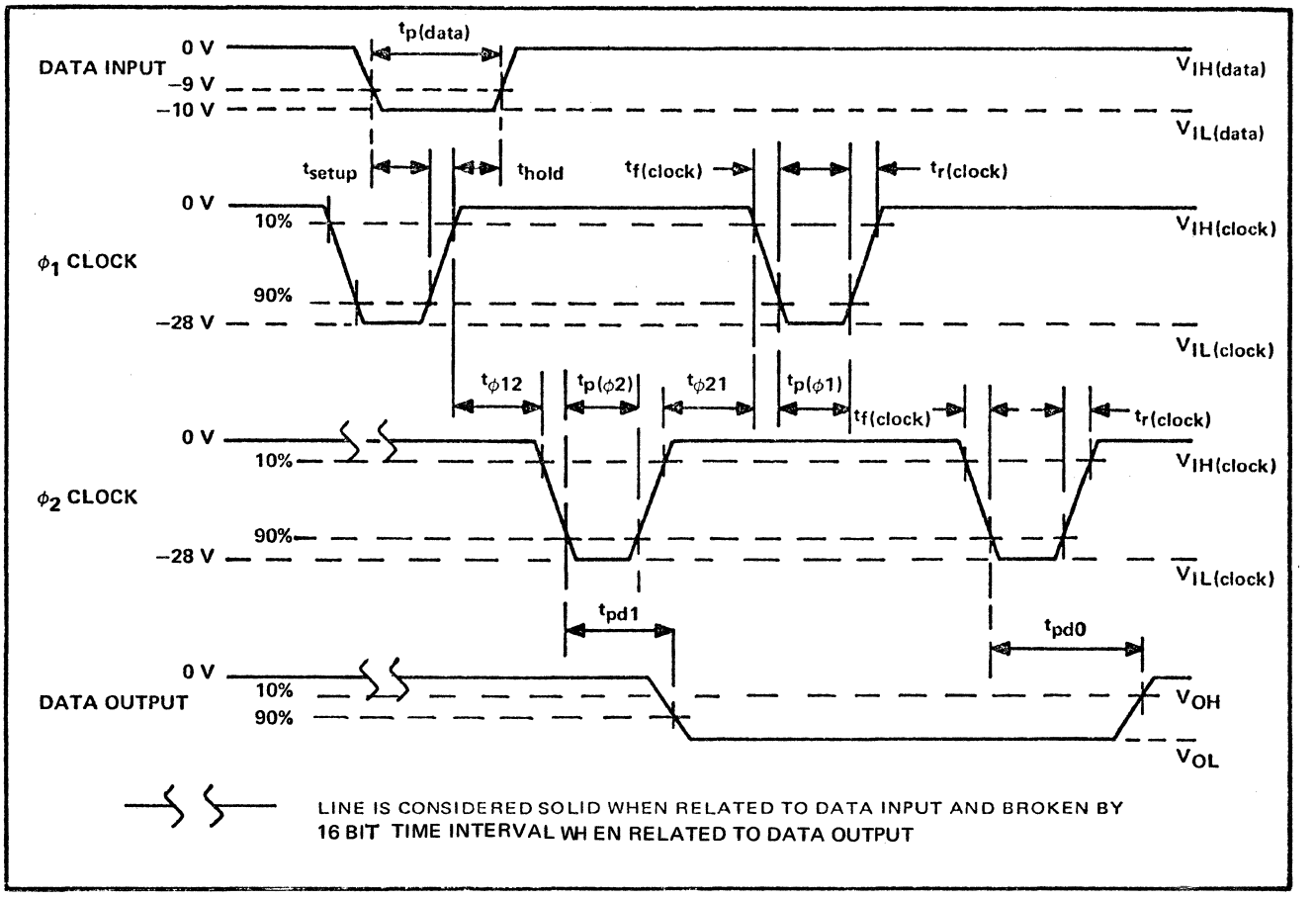
* Current into a terminal is a positive value.

switching characteristics, $V_{DD} = -14$ V, $V_{GG} = -28$ V, $R_L = 10$ mΩ, $C_L = 20$ pF, $T_A = 25°C$

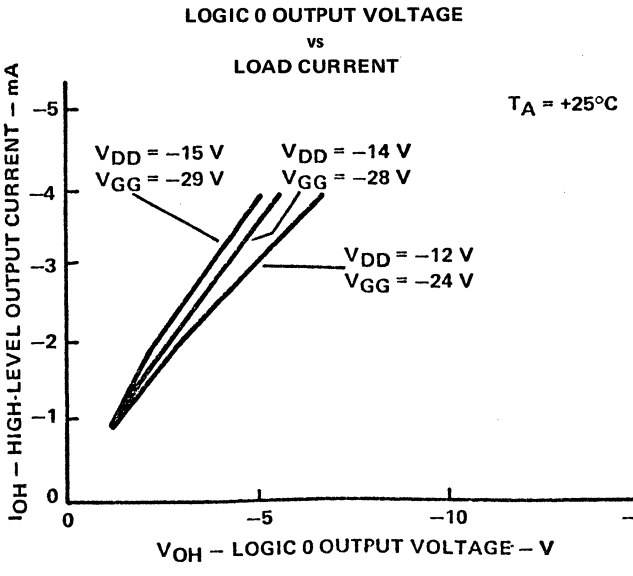
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms		250	400	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms		250	350	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	$V_I = 0$ V, $V_{I(\phi2)} = 0$ V, f = 1 MHz		6	10	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	$V_I = 0$ V, $V_{I(\phi1)} = 0$ V, f = 1 MHz		15	20	pF
C_{in}	Capacitance of data input	$V_I = 0$, f = 1 MHz		2	14	pF

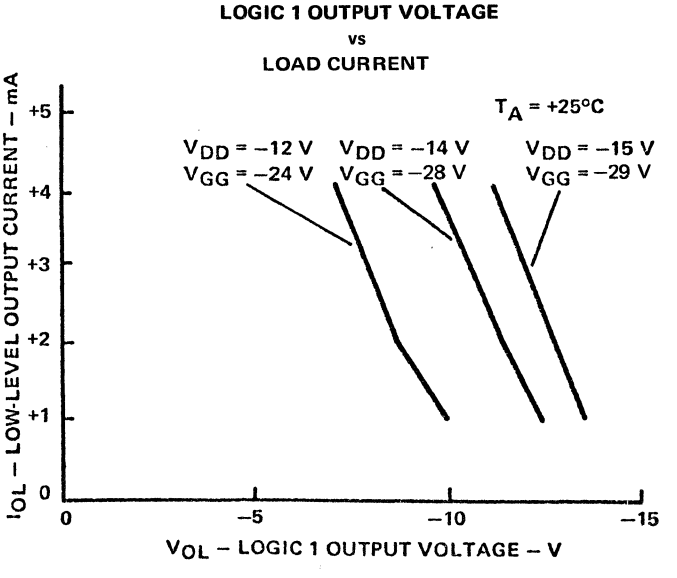
* $C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2 clock.

voltage waveforms



typical characteristics

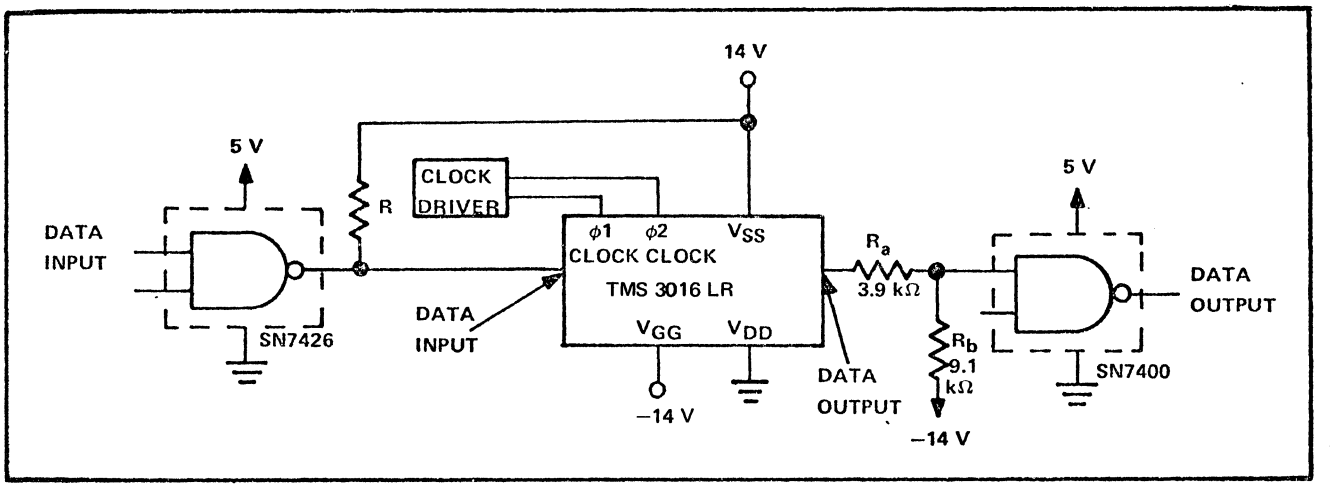




typical applications data

1) MOS/TTL interface

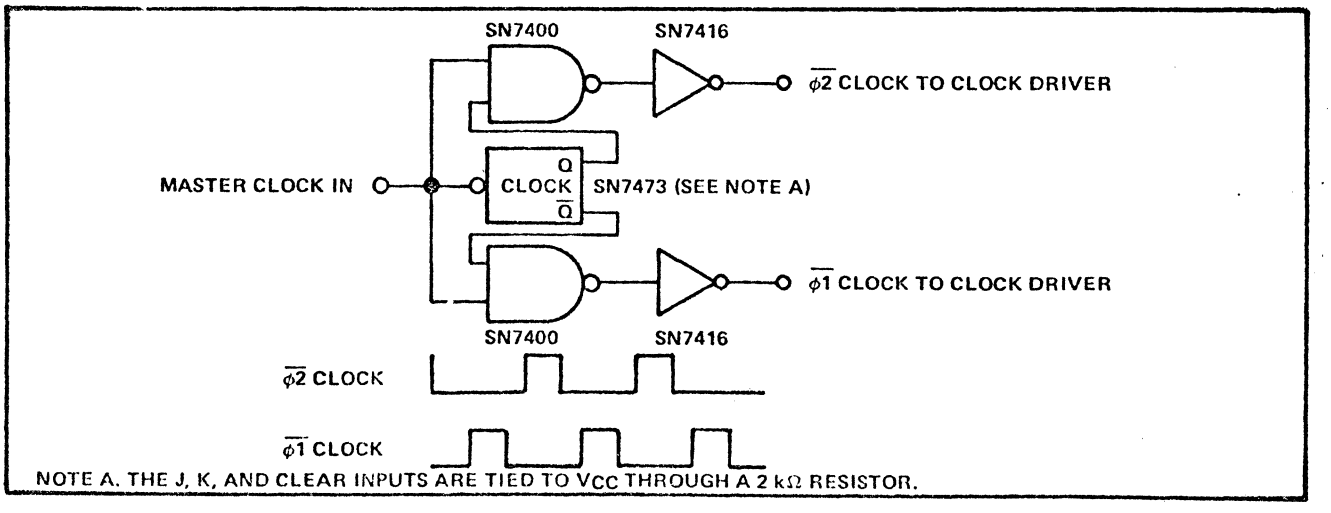
With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements — values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

At the output interface, the 9.1 kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9 kΩ resistor and the 9.1 kΩ resistor to −14 volts. The 3.9 kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

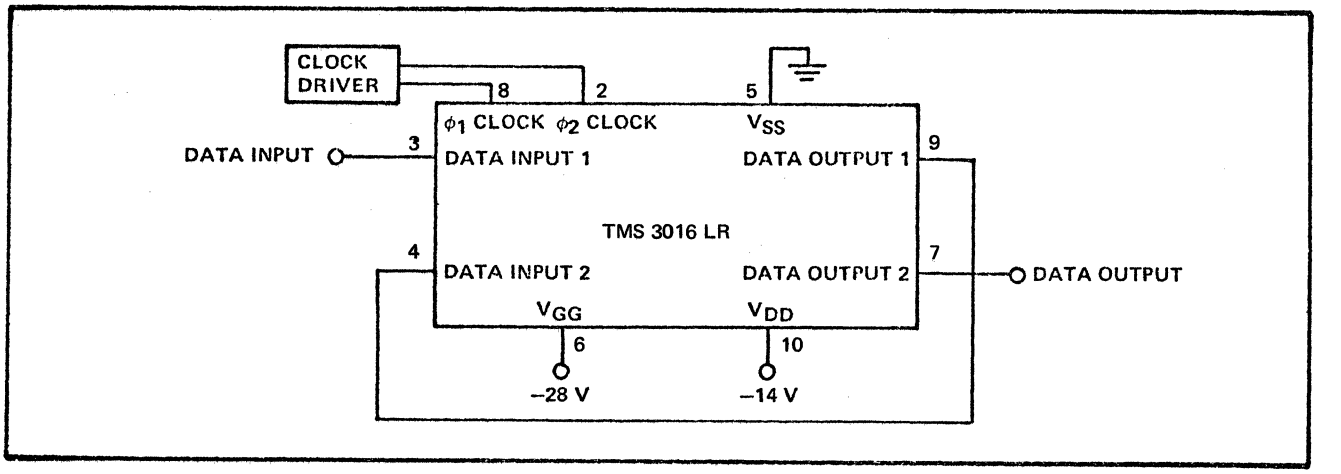
2) Two-phase clock generator



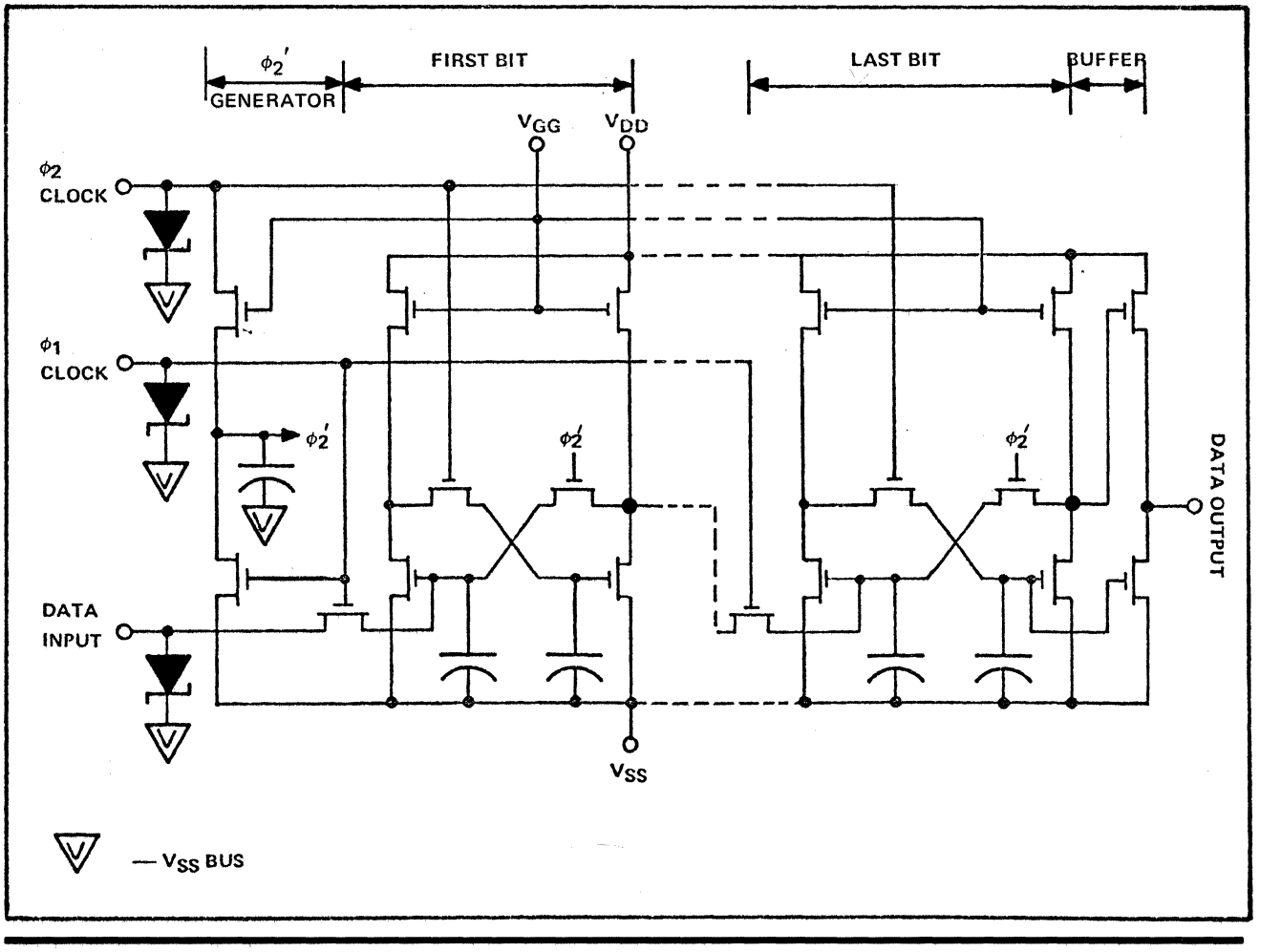
NOTE A. THE J, K, AND CLEAR INPUTS ARE TIED TO VCC THROUGH A 2 kΩ RESISTOR.

TMS3016LR
dual 16-bit static shift register

expansion to single 32 register



schematic (each register)



TMS3026JC
6-bit serial in parallel out static shift register

preliminary information

FEATURING

- **Static operation**
- **Single clock**
- **Single power supply**
- **TTL compatible**
- **Complementary parallel outputs**
- **Single ended output buffers**
- **16-pin ceramic dual-in-line packages**

description

The TMS 3026 JC is a 6-bit serial-input parallel-output static shift register, constructed on a single monolithic chip with MOS p-channel enhancement-mode transistors. Both true and complement are available at the parallel outputs. Each output has an unclocked single-ended output buffer. The output level is determined by different external load resistors and load power supply. One power supply, one clock, and ground are required for operation. Cross-coupled flip-flops are used to implement each bit of delay, enabling data to be stored indefinitely when the clock is grounded.

logic definition

Negative logic is assumed:

a) Logic 1 = most negative voltage

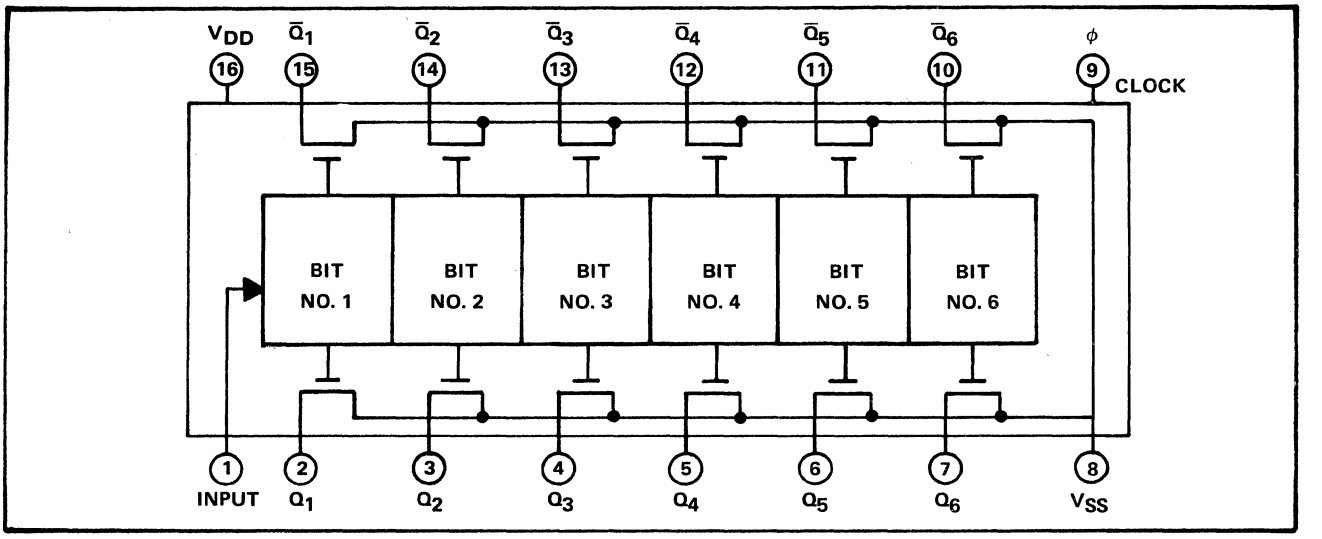
b) Logic 0 = most positive voltage

operation

Both transferring data into the register and shifting the data in the register are accomplished when the clock is at a logical 1. For long-term data storage, the clock must be held at logical 0. Output data appears on the positive-going edge of the clock pulse.

TMS3026JC
6-bit serial in parallel out static shift register

functional diagram and pin configuration



absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

Supply voltage V_{DD} range (See note) . . . . . −30 V to 0.3 V
Clock and data input voltage ranges (See note) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE: These voltage values are with respect to network V_{SS} terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Logical 1 data input voltage $V_{in(1)}$	−10	−12	−29	V
Logic 0 data input voltage $V_{in(0)}$	+0.3	0	−3	V
Logic 1 clock input voltage $V_{in(1)\phi}$	−10	−12	−29	V
Logic 0 clock input voltage $V_{in(0)\phi}$	+0.3	0	−3	V
Width of data pulse, $t_{p(data)}$ (See Voltage Waveforms)	1			μs
Rise time of clock pulse, $t_{r(clock)}$ (See Voltage Waveforms)			50	μs
Fall time of clock pulse, $t_{f(clock)}$ (See Voltage Waveforms)			50	μs
Clock repetition rate	0		0.25	MHz
Width of clock pulses, $t_{p(clock\ \phi)}$ (See Voltage Waveforms)	1			μs
Supply voltage V_{DD}	−23	−24	−29	V

electrical characteristics (at nominal operating conditions and 25°C unless otherwise noted)

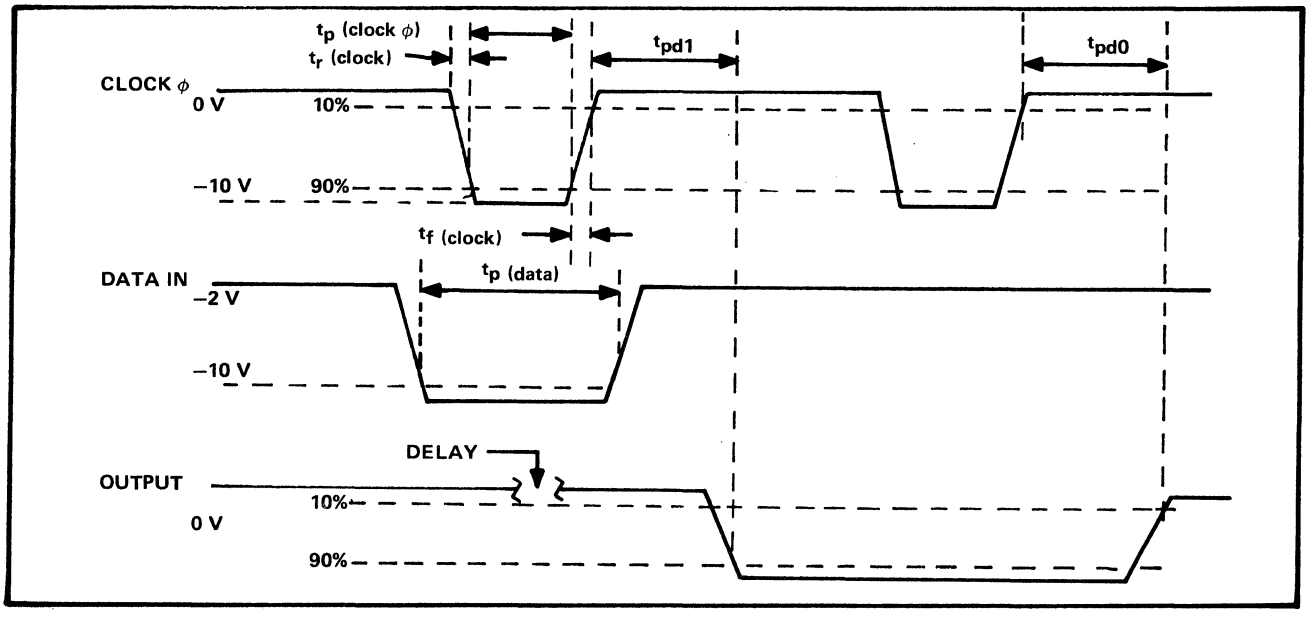
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{out(1)}$	Logic 1 output voltage (Note 1)			24		V
$V_{out(0)}$	Logic 0 output voltage	I_{out} = 1 mA		0.7	1.2	V
$V_{out(0)}$	Logic 0 output voltage	I_{out} = 2 mA		2	4	V
I_{in}	Input leakage current	V_{in} = −29 V			0.5	μA
$I_{in(\phi)}$	Clock leakage current	$V_{in\phi}$ = −29 V			0.5	μA
I_{DD}	Supply current			1.2	2.0	mA
f	Operating frequency		0		0.250	KHz

NOTE 1: For a logic 1 the MOS single-ended buffer is "off" and the output voltage is determined by the external load resistor and power supply voltage.

dynamic electrical characteristics (at nominal operating conditions and 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logic 1 level from clock ϕ to data output	See Voltage Waveforms		2	4	μs
t_{pd0}	Propagation delay time to logic 0 level from clock ϕ to data output	See Voltage Waveforms		1	2	μs
C_{in}	Capacitance of data input	V_{in} = 0, T_A = 25°C, f = 1 MHz		3.0	5.0	pF
$C_{in\phi}$	Capacitance of the clock input	$V_{in\phi}$ = 0, T_A = 25°C, f = 1 MHz		3.0	5.0	pF

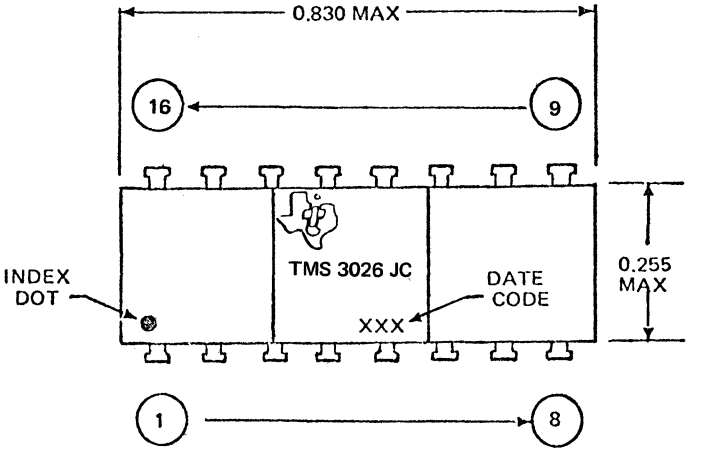
voltage waveforms



TMS3026JC
6-bit serial in parallel out static shift register

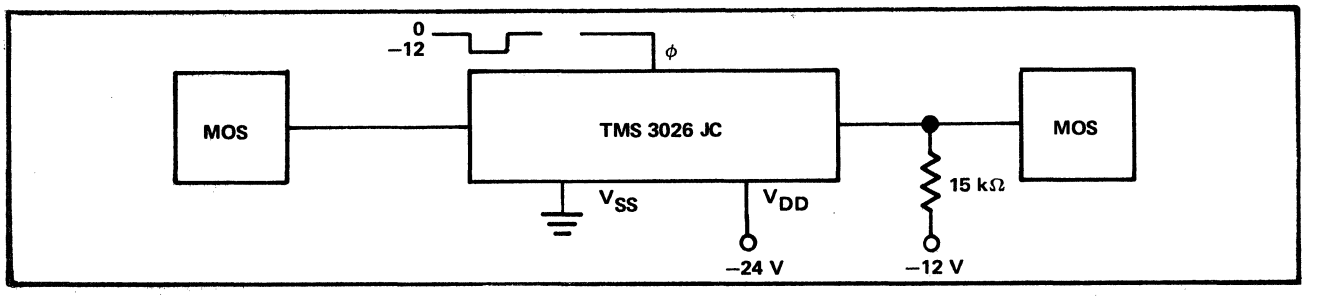
mechanical data

The TMS 3026 JC is mounted in a 16-lead, hermetically sealed, dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is intended for insertion in 0.024 ± 0.002-inch-diameter mounting holes, which are spaced 0.300 inches between row centerlines.

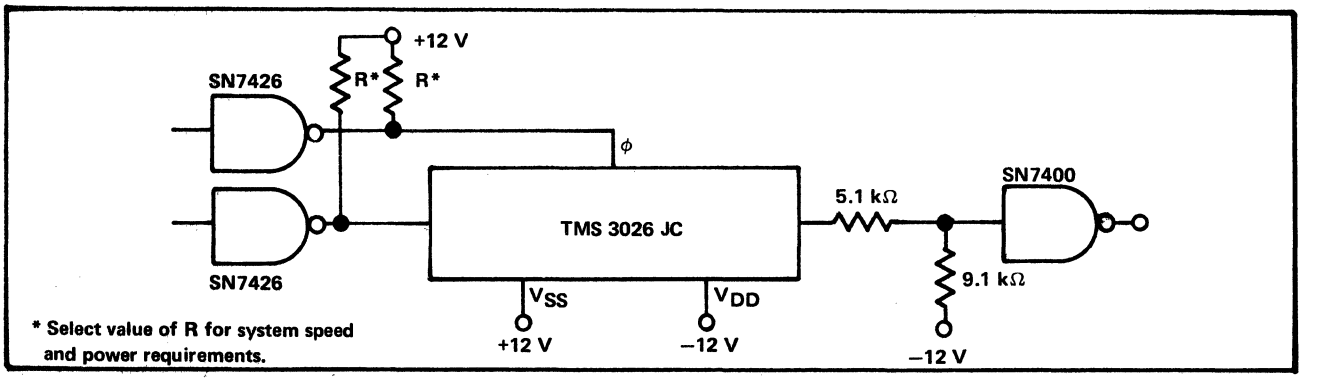


interface

a) MOS interface



b) TTL interface



TMS3101LC
dual 100-bit static shift register

preliminary information

FEATURING

- DC to 2.5 MHz operation
- Low power dissipation
- Direct interface with DTL/TTL
- Static operation
- Push-pull output buffer
- Low threshold technology

description

The TMS 3101 LC contains two 100-bit static shift registers constructed on a single monolithic chip, using thick-oxide techniques and P-channel enhancement mode transistors. Each register has independent input and output terminals, common clocks and power, and can operate from dc to 2.5 MHz. The inputs, which are zener protected, can be driven directly from DTL/TTL levels, and the register outputs can drive DTL/TTL circuits without the addition of external components.

logic definition

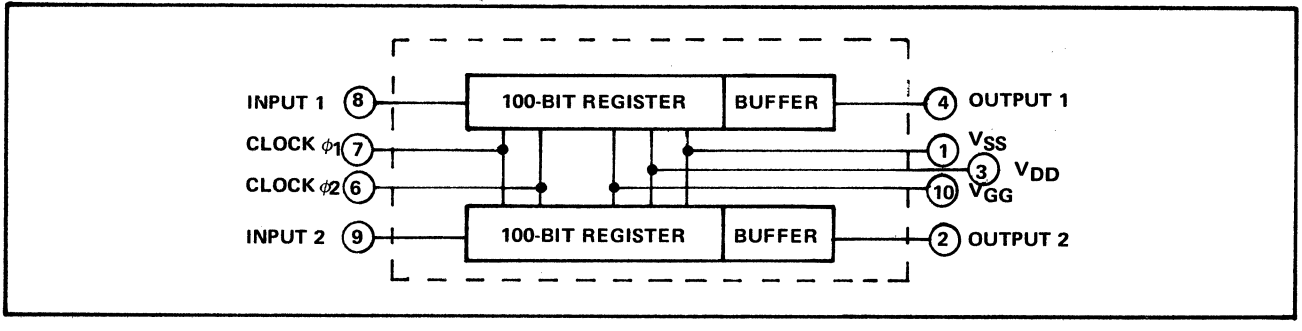
a) Logic 1 = most positive (HIGH) voltage

b) Logic 0 = most negative (LOW) voltage

operation

Cross-coupled flip-flops are used to implement each register bit and permit data to be stored indefinitely between clock pulses. Two external clock pulses are required for operation. Data is transferred into the register when clock pulse ϕ_1 is at a Low level. Data is shifted when clock pulse ϕ_1 is returned to a High level and clock pulse ϕ_2 is pulsed to a Low level. Output data appears on the High-to-Low transition of clock pulse ϕ_2. For long-term storage, clock pulse ϕ_1 must be held at a High level and clock pulse ϕ_2 at a Low level.

functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to +85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1. These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels (Note 2)				
Input High level V_{IH}	+3.5		+5.25	V
Input Low level V_{IL}	−13		0.8	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	+3		+5.25	V
Clock Low level $V_{\phi L}$	−13	−12	−11	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			3	μs
Clock pulse width 1 (See waveforms) $PW_{\phi 1}$	0.150		10	μs
Clock pulse width 2 $PW_{\phi 2}$	0.150		∞	μs
Pulse spacing				
Clock delay $t_{D\phi 12}$			10	μs
Clock delay $t_{D\phi 21}$			10	μs
Data setup t_{DS}	150			ns
Data hold t_{DH}	10			ns
Pulse overlap				
Clock (See Note 2)				ns
Pulse Repetition Rate PRR				
Data (See Note 3)	0		2.5	MHz
Clock (See Note 3)	0		2.5	MHz

NOTES: 2. Both clocks should not be simultaneously more than 2 V below V_{SS}.
3. C_L = 10 pF, one TTL load.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input current		V_I = 0 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current		V_I = −12 V,	V_{SS} = +5 V			20	μA
Output Voltage Levels								
	V_{OL}	Output LOW level	(See Note 4) 1 TTL load				+0.4	V
	V_{OH}	Output HIGH level	(See Note 4) 1 TTL load		+3.0	+3.5		V
	V_{OL}	Output LOW level	(See Note 4) MOS load (3101)		3.6			V
	V_{OH}	Output HIGH level	(See Note 4) MOS load (3101)				+0.4	V
Output Current								
	I_{OSC}	Short circuit						mA
Power Supply Current Drain								
	I_{SS}	Substrate supply	V_{out} = V_{OH} (See Note 5)			16	20	mA
	I_{DD}	Drain supply	See Note 6				0.5	mA
	I_{GG}	Gate supply	V_{out} = V_{OH} (See Note 5)			−16	−20	mA
	P_D	Power dissipation				270	360	mW

NOTES: 4. For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and 20 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

5. The device uses saturated logic. The current sourced by the 5 V power supply is sunk by the −12 V power supply.

6. Does not include output stage load or transient current. In the MOS load mode, the current will consist of transients due to capacitor discharge and/or leakage current. In the TTL load mode the current is the current sunk by the TTL (up to 1.6 mA).

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay								
	t_{DLH_1}	Output LOW Level	C_L = 10 pF,	TTL gate load		50	75	ns
	t_{DHL_1}	Output HIGH Level	C_L = 10 pF,	TTL gate load		100	125	ns
	t_{DLH_2}	Output HIGH Level	C_L = 10 pF,	MOS load		60	85	ns
	t_{DHL_2}	Output LOW Level	C_L = 10 pF,	MOS load		120	150	ns
Capacitance								
	C_{IN}	Input	V_I = 0 V,	f = 1 MHz		9	12	pF
	C_ϕ	Clock	V_I = 0 V,	f = 1 MHz		48	55	pF

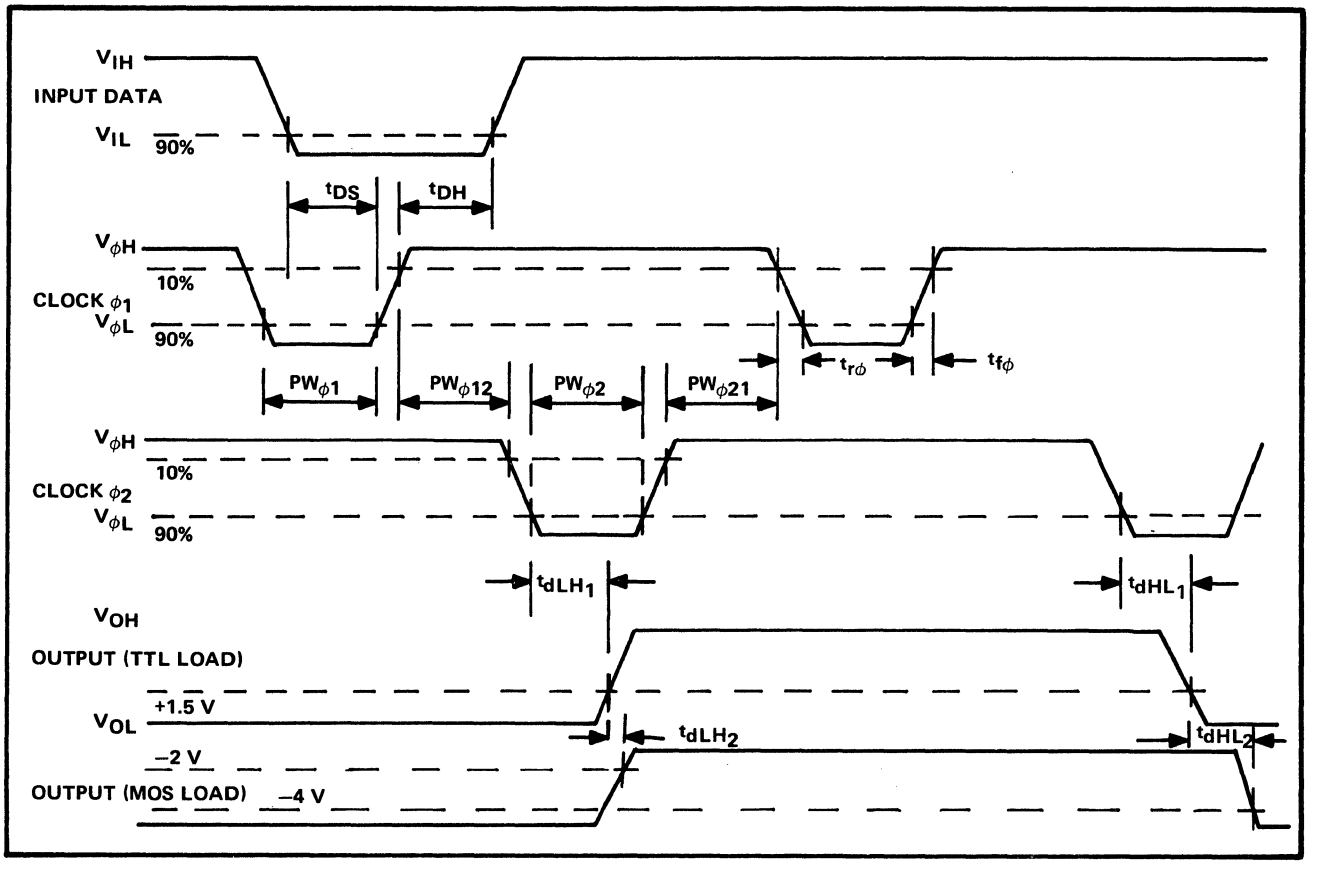
mechanical data and pin configuration

The TMS 3101 LC package outline is same as JEDEC TO-100 except for diameter of standoff.

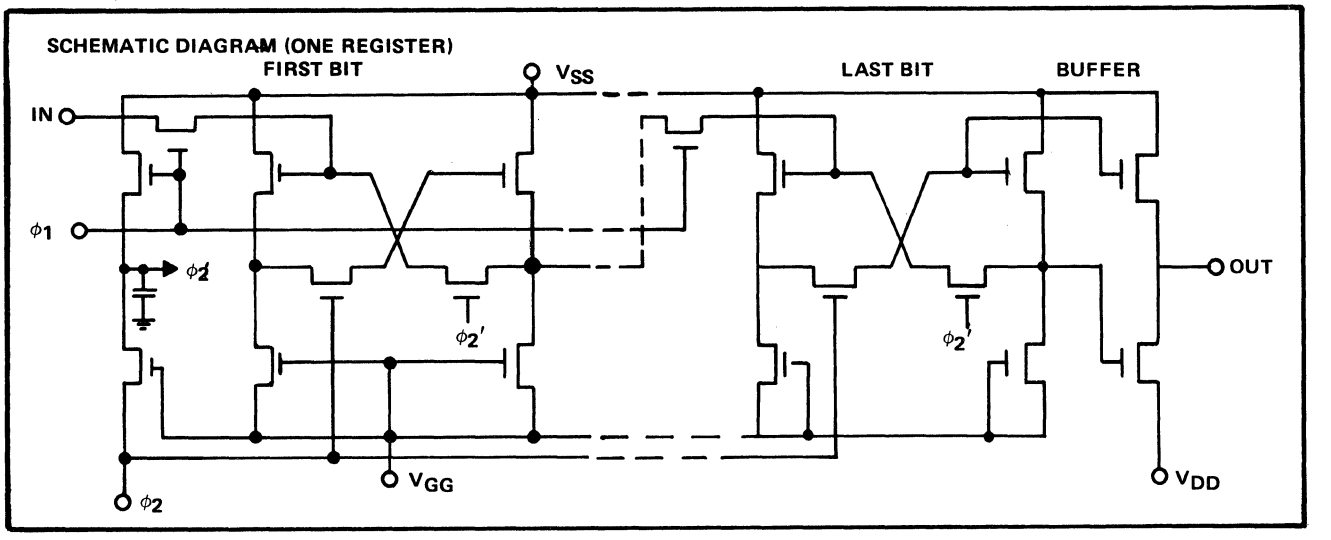
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	4	Output 1	7	Clock ϕ_1	10	V_{GG}
2	Output 2	5	No connection	8	Input 1		
3	V_{DD}	6	Clock ϕ_2	9	Input 2		

TMS3101LC
dual 100-bit static shift register

timing diagram and voltage waveforms

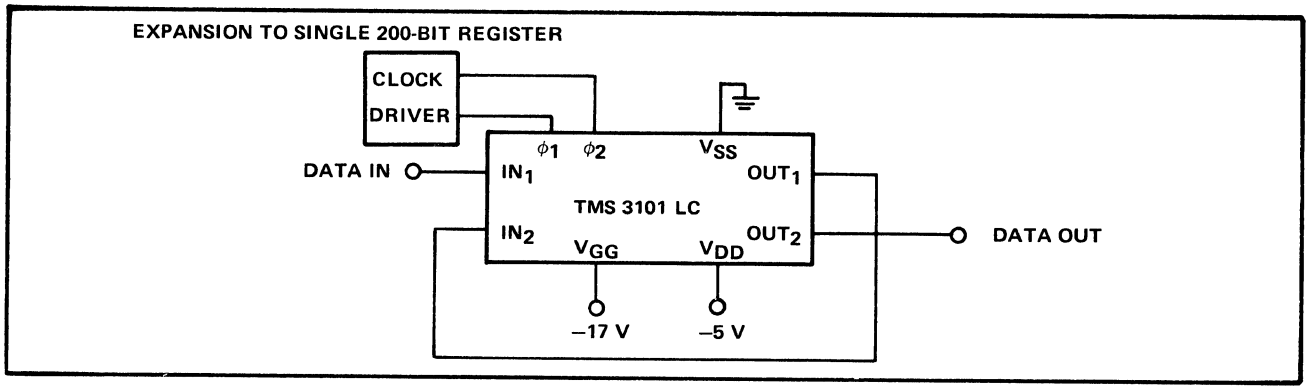


circuit diagram

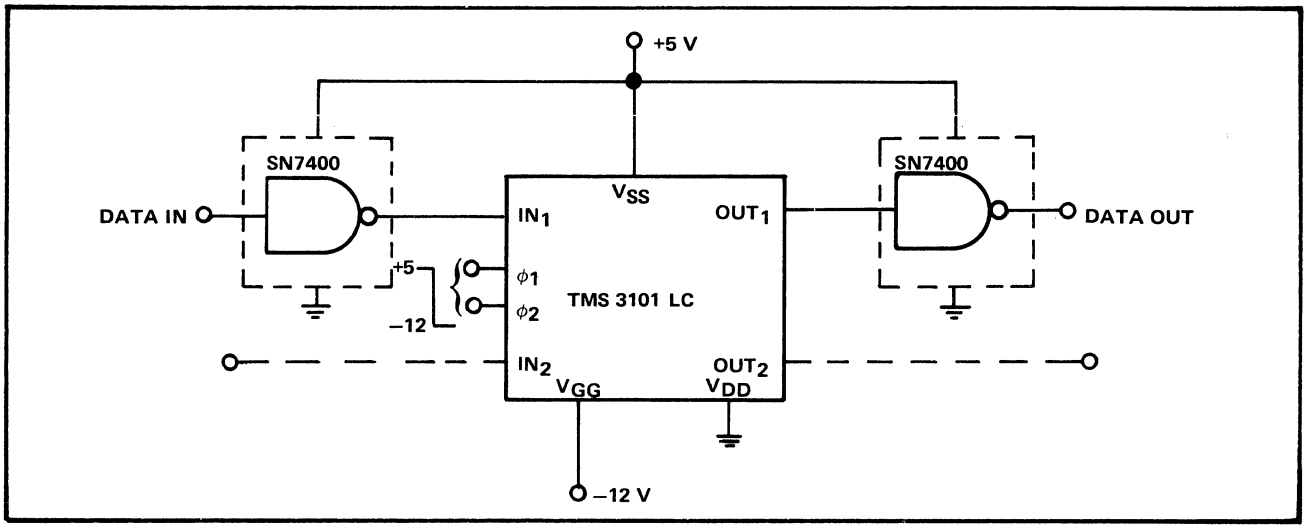


interface circuits

a) MOS



b) TTL



TMS3112JC
hex 32-bit static shift register

preliminary information

FEATURING

- Single clock (TTL levels)
- DTL/TTL compatible
- DC to 1 MHz
- Static operation
- Loading and recirculating control logic
- Gated-output control logic
- Ceramic dual-in-line package
- Single-ended (open drain) buffer
- Low-threshold technology

description

The TMS 3112 JC contains six separate 32-bit static shift registers constructed on a single monolithic chip, using thick-oxide techniques and P-channel enhancement-mode low-threshold MOS transistors.

A single clock is required for operation. The clock and all inputs can be driven directly from DTL/TTL logic levels and each register output can drive DTL/TTL circuits. The device also contains common control logic for loading, recirculation, and output enable.

logic definition

a) Logic 1 = most positive (High) voltage

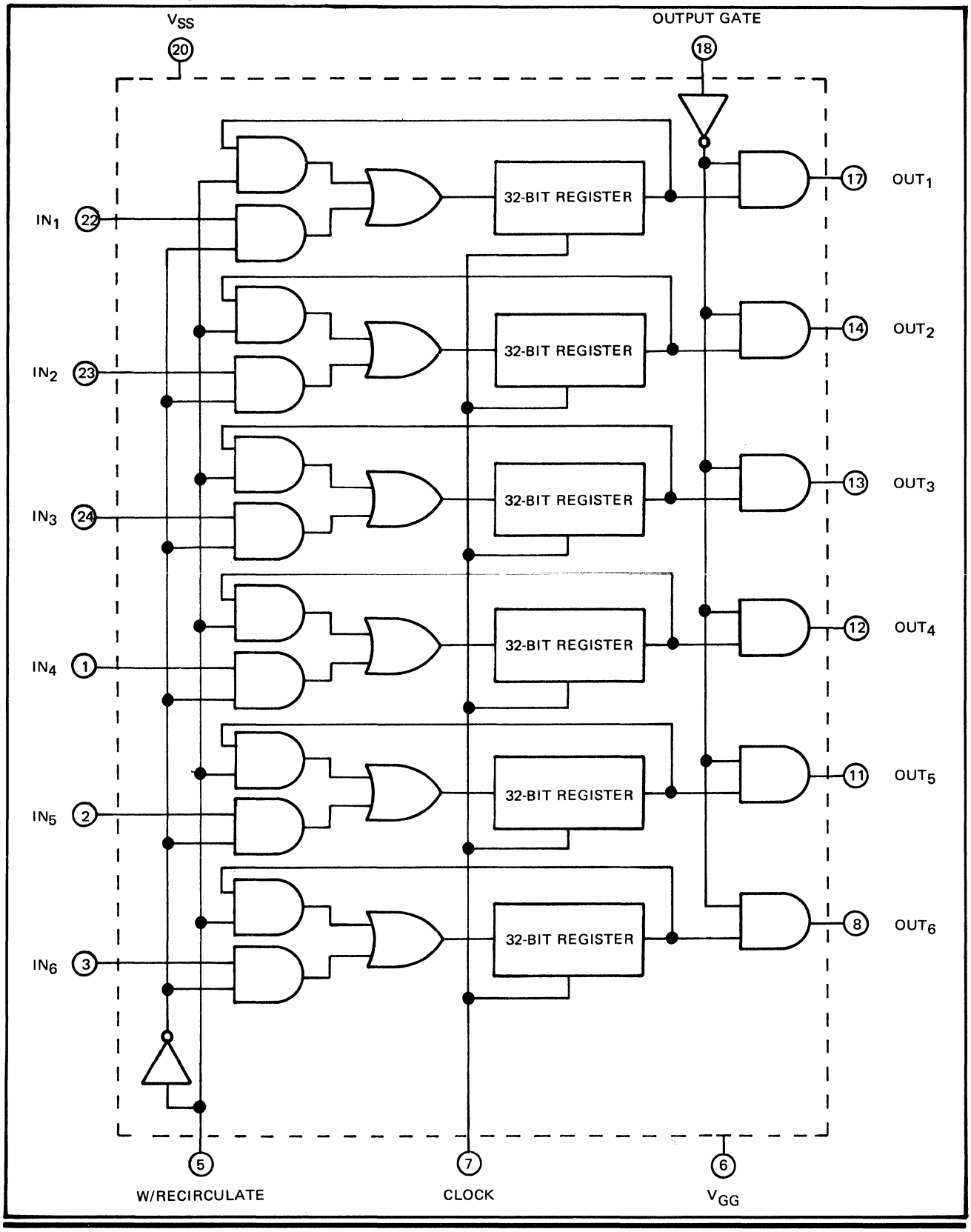
b) Logic 0 = most negative (Low) voltage

operation

Cross-coupled flip-flops are used to implement each register bit and permit data to be stored indefinitely between internal clock pulses. A single external clock pulse is required for operation. Data is transferred into the register when the clock pulse and recirculate control are at a Low level. Output data appears on the Low-to-High transition of the clock pulse. Data can be read out when the output gate control is held at a Low level. Recirculating data occurs when the recirculation control is at a High level.

The registers can drive DTL/TTL loads by using a 7.5-kΩ pull-down resistor connected between the output terminal and the V_{GG} supply.

functional block diagram and pin configuration



TMS3112JC
hex 32-bit static shift register

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{GG} range (See Note) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note) . . . . . −20 V to 0.3 V
Data input voltage range (See Note) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to +85°C
Storage temperature range . . . . . −55°C to +150°C

NOTE: These voltage values are with respect to V_{SS} (substrate).

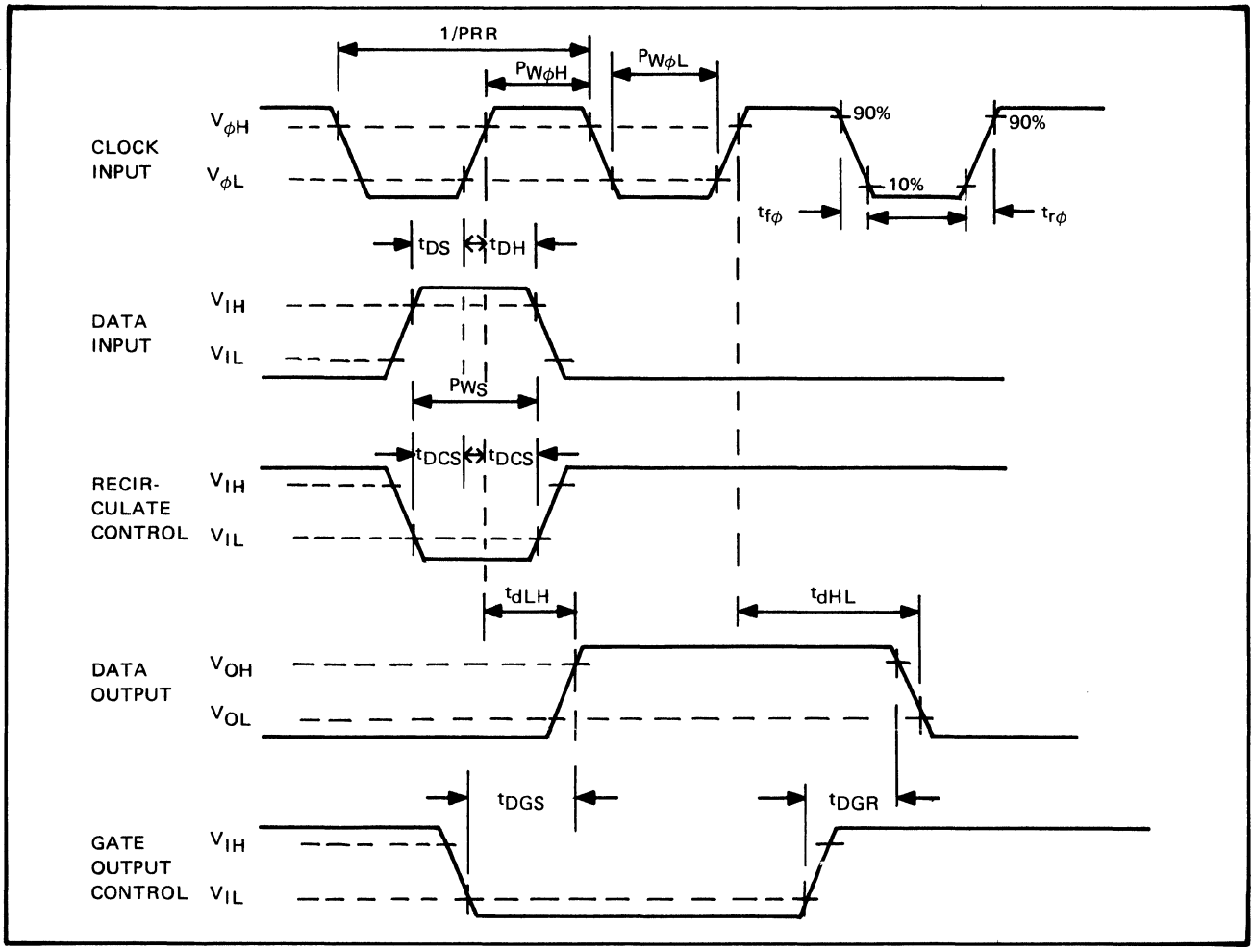
recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Gate supply V_{GG}	−11	−12	−13	V
Input High level V_{IH}	+3.5			V
Input Low level V_{IL}			+0.6	V
Clock High level $V_{\phi H}$	+3.5			V
Clock Low level $V_{\phi L}$			+0.6	V
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5000	ns
Clock High level $PW_{\phi H}$	600			ns
Clock Low level $PW_{\phi L}$	300			ns
Recirculate PW_s	600			ns
Output gate hold time t_{DGS}		180	250	ns
Output gate release time t_{DGR}		180	250	ns
Data setup t_{DS}	300			ns
Data hold t_{DH}	300			ns
Clock to store/recirculate t_{DCS}	300			ns
Clock PRR	0		1	MHz

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

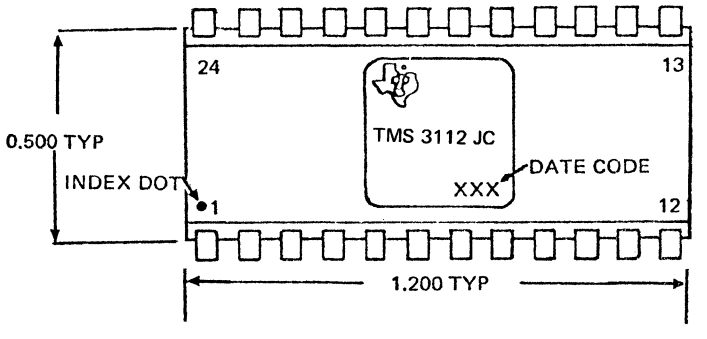
	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input current	V_I = +0.6 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current	V_ϕ = +0.6 V,	V_{SS} = +5 V			500	nA
V_{OL}	Output Low level	R_L = 7.5 kΩ to V_{GG},	I_{sink} = 1.6 mA			+0.5	V
V_{OH}	Output High level	R_L = 7.5 kΩ to V_{GG}		+4			V
I_{SS}	Substrate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15	20	mA
I_{GG}	Gate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15	20	mA
P_D	Power dissipation				255	340	mW
t_{dLH}	Output Low level	R_L = 7.5 kΩ,	C_L = 10 pF, TTL gate	350	450	600	ns
t_{dHL}	Output High level	R_L = 7.5 kΩ,	C_L = 10 pF, TTL gate	350	500	600	ns
C_{IN}	Input	V_I = 0 V,	f = 1 MHz		5	7	pF
C_ϕ	Clock	V_I = 0 V,	f = 1 MHz		6	7	pF

timing diagram and voltage waveforms



mechanical data and pin configuration

The TMS 3112 JC is mounted in a 24-pin hermetically sealed dual-in-line package consisting of gold-plated, ceramic sandwich body, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers. Pin-to-pin spacing is 0.100 inches.

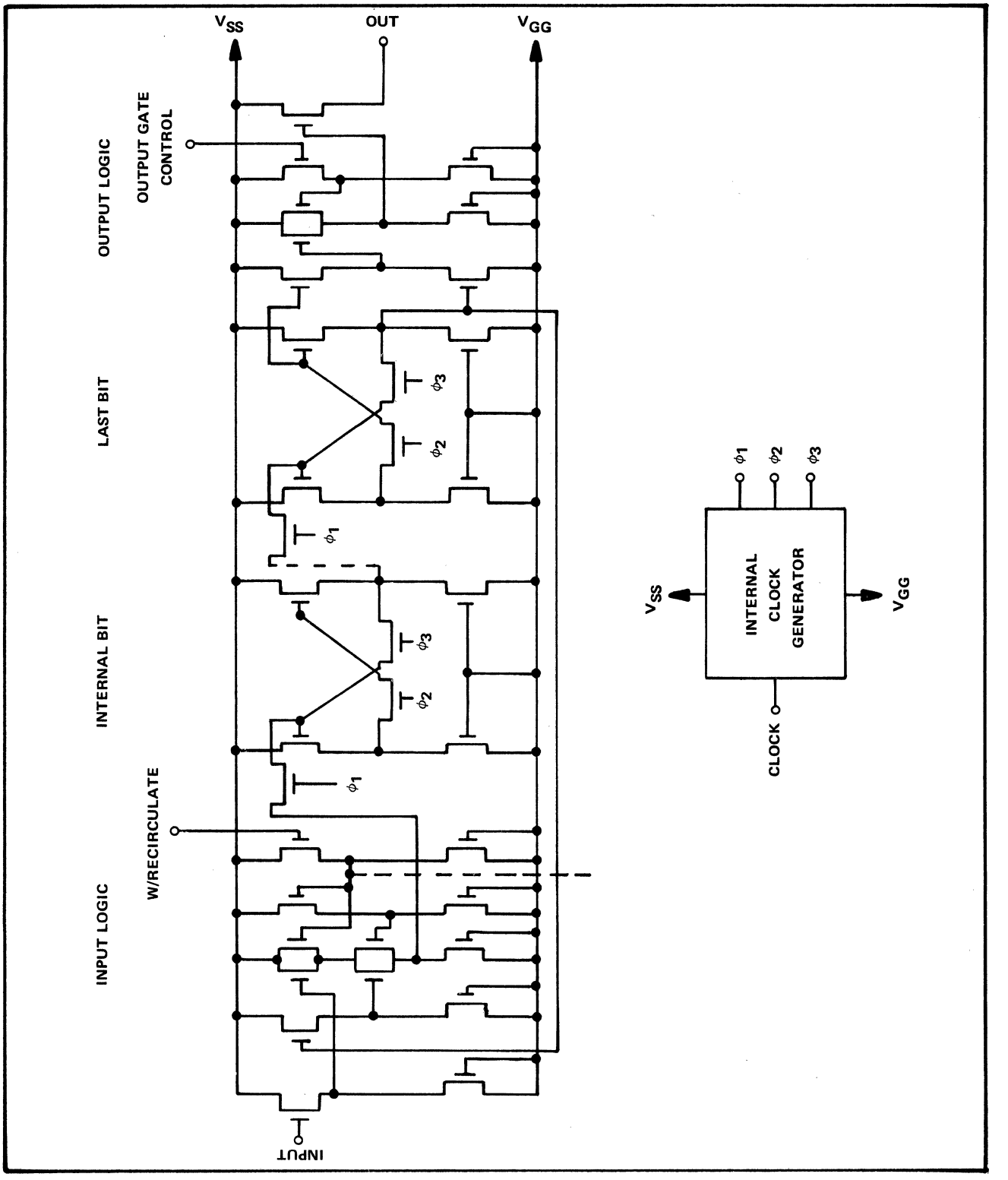


TERMINALS

PIN	FUNCTION	PIN	FUNCTION
1	Input 4	13	Output 3
2	Input 5	14	Output 2
3	Input 6	15	No connection
4	No connection	16	No connection
5	W/Recirculate control	17	Output 1
6	V_{GG}	18	Output gate control
7	Clock	19	No connection
8	Output 6	20	V_{SS}
9	No connection	21	No connection
10	No connection	22	Input 1
11	Output 5	23	Input 2
12	Output 4	24	Input 3

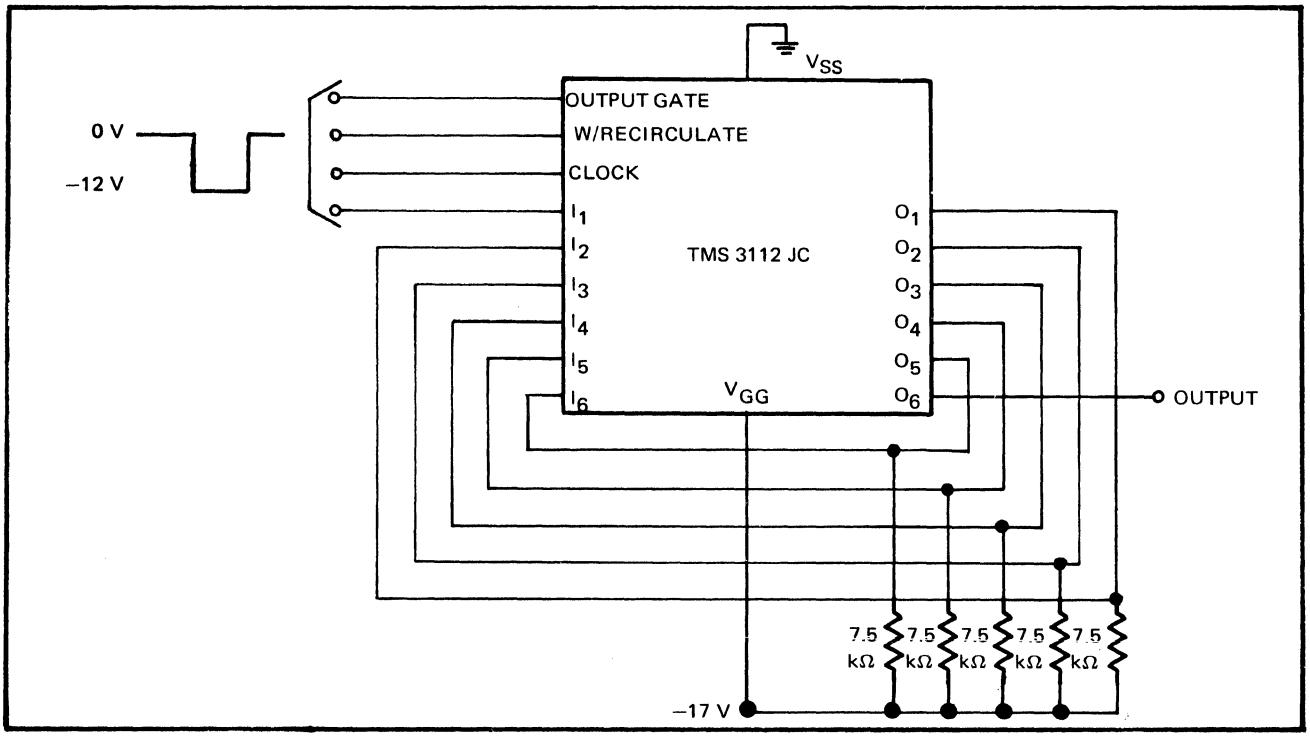
TMS3112JC
hex 32-bit static shift register

circuit diagram

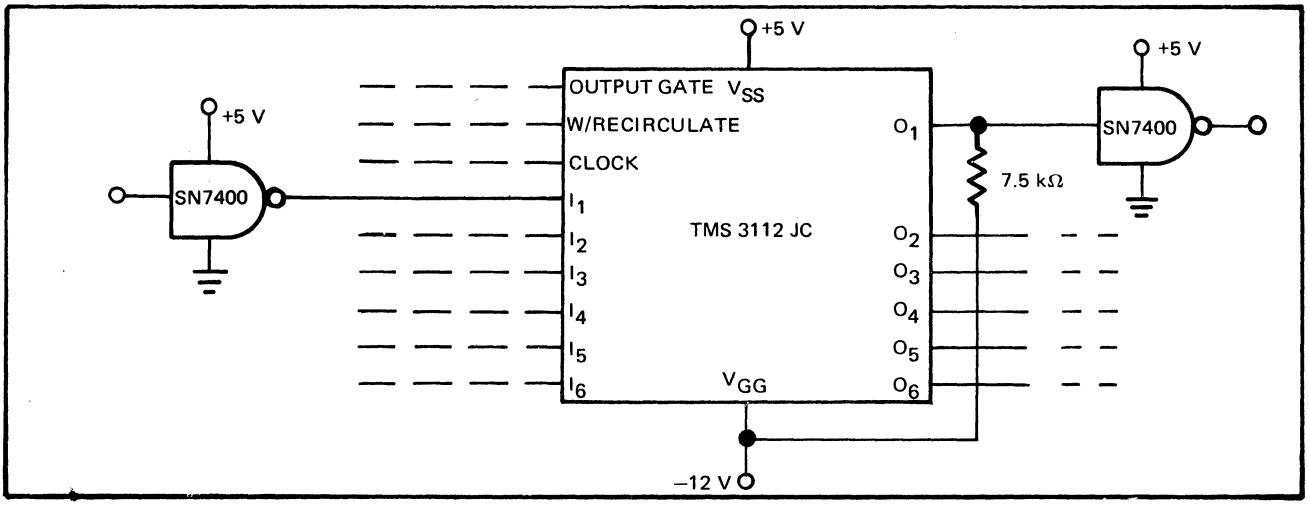


interface circuits

a) MOS



b) TTL



TMS3304LR-triple 66-bit dynamic shift register
TMS3305LR-triple 64-bit dynamic shift register

FEATURING

- 5-MHz operation
- TTL compatability
- Single ended open drain output buffers
- Low power dissipation

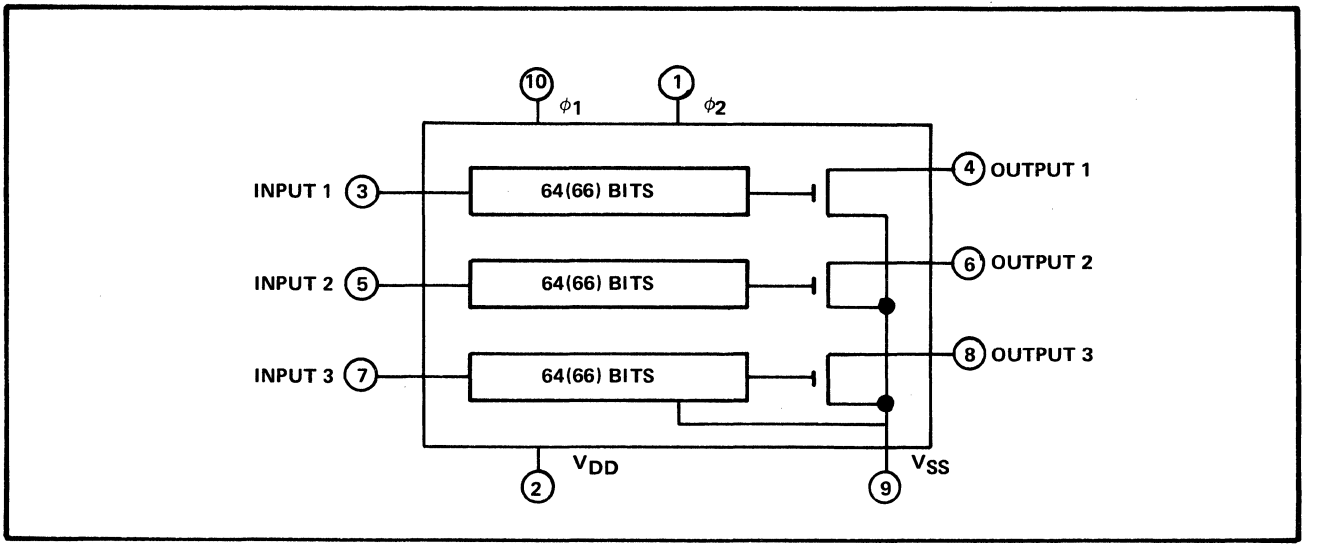
description

The TMS 3304 LR (TMS 3305 LR) consists of three separate 66(64) bit dynamic shift registers with independent input and output terminals and common clocks, power and ground. The gate capacitance of an MOS transistor is used for temporary storage of information between clock pulses. Each register has an unclocked single-ended output buffer to provide an output inverted from the input. The output level is determined by the external load resistor and load power supply.

operation

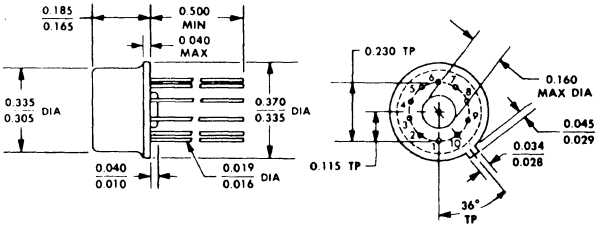
Transfer of data into the register is accomplished when the ϕ_1 clock is at a logic 1. Data shifting occurs when the ϕ_2 clock is momentarily pulsed to a logic 1, and the ϕ_1 clock to a logic 0. Output data appears on the negative going edge of the ϕ_2 clock pulse.

functional diagram

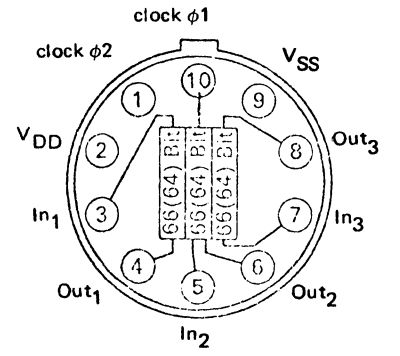


mechanical data and pin configuration

The package outline is the same as JEDEC TO-100 except for diameter of standoff.



DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED
ALL LEADS INSULATED FROM CASE



TOP VIEW

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to +0.3 V
Supply voltage V_0 range (See Note 1) . . . . . −30 V to +0.3 V
Clock and data input voltage range (See Note 1) . . . . . −30 V to +0.3 V
Power dissipation . . . . . 350 mW at T_A = 25°C
Operating free-air temperature range . . . . . −55°C to +85°C
Storage temperature range . . . . . −55°C to +150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions at T_A = 25°C

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−16	V
Supply voltage V_0	−5	−14	−29	V
Clock logic 0 voltage $V_\phi(0)$	0.3	0	−3	V
Clock logic 1 voltage $V_\phi(1)$	−20	−28	−29	V
Data logic 0 voltage V in (0)	0.3	0	−3	V
Data logic 1 voltage V in (1)	−8	−14	−29	V
Clock Overlap voltage (see figure)			−3	V
Clock pulse width, t_p $V_{\phi1}$ = −24 V V_{DD} = −12 V	0.1		50	μs
Clock pulse width, t_p V_ϕ = −28 V, V_{DD} = −14 V	0.08		50	μs
Data pulse width PW	0.15			μs

– CONTINUED –

recommended operating conditions at T_A = 25°C (continued)

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Clock delay time, t_d (See Voltage Waveforms)			200	μs
Clock rise and fall times, t_r, t_f (See Voltage Waveforms			5	μs
Clock repetition rate†	0.002	2	5	MHz
Data lead time, t_b (See Voltage Waveforms)	0.08			μs
Data delay time, t_a (See Voltage Waveforms)	0.01			μs

† V_{DD} = −14 V, $V_{\phi(1)}$ = −28 V, normal or extended with TTL output interface.

Nominal values of power supply and clock swing will result in maximum speed of operation. The device has been designed to operate over a broad range that allows the user to take advantage of readily available power supplies (e.g. +12 V, 0 V, −12 V).

electrical characteristics at 25°C and nominal operating conditions unless otherwise noted

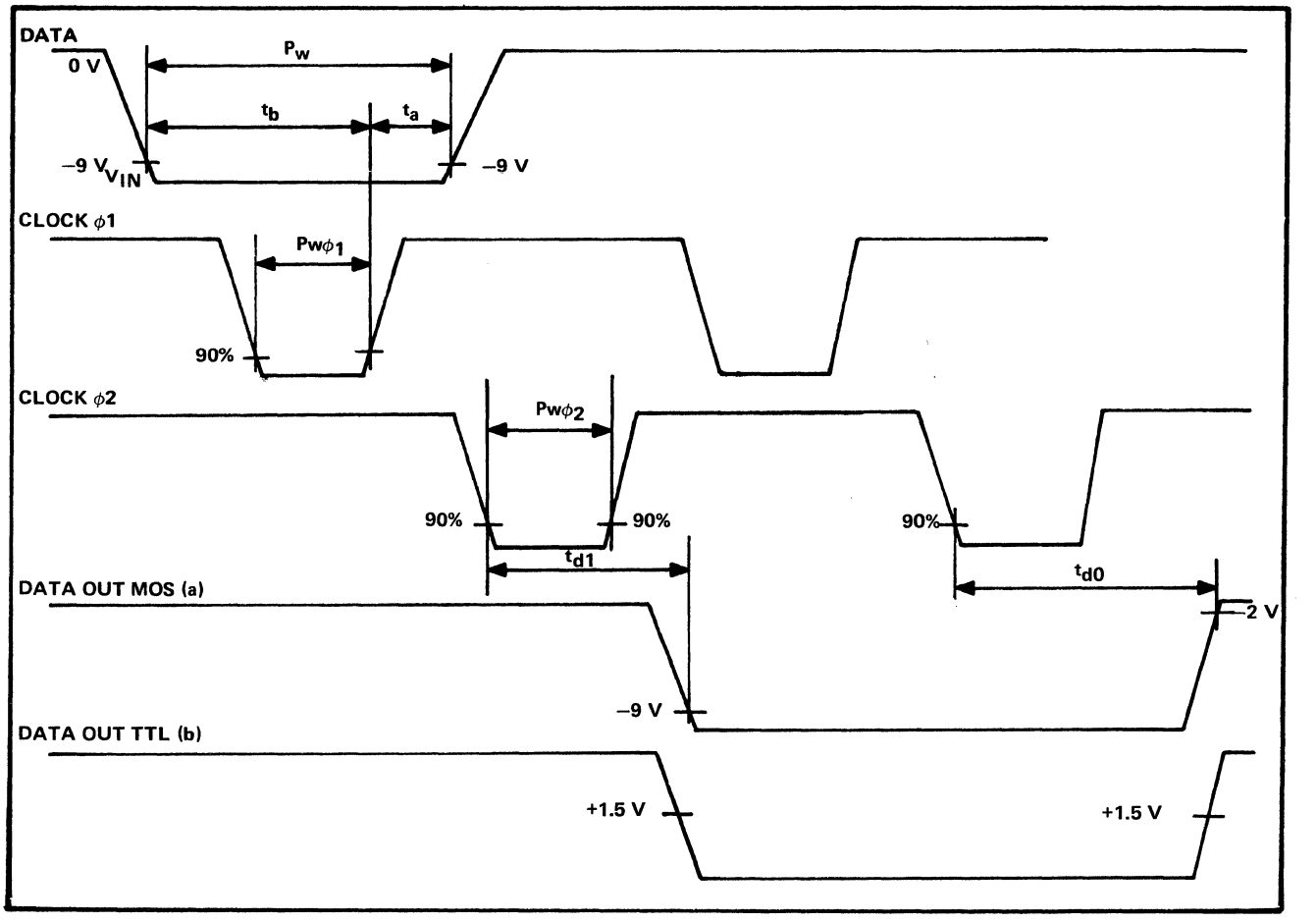
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{out}	Output voltage level logic 0 (V_ϕ between −20 V and −30 V)	V_0 = −14 V,	R_L = 10 kΩ		−0.8	−1.2	V
$V_{(1)}$	Output voltage level logic 1 (See Note 1)	V_0 = −14 V,	R_L = 10 kΩ	−9.0			V
$I_{out(1)}$	Output current logic 1	V_{out} = −14 V,	V_ϕ = −28 V	8	12		mA
		V_{out} = −12 V,	V_ϕ = −24 V	5	10		mA
I_{dd}	Power supply current drain	V_{DD} = −14 V, 20% clock duty cycle	V_ϕ = −28 V		6	12	mA
		V_{DD} = −12 V, 20% clock duty cycle	V_ϕ = −26 V		5	10	mA
$I_{\phi L}$	Clock leakage current	$V_{in\phi}$ = −28 V				10	μA
I_{in}	Input leakage current	V_{in} = −28 V				0.5	μA
	Power dissipation				100	350	mW

NOTE 1. For an output logic 1 the single ended MOS buffer transistor is "off" and the output voltage is equal to this output voltage power supply V_0.

dynamic electrical characteristics

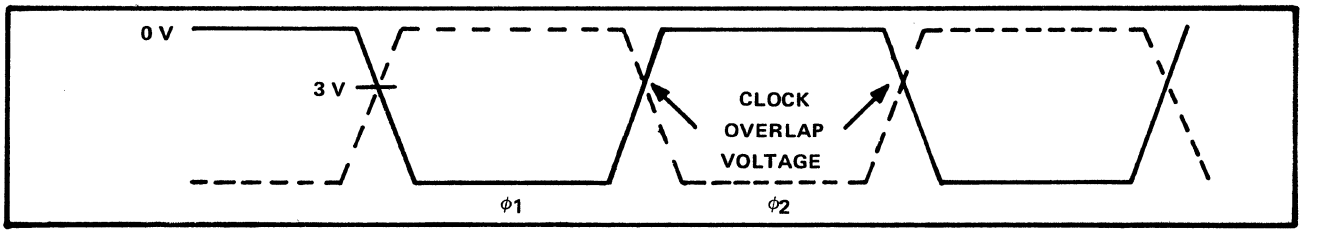
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{d0}	Output logic delay MOS interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		60	150	ns
t_{d1}	Output logic delay MOS interface (See voltage waveforms	R_L = 10 kΩ, C_L = 20 pF		120	250	ns
t_{d0}	Output logic delay TTL interface (See voltage waveforms)	R_L = 5.6 kΩ, C_L = 20 pF		50	100	ns
t_{d1}	Output logic delay TTL interface (See voltage waveforms)	R_L = 5.6 kΩ, C_L = 20 pF		60	120	ns
C_i	Data input capacitance	V_i = 0 V		5		pF
C_ϕ	Clock input capacitance	V_ϕ = 0 V		45		pF

voltage waveforms

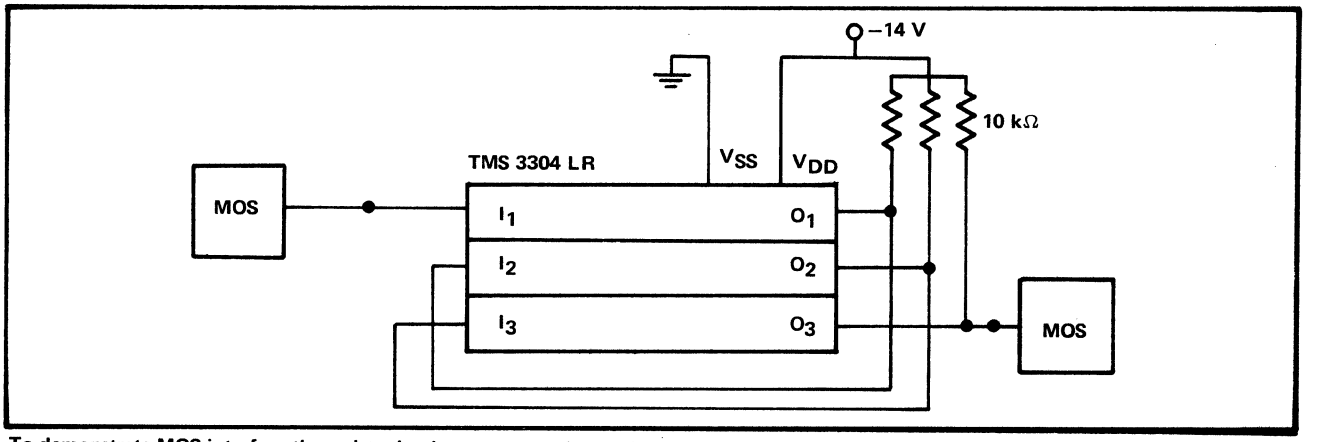


voltage waveforms (continued)

clock overlap voltage

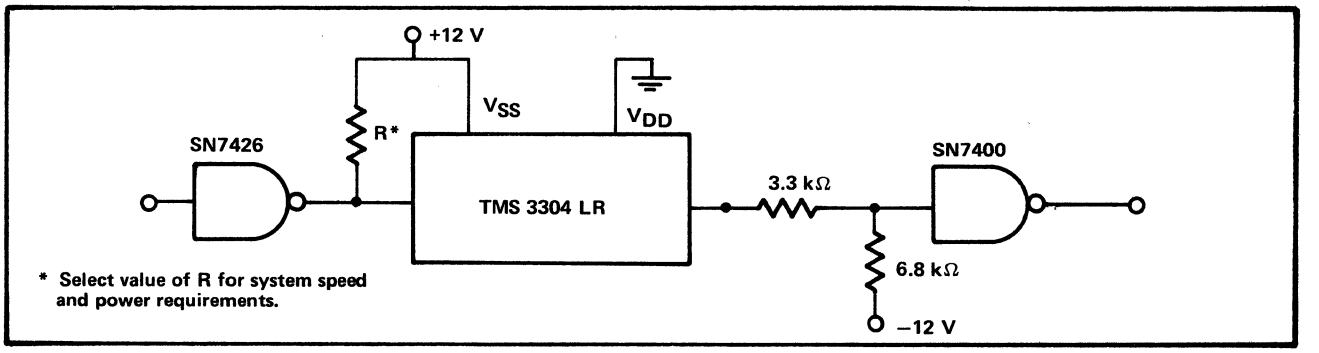


MOS interface



To demonstrate MOS interface the register has been connected as a 198-bit shift register.

TTL interface



TMS3309JC
twin 512-bit dynamic shift register/accumulator

preliminary information

FEATURING

- Two independent registers/accumulators
- 10-MHz guaranteed operating frequency
- Low power dissipation (typical 90 μW/bit at 1 MHz)
- TTL/DTL compatible
- Recirculate logic on the chip

description

The TMS 3309 JC is a twin 512-bit 4-phase dynamic shift register/accumulator, constructed on a monolithic chip, using thick-oxide P-channel enhancement mode transistors. The device contains two separate register/accumulators with independent control logic for recirculating information, and separate clock lines. The register/accumulators operate at pulse repetition rates from 10 kHz to 5 MHz. A 10-MHz speed of operation is obtained by multiplexing the two registers. Power dissipation is less than 90 μW/bit at 1 MHz.

logic definition

a) LOGIC 1 = most negative voltage

b) LOGIC 0 = most positive voltage

operation

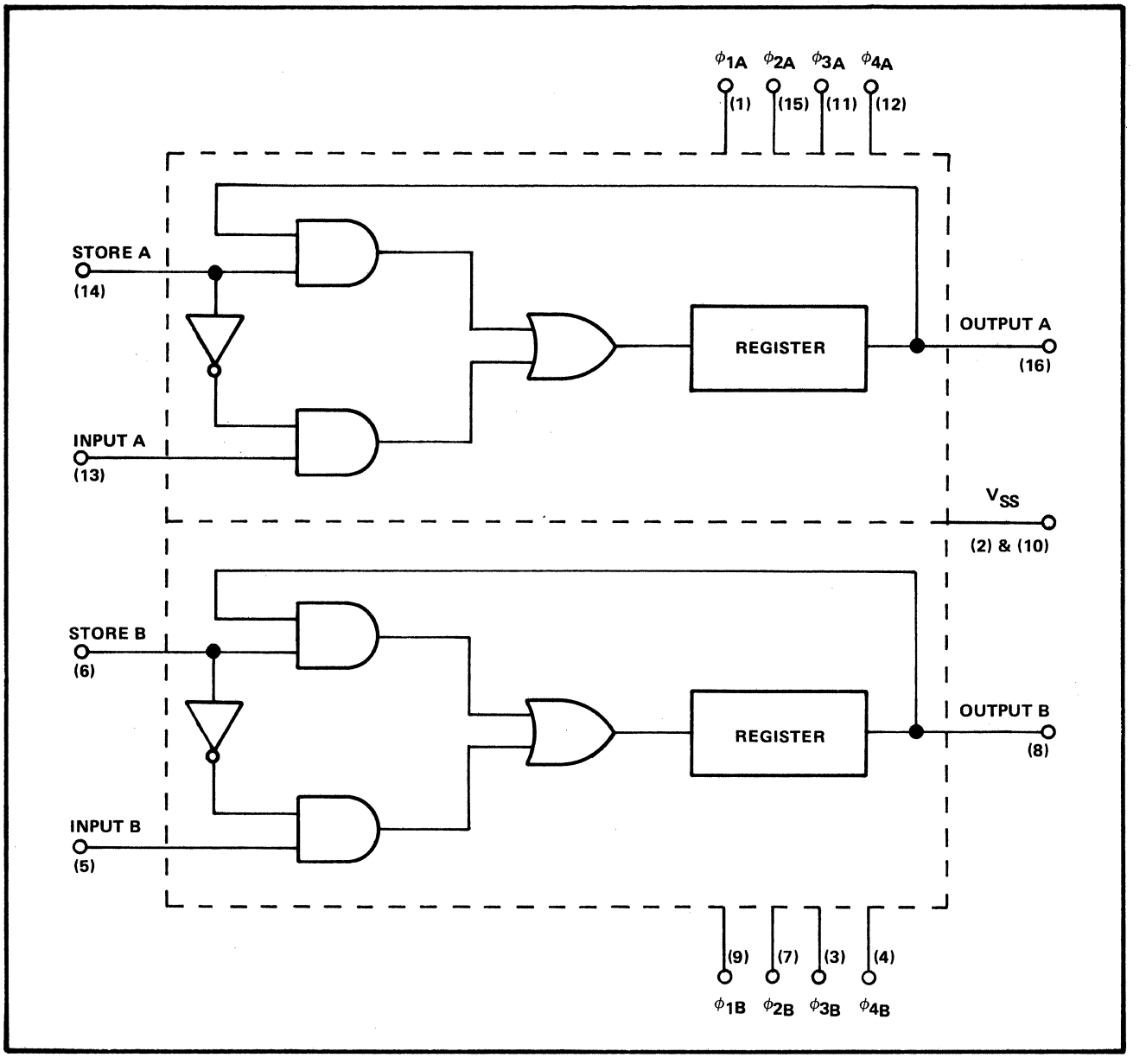
Four clocks are required for operation of the register/accumulators. Input data is transferred into the register after the end of clock pulse ϕ_1 and before the end of clock pulse ϕ_2. True output data appears after the end of clock pulse ϕ_4 and before the start of the next ϕ_4 clock pulse. Recirculate control is functional when the store pulse overlaps the trailing edge of clock pulse ϕ_3.

twin 512-bit dynamic shift register/accumulator

operation (continued)

The registers may be connected in cascade without external components. The circuit will interface with TTL/DTL and other bipolar logic.

functional diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Clock input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to +85°C
Storage temperature range . . . . . −55°C to +150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

PARAMETERS	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Logic Levels					
Store and Input Logic 0 $V_{IN(0)}$		+0.3	0	−3.5	V
Store and Input Logic 1 $V_{IN(1)}$		−9	−12	−26	V
Clock Voltage Levels					
Clock Low Logic Level $V_{\phi(0)}$		0.3	0	−2	V
Clock High Logic Level $V_{\phi(1)}$		−22	−24	−26	V
Pulse Timing					
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$				10	μs
Clock pulse width 1 $PW_{\phi1}$	V_ϕ = −24 V	25			ns
Clock pulse width 2 $PW_{\phi2}$	V_ϕ = −24 V	75		25,000	ns
Clock pulse width 3 $PW_{\phi3}$	V_ϕ = −24 V	25			ns
Clock pulse width 4 $PW_{\phi4}$	V_ϕ = −24 V	75		25,000	ns
Store PW_S		50			ns
Pulse Spacing					
Clock delay $t_{D\phi23}$	V_ϕ = −24 V	0		25,000	ns
Clock delay $t_{D\phi41}$	V_ϕ = −24 V, C_L = 10 pF	0		25,000	ns
Data setup t_{DS}		10			ns
Data hold t_{DH}		10			ns
Clock to store/recirculate t_{DCS}		30			ns
Pulse Overlap (See Note 2)					
Clock–Clock $t_{D\phi12}$, $t_{D\phi34}$	V_ϕ = −24 V	60		10,000	ns
Pulse Repetition Rate (Note 3)					
Data PRR	V_ϕ = −24 V	0.01		5	MHz
Clock PRR	V_ϕ = −24 V	0.01		5	MHz

NOTES: 2. Only clock pulse pairs ϕ_1, ϕ_2 or pairs ϕ_3, ϕ_4 may be simultaneously more than 2 volts below V_{SS}.
3. The maximum operating frequency pertains to each shift register operated independently. If multiplexing is used, double the maximum operating frequency.

TMS3309JC

twin 512-bit dynamic shift register/accumulator

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_L	Input Current (Leakage)	$V_I = -20$ V			500	nA
Φ_L	Clock Current (Leakage)	$V_{IN} = -26$ V			100	μA
Output Voltage Levels						
$V_{OUT(0)}$	Output Level (0)	$V_{\phi(0)} = -1.5$ V, $V_{IN(0)} = -3.5$ V		1.5	2.5	V
$V_{OUT(1)}$	Output Level (1)	$V_{\phi(1)} = -22$ V, $V_{IN(1)} = -9$ V	−10	−16		V
Power Dissipation/Bit		PRF = 1 MHz, $V_\phi = -24$ V, $C_L = 10$ pF		90		μW
Output Logic Delay						
t_{DL}	Output Logical 1 Level				0	ns
t_{DH}	Output Logical 0 Level				20	ns
Capacitance (See Note 4)						
C_{IN}	Input	$V_\phi = 0$ V		5		pF
C_ϕ	Clock $C_{\phi1} = C_{\phi3}$	$V_\phi = 0$ V		90		pF
C_ϕ	Clock $C_{\phi2} = C_{\phi4}$	$V_\phi = 0$ V		40		pF

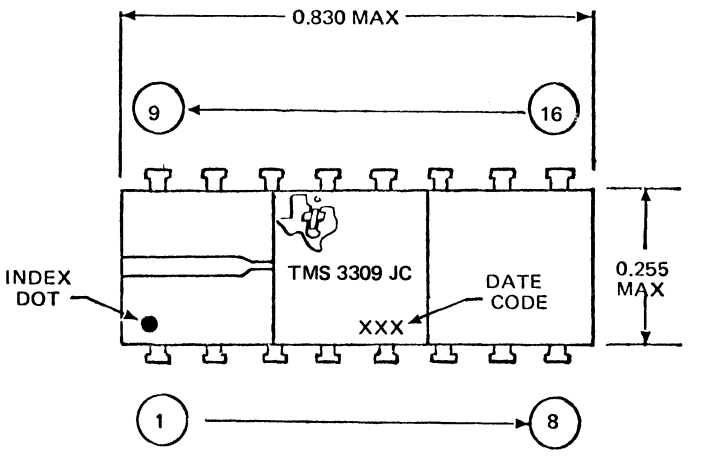
NOTE 4: The capacitance pertains to each register.

mechanical data

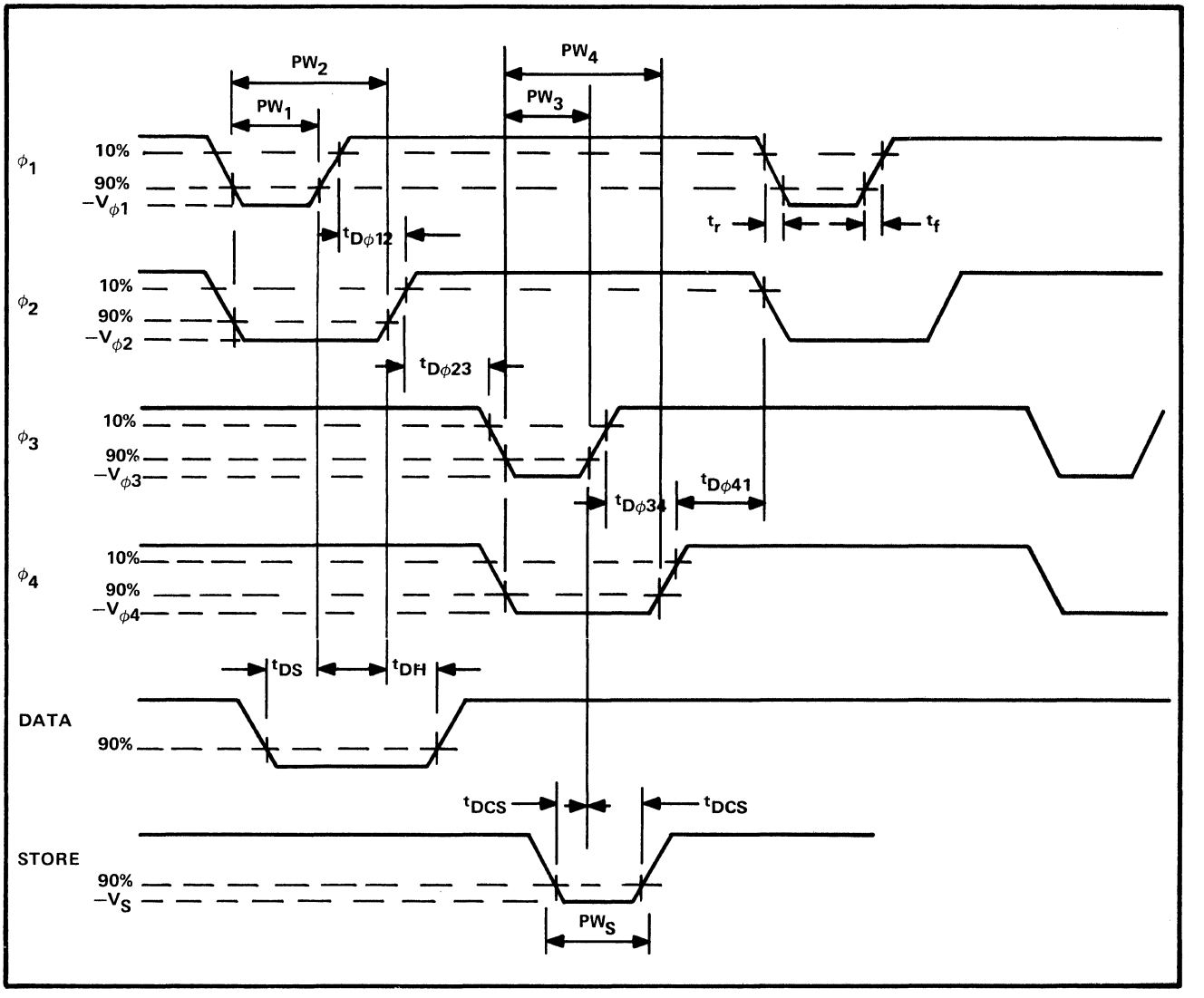
The TMS 3309 JC is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers.

PIN CONFIGURATION

PIN NO.	FUNCTION
1	Φ_1 (A)
2	V_{SS}
3	ϕ_3 B
4	ϕ_4 B
5	IN B
6	REC B
7	ϕ_2 B
8	OUT B
9	ϕ_1 B
10	V_{SS}
11	ϕ_3 A
12	ϕ_4 A
13	IN A
14	REC A
15	ϕ_2 A
16	OUT (A)



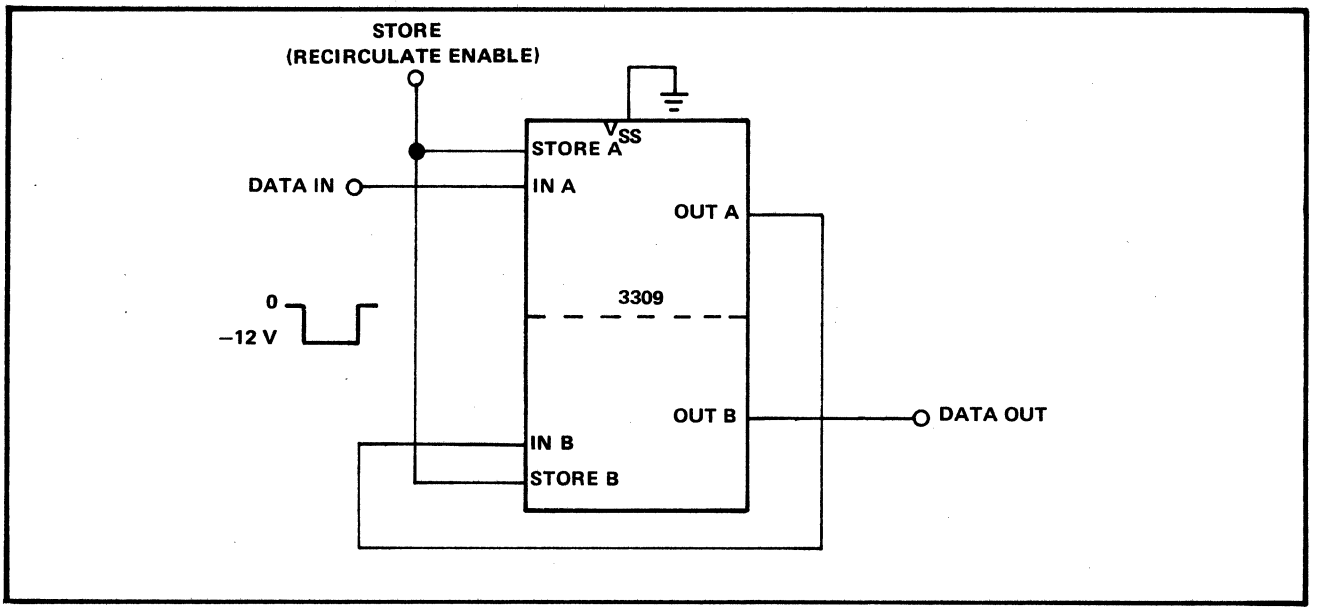
timing diagram and voltage waveforms



TMS3309JC
twin 512-bit dynamic shift register/accumulator

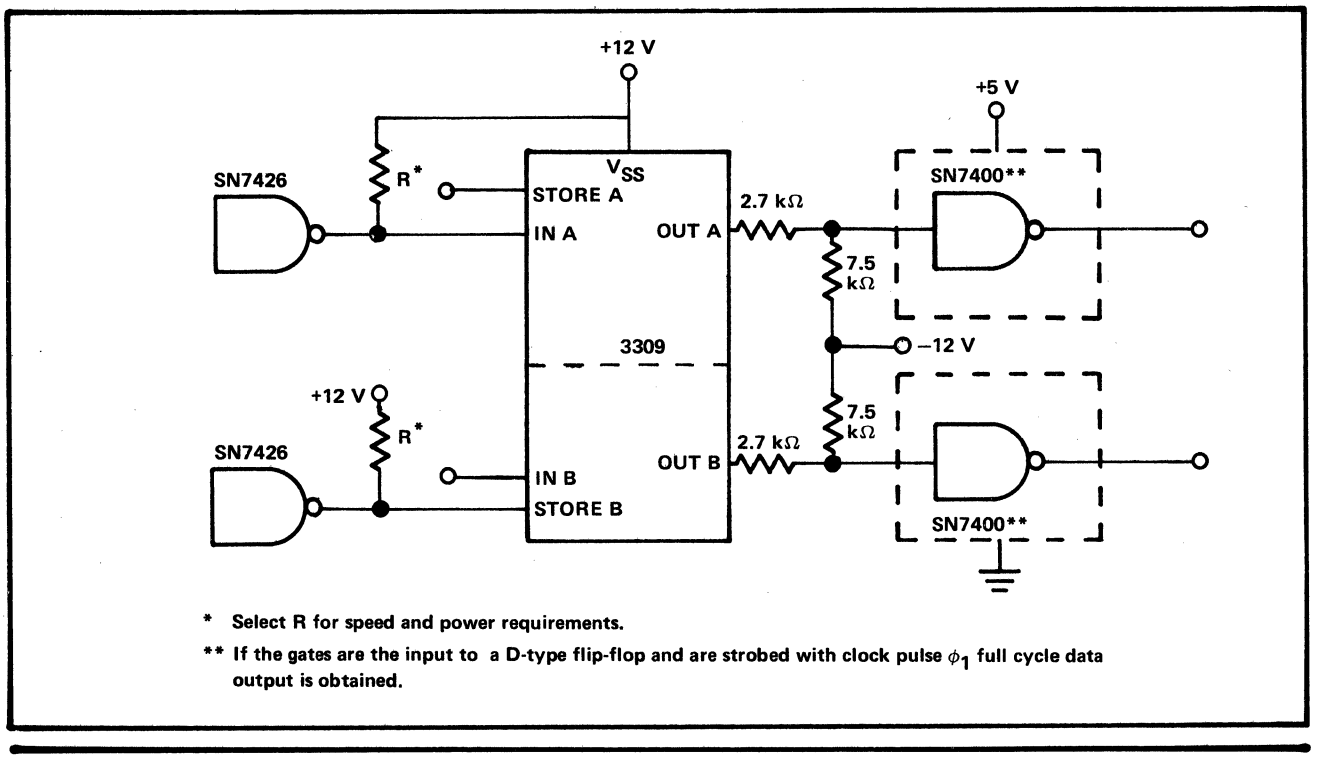
interface circuits

MOS interface



NOTE: In this figure the register has been connected as a 1024-bit shift register.

TTL interface

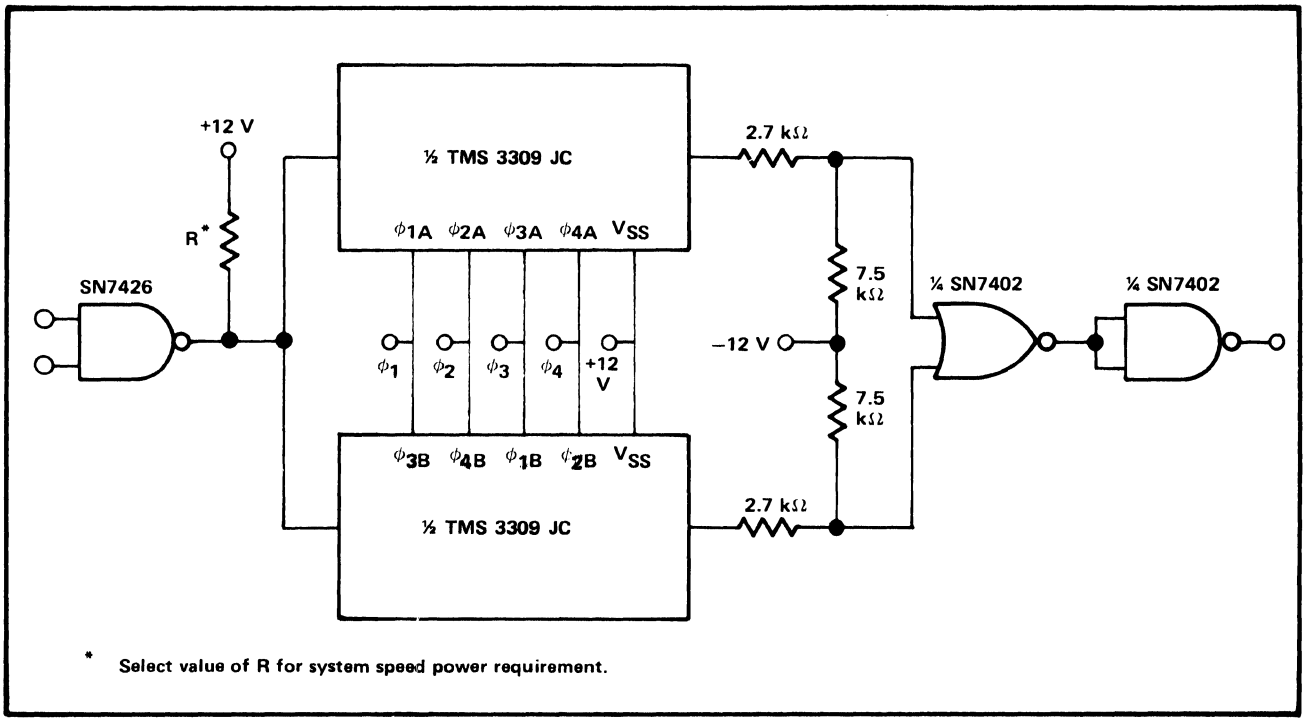


* Select R for speed and power requirements.

** If the gates are the input to a D-type flip-flop and are strobed with clock pulse ϕ_1 full cycle data output is obtained.

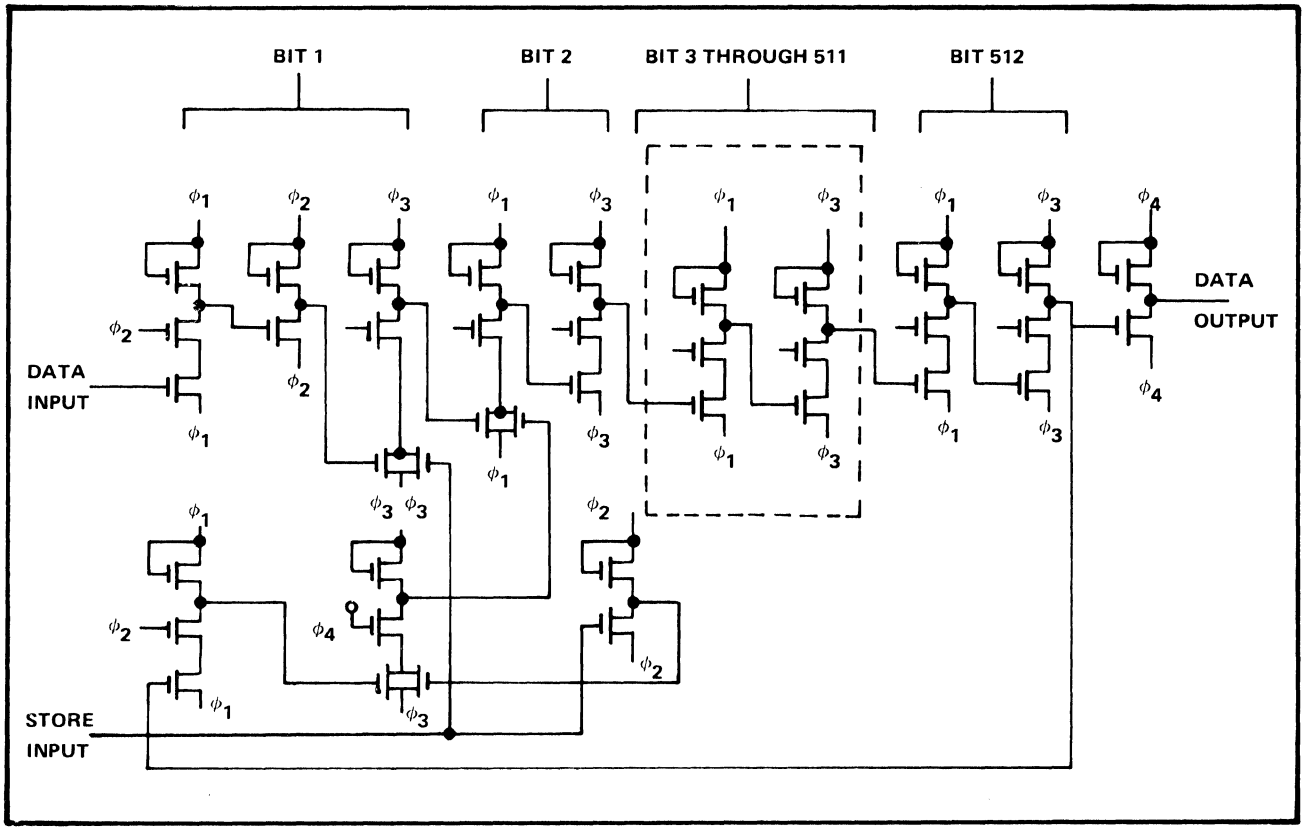
twin 512-bit dynamic shift register/accumulator

multiplexing of TMS 3309 JC, 10-MHz operation



* Select value of R for system speed power requirement.

circuit diagram



TMS3314JR
triple (60•4) dynamic shift register
preliminary information

FEATURING

- 2 MHz operation
- TTL compatible
- Open-drain output buffers
- Three 60-bit registers
- Three 4-bit registers

description

The TMS 3314 JR contains three separate 60-bit, and three separate 4-bit dynamic shift registers constructed on a single monolithic chip, using thick-oxide enhancement-mode P-channel MOS transistors.

Each register has independent input and output terminals and common clock and power lines. Each has an unclocked open-drain output buffer to provide an output inverted from the input. The inputs and outputs terminals of the registers are oriented for optimum printed-circuit-board layout.

The TMS 3314 JR is ideal for data handling applications in desk calculators, terminals, and peripheral equipment.

logic definition

Negative logic is assumed:

a) Logic 1 = most negative (LOW) voltage

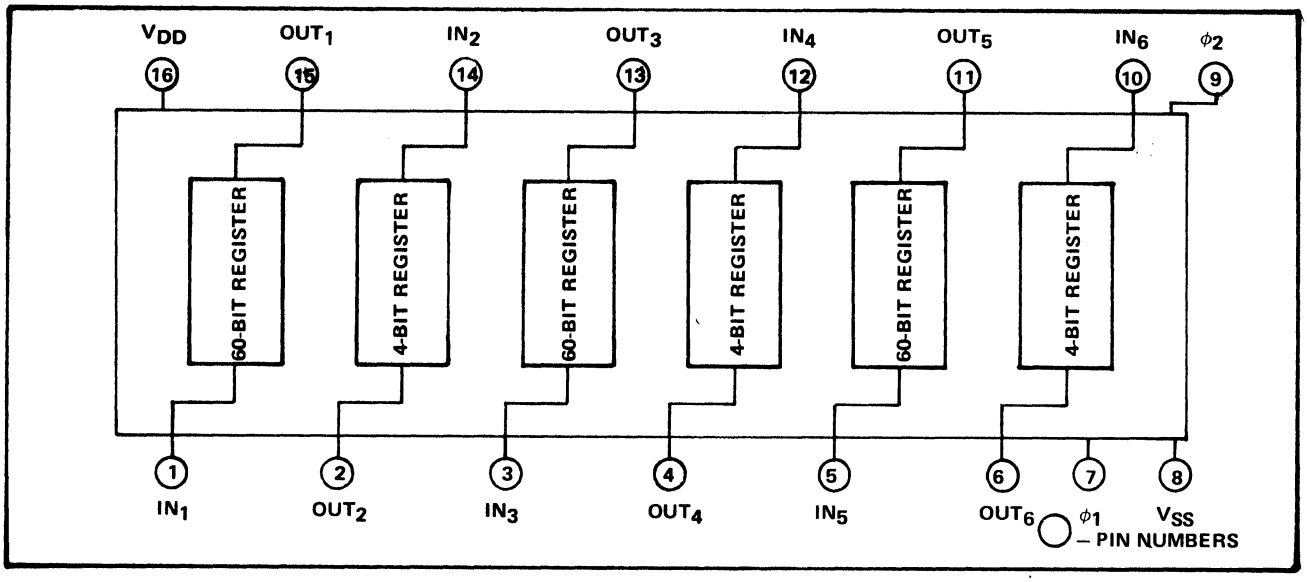
b) Logic 0 = most positive (HIGH) voltage

operation

Two clock pulses are required for operation of the registers. The pulses should not simultaneously be at Low levels, or data errors will occur. Data is transferred into the registers when clock pulse ϕ_1 is pulsed to a Low level. Data shift occurs when clock pulse ϕ_2 is pulsed to a Low level. Output data appears on the High-to-Low transition of clock pulse ϕ_2.

The registers can drive DTL/TTL gate loads by means of a pull-down resistor, connected between the output terminal and the V_{DD} supply.

functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −55°C to +85°C
Storage temperature range . . . . . −55°C to +150°C

NOTE 1. These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Drain supply V_{DD}	−11	−14	−16	V
Output supply V_O	−11	−14	−16	V
Logic Levels				
Input HIGH level (logic 0) V_{IH}	−3	0	+0.3	V
Input LOW level (logic 1) V_{IL}	−8	−14	−29.0	V
Clock Voltage Levels				
HIGH level (logic 0) $V_{\phi H}$	−3	0	+0.3	V
LOW level (logic 1) $V_{\phi L}$	−22	−28	−29.0	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5	μs
Clock pulse width 1 $PW_{\phi 1}$	0.22		10	μs
Clock pulse width 2 $PW_{\phi 2}$	0.22		10	μs

– CONTINUED –

recommended operating conditions (continued)

CHARACTERISTICS		MIN	NOM	MAX	UNITS
Pulse Spacing					
	Clock delay $t_{D\phi 12}$	0.01		100	μs
	Clock delay $t_{D\phi 21}$	0.01		100	μs
	Data setup t_{DS}	75			ns
	Data hold t_{DH}	75			ns
Clock Pulse Overlap (See Notes 2)			NOTE 2		ns
Pulse Repetition Rate (Note 3) PRR					
	Data	0.01		2	MHz
	Clock	0.01		2	MHz

NOTES: 2. The two clock pulses should not be simultaneously more than 3 V below V_{SS}.

3. R_L = 13 kΩ, C_L = 10 pF.

Maximum speed of operation will be obtained when operating at nominal conditions. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

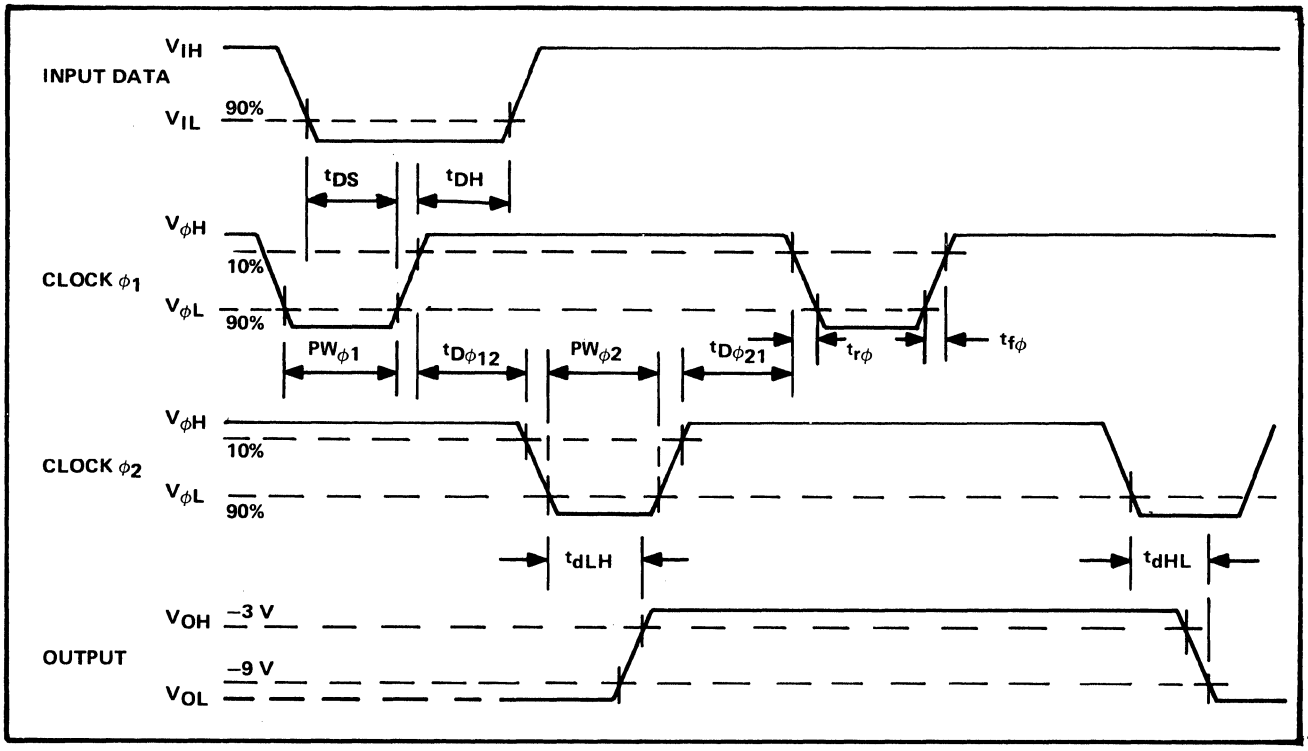
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current (Leakage)	V_I = −14 V			500	nA
$I_{\phi L}$	Clock Current (Leakage)	V_I = −29 V			100	μA
Output Voltage Levels						
V_{OL}	Output LOW level (logic 1)	R_L = 13 kΩ to V_{DD}, C_L = 10 pF	−9	−10		V
V_{OH}	Output HIGH level (logic 0)	R_L = 13 kΩ to V_{DD}, C_L = 10 pF			−3	V
Output Current						
I_O	Logic 0	−14 V applied to output			10	μA
I_O	Logic 1	−14 V applied to output	2			mA
Power Supply Current Drain						
I_{DD}	Drain supply	R_L = 13 kΩ to V_{DD}, $PW_{\phi 1} = PW_{\phi 2}$ = 200 ns, PRF = 2 MHz		15	20	mA
P_D	Power Dissipation			210	280	mW
Output Logic Delay						
t_{dLH}	Output Low level (logic 1)	R_L = 13 kΩ, C_L = 10 pF, V_ϕ = −25 V		80	150	ns
t_{dHL}	Output High level (logic 0)	R_L = 13 kΩ, C_L = 10 pF, V_ϕ = −25 V		225	300	ns
Capacitance						
C_{IN}	Input	V_ϕ = 0 V; f = 1 MHz		3	5	pF
C_ϕ	Clock	V_ϕ = 0 V, f = 1 MHz		55	65	pF

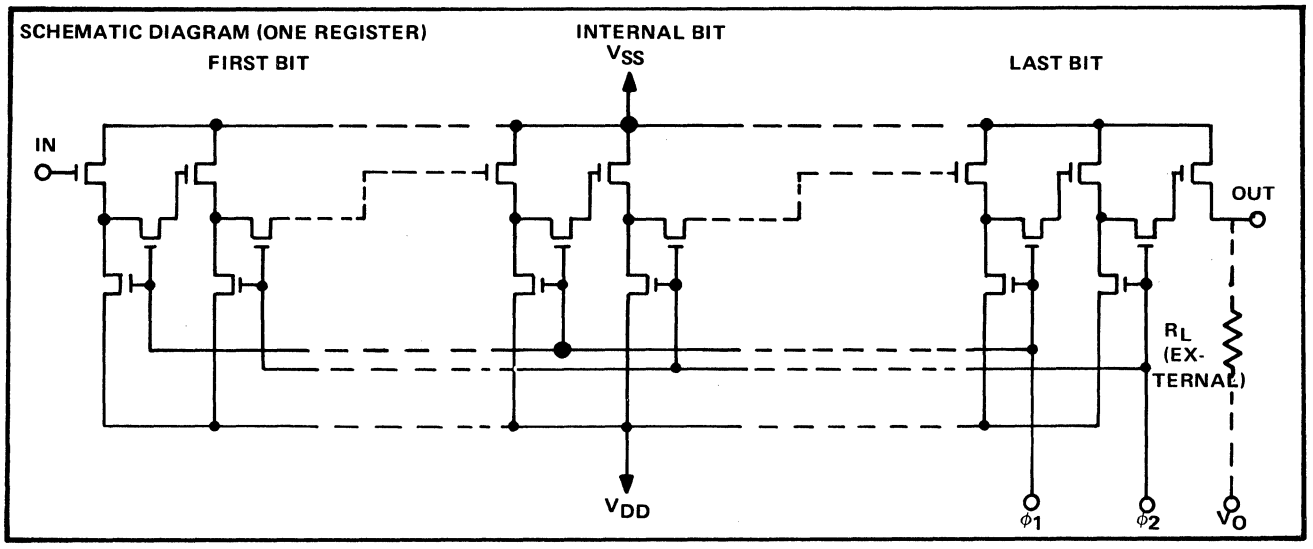
mechanical data

The TMS 3314 JR is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers.

timing diagram and voltage waveforms



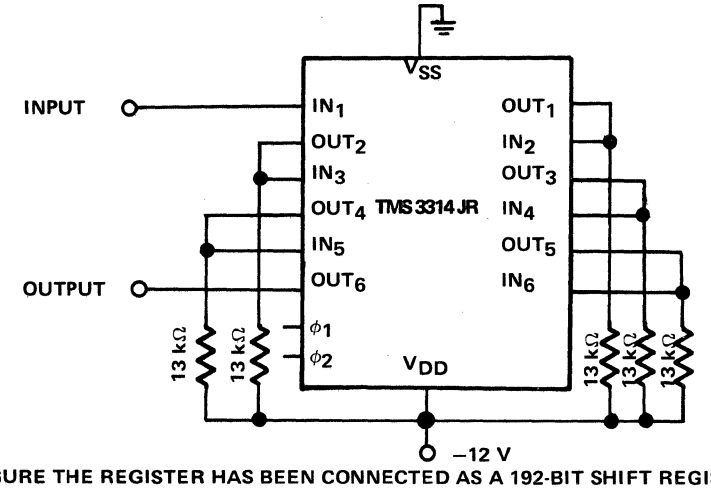
circuit diagram



TMS3314JR
triple (60-4) dynamic shift register

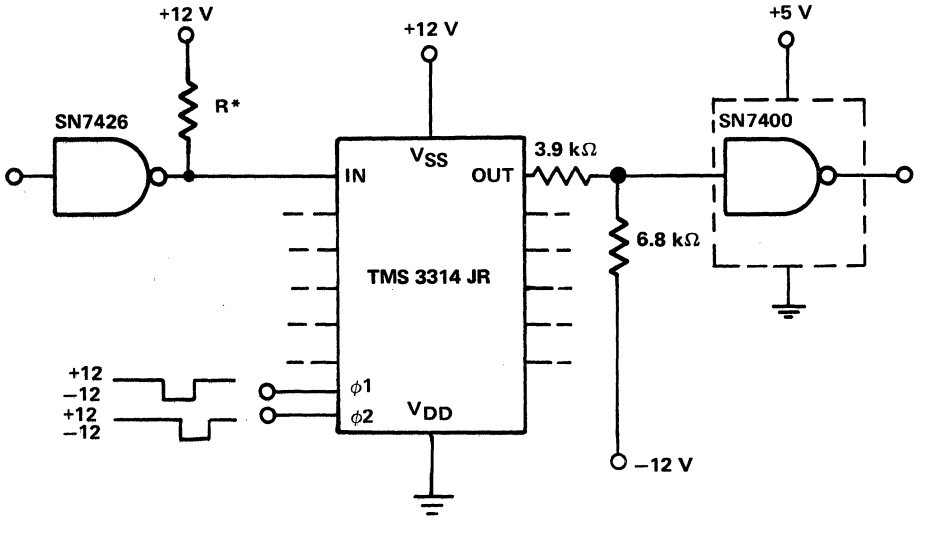
typical interface circuits

a) MOS interface



NOTE: IN THIS FIGURE THE REGISTER HAS BEEN CONNECTED AS A 192-BIT SHIFT REGISTER TO DEMONSTRATE MOS INTERFACE.

b) TTL interface



* SELECT R FOR SYSTEM REQUIREMENTS OF SPEED AND POWER DISSIPATION.

TMS3401LC
512 bit dynamic shift register
preliminary information

FEATURING

- Two-phase dynamic logic
- 5-MHz operation
- Directly TTL compatible at input and output
- No external resistors required
- Low power dissipation 0.2 mW/bit 1 MHz
- Output delay – 50 ns
- Low threshold technology
- Power supplies – +5 V, –12 V
- Push-pull output buffer

description

The TMS 3401 LC is a high-speed dynamic shift register with a maximum capacity of 512-bits. The bits are implemented by a ratioless two-phase design to minimize power consumption.

Because both input and output are TTL compatible without the use of external resistors, these registers can be strung together directly.

The entire device is constructed using MOS P-channel thick-oxide and low-threshold technologies to implement low-threshold MOS devices. The length of the device may be altered through single-level programming for a nominal charge.

logic definition

a) Logic 1 = most positive (HIGH) voltage

b) Logic 0 = most negative (LOW) voltage

operation

Data is transferred into the register when the ϕ_1 clock is Low (–12 V). The data must be held steady for at least 30 nanoseconds before the clock goes to the High state (+5 V). One of two internal resistors (1.5 kΩ or 6 kΩ) can be connected to assist in pulling up the logic 1 level provided by DTL or TTL.

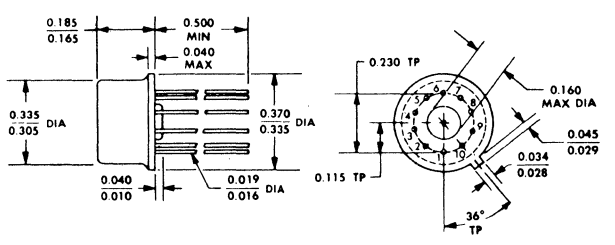
Output delay time is defined as the time required for the output to reach the DTL or TTL change-over threshold after the ϕ_2 clock reaches 90% of its Low voltage. This time is faster than 50 nanoseconds.

TMS3401LC
512 bit dynamic shift register

programming

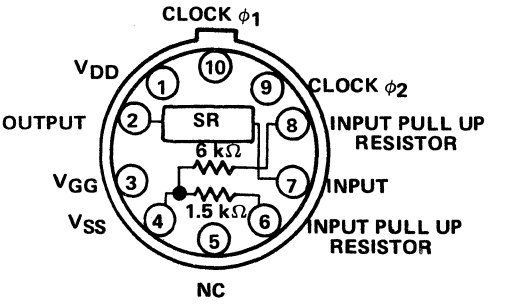
The TMS 3401 LC has been designed such that by changing only one level of artwork the designer can obtain any bit length between 233 and 512 bits. The TMS 3401 LC is a 512-bit shift register. Other bit lengths are obtained through use of computer-aided design methods, providing fast, accurate and economical turnaround. The electrical characteristics and pin configuration are the same for the whole family of devices.

functional diagram and pin configuration



DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE



TOP VIEW

NC – NO INTERNAL CONNECTION

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−20 V to 0.3 V
Data input voltage range (See Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to +85°C
Storage temperature range	−55°C to +150°C
Input pull-up resistor voltage range	−6 V to 0.3 V

NOTE 1. These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.5	+5	+5.5	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input HIGH level V_{IH}	+3.5		+5.5	V
Input LOW level V_{IL}	−13		+0.8	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$ (See Note 2)	4		5.25	V
Clock LOW level $V_{\phi L}$	−14	−12	−11	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			1	μs
Clock pulse width 1 (5 MHz) $PW_{\phi 1}$	0.075		10	μs
Clock pulse width 2 (5 MHz) $PW_{\phi 2}$	0.075		10	μs
Pulse Spacing				
Clock delay $t_{d\phi 12}$			50	μs
Clock delay $t_{d\phi 21}$			50	μs
Data setup t_{DS}	50			ns
Data hold t_{DH}	10			ns
Pulse Repetition Rate PRR				
Data	0.02		5	MHz
Clock	0.02		5	MHz

NOTE 2: Both clock pulses should not be simultaneously more than 2 V below V_{SS}.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input current (leakage)	V_I = 0 V, V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current (leakage)	V_ϕ = 0 V, V_{SS} = +5 V			50	μA
Output Voltage Levels						
V_{OL}	Output LOW level (Note 3)	TTL load, C_L = 10 pF, f = 5 MHz		+0.15	+0.4	V
V_{OH}	Output HIGH level (Note 3)	TTL load, C_L = 10 pF, f = 5 MHz	+3.6	+4.5		V
V_{OL}	Output LOW level (Note 3)	I_O = +1.6 mA		+0.15	+0.4	V
V_{OH}	Output HIGH level (Note 3)	I_O = −1 mA	+4.5	+4.7		V
Power Supply Current Drain						
I_{SS}	Substrate supply (Note 4)	f = 5 MHz		3.5	7	mA
I_{DD}	Drain supply (Note 5)				0.1	mA
I_{GG}	Gate supply (Note 4)			3.5	7	mA
P_D	Power dissipation			350		mW

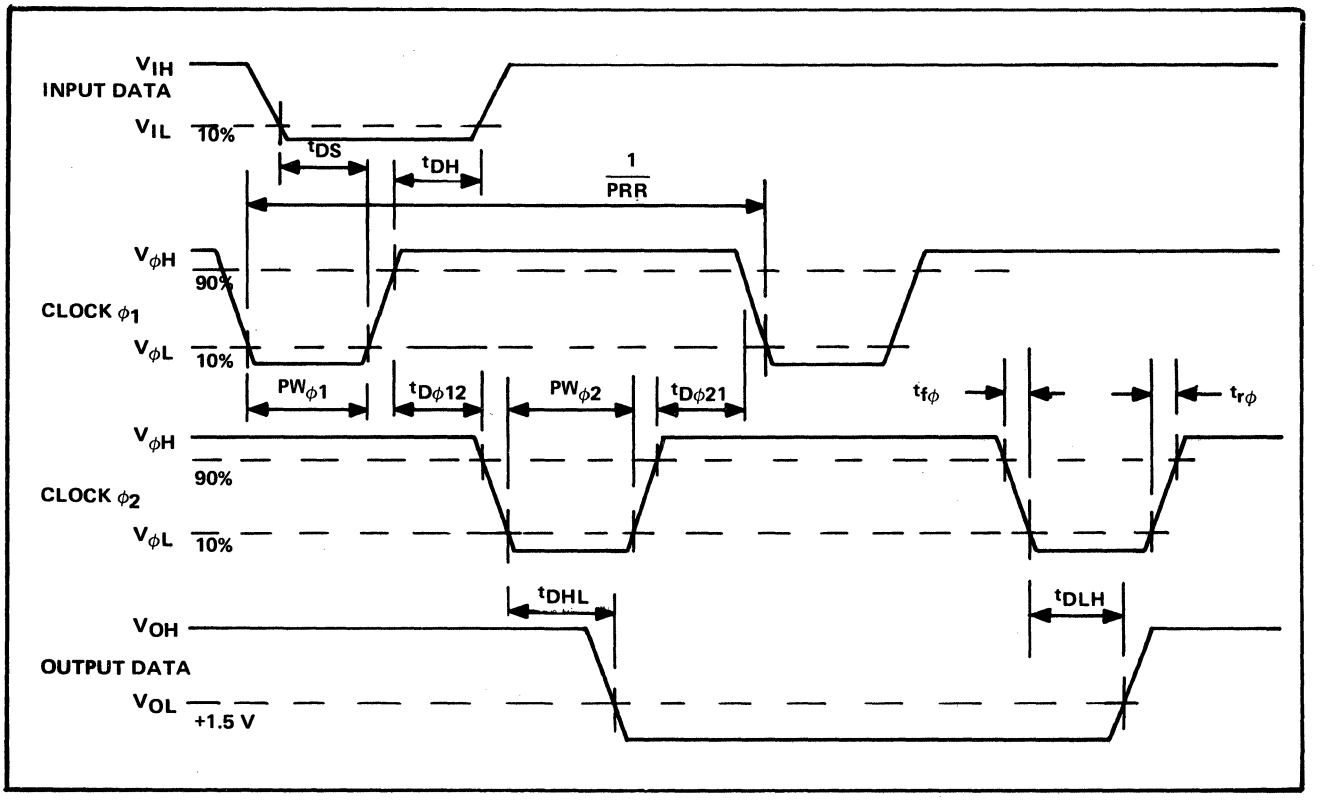
NOTES: 3. For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.
4. The device uses saturated logic. The current sourced by the 5 V power supply is sunk by the −12 V power supply.
5. Does not include output stage load or transient current. In the MOS load mode, the current will consist of transients due to capacitor discharge and/or leakage current.

TMS3401LC
512 bit dynamic shift register

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Delay						
t_{DLH}	Output LOW level	TTL load, C_L = 10 pF, f = 5 MHz		10	50	ns
		R_L = 10 MΩ, C_L = 10 pF, f = 5 MHz		15	50	ns
t_{DHL}	Output HIGH level	TTL load, C_L = 10 pF, f = 5 MHz		11	50	ns
		R_L = 10 MΩ, C_L = 10 pF, f = 5 MHz		4	30	ns
Capacitance						
C_{IN}	Input	$V_I = V_{SS}$, f = 1 MHz		5	7	pF
C_ϕ	Clock	$V_\phi = V_{SS}$, f = 1 MHz		220	280	pF

timing diagram and voltage waveforms

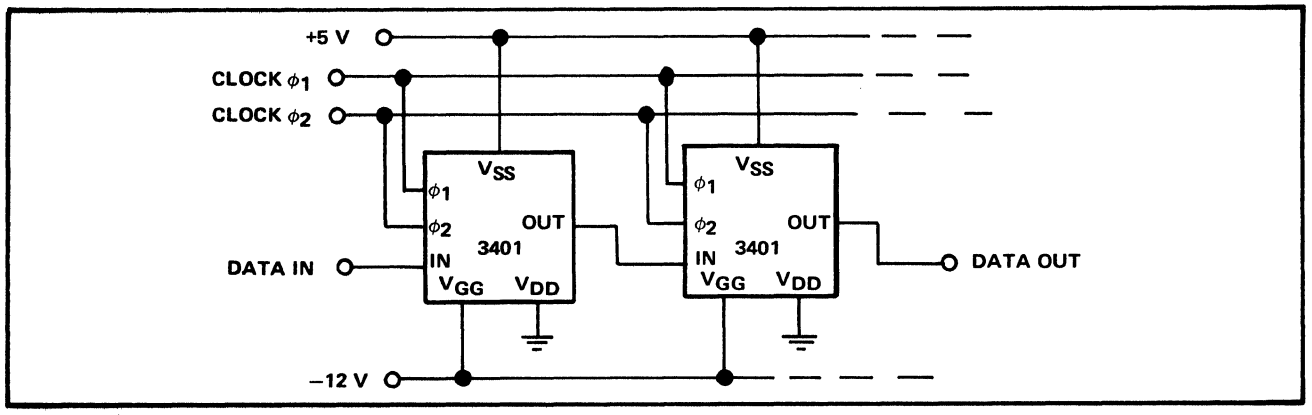


mechanical data

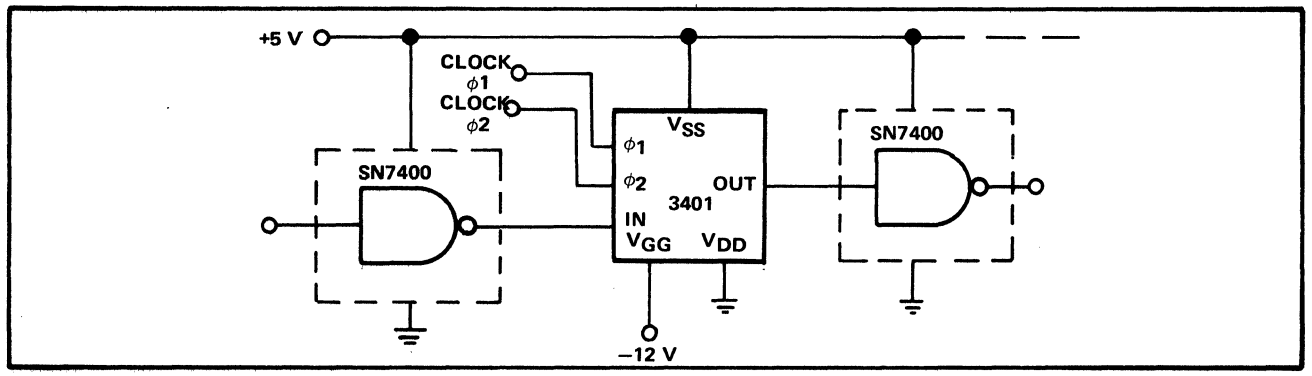
The TMS 3401 LC package outline is same as JEDEC TO-100 except for diameter of standoff.

interface circuits

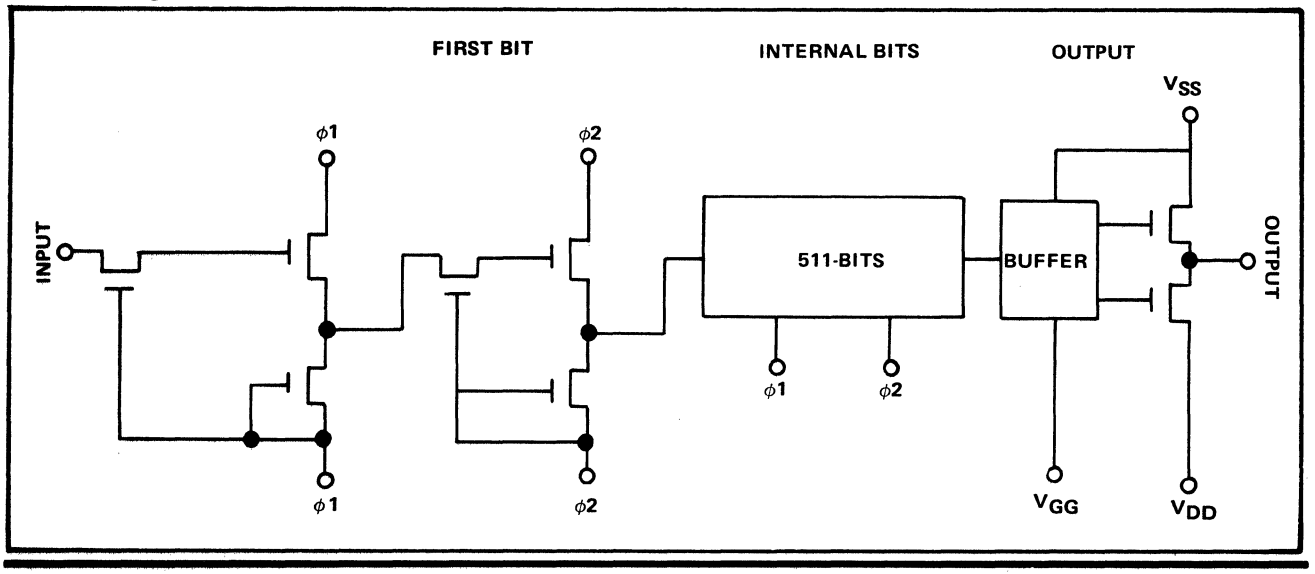
a) MOS



b) TTL



internal diagram



TMS3406LR
dual 100-bit dynamic shift register
preliminary information

FEATURING

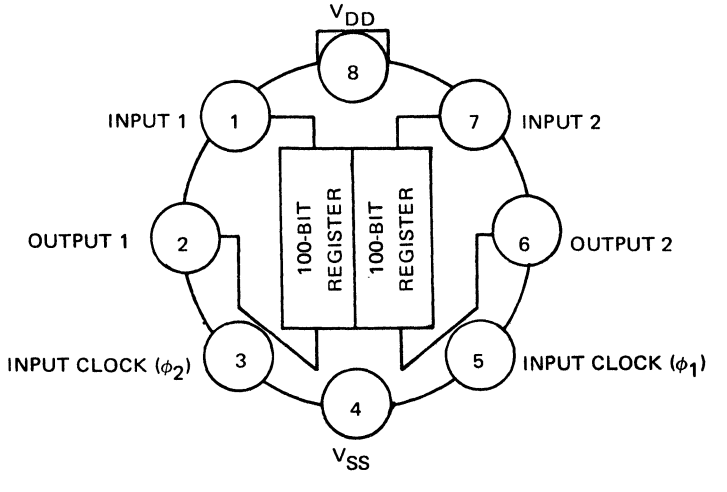
- Low power dissipation – 0.4 mW/bit typical at 1 MHz
  – 1 mW/bit typical at 2 MHz
- High frequency operation – 2.5 MHz guaranteed
- TTL/DTL compatible
- Single-ended output buffer
- Low threshold technology

description

The Texas Instruments TMS 3406 LR consists of two separate 100-bit dynamic shift registers with independent input and output terminals. Only one power supply and two clock phases are required for operation. Low-threshold, thick-oxide, MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMS 3406 LR and Bipolar integrated circuits.

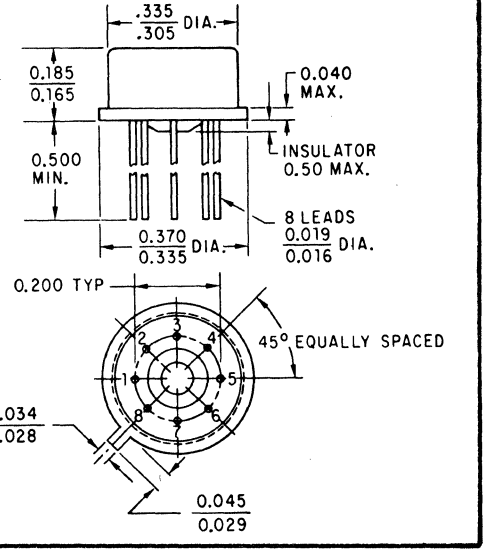
mechanical data and pin configuration

PIN CONFIGURATION



Top View

PACKAGE OUTLINE



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Clock voltage V_{ϕ} (See Note 1) . . . . . −20 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −20 V to 0.3 V
Power dissipation (See Note 1) . . . . . 600 mW
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions (−55°C to 85°C)

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD} (See Note 1)	−9	−10	−12	V
Clock voltage $V_{\phi L}$ (See Note 1) logic 0	−15	−16	−18	V
Clock voltage $V_{\phi H}$ (See Note 1) logic 1	+0.3	−0.5	−1.5	V
Width of clock pulse t_{p1} (See voltage waveforms)	150			ns
Width of clock pulse t_{p2} (See voltage waveforms)	150			ns
Transient time of clock pulse, t_r, t_f (See voltage waveforms)			5	μs
Clock delay time, t_d (See voltage waveforms)	20			ns
Width of data pulse, t_p (See voltage waveforms)	170			ns
Data pulse before clock change t_{p0} (See voltage waveforms)	150			ns
Clock repetition rate	0.01		2.5	MHz

NOTE 1. These are voltage values with respect to most positive supply voltage, V_{SS}.

logic definition

Positive logic is assumed

Logic 1 = most positive (high) voltage

Logic 0 = most negative (low) voltage

electrical characteristics (at nominal operating conditions and 25°C)

$V_{DD} = -5$ V, $V_{SS} = +5$ V, $V_{\phi H} = -11$ V, $V_{\phi L} = +5$ V, and $C_L = 10$ pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{in(1)}$	Logic 1 data input voltage		+3.0	+5	+5.3	V
$V_{in(0)}$	Logic 0 data input voltage		−10	+0.2	+0.8	V
$V_{out(1)}$	Logic 1 output voltage	Load = 3.3 kΩ, t_{p1} = 150 ns	+3.5			V
$V_{out(0)}$	Logic 0 output voltage	Load = 3.3 kΩ			−3.0	V
		Load = 3.3 kΩ, I_L = 1.6 mA			+0.4	V
R_{out}	Output resistance	Output at logic 0		300	450	Ω
$I_{R(in)}$	Input leakage current	$V_{in} = -5$ V, T_A = 25°C			0.5	μA
C_{in}	Capacitance of input	$V_{in} = +5$ V, T_A = 25°C, f = 1 MHz		5	7	pF
$C_{\phi 1,2}$	Capacitance of clock input	$V_\phi = +5$ V, T_A = 25°C, f = 1 MHz		40	50	pF
$I_{DD(1)}$	Average supply current (See Note 2)	f = 1 MHz (t_{p1} = 200 ns, t_{p2} = 200 ns)		6	16	mA
		f = 1 MHz (t_{p1} = 150 ns, t_{p2} = 150 ns)			12	mA
$I_{\phi 1,2}$	Average supply current for clock mode	f = 1 MHz ($t_{p1} = t_{p2}$ = 200 ns)			1.5	mA
		f = 1 MHz ($t_{p1} = t_{p2}$ = 150 ns)			1.2	mA

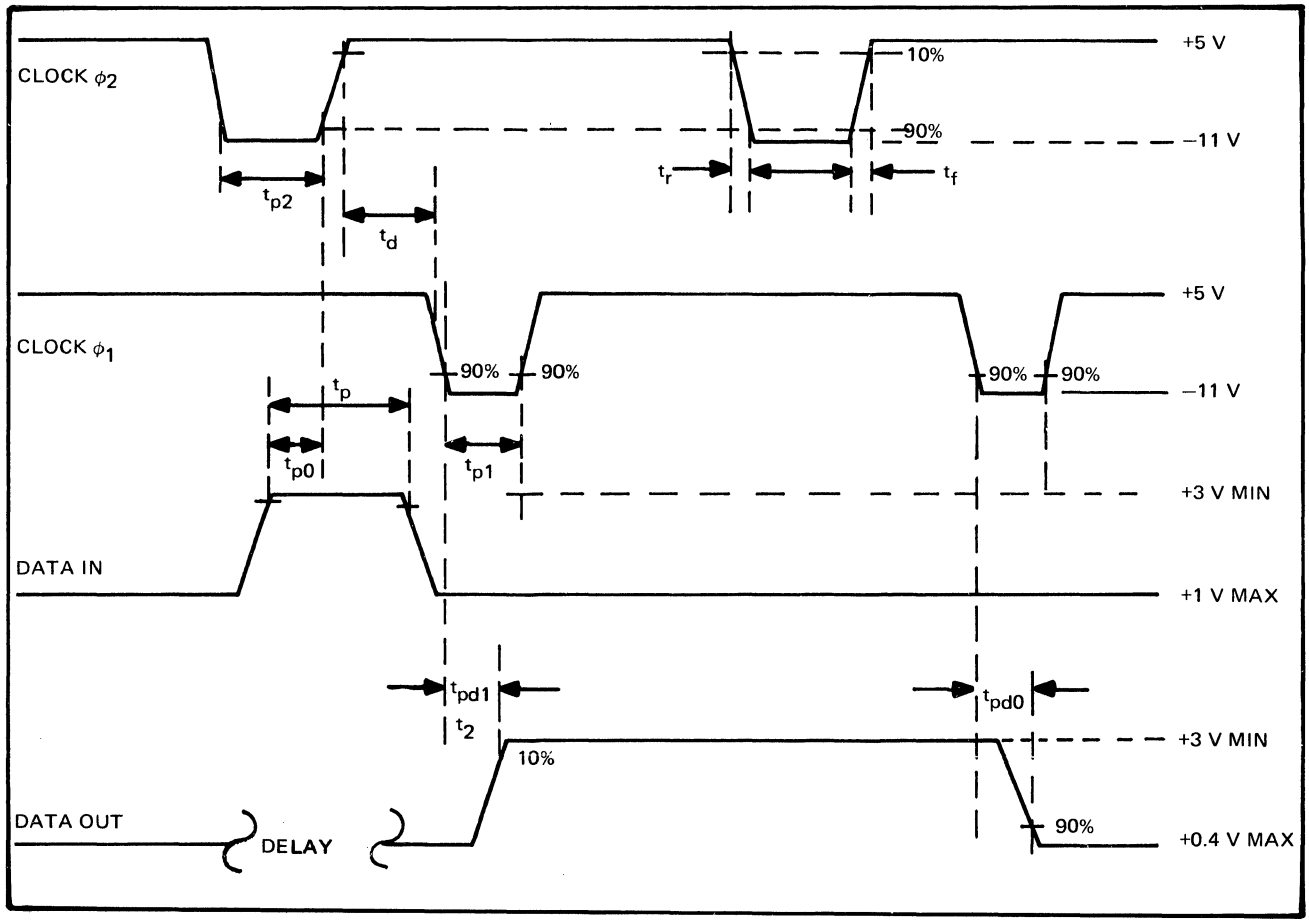
NOTE 2: These values do not include the current flowing through the load resistor.

switching characteristics

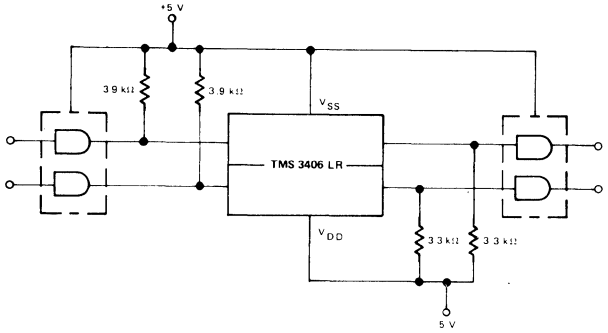
$V_{DD} = -5$ V, $V_{SS} = +5$ V, $V_{\phi H} = -11$ V, $V_{\phi L} = +5$ V, and $C_L = 10$ pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from clock ϕ_1 to data output	See Voltage Waveforms, Load = 3.3 kΩ		100	150	ns
t_{pd0}	Propagation delay time to logical 0 level from clock ϕ_1 to data output	See Voltage Waveforms, Load = 3.3 kΩ		120	180	ns

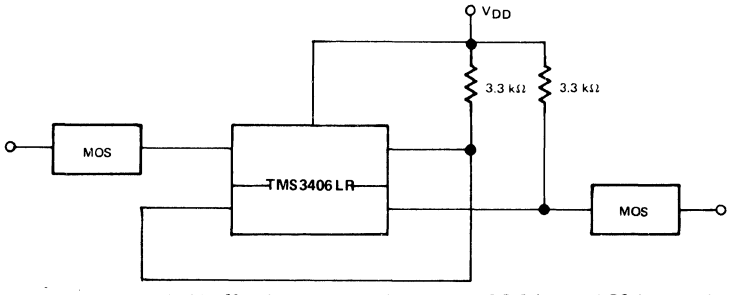
timing diagram



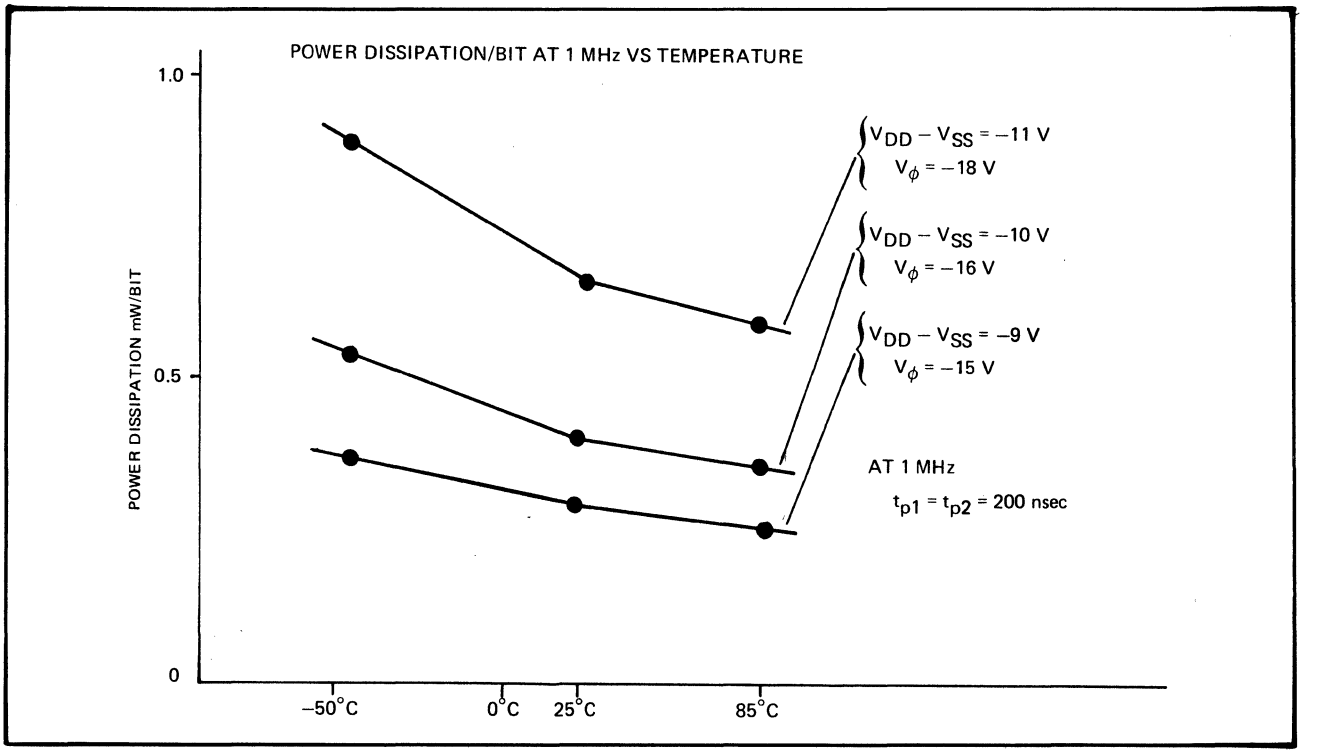
TTL interface

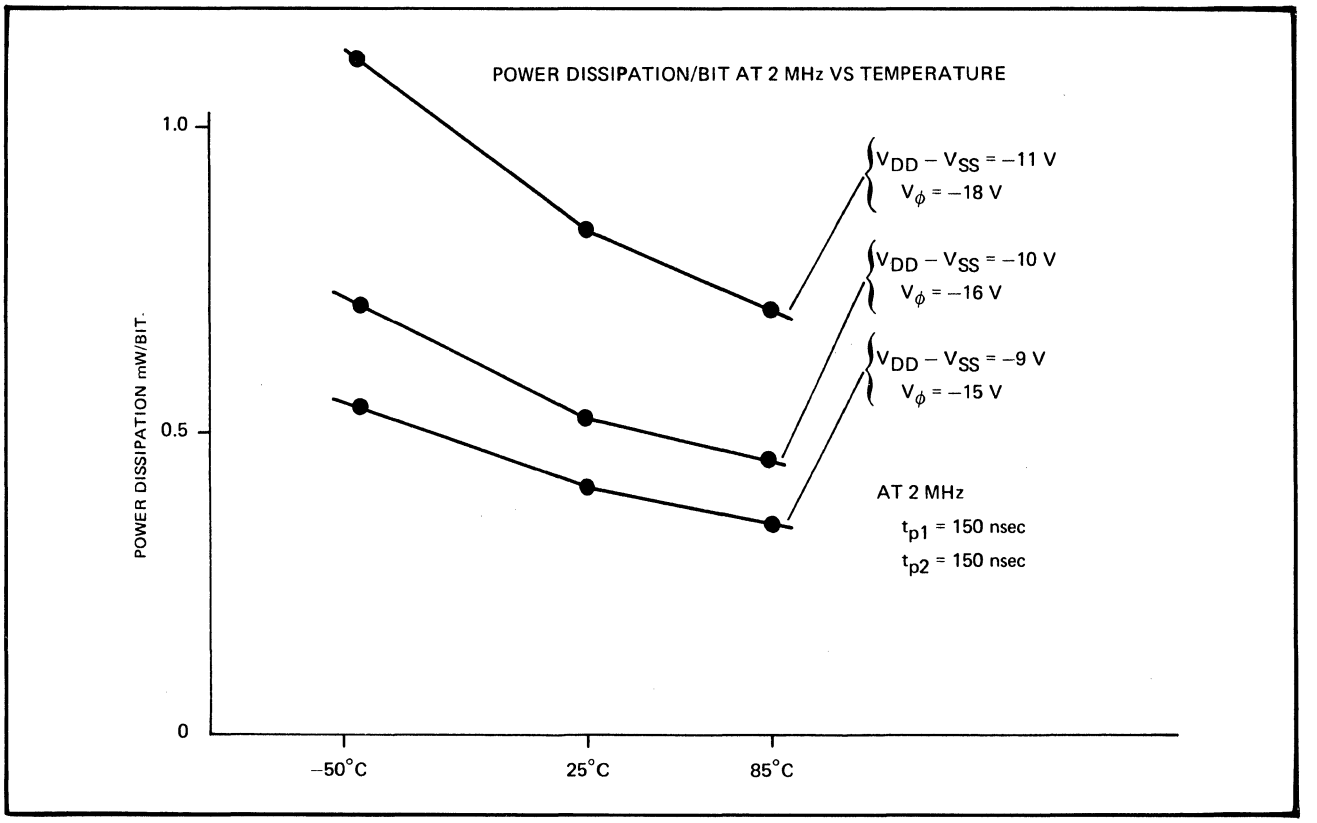


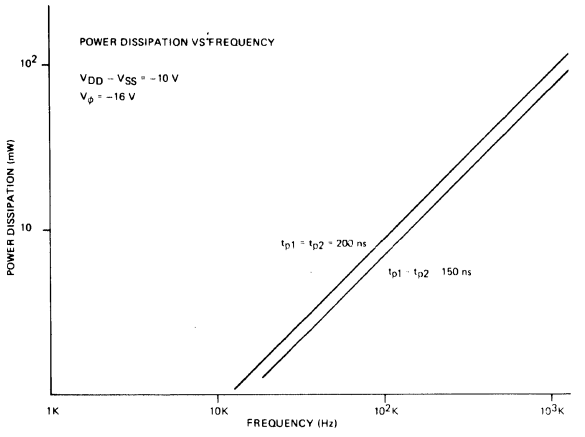
MOS interface

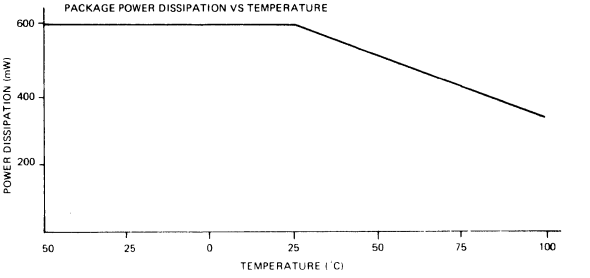


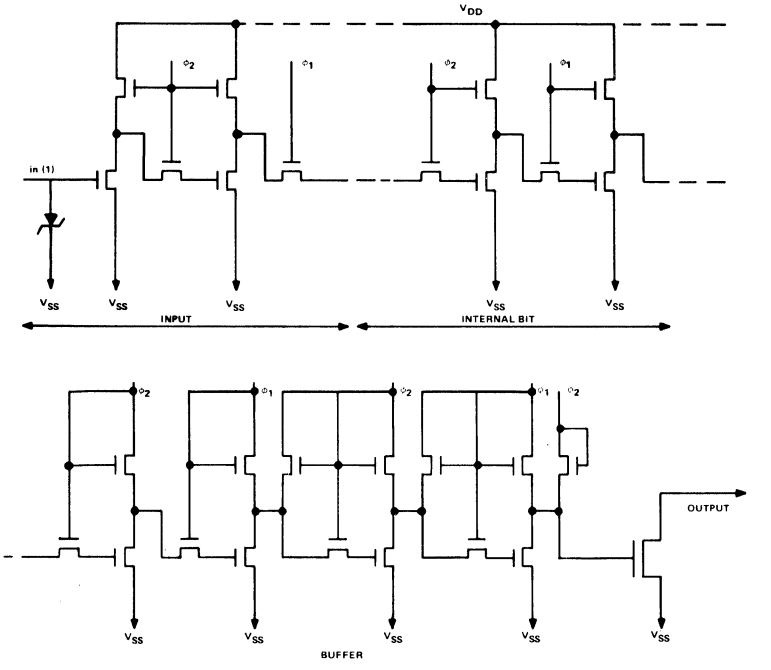
NOTE: The TMS 3406 LR features an open-ended buffer; however, load resistors of 3.3 kΩ and 20 kΩ can be programmed on the chip, upon request. At the input, resistors of 1 kΩ and 5 kΩ can be programmed upon request.











SCHEMATIC OF INTERNAL ORGANIZATION OF TMS 3406 LR

read only memories

1) INTRODUCTION

The information stored in a Read Only Memory (ROM) is permanently programmed into the memory at the time of its manufacture. Once the information is entered it cannot be changed – it can, however, be read out as often as desired. Before MOS circuits became available, the only practical means of realizing a ROM were with discrete diode matrices, or core memories. The most obvious advantages of MOS ROMs over these types are:

Cost – MOS typically one tenth that of diode matrix

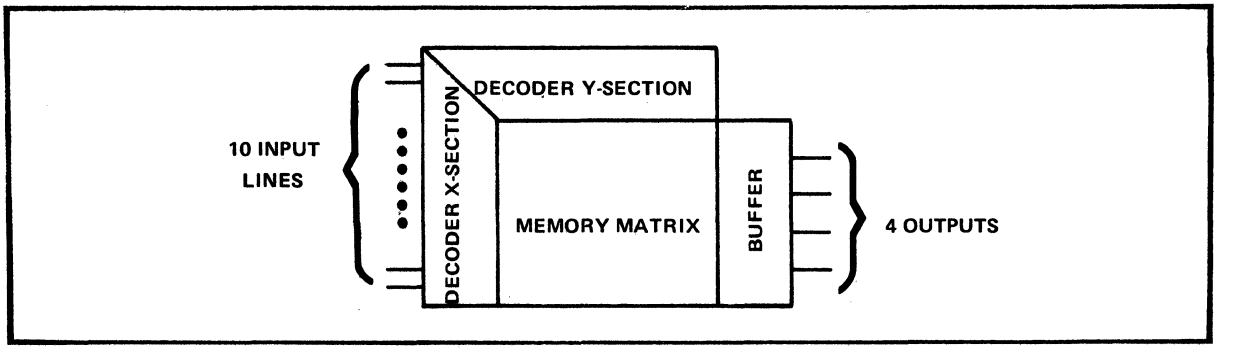
Size – MOS can put 4096 bits in a 24-pin package (chip size is 120 x 110 mil)

Speed – New MOS techniques can provide access times of 50 nsec.

2) STRUCTURE OF AN MOS ROM

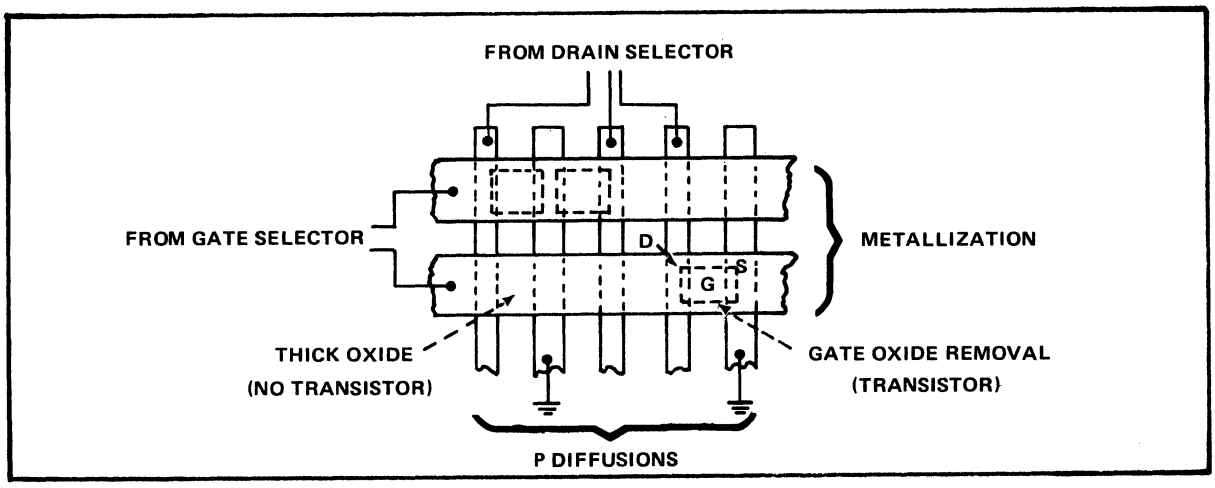
A single MOS ROM device will be made up of three sections:

- DECODER — in which the binary address is decoded and X-Y pairs of lines going to the memory matrix are enabled (one pair of X-Y lines if there is one bit per output word, two pairs of X-Y lines if there are two bits per output word, etc.)
- MEMORY MATRIX — containing as many MOS transistors locations as there are bits in the memory.
- BUFFER — which supplies output levels for the external circuitry.



EXAMPLE 1024 x 4 ROM

Consider for example a 4096-bit ROM organized as 1024 words of 4 bits. At the intersection of every X-line and Y-line, an MOS transistor can be either constructed or omitted by growing either a thin-gate oxide or a thick-gate oxide. The absence of an MOS transistor will be interpreted by the buffer as a logic 0, and the presence of a thin-gate MOS transistor will be interpreted as a logic 1. The programming of the memory (placement of the thin-gate oxide transistors) is performed during the manufacturing process.



MEMORY MATRIX

3) STATIC OR DYNAMIC?

Aside from the organization of the ROM, which defines its bit capacity, the most important parameter in most applications is probably access time. Access time is defined as the time required for a valid output to appear after a valid input has been applied.

In a static ROM there are no clocks required. If a valid input address is applied to the memory, after the expiration of the required access time, a valid output will appear. The output will remain valid as long as the input address remains unchanged. This is a tremendous advantage to the logic designer, and for this reason all present TI ROMs are of the static type. A dynamic ROM must be continually clocked at some minimum rate, otherwise the information vanishes.

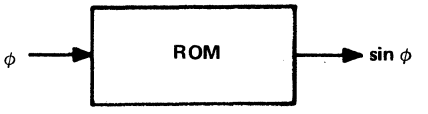
4) TYPICAL APPLICATIONS

Now that economical ROMs are available, the logic designer is taking advantage of this element. The most common areas of applications are found in:

- DISPLAYS
- COMPUTER TERMINALS
- COMPUTERS
- CALCULATORS

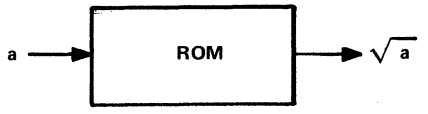
The most common applications are:

a) LOOK-UP TABLES – where the output is a mathematical function of the input. In computers for military applications, trigonometric functions are commonly used. A ROM can be used to obtain the sine of an angle instead of having to compute it by algorithm.



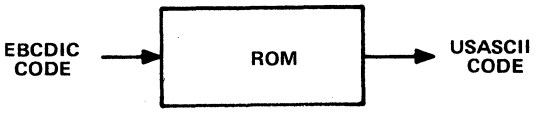
ROM AS TRIGONOMETRIC LOOK-UP TABLE

Some calculators also employ Look-up tables in performing arithmetic:



ROM AS ARITHMETIC LOOK-UP TABLE

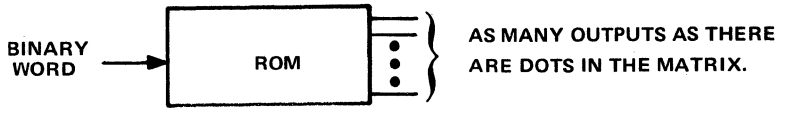
b) CODE CONVERSION – many applications require translating between one code and another. This is a common requirement of display manufacturers, computer terminal equipment manufacturers, and people involved with punched card reading and processing. For example, a ROM can be designed to accept input words in EBCDIC code and convert to words of USASCII code at the output.



ROM USED FOR CODE CONVERSION

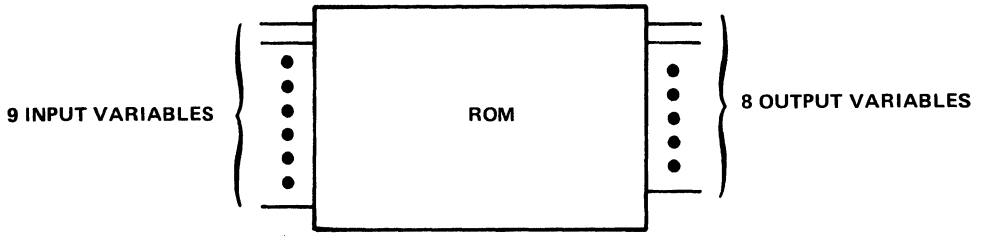
c) MICROPROGRAMMING – where a routine can be programmed directly (hard-wired programs), instead of being described (microprogram) on a stack of punched cards and then stored in the main memory. This technique is becoming more and more popular in medium-sized computers.

d) CHARACTER GENERATOR – where an alpha-numeric character is represented by a binary word. The characters can be visually represented by use of nixie tubes, a dot matrix, or a segment display. An example of a ROM used as a dot-matrix character generator is shown.



ROM USED AS CHARACTER GENERATOR

e) RANDOM LOGIC – ROMs can also be utilized to perform Boolean algebra. For example, a 4096-bit ROM organized as 512 words of 8 bits, has 9 inputs and 8 outputs. The ROM can be programmed to provide the outputs (which are Boolean functions of the input variables). One needs only to develop the truth table for the desired logic function.



ROM USED IN PERFORMING RANDOM LOGIC

$$0_1 = f_1 (A, B, C, \ldots .)$$

$$0_2 = f_2 (A, B, C, \ldots .)$$

To perform sequential logic the outputs would be fed back to the inputs.

5) **TI ROMs**

a) General Purpose Static ROMs

TMS 2800 JC	1024 bit capacity	256 x 4 organization
TMS 2600 JC	2048 bit capacity	512 x 4 or 256 x 8 organization
TMS 4300 JC	4096 bit capacity	4096 x 1 or 2048 x 2 or 1024 x 4 or 512 x 8 organization

b) Very-high speed Static ROM

TMS 4500 JC	2048 bit capacity	128 x 16 organization
TMS 4600 JC	2048 bit capacity	256 x 8 organization
TMS 4700 JC	2048 bit capacity	512 x 4 organization

c) Static Character Generators (5 x 7 dot matrix)

TMS 2400 JC	64 characters row output
TMS 4100 JC	64 characters column output
TMS 4880 JC	76 characters parallel output

For each series of devices TI has programmed at least one off-the-shelf device. This device can be used for evaluation by customers. For instance in the TMS 2400 JC series the TMS 2403 JC is an off-the-shelf ASCII row output character generator and the TMS 2404 JC is an off-the-shelf EBCDIC character generator.

custom bit pattern—customer interface

The programming of a single photomask permits the user to choose:

- Organization of the read-only memory
- Programming of the decode section
- Memory content
- Buffer configuration
- Chip enable polarities

All the other masks used during the processing are fixed and are common to a series of devices. For instance, all the devices of the TMS 2600 JC series (2048-bit Static ROM) use the same masks except the gate oxide removal mask which contains the custom pattern.

TI uses computer methods to assure a quick and fool-proof implementation of a custom bit pattern. This also reduces the cost of the implementation.

A "SOFTWARE PACKAGE" bulletin is used to transmit the customer inputs to TI, for each series of devices. These packages are available from the TI Sales Office.

The Software Package bulletin describes the format in which the inputs should be transmitted for best interface with the computer.

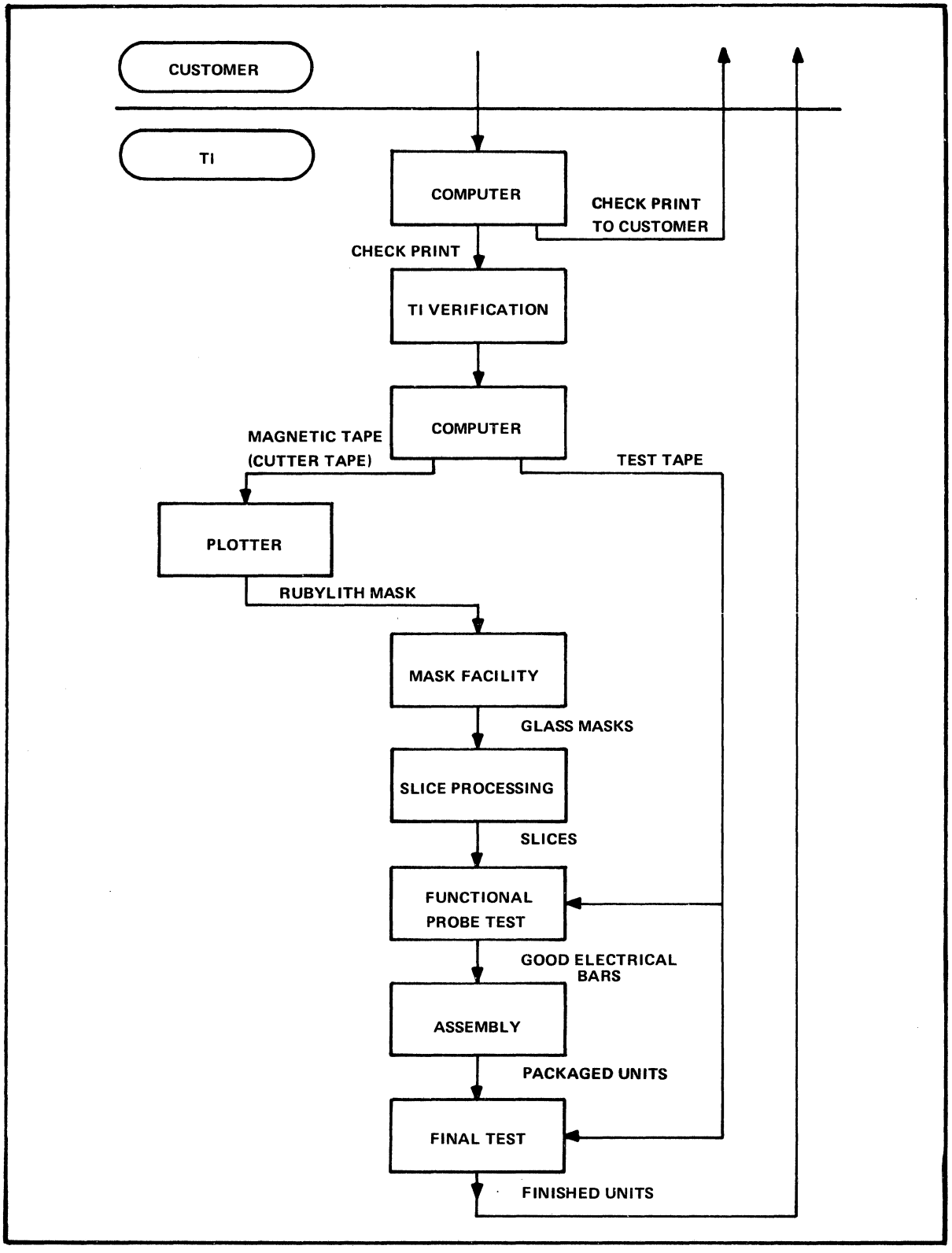
For character generators the Software Package includes grid on which the customer can map the desired outputs.

For read-only memories the Software Package describes the format used for writing the truth table of the ROM on punched cards.

Once the Software Package is received by TI it can be directly fed into a computer, or punched cards can be prepared from it and these punched cards can be fed into the computer.

The first computer output is a check print. If it is a read only memory the check print is a reconstitution of the truth table. In the case of a character generator, an overlay is produced. This overlay is in the same scale as the map included in the Software Package and permits easy verification of the punched cards. The check print is used for TI verification and a copy is sent to the customer.

custom bit pattern — customer interface



custom bit pattern—customer interface

Once the verification has been performed the computer generates a magnetic tape which will be used to drive a plotter, and a testing tape to be used for probe test and at final test.

The magnetic tape (cutter tape) is used to drive a plotter which cuts a film of rubylith mask. This rubylith mask when pealed is an enlargement of the gate oxide removal mask, which is used to to store the custom bit pattern. A glass mask is then made from the rubylith by a photographic process (reduction, step and repeat). This mask is used in production of the slice.

A slice contains many individual chips. Each chip is individually tested on a probe tester which uses the test tape generated by the computer.

The chips are then packaged and the completed units are final tested (logic and parametric tests). Finished units are then delivered to the customer.

TMS2400JC
row output character generator

FEATURING:

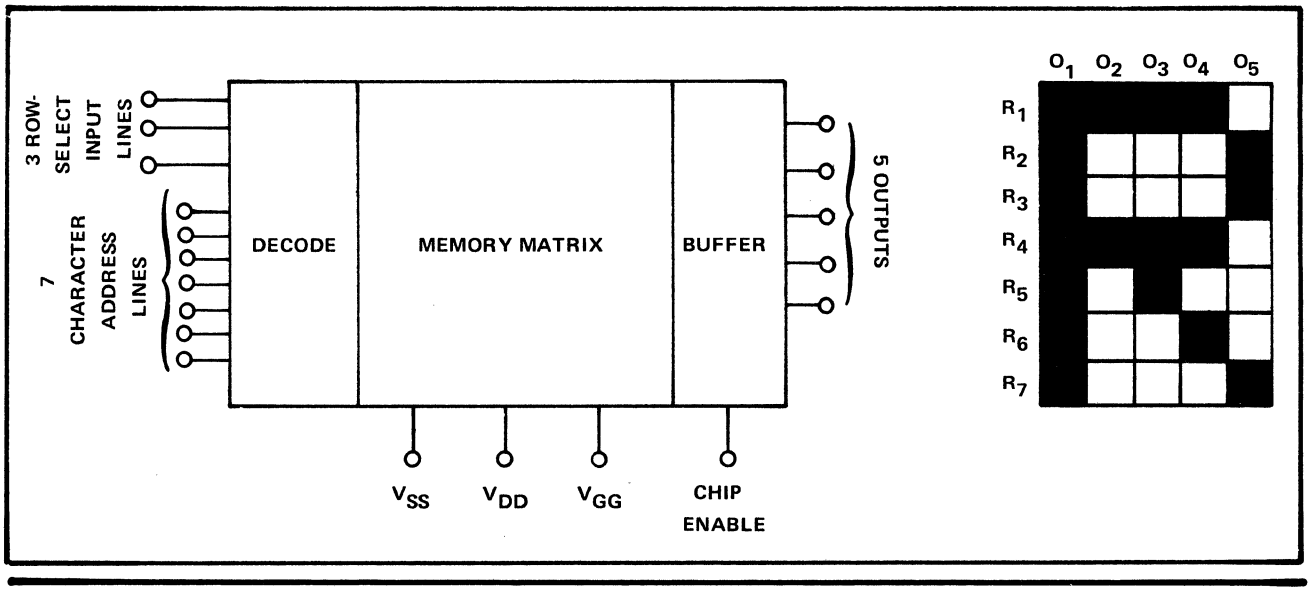
- Static operation
- 2240-Bit capacity
- 64 Characters of 35 bits (5 x 7)
- 7-Input character decoder
- 3-Input row decode
- 700 ns character access time
- Chip enable
- Open-drain or double-ended buffers
- TTL compatible

description

The TMS 2400 JC series is a family of read-only-memory subsystem components manufactured using MOS P-channel enhancement mode technology. All components in the series contain a 7-bit parallel-input character address decoder and a 3-bit parallel-input row address decoder, both complete with input inverters. Either open-drain or double-ended output buffers are provided for flexibility in external interfaces. The memory organization and data are permanently stored by programming a single mask during manufacture.

The memory is organized to function primarily as a row output character generator. The five outputs represent a row in a 5 x 7 dot matrix.

functional diagram



TMS2400JC
row output character generator

operation

The TMS 2400 JC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip enable) remains unchanged.

"Access time" is defined as the time required for all outputs to reach the minimum 1 level or maximum 0 level with the correct data. This time is measured from the point at which all address inputs and chip enable input are valid.

character scanning

The output character appears as a 7-word sequence on each of the five output lines. The sequence is controlled by the 3 row-select lines. The five outputs represent a row in a 5 x 7 character matrix. The row address can remain fixed while the character address changes (raster scan), or the character address may remain fixed while the row address changes (vertical or character scan).

row select truth table

ROW SELECT (NEGATIVE LOGIC)			SELECTS ROW
R_{s3}	R_{s2}	R_{s1}	
0	0	0	None
0	0	1	R 1
0	1	0	R 2
0	1	1	R 3
1	0	0	R 4
1	0	1	R 5
1	1	0	R 6
1	1	1	R 7

output buffers

The output buffers of the TMS 2400 JC may be programmed to be either single-ended (open drain) to drive TTL/DTL logic, or double-ended to drive MOS logic.

The number of characters is increased by hardwiring together the outputs of different chips. Note that, when using the hardwired output technique, one and only one of the chips that are hardwired together at the output should be double-ended; the remainder should be single-ended chips.

chip enable

The chip enable may be programmed to be either a 1 or a 0.

The decoder will accept a 7-bit parallel input. Because only 6 bits are required in order to give out the 64 input words, the seventh bit may be used as an extra chip enable in single-ended operations.

chip enable (continued)

A disable input on the chip enable input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer

logic definition

Negative logic is assumed on the inputs.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

An output blank is defined as the "off" state of the MOS output transistor, while an output dot is defined as the "on" state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1. These voltage values are with respect to network substrate terminal ($-V_{SS}$).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−16	V
Supply voltage V_{GG}	−22	−28	−29	V
Input, row select and enable logic 1	−9	−14	−16	V
Input, row select and enable logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

TMS2400JC
row output character generator

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(1)}$	Output blank current (open drain) See Notes 1 & 2	−14 applied to output			10	μA
$I_{out(0)}$	Output dot current (open drain) See Notes 1 & 2	−14 V applied to output	3	5		mA
$I_{out(0)}$	Output dot current (open drain)	V_{DD} = −12 V, V_{GG} = −24 V, −12 V applied to output	2	3		mA
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 0.5 mA		−0.7	−2	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 1 mA		−1.4	−2.5	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 1.5 mA		−2.0	−4	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 2 mA		−3	−5	V
$V_{out(1)}$	Output blank voltage (push-pull)	R_L = 1 mΩ	−10			V
$V_{out(0)}$	Output dot voltage (push-pull)	R_L = 1 mΩ			−2	V
	Power dissipation (Note 3)			350		mW
	Input leakage	−14 V applied to input			1	μA
I_{DD}	Drain current			20	30	mA
I_{GG}	Gate current			5	7	mA
	Input capacitance			5		pF

NOTES: 1. An output dot is defined as the ON state of the MOS output transistor. An output blank is defined as the OFF state.
2. See Switching Diagram
3. Open drain buffer, all outputs blank.

switching characteristics (under nominal operating conditions and at 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character access time (open drain) TTL load See Notes 1 & 2			600	800	ns
Character access time (open drain) TTL load See Notes 1 & 2	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		600	1000	ns
Row access time (open drain) TTL load See Notes 1 & 2			450	700	ns
Row access time (open drain) TTL load See Notes 1 & 2	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		550	850	ns
Chip enable access time (open drain) TTL load (See Notes 2 & 3)			100	300	ns
Chip enable access time (open drain) TTL load (See Notes 2 & 3)	V_{SS} = +12 V, V_{DD} = −0 V, V_{GG} = −12 V		125	300	ns

— continued —

dynamic electrical characteristics (under nominal operating conditions and at 25°C unless otherwise noted) — (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character access time (open drain) RC load (See Notes 1 & 2)	R_L = 1 kΩ, C_L = 10 pF		600	700	ns
Row access time RC load (See Notes 1 & 2)	R_L = 1 kΩ, C_L = 10 pF		400	650	ns
Character access time push-pull (See Notes 1 & 2)	R_L = 1 mΩ, C_L = 20 pF			1	μs
Row access time push-pull (See Notes 1 & 2)	R_L = 1 mΩ, C_L = 20 pF			1	μs

NOTES: 1. An output dot is defined as the ON state of the MOS output transistor. An output blank is defined as the OFF state.
2. See Switching Diagram.
3. Enable access time — time necessary to turn on or off the outputs through chip enable.

mechanical data

The TMS 2400 JC is mounted in a 28-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

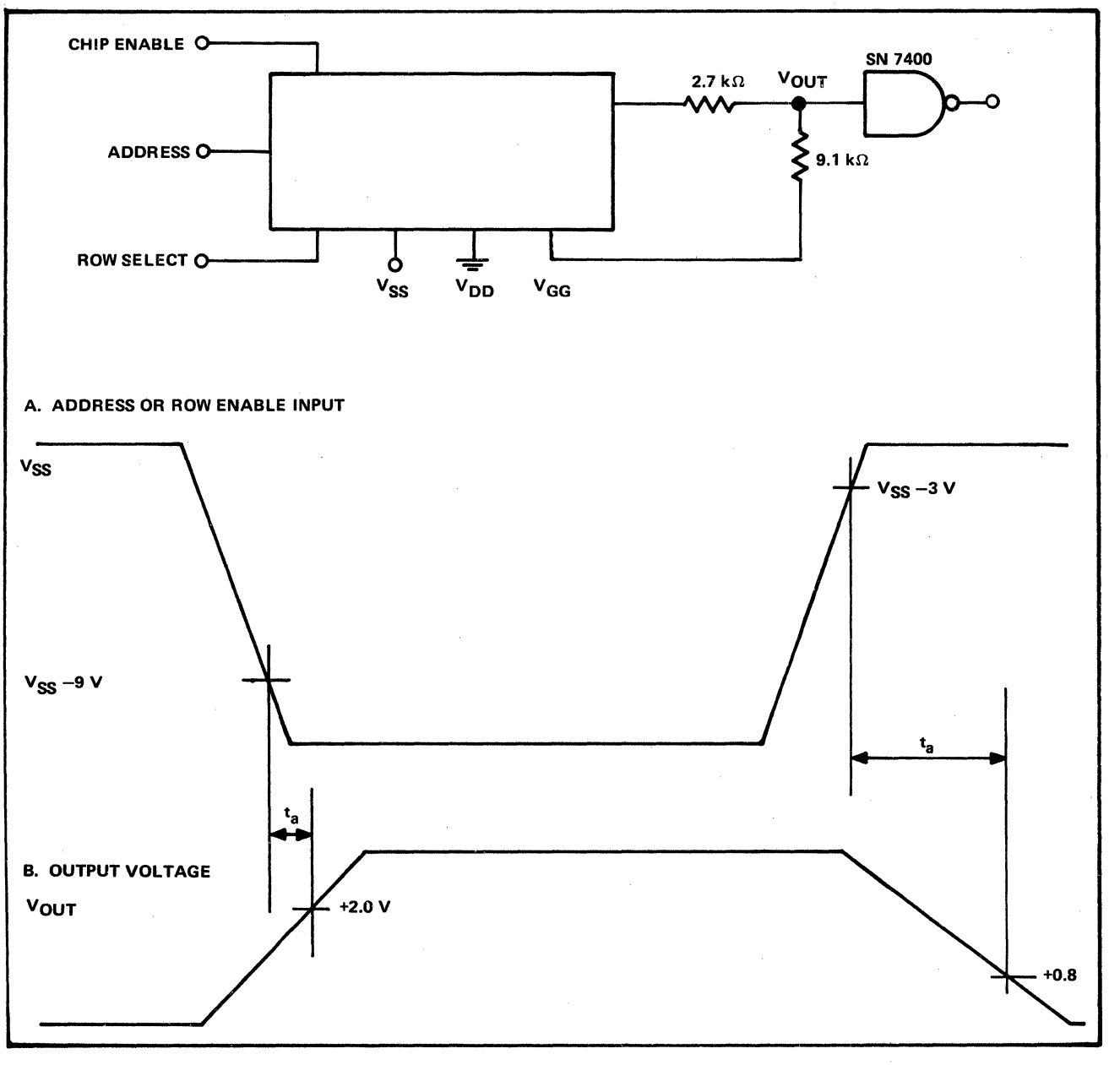
PIN CONFIGURATION

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NC	15	V_{SS}
2	RS_1	16	NC
3	RS_2	17	V_{DD}
4	RS_3	18	NC
5	NC	19	I_1
6	O_1	20	I_2
7	O_2	21	I_3
8	O_3	22	I_4
9	O_4	23	I_5
10	O_5	24	I_7
11	NC	25	NC
12	ENABLE	26	V_{GG}
13	NC	27	NC
14	NC	28	I_6

TMS2400JC
row output character generator

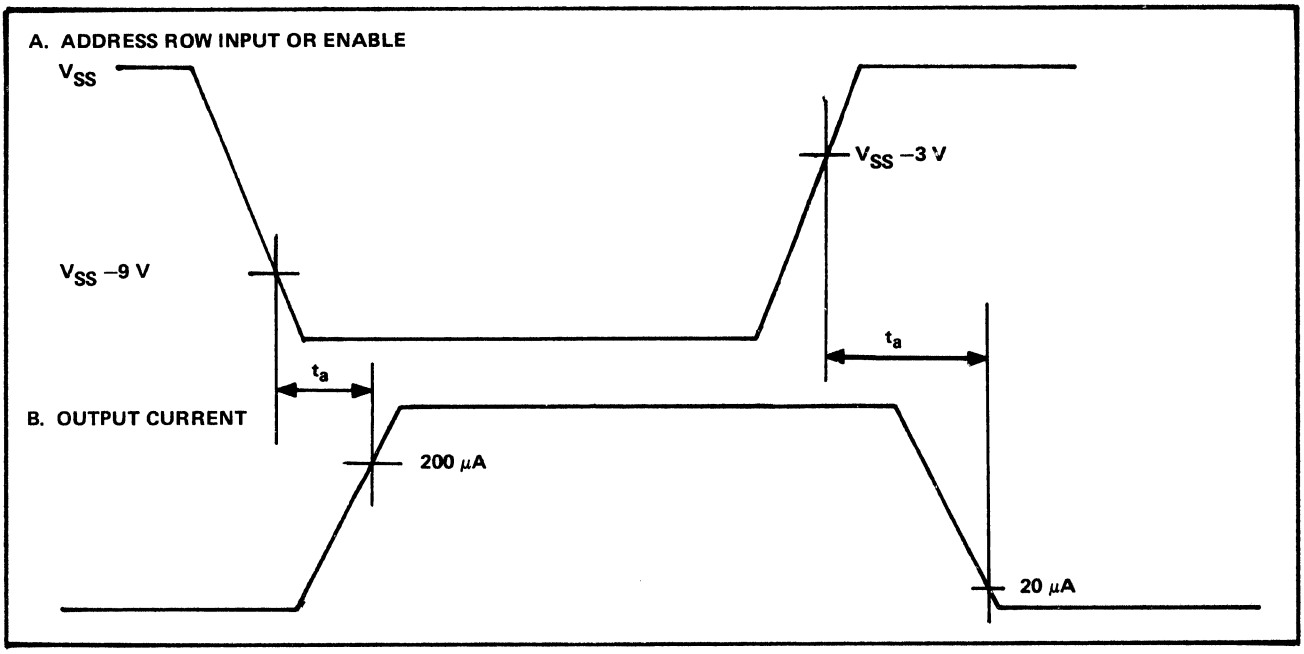
switching circuit and timing diagram

a) TTL load single ended buffer

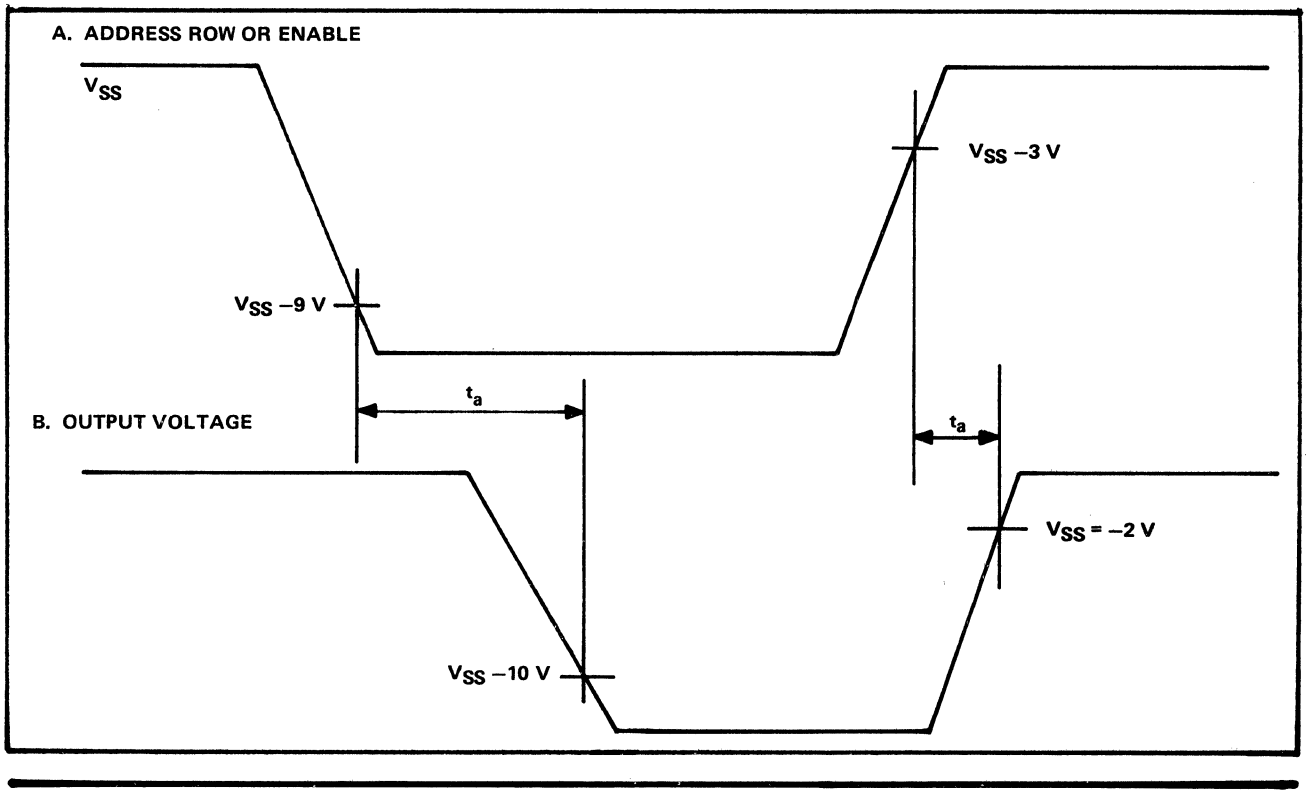


switching circuit and timing diagram (continued)

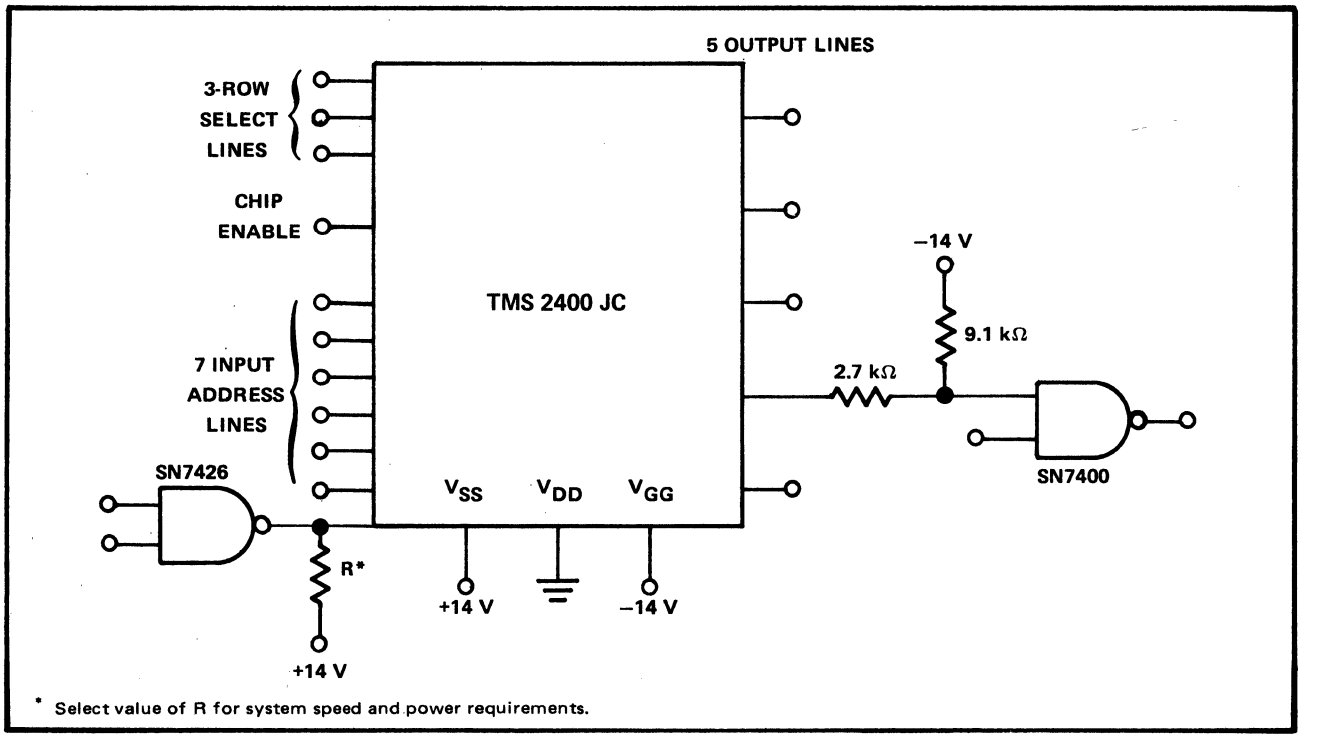
b) RC load single ended buffer



c) Double ended buffer



TMS2400JC
row output character generator
interfacing TMS 2400 JC in a TTL system



* Select value of R for system speed and power requirements.

custom circuits

The TMS 2400 JC series is programmed during the gate oxide removal stage of manufacturing. Only one mask per unique design need be created and all other processing steps remain the same for all devices. Options available to the customer during programming are:

- Character Format
- Enable Logic Polarity
- Single or Double-ended Outputs

The TMS 2400 JC series may also be used in micro-programming applications wherever a 448-word x 5-bit ROM may be useful.

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets (Software Package) are used. These encoding sheets are available from the TI sales offices.

standard circuits

Because certain codes are widely used, TI has created a series of standard devices, which are available off-the-shelf and for which there is no coding charge. The most widely used standard device is: TMS 2403 JC USASCII CODE (See attached character format).

Organization: 64-Character Storage

35-Bit Character Matrix

Chip Enable

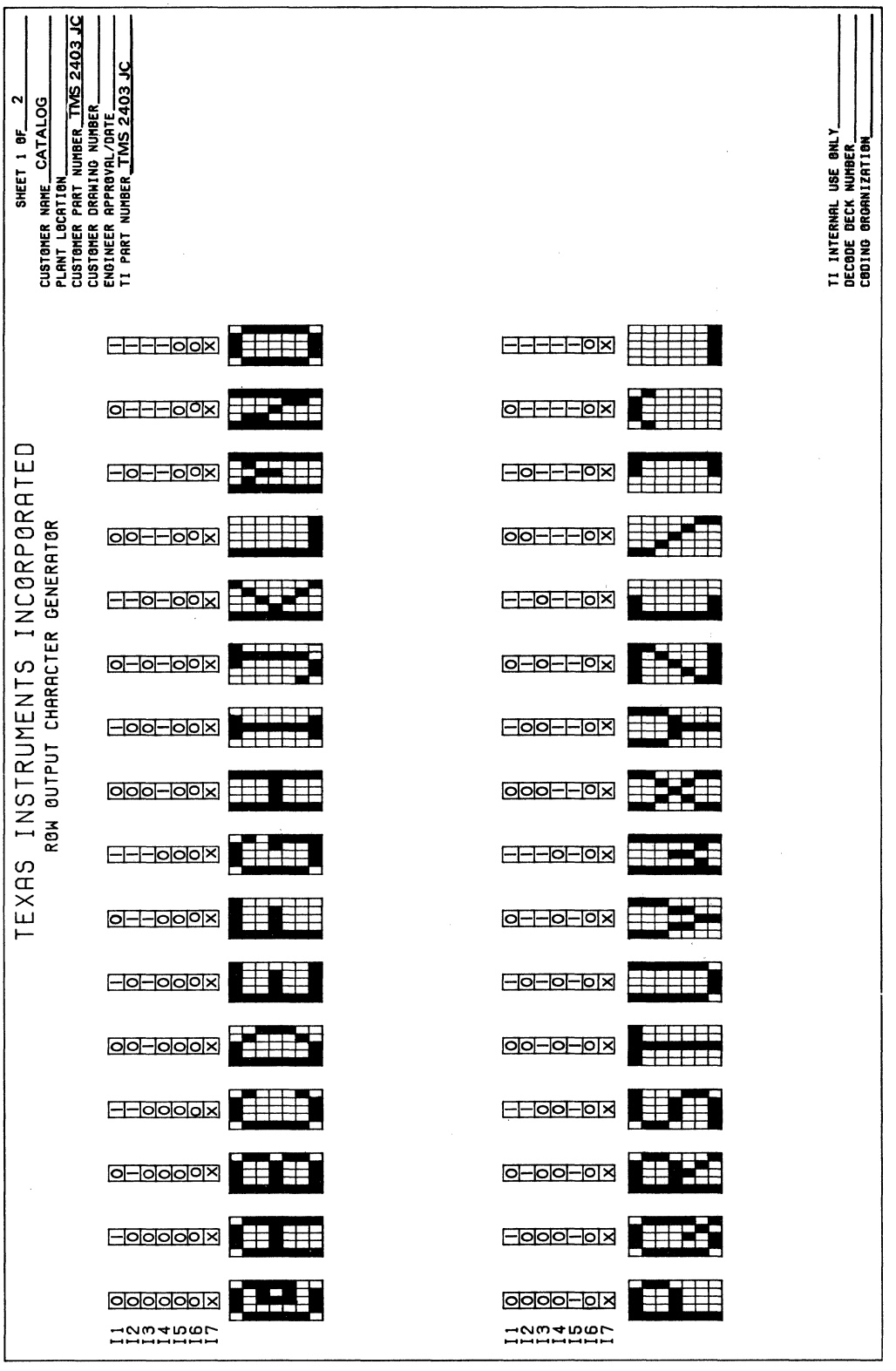
Other Available Standard Circuits:

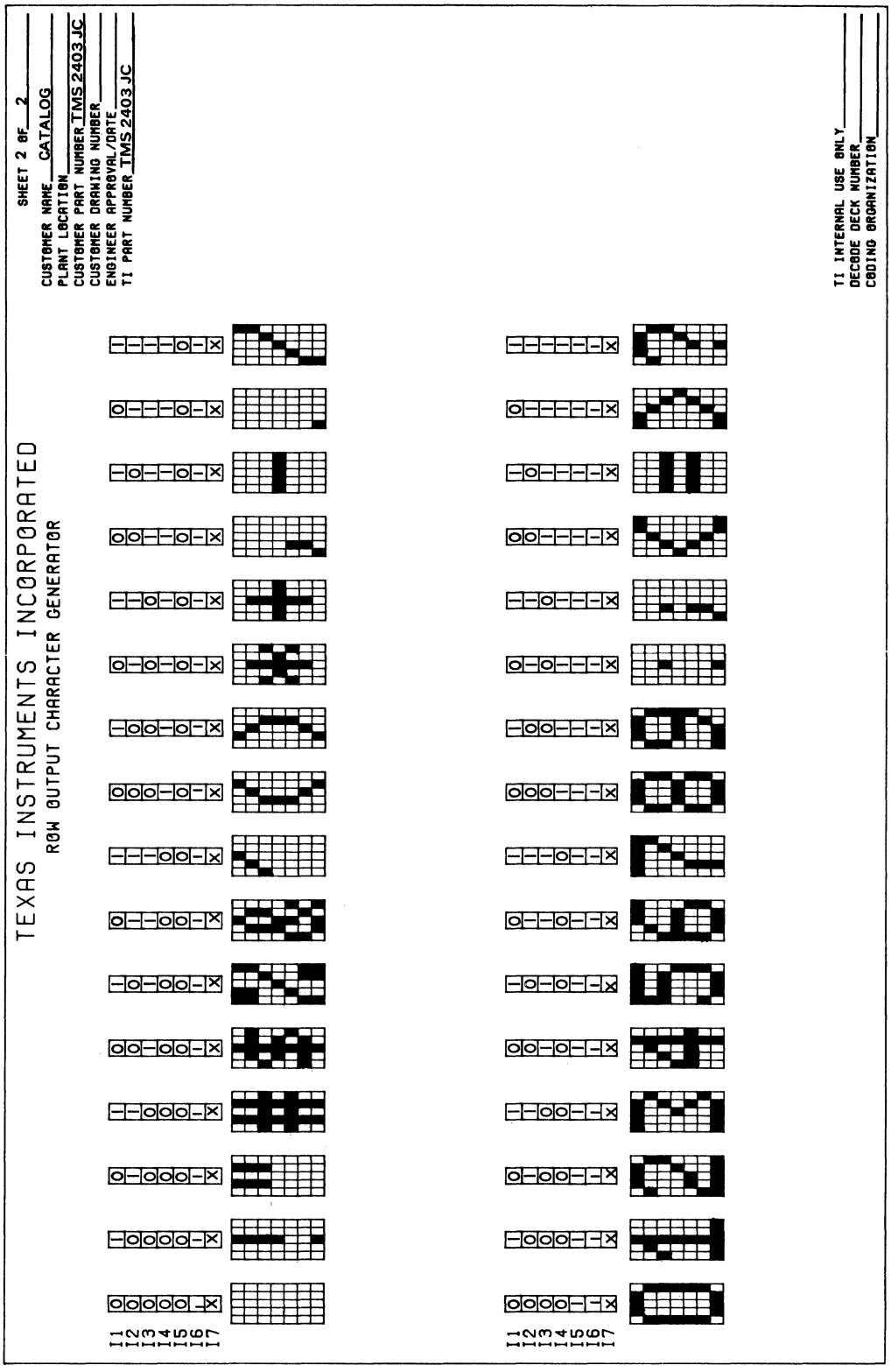
TMS 2404 JC – EBCDIC Character Generator (See attached character format)

66-Character Storage

35-Bit Character Matrix

TMS2400JC
row output character generator




SHEET 2 OF 2
CUSTOMER NAME CATALOG
PLANT LOCATION
CUSTOMER PART NUMBER TMS 2403 JC
CUSTOMER DRAWING NUMBER
ENGINEER APPROVAL/DATE
TI PART NUMBER TMS 2403 JC
TI INTERNAL USE ONLY
DECODE DECK NUMBER
CODING ORGANIZATION
TEXAS INSTRUMENTS INCORPORATED
ROW OUTPUT CHARACTER GENERATOR
I1 I2 I3 I4 I5 I6 I7

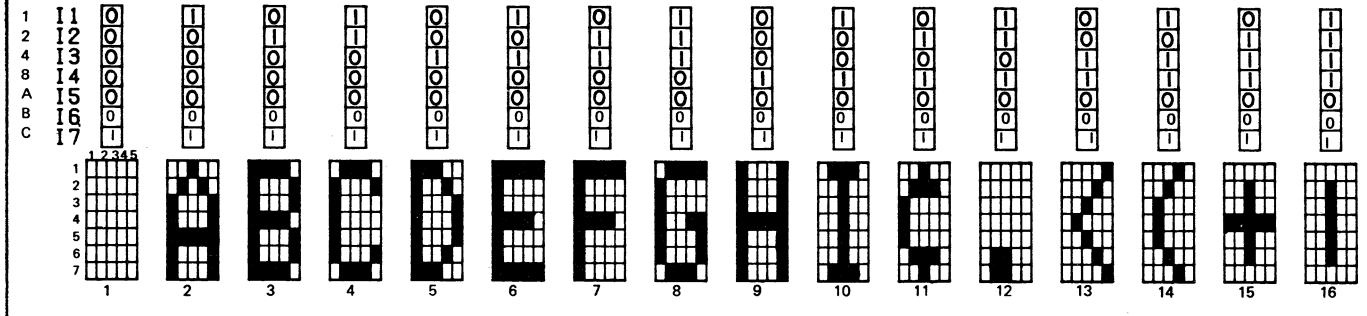
TEXAS INSTRUMENTS INCORPORATED

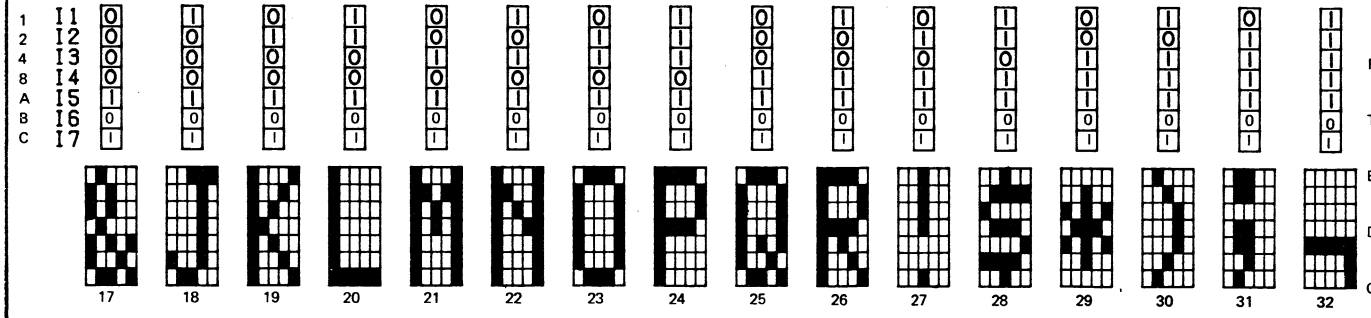
MOS ROW OUTPUT CHARACTER GENERATOR - TMS 2400 JC SERIES

Coding Sheet 1 of 2

CUSTOMER TI CATALOG

CUSTOMER PART No. CIRCUIT





Coding Symbols

1 — Most Negative Input
0 — Most Positive Input
X — Don't Care Condition

OPTIONS:

64 Characters of 5 x 7

I_6 is 0, Coding Sheet No. 1

I_6 is 1, Coding Sheet No. 2

Output Buffer:

Push Pull PP ☐

Open Drain OD ☒

Chip Is Enabled By:

1 ☒

0 ☐

For TI Use Only:

TI Part No. TMS 2404 JC

Engineering Approval BJB

Decode Deck 3

Character Array 0.3

Decode Array 0.3

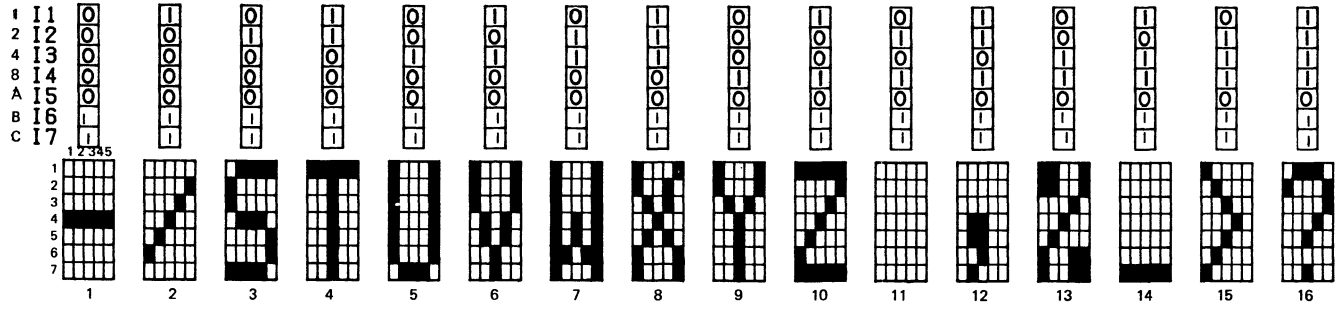
TEXAS INSTRUMENTS INCORPORATED

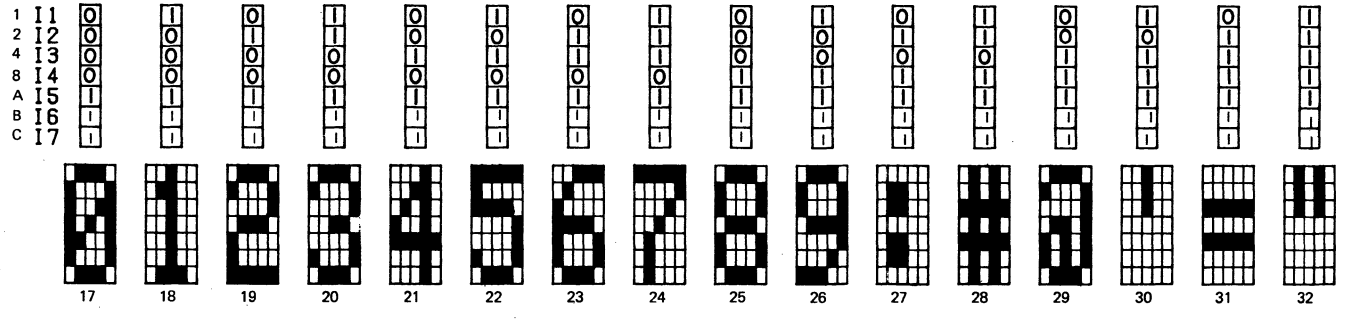
MOS ROW OUTPUT CHARACTER GENERATOR - TMS 2400 JC SERIES

Coding Sheet 2 of 2

CUSTOMER TI CATALOG

CUSTOMER PART No. CIRCUIT





Coding Symbols

1 – Most Negative Input
0 – Most Positive Input
X – Don't Care Condition

OPTIONS:

64 Characters of 5 x 7

I_6 is 0, Coding Sheet No. 1

I_6 is 1, Coding Sheet No. 2

Output Buffer:

Push Pull PP ☐

Open Drain OD ☒

Chip Is Enabled By:

1 ☒

0 ☐

For TI Use Only:

TI Part No. TMS 2404 JC

Engineering Approval BJB

Decode Deck 3

Character Array 0.3

Decode Array 0.3

TMS2600JC
2048-bit static read-only memory
preliminary information

FEATURING:

- **2048-Bit Capacity**
- **Static operation**
- **Maximum access time under 1 microsecond**
- **Two organizations available**
- **Open-drain output buffers or double-ended buffers**
- **TTL compatible**

description

The TMS 2600 JC series is a family of static read-only memories with capacity of 2048 bits.

Programming the memory content and output buffer configuration is accomplished by changing a single mask during the device fabrication.

Inputs are available for enabling the chip and for selecting between a memory organization of 512 words of four bits or 256 words of eight bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground (substrate).

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

logic definition

Negative logic is assumed

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2600 JC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times. Access time is defined as the time between a change of data on any logic input or chip select line and a change of data on the output of a TTL gate. (See switching circuit.)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

organizational control logic

		OUTPUTS	
		B_1 B_3 B_5 B_7	B_2 B_4 B_6 B_8
256 words of 8 bits (MC = Logical 0):	A_9 = Logical 1	Enabled	Enabled
512 words of 4 bits (MC = Logical 1):	A_9 = Logical 0	Enabled	Logical 1
	A_9 = Logical 1	Logical 1	Enabled

To use the device as a 512 words of 4 bits, connect B_1 to B_2, B_3 to B_4, B_5 to B_6, B_7 to B_8.

data encoding

Information concerning desired chip organization and type of output buffer should be submitted on the 2800 Software Package available from your TI field sales engineer. Data to be stored in the memory should be entered on punched cards in the format described by the Software Package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Data input voltage ranges (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1. These voltage values are with respect to V_{SS} (substrate).

TMS2600JC
2048-bit static read-only memory

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−22	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−22	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	550			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

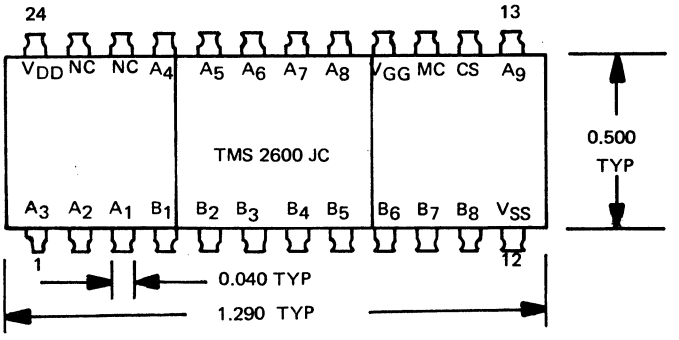
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3			mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		20	24	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.9	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Notes 1 and 3)	See switching circuit		600	900	ns
t_{A2}	Access time (Notes 1 and 3)	See switching circuit		620	900	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		170		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current (Note 2)	All outputs = Logical 0		14		mA
I_{GG}	Gate current			1.0		μA

NOTES: 1. Open-drain buffer
2. Push-pull buffer
3. See Switching Diagram
4. Either open-drain or push-pull configuration

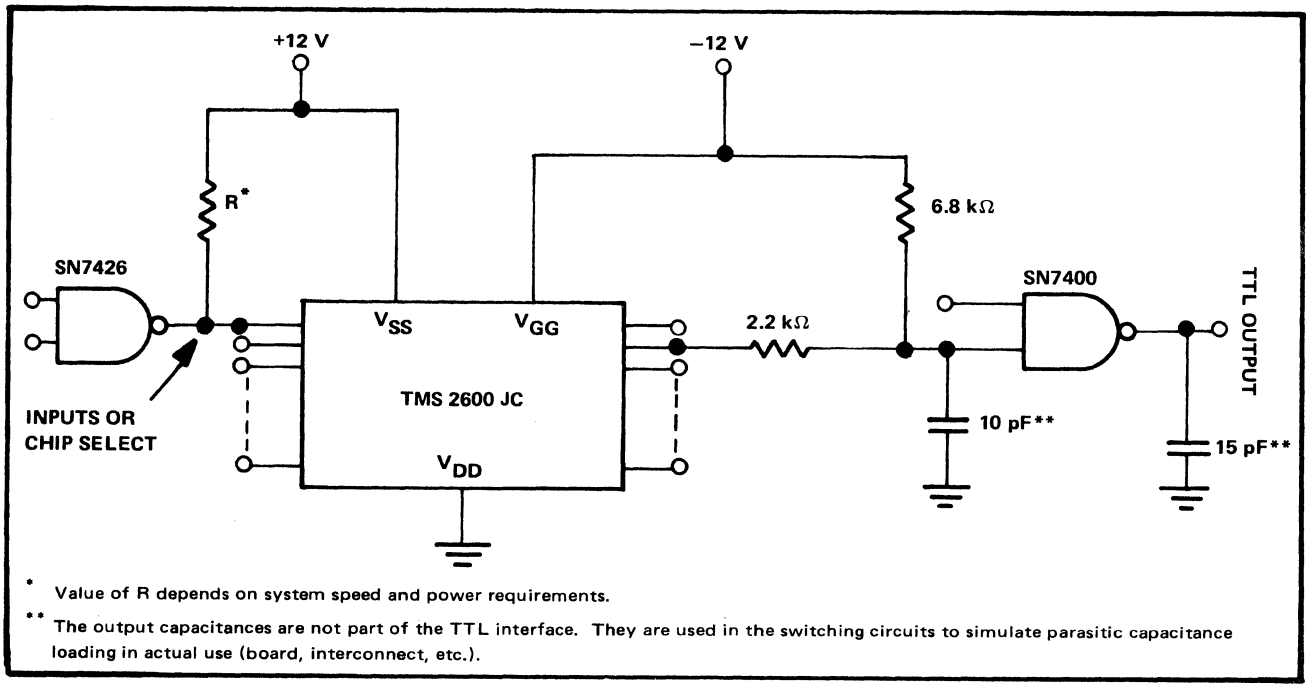
mechanical data and pin configuration

The TMS 2600 JC is mounted in a 24-pin hermetically sealed dual-in-line package consisting of gold-plated metal, ceramic sandwich body, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

A = input
B = output
MC = mode control
CS = chip select
V_{DD} = drain power supply
V_{GG} = ground power supply
V_{SS} = substrate



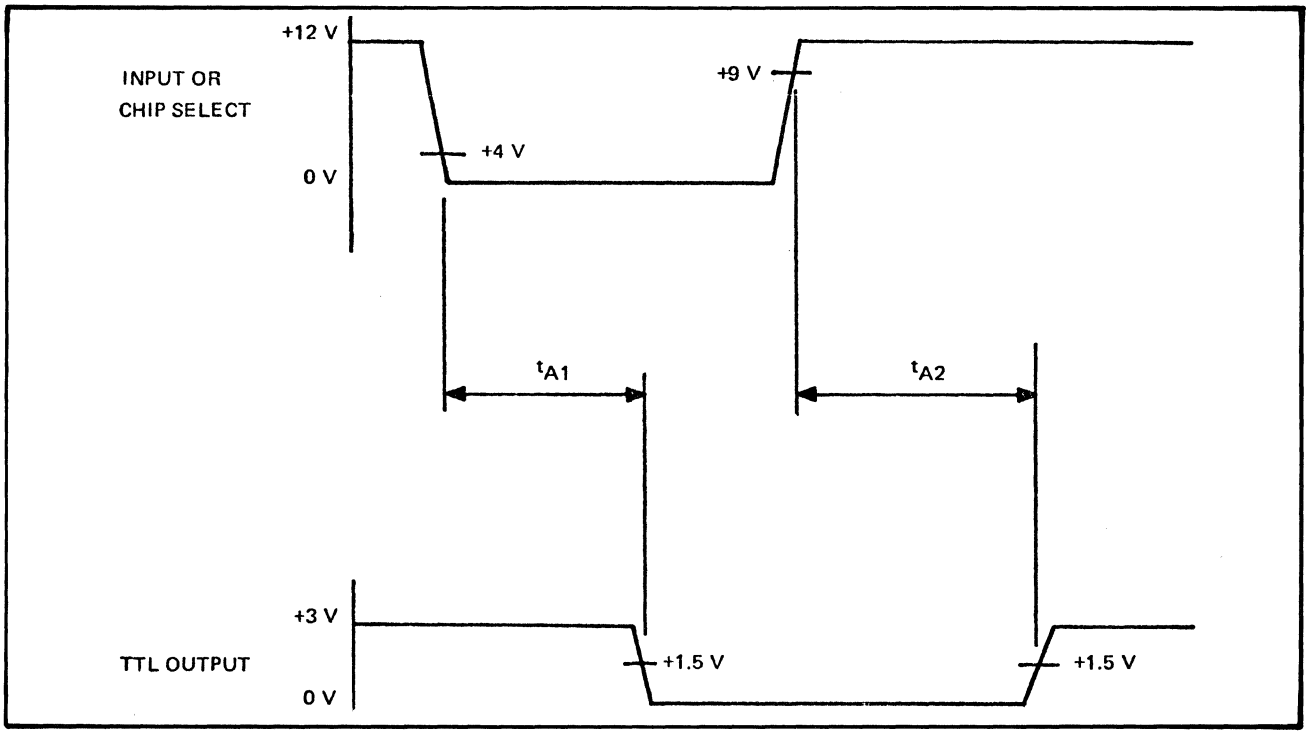
switching circuit and TTL interface



* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

switching diagram



The material herein is believed to be accurate and reliable; however, some parameters specified are derived from evaluation units and may change slightly after full characterization.

TMS2600JC

2048-bit static read-only memory

off the shelf devices

These devices have been programmed by TI and are available off the shelf:

1) TMS 2601 JC

   This device has been programmed to demonstrate the capabilities of the TMS 2000 JC series. It is used as a sample device. The buffers are single ended.

2) TMS 2602 JC Code Converter

   This device converts the USASCII code into the selectric line code and vice versa.

3) TMS 2603 JC Code Converter

   This device converts the full EBCDIC code into the USASCII code.

Truth tables of the TMS 2602 JC and 2603 JC are available upon request.

TRUTH TABLE, TMS 2601 JC

INPUT ADDRESS	$0_8 0_7 0_6 0_5 0_4 0_3 0_2 0_1$	INPUT ADDRESS	$0_8 0_7 0_6 0_5 0_4 0_3 0_2 0_1$	INPUT ADDRESS	$0_8 0_7 0_6 0_5 0_4 0_3 0_2 0_1$	INPUT ADDRESS	$0_8 0_7 0_6 0_5 0_4 0_3 0_2 0_1$
0	1 1 1 1 1 1 1 1	64	1 1 1 1 1 1 0 0	128	1 1 1 1 0 0 0 0	192	1 1 0 0 0 0 0 0
1	1 1 1 1 1 1 1 1	65	1 1 1 1 1 1 0 0	129	1 1 1 1 0 0 0 0	193	1 1 0 0 0 0 0 0
2	1 1 1 1 1 1 1 1	66	1 1 1 1 1 1 0 0	130	1 1 1 1 0 0 0 0	194	1 1 0 0 0 0 0 0
3	1 1 1 1 1 1 1 1	67	1 1 1 1 1 1 0 0	131	1 1 1 1 0 0 0 0	195	1 1 0 0 0 0 0 0
4	1 1 1 1 1 1 1 1	68	1 1 1 1 1 1 0 0	132	1 1 1 1 0 0 0 0	196	1 1 0 0 0 0 0 0
5	1 1 1 1 1 1 1 1	69	1 1 1 1 1 1 0 0	133	1 1 1 1 0 0 0 0	197	1 1 0 0 0 0 0 0
6	1 1 1 1 1 1 1 1	70	1 1 1 1 1 1 0 0	134	1 1 1 1 0 0 0 0	198	1 1 0 0 0 0 0 0
7	1 1 1 1 1 1 1 1	71	1 1 1 1 1 1 0 0	135	1 1 1 1 0 0 0 0	199	1 1 0 0 0 0 0 0
8	1 1 1 1 1 1 1 0	72	1 1 1 1 1 0 0 0	136	1 1 1 0 0 0 0 0	200	1 0 0 0 0 0 0 0
9	1 1 1 1 1 1 1 0	73	1 1 1 1 1 0 0 0	137	1 1 1 0 0 0 0 0	201	1 0 0 0 0 0 0 0
10	1 1 1 1 1 1 1 1	74	1 1 1 1 1 1 0 0	138	1 1 1 1 0 0 0 0	202	1 1 0 0 0 0 0 0
11	1 1 1 1 1 1 1 1	75	1 1 1 1 1 1 0 0	139	1 1 1 1 0 0 0 0	203	1 1 0 0 0 0 0 0
12	1 1 1 1 1 1 1 1	76	1 1 1 1 1 1 0 0	140	1 1 1 1 0 0 0 0	204	1 1 0 0 0 0 0 0
13	1 1 1 1 1 1 1 1	77	1 1 1 1 1 1 0 0	141	1 1 1 1 0 0 0 0	205	1 1 0 0 0 0 0 0
14	1 1 1 1 1 1 1 1	78	1 1 1 1 1 1 0 0	142	1 1 1 1 0 0 0 0	206	1 1 0 0 0 0 0 0
15	1 1 1 1 1 1 1 1	79	1 1 1 1 1 1 0 0	143	1 1 1 1 0 0 0 0	207	1 1 0 0 0 0 0 0
16	1 1 1 1 1 1 1 0	80	1 1 1 1 1 0 0 0	144	1 1 1 0 0 0 0 0	208	1 0 0 0 0 0 0 0
17	1 1 1 1 1 1 1 0	81	1 1 1 1 1 0 0 0	145	1 1 1 0 0 0 0 0	209	1 0 0 0 0 0 0 0
18	1 1 1 1 1 1 1 0	82	1 1 1 1 1 0 0 0	146	1 1 1 0 0 0 0 0	210	1 0 0 0 0 0 0 0
19	1 1 1 1 1 1 1 0	83	1 1 1 1 1 0 0 0	147	1 1 1 0 0 0 0 0	211	1 0 0 0 0 0 0 0
20	1 1 1 1 1 1 1 1	84	1 1 1 1 1 1 0 0	148	1 1 1 1 0 0 0 0	212	1 1 0 0 0 0 0 0
21	1 1 1 1 1 1 1 1	85	1 1 1 1 1 1 0 0	149	1 1 1 1 0 0 0 0	213	1 1 0 0 0 0 0 0
22	1 1 1 1 1 1 1 1	86	1 1 1 1 1 1 0 0	150	1 1 1 1 0 0 0 0	214	1 1 0 0 0 0 0 0
23	1 1 1 1 1 1 1 1	87	1 1 1 1 1 1 0 0	151	1 1 1 1 0 0 0 0	215	1 1 0 0 0 0 0 0
24	1 1 1 1 1 1 1 0	88	1 1 1 1 1 0 0 0	152	1 1 1 0 0 0 0 0	216	1 0 0 0 0 0 0 0
25	1 1 1 1 1 1 1 0	89	1 1 1 1 1 0 0 0	153	1 1 1 0 0 0 0 0	217	1 0 0 0 0 0 0 0
26	1 1 1 1 1 1 1 0	90	1 1 1 1 1 0 0 0	154	1 1 1 0 0 0 0 0	218	1 0 0 0 0 0 0 0
27	1 1 1 1 1 1 1 0	91	1 1 1 1 1 0 0 0	155	1 1 1 0 0 0 0 0	219	1 0 0 0 0 0 0 0
28	1 1 1 1 1 1 1 0	92	1 1 1 1 1 0 0 0	156	1 1 1 0 0 0 0 0	220	1 0 0 0 0 0 0 0
29	1 1 1 1 1 1 1 0	93	1 1 1 1 1 0 0 0	157	1 1 1 0 0 0 0 0	221	1 0 0 0 0 0 0 0
30	1 1 1 1 1 1 1 1	94	1 1 1 1 1 1 0 0	158	1 1 1 1 0 0 0 0	222	1 1 0 0 0 0 0 0
31	1 1 1 1 1 1 1 1	95	1 1 1 1 1 1 0 0	159	1 1 1 1 0 0 0 0	223	1 1 0 0 0 0 0 0
32	1 1 1 1 1 1 1 0	96	1 1 1 1 1 0 0 0	160	1 1 1 0 0 0 0 0	224	1 0 0 0 0 0 0 0
33	1 1 1 1 1 1 1 0	97	1 1 1 1 1 0 0 0	161	1 1 1 0 0 0 0 0	225	1 0 0 0 0 0 0 0
34	1 1 1 1 1 1 1 0	98	1 1 1 1 1 0 0 0	162	1 1 1 0 0 0 0 0	226	1 0 0 0 0 0 0 0
35	1 1 1 1 1 1 1 0	99	1 1 1 1 1 0 0 0	163	1 1 1 0 0 0 0 0	227	1 0 0 0 0 0 0 0
36	1 1 1 1 1 1 1 0	100	1 1 1 1 1 0 0 0	164	1 1 1 0 0 0 0 0	228	1 0 0 0 0 0 0 0
37	1 1 1 1 1 1 1 0	101	1 1 1 1 1 0 0 0	165	1 1 1 0 0 0 0 0	229	1 0 0 0 0 0 0 0
38	1 1 1 1 1 1 1 0	102	1 1 1 1 1 0 0 0	166	1 1 1 0 0 0 0 0	230	1 0 0 0 0 0 0 0
39	1 1 1 1 1 1 1 0	103	1 1 1 1 1 0 0 0	167	1 1 1 0 0 0 0 0	231	1 0 0 0 0 0 0 0
40	1 1 1 1 1 1 0 0	104	1 1 1 1 0 0 0 0	168	1 1 0 0 0 0 0 0	232	0 0 0 0 0 0 0 0
41	1 1 1 1 1 1 0 0	105	1 1 1 1 0 0 0 0	169	1 1 0 0 0 0 0 0	233	0 0 0 0 0 0 0 0
42	1 1 1 1 1 1 1 0	106	1 1 1 1 1 0 0 0	170	1 1 1 0 0 0 0 0	234	1 0 0 0 0 0 0 0
43	1 1 1 1 1 1 1 0	107	1 1 1 1 1 0 0 0	171	1 1 1 0 0 0 0 0	235	1 0 0 0 0 0 0 0
44	1 1 1 1 1 1 1 0	108	1 1 1 1 1 0 0 0	172	1 1 1 0 0 0 0 0	236	1 0 0 0 0 0 0 0
45	1 1 1 1 1 1 1 0	109	1 1 1 1 1 0 0 0	173	1 1 1 0 0 0 0 0	237	1 0 0 0 0 0 0 0
46	1 1 1 1 1 1 1 0	110	1 1 1 1 1 0 0 0	174	1 1 1 0 0 0 0 0	238	1 0 0 0 0 0 0 0
47	1 1 1 1 1 1 1 0	111	1 1 1 1 1 0 0 0	175	1 1 1 0 0 0 0 0	239	1 0 0 0 0 0 0 0
48	1 1 1 1 1 1 0 0	112	1 1 1 1 0 0 0 0	176	1 1 0 0 0 0 0 0	240	0 0 0 0 0 0 0 0
49	1 1 1 1 1 1 0 0	113	1 1 1 1 0 0 0 0	177	1 1 0 0 0 0 0 0	241	0 0 0 0 0 0 0 0
50	1 1 1 1 1 1 0 0	114	1 1 1 1 0 0 0 0	178	1 1 0 0 0 0 0 0	242	0 0 0 0 0 0 0 0
51	1 1 1 1 1 1 0 0	115	1 1 1 1 0 0 0 0	179	1 1 0 0 0 0 0 0	243	0 0 0 0 0 0 0 0
52	1 1 1 1 1 1 1 0	116	1 1 1 1 1 0 0 0	180	1 1 1 0 0 0 0 0	244	1 0 0 0 0 0 0 0
53	1 1 1 1 1 1 1 0	117	1 1 1 1 1 0 0 0	181	1 1 1 0 0 0 0 0	245	1 0 0 0 0 0 0 0
54	1 1 1 1 1 1 1 0	118	1 1 1 1 1 0 0 0	182	1 1 1 0 0 0 0 0	246	1 0 0 0 0 0 0 0
55	1 1 1 1 1 1 1 0	119	1 1 1 1 1 0 0 0	183	1 1 1 0 0 0 0 0	247	1 0 0 0 0 0 0 0
56	1 1 1 1 1 1 0 0	120	1 1 1 1 0 0 0 0	184	1 1 0 0 0 0 0 0	248	0 0 0 0 0 0 0 0
57	1 1 1 1 1 1 0 0	121	1 1 1 1 0 0 0 0	185	1 1 0 0 0 0 0 0	249	0 0 0 0 0 0 0 0
58	1 1 1 1 1 1 0 0	122	1 1 1 1 0 0 0 0	186	1 1 0 0 0 0 0 0	250	0 0 0 0 0 0 0 0
59	1 1 1 1 1 1 0 0	123	1 1 1 1 0 0 0 0	187	1 1 0 0 0 0 0 0	251	0 0 0 0 0 0 0 0
60	1 1 1 1 1 1 0 0	124	1 1 1 1 0 0 0 0	188	1 1 0 0 0 0 0 0	252	0 0 0 0 0 0 0 0
61	1 1 1 1 1 1 0 0	125	1 1 1 1 0 0 0 0	189	1 1 0 0 0 0 0 0	253	0 0 0 0 0 0 0 0
62	1 1 1 1 1 1 1 0	126	1 1 1 1 1 0 0 0	190	1 1 1 0 0 0 0 0	254	1 0 0 0 0 0 0 0
63	1 1 1 1 1 1 1 0	127	1 1 1 1 1 0 0 0	191	1 1 1 0 0 0 0 0	255	1 0 0 0 0 0 0 0

FEATURING:

- **1024-Bit Capacity**
- **Static operation**
- **Maximum access time under 1 microsecond**
- **Open-drain output buffers or double-ended buffers**
- **TTL compatible**

description

The TMS 2800 JC series is a family of static read-only memories with a capacity of 1024 bits.

Programming of the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

A chip select input is available.

The memory contents consist of 256 words of four bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground.

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

logic definition

Negative logic is assumed

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2800 JC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times.

Access time is defined as the time between a change of data on any logic input or chip select line and the change of data on the output of a TTL gate. (See timing diagram)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

data encoding

Information concerning desired chip organization and type of output buffer should be submitted on the 2800 Software Package available from your TI field sales engineer. Data to be stored in the memory should be entered on punched cards in the format described by the Software Package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Data input voltage ranges (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1. These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−22	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−22	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	550			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

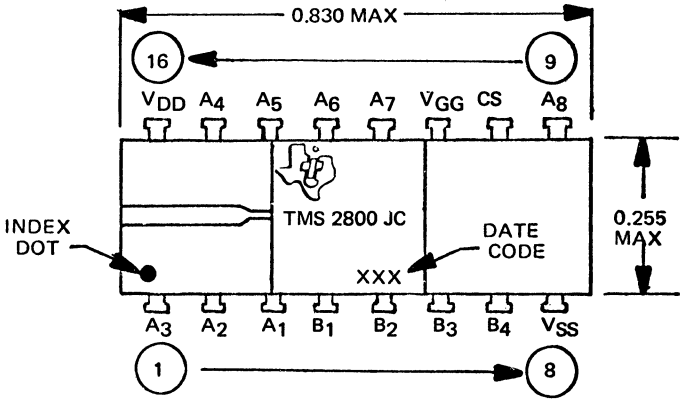
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3			mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3			24	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.9	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Note 3)	See switching circuit		600	900	ns
t_{A2}	Access time (Note 3)	See switching circuit		620	900	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		170		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current	All outputs @ Logical 0		14		mA
I_{GG}				1.0		mA

NOTES: 1. Open-drain buffer
2. Push-pull buffer
3. See Switching Diagram
4. Either open-drain or push-pull configuration

mechanical data and pin configuration

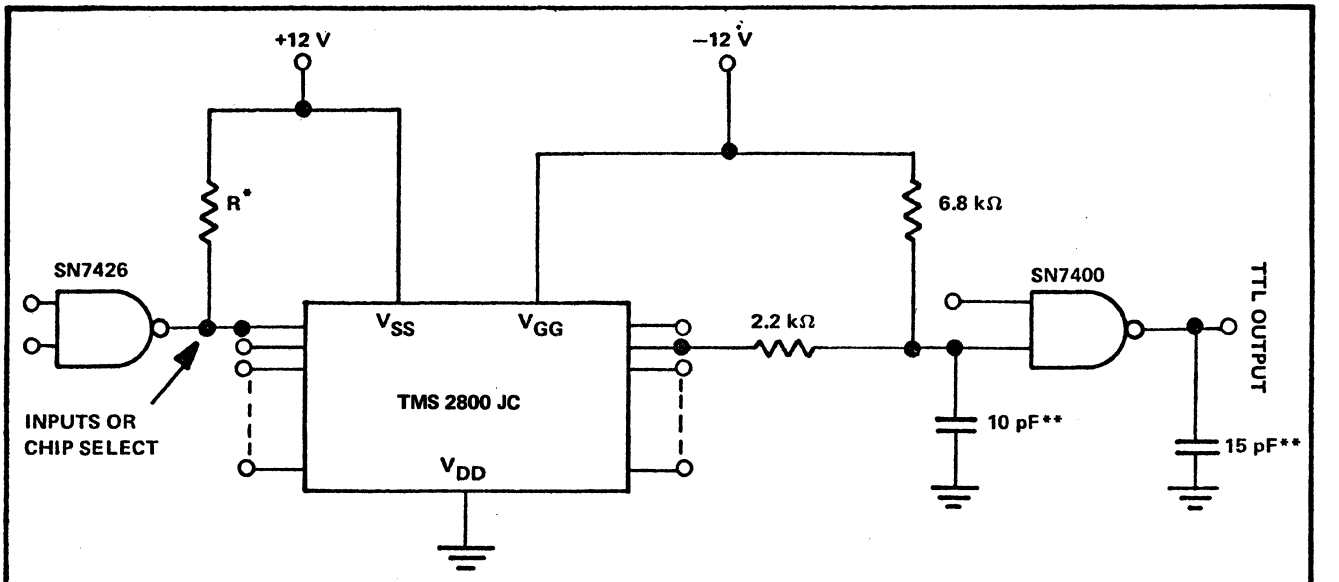
The TMS 2800 JC is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers.

A = input
B = output
V_{SS} = substrate
V_{DD} = drain supply
V_{GG} = gate supply



TMS2800JC
1024-bit static read-only memory

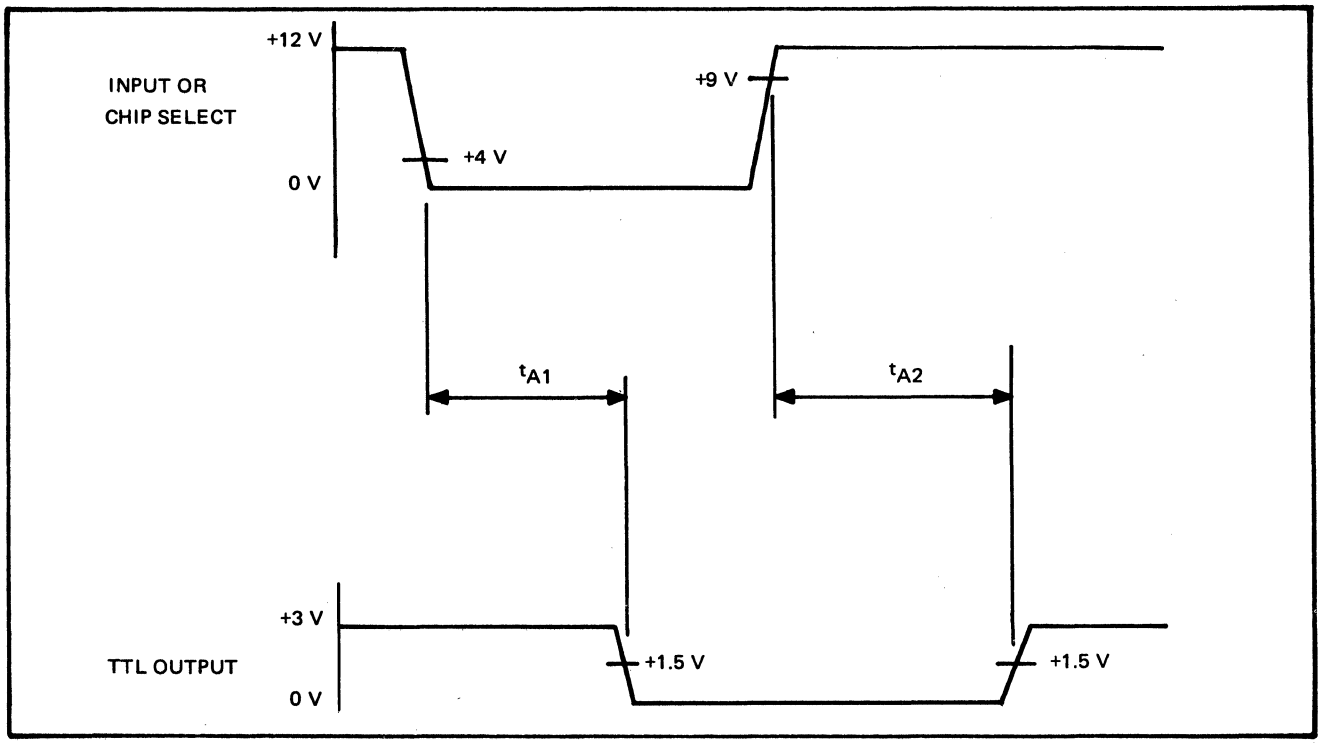
switching circuit and TTL interface



* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

switching diagram



FEATURING:

- Static operation
- 2240-Bit capacity
- 64 Characters of 35 bits (5 x 7) or
- 32 Characters of 70 bits (5 x 14)
- TTL compatible
- 700 ns maximum access time
- 7-Bit input address
- Single-ended open-drain output buffers

description

The TMS 4100 JC is a series of MOS Read Only Memories, with a total capacity of 2240 bits. Two organizations are available:

1) 64 words of 35 bits (5 x 7)

2) 32 words of 70 bits (5 x 14)

The memory is organized to function primarily as a character generator. The 7 outputs represent a column in a 5 x 7 dot matrix.

The output word appears as a 5-word sequence on each of the output lines. Sequence is controlled by 5 strobe lines (column select), which feed directly into the buffer section of the memory. By enabling the first strobe line, the first group of 7 bits (first column) is obtained at the output. Then the second, third, fourth, and fifth strobe lines are enabled. The column select can remain fixed while the character address changes, or the character address may remain fixed while the column select changes.

The decoder will accept a 7-bit parallel input. Since only 6 bits are required in order to decode the 64 input words, the seventh bit may be used as a chip enable. If the memory is organized as 32 words of 70 bits, it is possible to have two chip enable lines.

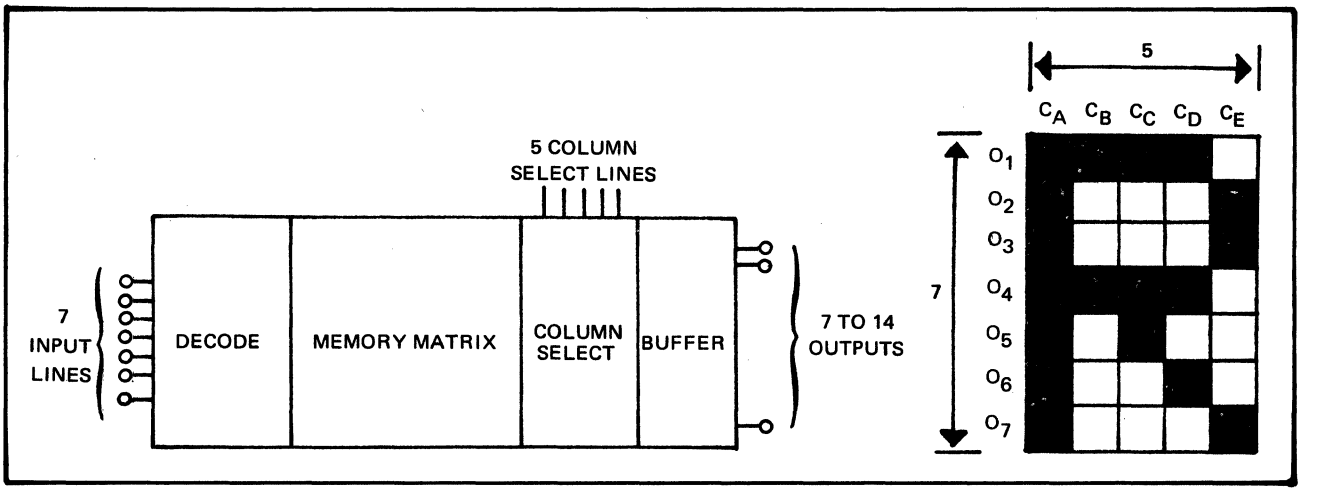
The TMS 4100 JC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times.

The output buffers are single ended, open drain and allow the wired OR connection.

The number of words per output is increased by hardwiring together the outputs of different devices. Hardwiring outputs perform the AND function in negative logic.

TMS4100JC
series character generator

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1. These voltage values are with respect to network ground terminal (V_{SS}).

logic definition

Negative logic is assumed for all inputs.

a) Logic 1 = most negative voltage (−14 V)

b) Logic 0 = most positive voltage (0 V)

An output dot is defined as the "on" state of the output MOS transistor and an output blank as the "off" state.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−16	V
Supply voltage V_{GG}	−24	−28	−29	V
Input, column select and enable logic 1	−9	−14	−16	V
Input, column select and enable logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{(1)}$	Output Blank Current (Note 1)	−14 V applied to output			10	μA
$I_{(0)}$	Output Dot Current (Note 1)	−14 V applied to output	1	2		mA
$I_{(0)}$	Output Dot Current (Note 1)	V_{DD} = −12 V, V_{GG} = −24 V, −12 V applied to output	0.5	1		mA
$V_{(0)}$	Output Voltage for a Dot (Note 1)	I_O = 0.5 mA		−1.3	−2.8	V
$V_{(1)}$	Output Voltage for a Dot (Note 1)	I_O = 1 mA		−2.5	−6	V
	Input and Column Select Leakage Current	−26 V applied to input			1	μA
I_{DD}	Drain Supply Current			14	25	mA
I_{GG}	Gate Supply Current				1	mA
	Power Dissipation			250	400	mW
	Address input Capacitance			6	15	pF

NOTE 1. An output dot is defined as the ON state of the MOS output transistor. An output blank is defined as the OFF state.

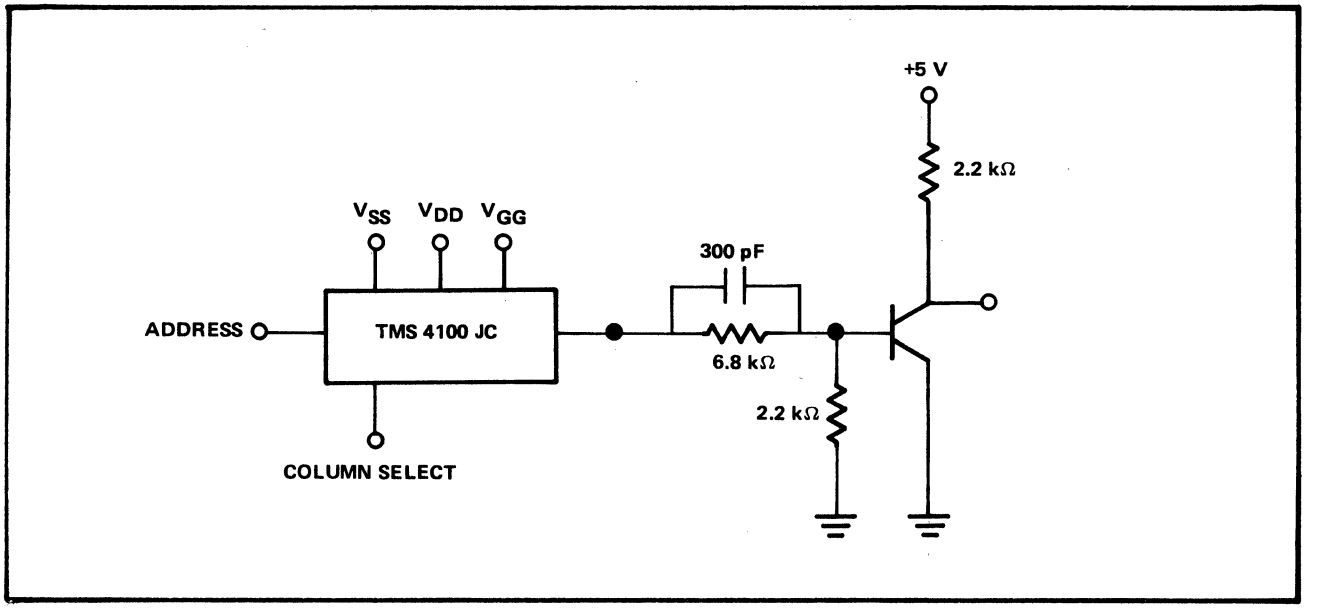
switching characteristics (at nominal operating conditions and 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character Access Time Bipolar Load (Note 2) See Switching Diagram			400	700	ns
Character Access Time Bipolar Load (Note 2) See Switching Diagram	V_{SS} = +12 V, V_{DD} = −0 V, V_{GG} = −12 V		500	700	ns
Column Select Access Time Bipolar Load (Note 2) See Switching Diagram			150	300	ns
Column Select Access Time Bipolar Load (Note 2) See Switching Diagram	V_{SS} = +12 V, V_{DD} = −0 V V_{GG} = −12 V		200	300	ns
Character Access Time Low Power TTL Load (Note 2) See Switching Diagram			500	850	ns
Character Access Time Low Power TTL Load (Note 2) See Switching Diagram	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		600	950	ns
Column Select Access Time Low Power TTL Load (Note 2) See Switching Diagram			200	400	ns
Column Select Access Time Low Power TTL Load (Note 2) See Switching Diagram	V_{SS} = +12 V, V_{DD} = 0 V V_{GG} = −12 V		300	500	ns
Chip Enable Access Time			400	700	ns

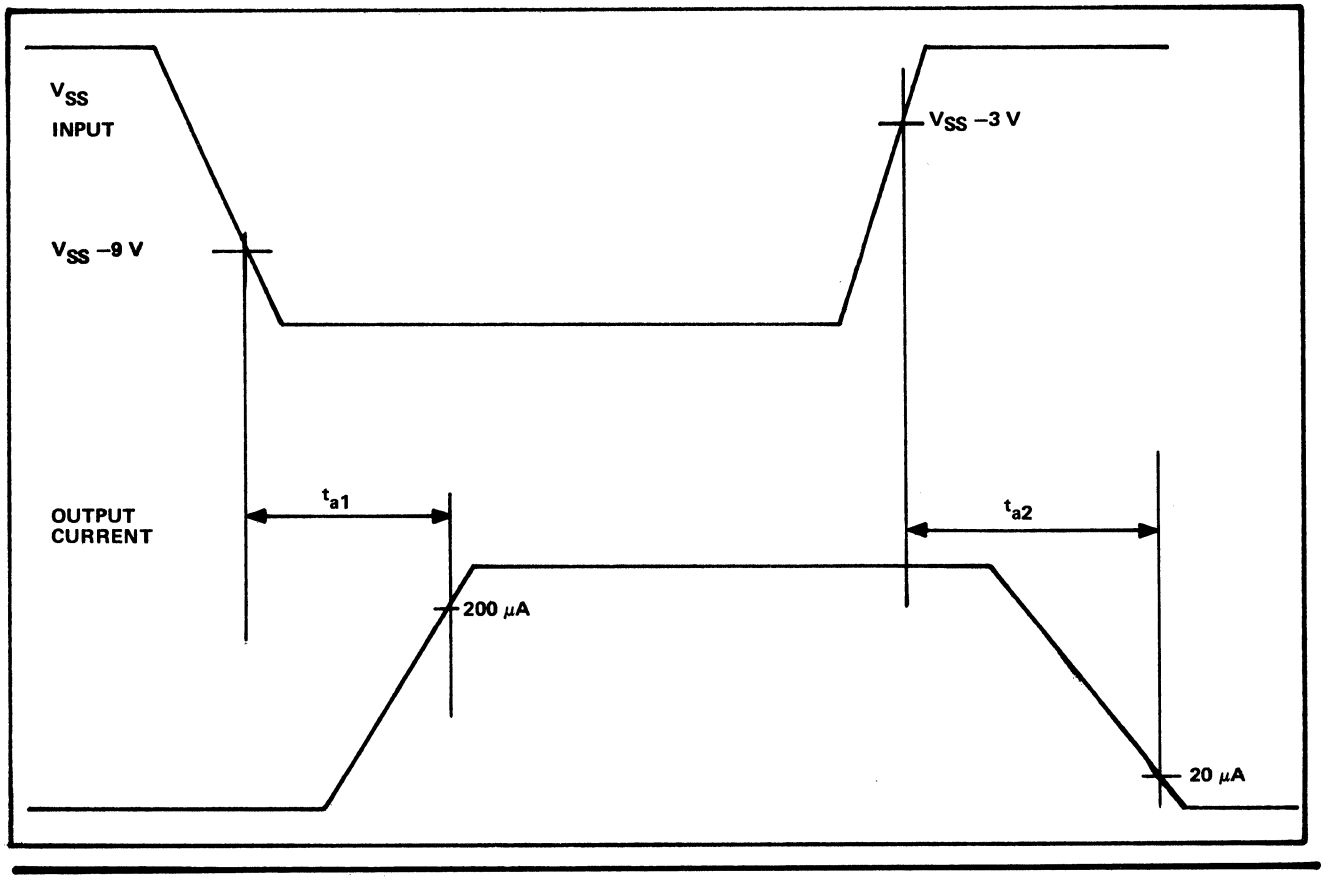
NOTE 2. Character access time is defined as the memory access time when changing the character address input and holding the column select input lines constant.

TMS4100JC
series character generator
switching circuit and switching diagram

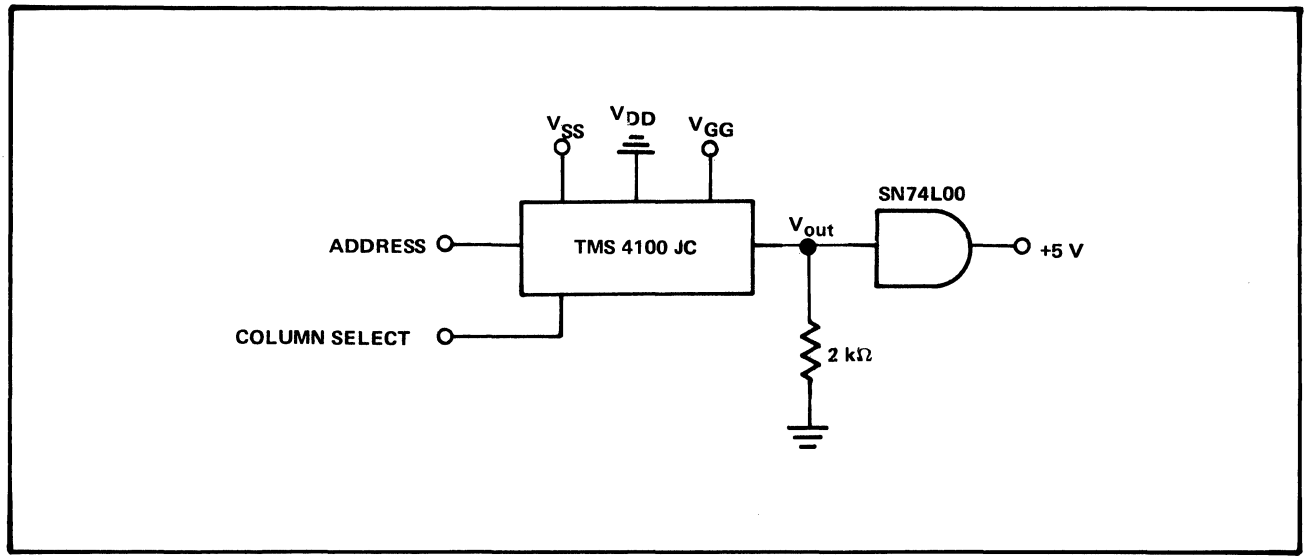
a) Bipolar load



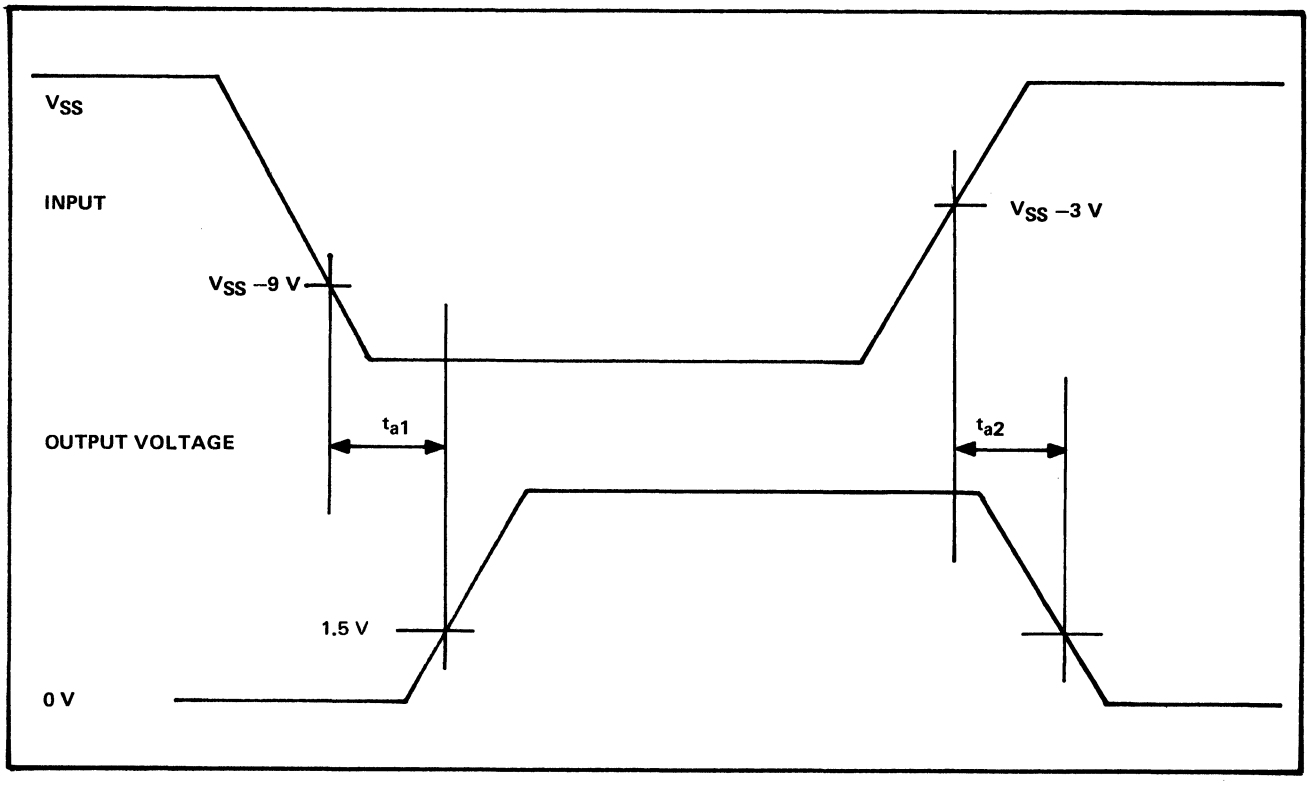
Address column select input voltage



b) Low power TTL load



Address column select input voltage



TMS4100JC
series character generator

mechanical data

The TMS 4100 JC is mounted in a 28-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

pin configuration

Depending on the organization of the memory, three pin configurations may be used.

Package Pin Configuration, TMS 4100 JC

PIN NO.	CONFIGURATION A — TOTAL OUTPUTS— 7 OR FEWER	CONFIGURATION B — TOTAL OUTPUTS— MORE THAN 7, FEWER THAN 14	CONFIGURATION C — TOTAL OUTPUTS— 14
1	O_1	O_1	O_1
2	NC	O_2	O_2
3	O_2	O_3	O_3
4	NC	O_4	O_4
5	O_3	O_5	O_5
6	NC	O_6	O_6
7	O_4	O_7	O_7
8	NC	O_8	O_8
9	O_5	O_9	O_9
10	NC	O_{10}	O_{10}
11	O_6	O_{11}	O_{11}
12	NC	O_{12}	O_{12}
13	O_7	O_{13}	O_{13}
14	V_{DD}	V_{DD}	O_{14}
15	V_{GG}	V_{GG}	V_{DD}
16	I_6	I_6	V_{GG}
17	V_{SS}	V_{SS}	I_6
18	C_A	C_A	V_{SS}
19	C_B	C_B	C_A
20	C_C	C_C	C_B
21	C_D	C_D	C_C
22	C_E	C_E	C_D
23	I_5	I_5	C_E
24	I_4	I_4	I_5
25	I_3	I_3	I_4
26	I_2	I_2	I_3
27	I_1	I_1	I_2
28	I_7	I_7	I_1

NC – NOT CONNECTED
C – COLUMN SELECT
O – OUTPUT
I – INPUT

custom programmed devices

The TMS 4100 JC series is programmed at the gate oxide stage of manufacturing. Programming charges are reduced to a minimum because only one mask per unique design need be created (gate oxide removal mask). All other processing steps remain the same for all devices. Options available to the customer during programming are:

- memory organization
- character format
- enable logic polarity (or permanently enabled)

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets are used. These encoding sheets (SOFTWARE PACKAGE) bulletins are available from the TI sales office.

standard devices

Because certain codes are widely used, TI has created a series of standard devices, which are available off the shelf and for which there is no coding charge. The most widely used standard device is:
TMS 4103 JC USASCII CODE (See attached character format).

Organization: 64-Character Storage
35-Bit Character Matrix
6 Parallel Character Address Input
Chip Enabled by Logic 1 Applied to I_7

Other Available Standard Circuits:

— TMS 4177 JC and 4178 JC. These two devices are used as a unit to implement a 7 x 10 row output character generator. The two devices are wired OR and are scanned in succession.

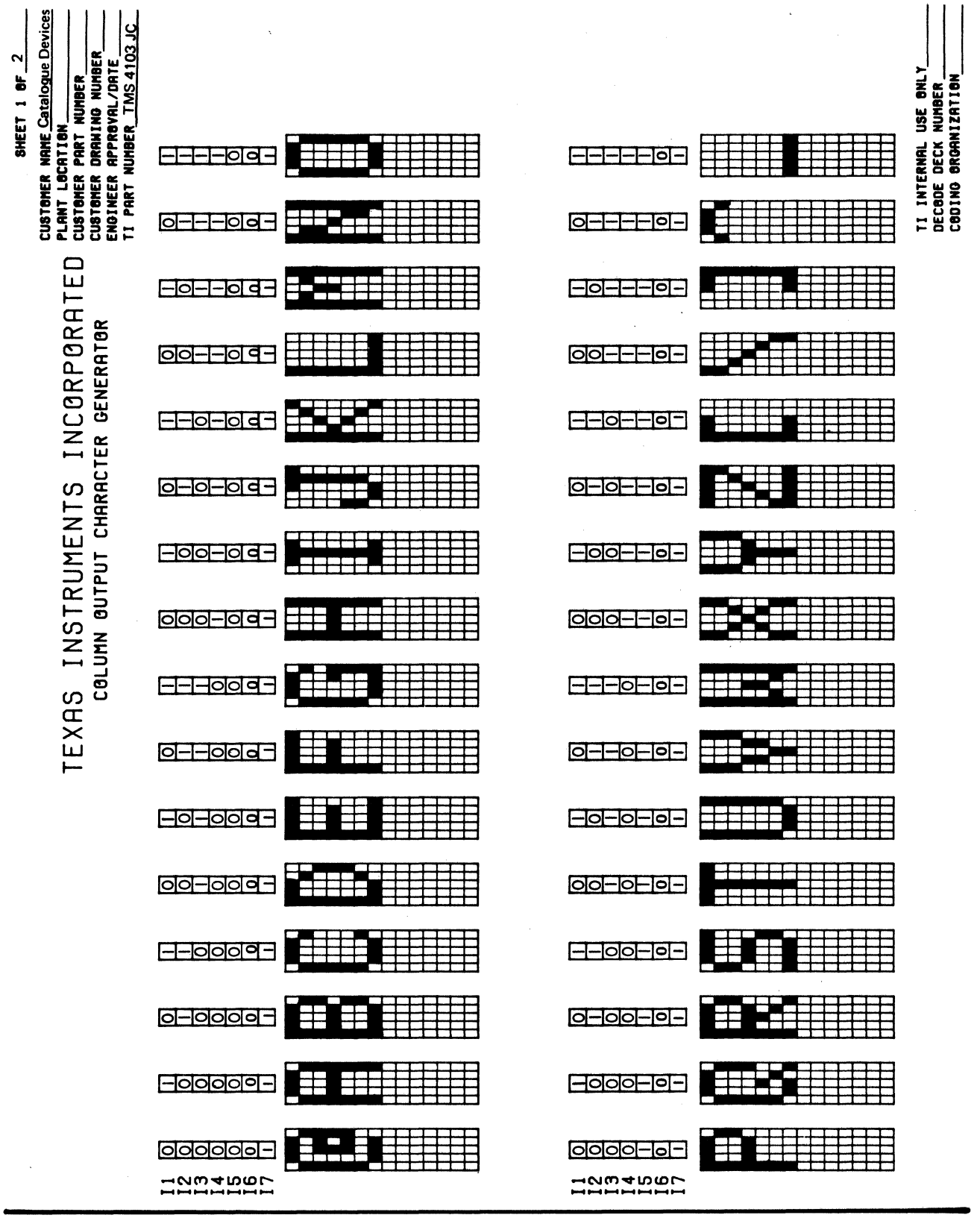
- USASCII Code
- 64 Character Storage
- 7 Bit Parallel Input

See attached character format.

— TMS 4179 JC.

- EBCDIC Code
- 64 Character Storage
- 7 Bit Parallel Input

See attached character format.


SHEET 1 OF 2
CUSTOMER NAME Catalogue Devices
PLANT LOCATION
CUSTOMER PART NUMBER
CUSTOMER DRAWING NUMBER
ENGINEER APPROVAL/DATE
TI PART NUMBER TMS4103JC
TEXAS INSTRUMENTS INCORPORATED
COLUMN OUTPUT CHARACTER GENERATOR
TI INTERNAL USE ONLY
DECODE DECK NUMBER
CODING ORGANIZATION
I1
I2
I3
I4
I5
I6
I7

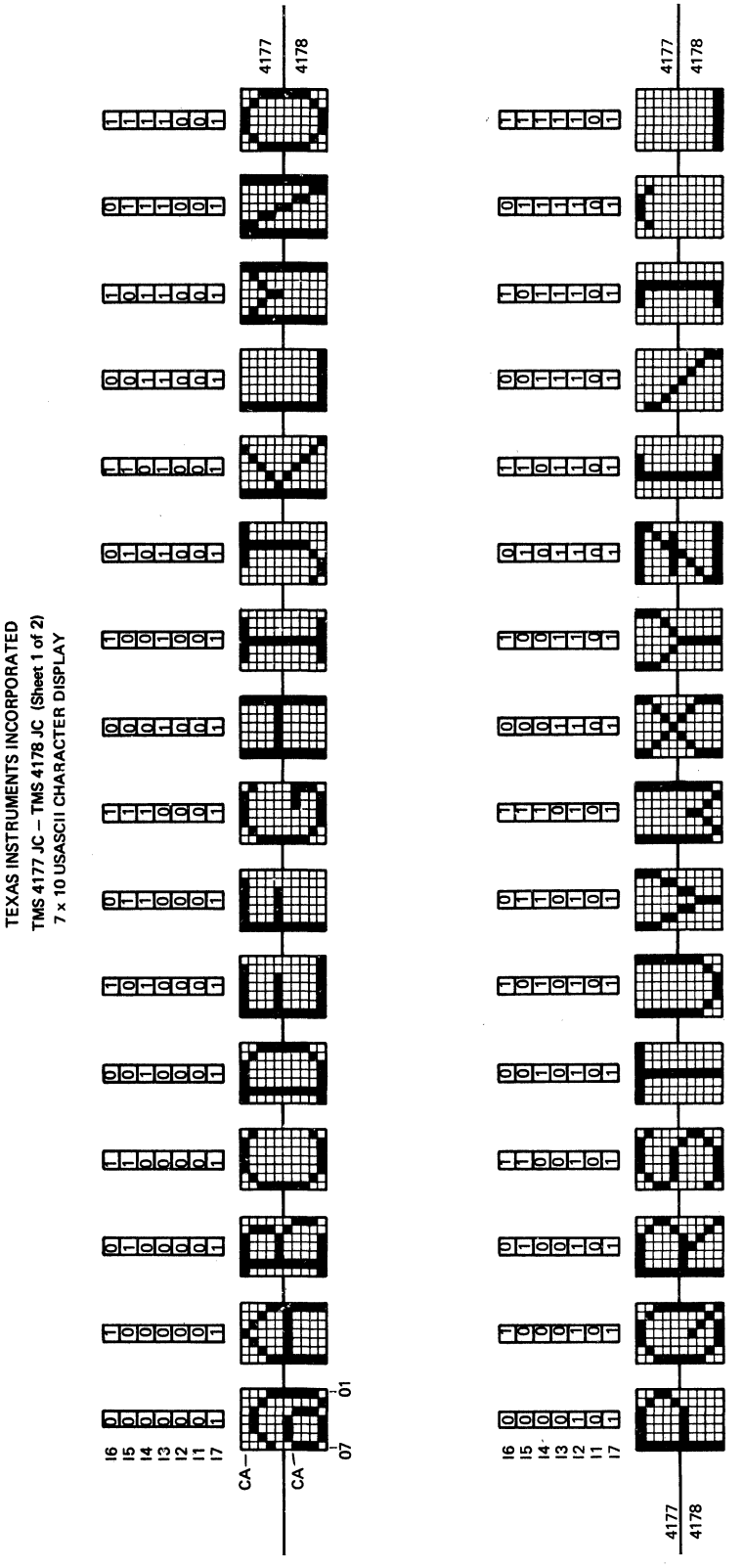
SHEET 2 OF 2

CUSTOMER NAME Catalogue Devices
PLANT LOCATION
CUSTOMER PART NUMBER
CUSTOMER DRAWING NUMBER
ENGINEER APPROVAL/DATE
TI PART NUMBER TMS 4103 JC

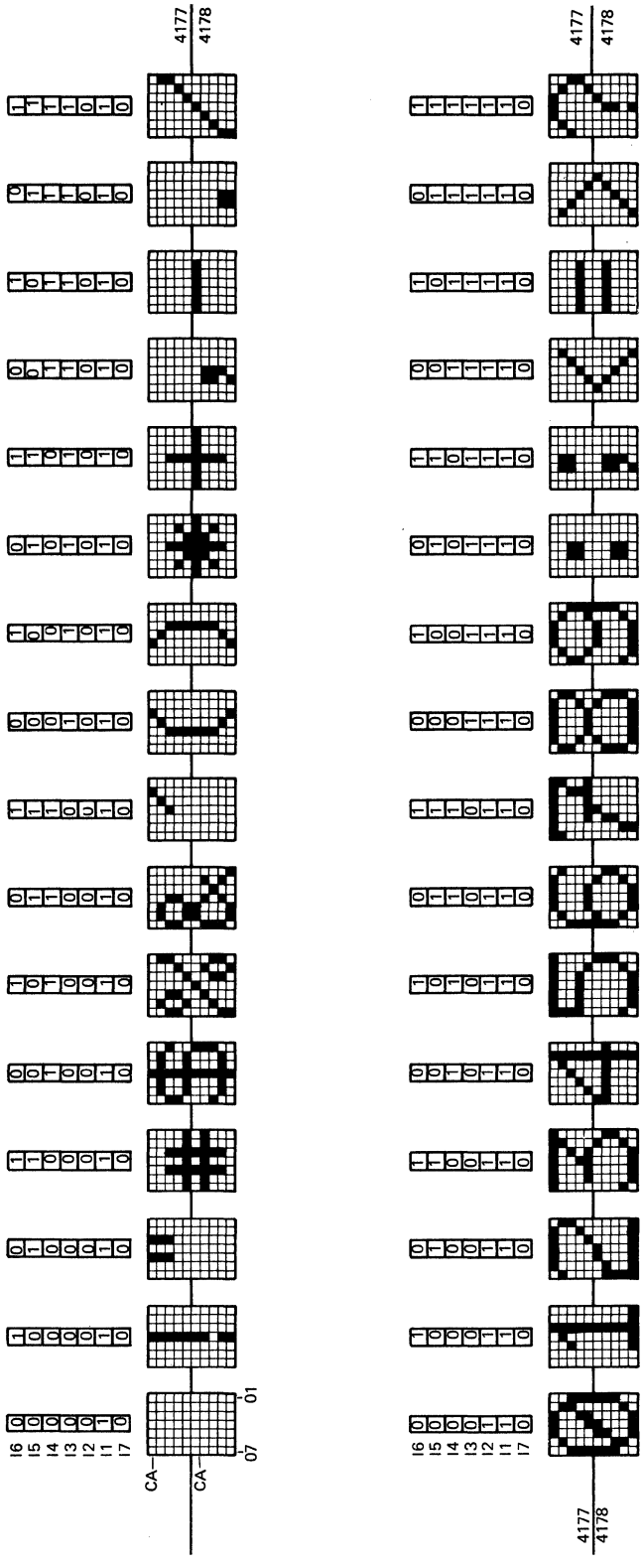
TEXAS INSTRUMENTS INCORPORATED

COLUMN OUTPUT CHARACTER GENERATOR

TI INTERNAL USE ONLY
DECODE DECK NUMBER
CODING ORGANIZATION


TEXAS INSTRUMENTS INCORPORATED
TMS 4177 JC – TMS 4178 JC (Sheet 1 of 2)
7 x 10 USASCII CHARACTER DISPLAY
4177
4178
I6
I5
I4
I3
I2
I1
I7
CA–
CA–
01
07
4177
4178

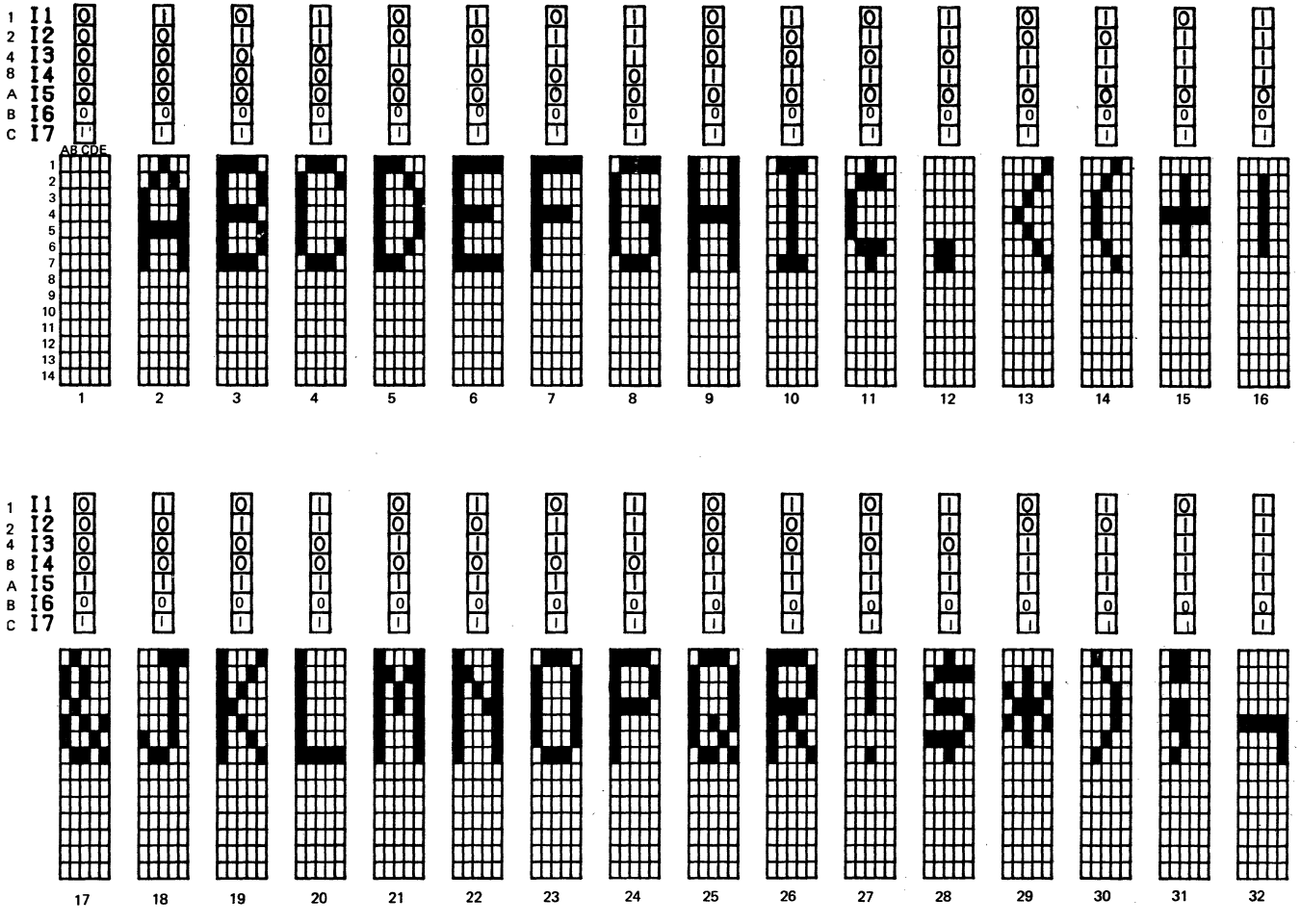
TEXAS INSTRUMENTS INCORPORATED
TMS 4177 JC – TMS 4178 JC (Sheet 2 of 2)
7 x 10 USASCII CHARACTER DISPLAY



TEXAS INSTRUMENTS INCORPORATED

MOS COLUMN OUTPUT CHARACTER GENERATOR - TMS 4100 JC SERIES

Coding Sheet 1 of 2



CUSTOMER TI CATALOG

CUSTOMER PART NO. CIRCUIT

Coding Symbols

1 – Most Negative Input
0 – Most Positive Input
X – Don't Care Condition

OPTIONS:

☐ 32 Characters – 5 x 14
I_6, Chip Enable:
1 ☐
0 ☐
(I_7 Must be X)

☐ 32 Characters – 5 x 13
I_6, Chip Enable:
1 ☐
0 ☐

☒ 64 Characters – 5 x 7
I_6 is 0, Coding Sheet No. 1
I_6 is 1, Coding Sheet No. 2
If I_7 is used as Chip Enable:
1 ☒
0 ☐
X ☐

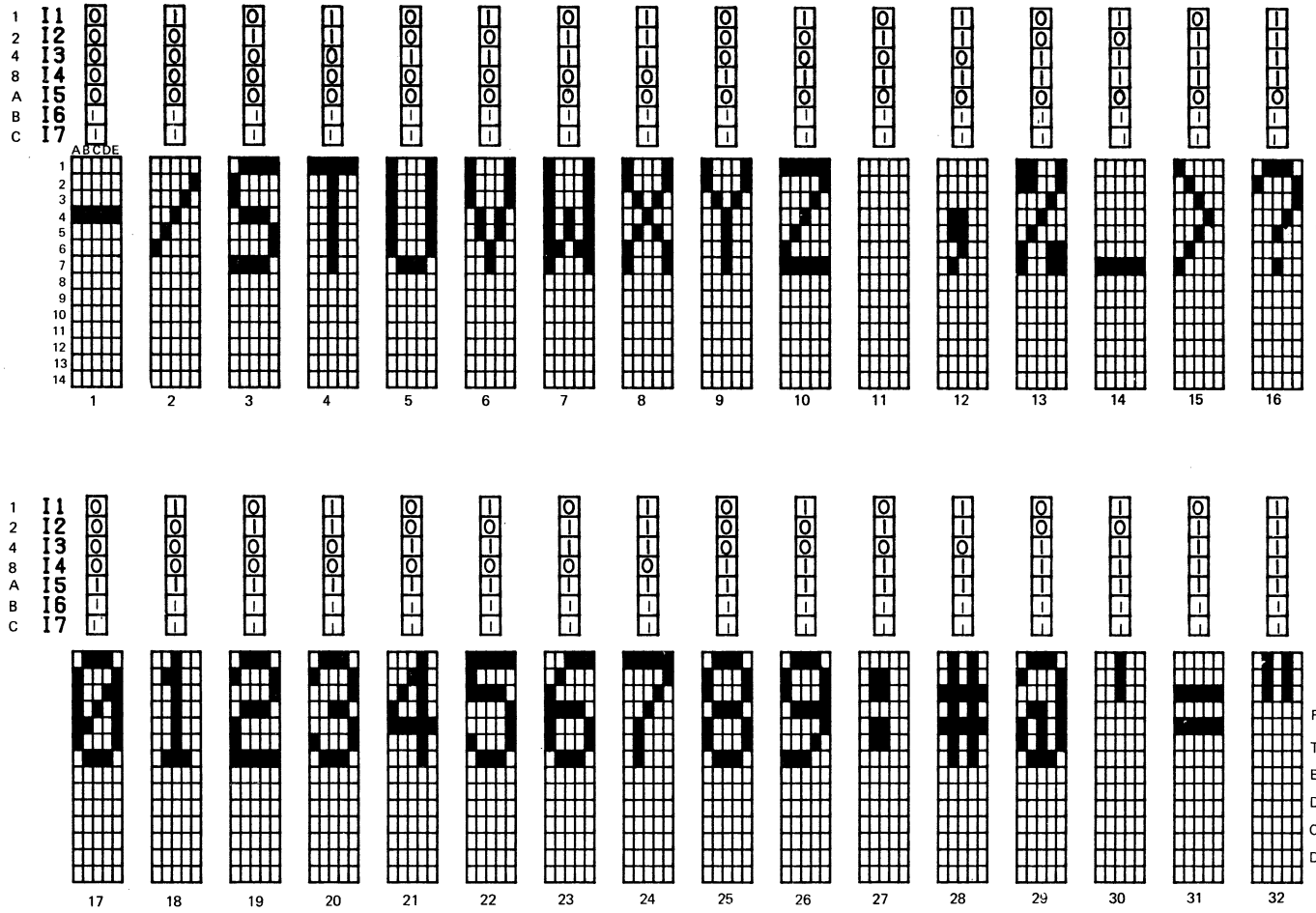
For TI Use Only:

TI Part No. TMS 4179 JC
Engineering Approval BJB
Decode Deck 3
Character Array 0.2
Decode Array 0.3

TEXAS INSTRUMENTS INCORPORATED

MOS COLUMN OUTPUT CHARACTER GENERATOR - TMS 4100 JC SERIES

Coding Sheet 2 of 2



CUSTOMER TI CATALOG

CUSTOMER PART NO. CIRCUIT

Coding Symbols

1 – Most Negative Input
0 – Most Positive Input
X – Don't Care Condition

OPTIONS:

☐ 32 Characters – 5 x 14
I_6, Chip Enable:
1 ☐
0 ☐
(I_7 Must be X)

☐ 32 Characters – 5 x 13
I_6, Chip Enable:
1 ☐
0 ☐

☒ 64 Characters – 5 x 7
I_6 is 0, Coding Sheet No. 1
I_6 is 1, Coding Sheet No. 2
If I_7 is used as Chip Enable:
1 ☒
0 ☐
X ☐

For TI Use Only:

TI Part No. TMS 4179 JC
Engineering Approval BJB
Decode Deck 3
Character Array 0.2
Decode Array 0.3

TMS4100JC series character generator

TMS4300JC
4096-bit static read-only memory
preliminary information

FEATURING

- **4096-Bit Capacity**
- **Static operation**
- **Access time less than 1 microseconds (single-ended buffer, TTL load)**
- **Four organizations available**
- **Open-drain output buffers or double ended buffers**
- **TTL compatible**

description

The TMS 4300 JC series is a family of static read-only memories with a capacity of 4096 bits. Four memory organizations and 2 output buffer configurations are provided through single-level mask programming.

The memory may be organized as 4096 words of one bit, 2048 words of two bits, 1024 words of four bits, or 512 words of eight bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground.

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

The chip select may be programmed for either logic 1 or logic 0 operation. Depending on the organization, select inputs I_9, I_{10} and I_{11} can also be used as chip select inputs. The SOFTWARE PACKAGE describes each specific case.

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage.

operation

The TMS 4300 JC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged.

"Access time" is defined as the maximum time required for all outputs to reach the minimum logic 1 levels or maximum logic 0 levels with the correct data. This time is measured from that point in time at which all address inputs and chip-select inputs are valid.

A disable input on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

data encoding

The data to be stored in the memory must be submitted to TI on computer-punched cards.

Information concerning chip organization, type of output buffer, and chip select must be submitted to TI on a standard form.

A SOFTWARE PACKAGE available from TI describes both documents.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Data input voltage ranges (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1. These voltage values are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−16	V
Supply voltage V_{GG}	−22	−28	−29	V
Input, chip select logic 1	−9	−14	−16	V
Input, chip select logic 0	+0.3	0	−3	V
Address pulse width V_{DD} = −14 V, V_{GG} = −28 V	500			ns
Address pulse width V_{DD} = −12 V, V_{GG} = −24 V	550			ns
Chip select pulse width V_{DD} = −14 V, V_{GG} = −28 V	150			ns
Chip select pulse width V_{DD} = −12 V, V_{GG} = −24 V	200			ns

Maximum speed of operation will be obtained when operating at nominal conditions. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(1)}$	Logic 1 output current (Note 1)	−14 V applied to output			10	μA
$I_{out(0)}$	Logic 0 output current (Note 1)	−14 V applied to output	3	7.5		mA
$I_{out(0)}$	Logic 0 output current (Note 1)	V_{DD} = 12 V, V_{GG} = −24 V, −12 V applied to output	3	5.5		mA
$V_{(0)}$	Logic 0 output voltage (Note 1)	I_O = 0.5 mA		−0.25	−0.6	V
V_O	Logic 0 output voltage (Note 1)	I_O = 1 mA		−0.5	−1	V
V_O	Logic 0 output voltage (Note 1)	I_O = 2 mA		−1.1	−2	V
$V_{out(1)}$	Logic 1 output voltage (Note 2)	R_L = 1 MΩ	−11		−14	V
$V_{out(0)}$	Logic 0 output voltage (Notes 2 & 3)	R_L = 1 MΩ	0		−2.0	V
	Power dissipation			250		mW
I_L	Input leakage current	−14 V applied to input			1	μA
	Input capacitance	f = 140 kHz		8.5		pF
	Chip select input capacitance	f = 140 kHz		3.5		pF
I_{DD}	Drain current			10	25	mA
I_{GG}	Gate current			0.5	1	mA

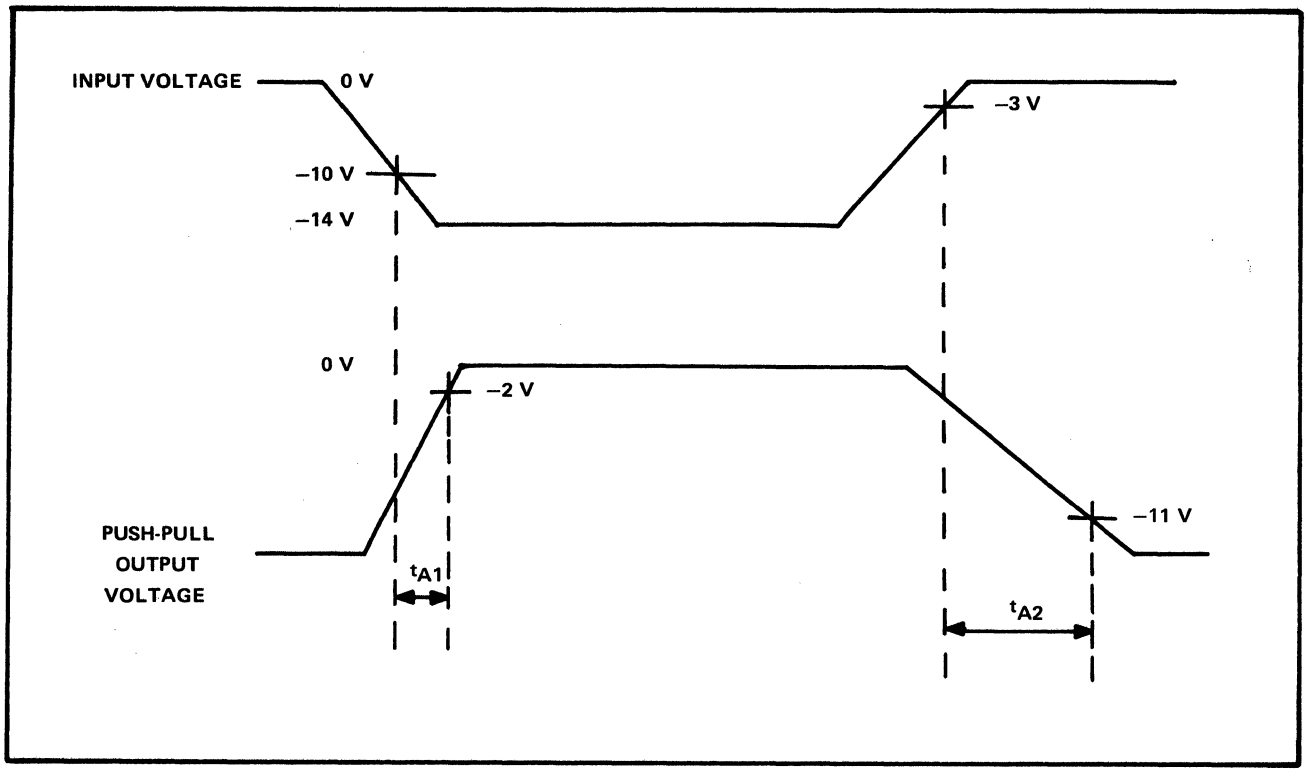
NOTES: 1. Open-drain buffer
2. Push-pull buffer
3. For 2048 x 2 or 4096 x 1, minimum voltage is 3.0 V.
4. All voltages are with respect to V_{SS}.

dynamic electrical characteristics (under nominal operating conditions and at 25°C unless otherwise noted)

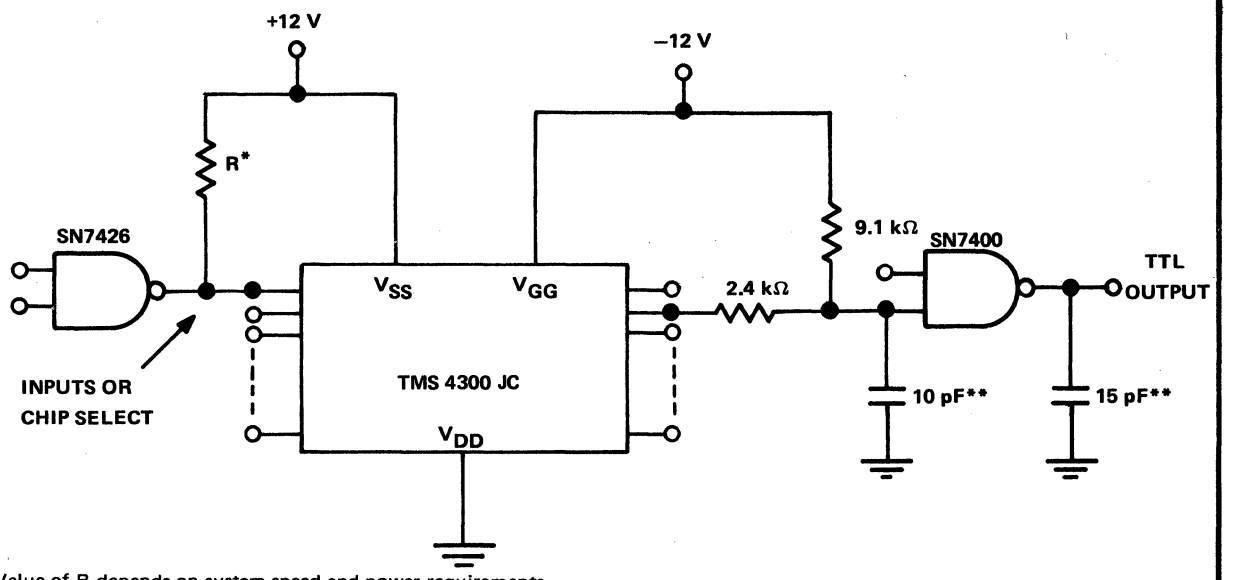
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{A1}	Access time TTL load	V_{SS} = +14 V, V_{DD} = 0 V, V_{GG} = −14 V		500	900	ns
	(See Notes 1 & 2)	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		600	950	ns
t_{A2}	Access time TTL load	V_{SS} = +14 V, V_{DD} = 0 V, V_{GG} = −14 V		450	900	ns
	(See Notes 1 & 2)	V_{SS} = V_{DD} = 0 V, V_{GG} = −12 V		550	950	ns
t_d	Access time RC load	V_{SS} = 0 V, V_{DD} = −14 V, V_{GG} = −28 V		600	900	ns
	(See Notes 1 & 2)	V_{SS} = 0 V, V_{DD} = −12 V, V_{GG} = −24 V		700	950	ns
t_f	Fall time RC load	V_{SS} = 0 V, V_{DD} = −14 V, V_{GG} = −28 V		200	400	ns
	(See Notes 1 & 2)	V_{SS} = 0 V, V_{DD} = −12 V, V_{GG} = −24 V		250	450	ns
t_{A1}	Access time (Notes 2 & 3)			0.8	2	μs
t_{A2}	Access time (Notes 2 & 3)			1.4	2	μs

NOTES: 1. Open ended buffer
2. See Switching Diagram
3. Push-pull buffer R_L = 17 kΩ C = 20 pF

switching diagram double ended buffer



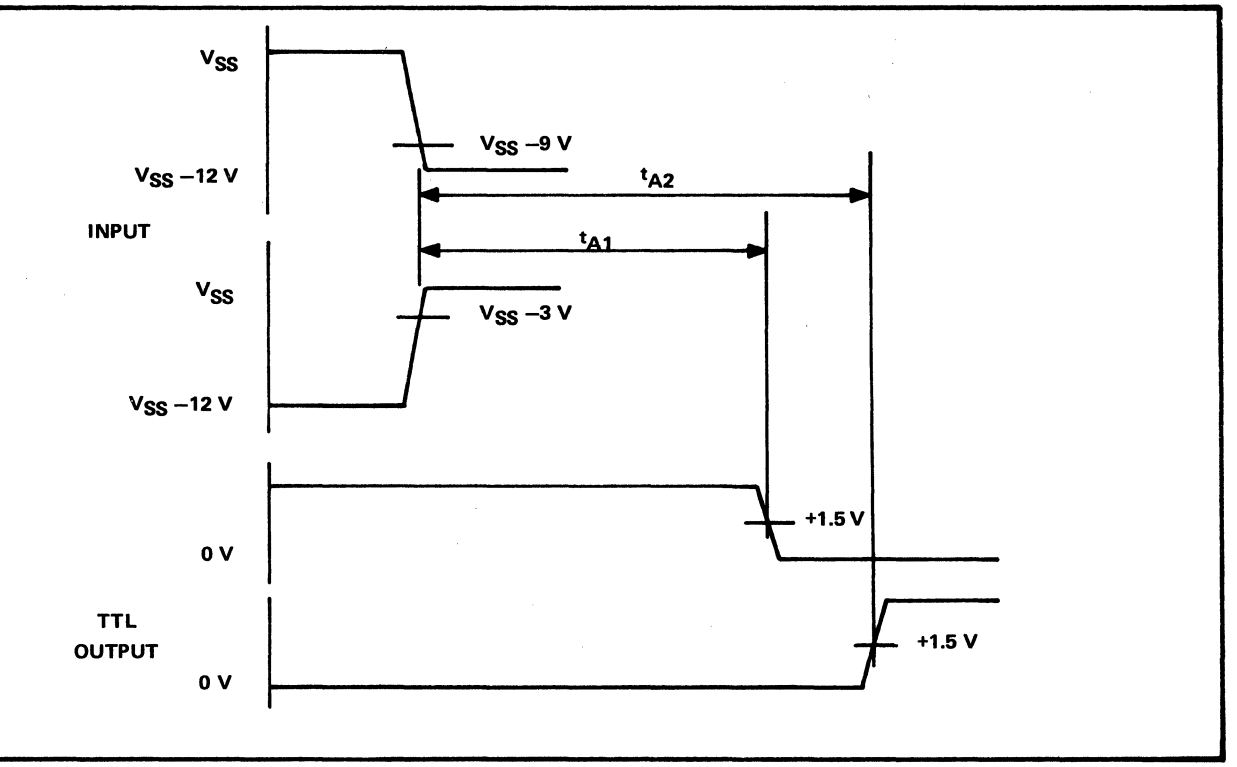
switching circuit (TTL load) and typical TTL interface (single-ended buffer)



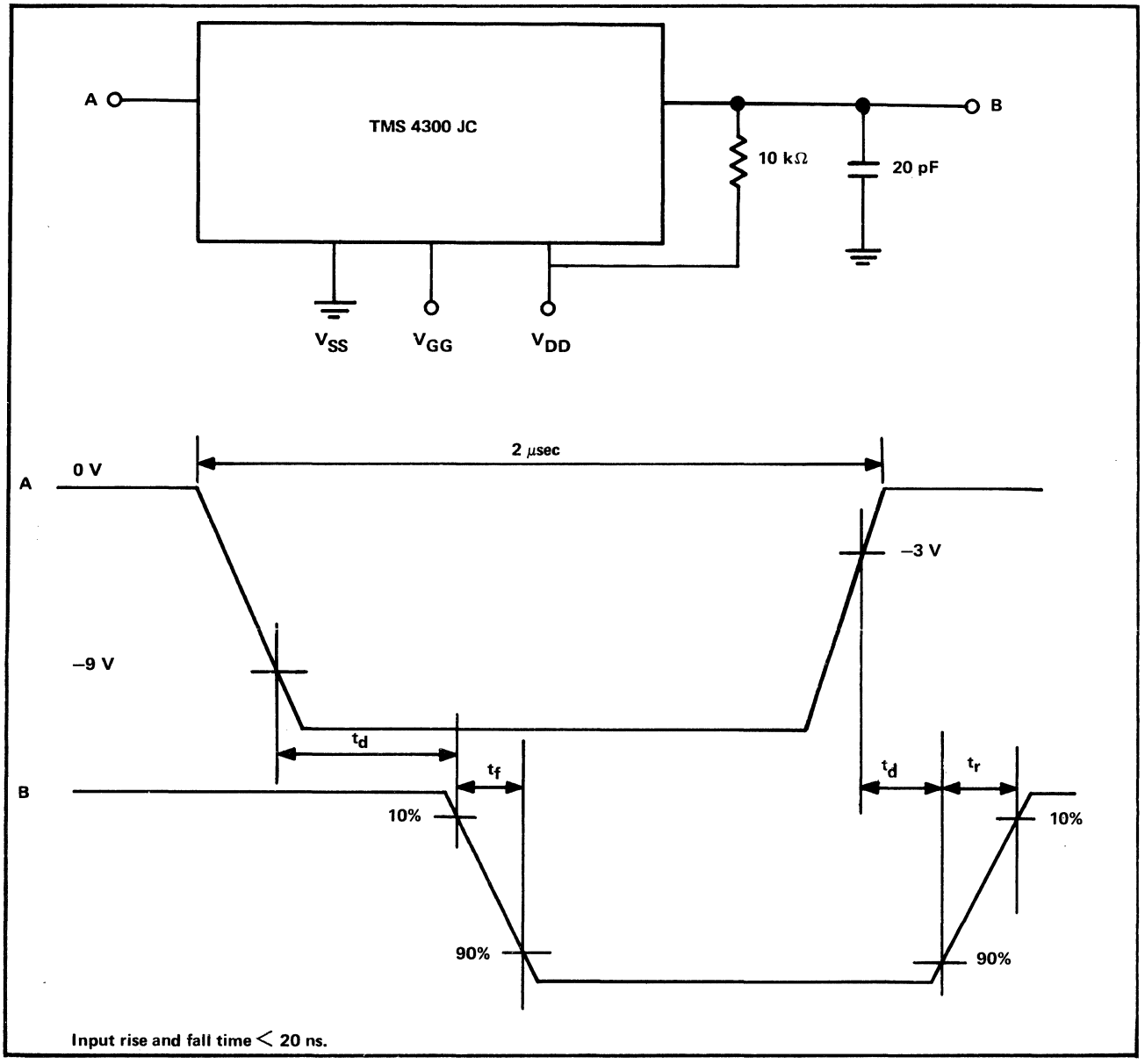
* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

switching diagram (TTL load)



switching diagram and parametric measurement information RC load (single-ended buffer)



mechanical data

The TMS 4300 JC is mounted in a 24-pin hermetically sealed dual-in-line package consisting of gold-plated metal, ceramic sandwich body, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

TMS4300JC
4096-bit static read-only memory

pin configuration

Depending on the organization of the memory, four pin configurations may be used:

PIN NO.	CHIP ORGANIZATION			
	512 x 8	1024 x 4	2048 x 2	4096 x 1
1	I_1	I_1	I_1	I_1
2	I_0	I_0	I_0	I_0
3	CE	CE	CE	CE
4	I_{11}	I_{11}	I_{11}	I_{11}
5	I_{10}	I_{10}	I_{10}	I_{10}
6	I_9	I_9	I_9	I_9
7	V_{GG}	V_{GG}	V_{GG}	V_{GG}
8	V_{DD}	V_{DD}	V_{DD}	V_{DD}
9	O_8	NC	NC	NC
10	O_7	NC	NC	NC
11	O_6	O_4	NC	NC
12	O_5	O_3	O_2	NC
13	O_4	O_2	NC	O_1
14	O_3	O_1	O_1	NC
15	O_2	NC	NC	NC
16	O_1	NC	NC	NC
17	V_{SS}	V_{SS}	V_{SS}	V_{SS}
18	I_8	I_8	I_8	I_8
19	I_7	I_7	I_7	I_7
20	I_6	I_6	I_6	I_6
21	I_5	I_5	I_5	I_5
22	I_4	I_4	I_4	I_4
23	I_3	I_3	I_3	I_3
24	I_2	I_2	I_2	I_2

I INPUT
O OUTPUT
NC NOT CONNECTED

off-the-shelf devices

For demonstrating the operation of the TMS 4300 JC series, two standard catalog parts are available:

TMS 4305 JC – this device is organized as 512 words x 8 bits and has a single-ended output buffer. The memory is programmed with a sine table.

The 0 – 90° arc is divided into 512 arcs and the value is given in binary form on the eight outputs.

TMS 4306 JC – This device is identical to the TMS 4305 JC, except for the output buffer, which is of the push-pull variety.

truth table, TMS 4305 JC (sheet 1 of 2)

INPUT ADDRESS	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	0
4	0	0	0	0	0	0	1	1
5	0	0	0	0	0	1	0	0
6	0	0	0	0	0	1	0	1
7	0	0	0	0	0	1	0	1
8	0	0	0	0	0	1	1	0
9	0	0	0	0	0	1	1	1
10	0	0	0	0	1	0	0	0
11	0	0	0	0	1	0	0	1
12	0	0	0	0	1	0	0	1
13	0	0	0	0	1	0	1	0
14	0	0	0	0	1	0	1	1
15	0	0	0	0	1	1	0	0
16	0	0	0	0	1	1	0	1
17	0	0	0	0	1	1	0	1
18	0	0	0	0	1	1	1	0
19	0	0	0	0	1	1	1	1
20	0	0	0	1	0	0	0	0
21	0	0	0	1	0	0	0	0
22	0	0	0	1	0	0	0	1
23	0	0	0	1	0	0	1	0
24	0	0	0	1	0	0	1	1
25	0	0	0	1	0	1	0	0
26	0	0	0	1	0	1	0	0
27	0	0	0	1	0	1	0	1
28	0	0	0	1	0	1	1	0
29	0	0	0	1	0	1	1	1
30	0	0	0	1	1	0	0	0
31	0	0	0	1	1	0	0	0
32	0	0	0	1	1	0	0	1
33	0	0	0	1	1	0	1	0
34	0	0	0	1	1	0	1	1
35	0	0	0	1	1	0	1	1
36	0	0	0	1	1	1	0	0
37	0	0	0	1	1	1	0	1
38	0	0	0	1	1	1	1	0
39	0	0	0	1	1	1	1	1
40	0	0	0	1	1	1	1	1
41	0	0	1	0	0	0	0	0
42	0	0	1	0	0	0	0	1
43	0	0	1	0	0	0	1	0
44	0	0	1	0	0	0	1	0
45	0	0	1	0	0	0	1	1
46	0	0	1	0	0	1	0	0
47	0	0	1	0	0	1	0	1
48	0	0	1	0	0	1	1	0
49	0	0	1	0	0	1	1	0
50	0	0	1	0	0	1	1	1
51	0	0	1	0	1	0	0	0
52	0	0	1	0	1	0	0	1
53	0	0	1	0	1	0	0	1
54	0	0	1	0	1	0	1	0
55	0	0	1	0	1	0	1	1
56	0	0	1	0	1	1	0	0
57	0	0	1	0	1	1	0	1
58	0	0	1	0	1	1	0	1
59	0	0	1	0	1	1	1	0
60	0	0	1	0	1	1	1	1
61	0	0	1	1	0	0	0	0
62	0	0	1	1	0	0	0	0
63	0	0	1	1	0	0	0	1
64	0	0	1	1	0	0	1	0
65	0	0	1	1	0	0	1	1
66	0	0	1	1	0	0	1	1
67	0	0	1	1	0	1	0	0
68	0	0	1	1	0	1	0	1
69	0	0	1	1	0	1	1	0
70	0	0	1	1	0	1	1	1
71	0	0	1	1	0	1	1	1
72	0	0	1	1	1	0	0	0
73	0	0	1	1	1	0	0	1
74	0	0	1	1	1	0	1	0
75	0	0	1	1	1	0	1	0
76	0	0	1	1	1	0	1	1
77	0	0	1	1	1	1	0	0
78	0	0	1	1	1	1	0	1
79	0	0	1	1	1	1	0	1
80	0	0	1	1	1	1	1	0
81	0	0	1	1	1	1	1	1
82	0	1	0	0	0	0	0	0
83	0	1	0	0	0	0	0	0
84	0	1	0	0	0	0	0	1
85	0	1	0	0	0	0	1	0
86	0	1	0	0	0	0	1	1
87	0	1	0	0	0	1	0	0
88	0	1	0	0	0	1	0	0
89	0	1	0	0	0	1	0	1
90	0	1	0	0	0	1	1	0
91	0	1	0	0	0	1	1	1
92	0	1	0	0	0	1	1	1
93	0	1	0	0	1	0	0	0
94	0	1	0	0	1	0	0	1
95	0	1	0	0	1	0	1	0
96	0	1	0	0	1	0	1	0
97	0	1	0	0	1	0	1	1
98	0	1	0	0	1	1	0	0
99	0	1	0	0	1	1	0	1
100	0	1	0	0	1	1	0	1
101	0	1	0	0	1	1	1	0
102	0	1	0	0	1	1	1	1
103	0	1	0	1	0	0	0	0
104	0	1	0	1	0	0	0	0
105	0	1	0	1	0	0	0	1
106	0	1	0	1	0	0	1	0
107	0	1	0	1	0	0	1	1
108	0	1	0	1	0	0	1	1
109	0	1	0	1	0	1	0	0
110	0	1	0	1	0	1	0	1
111	0	1	0	1	0	1	1	0
112	0	1	0	1	0	1	1	0
113	0	1	0	1	0	1	1	1
114	0	1	0	1	1	0	0	0
115	0	1	0	1	1	0	0	0
116	0	1	0	1	1	0	0	1
117	0	1	0	1	1	0	1	0
118	0	1	0	1	1	0	1	1
119	0	1	0	1	1	0	1	1
120	0	1	0	1	1	1	0	0
121	0	1	0	1	1	1	0	1
122	0	1	0	1	1	1	1	0
123	0	1	0	1	1	1	1	0
124	0	1	0	1	1	1	1	1
125	0	1	1	0	0	0	0	0
126	0	1	1	0	0	0	0	1
127	0	1	1	0	0	0	0	1
128	0	1	1	0	0	0	1	0
129	0	1	1	0	0	0	1	1
130	0	1	1	0	0	0	1	1
131	0	1	1	0	0	1	0	0
132	0	1	1	0	0	1	0	1
133	0	1	1	0	0	1	1	0
134	0	1	1	0	0	1	1	0
135	0	1	1	0	0	1	1	1
136	0	1	1	0	1	0	0	0
137	0	1	1	0	1	0	0	0
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139	0	1	1	0	1	0	1	0
140	0	1	1	0	1	0	1	1
141	0	1	1	0	1	0	1	1
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145	0	1	1	0	1	1	1	0
146	0	1	1	0	1	1	1	1
147	0	1	1	1	0	0	0	0
148	0	1	1	1	0	0	0	0
149	0	1	1	1	0	0	0	1
150	0	1	1	1	0	0	1	0
151	0	1	1	1	0	0	1	0
152	0	1	1	1	0	0	1	1
153	0	1	1	1	0	1	0	0
154	0	1	1	1	0	1	0	1
155	0	1	1	1	0	1	0	1
156	0	1	1	1	0	1	1	0
157	0	1	1	1	0	1	1	1
158	0	1	1	1	0	1	1	1
159	0	1	1	1	1	0	0	0
160	0	1	1	1	1	0	0	1
161	0	1	1	1	1	0	0	1
162	0	1	1	1	1	0	1	0
163	0	1	1	1	1	0	1	1
164	0	1	1	1	1	0	1	1
165	0	1	1	1	1	1	0	0
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167	0	1	1	1	1	1	0	1
168	0	1	1	1	1	1	1	0
169	0	1	1	1	1	1	1	1
170	1	0	0	0	0	0	0	0
171	1	0	0	0	0	0	0	0
172	1	0	0	0	0	0	0	1
173	1	0	0	0	0	0	1	0
174	1	0	0	0	0	0	1	0
175	1	0	0	0	0	0	1	1
176	1	0	0	0	0	1	0	0
177	1	0	0	0	0	1	0	0
178	1	0	0	0	0	1	0	1
179	1	0	0	0	0	1	1	0
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183	1	0	0	0	1	0	0	0
184	1	0	0	0	1	0	0	1
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186	1	0	0	0	1	0	1	0
187	1	0	0	0	1	0	1	1
188	1	0	0	0	1	1	0	0
189	1	0	0	0	1	1	0	0
190	1	0	0	0	1	1	0	1
191	1	0	0	0	1	1	1	0
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195	1	0	0	1	0	0	0	0
196	1	0	0	1	0	0	0	1
197	1	0	0	1	0	0	0	1
198	1	0	0	1	0	0	1	0
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201	1	0	0	1	0	1	0	0
202	1	0	0	1	0	1	0	1
203	1	0	0	1	0	1	0	1
204	1	0	0	1	0	1	1	0
205	1	0	0	1	0	1	1	1
206	1	0	0	1	0	1	1	1
207	1	0	0	1	1	0	0	0
208	1	0	0	1	1	0	0	0
209	1	0	0	1	1	0	0	1
210	1	0	0	1	1	0	1	0
211	1	0	0	1	1	0	1	0
212	1	0	0	1	1	0	1	1
213	1	0	0	1	1	1	0	0
214	1	0	0	1	1	1	0	0
215	1	0	0	1	1	1	0	1
216	1	0	0	1	1	1	0	1
217	1	0	0	1	1	1	1	0
218	1	0	0	1	1	1	1	1
219	1	0	0	1	1	1	1	1
220	1	0	1	0	0	0	0	0
221	1	0	1	0	0	0	0	1
222	1	0	1	0	0	0	0	1
223	1	0	1	0	0	0	1	0
224	1	0	1	0	0	0	1	0
225	1	0	1	0	0	0	1	1
226	1	0	1	0	0	1	0	0
227	1	0	1	0	0	1	0	0
228	1	0	1	0	0	1	0	1
229	1	0	1	0	0	1	0	1
230	1	0	1	0	0	1	1	0
231	1	0	1	0	0	1	1	1
232	1	0	1	0	0	1	1	1
233	1	0	1	0	1	0	0	0
234	1	0	1	0	1	0	0	0
235	1	0	1	0	1	0	0	1
236	1	0	1	0	1	0	1	0
237	1	0	1	0	1	0	1	0
238	1	0	1	0	1	0	1	1
239	1	0	1	0	1	0	1	1
240	1	0	1	0	1	1	0	0
241	1	0	1	0	1	1	0	1
242	1	0	1	0	1	1	0	1
243	1	0	1	0	1	1	1	0
244	1	0	1	0	1	1	1	0
245	1	0	1	0	1	1	1	1
246	1	0	1	0	1	1	1	1
247	1	0	1	1	0	0	0	0
248	1	0	1	1	0	0	0	1
249	1	0	1	1	0	0	0	1
250	1	0	1	1	0	0	1	0
251	1	0	1	1	0	0	1	0
252	1	0	1	1	0	0	1	1
253	1	0	1	1	0	0	1	1
254	1	0	1	1	0	1	0	0
255	1	0	1	1	0	1	0	0

TMS4300JC
4096-bit static read-only memory

truth table, TMS 4305 JC (sheet 2 of 2)

INPUT ADDRESS	0_1	0_2	0_3	0_4	0_5	0_6	0_7	0_8
256	1	0	1	1	0	1	0	1
257	1	0	1	1	0	1	1	0
258	1	0	1	1	0	1	1	0
259	1	0	1	1	0	1	1	1
260	1	0	1	1	0	1	1	1
261	1	0	1	1	1	0	0	0
262	1	0	1	1	1	0	0	0
263	1	0	1	1	1	0	0	1
264	1	0	1	1	1	0	0	1
265	1	0	1	1	1	0	1	0
266	1	0	1	1	1	0	1	0
267	1	0	1	1	1	0	1	1
268	1	0	1	1	1	1	0	0
269	1	0	1	1	1	1	0	0
270	1	0	1	1	1	1	0	1
271	1	0	1	1	1	1	0	1
272	1	0	1	1	1	1	1	0
273	1	0	1	1	1	1	1	0
274	1	0	1	1	1	1	1	1
275	1	0	1	1	1	1	1	1
276	1	1	0	0	0	0	0	0
277	1	1	0	0	0	0	0	0
278	1	1	0	0	0	0	0	1
279	1	1	0	0	0	0	0	1
280	1	1	0	0	0	0	1	0
281	1	1	0	0	0	0	1	0
282	1	1	0	0	0	0	1	1
283	1	1	0	0	0	0	1	1
284	1	1	0	0	0	1	0	0
285	1	1	0	0	0	1	0	0
286	1	1	0	0	0	1	0	1
287	1	1	0	0	0	1	0	1
288	1	1	0	0	0	1	1	0
289	1	1	0	0	0	1	1	0
290	1	1	0	0	0	1	1	1
291	1	1	0	0	0	1	1	1
292	1	1	0	0	1	0	0	0
293	1	1	0	0	1	0	0	0
294	1	1	0	0	1	0	0	1
295	1	1	0	0	1	0	0	1
296	1	1	0	0	1	0	1	0
297	1	1	0	0	1	0	1	0
298	1	1	0	0	1	0	1	1
299	1	1	0	0	1	0	1	1
300	1	1	0	0	1	1	0	0
301	1	1	0	0	1	1	0	0
302	1	1	0	0	1	1	0	1
303	1	1	0	0	1	1	0	1
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TMS4500JC,TMS4600JC,TMS4700JC
2048-bit high speed static read only memories

preliminary information

FEATURING

- Low threshold technology
- Static operation
- Access time under 60 ns
- Open drain outputs
- Low power dissipation
- 128 words of 16 bits TMS 4500 JC
- 256 words of 8 bits TMS 4600 JC
- 512 words of 4 bits TMS 4700 JC

description

The TMS 4500 JC, TMS 4600 JC, and TMS 4700 JC series are groups of high-speed read-only-memory integrated circuits constructed on a single monolithic chip with MOS P-channel enhancement-mode transistors. The memory content is specified by the customer and is permanently programmed on the chip during the manufacturing process. Access times typically less than fifty nanoseconds are possible. High speed is obtained by using TTL or equivalent logic for decoding inputs and sensing outputs.

application

The primary function of the TMS 4500 JC, TMS 4600 JC, and TMS 4700 JC ROMS is to provide a fast access time non-destructive readout memory for systems with limited space and low power consumption requirements.

device operation notes

The circuit designer has considerable control over output levels of the device. Output logic 1 levels spanning almost three decades of voltage may be obtained with the proper selection of V_{DD}, V_{in} and R_L. V_{DD} is applied to the device outputs through external load resistors with an ouput voltage swing being developed across the external load. Although output voltage levels may be increased by increasing R_L, propagation time through the device is also increased. The circuit designer must therefore decide what trade-offs will be made with respect to access time and output voltage swing.

The TMS 4500 JC has a 16-lead input section that is capable of decoding 128 valid input address codes. The input section is divided into three subgroups B, C, and D. Sections B and C have four inputs and Section D has eight inputs.

device operation notes (continued)

The TMS 4600 JC has an 18-lead input section that is capable of decoding 256 valid input address codes. The input section is divided into four subgroups, A, B, C, and D. Section A has two inputs. Sections B and C each have four inputs and Section D has eight inputs.

The TMS 4700 JC has a 20-lead input section that is capable of decoding 512 valid input address codes. The input section is divided into four subgroups, A, B, C, and D. Section A has four inputs. Sections B and C each have four inputs and Section D has eight inputs.

Only one input lead in each of the input sections may be at a logic 1 level at any given time. All other inputs must be at a logic 0 level. *The circuit has negative logic inputs and positive logic outputs.*

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note) . . . . . −22 V to +0.3 V
Data input voltage V_{in} range (See Note) . . . . . −22 V to +0.3 V
Operating free-air temperature T_A range . . . . . −25°C to +85°C
Storage temperature T_S range . . . . . −55°C to +150°C

NOTE: These voltage values are with respect to V_{SS}.

recommended operating conditions

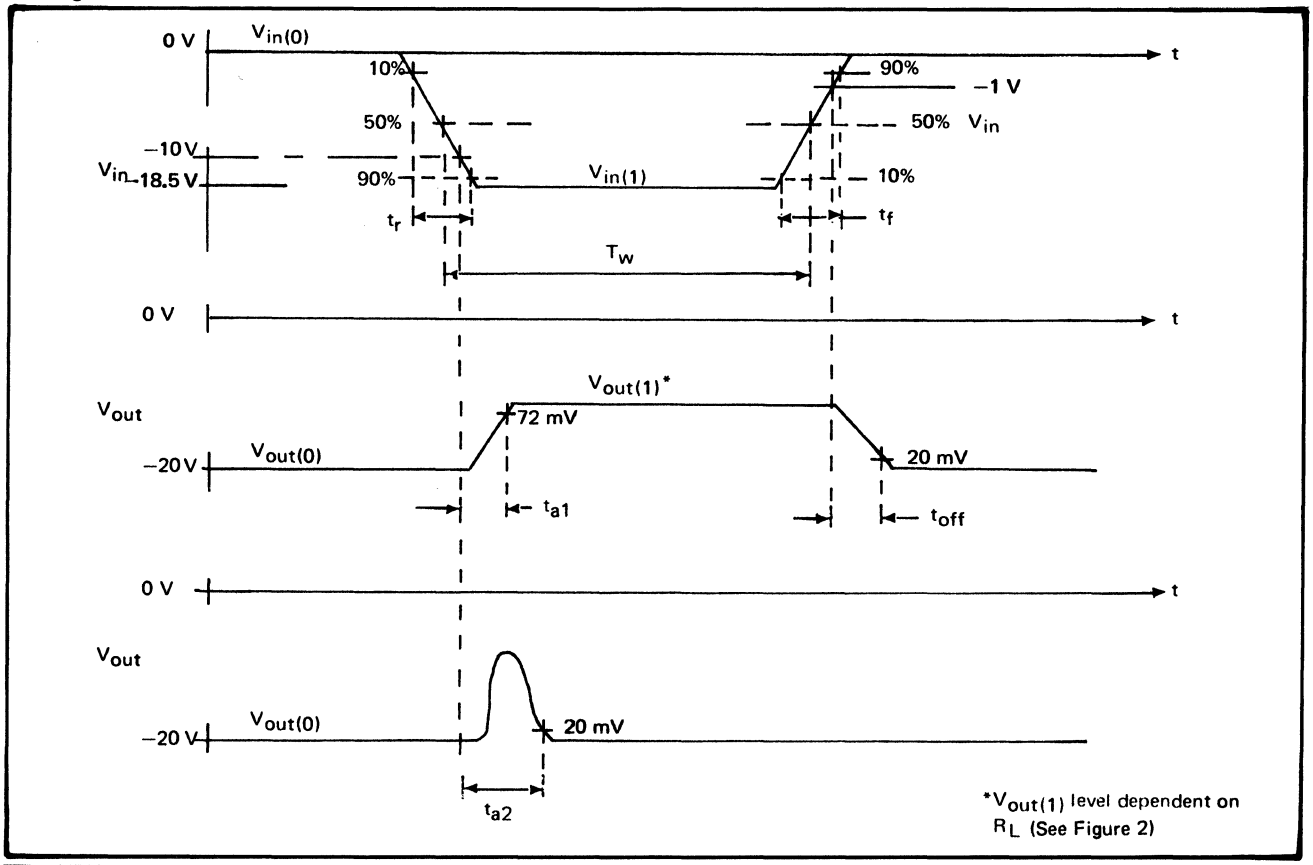
	CHARACTERISTICS	MIN	NOM	MAX	UNITS
V_{DD}	Supply voltage	−11	−20	−21	V
$V_{in(1)}$	Voltage required to ensure a logic 1 at any input	−10	−18.5	−21	V
$V_{in(0)}$	Voltage required to ensure a logic 0 at any input	+0.3	0	−1.0	V
t_r	Input voltage rise time (10% – 90%)	10	20		ns
t_f	Input voltage fall time (90% – 10%)	10	20		ns
R_L	Load Resistance	100	250		Ω

electrical characteristics, at nominal operating conditions and 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{out(1)}$	Logic 1 output voltage developed across R_L WRT V_{DD}	R_L = 250 Ω, V_{DD} = −20 V, $V_{in(1)}$ = −18.5 V	80	100		mV
$V_{out(0)}$	Logic 0 output voltage developed across R_L WRT V_{DD}	R_L = 250 Ω, V_{DD} = −20 V, $V_{in(1)}$ = −18.5 V		0		mV
t_{a1}	Access time to a 1 level	See Voltage Waveforms		25	50	ns
t_{a2}	Access time to a 0 level	See Voltage Waveforms		30	55	ns
t_{off}	Turn-off time from a 1 level to a 0	See Voltage Waveforms		30	50	ns
T_W	Width of data pulse	R_L = 250 Ω, See Voltage Waveforms	110	300		ns
C_{out}	Output capacitance to ground	Any output lead			8.0	pF
$C_{in(A)}$	Input capacitance to ground*	Any input lead — Section A			12.0	pF
$C_{in(B)}$	Input capacitance to ground	Any input lead — Section B			14.8	pF
$C_{in(C)}$	Input capacitance to ground	Any input lead — Section C			16.0	pF
$C_{in(d)}$	Input capacitance to ground	Any input lead — Section D			22.0	pF

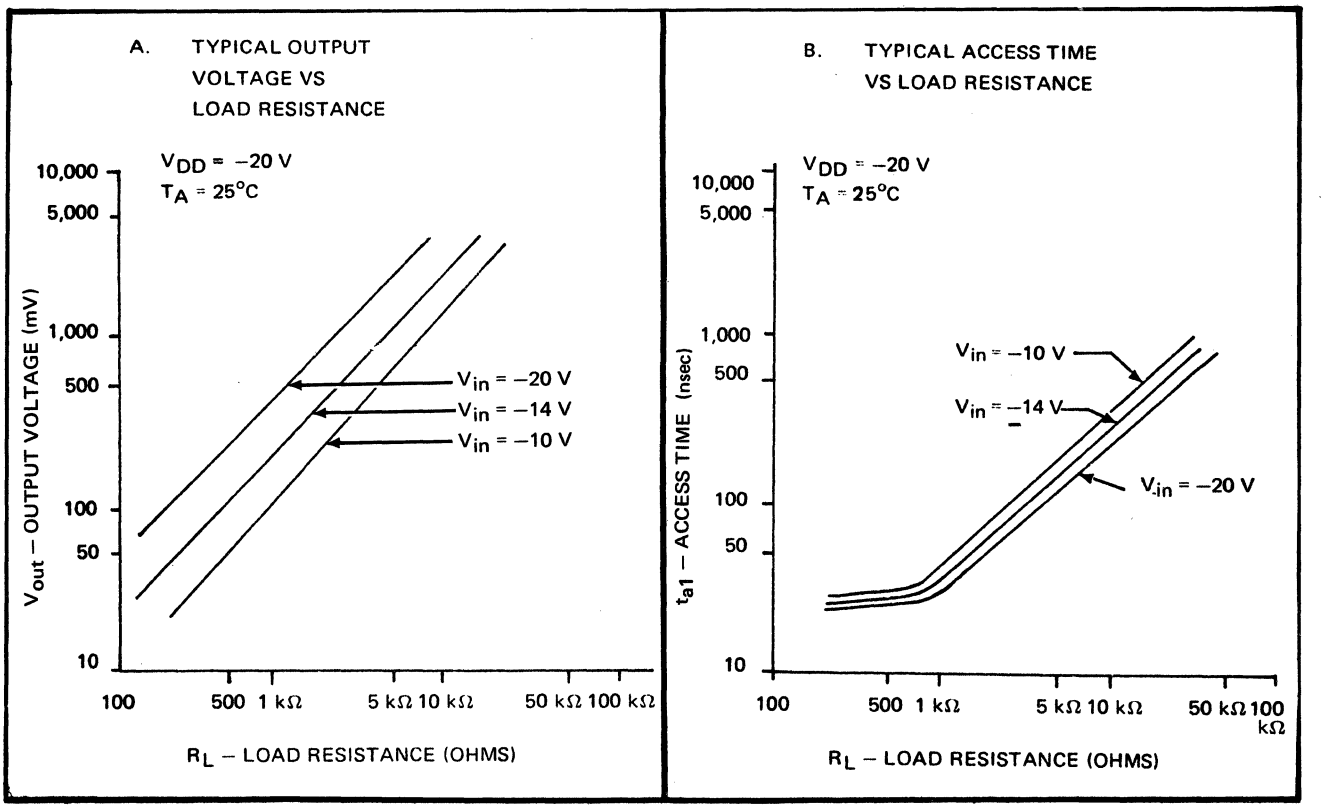
* Section A does not exist in TMS 4500 JC.

voltage waveforms

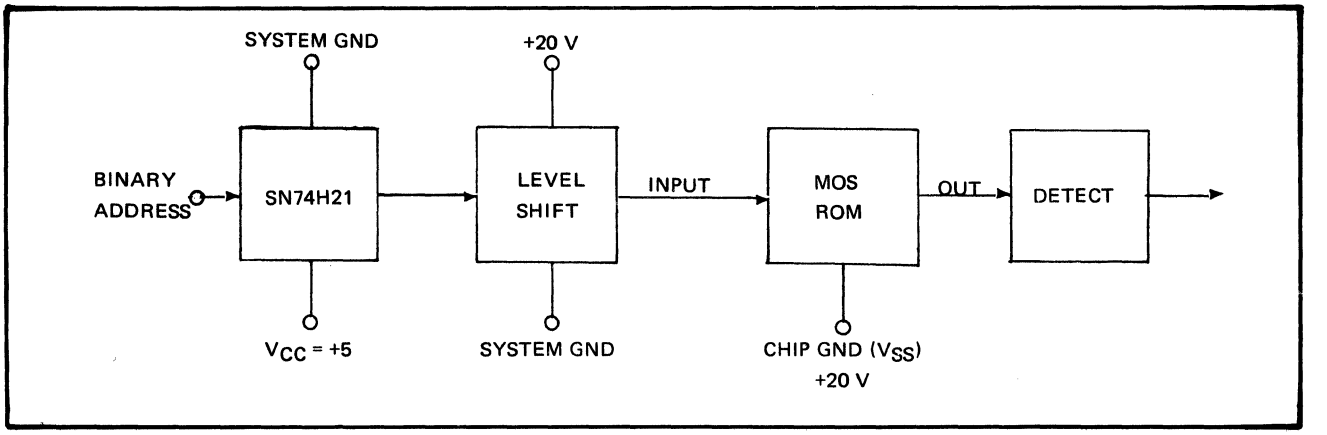


The material herein is believed to be accurate and reliable; however, some parameters specified are derived from evaluation units and may change slightly after full characterization.

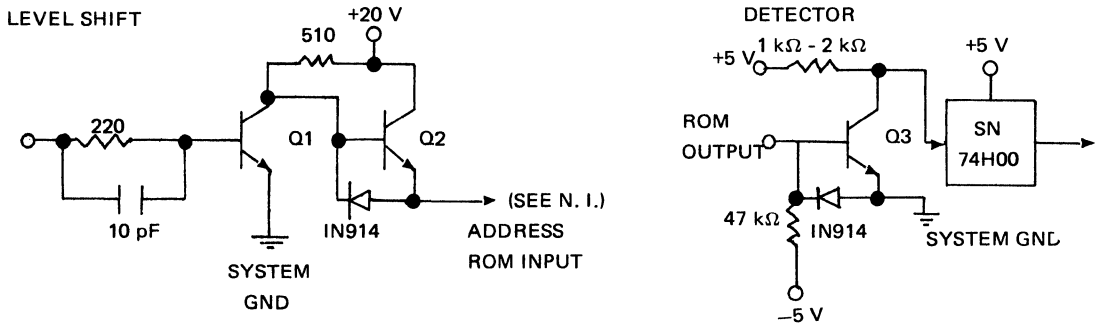
typical characteristics



system diagram



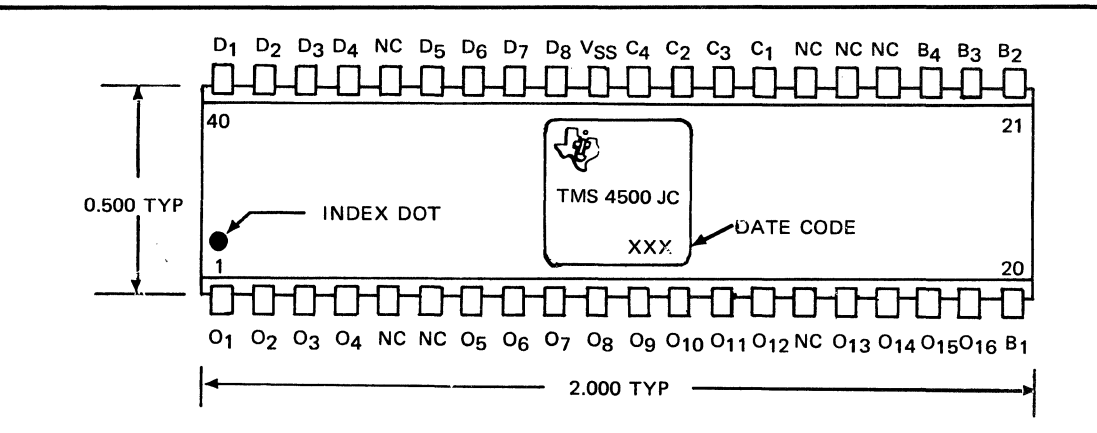
typical circuits



NOTES: 1. Address to inputs of ROM must not be connected to ground.
2. Electrical characteristics on page 2 apply only from ROM input to ROM output.
3. For faster speed, a SN74H20 can replace a SN74H21.
4. Q1, Q2 and Q3 are 2N2369.

mechanical data and pin configurations

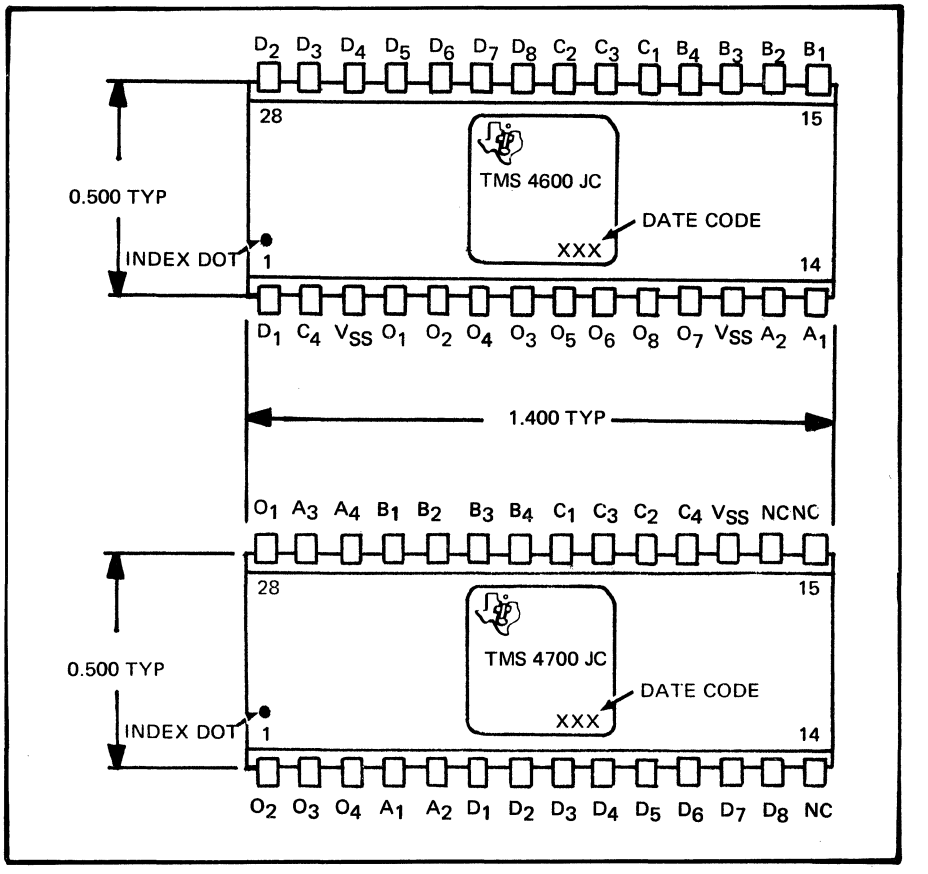
The TMS 4500 JC is mounted in a 40-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.



mechanical data and pin configurations (continued)

The TMS 4600 JC and TMS 4700 JC are mounted in a 28-pin hermetically sealed dual-in-line package, consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows of 0.600-inch centers.

A = INPUT
B = INPUT
C = INPUT
D = INPUT
O = OUTPUT
V_{SS} = SUBSTRATE



TMS4880JC
static read-only memory for parallel output character generator applications

preliminary information

FEATURING:

- Static operation
- 2736-bit capacity
- 37 parallel outputs
- 76 characters of 36 bits
- Optional input resistors
- 600 nsec maximum access time
- Single-ended open-drain output buffers

description

The TMS 4880 JC series is a family of read-only memories manufactured using MOS P-channel enhancement-mode technology. All components in the series contain a 7-bit parallel input character address decoder complete with input inverters. Each input is also provided with an optional 17 kΩ resistor to V_{SS} for internal pull-up. Open-drain output buffers are provided on all the 36 outputs for current mode interfacing. The memory organization and data are permanently stored by programming a single mask.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{DD} range (See Note 1)	−30 V to +0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to +0.3 V
Data input voltage range	−30 V to +0.3 V
Storage temperature range	−55°C to 150°C
Operating free-air temperature range	−25°C to 85°C

NOTE 1. These voltage values are with respect to network substrate terminal (V_{SS}).

logic definition

Negative logic is assumed on the inputs

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

TMS4880JC
static read-only memory for parallel output character generator applications

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−16	V
Supply voltage V_{GG}	−24	−28	−29	V
Input logic 1	−11	−14	−16	V
Input logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at nominal conditions. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplied (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_O	Output Logic 1 current	−14 V applied to output			10	μA
I_O	Output Logic 0 current	−14 V applied to output	0.6	0.8		mA
	Access time	V_{DD} = −14 V, V_{GG} = −28 V		400	600	nsec
	Access time	V_{DD} = −12 V, V_{GG} = −24 V		600	800	nsec
	Input Leakage Current (Note 1)	−16 V applied to input			1	μA
	Input Current (Note 2)	−14 V applied to input		0.8	1.2	mA
	Power Dissipation	V_{DD} = −14 V, V_{GG} = −28 V		300	450	mW

NOTES: 1. Internal resistor not connected.
2. Internal MOS resistor connected with nominal 17 kΩ value.

mechanical data

Depending on the organization of the memory, two packages may be used. When the desired number of outputs is 30 or fewer, a 40-pin package is used with configuration A as shown in the following table. When 31 to 36 outputs are desired, two 28-pin packages are used in configuration B. The initial coding fee is the same for both of these configurations.

mechanical data (continued)

PACKAGE PIN CONFIGURATION, TMS 4880 JC

PIN NO.	A	B	
	TOTAL OUTPUTS – 30 OR FEWER; ONE 40-PIN PACKAGE	TOTAL OUTPUTS – 31 TO 36; TWO 28-PIN PACKAGES	
		FIRST 28-PIN PACKAGE	SECOND 28-PIN PACKAGE
1	O_8	O_{35}	O_{36}
2	O_7	O_{33}	O_{34}
3	O_6	O_{31}	O_{32}
4	O_5	O_{29}	O_{30}
5	O_4	O_{27}	O_{28}
6	O_3	O_{25}	O_{26}
7	O_2	O_{23}	O_{24}
8	O_1	O_{21}	O_{22}
9	V_{DD}	O_{19}	O_{20}
10	V_{GG}	O_{17}	O_{18}
11	GND	O_{15}	O_{16}
12	I_7	O_{13}	O_{14}
13	I_6	O_{11}	O_{12}
14	I_5	O_9	O_{10}
15	I_4	O_7	O_8
16	I_3	O_5	O_6
17	I_2	O_3	O_4
18	I_1	O_1	O_2
19	O_{30}	V_{DD}	V_{DD}
20	O_{29}	V_{GG}	V_{GG}
21	O_{28}	GND	GND
22	O_{27}	I_7	I_7
23	O_{26}	I_6	I_6
24	O_{25}	I_5	I_5
25	O_{24}	I_4	I_4
26	O_{23}	I_3	I_3
27	O_{22}	I_2	I_2
28	O_{21}	I_1	I_1
29	O_{20}		
30	O_{19}		
31	O_{18}		
32	O_{17}		
33	O_{16}		
34	O_{15}		
35	O_{14}		
36	O_{13}		
37	O_{12}		
38	O_{11}		
39	O_{10}		
40	O_9		

TMS4880JC
static read-only memory for parallel output character generator applications

applications

The TMS 4880 JC series is especially suitable for use as a character generator. Configuration A will give 76 characters in a 5 x 6 format and configuration B will add the bottom row to give 76 characters in a 5 x 7 format as shown.

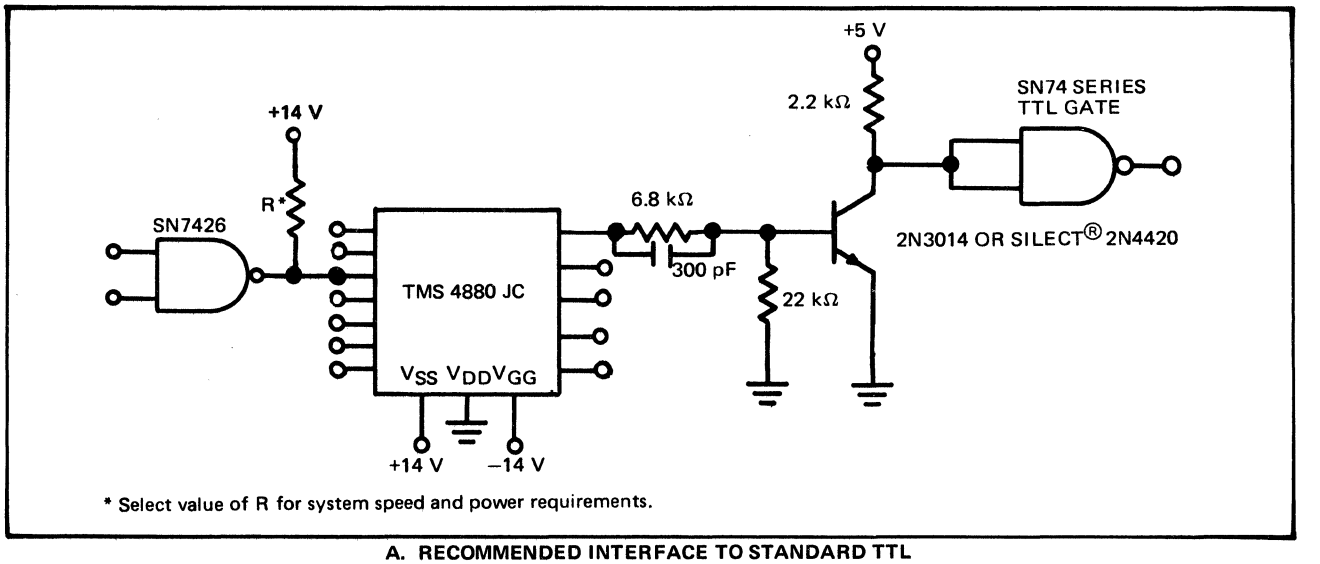
CONFIGURATION B

O_1	O_2	O_3	O_4	O_5
O_6	O_7	O_8	O_9	O_{10}
O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
O_{16}	O_{17}	O_{18}	O_{19}	O_{20}
O_{21}	O_{22}	O_{23}	O_{24}	O_{25}
O_{26}	O_{27}	O_{28}	O_{29}	O_{30}
O_{31}	O_{32}	O_{33}	O_{34}	O_{35}

CONFIGURATION A

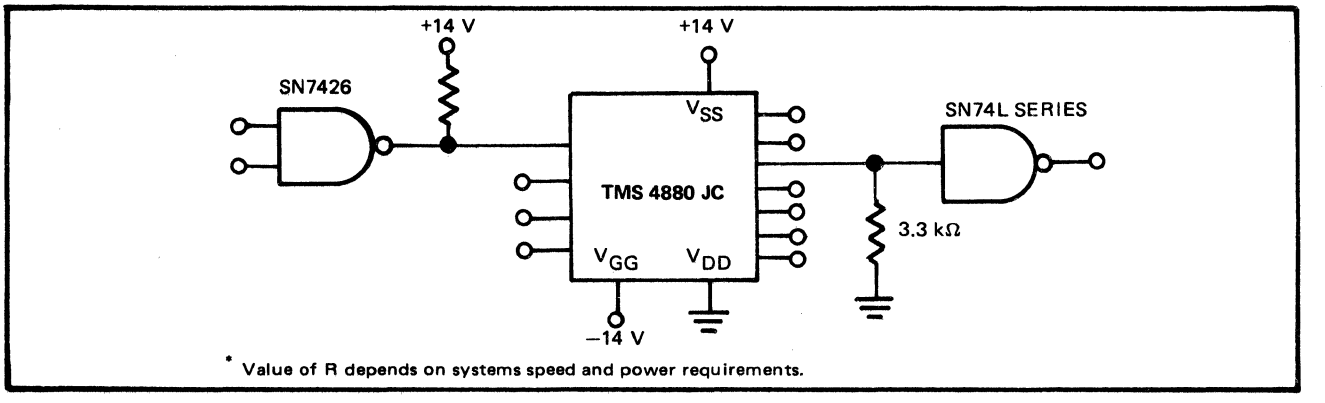
NOTE: The 36th bit is not generally used for the display but is associated with a cascade (chip enable etc.)

TTL interface



A. RECOMMENDED INTERFACE TO STANDARD TTL

No input resistors are necessary if internal input resistors are specified.



B. DIRECT LOW POWER TTL INTERFACE

custom circuits

The TMS 4880 JC series is programmed during the gate oxide removal stage of manufacturing. Only one mask per unique design need be created and all other processing steps remain the same for all devices. Options available to the customer during programming are:

- Character Format
- Enable Logic Polarity
- Input Resistors

The data to be stored in the memory must be submitted to TI on computer-punched cards.

Information concerning chip organization, type of output buffer, and chip select must be submitted to TI on a standard form.

A SOFTWARE PACKAGE bulletin available from TI describes both documents.

standard circuits

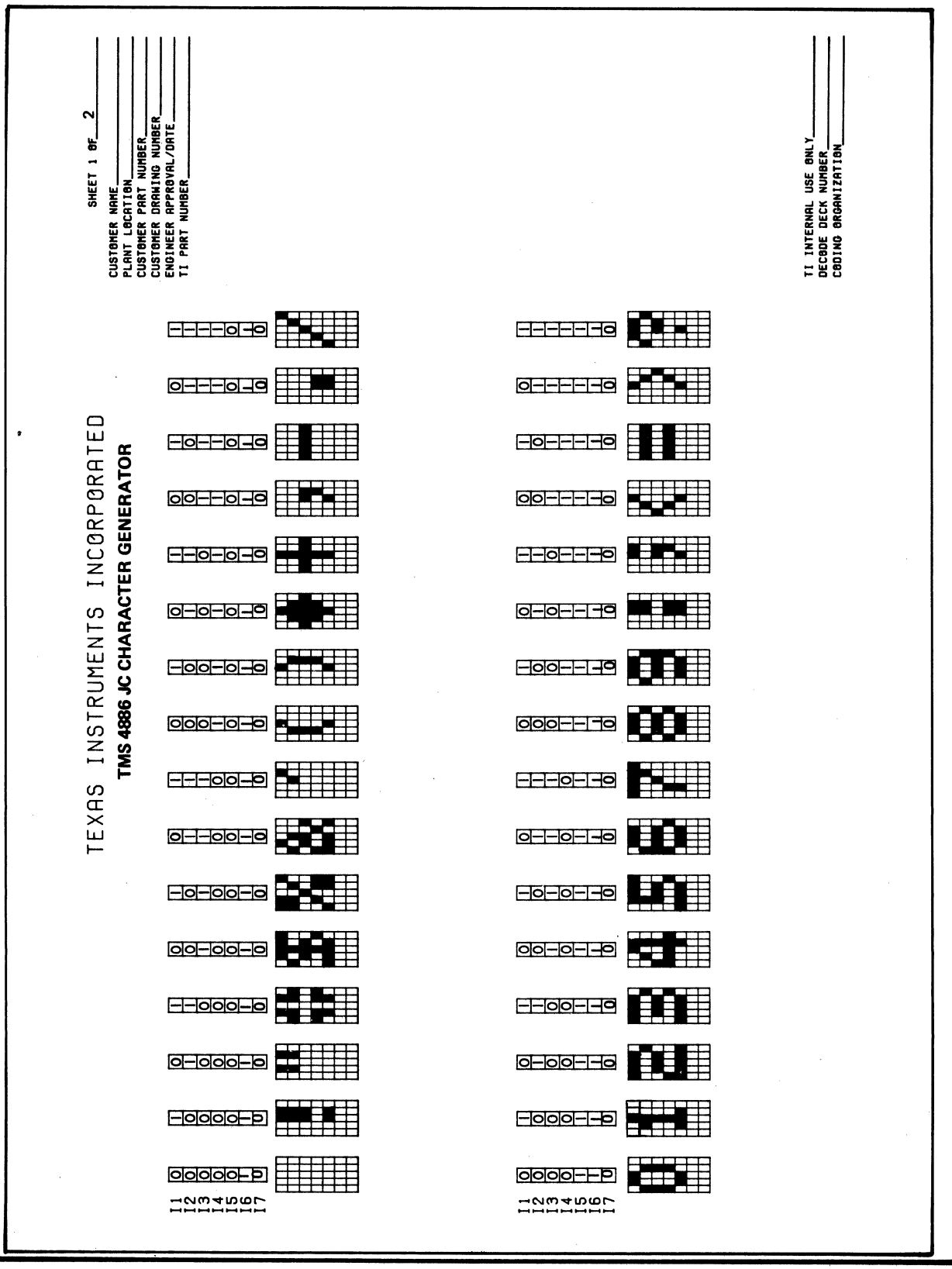
Because certain codes are widely used, TI has created a series of standard devices, which are available off the shelf and for which there is no coding charge. The most widely used standard device is: TMS 4886 JC USASCII CODE (See attached character format).

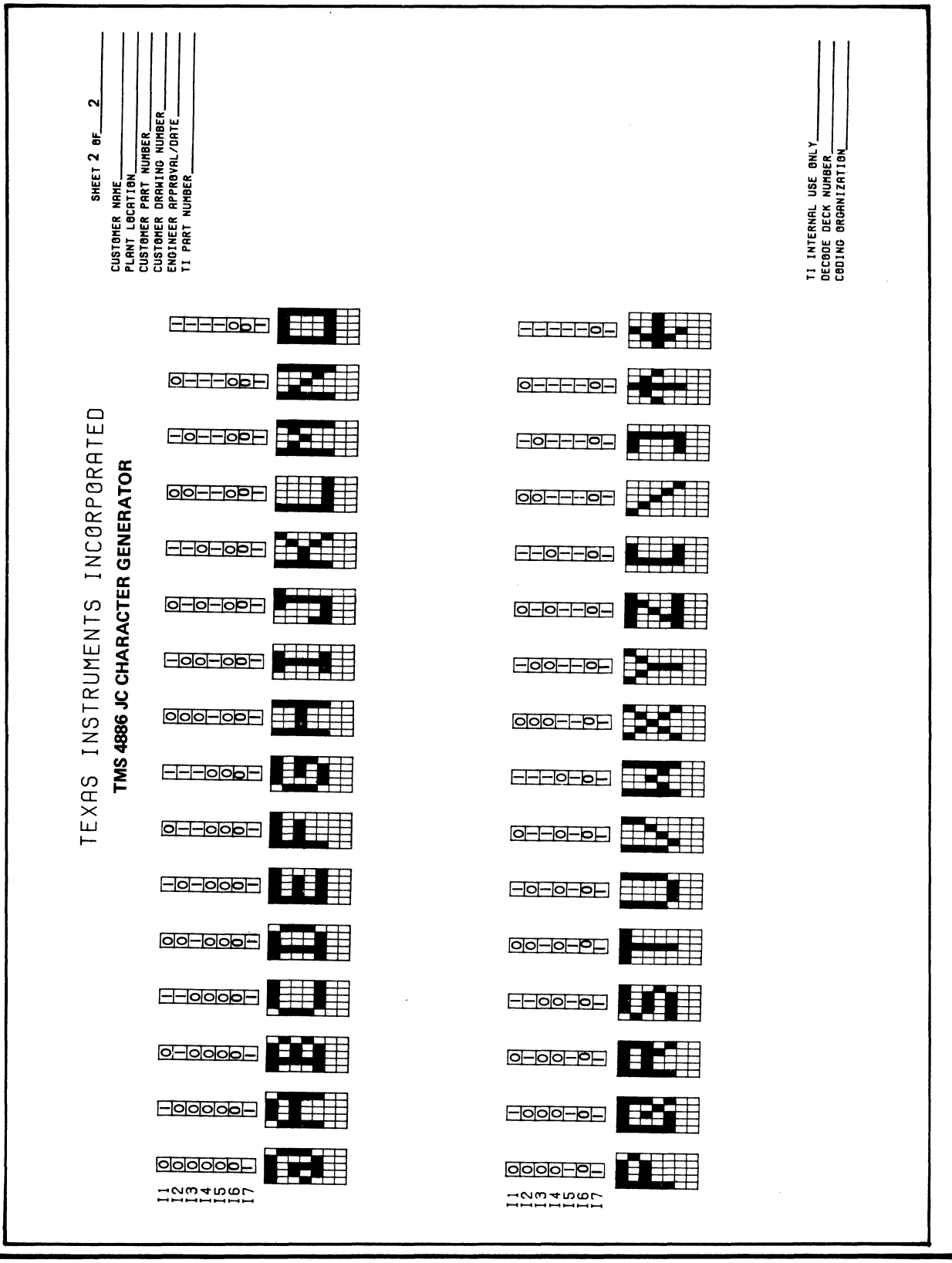
Organization: 64 Character Storage

25-Bit Character Matrix (5 x 5)

40-Pin Package

TMS4880JC
static read-only memory for parallel output character generator applications

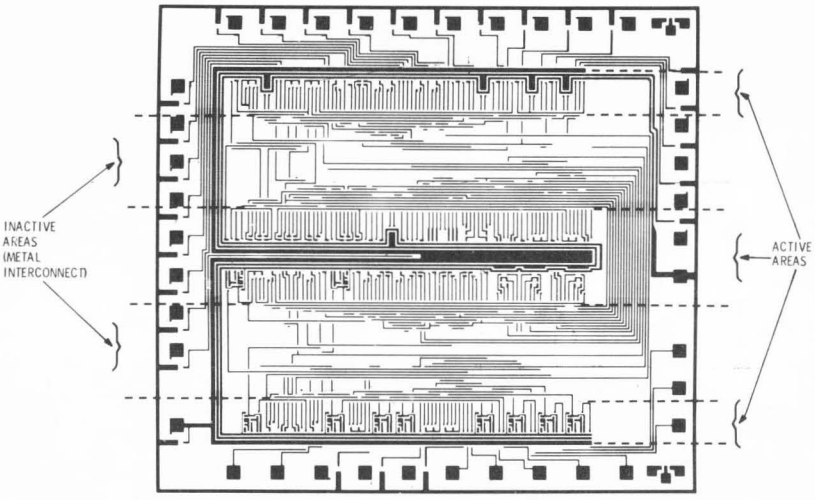




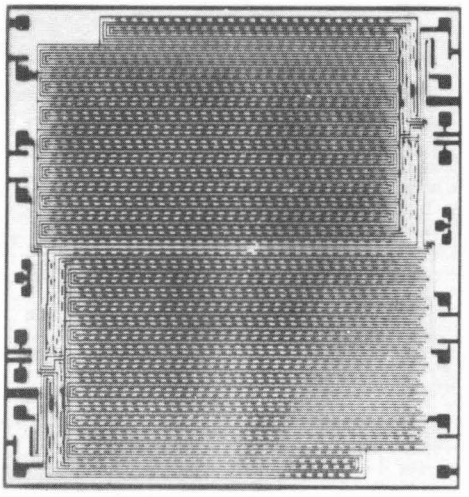
programmable logic arrays

Programmable logic arrays represent an economical and efficient way to implement random logic using programmable techniques. By random logic we mean a logic circuit that is not strongly structured, as opposed to such circuits as shift registers, read-only memories, etc. When a random logic circuit is implemented in MOS, a large part of the chip area is used for interconnection between the cells, as can be seen from the pictures below. This area is essentially wasted.

RANDOM LOGIC CHIP



SHIFT REGISTER CHIP



SOME ECONOMICS

A customer who wants to build a random logic circuit can choose any of three ways: use bipolar, relatively low complexity, integrated circuits; use a custom MOS circuit; use a programmable MOS circuit (such as read-only memory or a PLA).

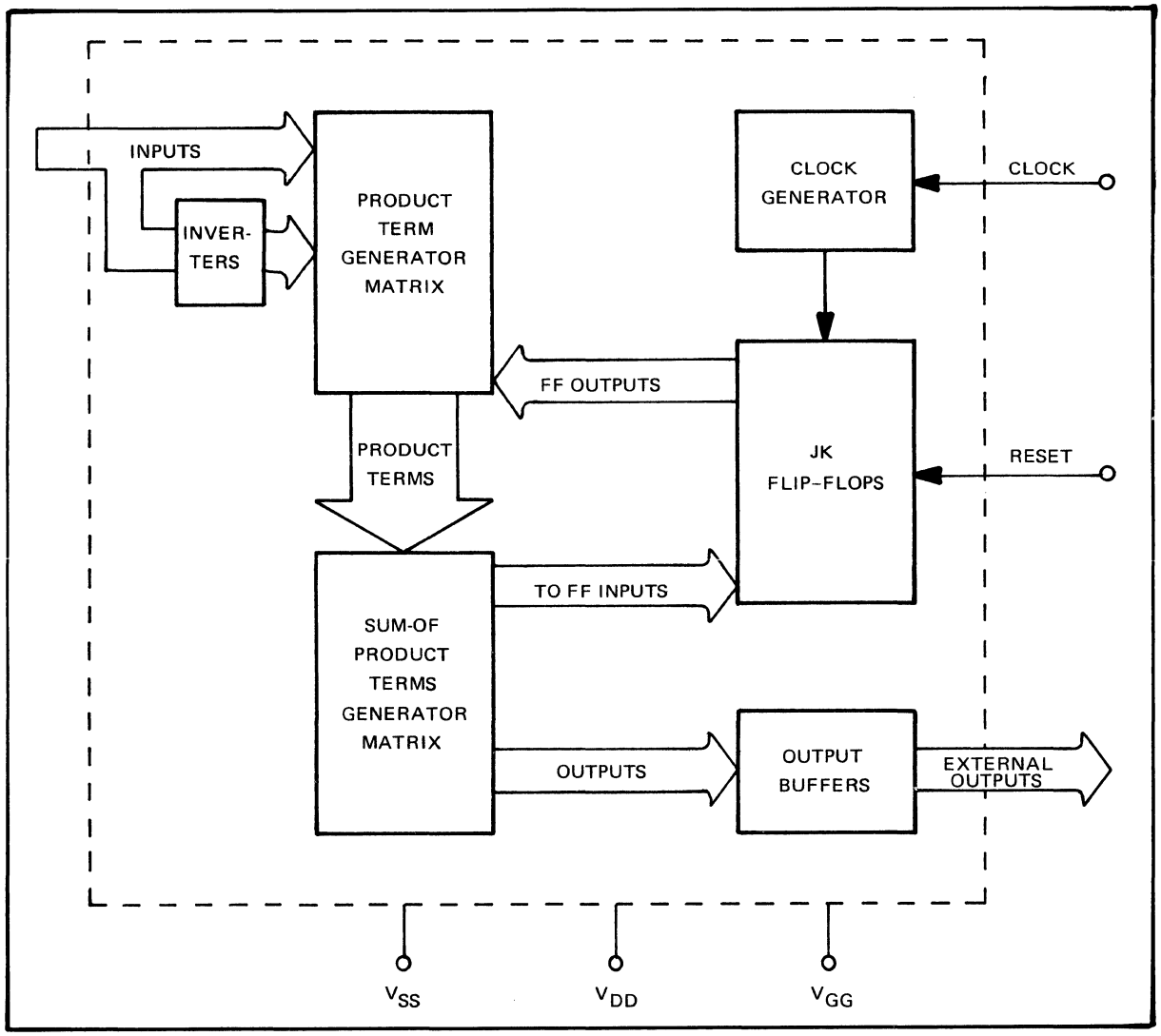
A custom MOS circuit will be designed from scratch. We will take the customer's logic and implement it on a piece of silicon. We will, of course, try to reduce the size of the chip as much as possible, but there will still be a large inactive area for interconnections. With the programmable approach we start with a circuit that is already designed. In order to program the device, we just modify one of our masks, and this is accomplished easily and economically.

PLA STRUCTURE

The PLA structure is extremely simple. Any logic equation can be written as a sum of products or as a product of sums, and that is exactly what has been implemented on the array.

The logic expression is written as a sum of products:

- A first programmable matrix generates the products terms (AND matrix)
- A second programmable matrix generates the sum of products (OR matrix)
- Flip-flops are used in feedback loops to permit implementation of sequential logic.



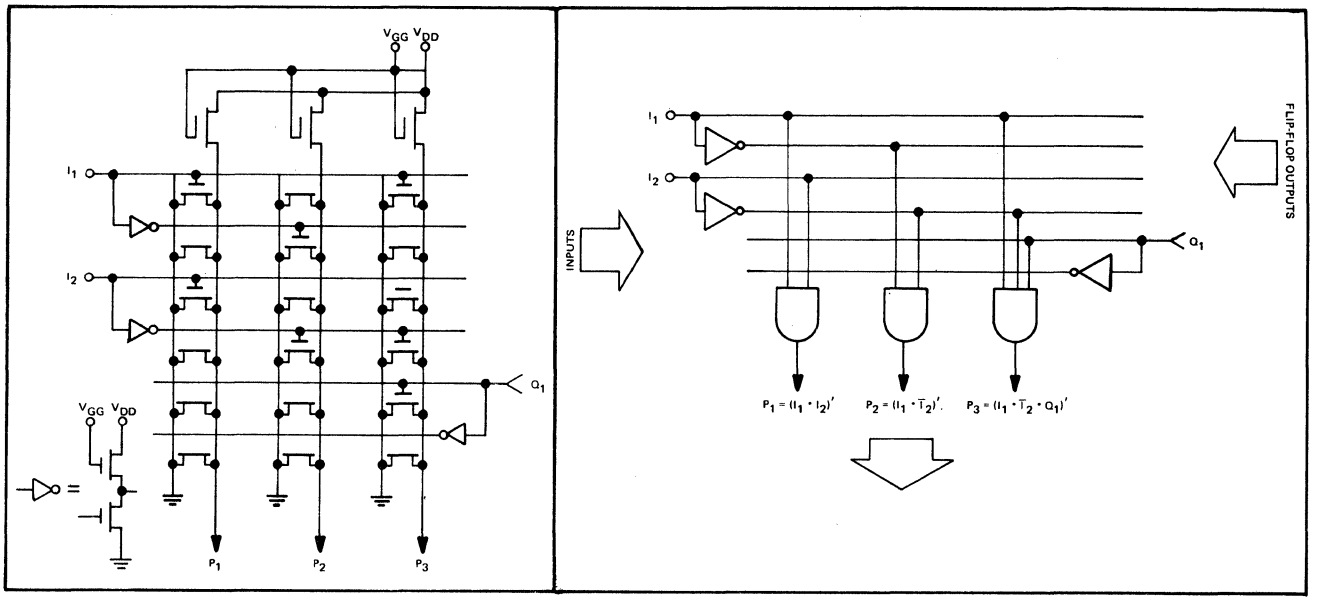
1) AND Matrix

The role of the AND matrix is to form the product terms of the input terms, and their complements.

The number of product terms has been arrived at by heuristic methods. We have set a limit of 60 product terms for the TMS 2000 JC, and 72 for the TMS 2200 JC.

PLA 'AND' MATRIX

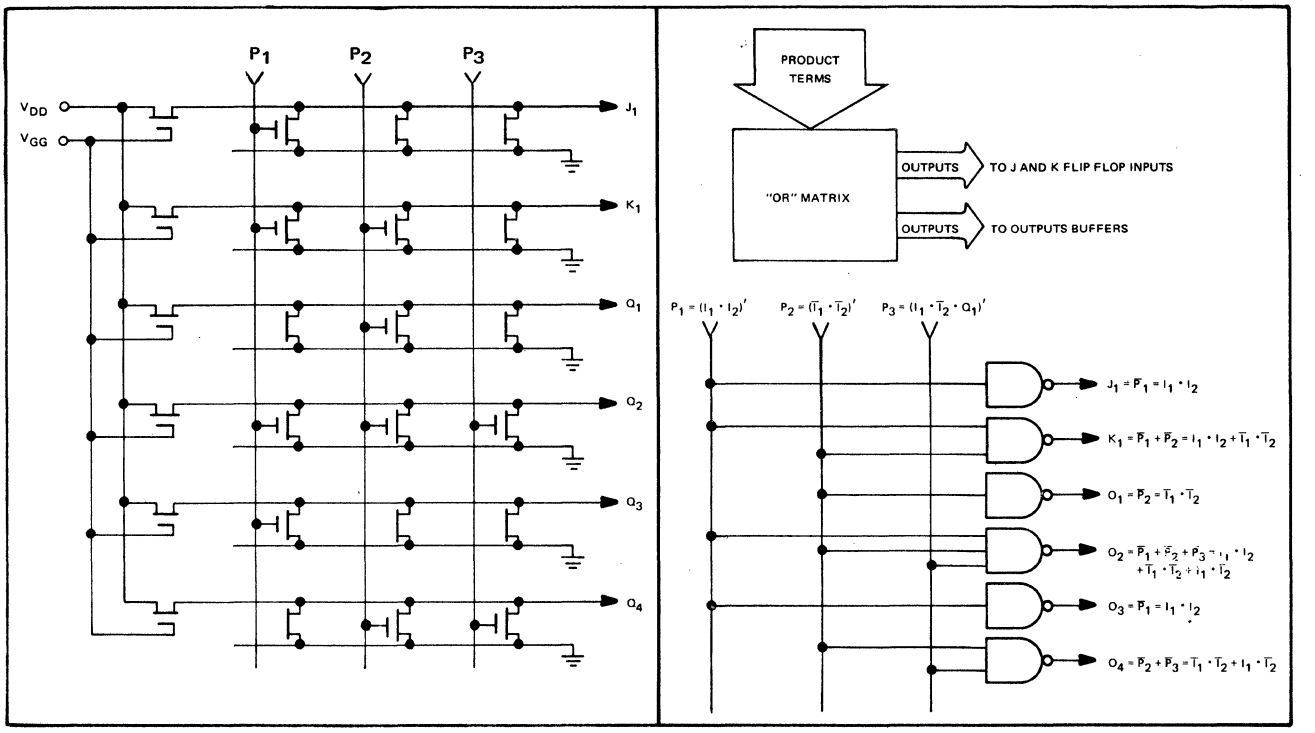
LOGIC EQUIVALENT OF PLA 'AND' MATRIX



2) OR Matrix (Sum of products)

PLA 'OR' MATRIX

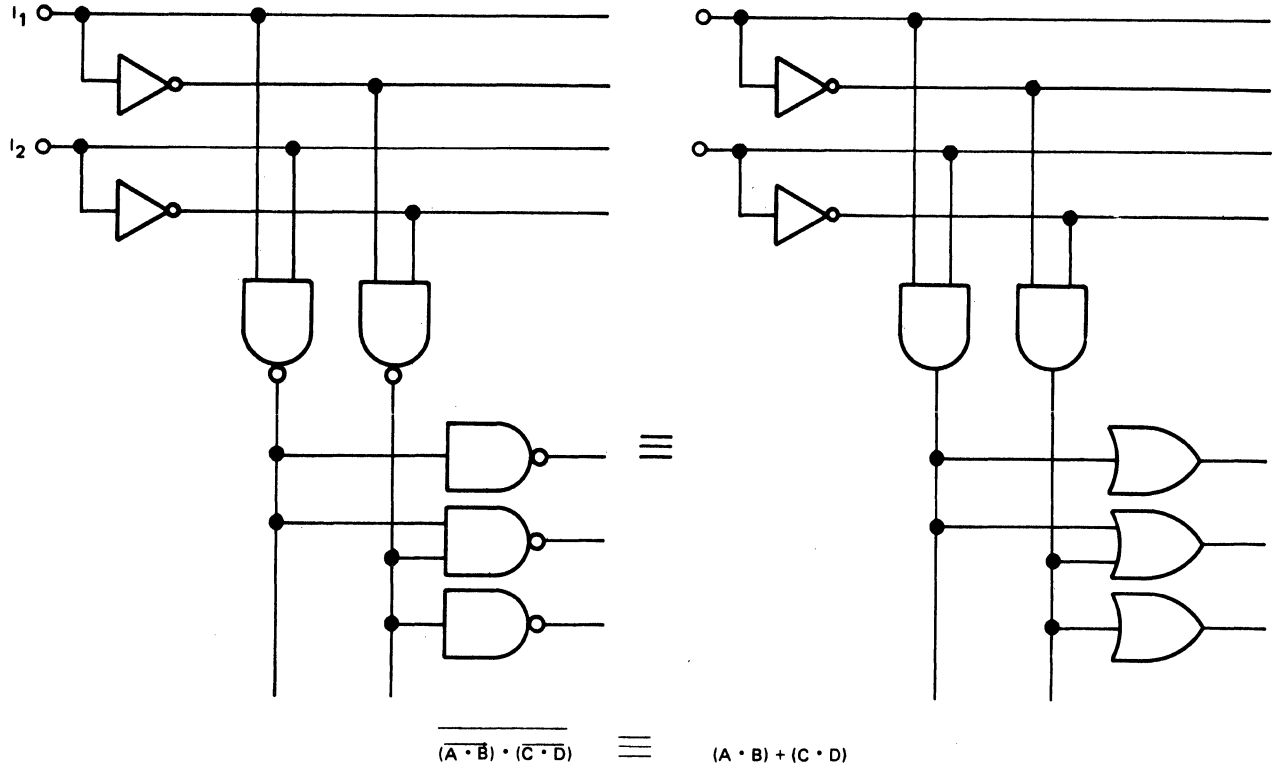
LOGIC EQUIVALENT OF PLA 'OR' MATRIX



The AND matrix feeds into the OR matrix. The OR matrix generates sums of product terms. Some of the outputs of the OR matrix are fed to the outside while others are fed back to the first matrix (AND) through flip-flops.

Both matrices are programmable. A product term can be of as many of the inputs and their complements as the designer wants. By this same token a sum of product terms can be of as many of the products as the designer wishes.

LOGIC EQUIVALENT OF PLA ORGANIZATION



3) Feedback Loops, Flip-Flops

In order to implement sequential logic, feedback loops are necessary. These feedback loops must be timed. If we fed back directly the outputs of this second matrix (OR matrix) to the inputs of the first matrix (AND), a race condition could develop. We use one JK master-slave flip-flop per feedback loop to take care of this timing. We are able to reset all these flip-flops to initialize the logic. The designer is free to choose which and how many outputs are fed back to the first matrix.

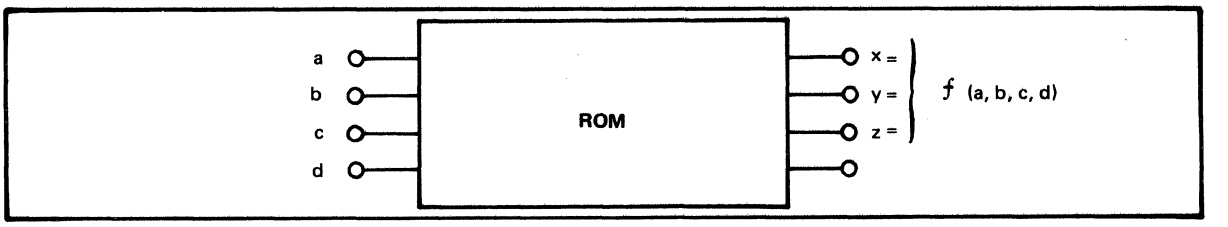
programmable logic arrays

PLA VERSUS ROM

As we have just seen, a PLA is actually a big Read Only Memory that has been adapted to the implementation of random logic. How does a PLA differ from a ROM and what are the advantages?

1) Combinational Logic

Combinational logic is easily implemented on a read-only memory. The truth table is written in such a way that the outputs are logic functions of the inputs.



The main drawback to this scheme is that everytime an input variable is added, the size of the ROM is doubled. This is because the decode scheme of the read-only memory is exhaustive. All the product terms are generated, and that soon becomes prohibitive. To do what our PLA TMS 2000 JC does through straight read-only-memory techniques would take 2^{25} words (17 external inputs and 8 inputs from the flip-flops), that is 8,288,608 words of 26 bits (18 external outputs and 8 feedback loops) — or a total capacity of 218,103,808 bits which is a ludicrous size for any read-only memory.

In a PLA we do not generate all the product terms. We have set the limit at 60 product terms for the TMS 2000 JC and to 72 for the TMS 2200 JC. These numbers have been arrived at through heuristic methods and have proven to be sufficiently large. It is not often that an equation is presented with 60 terms, each one being a product of up to 25 variables.

2) Sequential logic

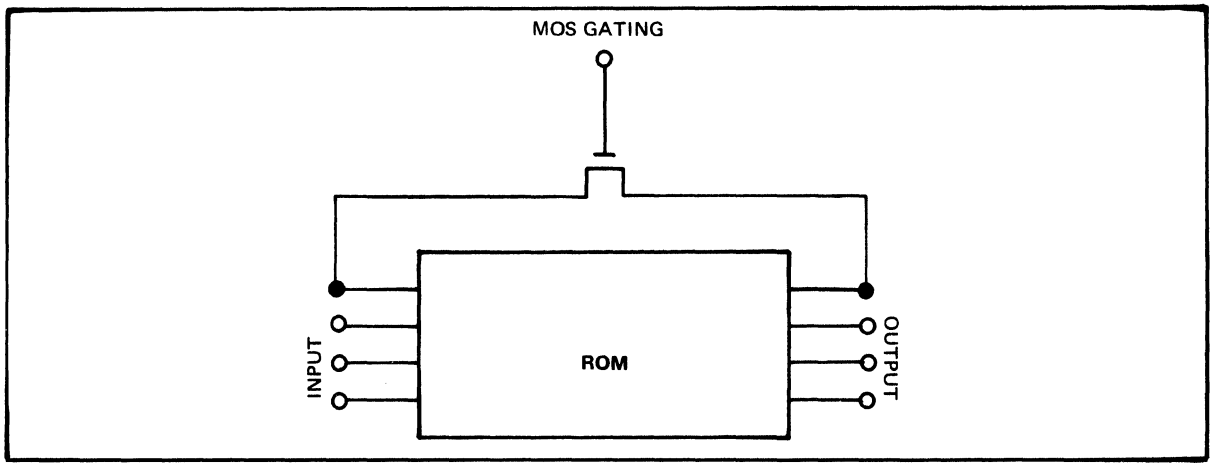
To perform sequential logic with a read-only memory, the outputs must be fed back to the inputs through a gating arrangement.

This is comparatively easy to do but has drawbacks.

- For each feedback loop two package pins are wasted.
- The gating arrangement has to be provided.
- Initialization of the logic is difficult.

In the PLAs the feedback loops are never brought outside, which saves a number of pins. The initialization is easy because JK flip-flops are used.

ROM CONNECTED TO PERFORM SEQUENTIAL LOGIC



CATALOG PLAs

We presently have two catalog PLAs:

TMS 2000 JC	TMS 2200 JC
40 pins	28 pins
17 external inputs	13 external inputs
18 outputs	10 outputs
8 flip-flops	10 flip-flops
60 product terms	72 product terms

These devices are produced using silicon nitride technology, which permits easy interface with TTL/DTL.

DESIGN CONSIDERATIONS

1) Logic design

Logic design with PLAs is easy. With the PLA approach the designer writes down the logic equations of each of the outputs in terms of the external inputs and feedback inputs.

Once this is done the programming of the matrices is handled by a computer program. A SOFTWARE PACKAGE bulletin describes in detail the mechanical aspects of the operation.

2) Design efficiency

The PLA is an extremely powerful tool. The designer must be careful to use as fully as possible the capability of the PLAs. To help him do that we have published a SOFTWARE PACKAGE bulletin and application report which includes design considerations. We have found the PLA technique to be extremely efficient from a silicon real-estate point of view.

TMS2000JC, TMS2200JC
programmable logic arrays
preliminary information

FEATURING

- Low-threshold MOS/bipolar technology
- Static operation
- Push-pull or single-ended output buffers
- Optional internal MOS pull-up resistor on inputs
- Hermetic ceramic dual-in-line package
- TTL compatible

description

The programmable logic array (PLA) is a device that is programmable by gate oxide mask. It is used to perform sequential and combinational logic.

The TMS 2000 JC and TMS 2200 JC series are groups of programmable logic arrays manufactured using P-channel enhancement-mode, low-threshold MOS and NPN bipolar techniques.

A PLA is a unique combination of master-slave JK flip-flops and static read-only memories on a single MOS/LSI chip. The programmable logic arrays have been designed to permit the implementation of custom random logic with the same low cost and quick turnaround using a read-only memory. Sequential and combinational logic may be implemented in a PLA. The logic is described in the form of Boolean equations, which are converted by TI software routines into the gate oxide mask.

In the TMS 2000 JC seventeen external inputs and the eight flip-flop outputs are combined by a product term generator into 60 product terms. These are then combined by a sum-of-product-terms generator into 16 lines for the 8J and 8K inputs to the 8 JK master-slave flip-flops and into 18 external outputs. The flip-flop operation is controlled by a common reset input and a single clock.

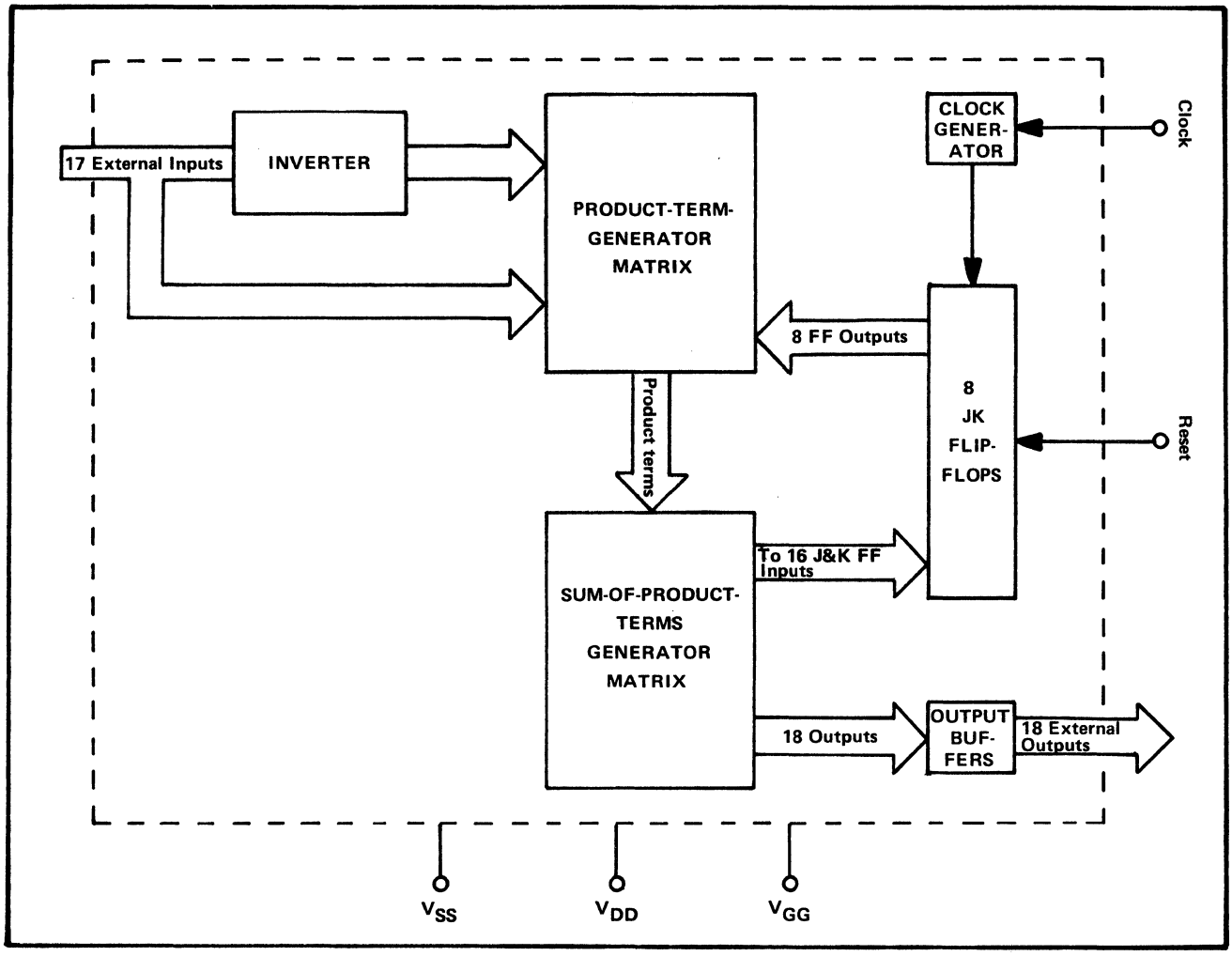
In the TMS 2200 JC thirteen external inputs and the ten flip-flop outputs are combined by a product term generator into 72 product terms. These are then combined by a sum-of-product-terms generator into 20 lines for the 10J and 10K inputs to the 10 JK master-slave flip-flops and into 10 external outputs. The flip-flop operation is controlled by a common reset input and a single clock.

The device inputs have optional internal pull-up resistors for easy interface. The output buffers incorporate bipolar NPN transistors and either push-pull or open-ended buffers may be chosen. These features facilitate interfacing the PLAs in TTL systems.

organization

	TMS 2000 JC	TMS 2200 JC
Number of product terms	60	72
Number of external inputs	17	13
Number of external outputs	18	10
Number of JK flip-flops	8	10

functional diagram of a programmable logic array (TMS 2000 JC)



operation

1) Input

The present external inputs and the previous flip-flop outputs control the state of the internal flip-flops.

2) Internal

Data is entered into the master flip-flop during the positive edge of the clock inputs, while the slave flip-flop is set during the negative edge.

The flip-flops may be reset at anytime by applying a low voltage on the reset input. However, if the reset input is taken high while the clock is high, an indeterminate flip-flop state may result.

3) Output

The external outputs can be a function of the present inputs or the present flip-flop outputs, or a function of both.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See note)	−15 V to +0.3 V
Supply voltage V_{GG} range (See note)	−25 V to +0.3 V
Clock and data input voltage ranges (See note)	−15 V to +0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C
Power dissipation	300 mW

NOTE: These voltage values are with respect to V_{SS}.

logic definition

Positive logic is assumed

a) Logic 1 = most positive voltage

b) Logic 0 = most negative voltage

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−4.7	−10	−11	V
Supply voltage V_{GG}	−15	−17	−18.5	V
$V_{in(0)}$ with internal resistor (TTL)	−4	−5	−5.25	V
$V_{in(1)}$ with internal resistor (TTL)	0	−5	−1.5	V
$V_{in(0)}$ without internal resistor (MOS)	−4	−5	−11	V
$V_{in(1)}$ without internal resistor (MOS)	+0.3	−0.5	−1.5	V

NOTE: All voltages are with respect to V_{SS}.

The design of the unit permits a broad range of operations that allows the user to take advantage of readily available power supplies (e.g., +5 V, −5 V, −12 V).

electrical characteristics at nominal operating conditions and 25°C

PARAMETER		TEST CONDITIONS†	MIN	NOM	MAX	UNITS
$V_{out(1)}$	Logical 1 output voltage	R_L = 10 kΩ to V_{DD} (See Note 1)	0	−0.7	−1.0	V
$V_{out(0)}$	Logical 0 output voltage	R_L = 10 kΩ to V_{SS} (See Note 1)	−8	−9	−10	V
$V_{out(1)}$	Logical 1 output voltage	R_L = 6.8 kΩ to V_{GG} (See Note 2)	0	−0.7	−1.0	V
$V_{out(0)}$	Logical 0 output voltage	R_L = 6.8 kΩ to V_{GG} (See Note 1)	−10	−11	−17	V
$I_{in(0)}$	Input leakage current	V_{IN} = −10 V (See Note 3)			−1.0	μA
$I_{in(0)}$	With internal resistor (TTL)		−0.8	−0.9	−1.1	mA
$I_{in(1)}$	With internal resistor (TTL)		0	−40	−125	μA
R_{in}	Input impedance	V_{IN} = 0 V to −10 V (See Note 4)	5	7	12	kΩ
C_{in}	Input Capacitance	V_{IN} = 0, f = 1 MHz		3	5	pF
I_{DD}	Supply current into V_{DD} terminal			18	25	mA
I_{GG}	Supply current into V_{GG} terminal			1.0	4.0	mA
I_{GG}	Supply current into V_{GG} terminal	See Note 5		15	20	mA

† Unless otherwise noted, R_L = 10 kΩ to V_{SS}.

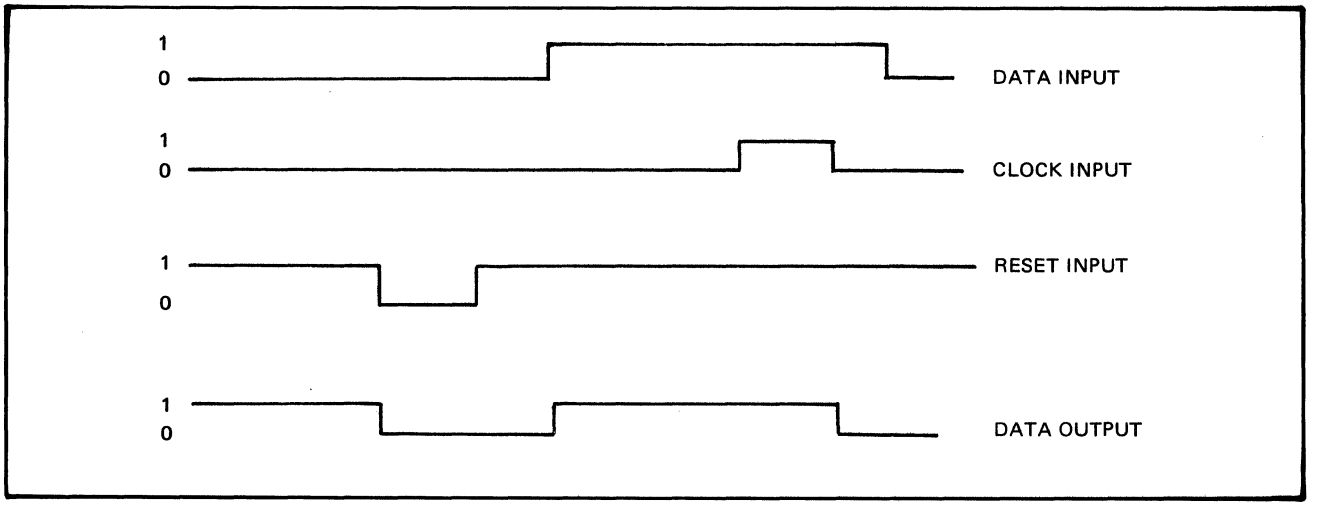
NOTES: 1. Push-pull output buffers used
2. Single-ended output buffer used
3. Optional input resistors not used
4. Optional input resistors used
5. All outputs at logic 1

TMS2000JC, TMS2200JC
programmable logic arrays

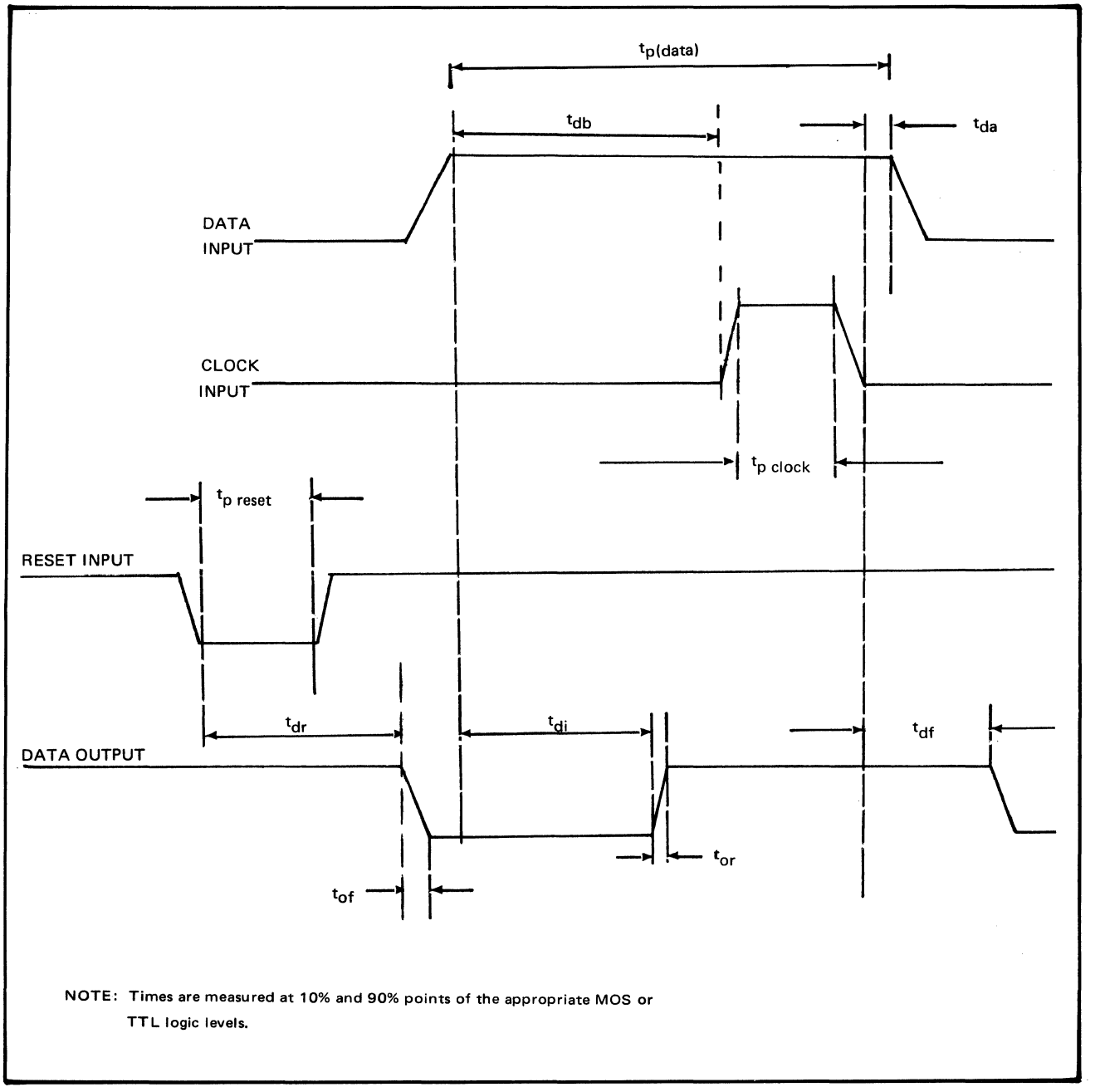
switching characteristics at nominal operating conditions and 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{p(data)}$	Width of data pulse	C_L = 30 pF, R_L = 1 MΩ	2.0			μs
$t_{p(clock)}$	Width of clock pulse	C_L = 30 pF, R_L = 1 MΩ	0.5			μs
$t_{p(reset)}$	Width of reset pulse	C_L = 30 pF, R_L = 1 MΩ	0.5			μs
f	Clock repetition rate	C_L = 30 pF, R_L = 1 MΩ	0		200	kHz
t_{di}	Propagation delay time from input to output with no clock	C_L = 30 pF, R_L = 1 MΩ	0.9	1.1	1.4 (25°C) 1.9 (85°C)	μs μs
t_{dr}	Propagation delay time from reset input to a change in external output	C_L = 30 pF, R_L = 1 MΩ		1.1	1.4 (25°C) 1.9 (85°C)	μs μs
t_{df}	Propagation delay time from clock input to a change in external output	C_L = 30 pF, R_L = 1 MΩ	0.9	1.1	1.4 (25°C) 2.1 (85°C)	μs μs
t_{db}	Delay time required between data input and positive edge of clock	C_L = 30 pF, R_L = 1 MΩ	1.9			μs
t_{da}	Input hold time after negative edge of clock	C = 30 pF, R_L = 1 MΩ	0.1			μs
t_{or}	Output rise time (single-ended output)	6.8 kΩ to V_{GG}	20	60	200	ns
t_{of}	Output fall time (single-ended output)	6.8 kΩ to V_{GG}	100	250	350	ns
t_{or}	Output rise time (push-pull output)	C_L = 30 pF, R_L = 1 MΩ	20	60	200	ns
t_{of}	Output fall time (push-pull output)	C_L = 30 pF, R_L = 1 MΩ	100	200	300	ns

timing diagram



voltage waveforms



NOTE: Times are measured at 10% and 90% points of the appropriate MOS or TTL logic levels.

TMS2000JC, TMS2200JC
programmable logic arrays

mechanical data

The TMS 2000 JC is mounted in a 40-pin hermetically sealed, dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

The TMS 2200 JC is mounted in a 28-pin hermetically sealed, dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

package pin configuration — TMS 2000 JC

PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{DD}	11	O_{10}	21	RESET	31	I_{10}
2	O_1	12	O_{11}	22	I_1	32	I_{11}
3	O_2	13	O_{12}	23	I_2	33	I_{12}
4	O_3	14	O_{13}	24	I_3	34	I_{13}
5	O_4	15	O_{14}	25	I_4	35	I_{14}
6	O_5	16	O_{15}	26	I_5	36	I_{15}
7	O_6	17	O_{16}	27	I_6	37	I_{16}
8	O_7	18	O_{17}	28	I_7	38	I_{17}
9	O_8	19	O_{18}	29	I_8	39	CLOCK
10	O_9	20	V_{SS}	30	I_9	40	V_{GG}

package pin configuration — TMS 2200 JC

PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{DD}	8	O_6	15	I_1	22	I_8
2	V_{GG}	9	O_7	16	I_2	23	I_9
3	O_1	10	O_8	17	I_3	24	I_{10}
4	O_2	11	O_9	18	I_4	25	I_{11}
5	O_3	12	O_{10}	19	I_5	26	I_{12}
6	O_4	13	V_{SS}	20	I_6	27	I_{13}
7	O_5	14	RESET	21	I_7	28	CLOCK

interfacing

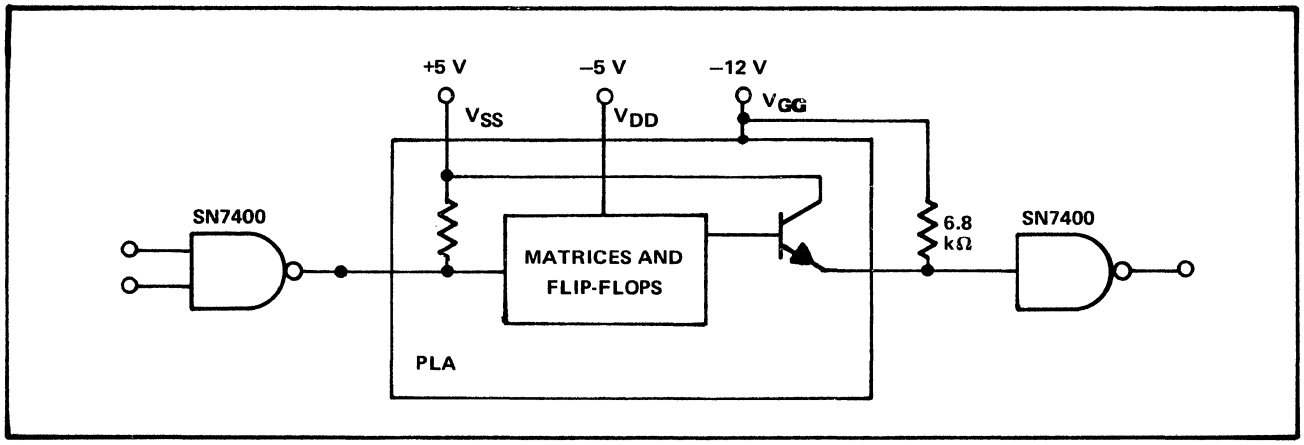
a) To TTL system

Each external input of the PLA has an optional internal MOS pull-up resistor available for interfacing with TTL. With V_{SS} at +5 volts, this internal resistor serves to pull up a logic 1 from the TTL specified level of 2.4 V to V_{SS}.

interfacing (continued)

The output buffer may be chosen at its programming stage as either push-pull or open-ended. To interface with TTL systems or when the wired-OR capability is required, the open-ended buffer would be used with an external resistor.

INTERFACE CIRCUITS WITH TTL SYSTEMS

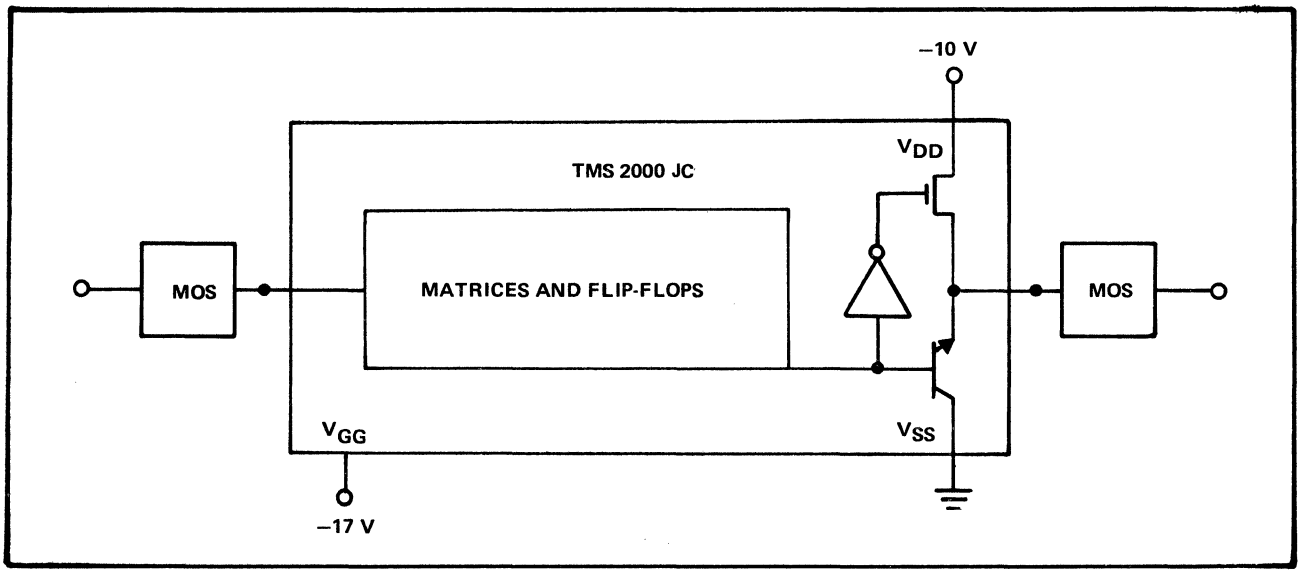


b) To MOS systems

For input interfacing from other MOS devices, the internal pull-up resistors are not required.

The output buffer is selected as a push-pull type to provide a high-capacitive drive without the need of an external resistor.

INTERFACING WITHIN MOS SYSTEMS



custom programming

The logic functions performed by the PLA are controlled by programming or coding the product-terms-generator matrix and the sum-of-product-terms-generator matrix.

The number of different product terms is limited to 60 (TMS 2000 JC) or 72 (TMS 2200 JC).

The logic equations define the sum of product terms. There will be one equation for each output and for each flip-flop input. A computer program is used to implement the logic equations on the chip.

Complete information on programming Texas Instruments MOS/LSI program logic arrays is contained in a PLA SOFTWARE PACKAGE.

The rapid evolution of MOS technology is causing the designer to re-evaluate his ideas on the practicality of MOS memories. Nobody expects MOS memories immediately to replace all magnetic memories, particularly in large main-frame applications. But rather new concepts are emerging which take advantage of the performance and cost benefits of MOS. Data handling systems using MOS random-access memories, and read-write scratch-pad memories are only a few of the more immediate applications of MOS memory technology.

CHARACTERISTICS

MOS RAMs are ideally suited for those applications requiring small to medium-size storage capability, high speeds, and low power dissipation. They can replace core memories used for scratch pads or small computer needs while offering faster access times and a simpler drive circuitry. Their low access times make them attractive in applications where other semiconductor memories were considered, but found unsatisfactory for reasons of cost, power dissipation, or package count.

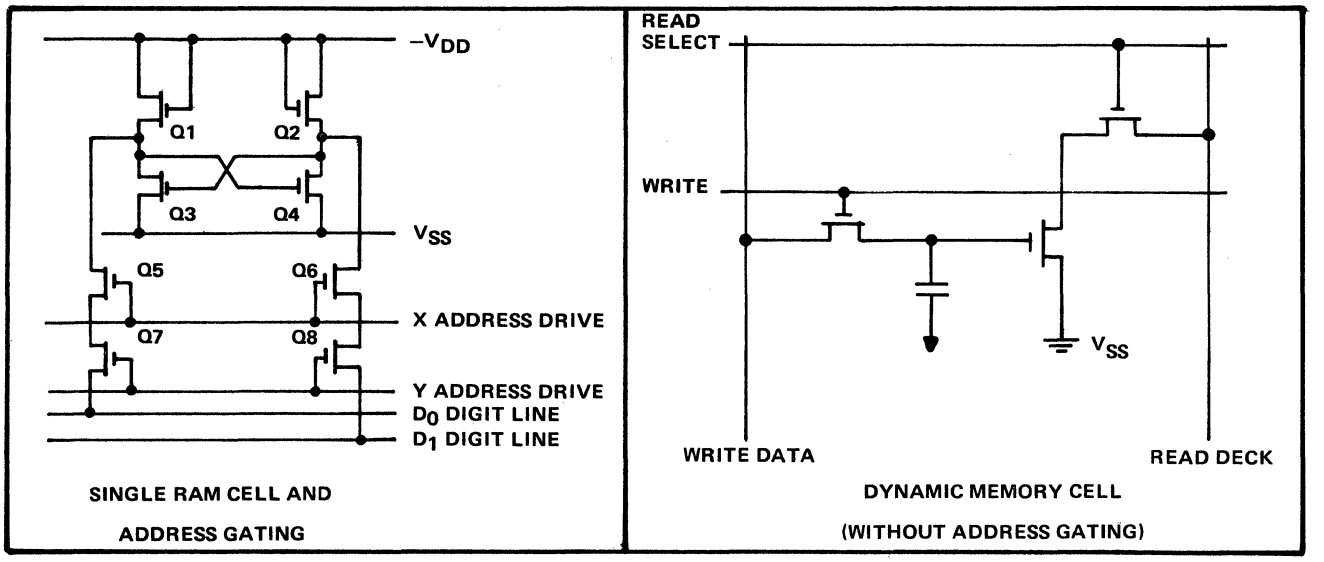
Random-access memories presently on the market are either static or dynamic.

- STATIC – An MOS flip-flop is used to store the information. Clocks are not needed. The data will stay in storage as long as the power is maintained.
- DYNAMIC – Clocks are used to maintain the data storage. Memory will be lost if the refresh clock is stopped.

Random-access memories can also be defined as:

- Fully-decoded Memories – A binary address determines the location in which the write or read operation is performed.
- Two-Dimensional Decode – The address of the word is given by an X-Y select.

For small systems, fully-decoded memories are easier to use. However, the speed of a fully decoded random access memory is about 6 times less than the speed of an off-the-chip bipolar decode X-Y select memory. Besides applications for large systems the same decode section may be used for several MOS chips, making the X-Y select type of RAMs much more appealing for cost, speed, and power dissipation considerations.



SINGLE RAM CELL AND ADDRESS GATING

DYNAMIC MEMORY CELL (WITHOUT ADDRESS GATING)

FEATURES

Whatever type of MOS RAM is considered, the following features are inherent:

- Non Destructive Read Out — In an MOS RAM the reading of information does not affect the content stored. So it is not necessary to do a Write after every Read operation as is normal in magnetic memories. This is why the important parameter in an MOS memory is the access time rather than cycle time.
- Speed — Speeds of 200 ns with separate decoding, or 1 microsecond with decoding on the chip are typical.
- Power Dissipation — Power dissipation is typically one-tenth mW per bit.
- Flexibility — MOS memories are available in much smaller sizes then the equivalent core memories. The memory configuration is very flexible and can be altered without appreciably increasing the basic price.
- Environmental Characteristics (temperature range, mechanical, etc.) — Semiconductors are able to work in much more rugged environment then cores with much greater reliability.
- Cost — MOS Memories are already more economical than magnetic memories cores for small and medium size systems. Mass assembly techniques, such as beam lead MOS devices are being used to manufacture MOS memory systems and to further reduce the cost.

TI DEVICES

TI produces two MOS memory elements:

- TMS 4003 JR – 256-bit high-speed random-access memory (with separate decode)
- TMS 4000 JC – 128-bit content addressable (associative) memory.

TMS 4003 JC – 256-bit high-speed random-access memory

The TMS 4003 JC is a direct-address memory having 16 X-address and 16 Y-address lines. Any one of the 256 bits in the memory can be selected at a time by driving one X- and one Y-address line in coincidence. Sensing the logical state of the selected bit is achieved by differentially observing two outputs D_0 and D_1 digit lines. These same digit lines are also used to write information into an addressed bit. A block diagram of the TMS 4003 JC is shown below.

No clock signals are required to operate the TMS 4003 JC or retain information. Such a design is referred to as static distinguished from dynamic which requires the continuous application of single or multiple clock signals to function properly.

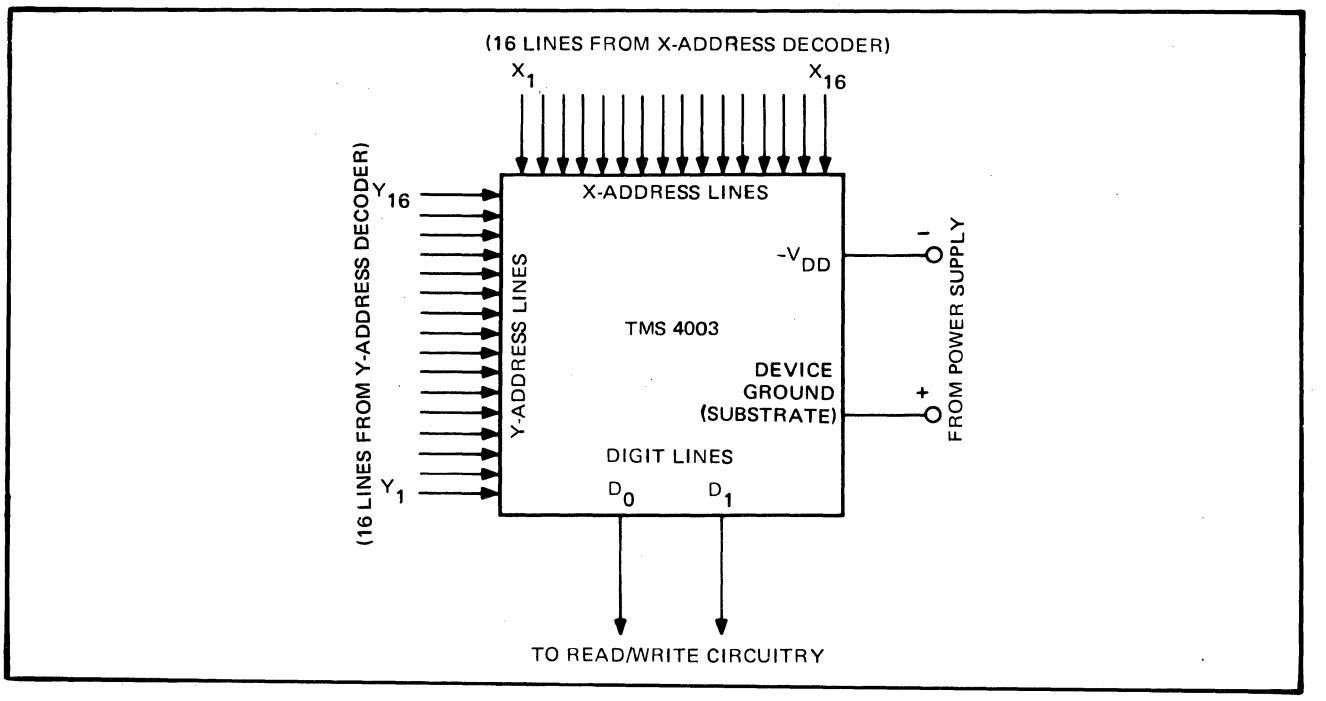
The memory organization of the TMS 4003 JC is referred to as 256-words-by-1-bit, since an address can only select one bit at a time. Larger memory systems can be constructed using this 256 x 1 memory as a basic cell.

Paralleling address lines can increase word size. For example, if eight memories were connected by tying their respective X- and Y-address lines together, a 256-word by 8-bit memory would be formed. A single X-Y address applied to this system would produce eight separate digital outputs.

The number of words can be increased by paralleling digit lines. For instance, to make a 1024-word by 1-bit memory plane, four 256 x 1 memories are used, resulting in 32 X-address and 32 Y-address lines and a single output consisting of two digit lines.

Memory planes like the one described can be paralleled in the same manner as individual memories. If eight 1024 x 1 planes, for example, had their corresponding X- and Y-address lines connected together, a 1024 x 8 memory system would result. A total of 32 TMS 4003 JC MOS RAMs would be necessary for such a system. Even larger systems are possible, the ultimate size being limited by the drive capabilities of the external address and write circuitry.

DESCRIPTIVE BLOCK DIAGRAM OF THE TMS 4003 MOS RAM



TMS 4000 JC — 128-bit content-addressable memory

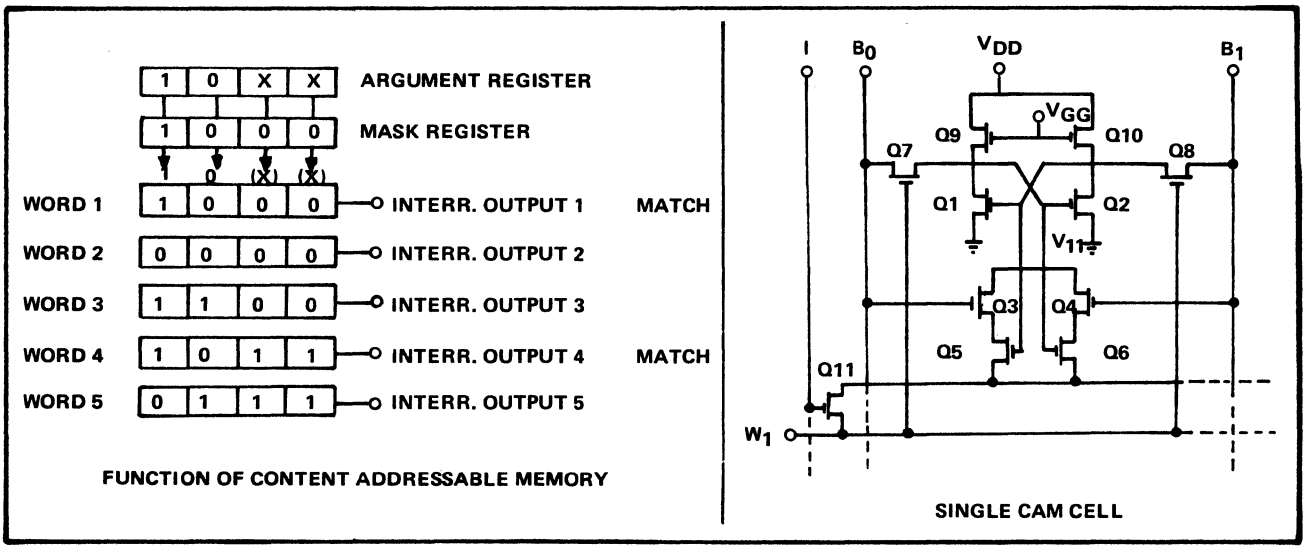
This device is a 128-bit content addressable memory organized as 16 words of 8 bits.

A content-addressable memory (or CAM, also referred to as associative memory) is a storage medium that can be accessed by searching for data content. To cite a simple example, consider the four-word, four-bits-per-word memory. Suppose our problem is to find all words that contain the data:

A = 1 or 0 (i.e., don't care)
B = 1
C = 0
D = 1 or 0

The conventional approach to solving this problem is to retrieve word 1 from memory, operate upon word 1's data to see if it matches the criteria, then retrieve word 2, operate upon word 2's data, etc., until all words have been searched. It is obvious that this conventional approach is quite time-consuming. Using the content-addressable memory to be described here, however, all words are simultaneously tested for the condition X10X where X represents the don't care. Associated with each word is an interrogate output which gives an output signal if the data contained in that word matches the information that the memory is being interrogated for. The next step could be to simply count how many of the words matched; or, the next step could be to sequentially "read out" the words which matched so as to find out what data those words held in bits A and D.

The concept of a content-addressable memory has been around for many years but has not previously been practical because of cost. However, the performance and economics of MOS integrated circuits now make the concept highly desirable from both technical and cost standpoints. MOS integrated-circuit technology has finally made practical the content-addressable memory.



A content-addressable memory (CAM) is one in which the words it contains can all be matched simultaneously against an argument word and outputs given wherever a true match is obtained. Each word has a Write input which can also be used to interrogate that word for a match. Two bit lines run through each column of cells allowing the word data to be written in. They may also be used for reading the contents of a word or for masking parts of the argument word where a Don't Care state exists.

In the basic CAM cell transistors, Q_1, Q_2, Q_9 and Q_{10} comprise a flip-flop for data storage. Q_7 and Q_8 are selection transistors which, when turned ON by the application of a negative voltage to the W line, connect the flip-flop nodes to the B_0 and B_1 bit lines. When the W line is at a 0, Q_7 and Q_8 are OFF isolating the flip-flop from the bit lines. Transistors Q_3, Q_4, Q_5, Q_6 and Q_{11} perform the INTERROGATE logic. For this mode each W lines is grounded through a small resistor and Q_{11} is turned ON. Transistors Q_3, Q_4, Q_5 and Q_6 compare the state of the memory cell flip-flop with the voltages externally applied to the bit lines. Thus the Word lines are controls for Write and Read operations but outputs for the Interrogate operation. The Bit lines are inputs for Write and Interrogate but outputs for Read.

TMS4000JC
high-speed content-addressable memory
preliminary information

FEATURING

- Static operation
- Nondestructive readout and interrogation
- High-speed operation – 250 ns typical system cycle time
- Low standby power dissipation
- Masked write and interrogation capability
- Low threshold technology

description

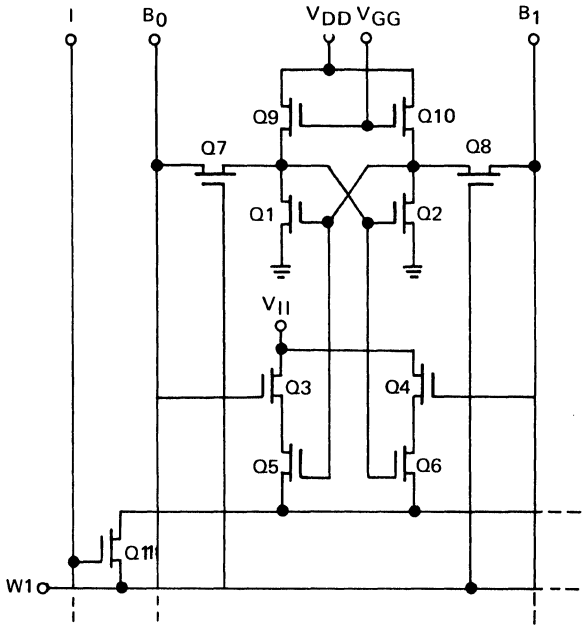
The TMS 4000 JC is a high-speed content-addressable memory organized as 16 eight-bit words. The entire device is constructed on a single monolithic chip using low-threshold MOS P-channel enhancement-mode transistors. Active-element design permits nondestructive readout and interrogation of memory contents. Bit lines can be wire-OR connected to obtain memory planes greater than 16 words. Word lines can be wire-OR connected to achieve word lengths of greater than eight bits per word. Selection of a given word for reading or writing is accomplished by connecting the selected word line to a negative voltage while holding all other word lines at ground. The common interrogation control 1, when returning to a negative voltage, allows all sixteen words to be interrogated simultaneously.

Memory writing is accomplished by addressing a desired word and bringing the appropriate bit lines to ground while holding the other bit lines at a negative potential. If both bit lines of a selected bit are held at the negative potential, the information in the bit will be unchanged during a writing cycle. Masked writing can therefore be achieved.

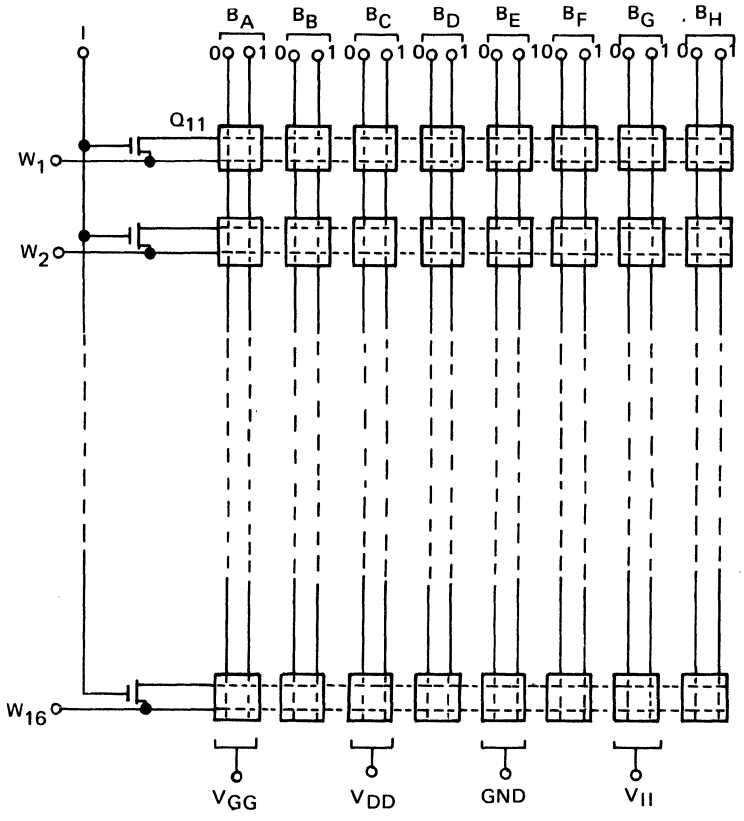
Reading each bit content of an addressed word requires sensing differential current between the two bit lines. Both lines should be held near a logic 1.

Interrogation of memory content is accomplished by activating the interrogation command I, bringing bit lines to appropriate voltages, and simultaneously sensing the current in each word line. If both bit lines of a particular bit are held at ground potential during an interrogation cycle, that bit will be excluded from the interrogation. If a word perfectly matches the interrogation information, no current will flow through the word lines. One or more mismatches will cause at least 200 μA to flow in the word line.

CONTENT-ADDRESSABLE MEMORY CELL



CONTENT-ADDRESSABLE MEMORY ORGANIZATION



logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

OPERATION	INPUT VOLTAGE				OUTPUT SIGNALS
	I	W	B_0	B_1	
Write 0	0	1	1	0	
Write 1	0	1	0	1	
Masked Write	0	1	1	1	
Read 0	0	1	1	1	Current in B_1 (200 μA minimum)
Read 1	0	1	1	1	Current in B_0 (200 μA minimum)
Interrogate 0	1	0	1	0	Current in W indicates mismatch (200 μA min.)
Interrogate 1	1	0	0	1	
Masked Interrogate	1	0	0	0	No current in W from this bit
Standby	0	0	X	X	(Note 1)

NOTE 1: X = 1 or 0 (don't care)

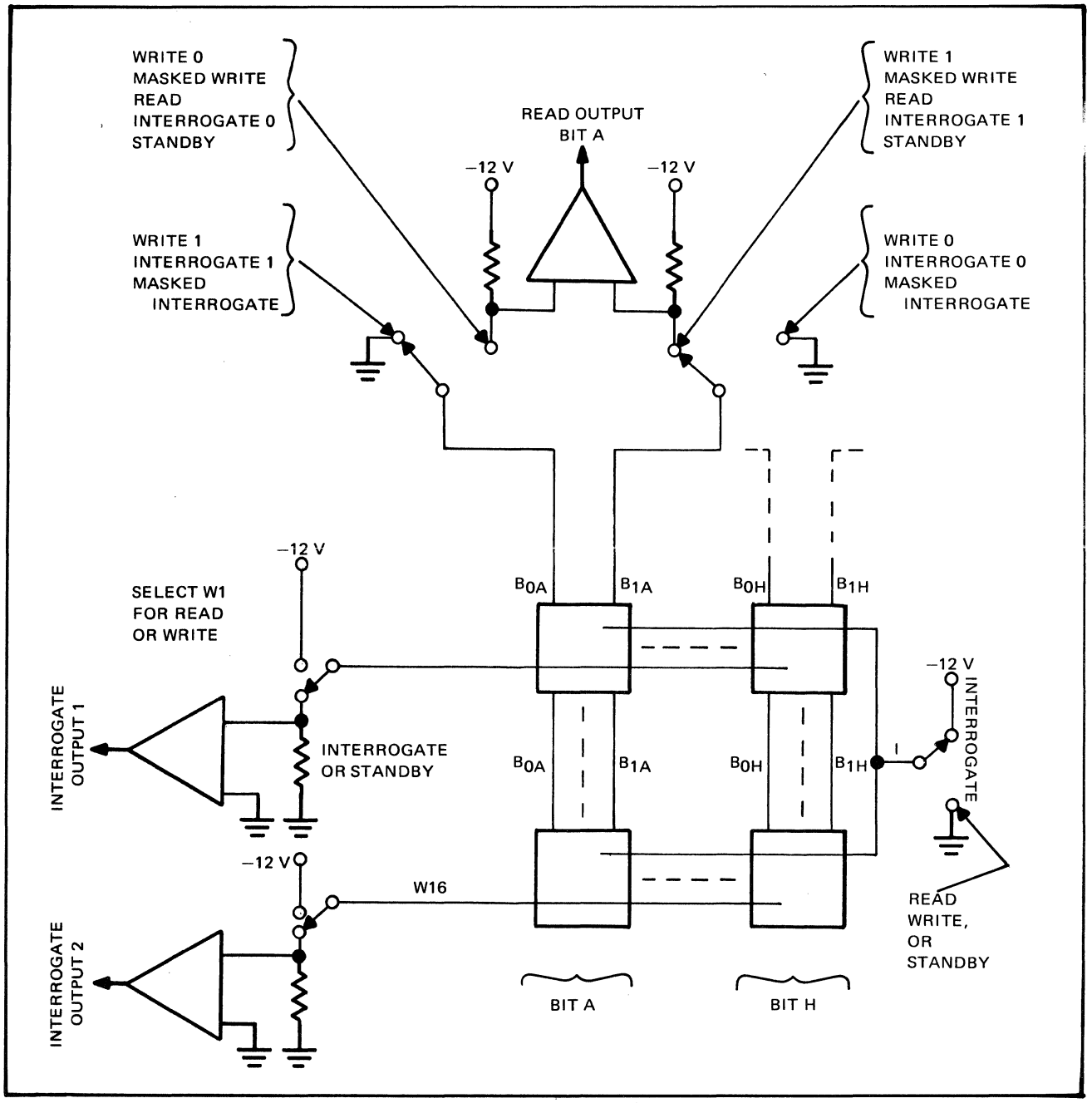
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −14 V
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{GG}	−11	−12	−13	V
Supply voltage V_{DD}	−11	−12	−13	V
Supply voltage V_{II}	−27	−3	−13	V
Write time (t_W)	60			ns
Settling time (t_s)	50			ns

content-addressable memory operational requirements



electrical characteristics (under nominal operating conditions at 25°C, unless otherwise noted)

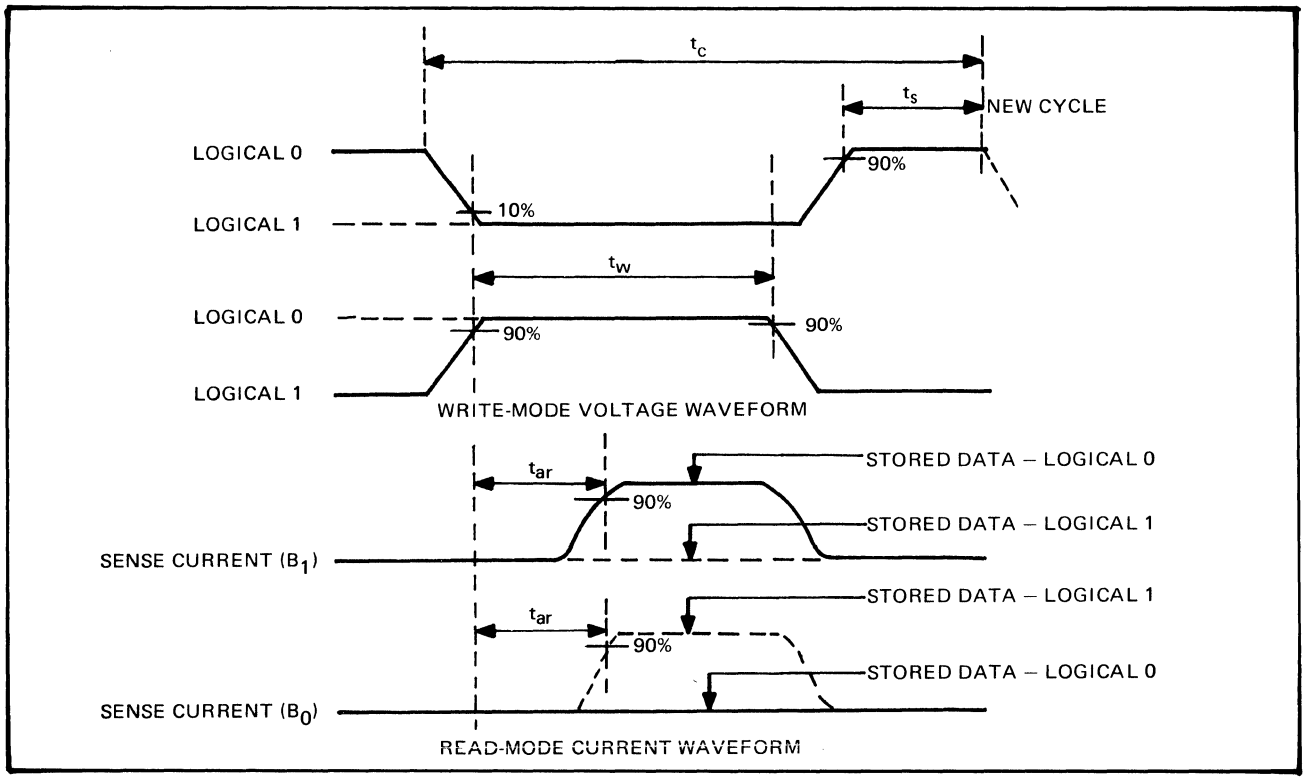
R_L = 100 Ω (See CAM operational requirements)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Read-mode sense current		Logic 0 stored in a bit cell	B_0			−10	μA
			B_1	−200	−400		
		Logic 1 stored in a bit cell	B_0	−200	−400		
			B_1			−10	
Interrogate-mode sense current		Matched				−10	μA
		One bit mismatched		−200	−400		
		All bits (8) mismatched			−2000	−3000	
I_B	Bit-line leakage current	16 in parallel @ −12 V				10	μA
I_W	Word-line leakage current	16 in parallel @ −12 V				10	μA
I_I	Interrogate line leakage current	At −12 V				100	μA
I_{DD}	Drain supply current				3.0	5.0	mA
I_{II}	Interrogation supply current per word	One bit mismatched		−0.2	−0.4		mA
		All bits (8) mismatched			−2.0	−3.0	
Total power dissipation		Standby			40	60	mW
		Read or Write				100	
		Interrogation				200	
C_B	Bit-line capacitance	V_B = 0 V,	f = 1 MHz		13		pF
C_W	Word-line capacitance	V_W = 0 V,	f = 1 MHz		12		pF
C_I	Interrogate-line capacitance	V_I = 0 V,	f = 1 MHz		40		pF

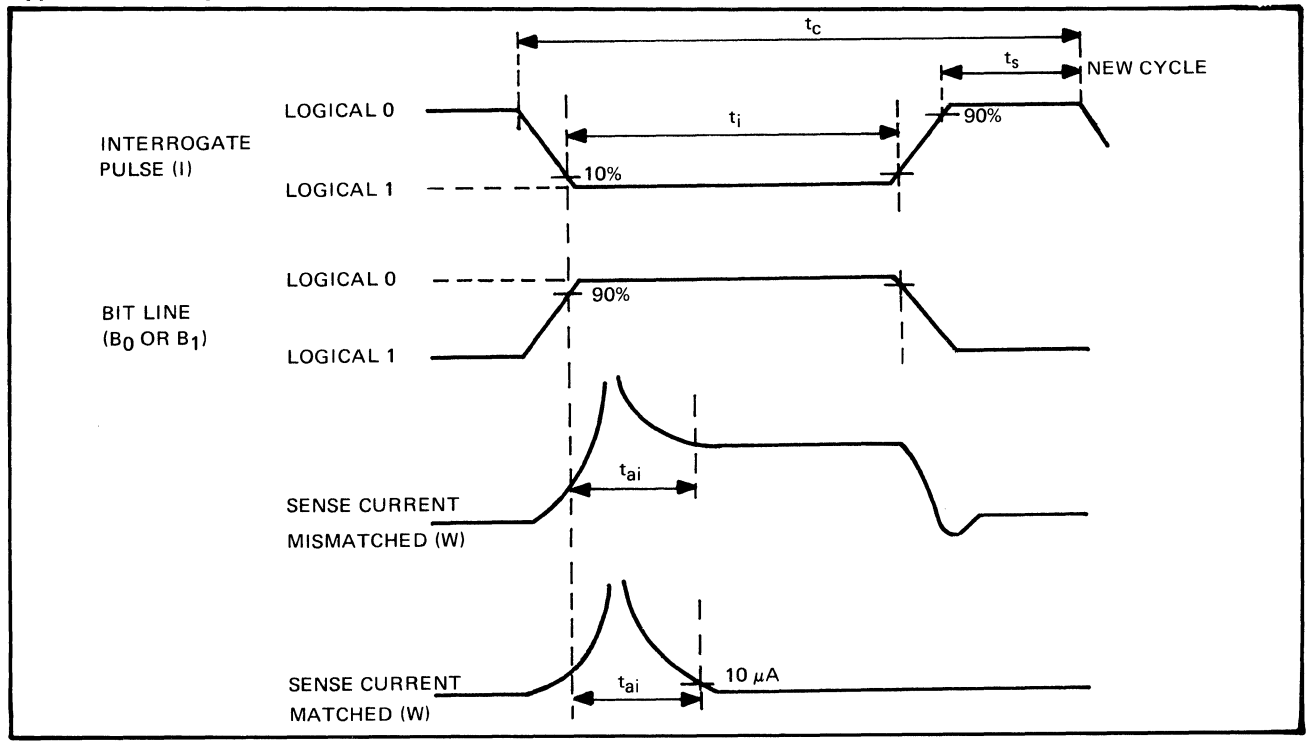
switching characteristics (under nominal operating conditions at 25°C, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_s	Settling time				50	ns
t_{ai}	Interrogate access time			50	80	ns
t_{ar}	Read access time			30	60	ns

typical switching waveforms (read and write)

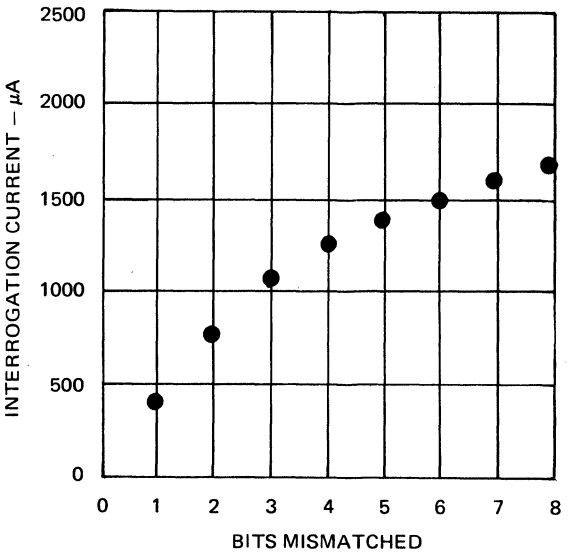


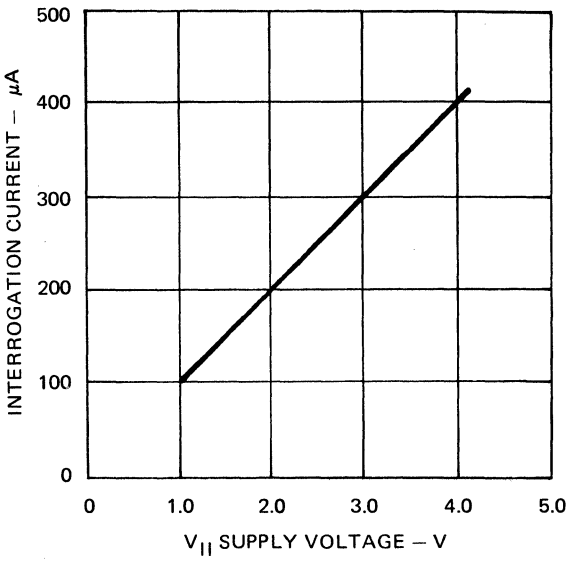
typical switching waveforms (interrogation)



Interrogation Current vs Number of Bits Mismatched, And vs V_{II} Supply Voltage

($R = 100\ \Omega$, $V_{DD} = -12$ V, $V_{GG} = -12$ V, Logical 1 = -12 V, $T_A = 25°C$)





TMS4000JC
high-speed content-addressable memory

mechanical data

The TMS 4000 JC is mounted in a 40-pin hermetically sealed, dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

pin configuration

PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	0 } B_6	11	W_8	21	1 } B_3	31	W_9
2	1 }	12	W_6	22	0 }	32	W_{11}
3	0 } B_8	13	W_4	23	1 } B_1	33	W_{13}
4	1 }	14	W_2	24	0 }	34	W_{15}
5	I	15	V_{GG}	25	V_{DD}	35	NC
6	GND	16	NC	26	NC	36	V_{II}
7	W_{16}	17	1 } B_5	27	W_1	37	0 } B_2
8	W_{14}	18	0 }	28	W_3	38	1 }
9	W_{12}	19	1 } B_7	29	W_5	39	0 } B_4
10	W_{10}	20	0 }	30	W_7	40	1 }

TMS4003JR
256-bit random-access memory

FOR MEMORY APPLICATIONS REQUIRING
HIGH-SPEED READ/WRITE CAPABILITY

- Nondestructive Readout
- Static Operation
- System Access Time Under 200 ns
- Low Power Dissipation

description

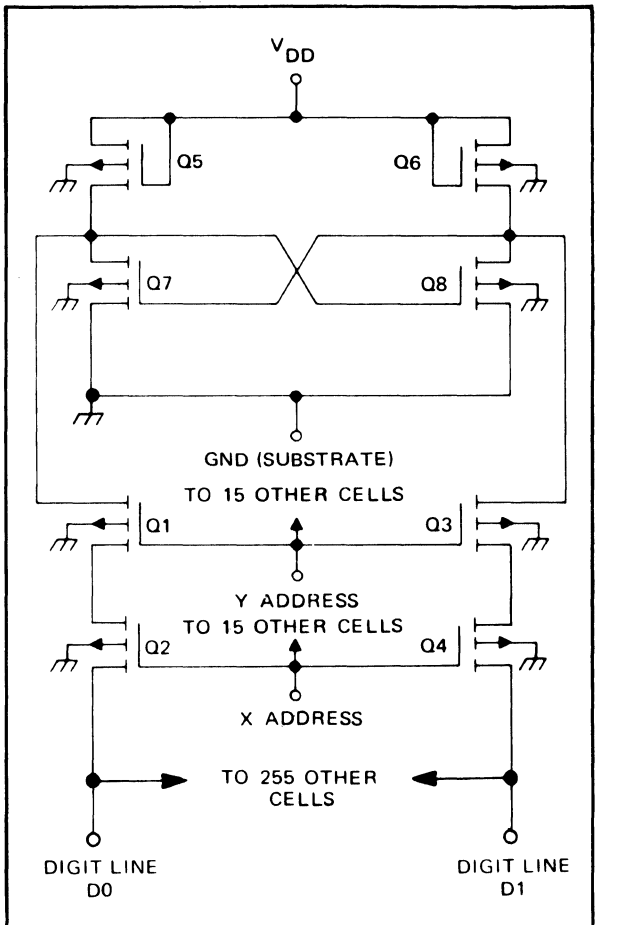
The TMS4003JR is a high-speed random-access memory consisting of 256 cross-coupled flip-flops organized as 256 one-bit words. The entire device is constructed on a single monolithic chip using thick-oxide techniques to produce MOS P-channel enhancement-type transistors. Active-element design permits nondestructive readout, since addressing each bit tends to reinforce its existing state. Digit lines can be wire-OR connected to obtain memory planes greater than 256 words. External decoding circuitry can be used for additional planes to achieve desired word length. Selection of a given bit for reading or writing is accomplished by the coincident addressing of one of 16 X lines and one of 16 Y lines. These two lines are taken to V_{DD} while all other X and Y lines are held at ground.

Memory writing is accomplished by externally addressing the desired cell and bringing the appropriate digit line to ground while holding the other digit line at its nominal V_{DD} potential.

Reading an addressed cell requires sensing a differential current between the two digit lines. Both digit lines should be held near their nominal value of V_{DD}. This causes addressing transistors Q1, Q2, Q3, and Q4 to act as additional load resistors in parallel with standby load resistors Q5 and Q6, (see Figure 1). Depending on the flip-flop state, current will flow in one of the digit lines and not the other.

Maximum speed of the circuit is limited by the propagation delay of the Y address voltage through a series of P-diffused tunnels. The write or read cycle time, including this delay and the TTL address-decode delay, will be under 200 nanoseconds, (see Figure 2).

Power dissipation is typically 0.6 mW per bit when the memory is operated with an 18-volt d-c power supply. Significantly lower average power dissipation may be obtained without sacrifice of system performance by synchronously or asynchronously pulsing the V_{DD} power supply. This feature is a result of the temporary data storage provided by the gate capacitance of transistors Q7 and Q8.



CELL SCHEMATIC (1 OF 256 CELLS)

FIGURE 1

logic

Logic levels for this memory are defined in terms of standard NEGATIVE LOGIC where:

−16 V to −20 V = LOGICAL 1
+0.3 V to −2 V = LOGICAL 0

OPERATING MODE	ADDRESS LINES OF SELECTED CELL		DIGIT-LINE TERMINALS	
	X	Y	D1	D0
Read	1	1	1	1
Write a zero	1	1	1	0
Write a one	1	1	0	1

A selected cell has both its X and Y address lines at logical 1. During read and write operations, only one cell should be selected at a time. An unselected cell is a cell which has at least one of its address lines at logical 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −22 V
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	−16	−18	−20	V
Write access time, t_{aw} (See Note 1 and Figure 3)	80			ns
Write pulse width, t_{pw} (See Figure 3)	30			ns

NOTE: 1. Write access time is the delay between the application of address voltages at the X and Y inputs and the start of the write pulse. Premature application of the write pulse may cause undesired writing into cells other than the addressed cell.

operating characteristics (unless otherwise noted T_A = 25°C)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Read-mode sense current	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 0 stored in cell nm	D0	−200	−400		μA
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−200	−400		
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 0 stored in cell nm	D0	−300	−500		
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−300	−500		
Address-line current (16 lines in parallel)	V_X or $V_Y = -20$ V, $V_{in(D0)} = V_{in(D1)} = V_{DD} = 0$ V				−10	μA
Total power dissipation	One cell addressed, $V_{DD} = -18$ V			150	300	mW
	One cell addressed, $V_{DD} = -20$ V, $T_A = -55$°C				500	

operating characteristics, continued (unless otherwise noted V_{DD} = −18 V, T_A = 25°C)

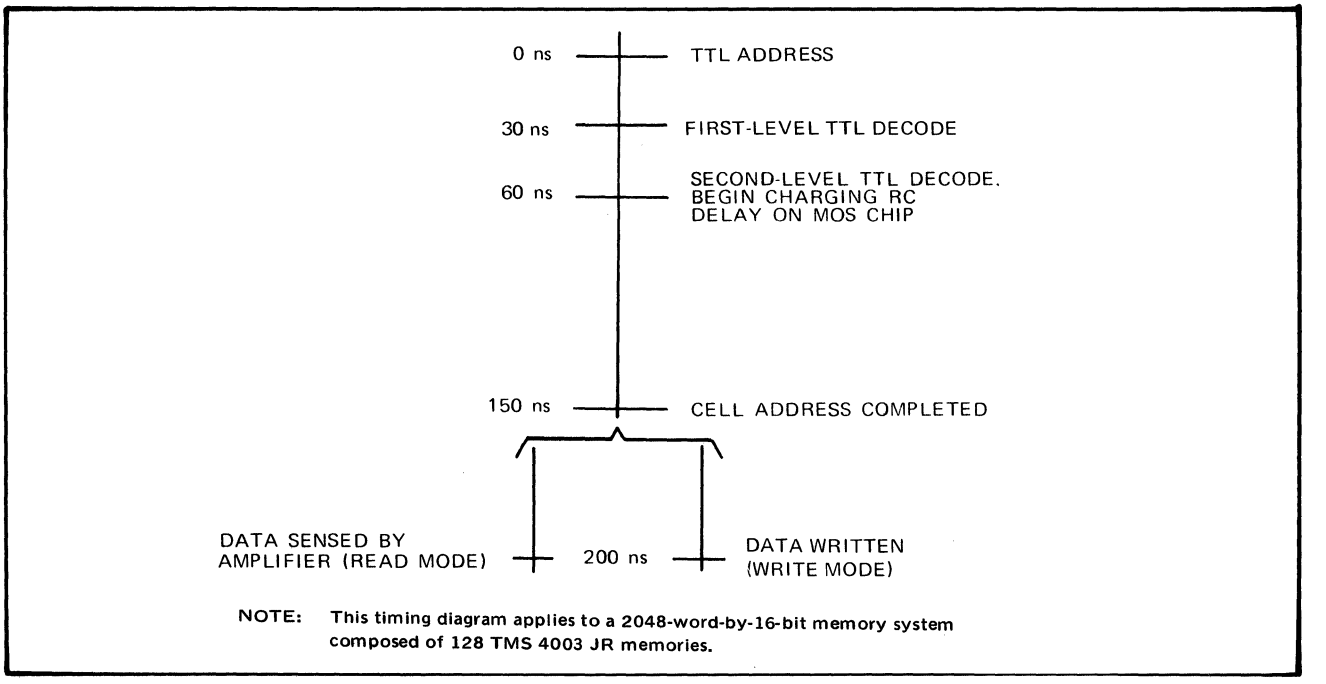
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitance between digit-line terminal and substrate	$V_{in(D0)} = V_{in(D1)} = 0$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		50		pF
	$V_{in(D0)} = V_{in(D1)} = -18$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		30		
Capacitance between digit-line terminal and physically adjacent address terminal (D0-to-X2 or D1-to-Y1, see Note 3)	$V_{in(D0)} = V_{in(X2)} = 0$ to −18 V, $V_{in(D1)} = V_{in(Y1)} = 0$ to −18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between address terminal and substrate	$V_X = V_Y = 0$ to −18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between V_{DD} terminal and substrate	$V_{DD} = V_X = V_Y = 0$ to −18 V, f = 140 kHz, See Note 2		50†		pF
Read access time, t_{ar} (see Note 4)	See Figure 3, R_L = 51 Ω		30	60	ns

NOTES: 2. All capacitances are measured with all other elements a-c grounded.

3. Typical capacitance between digit-line terminals and all other address lines will be less than that shown for the adjacent address lines.

4. Read access time is the delay between the application of address voltages at the X and Y inputs and the availability of differential current between the digit lines.

†These typical values are the average for the voltage range 0 to −18 V.



NOTE: This timing diagram applies to a 2048-word-by-16-bit memory system composed of 128 TMS 4003 JR memories.

FIGURE 2 – TYPICAL SYSTEM CYCLE TIME

PARAMETER MEASUREMENT INFORMATION

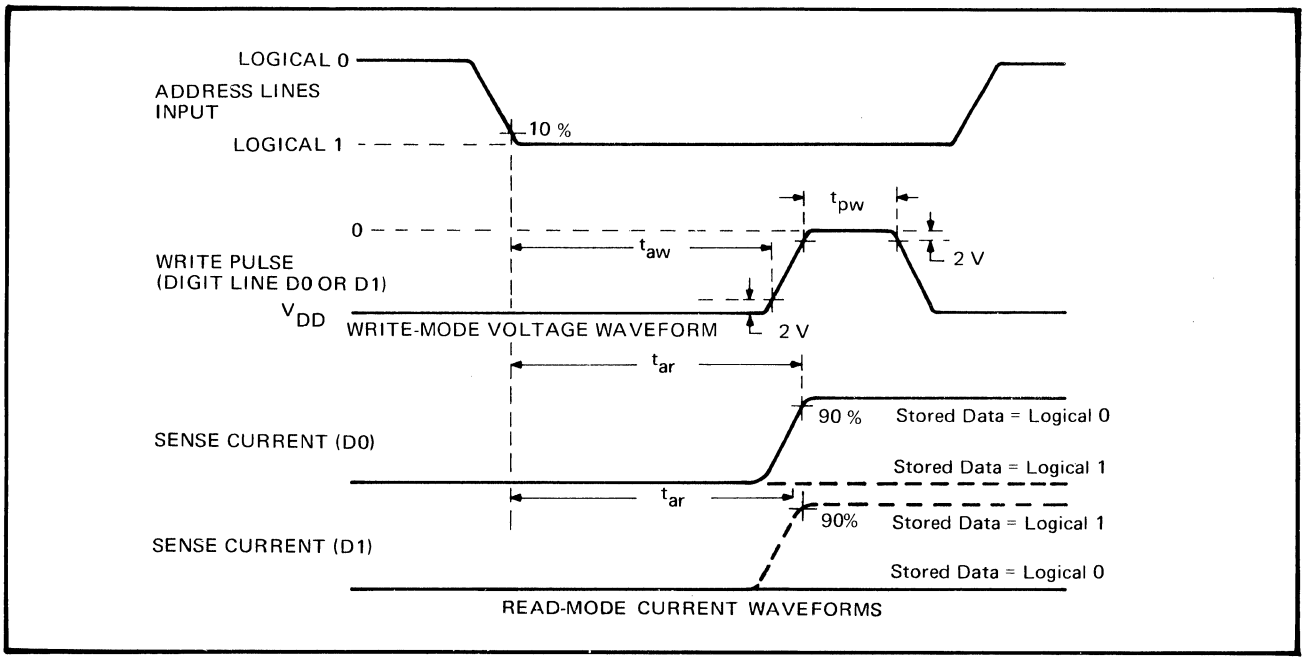


FIGURE 3 – TYPICAL SWITCHING WAVEFORMS

TYPICAL CHARACTERISTICS

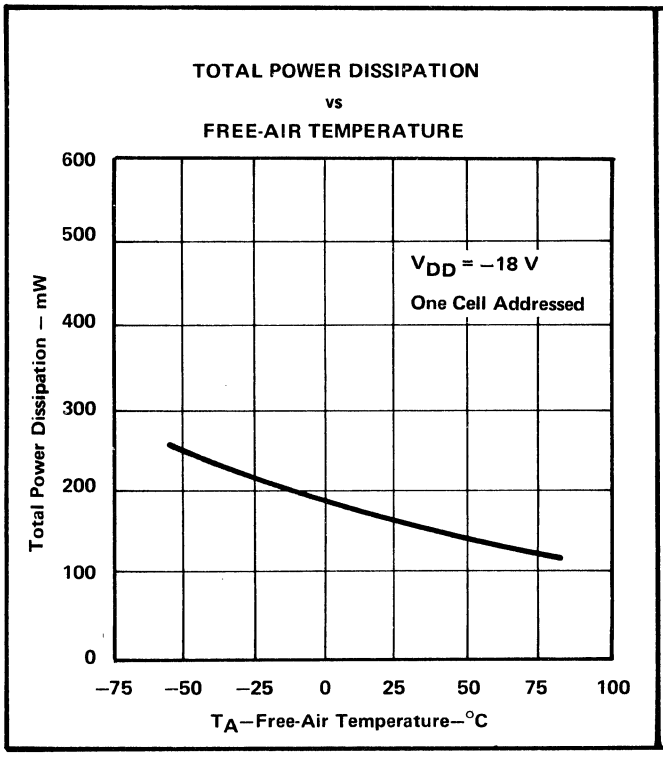


FIGURE 4

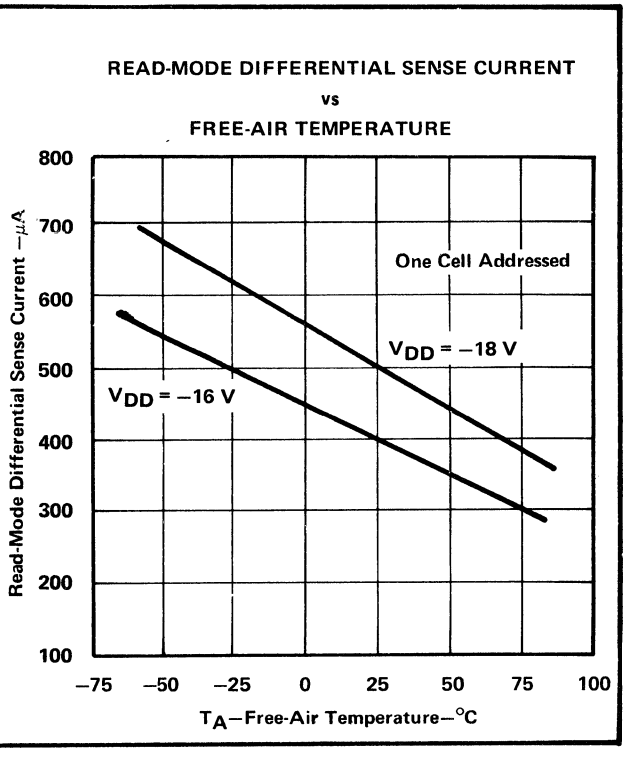
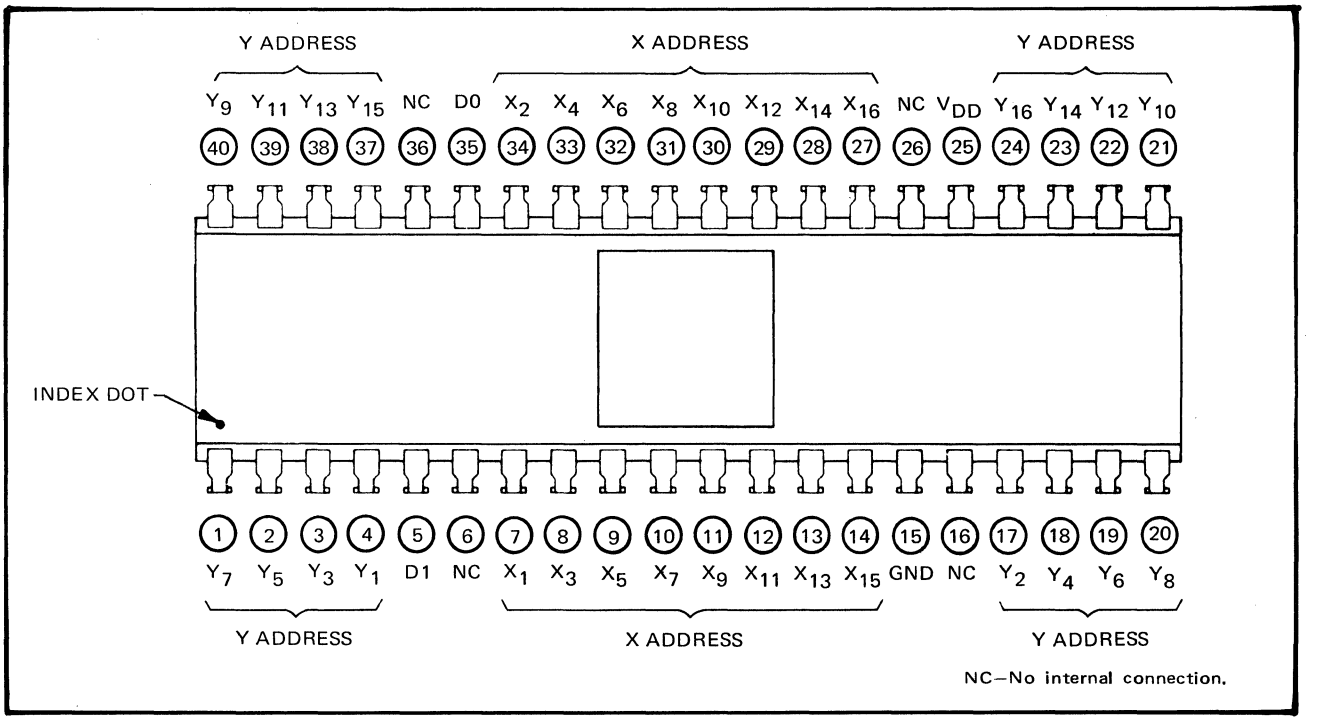


FIGURE 5

TMS4003JR
256-bit random-access memory

mechanical data and pin configuration

The TMS 4003 JR is mounted in a 40-lead, hermetically sealed, dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is intended for insertion in mounting holes of 0.024 ± 0.002 inch diameter which are spaced 0.600 inch between row centerlines. Typical package weight is 4.2 grams.



TYPICAL APPLICATION DATA

An actual negative supply for V_{DD} is not necessary. The V_{DD} terminal can be returned to system ground with a positive potential equal in magnitude to the voltage specified for V_{DD} applied to device ground (pin 15). This simplifies external circuitry, particularly when using bipolar systems such as TTL. The MOS device ground V_{SS}, is nominally +18 V while the V_{DD} terminal is at system ground. Addressing occurs when one X-address line and one Y-address line are pulled to ground. Unselected address lines should remain at V_{SS}.

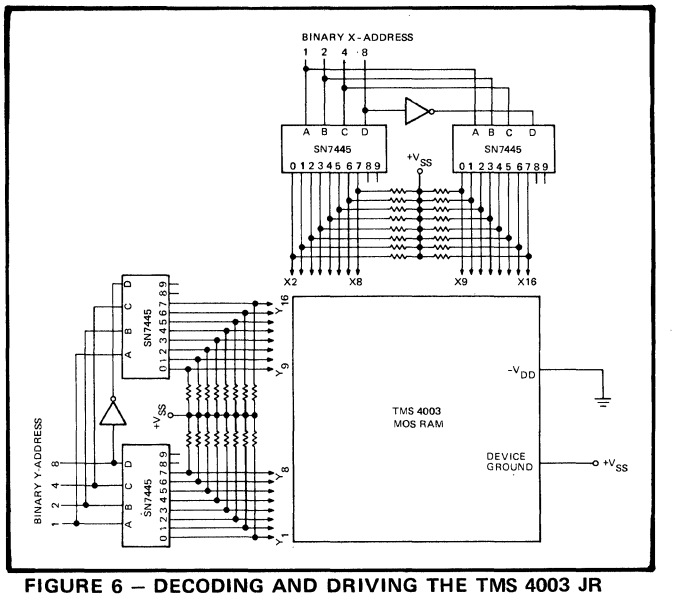
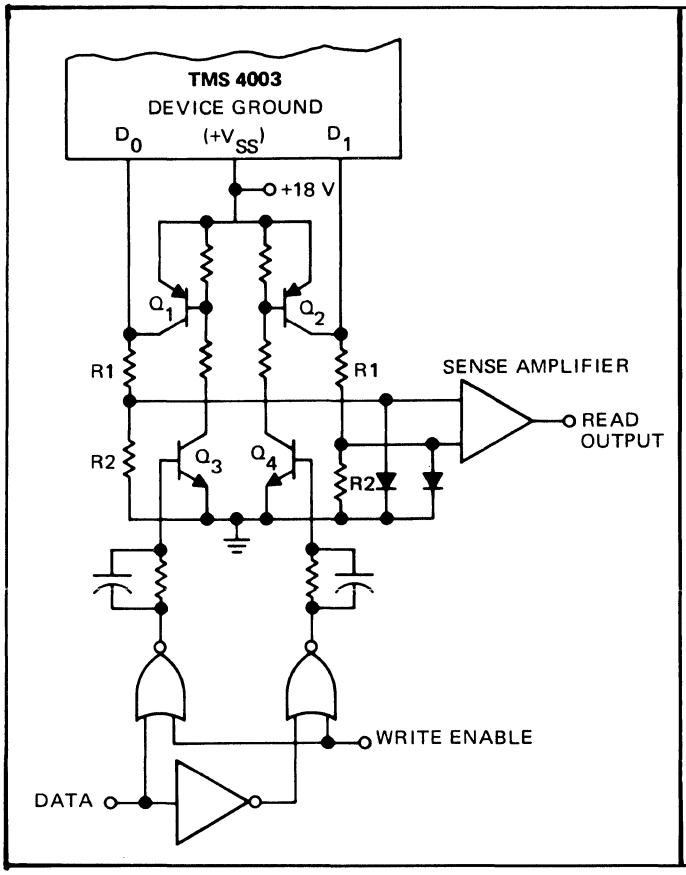


FIGURE 6 – DECODING AND DRIVING THE TMS 4003 JR BY USE OF THE SN74154

TYPICAL APPLICATION DATA (Continued)

TMS 4003 JR
MEMORIES WITH
PARALLEL CONNECTED
DIGIT LINES

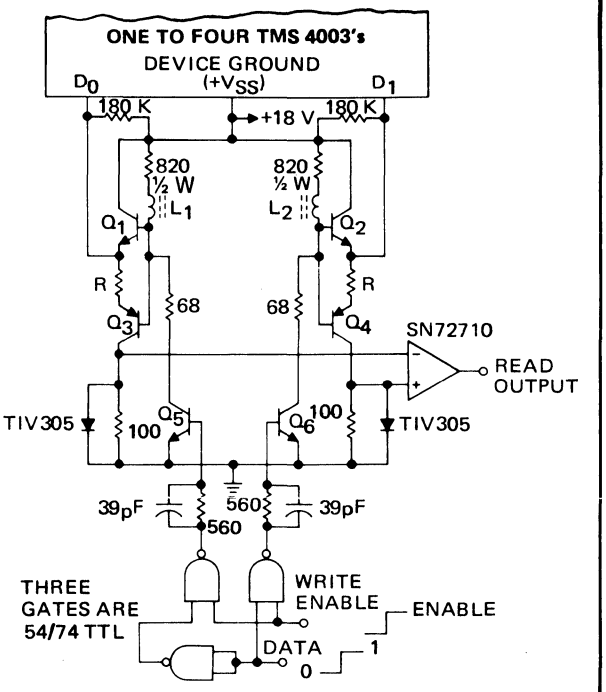


CIRCUIT COMPONENTS INFORMATION

Q1 and Q2: 2N3629
Q3 and Q4: 2N3014

FIGURE 7 – BASIC READ/WRITE CIRCUIT
LIMITED TO LOW-SPEED OPERATION

TMS 4003 JR
MEMORIES WITH
PARALLEL CONNECTED
DIGIT LINES



CIRCUIT COMPONENTS INFORMATION

L1 and L2: 2 1/2 T, No. 30 wire on Ferrite Bead (Allen-Bradley No. T0 135G144A or equivalent)
Q1, Q2, Q5, and Q6: 2N3014
Q3 and Q4: 2N3829

$$\text{R1 and R2: } \frac{180\ \Omega}{\text{No. of TMS 4003 JR memories}}$$

FIGURE 8 – HIGH-SPEED READ/WRITE CIRCUIT

TMS5700JC
digital differential analyzer element

preliminary information

description

The TMS 5700 JC is a monolithic, integrated, digital, differential analyzer element designed with MOS P-channel enhancement-mode transistors. Using this device in conjunction with a dual shift-register (such as TMS 3000 LR of 2 x 25 bits, or TMS 3001 LR of 2 x 32 bits) sets up a complete digital differential analyzer integrator of ternary type, designed to perform rectangular integration in a parallel operation set.

The block diagram shows TMS 5700 JC connected to a dual static shift register. Y and R adders are two full adder-subtractors, the carries of which are internally stored in dc flip-flops; hence the internal data are not lost during dc operation. Initial conditions Y_o and R_o are loaded in the registers when load input is set to 1, while the sums $Y+\Delta Y$ and $R+Y\Delta X$ are inserted when load input is 0. Two logic circuits are included in the R adder, detecting overflows and underflows of the R register; overflows and underflows are then stored in the dc flip-flops $\Delta Z+$ and $\Delta Z-$, which remain high or low during the entire next word time.

For dc operation, ϕ_1 must be a logic 0 and ϕ_2 must be a logic 1.

The numbers in the shift-registers are in serial form, least significant bit (LSB) first, and sign bit (P_o) last. Negative numbers are in two's complement form. The true length of each Y is chosen by appropriate scaling, i.e., by inserting a single 1 into the scale input at the time of the LSB of that number. Two ways of operating the R adder are possible – biased or unbiased roundoff error. The appropriate R output is connected to the input of the R register.

The DDA integrator can be used to solve differential equations; it can also be used in desk calculators and control systems.

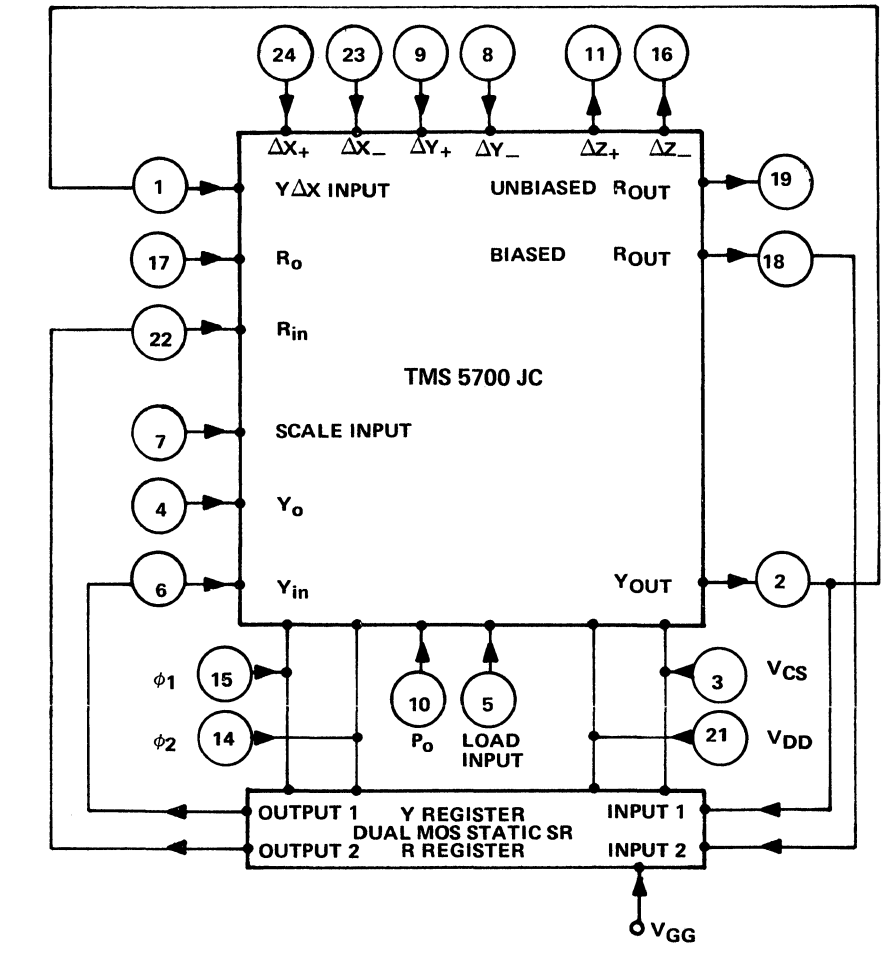
logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

block diagram



NOTES ON OPERATION:

- INPUTS MUST BE AVAILABLE DURING THE ENTIRE DECISION TIME.
- ALL UNUSED INPUTS MUST BE GROUNDED DURING OPERATION.
- PINS NOT REFERENCED TO ARE LEFT ELECTRICALLY OPEN.
- THE LOAD RESISTANCES MUST NEVER BE LESS THAN 5 kΩ.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Clock and data input voltage ranges (See Note 1)	−30 V to 0.5 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal (V_{SS}).

TMS5700JC
digital differential analyzer element

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Drain power supply V_{DD}	−11	−14	−16	V
Input logic 0	+0.3	0	−2	V
Input logic 1	−11	−14	−16	V
Clock logic 0	+0.3	0	−2	V
Clock logic 1	−26	28	29	V
Input pulse width ϕ_{pw}	1.2			μs
Clock pulse width ϕ_{pw1}	1.2		10	μs
Clock pulse width ϕ_{pw2}	0.8			μs
Clock delay	0.8		10	μs
Clock rise and fall time (10% to 90%)			0.1	μs
Clock repetition rate	0		500	kHz

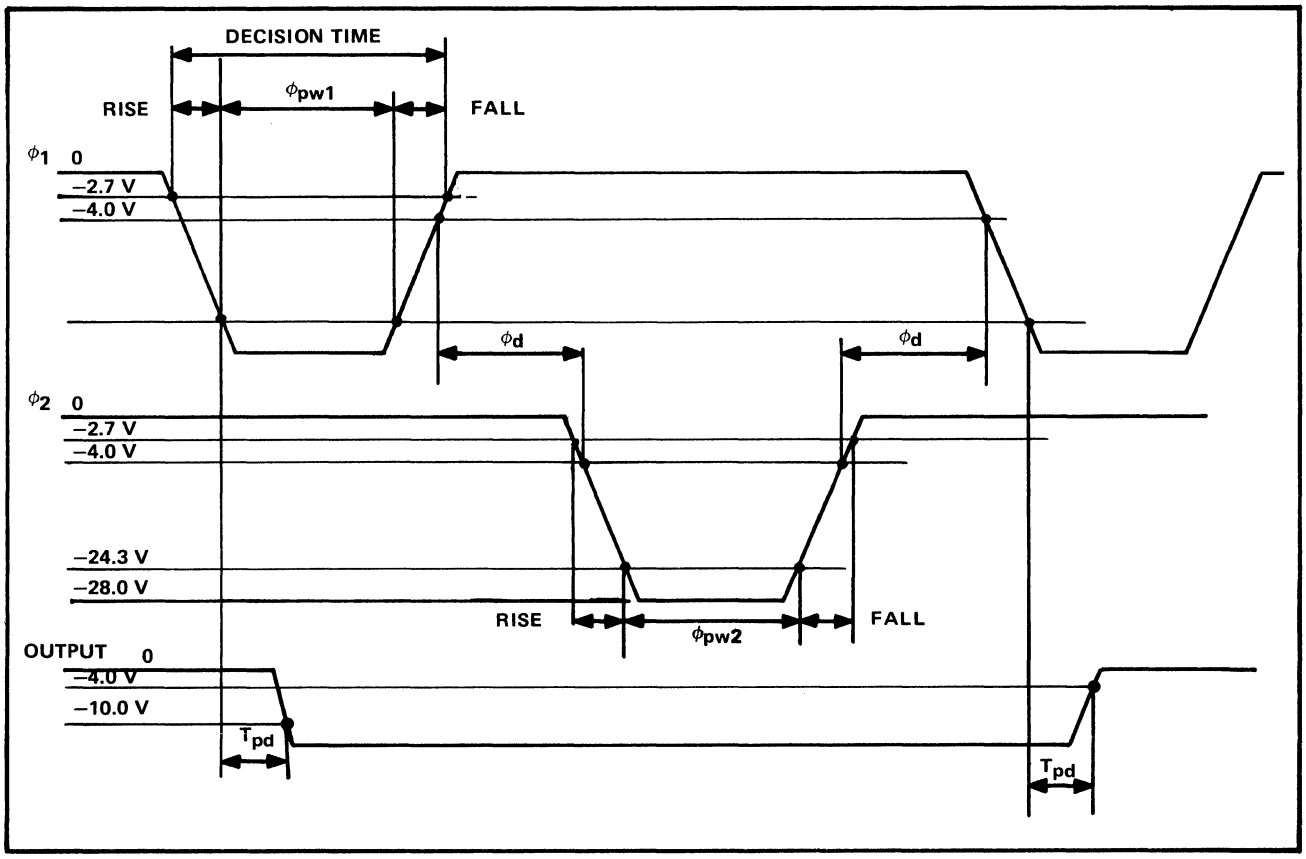
electrical characteristics (at nominal operating conditions and 25°C unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNITS
$I_{\phi(1)}$	Clock input current	ϕ_1 = 1,	ϕ_2 = 0		2		mA
$I_{\phi(2)}$	Clock input current	ϕ_1 = 1,	ϕ_2 = 1			100	μA
$V_{out(0)}$	Output logic 0	R_L = 10 MΩ,	C_L = 20 pF		−0.5	−1	V
$V_{out(1)}$	Output logic 1	R_L = 10 MΩ,	C_L = 20 pF	−11	−12		V
Z_{out}	Output impedance	V_{SS} (output at logic 0)			2		kΩ
$V_{out(1)}$	Output voltage logic 1	R_L = 20 kΩ		−10	−11		V
$V_{out(1)}$	Output voltage logic 1	R_L = 10 kΩ		−7.5	−10.5		V
I_{dd}	Power supply current	f = 500 kHz			4		mA
P	Power dissipation				120	300	mW
C_{in}	Input capacitance				3		pF
$C_{clock(1)}$	Clock capacitance	ϕ_1	ϕ_1 logic 0		12		pF
$C_{clock(2)}$	Clock capacitance	ϕ_2	ϕ_2 logic 0		5		pF
	Input leakage current	V_{in} = 20 V				1	μA

switching characteristics (at 25°C and nominal operating conditions unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS
T_{pdy}	Propgation delay through Y adder (see timing diagram)		350		ns
	Propagation delay through Y and R adders in series (see timing diagram)		800	1150	ns

timing diagram



mechanical data

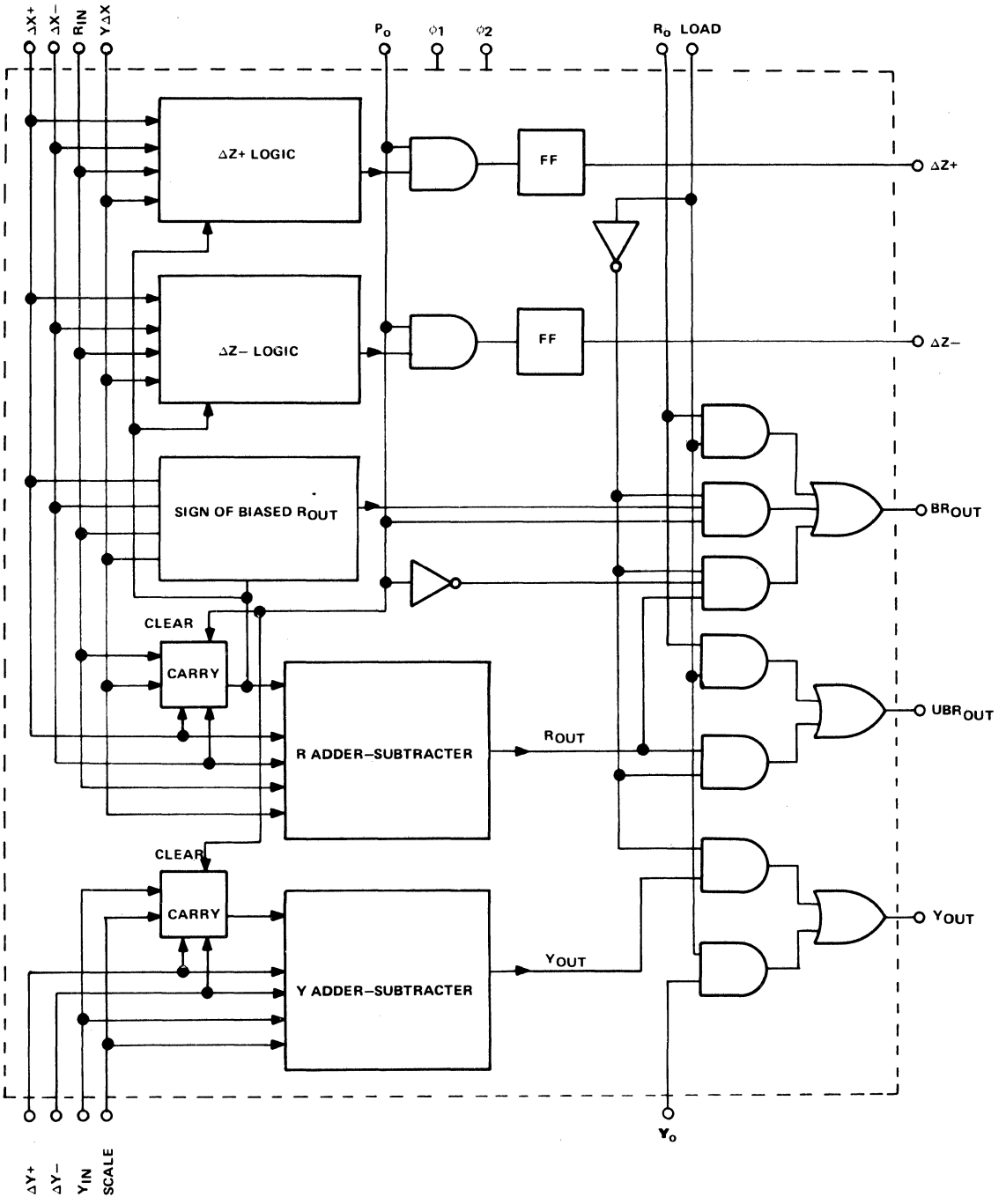
The TMS 5700 JC is mounted in a 24-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.600-inch centers.

pin configuration

NO.	FUNCTION	NO.	FUNCTION
1	YΔX input (YΔX)	13	No connection
2	Y adder output (Y_{out})	14	Clock (ϕ_2)
3	Ground (V_{SS})	15	Clock (ϕ_1)
4	Initial conditions input (Y_o)	16	Underflow output (ΔZ_)
5	Initial conditions load input (LOAD)	17	Initial conditions input (R_o)
6	Y adder input (Y_{in})	18	Biased R adder output (Biased R_{out})
7	Scale input (Scale)	19	Unbiased R adder output (Unbiased R_{out})
8	Y adder subtract input (ΔY_)	20	No connection
9	Y adder add input (ΔY_+)	21	Drain voltage (V_{DD})
10	Sign bit clock (P_o)	22	R adder input (R_{IN})
11	Overflow output (ΔZ_+)	23	R adder subtract input (ΔX_)
12	No connection	24	R adder Add input (ΔX_+)

TMS5700JC
digital differential analyzer element

logical diagram



TMS6000JR
common-source 10-channel analog switch for high-speed multiplexing applications

preliminary information

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line package
- $R_{DS(ON)} = 200\ \Omega$

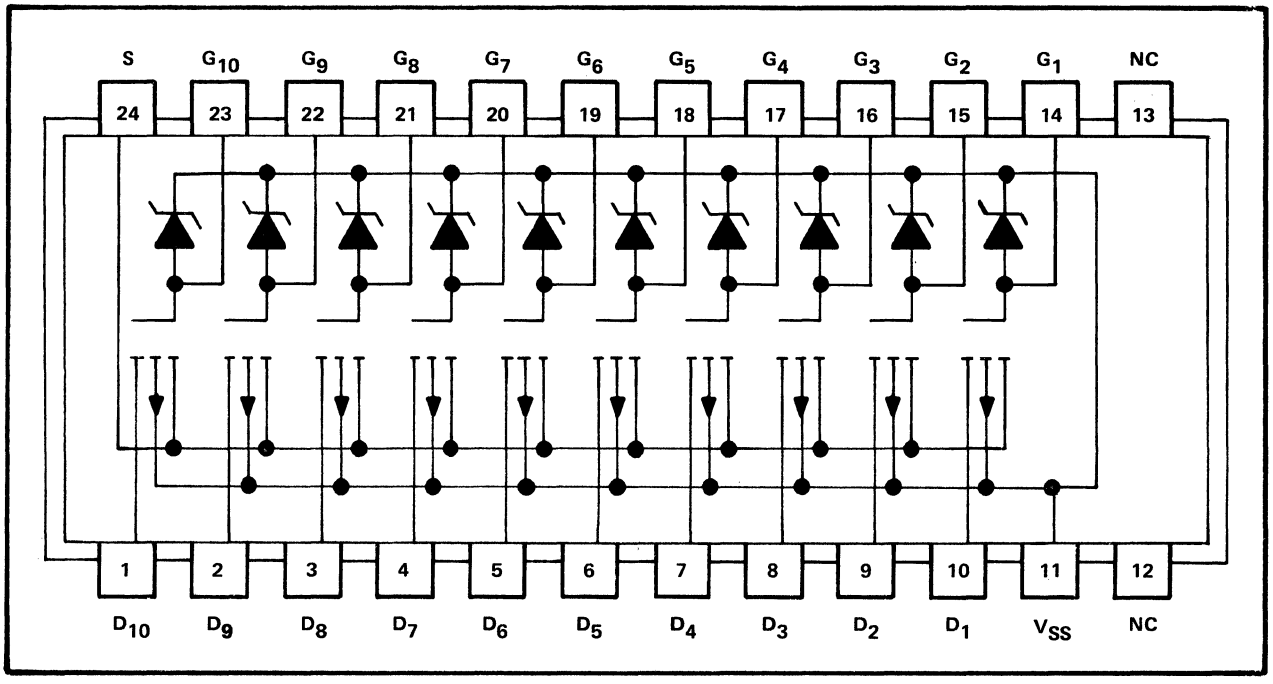
description

The TMS 6000 JR analog switch is a P-channel enhancement mode MOS monolithic integrated circuit. It consists of 10 MOS transistors having all 10 sources interconnected.

A gate input impedance greater than 10^{10} ohms coupled with low-source-off current, zero inherent offset voltage, and low on-state resistance ideally suits these switches for time-division multiplexing of analog and digital signals.

schematic and pin configuration

TOP VIEW



D = Drain
G = Gate
S = Source

V_{SS} = Substrate
NC = No Connection

The material herein is believed to be accurate and reliable; however, some parameters specified are derived from evaluation units and may change slightly after full characterization.

TMS6000JR
common-source 10-channel analog switch for high-speed multiplexing applications

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Drain-source voltage . . . . . −30 V
Gate-source voltage . . . . . −30 V
Gate-drain voltage . . . . . −30 V
Drain current . . . . . −50 mA
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$,	$V_{GS} = 0$ V	−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$,	$V_{DS} = 0$ V	−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$,	$V_{GD} = 0$ V	−30			V
I_{GSSF}	Gate-terminal forward current	$V_{GS} = -20$ V,	$V_{DS} = 0$ V		−0.05	−1	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V,	$V_{GS} = 0$ V			−3	nA
I_{SDS}	Zero-gate-voltage source current	$V_{SD} = -20$ V,	$V_{GD} = 0$			−6	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DS} = 0$ V,	$I_D = -10\ \mu A$	−2.5	−4	−6	V
$r_{DS(on)}$	Static-drain-source on-state resistance	$V_{GS} = -20$ V,	$I_D = -100\ \mu A$		140	200	Ω
$\lvert Y_{fs} \rvert$	Small-signal common-source forward transadmittance	$V_{DS} = -10$ V, f = 1 kHz	$V_{GS} = -10$ V,		3		mmho
$C_{(in)}$	Input capacitance (See Note 1)	$V_{DS} = -5$ V,	$V_{GS} = 0$ V		4	7	pF
$C_{(out)}$	Output capacitance (See Note 2)	$V_{SD} = -5$ V, f = 1 MHz	$V_{GS} = -5$ V,		13	20	pF
C_{gs}	Gate-source capacitance (See Note 3)	$V_{DS} = 0$ V, f = 1 MHz	$V_{GS} = 0$ V,		3	4.5	pF
C_{gd}	Gate-drain capacitance (See Note 3)	$V_{DS} = 0$ V, f = 1 MHz	$V_{GS} = 0$ V		2	3	pF
$t_{d(on)}$	Turn on delay time	See Switching Circuit			22	33	ns

NOTES: 1. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
2. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
3. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate, respectively, are connected to the guard terminal of the bridge.

ɔchanical data

The TMS 6000 JR is mounted in a 24-pin hermetically sealed dual-in-line package consisting of gold-plated metal, ceramic sandwich body, and gold-plated leads. The package is designed for insertion in mounting-hole rows of 0.600-inch centers.

tching characteristics

PARAMETER MEASUREMENT INFORMATION

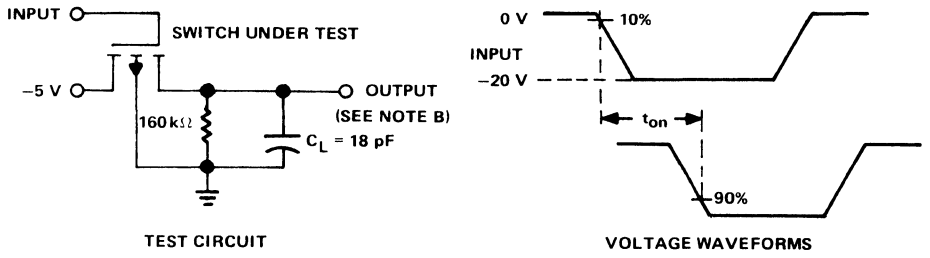


FIGURE 1

ES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.

B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

TYPICAL CHARACTERISTICS

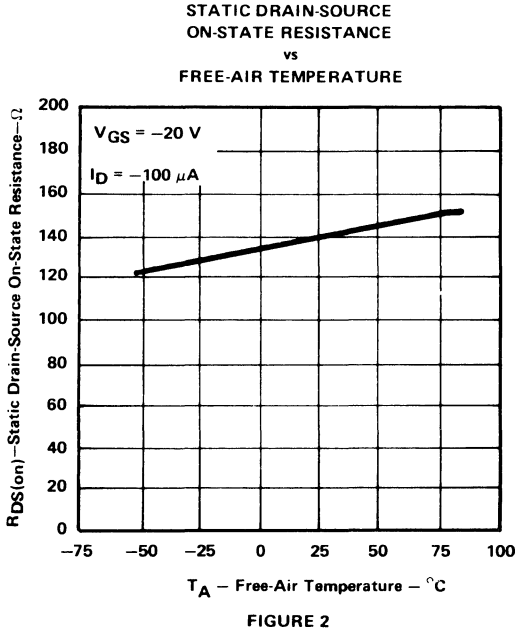


FIGURE 2

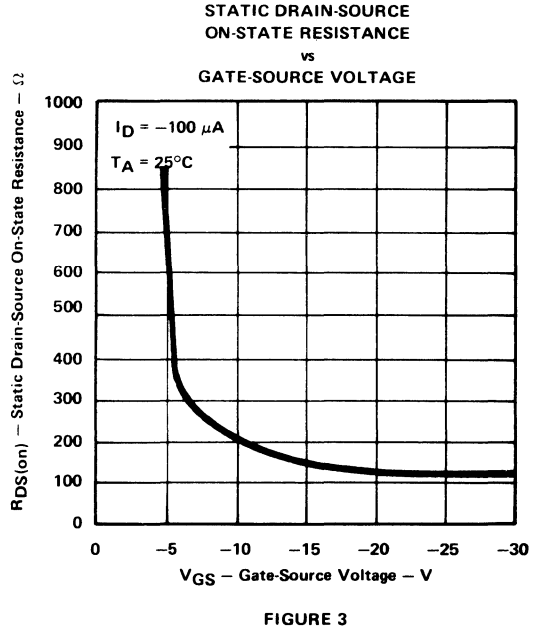
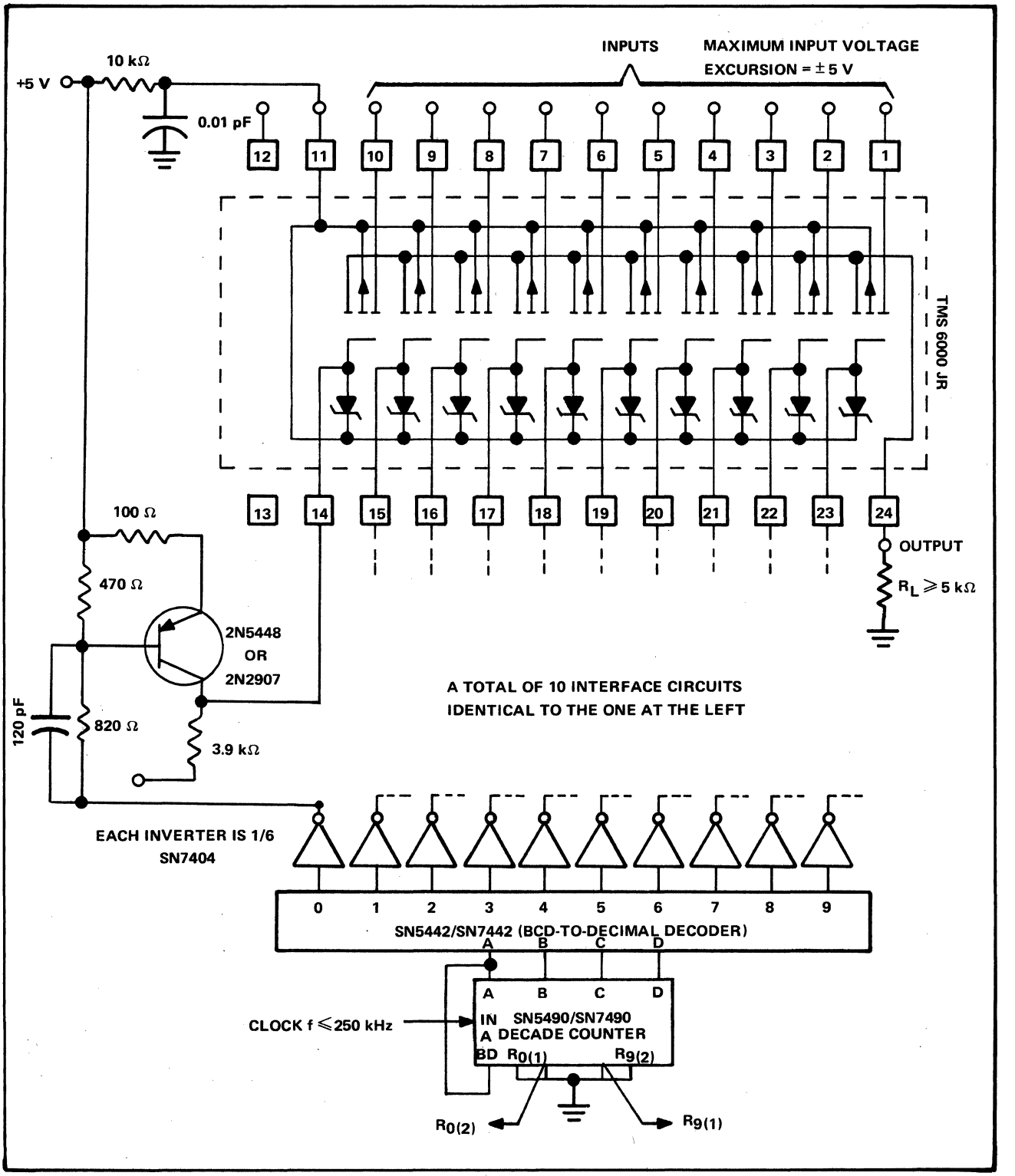


FIGURE 3

TYPICAL APPLICATION DATA

DIRECT-DOUPLED MULTIPLEXER ADDRESSED FROM SERIES 54/74 TTL



TYPICAL APPLICATION DATA (Continued)

In the above circuit, each input is sequentially connected through an MOS switch to an output circuit represented by load resistance R_L. A Series 54/74 TTL counter and decimal decoder are used to obtain sequential driving from a single clock.

An interface circuit using a p-n-p transistor translates TTL output voltage levels to those required by the MOS switch. In this circuit, +5 volts is used to turn the switch off, −20 volts is used to turn it on. Because the transistor saturates, a storage time exists which delays turn-off. This delay (about 150 to 300 ns) is used in the interface circuit shown to allow the previous MOS switch to turn off completely before the next one turns on. Clock frequency, f_{clock}, is limited by interface circuit storage and fall times to about 250 kHz before these times become an appreciable fraction of a clock cycle.

The substrate is biased at +12 V to allow the drains and sources of the MOS switches to go positive without forward-biasing the drain-substrate and source-substrate diffused diodes. Only leakage current flows into the substrate, so the simple R-C filter shown is sufficient to prevent noise from the +12 volt supply from interfering with switch operation.

TMS6002JR
six-channel analog switch
preliminary information

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

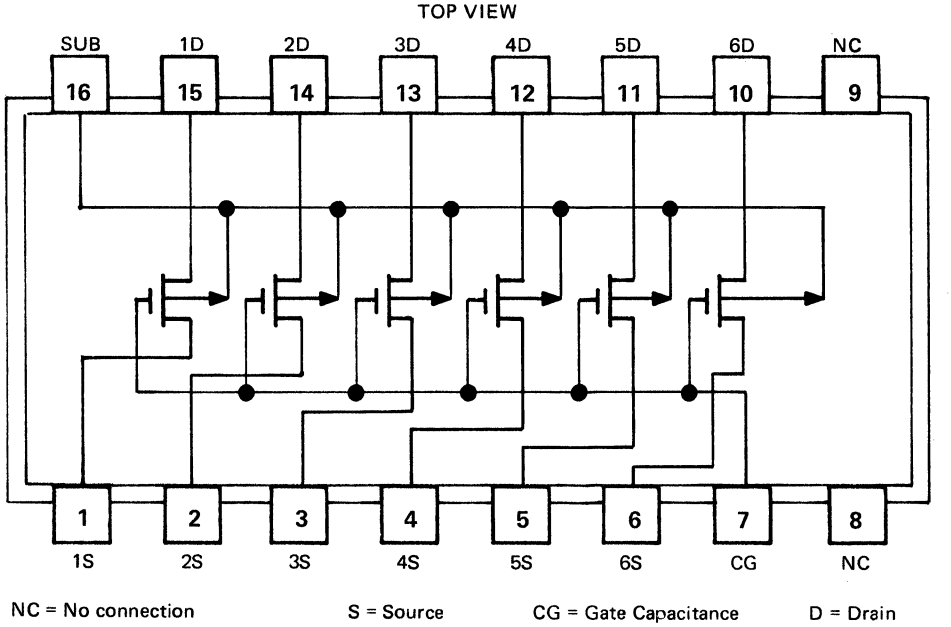
- Dual-in-line package
- $R_{DS(on)}$ . . . 200 Ω maximum

description

The TMS 6002 JR analog switch is a P-channel enhancement-mode MOS monolithic integrated circuit, utilizing thick-oxide technology. This general-purpose device consists of six MOS transistors having all six gates interconnected. The common gate is protected by a diode circuit and must be switched by an external driver. The analog switch is packaged in 16-pin dual-in-line ceramic package.

A gate input impedance greater than 10^{10} ohms, coupled with low source-cutoff current, zero inherent offset voltage, and low on-state resistance makes this switch ideally suited for time-division multiplexing of analog and digital signals.

schematic and pin configuration



NC = No connection S = Source CG = Gate Capacitance D = Drain

The material herein is believed to be accurate and reliable; however, some parameters specified are derived from evaluation units and may change slightly after full characterization.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Drain-source voltage	−30 V
Forward gate-source voltage (See Note 1)	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Gate-terminal reverse current (forward direction for zener clamp)	0.1 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2)	500 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTES: 1. Forward gate-source voltage is of such polarity that an increase in its magnitude above a threshold level causes the channel resistance to decrease.
2. Derate linearly to 85°C free-air temperature at the rate of 8.3 mW/°C.

electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$, $V_{GS} = 0$	−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0$	−30			V
I_{GSSF}	Gate-terminal forward current 6 gates	$V_{GS} = -20$ V, $V_{DS} = 0$		0.3	6.0	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V, $V_{GS} = 0$			3.0	nA
I_{SDS}	Zero-gate-voltage source current	$V_{SD} = -20$ V, $V_{GS} = 0$			6.0	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DG} = 0$, $I_D = -10\ \mu A$	−2.5	−4	−6	V
$R_{DS(on)}$	Static drain-source on-state resistance	$V_{GS} = -20$ V, $I_D = -100\ \mu A$		140	200	Ω
$\lvert y_{fs} \rvert$	Small-signal common gate forward transfer admittance	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 kHz		3		mmho
$C_{(in)}$	Input capacitance (See Note 3)	$V_{DS} = -5$ V, $V_{GS} = 0$, f = 1 MHz		4	7	pF
$C_{(out)}$	Output capacitance (See Note 4)	$V_{SD} = -5$ V, $V_{GS} = -5$ V, f = 1 MHz		4	7	pF
C_{gs}	Gate-source capacitance (See Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		3	4.5	pF
C_{gd}	Gate-drain capacitance (See Note 5)	$V_{DS} = 0$, $V_{GS} = 0$,		2	3	pF
t_{don}	Turn on delay time	See Switching Circuit		50	75	ns

NOTES: 3. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
4. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
5. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate or the source and substrate, respectively, are connected to the guard terminal of the bridge.

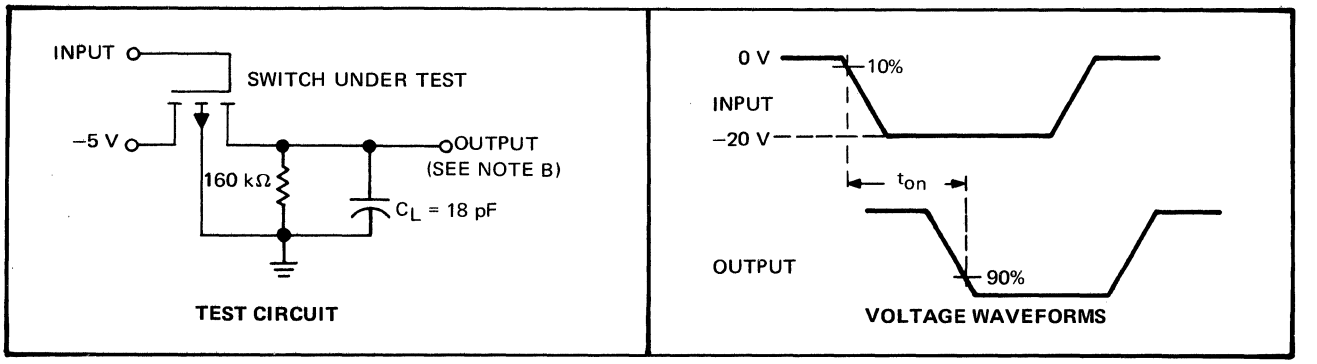
† The body (substrate) terminal is grounded to the reference terminal unless otherwise noted.

TMS6002JR

six-channel analog switch

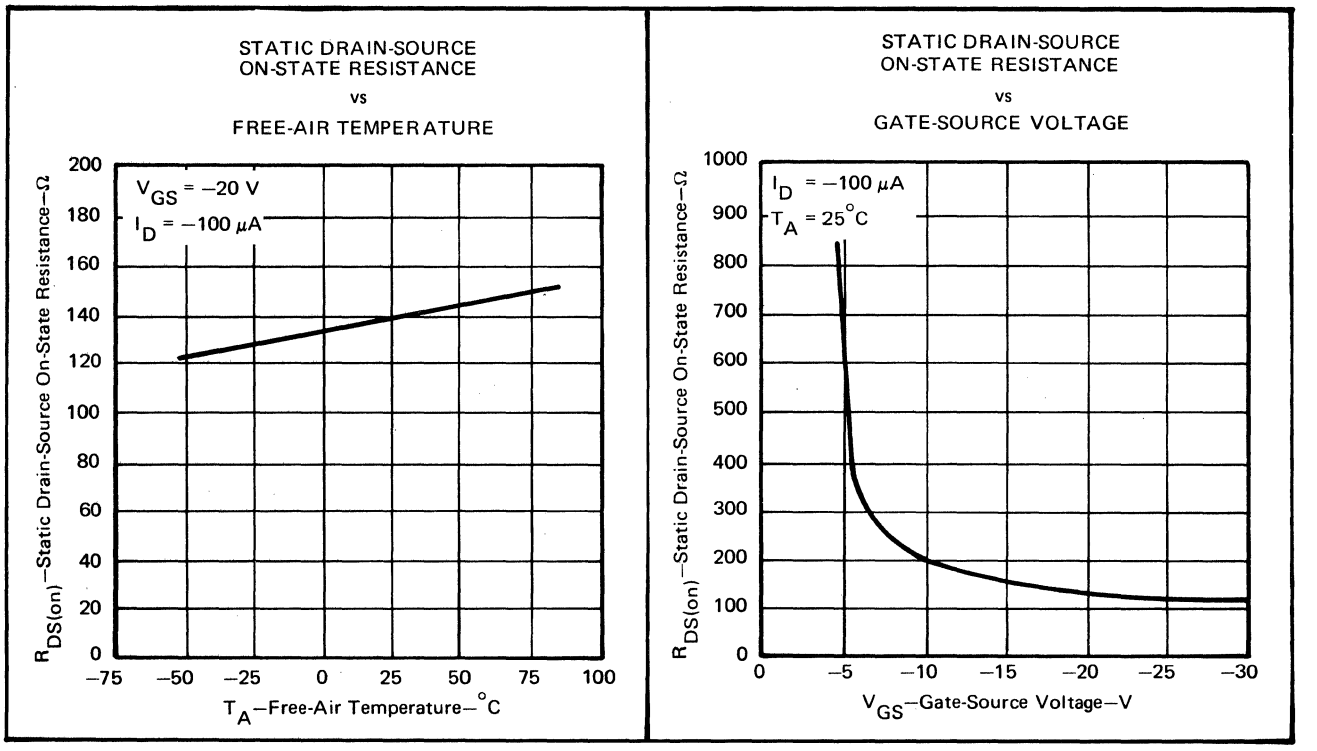
switching characteristics

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

TYPICAL CHARACTERISTICS



mechanical data

The TMS 6002 JR is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers.

TMS6005JR, TMS6009JR
six-channel analog switches

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-Line Package
- $r_{DS(on)}$ . . . 200 Ω Max

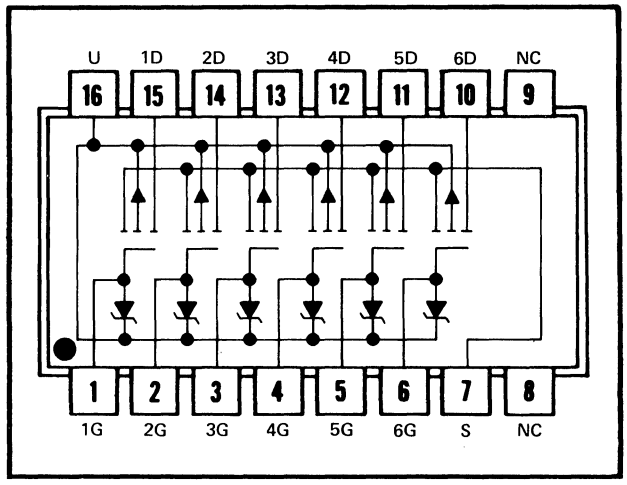
description

The TMS6005JR and TMS6009JR analog switches are P-channel enhancement-mode MOS monolithic integrated circuits utilizing thick-oxide technology. Each consists of six MOS transistors having all six sources interconnected. The gate of each MOS device is protected by a diode circuit and must be switched by an external driver. The analog switches are packaged in 16-pin dual-in-line ceramic packages.

The TMS6009JR is intended for applications requiring extremely low leakage currents. The TMS6005JR is a general-purpose device.

A gate input impedance greater than 10^{10} ohms coupled with low source cutoff current, zero inherent offset voltage, and low on-state resistance makes these switches ideally suited for time-division multiplexing of analog and digital signals.

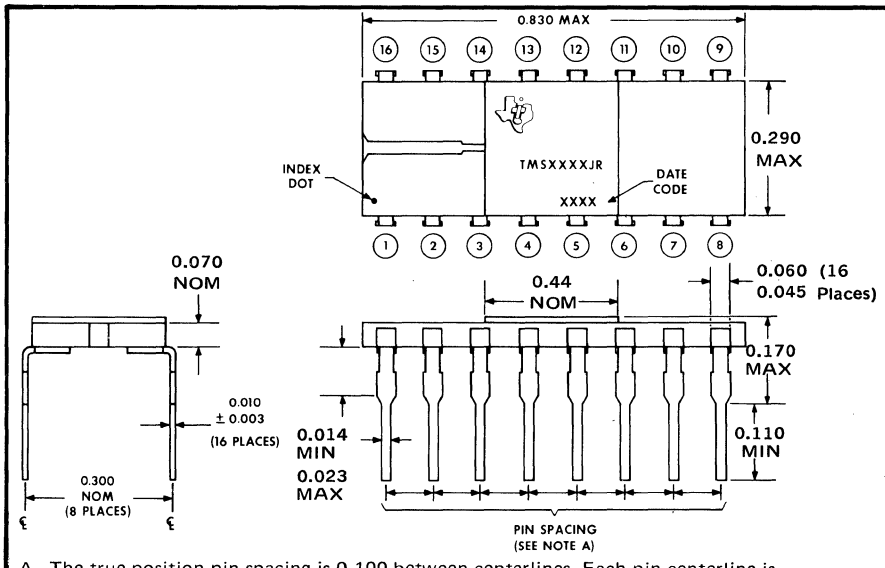
TOP VIEW



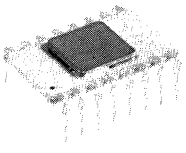
NC—No internal connection

mechanical data

The TMS6005JR and TMS6009JR are mounted in 16-pin hermetically sealed dual-in-line packages each consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers.



A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions are in inches.



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Drain-source voltage	−30 V
Forward gate-source voltage (see Note 1)	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Gate-terminal reverse current (forward direction for zener clamp)	0.1 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2)	500 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTES: 1. Forward gate-source voltage is of such polarity that an increase in its magnitude above a threshold level causes the channel resistance to decrease.
2. Derate linearly to 85°C free-air temperature at the rate of 8.3 mW/°C.

electrical characteristics at 25°C free-air temperature

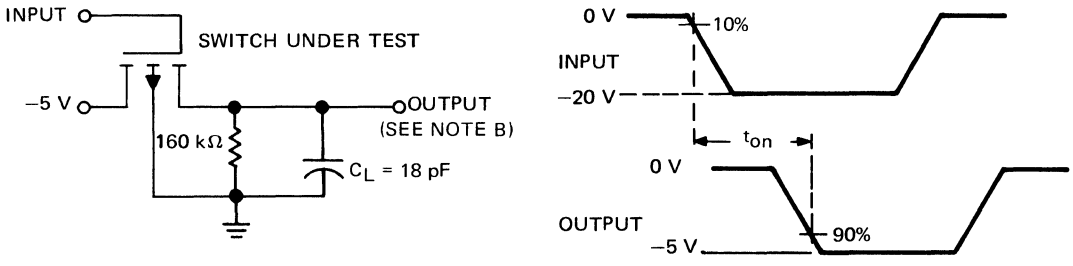
PARAMETER		TEST CONDITIONS†	TMS6005JR			TMS6009JR			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$, $V_{GS} = 0$	−30			−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−30			−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0$	−30			−30			V
I_{GSSF}	Gate-terminal forward current	$V_{GS} = -20$ V, $V_{DS} = 0$			−5		−0.05	−1	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V, $V_{GS} = 0$			−10			−3	nA
I_{SDS}	Zero-gate-voltage source current (total for six switches)	$V_{SD} = -20$ V, $V_{GD} = 0$			−30			−6	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DG} = 0$, $I_D = -10\ \mu A$	−2.5	−4	−6	−2.5	−4	−6	V
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{GS} = -20$ V, $I_D = -100\ \mu A$		140	200		140	200	Ω
$\lvert y_{fs} \rvert$	Small-signal common-source forward transfer admittance	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 kHz		3			3		mmho
$C_{(in)}$	Input capacitance (see Note 3)	$V_{DS} = -5$ V, $V_G = V_S = V_{SS}$ f = 1 MHz		4	7		4	7	pF
$C_{(out)}$	Output capacitance (see Note 4)	$V_{SD} = -5$ V, $V_G = V_S = V_{SS}$ f = 1 MHz		13	20		13	20	pF
C_{gs}	Gate-source capacitance (see Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		3	4.5		3	4.5	pF
C_{gd}	Gate-drain capacitance (see Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		2	3		2	3	pF
t_{on}	Turn-on time	See Figure 1		50	75		50	75	ns

NOTES: 3. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
4. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
5. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate or the source and substrate, respectively, are connected to the guard terminal of the bridge.

†The body (substrate) terminal is grounded to the reference terminal unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$. C_L includes oscilloscope input capacitance plus stray capacitance.

FIGURE 1

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

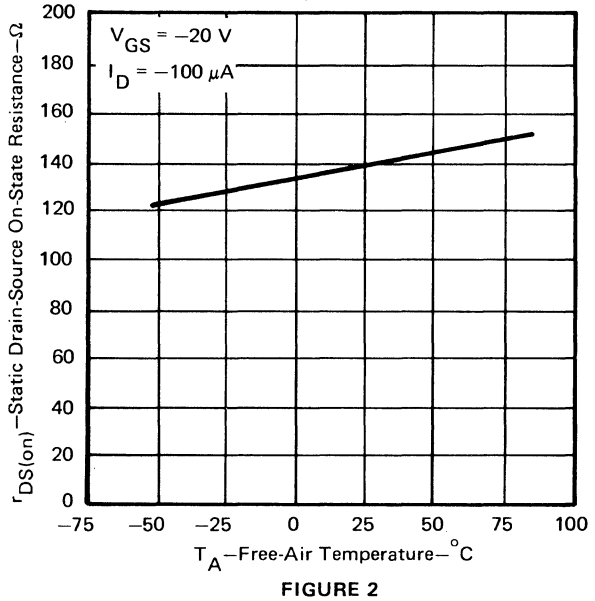


FIGURE 2

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs GATE-SOURCE VOLTAGE

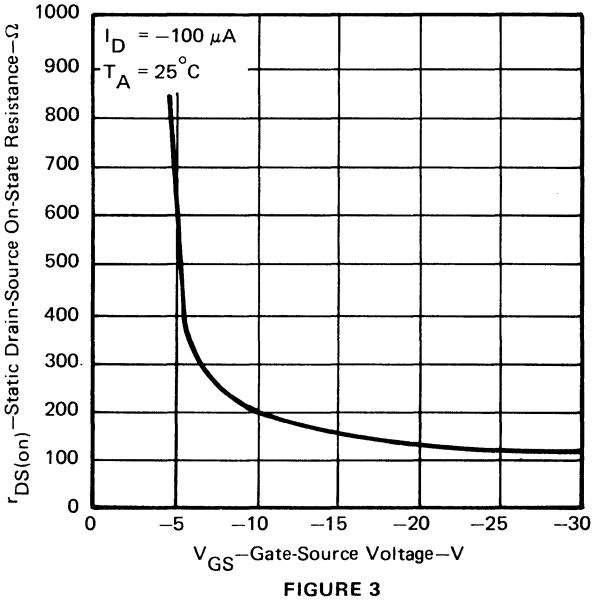
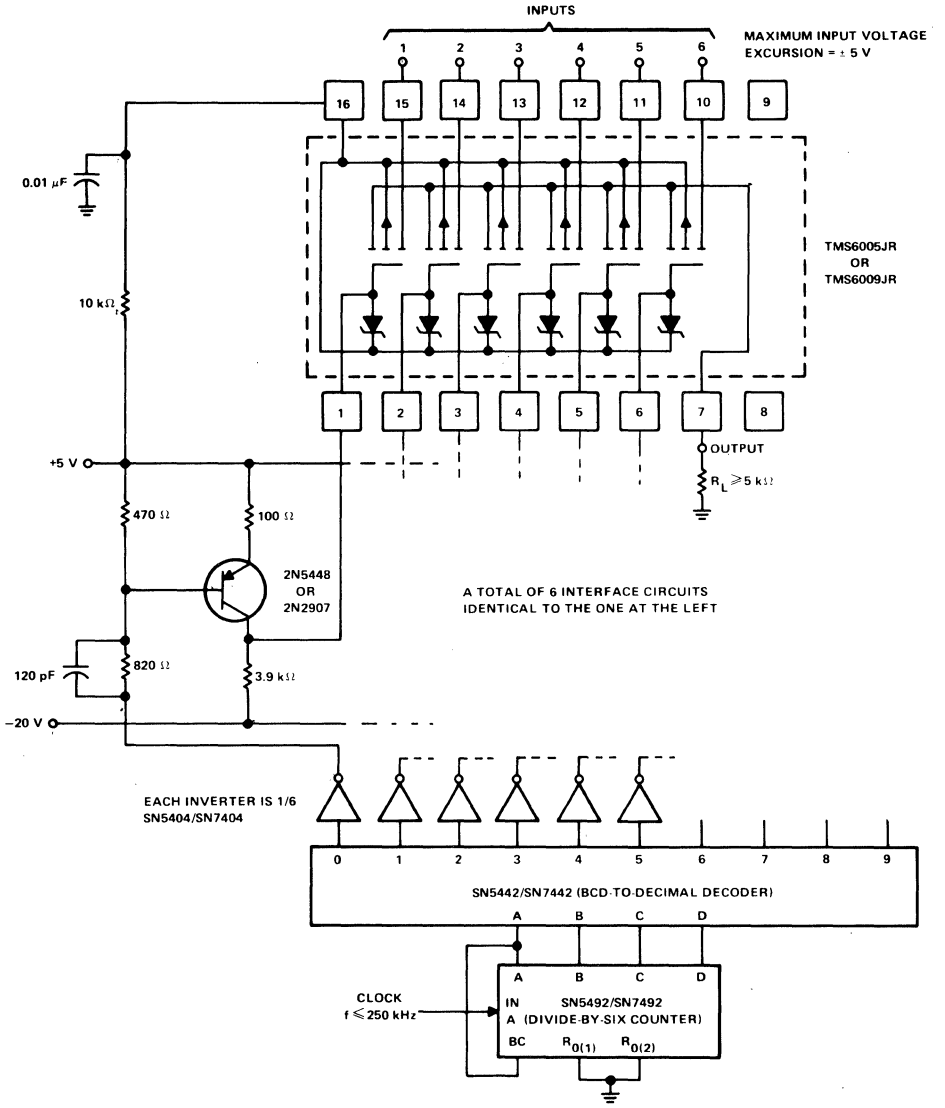


FIGURE 3

TYPICAL APPLICATION DATA

DIRECT-COUPLED MULTIPLEXER ADDRESSED FROM SERIES 54/74 TTL



In the above circuit, each input is sequentially connected through an MOS switch to an output circuit represented by load resistance R_L. A Series 54/74 TTL counter and decimal decoder are used to obtain sequential driving from a single clock.

An interface circuit using a p-n-p transistor translates TTL output voltage levels to those required by the MOS switch. In this circuit, +5 volts is used to turn the switch off, −20 volts is used to turn it on. Because the transistor saturates, a storage time exists which delays turn-off. This delay (about 150 to 300 ns) is used in the interface circuit shown to allow the previous MOS switch to turn off completely before the next one turns on. Clock frequency, f_{clock}, is limited by interface circuit storage and fall times to about 250 kHz before these times become an appreciable fraction of a clock cycle.

The substrate is biased at +5 volts to allow the drains and sources of the MOS switches to go positive without forward-biasing the drain-substrate and source-substrate diffused diodes. Only leakage current flows into the substrate, so the simple R-C filter shown is sufficient to prevent noise from the +5-volt supply from interfering with switch operation.

TMS3802LS
six-stage frequency divider
preliminary information

description

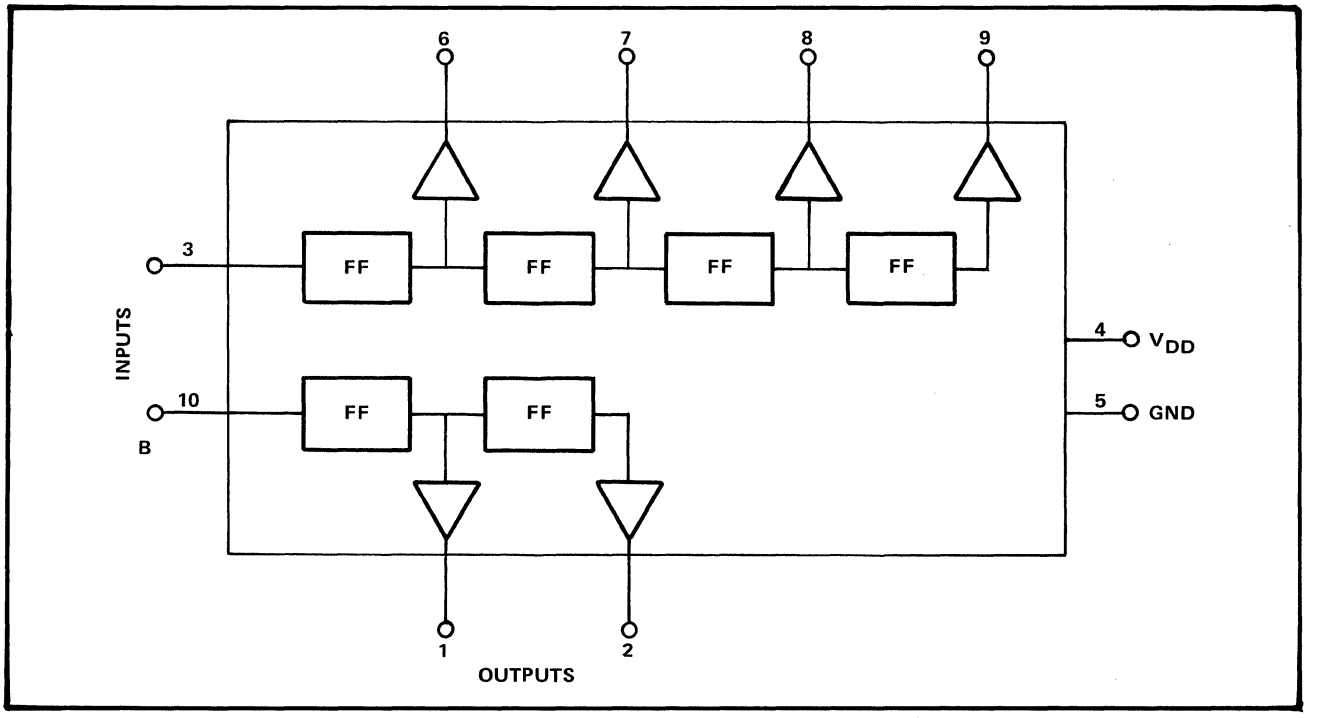
The TMS 3802 LS consists of six edge-triggered flip-flops with output buffers, and is particularly well suited for tone generation in electronic organs. The entire device is constructed on a single monolithic chip, using thick-oxide techniques and MOS P-channel enhancement-mode transistors.

operation

Four of the six flip-flops are connected in series to provide frequency division by 2, 4, 8 and 16, and the other two are connected in series to provide frequency division by 2 and 4.

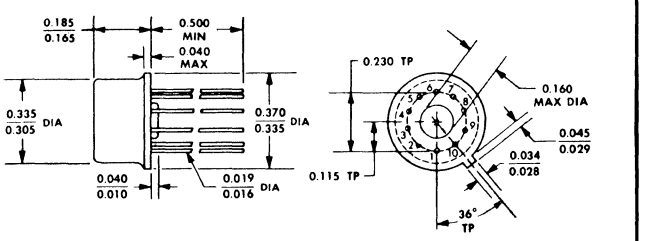
The circuit can be driven from any wave form if rise-time is not greater than 10 microseconds.

functional diagram



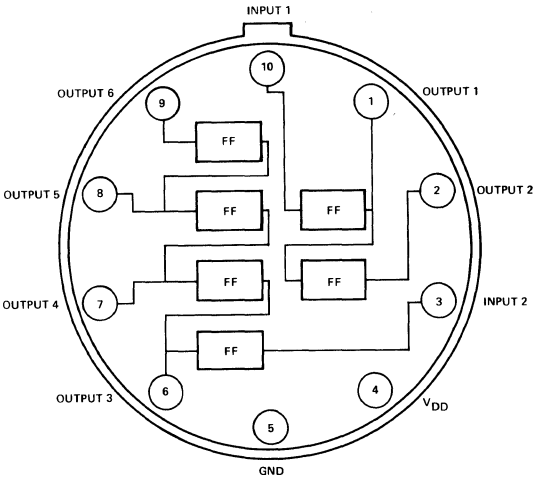
TMS3802LS
six-stage frequency divider

packaging



DIMENSIONS ARE IN INCHES
UNLESS OTHERWISE SPECIFIED

PIN 5 IS IN ELECTRICAL CONTACT WITH THE CASE



BOTTOM VIEW

NOTES: 1. All dimensions in inches.
2. Pin 5 is in electrical contact with the case.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 3) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 3) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −10°C to +55°C
Storage temperature range . . . . . −55°C to +100°C

NOTE 3. These voltage values are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply voltage V_{DD}	−26	−28	−29	V
Rise-time of input pulses (See voltage waveforms)			10	μsec
Fall-time of input pulses (See voltage waveforms)			10	μsec
Frequency-input pulses (Charge 10 kΩ, 10 pF to ground)	dc		100	kHz

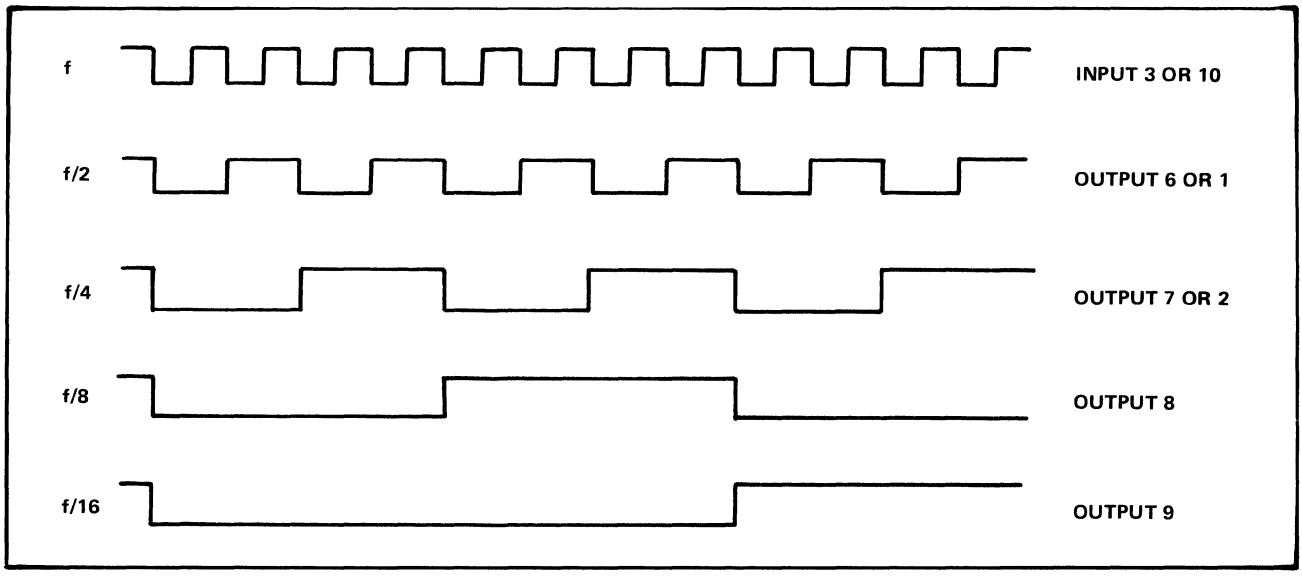
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{in(1)}$	Logical 1 input voltage		−9			V
$V_{in(0)}$	Logical 0 output voltage				−2.5	V
$V_{out(1)}$	Logical 1 output voltage	R load = 10 kΩ	−10	−13.5		V
$V_{out(0)}$	Logical 0 output voltage	I load = 1.5 mA		−1	−2	V
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −28 V				mA

switching characteristics T_A = +25°C, R_L = 10 kΩ, C_L = 20 pF

PARAMETER		TYP	UNITS
t_{pd}	Propagation delay time from input voltage to divide-by-two output	450	nsec
t_{pd}	Propagation delay time from input voltage to divide-by-16 output	1	μsec
t_{pd}	Propagation delay time from input voltage to divide-by-64 output	1.65	μsec

timing diagram



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MOS/LSI is very well suited for custom design:

High level of integration	*lower package count* *lower cost*
Two dimensional design	*easy simulation* *fast turnaround times*
Simple process	*high reliability* *low cost*

To respond to the large demand for MOS/LSI custom subsystems TI has geared its operations to handle hundreds of custom designs each year.

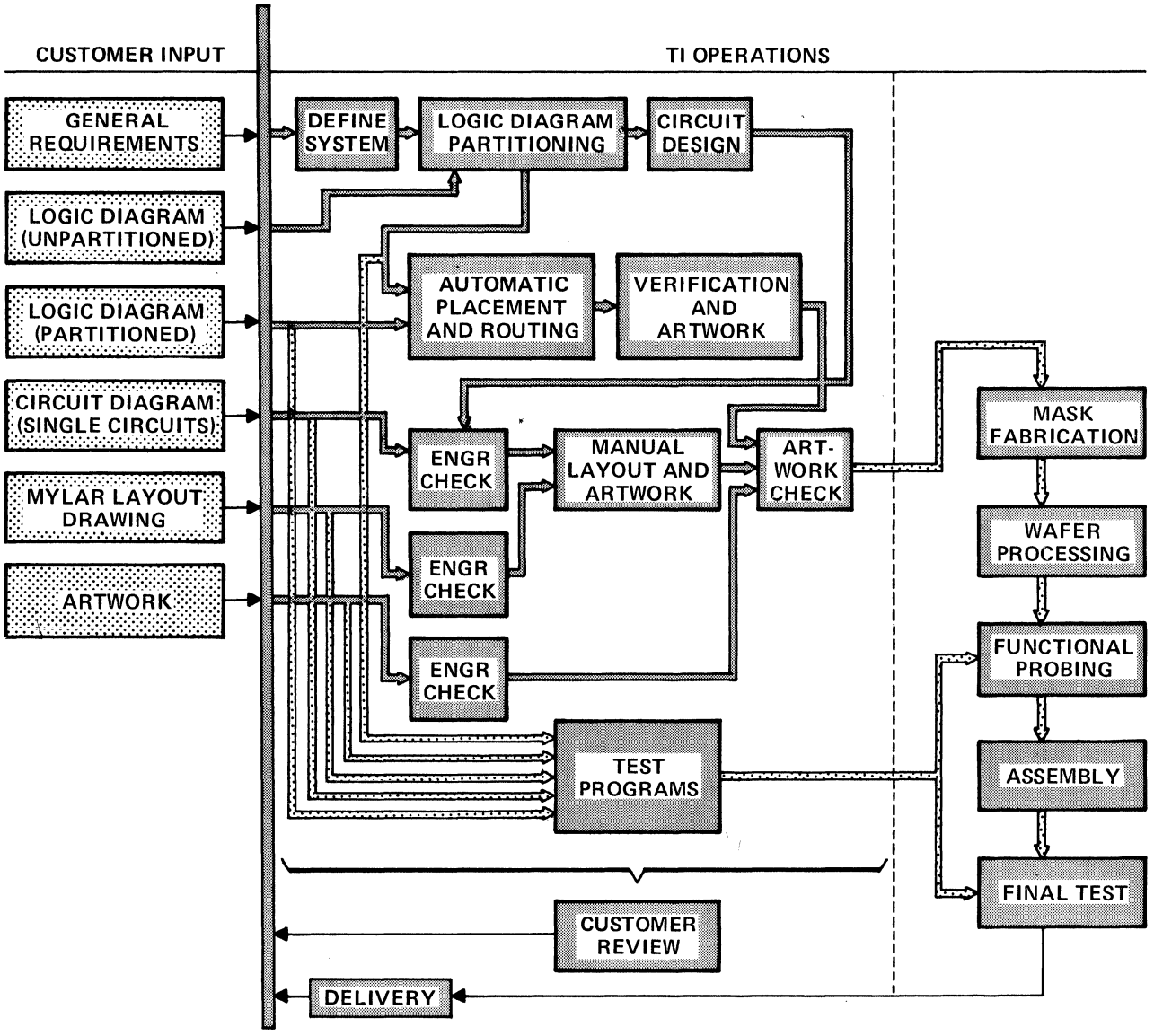
The level of complexity of MOS/LSI subsystems design is very high. Circuit designs are assisted by other specialists. A typical team approach to multichip system design will consist of

- Systems Engineers
- Circuit Designers
- Software Specialists
- Test and Reliability Engineers

In order to optimize design and minimize cost many computer programs have been developed. In a typical MOS/LSI multichip design the following computer aided design will be used to optimize the design:

- Subsystem simulation
- Circuit analysis
- Circuit simulation
- Automatic placement and routing (mask design)
- Manually assisted placement and routing (CRT implementation of mask design)
- Computer drawing
- Mask cutting
- Test pattern generation and grading

TI's involvement in custom MOS/LSI is complete. The TI-customer interface is very flexible. Inputs may range from general requirements ("Black Box" specifications) to finished working glass photo masks. Experience has shown that the best interface point is with partitioned logic diagrams; however, TI can also partition your logic diagrams or convert TTL/DTL implemented logic to MOS/LSI.



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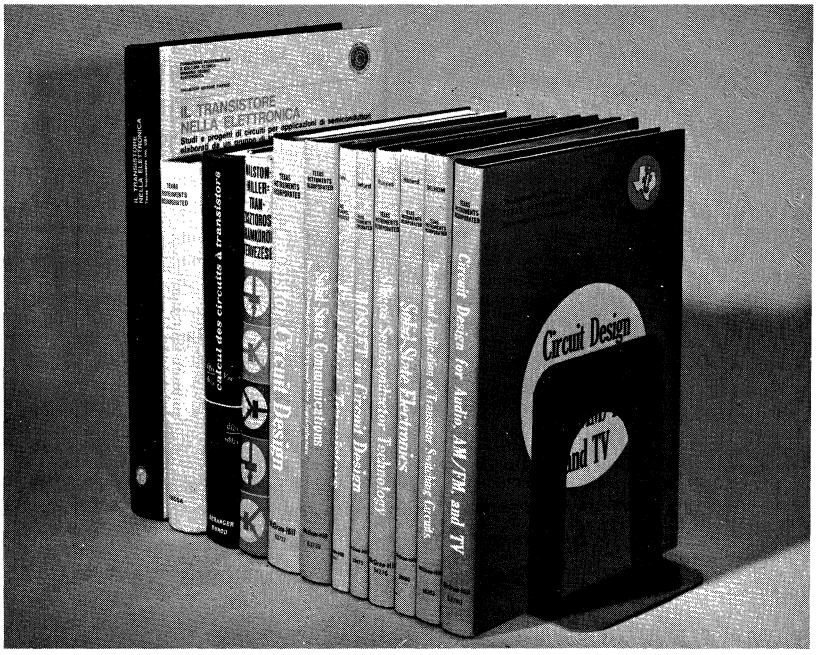

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Rua Cesario Alvim 770
Caixa Postal 30.103
Sao Paulo 6, Brasil
93-8278

CANADA

Texas Instruments Incorporated

663 Orly Avenue
Dorval (Montreal)
Quebec, Canada
631-6010

SF Caesar Avenue
Ottawa 12
Ontario, Canada
613-825-3716

280 Centre Str. East
Richmond Hill (Toronto)
Ontario, Canada
416-889-7373

DENMARK

Texas Instruments A/S

46D, Marielundvej
2730 Herlev, Denmark
91 74 00

FINLAND

Texas Instruments Finland OY

Fredrikinkatu 56, D.38
Helsinki 10, Finland
44 12 75

FRANCE

Texas Instruments France

379 Av de la Liberation
92 Clamart, France
644 55 30

30-31 Quai Rambaud
69 Lyon, France
42 78 50

3, Rue Lafayette
35 Rennes, France
30 56 85

20, Avenue Honore' Serres
31 Toulouse, France
62 82 85

GERMANY

Texas Instruments Deutschland GmbH

Arabellastrasse 4, Sternhaus/V
8000 Munchen 81, Germany
0811/91 10 61-9

Lazarettstr. 19
4300 Essen, Germany
2141/20916

Kuntzelstrasse 57
43 Essen, Germany
02141/86 10 16

Westendstrasse 52
6000 Frankfurt a.M., Germany
0611/72 64 41

Am Mittelfelde 169
3000 Hannover, Germany
0511/86 10 16

Im Kaisemer 5
7000 Stuttgart 1, Germany
0711/22 38 20

ITALY

Texas Instruments Italia SpA

Viale Lunigiana 46
20125 Milano, Italy
688 31 41

Via Val di Chiana 56
50127 Firenze, Italy
41 00 79

Via Padre Semeria
00154 Roma, Italy
512 36 10

Via Barbaroux 2
10122 Torino, Italy
54 06 93

MEXICO

Texas Instruments de Mexico S.A.

Poniente 116 #489
Col. Industrial Vallejo
Mexico City, D.F., Mexico
567-92-00

NETHERLANDS

Texas Instruments Holland N.V.

Entrepot Gebouw-Kamer 223
P. O. Box 7603
Schiphol-Centrum
020-15 92 93

UNITED KINGDOM

Texas Instruments Limited

165 Bath Road
Slough, Buckinghamshire, England
Slough 33411

2259 Coventry Road
Sheldon, Birmingham 26, England
021-743-5293

24 Rutland Street
Edinburgh EH1 2AN, Scotland
031-229-1481

York House, 12 York Street
Manchester 2, England
061-236-7282

46 F. Nichols Road
Southampton, Hants, England
0703-27267

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